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Current transport mechanisms and deep level transient spectroscopy of Au/n-Si Schottky barrier diodes

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ABSTRACT

The temperature-dependent electrical characteristics of the Au/n-Si Schottky diodes have been studied in the temperature range of 40–300 K. Current density–voltage (*J–V*) characteristics of these diodes have been analyzed on the basis of thermionic emission theory with Gaussian distribution model of barrier height. The basic diode parameters such as rectification ratio, ideality factor and barrier height were extracted. Under a reverse bias, the conduction process at low voltage is determined by Schottky emission over a potential barrier but at higher voltage the Poole Frenkel effect is observed. The capacitance–voltage (*C–V*) features of the Au/n-Si Schottky diodes were characterized in the high frequency of 1 MHz. The barrier heights values obtained from the *J–V* and *C–V* characteristics have been compared. It has been seen that the barrier height value obtained from the *C–V* measurements is higher than that obtained from the *J–V* measurements at various temperatures. Possible explanations for this discrepancy are presented. Deep level transient spectroscopy (DLTS) has been used to investigate deep levels in Au/n-Si. Three electron trap centers, having different emission rates and activation energies, have been observed. It is argued that the origin of these defects is of intrinsic nature. A correlation between *C–V* and DLTS measurements is investigated.

1. Introduction

It is well known that Schottky contacts have an important role for electronic technology [1,2]. Metal–semiconductor (MS) contact is one of the most widely used rectifying contacts in electronic industry [3,4]. Electronic properties of a Schottky diode (SD) are characterized by its barrier height and ideality factor parameters. The interface states play an important role on determination of Schottky barrier height and other characteristic parameters and these can affect device performance, stability and reliability [5,6]. The performance and stability of MS structures is of vital importance to all electronic and optoelectronic devices [7,8].

Many researchers have attempted to understand the physical parameters of Schottky barrier diodes. Yu and Mead [9] have reported the characteristics of Al/n-type silicon Schottky. They found that the *I–V* characteristics agree well with the theoretical thermionic emission model. The properties of d.c. sputtered molybdenum–silicon Schottky diodes (SD) are described by Mullins and Brunnschweiler [10]. They proposed a model which is capable of explaining most features of the observed *C–V* and *I–V* characteristics. Current-transport properties of Al/n-p Si (SD) have been studied both experimentally and theoretically by Wu et al. [11]. They proposed an analytical model for the *I–V* characteristic of a metal–n–p that has been developed by using an interfacial layer-thermionic-diffusion model. Keffous et al. [12] have investigated the current–voltage characteristics of the effect of series resistance on the non-ideal silicon Schottky diode (SSD) of two types of diodes: Al/n-Si and Au/n-Si, with high resistivity silicon bulk. The parameter R_s, the ideality factor n and the barrier height Φ_b are determined by performing different plots from the forward *I–V* characteristics. Siad et al. [13] have reported the investigation of series resistance on the Al/n-Si and Al/p-Si non-ideal Schottky diode, in their process fabrication. The comparison between Au/n-Si and Ag/n-Si Schottky photodiode were presented by Keffous et al. [14]. The silicon Schottky photodiodes were realized by thermal deposition of a thin metal layer (gold (Au) and silver (Ag)) on n-type Si (111). They introduced a current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements to determine the diode parameter. A mechanism of local lowering of the Schottky barrier height (SBH) is proposed by Maeda [15], which causes non-ideality in nearly ideal Au/*n*-Si and Au/*n*-GaAs Schottky barriers. He suggested that the thermionic-field emission current taking place in the strong electric field has influence on the *I–V* characteristics at low temperatures. He also reported the *C–V* characteristics of Au/Si SD, which observed an extra capacitance under the forward bias.

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The electrical properties of the Cr/p-Si and Cr/n-Si Schottky diodes were investigated by Tatar et al. [16] through capacitance–voltage and current–voltage measurements, performed under dark and light conditions at room temperature. Diode parameters of Cr/n-Si SD like ideality factor and barrier height were obtained and variations of them were monitored as a function of temperatures. Also, an attempt to explore the governing current flow mechanism was tried. Electrical properties of Ta/n-Si and Ta/p-Si Schottky barrier diodes obtained by sputtering of tantalum (Ta) metal on semiconductors have been investigated by Ocak et al. [17]. The characteristic parameters of these contacts like barrier height, ideality factor and series resistance have been calculated using *I–V* measurements.

Ion implantation is a well-characterized and widely used technique for the introduction of impurities (dopants) into semiconductors and offers more flexibility than diffusion [18,19]. In ion implantation, dopant atoms are volatilized, ionized, accelerated, separated by the mass-to-charge ratios, and directed at a target that is typically a silicon substrate [19]. The atoms enter the crystal lattice, collide with the host atoms, lose energy, and finally come to rest at some depth within the solid [18,19]. The primary defects in any energetic bombardment of crystalline semiconductors are vacancies and interstitials, a large percentage of which have been shown theoretically [20] and experimentally [21] to recombine with each other. Others escape the recombination process, and migrate until forming complexes either with themselves or with other defects. Pellegrino et al. [22] showed that the situation is indeed different in the case of defects caused by ion implantation. The study of these is very important because defects caused by ion implantation have far-reaching consequences. Various charge states of the defects can be detected by techniques such as Deep Level Transient Spectroscopy, DLTS [22,23].

The DLTS is an experimental tool for studying electrically active defects (known as charge carrier traps) in semiconductors [24,25]. This establishes fundamental defect parameters and measure their concentration in the material. Some of the parameters are considered as defect "finger prints" used for their identifications and analysis. It has also investigates defects present in a space charge (depletion) region of a simple electronic device. The most commonly used are Schottky diodes or p–n junctions [24–26].

Moreover, DLTS technique has a higher sensitivity than almost any other semiconductor diagnostic technique. For example, in silicon it can detect impurities and defects at a concentration of one part in 10^{12} of the material host atoms. This feature together with a technical simplicity of its design made it very popular in research labs and semiconductor material production factories [24–26].

Very often the interpretation of impurity-defect reactions is based on identification of electronic levels observed by DLTS [27,28]. To identify them, several features have to be taken into account, in particular the trap parameters determined from the temperature dependence of emission rate [27,28].

However, the fundamental physical mechanisms that determine SD parameters such as ideality factor n and the barrier height (BH) Φ_b are still not fully understood. The cause of popularity of such studies, which is rooted in their importance to the semiconductor industry, does not assure uniformity of the results or of interpretation.

In the present work, we have investigated the temperature-dependent *J–V* and *C–V* characteristics of Au/n-Si SD in the temperature range of 40–300 K. The forward bias *J–V–T* measurements are used to explain the current transport mechanism and inhomogeneity in the barrier and to estimate the SD parameters. Also, the temperature dependence of SBH characteristics of the SDs are interpreted based on the existence of the Gaussian distribution, GD of the BHs around a mean value due to the BH inhomogeneities prevailing at the metal/semiconductor interface. Moreover, DLTS has been applied at different emission rates in n-type silicon implanted with low doses of silicon to measure the activation energies of deep levels of Au/n-Si Schottky diodes.

2. Experimental

The starting materials used in this work were single-crystal phosphorus doped Czochralski silicon with electron concentrations of 2×10^{15} cm^{-3} and a resistivity between 2.5 and 3.5 Ω cm. The implantation with Si^+ ions with energy of 850 keV and doses of 1×10^{10} cm^{-2} was carried out. This dose was chosen to ensure that there was a minimum of carrier removal due to deep defect states after implantation. Implants were carried out at 7° off axis to avoid channeling effects and after the predicted ion ranges had been calculated using the freely available modelling tool transport of ions in matter (TRIM). After implantation, aluminium Ohmic contacts were evaporated on the rear face, and gold Schottky contacts on the front face. *C–V* and *I–V* measurements were carried out to determine the diode integrity, and also to check that the depletion region could be swept through the implanted region. DLTS experiments were then carried out to characterize the deep levels present. The selection of the temperature is dictated by the original DLTS measurement, i.e. a temperature is chosen at which there is a peak in the DLTS spectrum. A plot of a peak intensity as a function of emission rate is produced, and the area under each peak is proportional to the concentration of the deep level with that emission rate. In all our measurements the voltage range was chosen to ensure that the region of the interstitial rich near the tail of the implant was studied. The precise voltages required were fixed by a comparison of TRIM simulation calculations with *C–V* measurements.

3. Results and discussion

3.1. Current density–voltage characteristics of Au/n-Si diode

The typical semilog-current density–voltage (*J–V*) characteristics of the Au/n-Si Schottky diodes measured in the temperature range 40–300 K are illustrated in Fig. 1. It is observed that the characteristics of Au/n-Si Schottky diodes are uniform over different diodes. As can be seen from the figure, the device has a good rectifying property. The simple thermionic emission theory can be used

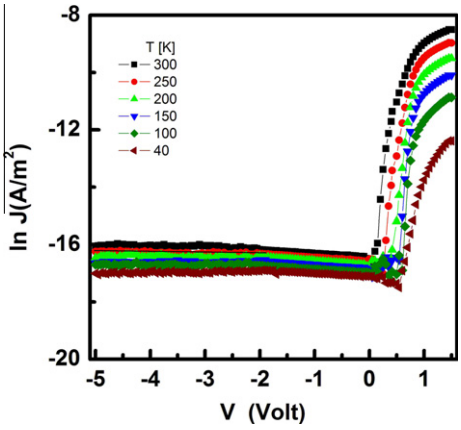

Fig. 1. ln *J–V* characteristics of Au/n-Si/Al Schottky diode in the temperature range 40–300 K.

to obtain the electrical properties of the Au/n-Si Schottky diodes. According to the theory, provided that the effect of minority carriers on the $V > 3kT/q$ region are ignored, thermionic emission (TE) model is valid. This theory suggests that J–V relationship is hold by the following relation [5,6],

$$J = J_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \quad (1)$$

where J_0 is the saturation current and it is defined by

$$J_0 = A^* T^2 \exp\left(-\frac{q\Phi_b}{kT}\right), \quad (2)$$

where A^* is the effective Richardson constant, T is the temperature in Kelvin, k is Boltzmann constant and q is electronic charge. The zero bias barrier height Φ_b can be obtained using Eq. (2)

$$\Phi_b = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right) \quad (3)$$

J_0 is obtained from the intercept of the linear extrapolation of the forward J–V curve at zero voltage.

The ideality factor n presents how closely the diode follows the ideal diode equation and can be determined from the slope of the linear region of the semi-log forward bias J–V characteristics using Eq. (1). The ideality factor n can be written in the form

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln J}\right) \quad (4)$$

The high n values for the Au/n-Si SD indicate that the J–V plots exhibit departures from the ideal thermionic behavior. According to the literature, most diodes show deviations from the ideal thermionic model. The non-ideal J–V characteristics might indicate there is intimate contact between Au and n-Si. Except to the experimental errors the influence of several other factors can cause such deviation from ideality, for example, the presence of interface layer, interface states and variation in the surface charge [29].

Fig. 2 shows the temperature dependence of the ideality factor n and the zero bias barrier height Φ_b of Au/n-Si Schottky diodes. Such behavior for the ideality factor and the barrier height have been attributed to the particular distribution of the interface states or an alternative approach to the lateral inhomogeneities that are found in the Schottky barrier interfaces, i.e. the Schottky barrier consisted of laterally inhomogeneous patches of different barrier heights. The patch with lower barrier height yields a larger ideality factor and vice versa. It is observed that the deviations in the ideality factor and barrier height may be due to spatially inhomogeneous barrier height and the potential fluctuations at the interface that consist of the low and high barrier heights [30–33], i.e. the current through the diode will flow preferentially through the lower barriers in the potential distribution. The current transport across the metal/semiconductor interface is a temperature activated process; at low temperatures, the current transport will be dominated by the current flowing through the patches of lower SBH and a larger ideality factor [30–32].

The large variation in ideality factor and zero bias barrier height values cannot be analyzed using the ideal thermionic emission model. Thus, the decrease in the zero bias barrier height and increase in ideality factor with a decrease in temperature have been successfully explained on the base of a thermionic emission mechanism with Gaussian distribution of the barrier heights, due to the barrier height inhomogeneities prevailing at the Au/n-Si interface [34,35].

Fig. 3 shows the plot of the zero bias barrier height versus the ideality factor of Au/n-Si Schottky diodes derived at each temperature. As illustrated, the zero bias barrier height becomes smaller as the ideality factors increase. That is, there is a linear relationship between the zero bias barrier height and ideality factor of Schottky contacts that can be explained by lateral inhomogeneities of the BH in Au/n-Si SD [35]. A laterally homogeneous BH value of approximately 0.91 eV for the Au/n-Si SD, was obtained from the extrapolation of the linear relationship between experimental effective BHs and ideality factors to $n = 1$. This inhomogeneity model is based on small local regions or patches with lower BH than the junction's main BH were assumed to exist at the junction. The reason of low Φ_b and high n values may be explained by the patch density. As well-known, the ideality factor, n and the zero bias barrier height, Φ_b depend on the patch density. As one might intuitively expect, the larger the patch density, thus the larger the respective ideality factor. This finding and assumption that the patches have smaller barrier heights than the homogeneous contact explains the experimentally observed reduction of the barrier heights with increasing ideality factors [30–32].

The barrier inhomogeneities are very important explanation of the higher values of the ideality factor. In order to analyze the barrier height inhomogeneities, such as Gaussian and log-normal, various types of distribution functions are suggested [34]. To explain the commonly observed abnormal deviation from classical TE theory, some authors [31,36] have considered a system of discrete regions or patches of low barrier imbedded in a higher background uniform barrier. This abnormal behaviors can be explained by assuming a Gaussian distribution, GD of the BH with a mean value Φ_b and standard deviation σ, which can be given as

$$P(\Phi_b) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{(\Phi_b - \Phi_m)^2}{2\sigma^2}\right], \quad (5)$$

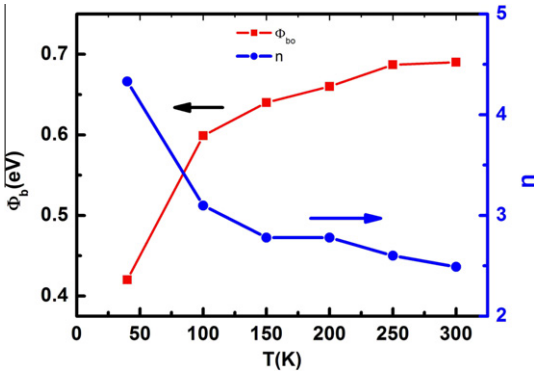

Fig. 2. Temperature dependence of the barrier height and ideality factor.

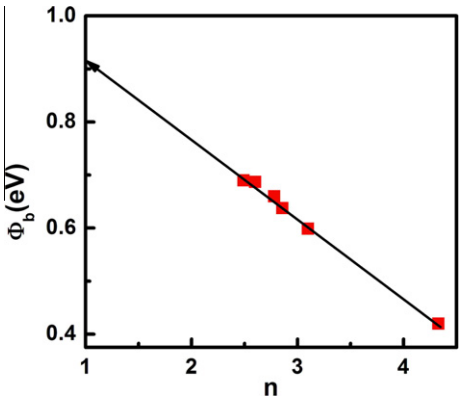

Fig. 3. Barrier height Φ_b vs. ideality factor n.

where $1/\sigma\sqrt{2\pi}$ is the normalization constant of the Gaussian BH distribution. σ is the standard deviation, Φ_b is the barrier height and Φ_m is the mean barrier height. The total current density, $J(V)$ across a Schottky diode, SD containing barrier inhomogeneities can be expressed as

$$J(V) = \int_{-\infty}^{+\infty} J(\Phi_b, V) P(\Phi_b) d\Phi, \tag{6}$$

where $P(\Phi_b)$ corresponds to the normalization constant. The total current density is determined after integrating through the Schottky contact is given by

$$J(V) = A^* T^2 \exp\left[-\frac{q}{kT}\left(\Phi_m - \frac{q\sigma}{2kT}\right)\right] \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{7}$$

The Gaussian distribution is affected by the bias and distribution parameters are defined as $\sigma = \sigma_0 + \rho_3 V$, here σ_0 and ρ_3 are standard deviation of the barrier height at zero-bias and voltage coefficient, respectively. The Gaussian distribution of the apparent barrier height and variation of the ideality factor with temperature are expressed by the following relations [37]

$$\Phi_a = \Phi_b - \frac{q\sigma_0^2}{2kT} \tag{8}$$

and

$$\left(\frac{1}{n_a} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT}, \tag{9}$$

where Φ_a is the apparent barrier height, n_a is the apparent ideality factor, ρ_2 and ρ_3 are voltage coefficients, which may depend on temperature, quantifying the voltage deformation of the barrier height distribution [37].Thus, the plot of Φ_a versus $1/2kT$ (Fig. 4) should be a straight line which gives Φ_m and σ_0 from the intercept and slope respectively. The values of Φ_m and σ_0 were found to be 0.72 eV and 4.2 meV, respectively. The values of ρ_2 and ρ_3 were determined from the intercept and the slope of the plot $\frac{1}{n_a} - 1$ vs. $1/2kT$ (Fig. 4). The obtained values of ρ_2 and ρ_3 were found to be 0.59 and 1.27 meV, respectively.

Fig. 5 shows typical reverse bias J–V characteristics as a function of temperature, plotted in the form of $\ln J$ vs. $V^{1/2}$. The current densities, under a reverse bias, were considerably lower than those for a forward bias. It can be seen from this figure that there are two distinct regions for each characteristic, which may be interpreted in terms of either the Schottky effect or the Poole–Frenkel effect (field-assisted thermal detrapping of carriers). The J–V expressions for these processes are given by [38]

$$J = A^* T^2 \exp\left(\frac{\Phi_s}{kT}\right) \exp\left(\frac{\beta V^{1/2}}{kTd_s^{1/2}}\right) \tag{10}$$

For the Shottky effect and

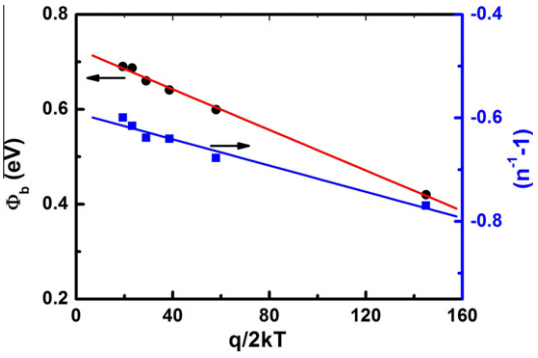

Fig. 4. Barrier height Φ_b and $(n^{-1}-1)$ vs. q/2kT.

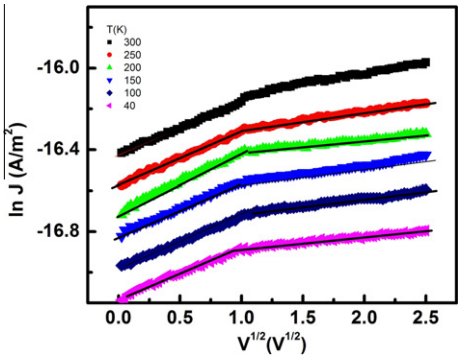

Fig. 5. Reverse bias ln J–$V^{1/2}$ characteristics at different temperatures.

$$J = J_{LF} \exp\left(\frac{\beta_{PF} V^{1/2}}{kTd_s^{1/2}}\right) \tag{11}$$

For the Poole–Frenkel effect, where A is the Richardson constant, Φ_s is the Schottky depletion height, J_{LF} is the lower-field current density, and β_s and β_{PF} are the respective Schottky and Poole–Frenkel field-lowering coefficients. Theoretical values of these coefficients are given by

$$2\beta_s = \beta_{PF} = \left(\frac{e^3}{\pi\varepsilon\varepsilon_0}\right)^{1/2} \tag{12}$$

This gives $\beta_s = 1.10 \times 10^{-5}$ and $\beta_{PF} = 2.20 \times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$ using $\varepsilon = 11.8$ [9]. Using the d_s value of 100 nm, obtained from the capacitance measurement, the mean values of β calculated from the slopes of Fig. 5 can be obtained and were found to be 2×10^{-6} and 1×10^{-6} eV m$^{1/2}$ V$^{-1/2}$ for the lower and higher voltage regions, respectively. The obtained values are at variance with that expected for the Schottky or Poole–Frenkel effect for β_s and β_{PF}. This difference may be attributed to a thermally assisted tunneling field emission of carriers occurring at the peak of the barrier where the effective barrier width is very narrow [39].

Alternatively, other workers [40,41] have explained this difference in terms of Schottky depletion region extending only in a distance d_s and not across the entire Si side.

Analysis of the temperature dependence of ln J–$V^{1/2}$ curves in the lower voltage region yields a mean value of the barrier height as $\Phi_s = 0.81$ eV, which is in good agreement with the value of the barrier height Φ_b derived previously from Fig. 2, thus providing further experimental evidence for the Schottky effect for the lower voltage region.

3.2. Capacitance–voltage characteristics of Au/n-Si Schottky diode

For metal/semiconductor devices, the capacitance measurement is one of the most important non-destructive methods for obtaining information on rectifying contact interfaces [42]. The capacitance–voltage characteristics of the studied diode were performed at a sufficiently high frequency of 1 MHz, because the interface state charges at this high frequency do not contribute to the capacitance of the diode. This will occur when the time constant is too long to permit the charge to move in and out of the interface states in response to an applied signal [43,35].

The dark capacitance–voltage characteristics have been analyzed using the depletion capacitance equation for SBD's as follows [5,6]

$$C = \frac{\varepsilon}{W_d} = \sqrt{\frac{q\varepsilon N_d}{2(V_{bi} - V - V_T)}}, \tag{13}$$

where C is the diode capacitance per unit area, N_d is the donor concentration, V_T is the thermal voltage (= k_BT/q), V is the applied bias, W_d is the depletion width and V_{bi} is the built-in voltage which is related to the barrier height Φ_b by the

$$\Phi_b = V_{bi} + V_T \ln\left(\frac{N_c}{N_d}\right) \tag{14}$$

N_c is the effective density of states at the conduction band.

The C–V results for the SD plotted as $1/C^2$ versus V gives a straight line in the all temperature range whose slope has been used to calculate the carrier concentration (N_d) values.

Fig. 6 shows the reverse bias C^{-2}–V characteristics of Au/n-Si/Al SBDs at 1 MHz, in the temperature range 40–300 K. The C^{-2}–V plots are linear for the whole temperature range. This indicates a constant donor concentration in the depletion layer and absence of metal–semiconductor interaction. Furthermore, the linear behavior of the curves can be explained the fact that the interface states and the inversion layer charge can not follow the a.c. signal at 1 MHz and consequently do not contribute appreciably to the diode capacitance [44].

Fig. 7 presents the built-in voltage and barrier height versus temperature, obtained from the C–V characteristics using Eq. (13). The built-in voltage and barrier height extracted from the C–V measurements increase slowly with decreasing temperature, in contrast to the J–V measurements. Therefore, there is more current at low temperature than predicted by thermionic emission theory and the results of the C–V measurements. From Fig. 7, the barrier height Φ_b values extracted from the C–V measurements are seen to be higher than those derived from the J–V measurements. This discrepancy could be explained by the existence of excess capacitance at the structure due to the interfacial layer or trap states in the semiconductor, the existence of the barrier inhomogeneity offers another explanation [37]. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise, they will yield different values.

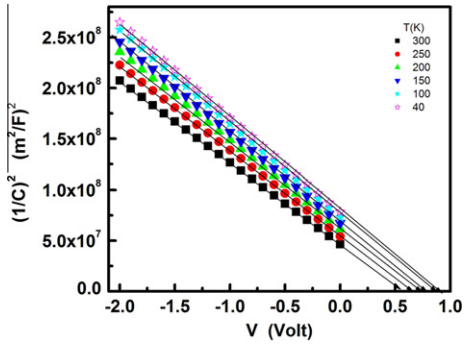

Fig. 6. Reverse bias $1/C^2$–V characteristics of Au/n-Si/Al Schottky diode.

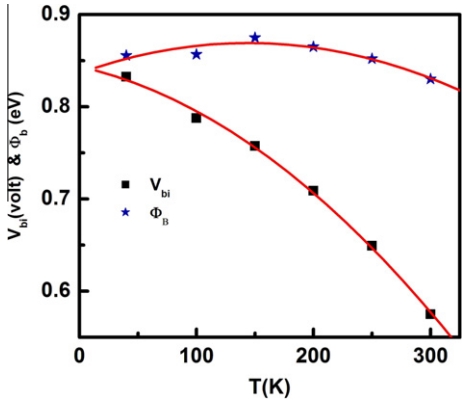

Fig. 7. Temperature dependence of built-in voltage V_{bi} and barrier height Φ_b.

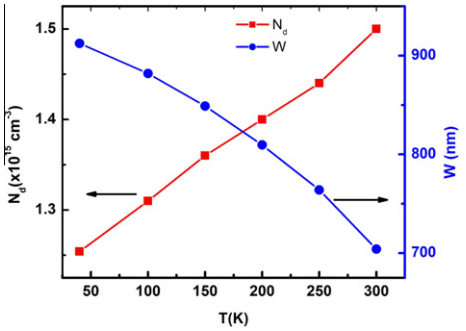

Fig. 8. Temperature dependence of both N_d and W.

Fig. 8 shows the temperature dependences of both the donor concentration and the depletion width obtained from C^{-2}–V characteristics at 1 MHz. It is noted that the donor concentration was found to increase with temperature while the width of the depletion width was found to decrease with temperature. A similar behavior was also found in the literatures [45,46,33]. This behavior can be explained by the fact that the measured capacitance may be considerably influenced by carrier trapping if the life-time of the trapping levels in the semiconductor is on the same order as the period of the ac signal applied during the capacitance measurement [33]. The increasing in temperature causes electrons to be released in the semiconductor making it into a conductor, then less width is required to store the required charge [45,46,33].

3.3. Deep levels trapping spectroscopy of Au/n-Si Schottky diode

Fig. 9 shows the DLTS spectrum for the Au/n-Si Schottky diode at different emission rates in the range 5–200 s^{-1}. Three DLTS peaks were observed. It is apparent that the linewidth of each peak corresponds to the density of the deep levels with activation energy of E_T. The density of the deep levels are 2.75×10^{20}, 6×10^{20}, 8.4×10^{19} cm^{-3} with activation energies E_{T1}, E_{T2} and E_{T3}, respectively. These densities of the deep trap levels concentration (N_T) can be determined by knowing peak height (δC_{max}) in the DLTS spectrum [47]. In the DLTS characterization, the capacitance transients of device at different temperatures were recorded.

Although conventional DLTS has played a major role in our understanding of the electronic levels associated with radiation

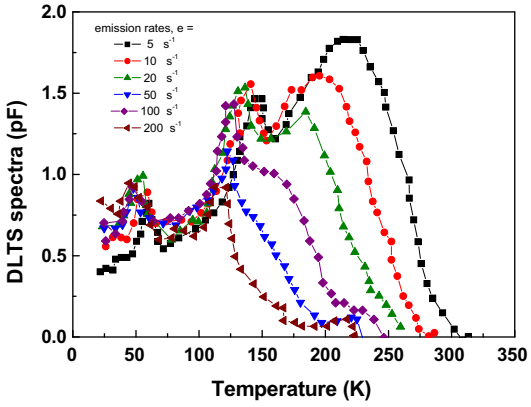

Fig. 9. DLTS spectra for Au/n-Si Schottky diode.

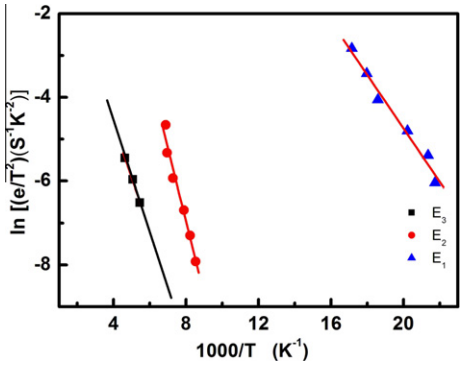

Fig. 10. Arrhenius plots of $ln\ e/T^2$ vs.1000/T for Au/n-Si Schottky diode.

damage in semiconductors, its ability to resolve levels closely spaced in energy is very poor. Among the numerous reasons for this is the fundamental way the spectrum is obtained. Even a perfect defect with no complicating factors produces a broad line on the DLTS spectrum. Any variation of time constant present in the defect emission results in an additional broadening of the peak, so fine structure is practically impossible to resolve unless the time constants are well separated [48].

When the electron emission dominates the relaxation of the trap states, the electron emission rate (e_n) at an energy level (E_T) can be given by [49]:

$$e_n = \sigma_n \gamma T^2 \exp\left(-\frac{E_T}{kT}\right), \tag{15}$$

where σ_n is the electron capture cross-section, γ is a constant, T is the absolute temperature and k is the Boltzmann constant. According to Eq. (15), it is known that the electron emission rate at each localized state exponentially depends on the energy position and temperature. Therefore, the initial rise of the DLTS signal at low temperatures can be attributed to the electron emission from the shallower localized states. As the temperature increases, the deep levels come into play in the rate window until the signal goes to zero. The electron-capture process mentioned above in Fig. 9 starts to affect the DLTS signal at the temperature at which an infection point occurs on the low-temperature side of the peaks. A peak maximum is reached when the charge decay rate from all the states equals $\ln[(t_0 + t_W)/t_0]/t_W$, where t_0 is the delay time and t_W is the period. Then the DLTS signal goes to zero where the electron emission rate for all states becomes larger than t_0^{-1} at high temperature. Arrhenius plots for all three of these levels are shown in Fig. 10. The calculated activation energies of the three deep levels E_{T1}, E_{T2} and E_{T3} are 55, 150 and 110 meV, respectively. A large number of deep levels have been identified in Si using various other techniques in conjunction with DLTS [50–53].

Although additional measurements have not been performed on these samples, some possibilities for the sources of these deep level defects have been identified in the literatures [54,55]. These possibilities are through both ionization and displacement. Ionization is a surface phenomenon. Displacement damage is a bulk phenomenon which results in the creation of defects such as vacancy, interstitial, di-vacancy, Frenkel pair, vacancy–impurity complexes namely A-center (V–O), E-center (V–P) and di-interstitial or higher order complexes called D-center [17]. The deep level defects introduced by irradiation are characterized using DLTS technique. DLTS is a high frequency capacitance transient thermal scanning method useful for observing a wide variety of deep defects in semiconductor devices [55].

4. Conclusions

The temperature dependence of both the J–V and C–V characteristics of Au/n-Si/Al structure were investigated. It was seen that ideality factor and barrier height exhibit abnormal temperature dependence and explained by invoking the Gaussian distributions of barrier heights. It was seen that there is a discrepancy between apparent barrier heights (BHs) obtained from J–V and C–V measurements. This discrepancy was especially explained by introducing a spatial distribution of SBHs due to barrier height inhomogeneities that occur at the Au/n-Si interface in the temperature range 40–300 K. The reverse current–voltage curves were interpreted in terms of a transition from electrode-limited Schottky emission to the bulk-limited Poole–Frenkel effect. The donor concentration and the depletion width were calculated using the capacitance–voltage characteristics at high frequency. The deep-level transient spectroscopy measurements were performed on Au/n-Si SD to characterize the influence of doping atoms on the electronic structure. These measurements have revealed the presence of a number of deep levels in the temperature range 40–300 K. We have also used the DLTS technique to characterize defect level observed in Au/n-Si. Three trap centers are obtained in each emission rates in the range 5–200 s^{-1}.

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