Materials Science in Semiconductor Processing 16 (2013) 1865–1872

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

A detailed comparative study on the main electrical parameters of Au/n-Si and Au/PVA:Zn/n-Si Schottky barrier diodes

Umut Aydemir [a], İlke Taşçıoğlu [a,*], Şemsettin Altındal [a], İbrahim Uslu [b]

[a] Department of Physics, Faculty of Arts and Sciences, Gazi University, Ankara, Turkey
[b] Department of Chemistry Education, Faculty of Education, Gazi University, Ankara,Turkey

ARTICLE INFO

Available online 3 August 2013

Keywords:
Au/n-Si SBD with and without PVA
Series and shunt resistance
Interface states
Comparison of main electrical parameters

ABSTRACT

We have fabricated Au/n-Si and Au/PVA:Zn/n-Si Schottky barrier diodes (SBDs) to investigate the effect of organic interfacial layer on the main electrical characteristics. Zn doped poly(vinyl alcohol) (PVA:Zn) was successfully deposited on n-Si substrate by using the electrospinning system and surface morphology of PVA:Zn was presented by SEM images. The current–voltage (I–V) characteristics of these SBDs have been investigated at room temperature. The experimental results show that interfacial layer enhances the device performance in terms of ideality factor (n), zero-bias barrier height (Φ_{B0}), series resistance (R_s), and shunt resistance (R_{sh}) with values of 1.38, 0.75 eV, 97.64 Ω, and 203 MΩ whereas those of Au/n-Si SBD are found as 1.65, 0.62 eV, 164.15 Ω and 0.597 MΩ, respectively. Also, this interfacial layer at metal/semiconductor (M/S) interface leads to a decrease in the magnitude of leakage current and density of interface states (N_{ss}). The values of N_{ss} range from 1.36×10^{12} at E_c—0.569 eV to 1.35×10^{13} eV^{-1} cm^{-2} at E_c—0.387 eV for Au/PVA:Zn/n-Si SBD and 3.34×10^{12} at E_c—0.560 eV to 1.35×10^{13} eV^{-1} cm^{-2} at E_c—0.424 eV for Au/n-Si SBD. The analysis of experimental results reveals that the existence of PVA:Zn interfacial layer improves the performance of such devices.

1. Introduction

In the literature, it can be seen that a large variety studies about Schottky barrier diodes (SBDs) are covered in terms of metal/semiconductor with and without interfacial layer (MS or MIS) type rectifying devices [1–9]. Since SBDs have technological importance, a full understanding of conduction mechanisms is of great interest. According to the Schottky and Mott theory [10,11], the barrier formation at M/S interface originates from the difference in the work functions of the metal (Φ_m) and semiconductor (Φ_s). However, experimentally observed barrier heights are less dependent metal work function than those predicted by Schottky and Mott relationship. The weak dependence of SBH on metal work function is a result of high density of interface states, which pin the Fermi Level (FL). Electronic states due to the defects and metal induced gap states were assumed to be origins of FL pinning [9]. The formation of barrier height (BH) depends on the existence of interfacial layer (deposited or native), process of surface preparation, doping concentration of semiconductor, the atomic inhomogenities at M/S interface caused by grain boundaries, multiple phases, facets, defects, mixture of different phases and the distribution of interface trap states [6–9]. Hudait and Krupanidhi [8] investigated substrate doping effect on the barrier height of Au/GaAs Schottky diodes at low temperatures. They explained the doping dependence of barrier height on the basis of

* Corresponding author. Tel.: +90 3122021247.
E-mail address: ilketascioglu@gmail.com (İ. Taşçıoğlu).

1369-8001/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mssp.2013.07.013

the thermionic field-emission (TFE) theory at low temperatures rather than TE mechanism. Lousberg et al. [5] demonstrated that increasing the n-Si substrate doping could lower the hole SBH of PtSi/n-Si junctions through an image force mechanism. On the other hand, Campbell et al. [12] demonstrated that the Schottky energy barrier between a metal and an organic material can be controlled by the insertion of an oriented dipole layer between the metal and the organic material. This dipole layer contributes to the potential drop across the metal/organic interface and a modification of the metal work function due to the adsorption of the organic molecules [12–14].

In this context, it is one of the research topics in which there is a controlled modification of electronic and transport properties of conventional metal/semiconductor structures by means of organic interfacial layers at the M/S interface. Recent studies focus on the enhancement of device performance by means of inserting new organic materials, such as rhodamine-101 [15], poly(aniline) [16], tetraamide-I [17], phenolsulfonphthalein [18], chitin [19], β-carotene [20], safranin T [21], etc. into metal–semiconductor (M/S) interface. In addition to this, using organic interfacial layer instead of inorganic one can contribute to rectification behavior of diode.

Polymers have potential advantages in large area device characterization especially in the fields of organic field effect transistors (FETs) [22,23], and organic solar cells (SCs) [24,25]. Among various conducting polymers, poly(vinyl alcohol) (PVA) is a potential material having high dielectric strength, good charge storage capacity and dopant-dependent conductivity. PVA is also considered to be important material because of its large scale applications such as in surgical devices, sutures, implantation, and for a synthetic articulate cartilage in reconstructive point surgery [26–28]. Its electrical conductivity depends on the thermally generated carriers and the addition of suitable dopant materials. A metal introduced into a polymer chain, as a rule, causes improvement in the polymer behavior and often brings about new performance properties [29–32]. Although the conducting polymers have been widely studied due to their attractive electrical, optical and other properties for applications, complete descriptions between their physical properties and chemical structures still remain unclear.

Normally polyvinyl alcohol (PVA) is a poor electrical conductor and the conductivity of the polymer is of major importance in constructing a Schottky barrier. Its electrical conductivity depends on the thermally generated carriers and the addition of suitable dopant materials. When a polymer is doped with metals especially transition elements such as Zn, Co, Ni, Cu, and Fe in various quantities and forms, their incorporation within a polymeric system may be expected to improve the conductivity [26–28]. In other words, diffusion of the dopant material into polymer matrix plays an important role in the conduction process. The doping process affects the chemical structure, crystallinity, and electrical conductivity of polymers [19,24,25].

Organic film/polymer forms a physical barrier between metal and semiconductor substrate preventing the metal to directly contact the semiconductor surface. The organic interfacial layer modifies the interface states which are established as the primary mechanism determining the energy level alignment at clean, abrupt, and defect free semiconductor interfaces [33]. It is desired that high-quality SBDs have low ideality factor, leakage current, series resistance, density of interface states and high shunt resistance by using nanometer sized organic interfacial layer. The reduction of leakage current is essential for developing polymer based SBDs. These devices should indeed be optimized for fabrication processing for low-leakage and reliable performance. Also non-optimized surface preparation conditions can influence the ultimate current–voltage characteristics strongly and lead to non-ideal behavior of SBDs.

There are many methods which are used for deposition of inorganic oxide thin films such as magnetron sputtering, chemical vapor deposition, pulsed laser deposition, molecular beam epitaxy, etc. However, all these methods are expensive and they require advanced laboratory conditions. On the other hand, organic materials were selected due to ease of process, commercial availability and fabrication by economic methods such as spin coating and electro-spinning at room temperature. That is one of the reasons why we used PVA:Zn as an organic interfacial layer in constructed SBDs.

Electrical characterization is one of the most convenient and sensitive methods for analyzing device behavior. Information on current–voltage (I–V) characteristics measured in the wide applied voltage range is vital to have an idea about the quality of the contacts and the rectifying behavior of device. Moreover, it is important to discuss the space charge limited current (SCLC) mechanism because it lets us know about charge transport properties of diode [34–38]. The flow of current is considered when carriers are injected in a semiconductor sample. If the injected carriers are more than the background carriers, the injected carriers spread and create a space charge field. The currents are controlled by this field and are known as SCLC. In spite of its technological potentials, theoretical and experimental studies on this mechanism are still not satisfied in the literature.

In this study, we doped PVA with Zn and report the improved rectification characteristics of Au/PVA:Zn/n-Si SBD in comparison with those of conventional Au/n-Si SBD. In MS and MIS type SBDs, the magnitude of main electrical parameters such as ideality factor, barrier height, leakage current, density of interface states, series and shunt resistance especially depends on the type of interfacial layer (organic or insulator). Our main purpose is to compare the main electrical parameters of fabricated diodes in respect to the presence of organic interfacial layer from I–V measurements. The effects of series resistance, shunt resistance, interface states and interfacial layer on device performance were discussed in detail. In addition, the SCLC mechanism was also discussed and detailed information can be found in the present paper. Additionally, scanning electron microscopy (SEM) analysis was carried out to provide a direct image of the organic film morphology.

2. Experimental details

The Au/PVA:Zn/n-Si SBDs were fabricated on n-type (phosphor doped) float zone (100) single crystal Si wafer

having a thickness of 350 μm and resistivity of 1–10 Ω cm. Firstly, the wafer was cleaned with RCA cleaning procedure. High purity Au metal (99.999%) with a thickness of ≈1500 Å was thermally evaporated onto the whole back side of Si wafer in a pressure of about 10^{-6} Torr in high vacuum thermal evaporation system. In order to perform good ohmic behavior, Si wafer was annealed at 450 °C with a pressure of 10^{-6} Torr.

Prior to deposition of organic film, the wafer was divided to two pieces. The PVA film was deposited on n-Si surface by the electrospinning technique. 0.1 g of zinc acetate was mixed with 0.9 g of PVA, molecular weight= 72,000 and 9 ml of deionised water. After vigorous stirring for 2 h at 50 °C, a viscous solution of PVA:Zn acetates was obtained. Using a peristaltic syringe pump, the precursor solution was delivered to a metal needle syringe (10 ml) with an inner diameter of 0.9 mm at a constant flow rate of 0.02 ml/h. The needle was connected to a high voltage power supply and positioned vertically on a clamp. A piece of flat aluminum foil was placed 15 cm below the tip of the needle to collect the nanofibers. Sample was placed on the aluminum foil. Upon applying a high voltage of 20 kV on the needle, a fluid jet was ejected from the tip. The solvent evaporated and a charged fiber was deposited onto the Si surface as a nonwoven mat. Another wafer piece was kept uncoated for reference diode. After the coating process of PVA:Zn interfacial layer, circular dots of 1 mm diameter and 1500 Å thick high purity (99.999%) Au rectifying contacts were formed on both of wafer pieces through a metal shadow mask in the thermal evaporation system with a pressure of about 10^{-6} Torr. In this way, organic modified Au/PVA:Zn/n-Si and conventional Au/n-Si SBDs were fabricated for the electrical measurements after the electrode connections were made by silver paste.

The surface images of PVA:Zn layer were taken by a JEOL JSM-6060LV scanning electron microscope (SEM) for various magnifications. Current–voltage (*I–V*) measurements were performed by means of a Keithley 2400 source-meter using Janis VPF-475 cryostat under pressure of $\sim 10^{-3}$ Torr. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

3.1. Surface morphology of PVA:Zn

In the literature, electrospinning is found to be unique in producing continuous nanofibers with several hundred micrometers length, flexibility and ease of production. Physical and chemical parameters of polymer solution such as viscosity, electrical conductivity, and polymer concentration can directly affect the formability and morphology of electrospun fibers [39,40]. SEM observations give microscopic information about the surface structure of PVA material. Morphological images of electrospun fibers taken by SEM are shown in Fig. 1, revealing the non-woven and interconnected structure of the nanofibers. Spinning of the PVA:Zn solutions resulted in uniform fibers with a broad distribution of the fiber diameter.

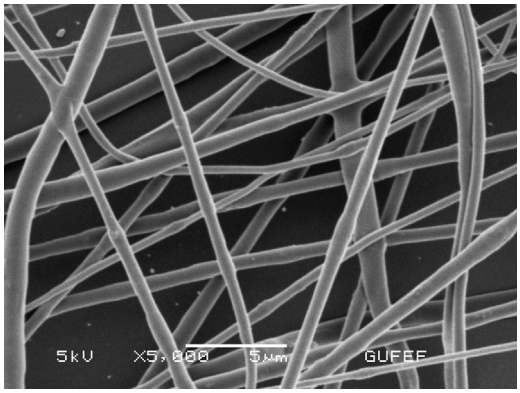

Fig. 1. SEM image of PVA:Zn polymeric interfacial layer.

Through this technique, electrospun architecture seems as nonporous smooth polymer nanofiber. Fig. 1 also confirms that the PVA:Zn film has been successfully deposited on the Si surface by electrospinning technique.

3.2. Electrical characterization

A typical semi-logarithmic forward and reverse bias *I–V* plots of the Au/n-Si and Au/PVA:Zn/n-Si SBDs are displayed in Fig. 2. It is clearly seen in Fig. 2(a) that Au/n-Si SBD with modified PVA:Zn interfacial layer has improved device characteristics with an ideality factor $n=1.38$, zero bias barrier height $\Phi_{B0}=0.75$ eV, a saturation current $I_0=6.90\times 10^{-9}$ A whereas those of Au/n-Si SBD are found as 1.65, 0.62 eV and 1.53×10^{-6} A, respectively. Generally, the high value of n greater than unity has been attributed to the presence of interfacial layer in the literature [6,7,17–20]. Thus, the electrons have to tunnel through the barrier presented by the interfacial layer, which causes the current for a given bias to be reduced. Uğurel et al. [6] investigated electron irradiation effect on Au/n-Si/Al Schottky diode and they found the values of n and Φ_{B0} as 1.44 and 0.73 eV for unirradiated sample. Özaydın et al. [7] compared electrical characteristics of Au/Cu(II) complex/n-Si (MIS) diode to conventional Au/n-Si (MS) contact. They reported that the value of $\Phi_b=0.736$ eV for the Au/Cu(II)complex/n-Si diode is higher than 0.680 eV for Au/n-Si contact. Our results show that PVA:Zn interfacial layer lowered ideality factor and increased barrier height in Au/n-Si SBD. This implies that organic interfacial layer improved the quality of diode compared to conventional Au/n-Si SBDs. Furthermore, the current bends slowly due to some effects such as series resistance (R_s), interface states (N_{ss}) and the presence of interfacial layer when applied bias voltage is sufficiently large. It is also seen in Fig. 2(b) that the leakage current of Au/PVA:Zn/n-Si SBD was also found to be two order lower than that of the Au/n-Si SBD. This is another evidence of enhancement of diode performance by using organic interfacial layer. As seen in Fig. 3, the values of rectification ratio of Au/PVA:Zn/n-Si and Au/n-Si SBDs were obtained as 7.89×10^5 and 2.89×10^3 at ± 2 V, respectively. According to the thermionic emission theory, the well known nearly ideal equation of SBD between current and applied forward

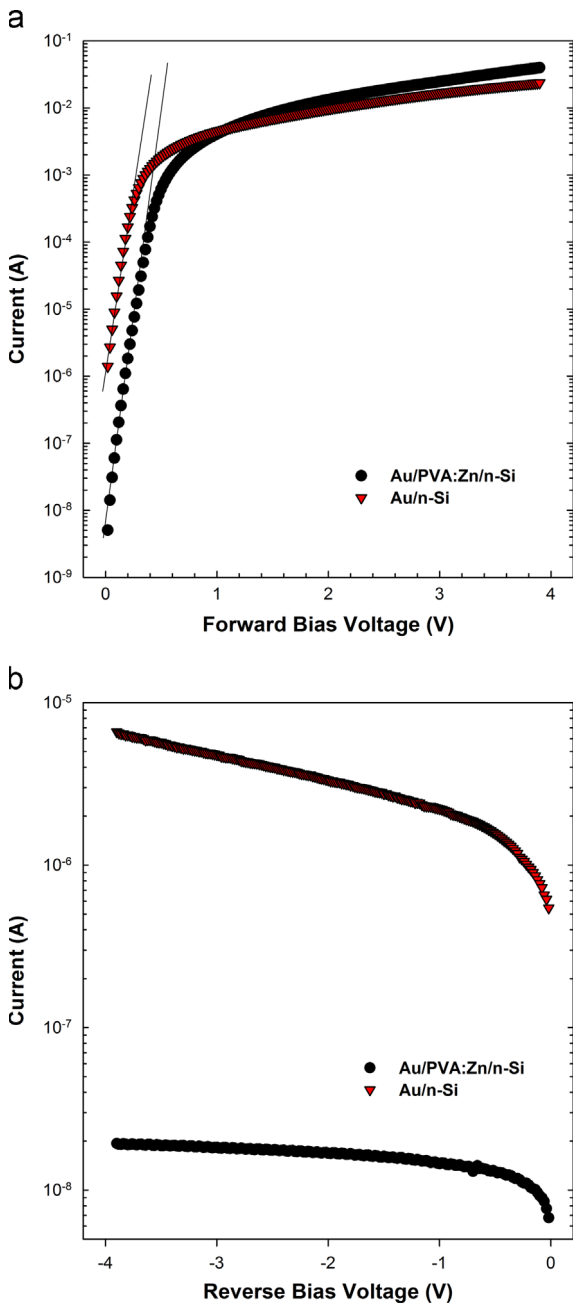

Fig. 2. The semi-logarithmic *I–V* characteristics of Au/n-Si SBD with and without PVA:Zn interfacial layer in (a) forward and (b) reverse bias conditions.

voltage ($V > 3kT/q$) can be expressed as [41,42]

$$I = I_0\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

where, V is the applied bias voltage, q is the electronic charge, n is the ideality factor, k is the Boltzmann constant, R_s is the series resistance of the diode, and T is the absolute temperature in Kelvin. The reverse saturation current I_0 is extracted from the straight-line intercept of ln *I–V* plot at

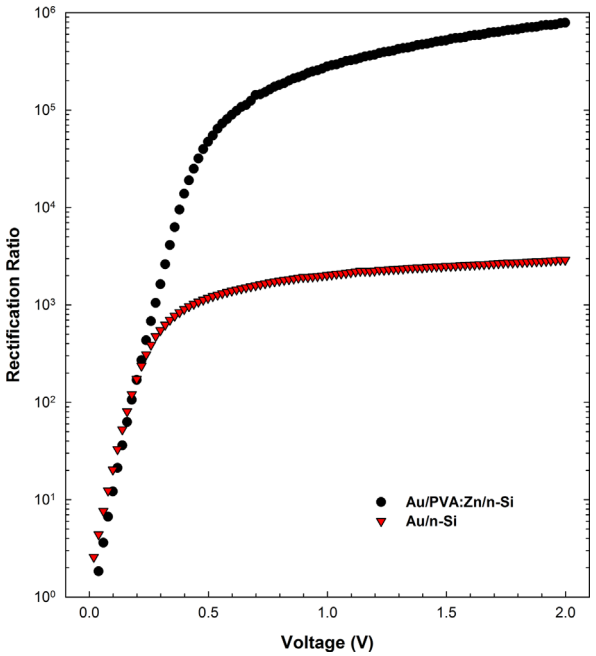

Fig. 3. The plot of rectification ratio vs. voltage for Au/n-Si SBD with and without PVA:Zn interfacial layer.

zero bias and is given by

$$I_0 = AA^*T^2\left(-\frac{q\Phi_{B0}}{kT}\right) \quad (2)$$

where A is the rectifier contact area, A^* is the effective Richardson constant (120 A/cm^2 K^2 for n-type Si) and Φ_{B0} is the zero bias barrier height which can be calculated from Eq. (2). Ideality factor n is obtained from the slope of the straight line region of the forward bias ln *I–V* plot and is given by

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (3)$$

Many authors have focused on space charge limited current (SCLC) mechanism to figure out charge transport via charging or discharging from trap centers of the injected carriers [36,37]. In order to understand charge transport mechanisms which control the behavior of the SBD, the forward bias double logarithmic *I–V* characteristics for Au/PVA:Zn/n-Si and Au/n-Si SBDs were presented in Fig. 4. This plot implies that the SCLC conduction is being dominant when the density of injected free carriers is much greater than equilibrium charge concentration and the thermally generated free carriers. In the first region, the dominant mechanism is governed by Ohm's law with slopes of slightly higher than unity for both of diodes. Possibly, high value of slopes than unity can be attributed to the fact that space charge limited behavior occurs at even applied voltages below 0.1 V. The plot shows the power law behavior between current and voltage ($I \propto V^{m+1}$) with different values of exponent ($m+1$). In the second region, the values of slopes were obtained as 6.74 and 3.46 for Au/PVA:Zn/n-Si and Au/n-Si SBDs, respectively. Here, the charge transport across the

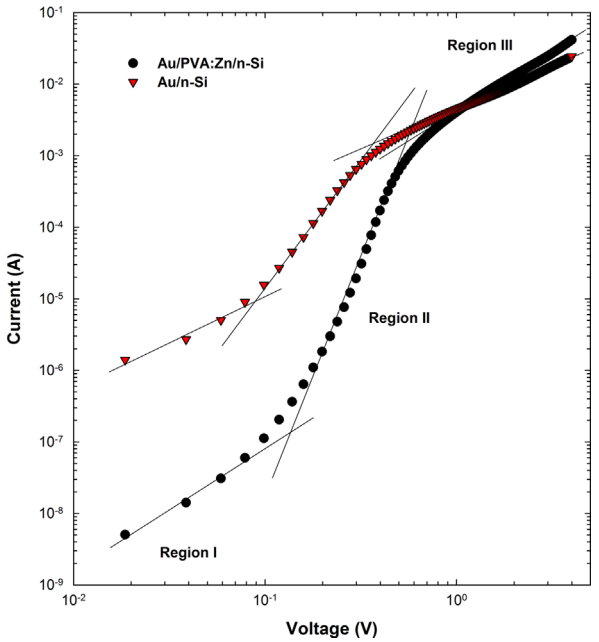

Fig. 4. Double logarithmic *I–V* characteristics of Au/n-Si SBD with and without PVA:Zn interfacial layer.

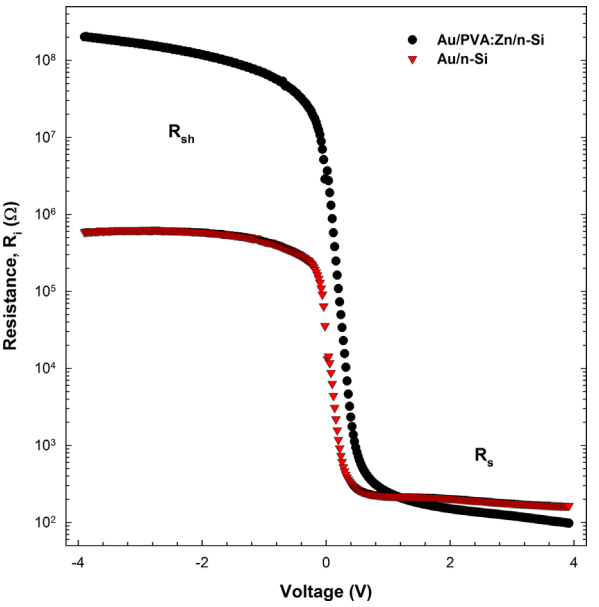

Fig. 5. The diode resistance vs. voltage characteristics of Au/n-Si SBD with and without PVA:Zn interfacial layer.

interfacial layer is governed by SCLC with exponentially distributed trap states [16,17,34–38]. Although Au/PVA:Zn/n-Si SBD has high slope value, the current magnitude is interestingly found higher than that of Au/n-Si SBD. On the other hand, the high value of slope is known as a parameter that measures the distribution of trap states located below the Fermi level. Referring to high value of slope for Au/PVA:Zn/n-Si SBD, we can say that the effective trap states can contribute to the current as well as injected carriers. The value of effective trap states is much larger and carriers are more easily released from these states of traps appearing in Au/n-Si SBD. For the third region, at high bias voltages, any contribution to current resulting from trap centers is not expected and diodes enter the trap-free SCLC. As a result, the slope of the curves tends to decrease as seen in Fig. 4.

The series resistance (R_s) and shunt resistance (R_{sh}) are two crucial parameters to understand performance quality of diode. In order to show the effect of PVA:Zn interfacial layer on R_s and R_{sh}, diode resistance (R_i) vs. applied bias voltage (V), given in Fig. 5, was drawn from the *I–V* characteristics by using following relation:

$$R_i = \frac{\partial V}{\partial I} \tag{4}$$

where V is the applied bias voltage and I is the current value of diode. It was clearly seen that the R_i values of Au/n-Si and Au/PVA:Zn/n-Si SBDs approach minimum values at high forward bias voltage which corresponds to series resistance with values of 97.64 and 164.15 Ω, while the maximum values of R_i correspond to shunt resistance with values of 203 and 0.597 MΩ respectively. For Au/PVA:Zn/n-Si SBD, the higher value of R_{sh} is a desired diode behavior which yields reduction of leakage current. There is a decrease in R_s and an increase in R_{sh} by using PVA:Zn interfacial layer. Such behavior of R_s and R_{sh} is a strong evidence of performance improvement of Au/PVA:Zn/n-Si SBD. Additionally, it is found the R_s value of Au/PVA:Zn/n-Si SBD is lower when compared to the one of Au/n-Si SBD. Also, doping of PVA could reduce the series resistance of Au/PVA:Zn/n-Si SBD. Similar results including improvement of conductivity of PVA film doped with some elements are reported in the literature [29–32]. In addition, the value of R_s can also be calculated from Cheung functions developed by Cheung [43] as follows:

$$\frac{dV}{d(\ln I)} = n\left(\frac{kT}{q}\right) + IR_s \tag{5a}$$

$$H(I) = n\Phi_{B0} + IR_s \tag{5b}$$

where IR_s is the voltage drop across the series resistance of the SBD. In Fig. 6(a) and (b), the values of $dV/d(\ln I)$–I and $H(I)$–I are plotted for Au/PVA:Zn/n-Si and Au/n-Si SBDs, respectively. The plots, $dV/d(\ln I)$–I and $H(I)$–I, will be linear at downward curvature region in forward bias semi-logarithmic *I–V* characteristics and the slopes of plots are used to determine the R_s. The values of R_s were obtained as 124.96 Ω and 126.26 Ω for Au/PVA:Zn/n-Si SBD, 195.62 Ω and 143.82 Ω for Au/n-Si SBD from Fig. 6 (a) and (b), respectively. Similar to the previous method, we found that the R_s values of diode modified with organic interfacial layer are lower than those of not modified one. This is because even if one studies in ultra-high vacuum, and uses an improved etching technique, it would be impossible to avoid the existence of a native interfacial oxide layer. The high R_s value can be attributed to the presence of a native interfacial layer between metal and semiconductor. Here, the discrepancies of R_s between Cheung functions and the previous method may be questioned. As a response to that it can be said that Cheung functions can only be applied in concave region (< 1 V) of

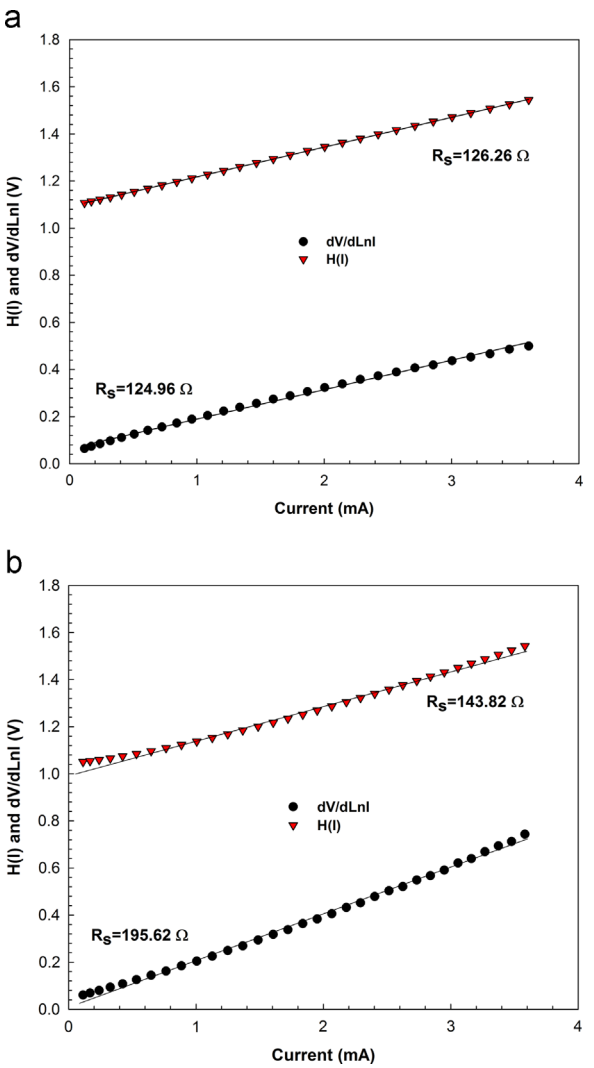

Fig. 6. The plots of $dV/d\ln I$ and $H(I)$ vs. current for Au/n-Si SBD (a) with and (b) without PVA:Zn interfacial layer.

the forward bias semi-logarithmic I–V plot. However, the calculated values of R_s from $R_i = \partial V/\partial I$ are at high forward bias voltages.

An alternative method was demonstrated by Norde [44] to determine R_s and Φ_B, according to this method, the $F(V)$ function is defined by

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{6}$$

where $I(V)$ is the current value obtained from I–V curve and γ is a constant greater than the ideality factor of diode. $F(V)$–V plot should have a minimum point which is used to calculate the values of Φ_B and R_s as follows:

$$\Phi_B = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{kT}{q} \tag{7a}$$

$$R_s = \frac{(\gamma - n)kT}{qI_{min}} \tag{7b}$$

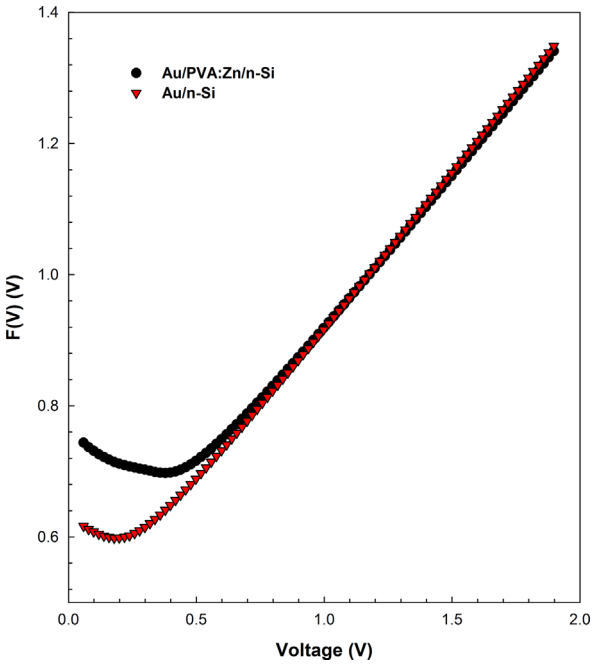

Fig. 7. The plot of $F(V)$ vs. voltage for Au/n-Si SBD with and without PVA:Zn interfacial layer.

where $F(V_{min})$ and V_{min} are the coordinates of minimum point in the $F(V)$–V plot shown in Fig. 7. I_{min} is the value of the forward bias current corresponding to V_{min}. The values of Φ_B were calculated as 0.87 eV and 0.65 eV for Au/PVA:Zn/n-Si and Au/n-Si SBDs, respectively. The R_s values obtained from Eq. (7b) are 93.67 and 124.71 for Au/PVA:Zn/n-Si and Au/n-Si SBDs, respectively. The values of R_s, obtained from Cheung and Norde's method, are not in agreement with each other for both the diodes. The discrepancy stems from the fact that Norde's method is valid for the ideal SBDs and it is applied to full forward bias I–V characteristics of the device [18,21]. Unlike Norde's method, the Cheung functions are only applied to concaving region of the forward bias I–V characteristics. The values of main electrical parameters for both the diodes are given in Table 1.

For metal/semiconductor SBD having N_{ss} which is in equilibrium with semiconductor, the ideality factor n becomes greater than unity, as deduced by Card and Rhoderick [45], and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{8}$$

where ε_i ($=8\varepsilon_o$) [23] and ε_s ($=11.8\varepsilon_o$) are the permittivities of the interfacial layer and the semiconductor, respectively, ε_o is the permittivity of free space ($\varepsilon_o = 8.5\times10^{-14}$ F/cm), δ is the thickness of the interfacial layer, W_D is the width of space charge region, and N_{ss} is the density of interface states in equilibrium with semiconductor. Furthermore, in n-type semiconductors, the energy of interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is

Table 1
Electrical parameters extracted from the *I–V* characteristics.

Sample	n	Rec. ratio	R_s (Ω)				R_{sh} (MΩ)	Φ_B (eV)	
			$\partial V/\partial I$	$dV/d \ln I$	$H(I)$	Norde		I–V	Norde
Au/PVA:Zn/n-Si	1.38	788,596	97.64	124.96	126.26	93.67	203	0.75	0.87
Au/n-Si	1.65	2890	164.15	195.62	143.82	124.71	0.597	0.62	0.65

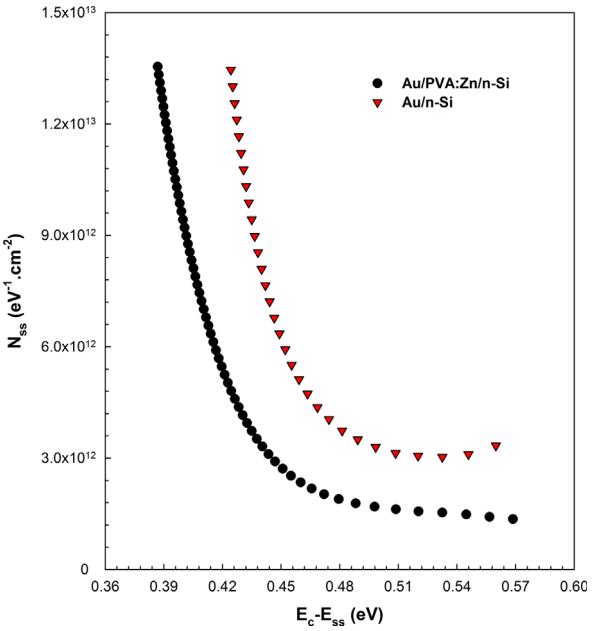

Fig. 8. The energy distribution profiles of N_{ss} for Au/n-Si SBD with and without PVA:Zn interfacial layer.

expressed as

$$E_c - E_{ss} = q[\Phi_e - V] \tag{9}$$

where V is the voltage drop across depletion layer and Φ_e is the effective barrier height.

The presence of interfacial layer between metal and semiconductor has a strong effect on interface states (N_{ss}) in terms of their density distribution and localization in the forbidden gap of semiconductor. Fig. 8 shows the energy distribution profiles of N_{ss} extracted from the forward bias I–V characteristics for Au/PVA:Zn/n-Si and Au/n-Si SBDs. As seen in Fig. 8, the N_{ss} values exponentially decrease from conduction band to mid-gap with increasing $E_c - E_{ss}$. The magnitude of N_{ss} ranges from 1.36×10^{12} at E_c—0.569 eV to 1.35×10^{13} eV^{-1} cm^{-2} at E_c—0.387 eV for Au/PVA:Zn/n-Si SBD and 3.34×10^{12} at E_c—0.560 eV to 1.35×10^{13} eV^{-1} cm^{-2} at E_c—0.424 eV for Au/n-Si SBD. Gökçen et al. [4] presented a study on Au/n-Si diodes with and without PVA (Bi_2O_3 doped) interfacial layer. They reported that the polymeric interfacial layer reduced interface state density and the leakage current of device. Since the carriers are more easily activated from trap states by low activation energy, it is very important to determine the location of N_{ss} as well as its density. As a result, it can be said that the interface properties have been improved by using PVA:Zn interfacial layer.

4. Conclusion

We have reported better rectifying properties of Au/n-Si SBD using PVA:Zn interfacial layer in comparison with Au/n-Si SBD. Low leakage current behavior was associated with the presence of PVA:Zn interfacial layer which passivates the Si surface and lowers the density of N_{ss}. In Au/PVA:Zn/n-Si SBD, an increase in barrier height of 0.62–0.75 eV was accompanied by a decrease in ideality factor from 1.65 to 1.38. Owing to the doped organic interfacial layer deposited on n-Si surface, there is a decrease in series resistance and an increase in shunt resistance for Au/PVA:Zn/n-Si SBD. Also, difference between density distribution profile of interface states for Au/PVA:Zn/n-Si and Au/n-Si SBDs has been observed. It is noted that SBD including PVA:Zn interfacial layer has low interface states. The SCLC mechanism was also discussed for both the diodes in detail. In summary, this paper presents a comparative study of Au/n-Si SBDs with and without organic interfacial layer. The results have been deduced for Au/PVA:Zn/n-Si SBD as follows:

- Decreased values of ideality factor, series resistance, and density of interface states.
- Increased values of rectification ratio, barrier height, and shunt resistance.

Acknowledgments

The authors wish to thank Gazi University-Biology Department for the SEM measurements. This study was also supported by Gazi University BAP project under the Project number BAP 05/2010-14.

References

[1] V. Mikhelashvili, P. Thangadurai, W.D. Kaplan, G. Eisenstein, Microelectronic Engineering 87 (2010) 1728.
[2] F. Yakuphanoğlu, M. Kandaz, B.F. Şenkal, Thin Solid Films 516 (2008) 8793.
[3] A.A.M. Farag, B. Gündüz, F. Yakuphanoğlu, W.A. Farooq, Synthetic Metals 160 (2010) 2559.
[4] M. Gökçen, Ş. Altındal, T. Tunç, İ. Uslu, Current Applied Physics 12 (2012) 525.
[5] G.P. Lousberg, H.Y. Yu, B. Froment, E. Augendre, A. De Keersgieter, A. Lauwers, M.-F. Li, P. Absil, M. Jurczak, S. Biesemans, IEEE Electron Device Letters 28 (2007) 123.
[6] E. Uğurel, Ş. Aydoğan, K. Şerifoğlu, A. Türüt, Microelectronic Engineering 85 (2008) 2299.

[7] C. Özaydın, K. Akkılıç, S. İlhan, Ş. Rüzgar, Ö. Güllü, H. Temel, Materials Science in Semiconductor Processing 16 (2013) 1125.
[8] M.K. Hudait, S.B. Krupanidhi, Physica B 307 (2001) 125.
[9] R.T. Tung, Journal of Vacuum Science and Technology B 11 (4) (1993) 1546.
[10] W. Schottky, Naturwissenschaften 26 (1938) 843.
[11] N.F. Mott, Proceedings of the Cambridge Philosophical Society 34 (1938) 568.
[12] I.H. Campbell, S. Rubin, T.A. Zawodzinski, J.D. Kress, R.L. Martin, D. L. Smith, Physical Review B 54 (1996) 14321.
[13] K. Seki, N. Hayashib, H. Oji, E. Ito, Y. Ouchi, H. Ishii, Thin Solid Films 393 (2001) 298.
[14] F.S. Tautz, M. Eremtchenko, J.A. Schaefer, M. Sokolowski, V. Shklover, K. Glockler, E. Umbach, Surface Science 502–503 (2002) 176.
[15] M. Çakar, N. Yıldırım, Ş. Karataş, C. Temirci, A. Turut, Journal of Applied Physics 100 (2006) 074505.
[16] A.F. Özdemir, A. Gök, A. Türüt, Thin Solid Films 515 (2007) 7253.
[17] T. Kılıçoğlu, M.E. Aydın, G. Topal, M.A. Ebeoğlu, H. Saygılı, Synthetic Metals 157 (2007) 540.
[18] Ö. Güllü, A. Türüt, Journal of Applied Physics 106 (2009) 103717.
[19] K. Akkılıç, M.E. Aydın, İ. Uzun, T. Kılıçoğlu, Synthetic Metals 156 (2006) 958.
[20] M.E. Aydın, T. Kılıçoğlu, K. Akkılıç, H. Hoşgören, Physica B 381 (2006) 113.
[21] Ö. Güllü, Ş. Aydoğan, A. Türüt, Semiconductor Science and Technology 23 (2008) 075005.
[22] M. Muccini, Nature Materials 5 (2006) 605.
[23] T.B. Singh, F. Meghdadi, S. Güneş, N. Marjanovic, G. Horowitz, N. S. Sarıçiftçi, Advanced Materials 17 (2005) 2315.
[24] S. Güneş, H. Neugebauer, N.S. Sariçiftçi, Chemical Reviews 107 (2007) 1324.
[25] D. Wöhrle, D. Meissner, Advanced Materials 3 (1991) 129.
[26] D.R. Garrel, P. Gaudereau, L. Zhang, I. Reeves, P. Brazeau, Journal of Surgical Research 51 (1991) 297.
[27] F.H. Abdel-Kader, S. Gaafar, Journal of Polymer Materials 10 (1993) 245.
[28] N.P. Peppas, E.W. Merril, Journal of Biomedical Materials Research 11 (1977) 423.
[29] A. Sheap, R.A. Abd. Allah, A.F. Basha, F.H. Abdel-Kader, Journal of Applied Polymer Science 68 (1998) 687.
[30] C. Uma Devi, A.K. Sharma, V.V.R.N. Rao, Materials Letters 56 (2002) 167.
[31] G.V. Kumar, R. Chandramani, Acta Physica Polonica A 117 (2010) 917.
[32] M.M. Bülbül, S. Bengi, İ. Dökme, Ş. Altındal, T. Tunç, Journal of Applied Physics 108 (2010) 034517.
[33] T. Kampen, A. Schuller, D.R.T. Zahn, B. Biel, J. Ortega, R. Perez, F. Flores, Applied Surface Science 234 (2004) 341.
[34] Ö. Vural, Y. Şafak, Ş. Altındal, A. Türüt, Current Applied Physics 10 (2010) 761.
[35] S.R. Forrest, Chemical Reviews 97 (1997) 1793.
[36] W. Brütting, S. Berlab, A.G. Mückl, Organic Electronics 2 (2001) 1.
[37] P. Stallinga, Electrical Characterization of Organic Electronic Materials and Devices, John Wiley and Sons, United Kingdom, 2009.
[38] Z. Ahmad, M.H. Sayyad, Physica E 41 (2009) 631.
[39] R. Ramaseshan, S. Sundarrajan, R. Jose, S. Ramakrishna, Journal of Applied Physics 102 (2007) 111101.
[40] N. Tomczak, S. Gu, M. Han, N.F. van Hulst, G. Julius Vancso, European Polymer Journal 42 (2006) 2205.
[41] E.H. Rhoderick, R.H. Williams, Metal Semiconductor Contacts, Clarendon Press, Oxford, 1988.
[42] S.M. Sze, Physics of Semiconductor Devices, third ed. John Wiley and Sons, New York, 2007.
[43] S.K. Cheung, N.W. Cheung, Applied Physics Letters 49 (1986) 85.
[44] H. Norde, Journal of Applied Physics 50 (1979) 5052.
[45] H.C. Card, E.H. Rhoderick, Journal of Physics D: Applied Physics 4 (1971) 1589.