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Leakage and trapping characteristics in Au-free AlGaN/GaN Schottky barrier diodes fabricated on C-doped buffer layers

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We investigate the DC and dynamic characteristics of AlGaN/GaN Schottky barrier diodes (SBDs) and the diodes with a gated edge termination (GET-SBD) fabricated on unintentional doped (UID) and carbon-doped AlGaN buffers. The off-state characteristics of diodes fabricated on UID buffer are dominated by buffer leakage and buffer breakdown voltage (BV) at higher reverse voltage (V_R larger than 300 V). An improvement in diode leakage and BV can be obtained by fabricating the GET-SBDs on C-doped buffers. A pronounced R_{ON} degradation of the AlGaN/GaN SBDs and GET-SBDs on carbon-doped buffers was observed by dynamic pulsed $I-V$ characterization. This dynamic R_{ON} degradation causes a clear forward current reduction for the AlGaN/GaN GET-SBDs. From combined off-state stress and current transient measurements on AlGaN/GaN SBDs, the collapsed current is recoverable and the R_{ON} degradation is due to a temporary trapping mechanism occurring in the buffer. A distinct trap level of 0.57 eV from trap spectra has been extracted for the diode fabricated on C-doped buffer, and the value was implemented in a TCAD simulator. The simulated results confirm a bulk trapping in the buffer layer for the SBD and show an additional trapping region in the GET-SBD architecture.

1 Introduction Schottky barrier diodes (SBDs) based on the AlGaN/GaN heterojunction have been promising candidates for next-generation high power switching applications owing to the excellent material properties [1–4]. Due to the formation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN interface, high performance AlGaN/GaN SBDs have been achieved with low on-resistance, high breakdown voltage and fast-switching capabilities [1]. To enable low production cost of AlGaN/GaN SBDs, many research groups are developing the heteroepitaxial growth of AlGaN/GaN active layers on large diameter silicon wafers [5–7]. Nevertheless, an increased amount of crystal defects originating from threading dislocations, impurities, point defects and unintentional dopants in the buffer can potentially degrade both the static and dynamic performances of the device [8, 9]. Buffer trapping in GaN HEMTs has been reported and investigated by current transient and back-gating measurements [10–13], but no extensive studies have been made on the buffer trapping in AlGaN/GaN SBDs.

The aim of this paper is to investigate the impact of a C-doped buffer on the parasitic buffer leakage and charge-trapping mechanisms in AlGaN/GaN SBDs grown on a silicon substrate. Wafers with unintentional doped (UID) and intentional carbon-doped AlGaN buffer layers were used for the fabrication of AlGaN/GaN SBDs. We performed pulsed $I-V$ measurements on the AlGaN/GaN SBDs and the diode with a gated edge termination (GET-SBDs) fabricated on these two buffers and compared the dynamic characteristics. A pronounced R_{ON} degradation has been observed for both AlGaN/GaN SBD and GET-SBD fabricated on the C-doped

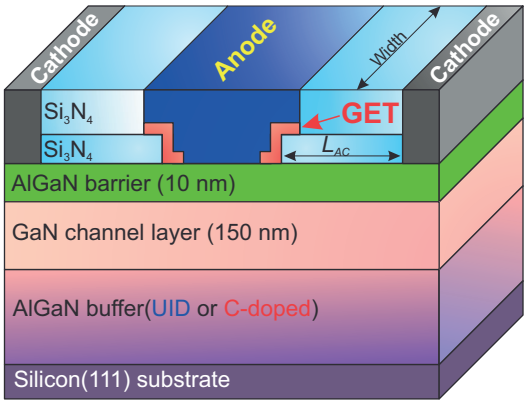

Figure 1 The schematic structure of AlGaN/GaN GET-SBD fabricated on UID or intentional C-doped buffers on silicon substrate.

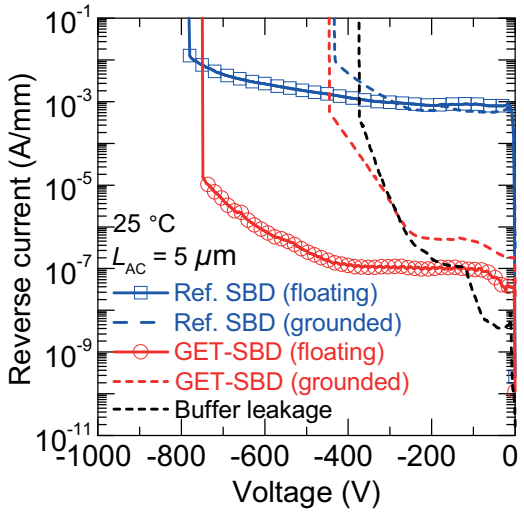

Figure 2 The off-state leakage characteristics of reference SBD and GET-SBD measured with substrate floating and grounding configurations, the vertical buffer leakage current in a UID buffer is also plotted.

buffer due to severe buffer trapping comparing with diodes on UID buffers. Due to the penetration of an increased electric field in the buffer under higher stressing voltages, more electrons can be injected from the anode and trapped in the buffer resulting in a bias-dependent R_{ON} degradation. A TCAD simulator was used to visualize the buffer trapping and explain the trapping phenomenon in GET-SBDs.

2 Experimental methodology AlGaN/GaN epitaxial layers were grown on 200 mm diameter *p*-type Si(111) wafers by metalorganic chemical vapor deposition (MOCVD). The epi-stack consists of 10 nm $Al_{0.25}Ga_{0.75}N$ barrier, a 150 nm GaN channel layer, a 2.8-μm step-graded AlGaN buffer layers, and a 200 nm AlN nucleation layer on silicon substrates. An AlN spacer layer was used between the AlGaN barrier and GaN channel layer with spacer thickness of 1 nm in the UID wafer and 0.5 nm in the wafer with carbon-doped buffers, respectively. UID and intentional carbon-doped AlGaN buffer layers as the back-barrier were used separately on two wafers to compare the DC and dynamic characteristics of AlGaN/GaN Schottky diodes. In the wafer with carbon-doped buffer, the top AlGaN back-barrier has a uniform carbon concentration of $\sim 2\times10^{19}$ cm^{-3} which was measured by SIMS profile. The entire stack was then encapsulated by a 140-nm Si_3N_4 layer by means of rapid thermal chemical vapor deposition (RTCVD). A Au-free stack of TiN-based and Ti/Al-based metals was used for the anode and cathode contacts, respectively [2]. The anode structure features a 1-μm field plate, a 5-μm anode-to-cathode spacing (L_{AC}) and the anode finger width is 100 μm. To redistribute the electric field in the vicinity of the Schottky contact, a gated edge termination (GET) structure was fabricated inside the anode trench by depositing 15-nm Si_3N_4 by means of plasma enhanced atomic layer deposition (PEALD). The AlGaN/GaN SBD without edge termination was also processed on both wafers as a reference device. A schematic structure of AlGaN/GaN GET-SBD fabricated on silicon substrate is shown in Fig. 1.

The buffer leakage and breakdown measurements of two buffers were performed by using a semiconductor device analyzer (Agilent B1505A). To evaluate the dynamic characteristics and trapping effects in AlGaN/GaN SBDs, pulsed $I-V$ and current transient spectroscopy were done with the Agilent B1505A. Pulsed forward $I-V$ characteristics are measured with a 10-ms stress pulse (quiescent state) preceding each $I-V$ point [14]. The stressing pulse at a negative voltage (V_R) is changed from 0 V to −100 V to evaluate the bias-dependent trapping mechanisms. 2DEG current transient spectroscopy on the conventional AlGaN/GaN SBD was employed to identify trap levels [15]. A TCAD simulator, with trap information defined, was used to confirm the trap location and understand the R_{ON} degradation in different device architectures.

3 Results and discussion

3.1 Buffer leakage and breakdown in GET-SBD

As is shown in Fig. 2, the conventional AlGaN/GaN SBD suffers from high leakage. Our previous study shows that this high leakage current is due to an enhancement of the electric field at the anode edge resulting in electron tunneling through the AlGaN barrier layer[16]. The significant band bending under high electric field condition can be mitigated by using an embedded edge termination inside the anode trench where the electric field is redistributed and the peak electric field at the anode edge is suppressed [16]. Comparing with the reference SBD, the GET-SBD shows 4 orders of magnitude reduction in leakage when the silicon substrate is in floating configuration. The breakdown voltage (BV) of the GET-SBD in this condition is approximately 750 V. However, a clear degradation of the diode leakage current and BV in GET-SBD is observed while grounding the substrate when the reverse voltage V_R exceeds 300 V. As is illustrate in Fig. 2, the buffer leakage current and breakdown dominate the off-state characteristics of the GET-SBD. The leakage current for

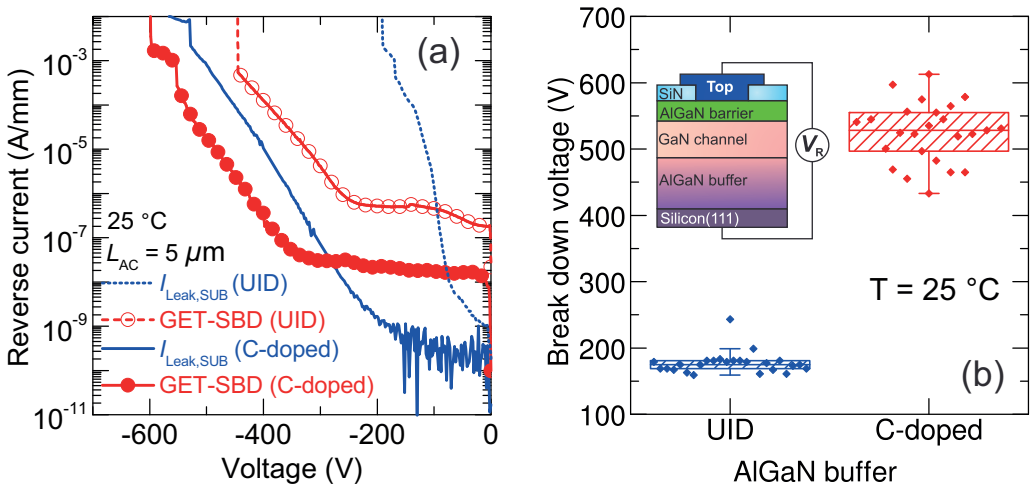

Figure 3 (a) The buffer leakage current and GET-SBD leakage current (at 25 °C) measured on UID and C-doped buffers, respectively. (b) Statistical evaluation of the vertical buffer BV for UID and C-doped AlGaN buffers.

the reference SBD is high for both floating and grounding substrate configurations and the BV of the reference SBD is also limited by the substrate leakage while grounding the substrate. As the reverse voltage increases, the electric field across the entire buffer layer intensifies which results in more carrier injection and trap-assisted tunneling currents in the vertical direction. The buffer breaks down when the reverse voltage exceeds a critical value independent of the anode topology.

Intentional carbon-doped GaN or AlGaN buffer layers as the back-barrier have been proposed to suppress the buffer leakage current in literature [17, 18]. The off-state electrical characterization has been performed on GET-SBD fabricated on UID and C-doped buffers in order to study the influence of the carbon. The buffer leakage current was suppressed for the GET-SBD fabricated on C-doped AlGaN buffer layers (Fig. 3(a)). The vertical buffer BV was statistically assessed on dedicated structure shown in Fig. 3(b). The top electrode in the breakdown (BD) test structure is a cathode contact (ohmic contact with the 2DEG), and the measurements were performed by applying a negative voltage at the top contact while grounding the silicon substrate. There is a significant improvement of buffer BV in C-doped AlGaN buffers, which is also reflected in the enhancement of the diode BV as displayed in Fig. 3(a). In the lower voltage range ($V_R < 200$ V), the overall leakage current of the GET-SBD is dominated by the injection of electrons from the anode contact to the GaN channel. As the V_R further increases, the buffer leakage current shows an exponential dependence on V_R which reflects in the rising leakage current of the GET-SBD. Though the suppression of buffer leakage and enhancement of buffer BV with a C-doped buffer, there is still a need to further optimize the buffer for higher voltage applications.

3.2 R_{ON} degradation and trapping effects The dynamic characteristics of the GET-SBD on two buffers have been performed by using a measurement procedure reported in [14]. When the AlGaN/GaN SBD is subject to a high reverse voltage, the 2DEG in the vicinity of the anode contact is depleted and the depletion region extends in the lateral direction towards the cathode contacts [19, 20]. The electrons can be injected from the anode contact into the GaN channel and in the buffer leading to the leakage current and trapping phenomena. The capture process of electrons during OFF-state stress for AlGaN/GaN HFET has been reported in [21], which also showed a temperature enhanced capture based on the Shockley–Read–Hall (SRH) model.

Typical pulsed *I*–*V* characteristics of AlGaN/GaN GET-SBDs fabricated on UID and C-doped buffers are presented in Fig. 4(a) and (b), respectively. In the fresh condition, the GET-SBDs on the two buffers showed different turn-on voltage due to different spacer thickness in the epi-stack. A thicker AlN spacer was used in the GET-SBD with a UID buffer, which leads to a higher turn-on voltage. However, it should not be the dominant factor in the electron trapping considering the very thin nature of the spacer. The GET-SBD on UID buffers shows stable forward characteristics without significant R_{ON} increase and current degradation with the increase of the stressing voltage V_R. However, the GET-SBD on C-doped buffers shows a clear degradation of the forward current due to the dominant dynamic R_{ON} increase with increased pulsed stress.

To investigate the dynamic stability of both AlGaN/GaN reference SBD and GET-SBD on two buffer structures, the bias-dependent dynamic R_{ON} increase (6 devices from different dies on the wafer) is presented in Fig. 5 and Fig. 6. The AlGaN/GaN SBDs and GET-SBDs on UID buffers show a more stable dynamic R_{ON} compared with reference SBDs and GET-SBDs on C-doped buffers. On both UID and C-doped buffers, GET-SBDs show lower dynamic R_{ON} increase compared with the reference SBDs. This can be due to the redistribution of the electric field in the vicinity of the Schottky contact [16]. The pronounced dynamic R_{ON} increase for diodes on C-doped buffers indicates that the R_{ON}

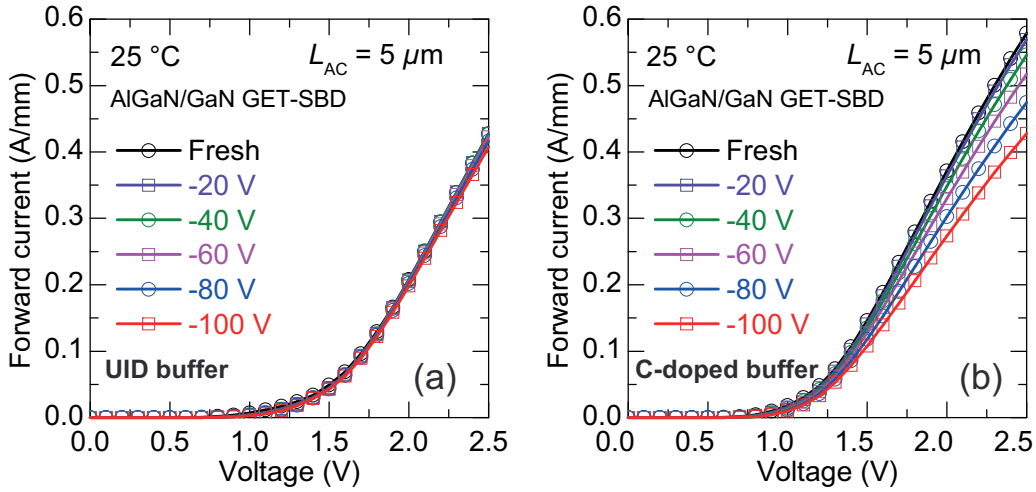

Figure 4 (a) Typical pulsed *I*–*V* characteristics of AlGaN/GaN GET-SBD fabricated on a UID buffer. (b) Typical pulsed *I*–*V* characteristics of AlGaN/GaN GET-SBD fabricated on a C-doped buffer.

degradation is due to the C-doped buffer and C-related trap states. In our recent work, the dominant buffer trapping causing the bias-dependent dynamic R_{ON} in AlGaN/GaN SBDs was attributed to the crystal defects generated during the growth of the C-doped buffer [22]. The GET-SBD on C-doped buffer, with much lower leakage current than the reference SBD, still showed a ∼30 % R_{ON} increase after a pre-bias at −100 V compared with negligible R_{ON} increase for the GET-SBD on UID buffers.

Current transient measurements on the reference SBD was performed to extract the energy levels. Direct transient measurements on the GET-SBD architecture can be difficult due to its much more complex structure and non-uniform trapping regions. Furthermore, a 2D TCAD simulation was performed on both reference SBD and GET-SBD to visualize the trapping region at a stress voltage of −100 V and to understand the dynamic R_{ON} increase as shown in Fig. 6.

3.3 Current transient and buffer trapping Current transient measurements on the 2DEG resistor after diode off-state stress at V_R of −100 V were performed to study the trapping mechanisms for the AlGaN/GaN SBD fabricated on C-doped buffer. More details regarding the measurement procedure can be found in [15]. The recovery of the 2DEG current in the AlGaN/GaN SBD structure after a 10-s stress at −100 V has been performed from 30 to 150 °C (Fig. 7(a)). As can be seen in Fig. 7(a), it takes ∼ 1000 s for the SBD structure to recover back to the fresh condition at 50 °C and the transient current saturates for longer times. In a power switching converter, however, the operating frequency ranges from kHz to several MHz [23, 24]. In this case, the trapped electrons do not have sufficiently long time to fully de-trap resulting in an increased ON-resistance. As a consequence, this leads to more power loss and lower conversion efficiency.

A sum of pure exponentials was used to fit the raw experimental data and smooth the de-trapping transient data [10, 25, 15]. This method assumes that the current transient process involves independent de-trapping characteristics. The number of trapped states decays with a characteristic time in an exponential fashion [10, 25], which gives an exponential increase of the recovery current. The validity of this method has been reported in [10].

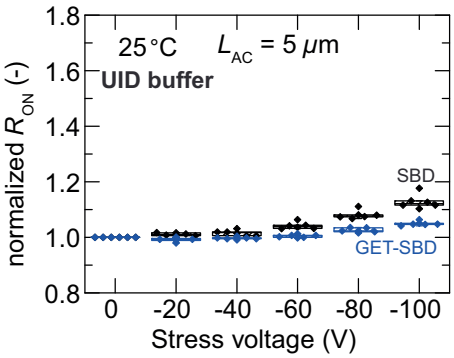

Figure 5 The normalized dynamic R_{ON} degradation for the reference SBD and GET-SBD on UID AlGaN buffers measured at 25 °C.

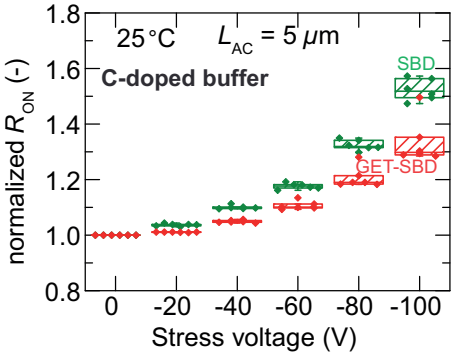

Figure 6 The normalized dynamic R_{ON} degradation for reference SBD and GET-SBD on C-doped buffers measured at 25 °C.

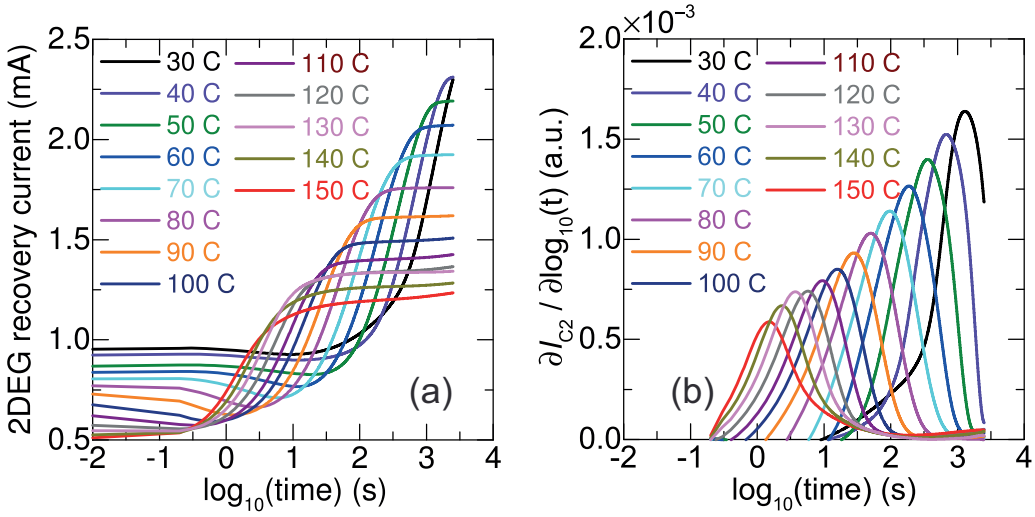

Figure 7 (a) The recovery current of 2DEG channel after the diode is biased at −100 V measured at elevated temperatures. (b) The time-constant spectra for different temperatures.

The time constant spectra (the derivative of the current transients) of the SBD are shown in Fig. 7(b). Each peak in the time constant spectra corresponds to a time-constant at a specific temperature. As the temperature increases, the peak moves to the left indicating that the degraded device recovers faster at high temperatures. The Arrhenius plot shown in Fig. 8 reveals the dominant trap level extracted from the current transient measurements performed on the SBDs fabricated on UID and C-doped buffers. There is a distinct trap level at 0.57 eV with a cross-section of 4.3 $\times 10^{-20}$ cm^{-2} extrapolated on the diode with C-doped buffers and a trap level at 0.65 eV with a cross-section of 0.89 $\times 10^{-20}$ cm^{-2} for the SBD fabricated on UID buffers which was previously identified as a surface trap [15]. It is important to note that the trap energy level can be associated with the buffer transport mechanisms during the electron emission process [8]. The small apparent cross-section can be explained by Hermann and Warfield's model [26, 27], in which the cross-section decreases exponentially with the depth due to an additional transport process needed in the de-trapping kinetics. The surface trap level was not observed in the SBD on C-doped buffer, this can be due to the dominant buffer trapping mechanism.

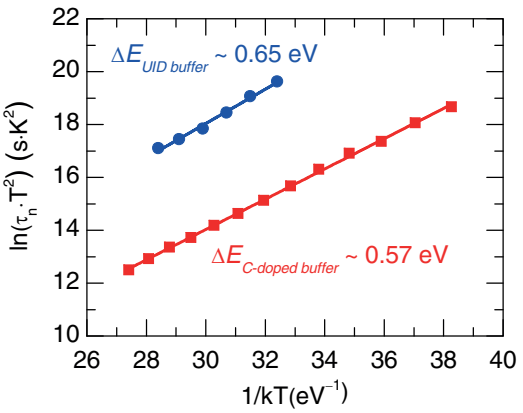

Figure 8 The Arrhenius plot for the diode on UID and C-doped buffer.

3.4 TCAD simulation Two-dimensional TCAD simulations have been performed by using a commercial semiconductor device simulator to visualize the trap location and understand the trapping phenomenon in both SBD and GET-SBD [28]. In the simulator, an acceptor trap at $E_C-0.57$ eV with uniform spatial density of 10^{17} cm^{-3} (similar to [29]) has been defined in the buffer layer. The electric field distribution in the AlGaN barrier (0.5 nm below the anode contact) at V_R of −100 V for the conventional SBD and GET-SBD is dipicted in Fig. 9(a) and (b), respectively. The edge termination in the GET-SBD architecture redistributes the electric field and suppresses the peak electric field at the anode edge, thus the leakage current of the GET-SBD is significantly reduced. It should be noted that there is an additional peak electric field at the edge of GET which withstands the voltage in the diode off-state operation.

As discussed before, the GET-SBD fabricated on C-doped buffers still shows pronounced R_{ON} degradation though a smoother electric field distribution is realized compared with the conventional SBD (shown in Fig. 6). The 2D buffer trap occupancy for reference SBD and GET-SBD is shown in Fig. 9(c) and (d) to confirm the trap location and understand the trapping mechanism. The occupancy of the acceptor states is "0" when it is not filled, and the occupancy equates to "1" when an electron is captured by the trap state. In Fig. 9(c), a trapping zone is shown in the buffer layer of the conventional SBD. The location of that trapping region is below the anode edge, which can be caused by the vertical depletion region and the injected electrons into the

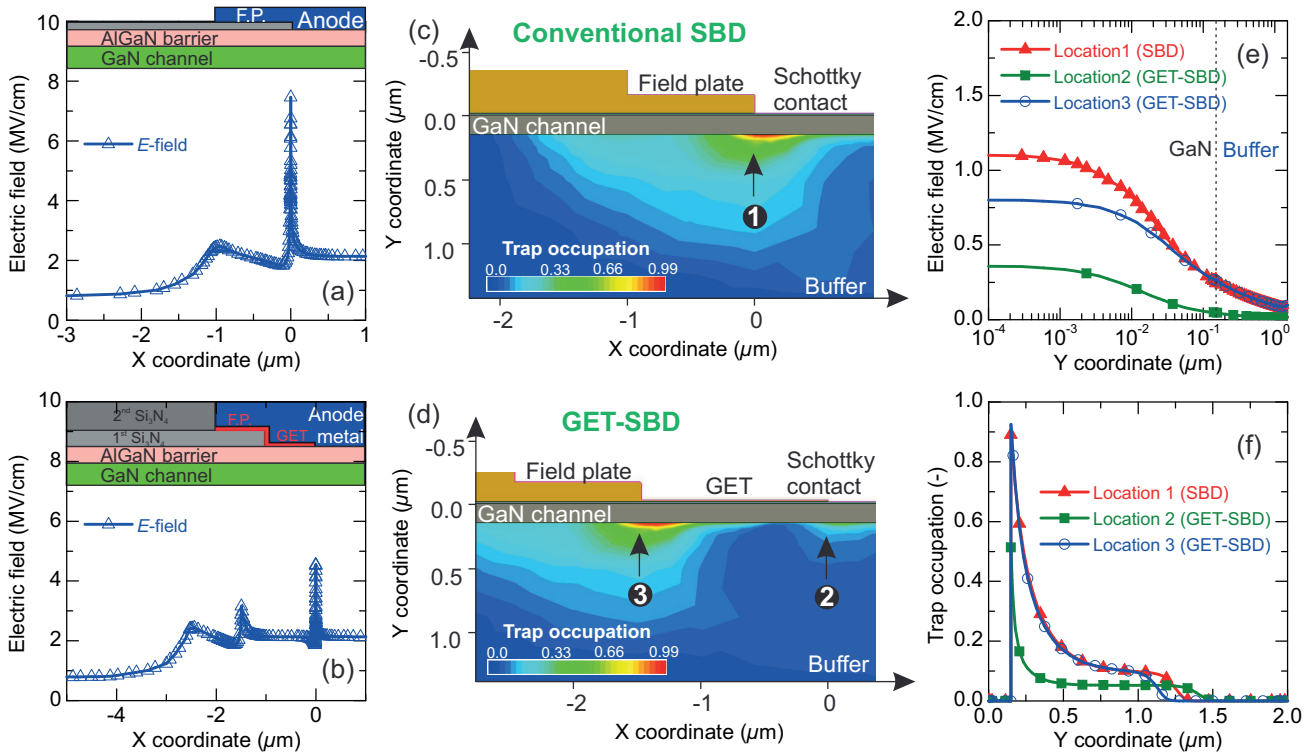

Figure 9 The electric field distribution in the AlGaN barrier (0.5 nm below the anode contact) at V_R of −100 V for the reference SBD (a) and the GET-SBD (b). The buffer trap occupancy at V_R of −100 V for the reference SBD (c) and GET-SBD (d). (e) The vertical electric field penetration into the GaN channel and buffer layer by taking a vertical cut-line at three different locations as indicated in (c) and (d). (f) The trap occupation in the buffer along the vertical cut-lines.

buffer due to the vertical electric field. The filled acceptor state, which is negatively charged, depletes the 2DEG and reduces the electron density due to the virtual gate effect [30]. This results in the R_{ON} degradation in the AlGaN/GaN SBD. In the case of the GET-SBD, the peak electric field at the anode edge is lower, resulting in a smaller trapping region below the anode edge (shown in Fig. 9(d)). However, an additional trapping region appears below the GET edge due to the electric field peak at the corner of the edge termination. In Fig. 9(e) and (f), the vertical electric field and trap occupation cut at the anode edge of the SBD (location 1), anode edge of the GET-SBD (location 2), and the corner of the edge termination (location 3) are shown, respectively. It can be seen that the field penetrates through the GaN channel into the AlGaN back-barrier. The magnitude of the electric field contributes to the 2D trapping regions in the SBD and GET-SBD. In Fig. 9(c), (d) and (f), we can observe that the trapping regions in the diodes are non-uniform due to the 2D electric field distribution. From simulated results, we clearly observe an additional trapping region in the buffer layer of the GET-SBD. Despite the different electric field distribution and trap occupation between SBD and GET-SBD, the trend of buffer trapping has been confirmed in both SBD and GET-SBD topologies which were fabricated on a carbon-doped buffer. We can conclude that the stability of the GET-SBD can be significantly improved by fabricating the diodes on "dispersion-free" buffers, in which case the dominant buffer trapping can be minimized.

4 Conclusions In this work, we have compared the leakage characteristics and dynamic stability of AlGaN/GaN SBDs fabricated on two buffer layers: UID and intentional C-doped buffers. The gated edge termination in GET-SBD enables the suppression of the diode leakage current in the low voltage regime, however, the buffer leakage and BV mechanisms dominate the diode off-state characteristics at higher voltage regimes (V_R larger than 300 V) due to the increasing vertical electric field. C-doped AlGaN buffer as the back-barrier is shown to suppress the buffer leakage and enhance the buffer BV, thus better diode performance can be obtained. However, a dominant buffer trapping at E_C−0.57 eV is degrading the dynamic characteristics of both reference AlGaN/GaN SBD and GET-SBD. TCAD simulation results show a trapping region located in the buffer when the diode is biased in the off-state (at V_R of −100 V). An additional trapping zone below the GET edge is shown in the GET-SBD architecture, which explains the severe R_{ON} degradation in the GET-SBD. This study indicates that the stability of low-leakage GET-SBD can be significantly improved by fabricating the diodes on a dispersion-free buffer layer.

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