

Distinction between silicon and oxide traps using single-trap spectroscopy

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In this work, both time domain random telegraph noise (RTN) and frequency domain Lorentzian spectra due to generation–recombination (GR) centres are studied in ultra-thin buried oxide (UTBOX) silicon-on-insulator (SOI) nMOSFETs. As will be shown, for a Si film-related RTN, the corner frequency is moderately dependent on the gate voltage, while a strong V_{GS} dependence is found for an oxide RTN. This translates in the time domain in a different behaviour of the capture and the

emission time constants and their ratio: for an oxide RTN, an exponential gate voltage dependence is observed for the time constant ratio, from which the trap depth in the oxide can be derived. On the other hand, for a defect in the silicon film, the ratio remains constant around one, indicating that the Fermi level is close to the trap level in that case. Based on this analysis, one can distinguish RTN due to gate oxide traps from RTN due to silicon film defects.

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1 Introduction As CMOS technology dimensions reach the nanoscale, both static and dynamic variability affect the device and circuit performance [1–5]. Dynamic variability, better known as low-frequency (LF) noise, generally scales with the inverse of the transistor area, so that large current fluctuations with time can occur in small transistors [6–9]. Ultimately, this results in so called random telegraph noise (RTN), caused by a single defect in the device. In that case, the current switches between a high and a low state with amplitude ΔI_D in the drain current (I_D) and average up and down time constants, which usually correspond with the capture and emission time [10]. The corresponding noise spectrum is a Lorentzian, characterised by a constant plateau amplitude and a corner frequency f_c . While most RTNs are believed to originate from traps in the gate dielectric at some distance from the channel, it has recently been shown that also traps residing in the fully depleted (FD) film of an ultra-thin buried oxide (UTBOX) silicon-on-insulator (SOI) nMOSFET can give rise to RTN [9].

In this work, methods to trace back the origin of Lorentzian-type generation–recombination (GR) noise will be discussed. In the case of partially depleted SOI or bulk transistors, some clear criteria have been established in the past to distinguish GR noise in the depletion region from Lorentzians due to oxide traps: one important finger print is that in the case of GR noise due to bulk traps the f_c is independent of the front gate voltage V_{GS} , when observed above threshold voltage V_T [11,12]2007. This is related to the fact that the Lorentzian noise is dominated by contributions of GR centres close to the crossing point of the quasi-Fermi level and the trap level E_T .

For fully depleted UTBOX devices, on the other hand, it has recently been shown that the corner frequency of a Lorentzian corresponding with bulk traps can exhibit a strong variation with V_{GS} [13], so that a more careful procedure has to be established. For example, the analysis of the LF noise at one interface can give information on the trap origin, by imposing the accumulation mode at the other

interface, thereby screening the influence of the corresponding oxide traps from the other interface [14]. At the same time, it has been shown that the GR noise associated with defects in the silicon film corresponds with a small number of trap centres [9], so that RTN fluctuations can be expected in the time domain.

In this work, frequency-domain spectroscopy combined with time-domain measurements were compared for two typical UTBOX SOI nMOSFETs, showing clearly distinct behaviour of the RTN and Lorentzian parameters as a function of V_{GS} . Based on that, criteria for the two types of traps, namely, gate oxide and film defects will be formulated.

2 Device and measurement details The devices studied are SOI UTBOX nMOSFETs fabricated for single-transistor (1T) floating-body random access memory (RAM) applications. The UTBOX device has an undoped channel and a highly doped source and drain without extensions. The gate length is 130 nm, the gate SiO_2 thickness is 5 nm, the silicon film thickness is 14 nm and the BOX thickness is 18 nm. More process details can be found elsewhere [15]. Typical input characteristics for the device are represented in Fig. 1 in linear and semi-logarithmic scale, with the back-gate voltage fixed at 0 V.

The current noise power spectral density (PSD) S_I is measured at room temperature using a semi-automatic probe station with an HP4142 DC analyser, an HP 35665 A signal analyser and a BTA9812B noise analyser, with NoisePro software from Proplussolutions. The device was biased in the linear operation regime ($V_{DS} = 0.05$ V) and with back-gate biased at 0 V. The front-gate voltage (V_{GS}) was stepped from weak inversion to strong inversion region. Time domain drain current measurement are also taken with the same bias and same system.

3 Data analysis The most important parameters describing the GR noise are the noise amplitude ($S_I(0)$), the corner frequency, and the capture (τ_c) and emission time

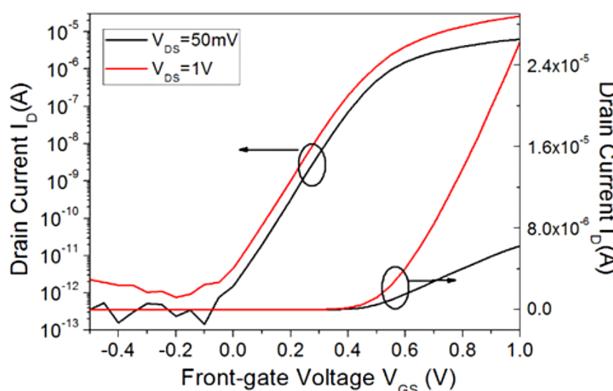


Figure 1 Typical input I_D - V_{GS} characteristics at zero back-gate bias with drain to source voltage V_{DS} at 50 mV and 1 V for a $W=0.11\text{ }\mu\text{m}$ and $L=130\text{ nm}$ UTBOX SOI nMOSFET.

constant (τ_e), which can be obtained from noise power spectrum and time domain measurements. In order to derive these parameters accurately, one can apply an optimised data analysis.

3.1 Spectrum analysis Normally, the noise power spectrum contains both flicker noise and GR noise at low frequencies [9]. The first step is to decompose the spectrum into a flicker or $1/f$ noise component and one (or more) GR noise components. In the case of one Lorentzian component, one can express the current noise PSD in general as [12, 16]

$$S_I(f) = B + K/f + A/(1 + (f/f_c)^2) \quad (1)$$

where A , B and K , are the Lorentzian noise, the white noise and the flicker noise amplitude factor, respectively, and f_c is the corner frequency. An example of a fit is given in Fig. 2.

Alternatively, the corner frequency of a Lorentzian corresponds with the peak in the $f \times S_I$ versus f characteristics is shown in Fig. 3.

3.2 Time domain data analysis In the presence of RTN, the drain current in a certain bias point will show a more or less complex switching behavior between two (or more) discrete levels, as illustrated in Fig. 4.

Time domain measurements can provide more information on the RTN. Combined with frequency domain data, one can have a better analysis of GR noise. Different measurement methods and analyses can be combined analyses can be combined, compared and checked for more consistency.

Traditionally, the RTN data can be grouped in a histogram, like in Fig. 5a, from which the amplitude ΔI_D and the average up and down time constants can be derived in the case of a simple two-level RTN. The up and down times are the duration of the current in the high and the low level. The up times and down times follow a Poisson distribution,

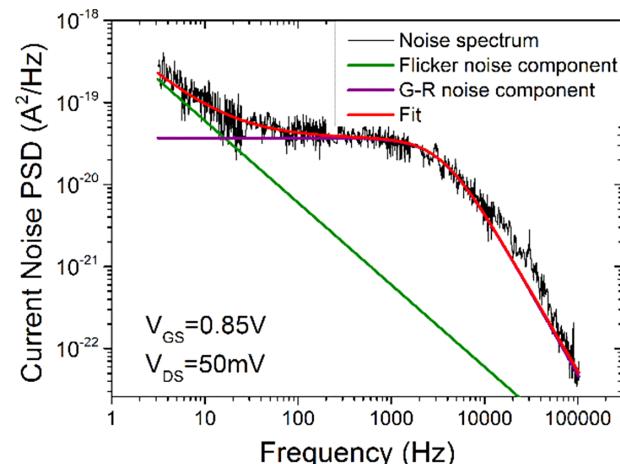


Figure 2 Typical Lorentzian noise spectrum and its decomposition into a flicker and GR noise component, according to Eq. (1).

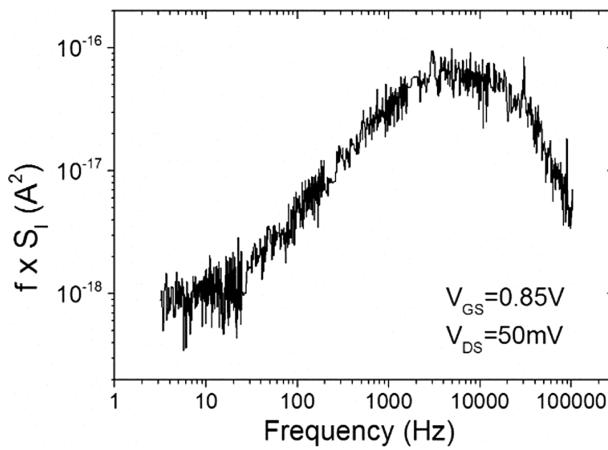


Figure 3 Typical peak in $f \times S_I$ versus frequency corresponding to a Lorentzian noise component in an UTBOX SOI nMOSFET.

given by [10]

$$P_1(t) = \frac{1}{\tau_1} \exp\left(-\frac{t}{\tau_1}\right), \quad (2)$$

with τ_1 the average value, corresponding either with τ_c or τ_e .

As the I_D in the low state and high state is Gaussian distributed, the ratio of peak heights represents the ratio of the total time duration of up state and down state. Moreover, from GR noise theory, it is known that

$$2\pi f_c = \frac{1}{\tau_c} + \frac{1}{\tau_e}, \quad (3)$$

relating the Lorenzian corner frequency to the RTN time constants. Taking advantage of the time constant ratio and the corner frequency derived from the spectrum, capture and emission time constants can also be calculated.

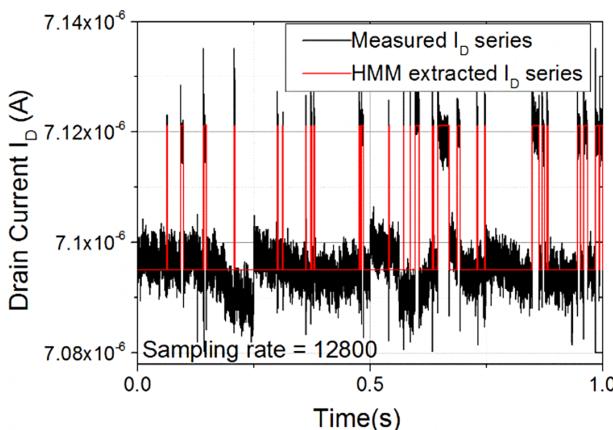


Figure 4 Drain current fluctuations and the corresponding extracted RTN state, as a function of the time in an UTBOX SOI nMOSFET at $V_{DS} = 0.05$ V and $V_{GS} = 0.8$ V.

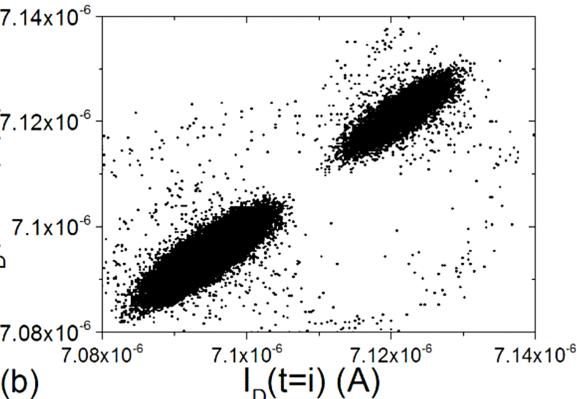
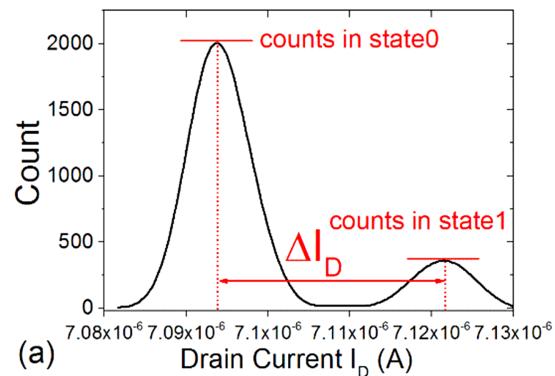


Figure 5 Histogram of a two-level RTN (a) and corresponding TLP (b).

When complex RTN occurs, with switching between more than two levels, a simple yet more accurate method consists in using a so-called time lag plot (TLP) [17–19]. It is a tool for analysing autocorrelation in time-series data and can be used to analyse time-domain RTN data. An I_D time lag plot is constructed by plotting I_D sampled at the i th time, $I_D(i)$ versus I_D sampled at $i + 1$ th time, $I_D(i + 1)$ [18], like in Fig. 5b. Using I_D histogram and I_D time lag plot, I_D levels and the RTN amplitude can be detected. In cases of multi-level RTN, the I_D TLP can have a better resolution.

The most accurate method to extract the capture and emission time is by a statistical method, for example, relying on a hidden Markov model (HMM) [17]. A HMM can be considered as the simplest dynamic Bayesian network. Given the I_D time series, the most likely trap state at each time step can be obtained, as well as the transmission probability between the low and high state. In Fig. 4, the measured I_D waveform and extracted RTN state series are plotted. In this way, capture time and emission time can be derived from the transition probability. The HMM extraction method is a significant improvement over the histogram and TLP methods of analysing RTN. HMM algorithms can get more accurate results than other methods for RTN with large signal-to-noise ratio.

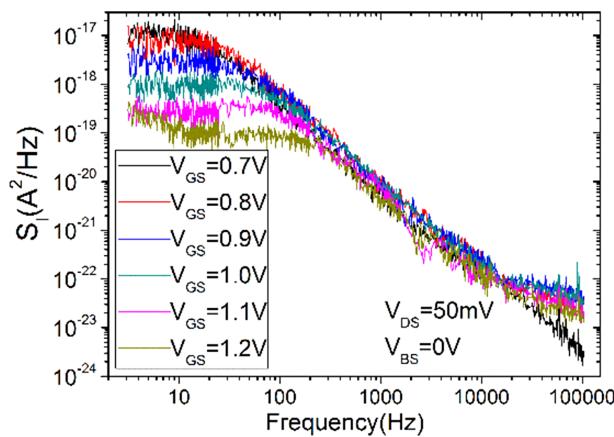


Figure 6 Lorentzian spectra at different front-gate voltages for a GR centre in the front gate dielectric of an FD UTBOX SOI nMOSFET.

4 Results In this section, the experimental results for two different RTNs will be described and the traps will be identified either as a gate oxide or as a silicon trap.

4.1 Gate oxide trap Gate oxide trap induced RTN is due to carrier capture and emission between the channel and a single trap in the gate dielectric. The Lorentzians of Fig. 6 exhibit a strong dependence of the corner frequency (Fig. 7) and plateau on the gate voltage in linear operation, making it a strong candidate for a standard gate oxide RTN. To more firmly establish this assignment, time domain measurement have been carried out, showing for example a more or less exponential reduction variation of the time constant ratio (τ_c/τ_e) on gate voltage (Fig. 8). This variation mainly comes from the reduction of τ_c with increasing V_{GS} (or carrier concentration) according to the Shockley–Read–Hall (SRH) theory [10].

The trap depth x_t in the front gate dielectric can be extracted from the dependence of τ_e/τ_c with front gate bias

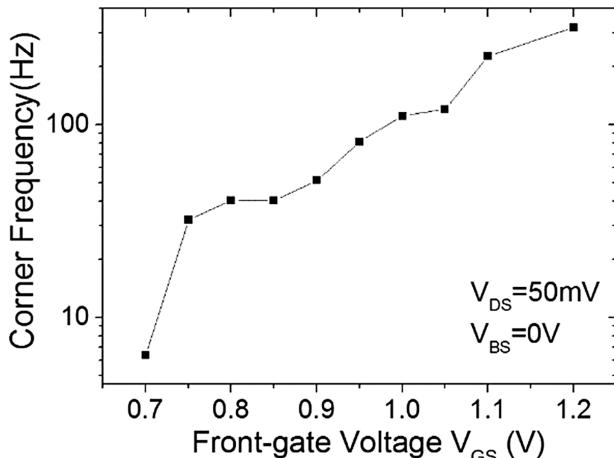


Figure 7 Corner frequency f_c at different front gate voltages for a GR centre in front gate dielectric of a FD UTBOX SOI nMOSFET.

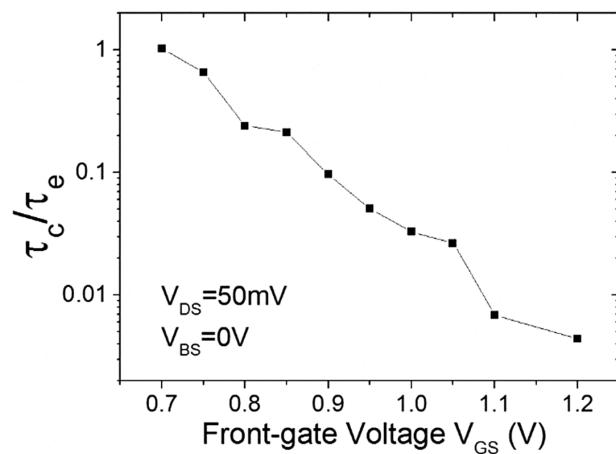


Figure 8 The ratio of capture and emission time at different front gate voltages for a GR centre in the front gate dielectric of an FD UTBOX SOI nMOSFET.

V_{GS} according to [10]

$$\frac{t_{ox} - x_t}{t_{ox}} = - \frac{kT}{q} \frac{\delta(\ln \tau_c / \tau_e)}{\delta V_{GS}} \quad (4)$$

with t_{ox} the gate oxide thickness, kT the thermal voltage and q the elementary charge. For the case of Fig. 8, t_{ox} is 5 nm, so that x_t has a value of 1.5 nm. At the same time, the RTN relative amplitude value ($\Delta I_D/I_D$) shows a peak shaped variation with V_{GS} as seen in Fig. 9.

4.2 Silicon trap The Lorentzian spectra of Fig. 10 exhibit a weak dependence on the gate voltage, whereby the corner frequency in Fig. 11 increases moderately, compared with Fig. 7. At the same time, the Lorentzian plateau amplitude $S_l(0)$ in Fig. 12 exhibits a gate voltage

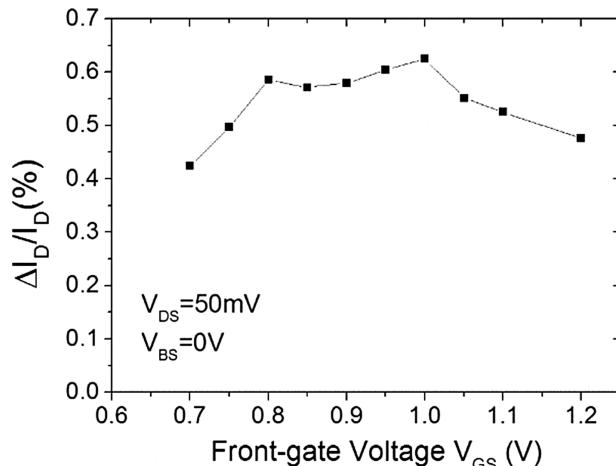


Figure 9 RTN relative amplitude at different front-gate voltages for a GR centre in the front-gate dielectric of a FD UTBOX SOI nMOSFET.

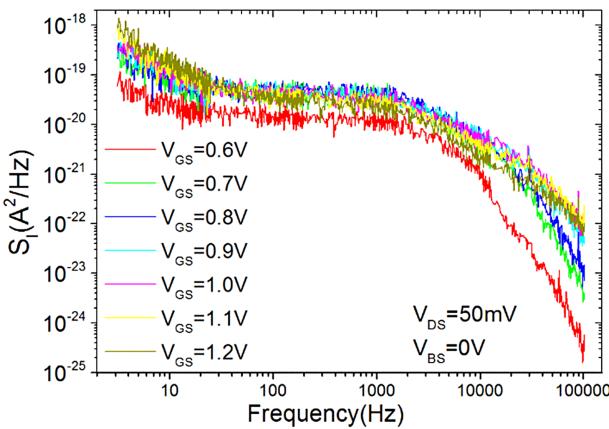


Figure 10 Lorentzian spectra at different front-gate voltages for a GR centre in the silicon film of an FD UTBOX SOI nMOSFET.

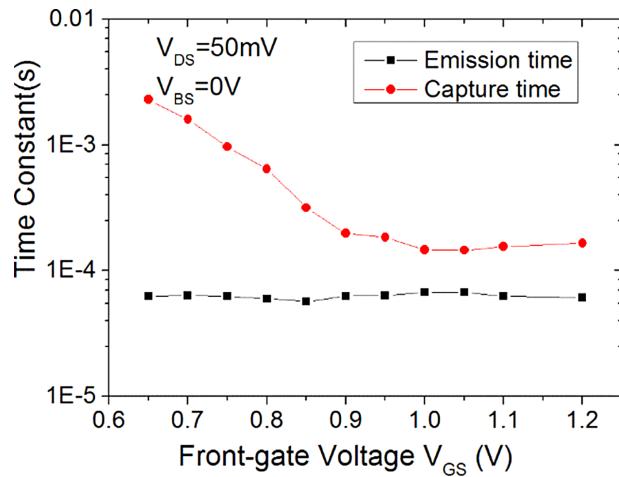


Figure 13 Time domain capture and emission time constant for a GR centre in the silicon film of an FD UTBOX SOI nMOSFET.

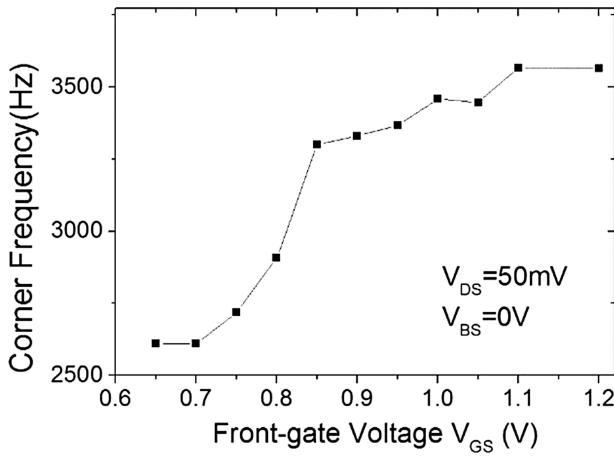


Figure 11 Corner frequency at different front-gate voltages for a GR centre in the silicon film of an FD UTBOX SOI nMOSFET.

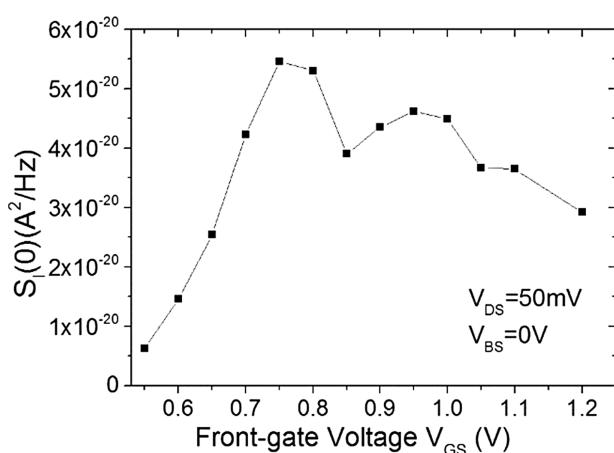


Figure 12 Plateau amplitude at different front-gate voltages for a GR centre in the silicon film of an FD UTBOX SOI nMOSFET.

dependence which has been identified as being typical for a silicon trap in UTBOX SOI nMOSFETs [13]. This behaviour can be understood in the frame of the SRH theory for the corner frequency, given by [10, 13, 20]

$$\begin{aligned}\tau &= 1/(2\pi f_c) \\ &= [c_n(n(x,y) + n_t) + c_p(p(x,y) + p_t)]^{-1}.\end{aligned}\quad (5)$$

In Eq. (5), c_n and c_p are the capture rates for electrons and holes, respectively, given by the product of the thermal velocity and the capture cross-section for electrons (holes) (σ_n or σ_p) and $n(x,y)/p(x,y)$ are the local free carrier densities, depending on the position of the trap (x,y) in the depletion region of the transistor. Based on Eq. (5), one can demonstrate that f_c is constant at low V_{GS} or, in other words, at low values of $n(x,y)$ for an nMOSFET (the hole terms can be neglected in Eq. (5) in most of the cases [13]).

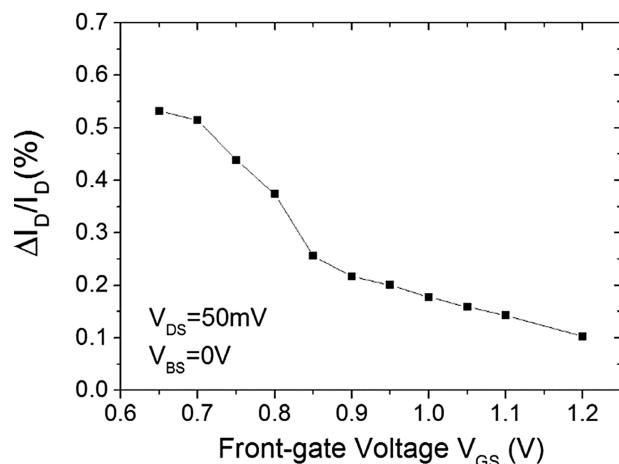


Figure 14 Time domain RTN relative amplitude for a GR centre in the silicon film of an FD UTBOX SOI nMOSFET.

Table 1 Variation of RTN and Lorentzian parameters for a gate oxide and a film trap with front-gate voltage in UTBOX SOI nMOSFETs, at constant V_{DS} .

parameter	gate oxide RTN	film RTN
τ_c	expon. decrease	moderate decrease
τ_e	slight increase	~constant
τ_c/τ_e	expon. decrease	~1
$\Delta I_D/I_D$	peak shaped	decrease
$S_l(0)$	decrease	const. + increase
f_c	expon. increase	moderate increase

In that case $2\pi f_c = 1/(c_n n_t)$, with n_t being the free electron concentration when the Fermi level is at the trap level E_T . With the increase of V_{GS} , $n(x,y)$ increases as well as f_c , like in Fig. 11. The variation of the plateau amplitude can be understood along the lines explained in [13].

The corresponding RTN parameters, displayed in Figs. 13 and 14 behave differently from the typical gate oxide trap RTN (Figs. 8 and 9). The time constants vary only moderately with the gate voltage, especially above 0.9 V, while their ratio is close to one in the same region. This can be explained by assuming that for $V_{GS} > 0.9$ V the quasi-Fermi level for electrons crosses the trap level somewhere in the silicon film, so that $\tau_c \sim \tau_e$. For smaller V_{GS} , as the channel carrier density decreases, the capture time increases. And for all gate bias, the emission time stays constant, indicating its insensitivity with gate bias or channel carrier density. The relative RTN amplitude reduces notably with increasing V_{GS} , different from what has been observed for the gate oxide trap in Fig. 9.

5 Summary and conclusion The foregoing results have been summarised in Table 1, showing the differences in parameter behaviour for a gate oxide and a film trap related Lorentzian and RTN. It is clear that mainly the capture time constant behaves differently in both cases and is most sensitive to the RTN trap position in the gate oxide or the silicon film. Further support for the trap identification in UTBOX SOI MOSFETs can come from measurements as a function of the temperature or with varying back-gate bias.

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