Interfacial conduction in organic ferroelectric memory diodes

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Solution-processed memory diodes based on phase separated blends of ferroelectric and semiconducting polymers in the low resistance on-state operate similar to a vertical field-effect transistor at the pinch-off. Numerical simulations have shown that the performance of the diode is dominated by the conduction of charge carriers at the interface between the semiconductor and ferroelectric phases. Here, we present an unambiguous experimental demonstration of the charge injection process in the diodes. We employ a modified diode structure, wherein the electrode in contact with the semiconductor phase has been intentionally removed. Even in the absence of an electrical contact with the semiconductor phase, the diode still shows resistance switching. We provide numerical simulations that reproduce the experimentally measured *I-V* characteristics and therefore confirm interfacial conduction in the diodes. Furthermore, we discuss the implications of the proposed memory structure particularly in the performance of light-emitting diodes with built-in memory functionality, i.e., MEMOLEDs. *Published by AIP Publishing.*
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Solution-processed organic memory diodes based on phase-separated blends of ferroelectric and semiconducting polymers are promising non-volatile memory candidates for flexible electronic applications.[1–8] The first 9-bit cross-bar memory array has been demonstrated in 2010 (Ref. 9) followed by the demonstration of a reconfigurable 1 kbit flexible memory array on a plastic foil in 2014.[10] To realize the storage medium, typically a blend solution of a semiconducting polymer (or a small conjugated molecule) and the ferroelectric random copolymer of poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] was prepared in a common solvent.[1,3,11–15] Thin films were realized by solution casting. The blend undergoes spinodal decomposition phase separation yielding a thin film with bicontinuous columnar semiconducting domains that are randomly distributed in the P(VDF-TrFE) matrix.[16–21] Resistance switching in the diodes was realized by deliberately choosing an injecting electrode that forms a Schottky contact with the semiconductor with a large barrier height, as schematically shown in Fig. 1(c). The ferroelectric polarization modulates the injection barrier [Fig. 1(d)], enabling reversible switching of the diode resistance between a non-volatile high-resistance off-state and a low-resistance on-state.[22,23]

Two-dimensional (2D) numerical models have quantitatively described the full hysteretic current-voltage (*I-V*) characteristics of the diodes as a function of both bias and temperature by combining the polarization-voltage response of the ferroelectric polymer with the charge injection and subsequent transport at the metal–organic semiconductor interface.[22,24,25] The model predicts the emergence of an in-plane component for ferroelectric polarization, which causes bending of the electric field lines near the semiconductor phase, as shown by dark-red arrows in Fig. 1(a). Hence, the electric field lines in the P(VDF-TrFE) phase in the vicinity of the semiconductor domain are no longer

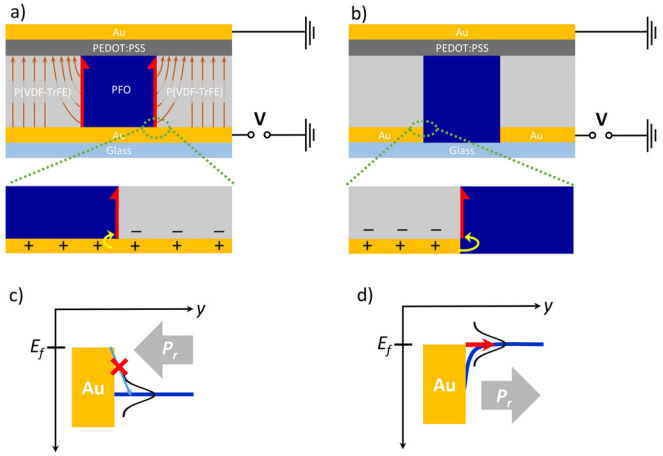

FIG. 1. (a) Conventional memory diode structure. Dark-red arrows show the electric field distribution in the P(VDF-TrFE) phase and the emergence of the in-plane electric field. The red-arrows show the confinement of the current to the PFO phase boundaries. (b) Bottom-contact-etched memory device structures. The zoom-in region shows the interface between the injecting contact and PFO|P(VDF-TrFE). Charges in the Au electrode and the P(VDF-TrFE) phases are shown for the on-state. The yellow-arrows show that charge injection takes place at the corner of the ternary interface. Both diode structures should exhibit the same switching behavior. Band diagram at the bottom gold contact with PFO for the diode in the (c) off-state and (d) on-state. The highest occupied molecular orbital (HOMO) of the PFO is shown as a thick blue line. The Gaussian DOS is centered at the HOMO level. In the off-state (c), the barrier is large and the charge injection is inefficient. In the on-state (d), the stray field lowers the injection barrier making tunneling of the carriers across the barrier very efficient.

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parallel to the interface and a lateral x-component of the electric field emerges. Therefore, a large stray electric field exists at the semiconductor (PVDF-TrFE) interface with the bottom contact that facilitates tunneling of the charge carriers and effectively lowers the barrier for charge injection. Due to the appearance of the x-component for the electric field, the injected charge carriers in the semiconductor are confined to the interface with the P(VDF-TrFE) phase, as schematically shown by the red arrows in Fig. 1(a). The theoretical 2D simulations have indicated that the memory diode is an interface device, wherein only a fraction of the contact just underneath the semiconductor|P(VDF-TrFE) interface, as shown in Fig. 1(a), is needed for the memory operation and that the charge transport takes place along the semiconductor|P(VDF-TrFE) interface. However, these key theoretical findings have not yet been proven experimentally.

Here, we unambiguously demonstrate charge injection from the contact point just beneath the semiconductor|P(VDF-TrFE) interface in the memory diodes. To this aim, we realized a modified memory device structure, shown in Fig. 1(b), where the part of the injecting bottom electrode in contact with the semiconductor is deliberately removed. Hence, the charge injection can take place only from the contact point under the semiconductor|P(VDF-TrFE) interface. P(VDF-TrFE) and poly(9,9-dioctylfluorene) (PFO) were used as the ferroelectric and the semiconductor polymer, respectively. We experimentally demonstrate that the memory diode shows a similar on-current upon switching of the ferroelectric polymer, while the off-current shows subtle but relevant differences. We further performed 2D numerical simulations taking the specific diode geometry into account. The model reproduced the experimentally measured I-V characteristics with an identical set of parameters for both diode geometries and further explains the origin of the observed off-state current. These findings can be used for further optimization of the memory devices and light-emitting diodes with built-in ferroelectric memory functionalities, i.e., the MEMOLEDs.[26,27]

The ferroelectric polymer [P(VDF-TrFE) (65%–35%)] was purchased from Solvay, Belgium. PFO was purchased from TNO, The Netherlands. Cyclohexanone was used as a common solvent and purchased from Sigma Aldrich. PEDOT:PSS (CLEVIOS P VP AI 4083) was purchased from Heraeus. All chemicals and polymers were used as received. A PFO:P(VDF-TrFE) solution in cyclohexanone, 4 wt. %, with a weight ratio of 1:9 was prepared.

Conventional memory diodes, Fig. 1(a), with Au (50 nm)/PFO:P(VDF-TrFE) (270 ± 10 nm)/PEDOT:PSS (70 nm)/Au (70 nm), were prepared according to previously published recipes.[18,22,28,29] The diodes in Fig. 1(a) were realized according to our previously reported works.[22,28] After deposition of the PFO:P(VDF-TrFE) blend film, in order to realize self-aligned etching mask for the gold bottom electrode, PFO columns and domains were selectively etched away using an orthogonal solvent,[17,30] e.g., hot toluene (60 °C) overnight. After drying, the substrates were immersed in a diluted solution of KI:I_2:H_2O (0.1:0.016 M or 0.05:0.008:27 mol ratio). The optimized etching time was 3 min to prevent severe gold underetching. P(VDF-TrFE) acted as a self-aligned etching mask for the bottom Au electrode. After the etching process, the substrates were thoroughly washed with deionized water and dried in a vacuum oven at 80 °C for 2 h. The holes in the P(VDF-TrFE) layer were subsequently back-filled with pure PFO (0.5 wt. % solution in toluene) using spin coating. After the PFO back-filling, the films were annealed. There was no apparent formation of a PFO ad-layer.[22,24] We note that the memory diodes also operate if an ad-layer is present provided that its thickness is below 70 nm.[31] The top electrodes were formed as explained previously.[22,28] The device area for all diodes amounted to 0.16 mm^2.

The surface morphology was probed using both a scanning electron microscope (SEM) and an atomic force microscope (AFM). The electrical characterization was performed in a vacuum (10^{-6} mbar) using an Agilent 4155B parameter analyzer. The work function of the Au bottom electrode was measured under atmospheric conditions using a Kelvin probe.

As the first step, the blend microstructure after thin-film formation was characterized. The top view SEM micrograph of the blend thin-film is given in Fig. 2(a), with the corresponding AFM height image given in the inset. The typical morphology of the phase-separated PFO:P(VDF-TrFE) is obtained, viz., PFO domains that are randomly distributed in the semi-crystalline P(VDF-TrFE) matrix.[18,22] The average diameter size of the PFO domains amounted to 300–500 nm. Figure 2(b) shows a typical SEM image of the film after selective removal of the PFO domains. The AFM height image shows that holes extend through the whole film thickness reaching the bottom contact. Next, the Au bottom electrode was etched away, back-filled with PFO, and subsequently annealed at 140 °C. A SEM image of the back-filled film is given in Fig. 2(c). The cross-sectional SEM image [inset of Fig. 2(c)] shows the complete back-filling of the holes. The backfilled PFO domains in Fig. 2(c) are larger than the PFO domains in Fig. 2(a) because for the backfilled case we have used an excess amount of PFO and therefore overfilled domains were obtained. Moreover, this overfill has

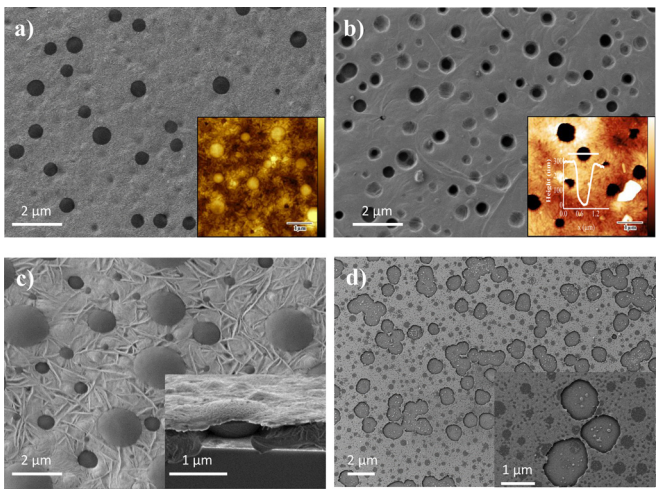

FIG. 2. (a) SEM images of the PFO:P(VDF-TrFE) 1:9 phase separated blend. The inset shows an AFM topography image. The height profile of the AFM image is from 0 to 70 nm. (b) SEM and AFM topography images of the films after PFO removal. The height profile of the AFM image is from 0 to 400 nm (excluding the bright area which corresponds to dust). The line profile shows that PFO domains are fully etched away. (c) Top- and cross-sectional view SEM images of a PFO back-filled film after annealing. (d) SEM image of an etched Au electrode.

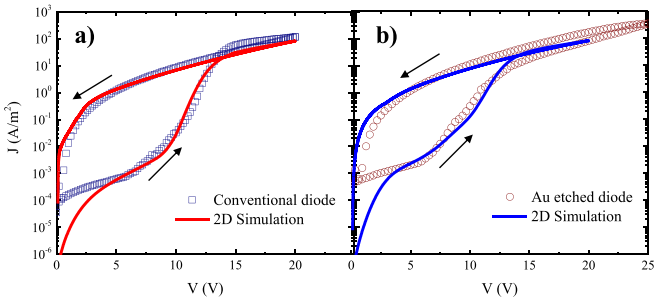

FIG. 3. Current-voltage characteristics of the (a) conventional diode with the device layout as shown in Fig. 1(a) and (b) diode with an etched gold bottom electrode, with the device layout as shown in Fig. 1(b). The solid lines are the results of the numerical 2D simulations.

no influence on the switching of the injection barrier since the switching experiment was done at the bottom contact. To inspect the morphology of the Au bottom electrode, the P(VDF-TrFE) masking layer was removed after the etching process by immersing the substrate in cyclohexanone overnight. A SEM image of the etched Au bottom contact is shown in Fig. 2(d). Au is partially etched only on the exposed positions of the removed PFO domains. Round holes are formed in the Au bottom electrode and the glass substrate is exposed. The size of the regions without gold is slightly bigger than the size of the removed PFO columns which could be due to slight underetching of gold.

The *I-V* characteristics of a conventional diode are shown in Fig. 3(a). The top electrode is biased at 0 V, while the voltage applied to the bottom Au electrode is swept from 0 V to +20 V and back from +20 V to 0 V. Since Au forms an injection-limited contact to PFO, at low bias, the current density is low, the resistance is high and therefore the diode is in the off-state. As the positive bias increases, P(VDF-TrFE) slowly polarizes. As the bias goes beyond the coercive voltage, here about 13 V (nearly 50 MV/m close to the coercive field of the ferroelectric phase), P(VDF-TrFE) is fully polarized, the current increases and hence the resistance is lowered by several orders of magnitude. Upon sweeping the bias back to 0 V, the ferroelectric polarization is maintained and the diode remains in the on-state. Application of a negative bias larger than the negative coercive voltage sets back the diode again in the off-state.

Interestingly, as shown in Fig. 3(b), the diode with the etched Au bottom contact shows hysteretic *I-V* characteristics similar to that obtained from the conventional diode. To be more precise, the on-current is basically the same, while the off-current is slightly higher, the origin of which shall be addressed later. Demonstration of hysteretic *I-V* characteristics for the diode with the modified geometry is an unambiguous experimental proof that the charge injection takes place at the ferroelectric|semiconductor interface and that organic ferroelectric memory diodes are interface devices.

To pinpoint the origin of the increased off-state current, we performed two-dimensional (2D) simulations for both of the diode structures, taking into account the diode geometries, particularly the configuration at the injecting contact. The model[22] takes into account the dynamic behavior of the ferroelectric polarization with the applied bias and couples that with the charge injection and transport through the semiconductor phase.[32–42] Detailed discussion of the model parameters is given in our previous report.[22] The calculated *I-V* characteristics at room temperature are given in Fig. 3, as solid lines, for diodes with a conventional and a contact-etched structure. We used the same set of physical parameters for both diodes, such as mobility and hopping distance. The simulations predict the on-state and off-state currents for both diode geometries as well as the full hysteric *I-V* loop.

The model pinpoints the origin of higher off-state current in the diode with etched contact. In the off-state, the stray field at the injecting bottom electrode is pointing in an opposite direction. Carrier tunneling does not take place and the contact remains injection limited. The electric field is maximum in the central part of the Au bottom contact. As a result, the off-state current is low and, as is shown in Fig. 4(a), it is limited to the central region of the contact. In contrast, in the case of the diode with an etched contact, the stray field at the interface of Au|P(VDF-TrFE) with PFO leads to a slightly improved charge injection and therefore a higher current is transported through the middle of the PFO phase, as shown in Fig. 4(b). The fact that charges can be injected from the edge is very similar to the case of vertical field effect transistors.[43–47] It is interesting to see that the numerical model nicely captures this point and produces a good fit to the experimentally measured *I-V* characteristics [Fig. 3(b)].

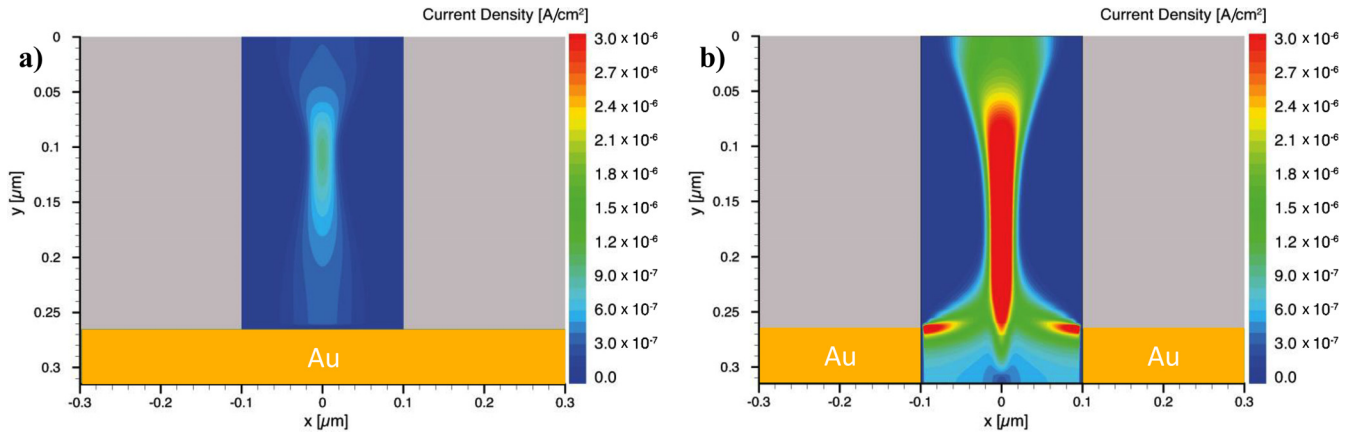

FIG. 4. Off-state current density calculated using 2D numerical simulations at the bias level of 5 V for (a) a conventional diode structure and (b) a diode with etched Au contact.

We have unambiguously demonstrated that the stray field at the interface of the injecting contact at the semiconductor|ferroelectric interface dominates the operation of the memory diode. To do so, a diode structure has been realized, wherein the injecting electrical contact at the semiconductor was deliberately removed. Hence, the charge injection could only take place at the semiconductor|ferroelectric|contact interface. The memory diode with a modified contact showed the same performance as a conventional diode. The memory operation mechanism, specifically the off-current, was elucidated by performing 2D numerical simulations. Moreover, removal of the major part of the contact area and the side contacting the semiconductor phase may have a major impact, particularly on the performance of the MEMOLED, an organic light-emitting diode with a built-in switch. One drawback of the MEMOLED design is that it relies on semi-transparent Au electrodes, which lead to at least 50% light loss.[26,48] To prevent these optical losses, transparent contacts are required. The proposed device structure is therefore ideally suited for the MEMOLEDs to enhance the light output since the semi-transparent Au contact under the PFO phase is completely removed.

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