Electrical characteristics of W-Si(100) Schottky barrier junctions

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The electrical characteristics of W-Si(100) Schottky barrier junctions formed by sputter deposition of W on both *n*- and *p*-type Si(100) have been measured in the temperature range 95–295 K using current-voltage and capacitance-voltage techniques. Auger electron and Rutherford backscattering spectroscopies were used to characterize the Si(100) surface prior to metal deposition, and to monitor the reaction between W and Si upon annealing. The results showed that initial silicide formation has very little or no effect on the barrier height. Annealing after initial silicide formation caused the junction characteristics to strongly deviate from the ideal thermionic emission behavior. For junctions with ideal thermionic emission behavior the barrier height was found to decrease with increasing temperature with a coefficient consistent with the predictions of recent models of barrier formation based on Fermi-level pinning in the center of the semiconductor indirect band gap.

I. INTRODUCTION

The role of chemical reactivity at metal-silicon interfaces in determining the Schottky barrier height has been emphasized by several authors.[1,2] Attempts to correlate barrier heights with measured quantities such as silicide heat of formation[1] and metal-Si eutectic temperature[3] have revealed many trends, without, however, elucidating the underlying mechanisms of barrier formation.

Schottky barrier heights are known to depend only weakly on the metal used, i.e., the Fermi level is pinned at the interface by states in the semiconductor band gap. The existence and nature of these interface states have become the central issues for the understanding of Schottky barrier formation. Surface electron spectroscopy studies on the near-noble metal Pd and Pt silicide-Si interfaces[4,5] have provided some evidence for the existence of interface states which appear to be associated with distinct metal-Si bonds formed at the interfaces as a result of silicide formation reaction. However, these spectroscopy techniques do not have the required sensitivity and energy resolution (less than 0.1 eV) to detect the presence of a small amount of band-gap states [(10^{13}–10^{14}) e/eV cm^2] which would be sufficient to pin the Fermi level and determine the barrier height. Therefore, the density and energy distribution of these states cannot be accurately measured to assess their role in determining the barrier height of the interfaces. Recently, attempts have been made to measure the density and energy distribution of electronic states at silicide-Si interfaces using capacitance spectroscopy techniques.[6] Ho *et al.*[6] measured capacitances in excess of the space-charge capacitances of forward-biased Pd and Ni silicide-Si Schottky contacts, and interpreted them as due to interface states associated with structural defects in Si at, or very close to, the interfaces. Werner, Ploog, and Quiesser,[7] however, argued that the excess capacitances measured in such experiments are not caused by interface states but instead by minority carriers injected into the bulk semiconductor, giving rise to excess diffusion capacitances. This then leaves open the question of what was observed by Ho *et al.*[6] The observations of these authors could only be accepted as the observations of interface states whose occupation is altered by the semiconductor quasi-Fermi level, i.e., of states which equilibrate with the semiconductor rather than the metal, which are of insufficient density to strongly affect band alignments at the interfaces.[8] If, on the other hand, the density of these states is sufficiently high to strongly affect band alignment, then this would lead to an increase in barrier heights from its initial value as forward voltage increases, resulting in current-voltage nonidealities, i.e., in a voltage-dependent ideality factor.[8,9] This is, however, contradicted by the experimental results,[10] and thus raises a fundamental question concerning whether the observed defect states play any role in determining the barrier height of such silicide-Si interfaces.

In the case of near-noble metals such as Pd and Pt on Si, interfacial reaction occurs at room temperature even in the presence of native oxides on the Si surfaces,[5] and as a result, it is unclear if the metal itself has the same barrier height as it silicides. In the case of refractory metals such as Ti on Si, where no measurable reaction occurs at room temperature,[11] silicide formation has been found to result in only a small change in barrier height of less than 0.1 eV.[12] Recently, we have also found that for W on Si(100), initial silicide formation has very little or no effect on the barrier height. It is therefore the intention of this paper to present measurements of Schottky barrier height for W and its silicides on Si(100). Barrier-height measurements on both *n*- and *p*-type Si(100) were carried out using current-voltage and capacitance-voltage techniques at temperatures ranging from 95 to 295 K.

II. EXPERIMENTAL DETAILS

The samples used in the present study were prepared by depositing 100–1500-Å W films simultaneously on 0.005-Ω cm n^+ and p^+ (100)-oriented Si wafers with 2-μm-thick, 10-Ω cm *n*- and *p*-type epitaxial layers, respectively. The W films were deposited using dc magnetron sputtering. The deposition chamber was evacuated to $\sim 8\times10^{-8}$ Torr prior

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to the introduction of high-purity (99.999%) argon to a pressure of 10 mTorr. The target was sputter cleaned at a potential of 450 V for 1 min prior to sputter deposition. The W films were deposited at a target potential of 450 V, resulting in a deposition rate of about 10 Å/s. The substrates were grounded during film deposition. The resistivity of the W films was 20–30 $\mu\Omega$ cm. A chemical cleaning procedure including a final dip in diluted HF, described by Taubenblatt, Thomson, and Helms,[13] was used to prepare the Si surface immediately prior to inserting the wafers into the deposition chamber. Auger electron spectroscopy (AES) was used to determine the effect of Si surface preparation on surface contaminant levels. Such a cleaning procedure was found to leave less than a monolayer of oxygen, and approximately one monolayer of carbon on the Si(100) surfaces.[13] During the same deposition, the following samples were made: bare Si samples for AES, and Rutherford backscattering spectroscopy (RBS), thermal SiO_2-covered Si samples with opening for current-voltage (I-V) characteristics, and bare Si samples held under a metal mask with openings of 1 and 2 mm diam. For the I-V measurements the deposition was made through a metal mask having 2.5-mm-diam holes, but the active areas of the diodes were defined by oxide openings with diameters of 129, 253, 505, and 1003 μm. The samples were processed together and annealed in the temperature range 773–1073 K for interfacial reaction in a continuous flow of helium purified both over Ti at 1123 K and then over Zr at 923 K.

RBS was used to examine in-depth compositional variation in the reacted samples, and AES coupled with Ar^+ ion sputtering at an estimated rate of $\sim$1 Å/min was used to examine compositional redistribution in the interfacial region upon annealing.

Schottky barrier height (SBH) values for n- and p-type Si(100) were determined by extrapolating the forward I-V characteristics to zero applied voltage. The extrapolation was made by a linear fit over two order of magnitude or greater of current on the semilog I-V characteristics. The measurements were made on all diode areas with samples held at temperatures in the range 95–295 K. SBH values were also determined from the activation energy analysis[14] of $\ln(J_F/T^2)$ vs $1/T$, where J_F is the saturation current density at zero applied voltage measured in the temperature range 95–295 K. SBH values were also determined from the capacitance-voltage (C-V) characteristics by extrapolating the linear portion of the $1/C^2$-vs-V data to the intercept on the voltage axis. The C-V measurements were made at 1 MHz, and with the samples held at temperatures in the range 95–295 K.

III. RESULTS

A. W-Si(100) reaction

Auger depth-composition profiles for the as-deposited and annealed samples are shown in Fig. 1. Figure 1(a) shows that the oxygen and carbon concentrations in the bulk of the as-deposited film and at its interface with Si are below the detectability limit of AES ($\leqslant$1 at. %). Annealing the

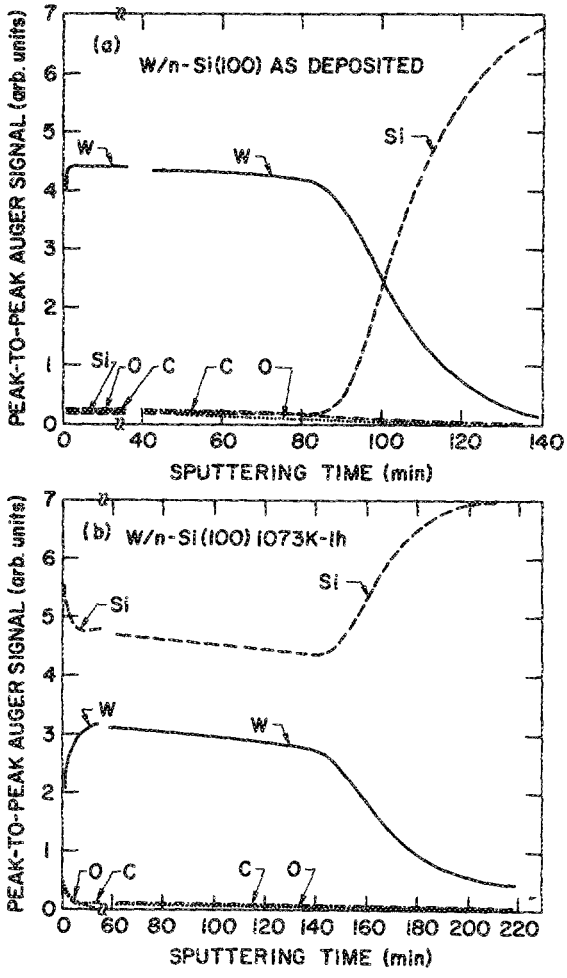


FIG. 1. Auger depth-composition profiles of $\sim$100 Å W film on n-type Si(100): (a) as-deposited and after annealing at (b) 1073 K for 1 h. W MNN(1736 eV), Si LVV(92 eV), O KLL(512 eV), and C KLL(272 eV) Auger transitions were monitored in the composition profiling. The sputtering rate was $\sim$1 Å/min.

samples up to 973 K for 1 h produce no compositional redistribution in the interfacial region as measured with a depth resolution of $\sim$20 Å, indicating that no extensive reaction such as atomic intermixing and silicide formation has occurred. However, upon further annealing to 1073 K, compositional redistribution occurred in the interfacial region. Extending the annealing at 1073 K to 1 h caused the W to fully react [see Fig. 1(b)]. RBS measurements showed that the silicide phase present after 1073 K annealing is WSi_2.

B. Schottky barrier heights

1. n-type Si(100)

The forward I-V characteristics plotted in Fig. 2(a) as a function of temperature show examples of the results obtained for samples in the as-deposited state. In Fig. 3 are shown the $1/C^2$-V characteristics measured on these samples. The samples exhibit linear $1/C^2$-vs-V plots to 5 V, indicating a uniform donor distribution. However, an increase in slope with decreasing temperature is observed, indicating partial donor compensation by deep levels which are most

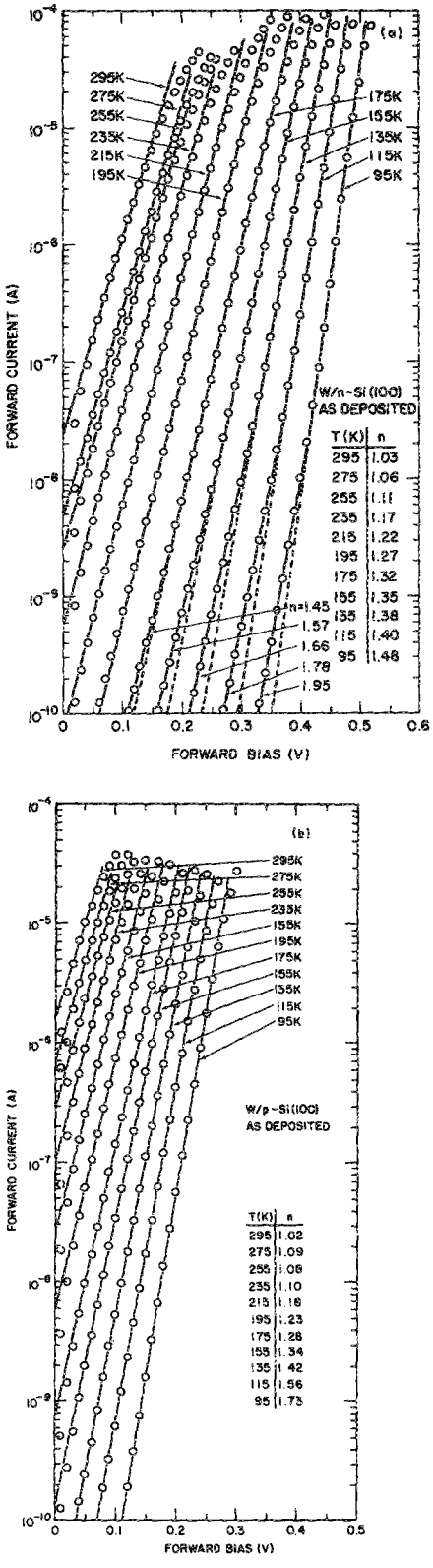


FIG. 2. Forward current-voltage characteristics of W on (a) n-type Si(100) and (b) p-type Si(100) as a function of temperature for samples in the as-deposited state. The diode area is 1.31×10^{-4} cm^2.

likely introduced into the Si substrate during the sputter-deposition process.[12] Values of the zero-bias diffusion potential V_D, the doping density N_d, and the corresponding bulk Fermi level ϕ_F, determined from these measurements as

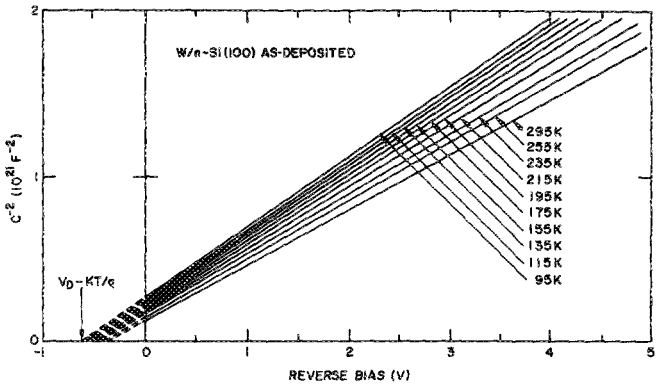


FIG. 3. $1/C^2$-V characteristics of W on n-type Si(100) measured at 1 MHz as a function of temperature for samples in the as-deposited states.

functions of temperature, are summarized in Table I. The value of N_d at 295 K is consistent with the donor concentration of the starting material. The data in Table I show that $(V_D+\phi_F)$ increases with decreasing temperature, and that the change in $(V_D+\phi_F)$ with temperature can be accounted for by the corresponding change in the indirect energy gap of silicon.[15]

It can be seen from Fig. 2(a) that above 255 K, the samples display a good ideality factor which remains essentially unchanged with temperature. Below 255 K, however, the ideality factor increases as the temperature is lowered, reaching a value of 1.48 at 95 K. This temperature dependence of the ideality factor is found to have the form $n=1+(T_0/T)$, where T_0 is a constant, independent of temperature. Figure 4 shows $nKT/q=K(T+T_0)/q$ plotted against KT/q. It is evident that the data can be fitted with a straight line parallel to the unity slope line. The value of T_0 for these samples is found to be 50 K. In addition, the dependence of $\ln(J_F/T^2)$ on $1/T$ is not linear in the temperature range 95–295 K; however, if $\ln(J_F/T^2)$ is plotted against $1/nT$, a straight line is obtained with a slope giving an activation energy of 0.72 eV, as shown in Fig. 5. This shows that J_F can be described by

$$J_F=A^*T^2\exp[q\phi_{Bn}/K(T+T_0)], \tag{1}$$

where A^* is the effective Richardson constant and ϕ_{Bn} is the n-type barrier height. Several authors found similar results for other Si,[16] GaAs,[17] and InP (Ref. 18) Schottky barriers.

TABLE I. Values of V_D, N_d, and ϕ_F, determined from C-V measurements on n-type samples in the as-deposited state as a function of temperature.

T (K)	V_D (V)	N_d (10^{14} cm^{-3})	ϕ_F (V)	$(V_D+\phi_F)$ (V)
295	0.391	5.867	0.273	0.664
255	0.435	5.582	0.233	0.668
215	0.489	5.172	0.193	0.682
175	0.536	4.916	0.153	0.689
155	0.559	4.827	0.133	0.692
135	0.583	4.755	0.114	0.697
95	0.628	4.621	0.076	0.704

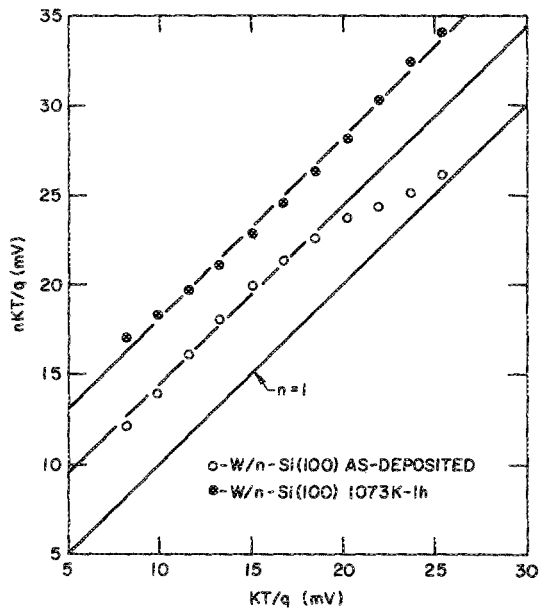


FIG. 4. Temperature dependence of the ideality factor for n-type samples in the as-deposited state (open circles) and after annealing at 1073 K for 1 h (solid circles).

Many efforts have been made to explain such a temperature dependence of the ideality factor in terms of particular distribution of interface state,[16,19] nonuniformly doped surface layer,[20] and tunneling.[21] It is quite possible that the temperature dependence observed in the present work may be attributable to a particular distribution of interface states. It can also be seen from Fig. 2(a) that a region of the forward characteristics with a higher value of ideality factor becomes more clearly evident at low voltages as the temperature is lowered below 175 K. A plot of $\ln(J_F/T^2)$, obtained by extrapolating the low-voltage linear region of the forward characteristics to zero applied voltage, versus $1/T$ (not shown here) in the temperature range 95–175 K yielded a straight line with a slope giving an activation energy of 0.26 eV. This low value of activation energy is evidently associated with recombination in the depletion region which causes deviation from thermionic emission behavior at low voltages and low temperatures.[14] It is to be noted that the barrier-height values calculated using Eq. (1) are in very good agreement with those determined from the C-V measurements (see Table I and Fig. 6). Moreover, from the open circles shown in Fig. 6, it can be seen that the barrier height calculated using Eq. (1) decreases with increasing temperature, consistent with the reported negative temperature dependence of the barrier height to n-type silicon.[12]

The forward I-V characteristics obtained after annealing the samples at 773 K for 1 h are shown in Fig. 7(a). Above 235 K, the ideality factor remains essentially unchanged wth temperature, while below 235 K, it increases with decreasing temperature. Again, this temperature dependence is found to have the form $n = 1 + (T_0/T)$, with T_0 having a value similar to that for the as-deposited samples. Moreover, a plot of $\ln(J_F/T^2)$ vs $1/T$ is not a straight line, whereas a plot of $\ln(J_F/T^2)$ vs $1/nT$ is a straight line in the

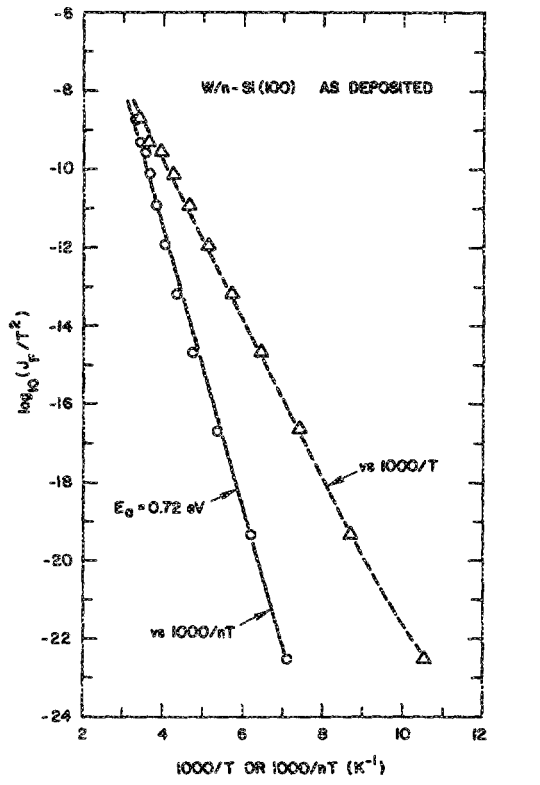


FIG. 5. Temperature dependence of forward current for n-type samples in the as-deposited states.

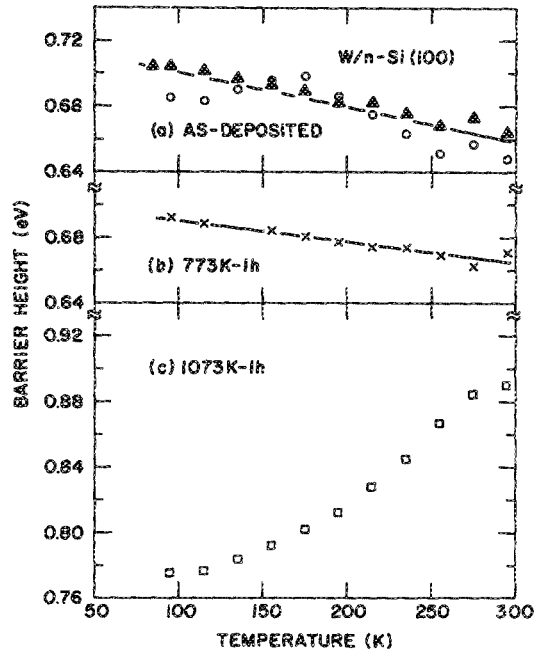
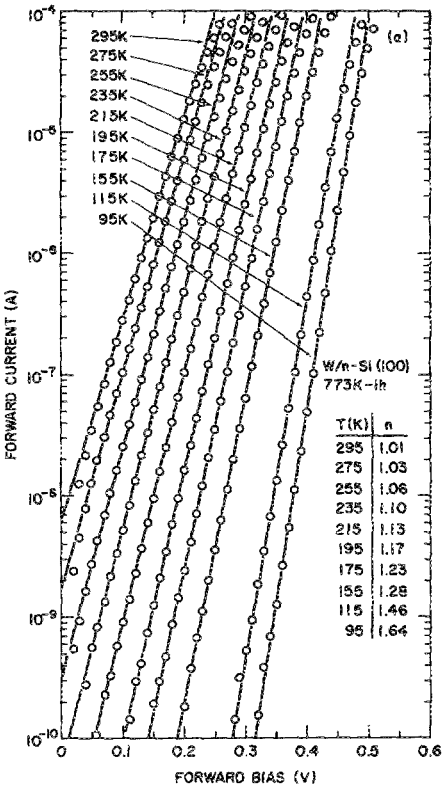


FIG. 6. Change of the barrier height of W on n-type Si(100) as a function of temperature for (a) as-deposited samples and samples annealed at (b) 773 K for 1 h, and (c) 1073 K for 1 h. Solid triangles: barrier-height values determined from C-V measurements. Open symbols and crosses: barrier-height values determined from I-V measurements. Solid lines: least-squares fit to the experimental data assuming a linear variation for ϕ_{Bn} from 95 to 295 K.



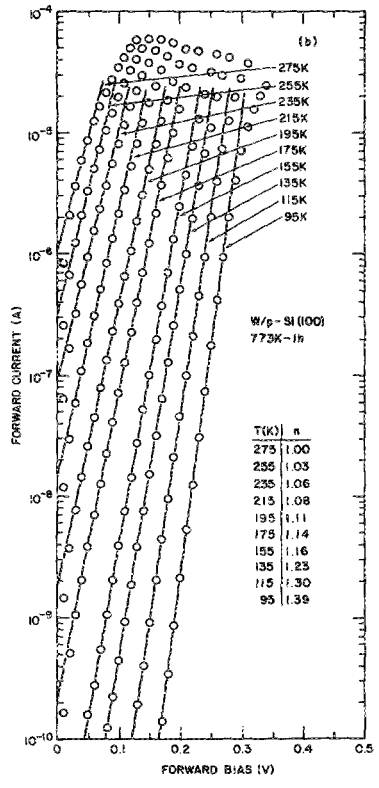


FIG. 7. Forward current-voltage characteristics of W on (a) n-type Si(100) and (b) p-type Si(100) as a function of temperature for samples annealed at 773 K for 1 h. The diode area is 1.31×10^{-4} cm^2.

temperature range 95–295 K with a slope giving an activation energy of 0.72 eV, as shown in Fig. 8. It is also clear from the crosses in Fig. 6 that in these samples the barrier height calculated using Eq. (1) decreases with increasing temperature.

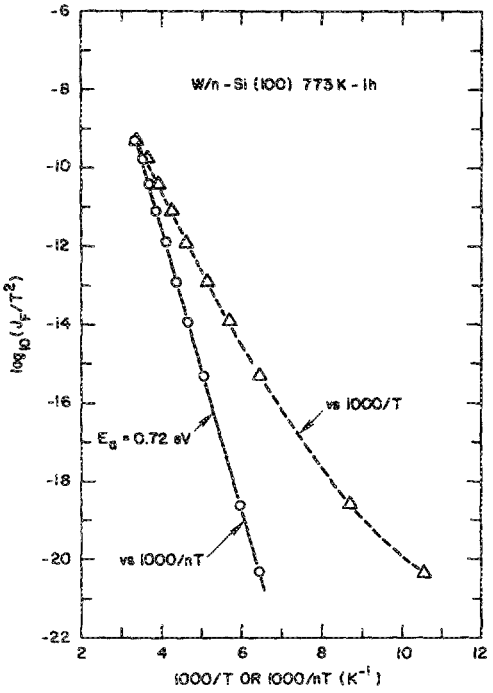
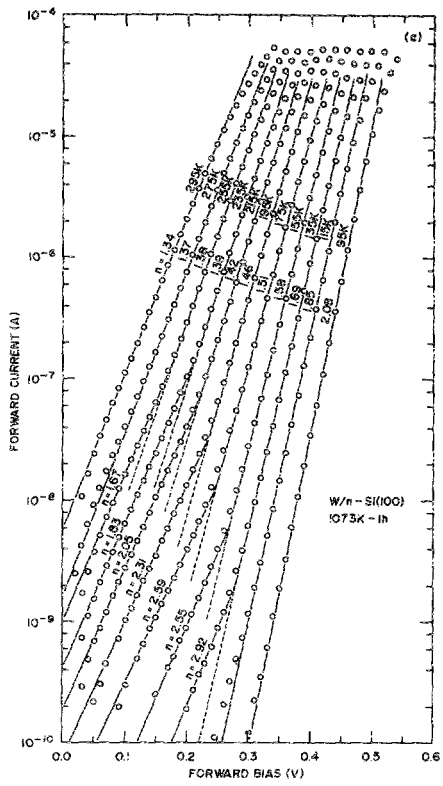


FIG. 8. Temperature dependence of forward current for n-type samples annealed at 773 K for 1 h.

The forward I-V characteristics plotted in Fig. 9(a) show the results obtained after further increasing the annealing temperature to 1073 K. The samples display a high ideality factor which increases with decreasing temperature, reaching a value of 2.08 at 95 K. Figure 5, however, shows that the data of $K(T+T_0)/q$ against KT/q can be fitted with a straight line parallel to the unity slope line. The value of T_0 for these samples is found to be 100 K. In addition, the dependence of $\ln(J_F/T^2)$ on $1/T$ is not linear, whereas the dependence of $\ln(J_F/T^2)$ on $1/nT$ is linear in the temperature range 95–295 K with a slope giving an activation energy of 0.65 eV, as shown in Fig. 10. However, if Eq. (1) is used to calculate the barrier height, the barrier height is found to increase with increasing temperature as shown by the open squares in Fig. 6. This is most likely due to recombination in the depletion region causing deviations from thermionic emission behavior which become more pronounced as the temperature is lowered.[14] This temperature dependence is in obvious disagreement with the reported negative temperature dependence of the barrier height to n-type silicon.[12]

The $1/C^2$-V characteristics measured on the 1073-K annealed samples are shown in Fig. 11. The samples exhibit nonlinear plots at all measured temperatures. It is to be noted that a silicide phase is formed after annealing at 1073 K for 1 h [see Fig. 1(b)]. The interdiffusion of W and Si during the silicide-formation reaction inevitably leads to the generation of point defects in the Si substrate, e.g., vacancies and/or interstitials; deep levels associated with such defects can act as recombination-generation centers or as traps and hence can strongly influence the current and capacitance characteristics of the metal-Si junction. The voltage-dependent slope observed in the $1/C^2$-V relationship is then likely due to the effects of such defect levels as pointed out by



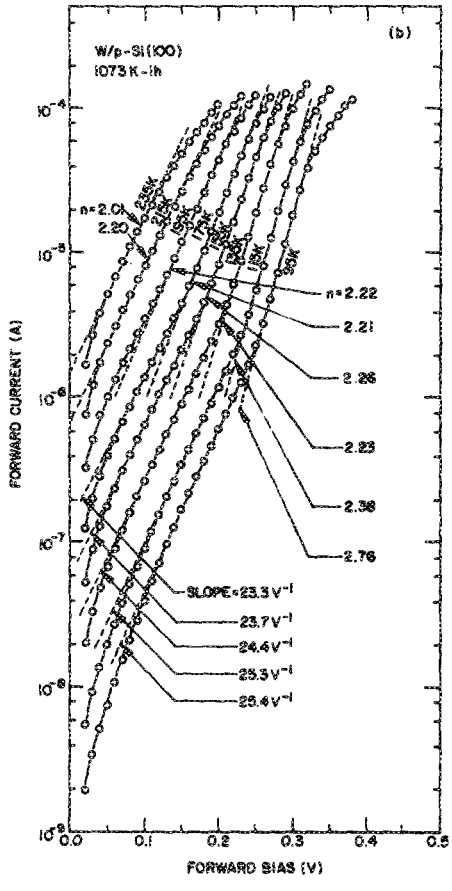


FIG. 9. Forward current-voltage characteristics of W on (a) n-type Si(100) and (b) p-type Si(100) as a function of temperature for samples annealed at 1073 K for 1 h. The diode area is 1.31×10^{-4} cm^2.

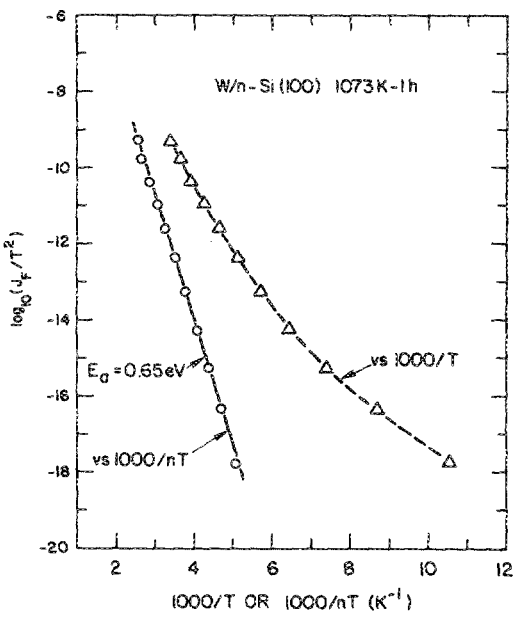


FIG. 10. Temperature dependence of forward current for n-type samples annealed at 1073 K for 1 h.

Roberts and Crowell[22] in their discussion of the capacitive effect of impurity levels in Si Schottky barriers. In these samples, it was therefore not possible to obtain reliable values for the barrier height from these measurements. However, it was found that with shorter silicide-formation reaction time (10 min at 1073 K), the samples displayed near ideal thermionic emission behavior at and above 195 K. In these samples the barrier height was found to have a value of 0.65 eV at 295 K, consistent with the results reported by Crowell, Sarace, and Sze[23] and by Itoh and Hashimoto[24] for WSi_2 formed on n-type Si(111) at and below 1323 K in 10 min. However, Itoh and Hashimoto,[24] using photoelectric measurements, found the barrier-height value to change (from 0.68 to 0.83 eV) with changing reaction time and temperature. The present results and those previously reported then lead to the question concerning the effect of annealing after initial silicide formation on the electrical characteristics of the W-Si(100) junction.

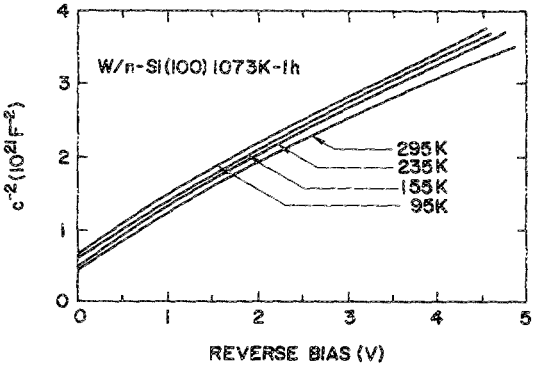


FIG. 11. $1/C^2$-V characteristics of W on n-type Si(100) measured at 1 MHz as a function of temperature for samples annealed at 1073 K for 1 h.

It can be seen from Fig. 9(a) that a region of the forward characteristics with a higher value of ideality factor is clearly evident at low voltages in the temperature range 135–255 K. An interesting feature of the forward characteristics in this region is that the slope of the $\ln J_F$-V plot (27–29 V^{-1}) is almost independent of temperature. However, a plot of $\ln J_F$, obtained by extrapolating the low-voltage linear region of the forward characteristics to zero applied voltage, versus T was found to be nonlinear, whereas a plot of $\ln(J_F/T^2)$ vs $1/T$ (not shown here) was linear in this temperature range with a slope giving an activation energy of 0.16 eV. Since nT is more or less constant, and $\ln J_F$ vs $1/nT$ was found to be a vertical plot,[25] thermionic-field emission can be ruled out as a possible mechanism in this region. Field emission is also most unlikely, since it would be expected to be significant only at very low temperatures in the lightly doped material used in the present work.[14] A temperature-independent slope of the $\ln J_F$-V plot and linear relation between $\ln J_F$ and T point to multistep tunneling[26] as a possible mechanism. The activation energy of 0.16 eV may then be associated with multistep tunneling in combination with recombination at low voltages in the temperature range 135–255 K.

2. p-type Si(100)

The forward I-V characteristics plotted in Fig. 2(b) as a function of temperature show examples of the results obtained for samples in the as-deposited state. In Fig. 12 are shown the $1/C^2$-V characteristics measured on these samples. The samples exhibit linear plots to 5 V, indicating a uniform acceptor distribution. Values of V_D, N_a, and the corresponding bulk Fermi level ϕ_F, determined from these measurements as a function of temperature, are summarized in Table II. The value of N_a at 295 K is consistent with the acceptor concentration of the starting material. The data in Table II show that $(V_D + \phi_F)$ increases with decreasing temperature, and that such a change can be accounted for by the corresponding change in the indirect energy gap of silicon with temperature.[15]

It can be seen from Fig. 2(b) that the samples display an ideality factor which increases with decreasing temperature, reaching a value of 1.73 at 95 K. In contrast to the n-type samples, the data of nKT/q against KT/q cannot be well fitted with a straight line parallel to the unity slope line, as shown in Fig. 13(a). However, if n is plotted against $1/T$, a straight line is obtained as shown in Fig. 13(b), thus showing that n has the form $n = \alpha + \beta/T$, where α and β are constants. In addition, a plot of $\ln(J_F/T^2)$ vs $1/T$ is not linear, whereas a plot of $\ln(J_F/T^2)$ vs $1/nT$ is linear in the temperature range 95–295 K with a slope giving an activation energy of 0.47 eV, as shown in Fig. 14. This shows that for p-type samples, J_F can also be described by Eq. (1). However, if Eq. (1) is used to calculate the barrier height, the barrier height is found to increase with increasing tem-

TABLE II. Values of N_D, N_a, and ϕ_F, determined from C-V measurements on p-type samples in the as-deposited states as a function of temperature.

T (K)	V_D (V)	N_a (10^{15} cm^{-3})	ϕ_F (V)	$(V_D + \phi_F)$ (V)
255	0.342	1.075	0.196	0.538
235	0.364	1.067	0.178	0.542
195	0.396	1.038	0.144	0.540
175	0.414	1.031	0.127	0.541
145	0.443	1.022	0.102	0.545
115	0.470	1.012	0.077	0.547
95	0.486	1.006	0.061	0.547

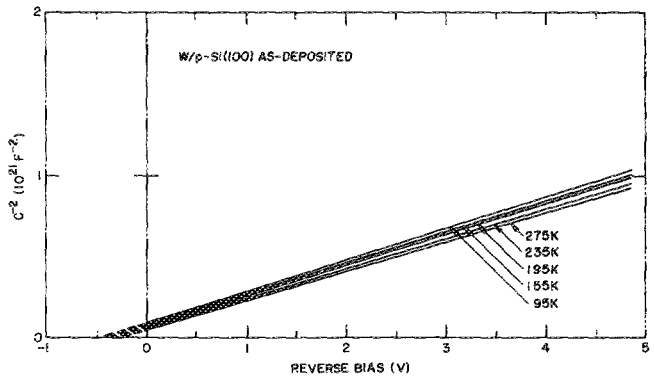


FIG. 12. $1/C^2$-V characteristics of W on p-type Si(100) measured at 1 MHz as a function of temperature for samples in the as-deposited state.

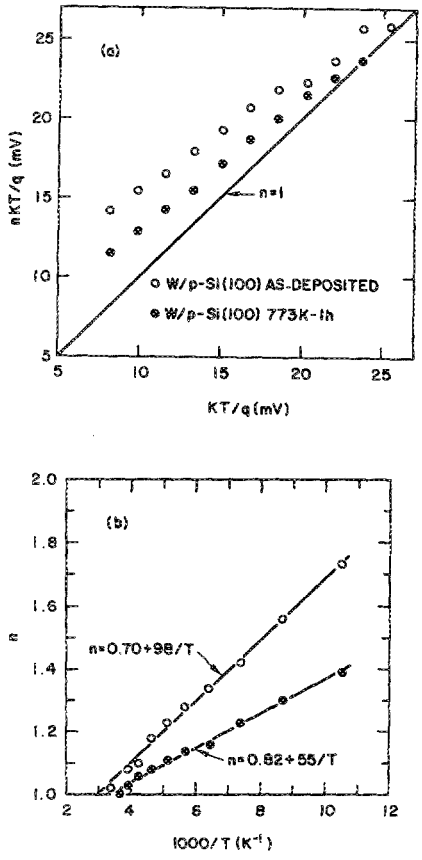


FIG. 13. (a) Temperature dependence of the ideality factor for p-type samples in the as-deposited state (open circles) and after annealing at 773 K for 1 h (solid circles). (b) Ideality factor vs 1/T for the samples as in (a).

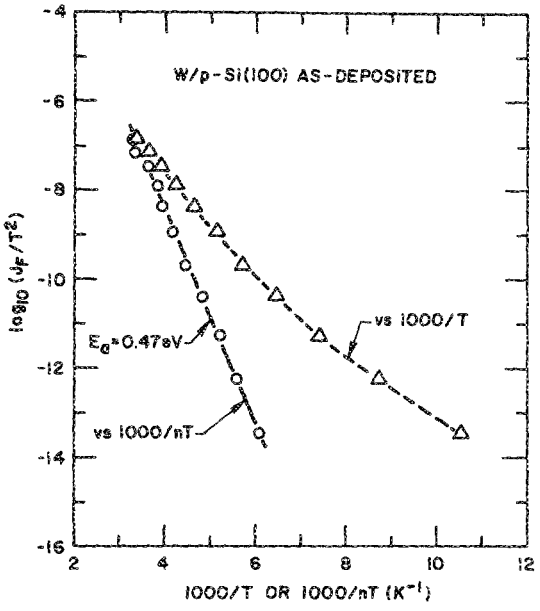


FIG. 14. Temperature dependence of forward current for p-type samples in the as-deposited state.

perature as shown by the open circles in Fig. 15, in disagreement with the reported negative temperature dependence of the barrier height to the p-type silicon.[12] Below 295 K, the reverse current was found to be proportional to $(V_D + V - KT/q)^{1/2}$, indicating that recombination-generation becomes relatively more important with decreasing temperature. This temperature dependence can therefore be attributed to recombination in the depletion region which causes deviations from thermionic emission behavior at low temperatures. On the other hand, it can be seen from the solid triangles shown in Fig. 15 that the barrier height determined from the C-V measurements decreases with increasing temperature. It is to be noted also that at 295 K, the barrier-height values calculated using Eq. (1) are in good agreement with those determined from the C-V measurements.

The forward I-V characteristics obtained after annealing the samples at 773 K for 1 h are shown in Fig. 7(b). The samples display an ideality factor which increases with decreasing temperature, reaching a value of 1.39 at 95 K. Again, a plot of n vs $1/T$ is a straight line, showing that n still has the form $n = \alpha + \beta/T$ [see Figs. 13(a) and 13(b)]. Moreover, the dependence of $\ln(J_F/T^2)$ on $1/T^2$ is not linear, whereas the dependence of $\ln(J_F/T^2)$ on $1/nT$ is linear in the temperature range 95–295 K with a slope giving an activation energy of 0.47 eV, as shown in Fig. 16. It is clear from the crosses shown in Fig. 15 that in these samples the barrier height calculated using Eq. (1) decreases with increasing temperature. These results thus indicate that recombination becomes somewhat less important after annealing at 773 K, and further suggest that the deviation of α from unity is caused by recombination in the depletion region.

The forward I-V characteristics plotted in Fig. 9(b) show the results obtained after further increasing the annealing temperature to 1073 K. An interesting feature of these characteristics is that for voltages less than 0.2 V, the slope of the $\ln J_F$-V plot is almost independent of temperature in the range 95–195 K, and consequently nT is more or less constant. In addition, $\ln J_F$ at 0.1 V is found to vary linearly with T rather than $1/T$ in this temperature range, as shown in Fig. 17(b), indicating that an activation energy is not involved in the dominant current mechanism. These features suggest multistep tunneling[26] as a possible mechanism in the temperature range 95–195 K. Such a mechanism gives the forward I-V characteristics a form represented by

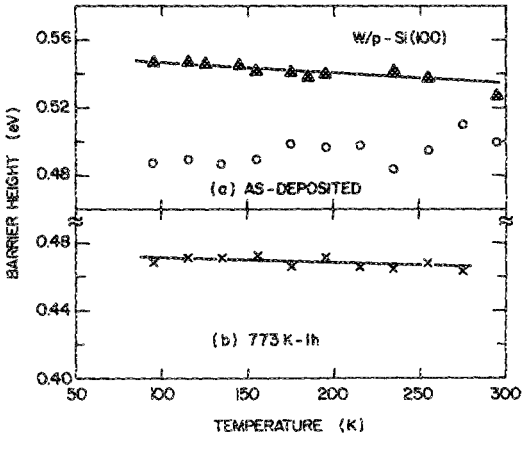


FIG. 15. Change of the barrier height of W on p-type Si(100) as a function of temperature for (a) as-deposited samples and samples annealed at (b) 773 K for 1 h. Solid triangles: barrier-height values determined from C-V measurements. Open circles and crosses: barrier-height values determined from I-V measurements. Solid lines: least-squares fit the experimental data assuming a linear variation for ϕ_{Bp} from 95 to 295 K.

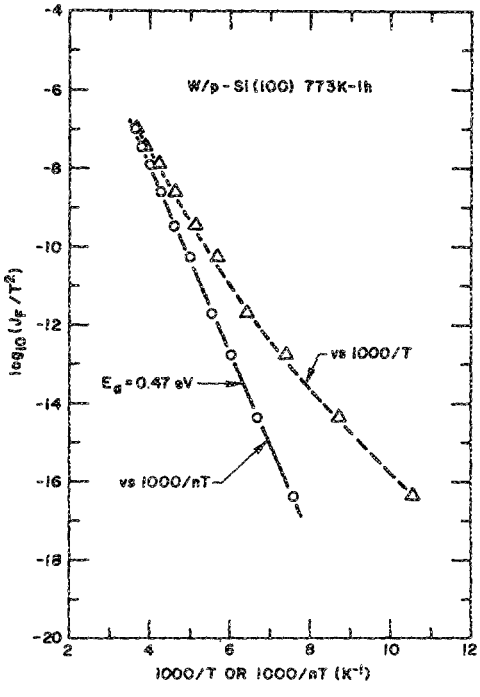


FIG. 16. Temperature dependence of forward current for p-type samples annealed at 773 K for 1 h.

$$J_F = J_t \exp[-A(V_D - V)] = J_0 \exp(AV),$$

where $J_0 = J_t \exp(-AV_D)$, J_t is a constant proportional to the density of traps in the Si depletion region, $A = \partial \ln J_F / \partial V$ is a constant, independent of temperature, and V_D is the zero-bias diffusion potential. This implies that the change in J_0 with temperature ($B = \partial \ln J_0 / \partial T$) is a result of the temperature dependence of V_D. The values of A and B determined from the results in Figs. 9(b) and 17(b) are 23–25 V^{-1} and 0.045 K^{-1}, respectively. Unfortunately, C-V measurements on these samples were not reliable because of their large parallel conductance in the range of temperature measured, and as a result, it was not possible to obtain a reliable value for $\partial V_D / \partial T$ from these measurements. Nevertheless, these values of A and B compare well with those reported in the literature in connection with multistep tunneling in a large number of heterojunctions,[27] as well as in metal-oxide-semiconductor tunnel junctions formed on p-type polycrystalline Si (22 V^{-1}) and 0.052 K^{-1}, respectively),[26] and in semiconductor-oxide-semiconductor junctions formed by ion-beam sputtering on p-type Si(24 V^{-1}) and 0.064 K^{-1}, respectively).[28]

It can also be seen from Fig. 9(b) that at higher voltages, the samples display a high ideality factor which again increases with decreasing temperature. In addition, a plot of $\ln(J_F/T^2)$, obtained by extrapolating the high-voltage linear portion of the forward characteristics to zero applied voltage, versus $1/T$ is not a straight line, whereas a plot of $\ln(J_F/T^2)$ vs $1/nT$ is a straight line in the temperature range 95–235 K with a slope giving an activation energy of 0.42 eV, as shown in Fig. 17(a). Again, this value of activation energy is evidently associated with recombination in the depletion region. In these samples it was therefore not possible to obtain reliable values for the barrier height in the range of temperature measured. However, for the silicide phase formed at 1073 K in 10 min, thermionic emission was found to be the dominant current mechanism, and the barrier height was found to have a value of 0.47 eV at 295 K. Values of the n- and p-type SBHs (ϕ_{Bn} and ϕ_{Bp}) at 295 K for the as-deposited and annealed samples are summarized in Table III. Also listed are the barrier-height values reported by Crowell *et al.*[23] and Itoh and Hashimoto[24] for W on n-type Si(111).

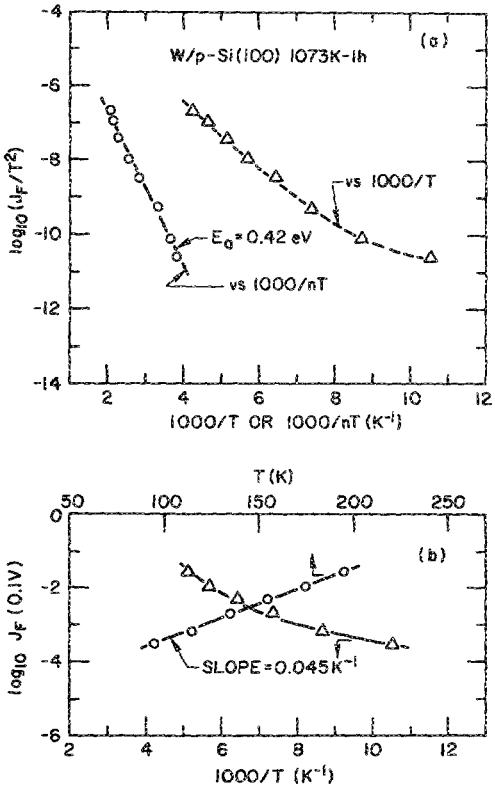


FIG. 17. Temperature dependence of forward current for p-type samples annealed at 1073 K for 1 h.

The data of Figs. 6 and 15 clearly show that only in samples where the thermionic emission current dominates, the n- and p-type barrier heights decrease with increasing temperature. The temperature coefficients of ϕ_{Bn} and ϕ_{Bp} as determined from these data, assuming a linear variation for the SBHs in the temperature range 95–295 K, are listed in Table III.

IV. DISCUSSION

Surface electron spectroscopy studies of the refractory metal V-Si(111) and Ti-Si(100) interfaces have shown that atomic intermixing (i.e., chemical reaction) does not occur upon metal deposition at room temperature.[5,29] Although spectroscopy measurements on the refractory metal W-Si(100) interface are not available at present, such an interface is also not expected to display any measurable reaction (atomic intermixing across the interface) at room temperature.[5,30] From the SBH data in Table III it can then be seen that for W on Si(100), initial silicide formation results in very little or no change in barrier height. Furthermore, for the V-Si(111) (Ref. 5) and Ti-Si(100) (Ref. 12) interfaces the barrier height has been found to vary by less than 0.1 eV with the onset of atomic intermixing and silicide formation across the initially unreacted interface. The results of these previous and the present studies thus indicate that the refractory metal silicide formation has only a small effect on the barrier height. In other words, a refractory metal and its

TABLE III. Values of SBHs (in eV) at 295 K for W on Si(100) and temperature coefficients of the n- and p-type SBHs (in 10^{-4} eV/K), obtained by straight-line least-squares fits to the experimental data. Temperature coefficient of the indirect energy gap of Si, $\partial E_g^i / \partial T$ is $\sim -2.6 \times 10^{-4}$ eV/K in the temperature range studied (Ref. 15).

	ϕ_{Bn}			ϕ_{Bp}			
Annealing condition	I-V	C-V	Photoelectric	I-V	C-V	$\frac{\partial \phi_{Bn}}{\partial T}$	$\frac{\partial \phi_{Bp}}{\partial T}$
None	0.65 (0.67)[a]	0.66 (0.65)[a]	0.65[a]	0.50	0.52	−1.96	−0.57
At 773 K for 1 h	0.67 (0.67)[a]	0.67		0.46		−1.28	−0.29
At 1073 K for 10 min	0.65		0.68–0.83[b]	0.47			

[a] Reference 23.
[b] Reference 24.

silicides have close values of barrier heights, thus deemphasizing the role of local charge redistribution associated with silicide formation at the interface[31] in determining the barrier height. Recently, experimental studies have pointed to the importance of interfacial structures in the Schottky barrier formation.[10] However, since the W and WSi_2 films are polycrystalline, there is no epitaxial structural effect involved in the small change in barrier height.

As pointed out earlier, material reaction leading to the formation of the silicide-Si interface inevitably involves the generation of point defects in the Si substrate, e.g., vacancies and/or interstitials. Deep levels associated with such defects may play a role in determining the Fermi-level position and hence the barrier height if they are formed at, or very close to, the interface.[34] However, the data in Table III clearly indicate that the barrier height is not determined by such defect levels, and thus deemphasize their role in barrier formation. Nevertheless, extending the annealing after initial silicide formation causes the current characteristics to deviate significantly from the ideal thermionic emission behavior, indicating that these defect levels are rather acting as recombination-generation centers or as traps giving rise to excess thermally activated current or excess tunneling current which causes such deviations from the ideal current characteristics. These results thus clarify a role of material reaction in determining the electrical characteristics of the W-Si junction.

Almost all theoretical models of Schottky barrier formation at metal-semiconductor interfaces have been based on the suggestion that the Fermi level is pinned at the interface by states in the semiconductor band gap.[32] Fermi-level pinning has been variously attributed to surface states,[32] intrinsic interface states,[33] or any of a variety of defects[31,34] in the semiconductor. Recently, a simple quantitative relationship between barrier heights and measured semiconductor properties has been proposed based on the suggestion of Fermi-level pinning in the center of the semiconductor indirect band gap.[33] The p-type barrier height ϕ_{Bp} was given by

$$\phi_B = \tfrac{1}{2}[E_g^i - (\Delta/3)] + \delta_m, \qquad (2)$$

where E_g^i is the semiconductor indirect band gap, Δ is the spin-orbit splitting (0.04 eV for Si at room temperature), and δ_m is an adjustable parameter, which allows for some shift in Fermi level from the center of the gap, depending upon the metal. Equation (1) has been used successfully to predict Schottky barrier heights for elemental and III-V compound semiconductors and explain variations in barrier height with semiconductor properties.[33] It is to be noted that since silicide formation, at least in the cases of refractory metals, does not significantly affect the barrier height, the model may also be applicable to such reacted interfaces, as long as the states which pin the Fermi level are dense enough and penetrate deep enough into the gap to screen the details of the interface. From the present data as well as those reported previously for W on elemental and compound semiconductors,[35] it can be inferred that the δ_W value for W is -0.12 eV, indicating that Fermi-level pinning occurs below the gap center. Comparing with the δ_{Au} value of -0.2 eV for Au (Ref. 33) (i.e., Fermi-level pinning occurs well below the gap center) and the δ_{Ti} value of ~ 0 eV for Ti (Ref. 12) (i.e., Fermi-level pinning occurs near the gap center), this δ_W value for W is reasonable in view of the fact that W is less electronegative than Au, but more electronegative than Ti. Thus, it is clearly evident that the silicon Schottky barrier height is sensitive to the property of the metal.[33,36]

The data in Table III show that the n-type barrier height decreases with increasing temperature with a coefficient close to one-half the temperature coefficient of the indirect energy gap of Si. This is consistent within the prediction of Eq. (2) regarding the temperature dependence of the barrier height, $\partial\phi_{Bn}/\partial T$. On the other hand, the p-type barrier height decreases with increasing temperature but with a coefficient much less than one-half the temperature coefficient of the Si energy gap. This is due to recombination in the depletion region. As a result, the barrier-height values calculated using the relation for thermionic emission show less negative or even a positive temperature dependence (see Fig. 15) since departures from ideal behavior due to recombination become more pronounced with decreasing temperature. This then stresses the importance of using experimental results obtained for metal-semiconductor interfaces with ideal thermionic emission behavior for comparison with proposed theoretical models of Schottky barriers.

CONCLUSION

The electrical characteristics of W-Si(100) Schottky barrier junctions formed by sputter deposition of W on both n- and p-type Si(100) have been measured in the temperature range 95–295 K. The results show that initial silicide formation has very little or no effect on the barrier height. Annealing after initial silicide formation causes the junction characteristics to strongly deviate from the ideal thermionic emission behavior. For junctions with ideal thermionic emission behavior the barrier height is found to decrease with increasing temperature with a coefficient consistent with the predictions of recent models of barrier formation based on Fermi-level pinning in the center of the semiconductor indirect band gap.

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