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RESEARCH PAPER

Current–voltage and capacitance–voltage studies of nanocrystalline CdSe/Au Schottky junction interface

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Abstract CdSe nanocrystalline thin films have been synthesized on indium tin oxide (ITO) substrates by an electrodeposition technique. A Schottky junction device in the configuration, ITO/nano-CdSe/Au has been fabricated to study the device interface properties by current (*I*)–voltage (*V*) and capacitance (*C*)–voltage (*V*) measurements and compared with the ITO/bulk-CdSe/Au device. The *I*–*V* characteristics of the nano-CdSe device shows a series resistance effect and *C*–*V* characteristics show the presence of surface/interface traps induced by a thin native oxide layer at the nano-CdSe/Au interface and is responsible to the deviation in the ideal Mott–Schottky behavior. The presence of a thin oxide layer on the CdSe nanocrystal surface has been identified from Rutherford backscattering (RBS) spectrometry. The low frequency capacitance response of the nano-CdSe device characteristics are being compared with the bulk device, which confirms the presence of surface/interface states within the band gap of CdSe nanocrystals. Mott–Schottky plots at different frequencies indicate the formation of a Schottky barrier between nano-CdSe and Au junction.

Keywords Nanostructure · Current–Voltage · Interface · Schottky · Thin film

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Introduction

Size quantization effect (SQE) in semiconductor nanocrystals has been the subject of intense study for past few years (Brus 1984; Tung 1992; Klein et al. 1996; Norris et al. 1996). Such SQE has resulted in decreased radiative recombination of carrier life time leading to enhanced electroluminescence efficiency in Schottky devices (Mattoussi et al. 1998). However, the interruption of atomic periodicity at the nanocrystal (NC) surface, large unsaturated dangling bonds, and the presence of a thin oxide layer at semiconductor surface have been responsible for the nonideal device interface characteristics and, hence, limit the electroluminescence efficiency, too. Thus, the interface, in general, is characterized by current (*I*)–voltage (*V*) and capacitance (*C*)–voltage (*V*) studies (Lee et al. 1992; Heo et al. 2004; Vanmaekelbergh et al. 1997; Kolvin et al. 1994; Yang et al.

1996; Artemyev et al. 1997; Dobbousi et al. 1995). Many of the important NC semiconductor-based devices reported belong to the II–VI group because of the ease of their material synthesis and device fabrication. Of special significance are the CdSe NC-based devices (Vanmaekelbergh et al. 1997; Kolvin et al. 1994; Yang et al. 1996; Artemyev et al. 1997; Dobbousi et al. 1995; Van de Lagemaat et al. 1996) where significant electroluminescence has already been reported (Kolvin et al. 1994). Colloidal route-based CdSe (Mattoussi et al. 1998) NC growth has been used to fabricate Schottky devices but no details of the interface properties have been reported. On the contrary, for bulk polycrystalline CdSe-based devices with Au/CdSe/Au configuration (Antohe et al. 2002), the *I–V* characteristics show ohmic behavior in the low applied bias regime. In the higher applied bias regime, it shows the space charge limited current (SCLC) behavior due to filling up of traps by the charge carriers (Antohe et al. 2002). As shown in Antohe et al. 2002, the *I–V* characteristics of Al/CdSe/Al (Abdel-Latif 1999) devices also show similar SCLC behavior in the higher applied bias regime whereas in the low applied bias regime, it shows an exponential increase in current. These results are contradictory to the Schottky behavior specific to the barrier height of the device reported by Panchal et al. 2008. The work function of Au is 5.01 eV (Novkovski et al. 2008), whereas the band gaps of bulk-CdSe and NC CdSe, in the present case, are 1.7 and 2.2 eV, respectively. As there is a large energy difference between Au work function and Fermi levels of CdSe, upon intimate physical contact between nano-CdSe or bulk-CdSe and Au should yield a Schottky barrier which can be confirmed by the study of the device characteristics. With this motivation, ITO/nano-CdSe/Au junction has been fabricated, and the device interface properties have been evaluated by *I–V* and *C–V* measurements. The results are compared with large crystalline ITO/CdSe/Au device.

Experimental

Two different crystalline size CdSe thin film samples on conducting ITO substrates were prepared by simply varying electrodeposition temperature and current density keeping deposition time, solution pH, and ionic concentrations constant. CdSe thin films prepared at 280 K and current density 2 mA/cm^2 have yielded smaller crystallites in the nanometer range, which show SQE (Sarangi and Sahu 2004) with the size being smaller than the Bohr exciton diameter, a_B of CdSe ($a_B = 9.8$ nm). These samples are designated as nano-CdSe. Samples prepared at 300 K at 5.0 mA/cm^2 current density always yielded larger crystallites in the nanometer range, which do not show SQE or do show a weak confinement effect due to the size larger than a_B. These samples are designated as bulk-CdSe. Particle-induced X-ray emission (PIXE) and Rutherford backscattering (RBS) spectroscopic measurements were carried out using H^+ and He^{2+} beams, respectively, from a 3 MeV Pelletron accelerator to identify the presence of impurity and stoichiometry of CdSe samples. Transmission electron microscopy (TEM) of CdSe samples were carried out using JEOL 2010 TEM operated at 200 kV to estimate the crystalline size. Metal-semiconductor junction devices in the configuration ITO/nano-CdSe/Au (device-I) and ITO/bulk-CdSe/Au (device-II) were fabricated by thermal evaporation of gold (Au) dots of 2 mm diameter through a mask on ITO and on CdSe samples. Contact leads were taken by copper wire through silver epoxy. Detail schematic of the device fabrication is being discussed in the results and discussion section. Forward biased *I–V* and *C–V* measurements at 300 K were carried out using Keithley Picoammeter and HP4284A variable frequency LCR meter, respectively.

Results and discussion

The presence of impurities in CdSe can influence the electrical characteristics of the device. Hence, PIXE analysis was carried out to identify presence of any impurity even at ppm level in the deposit. In this technique, inner shell ionization by high energy proton beam and target interaction results in characteristic X-ray emission from different elements present in ITO and CdSe which are detected by a Si(Li) detector. Figure 1a and b compares the PIXE spectra of bare ITO substrate (a) and that of a typical CdSe NC film deposited on ITO (b). The different elements present in ITO are Si, Ca, Fe, Zr, In, and Sn as shown in Fig. 1a. PIXE spectrum shown in Fig. 1b identifies the presence of Cd and Se in CdSe apart

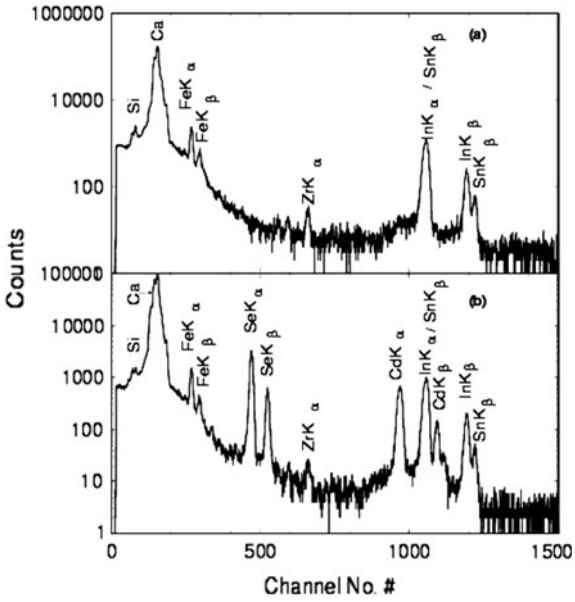

Fig. 1 The PIXE spectra of **a** ITO glass substrate and **b** nano-CdSe showing the presence of different elements in the substrates and of the sample on ITO

from the contributions from the ITO substrate. However, the Si(Li) detector used for PIXE analysis cannot identify low atomic number (Z) elements. Hence, the presence of low Z elements such as oxygen as an impurity in the sample cannot be ruled out. Grazing angle X-ray diffraction studies confirm that both nano-CdSe and bulk-CdSe exhibit cubic phase (Sarangi and Sahu 2004).

Figure 2a and b depict the transmission electron micrographs of the nano- and bulk-CdSe samples. Isolated and agglomerated CdSe NCs with average crystalline size of ~7.5 nm have been identified from Fig. 2a, whereas for bulk-CdSe (Fig. 2b), the surface is more compact, and the average grain size is ~15.0 nm. The bright areas on Fig. 2a are the background from carbon-coated Cu grids. The inset in Fig. 2b is the HRTEM of bulk-CdSe which exhibits the cubic phase with size as 15 nm. The 7.5 nm crystalline size shows SQE marked by blue shift in the optical absorption whereas 15.0 nm sizes do not show any SQE (Sarangi and Sahu 2004).

The forward biased *I–V* characteristics of device-I and device-II are shown in Fig. 3 in semi logarithmic plots. Inset is the schematic representation of the Schottky device fabricated as described in the experimental section. In short, NC and bulk-CdSe thin films were electrodeposited on ITO substrates, washed with water jets, and dried in the ambient. Au dots (2-mm diameter) as shown in Fig. 3 inset are vacuum evaporated on CdSe and ITO. Contact leads were taken as described in experimental section. The *I–V* characteristics of devices I and II were studied under both forward and reverse bias conditions. The reverse saturation current has been found to be negligibly small, whereas the forward current increases exponentially after certain threshold voltage (the voltage at which the current starts to flow) that depend upon the crystalline size of the samples for both the devices. The *I–V* characteristics suggest that Schottky contacts have been formed for both the devices (I and II). The ohmic behavior of the contact leads (made out of Au, Cu-wires, and Ag epoxy) were

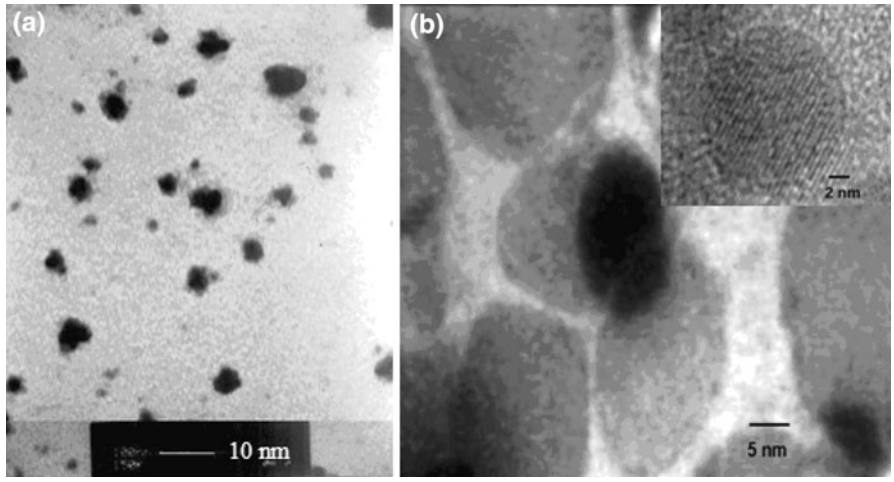

Fig. 2 Transmission electron micro graph of **a** nano-CdSe and **b** bulk-CdSe sample

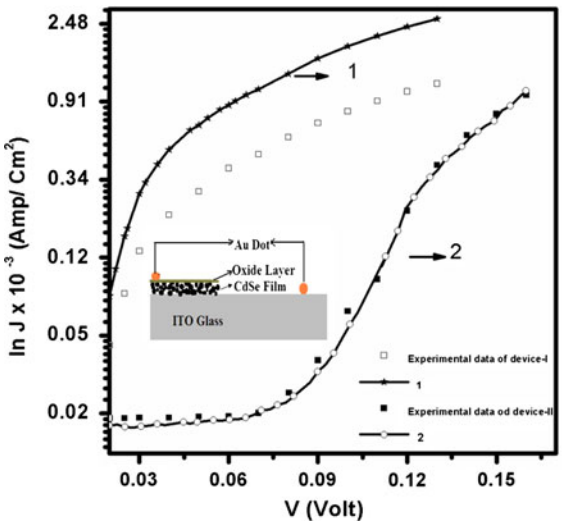

Fig. 3 ln *J–V* characteristics of the nano-CdSe/Au and bulk-CdSe/Au devices. Curves1 and 2, respectively, are the corresponding corrected *I–V* characteristics taking the series resistance into account. Inset is schematic of the Schottky device fabrication. Contact leads are from Au dot and conducting ITO substrate

confirmed from their forward and reverse characteristics. When CdSe is negatively biased and Au on CdSe is positively biased, this refers to the forward bias condition. It is evident from Fig. 3 that the voltage threshold for the current flow in the case of device-I is much less than that for device-II. The current in the case of device-I rises rapidly above 0.02 V whereas in the case of device-II, the rise in current occurs above 0.10 V but at a higher rate compared to device-I. The downward curvature in the *I–V* characteristic (Fig. 3) of the high forward bias regime is attributed to the presence of interface states (Tung 2001) and/or low barrier patches (Kiliçoğlu and Asubay 2005). The interface states can arise due to the presence of foreign impurities, off-stoichiometry, and native oxide in the sample. Absence of high Z foreign impurities has been confirmed from PIXE but the presence of the low Z elements cannot be ruled out in the sample. RBS confirms the stoichiometery and the presence of surface oxygen in the deposit (to be discussed later). This implies that the difference in the *I–V* characteristics of the two devices could be due to the presence of a native oxide layer. If the oxide layer is very thin, i.e., ~a few angstroms, then under forward bias, the carriers can cross over the device interface by tunneling and contribute to the total current flow.

Large surface to volume ratio in the case of NC CdSe (device-I) can introduce a high density of surface states at the interface. These surface states play an important role in the conduction process by providing a pathway for electron flow in the case of nanocrystalline sample as compared to its bulk counterpart. In this study, nanocrystalline CdSe thin films were grown by an electrochemical route in the ambient. Unprotected NC semiconductor surfaces exposed to the ambient are prone to oxidation (Alivisatos 1996). Therefore, a native thin oxide layer is expected in between nano-CdSe and Au coated area. The presence of oxide layer on the surface of the nano-CdSe sample is being confirmed from RBS experiment using 3MV He^{2+} ion beam from a 3.0 MeV pelletron accelerator. A typical RBS spectrum of nano-CdSe is shown in Fig. 4. The atomic concentrations of Cd and Se were estimated using GISA-III program. The presence of Cd and Se in the ratio Cd: Se = 1 has been estimated by simulation. Apart from Cd and Se, a prominent peak corresponding to oxygen (O) is also being detected which amounts to ~70% surface coverage along with Ti substrate contribution. The oxide thickness is estimated to be ~12 Å. Note that, from Fig. 4, the Cd and Se RBS peak heights are different. This is due to the fact that the RBS yields for Cd and Se are inversely proportional to their stopping power cross section. The stopping power cross section of Se being smaller (Chu et al. 1978) than Cd, one observes that the peak height of Se is more than Cd. For RBS analysis, CdSe samples were prepared on Ti

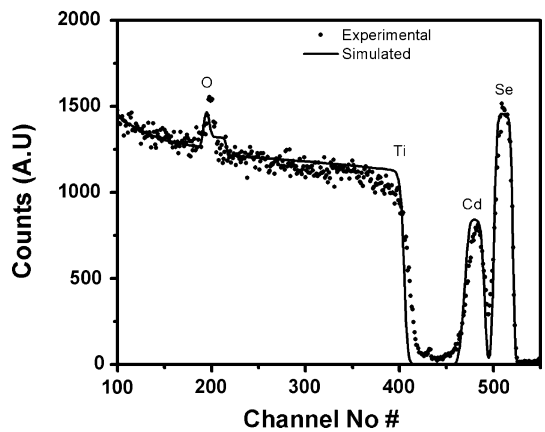

Fig. 4 RBS spectrum of nano-CdSe sample. The solid line is the theoretical fit to the experimental data

substrates instead of ITO to avoid complications in the analysis. However, the composition of the sample does not vary appreciably (Sarangi and Sahu 2004) even if the substrates (Ti & ITO) are different and the composition is within ±2% error. The RBS analysis of bulk-CdSe sample also shows stoichiometry (Sarangi and Sahu 2004) but found the presence of little oxygen on its surface. The presence of an oxide layer in the device introduces interface/surface states which will result in the distribution of the applied potential across the space charge and oxide layer. Thus, a series resistance due to the oxide in series with the space charge is introduced in the device, which is responsible in the deviation of ideal Schottky behavior. The *I–V* relationship is, thus, modified as reported by Muruska et al. 1992. The interface/surface states have a pronounced effect in current transport mechanism. At higher forward bias, the *I–V* curves tend to be a straight line, and the series resistance can be estimated from the slope of the *I–V* curve in the high forward bias regime ($\gg$3 kT/q) of Fig. 3. Thus, we observe a leakage current contribution to the device-I due to a thin oxide layer, which does not affect the shape of the *I–V* curve (Sugimura et al. 1999). The series resistance, Rs, estimated to be 474 Ω for the device-I whereas it is negligibly small for device-II. These results are consistent with those reported in previous studies (Tung 2001; Kiliçoğlu and Asubay 2005). Further, the theoretical fit versus the experimental *I–V* curves taking the series resistance into account are also shown in Fig. 3 as curve-1 and curve-2, respectively. Note that the Rs effect is dominant in the case of device-I compared to the device-II. The dominant contribution of interface/surface states in the device can be more clear from their *C–V* studies which we discuss in a later section.

Figure 5a and b shows the ln (*J*) versus *V* plots of device-I and device-II, respectively, in the forward bias regime. Note that a single slope has been observed above the applied voltage 0.07 V (i.e., above 3 kT/q). From the slope, the ideality factors (*n*) have been estimated for device-I and device-II, and the same is given in Table 1. For an ideal Schottky junction, the ideality factor is supposed to be 1 where the current should depend exponentially on the applied voltage. In this study, the ideality factor is 1.0 in the case of device-II where the sample surface oxidation is less. Note, from the Fig. 5b, that there is a non-linearity in the ln (*J*) versus *V* plot above 0.13 V,

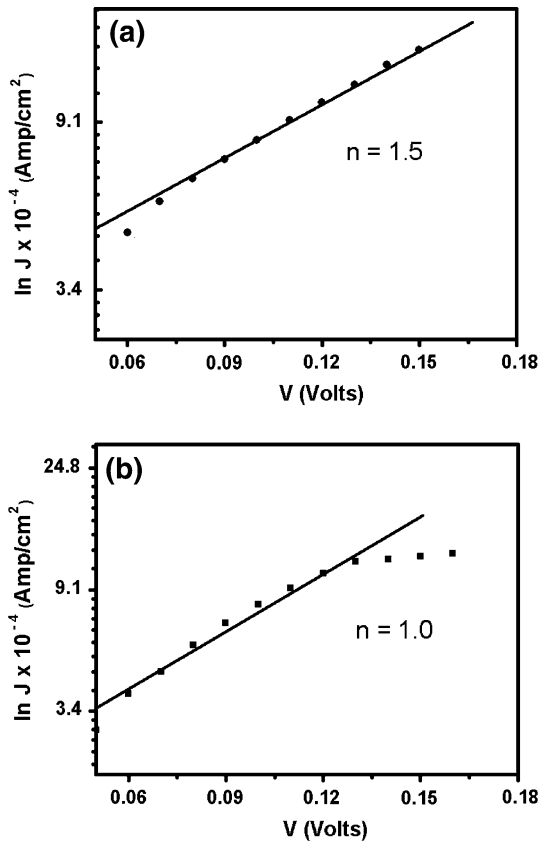

Fig. 5 ln (*J*)–*V* plots of nano-CdSe/Au **a** and bulk- CdSe/Au **b** devices for $V \gg 3$ kT/q

Table 1 Different electrical parameters obtained from *I–V* measurements

Device	Threshold voltage (V)	Ideality factor (*n*)	ϕ_{Bn} (eV)
Nano-CdSe/Au Device-I	0.02	1.5	0.65
Bulk-CdSe/Au Device-II	0.10	1.0	0.77

which needs explanation. For higher applied positive potential (low forward bias regime), above 0.13 V, the depletion width is larger than the half-width of the crystalline grain so that the applied potential is not able to penetrate into the bulk-CdSe structural units as the size being large. However, with increasing forward bias, the trap contribution to the current flow is significant so that one gets a large ideality factor as in device-I. For the same applied potential (high forward bias regime), the trap contribution is much less in device-II than in device-I due to less lateral variation in barrier heights as a result of lesser

oxidation. This oxidation should have introduced a series resistance effect in the device-II, but the same is not observable due to large size of CdSe (15.0 nm) compared to nano-CdSe (7.5 nm) (Pakma et al. 2008). Hence, we observe a non-linearity at low forward bias regime in device-II. Ideality factor 1.5 for device-I implies that there is lateral inhomogeneous distribution of barrier heights due to interface defects caused by oxidation of the sample surface. For an ideal Schottky device with dominant thermionic transport mechanism, the recombination is mediated via band to band or via traps. The ideality factor for such a device is close to 1 as is the case with device-II which suggests that the thermionic emission model can be applied to device-II to describe the forward biased current. However, the presence of a native oxide layer at the device interface would result in distribution of the applied voltage which in turn would introduce Schottky barrier height inhomogeneities (Hastas et al. 2004) within the contact area and hence a higher value of the ideality factor as in the case of device-I is being observed. The barrier inhomogeneities can induce series resistance into the Schottky device. Note that an excess current flow at lower forward bias in the case of device-I further suggests to the presence of barrier inhomogeneities (Hastas et al. 2004) within the Schottky contact area. Hence, the dominant transport mechanism in device-I is due to both thermionic emission and lateral inhomogeneous distribution of barrier heights. In order to verify the dual mechanism for smaller size NC samples, a sample with lower dimension was prepared at 1.0 mA/cm^2, keeping the temperature and deposition time same as device-I. No current was able to be measured for such a device as the contact leads short circuit the current path. Microscopic observations show that the sample thickness is very small and has an isolated island structure (Sarangi and Sahu 2004) on ITO. Such a high ideality factor is also reported for Si-based Schottky device (Kiliçoğlu and Asubay 2005; Hastas et al. 2004).

The reverse saturation current can be expressed as

$$I_0 = A * T^2 \exp\left(-\frac{q\phi_{\mathrm{Bn}}}{kT}\right) \quad (1)$$

Here A^* and ϕ_{Bn} are the effective Richardson constant and barrier height, respectively. From the known value of Richardson constant, $A^* = 15.5$ A/K^{2}cm^2 (Panchal et al. 2008), and the value of saturation current density obtained from the ln (J) versus V plot, the barrier heights, ϕ_{Bn}, have been estimated from Eq. 1 and are summarized in Table 1 along with ideality factor and threshold voltage for current flow for the two devices.

In order to study the capacitance (C) and voltage (V) behavior of the two devices (I and II), the Au contact on CdSe were positively biased, and CdSe on ITO negatively biased. This refers to the condition of forward bias as CdSe is an n-type semiconductor. The C–V characteristics at 500 Hz frequency for device-I and device-II are shown in Fig. 6 in the voltage region −1.0 to 0.5 V which is also the range with I–V forward bias as in Fig. 3. The capacitance magnitude of device-I is much higher than device-II. The higher capacitance observed in the case of device-I as compared to device-II is ascribed to the larger interfacial contact area (Alivisatos 1996) between the nano-CdSe and Au contact. For device-I, the capacitance increases slowly from 0.35 V and attains a peak structure at −0.3 V. With further increase of negative voltage, the capacitance falls without any sign of saturation. This C–V characteristic is typical of a metal-insulator-semiconductor (MIS) junction where M is Au, S is nano-CdSe, and I is the insulating oxide layer. On the contrary, device-II shows very little voltage-dependent variation of capacitance unlike device-I. The C–V characteristics of device-II on a zoomed scale are shown in the inset of Fig. 6, which reveal one shallow peak with a sharp

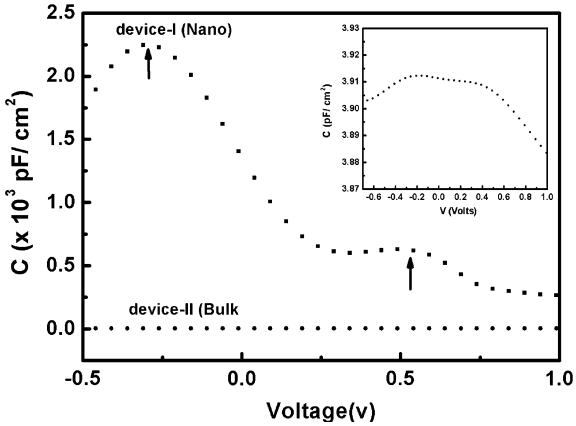

Fig. 6 C–V characteristics of nano CdSe/Au and bulk-CdSe/Au devices plotted for 500 Hz frequency. Inset shows the zoomed C–V characteristics of bulk-CdSe/Au device

fall of capacitance above 0.5 V. Such a feature in device-II suggests the absence of an oxide layer or the presence of a discontinuous oxide layer between bulk-CdSe and Au whose effect is evident from the *I–V* characteristics shown in Fig. 3. For both the devices, the capacitance falls more in the negatively biased regime i.e., for device-I, below −0.3 V and for device-II, below −0.25 V. In the case of device-I, under applied bias, the voltage will be distributed across the space charge (SC) region within nano-CdSe and the oxide layer. The total junction capacitance, C can be expressed as

$$\frac{1}{C} = \frac{1}{C_{sc}} + \frac{1}{C_{ox}} \tag{2}$$

where $C_{sc} = \frac{\varepsilon_s}{W_{sc}}$ and $C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}}$. The quantities ε_s, ε_{ox}, C_{sc}, and C_{ox} are dielectric constant of nano-CdSe, dielectric constant of the oxide layer, space charge (SC) or depletion capacitance, and capacitance from the oxide layer, respectively. The total junction capacitance will depend upon the change in the immobile charge concentration under the change in applied voltage across the junction. Under this situation, when Au is positively biased (low forward bias), the electrons (majority carriers of nano-CdSe are electrons) accumulate at the nano-CdSe and oxide/Au interface. A small change in the voltage should lead to a large change in the accumulated charges which should be reflected in its capacitance behavior. In that case, the total capacitance contribution should be from the oxide and depletion layers. For both the devices I and II, with increasing positive voltage, the capacitance falls steeply which implies that the depletion width increases compared to the half-width of the NC grain, and hence, the total junction capacitance is only from the depletion layer. Further, with increasing negative voltage (increasing forward bias), the depletion width decreases, and the electrons may tunnel through the oxide layer (thickness, 12 Å) which will decrease the charge density, and hence, the capacitance falls above −0.3 V. On the contrary, such capacitance behavior is nearly absent for device-II which suggests that the bulk-CdSe is not fully oxidized. Now, we consider the intermediate region of the *C–V* curves. When the applied positive voltage is decreased (in the higher forward bias regime), the capacitance increases slowly and then steeply in between 0.25 and −0.25 V in the case of device-I. Capacitance behavior in the voltage range 0.25 to −0.25 V is attributable to the thinning of the depletion layer by penetrating the potential deep into the NC units whose half-width is much smaller than the depletion width. This feature suggests the formation of a Schottky junction. The capacitance peak appearing at −0.3 V is due to the charge trapping by surface states. Under bias, when the Fermi level of the connecting leads coincides with the energy position of the surface states, the capacitance peaks up (Barret et al. 1983). As the crystalline size decreases, unsaturated dangling bonds on the surface due to interruption in atomic periodicity give rise to such surface traps. Hence, in the case of device-I, higher capacitance along with a peak structure has been observed in contrast to device-II.

The effect of surface state in the device performance can further be tested by the *C–V* behavior as a function of frequency. As discussed earlier, for device-I, the ideality factor is 1.5, which suggests the presence of high density of surface/interface states. These surface/interface states can inject minority carriers into the semiconductor metal junction under high forward bias which would give an additional diffusion capacitance apart from the depletion one. However, the rearrangement of the injected minority carriers does not take place instantaneously and becomes frequency (w) dependent. The injected minority carriers under high forward bias can hardly follow the a.c signal (Luuia et al. 1993).

The magnitude of the diffusion capacitance varies as $w^{-1/2}$ under forward bias. For low impressed a.c signal the total capacitance is essentially the sum of the diffusion and depletion capacitance. For frequencies higher than the characteristic frequency of recombination process, the injected minority carriers are not able to follow the a.c signal and the diffusion capacitance contribution to the total junction capacitance relaxes. Hence, at higher frequency, the diffusion capacitance contribution becomes much less. At higher frequencies, the diffusion capacitance contribution to the total junction capacitance will be negligible which implies that the *C–V* curves should decrease with increasing frequency. In order to test this, the *C–V* characteristics of device-I (at room temperature) are plotted at different frequencies in the voltage range −0.5 to 1.0 Vas shown in Fig. 7. The voltage range has been extended to identify if there are any more trap states apart from the one at −0.3 V as shown in Fig. 6. An additional trap state at

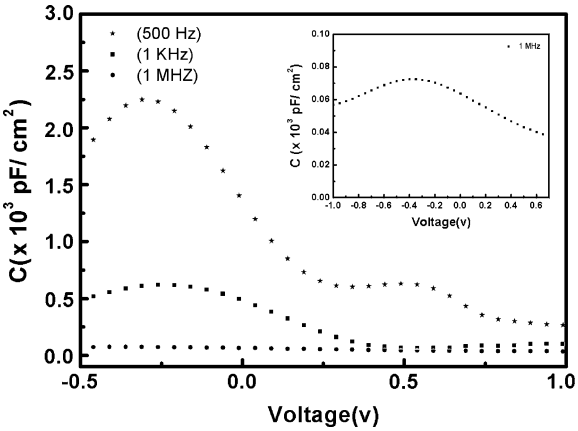

Fig. 7 *C–V* characteristics of nano-CdSe/Au device at different frequencies. Inset is the zoomed *C–V* plot for 1 MHz frequency

0.35 V apart from the one at −0.3 V has been identified. Note that the capacitance magnitude falls rapidly (Sahu and Chandra 1987; Basol and Stafsuad 1981) along with the disappearance of capacitance peak with increasing frequency. At 1 MHz frequency, the capacitance magnitude is very small as shown in Fig. 7 (inset). For high frequency a.c signal, the rate of change of surface state charge density with respect to the applied bias is small. This is because the surface state charge carriers can hardly follow the rapid fluctuation in the applied a.c signal. For this reason, the capacitance peaks disappear with increasing frequency.

Overall *C–V* behavior shows a frequency dispersion relation which can be expressed by a Mott–Schottky relation:

$$\frac{1}{C_{sc}^2} = \frac{2}{q \in_0 \in_s n_d}(V + V_{bi}) \tag{3}$$

The quantities $\in_0, \in_s, n_d$ and V_{bi} are, respectively, the permittivity of free space, dielectric constant of the semiconductor, CdSe, donor concentration and built-in potential. Mott–Schottky relation as given by Eq. 3 is valid under the following assumptions: (i) The metal and the nano-CdSe phases have zero resistance, (ii) no surface/interface traps or insulating oxide layer is present in between nano-CdSe/Au interface, (iii) the barrier has perfect blocking properties, (iv) the dielectric constant(ε_s) of nano-CdSe is independent of frequency, (v) the barrier formed by the metal and nano-CdSe under equilibrium has perfect blocking property, (vi) only one type of electronic defect is present whose distribution should be homogeneous, and (vii) the interface is planar. However, many of the conditions given above are never met in real situations, and our experimental results should be discussed under the above constraints. The Mott–Schottky (C_{sc}^{-2} vs V) plots of device-I at different frequencies (1 MHz, 1 kHz, and 500 Hz) are shown in Fig. 8. The *C–V* characteristic of device-I for $V > 0.1$ V and for $V < 0.5$ V shows nonlinearity. The degree of nonlinearity changes slightly at different frequencies. The intermediate region shows linearity in their (C_{sc}^{-2} vs V) behavior which implies that a Schottky junction is being formed between nano-CdSe and Au. However, the slope of the Mott–Schottky plots, shown in Fig. 8a, b and c for different frequencies, meet the voltage axis at two different points. For example, Mott–Schottky plots for frequencies 1 MHz (Fig. 8a) and 1.0 KHz (Fig. 8b) meet in the voltage axis at a common point −0.1 V, whereas the same plot for 500 Hz (Fig. 8c) meets at −0.01 V. The intercept on the voltage axis will give an estimate of the built-in potential, V_{bi} under the depletion condition. Knowing the barrier height, Φ_{Bn}, from the ln (*J*) vs *V* plot (Fig. 5, for device-I), one can estimate the quantity $V_n = E_c - E_f$ from the relation:

$$\phi_{Bn} = V_n + V_{bi} + \frac{kT}{q} \tag{4}$$

The quantities E_c and E_f in the above equation are, respectively, the conduction band edge and Fermi level of the semiconductor. The donor concentration, n_d, can be calculated from the relation:

$$n_d = n_c \exp\left[\frac{-(E_c - E_f)}{kT}\right] \quad \text{for } n_c \gg n_d \tag{5}$$

where n_c is the effective density of states in the conduction band. The Mott–Schottky plots for frequencies 1.0 MHz and 1.0 KHz merge to a common point. Hence, the estimation of n_d will be unreliable (Cardon and Gomes 1978; Laflere et al. 1974). On the contrary, for a frequency of 500 Hz, the Mott–Schottky plot meets the voltage axis at a different point (−0.01 V) which give the value of built-in potential. The donor concentration, n_d of nano-CdSe is estimated from Eq. 5, found to be 1.76×10^{16} cm^{-3}. The depletion width W_d has been estimated to be 78 Å using the relation

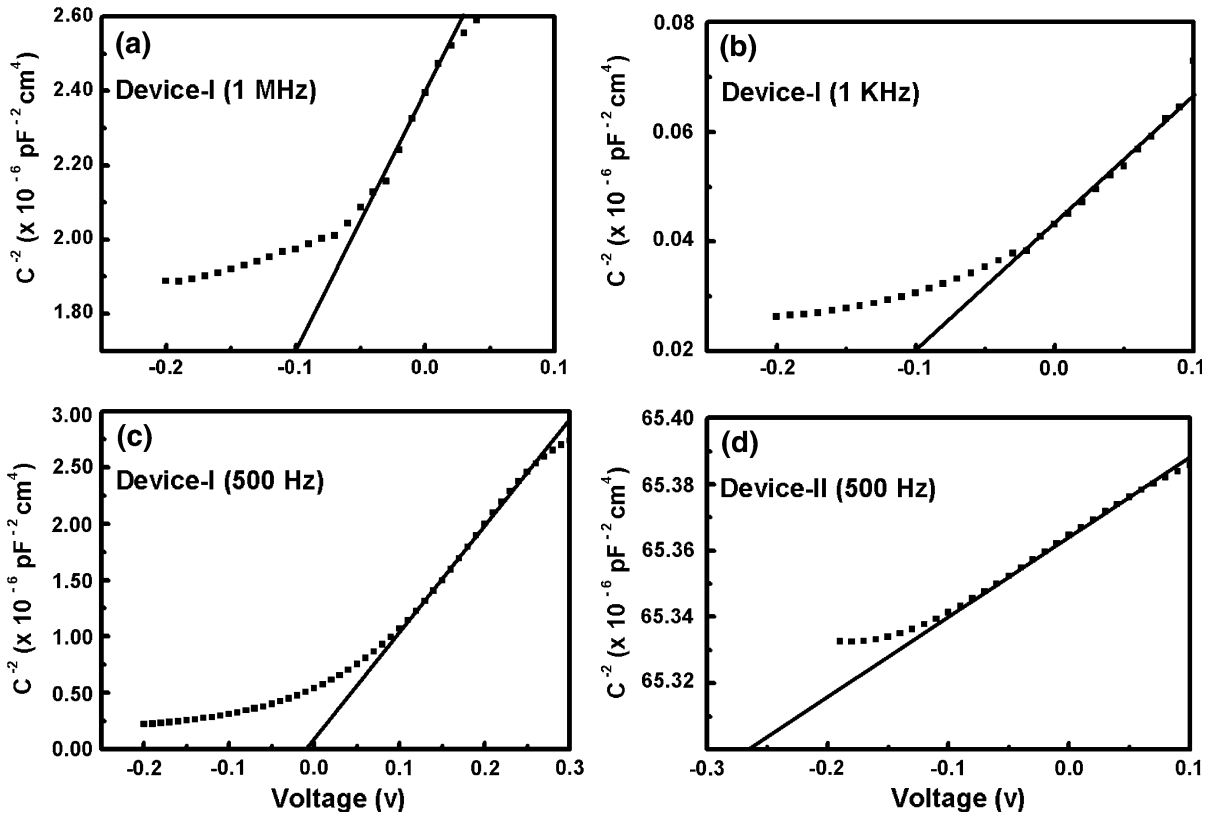

Fig. 8 (C_{sc}^{-2} vs V) plots for nano-CdSe/Au, device-I at frequencies **a** 1 MHz, **b** 1 kHz, **c** 500 Hz, and **d** at 500 Hz frequency for bulk-CdSe, device-II

$$W_d = \left(\frac{2\,\epsilon_0\epsilon_s\,V_{bi}}{qn_d}\right)^2 \tag{6}$$

A similar depletion layer is formed at bulk-CdSe/Au junction. The extrapolation of the Mott–Schottky plot at frequency 500 Hz for device-II, meets the voltage axis at −0.27 V which provides the value of built-in potential for device-II and is higher than the value obtained for device-I. Such frequency dependent Mott-Schottky plots have been observed for Schottky devices fabricated with TiO_2 and GaAs (Cardon and Gomes 1978; Laflere et al. 1974). The overall C–V behavior of device-I shows the characteristic of a leaky MIS diode involving nanostructured n-type CdSe, whereas device-II shows the normal Schottky behavior.

Conclusions

A Schottky device using nano-CdSe/Au junction has been fabricated whose device characteristics have been found to be influenced by the presence of (i) surface/interface traps and (ii) an insulating oxide layer in between nano-CdSe and Au contact. The device behaves as a leaky diode. Bulk-CdSe/Au device show a normal Schottky behavior. Large ideality factor and low threshold voltage for current flow due to tunneling of carriers in the case of nano-CdSe/Au device suggest a series resistance effect and barrier inhomogeneities induced by the presence of a thin oxide layer at the interface. The C–V behavior is found to be frequency dependent, and the linearity in the Mott–Schottky plots in intermediate voltage regime confirms the formation of a depletion layer leading to the formation of a Schottky junction.

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