Practical and simple circuitry for the measurement of small capacitance

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Practical and cost-effective circuitry with high sensitivity has been developed to measure a small capacitance using current compensation method. The circuitry uses an electronic switch to periodically connect or separate the capacitor under test (C_x) from a reference capacitor (C_r). When C_x is connected in parallel with C_r the total capacitance becomes C_x+C_r. On the other hand, as C_x is separated from C_r, the total capacitance is only C_r. This periodic change of the capacitance generates a periodic square-wave output with an amplitude in proportion to the capacitance of C_x. A high sensitivity of $\Delta V/\Delta C=202.2$ mV/pF has been achieved, making the circuitry a powerful tool in measuring small capacitances. Three applications have been performed to present its capability: (a) displacement, (b) height of liquid, and (c) angle of tilt. The experimental results demonstrate the performance of the circuitry.
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I. INTRODUCTION

Capacitive sensors are used in a wide variety of measurement and control systems, such as liquid-level gauges,[1] pressure meters,[2] accelerometers,[3] precision positioners[4] and surface roughness[5] due to many advantages including high sensitivity, quick response, and no need of touching the object. In these applications, the capacitances usually vary in the range of 0.1–100 pF. Therefore it is required to develop practical and simple circuits for the measurement of small capacitance. Some circuits have been reported for the measurement of small capacitance using resonance method,[6] ac bridge method,[7] and phase measurement.[8] In the resonance technique, a tuned *LC* circuit is driven at its resonant frequency, and capacitance changes are sensed in terms of amplitude or phase changes. A drawback of this method is that the signal-to-noise ratio is proportional to the quality factor of the tank circuit. Although the bridge methods provide a high accuracy, they are expensive and have a nonlinear output. They also suffer from the effects of stray capacitances, particularly in the measurement of small capacitance values. The phase measurement method is a cost-effective method, but it is tedious to choose a suitable value of resistor to get a maximum sensitivity.

In this article, we develop a cost-effective and high sensitivity circuitry to measure a small capacitance using current compensation method to stabilize the output voltage. An electronic switch is used to control the connection between the capacitor under test C_x and the reference capacitor C_r in a parallel or separation configuration. When C_x is connected in parallel with C_r the total capacitance becomes C_x+C_r. On the other hand, as the C_x is separated from C_r, the total capacitance is only C_r. This periodic change of the capacitance results in a periodic square-wave output with an amplitude proportional to C_x. The output voltage is a linear function of the capacitance and immune to stray capacitance. Furthermore we design three experiments to present its practical usefulness and demonstrate the performance of the circuitry.

II. CIRCUIT DESIGN

A. Operation principle

Figure 1 illustrates the block diagram of the capacitance measurement circuitry. The circuitry is divided into several subcircuits denoted by serial numbers. Initially when the switch is open and a voltage source $V_S \sin(\omega t)$ (block 1) is applied to this circuitry, the current flowing through the reference capacitor C_r is given by

$$I = V_s \omega C_r \cos(\omega t), \tag{1}$$

where V_s and ω are the amplitude and angle frequency of the voltage source, respectively. The current I indicated by Eq. (1) then flows through the feedback resistor R_f, establishing a voltage $V_1=-IR_f$ at the output of the differentiator subcircuit (block 5). A multiplier subcircuit (block 7) multiplies this voltage with a voltage which is from the voltage source phase shifted by 90° (block 2), giving an output voltage V_2 consisting of a dc signal and a double-frequency (2ω) ac signal. Following this multiplier, a low pass filter (block 9) is used to eliminate the ac signal and keep the dc signal intact. Therefore the output voltage V_5 of the low pass filter can be written as

$$V_5 = \frac{-V_s^2 \omega C_r R_f}{2}, \tag{2}$$

which is proportional to C_r. The voltage V_5 is integrated by an integrator (block 8) to become V_3, which is then multiplied using a multiplier (block 6) with a voltage that is from the voltage source phase shifted by −90° (block 3). The resultant voltage V_4 provides a feedback current I_f through the resistance R_1, and the current is given by

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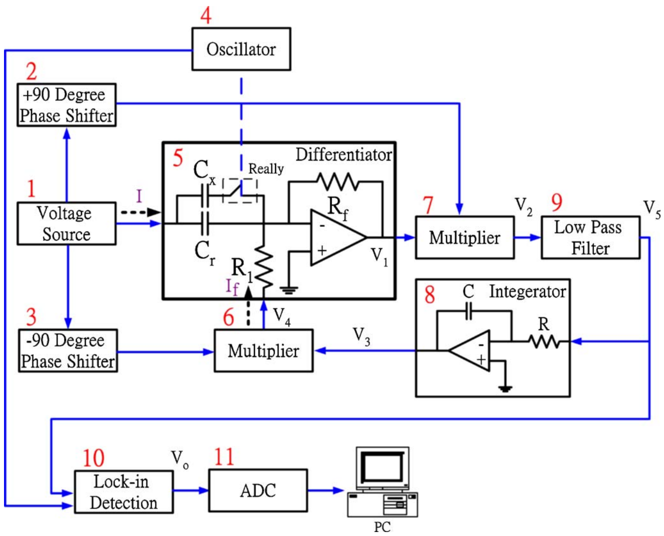

FIG. 1. (Color online) Block diagram of the capacitance measurement circuitry.

$$I_f = \frac{V_4}{R_1} = \frac{-V_s^3 \omega t C_r R_f \cos(\omega t)}{2RCR_1}, \tag{3}$$

where R and C are, respectively, the resistance and capacitance of the resistor and capacitor elements used in the integrator subcircuit (block 8). This feedback current serves as a compensation current to reduce the total current flowing through R_f, eventually making V_5 get stabilized at a voltage corresponding to C_r.

One of the key components in Fig. 1 is the reed relay (EDR201A1200) controlled by an oscillator (block 4). When the reed relay is closed, the capacitance under test C_x is connected in parallel with C_r and the total capacitance becomes C_x+C_r. When the reed relay is opened, the total capacitance is just C_r. A periodic change of the capacitance value between C_x and C_x+C_r is realized by an oscillator, and then a periodic square-wave output voltage with amplitude proportional to C_x is generated. For example, when the reed relay is opened and thus C_x is disconnected, a capacitor C_r of 100 pF gives rise to a 20 mV dc voltage. When 200 pF is used for C_r, the dc voltage is increased to 50 mV. If C_r and C_x are both 100 pF, the reed relay controlled by an oscillator switches the total capacitance values between 100 and 200 pF, and the output voltage changes between 20 and 50 mV. Therefore, a square-wave output of the amplitude, with the offset voltage deducted, proportional to C_x is generated. The lock-in detection subcircuit (block 10) is designed to extract the voltage component with the same frequency and phase with respect to the control voltage signal from this square-wave voltage. Finally the final analog output voltage V_o is fed into a monolithic 12 bit analog-to-digital converter (ADC) (block 11) to provide digital output data. Users only need to have a personal computer (PC) with a data acquisition card installed to acquire the digital data coming from the instrument.

B. Electronic circuits

The circuit diagram of this capacitance measurement system is shown in Fig. 2. For clear description, this circuitry is divided into eleven subcircuits, each of which is framed by dotted lines and denoted by numbers corresponding to the serial numbers in Fig. 1. The voltage source (block 1) with peak-to-peak voltage V_{pp} of 5.0 V and frequency of 78.5 kHz is connected to this circuitry and serves as the measurement source. Although using a voltage source with higher frequency can enhance the sensitivity of this circuitry, other devices such as operation amplifier (LM357) and multiplier (AD633), however, constrain the upper limit of the operation frequency due to their limited frequency performance. For this circuitry, the frequency of 78.5 kHz is determined based on the requirements of normal operation for each device. This voltage signal is additionally phase shifted by 90° and −90° through the subcircuits 2 and 3, respectively. The standard +90°/−90° phase shifters (blocks 2/3) consist of an operation amplifier, some resistors and capacitors to yield a leading/lagging wave form relative to the voltage source.

The differentiator subcircuit denoted by 5 consists mainly of C_x, C_r, a feedback resistor (10 kΩ), and an operation amplifier. The current passing through the feedback resistor is the sum of the current flowing through C_x or C_x+C_r and the compensation current given by the multiplier subcircuit (block 6). The output voltage V_1 of the differentiator is fed into a multiplier integrated circuit (IC) AD633 (block 7) together with the voltage which comes from the voltage source with phase shifted by 90° through a standard phase shifter (block 2). Therefore the output voltage V_2 of the multiplier is composed of a dc voltage signal and a double-frequency ac voltage signal. A low pass filter (block 9), consisting of two-stage active filters with cutoff frequency of 1 kHz, is then used to eliminate the ac signal and give the dc voltage signal to appear intact at the output terminal (V_5). Because the output voltage V_5 is in proportion to the capacitance C_r (or C_x+C_r), if the capacitance changes periodically between C_r and C_x+C_r, the output voltage V_5 will appear as a square wave.

The control signal used to switch the relay is generated by the oscillator subcircuit (block 4) operating at a frequency of 100 Hz. The oscillator subcircuit consists of a NE555 IC, which is capable of producing accurate time pulses, two external resistors (VR_3 and 470 Ω) and a capacitor (1 μF) to control the oscillation frequency and duty cycle of the wave form. The oscillation frequency can be tuned by varying the resistance of VR_3. It is possible that parasitic inductance and resistance are introduced into this circuitry by the relay and a transient voltage ripple could happen at the beginning when the relay switches, so a lock-in subcircuit (block 10) is used to eliminate the effect of transient response and accurately extract the amplitude of the square wave. This subcircuit consists of four stages, including voltage amplifiers, a multiplier, and a zero offset unit. The first stage in this subcircuit is a noninverted amplifier with fixed voltage gain, by which the voltage V_5 is enhanced. In the second stage, the enhanced voltage is then multiplied by the control voltage signal fed from the NE555 oscillator using AD633 IC. Of the enhanced voltage only the component having the same frequency and phase with respect to the control voltage signal from NE555 will be extracted. This measurement process is the so-called

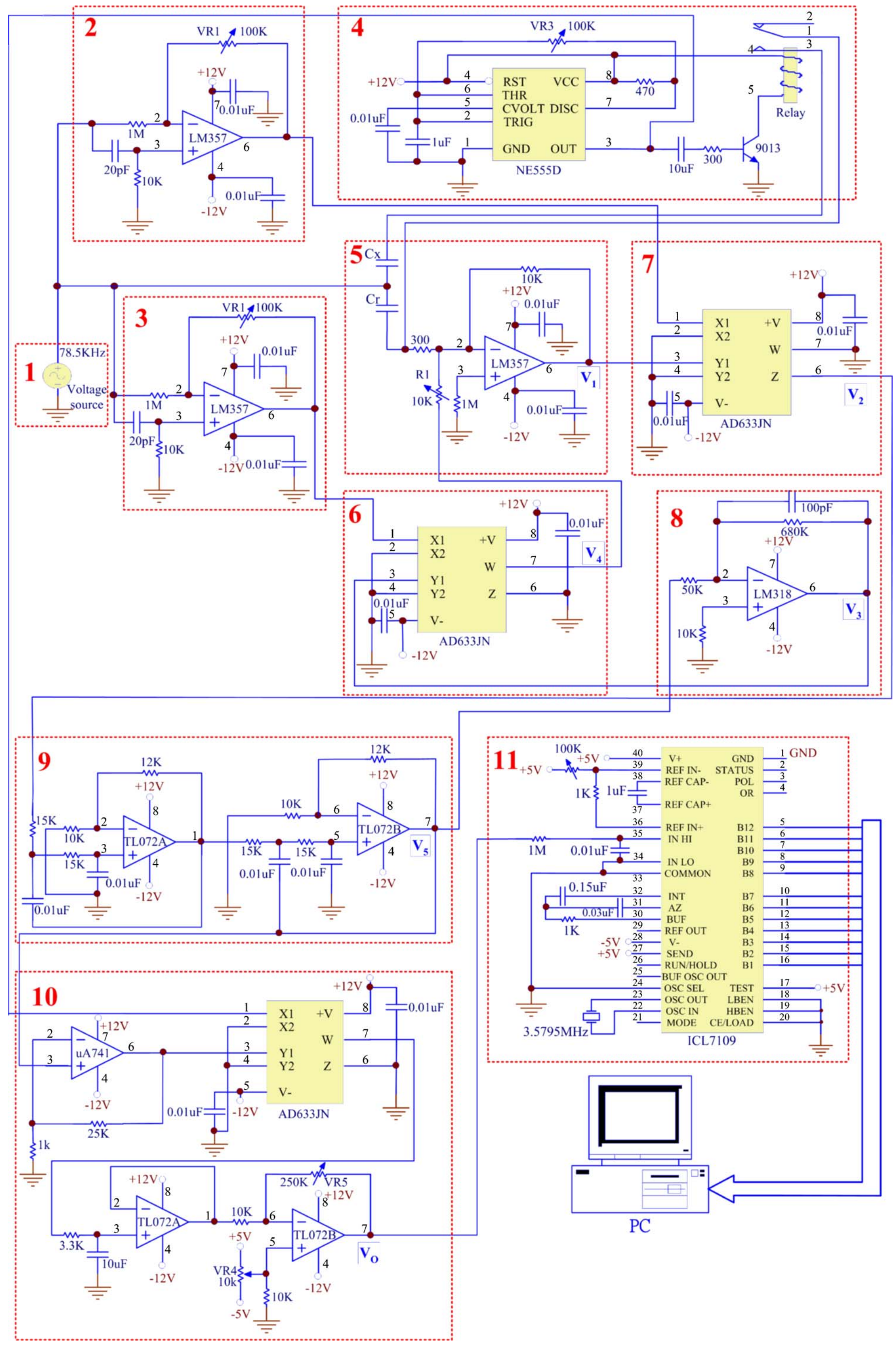

FIG. 2. (Color online) Electronic circuit diagram of the proposed circuitry: (1) voltage source; (2) +90° phase shifter; (3) −90° phase shifter; (4) oscillator; (5) differentiator; (6) current compensation multiplier; (7) signal multiplier; (8) integrator; (9) low pass filter; (10) lock-in detection subcircuit; and (11) analog-to-digital converter subcircuit.

lock-in detection. The third stage is a unit-gain buffer, which follows the AD633 multiplier to avoid the loading effect. The final stage is an operational amplifier, which is used to adjust the output voltage to a suitable level for different ranges of C_x and to zero the offset voltage as C_x is not connected. The analog output voltage V_o of the above-mentioned lock-in detection subcircuit is fed into a monolithic 12 bit ADC ICL7109 (block 11), through which a personal computer can acquire the digital data. The upper limit of the analog input voltage can be adjusted by a variable resistor $(100\ \mathrm{k}\Omega)$ connected to the pin 39. The circuitry configuration designed makes this measurement system highly user friendly.

The upper square wave (scaled by 0.005 and offset by 0.12 V for comparison with the lower square wave) in Fig. 3 is the control signal generated by the oscillator for switching the relay, while the lower square waves with transient ripples are the output voltages V_5 taken at the output terminal of the low pass filter for $C_r=100$ pF and various C_x values. The

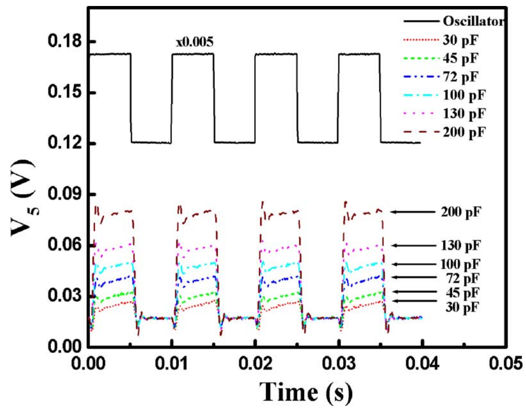

FIG. 3. (Color online) Square-wave output voltage signals from the control oscillator taken at the output terminal of the low pass filter for different values of C_x.

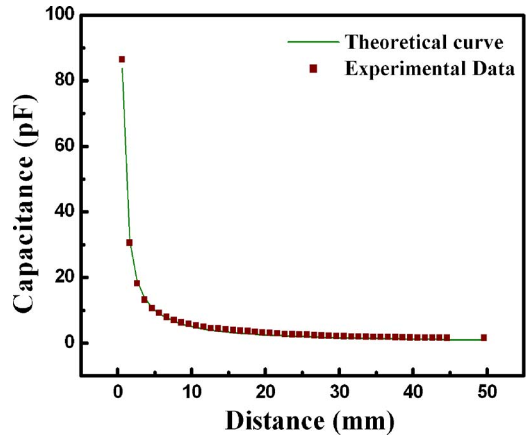

FIG. 5. (Color online) Measured capacitance (solid squares) and theoretical values (solid line) plotted against the plate separation for parallel electrodes.

amplitude shows a proportional increase with increasing C_x. The transfer characteristic, i.e., the final analog output voltage V_o versus the capacitance under test C_x, has been measured for the capacitance in the range of 0–100 pF for different magnification factors, which is determined by the variable resistor VR_5 in the lock-in subcircuit. The results are shown in Fig. 4, revealing a good linearity. It should be noted that the output voltage V_o gets saturated near the supply voltage, so it is practical to tune the VR_5 to a suitable value to measure a wide range of capacitance values with associated sensitivities. For example, when VR_5 is set to 101 kΩ the measurable range is limited below 50 pF but with a high sensitivity reaching $\Delta V/\Delta C = 202.2$ mV/pF.

III. APPLICATIONS

A. Displacement

The capacitance of two metal plates separated by a dielectric material is given by

$$C = \varepsilon \frac{A}{d}, \tag{4}$$

where ε is the permittivity of dielectric material, A is the area of metal plate, and d is the distance between the two plates. The product of distance and capacitance is a constant value when the area of metal plate and the permittivity are fixed. If we change the distance d, the capacitance is also changed. So it is possible to monitor a distance by measuring the capacitance. The experimental setup was made by fixing two pieces of metal plates to the two terminals of a plastic vernier. Each plate has area of 57 cm^2 and thickness of 0.2 mm. Connection wires are welded onto the metal plates for signal extraction. The distance between the two metal plates can be easily controlled by sliding the plastic vernier. For this experiment, the distance is changed from 1 mm to 5 cm. The measured capacitances (solid squares) deduced from the capacitance-voltage transfer characteristic and the theoretical values (solid line) calculated from Eq. (4) are shown in Fig. 5. A good agreement between the measured data and the theoretical values is found.

B. Height of liquid

The capacitance can also change as a result of different dielectric materials used. So measuring the capacitance can be used to determine the height of liquid in a container with two metal plates on both its sides. The inset of Fig. 6 shows the schematic drawing of a rectangular container made of acryl. The metal plates are fixed on both side walls of container and the height of liquid is marked on the see-through acryl wall. When water (or some kind of liquid) is poured

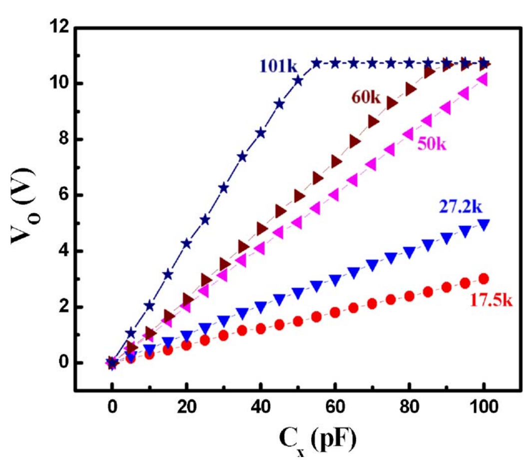

FIG. 4. (Color online) Output voltage as a function of the capacitance under test (C_x) for different values of VR_5.

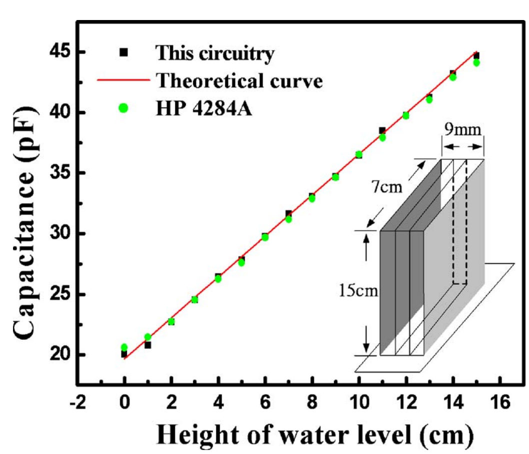

FIG. 6. (Color online) Capacitance measured by this circuitry (solid squares) and precision *LCR* meter (solid circles) as well as, theoretical values (solid line) plotted against height of water level. The insert is the schematic drawing of the rectangular container made of acryl.

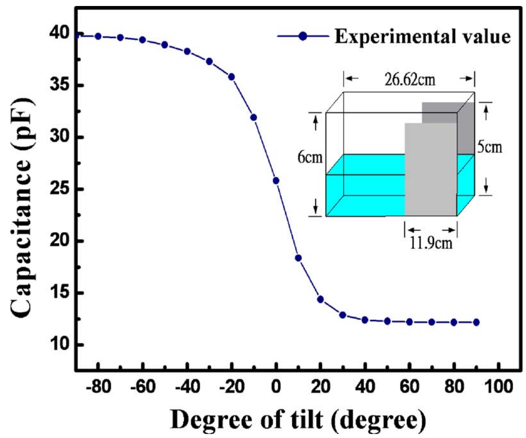

FIG. 7. (Color online) Measured capacitance vs degree of tilt. The insert is the schematic drawing of the experimental equipment made of acryl.

into this container to a certain level, the total capacitance between two plates can be divided into two parts. The one below the liquid level is named the lower capacitor, and the other one above the liquid level is named the upper capacitor. These two capacitors are connected in a parallel configuration. For the lower capacitor the dielectric material between two plates is the water layer sandwiched in the acryl plates, while the dielectric material becomes an air gap for the upper capacitor. In order to calculate the theoretical values of the capacitance in different levels of water (or some kind of liquid), first the equivalent dielectric constant of air gap and water layer sandwiched in the acryl plates should be determined. We measured the capacitances in empty and full of water conditions, respectively. The equivalent dielectric constants derived from Eq. (4) are 16.45×10^{-12} and 38.2×10^{-12} F/m for air gap and water layer sandwiched in two pieces of acryl, respectively. For the geometric dimension shown in the inset of Fig. 6 and assuming that the height of water h is unknown, the capacitance can be written as

$$C=\left(\frac{15-h}{15}16.45+\frac{h}{15}38.2\right)\frac{105}{0.9}\frac{1}{100}+0.48\ (\text{pF}), \qquad (5)$$

where 0.48 pF is the capacitance resulting from a strip of sealed acryl on the edge sides. If the height of water is changed, then the capacitance will be modified. We perform this experiment for the height below 15 cm. The measured values are shown in Fig. 6, presented by solid squares. Furthermore, we also measure the capacitance as a function of height of water using precision *LCR* meter (HP 4284) and the results are shown in Fig. 6 by solid circles. The theoretical values derived from Eq. (5) are also depicted by solid line in Fig. 6. The measured data using this circuitry match well the data measured by HP 4284A and agree to the theoretical values.

C. Degree of tilt

Similar to the second application described above, in this experiment we measure the capacitance to monitor the degree of tilt. The inset in Fig. 7 shows the schematic drawing of a sealed acryl box which has two metal plates fixed on the right-hand side and is partly filled with water. When the sealed acryl box is level, the height of water and air goes 50-50 between the two metal plates. When the sealed acryl box is tilted down to the right side, the height of water between the two plates is increased, in other words, the capacitance is increased. If the sealed acryl box is tilted down to the left side, the height of water between the two plates is decreased and a smaller capacitance is observed. The sealed acryl box has been tilted at different angles between +90° and −90° in steps of 10°. The measured results are shown in Fig. 7 by solid circles, and the solid curve is a guide to the eye. A good linear relationship between the tilt degree and the capacitance is observed ranging from −20° to 20°, in a resolution of −0.401 75 pF/deg. Assuming that the resolution of voltage in this capacitance measurement system is 1 mV, a high resolution of 0.012° for small angle measurement can be achieved.

IV. DISCUSSION

A cost-effective and high-performance circuitry was developed for the measurement of small capacitance. The high sensitivity of $\Delta V/\Delta C=202.2$ mV/pF can be achieved by this circuitry. Three experiments (displacement, height of liquid, and tilt angle) were designed and performed to show the applications and demonstrate the capability of this circuitry. Using this circuitry various capacitances spreading in a wide range can be measured by changing the capacitance of C_r or tuning the resistance of VR_5. We design a high precision and inexpensive circuitry for measuring the small capacitance. It is very convenient to equip this circuitry with an analog/digital acquisition card to feed the data into a computer to complete an automatic monitor or control system. This circuitry is also very useful for the differential capacitance sensors.

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