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Inhomogeneous electrical characteristics in 4H–SiC Schottky diodes

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Abstract
Hundreds of current–voltage (I–V) measurements of Ni, Pt and Ti Schottky diodes on 4H–SiC were conducted at low applied voltages. The SiC substrates contained homoepitaxial layers grown by either chemical vapor deposition or sublimation. While near-ideal contacts were fabricated on all samples, a significant percentage of diodes (∼7%–50% depending on the epitaxial growth method and the diode size) displayed a non-ideal, or inhomogeneous, barrier height. These 'non-ideal' diodes occurred regardless of growth technique, pre-deposition cleaning method, or contact metal. In concurrence with our earlier reports in which the non-ideal diodes were modeled as two Schottky barriers in parallel, the lower of the two Schottky barriers, when present, was predominantly centered at one of the three values: ∼0.60, 0.85 or 1.05 eV. The sources of these non-idealities were investigated using electron-beam-induced current (EBIC) and deep-level transient spectroscopy (DLTS) to determine the nature and energy levels of the defects. DLTS revealed a defect level that corresponds with the low- (non-ideal) barrier height, at ∼0.60 eV. It was also observed that the I–V characteristics tended to degrade with increasing deep-level concentration and that inhomogeneous diodes tended to contain defect clusters. Based on the results, it is proposed that inhomogeneities, in the form of one or more low-barrier height regions within a high-barrier height diode, are caused by defect clusters that locally pin the Fermi level.

(Some figures in this article are in colour only in the electronic version)

Introduction

Schottky contacts are integral components of the currently available commercial SiC devices, namely Schottky diodes and metal–semiconductor field-effect transistors (MESFETs). Due to its high temperature stability, large blocking voltage and thermal conductivity, SiC is ideal for applications in high temperature, high-power and high frequency electronic devices.

Although commercial SiC devices are available, current epitaxial material still suffers from defects that diminish the performance of the electronic devices. Excess current under both forward and reverse bias decreases the reliability and reproducibility of rectifying contacts to SiC.

The effects of selected defects on the reverse breakdown characteristics of SiC Schottky diodes [1–4] are well understood. Although some studies [5–9] have addressed non-ideal electrical behavior at low or moderate forward voltages, the effects of specific defects are not clear. Our recent study [10] showed evidence that defects, such as stacking faults and point defects, if present in high local concentrations, can locally pin the Fermi level at lower than ideal values and result in excess current at low forward voltages. The present study extends the prior studies through deep-level transient spectroscopy (DLTS) and electron-beam-induced current (EBIC) characterizations as well as current–voltage (I–V) and capacitance–voltage (C–V) measurements. Furthermore, two different diode fabrication processes on SiC

Table 1. Specifications of the 4H–SiC samples used in this research.

Sample number	Epitaxial layer thickness (μm)	Doping conc. $N_D - N_A$ (cm^{-3})	Epitaxial growth method	Diode metal(s)	Diode diameter (μm)	% of non-ideal diodes at R.T.	Characterization methods
CS 378	36	Mid-10^{16}	Sublimation	Ni	500	48	*I–V*, DLTS
S 247	36	Low-10^{16}	Sublimation	Ni	500	50	*I–V*, DLTS, EBIC
CVD 1	9	1×10^{16}	CVD	Ni	500	50	*I–V*, DLTS
Wafer 1	3	2.2×10^{16}	CVD	Ni, Ti, Pt	500	30	*I–V*, EBIC, CL
Wafer 2	26	2.5×10^{15}	CVD	Ni	500, 300	10	*I–V*, EBIC, CL

epilayers, produced either commercially or non-commercially by chemical vapor deposition (CVD) or sublimation, were employed to determine whether inhomogeneous Schottky contacts are unique to a particular diode fabrication process or a SiC growth method. The results in this study show that the Schottky-barrier inhomogeneities are common among the different samples.

Chemical vapor deposition is the most advanced method of growing SiC epitaxial layers. The advantages of CVD growth include the high purity of the epitaxial films and uniform doping concentration. The primary disadvantage is the relatively slow growth rate, typically a few μm h^{-1} [11]. Epitaxial growth via sublimation of SiC provides higher growth rates (>50 μm h^{-1}) [12] and thicker epitaxial layers which are required for high-power devices. However, sublimation epitaxy suffers from higher impurity incorporation, specifically boron.

Experimental procedure

Single crystal n-type 4H–SiC substrates with one surface (0 0 0 1) polished were purchased from Cree, Inc. (Durham, NC). The substrates were off-axis, oriented 8° towards $\langle 1\,1\,\bar{2}\,0\rangle$ and doped with N at concentrations $>1 \times 10^{18}$ cm^{-3}. On these substrates, 4H–SiC homoepitaxial layers were grown either at Linköping University (Linköping, Sweden) or purchased from Cree Research.

Specifications of the epitaxial layers are given in table 1. Four of the samples were provided by Linköping University: for two of the samples (CS 378 and S 247), the epitaxial layer was grown by sublimation (see [12] for details); for the other two samples (CVD 1 and Wafer 2), the epitaxial layer was grown by CVD. Wafer 1 contained an epitaxial layer grown commercially (at Cree, Inc., Durham, NC) by CVD.

The first four samples listed in table 1 were degreased in acetone and propanol, and then etched for 10 min in 10% HF to remove the thin oxide layer that was expected to be present on the surface. A sacrificial oxide layer of approximately 150 nm thick on samples from Wafer 1 was grown in oxygen at a temperature of 1100 °C, and then was removed using 10% HF. Ohmic contacts were formed on the backsides of the samples by sputtering a thick (∼1500 Å) layer of Ni and annealing for 15 min at 950 °C in Ar. Prior to the deposition of the Schottky contacts on the front side of the samples, the samples were again degreased and etched for 10 min in 10% HF, rinsed in de-ionized water and blown dry with nitrogen. The samples were then loaded into a UHV system (3×10^{-8} Torr) and desorbed at ∼700 °C for 15 min to remove hydrocarbons from the surface. Schottky contacts of either 100 or 500 Å thickness and 500 μm diameter were deposited through a shadow mask by electron-beam evaporation from elemental sources (99.95–99.995% pure). Metals used as Schottky contacts were Ti, Ni and Pt; these metals have work functions of $\phi_M = 4.33$ eV, 5.25 eV and 5.64 eV, respectively.

Wafer 2 contained a 26 μm thick epilayer with a doping concentration of 2.5×10^{15} cm^{-3}. A sacrificial oxide layer of approximately 150 nm thick was grown in oxygen at a temperature of 1150 °C, and then was removed using 10% HF. An Ohmic contact was formed on the backside of the sample by evaporating Ni and annealing in an Ar+H_2 mixture for 10 min at 950 °C. An SiO_2 layer between 1 and 2 μm thick was deposited using PECVD and patterned using standard photolithography techniques. The diode areas were defined by etching the patterned oxide using a buffered HF solution (NH_4F+H_2O+HF). Schottky contacts were fabricated by thermal evaporation of Ni. Standard photolithography was used to define the diodes within the oxide holes and with overlap onto the oxide wall. Finally, the excess Ni was removed using $FeCl_3$. The measured diodes were circular with diameters of 500 and 300 μm.

The Schottky contacts were characterized using *I–V* measurements. The *I–V* measurements were performed using an HP 4155B semiconductor parameter analyzer and a Signatone S-1060H-4QR high temperature prober. The *C–V* measurements were conducted using an HP 4284A LCR meter at frequencies of 1 MHz and 100 kHz and a voltage sweep of −10 to 1 V.

Electron-beam-induced current (EBIC) measurements were performed on both wafers using a Phillips XL-30 scanning electron microscope with a field emission gun at accelerating voltages from 5 to 30 kV and magnifications from 125× to 1000×. Secondary electron images were recorded for comparison. Deep-level transient spectroscopy (DLTS) measurements were performed on the Schottky contacts at temperatures from 90 to 350 K, with a bias voltage of −5 V, and a filling pulse of 5 V. Analysis of the DLTS data was performed using a double boxcar set-up, with a t_1/t_2 ratio of 1.3. Minority carrier transient spectroscopy (MCTS) measurements were performed on a few diodes on sample CS 378 to determine the boron concentration of the material.

Results

The *I–V* characteristics of approximately 600 diodes in total were measured between −20 V and 5 V. Of these diodes, 500 were on Wafer 2: all of these diodes were Ni. Whereas a majority of the diodes displayed near-ideal characteristics under forward bias (solid line in figure 1(*a*)), a significant percentage displayed a 'knee' at low voltages, characteristic of a non-ideal Schottky diode (diamonds in

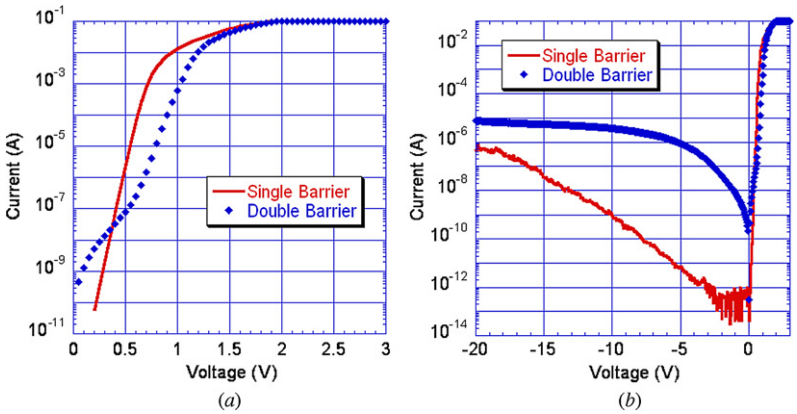


Figure 1. Near-ideal (solid line) and non-ideal (diamonds) Ni Schottky contacts to 4H–SiC with epitaxial layers grown by sublimation epitaxy under forward (*a*) and reverse (*b*) bias.

Table 2. Summary of *I–V* and *C–V* data of near-ideal diodes from selected samples in this study.

Sample number	Ideality factor	Barrier height (eV) (*I–V*)	Barrier height (eV) (*C–V*)
CS 378	1.26	1.17	1.53
CVD 1	1.06	1.35	1.43
Wafer 1	1.25	1.25	1.37

figure 1(*a*)). The percentage of non-ideal diodes varied from 5% to 50%, depending on the epitaxial growth method and diode size. Note that the near-ideal contacts have a much lower reverse leakage current than the non-ideal contacts, as shown in figure 1(*b*). Although two of the CVD samples (Wafers 1 and 2) contained a lower percentage of non-ideal diodes than sublimation samples, one of the CVD samples (CVD 1) contained approximately the same percentage as the sublimation samples. For all samples measured, there appeared to be no significant spatial dependence of the diode behavior as a function of position on the wafer/sample, except for a somewhat higher tendency for non-ideal diodes near the edge of Wafer 2. Clustering of the non-ideal diodes was not apparent in any of the samples investigated.

While there are significant variations across each sample in the *I–V* measurements, the *C–V* measurements show little overall variation. Table 2 summarizes the *I–V* and *C–V* data for near-ideal diodes. For sample CVD 1 the ideal barrier height for single-barrier diodes is approximately 0.08 eV less than the average *C–V* barrier heights. For sample CS 378, the *C–V* barrier height is approximately 0.36 eV larger than the ideal barrier height. The large discrepancy between Schottky-barrier heights determined by *I–V* and *C–V* for the sublimation sample (CS 378) might be due to termination of the SiC growth that results in a compensated layer at the surface. This could be the result of deposition during the cool down phase of the growth chamber, decreasing the nitrogen solubility in the material and creating a thin compensated layer with a higher Schottky-barrier height observed using *C–V* measurements.

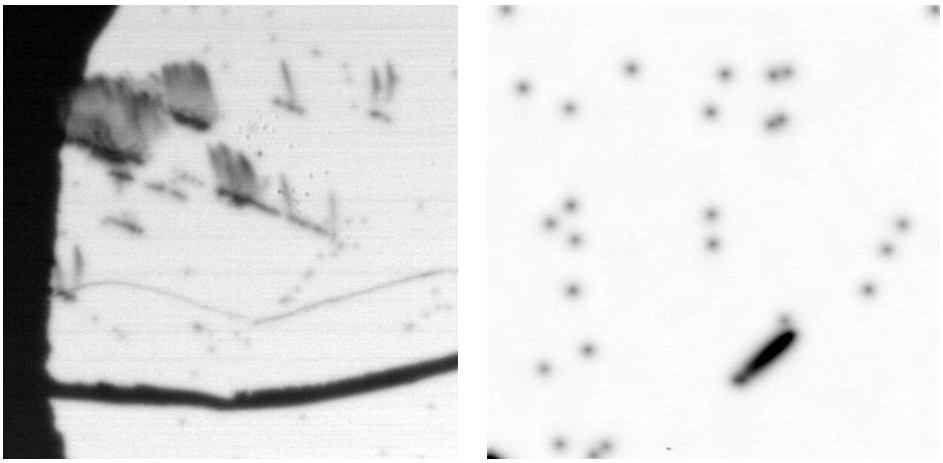
The near-ideal and non-ideal characteristics were modeled to determine quantifiable parameters, such as the Schottky-barrier height(s). Near-ideal Schottky contacts were modeled using the thermionic-emission equation [13], and non-ideal diodes were modeled as consisting of two barrier heights in parallel, as proposed in [6, 7, 10]. Details of our model for near-ideal and non-ideal contacts can be found elsewhere [10].

The near-ideal Ni diodes had Schottky-barrier heights of ∼1.30 eV and 1.20 eV for the CVD and sublimation epitaxial layers, respectively. Near-ideal Pt and Ti diodes were also formed on samples with CVD epitaxial layers for comparison. The average near-ideal Schottky-barrier heights were 1.40 and 0.80 eV for Pt and Ti, respectively. The non-ideal diodes for all the three metals had a range of high-barrier Schottky-barrier heights, ranging from 0.80 to 1.35 eV. The low-barrier Schottky-barrier heights (giving rise to the 'knee' in the log *I–V* characteristics) were predominantly centered at one of the three values: ∼0.60 eV, 0.85 eV and 1.05 eV

Two primary types of features were observed in EBIC characterizations of the CVD and sublimation material (both images from Wafer 1): dark streaks attributed to stacking faults (figure 2(*a*)) and circular spots attributed to dislocations or growth pits [14] (figure 2(*b*)). The lengths of the streaks match the calculated length of the projection of a stacking fault that is inclined (8°) on the basal plane, that originates at the substrate/epilayer interface and that terminates at the epilayer surface. Additionally, the dark lines are all oriented in a specific direction, as would be expected for stacking faults in this single-crystalline material. Due to material dicing and other sample processing, the exact crystallographic orientation of the dark lines could not be determined.

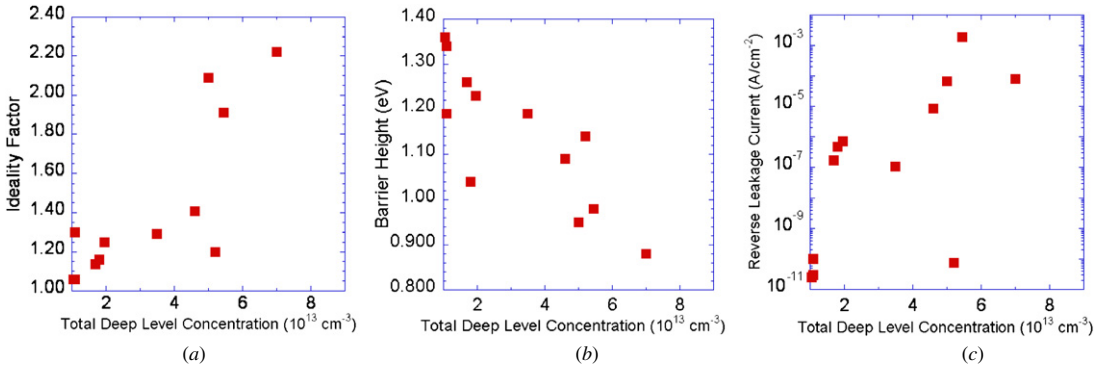
Whereas previous reports [7, 15] indicated a linear relationship between the ideality factor and the number of EBIC dark spots, no such correlation was observed in this research study. Some near-ideal diodes had a larger number of dark spots than non-ideal diodes. Near-ideal diodes also contained isolated stacking faults. However, the double-barrier diodes in all samples investigated had a noticeably higher concentration of stacking faults, figure 2(*a*). This phenomenon was only observed in the non-ideal diodes. The trend was observed for samples with and without sacrificial oxidation.

Deep-level transient spectroscopy (DLTS) was performed on the sublimation epitaxy sample CS 378 and the reference sample CVD1. The DLTS measurements revealed three majority-carrier deep-level states. The primary deep-level state in both samples was located at $E_C - 0.64$ eV, which is attributed to the Z_1/Z_2 point defect [16]. The concentration



(*a*) (*b*)

Figure 2. EBIC images of 'non-ideal' diodes to CVD material with (*a*) multiple stacking faults (upper left), and (*b*) an enlarged view of a stacking fault and surrounding screw dislocations.



(*a*) (*b*) (*c*)

Figure 3. (*a*) Ideality factor, (*b*) barrier height and (*c*) reverse leakage current plotted as a function of the total deep-level state concentration measured in Ni diodes on 4H–SiC CVD and sublimation epitaxy samples.

of the defect was in the range of 1–2 $\times$ 10^{13} cm^{-3} for the CVD sample, and 2–8 $\times$ 10^{13} cm^{-3} for the sublimation epitaxy sample. In the sublimation epitaxy sample, two additional defects were detected in few of the diodes. These deep levels are located at $E_C - 0.29$ eV and $E_C - 0.37$ eV and are believed to be ID 3 and ID 4 defects [16], respectively. Their concentrations were much less than the Z_1/Z_2 deep level, ~7–9 $\times$ 10^{12} cm^{-3}. The additional deep-level states and higher deep-level concentrations in the sublimation epitaxy sample likely result from the higher growth temperatures required, because higher temperature results in more vacancies. Since all of the deep levels detected are related to vacancies or vacancy complexes, it is a logical conclusion that the growth temperature affects the deep-level defect concentrations. Minority carrier transient spectroscopy was conducted on some of the diodes to determine the boron concentration in the sublimation epitaxy samples. The concentration varied only slightly, between 1.1 $\times$ 10^{15} cm^{-3} and 1.4 $\times$ 10^{15} cm^{-3}.

Parameters extracted from *I–V* characteristics (ideality factor, barrier height and reverse leakage current measured at -10 V) are plotted as a function of the total deep-level defect concentration in figure 3. In general, the ideality factors and reverse leakage currents increased with the total deep-level defect concentration, and the barrier heights decreased with the total deep-level defect concentration. These results suggest that there is either a direct or indirect association of the deep-level states with the electrical performance of the diodes. We propose that although the overall concentrations of the deep levels are three orders of magnitude less than the doping concentration of the epilayers, local regions with substantially higher defect densities could account for the observed changes in the diode behavior.

In our earlier study [10], we proposed that the low-barrier inhomogeneities with Schottky barriers of 0.60, 0.85 and 1.05 eV were caused by localized Fermi level pinning by high concentrations of specific defects. The local concentrations of these defects appear to be sufficiently high in only a variable, but significant, minority of diodes, i.e., those that show the described non-ideality at room temperature. For example, we observed 3C–SiC stacking faults at 2.40 eV using site-specific cathodoluminescence. If measured from the valence band, this energy corresponds with a level at ~0.85 eV below the conduction band of 4H–SiC. As a result, the Fermi level in that region could be pinned at 0.85 eV below the conduction band, if the local concentration of the stacking faults is sufficiently high. Similarly, the low-barrier Schottky-barrier heights of 0.60 eV could be attributed to local Fermi level pinning by the

Z_1/Z_2 point defects (located at 0.64 eV below the conduction band) observed in the present study. Although common to all 4H–SiC epitaxial layers, the Z_1/Z_2 defect would be required to be present in high local concentrations according to this model. Interestingly, we previously reported [10, 17] a 2.65 eV cathodoluminescence peak that was observed only in non-ideal diodes; this energy, if measured from the valence band, corresponds with a defect level at 0.65 eV below the conduction band, and thus a possible match with the Z_1/Z_2 point defect. Also in our prior study [17] we showed the intensity of the 2.65 eV (and the 2.2 eV) peak varies with position within individual diodes. This result supports the claim that the concentration of point defects is not constant within the SiC.

We must note here that, due to technical constraints, the DLTS measurements were performed on different samples than those examined using CL. This may explain why only the DLTS level at $E_C - 0.65$ eV matches one of the broad-area CL emissions (at 2.65 eV) in our previous studies [17]. We also strongly consider the possibility that DLTS does not detect the levels from site-specific CL because of the latter technique's localized nature.

The low-barrier Schottky-barrier heights of 1.05 eV may correspond to CL emissions of 2.20 eV observed previously in non-ideal diodes [17]. Although there are numerous point defects at this energy level that could be associated with this low Schottky-barrier height [17], we do not discuss this issue here.

Conclusions

Current–voltage measurements of hundreds of Schottky diodes on 4H–SiC homoepitaxial layers revealed Schottky-barrier inhomogeneities in a significant minority of diodes regardless of the SiC growth technique, pre-deposition cleaning method, or contact metal. This study expands our earlier work that focused on two (CVD) SiC samples for which non-ideal diodes were modeled as two Schottky barriers in parallel and for which the lower of the two modeled barriers were predominantly centered at one of the three values: 0.60, 0.85 or 1.05 eV. Our previous results showed a correlation between defects levels at 0.85 and 1.05 eV and the low-barrier Schottky-barrier height. In this study, DLTS revealed a defect centered at 0.60 eV, which could be the source of the 2.65 eV cathodoluminescence peak observed previously in non-ideal diodes and to the third low-barrier Schottky-barrier height of 0.60 eV determined by *I–V* measurements. In all non-ideal Schottky diodes, clusters of defects, such as stacking faults or dark spots, were observed. Additionally, an increase in the deep-level concentration tended to produce stronger non-ideal behavior in terms of ideality factors, reverse leakage current and Schottky-barrier heights. These results further support the hypothesis previously presented that high local concentrations (e.g., clusters) of defects can cause localized Fermi level pinning, which in turn produces the low-barrier regions. When the low-barrier regions are incorporated within the high (ideal)-barrier of the diode, an inhomogeneous Schottky-barrier diode is produced.

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