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Performance enhancement of solution-processed amorphous WZTO TFT with HAO gate dielectric via power ultrasound technology☆

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ABSTRACT

In this paper, power ultrasound technology (PUT) is employed to prepare the high-k hafnium-aluminum oxide (HAO) dielectric and thin film transistor (TFT). The continuous propagation of high-intensity ultrasonic waves in the metal oxide precursor solution can improve the dissolution efficiency of the solute and speed up the formation of the HAO precursor solution. The prepared HAO films have a smooth surface roughness of 0.36 nm and high optical transmittance of 85 %. Moreover, HAO films obtain excellent electrical properties with a relative permittivity of 15.9 and a leakage current density of 9.1×10^{-8} A/cm^2 at 2 MV/cm as well. Finally, we successfully fabricate TFT with HAO dielectric using PUT, these TFTs exhibit switch characteristics with field effect mobility of 18.7 $cm^2v^{-1}s^{-1}$, threshold voltage (V_{th}) of −0.47 V, and Vth shift of 0.35 V under positive gate bias stress. The results show that the PUT is a promising method that can remarkably decrease the preparation time of the precursor solution and improve the TFT performance.

1. Introduction

Solution processing has attracted widespread attention in large-area electronic devices such as amorphous oxide semiconductor thin-film transistors (AOS-TFTs) and organic solar cells with the advantages of a simple preparation process, low cost, and easily achievable stoichiometric tunability [1–5]. However, the solution processing approach is often accompanied by high-temperature treatment and a longer reaction time for formulating the precursor solution, which significantly increases the loss of time and resources and limits the application of the solution method [6–9]. So, we discover a power ultrasound technology (PUT) to resolve this problematic issue which is a quick and effective way to create homogenous and stable metal oxide precursor solutions in minutes which can significantly enhance the efficiency of preparing precursor solutions [10–12]. Our previous study has confirmed that the WZTO active layer TFTs fabricated by the PUT method can remarkably improve the reaction time of the WZTO precursor solution. However, there are few related studies on preparing the gate dielectric using the PUT method [13].

As an essential component of AOS TFTs, the gate dielectric plays a critical role in the performance of the TFT. In the past, low-k SiO_2 films were widely used as industry-standard gate dielectrics, resulting in most TFTs requiring high drive voltages [14]. However, with the rapid development of display technology in the direction of low power consumption and high resolution, TFTs must have lower driving voltages and smaller sizes. Some researchers have tried to increase the gate capacitance per unit area by reducing the thickness of SiO_2 film to improve the performance of TFTs [15]. However, as the dielectric gate thickness continues to decrease, the gate leakage current caused by direct electron tunneling increases, and SiO_2 is unable to offer sufficient reliability, which leads to higher power consumption [16–18]. Therefore, the conventional low-k SiO_2 gate dielectric is no longer sufficient, and a new high-k material is needed to replace it. The high-k gate dielectric can provide a thicker physical thickness, suppress direct electron attempt penetration, and maintain optimal gate capacitance, thus reducing gate leakage current and its resulting high-power consumption and improving device performance and reliability [19–22]. In recent years, various high-k gate dielectrics such as aluminum oxide (Al_2O_3) [23,24], hafnium oxide (HfO_2) [25,26], and zirconium oxide (ZrO_2) [27,28] have been used as potential candidates to replace conventional dielectric SiO_2 gates in TFTs. Among them, Al_2O_3 has a large band gap (~9 eV) and a high breakdown electric field, but it has a low

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dielectric constant (9) [24]. In contrast, HfO_2 has a high electrical constant (25), which provides a larger capacitance and allows sufficient charge injection into the TFT semiconductor layer, improving the on-state current of the device and reducing the driving voltage [29]. Therefore, HfAlO (HAO), a composite of Al_2O_3 and HfO_2, can exhibit more desirable properties and is expected to be a promising material for high-k gate dielectrics. Our previous work has investigated the effect of different Hf and Al ratios on the properties of HAO films. HAO films with a 2:1 ratio of Hf to Al exhibited excellent properties. However, the previous method of preparing HAO thin films was complicated and time-consuming, which is different from the concept of resource conservation [30].

This paper uses an efficient and green technique called PUT to prepare the HAO precursor solution. The spin-coated HAO films by PUT are thoroughly investigated and used as the gate dielectric of thin film transistors. It is the first report to prepare the tungsten zinc tin oxide (WZTO) active layer and HAO dielectric layer of an integrated TFT device by PUT.

2. Experimental section

First, the 0.3 mol/L HAO precursor solution is prepared by mixing hafnium dichloride oxide octahydrate ($HfCl_2O{\cdot}8H_2O$) [Alfa Aesar, 98 %] and aluminum-tri-*sec*-butoxide (Al $(OC_4H_9)_3$) [Sigma Aldrich, 97 %] into 2-methoxy ethanol (2-MOE). The atomic ratio of Hf: Al is 2:1. The WZTO precursor solution is prepared by mixing tungsten hexachloride (WCl_6) [Alfa Aesar, 99 %], zinc acetate dihydrate ($Zn(CH_3COO)_2{\cdot}2H_2O$) and chloride pentahydrate ($SnCl_4{\cdot}5H_2O$) [SIGMA, 98 %] in 2-methoxy ethanol by hydration method. The molar ratio of W: Sn: Zn in the precursor solution with a concentration of 0.3 M was 1: 30: 70. Our previous experiments have shown that 10 min is the most appropriate PUT treatment time [13]. In this experiment, the ultrasonic probe is immersed into the solution for ten minutes and the frequency is 20 kHz and the power is 300 W.

The stacked TFTs are fabricated with a bottom gate bottom contact structure on the glass substrate. A 50 nm thickness indium tin oxide (ITO) is sputtered and patterned as the gate electrode. The HAO precursor solution is spin-coated on that substrate. Repeat the above process three times to obtain the desired thickness, and then the HAO layer is etched and patterned with 1 % hydrofluoric acid at room temperature. Next, the 50 nm ITO deposited by AS is patterned into source and drain electrodes and annealed at 300 °C for one hour. The active layer is formed as follows: WZTO film is spin-coated on the HAO dielectric layer in the same process. The WZTO film is patterned by photolithography and etched with normal-temperature oxalic acid. Finally, the TFT device is annealed at 500 °C. The channel width (W) is 25 μm and the length (L) is 5 μm of the TFTs.

The thermal behavior of the HAO precursor solution is analyzed through thermogravimetric analysis (TGA, Q5000IR). The surface topography is inspected by atomic force microscope (AFM, Nanonavi SPA-400 SPM) and the average roughness of films is calculated according to AFM data, and chemical shift in HAO films is obtained by X-ray photoelectric spectroscopy (XPS). The optical properties are detected by UV–Vis spectrometer (H-3900, Hatachi). The thickness of the HAO films is measured by the step profiler (ET-150). Electrical measurement of devices is carried out with a semiconductor characterization system (Keithley, 4200-SCS) at room temperature in the dark.

3. Results and discussion

The ultrasonic probe is immersed in the solution container, and during the ultrasonic treatment, sound waves propagate through pressure oscillations in the liquid medium. PUT uses ultrasound to generate sonochemical reactions in the solution and form cavitation bubbles. The turbulence, growth, shrinkage, and rupture of cavitation bubbles will trigger physical and chemical changes that accelerate the alcoholization process of the precursor solution. PUT is proposed as a fast and convenient way to prepare oxide semiconductor precursor solutions directly. Table 1 compares existing solution processing routes and the PUT method. Compared with traditional water bath methods, the PUT method dramatically improves the efficiency of precursor solution preparation and successfully obtains excellent performance.

Table 1
Previous work on solution-processed oxide films.

Material	Process method	E_b (MV/cm)	J_{leak} (A/cm^2) @ (MV/cm)	k	Ref.
ZrO_x	stir 2 h	5	4.8×10^{-7} (@2)	13	[38]
HfO_x	stir 12 h	–	3.0×10^{-8} (@2)	8.1	[39]
Al_2O_3	water bath 3 h	–	7.0×10^{-7} (@1)	8.1	[40]
AlO_x	stir 4 h	–	2.5×10^{-6} (@0.26)	9.7	[41]
$Y_{1.2}Sc_{0.8}O_3$	stir 8–12 h	3.8	5.0×10^{-6} (@2)	9.6	[42]
LZO	stir 3 h	5.8	4.0×10^{-7} (@2)	13.1	[21]
HAO	water bath 3 h	4.5	1.69×10^{-7} (@2)	12.1	[30]
HAO	**PUT 10 min**	**5.9**	**9.1×10^{-8} (@2)**	**15.9**	**This work**

Fig. 1(a) shows the TGA curves of the HAO precursor solution, TG analysis is carried out in the air and the heating rate is 10 °C/min. The HAO precursor solution obtained by PUT for 10 min is consistent with the result of the water bath for 3 h, compared with the results of our previous studies [30]. Fig. 1(b) shows the transmittance of the HAO films with annealing temperatures of 400, 500, and 600 °C. All HAO films can obtain a high average transmittance (greater than 85 %), which meets the application requirements in the field of transparent display. Owing to their high transparency at the visible light wavelength, HAO thin films are supposed to have the potential to be applied to transparent electronic devices. Moreover, the optical band gap (Eg) of HAO thin films annealed at 400, 500, and 600 °C are 5.35, 5.44, and 5.68 eV, respectively. The band gap value is calculated by the Tauc formula: (ahv) 2 = C (hv - Eg) [31]. With the temperature increases, the Eg increase of the HAO films may be attributed to the reduction of defects in the film with high annealing temperature.

Fig. 2 demonstrates the corresponding XPS spectra of Al 2p, Hf 4f, and Cl 2p of HAO films with different temperatures. Table 2 shows the bond energies of Al 2p and Hf 4f at different annealing temperatures. As the annealing temperature rises, the chemical shift can be transferred to the low-energy region, which may be due to the gradual oxidation of metal cations, which reduces the distance between adjacent metal ions, reduces the voids in the membrane, and makes the HAO film denser [32]. It can be also seen from Fig. 2(c) that Cl relative impurities can be effectively eliminated when the annealing temperature is more than 400 °C, which is consistent with the TGA results [33].

Fig. 3 shows the surface morphology image of HAO films with different annealing temperatures for one hour, and the film thickness is 100 nm. Then calculate the root mean square (RMS) roughness value based on the AFM image. The RMS values of the HAO film after annealing at 400, 500, and 600 °C are 0.42, 0.36, and 0.67 nm, respectively. High-temperature annealing provides energy for the surface atoms of the film, thereby enhancing the diffusion of surface atoms. As these atoms are transferred to the existing voids and defects, the film's surface becomes smooth, and the surface roughness decreases. After the annealing temperature is higher than 500 °C, the RMS value increases, which is attributed to the growth of grains in the film after the annealing temperature increases [30]. The RMS roughness value of all HAO films is less than 1 nm, and they all show a uniform and smooth surface, which is beneficial to reduce carrier scattering on the semiconductor interface and improve the performance of TFT.

A parallel plate capacitor of MIM glass/ITO/HAO/Al structure was prepared to study the dielectric properties of the HAO film, as shown in Fig. 4(a). The film thickness of the HAO is 100 nm, and the diameter of

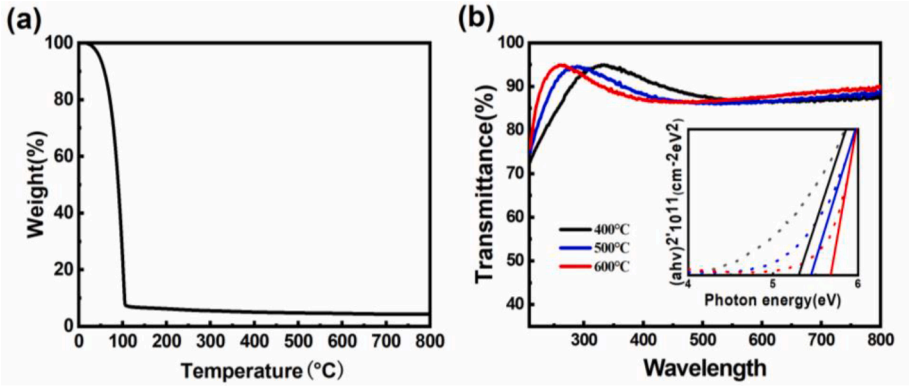

Fig. 1. (a) Thermal gravimetric curves of HAO precursor; (b) Optical transmission image of the HAO films with different annealing temperature. The inset shows the Tauc diagram of the HAO films.

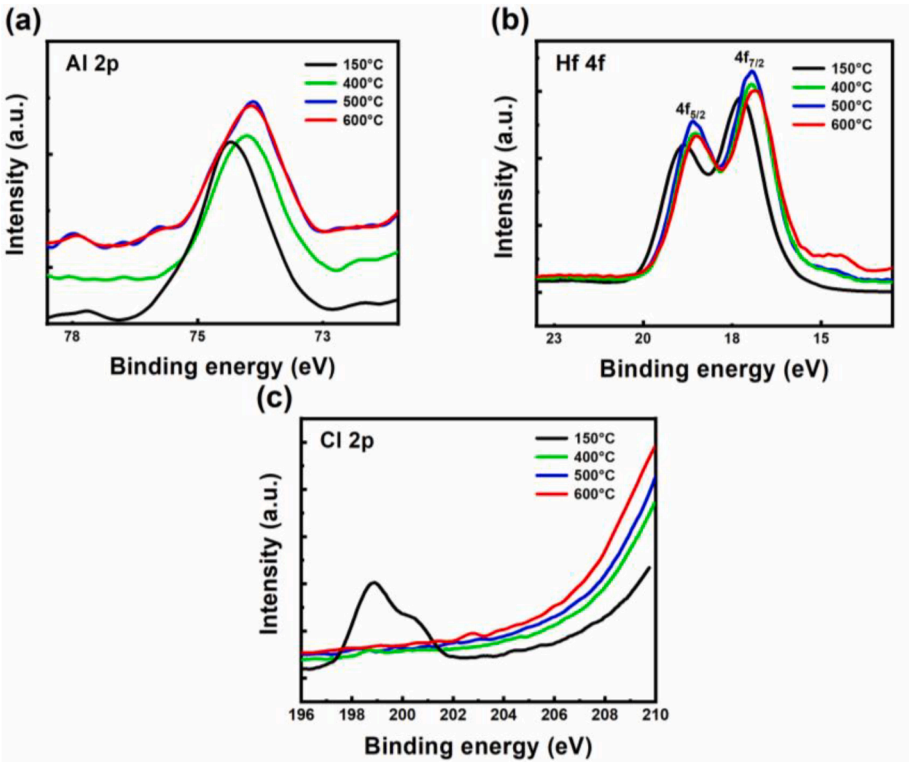

Fig. 2. XPS results for the (a) Al 2p, (b) Hf 4f and (c) Cl 2p spectra of the HAO films annealed at 400 °C, 500 °C, and 600 °C.

Table 2
XPS results of metal bond energy.

Annealing temperature (°C)	Al $2p_{3/2}$	Hf $4f_{7/2}$
150	74.3 eV	17.3 eV
400	73.9 eV	17.0 eV
500	73.8 eV	16.95 eV
600	73.8 eV	16.95 eV

the aluminum electrode is 1 mm. Fig. 4(b) shows the relationship between the leakage current density and the breakdown voltage with the applied electric field. The dielectric properties of the film are significantly influenced by the leakage current density. When the annealing temperature is raised from 400 °C to 500 °C, the J_{leak} of HAO film decreases gradually, and the HAO thin films annealed at 500 °C have the lowest J_{leak} of 9.1×10^{-8} A/cm^2 at 2 mV/cm and a high breakdown field of 5.9 MV/cm. Surface morphology is also essential in dielectric films. The film, annealed at 400 to 500 °C, has a smooth and dense surface, and electric fields are induced on the rough surface than on the smooth surface, so the J_{leak} is lower in the film annealed at 400 to 500 °C [28,34]. In addition, for the HAO films that anneal at 600 °C, a sudden increase in J_{leak} is observed at 5.1×10^{-7} a/cm^2 at 2 MV/cm, which is owing to the roughness of the HAO films that leads to the leakage current path.

Capacitance-voltage (C-V) curve at high frequency (100 kHz) is shown in Fig. 5(a). The thickness of HAO film is 100 nm. After annealing at 400, 500, and 600 °C, the capacitance density increases from 92 to 118, 120 nF/cm^2, and the relative dielectric constants of the HAO films are 12.4, 15.9, and 16.2. The relative dielectric constants of the films increase with the increase of the annealing temperature. The film's dielectric constant is related to the grain size and degree of crystallinity. AFM results confirm this. Fig. 5(b) shows the capacitance-frequency (C-F) curve of ITO/HAO/Al capacitors at 1 V. The frequency and voltage dependence of the HAO film are very weak, and as the annealing

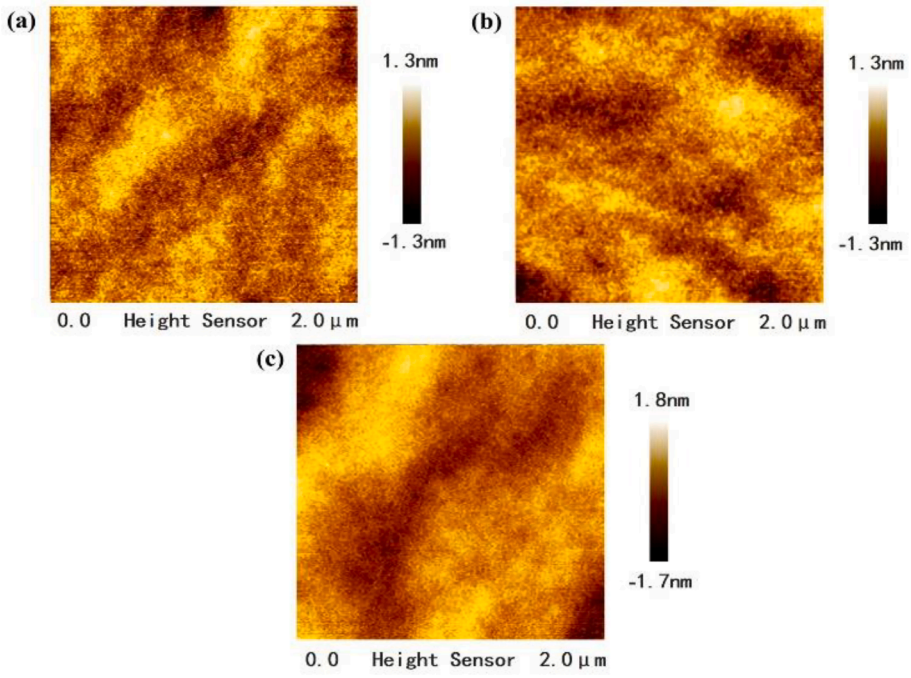

Fig. 3. AFM images of HAO films with different annealing temperatures: (a) 400 °C, (b) 500 °C, (c) 600 °C.

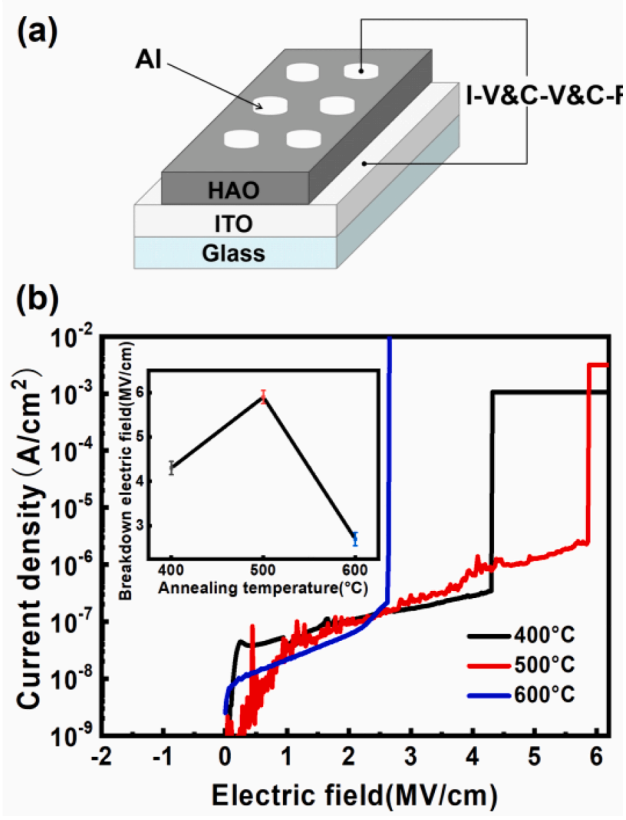

Fig. 4. (a) Schematic of the glass/ITO/HAO/Al capacitor, (b) J–E curves of HAO films annealed at 400 °C, 500 °C and 600 °C, the inset shows the data error bars about breakdown electric field.

temperature increases, the capacitance density increases. According to our previous research, the chemical reaction caused by heating causes the hafnium aluminum hydroxide to be converted to oxide, reducing the hydroxide impurities in the HAO film.

The WZTO TFTs with bottom-gate bottom-contact structures were fabricated on HAO film that had been annealed at 500 °C to research the device performance of the precursor solution prepared by PUT. Fig. 6(a) shows the Hysteresis characteristics of WZTO/HAO TFT, which had the mobility of 18.7 $cm^2v^{-1}s^{-1}$, a threshold voltage of −0.47 V, a sub-threshold slope of 0.11 V/dec, an I_{on}/I_{off} current ratio of 1.2×10^7. The performance of several solution-processed TFTs over the last few years is compared in Table 3. The WZTO/HAO TFT offers superior electrical qualities compared to other TFTs. This is likely due to the HAO films eliminating interfacial flaws and increasing device performance. The low voltage driving TFT built on this layer is advantageous in reducing power consumption and meeting the future development trend of low power consumption of display technology.

Fig. 6(b) is the output characteristic curve of the WZTO/HAO TFT device. The device is tested in a dark box at room temperature. The source and drain voltages vary from 0 to 5 V, the gate voltage varies from 0 to 1 V, and the interval voltage is 0.5 V. In the lower V_{GS} voltage range, the source-drain current increases with the increase of the voltage. There is no current blockage, indicating that a good ohmic contact is formed between the active layer and the electrode. In addition, it can be observed that there are obvious pinch-off behavior and current saturation characteristics, which shows that the gate voltage can well regulate the carrier transport in WZTO.

TFT devices will inevitably suffer from positive and negative gate bias stress in actual flat panel displays. Therefore, the most important issue is to maintain the long-term stability of the TFT device under positive and negative gate bias stress. To evaluate the positive bias stress (PBS) of WZTO/HAO TFT, the device is tested in a dark box at room temperature and the thickness of the gate dielectric in the TFT is 100 nm. To verify the stability of WZTO/HAO TFT in air, the gate bias voltage is set to 1 V, the V_{GS} is −2 V to 4 V, and the drain voltage is 1 V, as shown in Fig. 7(a). The WZTO/HAO TFT devices with passivation layers fabricated by the PUT method have excellent stability. After the gate bias stress time is 3600 s, the transfer characteristic curve shifts to the positive voltage direction, and the threshold voltage shifts (ΔV_{th}) is very small, only 0.35 V. When the PBS test is performed in the atmosphere, excess electrons accumulate in the channel layer, and the surrounding

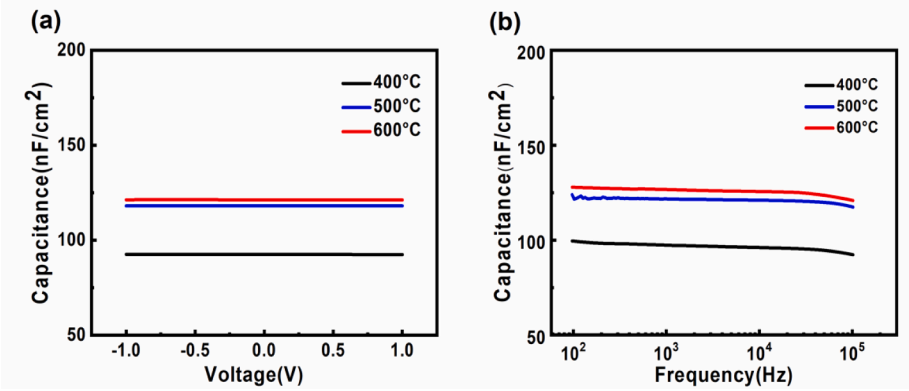

Fig. 5. (a) Capacitance-voltage and (b) capacitance–frequency curves of ITO/HAO/Al capacitor at the different annealing temperatures.

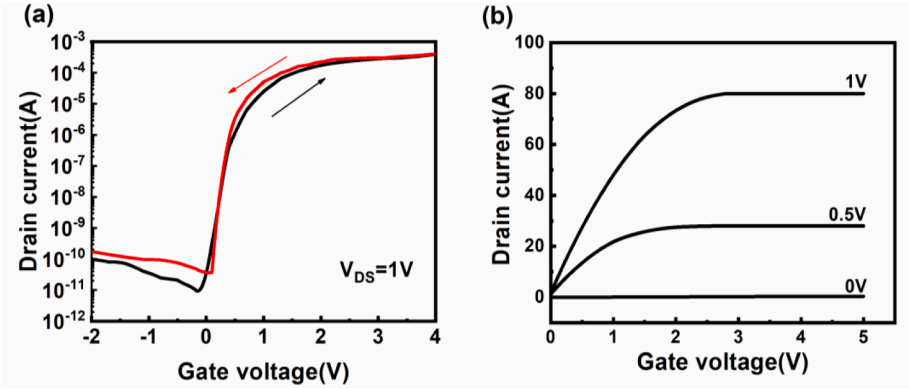

Fig. 6. (a) Hysteresis characteristic and (b) Output characteristic of the WZTO/HAO TFT device.

Table 3
Comparison of various solution processed TFTs performance.

Channel/dielectric	μ($cm^2v^{-1}s^{-1}$)	I_{on}/I_{off}	V_{th} (V)	Ref
IZO/HfO_2	0.46	6.31×10^5	3.04	[43]
InO_x/ZrO_x	1.65	1×10^5	–	[44]
In_2O_3/HfO_x	3.67	3.8×10^6	1	[45]
FTO/AlO_x	14.48	9.32×10^7	1.01	[46]
ZITO/HAO	13.5	7.2×10^6	−0.6	[47]
ZnSnO/DyO_x	2.5	2.4×10^6	0.5	[48]
ZnO/LZO	11.58	2.67×10^8	1.25	[49]
In_2O_3/SrO_x	5.61	1×10^7	0.11	[50]
In_2O_3/Yb_2O_3	4.98	1×10^6	–	[51]
InO_x/ZrLaO	2.2	2×10^6	0.59	[52]
WZTO/HAO	**18.7**	$\mathbf{1.2 \times 10^7}$	**−0.47**	**This work**

oxygen molecules are highly electronegative, which can capture electrons in the conduction band to form O^{2-}, and O^{2-} is adsorbed in the channel layer. Carriers will be depleted, so the threshold voltage will shift forward, which indicates that there are a few defects at the interface between the gate-insulating layer and the active layer [35].

In addition, even after the device is subjected to a bias voltage, the subthreshold swing of the TFT device does not change significantly, which indicates that the device does not produce additional defect states [36]. The performance and stability of TFTs are primarily determined by the gate-insulating layer. Materials with a higher k can compensate for the higher interface trap density, reduce SS and operating voltage, and improve the electrical performance of the device. The PUT is proven to be an effective method for preparing precursor solution and the HAO gate dielectric and can effectively enhance the WZTO TFT device's

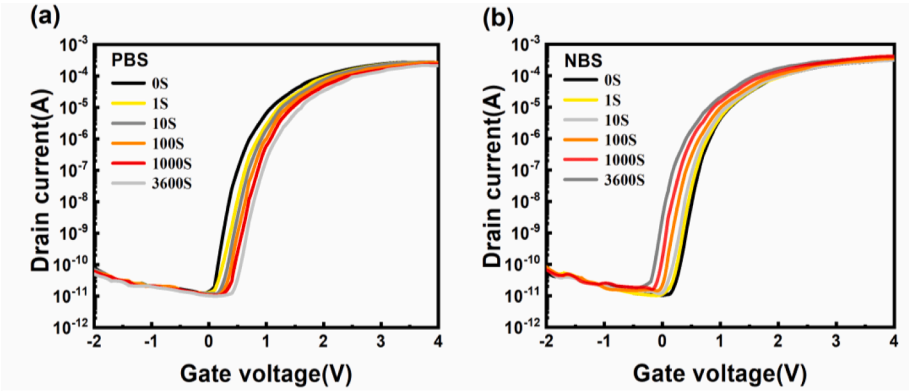

Fig. 7. Transfer curves of the WZTO/HAO TFT under (a) PBS and (b) NBS tests for 3600 s.

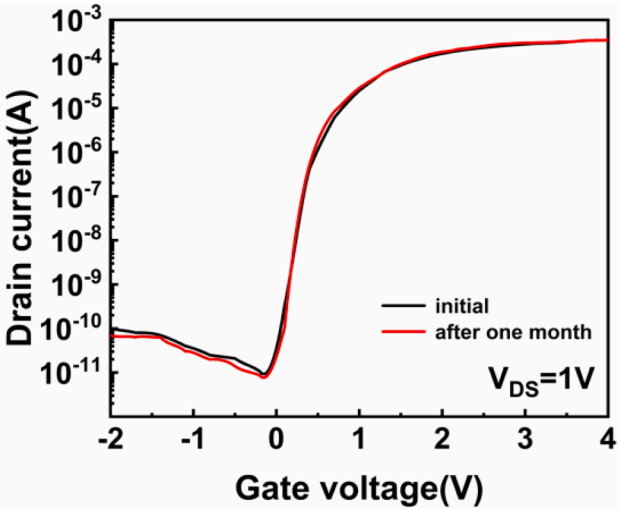

Fig. 8. Transfer characteristic curve of WZTO/HAO TFT with bottom gate bottom contact structure after one month.

performance.

Since AOS TFT is inevitably exposed to negative gate voltage for a long time when applying transparent electronic products, negative bias stress (NBS) stability is also an important index. Under the same test conditions as PBS, the gate bias is set to −1 V to measure the NBS stability curve of the WZTO/HAO TFT. The test result is shown in Fig. 7 (b). After 3600 s, the characteristic transfer curve of the device shifts to the negative direction of the voltage, and the threshold voltage shift is −0.48 V. The threshold voltage shift of the device caused by NBS is also minimal. Under normal circumstances, after a negative voltage is applied, free holes are attracted. After gathering at the gate insulating layer/active layer interface, some of the holes will remain trapped in the interface state or penetrate the gate dielectric layer, resulting in a negative shift of the transmission curve [37]. Storage stability of devices in the air for one month is shown in Fig. 8, which exhibits good storage stability of the TFT device using PUT, showing that the HAO film used in the PUT method is denser and reduces the effect of air on the device's performance.

4. Conclusions

In this paper, the high-k HAO dielectric precursor solution is rapidly formed by PUT at a frequency of 20 kHz and a power of 300 W within 10 min. It is a fast and efficient method for mixing metal-oxide precursor solution for high-quality dielectric with a smooth surface roughness of 0.36 nm and a high average transmittance of more than 85 %. From the XPS results, the metal bond energies decrease as the annealing temperature increases, and when the annealing temperature exceeds 400 °C, the Cl impurities are removed. The HAO gate dielectric also shows a low leakage current density of 9.1×10^{-8} A/cm^2 at 2 MV/cm and a very high breakdown field of 5.9 MV/cm. The prepared WZTO/HAO TFT has a high mobility of 18.7 cm^{2}v^{-1}s^{-1} and relatively good storage stability. The results indicate that PUT can be a promising method for preparing a precursor solution of dielectric.

CRediT authorship contribution statement

Sunjie Hu: Conceptualization, Methodology, Software, Investigation, Formal analysis, Writing – original draft. **Yanyu Yuan:** Data curation, Writing – original draft. **Cong Peng:** Visualization, Investigation. **Longlong Chen:** Software, Validation. **Xifeng Li:** Conceptualization, Funding acquisition, Resources, Supervision, Writing – review & editing. **Jianhua Zhang:** Resources, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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References

[1] J. Robertson, High dielectric constant gate oxides for metal oxide Si transistors, Rep. Prog. Phys. 69 (2) (2006) 327–396.
[2] E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: a review of recent advances, Adv. Mater. 24 (22) (2012) 2945–2986.
[3] S.Y. Lee, S. Chang, J.-S. Lee, Role of high-k gate insulators for oxide thin film transistors, Thin Solid Films 518 (11) (2010) 3030–3032.
[4] R. Chen, L. Lan, Solution-processed metal-oxide thin-film transistors: a review of recent developments, Nanotechnology 30 (31) (2019), 312001.
[5] A.C. Arias, J.D. MacKenzie, I. McCulloch, J. Rivnay, A. Salleo, Materials and applications for large area electronics: solution-based approaches, Chem. Rev. 110 (1) (2010) 3–24.
[6] J. Park, T. Gergely, Y.S. Rim, S. Pyo, Significant performance improvement of solution-processed metal oxide transistors by ligand dissociation through coupled temperature-time treatment of aqueous precursors, ACS Appl. Electron. Mater. 1 (4) (2019) 505–512.
[7] K.K. Banger, Y. Yamashita, K. Mori, R.L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol-gel on chip' process, Nat. Mater. 10 (1) (2011) 45–50.
[8] Y.H. Kang, K.S. Jang, C. Lee, S.Y. Cho, Facile preparation of highly conductive metal oxides by self-combustion for solution-processed thermoelectric generators, ACS Appl. Mater. Interfaces 8 (8) (2016) 5216–5223.
[9] H. Pu, Q. Zhou, L. Yue, Q. Zhang, Solution-processed indium gallium zinc oxide thin-film transistors with infrared irradiation annealing, Semicond. Sci. Technol. 28 (10) (2013).
[10] J. Xu, Y. Wang, H. Shan, Y. Lin, Q. Chen, V.A. Roy, Z. Xu, Ultrasound-induced organogel formation followed by thin film fabrication via simple doctor blading technique for field-effect transistor applications, ACS Appl. Mater. Interfaces 8 (29) (2016) 18991–18997.
[11] M. Eslamian, Excitation by acoustic vibration as an effective tool for improving the characteristics of the solution-processed coatings and thin films, Prog. Org. Coat. 113 (2017) 60–73.
[12] M. Souada, C. Louage, J.Y. Doisy, L. Meunier, A. Benderrag, B. Ouddane, S. Bellayer, N. Nuns, M. Traisnel, U. Maschke, Extraction of indium-tin oxide from end-of-life LCD panels using ultrasound assisted acid leaching, Ultrason. Sonochem. 40 (Pt A) (2018) 929–936.
[13] Y. Yuan, C. Peng, S. Yang, M. Xu, J. Feng, X. Li, J. Zhang, Rapid and facile method to prepare oxide precursor solution by using sonochemistry technology for WZTO thin film transistors, RSC Adv. 10 (47) (2020) 28186–28192.
[14] B.H. Wang, W. Huang, L.F. Chi, M. Al-Hashimi, T.J. Marks, A. Facchetti, High-k gate dielectrics for emerging flexible and stretchable electronics, Chem. Rev. 118 (11) (2018) 5690–5754.
[15] E.A. Chagarov, A.C. Kummel, Density functional theory simulations of high-k oxides on III-V semiconductors, in: Fundamentals of III-V Semiconductor MOSFETs, 2010, pp. 93–130.
[16] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, Nature 432 (7016) (2004) 488–492.
[17] J. Robertson, R.M. Wallace, High-K materials and metal gates for CMOS applications, Mater. Sci. Eng. R-Rep. 88 (2015) 1–41.
[18] G.D. Wilk, R.M. Wallace, J.M. Anthony, High-κ gate dielectrics: current status and materials properties considerations, J. Appl. Phys. 89 (10) (2001) 5243–5275.
[19] J.S. Lee, S. Chang, S.M. Koo, S.Y. Lee, High-performance a-IGZO TFT with ZrO2 gate dielectric fabricated at room temperature, IEEE Electron Dev. Lett. 31 (3) (2010) 225–227.
[20] N. Munzenrieder, C. Zysset, L. Petti, T. Kinkeldei, G.A. Salvatore, G. Troster, Flexible double gate a-IGZO TFT fabricated on free standing polyimide foil, Solid State Electron. 84 (2013) 198–204.
[21] S. Lee, S.H. Lee, N. On, J.K. Jeong, A solution-processed La-Zr-O dielectric at a low temperature for high-performance In-Ga-O transistors: engineering a precursor solution, Ceram. Int. 47 (5) (2021) 6918–6927.

[22] T.E. Taouririt, A. Meftah, N. Sengouga, M. Adaika, S. Chala, A. Meftah, Effects of high-k gate dielectrics on the electrical performance and reliability of an amorphous indium-tin-zinc-oxide thin film transistor (a-ITZO TFT): an analytical survey, Nanoscale 11 (48) (2019) 23459–23474.
[23] C. Avis, J. Jang, High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol-gel method, J. Mater. Chem. 21 (29) (2011) 10649–10652.
[24] W.Y. Xu, H. Wang, F.Y. Xie, J. Chen, H.T. Cao, J.B. Xu, Facile and environmentally friendly solution-processed aluminum oxide dielectric for low-temperature, high-performance oxide thin-film transistors, ACS Appl. Mater. Interfaces 7 (10) (2015) 5803–5810.
[25] M. Esro, G. Vourlias, C. Somerton, W.I. Milne, G. Adamopoulos, High-mobility ZnO thin film transistors based on solution-processed hafnium oxide gate dielectrics, Adv. Funct. Mater. 25 (1) (2015) 134–141.
[26] H. Shimizu, T. Sato, S. Konagai, M. Ikeda, T. Takahashi, T. Nishide, Temperature-programmed desorption analyses of sol-gel deposited and crystallized HfO2 films, Jpn. J. Appl. Phys. Part 1-Regul. Pap. Brief Commun. Rev. Pap. 46 (7A) (2007) 4209–4214.
[27] A. Liu, G.X. Liu, H.H. Zhu, F. Xu, E. Fortunato, R. Martins, F.K. Shan, Fully solution-processed low-voltage aqueous In2O3 thin-film transistors using an ultrathin ZrOx dielectric, ACS Appl. Mater. Interfaces 6 (20) (2014) 17364–17369.
[28] J.H. Park, Y.B. Yoo, K.H. Lee, W.S. Jang, J.Y. Oh, S.S. Chae, H.K. Baik, Low-temperature, high-performance solution-processed thin-film transistors with peroxo-zirconium oxide dielectric, ACS Appl. Mater. Interfaces 5 (2) (2013) 410–417.
[29] Y.S. Chun, S. Chang, S.Y. Lee, Effects of gate insulators on the performance of a-IGZO TFT fabricated at room-temperature, Microelectron. Eng. 88 (7) (2011) 1590–1593.
[30] L. Zhu, Y. Gao, X. Li, X.W. Sun, J. Zhang, Development of high-k hafnium–aluminum oxide dielectric films using sol–gel process, J. Mater. Res. 29 (15) (2014) 1620–1625.
[31] Y.J. Li, W.Y. Xu, W.J. Liu, S. Han, P.J. Cao, M. Fang, D.L. Zhu, Y.M. Lu, High-performance thin-film transistors with aqueous solution-processed NiInO channel layer, ACS Appl. Electron. Mater. 1 (9) (2019) 1842–1851.
[32] H. Lee, K. Beom, M. Kim, T.-S. Yoon, Post-annealing temperature-dependent electrical properties of thin-film transistors with a ZnO channel and HfOx gate insulator deposited by atomic layer deposition, Semicond. Sci. Technol. 35 (7) (2020).
[33] A. Liu, Z. Guo, G. Liu, C. Zhu, H. Zhu, B. Shin, E. Fortunato, R. Martins, F. Shan, Redox chloride elimination reaction: facile solution route for indium-free, low-voltage, and high-performance transistors, Adv. Electron. Mater. 3 (3) (2017).
[34] A. Liu, G.X. Liu, H.H. Zhu, F. Xu, E. Fortunato, R. Martins, F.K. Shan, Fully solution-processed low-voltage aqueous In2O3 thin-film transistors using an ultrathin ZrO (x) dielectric, ACS Appl. Mater. Interfaces 6 (20) (2014) 17364–17369.
[35] K. Zhao, Y. Gong, L. Yan, W. He, D. Wang, J. Wang, Z. Zou, C. Luo, A. Zhang, Z. Fan, J. Gao, H. Ning, G. Zhou, X. Lu, J. Liu, Room-temperature fabrication of high-quality lanthanum oxide high-κ dielectric films by a solution process for low-power soft electronics, Adv. Electron. Mater. 5 (10) (2019).
[36] A. Sharma, N.K. Chourasia, N. Pal, S. Biring, B.N. Pal, Role of electron donation of TiO2 gate interface for developing solution-processed high-performance one-volt metal-oxide thin-film transistor using ion-conducting gate dielectric, J. Phys. Chem. C 123 (33) (2019) 20278–20286.
[37] M.-S. Kang, W.-J. Cho, Verification of microwave annealing ambient effect on sol-gel-processed amorphous In–Ga–Zn–O thin-film transistors and application to inverter circuit, Semicond. Sci. Technol. 35 (3) (2020).
[38] M. Hasan, M.C. Nguyen, H. Kim, S.W. You, Y.S. Jeon, D.T. Tong, D.H. Lee, J. K. Jeong, R. Choi, High performance solution processed zirconium oxide gate dielectric appropriate for low temperature device application, Thin Solid Films 589 (2015) 90–94.
[39] S. Park, K.H. Kim, J.W. Jo, S. Sung, K.T. Kim, W.J. Lee, J. Kim, H.J. Kim, G.R. Yi, Y. H. Kim, M.H. Yoon, S.K. Park, In-depth studies on rapid photochemical activation of various sol-gel metal oxide films for flexible transparent electronics, Adv. Funct. Mater. 25 (19) (2015) 2807–2815.
[40] Y.L. Xu, X.F. Li, L.Y. Zhu, J.H. Zhang, Defect modification in ZnInSnO transistor with solution-processed Al2O3 dielectric by annealing, Mater. Sci. Semicond. Process. 46 (2016) 23–28.
[41] P.K. Nayak, M.N. Hedhili, D. Cha, H.N. Alshareef, High performance In2O3 thin film transistors using chemically derived aluminum oxide dielectric, Appl. Phys. Lett. 103 (3) (2013).
[42] W.B. Hu, B. Frost, R.L. Peterson, Thermally stable yttrium-scandium oxide high-k dielectrics deposited by a solution process, J. Phys. D: Appl. Phys. 49 (11) (2016).
[43] S. Lee, S.H. Lee, K. Woo, Y.J. Kim, S.Y. Bak, M. Yi, Performance improvement of solution-processed InZnO thin film transistor with HfO2 vertical diffusion layer, Microelectron. Eng. 215 (2019).
[44] X. Dong, G.D. Xia, Q. Zhang, L.B. Li, H.Y. Gong, J.Q. Bi, S.M. Wang, Room-temperature UV-ozone assisted solution process for zirconium oxide films with high dielectric properties, Ceram. Int. 43 (17) (2017) 15205–15213.
[45] J. Chung, Y.J. Tak, W.G. Kim, J.W. Park, T.S. Kim, J.H. Lim, H.J. Kim, Low-temperature fabrication of solution-processed hafnium oxide gate insulator films using a thermally purified solution process, J. Mater. Chem. C 6 (18) (2018) 4928–4935.
[46] J. Li, Y.H. Zhou, D.Y. Zhong, X.F. Li, J.H. Zhang, Simultaneous enhancement of electrical performance and negative bias illumination stability for low-temperature solution-processed SnO2 thin-film transistors by fluorine incorporation, IEEE Trans. Electron Devices 66 (10) (2019) 4205–4210.
[47] X.F. Li, L.Y. Zhu, Y.N. Gao, J.H. Zhang, Solution-processed low-operating-voltage thin-film transistors with bottom-gate top-contact structure, IEEE Trans. Electron Dev. 62 (3) (2015) 875–881.
[48] B. Yang, G. He, Y.C. Zhang, C. Zhang, Y.F. Xia, F. Alam, J.B. Cui, Solution-processed DyOx for aging diffusion ZnSnO transistors and applications in low-voltage-operating logic circuits, IEEE Trans. Electron Dev. 66 (8) (2019) 3479–3484.
[49] M.M. Islam, J.K. Saha, R.N. Bukke, M.M. Hasan, M.M. Billah, N.N. Mude, A. Ali, J. Jang, Solution-processed La alloyed ZrOx high-k dielectric for high-performance ZnO thin-film transistors, IEEE Electron Dev. Lett. 41 (7) (2020) 1021–1024.
[50] C.X. Fan, A. Liu, Y. Meng, Z.D. Guo, G.X. Liu, F.K. Shan, Solution-processed SrOx-gated oxide thin-film transistors and inverters, Ieee Trans. Electron Dev. 64 (10) (2017) 4137–4143.
[51] Z.D. Guo, A. Liu, Y. Meng, C.X. Fan, B. Shin, G.X. Liu, F.K. Shan, Solution-processed ytterbium oxide dielectrics for low-voltage thin-film transistors and inverters, Ceram. Int. 43 (17) (2017) 15194–15200.
[52] Y.X. Fang, C. Zhao, I.Z. Mitrovic, C.Z. Zhao, High-performance and radiation-hardened solution-processed ZrLaO Gate dielectrics for large-area applications, ACS Appl. Mater. Interfaces 13(42) (2021) 50101–50110.