Asymmetric band offsets in silicon heterojunction solar cells: Impact on device performance

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Amorphous/crystalline silicon interfaces feature considerably larger valence than conduction band offsets. In this article, we analyze the impact of such band offset asymmetry on the performance of silicon heterojunction solar cells. To this end, we use silicon suboxides as passivation layers—inserted between substrate and (front or rear) contacts—since such layers enable intentionally exacerbated band-offset asymmetry. Investigating all topologically possible passivation layer permutations and focussing on light and dark current-voltage characteristics, we confirm that to avoid fill factor losses, wider-bandgap silicon oxide films (of at least several nanometer thin) should be avoided in hole-collecting contacts. As a consequence, device implementation of such films as window layers—without degraded carrier collection—demands electron collection at the front and hole collection at the rear. Furthermore, at elevated operating temperatures, once possible carrier transport barriers are overcome by thermionic (field) emission, the device performance is mainly dictated by the passivation of its surfaces. In this context, compared to the standard amorphous silicon layers, the wide-bandgap oxide layers applied here passivate remarkably better at these temperatures, which may represent an additional benefit under practical operation conditions. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4959988]

I. INTRODUCTION

Amorphous/crystalline silicon heterojunction (SHJ) solar cells can reach conversion efficiencies beyond 25%.[1–3] This is largely associated with their almost recombination-free surfaces, enabled by thin intrinsic hydrogenated amorphous silicon [a-Si:H(*i*)] passivation layers inserted between the wafer and its carrier collecting contacts. These contacts consist of doped a-Si:H layers (*n*-type for electron collection, *p*-type for hole collection), capped by transparent conductive oxides (TCO).[4] Such low recombination directly translates into the very high operating voltages characteristic for this technology and which are also key to their low temperature coefficient for the efficiency (TC) of down to −0.2%/°C at device level.[5,6] In their most simple design, SHJ solar cells feature electron and hole contacts at opposite wafer surfaces. In such a case, the doped/intrinsic a-Si:H contacting stacks at the front contribute to parasitic absorption and hence limited current output.[7] To circumvent this issue, replacement materials for the involved a-Si:H films are currently actively researched, featuring higher transparency, while maintaining their desired functionality (i.e., carrier collection and surface passivation, respectively). In this context, molybdenum oxide (MoOx) was recently demonstrated to be an efficient, highly transparent, hole collector in SHJ solar cells.[8–12] Inspired by similar concerns, we recently exchanged the intrinsic a-Si:H passivation layer by wider bandgap intrinsic hydrogenated amorphous silicon suboxide [a-SiO_x:H(*i*)] passivation layers.[13]

When implemented at the hole-collecting side, the anticipated optical benefits are unfortunately offset by losses in fill factor (*FF*).[13,14] We attributed this to the presence of a thermionic transport barrier for holes in our devices, where the barrier is a consequence of the increased valence band offset (VBO, 0.3–0.45 eV), associated with strongly hydrogenated,[13] wider-bandgap a-SiO_x:H(*i*) layers.[15,16] Whereas such barriers impede efficient hole collection in devices at room temperature, they can nevertheless be overcome by thermionic (field) emission.[13] Such carrier transport issues may be further exacerbated by the *n*-type character of intrinsic a-SiO_x:H layers due to oxygen incorporation.[17–20] This casts doubt whether a-SiO_x:H(*i*) window layers can actually be integrated into hole collecting contacts to yield simultaneously higher short-circuit current density (J_{sc})[13] *and* high *FF*.

Based on these arguments, we use, in this article, oxide layers as a tool to study carrier collection across SHJ interfaces, enabling us to establish unambiguously the ideal structure for SHJ devices that feature electron and hole contacts at opposite wafer sides. To this end, we integrate a-SiO_x:H(*i*) layers in SHJ devices in all topologically possible passivation-layer permutations for this device architecture. We use this set of show-case samples and apply common characterization tools, namely, temperature-dependent dark and light current-voltage measurements (*J*-*V*) and temperature-dependent photoconductance decay (PCD) measurements to determine the effective

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minority-carrier lifetime (τ_{eff}). This enables an in-depth analysis of transport and passivation mechanisms in these devices from which we gain insight in the influence on device performance of the passivation layers' properties and their band offsets with the underlying c-Si substrate in particular. Our work also opens the road towards the efficient integration of wider bandgap window layers in electron collecting contacts.

II. EXPERIMENTAL DETAILS

We fabricated devices with or without a-SiO$_x$:H(*i*) layers and implemented the hole collecting contact either at the front or at the rear in: (1) reference devices [Fig. 1(a) (I) and (II)], or devices with an a-Si:H(*i*)/a-SiO$_x$:H(*i*) stack beneath; (2) the a-Si:H(*p*) [Fig. 1(b) (I) and (II)]; or (3) the a-Si:H(*n*) layer [Fig. 1(c) (I) and (II)]. Note that we chose an a-Si:H(*i*)/a-SiO$_x$:H(*i*) passivation layer *stack*, as we systematically obtained low lifetime results with oxide-only layers, deposited directly on the wafer.[13] For simplicity, this wide-bandgap passivation stack will be denoted by "*I*" (or *I*-layer) in the remainder of this article [standard a-Si:H(*i*) passivation by "*i*" or "*i*-layer"], so, e.g., *ip/In* represents an SHJ solar cell collecting holes at the front and featuring an a-SiO$_x$:H(*i*) layer underneath the *n*-layer at the rear.

For device fabrication, *n*-type floatzone (FZ), (100)-oriented silicon wafers were used (4 in., resistivity of 4 Ω cm, nominal thickness of 240 μm). In a first step, we performed saw damage removal and random-pyramid texturing using potassium hydroxide, followed by a standard chemical wafer cleaning. After standard surface oxide removal by hydrofluoric acid (5%, 60 s), the amorphous silicon layers (intrinsic and doped) were deposited in a medium-sized (electrode area: 15 × 16 cm^2), plasma-enhanced chemical vapor deposition (PECVD) cluster tool (INDEOtec, Octopus 1) at 200 °C. For the depositions, the following gases were used: silane (SiH_4), hydrogen (H_2), phosphine (PH_3, for *n*-type doping), trimethylborane [TMB short for $B(CH_3)_3$, for *p*-type doping], and carbon dioxide (CO_2) as oxygen source. Further experimental details are given elsewhere.[13,21] All the devices received the same a-Si:H layers, yet different device structures were fabricated (Fig. 1). For the deposition of the a-SiOx:H(*i*) layers, we fixed the carbon dioxide to silane input gas flow ratio ($[CO_2]/[SiH_4]$, where $[CO_2]$ and $[SiH_4]$ represent the gas flows in sccm) to 0.8 and integrated identical *I*-layers in the devices as the ones shown in Figs. 1(b) and 1(c). As we reported earlier,[13] the material deposited with the $[CO_2]/[SiH_4]$ ratio of 0.8 exhibits a small increase in the bandgap of ∼0.1 eV, from the bandgap of a-Si:H(*i*) (1.7 eV) to ∼1.8 eV, which we mainly associated with an increase in hydrogen content and to a lesser extent to the presence of oxygen. Note that the value of 1.8 eV represents the effective bandgap, measured over the full a-Si:H(*i*)/a-SiO$_x$:H(*i*) stack. Assuming a VBO for the a-Si:H(*i*)/*c*-Si interface of 0.3 eV as reported elsewhere,[16] this leads to a VBO of ∼0.4 eV. Even though we focus on charge carrier transport in the present work, it is noteworthy that the oxide layers used here yet have no sufficiently wide bandgaps to yield a marked increase in J_{sc};[13] we essentially observed identical performance trends for devices with hole collection or electron collection at the front. Consequently, for the clarity of the article, we concentrate here mainly on the former in the discussion of the results (Fig. 1). On textured wafers, the a-Si:H(*i*)/a-SiO$_x$:H(*i*) stacks measured ∼6 nm in thickness. These layer thicknesses were extracted from spectroscopic ellipsometry data, taken on co-deposited planar glass samples, fitted with a Tauc-Lorentz multi-layer model. The devices were completed by indium tin oxide (ITO) sputtering and metallization (screen printed silver, Ag, grids at the front, sputtered Ag blanket at the rear). Each wafer featured three 2 × 2 cm^2 cells, which were defined by shadow mask sputtering of ITO and Ag layers. See also Ref. 21 for further details on device architecture.

The finished devices were characterized using *J*-*V* measurements as a function of temperature (25–85 °C) both under illumination and in darkness (hereafter called light or dark *J*-*V*) and suns-V_{oc} measurements.[22]

The investigations of τ_{eff}'s temperature dependencies were performed on symmetrically passivated, *n*-type FZ, 300-μm-thick, 4 Ω cm, (100)-oriented double-side polished

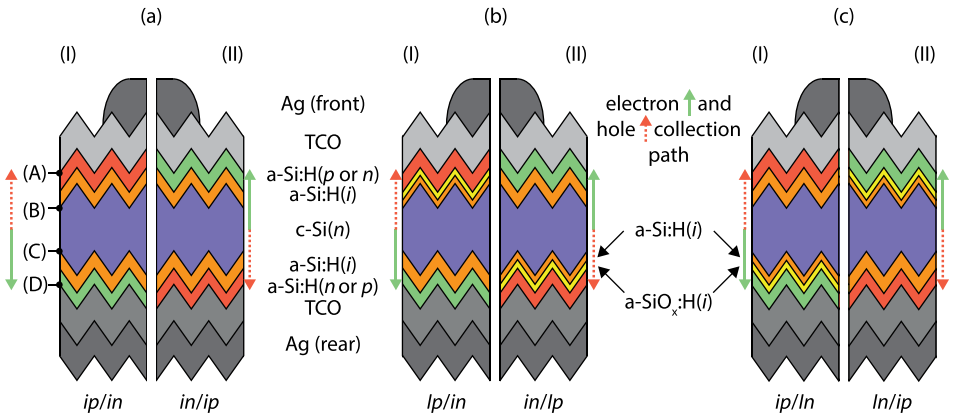

FIG. 1. Schematic of devices with hole contact at the front (I) or rear (II) investigated in this work. The solid and dashed arrows indicate the flow of charge carriers. (a) Reference all-a-Si:H devices with hole contact at (I) the front (*ip/in*) or (II) the rear (*in/ip*). (b) Devices with a-Si:H(*i*)/a-SiO$_x$:H(*i*) stack beneath the a-Si:H(*p*) layer, and (I) front (*Ip/in*) or (II) rear (*in/Ip*) hole collection; and the same for (c) with a-Si:H(*i*)/a-SiO$_x$:H(*i*) stack beneath the a-Si:H(*n*) layer (I) (*ip/In*) and (II) (*In/ip*). The labels (A)–(D) to the left indicate the different interfaces: TCO/a-Si:H(*p*), a-Si:H(*i*)/c-Si(*n*), etc.

TABLE I. Light *J-V* parameters obtained under standard testing conditions. The values given here represent the average over three cells on each wafer. The cell parameters of the best cell (with respect to efficiency) are given in parentheses. For the cell description, the stack on the left represents the front stack, while the stack on the right refers to the rear.

Structure (Fig. 1)	Cell	Label	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	*pFF* (%)	Efficiency (%)
(a) (I)	*ip*/*in*	*ip*/*in*	724 (726)	36.5 (36.5)	76.5 (76.9)	82.7 (83.6)	20.2 (20.3)
(a) (II)	*in*/*ip*	*in*/*ip*	718 (721)	36.6 (36.6)	76.0 (77.0)	83.4 (83.0)	20.0 (20.3)
(b) (I)	a-SiO$_x$:H(*i*)*p*/*in*	*Ip*/*in*	719 (719)	36.7 (36.9)	66.5 (66.9)	83.6 (83.7)	17.6 (17.7)
(b) (II)	*in*/a-SiO$_x$:H(*i*)*p*	*in*/*Ip*	705 (701)	36.6 (36.7)	64.4 (65.6)	82.2 (84.0)	16.6 (16.9)
(c) (I)	*ip*/a-SiO$_x$:H(*i*)*n*	*ip*/*In*	724 (724)	36.6 (36.6)	76.3 (76.6)	83.3 (83.4)	20.2 (20.3)
(c) (II)	a-SiO$_x$:H(*i*)*n*/*ip*	*In*/*ip*	717 (719)	36.5 (36.4)	75.0 (75.4)	82.3 (82.4)	19.6 (19.8)

silicon wafers. Note that these samples were taken from our previous study.[13] In this study, we used PECVD to deposit standard *i*-layers (~16 nm, denoted as *i*/*i*) or *I*-layers (denoted as *I*/*I* ~16 nm). For these samples, we used the same input gas flow ratio [CO_2]/[SiH_4] of 0.8 as for the devices. The samples were measured using a Sinton Instruments WCT-120-TS PCD system with a controllable temperature stage.[23]

III. RESULTS AND DISCUSSION

A. Temperature-dependent *J-V* analysis

The light *J-V* measurement performed at 25 °C yielded the values listed in Table I (average values, i.e., three cells per wafer and best cell result with respect to efficiency in parentheses). All the cells showed open-circuit voltages (V_{oc}) above 700 mV, including those with oxide stacks as passivation layers. For the *Ip*/*in* and *in*/*Ip* samples, we observe a characteristic difference in *FF* with respect to the reference sample of approximately 10% absolute at 25 °C.[48] Judging by the comparable pseudo-*FF* (*pFF*) values amongst the samples, which is an "idealized," resistance-free *FF* value, the *FF* loss cannot be related to significant differences in passivation (differences in V_{oc}). We therefore rather associate it with the insertion of an *I*-layer underneath the a-Si:H(*p*) layer (*Ip*/*in*). The presence of this layer results in the occurrence of an s-shaped *J-V* curve, which we link to a transport barrier for holes introduced by the VBO at the interface (B) (see Fig. 1).[13,16] The situation is illustrated in Fig. 2 which shows the increased VBO.[24–26,46] It is of note that the situation is different for the conduction band offset (CBO), which we assume to be subject only to minor changes when opening the oxide layer bandgap (CBO: 0.13–0.28 eV as reported elsewhere[15,27,28]). We base this assumption on the fact that our a-SiO$_x$:H layers mainly show an increased hydrogen content compared to the standard a-Si:H layers.[13] In this context, Schulze *et al.* found that additional hydrogen in an a-Si:H layer mainly varies the VBO and leaves the CBO virtually unaffected.[15] The same was found for silicon-carbon alloying by Brown *et al.*[29] Therefore, we argue that electron transport is largely unaffected over our "oxide" layers, rendering them promising candidates for application in devices with electron collection at the front.[13]

Returning to our measured *J-V* characteristics, the correlation between band offsets and s-shaped *J-V* curves was recently independently confirmed for SHJ as well as thin-film silicon solar cells.[20,30] Notably, the *FF* improves with increasing temperature, suggesting that the barrier is overcome by holes via thermionic emission or thermionic field emission. In turn, this results in a *positive* TC value for the *FF* values of both device polarities within the investigated temperature range [solid and open green diamonds, Fig. 3(a)].[13,31,32] An additional effect may be the unintentional *n*-type character of the *I*-layer due to oxygen

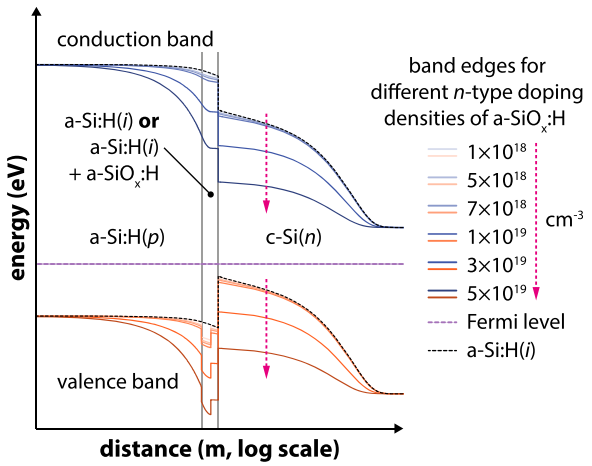

FIG. 2. Band diagram of the hole-collecting side of an SHJ device for: 3 nm plain a-Si:H(*i*) (black dashed line) and the a-Si:H(*i*)/a-SiO$_x$:H(*i*) (1.5 nm/1.5 nm) stack with increasing *unintentional* a-SiO$_x$:H *n*-type doping (indicated by the dashed arrows). Simulations performed with AFORS-HET.

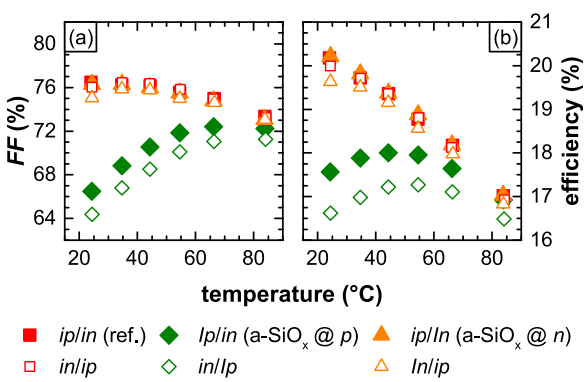

FIG. 3. Results obtained from light *J-V* measurements on *in*/*ip*, *Ip*/*in*, and *ip*/*In* devices with hole collection at the front (solid) and their inverse polarity counterparts (open). Temperature dependence of the (a) *FF* and (b) the efficiency. Note that each data point represents the average value of three 2 × 2 cm^2 cells on the same wafers.

incorporation, as reported by other authors.[17–20] In addition to the larger band offset, an *n*-doped passivation layer applied below the hole-collecting a-Si:H(*p*) layer will pull the bands downwards in energy and hence impede hole collection further. Minor changes in the bandstructure are already observed for comparatively low doping densities of $1–3 \times 10^{18}\,\mathrm{cm}^{-3}$, where typical doping densities of a-Si:H(*n* or *p*) layers are in the range of $1–5 \times 10^{19}\,\mathrm{cm}^{-3}$. To verify the precise contribution of this effect is beyond the scope of the present work, however.

Comparing now the results obtained for the *Ip/in* structure and the samples exhibiting an *I*-layer beneath the a-Si:H(*n*) layer [interface (C), Fig. 1] or the oxide-free reference samples [orange triangles and red squares, Fig. 3(a)], we see striking differences. These two types of devices show identical decreasing *FF* trends with temperature, suggesting that no overly pronounced transport barrier for electrons is present in the case of the *ip/In* and *In/ip* samples. This confirms that for the oxygen and hydrogen concentration (which largely dictate the values of the CBO and VBO) and the layer thickness used here, electrons are still efficiently collected, whereas hole collection is impeded.[33] Hence, in this case, it would be advisable to collect the holes at the rear, making void the need for an a-SiO_x:H "window" layer. In such a case, the reported collection issues can be avoided, while the device can still benefit from the improved transparency of the *I*-layers applied to the front beneath the electron-collecting layer. As our work mainly concerns carrier collection, a-SiO_x:H(*i*) layers with *wider* bandgap than those studied here, offering improved transparency in the blue, were not applied and will have to be tested in the future.

Even though it does not consider voltage dependent effects, represented, e.g., by *local* ideality factors,[34,35] a straightforward method to investigate the observed trends consists of fitting our experimental light and dark *J-V* data with a two-diode model with *fixed* ideality factors. The equivalent circuit of this model is shown in Fig. 4(a). The model is given by the following formula (with the light-generated current J_L, the dark saturation currents J_{01} and J_{02}, and the ideality factors n_{01} and n_{02} for the two respective diodes, the series resistance R_s, the shunt resistance R_{sh}, the Boltzmann constant k_B, and the absolute temperature *T*)

$$J(V) = J_L - J_{01}\left\{\exp\left[\frac{q(V+JR_s)}{n_{01}k_BT}\right]-1\right\} - J_{02}\left\{\exp\left[\frac{q(V+JR_s)}{n_{02}k_BT}\right]-1\right\} - \frac{(V+JR_s)}{R_{sh}}. \quad (1)$$

Here, we chose ideality factors of $n_{01}=1$ and $n_{02}=2$ for the two diodes, respectively, and use J_{01}, J_{02}, R_s, and R_{sh} as free fitting parameters. Classically, an ideality factor of 1 represents a perfect diode, while the value 2 accounts for depletion region recombination.[36] In SHJ devices, usually wafers of very high electronic quality are used. As a consequence, we make the following associations: (1) the first diode, with a dark saturation current density J_{01}, is linked with the passivation quality of the wafer surface; and (2) the second diode, with a factor J_{02}, is related to the junction quality. Figs. 4(b) and 4(c) show the example of the resulting fits, enabling the extraction of the series resistance (R_s) from both data sets, which qualitatively show the same trends [Fig. 4(d)].[47] Note that the fit of the dark *J-V* data deviates slightly from the data at lower voltages. This non-ohmic behavior was investigated already before.[37–39] Since this deviation impacts neither the operating voltage at the maximum power point nor the V_{oc} and the fit at higher voltages—the ones dominated by R_s—is reasonably good, we trust our extracted J_{01}, J_{02}, and R_s values as long as $R_{sh} > 1000\ \Omega\,\mathrm{cm}^2$, which is the case here. Compared to the other samples, the R_s values extracted for the *Ip/in* device systematically show significantly higher values and also a much more pronounced decrease with temperature. Assuming an Arrhenius dependency, it is possible to extract an activation energy for the R_s ($E_{act,Rs}$) from the data given in Fig. 4(d). The $E_{act,Rs}$ value represents an indirect measure of the band offsets and hence for its role in carrier transport. Despite its strong dependence, $E_{act,Rs}$ is not to be mistaken for the actual band offsets. Extracting $E_{act,Rs}$ for the dark *J-V* data, we obtain 345 meV, 165 meV, and 166 meV for the *Ip/in*, the *ip/In,* and the *ip/in* devices, respectively. The fact that the $E_{act,Rs}$ value of the *Ip/in* is more than double the value of the other two samples can be explained by the exacerbated barrier for holes [the VBO, interface (B), Fig. 1] and its unfavorable contribution to R_s. Yet, interestingly, we note that *all* our

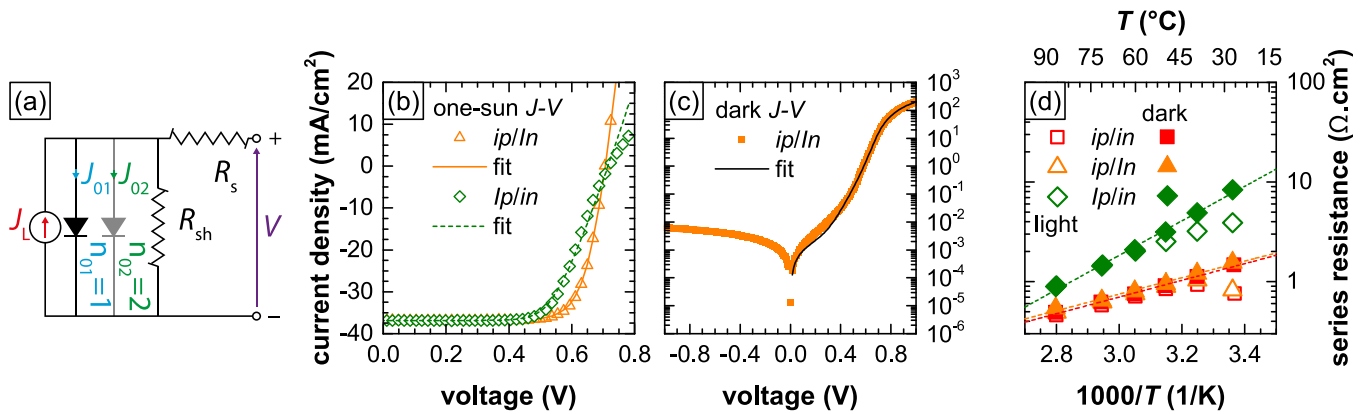

FIG. 4. (a) Equivalent circuit as used for the double-diode fitting model. (b) Example of fitted light and (c) dark *J-V* data used to extract the series resistance (R_s). (d) R_s data extracted from light (open) or dark (filled) *J-V* data fits. The dashed lines represent fits to R_s data obtained from the dark *J-V* data. The fitting results were used to extract the activation energy of the R_s.

devices qualitatively show a decreasing trend for their respective R_s values and a non-zero $E_{act,Rs}$. This points to the fact that carrier transport in reference *ip/in* as well as in *ip/In* cells is influenced by a temperature-dependent contribution to the R_s as well. A possible explanation for this phenomenon is the already discussed barriers associated with the band offsets. In this case, since both *ip/in* and *ip/In* cells essentially show identical trends, the determining barrier would be at the hole-collecting side as well. This would also mean that even our all-a-Si:H reference *i*-layers in principle features already too large VBO values (~0.3 eV)[16] to warrant fully unhindered hole collection at typical operating temperatures.

B. Transport and local ideality factor

In this section, we focus on the analysis of the transport mechanisms and recombination processes with the help of the local ideality factor (n_{local}) as introduced by McIntosh and Honsberg for homojunction devices.[40] The authors used this approach to investigate the influence edge recombination currents present in devices lacking full-area metallization. The parameter n_{local} is proportional to the differential of the *J-V* curve given as follows:

$$n_{local} = \frac{q}{k_B T} \cdot \left(\frac{\partial V}{\partial \ln(J)} \right). \quad (2)$$

Here, q is the elementary charge, k_B is the Boltzmann constant, T is the absolute temperature, V is the voltage, and J is the current density. This parameter enables insights into phenomena determining the structure of the *J-V* curve. Using the same formula, yet replacing V by the implied V_{oc} measured by PCD and J by the illumination intensity, n_{local} can also be extracted from PCD measurements.[41] Fig. 5 summarizes the n_{local} data of the devices presented before, which were extracted from PCD (directly after PECVD) and dark *J-V* (on finished devices) measurements.

In the PCD measurements on cell precursors (a-Si:H layers only, i.e., no TCO, no metallization)—which are not subject to R_s effects—the n_{local} data follow approximately the same trend as the combined Auger and radiative limit (see dashed line in Fig. 5). These measurements only consider effects within the silicon wafer and not across the interfaces. From these data, we conclude that from a passivation perspective our devices are not yet limited by these two intrinsic bulk recombination pathways (as would be desirable for high-efficiency devices)[2] but likely by recombination via defect states at the wafer surfaces. This is true for all three types of devices.

For the data extracted from dark *J-V* measurements (Fig. 5), the picture changes quite drastically. This is mainly because this measurement method *does* take carrier transport across the device interfaces into account highlighting R_s-related effects. In order to evidence the R_s effect, we compare n_{local} data with and without R_s contribution. To remove the R_s-related contribution, we simply recalculated the *J-V* curve using the parameters J_{01}, J_{02}, and R_{sh} obtained from the double diode fit, setting $R_s = 0$. Furthermore, removing the R_s contribution from the data yields essentially the same trends in n_{local} for all the three devices in the voltage range >0.4 V and only minor differences are observed (<0.4 V). This corroborates our previous conclusion that, indeed, an increase in R_s associated with the a-SiO$_x$:H(*i*) layer on the hole-collecting side represents the key issue here.

C. Minority-carrier lifetime analysis

Finally, we turn to the assessment of the passivation and τ_{eff} of symmetrically passivated *c*-Si wafers (*i/i* or *I/I*), using temperature-dependent PCD measurements. The results for these samples are shown in Figs. 6(a) and 6(b). At 30 °C, both samples show comparable lifetime values in excess of

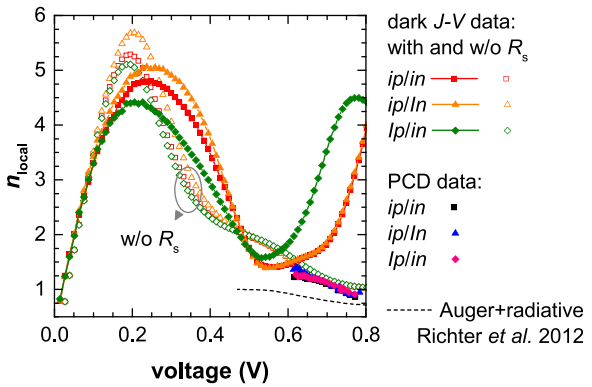

FIG. 5. Local ideality factor extracted from PCD and dark *J-V* measurements (with and without the R_s contribution) compared to the Auger and radiative lifetime limit.[45] Note that due to strong noise observed in the data sets, the curves have been smoothed, averaging over up to 20 adjacent points. The datasets from lifetime data are made up of two separate measurements (low and high injection).

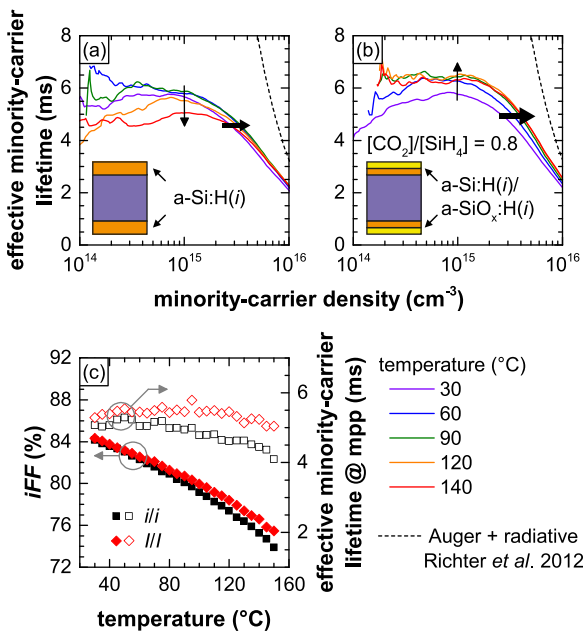

FIG. 6. Effective minority-carrier lifetime data of symmetrically passivated samples (a) a-Si:H(*i*)/a-Si:H(*i*) and (b) a-SiO$_x$:H(*i*)/a-SiO$_x$:H(*i*) (*i/i* and *I/I*). The dashed lines indicates the Auger and radiative lifetime limit,[33] the arrows the direction of the temperature evolution. Note that due to strong noise at lower minority-carrier densities, the data have been smoothed averaging over 20 adjacent points. (c) Implied *FF* data and effective minority-carrier lifetime at the implied maximum power point (mpp).

5 ms at minority-carrier densities (Δn) of $1 \times 10^{15}\,\mathrm{cm}^{-3}$. After a slight increase in lifetime, the *i*/*i* sample shows an overall decreasing trend with increasing temperature, especially for $\Delta n < 1 \times 10^{15}\,\mathrm{cm}^{-3}$ [Fig. 6(a)]. Even though the trend is less pronounced compared to what we reported earlier, it confirms our previous findings, where we observed a strongly decreasing trend in τ_{eff} for the entire Δn range.[42] As τ_{eff} at lower Δn values is mainly influenced by field-effect passivation, or the lack thereof,[43,44] we tentatively explained this observation by a lack of a sufficiently strong field-effect passivation in *i*/*i*-passivated samples at elevated temperatures. In contrast to this behavior, we see the opposite trend for the *I*/*I* sample, which shows a stabilization of the lifetime at temperatures above 60 °C followed by a slight decrease beyond 120 °C [Fig. 6(b)]. We observed a similar behavior for stacks of intrinsic and doped a-Si:H layers,[42] which may in fact indicate the presence of oxide-induced *n*-type doping as reported for a-SiO_x:H layers.[17–20,45]

From these lifetime data, we extract the so-called implied *FF* (*iFF*) and the lifetime at the implied maximum power point (τ_{mpp}) as shown in Fig. 6(c). These data reveal a subtle but striking difference. While for the *I*/*I* sample, τ_{mpp} does not show a pronounced temperature dependence, and it decreases for the *i*/*i* starting at around 80 °C. As a result, the rate at which Δn at the implied mpp (Δn_{mpp}) increases with temperature is different for both samples (data not shown). The *I*/*I* sample exhibits a steeper increase than the *i*/*i* sample as indicated by the horizontal arrows of different sizes in Figs. 6(a) and 6(b). For the *I*/*I* sample, this results in a more favorable temperature coefficient for the *iFF*, i.e., higher *iFF* values at elevated temperatures compared to the *i*/*i* sample.

These findings point to the fact that the high-temperature performance of a device may be, indeed, influenced not only by transport-related effects but also by the passivation provided by the materials applied on the surface.

IV. CONCLUSION

We have seen that wider bandgap a-SiO_x:H(*i*) passivation layers in silicon heterojunction solar cells can lead to severe collection problems when applied to the hole-selective contact. This is most probably related to the valence band offsets, which induce a significant contribution to the R_s. This interpretation is supported by the fact that applying the same layers to the electron-collecting contact does not yield any significant increase in R_s.

Furthermore, we show that for *all* our samples the R_s values diminish with increasing temperature. This effect is, however, much more pronounced for the samples with a-SiO_x:H(*i*) layers on the hole-collecting side. Therefore, we argue that collecting holes at the rear of the device is the ideal configuration. Nevertheless, this shows that also in our reference devices, a temperature-related effect on the R_s is present. This can be associated with a noticeable yet surmountable barrier for holes.

Finally, as we reported recently, the performance at elevated temperatures is affected not only by transport-related effects but also by passivation.[42] In the present work, we have shown that the wider-bandgap oxides used here may help maintaining higher passivation for the entire temperature range tested here (30–150 °C) and therefore potentially enable higher-performance devices.

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[46]This illustration is based on device simulations performed with AFORS-HET.[24–26] Here, we assumed that the introduction of oxygen into the a-Si:H(*i*) matrix merely opens the bandgap and the other material parameters did not change.
[47]Quantitatively there is a discrepancy between the R_s obtained from light and dark *J-V* at temperatures $<55\,^{\circ}C$. This is linked to the increasingly s-shaped *J-V* curves for the *Ip/in* samples which is not reproduced accurately by the fit with a two-diode model (see Fig. 4). Therefore, in this temperature regime the absolute R_s values obtained from the dark *J-V* may be more reliable.
[48]Note that the difference of the *in/Ip* to the *ip/in* or *in/ip* sample is slightly larger, which may be explained, in part, by the lower V_{oc} value obtained for the former. This in turn is likely due to cell-to-cell variations.