Applied Physics Letters ARTICLE scitation.org/journal/apl

Identification of bulk and interface state-induced threshold voltage instability in metal/SiN_x(insulator)/AlGaN/GaN high-electron-mobility transistors using deep-level transient spectroscopy

Cite as: Appl. Phys. Lett. **119**, 233502 (2021); doi: 10.1063/5.0078367
Submitted: 12 November 2021 · Accepted: 22 November 2021 ·
Published Online: 9 December 2021

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Note: This paper is part of the APL Special Collection on Wide- and Ultrawide-Bandgap Electronic Semiconductor Devices.
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ABSTRACT

The physical mechanism of threshold voltage (V_{TH}) instability in AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) was identified via capacitance-mode deep-level transient spectroscopy characterization. MIS-HEMTs with low-pressure chemical vapor deposited (LPCVD) SiN_x as the gate insulator feature two distinctive trap-emission transients. The initial transient corresponds to emission of states at the SiN_x/AlGaN interface, and the extracted density of state exhibits an exponential decay distribution. The subsequent transient is revealed due to hybrid emission of the interface and bulk states from the LPCVD-SiN_x gate insulator, which features an activation energy higher than 1.1 eV and a capture cross section that ranges between 1×10^{-11} and 1×10^{-10} cm^2. The bulk states in the LPCVD-SiN_x gate insulator become charged under high gate voltage overdrive, leading to severe V_{TH} instability in GaN-based MIS-HEMTs.

Gallium nitride-based power-switching transistors with insulated gates, e.g., metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs), are highly preferred over their Schottky-gate counterparts because of their suppressed gate leakage, enlarged gate swing, and better tolerance to voltage overshoot during switching.[1,2] Nitride-based dielectric SiN_x has emerged as a promising gate insulator for GaN-based MIS-HEMTs because of its high breakdown electric field (approximately 13 MV/cm) and long time-dependent gate dielectric breakdown (TDDB) lifetime.[3–10] However, the introduction of the gate insulator produces interface and bulk states, and their dynamic trapping and de-trapping result in severe threshold (V_{TH}) instability.[11,12]

Most existing investigations of the causes of V_{TH} instability have focused on the interface states between the gate insulator and the (Al)GaN layer,[13–15] but little attention has been paid to the bulk states in the dielectric itself.[16,17] To address the bulk states in SiN_x, several studies have been conducted based on silicon semiconductor platforms. Powell revealed that deep gap states are generally present in amorphous silicon nitride grown via chemical vapor deposition (CVD).[18] Krick *et al.* studied the nature of deep-level defects in amorphous SiN_x and found that the density of gap states in amorphous SiN_x films is closely related to the defects that originate from silicon dangling bonds.[19] Robertson and Powell calculated the energy levels of possible gap states in amorphous SiN_x.[20,21] The trapping and de-trapping behaviors of these bulk states are more complex than those of the interface states, as additional tunneling processes may be required.[17] Therefore, in the SiN_x/(Al)GaN/GaN MIS heterostructure,

it is of great importance to explore physics-based characterization methods in order to investigate the properties of insulator-related bulk states as well as their interactions with the interface states.

In this work, the distributions of the bulk states in the SiN_x gate insulator and at the SiN_x/AlGaN interface in AlGaN/GaN MIS-HEMTs are distinguished via capacitance-mode deep-level transient spectroscopy (C-DLTS). Two distinctive trap-emission transients are observed in the C-DLTS temperature scan measurement. The initial transient process ($t < 100$ ms) corresponds to the emissions from the interface states, and the extracted density of state exhibits an exponential decay distribution in the gap from the bottom of the conduction band (E_C), as noted in most of the published works. The subsequent transient process (100 ms $< t <$ 1 s) is confirmed to be contributed by hybrid emission of the interface and bulk states in the gate insulator SiN_x. The activation energy ($E_C - E_T$) of the bulk states $E_{T,bulk}$ is determined to be larger than 1.1 eV. Capture and emission of the bulk states in the SiN_x gate insulator are more difficult than with the interface states. The bulk states start to be filled at higher gate biases, resulting in a rightward V_{TH} shift. However, the emission time constant is quite long. This gives rise to a large clockwise V_{TH} hysteresis during the DC sweep measurements in Fig. 1(c). While most of the interface states feature shorter emission time constants, V_{TH} will recover quickly during down sweeping. This contributes to a small amount of V_{TH} hysteresis.

The cross-sectional schematic structure of the SiN_x/AlGaN/GaN MIS-HEMTs that were fabricated is depicted in Fig. 1(a). The AlGaN/GaN heterostructure wafer used in this work was grown via metal-organic CVD on a Si(111) substrate. The AlGaN barrier consists of a ~1 nm GaN cap, a ~4 nm $Al_{0.25}Ga_{0.75}N$ layer, and a ~1 nm AlN interface enhancement layer. First, the fresh wafers were cleaned using a standard Radio Corporation of America treatment. Then, a 44 nm of SiN_x was deposited via low-pressure CVD (LPCVD) at 780 °C. The LPCVD-SiN_x passivation in the source/drain contact regions was etched away using low-power CHF_3/SF_6 plasmas in an inductively coupled plasma (ICP) system. This was followed by wet treatment of the exposed AlGaN barrier surface in dilute HCl. A Ti/Al/Ti/TiN metal stack was evaporated and annealed at 550 °C for 90 s under N_2 to form the source/drain Ohmic contact. Device isolation was achieved via multi-energy argon ion implantation. Finally, a TiN/Ti/Al/Ti/TiN gate metal stack was sputtered over the LPCVD-SiN_x layer. The fabricated MIS-HEMTs were finally annealed at 280 °C for 4 min in N_2 ambient. Figure 1(b) shows the transfer characteristics of typical MIS-HEMTs ($L_G/L_{GS}/L_{GD}$: 2.25/1.25/1.75 μm). High ON/OFF current ratios (I_{ON}/I_{OFF}) of approximately 10^{10} and low gate leakage of approximately 10^{-7} mA/mm are obtained. A small clockwise V_{TH} hysteresis (ΔV_{TH} ~0.7 V) is identified when the device is swept up to a maximum gate bias of +6 V.

Since trapping and de-trapping may occur during the double-mode DC transfer sweeps,[22] a pulsed I_D-V_{GS} test was used to achieve an accurate determination of the ΔV_{TH} (extracted from the gate bias intercept of the linear extrapolation of the drain current at the point of peak transconductance) at different gate quiescent biases ($V_{GS,Q}$) and sweeping directions, as shown in Fig. 1(c). A MIS-HEMT with a relatively large gate length ($L_G/L_{GS}/L_{GD}$: 46/2/2 μm) was used in the pulsed I-V test to maximize control of the drain current I_D through the pulsed gate bias V_{GS}. The ΔV_{TH} was obtained by comparing the difference between the up-sweeping $V_{TH,\,up}$, i.e., the fresh V_{TH}, and the down-sweeping $V_{TH,\,down}$ under different $V_{GS,\,Q}$ conditions. The ΔV_{TH} first increases slowly at $V_{GS,\,Q} < +5$ V and then grows quickly to 17.9 V when $V_{GS,\,Q}$ reaches +30 V, as shown in Fig. 1(d). Finally, it saturates to a value of 20.2 V at $V_{GS,\,Q} = +40$ V. Such an S-shaped ΔV_{TH} suggests the co-existence of different emission processes, which will be discussed later. A ΔV_{TH} of approximately 19 V is also observed in a fabricated LPCVD-SiN_x/AlGaN/GaN MIS diode that features a structure similar to that of the MIS-HEMTs, as shown in Fig. 2(a). Note that de-trapping occurs during the down sweep of the C–V curves (sweep rate: 0.75 V/s). This results in a ΔV_{TH} that is smaller than that obtained in the pulsed I_D-V_{GS} test.[22]

The C-DLTS measurement was used to detect the emission process of trapped electrons within a limited depletion width near the gate in order to determine the physical mechanism of the significant V_{TH} instability in MIS-HEMTs. The measurement was performed in a PhysTech GmbH FT1030 DLTS system equipped with a Lakeshore low-temperature stage (10–400 K). The frequency of the capacitance meter in the DLTS system was 1 MHz. The effect of gate bias on the capture behaviors of the defect states was investigated via isothermal

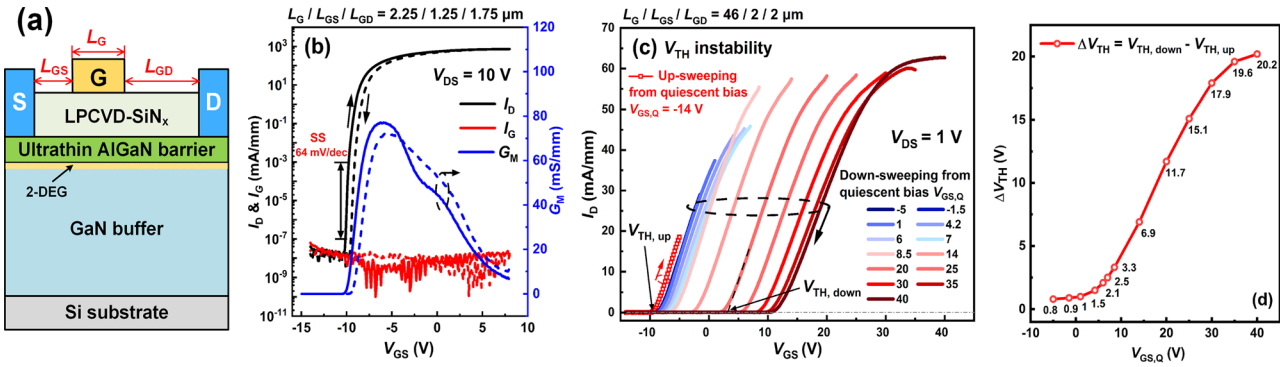

FIG. 1. (a) The cross-sectional schematic device structure of a LPCVD-SiN_x/AlGaN/GaN MIS-HEMT fabricated on ultrathin-barrier AlGaN/GaN heterostructures grown on a Si substrate. (b) DC transfer curves of typical MIS-HEMTs measured at $V_{DS} = 10$ V. The typical MIS-HEMT gate length (L_G), gate-source distance (L_{GS}), and gate-drain spacing (L_{GD}) are 2.25, 1.25, and 1.75 μm, respectively. (c) Pulsed I_D-V_{GS} transfer characteristics of the fabricated fat MIS-HEMT ($L_G/L_{GS}/L_{GD}$: 46/2/2 μm) with different quiescent bias and sweeping directions. The pulse width and period are 1 s and 5 ms, respectively. (d) Evolution of ΔV_{TH} with $V_{GS,Q}$ obtained between the up-sweeping $V_{TH,up}$ and the down-sweeping $V_{TH,down}$.

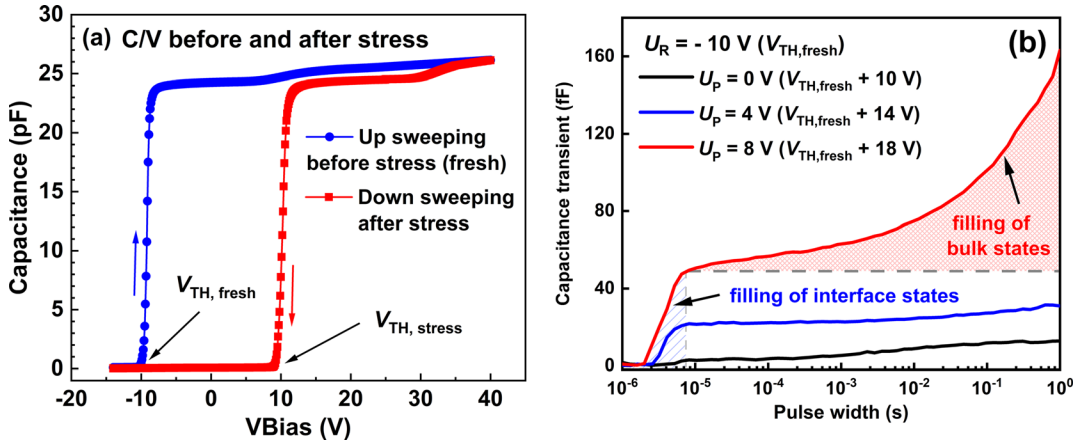

FIG. 2. (a) C–V characteristics of a fabricated LPCVD-SiN_x/AlGaN/GaN MIS diode before and after stress. (b) Evolution of a C-DLTS signal with the filling pulse t_P obtained from the isothermal capture transient ($T = 300$ K). The boundary between the interface and bulk states is marked with gray, dashed lines (for $U_P = 8$ V).

capture transient measurements performed at 300 K on a fabricated ring-shaped MIS diode ($R_G = 80\ \mu$m) with dimensions similar to those of the MIS-HEMTs.[17] Figure 2(b) shows the evolution of the C-DLTS signal with the pulse width (t_P). The pulse bias (U_P) increases from 0 V ($V_{TH} + 10$ V) to 8 V ($V_{TH} + 18$ V). The reverse measurement bias (U_R) is set to -10 V ($\sim V_{TH}$) to ensure complete release of the shallow interface states. At a U_P of 0 V, the C-DLTS signal increases slowly, indicating the slow charging of states at the LPCVD-SiN_x/AlGaN interface. When U_P increases to 4 V, the signal increases nearly exponentially at a t_P of less than 6.5 μs. When U_P is increased further to 8 V, the signal accelerates at t_P values of less than 6.5 μs. In addition, the DLTS signal continues to increase as t_P is increased further when $U_P = 8$ V. Typically, the behavior at $t_P < 6.5\ \mu$s corresponds to filling of the interface states due to its small capture time constant.[17] When $U_P = 8$ V, the behavior at $t_P > 6.5$ is likely due to filling of bulk states in the LPCVD-SiN_x gate insulator. Because interface states respond more quickly to changes in bias and pulse than bulk states, an extra tunneling process is required to fill the bulk states.

To distinguish trapping and de-trapping of possible bulk states from processes associated with interface states, the measurement bias U_R was pushed forward to the region where the 2D electron gas (2DEG) spills over to the LPCVD-SiN_x/AlGaN interface. Thus, most of the deep interface states remain charged during the C-DLTS measurements. According to the stressed C–V curves shown in Fig. 3(a), U_R is fixed at +25 V, and the filling bias increases from 30 to 40 V, then the emission transient is recorded from t_0 (12 ms) to t_1 (1.036 s) (inset figure). The filling pulse time t_p is varied between 1 and 100 ms. Figure 3(b) depicts the capacitance transients ($U_P = 35$ V and $t_P = 1$ ms) at different measuring temperatures (10–400 K). Two distinctive processes, labeled I and II in Fig. 3(b), appear as the temperature increases to 319 K. In general, the emission process of a discrete level follows an exponential time law, while that of continuous

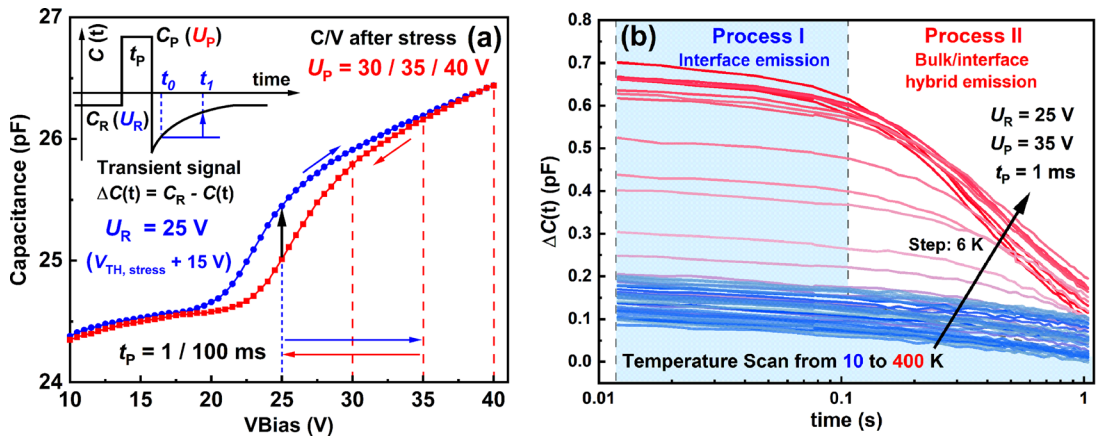

FIG. 3. (a) Measured C–V curves at 1 MHz after +40 V stresses with different sweeping directions of the fabricated LPCVD-SiN_x/AlGaN/GaN MIS diode for C-DLTS temperature-scan setup. (b) The capacitance transients $\Delta C(t)$ in C-DLTS temperature scans of the MIS diode (10–400 K). The transients composed of two emission processes (process I: interface emission and process II: bulk/interface hybrid emission) appear in the high-temperature part.

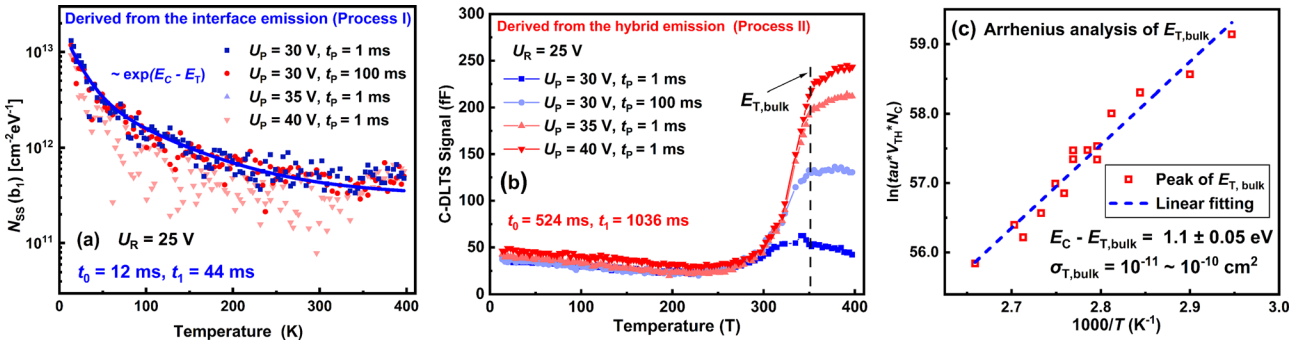

FIG. 4. (a) Distribution of interface states N_{SS} derived from the interface emission (process I) of the C-DLTS transients of the fabricated MIS diode. The distribution can be fitted effectively using an exponential function. (b) The C-DLTS temperature-scan spectra derived from the bulk/interface hybrid emissions (process II) of the transients of the fabricated LPCVD-SiN$_x$/AlGaN/GaN MIS diode at various filling pulse widths (t_P) and pulse biases (U_P). Bulk states $E_{T,bulk}$ are detected. (c) Arrhenius plot of $\ln(\tau_e \cdot V_{TH} \cdot N_C)$ for the detected $E_{T,bulk}$.

distributed states, e.g., interface states, follows a logarithmic time law that stems from the superposition of multiple exponential emissions.[23] That both processes I and II follow the logarithmic time law implies that both of them are contributed to by continuous distributed levels.

Process I is probably contributed to by the emissions of states at the LPCVD-SiN$_x$/AlGaN interface. Based on the analytical method described in Refs. 17 and 24, the extracted density of states N_{SS} from process I is obtained and shown in Fig. 4(a). The density of the interface states N_{SS} is proportional to the temperature and C-DLTS signal, for example, b_1, divided by a correction factor b_1',[23,24]

$$N_{SS}(b_1) = \frac{\varepsilon A N_S C_{ox}}{kTC_R{}^3}\frac{b_1}{b_1'}, \tag{1}$$

where C_{ox} is the oxide capacitance of the MIS capacitor, N_S is the shallow donor concentration, C_R is the capacitance at reverse bias in equilibrium, and A is the area. The correction factor b_1' considers the durations and classifications of the C-DLTS signal b_1. It can be determined numerically via integration followed by searching for the expected (mean) value in the b_1 vs T_W curve. The medium energy for N_{SS} at one temperature can be determined from the expected (mean) value of the emission time constant τ_e, which is referred to as $\langle \tau_e \rangle$ and calculated from the b_1 vs T_W curve. The related energy depth is

$$E_C - E_T = kT\ln\left(\nu_{th,n} N_C \sigma_n \langle \tau_e \rangle\right). \tag{2}$$

It is worth noting that the σ_n of the interface states may vary with the level depth and temperature. In this work, by assuming a fixed capture cross section $\sigma_n = 10^{-11}$ cm^2, the extracted N_{SS} decreases from 1×10^{13} cm^{-2}eV^{-1} at $T = 10$ K ($E_C - E_T = 0.026$ eV) to 4×10^{11} cm^{-2}eV^{-1} at $T = 400$ K ($E_C - E_T \sim 1.2$ eV), following an exponential decay law. It varies little with the height of U_P, as the Fermi level has already moved up to exceed the conduction-band minimum of the LPCVD-SiN$_x$/AlGaN interface at $U_P > 30$ V. In this regard, process I should be attributed primarily to the interface states. It is consistent with the N_{SS} distribution described in Ref. 25.

The C-DLTS signal from process II is analyzed and plotted in Fig. 4(b). It should be noted that the N_{SS} extracted from the signal at $T < 300$ K is consistent with the distribution shown in Fig. 4(a). The DLTS signal rises sharply at temperatures higher than 300 K, and a rising edge appears near 350 K. Arrhenius analysis of the rising edge indicates that it corresponds to an activation energy ($E_C - E_T$) of 1.1 ± 0.05 eV. Its capture cross section ranges between 1×10^{-11} and 1×10^{-10} cm^2. Such deep levels are more likely to be present in the LPCVD-SiN$_x$ gate insulator[26] than in the interface given the higher U_P used. The activation energy is similar to the gap states that originates from the silicon dangling bond ($\equiv Si^-$) in LPCVD-SiN$_x$.[19] Therefore,

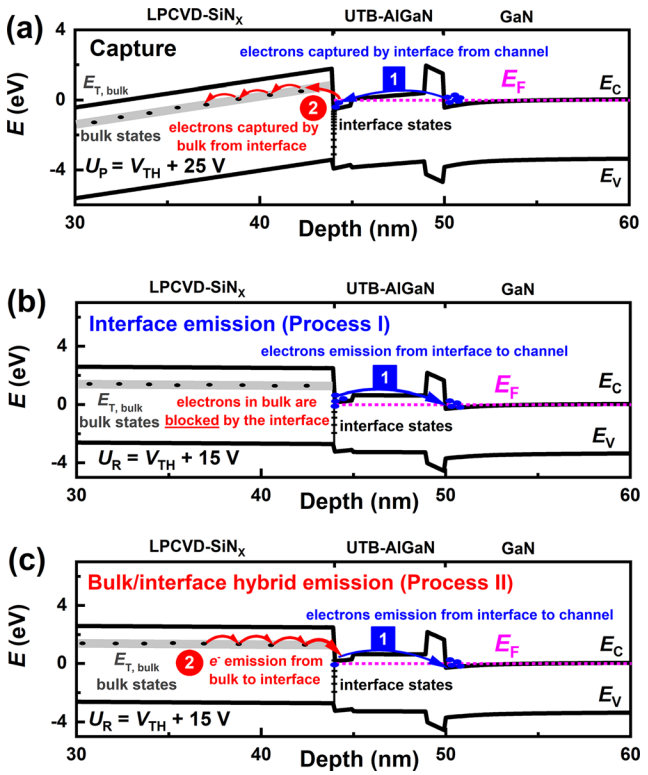

FIG. 5. Schematic energy band diagram across the gate stack at (a) capture, (b) interface emission, and (c) bulk/interface hybrid emission. The simulated energy band does not consider any bulk or interface states, and the bulk states $E_{T,bulk}$ in the LPCVD-SiN$_x$ gate dielectric are marked out.

process II represents hybrid emission of the continuous states at the LPCVD-SiN_x/AlGaN interface and the bulk states in the LPCVD-SiN_x itself.

To provide clarity, the energy bands of the LPCVD-SiN_x/AlGaN/GaN MIS structure under different gate biases, i.e., U_R and U_P, were calculated using the one-dimensional Poisson equation to illustrate the two transient processes, as shown in Fig. 5.[27] Both the interface and bulk states can be filled by electrons via thermal emission or possible tunneling-hopping processes when U_P is pulsed [Fig. 5(a)]. Increasing numbers of inner bulk states become trapped at higher U_P values. When the gate bias is relaxed to U_R, the electrons trapped at the LPCVD-SiN_x/AlGaN interface first emit back to the 2DEG channel [process I, Fig. 5(b)]. Emission from the bulk states in LPCVD-SiN_x is difficult because of the high energy of the negatively charged interface. The blocking effect of the interface states weakens with the release of interface states [Fig. 5(c)]. The bulk states begin to emit, which adds up to the interface emission. The co-emission of interface and bulk states results in the second set of steeper transients in the C-DLTS results (process II).

In summary, the physical mechanism of V_{TH} instability in metal/SiN_x(insulator)/AlGaN/GaN MIS-HEMTs was investigated via C-DLTS. Two distinctive trap-emission transients were revealed. The initial transient occurs due to emission from the LPCVD-SiN_x/AlGaN interface states, while the subsequent transient represents a hybrid emission from both the interface and bulk states in the LPCVD-SiN_x. The distribution of the interface states and level information from the bulk states were identified via individual analysis of each transient. High gate biases induced charging of bulk states in the SiN_x gate insulator and would give rise to severe V_{TH} instability in GaN-based MIS-HEMTs.

This work was supported in part by the National Natural Science Foundation of China under Grant Nos. 61822407, 62074161, 61527816, 11634002, 61631021, 62004213, and U20A20208; in part by the Key Research Program of Frontier Sciences, Chinese Academy of Sciences (CAS) under Grant No. QYZDB-SSW-JSC012; in part by the National Key Research and Development Program of China under Grant No. 2018YFE0125700; in part by the Youth Innovation Promotion Association of CAS; in part by the University of Chinese Academy of Sciences; and in part by the Opening Project of Key Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, CAS.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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