A self-consistent technique for the analysis of the temperature dependence of current–voltage and capacitance–voltage characteristics of a tunnel metal-insulator-semiconductor structure

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A new formalism is reported for the analysis of the current–voltage ($I-V$) characteristics of a tunnel metal-insulator-semiconductor (MIS) device, which considers a bias dependent distribution of interface states and barrier lowering due to the image force. Our theoretical expression for the $I-V$ characteristics is general in the sense that it is applicable even under conditions when both the thermionic emission and the diffusion mechanisms of current transport compete with each other. The method is ideal for new epitaxial materials and devices where the carrier density is not known precisely beforehand. A self-consistent method of analysis is reported to determine the characteristic parameters of MIS diodes, using simultaneously the $I-V$ and capacitance–voltage data as a function of temperature. This computational analysis has been used to examine the current transport mechanism in an Au/p-InP epitaxial MIS diode. The experimental verification of the theory and computational analysis is done by comparing the values of the interface state density distribution in thermal equilibrium with the semiconductor N_{ss}, obtained from the forward $I-V$ characteristics, with those directly measured by the multifrequency admittance method. Excellent agreement from these comparisons strongly supports the validity of the theory. Over the temperature range of 200–393 K, our results indicate that the interfacial layer-thermionic emission was clearly the dominant mechanism of the forward current transport in an MIS fabricated on a lightly doped InP:Zn epitaxial layer. The transmission coefficient through the insulator layer obtained from the reverse $I-V$ characteristics was $\theta_p = 1.43\times10^{-3}\pm7\%$ from which we estimate an oxide thickness of 2.2 nm. The analysis of the barrier height ϕ_{b0} versus temperature, obtained from 1 MHz $C-V$ data provided a value $\phi_0 = 1.06$ V$\pm10\%$ for the zero bias and zero temperature barrier height. [S0021-8979(97)07922-X]

I. INTRODUCTION

The excellent properties of InP based ternary and quaternary compounds for the fabrication of novel electronic and optoelectronic devices make InP a superior strategic material for microwave and photonic applications. The electronic and optoelectronic properties of these devices depend on the quality of InP epitaxial layers, and it is thus important to be able to characterize this material.

The metal-insulator-semiconductor (MIS) diode is an important research tool in the characterization of new semiconductor materials and at the same time the fabrication of this structure plays a crucial role in constructing some InP devices. The MIS diode is used to determine bulk and surface parameters of semiconductors[1] and for this reason the physics and fabrication of this device have been discussed in many articles[1–9] and much effort has been dedicated to the characterization of MIS contacts.[1,10–13] Frequently, however, the characterization assumes a constant interface state density distribution,[8,9,13] neglecting the experimental evidence showing a voltage dependent distribution of interface states.[1,10–12] On the other hand, few articles have analyzed the $I-V/T$ characteristics simultaneously with the $C-V/T$ data to determine the characteristic parameters of the MIS diodes.

This article develops a new formalism to analyze the $I-V$ characteristics in an MIS diode. This formalism considers the effect of a voltage dependent distribution of interface states and of the barrier lowering due to the image force on the majority carrier current. Our expression for the $I-V$ characteristics of an MIS diode is general in the sense that it is applicable even under conditions when both the thermionic emission and the diffusion mechanisms of current transport compete with each other. In our treatment, the position of the quasi Fermi level of the holes at the insulator/semiconductor interface is easy to calculate for the interfacial layer-thermionic emission (ITE) or the interfacial layer diffusion (ID) or when a combination of both mechanisms is present. This is important since the position of the quasi Fermi level is essential to determine the energy density distribution of the interface states.

In this work, we also report on a new method of analysis, which uses simultaneously the $I-V/T$ and $C-V/T$ data to determine the characteristic parameters of MIS diodes. This computational analysis has been used to examine the

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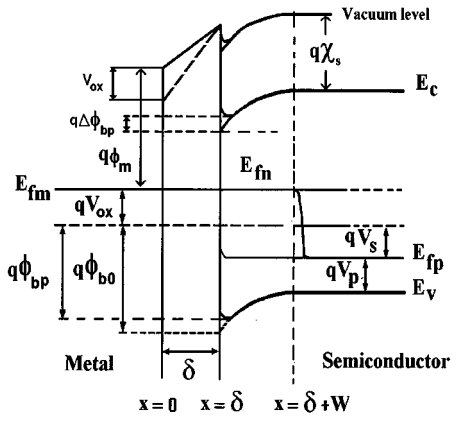

FIG. 1. Energy-band diagram of a metal/p-type semiconductor Schottky barrier diode with a thin interfacial layer.

transport mechanisms in a mesa etched Au/p-InP epitaxial MIS diode and to determine, among others, the value of the transmission coefficient through the insulating layer for the Au/p-InP, which is not well defined in the literature.

The article is organized as follows. Section II presents the interfacial layer model, which establishes the theoretical framework of our approach. Section III briefly describes the experimental method, Sec. IV presents the results and data analysis which are then discussed in Sec. V. We summarize our conclusions in Sec. VI.

II. INTERFACIAL LAYER MODEL

A. *I–V* characteristics of metal-insulator-semiconductor (MIS) diodes

The energy-band diagram for a forward bias V applied to an MIS contact fabricated on a p-type semiconductor substrate is shown in Fig. 1, where δ is the insulator layer thickness, χ_s is the electron affinity of the semiconductor, and ϕ_m is the work function of the metal. $\Delta\phi_{\rm bp}$ is the image force lowering and is given by

$$\Delta\phi_{\rm bp}=[q^3N_A(\phi_{b0}-V_s-V_p)/8\pi^2\epsilon_s^3]^{1/4}, \tag{1}$$

where N_A is the shallow acceptor concentration, ϕ_{b0} is the barrier height at zero bias, and ϵ_s is the semiconductor permittivity. In Eq. (1), qV_p is the energy difference between the majority carrier Fermi level ($E_{\rm fp}$) and the top of the valence band edge in the bulk.[14] V_s is the applied voltage drop across the surface depletion layer of the semiconductor and is related to the applied voltage through the equation

$$V_s=V-V_{\rm ox}, \tag{2}$$

where $V_{\rm ox}$ is the applied voltage drop across the interfacial layer and is measured with respect to its value at zero bias.

If the minority-carrier diffusion current in the neutral region of the semiconductor and the net recombination-generation rate for holes in the space-charge region are negligible, the total dark current is given by

$$I=-I_p(\delta+W)=-I_p(\delta+x_{\rm min}), \tag{3}$$

where I is taken as a positive quantity. The minus sign on the right side of Eq. (3) arises since the majority-carrier current at the interface, $I_p(\delta+x_{\rm min})$, is considered negative when the holes move to the left of the interface (Fig. 1). $x_{\rm min}$ is the location of the band minimum due to image force lowering and is given in Ref. 14, and W is the thickness of the space-charge layer defined by the relation

$$W=[2\epsilon_s(V_{b0}-V_s-kT/q)/qN_A]^{1/2} \tag{4}$$

$$V_{b0}=\phi_{b0}-V_p. \tag{5}$$

When the current transport at the interface is controlled by thermionic emission and is assisted by tunneling through the interfacial layer, I is expressed as

$$\begin{aligned} I&=I_{S\to M}(\delta+x_{\rm min})-I_{M\to S}(\delta+x_{\rm min})\\ &=I_{\rm th}\{\exp(qV/kT)\exp[-E_{\rm fp}(\delta+x_{\rm min})/kT]-1\} \end{aligned} \tag{6}$$

with

$$I_{\rm th}=AA^*T^2\theta_p\,\exp[-q(\phi_{\rm bp}+V_{\rm ox})/kT], \tag{7}$$

where $I_{S\to M}$ is the electrical current due to holes moving from the semiconductor into the metal, $I_{M\to S}$ is the electrical current from the metal to the semiconductor, θ_p is the transmission coefficient of holes across the interfacial layer at the energy of the potential minimum, A the area of the rectifying contact, A^* the effective Richardson constant ($A^*=60$ A K^{-2} cm^{-2} for p-InP), and $\phi_{\rm bp}$ is the barrier height at the forward bias V, given by

$$q\phi_{\rm bp}=q\phi_{b0}-q\Delta\phi_{\rm bp}. \tag{8}$$

In the space-charge layer, at a distance x from the interface, both drift and diffusion may contribute to the hole current $I_p(x)$ given by

$$I_p(x)=qAp(x)\mu_p\xi(x)-qAD_p dp(x)/dx \tag{9}$$

$$p(x)=p_b\,\exp\{-[E_{\rm fp}(x)+q\psi(x)]/kT\}, \tag{10}$$

where ψ is the electrostatic potential, $\xi=-d\psi/dx$ is the electric field, p the hole density, $E_{\rm fp}$ the hole quasi Fermi level, μ_p is the hole mobility, and $p_b(=N_A)$ is the hole density in the bulk of the semiconductor. $\psi(x)$ and $E_{\rm fp}(x)$ are measured with respect to their values in the bulk of the p-type semiconductor.

If $I_p(x)$ is a slowly varying function of x, substituting Eq. (10) into Eq. (9) and integrating over the depletion layer, the following relation is obtained

$$\exp[-E_{\rm fp}(\delta+x_{\rm min})/kT]=1+I_p(\delta+x_{\rm min})/I_D, \tag{11}$$

where I_D is the diffusion current and is given by

$$I_D^{-1}=\int_{\delta+x_{\rm min}}^{\delta+W}\frac{\exp[q\psi(x)/kT]dx}{A\mu_p p_b kT}. \tag{12}$$

Substituting Eq. (11) into Eq. (6), the electric current can be written as

$$I=I_{\rm th}F_p[\exp(qV/kT)-1] \tag{13}$$

with

$$F_p=I_D/[I_D+I_{\rm th}\exp(qV/kT)]. \tag{14}$$

When $I_D \gg I_{\rm th}\exp(qV/kT)$, the transport factor is equal to 1 ($F_p=1$) and Eq. (13) simplifies to the interfacial layer-thermionic emission (ITE) current expression, which was first derived by Wu[6]

$$I_{\rm ITE}=AA^*T^2\theta_p \exp[-q(\phi_{\rm bp}+V_{\rm ox})/kT] \times[\exp(qV/kT)-1]. \tag{15}$$

Moreover, Eq. (11) reduces to

$$\exp[-E_{\rm fp}(\delta+x_{\rm min})/kT]=1. \tag{16}$$

This equation suggests that the hole quasi Fermi level is flat throughout the space-charge region, $E_{\rm fp}(\delta+x_{\rm min})=E_{\rm fp}(\delta+W)$.

However, for $I_D \ll I_{\rm th}\exp(qV/kT)$, the transport factor can be expressed as

$$F_p=I_D/[I_{\rm th}\exp(qV/kT)]\ll 1 \tag{17}$$

and when $qV/kT \gg 1$, using Eq. (11), Eq. (13) reduces to the interfacial layer-diffusion (ID) current formula of Wu[6]

$$I_{\rm ID}=AqN_VV_D \exp[-q(\phi_{\rm bp}+V_{\rm ox})/kT]\exp(qV/kT), \tag{18}$$

where V_D is an effective diffusion velocity related with the transport of holes from the edge of the depletion layer ($x=\delta+W$) to the potential minimum ($x=\delta+x_{\rm min}$), which is defined by

$$V_D^{-1}=q\int_{\delta+x_{\rm min}}^{\delta+W}\frac{\exp\{q[\phi_{\rm bp}-V-V_p-\psi(x)]/kT\}dx}{A\mu_p p_b kT}. \tag{19}$$

Using Eqs. (3), (13), and (17), Eq. (11) simplifies to

$$E_{\rm fp}(\delta+x_{\rm min})=qV. \tag{20}$$

It can be seen from Fig. 1 that $E_{\rm fm}$ at the metal/insulator interface is up from the position of $E_{\rm fp}$ at the bulk of the semiconductor by an energy of qV. Therefore, Eq. (20) suggests that the hole quasi Fermi level at the band minimum coincides with the metal Fermi level.

It is important to point out that our formalism for the I–V characteristic in an MIS diode differs from that of Wu[6] in two aspects: first, the pre-exponential factor in our Eq. (13) is different from his Eq. (12); and second, in our treatment, the position of the hole quasi Fermi level at the insulator/semiconductor interface (which is essential to determine the energy density distribution of the interface states) is easy to calculate for the ITE or ID or when a combination of both mechanisms is present.

B. Capacitance of an MIS diode

For an MIS structure without interface states, the capacitance of the interface layer ($C_{\rm ox}$) is in series with the space-charge capacitance ($C_{\rm sc}$) and the equivalent circuit of the MIS structure is represented by Fig. 2(a). For this structure, the junction capacitance can be expressed as

$$C^{-1}=C_{\rm ox}^{-1}+C_{\rm sc}^{-1}, \tag{21}$$

where $C_{\rm ox}=A\epsilon_{\rm ox}/\delta$, $C_{\rm sc}=A\epsilon_{\rm s}/W$ and $\epsilon_{\rm ox}$ is the insulator permittivity. However, for an MIS structure with interface states, the equivalent circuit is complex because it depends on the occupancy function of the interface states (f_{t0}). The function f_{t0} is defined by the relation[2]

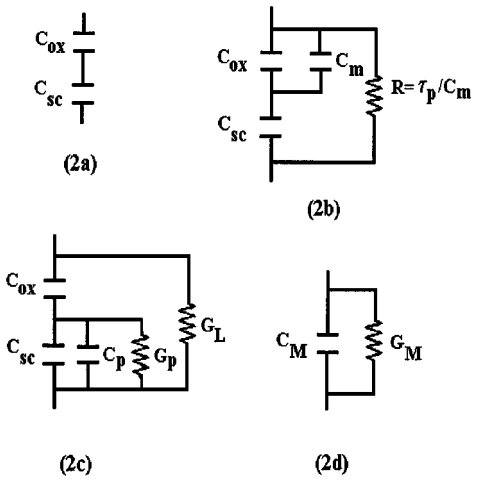

FIG. 2. Equivalent circuits for an MIS structure: (a) without interface states, (b) with a single trap level in thermal equilibrium with the metal, (c) with a continuous distribution of interface states in thermal equilibrium with the semiconductor, and (d) as determined by a lock-in amplifier.

$$f_{t0}=[\tau_{T0}f_{t00}+\tau_p f_{m0}]/[\tau_{T0}+\tau_p] \tag{22}$$

with

$$f_{t00}=[n_{s0}S_{n0}+p_1S_{p0}]/[(n_{s0}+n_1)S_{n0}+(p_{s0}+p_1)S_{p0}] \tag{23}$$

$$f_{m0}=\{1+\exp[(E-E'_{\rm fm})/kT]\}^{-1}, \tag{24}$$

where n_{s0} and p_{s0} are the electron and hole densities at the semiconductor surface. The quantities n_1 and p_1 are the electron and hole density at the interface if the Fermi level were at the energy of the interface states (E), and are given in Ref. 2. $E'_{\rm fm}$ is the Fermi level in the metal. Both E and $E'_{\rm fm}$ are measured from the top of the valence band at the semiconductor surface

$$E'_{\rm fm}=q\phi_{\rm bp}+qV_{\rm ox}. \tag{25}$$

In Eq. (23), $S_{n0}=N_{\rm ss}\langle\sigma_n\nu_{\rm thn}\rangle$, and $S_{p0}=N_{\rm ss}\langle\sigma_p\nu_{\rm thp}\rangle$, are the surface recombination velocities for electrons and holes where σ_n and σ_p are the capture cross section of traps for electrons and holes at the interface. $\nu_{\rm thn}$ and $\nu_{\rm thp}$ are the thermal velocity of electrons and holes, respectively, τ_{T0} is the tunneling time constant, and τ_p the surface recombination time constant is given by

$$\tau_p=[\langle\sigma_n\nu_{\rm thn}\rangle(n_{s0}+n_1)+\langle\sigma_p\nu_{\rm thp}\rangle(p_{s0}+p_1)]^{-1}. \tag{26}$$

The dc occupancy f_{t0}, Eq. (22), is a linear combination of the equilibrium occupancies of the metal f_{m0}, and of the semiconductor f_{t00}. One of these two occupancies will determine the value of f_{t0} depending on the semiconductor and metal properties. It is clearly seen that there are two limiting cases of special interest that deserve further discussion.

1. Interface states in thermal equilibrium with the metal

If the surface recombination time constant is large compared to the tunneling time constant, $\tau_p \gg \tau_{T0}$, then Eq. (22) simplifies to

$$f_{t0} = f_{m0} = \{1 + \exp[(E - E'_{\rm fm})/kT]\}^{-1}. \tag{27}$$

The occupancies of interface states f_{t0} and of metal states f_{m0} approach the same value. This is the case of interface states in thermal equilibrium with the metal and the equivalent circuit for the MIS structure as shown in Fig. 2(b).[2] In this figure, it is assumed that the applied ac voltage (V_1) develops a voltage V_{s1} at the interface of the semiconductor, and C_m is the surface state capacitance in thermal equilibrium with the metal, which, in the case of a single trap level, is given by[2]

$$C_m = q^2 A N_t f_{m0}(1 - f_{m0})/kT, \tag{28}$$

where N_t is the surface density of traps. Referring to Fig. 2(b), if the value of $C_{\rm ox}$ is large (i.e., $C_{\rm ox} \gg C_m$) then the total capacitance is independent of the frequency of the ac signal even when the density of the interface states is not negligible.

If the tunnelling time constant through the barrier is large compared to the surface recombination time constant, $\tau_{T0} \gg \tau_p$, then Eq. (22) simplifies to $f_{t0} = f_{t00}$. The occupancy f_{t0} approaches the value f_{t00},

$$f_{t0} = f_{t00} = [n_{s0} S_{n0} + p_1 S_{p0}]/[(n_{s0} + n_1) S_{n0} + (p_{s0} + p_1) S_{p0}]. \tag{29}$$

Assuming a p-type semiconductor with a heavily inverted surface, $p_1 \ll n_{s0}$ and $p_{s0} \ll n_1$ (reverse bias and large diffusion potential at zero bias), Eq. (29) can be written as

$$f_{t0} = f_{t00} = n_{s0}/(n_{s0} + n_1) = \{1 + \exp[(E - E'_{\rm fn})/kT]\}^{-1}, \tag{30}$$

where $E'_{\rm fn}$ is the quasi Fermi level for electrons measured from the edge of the valence band at the interface.

In the MIS configuration, there is no difficulty in the communication between the conduction band of the semiconductor and the metal. Any ultrathin interfacial or intermediary layer present is considered completely transparent to electrons. Thus the electron population at the interface must follow the metal carrier population, i.e., the quasi Fermi level for electrons $E'_{\rm fn}$ at the interface must be the same as the Fermi level in the metal $E'_{\rm fm}$. Then, Eq. (30) can be reduced to Eq. (27) and the interface states are in thermal equilibrium with the metal.

2. Interface states in thermal equilibrium with the semiconductor

For a p-type semiconductor with a noninverted surface, $p_1 \gg n_{s0}$ and $p_{s0} \gg n_1$ (forward bias), Eq. (29) can be written as

$$f_{t0} = f_{t00} = p_1/(p_{s0} + p_1) = \{1 + \exp[(E - E'_{\rm fp})/kT]\}^{-1}, \tag{31}$$

where $E'_{\rm fp}$ is the quasi Fermi level for holes measured from the edge of the valence band at the interface, given by

$$E'_{\rm fp} = q\phi_{\rm bp} - qV_s + E_{\rm fp}(\delta + x_{\rm min}) = q\phi_{\rm bp} - qV_s + kT \ln[I_D/(I_D - 1)]. \tag{32}$$

This is the case of interface states in thermal equilibrium with the semiconductor and the equivalent circuit for the MIS structure is shown in Fig. 2(c).

In Fig. 2(c), C_p and G_p are the equivalent parallel capacitance and conductance of a distribution of interface states and are given by[2]

$$C_p = qAN_{\rm ss}(E = E_{\rm fp})[\tan(\omega\tau_m)/\omega\tau_m] \tag{33}$$

$$G_p/\omega = qAN_{\rm ss}(E = E_{\rm fp}) \ln[(\omega\tau_m)^2 + 1]/\omega\tau_m, \tag{34}$$

where $N_{\rm ss}$ is the interface state density measured at the energy $E_{\rm fp}$, and $\tau_m = (p_{s0}\langle\sigma_p \upsilon_{\rm thp}\rangle)^{-1}$ is the maximum recombination time. In the parallel equivalent circuit of Fig. 2(d), the capacitance (C) and the conductance (G) of MIS junction are related to the values of C_p, G_p, G_T, and $C_{\rm ox}$ by

$$G_p = \frac{G - G_T}{(1 - C/C_{\rm ax})^2 + [(G - G_T)/\omega C_{\rm ax}]^2} \tag{35}$$

$$C_p + C_{\rm sc} = \frac{C_{\rm ox} - C}{(1 - C/C_{\rm ox})^2 + [(G - G_T)/\omega C_{\rm ox}]^2} - C_{\rm ox}, \tag{36}$$

where G_T is the tunnelling conductance and is given by Eq. (6.10) in Ref. 2. Using Eq. (35), Eq. (36) can be rewritten as

$$C_p + C_{\rm sc} = \frac{C_{\rm ox}}{(1 - C/C_{\rm ox})^2\{1 + G_p^2/[\omega^2(C_{\rm ox} + C_{\rm sc} + C_p)^2]\}} - C_{\rm ox}. \tag{37}$$

If the value of $C_{\rm ox}$ is large, i.e., $\omega\,(C_{\rm ox} + C_{\rm sc} + C_p) \gg G_p$, then C_p can be expressed as

$$C_p = \frac{C_{\rm ox} C}{C_{\rm ox} - C} - C_{\rm sc}. \tag{38}$$

We note that at sufficiently high frequencies both C_p, Eq. (33), and G_p/ω, Eq. (34), tend to zero. Here we shall make the assumption that at 1 MHz, C_p and G_p/ω can be neglected in Eq. (37) and the 1 MHz junction capacitance can be expressed by Eq. (21).

C. Determination of the $N_{\rm ss}$ value from the forward I–V characteristic

In the absence of any space-charge effects in the interfacial layer, the charge that develops on the metal surface (Q_M) can be written as

$$Q_M = -(Q_{\rm ss} + Q_{\rm sc}) \tag{39}$$

and employing Gauss's law, the applied voltage drop across the interfacial layer under nonequilibrium conditions may be written as[15]

$$V_{\rm ox} = \Delta Q_M/C_{\rm ox} = -[Q_{\rm sc}(0) + Q_{\rm ss}(0) - Q_{\rm sc}(V_s) - Q_{\rm ss}(V_s)]/C_{\rm ox}, \tag{40}$$

where Q_{sc} is the space-charge density in the surface depletion layer of the semiconductor and is given by

$$Q_{sc}(V_s) = -[2q\epsilon_s N_A(V_{b0} - V_s - kT/q)]^{1/2} \tag{41}$$

and Q_{ss} is the net charge trapped in the interface states given by[16]

$$Q_{ss} = -q\int_0^{E_G} N_{ss}(E) f_{t0}(E,V_s)dE + q\int_0^{E_G} N_{ss}^d(E)dE, \tag{42}$$

where $N_{ss}(E) = N_{ss}^a(E) + N_{ss}^d(E)$ is the sum of acceptor (N_{ss}^a) and donor (N_{ss}^d) type interface state densities. In Eq. (42), the occupancy of the interface states f_{t0} is assumed equal for both types of interface states.

The dependence of f_{t0} on the applied bias can be greatly reduced if the interaction rate of the interface states with majority carriers is much smaller than that with the metal or with minority carriers whose quasi Fermi level is pinned by the metal. This is the case of interface states in thermal equilibrium with the metal, which have an occupation function (f_{t0}) given by Eq. (27). In particular, it is clearly seen from Eq. (27) that f_{t0} depends on the applied voltage via E'_{fmp} which depends of V_{ox} as is shown in Eq. (25). However, for an ultrathin interfacial layer, V_{ox} is negligible in comparation with ϕ_{bp} so that E'_{fm} can be considered constant. Therefore, the occupation function will be kept unchanged for all reverse bias when the interface states are in equilibrium with the metal. Here, the net charge residing in the interface states is also kept constant and we can neglect the terms

$$\begin{aligned}\Delta Q_{ss} &= Q_{ss}(0) - Q_{ss}(V_s) \\ &= -q\int_0^{E_G} N_{ss}(E)[f_{t0}(E,0) - f_{t0}(E,V_s)]dE\end{aligned} \tag{43}$$

in Eq. (40), which can be simplified to

$$V_{ox} = -[Q_{sc}(0) - Q_{sc}(V_s)]/C_{ox} = V - V_s. \tag{44}$$

On the other hand, when the forward bias increases, the increment of majority carriers will force the occupation function to follow E'_{fp} [Eq. (32), Sec. II B 2), which is strongly dependent on the applied voltage.

Differentiating Eq. (43) with respect to the applied voltage drop across the semiconductor V_s, we have

$$\frac{\partial(\Delta Q_{ss})}{\partial V_s} = q\int_{E_V}^{E_C} N_{ss}(E)\,\frac{\partial f_{t0}(E,V_s)}{\partial V_s}\,dE. \tag{45}$$

Note that Eq. (31) is just the Fermi–Dirac distribution function for the p-type semiconductor at the surface. Thus we can approximate the partial differential term in the integrand of Eq. (45) with a delta function, i.e.,

$$\partial f_{t0}/\partial V_s = -q\,\delta(E - E'_{fp}) \tag{46}$$

and Eq. (45) can be written as

$$-q^2\partial(\Delta Q_{ss})/\partial V_s = N_{ss}(E'_{fp}). \tag{47}$$

By varying the forward bias within the validity range of the depletion approximation, the density distribution of interface states can be calculated from Eq. (47).

III. EXPERIMENTAL METHOD

The Au/p-InP MIS diode used in this work was fabricated on a lightly doped InP:Zn epitaxial layer grown by metal-organic vapor-phase epitaxy (MOVPE) on a highly doped InP p-type substrate. The epitaxial layer was approximately 3 mm thick. The MOVPE growth was performed using a horizontal quartz cold-wall reactor with a graphite susceptor. The details of our low-pressure MOVPE system have been reported elsewhere.[17] Growth precursors were trimethylindium (TMIn), pure phosphine (PH_3), and diethylzinc (DEZn). In this MOVPE experiment, the reactor pressure was maintained at 40 Torr, the growth temperature at 600 °C, and the V/III ratio was 250.

Before metal deposition, the epitaxial layer was degreased with trichloroethylene, acetone, and propanol for 10 min at 40 °C, and then chemically etched with HF:HCl:H_2O_2:H_2O (1:1:1:4) solution for 10 min to remove the native oxide. The back contact to the highly doped InP p-type substrate was made by thermal evaporation of Au/Zn/Au at a pressure of about 1×10^{-6} Torr and annealing for 5 min at 375 °C in N_2:H_2 (88:12) gas. The MIS contact to the epitaxial layer was fabricated by electron beam evaporation of Au at a pressure of about 5×10^{-7} Torr. Mesa etched rectangular Schottky contacts with area 4.76×10^{-4} cm^2 were defined by photolithography and liftoff techniques.

The current–voltage ($I-V$) and differential capacitance–voltage ($C-V$) measurements were made in the temperature range of 200–393 K. The $I-V$ characteristics of the Au/p-InP MIS diode were performed using two 619 Keithley electrometers and a Keithley 230 programmable power supply. A Hewllett Packard 4192A LF impedance analyzer was used to make the capacitance and conductance measurements as a function of bias voltage over a wide frequency (f) range (1 kHz$<f<$1 MHz).

IV. EXPERIMENTAL DATA AND ANALYSIS

A. $I-V$ and 1 MHz $C-V$ measurements at high temperature

The forward and reverse $I-V$ characteristics of an epitaxial p-InP/Au MIS diode at different temperatures over the range of 360–393 K are shown in Figs. 3 and 4, respectively. The high frequency C_M-V characteristics measured at $T=360$ and $T=393$ K under forward and reverse bias V are plotted in Fig. 5. To determine the series resistance R_s, we have followed Lien *et al.*[18] and Cheung *et al.*,[19] from the plot of I vs $dV_G/d(\ln I)$ which was linear over a wide range of I values. The values of R_s obtained from the slope of the linear parts of the curves are listed in Table I. When the series resistance is not small, the voltage drop across the MIS junction V differs from the applied voltage V_G, and is given by

$$V = V_G - IR_s. \tag{48}$$

The $I-V$ and high frequency $C-V$ characteristics at high temperatures ($T\geqslant360$ K) were analyzed simultaneously in terms of theoretical expression (13) and of the equivalent circuits of Figs. 2(a) and 2(d). The computational analysis can be divided into three main steps. In the first step, measured reverse $I-V$ characteristics at a fixed temperature are

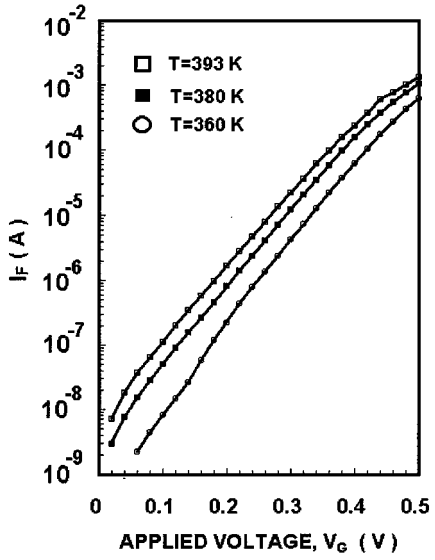

FIG. 3. Forward current–voltage characteristics of an Au/p-InP epitaxial MIS diode at high temperature. The solid curves represent theoretical fits using Eq. (13).

analyzed to determine the transmission coefficient of holes (θ_p) across the interfacial layer and the oxide capacitance ($C_{\rm ox}$). This analysis uses some initial values for the shallow acceptor concentration (N_A) and the barrier height at zero bias (ϕ_{b0}). In the second stage, these values of θ_p and $C_{\rm ox}$ are used to estimate the voltage dependence of the interface state density distribution ($N_{\rm ss}$) from the forward $I-V$ characteristics. Finally, in the third step, the values of $N_{\rm ss}$ and $C_{\rm ox}$ are used to determine the values of ϕ_{b0} and N_A from the 1 MHz $C-V$ characteristics. These values of ϕ_{b0} and N_A are

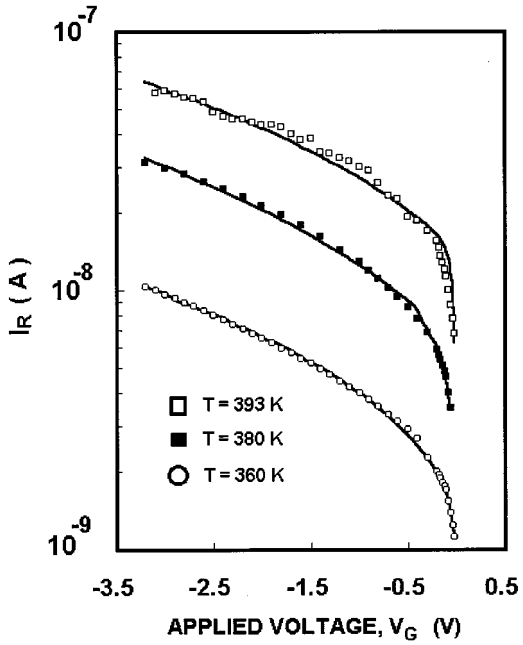

FIG. 4. Reverse current–voltage characteristics of an Au/p-InP epitaxial MIS diode at high temperature. The solid curves represent theoretical fits using Eq. (13).

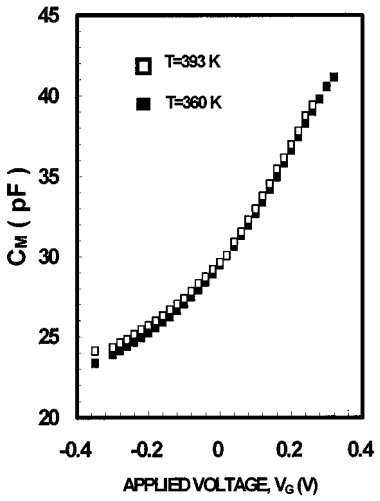

FIG. 5. High frequency capacitance–voltage characteristics measured at high temperature under forward and reverse bias.

compared with their initial values. If they are different, then the whole procedure is repeated iteratively to obtain self-consistent values of all the parameters. In our case, three iterations were enough to achieve self consistent results. The details of each computational step are given below:

Step 1: The experimental reverse I_R-V data was fitted to Eq. (13) using a nonlinear least-square curve fitting method. This fitting procedure initially provides the values of V_s and $V_{\rm ox}$ for each reverse bias by solving the nonlinear Eq. (44) using a self-consistent iterative technique and an initial value for ϕ_{b0}, N_A, and for $C_{\rm ox}$. Substituting these values of V_s and the initial values for N_A and ϕ_{b0} into Eq. (1), $\Delta\phi_{\rm bp}$ and $x_{\rm min}$ were calculated. Using these values of V_s, $\Delta\phi_{\rm bp}$, and $x_{\rm min}$, the initial value for θ_p and Eqs. (4), (5), (7), (8), (12), (13), and (14), I_R was calculated and compared to the experimental values of the reverse current. If the fit is not satisfactory, the program calculates the new values of θ_p and $C_{\rm ox}$. Using these new values, the procedure was repeated until a good fit between the theoretical and experimental values of the current is achieved.

Step 2: In the second stage, the forward bias across the junction (V_F) was obtained from the applied voltage (V_G) by making the correction for the effect of series resistance (R_s). Substituting the values of θ_p and $C_{\rm ox}$ obtained at the end of step 1, the initial value for N_A and ϕ_{b0} and a trial value for V_s, into Eqs. (1), (4), (5), (7), (8), (12), (14), and (41), $\Delta Q_{\rm sc}$ and F_p were calculated for a particular forward bias value. Using the calculated value of F_p, the correspond-

TABLE I. Best values of N_A, V_{b0}, ϕ_{b0}, θ_p, $C_{\rm ox}$, and R_s fitting parameters obtained from the current–voltage characteristics at high temperatures (360–393 K).

T (K)	N_A (10^{16} cm^{-3})	V_{b0} (V)	ϕ_{b0} (V)	θ_p (10^{-3})	$C_{\rm ox}$ (nF)	R_s (Ω)
393	2.27	0.492	0.719	2.61	1.51	44
380	2.34	0.508	0.726	2.92	1.37	33
360	2.26	0.524	0.729	2.68	1.43	33

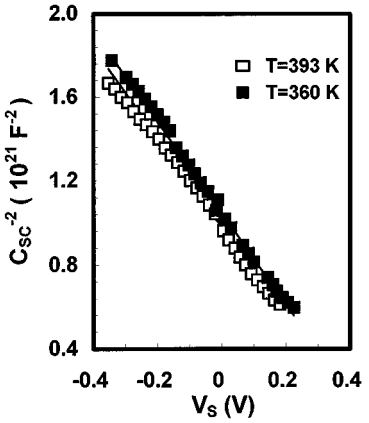

FIG. 6. $C_{sc}^{-2}-V$ characteristics obtained from C_M-V measurement (discrete points) at high temperature and the best fit (solid curves) of values of C_{sc}^{-2} to the Mott–Schottky equation.

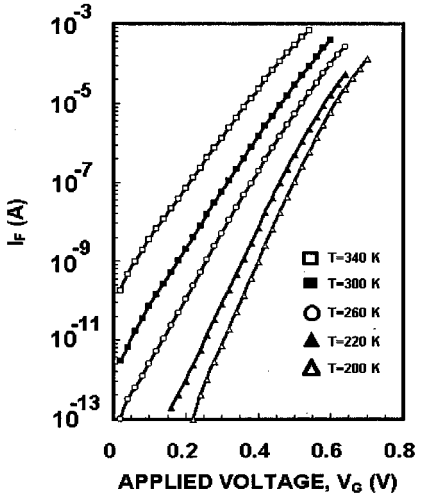

FIG. 7. Set of typical current–voltage characteristics measured at different temperature over the range of 200–340 K under forward bias. The solid curves represent theoretical fits to the data using Eq. (13).

ing measured value of I_F and Eq. (13), I_{th} was found and used in Eq. (7) to calculate the value of V_{ox}. Substituting the value of V_{ox} into Eq. (2), the value of V_s was recalculated and compared with its initial value. If the two values of V_s differ by more than 0.001%, the calculation is repeated with the last value of V_s until the convergence criterion is satisfied. To establish the bias dependence of V_s and V_{ox}, the calculation was repeated for all the forward bias values used in our experiment. Substituting the values of V_{ox}, V_s and $\Delta Q_{\text{sc}}=Q_{\text{sc}}(0)-Q_{\text{sc}}(V_s)$ into Eq. (40), the bias dependence of $\Delta Q_{\text{ss}}=Q_{\text{ss}}(0)-Q_{\text{ss}}(V_s)$ was calculated and substituted into Eq. (47) to obtain the forward bias dependence of N_{ss}.

Step 3: The high frequency capacitance (C_M) measured under both forward and reverse bias was corrected for the effect of series resistance to obtain the junction capacitance, C, using the following relation

$$C=\frac{C_M}{(1-R_sG_M)^2+(\omega R_sC_M)^2}, \tag{49}$$

where G_M is the measured conductance. The voltage dependence of C_{sc} was obtained substituting the values of C and C_{ox} into Eq. (21). $C_{\text{sc}}^{-2}-V$ characteristics were analyzed in terms of the Mott–Schottky theory[14] to calculate N_A and ϕ_{b0}. These values of ϕ_{b0} and N_A are compared with their initial values. If they are different, then the initial values of ϕ_{b0} and N_A are replaced by the one obtained from the $C_{\text{sc}}^{-2}-V_s$ data and the calculation procedure is repeated starting from step 1.

The best fits of our $I-V$ data to Eq. (13) for the temperature range of 360–393 K are shown in Figs. 3 and 4 (solid curves). The best fits of $C_{\text{sc}}^{-2}-V_s$ data for $T=360$ and $T=393$ K to the Mott–Schottky equation are shown in Fig. 6. The best values of N_A, ϕ_{b0}, θ_p, and C_{ox} provided by the above fitting procedure are listed in Table I.

B. *I–V* and 1 MHz *C–V* measurements at intermediate temperature

A set of typical forward I_F-V characteristics measured at different temperature between 200 and 340 K is shown in Fig. 7. The values of R_s obtained from I_F-V measurements are listed in Table II. The forward I_F-V and high frequency $C-V$ characteristics were analyzed simultaneously using the average values of $\theta_p(2.74\times10^{-3}\pm7\%)$ and $C_{\text{ox}}(1.44\text{ nF}\pm5\%)$ fitting parameters. This analysis also used the second and third steps of the above mentioned computational program. Figure 8 shows the $C_{\text{sc}}^{-2}-V_s$ data (discrete points) extracted by this method at $T=200$, $T=260$, and $T=340$ K and the best fit (solid curve) of the Mott–Schottky equation to the $C_{\text{sc}}^{-2}-V_s$ data. The best values of N_A, V_{b0}, and ϕ_{b0} fitting parameters obtained at different temperatures over the range of 200–340 K are listed in Table II. The temperature dependence of ϕ_{b0} and V_{b0} are shown in Fig. 9, where ϕ_{b0} values are well described by the relation

$$\phi_{b0}=(1.06-8.59\times10^{-4}\ \text{K}^{-1}\ T)\text{V}. \tag{50}$$

Finally, the energy density distribution of interface states extracted from the forward $I-V$ characteristics at room temperature is plotted in Fig. 10 (open rectangles).

C. Capacitance–frequency (*C–f*) measurements

Typical forward C_M-f characteristics measured at room temperature show a fairly large frequency dispersion in the

TABLE II. Best values of N_A, V_{b0}, ϕ_{b0}, and R_s fitting parameters obtained from the current–voltage characteristics at intermediate temperatures (200–340 K).

T (K)	N_A (10^{16} cm^{-3})	V_{b0} (V)	ϕ_{b0} (V)	R_s (Ω)
340	2.30	0.583	0.783	33
320	2.32	0.619	0.796	39
300	2.39	0.645	0.808	32
260	2.25	0.702	0.839	29
240	2.23	0.724	0.849	28
221	2.23	0.746	0.858	27
200	2.19	0.787	0.874	35

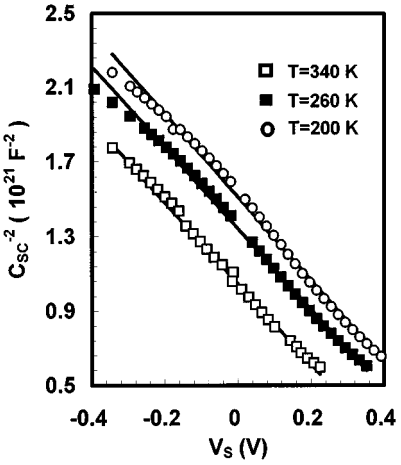

FIG. 8. Set of typical $C_{sc}^{-2}-V_s$ characteristics obtained from measurement (discrete points) at intermediate temperature and the best fit (solid curves) of the values of C_{sc}^{-2} to the Mott–Schottky equation.

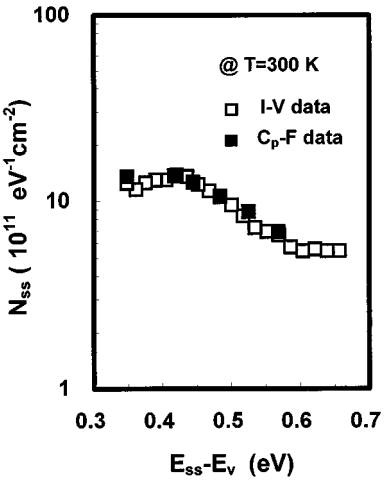

FIG. 10. Interface state density distribution obtained from the forward I_F-V and C_p-f characteristics at room temperature.

capacitance for voltages $V_F \geqslant 0.3$ V. It is assumed that this dispersion is caused by interface states in equilibrium with the semiconductor. Therefore, the junction capacitance for the forward bias values in the range of $0.3\ \text{V} \leqslant V_F \leqslant 0.58$ V was analyzed in terms of the equivalent circuit shown in Fig. 2(c). Substituting into Eq. (38) the corrected values of C_M for the effect of series resistance, the values of C_{ox} (Table I) and C_{sc} (Fig. 8), the frequency dependence of C_p at different forward bias voltage was established and is shown in Fig. 11 (discrete points). The best fits of the C_p-f experimental data to the theoretical relation (33) also are shown in Fig. 11 (solid curves). The values of $c_p=\langle \sigma_p \nu_{\text{thp}} \rangle$, and τ_m, and N_{ss} interface parameters extracted from these fits are listed in Table III and the interface state energy density distribution is shown in Fig. 10 (filled rectangles). Finally, the voltage dependence of σ_p was converted to a dependence on interface state energy, which is shown in Fig. 12. The values of σ_p were well fitted to $\sigma_p=\sigma_0 \exp[a_0(E_{\text{ss}}-E_V)]$ with $a_0=(26 \pm 9)\text{eV}^{-1}$ and $\sigma_0=(2.6\pm 0.9)\times 10^{-20}$ cm^2.

V. DISCUSSION

In the temperature range studied in this work (200–390 K), the experimental values of the majority-carrier current are well fitted by our theoretical Eq. (13) (Figs. 3 and 4, solid curves). This fact indicates that the Au/InP:Zn epitaxial diode does not obey the ideal Schottky theory. In the high temperature range, the fitting procedure provided average values of $2.74\times 10^{-3}\pm 7\%$ and $1.44\ \text{nF}\pm 5\%$ for θ_p and C_{ox}, respectively. The value of F_p under both forward and reverse bias remained close to unity within 1% over a wide temperature range of 200–360 K. This result provides sufficient evidence in favor of ITE as the dominant mechanism of current transport in an Au contact MIS, which is fabricated on a lightly doped InP:Zn epilayer.

For this Au/p-InP epitaxial MIS diode, the values of ϕ_{b0} obtained by our method at different temperatures were fitted to $\phi_{b0}=\phi_0+\beta T$ with $\phi_0=1.06\ \text{V}\pm 10\%$ and the tempera-

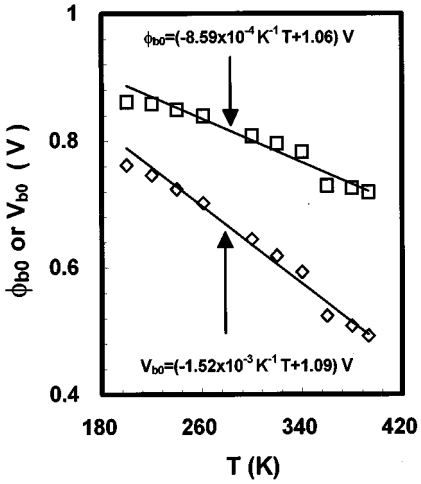

FIG. 9. Temperature dependence of ϕ_{b0} and V_{b0} for an Au/p-InP epitaxial MIS diode.

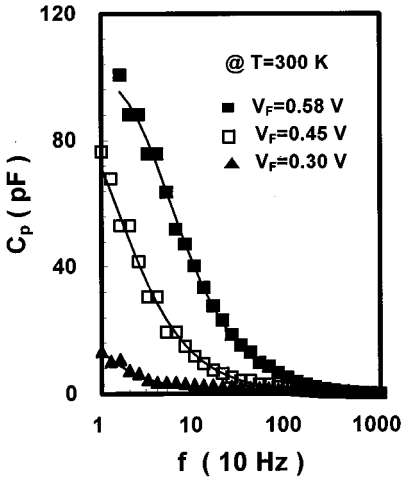

FIG. 11. Frequency dependence of C_p at different forward bias and at room temperature. The solid curve is the best fit of theoretical Eq. (33) to the C_p-f characteristics.

TABLE III. Best values of c_p, τ_m, and N_{ss} parameters obtained from C_p-F data at room temperature.

$E_{ss}-E_V$[a] (eV)	c_p (10^{-9} cm^3/s)	τ_m (10^{-5} s)	N_{ss} (10^{11} eV^{-1} cm^{-2})
0.348	341	87.0	6.89
0.417	74.9	67.5	8.23
0.444	33.7	32.6	10.7
0.484	12.7	18.4	12.7
0.525	3.33	8.66	13.7
0.569	1.08	5.25	13.6

[a]The value of $E_{ss}-E_V$ was obtained from Eq. (32).

ture coefficient of the zero-bias barrier height $\beta=-8.59\times10^{-4}$ V/K$\pm$8%. The value of ϕ_0 is not different from that obtained for a bulk p-InP/Au MIS diode.[12]

At room temperature and for $V_F\geqslant0.3$ V, the measured capacitance (C_M) clearly shows frequency dispersion which is attributed to interface states in thermal equilibrium with the semiconductor. However, for $V_F\leqslant0.2$ V, the charge in the interface states is bias independent since the measured capacitance is almost frequency independent. This latter effect may be due to (i) interface states in equilibrium with the semiconductor at sufficiently low density for these bias values or (ii) interface states in equilibrium with the metal. As the barrier height is relatively high, the terms containing the minority carrier concentration can no longer be neglected in Eq. (29). Therefore, both the majority and minority carriers at the interface determine the occupation function of the interface states. As the forward bias decreases and approaches the reverse bias, the terms containing the minority carriers contribution in Eq. (29) may dominate over the terms with majority carrier contribution. Then, the interface states will be in thermal equilibrium with the metal and as a consequence the frequency dispersion of the junction capacitance will not be observed.

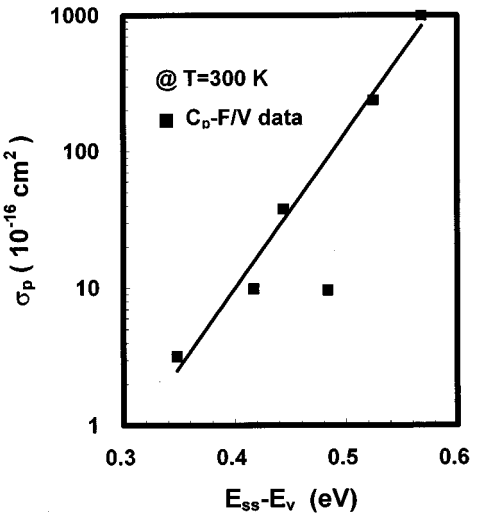

FIG. 12. Hole capture cross section of interface states as a function of energy. The solid curve is the best fit of $\sigma_p=\sigma_0\exp[a_0(E_{ss}-E_V)]$ to the data.

A careful examination of the experimental forward C_M-f/V_F data reveals that below 0.3 V, the junction capacitance starts to become independent of frequency and that for $V_F=0.2$ V, the frequency dispersion of the measured capacitance disappears. This sudden change cannot be explained on the basis of the slowly varying energy density distribution observed for $V_F\geqslant0.3$ V in Fig. 10. Therefore, we believe that below 0.3 V, the interface states are in thermal equilibrium with the metal.

In the $C-f$ data analysis, we have used Eq. (38) which requires that $\omega(C_{ox}+C_{sc}+C_p)\gg G_p$. For our experimental data, this condition is satisfied within an experimental error of 5%. The interface state density distribution derived from the experimental C_p-f data in the forward bias range of 0.3–0.58 V is a slowly varying function of the forward bias or of the interface state energy (Fig. 10). Similar results have been previously reported by Cova[1,10] and Singh.[12] The excellent agreement between the values of N_{ss} obtained from the forward $C-f/V$ (Fig. 10, filled rectangles) and I_F-V (Fig. 10, open rectangles) data provides experimental evidence in favor of our formalism for the analysis of the $I-V$ characteristic. The hole capture cross section of interface states estimated from our forward $C-f/V$ data varied over three orders of magnitude for interface energies in the range of 0.348–0.569 eV. Our results are in disagreement with those of Deuling *et al.*[20] but in agreement with those of Singh and Simmons.[21]

Finally, we would like to emphasize the importance of the interfacial layer model and the formalism which self-consistently takes into account the simultaneous analysis of $I-V/T$ and $C-V/T$ data and thus provides a reliable value of the Schottky barrier height (SBH). This method of analysis avoids the conflicting results often found in the literature where SBH values obtained from different measurement techniques ($I-V$, $C-V$, internal photoemission, etc.) are generally different. The method also allows, as an added bonus, the unequivocal determination of the transmission coefficient through the insulating layer, which can give us a measure of the diode fabrication technique. We have not found in the literature an experimental determination of this parameter with which to compare.

The transmission coefficient θ_p may be approximately expressed as

$$\theta_p=\exp[-4\pi(2m_p^*\chi)^{1/2}\delta/h], \tag{51}$$

where χ is the effective barrier height presented by the thin interfacial layer of thickness δ, which is assumed to be independent of the applied voltage.[22] Using a value of seven for the relative dielectric constant of the oxide,[23] and an average value of 1.44 nF for C_{ox} (see Table I), we estimate that δ is 2.2 nm and $\chi=1.04$ eV. Contrary to what happens in silicon surfaces, many different oxide species can coexist on InP. This is revealed by the continuous variation with the preparation procedures of the different In and P oxides surface atomic ratios.[24] In_2O_3, $In(OH)_3$, $InPO_4$, P_2O_5, as well as, hydrated compounds may exist in thin oxide layers. A correlation between surface composition evaluated with x-ray photoemission spectroscopy (XPS) and surface electrical properties has clearly established that surfaces with indium-

rich oxides give reproducible Au/InP structures, stable over several months. On the other hand, phosphorus-rich oxides result in poorly reproducible and electrically unstable contacts.[24] This result suggests that for the cleaning procedure [HF:HCl:H_2O_2:H_2O (1:1:1:4)] used to prepare the InP surface, the oxide grown unintentionally before metal deposition is In_2O_3, which was the major component detected on the InP surface prepared with HF (49%).[24] This explains therefore the good stability and reproducibility of our Au/InP contacts.

VI. SUMMARY

In summary, we have developed a new formalism for the analysis of the $I-V$ characteristics of a thin MIS diode. This treatment has been used to develop a new method for the simultaneous analysis of the $I-V$ and the $C-V$ characteristics in an epitaxial p-InP/Au MIS diode. The energy density distribution of the interface states obtained from the forward I_F-V data using this method agrees very well with that obtained directly from the $C-f/V_F$ technique, which strongly supports the validity of our model. Our value of ϕ_0 for the epitaxial p-InP/Au MIS diode is close to the one reported for bulk p-InP/Au MIS diodes.[12] Our experimental results suggest that above 0.3 V, the interface states are in equilibrium with the semiconductor and below 0.2 V, the interface states are in equilibrium with the metal. In the temperature range of 200–390 K, the forward current in an Au/p-InP MIS diode fabricated on a lightly doped InP:Zn epitaxial layer is controlled by the ITE mechanism. For this diode, the transmission coefficient across the insulating layer was $\theta_p = 2.74 \times 10^{-3} \pm 7\%$ from which we estimate a value of 2.2 nm for the insulator layer thickness and a value of 1.04 eV for the effective barrier height which is associated to native In_2O_3 oxide.

ACKNOWLEDGMENTS

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