# Industrial Czochralski n-type Silicon Wafers: Gettering Effectiveness and Possible Bulk Limiting Defects

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An assessment of the bulk material quality of industrial Czochralski (Cz) grown phosphorus-doped n-type silicon (Si) wafers along an ingot is reported. The minority charge carrier lifetimes of the Cz-Si wafer bulk before and after phosphorous (POCl₃) diffusion gettering are assessed, by applying room-temperature superacid surface passivation to avoid any additional gettering or hydrogenation effect. A substantial increase in the bulk lifetime of all of the n-type Cz-Si wafers along the ingot is observed, indicating the effectiveness of a gettering step for such wafers and the presence of getterable metallic impurities in these wafers. By experimentally monitoring the lifetime changes upon a gettering anneal and simulating the gettering kinetics based on different metal diffusivities, iron is identified to be a limiting defect, at least for the wafers from the tail part of the ingot. A dissolved iron concentration of $(8 \pm 2) \times 10^{11}\,\mathrm{cm}^{-3}$ is estimated from the bulk lifetimes of the tail wafers. This lifetime kinetics approach is also a demonstration of a new method to identify iron, or other getterable metals with moderate diffusivities such as chromium, in n-type silicon wafers.

## 1. Introduction

Silicon materials for photovoltaics (PV) generally contain more metal impurities and defects than microelectronic-grade silicon.[1] Gettering, by removing impurities from the silicon wafer bulk to a region of the device that is much less affected by impurities, mitigates the harmful impacts of some of the impurities on device performance. Gettering is hence a crucial step in silicon PV technology.[2] Among many gettering techniques, phosphorous (P) diffusion gettering (PDG or POCl₃ gettering) is one of the most effective and widely used in silicon PV.[2] In some cell

types where a conventional phosphorus diffusion step is not included, such as in silicon heterojunction (SHJ) cells, a phosphorus diffusion may be applied as a pre-gettering step to improve the bulk wafer quality prior to cell processing.[3,4] However, as wafer quality improves over time, the usefulness of a PDG process for current industrial-quality silicon wafers should be re-assessed, especially for n-type silicon wafers which generally have better electronic quality than p-type wafers.[5] Moreover, it is important to identify the limiting defects in industrial n-type silicon wafers, in order to identify ways to achieve further improvements in the future.

In p-type Si wafers, the measurement of minority carrier lifetimes before and after dissociating metal-dopant complexes is a widely used method for detecting iron (Fe) and chromium (Cr) concentrations in Si,[1] such as via iron-boron (Fe-B),[6,7] iron-gallium (Fe-Ga),[8,9] or chromium-boron (Cr-B) complexes[10] in p-type wafers. However, this is not possible on n-type wafers since no such metastable complexes between metal and dopant are available. As a result, detecting low concentrations of Fe or Cr in n-type Si wafers is challenging.

In the first part of this work, we assess whether or not a PDG process is necessary for current industrial-quality n-type Si wafers along a Cz-Si ingot. In the second part, we aim to identify the limiting defect(s) in the bulk of these industrial n-type Cz-Si wafers, by applying two approaches: 1) fitting the effective defect density ($N_{DD}$) (i.e., the inverse of the bulk lifetime, as explained below), as a function of the ingot solidified fraction using Scheil's equation to identify the segregation coefficient of the main bulk defect; 2) monitoring the kinetics of $N_{DD}$ changes upon a gettering anneal (using aluminium oxide (AlO$_x$))[11]. Combined with diffusion-limited gettering simulations[12] with different metal diffusivities,[1,13–15] the likely limiting metal impurity in these silicon wafers can be determined. This also demonstrates a new method to identify metal impurities in silicon wafers.

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## 2. Results and Discussion

### 2.1. POCl₃ Gettering Effectiveness

In order to quantify the POCl₃ gettering effectiveness, effective and bulk lifetimes of the Cz-Si wafers ($\tau_{\mathrm{eff,Cz}}$ and $\tau_{\mathrm{bulk,Cz}}$) along the ingot before and after gettering were assessed by applying
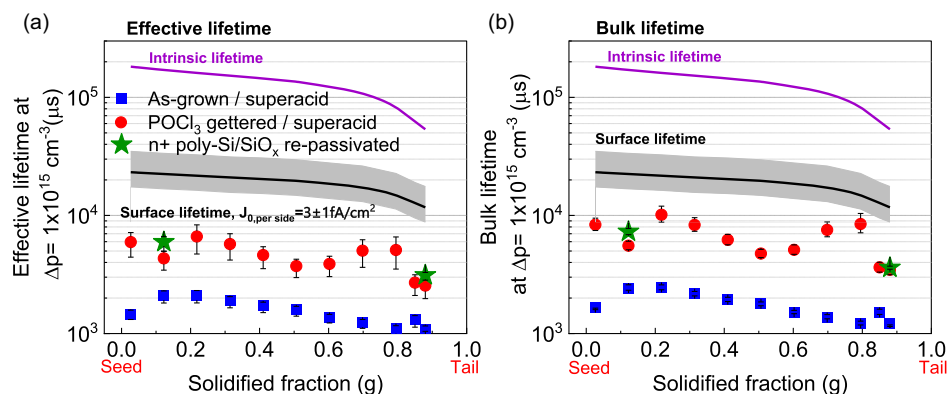
**Figure 1.** n-type Cz-Si wafers along an ingot, before and after gettering in terms of a) the effective lifetimes, $\tau_{eff}$; b) the bulk lifetimes, $\tau_{bulk}$, at an excess carrier density of $1 \times 10^{15}$ cm$^{-3}$. Intrinsic lifetimes from modelling[39,40] and surface-limited lifetimes estimated from the surface saturation current density ($J_0$) of co-processed FZ-Si control samples are also included in the plots. The star symbols refer to samples that received an additional POCl$_3$-diffused poly-Si/SiO$_x$ gettering and passivation step after the initial POCl$_3$ gettering and superacid passivation.

room-temperature superacid surface passivation,[16] which ensured no additional gettering or hydrogenation during surface passivation. As shown in **Figure 1**a, a significant increase of the effective lifetimes is observed after POCl$_3$ diffusion, for all of the n-type Cz-Si wafers along the ingot. The gettering effects can be observed more clearly in Figure 1b, which plots the bulk lifetimes of the Cz-Si wafers after considering intrinsic and surface lifetimes (Equation (1) and (2)). The surface saturation current density ($J_0$) derived from the co-processed float-zone silicon (FZ-Si) control samples, which amounted to $3 \pm 1$ fA cm$^{-2}$ per side, was used to estimate the surface lifetime ($\tau_{surface}$) of the Cz-Si samples.

As shown in Figure 1b, the gettering step increased the bulk lifetimes from an initial level of 1–3 ms in the as-grown state to 4–10 ms for the majority of the ingot. Only the tail part of the ingot (with an ingot solidified fraction ($g$) of $g > 0.8$) shows a smaller increase in $\tau_{eff}$, from 1–2 ms to 3–4 ms after gettering. The tail wafers will be examined in more detail in Section 2.3. The effectiveness of a gettering step for improving the bulk lifetimes across the entire ingot indicates that getterable metal impurities are one of the limiting defects in such Cz-Si wafers. Comparing the post-gettering bulk lifetimes with the surface and intrinsic lifetimes in Figure 1b, it can be seen that even after gettering, $\tau_{bulk}$ values across the entire ingot are still below $\tau_{surface}$ and are more than one order of magnitude lower than the intrinsic lifetime ($\tau_{intrinsic}$). There are two plausible explanations as follows:

Firstly, there may be potential to further enhance the gettering effect by optimizing the POCl$_3$ diffusion process. To examine this hypothesis, some wafers after POCl$_3$ diffusion and superacid passivation were re-passivated by POCl$_3$ diffused polysilicon films with an ultrathin thin silicon oxide interlayer (n + poly-Si/SiO$_x$) passivating contact structures on both sides. The P-doped poly-Si/SiO$_x$ structure is known to induce strong gettering effects during its formation,[17] and the good passivation quality of the n + poly-Si/SiO$_x$ ($J_0 = 2.5$ fA cm$^{-2}$ as derived from the co-processed FZ-Si control samples) allows us to extract the bulk lifetime. As shown in Figure 1, there is only a slight improvement in bulk lifetimes for the samples at $g = 0.12$ that underwent an additional poly-Si/SiO$_x$ gettering and passivation step. For the

tail samples at $g = 0.88$, no change in bulk lifetime is observed (Figure 1b). Therefore, we conclude that the initial PDG gettering step effectively removed any getterable impurities in these wafers.

The second possibility is that there are other defects within the silicon wafer bulk that cannot be removed by a typical gettering step. This aligns with the poly-Si/SiO$_x$ re-passivation results above. These remaining defects impose a limitation on the upper limit of the bulk lifetime after gettering. Photoluminescence imaging of the samples (not shown here) indicates no ring-defect formation after POCl$_3$ diffusion. However, oxygen-related defects in the Cz-Si wafer bulk cannot be entirely ruled out. As shown in Figure 1, the post-gettering lifetime variation along the ingot is not monotonic, that there is a decreasing trend in the middle of the ingot ($0.4 \leq g \leq 0.6$) before rising up and decreasing again. The decreasing lifetime towards the ingot tail can be explained by impurity segregation, as explained later in Section 2.2. However, the reason for the "dip" in lifetime in the middle of the ingot remains unclear. This cannot be explained by the variations in the sheet resistance after PDG (i.e., variations in the gettering effect), nor the variations in surface passivation among the Cz-Si samples. Therefore, the post-gettering lifetime trend along the ingot likely reflects the distribution of the remaining bulk defect or defects. The origin of the remaining defects after gettering, however, is unclear and requires further investigations.

Steinkemper et al. simulated the effect of the bulk lifetime on the cell efficiencies of various solar cell architectures, using conservative assumptions of the cell parameters. Their study suggests that, in general, bulk lifetimes exceeding 10 ms (for n-type silicon wafers with a resistivity range of $1-10\,\Omega$ cm) are required for achieving cell efficiencies above 25%.[18] A more recent analysis based on the high-efficiency n-type front junction (n-FJ) poly-Si/SiO$_x$ cell concept indicates that bulk lifetimes exceeding $\approx 11$ ms on n-type wafers with a resistivity of $1-10\,\Omega$ cm are necessary to achieve cell efficiencies above 26%.[19] The industrial n-type Cz-Si ingot investigated in this work shows that, despite heavy POCl$_3$ gettering, the overall bulk wafer quality across the entire ingot remains inadequate for achieving the production of very high-efficiency solar cells.
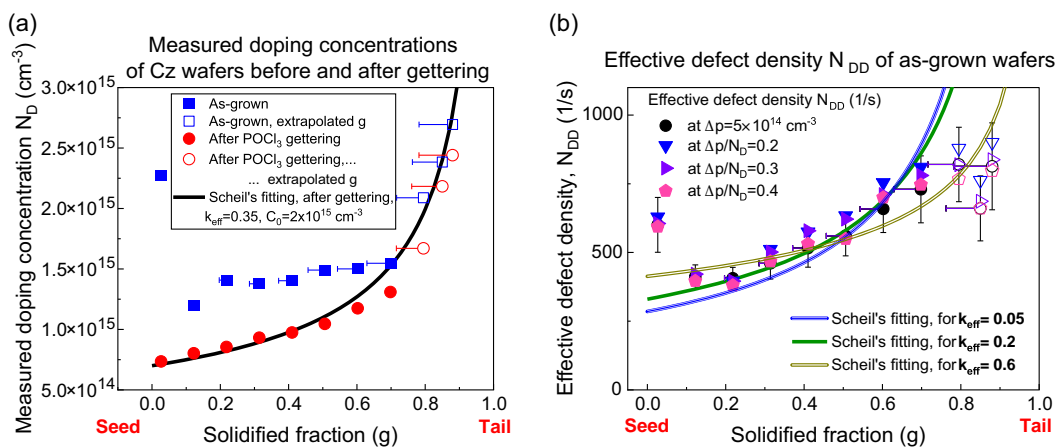
**Figure 2.** a) P-dopant concentration ($N_D$) from the measured wafer resistivity before and after gettering, and b) effective defect density ($N_{DD}$) of the as-grown wafers, as a function of the solidified fraction along the ingot. The smooth lines are fittings based on Scheil's equation.[20] The empty symbols in both (a and b) represent the data where the solidified fractions were estimated based on the extrapolated Scheil's fitting in (a).

## 2.2. Dopant Concentration and Scheil Fitting

**Figure 2**a shows the P-dopant concentrations ($N_D$), from resistivity measurements, before and after gettering. The P concentration variation along the ingot, after a high temperature POCl$_3$ diffusion-gettering process, obeys the Scheil law with a segregation coefficient of 0.35, which is consistent with the literature.[20] The discrepancy in $N_D$ values before and after gettering, in the seed and middle part of the ingot ($g < 0.6$), clearly indicates the presence of thermal donors in the as-cut wafers, which is a well-known effect in Cz-Si.[21–24] The discrepancy becomes smaller as $g$ increases, consistent with the known distribution of oxygen and thermal donors in Cz-Si ingots.[21]

There are uncertainties associated with the solidified fractions of the wafers, particularly for the wafers from the tail end of the ingot, due to an unknown amount of silicon melt remaining in the crucible after ingot growth, as well as an unknown proportion of the discarded tail section of the ingot prior to wafering. Consequently, the g values of the tail wafers ($g \geq 0.8$) were estimated based on the extrapolated Scheil's fitting to the measured N$_D$ data below $g < 0.8$ and the reported P segregation coefficient of 0.35 in Si.[20]

Figure 2b shows the bulk $N_{DD}$ of the as-grown Cz-Si wafers (from Equation (1) and (2)) as a function of g at different fixed dopant to excess carrier density ($N_D/\Delta p$) ratios and at a fixed injection level of $\Delta p = 5 \times 10^{14}$ cm$^{-3}$. Applying Scheil's law, the majority of the ingot ($0.12 \leq g \leq 0.8$) can be fitted using an effective segregation coefficient ($k_{eff}$) of less than 0.2. As $k_{eff} \leq 0.2$ is common for most of the metallic impurities in Si,[20] this fitting implies that metals may be the dominant limiting defects throughout the ingot. This agrees with the finding in Section 2.1 above that a gettering process to remove metals is shown to boost the bulk lifetimes for these Cz-Si wafers. Note that this analysis is based on the assumption that there is one single defect dominating the bulk lifetime of the Cz-Si wafers.

As shown in Figure 2b, the $N_{DD}$ data may also be fitted by a $k_{eff}$ of 0.6, if considering the tail part of the ingot (data denoted by empty symbols in Figure 2b). There are, however, much larger uncertainties associated with the solidified fractions of the wafers from the tail end of the ingot.

## 2.3. Identification of Bulk Limiting Metal Impurities

Given the presence of getterable metals within the Si wafers from the gettering results in Section 2.1, we introduced an additional step to identify the type of the metal in the wafers from the tail part of the ingot ($g \geq 0.8$), where the bulk lifetimes are the lowest. Because POCl$_3$ or poly-Si/SiO$_x$ gettering happens at high temperatures and at a rapid rate (due to fast metal diffusion at high temperatures), we cannot measure the gettering kinetics. Therefore, we used AlO$_x$ films as surface gettering layers[11,25] to getter the metal impurity from the silicon wafer bulk, and examined the lifetime changes (i.e., $N_{DD}$ changes) during the gettering process at 400 °C. This is because at low injection, the inverse of the Shockley–Read–Hall (SRH) lifetime ($N_{DD}$) is proportional to the defect density, if assuming one lifetime-limiting defect (Equation (3) and (5)). The lifetimes of the co-processed FZ-Si control samples with no bulk Fe implantation were found to be largely unchanged during the 400 °C anneals, indicating stable surface passivation. As the gettering kinetics is closely related to the metal diffusivity in Si, a diffusion-limited gettering model[26] was applied to fit the experimental $N_{DD}$ changes, as shown in **Figure 3**.

The method was first tested on an Fe-implanted n-type FZ sample with a known initial bulk Fe concentration of $(1.1 \pm 0.2) \times 10^{12}$ cm$^{-3}$ (Figure 3a). As shown in Figure 3a, the $N_{DD}$ kinetics can be well-fitted by the diffusion-gettering model using the literature reported Fe diffusivity in Si.[13] As described in ref. [26], the other fitting parameter in the model is the segregation coefficient of the applied AlO$_x$ films, which can be experimentally determined from the steady state Fe concentration ratio in Figure 3a.

Using a low injection level approximation (Equation (5)), from the lifetime measurements we estimated the bulk Fe concentration in these as-grown Cz tail wafers to be in the range of $(8 \pm 2) \times 10^{11}$ cm$^{-3}$. The hole capture cross section of Fe from ref. [13], $\sigma_p = 7 \times 10^{-17}$ cm$^2$, is used. In comparison, through the same lifetime approach, the bulk Fe concentration in the n-type Fe-implanted sample is estimated to be $1.5 \times 10^{12}$ cm$^{-3}$, which is very similar to the implanted dose of $(1.1 \pm 0.2) \times 10^{12}$ cm$^{-3}$.

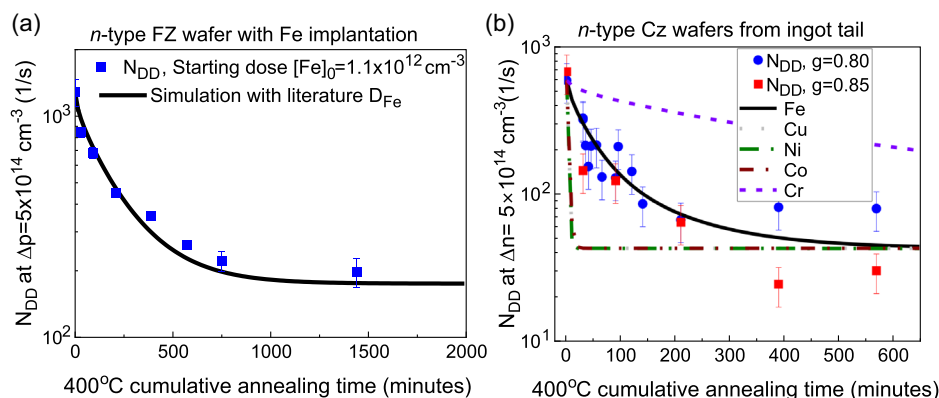**Figure 3.** 400 °C AlO$_x$ gettering kinetics of a) an n-type FZ-Si wafer with $1.1 \times 10^{12}$ cm$^{-3}$ Fe implanted into the silicon wafer bulk; and b) n-type Cz-Si tail wafers with solidified fractions of $g = 0.8$ and $g = 0.85$ (1.9 and 1.6 $\Omega$ cm). The smooth lines represent a simulation of the gettering kinetics based on different metal diffusivities, including Fe,[13] Cu,[14] Ni,[15] Co[1] and Cr.[27] The error bars arise from assuming a 20% uncertainty in the $N_{DD}$ (i.e., inverse lifetime) values.

The same model, including the same segregation coefficient of AlO$_x$ from Figure 3a, was then applied to fit the $N_{DD}$ kinetics of the Cz-Si tail wafers, as shown in Figure 3b, using the literature reported diffusivities of the common metal impurities in silicon: Fe,[13] Cu,[14] Ni,[15] Co[1] and Cr.[27] Figure 3b clearly shows that only Fe can fit the experimental $N_{DD}$ kinetics, due to the very large differences in the metal diffusivities (varying by orders of magnitude). This result suggests that Fe is the limiting defect in these Cz-Si wafers, at least in the wafers from the tail part of the ingot.

## 3. Conclusion

This work confirms the benefit of a gettering step for current industrial n-type Cz-Si wafers along the entire ingot length, by showing significant improvements in bulk lifetimes after gettering. Following a heavy POCl$_3$ diffusion-gettering process, bulk lifetimes increased from an initial level of 1–3 ms in the as-grown state to 4–10 ms for the majority of the ingot. However, the tail part of the ingot (with a solidified fraction $g > 0.8$) exhibited a smaller increase in effective carrier lifetimes, only from 1–2 to 3–4 ms. The bulk lifetimes after POCl$_3$ gettering, however, are still lower than both the surface lifetimes (with a $J_0$ of $3 \pm 1$ fA cm$^{-2}$ per side) and the intrinsic lifetime limits. This indicates that the bulk material quality is still a limiting factor for high-efficiency solar cells, at least for the industrial ingot investigated in this study.

The significant lifetime improvements after gettering suggests the presence of getterable metals in these Cz-Si wafers, limiting the wafer lifetimes in the as-grown state. Analysis of the bulk lifetime distribution throughout the ingot also suggests that metal impurities dominate the recombination activity of the bulk, although uncertainties in the solidified fractions for the tail wafers make this conclusion less strong. Nevertheless, further analysis of the lifetime changes during a low-temperature AlO$_x$ gettering process, accompanied with diffusion-gettering simulations based on the known metal diffusivities in silicon, confirm the presence of Fe in these wafers. In the tail part of the ingot, the bulk Fe concentrations are estimated to be $(8 \pm 2) \times 10^{11}$ cm$^{-3}$ for the investigated wafers. This gettering approach also demonstrates a new method to detect Fe, or other getterable metals with measurable gettering kinetics such as Cr, in n-type Si wafers.

## 4. Experimental Section

The silicon wafers examined in this study were industrially-grown n-type phosphorus (P)-doped Czochralski silicon (Cz-Si) wafers selected from along the same ingot. The ingot was grown in a single batch without melt recharging, and therefore Scheil's distribution of impurities is valid here. The resistivity of the wafers along the ingot ranged from 3.3 to 1.6 $\Omega$ cm in the as-grown state, and from 6.2 to 1.5 $\Omega$ cm after diffusion, due to thermal donor annihilation (as discussed in Section 2.2). The wafers were $145 \pm 5$ µm thick after saw damage etching. Co-processed control samples were n-type phosphorus-doped FZ Si wafers of $1.9 \pm 0.2$ and 100 $\Omega$ cm, and were $150 \pm 5$ µm thick after surface etching.

Phosphorus diffusion was achieved by using POCl$_3$ as a diffusion source in a quartz tube furnace. POCl$_3$ diffusions were carried out at 770 °C for 20 min, followed by a 30 min drive-in at 900 °C, achieving a sheet resistance of 20–35 $\Omega/\square$. After POCl$_3$ diffusion, the wafers were subject to a tetramethylammonium hydroxide (TMAH) etching of approximately 5 µm/side to remove the diffused layers. In this work, the gettering effectiveness of the applied PDG process was studied via assessing the lifetimes of the wafers before and after gettering using a room-temperature superacid passivation scheme.[16] This passivation scheme ensures that minimal gettering or hydrogenation occurs during surface passivation, unlike silicon nitride or aluminium oxide surface passivation.[4,28–31] The superacid passivation procedure is described below.

After TMAH etching of the wafer surfaces, the wafers underwent additional standard Radio Corporation of America (RCA) cleaning (RCA 1 and 2) steps. Subsequent to RCA2, the wafers were subjected to a hydrofluoric acid (HF) dip in a 0.5% HF solution until hydrophobic. The hydrophobic wafers were immediately immersed in a superacid solution (described as follows) in a fume-hood under ambient air for 45 s and then dried in the same fume-hood for a few minutes. Effective lifetimes were measured by a photoconductance-based lifetime tester (mentioned later) immediately after the completion of the drying process following superacid passivation.

The superacid solution was prepared by mixing 100 mg of bis(trifluoromethane)sulfonimid (TFSI) (from Sigma Aldrich, >95% purity) in 50 mL of hexane (Sigma Aldrich, >95% purity), shaking well until all solid dissolved.[16,32–34] Due to the air-sensitive nature of TFSI, all handling and

storage of TFSI were performed under a nitrogen glove box. A new 50 mL solution was prepared for each batch of passivation. The superacid passivation quality was evaluated using n-type FZ control wafers as described above. A good surface passivation of $J_0 = 2$–$4$ fA cm$^{-2}$ per side was consistently observed for the n-type FZ control wafers. The surface recombination velocities for TFSI in TFSI/hexane solutions were typically reported to be 2 cm s$^{-1}$, aligning well with our measured $J_0$ values.[34]

To verify the measured bulk lifetimes using an alternative surface passivation scheme, some of the POCl$_3$ diffused and superacid passivated samples underwent re-passivation with POCl$_3$ diffused polysilicon films with an ultrathin thin silicon oxide interlayer (poly-Si/SiO$_x$) passivating contact structure on both sides. As well as providing good surface passivation to extract the bulk lifetimes, this step also provides additional gettering effects, allowing the completeness of the prior PDG gettering to be assessed. n-type FZ-Si wafers of $1.9 \pm 0.2\,\Omega$ cm were co-processed to measure the surface passivation quality of the n + poly-Si/SiO$_x$ structure. The poly-Si/SiO$_x$ structures were fabricated as follows. After superacid passivation and measurements, the wafers were cleaned and thin silicon oxide layers were grown on the wafer surfaces through chemical oxidation in a 68 wt% nitric acid bath at 90 °C for 30 min, resulting in a SiO$_x$ layer thickness of $1.3 \pm 0.1$ nm, as measured by spectroscopic ellipsometry.[26] Subsequently, a 100 nm thick intrinsic amorphous silicon (a-Si) layer was deposited by low pressure chemical vapour deposition (LPCVD) at 500 °C. The samples then underwent a POCl$_3$ diffusion process at 84 °C for 20 min deposition and 30 min drive-in, resulting in a sheet resistance of $\approx 100\,\Omega/\square$. The loading and unloading temperatures were 70 °C, with a ramp-up and ramp-down rate of 10 °C min$^{-1}$.

For the defect identification studies using aluminium oxide (AlO$_x$) gettering kinetics, the industrial n-type Cz-Si wafers near the tail end of the ingot ($g \geq 0.8$) were used. The wafer resistivities were 1.9 and 1.6 $\Omega$ cm. Additional n-type FZ-Si control wafers, of $1.9 \pm 0.2\,\Omega$ cm and 290 μm thickness were prepared. One set of the FZ-Si wafers were ion implanted with Fe and annealed, resulting in $(1.1 \pm 0.2) \times 10^{12}$ cm$^{-3}$ Fe uniformly distributed in the bulk (see[35] for the ion implantation and annealing details), while the other set had no Fe implantation. Both of the Cz-Si and FZ-Si samples (with and without bulk Fe) were subject to depositions of plasma-enhanced atomic layer deposition (PE-ALD) of AlO$_x$ films on both sides. The PE-ALD AlO$_x$ films were 20 nm thick, deposited at 175 °C using trimethylaluminum (TMA) and oxygen (O$_2$) plasma (Beneq TFS 200 series reactor), followed by a forming gas anneal at 400 °C for 30 min for activating the passivation effect of the AlO$_x$ films.[36] For tracking the gettering kinetics, these double-side AlO$_x$ coated samples were subjected to cumulative anneals at 400 °C $\pm$ 5 °C on a hotplate in air with a temperature controller. The temperature of the hot plate was confirmed with a digital thermometer until the 400 °C $\pm$ 5 °C was stabilized. The effective minority carrier lifetimes after each anneal were measured (measurement details as follows).[25,28]

Injection-dependent effective minority charge carrier lifetime curves were measured by a photoconductance-based lifetime tester from Sinton Instruments.[37] The resistivity of the wafers was measured before and after gettering using the Sinton lifetime tester, based on the dark conductance. The surface saturation current density $J_0$ was extracted from the lifetime curves based on the Kane and Swanson method.[38] The inverse effective lifetime curves of the FZ-Si control samples, which are used to extract $J_0$, are included in Supplementary Information.

Assuming one dominant recombination active defect in the silicon wafer bulk, the effective defect density, $N_{DD}$, in the bulk of the wafers was determined by two approaches. Firstly, for the samples in Section 2.1 and 2.2, where there is a variation in wafer resistivity along the ingot, the bulk lifetime is estimated using Equation (1)

$$N_{DD} = \frac{1}{\tau_{bulk}} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{intrinsic}} - \frac{1}{\tau_{surface}} \tag{1}$$

Where $\tau_{bulk}$ is the bulk lifetime, $\tau_{eff}$ is the measured effective lifetime, $\tau_{intrinsic}$ is the intrinsic lifetime,[39,40] and $\tau_{surface}$ is the lifetime due to surface passivation. The surface lifetime in Equation (1) was calculated by[41]

$$\frac{1}{\tau_{surface}} = 2 \times J_0 \frac{N_D + \Delta p}{q n_i^2 W} \tag{2}$$

where $J_0$ is surface saturation current density derived from the lifetime curves of the co-processed FZ-Si control samples through the Kane and Swanson method,[38] $N_D$ is the P-doping concentration, $\Delta p$ is the excess carrier concentration, $q$ is the elementary charge, $n_i$ is the intrinsic carrier concentration, and $W$ is the wafer thickness.[41]

Secondly, for the samples undergoing AlO$_x$ gettering in Section 2.3, $N_{DD}$ was estimated using Equation (3). This is because, firstly, there is a substantial difference between the lifetimes of the co-processed control samples with no Fe (>4 ms) and the lifetimes of the Cz-Si tail samples ($\approx$1–2 ms), and secondly, there may be potential changes in the surface lifetimes of the control samples during cumulative annealing. Note that the FZ control samples did undergo a high temperature annealing (while being co-processed with ion implanted samples to distribute Fe) and the POCl$_3$ gettering to annihilate grown-in defects which may appear at low temperatures.[42]

$$N_{DD} = \frac{1}{\tau_{bulk}} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{eff, FZ\ control}} \tag{3}$$

Where $\tau_{eff, FZ\ control}$ is the measured effective lifetime of the parallel-processed FZ control wafer of similar resistivities, which is used to account for the overall effect of intrinsic and surface lifetimes, as well as the lifetimes due to potential external contamination during processing. Results later showed that the changes in $\tau_{eff, FZ\ control}$ during AlO$_x$ gettering anneals were small.

As reported in ref. [43], the SRH lifetime statistics can be rearranged in the linear form of

$$\tau_{SRH} = mX + b \tag{4}$$

where $X = \frac{n}{p} = \frac{(n_0 + \Delta n)}{(p_0 + \Delta n)}$, with $\Delta n$, $\Delta p$ being the excess electron and hole carrier density, and $n_0$ and $p_0$ are the equilibrium electron and hole carrier densities, respectively. The slope $m$ and the intercept $b$ of the linear form in Equation (4) are constants based on the defect parameters.[43]

For n-type Si, $\Delta n = \Delta p \gg p_0$ and thus $X \approx \frac{n_0 + \Delta p}{\Delta p} = 1 + \frac{n_0}{\Delta p}$. Consequently, the $\tau_{SRH}$ curve is a function of only $\frac{n_0}{\Delta p}$ (or $\frac{N_D}{\Delta p}$ with $N_D$ being the P-doping concentration). As a result, to compare the $N_{DD}$ of the wafers from different ingot positions, that is, different P-doping concentrations $N_D$, the same $\frac{N_D}{\Delta p}$ ratios were applied in Section 2.2. The $N_{DD}$ values at a constant injection of $\Delta p = 5 \times 10^{14}$ cm$^{-3}$ were also extracted for comparison in Section 2.2.

At low injection, where the excess carrier densities are much smaller than the doping concentration, according to Shockley-Read-Hall (SRH) statistics, $N_{DD}$ can be approximated by

$$N_{DD} \approx N_t \sigma_p \nu_p \tag{5}$$

where $\sigma_p$ is the hole capture cross section, $\nu_p$ is the carrier thermal velocity ($\nu_p = 1.1 \times 10^7$ cm s$^{-1}$)[5] and $N_t$ is the defect concentration. Equation (5) will then be used in Section 2.3 to estimate the Fe concentration in Cz-Si tail wafers from the lifetime measurements at low injection.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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