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An adaptive calibration technique of timing skew mismatch in time-interleaved analog-to-digital converters

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ABSTRACT

Because of the exponential increase of sampling rate, time-interleaved analog-to-digital converter (TIADC) has a fast growth in the high-speed applications. However, the channel mismatch error is a serious challenge for the performance of TIADC. In this article, we address the timing skew mismatch error and propose a novel adaptive calibration method. The principle and operating process of the calibration algorithm are explained. To validate the proposed technique, we designed a four-channel TIADC-based digital oscilloscope with a sampling rate of 10 GS/s. Based on this instrumentation platform, (i) calibration algorithm was implemented by hardware; and (ii) a test platform consisting of advanced instruments and tools was setup to testify the effect and robustness of proposed algorithm. Moreover, the technical details of instrumentation are described for the first time. The experimental results show that the calibration algorithm significantly suppresses the distortions due to timing skew mismatch error. The TIADC-based instrumentation achieves spurious-free dynamic range of 52.48 dB and effective number of bits of 5.83 bit, respectively. Besides, the complexity of the proposed algorithm is compared and discussed.

I. INTRODUCTION

The time-interleaved analog-to-digital converter (TIADC) structure breaks the bottleneck speed of single converter. Recent reports show that the state-of-the-art commercial analog-to-digital converters (ADCs) have achieved a sampling rate of up to 64 GS/s[1] and 72 GS/s[2] by using this structure. Currently, time-interleaved sampling technique is not only used in the design of ADCs, it has also been expanded to a lot of high-speed applications, such as radio base stations in the field of wireless communication, spectrometer in the field of instrumentation, and charge coupled device (CCD) imaging in medical image processing.[3–5]

However, since the characteristics of all the ADCs (or circuit channels) are not identical in reality, channel mismatch errors are caused. Among these channel mismatch errors, the TIADC is mainly of three types: offset errors, gain errors, and timing skew errors. These errors lead to distortion and degrade system performance seriously,[6–8] i.e., effective number of bits (ENOB) and spurious-free dynamic range (SFDR).

Because of the significant improvement and easy-to-use realization, TIADC technique attracts the attention of many researchers and many techniques and algorithms about calibration of channel mismatch errors have been proposed.[7–17] Gain and offset mismatch errors are investigated early; these two types of errors can be calibrated using a method that is easy to implement, such as Lagrange interpolation,[18] sine-fit,[14] and fast Fourier transform (FFT) based method.[19] When compared with gain and offset errors, timing skew errors cannot be easily calibrated by direct calculation methods and this problem has been investigated for a long period.[9–11,20]

Two types of timing skew error calibration are proposed in recent years. All-digital compensation is popular in the converter design where the skew errors are corrected by the digital filter. Nortz proposed a digital derivative-based timing skew error estimation algorithm and compensated

skew error in the digital domain.[11] However, all-digital technique requires an extra lookup table (LUT) for storing filter coefficients and additional resources for coefficient modification. Another type of calibration method is mixed-signal compensation that was used popularly in circuit-level applications.[9,10,20] In Ref. 20, the skew error is estimated by the cross covariance between outputs from two ADCs. The estimated value is compensated by an on-chip control. This type of method avoids the complexity of circuit design.

In this article, to address the problem of timing skew mismatch, a novel adaptive algorithm for timing skew mismatch error calibration is proposed. Based on this technique, an implementation of four-channel TIADC-based oscilloscope is presented. Comparison of similar calibration methods shows that the proposed algorithm has a good performance in the resource overhead. By using the adaptive calibration technique, the oscilloscope works with an ENOB of 5.8 bit and an SFDR of 52.48 dB. The remainder of the article is organized as follows: Sec. II illustrates the background of timing skew mismatch and the conceptual estimation algorithm. Then, a four-channel TIADC is implemented and presented in Sec. III. In Sec. IV, the experimental results and discussions are shown. Finally, future work is discussed in Sec. V.

II. MISMATCH ESTIMATION IN TIADC

A. Timing skew mismatch in TIADC

The ideal sampling instant in TIADC is integer times the sample period T_s. As shown in Fig. 1(a), timing skew mismatch, represented by Δt_i, is the static deviation between the ideal sampling instant and the real sampling instant. In the ith ADC, timing skew causes irregular sampling intervals, which leads to the voltage error between the ideal samples $\hat{x}_i[n]$ and real samples $\tilde{x}_i[n]$, as shown in Fig. 1(b). After signal reconstruction, serious distortions are generated in the final output due to the timing skew mismatch error.

If the frequency response of the input signal is $X(j\Omega)$ and the radian sampling rate of ADC is Ω_s, we can derivate the output spectrum of an M-channel TIADC using sampling theorem. Disregarding the gain and offset mismatch, the spectrum of output can be derived as

$$\tilde{X}(e^{j\Omega T_s}) = \frac{2\pi}{\Omega_s}\sum_{p=-\infty}^{\infty} X\left(j\left(\Omega - p\frac{\Omega_s}{M}\right)\right)\alpha_p\left(j\left(\Omega - p\frac{\Omega_s}{M}\right)\right), \quad (1)$$

where the influence of timing skew mismatch is given by

$$\alpha_p(j\Omega) = \frac{1}{M}\sum_{i=0}^{M-1} e^{-j\Omega\Delta t_i}\cdot e^{-jpi\frac{2\pi}{M}}. \quad (2)$$

For example, a full-scale cosine input signal with a response of $X(j\Omega) = \pi[\delta(\Omega-\Omega_0)+\delta(\Omega+\Omega_0)]$, where Ω_0 is the frequency of input, sampled by an M-channel TIADC will have response of

$$\tilde{X}(e^{j\Omega T_s}) = \frac{2\pi}{M\Omega_s}\sum_{p=-\infty}^{\infty}\sum_{i=0}^{M-1}\pi\left[\delta(\Omega-\Omega_0-p\frac{\Omega_s}{M}) + \delta(\Omega+\Omega_0-p\frac{\Omega_s}{M})\right]e^{-j(\Omega_0\Delta t_i - pi\frac{2\pi}{M})}. \quad (3)$$

It can be obviously seen that the spectrum is aliased by the distortions due to the timing skew mismatch error. Except for the original signals at $\Omega = \pm\Omega_0$, timing mismatch spurs that locate at $\Omega = \Omega_0 \pm p\Omega_s/M$ degrade the performance of TIADC seriously. To eliminate the timing mismatch distortions, we propose a practical timing skew mismatch calibration algorithm based on adaptive signal processing.

B. Calibration algorithm

Figure 2 illustrates analog signal $x(t)$ sampled by two-channel TIADC. The analog signal is digitized by ADC0 with a clock phase of Φ_0. We mark this signal as the signal without timing skew error, represented by $x_0[n]$. The signal digitized from the other ADC with a clock phase of Φ_1 is the signal that needs to be calibrated.

To explain the proposed algorithm, we define two reference signals, denoted as x_{ref1} and x_{ref2}. The reference channels must be selected either from the initial base reference channel or the calibrated channels. In this case, we define $x_{ref1}[n] = x_0[n]$ and $x_{ref2}[n] = x_0[n-1]$. Using the two reference signals, two error signals are defined as $e_1[n] = x_1[n] - x_{ref1}[n]$ and $e_2[n] = x_1[n] - x_{ref2}[n]$. When the timing skew error is eliminated, the reference channels are evenly spaced before

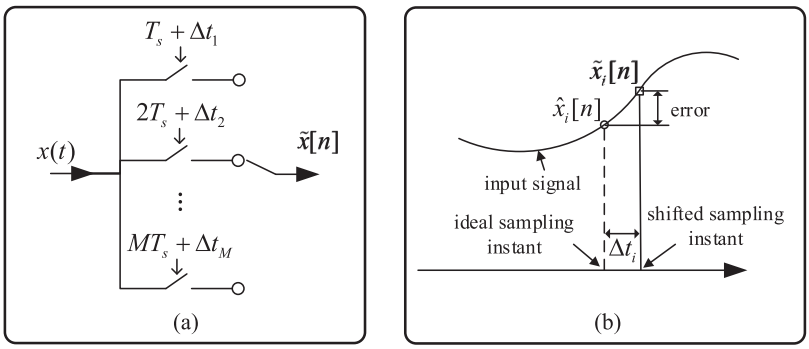

FIG. 1. Sampling diagram of an M-channel TIADC with timing skew mismatch error. Timing skew of the ith ADC is denoted as Δt_i. $\hat{x}_i[n]$ and $\tilde{x}_i[n]$ represent the ideal sample and real sample of the ith ADC. (a) Illustration of TIADC with timing mismatch. (b) Sampling in the ith ADC.

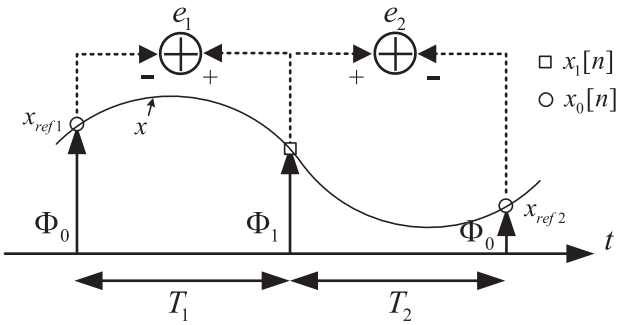

FIG. 2. Illustration of a waveform sampled by two-channel TIADC, with a sampling clock phase of Φ_0 and Φ_1; e_1 and e_2 are the voltage differences between two adjacent samples. Since there is no timing skew error between circle samples, two reference signals are selected to calibrate the signal with the phase of Φ_1.

and after the calibrated channel, i.e., $T_1 = T_2$. In this case, the following relationship can be established:

$$E(|e_1|) = E(|e_2|). \tag{4}$$

When the signal has timing skew error, the established equality relationship is broken. Expanding this relation to M-channel TIADC, a criterion of mismatch estimation can be established, given by $\hat{e}_i = E(|e_1|) - E(|e_2|)$. Based on this relationship, we proposed an adaptive calibration algorithm which is mainly comprised of two parts: strategy for reference signal selection and the calibration process of a single channel.

In the following discussion, the input signal is assumed quasi-stationary and band limited to the Nyquist frequency of the complete ADC system. Besides, the channel number M is required to be an integer power of two, i.e., $M = 2^D$. According to Ref. 12, it requires extra hardware resource to build a reference channel for calibration. However, there is no auxiliary hardware for the reference channel because each channel can serve as the reference channel in the proposed algorithm.

1. Strategy of reference signal selection

As mentioned above, the signal with timing mismatch error is estimated by two reference signals. The selection strategy expanded to arbitrary M-channel TIADC is explained in this part.

The analog signal digitized by the ith ADC is represented as $x_i[n]$. First, to have two reference signals for the start of calibration, we select the signal obtained by ADC0 as the initial overall base reference signal without timing skew error, denoted as $x_0[n]$. The base signal with unit latency is chosen as another reference signal, denoted as $x_0[n-1]$. Thus, the calibration process starts with $x_0[n]$ and $x_0[n-1]$. Second, the channel in the middle of two neighbored sample from ADC0 is selected as the signal to be calibrated. In the following, the calibration of a single channel starts. After calibration, the skew error of this channel is eliminated and this channel can serve as a new reference channel. The next round of calibration starts when the first round ends. It requires a total of $D = \log_2 M$ rounds of calibration. We let symbol k denote the round index, where $k = 1, 2, \ldots, D$. In the kth round, a total number of 2^{k-1} signals need to be calibrated. Symbol j denotes the index of the signal to be calibrated, where $j = 1, 2, \ldots, 2^{k-1}$. For the jth signal in the kth round, the corresponding channel index of the signal (from 0 to M) to be calibrated and the two reference signals can be calculated with the following equation:

$$i = I(j,k) = M \cdot \frac{2j-1}{2^k}, \tag{5}$$

$$ref1 = I_{left}(j,k) = M \cdot \frac{j-1}{2^{k-1}}, \tag{6}$$

$$ref2 = I_{right}(j,k) = \left\langle M \cdot \frac{j}{2^{k-1}} \right\rangle_M, \tag{7}$$

where the notation $\langle m \rangle_M$ denotes modulo.

Figure 3 shows the sampling sequences of a four-channel TIADC, where the sample instants are modelled by the impulse train. In the figure, the reference signal is represented by a regular up-arrow. The bold up-arrow that stands in the middle of the two reference signals denotes the uncalibrated signal. The dashed up-arrow represents the unused signal in this round of calibration. In the first round, ADC2 (with a clock phase of Φ_2) is calibrated using the neighboring two samples of ADC0 (with a clock phase of Φ_0). After the calibration process, ADC2 is the new reference channel for calibration. In the second round, the timing skew mismatch of ADC1 is corrected, using the reference signal from ADC0 and ADC2. Meanwhile, signal from ADC3 is calibrated by samples ADC2 and ADC0.

The strategy for the selection process follows a fast binary searching algorithm. The calibration starts in the middle of two base reference signals. This continues until all the signals are calibrated. The proposed calibration algorithm reduces the time consumed by the traditional algorithm that corrects errors channel by channel.

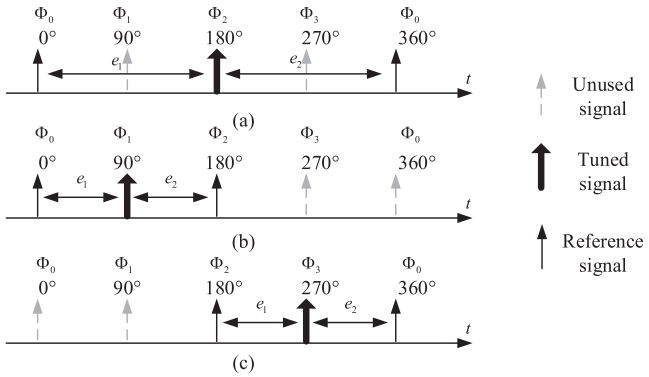

FIG. 3. Timing skew mismatch error calibration sampling sequence of four-channel TIADC; (a) first step: calibration of ADC2 (with a clock phase of Φ_2). After this process, ADC2 can be used as the reference channel for ADC1 (with a clock phase of Φ_1) and ADC3 (with a clock phase of Φ_3) calibration; (b) second step: calibration of ADC1; and (c) third step: calibration of ADC3.

2. Calibration of a single channel

After two reference signals are selected, the timing skew mismatch error of the calibrated channel should be estimated and compensated. In the proposed algorithm, skew error is estimated by an iterative calculation. When estimated timing mismatch error converges, the calibration process ends. Details of this procedure is explained as following.

First, e_1 and e_2 are calculated by subtracting the two signals from the reference channel to the uncalibrated channel. Next is the absolute value operation (ABS) of the two error signals. The difference between the two absolute sequences is calculated and the result is sent to the averaging unit to calculate the expectation value. After that, the estimation criteria $\hat{e}_i$ are obtained, which is the core evaluation of the adaptive algorithm. The adaptive estimation r_i is time varying, which is then updated by

$$r_i(k) = r_i(k-1) - \mu \cdot \hat{e}_i(k). \tag{8}$$

The above process is the estimation of the ith channel, which calculates the estimation of timing skew mismatch error r_i. Next, the phase of the sampling clock needs to be accurately tuned according to the estimated error. These adjustment elements are controlled by digital control word (DCW). Generally, the DCW is sent to a register that is embedded in a phase-locked loop (PLL) or ADC. After the phase tuning, one iteration of the entire calibration process is complete. After several training periods, the real timing skew error of the calibrated channel is suppressed.

Two points should be addressed in this process. The first is the stepping value of the update equation. When the algorithm works with larger μ, the convergence speed is fast, but the precision is lost; when μ is small, the estimation accuracy is high, but the convergence speed is slow. The second point is the convergence condition. In most cases, we use constant times of iteration or fixed training time. However, if the algorithm has requirements for high efficiency and accuracy, this condition can be modified as follows: when the estimation value converges to an extremely small factor, that is, when the condition of $[r_i(k) - r_i(k-1)]/r_i(k-1) < \varepsilon$ is satisfied, the algorithm ends immediately, where ε is the accuracy factor; otherwise, a new calibration period starts. But high accuracy needs extra power consumption on judgement. In actual applications, μ and the convergence condition need to be optimized and judged according to the actual requirement.

III. IMPLEMENTATION OF FOUR-CHANNEL TIADC

A four-channel TIADC example of the proposed mixed-signal timing skew calibration algorithm is shown in Fig. 4. The analog input is first divided into four channels by the splitting network. Then the signals are sent to the corresponding ADC for sampling. The output of the ADC should be fed back signal into timing skew estimator and compensation unit for calibration. After a period of calibration, the calibrated signals are combined into one data stream. As the important part of acquisition, the calibration algorithm follows the modular design. The estimation process is implemented in the block of timing skew estimator. The compensation process is mainly implemented in the compensation unit.

A. Timing skew estimator

The estimation of timing skew mismatch error has been investigated for a long time, including the Lagrange interpolation method,[18] three-parameter sine-fit method,[14] and FFT computing method.[19] In this work, we proposed an adaptive estimation method that requires lower computation and time complexity than the previous techniques. All the cell diagram blocks are implemented in the field programmable gate arrays (FPGAs). As depicted in Fig. 5, this module estimates the timing skew using four computing units: adders, absolute value calculation (ABS), one averaging unit (AVG), and adaptive engine. By collecting samples from the uncalibrated channel and the two reference channels, the timing skew mismatch error is estimated and finally converges.

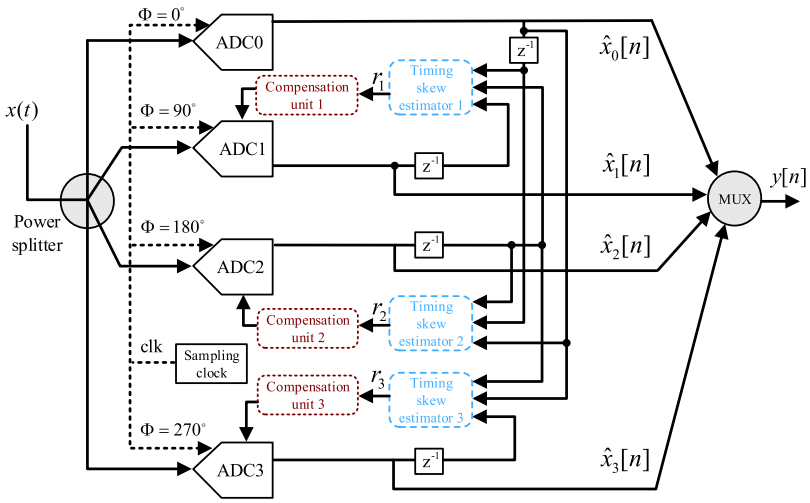

FIG. 4. Overall timing skew mismatch error calibration structure of four-channel TIADC. r_i and $\hat{x}_i[n]$ represent the value of the estimated error and calibrated signals of the ith channel, respectively. Because ADC0 is marked as the base reference channel, $\hat{x}_0[n]$ is just the output of ADC0. In the other channels, the output of ADC should be fed back to timing skew estimator and compensation unit for calibration.

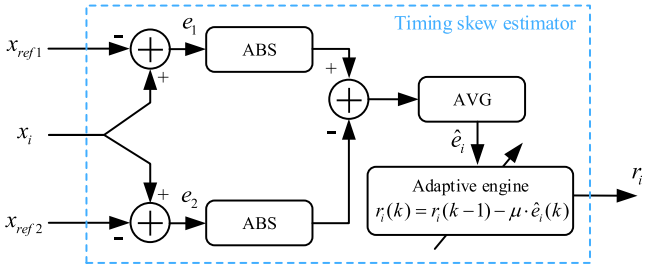

FIG. 5. Illustration of the timing skew estimator structure. Based on the uncalibrated signal x_i and two reference signals x_{ref1} and x_{ref2}, the value of the estimated error r_i is estimated. As the number of training periods increasing, the estimated error converges.

Since ADC0 is selected as the base reference channel, the output of ADC0 is the calibrated signal. In the first round of calibration, the original signal from ADC0 and its delayed signal, $\hat{x}_0[n]$ and $\hat{x}_0[n-1]$, serve as the reference signals to calibrate the output of ADC2. After convergence of the ADC2's estimation, the calibration process ends. Then, the signal $\hat{x}_2[n]$ is put into the reference signal set. Second, the outputs of ADC0 and ADC2 are used as reference signals to calibrate the outputs of ADC1 and ADC3. The corresponding reference signal selection strategy is summarized in Table I. In actual application, the two rounds can be processed simultaneously. All channels are calibrated when the three estimated errors converge.

B. Compensation unit

To avoid the complexity of digital circuits design and extra power consumption, this work uses the mixed-signal compensation technique. In this design, the selected ADC has an embedded external phase control register (EPCR) that supports the on-chip phase tuning. Figure 6 shows the workflow of the entire compensation process. The compensation unit has three inputs: uncalibrated signal, the estimation value, and sampling clock. In the beginning, the estimation value r_i is converted to DCW R_i. The kth conversion equation is

$$R_i(k) = R_i(0) - [r_i(k)/S], \tag{9}$$

where the notation $[\cdot]$ indicates rounding operation. The default value of DCW $R_i(0)$ and the adjustable step S are determined by the specific ADC. Taking the selected ADC as an example, the adjustable range of ADC is ~±15 ps with a step value of ~30 fs. The initial value of EPCR is a hexadecimal code "0x200" corresponding to 0 ps delay.[21] In this case,

TABLE I. Reference signal selection.

Channel	x_i	x_{ref1}	x_{ref2}
Channel 0	$x_0[n]$	Base reference	
Channel 1	$x_1[n]$	$x_0[n]$	$x_2[n]$
Channel 2	$x_2[n]$	$x_0[n-1]$	$x_0[n]$
Channel 3	$x_3[n]$	$x_2[n]$	$x_0[n-1]$

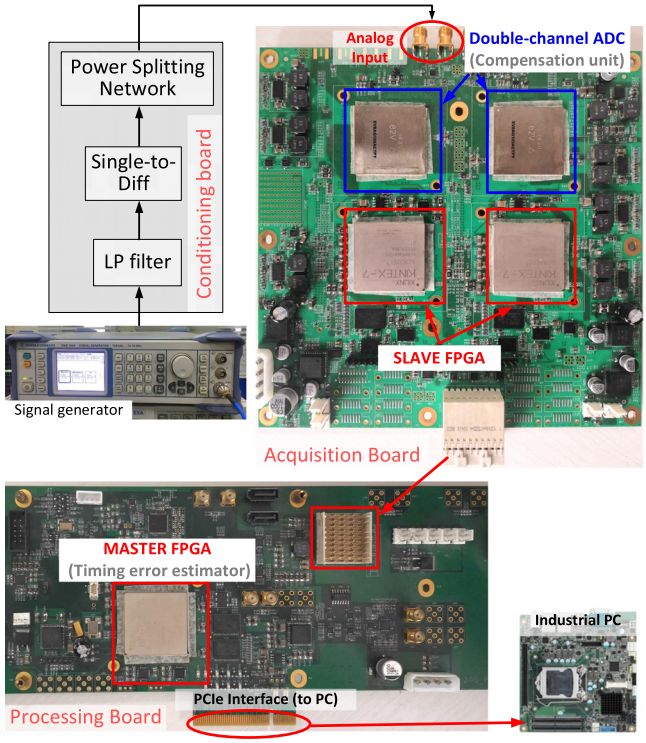

FIG. 6. Hardware implementation of 10 GS/s four-channel TIADC.

DCW of Eq. (9) has a hexadecimal value and is calculated by $R_i(k) = 0x200 - [r_i(k)/0.03]$. The calculation of DCW is implemented in FPGA. Second, the DCW is sent to EPCR through a serial peripheral interface (SPI) to generate a phase correction offset that adds to the sampling clock. This tuning process is implemented inside the ADC but under the control of FPGA. Finally, driven by the adjusted sampling clock, the ADC core is able to digitize signals at the correct instant. Through a period of training, the estimation of timing skew mismatch error of signal x_i converges. The calibration process ends.

C. Hardware implementation

The proposed calibration algorithm was totally implemented in a four-channel TIADC-based oscilloscope, as shown in Fig. 7. The hardware of the oscilloscope is mainly

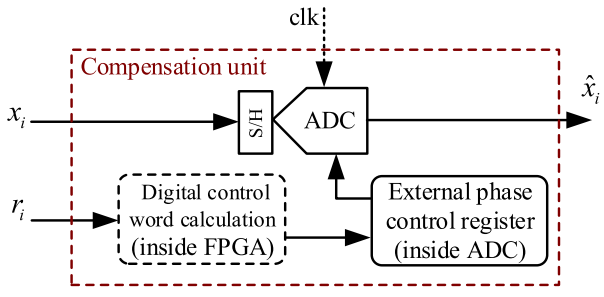

FIG. 7. Illustration of the compensation unit structure.

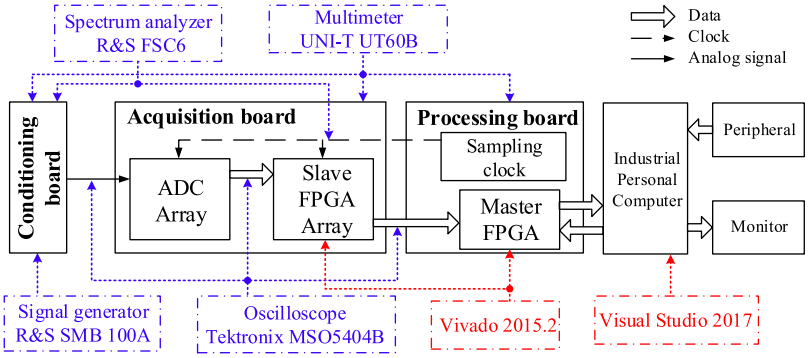

FIG. 8. Testing and application platform.

comprised of one embedded controller and three circuit boards: conditioning board, acquisition board, and processing board. Conditioning board is designed to adapt the ADC's input requirements and avoid signal aliasing, including modules of antialiasing filter, single-ended to difference circuit and power splitting network. These modules can be implemented with application-specific integrated circuits (ASICs).

The signal after conditioning is sent to the acquisition board through a Sub-Miniature-A (SMA) interface for sampling. The acquisition board consists of two parts: ADC array and FPGA. The selected ADC (EV10AQ165, Teledyne E2V) is a double-channel 8-bit converter, with 2.5 GS/s for each subchannel. With the combination of two ADCs (four cores), a four-channel TIADC is set up with sampling rates of up to 10 GS/s. Two FPGAs (XC7K160T, Xilinx, Inc., Kintex-7 series) receive high-speed data stream from the corresponding ADC. To match the operation speed of FPGA, the high-speed serial data are converted to parallel in the ISERDES module. Finally, the data are sent to the processing board for skew error estimation. The communication is set up through a compact peripheral component interconnection (CPCI) bus.

Except for the phase tuning operated internal ADC, the other blocks of calibration are implemented in the processing board. Using logic resources in the master FPGA, the timing skew estimator realizes absolute value operation, average operation, adaptive engine and float point calculation. The estimator module calculates the mismatch error and its corresponding DCW. The adjustment element of DCW is sent to ADC by the SPI interface. When the estimation skew error converges, the obtained four-channel signals are combined to the final high-speed data stream. Finally, high-speed data are sent out through a peripheral component interconnection express (PCIe) bus to the industrial personal computer (AIMB-275, Advantech) for advanced operations.

It should be noted that the gain and offset mismatch error cannot be neglected, so the calibration method of these two mismatches is synchronized-processed with foreground techniques and also implemented in the master FPGA. But this is not within the scope of this article. Other digital signal processing (DSP) algorithms, such as waveform processing and digital interpolation, are implemented in this FPGA.

Besides, the processing board supports the clock system of the whole system. The four-phase sampling clocks are generated by the clock circuit PLL (LMK04806B, Texas Instruments), which supports multiple channel differential clock signals with a voltage controlled oscillator (VCO) frequency up to 2600 MHz. Except the four-channel sampling clock of 2500 MHz, three clocks of 312.5 MHz are generated as the work clock of FPGA. These clocks are sent to the specific components for normal operation.

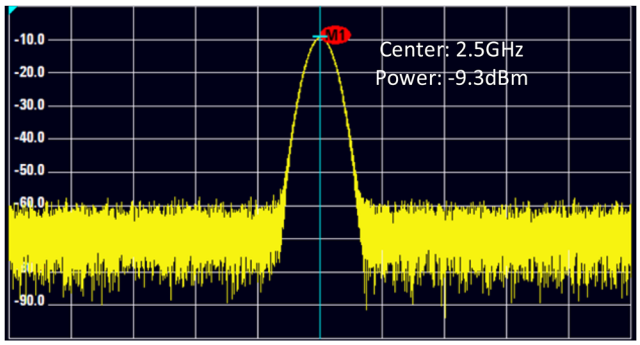

FIG. 9. Plot of the 2.5 GHz sampling clock signal in the frequency domain.

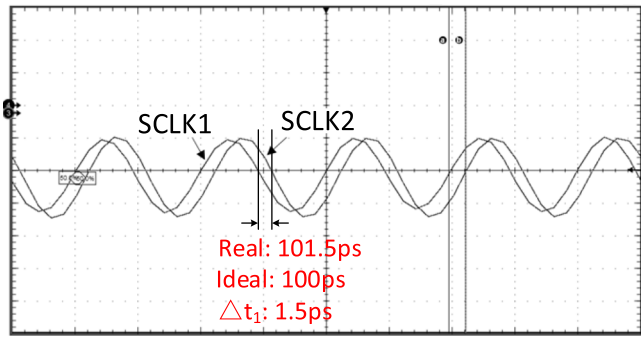

FIG. 10. Plot of the 2.5 GHz sampling clock signal in the time domain. The ideal timing delay between SCLK1 and SCLK2 is 100 ps, but the measured timing delay is 101.5 ps. The relative error is due to the timing skew error.

IV. EXPERIMENTAL RESULTS

Comprehensive functional and performance tests on the TIADC are performed on the testing and application platform, as shown in Fig. 8. Several measurement instruments and software integrated development environment (IDE) are used. The signal generator (SMB100A, Rohde & Schwarz) provides the test signal for sweep detection of the broadband acquisition system whose output signal has a frequency range of 9 kHz~6 GHz. A digital oscilloscope (MSO5404B, Tektronix) with four channels is the key signal measurement system for synchronization and hardware debugging. It has a −3 dB analog bandwidth of 2 GHz and maximum real-time sampling rate of 10 GS/s. Spectrum analysis of the SMA RF cable and 2.5 GHz sampling clock analysis are mainly performed by a spectrum analyzer (FSC6, Rohde & Schwarz) with the analysis frequency range of 9 kHz~6 GHz. A multimeter (UT60B, UNI-T) is mainly used for hardware debugging of the circuit boards and measurement of voltage, resistance, and impedance. In addition, Visual Studio 2017 (Microsoft) and Vivado 2015.2 (Xilinx) are used for software development and digital logic debugging analysis separately. Utilizing these tools, we have done two experiments, which fully verify the system's reliability and its performance. Tests below are performed using a sinusoid signal of 250 MHz as input.

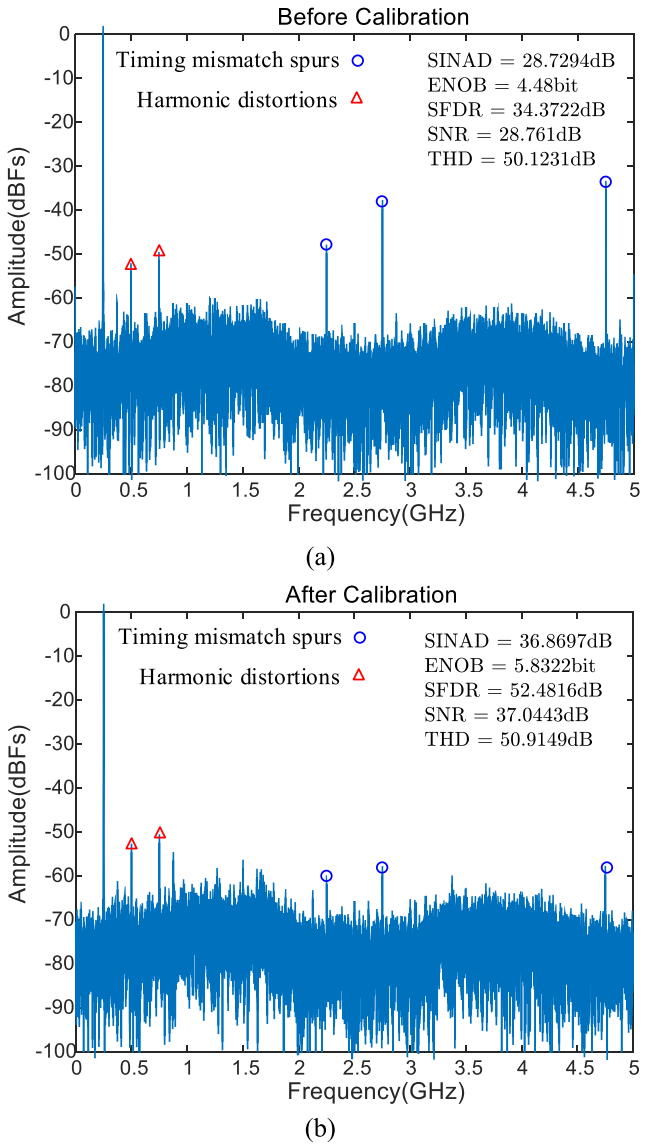

FIG. 11. (a) FFT plot of the input signal before calibration. Spectrums with a circle marker are caused by timing skew mismatch spurs. (b) FFT plot of the input signal after calibration. The dynamic parameters are calculated using the FFT result.

A. Clock

The quality of the sampling clock and the actual phase relationship are vital to the effective number of bits in the TIADC system. The 2.5 GHz sampling clock is tested by R&S's FSC6 spectrum analyzer, as shown in Fig. 9. The sampling clock signal frequency is 2.49 GHz, and the main lobe width greater than −55 dB is less than 15 MHz.

Ideal phases of the multichannel sampling clock have accurate offset from channel to channel. The clock from the processing board to the acquisition board clock input IO port is seriously affected by hardware factors. It is no longer the ideal phase difference, which eventually leads to an irregular sampling point instant. The real phase of the sampling clock needs to be tuned by the coarse adjustment of the PLL (step ~25 ps) or the fine adjustment of the ADC's own (~30 fs step) with an adjustment range of ~±15 ps to ensure the ideal phase difference between the multiple sampling clocks. SCLK1, SCLK2, SCLK3, and SCLK4 are the PLL output clocks of the processing board with phase differences of 100 ps. The phase difference between the sampling clocks is measured by

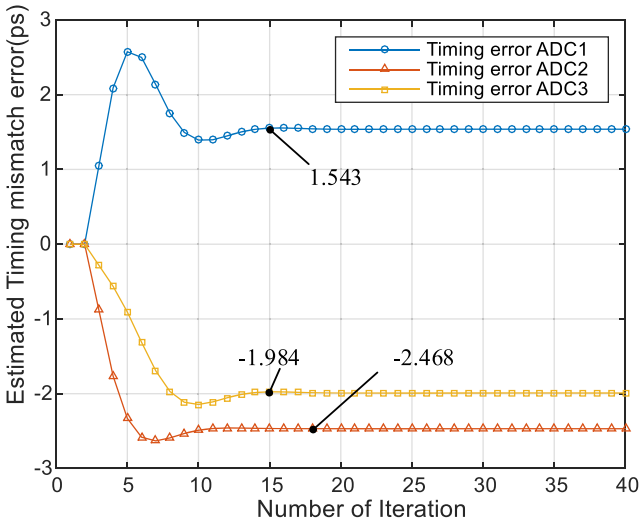

FIG. 12. Estimation of timing skew mismatch error versus different times of iteration. After fifteen cycles, the estimated value converges.

TABLE II. Complexity comparison.

Characteristics		Reference 20	This work
Computation complexity	Estimation criteria	$E(x_k[n]x_{k+1}[n])$	$E\left(\left\|x_k[n]-x_{ref1}[n]\right\| - \left\|x_k[n]-x_{ref2}[n]\right\|\right)$
	Number of additions	$(2M-3)NK$	$3(M-1)NK$
	Number of multiplications	$(2M-3)NK$	0
Time complexity	Number of calibration rounds	$M-1$	$\log_2 M-1$
	Iteration number of convergence	Not mentioned	15 ($M=4$)[a]

[a]This result is from Fig. 12.

Tektronix's MSO5404B digital oscilloscope. Figure 10 shows the phase relationship between SCLK1 and SCLK2. The SCLK2 has a time delay of 101.5 ps of SCLK1, which gives the measured time skew mismatch error of Δt_1 = 1.5 ps. The approximate timing skew in the other two channels can be measured with the same method. This experiment testifies that under proper clock configuration, the timing skew error is evitable in TIADC.

B. Spectrum

To testify the performance of TIADC, we used a signal of 250 MHz and analyzed the spectrum of the system output. The spectrum of the signal before calibration is illustrated in Fig. 11(a). Except the timing skew, the gain and offset mismatch are both unknown in advance. In this work, using the correction method described in Ref. 14, the gain and offset mismatch errors are corrected using the statistical characteristics of the samples' output. From the figure, some spurs can be seen outside the main bin. These spurs are caused by the timing skew mismatch error. Before applying the calibration technique, the amplitude of the timing mismatch spur is −49.85 dB, −34.37 dB, and −35.31 dB. Two spurs with the triangle marker are harmonic distortions from R&S's SMB 100A signal generator. The amplitudes of the second and third harmonics are measured at −52.48 dB and −54.61 dB, respectively. The SFDR is seriously affected by the mismatch error peaks; due to this influence, the SFDR is just 34.37 dB and ENOB is only 4.48 bit. The spectrum of the signal after calibration is depicted in Fig. 11(b). After calibration, the amplitude of timing mismatch spurs is suppressed to −59.71 dB or less. The SFDR is significantly improved to 52.48 dB, which is actually affected by the external factor. In addition, with the improvement of distortion the ENOB increases up to 5.83 bit. This experiment demonstrates a well calibration effect, which is directly proved by the indicators of SFDR and ENOB. Other dynamic performance indicators such as signal-to-noise and distortion (SINAD) ratio, signal-to-noise ratio (SNR), and total harmonic distortion (THD) are improved accordingly.

Meanwhile, we will analyze and discuss the estimation efficiency. Figure 12 illustrates the value of timing skew error versus number of iterations. After fifteen cycles, the estimation errors from three uncalibrated channels converge to 1.54 ps, −1.98 ps, and −2.46 ps separately. A positive value indicates that the actual sampling time is after the ideal sampling time, and a negative value is the opposite. This result is consistent with the measurement of SCLK but more accurate than the instrumentation measured result. After an accurate estimation, the timing skew mismatch error can be compensated correctly. Besides, the figure illustrates that the proposed algorithm converges with a low time consumption and has good robustness. Both of the low circuit complexity and low time complexity show great application values of the proposed calibration algorithm.

C. Comparison

An iterative method mentioned in Ref. 20 is similar to the proposed method. Both of these two methods use the iterative calibration technique and do not require auxiliary hardware for reference channel. However, the method in Ref. 20 uses a criterion of cross covariance. For an M channel TIADC ($M \geq 2$), the complexity of two methods is compared and listed in Table II, where N stands for the length of the sampled data and K denotes the number of iterations. The computation complexity is compared with the number of addition and multiplication. Time complexity depends on (i) the number of calibration rounds for all channels and (ii) the number of iterations for a single channel calibration. Based on the comparisons of these characteristics, it can be shown that the proposed technique has a high efficiency for application.

V. CONCLUSION

This article addresses the timing skew mismatch challenge in the TIADC system and presents a novel timing skew mismatch error calibration technique. In this work, the principle and details of the proposed calibration algorithm were described first. In addition, the algorithm was implemented by FPGA and an oscilloscope platform with a sampling rate of 10 GS/s was set up. For the first time, the technical details of the oscilloscope were described. We experimentally demonstrated the advantage of a calibration algorithm, which improved the performance of oscilloscope from the original SFDR of 34.37 dB to 52.48 dB and ENOB of 4.48 bit to 5.83 bit. Moreover, the complexity comparison of estimation shows that the proposed algorithm has advantages in terms of time and computation complexity in reality. Since the proposed

calibration algorithm has a significant improvement and high efficiency, it can be used in the TIADC system.

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REFERENCES

[1]J. Cao, D. Cui, A. Nazemi, T. He, G. Li, B. Catli, M. Khanpour, K. Hu, T. Ali, H. Zhang, H. Yu, B. Rhew, S. Sheng, Y. Shim, B. Zhang, and A. Momtaz, in Presented at the 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017.

[2]D. L. Lukas Kull, C. Menolfi, M. Braendli, P. Andrea Francese, T. Morf, M. Kossel, A. Cevrero, I. Ozkaya, and T. Toifl, in Presented at the 2018 IEEE International Solid-State Circuits Conference (ISSCC), 2018.

[3]R. Herrero, A. Carpeño, S. Esquembri, M. Ruiz, and E. Barrera, IEEE Trans. Nucl. Sci. **65**(2), 781–787 (2018).

[4]X. Hu, L. Zhao, C. Feng, W. Zheng, S. Liu, and Q. An, IEEE Trans. Nucl. Sci. **60**(6), 4588–4594 (2013).

[5]J. Liu and V. Mukundagiri, in Presented at the 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), 2013.

[6]Z. Hao, Y. Shi, and Z. Wang, in Presented at the IEEE Circuits and Systems International Conference on Testing and Diagnosis, 2009.

[7]C. Vogel, IEEE Trans. Instrum. Meas. **54**(1), 415–427 (2005).

[8]P. Lowenborg, H. Johansson, and L. Wanhammar, in Presented at the Circuits and Systems, 2001 Proceedings of the IEEE 2001 Midwest Symposium on Mwscas 2001, 2001.

[9]J. Li, S. Wu, Y. Liu, N. Ning, and Q. Yu, IEEE Trans. Circuits Syst. II **61**(7), 486–490 (2014).

[10]C. Wang and J. Wu, IEEE Trans. Circuits Syst. I **56**(6), 1102–1114 (2009).

[11]N. L. Dortz, J. Blanc, T. Simon, S. Verhaeren, E. Rouat, P. Urard, S. L. Tual, D. Goguet, C. Lelandais-Perrault, and P. Benabes, in Presented at the 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014.

[12]B. Xu and Y. Chiu, IEEE Trans. Circuits Syst. I **62**(5), 1306–1314 (2015).

[13]M. S. Dilmaghani and D. Asemani, in Presented at the 2017 Iranian Conference on Electrical Engineering (ICEE), 2017.

[14]L. Guo, S. Tian, and J. Jiang, Rev. Sci. Instrum. **86**, 034713 (2015).

[15]H. Johansson, IEEE J. Sel. Top. Signal Process. **3**(3), 384–396 (2009).

[16]J. Gao, W. Huang, W. Wei, L. Guo, H. Li, and P. Ye, in Presented at the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018.

[17]J. Song, S. Tian, and Y. Hu, IEEE Trans. Circuits Syst. I **66**(2), 655 (2019).

[18]J. Selva, IEEE Trans. Signal Process. **57**(1), 168–181 (2009).

[19]L. Guo, S. Tian, and Z. Wang, Metrol. Meas. Syst. **21**(3), 535–544 (2014).

[20]K. Yang, S. Tian, P. Ye, P. Zhang, and Y. Zheng, Math. Problems Eng. **2015**(6), 1–9.

[21]E2V, *Low Power QUAD 10-bit 1.25 Gsps ADC Operating up to 5 Gsps Quadruple Analog to Digital Converter* (EV10AQ190A Datasheet, 2013).