Numerical Simulations for In-Depth Analysis of Transmission Line Method Measurements for Photovoltaic Applications—The Influence of the p–n Junction

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For optimization of solar cell perfomance, the knowledge of the specific contact resistivity between grid finger and emitter is an important component. The contact resistivity is typically characterized by transmission line method (TLM) measurement directly on samples made from complete fabricated solar cells. Large contact spacing on solar cells leads to high measured resistances and thus high voltage drops along the emitter, measuring between several finger distances. This, in turn, imposes a strong load on the p–n junction and can lead to a parasitic current flow over the wafer base itself. The influence of this current flow on the TLM measurement evaluation for typical solar cell parameters is investigated. The 2D simulation of TLM measurements is used to derive handling instructions to improve the contact resistivity measurements. For typical solar cell TLM stripes with emitter sheet resistances of about $150\,\Omega\,\mathrm{sq}^{-1}$ and a reverse p–n junction characteristic similar to r_{shunt} in the range of $10\,\mathrm{k}\Omega\,\mathrm{cm}^2$, an influence of about 10% or higher ρ_{c} evaluation uncertainty is expected.

1. Introduction

Since the beginning of semiconductor research, the contact between metal and semiconductor plays a crucial role. Therefore, a lot of work was performed to investigate the physical understanding, which is directly correlated to an extensive measuring effort. Few test structures such as Cox and Strack,[1] linear transmission line method (TLM),[2–4] or circular TLM (CTLM)[5,6] were developed. In photovoltaic research, the linear TLM is extensively used to determine the contact resistivity between metal (e.g., silver or aluminum) and silicon or similar systems. Due to the silver H-grid pattern on solar cells, the linear TLM is simply applicable by solar cell slicing. The emitter is used as thin, in good approximation, 1D conductor which is electrically seperated

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from the wafer base by the p–n junction. Therefore, the system fulfills the principal requirements for TLM analysis.[7]

Several solar cell research groups studied the effect of different sample properties or measuring conditions on the contact resistivity. Guo et al. summarized the effects of sample geometry, e.g., stripe width and electrical properties such as edge shunting and nonuniform sheet resistance.[8] The influence of intermediate fingers and a thick sample was investigated by Müller[9] and Eidelloth and Brendel,[10] respectively. However, the influence of the p–n junction itself is poorly studied. Bystrova et al.[11] recognized a parasitic current flow into the wafer resulting in significant measurement discrepancies, but presented neither physical model nor measurement guidance to prevent the measurement from detrimental effect.

This work shows results of 2D FEM simulations of solar cell TLM test structures to gain a deeper understanding of the influence of the p–n junction properties, in this case shunt resistivity, on the results of TLM measurements and its evaluations, which leads to guidelines for measurement and evaluation that improve the measurement accuracy.

2. Simulation

To investigate a wide range of junction properties, the TLM measurements are simulated by 2D FEM model with the possibility to adjust the geometric and electrical parameters. The 2D COMSOL (COSMOL Multiphysics GmbH, Stockholm, Sweden)[12] domain consists of two contacts, with a distance corresponding to a multiple of the contact spacing d_{f} (see **Figure 1**a,b). Thus, we neglect intermediate fingers (see Figure 1b). Their possible influence can be found elsewhere.[8,9,13] Both contacts are connected to the emitter via contact resistivity ρ_{c}. The characteristics of the p–n junction between emitter and wafer, described by Equation (1), allow a current density j flowing in vertical direction across the junction.

$$j = -j_s\left[\exp\left(\frac{qV_{\mathrm{j}}}{nkT}\right) - 1\right] - \frac{V_{\mathrm{j}}}{r_{\mathrm{shunt}}} \tag{1}$$

where j_{s} is the saturation current density, V_{j} is the local voltage, q is the elementary electric charge, and k is the Boltzmann constant.
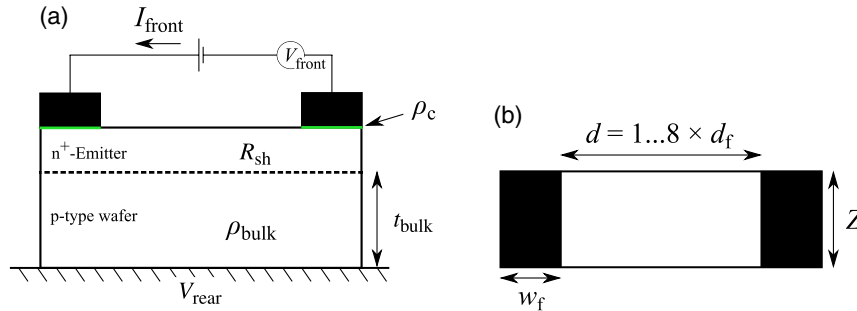
Figure 1. Schematic representation of a) sample cross section and b) top view of the simulated device.

The temperature T is set to 300 K and the ideality factor n is set to 1 and held constant during simulation. The reverse characteristic of the p–n junction is crucial as this provides the isolation between emitter and wafer base, which is governed by the shunt resistivity r_{shunt}. The r_{shunt} of the full cell leads to a linear correlation between the applied reverse voltage and the current flowing across the junction. The transfer of this property to the TLM sample is achieved by sample preparation with shallow grooves created with pulsed laser scribing and breaking at these trenches to avoid additional edge shunting. Otherwise the TLM measurement would be falsified, which is described in detail by Guo et al.[8]

Nevertheless, extending the measurement setup by a conductive chuck would enable experimentally the IV measurement directly for each TLM sample using the front contact probes and the chuck. The determined dark IV curve could be used to determine the junction characteristics for a sample in detail.

A defined current I_{front} was injected via one contact and extracted via the second (Figure 1a), where the rear side of the wafer is on a floating potential. The COMSOL AC/DC module is used in stationary mode for solving the partial differential equations of the drift current, by minimizing the overall power loss within the domain, revealing the current flow pattern and local voltage distribution. The resistance of the domain is calculated by Ohm's law using the voltage difference V_{front} between the contact and the given current. Varying only the distance between the contacts results in an $R(d)$ plot, which corresponds to the implementation in real measuring systems for ρ_c determination.

The input parameters are selected on the basis of industrial cz-PERC solar cells given by Fell et al,[14] where the contact width w_f is 60 μm, d_f is 1.483 mm, ρ_c is 2.7 mΩ cm, bulk resistivity ρ_{bulk} is 1.5 Ω cm, wafer thickness t_{bulk} of 170 μm, and a j_s of 1×10^{-14} A cm^{-2} is a typical saturation current density for highly efficient solar cells and is kept constant during simulation. A sample width Z of 3 mm was used to reduce the influence of the lateral finger conductivity on ρ_c evaluation.[8]

The sample characteristic is varied by the emitter sheet resistance R_{sh} from 100 to 250 Ω sq^{-1}, and the reverse characteristic of the p–n junction is varied by the shunt resistivity r_{shunt} in a range from 1 to 1000 kΩ cm^2. The measurement conditions are modified by measuring current I_{front}, which is changed from 1 to 1000 mA (see **Table 1**).

The evaluation of contact resistivity ρ_c is conducted according to the classical TLM model by fitting $R(d)$ for up to $8 \times d_f$, using Equation (2).[7] At the same time, the emitter sheet resistance R_{sh} of the sample is also determined, where L_T is the transfer length

Table 1. Overview of the varied input parameters and their variation range used for COMSOL simulations.

Symbol	Value	Description
R_{sh}	100, 150, 200, 250 Ω sq^{-1}	Emitter sheet resistance
r_{shunt}	1.1000 kΩ cm^2	Shunt resistivity
I_{front}	1.1000 mA	Measuring current

and d is the contact distance, which is a multiple of the finger distance d_f. The fit performed by OriginPro (OriginLab Corporation, Northampton, MA, USA)[15] also determines the standard error for the derived fit parameter which is plotted as error bars for ρ_c and R_{sh}.

$$R = \frac{R_{sh}d}{Z} + 2\frac{\rho_c}{L_T Z}\coth\left(\frac{w_f}{L_T}\right)$$
$$\text{with} \quad L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$

(2)

Furthermore, this analytical equation is used to calculate reference resistance R_a for a certain distance, which is unaffected by finite p–n junction isolation. The relative deviation R_{rel} of the simulated resistance R_s is calculated as $(R_s/R_a) - 1$ and used as parameter to rate the influence of the current flowing across the p–n junction.

3. Results

Exemplary results of simulated TLM measurements are shown in **Figure 2**. There is an excellent agreement between simulation and analytical model when the shunt resistivity tends toward infinity, resulting in $R_{rel} = 0$ and ρ_c of 2.7 mΩ cm^2 which corresponds exactly to the input parameter. The effect of a reduced r_{shunt} on the TLM analysis is visible especially for high contact spacing in Figure 2. For decreasing r_{shunt}, the simulated resistance deviates more strongly from the analytical calculation with perfect junction isolation. This is visible by R_{rel} of up to -5%, as shown in the upper graph of Figure 2. Due to the nonlinear increase, the discrepancy for long contact distance distorts the evaluation by a decreasing R_{sh} and thus increasing virtually the ρ_c. Therefore, the TLM evaluation is affected by the p–n junction properties.

The influence of r_{shunt}, R_{sh}, and I_{front} on evaluated ρ_c and R_{sh} is shown in **Figure 3**a,b, including the results from Figure 2.
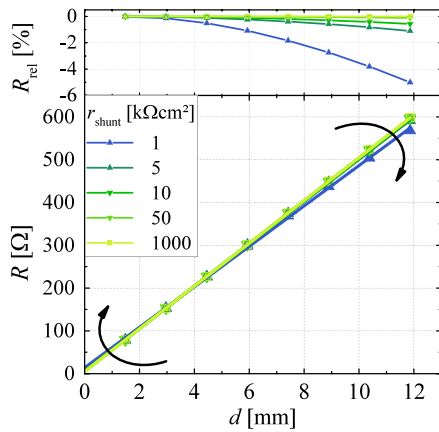
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Figure 2. $R(d)$ graph for simulated TLM measurement with $R_{sh} = 150\,\Omega\,\text{sq}^{-1}$ and measuring current I_{front} of 10 mA, p–n junction characteristic varied by r_{shunt} from 1 to 1000 kΩ cm². The relative deviation of the simulated resistance from the ideal, analytical one ($r_{shunt} \rightarrow \infty$) is shown in the upper part of the graph.
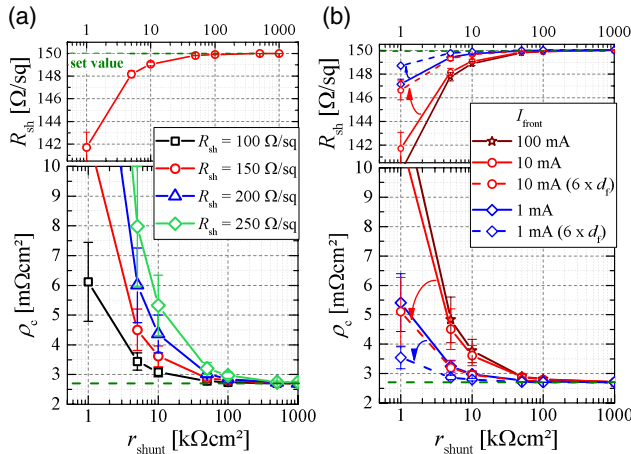

Figure 3. Influence of a) R_{sh} using a I_{front} of 10 mA and b) I_{front} for a constant R_{sh} of 150 Ω sq^{-1} on calculated R_{sh} and ρ_c depending on the r_{shunt}. Evaluation includes contact distance from 1 to $8 \times d_f$. The dashed green line represents the set values for ρ_c and R_{sh} in the simulation.

The perfect agreement between input value and ρ_c determined from the simulated TLM vanishes for $r_{shunt} \leq 100\,\text{k}\Omega\,\text{cm}^2$, which is also visible in decreasing R_{sh} in Figure 3a. For R_{sh} of 150 Ω sq^{-1} and r_{shunt} of 10 kΩ cm², the ρ_c increases to 3.6 mΩ cm², which corresponds to a 33% discrepancy from input value. In addition, the standard error for the ρ_c evaluation increases, represented by the error bars, to ±0.4 mΩ cm². This is due to the deviation of $R(d)$ from linear behavior (see Figure 2).

Similar effects are visible for the variation of the used measuring current I_{front} in Figure 3b, which shows the evaluation of ρ_c versus r_{shunt} for R_{sh} of 150 Ω sq^{-1}. With increasing I_{front}, both ρ_c and its standard error increase and deviate more strongly from the input value. Taking into account typical solar cell parameters, e.g., r_{shunt} of 50 kΩ cm² and R_{sh} of 150 Ω sq^{-1}, the determined ρ_c is 10% higher than the real one, when nine contact pairs are analyzed with I_{front} of 10 mA. This effect increases further for

reduced r_{shunt} or increased I_{front}. Due to the increased resistance deviation at high finger distances, the evaluation with a reduced maximum contact distance allows a more accurate determination of ρ_c. This is shown in Figure 3b for 1 and 10 mA, where the maximum distance is reduced from 8 to $6 \times d_f$. For the widely used I_{front} of 10 mA, the limitation of the distance leads to a ρ_c reduction from 3.7 to 3 m cm² at r_{shunt} of 10 kΩ cm². This can be further improved by the usage of only 1 mA leading to 2.8 mΩ cm² and therefore a deviation of less than 4% from the simulation input value.

4. Discussion

The strong dependence of the results evaluated by TLM method can be explained by a parasitic current flow over the p–n junction into the wafer base. This is, of course, mainly determined by its reverse characteristic properties. However, the extent to which this influences the measurement result depends on the sample properties and measurement conditions.

The important parameter is the voltage drop between the measured contacts, which determines the reverse load. This is determined by the R_{sh}, I_{front}, and other sample properties such as the maximum contact distance and sample width. The local voltage at the p–n junction is well visible in **Figure 4**; one side is at the local potential of the emitter (V_{pn-e}), linear decreasing from high to low terminal, whereas on the base side of the p–n junction (V_{pn-w}) a low potential in the range of 0.3–0.6 V is formed. This voltage is established due to the formation of a state of equilibrium of the current flow across the p–n junction.

At the beginning of the measurement, the wafer is at a potential of 0 V, and thus well below the potential of the emitter. Therefore, a certain current flows into the wafer base via the p–n junction. As this must be extracted by the second contact, a voltage above 0 V is established, depending on the forward and reverse characteristic
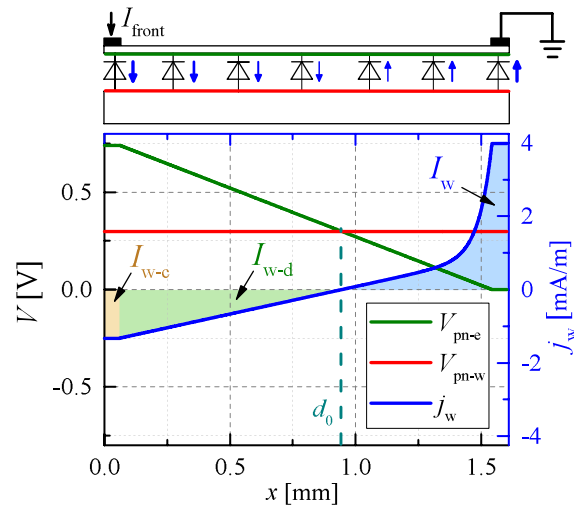

Figure 4. Local voltages on both sides of the p–n junction and the vertical current flow j_w across this junction (different contributions marked as filled areas) determined by COMSOL simulation with $r_{shunt} = 10$ kΩ cm², $R_{sh} = 150$ Ω sq^{-1}, $I_{front} = 10$ mA for $d = 1 \times d_f$. Schematic TLM domain on top of the graph illustrates the position of the displayed voltages and current path over the p–n junction.

of the p–n junction to achieve a current flow out of the wafer. The forward characteristics dominated by j_s is of minor influence as the diode is highly conductive under this condition.

The current density j_w flows along the entire distance between the contacts across the p–n junction into the wafer, as long as the local voltage on the emitter side (V_{pn-e}) is greater than on the wafer side (V_{pn-w}). When V_{pn-e} equals V_{pn-w}, we have a change in current direction through the p–n junction. This crossing point is indicated by the length d_0. This effectively results in parallel connection of emitter and wafer, and thus reduces the resistance between the two contacts, correspondingly reducing the effective R_{sh}. From Figure 4, the share of this parasitic current I_w flowing trough the wafer can be calculated, which in this case is 0.67 µA and thus 0.007% of the I_{front}. As the contact distances increase to $8 \times d_f$, the voltage drop and the area of the p–n junction between the contact fingers increase, resulting in a high parasitic current I_w of 90 µA, which is 0.9% of I_{front}. Accordingly, the current flow pattern moves away from the ideal 1D current flow through the emitter and deteriorates the measurement results by a relative change of the resistance by −0.6%, which results in a fitted ρ_c of 3 mΩ cm^2.

The current I_w is separated in first-order approximation into two components (see Figure 4). On the one hand, the current I_{w-c} flows under the first contact into the wafer, and on the other hand the current I_{w-d} flows between the contacts across the p–n junction into the wafer base until $V_{pn-e} \leq V_{pn-w}$ (see Equation (3)).

$$I_w = I_{w-c} + I_{w-d} \tag{3}$$

Under assumption of low contact resistivity, the potential below the contact is almost constant and I_{w-c} can be calculated by Equation (4). The relevant parameter is ΔV_{pn}, which is defined as the maximum voltage difference between local voltage at the emitter (V_{pn-e} at high terminal) and mean voltage at wafer side ($\bar{V}_{pn-w}$).

$$I_{w-c} = \frac{Z \Delta V_{pn}}{r_{shunt}} w_f \tag{4}$$

The current I_{w-d} in the intermediate region can be calculated taken into account the diode reverse characteristic, which is fully shunt determined, and a linear voltage decline between the contacts, which is determined by the emitter sheet resistance and sample width. The decisive factors are ΔV_{pn} and the position when both potentials cancel each other out (see d_0 in Figure 4) and the current reversal takes place. Thus, I_{w-d} is described by Equation (5) and (6).

$$I_{w-d} = \int_0^{d_0} \left(1 - \frac{x}{d_0}\right) \frac{Z \Delta V_{pn}}{r_{shunt}} dx$$
$$= \left(x - \frac{x^2}{2d_0}\right) \frac{Z \Delta V_{pn}}{r_{shunt}} \tag{5}$$

$$d_0 = \left(1 - \frac{\bar{V}_{pn-w}}{V_{pn-e}}\right) d \tag{6}$$

The analytical calculation of I_w leads to a perfect agreement with the values determined by COMSOL Multiphysics simulation (**Figure 5**).
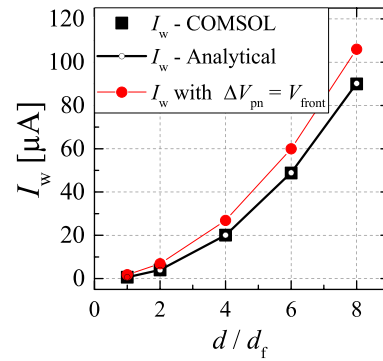

Figure 5. Comparison of I_w determined directly by COMSOL and analytical calculations considering 3-terminal measurement or 2-terminal measurement with simplification $\Delta V_{pn} = V_{front}$ for $r_{shunt} = 10 \, k\Omega \, cm^2$, $R_{sh} = 150 \, \Omega \, sq^{-1}$, and $I_{front} = 10 \, mA$.

However, the exact voltages at the p–n junction cannot be measured, and thus the measurement of the rear side potential of the wafer via a 3-terminal measurement (see Figure 1) is required. Our useful assumption of a sufficiently low ρ_c, $\max(V_{pn-e}) \approx V_{front}$ and $\bar{V}_{pn-w} \approx V_{rear}$, enables an estimation of I_w directly from the measurement. However, if the additional measurement is impossible, the rough simplification $\bar{V}_{pn-w} = 0$ and $V_{pn-e} = V_{front}$ can be used to get a very coarse estimation of the parasitic current flow through the base. The estimation forms an upper limit, as shown in Figure 5.

As discussed earlier, the parasitic current flow through the wafer influences the measured resistance. Thus, the decisive parameter is the amount of measuring current which flows through the wafer base, calculated as I_w/I_{front}. Analyzing the COMSOL simulations, a direct correlation between the determined ρ_c and I_w/I_{front} ratio is elaborated, which is shown as relative difference of ρ_c from its set value against I_w/I_{front} ratio, depending on the maximal used contact distance and r_{shunt} in **Figure 6**.

The simulated TLM measurements in Figure 3 with varied r_{shunt} and I_{front} are evaluated with different maximum contact distance (4 to $8 \times d_f$), where the maximal contact distance
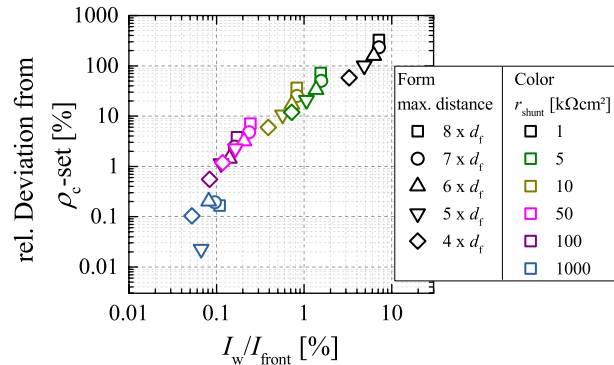

Figure 6. Plot of the relative deviation of the evaluated ρ_c from set value depending on maximal I_w/I_{front} of each simulated TLM measurement with varied r_{shunt}, R_{sh} of $150 \, \Omega \, sq^{-1}$, I_{front} of 10 mA, evaluated for maximum contact distance from 4 to $8 \times d_f$.

describes the largest contact distance used for the evaluation, as shown in Figure 3b. Independent from the used I_{front} and maximal contact distance, with decreasing r_{shunt} the current I_w rises and therefore the evaluation error. Even if the ratio I_w/I_{front} is not the only determining factor for a good measurement evaluation, it still allows an initial evaluation quality guess. The effect of reduced I_{front} and maximum contact distance to $4 \times d_f$ leads to the lowest relative ρ_c deviation within each r_{shunt} group, showing impressively the effect of the used evaluation conditions.

To ensure a ρ_c evaluation accuracy of less than 10%, the I_w/I_{front} should be $\leq 0.1\%$, which can be determined by measuring the voltage of the wafer rear and using Equation (4) and (5). Nevertheless, for a typical TLM sample, with a reverse characteristic is similar to a known r_{shunt} in the range of $10\,k\Omega\,cm^2$ or below, the measurement should be set up carefully, using a low measuring current in the range of $1\,mA$ and a maximum contact distance of $5 \times d_f$.

5. Conclusion

Numerical simulation of TLM measurements are set up taking into account the properties of the p–n junction. It enabled us to improve the understanding of parasitic current flow through the wafer base during TLM measurements. Thus, we consider the reverse and forward IV characteristic of the diode for TLM measurement evaluation.

We showed that the decisive factor is the voltage drop between the contacts, which should be kept as low as possible to reduce the parasitic current flow through the wafer base. This can mainly be influenced by the used sample geometry and measuring current. If this is not considered, a measurement evaluation error of 10% can occur for typical sample geometry and measurement parameters, which is caused by the parasitic current flow through the wafer. Evaluating samples with low r_{shunt} or larger contact spacing can increase the measurement uncertainty further. For typical solar cell TLM stripes with $R_{sh} \approx 150\,\Omega\,sq^{-1}$ and a reverse p–n junction characteristic similar to r_{shunt} in the range of $10\,k\Omega\,cm^2$, an influence of about 10% or higher ρ_c evaluation uncertainty is expected.

It was also shown that it is possible to calculate the parasitic current flow through the wafer by measuring the potential of the rear side of the wafer. Thus, it is possible to estimate the measuring error and to optimize the measuring conditions to achieve the most accurate measurement.

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