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Annealing of Degraded npn-Transistors—Mechanisms and Modeling

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***Abstract*— We report on the annealing of degraded npn-transistors, which includes a new model describing the decrease of base current during annealing. We found that two mechanisms are responsible for annealing: the recombination of charges and the bonding of hydrogen atoms on interface traps. Furthermore, we show that a heating of the whole device and a forward biasing of the emitter-base-diode activate these annealing mechanisms. This biasing deactivates the interface traps by recombination with a part of the streaming charge and results in a local increase in temperature, caused by the current. Both local and global heating yield an additional thermal generation of charges and an increasing diffusivity of hydrogen atoms. Consequently, an additional deactivation and passivation of interface traps is detected.**

I. Introduction

THE knowledge of device degradation effects becomes more and more important with further miniaturization of bipolar transistors. We investigated high performance self-aligned npn-transistors, realized in a 0.8 μm-technology, with a cutoff frequency $f_T = 25$ GHz, a current gain β of 100 and trench isolation [1]. It is well known, that the increase of base current with increasing emitter-base stress time is a hot-carrier effect [2]: electrons are accelerated by the applied field in the reverse mode. They can gain so much energy, that they may damage the Si/SiO_2 interface after scattering into this interface. The resulting interface traps are generation/recombination centers, and are the main reason for the increase of base current [3] (Fig. 1). In the worst case it results in a short circuit.

On the other hand, degraded junctions can be annealed by temperature and current (Fig. 1). Thus the knowledge and precise modeling of both effects: degradation and annealing is of vital importance for proper device design, V_{BE0} specification and real-world simulation of circuit malfunction due to degradation and respective annealing. Moreover, the physical background of the annealing mechanisms helps to understand degradation effects and vice versa.

In the following first the theoretical background is outlined, then experimental results are given and finally a comparison between measurement and simulation is done which shows the good accuracy of the models presented here.

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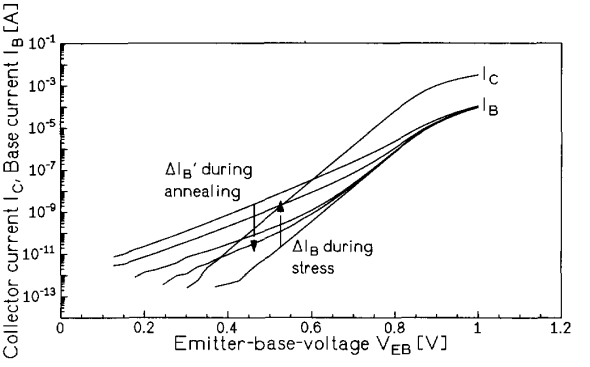

Fig. 1. Degradation and annealing of bipolar transistors described by the increase and decrease of base current. ΔI_B represents qualitatively the change of base current during stress, and $\Delta I_B'$ the change of base current during annealing.

To the authors' knowledge, this is the first annealing model of base current including the annealing mechanisms and their activation possibilities.

II. Annealing Model

The base current is made up of the diffusion current and the Shockley–Read–Hall generation-recombination current. We model the decrease of base current $\Delta I_B'$, which is only a generation-recombination current [4] and which is defined as the difference of the base current after stress and the base current after a certain annealing time.

A. Physical Mechanisms

Tang *et al.* [4] described, that after annealing of a stressed transistor the leakage current, follows the same temporal trend during the second stress as if the healing had not occurred. Therefore, we believe the annealing is the reciprocal process of damage with reciprocal mechanisms, the deactivation of interface traps caused by charge carrier trapping [5] and the passivation of interface traps by the bonding of hydrogen atoms [6].

As the Shockley–Read–Hall current is proportional to the density of interface traps [7], the decrease of the base current is proportional to the density of the annealed interface traps. Let $N_{tot1,2}$ be the total density of interface traps that can be annealed by charge carrier trapping (index 1) and bonding with hydrogen atoms (index 2) under certain annealing conditions with time constants τ_{An1} and τ_{An2}, respectively, the rate

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equations for the two densities $N_{1,2}(t_{An})$ of annealed interface traps are

$$\frac{dN_{1,2}(t_{An})}{dt_{An}} = \frac{N_{tot,1,2} - N_{1,2}(t_{An})}{\tau_{An1,2}} \quad (1)$$

with t_{An} as the annealing time. The solution is

$$N_{1,2}(t_{An}) = N_{tot1,2}\left(1 - e^{-\frac{t_{An}}{\tau_{An1,2}}}\right). \quad (2)$$

In consideration of the Shockley–Read–Hall theory [7] and (2) we get two different generation-recombination currents, which constitute as a sum the temporal behavior of the whole process as following:

$$\Delta I'_B(t_{An}) = C_{SRH}\left(N_{tot1}\left(1 - e^{-\frac{t_{An}}{\tau_{An1}}}\right) + N_{tot2}\left(1 - e^{\frac{-t_{An}}{\tau_{An2}}}\right)\right) \quad (3)$$

where C_{SRH} is completely described by the SRH theory.

B. Activation

So far we described the possible annealing mechanisms. The next question is, how these processes are initialized. Two different conditions are possible, which effects are contained in the sums N_{tot1} and N_{tot2}, respectively. In our model we get five terms arranged as following:

$$N_{tot1} = \sum_{i=1}^{3} N_{1i} \text{ and } N_{tot2} = \sum_{j=1}^{2} N_{2j} \quad (4)$$

1) Annealing by Global Increase of Temperature: To describe the effect of the global temperature the following formula is used:

$$N_{1,21} = B_{1,21}e^{-\frac{E_{1,2}}{k_B T}}. \quad (5)$$

It resembles a generally accepted law for thermal activated processes [8] with the Boltzmann constant, k_B, and the global device temperature, T. In our case a global heating of the device initializes the illustrated events, in which E_1 is the activation energy for deactivating interface traps and E_2 the energy for diffusion of hydrogen atoms.

2) Annealing by Forward Biasing the Emitter-Base-Diode: By forward biasing the emitter-base-diode a part of the current I_{An} flows underneath the SiO_2-spacer. The energy of the streaming charges is too low to surmount the energy barrier Si/SiO_2, which is nearly 3.1 eV for electrons and 4.8 eV for holes [9].

Nonetheless, some of these charge carriers flow directly to states, which are located at the Si/SiO_2-boundary, and deactivate these interface traps. Equivalent to the decharging of an R-C circuit, the temporal behavior of this deactivation process can be written as

$$N_{13} = B_{13}\left(1 - e^{-\frac{I_{An}t_{An}}{Q_{13}}}\right) \quad (6)$$

with $Q_{13} = C \cdot U_R$.

In addition, optical phonon scattering, which is the main scattering mechanism in silicon [10], is caused by the same current. A local heating is the result. This increases the deactivation of interface traps by additional generation of charges (index 12) and the passivation of interface traps by an increased hydrogen diffusion (index 22).

Their activation process can be considered as follows:

$$\frac{d(N_{12,22})}{dQ_B} = C_{12,22}f(N_{12,22}) - D_{12,22}N_{12,22} \quad (7)$$

$f(N_{12,22})$ is a function which describes the traps annealing rate taking existing deactivated and passivated traps into account. Q_B is the streaming charge. We assume

$$f(N_{12,22}) = N_{12,22}^{-m,n} \quad (8)$$

with m, n = const. This equation describes the fact, that it will become more difficult to deactivate or passivate interface traps, when the level of deactivation or passivation is higher. We get the following solutions:

$$N_{13,22}(Q_B) = B_{13,22}\left(1 - e^{\frac{-Q_B}{Q_{13,22}}}\right)^{\frac{1}{1+m,n}} \quad (9)$$

where $B_{12,22} = D_{12,22}/C_{12,22}$, $Q_{12,22} = 1/((1 + m, n)\ D_{12,22})$ and $Q_B = I_{An} \cdot t_{An}$.

As it will be shown within Section III, no temperature dependence of the mechanism described here can be detected. Thus it is not incorporated within the formulas given here.

C. Total Equation for Annealing

The following equation describes the whole annealing event and yields a consistent and noncontradictory mode of the whole process:

$$\Delta I'_B = C_{SRH}\left(\left(B_{11}e^{-\frac{E_1}{k_B T}} + B_{12}\left(1 - e^{-\frac{I_{An}t_{An}}{Q_{12}}}\right)^{\frac{1}{1+m}} + B_{13}\left(1 - e^{-\frac{I_{An}t_{An}}{Q_{13}}}\right)\right)\left(1 - e^{-\frac{t_{An}}{\tau_{An1}}}\right) + \left(B_{21}e^{-\frac{E_2}{k_B T}} + B_{22}\left(1 - e^{-\frac{I_{An}t_{An}}{Q_{22}}}\right)^{\frac{1}{1+n}}\right) \cdot \left(1 - e^{-\frac{t_{An}}{\tau_{An2}}}\right)\right). \quad (10)$$

The whole model is sketched in Fig. 2 in its schematic form. Due to the specific form of (10) it is not possible of course to determine the quantities C_{SRH} and B_{ij} separately but only in their multiplied form $C_{SRH} \cdot B_{ij}$.

III. Experiments and Results

For verification of the model we present data of transistors with an effective area of $10 \times 10\ \mu m^2$ and $20 \times 20\ \mu m^2$. The evaluation sequence was as follows: For the investigation of the temporal behavior during annealing, the bipolar transistors were stressed by reverse biasing the emitter-base junction with $V_R = 5.7$ V for 1000 seconds. To characterize the degree of degradation, we measured base and collector current I_B and I_C, respectively, at a selected forward bias V_{EB} before and after stress. As each forward biasing of the emitter-base junction is an annealing event in itself, the base-emitter voltage is kept constant at 0.7 V to keep this effect neglectable. Due

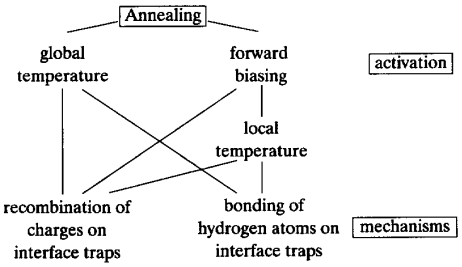

Fig. 2. Annealing processes for degraded *npn*-transistors. The annealing mechanisms, the recombination of charges, just as the bonding of hydrogen atoms on interface traps, are activated by a global temperature and a forward biasing of the emitter-base-diode. The forward biasing results in a direct recombination of charges and an increase of the local temperature.

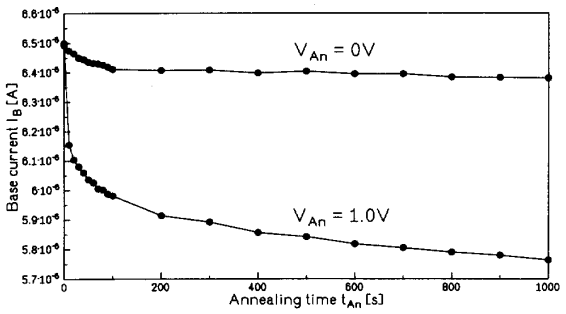

Fig. 3. Temporal behavior of base current I_B during annealing. The two cases present global thermal annealing (T_{An} = 298 K) and additional forward bias annealing (V_{An} = 1.0 V and T_{An} = 298 K) measured at V_{EB} = 0.7 V and a temperature T_M = 298 K.

to this measurement strategy the quantities $C_{SRH} \cdot B_{ij}$ only extracted for this specific V_{BE} value of 0.7 V. In this case, we get a stress effect of I_B/I_{B0} at V_{EB} = 0.7 V with a standard deviation of 4%. I_{B0} represents the base current before stress.

Finally, the annealing of the damaged transistor was done in intervals of 10 s for a total time of 10 000 s. Measuring at a temperature T_M = 298 K, the base current characterizes the level of annealing after each period. The only way to get correct results is to set the temperature during the measurement equal to that of annealing, because the heating and cooling needs a lot of time and would accordingly give rise to false results.

As an example, Fig. 3 shows a typical behavior during annealing of npn-transistors (emitter area 10 × 10 μm^2) detected at a forward bias V_{EB} = 0.7 V.

The base current decreases because of a global thermal activation (T_{An} = 298 K) from $I_B(t_{An} = 0\text{ s}) = 6.492 \cdot 10^{-6}$ A to $I_B(t_{An} = 1000\text{ s}) = 6.381 \cdot 10^{-6}$ A, i.e., a 1.7% decrease. By forward biasing the emitter-base-diode additionally (V_{An} = 1.0 V) the base current decreases from $I_B(t_{An} = 0\text{ s}) = 6.500 \cdot 10^{-6}$ A to $I_B(t_{An} = 1000\text{ s}) = 5.764 \cdot 10^{-6}$ A, i.e., a 11.3% decrease.

A. Investigations at Different Temperatures

We can gain important information about annealing mechanisms from the discussion of the time and temperature behavior of annealing events.

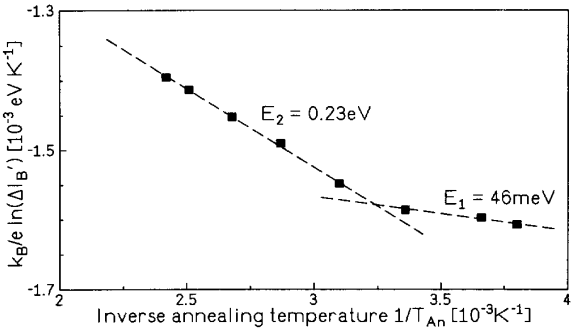

Fig. 4. The representation of the measurements after a global thermal annealing. The activation energies are E_1 = 46 meV and E_2 = 0.23 eV. Stress conditions: t = 1000 s, V_R = 5.7 V; Annealing conditions: t_{An} = 600 s, V_{An} = 0 V. Measuring conditions: V_{EB} = 0.6 V.

The temperature dependence of the annealing behavior was investigated by different stress conditions, variations in stress time t = 60–30 000 s and stress voltages V_R = 4.7–5.7 V. Fig. 4 represents a typical behavior in an Arrhenius plot; in this case an emitter area of 20 × 20 μm^2 is presented. The base current decreases from $I_B(t_{An} = 0\text{ s}) = 8.401 \cdot 10^{-7}$ A to $I_B(t_{An} = 600\text{ s}, T_{An} = 263\text{ K}) = 8.321 \cdot 10^{-7}$ A and $I_B(t_{An} = 600\text{ s}, T_{An} = 413\text{ K}) = 7.455 \cdot 10^{-7}$ A. Corresponding to the developed annealing model we extract activation energies of E_1 = 10–80 meV and E_2 = 0.22–0.27 eV.

The small activation energy E_1 cannot be associated with atomic diffusion, but with a deactivation process, where charge carriers are trapped at interface states: Itsumi reports on a similar value of 23 meV for electron trapping in thin films of thermal oxide [5].

The value of E_2 is in good agreement with the activation energy of hydrogen diffusion in silicon at temperatures between T = 70–400 K (= 0.3 eV [6]).

On the base of this reasoning (Fig. 4) we can predict, that the degradation, represented by the value of ΔI_B, will be completely annealed after 600 s with a temperature T_{An} = 630 K.

Besides this difference in activation energy these two processes are characterized by two different time constants: τ_{An1} = 40 s and τ_{An2} = 1500 s (Fig. 5) where the first can be identified with fast electron trapping and the second with a low hydrogen diffusion. The good agreement between model and measurement is notable, the products $C_{SRC} \cdot B_{11}$ and $C_{SRH} \cdot B_{21}$ were determined by Lagrange interpolation.

B. Investigations on the Combination of Temperature Treatment and Forward Biasing

When the emitter-base-diode operates additionally in forward mode, we can see an increased annealing rate (Fig. 3) [11]. To understand this effect in detail, transistors were annealed with different forward biases, annealing times, and temperatures.

Fig. 6 presents the $\Delta I_B'$-V_{An}-characteristic for two examples (emitter area 20 × 20 μm^2), where t_{An} = 600 s and

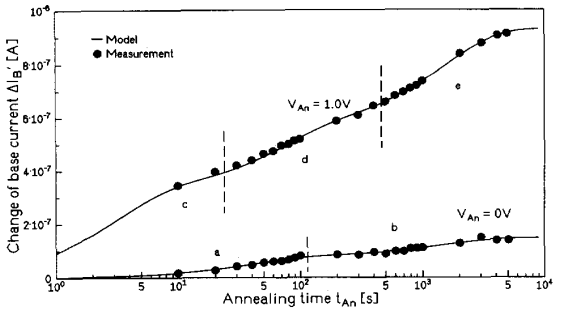

Fig. 5. Decrease of base current $\Delta I'_B$ with increasing annealing time with and without applied forward bias $V_{\mathrm{An}}(T_{\mathrm{An}} = 298$ K)–using the data of Fig. 3. In case of $V_{\mathrm{An}} = 0$ V we notice two parts, marked with a and b and characterized with $\tau_{\mathrm{An1}} = 40$ s and $\tau_{\mathrm{An2}} = 1500$ s, respectively. The second curve ($V_{\mathrm{An}} = 1.0$ V) is separated into three cases, whereas c and d give rise to an effective lifetime $\tau_{\mathrm{An1}} = 3$ s and e to $\tau_{\mathrm{An2}} = 1500$ s.

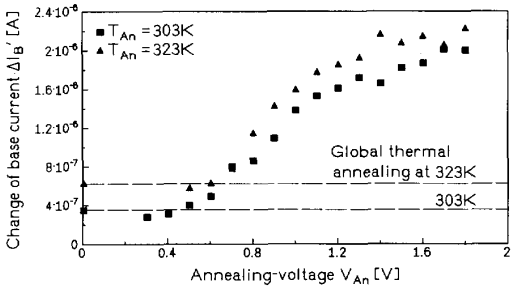

Fig. 6. Annealing of transistors with applied forward bias. The base current becomes smaller with increasing annealing-voltage V_{An}in forward mode, simultaneous it results in a decrease of base current with $\Delta I'_B$. The broken lines show the level of global thermal annealing at selected annealing temperatures T_{An}. Measurement in forward mode was done at $T_M = 298$ K and $V_{\mathrm{EB}} = 0.7$ V after an annealing time $t_{\mathrm{An}} = 600$ s.

$T_{\mathrm{An}} = 303$ K and $T_{\mathrm{An}} = 323$ K, respectively, were chosen. To recognize the effect of biasing, the level of the pure thermal effect was marked with the broken lines. We can see the effect of different temperatures, which yield a higher degree of annealing with increasing temperature. It is remarkable, that the effect caused by forward biasing predominates as against the global thermal annealing process for V_{An} greater than 0.6 V. That means that for a circuit relevant forward biasing of roundabout 0.9 V V_{EB} the annealing due to forward biasing is 130% larger than that of 323 K. The value of $\Delta I'_B$ increases with higher forward bias until a saturation point is reached. To be sure that this saturation is not caused by those degradation effects as discovered by J. A. del Alamo *et al.* [12] and R. A. Wachnik *et al.* [13], we checked the degradation of a virgin device by forward biasing the emitter-base diode. These investigations showed no damages, and thus no relevance of the findings of [12] and [13] for our investigations.

To get more information on the basic physics, we tried to separate the effect of global thermal annealing from that of annealing caused by forward biasing. The subtraction of the change of the base current caused by global thermal annealing and the value resulting from the additional forward bias annealing shows the characteristic of Fig. 7. We conclude,

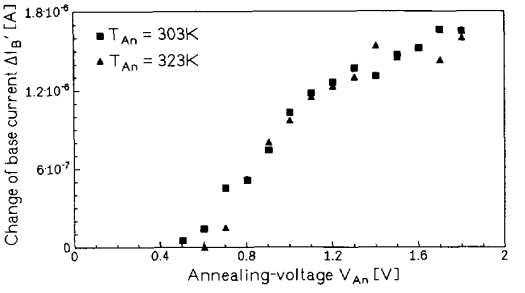

Fig. 7. $\Delta I'_B - V_{\mathrm{An}}$-characteristic at pure forward bias annealing, by subtraction of the global thermal annealing from global thermal/forward bias annealing ($T_M = 298$ K, $V_{\mathrm{EB}} = 0.7$ V, $t_{\mathrm{An}} = 600$ s).

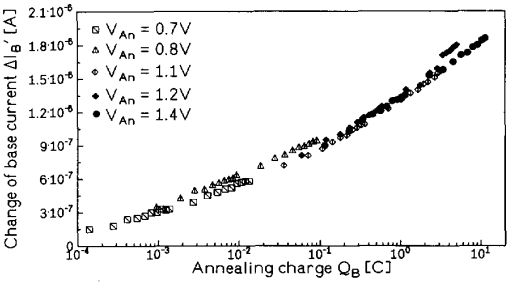

Fig. 8. Change of base current $\Delta I'_B$, caused by the streaming annealing charge Q_B. The forward bias annealing depends only on the charge, and is no function of the charge carrier energy. Annealing conditions: $T_{\mathrm{An}} = 298$ K, $t_{\mathrm{An}} = 600$ s. Measured at $T_M = 298$ K and $V_{\mathrm{EB}} = 0.7$ V. Emitter area of 20×20 μm^2.

that the total annealing is a sum of global thermal annealing and forward bias annealing, because both curves (Fig. 7), freed from changes of the base current caused by a global thermally activated process, lead to the same results. This is confirmed by comparing $\Delta I'_B(T = 323$ K, $V_{\mathrm{An}} = 0) - \Delta I'_B(T = 303$ K, $V_{\mathrm{An}} = 0) = 2.4 \cdot 10^{-7}$ A, averaged over 10 samples, with $\Delta I'_B(T = 323$ K, $V_{\mathrm{An}}) - \Delta I'_B(T = 303$ K, $V_{\mathrm{An}}) = 2.32 \cdot 10^{-7}$ A averaged over 14 samples at different V_{An} values ranging from 0.6 V to 1.8 V, such that we can state that we have verified the considerations of the model, that these two activation processes are additive, at least within the temperature range investigated. Nonetheless we cannot rule out a small, but neglectable temperature dependence.

The next step is to find the reason for the forward bias annealing. To check the effect of the streaming charge, we integrate the current I_{An} overtime t_{An} during annealing and get the streaming charge Q_B. The $\Delta I'_B - Q_B$-characteristic of Fig. 8 describes a single continued curve despite the different forward biases. There is no energy dependence, such that the amount of the charge carriers plays the major role.

To test the influence of Q_B on the complete process, we first compare the activation energies of global thermal annealing and the combined global thermal and forward bias annealing. As there are no differences, we conclude that the mechanisms are the same. Comparing the time dependence of the annealing process however, we recognize three different processes in

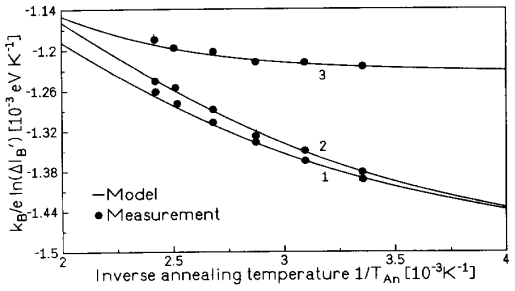

Fig. 9. Comparison model/measurement for transistors with emitter area of $10 \times 10\ \mu m^2$ in an Arrhenius plot. While the cases 1 and 2 show the effects of global thermal annealing at $t_{An} = 600$ s and $t_{An} = 1000$ s, respectively, case 3 describes annealing at $t_{An} = 600$ s and an additional forward mode with $V_{An} = 1.0$ V and $I_{An} = 4.5 \cdot 10^{-4}$ A, respectively.

Fig. 5 (case $V_{An} = 1.0$ V) marked by c, d, and e. The characterization by Lagrange interpolation of the respective permits the following conclusions:

As τ_{An2} (time constant for hydrogen passivation) is constant with respect for a sole temperature annealing and the number of annealing mechanisms does not change, the difference of $\Delta I'_B$ due to an additional forward bias on the passivation of interface traps has to be an increase in the diffusivity of the hydrogen atoms. Because the diffusivity is a function of the temperature, the charge carriers have to increase the local temperature by optical phonon scattering [7]. This effect is characterized by $Q_{22} = 2.8 \cdot 10^{-2}$ C (marked with e). τ_{An1} (time constant for electron deactivation) decreases from 40 s in case of global thermal annealing to 3 s by additional forward bias annealing. Thus so far τ_{An1} is just an effective lifetime which has to be caused by more than one process. Fig. 5 indicates the existence of 2 processes (region c and d). For region d the value of $Q_{12} = 2.9 \cdot 10^{-2}$ C is thus equal to $Q_{22} = 2.8 \cdot 10^{-2}$ C. Thus the increase of the local temperature leads to a higher generation of charges. In contrast, the direct recombination of charges is verified by the low value of Q_{13} (marked with c). Naturally, this direct recombination of charges on interface traps exhibits a very low critical value of $Q_{13} = 1 \cdot 10^{-5}$ C in comparison to Q_{12} and Q_{22}. Thus the change in τ_{An1} is caused by this mechanism.

In conclusion all assumptions of the model are confirmed by the experiments. The parameters of the model, characterized by the measurements, are listed in Table I. An example of the high level of agreement of model and measurement is shown in Fig. 9. It has be noted, that E_i, τ_{Ani}, m and n are generally valid quantities, whereas C_{SRH}, B_{ij}, Q_{ij} have to be determined for each different device, each stress condition and operation point V_{EB}.

IV. Conclusion

A new model for the decrease of base current during annealing of degraded high performance npn-transistors is presented. It is shown that the deactivation of interface traps by the recombination of charges, as well as the passivation of interface traps by the bonding with hydrogen atoms is responsible for the decrease of base current. The underlying mechanisms are initiated by global thermal activation or by forward biasing of the emitter-base diode. While a part of the streaming charge recombines directly at the interface traps, the flowing current causes a local heating. Both local and global heating increase the thermal generation of charges and the diffusivity of the hydrogen atoms and result in an increased deactivation and passivation of interface traps.

All experiments verify the model. On the base of this model we get basic information on the underlying physics and it is easy to implement it into a circuit simulator, what allows for simulating real world stress and annealing events for npn-bipolar transistors.

TABLE I
PARAMETERS OF THE ANNEALING MODEL

C_{SRH}[A]	B_{11}	B_{12}	B_{13}
$4.5 \cdot 10^{-7}$	1.0	0.52	0.54
B_{21}	B_{22}	m	n
1231.1	0.68	0.01	0.03
E_1 [meV]	E_2 [eV]	τ_{An1} [s]	τ_{An2} [s]
46	0.23	40;3	1500
Q_{12}[C]	Q_{13}[C]	Q_{22}[C]	
$2.9 \cdot 10^{-2}$	$1 \cdot 10^{-5}$	$2.8 \cdot 10^{-2}$	

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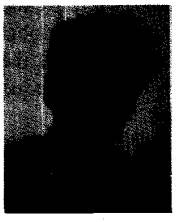
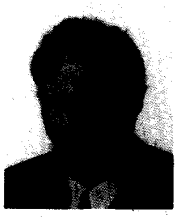
Helmut Wurzer was born in Mallersdorf, Germany, in 1965. He received the Dipl. Phys. degree from the Technische Universität München, in 1992. He is currently working toward the Dr. Ing. degree in electrotechnical engineering at the Universität der Bundeswehr München.

In 1991 he joined the Research and Development division of Siemens AG to make his Diplom thesis. With Siemens, he has worked in the BIPOLAR/BICMOS group to investigate bipolar transistors for degradation phenomena. In September 1992, he joined the Universität der Bundeswehr München. His current interest is the research and development of new sensor principles.



Reinhard Mahnkopf was born in Germany on June 5, 1960. In 1985 he received the Dipl. Ing. degree, and in 1990 the Ph.D. degree in electrical engineering from the Technische Universität Berlin.

In his Ph.D. thesis he worked on the characterization of hot carrier damages in submicron MOSFET's. Since joining the Research Laboratories of Siemens AG, München, in 1990, he has been involved in the research and development of high performance bipolar transistors.



Helmut Klose (M'91) was born in 1957 and received the Dipl. Ing. and Dr. Ing. degrees in electrotechnical engineering in 1984 and 1986, respectively.

He was engaged in the development of image reversal resists, of RF-bipolar modeling and measurement techniques, of soft codes for process- and device-simulation. Since 1986 he headed the BICMOS technology development project and since 1988 he is heading the BIPOLAR/BICMOS group at the corporate Research and Development. Starting in 1992 these activities were supplemented by sensor/actuator and 3D-integration techniques. He has authored and coauthored more than 40 papers and has 20 patents.

Dr. Klose is member of the GME.