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METALLURGICAL PROPERTIES AND ELECTRICAL CHARACTERISTICS OF PALLADIUM SILICIDE–SILICON CONTACTS

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Abstract—The fabrication, metallurgical properties, and electrical characteristics of palladium silicide (Pd_2Si) contacts to *n*-type Si have been investigated. Pd_2Si/Si contacts are similar in electrical and metallurgical behavior to PtSi/Si contacts, but can be fabricated at much lower temperatures. Pd was found to react readily with Si at 200°C to form a silicide phase which was identified as Pd_2Si from X-ray diffraction analysis. The electrical resistivity of the silicide is $40 \times 10^{-6}\ \Omega$ cm as determined from sheet resistivity measurements. The barrier height at the Pd_2Si/Si interface was determined from differential capacitance measurements to be 0.745 ± 0.015 V. Current-voltage measurements and activation energy analysis gave barrier heights within this same range. Contact resistance measurements were made on contacts to Si surfaces with phosphorus doping levels of 2×10^{20}/cm^3. Resistance values obtained are comparable to both theoretical predictions and measurements reported on PtSi and Al contacts to Si.

Résumé—On a étudié la fabrication, les propriétés métallurgiques et les caractéristiques électriques de contacts en silicure de palladium (Pd_2Si) contre du Si du type *n*. Les contacts Pd_2Si/Si ont un comportement électrique et métallurgique semblable aux contacts PtSi/Si, mais peuvent être fabriqués à des températures bien plus basses. On a trouvé que le Pd réagissait facilement avec le Si à 200°C pour former la phase silicure identifiée comme Pd_2Si par analyse de diffraction de rayons X. La résistivité électrique du silicure, déterminée par mesure de résistivité de feuilles est de $40 \times 10^{-6}\ \Omega$ cm. La hauteur de barrière à l'interface Pd_2Si/Si déterminée par mesures de capacité différentielle, est de $0{,}745 \pm 0{,}015$ V. Des mesures de résistance de contact ont été faites sur des contacts avec les surfaces Si en utilisant des niveaux de doping au phosphore de 2×10^{20}/cm^3. Les valeurs de résistance obtenues sont comparables aux prévisions théoriques aussi bien qu'aux mesures rapportées sur les contacts PtSi et Al avec le Si.

Zusammenfassung—Herstellungsverfahren, metallurgische Eigenschaften und elektrische Kenndaten von Palladiumsilizidkontakten auf *n*-Typ Silizium wurden untersucht. Die elektrischen und metallurgischen Eigenschaften dieser Kontakte sind ähnlich denen bei Verwendung von Platinsilizid. Sie können aber bei wesentlich niedrigeren Temperaturen erzeugt werden. Es wurde festgestellt, daß Pd schon bei 200°C mit Si reagiert und ein Silizid bildet, das durch Röntgenbeugungsanalyse als PdSi identifiziert werden konnte. Der spezifische elektrische Widerstand dieses Silizids wurde aus dem Schichtwiderstand zu $40 \cdot 10^{-6}\ \Omega$ cm bestimmt. Die elektrische Schottky-Barriere an der Phasengrenze wurde aus der differentiellen Kapazität ($0.745 \pm 0{,}015$) V ermittelt. Strom-Spannungsmessungen und eine Analyse der Aktivierungsenergie liefern Barrierenwerte im gleichen Bereich. Messungen des Kontaktwiderstandes wurden bei Siliziumoberflächen durchgeführt mit einer Dotierung von $2 \cdot 10^{20}$ Phosphoratomen/cm^3. Die Widerstandswerte sind vergleichbar mit theoretischen Werten und mit Meßwerten bei PtSi und Al auf Silizium.

NOTATION

A	area (cm^2)
Å	angstrom units (10^{-8} cm)
A^*	Richardson constant (amp/cm^2/°K^2)
C	capacitance (F)
D	diameter (cm)
E_m	maximum electric field (V/cm)
I_F	forward bias current (A)
I_R	reverse bias current (A)
J	current density (A/cm^2)
J_T	tunneling current density (A/cm^2)
k	Boltzman's constant
m^*	effective mass (g)
m_0	free electron effective mass (g)
N_D	donor doping density (atoms/cm^3)

q charge on electron (C)
R_c contact resistance (Ω)
R_I interface resistance (Ω)
R_{Si} spreading resistance in Si (Ω)
R_T zero bias tunneling resistance (Ω)
T absolute temperature (°K)
V bias voltage (V)
V_B barrier height (V)
V_F Fermi level relative to conduction band (negative when in band gap) (V)
V_I intercept voltage of differential capacitance plot (V)
V_R reverse bias voltage (V)
ΔV_B barrier lowering (V)
ϵ_r relative dielectric constant
ϵ_s dielectric constant of Si (C/V-cm)
ρ electrical resistivity (Ω-cm)
ρ_s electrical sheet resistivity (Ω/square)

1. INTRODUCTION

ALUMINUM and platinum silicide (PtSi) have become the most widely used small area metallic contacts to silicon[1, 2]. However the fabrication of these contacts involves a number of problems. Aluminum dissolves a considerable amount of Si at typical processing temperatures of 400–550°C, making its use on devices with shallow junctions or close tolerances undesirable[3, 4]. PtSi contacts suffer from a number of processing difficulties associated with the Pt. Because of its high melting temperature, Pt must be deposited using electron beam evaporation or sputtering, thereby endangering the threshold voltage stability of insulated gate field effect transistors[5]. Pt is reacted with Si to form PtSi at high temperatures, typically 600°C[6]. Removal of the unreacted Pt is accomplished with aqua regia[6]—an etchant that is incompatible with photoresist and corrosive to many other materials.

Palladium silicide (Pd_2Si) offers a useful alternative to Al and PtSi as a contact material. Pd_2Si/Si contacts are similar in electrical and metallurgical behavior to PtSi/Si contacts, but can be fabricated at a much lower temperature. In addition there are a number of other process related advantages associated with the use of Pd. These are identified in Sections 2 and 6.

The idea of using palladium silicide contacts to Si is not new[7]. However little information is available in the literature about them. In this paper the preparation and behavior of Pd_2Si contacts to n-type Si will be described. The results of experiments to identify the composition of the silicide and determine its electrical resistivity will be presented. The results of contact resistance measurements on ohmic contacts and of current-voltage, capacitance-voltage, and current-temperature measurements to determine the height of the barrier at the Pd_2Si/Si interface will be discussed.

2. CONTACT PREPARATION

Contacts were made to ⟨111⟩ oriented phosphorus doped Si surfaces through openings in a thermally grown SiO_2 layer. The openings were chemically etched using standard photolithographic techniques. Contact resistance measurements were made on contacts formed by evaporating Pd from a tungsten boat onto chemically cleaned Si surfaces. However, in order to eliminate the influence on the barrier height measurements of the SiO_2 and chemical residues present on the silicon surface, the contact regions were ion-etch cleaned *in situ* in order to remove these contaminants along with 100–200 Å of Si.* The ion etching was performed with 90 V argon ions immediately before the sputter deposition of the Pd contact metal. These processes were carried out in a sorption roughed, ion and sublimation pumped vacuum system (Varian VI-221) which was backfilled with 99.999 per cent pure Argon to a pressure of 60 milli-Torr and sealed off. Prior to backfilling with Argon, the system was evacuated to $2–4 \times 10^{-9}$ Torr.

During deposition of the Pd, the Si wafer was heated to 200°C. At this temperature the Pd deposited in the exposed contact regions reacted to form palladium silicide. (The silicide penetrated deeper into the Si than any region of damage associated with the ion etching.) For Pd depositions of thickness greater than ~200 Å, the silicide is uniform, rougher in texture, and darker in appearance than the unreacted Pd (cf. Fig. 1). Because of the darker appearance of the Pd_2Si, poorly opened contact windows are easily discernable. The unreacted Pd was etched away with an aqueous solution of $KI + I_2$, an etchant which does not attack Pd_2Si. Where expanded metal contacts were required for the measurements reported below, a subsequent deposition of Al or Ag was used.

*Barrier heights obtained from measurements on contacts to chemically cleaned surfaces were similar in value to those obtained from *in situ* cleaned contacts, but the spread in values was much greater.

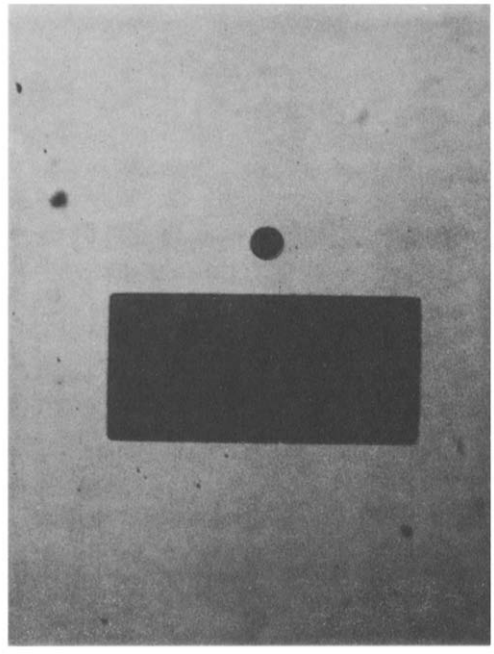

Fig. 1. Pd_2Si in contact openings against a contrasting field of unreacted Pd. (mag. 170×)

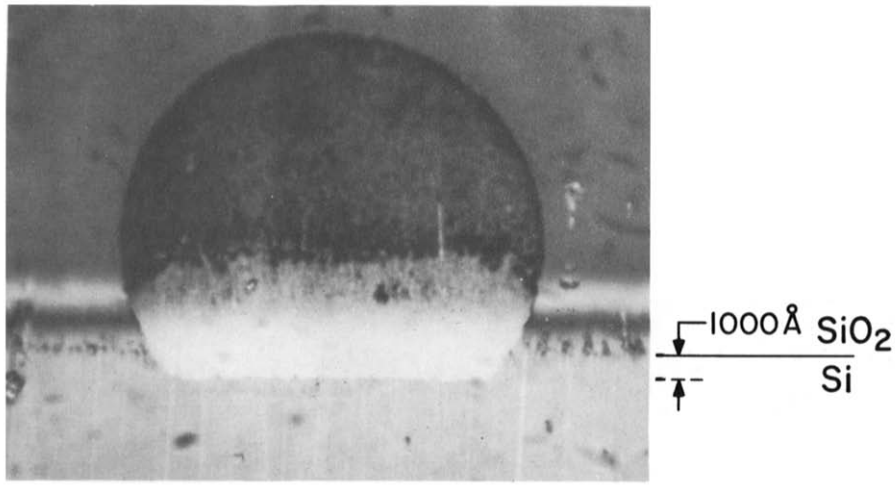

Fig. 2. Beveled section through Pd_2Si/Si contact showing 1000 Å penetration of silicide into Si. Photo taken at 755X. Bevel angle −1.1°. Silicide formed from 1000 Å Pd film at 250°C.

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3. PROPERTIES OF Pd_2Si

The palladium silicide was identified using a glancing angle Seeman–Bohlin X-ray diffractometer. The diffraction pattern of a 500Å Pd film reacted with Si included all the ASTM file lines of reduced intensity greater than 30 for Pd_2Si. No other phase could be identified. Whether or not there is a small amount of PdSi phase present at the silicide–Si interface is not certain. It would not have been observed if it were present in an amount corresponding to a layer less than 50Å in thickness.

Angle lapped sections were made through contacts that were deposited on wafers held at 250°C. The Pd_2Si/Si interface lies below the original Si surface by an amount approximately equal to the thickness of the Pd deposit (cf. Fig. 2). The interface is flat on the scale of the metal thickness. No difference was observed on sections through contacts which were heat treated to 500°C for 20 min (in Argon) after deposition of the Pd. However, heat treatment to 700°C appeared to embrittle the silicide and useful sections could no longer be obtained.

The electrical resistivity of Pd_2Si was determined using a technique similar to that used for measuring diffusion sheet resistivity. Pd_2Si was formed in a long, narrow rectangular contact-opening on 1 Ω-cm n-type Si. A four probe resistance measurement could then be made because the potential barrier at the silicide to Si interface confines the current flow to the Pd_2Si. The resistivity may be determined (to a first order) as accurately as the thickness of the Pd_2Si layer is known. The value obtained was 40×10^{-6} Ω-cm.

4. BARRIER HEIGHT MEASUREMENTS

One of the fundamental parameters which determines the current transport across a metal/semiconductor interface is the height of the potential barrier at the interface. The present understanding of a metal/semiconductor interface is not complete enough to allow prediction of the barrier height which will result when a particular metal and semiconductor are joined. However, it can be determined experimentally in several ways[8]. The barrier height, V_B, at the Pd_2Si/Si interface was determined from differential capacitance and current-voltage measurements, and activation energy analysis. All of the measurements were made on 0.010 in. dia. contacts to 1 Ω-cm phosphorous doped Si.

The diode capacitance, C, was measured as a function of the bias voltage, V, with a Boonton 75D capacitance bridge. Representative data are shown in Fig. 3 for two diodes on the same wafer. The difference between the two sets of data is typical of the spread observed on a given wafer.

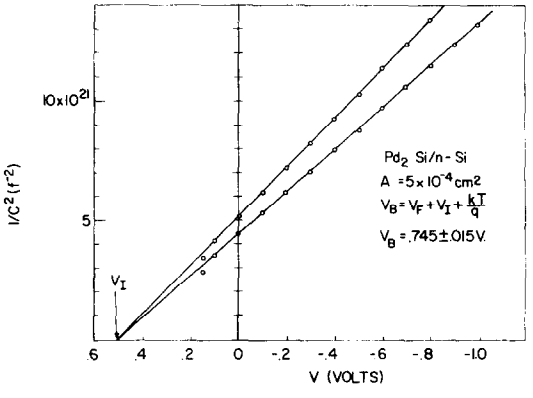

Fig. 3. Capacitance–voltage data for reverse biased Pd_2Si/Si diodes.

Values of the intercept voltage V_I and the slope $[d(1/C^2)/dV]$ are obtained from a computer calculated best straight line fit to the data using a least mean square deviation criterion. V_B is calculated from the relation[9]

$$V_B = V_F + V_I + \frac{kT}{q} \tag{1}$$

where the Fermi level, V_F, is calculated using the doping density N_D, obtained from the slope of the capacitance data. T, k, and q are respectively the absolute temperature, Boltzmann's constant, and the magnitude of the charge on the electron. The value of V_B obtained is $0.745 \pm 0.15V$. The uncertainty indicated is the spread in the V_I values obtained in measurements on diodes on five wafers prepared at different times, but in similar fashion.

The forward bias current-voltage behavior was measured on some of the same diodes. Typical data are shown in Fig. 4. For the doping density used, the dominant current flow mechanism is thermionic emission over the barrier[10, 11]. The observed dependence of the current density J on the applied voltage V agrees with the thermionic emission theory for which

$$J = J_s[e^{qV/nkT} - 1]. \tag{2}$$

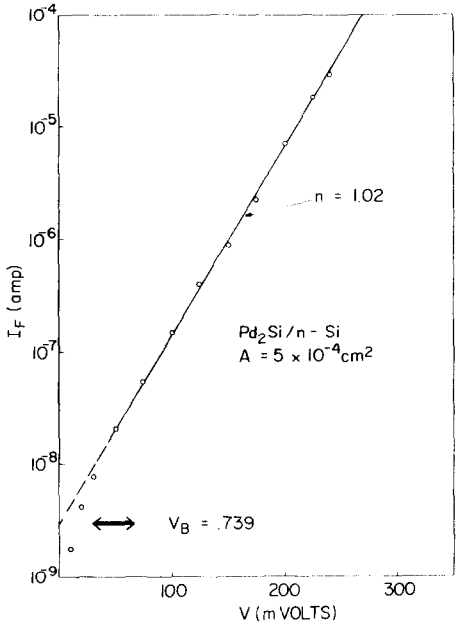

Fig. 4. Forward bias current–voltage characteristic for typical Pd_2Si/Si diodes.

A value of $n = 1.02$ was obtained. The barrier height can be calculated from the saturation current density, J_s, given by [12]

$$J_s = A^* T^2 e^{-(q/kT)(V_B - \Delta V_B)} \tag{3}$$

where A^* is the Richardson constant. The barrier lowering, ΔV_B, due to the image force is related to E_m, the maximum electric field in the junction by [13]

$$\Delta V_B = \left[\frac{qE_m}{4\pi\epsilon_s}\right]^{1/2} \tag{4}$$

where

$$E_m = \left[\frac{2qN_D}{\epsilon_s}(V_I - V)\right]^{1/2} \tag{5}$$

and ϵ_s is the dielectric constant of Si. For $N_D = 4 \times 10^{15}/cm^3$ and forward bias conditions, ΔV_B is small and can be neglected. Thus V_B can be calculated from equation 3, using the value of J_s determined experimentally from the straight line extrapolation of I_F to $V = 0$ (cf. Fig. 4). Using $A^* = 112$ amps/cm²/°K² [14] the value of V_B obtained was 0.739 V, in good agreement with the value obtained from the capacitance data.

The barrier height can also be obtained from the temperature dependence of the current, i.e. from an activation energy analysis. For $V > 0{\cdot}1$ V, equations 2 and 3 can be combined to obtain:

$$\ln\left(\frac{J}{T^2}\right) \simeq \ln A^* - \frac{q}{k}(V_B - V)\cdot\frac{1}{T} \tag{6}$$

Thus V_B can be obtained from the slope of $\ln(J/T^2)$ vs. $1/T$ plot for which V has been held constant. Such an activation energy plot for a typical Pd_2Si/Si diode is shown in Fig. 5. The value of V_B obtained from a least mean square deviation straight line fit to the data is 0·753 V, in good agreement with the C–V and J–V results.

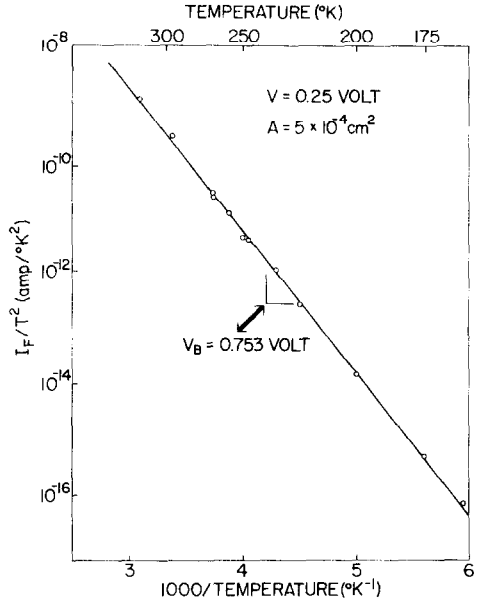

Fig. 5. Activation energy plot for forward biased Pd_2Si/Si diode.

Although the barrier lowering (equation 4) is small at low biases for the doping level used in these experiments, its effect can be seen at high reverse bias. To examine the barrier lowering in more detail, the reverse bias current-voltage characteristics of similar diodes were measured. For these experiments the diodes were fabricated with p–n junction guard rings to eliminate the

influence of leakage at the perimeter[6]. Typical data are shown in Fig. 6. The observed current exceeded that to be expected from image force lowering alone, as indicated by the dotted curve. A similar excess current has been observed for PtSi/Si diodes also[14], where it was interpreted as being the result of an additional barrier lowering (caused by a dipole layer at the interface) which is linearly proportional to E_m. Such an interpretation leads to the following expression for the barrier lowering:

$$\Delta V_B = \left[\frac{qE_m}{4\pi\epsilon_s}\right]^{1/2} + CE_m. \tag{7}$$

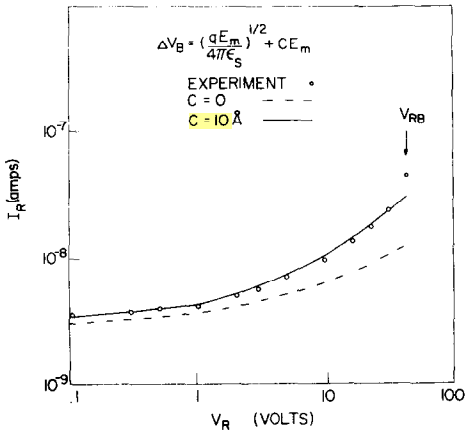

Fig. 6. Reverse bias current–voltage characteristic for Pd_2Si/Si diode with p–n junction guard ring. Theory for image force lowering of barrier height -----. Theory for additional barrier lowering proportional to E_m ————.

The reverse I–V data is accurately described using equation 7 together with equations 2, 3 and 5 as shown by the solid curve in Fig. 6. It should be noted that a number of other interface phenomena [15] have been described in the literature which would result in similar behavior. Hence the cause of the excess current is not clear at this point.

5. CONTACT RESISTANCE MEASUREMENTS

Contact resistance measurements were made on contacts to heavily doped Si surfaces. A 0·1 Ω-cm, n-type Si wafer was given a blanket diffusion to obtain a surface doping level of $\sim 2\times10^{20}$ phosphorus atoms/cm^3. Contacts were then made through openings in a thermally grown SiO_2 layer.

The four probe resistance measurement technique used is indicated in the inset in Fig. 7. One of the current probes was connected to a 0.001 in. contact on the Si surface and the other to the back of the wafer. One terminal of a high impedance voltmeter was also connected to the 0.001 in. contact by a separate lead. The other voltmeter terminal was connected to the adjacent potential probe contact which has a much larger area. The equipotential which terminates at this contact follows a contour which lies some distance into the Si below the Pd_2Si/Si interface. Consequently $R_c (R_c \equiv V/I)$ includes a certain amount of semiconductor bulk resistance as well as the actual interface resistance, R_I of the 0.001 in. contact. That is,

$$R_c = R_I + R_{Si} \tag{8}$$

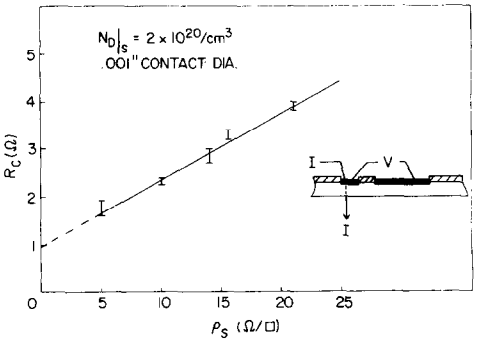

Fig. 7. Measured resistance (V/I) as a function of the sheet resistance of the blanket diffusion given to Si wafer. Measurement method shown in insert.

In order to determine the magnitude of R_{Si} and to permit separation of R_I from it, measurements were made on contacts to wafers which had received initial diffusions of increasing depth, but the same surface doping level. The measured resistances are plotted in Fig. 7 as a function of the sheet resistivity, ρ_s, of the diffusion. The observed linear dependence of R_c on ρ_s is a consequence of the fact that the current flow close to the contact (between the potential probes) is primarily lateral, i.e. it remains close to the surface in the low resistivity diffused region. For diffusions deeper than the range used in the measurements, the current flow would acquire a significant downward

component close to the contact, ultimately reaching the distribution for a contact to a uniformly doped wafer as ρ_s becomes very small. As a result of this redistribution of current flow, measured values of R_c for small ρ_s would be below the dotted extrapolation shown in Fig. 7. Thus an upper bound on R_I can be obtained using the linearly extrapolated intercept, $R_s|_{\rho_s \to 0}$:

$$R_{I\max} = R_c|_{\rho_s \to 0} - R_{u\mathrm{Si}}, \tag{9}$$

where $R_{u\mathrm{Si}}$ is the spreading resistance of a contact to a wafer that is uniformly doped to the level of the surface concentration. The value of $R_{u\mathrm{Si}}$ can be calculated using the results of Holm who has shown that [16]

$$\frac{\rho}{\pi D} < R_{u\mathrm{Si}} < \frac{\rho}{2D} \simeq 0.1\,\Omega$$

where ρ is the resistivity of the material and D the diameter of the contact. Thus $R_{I\max}$ is 0.7 Ω. Scaled to the area of the contact, this resistance corresponds to $4 \times 10^{-6}\,\Omega\text{-cm}^2$, assuming a uniform current density over the contact area. This upper bound is already comparable to values reported for PtSi contacts to Si with the same surface doping level [17, 18]. However, it appears that these data also include some Si resistance.

In the absence of additional sources of resistance, R_I is governed primarily by tunneling of electrons through the potential barrier at the metal/semiconductor interface. As this mechanism sets a lower bound on R_I, it is of interest to know by how much the theoretically predicted tunnel resistance lies below $R_{I\max}$. Padovani and Stratton [11, 19] have calculated the tunneling current density J_T for a parabolic metal/semiconductor potential barrier using the WKB approximation. For small forward biases where $0 < V < V_F$,

$$J_T = \frac{A^*}{(C_{1F}kT)^2} e^{-b_{1F}} \left[\frac{\pi C_{1F} kT}{\sin(\pi C_{1F} kT)} (1 - e^{-C_{1F}V}) - C_{1F} V e^{-C_{1F}V_F} \right] \tag{10}$$

where

$$A^* = \frac{4\pi m^* q (kT)^2}{h^3} \tag{11}$$

$$C_{1F} = \frac{1}{2E_{00}} \ln\left(\frac{4(V_B - V)}{V_F}\right) \tag{12}$$

$$b_{1F} = \frac{q(V_B - V)}{E_{00}} \tag{13}$$

and

$$E_{00} = \frac{qh}{4\pi}\left(\frac{N_D}{\epsilon_s m^*}\right)^{1/2}, \tag{14}$$

provided that the temperature is low enough that

$$kT < 2E_{00}\left[\ln\left(\frac{4V_B}{V_F}\right) + \left(\frac{2E_{00}}{V_F}\right)^{1/2}\right]^{-1}. \tag{15}$$

This condition is satisfied at 300°K for Pd_2Si contacts as long as $N_D \geq 1 \times 10^{20}/\text{cm}^3$. Under the assumptions of the theory, J_T is specified by N_D, V_B, ϵ_s, and the effective mass of the tunneling carrier m^*. Using $\epsilon_r = 11.7$ for the relative dielectric constant of Si and $m^* = 0.259 m_0$ [20] where m_0 is the free electron mass, equation 10 predicts a zero bias tunnel resistance, R_T, of 0.13 Ω. A more exact treatment would result in a somewhat lower value of R_T [19]. However this will be offset to some extent by the nonuniformity of J_T over the contact area in the experimental structure used. Consequently, $R_T \sim 0.1\,\Omega$ is a reasonable lower bound for R_I. Thus $0.1 < R_I < 0.7$, and one can conclude that there was no significant contribution to R_I beyond that expected from the tunneling probability.

6. SUMMARY

The results presented in this paper describe the fabrication and behavior of Pd_2Si ohmic and rectifying contacts to n-type Si. The Pd_2Si phase has been identified with X-ray diffraction analysis, and its penetration depth into a Si contact examined. The electrical resistivity of Pd_2Si has been measured. The barrier height and contact resistance of Pd_2Si/Si contacts have been determined. Both the electrical and metallurgical characteristics of Pd_2Si contacts are very similar to those of PtSi contacts. The fabrication procedures for Pd_2Si and PtSi are significantly different, however. Pd_2Si forms at much lower temperatures. Unreacted Pd can be readily etched away with an aqueous solution of $KI + I_2$, an etchant compatible with photoresists and a variety of other materials. Finally, Pd is readily deposited by evaporation from a tungsten boat.

There are a number of Si device applications in which these differences can be used with advan-

tage. For example, the threshold voltage stability problems observed with MOSFET's which are attributed to the exposure of the device to an electron beam or sputtering environment have already been cited. In the fabrication of passivated contacts (e.g. metal–Si diodes) where the contact metal overlaps the SiO_2 surrounding the contact opening, photoresist compatibility is desirable. There are other applications for which the low formation temperature is important.

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