Applied Physics Letters ARTICLE scitation.org/journal/apl

Charge transport mechanism in the metal–nitride–oxide–silicon forming-free memristor structure

Cite as: Appl. Phys. Lett. **116**, 203502 (2020); doi: 10.1063/5.0001950
Submitted: 21 January 2020 · Accepted: 26 March 2020 ·
Published Online: 19 May 2020

View Online Export Citation CrossMark

A. A. Gismatulin,[1,2,a)] Oleg M. Orlov,[3,4] V. A. Gritsenko,[1,2,5] V. N. Kruchinin,[1] D. S. Mizginov,[3] and G. Ya. Krasnikov[3]

AFFILIATIONS

[1]Rzhanov Institute of Semiconductor Physics SB RAS, 13 Lavrentiev Ave., 630090 Novosibirsk, Russia
[2]Novosibirsk State University, 2 Pirogov Str., 630090 Novosibirsk, Russia
[3]Molecular Electronics Research Institute, 1st Zapadnyi Proezd 12/1, 124460 Zelenograd, Moscow, Russia
[4] Moscow Institute of Physics and Technology, 9 Institutskiy per, 141701 Dolgoprudny, Moscow Region, Russia
[5]Novosibirsk State Technical University, 20 Marx Ave., 630073 Novosibirsk, Russia

[a)]**Author to whom correspondence should be addressed:** aagismatulin@isp.nsc.ru

ABSTRACT

Silicon oxide and silicon nitride are two key dielectrics in silicon devices. The advantage of Si_3N_4 over other dielectrics is that silicon nitride is compatible with silicon technology. It is required to study in detail the charge transport mechanism in a Si_3N_4-based memristor to further improve the cell element and to create a matrix of these elements. Despite many research activities carried out, the charge transport mechanism in Si_3N_4-based memristors is still unclear. Metal–nitride–oxide–silicon structures that exhibit memristor properties were obtained using low-pressure chemical vapor deposition at 700 °C. The fabricated metal–nitride–oxide–silicon memristor structure does not require a forming procedure. In addition, the metal–nitride–oxide–silicon memristor has a memory window of about five orders of magnitude. We found that the main charge transport mechanism in the metal–nitride–oxide–silicon memristor in a high resistive state is the model of space-charge-limited current with traps. In a low resistive state, the charge transport mechanism is described by the space-charge-limited current model with filled traps. Trap parameters were determined in the Si_3N_4-based memristor in the high resistive state.

Silicon oxide and silicon nitride form the silicon technology basis. Unlike silicon oxide, Si_3N_4 has a high concentration of electron traps and is widely used as a storage medium in TaN –alumina–nitride–oxide–silicon (TANOS) charge trap flash memories.[1] Currently, the intensive research is under way to develop a universal memory. One of the promising candidates for the universal memory is a memristor-based resistive random-access memory (ReRAM).[2] The memristor operation principle is based on switching the dielectric active medium between the logical states with a high resistive state (HRS) and low resistive state (LRS). Various non-stoichiometric dielectrics, such as HfO_x,[3,4] ZrO_x,[5–7] TaO_x,[8–10] AlO_x,[11,12] NbO_x,[13,14] and SiO_x,[15,16] are currently being studied as an active medium.

It is now widely accepted that Si_3N_4 is a good resistive switching layer due to its abundant traps for non-volatile memory applications.[17–19] The introduction of the SiO_2 tunnel layer into the Si_3N_4-based memristor structure leads to an increase in the injected current at a fixed voltage due to the difference in dielectric constants or the switching voltage decreases at a fixed current and; consequently, the power is decreased.[18,20]

The charge transport mechanism in the metal–nitride–oxide–silicon (MNOS) structure with a thick Si_3N_4 layer was studied in Ref. 21. Such a structure did not exhibit memristor properties and the main charge transport mechanism was the multiphonon isolated trap ionization model. The charge transport mechanism of the memristor based on silicon nitride in the LRS was studied in Refs. 22 and 23. In weak electric fields, the charge transport is interpreted based on the Frenkel effect. In strong fields, the charge transport is interpreted in terms of the Fowler–Nordheim tunnel effect. In Ref. 24, the charge transport in LRS in silicon nitride is interpreted in the Schottky effect model. For Ni/SiN_x/p^{++}-Si memristors in the high resistance state (HRS) with different parameter x values, the charge transport mechanism was studied in Ref. 25. The charge transport is interpreted in the

framework of Frenkel model. In Ref. 26, the charge transport in the LRS state was interpreted in terms of the Schottky effect model. A hole barrier of 0.301 eV was obtained at the Ni/Si_3N_4 interface. The charge mechanism of silicon nitride in the LRS and HRS was studied in Refs. 27 and 28. The charge transport is interpreted in the space-charge-limited current (SCLC) model without a detailed discussion about model parameters. However, at present, there is no single universal charge transport model of a memristor based on Si_3N_4. In Ref. 28, the charge transport mechanism in a PECVD SiN_x-based memristor is the phonon-assisted tunneling between traps. The aim of this paper is an experimental study of the charge transport in the MNOS memristor, a comparison with the theory and the determination of trap parameters in a memristor.

For the researched charge transport mechanism in an MNOS with a thin Si_3N_4 layer, we fabricated a Ni/Si_3N_4/SiO_2/p^+-Si memristor structure. An initially doped p-type silicon substrate with resistance of 11.5 Ω × cm was used. Then a 2 nm thick SiO_2 layer was formed by thermal oxidation, and a 4 nm Si_3N_4 film, which served as a resistive switching layer, was then deposited using low-pressure chemical vapor deposition (LPCVD) at 700 °C, with a mixture of SiH_2Cl_2 and NH_3 (at a ratio ∼1:3). Ion implantation (BF_2^+ with the energy of 40 keV and the dose of 8×10^{14} cm^{-2}) was performed through the resulting layers to the obtained high-doped p^+-type silicon substrate. After the implantation, the rapid thermal annealing at 1030 °C was performed, followed by dielectric (SiO_2 and Si_3N_4) layers and lattice damages curing and dopant activation. As a result, the result numbers of technological operations were additionally decreased excluding the buffer oxide by forming and removing it. Finally, the Ni (100 nm thick) top electrode was deposited with a thermal evaporator using a shadow mask. The Ni electrode diameter was 200 μm. The current–voltage characteristics were measured by the Agilent B1500A semiconductor parameter analyzer. The bottom electrode (p^+-Si) was grounded during the measurement. The current–voltage characteristics were measured at different temperatures while keeping the memristor in the fixed resistance and the sweep less than the set/reset voltage. The experimental current–voltage characteristics were compared with the Frenkel model and the model of space-charge-limited currents (SCLC).

With the aim of high-spatial scanning ellipsometer Microscan-3M (ISP SB RAS),[29] the central 8×8 mm^2 region of the sample (10×10 mm^2) was mapped. The steps of mapping (x, y) were 1 mm. The light beam angle (E = 1.96 eV) on the sample was 60°. The laser beam was focalized into the 10 μm light spot with the high-quality non-polarizing microlens. The ellipsometer is equipped with a computer operated scanning stage that allows measuring the optical parameters distribution over the sample surface up to 150×150 mm^2. A four-zone measurement technique was used, followed by the averaging over all zones. The thickness in each scanning Si_3N_4 layer point was calculated independently by solving the numerical-inversion problem of ellipsometry[30] for the simple optical model: Si-SiO_2 (2 nm, n = 1.46)–Si_3N_4 (n = 2.00). Figure 1(a) shows a high homogeneity in the Si_3N_4 dielectric film thickness (4 nm ± 5%).

It is shown in Fig. 1(b) that the 10 cycle typical bipolar resistive switching is observed in our fabricated MNOS structure at room temperatures. The device was set under the current compliance (CC) of 3 mA to prevent a permanent dielectric breakdown and to obtain a reset process. The positive bias leads to the set switching, in which the devices are switched from HRS to LRS. Our fabricated forming-free MNOS structure shows a reproducible bipolar switching. The operation voltage was within 3.6–5.0 V during the set process (V_{set} = 3.6–4.0 V, V_{reset} = −1.6 to −2.2 V). The memory window was at least five orders of magnitude. It should be noted that the leakage current is small enough (10^{-11} A at 1 V) and room temperature is in the initial state.

It is shown in Fig. 1(b) that the HRS is not stable, and it is confirmed by the further cycling in Fig. 1(c). We are able to reach the stability LRS through the use of the current compliance value of 3 mA. We assume that the HRS is observed to be non-stable due to the presence of a residual filament from the incomplete filament dissolution in the switching process. The following parameters were used to measure the cycling: pulse time 50 ms; V_{set} = 4.5 V, V_{reset} = −3.5 V and the compliance set/reset = 3 mA. After ten cycles, the memristor resistance was measured in HRS and LRS at V_{read} = 0.5 V. The retention measurements were carried out after thermal heating at 85 °C at different times from 10 to 10^5 s at voltage V_{read} = 0.5 V. The current at 0.5 V in the LRS state does not change in 10^5 s. The current at 0.5 V in the HRS state increases in 10^5 s, that is, the memory window grows in time; therefore, it is impossible to extrapolate the data to years at room temperature to estimate the charge storage time.

To simulate the experimental data only in the nitride layer, the current–voltage characteristics were recalculated with the voltage drop deduction in the SiO_2 layer from the voltage drop of the entire structure. To simulate the current–voltage characteristic, only the part with negative voltages was used to exclude the space charge region of the p-type substrate.

The current I in the material with traps is described by the expression[31,32]

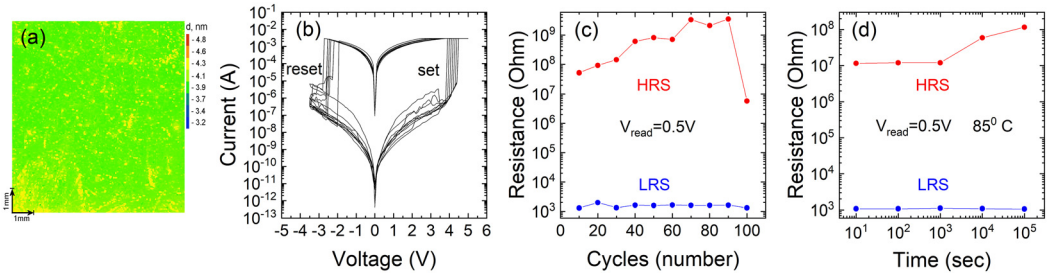

FIG. 1. (a) Scanning ellipsometry of silicon nitride layer thickness of the MNOS memristor structure; (b) 10 cycle HRS–LRS loop of the Si_3N_4-based memristor; (c) MNOS memristor endurance at room temperature. Pulse width = 50 ms, V_{set} = 4.5, V_{reset} = −3.5 V, V_{read} = 0.5 V; (d) MNOS memristor retention at 85 °C in HRS and LRS states.

$$I = eN^{2/3}SP. \quad (1)$$

Here e—electron charge, $N = a^{-3}$—trap concentration, a—average distance between traps, S—contact area, and P—trap ionization probability.

The Frenkel effect describes the potential lowering of an isolated Coulomb trap under the influence of applied electric field [Fig. 2(a)]. The trap ionization probability by the Frenkel effect is described using the expression[33,34]

$$P = \nu \exp\left(-\frac{W - \beta_F\sqrt{\frac{U}{d}}}{kT}\right), \quad \beta_F = \left(\frac{e^3}{\pi\varepsilon_\infty\varepsilon_0}\right)^{\frac{1}{2}}. \quad (2)$$

Here, $\nu = W/h$—attempt to escape factor, W—trap ionization energy, β_F—Frenkel constant, U—voltage, d—thickness, k—Boltzmann constant, T—temperature, e—electron charge, ε_∞—high frequency permittivity, and ε_0 —dielectric constant.

The current–voltage characteristics description of the MNOS memristor in HRS using the Frenkel model gives the trap ionization energy value $W = 0.62$ eV. The attempt to escape factor is determined from the expression $\nu = W/h$ and is equal to $\nu = 1.5 \times 10^{14}\,s^{-1}$. When modeling the experimental data of the MNOS memristor in the HRS by the Frenkel model, the trap concentration was anomalously small $N = 1 \times 10^7\,cm^{-3}$. In addition, the Frenkel model gives an abnormally big high-frequency dielectric constant value $\varepsilon_0 = 100$ [Fig. 2(b)]. Therefore, the Frenkel model does not describe the current–voltage characteristics of the MNOS memristor in HRS. The current–voltage characteristics of the MNOS memristor in LRS are weakly dependent on temperature; therefore, the Frenkel model is not applicable for describing the charge transfer in LRS.

The theory of space-charge-limited current (SCLC) between flat parallel electrodes is presented in detail in Ref. 35. The current in the SCLC model consists of several sections with different current voltage dependences. In our case, there are Ohmic and quadratic parts, which are given by the expression[36]

$$I = I_{Ohm} + I_{SCLC} = Se\mu n\frac{U}{d} + S\frac{9}{8}\mu\varepsilon\varepsilon_0\theta\frac{U^2}{d^3}, \quad (3)$$

$$n = \frac{2N_d}{1 + \sqrt{1 + \frac{4gN_d}{N_c}\exp\left(\frac{E_a}{kT}\right)}},$$

Here

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}} \quad \text{and} \quad \theta = \frac{1}{1 + \frac{N_t}{N_c}\exp\left(\frac{W_t}{kT}\right)}. \quad (4)$$

Here S—area involved in the charge transport, μ—electron mobility, n—free electron concentration in the dielectric, ε—static dielectric constant, θ—the fraction of free electrons from all injected ones (trapped and free), N_d—donor concentration, g—degeneracy factor, N_c—effective density of states, E_a—donor activation energy, N_t—trap concentration, W_t—trap energy, m^*—electron effective mass, and h—Planck constant.

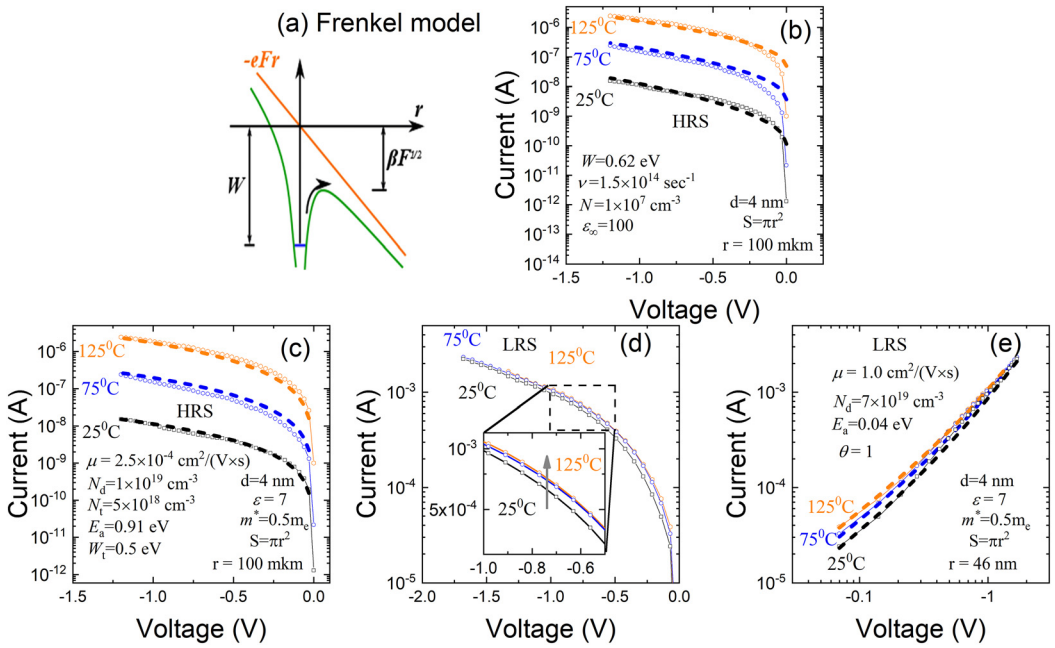

FIG. 2. (a) The potential lowering of an isolated Coulomb trap under the influence of applied electric field in the Frenkel model; (b) current–voltage characteristics of the Ni/Si_3N_4/SiO_2/p^+-Si memristor structure in HRS and simulation curves by the Frenkel model; (c) current–voltage characteristics of the Ni/Si_3N_4/SiO_2/p^+-Si memristor structure in HRS and simulation curves by the SCLC model; (d) current–voltage characteristics of the Ni/Si_3N_4/SiO_2/p^+-Si memristor structure in LRS and zoomed-in inset; (e) current–voltage characteristics of the Ni/Si_3N_4/SiO_2/p^+-Si memristor structure in LRS and simulation curves by the SCLC model in double logarithmic scale.

The SCLC model has many parameters. To reduce the number of variable parameters, some of the parameters are taken from the published data. The effective mass ($m^* = 0.5\,m_e$) and static dielectric constant ($\varepsilon = 7$) values were taken from the typical values of Si_3N_4.[37–39] Since the MNOS memristor is forming-free, in the HRS state, we assume parameter S as the entire contact ($r = 100\,\mu m$). We assume the filament conduction model in the MNOS structure in LRS, where the filaments are amorphous silicon. Therefore, for the LRS case, we took the mobility equal to the mobility in amorphous silicon [$\mu = 1\,cm^2/(V \times s)$]. The donor concentration determines the theoretical curve slope in the SCLC model at low voltages and the trap concentration determines the slope at high voltages.

The current–voltage characteristics of the MNOS memristor in HRS are well described by the SCLC model with the donor concentration $N_d = 1 \times 10^{19}\,cm^{-3}$, activation energy $E_a = 0.91$ eV, trap concentration $N_t = 5 \times 10^{18}\,cm^{-3}$, and trap energy $W_t = 0.5$ eV [Fig. 2(c)]. The charge transport goes through the entire contact area and the mobility obtained from the SCLC model is the mobility equal to $\mu = 2.5 \times 10^{-4}\,cm^2/(V\,s)$ that is close to the value obtained in Ref. 40. The donor activation energy from the SCLC model is quite large due to deep traps. All these indicate that the charge transport goes through the silicon nitride material.

The current–voltage characteristics of the MNOS memristor in LRS are weakly dependent on temperature; therefore, $\theta = 1$ [Fig. 2(d)]. Although LRS is weakly dependent on temperature, with the increasing temperature, the current in the Ohmic section of the current–voltage characteristic increases, and it indicates that the filament nature is closer to the semiconductor than to the metal one [inset in Fig. 2(d)]. In comparison with the experiment, the SCLC model gives the following parameters [Fig. 2(e)]: donor concentration $N_d = 1 \times 10^{20}\,cm^{-3}$ and activation energy $E_a = 0.06$ eV. If we take the mobility parameter as for amorphous silicon, then the effective radius of such a filament, according to the SCLC model, will be $r = 50$ nm.

The charge transport mechanism and the memristor storage properties are highly dependent on the active memristor layer fabrication technology. The silicon oxide and nitride thicknesses are comparable to the MNOS from Refs. 18 and 20, but due to a different fabrication technology, the memory window of our MNOS memristors is larger and they do not require a forming procedure.

In conclusion, the MNOS structures exhibiting memristor properties were obtained. The MNOS memristor does not require the forming procedure. The MNOS memristor has a memory window of about five orders of magnitude. The main charge transport mechanism of MNOS memristor in HRS is the SCLC model with traps. In LRS, the transport mechanism is described by the SCLC model with filled traps. Trap concentration $N_t = 5 \times 10^{18}\,cm^{-3}$ and trap energy $W_t = 0.5$ eV were determined in silicon nitride in HRS.

The fabrication of experimental samples and the experiments were carried out by grant of the Russian Foundation for Basic Research (Project No. 19-29-03018). The experimental data simulation was carried out with the support of the Russian state research No. 0306-2019-0005.

REFERENCES

[1] V. A. Gritsenko, in *Thin Films on Si: Electronic and Photonic Applications*, edited by V. Narayanan, M. Frank, and A. A. Demkov (World Scientific Press, 2016), pp. 273–322.
[2] M. A. Zidan, J. P. Strachan, and W. D. Lu, Nat. Electron. **1**(1), 22–29 (2018).
[3] L. Goux, P. Czarnecki, Y. Y. Chen, L. Pantisano, X. P. Wang, R. Degraeve, B. Govoreanu, M. Jurczak, D. J. Wouters, and L. Altimime, Appl. Phys. Lett. **97**(24), 243509 (2010).
[4] B. Ku, Y. Abbas, S. Kim, A. S. Sokolov, Y. R. Jeon, and C. Choi, J. Alloy Compd. **797**, 277–283 (2019).
[5] C. C. Hsu, T. C. Wang, and C. C. Tsao, J. Alloy Compd. **769**, 65–70 (2018).
[6] P. He, C. Ye, J. J. Wu, W. Wei, X. D. Wei, H. Wang, R. L. Zhang, L. Zhang, Q. Xia, and H. B. Wang, Semicond. Sci. Technol. **32**(5), 055016 (2017).
[7] Y. Abbas, I. S. Han, A. S. Sokolov, Y.-R. Jeon, and C. Choi, J. Mater. Sci. **31**, 903–909 (2020).
[8] B. Wang, K. H. Xue, H. J. Sun, Z. N. Li, W. Wu, P. Yan, N. Liu, B. Y. Tian, X. X. Liu, and X. S. Miao, Appl. Phys. Lett. **113**(18), 183501 (2018).
[9] Y. Abbas, M. R. Park, Q. Hu, T. S. Lee, H. Abbas, T. S. Yoon, and C. J. Kang, J. Nanosci. Nanotechnol. **16**(10), 10231–10236 (2016).
[10] Y. S. Fan, L. Q. Zhang, D. Crotti, T. Witters, M. Jurczak, and B. Govoreanu, IEEE Electron Device Lett. **36**(10), 1027–1029 (2015).
[11] S. Kim and Y. K. Choi, Appl. Phys. Lett. **92**(22), 223508 (2008).
[12] W. Banerjee, X. X. Xu, H. T. Liu, H. B. Lv, Q. Liu, H. T. Sun, S. B. Long, and M. Liu, IEEE Electron Device Lett. **36**(4), 333–335 (2015).
[13] S. Li, X. J. Liu, S. K. Nandi, and R. G. Elliman, Nanotechnology **29**(37), 375705 (2018).
[14] J. Park, E. Cha, I. Karpov, and H. Hwang, Appl. Phys. Lett. **108**(23), 232101 (2016).
[15] N. Xiao, M. A. Villena, B. Yuan, S. C. Chen, B. R. Wang, M. Elias, Y. Y. Shi, F. Hui, X. Jing, A. Scheuermann, K. C. Tang, P. C. McIntyre, and M. Lanza, Adv. Funct. Mater. **27**(33), 1700384 (2017).
[16] Y. F. Chang, B. Fowler, F. Zhou, Y. C. Chen, and J. C. Lee, Appl. Phys. Lett. **108**(3), 033504 (2016).
[17] X. F. Jiang, Z. Y. Ma, J. Xu, K. J. Chen, L. Xu, W. Li, X. F. Huang, and D. Feng, Sci. Rep. **5**, 15762 (2015).
[18] S. Kim, S. Jung, M. H. Kim, S. Cho, and B. G. Park, Appl. Phys. Lett. **106**(21), 212106 (2015).
[19] S. M. Hong, H. D. Kim, H. M. An, and T. G. Kim, IEEE Electron Device Lett. **34**(9), 1181–1183 (2013).
[20] S. Kim and B. G. Park, J. Alloy Compd. **663**, 256–261 (2016).
[21] K. A. Nasyrov, V. A. Gritsenko, A. K. Kim, H. S. Chae, S. D. Chae, W. I. Ryu, J. H. Sok, J. W. Lee, and B. M. Kim, IEEE Electron Device Lett. **23**(6), 336–338 (2002).
[22] S. Kim, S. Jung, M. H. Kim, Y. C. Chen, Y. F. Chang, K. C. Ryoo, S. Cho, J. H. Lee, and B. G. Park, Small **14**(19), 1704062 (2018).
[23] S. Kim, H. Kim, S. Hwang, M. H. Kim, Y. F. Chang, and B. G. Park, ACS Appl. Mater. Interfaces **9**(46), 40420–40427 (2017).
[24] S. Kim, Y. F. Chang, and B. G. Park, RSC Adv. **7**(29), 17882–17888 (2017).
[25] S. Kim, Y. F. Chang, M. H. Kim, and B. G. Park, Appl. Phys. Lett. **111**(3), 033509 (2017).
[26] S. Kim, S. Cho, and B. G. Park, AIP Adv. **6**(1), 015021 (2016).
[27] S. Kim, S. Jung, M. H. Kim, T. H. Kim, S. Bang, S. Cho, and B. G. Park, Nanotechnology **28**(12), 125207 (2017).
[28] S. V. Tikhov, A. N. Mikhaylov, A. I. Belov, D. S. Korolev, I. N. Antonov, V. V. Karzanov, O. N. Gorshkov, D. I. Tetelbaum, P. Karakolis, and P. Dimitrakis, Microelectron. Eng. **187-188**, 134–138 (2018).
[29] E. V. Spesivtsev, S. V. Rykhlitskii, and V. A. Shvets, Optoelectron., Instrum. Data Process. **47**(5), 419–425 (2011).
[30] H. G. Tompkins and E. A. Irene, *Handbook of Ellipsometry* (William Andrew Publishing, Springer, 2005).
[31] V. A. Gritsenko, T. V. Perevalov, V. A. Voronkovskii, A. A. Gismatulin, V. N. Kruchinin, V. S. Aliev, V. A. Pustovarov, I. P. Prosvirin, and Y. Roizin, ACS Appl. Mater. Interfaces **10**(4), 3769–3775 (2018).
[32] D. R. Islamov, V. A. Gritsenko, and A. Chin, Optoelectron. Instrum. Data Process. **53**(2), 184–189 (2017).

[33]J. Frenkel, Tech. Phys. USSR **5**(8), 685–695 (1938).
[34]J. Frenkel, Phys. Rev. B **54**, 647 (1938).
[35]M. A. Lampert and P. Mark, *Current Injection in Solids* (Academic Press, New York, 1970).
[36]V. A. Voronkovskii, V. S. Allev, A. K. Gerasimova, and D. R. Islamov, Mater. Res. Express **6**(7), 076411 (2019).
[37]A. V. Shaposhnikov, I. P. Petrov, V. A. Gritsenko, and C. W. Kim, Phys. Solid State **49**(9), 1628–1632 (2007).
[38]V. A. Gritsenko, Phys. Usp. **55**(5), 498–507 (2012).
[39]V. A. Gritsenko, E. E. Meerson, and Y. N. Morokov, Phys. Rev. B **57**(4), R2081–R2083 (1998).
[40]R. Hattori and J. Shirafuji, Appl. Phys. Lett. **54**(12), 1118–1120 (1989).