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Capacitance–voltage characterization of metal–insulator–semiconductor capacitors formed on wide-bandgap semiconductors with deep dopants such as diamond

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Atsushi Hiraiwa,[1,2,a)] Satoshi Okubo,[3,b)] Masahiko Ogura,[4] Yu Fu,[3,5] and Hiroshi Kawarada[1–3]

AFFILIATIONS

[1]Research Organization for Nano and Life Innovation, Waseda University, 513 Waseda-tsurumaki, Shinjuku, Tokyo 162-0041, Japan
[2]Kagami Memorial Laboratory for Material Science and Technology, Waseda University, 2-8-26 Nishiwaseda, Shinjuku, Tokyo 169-0051, Japan
[3]Faculty of Science and Engineering, Waseda University, 3-4-1 Okubo, Shinjuku, Tokyo 169-8555, Japan
[4]Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
[5]School of Electronic Science and Engineering, University of Electronic Science and Technology of China, No. 2006 West Hi-Tech Zone, Chengdu 611731, China

[a)]**Author to whom correspondence should be addressed:** qs4a-hriw@asahi-net.or.jp
[b)]**Present address:** Renesas Electronics Corporation, Takasaki, Gunma 370-0021, Japan.

ABSTRACT

As diamond possesses only deep dopants, certain conventional physics and characterization methods are not applicable to diamond devices, owing to the explicit or implicit assumption of shallow dopants. To resolve this limitation, the capacitance–voltage (C–V) characteristics of metal–insulator–semiconductor (MIS) capacitors formed on a semiconductor substrate with deep and compensating dopants were successfully formulated. Based on these equations, methods for accurately estimating the MIS capacitor properties were developed and validated through their application in the analysis of an actual MIS capacitor formed on a boron-doped hydrogen-terminated diamond substrate. The high-frequency C–V characteristic of the capacitor exhibited a prominent dip specific to deep dopants. However, the dip depth was considerably shallower than theoretically expected. This C–V characteristic was accurately reproduced theoretically, assuming the presence of a surficial diamond layer that contains acceptors with an activation energy of 0.23 eV, which is less than the value 0.37 eV for boron, and has a thickness of the extrinsic Debye length (40 nm in this study) or larger. The insulator charge of the MIS capacitor was estimated as -4.6×10^{12} cm^{-2} in units of electronic charge, which is sufficiently large to induce two-dimensional hole gas. The interface-state density was 1.4×10^{12} cm^{-2} eV^{-1} for interface-state energies of 0.3–0.5 eV above the valence band maximum. Hence, the proposed methodology and the possible presence of the reduced activation energy layer will guide the development of diamond-based devices.

I. INTRODUCTION

Modern technology is supported by various electronic devices that are generally fabricated using semiconductors, among which silicon is the most essential because its properties facilitate the economical mass production of highly integrated microdevices.[1] However, as silicon exhibits a relatively small bandgap of 1.12 eV,[2] the application of wide-bandgap semiconductors (WBGSs) is being expanded to optical and power control devices.[3,4] In addition to being the most popular material for jewelry, diamond is a WBGS with a bandgap of 5.5 eV,[5] which is larger than those of SiC, GaN, and Ga_2O_3. This wide bandgap can effectively enhance the breakdown

voltage of devices to potentially realize high-power devices with low power consumption.[6] Additionally, diamond has unique properties, such as negative electron affinity[7] and the generation of two-dimensional hole gas (2DHG),[8–10] both of which are caused by the hydrogen termination of the diamond surface along with the negative charge on the diamond surface for the latter. The wide bandgap and 2DHG are vital for realizing high-voltage and high-performance diamond metal–insulator–semiconductor field-effect transistors (MISFETs).[11]

To practically use the diamond devices, their fabrication technology and performance should be further improved. This improvement should be effectively achieved based on a deep understanding of the devices, which requires their accurate characterization. As diamond possesses only deep dopants, unlike other semiconductors, the appropriate management of the effects of these deep dopants remains a considerable challenge. However, the methods for the characterization[1,12,13] have been developed for semiconductors except diamond, such as Ge, Si, and GaAs, owing to their pioneering dominant role in the electronics industry. Therefore, several useful equations and analysis methods cannot be applied to diamond devices because they were derived or developed by explicitly or implicitly assuming shallow dopants. For instance, the concentration of carriers supplied by dopants was frequently assumed to be equal to the dopant concentration. However, the carrier concentration for deep dopants is significantly reduced from the dopant concentration by several orders of magnitude, and therefore, it should be adequately formulated and addressed,[14] similar to the investigation of activation energies of dopants (e.g., boron[15] and phosphorus[16]). Moreover, the capacitance–voltage (C–V) characteristics of metal–insulator–semiconductor (MIS) capacitors formed on a semiconductor substrate with shallow dopants vary monotonously and smoothly with the gate voltage, except in the case of inversion, whereas a dip was observed for the flatband gate voltage in the C–V characteristics of MIS capacitors formed on an indium-doped p-type silicon substrate.[17] The dip was caused by the relatively deep acceptor level of 0.157 eV[18] generated by substitutional indium. The C–V characteristics with the dip were reproduced theoretically only by considering deep levels.[17] Although boron—the shallowest dopant in diamond—exhibits an activation energy of 0.37 eV,[15] the diamond MIS capacitors did not show a dip in the C–V characteristics,[19–23] except those reported earlier.[24–27] As an exception, a prominent dip was observed in the C–V characteristics, but it was found to be an artifact caused by the interface states as the dip disappeared for high-frequency (HF) measurements, which suppressed the effect of the interface states on the measured capacitance.[27] The dips in certain exceptions might also be attributed to the interface states, as the authors only measured the low-frequency (LF) capacitance, which is influenced by interface states.[25,26] Although kinks were observed in the HF C–V characteristics of another report,[24] they required further investigations to identify the dips that are specific to deep dopants. Recently, a trace dip was observed in the HF C–V characteristics of an MIS capacitor formed on a Si-terminated diamond substrate.[28] However, even this dip is considerably shallower than the theoretical expectations.

The aforementioned formulas developed for In-doped Si can significantly aid in investigating the discrepancy between the In-doped Si and B-doped diamond. However, to a certain extent, the actual p-type diamond contains nitrogen as impurities, which can generate donor levels that are 1.7 eV below the conduction band minimum (CBM).[29] Therefore, the compensation effect by the donors neglected in the previous formulation should be considered in the C–V analysis of diamond MIS capacitors. Additionally, even the shallowest donor in diamond, i.e., phosphorus, requires an activation energy (0.57 eV)[16,30] that is larger than that of boron, hence necessitating the formulation of n-type substrates. Furthermore, the capacitance methods developed for interface-state characterization assume that most interface states—located above the valence band maximum (VBM) by an amount of energy comparable to the activation energy of boron—do not respond to HF modulation. This implies that the aforementioned formula, which implicitly assumes the instantaneous response of acceptors to modulation, might not apply to the capacitance measured at such high frequencies. Therefore, the capacitance must be clarified for superhigh-frequency (SHF) modulation, which fails to excite any response in deep dopants.

To address the aforementioned problems, this study successfully derived C–V formulas for deep dopants considering the compensation effect for both LF and SHF modulation using elementary functions that are suitable for physical investigations and simulations. The formulas were naturally applicable to n-type diamonds. Subsequently, to determine the cause of the missing dip, the theoretical results simulated using the formulas and a commercial device simulator were compared with the experimental results obtained using diamond MIS capacitors, which exhibited a prominent dip in the C–V characteristics. The model developed through the investigation properly reproduced the experimental C–V characteristics with the dip.

II. EXPERIMENTAL METHOD

The MIS capacitors used in this study were fabricated as follows. On a (001)-oriented IIb diamond substrate doped with boron to a concentration of 3×10^{19} cm^{-3}, a 4.7-μm-thick epitaxial layer was formed in an ambient of 33 hPa by introducing 1.2 SCCM CH_4, 399 SCCM H_2, and 0.12 SCCM 0.01% trimethylboron/H_2 using a microwave plasma chemical vapor deposition method.[31] After successive cleaning in H_2SO_4/HNO_3 mixture at 200 °C, piranha solution, NH_4OH/H_2O_2 mixture at 80 °C, and HCl/H_2O_2 mixture at 80 °C, the substrate surface was hydrogen-terminated in a hydrogen-containing environment with remote plasma production using microwaves. Subsequently, a 33-nm-thick Al_2O_3 film was formed by atomic layer deposition at 450 °C[6] using trimethylaluminum and H_2O as the precursors of Al and oxidant, respectively. Nitrogen was used as the purge and carrier gas for the precursors. The details of the atomic layer deposition process are described in a previous report.[32] Owing to the high temperature, the airborne adsorbates were preliminarily removed *in situ* during the standby period to stabilize the sample temperature. Subsequently, gate electrodes were formed by evaporating Au through the openings of a metal mask using a resistive heating method. Finally, the Al_2O_3 film parasitically formed on the backside of the substrate was removed, and a stack of a 20-nm-thick Ti film and 250-nm-thick Au film was formed as an ohmic contact to the substrate using ion-beam sputtering and deposition methods, respectively. Moreover,

TABLE I. Definitions of dimensionless quantities.

Notation	u_A	u_D	u_V	u_C	$u_F = u_B + v$	u_B	$v = \beta q \psi$
Definition	$\beta(E_A - E_V)$	$\beta(E_C - E_D)$	$\beta(E_V - E_i)$	$\beta(E_C - E_i)$	$\beta(E_F - E_i)$	$\beta(E_F - E_{i,0})$	$\beta(E_{i,0} - E_i)$

As shown in Fig. 1, the quantities E_A, E_D, E_V, E_C, E_F, and E_i, denote the energies of the acceptors, donors, VBM, CBM, Fermi level, and intrinsic Fermi level, respectively. $E_{i,0}$ denotes the value of E_i in the bulk. The quantity β is defined as $\beta = 1/(kT)$.

no post-metallization annealing was applied, as damage was not expected from the resistive heating deposition.

The impurity depth profiles in the substrate were measured using secondary ion mass spectroscopy (SIMS) at the Foundation for Promotion of Material Science and Technology of Japan. The C–V characteristics of the MIS capacitors for modulation frequencies of 1–100 Hz and 1 kHz–1 MHz were measured using a Keysight B2912A precision source/measure unit and a B1520A multifrequency capacitance measurement unit embedded in a B1500A semiconductor device analyzer (Keysight Technologies), respectively. The amplitude of the alternating current (AC) modulation for the capacitance measurements was 30 mV, and all the measurements were conducted at 296 K.

III. FORMULATION OF C–V CHARACTERISTICS FOR DEEP DOPANTS

A. Depth distributions of potential and carrier concentrations

The characterization of MIS capacitors using C–V methods is based on the analysis of the depth distributions of electrostatic potential and carriers in the semiconductor substrate, as summarized in this section. Gauss's law of electromagnetism requires the electrostatic potential ψ in the substrate to satisfy the Poisson equation

$$-\varepsilon_S \frac{d^2\psi}{dx^2} = \rho, \tag{1}$$

where ε_S and ρ are the permittivity and charge density of the substrate, respectively. Here, the origin and positive x-axis direction were set at the gate insulator/substrate interface and toward the interior of the substrate, respectively. Substituting N_A and N_D for the concentrations of acceptors and donors in the substrate, respectively, ρ can be expressed as

$$\rho = q(p - f_A N_A + f_D N_D - n), \tag{2}$$

where q is the electronic charge; p and n are the hole and electron concentrations in the substrate, respectively; and f_A and f_D are the ratios of the ionized acceptors and donors, respectively. Here, to facilitate the formulation and numerical calculations, we defined dimensionless quantities (Table I and Fig. 1), where E_A, E_D, E_V, E_C, E_F, and E_i denote the energies of the acceptors, donors, VBM, CBM, Fermi level, and intrinsic Fermi level, respectively. The quantity β is defined as $\beta = 1/(kT)$, where k and T are the Boltzmann constant and temperature, respectively. Physically, u_A and u_D denote the dimensionless activation energies of the acceptors and donors, respectively; u_V and u_C are the dimensionless energies of the VBM and CBM with respect to the intrinsic Fermi level, respectively; and u_F is the dimensionless deviation of the Fermi level from the intrinsic Fermi level. These definitions referring to the intrinsic Fermi level render the results for p- and n-type substrates symmetrical, as explained herein. Notably, although E_A, E_D, E_V, E_C, and E_i vary with the applied gate voltage V_G and depth x, the dimensionless quantities u_A, u_D, u_V, and u_C are constant, regardless of V_G and x, facilitating the formulation in this study. Only u_F varies with V_G and x according to the intrinsic Fermi level E_i because the Fermi level E_F in the substrate remains constant under the assumed thermal equilibrium and its role as the energy reference defines V_G. As the potential ψ is conventionally defined with respect to the value in the bulk of the substrate, i.e., $\psi = 0$ in the bulk,[1,33] the band bending in the substrate is given by $-q\psi$. Therefore, the intrinsic Fermi level is expressed as $E_i = E_{i,0} - q\psi$, where $E_{i,0}$ is the intrinsic Fermi level in the bulk. The dimensionless deviation of Fermi level u_F equals $u_B + v$, where u_B is the value of u_F in the bulk, expressed as $u_B = \beta(E_F - E_{i,0})$, and

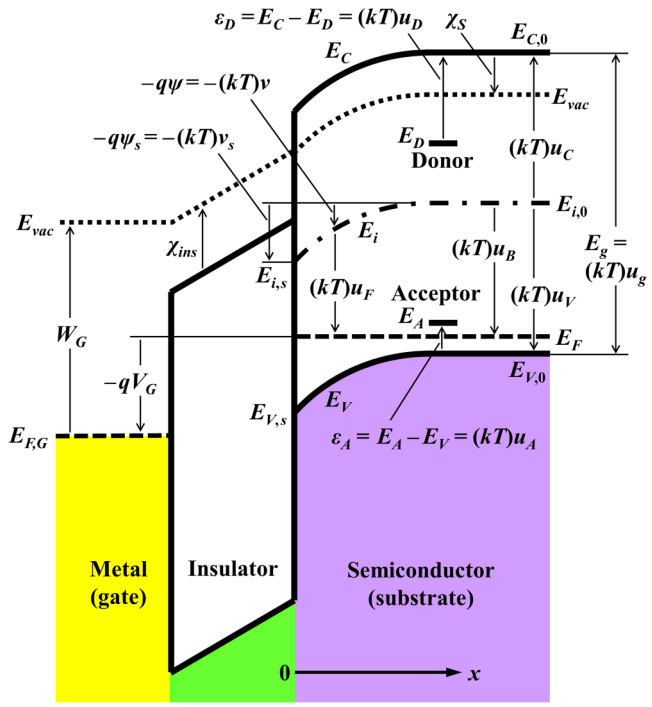

FIG. 1. Band diagram of a H-terminated diamond MIS capacitor. Gate is positively biased.

$\nu \equiv \beta q\psi$. For nondegenerate semiconductors, the hole and electron concentrations are approximately derived as $p = N_V e^{\beta(E_V - E_F)} = N_V e^{u_V - u_B - \nu}$ and $n = N_C e^{\beta(E_F - E_C)} = N_C e^{u_B - u_C + \nu}$, respectively, where N_V and N_C are the effective density of states of the valence and conduction bands, respectively.[1,12,14] Moreover, the hole and electron concentrations are expressed as

$$p = p_0 e^{-\nu}, \tag{3}$$

$$n = n_0 e^{\nu}, \tag{4}$$

where p_0 and n_0 are the values of p and n in the bulk, respectively, which are expressed as $p_0 = N_V e^{u_V - u_B}$ and $n_0 = N_C e^{u_B - u_C}$. The ionization functions f_A and f_D are expressed as[12]

$$f_A = 1/\{1 + g_A \exp(u_A + u_V - u_F)\},$$

$$f_D = 1/\{1 + g_D \exp(u_D - u_C + u_F)\},$$

where g_A and g_D represent the ground-state degeneracies of the acceptor and donor levels, respectively. Using p_0 and n_0, the ionization functions can be expressed as follows:

$$f_A(\nu) = 1/[1 + (p_0/\tilde{N}_V)e^{-\nu}], \tag{5}$$

$$f_D(\nu) = 1/[1 + (n_0/\tilde{N}_C)e^{\nu}], \tag{6}$$

where $\tilde{N}_V$ and $\tilde{N}_C$ are defined as $\tilde{N}_V \equiv N_V e^{-u_A}/g_A$ and $\tilde{N}_C \equiv N_C e^{-u_D}/g_D$.

As the bulk substrate ($\nu = 0$) is neutral, p_0 and n_0 satisfy the following equation:

$$p_0 - f_A(0)N_A + f_D(0)N_D - n_0 = 0.$$

For a p-type substrate, that is, $u_B < 0$, n_0 is considerably smaller than $\tilde{N}_C$; therefore, $f_D(0) \approx 1$, and the charge neutrality equation along with Eq. (5) yields the solution p_{p0} for p_0, expressed as[34]

$$p_{p0} = \frac{(\tilde{N}_V + N_D)}{2}\left[\sqrt{1 + \frac{4\tilde{N}_V(N_A - N_D)}{(\tilde{N}_V + N_D)^2}} - 1\right]. \tag{7}$$

Similarly, the minority carrier density n_{p0} can be expressed as

$$n_{p0} = N_V N_C e^{-\beta E_g}/p_{p0}, \tag{8}$$

where E_g denotes the bandgap of the semiconductor substrate. Similar to p_{p0} and n_{p0}, the majority and minority carrier densities, n_{n0} and p_{n0}, in an n-type substrate can be derived as

$$n_{n0} = \frac{(\tilde{N}_C + N_A)}{2}\left[\sqrt{1 + \frac{4\tilde{N}_C(N_D - N_A)}{(\tilde{N}_C + N_A)^2}} - 1\right], \tag{9}$$

$$p_{n0} = N_V N_C e^{-\beta E_g}/n_{n0}. \tag{10}$$

For a p-type substrate with shallow dopants, as $\tilde{N}_V$ is considerably larger than N_A and N_D owing to the nondegeneracy assumption, the majority carrier concentration p_{p0} is approximately equal to $N_A - N_D$ as expected. The result for n_{n0} for shallow dopants is similar. The specific examples of hole concentrations evaluated for diamond have been reported in a previous study.[35] After deriving the majority carrier concentrations using Eqs. (7) and (9), the Fermi levels of the p- and n-type substrates were estimated using Eqs. (3) and (4), respectively,

$$E_F - E_{V,0} = kT \ln(N_V/p_{p0}), \tag{11}$$

$$E_F - E_{C,0} = -kT \ln(N_C/n_{n0}), \tag{12}$$

where $E_{V,0}$ and $E_{C,0}$ represent the values of E_V and E_C in the bulk, respectively.

B. Formulation of *C–V* characteristics for low-frequency modulation

First, we derive the equations for an ideal gate insulator, i.e., empty of interface states and insulator charge. The capacitance of a capacitor is determined from the response of the capacitor charge to a small AC modulation superimposed on the bias voltage applied to the gate electrode. For LF modulation, the capacitor charge responds instantaneously to modulation. This implies that the substrate of the capacitor is in thermal equilibrium for any instantaneous value of the AC-modulated gate voltage. Thus, the gate capacitance C_G for LF modulation is obtained as

$$C_G = -\frac{dQ_S}{dV_G} = -\frac{dQ_S}{d\psi_s}\Big/\frac{dV_G}{d\psi_s}, \tag{13}$$

where Q_S is the charge stored in the substrate and ψ_s is the surface potential; that is, the value of potential ψ at the interface ($x = 0$). As the field F in the semiconductor approaches 0 in the limit of large x, Q_S is expressed using Gauss's law as follows:

$$Q_S = -\varepsilon_S F_s, \tag{14}$$

where F_s denotes the value of F at the interface. The gate voltage V_G is expressed as $V_G = V_{fb,0} + \psi_s + d_{ins}F_{ins}$, where d_{ins} and F_{ins} are the thickness and electric field of the gate insulator, respectively, and $V_{fb,0}$ is the flatband voltage for the ideal gate insulator, which is specifically expressed as

$$V_{fb,0} = \{W_G - [\chi_S + E_g - (E_F - E_{V,0})]\}/q, \tag{15}$$

assuming W_G and χ_S as the work function of the gate and the electron affinity of the substrate, respectively. Based on the relation $\varepsilon_{ins}F_{ins} = \varepsilon_S F_s$ derived using Gauss's equation, where ε_{ins} is the permittivity of the gate insulator, V_G can be expressed as follows:

$$V_G = V_{fb,0} + \psi_s + \varepsilon_S F_s/C_{ins} = V_{fb,0} + \nu_s/(\beta q) + \varepsilon_S F_s/C_{ins}, \tag{16}$$

where C_{ins} is the capacitance of the gate insulator expressed as $C_{ins} = \varepsilon_{ins}/d_{ins}$. The substitution of Eqs. (14) and (16) into Eq. (13) yields the gate capacitance C_G as follows:

$$C_G = \frac{1}{1/C_S + 1/C_{ins}}, \tag{17}$$

where C_S is the substrate capacitance (or semiconductor capacitance) expressed as $C_S = -dQ_S/d\psi_s$, which can be further reduced using Eq. (14) to $C_S = \varepsilon_S dF_s/d\psi_s$. As F is expressed as $F = -d\psi/dx$ and both ψ and F approach 0 in the limit of large x or equivalently small ψ, the electric field F_s at the interface is obtained as follows:

$$F_s = \mathrm{sign}(\psi_s)\left(-\frac{2}{\varepsilon_S}\int_0^{\psi_s}\rho d\psi\right)^{1/2} = \mathrm{sign}(v_s)\left(-\frac{2}{\varepsilon_S\beta q}\int_0^{v_s}\rho dv\right)^{1/2}, \tag{18}$$

using Eq. (1) and the following equation:

$$\frac{d^2\psi}{dx^2} = -\frac{dF}{dx} = -\frac{dF}{d\psi}\frac{d\psi}{dx} = \frac{dF}{d\psi}F = \frac{1}{2}\frac{dF^2}{d\psi}.$$

In Eq. (18), the values of $\mathrm{sign}(\psi_s)$ are equal to 1 and -1 if ψ_s is positive and negative, respectively. Thus, C_S can be derived as

$$C_S(\psi_s) = -\frac{1}{F_s}\left(\rho_s + \int_0^{\psi_s}\frac{\partial\rho}{\partial\psi_s}d\psi\right) = -\frac{1}{F_s}\left(\rho_s + \int_0^{v_s}\frac{\partial\rho}{\partial v_s}dv\right), \tag{19}$$

where ρ_s is the value of ρ at the interface. Notably, this result was derived without assuming a uniform charge distribution. The partial differential term is evaluated based on the dopant depth distribution, as follows. To perform the integration in Eq. (18), the dopant distributions $N_A(x)$ and $N_D(x)$ must be expressed as a function of ψ or equivalently v. This is achieved using the inverse function $x = h^{-1}(v)$ of $v = h(x)$, as $\bar{N}_A(v) = N_A[h^{-1}(v)]$. Because the function $h(x)$ depends on the surface potential, $\bar{N}_A(v)$ is also a function of the surface potential. Thus, $\bar{N}_A(v)$ can be expressed as $\bar{N}_A(v,\ v_s)$, which is similar for N_D and ρ. Therefore, $\partial\rho/\psi_s$ and $\partial\rho/v_s$ in Eq. (19) should be interpreted as $\partial\bar{\rho}(\psi,\ \psi_s)/\partial\psi_s$ and $\partial\bar{\rho}(v,\ v_s)/\partial v_s$, respectively. In the case of uniform dopant distributions, as p, n, f_A, and f_D are functions of only the potential, without explicitly depending on x as confirmed in Eqs. (3)–(6), the charge density is also solely dependent on the local potential and has a functional relation that is uninfluenced by the surface potential. Although the potential itself is a function of the surface potential even in the case of uniform distributions, it is the integration variable here. Consequently, the integral in Eq. (18) depends on the surface potential only through the upper limit of integration, thereby eliminating $\partial\rho/\partial\psi_s$. Thus, the electric field F_s at the interface is calculated as $F_s(\psi_s) = \hat{F}_s(\beta q\psi_s)$, where $\hat{F}_s(v)$ is given, using Eqs. (2)–(6) and (18), by

$$\hat{F}_s(v) = \mathrm{sign}(v)\sqrt{2/(\varepsilon_S\beta)}\left\{\begin{array}{c} p_0(e^{-v}-1) - N_A\ln[f_A(v)/f_A(0)] \\ -N_D\ln[f_D(v)/f_D(0)] + (N_A - N_D)v + n_0(e^v - 1)\end{array}\right\}^{1/2}. \tag{20}$$

For p-type substrates, p_0 and n_0 should be replaced with p_{p0} [Eq. (7)] and n_{p0} [Eq. (8)], respectively. For reference, the flatband capacitance C_{fb} was evaluated using Eq. (17) and the substrate capacitance $C_{S,fb}$ of the flatband obtained in the limit of small ψ_s, as follows:

$$C_{S,fb} = \sqrt{\varepsilon_S\beta q^2}\{p_0 + [1 - f_A(0)]f_A(0)N_A + [1 - f_D(0)]f_D(0)N_D + n_0\}^{1/2}. \tag{21}$$

For shallow dopants, as $f_A(0)$ and $f_D(0)$ are approximately equal to either 1 or 0, $C_{S,fb}$ is reduced to the conventional value $C_{\mathrm{Debye}} = \varepsilon_S/\lambda_{\mathrm{Debye}}$, where λ_{Debye} is the extrinsic Debye length expressed as $\lambda_{\mathrm{Debye}} = \sqrt{\varepsilon_S/[\beta q^2(p_0 + n_0)]}$.[13] Finally, the C–V characteristics of a capacitor formed on a p-type substrate with deep dopants were analytically simulated, considering ψ_s as an auxiliary parameter, based on Eqs. (2)–(8), (16), (17), (19), and (20), where $\partial\rho/\partial\psi_s = 0$. As these equations are expressed using only the elementary functions, they are suitable for the investigation of device characteristics as well as for spreadsheet calculations, which are interactively and instantaneously executed. In the case of no compensating donors (i.e., $N_D = 0$), the obtained equations of C–V characteristics are consistent with those reported in previous studies.[17] The C–V characteristics for n-type substrates are similarly obtained using Eqs. (9) and (10) instead of Eqs. (7) and (8).

As confirmed in Eqs. (16) and (17), the properties of the gate insulator influenced the C–V characteristics only through the insulator capacitance C_{ins}. Therefore, provided that the values of C_{ins} are equal, the capacitors have the same C–V characteristics, regardless of the gate insulator. Thus, the thickness of the insulator can be conveniently estimated using the equivalent SiO_2 thickness (EOT) d_{eo} defined as $d_{eo} \equiv (k_{\mathrm{SiO}}/k_{ins})d_{ins}$, where k_{SiO} ($= 3.9$) and k_{ins} are the dielectric constants of SiO_2 and the gate insulator, respectively, because C_{ins} ($= k_{ins}\,\varepsilon_0/d_{ins}$) is equal to $k_{\mathrm{SiO}}\,\varepsilon_0/d_{eo}$, where ε_0 is the permittivity of the vacuum. Another merit of adopting EOT is the ease of its estimation, as the gate capacitance approaches C_{ins} in the limit of deep accumulation, i.e., $V_G \to -\infty$ for p-type substrates, and therefore, the EOT of the insulator is easily estimated from the gate capacitance measured for deep accumulation. This merit is especially enjoyed when the gate insulator is not a thermally grown SiO_2, and therefore, its dielectric constant or thickness is difficult to measure. The aforementioned equations are accurate because they were derived assuming only the nondegeneracy of the substrate. Additionally, they yield the relation between the surface potential and gate capacitance, as expressed by Eqs. (17) and (19). This relation is essential for investigating the C–V characteristics of MIS capacitors, and it cannot be easily obtained using commercially available device simulators.[36]

C. Formulation of C–V characteristics for superhigh-frequency modulation

The gate capacitance for the SHF modulation is derived. As the deep dopants do not respond to SHF modulations, the substrate is not in thermal equilibrium for the instantaneous values of the AC-modulated gate voltage. This requires a unique formulation that is distinct from the aforementioned formulations. First, the substrate-charge varying synchronously with the SHF modulation ΔV_G is denoted by ΔQ_S. Hereinafter, similar to ΔQ_S, the quantity with an antecedent character Δ represents the variation in the respective quantity caused by the modulation. Once ΔV_G and ΔQ_S are expressed as functions of $\Delta\psi_s$, the SHF capacitance $C_{G,SHF}$ can be obtained as the value in the limit of small $\Delta\psi_s$, expressed as

$$C_{G,SHF} = \lim_{\Delta\psi_s \to 0}\left(-\frac{\Delta Q_S}{\Delta V_G}\right).$$

Using Eqs. (14) and (16), ΔV_G and ΔQ_S are given as $\Delta V_G = \Delta\psi_s + \varepsilon_S \Delta F_s/C_{ins}$ and $\Delta Q_S = -\varepsilon_S \Delta F_s$. Thus, similar to the aforementioned capacitance, $C_{G,SHF}$ can be expressed as

$$C_{G,SHF} = 1/(1/C_{S,SHF} + 1/C_{ins}), \tag{22}$$

where $C_{S,SHF}$ is expressed as

$$C_{S,SHF} = \lim_{\Delta\psi_s \to 0}\frac{\varepsilon_S \Delta F_s}{\Delta\psi_s} = \lim_{\Delta\nu_s \to 0}\frac{\beta q \varepsilon_S \Delta F_s}{\Delta\nu_s}. \tag{23}$$

As deep dopants do not respond to SHF modulation, the ionization functions are fixed at the values for a respective bias voltage V_G during the SHF modulation. Therefore, the charge deviation $\Delta\rho$ in the substrate is given as $\Delta\rho = q(\Delta p - \Delta n)$. Owing to the continuity equation, the modulated quantities satisfy the following equation for holes:

$$\mu_h(p + \Delta p)\frac{d(\psi + \Delta\psi)}{dx} + D_h\frac{d(p + \Delta p)}{dx} = 0,$$

where μ_h and D_h are the mobility and diffusivity of holes, respectively. As the thermal equilibrium quantities (e.g., p and ψ) also satisfy the continuity equation, we obtain the following equation using dimensionless quantities for simplicity:

$$p\frac{d\Delta\nu}{dx} + \frac{d\nu}{dx}\Delta p + \frac{d\Delta p}{dx} = 0,$$

where Einstein relation was used, and only the terms up to the first order of the modulated quantities were retained. Using Eq. (3), this equation is solved for Δp, as follows:

$$\Delta p = -p\Delta\nu. \tag{24}$$

In p-type WBGSs, the term Δn can be neglected. Therefore, the variation $\Delta\rho$ in the charge can be expressed as $\Delta\rho = q\Delta p = -qp\Delta\nu$. Because $\Delta\nu$ and $\Delta\rho$ satisfy the Poisson equation [Eq. (1)], Eq. (18) can be employed to compute ΔF_s, yielding along with Eq. (3),

$$\Delta F_s = \mathrm{sign}(\Delta\nu_s)\left[\frac{2p_0}{\varepsilon_S\beta}\int_0^{\Delta\nu_s}\Delta\nu\exp(-\nu)d\Delta\nu\right]^{1/2}. \tag{25}$$

Here, ν should be treated as a function of $\Delta\nu$, similar to treating N_A and N_D as functions of ν in Eq. (18). Although this function cannot be accurately determined, an approximate function can be obtained for large ν_s, for which ν is also large and the charge density expressed in (2) is, therefore, approximately equal to $-qN_A$ (a constant independent of x). Thus, the solution of Eq. (1) has the form of $\nu = A(x-a)^2$ for $x \le a$. For this ν, the charge variation expressed in Eq. (24) is negligible, similar to the hole density p. Therefore, $\Delta\nu$ can be expressed as $\Delta\nu = B(x-b)$ for $x \le b$. As the electrostatic effect from the gate is shielded by the carriers in the neutral region, the potential varies mostly in the depletion layer. Therefore, a and b are assumed to be equal, and ν is expressed as $\nu = (\nu_s/\Delta\nu_s^2)\Delta\nu^2$, where ν equals ν_s for $\Delta\nu = \Delta\nu_s$. Based on these results and Eqs. (23) and (25), the SHF substrate capacitance is given as

$$\hat{C}_{S,SHF}(\nu_s) = \frac{\varepsilon_S}{\lambda_p}\sqrt{\frac{1-e^{-\nu_s}}{\nu_s}}\ (p\text{-type for large}\nu_s), \tag{26}$$

where λ_p is defined by $\lambda_p = \sqrt{\varepsilon_S/(\beta q^2 p_{p0})}$, which is approximately equal to the extrinsic Debye length because n_{p0} is negligible. Although a p-type substrate was assumed for deriving Eq. (26), this equation can also be applied to n-type substrates by replacing ν_s and λ_p with $-\nu_s$ and $\lambda_n = \sqrt{\varepsilon_S/(\beta q^2 n_{n0})}$, respectively. The SHF substrate capacitance $C_{S,SHF}(\psi_s)$ as a function of the surface potential ψ_s is given by $C_{S,SHF}(\psi_s) = \hat{C}_{S,SHF}(\beta q\psi_s)$. For reference, the value of $C_{S,SHF}$ for the flatband can be evaluated in the limit of small ψ_s, in the form $C_{S,fb,THF} = \varepsilon_S/\lambda_p$, which is approximately equal to C_{Debye}. Similar to the results for lower frequencies, the SHF C–V characteristics of the capacitor were simulated using Eqs. (22) and (26) for $C_{G,SHF}$ and using Eq. (16) for V_G, where $F_s(\psi_s)$ $(=\hat{F}_s(\nu_s)$, $\nu_s = \beta q\psi_s)$ is expressed in Eq. (20). The specific frequency of SHF is presently unclear. Given that the GHz operation of diamond MISFETs[37–39] is understood in the framework of HF formulation, SHF is supposed to be considerably larger than GHz, requiring further studies.

D. Formulation of C–V characteristics of MIS capacitors with non-ideal gate insulator

Owing to the heterointerface, the MIS capacitors inevitably have interface states that alter their charge Q_{it} with the gate voltage, according to their energy level relative to the Fermi level. Furthermore, because most gate insulators are amorphous and incorporated impurities in the sample preparation process, they are charged at imperfections. As it is difficult to estimate the charge distribution in the gate insulator, the charge is conventionally assumed to be located at the interface.[1,33] This convention may cause an error in the estimated insulator charge, which was consciously or unconsciously accepted in previous studies. Unlike the interface-state charge, the insulator charge does not vary with the

gate voltage. However, since deep-interface states do not alter their charge either (Sec. IV), the two are indistinguishable from each other. Therefore, for simplicity, the insulator charge is included in the interface-state charge here. As the interface-state charge shifts the relation between F_{ins} and F_s toward $\varepsilon_{ins}F_{ins} = \varepsilon_S F_s - Q_{it}$ according to Gauss's law, the gate voltage of MIS capacitors with interface states is given as

$$\begin{aligned} V_G &= V_{fb,0} + \psi_s + (\varepsilon_S F_s - Q_{it})/C_{ins} \\ &= V_{fb,0} + \nu_s/(\beta q) + (\varepsilon_S F_s - Q_{it})/C_{ins}. \end{aligned} \tag{27}$$

Thus, the flatband voltage equals $V_{fb} = V_{fb,0} - Q_{it}/C_{ins}$. The gate capacitance is obtained using this V_G and by replacing Q_S with $Q_S + Q_{it}$ in Eq. (13). The differentiation of terms in Eq. (13) must consider the frequency of the AC modulation for capacitance measurements. For sufficiently low frequencies, the interface states respond to the modulation, and, therefore, the differentiation in Eq. (13) yields[13]

$$C_{G,LF} = \frac{1}{1/(C_S + C_{it}) + 1/C_{ins}}, \tag{28}$$

where C_{it} is the capacitance associated with the interface states defined as $C_{it} \equiv -dQ_{it}/d\psi_s$. However, for the HFs suppressing the response of the interface states, the differentiation of the interface-state charge yields 0, as the interface-state charge remained constant. Therefore, the gate capacitance is equal to that of the no-interface-state case as follows:

$$C_{G,HF} = C_G \text{ [Eq. (17)]}. \tag{29}$$

Although the HF capacitance is unaffected by the interface states, the gate voltage is shifted by the interface charge [Eq. (27)], causing the "stretch-out," which is used to extract the density of the interface states using the Terman method.[40] In a low-temperature limit, the interface-state charge is caused by the interface states located between the Fermi level and charge neutrality level, which is the energy level of the interface states at the Fermi level for the neutral interface-state charge.[1] As the energy level E_{it} of interface states varies with the gate voltage, an energy E defined relative to the intrinsic Fermi level $E_{i,s}$ at the interface should be conveniently used, defined as $E \equiv E_{it} - E_{i,s}$. The relative energy of the interface states located at the Fermi level is expressed as $E = E_F - E_{i,s} = q\psi_s + u_B/\beta$, where E_{it} equals E_F. Therefore, the interface-state charge Q_{it} is given by

$$Q_{it}(\psi_s) = q\int_{q\psi_s + u_B/\beta}^{q\psi_{cnl} + u_B/\beta} D_{it}(E)\, dE, \tag{30}$$

where D_{it} is the interface-state density and ψ_{cnl} is the surface potential for which the interface-state charge is neutral. The interface-state capacitance is then obtained as $C_{it}(\psi_s) = q^2 D_{it}(q\psi_s + u_B/\beta)$. For reference, ψ_{cnl} is supposed to be located deep in the bandgap.

E. Theoretical *C–V* characteristics of MIS capacitors formed on WBGS with deep dopants

To facilitate the analysis of the experimental results described in Sec. IV, the *C–V* characteristics of the MIS capacitors formed on the deep-dopant WBGS were theoretically investigated using the aforementioned equations. In the simulations, the substrate was assumed to be a *p*-type diamond. The interface was assumed to be empty of the interface states, and thus, the LF and HF capacitances were the same. The activation energy of boron (acceptor) was assumed to be 0.37 eV,[15] and the effective density of states in the valence band at 300 K was assumed to be $2.07 \times 10^{19}\,\mathrm{cm}^{-3}$ based on the effective hole mass $m_{eff,h} = 0.878\ m_0$, where m_0 is the electron mass. This effective mass was estimated using the equation $m_{eff,h}^{3/2} = m_{lh}^{3/2} + m_{hh}^{3/2} + m_{so}^{3/2}$, where m_{lh} ($= 0.208\ m_0$),[41] m_{hh} ($= 0.614\ m_0$),[41] and m_{so} ($= 0.394\ m_0$)[42] are the effective masses of light, heavy, and spin–orbit split-band holes, respectively. For electrons, the effective density of states at 300 K was estimated as $1.07 \times 10^{19}\,\mathrm{cm}^{-3}$ using the effective electron mass $m_{eff,e} = (m_l m_t^2)^{1/3} = 0.566\ m_0$, where m_l ($= 1.4\ m_0$)[43] and m_t ($= 0.36\ m_0$)[43] are the longitudinal and transverse effective electron masses, respectively. Furthermore, g_A, g_D, E_g, and EOT of the gate insulator were assumed to be 6, 2, 5.5 eV,[5] and 20 nm, respectively.

The *C–V* characteristics of B-doped diamond MIS capacitors simulated for various doping concentrations are shown in Fig. 2, where Figs. 2(a)–2(c) show the results of the LF modulation, an enlarged image of (a), and the results of the SHF modulation, respectively. The SHF results were obtained using Eq. (26), which is valid only for $V_G > V_{fb}$. Therefore, they are shown only for this voltage range. The concentration of compensating donors was assumed to be $0\,\mathrm{cm}^{-3}$. Unlike those for shallow dopants, the LF *C–V* characteristics show a dip at the flatband voltage. Moreover, the minimum capacitance at the dip, expressed in Eqs. (17) and (21), increases with the acceptor concentration, which is in qualitative agreement with the results obtained in a previous study.[26] Regardless of the acceptor concentrations, the LF capacitances for accumulation do not vary significantly, whereas that for depletion increases with the acceptor concentration. Additionally, the LF capacitances for deep depletion differ—one abruptly increases and the other decreases with the gate voltage. In particular, the former was obtained by assuming the presence of minority carriers (inversion electrons) at thermal equilibrium, as given by Eq. (8). The threshold gate voltage for the onset of this inversion increases with the acceptor concentration, similar to that for shallow dopants. However, the inversion capacitance is practically difficult to observe in WBGS MIS capacitors for the following reason. To realize the inversion, the substrate should be in thermal equilibrium under the applied gate voltage for which the surface potential approximately equals the bandgap of the substrate in units of q, e.g., 5.5 V in diamond. The problem is that the time necessary for the substrate to reach the thermal equilibrium exponentially increases with the surface potential. Owing to this, in the time-limited capacitance measurements, the thermal equilibrium is practically reached only for $\psi_s < 0.7$ V[44] in *p*-type WBGS, which is significantly smaller than the aforementioned value for realizing the inversion. For reference, a practical method of supplying electrons for the inversion is to form an *n*-type (opposite to the

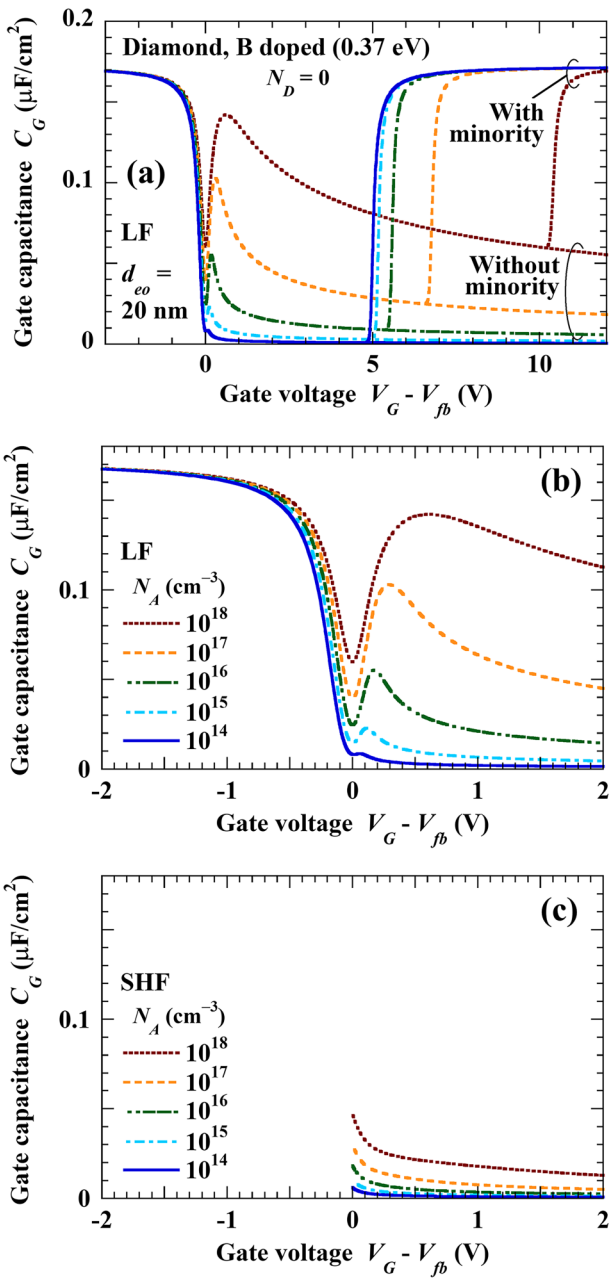

FIG. 2. Theoretical *C–V* characteristics of B-doped diamond MIS capacitors for various doping concentrations. Concentration of compensating donors and EOT of the gate insulator were assumed to be 0 cm^{-3} and 20 nm, respectively. Figures 2(a)–2(c) show the results for LF modulation, a magnified image of (a), and the results for SHF modulation, respectively. The SHF results are presented only for $V_G > V_{fb}$, owing to the limitation of the equation used for obtaining the results. The LF capacitance for high gate voltages splits into two branches that do and do not assume the presence of inversion minority carriers in the thermal equilibrium, represented by the upper and lower lines in Fig. 2(a), respectively. The SHF capacitance for high gate voltages is not branched because it was simulated without assuming the presence of minority carriers (not shown).

substrate) diffusion layer that overlaps with the gate and is electrically connected to the ohmic contact with the substrate. As they were derived assuming the thermal equilibrium (i.e., the presence of inversion carriers), the aforementioned equations for LF *C–V* characteristics are not applicable for deep depletion without inversion carriers. However, this case can be simulated by simply assuming an abnormally large value for the bandgap of the substrate in Eq. (8). The *C–V* characteristics determined using this method form the other branches, as shown in Fig. 2(a). Unlike the LF capacitance, the SHF capacitance, shown in Fig. 2(c), monotonously decreased with the gate voltage without exhibiting a dip. This is considerably smaller than the LF capacitance. This result is quite natural because the holes, which are the only component responding to SHF modulation, have a concentration that is significantly smaller than the acceptor concentration, owing to the deep acceptor level. Intriguingly, the SHF capacitance in the vicinity of the flatband extreme appeared to be smoothly connected to the LF capacitance for accumulation. As Eq. (26) was derived without assuming the presence of minority carriers, the SHF capacitance is not branched for high gate voltages (not shown).

Figure 3 shows the *C–V* characteristics for acceptor activation energies ($\varepsilon_A = E_A - E_V$) ranging from 0 to 1.7 eV. The acceptor concentration was assumed to be 1×10^{17} cm^{-3}, and the donor concentration and EOT of the gate insulator were the same as those in Fig. 2. Figures 3(a)–3(c) show the results for LF and SHF modulations, similar to Figs. 2(a)–2(c). Evidently, the dip in the LF *C–V* characteristics becomes shallower with diminishing acceptor energy and disappears for an activation energy of 0 eV (thick dotted line, black in color printing). Except for the dip, the LF *C–V* characteristics for activation energies of 0.57 eV and below differ slightly. For reference, the LF *C–V* characteristics for activation energies of 0.57 and 1.7 eV obtained by reversing the polarity of $V_G - V_{fb}$ in Fig. 3 are reasonably consistent with those expected for phosphorus- and nitrogen-doped *n*-type diamond MIS capacitors. This is because the substitutional phosphorus and nitrogen generate donors that are 0.57[16,30] and 1.7 eV[29] below CBM, respectively. The error in this convention is caused by the difference between g_A and g_D and between N_V and N_C. The threshold voltage for the onset of inversion marginally relied on an activation energy less than 0.57 eV. By contrast, the SHF capacitance, shown in Fig. 3(c), significantly increased with the decreasing activation energy owing to the increased hole concentration, in the same way as it increased with acceptor concentration, as observed in Fig. 2(c). For reference, as the LF gate capacitance in this study is the derivative of substrate charge with respect to gate voltage, as expressed by Eq. (13), the substrate charge as a function of gate voltage is investigated in the supplementary material to help understand the LF *C–V* characteristics of the capacitors with deep dopants, as investigated herein.

To a certain extent, actual *p*-type diamonds contain nitrogen as impurities that act as donors, as discussed earlier. To investigate the effect of this compensation, Fig. 4 shows the *C–V* characteristics of diamond MIS capacitors containing boron and nitrogen as acceptors and compensating donors, respectively. In the simulations, the net acceptor concentration, $N_A - N_D$, was maintained constant (1×10^{17} cm^{-3}) because the dopant concentration in the substrate is often estimated using the *C–V* characteristics of

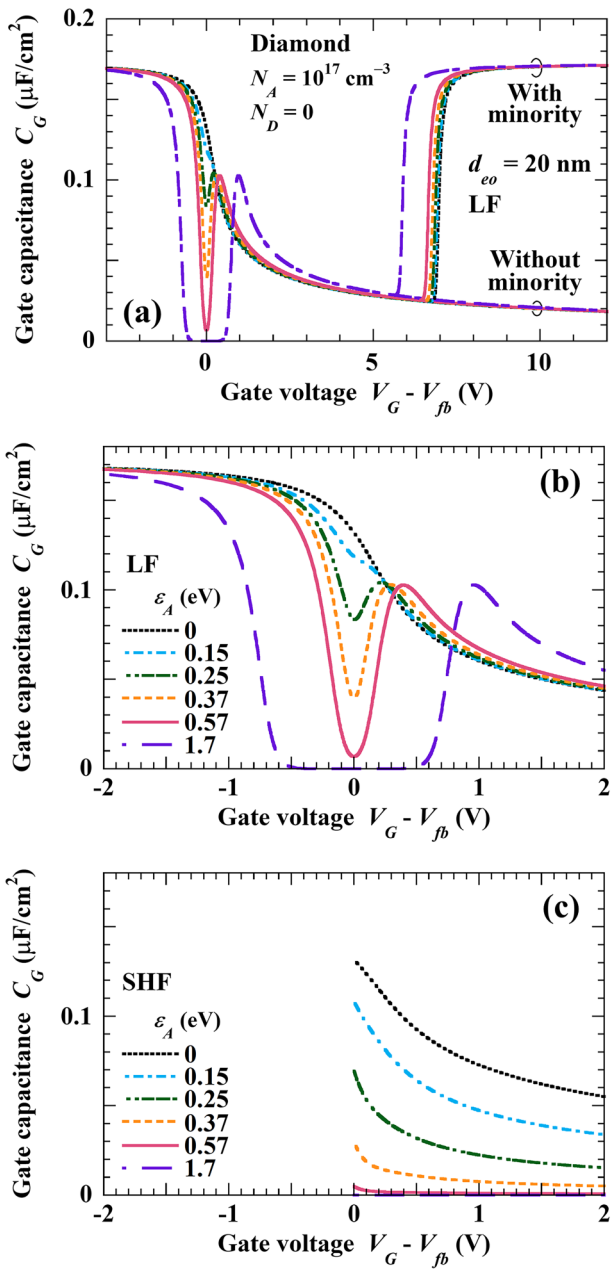

FIG. 3. Theoretical *C*–*V* characteristics of *p*-type diamond MIS capacitors for various activation energies of acceptors. Concentration of acceptors was assumed to be 1×10^{17} cm^{-3}. The donor concentration and EOT of the gate insulator were equal to those considered in Fig. 2. Here, ε_A represents the activation energy of acceptors, as given by $\varepsilon_A = E_A - E_V$. Figures 3(a)–3(c) show the results for LF and SHF modulations, similar to Figs. 2(a)–2(c).

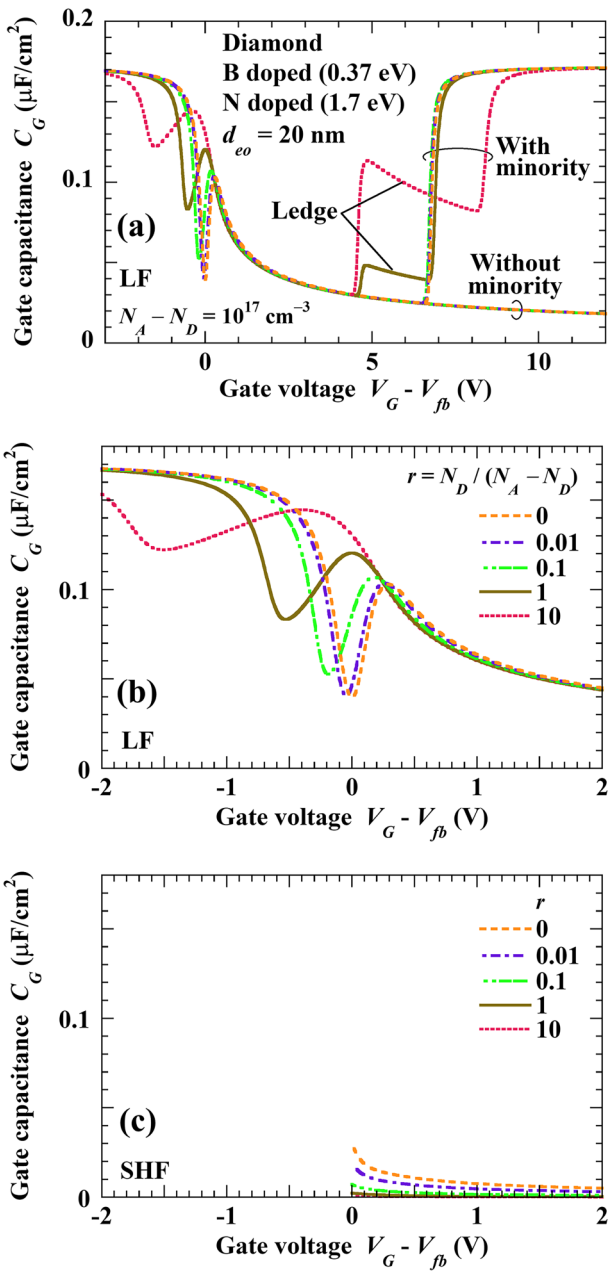

FIG. 4. Theoretical *C*–*V* characteristics of B-doped diamond MIS capacitors for various compensation ratios. Nitrogen was assumed as the donor, and the net acceptor concentration was set at 1×10^{17} cm^{-3}. Similar to those in Figs. 2 and 3, the same EOT of gate insulator was considered, and Figs. 4(a)–4(c) show the results for LF and SHF modulations.

capacitors, and the estimated concentration is the net value (Sec. III F). The ratio $r \equiv N_D/(N_A - N_D)$ (called compensation ratio) of the donor concentration to the net acceptor concentration ranged from 0.01 to 10. Figures 4(a)–4(c) show the results for LF and SHF modulations, similar to Figs. 2(a)–2(c) and 3(a)–3(c). For comparison, the result for no compensation is also shown, indicated by the middle-dashed lines (orange), which were reproduced from Figs. 2 and 3. The LF *C*–*V* characteristics differed according to

donor concentration, even for the same net acceptor concentration. The dip specific to the deep dopants shifts negatively and widens with the donor concentration, whereas the minimum capacitance at the dip increases with the donor concentration. By contrast, the LF capacitance for high gate voltages remains almost constant, regardless of the degree of compensation, except for the inversion components. Characteristically, a ledge is observed in the inversion components instead of a dip near the flatband. This ledge was formed in the following way. As the gate voltage increased, the donors in the vicinity of the interface became located at the Fermi level for a certain gate voltage, and responded to the AC modulation, yielding an increase in the capacitance. With further increasing gate voltage, the front in which the donor level coincided with the Fermi level proceeded from the interface into the bulk, continuing to enhance the capacitance. However, because the front became deeper, the degree of the capacitance enhancement reduced. Hence, the negatively sloped ledge was formed. As expected from this mechanism, the ledge height increases with the compensation ratio, whereas the gate voltage for the ledge appearance is almost maintained at the value for which the donor level at the interface is located at the Fermi level, regardless of the compensation ratio. The ledge disappears when the CBM at the interface reaches the Fermi level and produces inversion electrons, which abruptly increase the capacitance. The ledge-appearance gate voltage increases if the activation energy of the donors diminishes (not presented). In stark contrast to the LF C–V characteristics for shallow dopants, which are solely determined by the net dopant concentration, the aforementioned significant variation in the dip with the compensation ratio indicates that the MISFETs formed on deep-dopant semiconductors cannot be solely characterized by the net dopant concentration.

The SHF capacitance, shown in Fig. 4(c), decreased with the compensation ratio owing to the reduced hole concentration, as discussed herein. The hole concentration in the bulk material as a function of the net acceptor concentration and compensation ratio is depicted in Figs. 5(a) and 5(b), respectively, where the acceptor was assumed to be boron and the results were not influenced by donor choice. As shown in Fig. 5(b), even when the net acceptor concentration was maintained constant, the hole concentration decreased with the compensation ratio, thereby reducing the SHF capacitance, as presented in Fig. 4(c). Regardless of the net acceptor concentrations, the hole concentration remarkably converged to the same value, and it was inversely proportional to the compensation ratio. This relation, represented by the dotted line (black) in Fig. 5(b), is obtained as $p_{p0} = \tilde{N}_V/r$ by estimating the extreme form of Eq. (7) to the limit of a high compensation ratio. These results demonstrate the significance of reducing the compensating dopants in the fabrication of MIS devices formed on deep-dopant semiconductor substrates. By contrast, for small compensation ratios, the hole concentration is solely determined by the net acceptor concentration, regardless of the compensation ratio, and it is considerably smaller than the net acceptor concentration because of the deep acceptor level, as shown in Fig. 5(a). Except for the low net acceptor concentrations, the hole concentration for small compensation ratios can be derived as $p_{p0} = \sqrt{\tilde{N}_V(N_A - N_D)}$ (dotted-straight line in Fig. 5(a), black), as confirmed using Eq. (7).

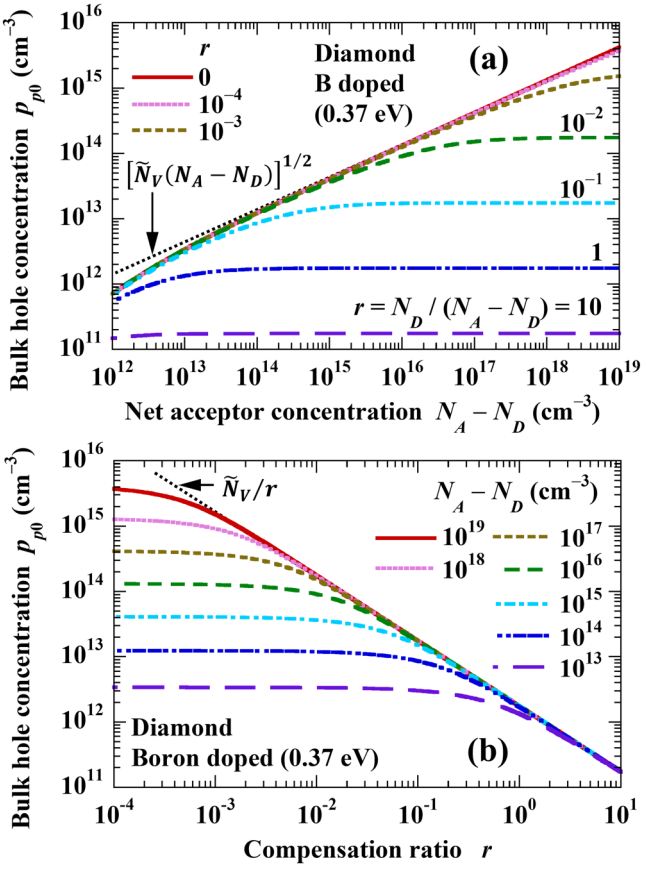

FIG. 5. Bulk hole concentration in a B-doped diamond as a function of (a) net acceptor concentration and (b) compensation ratio. The results are independent of donor types.

F. Validity of depletion layer approximation

As the past investigations of the electrical characteristics of MIS capacitors and MISFETs are significantly based on the depletion layer approximation (DLA) developed for shallow dopants, the validity of its application to deep-dopant semiconductors is investigated herein. In a p-type substrate, except for a small v that renders $f_A(v)$ slightly or appreciably less than 1, the charge density is approximately equal to $-q(N_A - N_D)$, as confirmed using Eqs. (2)–(8). Therefore, DLA also applies to semiconductors with deep dopants, and thereby, the differential capacitance method (DCM) of estimating a dopant or carrier distribution in the substrate has been validated for deep dopants. This method was originally developed for pn junctions[45,46] and was later applied to MIS capacitors.[47] Notably, the original equation for pn junctions can be applied to MIS capacitors without any modification, thereby yielding an estimate of the net dopant or majority carrier concentration N_{CV}, expressed as

$$N_{CV} = \frac{2}{q\varepsilon_S}\left(\frac{dC_G^{-2}}{dV_G}\right)^{-1}. \tag{31}$$

The value computed using this equation was originally considered to be the concentration of dopants;[45] however, it was later found to be more consistent with the concentration of carriers than that of dopants.[46] To investigate the case with deep dopants, diamond was assumed as the substrate, and the concentrations estimated using DCM and the hole concentrations at the flatband are compared in Fig. 6, as indicated by the solid and dashed lines, respectively. The hole concentrations and the C–V characteristics for the DCM analysis were theoretically prepared using a commercial device simulator (Atlas, SILVACO), assuming the acceptor distribution, as denoted by the dashed-dotted line in the figure (black). The results not only for boron but also for virtual acceptors with an activation energy of 0 eV, for comparison, are presented in Fig. 6, indicated by thin (orange and magenta) and thick (light blue and dark blue) lines, respectively. For an activation energy of 0 eV, the concentration estimated by DCM (thick solid line, dark blue) was almost similar to the hole concentration (thick dashed line, light blue), in accordance with the aforementioned DCM interpretation for shallow dopants. The concentration estimated for the activation energy of 0.37 eV (boron) by DCM (thin solid line, magenta) is quite similar to that for shallow acceptors, and it is considerably larger than the hole concentration (thin dashed line, orange). Therefore, the concentration estimated for deep dopants by DCM predominantly reflects the dopant concentration, in stark contrast to that for shallow dopants. These apparently contradictory results can be explained as follows. The shallow dopants were almost completely ionized in the depleted and neutral regions without varying their charge during AC modulation for capacitance measurements. Therefore, the charge responding to the AC modulation comprised carriers that were mostly located at the front of the depletion layer. Thus, the concentration estimated using the differential method represented the carrier concentration at the depletion layer edge. By contrast, most deep dopants located at the edge of the depletion layer were not ionized and the carrier concentration was smaller than the dopant concentration by more than several orders of magnitude. Therefore, the substrate-charge variation induced by AC modulation is typically caused by the ionization/neutralization of dopants. Hence, DCM yields an approximate distribution of deep dopants. In summary, the DCM yields the concentrations of carriers and dopants in case the dopants at the depletion layer edge are completely ionized and not ionized, respectively. As such, DCM yields a net concentration when both types of dopants coexist. Notably, the presence of accumulations of holes/acceptors in the DCM estimates in the vicinity of the interface is observed, unlike the simulated holes for both activation energies. These peaks are artifacts resulting from the error of the DLA, which was assumed to develop DCM, as the error margin of the DLA is known to increase toward the flatband voltage, i.e., for small v. Moreover, for the small v, the carrier distribution in the vicinity of the interface varies considerably with the gate voltage. Because of these reasons, the DCM yielded no physically significant results in the vicinity of the interface, even for shallow dopants. Therefore, the two-dimensional hole gas induced under a hydrogen-terminated diamond surface was not adequately characterized by this method, contrary to the claims of previous studies.[48,49] The SHF C–V characteristics cannot be analyzed by the differential method, as DCM assumes the thermal equilibrium for the instantaneous values of the AC-modulated gate voltage, which is not realized for SHF.

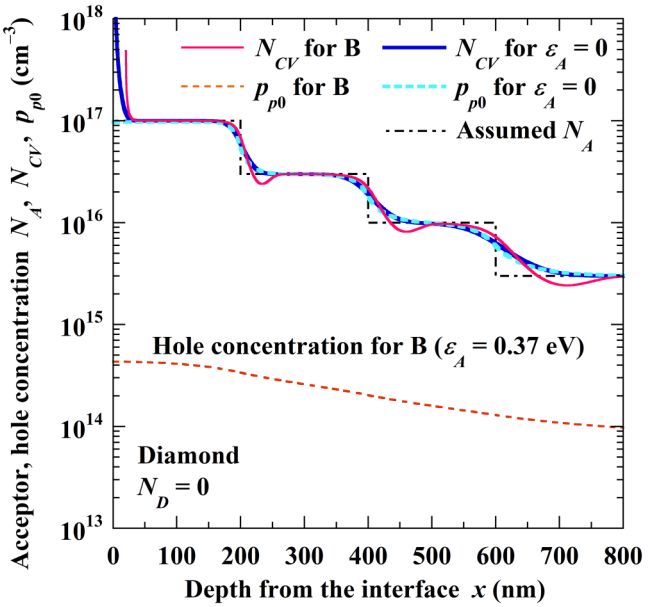

FIG. 6. Comparison between simulated hole concentrations and hole/acceptor concentrations estimated using DCM for p-type diamond. Hole concentrations represented by the dashed lines were evaluated using a commercial device simulator (Atlas, SILVACO) assuming a flatband at the interface and the acceptor distribution, represented by dashed-dotted line (black in color printing). Hole/acceptor concentrations were estimated using DCM based on C–V characteristics numerically produced by the simulator, assuming the aforementioned acceptor distribution. In addition to the results for boron of an activation energy ε_A of 0.37 eV (thin lines, orange and magenta), those for acceptors of $\varepsilon_A = 0$ eV (thick lines, light and dark blue) are presented for comparison. As clearly shown in this figure, the estimates using the DCM yielded the distributions of majority carriers (holes) and dopants (acceptors) for shallow and deep dopants, respectively. Accumulations of holes/acceptors in the estimates using DCM might be noticed at the vicinity of the interface, unlike simulated holes for both activation energies. These peaks resulted from the error of DLA, which was assumed to develop DCM, as the error margin of DLA is known to increase toward the flatband. Furthermore, theoretically, the carrier distribution at the vicinity of the interface varies with gate voltage. Therefore, DCM yields no physically significant results in that region, even for shallow dopants.

In the application of DLA, the capacitance should be measured using an HF modulation to suppress the effect of interface states. Nevertheless, as the stretch-out is inevitable as mentioned earlier, the results obtained by DCM are influenced by the interface states. To investigate this phenomenon, Eq. (31) can be rewritten as

$$N_{CV,it} = \frac{2}{q\varepsilon_S}\left(\frac{dC_G^{-2}}{dV_{G,0}}\right)^{-1}\frac{dV_G}{dV_{G,0}} = \frac{2}{q\varepsilon_S}\left(\frac{dC_G^{-2}}{dV_{G,0}}\right)^{-1}\frac{dV_G/d\psi_s}{dV_{G,0}/d\psi_s},$$

where $V_{G,0}$ is the gate voltage for the no-interface-state case expressed in Eq. (16). As the correct concentration $N_{CV,0}$ is obtained for $V_{G,0}$, the concentration $N_{CV,it}$ expressed by this

equation can be further reduced using Eq. (27) to

$$N_{CV,it} = \left(1 + \frac{C_{it}}{C_{ins} + C_S}\right) N_{CV,0}. \quad (32)$$

Significantly, the term in the parentheses is identical to that for the subthreshold swing of MISFETs.[1] As the presence of interface states is inevitable in actual capacitors, the DCM might seem useless. However, this is not the case. The interface states for deep depletion, i.e., for $\psi_s > 0.7$ V in a p-type substrate, do not follow the sweep of the gate voltage, let alone the HF modulations.[44] Therefore, the interface-state charge should remain unchanged for the gate voltages of deep depletion. Thus, as C_{it} is negligibly small, the DCM yields accurate results even in the presence of interface states if the analysis is performed for deep depletion. However, this result suggests the possibility of a large error margin caused when the method is applied to narrow-bandgap semiconductor MIS capacitors that contain an appreciable number of interface states, because the deep depletion cannot be realized owing to the narrow bandgap.

When the dopants are uniformly distributed in the substrate, the integral form of Eq. (31) can be derived for $v_s > 12$ ($\psi_s > 0.3$ V at 296 K) in a p-type substrate without using DLA (refer to the Appendix), yielding

$$\frac{1}{C_G^2} - \frac{1}{C_{ins}^2} = \frac{2}{\varepsilon_S q(N_A - N_D)}[V_G - (V_{fb,0} - Q_{it}/C_{ins} + \delta\psi_p)], \quad (33)$$

where $\delta\psi_p$ is expressed as

$$\delta\psi_p = \frac{p_{p0} - N_A \ln f_A(0)}{(N_A - N_D)\beta q} = \frac{kT}{q}\frac{p_{p0} - N_A \ln f_A(0)}{(N_A - N_D)}. \quad (34)$$

For shallow acceptors, as $p_{p0} \sim N_A - N_D$ and $f_A(0) \sim 1$, $\delta\psi_p$ approximately equals $1/(\beta q) = kT/q$, consistent with previous results.[33] The term $\delta\psi_p$ was neglected in previous studies[23,28] except for a study[50] that assumed the value for shallow dopants. Similarly, for $v_s < -12$ ($\psi_s < -0.3$ V at 296 K) in an n-type substrate, we can derive

$$\frac{1}{C_G^2} - \frac{1}{C_{ins}^2} = -\frac{2}{\varepsilon_S q(N_D - N_A)} \times \left\{V_G - \left[V_{fb,0} - Q_{it}/C_{ins} - \frac{n_{n0} - N_D \ln f_D(0)}{(N_D - N_A)\beta q}\right]\right\}. \quad (35)$$

A few examples of $\delta\psi_p$ for B-doped diamond as a function of the net boron concentration and compensation ratio are shown in Figs. 7(a) and 7(b), respectively. For small compensation ratios of at most 0.01, this term has a magnitude of at least 0.1 on practically doped substrates. Therefore, it should not be neglected. However, this is negligible for shallow dopants in nondegenerate semiconductors.

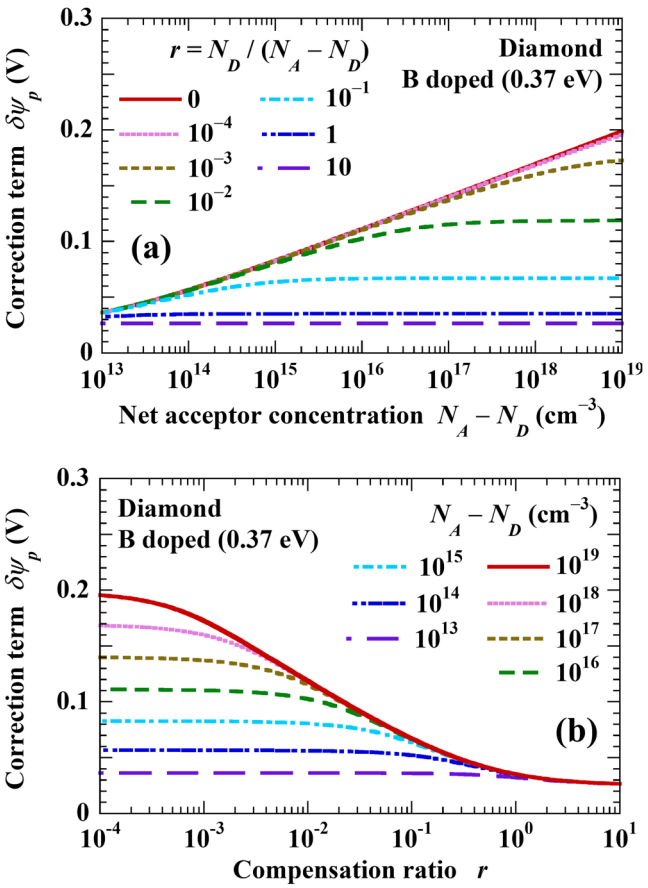

FIG. 7. Common correction terms for surface potential and interface-state-free flatband voltage estimated using DLA and MS plots, respectively, as a function of (a) net acceptor concentration and (b) compensation ratio. Results of B-doped diamond are presented here. $\delta\psi_p$ is given by Eq. (34).

IV. EXPERIMENTAL RESULTS

Figure 8 shows the C–V characteristics of the Au/Al_2O_3/H-terminated B-doped diamond capacitor measured at modulation frequencies of 1 Hz to 1 MHz from accumulation to depletion with a voltage step of 0.1 V. The EOT of the gate insulator was estimated as 17.2 nm by fitting the theoretical C–V characteristics to the 1 MHz result (double-dashed two-dotted line, red) for deep accumulation. As expected from Figs. 2–4, a dip specific to deep dopants was distinctly observed even at 1 MHz. The net boron concentration was estimated as a function of depth from the interface using DCM, as represented by the solid line in Fig. 9. This is consistent with the boron depth profile measured using SIMS for depths of 100–170 nm, averaging 5.7×10^{16} cm^{-3}. This excellent agreement assures that most boron atoms certainly follow the 1 MHz modulation, which validates the application of the LF and HF equations developed in this study. As the compensating nitrogen concentration was not remarkably different from the detection

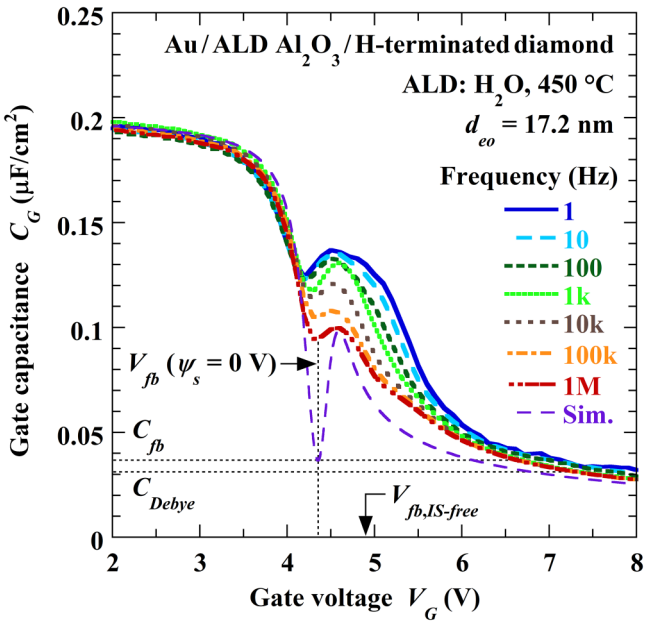

FIG. 8. Experimental *C–V* characteristics of Au/Al_2O_3/H-terminated diamond capacitor. Thick lines represent the experimental results for modulation frequencies from 1 Hz to 1 MHz. The thin line (long dashed, purple) represents the theoretical result obtained using the derived equations, assuming the same gate insulator thickness (EOT) and boron concentration as those estimated using the 1 MHz characteristic displayed herein. Specifically, the EOT of the gate insulator was 17.2 nm, and the net boron concentration was 5.7×10^{16} cm^{-3} as estimated in Fig. 9. Additionally, the donor concentration was assumed as 0 cm^{-3}, the effect of interface states was neglected, and the flatband voltage was 4.353 V, which was estimated based on Eq. (37) following the conventional definition, i.e., gate voltage for $\psi_s = 0$ V. $V_{fb,IS\text{-}free}$ denotes the interface-state-free flatband voltage estimated using an MS plot for deep depletion. Upper and lower thin horizontal dotted lines represent flatband capacitances for deep and shallow dopants, respectively. Both yielded considerably erroneous flatband voltages when applied to the analysis of actual diamond capacitors, owing to the missing or considerably shallow dip. Notably, the flatband capacitance for deep dopants should be calculated using the carrier (hole) concentration instead of the dopant concentration.

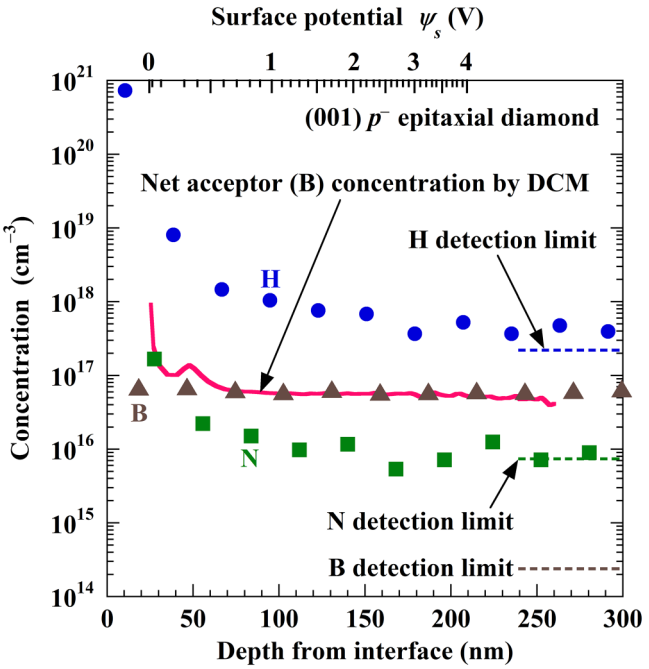

FIG. 9. Impurity distributions in the diamond substrate used for fabricating MIS capacitors in this study. Symbols represent impurity concentrations measured by SIMS. For comparison, solid line (red) represents the net acceptor concentration estimated using DCM with 1 MHz *C–V* characteristic, as shown in Fig. 8. For reference, as displayed on the second *x*-axis, the surface potential for the depth was estimated using Eq. (37) and the 1 Hz *C–V* characteristic, as shown in Fig. 8.

limit (green dashed line), which was approximately one order of magnitude smaller than the boron concentration, the compensation ratio should be less than 0.1. The increasing concentrations of hydrogen and nitrogen toward the interface were supposedly caused by the contaminants present on the SIMS sample surface. For comparison, we simulated a theoretical *C–V* characteristic for the aforementioned gate insulator thickness and boron concentration (no compensation), assuming no interface states, as represented by the thin long-dashed line (purple) in Fig. 8. The flatband voltage, that is, the dip extremity, was set at 4.353 V, which was estimated using the method described later. For shallow dopants, the flatband voltage has conventionally been estimated as the gate voltage that yields the flatband capacitance C_{fb}, expressed in Eqs. (17) and (21). For boron-doped diamond, the flatband capacitance (thin upper-horizontal dotted line in Fig. 8, black) evaluated using the aforementioned gate-insulator thickness and boron concentration was equal to the capacitance of the dip extremity in the theoretical *C–V* characteristic, thereby yielding a flatband voltage that is equal to the value assumed in the simulation. However, the actual 1 MHz *C–V* characteristic exhibits a much shallower dip owing to the reason discussed in Sec. V. Therefore, this flatband capacitance method fails. Specifically, the gate voltage for the flatband capacitance is 6.665 V, which differs from the flatband voltage by more than 2 V. In a worse case, the flatband capacitance for shallow dopants, which is provided by the Debye length capacitance C_{Debye} (horizontal thin-dotted line in the lower portion of Fig. 8, black), was erroneously adopted in previous studies,[23,51] which caused a larger error margin. In the studies, the flatband capacitance was evaluated based on the Debye length that was calculated erroneously using the acceptor concentration[23] and 2DHG hole concentration[51] instead of the bulk hole concentration, and therefore, the flatband capacitance was doubly mistaken.

An accurate estimation of the flatband voltage was achieved using the surface potential estimated using the Berglund integration method.[52] The challenging task for the method is to set the indeterminate integral constant. To resolve this problem, we select an arbitrary gate voltage $V_{meas,dep}$ in an experimental *C–V* characteristic for deep depletion, wherein the interface states do not respond to either AC modulation or scanned bias voltage. Thereafter, using

the DLA and capacitance $C_{meas,dep}$ for this $V_{meas,dep}$, the surface potential $\psi_{meas,dla}$ for the $V_{meas,dep}$ is approximately estimated as follows:

$$\psi_{meas,dla} = \frac{\varepsilon_S q(N_A - N_D)}{2}\left(\frac{1}{C_{meas,\,dep}} - \frac{1}{C_{ins}}\right)^2. \quad (36)$$

As it is shifted from the actual value by $\delta\psi_p$ (appendix), the surface potential for any gate voltage, including those for other than deep depletion, is obtained by performing the Berglund integration as follows:

$$\psi_s(V_G) = \int_{V_{meas,dep}}^{V_G}\left(1 - \frac{C_{meas,LF}}{C_{ins}}\right)dV_G + \psi_{meas,dla} + \delta\psi_p. \quad (37)$$

Significantly, the LF capacitance is used herein. Therefore, this equation applies to actual capacitors with interface states. Based on this equation, the flatband voltage was estimated as the gate voltage for which $\psi_{meas}(V_G)$ equals 0, specifically, 4.353 V, as indicated by the vertical dotted line in Fig. 8. This value is approximately equal to the gate voltage of 4.27 V for the dip extremity in the 1 MHz characteristic (Fig. 8). Nonetheless, it exhibited a marginal positive shift, and the cause of this shift is discussed in Sec. V.

The interface-state density of a capacitor estimated by any capacitance method denotes the value for the interface states that are located at the Fermi level under the applied bias voltage, as discussed earlier. Therefore, their energy with respect to that of the VBM is expressed as $E_{it} - E_{V,s} = E_F - E_{V,s} = q\psi_s + (E_F - E_{V,0})$. The term $E_F - E_{V,0}$ is expressed in Eq. (11) and specifically shown for B-doped diamond as a function of the net acceptor concentration and compensation ratio in Figs. 10(a) and 10(b), respectively. Thus, using the aforementioned $\psi_s(V_G)$ [Eq. (37)] and the high–low frequency method[53] as formulated,

$$D_{it} = \frac{1}{q^2}\left(\frac{1}{1/C_{LF} - 1/C_{ins}} - \frac{1}{1/C_{HF} - 1/C_{ins}}\right), \quad (38)$$

the interface-state density of the aforementioned capacitor was estimated as a function of the interface-state energy, $E_{it} - E_{V,s}$. The result is represented by the symbols in Fig. 11, where the 1 Hz and 1 MHz C–V characteristics (Fig. 8) were used and $E_F - E_{V,0}$ was estimated as 0.282 eV for the aforementioned B concentration. For reference, the surface potential corresponding to the interface-state energy is denoted on the second x-axis. For $E_{it} - E_{V,s} > E_F - E_{V,0}$, the interface-state density remained approximately constant at $1.4 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ and exponentially decreased with $E_{it} - E_{V,s} > 0.5$ eV, eventually to the level below the detection limit of the high–low frequency method for $E_{it} - E_{V,s} > 1$ eV. The surface potential for this threshold $E_{it} - E_{V,s}$ (1 eV) is approximately equal to 0.7 V, and it corresponds to the depth below which the net acceptor concentration by DCM increases with the diminishing depth (Fig. 9). Based on this correspondence, the enhancement of the net acceptor concentration for depths <80 nm (Fig. 9) is considered to be an artifact resulting from the interface states, as expected in Eq. (32). The dip observed below $E_F - E_{V,0}$ in Fig. 11 might be only apparent and was supposedly caused by the shift in C–V characteristics during the measurements because the capacitance for those surface potentials abruptly changed with the gate voltage and, therefore, even a marginal shift produces a large error margin in the estimated interface-state densities. The exponential reduction in the interface-state density for $E_{it} - E_{V,s} > 0.5$ eV is also likely to be apparent, as the response of those interface states—even to LF modulations—considerably decelerates with the interface-state energy. The interface-state density of the Au/Al_2O_3/H-terminated diamond capacitor thus estimated was slightly smaller than $2 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ for an Au/Al_2O_3/SiO_2/Si-terminated diamond capacitor.[28] A meaningful comparison with the other previous results will be made after re-examining them using advanced methods for interface characterization, such as our proposed methods.

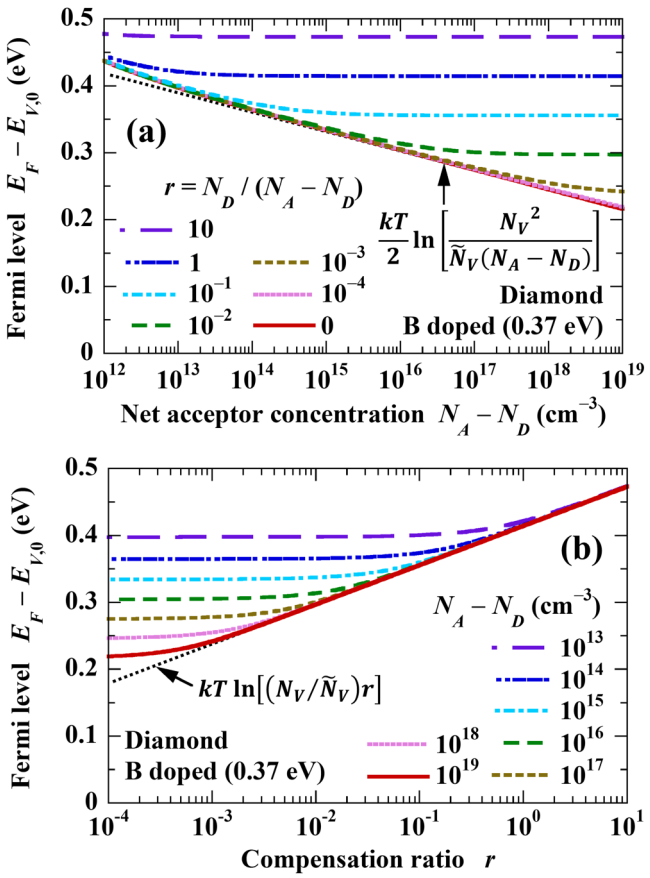

FIG. 10. Fermi level in B-doped diamond as a function of (a) net acceptor concentration and (b) compensation ratio. The values with respect to the VBM energy are shown.

For deep depletion (i.e., $\psi_s > 0.7$ V at 296 K), the interface-state charge keeps constant and, therefore, as confirmed using Eq. (33), a graph displaying $C_G^{-2} - C_{ins}^{-2}$ as a function of V_G, called the Mott–Schottky (MS) plot, can be fitted by a linear function, which provides $V_{MS} = V_{fb,0} - Q_{it,dep}/C_{ins} + \delta\psi_p$ at the intersection with V_G-axis, where $Q_{it,dep}$ is the interface-state charge for the deep

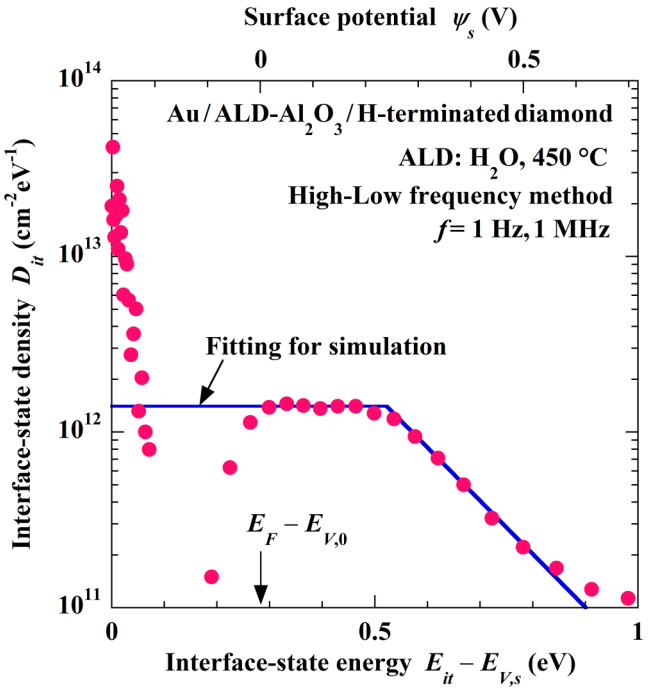

FIG. 11. Interface-state-density distribution in the Au/Al_2O_3/H-terminated diamond capacitor. Interface-state density was estimated by high–low frequency method employing 1 Hz and 1 MHz C–V characteristics, as shown in Fig. 8. Surface potential was estimated following the same approach as that in Fig. 9 and the interface-state energy is expressed as $E_{it} - E_{V,s} = q\psi_s + (E_F - E_{V,0})$, where $E_F - E_{V,0}$ was estimated as 0.282 eV. Solid line represents interface-state-density distribution assumed in the undermentioned simulations.

depletion. Using this V_{MS}, the interface-state charge for deep depletion is obtained as

$$Q_{it,dep} = C_{ins}(V_{fb,0} - V_{MS} + \delta\psi_p) \text{ (for } p\text{-type substrate)}. \quad (39)$$

As there is no distinction between this deep-interface-state charge and the insulator charge as mentioned earlier, we regard the value estimated in Eq. (39) as the insulator charge, similar to previous studies.[23,28] In this case, $V_{fb,IS\text{-}free} \equiv V_{fb,0} - Q_{it,dep}/C_{ins}$ is the flatband voltage of a virtual capacitor empty of the interface states and experimentally estimated as $V_{fb,IS\text{-}free} = V_{MS} - \delta\psi_p$, where the term $\delta\psi_p$ was neglected in previous studies.[23,54] As suggested in Fig. 9, the MS plot of the 1 MHz C–V characteristic (Fig. 8) was precisely fitted by a linear function (not shown) for gate voltages of 6.4–8.4 V, wherein the depth ranged from 100 to 170 nm, yielding an estimated V_{MS} of 4.999 V, where N_D was assumed as 0 cm^{-3}. For this value and $\delta\psi_p = 0.133$ V, $V_{fb,IS\text{-}free}$ equals 4.866 V and the insulator charge was estimated as -4.6×10^{12} cm^{-2} in units of q using Eqs. (15) and (39), where $E_F - E_{V,0}$ was 0.282 eV as mentioned earlier, and W_G (Au) and χ_S (H-terminated diamond) were assumed as 5.1[55,56] and −1.3 eV,[57,58] respectively. This negative charge has a sufficiently large magnitude to induce 2DHG,[59] which is caused by the negative charge regardless of its origin. As the Al_2O_3 gate insulator in this study was formed at 450 °C, the negative charge was induced by Al_2O_3 and not by airborne adsorbates, which is consistent with previous studies reporting the same effect.[60,61]

V. DISCUSSION

The dip observed in the 1 MHz C–V characteristic (double dashed-double dotted line in Fig. 8, red) is much shallower than theoretically expected (thin long-dashed line, purple). Although it was rather unclear, a similar dip was observed in the C–V characteristics of an MIS capacitor formed on a Si-terminated diamond substrate.[28] Therefore, the presence of the dip is not specific to the hydrogen termination applied in this study. The model simulations of C–V characteristics (Fig. 3) suggest that the energy level of boron was reduced in the samples exhibiting a shallow dip. Notably, the experimental 1 MHz result represented by the symbols in Fig. 12 was appropriately fitted by a theoretical C–V characteristic, as represented by the thick solid line (black) in Fig. 12. For reference, this experimental result was identical to the 1 MHz result in Fig. 8, and the theoretical result was simulated assuming the activation energy of acceptors and the insulator charge in units of q as 0.23 eV and -4.0×10^{12} cm^{-2}, respectively. Moreover, the acceptor and donor concentrations including the gate insulator thickness were assumed as the same as those used for the theoretical characteristic shown in Fig. 8. Similar to Figs. 2–4, a magnified image of Fig. 12(a) is shown in Fig. 12(b). The effect of the interface states was reflected in the simulations assuming the interface-state distribution (solid line in Fig. 11) and using Eqs. (27) and (30). The magnitude of the aforementioned insulator charge assumed in the simulations was slightly less than that of the value -4.6×10^{12} cm^{-2} estimated based on the interface-state-free flatband voltage. This mismatch indicates that the interface-state density (Fig. 11) might be underestimated owing to the possible presence of fast interface states responding to 1 MHz modulation. Although the simulation accurately reproduced the experimental characteristic, the activation energy of the acceptors did not potentially reduce in the entire substrate. Thereafter, assuming that the reduction in the activation energy of the acceptors is restricted to the vicinity of the interface [inset in Fig. 12(a)], the C–V characteristics were simulated for low-activation-energy-layer (LAEL) thicknesses d_A of 5–50 nm (lines in Fig. 12). For comparison, the C–V characteristic for an activation energy of 0.37 eV ($d_A = 0$) is indicated by the thin long-dashed line (purple) in Fig. 12(b). This was identical to the theoretical characteristic shown in Fig. 8 (the same representation), excluding the variations in the flatband voltages. Except for activation energies, the simulation conditions in Fig. 12 were the same as those for 0.23 eV, as mentioned earlier. Even when LAEL was thin [$d_A = 5$ nm, thin solid line in Fig. 12(b), light blue], the dip located at $V_G = 4.41$ V disappeared and another dip appeared at $V_G = 4.34$ V instead, thereby increasing the bottom capacitance with LAEL thickness. The gate voltages corresponding to the locations of the former and latter dip extremities were approximately equal to the flatband voltages for acceptors with uniform activation energies of 0.37 ($d_A = 0$ nm) and 0.23 eV ($d_A = \infty$ nm), respectively. As shown in Fig. 12, when the activation energy reduced in a

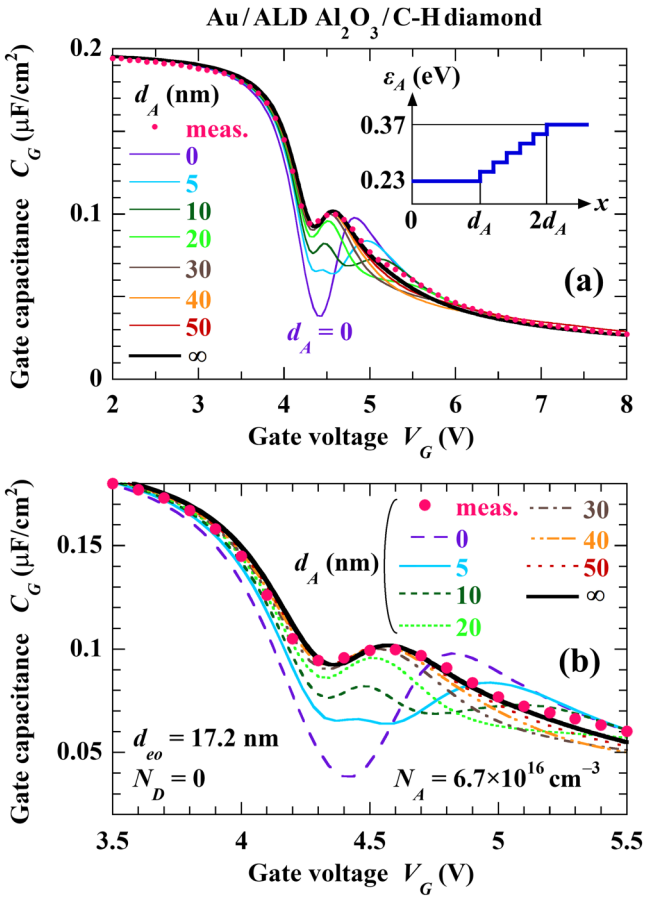

FIG. 12. Theoretical *C–V* characteristics of MIS capacitors formed on diamond substrates with LAEL. *C–V* characteristics represented by lines were simulated using the aforementioned device simulator, assuming the presence of LAEL with the acceptor distribution shown in the inset of Fig. 12(a). In the simulations, the gate work function, gate insulator thickness, and the electron affinity and dopant concentrations in the substrate were assumed to be the same as those of real capacitors. However, the insulator charge was assumed as -4.0×10^{12} cm^{-2} to achieve the best agreement of the *C–V* characteristics between the experiment for 1 MHz (symbols) and the simulation for the entirely reduced activation energy ($d_A = \infty$ nm, thick solid line, black). The influence of interface states was considered in the simulations, using Eqs. (27) and (30) and assuming aforementioned interface-state distribution profile (solid line in Fig. 11). As earlier, Fig. 12(b) is a magnified image of (a).

region extending for more than 40 nm (double-dashed two-dotted line, orange), the *C–V* characteristics did not significantly vary from that for the entirely low activation energy (thick solid line, black). This threshold thickness is equal to the extrinsic Debye length for the acceptors that have the reduced activation energy (0.23 eV) and the estimated acceptor concentration mentioned earlier (5.7×10^{16} cm^{-3}). This agreement is not a coincidence because, at flatband, a small modulation imposed on the gate for capacitance measurements only influences the substrate region located within the extrinsic Debye length from the interface. To the best of our knowledge, this type of reduction in the activation energy of boron has not been observed previously. Nevertheless, this should not be dismissed, as the area concentration of the holes additionally generated by the presence of a 50-nm-thick LAEL was less than 3×10^{10} cm^{-2}, which is difficult to detect. Although the reason for the failure to observe the dip earlier remains unclear, the proposed LAEL model will contribute to answering this question.

The presence of the LAEL requires revision of the stated method to estimate the flatband voltages using Eq. (37), as investigated hereinafter. In this case, we neglected the presence of interface states for simplicity. To take the case of a 50-nm-thick LAEL as an example, the flatband voltage according to the conventional definition, that is, the gate voltage for a surface potential of 0 V, is 1.288 V, whereas the simulation for this LAEL yields a flatband voltage of 1.149 V. For reference, the flatband in the LAEL substrate is achieved when the derivative of the potential at the interface, i.e., the electric field, equals 0. Additionally, the electric field in an ideal

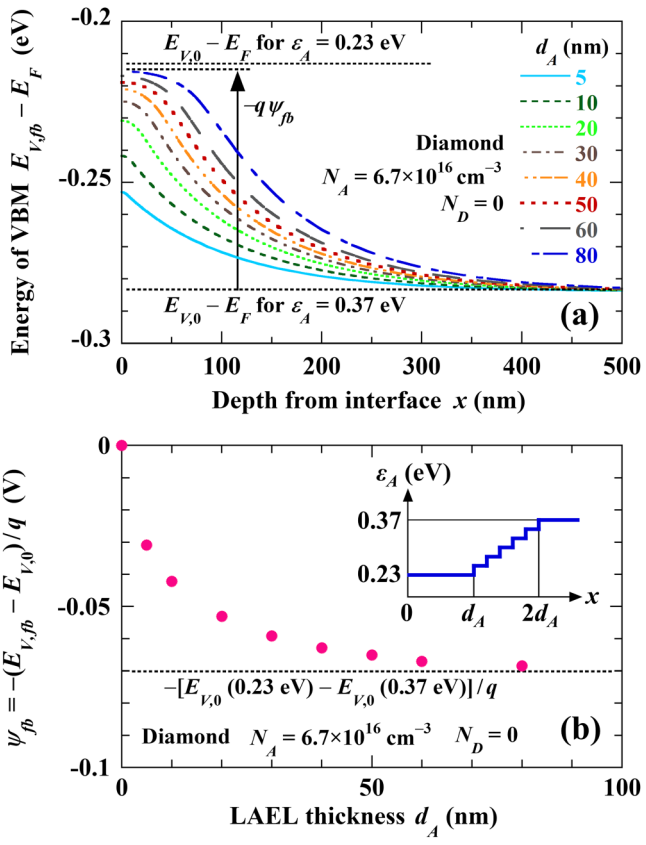

FIG. 13. Theoretical (a) depth distribution of VBM energy and (b) surface potential in B-doped diamond substrates with LAEL at flatband. Simulations were performed under the same conditions as those in Fig. 12. The values with respect to the Fermi level are shown in Fig. 13(a). As shown in Fig. 13(b), the flatband of LAEL substrates was achieved for the negative surface potential that is determined by LAEL thickness, instead of the conventional surface potential of 0 V.

gate insulator at the flatband vanishes. The aforementioned difference in flatband voltages is caused by the band bending in the vicinity of the interface at the flatband, as observed in Fig. 13(a), which depicts the simulated VBM energies with respect to the Fermi level for LAEL thicknesses of 5–80 nm. As shown in the figure, the VBM bends upward from the bulk toward the interface. Therefore, the surface potential at the flatband ψ_{fb} no more equals 0 V, as shown in Fig. 13(b), wherein ψ_{fb} is plotted as a function of the LAEL thickness. For reference, when the LAEL was depleted, there was no difference in the VBM bending between the substrates with and without the LAEL, as the space charge in the depletion layer, which determines the band bending, is not influenced by the dopant activation energy. For the 50-nm-thick LAEL stated earlier, ψ_{fb} equals −0.065 V, and the gate voltage for this value was estimated as 1.160 V, which approximately agrees with the aforementioned flatband voltage of 1.149 V. Therefore, in the presence of LAEL, the flatband voltage was more accurately estimated for ψ_{fb}. In the case of the experimental 1 MHz result shown in Figs. 8 and 12, the gate voltage for a surface potential of −0.03 V is equal to the value for the dip extremity, i.e., 4.27 V. The LAEL thickness for this value is ∼5 nm. Although the theoretical C–V characteristic for this LAEL thickness fit the experimental result only modestly, as shown in Fig. 12, the assumption of the presence of the LAEL improves the fitting accuracy. Therefore, this further supports the reduction in the boron activation energy in the vicinity of the interface. In future, studies should be conducted to detect LAEL and clarify the mechanism of LAEL formation, including the investigation of other models.

VI. CONCLUSIONS

This study successfully formulated the C–V characteristics of the MIS capacitors formed on a semiconductor substrate with deep and compensating dopants using elementary functions suitable for physical investigations and simulations. Subsequently, the methods for accurately estimating the interface-state-free flatband voltage and surface potential for deep depletion using an MS plot and depletion layer approximation, respectively, were developed and incorporated into equations that were expressed as elementary functions of the dopant concentrations. In particular, the former enhanced the accuracy of the estimated insulator charge. Using the latter and the Berglund method, the method for accurately estimating the surface potential for any gate voltage was presented. The validity and effectiveness of the methodology in this study were confirmed through its application to the analysis of experimental C–V characteristics of an MIS capacitor formed on a boron-doped hydrogen-terminated diamond substrate. The HF C–V characteristic of the capacitor exhibited a prominent dip that is specific to deep dopants. However, the dip depth was considerably shallower than theoretically expected. This C–V characteristic was theoretically reproduced with excellent accuracy, assuming the presence of a surficial diamond layer that contains acceptors with an activation energy of 0.23 eV, which was less than the conventional value of 0.37 eV for boron, and has a thickness of at least the extrinsic Debye length (40 nm in this study). In the presence of this layer, the flatband of the capacitor was not achieved for the conventional surface potential of 0 V, but for that ranging from 0 to −0.07 V, depending on the thickness of the layer. Moreover, the lower limit of the surface potential was determined based on the dopant concentration. The flatband voltage of the aforementioned capacitor estimated by considering this effect was close to the dip extremity, corresponding to the approximate location of the flatband voltage determined by theoretical means. Based on the aforementioned interface-state-free flatband voltage, the insulator charge was estimated as -4.6×10^{12} cm^{-2} in units of q, and its magnitude was sufficiently large to induce 2DHG. Moreover, the interface-state density was 1.4×10^{12} cm^{-2} eV^{-1} for interface-state energies of 0.3–0.5 eV above VBM and decreased below 1×10^{11} cm^{-2} eV^{-1} for interface-state energies of at least 1 eV above VBM, which was caused by the limit of the capacitance method. Hence, the methodology developed in this study and the possible presence of LAEL will enhance the physics and engineering of diamond devices.

Finally, the methods developed in this study for accurate estimation of the insulator charge, flatband voltage, surface potential, and interface-state distribution of MIS capacitors formed on p-type deep-dopant substrates, such as B-doped diamonds, are summarized as follows:

(1) The measurement of the LF ($\lesssim$1 Hz) and HF ($\gtrsim$1 MHz) C–V characteristics of the capacitor was conducted.
(2) The net acceptor concentration was estimated using the slope of the MS plot [Eq. (33)] of the HF C–V characteristic for deep depletion, and the compensation ratio was estimated using SIMS.
(3) Based on the acceptor concentration estimated in (2), the bulk hole concentration and Fermi level $E_F - E_{V,0}$ were calculated using Eqs. (7) and (11), respectively.
(4) The insulator charge (deep-interface-state charge) was estimated using Eq. (39), where $V_{fb,0}$ and $\delta\psi_p$ were calculated using Eqs. (15) and (34), respectively, and V_{MS} is the gate voltage for which the aforementioned MS plot intersected the V_G-axis. In Eq. (34), $f_A(0)$ is given by Eq. (5) using the hole concentration evaluated in (3).
(5) An arbitrary gate voltage $V_{meas,dep}$ was selected for deep depletion in the HF C–V characteristic, and the tentative surface potential $\psi_{meas,dla}$ was estimated using the capacitance for this $V_{meas,dep}$ and DLA [Eq. (36)].
(6) Berglund integration was performed from $V_{meas,dep}$ to V_G using the LF C–V characteristic. With this integral, the surface potential ψ_s was given by Eq. (37) using $\psi_{meas,dla}$ and $\delta\psi_p$ obtained in (5) and (4), respectively.
(7) The interface-state density D_{it} was estimated as a function of V_G by the high–low frequency method [Eq. (38)] along with the LF and HF C–V characteristics. Using the Fermi level and ψ_s obtained in (3) and (6), respectively, D_{it} can be evaluated as a function of the interface-state energy $E_{it} - E_V = \psi_s + (E_F - E_{V,0})$.
(8) Based on ψ_s obtained in (6), V_{fb} was estimated as V_{meas} for $\psi_s = 0$. In the presence of LAEL, the surface potential at the flatband ψ_{fb} should be estimated, and the gate voltage for this ψ_{fb} should be interpreted as the flatband voltage. However, if a dip is observed in the HF C–V characteristic and compensation by donors is negligible, the location of the dip extremity yields an accurate estimate of the flatband voltage.

Similar methods were employed for n-type substrates.

SUPPLEMENTARY MATERIAL

See the supplementary material for the substrate charge (semiconductor charge), which yields the LF capacitance when differentiated with respect to the gate voltage.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Atsushi Hiraiwa: Conceptualization (equal); Data curation (equal); Formal analysis (lead); Investigation (equal); Methodology (equal); Software (lead); Validation (equal); Writing – original draft (lead); Writing – review & editing (lead). **Satoshi Okubo:** Conceptualization (equal); Data curation (equal); Investigation (equal); Methodology (equal); Validation (equal). **Masahiko Ogura:** Data curation (supporting). **Yu Fu:** Investigation (supporting); Methodology (supporting). **Hiroshi Kawarada:** Funding acquisition (lead); Investigation (supporting); Validation (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

APPENDIX: DERIVATION OF COMMON CORRECTION TERM FOR SURFACE POTENTIAL AND INTERFACE-STATE-FREE FLAT-BAND VOLTAGE

Here, we treat the case of non-ideal gate insulators for HF modulations. First, we investigated the error of the surface potential estimated via DLA. For $v_s > 12$ ($\psi_s > 0.3$ V at 296 K) in a p-type substrate, as $p \ll N_A$, $n \ll N_A$, $n_{p0} \ll N_A$, $e^{-v} \ll 1$, $f_A(v_s) \approx 1$, $f_D(v) \approx 1$, and $f_D(0) \approx 1$, the charge density in the substrate and the substrate electric field at the interface were approximately derived using Eqs. (2)–(4) and (20), as follows:

$$\rho_s(v_s) \approx -q(N_A - N_D), \tag{A1}$$

$$\hat{F}_s(v_s) \approx \mathrm{sign}(v_s)\sqrt{2/(\varepsilon_S\beta)}[-p_{p0} + N_A \ln f_A(0) + (N_A - N_D)v_s]^{1/2}, \tag{A2}$$

respectively. Equations (A1) and (A2) along with Eqs. (19) and (29) ($\partial\rho/v_s = 0$) relate the surface potential determined by the DLA to the actual value as follows:

$$\psi_{meas,dla} = \frac{\varepsilon_S q(N_A - N_D)}{2}\left(\frac{1}{C_{meas,\,dep}} - \frac{1}{C_{ins}}\right)^2$$

$$= \frac{\varepsilon_S q(N_A - N_D)}{2}\frac{1}{C_S^2} = \frac{\varepsilon_S q(N_A - N_D)}{2}\left(\frac{\hat{F}_s}{\rho_s}\right)^2, \tag{A3}$$

$$= \psi_s - \frac{p_{p0} - N_A \ln f_A(0)}{(N_A - N_D)\beta q} \quad (\because \psi_s = v_s/(\beta q)). \tag{A4}$$

Subsequently, we derived the integral form of the DCM. Based on Eqs. (18) and (A1), the substrate field $\hat{F}_s(v_s)$ can be expressed as a function of the substrate capacitance as follows:

$$\hat{F}_s(v_s) = q(N_A - N_D)/C_S. \tag{A5}$$

Additionally, the surface potential was obtained as a function of the substrate capacitance using Eqs. (A3) and (A4), as follows:

$$\psi_s = \frac{\varepsilon_S q(N_A - N_D)}{2}\frac{1}{C_S^2} + \frac{p_{p0} - N_A \ln f_A(0)}{(N_A - N_D)\beta q}. \tag{A6}$$

Substituting Eqs. (A5) and (A6) into Eq. (27) and using Eq. (29), the gate voltage can be derived as follows:

$$V_G = V_{fb,0} - Q_{it}/C_{ins} + \frac{p_{p0} - N_A \ln f_A(0)}{(N_A - N_D)\beta q} + \frac{\varepsilon_S q(N_A - N_D)}{2}\left(\frac{1}{C_G^2} - \frac{1}{C_{ins}^2}\right),$$

which is evidently equivalent to Eq. (33).

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