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Simple low power nanosecond pulses from a continuous wave diode laser

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J. P. McClymer[a)]

AFFILIATIONS

Department of Physics and Astronomy, University of Maine, Orono, Maine 04469-5709, USA

[a)]McClymer@maine.edu

ABSTRACT

A low power continuous wave diode laser is rapidly modulated using the inherent propagation delay and finite slew rate of an inverter to create overlapping time transistor-transistor logic pulses to activate an AND gate to create sub-nanosecond laser pulses at user controller repetition rate up to 100 KHz.

This note describes how to make a simple, inexpensive, and low part count modulated milliwatt level laser system to produce nanosecond (ns) scale pulses. This circuit uses a fast AND gate to generate high repetition nanosecond pulses which directly drive a laser diode. The laser diode is a generic 5 mw (red) laser diode with a nominal output at 650 nm.

The idea is to provide two HIGH level pulses which overlap for a short period of time (ns in this case) resulting in a HIGH output from the AND gate which directly drives the laser for a time comparable to the overlap. There are multiple ways to create the time shifted input pulses.

A time delay between two pulses may be introduced by addition of a delay line. The delay line however is subject to mechanical and thermal perturbations which will cause fluctuations and drift in the time delay. This line also introduces reflections on the time scale of interest that need to be suppressed.

One example circuit[1] subjects a pulse to two different RC time constants. Without further introduction of delay, one pulse is inverted with respect to the other using two comparators and introduced to the AND gate resulting in a user controllable output pulse from about 1 to 50 ns. This circuit requires 5 external resistors and capacitors for the time delay and 3 additional components and two comparators for the inversion before reaching the AND gate. Each component and connection adds additional parasitic capacitance and noise.

By contrast, the circuit described in this note uses the intrinsic propagation delay of a fast inverter to both set the delay time and invert the pulse, replacing the 2 comparators and the 8 external components with only one inverting gate and no external components.

An initial transistor-transistor logic (TTL) pulse is connected to both an inverter and one input of the AND gate. The inverted and delayed pulse from the inverter goes to the other input of the AND gate, as shown in Fig. 1. The initial inverter in the schematic is to produce a cleaner pulse than provided by the function generator. The example circuit also uses an initial comparator for the same purpose.

In the simplest model, the two pulses would be shifted by one propagation delay resulting in an output pulse no shorter than this delay. This circuit uses a 74HCT04 chip with a specified typical propagation delay of 8 ns with a supply voltage of 5 V and driving a 15 pF load. The specifications do not however provide the "intrinsic" propagation delay of the gate, which depends on details of construction. The gate input capacitance is given as 3.5 pF, well below the value for which the delay is specified. The propagation delay can be modeled[2] as an intrinsic delay plus a term linear in capacitance. We should therefore expect a propagation delay shorter than specified and approaching the intrinsic delay time of the gate. The chip data sheet does not provide any information on this intrinsic delay. The actual time during which both pulses are HIGH also depends on the rise and fall time of the signals, which is also a function of load. For the AND gate used in this circuit, the typical HIGH and LOW level inputs are 1.6 V and 1.2 V, respectively. These are typical values, and each chip could have other values.

The circuit is constructed to achieve the minimum propagation delay. All chips are not identical, and some chip to chip variation

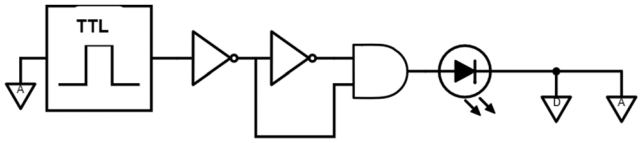

FIG. 1. Circuit schematic.

is expected. The chips used in this circuit were used "off-the-shelf" with no *a priori* testing.

This circuit keeps part counts and inter-connections low. The circuit is constructed in the "interdigitated dead-bug" style; a 74HCT04 hex-inverter DIP chip is glued upside down, "dead-bug style," to a copper plate. A 74HCT08 AND gate DIP chip is then glued, upside down, inside and displaced by 1 pin from the 7404-inverter chip. This arrangement allows leads on the two chips to be directly soldered together. This arrangement minimizes parasitic capacitance and pulse reflections, leading to cleaner and shorter laser pulses. The laser diode anode is directly soldered to the output of the AND gate. The schematic is shown in Fig. 1 and the assembly in Fig. 2.

All unused gates are tied to ground at the same point on the copper plate, so the digital and analog grounds are shared. No improvement was seen with the use of bypass capacitors, so none were used in this circuit. Both chips are operated with the same supply voltage above 6 V but below the maximum 7 V.

An external TTL pulse, from a HP function generator, enters an inverter which produces a clean inverted TTL pulse. This function generator could be replaced by a 555 timer or a circuit that functions similarly to keep total cost and size down. The function generator is operating at approximately 100 KHz. I use an initial inverter after the function generator to slightly clean up the pulse. This TTL pulse enters both one input of the AND gate and into another inverter whose output enters the AND gate. The result is a TTL pulse and a time shifted, by one propagation delay, inverted TTL pulse (Fig. 3) both entering the AND gate, whose output is HIGH during the overlap (Fig. 4). A 500 MhZ, 2 GSa/s oscilloscope, with 50-Ω input impedance, is used to better capture the fast rise times and short pulse widths. All signals are averaged 64 times with real time sampling.

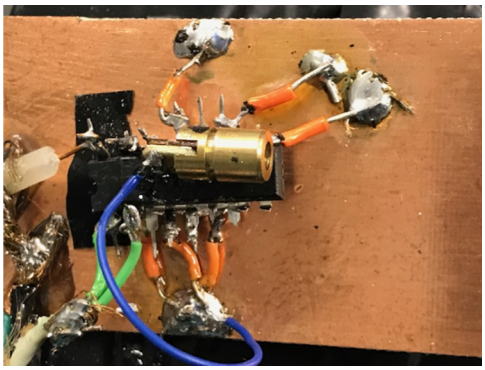

FIG. 2. Laser diode inside the AND gate which is inside the inverter DIP chip and offset by 1 pin. Green wires are V_{cc}. The shielded cable (middle left) provides the TTL pulse from the function generator.

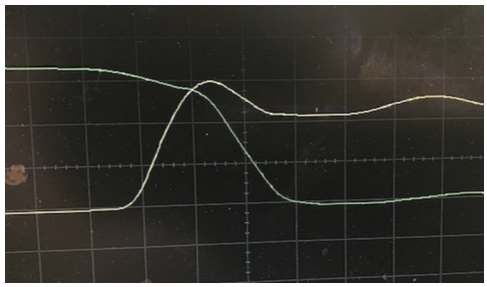

FIG. 3. Overlap of the falling TTL signal and rise of delayed and inverted signal from 7404. Time scale is 2 ns/division, and voltage scale is 2 V/division. Both pulses overlap above 2 V for approximately 4 ns.

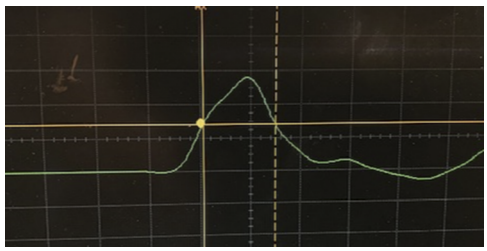

FIG. 4. Output of the AND gate. Signal has a FWHM of 2.8 ns and a maximum voltage of 3.1 V. Voltage scale is 1 V/div.

The output of the AND gate is directly connected to the anode of the diode laser. The laser has a turn on voltage of approximately 2.7 V (the turn on voltage and current are both temperature dependent), so the laser pulse, Fig. 5, is significantly narrower than the AND output pulse. The chip provides sufficient current to turn on the laser.

The laser pulse is measured (Fig. 5) with a high-speed commercial SI photodiode[3] with a nominal rise time and Full Width Half Maximum (FWHM) of 1 ns showing a laser pulse with a FWHM of 1.6 ns. A somewhat faster lab-built photodiode circuit gave a shorter pulse width of 1.2 ns (Fig. 6).

The laser is easily seen in a normally illuminated room. The apparent laser brightness decreases as the TTL rep rate decreases, eventually becoming too dim for me to see. The laser pulse intensity

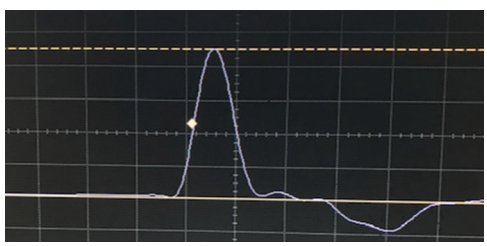

FIG. 5. Laser pulse with FWHM 1.6 ns. Time base is 2 ns/div, and voltage scale is 13 mv/div.

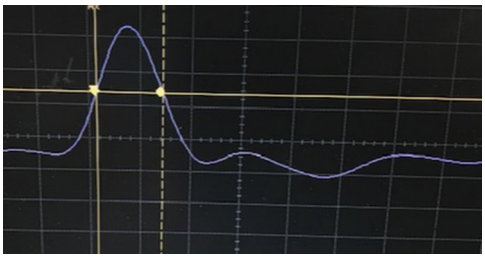

FIG. 6. Laser pulse, 1.28 ns FWHM with sub 800 ps rise time. Time base is 1 ns/div, and voltage scale is 10 mv/div.

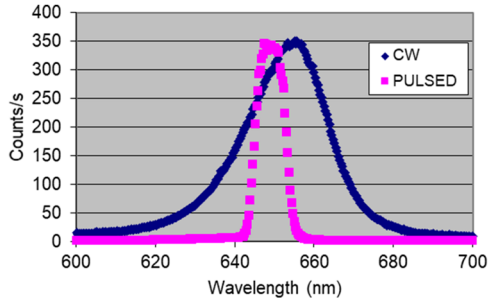

FIG. 7. Spectrum of the modulated (square) and DC (diamond) driven diode laser.

can be estimated using the nominal responsivity of the commercial photodiode of .4 A/W, giving a maximum pulse intensity of 2.8 mw.

The laser is indeed lasing and not simply acting as a light-emitting diode (LED). The beam is just as collimated as when used with a DC supply, with the beam traveling 3 m or so across a room. A spectrum of the pulsed and DC excited laser (Fig. 7) from the same batch shows that the pulsed laser has a narrower bandwidth than that of the DC with peak shifted to a somewhat lower wavelength. Since the spectrum is not measured for the same laser under pulsed and DC excitation, the results should not be interpreted as generic.

The oscilloscope and photodiode combination is too slow to accurately give the true FWHM of the laser pulse. This true width can be estimated by adding the FWHM from each component in quadrature where the FWHM is estimated[4] from FWHM ≈ 0.4/bandwidth. Using the nominal oscilloscope bandwidth, the bandwidth of the photodiode and cable (bandwidth 3 GHz), the FWHM of the laser pulse is estimated to be approximately 600 ps.

I thank Bob Rice for providing the oscilloscope.

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[1] See https://www.analog.com/media/en/technical-documentation/application-notes/an98f.pdf for Circuit 19 in Linear Technology Application Note 98 (AN-98) by Jim Williams, 2004.
[2] See for example, V. Adler and E. G. Friedman, Analog Integr. Circuits Signal Process. **14**, 29–39 (1997).
[3] DET 210 photodiode from Thor Labs.
[4] See https://www.newport.com/n/insights-into-high-speed-detectors-and-high-frequency-techniques for Insights into High-Speed Detectors and High-Frequency Techniques (Application Note).