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Potential application of *p–i–n* semiconductor capacitor with non-linear voltage–charge characteristic for secondary battery

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ABSTRACT

We carried out the time-dependent drift–diffusion simulation to study a capacitor with semiconductor electrodes and its potential application for a battery-like operation. We employed the *p–i–n* and *p–n* structures with an insulator inserted in the middle of the devices. Both devices can store and retain the charge and voltage without any degradation, thanks to the insulator which inhibits carrier recombination. Additionally, they have a strong non-linear dependence between the stored charge and voltage, whereas a conventional capacitor shows linearity. The non-linearity is induced as follows. The junction capacitance dominates under smaller bias than the built-in potential. When the voltage exceeds the built-in, the capacitance associated with the insulator characterizes the charge–voltage relation. The intrinsic layer further enhances the non-linearity and keeps the output voltage high until the stored charge becomes significantly small due to its small capacitance. As a result, the *p–i–n* like structure with the insulator stores larger energy than that of the conventional capacitor and realizes the battery-like operation.

I. INTRODUCTION

The demands for rechargeable storage devices are ever-increasing for various kinds of electrical applications. Many review papers have been devoted to categorizing storage devices by the Ragone plot.[1–3] Among them, battery and supercapacitor[4,5] are attractive for applications, such as electric vehicles and renewable energy sources. Additionally, the miniaturization of storage devices such as micro-battery[6–8] and -capacitor[9] is of importance and has been studied for the system-on-chip (SoC),[7,10–12] internet-of-things, medical, flexible, and wearable devices.[13]

In terms of the batteries, the Li-ion battery is leading the storage devices. The novel batteries with Mg,[14] Na,[15] K,[16] and Li–S[17] and also the all-solid-state Li-ion battery[18,19] have been studied as candidates for the post-Li-ion battery. In the supercapacitor, it employs the electric double-layer and/or reversible redox reactions at the electrode. Batteries and supercapacitors are categorized as the electrochemical storage since their charge and discharge processes are based on mass transport of chemical species and/or electrochemical reaction at the electrode.

On the other hand, non-chemical and solid-state energy storage devices, i.e., dielectric capacitor, are attractive since their charge and discharge operations are carried out by carriers and/or polarization of the insulator. In terms of the electrostatic charging device, the metal-oxide-semiconductor (MOS) capacitor structure is widely employed in electronic devices such as a flash memory. Furthermore, the Si-based 3D capacitor has been studied in the applications of SoC and system-in-package to supply stable electric power for a decade.[11,20–23]

As categorized in the Ragone plot, however, a simple capacitor supplies the high electric power rather than the energy, whereas the battery has opposite properties. It is because the conventional capacitor shows a linear dependence between stored charge and output voltage and is regarded as a small storable energy. It indicates that if a capacitor has a voltage dependent capacitance and thus shows a non-linear relation between the stored charge and voltage, we could increase the stored energy. Therefore, it would be attractive that a high energy storage is realized by solid-state devices without the electrochemical operation.

Aiming for high energy storage by the non-chemical process, the insulating materials showing the anti-ferroelectric property have been intensively studied.[2,24–28] The anti-ferroelectric material is strongly polarized when the external electric field is applied. As a result, the polarization stores and supplies the electric energy from/to the external circuits.

Recently, Sasaki *et al.*[29] reported a pioneering demonstration of a solid-state secondary-battery by using semiconductor electrodes and the conventional insulator material. They employed NiO_x (p-type) and TiO_x (n-type) as the anode and cathode electrodes, respectively, and SiN_x as the insulating layer. Their device has a structure similar to that of a simple p–n diode except for the insertion of an insulator, but it shows a non-linear charge–voltage curve and has a potential application for a large charge and electric-energy storage. The basic origin for their operation, however, has not been studied yet. We believe one of the origins of the non-linear charge–voltage relation is induced by their electrodes and the insulator inserted. It is because the p–n diode generally works as a capacitor[30] under the reverse bias condition and is known as the junction capacitor. Additionally, the diode capacitance under the forward bias also shows non-linear dependence on the bias, which is known as the diffusion capacitance, while it cannot retain the charges.

Significant non-linear voltage–charge (V–Q) characteristics are essential for the further development of the semiconductor battery based on the p–n structures. In this paper, we carry out the drift–diffusion (DD) simulation for the semiconductor capacitor and study the effect of inserting the i-layer between p- and n-layers on V–Q characteristics. While Sasaki employed rather a thick SiN_x insulator, we use a semiconductor capacitor incorporating with p- and n-type electrodes with a thin insulator layer between those layers to focus on the fundamental properties of semiconductor electrodes. In addition to the fact that the stored charge is retained by the insulator that inhibits carrier recombination, the device in which the i-layer is inserted exhibits a strong non-linear V–Q characteristic compared to that of the p–n based structure. As a result, the p–i–n structure is expected to have a higher electric energy storage than the p–n based device and the conventional metal–electrode capacitors.

II. TRANSIENT DRIFT-DIFFUSION SIMULATION

We employ the time-dependent (TD) DD method[31] in 1D for the present device since the charging, discharging, and retention operations are carried out in the time domain. In TD-DD, we solve the Poisson equation to determine the electrostatic potential,

$$\frac{d}{dx}\left(\varepsilon\frac{d\psi}{dx}\right) = -e(p - N_A - n + N_D), \tag{1}$$

where ε is the dielectric constant, ψ is the electrostatic potential, e is the elementary charge, p is the hole concentration, n is the electron concentration, N_A is the ionized accepter concentration, and N_D is the ionized donor concentration. Additionally, electron and hole continuity equations are given by

$$\frac{\partial n}{\partial t} = \frac{1}{e}\frac{dJ_n}{dx} - R, \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{e}\frac{dJ_p}{dx} - R, \tag{3}$$

where J_n and J_p are electron and hole current densities, respectively, and R is the carrier recombination rate. In this study, we consider the Shockley–Read–Hall (SRH) recombination. Additionally, surface recombinations are automatically incorporated as minority carrier currents at the contacts due to the boundary condition where carrier concentrations must be the same as those in the equilibrium or quasi-Fermi level of the minority carriers must coincide with that of majorities. For the electron and hole, we consider the Fermi statistics by following Ref. 32.

In the transient simulation, the total current J is given by the sum of J_n, J_p, and the displacement current, J_D. J_D is given by

$$J_D = -\frac{\partial}{\partial t}\left(\varepsilon\frac{d\psi}{dx}\right). \tag{4}$$

By taking the spatial derivative of J and using Eqs. (1)–(4),

$$\begin{aligned}\frac{dJ}{dx} &= \frac{d}{dx}(J_D + J_p + J_n)\\ &= -\frac{\partial}{\partial t}\left[\frac{d}{dx}\left(\epsilon\frac{d\psi}{dx}\right)\right] - e\left(\frac{\partial p}{\partial t} - \frac{\partial n}{\partial t}\right)\\ &= 0.\end{aligned} \tag{5}$$

It indicates that the current continuity condition must be satisfied even under the transient simulation.

The device structure is schematically presented in Fig. 1. The structure is similar to a simple p–i–n diode but has an insulator in the middle of the device. The heterointerface between the semiconductor and the insulator is modeled by following Ref. 33. Since we employ a thick and high offset energy for the insulator, the

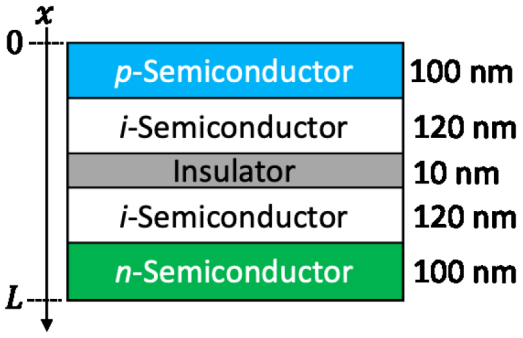

FIG. 1. Schematic of the employed device structure. L is the total thickness of the device.

TABLE I. Parameters employed in this study. Symbols are defined in the main text. ε_0 and m_0 are the permittivity constant in vacuum and electron rest mass.

Symbol	Value	Symbol	Value	Symbol	Value
N_A	10^{19} cm^{-3}	μ_h	5 cm^2/Vs	ε(Semi)	$12\varepsilon_0$
N_D	10^{19} cm^{-3}	μ_e	5 cm^2/Vs	ε(Ins)	$80\varepsilon_0$
τ_h	10^{-9} s	E_G(Semi)	1.5 eV	T	300 K
τ_e	10^{-9} s	E_G(Ins)	4.5 eV	E_t(SRH)	$E_G/2$
N_V	10^{20} cm^{-3}	m_h	$0.3m_0$	ΔE_V	1.5 eV
N_C	10^{20} cm^{-3}	m_e	$0.3m_0$	ΔE_C	1.5 eV

tunneling effect is neglected. The parameters are listed in Table I. In the table, N_C and N_V are the effective density of states of the conduction band (CB) and the valence band (VB), respectively. μ_i, τ_i, and m_i are mobility, lifetime, and mass of carriers, respectively, where subscript e and h express the electron and the hole. E_G is bandgap energy, and ΔE_C and ΔE_V are band offsets between the semiconductor and the insulator for CB and VB, respectively. SRH trap-state energy, E_t(SRH), is a middle of the bandgap.

We employ ideal ohmic contacts for both anode and cathode and, thus, the charge neutrality must be satisfied at each contact. Additionally, we use the controlled current boundary condition, and then the potentials at the contacts are self-consistently determined depending on quantities of the stored charge and contact current density.

The boundary condition is applied as follows. By taking a difference between Eqs. (2) and (3) and integrating the difference in space,

$$\int_0^L \frac{\partial p}{\partial t}dx - \int_0^L \frac{\partial n}{\partial t}dx = -\frac{1}{e}\int_0^L \frac{d}{dx}(J_n + J_p)dx. \tag{6}$$

The RHS of the above equation becomes zero due to the employed boundary conditions. As a result,

$$\int_0^L \frac{\partial p}{\partial t}dx = \int_0^L \frac{\partial n}{\partial t}dx. \tag{7}$$

This condition allows us to define the stored charge density Q as

$$Q(t) = e\int_0^t\int_0^L \frac{\partial n}{\partial t'}dxdt' = e\int_0^t\int_0^L \frac{\partial p}{\partial t'}dxdt'. \tag{8}$$

Therefore,

$$\begin{aligned}\frac{dQ}{dt} &= e\int_0^L \frac{\partial n}{\partial t}dx = \int_0^L \left(\frac{dJ_n}{dx} - eR\right)dx \\ &= J_n(L, V_{\text{Cathode}}) - J_n(0, V_{\text{Athode}}) - e\int_0^L Rdx,\end{aligned} \tag{9}$$

where the first argument in J_n expresses the contact position presented in Fig. 1. A similar equation can be found for holes by employing Eq. (3). The current controlled by an external circuit J_{Ext} is expressed as

$$J_{\text{Ext}} = J_D + J_n + J_p \tag{10}$$

by Kirchhoff's law. As pointed above, $J_D = 0$ since the charge neutral and the ideal ohmic contact conditions are adopted. Finally, we employ the Newton method to find potentials of anode V_{Anode} and cathode V_{Cathode} by using Eq. (10) with satisfying Eq. (9). The voltage V is defined as $V = V_{\text{Cathode}} - V_{\text{Anode}}$.

We carry out the charging operation within 5 s with $J_{Ext} = 1.0\,\mu$A/cm^2. It indicates that the external circuit supplies $5.0\,\mu$C/cm^2 $= 3.15 \times 10^{13}$ cm^{-2} $= 1.39$ nAh/cm^2 to the device. After the charging, we take the retention operation in 10 s and finally constant current discharging process with $J_{Ext} = -1.0\,\mu$A/cm^2.

III. RESULTS AND DISCUSSION

The time dependent characteristics of voltage and charge are plotted in Fig. 2. The results of the device without the intrinsic layer noted as the p–n structure are also presented. The p–n structure has 220 nm thick p- and n-type semiconductor electrodes with 10 nm thick insulator inserted in the middle. We employ the charge concentration unit in cm^{-2} neither in C/cm^2 nor Ah/cm^2 for convenience.

The calculated band diagram, current density, and excess carrier concentration profiles of the p–i–n device are shown in Fig. 3 at the beginning of the charging stage ($t = 0.01$ s). The excess carrier concentration is defined as a concentration difference from that in the equilibrium. Note that the excess carrier concentration is equivalent to the concentration injected from the electrode because the insulator inhibits the carrier diffusion in the present structre. In terms of the current continuity, the displacement current dominates in the middle of the device, while carrier currents are only in the doped semiconductor regions. As a result, the current continuity is satisfied in the device. It indicates that our

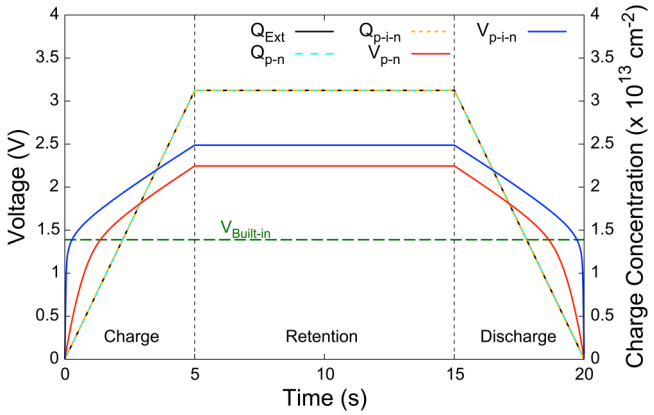

FIG. 2. Time dependence of voltage, V, and charge concentration, Q, for p–i–n and p–n structure devices. Q_{Ext} is the concentration from/to the external circuit. $V_{\text{Built-in}}$ is the built-in potential and 1.39 V.

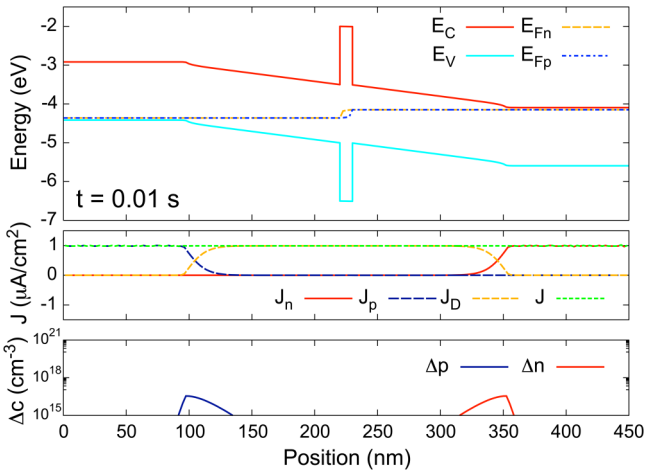

FIG. 3. (Top) Calculated band diagram, (middle) current density profile, and (bottom) excess carrier concentration at $t = 0.01$ s. E_C and E_V are the band edges of CB and VB, respectively. E_{F_n} and E_{F_p} are quasi-Fermi levels of electrons and holes, respectively. J, J_n, J_p, and J_D are total, electron, hole, and displacement current densities, respectively. The excess carrier concentration, Δc, is defined as a concentration difference from that in the equilibrium, where Δp and Δn are for holes and electrons, respectively. In the preset structure, the excess carrier concentration is equivalent to the concentration injected from the electrode because the insulator inhibits the carrier diffusion. The voltage is 0.21 V.

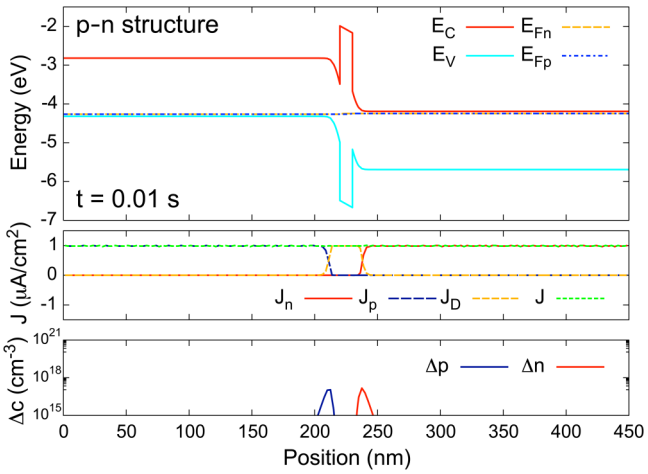

FIG. 4. (Top) Calculated band diagram, (middle) current density profile, and (bottom) excess carrier concentration of the p–n structure at $t = 0.01$ s. The voltage is 0.02 V.

simulation finds a voltage that satisfies the boundary condition by following Eq. (9) and also the current continuity.

In this stage, the voltage of the p–i–n structure increases rapidly compared to that of the p–n device. As presented in Fig. 3, the injected hole and electron currents in the p–i–n device decrease around the boundary between p- and i-layers and the boundary between i- and n-layers, respectively. It is because those fluxes are unable to overcome the electric field in the i-layer. Therefore, injected holes and electrons are accumulated around those boundary regions as excess carrier profile indicates. As a result, the voltage increase, or dominant capacitance, is roughly characterized by the thickness of the i- layer.

On the other hand, carrier accumulations in the p–n structure occur around the edges of the depletion region, as the hole and electron currents and their excess carrier concentrations indicate in Fig. 4. Thus, the depletion width determines the capacitance of the p–n device is thinner than the i-layer in the p–i–n device. Those analyses describe that the p–i–n device has a smaller capacitance than the p–n structure. As a result, the p–i–n structure obtains a larger voltage than the p–n device when the same amount of charges is supplied.

When the voltage exceeds the built-in potential ($V_{\mathrm{Built-in}} = 1.39$ V), the voltage increase becomes slower. Moreover, the p–i–n and p–n devices show similar dV/dt. The band diagram, current density, and excess carrier profiles of the p–i–n device are presented in Fig. 5 at $t = 2.0$ s. The hole and electron currents approach to the insulator layer, and the displacement current is only confined within that layer. Similar current profiles are found in the p–n device (not shown here). The electric field across the insulator is inverted compared to the case of $V < V_{\mathrm{Built-in}}$, which results in strong carrier accumulations around the insulator. Due to the strong screening effect induced by the carrier accumulations, the change in electrostatic potential depending on the voltage is limited to the space between the insulator and these accumulation layers. Furthermore, the thickness of the strong carrier accumulation region is thinner than that of the depletion width of the p–n structure, as presented in Fig. 4. Therefore, the capacitance associated with the carrier accumulation region is larger than that characterized by the depletion width of the p–n

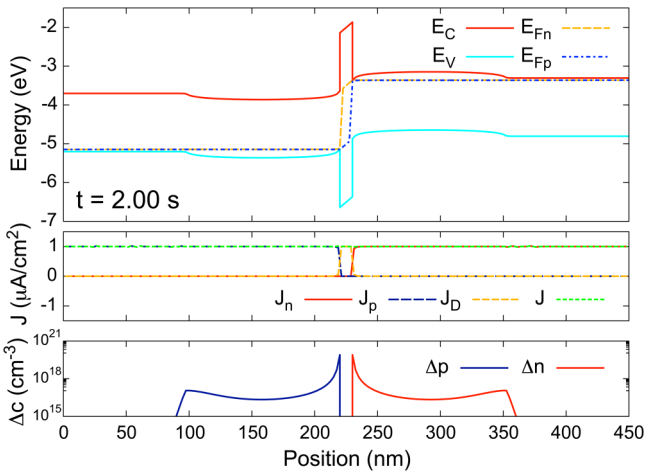

FIG. 5. (Top) Calculated band diagram, (middle) current density profile, and (bottom) excess carrier concentration at $t = 2.0$ s. The voltage is 1.88 V.

device under $V < V_{\mathrm{Built-in}}$. As a result, the difference of dV/dt between two devices is negligible, and dV/dt depends on a capacitance characterized by accumulation layers and the insulator.

It should be noted that the split of quasi-Fermi levels of electrons and holes is negligibly small in the left- and right-side semiconductor layers but significant within the insulator. It is expected that carrier recombinations in the semiconductor layers are negligible. In the insulator, the recombination is also very small since it has high bandgap energy and negligibly small carrier concentrations. This point becomes crucial under the retention operation as described below.

During the retention, Eq. (9) becomes

$$\frac{dQ}{dt} = -J_p(L, V_{\mathrm{Cathode}}) - J_n(0, V_{\mathrm{Anode}}) - e\int_0^L R dx, \qquad (11)$$

where $J_n + J_p = 0$ is employed for the cathode contact. In this expression, $J_p(L, V_{\mathrm{Cathode}})$ and $J_n(0, V_{\mathrm{Anode}})$ denote the surface recombination currents at the cathode and anode, respectively. Therefore, dQ/dt and voltage are characterized by carrier recombination within the device.

As presented in Fig. 2, both devices have no degradation in the voltage and the charge during the retention operation. Therefore, the insulator well blocks electron and hole diffusions to the left and right side semiconductor layers, respectively. It should be noted that both devices start to lose stored carriers and voltage after a long time such as 2 years, which will be reported in a future study. Hence, the analysis of the present device must be carried out in the transient simulation.

In the discharged process, the voltage slowly decreases until it becomes smaller than $V_{\mathrm{Built-in}}$. When $V < V_{\mathrm{Built-in}}$, it drops rapidly as shown in Fig. 2. The voltage–charge relations of both devices are completely the same found in their charging operations. It indicates that the stored charge is conserved during the retention operation and extracted without any degradation.

The voltage dependences on the extracted charge concentration are presented in Fig. 6. Those curves are evaluated from the results found in Fig. 2. As a reference, we plot the line calculated by a capacitor $C_{\mathrm{Insulator}}$ with metal electrodes. The capacitance density is given by $\epsilon_{\mathrm{Insulator}}/d_{\mathrm{Insulator}}$, where $d_{\mathrm{Insulator}}$ is the thickness of the insulator. While the conventional capacitor has a linear dependence between the charge and the voltage, the devices with semiconductor electrodes show a strong non-linearity. When $V > V_{\mathrm{Built-in}}$, $|dV/dQ|$ is larger than the conventional capacitor since effective capacitances of the semiconductor electrodes have additional thickness based on the accumulation region around the insulator, whereas that region is negligible for the metal electrode.

As pointed in the Introduction, the capacitance of the p–n (or p–i–n) diode shows the diffusion capacitance[30] under the forward bias. The diode, however, cannot retain charges and only shows its steady-state operation, since stored carriers are recombined. Moreover, the significant non-linearity is due to the recombination in the diode. On the other hand, the non-linearity of the present device is due to the accumulated carriers as the insulator inhibits carrier recombination, which is fundamentally different from that

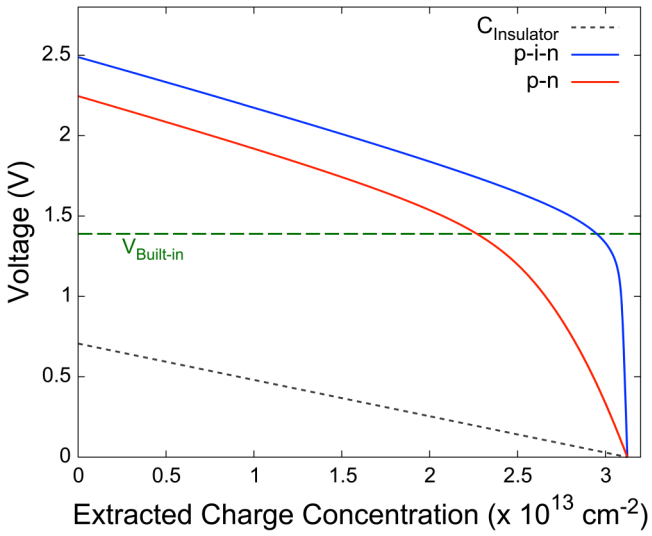

FIG. 6. Calculated voltage–discharge curves evaluated from Fig. 2. $C_{\mathrm{Insulator}}$ is a result when we replace semiconductor electrodes to metal ones, i.e., a conventional dielectric capacitor (metal–insulator–metal structure).

of the diode. Therefore, the insulator is inevitable for the storage device operation.

The stored energy, W, is evaluated as

$$W = \int V dQ, \qquad (12)$$

from the V–Q curve. p–n and p–i–n devices have an advantage for electric-energy storage compared to the conventional capacitor as V–Q curves indicate in Fig. 6, thanks to $V_{\mathrm{Built-in}}$ induced by p- and n-type semiconductor electrodes. Furthermore, the i-layer can keep the output voltage high until the charge becomes significantly small since it has a smaller capacitance than that of the p–n device under $V < V_{\mathrm{Built-in}}$. As a result, the p–i–n device improves a battery-like operation, thanks to a shift of dominant capacitors mainly based on the i-layer and the insulator for low and high voltages, respectively, compared to the p–n based structure.

Finally, we comment on several aspects of the present device. Since $V_{\mathrm{Built-in}}$ boosts the output voltage, the device that has a large $V_{\mathrm{Built-in}}$ would be suitable for high energy storage. In other words, we can choose the output voltage by selecting semiconductor materials that have from narrow to wide bandgap energy. For example, InAs and GaN could have these voltages less than 0.36 V and 3.4 V, respectively, at 300 K. The stored charge concentration in the present study, however, is quite small compared to electrochemical batteries. Thus, we should increase the dielectric constant of the insulator and reduce the insulator thickness as thin as the carrier diffusion and the tunneling can be prevented, and the breakdown does not occur under operation voltage. The detailed dependence on the band offset energy and the operation temperature will be discussed somewhere. Additionally, the surface area modification of

the insulator would be beneficial by introducing 2D or 3D structures employed in the micro-batteries and -capacitors.[11,20–23] These points are also beyond the scope of this work and will be reported in a future study.

In terms of the device structure, the rapid reduction of the output voltage is due to the intrinsic layer and its smaller capacitance than that of the insulator, when the stored charge becomes significantly small. Thus, we address that the position of the insulator layer is acceptable anywhere as long as it locates within the depletion region or/and the intrinsic layer.

IV. CONCLUSION

We carried out the TD-DD simulation for the *p–i–n* structure with the insulator barrier to study its potential for a secondary-batter-like operation. The insulator well blocks carrier diffusion and recombination, and then, the stored charge and voltage are hardly degraded during the retention operation. The strong nonlinear V–Q curve is induced by the *i*-layer and indicates that the *p–i–n* structure can improve a battery-like operation compared to the *p–n* device. The output voltage is characterized by the built-in potential, and the device increases the stored electric energy compared to a conventional capacitor. Additionally, it allows us to choose the voltage depending on the semiconductor materials. The stored charge concentration, however, is rather small, and great efforts to overcome this problem should be required.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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