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Ultra-thin wafer technology and applications: A review

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ABSTRACT

Ultra-thin wafers with thickness of typically less than 200 μm are important building blocks in semiconductor device manufacturing. Due to the special mechanical properties of ultra-thin wafers, the fabrication and handling of ultra-thin wafers are substantially different from traditional ones. Thus, the progresses of ultra-thin wafer technology from manufacturing process to wafer transportation and device application are reviewed herein. The combination of mechanical grinding and stress relief through polishing or etching has become the standard wafer thinning process. Owing to the rising of TAIKO wafers, special equipments and carriers have the potential to be eliminated in ultra-thin wafer handling. Ultra-thin wafer has broad applications in semiconductor device fabrication and would have long-term impact on semiconductor industrial.

1. Introduction

Silicon wafer has great significance to modern electronic industrial due to the fundamental function of silicon, such as robust mechanical strength and semiconductive property [1–4]. Larger the wafer size allows more devices to be manufactured simultaneously, which enables the cost cut. Compared with traditional wafers with thickness of ~700 μm, the mechanical stability of the ultra-thin wafers with thickness of less than 200 μm would be greatly reduced, which might cause bending or even breakage due to the influence of its own gravity [3]. To provide sufficient mechanical and thermal stability of the large size wafer, the thickness of the wafer should be thicker to ensure wafer safe (without breakage) during the processing steps in manufacturing. However, from the point of view of device performance, the wafer should be thinned (typically less than 200 μm) to maintain Moore's Law, especially for the devices with 3D stacking [5–7]. One way to overcome the contradiction mentioned above is bonding the thinned wafer with large size to a glass or plastic carrier [8–11]. Owing to the coefficient of thermal expansion mismatch from the different materials used in the bonding wafer, the interface bears high thermal and/or mechanical stresses, which limits the application of the ultra-thin wafer with carrier below. Furthermore, the carrier used would have no assistance to overcome the damages introduced during the back-grinding process, which could not reduce the wafer breakage risk in the dicing process. One alternative way is dicing-before-grinding (DBG) technology, where the wafer is half-cut to enable the automatic die separation during the subsequent back-grinding [12–14]. Though the difference between the DBG process and the standard back-grinding process is just the process sequence, ultra-thin wafer state actually does not exist in DBG process due to the formation of separated die when the wafer is thinned. Thus, the dicing speed could be increased due to the reduction of backside chipping risk, and the production capacity increases correspondingly. In addition, for the reason carrier is not used in DBG process, it could avoid carrier warpage and outgas in the vacuum system caused by the coefficient of thermal expansion mismatch [1,15–17]. However, DBG process is only suitable for advanced packaging, where the devices are already fabricated to form the dies. As another alternative ultra-thin wafer technology without carrier, TAIKO wafer has witnessed rapid development in recent years [18–20]. The elimination of carriers brings great convenience to ultra-thin wafer technology, where ultra-thin wafer has the potential to be processed as conventional wafer. In contrast to DBG process, TAIKO wafer could be used in both electronic devices fabrication and packaging. Ultra-thin wafer has obvious significance to electronic devices, for either manufacturing or packaging. From the point of view of device fabrication, ultra-thin wafer could reduce the on-state resistance in the vertical structure devices. For the devices with lateral architecture, the state of ultra-thin wafer mainly appears in the packaging process, which could achieve wafer level packaging with economies of scale and provide the geometrical advantage to create through contacts in the die. However, TAIKO wafer also faces some inadequacies. The thicker edge/ring area in TAIKO wafer makes effective area of the wafer for device fabrication decreases, and the removal of the thicker edge/ring area in TAIKO wafer has challenges in the packaging process.

Thus, methods and apparatus for ultra-thin wafer manufacturing, manipulating, dicing, and packaging are different from conventional

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ones, indicating new processes and equipment might need to be developed. Recently, though relevant researchers have completed a lot of works and achieved fruitful results, few review articles have been published to summarize these achievements and prospects related to this field, especially for the connection of ultra-thin wafer technology from manufacturing process to device application. In this review, we describe the manufacturing, transportation, and application of ultra-thin wafer. These contents might bring new thinking to the semiconductor industrial community because the thinning of device wafer has become a standard practice in semiconductor device.

2. Ultra-thin wafer manufacturing process

In terms of actual production, Dhadda et al. [21] reported ultra-thin wafer manufacturing in IR (International Rectifier Co., Ltd.), where an 8-inch (200 mm) ultra-thin wafer producing line has been established. In IR, the mass production of 8-inch ultra-thin wafers with thickness of 120 μm and 70 μm has been realized. The samples with thickness of 50 μm and 30 μm have also been proven to be viable.

2.1. Grinding and polishing

The mainstream method for ultra-thin wafer fabrication is mechanical grinding and polishing [22–26]. It allows the wafer thickness to be reduced from about 750 μm to less than 100 μm in a few minutes. The uniformity could be well controlled for both within-wafer and cross-wafer. In recent years, ultra-thin wafers are moving toward to achieving carrier-free. As can be seen in Fig. 1, the ultra-thin wafer without carrier or so-called TAIKO wafer has a 2–3 mm edge area that is not thinned, which stabilizes the wafer to avoid warpage or deflection [18,27] (See also the URL https://www.disco.co.jp/eg/solution/library/taiko.html). Under the influence of its own gravity, the traditional ultra-thin wafer tends to bending, whereas the TAIKO wafer has no obvious warpage and achieves free-standing (Fig. 1a). This is because the unthinned edge ring in TAIKO wafer could provide the mechanical supporting (Fig. 1b). Thus, carrier could be eliminated in TAIKO wafer (Fig. 1b), whereas the traditional ultra-thin wafer is often bonded to a carrier by glue to keep flat (Fig. 1c). Furthermore, the sharp edge of traditional ultra-thin wafer with carrier is also eliminated in TAIKO wafer (Fig. 1b and c). To obtain ultra-thin wafer through mechanical grinding, a grinder is usually adopted, which mainly contains motor, wheel and chuck from the top to the bottom (Fig. 2). The wafer fixed on the chuck could be thinned by the rotating grinding wheel. As also shown in Fig. 2a, the grinding wheel is larger than the wafer in conventional wafer thinning process which guarantees the uniformity [23]. On the contrary, in TAIKO process [22] the grinding wheel is substantially smaller than the wafer to be thinned, where the grinding only happens in the inner portion with wafer edge eliminated of 2–3 mm (Fig. 2b). In TAIKO wafer, the inner portion could be thinned to be less than 200 μm, whereas the rim portion keeps at the wafer original thickness. This architecture has a similar shape compared with a Japanese drum named “TAIKO”, where the inside portion is supported by the edge [1]. The TAIKO wafers do not use carriers and adhesives, allowing the device fabrication based on TAIKO wafers to be processed on both sides of the wafer and subjected to higher process temperatures. Besides, TAIKO wafers do not require special equipment to transport, which could reduce cost in ultra-thin wafer handling process. But admittedly, TAIKO technology does have disadvantages. With the increasing of wafer size, the method to mark the wafer orientation changes from flat edge to notch. The thicker edge area in TAIKO wafer expands due to the existence of the notch. This could decrease the effective area of the wafer, which further restricts the development of TAIKO wafer. Another inadequacy of TAIKO wafer is the uneven back of the wafer with unthinned edge ring remaining, resulting in measurement and dicing difficulties in the packaging process. Thus, before measuring and separating the dies, the thicker edge/ring area of TAIKO wafer needs to be removed where a special blade dicing process or a laser dicing process is often required.

Considering damages would be produced during the mechanical grinding, the ultra-thin wafer has breakage risk due to the concentrated

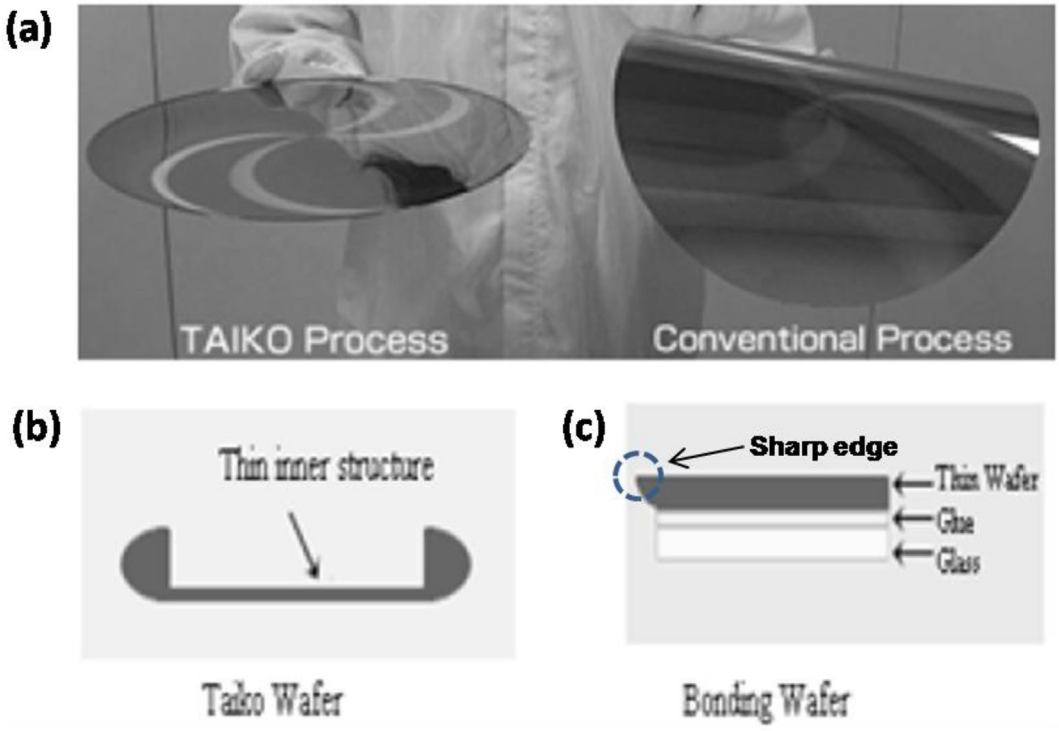

Fig. 1. Comparison of ultra-thin wafer fabricated by TAIKO process and conventional process: (a) Traditional ultra-thin wafer tends to bending under the influence of its own gravity, whereas the TAIKO wafer could achieve free-standing. (b) Schematic of TAIKO wafer. (c) Schematic of traditional ultra-thin wafer bonded on glass substrate by glue. Reproduced from Ref. [27] with permission of Electrochemical Society.

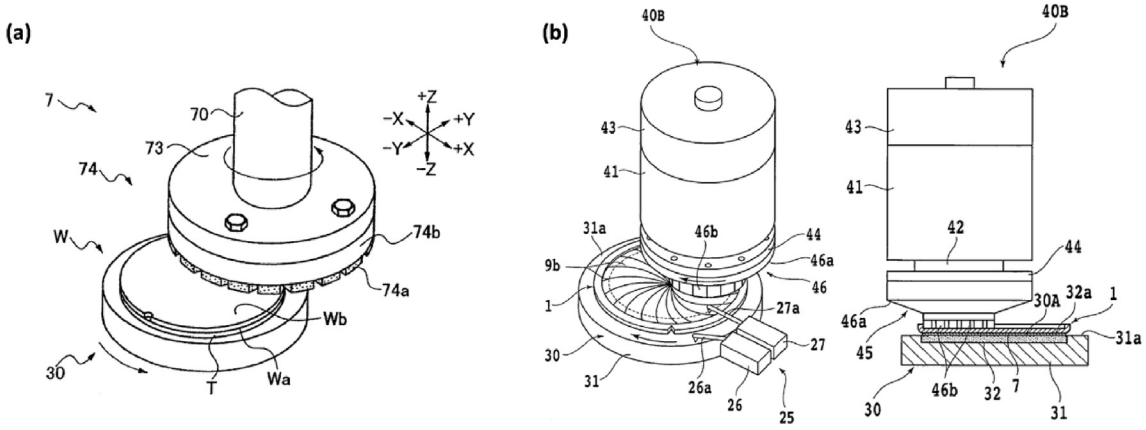

Fig. 2. Mechanical grinding apparatus for (a) conventional process and (b) TAIKO process. Reprinted from Refs. [22–24].

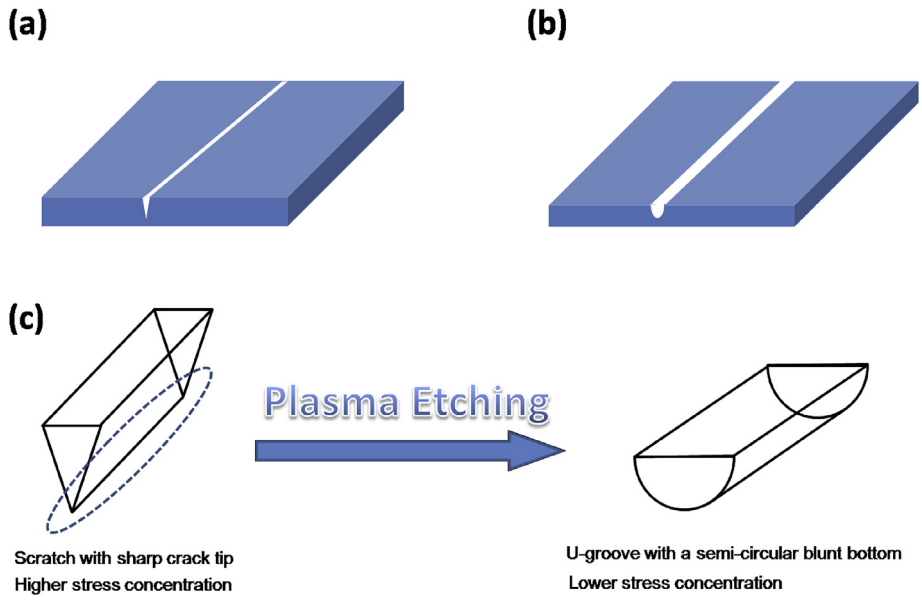

Fig. 3. Typical serious defect introduced by mechanical grinding: (a) Sharp crack tip on the wafer before dry etching; (b) U-groove forming after dry etching; (c) schematic illustration of the plasma etching effect on the defect. Adapted from Ref. [38].

stresses on the shallow damages. Thus, stress relief is required to reduce the damage introduced by grinding, which is usually realized through polishing. Dry polishing is an environmental friendly method of stress relief with lower cost and elimination of waste slurry compared with chemical-mechanical-polishing (CMP). Wet/dry etching could also be adopted in stress relief, which will be introduced in the coming part. Nowadays, the combination of mechanical grinding followed by stress relief has become the standard wafer thinning process.

2.2. Wet etching

Though the wafer without carrier mentioned above could increase wafer rigidity and avoid the sharp edge, the back-grinding damage and residual stress on the processed surface is still a problem due to the usage of mechanical grinding [28]. To address this issue, thinning the wafer by etching could reduce surface damage and residual stress. Wet etching is one of the etching methods, which uses chemical solutions to react with wafers. Immersing the wafer into the chemical solution is a common choice for wet etching, whereas spin or spray etching is often used if the wafer could only be exposed to the chemicals on one side, such as ultra-thin wafer bonded on carriers. For the single-side wet etching, MATECH (Materials and Technologies, Corp.) in United States has developed an all-chemical wafer thinning process (WaveEtch™). The WaveEtch™ process could not only thin the wafers to 40 μm or less, but also improve the wafer surface uniformity and flexibility [29,30]. It is noted that this system could naturally accommodate wafers with large size and thick shape, indicating wet etching itself alone has the potential to be used for wafer thinning from its original thickness. Depending on alkaline or acidic solutions used in wet etching process, it could be roughly divided into two types. Park et al. [31] used wet etching with KOH solution to remove the surface stress of the ultra-thin wafer for device packaging. Compared with that of acidic solution, wet etching by alkaline solution has lower etching rate but higher etching selectivity. In order to reduce the wafer surface damage after mechanical grinding, Yoshikawa and his colleagues developed a wet etching wafer thinning method that etches the wafers by HF/HNO_3 solution where a higher etch rate could be achieved (approximately 800 μm/min with uniformity of 3% in 6–8 inch wafer) [32,33]. In addition to the wafer surface damage reduction after mechanical grinding, wet etching could also be used to enhance the die strength in ultra-thin wafer [34]. Li et al. [35] demonstrated the chip side wall could be smoother after wet etching process, where most of the voids and microcracks introduced by dicing process were removed.

2.3. Dry etching

Dry etching [36,37] is another wafer thinning/etching method using plasma reaction with high surface quality but relatively low manufacturing through-put. McLellan et al. [38] studied the plasma etching effect on wafer surface roughness and morphology. As illustrated in Fig. 3a and b, the sharp and deep scratch on the wafer surface was replaced by U-grooves with a semi-circular blunt bottom after the plasma etching process, where the blue cuboids and white blanks represent the wafer and scratch, respectively. This meaningful result proved the wafer roughness could be improved by plasma etching, because the stress concentration at the crack tip σ_m is estimated by a function of crack length a and crack tip radius ρ ($\sigma_m = 2\sigma_0(a/\rho_t)^{1/2}$), where σ_0 is the nominal applied stress. Fig. 3c shows the scratch with sharp crack tip has become U-groove with a semi-circular blunt bottom after dry etching. Correspondingly, the stress concentration would become lower during the plasma etching process due to the decrease of a/ρ_t ratio, indicating that the dry etching method could improve surface roughness. Thus, dry etching is the most effective stress relief method to remove the damaged layers after back-grinding [39]. Besides, similar to wet etching, dry etching could also perform the front-side stresses relief after dicing process [1,35]. In contrast to mechanical grinding and wet etching, dry etching itself alone is not suitable for wafer thinning process for the reason of low etch rate, high cost, environmental and particle issues.

Due to their own advantages of mechanical grinding, polishing, wet etching and dry etching, the combination of the mechanical grinding and the post-grinding treatment by polishing or etching could become standard wafer thinning process to achieve high surface quality and manufacturing through-put simultaneously. In general, surface quality could be determined by root-mean-square roughness (Rq) given by an atomic force microscopy (AFM) or a 3D measuring laser microscope. Thus, the damage introduced by thinning process would deteriorate the surface quality by definition. Due to the low surface quality after mechanical grinding, post-grinding treatment by polishing or etching is required to release the stresses concentrated on the damages. It is noticed that the stress could also be utilized to obtain ultra-thin wafer in photovoltaic applications [40], but eventually the surface quality should further be improved by wet/dry etching as well to release the stresses and clean the surface [41]. If the surface quality in mechanical grinding process or manufacturing through-put in dry etching process could be improved, the cost in wafer thinning process would be reduced because only one method is required. In all, some technical challenges in following aspects should be addressed in ultra-thin wafer manufacturing: (a) wafer thickness and total thickness variation (TTV) control; (b) surface damage and residual stress control; (c) production mass and cost.

3. Ultra-thin wafer transportation

After ultra-thin wafer is manufactured, it requires related operations, i.e. wafer manipulation method. The ultra-thin wafers are difficult to handle because they have poor mechanical properties. The figure-of-merits evaluating mechanical property mainly includes elasticity, plasticity, stiffness, strength and hardness. For ultra-thin wafer, the reduction of thickness could affect the elasticity, stiffness and strength, where ultra-thin wafers are easy to be bending due to the increasing of the elasticity/reduction of stiffness and easy to be broken owing to the decreasing of strength introduced by the damages on the surface. Fukuda [42] found the shear stress of silicon wafer would increase with the increase of wafer diameter, which could further cause wafer bending/warpage. Namazu et al. [43] reported the silicon beam size has little influence on the Young's modulus in the (110) direction but has large effect on the bending strength. Colleti et al. [44] demonstrated the measurement of mechanical properties of thin wafers with thickness between 120 and 320 mm using ring on ring breakage tester, and the breakage force F and wafer thickness are found to have linear relationship. Considering the poor mechanical properties of ultra-thin wafers with high dependence on the diameter and thickness mentioned above, it is important to develop cheap, efficient and stable ultra-thin wafer handling methods.

3.1. Ultra-thin wafer with carrier

At present, the ultra-thin wafer bonded with carrier is a mainstream method for ultra-thin wafer manipulation [45–48]. The carrier and ultra-thin wafer are temporarily bonded together by the polymer glue, and the carrier protects the ultra-thin wafer from being broken. After the corresponding processes performed on the ultra-thin wafer with carrier are completed, the ultra-thin wafer is debonded from the carrier. In this method, the nature of the adhesive is critical to the success of the wafer-level temporary bonding process. After temporarily bonding the ultra-thin wafer to the carrier, it is necessary to ensure that the wafer surface has high flatness and high bonding strength, but the carrier should also be easy to remove. Jouve et al. [49] evaluated the performance of a new removable high temperature spin-coating adhesive in temporary wafer bonding process. The results showed that the properties of the adhesive, such as bond strength, chemical resistance, thermodynamic stability, adjustable debonding temperature, fulfill the requirements, and no damages would be introduced into the bottom of the through silicon via (TSV) structure in the ultra-thin wafer process when debonding the carrier and removing the adhesive. Electrical measurements have shown that the via resistance of the device based on temporary carrier is as the same as the value of the permanent carrier. Pargfrieder et al. [50] reported the specific process of temporary bonding and debonding as well as the related considerations in detail. The bonding, debonding and cleaning of the ultra-thin wafers are performed on the same platform. They demonstrated that this technology is an efficient and low cost method for TSV manufacturing on ultra-thin wafers.

When the ultra-thin wafer is processed by the temporary bonding-debonding technique, the removal result of the adhesive plays a decisive role. Nowadays, there are two methods for the adhesive removing. One is to change the viscosity of the adhesive by heating, thereby separating the ultra-thin wafer from the carrier [49,51]. Although this method is relatively simple, it has a limitation. If the temperature is too low, the removing result is unsatisfied. On the contrary, if the temperature is too high, the device might be damaged. Another method for the adhesive removing is using radiation (ultraviolet or laser) to degrade the adhesive, change the viscosity, and remove the bonding [52–54]. This method requires special radiation equipment at a high cost and the carrier to be transparent. Shuangwu et al. [52] discussed the thermodynamic behavior, stability, and the effect on the TSV process of two kinds of temporary adhesives (UV radiation and thermal cure). The results showed that the use of these two adhesives has their own limitations, and it is necessary to select a suitable adhesive according to the specific process conditions. In addition, in the 3D ultra-thin wafer stacking technology, it is required to develop a connection process using via holes with different aspect ratio. This TSV process requires reliable ultra-thin wafer handling techniques. Temporary bonding technology has become a relatively common ultra-thin wafer handling method in 3D stacking technology. Charbonnier et al. [55] described how a temporary bonding process could be used to fabricate a TSV with diameter of 65 μm on a 70 or 120 μm ultra-thin wafer. The process results showed that the parameters of the 8-inch ultra-thin wafer fabricated by this temporary bonding process fulfill the requirements of the next step (3D integrated dicing and stacking). Zoschke et al. [56] conducted a series of evaluations on wafer thinning and backside processes for temporary bonding techniques. These results indicated that the temporary bonding technology could be applied to the 3D integration system. One problem in ultra-thin wafers using temporary bonding techniques is the difficulty to accurately measure

the thickness of ultra-thin wafers due to the presence of adhesives and carriers. Optical method is currently used to measure the thickness of ultra-thin wafers, but the results of this method are easy to be affected by the material of the bonding layer and pattern on the wafer surface. Kim [57] measured the thickness of ultra-thin wafers by Fourier transform infrared spectroscopy (FTIR) and discussed the effect of different adhesive materials on the measured thickness. Although the results of this research proved that the optical method could measure the thickness of ultra-thin wafers, limitations of this method should not be eliminated. For instance, the optical measurement is not suitable for the wafer containing materials with low-transmittance, and the accuracy of optical measurement could also be reduced for the weakly bonded or non-bonded wafer due to the unclear heterogeneous interface. Therefore, it is necessary to develop a method for accurately measuring the thickness of a wafer in a multi-layer bonded wafer system.

In addition to the bonding of ultra-thin silicon wafers onto other substrates, silicon wafers themselves could also be used as carrier for the bonding of ultra-thin wafers of other materials [58]. Daix et al. [59] demonstrated 200 mm InGaAs-on-insulator wafer directly bonding to silicon receiver wafer. The bonding energy is ensured by deposition of Al_2O_3 thin film with thickness of 20–30 nm on both InGaAs surface and silicon receiver wafer. After the bonding, the thickness of InGaAs could be further reduced by a post-transferred CMP. This technique combines the advantages of wafer on insulator (low power and back biasing) with the high mobility of InGaAs channels (6000 $cm^2 V^{-1} s^{-1}$ measured by Hall effect and 2000–3000 $cm^2 V^{-1} s^{-1}$ extracted by field effect transistors).

3.2. Ultra-thin wafer without carrier

For the ultra-thin wafer without carriers, the traditional holder with mechanical contact between holder and the wafer to be held would induce contamination and mechanical stresses/damages to the wafer. Thus, non-contact holders should be employed for ultra-thin wafer transportation. Siniaguine et al. [60] invented a holder for wafer-like articles with at least one annular groove therein (Fig. 4a). The gas moving in the groove with diameter of d could be circulated in a clockwise or counter clockwise fashion (Fig. 4b), leading the formation of a vortex adjacent to the article facing surface. The vortex provides the dynamic to hold the wafer-like articles in accordance with Bernoulli principle (pressure in a stream of fluid reduces as the speed of flow increases) [61]. As shown in Fig. 4c, where the radius r is less than $d/2$, the ambient pressure is higher than the gas pressure in the gap. This positive pressure difference ΔP makes the wafer-like articles press to the holder. On the other hand, for the radius r greater than $d/2$, the negative pressure difference ΔP between ambient pressure and gas pressure in the gap pushes the wafer-like articles out of the holder. This is the reason why the wafer-like articles could be held in a suspended state without touching the holder. Considering the holder could hold the wafer in any orientation with no contact to the holder surface according to the dynamics mentioned above, the wafer transportation has two working models with the wafer either places below or lies above the holder. The gap height h between wafer and the holder would find an equilibrium to balance the weight W of the wafer. The annular groove might also be provided with plurality quantity. As illustrated in Fig. 4d, a plurality of the annular grooves is employed in an actual ultra-thin wafer holder with fork-shaped end to preventing any rotation of the wafer, where the blue dashed line represents the ultra-thin wafer being manipulated. Obviously, the advantage of Bernoulli method is the reduction of the ultra-thin wafer breakage risk and contamination without contact between holder and wafer. Thus, it is a mature ultra-thin wafer handling technology for photovoltaic industrial [62]. But admittedly, Bernoulli method does have limitations. First, it is not suitable for the ultra-thin wafer with large size, such as 12-inch ultra-thin wafer. Recently, Liu et al. [63] developed a distributed Bernoulli gripper for 8-inch ultra-thin wafer manipulation, where air flow rate and gap height are two key operation parameters. Second, Bernoulli method is also not suitable for the ultra-thin wafer transportation in vacuum due to the using of pressure difference to manipulate the wafer. Third, the air drag and the inertia forces of the wafer would aggravate the bending of the ultra-thin wafer or even lead to breakage when the ultra-thin wafer is moving with high speed in air through Bernoulli

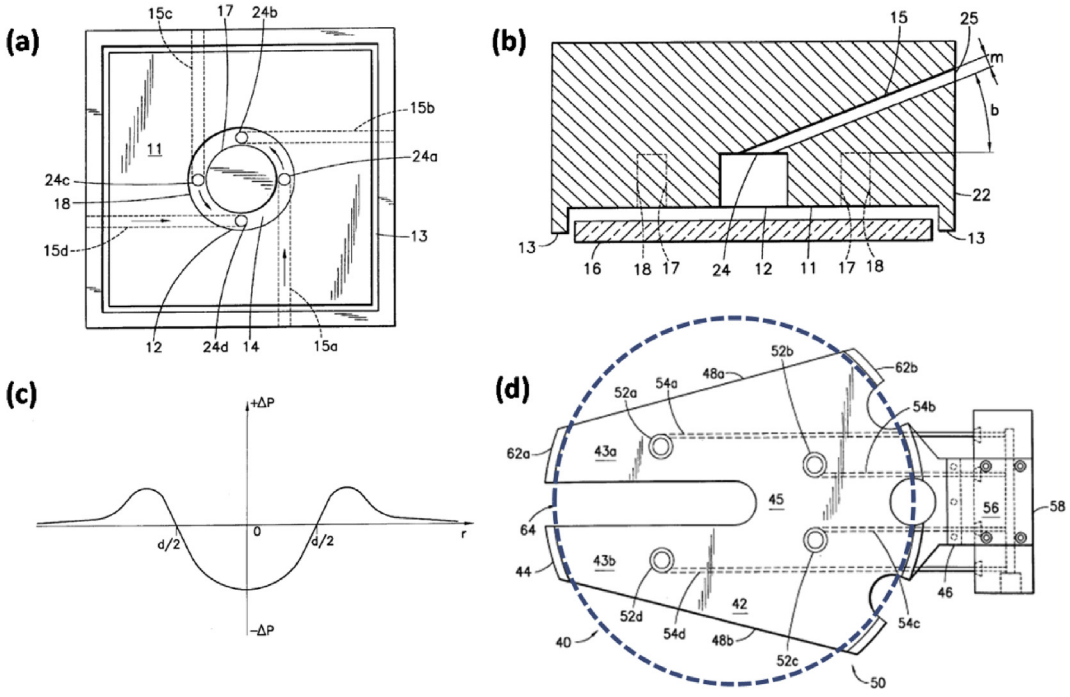

Fig. 4. The Bernoulli principle based ultra-thin wafer transfer holder: (a) top-view and (b) side-view of the gas moving annular groove integrated holder; (c) the distance dependent pressure difference of the holder; (d) plurality of the annular grooves employed robot arm for ultra-thin wafer transfer. Reproduced from Ref. [60].

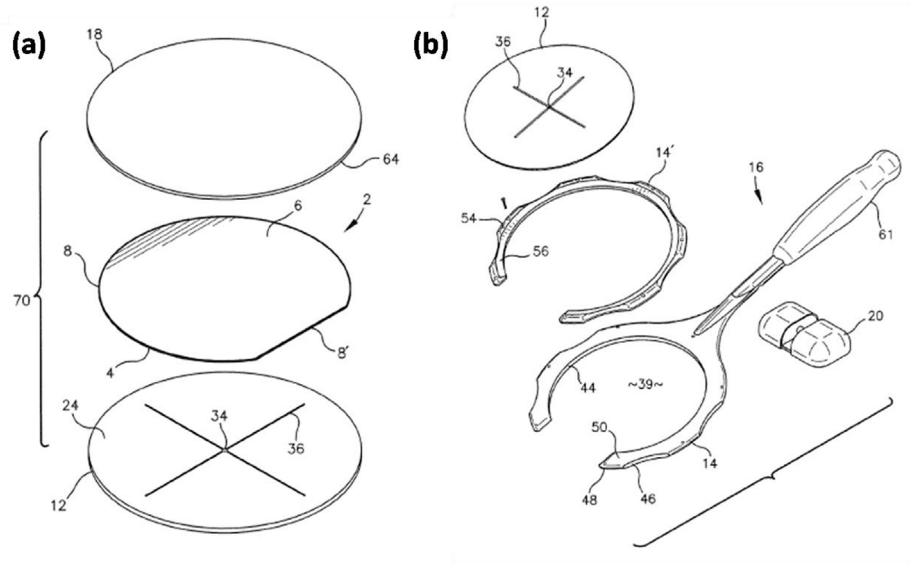

Fig. 5. The full dimension supporting apparatus for thin wafer transfer: (a) sandwich structure of the top disk, device wafer, and wafer transfer disk; (b) the elongated handle extending from the wafer transfer disk. Reprinted from Ref. [65].

method [64].

Another method to handle ultra-thin wafer, including debonded device wafer and wafer after backside processing, is employing full dimension supporting by a wafer transfer disk with non-stick and low bonding strength interface between the wafer-engaging surface and the device wafer [65]. The thickness of the debonded device wafer is usually less than 200 μm, or even more preferably less than 100 μm. As shown in Fig. 5a, the wafer transfer assembly contains a wafer transfer disk with an end effector for supporting it and an elongated handle extending from the end effector. The wafer transfer disk is made of thermally-stable materials, such as metals, polymers, glass, and ceramics, with thickness of about 0.3–0.6 cm. The non-stick property of the wafer-engaging surface is achieved by surface modifications, such as polishing and coating. A top disk with the same shape and size as the wafer transfer disk is employed to keep the ultra-thin wafer from warping or bowing during transfer (Fig. 5b).

The process for ultra-thin wafer transportation mentioned above requires special equipment which should be facilitated [49]. Due to the rising of TAIKO wafers and reduced damage to wafer surface through dry etching during wafer thinning, ultra-thin wafer transfers will evolve toward the same process as conventional wafers without using of special equipment. Bieck et al. [20] reported a kind of ultra-thin wafer with slit structure on its edge area which is very similar to the TAIKO wafers. The effective area of this kind of ultra-thin wafer without carrier could be increased due to the reduction of the stress concentration near the notch. This kind of ultra-thin wafer with thickness of 60 μm could be handled without wafer-support-systems (WSS). In contrast to ultra-thin wafer technology with carriers, mechanical stability is integrated into backside processing technology at the same time in ultra-thin wafer technology without carriers.

4. Ultra-thin wafer applications

The ultimate mission of ultra-thin wafer manufacturing and handling is to provide small-sized and high-performance semiconductor device fabrication. Ultra-thin wafer has a broad application in device fabrication, such as 3D package/TSV processing [39,49,66–68], power chip [21,27], solar cell [69–71], RFID (radio frequency identification device) [1], complementary metal oxide semiconductor (CMOS) device [32,72,73], and so on.

The wafer level chip size package (WLCSP) could achieve economies of scale because all the dies are packaged on the wafer at the same time rather than one die separately at a time, which fully complies with joint electron device engineering council (JEDEC) and surface mount technology (SMT) standards [66]. Thus, in WLCSP the dies should be thinned in wafer form which requires ultra-thin wafer technology, where thickness is a crucial factor in a variety of size sensitive electronic products. Furthermore, ultra-thin wafer also provides the geometrical advantage to create through contacts in the die. As the market demand for smaller electronic and optical devices grows, it is increasingly important to reduce the size and weight in package of integrated circuits. For ultra-thin wafers in the packaging process, such as thinning, handling, and dicing, it is especially significant to ensure that the ultra-thin wafers have sufficient strength without being broken. Vincent et al. [39] reported the effect of wafer thinning parameters on the die strength which impacts the integrity and reliability of the semiconductor device. The wafer thinning parameters they evaluated include spindle speed, feed rate, and chuck table speed. It is found that the dies have comparable strength when different the wafer thinning parameters used in the rough grinding, because the damage layer is deep enough. In contrast, the die strength decreases when the wafer TTV is improved in the rough grinding. For the ultra-thin wafer without carriers, Spiller et al. [18] reported the process of 300 mm ultra-thin wafer manufacturing, and sequentially verified the mechanical stability of the 300 mm ultra-thin wafer. After spinning, exposure and development of polymer on the ultra-thin wafer, Ti and Cu are deposited by PVD and electroplating. This process could be applied for TSV packaging and power devices. The experimental results also proved that the ultra-thin wafer fabricated by this process (without carriers) has obvious advantages in cost when it is compared with the ultra-thin wafer with carriers. In addition, DISCO GmbH has developed some advanced technologies in regarding to ultra-thin wafer technology, such as TAIKO wafer, laser dicing, and so on. It is also feasible to introduce plasma etching technology into TSV process based on TAIKO ultra-thin wafer [74].

In addition to the geometrical advantages in the packaging process, ultra-thin wafer could improve the device performance in power chips [18,21]. The on-state resistance $R_{DS(on)}$ from drain to source of the chip is one of the key figure-of-metrics for power chips, which should be as low as possible to conduct high current to its load (minimize the energy loss). As shown in Fig. 6, a typical vertical structured field effect transistor (FET) mainly contains gate electrode, source electrode and drain electrode, where the source-drain current could be regulated by the gate. In detail, this is a schematic of a NPN type FET with enhancement

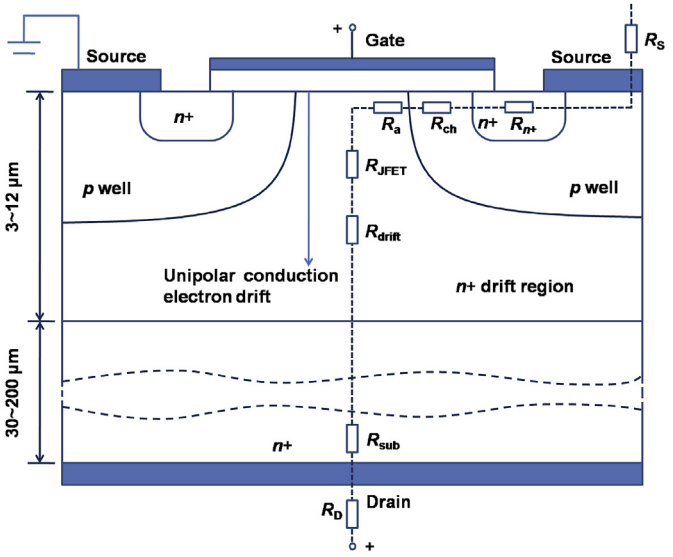

Fig. 6. Schematic of the resistances in a power device showing the R_{sub} is dependent on the wafer thickness without key electrical function. Adapted from Ref. [21].

mode. When a positive voltage is applied on gate electrode, the electrons in n-type semiconductor (in source and drain electrodes) are driving to the gate (the oxide layer or Schottky contact of gate electrode could prevent gate leakage current), which forms the on-state source-drain current $I_{DS(on)}$. When a negative or zero voltage is applied on gate electrode, the high channel resistance R_{ch} could switch off the device. Compared with the traditional mechanical power switch, the on-off regulation through gate in power chip could achieve high switching speed and avoid uncontrolled sparking. Though $R_{DS(on)}$ consists of many individual resistances, in the devices with vertical architecture where the current flows through the whole wafer, the device thickness has great impact on the $R_{DS(on)}$. Considering the major electrical function of the device is provided by the region with depth of dozens of microns in the wafer surface, the remainder of the wafer thickness just adds resistance R_{sub} to the power chip which should be as low as possible (Fig. 6). Thus, thinner silicon wafer could provide better device performance in power chips. For example, insulated gate bipolar transistor (IGBT) is a typical power chip with both high on-state current and fast switching speed, where ultra-thin wafer with thickness of 120 μm or less is demanded. This is because the power consumption is smaller and integration density is greater when the wafers for IGBT devices become thinner. TAIKO wafer has been used in field stop insulated gate bipolar transistor (FS-IGBT) fabrication due to its advantage of warpage and transportation [27]. Owing to the arising of the third-generation electronic materials with wide band gaps, such as gallium nitride and silicon carbide, the power device could be even thinner (1/10 thickness compared with that of silicon in theory).

Similarly, solar cell is another device seeking ultra-thin wafer technology due to the reduction of the internal resistance with lower wafer thickness. The probability of photo-generated carrier recombination is higher when the internal resistance is larger, which could reduce the open circuit voltage [69]. Besides, solar cells fabricated by ultra-thin wafers are flexible, low-cost and compatible with thin film technology. However, in contrast to power chip, wafer that is too thin in thickness is not the better for solar cell fabrication. This is because too thin in wafer thickness would reduce light absorption, which further reduces the power conversion efficiency (PCE). Thus, in industrial production line the wafer for solar cell fabrication typically has a thickness of 120–200 μm. Recently, by both theoretical and experimental investigations, the thickness of ultra-thin wafer for solar cell fabrication is proved to have the potential to be further reduced. Han et al. [70] designed surface nanostructures in thin crystalline silicon solar cell with an absorption toward the Lambertian limit through group theory, indicating a potential to further reduce the silicon thickness or mass. As for the experimental study, Zhang et al. [71] demonstrated plasmonic nanostructure is an effective strategy to increase light trapping, where the wafer thickness could be reduced to ~10% of the original thickness without obvious PCE loss, proving that reducing the silicon wafer thickness at a minimized efficiency loss is a practicable way for the development of crystalline silicon solar cell.

Moreover, radio frequency identification is to identify entities through radio frequency without physically contacting [1]. Ultra-thin wafer would provide the possibility to integrate RFID into thin foils or even paper documents. Thin RFID technology also facilitates the usage of organic compounds to build electronic transistors where high data rate could be achieved.

Furthermore, ultra-thin wafers have also been applied to the fabrication of CMOS devices. After the wet chemical thinning process, Watanabe et al. [32] analyzed the etched surface and fracture stress of the die by transmission electron microscopy (TEM) and electron energy-loss spectroscopy (EELS). Though the fracture stress introduced by this wet etching process is higher than other thinning processes, such as the back-grinding process, the MOSFET performance changes are small when thinning the CMOS wafers to 50 μm by this wet etching process. Kim et al. [73] reduced the wafer thickness to less than 10 μm using high-resolution grinding techniques equipped with Auto-TTV and non-contact gauge (NCG) methods. The measurement of the impact of ultra-thin wafer on the CMOS logic and FRAM device electrical performance showed that the bonding, thinning, and debonding processes have no effect on the electrical properties of the device. On this basis, they [72] thinned 300 mm wafers to 4 μm for 2 GB DRAM at 40 nm node for the first time, and the ultra-thin wafer surface uniformity was about 1 μm. After the wafer was thinned, the retention and distribution characteristics of the 2 GB DRAM were not deteriorated, indicating the bonding and debonding processes do not bring damages to the devices. These results shown above demonstrated that CMOS logic devices, FRAM and DRAM memory devices could achieve 3D integration.

5. Conclusion and outlook

In summary, with the increasing semiconductor device integration density, device performance and market demand in recent years, ultra-thin wafer has become important building block in semiconductor device manufacturing. Reduced wafer thickness means the increasing difficulty of manufacturing and manipulating of the corresponding ultra-thin wafers. These processes are integrated ones that cannot be considered for splitting, together with application of ultra-thin wafers. The mechanical grinding followed by stress relief through polishing or etching has become the standard wafer thinning process, and the ultra-thin wafer transportation would no longer require special equipment due to the rising of TAIKO wafers. Thus, ultra-thin wafer has significant impact on semiconductor industrial with broad applications in its current status.

Looking into the foreseeable future, investigation on ultra-thin wafer could still be a hot topic, and the related researches would be carried out in full swing. For the ultra-thin wafer manufacturing, it is not doubted the ultra-thin wafer would become thinner and thinner with thickness of several micrometers or even hundreds of nanometers in the near future, where dry etching should be an indispensable method for obtaining ultra-thin wafer. Correspondingly, the development of dry etching has mainly two roads. One is to increase etching rate or manufacturing through-put, and another one is to expand its inherent advantage of effective stress relief or damage remove [75]. Following the Moore's Law, it has increasing demand of wafer surface quality for the reason that devices are getting smaller. The improved wafer roughness by dry etching could reduce the issues in epitaxial process or even eliminate it. For the ultra-thin wafer manipulating,

Bernoulli method would be improved to handle the ultra-thin wafer with large size. With the increasing of automation in semiconductor industrial, it seeks reduction of the time and distance for ultra-thin wafer transportation. For the ultra-thin wafer application, a wider variety of devices might adopt ultra-thin wafer. For instance, in micro-electro-mechanical system (MEMS) device, the ultra-thin wafer could bring flexibility into it, making wearable devices compatible with traditional silicon electronics. Ultra-thin wafer could also reduce degradation time of implantable devices in living organisms. In all, ultra-thin wafer technology is valuable for both scientific and industrial communities with broader applications in the near future.

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