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Impact of contact integrity during thermal stress testing on degradation analysis of copper-plated silicon solar cells

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ABSTRACT

In this study, silicon solar cells with copper-plated front side metallisation were exposed to long-term reliability thermal stress conditions and the material integrity of the plated contacts after stress testing was investigated using imaging and electrical measurements. Significant voltage 'bend-back' was observed in Suns-V_{OC} measurements at high illumination intensities (> 1 Sun) following thermal stress testing at 200 °C for 500 h of laser-ablated cells with a nickel/copper/silver plated front metal grid. Using a combination of focussed ion beam milling, high resolution imaging and energy dispersive X-ray spectroscopy, it was shown that large voids can form between the silver capping layer and the main copper stack during thermal annealing. However, even more revealing was the detection of a new metal layer comprising largely of diffused copper overlying the silver capping. The cause of the Schottky 'bend-back' behaviour was theorised to be due to increased contact resistance arising from the voids which are presumed to form as a result of grain boundary diffusion of copper through the silver capping layer. Errors of 5–10% in the determination of *pFF* from Suns-V_{OC} occur as a result, with the scale of the error dependent on the capping method and sintering conditions. Collapsing the voids was subsequently shown to remove the Schottky behaviour and improve reliability of the fitted diode parameters extracted from Suns-V_{OC} measurements.

1. Introduction

Front contact metallisation, which is predominantly achieved by silver (Ag) screen-printing, remains one of the most costly and critical steps in solar cell production [1]. Copper (Cu) plating is frequently presented as the obvious candidate to replace screen-printing, offering lower cost and higher performance capabilities, with plating-based technologies expected to hold increasing market share (~10%) over the next 10 years [2,3]. Despite this, widespread adoption of plating in industrial cell manufacturing is slow due to several issues, namely metal contact adhesion to silicon (Si) and long-term reliability concerns related to Cu penetration into the underlying Si wafer [4]. Copper is highly mobile and can diffuse readily in silicon where, in sufficient concentrations, it can lead to significant degradation in a cell's electrical performance due to the formation of recombination centres typically including Cu precipitates [5–7]. To mitigate this issue, an intervening metal layer is often employed as a diffusion barrier, with nickel (Ni) most commonly used in plated solar cells [8,9]. However, variability in barrier quality can reduce its effectiveness [10–12] and thus some form of reliability testing is required to assess the stability of plated barrier layers on silicon solar cells.

In order to study the reliability of plated solar cells, an accelerated aging test was reported by Bartsch et al., whereby plated cells are exposed to elevated temperatures for extended periods to simulate long term operation, with a reduction in pseudo fill factor (*pFF*) being used as an indicator of copper-related degradation [13]. By monitoring *pFF*, the effects of series resistance in the cell are eliminated, thereby providing more accurate analysis of the diode quality of the cell which can be used as an indicator of enhanced recombination due to Cu defect formation in or close to the space-charge region. It has been proposed that this method can be used to predict cell lifetime under field conditions, with sufficient long-term reliability of plated cells having been demonstrated in several studies [14–17]. However, the Suns-V_{OC} technique [18] which is used to extract *pFF* values can be influenced by properties of the contact such as contact resistance, and poor contact material integrity can result in non-ohmic behaviour which can lead to errors in extracted diode parameters. The possibility of degraded contact integrity in these tests has major implications for the accuracy of

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long-term reliability tests using this method, as minor errors in degradation measurements can have large impacts on the estimated lifetime of plated cells [13].

In this study, silicon solar cells with plated Ni/Cu/Ag stacks underwent thermal stress testing to assess the material integrity of the contacts and the electrical properties of the cells after extended exposure to elevated temperatures. A combination of electrical and material characterisation techniques were used to investigate changes in contact structure and analyse the influence of changes in that structure after thermal stress testing on extracted diode parameters via Suns-V_{OC} measurements. Insights were gained into the impact of cell metallisation degradation on the analysis and assessment of long-term reliability via Arrhenius modelling. The study also highlights the propensity of Cu to diffuse through polycrystalline metals at relatively low temperatures and therefore raises further concerns about Cu diffusing through Ni barrier layers and penetrating the silicon of the cell.

2. Experimental

2.1. Sample preparation and thermal stress testing

Cells were fabricated using 156 mm boron-doped 1–3 Ω cm Czochralski (Cz) silicon wafers with random-pyramid texturing. A phosphorus-doped emitter with a sheet resistivity ~110–120 Ω/□, surface concentration of ~2×10^{19} cm^{-3} and junction depth of ~0.4 μm was formed using $POCl_3$ diffusion. After rear etching, a 75 nm silicon nitride (SiN_x) anti-reflection coating was deposited using direct plasma enhanced chemical vapour deposition (PECVD) and a full-area aluminium rear contact was screen-printed and fired to form a full-area back surface field (BSF).

Small cell contact grids (25 mm × 25 mm cell area) were patterned on the front surface using a 266 nm ps Lumera Super Rapid Nd: YAG laser with a BBO crystal for the 4th harmonic, with an average laser fluence of 0.44 J/cm^2 and 37% pulse overlap being used to form both the fingers and busbars. The ablated finger width was 13 μm and a finger spacing of 1.5 mm (16 fingers in total) was used to form the metal grids via stage scanning. Busbars 1 mm-wide were ablated with a 9 μm pitch between adjacent laser scans using stage scanning. After removal of the native oxide by immersion of the front surface in 1% (w/v) hydrofluoric acid (HF), front contacts were formed on the exposed Si by plating a stack of Ni (~1 μm) and Cu (8–10 μm) using bias-assisted light induced plating (LIP) with Barrett SN1 Ni sulphamate (MacDermid Inc.) and Helios EP2 Cu (MacDermid Inc.) plating solutions, respectively. Bias currents of 23 mA/cm^2 and 40 mA/cm^2 were used for Ni and Cu LIP, respectively.

Two different capping methods were used – Ag capping with bias-assisted LIP (MacDermid Helios Silver EPF 400), and capping with a Ag immersion solution (MacDermid Helios Silver IM 452). The average thicknesses of the capping metals were ~1.0 μm and ~0.3 μm respectively. Each 156 mm cell precursor contained 25 small cells, so individual cells were laser cleaved after plating for edge isolation, characterisation and further processing. Some samples were sintered in a rapid thermal processing (RTP) furnace at 350 °C for 1 min in N_2 ambient before characterisation, whilst other samples were characterised without sintering. One cell from each set was used as a control for contact characterisation and did not undergo thermal stress testing. Cells were exposed to 200 °C in a muffle oven with N_2 ambient for 500 h to simulate long-term operation at elevated temperatures.

After thermal annealing at 200 °C, some cells were quenched in ethylene glycol (cooling rate ~1000 K/s) immediately after thermal treatment followed by rinsing in DI water while the remaining cells were cooled under ambient conditions (cooling rate ~4 K/s). The different quenching methods were examined because Flynn et al. [19] had previously shown that quenching after thermal annealing of laser-doped Ni/Cu-plated cells can result in the formation of Cu precipitates close to the laser-doped surface and reduce photoluminescent imaging intensity, whereas no Cu precipitates were able to be detected with slow cooling. The impact of cooling rate on Cu out-diffusion and precipitation in Si has also been observed in several other studies [20,21]. This study aimed to see whether the quenching process contributed to any changes in the contact integrity after thermal annealing.

2.2. Cell characterisation

Cells were electrically characterised before and after thermal exposure using a combination of light and dark *I-V* measurements using a calibrated in-house constant illumination *I-V* tester under standard test conditions. Suns-V_{OC} measurements were performed using a Sinton Instruments Illumination-voltage tester, with Suns-V_{OC} being measured at three points along the 25 mm long busbar (one at each end of the busbar and one in the centre). Characterisation of the contact structure at regions of interest was performed by obtaining cross-sections using single beam focussed ion beam (FIB) milling (FEI XP200), followed by high-resolution imaging of the contact cross-section. Transmission electron microscope (TEM) specimens were then prepared using the FEI XP200 and TEM imaging was performed with a Philips CM200 TEM system. Energy dispersive X-ray Spectroscopy (EDS) measurements were obtained with a Bruker SDD detector.

3. Results and discussion

The first indication of thermally-induced contact damage impacting plated cell characterisation can be observed in the Suns-V_{OC} curve in Fig. 1. This response was measured for a Cu-plated cell with a LIP Ag capping layer that had been annealed at 200 °C for 500 h with the reversal in the open-circuit voltage (V_{OC}) occurring at illumination intensities greater than ~2 Suns. This V_{OC} 'bend-back' can indicate the presence of a Schottky barrier between the probe and the Si, the diode resulting in an opposing voltage to the cell junction voltage at high illumination intensities. This phenomenon has been previously described [18,22,23], usually in relation to rear point contacts. It has also been reported for plated laser-doped bifacial cells, where insufficient p-type dopants were incorporated at the laser-doped contacts [24].

Contacts can be modelled as a Schottky diode in parallel with a shunt resistance, the latter representing the contact resistance of the metal to the Si as depicted in Fig. 2. At a well-formed contact, the Schottky diode is bypassed by the shunt resistance and no voltage exists over the diode at the metal-Si interface. However, if the contact between the probe and Si is highly resistive, then at illumination intensities above normal operating conditions, current cannot be

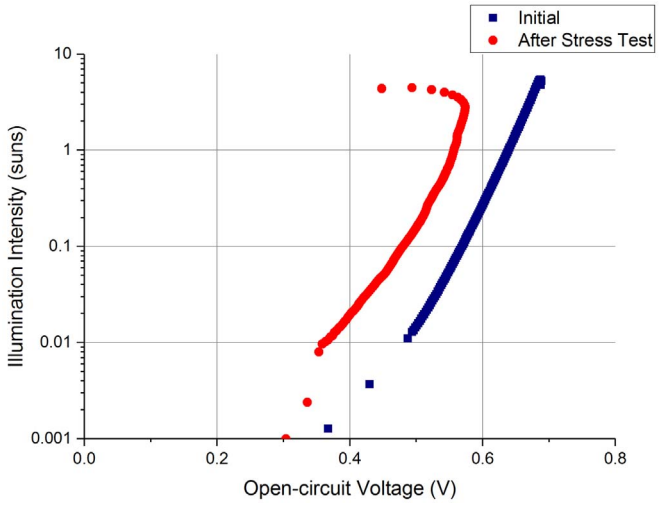

Fig. 1. Suns-V_{OC} curve measured on a Cu-plated solar cell with a LIP Ag capping layer (sintered) before and after thermal exposure at 200 °C for 500 h.

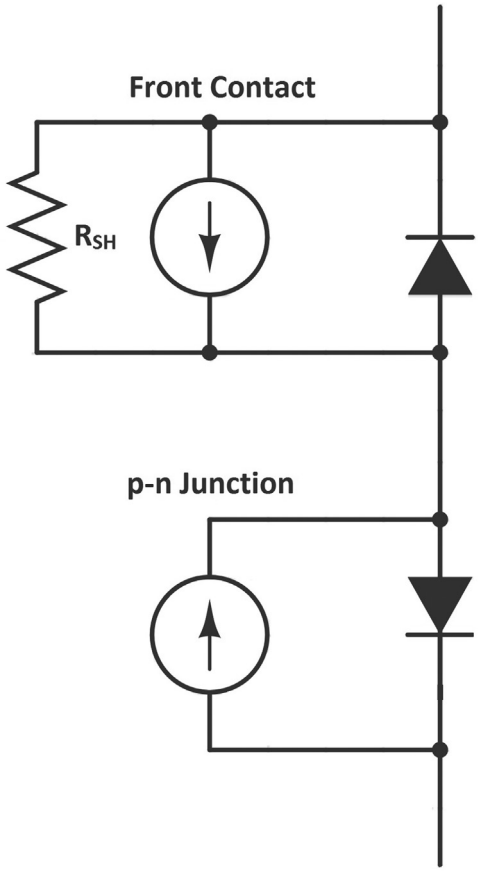

Fig. 2. Equivalent circuit diagram that can be used to model the Schottky behaviour of a thermally-aged front plated Ni/Cu/Ag contact in relation to the solar cell p-n junction.

extracted from the cell through the shunt resistance, resulting in voltage build-up across the Schottky junction. Since the characteristic 'bend-back' behaviour was not observed in Suns-V_{OC} measurements recorded before thermal stress testing (see Fig. 1), the observed non-ohmic behaviour after thermal annealing indicated some degradation at the front contact due to the prolonged exposure of the cell to elevated temperatures.

The effect of this Schottky behaviour was also evident when comparing V_{OC} results obtained by both *I-V* and Suns-V_{OC} measurements. For cells exhibiting Schottky 'bend-back' in the Suns-V_{OC} curve, there was a significant reduction in the 1-Sun V_{OC} measured when compared to V_{OC} values measured on the same cells using an *I-V* tester. Additionally, the severity of the voltage mismatch between the *I-V* and Suns-V_{OC} measurements varied between different front contact structures and processing sequences. Fig. 3 graphs V_{OC} values obtained from *I-V* and Suns-V_{OC} measurements. As is clear from the graph, the V_{OC} mismatch was significantly larger (up to 100 mV) in cells plated with a LIP Ag capping layer (labelled LNS and LS in Fig. 3). Plated cells that were capped with an immersion Ag layer (INS and IS) resulted in a significantly smaller mismatch in V_{OC} (up to ~50 mV). Regardless of the Ag capping method used, the largest mismatch occurred in plated cells that had undergone sintering prior to thermal stress testing. However, no clear correlation was evident between cooling method (i.e., quenched or non-quenched) and the severity of the V_{OC} mismatch.

In order to understand the underlying cause of the Schottky contact formation in the different plated contact stacks, FIB cross-sectional images were obtained on plated cells before and after annealing at 200 °C for 500 h in N_2 (examples from sintered cells can be seen in Fig. 4). The images show no evidence of void formation or separation of the metal stack at the Ni/Si or Ni/Cu interfaces in any of the cells before annealing. However, voids are clearly evident between the Cu and the

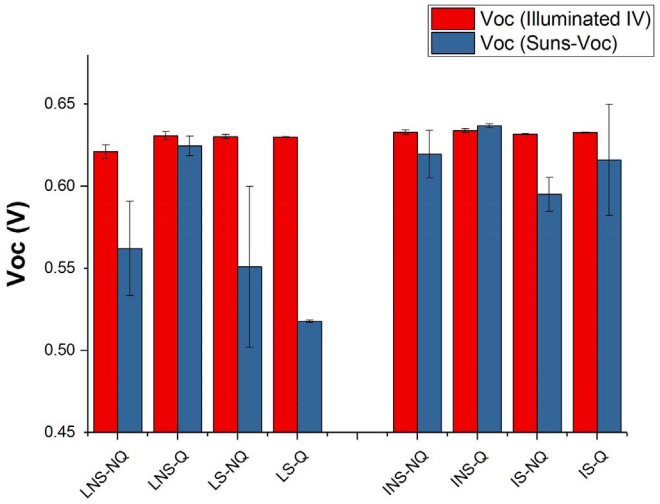

Fig. 3. Comparison of V_{OC} measurements on different Ni/Cu/Ag plated cells using *I-V* and Suns-V_{OC} measurements. The cell processing sequence can be identified by the labels: L/I = LIP Ag/Immersion Ag, NS/S = no sinter/sinter, NQ/Q = no quenching/quenching.

Ag capping layer. These voids were several micrometres long in the LIP Ag capped cells (Fig. 4d) while in the immersion Ag cells (Fig. 4c) they are smaller and more dispersed. Furthermore, a new layer (with a thickness of 0.5–1.5 μm) appears to have formed above the capping Ag in both the LIP Ag and immersion Ag capped cells. This newly-formed surface layer resulted in a clear discoloration of the plated contacts uniformly across both LIP Ag and immersion Ag cells, the surface changing from the bright white-grey of the plated Ag to a much darker grey appearance. Subsequent TEM/EDS analysis of these cross-sections revealed that this new layer above the capping Ag metal is in fact a second layer of Cu that has formed during thermal stress testing. The EDS line scan in Fig. 5 identifies this layer to be predominantly Cu, but with a small amount of O also being detected. The EDS map in Fig. 6 more clearly shows the separation of the two distinct Cu regions by the Ag capping layer, with TEM/EDS analysis also able to confirm the presence of the voids observed in the FIB cross-sectional images.

The presence of such a significant layer of diffused Cu on top of the Ag capping layer is surprising, although not entirely unexpected. Studies on the diffusivity of Cu through different barrier layers have shown that most barriers act as a retardant to Cu diffusion rather than a complete barrier [21,25]. Diffusion of Cu through plated metals can occur via two mechanisms – lattice diffusion and diffusion along defects such as dislocations and grain boundaries. Mass diffusion of Cu through electroplated gold (Au) capping layers at different temperatures has been previously reported [26,27]. Pinnel and Bennett [26] showed that the diffusion coefficient of Cu at low temperatures (≤ 250 °C) was much higher than predicted when extrapolating the high-temperature Arrhenius relationship, estimating that, at these lower temperatures, the activation energy for Cu diffusion in Au was ~ half that observed at high temperatures, where diffusion through the lattice occurs. At lower temperatures, Cu diffusion along grain boundaries and dislocations in the electroplated metal is the dominant diffusion mechanism. Tompkins and Pinnel subsequently estimated that at 150 °C, the rate of growth of a diffused Cu layer over the electroplated capping layer was ~45 Å per day [27].

Models of grain boundary diffusion typically assume an empty 'pipe' (i.e., a grain boundary or dislocation) and an 'infinite sink' at the surface. A sink is usually assumed to be a chemical reaction at the surface such as oxidation of the Cu, with an 'infinite sink' signifying that the rate of diffusion is slower than the rate of the surface reaction. Tompkins and Pinnel showed that for Au-capped Cu on printed circuit boards, different 'surface sinking' environments could impact the rate at which the Cu penetrated the Au capping layer. Annealing samples in a

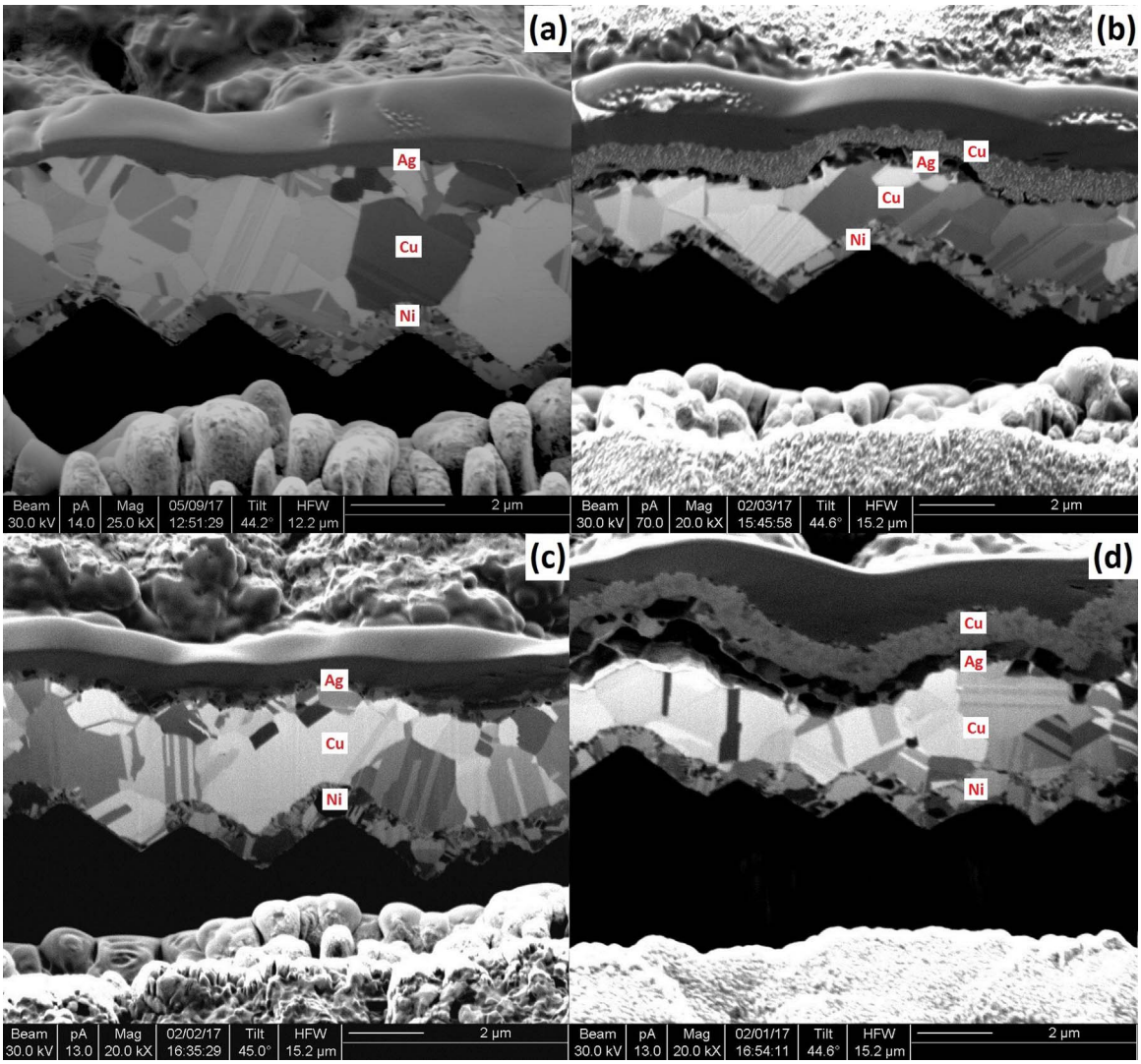

Fig. 4. Cross-sectional FIB Images of Ni/Cu/Ag plated and sintered contacts with different capping layers before and after thermal testing: (a) immersion Ag before; (b) immersion Ag after; (c) LIP Ag before; and (d) LIP Ag after. The average thickness of the Ag capping layer was 0.3 and 1 µm for the immersion Ag and LIP Ag cells, respectively.

vacuum resulted in less Cu transport through the capping layer than when samples were annealed in air, where Cu at the surface could be oxidised thereby providing a more effective 'sink' reaction. However, even more extensive Cu transport through the Au was observed when the Cu/Au samples were annealed on the printed circuit board. During annealing, chlorine (Cl) was released from the board, and it was proposed that the Cl could react with the Cu as traces of Cl were detected in the surface Cu layer [27]. Due to this low temperature diffusion mechanism, impurities such as tungsten, phosphorus or nitrogen have been used to eliminate or reduce effectiveness of such defect diffusion paths and improve the ability of barrier metals to retard the diffusion of Cu [28–30].

For the present study, it was not clear what surface reaction provided the 'surface sink' given that the cells were annealed in N_2, which should have minimised surface Cu oxidation. Without such a sink, the diffusion channels through the Ag would have been expected to become saturated and reduce the amount of Cu transported through the capping layer. However, a small amount of O was detected in the EDS analysis of the surface Cu layer after thermal annealing. This may have been due to low levels of O being present in the muffle furnace during annealing, or due to impurities that may have been incorporated in the plated stack during deposition. It can be very difficult to completely eliminate O at each of the Si, Ni and Cu surfaces while plating and during sintering/annealing, desorption of such impurities to the surface may offer an appropriate sink [31,32].

Although models of varying complexity have been proposed to describe grain boundary diffusion [33–35], the dependence of the diffusive mass transport on the specifics of the crystal structure (e.g., grain size, impurities at the grain surfaces, boundary width and tortuosity) and the varying nature of the surface sink makes it difficult to directly apply previous measurements of Cu diffusion rate to the current system of Cu diffusion through a plated Ag capping layer. The grain structure of the Ag capping layer depends on the deposition method, with LIP layers typically being thicker (~1 µm in this study) and comprising larger grains whereas the immersion Ag layers are thinner (< 0.5 µm) with smaller grains. Sintering is known to increase grain size [36], and in doing so may have provided more effective paths for Cu diffusion through the Ag capping layer, which may have resulted in the observed non-ohmic behaviour of sintered cells with both types of Ag capping layer.

The formation of the voids through grain-boundary diffusion is not dissimilar to the formation of Kirkendall voids [37] during high temperature inter-diffusion when through-lattice diffusion dominates. If the diffusion coefficients of the metals differ, then inter-diffusion can result in the formation of vacancies in the metal with the higher diffusion coefficient. These vacancies can then coalesce to form voids. The

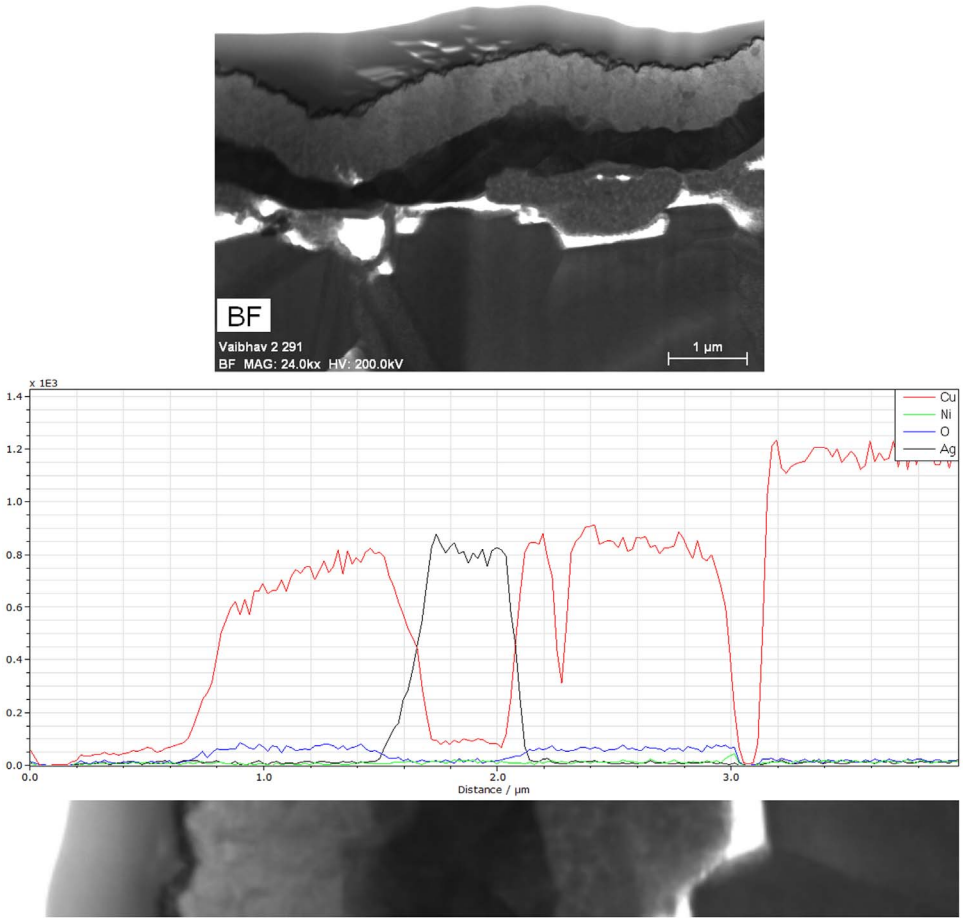

Fig. 5. High-resolution TEM Image (top) and an EDS line scan across a plated Cu contact stack capped with LIP Ag (bottom).

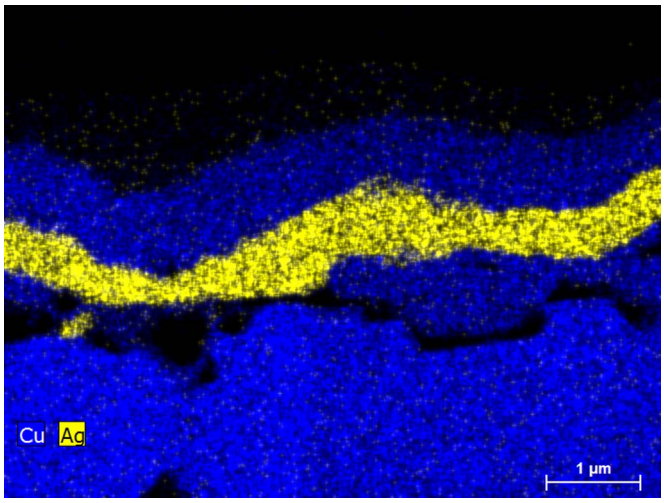

Fig. 6. EDS map taken at the Ag/Cu interface of a plated and sintered contact with a LIP Ag capping layer.

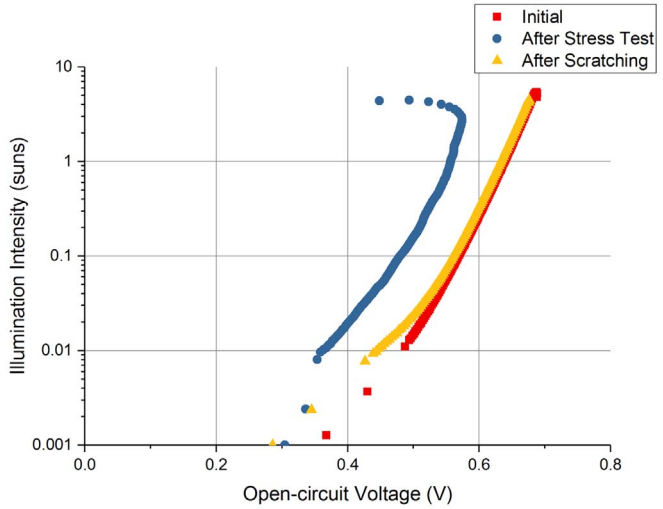

Fig. 7. Comparison of Suns-V_{OC} curves obtained before and after 'scratching' of the busbar region on a plated solar cell with a LIP Ag capping layer (sintered) after 500 h at 200 °C.

Kirkendall effect has been shown to be responsible for the creation of voids in local aluminium back surface field formation through Si-Al alloying [38,39]. Void formation due to Cu diffusion has also been observed for Cu electromigration [40], where net fluxes of Cu occurred between grains. The more extensive voids that were observed for the LIP Ag capping layers may be a result of less tortuous diffusion paths through the larger grains, or due to a different 'surface sink' reaction due to the different impurities incorporated during both the Cu and Ag plating.

In an attempt to eliminate the Schottky behaviour in Suns-V_{OC} measurements, the busbar regions that were originally measured were 'scratched' with a probe and the Suns-V_{OC} measurement was repeated for some cells. Fig. 7 shows that this 'scratching' eliminated the Schottky behaviour and the measured V_{OC} was similar to that measured using the calibrated *I-V* tester. Small differences in V_{oc} were expected due to the different light sources used in the Suns-V_{OC} and *I-V* measurements (flash lamp compared to steady-state halogen lights).

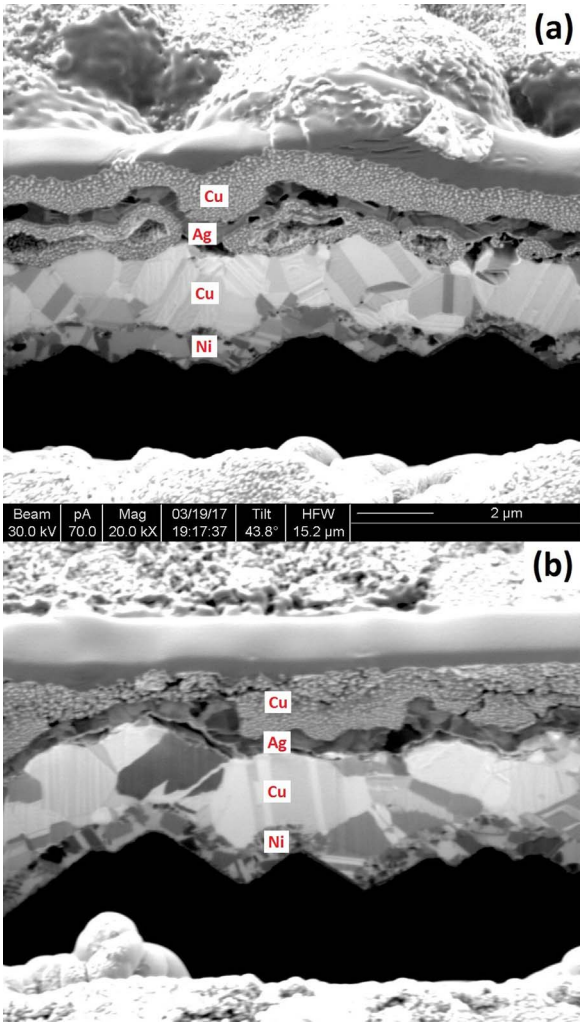

Fig. 8. Cross-sectional FIB Images of plated contact (sintered) with a LIP Ag capping layer (a) before 'scratching' the busbar and (b) after 'scratching' the busbar.

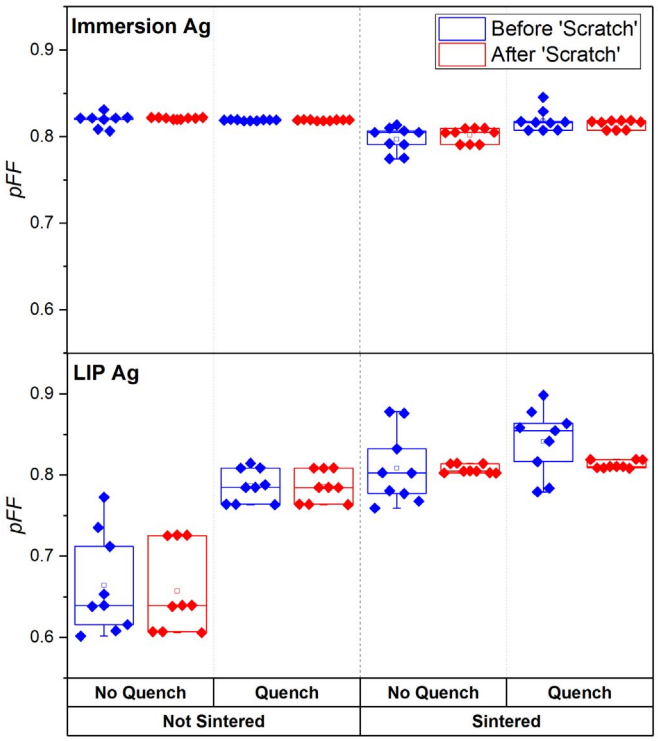

Fig. 9. Summary of *pFF* estimates obtained by Suns-V_{OC} measurements on plated solar cells with different processing sequences.

Voltage mismatch may also occur due to differences in the probes used (needle-type probe compared to flat/blunt probe), although needle-type probes were used in both *I*-V and Suns-V_{OC} measurements so this effect should be minimal. Although this result could be interpreted as evidence for the presence of a resistive oxide on the surface (cuprous oxide is known to act as a semiconductor [41], potentially creating a Schottky barrier at the surface), the FIB images in Fig. 8 tell a different story. It appears that the main effect of the busbar 'scratching' was to collapse the voids at the Cu/Ag interface. Thus, it was theorised that the presence of voids in the Cu/Ag interface has the effect of essentially reducing the contact area between the probe and the cell underneath, which increases contact resistance [22]. Tompkins and Pinnel did not report the formation of voids at the Cu/Au interface, although they did report a large increase in contact resistance after low-temperature annealing (10 mΩ to > 10 Ω after annealing at 125 °C for 5 days) [27]. By collapsing the voids, the contact resistance between the probe and Si was reduced, thus eliminating the Schottky behaviour from the Suns-V_{OC} measurement. Hence, it can be confirmed that the cause of the Schottky behaviour in these cells was not due to the diffused layer of Cu overlying the Ag, but the formation of voids underneath the capping layer.

These results suggest that when performing a cell lifetime estimation using the *pFF* technique reported in [13], it is important to check for the presence of any Schottky behaviour in the Suns-V_{OC} measurement. Fig. 9 summarises the *pFF* results obtained in this study, both before and after 'scratching' the busbar. The spread in *pFF* is significantly greater in the data obtained before 'scratching' (blue results in Fig. 9), with both underestimations and overestimations of *pFF* occurring. The value of *pFF* differed by 5–10% compared to that measured after 'scratching' the busbar, with variations also occurring between the three different Suns-V_{OC} measurements along the busbar. After 'scratching', all three measurements produced similar outputs for diode parameters and *pFF* indicating improved contact uniformity. The spread of the data was greatly reduced after 'scratching', with the remaining spread a result of variations between individual cells in each batch. The low *pFF*s of the non-sintered, non-quenched LIP Ag cells were most likely the result of laser ablation and plating variability. They resulted in a more significant degradation of the cell after extended thermal exposure at 200 °C. Current studies of long-term plating reliability based on the method developed by Bartsch et al. set a threshold for cell degradation at 5% reduction in *pFF* [13–15]. By performing the same measurements at different temperatures, a group of time-temperatures combinations can be plotted into an Arrhenius relationship which can then be extrapolated to estimate the time required to reach the same degradation state under field conditions. However, since the diffusion behaviour described by this Arrhenius relationship is exponential, small uncertainties can result in significant differences in estimated lifetime. Thus, a 5–10% variation in *pFF* could lead to an incorrect determination of threshold degradation time for a certain temperature, which will shift the Arrhenius plot, leading to an incorrect estimation of cell lifetime. The behaviour presented here may be an extreme case, but it highlights the importance of checking contact integrity when using *pFF* values obtained from Suns-V_{OC} measurements to establish long-term reliability of Cu-plated cells.

Another very important question raised by this study is whether Cu diffuses through Ag capping layers in encapsulated modules operating in the field, and if this occurs what is the impact. If this was to occur, then Cu would be expected to come into contact with encapsulant and evidence of Cu reaction with encapsulant should be apparent. Alternatively, Cu diffusion through the capping metal may potentially

impact the long-term reliability of solder joints in interconnected cells. However, there are no reports of either of these effects to the authors' knowledge. The temperature of 200 °C used in this study is significantly higher than expected field temperatures, and so some cells were exposed to a typical field-operating temperature of 80 °C for 500 h. At this annealing temperature there was no evidence of voids at the Cu/Ag interface or a diffused Cu layer above the Ag in the contacts of cells capped with immersion Ag and LIP Ag, suggesting that the Cu diffusion only occurs at a higher temperature. It would be useful in the future to determine the threshold temperature for this Cu grain boundary diffusion, as it may shed further light on the possibility of Cu diffusion through plated (polycrystalline) Ni barrier layers. Another key difference between the cell tests reported in this paper and module operation in the field, is that the sink reaction for the grain boundary diffusion will be different in the module where the Ag surface of the contact is sealed within encapsulant. Plated modules operating in the field have shown no evidence of early failure after 12 years of operation, indicating that this effect may not occur in encapsulated modules [42]. However, future studies will attempt to quantify threshold temperatures for Cu diffusion through Ag capping layers and determine whether a similar Cu diffusion phenomenon occurs in Cu-plated modules.

4. Conclusion

Copper-plated solar cells exhibited significant voltage 'bend-back' at high illumination intensities in Suns-V_{OC} measurements performed following thermal stress testing at 200 °C for 500 h. This Suns-V_{OC} behaviour has been observed previously and has been attributed to Schottky diode properties at the metal-Si interface becoming dominant in the presence of high contact resistance. An examination of the plated contact cross-section revealed the presence of voids at the Cu/Ag interface and a thick layer of diffused Cu on top of the Ag capping layer. It was hypothesised that the voids form due to grain-boundary diffusion through the capping metal, this hypothesis being supported by previous reports of low-temperature Cu diffusion along dislocations and grain boundaries of polycrystalline metals. The voids increase the contact resistance between the probe and the Si, resulting in the observed Schottky behaviour in Suns-V_{OC} measurements. It was shown that by 'scratching' the busbar with the measurement probe, the voids could be collapsed, after which Schottky behaviour was no longer observed in Suns-V_{OC} measurements.

The extent of void formation was significantly greater in cells that were capped with a LIP Ag layer compared to cells capped with immersion Ag despite the immersion Ag capping layers typically being slightly thinner. This may be due to the Ag capping produced by LIP being more polycrystalline due to the electrodeposition process. Sintering in an RTA at 350 °C after plating also increased the likelihood of the 'bend-back' being evident in the Suns-V_{OC}. Sintering has been shown to cause grain growth, with impurities being gettered to grain boundaries. This may act to increase grain boundary diffusion of Cu.

Although diffusion of Cu through the capping metal may raise concerns about plated module reliability, it was shown that if the thermal testing was performed at the lower temperature of 80 °C, then void formation could be avoided and no diffused Cu layer was evident. Furthermore, because grain boundary diffusion is driven by the presence of 'sinks', the encapsulant surrounding the metal may eliminate 'sink' reactions that were present in this cell study. Further studies that attempt to determine the heat treatment threshold for this Cu diffusion could clarify this situation, however present knowledge would suggest that this phenomenon is most relevant to thermal annealing tests designed to predict plated Si PV module lifetime.

This study highlights the importance of checking metal contact integrity before using Suns-V_{OC} measurements of *pFF* for lifetime estimates of plated Si solar cells. The error in the *pFF* measured for cells with voids was 5–10%. Although in extreme cases the 'bend-back' in the Suns-V_{OC} curve may indicate a possible problem, in less extreme cases or when high light intensities are not used for the measurement, small errors may pass unnoticed. These small errors can result in significant deviations in the Arrhenius analysis used in lifetime estimation of plated solar cells.

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