Analysis of the forward and reverse bias *I-V* characteristics on Au/PVA: Zn/n-Si Schottky barrier diodes in the wide temperature range

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In this study, the forward and reverse bias current-voltage (*I-V*) characteristics of Au/Zinc acetate doped polyvinyl alcohol/n-Si Schottky barrier diodes (SBDs) have been investigated over the temperature range of 80-400 K. The values of zero-bias barrier height evaluated from forward and reverse bias *I-V* data, (Φ_{BFo}) and (Φ_{BRo}), increase with increasing temperature, and a discrepancy is observed between the values of Φ_{BFo} and Φ_{BRo}. Because the apparent barrier height (BH) seen from metal to semiconductor is higher than the one seen from semiconductor to metal, the obtained value of Φ_{BFo} is always greater than Φ_{BRo} value. The difference between them is almost the same as the Fermi energy level. The crossing of the experimental forward bias semilogarithmic ln *I-V* plots appears as an abnormality when compared to the conventional behavior of ideal SBDs. This behavior was attributed to the lack of free charge at a low temperature and could be expected in the temperature region where there is no carrier freezing out, which is non-negligible at low temperatures. Prior to intersection, the voltage dependent value of resistance (R_i) obtained from Ohm's law decreases with increasing temperature, but it begins to increase after this intersection point. Such an increase in Φ_{Bo} and series resistance (R_s) with temperature corresponding to high voltage region is in obvious disagreement with the reported negative temperature coefficients. However, the value of shunt resistance (R_{sh}) corresponding to a low or negative voltage region decreases with increasing temperature. In addition, the temperature dependent energy density distribution profiles of interface states (N_{ss}) were obtained from forward bias *I-V* measurements by taking into account the bias dependence of the effective barrier height (Φ_e) and R_s of the device, and the values of N_{ss} without considering R_s are almost one order of magnitude larger than N_{ss} when considering R_s value. © *2011 American Institute of Physics*. [doi:10.1063/1.3552599]

I. INTRODUCTION

Organic materials have received increased interest from the scientific community over the last two decades due to their unusual electrical and optical properties.[1–5] Among them, conducting polymers have attracted the most attention for possible application in molecular electronic devices because of their unique properties and versatility. Composite(s) of conducting polymer between the metal and the semiconductor can be used as an interfacial layer for fabrication of Schottky barrier diodes (SBDs). It is well known that an interfacial organic film or insulator layer forms a physical barrier between the metal and the semiconductor, preventing the metal from directly contacting the semiconductor surface. Therefore such an interfacial layer not only prevents inter-diffusion and reaction between them but also isolates/protects the metal from the semiconductor. These metal/insulator or polymer/semiconductor type SBDs and solar cells have been extensively studied in the past five decades.[6–19]

Normally polyvinyl alcohol (PVA) is a poor electrical conductor, and the conductivity of the polymer is of major importance in constructing a Schottky barrier. Its electrical conductivity depends on the thermally generated carriers and the addition of suitable dopant materials. When a polymer is doped with metals, especially transition elements such as Zn, Co, Ni, Cu, and Fe in various quantities and forms, their incorporation within a polymeric system may be expected to improve the conductivity.[20–22] In other words, diffusion of the dopant material into polymer matrix plays an important role in the conduction process. The doping process affects the chemical structure, crystallinity, and electrical conductivity of polymers.[13,18,19] A low doping of the polymer associated with a low number of charge carriers can lead to an extended depletion layer in the structure. On the other hand, high-charge carrier densities in the polymer may give rise to a thin barrier with a high probability of tunneling through the barrier. Therefore in the present study, the zinc acetate doped PVA (PVA:Zn) interfacial layer has been formed onto the front surface of n-Si substrate. This interfacial layer influences the interface states, which are established as the primary mechanism determining the energy level alignment at clean, abrupt, and defect free semiconductor interfaces,[23] and modifies some characteristics of the device. Moreover, the reduction of the leakage current is essential for developing polymer based SBDs. As a consequence, by using a nanometer sized organic interfacial layer, these devices may be optimized for low-leakage and reliable performance.[24,25]

The presence of an interfacial layer (organic or insulator) between the top contact and the semiconductor could lead to increase in barrier height (BH). This increase in BH

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was related to many parameters such as the formation of an interfacial layer and its thickness, the process of surface preparation under optimal conditions, the impurity concentration of a semiconductor, the interfacial layer induced dipole at the M/S interface, the good passivation of the semiconductor surface, the applied bias voltage, and the device temperature.[6,14,16,25] Also, PVA:Zn governs the surface electric field and the amount of band bending due to space charge in a thin interfacial layer, hence controlling the Schottky barrier height. In summary, Schottky barrier can be modified by organic thin film formed on semiconductor. Similar results have been published in literature.[26–29]

Analysis of the forward and reverse bias *I-V* characteristics of SBDs with and without interfacial layer measured at only room temperature and in the narrow applied bias voltage range does not give detailed information about the conduction process/mechanism and the nature of barrier formed at metal/semiconductor (M/S) interface. The temperature dependence of the forward bias *I-V* characteristics in the wide range of temperature and applied bias voltage gives a better picture of various conduction mechanisms and allows one to understand different aspects that shed light on the validity of various processes involved.[6,17,30] The series resistance (R_s) and interface states (N_{ss}) considerably affect the forward bias *I-V* characteristics. The effects of these parameters and temperature on *I-V* characteristics of SBDs are still intensively studied.[14–17,30–42] However, a complete description of the current conduction through a SBD is still a challenging problem. These types of studies show that there is a deviation from linearity of *I-V* characteristics in the semilogarithmic scale at high voltages due to the series resistance of device when the applied voltage is sufficiently large.[43,44] Some authors purposed the effects of the presence of an interfacial layer and N_{ss} on the behavior of SBDs, discussed the occupation of interface states as a function of applied voltage, and extracted the density distribution of the N_{ss} in the semiconductor bandgap from the nonideal *I-V* characteristics. Generally, the *I-V* characteristics of SBDs deviate from the ideal/pure thermionic emission (TE) theory (n=1). It has been observed that zero-bias barrier height (Φ_{Bo}) increases with increasing temperature. Such behavior of Φ_{Bo} has been successfully explained on the basis TE theory with Gaussian distribution of the barrier height (BH).[6,32–39]

There are many theoretical and experimental studies reporting a possibility of the intersection/crossing in the *I-V* plots of SBDs measured at different temperatures as well as the effect of the R_s on this intersection.[31–37] Osvald[37] has presented a theoretical analysis of Schottky diodes with nanosize dimensions. The author has discussed the intersection behavior of *I-V* plots and supported idea that the R_s presence is a necessary condition of this observation. This effect is rather unexpected and seems to be in contradiction with the thermionic concept of the current transport.[17,32] On the other hand, according to Chand,[34] the intersection may occur because of decreasing apparent barrier height with decreasing temperature, and the presence of R_s keeps this intersection hidden and unobservable in homogeneous Schottky diodes. Dökme and Altındal[31] and, Pakma *et al.*[32] have also written a paper concerned with the effect of series resistance on the intersection behavior of *I-V* plots of SBDs with SiO_2 and TiO_2 interfacial insulator layers, respectively. Similar results have also been reported by Ravinandan *et al.*[45] and Huang *et al.*[46] for the metal/GaN SBDs in literature.

In this study, the values of zero-bias barrier height were obtained from both forward and reverse bias *I-V* data to understand the different aspects of conduction mechanisms in the temperature range of 80-400 K. The origin of anomalous behavior of the barrier height and the intersection behavior in the forward bias *I-V* plots of the Au/PVA:Zn/n-Si have been investigated. In addition, the temperature dependent energy distribution profile of N_{ss} was obtained from the forward bias *I-V* characteristics by taking into account the bias dependence of the effective barrier height (Φ_e), ideality factor (n) and R_s.

II. EXPERIMENTAL DETAILS

The Au/PVA:Zn/n-Si SBDs were fabricated on an n-type (phosphor doped) float zone (100) single crystal Si wafer. First, the wafer was cleaned with RCA cleaning procedure. High purity Au metal (5N) with a thickness of ~1500 Å was thermally evaporated onto the whole back side of Si wafer in a pressure about 10^{-6} Torr in high vacuum thermal evaporation system. To perform good ohmic behavior, Si wafer was annealed at 450 °C in pressure of 10^{-6} Torr.

The uniform PVA:Zn film was successfully deposited on n-type Si substrate by using electrospinning system. Zinc acetate (0.1 g) was mixed with 0.9 g polyvinyl alcohol (PVA), molecular weight = 72 000, and 9 ml de-ionized water. After vigorous stirring for 2 h at 50°C, a viscous solution of PVA:Zn acetates was obtained. Using a peristaltic syringe pump, the precursor solution was delivered to a metal needle syringe (10 ml) with an inner diameter of 0.9 mm at a constant flow rate of 0.02 ml/h. The needle was connected to a high voltage power supply and positioned vertically on a clamp. A piece of flat aluminum foil was placed 15 cm below the tip of the needle to collect the nanofibers. An Si wafer was placed on the aluminum foil. Upon applying a high voltage of 20 kV on the needle, a fluid jet was ejected from the tip. The solvent evaporated, and a charged fiber was deposited onto the Si wafer as a nonwoven mat. After spinning process, circular dots of 1 mm diameter and 1500 Å thick high purity (%99.999) Au rectifying contacts were formed on the PVA:Zn surface of the wafer through a metal shadow mask in high vacuum system with pressure of about 10^{-6} Torr. In this way, Au/PVA:Zn/n-Si SBDs were fabricated for the electrical measurements, and the electrode connections were made by silver paste.

Current-voltage (*I-V*) measurements were performed by means of a Keithley 2400 source meter in the wide temperature range of 80-400 K using a temperature controlled Janis VPF-475 cryostat with vacuum of $\sim 10^{-3}$ Torr. The sample temperature was always monitored by using a copper-constantan thermocouple close to the sample and measured with a Keithley 2400 sourcemeter with the help of Lake Shore model 321 auto-tunning temperature controllers with sensitivity better than ±0.1 K. All measurements were carried out

with the help of a microcomputer through an IEEE-488 ac/dc converter card.

III. RESULTS AND DISCUSSION

When the SBD with a series resistance and an interfacial layer, the *I-V* relation based on thermionic emission (TE) theory (V≥3 kT/q) is given by,[41–45]

$$I = I_o \exp\left(\frac{qV - IR_s}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right], \quad (1)$$

where V, n, q, IR_S, and T are the applied bias voltage, the ideality factor, the electronic charge, the voltage drop across series resistance of SBD, and the temperature in Kelvin, respectively. I_o is the reverse saturation current extracted from the straight line intercept of ln*I-V* plot at zero bias and is given by,

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{B0}}{kT}\right), \quad (2)$$

where A, A^*, Φ_{Bo} are the rectifier contact area, the effective Richardson constant (120 A/cm^{2}K^2 for n-type Si), and the zero bias or apparent barrier height, respectively.

The semilogarithmic forward and reverse bias *I-V* curves of the Au/PVA:Zn/n-Si SBD in the temperature range of 80-400 K are shown in Fig. 1. The forward bias *I-V* characteristics are linear at low forward bias voltages but deviate considerably from linearity due to R_s and the interfacial layer (PVA:Zn) effect. As a consequence of series resistance, when the current carriers are thermally generated, it is assumed that for higher temperatures, the larger current will flow through the diode. It is clearly seen from Fig. 1 that the curves intersect at an almost common point, implying that at this point, the slope of ln*I-V* curves is independent of temperature. As shown in Fig. 1, the increase of n-Si resistivity causes an increase of R_s, which leads to downward *I-V* curves at voltages larger than 1 V. Contrary to the forward-biased current, the reverse-biased current increases with increasing temperature in accordance with literature. A number of researchers have obtained similar results in their theoretical and experimental studies in the literature.[31–37,45] Among them, Chand[34] argues that the intersection may occur at almost the same point, but the ln*I-V* curves are bent due to current saturation effect of series resistance in each elementary barrier, so it is hidden and not observable. According to Osvald,[37] if we want to observe the intersection of *I-V* curves, we have to lower the diode dimensions practically to a nanometer scale. For larger dimensions, the intersection is shifted to a higher voltage region, where *I-V* curves are not commonly measured. Moreover, Horvath *et al.*[47] reported that by experimenting they found an intersection point in the forward bias *I-V* characteristics of the Al/SiO_2/Si structure with SiC nanocrystals. This intersection of *I-V* curves seems to be an abnormality when compared to the conventional behavior of SBDs. We think that, for our sample (SBD), this downward and intersecting behavior in the forward bias *I-V* curves originates from the magnitude of R_s.

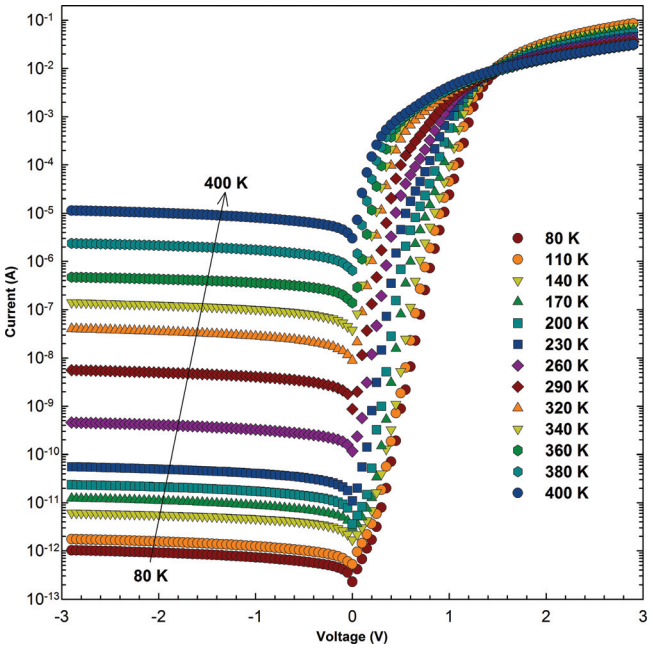

FIG. 1. (Color online) The semilogarithmic forward and reverse bias *I-V* curves of the Au/PVA:Zn/n-Si SBD in the temperature range of 80-400 K.

To compare the forward bias *I-V* characteristics with reverse bias ones, a semilogarithmic plot of $I/[1-\exp(-qV/kT)]$ vs V according to Eq. (1) was drawn in the bias range of (−1)-0 V using the reverse bias data at each temperature and given in Fig. 2. As can be seen in Fig. 2, the semilogarithmic plot of $I/[1-\exp(-qV/kT)]$ vs V has a good linear behavior, and the values of I_o were obtained from the y-axis intercept at zero voltage for each temperature. The values of I_o range from 4.14×10^{-13} A (at 80 K) to 4.60×10^{-6} A (at 400 K). Using these I_o values in Eq. (2), the values of barrier height (BH) calculated from the forward and reverse bias, Φ_{BFo} and Φ_{BRo}, were given in Table I and Fig. 3 for each temperature. The experimental values of the BH in the reverse bias

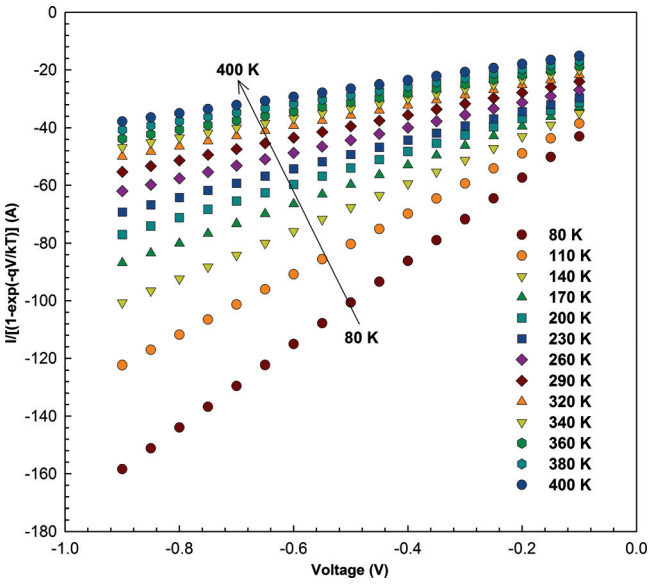

FIG. 2. (Color online) The semilogarithmic plot of $I/[1-\exp(-qV/kT)]$ vs V for the Au/PVA:Zn/n-Si SBD in the temperature range of 80-400 K.

TABLE I. Temperature dependent various electrical parameters determined from the forward and reverse bias *I-V* characteristics of the Au/PVA:Zn/n-Si SBD.

T (K)	Φ_{Bfo} (eV)	Φ_{Bro} (eV)	R_s (at 1 V) (Ω)	R_s (at 5 V) (Ω)	R_{sh} (at −1 V) (Ω)	R_{sh} (at −5 V) (Ω)
80	0.328	0.257	41539.34	20.08	1.36E+12	4.65E+12
110	0.427	0.354	22106.68	21.62	8.03E+11	2.74E+12
140	0.536	0.44	10358.61	25.15	2.14E+11	7.40E+11
170	0.628	0.531	3909.9	29.95	1.14E+11	3.88E+11
200	0.699	0.62	1713.75	35.65	5.76E+10	2.04E+11
230	0.745	0.702	938.48	42.12	2.46E+10	7.35E+10
260	0.788	0.751	607.83	45.85	3.07E+09	1.05E+10
290	0.813	0.781	448.38	52.5	2.46E+08	7.35E+08
320	0.837	0.815	334.22	56.53	3.51E+07	1.00E+08
340	0.853	0.831	280.52	57.76	9.85E+06	2.94E+07
360	0.867	0.842	268.75	58.32	2.78E+06	9.63E+06
380	0.876	0.851	265.03	56.55	5.76E+05	2.04E+06
400	0.878	0.853	236.73	53.61	1.23E+05	4.19E+05

characteristics range from 0.257 eV (at 80 K) to 0.835 eV (at 400 K). It is observed that Φ_{BFo} and Φ_{Bro} increase with increasing temperature up to 230 K and then go to saturation. The change in BH with temperature shows the unusual behavior indicating deviation from the TE theory and arises perhaps due to current resulting by other conduction processes such as thermionic field emission (TFE), field emission (FE), multi-step tunneling via interface states, or dislocations. However, the FE is an unlikely conduction mechanism because it would predominate at quiet low temperatures for the semiconductor material having doping concentrations, which is not the case for the Si substrate in the present work. On the other hand, the TFE mechanism may be dominated for the current transport mechanism at an intermediate temperature. Assuming that a diode consists of SBH inhomogeneity, the current conduction will be dominated by patches of lower BH at lower temperatures. However, as the temperature increases, the patches with higher BHs take effect due to the fact that electrons gain sufficient energy to surmount them. Moreover, such temperature dependence of Φ_{Bo} is in obvious disagreement with the reported negative coefficient of the barrier height or the forbidden bandgap of a semiconductor Si.

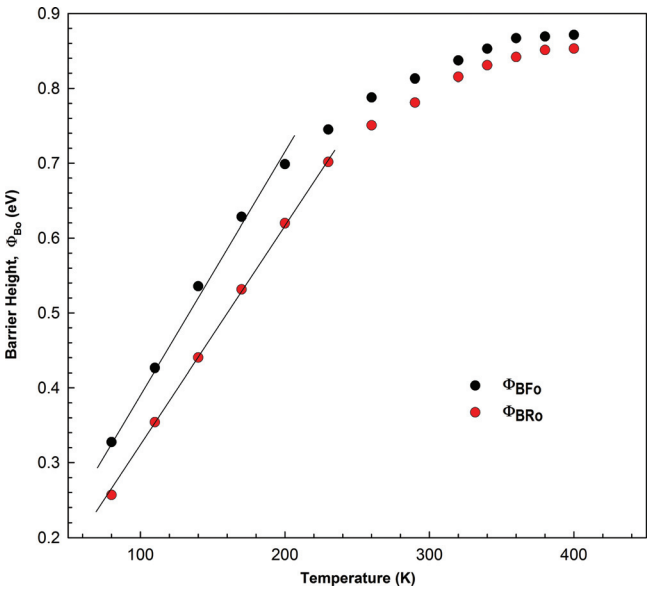

FIG. 3. (Color online) The Φ_{Bo} vs *T* plot for Au/PVA:Zn/n-Si SBD.

It is also necessary to discuss how the BH varies with applied voltage in the forward and reverse bias condition. As can be seen in Table I and Fig. 3, there is a consistent disagreement between the values of BHs determined from the forward and reverse bias *I-V* data, and the value of Φ_{BFo} is greater than Φ_{Bro} value for each temperature. This discrepancy is more prominent at low temperatures. Similar results have been reported in the literature by Padovani and Stratton,[48] Ravinandan *et al.*,[45] and Çınar *et al.*[49] They proposed that the quantum mechanical tunneling (TFE and FE) in forward biased metal/semiconductor (MS) contacts or SBD considers the current from the semiconductor to metal ($I_{s\text{-}m}$) due to tunneling of the charge carriers from the semiconductor into the metal. Because this current is negligible in reverse bias, the resulting tunneling current from the metal into the semiconductor ($I_{m\text{-}s}$) will be important in reverse-biased MS contacts or SBD.[43,45,48,49] Tung[50] also proposed a new model based on the pinch-off phenomenon, which is used to explain the voltage dependence of BH. According to this model, the pinch-off is stronger under forward bias than under reverse bias, and under high reverse bias, the pinch-off may be relaxed. Thus it can be concluded from this effect that the effective barrier height should be higher under forward bias than under reverse bias. Normally a rectifying device has a low reverse current and high forward conductivity, which needs a low-barrier electrode under forward bias and a high-barrier electrode under reverse bias. However, the pinch-off model stated that an inhomogeneous Schottky contact may behave like a high-barrier contact under forward bias, a low-barrier contact under reverse bias.[51] Ejderha *et al.*[52] also discussed the voltage dependence of BH and reported that due to the potential drop across the interfacial layer, the zero bias BH is lower than expected in an ideal diode in the reverse bias conditions, and the potential across the interfacial layer with bias because of electric field present in the semiconductor and the change in the interface state

charges as a result of applied voltage, and thus modifies the BH. Hence the additional barrier decreasing in the reverse bias stems from the potential change across the interfacial layer rather than image force lowering. We think that this discrepancy stems from the fact that the apparent BH seen from metal to semiconductor is higher than the one seen from semiconductor to metal.

For the evaluation of the voltage dependent barrier height in the forward bias region, one may also make use of the Richardson plot of the saturation current at any bias voltage and Eq. (2) can be rewritten as,

$$\ln\left(\frac{I(V)}{T^2}\right) = \ln(AA*) - \frac{q\Phi_B(V)}{kT}. \tag{3}$$

From the slope of Richardson plot, the barrier height corresponding to activation energy $[E_a(V)]$ can be determined for each forward bias voltage.[51,53] To investigate the bias dependent barrier height, we have drawn the $\ln(I/T^2)$ vs q/kT plots of Au/PVA:Zn/n-Si SBD in the forward bias region for various voltages and shown in Fig. 4(a). As shown in Fig. 4(a), the forward bias $\ln(I/T^2)$ vs q/kT curves appear to exhibit a thermally activated behavior over the whole temperature range. The $\ln(I/T^2)$ vs q/kT plots give straight lines at each voltage and, by using the slope of the best linear region of these plots; the experimental values of activation energy (E_a) were obtained and given in Fig. 4(b). The values of E_a vary from 0.413 eV (for 0.25 V) to 0.185 eV (for 0.60 V). Here we can conclude that at any given temperature, the E_a values decrease with increasing applied bias voltage. As shown in Fig. 4(b), the values of E_a are lower than the half of forbidden gap of Si ($E_g/2$) in the intermediate bias voltage region. The experimental results show that the change in E_a and Φ_{Bo} cannot be explained by the classical drift diffusion or by generation-recombination mechanisms. Similar results have been reported in the literature.[33,54,55]

The series resistance (R_s) and shunt resistance (R_{sh}) values of device are obtained from the structure resistance (R_i) versus applied bias voltage (V_i) plot determined from both the reverse and forward bias I-V characteristics by using Ohm's law as following relation;

$$R_i = dV_i/dI_i. \tag{4}$$

It is observed that the value of R_{sh} corresponds to the maximum value of resistance in the reverse bias region, whereas R_s corresponds to the minimum value of resistance in forward bias region. To see the change in R_s and R_{sh} with temperature, we have drawn the R_s and R_{sh} vs temperature at two different applied bias voltages. Figure 5(a) shows the variation of R_s as a function of temperature before intersection (at 1 V) and after intersection (at 5 V). It is an interesting feature that R_s decreases with increasing temperature before the intersection point and increases with increasing temperature after the intersection point. For the voltages higher than the voltage of the intersection point, the current flowing through the diode is higher at a lower temperature. This effect is rather unexpected in its nature and at first look is in contradiction with the thermionic concept of the current

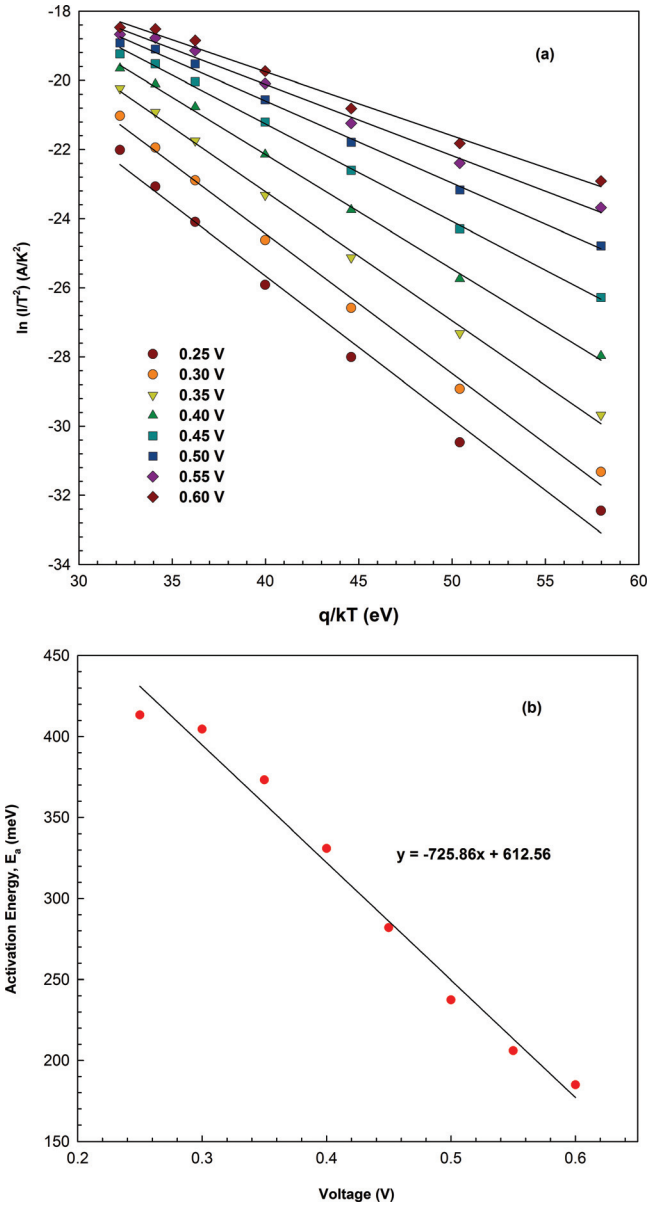

FIG. 4. (Color online) (a) ln (I/T^2) vs q/kT and (b) E_a vs V plots of Au/PVA:Zn/n-Si SBD.

transport. Generally, such temperature dependence of R_s is in obvious disagreement with the reported negative temperature coefficients. Such behavior of R_s may be attributed to a lack of free charge at a lower temperature and in the temperature region where there is no carrier freezing out, which is non-negligible at a low temperature.[31,32,37,45] Such a similar phenomenon was observed and reported in literature.[31–37,45] Figure 5(b) shows the variation of R_{sh} values as a function of temperature at -1 and -5 V, respectively. As shown in Fig. 5(b), contrary to R_s, the value of shunt resistance (R_{sh}) corresponding to negative voltage region decreases with increasing temperature for two different bias voltages. Here the high values of R_{sh} correspond to the low temperature region, and it has a maximum value at 80 K due to the lowest leakage current seen at 80 K.

It should be indicated that the effect of series resistance R_s is usually modeled with a series combination of a diode

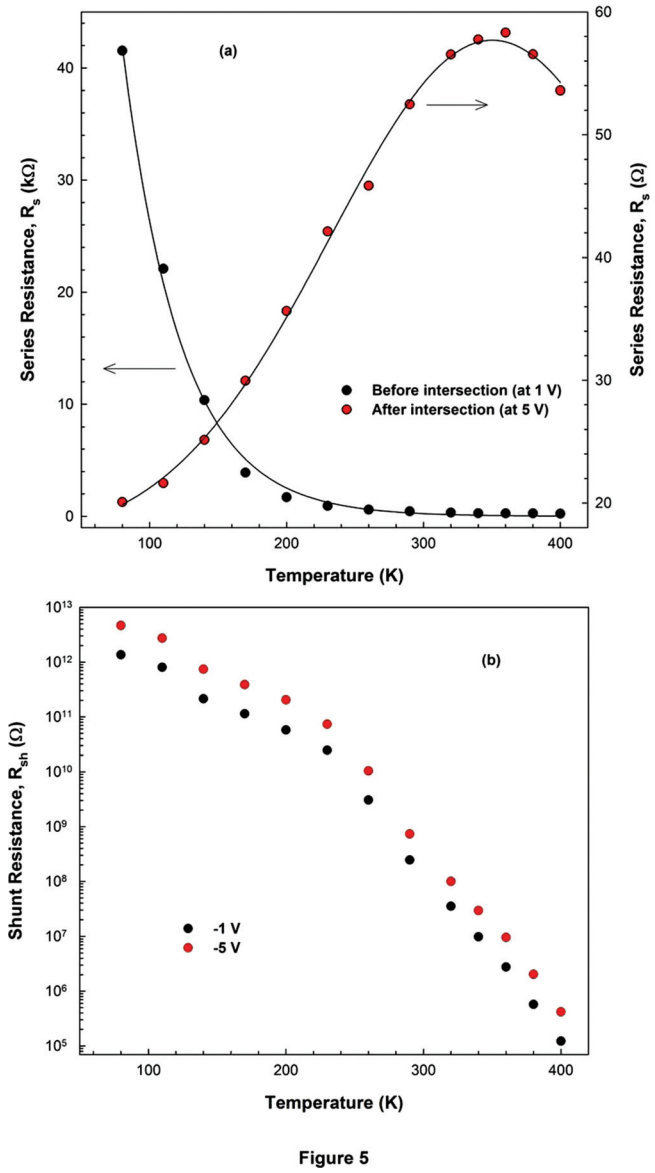

Figure 5

FIG. 5. (Color online) (a) The R_s vs T plot and (b) The R_{sh} vs T plot of Au/PVA:Zn/n-Si SBD.

and a resistor with resistance R_s through which the current I flows. When a forward bias V is applied across the diode, it will be shared by interfacial layer (V_i), the depletion layer (V_s), and series resistance combination of the diode R_s, and thus V can be given as

$$V = V_s + V_i + IR_s. \tag{5}$$

The effective barrier height (Φ_e) is assumed to be applied bias-dependent due to the presence of an interfacial insulator layer and N_{ss} located at PVA:Zn/Si interface. The bias dependence of Φ_e can be expressed as[41,44]

$$\frac{d\phi_e}{dV} = \alpha = 1 - \frac{1}{n(V)}, \tag{6}$$

where α is the voltage coefficient of the Φ_e. In the preceding formulation, in the event that the interface states are in equilibrium with semiconductor, the applied bias voltage dependence of the BH, $d\Phi_e/dV$, is a parameter that combines the effects of the both interface states and interfacial layer thickness. The Φ_e is given by[15,41,44,56,57]

$$\Phi_e = \Phi_{bo} + \alpha(V - IR_s) = \Phi_{bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s). \tag{7}$$

For MIS type SBD with N_{ss}, which is in equilibrium with the semiconductor, the ideality factor n becomes greater than unity and the voltage dependence of n can be expressed as

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right]. \tag{8a}$$

The expression for N_{ss} deduced by Card and Rhoderick[41] is reduced as follows[41,44,57]

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right]. \tag{8b}$$

Here, $\varepsilon_I(=8\varepsilon_o)$ and $\varepsilon_s(=11.8\varepsilon_o)$ are the permittivities of the interfacial layer and the semiconductor, respectively, ε_o is the permittivity of free space ($\varepsilon_o = 8.5 \times 10^{-14}$ F/cm). δ is the thickness of the interfacial layer, and W_D is the width of space charge region. In addition, in n-type semiconductors, the energy of interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given by[57]

$$E_c - E_{ss} = q[\Phi_e - (V - IR_s)]. \tag{9}$$

Figure 6 shows the energy distribution profiles of N_{ss} as a function of E_c-E_{ss} extracted from the forward bias I-V characteristics by taking into account the bias dependence effective barrier height (Φ_e), ideality factor $n(V)$, and series resistance of the device. It is clearly seen from Fig. 6 that N_{ss} has an exponential growth from midgap of Si toward to

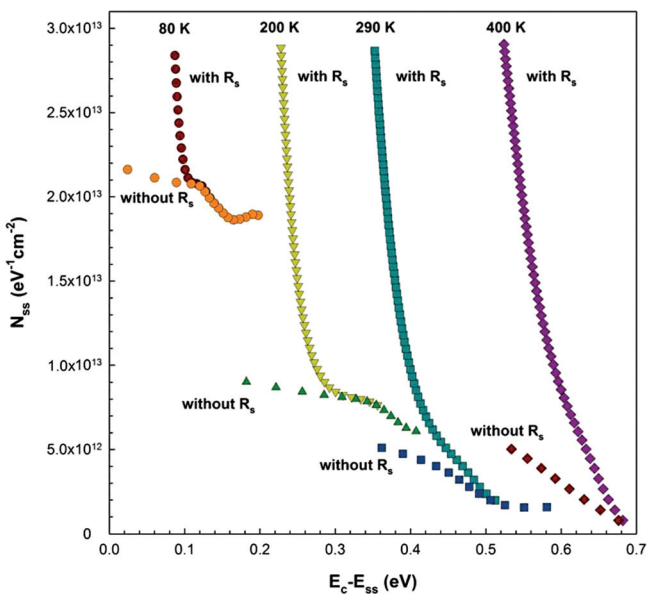

FIG. 6. (Color online) The energy distribution profiles of N_{ss} as a function of E_c-E_{ss} extracted from the forward bias I-V data of Au/PVA:Zn/n-Si SBD at various temperatures.

bottom of conduction band and increase with decreasing temperature. Such behavior of N_{ss} can be attributed to molecular restructuring and reordering of the M/S interface with the effect of temperature. Another important point that should be considered is the R_s effect on N_{ss}, which depends on the thickness of interfacial layer inserted in M/S interface. As seen in Fig. 6, the energy values of the density distribution of N_{ss} are in the range E_c-0.06 eV to E_c-0.23 eV at 80 K and E_c-0.53 eV to E_c-0,68 eV at 400 K. The magnitude of N_{ss} with and without R_s in E_c-0.06 eV is 2.84×10^{13} and 2.16×10^{13} at 80 K, respectively. Also the magnitude of N_{ss} with and without R_s in E_c-0.53 eV is 2.90×10^{13} and 5.02×10^{12} at 400 K, respectively. The values of N_{ss} obtained by taking into account the R_s are about one order lower than those obtained without considering the R_s near the conduction band. Therefore the effect of R_s must be taken into account in calculations of main electrical parameters such as n, Φ_B, and N_{ss}.

IV. CONCLUSION

In the present paper, the forward and reverse bias *I-V* characteristics of Au/n-Si SBDs modified with uniform PVA:Zn interfacial layer have been studied over a wide temperature range (80-400 K). The PVA organic film seems to cause a significant modification of interface states, although the organic-inorganic interface seems abrupt and unreactive. Experimental results show that the forward bias *I-V* plots intersect at an almost common point, implying that at this point, the slope of ln*I-V* curves is independent of temperature. The downward and intersecting behavior in the forward bias *I-V* curves originates from the magnitude of R_s. This crossing behavior of *I-V* curves appears as an abnormality when compared to the conventional behavior of SBD. This crossing can be observed in the forward bias *I-V* plot even if series resistance is finite (nonzero). The R_s value of the device increases with increasing temperature after the intersection point. For the voltages higher than the voltage of the intersection point, the current flowing through the diode is higher at lower temperature. Such temperature dependence of R_s is in obvious disagreement with the reported negative temperature coefficients. Also the zero bias barrier heights, Φ_{BFo} and Φ_{BRo}, evaluated from the forward and reverse bias *I-V* data, reveal a discrepancy. The underlying reason of this discrepancy was explained based on Tung's pinch-off model. The pinch-off strongly influences the current transport across inhomogenous SBDs, and low barrier regions will be pinched-off under forward bias rather than under reverse bias. The voltage dependent value of E_a obtained from the slopes of $\ln(I/T^2)$ vs q/kT curves decreases with increasing applied bias voltage under the forward bias condition. Such behavior of E_a may be attributed mainly to interfacial layer effects with a small contribution because of image force lowering. The N_{ss} values obtained taking into account the R_s value are lower than those obtained without considering the R_s near the conduction band Si for each temperature. As a result, it can be said that the R_s, N_{ss}, and applied bias voltage effects should be taken into account in calculations for an accurate determination of main barrier parameters obtained from the forward bias *I-V* data.

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