IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. **37** (2022) 095017 (7pp) https://doi.org/10.1088/1361-6641/ac84fc

Characterization of traps in GaN-based HEMTs by drain voltage transient and capacitance deep-level transient spectroscopy

Shijie Pan[1], Shiwei Feng[1,*], Xuan Li[1], Kun Bai[1], Xiaozhuang Lu[1], Yamin Zhang[1], Lixing Zhou[1], Erming Rui[2], Qiang Jiao[2] and Yu Tian[2]

[1] Institute of Semiconductor Device Reliability Physics, Beijing University of Technology, Beijing 100124, People's Republic of China
[2] China Astronautics Standards Institute, Beijing 100071, People's Republic of China

E-mail: shwfeng@bjut.edu.cn

Received 10 May 2022, revised 20 July 2022
Accepted for publication 28 July 2022
Published 8 August 2022

Abstract

This paper presents a detailed investigation of trapping effect in AlGaN/GaN high-electron-mobility transistors based on the pulsed current–voltage characterization, drain voltage transient (DVT) measurement, and capacitance deep-level transient spectroscopy (C-DLTS). By monitoring the DVTs at various filling voltages and temperatures, the properties of three electron traps were obtained with the DVT measurements. Specifically, the energy levels of the former two traps were determined to be 0.28 and 0.48 eV, which was confirmed by the C-DLTS measurement performed on the same device. In addition, a third temperature-independent trap located in the GaN buffer was observed only with the DVT measurement, indicating the advantage of transient curves measurement in characterizing the traps insensitive to temperature. The combined measurements demonstrate the correlation of different techniques, which allows identifying the same trap levels to investigate the physical origin of traps.

Keywords: capacitance deep-level transient spectroscopy (C-DLTS), drain voltage transients (DVTs), gallium nitride (GaN), high-electron-mobility transistors (HEMTs), trap

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN-based high-electron-mobility transistors (HEMTs) have demonstrated excellent performance in high power [1], high voltage [2], and high frequency applications [3] owing to the superior characteristics [4–7]. However, the traps existing in the barrier or buffer layer of the HEMTs significantly restrict the performance and long-term reliability of the device [8, 9], and the physical properties of these traps still require further investigation [10].

There are various methods to explore the trapping behaviors in GaN HEMTs, such as deep-level transient spectroscopy (DLTS) [11, 12], gate-lag measurement [13], pulsed current–voltage characterization [14], and current-transient method [10]. In particular, the current transients have been widely applied to obtain the properties of traps through the construction of time constant spectrum (TCS), such as the multiexponential fitting [10], the derivative of current transients [9], and the Bayesian deconvolution [15]. The identified trap levels can

* Author to whom any correspondence should be addressed.

be related to the results obtained with the DLTS measurement, which was one of the most classical techniques employed to investigate the deep levels [9, 10]. For example, Joh *et al* have identified a trap with an energy level of 0.57 eV using the current-transient method through the multiexponential fitting [10], which was directly related to the traps at similar energy levels observed with DLTS in previous reports [16, 17]. Besides, Wang *et al* have identified a shallow trap with an energy level of 66 meV with the derivative of drain current transients [18], which was confirmed with the DLTS carried out on the metal-insulator-semiconductor (MIS)-diode.

Although the former two methods used to extract the time constant of traps have been compared and verified with the DLTS method, the feasibility of the Bayesian deconvolution method proposed in our previous studies requires further confirmation [15]. In addition, for the current-transient method, the voltage drift during the transient current measurement may severely affect the measurement accuracy [19]. Based on the current-transient method, we developed the drain voltage transient (DVT) measurement to effectively solve this problem [20]. Furthermore, we combined the DVT method and the Bayesian deconvolution method to establish a complete trapping measurement and analysis system, which can be used to extract the time constants of traps based on the voltage transient curves [19]; nevertheless, the comparison of experimental data obtained within this DVT measurement with other technique have not been studied in such systems.

In this work, we investigated the trapping effect of HEMTs with the combination of the pulsed *I*–*V* characterization, DVT measurement, and capacitance deep-level transient spectroscopy (C-DLTS) performed on the same device. The trapping behaviors obtained with different methods were discussed, and the trap levels identified with DVT and C-DLTS measurements were also compared. A good agreement was observed for the energy levels of two electron traps obtained by both two techniques, and a temperature-independent trap was determined only with the DVT measurement. The above results were compared with the data presented in previous reports to investigate the physical origin of traps.

2. Experimental details

The device used in this study consisted of a 25 nm AlGaN layer, 1.47 μm GaN layer, and 150 μm SiC substrate. The source-gate distance, gate length, and gate-drain distance were 2 μm, 0.45 μm, and 4 μm, respectively [20]. The device was composed of ten fingers with a total gate width of 350 μm. In this study, the trapping effect of GaN HEMTs was studied with three kinds of techniques. The pulsed current–voltage characterization was performed using a Keysight B1500A semiconductor parameter analyzer. The drain-source transient voltages were measured using the DVT measurements [21] and the differential amplitude spectrum (DAS) [19, 22] to analyze the properties of traps. In addition, the C-DLTS measurement was performed on the same device using a PhysTech GmbH FT1030 DLTS system to confirm the obtained trap levels.

3. Results and discussions

3.1. Pulsed characterizations

Firstly, the device was submitted to a pulsed current–voltage measurement to quickly analyze the presence of charge trapping from the changes in drain-source current (I_{DS}), threshold voltage (V_{TH}), and transconductance peak (g_m) [9, 14, 23]. The period of the driving waveform was 50 ms, and the data points were collected with short pulses of 500 μs [22]. Figures 1(a) and (b) presented the results of pulsed g_m variation and I_D–V_D under different bias points, respectively. Specifically, figure 1(a) presented a remarkable V_{TH} positive shift and $g_{m,peak}$ reduction, suggesting that the current collapse can be probably related to the negative charge trapping under the gate and in the access region [24–26]. In addition, the current collapse was presented in the pulsed I_D–V_D curves in figure 1(b), suggesting that most of the collapse appeared at the current saturation region with a minimum change in the linear part. It can be observed that the degradation of I_{DS} under the quiescent bias of (V_{GQ}; V_{DQ}) = (−5 V; 15 V) was approximately 13.8%. It indicated that the traps under the gate may dominate the current collapse and the charging at the surface of access regions may be relatively small [27]. The pulsed characterization can be effective for a preliminary analysis of trapping effect, whereas it may not provide detailed information on the dynamic trapping behavior of traps, and the trap levels responsible for the current collapse should be identified with other techniques [9, 19].

3.2. DVT measurements

To achieve complementary information about the trapping effect, the DVT measurements were performed on the device starting from different bias voltages (V_{GF}; V_{DF}) [22]. According to the biasing sequence in figure 2(a), a 30 s long filling process with various gate and drain voltages were applied on the device, and then the detrapping process was detected by monitoring the DVTs at conditions of (V_{GM}; I_{DM}) = (0 V; 200 mA) [21], as shown in figure 2(b). It indicated that the drain-source voltage (V_{DS}) was approximately 0.5 V under the above measurement conditions, and thus the power in the experiments was 0.1 W. The thermal resistance of the device was 7.3 °C W^{-1} with the structure function method [28], and thus the effect of the highest temperature rise of 0.73 °C can be negligible [19, 29]. It can be noticed that the voltage transients in figure 2(b) gradually decreased to a steady state as time increased and can be explained as follows. In the off-state operation, the electrons from the gate can be trapped in the AlGaN barrier or GaN buffer due to the electric field distributed in the depletion region [7, 30–32]. When the gate voltage switched to 0 V, the captured electrons get detrapped and enable the recovery of the two-dimensional electron gas (2DEG) density [9, 10], and thus the transient drain voltage gradually decreased under a constant drain current in figure 2(b) [21]. It was also observed that the variation of voltage transient increased with larger filling stress,

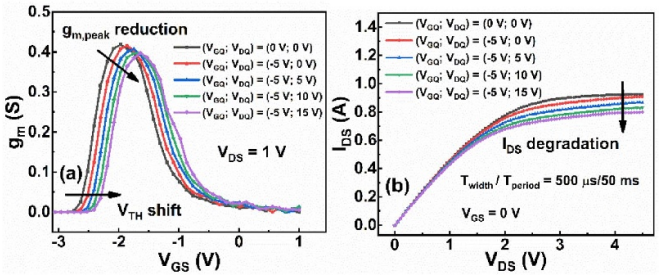

Figure 1. (a) g_m (extracted from I_D–V_G) pulsed characterizations and (b) I_D–V_D for different quiescent bias points: the dynamic current collapse appears at the current saturation region.

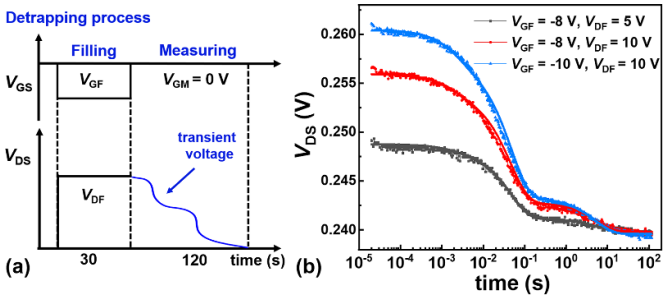

Figure 2. (a) Biasing sequence of detrapping process performed with the DVT measurements. (b) Recorded (dots) and reconstructed (lines) detrapping transients under different filling conditions.

which represented a stronger trapping process under higher bias voltages [2].

To further demonstrate the effect of filling conditions, the TCS [15] and DAS [22] were employed to analyze the time constant and absolute amplitude of traps, respectively. As the detrapping transients may involve several independent detrapping process and can be regarded as a sum of exponentials [10, 19], the measured voltage transient curve V_{ds} (t) can be fitted as [15, 22]

$$V_{ds}(t) = \sum \Delta V_i \exp\left(-\frac{t}{\tau_i}\right) + V_\infty \qquad (1)$$

where ΔV_i is the amplitude, τ_i is the time constant of trap, and V_∞ is the drain voltage at a steady state. Therefore, the time constant of traps can be obtained based on the Bayesian deconvolution, which was also used in the current-transient method [15].

Figure 3(a) presented the TCS of three electron traps identified from the voltage transient curves in figure 2(b). It revealed that the time constants of three traps were almost constant under different filling voltages, suggesting that the traps should be individual trap levels due to the unchanged charge trapping rate [8, 33]. In addition, the absolute amplitudes of three traps identified with the DAS were shown in figure 3(b), which reflected the contribution of each trap to the transient variation exactly [22]. It can be noticed that the transient curves reconstructed with the identified time constants and amplitudes of three traps agreed well with the recorded data in figure 2(b), indicating that the extracted TCS and DAS can be accurate [22].

Figure 3(c) revealed the absolute amplitudes of three traps under different filling voltages, which was directly extracted with the method in figure 3(b) inset. As the dependence of amplitude on the filling bias voltage has been studied in previous report [19], the absolute amplitudes under three bias voltages in this study were used to analyze the location of traps preliminarily. The results in figure 3(c) suggested that the amplitudes of DP1 and DP2 presented a remarkable increase as the gate and drain voltages both increased, whereas the amplitude of DP3 only increased obviously with the drain voltage. It has been reported that the traps in the AlGaN layer may be affected by both the gate and drain voltages due to the high electric field in the gate-drain region [31, 34], whereas the traps primarily affected by the lateral electric field may be located in the GaN buffer [8]. Nevertheless, the above discussions may not be sufficient for the analysis of the properties of traps, and the detailed information, such as the energy levels and cross sections of traps, still required further investigation.

In order to obtain the energy levels of the traps, the DVTs were monitored at various temperatures shown in figure 4(a) and the corresponding TCS were presented in figure 4(b). As the time constants of the former two traps were reduced with increasing temperature, the energy levels and capture cross sections can be derived from the Arrhenius plot [15]. As shown in figure 4(c), the energy levels of DP1 and DP2 were 0.28 eV and 0.48 eV, and the cross sections were 0.46×10^{-18} cm^2 and 0.50×10^{-16} cm^2, respectively. In addition, the time constant of the third trap DP3 was almost unchanged with increasing temperature in figure 4(b). The above results can be compared with the traps reported in previous studies to understand the physical origin and possible location of traps. Besides, the energy level and cross sections of the traps can be confirmed with the experimental results obtained with other technique in the subsequent section.

3.3. C-DLTS

To confirm the trap levels obtained with the DVT measurements, the C-DLTS was also performed on the same device using a PhysTech GmbH FT1030 DLTS system. The C-DLTS has been widely applied to investigate the traps in GaN HEMTs and the details have been presented in previous reports [12, 35]. Figure 5(a) presented the transient capacitance signal measured from 45 K to 450 K with pulse width (t_p) of 0.1 ms [36]. In our study, the C-DLTS was conducted being pulsed from lower reverse bias to higher reverse pulse bias [37], with the reverse and pulse gate bias of −0.5 V and −3 V, respectively. The similar voltages have been used in the current deep-level transient spectroscopy [34] and C-DLTS measurement in GaN HEMTs [37–40]. It has been reported that the application of a more negative bias pulse should increase the negative charges captured by the traps, and the traps can emit the electrons after removing this negative bias pulse [39, 40]. The applied voltages were in accordance with the voltage conditions during transient curve measurement [41],

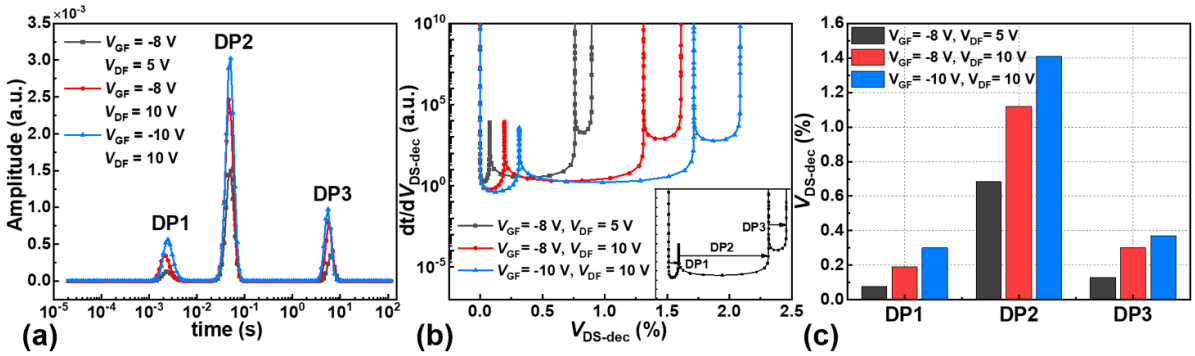

Figure 3. (a) Time constant spectra (TCS) under different filling conditions. Three detrapping behaviors contributed to the voltage transient were designated as DP1, DP2, and DP3, respectively. (b) The corresponding differential amplitude spectra (DAS). (Inset) The extraction method of absolute amplitude of each detrapping behavior. (c) Comparison of the three traps' amplitudes read from the DAS.

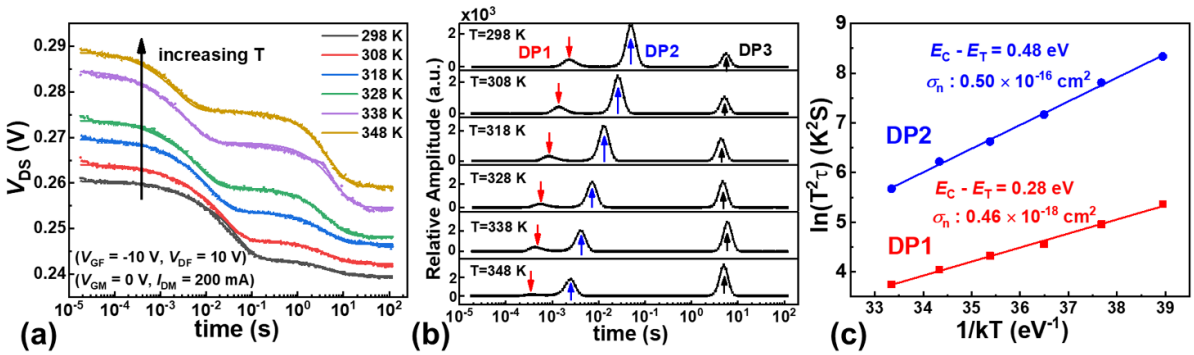

Figure 4. (a) Detrapping transients at various temperatures with (V_{GF}; V_{DF}) = (−10 V; 10 V). (b) TCS at various temperatures. Note that the temperature dependence of DP1 and DP2 could be used to extract the Arrhenius plots, and the time constant of DP3 was insensitive to temperature. (c) The corresponding Arrhenius plots of DP1 and DP2 with energy levels of 0.28 and 0.48 eV, respectively.

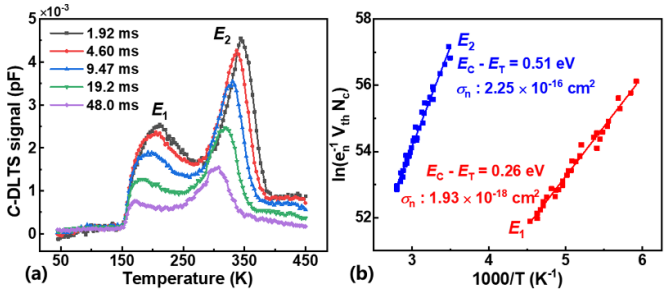

Figure 5. (a) The C-DLTS spectra as a function of transient periods (T_w) from 1.92 to 48.0 ms. (b) Arrhenius plots of the observed two traps with energy levels of 0.26 and 0.51 eV, respectively.

Table 1. The trap energy level (E_a) and cross section (σ_n) determined by the DVT measurement and C-DLTS methods.

Trap	E_a (eV)	σ_n (cm^2)
DP1 (DVT measurement)	0.28	0.46×10^{-18}
E_1 (DLTS)	0.26	1.93×10^{-18}
DP2 (DVT measurement)	0.48	0.50×10^{-16}
E_2 (DLTS)	0.51	2.25×10^{-16}
DP3 (DVT measurement)	T-independent	—

and the analysis was also consistent with the filling mechanisms with a negative gate bias during the transient curve measurement [7, 30–32].

To determine the energy levels of two electron traps, the DLTS spectra were measured with transient period (T_w) ranging from 1.92 ms to 48.0 ms, and the peaks of the traps shifted correspondingly in figure 5(a). Figure 5(b) presented the Arrhenius plots of two electron traps, which were obtained from the 'maximum evaluation' method of the DLTS system [12]. It can be seen that the values of energy level and capture cross section were determined to be 0.26 eV and 1.93×10^{-18} cm^2 for E_1, and 0.51 eV and 2.25×10^{-16} cm^2 for E_2. The above values obtained with C-DLTS were presented in table 1, along with the results of the DVT measurement. It revealed that the energy levels and cross sections of DP1 and DP2 were close to those of E_1 and E_2, respectively, suggesting that the traps observed with two techniques may be attributed to the same origin.

To obtain more information of the trapping behaviors, the above results observed with two techniques were compared with the trap levels reported in previous literatures as summarized in table 2. Specifically, the traps with similar energy level of 0.28 eV were identified to be located in the surface of AlGaN layer, which has been widely reported in previous studies using transient curves measurement [19, 24] and DLTS

Table 2. A summary of energy levels in AlGaN and GaN layers of GaN HEMTs.

Literatures	Method to obtain the energy level	E_a (eV)	Interpretations and positions
DasGupta *et al* [24]	Current-transient method	0.26	AlGaN surface
Okino *et al* [42, 43]	Current deep-level transient spectroscopy (I-DLTS)	0.34/0.3	AlGaN surface states
Jabbari *et al* [35]	Capacitance deep-level transient spectroscopy (C-DLTS)	0.31	AlGaN barrier layer
Gassoumi *et al* [44]	I-DLTS	0.24	AlGaN surface
Our work	DVT measurement/C-DLTS	0.28/0.26	Possibly AlGaN surface
Joh and Alamo [10]	Current-transient method	0.57	AlGaN barrier layer
Chini *et al* [17, 34]	Pulsed *I*–*V*, I-DLTS	0.5	AlGaN barrier layer at the gate-drain edge
Sozza *et al* [13]	Gate-lag measurement	0.53	AlGaN barrier layer
Sin *et al* [45]	I-DLTS	0.5	N antisites in the AlGaN barrier
Our work	DVT measurement/C-DLTS	0.48/0.51	Possibly AlGaN barrier layer
Joh and Alamo [10, 31]	Current-transient method	T-independent	GaN buffer
Zheng *et al* [21, 46]	DVT measurement/ current-transient method	T-independent	GaN buffer
DasGupta *et al* [24]	Current-transient method	T-independent	GaN buffer
Wang *et al* [47]	Current-transient method	T-independent	GaN buffer
Our work	DVT measurement	T-independent	Possibly GaN buffer

measurement [35, 42, 43]. The traps were likely to be originated from the surface states and can be filled by the electrons from gate under the reverse gate voltage [44]. Besides, the traps with similar energy level have also been identified using the DLTS measurement with a negative gate bias [42, 43], which was related with the depth of surface states from the conduction band probably due to the electron hopping between surface states [36, 42]. In addition, the traps with energy level close to 0.48 eV were reported to be located in the AlGaN barrier layer using DLTS [34, 38, 45, 48] and other techniques [10, 13, 49]. The traps in the AlGaN barrier were also observed using DLTS with the peak presented at 300 K [45], which was similar to our results in figure 5(a). Furthermore, the electron traps with cross section of 1×10^{-16} cm^2 were also reported to be in the AlGaN barrier using the current-transient method [17]. Besides, the traps with similar time constant ($\sim$ms) have also been observed in the AlGaN layer in previous studies [10, 17, 19].

From the table 2, one can see that the experimental data of the former two traps obtained with two methods in our work agreed well with the results of the listed literatures. Besides, the assumptions of the DP1 and DP2 located in the AlGaN barrier layer were consistent with the dependence of charge trapping on filling voltages analyzed before in figure 3(c), for the traps in the AlGaN layer were affected by both the gate and drain voltages [31, 34]. The possible locations of DP1 and DP2 were also consistent with the results of pulsed measurements. Specifically, it can be observed that the amplitude of DP1 was relatively small compared with the other two traps in figure 3(c), suggesting that the traps in the surface may be few [19]. This result was consistent with the decrease in $g_{\mathrm{m,peak}}$ in figure 1(a), which verified that the DP1 can be related to the surface states in the access region [9, 14]. In addition, it can be observed that the amplitude of DP2 was the largest of the three traps in figure 3(c), suggesting that this trap may dominate the trapping effect [22]. The above results were also in accordance with the remarkable positive shift in V_{TH} in figure 1(a), indicating that the current collapse was mainly related to the traps under the gate in the AlGaN layer [24–26]. Based on the above discussions, we analyzed that the trap levels determined by different methods can be correlated to present a detailed comprehension of the properties of traps.

In particular, a temperature-independent trap designated DP3 was only observed with the DVT measurements in this study. The traps with the time constant insensitive to temperature have been reported in previous studies with the transient curve measurement in GaN HEMTs [21, 24, 46]. In this study, the thermal response due to the self-heating can be ruled out, because the time constant of this trap ($\sim$5 s) was much slower than typical thermal time constant ($\sim\mu$s) [50]. Besides, as the DP3 was insensitive to temperature, it was unlikely to be a hot-electron trapping process with negative temperature dependence [46, 51]. Therefore, we analyzed that this trap can be related to the electrons trapping perhaps through a tunneling process [10, 46], which has been reported with the similar bias voltages applied on the GaN HEMTs [24] and may be linked to the tunneling of electrons into 2DEG states from the buffer [19, 24]. This kind of trap was considered to be located in the GaN buffer [10, 24, 50], which may involve a bottleneck transport process in series with a detrapping process [21, 47].

In addition, the effect of filling voltage on the amplitude of DP3 in figure 3(c) was also consistent with the analysis, for the charge trapping in the GaN buffer was mainly affected by the drain voltage whereas the impact of gate voltage was slight [8, 10, 30]. It may result in the variation of the transient current or voltage and the degradation of the device performance [30, 47], which deserves further investigation. As this kind of trap can be identified with the dynamic current or voltage measurement, it suggested that the transient curves analysis may be particularly effective in characterizing this kind of trap.

4. Conclusion

In summary, a comprehensive investigation of trapping behaviors in GaN HEMTs was presented based on the pulsed *I*–*V* characterization, DVT measurement, and C-DLTS method. The pulsed transfer and output measurements were performed on the device, and the results reflected the trapping effect under the gate and in the access region preliminarily. The dynamic trapping behaviors were investigated with the DVT measurement and the properties of three traps were obtained. To confirm the above results, the C-DLTS measurement was performed on the same device, and a good matching of two electron traps was observed with the energy levels of 0.28 eV and 0.48 eV, respectively. In addition, a third trap insensitive to temperature in the GaN layer was obtained only with the DVT measurement, which was also reported with the current-transient method. It suggested that the measurement of transient curves can be efficient in characterizing the temperature-independent traps. This comparison can provide the feasibility of DVT measurement along with the correlation to C-DLTS method, which allows investigating the origin of traps with the data presented with different techniques.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

The authors acknowledge the National Natural Science Foundation of China (NNSFC) under Grant No. 61974007 and the Beijing Municipal Education Commission under Grant KZ202110005001. We are thankful for the PhysTech GmbH FT1030 DLTS system supported from China Astronautics Standards Institute.

ORCID iDs

Shijie Pan https://orcid.org/0000-0002-0793-8806
Xuan Li https://orcid.org/0000-0002-6552-269X
Kun Bai https://orcid.org/0000-0002-2251-8623
Lixing Zhou https://orcid.org/0000-0002-5472-0682

References

[1] Zhu J J *et al* 2020 *Appl. Phys. Lett.* **116** 222101
[2] Chen X *et al* 2020 *Appl. Phys. Lett.* **117** 263501
[3] Omika K, Takahashi K, Yasui A, Ohkochi T, Osawa H, Kouchi T, Tateno Y, Suemitsu M and Fukidome H 2020 *Appl. Phys. Lett.* **117** 171605
[4] Zheng X-F, Dong S-S, Ji P, Wang C, He Y-L, Lv L, Ma X-H and Hao Y 2018 *Appl. Phys. Lett.* **112** 233504
[5] Subramani N K, Couvidat J, Hajjar A A, Nallatamby J-C and Quéré R 2018 *IEEE Electron Device Lett.* **39** 107
[6] Sun W Y, Jimenez J L and Arehart A R 2020 *IEEE Electron Device Lett.* **41** 816
[7] Hu J, Stoffels S, Lenci S, Groeseneken G and Decoutere S 2016 *IEEE Electron Device Lett.* **37** 310
[8] Duffy S J, Benbakhti B, Zhang W, Ahmeda K, Kalna K, Boucherta M, Mattalah M, Chahdi H O, Bourzgui N E and Soltani A 2020 *IEEE Trans. Electron Devices* **67** 1924
[9] Bisi D, Meneghini M, Santi C D, Chini A, Dammann M, Bruckner P, Mikulla M, Meneghesso G and Zanoni E 2013 *IEEE Trans. Electron Devices* **60** 10
[10] Joh J and Alamo J A 2011 *IEEE Trans. Electron Devices* **58** 1
[11] Yang S, Huang S, Wei J, Zheng Z Y, Wang Y R, He J B and Chen K J 2020 *IEEE Electron Device Lett.* **41** 685
[12] Fang Z, Claflin B, Look D C, Green D S and Vetury R 2010 *J. Appl. Phys.* **108** 063706
[13] Sozza A *et al* 2005 *IEDM Technical Digest* 590
[14] Meneghini M, Ronchi N, Stocco A, Meneghesso G, Mishra U K, Pei Y and Zanoni E 2011 *IEEE Trans. Electron Devices* **58** 2996
[15] Zheng X, Feng S W, Zhang Y M and Yang J W 2016 *Microelectron. Reliab.* **63** 46
[16] Mizutani T, Okino T, Kawada K, Ohno Y, Kishimoto S and Maezawa K 2003 *Phys. Status Solidi* a **200** 195
[17] Chini A, Fantini F, Lecce V D, Esposto M, Zanoni E, Stocco A, Ronchi N, Zanon F and Meneghesso G 2009 *IEEE Electron Devices Meeting* p 1
[18] Wang X H, Kang X W, Zhang J H, Wei K, Huang S and Liu X Y 2017 *Int. Symp. on Power Semiconductor Devices and IC's* p 231
[19] Pan S J, Feng S, Li X, Zheng X, Lu X Z, He X, Bai K, Zhang Y M and Zhou L X 2021 *IEEE Trans. Electron Devices* **68** 5541
[20] Liao Z, Guo C, Meng J, Jiang B, Gao L, Su Y, Wang R and Feng S 2017 *Microelectron. Reliab.* **74** 52
[21] Zheng X, Feng S W, Gao Y, Zhang Y P, Jia Y and Pan S 2019 *Microelectron. Reliab.* **93** 57–60
[22] Zheng X, Feng S W, Zhang Y M, He X and Wang Y 2017 *IEEE Trans. Electron Devices* **64** 4
[23] Zhu H, Meng X, Zheng X, Yang Y, Feng S W, Zhang Y M and Guo C S 2018 *Solid-State Electron.* **145** 40
[24] DasGupta S, Sun M, Armstrong A, Kaplar R J, Marinella M J, Stanley J B, Atcitty S and Palacios T 2012 *IEEE Trans. Electron Devices* **59** 2115
[25] Vetury R, Zhang N Q, Keller S and Mishra U K 2001 *IEEE Trans. Electron Devices* **48** 3
[26] Benvegnù A, Bisi D, Laurent S, Meneghini M, Meneghesso G, Barataud D, Zanoni E and Quere R 2016 *Int. J. Microw. Wirel. Technol.* **8** 663
[27] Kuzmik J *et al* 2007 *Phys. Status Solidi* a **204** 2019
[28] Li X *et al* 2020 *IEEE Trans. Electron Devices* **67** 12
[29] Pan S J, Feng S W, Li X, Zheng X, Lu X Z, Hu C X, He X, Bai K, Zhou L X and Zhang Y M 2021 *Semicond. Sci. Technol.* **36** 095011
[30] Butler P A, Uren M J, Lambert B and Kuball M 2018 *IEEE Trans. Nucl. Sci.* **65** 12
[31] Joh J and Alamo J D 2008 *IEEE Int. Electron Devices Meeting* p 1

[32] Gu Y, Wang Y, Chen J, Chen B, Wang M and Zou X 2021 *IEEE Trans. Electron Devices* **68** 3290
[33] Anand M J, Ng G I, Arulkumaran S, Syamal B and Zhou X 2015 *Appl. Phys. Express* **8** 104101
[34] Chini A, Esposto M, Meneghesso G and Zanoni E 2009 *Electron. Lett.* **45** 426
[35] Jabbari I, Baira M, Maaref H and Mghaieth R 2018 *Physica* E **104** 216
[36] Zhu Q, Ma X-H, Chen W-W, Hou B, Zhu J-J, Zhang M, Chen L-X, Cao Y-R and Hao Y 2016 *Chin. Phys.* B **25** 067305
[37] Polyakov A Y, Smirnov N B, Govorkov A V, Kozhukhova E A, Pearton S J, Ren F, Lui L, Johnson J W, Kargin N I and Ryzhuk R V 2013 *J. Vac. Sci. Technol.* B **31** 011211
[38] Polyakov A Y, Smirnov N B, Dorofeev A A, Gladysheva N B, Kondratyev E S, Shemerov I V, Turutin A V, Ren F and Pearton S J 2016 *ECS J. Solid State Sci. Technol.* **5** 260
[39] Polyakov A Y, Smirnov N B, Govorkov A V, Markov A V, Dabiran A M, Wowchak A M, Osinsky A V, Cui B, Chow P P and Pearton S J 2007 *Appl. Phys. Lett.* **91** 232116
[40] Polyakov A Y, Smirnov N B, Govorkov A V, Kozhukhova E A, Pearton S J, Ren F, Karpov S Y, Shcherbachev K D, Kolin N G and Lim W 2012 *J. Vac. Sci. Technol.* B **30** 041209
[41] Polyakov A Y and Lee I H 2015 *Mater. Sci. Eng.* R **94** 1
[42] Okino T, Ochiai M, Ohno Y, Kishimoto S, Maezawa K and Mizutani T 2004 *IEEE Electron Device Lett.* **25** 8
[43] Mizutani T, Ohno Y, Akita M, Kishimoto S and Maezawa K 2003 *IEEE Trans. Electron Devices* **50** 2015
[44] Gassoumi M, Grimbert B, Gaquiere C and Maaref H 2012 *Semiconductors* **46** 3
[45] Sin Y, Foran B, Joh J and Alamo J A 2011 *Phys. Status Solidi* a **208** 161
[46] Zheng X, Feng S W, Zhang Y M, Li X and Bai K 2019 *IEEE Trans. Device Mater. Reliab.* **19** 509
[47] Wang C, Zhu H, Wang S, Chu D, Liu K, Jin L, Lin R, Feng S W and Guo C S 2020 *IEEE Trans. Electron Devices* **67** 2
[48] Gassoumi M, Bluet J M, Chekir F, Dermoul I, Maaref H, Guillot G, Minko A, Hoel V and Gaquiére C 2005 *Mater. Sci. Eng.* C **26** 383
[49] Pan S J, Feng S W, Li X, Zheng X, Lu X Z, Hu C X, Shao G J and Lin G 2021 *IEEE Trans. Electron Devices* **68** 3968
[50] Zheng X, Feng S W, Zhang Y M and Jia Y P 2018 *Solid-State Electron.* **147** 35
[51] Ruzzarin M, Meneghini M, Rossetto I, van Hove M, Stoffels S, Wu T, Decoutere S, Meneghesso G and Zanoni E 2016 *IEEE Electron Device Lett.* **37** 1415