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Investigation of defect states in AlGaN/GaN high electron mobility transistors by small-signal admittance analysis

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ABSTRACT

We have performed a small-signal admittance analysis to extract trap parameters in an AlGaN/GaN high electron mobility transistor-on-Si. Whereas the admittance in the accumulation- and depletion-bias regimes is primarily due to the interface traps, the admittance near the threshold voltage and below is due to mono-energetic traps inside GaN. The density extracted for threading dislocation-related 1D traps at ≈ 0.22 eV below the GaN conduction band edge is similar to that previously reported by reverse-biased gate leakage analysis of the analyzed device. Our analysis suggests additional 1D traps of comparatively lower density $\approx 4 \times 10^{14}\,\mathrm{cm}^{-3}$ but considerably large capture cross section $\approx 8 \times 10^{-14}\,\mathrm{cm}^2$ in the GaN layer at ≈ 0.31 eV below the conduction band. The AlGaN trap density is considerably larger near the AlGaN/GaN interface than in the bulk AlGaN. The AlGaN traps mainly contribute to the voltage stretch; their admittance contribution is negligible. Gate leakage dominates the conductance at lower frequencies.

I. INTRODUCTION

In recent times, GaN-based high electron mobility transistors (HEMTs) have emerged as excellent candidates for high-frequency and high-power applications.[1,2] The large energy bandgap of GaN (3.4 eV) enables the HEMT device to withstand high temperatures and voltages, and the highly conductive two-dimensional electron gas (2DEG) at the AlGaN/GaN interface enables it to operate at higher frequencies. GaN-HEMTs, however, suffer from inherent material defects that manifest in the form of dynamic power reduction associated with gate- and drain-lag effects, current collapse, threshold voltage (V_{TH}) dispersion causing hysteresis effects, and extensive gate leakage under the reverse gate bias (V_G).[3–5] It is essential that we correctly identify the electrically active defects, which requires the extraction of the spatial and energetic profile of defect-related energy states (traps). Physics-based modeling of the device characteristics can be instrumental in extracting the trap parameters.

Traps change occupancy in response to an applied voltage signal and alter the 2DEG density through the Coulomb interaction. Delayed trap response to emit the electrons captured during the filling pulse causes a reduction in 2DEG, and hence a decreased drain current (I_D), compared to the steady state. Gate lag (a delayed

TABLE I. Parameters used for simulations in this work. "AlGaN" stands for the $Al_{0.24}Ga_{0.76}N$ barrier layer.

Q_P	Polarization charge (C cm^{-2})
ϵ_0	Vacuum permittivity (=8.85 × 10^{-14} F/cm)
ϵ_S, ϵ_B	GaN, AlGaN permittivity (= 9.8 × ϵ_0, 9.56 × ϵ_0 F/cm)
w_S, w_B	GaN, AlGaN thickness (=1500, 22 nm)
N_d	Unintentional n-type doping inside GaN (=10^{14} cm^{-3})
$E_{g,\,GaN}$	GaN bandgap (=3.4 eV)[a,b]
$E_{g,\,AlGaN}$	AlGaN bandgap (=3.85 eV)
E_B	Magnitude of the electric field inside AlGaN (V/cm)
C_B	AlGaN barrier layer capacitance (F/cm^2)
C_s	Bias-dependent GaN capacitance (F/cm^2)
C_t	Frequency-independent trap capacitance (F/cm^2)
G_t	Frequency-independent trap conductance (S/cm^2)
D_{it}	AlGaN/GaN interface trap density (cm^{-2} eV^{-1})
N_t', N_t	Trap density (cm^{-2}), (cm^{-3})
N_{bt}	Trap density inside AlGaN (cm^{-3} eV^{-1})
Y_{traps}	Small-signal trap admittance (S/cm^2)
Y_{st} (Y_{bt})	Small-signal GaN (AlGaN) trap admittance (S/cm^2)
$E_{c,\,AlGaN}$	AlGaN conduction band minimum energy (eV)
$E_{c,\,GaN}$	GaN conduction band minimum energy (eV)
ΔE_c	AlGaN/GaN conduction band offset (=0.282 eV)
E_{c0}	GaN conduction band minimum energy at the AlGaN/GaN interface (eV)
E_{v0}	GaN valence band maximum energy at the AlGaN/GaN interface (eV)
E_{t0}	Trap energy level at the AlGaN/GaN interface (eV)
E_f	Fermi energy level inside GaN (eV)
x (x')	Distance into AlGaN (GaN) from the AlGaN/GaN interface (cm)
σ_n	Trap capture cross section for electrons (cm^2)
R_{leak}	Gate leakage resistance (Ω cm^2)
R_S	Series resistance (Ω cm^2)
q	Electron charge (=1.602 × 10^{-19} C)
k	Boltzmann's constant (=1.38 × 10^{-23} J/K)
h	Planck's constant (=6.626 × 10^{-34} J s)
$\hbar$	Reduced Planck's constant (=$h/2\pi$)
T	Temperature (=298 K)
m_0	Free electron rest mass (=9.1 × 10^{-31} kg)
m_n^*	Electron effective mass (kg)
N_c	Conduction band effective density of states [~2.51 × 10^{25}(m_n^*/m_0)$^{3/2}$(T/300)$^{3/2}$ m^{-3}] (assumed 2.2 × 10^{18} cm^{-3} inside GaN in this work at 300 K)[c]
v_{th}	Electron thermal velocity [~ 1.17 × 10^5(m_0/m_n^*)$^{1/2}$(T/300)$^{1/2}$ m/s] (assumed 2.6 × 10^7 cm/s in this work at 300 K)[c]
c_n	Trap capture co-efficient for electrons (=σ_n v_{th} cm^3/s)
n_s	Free electron concentration inside GaN at the AlGaN/GaN interface (cm^{-3})
j	= $\sqrt{-1}$
ω	Angular frequency (rad/s)
V_{TH}	Threshold voltage (=−3.3 V)

[a]See Ref. 19.
[b]See Ref. 20.
[c]See Ref. 21.

response in I_D to a V_G pulse) is usually ascribed to the traps in the source- and drain-access regions at (near) the AlGaN surface,[3,4,6] whereas drain lag (a delayed I_D response to a drain voltage [V_D] pulse) and current collapse (a recoverable decrease in I_D when V_D is ramped to large voltages) to traps inside the GaN buffer layer.[3] Meneghini *et al.*[4] identified the V_{TH} dispersion and hysteresis effect with traps at the gate/AlGaN interface, whereas Polyakov *et al.*[7] associated the same with traps inside the GaN buffer. Zhang *et al.*[8] and Zhou *et al.*[9] were able to simulate the experimentally observed gate-lag turn-on transients by considering acceptor-type traps inside the GaN buffer. It is apparent from these reports that the observed parasitic behavior could be a cumulative effect of traps in different parts of the device.

Capacitance- (*C*-) and current- (*I*-) deep-level transient spectroscopy (DLTS) techniques are regularly used to extract trap energy (E_t) and capture cross section for electrons (σ_n) in GaN devices.[10] (Refer to Table I for the definition of parameter labels used in this work.) However, the extracted traps are usually assigned to defects at (near) the AlGaN surface or (and) inside the GaN buffer layer. For example, Mitrofanov and Manfra extracted traps ≥ 10^{12} cm^{-2} at ≈ 0.54 eV below the semiconductor conduction band edge (E_c) in a HEMT-on-SiC device using *I*-DLTS.[6] They concluded that the associated defects were donor-type and positioned at the AlGaN surface on the drain side of the gate contact. Their deduction was based on the observed strong dependence of the electron emission rate (fitted with the Poole–Frenkel emission model) on the electric field. On the other hand, Polyakov *et al.*[7] suggested that the traps at $E_c - E_t \approx 0.25$, 0.6, and 0.9 eV in their HEMT-on-sapphire devices, extracted using *C*-DLTS, were located inside the GaN buffer layer. Their belief was informed by previous reports on similar trap energy levels extracted in other GaN films. However, one cannot rule out the possibility of traps at the AlGaN/GaN interface and on the AlGaN side of the interface contributing to the current and capacitance transients. Amir *et al.*[11] extracted traps of order 10^{19} cm^{-3} eV^{-1} on the AlGaN side of the interface in a HEMT-on-SiC device by analyzing the low-frequency noise and also by calculating the small-signal admittance with a distributed circuit model for AlGaN traps. They reported interface trap density (D_{it}) in the mid-10^{12} cm^{-2} eV^{-1} range using the conductance (*G*) method. Vodapally *et al.* estimated effective trap density in mid- 10^{21} and 10^{22} cm^{-3} eV^{-1} near the AlGaN/GaN interface in planar HEMT-[12] and metal-insulator-semiconductor heterojunction field-effect transistor- (MISHFET-)[13] on-sapphire, respectively, from the low-frequency noise analysis. In the present work, we have extracted D_{it} of about 2 × 10^{13} cm^{-2} eV^{-1} at shallow energy levels (defined in Table II) and AlGaN traps of order 10^{19} cm^{-3} eV^{-1}. Thus, the density of traps (at) near the AlGaN/

TABLE II. Biasing regime and energy range defined in this work. V_{TH} is assumed to be −3.3 V.

Accumulation bias regime	$-2.5 < V_G < 0$ (V)
Depletion bias regime	$V_{TH} \le V_G \le -2.5$ (V)
Pinch-off bias regime	$V_G < V_{TH}$ (V)
Shallow energy levels	$E_{c0} - E_{t0} < 0.25$ (eV)

GaN interface can be significant, and, considering their proximity to the 2DEG channel and a broad range of response time, they can considerably contribute to the undesirable transient effects mentioned above. Therefore, their analysis is also important. In this work, we extract trap parameters at (near) the AlGaN/GaN interface using the small-signal admittance analysis.

GaN HEMTs grown on foreign substrates usually contain threading dislocations (TDs) of order $\sim 10^8$–$10^{10}\,\mathrm{cm}^{-2}$.[14–18] In an earlier report on gate leakage in the AlGaN/GaN HEMT-on-Si device analyzed in this work,[5] we extracted TD-related one-dimensional (1D) traps of density $\approx 2.4 \times 10^{16}\,\mathrm{cm}^{-3}$ at energy levels $\approx E_c - 0.49$, 0.75, and 0.81 eV inside AlGaN and slow traps (that did not contribute to the 1 MHz capacitance) of density about $1 \times 10^{12}\,\mathrm{cm}^{-2}$ at shallow energy levels. In the present work, we analyze the effect of the TD-related 1D traps on the device's small-signal admittance. We also extract other traps that contribute to the admittance.

The small-signal equivalent circuit models, initially developed for the metal–oxide–semiconductor capacitor (MOSCAP) structure, are also applicable to MISHFETs[22–24] [the circuit, however, must be correctly modified to model the barrier layer resistance accurately as discussed in Rai *et al.*[25]] and can be readily applied to the AlGaN/GaN HEMTs under reverse bias, where the AlGaN barrier layer acts as the insulator. In the small-signal admittance method, D_{it} and trap response time are extracted from the frequency dispersion in the measured capacitance and conductance. One, however, needs to separately obtain a profile of interface potential vs V_G, e.g., by comparing the simulated ideal capacitance with the measured high-frequency capacitance, to plot the energetic profiles of D_{it} and σ_n. The conductance method is regularly used to extract interface trap parameters from the measured admittance. However, we shall see that there are additional sources to the admittance, and a precise analysis requires a detailed numerical simulation.

We have organized this report in the following sections. We briefly discuss the device structure and fabrication steps in Sec. II. We discuss the interface trap admittance in Sec. III A. We also introduce the effect of series resistance (R_S), energetic profile of σ_n, and gate leakage on the admittance. In Sec. III B, we match the admittance by considering traps at the interface and inside GaN and AlGaN. We calculate the AlGaN trap admittance in Sec. III C and determine the proportion of traps at the interface and inside AlGaN. We conclude with final remarks in Sec. IV.

II. DEVICE STRUCTURE

A schematic of the AlGaN/GaN HEMT simulated in this work is shown in the inset in Fig. 1. The details of the fabrication process for this device reported by Sarkar *et al.*[26] are summarized here. The device was fabricated on a 1 mm thick Si ⟨111⟩ substrate. The buffer layers consist of an ≈250 nm AlN layer, followed by three AlGaN layers with varying Al mole fractions (≈250 nm $Al_{0.8}Ga_{0.2}N$/≈250 nm $Al_{0.55}Ga_{0.45}N$/≈500 nm $Al_{0.25}Ga_{0.75}N$), and ≈900 nm GaN layer. On top of GaN is a 22 nm thick $Al_{0.24}Ga_{0.76}N$ barrier layer. The III-nitride heterostructure was grown using the low-pressure metal oxide vapor phase epitaxy (MOVPE) technique. The heterostructure was patterned for the source and drain ohmic contacts and the Schottky-gate contact using the electron beam lithography (EBL) technique. The ohmic contacts were formed by depositing Ti/Al/Ni/Au metal stack by electron beam evaporation and annealed at 860 °C for 40 s in the N_2 ambiance. The gate contact was formed by depositing the Ti/Au (30/100 nm) metal stack. The separation between the ohmic contacts is 8.5 μm, and the 1.5 μm long gate lies at the center.

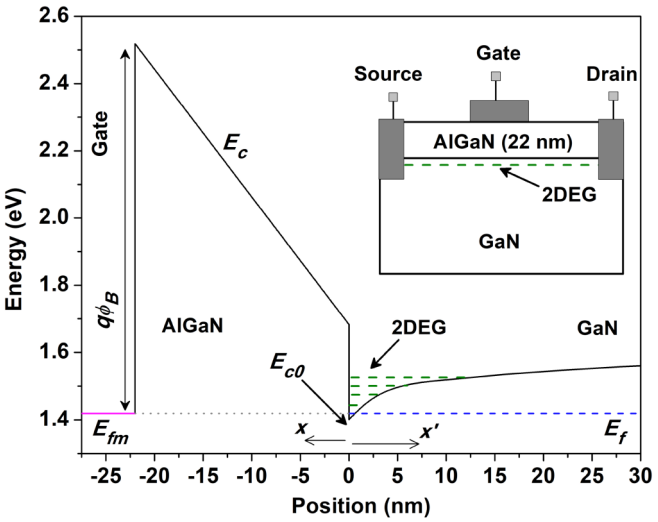


FIG. 1. Conduction band minimum energy, E_c, of the analyzed AlGaN/GaN HEMT structure simulated at zero gate bias. The intrinsic (midgap) energy level inside bulk GaN is at zero potential. x and x' are distances measured from the AlGaN/GaN interface into AlGaN and GaN, respectively. A schematic of the simulated device is shown in the inset. The labels are explained in the text.

III. SIMULATION METHODOLOGY, RESULTS, AND DISCUSSION

The material parameters used in the simulations are given in Table I. $E_{g,\mathrm{AlGaN}}$ was computed using a Vegard-type law with bowing parameter as unity.[27] $E_{g,\mathrm{AlN}} = 6.026$ eV was used.[28] We have assumed ΔE_c as 63% of the AlGaN and GaN bandgap difference. $Q_P = 1.87 \times 10^{-6}\,\mathrm{C\,cm}^{-2}$ is the polarization charge induced due to the difference in (spontaneous + piezoelectric) polarization inside AlGaN and the spontaneous polarization inside GaN, was placed at the AlGaN/GaN interface to simulate the quasi-static capacitance for the ideal device. Fixed potentials (Dirichlet boundary conditions) were used at the top of AlGaN and the bottom of GaN (refer Fig. 1); the bottom potential was fixed at 0 V. The expressions to calculate the polarization charge were taken from Ambacher *et al.*[27] An in-house self-consistent Schrödinger–Poisson MATLAB-based solver was used for the ideal $C - V_G$.

Figure 1 shows the energy band diagram of the simulated device at $V_G = 0$ V. $q\phi_B \approx 1.08$ eV is the gate Schottky barrier height.[26] $E_B = 0.38$ MV/cm was used to plot $E_{c,\mathrm{AlGaN}}$ in Fig. 1. $E_B - V_G$, which is needed to calculate the admittance due to traps inside AlGaN (discussed in Sec. III C), has been calculated using

$Q_P = 1.42 \times 10^{-6}$ C cm^{-2}. Experiments have shown that measured E_B is usually considerably lower than the theoretical and is in the mid-10^5 V/cm range at zero gate bias in normally-on GaN-HEMTs.[29] Note that the *shape* of ideal $C - V_G$ does not depend on Q_P, and, therefore, the assumed Q_P differing from the theoretical does not impact the results we report here.

We have approximated the device behavior in terms of lumped element models (LEMs), a valid approximation for frequencies (up to 1 MHz) considered in this work. The LEMs are given in Fig. 2. The equivalent circuit for the ideal device is a series connection of C_B and C_s [cf. Fig. 2(a)]. Thus, we have assumed zero gate current in the ideal case. The dashed line in Fig. 3(a) shows the simulated ideal quasi-static capacitance. Ideal V_{TH} in our case is ≈ -4.1 V; ideal $C - V_G$ in Fig. 3(a) is shifted by $+0.6$ V for the sake of comparison. We will assume measured V_{TH} as -3.3 V, referenced from the 100 kHz measured $C - V_G$. The difference in theoretical and experimental V_{TH} can be due to an error in the assumed Q_P and work function difference between gate and GaN or (and) due to traps and fixed charges. Therefore, it is difficult to comment on whether the traps within the device are of acceptor or donor type. In this work, we have assumed that all traps are of acceptor type. The stretch in V_G depends on the trap energetic and spatial profile. Therefore, the simulations can also be matched by assuming all traps of donor type or a mixture of donor and acceptor type; the net trap profile should, however, remain unchanged. The simulated curves must then be horizontally shifted accordingly along the V_G axis to align with the experimental data.

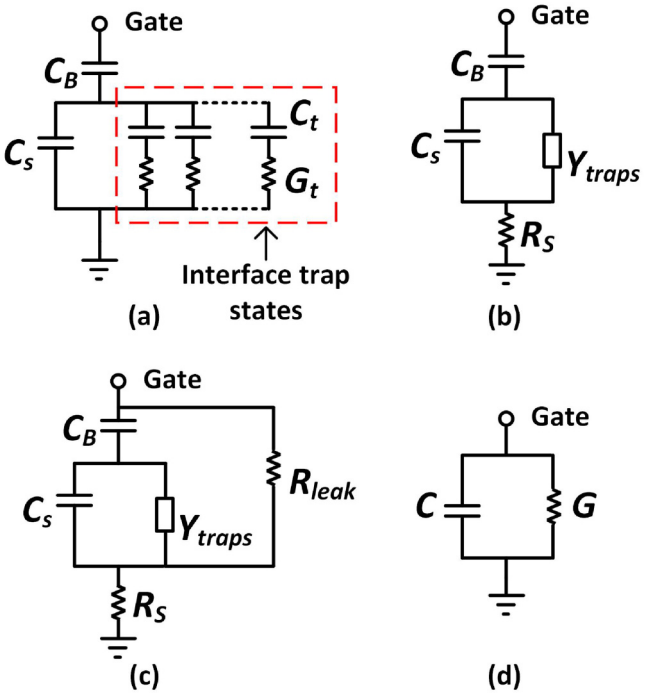


FIG. 2. Lumped element models, LEMs, of the simulated AlGaN/GaN HEMT. (a) LEM in the presence of a continuum of trap energy levels, D_{it}, at the AlGaN/GaN interface, (b) is applicable for all traps that respond to the small-signal voltage variations at the interface; R_S is the series resistance, (c) includes a finite gate leakage resistance, R_{leak}, and (d) shows overall admittance as a parallel combination of total capacitance C and conductance G. Legends are explained in Table I.

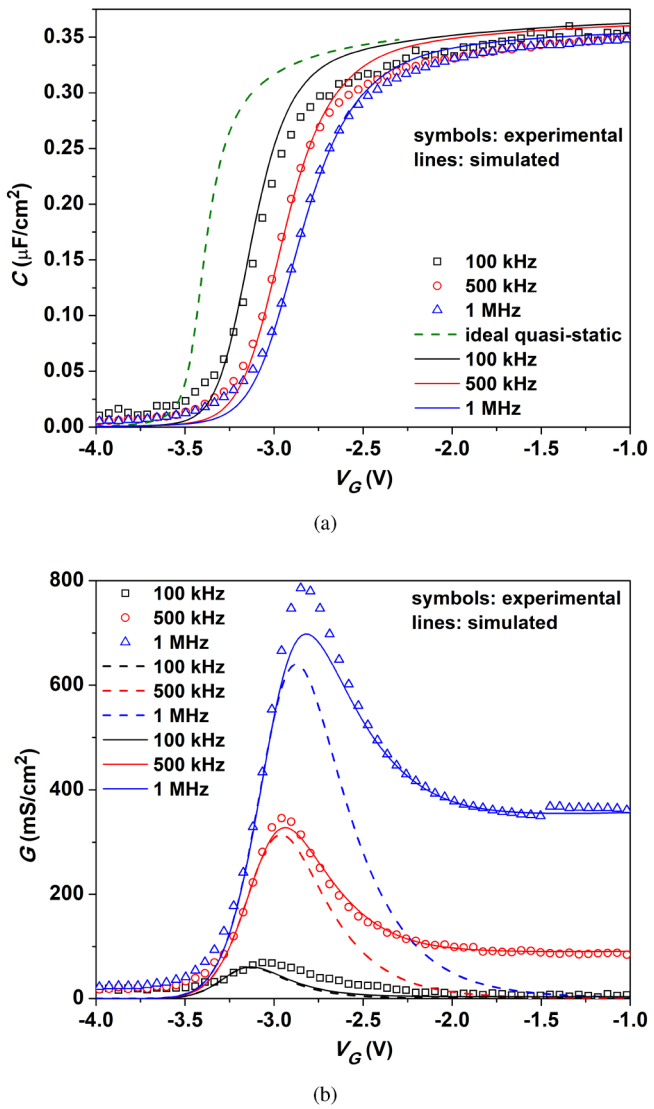


FIG. 3. (a) Capacitance and (b) conductance of the AlGaN/GaN HEMT structure (see Fig. 1) simulated with interface trap density $D_{it,1}$ and a constant trap capture cross section $\sigma_{n,1}$ ($= 8 \times 10^{-15}$ cm^2). D_{it} and σ_n profiles are shown in Fig. 4. The dashed line in (a) shows the ideal quasi-static capacitance. The solid-line curves include $R_S = 7 \times 10^{-2}\ \Omega\ \text{cm}^2$, whereas the dashed-line conductance curves are without series resistance. The experimental 500 kHz $C - V_G$ in this figure (and in other figures in this report) is from Sarkar *et al.*[26] Reproduced with permission from Sarkar *et al.*, IEEE Trans. Electron Devices **68**, 2653–2660 (2021). Copyright 2021 IEEE.

A. AlGaN/GaN interface traps

Considering that the ideal device should not show frequency-dependent behavior, the frequency dispersion in the experimental small-signal admittance must be related to traps inside the device. Hetero-interfaces are generally more prone to defect formation compared to the epilayer bulk. Therefore, we will analyze first the traps at the AlGaN/GaN interface. At the interface, we will assume a continuum of trap energy levels, D_{it}. We will neglect the admittance due to traps at the gate/AlGaN interface because, had there been such trap admittance, it must be seen at $V_G < V_{TH}$ as well, which is not the case. Traps at other interfaces are too distant to show any perceivable response to the small-signal AC variations on the gate contact.

The LEM with interface traps is shown in Fig. 2(a), where each trap branch consists of C_t in series with G_t. Each branch represents traps at energy level E_{t0}. C_t and G_t are given by Ref. 30,

$$\begin{aligned} C_t &= \beta q N_t' f_t (1 - f_t), \\ G_t &= \beta q N_t' c_n n_s (1 - f_t), \end{aligned} \tag{1}$$

where $\beta = q/kT$ and N_t' is trap density per unit area. f_t is the Fermi–Dirac occupation probability of electrons at energy E_t and is given by

$$f_t(E_t) = 1/\left[1 + \exp\left(\frac{E_t - E_f}{kT}\right)\right]. \tag{2}$$

When interface traps are present at multiple energy levels, then the admittances due to all the corresponding trap branches get added. In the case of a continuum distribution of interface trap energy levels, D_{it}, the summation is replaced by an integral.[25,30] Thus, the D_{it} admittance is given by

$$Y_t = j\omega \int_{E_{v0}}^{E_{c0}} \frac{C_t G_t}{j\omega C_t + G_t}, \tag{3}$$

where we replace N_t' with $D_{it}(E_{t0})dE_{t0}$ in (1).

Note that the trap capture time for electrons is given by $\tau_n = 1/(c_n n_s)$. c_n and n_s are temperature dependent. Therefore, a trap's response time is temperature dependent and decreases with increasing temperature. Thus, we can apply the small-signal admittance analysis technique to extract parameters of traps lying deeper in energy by performing measurements at higher temperatures. In this work, however, we have reported trap parameter extraction only at room temperature.

The admittance simulated with interface trap density $D_{it,1}$ and a constant trap capture cross section $\sigma_{n,1} = 8 \times 10^{-15}\,\text{cm}^2$ is shown in Fig. 3. D_{it} and σ_n profiles are given in Fig. 4. We can see in Fig. 3 that although $D_{it,1}$ manages to produce the required V_G stretch, the simulated capacitance is, however, considerably large. On the contrary, the peak conductance at 1 MHz is low. A lower value of $\sigma_{n,1}$ would reduce the trap response at higher frequencies, leading to an increased frequency dispersion in $C - V_G$ and a rightward shift of the conductance peak. A lower D_{it} would reduce the V_G stretch. Figure 3 is the best fit we could get with D_{it} and a constant σ_n. The solid-line admittance curves include $R_S = 7 \times 10^{-2}\ \Omega\,\text{cm}^2$. The LEM with R_S is shown in Fig. 2(b).

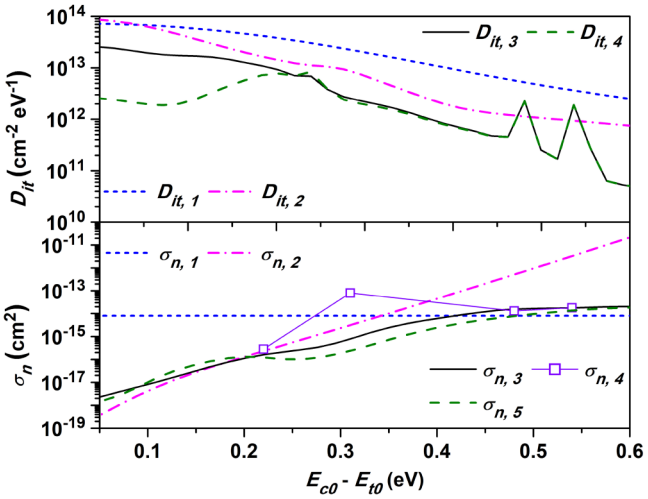


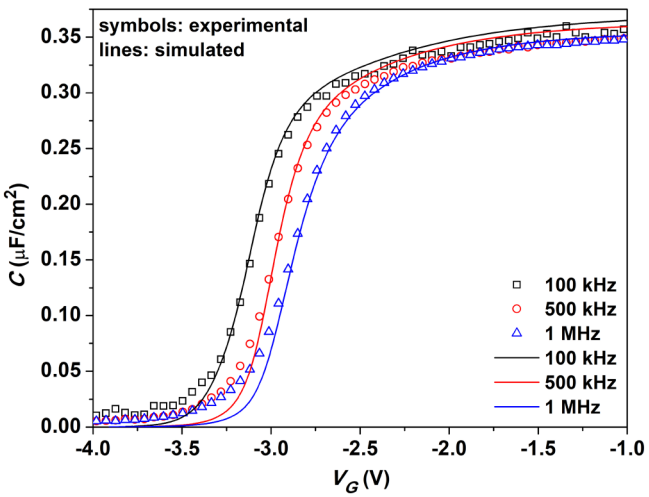
FIG. 4. Profiles of interface trap density, D_{it}, and trap capture cross section for electrons, σ_n, used in this work. σ_n has been paired with various traps in the following manner: $\sigma_{n,1}$ with $D_{it,1}$, $\sigma_{n,2}$ with $D_{it,2}$, $\sigma_{n,3}$ with $D_{it,3}$ and $D_{it,4}$, $\sigma_{n,4}$ with mono-energetic traps inside GaN (see also Table III), and $\sigma_{n,5}$ with the traps inside the AlGaN barrier layer. $D_{it,3}$ and $\sigma_{n,3}$ are the extracted profiles for the interface traps.

We next try to match the admittance with an energetic profile for σ_n. The profile for D_{it} is modified accordingly. Figure 5 shows the admittance simulated with $\sigma_{n,2}$ and $D_{it,2}$. $R_S = 3.2 \times 10^{-2}\ \Omega\,\text{cm}^2$ is included. Although fitting is better in this case, there is still a considerable mismatch. The simulated admittance is low at $V_G < -3$ V; the mismatch increases with increasing frequency. The 1 MHz simulated conductance is low at $V_G > -2.5$ V. The 100 kHz conductance is significantly low. Though we can increase the 1 MHz conductance in the accumulation bias regime by using a larger R_S, it would lead to overestimated G in the $-3 < V_G < -2$ V voltage range. R_S shows negligible effect at 100 kHz, and an additional conductance source must be considered to remove the mismatch.

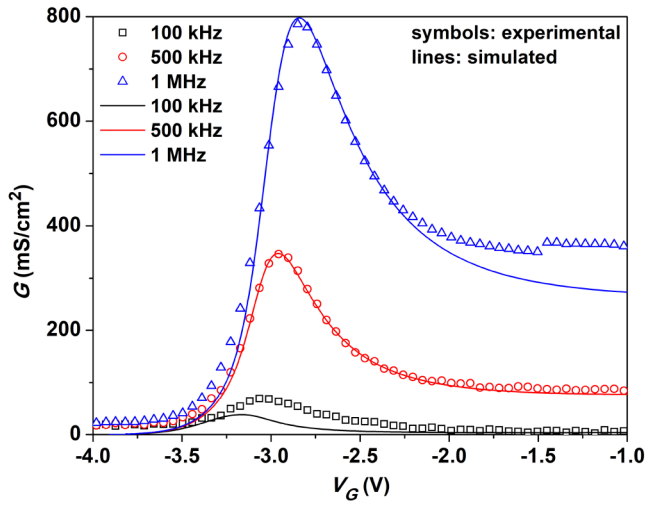
The analyzed device shows considerable gate leakage under reverse bias (see Sarkar *et al.*[26]). We realized that the 100 kHz conductance peak is because of gate leakage. The LEM with a finite gate leakage resistance, R_{leak}, is shown in Fig. 2(c). R_{leak} introduces additional conductance at higher frequencies as well. Therefore, to introduce R_{leak}, we must first reduce the conductance due to $D_{it,2}$. Though we can reduce G by increasing $\sigma_{n,2}$ over the relevant energy range, it would lead to a leftward shift of conductance peaks and a decreased frequency dispersion in the capacitance. Hence, the only way to lower G is by reducing $D_{it,2}$. However, reduced D_{it} will decrease the voltage stretch. Therefore, we must also incorporate other types of traps that would compensate for the reduced V_G stretch but would produce relatively lower admittance than D_{it}.

B. Traps inside the GaN layer

In an investigation of reverse-biased gate leakage current in the HEMT device analyzed in this work, we extracted threading



(a)



(b)

FIG. 5. (a) Capacitance and (b) conductance simulated with $D_{it,2}$ and $\sigma_{n,2}$ (see Fig. 4). $R_S = 3.2 \times 10^{-2}$ Ω cm^2 is included. A combination of D_{it} and σ_n is insufficient to fit the data.

dislocation-related 1D traps $\approx 2 \times 10^{16}$ cm^{-3} at about 0.49, 0.75, and 0.81 eV below $E_{c,\mathrm{AlGaN}}$.[5] Assuming $\Delta E_c = 0.28$ eV in our case, the TD-related 1D traps inside AlGaN are 0.21, 0.47, and 0.53 eV, respectively, below E_{c0}. Considering that TD-related 1D traps are approximately aligned in energy across the AlGaN/GaN heterostructure, see the report by Zhang *et al.*[31] and our discussion on the possible source of the extracted 1D traps,[5] we expect TD-related 1D traps at similar energy levels inside GaN. There could also be linear defects from other sources. We will refer to the various 1D traps as mono-energetic traps, METs. In this section, we analyze the effect of METs inside GaN on the device's small-signal admittance.

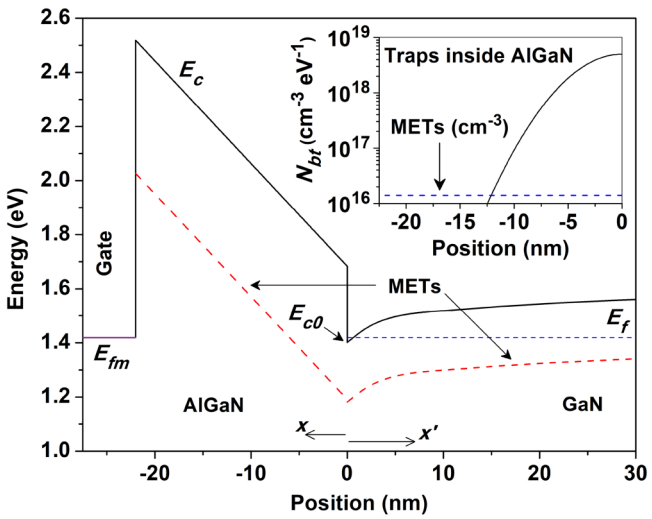


FIG. 6. Energy diagram with mono-energetic traps, METs, at 0.22 and 0.21 eV below E_{c0} inside GaN and AlGaN, respectively. The inset shows a typical spatial profile for traps (solid-line curve) inside AlGaN considered in this work.

Figure 6 shows METs inside GaN at $E_c - E_t = 0.22$ eV. METs at various energy levels inside GaN considered in this work are summarized in Table III. We have calculated small-signal admittance of GaN METs as[30]

$$Y_{st} = j\omega \int_0^{w_S} \left(\frac{V_{x'}}{V_0}\right)^{\beta} \frac{C_{tx'} G_{tx'}}{j\omega C_{tx'} + G_{tx'}}\, dx', \tag{4}$$

where $C_{tx'}$ and $G_{tx'}$ are trap capacitance and conductance, respectively, calculated using (1) [with N_t' (cm^{-2}) replaced by N_t (cm^{-3})] with electron concentration and trap occupation probability evaluated at a distance x' from the interface (cf. Fig. 6). The factor $(V_{x'}/V_0)^{\beta}$ accounts for the reduction in small-signal AC voltage away from the interface, where V_0 and $V_{x'}$ are the DC potentials at the interface and x', respectively, and β is a fitting parameter. The potential is zero at $x' = w_S$. A more precise calculation of Y_{st} requires the multiplier $(V_{x'}/V_0)^{\beta}$ in (4) be replaced by small-signal voltage ratio obtained from small-signal Poisson solution with AC variations in trap charge taken into account. Here, we have adopted a simplistic approach to account for the AC coupling between the interface and x' where we first calculate the DC voltage ratio $V_{x'}/V_0$ for the ideal device and then modulate the ratio using β to fit the data. $\beta = 1.7$ was needed for the match.

TABLE III. Parameters of mono-energetic traps inside GaN.

$E_{c,\mathrm{GaN}} - E_t$ (eV) [Label]	N_t (cm^{-3})	σ_n (cm^2)
0.22 [METs-1]	1.4×10^{16}	2.8×10^{-16}
0.31 [METs-2]	4×10^{14}	8×10^{-14}
0.48 [METs-3]	1.4×10^{16}	1.3×10^{-14}
0.54 [METs-4]	1.4×10^{16}	1.8×10^{-14}

Figure 7 shows the admittance simulated with interface traps $D_{it,3}$ and the METs inside GaN. The GaN MET parameters are listed in Table III. We can see that the simulation nicely matches the measurement. Solid-line curves include R_{leak}, whereas dashed-line conductance graphs in Fig. 7(b) do not. R_{leak} is shown in the inset of Fig. 7(a) and was obtained by differentiating the room temperature gate leakage current density with respect to the gate voltage (the current density graph is given in Fig. 2 of Sarkar *et al.*[26]). R_{leak} has a negligible effect on capacitance. LEM with R_{leak} is shown in Fig. 2(c).[32] $R_S = 6 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ is included in Fig. 7. The admittance also contains contributions from traps inside AlGaN. The AlGaN trap admittance is negligible; the traps, however, help adjust the voltage stretch. METs, as well as traps with spatial and energetic profiles, have been considered inside AlGaN. A typical spatial profile of AlGaN traps is shown in the inset of Fig. 6. AlGaN trap admittance is discussed in Sec. III C.

The device admittance when $D_{it,3}$ (solid lines) and the METs inside GaN (dashed lines) are considered separately is shown in Fig. 8. The graphs have been plotted against a common voltage

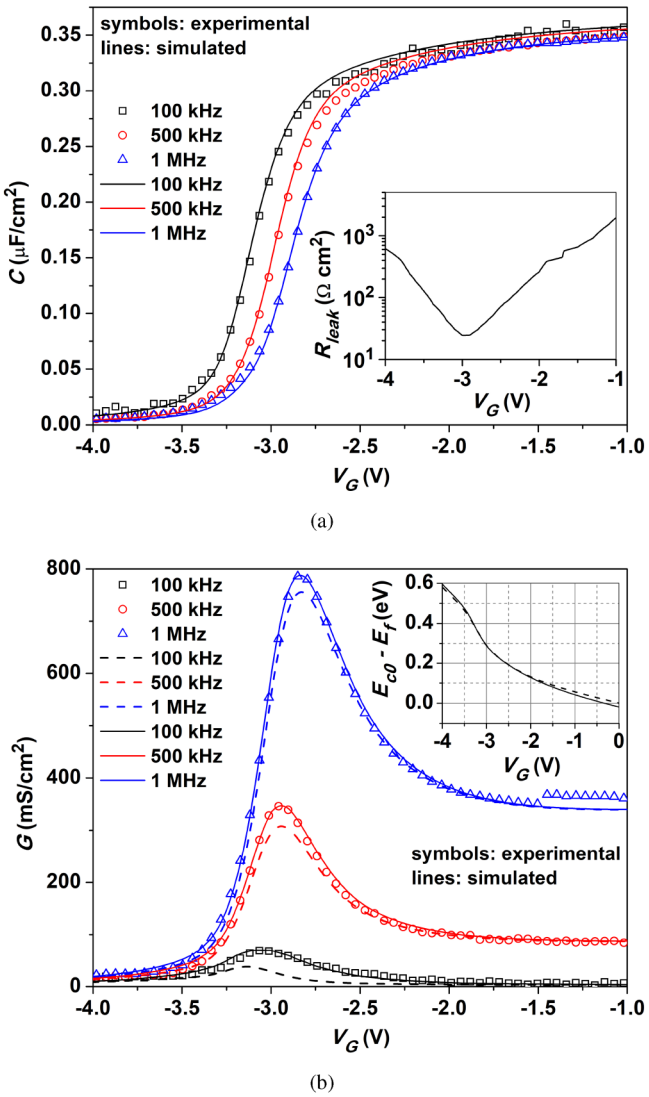


FIG. 7. (a) Capacitance and (b) conductance simulated with $D_{it,3}$ and $\sigma_{n,3}$ (see Fig. 4), and the METs inside GaN (cf. Table III). The solid-line curves include R_{leak}, whereas the dashed-line conductance curves do not. R_{leak} is shown in the inset of (a). $R_S = 6 \times 10^{-2}\ \Omega\,\mathrm{cm}^2$ is included. The inset in (b) shows $E_{c0} - E_f$ plotted against the voltage axis of the present figure (solid line) and against V_G of Fig. 10 (dashed line).

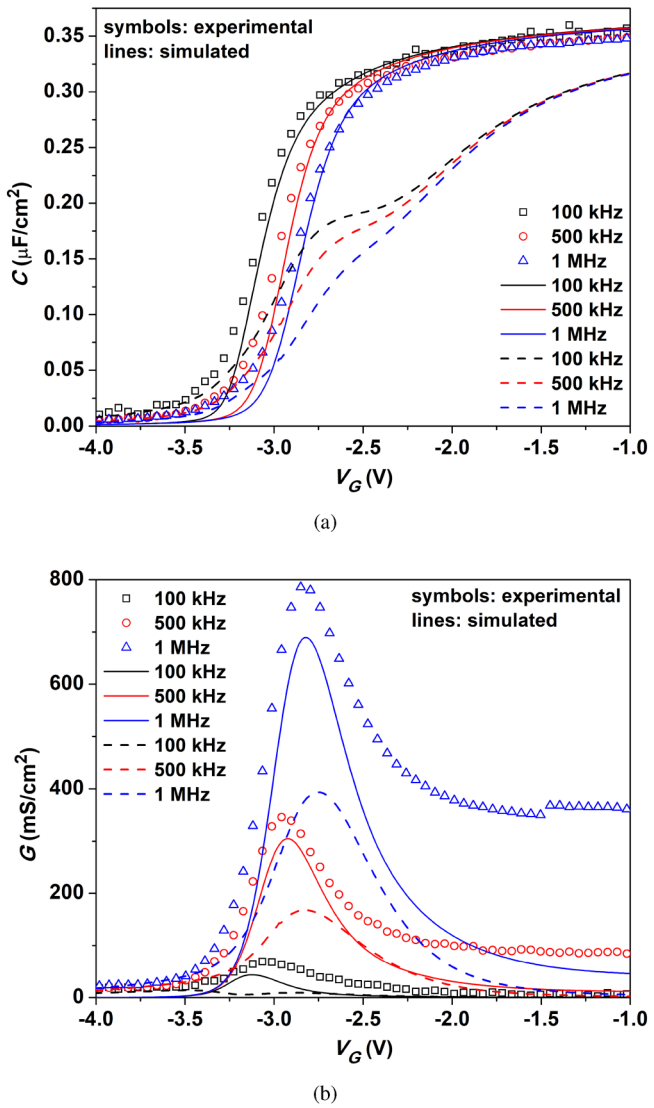


FIG. 8. (a) Capacitance and (b) conductance when $D_{it,3}$ (solid lines) and METs inside GaN (dashed lines) are considered separately. A common voltage axis, that of Fig. 7, has been used. The combined admittance is shown in Fig. 7. R_{leak} and R_S are excluded.

axis, which is the same as that in Fig. 7. The combined admittance is shown in Fig. 7. R_S and R_{leak} were excluded in Fig. 8. GaN METs mainly increase the admittance at $V_G < -3$ V and help adjust the stretch in V_G. The METs at $E_{c,\mathrm{GaN}} - E_t = 0.48$ and 0.54 eV, labeled respectively as METs-3 and METs-4 in Table III, contribute only to the V_G stretch. The majority of MET admittance comes from the traps at $E_{c,\mathrm{GaN}} - 0.22$ eV (labeled METs-1 in Table III). Additional METs of considerably large capture cross section located at $E_{c,\mathrm{GaN}} - 0.31$ eV (labeled METs-2 in Table III) were needed to match the capacitance at $V_G < -3$ V.

As discussed previously, we require traps that produce larger voltage stretch than D_{it} for similar admittance contributions. GaN METs mostly fulfill the requirement; the remaining voltage contribution comes from traps inside AlGaN. Only those traps that lie within a few kT of E_f and possess response time comparable to the measurement frequency can change occupancy in response to the applied AC signal and add to the small-signal admittance. In the case of GaN METs, the traps should also be closer to the interface for stronger AC coupling. For example, consider METs-1 shown in Fig. 6. The crossover of METs-1 and E_f occurs at $x' \approx 170$ nm at zero bias; note that $E_{c,\mathrm{GaN}} - E_f = 0.28$ eV inside bulk GaN in our case. Therefore, METs-1 admittance is negligible at $V_G = 0$ V as seen in Figs. 8 and 9. With the increasing negative bias, the crossover point of METs-1 and E_f moves closer to the interface, and the MET admittance increases, reaching the maximum value when the crossover point is at the interface. After that, the MET admittance decreases as there is no crossover. The dash-dot lines in Fig. 9 show the device admittance when only METs-1 is considered. The voltage axis is the same as that in Fig. 7. The METs-1 conductance peaks at $V_G \approx -2.75$ V, which is the bias when $E_{c0} - E_f \approx 0.22$ eV as shown by the solid line curve in the inset of Fig. 7(b). We can similarly describe the METs-2 admittance. The device admittance considering METs-2 alone is shown by solid lines in Fig. 9. Overall, the METs-2 admittance is negligible; its main role is to increase the capacitance at $V_G < -3$ V. The METs-2 capacitance at different frequencies overlap owing to a considerably large σ_n. Whereas the GaN MET admittance decreases as the crossover point moves away from the interface, the METs add an almost equal incremental voltage at each V_G as long as the crossover happens. Thus, the GaN METs produce a larger voltage stretch than D_{it} for similar admittance contributions. Note that unintentionally doped GaN, as in the present case, is usually strongly n-type, and E_f could be much closer to $E_{c,\mathrm{GaN}}$ than we have considered. However, that would only affect the value of ideal V_{TH} and not the extracted GaN-MET energy levels.

We can see a narrow peak (delta function-like spike) in $D_{it,3}$ centered at $E_{c0} - E_{t0} \approx 0.24$ eV in Fig. 4. Such a spike in D_{it} is required to produce a large conductance peak of narrow width. The spike in $D_{it,3}$ and METs-1 lie at similar energy levels and could be correlated. Assuming a similar correlation for METs at other energy levels, we have placed spikes in $D_{it,3}$ at energies similar to METs-3 and METs-4. However, these deep traps inside GaN and at the interface have negligible admittance contributions; they mainly add to the voltage stretch.

In our study of gate leakage in the analyzed device,[5] we have reported TD-related 1D traps of density $2.4 \times 10^{16}\,\mathrm{cm}^{-3}$ at energy levels similar to METs-1, METs-3, and METs-4. In the present work, we required MET density of about $1.4 \times 10^{16}\,\mathrm{cm}^{-3}$ to produce the match. The slightly larger value of 1D trap density in our earlier report could be due to a slightly larger time constant assumed for the tunneling time [see τ_0 in Table 1. and Eq. (7) in Rai *et al.*[5]]. The extracted METs-2 density (cf. Table III) is similar to that usually reported for pure screw threading dislocations (c−TDs).[14] σ_n of METs-2 is considerably large compared to the other traps (cf. Fig. 4). Large σ_n has been reported for gallium- and nitrogen-vacancy complexes in GaN.[33] However, point-defect complexes with Ga-vacancy bound to N-vacancy and even to oxygen

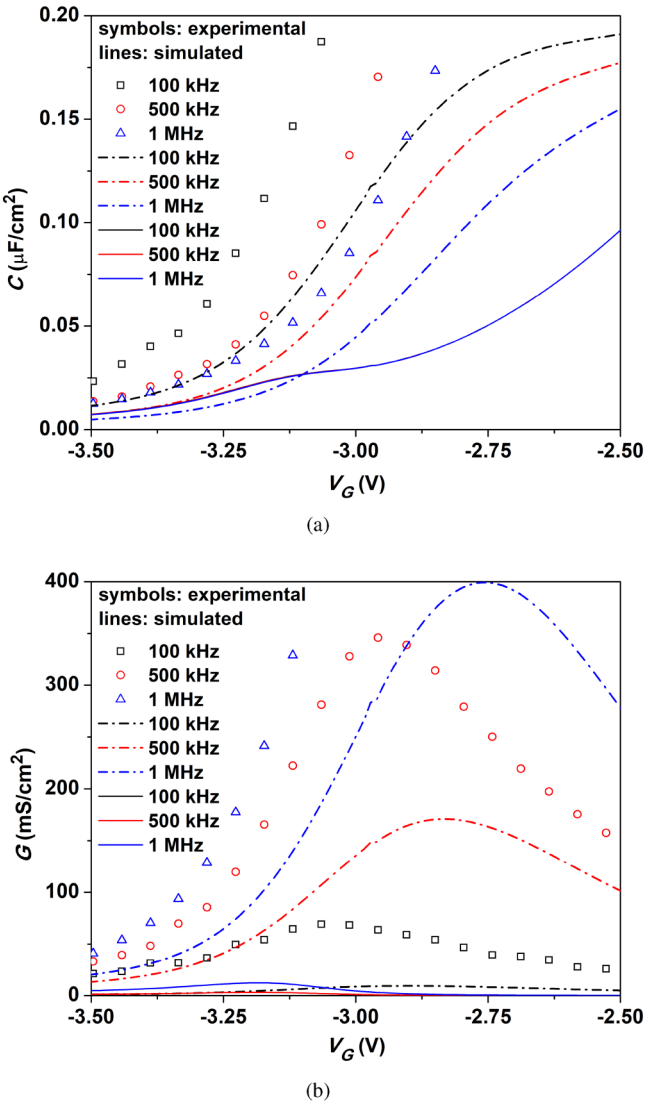


FIG. 9. (a) Capacitance and (b) conductance simulated with the monoenergetic traps, METs, inside GaN at 0.22 (dash-dot lines) and 0.31 eV (solid lines) below $E_{c,\mathrm{GaN}}$. The 1D traps are labeled METs-1 and METs-2, respectively, in Table III. The METs-2 capacitances overlap, and the conductance is negligible at the considered frequencies.

and silicon substitutional point defects have energy states very deep within the GaN bandgap.[33–35] The point defects and their complexes can, however, get trapped at extended defects, altering the local environment and broadening the energy levels.[35] C. B. Soh *et al.* reported $c-$TD-related states at ≈ 0.18 eV and $\approx 0.24-0.27$ eV below $E_{c,\mathrm{GaN}}$ associated with defect clusters along screw dislocations.[36] Northrup has suggested that $c-$TD-related states can be dispersed across the GaN bandgap.[37] Therefore, we believe that METs-2, located at $\approx E_{c,\mathrm{GaN}} - 0.31$ eV, could be associated with defect clusters trapped along $c-$TDs. We have discussed the source of METs-1, METs-3, and METs-4 in Rai *et al.*,[5] where METs-4 was associated with edge-TDs, and METs-1 and METs-3 with mixed-TDs.

C. Traps inside the AlGaN barrier layer

As mentioned previously, we are required to consider traps inside the AlGaN barrier layer to match the slope of admittance in Fig. 7. In this section, we calculate the admittance, Y_{bt}, due to AlGaN traps. We have used the model developed by Heiman and Warfield[38] to calculate Y_{bt}, where we have assumed that the traps exchange electrons with the 2DEG channel only via tunneling. The list of equations used to calculate Y_{bt} is given below, and the related parameters are explained in Table IV,

$$Y_{bt} = j\omega C_B \frac{dV_{ss}}{d\psi_s}, \tag{5}$$

$$\frac{dV_{ss}}{d\psi_s} = -\frac{q^2}{C_B}\int_0^{w_B}\int_{E_{v0}}^{E_{c0}} N_{bt}(x, E_t) g(x, E_t) \times [1 + j\omega\tau_c(x, E_t)]^{-1} \frac{\partial f_t}{\partial E_t}\, dE_t\, dx, \tag{6}$$

$$g(x, E_t) = 1 - e^{-e^{-2\kappa(x-x_m)}}, \tag{7}$$

$$\kappa = \frac{1}{\hbar}\sqrt{2m_n^*(E_{c,\mathrm{AlGaN}}(x) - E_x)}, \tag{8}$$

TABLE IV. Parameters used to simulate the admittance due to traps inside the AlGaN barrier layer.

Q_{ss}	Charge due to traps inside AlGaN (cm^{-2})
V_{ss}	Voltage equivalent of Q_{ss} ($=-Q_{ss}/C_B$) (V)
ψ_s	Potential at the AlGaN/GaN interface (V)
$N_{bt}(x, E_t)$	Trap distribution inside AlGaN ($\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$)
$g(x, E_t)$	Pseudo-Fermi function
κ	Decay constant of tunneling electrons (cm^{-1})
T_m	Measurement time at a given bias (s)
x_m	Maximum distance up to which traps can be filled during T_m (cm)
$\bar{\nu}$	Average thermal speed of electrons (cm/s)
τ_c	Trap's response time (s)
E_x	Electron energy in the tunneling direction (eV)

$$E_{c,\mathrm{AlGaN}}(x) = E_{c0} + \Delta E_c + qE_B\, x, \tag{9}$$

$$x_m = \frac{1}{2\kappa}\ln[T_m\sigma_n\bar{\nu}n_s], \tag{10}$$

$$\tau_c = \frac{1}{\sigma_{nx}\bar{\nu}[n_s + n_1]}, \tag{11}$$

$$\sigma_{nx} = \sigma_n\, e^{-2\kappa x}, \tag{12}$$

$$n_1 = N_c \exp\left(-\frac{E_{c0} - E_t}{kT}\right). \tag{13}$$

The factor $\partial f_t/\partial E_t = -\partial f_t/\partial E_f$ in (6) peaks at $E_t = E_f$ [cf. (2)] and signifies that only traps within a few kT of E_f contribute to the admittance. In (9), we have assumed that the electric field inside the AlGaN barrier layer is directed toward the gate/AlGaN interface, which is true for normally-on GaN HEMTs under reverse bias. We have assumed $E_x = E_{c0}$ and $\bar{\nu} = \nu_{th}$. We have used $T_m = 120$ s,[38] and $m_n^* = 0.27m_0$ inside AlGaN.[39]

We need a bias-dependent E_B profile to calculate Y_{bt}. We have calculated $E_B - V_G$ using the 100 kHz experimental $C - V_G$. We integrated the $C - V_G$ from the off state (i.e., $V_G \ll V_{TH}$) up to each V_G to get $Q_{2DEG} - V_G$. Note that Q_{2DEG} calculated in this manner also contains charge due to fast traps that contribute to the 100 kHz capacitance. We then calculated E_B at the AlGaN/GaN interface using Gauss's law

$$E_B(V_G) = \frac{Q_P - Q_{2DEG}(V_G)}{\epsilon_B}. \tag{14}$$

The calculated $E_B - V_G$ is shown in the inset of Fig. 10(a). Since the E_B excludes charge due to slow traps, it could be slightly different in shape from the actual. We have assumed position-independent E_B to calculate Y_{bt}.

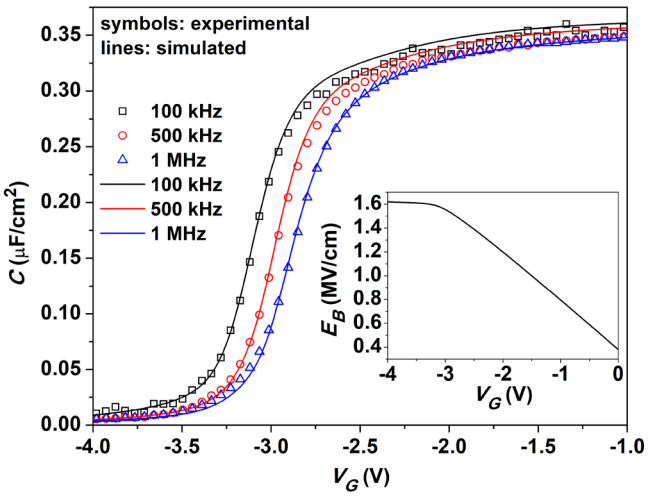
AlGaN traps considered in this work consist of METs at $E_{c0} - E_{t0} = 0.21$ and 0.47 eV and traps with spatial and energetic profiles given by

$$N_{bt}(E_t, x) = N_{bt}(E_t)\exp\left(-\frac{x}{C_x}\right)^2, \tag{15}$$

where

$$N_{bt}(E_t) = \sum_{i=1}^{N} A_{Ei}\exp\left(-\frac{E_t - B_{Ei}}{C_{Ei}}\right)^2. \tag{16}$$

The admittance in Fig. 7 contains Y_{bt} simulated with $C_x = 5\times10^{-7}$ cm and $N = 2$ where $[A_{E1} = 2\times10^{18}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, $B_{E1} = 0.21$ eV, and $C_{E1} = 0.12$ eV] and $[A_{E2} = 5\times10^{18}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, $B_{E2} = 0.47$ eV, and $C_{E2} = 0.12$ eV]. $\sigma_{n,5}$ (see Fig. 4) has been used to calculate Y_{bt}. To compute Y_{bt} due to



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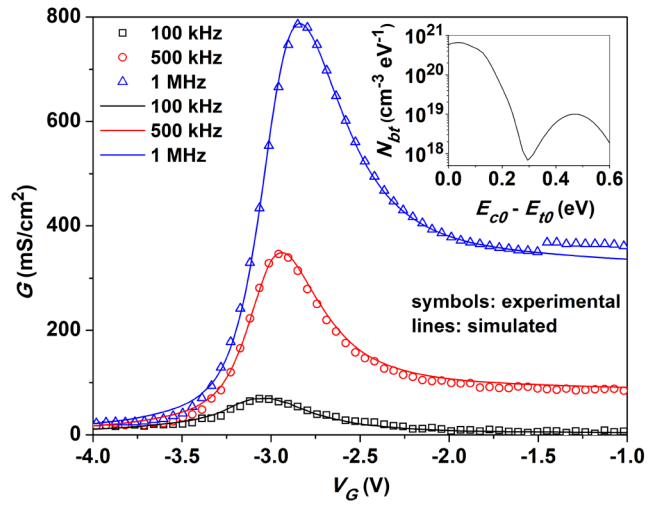


(b)

FIG. 10. (a) Capacitance and (b) conductance simulated with $D_{it,4}$, METs inside GaN, and traps inside AlGaN. The calculated electric field in the AlGaN barrier layer is shown in the inset of (a). The energetic profile of the AlGaN traps is shown in the inset of (b), and the representative spatial variation is given in the inset of Fig. 6. $R_S = 5.4 \times 10^{-2}\ \Omega\,\text{cm}^2$ and R_{leak} are included.

METs, we expressed the trap energy level in terms of x as

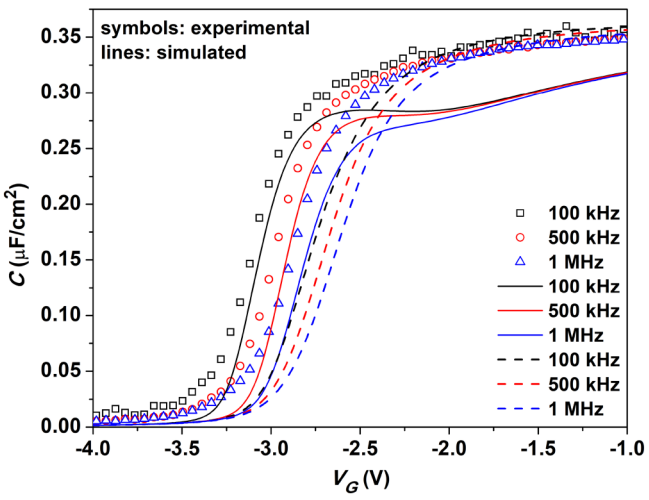
$$E_t(x) = E_{t0} + qE_B\,x. \tag{17}$$

Using (17) in (6), we then integrated over x to get the admittance. $\sigma_n = 1.5 \times 10^{-16}$ and $1.45 \times 10^{-14}\,\text{cm}^2$ were used with the AlGaN METs at $E_{c0} - E_{t0} = 0.21$ and 0.47 eV, respectively. The role of METs in Y_{bt} is insignificant, and there was no need to consider the METs at $E_{c0} - E_{t0} = 0.53$ eV in the calculations.

Traps inside AlGaN are slow to respond compared to the traps at the AlGaN/GaN interface and inside GaN due to the exponential dependence of the tunneling time on x [cf. (11) and (12)]. However, the AlGaN traps at shallow energy levels can contribute significantly to the admittance in the accumulation bias regime. Therefore, to check their effect on the admittance, we increased AlGaN traps and correspondingly reduced D_{it} at shallow energy levels. The simulated admittance is shown in Fig. 10. The relevant D_{it} profile is labeled $D_{it,4}$ in Fig. 4 and the energetic profile of AlGaN traps is shown in the inset of Fig. 10(b). $N_{bt}(x, E_t)$ was obtained by increasing N and tweaking other parameters in (16). $C_x = 4.5 \times 10^{-7}$ and 0.5×10^{-7} cm were used for traps centered at $E_{c0} - E_{t0} = 0.47$ eV and at shallow levels, respectively [cf. (15)]. $\sigma_{n,3}$ and $\sigma_{n,5}$ were used with $D_{it,4}$ and AlGaN traps, respectively. The simulated admittance in Fig. 10 also contains admittance due to METs inside GaN shown in Fig. 8. R_{leak} and $R_S = 5.4 \times 10^{-2}\ \Omega\,\text{cm}^2$ are included in Fig. 10. The device admittance when $D_{it,4}$ and AlGaN traps are considered separately is plotted in Fig. 11 against a common voltage axis which is the same as in Fig. 10. $E_{c0} - E_f$ plotted against this voltage axis is shown by the dashed-line curve in the inset of Fig. 7(b).

We used $C_x = 0.5$ nm [cf. (15)] at shallow energy levels to simulate the admittance in Fig. 10. The dispersion in $C - V_G$ is still large in the accumulation bias regime [compared to the dispersion obtained with $D_{it,3}$ in Fig. 7(a)]. Therefore, we must reduce C_x, which means that the admittance is primarily due to traps at the interface. We had previously reported slow traps $\approx 1 \times 10^{12}\ \text{cm}^{-2}$ at shallow energy levels in the analyzed device in Rai *et al.*[5] (see the inset of Fig. 2 in that report). Therefore, we expect a larger C_x for AlGaN traps. For $C_x = 0.5$ nm, the AlGaN trap profile shown in the inset of Fig. 10(b) results in a trap density $\approx 7 \times 10^{12}\ \text{cm}^{-2}$ at the shallow energy levels. If we assume that C_x is 4.5 nm, as required for traps centered at $E_{c0} - 0.47$ eV, then the AlGaN trap profile in Fig. 10(b) must be reduced by nine times to maintain the same trap charge per unit area. The profile must be further decreased by approximately seven times to have $\approx 1 \times 10^{12}\ \text{cm}^{-2}$ slow traps at the shallow energy levels. Thus, we expect the AlGaN trap density to be of order $1 \times 10^{19}\ \text{cm}^{-3}\ \text{eV}^{-1}$. The slight difference in the *shape* of $\sigma_{n,5}$ and $\sigma_{n,3}$ (cf. Fig. 4) could be due to a slightly different shape of the calculated $E_B - V_G$ from the actual. For the voltages where E_B is in excess of the actual, a lower σ_n is needed to produce the desired admittance; thus, $\sigma_{n,5}$ is lower than $\sigma_{n,3}$ at those voltages. The actual shape of E_B is given in Fig. 2 (labeled E_{B4}) of Rai *et al.*[5]

Kayis *et al.* performed low frequency-noise, LFN, analysis on an AlGaN/GaN heterostructure field effect transistor grown on a sapphire substrate.[40] They suggested that the broad additive noise peak observed in the LFN signal was associated with the electron capture and emission by traps at $\approx E_c - 0.71$ eV inside AlGaN close to the 2DEG channel and that the traps had a non-uniform spatial distribution. In this work, the extracted AlGaN traps centered at $E_{c0} - 0.47$ eV (≈ 0.75 eV below $E_{c,\text{AlGaN}}$) and 0.21 eV (≈ 0.49 eV below $E_{c,\text{AlGaN}}$) also have a non-uniform spatial profile with approximately 10× and 100×, respectively, larger trap density near the AlGaN/GaN interface than inside the bulk AlGaN. We can expect a similar trend for the AlGaN traps centered at $E_{c0} - 0.53$ eV (though we have not considered these deep traps in the small-signal admittance calculations). Subramani *et al.*[41]



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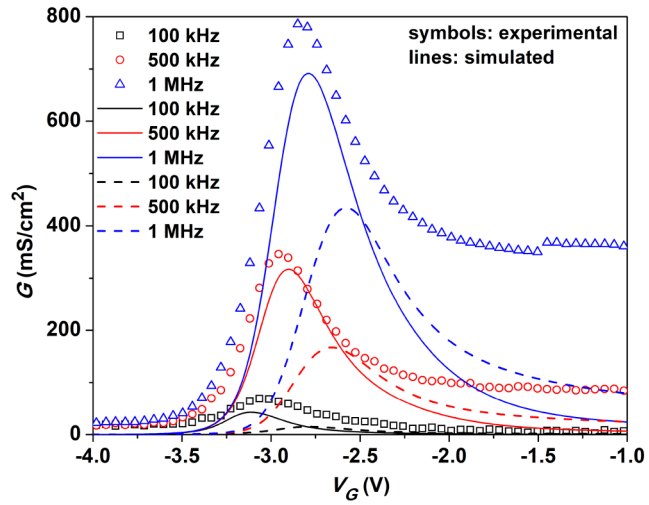

(b)

FIG. 11. (a) Capacitance and (b) conductance when $D_{it,4}$ (solid lines) and the traps inside AlGaN (dashed lines) are considered separately. A common voltage axis, that of Fig. 10, has been used. The combined admittance, along with the admittance due to the METs inside GaN (shown in Fig. 8), is shown in Fig. 10. R_{leak} and R_S are excluded.

analyzed low-frequency drain noise characteristics of a GaN/AlGaN/GaN HEMT-on-SiC by performing TCAD simulations and extracted linear traps at $\approx$ 0.51 and 0.57 eV below $E_{c,\mathrm{GaN}}$, of density of similar order as the $E_{c,\mathrm{GaN}}-$ 0.48 and 0.54 eV traps considered in this work. Thus, through small-signal admittance analysis, we were able to successfully extract density as well as spatial and energetic profiles of traps within the AlGaN/GaN heterostructure that were previously extracted or suggested in other reports. Additionally, we have accurately extracted interface trap parameters that would not be possible from the conventional capacitance and conductance methods of interface trap analysis. The extracted traps at (near) the interface have a response time in the range $\approx 10^{-8} - 10^{2}$ s and, therefore, can contribute to the device noise over a wide frequency range and also to the various other transient parasitic effects observed in AlGaN/GaN HEMTs. The traps are not only detrimental to the device performance but also the reliability as they can give way to more trap generation under high electric field stress conditions.[40]

IV. CONCLUSION

We have numerically computed the small-signal admittance of an AlGaN/GaN HEMT-on-Si and extracted trap parameters that can be easily missed in the conventional conductance and capacitance methods. The admittance near the threshold voltage and below, particularly at higher frequencies, is primarily due to the 1D traps inside GaN at $\approx E_c - 0.22$ and 0.31 eV; the latter could be associated with screw threading dislocations. In addition to the threading dislocation-related 1D traps of order $1 \times 10^{16}\,\mathrm{cm}^{-3}$ previously reported in the analyzed device, about $2 \times 10^{13}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ traps were extracted at shallow energy levels at the AlGaN/GaN interface and $\approx 1 \times 10^{19}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$ traps inside AlGaN. The density and spatial and energetic profiles of traps extracted within GaN and AlGaN in this work are similar to those previously suggested or extracted from low-frequency noise analyses in other AlGaN/GaN heterostructures. With proximity to the 2DEG channel and response time ranging over orders of magnitude, the traps at (near) the AlGaN/GaN interface can adversely affect the device's performance and reliability, and their accurate extraction is, therefore, important. This work will help elucidate the trap electronic structure within the AlGaN/GaN heterostructures and, thereby, their role in the various parasitic effects observed in HEMTs.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Narendra Rai: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Project administration (lead); Software (lead); Supervision (lead); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **Ritam Sarkar:** Data curation (supporting). **Ashutosh Mahajan:** Software (supporting). **Apurba Laha:** Investigation (supporting). **Dipankar Saha:**

Investigation (supporting). **Swaroop Ganguly:** Conceptualization (supporting); Formal analysis (supporting); Funding acquisition (lead); Investigation (supporting); Methodology (supporting); Supervision (supporting); Validation (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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