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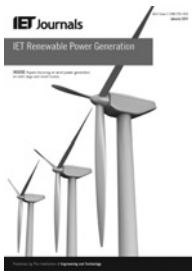

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Optimisation of the *I–V* measurement scan time through dynamic modelling of solar cells

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Abstract: High-performance solar cells and photovoltaic modules exhibit high internal capacitance, limiting the speed of their transient responses including the current–voltage characteristics scans. This study proffers a model-based method to obtain optimal scan time during the current–voltage performance characterisation of a solar cell or module while preserving a pre-set accuracy. Static model parameters are extracted from the quasi-static current–voltage characteristic, whereas the capacitive character, modelled by two bias voltage dependent capacitances, is determined from the open-circuit voltage decay measurement. The obtained model is used to calculate the optimal current–voltage curve scan time. Efficacy of the proposed method is demonstrated through test results obtained on three wafer-based solar cells. *I–V* curve errors determined by the proposed method at different scan times are in good agreement with the measurements. Results show that in order to achieve $< 0.5\%$ error in curve fitting, determined scan times of tested crystalline silicon solar cells lie within the range of 3.6–45 ms for constant angle step semiconductor curve tracer. Use of a capacitive-based curve tracer, however, requires approximately twice that time to retain a comparable error.

1 Introduction

High volume production of photovoltaic solar cells (PVSCs) and modules, regardless of the technology, requires high throughput measurement set-ups for fast and accurate cell or module characterisation. Most of the present current–voltage (*I–V*) curve tracers are either semiconductor based, where the load is varied using a high power semiconductor device, or capacitor based, where the *I–V* curve is measured during the charging phase of the connected load capacitor.

Flash solar simulators together with semiconductor *I–V* tracers that are an industry standard, deliver a short light pulse ranging from 1.5 ms (Spectrolab 460) up to 10 ms (Berger PSS series), during which an *I–V* characteristic should be measured. Despite the possible variations of measurement principles using multiple flashes, a too short *I–V* scan time is known to be a source of error [1].

Capacitor based *I–V* tracers on the other hand are very attractive owing to their low price, high power performance and portability, but owing to the limited capacitance that can be realised in such an instrument, the *I–V* curve scan time is determined by the current capabilities of the measured device. During an *I–V* scan of a high-current device, too short transient times can be reached introducing an error that is hard to detect.

Although the physical background of the discrepancy between the quasi-static and transient measurement is still not completely understood, it has been demonstrated that a parasitic bias dependent capacitance of a PVSC plays a major role in high speed measurements [1].

The gain in performance of crystalline silicon PVSCs has established a rising trend in base minority carrier lifetime and consequentially in diffusion capacitance (C_d). The PVSCs' dynamic behaviour is also affected by the junction capacitance (C_j), formed in the space charge region at the p–n junction. Both capacitances exhibit voltage dependence in a non-linear manner.

It is not only the quality of semiconductor material, but also the cell type that determines its capacitive character. Conventional front contact and emitter wrap through homojunction silicon PVSCs use medium grade silicon as their performance is not strongly effected by material quality [2]. Such solar cells typically exhibit low-to-medium internal capacitances. On the other hand, pure, electronic grade silicon that is typically used in backside contacted homojunction PVSCs [2] and thin-film PVSCs that use a-Si/c-Si materials such as heterojunction PVSCs with intrinsic thin layer can have diffusion capacitance that is orders of magnitude higher than that of conventional silicon PVSC [3]. Regardless of the technology (material quality and cell type) the increase of the surface area raises both internal capacitances in PVSCs.

I–V measurement time of a PVSC is usually upward limited by an error induced by radiation heating of the specimen on one hand and downward limited by PVSCs dynamic behaviour inducing an error at short scan times on the other hand. Extracted dynamic properties can be used to obtain the optimal scan time, which should be as short as possible while maintaining a good balance between the two possible sources of error. Dynamic characteristic is also a

useful tool for hardware and software optimisation of maximum power point trackers [4, 5], however, once solar cells or modules are used in a properly designed target system, large input capacitors of electronic converter determine the time constant of the system making the importance of photovoltaic (PV) generator capacitance inferior and negligible.

C–V meters are one of the common commercially available methods for dynamic semiconductor characterisation. Such methods are not suitable for large area silicon PVSCs exhibiting low-lumped shunt resistance. A possible solution to overcome the problem has been presented in [6], where shunt resistance is compensated prior to *C–V* measurement. Application of such a method to forward biased large-area high-efficiency PVSCs is further limited because of a small angle between the real and the complex impedance value as well as the output power of the measurement setup. Power limitations can be avoided using a high-power operating amplifier (e.g. Kepco BOP series) that also considerably increases the price and complexity of the measurement setup. Another time domain impedance measurement method has been presented in [7], where an audio power amplifier was utilised to fulfill the high-power requirements.

Simulation of a device, measured with the *C–V* method requires an arbitrary voltage dependent capacitance model, where the capacitance should be defined at small voltage intervals. To avoid manipulation of large amounts of measurement results and to gain an insight into the physical background of the device, models describing physical processes (C_d and C_j) could be used and required model parameters could be measured. There are several methods such as impedance spectroscopy, reverse recovery measurement or open-circuit voltage decay (OCVD) for precise device parameter extraction [8]. The OCVD method was selected in this work, as it can be measured with a simple apparatus and the measurement result expresses dependency on both capacitance parameters.

This paper presents a method to extract parameters of the whole dynamic model of a PVSC by an upgraded OCVD method. Furthermore, the obtained dynamic parameters are used to determine the optimal *I–V* scan time for minimisation of the *I–V* measurement error because of internal PVSC capacitance. To ascertain whether the model is accurate and can be used for estimation of error introduced by capacitor-based *I–V* tracers, the concept is verified with several *I–V* curve measurements using different capacitive loads.

2 Measurement theory

A two-diode model (Fig. 1) consisting of diodes D_1 and D_2 representing the Shockley diffusion direct current and space charge recombination current, respectively, lumped shunt resistance R_{sh}, lumped series resistance R_s and the photogenerated current under illumination I_{ph} is used in simulations [5]. Diodes D_1/D_2 are modelled with the saturation currents I_{s1}/I_{s2} and the diode ideality factors n_1/n_2.

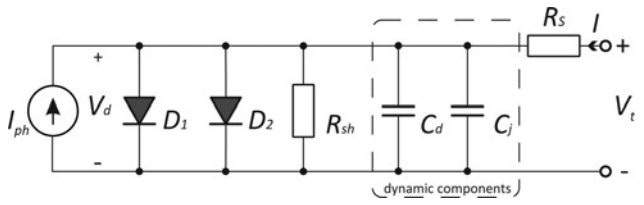

Fig. 1 *Dynamic PVSC model used for simulation*

Two capacitances (C_d and C_j) inserted into the static model (Fig. 1) determine the dynamic properties of the PVSC under investigation. Assuming an abrupt p^+–n or n^+–p junction, an analytical expression of C_j is derived from the $C_j(V_d) = -dQ/dV_d$ equation [9]

$$C_j(V_d) = A\sqrt{\frac{qN_B\varepsilon\varepsilon_0}{2(V_{bi} - V_d - (2kT/q))}} \tag{1}$$

where A is the PVSC area, q is the electron charge, N_B is the doping concentration of the base region, ε and ε_0 are the relative permittivity of the semiconductor material and the permittivity of free space, V_{bi} is the built-in voltage, k is the Boltzmann constant, T is the absolute temperature and V_d is the internal PVSC voltage – positive/negative for forward/reverse bias. Material and geometrical properties can be combined into the C_{j0} constant that physically represents the junction capacitance at zero applied voltage. Assuming ideal box profiles for depletion charges [9], (1) can be approximated as

$$C_j(V_d) = \frac{C_{j0}}{\sqrt{1 - V_d/V_{bi}}}, \quad V_d < V_{bi} \tag{2}$$

that is widely used in literature for description of junction capacitance [10–12]. Equation (2) has an evident singularity point in forward bias resulting in an inaccurate junction capacitance representation when V_d approaches V_{bi}, which in PVSCs is close to V_{oc}. Van Halen and Habib [13] presented possible corrections of junction capacitance models although we will confirm later, the model of junction capacitance in the simulation program with integrated circuit emphasis (SPICE) built-in diode-model [14]

$$C_j(V_d) = \begin{cases} \dfrac{C_{j0}}{(1 - ((V_d)/(V_{bi})))^m}, & V_d \le f_c V_{bi} \\ \dfrac{C_{j0}}{(1 - f_c)^{m+1}}\left(1 - f_c^{(1+m)} + m\dfrac{V_d}{V_{bi}}\right), & V_d > f_c V_{bi} \end{cases} \tag{3}$$

where m is junction gradient coefficient (0.5 for an abrupt junction) and f_c is a correction factor (typ. value 0.5), delivers sufficient accuracy for the whole voltage range from 0 V up to V_{oc}.

The second key component of PVSCs' dynamic behaviour, C_d, is a consequence of minority charge carrier storage in neutral regions, where because of the high doping concentration of the emitter most charge is stored in the base. C_d is thus proportional to the base minority carrier lifetime. For $V_d \gg kT/q$ (forward-biased solar cell), C_d can be written as a function of temperature, applied voltage and carrier lifetime using the following simplified equation

$$C_d(V_d) = \frac{q}{2nkT} I(V_d)\,\tau_d = \frac{q}{2nkT} I_S\, e^{(q\,V_d/nkT)}\tau_d \tag{4}$$

where q is the electron charge, n is the diode quality factor, τ_d is the effective diode base minority carrier lifetime and $I_S e^{(qVd/nkT)}$ is the diode forward DC current. In the sum of C_j and C_d in Si cells, the junction capacitance C_j is dominant up to ~0.4 V [15]. The diffusion capacitance C_d is significant from 0.4 V onwards thus the assumption of $V_d \gg kt/Q$ is justified. Furthermore, even though (3) at

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voltages V_d approaching V_{oc} does not exactly match the actual characteristics [13], the error does not contribute significantly to the total capacitance because of the dominance of C_d.

Measurement of C_d using direct C–V measurement is aggravated because of high-PVSC currents in forward bias. More often C_d is calculated from (4) whereas the lifetime τ_d is measured using one of the available methods (reverse recovery [16], short-circuit [SC] current decay [17], OCVD).

OCVD measurement starts with externally driving the device under test (DUT) with a predefined current. At $t = 0$ the current is abruptly switched off. The voltage decay on the terminals of the DUT is measured as the charge stored in the DUT diminishes with time. Voltage should be monitored as close to the DUT as possible to avoid the error of the measuring set-up series resistance.

Three characteristic regions can be defined when analysing solar cells OCVD [10]:

(i) the voltage drop because of the PVSC's series resistance,
(ii) the quasi linear region because of the charge storage in neutral region (diffusion component) – the charge is mostly released through the recombination process,
(iii) the exponential decay starts with diffusion capacitance component dropping below C_j (~0.35 V) – the charge stored in the space charge region is released through the recombination process and PVSCs shunt resistance R_{sh}.

Even though the OCVD method is most commonly used for determination of effective minority carrier lifetime [8], with both capacitances included and the static model parameters determined, we have means to extract both, the τ_d and the C_{j0} parameters. C_{j0} is extracted with minimisation of the error between measurement and simulation. τ_d, initially obtained analytically, is also included in the multivariable minimum search method to attain the best OCVD alignment possible.

3 Parameter extraction algorithm

The algorithm starts with extraction of the two-diode static model parameters (I_{s1}, n_1, I_{s2}, n_2, R_s and R_{sh}) from a quasi-static I–V curve measurement of PVSC under investigation using an improved method defined in [18]. A fully automated algorithm is developed in MATLAB® and involves the following steps:

- Influential range for series resistance R_s, diode D_1, and diode D_2 is determined from the second derivative of the input I–V curve in logarithmic scale.
- The series resistance and the diode D_1 ideality factor are extracted using a bijective transformation and linear regression [18]. The cell's internal potential $V_d = V - R_s I$ is calculated for further parameter extraction steps.
- D_1 diode saturation current is calculated using a derivative-free unconstrained simplex multivariable minimum search method (*fminsearch*) [19], I_{s1} parameter is varied until best fit between measurement and model in the upper exponential range of the I–V curve is obtained. The MATLAB *fminsearch* method is provided with the following function

$$\theta_{RMS} = \sqrt{\frac{\sum_{i=1}^{n} 2\log|I_{meas}(U_i)/|I_{model}(U_i)|}{n}} \quad (5)$$

to be minimised. It is defined as the RMS error between the target (measured) and modelled current in logarithmic scale.
- The target current for determination of the diode D_2 parameters (lower exponential range) is determined by subtracting the diode D_1 current from the total measured current. As in case of D_1 *fminsearch* function and the error function from Eq. (5) are used to determine the preliminary parameters of the diode D_2.
- The shunt resistance R_{sh} is calculated as the derivative of the I–V curve at zero voltage, subtracted by the derivative of D_1 and D_2 characteristics [18].
- The diode D_2 parameters are recalculated (*fminsearch*) also taking R_{sh} into account.
- An additional step is added to recalculate the diode D_1 parameters (*fminsearch*) to minimise the error in the range where currents of both diodes are of comparable magnitudes.

Once the static parameters are determined, we proceed with the extraction of the dynamic parameters (τ_d for C_d, C_{j0} for C_j). The effective lifetime τ_d can be extracted from the OCVD signal using equation [15]

$$\tau_d = \frac{nkT/q}{dV_d/dt} \quad (6)$$

where dV_d/dt is the slope of the linear region of the OCVD signal (region ii). In case of long lifetimes, the voltage decay is influenced by base-emitter coupling effect causing the linear region ii to deviate from a straight line [15]. In such a case, the extraction of τ_d from (6) is unreliable, therefore τ_d is further optimised after analytical extraction.

The initial approximation of the C_{j0} parameter can be calculated from (1) by considering typical semiconductor parameters of the PVSC under investigation. A higher precision of C_{j0} is obtained from region iii of the OCVD signal, where the exponential decay is driven by C_j.

An unconstrained simplex multivariable minimum search optimisation algorithm is used to minimise the error between OCVD simulation and measurement. Best fit is obtained for both, the τ_d and the C_{j0} parameters at the same time. The MATLAB code generates a SPICE netlist of the modelled solar cell with static parameters determined in the procedure defined above and dynamic parameters obtained from the abovementioned initial approximations. Transient SPICE simulation is executed within MATLAB and OCVD results are loaded into the MATLAB workspace. An error in comparison to the preloaded measurement is calculated and passed to the optimisation algorithm (*fminsearch*) that optimises the dynamic parameter values. Netlist is updated and transient simulation with all following steps are repeated until error between measured and simulated OCVD signals falls below the preselected error threshold. An abrupt junction is assumed while the value of f_c is kept at 0.5, as it does not significantly affect the simulation of the OCVD signal.

3.1 Importance of D_2 in a static PVSC model

In the early stages of our method development a one-diode model was used. However, regardless of the parameters, a one-diode model could not accurately match the measured I–V curves of several crystalline silicon PVSCs, causing additional error in extraction of the dynamic parameters. The two-diode model enabled much better matching. Fig. 2*a* shows comparison between a one- and two-diode

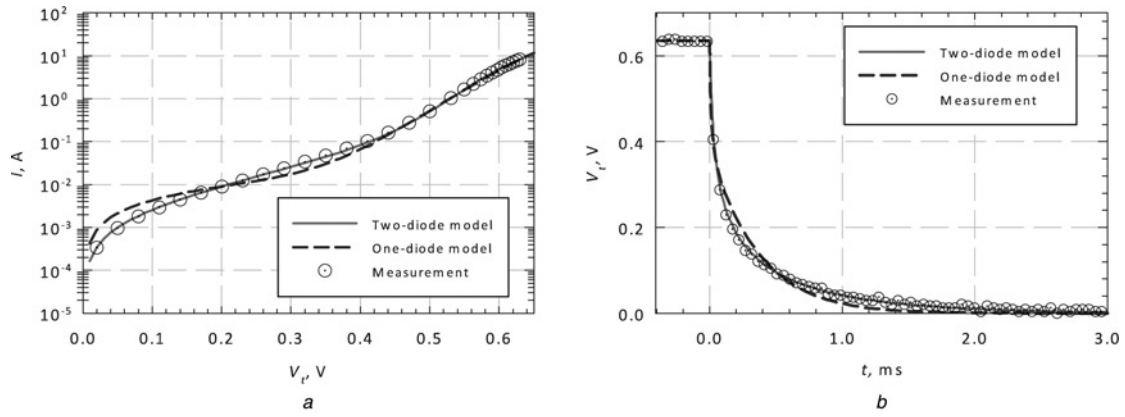

Fig. 2 *Importance of D_2 in a static-PVSC model*

a *I–V* characteristics of a measured cell and extracted one- and two-diode model calculations
b One- and two-diode OCVD signals simulations against measurement

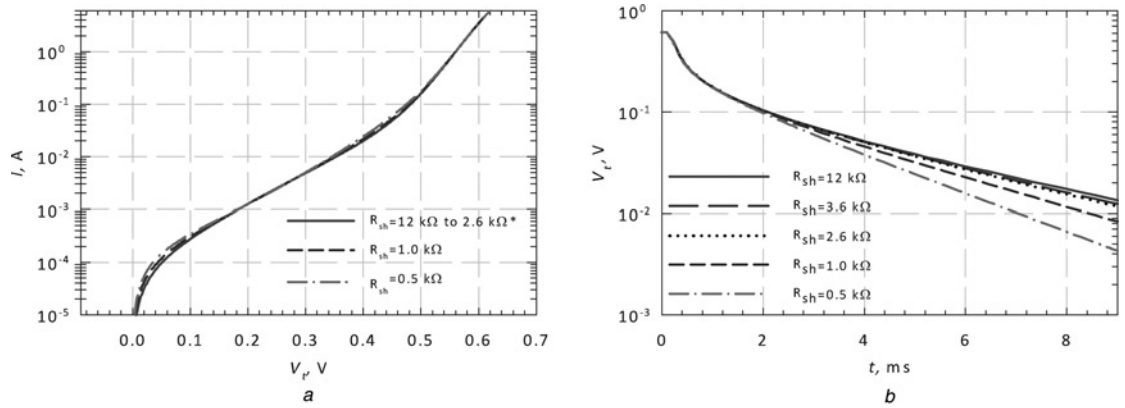

Fig. 3 *Effect of shunt resistance on dynamic parameter extraction in a two-diode model*

a Impact of erroneous R_{sh} extracted from measured *I–V* curve on modelled *I–V* curve for monocrystalline Si PVSC
b Impact of erroneous R_{sh} on modelled OCVD signal for monocrystalline Si PVSC

model *I–V* curve of a polycrystalline silicon PVSC. As the shunt resistance and the differential diode resistance at low voltages are of significant importance during the OCVD process, on Fig. 2*b* one can observe the influence of inaccurate *I–V* model on the shape of the OCVD signal. It is impossible to find good alignment between the measured OCVD and simulation when an inaccurate static model is involved (Fig. 2*b*, one-diode model).

The mismatch between the measurement and the model appears in the exponential region, therefore the extraction of C_j from OCVD strongly relies on a good static model of the PVSC under investigation. In case of a PVSC characteristic where even the two-diode model leads to insufficient *I–V* curve matching, a piecewise linear PVSC model with adjustable accuracy [20] can be used. However, use of a piecewise linear model lacks the temperature model, so all measurements and simulations have to be performed at equal temperatures.

Another possible source of error in dynamic parameter extraction is the shunt resistance value that is hard to distinguish from the influence of D_2. The error of shunt resistance determination is partially compensated for with the change of D_2 parameters. To avoid additional characterisation methods we have conducted a series of simulations to test how variation of shunt resistance in a dynamic two-diode model affects dynamic parameter extraction (Fig. 3). In Fig. 3*b*, where voltage is shown in logarithmic scale, the differences arise at lower voltages at latter times.

Based on the simulations we can conclude that change in ratio between R_{sh} and D_2 diode parameter values does not affect the dynamic parameter extraction quality as long as the modelled *I–V* curve stays in good alignment with the measured *I–V* curve.

After the static parameter extraction, the possibility of errors in dynamic parameter extraction can be detected and avoided by evaluating the agreement between measured and modelled *I–V* curve.

3.2 I–V curve comparison

Comparing *I–V* curves is problematic because of the wide curve slope span (dI/dV_t) from I_{sc} to V_{oc}. Neither current mismatch at equidistant voltage intervals nor voltage mismatch at equidistant current intervals is appropriate. We have developed and implemented a method that delivers a global *I–V* curve comparison, without favouring areas around I_{sc}, V_{oc} or maximum power point (P_{MPP}).

Compared curve points are stored in matrices $\boldsymbol{R}_{IV}$ and $\boldsymbol{P}_{IV}$ where index *I* denotes the current and *V* denotes the voltage column. The error vector is derived from loading perspective of the PVSC, calculating the error as the

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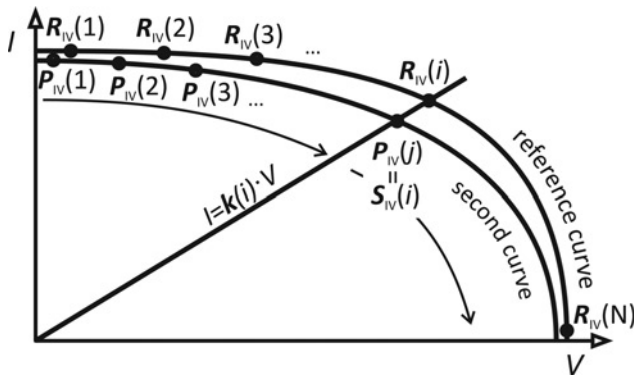

Fig. 4 *Error calculation geometry*

distance between the two intersections [points $\boldsymbol{R}_{IV}(i)$ and $\boldsymbol{P}_{IV}(j)$, Fig. 4] of a variable linear resistive load and both curves being compared.

The variable resistive load characteristic is defined as $I = \boldsymbol{k}(i)V$. At first, vector $\boldsymbol{k}$ is calculated as $\boldsymbol{k}(i) = \boldsymbol{R}_I(i)/\boldsymbol{R}_V(i)$ for each of N points of the reference curve. The point on the second curve with the smallest distance to the line $I = \boldsymbol{k}(i)V$ is determined and stored in the $\boldsymbol{S}_{IV}(i)$ matrix. Finally, the components of the error vector can be calculated as a normalised distance between points $\boldsymbol{R}_{IV}(i)$ and $\boldsymbol{S}_{IV}(i)$

$$\boldsymbol{E}_{\text{load}}(i) = \sqrt{\left(\frac{\boldsymbol{S}_V(i) - \boldsymbol{R}_V(i)}{V_{\text{oc}_{\text{ref}}}}\right)^2 + \left(\frac{\boldsymbol{S}_I(i) - \boldsymbol{R}_I(i)}{I_{\text{sc}_{\text{ref}}}}\right)^2}, \quad i = 1, \ldots, N \tag{7}$$

where $V_{\text{oc}_{\text{ref}}}$ and $I_{\text{sc}_{\text{ref}}}$ denote the OC voltage and the SC current of the reference curve. Length of the vector $\boldsymbol{E}_{\text{load}}$ equals to the length of the $\boldsymbol{R}_{IV}$ matrix. The maximum value of error vector $E_{\max} = \max(\boldsymbol{E}_{\text{load}})$ was chosen as a qualitative comparison factor to obtain information on maximum error between the two curves typically appearing close to the maximum power point. The method is susceptible to the discretisation error of the second I–V curve. Either interpolation has to be implemented or the condition

$$E_{\max} \gg \max\left[\sqrt{\left(\frac{\boldsymbol{S}_V(i) - \boldsymbol{S}_V(i \pm 1)}{V_{\text{oc}_{\text{ref}}}}\right)^2 + \left(\frac{\boldsymbol{S}_I(i) - \boldsymbol{S}_I(i \pm 1)}{I_{\text{sc}_{\text{ref}}}}\right)^2}\right], \quad i = 1, \ldots, N \tag{8}$$

has to be fulfilled to assure the discretisation error is negligible compared with the curve error.

3.3 Parameter extraction method evaluation

Evaluation of the parameter extraction method was accomplished by a series of I–V curve measurements using different capacitive loads, allowing us also to test whether the implemented dynamic two-diode model could be used for minimum scan time determination of capacitor-based I–V curve tracers. Different parallel configurations of electrolytic capacitors with values (C_{m}) listed in Table 2 were selected. Prior to the measurement, the capacitors had to be biased at -1 V to compensate for the capacitor and measurement circuitry series resistances. At $t = 0$ the selected set of capacitors was connected to the device under investigation using a low R_{DSon} MOSFET. During the charge phase of the capacitor, the I–V characteristic was measured using the NI PCI-6014 DAQ interface. Different capacitances were used to utilise different I–V curve scan times. Voltage and current transient errors as well as I–V curve errors between model simulations and measurements were calculated and will be presented in Section 4.

3.4 Scan time determination

Minimum required scan time at a predefined error threshold can be calculated from a series of transient response I–V curve simulations using the dynamic model of the device under investigation.

1. MATLAB is used to generate two SPICE netlists for simulation of I–V curve measurement. The first netlist contains an operating point analysis with variable load to ensure quasi-static conditions for the reference curve. The second netlist contains two initial transient analyses, where very short and very long initial scan times of transients are selected to yield errors above and below the predefined error threshold.
2. SPICE is executed within MATLAB for simulation of generated netlists.
3. Results are loaded into the MATLAB workspace and the curves are compared according to the algorithm defined in Section 3.2. The Newton method is utilised to calculate approximate scan time required for predefined error threshold and a new netlist is generated using the calculated scan time.
4. Steps 2–4 are repeated until the simulated transient curve error stays within a specified region around the predefined threshold ($E_{\max} \pm \delta$).

Algorithm output for cell TC2 is presented in Fig. 5. Convergence is fast as the error against scan time curve is monotonous. 15 s are required for simulation and calculation of eight points, needed to extract optimum scan time with $E_{\max} = 0.5 \pm 0.02\%$, when initial scan times were selected at 2 and 80 ms.

Different measurement load set-ups can be implemented in the simulation circuit allowing us to also analyse scan times of PVSCs connected to different curve tracer technologies.

Optimal scan time values on a set of three available conventional PVSCs of different types: a polycrystalline (TC1), monocrystalline (TC2) and back-contact monocrystalline silicon PVSC (TC3) were determined. The latter PVSC type is known for its high diffusion capacitance and is therefore of particular interest in this study.

4 Results

Dark and illuminated I–V curves and OCVD signals were measured on TC1, TC2 and TC3 solar cells. A curve tracer was constructed from parallel connection of three independent channels of two Keithley SMU 2602A units. One channel was configured as a voltage source determining the measurement voltage whereas the other two channels were configured as current sources connected in parallel, extending the current range of the set-up. All the channels were interconnected with the TSP link to provide

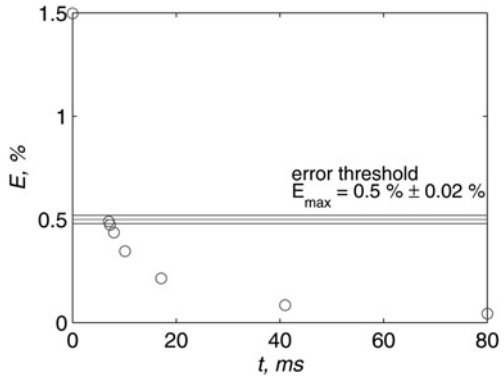

Fig. 5 *Output of optimal scan time determination algorithm for TC2 cell*

single script output control. The set-up was capable of measurements up to 1 V and 9 A with worst case voltage measurement accuracy of ±0.053% and worst case current measurement accuracy of ±0.151% [21]. OCVD measurement set-up was based on a PCI-6014 DAQ card controlling the MOSFET and measuring the voltage decay. Samples were taken at 200 ksa/s with worst case voltage measurement accuracy of ±0.031% [22].

Measurements under illumination were carried out on a temperature controlled chuck under a Newport class A continuous solar simulator. The cell temperature regulation was set to 25°C throughout the measurements and the solar irradiance of 1000 W/m^2 was set using a calibrated reference solar cell with ±2% accuracy [23].

Table 1 Parameters of the three solar cells under test

Name	TC1	TC2	TC3
type	poly si	mono si	mono si BC
A, cm^2	240	240	153
I_{sc}, A	7.52	8.59	5.88
V_{oc}, V	0.590	0.631	0.660
FF, %	69.0	78.2	72.0
P_{MPP}, W	3.06	4.24	2.70
η, %	12.5	16.9	17.9
	extracted parameters		
R_s, mΩ	0.340	0.037	0.200
R_{sh}, Ω	2854	10 479	115
I_{s1}, nA	104.0	28.8	204.1
n_1	1.293	1.260	1.543
I_{s2}, μA	1680	150	420
n_2	4.240	3.588	4.550
τ_d, μs	5.0	35.0	240.0
C_{j0}, μF	12.5	5.0	1.0

Table 2 Minimum scan times of the compared PVSCs

		TC1 poly Si	TC2 mono Si	TC3 mono BC Si
C_m, mF	Meas.	Scan time, ms		
39.1 ± 2%	A	22.0	20.5	27.0
28.5 ± 2%	B	17.1	14.9	19.0
17.7 ± 2%	C	10.3	9.1	11.0
11.6 ± 2%	D	7.0	6.2	7.4
5.0 ± 2%	E	3.1	2.8	3.2
	scan method comparison at $E_{max} < 0.5\%$			
constant angle $t_{R\min}$, ms		3.6	7.7	45.0
capac. scan $t_{C\min}$, ms		7.1	12.4	98.0

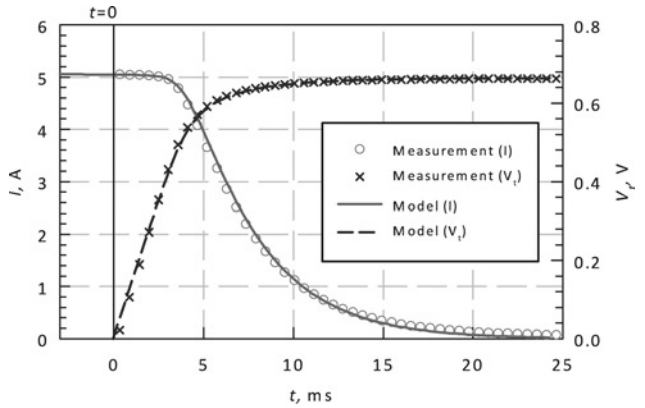

Fig. 6 *Time dependence of current and voltage – simulation against measurement of TC3 solar cell with the load of C_m = 17.7 mF (measurement C)*

Measured performance parameters as well as extracted static and dynamic model parameters of the three solar cells under test are listed in Table 1.

4.1 Parameter extraction method evaluation based on capacitive load

Evaluation of the extraction method was performed using different capacitive loads achieving different *I–V* scan times. In capacitive measurement we can define the scan time as the time in which the current into the capacitor drops below 1% of its SC value. Higher the C_m, longer the scan time (Table 2). Acquired *I–V* curve scan times using different capacitor configurations (measurements A–E) are listed in Table 2. A typical measurement result of the TC3 cell is shown in Fig. 6.

Measurements and simulations for listed C_m values were performed and the errors between the curve of the longest scan time (measurement A) and all other curves were calculated. Fig. 7*a* depicts the alignment of the *I–V* curve error between measurement and simulation for the TC2 cell that implies moderate diffusion lifetimes.

Three distinctive voltage ranges can be observed in Fig. 7

- Voltage range from 0 to 0.35 V is the area of nearly constant current where (because of the low-current slew rate) the capacitance of PVSC has no influence on the measurement error. The error in this range is only a result of measurement, illumination and temperature mismatch between the reference and the compared cell.
- Range from 0.35 to 0.58 V is the area where the PVSC capacitance limits the measurement slew rate. The error peak appears close to the point of maximum power.
- Range above 0.58 V, where the measurement slows down significantly as the capacitor is approaching its final charge causing the error to reduce. Error detected in this area is very likely caused by a change in the cell temperature.

Observing the error of measurement B, only a minor error peak around the MPP point can be detected confirming the error caused by internal capacitance compared with the reference curve is in most cases smaller than the uncertainties of other measurement parameters. The error of measurement C (9 ms) shows a small error peak starting to form about 0.5 V. The shortest measured scan time (E) of the TC2 cell is completed in 2.8 ms, where the internal capacitance of the measured cell induces an error of almost

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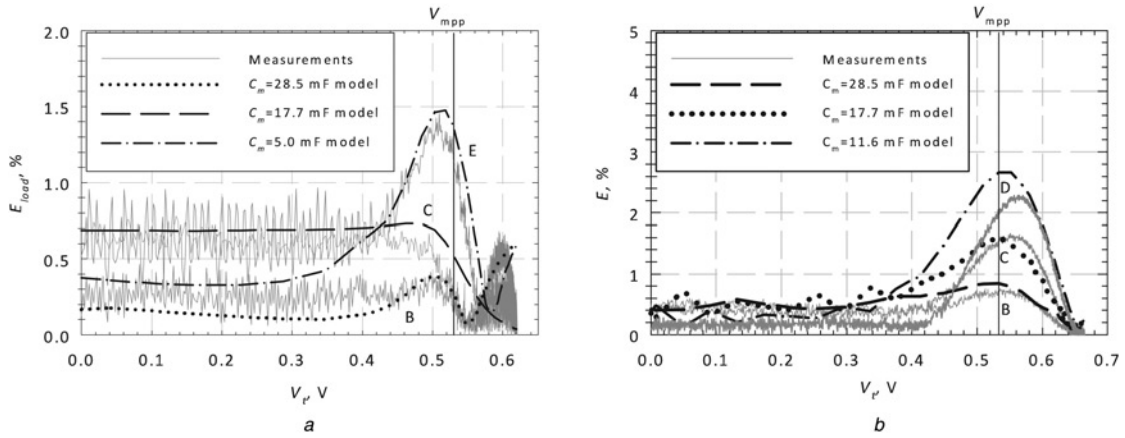

Fig. 7 *I–V curve error as a result of measured and simulated dynamic PVSC characteristics of*
a TC2
b TC3 cells

1.5%. At all scan times the errors of the model and the measurement are in good alignment, whereas at the maximum error the maximum deviation is very small (0.15%).

In case of TC3, the simulation results deviate more from the measurement ones. Fig. 7*b* displays the error of *I–V* measurements B, C and D compared with the reference curve (A). One can observe the error peak tends to be slightly overestimated and shifts towards the lower voltage.

Equation (4) of our PVSC model implements a linear OCVD signal in region ii, that cannot be exactly matched by devices with pronounced diffusion lengths (base-emitter coupling). The mismatch in $C(V)$ dependence between the model and the device causes the error peak to shift and offset. Nevertheless simplification of the model inclines towards overestimation of the error which implies one will always achieve at least the desired precision. Furthermore, our goal is to detect and avoid the error caused by the cell's dynamic behaviour and the model is satisfactorily accurate even above the error of 1%.

The comparison of voltage and current transients between measurement and simulation in Fig. 6 shows a good degree of alignment thus demonstrating that the model can be used for scan time determination for capacitive loads.

4.2 Solar cell type comparison using semiconductor-based load

To compare three different cell types, the desired maximum error was set at 0.5% as a maximum tolerable error in measurement. The cell load resistance is swept from 0 to $\infty\,\Omega$ in linear angular steps simulating a typical semiconductor-based curve tracer. Finally, a comparison to capacitor-based curve tracer is performed.

TC1 is as expected least sensitive to the *I–V* scan time. The minimum scan time that meets the given error criteria is 3.6 ms. TC2 exhibits higher diffusion capacitance and lower junction capacitance causing the error to build-up at a higher voltage range. The minimum scan time of TC2 is 7.7 ms, which is already outside flash pulse length range of many flash solar simulators (e.g. Endeas QuickSun 800, Sciencetech PSS06, Spectrolab 420/460 etc.).

The back contact cell TC3 having effective minority carrier lifetime more than a decade higher, induces high error even at a scan time of 20 ms. Only at a time above 45 ms, the measured result falls below the preset error threshold. Fig. 8 displays the influence of varied scan time on *I–V* curve shape of TC3.

Typical scan direction sensitive *I–V* curve (hysteresis between forward and reverse scan direction) of PVSC with high internal capacitance can also be observed in Fig. 8. In

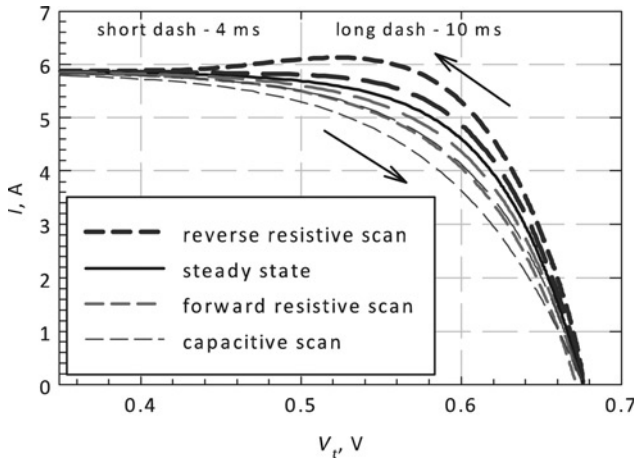

Fig. 8 *Simulation of I–V curves measured at different scan times with semiconductor and capacitive-curve tracer based on the parameters of the TC3 cell*

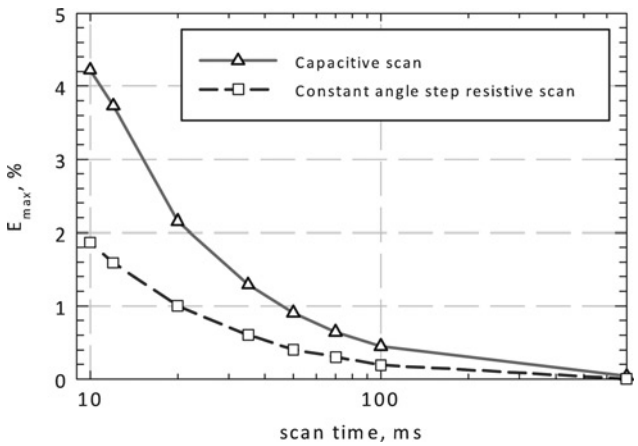

Fig. 9 *Error comparison between simulation of capacitor-based and semiconductor-based I–V tracer on TC3 cell (lines as guide to the eye)*

the reverse scan direction the curve tracer sweeps from OC condition towards the SC condition, the voltage of the parasitic PVSC capacitance cannot follow the forced current on the cell terminals resulting in overestimation of the measured curve. Starting in SC condition (forward scan direction) the capacitor cannot charge fast enough causing the *I–V* to be underestimated.

4.3 Evaluation of capacitor-based I–V measurements

Capacitors with high energy volume densities are very convenient for high power *I–V* scanners. However, besides the fact that often very short times are utilised in capacitor-based *I–V* tracers, the speed of the curve scan varies vastly with bias voltage because of the time dependence of the current flowing into the capacitor. From the *I–V* measurement error point of view, the initial fast transient is effectively decreasing total scan time as the load is varied in a too fast, non-optimal manner. The effect can be seen in Fig. 8, where comparison of semiconductor and capacitive curve tracer shows that at equal scan times a larger error is introduced in the capacitive measurement system. When capacitive measurement approaches V_{oc}, the charging rate slows down and the error decreases.

Fig. 9 demonstrates *I–V* curve error (E_{max}) of the TC3 cell measured with capacitor-based *I–V* tracer and with a more optimal constant angle step *I–V* scan method that can be implemented with a semiconductor-based *I–V* tracer. The capacitive scan error increases almost two times faster, therefore additional attention is required with capacitive measurements (the scan time depends on the power of measured device). Table 2 demonstrates ~100% increase of the minimum scan times for capacitive measurement regardless of the PVSC technology at $E_{max} < 0.5\%$.

5 Conclusions

A method for static and dynamic PVSC parameter extraction has been introduced acquiring all the required parameters from two simple measurements, an *I–V* scan and an OCVD signal. Influences of the quality of shunt resistance extraction and the quality of static model on dynamic parameters have been studied. Procedures to detect and avoid errors have been suggested. Using the newly introduced error function to estimate the *I–V* curve mismatch, a method to calculate minimum scan time has been presented.

The proposed extraction method has been applied but is not limited to different wafer based solar cells. Verification was achieved using capacitor-based *I–V* curve measurement using different capacitors and different scan times. The extraction method gives good results although there is still some space for dynamic model improvement for PVSCs with high carrier lifetimes. Influence of *I–V* curve sweep times on the curve accuracy of three different PVSC types has been analysed and a high spread of minimum scan times extending from below 3.6 up to 45 ms while keeping error within 0.5% were measured thus confirming that dynamic characteristics of high efficiency PVSC must be considered before measuring *I–V* characteristics of solar cells. Especially in case of capacitive-based curve tracers, where minimal scan times are doubled compared with the constant angle step semiconductor-based curve tracer.

The error because of internal capacitance increases with increasing conversion efficiency mostly because of C_d. Use of the proposed model and method of parameter extraction is yet a good method to study PVSC dynamic behaviour and error because of PVSC capacitance that is commonly overlooked.

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