

Deep-level transient spectroscopy of Al/a-Si:H/c-Si structures for heterojunction solar cell applications

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A Deep-Level Transient Spectroscopy study is performed on Metal-Insulator-Semiconductor capacitors with a 70 nm amorphous silicon (a-Si:H) passivation layer, in order to study the electrically active defects present at the n- or p-type crystalline silicon (c-Si)/a-Si:H heterojunction. Trap filling kinetics identify two types of traps, namely, P_{b0} dangling bond centers at the Si(100) interface and similar D centers in the a-Si:H, which are in close proximity to the interface and giving rise to a dominant peak around silicon midgap. The distinction between both kinds of deep levels is based on the carrier capture behavior, which is more point-defect-like for the P_{b0} centers and varies according to the logarithm of the voltage pulse duration for the D defects, indicating capture of majority carriers from the substrate by tunneling into a-Si:H, the densities of which are correlated with capacitance-voltage measurements. This directly demonstrates that the recombination properties of the c-Si/a-Si:H interface are both determined by P_{b0} and D defect states. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4904082>]

INTRODUCTION

Attaining high efficiency solar cells requires effective collection of the photo-generated carriers, so any mechanism whereby these carriers recombine will limit cell performance. Methods employed to ensure this include use of heterojunctions, efficient passivation layers, or even passivated contacts.^{1,2} That such efforts are considered highlights the significance of defects in these devices, and justifies the objective of controlling their densities. In the case of silicon solar cells, defects can be present in the bulk of the silicon layer, in passivation layers, at the c-Si/passivation layer interface, or at the region where the metal contacts the heavily doped silicon layer. The bulk layer characteristics, and defects therein, are strongly material dependent, and the use of single crystal silicon can enable low defect densities. At the interface between crystalline silicon and an amorphous passivating layer (for instance, SiO_2 , Al_2O_3 , a-Si:H, or Si_3N_4), the defect densities are very process specific, so any given cell design will have to be engineered to control these interfaces. Defects at the c-Si/passivating layer interface result in an increased saturation current density, which consequently reduces the device open circuit voltage and cell efficiency.³ To this end, the open circuit voltage is a monitor for the recombination within a solar cell, and some of the highest values reported (for silicon solar cells) have been obtained for a-Si:H/c-Si heterojunction type cells, where values up to 740 mV have been achieved. Indeed, the record silicon solar cell efficiency has been reached by a heterojunction silicon solar cell, which was recently reported with 25.6% efficiency.⁴ Of course, another advantage inherent in incorporating a material with a bandgap higher than crystalline silicon (such as amorphous silicon) is the

repulsion of minority carriers, and enabling their collection at the appropriate terminal.

Quantifying the defects present in the a-Si:H/c-Si type solar cell offers further understanding and serves as a prerequisite for achieving such values, and provides the focus of this work. Amorphous silicon layers, on c-Si substrates when measured cryogenically, exhibit low conductivity, and in fact, behave as insulating layers for a-Si:H layers of ≥ 50 nm thickness.⁵ Of course, this finding opens the door for Metal-Insulator-Semiconductor (MIS) technology to be applied, thereby enabling techniques developed for CMOS technologies and brings new understanding to the layers in question.

Recently, it has been shown that capacitance based measurements of a-Si:H enable the calculation of defect densities at the c-Si/a-Si:H interface, and indeed in the a-Si:H bulk.⁵ In this study, these measurements are complemented by Deep-Level Transient Spectroscopy (DLTS), a technique which can probe the electrical activity of defects in the a-Si:H layer, and those located at its interface with the c-Si base material. Such analysis builds on the studies performed on the c-Si/ SiO_2 interface⁶⁻⁹ and on some early DLTS analysis of a-Si:H-based MIS structures.^{10,11} Compared with the capacitance voltage (CV) analysis reported on similar samples previously,⁵ additional information is gained on the distribution of the Density-of-States (DOS) with respect to the energy in the silicon band gap and on the associated capture cross sections for electrons (n-Si) and holes (p-Si). In this case, we also report the results of intrinsic amorphous silicon, where any impact of a doped layer previously present is removed. It is shown here that both dangling bond P_{b0} centers at the a-Si:H/c-Si interface and D centers in the a-Si:H layer can be detected, whereby the distinguishing parameter is the trap filling kinetics. While in the first case, the DLTS peak amplitude saturates for long filling pulse duration (t_p), a logarithmic increase with t_p is found in the second case. This points to the tunneling of carriers into so-called border traps

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(BTs) present in the a-Si:H layer.^{8,9,12} In this way, such border traps can also contribute to the interface recombination properties of c-Si/a-Si:H heterojunction solar cells.

EXPERIMENTAL DETAILS

In this work, starting substrates were mirror polished n-type and p-type Czochralski (CZ)-silicon, with resistivity in the range of 1–10 Ω cm for the boron doped (p-Si) and 1–5 Ω cm for the phosphorus doped (n-Si) cases. Wet chemical cleaning was performed ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$, 10 min), followed by a de-ionised water rinse. This was followed by an HF step (1%, 2 min) to ensure a hydrophobic surface, shortly before passivation layer processing, all performed in a cleanroom environment. The a-Si:H stacks examined were deposited in an Oxford Instruments parallel plate Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor, operating at 13.56 MHz. The deposition was performed at 1.7 Torr, with SiH_4 (25 sccm) and H_2 (75 sccm), at 45 mW/cm^2 power density. An *in situ* hydrogen plasma step was subsequently executed, to enhance the passivation of the intrinsic a-Si:H layer.¹³ PECVD processes were executed at $\sim 200^\circ\text{C}$.

Metallisation was performed by thermal evaporation of aluminium, using an Alcatel system at a deposition rate of ~ 60 nm/min. The maximum temperature the sample experienced was less than 100°C , as detected using temperature strips co-mounted in the process chamber. The thickness of the intrinsic a-Si:H layer was approximately 70 nm. The relative permittivity of the intrinsic a-Si:H layers examined lies in the range of 9–10, and the lower value than for c-Si (11.7) is consistent with the hydrogen incorporation in the layer. Although the intrinsic layer thickness is higher than that used in heterojunction devices,¹⁴ this value is used to prevent excessive conduction in the capacitance-measurements due to the band structure and low bandgap of the a-Si:H layer (1.75 eV, as determined by spectroscopic ellipsometry, compared to 9.0 eV for SiO_2).

High frequency CV analysis was performed on the a-Si:H samples, at temperatures from ~ 74 K to ~ 320 K; an

example is shown in Fig. 1 for an MIS capacitor on a p- and n-type c-Si substrate, where the aluminium contact is defined as the gate, as per Metal-Oxide-Semiconductor (MOS) technology nomenclature. The voltage required to attain flat band condition (flat-band voltage, or V_{fb}) can be instructive to evaluate the charge levels in the films, and was evaluated from the high frequency CV data, using the flat band capacitance method, as described in Ref. 15. Bulk and interface charge density estimation in the a-Si:H layers were derived from this V_{fb} value, using the methodology highlighted previously.⁵ The substrate doping density N_{dop} has been calculated from the CV in deep depletion, correcting for the insulator capacitance in accumulation. This gives typical values in the order of $1.7 \times 10^{15} \text{ cm}^{-3}$ (n-Si) and $4.5 \times 10^{15} \text{ cm}^{-3}$ (p-Si).

Capacitance DLTS has been performed using a Fourier-Transform-based digital system, with a capacitance bridge operated at a fixed frequency of 1 MHz. MIS capacitors with a diameter of 500 μm have been characterized by Current-Voltage (IV), CV, and DLTS. A bias pulse from depletion into accumulation was applied to the gate contact, while the c-Si substrate was grounded. Typical pulses are from +1 V to -1 V for the p-type and from -1 V to +1 V for the n-Si capacitors. The maximum accumulation voltage was limited by the high forward leakage current through the MIS structures. Samples were mounted in a liquid-nitrogen flow cryostat, enabling temperature (T) scan DLTS from about 75 K to slightly above room temperature (RT) (320 K). At the same time, isothermal frequency-dependent scans at a constant temperature have also been performed, whereby the sampling time constant (t_w) was varied in the range from 1 ms to 10 s. It corresponds approximately with the period between two consecutive bias pulses and determines the emission time constant (or rate window) as defined by Eq. (12) in Ref. 16. The trap filling was investigated by measuring the DLTS peak amplitude ($\sim \Delta C$) in function of the pulse duration t_p at RT.

RESULTS

Capacitance-voltage measurements were performed on the n- and p-Si samples, at temperatures in the range of 74 K and 320 K, and the results are shown in Fig. 1. The plots clearly demonstrate a negative V_{fb} shift (upon cooling) on p-Si substrates, and a positive V_{fb} shift (upon cooling) for n-Si substrates. These trends point towards the presence of donor traps in the lower region of the bandgap (i.e., from $E_{F \text{ p-Si @ 77K}}$ to $E_{F \text{ p-Si @ 320K}}$, with $E_{F \text{ p-Si}}$ the Fermi level at the interface at the respective temperatures in p-type Si), and acceptor traps in the upper half of the silicon bandgap (i.e., from $E_{F \text{ n-Si @ 77K}}$ to $E_{F \text{ n-Si @ 320K}}$, with $E_{F \text{ n-Si}}$ the Fermi level at the interface at the respective temperatures in n-type Si). Such a trend has previously been shown for the Si/SiO₂ interface and the interface defects responsible for this trend identified as P_{b0} silicon dangling bonds by Electron Spin Resonance (ESR).¹⁷

The data measured at 77 K at different frequencies f , on both n- and p-Si are shown in Fig. 2, while in this case a double CV sweep is presented, with the device biased from

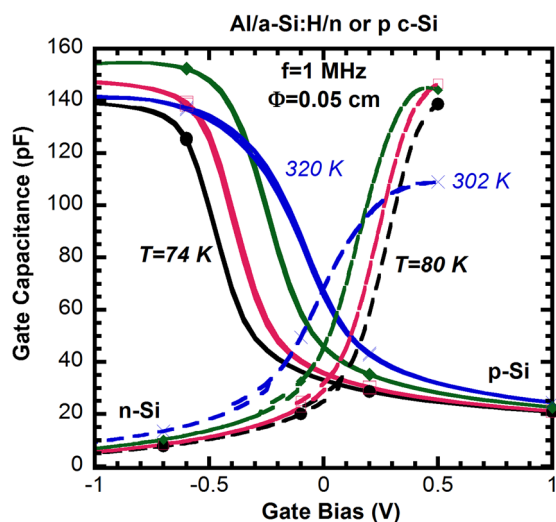


FIG. 1. CV characteristics at $f = 1$ MHz for MIS structures with a 70 nm a-Si:H insulator layer and an Al gate with a diameter of 500 μm . The temperature was varied from 74 K to 320 K (p-Si) and from 80 K to 302 K (n-Si).

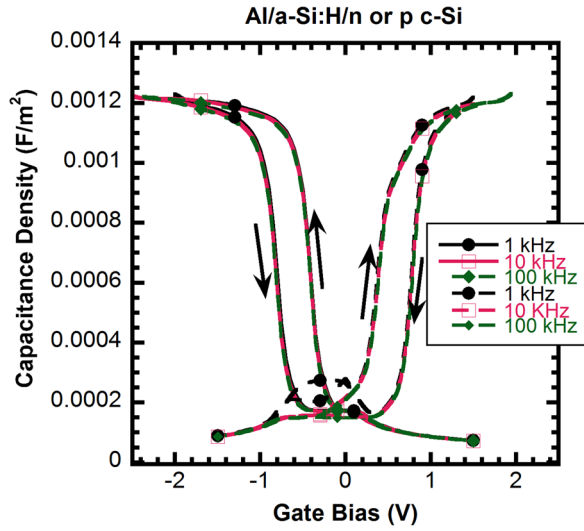


FIG. 2. High-frequency CV data, measured on Al/intrinsic a-Si:H/silicon at 77 K. Results are presented for both n-Si and p-Si substrates. Large hysteresis is observed when the bias is swept from accumulation to inversion and back, in both cases. This indicates a large defect density in the a-Si:H layers.

accumulation to depletion and back to accumulation. Immediately evident is the large hysteresis present in both cases, where the sweep from accumulation to inversion has ~ 400 mV lower (higher) flat band voltage for p-Si (n-Si). This trend has been demonstrated previously, on intrinsic/p⁺ a-Si:H samples, where it was attributed to defects in the intrinsic a-Si:H layers.⁴ This assertion can clearly be confirmed by these results, given there is no doped layer present in this case. The density of defects responsible for this feature is evaluated as $\sim 6 \times 10^{11} \text{ cm}^{-2}$, assuming a uniform defect distribution throughout the intrinsic a-Si layers with a volume density of $8.5 \times 10^{16} \text{ cm}^{-3}$ for both the n- and p-Si substrates. This uniform distribution has been derived previously from the variation in the magnitude of the hysteresis δV with the thickness of the intrinsic a-Si:H layer, using $D_t = C_{a\text{-Si:H}} \delta V / q$ (in cm^{-2}), with $C_{a\text{-Si:H}}$ the capacitance per unit of area of the a-Si:H layer and q the elementary charge.⁵ The density of states at the c-Si/a-Si:H interface is evaluated as $\sim 4 \times 10^{11} \text{ cm}^{-2}$. As specified in the Experimental Details section, and cited accordingly, the interface state density is calculated using the difference in flat-band voltage values on n-Si and p-Si substrates, measured at 77 K. This method has been previously published,⁵ and the equation is shown below. In both cases, the flat-band voltage value from the CV sweep biased from accumulation is used.

$$V_{fb\text{ n-Si}} - V_{fb\text{ p-Si}} = \frac{E_{f\text{ n-Si}}}{q} - \frac{E_{f\text{ p-Si}}}{q} + \frac{qN_{it}}{\epsilon_0\epsilon_r} T_{a\text{-Si:H}}, \quad (1)$$

where $V_{fb\text{ n-Si}}$ is the flat-band voltage of the sample on an n-Si substrate, $V_{fb\text{ p-Si}}$ is the flat-band voltage of the sample on a p-Si substrate, $E_{f\text{ n-Si}}$ is the Fermi level position in the n-Si substrate, $E_{f\text{ p-Si}}$ is the Fermi level position in the p-Si substrate at the measurement temperature, q is electronic charge, N_{it} is the interface state density between the Fermi level positions on p-Si and n-Si, respectively, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the intrinsic

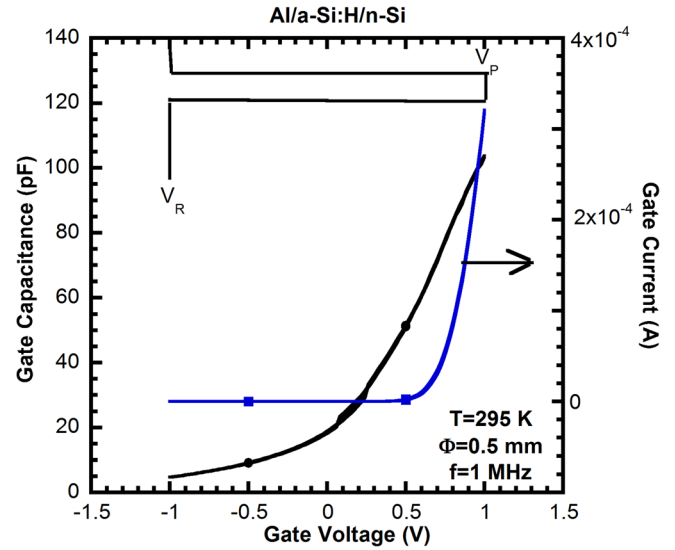


FIG. 3. CV and IV characteristic of an Al/a-Si:H/n-Si MIS structure with diameter $\Phi = 500 \mu\text{m}$ at 295 K. The capacitance measurement frequency is 1 MHz. Also indicated is the bias pulse applied periodically during DLTS.

a-Si:H layer, and $T_{a\text{-Si:H}}$ is the thickness of the intrinsic a-Si:H layers (on both n-Si and p-Si substrates).

In Fig. 3, the IV and 1-MHz CV characteristics at RT of an n-Si MIS capacitor are shown, together with the applied bias pulse during DLTS from the quiescent reverse bias (V_R) to the pulse bias (V_P). In principle, both traps in the c-Si depletion region, at the a-Si:H/c-Si interface and BT in the dielectric can be filled during this pulse. As shown in the isothermal spectrum of Fig. 4, a broad peak is observed at 295 K for a pulse from -1 V to $+1$ V, while at the same time, for a pulse limited to the silicon depletion region from -1 V to 0 V, a negligible signal is observed, indicating no deep levels in the n-Si substrate above the DLTS detection limit of about $10^{-4} \times N_{\text{dop}}$, i.e., above a few 10^{11} cm^{-3} . This implies that the deep levels are present either at the interface or in the undoped a-Si:H.⁶ At the same time, there is no

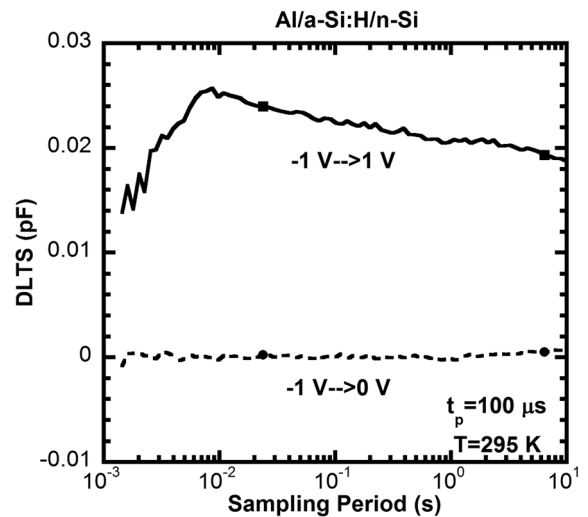


FIG. 4. Isothermal frequency scan at room temperature of a $500 \mu\text{m}$ diameter Al/a-Si:H/n-Si MIS capacitor pulsed from depletion towards accumulation, from $-1 \text{ V} \rightarrow 0 \text{ V}$ and from $-1 \text{ V} \rightarrow 1 \text{ V}$. The pulse duration $t_p = 100 \mu\text{s}$.

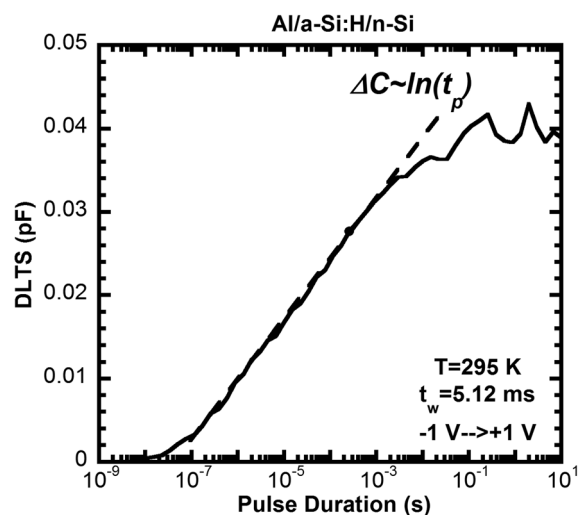


FIG. 5. DLTS amplitude versus pulse duration for a pulse from -1 V to $+1$ V for a $500\text{ }\mu\text{m}$ diameter Al/a-Si:H/n-Si MIS capacitor at 295 K. A sampling period of 5.12 ms has been employed. The amplitude increases with $\ln(t_p)$ over several decades.

evidence of a so-called minority carrier inversion response of the capacitance to the bias pulse,^{18,19} so that we can safely rule out this possible cause for the DLTS peaks.

The trap filling curve of Fig. 5 is instructive for the nature of the deep levels observed in the RT spectrum of Fig. 4. It is found that for t_p between 100 ns and 0.01 s, the DLTS amplitude increases proportional with $\ln(t_p)$. In the case of a MIS capacitor, this points to majority carriers which tunnel into traps in the dielectric, whereby the tunneling depth d increases with $\ln(t_p)$.^{8,9,12} This explains the increase of the DLTS amplitude (ΔC) with t_p : as the number of filled traps during the bias pulse increases with the tunneling distance in the a-Si:H (i.e., proportionally with $\ln(t_p) \sim d$), the capacitance transient will be generated through thermal emission of the carriers from a higher surface density of traps, given by $d \times N_t$ (in cm^{-2}), with N_t the trap concentration in a-Si:H (in cm^{-3}). The fact that a linear relationship is found over more than five decades confirms a rather uniform trap concentration N_t over the tunneling distance probed by the carriers. The reason for the apparent saturation of the DLTS signal beyond 0.01 s in Fig. 5 is in the first instance related with the re-emission of carriers from the traps in the a-Si:H to the c-Si substrate during the trap filling,⁹ since the electron barrier between a-Si:H and c-Si is rather low.^{20,21} The electron emission time constant corresponding with Fig. 5 is $\tau_n \sim 2.5$ ms, which corresponds approximately with the t_p where the DLTS signal starts to saturate. In the event of significant re-emission, only a fraction $1/[1 + e_{nt_p}]$ of the traps will become filled at the tunneling depth defined by t_p , so that for a sufficiently long pulse, no additional traps in the a-Si:H layer will become filled during the pulse, leading to a saturation of the DLTS amplitude.

Finally, Fig. 6 represents typical DLT-spectra for an n-Si MIS capacitor between 75 K and 320 K, for different filling pulse durations. Again, one can derive from the -1 V to 0 V spectrum that the depletion region in the c-Si substrate is free from deep levels within the detection limit of the technique. This indicates good quality defect-free silicon, a requirement for devices with high open circuit voltage/

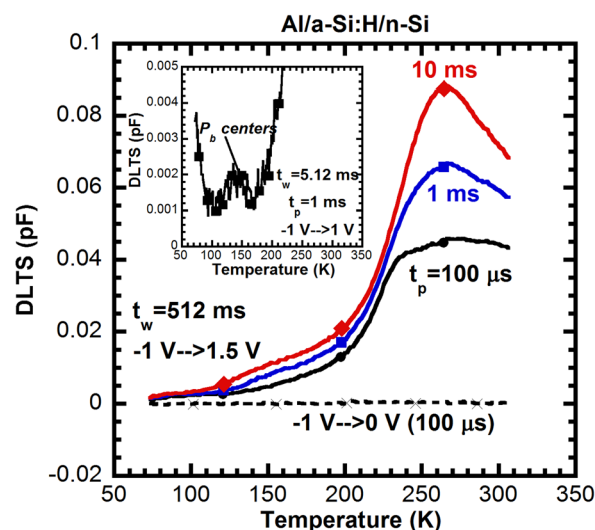


FIG. 6. T-scan DLT-spectra at $t_w = 512$ ms for an Al/a-Si:H/n-Si MIS capacitor at different pulse durations and for a pulse from -1 V to -1.5 V. The flat line for the -1 V \rightarrow 0 V pulse indicates that there are no deep levels in the n-type c-Si substrate within the detection limit. The inset shows a blow up of the P_b interface state peak at about 130 K, showing no dependence of the amplitude with the pulse duration.

efficiency. Also, no inversion response of the MIS capacitor is found in the temperature range studied.

For the -1 V to 1.5 V spectra, a clear peak with maximum at 260 K and a tail extending to lower temperatures is found, whereby the amplitude increases with t_p . This can be compared with the broad feature in Fig. 4, showing the same peak at room temperature and as a function of the sampling time, extending the range to longer emission time constants beyond the fixed value of 222 ms of Fig. 6, which is approximately $t_w/2$.¹⁶ In some measurement conditions, a smaller peak around 130 K, shown in the inset of Fig. 6, can be clearly distinguished. Its DLTS peak width is more typical for a point defect, compared with the broad feature of the dominant signal. Moreover, the amplitude does not change by varying the pulse duration between 100 μs and 10 ms, indicating complete trap filling below 100 μs pulse duration. Its different appearance and response to t_p indicates that a second type of defects is observed in the n-Si MIS capacitors; moreover, they are absent in the -1 V \rightarrow 0 V spectrum of Fig. 6, so that it strongly suggests the presence of a deep level at the a-Si:H/n-Si interface.⁶

Quite symmetric behavior is observed for the p-Si counterparts. As can be seen from Fig. 7, the 1-MHz capacitance in accumulation suffers from the high forward conduction, consistent with the low barrier heights at the c-Si/a-Si:H interface. Again, a rather broad peak is found at RT in the isothermal spectrum of Fig. 8 for a pulse from $+1$ V to -1 V, while the silicon depletion region is free from deep levels, according to the $+1$ V \rightarrow 0 V trace. The filling kinetics follows an $\ln(t_p)$ law over at least three decades, followed by a saturation of the DLTS amplitude (Fig. 9), analogue as for the n-Si case. Besides the impact of the re-emission of holes from the traps in the a-Si to the c-Si substrate, the high electron leakage current injected from the negatively biased Al gate during the voltage pulse in p-Si

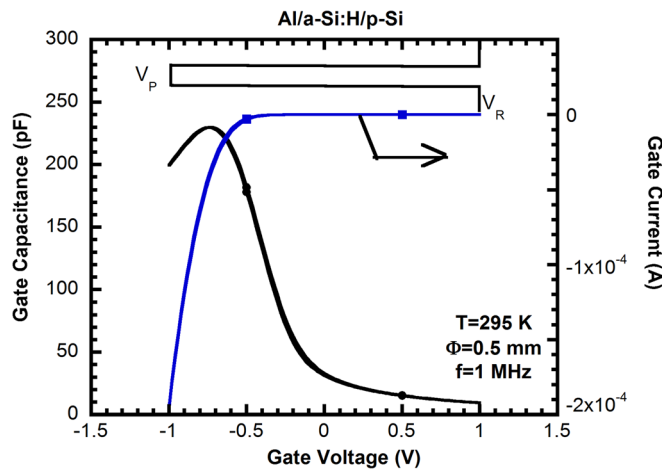


FIG. 7. CV and IV characteristic of an Al/a-Si:H/p-Si MIS structure with diameter $\Phi = 500 \mu\text{m}$ at 295 K. The capacitance measurement frequency is 1 MHz. Also indicated is the bias pulse applied periodically during DLTS.

capacitors also contributes to the saturation of the DLTS amplitude. These electrons can recombine with trapped holes in the deep-level centers during the pulse, reducing therefore the density of filled traps according to the ratio of $n\sigma_n/p\sigma_p$. It may explain the lower trap density found in the p-type samples compared with the n-Si counterparts, as reported below.

Comparing the peak amplitudes in Figs. 5 and 9 indicates similar trap concentrations for both n- and p-type samples (to within 20%). Figure 10 represents the DLT-spectra for different pulse lengths, showing a broad peak at about 300 K, which increases with t_p in the range investigated. Judging from the $+1 \text{ V} \rightarrow 0 \text{ V}$ spectrum, no deep levels are observed in the silicon depletion region from 75 K up to 320 K. Finally, the activation energy E_t and electron (σ_n) and hole (σ_p) capture cross section obtained from an Arrhenius plot in the peak maxima of Figs. 6 (n-Si) and 10 (p-Si) are represented in Table I, revealing around silicon midgap position in both cases and about 50 times higher hole versus electron capture cross section.

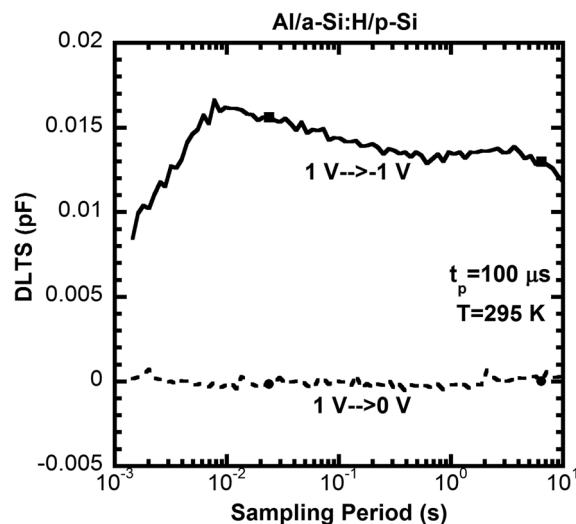


FIG. 8. Isothermal frequency scan at room temperature of a $500 \mu\text{m}$ diameter Al/a-Si:H/p-Si MIS capacitor pulsed from depletion towards accumulation, from $+1 \text{ V} \rightarrow 0 \text{ V}$ and from $+1 \text{ V} \rightarrow -1 \text{ V}$. The pulse duration $t_p = 100 \mu\text{s}$.

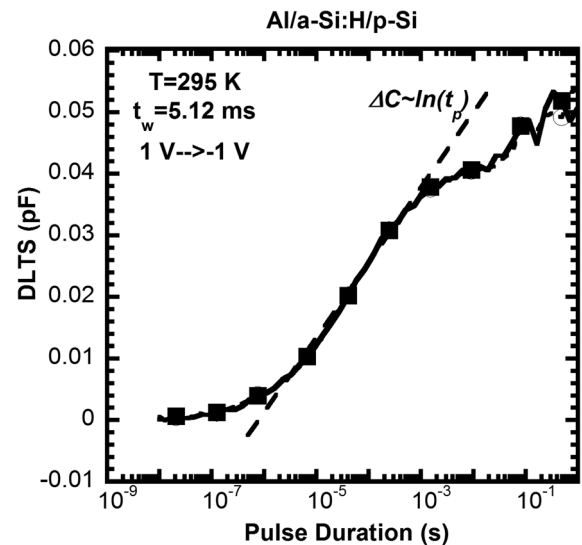


FIG. 9. DLTS amplitude versus pulse duration for a pulse from $+1 \text{ V}$ to -1 V for a $500 \mu\text{m}$ diameter Al/a-Si:H/p-Si MIS capacitor at 295 K. A sampling period of 5.12 ms has been employed. The amplitude increases with $\ln(t_p)$ over several decades, as indicated by the dashed line.

DISCUSSION

The foregoing results can be summarized as follows: in a-Si:H MIS capacitors on p- and n-type c-Si, a broad peak is observed with position around the silicon midgap (Table I). The peak amplitude (or equivalent, the trap concentration) evolves over at least three decades proportional with $\ln(t_p)$, which is interpreted as resulting from a separation between the traps in the dielectric and the free carriers at the interface. Therefore, carrier capture is believed to occur through tunneling. In the case of purely elastic tunneling, the capture time can be written as¹²

$$t_p = \tau_0 \exp(\alpha_t d), \quad (2)$$

with τ_0 the capture time at the interface ($d = 0$) and α_t the tunneling parameter, defined by

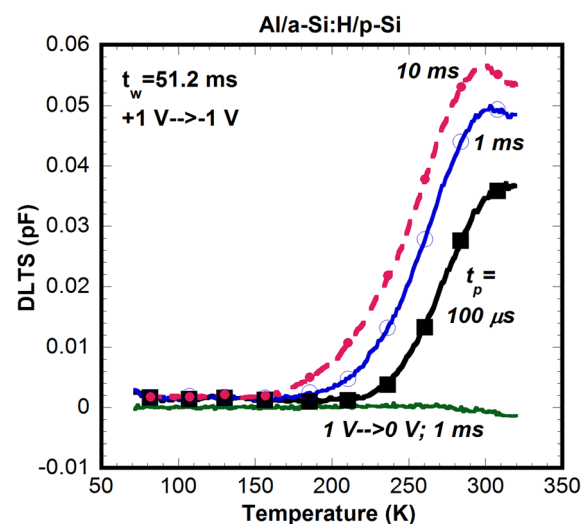


FIG. 10. T-scan DLT-spectra at $t_w = 51.2 \text{ ms}$ for an Al/a-Si/p-Si MIS capacitor at different pulse durations and for a pulse from $+1 \text{ V}$ to -1 V . The flat line for the $+1 \text{ V} \rightarrow 0 \text{ V}$ pulse indicates that there are no deep levels in the n-type c-Si substrate within the detection limit.

TABLE I. Deep level parameters derived from an Arrhenius analysis of the DLT-spectra of Figs. 6 and 10 and from the density-of-states graphs of Fig. 11, where E_t is the trap activation energy, σ_n and σ_p the capture cross section for electrons and holes, respectively. D_t is the bulk trap density and D_{it} is the interface trap density.

c-Si	E_t (eV)	σ_n or σ_p (cm ²)	D_t (cm ⁻²)	D_{it} (cm ⁻²)
n-Si	0.560	5.6×10^{-16}	3.8×10^{11}	1.1×10^{11}
p-Si	0.660	3.2×10^{-14}	4.2×10^{11}	1.6×10^{10}

$$\alpha_t = \frac{2}{\hbar} \sqrt{2q m_{a-Si} \Phi_{it}}. \quad (3)$$

In Eq. (3), q is the elementary charge, \hbar the reduced constant of Planck, m_{a-Si} the tunneling effective mass in the a-Si:H, and Φ_{it} the potential barrier for tunneling. Filling in realistic values for the parameters in Eqs. (2) and (3) results in an estimated tunneling distance of about 4.5 nm (p-Si) to 6.4 nm (n-Si), corresponding with a filling time t_p of 10 ms. This is in line with other estimates in the literature.²² The difference in tunneling distance between n- and p-Si is in the first instance related with the different barrier height at the a-Si:H/c-Si interface, being smaller for n-type substrates. Note, however, that these estimates are to be considered upper limits for the tunneling depth, neglecting possible multi-phonon relaxation upon capture and, thus, the occurrence of capture by inelastic tunneling.²³

In order to quantify the equivalent surface trap density (D_t), the N_t in the a-Si:H is considered uniform (as shown by the CV hysteresis analysis) and it is furthermore assumed that the DLTS signal increases proportionally with the tunneling depth, so that $D_t = N_t \times d$ cm⁻². On the other hand, the surface DOS in a MIS capacitor can be derived from^{5,22}

$$D_{t,ins} = \frac{\varepsilon_{Si} A C_{ins} N_{dop} \Delta C}{\beta k T C_R^3} \text{ (in cm}^{-2} \text{ eV}^{-1} \text{)}. \quad (4)$$

In Eq. (4), ε_{Si} is the permittivity of silicon $\sim 10^{-12}$ F/cm, A the area of the capacitor, C_{ins} the a-Si:H capacitance (in F), N_{dop} is 4.5×10^{15} cm⁻³ (p), and 1.7×10^{15} cm⁻³ (n). Finally, β is a semi-empirical peak width factor, estimated 2.5 from the Full Width at Half Maximum of the theoretical b1 Fourier-transform DLTS signal¹⁶ and k is Boltzmann's constant. C_R is the quiescent capacitance at V_R and ΔC is the capacitance transient amplitude, which is proportional with the vertical axis in Figs. 6 and 10.

To convert the T-axis into an activation energy, use is made of²⁴

$$E_t = E_{V,Si} + kT \ln(\sigma_p \times 3.33 \times 10^{21} T^2 \tau_0) \text{ (p-Si)}, \quad (5a)$$

$$E_t = E_{C,Si} - kT \ln(\sigma_n \times 8.23 \times 10^{21} T^2 \tau_0) \text{ (n-Si)}, \quad (5b)$$

with τ_0 the emission time constant and σ_n , σ_p reported in Table I. $E_{V,Si}$ and $E_{C,Si}$ are the valence band maximum and the conduction band minimum in silicon, respectively. To refer the activation energy in the case of n-Si to the valence band maximum, the activation energies obtained from Eq. (5b) are subtracted from the temperature dependent bandgap $E_{G,Si}$, calculated from^{25,26}

$$E_{G,Si}(T) = 1.17 - \frac{4.73 \times 10^{-4} \times T^2}{T + 636} \text{ (in eV)}. \quad (6)$$

The resulting DOS (or $D_{t,ins}$) versus activation energy for an n- and p-type c-Si MIS capacitor is shown in Fig. 11. The surface densities (D_t and D_{it}) corresponding with the different peaks are summarized in Table I and are obtained by integrating the area under the DOS peaks. It can be observed that the dominant peak in both types of samples occurs at approximately the same position in the silicon bandgap, with a similar DOS, indicating that capture and emission to the same band of defects in the a-Si:H is likely to happen in both cases. The respective peak positions correspond with the activation energies mentioned in Table I, derived from an Arrhenius plot in the peak maximum. It is clear from Fig. 11 that the energy range of the DOS depends on the value for the capture cross section, used to convert the temperature into an activation energy axis, based on Eq. (5). This can be derived from the second p-Si peak in Fig. 11, which has been calculated assuming a hole capture cross section equal to the σ_n value in Table I and showing an energy shift of the DOS by about 0.1 eV to lower values. In fact, it is likely that the capture cross section depends on the activation energy and moreover, is thermally activated (inelastic tunneling), which will change slightly the shape of the DOS in Fig. 11. Nevertheless, a good agreement has been obtained between the D_t derived from DLTS in Table I and the data extracted from the hysteresis in the CV curves mentioned before, where values of 6×10^{11} cm⁻² were calculated on both n- and p-type Si substrates.

When comparing the D_t and D_{it} data in Table I, it is obvious that the D_{it} in n-Si is about ten times higher than in p-Si. This is related to the fact that the total area under the feature indicated as $P_{b0}^{0/-}$ in Fig. 11 has been used to derive the D_{it} , which also contains a contribution of the broad D center peak. The D_{it} in p-Si suffers less from this and shows a value which is typical for a well-passivated Si surface. Overall, the global density $D_t + D_{it}$ is within 10% the same

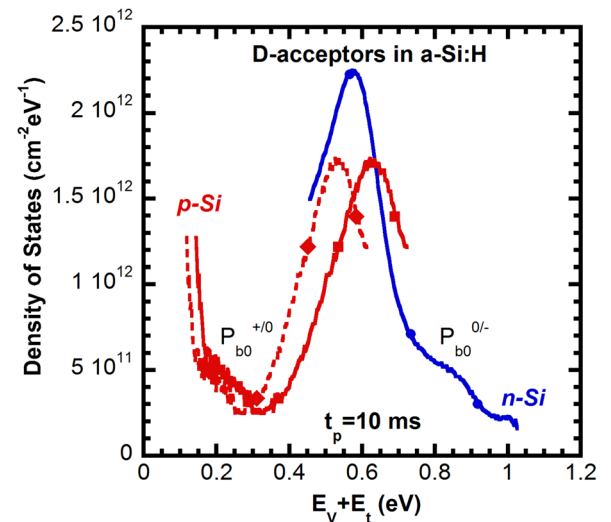


FIG. 11. Density of states versus energy of the deep levels derived from the n- and p-Si spectra at $t_p = 10$ ms of Figs. 6 and 10, respectively. The dashed curve has been calculated, assuming $\sigma_p = \sigma_n = 5.6 \times 10^{-16}$ cm².

for n- and p-Si, which is within the estimated error bar of 20% for the trap densities.

In Fig. 11, the main peak has been ascribed to the dangling bond (D) centers in the a-Si:H, which can communicate with the carriers in the c-Si substrate and, hence, have an impact on the recombination lifetime, as suggested before.^{20,22} From the fact that the hole capture cross section is much larger than σ_n —and assuming that they belong to the same defects—it can be derived that the trap levels have an acceptor character. It has been shown before that the D centers in a-Si:H exhibit two near mid-gap-bands of states in DLTS,^{10,11,27–31} with an amphoteric character: a donor band and an acceptor band separated by a positive correlation energy U .^{32–35} Given the band alignment of a-Si:H with respect to c-Si,^{20,21} the peak observed here could correspond with the $E_{C,a-Si}-0.83$ eV acceptor state of the D defects.³⁶ On the other hand, Temperature Stimulated Capacitance (TSCAP) measurements revealed a DOS peaking at ~ 0.8 to 0.9 eV from $E_{V,a-Si}$,³⁷ which is close to the peak position observed here, when account is made for the ~ 0.4 eV valence band offset between c-Si and a-Si:H.

A question which remains to be answered is where are the donor states corresponding with the D defects and causing the negative flat-band shift and hysteresis in the CV characteristics of p-Si capacitors? Considering a positive U shift between the donor and the acceptor states would place the corresponding DLTS peak in the bottom half of the c-Si bandgap, close to the valence band. According to Fig. 11, the DOS increases dramatically below $E_V + 0.2$ eV, which could correspond with the onset of the donor band of the D defects. However, measurements below liquid nitrogen temperature are required to more firmly support this assumption.

The rather large hole capture cross section is in line with recent estimates for σ_p^- used in the recombination modelling at the a-Si:H/c-Si interface,³⁵ so that the hole capture in p-Si substrates most likely occurs through the acceptor states. The electron capture cross section in Table I is between the values assumed for $\sigma_n^0 \sim 5 \times 10^{-18} \text{ cm}^2$ and $\sigma_n^+ \sim 2.5 \times 10^{-15} \text{ cm}^2$.³⁵ The electron cross section value found here is higher than the range of data reported in the literature and derived from space-charge-limited conduction.³⁸ Of course, values for the capture cross sections derived from the intercept of an Arrhenius plot have a large error bar and yield an order of magnitude estimate. A direct measurement of σ_n/σ_p as a function of the filling pulse duration at a fixed temperature provides normally more accurate data, but is not straightforward in this case, given the non-standard logarithmic trap filling kinetics in Figs. 5 and 9. In fact, also direct capture cross section measurements on a-Si by DLTS have proven to be difficult, given the complex trap filling kinetics observed.²⁵ However, considering the activation energy in Table I and the conduction band offset, it is reasonable to assume that electron capture in the n-type samples is also dominated by the acceptor states of the D defects in a-Si:H, consistent with the positive flat band voltage shift observed on n-Si, shown in Fig. 3. Finally, it has been reported that the electron capture cross section was found relatively T-independent from $E_{C,a-Si}-0.78$ eV to $E_{C,a-Si}-0.89$ eV,³⁰ justifying to some extent the use of a constant σ_n value in the

conversion of the T-axis into an activation energy for the n-Si data.

The two minor features in Fig. 11 have been assigned to the donor (p-Si) and acceptor (n-Si) level of the P_{b0} centers at the a-Si:H/(100)c-Si interface; the corresponding integrated surface density is given in Table I. The presence of P_{b0} centers at the heterojunction interface has been well-established by ESR³⁹ and has also been observed on similar samples as the ones studied here.⁵ In addition, the smaller features around 130 K behave more like point defects with a saturation of the peak amplitude in function of the pulse duration (see inset of Fig. 6). While it is difficult to derive an Arrhenius plot for the small DLTS peak, its temperature position matches closely the literature data for the P_{b0} acceptors.^{24,40–45}

While it has been shown before that also deep levels in the a-Si:H adjacent to the interface with c-Si contribute to its surface recombination properties,^{5,39} DLTS on MIS capacitors confirms this in a more direct and straightforward manner and allows a separation of the two contributions. It also provides a time scale for the capture and emission of majority carriers from the silicon substrate and demonstrates that the near midgap D defects in the first 5 to 10 nm from the interface act as active traps (recombination centers), with time constants up to a few ms. The centers further from the interface respond with longer time constants, which is obvious in the hysteresis of the CV curves at 77 K.

CONCLUSIONS

DLTS analysis of MIS capacitors with a-Si:H as a gate dielectric has shown the presence of two types of deep levels, affecting the electrical properties of the interface. They have been correlated with the P_{b0} dangling bond states, giving rise to acceptor (n-type) and donor levels (p-type) in the upper and lower half of the silicon bandgap and, second, the dangling bond related D acceptor defects in a-Si:H, resulting in a near silicon midgap band of states. In the latter case, carrier capture occurs by tunneling through the potential barrier at the interface up to distances of 5 to 10 nm in the amorphous silicon. The density of states derived from the DLTS peak is in good agreement with values derived from the hysteresis in low-frequency CV measurements.

¹S. De Wolf, A. Descoedres, Z. C. Holman, and C. Ballif, *Green* **2**, 7 (2012).

²P. J. Cousins, D. D. Smith, H.-C. Luan, J. Manning, T. D. Dennis, A. Waldhauer, K. E. Wilson, G. Harley, and W. P. Mulligan, in *Proceedings of the 35th IEEE Photovoltaic Specialists Conference (PVSC)*, Honolulu, Hawaii (2010), p. 275.

³M. A. Green, *Silicon Solar Cells Advanced Principles & Practice* (Centre for Photovoltaic Devices & Systems, 1995), p. 123.

⁴See <http://panasonic.co.jp/corp/news/official.data/data.dir/2014/04/en140410-4/en140410-4.html> for Panasonic press release, April 2014.

⁵N. H. Thoan, M. Jivanescu, B. J. O'Sullivan, L. Pantisano, I. Gordon, V. V. Afanas'ev, and A. Stesmans, *Appl. Phys. Lett.* **100**, 142101 (2012).

⁶K. Yamasaki, M. Yoshida, and T. Sugano, *Jpn. J. Appl. Phys., Part 1* **18**, 113 (1979).

⁷N. M. Johnson, *J. Vac. Sci. Technol.* **21**, 303 (1982).

⁸D. Vuillaume, J. C. Bourgoin, and M. Lannoo, *Phys. Rev. B* **34**, 1171 (1986).

⁹H. Lakhdari, D. Vuillaume, and J. C. Bourgoin, *Phys. Rev. B* **38**, 13124 (1988).

¹⁰I. Thurzo, S. Teramura, R. Durny, V. Nádaždy, M. Kumeda, and T. Shimizu, *J. Appl. Phys.* **82**, 4372 (1997).

- ¹¹I. Thurzo, V. Nádaždy, S. Teramura, R. Durny, M. Kumeda, and T. Shimizu, *J. Appl. Phys.* **84**, 6906 (1998).
- ¹²E. Simoen, H.-C. Lin, A. Alian, G. Brammertz, C. Merckling, J. Mitard, and C. Claeys, *IEEE Trans. Device Mater. Reliab.* **13**, 444 (2013).
- ¹³M. Mews, T. F. Schulze, N. Mingirulli, and L. Korte, *Appl. Phys. Lett.* **102**, 122106 (2013).
- ¹⁴S. De Wolf, S. Olibet, and C. Ballif, *Appl. Phys. Lett.* **93**, 032101 (2008).
- ¹⁵E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley & Sons, 1982), p. 487.
- ¹⁶S. Weiss and R. Kassing, *Solid-State Electron.* **31**, 1733 (1988).
- ¹⁷N. H. Thoan, K. Keunen, V. V. Afasas'ev, and A. Stesmans, *J. Appl. Phys.* **109**, 013710 (2011).
- ¹⁸N. O. Pearce, B. Hamilton, A. R. Peaker, and R. A. Craven, *J. Appl. Phys.* **62**, 576 (1987).
- ¹⁹S. N. Volkos, E. S. Efthymiou, S. Bernardini, I. D. Hawkins, A. R. Peaker, and G. Petkos, *J. Appl. Phys.* **100**, 124103 (2006).
- ²⁰T. F. Schulze, C. Leendertz, N. Mingirulli, L. Korte, and B. Rech, *Energy Proc.* **8**, 282 (2011).
- ²¹C.-L. Zhong, R.-H. Yao, and K.-W. Geng, *IEEE Trans. Electron Devices* **61**, 394 (2014).
- ²²S. De Wolf, C. Ballif, and M. Kondo, *Phys. Rev. B* **85**, 113302 (2012).
- ²³E. Simoen, J. W. Lee, and C. Claeys, *IEEE Trans. Electron Devices* **61**, 634 (2014).
- ²⁴E. Simoen, C. Gong, N. E. Posthuma, E. Van Kerschaver, J. Poortmans, and R. Mertens, *J. Electrochem. Soc.* **158**, H612 (2011).
- ²⁵C. D. Thurmond, *J. Electrochem. Soc.* **122**, 1133 (1975).
- ²⁶R. Couderc, M. Amara, and M. Lemiti, *J. Appl. Phys.* **115**, 093705 (2014).
- ²⁷R. S. Crandall, *J. Electron. Mater.* **9**, 713 (1980).
- ²⁸R. S. Crandall, *Phys. Rev. B* **24**, 7457 (1981).
- ²⁹J. D. Cohen, J. P. Harbison, and K. W. Wecht, *Phys. Rev. Lett.* **48**, 109 (1982).
- ³⁰D. V. Lang, J. D. Cohen, and J. P. Harbison, *Phys. Rev. B* **25**, 5285 (1982).
- ³¹N. M. Johnson and D. K. Biegelsen, *Phys. Rev. B* **31**, 4066 (1985).
- ³²R. A. Street, J. Zesch, and M. J. Thompson, *Appl. Phys. Lett.* **43**, 672 (1983).
- ³³F. Vaillant and D. Jousse, *Phys. Rev. B* **34**, 4088 (1986).
- ³⁴J. Hubin, A. V. Shah, E. Sauvain, and P. Pipoz, *J. Appl. Phys.* **78**, 6050 (1995).
- ³⁵S. Olibet, E. Vallat-Sauvain, and C. Ballif, *Phys. Rev. B* **76**, 035326 (2007).
- ³⁶H. Kida, K. Hattori, H. Okamoto, and Y. Hamakawa, *J. Appl. Phys.* **59**, 4079 (1986).
- ³⁷J. Beichler, H. Mell, and K. Weber, *J. Non-Cryst. Solids* **59–60**, 257 (1983).
- ³⁸R. Meaudre and M. Meaudre, *Appl. Phys. Lett.* **85**, 245 (2004).
- ³⁹B. M. George, J. Behrends, A. Schnegg, T. F. Schulze, M. Fehr, L. Korte, B. Rech, K. Lips, M. Rohrmüller, E. Rauls, W. G. Schmidt, and U. Gerstmann, *Phys. Rev. Lett.* **110**, 136803 (2013).
- ⁴⁰E. H. Poindexter, G. J. Gerardi, M.-E. Rueckel, P. J. Caplan, N. M. Johnson, and D. K. Biegelsen, *J. Appl. Phys.* **56**, 2844 (1984).
- ⁴¹D. Vuillaume and J.-C. Bourgoin, *J. Appl. Phys.* **58**, 2077 (1985).
- ⁴²H. G. Grimmeiss, W. R. Buchwald, E. H. Poindexter, P. J. Caplan, M. Harmatz, G. J. Gerardi, D. J. Keeble, and N. M. Johnson, *Phys. Rev. B* **39**, 5175 (1989).
- ⁴³D. Vuillaume, D. Goguenheim, and G. Vincent, *Appl. Phys. Lett.* **57**, 1206 (1990).
- ⁴⁴R. Beyer, H. Burgardt, I. Thurzo, D. R. T. Zahn, and T. Geßner, *Solid-State Electron.* **44**, 1463 (2000).
- ⁴⁵L. Dobaczewski, S. Bernardini, P. Kruszewski, P. K. Hurley, V. P. Markevich, I. D. Hawkins, and A. R. Peaker, *Appl. Phys. Lett.* **92**, 242104 (2008).