Space charge limited current in 4H-SiC Schottky diodes in the presence of stacking faults

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ABSTRACT

The presence of crystallographic defects can induce notable effects on the mechanisms ruling the current transport in metal/semiconductor contacts. In this context, in this Letter, the impact of stacking faults (SFs) on the characteristics of 4H-SiC Schottky diodes was investigated under both forward and reverse bias. In particular, in the presence of SFs under the contact, while no significant effect on the ideality factor and barrier height was observed under forward bias, an anomalous increase in the leakage current occurred under reverse bias. The observed behavior of the leakage current could be explained by a space-charge limited current model, consistent with the presence of a distribution of trapping states in the gap of 4H-SiC. An increase in the reverse bias above 30 V leads to a complete trap filling. The weak temperature-dependence of the leakage current observed in this regime suggests the coexistence with a tunneling of the carriers through the barrier. The results can be useful to understand unexpected failures in 4H-SiC Schottky diodes.

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Nowadays, the hexagonal polytype of silicon carbide (4H-SiC) has become a material of choice for the development of more efficient devices in power electronics.[1,2] In fact, the outstanding physical properties of 4H-SiC,[3] such as a wide bandgap (3.26 eV), a high critical electric field (2 MV/cm), and a saturated drift velocity ($> 2 \times 10^7$ cm/s), allow us to achieve low values of on-state voltage, high values of breakdown voltage and switching speed, and, hence, better performances than Si devices.

In this context, today, 4H-SiC Schottky barrier diodes (SBDs) are used in several applications. The high performances and reliability of these devices benefit from the good crystalline quality of the available material, as well as from the maturity level reached by the device processing.[4–6] However, the mechanisms governing the current transport through the core of the device, i.e., the Schottky barrier, are continuously the subject of investigation, as any deviation from ideal behavior can be a signature of the presence of defects generated during either material growth or device fabrication.

Among the crystallographic defects, stacking faults (SFs) can be created, e.g., in 4H-SiC p–n junctions during forward bias stress,[7] under high temperature operation[8] or electron-beam irradiation.[9] While the effects of SFs on the electrical behavior of p–n junctions have extensively been investigated in 4H-SiC,[10] less work has been done in the case of unipolar devices like SBDs.[11,12] In this regard, it has been demonstrated that the presence of very few SFs in 4H-SiC epilayers can cause an increase in the reverse leakage current in Schottky diodes.[11,12] On the other hand, in forward bias, only a small reduction in the Schottky barrier height was observed even in the presence of a significant amount of SFs under the anode of SDBs.[11] In other cases, when a relevant reduction in the Schottky barrier (0.25 eV) was observed under forward bias, the behavior of the reverse leakage current remained unclear.[13,14] Clearly, the impact of SFs on the electrical current transport mechanisms in 4H-SiC Schottky diodes deserves further quantitative investigation. In particular, a physical model explaining the increase in the reverse leakage current and its temperature behavior was not proposed in the previous studies.

In this Letter, the impact of the SFs on the electrical behavior of 4H-SiC Schottky diodes was studied by cross-correlating micro-photoluminescence (μ-PL) and scanning capacitance microscopy (SCM) measurements, with the temperature-dependent electrical characteristics of Schottky diodes. The anomalous increase in the reverse leakage current in the diode characteristic was associated with the presence of SFs in the contact area. For this system, we have studied the current transport mechanisms by temperature dependent measurements, observing that in the presence of stacking faults the leakage current can be explained by a space-charge limited current (SCLC) model.

The samples used in this study were $2 \times 2\,cm^2$ pieces, cut out from a 200 mm 4H-SiC(0001) commercial wafer. The wafer consisted of a 6.5 μm-thick epitaxial layer with an n-type nitrogen doping level of $1.0 \times 10^{16}\,cm^{-3}$, grown onto a heavily doped substrate. The sample surface was first prepared by a piranha etch followed by a diluted HF etch. On this material, Schottky diodes were fabricated, consisting of a large-area back-side nickel silicide Ohmic contact[15] and circular tungsten (W) Schottky contacts with a diameter of 300 μm on the front side. The schematic cross section of the fabricated diodes is depicted as inset in Fig. 1(a). The Schottky contacts were defined by optical lithography and lift-off processes and then thermally annealed at 700 °C for 10 min in N_2 atmosphere.[16] The electrical properties of the diodes were characterized by current–voltage (I–V) measurements, under both forward and reverse bias, carried out in a Karl-Suss MicroTec probe station equipped with a parameter analyzer. The I–V measurements were acquired also in the temperature range of 25–150 °C, to get insight into the carrier transport mechanisms. The material quality was monitored by μ-PL measurements, performed with a Horiba Jobin Yvon HR800 spectrometer under an excitation line at 325 nm (He–Cd laser), with the aim to detect the presence of extended defects close to the surface. A nanometric scale morphological and electrical analysis of the epilayer surface was performed by atomic force microscopy (AFM) and in-plan scanning capacitance microscopy (SCM) measurements, using a Digital Instrument D3100 equipped with a Nanoscope V controller.[17]

First, we investigated the electrical characteristics of the fabricated W/4H-SiC Schottky contacts in two pieces cut out from different regions of the 4H-SiC sample, one in the center and the other in a lateral region at around 65 mm from the center, labeled region A and region B, respectively. This electrical characterization revealed the occurrence of a different behavior of the diodes fabricated on the two regions. In particular, Fig. 1 reports, in a semilog plot, the devices forward current density–voltage (J–V) characteristics taken in region A and in region B.

As can be seen in Fig. 1(a), the contacts featured similar forward J–V characteristics. The linear region of the semilog plot was analyzed according to the thermionic emission (TE) theory,[18] deriving the relevant electrical parameters, i.e., the Schottky barrier height (Φ_B) and the ideality factor (n).

In particular, by performing a fit of the linear region of the forward J–V curves collected on 10 diodes for each sample, the same

values of barrier height and ideality factor were obtained for both contacts, i.e., $\phi_B = 1.24 \pm 0.03\,eV$ and n = 1.09 ± 0.03. These electrical parameters exhibited a temperature-dependence that can be explained by a local inhomogeneity of the barrier at a nanometric scale, as described by the Tung's model (Fig. S1 in the supplementary material).[19] Instead, a significant difference in the contacts behavior was observed under reverse bias [Fig. 1(b)], with an anomalous increase in the leakage current in region B, up to more than three decades at high reverse bias. Noteworthy, the same epilayer doping concentration ($\sim 1.0 \times 10^{16}\,cm^{-3}$) was determined from a C–V analysis of both samples (Fig. S2 in the supplementary material). Hence, the anomalous leakage current in region B cannot be explained by a different doping of the sample.

To better understand the observed different electrical behavior of the diodes illustrated in Fig. 1, μ-PL measurements were acquired in the two regions, in the spectral range of 380–480 nm. This analysis allows discriminating the expected band-to-band transition of 4H-SiC (PL emission peak centered around 390 nm) from other peaks related to the presence of defects, e.g., SFs that typically give a PL signal in the 415–480 nm range.[20] In order to inspect the region under the metal layer, we intentionally removed a metal strip on the contact to allow the laser radiation reaching the semiconductor surface. Figure 2(a) reports the PL spectra in the range of 390–470 nm acquired in a position close to the edge of the diodes fabricated in regions A and B. In both spectra, the peak at 395 nm related to the band-to-band transition is well visible. Moreover, an additional band centered around 425 nm is present in the spectrum of the diode in region B. The appearance of such a peak indicates the presence of defects in this region. In particular, Fig. 2(b) shows the μ-PL map at room temperature at the emission signal between 425 and 430 nm acquired close to the circular diode fabricated in region B. A triangular shaped PL-feature appears near the edge of the diode and, as highlighted by the removed metal region of the contact pad, this PL signal started in an external region of the contact and extend under the contact area.

As matter of fact, in 4H-SiC, various types of SFs can form, differing in their structure,[21] which can be discriminated by their PL fingerprints. In our case, the observed PL signal centered around 425 nm (2.92 eV) can be associated either to bar-shaped SFs or to single Shockley SFs (1SSFs), usually observed in epitaxial 4H-SiC layers.[20] However, the triangular shape revealed by the PL scanning in region B
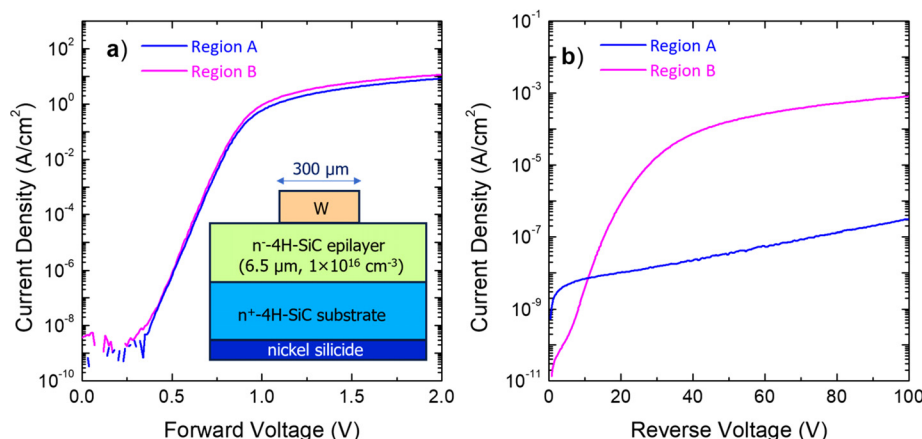

FIG. 1. Representative forward (a) and reverse (b) J–V curves acquired at room temperature in W/4H-SiC Schottky contacts located in two different regions of the sample. Measurement under forward bias (bias sweep from 0 to 2 V) was performed before the measurement under reverse bias (bias sweep from 0 to 100 V). The schematic cross section view of the contacts is reported as the inset of (a).
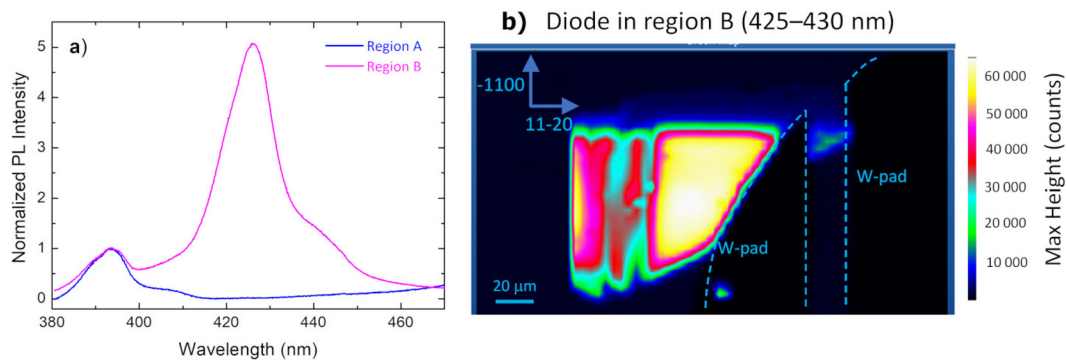
FIG. 2. (a) PL spectra in the range of 380–480 nm, detected in two selected positions close to the Schottky contact in region A and in region B. (b) μ-PL intensity map in the range of 425–430 nm acquired in the defective area in region B.

leans toward the presence of 1SSF defects, probably coming from basal plane dislocations (BPDs), for which the triangular shape is peculiar.[22] However, the presence of other defects under the contact pad, not detected by PL, cannot be excluded. As an example, x-ray topography allowed to classify a variety of defects affecting the leakage current of Schottky diodes in diamond.[23] On the other hand, Kodolitsch et al.[23] detected a large number of defects in 4H-SiC epilayers and reported a correlation between these defects and the leakage current in p–n junctions. However, based on their findings, the presence of micropipes and triangular defects can be ruled out in our case, since they would have a "killer effect" on the device functionality.[24]

The nanoscale electrical properties of the bare epilayer surface in the defective region B was further investigated by means of SCM analysis performed where the metal contact was removed. Figure 3 reports the morphological AFM scan (a) with the associated SCM map (b).

From the AFM map of Fig. 3(a), the topography in region B exhibits the commonly observed steps of 4H-SiC surface. Furthermore, the evaluated root mean square roughness (RMS ~ 0.70 nm) is very similar to the one measured in the sample region A. The SCM map consists of the differential capacitance (dC/dV) signal measured by the metal tip scanned in contact with SiC surface, in response to a high frequency AC bias. It provides information of the local charge density in the near surface region. Noteworthy, the electrical map in Fig. 3(b) is not influenced by the surface topography in Fig. 3(a), whereas it exhibits an extended feature with brighter contrast (high dC/dV) and nearly triangular shape, corresponding to the SF region previously identified by optical (μ-PL) measurements. The detected change in the SCM signal between the SF
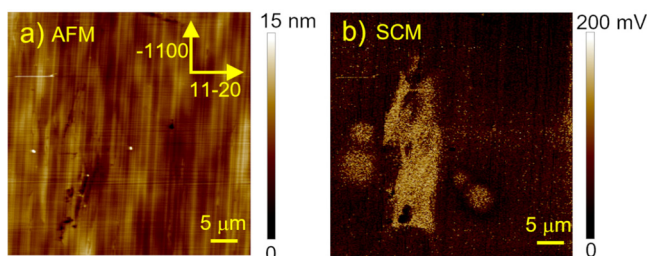
and outside regions can be due either to a difference in the active dopant concentration (N_D-N_A) in the epitaxy or to charges trapping in the near surface-region of the defect. However, macroscopic C–V characterizations of diodes on the two samples show very similar doping concentrations, allowing us to exclude a different incorporation of active dopants in the SF region of the epitaxy. Hence, the locally increased SCM signal on the SF was ascribed to trapped charges in the surface region.

In order to gain additional insight on the impact of these electrically active defects on the macroscopic behavior of the diode, we studied the temperature-dependence of the electrical characteristics. Under forward bias, the temperature dependence of the Schottky barrier height and ideality factors indicated the formation of an inhomogeneous barrier in both regions (see Fig. S3). Instead, a different behavior of the reverse leakage current was observed. In particular, the reverse current of the diode in region A can be well described by the thermionic-field-emission (TFE) model[25] (see the supplementary material, Fig. S1), as previously observed in similar contacts.[16,26]

On the other hand, already at room-temperature, the TFE cannot describe the leakage current in the defective area (region B), but other mechanisms must be involved in the current transport. Clearly, the presence of the defect in the contact region can be considered at the origin of the anomalous leakage current increase. In fact, the log–log plot of the reverse current in region B [Fig. 4(a)] indicated a power-law dependence of the current on the applied voltage ($J \propto V^m$). Specifically, three regions characterized by different values of the exponent m were visible, i.e., $m \approx 1$ (below 10 V), $m = 7.5$ ($10\,V < V_R < 30\,V$), and $m \approx 2$ (above 30 V). Such a behavior of the leakage current is typically explained considering a space-charge-limited current (SCLC) model in the presence of a trap distribution,[27–29] which rules the electron transport.[30] In our case, we can assume that this trap distribution is associated with the SF defect detected under the contact. According to the SCLC model, an ohmic behavior ($J \propto V$) is expected at low voltage, with the density of thermally generated free carriers in the semiconductor dominating over the injected carriers from the metal. By increasing the applied voltage, carriers injected from the metal start filling up the traps in semiconductor and, hence, a space-charge starts to appear. Then, a further increase in the bias induces the complete filling of these traps. In this situation, a further injection of charge is limited and space-charge controlled current occurs. This case can be assumed like a trap-free situation, with the current ruled by the
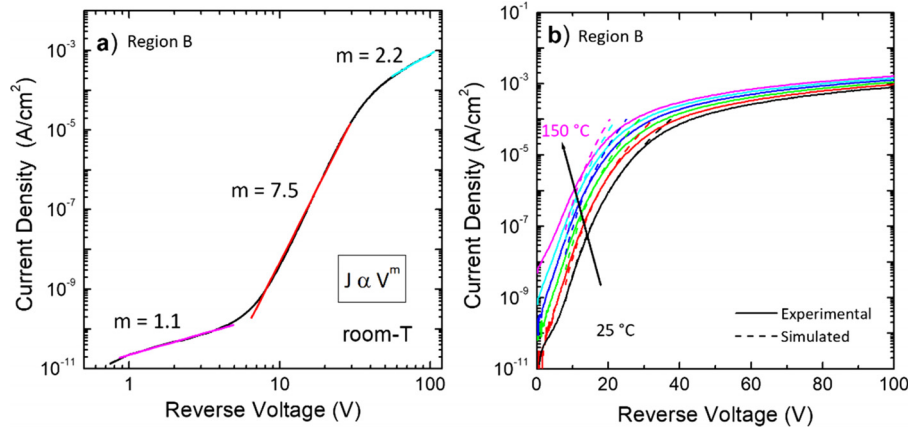

FIG. 3. (a) AFM morphological and (b) the associated SCM maps, acquired by in-plan scan in the contact area where the metal was removed.

FIG. 4. (a) Log–log plot of the room-temperature reverse J–V characteristic in the region B, highlighting the power-law dependence in the different voltage ranges. (b) Temperature-dependence of the reverse leakage current in region B.

Mott–Gurney law ($J \propto V^2$).[31] Hence, it can be argued that the presence of SFs introduced energy levels in the bandgap of 4H-SiC, which assist the carrier conduction under reverse bias.[22,32]

Quantitatively, from the intermediate voltage region analysis, the high-power function of the applied voltage (m = 7.5) is consistent with the presence of a trap distribution that decreases exponentially with the distance from the conduction band edge, i.e.,[27]

$$N_t(E) = N_t \, exp \left(-\frac{E_C - E}{kT_t} \right), \quad (1)$$

where $N_t(E)$ is the concentration of traps per energy unit at energy E, N_t is the total trap density, T_t is a temperature parameter characterizing the trap distribution with energy, and E_C is the minimum energy of the conduction band. In this case, for $T_t > T$, the current density dependence on the voltage V_R can be expressed as

$$J_{SCLC} = q\mu N_C \left(\frac{\varepsilon_S}{qN_0 kT_t} \right)^l \frac{V_R^{l+1}}{L^{2l+1}}, \quad (2)$$

where μ is the free-electron mobility, N_C is the conduction-band state density, L is the thickness of space-charge layer, and $l = m - 1$. By considering the temperature-dependence of the exponent l, it is possible to derive the parameter T_t from a linear fit of curve $l = T_t/T$.[33] Accordingly, a characteristic temperature parameter $T_t = 2515\,K$ ($\sim$0.215 eV) is obtained. This is an indication of a rapid variation of the trap distribution with energy. Furthermore, by choosing an arbitrary (J,V) point on the reverse characteristic in the intermediate region, it is possible to derive from Eq. (2) the N_t value, which for room-temperature is $9 \times 10^{18}\,cm^{-3}\,eV^{-1}$. The curves, simulated according to Eq. (2), are reported by dashed lines in Fig. 4(b).

In the highest part of the investigated voltage range (V > 30 V), the J–V characteristics can approximately be described by a quadratic law. According to the SCLC model, such a dependence is associated with the complete filling of the traps. In addition, this saturation behavior can be explained considering that moving from the substrate toward the surface, the SF expands inside the epilayer. Hence, with the increase in the depletion width by increasing the reverse bias (up to 3.3 μm for the applied reverse bias), the contribution of the SF gradually decreases, and the leakage current tends to saturate. Furthermore, the high reverse bias produces a notable band bending and thinning of

the barrier. This aspect, considering also the experimentally observed weak temperature dependence of the leakage current, allows to suppose the coexistence of a tunneling mechanism of the carriers through the barrier is likely to occur.[27]

In conclusion, we have investigated the impact of stacking faults (SFs) on the characteristics of 4H-SiC Schottky diodes under both forward and reverse bias. The defect presence under the contact was confirmed by μ-PL characterization and SCM analysis. An anomalous increase in the leakage current occurred for the diode fabricated on the defective region, while no significant effects were observed on the Schottky barrier height and ideality factor of the diode. The reverse leakage could be explained by a space-charge limited current model, consistent with the presence of a trap distribution in the bandgap of 4H-SiC. The weak temperature dependence of the reverse current observed for the highest voltage suggests that carrier tunneling sets in and may coexist with SCLC. Our investigation can be useful to explain unexpected anomalies in the reverse electrical behavior of 4H-SiC Schottky diodes.

See the supplementary material for additional information on the temperature-dependence of the barrier height and ideality factor, capacitance–voltage characterization, and current transport mechanism derived for diode in not-defective region.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Marilena Vivona: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal);

Writing – original draft (equal); Writing – review & editing (equal). **Patrick Fiorenza:** Formal analysis (equal); Investigation (equal); Methodology (equal). **Viviana Scuderi:** Formal analysis (equal); Investigation (equal). **Francesco La Via:** Formal analysis (equal); Investigation (equal). **Filippo Giannazzo:** Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Fabrizio Roccaforte:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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