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Laterally inhomogeneous barrier analysis of identically prepared *Cd/CdS/n-Si/Au–Sb* structures by SILAR method

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ABSTRACT

In this study, CdS thin films have been deposited on *n*-Si substrate using a successive ionic layer adsorption and reaction (SILAR) method at room temperature. Structural properties have been investigated by means of X-ray diffraction (XRD) and scanning electron microscopy (SEM) measurements. The XRD and SEM investigations show that films are covered well, polycrystalline structure and good crystallinity levels. The *Cd/CdS/n-Si/Au–Sb* structures (28 dots) have been identically prepared by the SILAR method. The effective barrier heights and ideality factors of these structures have been obtained from forward bias current–voltage (*I–V*) and reverse bias capacitance voltage (*C–V*) characteristics. The barrier height (BH) for the *Cd/CdS/n-Si/Au–Sb* structure calculated from the *I–V* characteristics have ranged from 0.664 eV to 0.710 eV, and the ideality factor from 1.190 to 1.400. Lateral homogeneous barrier height has been determined approximately 0.719 eV from the experimental linear relationship between BHs and ideality factors. The experimental BH and ideality factor distributions obtained from the *I–V* characteristics have been fitted by a Gaussian function, and their means of values have been found to be (0.683 ± 0.01) eV and (1.287 ± 0.05), respectively. The barrier height values obtained from the reverse bias C^{-2}–*V* characteristics have ranged from 0.720 eV to 0.865 eV and statistical analysis yields the mean (0.759 ± 0.02) eV. Additionally, a doping concentration obtained from C^{-2}–*V* characteristics has been calculated $(8.55 \pm 1.62) \times 10^{14}$ cm^{-3}.

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1. Introduction

The electrical properties of metal–semiconductor (MS) contacts have been widely studied, both for their basic physical properties and for their technological applications to electronic industry [1–6]. Interfaces between inorganic semiconductors and electrically active molecules have been useful tools in studying general charge-transfer theories and also raise many questions of their own. For semiconductor interfaces, the direct measure of carrier flux in the form of an electric current can then be directly related to a charge transfer velocity if the interfacial potential barrier built into the semiconductor is known and if the heterogeneous charge transfer process dominates the kinetics. The potential barrier Φ_{bp} arises from the region of ionized dopant atoms that forms during charge transfer equilibration when a semiconductor is contacted to another electroactive material [7].

The quantitative basis for the extraction of charge-transfer rate constants comes from the thermionic emission theory [8] originally developed for semiconductor–metal interfaces [9,10]. The *I–V* characteristics of real Schottky diodes usually deviate from the ideal thermionic emission model, which assumes the junction to be abrupt with a fixed Schottky barrier height (SBH). These deviations have been explained by assuming the presence of the barrier height inhomogeneities [11–21]. Two different approaches are adopted to describe the inhomogeneities. One approach assumes a continuous spatial distribution of SBH and the total current across a Schottky diode is simply calculated by integrating the current determined by the ideal thermionic-emission–diffusion (TED) model with an individual barrier height and weighted by the distribution function (parallel-conduction model) [11–17]. For the other approach, one assumes that some small patches of low SBH are embedded in the uniform SBH area [18–21]. The patch parameter is determined by multiplying the patch area and the SBH reduction. Using a pinch-off model, the current through a small patch is similar to a diode with an effective SBH and an effective area, both of which are dependent on the patch parameter and the bias voltage. The total current is composed of the current through the whole area with a uniform SBH and the current through the patches. The latter may dominate at small bias, especially at low temperature, thus a double threshold behavior may be seen in the *I–V* characteristics.

The majority of MS and metal–insulator-semiconductor (MIS) contacts investigated up to now have been characterized with *I–V*, *C–V*, and photoresponse spectros-copies [22]. These techniques remain the primary tools with which the SBH at a particular

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MS contact is evaluated [23]. An additional method has recently been developed for studying barrier formation at MS interfaces and semiconductor heterojunctions is ballistic-electron-emission microscopy (BEEM) [24]. Unlike conventional methods (*I–V, C–V*) where the entire area of the contact is sampled in evaluating the SBH, BEEM is a local probe that can in principle resolve the SBH on a nanometer scale, and provide information about the spatial distribution of the SBH [25].

Successive ionic layer adsorption and reaction (SILAR) method is the trend which involves the growth of thin films from solution, ionic layer by layer at room temperature and at normal pressure. Single SILAR deposition cycle involves the immersion of the substrate alternately in cationic and anionic precursor solutions and rinsing between every two consecutive immersions with de-ionized water to avoid homogeneous precipitation in the solution, so that only the tightly adsorbed layer stays on the substrate. The adsorption is a surface phenomenon occurring due to attractive force between ions and surface of substrate. This attractive force is of Van der Waals type that basically originates due to the residual or unbalanced force present in the substrate. Thus, ad-atoms can be holding on the surface of the substrate by that residual force [26,27].

In this study, the SILAR method was used to deposition of CdS thin film on *n*-Si substrates. The films were characterized for their structural and optical properties by using XRD and SEM methods. The *Cd/CdS/n-Si/Au–Sb* structure was identically prepared on the same *n*-Si semiconductor substrate by SILAR method and then calculated electrical parameters from the *I–V* and *C–V* measurements. The effective BHs and ideality factors from the experimental forward bias *I–V* and reverse bias *C–V* characteristics of these structures were calculated using the thermionic emission theory. The homogeneous BH value for the device was obtained from the linear relationship between experimental effective BHs and ideality factors. The statistical distribution of the characteristic parameters of the devices was made by means of the Gaussian function.

2. Experimental

n-Type Si single crystal has been used as semiconductor substrate with a [1 1 1] surface orientation, 400 μm thickness and 1–10 Ω-cm resistivity. The wafer was chemically cleaned using the RCA cleaning procedure (i.e. 10 min boil in $NH_3 + H_2O_2 + 6H_2O$ followed by $HCl + H_2O_2 + 6H_2O$ at 60°C). The native oxide on the front surface of the *n*-Si substrate was removed in $HF + 10H_2O$ solution and finally the wafer rinsed in de-ionized water for 30 s. The wafer was dried with high-purity nitrogen, and inserted into the deposition chamber immediately. The ohmic contact was made by evaporating Au–Sb alloy on the back of the substrate in a vacuum-coating unit of 10^{-5} Torr, then, it was annealed at 420 °C for 3 min in N_2 atmosphere. After ohmic contact made, the ohmic contact side and the edges of the *n*-Si semiconductor substrate were covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed to the cationic precursor solution employed for SILAR method. More details of SILAR method for the deposition of CdS thin film are well documented in literature [28]. The homogeneous interface thin film layers were obtained after repeated 25 SILAR cycles. Then to perform the electrical measurements Cd dots with diameter of about 1.0 mm (the contact area = 7.85×10^{-3} cm^2) were evaporated on the CdS thin film in vacuum coating unit at about 10^{-5} torr. In this way, the *Cd/CdS/n-Si/Au–Sb* structure was obtained.

The films on Si substartes were characterized for their structural properties by using X-ray diffractometer in the range of scanning angle 20–70° using Rigaku D/Max-IIIC diffractometer and ZEISS SUPRA 50VP scanning electron microscope. The *I–V* and *C–V* characteristics of this structure were measured using a HP 4140B picoampermeter and a HP model 4192A LF impedance analyser, respectively, at room temperature and in the dark.

3. Results and discussion

The deposited CdS thin films were analysed by X-ray diffraction pattern for structural analysis by using CuKα radiation with the help of Rigaku D/Max-IIIC X-ray diffractometer. Fig. 1 shows the XRD diffraction pattern of the *n*-Si with CdS thin film. The intensity of the peaks demonstrates hexagonal phase of the products and high crystallinity along different planes and phases of the CdS thin films grown by SILAR. The plane of Si (1 1 1) substrate is clearly observed in Fig. 1 and the plane intensity is dominant comparison with the other ones. The *d*-values were calculated by calculating θ values from the peaks of the X-ray spectrum by using Bragg's relation [29,30];

$$2d\mathrm{Sin}\theta = n\lambda \tag{1}$$

In the present study n is 1 and λ is 1.5405 for Cu Kα. The observed d value is found 3.179 Å for single crystal Si (1 1 1) substrate. Fig. 1 shows the well resolved peaks d = 3.360 Å (0 0 2); d = 2.956 Å (2 0 0); d = 2.479 Å (1 0 2); d = 2.060 Å (1 1 0); d = 1.7540 Å (1 1 2). These d values were compared with the standard JCPDS data to confirm the structure of CdS. It is seen that d values are good agreement with those given in literature [31–34].

The SEM image in Fig. 2 shows the general morphology of the as-prepared product, SEM micrograph shows that the films are continuous fairly uniform and polycrystalline on the Si substrate. The grain size in the film is seen to be almost uniform. There are no macroscopic defects like void, pinhole, peeling or cracks.

The *I–V* characteristics of the MS contacts due to thermionic emission current can be expressed [23]

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{2}$$

where V is the applied voltage, n is the ideality factor and I_0 is the saturation current determined by

$$I_0 = AA^*T^2\exp\left(\frac{-q\Phi_{b0}}{kT}\right) \tag{3}$$

where A is the diode area, A^* is the effective Richardson constant, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge and Φ_{b0} is the barrier height. For values of V greater than $3kT/q$, the ideality factor and barrier height can be written as, respectively:

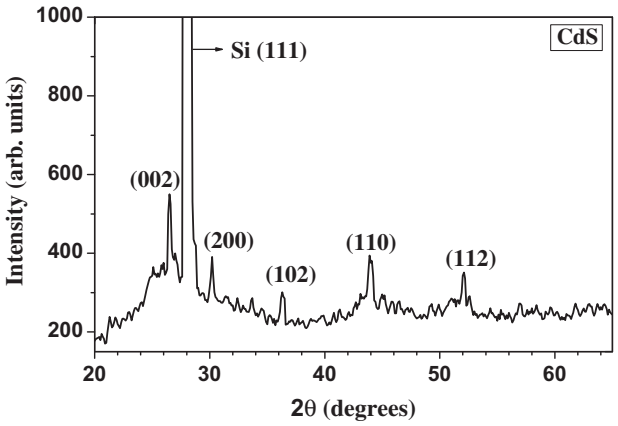

Fig. 1. XRD pattern of CdS thin films grown on *n*-Si substrate.

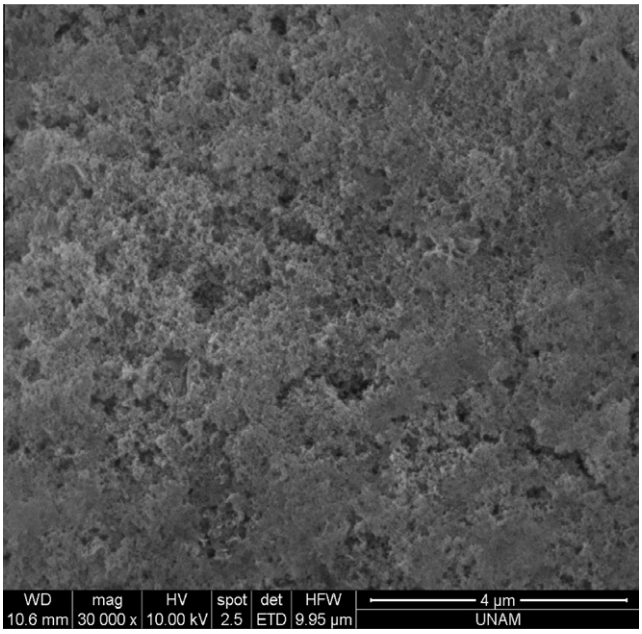

Fig. 2. SEM image of CdS thin films grown on *n*-Si substrate.

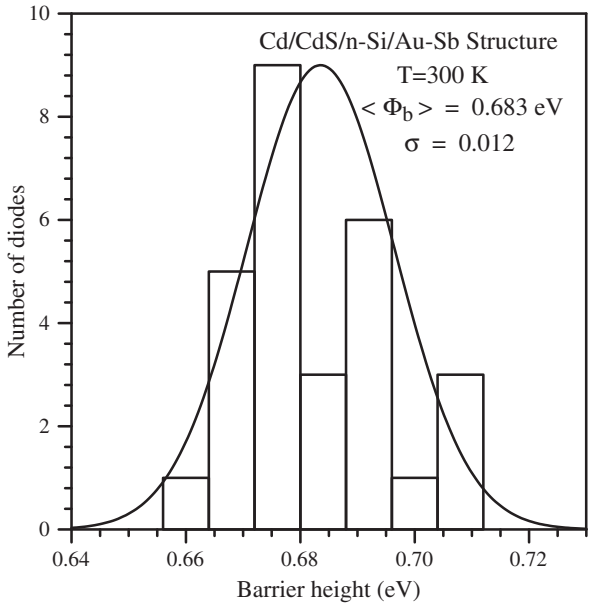

Fig. 4. Gaussian distribution of barrier heights obtained from the *I–V* characteristics of *Cd/CdS/n-Si/Au–Sb* structure at room temperature. The Gaussian fit yields Φ_b = 0.683 eV and σ = 0.01 eV for the barrier heights.

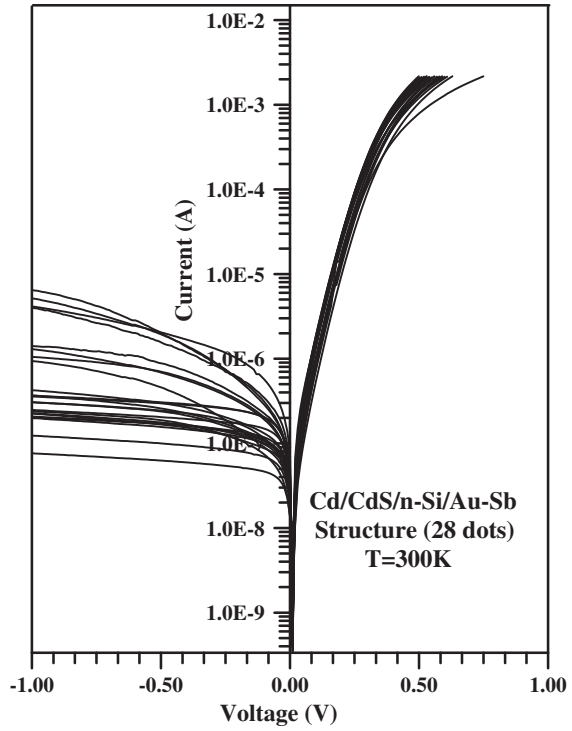

Fig. 3. Forward and reverse bias current–voltage characteristics of *Cd/CdS/n-Si/Au–Sb* structure at room temperature.

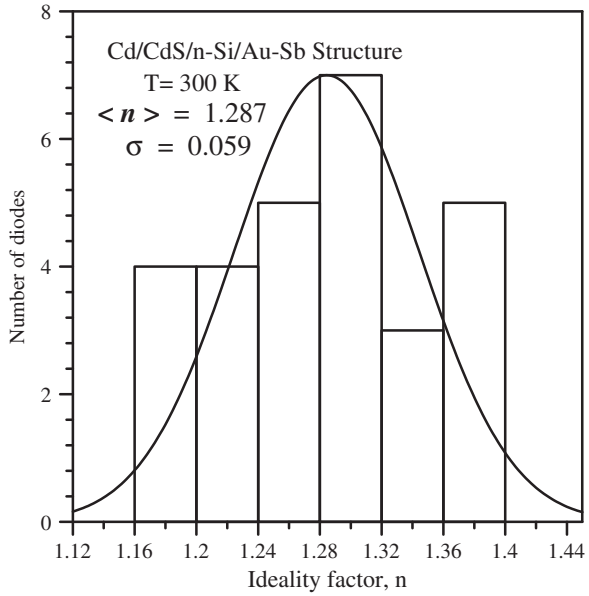

Fig. 5. Gaussian distribution of ideality factor obtained from the *I–V* characteristics of *Cd/CdS/n-Si/Au–Sb* structure at room temperature. The Gaussian fit yields n = 1.287 and σ = 0.05 for the ideality factors.

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{4}$$

$$\Phi_{b0} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \tag{5}$$

Fig. 3 shows the experimental semi-log forward and reverse bias characteristics of the *Cd/CdS/n-Si/Au–Sb* structure at room temperature. We prepared 28 dots for the *Cd/CdS/n-Si/Au–Sb* structure on the same *n*-type Si semiconductor substrate. According to Eq. (2), the respective slope parameter gives the ideality factor and extrapolation the zero applied voltage gives the zero bias BH. The calculated BH for the structure ranged from 0.664 eV to 0.710 eV, and the ideality factor n ranged from 1.190 to 1.400. The high values of *n* can be attributed secondary mechanisms which include interface dipoles due to interface doping or specific interface structure as well as fabrication-induced defects at the interface [18,23,31–36]. Furthermore, the high values of *n* can be attributed to the presence of a wide distribution of low-SBH patches caused by lateral barrier inhomogeneity [18].

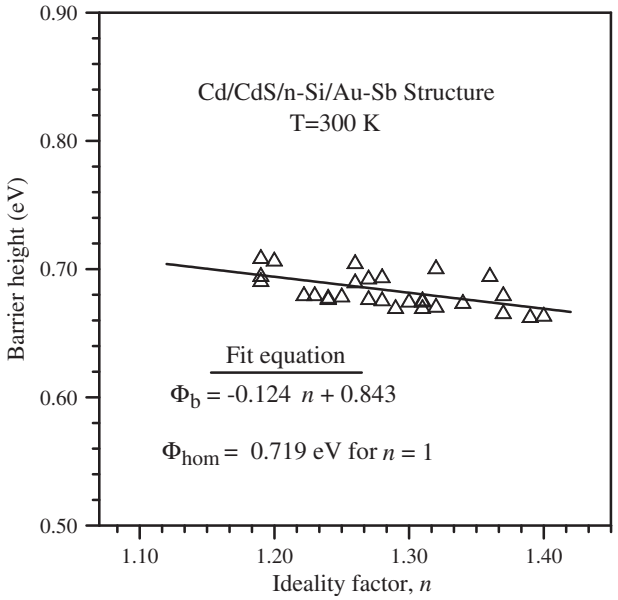

Fig. 6. Plot of experimental barrier height versus ideality factor of the *Cd/CdS/n-Si/Au–Sb* structure at room temperature.

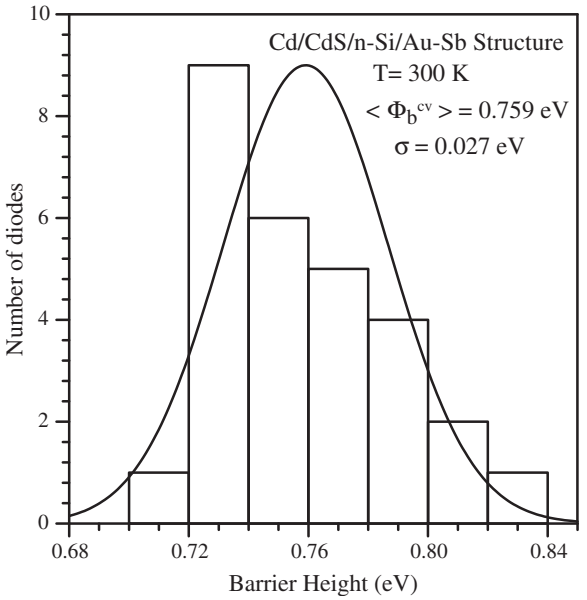

Fig. 8. Gaussian distribution of barrier heights obtained from the the reverse bias C^{-2}–V characteristics of *Cd/CdS/n-Si/Au–Sb* structure at a frequency of 500 kHz and room temperature. The Gaussian fit yields $\Phi_b = 0.759$ eV and $\sigma = 0.027$ eV for the barrier heights.

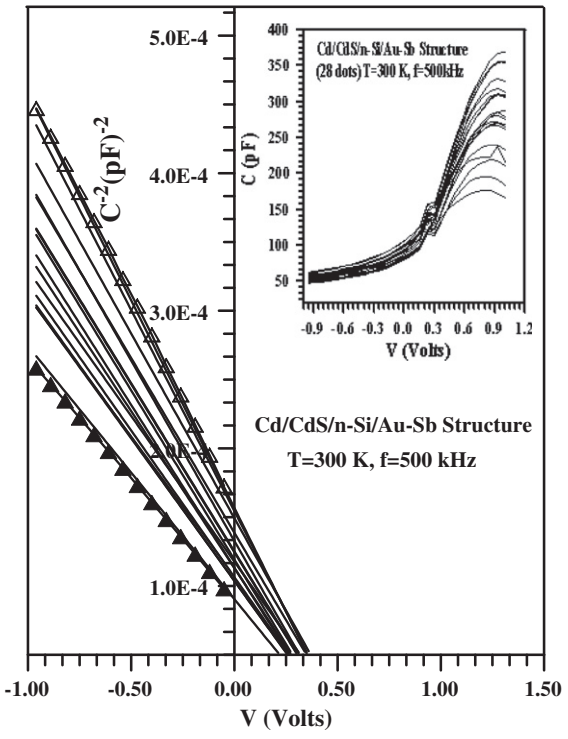

Fig. 7. Capacitance–voltage and reverse bias C^{-2}–V characteristics of the *Cd/CdS/n-Si/Au–Sb* structure at a frequency of 500 kHz and room temperature.

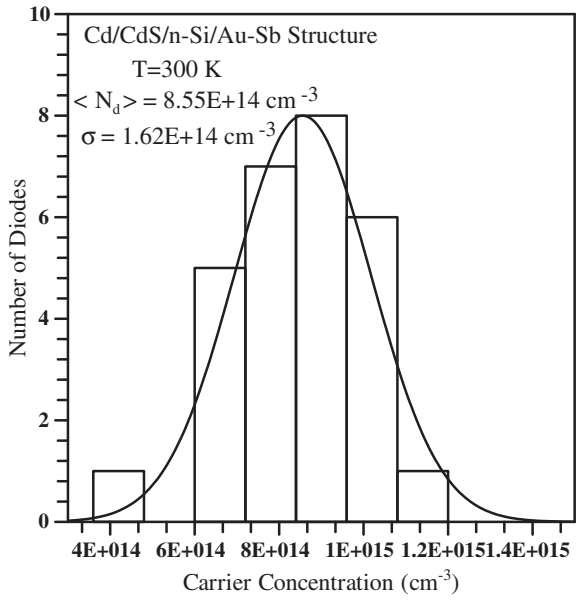

Fig. 9. Gaussian distribution of carrier concentrations obtained from the reverse bias C^{-2}–V characteristics of *Cd/CdS/n-Si/Au–Sb* structure at a frequency of 500 kHz and room temperature. The Gaussian fit yields $N_d = 8.55 \times 10^{14}$ cm^{-3} and $\sigma = 1.62 \times 10^{14}$ cm^{-3} for the carrier concentrations.

The BHs and ideality factors vary from diode to diode, therefore, it is common practice to take averages [35]. Figs. 4 and 5 show histograms of the BHs and ideality factors of the *Cd/CdS/n-Si/Au–Sb* structure (28 dots). The statistical analysis yielded a mean BH value of 0.683 ± 0.01 eV and a mean ideality factor value of 1.287 ± 0.05. The experimental distributions of the effective BHs and ideality factors were fitted by the Gaussian function.

Fig. 6 shows the BH of the *Cd/CdS/n-Si/Au–Sb* structure as a function of their ideality factors. As can be seen from Fig. 6, the BHs are smaller as the ideality factor increase. Therefore Fig. 6 confirms the well-known linear correlation between effective BHs and ideality factors [35–41]. These findings may be attributed to lateral inhomogeneities of the BHs in metal–semiconductor contacts [35]. The inhomogeneities of the BHs may play an important role and have to be considered in the evaluation of experimental *I–V* characteristics [18,35,42–46]. The application of standard procedures Eq. (1) gives the effective BH and ideality factor. A system of discrete regions or 'patches' as low BH imbedded in a higher barrier uniform barrier is used to explain commonly observed deviations

from the standard thermionic emission theory [18]. The patches are taken to be small relative to the size of the depletion region causes pinch-off or saddle point in the potential barrier away from the interface [47]. The laterally homogeneous BH value was found to be 0.719 eV from Fig. 6. It can be instructive to see whether the slope correlates patch parameters. This is relationship between the apparent ideality factor and the fluctuations in the barrier heights in Tung's model [18,48,49]. This finding and the assumptions that the patches have smaller BHs than homogeneous contact explain the experimentally observed reduction of the BHs with increasing ideality factors [35].

Fig. 7 shows reverse bias C–V and C^{-2}–V characteristics of *Cd/CdS/n-Si/Au–Sb* structure at 500 kHz and room temperature. As can be seen from Fig. 7, the C^{-2}–V characteristics are linear over the range of 0.0–1.0 V for each dot.

In *MS* contact, the depletion layer capacitance can be expressed as [23,49]

$$C^{-2} = \frac{2(V_{d0} + V)}{\varepsilon_s q A^2 N_d} \tag{6}$$

The slope of the reverse-bias C^{-2}–V plot can also be given by

$$\frac{d(C^{-2})}{dV} = \frac{2}{\varepsilon_s q A^2 N_d} \tag{7}$$

where A is the area of the diode, V_d is the diffusion potential at zero bias and is determined from the extrapolation of the linear C^{-2}–V plot to the V-axis. The value of the BH can be calculated by the relation:

$$\Phi_b^{cv} = V_d + V_n \tag{8}$$

where V_n is the potential difference between the Fermi level and the bottom of the conduction band for n-Si in the neutral region; it can be calculated knowing the carrier concentration N_d from the slope of the linear C^{-2}–V plot and is obtained from the following relation:

$$V_n = kT \ln\left(\frac{N_c}{N_d}\right) \tag{9}$$

where $N_c = 2.8 \times 10^{19}\ \mathrm{cm}^{-3}$ (at $T = 300$ K) is the state density in the conductance band for n-Si [50].

The BH and carrier concentration values of *Cd/CdS/n-Si/Au–Sb* structure were determined from its reverse bias C^{-2}–V characteristics. The BH and carrier concentration values obtained from the reverse bias C^{-2}–V characteristics have ranged from 0.720 eV to 0.865 eV and from $7.147 \times 10^{14}\ \mathrm{cm}^{-3}$ to $1.100 \times 10^{15}\ \mathrm{cm}^{-3}$, respectively. As can be seen from Figs. 8 and 9, the experimental distributions of the BHs and donor concentrations were fitted by the Gaussian function. The statistical analysis of BHs and doping concentrations obtained from C^{-2}–V characteristics has yielded a mean BH value of 0.759 eV with standard deviation of 0.02 eV and mean a donor concentration value of $8.55 \times 10^{14}\ \mathrm{cm}^{-3}$ with a standard deviation of $1.62 \times 10^{14}\ \mathrm{cm}^{-3}$ for *Cd/CdS/n-Si/Au–Sb* structure.

As can be seen from the mean values, the BH calculated from the I–V characteristics is not equal the BH extracted from C–V characteristics. Both techniques are differently sensitive to possible occurance of inhomogeneities and especially small patches with a lower Schottky BH at the contact, strongly influences the resulting appearent SBH. On the other hand, BHs calculated from the C–V measurements have a tendency to be an average value of the SBHs of patches present in the contact (BH inhomogeneities that are present in the CdS/n-Si interface), that is, average BH is the mean value of the barrier minima plus barrier maxima [51].

4. Conclusion

We used the SILAR method to deposit CdS thin films on n-Si subsrate. Structural and morphological properties of CdS thin film were investigated by XRD and SEM methods. The CdS films were found to have polycrystalline, homogeneous and covered the substrate well. The BHs and ideality factors of *Cd/CdS/n-Si/Au–Sb* structure have been calculated from the I–V characteristics. Although the structure identically prepared, the effective BH and ideality factor varied from the diode to diode. The mean vaule of effective BH found to be 0.683 eV by using Gaussian distribution. Plotting the BH versus ideality factor curve for *Cd/CdS/n-Si/Au–Sb* structure, lateral homogeneous BH was calculated as a value of 0.719 eV from the observed linear correlation between BH and ideality factor, which can be explained by laterally inhomogeneities of BHs. The BH value obtained from the reverse bias C^{-2}–V characteristics has ranged from 0.720 eV to 0.865 eV and statistical analysis yields the mean BH value (0.759 ± 0.02) eV. Additionaly, a doping concentration obtained from C^{-2}–V characteristics has been calculated $(8.55 \pm 1.62) \times 10^{14}\ \mathrm{cm}^{-3}$. It has been shown that CdS thin film layer grown by means of SILAR method can be confidently used in the Cd/n-Si metal–semiconductor contacts as alternatively MBE, MOCVD, sputtering and vacuum evaporation methods.

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