Tutorial: Organic field-effect transistors: Materials, structure and operation

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Chemical versatility and compatibility with a vast array of processing techniques has led to the incorporation of organic semiconductors in various electronic and opto-electronic devices. One such device is the organic field-effect transistor (OFET). In this tutorial, we describe the structure, operation, and characterization of OFETs. Following a short historical perspective, we introduce the architectures possible for OFETs and then describe the device physics and the methods for extracting relevant device parameters. We then provide a brief overview of the myriad organic semiconductors and deposition methods that were adopted for OFETs in the past decades. Non-ideal device characteristics, including contact resistance, are then discussed along with their effects on electrical performance and on the accuracy of extracting device parameters. Finally, we highlight several measurements involving OFETs that allow access to fundamental properties of organic semiconductors and the mechanism of charge transport in these materials. *Published by AIP Publishing.* https://doi.org/10.1063/1.5042255

I. INTRODUCTION

The field of organic electronics has attracted significant interest since its beginning in the 1960s with the identification of the first organic semiconductors,[1,2] followed by the discovery of doped polyacetylene in 1977,[3] and the Nobel Prize awarded to Heeger, Diarmid, and Shirakawa in 2000.[4] Research efforts have focused on manipulating the chemical structure and degree of order of the semiconductor layer, understanding and controlling the processes taking place at device interfaces, light manipulation, integration with biological systems, and more. These efforts have been largely successful, and, as the field has seen radical improvements, an increasing number of products are approaching the marketplace. The structure of organic semiconductors departs quite heavily from that of the traditional inorganic semiconductors: organic solids are characterized by weak van der Waals bonds, in contrast to semiconductors like Silicon or Germanium, where covalent bonds define the crystals. This is a key difference which impacts their properties and processing: while the inorganic compounds require extreme processing conditions, such as high temperature and vacuum, the weak bonding present in organic materials allows for processing at or around room temperature and in ambient pressure via ink-jet printing, laser printing,[5–7] or other simple methods, opening the realm of plastics,[8–16] textiles,[17] and paper[7,18,19] for use as substrates. Silicon-based transistors have revolutionized modern electronics and are ubiquitous not only in many technologies that shape our personal lives, but also in industries such as transportation, communication, manufacturing, engineering, medicine, energy, defense, and national security. Organic electronic devices are envisioned to supplement the existing silicon-based technologies by enabling applications inaccessible to rigid electronics. The electrical properties of organic semiconductors arise from the conjugated π-orbitals present, which facilitate electron delocalization and charge transport. Different types of devices based on organic semiconductors have been demonstrated, including organic photovoltaics (OPVs),[20–23] organic light-emitting diodes (OLEDs),[24,25] sensors,[26–28] and organic field-effect transistors (OFETs).[29–31] Since the earliest OFETs developed in the 1980s,[32–35] device performance has radically improved due to a better understanding of the impact of the chemical and solid-state structures of the semiconductor, the effects of the dielectric layer, and the injection processes at the contacts. On one hand, the OFETs have an enormous technological appeal since they can provide the basic unit that can act as on/off switches in a broad range of electronic and opto-electronic applications. On the other hand, they are excellent platforms for answering intriguing scientific questions about charge transport in organic semiconductor materials, with a fine control of the charge density in the semiconductor layer. In this tutorial review, we introduce the components, device physics, materials, and fabrication methods for OFETs, the models used for their characterization, the deviations from these ideal characteristics, and their impact on the accuracy of the extracted parameters.

In Sec. II, we describe the various structures adopted for OFETs, their mechanism of operation, and the models used to characterize transistor operation. Section III outlines the materials incorporated in OFET architectures, including organic semiconductors, dielectrics, and electrodes. The effects of contact resistance on OFET operation are explained in Sec. IV, along with several methods to evaluate its magnitude. Section V describes different measurements which can be carried out on OFET structures in order to extract information about the basic properties and charge transport mechanism in organic semiconductors.

II. OFET STRUCTURE AND OPERATION

A. Device geometry

The OFET is comprised of several electrically active layers assembled on a substrate: the organic semiconductor, the gate dielectric, and the electrodes (contacts), namely, the gate, source, and drain electrodes. These layers are generally arranged in one of four device architectures, depending on the order in which the layers have been deposited (Fig. 1): bottom gate, bottom contacts [BGBC—Fig. 1(a)]; bottom gate, top contacts [BGTC—Fig. 1(b)]; top gate, bottom contacts [TGBC—Fig. 1(c)]; and top gate, top contacts [TGTC—Fig. 1(d)]. These four structures are divided into two categories, coplanar (BGBC and TGTC) and staggered (BGTC and TGBC). Here, coplanar refers to the source, drain, and conducting channel being located on the same plane, and in the staggered structures the conducting channel is offset from the plane of the source and drain contacts. If the semiconductor is in a thin-film form, the devices are referred to as organic thin-film transistors (OTFTs). Similarly, single crystals create single crystal field-effect transistors (SC-FETs). Each of the four structures presents advantages and disadvantages, and the type of structure to be adopted is a direct consequence of its purpose. For instance, the BGBC structure allows for quick examination of new semiconductor materials and processing methods because the gate electrode, gate dielectric, and source and drain contacts are pre-fabricated, and the semiconductor is deposited in the last step of the process. This also has the advantage of maintaining a pristine semiconductor-dielectric interface as no additional steps are required after deposition of the semiconductor. However, this structure leaves the semiconductor exposed to ambient conditions which may accelerate degradation due to oxygen, water, and other factors. The structures which involve a top-gate electrode, TGBC, and TGTC, can reduce environmental degradation of the semiconductor as the dielectric also acts as an encapsulation layer, however the dielectric must be chosen carefully to preserve the integrity of the semiconductor.

B. OFET operation and determination of device parameters

The operation of an OFET relies on the application of two potentials, one at the gate electrode and the other at the drain electrode, with the source electrode held at ground. The resulting two voltages are the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}). For the following discussion, the OFET channel is assumed to be p-type, where the majority charge carriers are holes, though for n-type, where the charge carriers are electrons, the polarities are simply reversed (more details on the type of transport will be provided in Sec. III). With no V_{GS} being applied, there is no charge accumulation at the semiconductor-dielectric interface, i.e., the device is turned "off" (note: this only applies in the case of ideal devices, with zero threshold voltage). At the simplest level, an applied V_{GS} polarizes the dielectric causing the accumulation of charge carriers at the semiconductor-dielectric interface: the transistor turns "on." An applied V_{DS} forces these accumulated charge carriers from the source to the drain electrode where the drain current (I_D) is measured. The charge density in the transistor channel and, thus, the current, are modulated by the magnitude of the field applied, V_{GS}, hence the "field-effect" terminology. In a real device, a small, negative V_{GS} is often required first to fill charge traps at the semiconductor-dielectric interface before free charge carriers can accumulate in the conduction channel. This trap-filling potential is known as the threshold voltage (V_{Th}) and can result from sources like crystal defects, impurities, or interfacial roughness. In addition, small amounts of dopants in the semiconductor and surface dipoles can result in a positive threshold voltage wherein the device is already "on" at $V_{GS} = 0\,\text{V}$ and requires a positive V_{GS} to reach the "off" state.

Figure 2(a) shows the evolution of the drain current with increasingly negative drain-source voltage where each curve is measured at a fixed, negative, gate-source voltage; this type of measurement is known as the "output characteristics." When $V_{DS} < |V_{GS} - V_{Th}|$, the device is in the *linear regime*, Fig. 2(b); here the drain current increases linearly with the drain-source voltage and the device acts as a gate voltage-controlled variable resistor. As V_{DS} increases and the magnitude approaches that of V_{GS}, the shape of the conduction channel changes due to the two interacting potentials, with the details of this transition being dictated by the magnitude of the threshold voltage. At the critical point, where $V_{DS} = |V_{GS} - V_{Th}|$, the area near the drain electrode is depleted of free charge carriers and the channel becomes pinched off, Fig. 2(c). A space-charge limited current flows across this depletion region as the applied electric field moves the charge carriers from the pinch-off point to the drain electrode. Further increase in V_{DS} results in competing effects of the increasing potential forcing charges from source to drain and the growing depletion zone near the drain cause a saturation of I_D, Fig. 2(d), leading to the *saturation regime*. Figures 3(a) and 3(b) show in black the drain current on a logarithmic scale as a function of gate-source voltage with drain-source voltage held constant in the linear and saturation regimes respectively. In blue, Fig. 3(a) shows the drain current on a linear scale and Fig. 3(b) shows the square-root of drain current on a linear scale. This type of measurement is known as the "transfer characteristics." The field-effect mobility, μ, a measure of how quickly charge carriers move in response to an external electric field, is
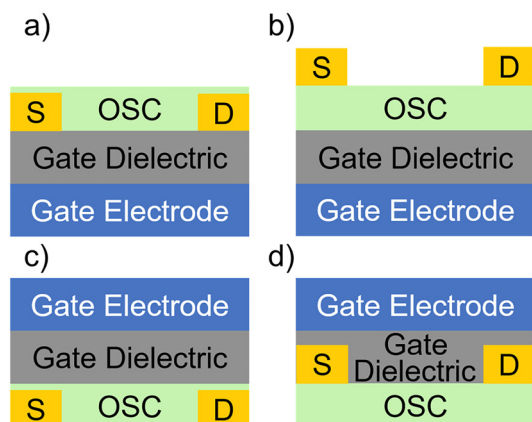

FIG. 1. OFET device structures: (a) bottom gate, bottom contact, (b) bottom gate, top contact, (c) top gate, bottom contact, and (d) top gate, top contact.
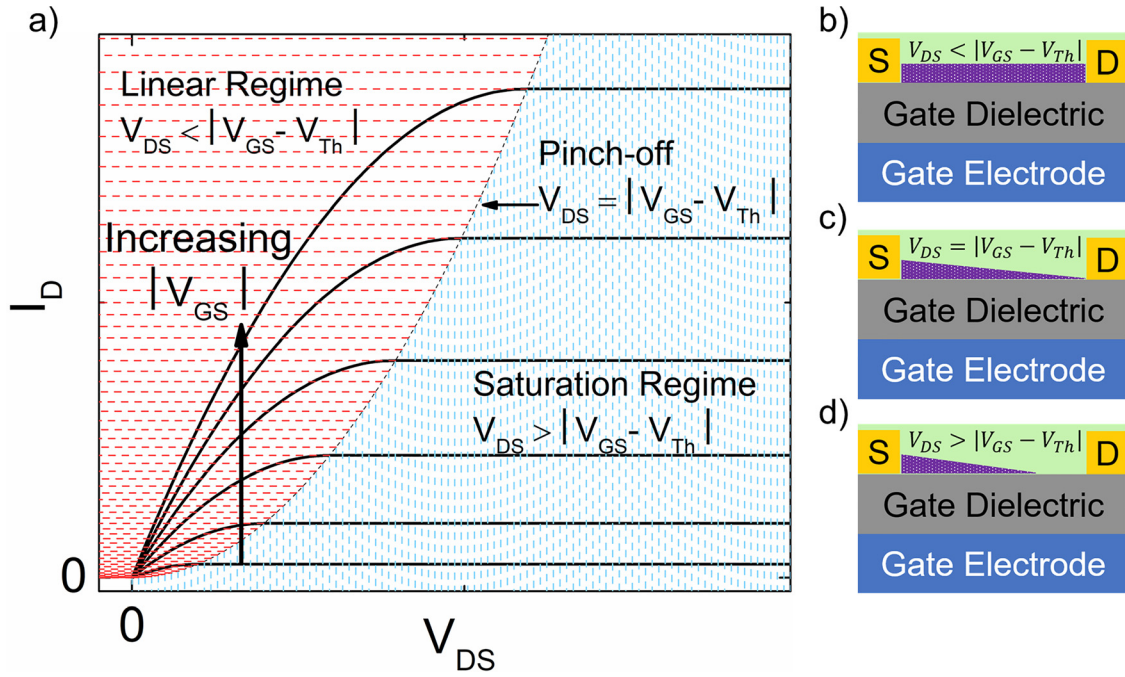
FIG. 2. (a) Ideal OFET output characteristics, (b)–(d) BGBC structures with the conduction channel in purple, (b) in the linear regime, (c) at pinch-off, and (d) in the saturation regime.
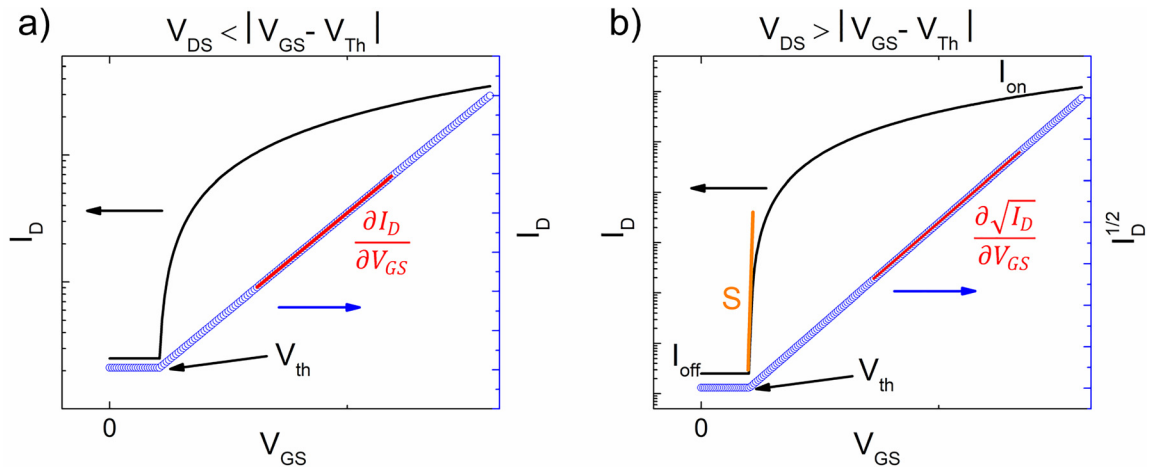

FIG. 3. Evolution of I_D at fixed, negative, V_{DS} as a function of increasingly negative V_{GS} in (a) the linear regime and (b) the saturation regime.

calculated from the slope of the red line in Fig. 3(a), $\frac{\partial I_D}{\partial V_{GS}}$, for the linear regime, and from the slope of the red line in Fig. 3(b), $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$, for the saturation regime, as we will detail below. The mobility μ has units of cm^2/Vs: as a reference the mobility of amorphous silicon is approximately 1 cm^2/Vs and that of single-crystal silicon is 100–1000 cm^2/Vs, depending on the fabrication conditions.[36] Another important set of values which can be extracted from Fig. 3 are the "on" current, I_{on}, and the "off" current, I_{off}, which, when taken together, provide the on/off ratio. A large on/off ratio is needed such that the "on" state and the "off" state are clearly distinguishable. I_{off} can be minimized through the choice of dielectric material, proximity to adjacent devices, and patterning both the semiconductor and the gate electrode, among other techniques. I_{on} can depend on numerous factors such as the mobility of the semiconductor, the capacitance of the gate dielectric, the operating voltages, and the density and type of

trap states present at the semiconductor-dielectric interface. Figure 3 also yields the value of the threshold voltage, V_{Th}, which is calculated by finding the intercept of $I_D = 0$ and the red line.[37] The threshold voltage is a result of trap states being present in the semiconductor layer; these traps are first filled by the applied V_{GS} and then free charge carriers contribute to the drain current. In most cases, the density of trap states increases with decreasing temperature (exceptions include the devices fabricated on dielectrics for which the dielectric constant varies with temperature, such as ferroelectrics),[38,39] thus V_{Th} is dependent on temperature, allowing an estimation of the density of interfacial trap states, N_{it}, through measurements at varying temperature and application of the below equation

$$N_{it} = \frac{C_{diel}}{k_B q} \frac{\partial V_{Th}}{\partial T}, \tag{1}$$

where k_B is Boltzmann's constant, T is the temperature, C_{diel} is the gate dielectric capacitance per unit area, and q is the elementary charge.[40]

In addition to the threshold voltage, another indication of the presence of charge traps can be seen in the sub-threshold swing or inverse sub-threshold slope (S), the inverse slope of the orange line in Fig. 3(b). S is a measure of how fast the device switches from the off to the on state, meaning how rapidly I_D increases with V_{GS} at fixed V_{DS}. S has units of V/decade and expresses the increase in V_{GS} to cause a 10-fold increase in I_D

$$S = \frac{\partial V_{GS}}{\partial(\log_{10}(I_D))}. \tag{2}$$

S depends on the interfacial trap states, and the gate dielectric as defined in the following equation:

$$S = \frac{k_B T ln(10)}{q}\left(\frac{N_{it}q^2}{C_{diel}} + 1\right). \tag{3}$$

A smaller value of S indicates that the device has a sharp turn-on and the theoretical lower limit of S at room temperature ($T = 300$ K) is 60 mV/dec, as the first term in Eq. (3) approaches zero.

Another signature of the existence of traps is device hysteresis, where there is a significant difference in current characteristics in the forward voltage sweep and the reverse voltage sweep. This difference can occur when charges become trapped and then released on the forward and reverse sweeps, respectively, and also in the presence of highly polar dielectrics. A series of extremely useful methods for characterizing the trap states in an OFET have emerged whereby the trap density as a function of energy in the band gap (trap density of states, or trap DOS) is calculated from the standard transistor measurements.[41–43]

To analyze the electrical properties of an OFET, *the gradual channel approximation* is made. In the frame of this model, the electric field between the source and gate electrode is much larger than the electric field between the source and drain electrodes. This is generally accomplished by ensuring that the gate dielectric thickness, d, and the channel length, L, satisfy the relation $\frac{L}{d} \geq 10$, and therefore its adoption may become problematic in devices with very short channel lengths.[44] With this relation in place, the magnitude of V_{GS} dictates the density of charge accumulation at the semiconductor-dielectric interface, and the potential distribution can be approximated as one-dimensional across the channel. The total charge density in the transistor channel is given by Eq. (4), with x representing the distance across the channel measured from the source to the drain electrode

$$Q = -C_{diel}V_{total}(x), \quad V_{total}(x) = V_{GS} - V(x). \tag{4}$$

Here, $V_{total}(x)$ is the total potential in the channel resulting from an applied V_{DS} and V_{GS}. However, as mentioned earlier, in a real device, a potential V_{Th}, is required to fill traps before mobile charge carriers are accumulated and thus Eq. (4) becomes

$$Q_{mobile} = -C_{diel}(V_{GS} - V(x) - V_{Th}). \tag{5}$$

The mobile charges present along the x-direction, between the source and drain electrodes, create the current I_D defined as

$$I_D = \mu QWE_x, \quad E_x = -\frac{dV}{dx}, \tag{6}$$

where E_x is the electric field in the direction of current flow, W is the channel width, and μ is the charge-carrier mobility. Substituting Eq. (5) into Eq. (6) gives

$$I_D dx = W\mu C_{diel}(V_{GS} - V(x) - V_{Th})dV, \tag{7}$$

and, assuming that the charge-carrier mobility μ does not vary with the applied potential, integrating Eq. (7) along the channel from $x = 0$ to the channel length L, and from $V = 0$ to V_{DS} as such

$$\int_0^L I_D dx = W\mu C_{diel}\int_0^{V_{DS}}(V_{GS} - V(x) - V_{Th})dV$$

results in

$$I_{D,lin} = \frac{W}{L}\mu C_{diel}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{8}$$

Equation (8) is valid in the linear regime, however the drain current in the linear and saturation regimes will follow different relations due to the pinch-off at saturation which results in an effective maximum drain-source voltage of $V_{DS} = V_{GS} - V_{Th}$. Substituting this expression for V_{DS} into Eq. (8) yields for the saturation drain current

$$I_{D,sat} = \frac{W}{2L}\mu C_{diel}(V_{GS} - V_{Th})^2. \tag{9}$$

Then, taking the derivative with respect to V_{GS} and rearranging Eqs. (8) and (9) gives the following expressions for the calculation of the charge-carrier mobility in the linear and saturation regimes, respectively,

$$\mu_{lin} = \frac{L}{C_{diel}WV_{DS}}\frac{\partial I_D}{\partial V_{GS}}, \tag{10}$$

$$\mu_{sat} = \frac{2L}{WC_{diel}}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2. \tag{11}$$

In these equations, L is defined as the distance between the source and drain electrodes, and W is the width of the electrodes perpendicular to the channel. In an ideal device, the values for the μ_{lin} and μ_{sat} are identical, however in devices which have a significant contact resistance, μ_{lin} is substantially lower than μ_{sat}. Any resistance at the contacts will result in a reduced effective V_{DS}. Since in the linear regime, the potential between source and drain electrodes is already quite small compared to the saturation regime, this regime is affected to a larger degree by contact resistance, the causes of which are discussed in Sec. IV.

C. Metrics for high performance OFETs

In evaluating the performance of an OFET device, a high field-effect mobility is a signature of good performance

since its value dictates the applications that the OFET can address. Nevertheless, a high mobility is not sufficient, and additional characteristics are necessarily considered as well. The on/off current ratio must be maximized in order for the OFET to truly act as an on/off switch that introduces a clear difference between the "on" state and the "off" state: a target value is above 10^6. The threshold voltage, V_{Th}, provides an indication of the operating voltages of the device, and for OFETs to remain cost-efficient, V_{Th} should be close to 0 V. An abrupt turn-on region is obtained in devices with a low concentration of shallow traps, a property reflected in a small subthreshold swing, S. A low value for S allows the use of these devices at faster switching speeds, which is essential to many applications. A reasonable value for the subthreshold swing is 1 V/dec, however, many high-performance devices operate with a value less than 0.5 V/dec.

III. MATERIALS FOR OFETs

A. Organic semiconductors

Organic semiconductors are commonly classified into two broad categories: small molecules and polymers. Small molecules are oligomers made up of a finite number of conjugated monomer units, while polymers consist of several conjugated monomer units forming long chains and sometimes more complicated structures. The structure of the fundamental repeating monomer units dictates the processability and properties of polymers. Depending on the type of charge carriers that they predominantly transport in devices, these materials can be further sub-categorized as semiconductors that allow for p-type, n-type, and ambipolar transport channels when incorporated in OFETs. Organic semiconductors are intrinsic semiconductors, thus, in principle they can all yield ambipolar OFETs given that the right contact is chosen. Nevertheless, this is not always the case, since several extrinsic factors can limit transport to unipolar. Several recent review articles cover this topic and can serve as additional resources for interested readers.[29,30,45–48] This section will provide a brief discussion on materials that can be incorporated in the semiconductor layer in OFETs, including small molecules, polymers, doped organic semiconductors, charge transfer (CT) complexes, and organic semiconductor/insulator composites.
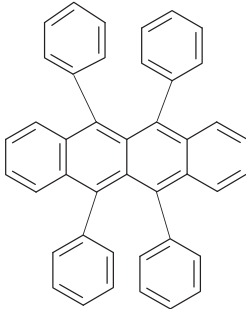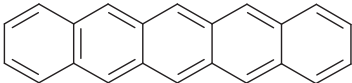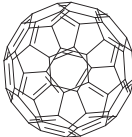
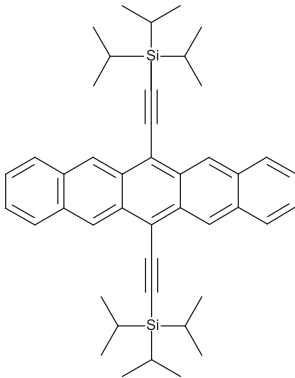### 1. Small molecule organic semiconductors
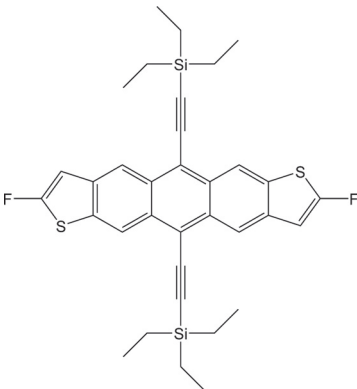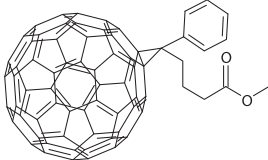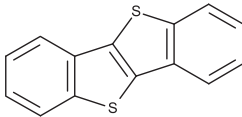
The most common small molecule organic semiconductors that function as p-type channels in OFETs are based on polyacenes and heteroacenes; several molecular structures that have gained a lot of attention are given in Table I. Pentacene and rubrene have been extensively studied in the early 2000s since their simple molecular structure consisting of only Carbon and Hydrogen made them excellent model systems.[49–61] The search for solution-processable small molecules has led to the discovery of several other classes of materials. Derivatives of pentacene modified using functionalized side groups to enhance solubility have been synthesized and tested in OFETs.[62–68] Examples include the triisopropylsilylethynyl pentacene (TIPS pentacene[62–64]), and heteroacene derivatives such as triethylsilylethynyl
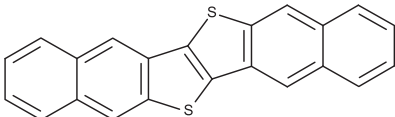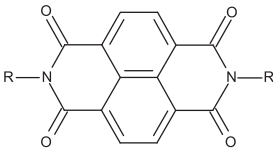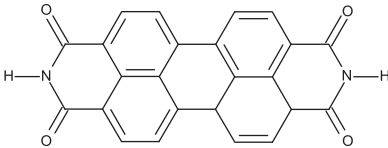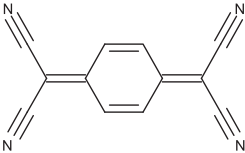
anthradithiophene (TES ADT) and di-fluorinated triethylsilylethynyl anthradithiophene (diF TES ADT).[69,70] In addition to improved solubility in common organic solvents, these functionalized materials also show improved π-stacking resulting in hole mobilities greater than 4 cm^2/Vs in solution-processed devices.[67,71] Heteroacenes consisting of fused thiophene rings in a ladder-shaped molecular structure, such as [1]benzothieno[3,2-b][1]benzothiophene (BTBT) and dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT), and their derivatives, have shown excellent p-type transport, with mobilities as high as 16.4 cm^2/Vs and 12 cm^2/Vs respectively.[72–78] The thiophene sub-structure gives rise to low-lying highest occupied molecular orbital (HOMO) levels, e.g., −5.0 eV to −5.5 eV, thereby improving stability. Hence, OFETs derived from BTBT, DNTT, and their derivatives can operate under ambient conditions without degradation.[47,79,80]

Most organic semiconductor materials favor p-type charge transport due to the difficulty in using low work function metals (2–3 eV) to inject into the lowest unoccupied molecular orbital (LUMO) of the semiconductor as the low ionization potential renders them considerably more reactive. In addition, compared to holes, electrons are more easily trapped within the semiconductor-dielectric interface or within charge trapping centers, such as grain boundaries or any other impurities, as a result of the smaller effective mass.[81] In order to realize transistors with n-type channels, there has been substantial effort to synthesize materials with lower LUMO levels (or high electron affinity) that align with the work function of air-stable metals. Fullerenes and their derivatives such as C$_{60}$ and phenyl–C$_{61}$–butyric acid methyl ester (PCBM), which have comparatively higher electron affinities, have yielded n-channel transistors with good electron mobilities.[82–84] By adding strong electron withdrawing groups such as fluorine, cyano, and diimides to the core of small molecules, the electron affinity can be significantly enhanced. Naphthalene tetracarboxylic diimide (NTCDI) and its derivatives,[85,86] perylene tetracarboxylic diimide (PTCDI) and its derivatives including dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN$_2$),[87–91] fluorinated copper phthalocyanine (FCuPC),[92] and α,ω-diperfluorohexylsexithiophene (DHF-6T)[93] are some examples of functionalized small molecules that have demonstrated stable n-channel transistors. In addition, air-stable n-type OFETs have been fabricated with single crystals of tetracyanoquinodimethane (TCNQ) yielding electron mobilities of up to 0.5 cm^2/Vs.[94] More recently, single crystal OFETs based on 2,6-dichloro-naphthalene diimide with two fluoroalkyl side chains attached to the imide nitrogens demonstrated electron mobilities as high as 8.6 cm^2/Vs.[95] For a detailed review on materials for n-channel OFETs refer to the review by Anthony *et al.*[96]

Ambipolar OFETs exhibit both p- and n-type charge transport in a single organic semiconductor layer and can serve in complementary-like circuits[97] and organic light emitting transistors.[98–100] Research is ongoing to realize ambipolar transport in OFETs either by employing p- and n-type blended or bilayer organic semiconductors,[101,102] or by utilizing suitable electrodes and bias conditions that can favor injection of both types of charge carriers.[103,104] Ambipolar transport was reported in PCBM and other fullerene derivatives, although the mobilities were very low

TABLE I. Chemical structures of small molecules utilized as p-type and n-type channels in OFETs.

p-type small molecules		n-type small molecules

Rubrene

Pentacene

Fullerene

TIPS-pentacene

diF TES ADT

PCBM

NTCDI

PTCDI

BTBT

DNTT
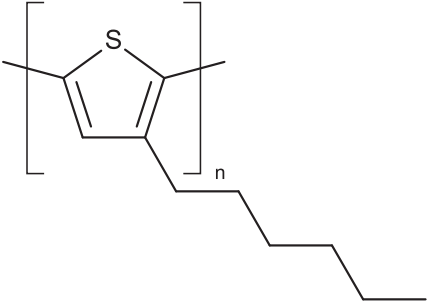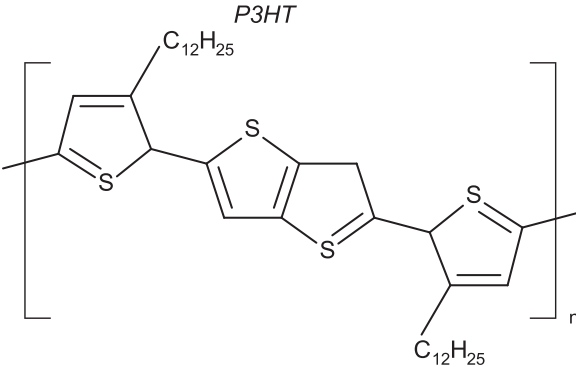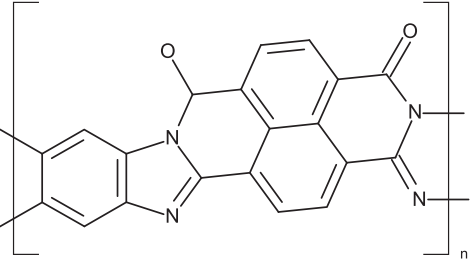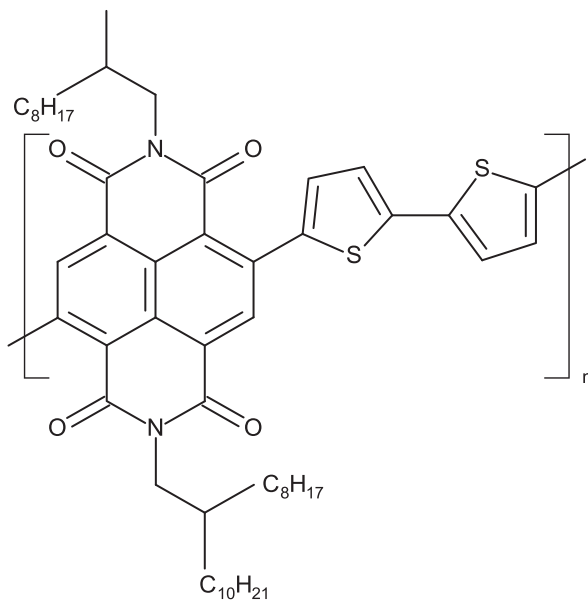
TCNQ

(10^{-5}–10^{-2} cm^2/Vs).[105–108] Single crystals such as TCNQ and rubrene have showed ambipolar transport with a vacuum gap dielectric on PDMS substrates.[109] Evaporated films of a nitrogen-substituted TIPS-Pentacene derivative exhibited ambipolar characteristics in a top-contact, bottom-gate geometry with a maximum hole mobility of 0.22 cm^2/Vs and a maximum electron mobility of 1.1 cm^2/Vs.[110] Another TIPS-Pentacene derivative, 8,9,10,11-tetrachloro-6,13-bis-(triisopropylsilylethynyl)-1-azapentacene, produced a hole mobility of 0.12 cm^2/Vs and an electron mobility of 0.14 cm^2/Vs.[111] Light-emitting OFETs displaying ambipolar behavior have also been reported, where single crystals of *p*-bis[(*p*-styryl)styryl] benzene showed a hole mobility of

0.38 cm^2/Vs and an electron mobility of 0.28 cm^2/Vs.[112] For more examples of ambipolar materials, the reader is directed to the review by Zaumseil and Sirringhaus.[113]

2. Polymer semiconductors

Polymers typically exhibit a lower degree of crystallinity, and show inferior performance compared to small molecule semiconductors. Nevertheless, most recent reports on polymer transistors have highlighted charge carrier mobilities on par with the best small molecules, as will be discussed below.[114–128]

TABLE II. Chemical structures of polymers incorporated in p-type and n-type channels in OFETs.

p-type polymers	n-type polymers

P3HT

BBL

PBTTT

P(NDI2OD-T2)

Most solution-processable polymers incorporated in p-type OFETs are based on polythiophenes, see Table II. While polythiophenes by themselves are insoluble, alkyl substituted polythiophenes such as poly (3-hexyl thiophene) (P3HT) have excellent solubility in most common solvents and have exhibited hole mobilities greater than 0.1 cm^2/Vs.[114,116,117] Poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3, 2-b]thiophene (PBTTT)[118,119] and poly(3,3$'''$-didodecylquaterthiophene) (PQT-12)[120] are other examples of polymers based on alkyl-substituted polythiophenes that show hole mobilities greater than 0.1 cm^2/Vs, as well as good air stability.

In recent years, the performance of polymer semiconductors has begun to compete intensely with that of molecular crystals composed of small molecules. Diketopyrrolopyrrole (DPP)-based polymers, namely P-29-DPPDBTE and P-29-DPPDTSE, have attained hole mobilities as high as 12 cm^2/Vs via side chain engineering.[121] Using nano-grooved substrates and the polymer poly[4-(4,4-dihexadecyl-4H-cyclopenta[1,2-b:5,4-b$'$]dithiophen-2-yl)-alt-[1,2,5]thiadiazolo-[3,4-c]pyridine] (PCDTPT), Luo *et al.* reported hole mobilities of 36.3 cm^2/Vs.[122] There are a very few polymers that have exhibited n-type transport in OFETs, one example is poly(benzimidazobenzophenanthroline) (BBL) with electron mobilities of 0.1 cm^2/Vs.[123] Recently, Zhao *et al.* produced OFETs with n-type channels using a selenophene containing polymer, PNBS, with electron mobilities up to 8.5 cm^2/Vs.[124] Electron mobilities of 6.3 cm^2/Vs have been realized with a DPP-based polymer.[129]

The donor-acceptor copolymers, consisting of two or more different oligomers polymerized together, have emerged as new paradigms for polymeric semiconductors. In spite of the lack of long-range order, these polymers outperform some of the highly-ordered semiconducting polymers synthesized so far. Examples include the copolymer of cyclopentadithiophene and benzothiadiazole (CDT-BTZ), which exhibited hole mobilities up to 3.5 cm^2/Vs,[125] or its derivative, C$_{20}$CDT-BTZ, that reached hole mobilities of up to 8.4 cm^2/Vs.[126] Other classes of copolymers are based on isoindigo (IID) or indacenodithiphene (IDT). IID copolymerized with bithiophene[130] and indacenodithiophene–benzothiadiazole copolymer (IDT-BT)[127] have attained hole

mobilities of 3.6 cm^2/Vs and a hole mobility of 14.4 cm^2/Vs was measured in the copolymer PTIIG-Np.[131] N-type transport with electron mobilities close to 1 cm^2/Vs has been observed in a donor-acceptor copolymer of naphthalenediimide and bithiophene (PNDI2OD-T2)[132] and electron mobilities of 9.7 cm^2/Vs in p2FIId-2FBT.[128]

Yun *et al.* provided an example of an ambipolar polymer semiconductor in Poly[2,5-bis(2-octyldodecyl)pyrrolo[3,4-c]pyrrole-1,4(2 *H*,5 *H*)-dione-(E)-[2,2′-bithiophen]-5-yl)-3-(thiophen-2-yl)acrylonitrile] (PDPP-CNTVT) where an electron mobility of 7.0 cm^2/Vs, and a hole mobility of 0.75 cm^2/Vs was obtained.[133] A copolymer of DBPy and biothiophene, showed ambipolar transport with an electron mobility of 6.3 cm^2/Vs and a hole mobility of 2.78 cm^2/Vs.[129] More information on donor-acceptor copolymers and recent progress in material development can be found in a review by Sirringhaus.[30]

3. Doped organic semiconductors

One way of tuning the electrical conductivity of organic semiconductors is by doping, i.e., the addition of impurities to a semiconductor material to shift its Fermi level. The impurity added to the host material can either donate electrons to the LUMO of the host (n-type doping) or accept electrons from the HOMO of the host, leaving holes behind (p-type doping). Therefore, for efficient transfer of charge carriers, it is required that the electron affinity of the dopant be greater than the ionization potential of the host for p-type doping or that the ionization potential of the donor be smaller than the electron affinity of the host for n-type doping. In general, an additional activation energy is required to generate free charge carriers even if the energy levels of the host and the dopant match well for efficient transfer of charge carriers.[134] The impact that doping can have on OFETs is many fold: it can improve saturation currents, transconductance, and stability. However, doping can also result in large off currents, thus low on/off ratios, due to the greater concentration of free charge carriers generated in the semiconductor layer.[135–137]

P-type dopants can be in the form of small molecules, polyelectrolytes, elemental species such as Br$_2$, Cl$_2$, O$_2$, metal oxides such as MoO$_3$, and Brønsted and Lewis acids.[138] One of the most common small molecule p-type dopants is F$_4$-TCNQ. This material has an electron affinity of 5.2 eV in the solid state and easily blends with many hosts.[139] Efficient p-type doping with F$_4$-TCNQ in films of P3HT has been reported in OFETs.[139] Very recently, enhanced stability, as well as high mobilities, have been reported with IDT-BT copolymers doped with F$_4$-TCNQ.[140]

Several types of n-type dopants have been realized, including elemental dopants such as Na, K, inorganic solids such as Na$_2$CO$_3$, small molecules, organic salts, anionic dopants, hydride donor molecules, and dimers.[138] Small-molecule n-type dopants with low ionization potentials are sensitive to oxidation and hence, efforts are ongoing to produce stable n-type doping with organic small molecules. The donor tetrathianaphthacene (TTN) has been used as an n-dopant for hexadecafluorophthalocyaninatozinc (F16-

ZnPc).[141] For more information on other types of dopants, the reader is directed to the review by Lüssem *et al.*[138]

4. Charge-transfer complexes

Charge transfer (CT) complexes are materials formed by combining an electron donating molecule (donor) and an electron accepting molecule (acceptor) in which the coupling between the donor and acceptor units leads to a fraction of the electronic charge being transferred between the molecules. The degree of charge transfer is determined by the ionization potential of the donor and the electron affinity of the acceptor, with the solid state packing also playing a role.[142,143] The electronic properties of the CT complexes depend on the degree of charge transfer and can vary from insulators to superconductors.[144,145] Ambipolar OFETs have been fabricated with CT complexes of TCNQ with Fullerene derivatives,[146,147] and with dibenzotetrathiafulvalene-tetracyanoquinodimethane (DBTTF–TCNQ).[143,148] For more details and examples on CT complexes, refer to the reviews by Goetz *et al.*[149] and Wang *et al.*[150]

5. Organic semiconductor/insulator composites

Another major class of organic materials that has advanced a great deal over the recent years is the composite of organic semiconductors with electrically insulating units (EIUs) in the form of non-conjugated organic moieties. EIUs have long been considered defects that hinder charge transport, but recent work proved that their careful incorporation into organic semiconductor films can, in fact, enhance OFET characteristics.[151,152] They have been used for passivation of traps and impurities at the semiconductor-dielectric interface,[151] better self-organization of the semiconductor film due to slower solvent evaporation,[151] decreased resistance at grain boundaries,[153] increasing the uniformity of device characteristics over large areas,[154] and minimizing the effects of dissimilar thermal expansion in layered devices.[155] In addition to improving performance, EIUs can impact OFETs in several other ways. For example, they can aid in solution processability, enhance environmental and electrical stability, improve mechanical properties, or self-organize as gate dielectrics.[151] EIUs can be either covalently attached to the organic semiconductor through chemical synthesis or they can form semiconductor/insulator blends by simple processing. A combination of small-molecule and polymer blends along with a chemical dopant has been realized to achieve a hole mobility of 13 cm^2/Vs.[156] For a review of various other OFETs fabricated using semiconductor/insulator blends with small molecules and polymers, refer to the review by Kang *et al.*[151]

B. Deposition methods for the organic semiconductor

Organic semiconductors can be deposited either from the vapor or solution phase, depending on their vapor pressure and solubility. Different deposition methods can result in different film morphologies and molecular structures which in turn can cause varying device performance.

1. Single crystal growth

The first single crystal OFETs were based on tetracene[157] and pentacene.[158] Single crystals grown from the vapor phase are of very high purity due to the lack of solvents involved in the growth process. They can be grown in two ways, either by vacuum sublimation or by physical vapor transport (PVT).[159,160] Vacuum sublimation involves sublimation of a semiconductor powder inside a clean quartz tube with one end sealed and the other end connected to a vacuum pump in the presence of a temperature gradient. Convection currents cause the sublimed material to recrystallize in a cooler region of the temperature gradient. In the PVT technique, an inert gas at ambient pressure carries the sublimed material to a cooler region. The morphology of the crystals depends on the shape of the tubes and the temperature gradient. Single crystals form a highly ordered microstructure with no grain boundaries that hinder charge transport. Hence, they ensure high device performance and can serve as model systems to determine benchmark electrical properties for a given material. However, their electrical properties vary significantly depending upon their crystallographic orientation giving rise to anisotropy.[161–163] Due to their ultra-pure form, single crystals grown from the vapor phase, such as rubrene, have been reported to have mobilities as high as 20 cm^2/Vs in OFETs.[58–61] For an overview of organic single crystal field-effect transistors, refer to the review by de Boer *et al.* and the editorial by Podzorov.[69,164–167]

The main bottleneck for realizing single crystal OFETs practically is the difficulty in growing large-sized organic crystals with controlled dimensions. Additionally, fabrication of single crystal OFETs involves the growth of the crystals followed by the careful placement and orientation of the fragile crystals by hand on suitable substrates which, again, limits their potential use in industrial applications. Efforts have been undertaken to grow large area single crystals from solution methods, but these crystals usually have less uniformity and coverage.[168] Ultrathin single crystals with large area coverage have been successfully grown by means of a meniscus-driven solution-based crystal growth technique.[169] OFETs based on these crystals yielded hole mobilities as high as 10 cm^2/Vs. Nevertheless, the viability of single crystal OFETs for large scale industrial applications remains low. Hence, researchers shifted attention towards thin film technologies where single crystals are replaced by thin films of the organic semiconductor material. Even though thin films are typically of lower quality than single crystals, they can be applied over very large areas and hence have more technological appeal.

2. Thermal deposition

Sublimation under vacuum is a process used to deposit and/or purify small organic molecules in the form of thin polycrystalline films. Until the emergence of solution-based deposition techniques, thin films of organic semiconductors were exclusively deposited using this process. In this technique, the material is placed under high vacuum, typically in the range of 10^{-8} to 10^{-6} Torr, and heated to cause sublimation, followed by condensation on a substrate forming thin films. The vacuum ensures the vapor particles travel directly to the substrate without deflection as well as evacuates any contaminant gases such as oxygen that could react with the material. Small molecules, such as pentacene, that are insoluble in common organic solvents are deposited using this technique.[56] Thermally deposited films have high uniformity and good reproducibility. Additionally, deposition of several layers of organic semiconductors without destroying the underlying layers is possible. An example is the flexible transistors obtained using evaporated diphenyl-dinaphtho[2,3-*b*:2′,3′-*f*]-thieno[3,2-*b*]thiophene (DPh-DNTT) fabricated on a self-assembled monolayer (SAM)-based dielectric, which showed remarkable resilience under thermal stress and a 2 V operating voltage.[79] Another instance of evaporated DNTT derivatives resulted in mobilities up to 8.0 cm^2/Vs using 3,10-C$_{10}$DNTT.[170]

Vacuum sublimation of the active semiconductor layer has already been used commercially in the fabrication of large-area, full-color organic displays made of OLEDs.

3. Solution deposition

Solution deposition methods are compatible with ambient temperatures and pressure and hence can be used without incurring the significant infrastructure costs associated with high vacuum systems. They can be compatible with large-area thin film fabrication and therefore result in lower production cost. Following are some of the standard techniques that are used to deposit organic semiconductors from solution.

The most common solution-based deposition method for thin films is spin coating. Spin coating involves depositing a small pool of semiconductor solution onto the center of the substrate and spinning the substrate at high speeds (~1000 rpm or higher). Centripetal acceleration causes the solution to spread on the substrate and finally off its edge, leaving behind a thin film upon solvent evaporation. The thickness and quality of the thin film depend on the nature of the semiconductor solution such as solvent type, surface tension, viscosity and concentration, and the spin parameters such as the spin speed and acceleration. Variations in spin parameters give rise to changes in the solvent evaporation rate during film formation and hence result in different film microstructures.[171] Additionally, the type of solvent can significantly impact OFET device performance as they too can cause variations in the film microstructure as well as create different polymorphs of the same material.[172]

Drop casting is a solution-based technique that involves dropping the semiconductor solution onto the substrate and letting the solvent evaporate spontaneously on its own, leaving behind individual crystals or thin films. This technique is much simpler than spin coating with less material wastage. However, the film coverage is non-uniform and the thicknesses of the films are hard to control. Modifications to the traditional drop casting method have been made in order to improve the quality of films and crystals. Vibration-assisted crystallization (VAC) relies on vibrating the substrate at a controlled frequency and amplitude during film crystallization.[173] Gentle vibrations provide sufficient energy for the molecules to escape metastable potential energy minima and settle into the minimum potential

energy configuration with the highest degree of order. Another modified drop casting technique is solvent-assisted crystallization (SAC) which involves film crystallization in the presence of a solvent rich environment, thereby controlling the rate at which solvent evaporates. This is typically done in a petri dish containing the drop cast substrate with additional solvent dropped around it.[174]

Spray coating has a key advantage of being high throughput and compatible with large area processing. This technique employs an inert carrier gas to convert the small droplets of solution into aerosols and eject them from a nozzle to direct them onto the substrate. Hence, the shape and size of the nozzle, as well as the pressure of the gas, are important processing parameters. Spray coating is an industrial technique employed in obtaining high-quality thin films on large area substrates and was successfully demonstrated for OFET fabrication.[65,154,175–179]

Inkjet printing is a low-cost solution-based technique useful in large-area processing and is compatible with flexible substrates. It involves the deposition of a jet of ink in the form of small droplets onto a substrate which is ejected from a chamber via a piezoelectric or thermal process. The ink-substrate interaction influences the pattern formed on the substrate and hence the surface energy of the substrate as well as the viscosity of the printing solution are some of the key processing parameters. Charge carrier mobilities as high as $16.4 \, cm^2/Vs$ have been attained with inkjet-printed single crystal OFETs based on 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C(8)-BTBT).[77]

Solution shearing is another popular coating method that involves moving a shearing blade containing an organic semiconductor solution above a temperature-controlled substrate. The blade is moved relative to the substrate at a fixed speed, allowing the solvent to evaporate and thereby forming thin films. This technique has been used in the formation of strained molecular packing which lead to improved hole mobilities of up to $4.6 \, cm^2/Vs$ in TIPS-pentacene.[71]

4. Laser printing

Laser printing is a low-cost, highly scalable, large-area technique that can be used for simultaneous patterning and coating. It involves the transfer of a toner in the form of a fine powder onto a flexible substrate such as paper or plastic to form the desired pattern. This is achieved via temporary transfer to an organic photoconductor drum that is selectively discharged using a laser within a printer. This technique is ubiquitous in other areas but has only recently been explored for electronic device fabrication when Diemer *et al.* built the first laser printed OFET based on a toner formulated with TIPS-pentacene organic semiconductor using a commercially-available laser printer.[7] The first generation devices showed charge carrier mobilities on the order of $10^{-3} \, cm^2/Vs$, which is quite low but on par with the first vacuum deposited OFETs. Further improvement of this technique in terms of toner formulation and instrument design will most likely lead to better device properties and appeal to technological applications.

C. Dielectrics

In rigid devices, where the focus is not on flexibility, many different dielectrics can be used including the standard, silicon dioxide (SiO_2). SiO_2 has been incorporated for decades in the ubiquitous silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) and has been commonly used in OFETs as well due to the ease of processing. One of the drawbacks of using SiO_2 as a dielectric in OFETs, however, is that the chemical structure of SiO_2 contains a significant amount of surface states which can act as charge traps. Passivation of the silicon oxide surface can circumvent the effects of these traps and allow more efficient device operation.[81]

The choice of the dielectric material depends heavily on the desired application, as the use of a flexible substrate will require a flexible dielectric as well. Dielectrics compatible with flexible substrates include Cytop,[115,180,181] divinyltetra-methyldisiloxane-bis(benzocyclobutene) (BCB),[44,182] poly (methyl methacrylate) (PMMA),[183] self-assembled monolayers and hybrids thereof.[56,184–186] Several properties of the dielectric layer are relevant for OFET operation. A reduced roughness at the interface with the semiconductor limits charge scattering and thus the density of electronic traps in the transistor channel.[187] The dielectric constant and thickness also play important roles. High-k dielectrics (inorganic, organic, and electrolytes) were developed and used in organic devices,[188–197] however such a highly polarizable material can cause charge scattering and reduce device performance via the formation of Frölich polarons.[38,198] Nevertheless, a low-k dielectric results in a lower capacitance and therefore diminished charge accumulation, requiring higher voltages for device operation. Several solutions have been proposed for this problem: the large operating voltages can be reduced by decreasing the dielectric thickness, however creating high quality dielectrics thinner than 100 nm is practically impossible because of the inherent formation of pinholes that lead to high leakage currents. The use of SAM dielectrics has proven an effective way to minimize operating voltages and sub-threshold swings.[56,186,199–203] The monolayers form a dielectric layer of thicknesses ranging from 2 to about 10 nm, depending on the length and orientation of the SAM, and when they are densely packed, leakage currents are extremely low (less than $10^{-8} \, A/cm^2$).[186] Their capacitance can reach $1 \, \mu F/cm^2$,[204] which is one order of magnitude higher than the value typically used in OTFTs (17.3 nF/cm^2, corresponding to 200 nm SiO_2 dielectric), and thus the same charge can be accumulated in the transistor channel at 10 times lower V_{GS} [see Eq. (4)]. Another strategy implies the use of bilayered or multilayered dielectrics comprising of a high-k layer and a low-k dielectric at the interface with the semiconductor,[205–207] or the use of electrolyte gating.[196,197,208–211]

D. Contacts

1. Charge injection in OFETs

Choosing the proper contacts for an OFET is of the utmost importance to achieving good device performance. The goal is to obtain an ohmic contact, or one that results in a

negligible voltage drop and should be able to act as a charge carrier reservoir. Charge injection is largely determined by the alignment between the work function of the contact W_F and the HOMO/LUMO levels of the semiconductor, Fig. 4. The injection barrier Φ_B depends on the difference between W_F and the HOMO for p-type channels (W_F and the LUMO for n-type), but its magnitude is influenced by many complex effects, including the formation of interface dipoles and charge transfer between interfaces brought into contact. Since most organic semiconductor materials are intrinsically ambipolar, the alignment of W_F with the HOMO/LUMO levels can, in principle, determine if a device operates as p-type, n-type, or ambipolar. In p-type devices, W_F of the electrode aligns with the HOMO of the organic semiconductor, in n-type with the LUMO, and ambipolar transport requires that W_F lies in between the HOMO and LUMO levels. Such a simplistic band diagram does not always guarantee the predicted type of injection because of the afore mentioned extrinsic effects.[212]

Alignment of the contact work function and the semiconductor HOMO/LUMO levels is not trivial since the work function is a surface property and is subject to environmental effects. The electron cloud of a bare metal extends slightly into vacuum, creating an electric field oriented away from the metal. Any charge entering or leaving the metal will have to overcome the potential of this electric field, an effect that the work function accounts for. When a new material is brought near to or in contact with the metal, the electron cloud of the new material pushes back the electron cloud of the metal. This changes the magnitude of the electric field at the surface and therefore the work function. This is known as the push-back or pillow effect.[213] Additionally, two materials brought in contact most often have different Fermi energies, and they will establish a common Fermi energy (i.e., thermal equilibrium) by exchanging carriers. A depletion or accumulation zone (depending on the relative Fermi energies) forms in the semiconductor creating an additional electric field. This is commonly known as band bending, and it is schematically shown in Fig. 4.[214–217] This new electric field also alters the work function, shifting the injection barrier.

Since the Fermi energy of an intrinsic semiconductor is positioned between the HOMO and LUMO energies, attempting to match a metal with a work function close to one of these bands will cause significant charge transfer to occur to establish equilibrium. This, in turn, shifts the HOMO and LUMO levels and an energy barrier remains, an effect known as Fermi level pinning.[218,219] With these and other effects, it is impossible to predict the energy level alignment at the contact/semiconductor interface given only the contact work function and semiconductor HOMO/LUMO levels, making the contact selection difficult. For more information on contact energetics, the reader is directed to the works by Natali and Caironi,[218] Knupfer and Paasch,[213] and Gundlach *et al.*[212]

Traditionally, charge injection into semiconductors has been characterized by the same theories that describe electron emission from a metal into vacuum. There are two models: thermionic emission, following the Richardson-Schottky formulation, and field emission, which converges to Fowler-Nordheim tunneling in the low temperature limit. Thermionic emission occurs when charge carriers have sufficient energy to overcome the injection barrier and is applicable for moderate temperature and applied electric field. Field emission, more applicable at low temperature and/or high applied electric field, is a quantum mechanical tunneling effect where charges do not need to have energy greater than the barrier. Deciding on the more appropriate model is not trivial, and there is an intermediate region where both processes make significant contributions to emission. Studies by Murphy and Good,[220] and later Christov,[221] show that the boundaries of each model are dependent on temperature, injection barrier, and the strength of the applied electric field. In general, the upper bound on electric field strength for thermionic emission (and lower bound for field emission) increases with temperature and injection barrier. Since these models were developed for emission into vacuum, they may not be directly applicable for injection into an organic semiconductor,[222] although the general characteristics still seem to hold. For example, crossovers from thermal to field emission have been found theoretically by increasing the applied
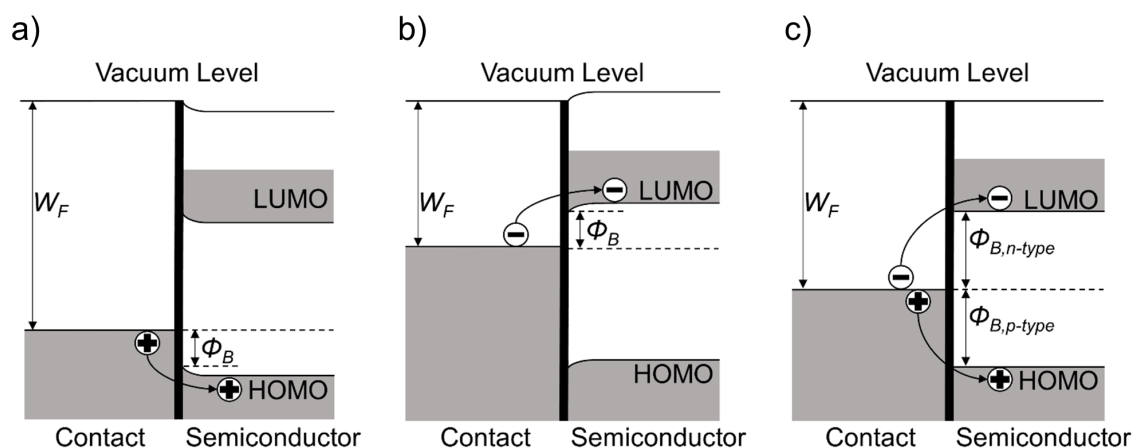
FIG. 4. The injection barrier Φ_B is the difference between the work function of contact and the corresponding semiconductor band. (a) Holes are injected into the semiconductor HOMO in a p-type device. The proximity of W_F to the HOMO level causes energy level bending, shifting the level from its nominal value at the interface. (b) Electrons are injected into the semiconductor LUMO in a n-type device. (c) A work function in between the HOMO and LUMO levels can facilitate ambipolar transport, though injection barriers will always be larger than in the corresponding unipolar device. Energy level bending is minimal when W_F is near the Fermi level of the semiconductor.

field[223] and experimentally by decreasing the temperature.[224] Others have found limiting behavior similar to thermionic and field emission.[225,226] Still, at a metal/semiconductor interface, a third injection mechanism is possible as charges can hop through localized states into the bulk. It is most likely that the injection process into organic semiconductors is a combination of all three mechanisms, described as thermally assisted tunneling through localized states.[222,227] For further discussion on charge injection theory, the reader is directed to the review by Scott.[222]

Metallic contacts are often used due to their chemical stability, reliable processing, and well-known properties. These include gold, silver, copper, platinum, calcium, and aluminum, among others, and are generally deposited through thermal or electron-beam evaporation in high vacuum. In the pursuit of all-organic or printable devices, several groups have experimented with using organic metals as the electrodes or as a surface treatment to other metallic electrodes.[228] One example is poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS), a solution-processable macromolecular salt[229] that can exhibit high conductivities (up to 3065 S/cm).[230] Another class of compounds that falls into the organic metal family is charge-transfer (CT) complexes,[149,231,232] which have garnered considerable attention due, in part, to the relative ease of work function modification through chemical substitution, as exemplified by the transition from p-type, to n-type, and finally to ambipolar behavior on the same semiconductor through manipulation of the donor and acceptor constituents.[148] One issue that arose with the use of CT complexes, however, is their low solubility in common organic solvents. One approach to overcome this challenge was introduced by Hiraoka *et al.* through the use of "double-shot inkjet printing," where the more soluble donor and acceptor components were individually deposited and the CT complex was allowed to form on the substrate.[233] π-conjugated carbon in the form of carbon nanotubes or graphene is also gaining considerable interest as an electrode material in OFETs due to the reduced injection barrier stemming from the interfacial morphology as well as possibly aiding in the growth of an overlaid organic semiconductor.[234–240]

2. Tailoring contact properties by chemical treatment

Chemical modifications of metallic contacts can create a tunable and sometimes more favorable interface for charge injection into the organic semiconductor. Metal oxides such as molybdenum oxide and titanium oxide were used to modify the work function by a large degree in either direction.[219,241,242] Charge transfer salts[149,228] and SAMs[52,63,243–246] can also shift the work function of the source and drain electrodes and can impact the semiconductor morphology.[246,247] Two reports have proposed robust strategies that are generally applicable to a large number of semiconductors and yield low, or high work function electrodes, respectively.[248,249] The first relies on treatment of the electrode surface with polymers containing aliphatic amine groups, while in the latter, an interlayer inserted between the electrode and semiconductor ensures

electrostatic decoupling of the two and, consequently, a shift in the Fermi level.

Another method for work function tuning is through treatment with polar SAMs, usually thiol-based small molecules.[218] The SAM adheres spontaneously to the metal surface as the thiol group forms a covalent bond with metals. The presence of the SAM modifies the local electric field at the surface of the electrode by creating a dipole at the interface. The electric field of this dipole, combined with the polar dipole of the SAM itself, changes the work function of the contact. The sign and magnitude of the SAM dipole, together with the degree of order and orientation of the SAM molecule on the surface, determines the work function shift.[37,200,250] In general, alkane terminals decrease the work function while halogenated terminals increase the work function.[251] The work function can be further fine-tuned using a blend of SAMs.[245] The surface potential, and therefore the work function, resulting from a SAM assembled on an electrode can be measured through ultraviolet photoelectron spectroscopy (UPS)[37,252,253] or Kelvin probe microscopy (KPM).[247,251]

IV. CONTACT RESISTANCE IN OFETs

A. The origin of contact resistance in OFETs

The models adopted for OFET characterization assume a negligible contact resistance, and thus it is important to recognize the non-idealities that may be present in real OFETs in order to aid in device design and to ensure that the extracted device parameters are correct. With the advent of new semiconducting materials with high intrinsic mobilities and correspondingly low channel resistances, R_{Ch}, the impact of contact resistance, R_C, became much more significant. In addition, the focus on device downscaling has exacerbated this issue as the channel resistance decreases, yet the contact resistance remains constant with smaller channel length. The contact resistance originates from the fact that a finite voltage is necessary to transfer the charges from the electrode surface into the semiconductor and vice versa, see Fig. 5. For an OFET to function as described in Sec. II B, which grants the use of standard models for the extraction of device parameters, the resistance due to the contacts must be substantially lower than the resistance due to the channel. If this is not the case, the voltage drop at the contacts results in a smaller effective potential across the channel. There exist two main contributions to the contact resistance: charge
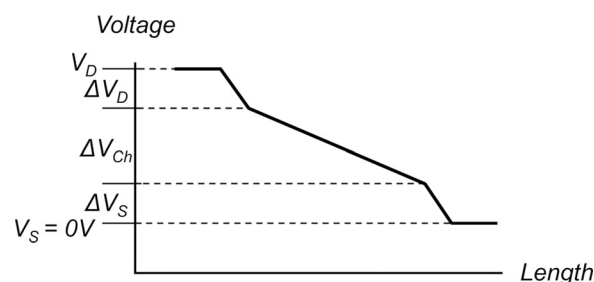
FIG. 5. The voltage dropped across the channel (V_{DS}) consists of the voltage dropped at the source electrode (ΔV_S), at the drain electrode (ΔV_D), and in the channel (ΔV_{Ch}).

injection from the contacts into the organic semiconductor layer ($R_{C,int}$), and charge transport in the semiconductor from the electrode interface to the device channel ($R_{C,bulk}$).[212] While the injection barrier is the main source of $R_{C,int}$, additional factors can have a significant effect, as described in Sec. III D. The bulk resistance $R_{C,bulk}$, or the resistance due to the depleted semiconductor between the contacts and the conducting channel, can be reduced through device geometry. In a staggered device geometry, Figs. 1(b) and 1(c), injection occurs along the electrode surface parallel to the channel; as the gate voltage is increased, more of this surface participates in injection due to increased channel conduction, effectively reducing R_C. In the next step, the injected charges migrate from the electrode surface to the channel, thus the thickness and conductivity of the semiconductor layer in the direction perpendicular to the channel determine $R_{C,bulk}$. In contrast, in coplanar devices, Figs. 1(a) and 1(d), injection occurs directly into the channel along the electrode surface perpendicular to the channel. This eliminates $R_{C,bulk}$, but the injecting surface is limited to the thickness of the conduction channel, typically only a few nanometers. Generally, long channel-length (50–100 μm) devices with mobilities around $1\,\mathrm{cm^2/Vs}$ will not display significant contact effects as long as R_C is less than a few kΩcm, however as mobilities increase past $5\,\mathrm{cm^2/Vs}$, R_C must be less than $1\,\mathrm{k\Omega}$ cm. At small channel length, the restriction on these resistance values is even greater, especially at high frequencies.[254]

B. Mobility underestimation and overestimation due to large contact resistance

Depending on the source and magnitude of contact resistance, extracting the mobility from current-voltage characteristics can lead to both underestimation and overestimation, as described in detail in the excellent study by Liu *et al.*[255] Mobility overestimation was also proposed to arise from minority carrier injection and trapping, and discussed in several manuscripts.[256] Here, we will expand on the case where a large contact resistance can result in non-ideal current-voltage characteristics that can lead to mobility overestimation. One example is shown in Fig. 6, where the $I_D^{1/2}$ vs. V_{GS} curves exhibit a "kink," where the current first abruptly increase and then reaches a steady state.[257,258] Such device characteristics lead to an overestimation of the field-effect mobility if the value for $\frac{\partial\sqrt{I_D}}{\partial V_{GS}}$ is extracted in the low voltage regime (red line), and the true mobility in this example corresponds to the dotted blue line. The mobility is overestimated by 6 times in this example, but the overestimation can be greater than one order of magnitude in other cases. This phenomenon was attributed to a large injection barrier at the contacts, leading to a very large contact resistance, i.e., the gated Schottky contacts.[257–260] The contact resistance may, in some cases, exceed the channel resistance, but it is reduced with increasing V_{GS}, and access to the intrinsic mobility of the semiconductor is now possible. Since the accuracy of the mobility value extracted from OFET analysis depends on the use of the appropriate device models, contact engineering to reduce contact resistance should be employed
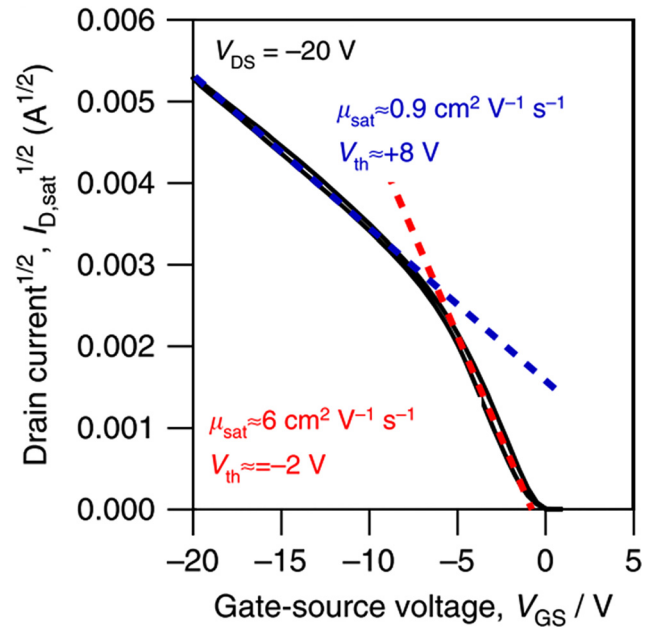

FIG. 6. An $I_D^{1/2}$ vs. V_{GS} curve showing the overestimation of the mobility due to gated contacts. Reproduced with permission from Bittle *et al.*, Nat. Commun. **7**, 10908 (2016). Copyright 2016 Macmillan Publishers Ltd.[257]

immediately when one is faced with such device characteristics. For example, Uemura *et al.* reduced contact resistance through a contact-annealing procedure which resulted in a shift from highly non-ideal current-voltage curves to the expected linear relation of $I_D^{1/2}$ vs. V_{GS}.[259] If, however, a more ideal electrical characteristics cannot be obtained, plotting the evolution of mobility with V_{GS} can minimize the errors. An abrupt increase, followed by a peak mobility, then a continuous decrease is problematic and should be avoided. Nevertheless, if the mobility first increases, but then reaches a plateau (with or without a peak between the two regimes), the plateau value should be considered as the device mobility.

C. Models for evaluation of contact resistance in OFETs

1. Gated transmission line method (gated TLM)

Several techniques have been developed to measure contact resistance both directly and indirectly. An example of an indirect method is the gated transmission line method (gated TLM), which relies on the assumption that the organic semiconductor is uniform and isotropic, and thus the channel resistance scales linearly with the channel length.[206,212,219,253,261,262] In this technique, the total resistance of the device R_{device} is extracted at a given applied gate voltage by taking the value of I_D at a particular V_{GS} in the linear regime transfer curve and dividing by the applied V_{DS} [Fig. 3(a)]. This procedure is repeated for devices of differing channel length L and since R_{device} is given by the series combination of the contact resistance (independent of the channel length), and the channel resistance (directly proportional to the channel length)

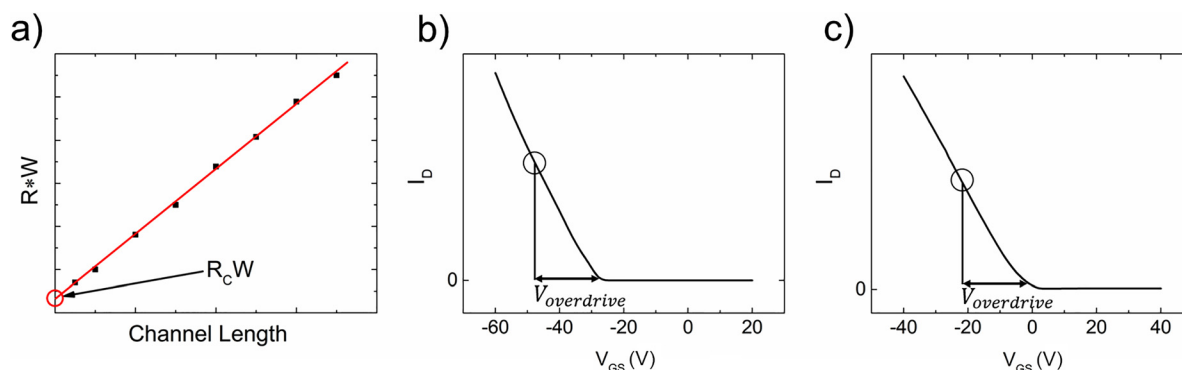$$R_{device} = R_C + R_{Ch}(L), \tag{12}$$

FIG. 7. (a) Example gated TLM graph showing the determination of the contact resistance. (b) and (c) Two devices with different threshold voltages, highlighting the necessity of the overdrive voltage.

by plotting the R_{device} vs. L and extrapolating to $L = 0$ (y-intercept), R_C is extracted, Fig. 7(a). To account for the different device geometries, the width-normalized device resistance $R_C W$ is generally used [see Fig. 7(a)]. The contact resistance is dependent on the gate voltage, therefore, it is important that the devices are compared at the same effective V_{GS}. To minimize the errors due to the fact that each device has a different threshold voltage, thus will experience a different effective gate voltage, the drain current must be measured at a particular value of V_{GS} called the overdrive voltage to ensure consistency between devices ($V_{GS} - V_{Th}$ $= V_{overdrive}$).[262] Figures 7(b) and 7(c) show two devices with different V_{Th} in the linear regime highlighting the importance of the overdrive voltage.

2. Scanning Kelvin probe microscopy (SKPM)

Another method of measuring contact resistance uses scanning Kelvin probe microscopy (SKPM) with a metal-coated atomic force microscope (AFM) tip to measure the surface potential across the channel of a biased device during operation.[263–267] This measurement provides direct access to the value of the drain current and the voltage drop at the contacts, as shown in Fig. 5, and thus the contact resistance can be extracted from the ratio of the two. An example is provided in Fig. 8, where devices using contacts of two different materials were examined using SKPM and the larger contact resistance of Ni compared to Pd is clearly seen in the significant voltage drop at the contact in Fig. 8(a).[265] The difference between the contact work function and the pentacene HOMO level is much greater with Ni than with Pd, leading to the large injection barrier. Then, the output characteristics in Fig. 8(b), show a drastic reduction in drain current when using Ni contacts, reflecting the considerable resistance to injection. The limitation of this technique is that it can only be used in device configurations where the contacts and the channel are accessible with the SKPM tip.

3. Impedance spectroscopy (IS)

Impedance spectroscopy (IS) is the measurement and analysis of the linear electrical response of materials; a general review of theory and technique is available in the work by Macdonald.[268] In terms of organic transistors, impedance spectroscopy allows for precise measurement of the contact

resistance R_C and the ability to correctly evaluate the channel mobility even in devices dominated by contact resistance.[257,269–271] A great advantage of this method is that it only requires a single device, as opposed to the multiple devices required for gated TLM. A much larger statistical data set can therefore be obtained with the same number of
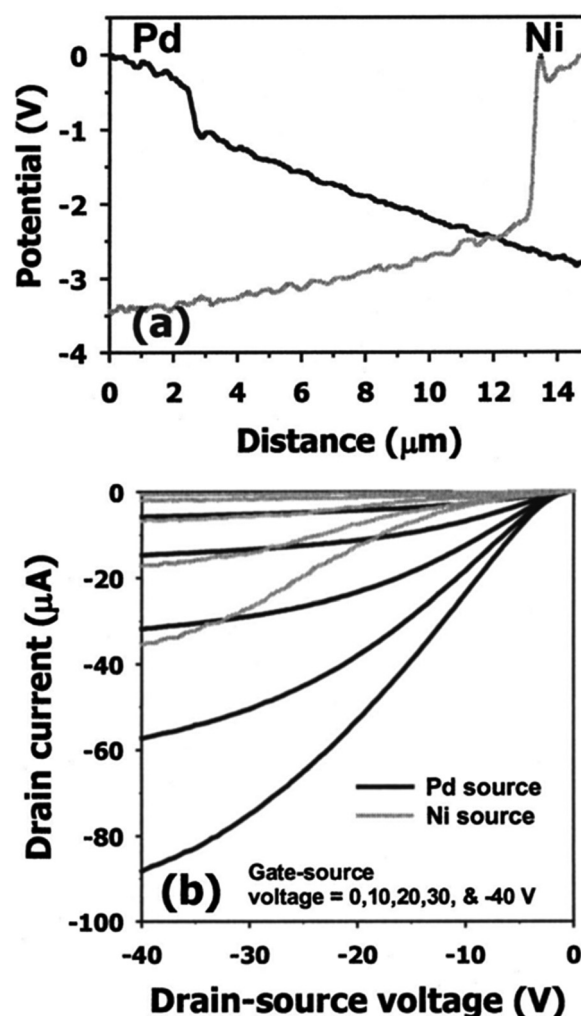

FIG. 8. An SKPM study on the effects of different contacts. (a) A line scan across the semiconducting channel showing the potential drop at contacts of differing materials. (b) The effect of different contact potential drops on the output characteristics. Reproduced with permission from Nichols, *et al.* Appl. Phys. Lett. **83**, 2366–2368 (2003). Copyright 2003 AIP Publishing LLC.[265]

devices and without relying on device-to-device uniformity; however, the accuracy of the results hinges on the proper choice of the equivalent circuit model for the organic transistor. A transmission line model adapted from inorganic metal-oxide-semiconductor (MOS) devices and modified by a parallel RC circuit at the drain and source contacts, Fig. 9, has been found to provide excellent fits to data.[269] The RC circuit models the contact resistance and capacitance (R_C and C_C), while the transmission line models the channel resistance R_{Ch} and the interface and oxide capacitance per unit area c_i and c_{ox}. The interface capacitance in an organic transistor arises from traps at the semiconductor-dielectric interface,[269] while the oxide capacitance is simply the capacitance of the dielectric. Note that c_{ox} is either directly measured or calculated by dividing the dielectric's permittivity by its thickness. The total impedance Z_T of this circuit can be separated into two parts

$$Z_T = Z_C + Z_{Ch}, \tag{13}$$

where Z_C is the impedance of the contact and Z_{Ch} is the impedance of the channel. Circuit analysis gives[257]

$$Z_C = \frac{jR_C}{j - \omega R_C C_C}, \tag{14}$$

$$Z_{ch} = \frac{1}{j\omega WLc'} \lambda \coth\lambda, \quad \lambda = \sqrt{\frac{1}{4}j\omega c' r L^2}, \tag{15}$$

where j is the imaginary unit, W and L are the width and length of the channel, respectively, and r is the sheet resistance, which is related to the channel resistance by

$$dR_{Ch} = \frac{r}{W} dx. \tag{16}$$

The parameter c' is given by

$$c' = \frac{c_{ox}c_i}{c_{ox} + c_i}. \tag{17}$$

An alternative circuit model proposed by Zaki *et al.* relies on the transconductance g_m of the device, and has been shown to produce accurate predictions of device resistance, capacitance, mobility, and transfer frequency.[271]

Impedance spectroscopy is most easily carried out with an LCR meter, capable of performing the necessary frequency and voltage scans. For measurement, the source and drain contacts are shorted and the gate is DC-biased in the
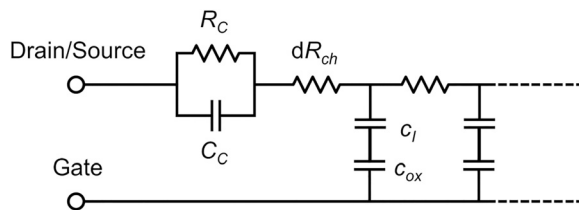

FIG. 9. Contacts are represented through a parallel RC circuit, while the TLM models the channel resistance and the capacitance of the semiconductor/insulator interface. Note that the drain and source contacts are shorted to form a single node. A DC voltage with a small AC signal is applied to the gate.[257]

linear regime along with a small AC signal, typically 25–100 mV.[257,269,270] The DC bias is stepped through its range, and at each point the AC frequency is swept typically from Hz to the MHz range. The LCR will record the inductance, capacitance, and resistance of the device, i.e., the real and imaginary parts of impedance Z_T, and parameters are extracted from fits to this data.

Contact resistance R_C and channel resistance R_{Ch}, along with the other parameters described in Eqs. (14)–(17), can be individually derived from fits of Eq. (13) to data.[257] Mobility can be calculated from the sheet resistance r and the accumulated charge in the transistor channel Q_I. The amount of accumulated mobile charge is found by integrating the area under the C–V_{GS} curve[269]

$$\mu = \frac{1}{Q_I r}, \quad Q_I = \int_\infty^V c' dV_{GS} \approx \sum_\infty^V c' \delta V_{GS}, \tag{18}$$

where r and c' are given by the data fit. This method has been shown to produce reliable mobility estimates even in the low gate voltage regime, which is typically dominated by contact resistance in DC current-voltage measurements.[257] However, it is still not completely free from contact effects; at low frequency, AC measurements approach the DC regime and are subject to the same issues. Contact resistance limits charge accumulation in the channel, affecting the fit of r and therefore the calculated mobility. Typically, an apparent increase in mobility is observed with decreasing frequency.[257]

D. Four-point probes: A method for reducing the impact of contacts

In a standard OFET characterization, where two probes (the source and the drain) are responsible for both the current and voltage data, the measurements of charge injection and conduction are intertwined; four-point probe set-ups can disentangle the two. The gated linear four-point probe provides an easy means of measuring contact and channel resistance,[272] as well as mobility,[273] while the more recently developed gated van der Pauw (gVDP) method allows for extremely precise mobility and threshold voltage determination independent of the magnitude of the contact resistance.[274]

1. Gated linear four-point probes

The gated linear four-point probe uses the BGTC or BGBC transistor layouts, with two additional "sense" probes placed at 1/3 and 2/3 the length of the channel, as shown in Fig. 10.[272] Note that these probes are typically placed on the side of the channel and penetrate slightly into the channel, and ideally are point-like. When a linear potential in the channel is assumed, measurement of the voltage at these sense probes (V_1 and V_2) allows for estimation of the contact resistance, as detailed below. The voltage drop across the source contact is

$$\Delta V_S = \left[V_1 - \frac{V_2 - V_1}{L_2 - L_1} L_1 \right] - V_S, \tag{19}$$
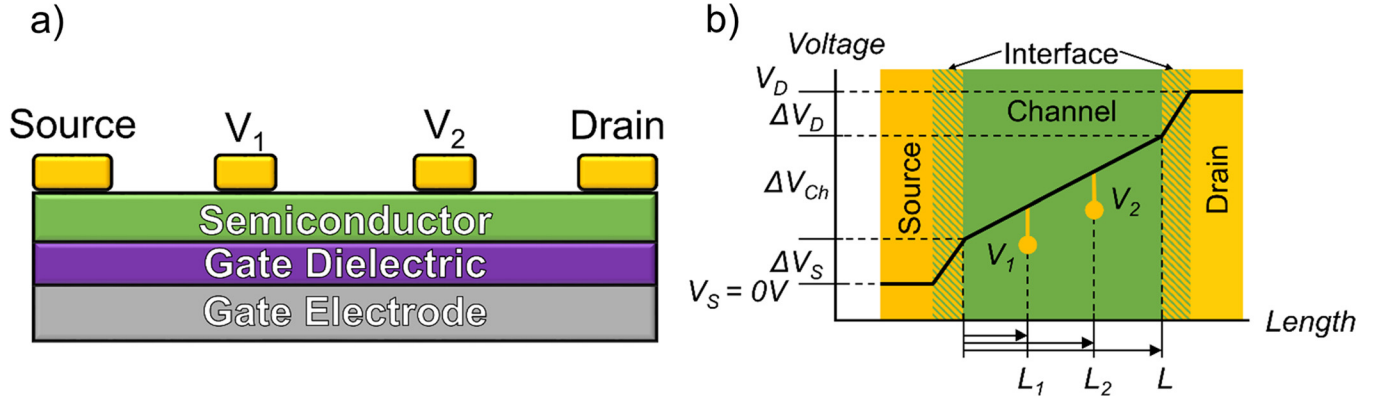
a)

b)

FIG. 10. (a) In the linear four-point probe, two voltage sense probes are placed in the channel of the device. (b) Geometry and linear assumptions determine the voltage drops across source, drain, and channel, allowing resistances to be calculated from Ohm's law.

where L_1 and L_2 are the distances between the source electrode and the first and second sense probes, respectively, and V_S is the potential at the source electrode with reference to ground. Note that the source contact is grounded, in which case $V_S = 0$ V. Similarly, the voltage drop across the drain contact is

$$\Delta V_D = V_D - \left[V_2 + \frac{V_2 - V_1}{L_2 - L_1}(L - L_2) \right], \qquad (20)$$

where L is the length of the OFET channel (source-drain distance), and V_D is the potential at the drain electrode with reference to ground. Therefore, the voltage drop across the channel is equal to

$$\Delta V_{Ch} = \frac{V_2 - V_1}{L_2 - L_1} L, \qquad (21)$$

which is equivalent to the source-drain voltage less ΔV_S and ΔV_D. By substituting the measured drain current I_D into Ohm's law, the resistance of the contacts and the channel can be calculated

$$R_i = \frac{\Delta V_i}{I_D}, \quad i = S, D, Ch. \qquad (22)$$

The total contact resistance is then simply the sum of R_S and R_D. Note that a significant advantage of the gated four-point probe method is it separates source and drain contact resistances. This can be particularly useful when studying devices with different source and drain construction.

Four-point probes can also be used to extract mobility values. From the same current-voltage measurements as above, it is calculated as

$$\mu_{4p} = \left(\frac{1}{C} \right) \left(\frac{L_2 - L_1}{W} \right) \frac{\partial (I_D / (V_2 - V_1))}{\partial V_G}, \qquad (23)$$

where C is the gate-channel capacitance, W is the width of the voltage contacts, and V_G is the gate voltage. However, it has been found that this evaluation can lead to significant overestimation of mobility, and Choi *et al.* have developed a table and code (available in their work) for calculating numerical correction factors.[273]

2. Gated van der Pauw

Van der Pauw (VDP) methods can be used to measure resistivity, sheet carrier density, and mobility, provided the sample is roughly two-dimensional, homogenous and isotropic.[275] The gated van der Pauw (gVDP) method introduced by Rolin *et al.* utilizes the sheet resistance to extract the mobility and threshold voltage in OFETs.[274]

The contact geometry necessary for the van der Pauw measurements is shown in Figs. 11(a) and 11(b). The electrodes are placed at the corners of the device, and numbered counter-clockwise from the top left. The contact area should be minimized in order to stay within the assumptions of the van der Pauw measurement. However, clever patterning of the semiconductor can circumvent this; the cloverleaf pattern of the semiconductor [Fig. 11(b)] is preferred for its ease of use and tolerance against misalignment.[274] This pattern can be formed through shadow mask deposition or scribed manually.[274]

The van der Pauw method is similar to the 4-probe technique described in Sec. IV D 1 in that the current and voltage are measured at different locations in the device. When the geometry in Fig. 11(b) is adopted, the current is evaluated across contacts 1 and 2 (I_{12}) while the voltage is measured between contacts 3 and 4 (V_{34}). Note that this arrangement places both the current and voltage measurement in the vertical direction. The resistance given by this measurement is

$$R_{12,34} = \frac{V_{34}}{I_{12}}. \qquad (24)$$

Reciprocity demands that $R_{12,34}$ be equal to $R_{34,12}$, so accuracy can be enhanced by switching the injecting and sensing contacts and averaging these two measurements. The average resistance for the vertical direction is then

$$R_V = \frac{R_{12,34} + R_{34,12} + R_{21,43} + R_{43,21}}{4}. \qquad (25)$$

Similarly, the average resistance in the horizontal direction is

$$R_H = \frac{R_{23,41} + R_{41,23} + R_{32,14} + R_{14,32}}{4}. \qquad (26)$$
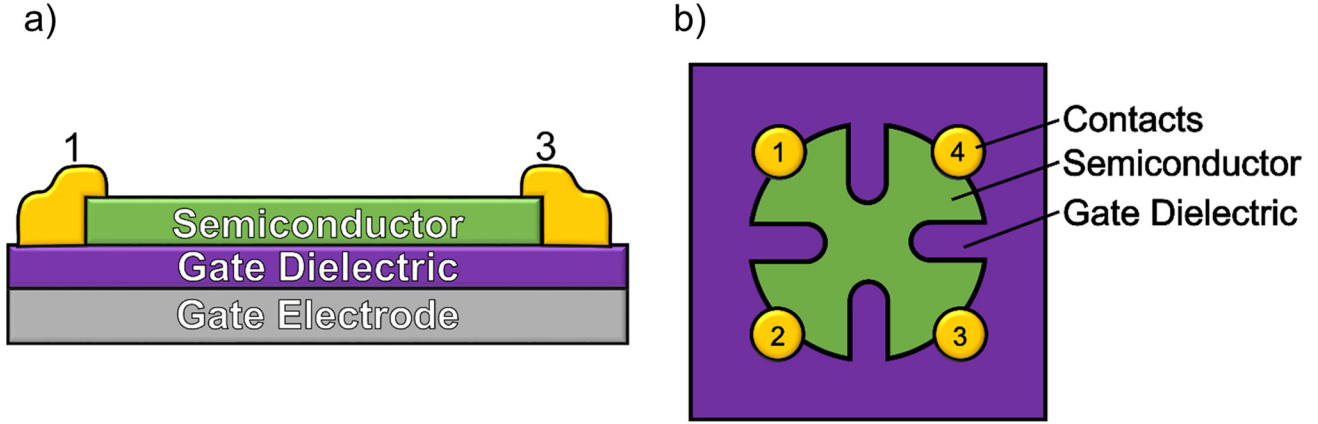
a)

b)

FIG. 11. (a) In the gated van der Pauw geometry, contacts are placed at the corners of the probed region, while a common gate creates transistor-like operation. (b) The cloverleaf design will maximize accuracy due to its smaller effective contact size, but it is more difficult to fabricate than a square or rectangle.

The sheet resistance R_S is calculated then from the van der Pauw formula[275,276]

$$e^{-\frac{\pi R_H}{R_S}} + e^{-\frac{\pi R_V}{R_S}} = 1. \tag{27}$$

Assuming that R_H and R_V are the same for the material of interest, sheet conductance is then

$$\sigma_S = \frac{\ln(2)}{\pi \overline{R}}, \tag{28}$$

where $\overline{R}$ is the average of R_V and R_H.

For the gated van der Pauw method, a gate voltage V_{GS} is applied, leading to charge accumulation at the semiconductor-dielectric interface. Note that, in contrast to typical current-voltage measurements, gVDP works best when the grounded contact is the current sink.[274] Using the thin film transistor generic charge drift model developed by Marinov *et al.*,[277] Rolin *et al.* showed that the sheet conductance in this configuration is equal to

$$\sigma_S = \mu_{tfsc} C_{diel} |V_{GS} - V_{Th} - V_C|, \tag{29}$$

where μ_{tfsc} is the mobility of the channel only (not the total device), C_{diel} is the gate insulator capacitance per unit area, V_{Th} is the threshold voltage, and $V_C = \frac{V_3 + V_4}{2}$.[274] Therefore, the mobility is simply the slope of the σ_S vs. $(V_G - V_C)$ curve, and the threshold voltage is the *x*-axis intercept. This is very similar to the gradual channel approximation model in the linear regime

$$\sigma_S = \mu_{app} C_{diel} \left| V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right|, \tag{30}$$

where μ_{app} is the apparent mobility of the total device, which includes contact effects. However, Eq. (30) relies on the drain-source voltage and is convoluted with contact effects. In contrast, the gVDP contacts measuring V_C in Eq. (29) are not involved in the charge injection process, so μ_{tfsc} is by experimental design independent of the contact effects that plague two-probe techniques. This has been demonstrated with devices made from C_8-BTBT, a material prone to contact problems due to a deep HOMO level.[274] Devices were

made with Ag, Au, and MoOx/Au contacts, with contact resistances spanning four orders of magnitude, yet the μ_{tfsc} mobility values showed low spread and are within error of each other, Fig. 12.[274]

a)

b)
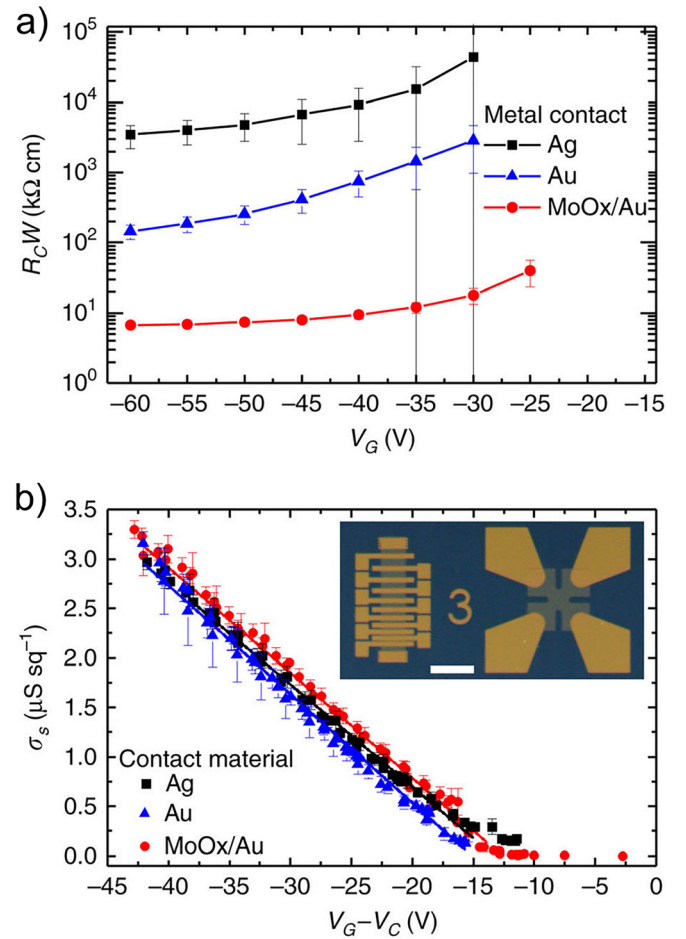
FIG. 12. (a) V_G dependence of contact resistance extracted from TLM measurements based on three different contact materials. The error bars are obtained from the linear regression over the total resistance vs. channel length data. (b) σ_S extracted from gVDP. The error bars are computed by averaging over 8 measurements, 2 along each side of the gVDP structure. Lines are linear fits. Inset: photograph of a sample with side-by-side TLM and gVDP devices. Scale bar is 1 mm long. Reproduced with permission from Rolin, *et al.* Nat. Commun. **8**, 14975 (2017). Copyright 2017 Macmillan Publishers Ltd.[274]

V. OFETs: TOOLS FOR ACCESSING FUNDAMENTAL PROPERTIES OF ORGANIC SEMICONDUCTORS

In Sec. V, we will briefly outline several types of measurements that exploit OFET structures to extract information about the basic properties of organic semiconductors. This list is not to be considered exhaustive.

A. Field-dependent charge carrier mobility: Poole-Frenkel (PF) model

The dependence of mobility on the electric field parallel to the conduction channel offers a powerful method to investigate the quality of the semiconducting film and the trap states at the semiconductor-dielectric interface. Based on the classical OFET models, the mobility is expected to be constant regardless of the magnitude of applied longitudinal electric field. In real devices, however, a field-dependent mobility was observed, and this was assigned to the presence of electronic trapping states. Trap formation results from static or dynamic disorder within the semiconductor layer, impurities, scattering of the charge carriers by polarons, or interactions at interfaces, among other factors. Increasing electric fields reduces the Coulomb potential energy of a trap in the field direction, allowing charges to be thermally excited and escape the trap.[278] Such a behavior has been observed both in small molecule and polymeric OFETs, and the relationship between mobility and longitudinal electric field was described by adopting a Poole-Frenkel (PF)-like model

$$\mu = \mu_0 \exp\left[\gamma\sqrt{E}\right], \tag{31}$$

where μ_0 is the zero-field mobility, i.e., the mobility extrapolated to $V_{DS} = 0$, and E is the electric field created by V_{DS}. The Poole-Frenkel cofactor γ is a temperature-dependent term that quantifies the degree of field dependence of a particular device.[279]

The cofactor γ can be determined by plotting the natural logarithm of mobility versus the square root of the applied electric field. The slope of the linear fit to the data is γ, and the extrapolation to the value of the mobility at zero applied field provides the natural log of the zero-field mobility, as shown in Fig. 13. Here, we include the field dependence of mobility in three different devices, as well as the relation between the corresponding γ values, where a large γ indicates a greater dependence on the field. In general, a low trap density in the semiconductor layer is reflected in a higher mobility, which is also correlated with a small γ and therefore a mild field dependence of mobility on the applied field.

The electric field E is approximated by V_{DS}/L, a relation which implies that the electric field is constant across the device and was validated by numerical simulations.[280] This model for field-dependent mobility in organic semiconductors defers from the original Poole-Frenkel model on several accounts. First, it assumes delocalized carriers and band transport, which does not apply in the case of organic semiconductors.[281,282] In addition, the PF effect requires the presence of a large concentration of charged Coulomb centers in
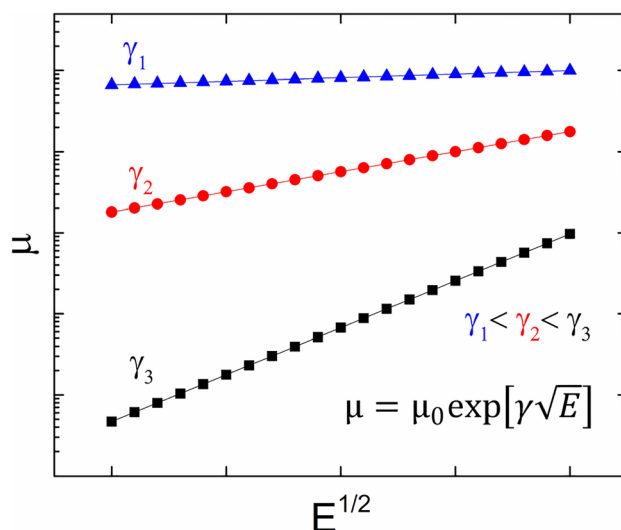

FIG. 13. Logarithmic plot of mobility vs the square root of the electric field. The slopes of the lines yield values for γ, a cofactor used to quantify field dependence in a device.

the semiconducting film. A high electric field causes the ionization of a system of neutral atoms, yielding freely moving electrons and a uniform distribution of static positive ions that generate an additional field. Such Coulomb centers are unlikely to occur in organic materials.[281] Nevertheless, since the experimental results found a dependence of mobility of the applied electric field similar to that described in Eq. (31), the PF model was adopted for organic semiconductors.

The cofactor γ that quantifies field dependence can vary greatly depending on the material choice, device structure, and deposition method, and currently the relationship between γ and μ is not fully understood. Single crystal field-effect transistors, which show the highest degree of order, can exhibit a field-independent mobility ($\gamma \approx 0$).[283] In the polymer poly(2,5-bis(3-tetradecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT-C14), the deposition method of the semiconducting film was shown to have a great effect on field dependence.[280] While as-cast (AC) samples displayed $\gamma \approx 10^{-4}$, devices cast in the liquid-crystal (LC) mesophase had one order of magnitude higher $\gamma \approx 10^{-3}$. This was unexpected as the LC devices show better film ordering and an order of magnitude higher mobility than the AC samples. In the polymer P3HT, a negative γ has been observed (mobility decreasing with increasing electric field) and was attributed to high electric fields preventing charge carriers from moving around defects that would be avoided at weaker fields.[284] For organic small molecules, such as TIPS-pentacene, γ values of 10^{-3} have been observed.[285]

B. Insights into the charge transport mechanism in organic semiconductors from temperature-dependent FET measurements

Temperature-dependent measurements of mobility offer insight into the charge transport mechanism in the semiconducting layer through the sign of the correlation between mobility and temperature. Band-like transport is generally seen in highly-ordered systems, such as single crystals, and it

corresponds to a decrease in mobility with increasing temperature following a power law relation $\mu \propto T^{-n}$ where $0.5 \leq n \leq 3$,[286] as can be seen in the black curve in Fig. 14. This dependence resembles that described by the classical band transport picture, but is, nevertheless, fundamentally different, hence the name band-*like*. Here, the charge carriers are delocalized over several molecules, and the lattice phonons act as scattering sites. Since the lattice vibrations are reduced with lowering temperature, the mobility is enhanced. Band-like transport has been seen in vapor grown single crystal devices,[109,287] in solution-processed films of TIPS-pentacene,[66,288] and in polymers.[289,290]

When the trap density in the semiconductor is high, as is the case of amorphous or polycrystalline thin films, transport can occur by hopping or tunneling between localized states. This process is activated by temperature; therefore the mobility is proportional to temperature and for the simplified case of a single trap level can be modelled by an Arrhenius-like relation

$$\mu \approx e^{\frac{-E_A}{k_B T}}, \tag{32}$$

where E_A is the activation energy. Higher temperature provides sufficient energy for charge carriers to escape from traps and contribute to transport. Several models for activated charge transport have been developed, including the variable-range hopping model and the multiple trapping and release model.[29,291–294] In the first, charge carriers tunnel through the energy barriers between localized electronic states. The probability of tunneling is determined by the distance between traps and the energy barrier between them, so increasing temperature, thereby increasing the kinetic energy of charge carriers, allows for more frequent hopping. In the second model, charge carriers cannot move directly between traps, so instead transport occurs in an extended-state band into which charge carriers are thermally excited. A more recent model that bridges those of band-like and activated transport is the transient localization model, in which charge transport is localized by dynamical disorder arising from

thermal deviations from the perfect crystal structure.[295] For activated transport, the activation energy can be found by plotting $\ln(\mu) \, vs. \, 1/T$ and multiplying the slope of the linear fit by k_B. Generally, E_A is in units of meV.[155,296]

Work has been done to study the relationship between mobility μ and activation energy E_A. In a study of 7 different organic semiconductors, it was shown that there is an inverse relationship between E_A and μ.[296] In this same study, ambipolar materials operated in the n-channel regime exhibited $E_A = 27 \, \text{meV}$, while the same material operated in the p-channel regime showed an activation energy of 250 meV. A different study showed that the activation energy of diF-TES ADT can be tuned from 51 meV to 16 meV by switching the dielectric from SiO_2 to Cytop.[297] This was attributed to a two orders of magnitude decrease in the trap density of states at the semiconductor-dielectric interface and an accompanying decrease in contact resistance when moving from the inorganic dielectric to the polymer. The microstructure of the film also plays a role, as demonstrated in the work of Nelson *et al.*, where pentacene TFTs exhibited highly activated or temperature independent transport depending on the quality of the semiconductor film.[298]

Recent work by Mei *et al.* has shown that the mismatched coefficients of thermal expansion (CTE) of adjacent device layers can create a local, non-uniform strain in the semiconducting film, which gives rise to structural imperfections and hence charge trapping.[155] They concluded that while a highly-ordered semiconducting layer is necessary for achieving band-like transport, it alone is not sufficient. The insertion of an ultrathin insulating polymer of similar CTE with that of the organic semiconductor between the semiconductor and dielectric with mismatched CTE was shown to consistently yield band-like transport, regardless of the differences in the thermal expansion properties of the semiconductor and dielectric layer. While mismatched CTE values serve as one source for temperature dependent trapping states, Fröhlich polarons induced by highly polarizable dielectrics can also trap slow-moving charges.[198] By increasing the dielectric constant of the gate dielectric alone, charge transport was tuned from band-like to activated.

C. Gate-modulated Seebeck coefficient

The generation of an electrical potential difference (ΔV_t) as a result of an applied temperature gradient (ΔT) is referred to as the Seebeck effect. The Seebeck coefficient ($\alpha = \Delta V_t/\Delta T$) is a fundamental property of solids that quantifies the entropy carried by thermally excited charge carriers and therefore involves mainly electronic contributions. Hole transport leads to a positive α-value, whereas electron transport yields negative α. Seebeck effect measurements can be carried out in a two-probe configuration, however, and its measurement in a transistor structure allows one to vary the Fermi-level position by applying a gate voltage. The temperature and gate-dependent Seebeck coefficient provide important information about the microscopic model for the charge transport in organic semiconductors.[299] In the case of band-like transport, the electron–phonon interaction leads to a temperature-dependent mobility, without significantly
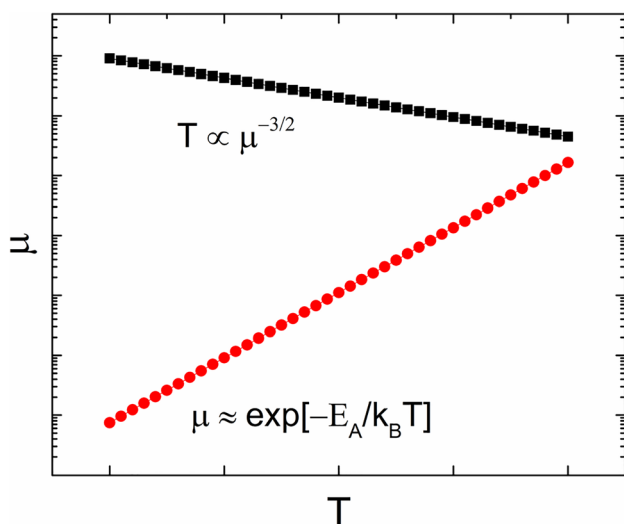

FIG. 14. Example of band-like (black), using an exponent of n = 3/2, and activated (red) transport.

affecting α.[300,301] On the contrary, if the transport takes place by hopping between localized states, then the interaction between the free charge carriers and the lattice induces phonon softening, which leads to larger α.[302,303] The broad range of induced charge density, n that can be obtained using OFET structures may also lead to the discovery of new phenomena that were not accessible before. For example, an unexpected direct proportionality between α and n was observed at high gate voltages and low temperatures in pentacene OFETs.[304] This was associated with a transition from hopping transport, where the charges are localized, to a band-like transport, characterized by extended states.

D. Organic phototransistors

OFETs have successfully been incorporated in light detectors in the form of organic phototransistors (OPTs).[305–307] Organic photodetectors merge the ease of processing characteristic to organic semiconductors with remarkable optical properties such as high external quantum efficiencies and broad spectral absorption that can be tuned by modifying the molecular structure. They are targeted for novel applications addressing the fields of imaging, radiation detection, or optical communication on either flat or flexible substrates. The two basic structures are the photodiodes and phototransistors, with the latter typically exhibiting higher photoresponsivities due to their intrinsic ability to amplify the signal by the two applied voltages V_{DS} and V_{GS}.

The device structures shown in Figs. 1(a) and 1(b) can function as OPTs since here the organic semiconductor is exposed and can absorb light. OPTs convert the photon flux into a charge flux that is monitored as a function of light intensity and/or wavelength. The exciton generated within the semiconductor layer upon photon absorption has a binding energy of a few hundreds of meV and will dissociate upon the application of an external electric field yielding free charges. The details of this process are dependent on the intrinsic properties of the semiconducting layer. Charge photogeneration is enhanced at donor/acceptor (D/A) interfaces, and therefore bilayer and bulk D/A heterojunctions have been proposed.[305,308] The figures of merit for OPTs include the OFET characteristics described in Sec. II B, as well as the responsivity (R) and the photocurrent on/off ratio

$$R = \frac{I_{light} - I_{dark}}{P}, \tag{33}$$

$$\frac{on}{off}_{ph} = \frac{I_{light}}{I_{dark}}, \tag{34}$$

where I_{light} and I_{dark} are the current between the source and drain electrodes under illumination and in dark, respectively, and P represents the incident optical power of the light source.

OPTs have been demonstrated on both small molecule and polymer semiconductors and several examples are included below. For a thorough discussion on this topic, the reader is referred to the review by Baeg *et al.*[24] Using solution-grown single-crystalline semiconductors, responsivities as high as $12\,kA/W$ and $14\,kA/W$ have been obtained in

OPTs based on 6-methyl-anthra[2,3–*b*]benzo[*d*]thiophene (Me-ABT)[309] and a conjugated anthracene-based compound,[307] respectively. In drop-cast samples, responsivities between 2500 and 4300 A/W were demonstrated using 1,2,4,5-tetra(5′-hexyl-[2,2′]-bithiophenyl-5-vinyl)-benzene (4(HPBT)-benzene).[310] While they show lower performance, OPTs based on polymer semiconductors have also been reported. In regioregular poly(3-heylthiophene) (P3HT), a responsivity of 24.5 A/W was produced,[311] and in poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2), OPTs with responsivities up to 18.5 A/W were achieved.[312]

VI. SUMMARY

The organic field-effect transistor is the fundamental building block in many applications driven by organic semiconductors and it offers a great experimental platform for elucidating the intrinsic properties of organic semiconductors. The performance of OFETs has steadily improved in the past decades through the development of new materials, optimization of the organic semiconductor microstructure, and enhanced control of the processes occurring at the semiconductor-dielectric and semiconductor-electrode interfaces. The seemingly unlimited variety of organic semiconductors, both small molecule and polymer, has given rise to a diverse assortment of processing conditions which can be tailored both to the material as well as the application. Analysis methods which can isolate the electronic contribution of the individual OFET components have allowed a deeper insight into the functioning of these devices and by doing so, highlighted the deficiencies which must be studied in greater detail. In addition, device operation under varied conditions (temperature, light, and electric field) can provide a more comprehensive understanding of the processes involved in charge transport through OFETs. These concepts together make the field of organic electronics a rich exploration into application-driven science.

ACKNOWLEDGMENTS

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