Boron-emitter development for TOPCon c-Si solar cells based on plasma-deposited boron diffusion source and poly-Si(n) passivating contact

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ABSTRACT

The n-type TOPCon technology is currently the leading approach in the industry. Generally, it involves two high-temperature steps that can result in long cycle times and expensive processes. In this context, we propose a lean manufacturing process based on the successive PECVD-deposition of the front and rear doped layers, followed by a co-annealing step in which front emitter formation and rear passivating contact activation are performed simultaneously. We first investigated the influence of the PECVD process parameters and the thermal budget of the co-annealing step on the active boron concentration profile, the passivation quality, and contact resistivity. Then, we investigated the effect of a drive-in step under O_2 environment to reduce the surface concentration and increase the depth of the emitter. Finally, we investigated the compatibility of the rear passivating contact with the drive-in step. The introduction of the drive-in step made it possible to obtain active boron concentration profiles with the desired surface concentration and depth. However, even though we obtained promising results regarding the compatibility of the rear passivating contact with the drive-in step, we observed that further optimization is necessary to avoid blistering of the n-type poly-Si layer and improve the uniformity of the rear passivation.

1. Introduction

In the context of high-efficiency crystalline silicon (c-Si) solar cells, n-type Tunnel Oxide Passivating Contacts (TOPCon) technology [1] is currently the leading approach in the industry and is expected to become the dominant technology in terms of market share in the course of 2025 [2]. Industrial TOPCon solar cells feature a boron (B) emitter at the front of a n-type wafer to form the p+/n junction, and a c-Si(n+)/SiO$_x$/poly-Si(n) interface at the rear that acts as an electron selective contact. The interfacial silicon oxide (SiO$_x$) grown on the c-Si wafer at the rear is typically 1–2 nm thick and provides chemical passivation, while the highly doped n-type polycrystalline silicon (poly-Si) layer on top provides field-effect passivation, carrier selectivity and low contact resistance. Considerable research efforts over the past decade in passivating contacts have led to a significant reduction in recombination losses in these contacts, resulting in a record power conversion efficiency (PCE) above 26% at cell level [3]. Owing to the high-quality surface passivation of the rear passivating contact, recombination losses in the front B emitter have become the most limiting factor to device performance [4,5].

The front B emitter profile plays a crucial role in these recombination losses, and therefore in the final device performance. In the design of B emitter profiles, increasing the surface concentration and emitter depth improves the fill factor (FF), thanks to a better lateral conductivity of the diffusion region and a lower contact resistance to the metallization. However, it also increases recombination at the interface with the passivating dielectric layers and Auger recombination in the diffusion region, which results in a decrease of the implied open circuit voltage (iV_{oc}). Thus, a compromise must be found between FF and iV_{oc} to obtain the best B emitter profile. Based on calculations performed with EDNA [6] and suggestions from the literature [7–10], an optimized B emitter profile that offers the best trade-off between FF and iV_{oc} with commercial screen-printed high-temperature Ag–Al paste metallization typically requires a surface concentration of 1 to 5 $\times 10^{19}$ cm^{-3} and an emitter depth of 700 to 1000 nm. However, recent technological advances on metallization such as laser-enhanced contact optimization (LECO) [11] and fine printing [12,13] have relaxed the requirements in terms of surface concentration and emitter depth. The

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iTOPCon

- Texturing + cleaning
- B diffusion
- Single-side rear etching
- SiO_x + poly-Si(i)
- P diffusion
- Single-side front etching
- Surface passivation
- Screen-printing + firing

co-annealed TOPCon

- Texturing + cleaning + SiO_x
- Front B dopant source } PECVD
- Rear poly-Si(n)
- Co-annealing
- Single-side front etching
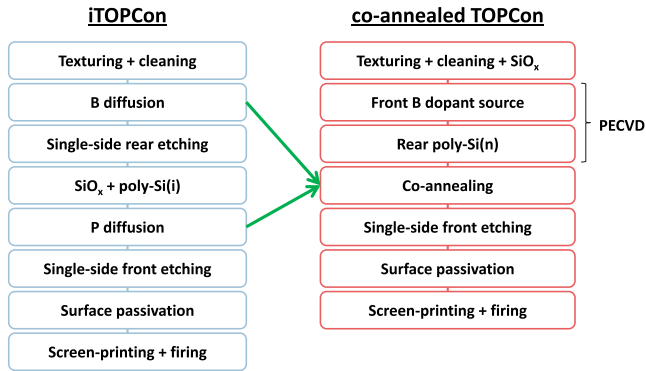- Surface passivation
- Screen-printing + firing

Fig. 1. Manufacturing processes of industrial and co-annealed TOPCon devices.

use of these two technologies would make it possible to use B emitter profiles with a surface concentration of 1 to 5×10^{18} cm^{-3} and an emitter depth of 500 to 600 nm [12,13] with contact resistivity values below $1 \, m\Omega \, cm^2$ previously reported in the literature [13].

In conventional industrial TOPCon solar cell manufacturing processes, two high-temperature steps are required; one to form the front p-type emitter and another one to form the rear passivating contact [14]. The front emitter formation step aims to create the junction, getter impurities and create lateral conductivity, and conventional processes use tube furnace diffusion in a boron tribromide (BBr_3) or boron trichloride (BCl_3) environment. Such industrial tube diffusion processes generally feature a temperature profile consisting of several steps and gas introduction phases. The first step, generally referred to as the deposition step, is designed to deposit a borosilicate glass (BSG) layer, which consists of a B_2O_3/SiO_2 stack. The second step, generally referred to as the diffusion step, is carried out at a higher temperature and aims to diffuse B from the BSG into the wafer. Finally, a third step, generally referred to as the post-oxidation step, is eventually added to lower the surface concentration and increase the emitter depth [7–9]. Tube furnace diffusion processes yield B emitter profiles with surface concentrations and emitter depths compatible with standard industrial metallization approaches, and several studies have already reported systematic variations in temperatures, gas flows and durations of the various process steps on emitter characteristics [5,7–9,15]. However, these processes have the drawbacks to be time- and energy-consuming and, in addition, to form BSG on both sides, which requires removal and additional chemical cleaning prior to subsequent surface passivation.

In order to reduce manufacturing costs, several research groups have investigated the feasibility of using a single high-temperature step, referred to as co-annealing, in the manufacturing process of TOPCon solar cells [16,17]. In this context, we aim to develop a lean manufacturing process for co-annealed TOPCon devices, as shown in Fig. 1, in which the front and rear doped layers are subsequently deposited by plasma-enhanced chemical vapor deposition (PECVD) prior to a co-annealing step that simultaneously enables the formation of the front emitter and the activation of the rear passivating contact. This proposed lean manufacturing process for TOPCon solar cells aims to reduce manufacturing costs and/or complexity, thanks to a reduced number of processing steps by co-annealing, and to the minimization of wrap-around by using PECVD. Such a lean manufacturing process would prove particularly advantageous in countries where facility and equipment costs are high. Furthermore, high-throughput PECVD tools developed for the production of Si heterojunction (SHJ) solar cells, enabling rapid deposition of amorphous silicon on both sides, could also be repurposed to deposit both the B diffusion source on the front and the TOPCon structure on the rear. This would enable a lean manufacturing process which we discussed in an earlier publication [18].

Emitter formation with B diffusion from a plasma-deposited B diffusion source has already been reported in literature by other research groups, all of them using a gas mixture of SiH_4, H_2 and B_2H_6, with a B diffusion source consisting of either B-doped SiO_x or BSG. With high-temperature annealing under N_2 and O_2, Cheng et al. [19] have shown that this technique can yield B emitter profiles similar to those obtained by conventional tube diffusion processes for integration into conventional TOPCon manufacturing processes based on two high-temperature steps. Extensive research on B emitter formation via B diffusion from plasma-deposited BSG has also been carried out by Wehmeier et al. [20–22] in the context of back junction formation for n-type Passivated Emitter and Rear Totally Diffused (PERT) solar cells. However, neither Cheng et al. [19] nor Wehmeier et al. [20–22] compared the active B concentration with the total B concentration for B emitters diffused from a plasma-deposited B diffusion source. They also did not study the influence of a drive-in step under O_2 environment in such applications. As mentioned above, the concept of a single high-temperature step to manufacture TOPCon solar cells has already been studied by other research groups as well. Using rapid direct vapor-phase doping (RVD) to form the front emitter, Driessen et al. [16] achieved a PCE of 23.3% at the cell level, which is similar in performance to the PCE they obtained with a reference sample obtained with sequential BBr_3 diffusion. In a manner more similar to our proposed manufacturing process, Du et al. [17] used PECVD to deposit precursor layers, followed by a one-step high-temperature annealing. Using photolithography and electroplating to form the front Ti/Pd/Ag electrodes, and a magnesium fluoride (MgF_2) layer to optimize the front passivation and antireflection, they achieved a PCE of 24.07% at the cell level. Several differences can be highlighted between the co-annealing-based manufacturing processes already reported by other research groups [16,17] and ours. First, while Driessen et al. [16] grow the interfacial SiO_x in an N_2/O_2 environment, we aim to form ours by N_2O plasma treatment, which should provide good passivation quality [23,24] and could be carried out in the same PECVD cycle as the deposition of the rear poly-Si(n) layer. Second, the interfacial SiO_x at the front needs to be removed prior to the RVD process, as its presence would prevent B from incorporating into c-Si, whereas in our process, B diffuses easily through it. In addition, the rear poly-Si(n) layer must be covered with a 400 nm thick SiO_x layer prior to the RVD process to prevent B dopants from incorporating into poly-Si(n), and this capping layer must be removed later. While Du et al. [17] use a B diffusion source that consists of a nano-SiO_x/B-doped a-Si:H stack, which requires alternating HNO_3 oxidation and HF etching to be removed, our B dopant source layer is composed solely of B-doped SiO_x which can be removed by HF etching in a single step. Based on the differences mentioned above between our lean manufacturing process and those already demonstrated by other research groups, we consider our manufacturing process to be innovative as a whole and that the results we report here are valuable for guiding the industrial development of TOPCon technology.

In this work, we build on the results presented in our previous publication [18] and further develop the boron emitter formation process. We first study the influence of the doping gas flow and the co-annealing thermal budget on the B emitter profile, passivation quality and contact resistivity, and investigate the presence of electrically inactive dopants in the emitter region by comparing the depth profiles of active dopant concentration with the depth profiles of total B concentration. Based on the knowledge acquired, we modify the co-annealing step by adding a drive-in phase carried out in an O_2 environment in order to reduce the surface concentration and increase the emitter depth. We show that while this modification reduces the surface concentration and increases the emitter depth, resulting in reduced surface recombination and improved compatibility with standard industrial metallization processes, further improvements are required to enhance passivation quality and reduce contact resistivity. Finally, we further investigate the influence of the different phases of the co-annealing step on the B emitter profile, and elaborate on prospects for the compatibility of the rear passivating contact with the modified co-annealing step.
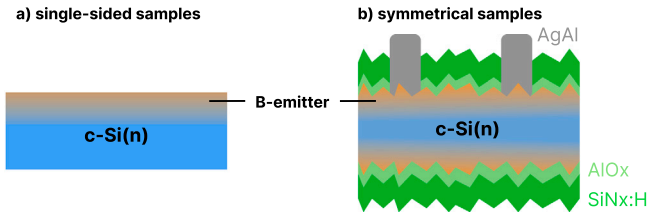
Fig. 2. Resulting (a) single-sided and (b) symmetrical structures.

Fig. 3. (a) Single-step temperature profile and (b) two-step temperature profile with drive-in under O_2 environment.

2. Experimental details

2.1. Sample preparation

The experiments were performed on 4″, <100> oriented, n-type float-zone (FZ) c-Si wafers with resistivity of $2\,\Omega\,cm$ and thickness of $200\,\mu m$. Two types of samples were produced: single-sided samples for depth profiling and sheet resistance characterization, and symmetrical samples for passivation and contact resistivity assessment. For the single-sided samples, shiny etched (SE) wafers were used. After an initial cleaning step, thin interfacial SiO_x layers ($\sim 1.2\,nm$) were formed by immersing the samples in HNO_3 at $80\,°C$ for 10 min. The B dopant source layers, which consist of B-doped silicon oxide ($SiO_x(p)$), were then deposited by parallel-plate, capacitively coupled PECVD (Kai-M reactor, Unaxis). We used a gas mixture of SiH_4, CO_2, H_2, and 2% $B(CH_3)_3$ (trimethylboron, TMB) diluted in H_2, with gas flow ratios $SiH_4/CO_2 \simeq 2.5\%$ and $SiH_4/H_2 \simeq 0.1\%$. The PECVD process pressure, temperature and frequency were set to $1\,mbar$, $200\,°C$ and $40.56\,MHz$, respectively. With a power density $\simeq 200\,mW\,cm^{-2}$ and a deposition time of $3\,min$, the estimated B-doped SiO_x layer thickness is $\simeq 20\,nm$. The PECVD-deposition of the B-doped SiO_x layer was followed by annealing with different temperatures and dwell times. The B-doped $SiO_x(p)$ layers were then removed using 5% HF diluted in deionized (DI) water. For the symmetrical samples, the wafer surfaces were textured and the process described above was applied to both sides. Prior to subsequent passivation steps, surfaces were cleaned either by oxidation using O_3 in DI water followed by HF etching or standard clean 2 (SC2). After deposition of a thin AlO_x layer (5–10 nm) by atomic layer deposition (ALD), a hydrogen-rich silicon nitride ($SiN_x:H$) layer was deposited by PECVD. Finally, patterns for transfer length method (TLM) were screen-printed using Ag–Al paste, followed by a firing process at $840\,°C$. The resulting single-sided and symmetrical structures are depicted in Fig. 2.

2.2. Characterization techniques

Single-sided samples were used to characterize the depth profile of active dopant concentration and total B concentration, and sheet resistance. The depth profile of active dopant concentration was characterized by electrochemical capacitance-voltage (ECV) profiling with a Wafer Profiler CVP21 (WEP) tool using an electrolyte solution of $0.1\,M$ NH_4HF_2. The sheet resistance R_{sh} was either calculated from the profile depth of active dopant concentration using the online calculator EDNA 2 [6] or measured by four-point probe (4PP). The depth profile of total B concentration was characterized by secondary ion mass spectrometry (SIMS) with an IMS 1280HR (CAMECA) tool using an O_2 primary ion beam. Symmetrical samples were used to extract iV_{oc} from non-metallized areas and ρ_c from TLM patterns. The iV_{oc} was extracted by quasy-steady-state photoconductance decay (QSSPC) using a WCT-120TS (Sinton Instruments) tool and the contact resistivity ρ_c was determined with the transfer length method (TLM).
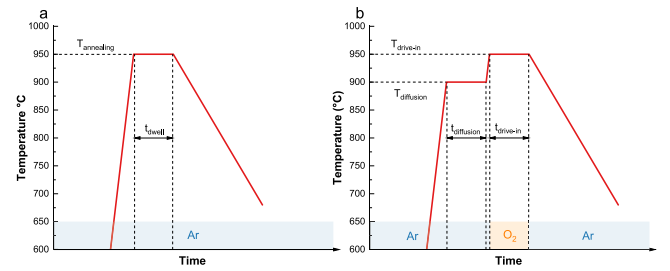
3. Results and discussion

3.1. Annealing with single-step temperature profile

First, we studied the emitter formation through an annealing with a single-step temperature profile, as shown in Fig. 3.a. After stabilizing the temperature at around $40\,°C$, the temperature profile consists of a heating ramp ($+10\,°C/min$), followed by a plateau at a given annealing temperature ($T_{annealing}$) for a given dwell time (t_{dwell}), and ends with a cooling ramp ($-2\,°C/min$) until the temperature reaches $680\,°C$. The entire annealing process is carried out under Ar atmosphere.

3.1.1. Influence of thermal budget and doping gas flow

We first investigated the influence of thermal budget and doping gas flow on the emitter profile, passivation quality, and contact resistivity. Single-sided samples were produced with TMB flows of 30, 50 and $90\,sccm$ and thermal budgets of $900\,°C/1\,h$, $900\,°C/3\,h$, and $950\,°C/1\,h$ ($T_{annealing}/t_{dwell}$). Emitter profiles were characterized by ECV profiling and R_{sh} was calculated with EDNA. Symmetrical samples were produced under the same process conditions to extract iV_{oc} by QSSPC and ρ_c by TLM.

Fig. 4.a shows the influence of the thermal budget on the emitter profile with a constant TMB flow of $50\,sccm$. While the surface concentration does not depend on the thermal budget, the emitter depth increases with it. Fig. 4.b shows the influence of the TMB flow on the emitter profile with constant thermal budget of $900\,°C/1\,h$. In this case, both the surface concentration and emitter depth increase with the TMB flow. Based on these observations, we can assume that while the surface concentration can be adjusted by the TMB flow, the emitter depth can be adjusted by the thermal budget. Moreover, under the process conditions studied, increasing the annealing temperature is more beneficial than increasing the dwell time for increasing the emitter depth. However, the process parameters tested yield emitter profiles with surface concentrations that are too high or profile depths that are too shallow. The emitter depth could be increased by increasing the annealing temperature or dwell time, but this would most likely result in high thermal budgets that would cause severe degradation of the rear passivating contact when the co-annealing step is applied in the TOPCon solar cell manufacturing process, as described in Fig. 1. It can also be observed that with a high TMB flow ($90\,sccm$) and thermal budget of $900\,°C/1\,h$, the maximum dopant concentration exceeds the solid solubility of B in c-Si at the annealing temperature [25].

Fig. 4.c shows the influence of the TMB flow and the annealing temperature on iV_{oc} with a constant dwell time of $1\,h$. For both thermal budgets, iV_{oc} decreases with increasing TMB flow. Modeling in EDNA suggests that the low iV_{oc} values ($<700\,mV$) obtained are due to high surface recombination velocities (SRV) at the interface with the passivating dielectric because of high surface concentration and, to a lesser extent, to Auger recombination in the diffusion region. The low iV_{oc} values obtained could also result from a poor bulk lifetime, which could be related to the initial wafer quality, or to bulk defects introduced
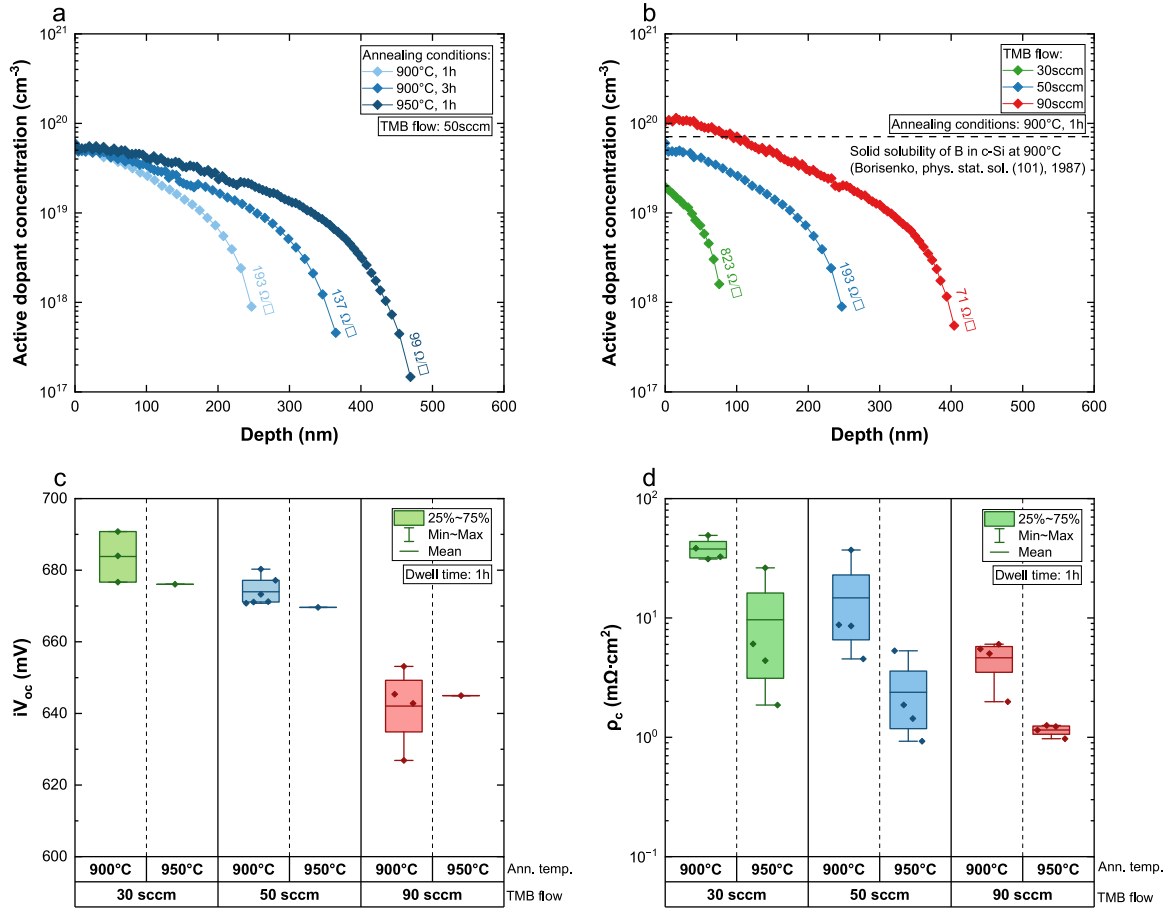
Fig. 4. (a) Influence of the thermal budget on the emitter profile with a constant TMB flow of 50 sccm, (b) influence of the TMB flow on the emitter profile with constant thermal budget of 900 °C/1 h, (c) influence of the TMB flow and the annealing temperature on iV_{oc} with constant dwell time of 1 h and (d) influence of the TMB flow and the annealing temperature on ρ_c with constant dwell time of 1 h.

throughout the process, as suggested by some samples that showed a decrease in effective lifetime at low injection after firing. With TMB flows of 50 and 90 sccm, thermal budgets of 900 °C/1 h and 950 °C/1 h, ρ_c values of less than 10 mΩ cm² were obtained on symmetrical samples as shown in Fig. 4.d.

3.1.2. Depth profiles of active dopant concentration and total B concentration

To further investigate the source of recombination losses in the emitter region, we compared the depth profile of the active dopant concentration measured by ECV profiling with the depth profile of the total B concentration measured by SIMS. To this end, single-sided samples with TMB flows of 50 and 90 sccm and thermal budget of 950 °C/1 h were produced and characterized with the two profiling techniques. The results are presented in Fig. 5.

The sputtering rate and the conversion factor between SIMS signal intensity and concentration were adjusted so that the tail regions of the depth profiles measured with the two profiling techniques coincide, since we assume that in this region the active dopant concentration is very close to the total B concentration. However, due to the depth resolution and the uncertainties of the two profiling techniques, slight discrepancies between the different depth profiles remain in these regions.

With both TMB flows, we observe that the depth profiles of the active dopant concentration and the total B concentration differ near the surface of the emitter when the concentration exceeds 10^{19} cm⁻³. This suggests the presence of electrically inactive dopants that would very likely result in an increased defect density in the emitter region,
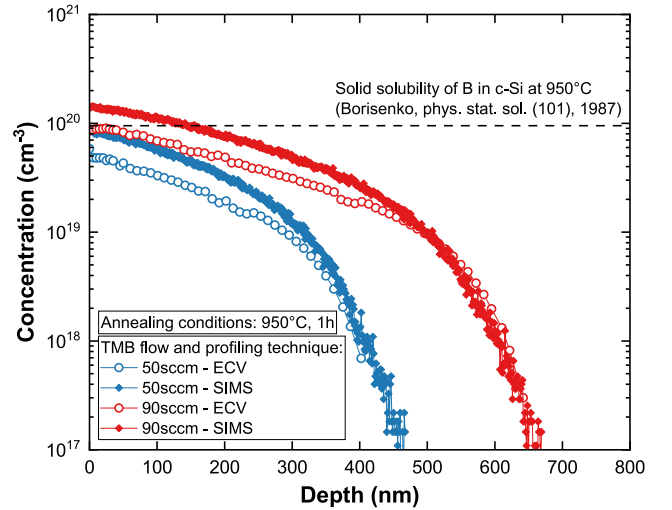

Fig. 5. Depth profiles of active dopant concentration (measured by ECV) and total B concentration (measured by SIMS) obtained with TMB flows of 50 and 90 sccm and thermal budget of 950 °C/1 h.

which could explain the low iV_{oc} values obtained with such emitter profiles.

The presence of electrically inactive B in emitters has already been studied for the formation of B emitters by implantation doping [26,27].
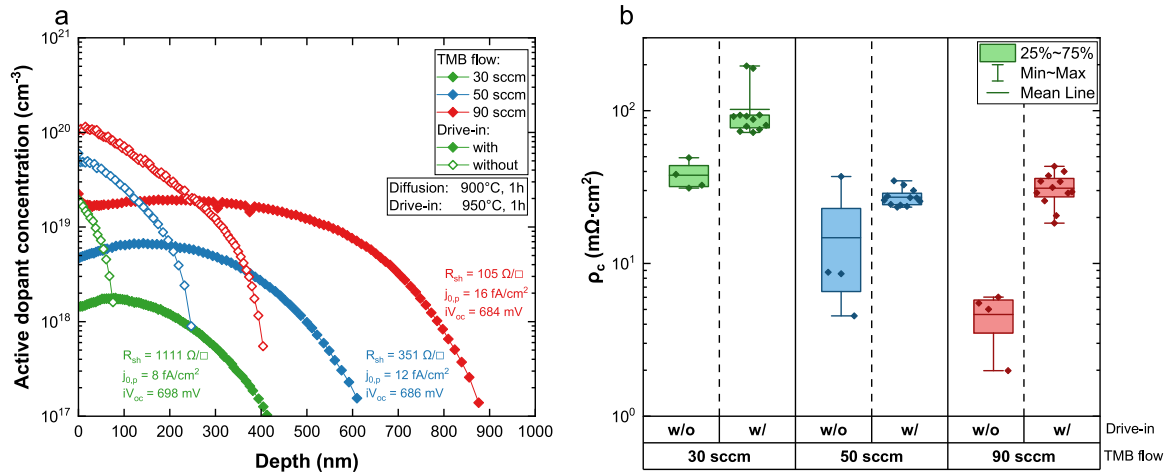
Fig. 6. (a) Emitter profiles and (b) contact resistivity values for TMB flows of 30, 50 and 90 sccm, diffusion conditions of 900 °C/1 h and drive-in conditions of 950 °C/1 h, with and without drive-in.

In a similar experiment, Raghuwanshi et al. [26] observed maximum SIMS-ECV differences in the first 100 nm of B-implanted emitters. They used atomic probe tomography (APT) to characterize the atomic distribution of B and showed that the SIMS-ECV difference is mainly due to the presence of boron interstitial clusters (BICs) which were reported to form near the emitter surface [28]. They concluded that the presence of BICs in the most doped regions of the emitter is the main reason for the high recombination current in B-implanted emitters. They attributed the clustering of B atoms to the low solid solubility of B in c-Si at the annealing temperature of 950 °C that they used, and succeeded in reducing the BIC density by a factor of 4.5 by increasing the annealing temperature from 950 °C to 1050 °C. However, increasing the annealing temperature to over 950 °C would require optimized rear TOPCon layers capable of withstanding such high temperatures, which is not the case with ours in which the interfacial SiO_x is obtained either by HNO_3 or UV-O_3 oxidation [29]. However, the use of a N_2O plasma treatment could extend the temperature range compatibility of our rear TOPCon layers, as discussed in the context of a drive-in step under O_2 environment in Section 3.3 below. Previous studies on the presence of BICs in emitters obtained by tube diffusion in BCl_3 or BBr_3 environment showed that it is possible to avoid the clustering of B atoms via tube diffusion processes [8,26], which makes our proposed manufacturing process less competitive in this respect. In *p*-type solar cells, similar phenomena are observed in heavily phosphorous (P)-doped emitters, with electrically inactive P giving rise to precipitates [30], and several studies suggest that most recombination losses in P-doped emitters are caused by SRH recombination via defect states introduced by electrically inactive P [30–32]. These studies could therefore serve as a starting point for a more in-depth study of recombination losses in the B emitters obtained in the context of this work, and provide the basis for modeling the various recombination mechanisms of interest.

3.2. Annealing with two-step temperature profile with drive-in under O_2 environment

The above observations enabled us to gain a good understanding of the influence of thermal budget and doping gas flow on the emitter profile, passivation quality, and contact resistivity, as well as shedding light on the potential origin of recombination losses in the emitter. However, the emitter profiles obtained showed surface concentrations that were too high and/or emitter depths that were too shallow. Even if the emitter depth could be increased by increasing the thermal budget, this would most likely lead to severe degradation of the rear passivating contact and excessively long cycle times.

To optimize the emitter profiles (i.e. to reduce the surface concentration and increase the depth of the emitter), we added a second

step in the annealing temperature profile, as illustrated in Fig. 3.b. This two-step temperature profile, inspired from conventional tube furnace diffusion processes [5,7,9,15,33], consists of a first step carried out under Ar environment, referred to as the diffusion step ($T_{diffusion}$, $t_{diffusion}$), and a second step carried out in an O_2 environment, referred to as the drive-in step ($T_{drive-in}$, $t_{drive-in}$). The heating and cooling rates are identical to those of the single-step temperature profile studied previously. The purpose of introducing O_2 is multiple. First, during the drive-in step we expect the B atoms to continue to incorporate into the c-Si wafer and diffuse deeper into it [7,9]. Second, we expect the B atoms to redistribute in a thermally grown intrinsic SiO_x layer [7,9,34]. Finally, we expect the most doped regions at the c-Si/SiO_x interface to oxidize and be subsequently removed by HF etching. These three above-mentioned effects should therefore result in emitter profiles with reduced surface concentration and increased depth compared with the emitter profiles obtained with the one-step temperature profile studied previously.

3.2.1. Investigation of feasibility

To investigate the feasibility of a co-annealing with a two-step temperature profile with drive-in under O_2 environment, we produced single-sided and symmetrical samples with TMB flows of 30, 50 and 90 sccm. The diffusion step under Ar was carried out at 900 °C for 1 h, while the drive-in step was carried out at 950 °C for 1 h. Emitter profiles, iV_{oc} and ρ_c values obtained with these process conditions are shown in Fig. 6.

We observe that the drive-in step introduced into the co-annealing process enabled a reduction in surface concentration and an increase in emitter depth. With a TMB flow of 90 sccm, we successfully obtained an emitter profile with both surface concentration (2.24×10^{19} cm^{-3}) and emitter depth (880 nm) in the target range. However, this emitter profile shows an increase in active dopant concentration near the emitter surface, which could be due to a SiO_x(p) layer not being completely removed by HF or to the formation of a B-rich layer. With other TMB flows, we observe a surface depletion of active dopants, due to the higher solid solubility of B in the SiO_x layer grown during the drive-in step than in c-Si [8]. This could improve surface passivation and should not deteriorate carrier collection if metallization is achieved via screen-printing and firing-through of Ag–Al paste, since with this metallization technique the penetration of metal crystallites into the emitter can reach depths of up to several μm [35–39]. Fig. 7.a shows that the introduction of the drive-in step reduces recombination losses as indicated by the increase in iV_{oc} values. To verify whether the improvement can be linked to the lower surface concentration, we show in Fig. 7.b the dependence of effective SRV on surface concentration.
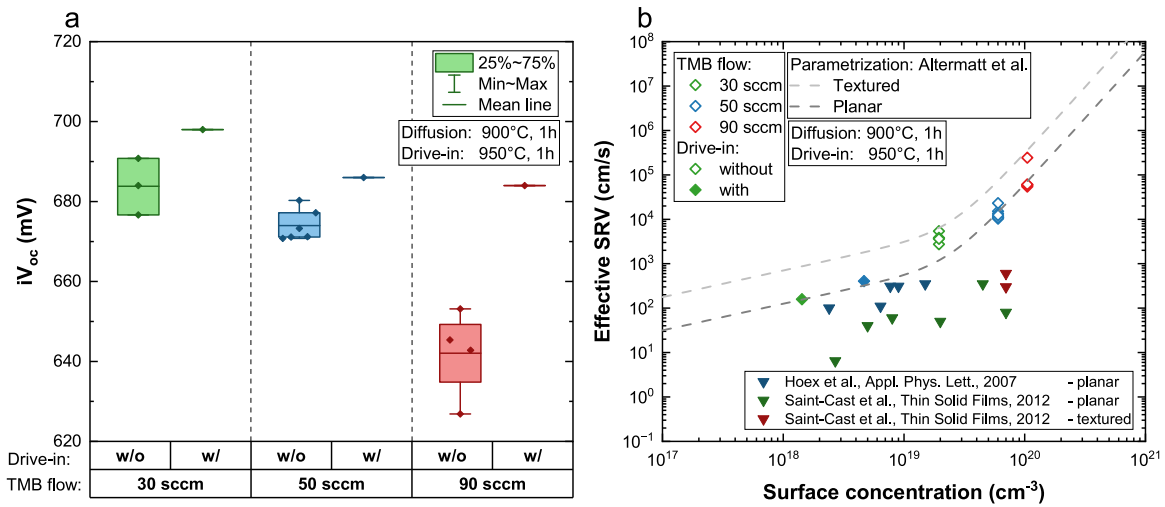
Fig. 7. Influence of the drive-in step on (a) iV_{oc} and (b) SRV as a function of surface concentration.

Table 1
Investigated diffusion and drive-in conditions with constant TMB flow of 50 sccm.

Diffusion	Drive-in
900 °C/1 h	
900 °C/3 h	
950 °C/1 h	950 °C/1 h
950 °C/3 h	
	900 °C/1 h
	900 °C/3 h
900 °C/1 h	950 °C/1 h
	950 °C/3 h

The SRV values were extracted from the experimental emitter recombination current density values measured by QSSPC and the active dopant concentration profiles characterized by ECV profiling using numerical modeling in EDNA [6], with recombination models developed by Fell et al. [40] (radiative) and Niewelt et al. [41](Auger). We find that our samples fall close to reported data by Hoex et al. [42] for planar ALD-AlO$_x$-passivated diffusion profiles of boron. However, further optimization would be necessary to achieve the level of passivation demonstrated by Saint-Cast et al. [43] for PECVD-AlO$_x$ passivated boron diffusion profiles on flat and textured surfaces. We superimpose on this graph two parametrizations established by Altermatt et al. [44, 45] for P diffusion profiles passivated with SiO$_x$ in order to illustrate the expected behavior at low and high surface concentrations. These parametrizations also justify the higher SRV values we obtained on textured surfaces compared to the data reported by Hoex et al. [42] on flat surfaces. The improvement in surface passivation found after the introduction of the drive-in step is thus mainly related to a reduction in effective SRV, thanks to a reduced surface concentration resulting in a reduction in defect density at the interface. However, iV_{oc} values remained below 700 mV. As mentioned earlier, these low iV_{oc} values could be due to poor surface passivation, poor bulk quality or bulk defects introduced throughout the process. This reinforces the need to improve the passivation with an AlO$_x$/SiN$_x$:H stack and to further investigate the origin of recombination losses.

3.2.2. Influence of diffusion and drive-in conditions

To investigate the influence of diffusion and drive-in conditions on the emitter profile, we produced single-sided samples with a TMB flow of 50 sccm, and varying diffusion and drive-in conditions that are given in Table 1. The emitter profiles characterized by ECV profiling for these diffusion and drive-in conditions are shown in Fig. 8.

In Fig. 8.a, we observe that the surface concentration and the emitter depth increase with the diffusion temperature, as more dopants are incorporated into the c-Si wafer prior to the drive-in step. The same trend is observed with the diffusion time. Fig. 8.b shows a more complex trend with regard to the drive-in temperature. The emitter depth increases with the drive-in temperature, but the influence of the drive-in temperature on the surface concentration seems to depend on the drive-in time. With a short drive-in time (1 h), the surface concentration increases with the drive-in temperature, whereas the opposite trend is observed with a long drive-in time (3 h). This suggests that during the drive-in, first more dopants are incorporated into the c-Si wafer, and then they diffuse back into the thermally grown SiO$_x$ layer. We can also observe that the surface concentration decreases when the drive-in time increases. Moreover, with a high drive-in temperature (950 °C), the emitter depth seems to saturate at a stable value. Consequently, while keeping a constant emitter depth, the surface concentration could probably be adjusted by adjusting the drive-in time, which would enable a very interesting customization of the emitter profile.

The effect of the drive-in step is somewhat similar to the post-oxidation step in conventional tube furnace diffusion processes, which also significantly decreases surface concentration [7]. However, the relative importance of the different mechanisms involved (oxidation-enhanced diffusion, SiO$_x$ growth, B segregation in SiO$_x$) is highly dependent on the range of parameters studied. Although it is not clear how the trends observed in this work compare with those observed with tube diffusion processes, we can nevertheless state that, in addition to the diffusion and drive-in conditions, the TMB flow constitutes an additional parameter that has a significant effect on the emitter profile in our manufacturing process. There appears to be no equivalent parameter in conventional tube furnace diffusion processes, as large variations in BBr$_3$ or BCl$_3$ flow during BSG deposition do not lead to significant changes in overall doping concentration [5,8]. In addition to the work presented above, the influence of other parameters of the drive-in step needs to be further investigated. For example, it was reported that the ambient composition can influence the diffusivity of B in SiO$_x$ [34], or that the O$_2$ flow rate and pressure can influence the diffusivity and uniformity of B in SiO$_x$ [5,8].

3.3. Preliminary results on the compatibility of the rear passivating contact with the drive-in step under O$_2$ environment

To ensure that the drive-in step is compatible with our proposed lean manufacturing process for TOPCon solar cells, we must verify that it does not have any significant negative effects on the rear passivating contact. During the drive-in step, we suspect several interactions between the rear passivating contact and O$_2$ introduced into the furnace. First, oxidation could thicken the SiO$_x$ interfacial layer
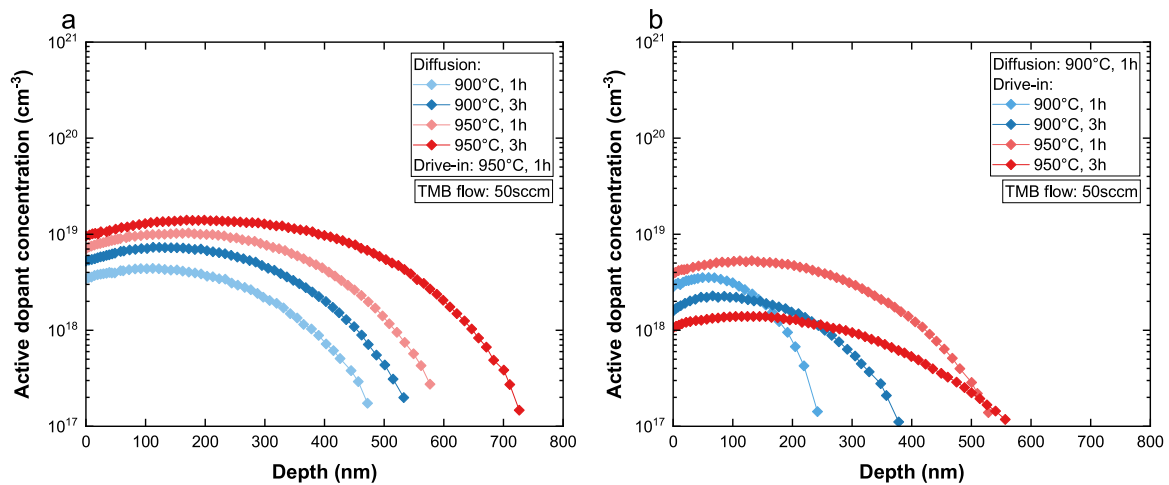
Fig. 8. Emitter profiles obtained with constant TMB flow of 50 sccm for (a) varying diffusion conditions and (b) varying drive-in conditions.

and thus increase ρ_c. Second, the rear poly-Si layer could oxidize and become less resistant to subsequent HF etching.

A preliminary experiment was carried out to evaluate the compatibility of the rear passivating contact with the drive-in step. For this purpose, symmetrical samples with a TOPCon SiO_x/poly-Si(n) structure were produced. The interfacial SiO_x layer was obtained by immersion in HNO_3 followed by exposure to UV radiation in an O_3 environment and nitrous oxide (N_2O) plasma treatment. The poly-Si(n) layer consisted of silicon-rich silicon carbide (SiC(n)) deposited by PECVD. After deposition, the samples underwent the entire manufacturing process for the front emitter formation (annealing and HF etching), with diffusion and drive-in conditions of 900 °C/1 h and 950 °C/1 h, respectively. They were then hydrogenated by deposition of a SiN_x:H layer followed by a firing step carried out at 840 °C. The SiN_x:H layers were finally removed by immersion in HF and ITO/Ag TLM patterns were sputtered in order to evaluate ρ_c by TLM. The passivation quality was evaluated by QSSPC and photoluminescence (PL) imaging after each step of the process. Different deposition conditions were studied, and the one that gave the most promising performance consisted of a poly-Si(n) layer that was made thick in order to resist thermal oxidation and subsequent HF etching. This condition gave iV_{oc} values of 701, 700 and 717 mV after annealing, HF etching and SiN_x:H deposition, respectively. However, iV_{oc} dropped to 699 mV after firing. Images acquired by optical microscopy suggest that this decrease in iV_{oc} was due to blistering. PL images showed non-uniform passivation quality after drive-in, and the ρ_c values were approximately 100 mΩ cm², which could be suitable for full-area rear metallization. Overall, this preliminary experiment showed that further optimization is needed on the rear passivating contact to avoid blistering and improve the uniformity of the passivation.

4. Summary and conclusion

In this study, we investigated a lean manufacturing process for TOPCon solar cells based on the successive PECVD-deposition of the front and rear doped layers, followed by a co-annealing step to simultaneously achieve front emitter formation and rear passivating contact activation. We showed that while only the emitter depth increases with the thermal budget, both the emitter depth and surface concentration increase with the doping gas flow, and that contact resistivity values below 10 mΩ cm² were achievable with our process. However, we obtained emitter profiles with too high surface concentrations and/or too shallow emitter depths. In addition, iV_{oc} values below 700 mV suggested that further improvements to the AlO_x/SiN_x:H passivation stack were needed and that the origin of recombination losses in the emitter region should be investigated further. To study this last point, we

compared the depth profiles of the active dopant concentration with the depth profiles of the total B concentration, and observed discrepancies between the two characterization techniques at concentrations above 10^{19} cm⁻³, suggesting the presence of electrically inactive dopants such as interstitial B clusters that could lead to an increase in defect density in the region close to the interface with the passivating dielectric.

Based on our understanding of the above-mentioned influences, we adapted our co-annealing process, initially carried out under Ar environment, by adding a drive-in step under O_2 environment. We showed that this two-step co-annealing process allows reducing the surface concentration and increasing the depth of emitters diffused from a plasma-deposited B diffusion source. This optimization of the co-annealing process enabled us to obtain an emitter profile with a surface concentration of 2.2×10^{19} cm⁻³ and an emitter depth of 880 nm, making it compatible with standard industrial metallization obtained by screen-printing and firing-through Ag–Al paste. We investigated the influence of the different co-annealing process steps in more detail and showed that this fabrication process offers highly adjustable emitter profiles.

Finally, we investigated the compatibility of the rear passivating contact with the optimized co-annealing process and obtained promising results with iV_{oc} and ρ_c values of approximately 700 mV and 100 mΩ cm² after the entire manufacturing process. However, the quality of the passivation after co-annealing was not uniform and blistering of the layers was observed after firing.

Further development of this lean manufacturing process will involve optimizing the front passivation with AlO_x/SiN_x:H and metallization, in order to improve iV_{oc} and reduce ρ_c. In addition, the deposition conditions for the rear passivating layers will be studied to make them compatible with the optimized co-annealing process. Although we seek to minimize wrap-around by using single-sided PECVD deposition, its presence and influence on shunt effects should be investigated in more detail. In the longer term, we aim to produce proof-of-concept co-annealed TOPCon devices with the introduction of the drive-in step in a O_2 environment, similar to the co-annealed devices we have previously reported without this latest development [18].

CRediT authorship contribution statement

Thibault Schaller: Writing – review & editing, Writing – original draft, Methodology, Investigation, Conceptualization. **Ezgi Genç:** Writing – review & editing, Methodology, Investigation, Conceptualization. **Julien Hurni:** Writing – review & editing, Methodology, Investigation, Conceptualization. **Ludovica Lunghi:** Writing – review & editing, Methodology, Investigation, Conceptualization. **Christophe Ballif:**

Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition, Conceptualization. **Audrey Morisset:** Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition, Conceptualization. **Franz-Josef Haug:** Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no conflicts of interest.

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Data availability

The raw data underlying the results of this contribution are available on the Zenodo repository under the following doi:10.5281/zenodo. 15279416.

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