Perspective

Polysilicon passivated junctions: The next technology for silicon solar cells?

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SUMMARY

Despite the maturity of crystalline silicon photovoltaics (c-Si PV), the last 6 years have seen a string of efficiency improvements, most of which are centered around reducing the losses related to the directly metallized, heavily doped regions found in conventional c-Si solar cells. Among these advancements, polysilicon (poly-Si) passivated junctions, formed by embedding a thin silicon oxide (SiO$_2$) layer between the c-Si wafer and a highly doped poly-Si layer, are emerging as one of the most promising alternatives, and efficiencies above 26% have already been demonstrated. The excellent performance of this junction architecture has been found to be remarkably independent of the deposition and/or doping technique used—even extending to techniques already prevalent in industry. This greatly reduces the capital and retraining expenditure needed to integrate the new technology into mainstream production lines, allowing it to be an evolutionary, rather than disruptive advancement. This has led to the rapid demonstration of large-area cells featuring poly-Si contacts by multiple PV manufacturing companies, with efficiencies above 24.5%. Although a bright future for poly-Si junctions is anticipated, as supported by the predictions of the International Technology Roadmap of Photovoltaics, several issues remain to be resolved, including those associated with the cost of and damage to the poly-Si layers due to the cell's metallization process. This paper provides a perspective of the remaining challenges and potential of poly-Si junctions to transform the PV industry.
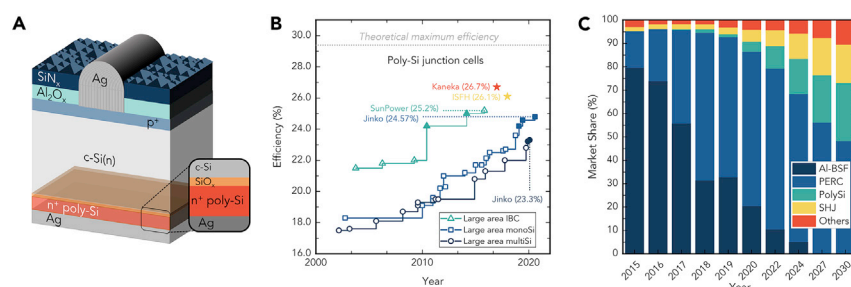
INTRODUCTION

Crystalline silicon (c-Si) solar cells have enjoyed longstanding dominance of photovoltaic (PV) solar energy, since megawatt-scale commercial production first began in the 1980s, to supplying more than 95% of a market entering the terawatt range today.[1] The rapid expansion of c-Si PV production has been accompanied by continual technological improvements that have enhanced performance and reduced costs, such that according to the International Energy Agency "solar projects now offer some of the lowest cost electricity ever seen."[2] The latest of these technological evolutions focuses on combining the functions of surface passivation and charge carrier selection, using what has come to be called "passivated" contacts, or junctions. Among the many approaches tested so far, those based on either hydrogenated amorphous silicon heterojunctions (SHJ) or on doped polysilicon (poly-Si) junctions are favored. The SHJ approach, which is not covered in this perspective, currently holds the c-Si efficiency record at 26.7%.[3] As a longstanding premium option, the SHJ technology continues to increase market share

Context & scale

After 40 years, crystalline silicon (c-Si) solar cells remain the clear leaders of the terrestrial photovoltaic market. This position is largely due to continual adjustments of the c-Si cell architecture, which have provided steady efficiency gains, together with drastic cost reductions brought about by large-scale manufacturing. To maintain forward momentum and lift the industry average power conversion efficiency to ~25%, the next major change to take place is the integration of "passivated contacts," which address the losses implicit to the metal-silicon contacts used in today's cells. Recent years have seen increased investment and rapid improvement in a few passivated contact technologies. The decision of when and which passivated contact scheme to adopt is not straightforward, requiring consideration of factors beyond the standard cost-to-performance ratio, such as ultimate efficiency potential as well as capital and retraining expenditure. This perspective focuses on one stream of future c-Si solar cells incorporating passivated contacts based on doped polycrystalline silicon/SiO$_2$ junctions, commonly called poly-Si junctions.

Figure 1. Current status and future growth of cells featuring poly-Si junctions

(A) Cross-sectional diagram of an n-type solar cell with a front boron-diffused junction and a rear phosphorus-doped poly-Si/SiO$_x$-passivated junction, commonly referred to as the TOPCon cell.

(B) Evolution of the conversion efficiency of industrial (large area) silicon solar cells that incorporate poly-Si passivated junctions.[13,14] The current record for such cells (26.1% laboratory size) is also indicated,[7] as well as the world record for c-Si solar cells (26.7%),[3] achieved with amorphous silicon heterojunctions. The upper limit conversion efficiency imposed by fundamental recombination mechanisms is indicted with the gray line at 29.4%.[15]

(C) Evolution of different technologies for silicon solar cells according to the 2020 International Technology Roadmap for Photovoltaics.[12] Al-BSF (aluminum back surface field), PERC (passivated emitter and rear cell), SHJ (silicon heterojunction), poly-Si (polysilicon/SiO$_x$ junction), and others (interdigitated back contact and tandem cells).

despite significant differences in production equipment and processes compared with those of the current mainstream c-Si PV technology.[4] This is in contrast with cells featuring poly-Si junctions, which utilize high-temperature processes and metallization techniques already prevalent in industry and hence can be viewed as an upgrade to the existing mainstream technology. As shown in Figure 1A, poly-Si junctions are formed by embedding a thin insulating layer of silicon oxide (SiO$_2$) between the c-Si wafer and a highly doped poly-Si layer. In the past 4 years, small-area (~4 cm^2) cells with poly-Si junctions have exceeded 26% conversion efficiency for both n- and p-type substrates with either "front- and back-contacted" or "interdigitated back contact" architectures.[5–7] These promising results have motivated a technology push among the large PV manufacturers to integrate poly-Si junctions into their high-efficiency production lines. The results of this push are clearly shown in Figure 1B, in which all solid markers, displaying recent large-area cell efficiency breakthroughs, use at least one poly-Si passivating junction. Many of the largest PV manufacturers have publicly reported research on poly-Si passivating junctions, including CanadianSolar, GCL, JinkoSolar, Jolywood, SunPower, TrinaSolar, and Yingli.[8–10] Of the three largest manufacturers, two have already built pilot lines that produce large-area cells featuring poly-Si junctions with efficiencies above 24.5%.[10,11] The International Technology Roadmap for PV (ITRPV) predicts that the uptake of poly-Si junction architectures will continue to grow over the next decade,[12] as shown in Figure 1C—amounting to almost 35% of the entire market, reaching industry average efficiencies of 24% and 24.5% for p- and n-type substrates, respectively, by the year 2030.

Complementing and updating previous reviews,[8,16,17] this paper provides a focused perspective, accessible to a generalized scientific audience, of poly-Si junctions and their potential to transform the PV industry, from the point of view of both academia and industry. It examines the physics, technological progress, and remaining challenges for poly-Si passivating junctions in c-Si solar cells. An overview of the current approaches for fabricating poly-Si junctions in both research laboratories and industry is given and compared in terms of their electrical performance, ease of implementation, reliability, and cost.

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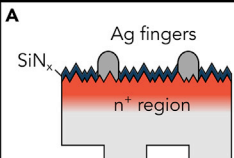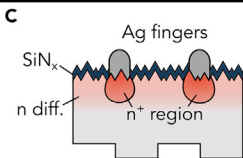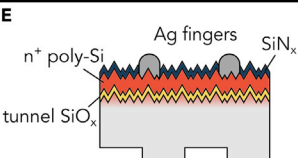
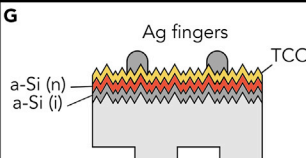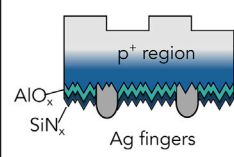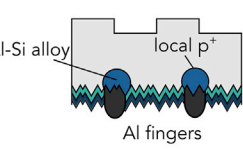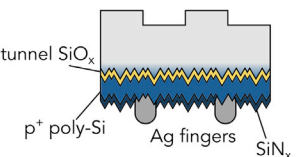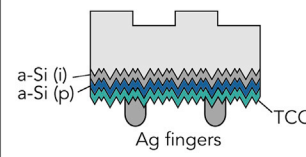[3]GCL System Integration Technology, Suzhou, China

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Figure 2. Toolbox of junction technologies based on doping crystalline, polycrystalline, or amorphous silicon

Typical values for the characteristic recombination current parameter J_0 attainable using today's technology are given for both the electron and hole-selective junctions, assuming a metallization fraction of 3% for Ag contacts and 4% for Al contacts. The whole surface $J_0 = f \times J_{0-metal} + (1 - f) \times J_{0-nonmetal}$, where f represents the metallisation fraction of either Ag or Al pastes, $J_{0-metal}$ represent the recombination current density under the metal contacts, and $J_{0-nonmetal}$ indicates the recombination current density in the dielectric coated regions. In the SHJ case, the whole-surface J_0 is the same for metal contacted regions and nonmetal contact regions. The corresponding data are obtained from references.[11,24–28]

CARRIER-SELECTIVE JUNCTION TECHNOLOGIES BASED ON DOPED SILICON

The optimization of c-Si solar cell design involves several interrelated factors. First, and most obvious, the number of photons absorbed by the c-Si solar cell must be maximized. Experimentally demonstrated cells with short-circuit currents $J_{sc} > 42$ mA/cm² are already approaching the theoretical optimum value of 43.3 mA/cm² for c-Si.[15] Less obvious is that the concentration of free electrons and holes held in the solar cell must be maximized, as their product determines the cell's voltage. For c-Si this can be increased up until fundamental processes like radiative and Auger recombination dominate, which limit the open circuit voltage to about 760 mV, and the maximum power point voltage to ~700 mV.[18] Once the device current and internal voltage are maximized, it is necessary to provide a preferred route for electrons and holes toward opposite metal terminals. These carrier-selective routes, typically achieved by junctions at the cell's surfaces, play a crucial role in all these processes. The performance of junctions is assessed by a pair of metrics; the junction or contact recombination factor J_0, which is minimal when the unwanted carrier is effectively blocked; and the contact resistivity ρ_c, which represents the resistance toward the collected carrier. Attempts have been made to combine these into a single "carrier-selectivity" metric,[19–21] but because of their widespread usage, J_0 and ρ_c are favored here.

The three most successful families of junctions, shown in Figure 2, utilize doped silicon layers to achieve selective carrier transport. The conventional approach, shown in Figures 2A–2D, is to introduce high concentrations of n-type (e.g., phosphorus) or p-type (e.g., aluminum and boron) dopants underneath opposite metal electrodes of the solar cell. This introduces several favorable mechanisms, as
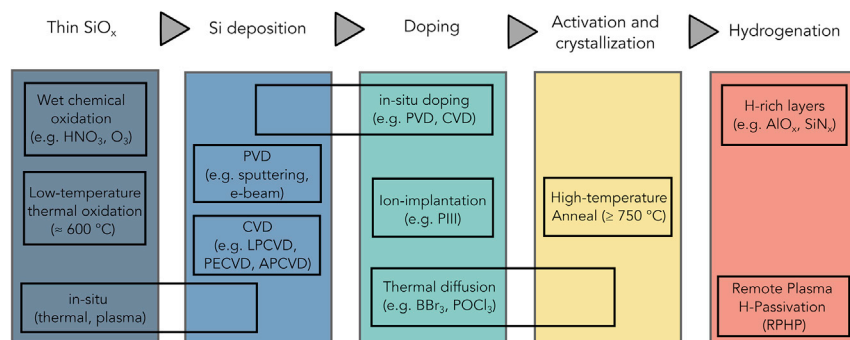
illustrated by the example of a phosphorus-doped n^+ region: the resulting high concentration of free electrons provides a high conductivity to the photoexcited electrons, both laterally and vertically, and it also facilitates direct tunneling through the barrier commonly found at c-Si/metal interfaces.[22] The high n^+ electron concentration also reduces the surface hole (minority carrier) concentration, even under illumination, which is the limiting driver for surface recombination. In addition, heavy doping introduces secondary benefits such as impurity gettering.[23] These reasons, and the comparative simplicity of creating shallow doped regions in the c-Si wafer absorber, explain why this approach has remained the dominant junction technology throughout the history of c-Si cell development. The latest iteration of this technology, which currently dominates the c-Si PV industry, is known as the passivated emitter and rear cell (PERC). Unfortunately, heavy doping also comes with fundamental limitations like Auger recombination and band-gap narrowing. A common strategy to address these losses is to apply heavy doping in the regions immediately under the metal electrodes, taking up just 3%–4% of the area, leaving the rest of the area to be moderately doped and covered by surface-passivating anti-reflection coating films such as silicon nitride (SiN_x), as shown in Figure 2A, or a stack of aluminum oxide (AlO_x) and SiN_x, as shown in Figure 2B. In the case of phosphorus doping, industrially compatible processes such as laser over-doping are increasingly being adopted to form such n^{++}/n^+ junctions. Although superior to the simpler uniform n^+ diffusion, the performance of these n^{++}/n^+ junctions is still dominated by recombination at the metal-silicon interface, with a typical metalized region J_0 of about 1,400 fA/cm^2, bringing the whole-surface J_0 to about 70 fA/cm^2.[24] In the case of p^+ doping, the dominant process in PERC cells is to create localized p^+ regions by using screen-printed aluminum as a contact and dopant source in about 4% of the surface and passivate the rest with an AlO_x/SiN_x stack (Figure 2D), which permits a whole-surface J_0 of about 30 fA/cm^2.[24]

The above limitations have urged researchers to seek alternative ways to form the necessary carrier-selective junctions without compromising either surface passivation or ohmic contact formation. Currently, the most successful ways to achieve passivated junctions are based on combining either doped poly-Si layers and an ultrathin SiO_x layer (see Figures 2E and 2F), or intrinsic and doped a-Si:H (see Figures 2G and 2H). These strategies both eliminate or minimize direct metal contact to, and heavy doping within, the c-Si absorber, the benefits of which can be seen by the lower J_0 values listed in Figure 2. There is a high degree of processing compatibility between the conventional and poly-Si junction technologies, which facilitates their concurrent use; for example, a popular combination is to use Figure 2B at the front and Figure 2E at the back of an n-type wafer.

It should also be mentioned that other junction technologies exist; for example, it is possible to deposit onto the c-Si wafer materials whose work function or band alignment makes them selective to either electrons or holes.[29–31] Such approaches are, nevertheless, at an earlier stage of research and not covered in this perspective.

DOPED POLYSILICON JUNCTIONS

Following a brief mention in 1981 to the possible use of poly-Si under the front metal grid lines,[32] no doubt inspired by earlier microelectronics research,[33,34] the first experimental demonstrations of poly-Si and semi-insulating poly-Si (SIPOS) junctions in c-Si PV were reported in the mid-1980s.[35–40] By the end of this decade many of the salient features of poly-Si contacts were already identified, such as the indispensable role of a thin interfacial oxide and the occurrence of dopant
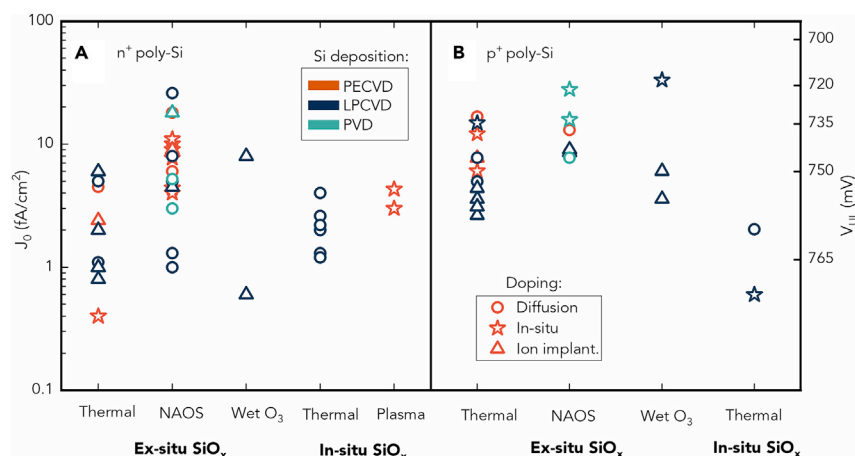
Figure 3. Building blocks indicating the main steps for the fabrication of poly-Si/SiO$_x$-passivated junctions
The horizontal rectangles indicate possibilities of performing two functions in a single step.

in-diffusion.[41] In 2005 Swanson, one of the early proponents of poly-Si in c-Si PV, pointed out that "new contacts" were needed for silicon solar cells to realize their ultimate potential[42] and filed a patent licensed to SunPower on the use of doped poly-Si layers deposited onto thin SiO$_x$ layers to make advanced "point contact silicon solar cells."[43] SunPower Corporation filed several more patents, including one that dealt with poly-Si/SiO$_x$ contacts[44] and explicitly mentioned the incorporation of "passivated contacts" into their interdigitated back contact cells from 2010,[45] subsequently achieving a 25.2% conversion efficiency in 2016.[46] Related bifacial cell structures were later developed by TetraSun (first patents filed in 2010)[47] and then Silevo (papers published in 2014)[48] each with passivated contact variants between SHJ and poly-Si/SiO$_x$ and copper plating metallization. Despite the interest in these architectures, none of them were able to achieve massive penetration of the c-Si PV market.

Perhaps because much of the abovementioned work took place in the secrecy of industrial environments, poly-Si junctions received comparatively little attention from the c-Si PV research institutes for >20 years after the 1980s. That changed in 2013 when researchers from Fraunhofer ISE presented 23.3% efficient n-type Si cells incorporating at the rear what they called a TOPCon (tunneling oxide passivated contact) consisting of a recrystallized Si film deposited onto an ultrathin SiO$_x$.[49] Coincidentally, Brendel et al. from ISFH, also presented at the same conference initial J_0 and ρ_c results for what they called POLO (polysilicon on oxide) junctions.[50] These results marked the beginning of a resurgence of interest in poly-Si junctions among c-Si PV researchers, and in the following 6 years more than ten PV institutes and a handful of companies reported cell efficiencies in the 21%–26% range using them. The broad demonstration of compelling results in recent years reflects both the replicability and robustness of the poly-Si/SiO$_x$ junction technology and the ease in which it can be implemented using equipment available at most PV laboratories, particularly for phosphorus-doped poly-Si.

Contemporary approaches for the fabrication of poly-Si/oxide junctions involve five generic building blocks, as shown in Figure 3: (1) growth or deposition of a thin interfacial layer, generally SiO$_x$, (2) deposition of a silicon/silicon compound film, (3) incorporation of dopants into the silicon film, (4) recrystallization of the silicon and activation of the dopants, and (5) hydrogenation. Two or more of these interdependent building blocks are commonly combined into a single processing step.
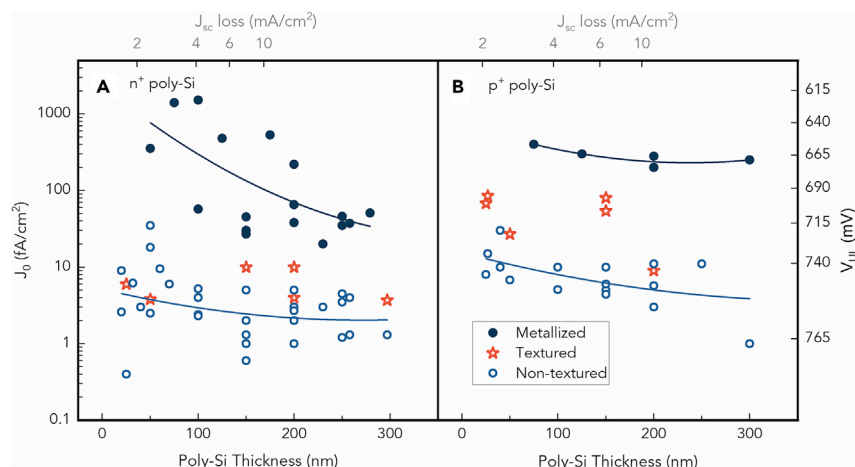
Figure 4. Recombination behavior of poly-Si junctions formed via different fabrication approaches

Recombination current density J_0 (left axis) and upper limit voltage V_{UL} (right axis) achieved for different techniques to grow the interfacial oxide, for both n^+ poly-Si (Figure 4A) and p^+ poly-Si (Figure 4B) junctions. V_{UL} has been estimated with an additional 5 fA/cm^2 recombination contribution from an Auger-limited 150-μm Si wafer. Thermal, dry O_2 thermal oxidation; NAOS, hot nitric acid oxidation of silicon; Wet O_3, ozonized water oxidation; Plasma, O_2 plasma oxidation. *Ex situ* SiO$_x$, SiO$_x$ is grown in separate processing step; *In situ* SiO$_x$, SiO$_x$ is grown immediately prior to Si deposition in the same chamber. These data points were obtained from references.[7,11,27,54,56,59,60,63–98]

In terms of suppressing recombination, the interfacial layer is key for the separation of the poly-Si layer from the c-Si absorber. During the dopant activation process, the interfacial layer works as diffusion barrier to reduce the penetration of dopants into the c-Si absorber and prevent epitaxial growth of the poly-Si film onto it. With very few exceptions,[51,52] sub-stoichiometric silicon oxide SiO$_x$ is used for the thin (1–3 nm) interfacial layer. This is commonly grown either chemically, by immersion in hot ~90°C nitric acid, which produces a self-limited ~1.4 nm film,[53] or thermally, at 550°C –700°C in O_2 for short periods (e.g., 10 min to obtain ~2 nm).[54] Alternative processes based on UV/ozone and ozonized deionized water have also been trialed.[55] However, provided that the remainder of the fabrication scheme is adjusted in accordance with the SiO$_x$ thickness (thicker interfacial layers require higher recrystallization and activation temperatures) the resulting J_0 and ρ_c are surprisingly uniform. As shown in Figure 4, $J_0 < 10$ fA/cm^2 have been demonstrated for n- and p-type poly-Si/SiO$_x$ junctions using a range of SiO$_x$ growth techniques.[55–60] Due to this uniformity of results, recent attempts have instead focused on integrating the SiO$_x$ growth with the subsequent deposition of the Si layer, for example, using a plasma enhanced or low-pressure chemical vapor deposition (PE/LP CVD) chamber.[61–63] These too have already yielded results in line with those highlighted above.

Multiple CVD and physical vapor deposition (PVD) techniques have been successfully used to deposit the Si layer in poly-Si/SiO$_x$ junctions. Low-pressure CVD of poly-Si, performed by thermally cracking silane (>500°C) in a low-pressure quartz tube, is currently the preferred method in industry.[10,11,25,64,99] The high uniformity and consistent performance of this technique is however partially offset by the non-directional nature of deposition and the need to remove poly-Si from one side of the wafer. Plasma enhanced CVD, a directional deposition technique performed by plasma cracking of silane and other precursors at low temperature

Figure 5. Recombination and current losses from poly-Si junctions as a function of poly-Si thickness

(A and B) Recombination current density J_0 (left axis) and upper limit voltage V_{UL} (right axis) for both: (A) n$^+$ poly-Si; and (B) p$^+$ poly-Si junctions as a function of the thickness of the poly-Si layer. The upper points and trend lines correspond to layers that have been metallized by screen printing. Also shown in the top horizontal axis is the estimated loss in the short-circuit current density if such layers are placed at the front of the solar cell, which is based on Reiter et al.[110] The lines provide a guide to the eyes only. Metallized = J_0 measured on metallized polysilicon surface. Non-textured = J_0 measured on planarized surfaces, Textured = J_0 measured on textured surfaces. The data were obtained from references.[7,11,27,54,56,59,63–68,70–86,88–98,110]

(<500°C), is already pervasive in the PV industry for the deposition of SiN_x, Al_2O_3, and SiO_x films for surface passivation and antireflection, and is also used to deposit a-Si:H in silicon heterojunction cells.[18,29] Although the high concentration of hydrogen in the deposited layers is necessary in those applications, it can lead to the formation of blisters in poly-Si films, particularly for the thicker poly-Si films needed to withstand damage during fire-through metallization process.[100,101] Regardless, PV researchers and equipment manufacturers are still motivated to implement PECVD into the mass production lines due to its ability to deposit selectively on one side.[65] After the initial work at Fraunhofer ISE,[66] many other research institutes have reported results using PECVD on par with those achieved by LPCVD.[54,57,62,100,67,102,103] Other single-side CVD methods that have been used to form poly-Si junctions include atmospheric pressure CVD (APCVD) and Hot Wire CVD,[68,104,105] although they are not as widespread. PVD such as sputtering and electron beam evaporation are very promising as a single-side deposition alternative. Compared with CVD, the main advantages of PVD are the absence of dangerous precursor gases (such as silane and diborane), the ability to deposit dense films with low or no hydrogen content (removing blistering issues),[69,70,106] and low temperature deposition (down to room temperature). Although PVD is an integral part of SHJ technology (to deposit transparent conductive oxides), its use for depositing poly-Si films in industry is still under development.[107,108]

The thickness of the deposited Si layer can have a significant impact on junction performance, as shown in Figure 5, for several reasons. First, photons absorbed in poly-Si are lost to recombination (although a recent study suggests a small percentage of minority carriers generated in the poly-Si might be collected).[109] Doped poly-Si has an absorption coefficient similar to that of c-Si, and the loss in J_{sc} caused by such "parasitic absorption" has been quantified as 0.4–0.5 mA/cm^2 per 10 nm of poly-Si, when placed at the front of the solar cell,[110,111] as depicted in the top x axis of Figure 5. In addition, the

free charge carriers present in the poly-Si layer absorb infrared photons, much in the same way as they do in c-Si.[110] This loss also occurs when the poly-Si layer is placed at the back of a solar cell, amounting to 0.3–0.5mA/cm^2 (depending on doping) for a 140-nm-thick poly-Si layer.[112] Although increasing poly-Si thicknesses increases J_{sc} losses, it also decreases J_0 particularly for n$^+$ poly-Si films contacted with screen-printed metal pastes, as shown in Figure 5. This trade-off has made it difficult to apply poly-Si junctions to the sunward side of solar cells. To reduce the optical losses several groups have looked at the dilution of the poly-Si layer with small concentrations of oxygen and carbon,[112,113] broadening the band gap but often at the expense of device fill factor, or selective thinning/etching of the poly-Si in the non-metallized regions.[114]

The doping level of the poly-Si layer has a strong impact on the electrical performance of the poly-Si/SiO$_x$ junction. A low dopant concentration (below 10^{19} cm^{-3}) results in high J_0 and ρ_c, whereas a high concentration (above 10^{20} cm^{-3}) can lead to excessive oxide breakup and dopant penetration into the c-Si substrate, resulting in increased J_0.[100,111,113,71,72,115] Dopant incorporation can be achieved by a variety of methods, such as *in situ* deposition together with the silicon film, ion implantation, or thermal diffusion.[49,59,116] *In situ* doping, the most direct method, is possible in both LP- and PE-CVD by mixing controlled rates of PH$_3$, B$_2$H$_6$/BCl$_3$ with silane, for n-type and p-type doping, respectively. However, the deposition rate of the *in-situ*-doped silicon is one order of magnitude lower than undoped silicon, and the final films have a poor lateral uniformity.[117–119] In PVD, *in situ* doping can be achieved by using solid sources, for example, a GaP thermal effusion cell in the case of electron beam deposition,[106] or an elemental boron target in the case of sputtering.[69] Among the *ex situ* doping methods, thermal diffusion is the most popular, as diffusion furnaces are ubiquitous in PV industrial production lines, especially for n-type doping using POCl$_3$ vapor as the source, but increasingly also for p-type doping, using BBr$_3$/BCl$_3$ vapor sources.[11,54,56,59,64,25] Alternatively, liquid spin-on or spray-on dopants, dopant inks or pastes can be used to form patterned doped regions, with promising results already shown for P, B, and Ga based films.[120–122] An advantage of all thermal diffusion approaches is that the recrystallization of the Si film and the activation of the dopants occur during the same process, making a separate high-temperature step unnecessary. Such a step is required for ion implantation, whose ability to control both depth and lateral dopant distributions has been particularly useful to achieve a 26.1% poly-Si based interdigitated back contact (IBC) solar cell.[7] Despite its flexibility and promising laboratory scale results, it is challenging to implement ion implantation in the PV industry due to its high running and maintenance cost, as well as its difficulty in meeting the continually increasing throughput requirements. However, we note the use of plasma immersion ion implantation (PIII) might reduce costs and increase throughput.[123,124]

As mentioned above, unless thermal diffusion is used to dope the poly-Si layer, a separate high-temperature annealing step, usually performed in a quartz furnace, is necessary to activate the dopants and recrystallize the silicon. The final doping profile, the degree of crystallization of the silicon film, control of the dopant "tail" in the c-Si absorber and the interfacial layer properties, all of which determine the performance of the poly-Si junctions, depend strongly on the temperature and time of the activation step.[59,68,125] The optimization of this dopant activation step follows a similar set of rules as that of a thermal dopant diffusion step, which adds weight to the use of the latter. Alternatively, it would be desirable to combine the dopant activation step into the "firing" of the screen-printed metallization. Firing is a rapid thermal step reaching temperatures in the range of 750°C–850°C for only a short period of time (<1 min), which greatly limits the time for recrystallization,
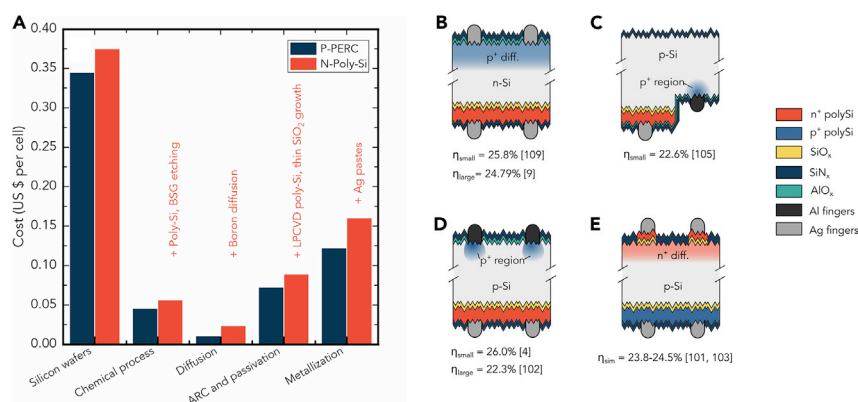
dopant activation, and dopant diffusion into the c-Si wafer. Despite that, good p-type poly-Si junctions with a J_0 ~11–14 fA/cm^2 have been demonstrated using this rapid annealing process, although not yet with metallization.[126,127] A final hydrogenation step, which passivates unsatisfied bonds within the contact structure, can improve the surface passivation by more than an order of magnitude. Such hydrogenation can be realized using a remote hydrogen plasma or by capping with films that contain atomic hydrogen.[54,64,66,73] The latter approach, particularly when using PECVD SiN$_x$, has the added advantage of being an integral part of existing industry processes. The abovementioned firing step can also be used to release the hydrogen from a SiN$_x$ layer, a process that has already been shown to enhance performance stability of the poly-Si junctions.[64,73,128]

Despite the uniformity of results using different fabrication steps shown in Figures 4 and 5, a consistent trend of lower J_0 for phosphorus-doped, versus boron-doped, poly-Si contacts has been observed. This can largely be ascribed to the segregation of dopants; phosphorus' segregation coefficient is much higher at the poly-Si/SiO$_x$ interface compared with boron (more than three orders of magnitude).[129,130] This greatly reduces the amount of phosphorus diffusing into the SiO$_x$ and beyond into the c-Si absorber. Conversely, boron-doped poly-Si layers commonly end up with a high concentration of boron in both the SiO$_x$ layer, which can increase surface recombination, and within the c-Si absorber, which increases Auger recombination.[52,56,111]

INDUSTRIAL ADOPTION

The recent interest in poly-Si junctions is driven by the ever-present push toward higher efficiencies, which not only improves the module $/W ratio but also reduces the balance-of-systems costs. Aside from market forces, this push has been promoted by government policies, particularly in China, the world's largest PV producer, where the "Top Runner Program" has, since 2015, encouraged through rebates the sale of PV products that exceeded a moving efficiency benchmark, set in 2017 at 21.6% for mono-crystalline silicon. This has created an excellent environment for the integration of a higher efficiency poly-Si technology. Given the very low J_0 and ρ_c parameters already achieved, the ultimate conversion efficiency of c-Si solar cells featuring poly-Si junctions in research environments is largely determined by other factors, such as the quality of the silicon wafer, the optical losses, and the particular design of the device. For example, based on the highest carrier lifetimes measured for c-Si,[131] the lowest achievable recombination in the bulk of a silicon wafer can be estimated as J_{0bulk} 5–9 fA/cm^2 (for wafer thicknesses of 100–180 μm). This means that the best poly-Si J_0 values reported thus far would not be an impediment to achieve conversion efficiencies in excess of 27%, assuming an unconstrained architecture and budget. In an industrial environment, where there is less flexibility, the practical efficiency will most likely be in the 24%–25% range,[132] and indeed large-area cells with efficiencies >24% already confirm the feasibility of these figures.[10,11]

The same drivers mentioned above explain the increasing market share of solar cells based on n-type Si wafers, which, as shown in Figure 1, is expected to reach 50% by 2030. Phosphorus-doped n-type silicon has long been the material of choice for high-efficiency industrial devices, including IBC and SHJ cells. This is largely because n-type Si is exempt from boron-oxygen defects and the associated light-induced degradation, is more tolerant of most metal impurities, and thus usually presents a higher minority carrier lifetime than p-type.[133,134] In cell structures that rely on

Figure 6. Industrial exploration of cells featuring poly-Si junctions

(A) Manufacturing cost comparison between p-type PERC and n-type poly-Si-junction cells, including the cost of materials (silicon wafer) and the four main process categories, from Kafle et al.[135] BSG, borosilicate glass.

(B–E) Solar cell structures currently being developed for the industrial adoption of poly-Si-passivated junctions. η_{small}, best cell efficiency demonstrated on small-area cells (~4 cm^2); η_{large}, best cell efficiency demonstrated on industrial scale cells; η_{sim}, simulated average practical efficiency limit for industrial solar cells.

lateral transport of majority carriers, n-type silicon also offers approximately three times better conductivity than p-type c-Si at equal doping. Not surprisingly, the first application of poly-Si junctions has been to n-type Si cells (Figure 6B), where it has proved its worth by lifting the efficiency of champion cells made in R&D production lines up to 24.79%.[10] Nevertheless, although PV companies trialing the adoption of poly-Si technology are universally reporting higher cell efficiencies, cost competitiveness remains a major challenge. According to a recent study by Kafle et al.[135] the cost of an n-type solar cell with a front boron diffusion and a rear n$^+$ poly-Si layer is 18% higher than the cost of a p-type PERC cell (0.07042 versus 0.05965 $/cell, assuming 161.75 mm per side square wafers). Figure 6A shows that, in addition to the costs of boron diffusion and LPCVD Si film deposition, which are relatively low, the cost difference is mainly due to the use of n-type wafers instead of p-type and to the cell's metallization. In particular, the largest extra costs originate from the need to use silver to contact both the front boron diffusion and the rear poly-Si layer of the n-type cells. In terms of $/W, this cost gap can be compensated for if PV modules made with poly-Si junctions have at least a 0.4% higher conversion efficiency than conventional PERC modules. It can be expected that equipment development and production optimization relevant to poly-Si based architectures will drive significant yield increases and cost reductions, further reducing the cost gap between n-type poly-Si cells and p-type PERC. There are also options for future architectural improvements to the industrial n-type poly-Si cell, such as the addition of a selective p$^+$ diffusion underneath the metal grid, like most laboratory record cells do, or a selective boron-doped poly-Si junction, as some incipient laboratory experiments indicate.[114,74]

TECHNICAL CHALLENGES

The adoption of poly-Si based junctions is compromised by passivation damage during conventional screen-printed metallization processes. This degradation is mainly associated with the removal of poly-Si and the appearance of etch pits underneath the metal fingers during firing[75,76,136] and is generally more pronounced the thinner the poly-Si layer is, increasing the J_0 by up to two orders of magnitude, as

shown in Figure 5. An additional complicating factor is the need to optimize hydrogenation from the SiN_x:H layer during the firing step at the same time as the ρ_c. At low firing temperatures <750°C the passivation quality of poly-Si layers in the metallized regions is similar to that in the non-metallized regions, at the expense of a high ρ_c (up to 100 $m\Omega$-cm^2).[75–77] The opposite occurs at high firing temperatures >750°C, and as such, the balancing of paste formulation and firing conditions is a major area of active development for research institutes and paste manufacturers. Already significant progress has been made, with screen-printed metallized poly-Si contacts attaining J_0 values <30 fA/cm^2,[11,65,77] which can permit whole-surface J_0 down to 6 fA/cm^2. Another option is electroplating, possibly combined with a thin seed layer. Metallization by plating has been demonstrated in industrial production,[9,48,137] and it allows the use of cheaper metals like copper to avoid the high cost of silver. It also permits to use much thinner poly-Si layers, down to ∼20 nm for better optical response. Feldmann et al. have demonstrated 22.9% large-area n-type silicon solar cells with poly-Si contacts having a Ni/Cu plated metal grid.[138] Kluska et al. indicated the cost of ownership (COO) of solar cells with a single (double)-sided plating was 16% (41%) lower than that of cells with double screen-printed metallization.[139,140] Nevertheless, environmental concerns and regulations (mainly due to waste disposal) can hinder the use and cost of large volumes of plating solutions. Regardless of the metallization method, it is likely that further improvements in metallization of poly-Si junctions will be made soon, and strategies such as multi-bus bars smart-wire will likely play a role in this.

Surface texturing, a necessary light trapping feature in c-Si solar cells, also introduces a challenge for poly-Si junction adoption. This is particularly true given the growing trend toward bifacial cells, where both surfaces should preferably be textured. Pyramidally textured surfaces are challenging to passivate due to the presence of sharp tips, edges, and deep valleys. The J_0 of poly-Si junctions on textured surfaces is approximately 10× higher than that on planar (100) surfaces, irrespective of the SiO_x growth method and silicon deposition technique. The increased J_0 can be attributed to the higher defect density at the SiO_x/(111) c-Si interface, thickness nonuniformities in the SiO_x and poly-Si layers,[78] and nonuniform dopant diffusion profiles over the pyramidal features.[78,141] A slight etching of the pyramid tips helps to improve the J_0 without incurring excessive reflectance losses.[11,142] Together with an optimized diffusion process and hydrogenation from SiN_x this has allowed the achievement of $J_0 < 5$ fA/cm^2 values for poly-Si passivated textured surfaces.[11,73]

FUTURE DEVICE ARCHITECTURES

Although until now poly-Si junctions have mainly served to enhance n-type cells, p-type Si wafers will remain the workhorse of the industry for several years, particularly considering the ongoing shift from boron to gallium as the preferred dopant, which may reduce in-field degradation. Hence, it is desirable to develop ways to incorporate poly-Si junctions into p-type c-Si wafers. In p-type PERC cells the combination of AlO_x/SiN_x on 96% of the surface and localized Al-doped p^+ regions on the remainder gives a low J_0 of ∼30 fA/cm^2.[24] A full-area boron-doped poly-Si junction can achieve lower values, in the range of $J_0 \sim 6$-10 fA/cm^2, after hydrogenation, but that gives only a 0.2%–0.4% improvement to the conversion efficiency.[143] This is because a passivated p^+ contact on the rear does not address the main limitation of current PERC cells, which is the front n^+ diffusion,[24] mostly due to recombination underneath the metal grid. A possible way to address such limitation is to implement an n^+ poly-Si contact underneath the front Ag metal

grid while retaining the current localized Al-doped p$^+$ regions at the back. The estimated efficiency for this approach is 24.1%, compared with a reference value of 23.7% for an optimized PERC structure.[24] If poly-Si junctions were used at both the front (localized n$^+$ poly-Si) and back (full area p$^+$ poly-Si) sides (Figure 6E) then the efficiency could increase by up to 0.6%–0.7%.[143]

A drastically different pathway for improving p-type silicon cells is to turn the PERC structure upside down, moving the n$^+$ junction to the back, and the localized p$^+$ regions to the front (Figure 6D). This permits to use n$^+$ poly-Si at the back without excessive optical losses, just like in the n-type TOPCon cell structure. In addition, by using narrow, closely spaced metal fingers at the front it is possible to restrict the front p$^+$ region to just under those fingers and rely on the conductivity of the p-type wafer to transport holes laterally. Such localized p$^+$ regions can be formed by boron diffusion, as demonstrated by the 26% lab prototype cell made by Richter et al.[6] Or they can be formed using the same Al-alloying technique currently used for PERC cells, as demonstrated by the 22.3% large-area device recently reported.[144] In addition to its compatibility with current PERC technology, this promising approach with a practical efficiency limit of 24.7%[26] also addresses one of the economic challenges mentioned above for n-type cells with a rear n$^+$ poly-Si layer (Figure 6B), given that it just needs one Ag metal grid at the back. Nevertheless, Al metal lines are generally wider than Ag ones, causing comparatively more shading at the front, and, in addition, this back-junction cell structure relies on the p-type wafer being of very high quality.

As the 26.7% current world record for Si solar cells attests, an interdigitated back contact structure permits to achieve the highest conversion efficiency under standard testing conditions.[3] Kruse has estimated that industrial-size IBC cells with poly-Si contacts of both polarities can realistically achieve an efficiency of 25.8%.[132,26] To make the fabrication of IBC cells more like that of PERC, ISFH researchers have used a screen-printed Al paste to form the p$^+$ region at the back, together with interdigitated n$^+$poly-Si regions (Figure 6C), achieving an efficiency of 22.6% in small-area lab prototypes.[145] Nevertheless, albedo-collecting, bifacial solar cells are increasingly being recognized as a clear pathway toward lower LCOE (levelized cost of energy), and this makes classical two-sided cell architectures more attractive for large-scale applications.

Finally, progression closer to silicon's single junction fundamental efficiency limit at 29.4% has prompted research into tandem cell architectures that can extract more energy from the solar spectrum. In particular, the last 6 years have seen dramatic improvements in tandems based on a metal halide perovskite cell stacked atop a c-Si cell, whereby the perovskite efficiently absorbs the visible portion of the spectrum and the c-Si absorbs the near infrared. Although most leading results thus far utilize the SHJ architecture in the c-Si bottom cell,[146] the recent results achieved with poly-Si junctions offer new possibilities. Poly-Si junctions have excellent thermal stability, withstanding anneals above 450°C without damage. This is a useful characteristic in the two-terminal perovskite/c-Si configuration as it allows the deposition of the perovskite's bottom contact at higher temperature, for example the deposition of TiO$_x$ at 450°C.[147,148] The temperature stability of poly-Si junctions also permits the use of all-inorganic perovskite absorbers, which many believe have greater potential for stability, but which require temperatures >200°C for deposition. It has also been shown that a boron-doped poly-Si layer used as the top junction in the c-Si cell can directly contact a TiO$_x$ bottom electron contact of the perovskite top cell. This advantage, which can likely be extended to other metal oxide contacts in combination with poly-Si, removes the need for an

additional transparent conductive oxide layer (sometimes called the "recombination layer"), which both simplifies the fabrication and reduces parasitic absorption.[149]

CONCLUSION

Silicon solar cell architectures featuring poly-Si based junctions are poised to become the next evolutionary step for mainstream silicon PVs, paving the way toward an average industry cell efficiency of 25% over the next decade. The largely uniform results across multiple poly-Si fabrication procedures speaks to the versatility of the approach and the potential for transfer to low-cost techniques, which has become a dominant research focus. Several candidate cell architectures are being explored with both n- and p-type substrates, most of which offer a ~1% absolute lift in efficiency over the current industry dominating PERC technology. Early trials, particularly on the n-type "TOPCon" architecture, suggest rapid < 5-year technology transfer time, due largely to its compatibility with existing production tools and expertise. However, several challenges remain to be met, most associated with the cost and performance of poly-Si junction metallization. These challenges are largely responsible for the current ~18% higher manufacturing cost of poly-Si junction cells compared with PERC. Given the early stage of development, this margin is expected to decrease, as informed by the rapid decrease in PERC costs during its first years of production. Although it is useful to compare them, the two technologies should not be regarded as excluding each other. Rather, poly-Si junctions provide a pathway for upgrading current PERC technology, and it is likely that over the next decade both architectures will develop further, alongside other solar cell technologies, including silicon heterojunctions.

DECLARATION OF INTERESTS

C.Z. is an employee of GCL System Integration Technology. Y.W. is an employee of Risen Solar Technology. X.Z. is an employee of Zhejiang Jinko Solar. Y.W., X.Z., D.Y., and A.C. hold various patents relevant to poly-Si junction technologies.

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