Applied Physics Reviews REVIEW scitation.org/journal/are

Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies

Cite as: Appl. Phys. Rev. **7**, 021305 (2020); doi: 10.1063/1.5139202
Submitted: 18 November 2019 · Accepted: 5 March 2020 ·
Published Online: 24 April 2020

Martin Hermle,[a] Frank Feldmann, Martin Bivour, Jan Christoph Goldschmidt, and Stefan W. Glunz

AFFILIATIONS

Fraunhofer Institute for Solar Energy Systems, ISE, Heidenhofstraße 2, 79110 Freiburg, Germany

[a]Author to whom correspondence should be addressed: martin.hermle@ise.fraunhofer.de

ABSTRACT

The efficiency of photovoltaic energy conversion is a decisive factor for low-cost electricity from renewable energies. In recent years, the efficiency of crystalline silicon solar cells in mass production has increased annually by about 0.5–0.6%$_{abs}$ per year. In order to maintain this development speed, new technologies must be developed and transferred to industrial production. After the transition from full area Al back surface field cells to passivated emitter and rear contact cells, passivating contacts are an important step to get as close as possible to the efficiency limit of single junction Si solar cells. The theoretical background and the two prominent technologies for passivating contacts are presented and discussed. After implementing passivating contacts, the fundamental limit of single junction Si solar cells of 29.4% is in reach. Multi-junction solar cells are the most promising option to achieve efficiencies greater than 30%. Tandem technologies based on crystalline silicon as bottom cells have the advantage that they are based on a mature technology established on a gigawatt scale and can partially use the existing production capacity. In addition, silicon has an ideal bandgap for the lower subcell of a tandem solar cell. The two most promising material candidates for the top cell, i.e., III/V and perovskites, will be discussed. The presented technology routes show that silicon is able to maintain its outstanding position in photovoltaics in the coming years.

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I. INTRODUCTION

Crystalline silicon solar cells are dominating the photovoltaic market for decades. One of the reasons for this predominance is that modules based on crystalline silicon had a cost degression of around 24% per year for over 30 years.[1] This strong cost reduction is based, on the one hand, on the constant increase in throughput of the production tools[1] and the reduction of material costs, starting from the silicon wafer up to module production. A second factor that has led to a reduction in module costs and above all to system costs is the increase in efficiency at the cell level. Due to the fact that many system costs are area-related costs (e.g., mounting and cabling), modules with higher power lead to lower system costs and thus to a lower levelized cost of electricity (LCOE). In addition to cost considerations, the sustainable use of resources is a key argument for solar cells with higher efficiencies. Solar modules with a higher efficiency lead to a more effective use

of materials, require less energy during production, and require less space to produce electrical energy. Thus, highly efficient solar cells are using the available space (e.g., roof top areas or, in the future, vehicles) and the system components more effectively. This way of increasing the efficiency further is a key requirement for the lower LCOE.

In the production of solar cells, it is possible to increase the efficiency through different developments. In recent years, this has mainly been achieved through incremental process improvements. Figure 1 shows the efficiency increase in mass and pilot line production at Hanwha Q-Cells from 2010 to 2019.

Until 2013, silicon solar cell production almost exclusively produced aluminum back surface field (Al-BSF) solar cells. Since the beginning of solar cell production on a MW scale at the beginning of the 2000s, this cell structure has not changed significantly, but the efficiency increased yearly by around 0.5–0.6%$_{abs}$. The main reasons for the efficiency increase included the improvement in the material quality of the silicon wafer, improvements in the rear side Al pastes leading to better BSF, the front grid Ag metal paste with regard to contact of lower doped emitters, and the width of the resulting metal fingers, as well as optimization of the front phosphorus emitter. In 2012, the efficiency of the Al-BSF cell stagnated at approximately 20% and could not be further increased. The main reason for this efficiency limit is the full-area aluminum rear contact with the Al-BSF alloyed into the rear side of the cell. This back contact limits, on the one hand, the open circuit voltage of the device, due to the high recombination current of J_0 ~200 fA/cm^2.[3] On the other hand, the light capture of the long-wavelength photons is limited since the Si/Al backside only has a backside reflection of approximately 60% (Ref. 4), which leads to a reduced short-circuit current of the solar cell. The recombination of the rear Al-BSF could be slightly reduced by the addition of boron,[3] but the basic limitation of this backside structure could not be reduced significantly. Interestingly, the limitation of the Al-BSF cell has also led to a focus on the industrialization of new technologies that can circumvent the existing limitations of the Al-BSF cell.

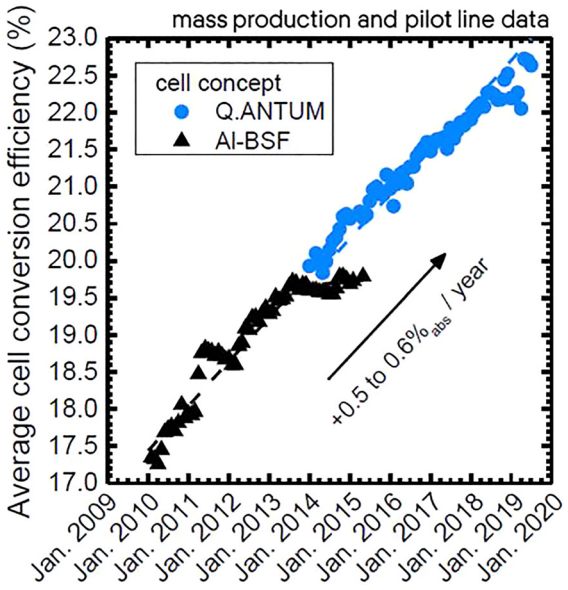

FIG. 1. Evolution of avg. cell efficiency in mass and pilot line production at Hanwha Q-Cells from 2010 to 2019. Q.ANTUM technology is the passivated emitter and rear contact cell (PERC) trademark from Hanwha Q-Cells.[2]

The PERC[5] (Passivated Emitter and Rear Contact) solar cell (labeled as Q.ANTUM in Fig. 1) can surpass the performance of the Al-BSF cell by utilizing a dielectric layer between Si and aluminum that passivated the surface better than the Al-BSF and, at the same time, enabled an optical mirror with reflection values of over 90%.[4] In the original PERC cell, Ohmic contacts with an evaporated Al layer were used. In the original Al-LBSF (Local Back Surface Field) cell,[6] Al evaporated and an annealing step was used to form the alloyed local BSF. In industry, the local rear contacts are made via local laser openings in the dielectric layer and an alloying step of screen printed Al to create the local Al-BSF (similar to the Al-BSF cell but limited to about 1% of the rear surface). These changes in the cell structure allowed the industry to stay on the 0.6%$_{abs}$ per year efficiency improvement path. The highest efficiency of a laboratory scale PERL (Passivated Emitter and Rear Locally Diffused) cell using locally diffused boron BSFs is 25% (Ref. 7), which was a long-lasting record for silicon cells until 2014. However, a basic limitation of these kinds of cell structures is that the highly recombinative metal-semiconductor contacts have to be made smaller and smaller in order to reduce the contribution to the overall recombination. It is difficult to predict which efficiencies PERC/PERL solar cells can achieve on an industrial scale using economically relevant processes. In a very extensive simulation study, Min *et al.* have shown that efficiencies of up to 24% are possible,[8] with technologies principally available. Thus, if industry wants to stay on the efficiency learning curve of 0.6%$_{abs}$ per year, new technologies have to be implemented.

In this review paper, two approaches to achieve such high efficiency silicon based solar cells will be presented: the first, passivating contacts, for the next generation of single-junction silicon solar cells, and the second, multi-junction cells, for medium-to-long-term implementation.

All silicon solar cells with efficiencies above the 25% PERL cell feature passivating contacts. Thus, the principle concept of passivating contacts will be presented in the Sec. II, and the two most important implementations will be described in more detail. With the implementation of this technology, efficiencies of nearly 27% are achieved, which is very close to the theoretical limit of single junction silicon solar cells.

This limit of 29.4%,[9] which results from unavoidable spectral losses and Auger recombination in the silicon material, can be overcome by adding a second solar cell to the silicon solar cell. Such multi-junction concepts will be discussed in the second part of this paper.

It will be shown that by introducing these technologies, the yearly efficiency improvement of silicon solar cells can be maintained, which is one requirement to stay on the cost reduction curve for the LCOE of photovoltaics.

II. PASSIVATING CONTACTS

A. Theory of passivating contacts

The fundamental requirement of electrical contacts in solar cells is the extraction of photo-generated electrons and holes from the device. A crystalline silicon solar cell consists of a silicon wafer, which acts as the absorber material to generate electron–hole pairs by absorbing photons with energies larger than the bandgap. To supply power to an external electric circuit, the electrons and holes have to be separated and transported to their respective contacts, the electron and hole contact. These contacts are connected to the external circuit by

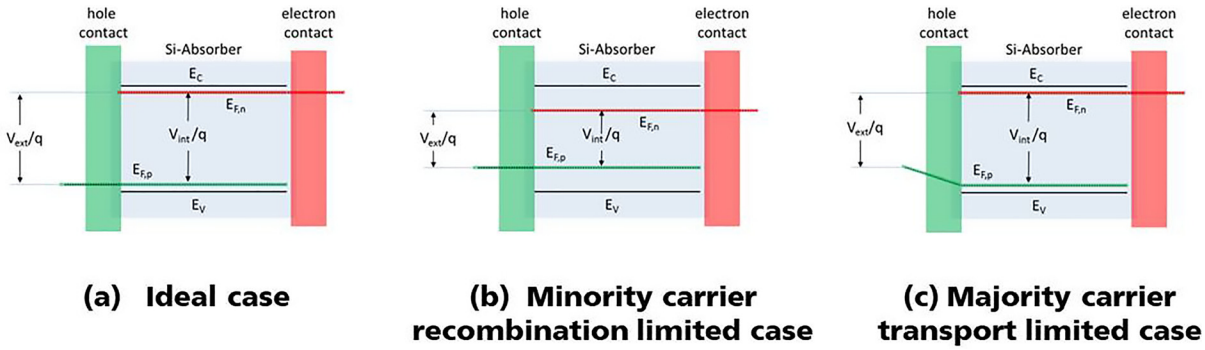

FIG. 2. Schematic silicon bad diagram with different electron and hole contact systems, leading to either an ideal solar cell [case (a)] or recombination or transport limited solar cells [case (b) and (c)], respectively.

electrical conductive electrodes. The definition of contacts in the following envelops not only the metal/semiconductor interface itself but includes any induced or diffused regions inside of the silicon wafer. Thus, the contacts in this definition are responsible for the extraction of electrons and holes out of the silicon absorber.

In Fig. 2, a schematic silicon band diagram with a silicon absorber and three different electron and hole contacts is shown. The minority carrier recombination limited case (b) represents the standard case of currently industrially realized solar cells. The direct contact of the metal to a semiconductor creates a highly recombinative interface with a quasi-continuous defect distribution in the semiconductor bandgap region. Therefore, this interface is an enormous sink for minority carriers and the separation of the quasi-Fermi-levels or the implied voltage V_{int} is strongly reduced. (Note that we have assumed silicon material with a very high lifetime or long diffusion length, respectively.) The present industry's way in Al-BSF and PERC cells to reduce this recombination rate at such a highly recombinant metal-semiconductor interface is to introduce a highly doped region as the before-mentioned Al-BSF that reduces the number of minority carriers at the interface and thus reduces the recombination rate. Figure 3 shows the simulated recombination current density J_0, which is a good measure of the recombination rate, as a function of semiconductor surface concentration.

For passivated interfaces (e.g., SiO_2), lower doped silicon lead to lower J_0 values, whereas the lowest J_0 values for metal-contacted surfaces can be achieved with highly doped surfaces. However, such a highly doped region leads to an increase in the unavoidable Auger recombination. Due to this conflict of objectives, the second approach to minimize recombination is to reduce the area of the strongly diffused and contacted area, as moving from full area Al-BSF to locally contacted and Al-alloyed PERC cells.

Although the share of the metallized surface in this cell is less than 1%, these surfaces still dominate the overall recombination of this type of solar cell device.[10] Furthermore, the shrinking of the metal contacts to local point contacts leads to an additional loss mechanism, since the transport path of the majority carriers is increased and a current overfilling occurs at the local contacts, which leads to an additional power loss.[11]

To further reduce these losses, an alternative contact scheme has to be used, which avoids direct contact between metal and the silicon wafer, without generating a barrier for majority carriers. Such contacts are called "passivating contacts."

If passivating contacts are realized perfectly, they are close to the ideal case [Fig. 2(a)] where the internal or implied voltage (V_{int}), which is defined by the separation of the quasi-Fermi levels ($E_{F,n} - E_{F,p}$) in the absorber, is only limited by the recombination losses of the silicon absorber itself and the external voltage (V_{ext}) measured at the metal electrodes corresponds to the internal voltage.

In the third case [Fig. 2(c)], the implied voltage of the cell is similar to the ideal case (a) but the external voltage is reduced ($V_{ext} < V_{int}$), which results from a voltage drop of the majority Fermi energy in the contact region. Such a gradient of the majority Fermi energy (in this case $E_{F,p}$) occurs, if a majority of carriers faces any kind of transport losses.

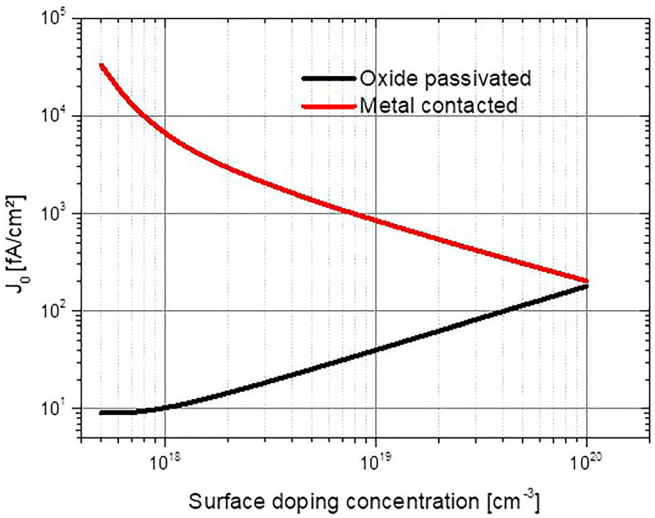

FIG. 3. Simulated recombination current density for a phosphorus doped surface either passivated with SiO_2 (surface recombination velocity, SRV, is a function of N_A after Ref. 12) or contacted with metal (SRV = 10^7 cm/s) as a function of the surface doping concentration. Low saturation current densities can be achieved with passivated lowly doped surfaces. The metallization of such lowly doped surfaces leads to very high J_0 values. J_0 can be decreased by increasing the surface doping concentration. However, values of at least one order of magnitude higher than the passivated areas are still present. The simulations were performed using the software EDNA.[13]

From this, the following three fundamental prerequisites of a passivating contact system can be deduced:

(1) The recombination in the vicinity of the contact has to be suppressed to allow for a high internal voltage (V_{int}).
(2) The majority Fermi energy in the contact region has to be constant at open-circuit conditions ($V_{ext,oc} = V_{int,oc}$).
(3) The majority carrier voltage drop at maximum power point has to be as small as possible, which means that a low resistivity for the majority carrier transport has to be guaranteed.

Requirement (2) and (3) can be realized by highly doped regions directly in contact with an appropriate metal layer, forming an Ohmic contact. However, this leads to a relevant recombination in the highly doped region by Auger recombination (see Fig. 3) and at the metal–semiconductor interfaces and thus contradicts requirement (1). To fulfill requirement (1), highly doped regions in the silicon absorber have to be avoided and the surface has to be passivated. That's why ideal contacts are named "passivating contacts."

An often used synonym of passivating contact is carrier-selective contact. In principal, the three requirements stated above can be combined into one statement proposed by Würfel *et al.*[14] A selective contact "is achieved by differences in the conductivities of electrons and holes in two distinct regions of the device, which, for one charge carrier, allows transport to one contact and blocks transport to the other contact." This difference in conductivity leads to a suppression of recombination of on carrier type [requirement (1)] and the loss-free extraction of the other carrier type [requirement (2) and (3)].

If requirement 2 is fulfilled, the standard one-diode equations can be used to describe the contact. In this case, the selectivity of the contact can be described quantitatively as the resistance ratio for carriers to be blocked and carriers to be collected.[15] Thus, the selectivity depends only on the ratio between the recombination current J_0 and the contact resistance ρ_c. A highly phosphorus-doped region under a metal contact, e.g., is in this definition a very good electron-selective contact as the ratio between J_0 and the contact resistance ρ_c is very small, due to the very low contact resistance. A passivating contact has not only a good selectivity (low ratio J_0/ρ_c) but also a very low recombination current.

In Secs. II B and II C, different technological approaches for passivating contacts will be presented.

B. Amoprhous Si heterojunction

The well-known example of a passivating contact is the silicon heterojunction (SHJ) formed between hydrogenated amorphous Si (a-Si:H) and the crystalline silicon (c-Si) absorber (Fig. 4), which enables the highest efficiencies for silicon wafer based photovoltaics.[16] To a large extent, the excellent performance and current achievements result from the fact that this contact scheme combines the best ingredients of two different photovoltaic technologies: (i) the Si wafer-based solar cell technology, which is clearly dominating the photovoltaic (PV) markets,[17] brings in high-quality absorbers and expertise for high-volume production such as wafer texturing and cleaning, metallization and module integration. (ii) The silicon thin film (SiTF) solar cell technology, for which efficiency limitations are often ascribed to the quality of the silicon thin film absorber,[18] provides expertise for high-volume thin film deposition and extensive knowledge regarding engineering of the transparent, and conductive metal oxide (TCO) and Si thin films stacks, which form the passivating contacts of the wafer based SHJ solar cells.

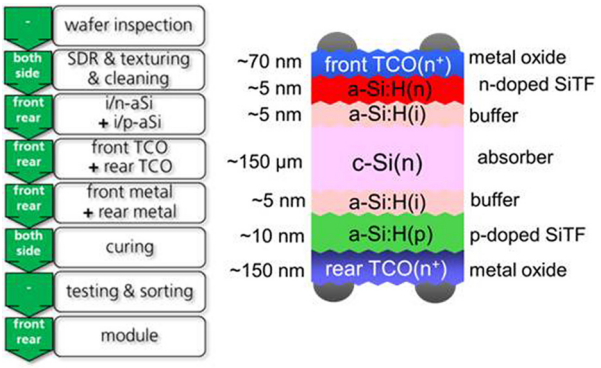

FIG. 4. Process steps (left) and illustration of the silicon heterojunction solar cell (right).

As shown by many institutes and companies and further pointed out below, the combination of high-quality c-Si absorbers and low-temperature deposited heterojunction allows to overcome the efficiency limitations of the well-established homojunction approaches[19] and hence to further push silicon solar cell efficiency to its theoretical limit. However, processing of such contacts calls for different strategies as compared to homojunctions with emphasis on the thin films and their interfaces. One major challenge is to balance the often conflicting optical and electronical properties of the only several nanometer thin doped and undoped silicon thin films and the anti-reflective, transparent, and conductive metal oxides (TCOs). The use of high-quality absorbers is essential since the SHJ cell process is limited to about 200 °C, hardly changing (deteriorating/improving) the electronic quality of the crystalline silicon absorber. The limited back-end temperature calls for adaptions for metallization and module integration compared to the well-established homojunction approaches. Furthermore, such large-area (~250 cm^2) contact-limited devices are highly sensitive to the absorber's surface and the opto-electronic contact properties, which need to be addressed for proper high-volume manufacturing.

In this chapter, the history, operation principles, important design parameters, and challenges of silicon heterojunction solar cells are briefly outlined. Some emphasis is put on the fill factor, which is one of the main challenges with respect to the basic understanding of the device physics and thus for effective engineering toward highly efficient and economic devices. The latter is highlighted by a few experiments performed by the authors. For further reading, we refer to, e.g., Refs. 20–23. In this review, only heterojunctions using intrinsic and doped amorphous silicon are discussed. Non-silicon based carrier-selective contacts are beyond the scope of this review, but a good review can be found elsewhere.[24]

1. History

The principle application of heterojunctions for electronic devices was proposed back in 1948 by Shockley[25] in order to overcome the limitations for homojunctions. In contrast to homojunction devices, where engineering of the material and junction properties is limited to the doping type and profile as well as the device geometry, heterojunction device engineering quickly proved to have unprecedented degrees of freedom. The heterojunction approach applied to solar cells is

somewhat inspired by the heterojunction transistor proposed by Shockley, which was discussed in detail by Kroemer,[26] who received the Nobel prize in 2000 for "developing semiconductor heterostructures used in high-speed and opto-electronics."

Pioneering work of the heterojunction formed between doped amorphous silicon and a crystalline silicon absorber (aSi/cSi SHJ) started back in 1974 by Fuhs *et al.*[27] SHJs using thin film absorbers such as alloyed aSi and partly crystalline Si (μcSi, polySi) have been presented back in 1983 by Hamakawa *et al.*[28] The latter and related work triggered commercialization of thin film silicon solar cells and in 1992, Tanaka *et al.* (Sanyo Corp., now Panasonic Corp.)[29] presented significant improvements for the SHJ using wafer based absorbers. This was realized by introducing an undoped and hence less defective a-Si layer in-between the doped a-Si and the c-Si absorber. It might be interesting to mention that early HIT (heterojunction with an intrinsic thin layer) cells from Sanyo were investigated using both monocrystalline and multicrystalline Si absorbers.[30] Early work also addressed the use of non-silicon based contact materials to form carrier-selective heterojunctions with wafer or thin film Si based absorbers. Among others, high/low work function contact materials (MoO_x,[31] TiO_x[28]) and, more recently, organic layers[32] and silicide's[33] have been mentioned. Some of those materials are currently re-explored.[24] Work in this field can be understood as a renaissance of the induced silicon junctions from the 1970s[9] (metal–insulator–semiconductor), taking advantage of novel or better studied materials partly adapted from the Schottky barrier-height engineering approaches[34] used in microelectronics, photo-electrodes, and from organic and thin film electronics.[10]

Taguchi *et al.*[35] motivated the SHJ approach by the following simple features of a HIT structure:

(1) Simple structure: a high efficiency can be obtained with no complicated structural techniques, such as partly heavy doping or a partial oxidation method.
(2) Simple low temperature process: due to the simple structure, the process is very simple and cost effective. In addition, the process temperature is so low (<200 °C) that degradation of the minority carrier lifetime for the substrate is negligible even for low-quality Si materials.
(3) Simultaneous realization of surface passivation and p–n junction: With the insertion of a very thin intrinsic a-Si layer at the a-Si/c-Si heterojunction, surface recombination is drastically suppressed. Therefore, during the junction fabrication process, good surface passivation on the c-Si surface is also realized.
(4) The BSF structure can be realized with the same process: the HIT structure is also suitable for fabricating the Back Surface Field (BSF) structure. The same process with a different impurity can be used to obtain the BSF structure and good surface passivation.
(5) Stability: the Staebler–Wronski effect, which is seen in a-Si based solar cells, is not seen in the HIT cell. This is probably due to the fact that the a-Si layers are very thin and contribute little to the power generation. Besides, the degradation of the carrier lifetime caused by the metastable defect related to the boron-oxygen complex does not apply to the HIT cell, which uses phosphorus doped Czochralski (Cz) Si.
(6) Improved high-temperature performance: one disadvantage of c-Si solar cells for practical use is their poor high-temperature performance compared with a-Si solar cells. The HIT cell, which has both a-Si and c-Si, shows an improved high-temperature performance.… The HIT cell has better temperature dependence than the conventional p-n diffused cell.… The HIT cell showed 8.8% higher output power under this condition.

The HIT concept sets the basis for the commercialization and the current achievements of SHJ cells and more players entered the market after expiration of Sanyo's patent in 2010. Until 2014, Panasonic could increase efficiency to 24.7% for both side contacted cells[36] and 25.6% using the interdigitated back contact (IBC) design.[37] Another company with strong background in TCOs and SiTFs (Kaneka Corp.) could further boost the efficiency of both side contacted cells to 25.1% (Ref. 38) in 2015 and IBC efficiency to the current world record of silicon solar cells of 26.7%.[16] Approaches to reduce the complexity of IBC cell processing are under investigation showing promising efficiencies up to 25%.[39] However, so far both side contacted design is the more viable option for production and several companies and institutes have reported efficiencies exceeding 23% for such devices with clear roadmaps for further improvements in performance and costs.[23]

2. Working principle

A band diagram showing the individual layers of the standard SHJ before and after contact formation is sketched in Fig. 5.

It can be seen that the c-Si absorber is sandwiched between three thin films on each side, two a-Si films, and one TCO. Put simply, the undoped a-Si enables low c-Si surface recombination and the doped a-Si forms the hole (electron) selective contact to the absorber and the TCO. The main function of the TCO is improved light coupling into the absorber and low resistive (lateral and vertical) transport from the doped a-Si to the local metal electrodes. The lateral hole and electron transport is governed by the sheet resistance of the TCO and absorber while actual hole and electron resistance in the absorber will be governed by the absorbers' excess hole and electron density (and their mobility) during operation (Fig. 6).

The function of the 5–10 nm thick nominal undoped a-Si is to provide chemical passivation of the absorber surface and to decouple c-Si surface recombination from the abundance of defects in the subsequent layers (first basic requirement for passivating contacts). Important requirements for chemical c-Si surface passivation are a properly cleaned c-Si surface,[41] an atomically sharp a-Si/c-Si interface,[42] and an i-a-Si featuring a low defect density and sufficiently high hydrogen content.[43] The high bandgap and low mobility of a-Si[44,45] make the a-Si electrically opaque,[46] which is essential to screen the doped a-Si (TCO and metal) defects from the c-Si surface. Hence, the i-a-Si buffer layer is the important ingredient that turns a non-passivating and carrier-selective contact into a passivating and carrier-selective contact.

About 10 nm thick p- and n-doped Si films are deposited on top of this buffer layer to control the hole and electron density in the contact region, respectively. This has two important implications. (i) It creates the shortage of one type of carrier, which besides chemical passivation is an effective means to minimize recombination of the absorber's excess holes and electrons at the i-a-Si/c-Si interface. This interplay between chemical and "field-effect" passivation defines the

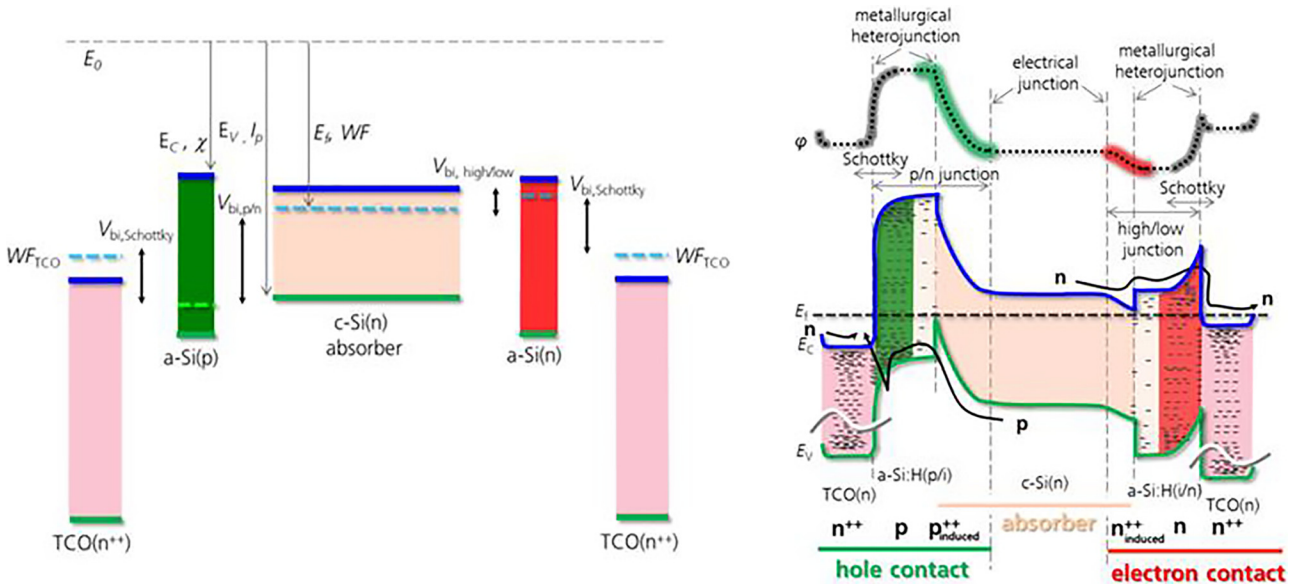

FIG. 5. Schematic band diagram of the silicon heterojunction solar cell before (left) and after (right) contact formation.

upper limit of the cell's V_{oc} and fill factor (FF). The latter is motivated in Fig. 6. It can be seen that shortage of either holes (3—accumulation) or electrons (2—inversion) is highly beneficial compared to the case when both carriers are present at the absorber's surface (1—depletion).[45,47] The latter case is dominated mainly by the chemical passivation, which in this experiment improved with i-a-Si thickness (different colors). (ii) The second function of the doped layers is to form the hole (electron) selective contact to the absorber and the TCO. This is done by creating a highly hole (electron) conductive contact region[48] to "guide" the photo-generated excess holes (electrons) in the absorber toward the electrode with minimal losses. This selective extraction of only one type of charge carrier ensures that the recombination-limited cell's V_{oc} and most of the *FF* values can be utilized by an external load[45] (second basic requirement for passivating contacts). For the i-aSi/absorber part of the contact, selective conductivity is mainly defined by the a-Si doping type and strength. As indicated in Fig. 5, sufficient n-type[20] or p-type[49] doping and potentially alloying[49] are used to decrease and increase the work function of the a-Si, respectively. The aim is to maximize the built-in potential ($V_{bi,aSi/cSi}$, Fig. 5). The latter represents the modification of the hole (electron) concentration and hence conductivity after contact formation in the i-aSi/absorber part of the contact. This requirement is similar as for related contact systems based on induced junctions[9] using different approaches and contact materials for "barrier-height/work function engineering." Basically, the doped a-Si causes a proper work function difference with respect to the c-Si and thus the formation of an

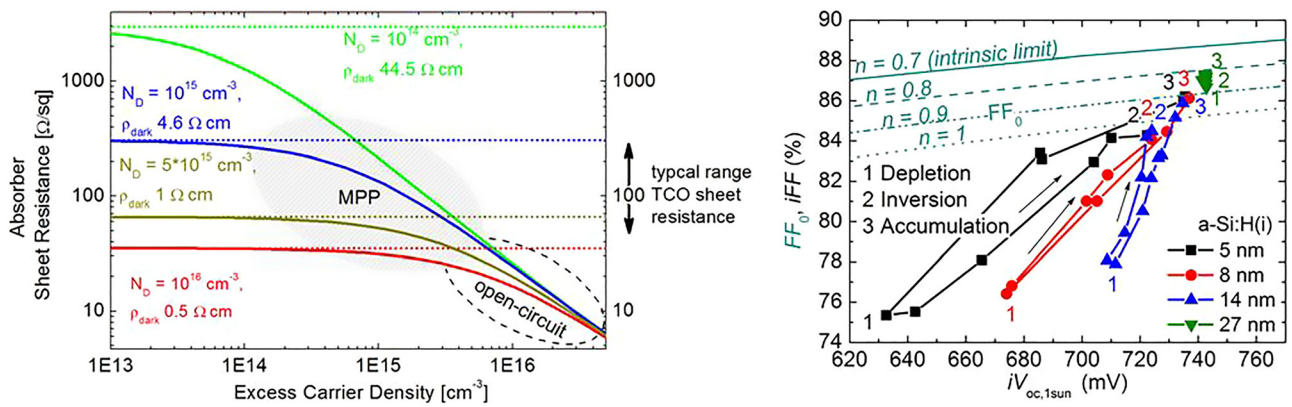

FIG. 6. Left: modeled sheet resistance (holes + electrons) of a 150 μm thick absorber as a function of its excess carrier density for four different doping densities. The highlighted areas give a rough indication for the relevant range during maximum power point (MPP) and open-circuit conditions. For high-injection conditions, the absorber sheet resistance drops significantly below its value in the dark approaching values of the TCO. Right: measured dependence of implied FF on implied iVoc. The calculated upper limit of the implied FF, the FF0 as a function of the used ideality factor,[40] is shown as well. The numbers along the measured points are indicating the corresponding c-Si surface conditions, i.e., depletion, inversion, and accumulation.

induced homojunction at the c-Si surface. This induced homojunction is the reason why properly designed heterojunctions can be well described by the (simple) homojunction theory for the typical range of operation.[50] It implies that the rest of the contact, the undoped and doped a-Si, the TCO/doped a-Si heterojunction, and the TCO/metal contact are designed in such a way that the overall contact characteristics are still dominated by the induced homojunction. The rest of the contact should provide only (low) Ohmic transport losses, which can be well described by a lumped series resistance. However, in the unoptimized case contacts might not obey the standard diode theory, which means that the "classical" electrical losses like recombination and Ohmic transport which are well quantified by saturation current density J_0 and the series resistance R_s are not sufficient to describe the dominating losses.[45] In such a case, engineering toward a sufficient selectivity and hence validity of the diode theory by improving the selective conductivity in the contact region is needed.[49,51]

Sufficient a-Si doping is not only needed to form the junction with the absorber but also with the TCO. Sufficient selective conductivity is needed at the TCO/doped a-Si heterojunction to "guide" the holes (electrons) from the induced c-Si junction toward the electrode. The requirements on the doped a-Si are clearly increased beyond what is needed to form the junction with the absorber by the fact that the work function of most TCOs is around mid-gap of a-Si. Higher a-Si doping and thickness are needed to account for the large work function mismatch at the anisotype n-TCO/p-a-Si and the isotype n-TCO/n-Si heterojunction. It results in parasitic Schottky-like induced junctions in which depletion regions are lowering the selective a-Si conductivity. Below certain conductivity, a voltage drop in the contact region occurs such that the contact fails to fully extract the implied voltage at the external electrodes. Losses of the SHJ often show signatures of such parasitic junctions, e.g., for too low a-Si doping or thickness mainly affecting the transport related *FF* losses.[52] For the case that the doped a-Si thickness is below its screening length,[53] the doped a-Si fails to properly screen the TCO work function from the i-aSi/c-Si junction, which results in a collapse of the built-in potential of the induced homojunction and hence also the $V_{oc.}$[49,54] For such conditions, the overall contact characteristic becomes dominated by the parasitic TCO/a-Si junction rather than the actual a-Si/c-Si junction. Such non-ideal contacts do not obey the classical diode theory as reflected in s-shaped or double-diode like *JV* curves and unusual temperature dependencies.

Approaches to mitigate the influence of the parasitic TCO/a-Si junction are based on a low "effective barrier height" as shown for the metal/a-Si junctions.[55] However, this might be an oversimplification for lowly doped TCOs, which do not show metal-like behavior and especially for the anisotype n-TCO/p-a-Si heterojunction where efficient transport also calls for efficient recombination of majority holes from the p-a-Si with a majority of electrons from the TCO.[56] Accordingly, besides high doping a certain amount of defects at and close to the TCO/aSi interface is assumed to have a positive influence on the transport since they provide an alternative transport path in this typically highly defective material system.[57] Another important function of defects is the significant reduction of the screening length and hence barrier width in the doped aSi.[58] However, the main approach is to minimize the widths of the barriers by sufficiently high doping on both sides of the junction, in the aSi and TCO. Reducing the height of the barrier by matching the TCO work function to that of the doped aSi has also been shown to be an effective means[34] as long as improved work function matching is not overcompensated by, e.g., less metal-like behavior of the TCO.[45,59] With respect to sufficient thin film Si doping,[49,58,60] partly crystalline materials[61] are assumed to be preferred over amorphous Si owing to its higher doping efficiency. This is especially true for p-aSi, which shows lower doping efficiency compared to n-aSi.[62] In general, optimizing the hole contact is found to be more challenging compared to electron contact owing to the lower doping efficiency of p-aSi, the more complex anisotype n-TCO/p-aSi heterojunction, and the higher majority carrier band offset at the aSi/cSi heterojunction.

To highlight the influence of the different layers of the SHJ on the selective hole and electron extraction from the absorber, transport

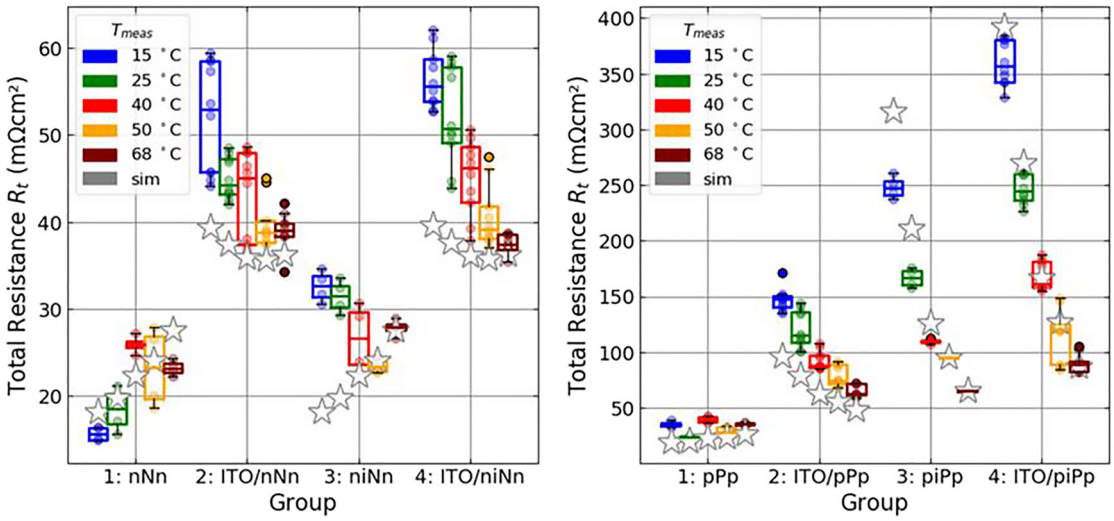

FIG. 7. Total resistance of test structures, which is dominated by the contact resistivity ρ_c of different electron (left) and hole contact (right) heterojunction stacks. Results are shown for different measurement temperatures. Results from numerical device simulations are shown by the gray stars.

losses quantified by the contact resistance are shown in Fig. 7.[63] The contact resistances measured at different temperatures for hole and electron selective SHJs with increasing complexity have been investigated. The metal/doped aSi/cSi structure (pPp, nNn) is presenting the simplest structure showing the lowest resistance. Adding the TCO electrode (TCO/pPp, TCO/nNn), which is needed in the solar cell for optics and lateral transport,[52] comes at the cost of additional vertical transport losses and changes the temperature dependence of contact resistance of the stack. A similar trend is overserved when i-aSi is added (piPp, niNn), which is needed at the cell level for cSi surface passivation. Basically, i-aSi enables higher V_{oc} and *pFF* at the cost of transport losses. The influence of the TCO and the i-layer adds up in the device relevant structure (TCO/piPp, TCO/niNn) and has a stronger influence for the hole contact. In principle, it can be seen that higher contact resistance comes along with a more negative temperature dependence. This indicates that these higher contact resistances are not of Ohmic nature but dominated by thermally activated transport and insufficient tunneling.

The efficiency of current SHJ devices is typically limited by J_{sc} (short circuit current) and FF. Strategies for improving the blue response are based on minimizing the "optical thickness" of the front aSi stacks by lowering the physical thickness[52] and reducing the absorption coefficients by alloying[64] or growing partly crystalline Si films.[65,66] However, J_{sc} gains have to be carefully balanced with less efficient surface passivation and (vertical) transport or even loss of selectivity.[52,64,67] Improvements in the IR response are governed by the conductivity-transparency trade-off of the TCOs which is less pronounced if high mobility TCOs can be used.[68] To benefit from more transparent TCOs, the less efficient lateral transport in the TCO[52] can be partly compensated by a smaller pitch of the fingers. However, the gains in the IR response have to be balanced with higher metal shading and potentially higher metal/TCO and TCO/aSi contact resistance.[69] A significant part of the lateral hole and electron transport can also be realized by the absorber, depending on the device design[70] and the actual absorber conductivity at MPP conditions (Fig. 6).

With respect to the latter, low device recombination (thus high excess carrier density) does not only help to increase the upper FF limit (Fig. 6)[38,47] but also increase the (lateral) absorber hole and electron conductivity.[45,64,65] Depending on the optimization route, this allows reducing the conductivity-transparency trade-off of the TCOs or the *FF* losses related to lateral transport.

3. Outlook

Despite the clear advantage in terms of efficiency, the marked share of SHJ technology is still small[17] and current efforts are clearly driven by proving industrial feasibility and competitiveness. SHJ based PV-systems hold the promise of low LCOE and higher energy yield[66] thanks to the better temperature coefficient, intrinsic bifaciality, and absence of severe degradation over time.[67] Regarding the cSi absorber, negligible defects in the bulk and at the surface are essential to fully benefit from the excellent surface passivation of the SHJ. This means that very high-quality cSi wafers, efficient approaches for defect-free wafer handling, and thin film deposition in a high-volume industrial environment are needed. However, low-cost and high-volume production is still an open point, which is addressed along the entire value chain. Although a lower amount of process steps is involved compared to other high efficiency concepts, capital expenditure (CAPEX) and operational expenses (OPEX) reduction is essential for the widespread adoption of this technology.

Proper large-area deposition of nanometer thin SiTF on both sides of the wafer with high cycle time, the avoidance of cross contamination between deposition of the thin films, etc., is currently the main driver for CAPEX. Significant improvements are expected from the growing industrial momentum by the entry of (equipment) manufacturers with experience in high-volume SiTF PECVD deposition (SiTF solar cells, flat-panel displays).

OPEX is clearly dominated by the electrodes (low-temperature Ag paste and indium-based TCOs) and a holistic approach is needed to balance cost reduction and potential performance loss. Strategies for indium reduction will be become more important for significant increase in production volume to account for its limited supply and price fluctuations.[68] The most obvious solution would be the use of indium-free TCOs, but their lower mobility results in a more pronounced conductivity-transparency trade-off with implication on device performance. Good long time stability and easy production are other factors why indium tin oxide (ITO) is the TCO of choice, so far. Thinner indium based TCOs (with better performance) or the use of the IBC cell design, which uses a (indium-free) TCO only at the rear, would be other approaches.

Ag consumption for the low-temperature screen printing has already been reduced by paste improvements enabling higher finger conductivity and higher aspect ratios. This work also led to faster printability and approaches to increase throughput for curing are under investigation.[69] Alternative printing technologies, like Inkjet[70,71] or FlexTrail printing,[72] show further potential to minimize Ag consumption and finger shading. Besides the use of non-Ag based printing approaches,[73,74] an efficient process integration of Cu plating[75–78] would allow for a nearly Ag-free and highly conductive metallization of SHJ cells.

Low-temperature processing of SHJ cells influences the interconnection process for module integration as well. Meyer Burger Technology AG promotes the SmartWire Connection Technology (SWCT).[79,80] Here, Cu wires coated with a low-temperature solder are embedded into a polymer foil, contacting the fingers of the SHJ cell during the lamination process. This approach shifts the carrier transport and hence the Ohmic transport losses from the cell metallization into the module, which strongly reduces the requirements on finger resistivity. With respect to busbar-based interconnection, in the past few years, a major difficulty for the interconnection has been the low paste adhesion of the busbars to the SHJ wafer surface after soldering.[81] Progress in screen-printing paste chemistries now allows an interconnection with ribbons. To omit the expensive Ag busbars, an option is the interconnection with electrically conductive adhesives (ECAs).[82] The electrical connection is realized by application of the pasty ECA, positioning of the ribbon and thermal curing at 120–200 °C for < 30 s within the stringer.[83] Current interconnection approaches also focus on soldering SHJ cells with conventional stringers.[84] Short soldering times (<3 s) allow process temperatures above 200 °C during infrared soldering with Pb-containing solder alloys.

C. Polycrystalline Si-based contacts

An alternative approach to SHJ is poly-Si based passivating contacts. They are considered as a key-enabling technology for

high-efficiency solar cells as this technology allows very low recombination current (J_0) values in the vicinity of 1 fA/cm^2 and reasonably low contact resistivity (ρ_c) values on the order of 1 mΩ cm^2. Hence, record efficiencies of 25.8% for both side contacted cells[85] and 26.1% for single side contacted cells[86] have been demonstrated. The principle technology was introduced into solar cells in the early 1980s.[87–89] 2013 Feldmann *et al.*[90] have introduced TOPCon (tunnel oxide passivating contact) in a both-side contacted cell and revived this technology. The importance of this technology is expressed in >100 papers published in the years 2014–2018 as well as two recently published review papers.[91,92] Since these two review papers already provide a very good overview of the historic development, the working principle—with special emphasis on the charge carrier transport—and relevant fabrication processes, this work will only briefly touch the aforementioned topics and will address important issues for industrialization such as metallization and integration into industrial-viable and lean process sequences in more detail.

1. Working principle

TOPCon describes a stack of a 1–3 nm thin interfacial oxide layer and a heavily-doped poly-Si layer. It is realized in four general process steps: (i) growth of interfacial oxide (HNO_3,[90,93] O_3, or UV/O_3,[94,95] thermally,[96,97] plasma oxidation[98]), (ii) deposition of an a-Si/poly-Si layer by, e.g., low-pressure chemical vapor deposition (LPCVD),[96,97,99–101] PECVD,[90,93,95,102–105] atmospheric pressure chemical vapor deposition (APCVD),[106] sputtering,[107] evaporation,[108] or liquid silicon,[109] (iii) a high-temperature annealing in an inert atmosphere at temperatures in the range of 700 °C–1050 °C, and (iv) hydrogenation by preferably atomic hydrogen. As pointed out by Schmidt *et al.*[92] various processes and combinations thereof have been utilized so far and resulted in a contact scheme characterized by comparable electrical properties.

The interfacial oxide is a vital part of TOPCon as it effectively passivates dangling bonds at the c-Si surface and thereby reduces the interface trapped charge density (D_{it}). As shown by Steinkemper *et al.*, a poly-Si contact requires a thin interfacial oxide [even in the unlikely case that a very low surface recombination velocity at the interface (S_{int} ~1 cm/s) would be possible without an oxide] as it poses a tunnel barrier to minority charge carriers and thus prevents minority charge carrier recombination at the metal contact.[110] This has been shown experimentally in Refs. 87 and 90. The poly-Si layer is likewise important. It typically is a heavily doped poly-Si layer but can be alloyed with carbon or oxygen, which alters its material properties (i.e., widening of the bandgap). Its work function determines its selectiveness to electrons and holes by inducing a strong band bending in the near-surface region of the c-Si. Further on it is providing sufficient conductivity in order to maintain the quasi-Fermi level splitting at the external contacts (i.e., $V_{ext,oc} = V_{int,oc}$). The minority charge carrier density in the near-surface region can also be reduced by a doped region, which can be formed during the high-temperature anneal as dopants diffuse from the poly-Si layer through the oxide into the c-Si. On the other hand, its large doping level enhances Auger recombination and increases the recombination velocity at the c-Si/SiO_x interface. The latter effect has been identified as the main source of recombination.[111,112] Hence, it is understood that dopant diffusion into the c-Si has to be kept to a minimum. Fortunately, the oxide layer, especially in the case of phosphorus, can be a very effective diffusion barrier. The high-temperature annealing not only triggers dopant diffusion but promotes crystallization of the Si layer and presumably changes the oxide properties in two ways: (i) formation of pinholes in the oxide and (ii) structural reorganization of the atomic bonds at the Si/SiO_x interface. It has been shown that pinhole formation not necessarily degrades the surface passivation but can be exploited to significantly reduce the contact resistivity of TOPCon structures featuring thicker oxides where tunneling is less efficient. According to Peibst *et al.*, a pinhole density of about 10^8 to 10^9 cm^{-2} allows both very low J_0 and ρ_c values.[113,114] Glunz and Feldmann pointed out that the dominant charge carrier transport mechanism (i.e., tunneling or pinhole-mediated transport) depends strongly on the sample preparation and therefore cannot be generalized.[91] The majority carrier transport for optimal annealed samples is a superposition of tunneling and pinhole transport, where the relative share of current paths depends on the oxide. The second effect is motivated from studies on thermally grown gate oxides but this hypothesis needs further research. Finally, the surface passivation quality is improved by hydrogenation, whereby atomic hydrogen presumably passivates electrically active defects at the c-Si/SiO_x interface (interface traps)[115] and within the poly-Si layer.[116] Hydrogen can effectively be supplied by hydrogen plasma or by H-containing dielectrics (e.g., SiN_x[95,97,117] and Al_2O_3[115]) and even TCOs,[118] while a forming gas annealing (molecular hydrogen) does not lead to substantial improvements in surface passivation.[95,119] Recently, it has been demonstrated that an annealing atmosphere containing water vapor can also effectively passivate electrically active defects.[120] Moreover, Ingenito *et al.* demonstrated that high-temperature annealing and the hydrogenation can be combined into a single firing step.[121]

As shown by Schmidt *et al.*,[92] many research groups have reported very low J_0 values, especially for n-type TOPCon, although using different fabrication routes and methods. Although the number of papers reporting J_0 values for p-TOPCon below 5 fA/cm^2 is increasing, there is still a remarkably large performance gap (in terms of J_0) between n-type and p-type TOPCon on textured surfaces: while J_0 values range from 2 to 8 fA/cm^2 for n-TOPCon, J_0 values for p-TOPCon ranging from 8 fA/cm^2 (Ref. 122) to 50 fA/cm^2 (Ref. 123) have been reported. This can partly be explained by an increase in J_0 on (111)-oriented surfaces as observed by Larionova *et al.*[123] Moreover, the growth rate of SiO_2 depends on the crystal orientation and in the case of oxides thinner than 3 nm is reduced on (111) than on (100)-oriented surfaces. Moreover, the authors observed non-homogeneous oxide growth on the pyramids' facets which they attributed to the presence of a nanoscale roughness on the (111)-oriented planes. Hence, inhomogeneously grown oxide layers combined with a higher interface trapped charge density seem to degrade the performance of p-TOPCon on textured surfaces. However, it has been shown that different combinations of AlO_x and SiN_x stacks can reduce J_0 significantly compared to a single SiN_x layer.[122]

2. Integration into industrial solar cell concepts

Since TOPCon provides excellent surface passivation, tolerates high-temperature processes, and apparently is a very robust process, it is an appealing choice for high-efficiency solar cells. TOPCon has been successfully integrated into three general solar cell architectures:

(i) TOPCon cell featuring a homojunction emitter/front surface field (FSF) at the front and a passivating rear contact;
(ii) IBC solar cell featuring both polarities of the passivating contact at the rear;
(iii) double-side contacted solar cell featuring TOPCon top/rear contacts (comparable to the heterojunction cell).

The record efficiencies of each of these three devices are currently 25.8%,[85] 26.1%,[86] and 22.6%.[124] As these record cells have been realized using laboratory processes such as photolithography and evaporation of metal, there were and still are a few challenges and innovations needed in order to realize an industrial viable solar cell process sequence. This will be addressed in the following.

a. Deposition technology. Currently, different deposition technologies are being developed and tested. Low-pressure chemical vapor deposition (LPCVD) is a start-of-the-art technology in microelectronics for deposition of amorphous and poly-Si and has been implemented into pilot production lines of leading solar cell manufacturers. It is a mature technology and has been adapted to the needs of the PV industry; still it has some inherent drawbacks such as a low deposition rate (which depends strongly on the deposition temperature) and the unavoidable double-sided deposition. Alternative single-sided deposition technologies such as PECVD or sputtering have been investigated. While one drawback of PECVD films, blistering due to too large hydrogen concentrations, can be controlled by increasing the deposition temperature or alloying with carbon, there are many more factors (e.g., throughput, uptime, and run-to-run reproducibility), which decisively influence the success or failure of one technology.

b. Metallization. In laboratory, TOPCon cells are typically metallized by evaporation of Ag or Al. However, evaporation is not yet considered a cost-effective metallization technology and there are more economically attractive solutions. The most promising metallization scheme is screen-printing and fast-firing. In view of the third cell concept, transparent conductive oxide (TCO)/metal stacks have been considered as well. First works for electrochemical solutions (e.g., plating) are under investigation.[125]

Stodolny *et al.* realized the first industrial prototype of a TOPCon cell whereby contact formation to TOPCon is realized by silver screen-printing and fast-firing.[97] Contact formation with screen-printed pastes has been very challenging in the beginning as the pastes, which were by then optimized for contacting phosphorus-doped emitter, partly consumed the poly-Si, and thereby locally degraded the passivation of the contact scheme.[126,127] Since then, dedicated pastes have been developed and tested for this application. Thereby, a significant reduction in $J_{0,met}$ by about a factor of 10 could be achieved [e.g., 200 nm poly-Si: 386 fA/cm^2 (Ref. 126) to ∼35 fA/cm^2 (Ref. 128)]. Despite these encouraging results, $J_{0,met}$ values obtained on poly-Si layers thinner than 100 nm are rather high and lead to substantial V_{oc} losses.

The TCO as a contact material for TOPCon is of importance for both-side contacted solar cells featuring very thin poly-Si layers as it serves as an anti-reflection coating and provides sufficient lateral conductivity for charge carrier collection at the metal fingers. TCOs are typically deposited by a sputter process which is known to degrade surface passivation. For TOPCon, the following observations have been made: (i) samples featuring a textured surface are more sensitive to sputter damage than those featuring a planar surface (e.g., compare V_{oc} values on planar and textured cells in Ref. 124) and (ii) thicker poly-Si layers mitigate the adverse impact of sputter damage.[118,124] The poly-Si layer shields the critical c-Si/SiO_x interface from UV radiation, and penetration depth in poly-Si is less than 10 nm. Still, it cannot be distinguished between particle bombardment and soft x-rays (penetration depth ≫10 nm) as the root cause of sputter-induced damage.[118] In contrast to heterojunction technology (HJT), it has been found that sputter damage cannot be cured at low temperatures of about 200 °C but requires higher curing temperatures of about 350 °C. These, in turn, impede efficient charge carrier transport across the TOPCon/TCO interface.[118,129,130] Using transmission electron microscopy (TEM), energy-dispersive X-ray spectroscopy and electron energy loss spectroscopy (EELS) spectra, Wietler *et al.* identified a 2–3 nm thin silicon oxide like layer at the interface between poly-Si and aluminum-doped zinc oxide (AZO) after annealing at 400 °C in air.[129] This transport problem can be mitigated by vacuum annealing, which can restore the surface passivation without degrading the contact resistivity.[118] Furthermore, high annealing temperatures lead to microstructural changes of the TCO, which adversely affect the optoelectronic properties of ITO but improve those of ICeO[118] or AZO.[129]

c. Integration into solar cell structures. Table I provides an overview of the efficiencies achieved so far using one of the above-mentioned cell structures. From this list, one can conclude that the TOPCon cell concept currently seems to be the most appealing choice for industrialization. One very compelling argument in favor of this cell concept is the possibility to upgrade existing (outdated) production lines by implementing only a few new tools and retrofitting old equipment. This was impressively shown by Chen *et al.*[131]

The TOPCon cell features a dielectrically passivating front homojunction and a passivating rear contact. The lab variant utilizes evaporated Ag which makes a low-resistive contact to TOPCon and serves as an excellent mirror for IR light.[90] Due to full-area metallization, the cell performance is nearly unaffected by changes in wafer resistivity and allows high FF even on a 100 Ω cm material.[141] The industrial version (see Fig. 8), however, features a screen-printed metal grid at the front and rear and, therefore, is inherently bifacial but also demands low-resistive wafers (which are not as stringent as those of PERC cells).

Another aspect which is different from the lab cells is the thickness of the poly-Si layer. As outlined above, heavily doped poly-Si layers thicker than 100 nm are required for reducing metallization-induced recombination losses. However, this affects the performance of the solar cell twofold. First, these heavily doped layers introduce significant free carrier absorption losses. For instance, a J_{sc} loss of about 0.3 mA/cm^2 and 0.5 mA/cm^2 was determined from quantum efficiency measurements of TOPCon solar cells featuring a ∼140 nm poly-Si layer with an average poly-Si doping level of 1.3×10^{20} cm^{-3} and 1.9×10^{20} cm^{-3}, respectively.[142] Second, bifaciality of these cells is reduced compared to an n-PERT cell as the blue response of the rear-illuminated cell is reduced by parasitic absorption in the thick poly-Si layer. For instance, Stodolny *et al.* reported a bifaciality of ∼88% (Ref. 122) while Trina's 23% TOPCon cells have a bifaciality of ∼80%. While reducing the poly-Si doping level mitigates free-carrier absorption losses, it only marginally improves rear efficiency and presumably leads to higher contact resistivities. It has been reported that incorporation of oxygen into the poly-Si layer can reduce free carrier

TABLE I. Comprehensive list of solar cells featuring TOPCon.

Company/Institute	Area (cm^2)	TOPCon (depo method)	Metal-lization	η (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
Both-side contacted TOPCon cells							
ISE[13,88]	4	n-SiC_x (PECVD)	PVD Ag	25.8	724	42.9	83.1
ISE (mc-Si)[16,132]	4	n-SiC_x PECVD	PVD Ag	22.3	674	41.1	80.5
ISE	100	n-SiC_x PECVD	PVD Ag	23.4	697	41.4	81.1
ANU[133]	4	n-poly PECVD + $POCl_3$ diff.	PVD Ag	24.7	705	42.4	82.6
EPFL[121]	4	p-SiC_x PECVD	PVD ITO/Ag	21.9	698	39.4	79.5
TU Delft	7.84	p-poly LPCVD + B implant.	PVD Ag	20.8	656	40.7	75.2
Trina Solar[134]	244	LPCVD	n/a	24.6			
Jinko Solar[135]	244	LPCVD	n/a	24.2	724	40.7	82.4
Trina Solar[131]	244	LPCVD	SP FT Ag	23.6	717	40.2	82.0
MeyerBurger[a]		PECVD	SP FT Ag	23.3	696	41.3	81
Jolywood[a]	239	LPCVD	SP FT Ag	23.06	694	40.2	82.1
GCI[a]			SP FT Ag	23.0	698	40.3	81.6
SERIS[136]		PECVD	SP FT Ag	22.8	696	40.5	80.9
ECN[97]	239	n-poly LPCVD	SP FT Ag	21.5	676	39.7	80.4
GIT[93]	239	n-poly PECVD	PVD Ag	21.2	683	39.7	78.1
IBC solar cells with poly-Si contacts							
ISFH[86]	4	Poly-Si LPCVD + implantation	PVD Al	26.1	727	42.6	84.3
ISE[137]	4	Poly-Si LPCVD + implantation	PVD Al	23.7	720	41.3	79.6
SunPower[138]	153	n/a	n/a	25.2	737	41.3	82.7
Trina Solar	239	n-poly LPCVD	SP Ag	25.0	716	42.3	82.8
TOPCon top/rear cells							
EPFL[124]	4	SiC_x PECVD	PVD ITO SP Ag	22.6	720	38.8	81.0
TetraSun[139]	239	n/a	Plating	22.0	702	38.8	80.9
ISFH[140]	244	Poly-Si LPCVD +implantation	PVD ITO SP Ag	22.3	714	38.5	81.1

[a]Presentations at PV-CellTech 2019.

absorption (FCA) losses[143] but it is still to be shown if this is an effect of enhanced bandgap or reduced doping level. Still factors such as bifaciality, operational expenses (OPEX), and capital expenditure (CAPEX) which drive levelized cost of electricity (LCOE) will inevitably trigger a further reduction in poly-Si thickness.

Table I shows that a few players like MeyerBurger, Jolywood, Trina Solar, and SERIS demonstrated efficiencies of about 23%. V_{oc} values close to 700 mV were achieved but by means of a simple loss analysis minority charge carrier recombination at the front has been identified as the main loss mechanism.

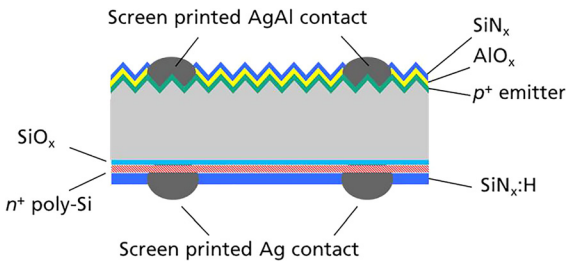

FIG. 8. Sketch of an n-type TOPCon cell with a dielectrically passivated front homojunction and a passivating rear contact, metallized with screen printed silver fingers.

The cell concept featuring top/rear poly-Si contacts holds the promise of sharing the same advantages with the HJT cell concept (i.e., higher V_{oc}) as well being able to leverage on the knowledge generated when producing HJT cells. Furthermore, TOPCon allows a higher back-end temperature, which opens up new routes for optimizing TCO and low temperature pastes. For instance, it was reported that the line resistance of a conventional low-temperature Ag paste could be reduced from 6.5–9.4 $\mu\Omega$ cm (200 °C) down to 2.4–3.5 $\mu\Omega$ cm (350 °C) while maintaining good contact resistivity values of 1.0–2.5 mΩ cm^2.[144] However, these potential benefits have only been demonstrated on test structures and are yet to be shown at the cell level. Another drawback is associated with substantial parasitic absorption losses invoked by TOPCon at the front. While poly-Si layers result in J_{sc} losses of ~0.5 mA/cm^2 per 10 nm film thickness,[4,145] J_{sc} losses in Si-rich SiC_x layers have been reported to be ~1.2 mA/cm^2 per 10 nm film thickness.[124] As outlined above, sputter damage further complicates things as mitigation strategies like thicker poly-Si layers or alloying with carbon trade V_{oc} gains against J_{sc} losses. Hence, an efficiency of 22.6% (Ref. 124) on a small area and 22.3% (Ref. 140) on a large area has been achieved so far. It is noteworthy that TetraSun was the first to industrialize such a cell concept.[139] In contrast to the approaches above, TCO layers were omitted. Instead, TOPCon was covered by SiN_x and contact was made by an elaborate PVD seed and plate process sequence.

Finally, the IBC cell concept is in terms of efficiency the ultimate cell concept. The IBC cell was pioneered by SunPower, which introduced passivating contacts in their third generation of commercial cells.[146] In an IBC cell, the contacts for both polarities are placed at the rear and, thereby, optical shading losses as well as parasitic absorption losses in the poly-Si layer (except for infrared absorption losses due to FCA) are avoided. The latter aspect enables high V_{oc} values without sacrificing J_{sc}. Moreover, the structure permits the use of thick and broad metal grid lines thereby virtually eliminating resistive losses. This is underlined by the 26.1% p-type record cell published by Haase *et al.*[86]

An important aspect of IBC cells featuring poly-Si contacts is the transition region between n-type and p-type contact. SunPower showed that touching of p- and n-type poly-Si regions leads to appreciable recombination losses but can be avoided by physically separating these regions.[147] Most commonly these regions are separated by a trench, which is etched into the poly-Si layer. Alternatively, p- and n-regions can be separated by undoped poly-Si. Reichel *et al.*; however, a strong degradation was observed in pseudo FF and consequently FF due to strong recombination in the space charge region.[137] Hollemann *et al.* assessed the influence of a poor passivating intrinsic poly-Si region by numerical simulation.[148] Nevertheless, ISFH's record cell features an intrinsic poly-Si region, which is partially doped from the adjacent doped regions during the high-temperature annealing.

The downside of IBC cells is the patterning of the rear electrodes, which renders this technology not cost-effective. There are different approaches to simplify the process sequence under investigation: (i) printing of local poly-Si layers (liquid silicon) or (ii) use and expansion of PERC technology by LPCVD for the n-type rear contact.[149]

3. Outlook

TOPCon is a promising contender for next generation high-efficiency solar cells as very promising results have been obtained by universities and research institutes and also by companies. To date, the industry seems to focus on the industrialization of the TOPCon cell and the joint work of paste suppliers and cell manufacturers has accelerated the development of the metallization process, which is one critical aspect. Compared to PERC, silver consumption is almost doubled, more expensive n-type wafers are employed, and the process sequence encompasses 1–2 additional processes. The next years will show if TOPCon can be implemented cost effectively while still keeping an efficiency gap of ∼1% to PERC.

From the scientific point of view, more research is required and encouraged to better understand the inferior passivation properties of p-TOPCon, especially on textured surfaces. This goes together with the development of advanced hydrogenation schemes passivating surface states more effectively. Another aspect is the poly-Si layer. Specifically, for top/rear contact cells knowledge of the minimum poly-Si thickness capable of maintaining the quasi-Fermi level splitting is important. In this respect, the positive influence of bandgap widening by alloying with carbon or oxygen on V_{oc} and apparently resilience to sputtering requires more work. Finally, the role of the high-temperature annealing which presumably leads to a rearrangement of atoms at the Si/SiO_x interface is an on-going research topic.

III. SILICON BASED TANDEM SOLAR CELLS

A. Introduction to tandem solar cells and how to interconnect them

The efficiency of silicon solar cells is fundamentally limited by spectral losses. Photons with energies below the bandgap cannot generate free charge carriers, which accounts for about 20% of the incident energy being lost. Additional 35% are lost; because for higher energy photons, the energy in excess of the bandgap is transformed to heat. These thermalization losses can be substantially reduced by adding one or more solar cells with a higher bandgap on top of the silicon, thus pushing the limiting efficiency to 42% for a tandem device with two p/n junctions.[150]

We can differentiate several ways the solar cells are combined into one device (see Fig. 9). In the so-called four-terminal

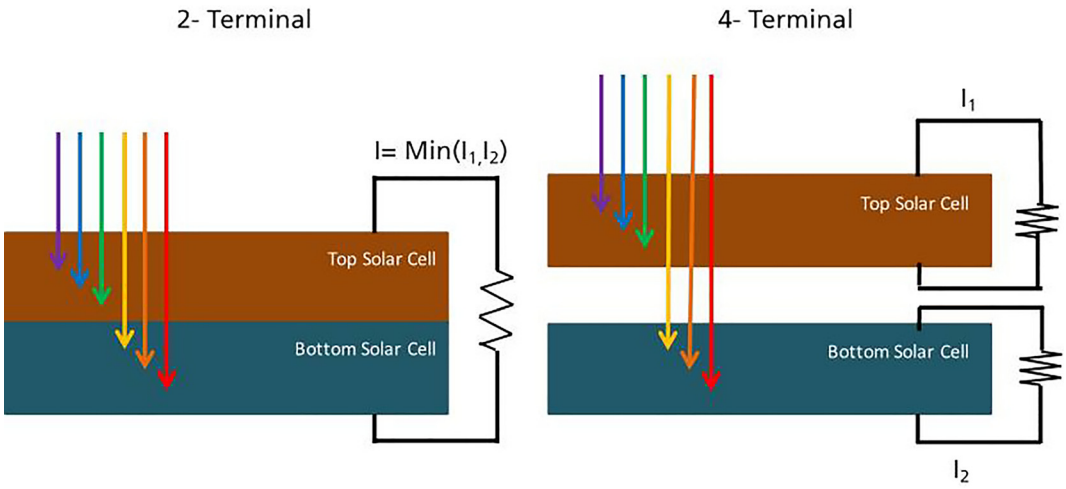

FIG. 9. The two main configurations for the realization of tandem solar cells. In the two-terminal configuration (left), the solar cells are connected in series. This creates the need for current matching, but the overall module and system architecture can remain like for single-junction devices. In the four-terminal configuration (right), the solar cells are operated individually. There is no need for current matching, which leads to a higher theoretical efficiency potential. Practically, however, module and system complexity increases and additional optical losses occur.

configuration, each solar cell is contacted individually. There is only a mechanical connection between the solar cells, which ideally also provides optical coupling to avoid unnecessary reflection losses. The electrical operation of each solar cell remains independent. In contrast, in the two-terminal configuration the two (or more) solar cells are connected in series. This means that the same current is flowing through all solar cells and thus, the currents of the sub-cells should be closely matched for an efficient operation. This leads to theoretically slightly lower efficiency limits in comparison to the four-terminal case. However, module and system integration is less complex in the two-terminal case and several causes for optical losses, such as highly conductive layers for lateral current transport and the need for an insulating interconnection layer, are avoided.[151] As another option, three-terminal configurations were suggested.[152] The general idea is that excess current that would be lost in the two-terminal configuration could be extracted by a third electrode. Due to the conceptual complexity both at the solar cell level and also for later module and system integration, three-terminal devices are far less common.

Currently, mainly two material classes are investigated for the top cell of silicon-based tandem solar cells: III–V semiconductors and perovskites. The current status for these two approaches will be discussed in the following.

B. III/V on silicon

III–V semiconductors are attractive as top solar cells, because of their extremely high efficiency potential, documented in record efficiencies as high as 46% for a purely III–V semiconductor four junction device.[153] To combine the III–V top solar cell with the silicon bottom solar cell, there are different technological options: mechanical stacking with some kind of adhesive can be realized without and with electrical interconnection, the III–V top cell can be wafer bonded onto the silicon, or the III–V solar cell is directly grown on top of the silicon.

The highest efficiency of 35.9% for a silicon-based tandem device was achieved by mechanical stacking.[154] First, a dual junction GaAs/GaInP solar cell was realized on a GaAs wafer and then transferred to a glass substrate. This substrate was then connected with an adhesive to an a-Si/c-Si heterojunction (SHJ) solar cell. For a successful transfer to industrial production of this concept, several severe challenges need to be overcome, such as the reuse of the III–V wafers or the use of cheap substrates in combination with a cheap growth of the top solar cell layers.[154]

Using an array of Pd nanoparticles produced by a self-assembled polymer template as an adhesive and conductive interconnection layer, Mizuno *et al.* realized a mechanically stacked, but electrically interconnected III–V silicon device.[155] They also used a GaAs/GaInP top solar cell. However, the bottom silicon solar cell was only a classical Al back surface field (BSF)-type c-Si cell, with a diffused emitter but no front surface passivation to allow for the electrical interconnection. The overall efficiency was thus limited to only 25.1%.

An adhesive layer between the solar cells and the associated optical losses can be completely avoided by using wafer bonding. For such bonding, the very clean surfaces of the silicon and the III–V solar cell are activated by ion bombardment and then pressed together at elevated temperature. Like this, mechanically strong interconnection with high electrical conductivity can be achieved.[156] In Ref. 157, wafer bonding was used to achieve 33.3% record efficient two-terminal silicon based tandem devices. The top cell was again a GaAs/GaInP dual junction cell. The bottom solar featured TOPCon passivating selective contacts for high voltages and fill factors and a nanostructured rear side diffraction grating for high current.

The costs for the additional III–V substrate and the need of additional interconnection steps could be avoided by direct growth of the III–V solar cells on top of the silicon. The main challenge of this approach is the nucleation of polar III–V on non-polar silicon followed by a lattice-grading of 4% to allow the growth of an unstrained GaAs and GaInP absorber with high crystal quality. The formation of defects like anti-phase domains, twins, threading-dislocations, or stacking faults limits the performance of these devices today. Other issues like the degradation of the minority carrier lifetime in silicon due to the overgrowth by MOVPE or MBE have been studied intensively[158,159] and can be avoided today.[160] However, there has been rapid progress lately and efficiencies as high as 24.3% have been reported.[161,162]

In conclusion, the main challenge for the III–V on silicon tandem technology will not be in achieving substantial efficiency increases, but realizing those at attractive costs.

C. Perovskite on silicon

1. History

Since the first application in photovoltaics in the year 2019, perovskite solar cells have seen an unparalleled fast rise in research activity, attempts for industrialization, and efficiencies. For specific reviews, see, e.g., Refs. 163 and 164. In the context of tandem devices, high single-junction efficiencies of up to 24.2% (Ref. 165) (cell area 0.0955 cm^2) promise that overall efficiency can be increased by the addition of a perovskite top solar cell to a silicon bottom cell. The ABX_3 crystal structure of the perovskite allows for a high degree of compositional variation, enabling the precise bandgap adjustment for the needs in a tandem device. Furthermore, both solution-based printing techniques as well as evaporation approaches promise low manufacturing costs. All this makes perovskite solar cells ideal as top cells in tandem configurations. In the following, some major steps in their development are reviewed.

The first perovskite silicon tandem solar cell was realized in a four-terminal configuration by Löper *et al.* in 2015.[166] For the top solar cell, they used an at that time established *nip* or sometimes also called regular mesoporous configuration. Please note that *nip* designated the sequence of deposition of the electron (ETL) and hole (HTL) transport layers. In a *nip* device, the ETL layer is deposited first. The solar cell was realized by depositing a compact and a mesoporous TiO_2 layer on top of an FTO (Fluor doped tin oxide) coated glass substrate. These layers served as an electron selective layer (ETL). The absorber was $CH_3NH_3PbI_3$ with a bandgap of 1.57 eV deposited via spin-coating. The hole transport layer (HTL) was 2,20,7,70-tetrakis(N,N-di-p-methoxyphenylamine)-9,90-spirobifluorene (Spiro-OMeTAD). For opaque solar cells, a gold contact would have been evaporated on top of the HTL. However, for the realization of a tandem solar cell, semi-transparency is necessary. Therefore, an ITO layer was sputtered as contact. As this sputtering could cause severe damage in the Spiro-OMeTAD layer, an additional MoO_x served as a buffer between Spiro-OMeTAD and ITO. Like this, the perovskite solar cell could be used in a superstrate configuration in a tandem device. The bottom solar cell was a standard double-side textured a-Si hetero

junction solar cell. The semi-transparent perovskite solar cell with 0.25 cm^2 achieved a J_{sc} of 14.5 mA/cm^2, 821 mV V_{oc}, and a FF of 51.9%, resulting in an overall efficiency of 6.2%. Because the ITO rear contact did not achieve the same conductivity as the full-area Ag metallization, this FF was considerably lower than that of an opaque reference cell (FF = 67%). The top cell transmitted about 55% of the photons in the wavelength range from 800 to 1200 nm. Under these illumination conditions, the silicon solar cell achieved 13.7 mA/cm^2 J_{sc}, 689 mV V_{oc}, and 76.7% *FF*, resulting in 7.2% efficiency. Adding the efficiencies of the individual sub-cells results in 13.4% efficiency, about 1.2%$_{abs}$ more than for the opaque perovskite reference, but considerably less than the efficiency of the silicon bottom solar cell.

The first two-terminal perovskite silicon solar cell was realized by Mailoa *et al.* in 2015 as well.[167] Now, the perovskite solar cell was processed directly on top of the silicon solar cell, again in a mesoporous *nip* configuration. The compact TiO_2 layer was deposited by atomic layer deposition (ALD) and the mesoporous layer by spin-coating and subsequent sintering at 450 °C. Because of this high temperature step, it was not possible to use a-Si heterojunction bottom solar cells. Instead, ion implantation was used for emitter and back-surface field formation. For the electric interconnection of the two sub-cells, a silicon tunnel junction was used. The junction was formed by PECVD deposition of an amorphous n^{++} on top of the p^{++}-emitter with subsequent annealing at 680 °C. Such a silicon tunnel junction has a refractive index matched to the silicon thus avoiding parasitic reflection losses, as well as relatively low absorption because of the indirect bandgap of silicon. As perovskite absorber $CH_3NH_3PbI_3$ was used, Spiro-OMeTAD was used as the HTL. The problem of creating damage by sputtering a TCO was circumvented by using Ag nanowires as the top electrode, capped with a LiF antireflection coating. The solar cell with a 1 cm^2 area achieved 13.7% efficiency.

Only one year later, Werner *et al.* surpassed the 20% efficiency mark, in a work that allowed for direct comparison of two- and four-terminal configurations.[168] As the bottom solar cell, a planar SHJ solar cell was used. The perovskite solar cell was deposited in *nip* configuration, with polyethylenimine (PEIE)/phenyl-C61-butyric-acid-methyl-ester (PCBM) as the bilayer ETL, $CH_3NH_3PbI_3$ as the absorber, and Spiro-OMeTAD as the HTL, protected by MoO_x from the sputtered hydrogenated indium oxide/indium tin oxide (IO:H/ITO) TCO stack. In the two-terminal configuration, the perovskite solar cell was deposited on top of an indium zinc oxide (IZO) interconnection layer, in the four-terminal case on an ITO covered glass substrate. In the two-terminal configuration, the Spiro-OMeTAD layer was facing toward the sun resulting in strong parasitic absorption losses up to 400 nm as well as in reflection losses due to the rather low refractive index of Spiro-OMeTAD. These losses could be avoided in the four-terminal configuration, where the perovskite solar cell was applied with the glass facing the sun. However, due to the need for additional lateral conductivity, the accordingly highly doped and thick TCO layers created parasitic absorption losses above 900 nm. In the end, the four-terminal device had an efficiency of 25.2% on an area of 0.25 cm^2, while the two-terminal configuration achieved 20.5% on 1.43 cm^2.

The parasitic absorption losses in the two-terminal configuration could be substantially reduced by switching to a pin configuration.[169] Bush *et al.* presented a device with a rear side texture SHJ bottom solar cell, an ITO interconnection layer, and NiO as the HTL. As the absorber, the more stable perovskite composition $Cs_{0.17}$ $FA_{0.83}$ $Pb(Br_{0.17}$ $I_{0.83})_3$ was used. Additionally, a complex front electrode consisting of a LiF passivation layer, PCBM, ALD deposited SnO_x or ZTO (Tin Zinc Oxide), sputtered ITO, and a LiF antireflection coating was used. The combination of the dense electrode and the stable absorber allowed for passing 1000 h of damp-heat test for an encapsulated device, demonstrating that also reasonable stability is in reach for perovskite silicon tandem devices.[169]

Comparable structures were then used by several groups to exceed 25% efficiency. Bush *et al.*[170] improved their device by optimizing especially the optics with adapted layer thicknesses and a polydimethylsiloxane (PDMS) stamp with random, pyramidal texture. Electrical improvements included using poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) as a hole transport material instead of NiO_x and a wider 1.68 eV bandgap perovskite composition, reaching overall 25% on 1 cm^2. Sahli *et al.*[171] realized the perovskite top cell on a both side textured silicon wafer, by using a hybrid deposition process for the perovskite absorber combining evaporation of Pb and Cs precursors with spin coating of solutions containing the organohalides. Furthermore, a nano-crystalline silicon tunnel junction was used. Specifically, the front side texture led to very high current and an overall 25.2% efficient device. However, the same efficiency was also achieved with a planar front and carefully optimized layer thicknesses.[172] Slightly higher efficiency is nevertheless possible by applying a textured light management foil and slightly reducing the absorber bandgap reaching 25.5%.[173] Further on, the energy yield for an encapsulated tandem cell with a textured front side is higher than for a comparable cell with a planar front.[174]

The highest efficiency for a perovskite silicon tandem device has been reported by the company Oxford PV, which achieved 28% on 1 cm^2.[175] Unfortunately, no details about the device structure have been published. A typical device configuration of perovskite silicon tandem solar cells, for a mesoporous nip solar cell and a pin configuration on silicon heterojunction solar cells, is shown in Fig. 10. Figure 11 shows the development of the efficiency of perovskite silicon tandem solar cells until end of 2019.

2. Outlook

The main limitation for the perovskite solar cells and thus also the perovskite silicon tandem devices is in the carrier extraction.[193] As typically bulk recombination is not an issue, the main challenge lies in the realization of well-passivated selective contacts that are effective for charge carrier extraction. Thus, many aspects discussed in the first part of this paper are also relevant for perovskite solar cells. In principle, similar materials could be applied for contact formation. However, in the past processing temperatures applied in perovskite silicon tandem solar cells were limited, due to the use of ITO covered a-Si SHJ bottom solar cells, and the temperature sensitivity of the perovskite absorbers. In consequence, low-temperature processes were developed, e.g., for TiO_2.[194] Building on the progress reported above on new passivated selective contact materials and interconnection layers, e.g., on the basis of nano- or polycrystalline silicon, the allowable thermal budget for the bottom solar cell should have been increased, allowing for the use of higher temperatures at least for the first contact layer deposited. Further going into that direction, it should even be possible to completely eliminate the need for an interconnection layer by creating a tunnel junction directly between the last contact layer of the silicon

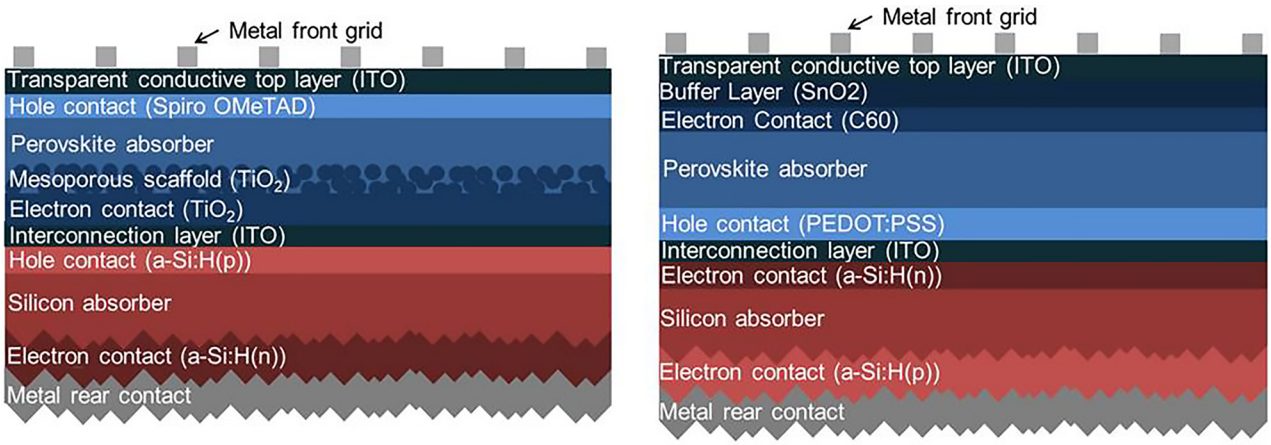

FIG. 10. Typical device configuration of perovskite silicon tandem solar cells, for a mesoporous *nip* solar cell on the left, and a *pin* configuration on the right.

solar cell and the first contact layer of the perovskite solar cell, as demonstrated in Ref. 195. Here, a recombination contact was formed between boron-doped p^{++} emitter of the silicon solar cell and the solution process SnO_2 ETL of the perovskite solar cell.

Nevertheless, temperature and process limitations will remain for all layers deposited after the perovskite absorber is formed. Related to this issue is the question, whether the nip or the pin configuration is most suitable for two-terminal perovskite silicon tandem solar cells. As discussed above, currently the *nip* configuration is limited by strong parasitic absorption happening in the HTL, which faces the sun. On the other hand, record perovskite single junction devices are realized in the nip configuration.[196] Finding low absorbing HTL materials will therefore be crucial to tap the high efficiency potential of the *nip* configuration also for tandem devices.

Much less attention has been devoted until now to the rear side of a perovskite silicon tandem solar cell. As discussed above, typically rear side textured SHJ solar cells are being used in research. This could also be a viable approach for industrial production, if new facilities for the production of perovskite silicon solar cells have been installed, as under way by Oxford PV and Meyer Burger.[197] On the other hand, when already existing production infrastructure should be used, PERC like rear structures could be an option. However, only little work has been performed on the realization of perovskite silicon solar cells using PERC like bottom solar cells. One challenge is that the front processes have to be adapted considerably to realize the electrical interconnection to the perovskite solar cell while maintaining surface passivation.[187]

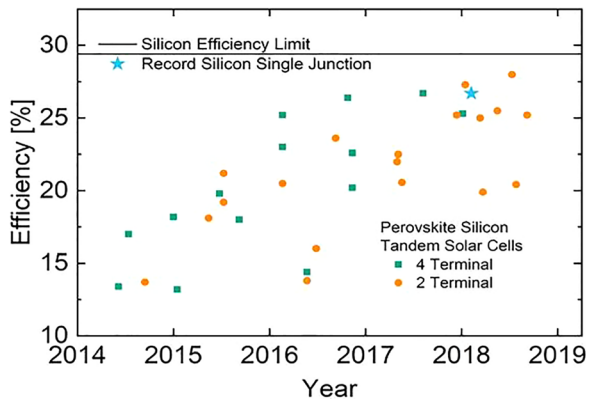

FIG. 11. Development of the efficiency of perovskite silicon tandem solar cells. In the four years since the first realization, the efficiency could be doubled. With data from Refs. 166–173 and 173,175–192, silicon record efficiencies have already been exceeded and the fundamental efficiency barrier for silicon solar cells is approaching fast.

Another major task for future research on perovskite silicon tandem solar cells is the integration of a front surface texture. Many publications have predicted the possibility of practical efficiencies beyond 30%, but detailed analyses suggest that textured fronts are necessary to achieve this goal.[166,174,198] The used anti-reflection foils used in the record device reported above do not work in a module configuration, because of their low-refractive index. However, there is only little work on the deposition of perovskite absorbers on textured surfaces.[171,199] Furthermore, it will be necessary that all selective contacts, passivation, and buffer layers can also be deposited pinhole-free on these textured surfaces. These might require also adaption of silicon surface textures. Hence, one can conclude that substantial additional research is necessary to tap the full potential of perovskite silicon tandem solar cells.

IV. CONCLUSION

In this overview paper, potential technologies were discussed, which are suitable to realize silicon based solar cells with the highest efficiencies. Assuming the efficiency development from Fig. 1 as a starting point and the 0.5%–0.6% annual efficiency improvement also for future development, the technologies presented in this paper can be built in as follows (see Fig. 12).

Today, the top efficiency in PERC production is at around 22.9% (star in Fig. 12). Technologies for improving this efficiency are already known (selective emitter, thinner metal fingers, improved material, and passivation) and can be integrated into production. However, the fundamental efficiency limitation of the PERC cell, the metal/semiconductor interface recombination, is limiting this cell concept. Further efficiency improvements for PERC solar cells require further

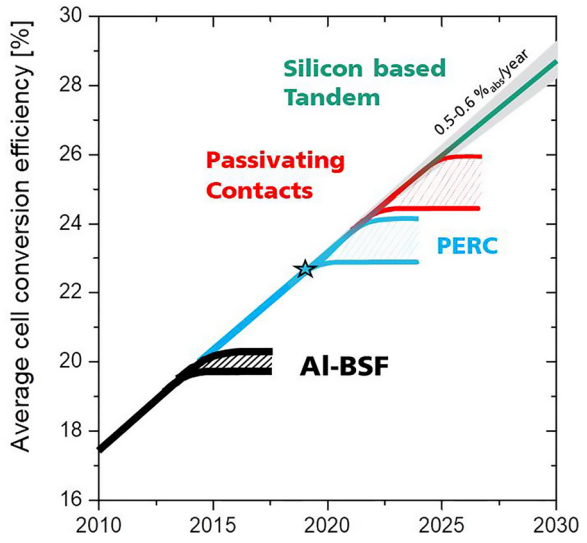

FIG. 12. Potential further technological development in silicon photovoltaics based on historical efficiency increases (0.5–0.6%$_{abs}$) and the technologies currently being investigated in research. Within the area of passivating contacts, both side contacted solar cells and back junction back solar cells can be relevant technologies.

miniaturization of the metallized areas; thus, improving existing technologies or developing new technologies is necessary to stay on the efficiency improvement path. For example, further reduction of the metallized surface leads to higher demands on the alignment accuracy between the highly doped areas and the metal, which can lead to higher process costs. This possible stagnation of efficiency can open the door for alternative high efficiency concepts to come into the market.

Solar cells with passivating contacts, such as silicon heterojunctions (SHJs) or polysilicon-based contacts (e.g., TOPCon), are able to exceed the efficiency limit of PERC. The SHJ technology is already in the starting blocks and is being evaluated by several cell manufacturers. For example, the company Renewable Energy Corporation (REC), in cooperation with equipment manufacturer Meyer Burger, has produced a 380 Wp SHJ module, which is scheduled to go into production in 2019. For the TOPCon technology, some cell manufacturers have already shown that very high efficiencies can be achieved by upgrading existing lines. The advantage of retrofitting existing lines is that the capital costs required are much lower than for the construction of a completely new technology, such as the SHJ. However, there are still some open questions to be answered: Which deposition technology is the most cost efficient? Which metallization produces the least damage with the least poly Si-layer thickness? Can both side contacted solar cells be used to achieve the highest efficiencies or do we need a low cost production technology for back junction back contact solar cells? Whether passivating contacts can enter mass production and replace the PERC technology as the industrial standard depends on whether a cost-effective production technology can be developed that can compete with the already scaled standard technologies.

With silicon-based tandem solar cells, many more questions need to be answered before industrialization on a large scale is possible. The biggest advantage of this approach, however, is the high efficiency potential allowing efficiencies above the theoretical limit of single-junction silicon solar cells. These high efficiencies offer a unique selling point that allows a market entry at higher cost. Applications such as integration in cars, aircrafts, or high-altitude pseudo-satellites (HAPS) are already being investigated and deployed. These markets with a lower cost pressure are necessary to finance the necessary development costs.

In summary, it can be said that silicon technology in photovoltaics has not only shown an outstanding development in the past, but that there are new exciting technologies that have the potential to further advance photovoltaics in the coming years.

ACKNOWLEDGMENTS

The authors would like to thank sincerely all co-workers at Fraunhofer ISE who have contributed to the development of high-efficiency silicon solar cells in the last decades.

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