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Space-charge limited current in the series resistance of GaAs solar cells

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Abstract
We report the observation of space-charge limited current in the current–voltage characteristics of GaAs solar cells as evidenced by an abrupt decrease in the series resistance, a concurrent steep increase in the dark current at a threshold voltage and the observation of a quadratic dependence of the dark current on the voltage across the series resistance above threshold. The abrupt decrease in the series resistance at threshold, results in the observation of negative differential resistance and a subsequent hysteresis in the current–voltage characteristics. Auger electron spectroscopy analysis shows that the space-charge limited current can be attributed to a thin insulating CrAs layer at the contact/semiconductor interface.

(Some figures may appear in colour only in the online journal)

The energy conversion efficiency of GaAs solar cells can be degraded by non-optimized material quality and surface passivation [1], a large series resistance [2] and other processing-induced effects. The typical model [3] for the series resistance of a GaAs solar cell includes a lumped series resistance component in series with a processing-dependent contact resistance. We recently reported the observation of an anomalously large series resistance, a charge-induced decrease in the series resistance and a concurrent steep increase in the dark current at a threshold voltage and subsequent hysteresis in the current–voltage (I–V) characteristics of GaAs single p–n junction solar cells [4]. Our data suggested that the observed switch in the series resistance can be attributed to a thin insulating layer at the contact/semiconductor interface that contributes to a voltage-and-light-dependent component in the solar cell series resistance. In this paper we show that the observed charge-induced resistance switching can be attributed to space-charge-limited current flow in a thin insulating CrAs layer at the contact/p-GaAs interface.

The equivalent circuit model [5] of a solar cell, which includes the series resistance and neglects shunt resistance, yields the following expression for the dark current I, as a function of the applied voltage V,

$$I = I_0(e^{q(V-V_r)/nkT} - 1) \quad (1)$$

I_0 is the reverse dark current, V_r is the voltage across the series resistance, q is the electron charge, n is the empirical diode ideality (typically $1 \leqslant n \leqslant 2$), k is the Boltzmann constant and T is the temperature. This model uses a lumped series resistance to approximate the voltage-dependent distributed series resistance associated with non-uniform current flow across the p–n junction to the contacts [7, 8] and allows for the possibility that V_r may have a nonlinear dependence on I. The shunt resistance of our solar cells, which is $1.5 \times 10^9\ \Omega$, has a negligible effect on the I–V characteristics for $V > 0.1$ V.

The non-optimized solar cell structures used in our measurements, which were grown by molecular-beam-epitaxy, consist of the following layers: a n-GaAs substrate with a doping of 10^{18} cm^{-3}, 0.6 μm n-GaAs doped 5×10^{17} cm^{-3}, 0.5 μm p-GaAs doped 5×10^{17}, 300 Å p-$Al_{0.45}Ga_{0.55}As$ doped 1×10^{18} cm^{-3}, and 500 Å p-GaAs doped 3×10^{18}. Standard photolithography and a phosphoric acid etch were used to define mesa-isolated 1 and 2 mm square cells. A gold/tin/gold metallization (on the order of 150 A/250 A/2500 A) was deposited in an electron beam vacuum evaporator onto the back of the substrate; followed by rapid thermal annealing at 350 C for 60 s. Photolithography was used to define the p-type metal contact pattern on each mesa and a chromium/gold metallization (on the order of 300 A/2500 A) was deposited followed by a metal liftoff. The sample temperature during metal deposition was around 300 K. Just prior to loading the samples into the deposition chamber, the devices were dipped in a 1 : 1 solution of H_2O : HCl for 60 s, rinsed in de-ionized H_2O for approximately 30 s then blown dry with nitrogen gas. Current–voltage measurements were carried out on devices in the dark using a source-measure power supply and 0.01 V increments in its output to increase the applied voltage and measure current. A separate voltmeter was used to measure the applied voltage across the solar cell.

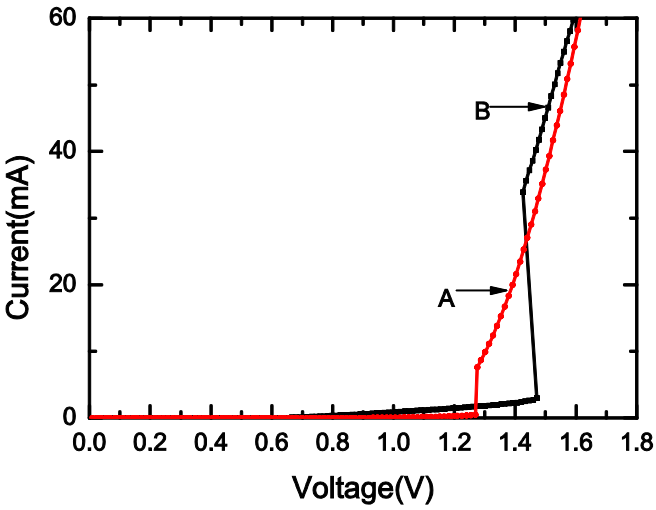

Figure 1. 295 K dark current–voltage characteristics of solar cells that exhibit space-charge limited current.

Figure 1 shows the dark current–voltage (I–V) characteristics of two solar cells that exhibit anomalous series resistance and diode turn-on characteristics. With increasing forward voltage, device A and device B exhibit an anomalous small decrease in $\mathrm{d}V/\mathrm{d}I$ over the range $V < 1.27$ V and $V < 1.45$ V respectively, and a steep increase in current with a concurrent decrease in the series resistance at $V = 1.27$ V and $V = 1.46$ V, respectively. The I–V characteristics of these devices and the anomalous decrease in $\mathrm{d}V/\mathrm{d}I$ can only be fitted by (1), indicating that device A and device B have an anomalous voltage-dependent series resistance component that is much larger than the typical contact series resistance over the range $V < 1.27$ V and $V < 1.45$ V, respectively. The relatively large resistance of the voltage-dependent component compared to the contact resistance prevents a sharp decrease in $\mathrm{d}V/\mathrm{d}I$ (increase in the diode current) with increasing forward bias. Over the range $0\,\mathrm{V} < V \leqslant 0.6\,\mathrm{V}$, the measured idealities of device A and device B are 2 and 1.4 respectively, indicating that the anomalous series resistance in these devices is not related to transport across the p–n junction.

At $V = 1.27$ V for device A and $V = 1.43$ V for device B, the voltage-dependent series resistance component undergoes an abrupt transition from a high-resistance regime to a low-resistance regime as manifested by the very steep rise in current. Due to the abrupt decrease in the resistance of the voltage-dependent component, the current is determined primarily by the p–n junction at threshold and by the thin insulating layer above threshold. The abrupt decrease in the series resistance of device B results in the observation of negative differential resistance at threshold and a hysteresis in the I–V characteristics as the applied voltage is decreased slowly from the region $V \geqslant 1.43$ V as shown in figure 2. The hysteresis is unstable if the applied voltage is decreased faster than a certain undetermined rate. These observations confirm that the voltage-dependent series resistance switching involves the trapping of carriers. The observed current increase at threshold depends on the p–n junction characteristics, the insulating layer trap density and lifetime, as well as the measurement time.

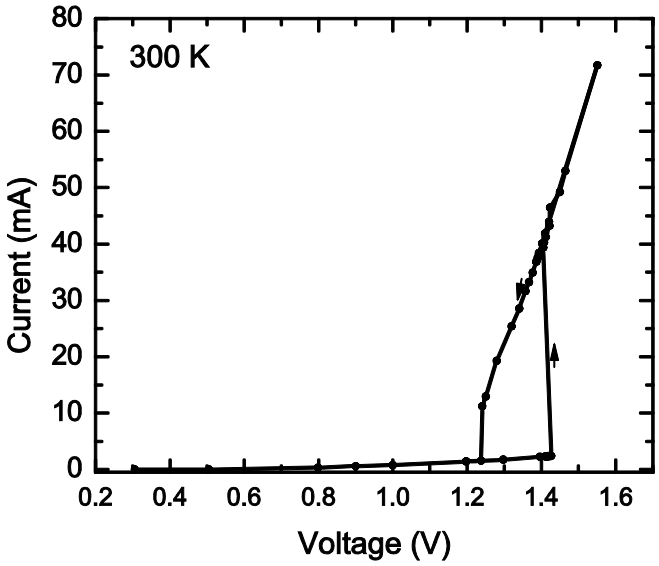

Figure 2. Observed hysteresis when the applied voltage to solar cell B is decreased from the region $V > 1.45$ V. Reprinted from [2]. Copyright 2012, AIP. Licensed under Creative Commons Attribution 3.0 Unported.

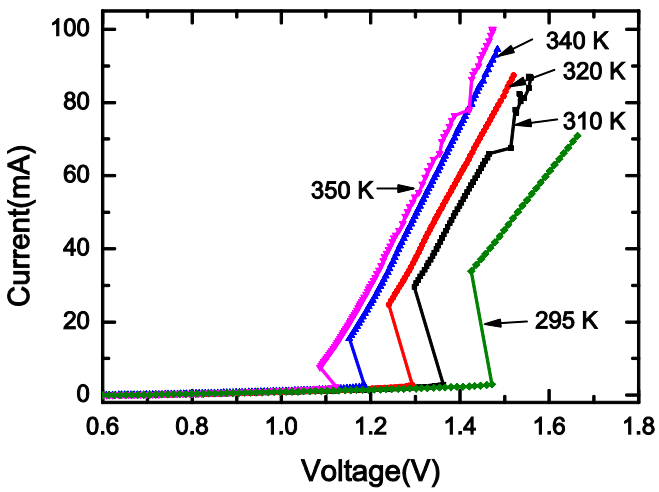

Figure 3. Dark current–voltage characteristics of solar cell B over the range 295–350 K. Reprinted from [2]. Copyright 2012, AIP. Licensed under Creative Commons Attribution 3.0 Unported.

The temperature dependence of device B's I–V characteristic over the range 295 to 350 K, shown in figures 3 and 4, shows that the threshold voltage for resistance switching and the magnitude of the current increase at threshold, decrease with increasing temperature. Figure 4 shows clearly that device B's turn-on is good for $V < 0.7$ V but suffers from the effect of the insulating layer series resistance for $V > 0.7$ V. One possible mechanism for the observed I–V characteristics is space-charge limited current flow in a thin insulating layer in series with the junction. It is well known that under an applied voltage, charge injection occurs at the semiconductor/insulator and metal/insulator interfaces when the metal or semiconductor work function is lower than that of the insulator. Current flow in the insulator is space-charge limited and dependent on the trap density in the insulator [6–10]. At a threshold voltage called the traps-filled-limit

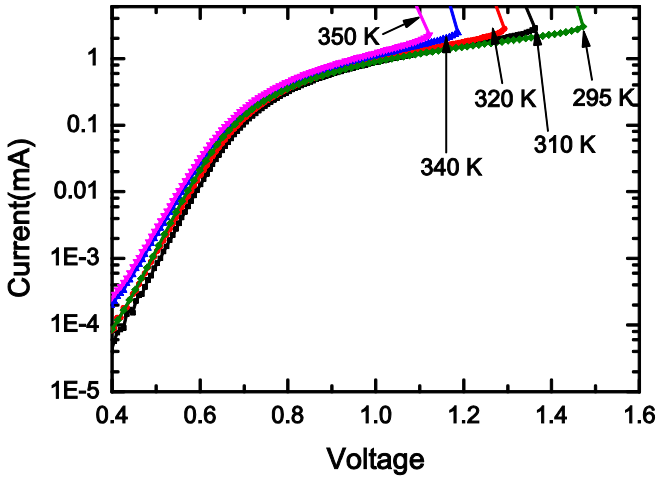

Figure 4. Low current region of the dark current–voltage characteristics of solar cell B over the range 295–350 K.

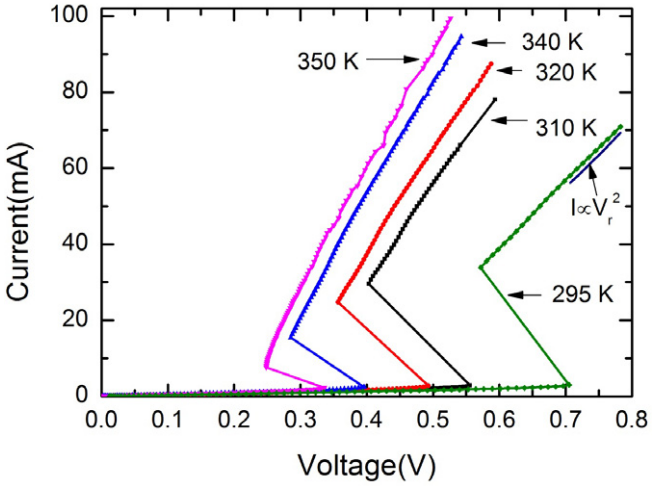

Figure 5. Dark current–voltage characteristics of the series resistance in solar cell B over the range 295–350 K.

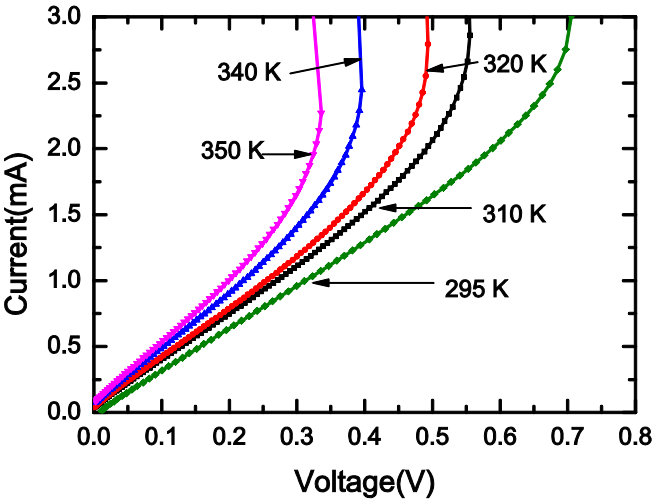

Figure 6. Low current region of the dark current–voltage characteristics of the series resistance in solar cell B over the range 295–350 K.

voltage, current flow undergoes a sharp transition from a relatively high-resistance Ohm's law regime ($I \propto V_r$) to a low-resistance Mott–Gurney's law regime ($I \propto V_r^2$) as manifested by a steep rise in current. The traps-filled-limit threshold voltage across the insulator V_T, is given by the expression $V_T = ea^2N_t/2\varepsilon$, where, e is the electron charge, a is the thickness of the insulating layer, N_t is the insulator trap density and ϵ is the static dielectric constant of the insulator [6]. The voltage across the insulating series resistance $V_r(I)$, can be obtained from the measured solar cell I–V characteristics using the following procedure. A plot of the normalized dark current as a function of applied voltage over the range $0\,V < V \leqslant 0.6\,V$ is first used to determine the diode ideality. Measurements show that $I < 10\,\mu A$ for $V \leqslant 0.5\,V$ so we can make the approximation that $V_r \approx 0$ over this range. This approximation has a negligible effect on the analysis if the resistance of the insulating layer is less than approximately $3000\,\Omega$. Using this approximation, the reverse dark current is determined by fitting the measured I–V characteristic with equation (1) over the range $V \leqslant 0.5\,V$. $V_r(I)$ is then obtained by fitting the I–V characteristics with equation (1) for $V > 0.5\,V$. Figures 5 and 6 show the I–$V_r(I)$ characteristics obtained for the insulating series resistance in device B for various temperatures over the range 295–350 K. The 295 K data show that $I \propto V_r$ for $V_r < 0.45\,V$, the occurrence of a traps-filled-limit threshold at $V_r = V_T = 0.71\,V$, and that $I \propto V_r^2$ for $V_r > 0.72\,V$ confirming the occurrence of space-charge-limited current flow in the series insulating layer. A theoretical fit line is also shown in figure 5 with a vertical offset to more clearly show that at 295 K, $I \propto V_r^2$ for $V_r > V_T$. We determine from figure 6 that, for $V_r < 0.45\,V$, the 295 K resistance of the thin insulating layer in series with the junction, is approximately $308\,\Omega$ which confirms the validity of the approximation that $V_r \approx 0$ over the range $V \leqslant 0.5\,V$. The observed negative differential resistance at threshold is a consequence of the series configuration of the p–n junction and the insulating layer. Figure 5 shows that V_T monotonically decreases with increasing temperature up to 350 K. The decrease in V_T with increasing temperature can be attributed to either an increase in ϵ or a decrease in N_t.

Temperature cycling over the temperature range 295–350 K shows that changes in V_T are reversible. This shows that N_t is not sensitive to temperature over this temperature range since temperature-induced changes in N_t are usually irreversible. We therefore neglected the temperature dependence of N_t. Due to trapping of carriers in the insulator, ϵ may be thermally activated [9, 11] with a dependence given by $\varepsilon = \varepsilon_0 e^{-\phi/kT}$ where ϵ_0 is the dielectric constant at $T \gg 300\,K$ and ϕ is the activation energy required to change the trap occupancy of the traps involved in the trap-mediated dielectric response of the insulating layer. The data shows that $\phi \approx 0.1\,eV$. The insulating series resistance in device A exhibits similar characteristics but has $V_T = 0.18\,V$ at 300 K.

Our data suggests that the observed effects can be attributed to a thin insulating layer between the Au/Cr Ohmic metal and the p-GaAs. Auger electron spectroscopy (AES) analysis of the Ohmic metal/p-GaAs interface was carried out on a device that exhibited a low contact resistance and on a device with an insulating series resistance comparable to that in device B. The AES sputter depth profile of the device

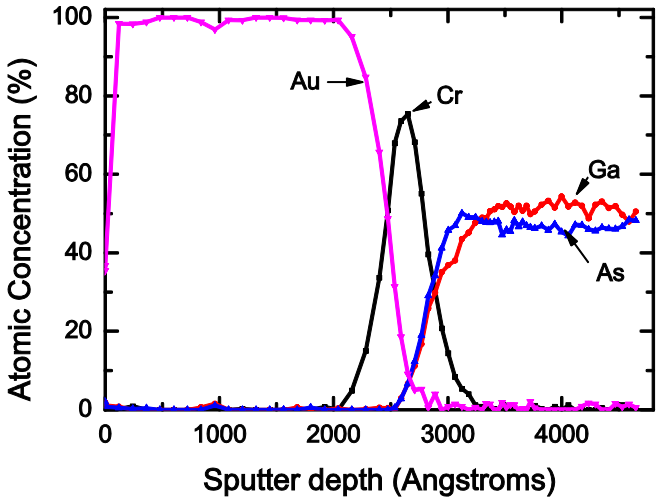

Figure 7. Auger sputter depth profile of the sample with a normal contact resistance.

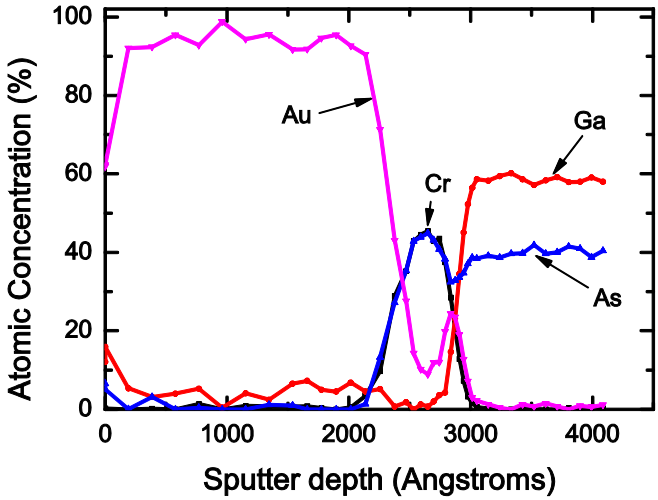

Figure 8. Auger sputter depth profile of the sample with an insulating CrAs layer at the Au/Cr contact/p-GaAs interface.

with an insulating series resistance (see figure 8) shows the presence of a 400 Å thick CrAs layer at the GaAs interface that is formed after diffusion of As out of GaAs into the deposited Cr layer. In contrast, figure 7 shows that the device with the low contact resistance does not show any diffusion of As into the Cr layer. Strong chemical reactivity and the formation of Cr–As [12] and Cr–Ga [13] compounds have been observed before at the Cr/GaAs interface. The data implies that under an applied voltage, holes are injected into the insulating layer before they are collected by the contact metal. The thickness of the insulating CrAs layer in device $B \approx 400$ Å, and assuming that $\varepsilon \approx 10\varepsilon_0 = 8.85 \times 10^{-13}\,\mathrm{F\,cm^{-1}}$ at 295 K, we estimate that the insulating CrAs trap density $N_t = 2\varepsilon V_T/ea^2 \approx 4.8 \times 10^{17}\,\mathrm{cm^{-3}}$. It can be shown that $N_t/n_0 \approx S_T/S_0$, where n_0 is the equilibrium carrier density in the insulating layer, S_T and S_0 are the slopes of the insulator I–V_r characteristic at threshold and in the Ohmic region, respectively [6]. Using the data in figure 6 and the contact area we estimate that $n_0 \approx 2.3 \times 10^{15}\,\mathrm{cm^{-3}}$ and that the insulator mobility, $\mu \approx 1.8 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at 295 K. The low mobility suggests that the low-field hole transport mechanism involves hopping between traps in the insulator [14]. Figure 6 shows that the low-field series resistance decreases monotonically over the range 295–350 K. A plot of $\log \mu$ as a function of $1/T$ shows that the hole mobility is thermally activated and given by the expression [14]

$$\mu = \mu_0 \mathrm{e}^{-E_a/kT} \tag{2}$$

where μ_0 is the hole mobility at $T \gg 300$ K and E_a is the activation energy. The data shows that for space-charge limited hole transport in the CrAs insulating layer, $E_a \approx 0.05$ eV and $\mu_0 \approx 4 \times 10^{-2}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Resistance switching in metal/oxide/metal devices has been observed and attributed to interface [15] or bulk [16, 17] charge-induced changes in the interface barrier height. The observed linear dependence over the low-voltage range of the I–V_r characteristic, shown in figure 6, does not support a mechanism involving transport over an interface barrier. The observed temperature dependence of the I–V_r characteristic precludes direct tunnelling and suggests a temperature-activated hopping or tunnelling low-field transport mechanism.

In conclusion, we report the observation of space-charge limited current in the series resistance of GaAs solar cells as evidenced by an abrupt decrease in the series resistance, a concurrent steep increase in the dark current at a threshold voltage and a quadratic dependence of I on V_r above threshold. The abrupt decrease in the series resistance at threshold, results in the observation of negative differential resistance and subsequent hysteresis in the current–voltage characteristics. Auger electron spectroscopy data shows that the space-charge limited current can be attributed to a thin insulating CrAs layer at the p-GaAs contact/p-GaAs interface that contributes to a voltage-dependent component in the solar cell series resistance. The Au/Cr system is commonly used to form an unannealed or a low-temperature-annealed Ohmic contact to p-GaAs that has a low specific contact resistance $\approx 10^{-5}\,\Omega$ cm, excellent adherence and morphology, and good stability [13, 18]. Even though a large processing-induced series resistance is not observed in all GaAs solar cells with Au/Cr p-type contact, it is important to understand the processing-induced formation of an insulating layer in GaAs solar cells because this could ultimately lead to an increase in the processing yield and reduced manufacturing cost of GaAs solar cells. Further research is needed to determine and eliminate the processing-induced conditions that result in the formation of the insulating CrAs layer in some solar cells. The results presented in this paper provide useful insight in future research on this problem.

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