Review of Scientific Instruments | ARTICLE | scitation.org/journal/rsi

How to maximize the bandwidth without increasing the noise in op-amp-based transimpedance amplifiers using positive feedback

Cite as: Rev. Sci. Instrum. 93, 043004 (2022); doi: 10.1063/5.0079747
Submitted: 24 November 2021 • Accepted: 21 March 2022 •
Published Online: 13 April 2022

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ABSTRACT

The bandwidth of very high gain (≥100 MV/A) transimpedance amplifiers is restricted to below 100 kHz, unless measures are employed to mitigate the effect of circuit parasitic capacitances. Current approaches involve significantly increased circuit complexity and component count. They may suffer unwanted noise pickup or destructive capacitive coupling to ground, the latter restricting the available bandwidth. We demonstrate that combining a positive feedback circuit with a low-pass filter network extends the bandwidth of a transimpedance amplifier out to the limit of gain peaking (>1 MHz) without increasing the noise signal. The circuit uses a single inverting amplifier and very large feedback-resistance to provide a canceling parasitic-capacitance positive feedback signal. This can negate both the negative feedback-resistor parasitic-capacitance and the input/output pin parasitic-capacitance of the transimpedance amplifier. The circuit solves the problem of destructive distributed-capacitive coupling to ground along the feedback resistor.

I. INTRODUCTION AND MOTIVATION

Transimpedance amplifiers (TIAs) provide the first stage high-gain, low-noise, amplification from current-source devices, such as receiving terahertz antenna,[1,2] photodiodes, and ion-cyclotron resonance cells employed in Fourier-transform mass spectroscopy.[3] The TIA converts the current source signal to an amplified voltage signal; thereafter, cascaded voltage amplification stages may be added to achieve the required signal voltage-magnitude and total circuit bandwidth. Decompensated operational-amplifiers (op-amps) with their enhanced gain bandwidth product (GBWP) and lowest values of both inverting input-spot-current-noise (i_n) and noninverting input-spot-voltage-noise (e_n) provide the best performance in terms of both bandwidth and signal to noise at very high gains (>1 MV/A) and low capacitive inputs (~10 pF).

A thorough review of previous work to extend the bandwidth of TIAs is presented by Štubian *et al.*[3] However, it is useful to illustrate both the cause of the bandwidth limitation inherent in very high gain TIAs and the signal to noise advantage afforded overcoming this constraint (the latter is often assumed without explanation in the literature) before discussing the merits and limitations of the three main approaches presented to date.

Figure 1 displays, in schematic, a standard configuration of a current source (of infinite parallel-source resistance) of magnitude 1 nA amplified by a TIA. Parasitic capacitance C_F of 50 fF in parallel to the feedback resistor R_F is presented and quoted for a standard 0805 resistance package. Employing suitable spice software, for example, Micro-Cap or LTspice, bandwidth and voltage-output-noise-density V(Onoise) representative signals of various resistor feedback configurations may be computed. Employing a 1 GΩ feedback resistor on the TIA would yield a useful 1 V signal at its output and a V(Onoise) of 4 $\mu V\sqrt{Hz^{-1}}$. However, the bandwidth is severely constrained by the parasitic capacitance and rolls-off at 5.5 kHz with a total rms noise of 240 μV. To achieve a flat response out to 1 MHz,

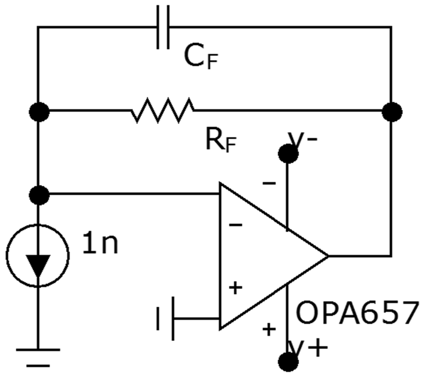

FIG. 1. Schematic of TIA.

the TIA feedback resistor must decrease to 1 MΩ, delivering a 1 mV signal with a noise floor of 130 $\mathrm{nV}\sqrt{\mathrm{Hz}^{-1}}$ and total RMS noise of 120 μV. Immediately obvious is that whereas voltage output scales with gain, noise scales only with the square root of gain. Two cascaded following voltage-gain stages of total 1000 gain are required to restore the 1 V signal with 130 $\mu\mathrm{V}\sqrt{\mathrm{Hz}^{-1}}$ floor noise and total RMS noise of 120 mV (at 1 MHz). However, reducing the parasitic capacitance to 0.1 fF, a 1 GΩ feedback resistor delivers a flat gain response out to 1 MHz with the original floor-noise of 4 $\mu\mathrm{V}\sqrt{\mathrm{Hz}^{-1}}$ and total RMS noise signal of 7 mV. There is a clear, signal to noise, advantage to be gained by reducing the effect of the feedback parasitic capacitance. Before proceeding, it must be ascertained if the TIA is now stable. Employing the Tian method within Micro-Cap delivers a phase margin of 57° and a gain margin of 60° indicating that this is so.

A number of approaches to reduce the effect of parasitic feedback capacitance within a TIA have been proposed and can be divided broadly into three categories. The first employs an additional low-pass filter of equal time constant in the feedback path,[3–5] $R1C_G = R_FC_F$ see Fig. 2, to exactly counter the impedance fall-off of $R_F \| C_F$ leaving an effective impedance of R_F + R1 up to the cut-off frequency $(R1C1)^{-1}$. A drawback to this approach, if R1 is of too great a magnitude, is noise pick-up occurring at and beyond the connecting node between R_F and R1 feeding back into the TIA inverting input. A constraint on reducing R1 is suitable capacitors with high frequency performance above 1 nF. A variation on this method employs a resistive divider to reduce the magnitude of the feedback resistor while delivering the same transimpedance.[6] For a simple front-end TIA, this approach has no value, since the path to ground connected to the input of the TIA increases the noise signal sufficiently to negate the bandwidth advantage.

The second employs shielding to ground between the resistor pads of the feedback resistor to decrease the parasitic capacitance.[1] While this is effective, the capacitive coupling to ground under the feedback resistors gives rise to a potential infinite number of poles, tending to a lossy and non-uniform transmission line and is considered difficult to compensate for,[5] although no evidence for this assertion is presented in the literature. The last method adds additional follow-on circuitry to counter the gain roll-off.[7] Here, an additional voltage amplifier stage with gain increasing with frequency is added after the TIA to counter the signal roll-off. A spice analysis of the circuit expounded in Ref. 7 reveals that this approach can significantly extend the gain bandwidth by two orders of magnitude while halving the input referred to noise signal. However, the bandwidth is still limited to the low 10's of kHz for the transimpedance gain of 1 GV/A.

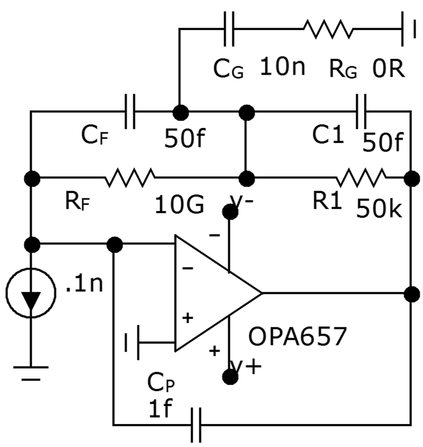

FIG. 2. Fully compensated feedback network. Note that C_P is the parasitic capacitance across input/output pins due to pads or wire connections and R_G may be added to restrict the bandwidth to aid stability.[3]

II. INCREASED CIRCUIT GAIN BANDWIDTH PRODUCT

To date, a far more effective approach is the combination of the first method with additional gain stages added within the feedback loop to increase the open loop gain.[3–5] This is demonstrated with reference to the amplifier circuit shown in Fig. 2. Here, if the pad/connection parasitic capacitance across the input and output pins of the TIA is neglected, a gain bandwidth of 370 kHz is theoretically possible with a fully compensated feedback network. Conversely, just 1 fF additional stray capacitance (C_p) across these pins reduces this to just 25 kHz as the feedback network cannot compensate for this capacitance. However, the standard technique of adding gain stages within the feedback loop (Fig. 3) to enhance

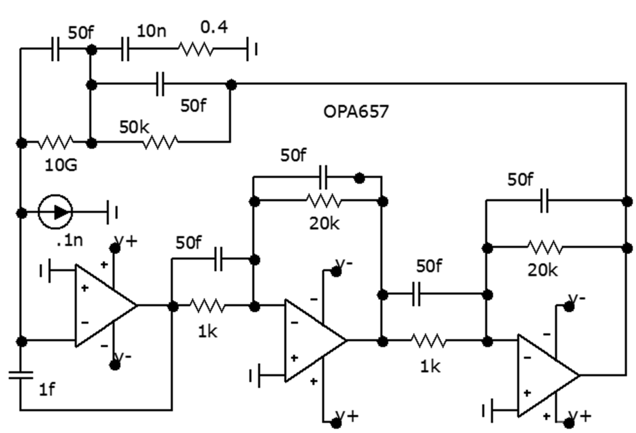

FIG. 3. Additional gain stages within the feedback loop.

the loop gain and thus directly the circuit bandwidth works well for very high transimpedance amplifiers.

To extend the bandwidth back out to the original 370 kHz requires the gain bandwidth product (GBWP) of the circuit to be increased from the initial 1.6 GHz of the OPA657 amplifier to 24 GHz (1.6 × 370/25), corresponding to an increase by a factor of 15 in the open loop gain. However, if the GBWP is instead substantially increased to 640 GHz by the inclusion of two additional 1:20 voltage gain stages, this dramatically increases the tolerance of the circuit to the 1 fF parasitic capacitance, extending the bandwidth out to 10 MHz. A GBWP of 300 GHz is quoted for the circuit presented in Ref. 5 and a spice analysis undertaken by the present authors of the circuit produces a flat frequency response out beyond 1 MHz at the transimpedance gain of 10 GV/A, in-line with the results presented. The computed V(Onoise) is 15 $\mu\mathrm{V}\sqrt{\mathrm{Hz}^{-1}}$. For the circuit presented in Ref. 3, provided all protection circuitry is removed, a spice analysis also indicates that a flat frequency response out to 1 MHz is possible with a computed V(Onoise) of 4 $\mu\mathrm{V}\sqrt{\mathrm{Hz}^{-1}}$. Here, the transimpedance gain is 1 GV/A.

The reference design for the implementation of a low pass filter and additional gain stages all within the feedback loop is presented in Ref. 5. To achieve the impressive performance, care was taken to achieve a flat frequency response of the "fully compensated feedback network." For a feedback resistor value of 10 GΩ, the transfer characteristics quoted are flat, out beyond 6 MHz with no appreciable phase shift up to a frequency of 5.7 MHz. This uniformity of the feedback-loop transfer function was realized by double shielding of the 10 GΩ resistor to prevent destructive capacitive coupling to ground. The input stage amplifier is a cascade arrangement that minimizes the Miller capacitance and maximizes bandwidth. The second gain stage now comprises a relatively low value of feedback resistance (~5.4 MΩ) limiting the effect of both the parasitic feedback capacitance and any stray capacitance present across the input/output pins on its bandwidth. Finally, the input amplifier comprising the four junction FETs and the 10 GΩ feedback resistor with the capacitance compensation network are mounted "in air." This last point is often overlooked; at frequencies out to 1 MHz coupled with such large circuit resistance values, inductance is not an issue. However, parasitic capacitance is problematic, mounting components in air instead of on the circuit board while optimizing lead lengths, proximity, and orthogonal orientations minimizes this.

Achieving such a large bandwidth in reality is not straightforward. Information on stability of the circuit and indeed published results are sparse to say the least in Ref. 5. The more recent publication of Ref. 3 is far more generous in the detail and quotes a bandwidth of ~100 kHz for a feedback resistance of 1 GΩ; this compares with a spice analysis of 250 kHz for the full circuit where additional routing stray capacitances are not considered. Stripping out all the circuit protection achieves a theoretical bandwidth of 1.6 MHz. However, within the text, circuit stability is alluded to as being a significant issue with additional protection circuity incorporated to ensure stable operation and it is uncertain if this bandwidth would be achieved in practice.

What is not in doubt is the considerable increase in component count and circuit complexity required by these approaches to mitigate the presence of the parasitic feedback capacitance, C_F, and the capacitance across the input/output pins of the TIA, C_p. We propose a different approach, one that only requires an additional inverting unity-gain voltage amplifier placed after the TIA with its output fed, via a high value resistor, back to the input of the TIA. The circuit has the advantage that all components are placed onto the PCB using standard pad dimensions. The proposed circuit can compensate for both the parasitic feedback capacitance (C_F) and the capacitance (C_p) generated across the input/output pins of the TIA. The final and significant advantage is the circuit's tolerance to distributed parasitic capacitive coupling to ground along the feedback resistors.

III. POSITIVE FEEDBACK INTRODUCTION

One overlooked method to extend the bandwidth of a TIA is to use a follow-on unity-gain and inverting voltage amplifier to feed a positive signal back to the input of the TIA that exactly counters all negative capacitive feedback signals. Unlike negative feedback, the consideration of positive feedback from the output of an amplifier to the input is uncommon. There are a number of reasons for this. The idea is only useful if the signal originates from a current source and a TIA is utilized as the first stage amplification. For a voltage amplifier circuit, the ratio of the capacitive feedback to the resistive feedback signal can be minimized simply by reducing the magnitude of the feedback resistor value. Additional signal amplification can then be undertaken in the following amplification stages with minimal loss of signal to noise ratio. For a first stage TIA, decompensated amplifiers are often considered due to their high GBWP. An example is the LTC6268-10, which is gain of 10 stable and requires that $C_{IN}/C_F \geq 10$. Consequently, here, the application of positive feedback is of most use for very high values of the feedback resistor (>100 MΩ) and very low values (<1 pF) of total capacitance to ground, C_{IN}, at the negative pin input. The stability minimum feedback capacitance can be calculated from[8]

$$C_F + C_P > \sqrt{(C_{IN}/(2\pi \times GBWP \times R_F))}, \tag{1}$$

and is now below 1 fF. Attaining such a low value of capacitance across the input and output pins of the TIA is difficult, restricting the attainable bandwidth. However, such low values of capacitance are possible employing positive feedback. The final reason is a direct quote and regards human nature.[9] "Amplifier gain enhancement via positive feedback has not yet gained widespread acceptance due to popularly held beliefs regarding the potential for instability. These conceptions are rooted in the fact that researchers have not considered using these structures as part of a larger system providing negative feedback." In other words, researchers consider the addition of a positive feedback element to be intrinsically unstable even if the total circuit feedback is negative. This is not the case.

IV. POSITIVE FEEDBACK METHODOLOGY

The positive feedback circuit should add a constant additional 180° phase change over the frequency range of interest. The positive feedback path and pads should be as identical to the negative feedback path and pads as possible and use the same resistor component package. This should ensure that the two feedback paths experience matching parasitic capacitive coupling to ground. This requirement is expanded upon in Secs. V and VI.

As the positive feedback stage is unity gain, decompensated op-amps may not be used. However, if both decompensated and compensated versions of an op-amp are available, for example, LTC6268-10 and LTC6268, then the former may be used for the TIA and the latter the following unity-gain stage. Here, the 350 MHz, unity-gain, bandwidth of the LTC6268 ensures a sufficiently flat output over the <10 MHz bandwidth required. An alternative would be the AD8057 with its large −0.1 dB bandwidth of 28 MHz.

A schematic of the circuit is detailed in Fig. 4. For this circuit, Eq. (1) can be rewritten as

$$C1 + C5 + \left(G_f \times \langle C4 + C7\rangle\right) > \sqrt{\frac{C_{IN}}{2\pi \times GBWP} \times \left[\frac{1}{R1} + \frac{G_f}{R4}\right]}, \quad (2)$$

where G_f is the gain of the following voltage-amplifier at frequency f and $R1 < R4/G_f$. The circuit operation is straightforward. The gain of the following-voltage amplifier is adjusted by varying R2 to minimize the magnitude of $C1 + C5 + \left(G_f \times \langle C4 + C7\rangle\right)$ to the limit given by Eq. (2). Provided Eq. (2) is satisfied, the transimpedance gain, G, of the circuit may usefully be expressed as

$$G = -\frac{1}{\left[\frac{1}{R1} + \frac{G_f}{R4}\right] + \omega\left[C1 + C5 + \left(G_f \times \langle C4 + C7\rangle\right)\right]}, \quad (3)$$

where $\omega = 2\pi f$. Note that the following voltage amplifier is also inverting, hence has negative gain. In addition, the resistive value of R4 could essentially be made infinite. The positive feedback would then be purely capacitive in nature and add negligible additional noise to the circuit. Finally, as there will be a small propagation delay and hence phase shift of the positive feedback signal compared with that of the negative feedback signal, the magnitude of C2 or C3 may be adjusted to better match the two feedback signal phases at increased frequencies where this becomes problematic.

Without positive feedback, a simulated bandwidth of 550 Hz is obtained (see Fig. 5). Conversely, with positive feedback and the initial values displayed in Fig. 4, the bandwidth extends out to 500 kHz.

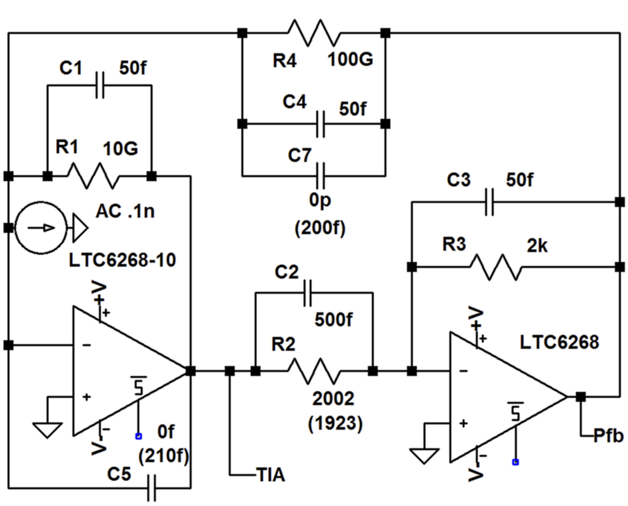

FIG. 4. Schematic of the positive-feedback circuit; for values in parentheses, see the text.

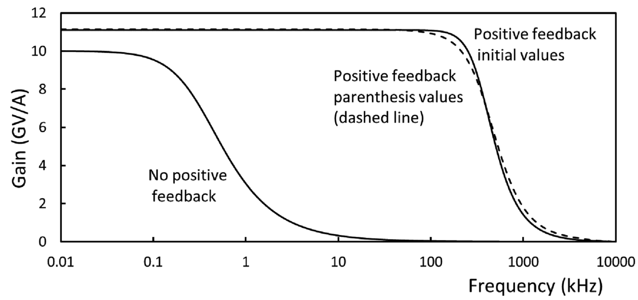

FIG. 5. Bandwidth as a function of frequency; for component values, see Fig. 4.

The onset of gain peaking is just present, indicated by the contracted gain roll-off.

Note that the gain is increased to 11.1 GV/A as dictated by Eq. (3). This increases the floor noise-density from 13 $\mu V\sqrt{Hz}$ with no positive feedback to 15 $\mu V/\sqrt{Hz}$ for both sets of positive feedback circuit values. Higher values of R4, if available, would reduce this. Alternatively, R1 may be reduced to compensate. Equation (2) indicates that the circuit is able to provide compensation not only for the parasitic capacitance of the negative feedback resistor but also for additional stray capacitance across the input/output pins of the TIA. Replacing the initial values shown in Fig. 4 with those in parentheses still realizes a simulated bandwidth of 500 kHz. Note that the large value of added parasitic capacitance (C5) across the input and output pins of the TIA is 210 fF and is not required to be equal (C7 = 200 fF) to that added across R4.

V. POSITIVE FEEDBACK CIRCUIT LAYOUT

The complete transimpedance amplifier circuit, designed and laid-out in Eagle software, is displayed in Fig. 6(a) with the schematic and component values used in Fig. 6(b). Relevant dimensions are given to enable the circuit layout to be reproduced. Eagle files are available on request.

Resistor R(input) provides a means to stabilize the circuit at high bandwidth,[1] typical values range from 10 Ω to 1 kΩ. R1A and R1B are the TIA negative feedback resistors and match the positive feedback resistors R4A and R4B in pad and package. The resistors R2A and R2B are the input resistors to the following voltage unity-gain stage. Typically, R2A is 2 kΩ with R2B enabling small values to be added. The resistors R5A and R5B allow additional small value capacitance (~50 fF) to be added to the input in the form of 50 GΩ resistors or higher value capacitors. Resistors R3A and R3B provide unity gain feedback (typically 2 kΩ and 1 Ω, or two 1 kΩ). Resistor R6 can provide a low impedance (~1 to 10 kΩ, <0.1 pF) to ground at the unity-gain output to reduce noise pickup and gain at higher frequencies. Likewise, the addition of capacitance C1 would reduce gain at higher frequencies and provide gain peaking. The ground-plane was removed from the high value feedback paths to moderate the effect of capacitive coupling to ground; this is expanded upon in Sec. VI.

The circuit layout of the positive and negative feedback paths to the TIA input, detailed in Fig. 6(a), should be as identical as possible. This is important to ensure that capacitive coupling to ground in the negative feedback arm is faithfully replicated in the positive

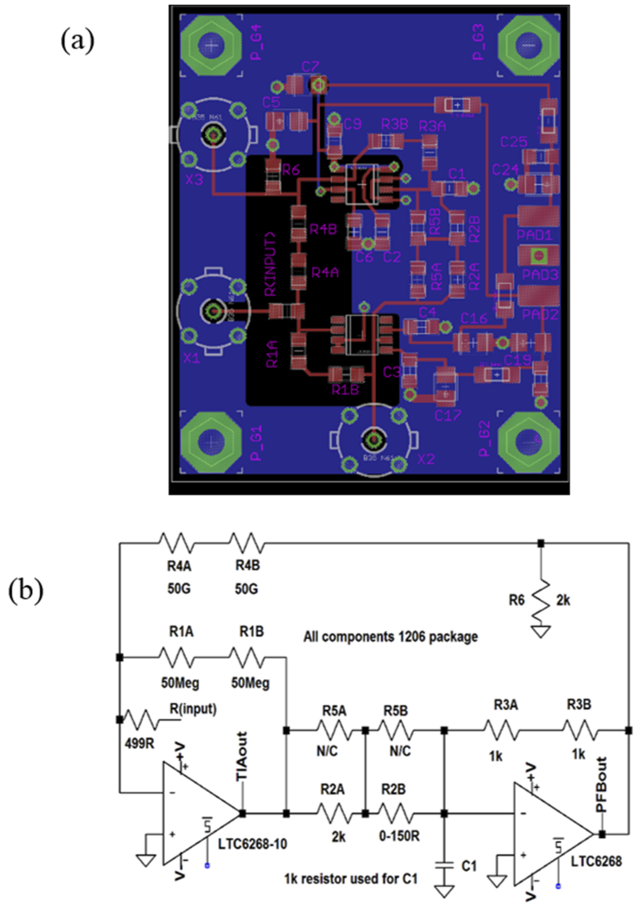

FIG. 6. (a) Printed circuit board (PCB) layout of TIA incorporating positive feedback. Dimension is 50 by 60 mm, feedback resistor package is R-US_R1206, and the wire width is 0.4064 mm. Mean separation of the ground plane from feedback wire is 6.5 mm. (b) Schematic of the PCB layout with component values used. Bypass capacitors (not shown) are 100 nF ceramic and 2.2 μF electrolytic.

one. If this is achieved, then the equivalent transfer functions of the two arms, *no matter how complex*, will cancel at the input to the TIA. For example, the negative arm of the simple circuit in Fig. 4 may be considered as a pure 11.1 GΩ resistor in parallel with a real 100 GΩ resistor exhibiting parasitic capacitance of 50 fF. The transfer functions of the two 100 GΩ resistors with 50 fF parasitic capacitance cancel at the input to the TIA, leaving only the transfer function of the negative feedback 11.1 GΩ pure resistor.

VI. TIA BANDWIDTH ENHANCEMENT RESULTS

Characterization of the circuit bandwidth utilized a 2 mV pk/pk voltage signal terminated with 50 Ω and fed through a 100 kΩ resistor. This arrangement was mounted in air and connected directly to the circuit with no intervening coax cable. See Ref. 1 for more information. As signals extend out to 5 MHz, signal amplitudes were corrected to account for the parasitic capacitance (~50 fF) across the 100 kΩ resistor. The correction signal was obtained by substituting a 50 GΩ resistor for the 100 kΩ resistor. A 100 MΩ total negative feedback resistance is chosen such that the 100 GΩ total positive feedback resistance will add negligible additional noise to the circuit. Figure 7 displays the bandwidth results for a single negative-feedback resistor of 100 MΩ. With no positive feedback (voltage op-amp unpopulated), the bandwidth is 14 kHz. Applying positive feedback gives a smooth progression to higher bandwidths with decreasing values of R2B. At small values of R2B (<20 Ω), the circuit becomes progressively more unstable with the onset of gain peaking; however, this instability may be partially countered by increasing the value of R1. For all results presented here, R1 was kept at a value of 499 Ω. It needs to be stated here that circuit instability is not a consequence of employing positive feedback to extend the gain of the TIA. Rather, it is the ability of positive feedback to extend the gain sufficiently that this occurs.

With positive feedback present, the very slow gain roll-off with increasing frequency indicates the gain limitations of these devices employing such large feedback resistances, compared with their spice model predictions. This gain roll-off is due to parasitic capacitances within the op-amp circuitry itself, limiting the gain at higher frequencies. The use of a low-pass filter to match-out the parasitic capacitance of the feedback resistor both masks and, to a degree, compensates for this. Here, overcompensation of the feedback capacitance to achieve a flat gain response increases the circuit gain at higher frequencies and unwittingly compensates for the amplifier gain roll-off. However, the inability of the low-pass filter to compensate for the parasitic capacitance present directly across the input/output pins of the TIA limits the bandwidth where this is required. One possible alternative cause of this slow gain roll-off would be a non-flat response from the following voltage stage. To examine this, the data points for no positive feedback in Fig. 7 are fitted using LTspice to the single feedback resistor circuit shown in Fig. 1. Here, a parasitic feedback capacitance of 200 fF gives a good fit. Fitting two points of the R2B = 25 Ω (Fig. 7) gain curve at 30 kHz (85 MV/A) and 300 kHz (43 MV/A) would require parasitic capacitances of 32 and 12 fF, respectively. As the capacitance compensation is proportional to voltage, this would imply a voltage difference of 11% between the two points. We examined the response of the

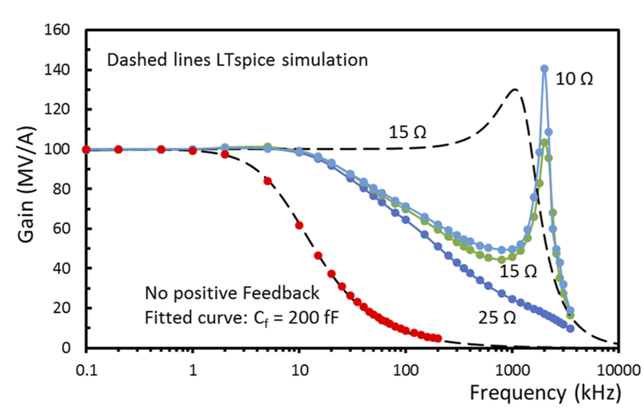

FIG. 7. Single resistor feedback (R1B and R4B 0 Ω) gain curves for no positive feedback and with positive feedback for three values of resistor R2B; for all other values, see Fig. 6(b).

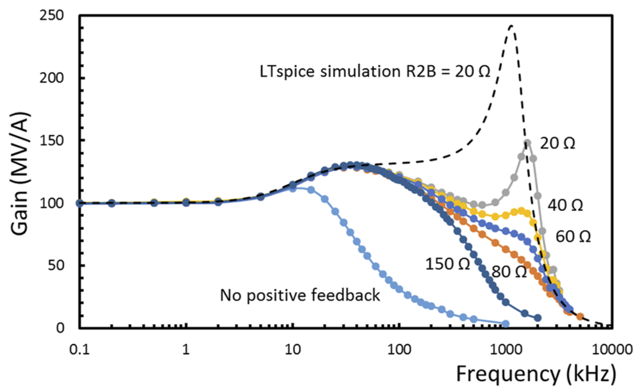

FIG. 8. Two resistor feedback and gain curves for no positive feedback and with positive feedback for various values of resistor R2B; for all other values, see Fig. 6(b).

following voltage stage (1 V pk/pk) that yielded a variation of much less than 1% between these two points.

This gain roll-off could be countered by additional amplifier stages within the feedback loops to increase the open-loop gain, detailed in Sec. II. Here, as a proof of principle, a different approach is used. Capacitive coupling to ground to provide a low-pass filter is used to increase the gain at higher frequencies, achieved by the use of two resistors in each feedback loop. In Fig. 6(a), the distancing of the ground plane from the connected pads of R2A to R2B and R4A to R4B and their pad dimensions creates this capacitive coupling to ground. This is grossly modeled, in Figs. 8 and 9 (by a best fit between measured frequency response and simulation), as a 0.35 pF capacitance to ground at the junction of the two feedback resistors. Contrary to published statements within Ref. 5, capacitive coupling to ground along the resistor feedback elements is not always disruptive or difficult to simulate.[1] Here, it is usefully employed to add a small capacitance that would be difficult with discrete components. To reduce the magnitude of this capacitive coupling, the pad dimensions may be reduced or the distance to the ground plane increased. In Fig. 8 with capacitive coupling present, the bandwidth with no positive feedback is increased from 14 to 60 kHz, with a slow-rising peak present, indicating capacitive coupling to ground at both the

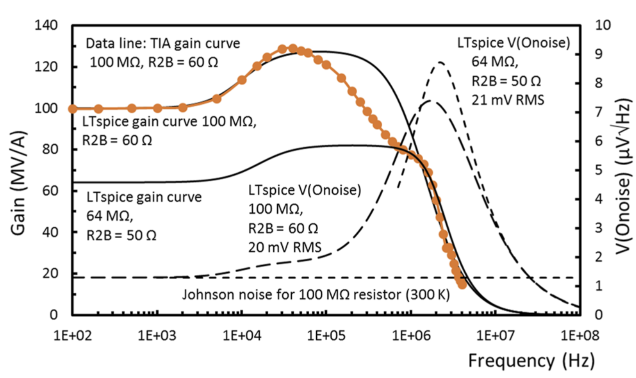

FIG. 9. Amplifier gain curve and LTspice fitted gain and V(Onoise) curves.

junction of the two feedback resistors and to a very much lesser extent the body of the two resistors.[1] Positive feedback extends the bandwidth out to a maximum of 2.6 MHz, with a smooth progression to higher bandwidths with decreasing values of resistor R2B. Note that the gain curve is not flat, with the peak occurring at 40 kHz. This can be modified by changing the ratio of the two resistor values or further finessed by adding more resistors within the feedback loops and using additional discrete small value capacitors to flatten the curve. However, a better solution is to increase the open loop gain of the feedback loops. Both these solutions are expanded upon in the discussion. The achievable bandwidth is ultimately limited by the onset of gain peaking, a consequence of Eq. (2). The gain bandwidth limit (F_{-3dB}) may be derived from Eq. (2) as

$$F_{-3dB} < \sqrt{\frac{GBWP}{2\pi \times R_f \times C_{IN}}}. \tag{4}$$

For a total value of 1.1 pF for C_{IN}, due to the input pads of R(input), R1A and R4A [Fig. 6(b)], and the differential and common input capacitance of the LTC6268-10 op-amp, a bandwidth limit of 2.4 MHz is obtained, which is in good agreement with the results presented in Fig. 8.

Finally, it should be noted that the positive arm now not only employs two 50 GΩ resistors but also adds capacitance to ground. In comparison, careful measures were necessary in Ref. 5 to shield the 10 GΩ feedback resistor from ground. The transfer function of the distributed capacitance to ground along the resistor body is comprised of an infinite number of poles. This cannot be fully compensated for by the low-pass filter and would limit the obtainable bandwidth.

VII. NOISE ANALYSIS

To assess the positive feedback circuit TIA, the value of R2B is set at 60 Ω to limit gain peaking. This reduces the bandwidth to 2 MHz. The gain curve is displayed in Fig. 9 with the best fit LTspice gain curves and associated V(Onoise).

Here, V(Onoise) is chosen in preference to I(noise) to display the noise peaking present when the bandwidth is extended close to the limit of gain peaking. Both gain peaking and noise peaking are not a direct consequence of employing positive feedback to extend the gain of the TIA. Rather, it is the ability of positive feedback to extend the gain sufficiently that these conditions occur. The V(Onoise) curve will both slightly under-represent the peak noise signal and over-represent its width. This can be checked by adjusting R2B to 50 Ω and R1A and R1B to 32 MΩ in simulation. Here, the LTspice gain curve fits the gain peak evident in the data, while the rms noise only increases slightly to 21 ms, as the majority of the noise signal is generated in the noise peak. The output noise signal of the TIA is displayed in Fig. 10. Here, the TIA is placed within a Faraday cage, the 100 kΩ resistor at the TIA input removed, and the input left open. The rms noise of 20 mV is in agreement with the LTspice analysis.

In Fig. 11, the V(Onoise) is plotted for the TIA. At lower frequencies, the noise signal is larger than expected. This has previously been attributed to capacitive coupling of voltage noise at the source terminals of the input FETs to their gates.[3] This additional noise

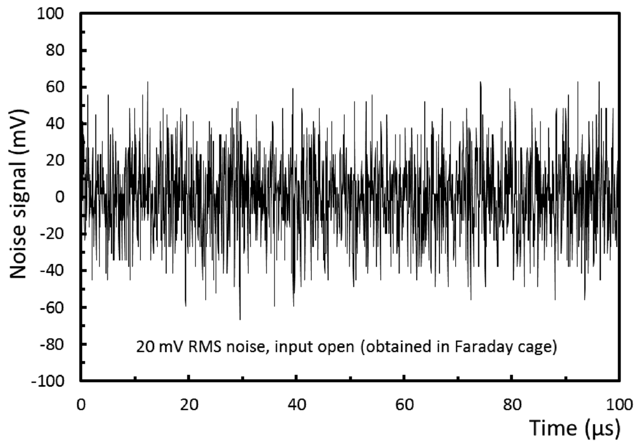

FIG. 10. TIA noise signal with time.

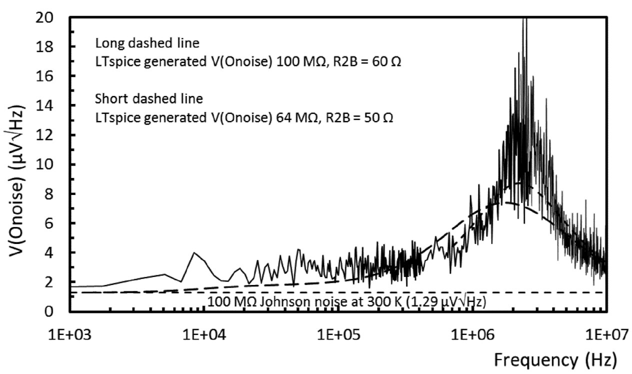

FIG. 11. TIA V(Onoise) profile with 100 kΩ resistor removed and input open.

source is similar to that of an added input capacitance, with the consequence that, at low values of input capacitance, noise signals will be greater than their spice simulations suggest. Clearly visible at higher frequency is the peak in the noise signal due to gain peaking.

VIII. DISCUSSION

For comparison, we have examined the use of a low-pass filter network to extend the gain of TIAs. In Fig. 12, results are presented for a three-resistor negative-feedback network mounted in air (see the inset). The TIA input pin is raised off the board with capacitance to ground provided by discrete, <10 pF, surface mount capacitors soldered vertically to ground and connected to the resistor-end solder-pads via 0.2 mm diameter wire. The feedback resistors used were the larger package 2010. This minimized both the parasitic capacitance due to package (~30 fF in air) and any additional parasitic capacitance connecting the discrete capacitors to the feedback resistors.

With no capacitance added to ground, curve (1) Fig. 12, the bandwidth is 70 kHz and comparable to that obtained in Fig. 8 with no positive feedback. Adding combinations of capacitance to ground does not simply extend the gain bandwidth at 100 MV/A as

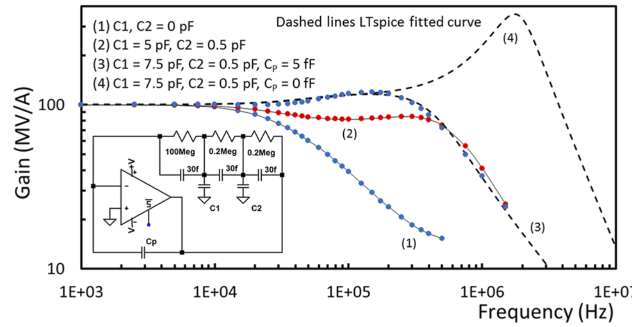

FIG. 12. TIA gain curves for a three-resistor feedback network (inset).

would occur by reducing the parasitic capacitance across the feedback resistor, were that possible. Rather, in addition, it can increase the gain at higher frequencies, as capacitors C1 and C2 short both the feedback resistors and their parasitic capacitances. This is most evident in the difference between curve (2) and curve (3) of Fig. 12. Both curves exhibit the same final bandwidth roll-off (limited by C_p); however, added capacitance in curve (2) is too little to lift the gain sufficiently, while in curve (3), it is too much. The ability of the low-pass filter to lift the gain at higher frequencies coupled with its inability to match out parasitic capacitance present directly across the input/output pins of the TIA ensures that the gain-bandwidth limitation of op-amps at such high transimpedances (due to internal parasitic capacitances) is not readily observed. Note that the bandwidth achieved (750 kHz) is much less than that achieved in Fig. 8. Gain peaking due to Eq. (1) is absent; no combination of the low-pass filter network extended the gain sufficiently. Modeling this circuit in LTspice suggests this can be attributed to an approximate 5 fF parasitic capacitance (C_p) present directly across the input and output pins of the TIA due to lead connections. Reducing the value of C_p to zero extends the simulated bandwidth, curve (4), out to 5 MHz, which exhibits significant gain peaking. In Fig. 13, a THz antenna is connected to the input of the TIA via ~5 cm, 50 Ω, co-ax cable, adding a total of ~15 pF to ground. This reduces the bandwidth to 500 kHz and the initial onset of gain peaking is just present, indicated by both the contracted gain roll-off and the small peak produced at the tail. Here, effort was made to produce a flat gain profile

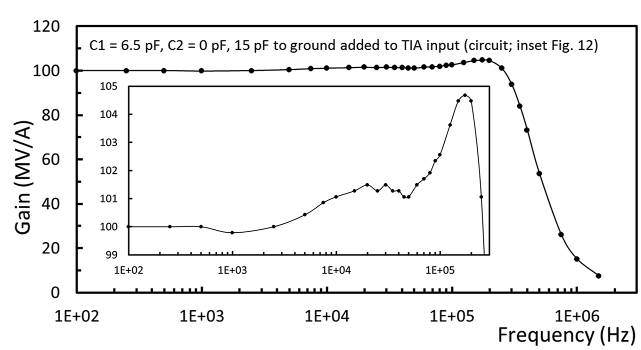

FIG. 13. TIA gain profile flatness for the three-resistor feedback network; the inset shows the restricted Y-axis.

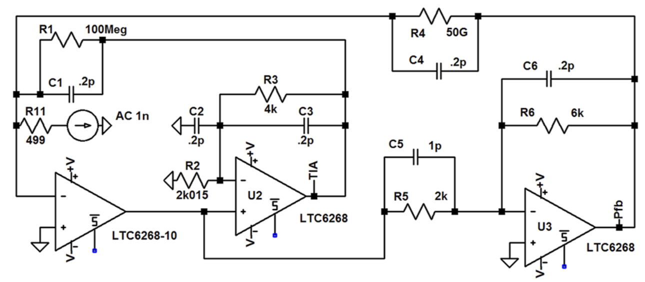

FIG. 14. Positive feedback circuit employing additional gain within the feedback loops.

by adjusting the added capacitances C1 and C2, achieving a profile flatness of better than 2% (1 V pk/pk output) until the onset of gain peaking at the tail (see the inset in Fig. 13).

The use of positive feedback can extend the bandwidth of a TIA out to the limit of gain peaking. In so doing, it exposes a very slow gain roll-off that is evident in the results presented in Fig. 7. The origin of this loss of gain at increased frequency is parasitic capacitance within the internal circuitry of the op-amp itself, the operation of which will have been optimized for known external component parameters (in particular, their parasitic capacitance) and not designed for such large transimpedances at extended bandwidths. This slow gain roll-off is countered here by the inclusion of a low-pass filter that is able to lift the gain at higher frequencies. However, the −3 dB point of the upper gain curve (R2B = 10 Ω) presented in Fig. 7 is 1 MHz. Consequently, the GBWP of the circuit need only increase by a factor of three to extend the bandwidth back out to 2.6 MHz. This invites the consideration of the alternative solution of adding a non-inverting amplifier to the negative feedback arm and increasing the open-loop gain of the positive feedback amplifier to match, as outlined in Fig. 14. The advantage of this circuit is an assured flat gain profile as the closed loop gain is dominated by the 100 MΩ resistor (R1 $\ll$ R4, Fig. 14).

The low additional gain required for the following stages allows a large GBWP margin between the TIA and that of the voltage amplifiers, ensuring circuit stability.[10] The two following voltage amplifiers may operate in parallel with equal gain, as depicted in Fig. 14, countering a potential phase shift or in series with a final positive feedback amplifier of unity gain. The final advantage is the shift in the onset of gain peaking to higher frequencies due to the larger GBWP term in Eq. (2). This permits a higher obtainable bandwidth.

IX. CONCLUSIONS

The use of positive feedback, in addition to a low pass filter, is able to extend the bandwidth of a TIA out to the limit of gain peaking. Components may be mounted directly on the circuit board with standard pad dimensions. There is no necessity to mount components in air[11] or employ additional circuitry to counter the input/output pin capacitance and its restriction on bandwidth. Both the circuit component count and complexity are low. A significant advantage is the elimination of the potential problem of distributed capacitive coupling along the feedback resistors to ground. This can disrupt the uniformity of the feedback circuit transfer-function, restricting the attainable bandwidth. Previously, this has been achieved, at the cost of significant increased complexity, with the low-pass filter capacitor designed as a tube around the feedback resistor to shield it from ground. The use of positive feedback eliminates this necessity.

ACKNOWLEDGMENTS

This work was supported by the National Natural Science Foundation of China (Grant No. 61575131).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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