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Numerical simulation of CdSe/ZnTe thin film solar cells by SCAPS-1D: Optimization of absorber layer thickness

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ABSTRACT

The numerical simulation is a crucial approach for optimization of different architectures of solar cells. Currently, there is an explicit demand of device design and numerical simulation associated to the thin film solar cells. In order to taper the scope and bridge this research gap, the optimization of absorber layer thickness is undertaken employing SCAPS-1D software. Herein, device designing and numerical simulation to the CdSe/ZnTe based hetero-junction solar cell bearing device architecture of glass/FTO/ZnTe/CdSe/Ag is undertaken. The thickness of CdSe absorber layer is varied from 1 μm to 5 μm with an interval of unity. The findings revealed that better performance comprising V_{oc} of 698 mV, J_{sc} of 3.0689 mA/cm^2, FF of 82.76% and power conversion efficiency of 1.79% is predicted for absorber layer thickness of 5 μm. The quantum efficiency of more than 60% is observed in lower wavelength region for devices having higher absorber thickness. It could be believed that present concise study on CdSe/ZnTe hetero-junction solar cells would provide novel road map and withdraw the attention of researchers for development of facile devices.

1. Introduction

In the era of cutting edge technology, the demand of energy is rising in rapid manner due to large increment in population, huge development of industries and massive use of digital materials while exploit of conventional energy sources like fossil fuels led to impact the environment in adverse nature [1]. Depleting nature of fossil fuels and release of CO_2 by these, and subsequent aroused global warming have led to furnish the critical challenge to the researchers and veterans to hunt for reliable energy alternatives those should minimize carbon footprint and can provide pollution free energy to community. Among variety of renewable energy resources, the solar energy is a dominant and reliable renewable source where effective harness of solar power and its conversion to electrical energy can tackle the global warming concerns and can certainly minimize the dependence on hydrocarbons [2]. The harness of solar energy could be done by solar photovoltaic (PV) or solar cells. Since the invention of solar cells, a variety of PV devices have been developed and categorized in three associated generations wherein Silicon wafer based solar cell devices bestow maximum power conversion efficiency (PCE) but, these are affected by pricey manufacturing equipment, need of expensive Silicon wafer, inflexibility, consumption of relatively large amount of material etc. These crucial drawbacks of champion Silicon solar cells piloted towards the development of thin film solar cell (TFSC) technologies those yielded impressive performance like appropriate PCE, environmental friendliness, cost effectiveness, facile industrial scale manufacturing etc [3].

The prime TFSCs comprise CdTe, amorphous Silicon (a-Si) and CIGS PVs wherein Cd based CdTe solar cell technology dominate since it is 30% and 40% cheaper than CIGS and a-Si technologies, respectively. The CdTe based solar cells have presented 22.1% and 18.6% laboratory and module scale efficiencies and thus have maximum efficiency to cost ratio [4]. However stagnant and saturated value of achieved PCE for a long duration and less sufficient room for further improvement led to emphasize the researchers to further explore alternative potential Cd-based absorber materials. In this line, the cadmium selenide (CdSe) is an appropriate and cheaper light absorption material alternative to CdTe since, it has higher absorption coefficient ($>10^5$ per cm), suitable electron affinity, larger photosensitivity, apt band gap of 1.74 eV. The CdSe could not only be used in single junction but in multi-junction solar cells too due to astounding band gap. Moreover, CdSe based devices could be more stable to thermal stress vis-à-vis the highly degradable perovskite solar cells [5,6]. Persistent research efforts have been carried

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out on development and characterization of CdSe films by undertaking evolutions on film thickness and substrate temperature [7–9], growth potential [10], deposition temperature, dopant nature and concentration [11,12], annealing [13,14], chloride treatment [15,16] etc for variety of applications viz. solar cells, thin film transistors, light emitting diodes etc. The electrochemical synthesis of Fe doped CdSe films is carried out by Shinde et al. [17] for solar cell applications where fabricated devices showed better open circuit voltage of 273.18 mV. Shaikh et al. [18] employed p-Cu_2Se window layer to develop the solid state solar cell devices based upon n-CdSe absorber layer where developed devices showed poor PCE of 0.67%. Ivashchenko and Opanasyuk [19] undertook simulation modeling on CdSe based absorber layer where ZnSe and ZnTe layers are employed as buffer layers. Predicted CdSe/ZnTe and CdSe/ZnSe solar cells exhibited fill factor of 71.02% and 42.34%, respectively. Hence, CdSe is a potential absorber layer material which requires extensive research on fabrication of high performance and facile CdSe based solar cells.

The exploration of physical properties and modeling of solar cell devices could be accomplished by numerical simulation which is crucial approach for interpretation of complex structures and optimization of innovative solar cell architectures. Undoubtedly simulation modeling provides the road map to anticipate an impact of layer parameters on performance of the predicted device. A variety of simulators like AMPS-1D, SCAPS-1D, SILVACO, ATLAS, COMSOL, wxAMPS are currently available for solar cells. Among these, SCAPS-1D has drawn significant attention and extensively used by researchers so far since, it allows the modeling of utmost seven layers structure [1].

In the present work, critical insights to numerical simulation of CdSe thin film solar cell is successfully presented wherein ZnTe layer is used as apt partner for formation of heterojunction. The performance of solar cells in simulation approach is governed by different physical parameters like carrier life time, film thickness, back contact barrier, defect density, carrier concentration, nature of metals for contacting, doping concentration, deep level defects in associated absorber, window and buffer layers. Thickness of absorber layer material is crucial and important parameter which affects the overall performance of solar cells. Utilization of inadequate thickness of absorber layer material could lead to huge loss in absorption of photons which eventually results into decrement in photo current density. Similarly, higher thickness of absorber layer material may result into saturated performance of device [20–22]. Optimization of absorber layer thickness would assist in reduction of material consumption and minimization in fabrication duration which eventually consequent into reduced solar cell manufacturing cost [3]. These facts draw an attention towards importance of optimization of absorber layer thickness to solar cells. Therefore in current work, an influence of absorber layer thickness on performance of CdSe/ZnTe hetero-junction solar cell is investigated employing device designing and simulation modeling. The thickness of CdSe absorber layer is varied from 1 μm to 5 μm and its impact on open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF) and power conversion efficiency (PCE) is elaborated deeply.

2. Device modeling and numerical simulation

In the present study, numerical simulation of CdSe devices is carried out by using solar cell capacitance simulator-one dimensional (SCAPS-1D) having version 3.3.0.10 which is developed by Burgelman's group with LabWindows/CVI at University of Gent. The SCAPS software is freely accessible to scientific community for research and development purposes [23–25]. Initially, this graphic simulator is developed for CIGS and CdTe multilayer solar cells and presently, it is configured for most of the solar cell device designing. The SCAPS-1D can provide numerical measurements like current density-voltage (J-V), capacitance voltage (C–V), capacitance frequency (C-f), spectral response (Q(λ)), electric field, band diagram and band structure, carrier densities, recombination profile, carrier transport phenomenon etc. Herein, the algorithm behind numerical simulation of designed solar cells is based upon Poisson's equation as well as electron and hole continuity equations [1,25] which are given as under:

Poisson's equation

$$\frac{\partial}{\partial x}\left(-\varepsilon(x)\frac{\partial V}{\partial x}\right)=q\left[p(x)+N_D^{+}+p_t(x)-n(x)-N_A^{-}-n_t(x)\right]$$

Electron continuity equation

$$\frac{\partial n}{\partial x}=\frac{1}{q}\frac{\partial J_n}{\partial x}+G_n-R_n$$

Hole continuity equation

$$\frac{\partial p}{\partial x}=-\frac{1}{q}\frac{\partial J_p}{\partial x}+G_p-R_p$$

Where ε, q *and* V stand for dielectric permittivity, charge and potential, respectively. The $p(x)$, N_D^{+}, $p_t(x)$ represent free hole concentration, ionized donor concentration and hole trap density, respectively whereas $n(x)$, N_A^{-}, $n_t(x)$ correspond to free electron concentration, ionized acceptor concentration and electron trap density. The J_n and J_p denote the current density of electrons and holes, respectively. The G_n and G_p are generation rates for electrons and holes whereas recombination rates of holes and electrons are represented by R_p and $R_{n,\ respectively}$

In this research work, device architecture glass/FTO/ZnTe/CdSe/Ag to thin film solar cell is designed by employing SCAPS software. The fluorine doped tin oxide (FTO) having high transparency is used as transparent conducting oxide (TCO) layer. The thickness to the constituent layers and associated contacts are undertaken on the basis of experimental validation to be undertaken in due course of time. In order to transmit the maximum incident solar irradiance at the associated absorber, rest of the layers should be as thin as possible and accordingly, the optical window thickness is undertaken 100 nm typically similar to that of the CdS layer employed so far in second generation based TFSCs. It has been strongly considered that the designed device should efficiently capture incident irradiance, generate charge carriers and collection of these at the associated electrodes when experimental validation is undertaken. Accordingly, thickness of TCO layer is taken as 50 nm [3] and it is attached to a flat band contact. The p-type ZnTe layer is used as an optical window which establishes asymmetric hetero-junction with absorber layer. Thickness of optical window is taken to 100 nm in predicted device in view of available associated literature for window layer [1,20,22] as stated. The n-CdSe material is used as an absorber layer whose thickness is varied from 1 μm to 5 μm. Lastly device structure is completed by inserting Ag metal contact layer [26,27] whose work function is 4.74 eV [28]. In this study, different parameters of constituent layers for simulation purposes have been chosen from literature [3,29,30] whereas some parameters are estimated within the allowed range in view of theoretical aspects. Since during the synthesis of CdSe and ZnTe layers and fabrication of realistic solar cell, donor and acceptor like defects may be originated in these layers. Typically during the growth of CdSe films, higher Se vacancies (V_{Se}^{2+}) are introduced which are positively charged defects and such defects are recognized as donor defects [31]. Hence during the simulation of targeted device, donor defects with lower density of 10^{14} cm^{-3} are introduced in CdSe absorber layer. In analogy with this fact and knowing that ZnTe is typically having Zn vacancies, those are negatively charged defects and thus, acceptor defects are introduced in ZnTe layer [32]. Hence, acceptor defects with lower density of 10^{14} cm^{-3} are introduced in window/buffer layer during simulation. The surface recombination velocity for electrons and holes at front contact is set to 1

$\times$ 10^7 cm/s and 1 $\times$ 10^5 cm/s, respectively whereas at back contact, these are taken as 1 $\times$ 10^5 cm/s and 1 $\times$ 10^7 cm/s. These physical parameters of different layers are listed in Table 1. The device designing is undertaken at 300 K with AM 1.5 global irradiance spectra having illumination of 100 mW/cm^2 where light is entered from FTO coated glass side. The device architecture of complete CdSe/ZnTe hetero-junction solar cell is shown in Fig. 1 (a). The energy band alignment via position of valence band maxima (VBM) and conduction band minima (CBM) of different constituent layers is depicted in Fig. 1 (b) whereas band bending diagram of predicted device having 1 μm thin absorber layer is shown in Fig. 1(c). The conduction band offset (CBO) between CdSe and ZnTe layers is determined using electron affinities and it is observed as 1.09 eV. Positive value of CBO indicates formation of spike/step like structure in bend bending diagram as described elsewhere [33]. It has been reported that such kind of structure is observed to be found more favorable for higher performance of devices [33]. Estimated value of CBO possibly prevents the movement of electrons towards ZnTe and hence, electrons are collected at back (Ag) electrode. The valence band offset (VBO) between these layers is observed as 0.59 eV and it allows facile transportation of holes towards ZnTe and these holes are finally collected at front contact. Lower value of VBO possibly contributes into higher V_{oc} of simulated CdSe based solar cells as given in Table 2 [34].

3. Results and discussion

The influence of absorber layer thickness on J-V characteristics of simulated devices is presented in Fig. 2 wherein almost square J-V curves are obtained which may indicate prediction of suitable device design. The overlapping current density is seen up to 0.45 V for all the devices and inset shows this portion on modified scale which indicates that slight increment in current density is observed with absorber thickness. In J-V characteristics, no roll-over phenomenon is observed which could be arisen due to back contact barrier and it is commonly appeared in characteristics of developed devices [35].

In order to explore the impact of absorber layer thickness on performance of predicted devices, the open circuit voltage (V_{oc}), short circuit current density (J_{sc}), fill factor (FF) and power conversion efficiency (PCE) are computed.

Table 1
Various physical parameters associated to FTO, ZnTe and CdSe materials employed during simulation.

Parameters	FTO [3]	ZnTe [30]	CdSe [29]
Thickness (μm)	0.05	0.10	1–5
Band gap (eV)	3.6	2.26	1.74
Electron affinity (eV)	4	3.65	4.74
Dielectric permittivity (relative)	9	14	10.6
CB density of states (1/cm^3)	2.1 $\times$ 10^{18}	7.5 $\times$ 10^{17}	2.2 $\times$ 10^{18}
VB density of states (1/cm^3)	1.9 $\times$ 10^{19}	1.5 $\times$ 10^{19}	1.8 $\times$ 10^{19}
Electron mobility (cm^2/Vs)	100	70	100
Hole mobility (cm^2/Vs)	25	50	25
Shallow uniform donor density N_D (1/cm^3)	1.10 $\times$ 10^{18}	0	1.10 $\times$ 10^{10}
Shallow uniform acceptor density N_A (1/cm^3)	0	1 $\times$ 10^{12}	0
Electron thermal velocity (cm/s)	1 $\times$ 10^7	1 $\times$ 10^7	1 $\times$ 10^7
Hole thermal velocity (cm/s)	1 $\times$ 10^7	1 $\times$ 10^7	1 $\times$ 10^7
Defect density N_t (1/cm^3)	–	10^{14}	10^{14}
Reference for defect level Et	–	Above EV	Above EV
Energy corresponding to reference (eV)	–	0.60	0.60

Surface recombination velocity	At front contact	At back contact
For electrons (cm/s)	1 $\times$ 10^7	1 $\times$ 10^5
For holes (cm/s)	1 $\times$ 10^5	1 $\times$ 10^7

The open circuit voltage is the potential developed across the electrodes of solar cell devices when an external load is absent, indeed, it represents the maximum voltage which could be extracted from the device. As per Fig. 3(a), the simulated devices having CdSe absorber layer thickness of 1 μm, 2 μm, 3 μm, 4 μm and 5 μm exhibited V_{oc} of 657 mV, 674 mV, 685 mV, 691 mV and 698 mV, respectively. Thus, V_{oc} is found to enhance with increment in CdSe absorber thickness. Generally, the recombination rate of charge carriers before their collection is very high at lower absorber thickness. Therefore, enhanced thickness of CdSe absorber suppressed the recombination phenomenon and led to the increased V_{oc} [4]. The improvement in built-in-potential along with lesser defects could also be considered as responsible factors for enhancement in V_{oc} with thickness [36,37]. A variety of CdSe sensitized solar cells have been developed by Hossain et al. [38] where V_{oc} of devices is ranged between 535 mV and 600 mV.

The short circuit current represents the quantity of current which can flow in circuit when voltage across solar cell device is zero or the current obtained under the condition of short circuiting of electrodes. It is maximum current that could be extracted from a solar cell device. The short circuit current density (J_{sc}) and open circuit voltage could be correlated by following relation [21,33]:

$$V_{OC} = \frac{k_B T}{q} \ln\left[\frac{J_{SC}}{J_0} + 1\right]$$

Where q, k_B, T and J_0 are charge, Boltzmann constant, operating temperature and reverse saturation current respectively. The short circuit current density of simulated devices is observed as 3.067 mA/cm^2, 3.0680 mA/cm^2, 3.0683 mA/cm^2, 3.0686 mA/cm^2, 3.089 mA/cm^2 having CdSe absorber layer thickness of 1 μm, 2 μm, 3 μm, 4 μm and 5 μm, respectively as depicted in Fig. 3(b). Enhancement in J_{sc} with CdSe thickness is ascribed to the increased width of space charge region (SCR) which might also lead to modify the associated acceptor/donor concentration [39]. The photoelectrochemical solar cells having Al doped CdSe as absorber layer are developed employing chemical bath deposition technique by Gawali et al. [40] wherein devices showed short circuit current of 1.08 mA.

The fill factor of solar cell devices is expressed by the ratio of area enclosed by current and voltage at maximum power point (P_{max}) to product of J_{sc} and V_{oc}. It is the measure of squareness of J-V curve of the solar cell devices [22] and it is represented as:

$$FF = \frac{I_{max}.V_{max}}{J_{sc}.V_{oc}}$$

Where J_{max} and V_{max} denote the current and voltage at maximum power point (P_{max}) [22]. The fill factor is found as 82.27%, 82.48% 82.56%, 82.67% and 82.76% for CdSe/ZnTe hetero-junction devices having absorber thickness of 1 μm, 2 μm, 3 μm, 4 μm and 5 μm, respectively. It could be observed that FF is also improved with thickness but increment is marginal. The FF of the designed devices could be increased due to lessening in recombination of electrons and holes at rear metal contact [30]. Decline in bulk resistance, decrease in recombination and increase in built-in-potential could be regarded as possible reasons behind improvement in FF with CdSe absorber thickness [25,36,41]. On increasing the thickness to the absorber layer, the carrier lifetime may be enhanced possibly due to lesser probability of recombination of excitons which eventually leads to improve the built-in-potential, makes a movement of rear surface of device far from the depletion region and thereby improves fill factor of devices [42]. Also the reduction in series resistance along with enhancement in charge carrier concentration could also be considered as a possible cause behind the improvement of fill factor of devices with increased absorber layer thickness [43]. Zyoud et al. [44] undertook the synthesis of polycrystalline CdSe films employing electrochemical deposition and chemical bath deposition techniques for photoelectrochemical solar cell applications where

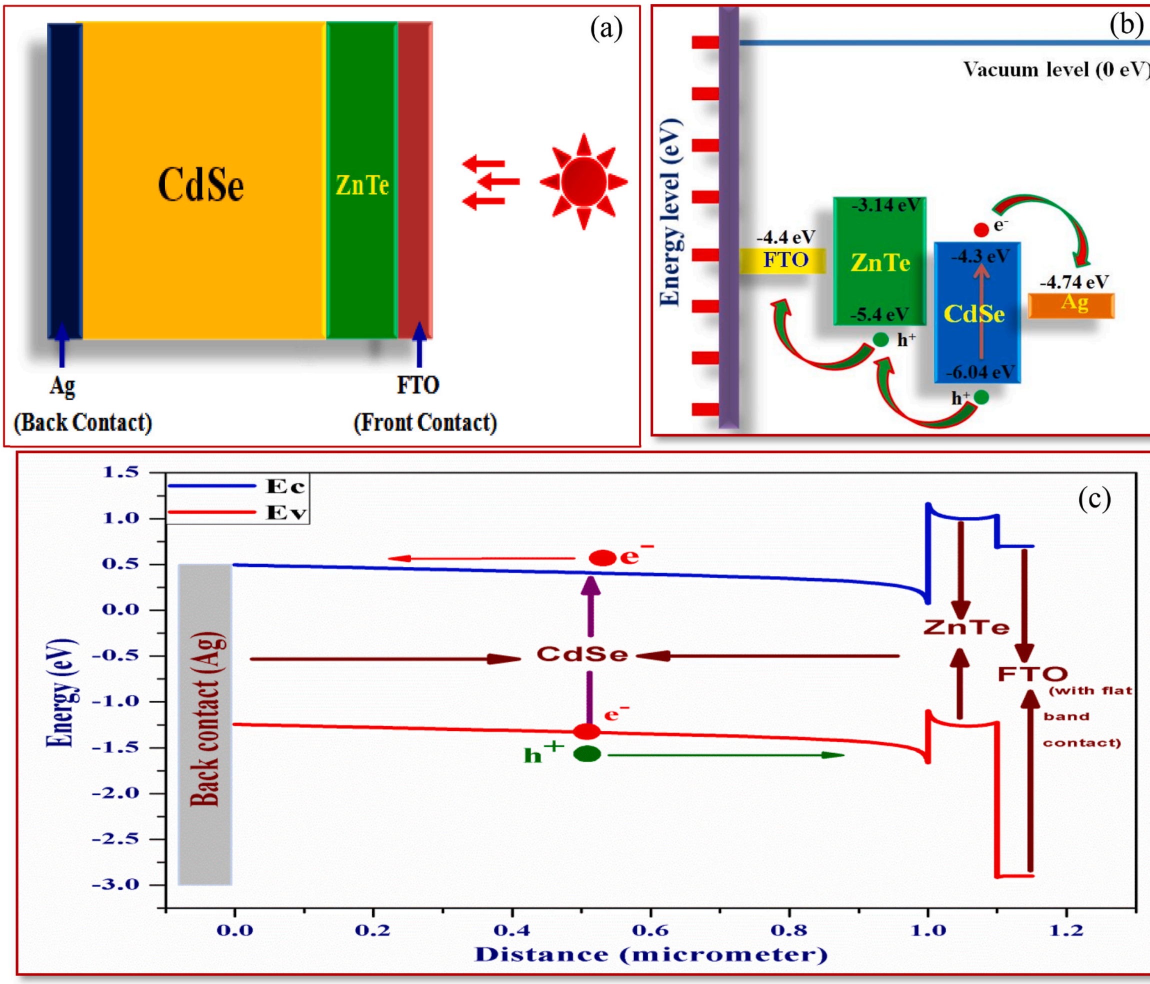

Fig. 1. (A) Device architecture, (b) energy band alignment via positions of VBM and CBM of constituent layers, and (c) band bending diagram of CdSe/ZnTe hetero-junction solar cell.

Table 2
Performance parameters of simulated devices having variable absorber layer thickness.

CdSe thickness	V_{oc}	J_{sc}	FF	PCE
1 μm	657 mV	3.067 mA/cm^2	82.27%	1.65%
2 μm	674 mV	3.0680 mA/cm^2	82.48%	1.70%
3 μm	685 mV	3.0683 mA/cm^2	82.56%	1.74%
4 μm	691 mV	3.0686 mA/cm^2	82.67%	1.77%
5 μm	698 mV	3.0689 mA/cm^2	82.76%	1.79%

developed devices exhibited better fill factor of ~74%.

The power conversion efficiency (PCE) is measure of capability of device for conversion of solar energy into electrical energy. It is defined as ratio of maximum power (P_{MAX}) delivered at operating point to the incident power density (P_{in}) and given as:

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{max}.V_{max}}{P_{in}} = \frac{J_{sc}.V_{oc}.FF}{P_{in}}$$

Where P_{in} is incident power density [22]. It primely represents the effectiveness of developed device. The PCE of simulated CdSe/ZnTe hetero-junction devices is achieved as 1.65%, 1.70%, 1.74%, 1.77% and 1.79% having CdSe absorber thickness of 1 μm, 2 μm, 3 μm, 4 μm and 5 μm, respectively. Hence, PCE of devices is found to improve with increase in thickness of absorber layer. The thicker layer ensures higher absorption of incident photons which leads to create electrons and holes

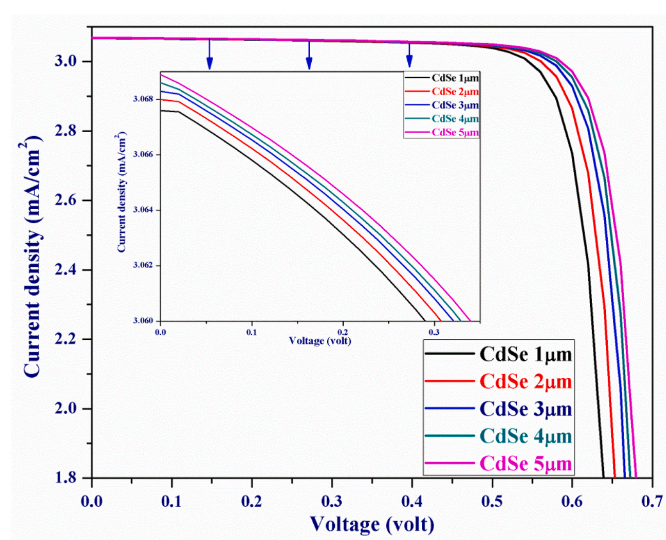

Fig. 2. J-V characteristics of simulated devices having different absorber layer thickness.

in large density those effectively contribute in associated current and power conversion efficiency [2,45–47]. An improvement in PCE of simulated devices is also reported with increase in thickness of CdTe

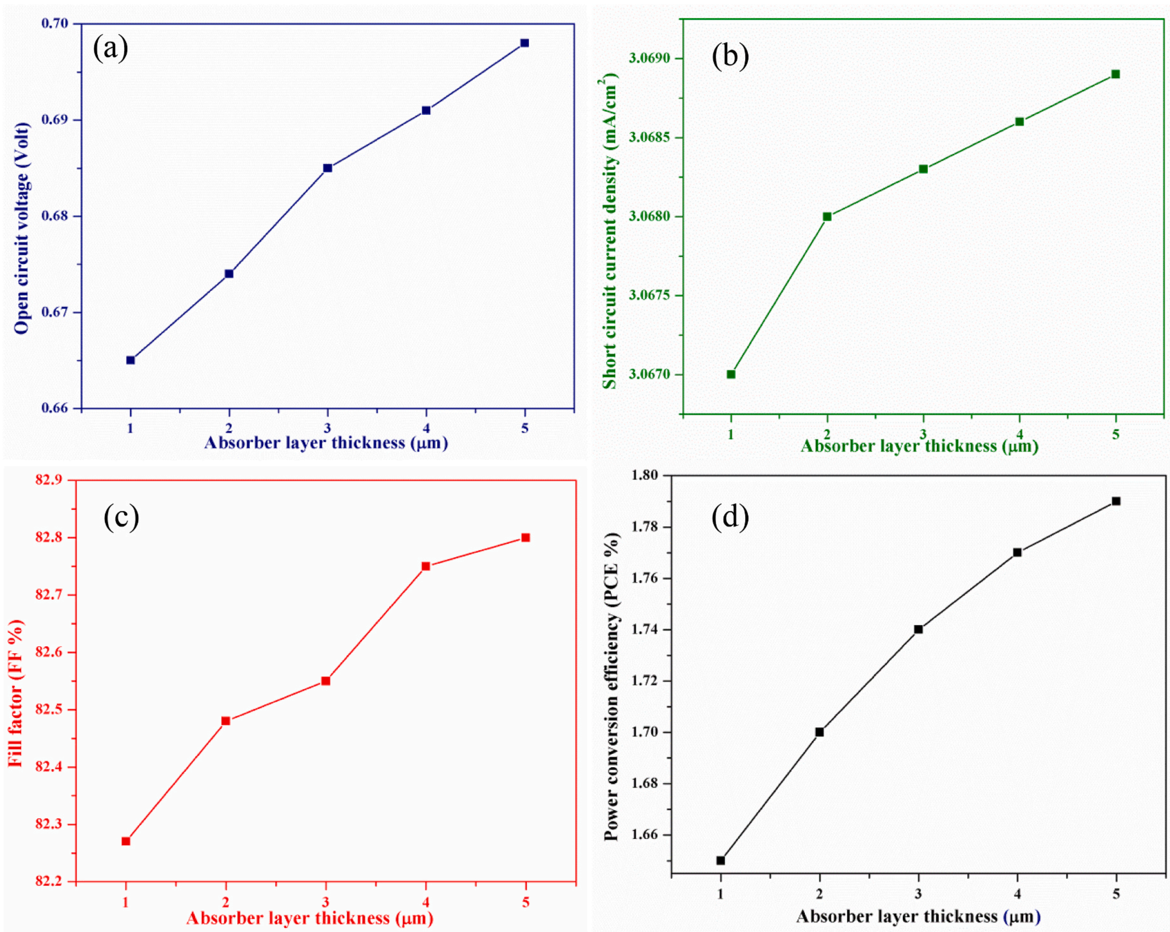

Fig. 3. Variation in (a) open circuit voltage, (b) short circuit current density, (c) fill factor and (d) power conversion efficiency of simulated devices.

absorber layer [22]. Majidi et al. [48] fabricated CdSe based planar and extremely thin absorber layer solar cells which showed power conversion efficiency of 1.03% and 1.34%, respectively. The rapid thermal evaporation of CdSe films for fabrication of FTO/ETL/CdSe/HTL/Au solar cells is undertaken by Li et al. [49] where optimized devices demonstrated PCE of 1.88%.

In view of computed values of performance parameters of the predicted CdSe/ZnTe hetero-structure solar cell devices, the better behavior is observed for devices designed with absorber layer thickness of 5 μm vis-à-vis the others. Therefore, quantum efficiency (QE) of these devices is undertaken and presented in Fig. 4.

Generally, QE represents the behavior of devices in gathering of charge carriers as a function of wavelength [22]. Maximum QE of ~64% is achieved at 300 nm wavelength and later decreased with wavelength. In lower wavelength region up to 550 nm, parasitic absorption losses are quite lower which gives rise to increase in current and eventually improvement in QE of the optimum device [3]. As per quantum efficiency curve, in shorter wavelength, most of the high energy photons incident on the device resulted in generation and collection of charge carriers in the associated absorber and electrodes, respectively to the devices. Consequently, quantum efficiency curve is started from top possibly owing to least recombination current. On increasing the wavelength i.e. in case of low energy photons, parasitic and recombination losses might be started to take place and carrier transportation might be hampered resulting in diminishing trend of quantum efficiency. Similar results are reported for CdSe [50], CZTSe [43] and CdTe [51] solar cells where behavior of quantum efficiency is started from the top. Nonetheless, the better quantum efficiency findings are acquired in the lower wavelength region might be due to the associated classical absorbtion region while for the higher wavelength poor results are obtained which invite potential to resolve the concerns as typically the quantum efficiency curve bears squared behavior for ideal one and for devloped devices, it could be near the same. Besides, thin film layers are comprised of grain boundaries those behave like recombination centers

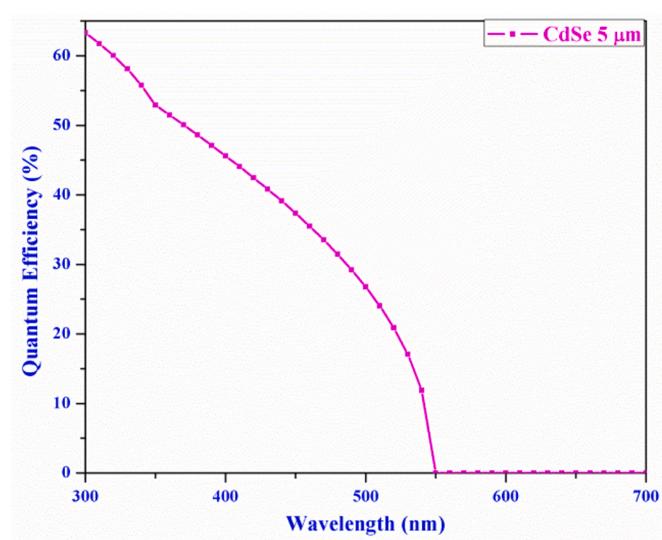

Fig. 4. Behavior of quantum efficiency with wavelength for simulated devices bearing 5 μm absorber layer thickness.

and trap states for the charge carrier and potentially impact their transportation and thus, these must also be incorporated in the associated device designing code.

4. Conclusion

In the present concise device designing work, numerical simulation of CdSe/ZnTe hetero-junction solar cell is carried out by employing SCAPS-1D software. For the simulation, devices having architecture as glass/FTO/ZnTe/CdSe/Ag are designed. In predicted device, FTO with thickness 50 nm worked as TCO whereas *p*-ZnTe with thickness of 100 nm is used as window layer which created hetero-junction with the associated absorber CdSe layer. For optimization of absorber layer thickness, CdSe layers having thickness in range of 1–5 μm are used. The performance parameters are computed by illuminating the devices using AM 1.5 global spectra at 300 K temperature. The open circuit voltage of simulated devices is enhanced from 657 mV to 696 mV with increase in CdSe thickness possibly due to improved built-in-potential. The short circuit current density of predicted devices is increased from 3.0670 mA/cm^2 to 3.0689 mA/cm^2 with enhancement in thickness of absorber owing to the improved width of SCR. Fill factor of modeled devices is found to slightly increase from 82.27% to 82.76% due to reduction in bulk resistance and recombination. The PCE of devices is increased from 1.65% to 1.79% with increase in absorber layer thickness due to the enhanced absorption of incident photons by thicker layer. The lesser parasitic losses resulted into higher quantum efficiency in lower wavelength region. The findings to designed devices suggested that higher performance of CdSe/ZnTe thin film solar cells could be achieved using 5 μm thin absorber layer. Since, the research work on simulation of CdSe solar cells is limited, therefore, it is believed that present investigation would further encourage the researchers to perform modeling on CdSe based solar cells and their subsequent fabrication for experimental validation of the theoretical predictions. The design still needs to resolve the poor findings associated to the quantum efficiency and associated code needs incorporation of the impact of grain boundaries in the employed simulation.

Credit author statement

Himanshu: Conceptualization, Investigation, Formal analysis, Writing - Original Draft. **Kamlesh**: Formal analysis, Writing - Original Draft. **D. Suthar**: Formal analysis, Writing - Original Draft. **M.S. Dhaka**: Investigation, Formal analysis, Writing - Original Draft, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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