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SiC-based high electron mobility transistor

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ABSTRACT

This paper describes the fabrication of a SiC-based high electron mobility transistor (HEMT). A single-crystal 3C–SiC layer was grown on a C-face 4H–SiC substrate, and 2D electron gas was induced at the 3C–SiC/4H–SiC heterointerface due to the unique polarization physics. The measured Hall mobility of the 2DEG was 586 $cm^2/V\,s$ at room temperature. Source, gate, and drain electrodes were fabricated on the 3C–SiC surface. The drain current for the fabricated SiC-HEMT was measured to be 47.5 mA/mm, and the transconductance was estimated to be 13.5 mS/mm.

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Carbon-face (C-face) 3C–SiC/4H–SiC heterostructures are promising for novel high electron mobility transistors (HEMTs). High-power and high-frequency amplifiers are required for many applications, such as high-power radars, broadband telecommunications, and high-resolution LiDARs. Over the past half-century, GaAs, InP, and GaN-based HEMTs have been extensively studied. C-face 3C–SiC/4H–SiC heterostructure-based HEMTs may offer comparable, or even superior, performance to conventional high-power, high-frequency devices, such as GaN-HEMTs. In addition to Johnson's figure-of-merit, the electron saturation velocity is a key material property for high-frequency devices,[1] and the saturation velocity for 3C–SiC is as high as 2.5×10^7 cm/s.[2] This value is comparable to that of GaN.[4] Recently, we also demonstrated a high 2D electron gas (2DEG) mobility of 780 $cm^2/V\,s$ for a 3C/4H–SiC heterostructure at room temperature.[3] This value is about half of that for GaN.[5] Crystal quality has been a key issue in the development of GaN-based HEMTs. In this respect, HEMTs based on 3C/4H–SiC could have an advantage because the lattice mismatch and thermal expansion mismatch at the heterostructure interface are negligibly small.[6–8] In addition, SiC exhibits superior heat dissipation properties to other materials including GaN.[9–12] This is important for HEMTs that require a high-power density. Furthermore, processes that are difficult when fabricating conventional HEMTs, such as gate oxidation and p-type ion implantation, are possible with SiC.

Despite these attractive properties, there are a few experimental studies on 3C/4H–SiC heterostructures[3,13] and no reports on the subsequent fabrication of HEMTs. In this paper, we describe the fabrication of a HEMT based on C-face 3C/4H–SiC and evaluation of its electrical properties. The heterostructure was processed to form a planar-type transistor and its DC characteristics were evaluated. Channel current modulation by a gate bias voltage was verified, which is the criterion for the fabrication of a SiC-based HEMT.

First, we describe the proposed SiC-based HEMT concept. Figure 1(a) shows a schematic illustration of the energy band structure for conventional AlGaN/GaN-based HEMTs. Due to the polarized nature of nitride semiconductors, high-density 2D electron gas (2DEG) is induced at the AlGaN/GaN heterointerface without intentional donor impurity doping in the AlGaN barrier layer.[14] The band structure for 3C–SiC/4H–SiC is shown in Fig. 1(b). Due to a similar difference in spontaneous polarization between 3C–SiC and 4H–SiC,[15] positive bound charges are formed at the 4H-SiC side of the 3C–SiC/4H–SiC heterointerface with a density of more than $1 \times 10^{13}\,cm^{-2}$. These charges cause the formation of 2DEG in 3C–SiC to achieve charge neutrality. This 2DEG is expected to have a narrower spatial distribution than that in GaN-based heterostructures, owing to stronger electron confinement caused by the large spontaneous polarization in 4H–SiC[16] and the large conduction band offset (0.93 eV) at the heterointerface,[17] compared to 0.38 eV at $Al_{0.3}GaN/GaN$ interface.[18] The 3C–SiC thickness should be several tens of nanometers, which is comparable to that for the AlGaN barrier in GaN-HEMTs, so that the 2DEG density can be modulated by a gate electrode on the 3C–SiC layer.

Device fabrication started with undoped 3C–SiC growth on a C-face 4H–SiC substrate (12×12 mm) by thermal chemical vapor deposition. This substrate was cut from a commercial 4-in. wafer and

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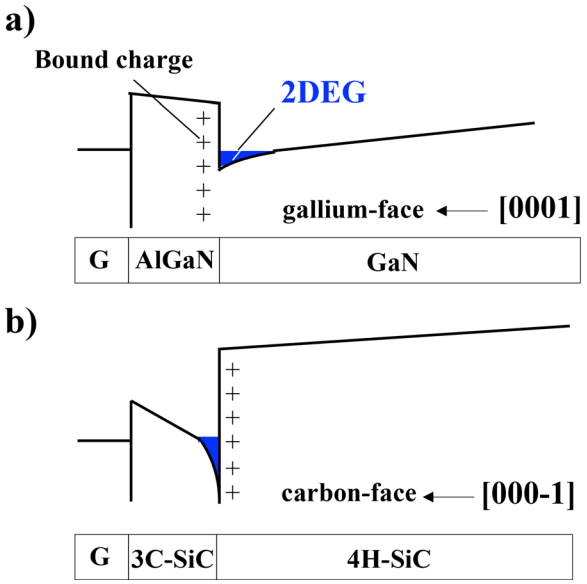

FIG. 1. Schematic band diagrams for (a) AlGaN/GaN heterostructure and (b) C-face 3C/4H–SiC heterostructure.

processed by CMP so that the off-orientation and off-angle are [1–100] and 0.14°, respectively. The resistivity specification at room temperature of the commercial wafer is greater than $1 \times 10^7\,\Omega$ cm. To obtain single-crystal 3C–SiC, a series of atomic steps was formed on the 4H–SiC substrate, each with a height of one unit cell (1*C*, 1.0 nm).[3] The thickness of the 3C–SiC layer was set to 24 nm based on the deposition time. The formation of an abrupt 3C/4H–SiC heterointerface was confirmed by cross-sectional high-resolution transmission microscopy (HR-TEM), as shown in Fig. 2. The electron mobility (μ_{Hall}) and sheet carrier density (N_s) for the heterostructure were 586 cm^2/V s and $1.48 \times 10^{13}/cm^2$, respectively, as evaluated by Hall effect measurements using the van der Pauw method at room temperature.

Figure 3(a) is a schematic cross section of a fabricated SiC-HEMT. Following cleaning of the 3C–SiC/4H–SiC chip using an RCA solution,[19] a mesa structure was formed by inductively coupled plasma etching at a depth of 200 nm. The source (S) and drain (D) electrodes were formed by depositing a Ni layer with a thickness of 50 nm and subsequent patterning using a conventional lift-off process.

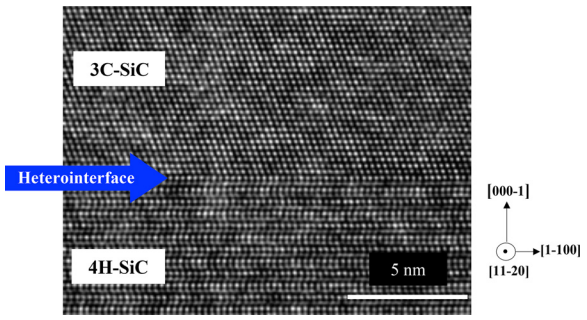

FIG. 2. Typical cross-sectional HR-TEM image of C-face 3C/4H–SiC heterostructure.

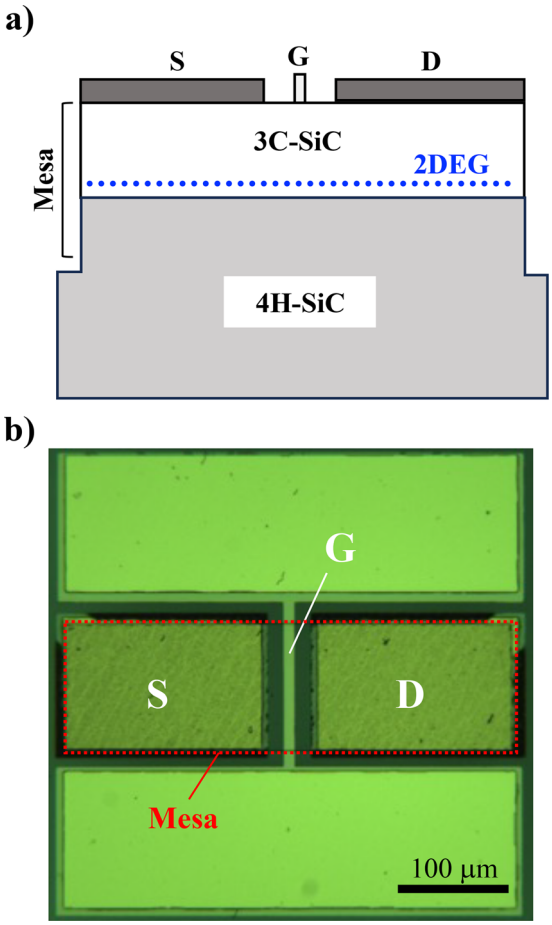

FIG. 3. Fabricated device structure: (a) schematic cross section and (b) plan-view optical micrograph.

The structure then annealed at 850 °C for 2 min in an Ar ambient to form source and drain ohmic contacts.[20] A Au layer with a thickness of 30 nm was also deposited and patterned on the 3C–SiC layer to form a Schottky gate electrode (G).[21] All metals were deposited by electron beam evaporation under a background pressure of less than 3×10^{-7} Pa. Figure 3(b) shows a plan-view optical micrograph of the fabricated device. Both the source-gate and gate-drain spacings were designed to be 15 μm. The gate length (L_g) and width (W_g) were 10 and 115 μm, respectively. The device had no contact metal on the back side, which was left electrically floated. The DC characteristics of the transistor were evaluated at room temperature using a Keysight B1500A semiconductor device parameter analyzer.

Figure 4(a) shows the measured drain current density (I_d) as a function of the drain–source voltage (V_{ds}) for gate–source voltage bias (V_{gs}) values ranging from 0 to −4 V in −1 V increments. I_d is seen to decrease as V_{gs} becomes more negative. The fact that I_d (i.e., the 2DEG density under the gate) can be modulated by the gate bias voltage indicates transistor operation. Although I_d did not reach zero due to the gate leakage current, the threshold voltage (V_{th}), extrapolated from the I_d values at V_{gs} of 0 and −3 V, was −3.8 V. Therefore, the fabricated

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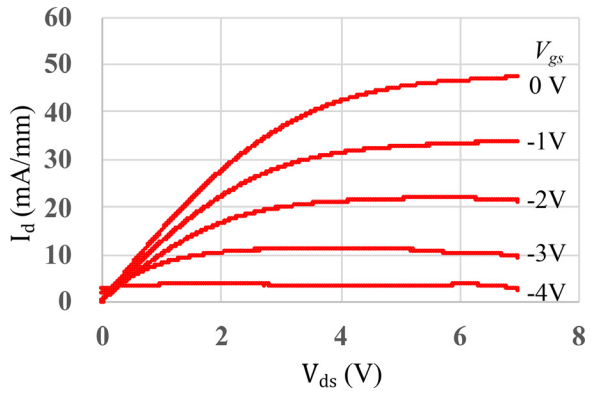

FIG. 4. *I–V* characteristics of fabricated transistor. The gate voltage bias (V_{gs}) was varied from 0 to –4 V in –1 V increments.

SiC-HEMT exhibited normally on operation. The maximum I_d was 47.5 mA/mm at $V_{gs} = 0$ and $V_{ds} = 7$ V. Using the saturated I_d values at V_g of 0 and –1 V, we estimated the transconductance for the device to be about 13.5 mS/mm. Further work is required to improve the blocking performance of the Schottky gate and on/off current ratio.

Since the measured current density for the SiC-HEMT was one order of magnitude smaller than those for GaN-HEMTs,[22] the factors limiting the drain current were investigated. The saturation current per unit gate width (I_{sat}) for HEMTs is expressed as[23]

$$I_{\text{sat}} = \frac{(V_g - V_{th})}{R_c + \frac{L_{gs}}{q\mu N_s} + \frac{2L_g}{\mu C_g (V_g - V_{th})}} \quad (1)$$

with

$$C_g = \frac{\varepsilon_s \varepsilon_0}{t}, \quad (2)$$

where V_g is the gate voltage, V_{th} is the threshold voltage, R_c is the source contact resistance, L_{gs} is the source–gate spacing, q is the elementary charge, μ is the 2DEG mobility, C_g is the gate capacitance per unit area, ε_0 is the permittivity of vacuum, ε_s is the permittivity of the 3C–SiC layer, and t is the thickness of the 3C–SiC layer. Substituting into Eq. (1), the threshold value of −3.8 V estimated from Fig. 4, the μ_{Hall} value of 586 $\text{cm}^2/\text{V s}$ and the N_s value of $1.48 \times 10^{13}/\text{cm}^2$ determined by Hall effect measurements, and the R_c value of 18.2 Ω mm obtained from measurements using the transfer length method, the saturation current is calculated to be 69.1 mA/mm. This is the same order of magnitude as the maximum I_d value of 47.5 mA/mm shown in Fig. 4. Based on the above-mentioned results, methods for increasing the current density in SiC-HEMTs can be considered. Equation (1) indicates that the current density is limited by the low μ_{Hall}, high R_c, and large size of the fabricated device. The current density is in fact inversely proportional to both L_{gs} and L_g, as shown in Eq. (1). By further improving the quality of the epitaxial layer to increase the 2DEG mobility, reducing the resistance of the ohmic contacts, and decreasing the device dimensions, it is expected to be possible to fabricate lateral-type transistors with a current density comparable to that for GaN-HEMTs.

In summary, we have fabricated a SiC-based HEMT using a C-face 3 C/4H–SiC heterostructure. The formation of 2DEG by spontaneous polarization was experimentally verified, and modulation of the channel current using a gate bias voltage was demonstrated.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Hiroyuki Sazawa: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Funding acquisition (lead); Project administration (lead); Supervision (lead). **Akira Nakajima:** Formal analysis (equal). **Shigeyuki Kuboya:** Data curation (supporting); Formal analysis (supporting). **Hitoshi Umezawa:** Data curation (supporting); Formal analysis (equal). **Tomohisa Kato:** Data curation (supporting); Formal analysis (equal). **Yasunori Tanaka:** Project administration (equal); Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]E. O. Johnson, RCA Rev. **26**, 163 (1965).
[2]C. Codreanu, M. Avram, E. Carbunescu, and E. Iliescu, Mater. Sci. Semicond. Process. **3**, 137 (2000).
[3]H. Sazawa and H. Yamaguchi, Appl. Phys. Lett. **120**, 212102 (2022).
[4]M. Shur, B. Gelmont, and M. A. Khan, J. Electron. Mater. **25**, 777 (1996).
[5]A. Hospodkova, F. Hajek, T. Hubacek, Z. Gedeonova, P. Hubík, J. J. Mares, J. Pangrac, F. Dominec, K. KuldovA, and E. Hulicius, J. Crystal Growth **605**, 127061 (2023).
[6]P. Kackell, B. Wenzien, and F. Bechstedt, Phys. Rev. B **50**, 17037 (1994).
[7]Z. Li and R. C. Bradt, J. Appl. Phys. **60**, 612 (1986).
[8]D. N. Talwar and J. C. Sherbondy, Appl. Phys. Lett. **67**, 3301 (1995).
[9]L. Barrett, R. G. Seidensticker, W. Gaida, and R. H. Hopkins, J. Cryst. Growth **109**, 17 (1991).
[10]E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and J. Schmidt, Appl. Phys. Lett. **107**, 091605 (2015).
[11]R. O. Carlson, G. A. Slack, and S. J. Silverman, J. Appl. Phys. **36**, 505 (1965).
[12]J. M. S. Gordillo, G. G. Diez, M. P. Pujado, M. Salleras, D. Estrada-Wiese, M. Dolcet, L. Fonseca, A. Morata, and A. Tarancon, Nanoscale **13**, 7252 (2021).
[13]M. V. S. Chandrashekhar, C. I. Thomas, J. Lu, and M. G. Spencer, Appl. Phys. Lett. **91**, 033503 (2007).
[14]O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999).
[15]V. M. Polyakov and F. Schwierz, J. Appl. Phys. **98**, 023709 (2005).
[16]A. Qteish, V. Heine, and R. J. Needs, Phys. Rev. B **45**, 6534 (1992).
[17]B. K. Park, Y. Ding, J. P. Pelz, P. G. Neudeck, and A. J. Trunek, Appl. Phys. Lett. **89**, 042103 (2006).

23 March 2024 11:57:08

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[18]H. Angerer, D. Brunner, F. Freudenberg, O. Ambacher, M. Stutzmann, R. Hopler, T. Metzger, E. Born, G. Dollinger, A. Bergmaier, S. Karsch, and H. J. Korner, Appl. Phys. Lett. **71**, 1504 (1997).
[19]W. Kern, J. Electrochem. Soc. **137**, 1887 (1990).
[20]J. Wan, M. A. Capano, and M. R. Melloc, Solid State Electron. **46**, 1227 (2002).
[21]S. Yoshida, K. Sasaki, E. Sakuma, S. Misawa, and S. Gonda, Appl. Phys. Lett. **46**, 766 (1985).
[22]H. Amano, Y. Baines, E. Beam *et al.*, J. Phys. D **51**, 163001 (2018).
[23]S. M. Sze, *Physics of Semiconductor Devices*, 3rd ed. (John Wiley & Sons, Inc., 2007).

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