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Au/SnO_2/n-Si (MOS) structures response to radiation and frequency

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Abstract

Metal–insulator–semiconductor (MOS) structures with insulator layer thickness of 290 Å were irradiated using a ^{60}Co (γ-ray) source and relationships of electrical properties of irradiated MOS structures to process-induced surface defects have been investigated both before and after γ-irradiation. The density of surface state distribution profiles of the sample Au/SnO_2/*n*-Si (MOS) structures obtained from high–low frequency capacitance technique in depletion and weak inversion both before and after irradiation. The measurement capacitance and conductance are corrected for series resistance. Series resistance (*R*s) of MOS structures were found both as function of voltage, frequency and radiation dose. The $C(f)-V$ and $G(f)-V$ curves have been found to be strongly influenced by the presence of a dominant radiation-induced defects. Results indicate interface-trap formation at high dose rates (irradiations) is reduced due to positive charge build-up in the semiconductor/insulator interfacial region (due to the trapping of holes) that reduces the flow rate of subsequent holes and protons from the bulk of the insulator to the Si/SnO_2 interface. The series resistance decreases with increasing dose rate and frequency the radiation-induced flat-band voltage shift in 1 V. Results indicate the radiation-induced threshold voltage shift (ΔV_T) strongly dependence on radiation dose rate and frequency.

Keywords: γ-rays; MOS structure; Radiation effect; MOS; Interface states; Series resistance

1. Introduction

The metal–insulator–semiconductor (MOS) structures consist of a semiconductor substrate covered by an insulator layer (between ≈ 50 and 5000 Å) upon which a metal electrode gate is deposited. Due to its importance in Si technology, MOS devices have been a focus intensive study for more than 40 years [1–28]. In real MOS structures localised interface states exist at the semiconductor–insulator interface and the device behaviour is different than ideal case due to their presence. The reason for their existence is the interruption of the periodic lattice structure at the surface [1,29], surface preparation, formation of insulator layer and impurity concentration of semiconductor [11]. These interface states usually cause a bias shift and frequency dispersion of the capacitance–voltage (C–V) and conductance–voltage (G–V) curves [2]. In MOS structures with thick insulator layer ($d_{ox} \geq 50$ Å, typically ≈ 500 Å), the interface states are equilibrium with semiconductor and $d_{ox} \leq 10$ Å, surface states are equilibrium with metal [2]. When the insulator layer thickness is less than 50 Å, direct tunnelling becomes possible in MOS structures [6]. Nevertheless satisfactory understanding in all details has still not been achieved. Various measurement techniques for determining the interface state density traps such as the high–low frequency capacitance [30,31], quasi-static capacitance [32], surface admittance [33] and conductance techniques have been developed and among than the more important ones are high–low frequency capacitance and conductance technique [10]. Because both the input conductance and capacitance are contain similar information about the interface traps. The (high–low) capacitance measurement, however, can give rapid evaluation of the flat band shift and the total interface trapped charge (Q_{it}). This technique uses the fact that the difference in measured capacitances is attributed to the inability of interface traps to respond to the small signal at high frequencies.

Because at high frequencies ω (such the carrier life time τ is much larger than $1/\omega$) the charge at the interface states cannot follow an ac signal. When the measured capacitance

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is corrected for series resistance (R_s), the interface trap density (D_{it}) is obtained as a function of gate bias for energies not near the band edge. The conductance technique, as developed by Nicollian and Goetzberger [1], is generally considered to be the most complete method for probing the interface traps due to its high sensitivity and accuracy, as it is able to detect trap densities as low as $10^8\ cm^{-2}\ eV^{-1}$ [29]. The high–low frequency method is the simplest one to use and the density of interface traps detectable by this method is in the order of $10^{10}\ cm^{-2}\ eV^{-1}$, which is enough for many applications method [30].

Recently, the radiation response of MOS devices has been found to change significantly when these devices are exposed to irradiation stress treatments [12–28]. Winokur et al [13,18,21] and Ma [22] were among the first to make a systematic observation of the after irradiation behaviour of radiation-induced D_{it} in MOS devices. In some highly specialised applications, MOS devices may be subjected to radiation levels in the megarad range. Exposure of radiation doses greater than a kilorad may cause strong electrical changes in the MOS structures. Especially there are two effects of radiation: the transient effects are due to the electron–hole pair generation and permanent effect is due to the bombardment of a devices with radiation which causes changes in the crystal lattice. The radiation-generated electrons either recombine with the holes are move out of insulator. The radiation-generated holes may diffuse in the insulator, bur are less mobile than the electrons; many stationary hole traps are also present.

In order to achieve a better understand of the effects of different charge surface states on MOS devices we measured the C–V and G–V characteristics as a function of γ-ray irradiation doses (3–500 kGy) and oxide thickness for a wide frequency range (500 Hz–10 MHz) at room temperature. The major purpose of this study was to compare estimates of interface trap densities obtained experimentally for the MOS devices using low–high frequency technique before and after irradiation.

2. Experimental detail

The MOS capacitor used in this work was fabricated using n-type (P-doped) single crystals silicon wafer with ⟨111⟩ surface orientation, 280 μm thick, 2″ diameter and 4.45 Ω cm resistivity. The Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$: 1HF: $35H_2O$, 20%HF. Preceding each cleaning step, the wafer was rinsed thoroughly in deionised water of resistivity of 18 MΩ cm. Immediately after surface cleaning, high purity Au metal (99.999%) with a thickness of 2500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of 1×10^{-6} Torr. Sintering the evaporated Au back contact was formed the ohmic contact under vacuum. Immediately after ohmic contact, a thin layer of SnO_2 was grown on the Si substrate by spraying a solution consisting of 32.21 wt% of ethyl alcohol (C_2H_5OH), 40.35 wt% of deionised water (H_2O) and 27.44 wt% of stannic chloride ($SnCl_4{\cdot}5H_2O$) on the substrate, which was maintained at a constant temperature of 400 °C. The temperature of the substrates was monitored by chromel–alumel thermocouple fixed on top surface of the substrate. The variation of the substrate temperature during spray was maintained within ±2 °C with the help of a temperature controller. The rate of spraying was kept at about 30 cc min^{-1} by controlling the carrier gas flowmeter. N_2 was used as the carrier gas. SnO_2 dots were 4 mm in diameter. After spraying process, circular dots of 2 mm in diameter and 2500 Å thick Au rectifying contacts were deposited onto the SnO_2 surface of the wafer through a metal shadow mask in liquid nitrogen trapped oil-free ultra-high vacuum system in the pressure of 1×10^{-6} Torr. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The deposition rates were about 1–3 Å s^{-1}. The interfacial oxide layer thickness was estimated to be about 290 Å from measurement of the oxide capacitance in the accumulation for MOS1. The C–V and G–V measurements were performed in the dark before and after irradiation at various frequency (500 Hz–10 MHz) and various radiation dose rate (3–500 kGy) by using HP 4192A LF impedance analyser (5 Hz–13 MHz). Small sinusoidal signal of 40 mV p–p from the external pulse generator is applied to the sample in order to meet the requirement [1].

3. Results and discussion

3.1. Theoretical background

The C–V and G–V curves were measured at various frequencies both before and after γ radiation by using an HP 4192A LF impedance analyser (5 Hz–13 MHz) and the impedance analyser was controlled by the data requisition software. A small sinusoidal ac signal of 40 mV p–p from external pulse generator is applied to the MOS structure in order to meet requirement [1,10,11]. Interface trap densities were changed in the test devices by using the ^{60}Co γ-ray source with the dose rate of 2.12 kGy h^{-1}. Seven exposures were performed at doses of 3, 10, 30, 50, 100, 300 and 500 kGy. Bias was not during γ-irradiation. The measurements were performed at various frequency but six spot frequencies from 100 kHz to 1 MHz at room temperature.

Before any analysis the series resistance is calculated from the measured admittance when the MOS devices is based in strong accumulation [29]. The corrected admittance is converted into the parallel admittance using

the equation

$$\frac{G_p}{\omega} = \frac{\omega G_a C_{ox}^2}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \quad (1)$$

where C_c and G_c are the represent measured capacitance and conductance, respectively, of the MOS device corrected for series resistance. Series resistance was calculated from the admittance measured in strong accumulation according to Ref. [29]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \quad (2)$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance in strong accumulation region. The series resistance, corrected capacitance, and conductance values were obtained as a function of angular frequency from the direct measured C_m and G_m according to,

$$C_c = \frac{\lfloor G_m^2 + (\omega C_m)^2 \rfloor c_m}{a^2 + (\omega C_m)^2} \quad (3)$$

and

$$G_c = \frac{G_m^2 + (\omega C_m)^2 a}{a^2 + (\omega C_m)^2} \quad (4)$$

where

$$a = C_m - \left\lfloor G_m^2 + (\omega C_m)^2 \right\rfloor R_s \quad (5)$$

The insulator layer thickness calculated from the strong accumulation capacitance is found to be 290 Å for samples MOS1. The substrate doping density (N_D) was deduced from the slope of the 1 MHz C–V curve in the depletion region and found about 10^{15} cm^{-3} for all the samples.

3.2. High–low frequency capacitance (C_{HF}–C_{LF}) technique

The advantage of this method comes from the fact that it permits determination of many properties of the insulating interface layer, the semiconductor substrate, and interface easily. In this method [30], the interface state density is extracted from its capacitance contribution to the measured experimental C–V curve. In the equivalent circuit of MOS capacitor, the oxide capacitance C_{ox} is in series with the parallel combination of the interface state capacitance C_{it} and the space charge capacitance C_{sc} : The interface state capacitance C_{it} can be determined by subtracting the space charge capacitance C_{sc} (extracted from the measured high frequency capacitance C_{HF}) from the space charge capacitance in parallel with the interface state capacitance (extracted from the measured low frequency capacitance C_{LF}) and is given as:

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right]^{-1} - C_{sc} \quad (6)$$

At high frequencies, surface states cannot respond to the ac excitation, so they do not contribute to the total capacitance directly, but stretch-out of the C–V curve occurs. Therefore the equivalent capacitance is the series connection of insulator layer capacitance C_{ox} and space charge capacitance C_{sc}, is given as:

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}} \quad (7)$$

Thus combining Eqs. (6) and (7), the interface state density D_{it} is calculated from

$$qAD_{it} = C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right]^{-1} \quad (8)$$

This integration is performed numerically from the flat band to strong accumulation and to strong inversion as in Ref. [34]. The measured high–low frequency curves are shown in Fig. 1. For the case of an Au/SnO_2/n-Si (MOS1) capacitor with an insulator layer thickness of 290 Å as determined from oxide capacitance C_{ox}. Surface potential versus applied voltage for the Au/SnO_2/n-Si (MOS1) sample is shown in Fig. 2 before and after irradiation. The energy position in the n-Si band gap is calculated as:

$$E_c - E_{ss} = q(\varphi_s - \phi_F) \quad (9)$$

where ϕ_F is the position of fermi energy level,

$$\phi_F = \frac{kT}{q} \ln(N_C/N_D)$$

The surface potential as a function of bias is found from the numerical integration of the lowest measurable frequency C–V curve according to,

$$\bar{\Psi}_s = \int_{V_a}^{V_G} \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV_G + \Psi^* \quad (10)$$

where V_a is the bias voltage in strong accumulation when the capacitance is equal to the oxide capacitance C_{ox} and

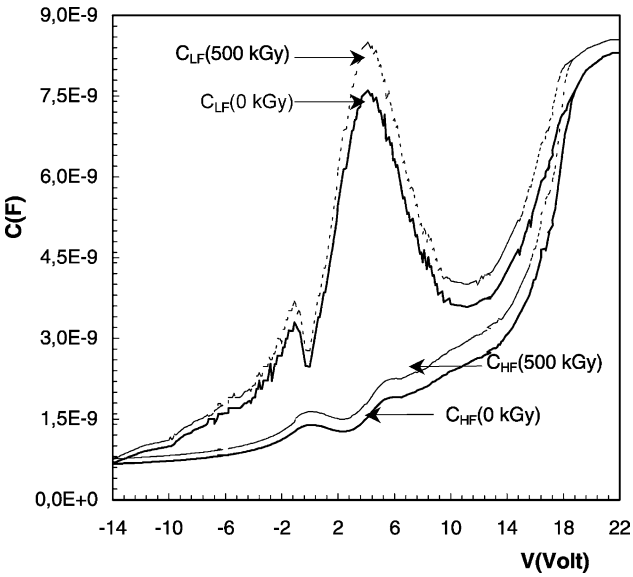

Fig. 1. Measured high–low frequency C–V plots at before and after irradiation.

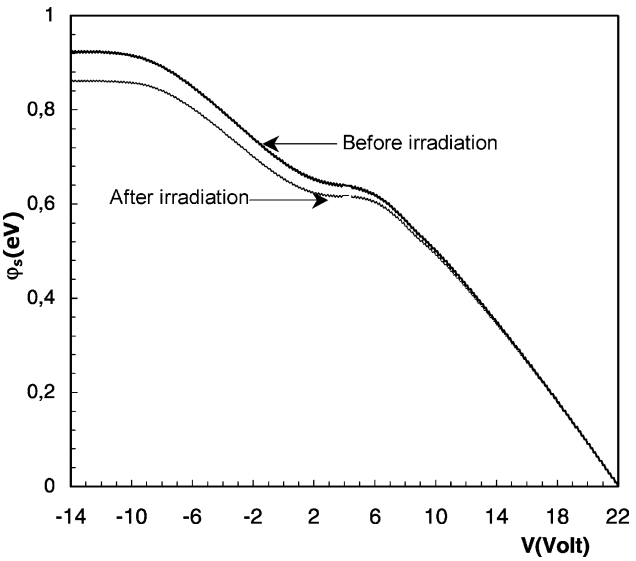

Fig. 2. Surface potential vs gate bias characteristic.

the integration constant ψ^* was found by extrapolating the $C_{sc}^{-2}-\psi_s$ curve in the depletion region (0.36 eV) to $C_{sc}^{-2}=0$ [29,34]. The density of surface states distribution profiles of the sample MOS1 obtained both before irradiation and after irradiation (500 kGy) from the high–low capacitance measurements is shown in Fig. 3. Both before and after irradiation (500 kGy), the surface states distribution profiles over accessible band gap energy with peaked structure. The density of surface states is seen to rise sharply toward the middle of Si band gap. The surface states distributions with peaked structure were also observed in the past [5,10,33,35].

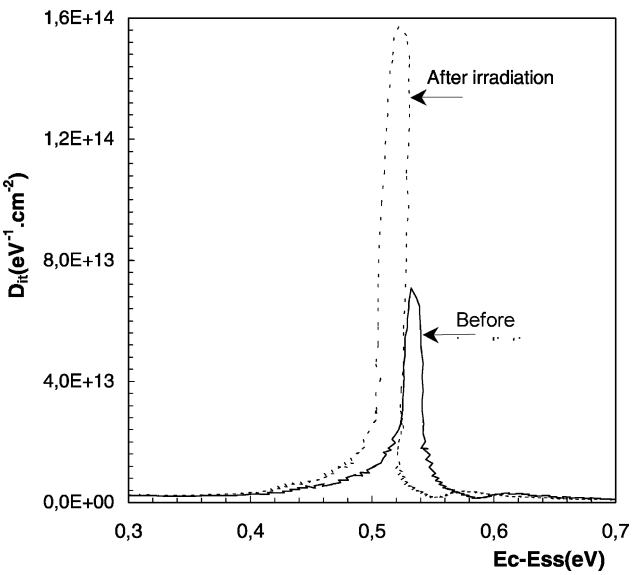

Fig. 3. Experimental surface state density D_{it} distribution as a function of the band gap energy obtained from high–low frequency capacitance technique at before and after irradiation.

3.3. Conductance technique

The conductance technique [1] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small ac signal is applied to the MOS devices. The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the dc bias, when the MOS device is in the depletion. In Nicollian and Goetzberger's statically theory [1,35], in which random distribution of discrete insulator charges and charged surface states in the semiconductor/insulator (Si/SnO_2) interface plane cause a non-uniform distribution of surface band bending over the interfacial plane.

Fig. 4(a) and (b) show the measured C_m-V and $G_m/\omega-V$ characteristics of MOS1 devices at various frequencies

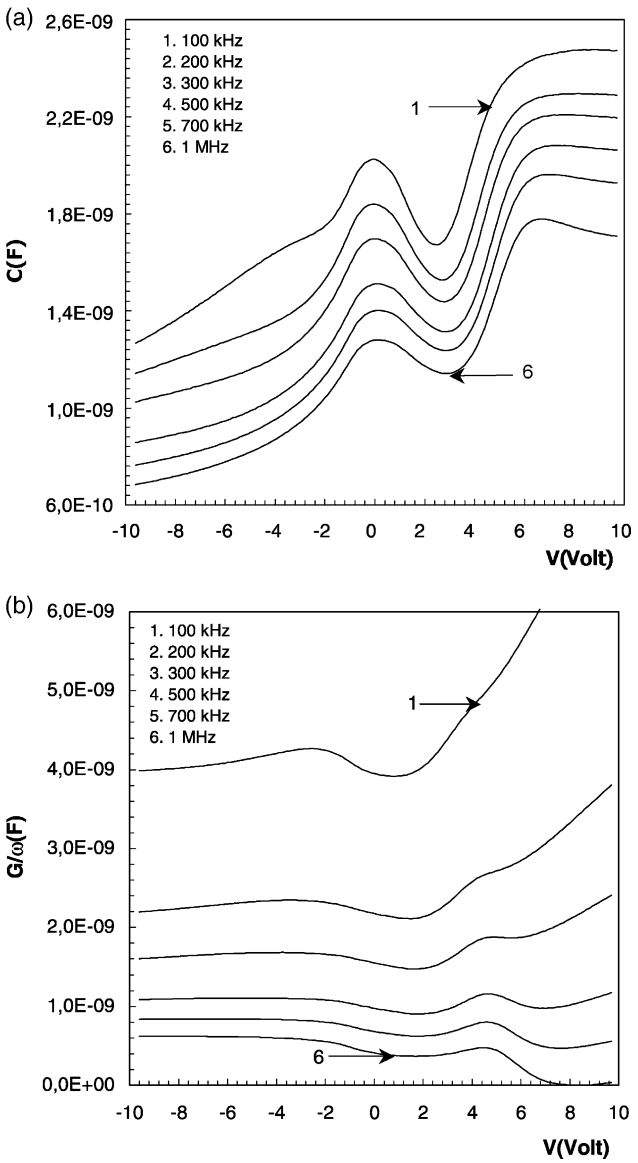

Fig. 4. Measured capacitance (C) and equivalent parallel conductance (G/ω) vs gate bias at various frequencies.

before irradiation. Here, all the data used in these figures are corrected for the series resistance. As a result, the magnitude and profile of the G_p/ω–f are quite different for the gate bias. This result suggests that distribution profile is not inherent but a consequence of formation of states at the interface during and after the sample processing.

The parallel conductance G_p/ω–f characteristics for the samples at various gate biases in the depletion region illustrated in Fig. 5. The G_p/ω–f characteristics of MOS1 consist of a peak. This peak due to surface state contribution shifts from low frequency to high as the bias changes from depletion toward the flat band condition as predicted by the theory. The MOS structures were given different radiation doses to increase the charge trapping, which decreases for insulator layer thickness less than 100 Å [3]. The variations of C–V and G–V characteristics for high frequency (500 kHz) applied voltage are shown before and after γ-ray irradiation in Fig. 6(a) and (b), respectively. The voltage shift ΔV changes about 1 V with increasing the irradiation dose from 3 to 500 kGy.

We do not show the quasi-static C–V curves but we show low frequency C–V curves. The oxide-trapped charge is determined from the radiation-induced voltage shift. The interface-trap distribution was calculated by conductance method. The series resistance of MOS structure calculated at strong accumulation region for the test devices irradiated to 3, 10, 30, 50, 100, 300, 500 kGy were 163, 162, 161, 160, 159, 155, 152 and 154 Ω, respectively. These very significant values of R_s demanded that special attention be given to the effects of series resistance in the application of the C–V and G–V measurements. In addition to voltage dependent and frequency dependent series resistance were found as shown in Figs. 7 and 8, respectively. In addition to both voltage and radiation doses dependent on series resistance is given in Fig. 9.

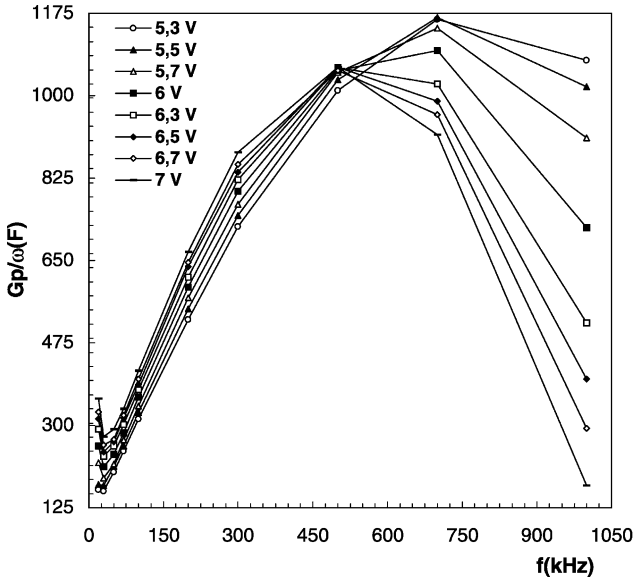

Fig. 5. Equivalent parallel conductance G_p/ω vs frequency at various gate bias.

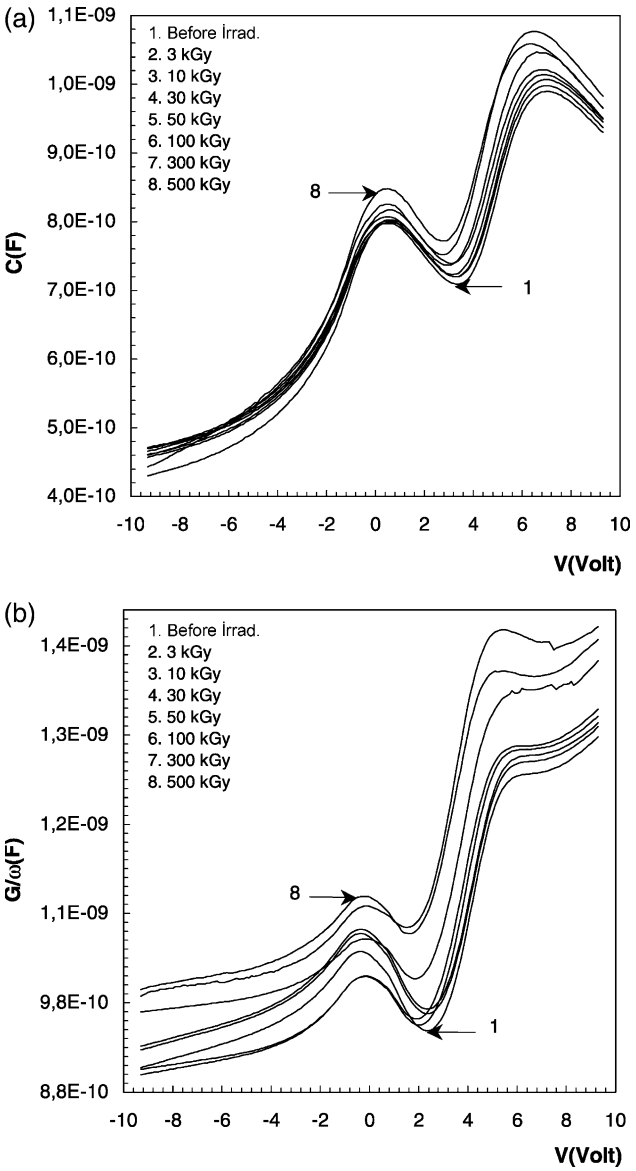

Fig. 6. Measured capacitance (C) and equivalent parallel conductance (G/ω) vs gate bias under different doses at 500 kHz.

4. Conclusions

During the oxidation, a number of strained bonds are formed in the insulator layer (SiO_2 or SnO_2). The γ-irradiation causes many of these strained bounds to break [High- and low-frequency data were taken to determine the initial surface states density, which was found to be high, from 2×10^{12} to 8×10^{13} $cm^{-2}eV^{-1}$, for all the samples]. The high–low frequency capacitance method uses the difference in high and low frequencies C–V characteristics measured in depletion and weak inversion to estimate a distribution of interface trap densities between the flat-band

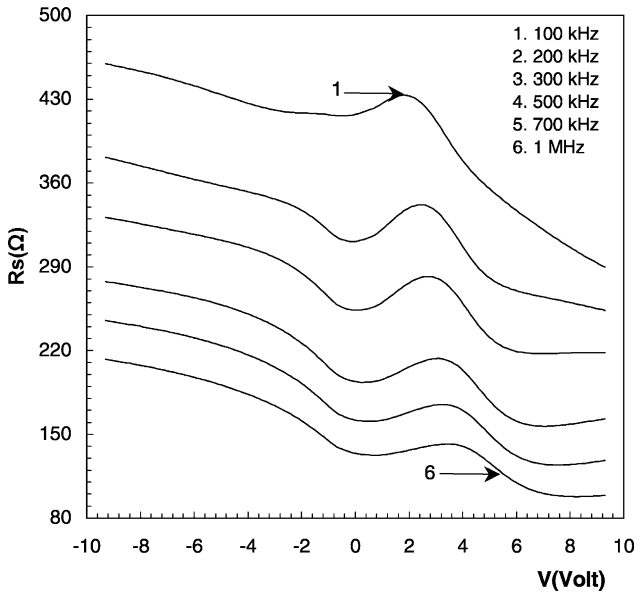

Fig. 7. Voltage dependent of series resistance at various frequencies.

and threshold. The resulting stretch-out of the C–V characteristics is due to both interface states and lateral non-uniformities of radiation-induced space charge. Such effects are directly related to the number of process-induced surface defects.

Especially, there are four points can be noted. First, the density of interface states increases monotonically with increasing oxide thickness. Second, all MOS devices show a dependence of series resistance and capacitance on frequency. Third, the positive trapped charge increases by increasing the radiation dose without saturation to 500 kGy. Fourth, both series resistance and interface states decrease with increasing radiation dose.

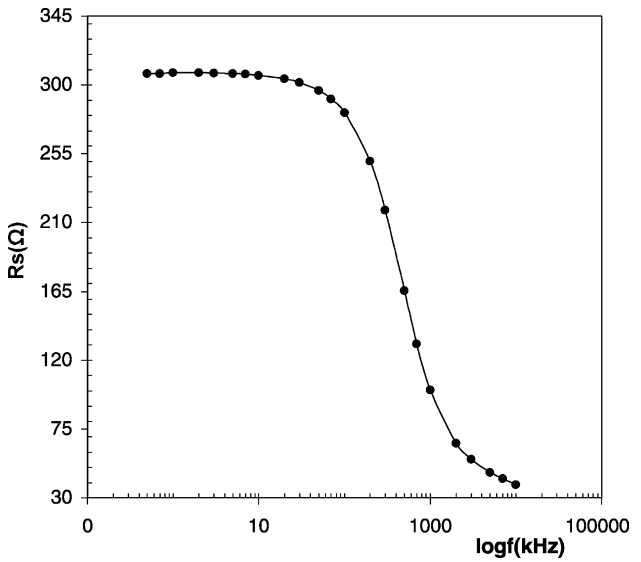

Fig. 8. Frequency dependent of series resistance.

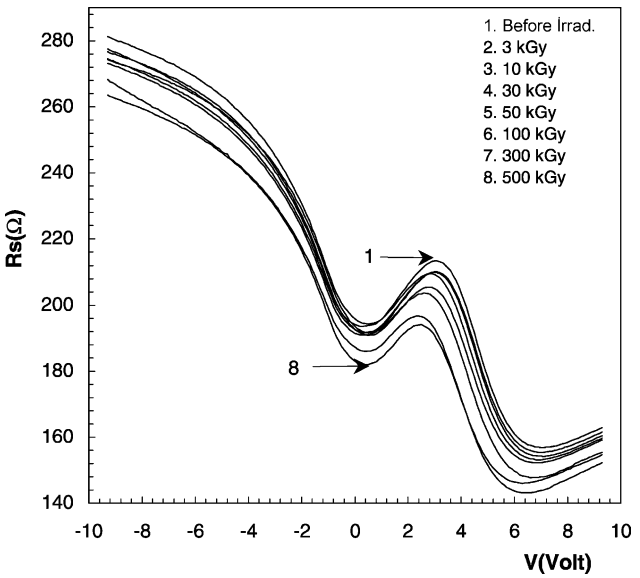

Fig. 9. Voltage dependent of series resistance at various doses.

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