Temperature Coefficient of Silicon-Based Carrier Selective Solar Cells

Nithin Chatterji, Aldrin Antony, and Pradeep R. Nair

***Abstract*—Carrier selective (CS) Silicon solar cells are increasingly explored as a low-cost alternative to PN junction Silicon solar cells. While the recent trends on power conversion efficiency are encouraging, the temperature coefficient and hence the power output under elevated temperatures are not well explored for such solar cells. Here, we address this issue through detailed numerical simulations to explore the influence of interface and material parameters on the temperature coefficient. Our results indicate that irrespective of the interface quality, the temperature coefficient of CS solar cells improves with an increase in band discontinuities. Interestingly, contrary to the trends related to efficiency, our results indicate that the temperature coefficient of CS solar cells is more critically affected by the interface quality of the minority carrier extraction layer than the majority carrier extraction layer. These insights have important implications toward the choice of optimal material and processing conditions for Si-based CS solar cells**

***Index Terms*—Photovoltaic cells, semiconductor device modeling, temperature coefficient.**

I. Introduction

SI-BASED carrier selective (CS) solar cells are considered as a good candidate to challenge the market dominance of conventional PN junction based solar cells. The perceived competitiveness stems from a few advantages like -

1) Large bandgap materials used as CS layers provide carrier selectivity through appropriate band offsets [1], [2].
2) It reduces the parasitic absorption as compared with the heavily doped emitter layer in PN junction solar cells or doped a-Si in heterojunction with intrinsic thin-layer (HIT) solar cells [3].
3) The intrinsic doping density of many CS materials [4]–[6] could be significant enough to eliminate the need for any additional intentional doping process.
4) Possibility of low temperature deposition processes for CS layers [6]–[11].

These aspects could lead to reduced thermal budget and hence lower the cost of fabrication, which motivates the significant recent research interest in CS-based solar cells. Accordingly, different materials, such as TiO_2 [4], [5], [12], a-Si [3], poly-Si [13], LiF_x [7], KF_x [8], PEDOT:PSS [6], MoO_x [9]–[11], [14],V_2O_5 [11], and WO_3 [11] have been extensively studied. Similarly, there are many simulations and analytical studies to understand the working of these types of solar cells [15]–[21]. However, most of these studies were at standard test conditions (STCs), which could be significantly different from the actual conditions at the place of deployment. The power output from a panel at actual conditions could be significantly different from that at STC because of the strong dependence of efficiency on temperature. In this regard, the temperature coefficient of efficiency for a solar cell is often treated as a critical parameter to ascertain and compare the performance of various technologies. Indeed, the temperature coefficient of PN junction [22], [23] and HIT solar cells [24] are well explored. However, such a detailed study has not been reported yet on CS solar cells (although temperature coefficient of MoO_x was recently discussed [20], [21]). Since diverse materials are being investigated as CS layers, *a priori* knowledge of temperature coefficient as a function of material parameters would be immensely beneficial.

In this article, the temperature coefficient for CS-based solar cells is established through detailed modeling and is then compared with the well-established HIT and passivated emitter and rear contact (PERC) solar cell technologies. For this, we first develop an analytical model to predict the functional dependence of temperature coefficient on important parameters like band discontinuity and interface quality (see Section II). These predictions are then validated through detailed numerical simulations (see Section III). Our results indicate that the temperature coefficient is limited by V_{oc} for smaller band discontinuities and it follows the trend of FF for larger magnitudes of band discontinuity. Additionally, unlike efficiency [17], temperature coefficient of CS-based solar cells is dominated by the interface quality of the minority carrier collection junction. Below we first develop an analytical model to predict the temperature coefficient.

II. Analytical Model

Fig. 1 shows band level alignments of Si heterojunction solar cell with CS layers (the material parameters are provided in the appendix). Selective collection of electrons and holes at different electrodes are made possible through the electron selective layer (ESL) and hole selective layer (HSL), respectively. The large valence band offset at ESL/Si interface blocks the transport of holes from Si to ESL. However, the smaller conduction band offset at the same interface aids the transport of electrons

Manuscript received August 22, 2018; revised November 9, 2018; accepted December 16, 2018. Date of publication February 12, 2019; date of current version April 19, 2019. *(Corresponding author: Nithin Chatterji.)*

The authors are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India (e-mail: nithin@ee.iitb.ac.in; aldrinantony@iitb.ac.in; prnair@ee.iitb.ac.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org

Digital Object Identifier 10.1109/JPHOTOV.2019.2892127

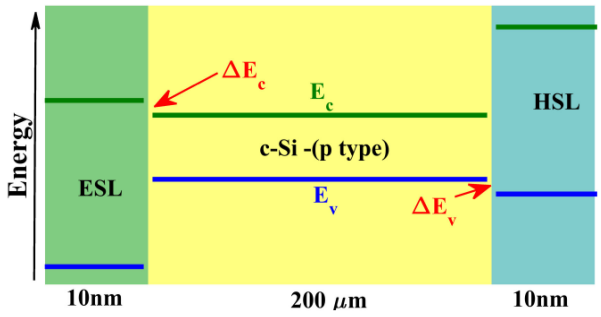

Fig. 1. Energy level alignments of a Si-based CS solar cell. Refer Table I for simulation parameters.

to ESL. Note that a positive value for band offset indicates that the photogenerated carriers need to overcome a barrier to reach the corresponding selective layer, where as a negative value for the offset indicates that the carrier injection from transport layer to silicon is limited by a potential barrier. Further there could be imperfections in the interface as traps. Similarly, we assume that the Si/HSL interface to be perfect electron blocking with a smaller valence band offset that aids hole collection. Here we explicitly consider the temperature coefficient variations of such solar cells as a function of transport barrier and interface trap density. As such, temperature coefficient could also be influenced by parameters like the effective doping and thickness of CS layers, nature of metal or TCO contact with the CS layers, etc. With the aim of developing a coherent description of the various effects, here we make a few simplifying assumptions.

1) The contact layers are assumed to be doped.
2) The metal or TCO contact with selective layers are assumed to be ohmic in nature.
3) Over-the-barrier transport is assumed as the dominant transport mechanism at Si/CS layer interface.
4) Uniform density of traps at Si/CS layer interface with top half of the bandgap occupied by the acceptor like traps and bottom half of the bandgap occupied by the donor like traps.

We stress that because of assumption (3) listed above, our analysis will not be directly valid for hole quenching contact materials, such as MoO_x, V_2O_5, and WO_3. However, it should be generally valid for all materials where over-the-barrier transport remains the dominant charge collection mechanism. With these assumptions, we first develop an analytical model to predict the device performance. Later, results from detailed numerical simulations (self-consistent solution of Poisson and carrier continuity equations) are provided to further refine analytical predictions. The parameters used in this study are listed in Appendix A.

The temperature coefficient of the efficiency is defined as

$$\mathrm{TC}\eta = \frac{1}{\eta\,(\mathrm{STC})}\frac{\partial \eta}{\partial T} \tag{1}$$

where STC denotes the standard test conditions. The efficiency of a solar cell, in turn, depends on the open-circuit potential (V_{oc}), short-circuit current (J_{sc}), and the fill factor (FF) [25]. Accordingly, a first-order estimate for $\mathrm{TC}\eta$ can be obtained in terms of the individual temperature coefficients as follows:

$$\frac{1}{\eta\,(\mathrm{STC})}\frac{\partial \eta}{\partial T} = \frac{1}{V_{\mathrm{oc}}\,(\mathrm{STC})}\frac{\partial V_{\mathrm{oc}}}{\partial T} + \frac{1}{J_{\mathrm{sc}}\,(\mathrm{STC})}\frac{\partial J_{\mathrm{sc}}}{\partial T} + \frac{1}{\mathrm{FF}\,(\mathrm{STC})}\frac{\partial \mathrm{FF}}{\partial T}. \tag{2}$$

Here, the terms in the right-hand side (RHS) denote temperature coefficients of V_{oc} $(\mathrm{TCV_{oc}})$, J_{sc} $(\mathrm{TCJ_{sc}})$, and FF (TCFF), respectively. Note that each of these temperature coefficients is defined against the respective parameter at STC. As such, good estimates for the temperature coefficient of efficiency can be obtained through detailed knowledge about the temperature dependence of parameters like V_{oc}, J_{sc}, and FF. With this aim, and to develop quantitative insights, we first explore the effect of ESL/Si interface parameters on $\mathrm{TC}\eta$ with ideal conditions assumed for Si/HSL interface (i.e., zero band offset for holes, perfect electron blocking, and lack of any interface trap states).

1) *Effect of ΔE_c on TCV_{oc}*

It is well known that the temperature coefficient of solar cell is dominated by the temperature sensitivity of V_{oc} [26]. For a solar cell, the maximum achievable V_{oc} is dictated by the detailed balance of carrier generation with various recombination mechanisms [17]

$$\int G dx = -\frac{J}{q} + R_{\mathrm{bulk}} + R_{\mathrm{interface}} \tag{3}$$

where left-hand side is the total generation in the device, $-J/q$ is the current through the ESL, R_{bulk} is the total bulk recombination in the device, and $R_{\mathrm{interface}}$ is the interface recombination. The asymptotic limits of $V_{\mathrm{oc}}$for a CS solar cell in the presence of interface traps were recently reported [17]. Specifically, in the absence of any interface recombination the V_{oc} will be at a maximum and is given by

$$V_{\mathrm{oc,max}} = \frac{\mathrm{kT}}{q}\ln\left(\frac{G\,\tau_b N_A}{n_i^2}\right). \tag{4}$$

On the other hand, if interface recombination dominates, then V_{oc} could be at its minimum and is given as

$$V_{\mathrm{oc,min}} = \frac{2\mathrm{kT}}{q}\ln\left(\frac{2G w_{\mathrm{Si}}}{c_{ns} D_{\mathrm{it}} E_{g,\mathrm{Si}} n_i}\right). \tag{5}$$

Here, $V_{\mathrm{oc,max}}$ and $V_{\mathrm{oc,min}}$ are the maximum and minimum values of V_{oc}, respectively, k is the Boltzmann constant, G is the carrier generation rate in Silicon, τ_b is the effective bulk life time in Silicon [the combined effects of Shockley–Read–Hall (SRH), radiative, and Auger recombinations], N_A is the acceptor doping in Silicon, n_i is the intrinsic carrier concentration in Silicon, D_{it} is the interface defect density at the ESL/Si interface, w_{Si} is the thickness of the bulk silicon, c_{ns} is the capture coefficient for electrons in the traps, and $E_{g,\mathrm{Si}}$ is the bandgap of Silicon. Note that $V_{\mathrm{oc,max}}$ is influenced only by the bulk lifetime, while $V_{\mathrm{oc,min}}$ is entirely dictated by the interface recombination. Although (5) considers interface recombination

at Si/ESL junction only, it could be easily modified to account for the recombination in Si/HSL junction as well [17].

Equations (4) and (5) allow the estimation of the asymptotic limits for temperature coefficient of $V_{\rm oc}$. Accordingly, the maximum and minimum values of $\rm TCV_{oc}$ is determined as $-0.19\%/^{\circ}\rm C$ and $-0.37\%/^{\circ}\rm C$ with $\rm T = 298\ K$ as the temperature at STC (followed throughout this article), respectively, for typical values of one sun generation with the $D_{\rm it} = 10^{12}\rm cm^{-2}eV^{-1}$ and $\tau_b = 1\ \rm ms$. The values for radiative and Auger coefficients are given in Appendix A. The dominant temperature dependence of both the limits is through n_i^{-2}, which has an exponential relation with temperature $(n_i^2 \sim e^{-E_g/\rm KT})$. Hence, the temperature coefficient $\frac{1}{V_{\rm oc}(\rm STC)}\frac{\partial V_{\rm oc}}{\partial T}$ is negative. The smaller the magnitude of temperature coefficient for $V_{\rm oc}$, the better is its performance at high temperature.

Although the above-mentioned discussion allows the estimation of the asymptotic limits of $\rm TCV_{oc}$, it still lacks quantitative information on the functional dependence of $\rm TCV_{oc}$ on various parameters like band offset ΔE_c, interface state density $D_{\rm it}$, etc. To obtain the same, we rely on the modified analytical model for $V_{\rm oc}$ reported in [17]. Although the interested reader is recommended to [17] for details, here we provide a brief summary of the above-mentioned model. An explicit solution of the detailed balance model [i.e., (3)] under $V_{\rm oc}$ conditions is obtained by accounting for bulk and interface recombination. This requires very good estimates for not just the bulk carrier densities, but the interface carrier densities as well, which depend on the energy difference between the band levels (i.e., either conduction or valence band) and the corresponding quasi-Fermi levels. Under $V_{\rm oc}$ conditions, the quasi-Fermi levels are assumed to be spatially constant and analytical expressions for the band bending is obtained through solution of Poisson's equation near the CS layer/Si interface. Such a self-consistent approach allows the estimation of the $V_{\rm oc}$ and its functional dependence on parameters like band offset, doping density, dielectric constant, interface state density, etc. Once the $V_{\rm oc}$ is obtained, $\rm TCV_{oc}$ is estimated through (2) to explore the critical dependence of the same on interface and material parameters.

Fig. 2(a) shows the variation of $V_{\rm oc}$ with temperature as function of band discontinuity ΔE_c between ESL and Si with $D_{\rm it} = 10^{12}\rm cm^{-2}eV^{-1}$. As in [17], it indicates that $V_{\rm oc}$ varies almost symmetrically with ΔE_c, with minimum at $\Delta E_c \approx 0$. This is because of the fact that interface recombination maximizes under such conditions. The model also indicates that $V_{\rm oc}$ improves for large magnitudes of ΔE_c because of the reduction in interface recombination due to field effect passivation. As expected, the $V_{\rm oc}$ decreases with temperature because of its strong dependence of n_i [also predicted by (4) and (5)].

Fig. 2(b) shows the temperature coefficient of $V_{\rm oc}$ with variation in interface trap density $D_{\rm it}$, and ΔE_c. In general, the temperature coefficient degrades with an increase in $D_{\rm it}$ as the interface recombination becomes significant. However, for large magnitudes of ΔE_c, the interface recombination decreases because of enhanced field effect passivation of traps, which results in an increase in $V_{\rm oc}$ and improvement in $\rm TCV_{oc}$.

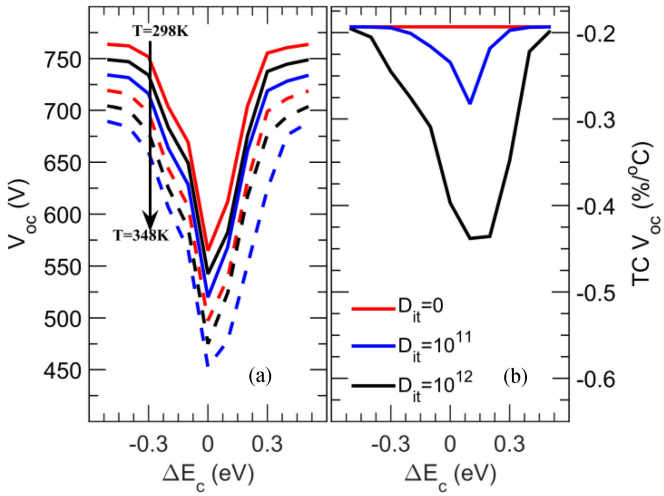

Fig. 2. ESL/Si interface: Variation of $V_{\rm oc}$ with ΔE_c, temperature and $D_{\rm it}$. (a) shows the variation of $V_{\rm oc}$ with temperature for $D_{\rm it} = 10^{12}\rm cm^{-2}eV^{-1}$. (b) shows the variation of temperature coefficient with $D_{\rm it}$.

2) *Effect of ΔE_c on $\rm TCJ_{sc}$ and TCFF*

$J_{\rm sc}$ depends on the number of absorbed photons in c-Si bulk and hence increases with temperature as Si bandgap decreases with temperature. This leads to a positive temperature coefficient of 0.0156%/°C which is very small compared with the $\rm TCV_{oc}$ reported in Section II.1. If we further account for the fact that the parasitic absorption in the ESL also increases with temperature, then the effect of temperature on $J_{\rm sc}$ is expected to decrease further. As this effect is insignificant relative to the $\rm TCV_{oc}$, we neglect the effect of bandgap variation on $J_{\rm sc}$ and assume that the effective photo-carrier generation rate is invariant with temperature.

While the net carrier generation rate could be rather insensitive to temperature variation, the charge collection efficiency could show strong temperature dependence and hence influence $J_{\rm sc}$. Over-the-barrier transport of carriers across the ESL/Si junction is a dominant mechanism for collection of photogenerated carriers, which might introduce additional temperature dependence on $J_{\rm sc}$. At short-circuit conditions, the interface recombination is negligible and the interface carrier density is given as $n_s \sim \frac{n_i^2}{N_A}e^{+\frac{q\psi_{\rm Si}}{\rm kT}}$, where $\psi_{\rm Si}$ is the band bending in Si at ESL/Si interface. Hence, the current through the ESL, which is $J_{\rm sc}$, is given as [17]

$$J_{\rm sc} \propto n_s e^{-\frac{\Delta E_c}{\rm kT}}. \tag{6}$$

Equation (6) can be conveniently interpreted in terms of the supply of electrons (n_s on the RHS), and the factor $e^{-\frac{\Delta E_c}{\rm kT}}$ denotes the probability of carriers crossing the barrier because of band offset (i.e., for $\Delta E_c > 0$. Else, the diffusion of electrons from bulk to Si/ESL interface will limit the current.).

It has been recently shown that the band bending in Si $(\psi_{\rm Si})$ at the Si/ETL interface increases with increase in ΔE_c [17]. Accordingly, the n_s increases with increase in ΔE_c and compensates for the reduction in the probability of crossing the barrier [see (6)] and hence $J_{\rm sc}$ remains invariant till strong

inversion happens [17]. Therefore, the temperature coefficient will be negligible for small ΔE_c . However, for large ΔE_c , strong inversion conditions arise at Si interface and hence the n_s will no longer increase with ΔE_c . This results in a decrease in $J_{\rm sc}$ for large ΔE_c , as predicted by (6). However, for such cases, the probability of carriers crossing the barrier increases with temperature, and as a result $J_{\rm sc}$ also improves with temperature [see (6)]. Hence, the temperature coefficient for large band offsets will be positive.

FF, which is a measure of collection efficiency at maximum power point, was shown in [17] to follow the trends of $V_{\rm oc}$ for small ΔE_c and $J_{\rm sc}$ for large ΔE_c. Accordingly, for small ΔE_c, the temperature coefficient of FF will be proportional to the temperature coefficient of $V_{\rm oc}$. However, for large ΔE_c, the FF follows the trend of current at maximum power point similar to that of $J_{\rm sc}$. Accordingly, the FF improves with temperature because of the increase in probability of carriers crossing the barrier, and hence, its temperature coefficient will be positive.

Finally, the temperature coefficient of efficiency, which is the sum of the temperature coefficients of $V_{\rm oc}$, $J_{\rm sc}$, and FF is significantly affected by the $V_{\rm oc}$ for lower band discontinuities. For these cases, the FF too follows $V_{\rm oc}$ trends. For larger band discontinuity ($> 0.4\,{\rm eV}$) the temperature coefficient is dictated by FF, as over-the-barrier transport of carriers at maximum power point increases with temperature. The analysis in this section predicts that temperature coefficient of efficiency improves with increase in magnitude of ΔE_c. Interestingly, the temperature coefficient might become positive for large magnitudes of ΔE_c, however, the overall efficiency could still be lower than the corresponding values for small magnitudes of ΔE_c. Therefore, there is an optimal band offset considering the tradeoff between efficiency and temperature coefficient, which will be explored in detail using numerical simulations.

III. Numerical Simulations

In Section II, we used the analytical model to explore the variation of temperature coefficient as a function of band discontinuity and interface quality. The model predicts that TCη closely follows the features of TC$V_{\rm oc}$. In this section, we discuss the results of detailed numerical simulations. Current–voltage characteristics of the modeled device were obtained through self-consistent solution of Poisson and drift diffusion equations [27]. From the obtained characteristics, temperature coefficient of $V_{\rm oc}$, $J_{\rm sc}$, FF, and efficiency were estimated. Note that the TCη is estimated directly through (1) and as such, the numerical simulations do not rely on the simplifying assumptions made in the derivation of the analytical model [for example, validity of (2), and also see the discussion on FF in Section II] and hence can be used as a test bed for analytical predictions. As before, initially, we study the effect of conduction band offset ΔE_c at the ESL/Si interface on the temperature coefficient, while keeping Si/HSL interface perfect ($\Delta E_v = 0\,{\rm eV}$ and $D_{\rm it} = 0$). The interface trap density at the ESL/c-Si interface is assumed to be uniform as in the analytical model. Later the effect of band offsets at Si/HSL interface and the combined effect of both the offsets are also discussed. The list of parameters used in simulations is given in Appendix A.

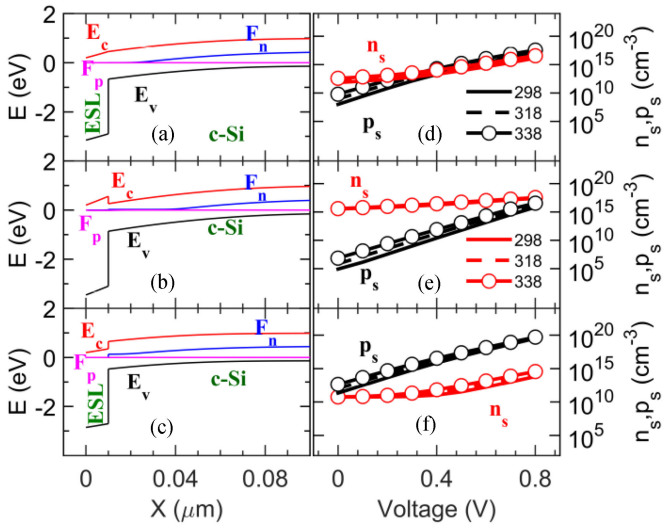

Fig. 3. Effect of ΔE_c on band bending and carrier densities at ESL/c-Si interface with $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$ (numerical simulations, under illumination). (a)–(c) show the energy band diagram for $\Delta E_c = 0\,{\rm eV}$, $\Delta E_c = 0.3\,{\rm eV}$, and $\Delta E_c = -0.3\,{\rm eV}$, respectively, at short-circuit conditions. (d)–(f) show the variation in interface carrier densities n_s, p_s with bias and temperature for the corresponding cases.

The influence of band offset on the interface recombination is highlighted in Fig. 3. Here we consider three cases of ΔE_c and the subsequent effect on interface recombination. A comparison of Fig. 3(a) and (b) indicates that the band bending in Si near Si/ESL interface increases with positive ΔE_c. Accordingly, p_s decreases with an increase in band offset [see Fig. 3(d) and (e)]. As a result, the interface recombination reduces and hence $V_{\rm oc}$ increases as ΔE_c increases. Similarly, comparison of Fig. 3(a) and (c) shows that the band bending in Si decreases with negative ΔE_c resulting in the increase of p_s and decrease of n_s. This again results in the reduction of interface recombination and increase in $V_{\rm oc}$. Further, there is an increase in minority carrier density [p_s in Fig. 3(d) and (e), and n_s in Fig. 3(f)] with temperature. The increase in minority carrier density with temperature leads to an increase in interface recombination and hence reduces $V_{\rm oc}$.

Fig. 4 shows the variation of normalized performance metrics with temperature and ΔE_c. Normalization is done with respect to the corresponding value (same ΔE_c) at STC conditions and then multiplying by 100. Fig. 4(a) shows that the slope for the normalized $V_{\rm oc}$ is more for $\Delta E_c = 0$ and that the slope decreases as the magnitude of ΔE_c increases. This is expected from the analytical model on $V_{\rm oc}$ and supported by the simulation results provided in Fig. 3. For small magnitude of ΔE_c, the $V_{\rm oc}$ is dominated by interface recombination, whose contribution decreases as magnitude of ΔE_c increases. Accordingly, the $V_{\rm oc}$ degradation decreases as magnitude of ΔE_c increases. Normalized $J_{\rm sc}$ [see Fig. 4(b)] remains invariant with ΔE_c for the temperature range under consideration because of the following: 1) the assumption of a constant generation rate; and 2) the fact that over-the-barrier transport of carriers is yet to be

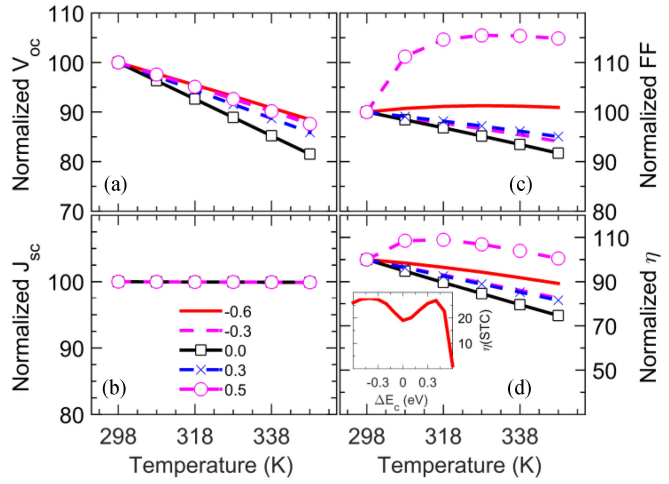

Fig. 4. ESL/Si interface: Effect of ΔE_c and temperature on normalized performance metrics. (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) efficiency of CS Si solar cells for $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$. The labels represent $\Delta E_c = -0.6,\ -0.3,\ 0,\ 0.3,\ 0$, and $0.5\,{\rm eV}$. The inset in (d) shows the effect of ΔE_c on efficiency with $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$.

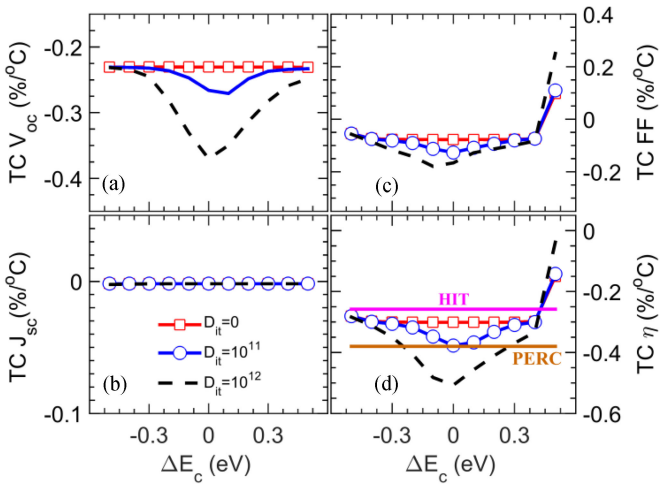

Fig. 5. ESL/Si interface: Effect of ΔE_c on temperature coefficient of parameters (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) efficiency for different $D_{\rm it}\,({\rm cm}^{-2}{\rm eV}^{-1})$ values. The trends are broadly consistent with the analytical model for $V_{\rm oc}$. FF follows the trends of $V_{\rm oc}$ for low values of ΔE_c and for high values of ΔE_c, it increases with temperature because of the increase in current at maximum power point.

significantly influenced by the band offsets—these arguments are consistent with those provided in Section II. Normalized FF [see Fig. 4(c)] follows the trends of $V_{\rm oc}$ for lower values of ΔE_c. For $\Delta E_c = 0.5\,{\rm eV}$, the FF increases with temperature initially and then decreases. This result could be understood as follows: For large ΔE_c, the current at maximum power point conditions at STC is dominated by over-the-barrier transport limitations because of ΔE_c band offset. An increase in temperature results in larger over-the-barrier transport, which leads to better charge collection efficiency, and hence the FF. For still higher temperatures the increase in collection efficiency is counter balanced by the decrease in $V_{\rm oc}$ and this results in the FF peaking to a maximum value and then decreasing [see Fig. 4(c)] [28]–[30]. While the trends indicate that it is beneficial to have large ΔE_c from the perspective of temperature coefficient, we stress that the efficiency could be low for such cases (see inset in Fig. 4(d) for effect of ΔE_c on efficiency at STC with $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$). Accordingly, maximum power output at higher temperature could still be given by an optimum ΔE_c.

Fig. 5 shows the temperature coefficient for all performance parameters as a function of ΔE_c and $D_{\rm it}$. The trends in Fig. 5(a) are broadly similar to that in the analytical model for temperature coefficient of $V_{\rm oc}$ [see Fig. 2(b)]. As explained already in the analytical section (see (5) and Fig. 3), $V_{\rm oc}$ and its temperature coefficient is indeed limited by the interface traps when ΔE_c is low. Further, for larger values of ΔE_c, $V_{\rm oc}$ improves because of the field effect passivation (see Fig. 3) of the interface traps thus improving its temperature coefficient as well. As explained before, this improvement in passivation is because of the increase in band bending with increase in ΔE_c between ESL/Si and the corresponding decrease in the minority carrier concentration at the interface.

The temperature coefficient of $J_{\rm sc}$ [see Fig. 5(b)] at small ΔE_c is zero because of insignificant variation in net carrier generation rate, and the over-the-barrier transport is unaffected for the range of ΔE_c under consideration (as predicted by the analytical model). The trends for the temperature coefficient of FF [see Fig. 5(c)] are similar to temperature coefficient of $V_{\rm oc}$ for most values of ΔE_c. However, for large values of ΔE_c, the current at maximum power point increases with temperature, which leads to an improvement in TCFF. Fig. 5(d) shows the variation of temperature coefficient of efficiency, which follows the trends of $V_{\rm oc}$ and FF. The same figure also highlights a comparison of the temperature coefficient of CS solar cells with that of state-of-the-art PERC and HIT solar cells (*n*-doped bulk Si) [24]. It is evident that unless the band discontinuity is small and the interface quality is very bad, temperature coefficient of CS solar cells can be better than PERC solar cells (of course, the effect of HTL/Si interface should also be accounted for a proper comparison, which will be attempted later). Further, HIT ($\Delta E_c = 0.25\,{\rm eV}$, $\Delta E_v = 0.45\,{\rm eV}$ [3]) cells are almost universally better than both the CS as well as the PERC cells. However, we note that for very large ΔE_c, CS solar cells show better ${\rm TC}\eta$ than even HIT cells. This is a regime where the charge collection efficiency and hence the FF is limited by over-the-barrier transport. Therefore, although the ${\rm TC}\eta$ is better, the efficiency of such cells is still much lower than that of comparable HIT cells.

Till now, the influence of minority carrier extraction interface on the temperature coefficients has been detailed. Here, we extend the same to majority carrier extraction interface (i.e., c-Si/HTL). The effects of temperature and band discontinuity (i.e., ΔE_v) at c-Si/HSL interface on the normalized solar cell performance metrics are shown in Fig. 6. As before, here we assume ideal conditions at ESL/c-Si interface (i.e., zero band offset and no traps). While the trends in $V_{\rm oc}$ degradation with temperature [see Fig. 6(a)] are somewhat similar to the results for minority carrier collection [as discussed in Fig. 4(a)], the trends for $J_{\rm sc}$ variation with temperature is distinctly different [i.e., compare Fig. 6(b) with Fig. 4(b)]. Specifically, the results

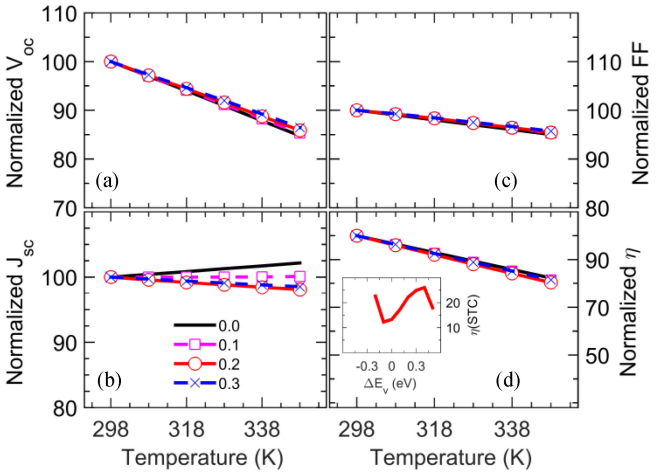

Fig. 6. HSL/Si interface: Effect of temperature on normalized performance metrics (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) efficiency of CS Si solar cells for $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$. The labels represent $\Delta E_v = 0,\ 0.1,\ 0.2,$ and $0.3\,{\rm eV}$. The inset in (d) shows the effect of ΔE_v on efficiency with $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$.

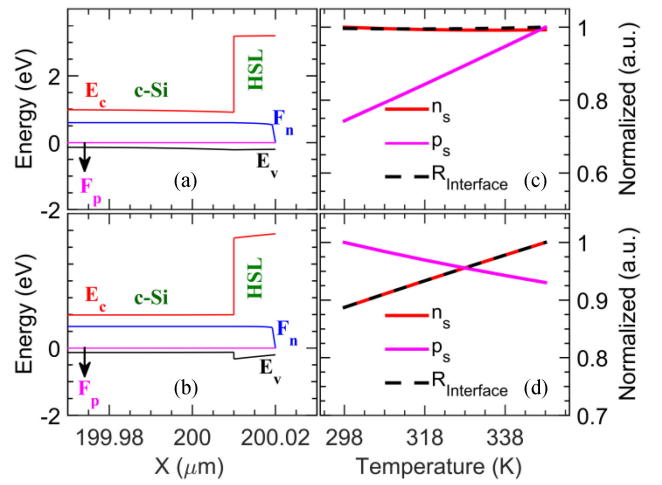

Fig. 7. HSL/Si interface: Effect of ΔE_v on band bending and carrier densities at c-Si/HSL interface with $D_{\rm it} = 10^{12}{\rm cm}^{-2}{\rm eV}^{-1}$ (numerical simulations, under illumination). (a) and (b) show the energy band diagram for $\Delta E_v = 0\,{\rm eV}$ and $\Delta E_v = 0.2\,{\rm eV}$, respectively, at short-circuit conditions. (c) and (d) show the variation in normalized interface carrier densities n_s, p_s, and normalized interface recombination with temperature at short-circuit conditions for $\Delta E_v = 0\,{\rm eV}$ and $\Delta E_v = 0.2\,{\rm eV}$, respectively.

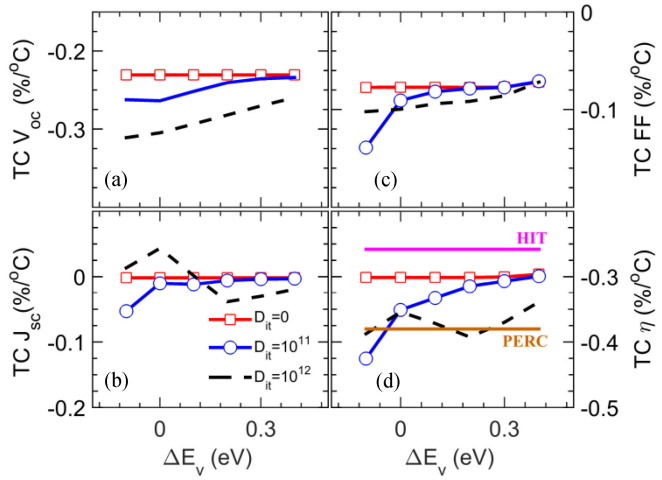

Fig. 8. HSL/Si interface: Effect of ΔE_v on temperature coefficient of performance metrics (a) $V_{\rm oc}$, (b) $J_{\rm sc}$, (c) FF, and (d) efficiency in the presence of interface traps. Because of the variation in $J_{\rm sc}$, the curves for efficiency are different from the corresponding curves for ΔE_c.

indicate a positive temperature coefficient for small ΔE_v. As a result, the FF [see Fig. 6(c)] and efficiency [see Fig. 6(d)] trends are different compared with Fig. 4.

The trends in $J_{\rm sc}$ can be explained by using Fig. 7. Fig. 7(a) and (b) indicates the energy band diagrams for $\Delta E_v = 0\,{\rm eV}$ and for $\Delta E_v = 0.2\,{\rm eV}$, respectively. For these two cases, the variation in interface carrier densities (n_s, p_s) and the net interface recombination are plotted in Fig. 7(c) and (d). Fig. 7(c) shows that for $\Delta E_v = 0\,{\rm eV}$, n_s and the interface recombination remains almost unaffected by the temperature and that the p_s increases with temperature. As a result the collection efficiency improves and hence it leads to an increase in $J_{\rm sc}$ with temperature as observed in Fig. 6(b) for $\Delta E_v = 0\,{\rm eV}$ (positive ${\rm TCJ_{sc}}$). However, Fig. 7(d) shows that n_s (as the bands bend upward) and the interface recombination increase with temperature and lead to a decrease in p_s for $\Delta E_v = 0.2\,{\rm eV}$. This increase in interface recombination with temperature coupled with the decrease in p_s contributes to a reduction in $J_{\rm sc}$ and hence, the temperature coefficient for $J_{\rm sc}$ is negative at higher band discontinuities. Finally, the trends from Fig. 7 indicate that the band bending and hence $J_{\rm sc}$ is affected by the small variations in ΔE_v.

Fig. 8 shows the effect of c-Si/HSL interface quality (ΔE_v, $D_{\rm it}$) on temperature coefficient of parameters for CS solar cell. As the band offset increases, interface recombination decreases and hence the ${\rm TCV_{oc}}$ improves. These trends are similar to the results shown in Fig. 5(a). However, the temperature coefficient for $J_{\rm sc}$ [see Fig. 8(b)] show slight variations (compared with ${\rm TCV_{oc}}$). The difference between the corresponding curves in Fig. 5(b) is because of lower band bending at the PP+ junction between HSL and Si for low values of ΔE_v. Further, the trends in Fig. 7 indicate how ΔE_v can affect the band bending and affect $J_{\rm sc}$ and its variation with temperature (also described in previous paragraph). This results in the wavy nature of ${\rm TCJ_{sc}}$. Fig. 8(c) and (d) shows the variation in temperature coefficient of FF and efficiency, respectively. We find that ${\rm TC}\eta$ broadly follows the trends of ${\rm TCV_{oc}}$. However, for small ΔE_v, the trends are influenced by the ${\rm TCJ_{sc}}$ as well. The comparison with state-of-the-art PERC and HIT cells gives similar inferences as in Fig. 5(d).

The combined effect of interface non-idealities at ESL/Si and HSL/Si interfaces on temperature coefficient is shown in Fig. 9. Here, Fig. 9(a) and (b) shows the variation in temperature coefficient when $\Delta E_c = \Delta E_v = 0\,{\rm eV}$ and $\Delta E_c = \Delta E_v = 0.3\,{\rm eV}$, respectively. For a given interface trap density, the lower band discontinuities result in a larger magnitude of temperature coefficient. Curiously, the same results indicate that the quality of minority carrier extraction layer interface with Silicon is more critical for temperature coefficient of the device than the quality of majority carrier extraction layer interface with Silicon. This is because of the effect of interface recombination on ${\rm TCV_{oc}}$

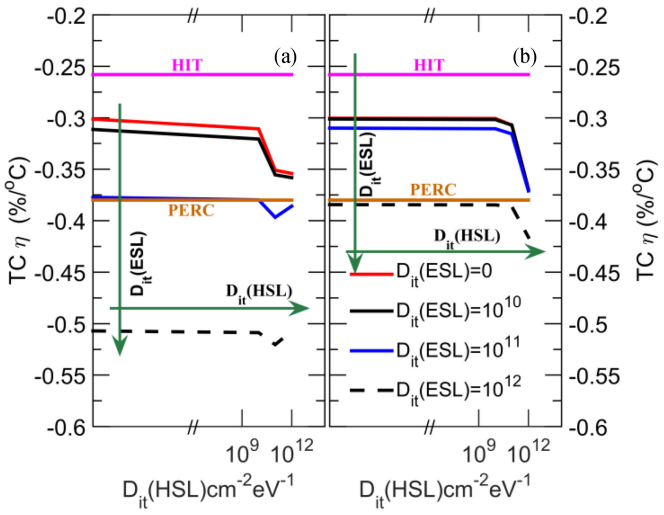

Fig. 9. Effect of traps at both the HSL and the ESL interfaces with c-Si on temperature coefficient for (a) $\Delta E_c = \Delta E_v = 0\,\mathrm{eV}$ and (b) $\Delta E_c = \Delta E_v = 0.3\,\mathrm{eV}$. The quality of minority carrier extraction layer interface with Silicon is more critical for temperature coefficient of the device than the quality of majority carrier extraction layer interface with Silicon.

for these cases. $\mathrm{TCV_{oc}}$ is affected more by the trap states in the minority carrier interface [see Figs. 5(a) and 8(a)] and hence, the temperature coefficient is more critically affected by interface quality at the minority carrier layer. Finally, we note that the effect of interface traps is not cumulative on the temperature coefficient, i.e., for same D_{it}, the sum of temperature coefficients with traps at only one interface (ESL/Si or HSL/Si) is more than the temperature coefficient with traps at both interfaces. This again is because of the fact that the interface quality at the minority carrier extraction layer affects $\mathrm{TCV_{oc}}$ more than that of the majority carrier extraction layer. As a result, for a device with traps at both interfaces, the $\mathrm{TCV_{oc}}$ is dominated by the traps at the minority carrier interface. Accordingly, the TC of device with traps at both interfaces is less than the sum of the TCs of devices with traps at ESL interface (HSL interface has no traps) and HSL interface (ESL interface has no traps). Comparison with the state-of-the-art cells indicates that, while HIT cells may continue to boast excellent temperature coefficients, well-designed CS solar cells might perform better than PERC cells.

IV. Conclusion

To summarize, here we addressed the temperature coefficient of Si-based CS layers as a function of the band discontinuity and interface quality. Through an analytical model, we explored the functional dependence of temperature coefficient on such material and interface properties. These observations were validated using detailed numerical simulations. The results show that the temperature coefficient improves with band discontinuity if the interface quality is imperfect. Further for larger band discontinuity the temperature coefficient improves because of the increase in over-the-barrier transport with temperature irrespective of the interface quality. However, it should be noted that the efficiency at STC for these cases is lower than devices with low magnitudes of band discontinuity. In addition, our results show that the passivation quality at the minority carrier layer interface is more critical than the majority layer interface and that the temperature coefficient is not cumulative, i.e., the temperature coefficient of a structure with traps at both interfaces is better than the sum of the temperature coefficient of separate device structures with traps being present at only one interface (either ESL/Si or HSL/Si). Finally, our results indicate that with appropriate design, CS solar cells can achieve temperature coefficients better than PERC solar cells – although they might still be inferior to HIT solar cells. These interesting insights could be of broad interest to the community towards the optimization of process and material considerations for Si based CS solar cells.

Table I
Parameters Used in Numerical Simulations

Parameter	c-Si	ESL	HSL
N_c (cm^{-3})	3.23×10^{19}	2.5×10^{20}	2.5×10^{20}
N_v (cm^{-3})	1.83×10^{19}	2.5×10^{20}	2.5×10^{20}
Mobility($\mathrm{cm^2V^{-1}s^{-1}}$ (n, p))	1417, 470.5	20, 2	20, 2
ς (n, p)	2,5, 2.2	2,5, 2.2	2,5, 2.2
τ SRH (s)	10^{-3}	10^{-6}	10^{-6}
Radiative Recombination coefficient ($\mathrm{cm^3s^{-1}}$) [32]	1.1×10^{-14}		
Auger Coefficients ($\mathrm{cm^6s^{-1}}$) (n,p) [33]	1×10^{-31}, 0.79×10^{-31}		
Doping (cm^{-3}) n/p	p - 10^{17}	n - 10^{17}	p - 10^{17}

Appendix

A. Parameters used in simulations

The band offset ΔE_c at the ESL/c-Si interface is varied from $-0.6\,\mathrm{eV}$ to $+0.6\,\mathrm{eV}$, while the barrier for holes is kept fixed (2.28 eV). Accordingly, in our simulations, the ESL bandgap varies from 2.8 to 4 eV, which is comparable with the bandgap of TiO_2 ($\sim$3.4 eV). At the c-Si/HSL interface, ΔE_v is varied from -0.1 eV to $+0.4\,\mathrm{eV}$, while the barrier for electrons is kept fixed (2.28 eV). Correspondingly, the HSL bandgap varies from 3.3 to 3.8 eV. For ease of analysis, we have used same dielectric constant (6.2) for both ESL and HSL. We consider uniform distribution of traps at the interface of CS layer and Si. The capture cross section of these traps was assumed as $10^{-16}\mathrm{cm}^{-2}$. The rest of the parameters are provided in Table I.

Further, the temperature dependence of bandgap is given by [31] $E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta}$, where $E_g(T)$ is the bandgap at T and $E_g(0)$ is the bandgap at 0 K, $\alpha = 4.73 \times 10^{-4}\mathrm{eV}\,K^{-1}$, $\beta = 636\,\mathrm{K}$. Phonon scattering (constant mobility model) is considered in numerical simulations [27] as $\mu_{\mathrm{constant}} = \mu_L(\frac{T}{300\,\mathrm{K}})^{-\varsigma}$. The values of μ_L and ς are listed in Table I.

Acknowledgment

The authors acknowledge Center of Excellence in Nanoelectronics (CEN) and National Center for Photovoltaic Research and Education (NCPRE), IIT Bombay for computational facilities.

REFERENCES

[1] J. C. Bean, "Silicon-based semiconductor heterostructures: Column IV bandgap engineering," *Proc. IEEE*, vol. 80, no. 4, pp. 571–587, Apr. 1992.

[2] H. Kroemer, "Heterostructure devices: A device physicist looks at interfaces," *Surf. Sci.*, vol. 132, no. 1, pp. 543–576, 1983.

[3] S. de Wolf *et al.*, "High-efficiency silicon heterojunction solar cells: A review," *Green*, vol. 2, no. 1, pp. 7–24, 2012.

[4] S. Avasthi *et al.*, "Hole-blocking titanium-oxide/silicon heterojunction and its application to photovoltaics," *Appl. Phys. Lett.*, vol. 102, no. 20, pp. 203901, May 2013.

[5] K. A. Nagamatsu *et al.*, "Titanium dioxide/silicon hole-blocking selective contact to enable double-heterojunction crystalline silicon-based solar cell," *Appl. Phys. Lett.*, vol. 106, no. 12, p. 123906, Mar. 2015.

[6] D. Zielke, A. Pazidis, F. Werner, and J. Schmidt, "Organic-silicon heterojunction solar cells on n-type silicon wafers: The BackPEDOT concept," *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 110–116, 2014.

[7] J. Bullock *et al.*, "Lithium fluoride based electron contacts for high efficiency n-type crystalline silicon solar cells," *Adv. Energy Mater.*, vol. 6, no. 14, p. 1600241, Jul. 2016.

[8] J. Bullock *et al.*, "Efficient silicon solar cells with dopant-free asymmetric heterocontacts," *Nat. Energy*, vol. 1, Jan. 2016, Art. no. 15031.

[9] B. Macco, M. F. J. Vos, N. F. W. Thissen, A. A. Bol, and W. M. M. Kessels, "Low-temperature atomic layer deposition of MoOx for silicon heterojunction solar cells," *Phys. Status Solidi—Rapid Res. Lett.*, vol. 9, no. 7, pp. 393–396, 2015.

[10] M. Bivour, J. Temmler, H. Steinkemper, and M. Hermle, "Molybdenum and tungsten oxide: High work function wide band gap contact materials for hole selective contacts of silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 34–41, 2015.

[11] L. G. Gerling *et al.*, "Transition metal oxides as hole-selective contacts in silicon heterojunctions solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 145, pp. 109–115, Feb. 2016.

[12] T. G. Allen *et al.*, "A low resistance calcium/reduced titania passivated contact for high efficiency crystalline silicon solar cells," *Adv. Energy Mater.*, vol. 7, no. 12, p. 1602606, Jun. 2017.

[13] B. Nemeth *et al.*, "Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells," *J. Mater. Res.*, vol. 31, no. 6, pp. 671–681, Mar. 2016.

[14] J. Geissbühler *et al.*, "22.5% efficient silicon heterojunction solar cell with molybdenum oxide hole collector," *Appl. Phys. Lett.*, vol. 107, no. 8, p. 81601, Aug. 2015.

[15] R. Islam, K. N. Nazif, and K. C. Saraswat, "Si heterojunction solar cells: A simulation study of the design issues," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4788–4795, Dec. 2016.

[16] H. Imran, T. M. Abdolkader, and N. Z. Butt, "Carrier-selective NiO/Si and TiO2/Si contacts for silicon heterojunction solar cells," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3584–3590, Sep. 2016.

[17] N. Chatterji, A. Antony, and P. R. Nair, "Interface-dependent efficiency tradeoff in Si-based carrier-selective solar cells," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2509–2516, Jun. 2018.

[18] C. Messmer, M. Bivour, J. Schön, S. W. Glunz, and M. Hermle, "Numerical simulation of silicon heterojunction solar cells featuring metal oxides as carrier-selective contacts," *IEEE J. Photovolt.*, vol. 8, no. 2, pp. 456–464, Mar. 2018.

[19] R. A. Vijayan *et al.*, "Hole-collection mechanism in passivating metal-oxide contacts on Si solar cells: Insights from numerical simulations," *IEEE J. Photovolt.*, vol. 8, no. 2, pp. 473–482, Mar. 2018.

[20] R. A. Vijayan *et al.*, "Numerical simulation of temperature dependence of MoOx based SHJ solar cell," *AIP Conf. Proc.*, vol. 1999, no. 1, 2018, Art. no. 040002.

[21] C. Messmer, M. Bivour, J. Schön, and M. Hermle, "Requirements for efficient hole extraction in transition metal oxide-based silicon heterojunction solar cells," *J. Appl. Phys.*, vol. 124, no. 8, 2018, Art. no. 085702.

[22] C. Wu and J. Chen, "Temperature coefficients of the open-circuit voltage of p-n junction solar cells," *J. Appl. Phys.*, vol. 53, no. 5, pp. 3852–3858, 1982.

[23] S. Ponce-Alcántara *et al.*, "A statistical analysis of the temperature coefficients of industrial silicon solar cells," *Energy Procedia*, vol. 55, pp. 578–588, 2014.

[24] Pansonic Corporation, HIT photovoltaic module. (2017). [Online]. Available: https://panasonic.net/ecosolutions/solar/download/pdf/HIT_N330_N325_Brochure.pdf

[25] J. Nelson, *The Physics of Solar Cells*, 1st ed. London, U.K.: Imperial College Press, 2003.

[26] M. A. Green, "General temperature dependence of solar cell performance and implications for device modelling," *Prog. Photovolt. Res. Appl.*, vol. 11, no. 5, pp. 333–340, 2003.

[27] Synopsys, *Synopsys TCAD*. Mountain View, CA, USA: Synopsis, 2013.

[28] M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Improving the a-Si:H(p) rear emitter contact of n-type silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 106, pp. 11–16, 2012.

[29] R. V. K. Chavali, E. C. Johlin, J. L. Gray, T. Buonassisi, and M. A. Alam, "A framework for process-to-module modeling of a-Si/c-Si (HIT) heterojunction solar cells to investigate the cell-to-module efficiency gap," *IEEE J. Photovolt.*, vol. 6, no. 4, pp. 875–887, Jul. 2016.

[30] G. Nogay *et al.*, "Nanocrystalline silicon carrier collectors for silicon heterojunction solar cells and impact on low-temperature device characteristics," *IEEE J. Photovolt.*, vol. 6, pp. 1654–1662, 2016.

[31] Robert F. Pierret, *Advanced Semiconductor Fundamentals*, 2nd ed. Upper Saddle River, NJ, USA: Pearson, 2003.

[32] W. Gerlach, H. Schlangenotto, and H. Maeder, "On the radiative recombination rate in silicon," *Phys. Status Solidi*, vol. 13, no. 1, pp. 277–283, 1972.

[33] M. A. Green, "Limits on the open-circuit voltage and efficiency of silicon solar cells imposed by intrinsic auger processes," *IEEE Trans. Electron Devices*, vol. ED-31, no. 5, pp. 671–678, May 1984.