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Temperature dependent of the current–voltage (I–V) characteristics of $TaSi_2$/n-Si structure

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ABSTRACT

Tantalum silicide ($TaSi_2$) thin films were deposited on n-type silicon single crystal substrates using a dual electron-gun system and with Ta and Si targets. The electrical transport properties of the $TaSi_2$/n-Si structures were investigated by temperature-dependent current–voltage (I–V) measurements. The temperature-dependent I–V characteristics revealed that the forward conduction was determined by thermionic-emission and space-charge-limited current mechanisms at low and high voltage respectively. On the other hand, the reverse current is limited by the carrier generation process.

1. Introduction

Devices based on silicide compounds/Si have gained great importance due to their wide variety optoelectronic and high-frequency applications [1–3]. The formation of silicide results in displacement of metal/semiconductor (M/S) interface deep into the semiconductor [3].

The refractory metal silicides, such as, WSi_2, $TaSi_2$, $MoSi_2$ and $TiSi_2$ are becoming useful gate and interconnect materials in very large scale integrated circuits (VLSI) [4–6]. Refractory metal silicides have been studied intensively because of their importance in the semiconductor industry. The low resistivity and an excellent chemical stability make them one of the attractive materials for interconnections and low resistance contacts in integrated circuits [7]. They are used as protective layers against oxidation on metallic surfaces at high temperatures [8].

Due to importance of metal silicides in integrated circuit technology, $TaSi_2$ films on Si have received a lot of attention [9–14]. $TaSi_2$ films have p-type conductivity, mobility of 10–30 $cm^3\,V^{-1}\,s^{-1}$ and carrier concentration of $(1–5)\times 10^{13}\,cm^{-3}$ [9]. In our previous works, X-ray diffraction results of $TaSi_2$ thin films show changes in the structure from amorphous to crystalline after annealing at temperature 1173 K [15]. According to XRD analysis, a complete conversion yielding single-phase disilicide $TaSi_2$ was achieved from the sample composition of Ta:Si = 1:2 [15]. This is in agreement with other work in the literature [16,17]. As to the $TaSi_2$ layer, the resistance of the film decreases with increasing annealing temperature. The results indicate that, the conduction in these samples is through an activated process having two conduction levels [15]. However, there is a little experimental information in the literature about current–conduction mechanisms in this devices. The current–conduction mechanisms in semiconductor devices such as metal–semiconductor (MS), metal–insulator–semiconductor (MIS) and solar cells are dependent on various parameters, such as the process of surface preparation, formation of barrier height (ϕ_b) at metal/semiconductor (M/S) interface and its homogeneity, impurity concentration of semiconductor, density of interface states or dislocations, series (R_s) and shunt resistance (R_{sh}) of device, device temperature and applied bias voltage.

In our best knowledge, the reported works on $TaSi_2$/Si lack information about the conduction and mechanisms of

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the devices. The main aim of this study is to investigate experimentally the temperature dependent current–voltage (*I–V*) characteristics of $TaSi_2$/n-Si. The dependence of *I–V* characteristics on the temperature in both forward and reverse bias was studied in an attempt to obtain information on the transport mechanisms of the devices.

2. Experimental details

Single-crystal substrate of n-Si(100), was used. Chemical etching of n-Si was performed with HF: HNO_3: CH_3COOH in ratio 1: 6: 1 for 10 s, then rinsed with deionised water and dried. Thin films of $TaSi_2$ alloys were prepared by simultaneous evaporation of the components (Ta and Si) in a UHV double electron-gun evaporation system [15]. The UHV was provided with a titanium sublimation pump and circulating liquid N_2. The evaporation process was started approximately 2 min before the opening of the shutter and as a result the base pressure which was in the lower 10^{-9} mbar rose to 5×10^{-8} mbar. Formation of stoichiometric $TaSi_2$ on Si-single crystal substrates requires as-deposited films with a Ta:Si thickness ratio of 1:2, which takes into account material densities [15]. The thickness was measured with a quartz monitor, whose tooling factors had to be calibrated from direct x-TEM measurements of the layer widths [15]. The deposited film thicknesses were in the range 500 nm.

The *I–V* characteristics of the fabricated $TaSi_2$/n-Si structure were achieved by measuring the resulted current corresponding to a certain potential difference dropped across the junction, using a conventional circuit for current–voltage measurement. The voltage across the configuration system and current passing through it, were measured simultaneously using a high impedance electrometers (Keithley 617, 616 respectively). The dark current–voltage characteristics were obtained in a complete dark chamber at room temperature or inside a dark furnace in case of measurements at higher temperatures.

3. Results and discussion

The *I–V* characteristic of $TaSi_2$/n-Si structure shows the rectification behavior, which indicates the formation of depletion layer between $TaSi_2$ and Si substrate. The *I–V* characteristic of this structure is shown in Fig. 1. The ratio of the forward current to the reverse current at a certain applied voltage is defined as the rectification factor RR. It is evident from Fig. 1 that the junction exhibits Schottky behavior with RR value of ~19.5 at 1 V.

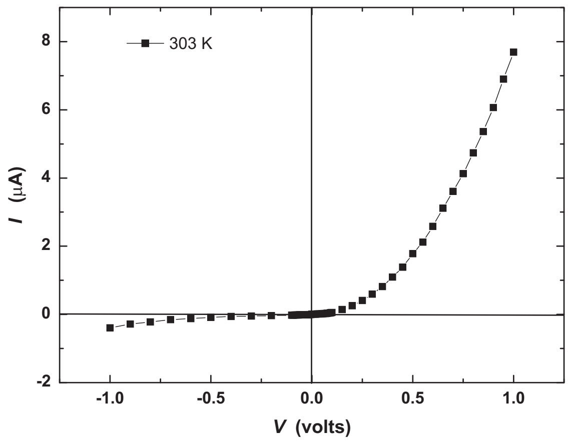

Fig. 1. The *I–V* characteristic of $TaSi_2$/Si structure at room temperature.

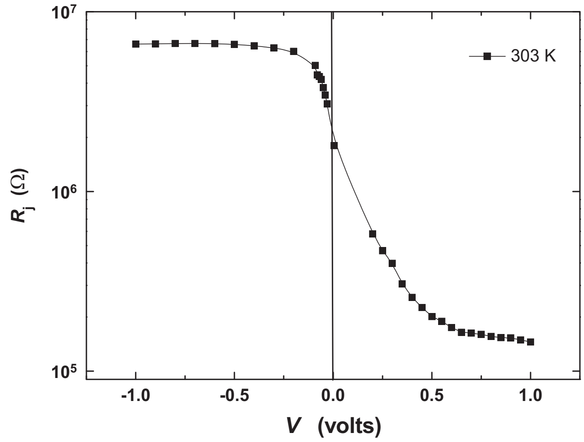

Fig. 2. Variation of junction resistance (R_j) under bias voltage of $TaSi_2$/Si structure at room temperature.

The series (R_s) and shunt resistances (R_{sh}) are determined from the plot of diode resistance (R_j), against voltage (V), where $R_j=dV/dI$, which have been determined from the *I-V* characteristics. A plot of R_j against voltage (V) is shown in Fig. 2. It was observed that at sufficient high forward voltage, the junction resistance approaches to a constant value, which is the series resistance (R_s) (the sum of total resistance values of the resistors in series and resistance in semiconductor device in the direction of current flow). On the other hand, the junction resistance is also constant at high reverse bias, which is equal to the diode shunt resistance (R_{sh}) (a high-precision resistor, which can be used to measure the leakage current flowing through a device). The values obtained for the series and shunt resistances are found to be 153 kΩ and 6.6 MΩ respectively.

The information about the conduction mechanism can be obtained from the *I–V* characteristics at different temperatures. Semilogarithmics plot of *I–V* characteristics for $TaSi_2$/Si structure in the temperature range of 303–353 K are shown in Fig. 3. The RR, R_s and R_{sh} of the $TaSi_2$/Si structure were calculated at different temperatures and listed in Table 1. Increase in R_s with drop in temperature is believed to be a result of the lack of free carrier concentration at low temperatures [18].

The forward *I–V* characteristics as shown in Fig. 3 can be classified into two regions according to the applied voltages. In region II, above ~0.1 V, the forward current deviates from linearity due to the effect of a series resistance and interfacial layer on the $TaSi_2$/Si structure. In region I, below ~0.1 V, the temperature dependence of the forward currents was tentatively analyzed by either the diffusion model, the emission model, or the recombination model [19,20].

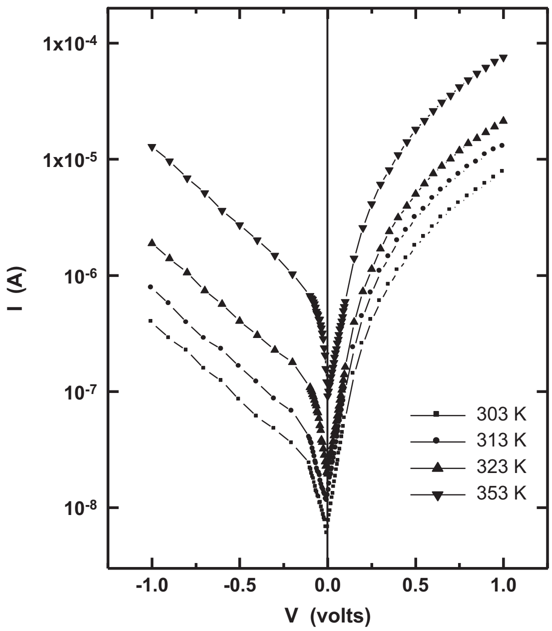

Fig. 3. Semi-logarithmic plot of both forward and reverse current versus applied voltage at different temperatures.

Table 1
Parameters calculated from the I–V measurements.

T (K)	RR	I_o (nA)	n	R_s (kΩ)	R_{sh} (MΩ)
303	19.5	6.01	1.72 ± 0.02	153	6.6
313	16.6	11.27	1.74 ± 0.01	87	3.4
323	11.3	19.93	1.72 ± 0.02	54	1.3
353	5.9	92.77	1.75 ± 0.03	15	0.2

In region I, below ~0.1 V, the temperature dependence of the forward currents was tentatively analyzed by using a simple Schottky model. In this model, the carrier transport occurs across the barrier by thermionic emission, the drift and diffusion of carriers within the depletion region are less important. Then, the current as a function of applied biasing voltages is given by [21]

$$I = I_o\left[\exp\left(\frac{eV}{nk_BT}\right) - 1\right] \tag{1}$$

where n is the diode quality factor, k is the Boltzmann constant, T is the absolute temperature in Kelvin. The parameters I_o and n can be readily determined from the curve (room temperature measurement) shown in Fig. 3 together with Eq. (1). The values of I_o and n are calculated as 6.01×10^{-9} A and 1.72 ± 0.02, respectively. Deviation of n from unity may be attributed to either recombination of electrons and holes in the depletion region, and/or the increase of the diffusion current due to increasing applied voltage [19]. The diode quality factor was found to be almost constant at different temperatures (Table 1). This behavior is believed to be due to the fact that the predominant current mechanism is Schottky emission of carriers over the potential barrier of a device; I_o is expected to have the form [22]

$$I_o \propto T^2 \exp\left(-\frac{e\phi_b}{k_BT}\right) \tag{2}$$

where ϕ_b is the potential barrier height. A plot of ln (I_o/T^2) against $1000/T$ was made to determine the value of ϕ as illustrated in Fig. 4. The value of ϕ_b was found to be 0.45 ± 0.05 eV.

At relative high forward voltage (~0.1 V) different mechanism is operating. As observed from Fig. 5 the current shows a power-law exponent of the form $I \sim V^m$. The slope of the log(I)-log(V) characteristics, is about 2.1 ± 0.01, clarifying that the forward biased current is space-charge-limited (SCLC) controlled by a single dominating trap level. The current in this case is expressed as [23]

$$I \propto V^2 \exp\left(\frac{-E_t}{k_BT}\right) \tag{3}$$

where E_t is energy of the single trap level above the valence band edge, which was calculated to be 0.42 ± 0.05 eV by plotting ln (I) against $1000/T$ as shown in Fig. 6.

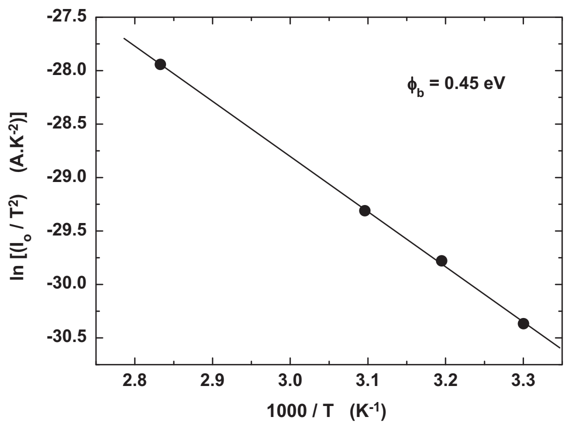

Fig. 4. Plot of ln(I_o/T^2) versus $1000/T$ for $TaSi_2$/Si structure.

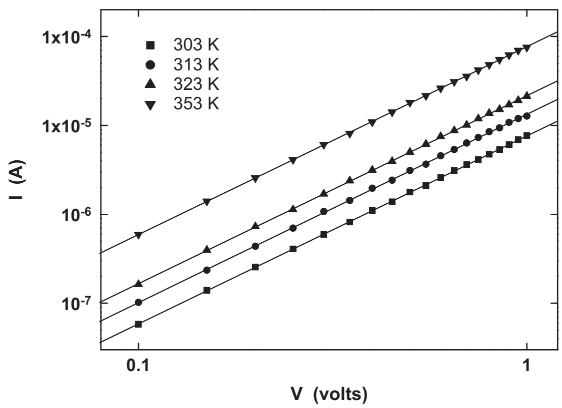

Fig. 5. Variation of log (I) with log (V) at higher forward voltage bias for $TaSi_2$/Si structure.

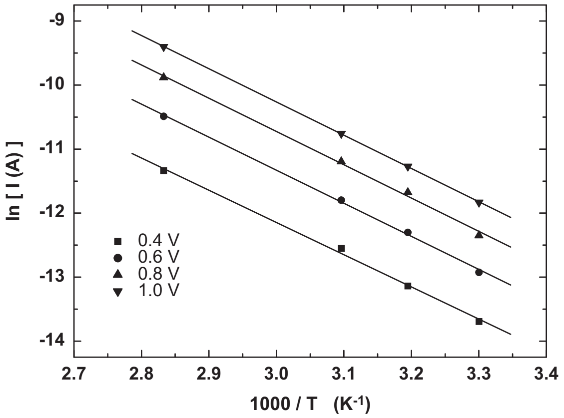

Fig. 6. Variation of ln (I) with 1000/T in SCLC for $TaSi_2$/Si structure at different voltages.

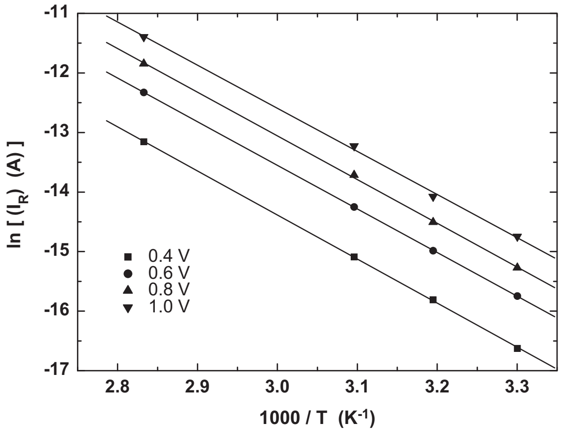

Fig. 7. Plot of ln (I_R) versus 1000/T for $TaSi_2$/Si structure at different voltages.

On the other hand, the reverse current–voltage characteristics of $TaSi_2$/Si structure at different temperatures ranging from 303 to 353 K are shown in Fig. 3. As usual for reverse direction of a rectifier, the current does not nearly depend on voltage. At relatively high voltage, the dependence of the current on voltage is stronger than predicted by pure thermionic emission or Schottky effect. That leads to the assumption that nearly flat reverse I–V characteristics could be fit over a wide range of voltages assuming that generation and recombination of carriers in the Si substrate is the dominant source of the reverse current [24]. The reverse current due to carrier recombination is thermally activated with [25]

$$I_R \propto \exp(-\Delta E/k_B T) \tag{4}$$

where ΔE is the carrier activation energy. The plot of ln (I_R) versus 1000/T is shown in Fig. 7. As shown, the activation energy is determined from the slope of the straight line, which has a value of 0.57 ± 0.04 eV. The obtained activation energy is approximately equal to half the band gap of Si. This suggests that the main source of the reverse current is Si substrate and indicates that the reverse current should be limited by the carrier generation-recombination process.

4. Conclusions

Thin layer of $TaSi_2$ was deposited on n-Si single crystals substrates to fabricate $TaSi_2$/n-Si junction. This junction shows Schottky behavior and exhibit rectifying characteristics with rectification ratio (RR) 19.5 at ± 1 V. The dark current-voltage measurements suggest that the forward current in these junctions involves thermionic-emission mechanism at low temperature. In addition, at high-applied voltage a space-charge-limited current mechanism was active with single trap level, which has a value of 0.42 eV. On the other hand, the reverse current may be reasonably ascribed to a generated current.

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