Extraction of Schottky Barrier Parameters for Metal–Semiconductor Junctions on High Resistivity Inhomogeneous, Semiconductors

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***Abstract*— We present a novel method for the extraction of the relevant electrical and physical parameters of Schottky diodes realized on polycrystalline thin films. The proposed approach relies on a limited set of current–voltage characteristics measured at different temperatures and does not require the previous knowledge of any semiconductor parameter. The procedure provides satisfactory results in terms of relative errors even in the case of nonideal characteristics, including a very large series resistance and strong temperature and bias dependence of both barrier and ideality factor. We tested the approach on both simulated devices and real Cr–poly-Si Schottky diodes.**

***Index Terms*— Metal semiconductor junctions, Schottky barrier measurement, Schottky junction, semiconductor parameter extraction.**

I. Introduction

THE characterization of metal–semiconductor (m–s) contacts has been widely studied and several Schottky barrier height (SBH) extraction methods have been proposed [1]–[5]. The classical approach for extracting diode parameters assumes that the current–voltage characteristics of an m–s junction can be represented by the Schottky equation for thermionic emission

$$I = SA^*T^2e^{-\frac{q\phi}{kT}}\left(e^{\frac{q(V-RI)}{nKT}}-1\right) \tag{1}$$

with S the junction area, A^* the reduced Richardson constant, ϕ the SBH, n the ideality factor, k the Boltzmann constant, T the temperature, and R the series resistance. For pure thermionic emission $n = 1$, whereas n varies in the case of deviations of the electronic transport from the ideal thermionic model [6]. It was also shown that n can be bias and temperature dependent [7]. In high quality and defect-free semiconductors, such dependencies can be often neglected without hampering the accurate extraction of the diode parameters, but must be considered when dealing with polycrystalline and amorphous films [8]. Moreover, the reduced Richardson constant is strongly affected by the semiconductor surface and fabrication process [9] and, consequently, it can be quite unpredictable in highly inhomogeneous substrates. Despite the several fitting and extracting approaches proposed to date, it is still lacking a method well suited for defected, inhomogeneous, highly resistive substrates, particularly in the absence of assumptions for the semiconductor properties. Simple I–V and C–V approaches [1] work for diodes with low series resistance and bias-independent ideality factor. However, these rely on the knowledge of the junction area S, the Richardson constant A^*, or the SA^* product [4]. The method proposed in [2] addresses the issue of devices with large series resistance but it does not handle bias- and temperature-dependent ideality factors. Current–temperature (I–T) Richardson plots are commonly employed for the extraction of the SBH when the SA^* product is unknown. However, they cannot be used for inhomogeneous Schottky barriers whose ideality factor significantly depends on temperature [5]. More complex methods involving numerical fits provide results in good agreement with the theory of inhomogeneous Schottky barriers [5], but they assume an ideality factor expressed, as in (2). The latter only works if the series resistance of the diodes is negligible and if $(dn/dV) \simeq 0$. If these conditions are not satisfied, the differentiation of (1) yields (3). In such particular circumstances, (2) cannot be employed and, consequently, the determination of n is hindered

$$n = \frac{q}{kT}\left(\frac{dlnI}{dV}\right)^{-1} \tag{2}$$

$$\frac{dlnI}{dV} = \frac{q}{kT}\left(\frac{n-\frac{dn}{dV}V}{n^2} - \frac{nR\frac{dI}{dV} - RI\frac{dn}{dV}}{n^2}\right). \tag{3}$$

One of the most complete theory on inhomogeneous Schottky junctions was proposed in [6]. It provides a good model for Schottky barriers affected by significant patchiness, but requires several fitting parameters. As mentioned before, when dealing with devices for which no initial guesses can be made (e.g., doping, density of states, and Richardson constant are unknown), to obtain good results from a pure fitting procedure is extremely difficult. Due to the large number of parameters involved in the fit, it is likely to get different parameter sets corresponding to the experimental data. Optical measurements are probably the most reliable for the extraction of the SBH but cannot provide information on the ideality factor [1]. They rely on photocurrent spectroscopy and can be quite cumbersome due to the low signal

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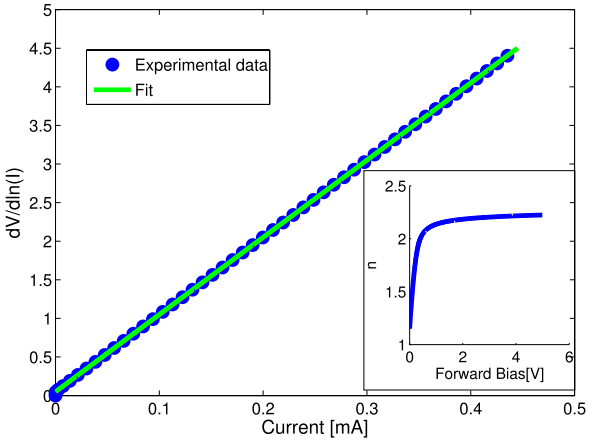

Fig. 1. Extraction of the series resistance with Cheung's method. Calculated $(dV/dln(I))$ (circles) and linear fit (straight line). Inset: calculated n–V characteristics.

level typically produced by sub-bandgap photons in defected materials [10].

II. Extraction Method

In this paper, we present a method that relies on I–V measurements at various temperatures. The I–V characteristics are employed in a multistep procedure: the first step is a fit, to obtain the value of the series resistance; then, the ideality factor is calculated in a small range of the I–V characteristics and, finally, R and n are used to generate a modified Richardson plot for extracting the SBH and the SA^* product. The approach will be discussed and detailed in the following. The procedure starts with the acquisition of a set of I–V curves at various temperatures. Once the I–V curves have been acquired, the series resistance of the diode is extrapolated, as proposed by Cheung and Cheung [3] using

$$\frac{dV}{dln(I)} = RI + \frac{KTn}{q}. \tag{4}$$

The above equation neglects the dependence of the ideality factor on the diode current but, even for devices with large n variations, it is always possible to find a linear portion of the curve $(dV/dln(I))$ to extract the value of R. Fig. 1 shows a calculated $(dV/dln(I))$ and the results of the linear fitting procedure; the corresponding ideality factor versus bias is plotted in the inset. In spite of the n variation with applied bias, the $(dV/dln(I))$ plot is still linear. In this example, we purposely chose a very steep n–V curves to show that, even in critical cases, the Cheung's plot remains linear.

The second step of the procedure focuses on the ideality factor. For large enough bias, V–$RI \gg (q/KT)$ and (1) can be rewritten, as in (5). The $ln(I)$ versus V–RI plot shows a linear trend only for a moderate dependence of n on V–RI. Real diodes usually have such behavior in a certain bias range (usually for large applied voltages) thus allowing the extraction of the ideality factor by a simple linear extrapolation, as shown in Fig. 2(a)

$$ln(I) = ln(SA^*T^2) - \frac{q\phi}{KT} + \frac{q(V-RI)}{nKT}. \tag{5}$$

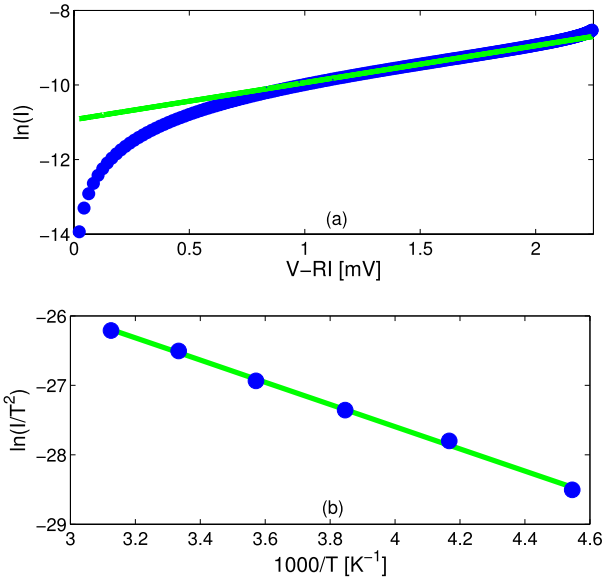

Fig. 2. (a) Extraction of the ideality factor. Calculated $ln(I)$ (circles) and linear fit (straight line). (b) Calculated corrected Richardson plot (circles) and linear fit (straight line).

The obtained ideality factor can be trusted only in the small bias range where the linear fit actually reproduces the $ln(I)$ versus V–RI trend. In particular, we selected a single bias point where the linear extrapolation best fits the curve and used the corresponding voltage and current.

A complete set of R, n, V, I, and T values can be obtained by repeating the first two steps for all temperatures. Such values are, subsequently, employed for computing a modified Richardson plot as in the below and Fig. 2(b)

$$ln\left(\frac{I}{T^2}\right) - ln\left(e^{\left(\frac{q(V-RI)}{nKT}\right)} - 1\right) = ln(SA^*) - \frac{q\phi}{KT}. \tag{6}$$

Data can be linearly fit versus $1/T$ to extrapolate both the SBH and the SA^* products. As in the standard Richardson extraction, the obtained barrier height is a 0-K SBH and shall be considered temperature independent. This approximation can be quite substantial for highly inhomogeneous substrates [8]. If the barrier height is temperature dependent, (6) can be rewritten as [1]

$$ln\left(\frac{I}{T^2}\right) - ln\left(e^{\left(\frac{q(V-RI)}{nKT}\right)} - 1\right) = ln(SA^*) + \frac{q\xi}{K} - \frac{q\phi_0}{KT} \tag{7}$$

where ξ is the linear SBH temperature coefficient and ϕ_0 is the extrapolated 0-K SBH. The extrapolation of SA^* is hindered by the presence of ξ. The stronger the dependence of the SBH on temperature, the larger the difference between the ideal SA^* product and the result of the linear fit.

A further result of the extrapolation by means of (7) is the calculation of the diode saturation current from

$$I_s = SA^*T^2e^{\frac{-q\phi_0}{KT}} \tag{8}$$

$$n(V) = \frac{q(V-RI)}{KTln\left(\frac{I}{I_s}+1\right)}. \tag{9}$$

TABLE I
SIMULATED DIODES PARAMETERS

	ϕ[eV]	Area[cm^2]	A*[$\frac{A}{cm^2K^1}$]	R[Ω]	n
D1	0.58	1e-8	75	5e-3-0.005T	2
D2	0.88	50e-6	100	2e7-2T	1.7
D3	0.62	714e-6	70	200-0.01T	3.5
D4	0.24	5e-7	50	10-0.001T	1.5
D5	0.91	1.2e-6	100	1e7-2T	3

The calculated I_s can now be employed for extrapolating the bias-dependent ideality factor according to (9) and so the procedure is complete.

It is worth noting that the use of a voltage-dependent ideality factor extends the method capabilities to different m–s behaviors, from standard thermionic emission to structures dominated by field emission mechanisms. As stated before, the only parameter with a high degree of uncertainty is the SA^* product because of the unknown temperature dependence of the SBH. However, some assumptions can be safely made at this point on the characteristics of the diode. According to Tung's theory, the patchiness of the Schottky barrier yields a junction with a mean SBH (i.e., the 0-K SBH obtained through the extraction procedure) and an active surface that can be quite different from the actual m–s area. Using a simplified version of Tung's theory, we can attribute the difference between the ideal and the extrapolated SA^* products to the temperature dependence of the SBH. Therefore, it is possible to extract an approximated $\phi - T$ characteristic by means of

$$\phi(T) = \frac{KT}{q} ln\left(\frac{SA^*_{\text{ideal}} T^2}{I_s}\right) \tag{10}$$

where SA^*_{ideal} is the product of the nominal m–s junction area (which is usually well known) and an arbitrarily chosen Richardson constant. Due to the logarithmic dependence, the resulting error on the $\phi - T$ calculation is less than 10% even with an error of one order of magnitude in the initial guess of the Richardson constant.

III. METHOD VALIDATION

To test the validity of the proposed extraction method, we ran several simulations. The first set included ideal diodes, with temperature- and voltage-independent ideality factor and SBH. As for the series resistances, we considered a linear temperature coefficient and values ranging from 1 to 10^7 Ω. Table I shows a set of typical diode parameters used to generate the I–V characteristics.

For each simulated diode, six I–V curves with temperatures from 220 to 320 K were generated and processed as explained in the previous section. The error was evaluated according to (11), where p can be SA^*, ϕ, n or R, and p^* indicates the nominal value of the parameter (Table I)

$$e_p = 100 \cdot \frac{p - p^*}{p^*}. \tag{11}$$

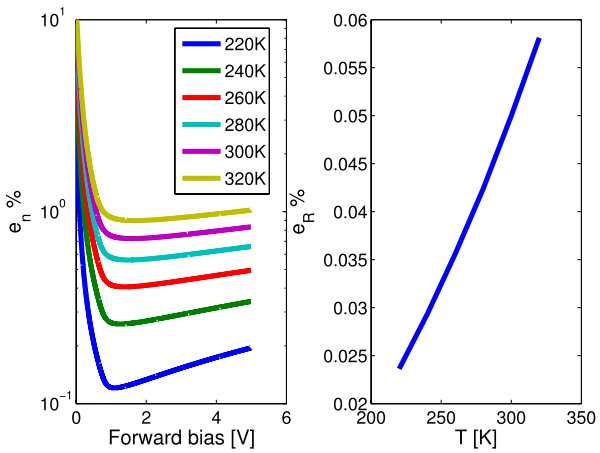

Fig. 3. Error plots for diode D1. Ideality factor versus bias (left) and resistance versus temperature (right). Other errors are $e_{SA^*} = 2.4\%$ and $e_\phi = 0.5\%$.

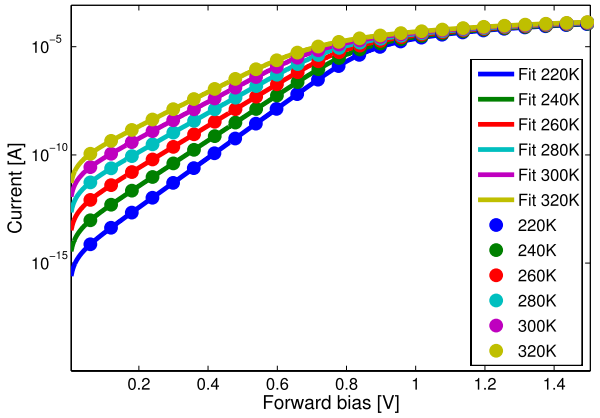

Fig. 4. Simulated (circles) and fitted curves (straight lines) for diode D1.

TABLE II
D1–D5 FITTING ERRORS (%)

	e_ϕ	e_{SA^*}	e_R [min max][1]	e_n [min max][2]
D1	0.22	0.33	[-2e-3 5.8e-2]	[5.8e-6 1.5]
D2	0.12	0.93	[1.7e-2 4.7e-2]	[5.4e-6 1.3]
D3	0.21	2.16	[8e-2 0.2]	[1e-5 1.74]
D4	5.54	0.23	[7e-3 0.39]	[0.27 13.64]
D5	0.023	9.81	[1e-2 3.7e-2]	[1.6e-7 0.26]

1: for T from 220K to 320K; 2: for V from 0V to 5V

Fig. 3 shows the calculated errors for n and R for diode D1. Except for a very narrow bias range in the low bias regime, all extracted parameters match the corresponding nominal ones. Fig. 4 shows good agreement between I–V curves calculated with the parameters in Table I and the corresponding curves obtained with the extracted parameters.

We obtained similar results for all simulated diodes, as visible in Table II.

All extracted values for ϕ are in good agreement with the expected ones, with a maximum error of about 5%. As for the ideality factor, the errors drop below 1% at bias voltages greater than 0.5 V. Errors on the series resistance

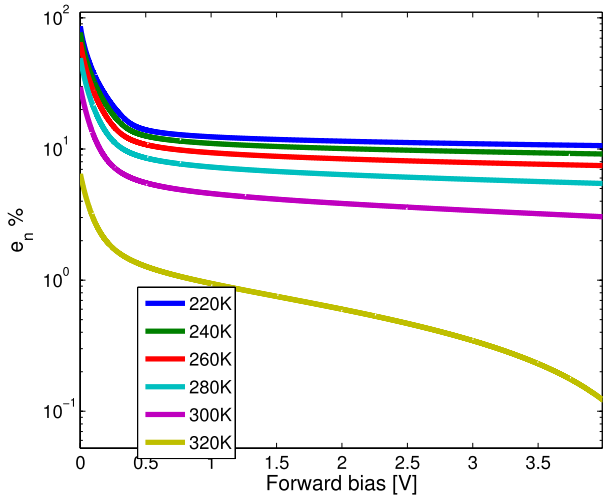

Fig. 5. Ideality factor determination error for diode D6.

TABLE III
D6–D8 FITTING ERRORS (%)

	$e_{\phi 0}$	e_{SA^*}	e_R **[min max]**[1]	e_n **[min max]**[2]
D6	8	359	[0.26 0.54]	[0.25 85]
D7	2	112	[0.19 0.21]	[1.2 30]
D8	1	31	[0.02 0.18]	[0.4 32]

[1] for T from 220K to 320K; [2] for V from 0V to 5V

are always negligible. The SA^* product exhibited a maximum error below 10%. The results in Table II compared with the real parameters in Table I suggest a correlation between high values of e_{SA^*} and the magnitude of the ideality factor.

Until now, we showed the results regarding diodes with almost ideal characteristics; the proposed method, however, should work also with diodes far from being ideal. To check the performance of our procedure when dealing with highly nonideal diodes, we simulated several Schottky junctions with temperature-dependent SBH and resistivity as well as bias- and temperature-dependent ideality factor.

The results shown in Table III demonstrate (even for highly nonideal diodes) the ability to extract the 0-K SBH with an error lower than 10%, and the ideality factor with an error lower than 20% for a forward bias greater than 0.5 V (Fig. 5). For applied biases lower than 0.5 V, the e_n error can be very high but, in this case, due to the large voltage drop on the series resistance, the diode is barely conducting. Unfortunately, we obtained large SA^* errors (Table III). As already discussed, such large errors stem from the temperature dependence of the SBH. We evaluated the $\phi(T)$ by means of (10) and then calculated e_ϕ at each temperature; the results are shown in Fig. 6.

The e_ϕ versus T plot shows that, even for large overestimations of the SA^* product, the accumulated error in the $\phi(T)$ calculation is still lower than 30%. It should be pointed out that, using the nominal S value in (10), we overestimate the SA^* product. Due to the patchiness of the Schottky barrier, in fact, the actual junction area is smaller than the nominal one. Therefore, we suggest to deliberately

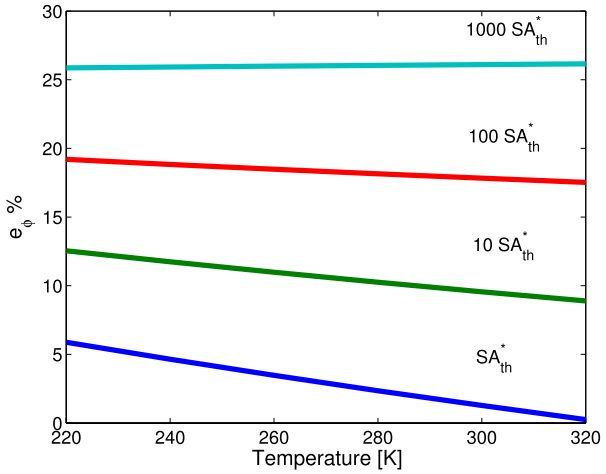

Fig. 6. e_ϕ versus temperature for various SA^* values for diode D6.

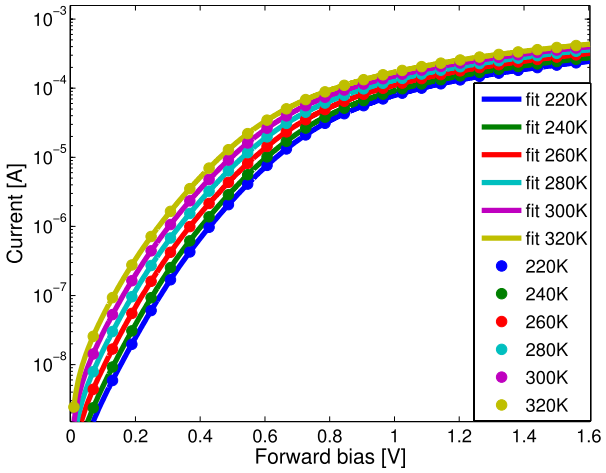

Fig. 7. I–V curves of a Cr–poly-Si Schottky junction at various temperatures. Measured (circles) and calculated (straight lines) characteristics.

introduce an underestimation of the Richardson constant to reduce the final error on $\phi(T)$. Finally, we like to stress that, even though the procedure introduces appreciable errors during the determination of the SA^* product, it is able to extract the SBH, the ideality factor, and the series resistance with very high accuracy.

IV. CHARACTERIZATION OF Cr–POLY-SI DIODES

We also tested our method on a set of real Schottky diodes; the junctions were made of chromium evaporated on a (recrystallized by excimer laser) polycrystalline intrinsic silicon film. The fabrication details are reported elsewhere [11]. Because of the low conductivity of the substrate (no dopants were intentionally added during the silicon deposition), the diodes exhibited a large series resistance whereas, due to the substrate polycrystallinity, the Schottky junctions were quite inhomogeneous. Fig. 7 shows the experimental and simulated I–V characteristics for a typical diode at various temperatures; the curves were acquired with a Keithley SMU236 and a nitrogen cooled

TABLE IV
Cr–POLY-Si DIODES PARAMETERS

	A	B	C	D	E
ϕ_0 [eV]	0.26	0.08	0.2	0.11	0.29
ϕ [eV]	0.74	0.72	0.7	0.7	0.7
SA^* [AK^{-1}]	4.36e-9	5.94e-12	3.58e-10	8.17e-12	2.5e-9
$R[\Omega]$	2.17e3	2.15e3	6.37e3	4.57e3	6.98e3
n	2.75	2.88	2.9	2.95	2.75

ϕ R and n are calculated at 300K

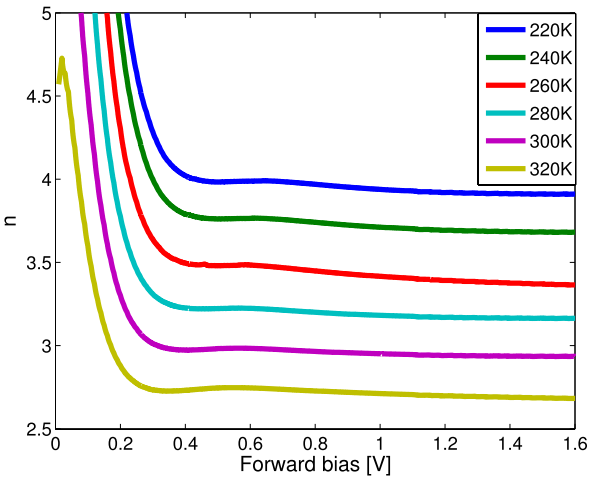

Fig. 8. Ideality factor versus applied voltage at various temperatures.

cryostat on diodes with various junction areas. All diodes were fabricated on the same substrate with the same process.

Fig. 7 clearly shows that, after the extraction procedure, the calculated I–V curves perfectly fit the measured characteristics. This is expected since the proposed extraction method calculates the Schottky barrier parameters by optimizing the current values with respect to the measured curves. The results of the extraction procedure are shown in Table IV for devices with various areas ranging from $2.4 \cdot 10^{-4}$ to $26 \cdot 10^{-4}$ cm^2 (labeled from A–E, with A corresponding to the largest device). The extracted SBH ϕ at room temperature is nearly the same for devices of different sizes, even though ϕ_0 shows a relatively high degree of change. The ideality factor n at 300 K is almost the same, as well. All diodes exhibit a positive SBH temperature coefficient and a negative n temperature coefficient. Such behavior was previously observed in inhomogeneous silicon Schottky junctions [5] and can be associated to a Gaussian distribution of patches with low SBH [6]. Extracted ideality factors versus applied bias show the dependence of n on temperature, as visible in the set shown in Fig. 8.

Fig. 9 compares the calculated (straight lines) and measured (circles) I–V characteristics for various device areas. The good agreement between the model and experimental data demonstrates that the junction area affects neither the values of the extracted parameters nor their accuracy. It should be noted that the method works despite the poor measured current scaling with respect to the junction area visible in Fig. 9.

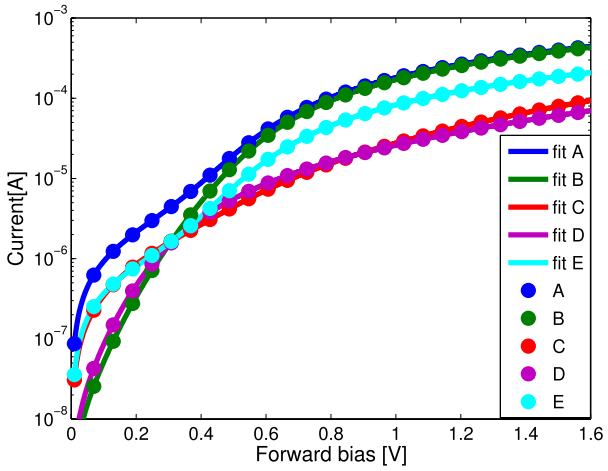

Fig. 9. I–V curves of a Cr–poly-Si Schottky junction with various areas. Measured (circles) and calculated (straight lines) characteristics.

We attribute such behavior to the inhomogeneity of our polysilicon substrate. In particular, whereas the short-range inhomogeneity accounts for the Schottky barrier patchiness and the low effective area of the device, the long-range inhomogeneity makes the device currents uncorrelated to the geometry. Therefore, the large dispersion of the extracted SA^* products can be considered a consequence of such a long-range inhomogeneity and not as an issue of the method.

V. CONCLUSION

We presented a method for the extraction of the Schottky barrier parameters on the basis of a relatively small set of I–V measurements at various temperatures. Unlike other approaches, it can be employed for the analysis of Schottky diodes realized on substrates with completely unknown physical characteristics. Even in the case of very large series resistance and strong temperature and bias dependence of the SBH and the ideality factor, the proposed method can still provide useful results with low errors (less than 20%), thus proving to be a fast and reliable way to characterize nonideal devices. We tested our approach on both *ad hoc* simulated and actually fabricated Cr–poly-Si Schottky diodes.

In simulated junctions, the method gave good results and proved its validity. In actual devices, the approach yielded results in good agreement with the theory of inhomogeneous Schottky barriers.

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