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Thermally Robust High-Resistance Layers on Low-Resistance Silicon Synthesized by Molecular CO^+ Ion Implantation

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Using nanoscale inclusions of a wide-band SiC semiconductor and SiO_2 dielectric formed in CO^+ molecular ion-implanted (COII) layers allows creating highly resistive regions inside a moderate-doped silicon substrate. Contrary to the well-known implanted proton or argon-ion insulation, where the high resistance is provided by the unstable radiation defect Fermi-level pinning, such two-type antidots form a bend of the silicon bandgap on the heteroboundaries around them, similar to the insulating layer in the p−n junction, and guarantee the absence of mobile charge carrier transport at a certain concentration of antidots and working temperatures below 400 K. These insulating regions save their properties even after hard thermal treatment (1400 K). Moreover, a gas blistering suppression is observed for the silicon-on-insulator (SOI) wafers with an ultrathin (10–40 nm) buried oxide (BOX). SIMS measurements demonstrate the strong mobile impurity accumulation at the COII region during subsequent thermal treatments.

1. Introduction

To decrease signal interconnections in photonic and radio frequency (RF) silicon integral circuits (ICs) produced on silicon-on-insulator (SOI) structures, high-resistivity (HR) silicon wafers with a trap-reach layer (TR) are often used.[1] However, the cost of such substrates is usually much higher than that of standard Si wafers. Moreover, the quality of large-diameter HR silicon is still worse than that of Czochralski silicon (Cz-Si). Another way to diminish the RF interconnection or increase the resistance is using thick HR epitaxial layers on the Cz-Si wafers with intrinsic gettering of metals in a silicon wafer.[2,3]

The use of ion beam techniques is a very attractive method to adjust layer properties. It is essentially important for surface patterning. In addition, the proton implantation in semiconductors was aimed at increasing the resistivity of standard gallium arsenide substrates for the manufacture of radio frequency devices. It consists of breaking polar covalent bonds and creates a large density of compensating defects. In silicon MOSFET structures or solar cells, such defects also capture the charge carriers at the Si/SiO_2 interface of the semiconductor and the oxide, which leads to a decrease in the conductivity of an inverted or enriched layer and a decrease in the leakage currents induced by charges in the oxide. The main disadvantage of the method is the impossibility of its use in CMOS technology due to the low thermal stability.[4,5] Silicon recrystallizes and recovers its resistivity above 600 °C, as well as it leaks along the oxide.[5]

Further improvement of epilayer properties has been demonstrated recently by the multielement molecular ion implantation in Cz-Si wafers before the thick epitaxial layer overgrowth.[6–10] These authors implanted molecular hydrocarbon (C_xH_y), methyloxidanyl (CH_3O), or cyanide (CH_4N) molecular ions at moderate fluences (1–5) × 10^{15} cm^{-2} as the related multielement gettering layers. They proved successful gettering in the implanted layers of not only metal impurities such as Fe or Cu, but even hydrogen atoms at 10^{18} cm^{-3} concentration after silicon epitaxial layer overgrowth and furnace annealing at 1100 °C. The authors showed that carbon atoms formed SiC precipitates, whereas oxygen or nitrogen atoms are responsible mainly for the extended defect formation.[6–10] They did not investigate the oxygen or nitrogen atom roles in the silicon oxide and nitride gettering properties.

The objective of our study was to investigate the properties of silicon and SOI wafers both with high-*k* or silica BOX and substrate layers after high-fluence (5–30) × 10^{15} cm^{-2} CO^+ molecular implantation for using them instead of HR-TR Si or SOI wafers.

2. Si and SOI Sample Fabrication

2.1. N- and P-type Silicon Wafers Implanted by CO^+ Ions

The gettering of mobile gas atoms and conductivity compensation with carbon and oxygen precipitates in the 500 μm n- and

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p-type silicon substrate near the surface were used to decrease the sheet conductivity in the implanted layers, including local regions. The Si substrates were implanted by CO^+ and N_2^+ ions (COII) with the energy of 90 and 200 keV into thermally oxidized Si substrates through a 40–60 nm thick SiO_2 layer prior to annealing. CO_2 gas was used in the Bernas ion gas source for producing of the molecular ion beam. The N_2^+ ion fraction in the ion beam did not exceed several percent and was estimated by the atomic ion current ratio $I_{N+}/I_{C+} = 2\%$. The ion ranges in SiO_2 for the energy $E = 90$ keV are almost equal to the ranges in silicon, where the ranges for C^+, N^+, and O^+ ions in the molecular mass of $m = 28$ a. m. u. were 118, 120, and 127 nm, respectively. A different silica layer thickness provides a different position of implanted species relative to the Si/SiO_2 interface and its different diffusional redistribution during high-temperature treatment at $T = 1100\,^{\circ}C$.

2.2. SOI Wafers with CO^+ Ion-Implanted Silicon Substrates

Similar to the Smart Cut process, flows were used for producing SOI structures (S-SOI and D-SOI) with a different layer transfer, as shown in **Figure 1**. The COII getter layers were created on an IBS-200 implanter by the irradiation of virgin and oxidized silicon wafers with CO^+ and N_2^+ ions at energies $E = 90$ and 200 keV and fluence $\Phi = (0.5–3.0) \times 10^{16}$ at $T_{imp} = 100–300\,^{\circ}C$ and the 7° angle of incidence. The H_2^+ ($E = 120$ keV) ion implantation into the donor wafers, bonding, and thermally induced cleavage by SmartCut or DeleCut processes in the vacuum chamber formed the SOI structures (Figure 1).[11] The corresponding SOI structures will hereinafter be referred to as S-SOI and D-SOI with a COII getter. The ranges of H^+ ions with the energy of 60 keV and also for C^+, N^+, and O^+ with the energy of 200 keV for molecular ions with the mass of $m = 28$ a. m. u. were 550, 247, 244, and 265 nm, respectively. The projectile ranges for the 90 keV molecular ions were presented earlier. The molecular ion energies provided gettering diffused impurity atoms by defects either in the transferred (active) 500 nm-thick Si layer or at a similar depth in the p- (0.3–0.5 and 20 Ohm cm) and n-type (1–5 Ohm cm) silicon substrates under the thermal oxide (BOX) during the furnace (FA) or rapid thermal annealing (RTA). Silicon films in SOI structures were then thinned by the subsequent steps of chlorinated oxidation at the 1100 °C/etching (O/E) of the oxide in the 1% HF solution to a final SOI layer thickness of 10–200 nm.

When such a getter was formed in the substrates of SOI structures, the implantation of CO^+ and N_2^+ ions was conducted in HfO_2 covered or thermally oxidized Si substrates through a SiO_2 layer of 20 to 350 nm thick prior to bonding. The ion ranges in SiO_2 for the energy $E < 100$ keV are almost equal to the ranges in silicon. Some silicon substrates with SOI structures were fabricated without a COII getter for control purposes.

Before vacuum bonding, the pairs of wafers were treated in RF N_2/O_2 plasma for 60 s. The silicon layers' transfer from the n-type silicon wafers with resistivity $\rho = 1–5$ Ohm cm ($4–8 \times 10^{14}\,cm^{-3}$), doped with hydrogen on to the 100 mm oxidized silicon wafers with the 50 nm-thick thermally grown silicon dioxide on the surface, was conducted according to the technology using direct bonding in vacuum at ≈100 °C to increase the bonding area.[11] The transfer of a Si/SiO_2 or only Si layer to an oxidized silicon substrate occurred during the thermal cleavage ($T = 450\,^{\circ}C$).

The SOI wafers obtained this way were subjected to subsequent annealing in argon and oxygen ambient at 650–1100 °C (FA and RTA) and a step-by-step O/E thinning of the silicon layer. Moreover, these thinned S-SOI and D-SOI wafers with an ultrathin (UT) (10–40 nm) SOI and buried oxide (BOX) layers and COII getter demonstrate a gas blistering suppression in comparison with the SOI wafers without a getter. The layer

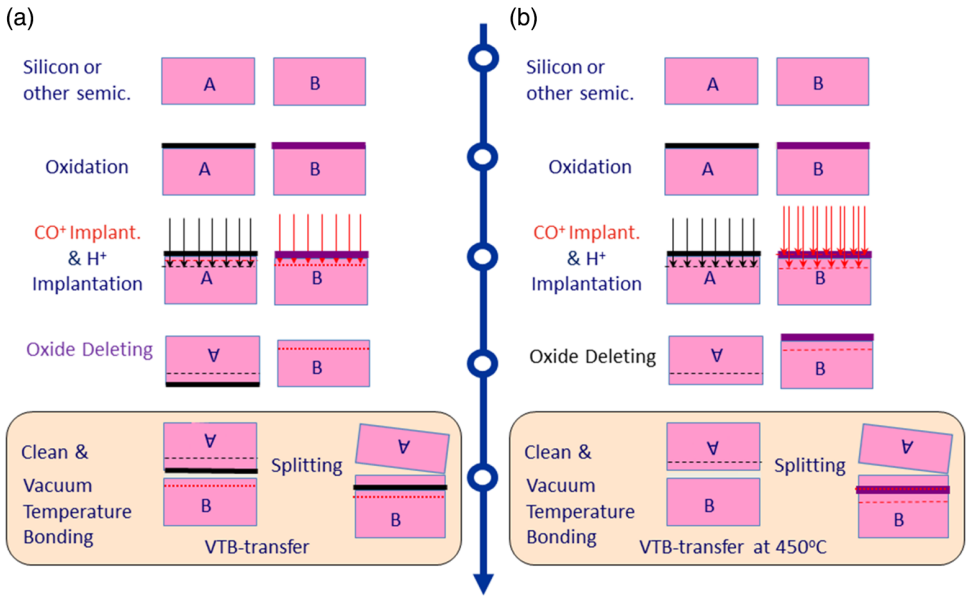

Figure 1. The gettering layer formation by the CO^+ molecular ion implantation with the fluence $\Phi = (0.5–3) \times 10^{16}\,cm^{-2}$ in the Si substrate for a) S-SOI and b) D-SOI structures.

thicknesses of all SOI structure layers were monitored by the spectral ellipsometry (SE) method after each annealing or etching step.

3. Properties of Si and SOI Structure with a Getter

3.1. Properties of Si Substrate with a Getter

The detailed distribution profiles of implanted or impurity atoms in the COII layers were determined by the method of secondary-ion mass spectrometry (SIMS) of negatively charged ions sputtered by the initial Cs^+ ions with the energy of 1 keV on the TOF.SIMS 5 (IONTOF) facility (**Figure 2**). Before measurements, the upper silica layer was etched in some cases to increase the resolution of the SIMS method in the analysis of border regions of a silicon substrate underneath containing a COII getter. The electrophysical properties were studied on the mesastructures by means of the $C-V$, $I-V$, and four-point probe technique in Van der Pauw geometry with tungsten probes, which were 100 μm spaced and had a 20 μm tip radius and 60 g pressure force, as contacts. The backside contacts to the substrate were the InGa paste.

In Figure 1a,b are the results of determining the distribution profiles and concentrations of impurities in the Si subsurface layers by the SIMS method. The origin of the sputtered SiN ions in the SIMS spectra is associated with a significant part of the N_2^+ ion current in the total ion current, but there is practically no nitrogen impurity inside the SiO_2 oxide (Figure 2a). Probably, the CO^+ ion implantation of Si was accompanied by the uncontrolled coimplantation of N_2^+ ions from the residual atmosphere in the source, as evidenced by the similarity of the C and SiN profiles in the silicon substrate and at the SiO_2/Si boundaries. This cannot be explained by the SIMS measurement effects, in particular by the sputtering of C_2H_2O molecules, as the SiN, H, and C profiles do not correspond to each other in the thin SiO_2 layer. Moreover, sputtering in the SIMS setup was conducted by a primary beam of Cs^+ ions, which provided the necessary m/e resolution and separation of these molecules.

The depth-dropping profiles of the fluorine and chlorine atoms, as well as the ^{16}O isotope deficiency in the upper silica layer, are associated with the thermochemical processing of the wafers prior to the SIMS measurements. Attention is paid to the high content of hydrogen atoms and the low content of carbon atoms, $\approx 10^{19}$ cm^{-3}, in the SiO_2 layers, and this also corresponds to the data in Figure 2b, where the C atoms mainly migrate to the heteroborders without remaining at the path depth in silicon dioxide. In addition to the silica layer, the hydrogen gettering occurs at the boundaries with SiO_xC_y or SiO_2/SiC precipitates, as evidenced by the peaks of hydrogen concentrations both at the SiO_2/Si boundaries and at a depth of ≈110 nm corresponding to the range of carbon and oxygen ions in the Si substrate (Figure 2). In the thick silica layer (not presented here), no more than 10^{15} cm^{-2} of the carbon layer concentration remains and about 4×10^{15} cm^{-2} on the SiO_2/Si border. The C atoms escape from the silica layer and three SiC nucleation peaks at the center and a possible border position between the crystalline and amorphous Si layer, formed due to a high dose implantation inside the bulk silicon, also correlate with the data.[12,13] It is interesting to note that there is not a strong C and O atom correlation inside silicon. Similar reasons are responsible for the shape of the SIMS profile of the detected secondary SIN ions. The similarity of nitrogen distribution to the profile of ^{12}C atoms, with the exception of the SiO_2/Si boundaries, indicates the coimplantation of N_2^+ ions with CO^+ ions, as well as their coprecipitation with carbon atoms.

The four-point probe technique in the Van der Pauw (VdP) geometry was used for sheet resistance measurements on the surface layers with the COII getter, as well as on the backside of Si wafers. The results are shown in **Table 1**.

The electrophysical properties of Si and SOI mesa structures were determined from the $C-V$ measurements on an Agilent E4980A measuring module with a W-probe and the InGa paste as a low-voltage potential electrode on the substrate backside (**Figure 3**) and the $I-V$ characteristics with tungsten probe electrodes with InGa drop at the end of tungsten needle electrode (tip radius: 20 μm) with a clamping force of 60 g as the anode and (back-gate) gate cathode, which was a silicon substrate with the ohmic InGa contact (**Figure 4**). The $C-V$ data evidence a

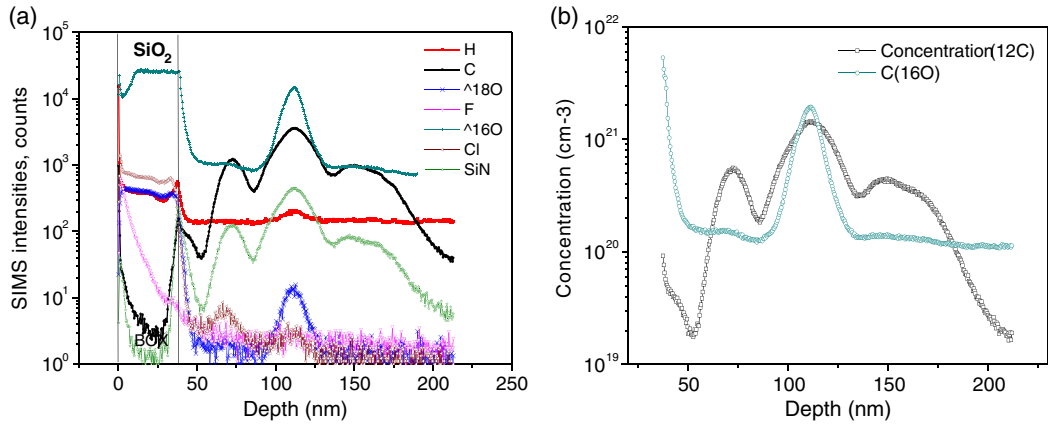

Figure 2. a) SIMS profiles of the impurity atom distribution in UTBB D-SOI structures implanted with CO^+ at energy $E = 90$ keV and fluence $F = 1 \times 10^{16}$ cm^{-2} into the Si substrate through the SiO_2 layer (40 nm) and annealing at 1100 °C for 2 h. b) The same but for the concentration profile of the ^{12}C and ^{16}O atoms in the Si substrate.

Table 1. The sheet resistivity (ohm sq.$^{-1}$) for both the COII getter (CO^+ ion energy $E = 90$ keV and fluence $F = 1.0 \times 10^{16}$ cm^{-2}) side and backside of Cz n- and p-type wafers after FA thermal treatment at 1100 °C for 1 h.

Wafer side[a)]	n-type	n-type	p-type	p-type
	0.5–1.0	5–10	0.3–0.6	10–20
COII layer	1914	3320	3400[b)]	4200
Backside	193	165	170	230

[a)]Whole wafer thickness: 470 μm; [b)]CO^+ ion energy $E = 200$ keV and fluence $F = 2.5 \times 10^{16}$ cm^{-2} after RTA at 800–1000 °C for 30 s.

minimal capacity due to the space−charge region (SCR) formation in the COII getter layer with the CO^+ ion fluence $F = 1.0 \times 10^{16}$ cm^{-2}.

Before measuring the $I-V$ characteristics, the 40 nm silicon dioxide was removed in 1% hydrofluoric acid solution. The potential bias electrode of the laboratory power supply (V_{bias}) was applied to the probe contact on the irradiated wafer side. The ground electrode of the power supply was fed to a metal table in contact with the nonirradiated wafer side after rubbing the InGa paste into it. The potential electrode had a contact with the wafer-irradiated side through the InGa drop at the tungsten needle end (drop area: 3.5 mm^2).

The $I-V$ curve type indicates the p−n junction formation with a rectification coefficient of $\approx 10^3$ at a displacement bias $V_{bias} = \pm 10$ V in the upper silicon layer after COII and annealing. An increase in the ion fluence leads to an increase in the p-layer thickness, as evidenced by lower currents in the forward (up to +5 V) and reverse (up to −10 V) current directions and their superiority at high voltage values due to an increase in the

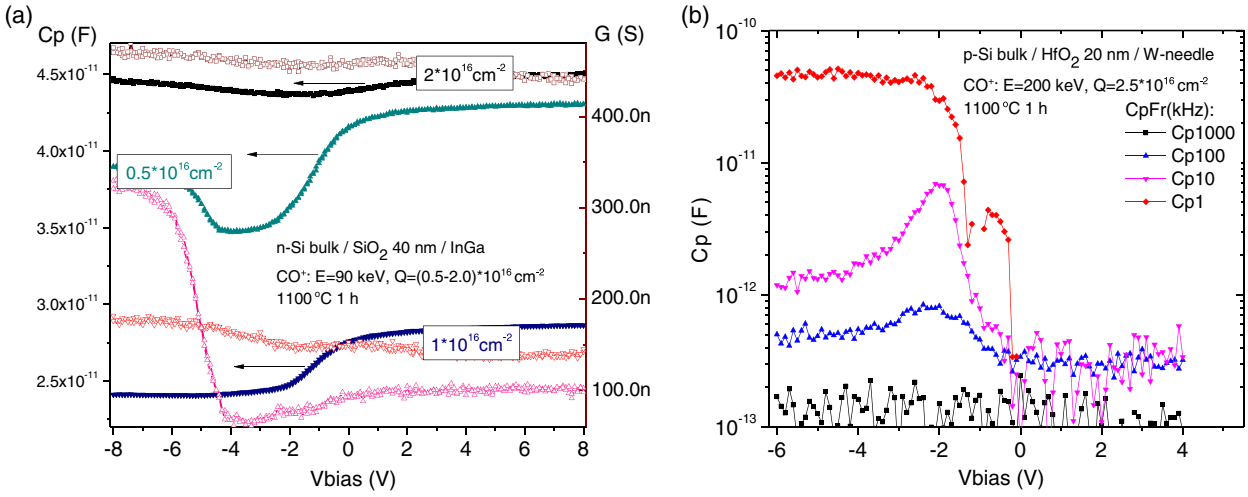

Figure 3. a) *C–V* (filled symbols) and *G−V* (open symbols) curves measured at 10 kHz frequency for three different fluencies, $F = 0.5$, 1.0, and 2.0×10^{16} cm^{-2}, implanted by CO^+ ions at energy $E = 90$ keV into the n-Si substrate through the SiO_2 layer (40 nm) and via annealing at 1100 °C in 1 h. b) *C–V* curves measured at different frequencies, but for the p-type Si substrate with 20 nm HfO_2, implanted by CO^+ ions at the energy $E = 200$ keV and fluence $F = 2.5 \times 10^{16}$ cm^{-2}.

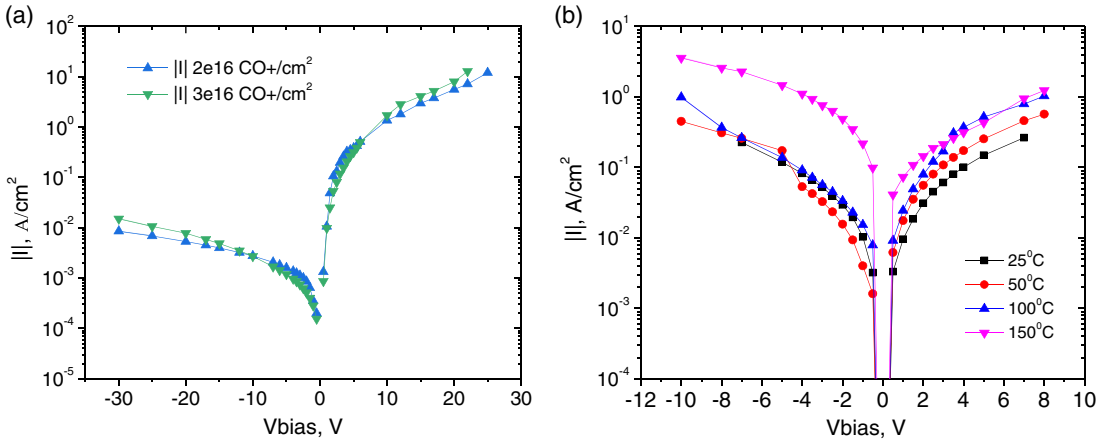

Figure 4. a) *I–V*-measured Schottky barrier diode (SBD) curves in n-type silicon (3–5 Ohm cm) implanted with CO^+ ions at energy $E = 90$ keV and two fluences $\Phi = 2.0$ and 3.0×10^{16} cm^{-2} into the Si substrate after the annealing at 1100 °C for 1 h. b) The same but for the p-type Si (0.3–0.5 Ohm cm) substrate implanted with CO^+ ions with the fluence $\Phi = 1 \times 10^{16}$ cm^{-2} for different measurement temperatures.

concentrations of deep centers in the compensated region (Figure 4a).

Quite similar behavior was observed for the p-type silicon wafers with COII getter layers even for the heavily doped substrate and at elevated temperatures, ≈100–150 °C (Table 1, Figure 4b). It means the formation of n- or i-type layers, where the hole concentration is much lower than in the bulk p-type silicon substrate. These results confirm the data of VdP and $C-V$ measurements relative to the HR SCR formation in the COII getter regions.

3.2. Electric Properties of the SOI Structure with a COII Getter

The SOI electrophysical properties with a COII getter were studied additionally, relative to the Si substrates, by the transient characteristics of pseudo metal–oxide–semiconductor (MOS) field effect transistors (FETs) or pseudo-MOSFETs with tungsten probes, which were 100 μm spaced. They had a 20 μm tip radius, 60 g pressure force, as source−drain contacts, and a back gate, which was a silicon substrate with an ohmic contact.

The observed negative drain currents in pseudo-MOSFETs after RTA are due to the leakage into the substrate through the BOX layer. The channel formation in the electron accumulation is suppressed by the SCR in a reverse-biased p−n (i−n) junction between the BOX and the n-Si substrate (**Figure 5**). Instead of the hole channel drain current, there is leakage into the substrate from the source and drain, because the sums of all currents in a three-terminal measurement circuit are equal to 0 A. Regardless of the BOX layer thickness, the leakage current is greater at negative offsets for all $F > 2 \times 10^{16}\ \mathrm{cm}^{-2}$.

When only the silicon layer was transferred on the substrates with COII-irradiated BOX layer (D-SOI), the leakages through the insulating BOX are observed at a positive bias on the substrate at $V_g > 4$ V in the D-SOI pseudo-MOSFET drain−gate characteristics (Figure 5b).

The hysteresis decreases after the sequential O/E step, reducing the Si layer thickness to 180–220 nm (**Figure 6**). This hysteresis of the characteristics is due to the recharging of defects in the BOX and SCR.

4. Discussion of the Electrical Properties of Si and SOI with a COII Getter

The built-in positive charge and the defects in the SiO_2 or BOX layers damaged by CO^+ ions are not annealed even at 1100 °C after O/E thinning operations. Hot implantation of SOI structures with UT dielectric layers allows one to form the source drains and back gates of double-gate SOI transistors and reduce the defect concentration.[14–16] However, upon the hot implantation with fluences $F > 2 \times 10^{16}\ \mathrm{cm}^{-2}$, a G-band of graphite appears in the Raman-scattering UV spectra of the silicon–oxide hetero borders.[16] The possibility of using hot implantation to form COII getters in bulk silicon or SOI structures requires additional research work.

In an SOI structure with a COII getter in a silicon substrate, the effective electron mobility $\mu_n = 56\ \mathrm{cm}^2/(\mathrm{V\,s})$ is determined by the Y-function of Equation (1).[17]

$$\mu_{n,p} = (\beta_{n,p})^2 (f_n C_{BOX} V_{DS})^{-1} \quad (1)$$

where g_m is the channel conductivity, $\beta_{n,p}$ is the slope of Y-function branches, $f_n = f_p = 0.75$ is the geometry factor, C_{BOX} is buried dielectric capacitance, and V_{DS} – drain−source voltage, which is three times less than the mobility in a similar SOI structure without a getter (Figure S1a, Supporting Information). The structural and electrophysical properties of the silicon and silicon dioxide layers were the same for both types of SOI structures and differed only in the substrate properties, and they are not taken into account when determining mobility. The reason for the discrepancies may be in the different thicknesses of the SCR of the substrate with and without a getter. If there is a wider SCR in the getter substrate, then the contribution of its sequential capacitance will dominate and determine a much lower capacitance in comparison with the BOX dielectric capacitance.

This conclusion is also supported by the C–V data on the relative capacitance near 0 V (Figure S1b, Supporting Information) which, under these conditions, should have been maximum for standard n-type SOI structures, as it is determined by the capacitance of the BOX dielectric with a built-in positive charge and

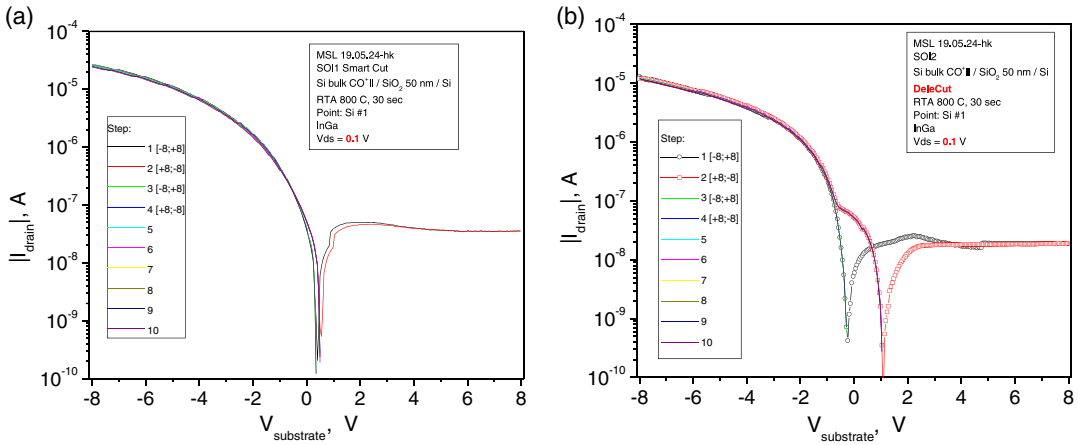

Figure 5. The drain-gate leakage currents through the BOX layer in the n-type pseudo-MOSFET structures (500 nm Si and 40 nm BOX layers) of a) S-SOI and b) D-SOI after RTA at 800 °C for 30 s.

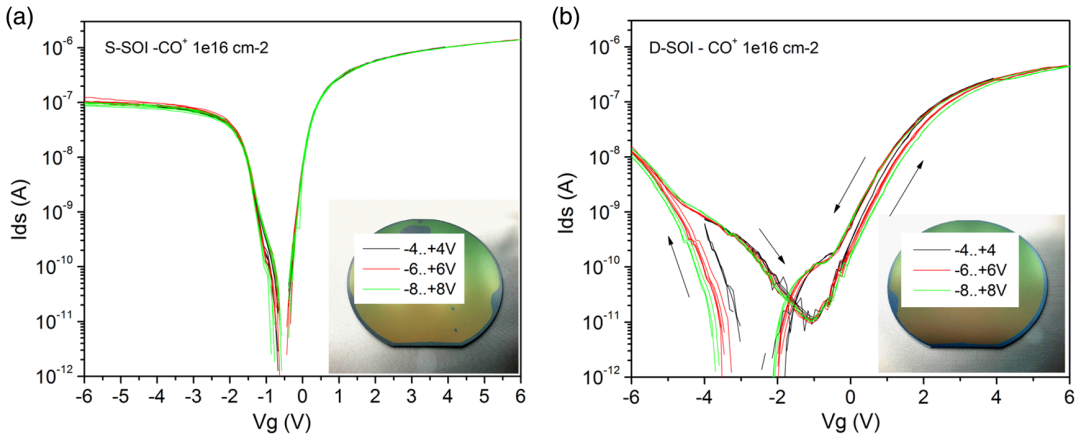

Figure 6. The transient characteristics of a) S-SOI and b) D-SOI n-type pseudo-MOSFET structures (180 nm Si and 40 nm BOX) after the additional (FA O/E 1100 °C for 5 h) annealing. In the insets are the photoimages of a) S-SOI and b) D-SOI with few small holes and blisters in SOI layer.

should not depend on the frequency of $C-V$ measurements. For the maximum frequency of C−V measurements of 1 MHz, C−V dependences correspond to the behavior of classical p-type SOI structures. If one neglects the capacitances of states at the Si/SiO_2 interfaces, one can estimate the maximum SCR depth d_{max} and the hole concentration in the SCR from Equation (2) and (3)[18]

$$C_{sub} = \frac{C_{max}C_{min}}{C_{max} - C_{min}}\left(\frac{1}{A}\right) = \frac{\varepsilon_{Si}}{N_a} \tag{2}$$

$$N_a = 2\Phi_F + \frac{4\varepsilon_{Si}}{qd_{max}^2}\frac{kT}{Aq}\ln\frac{N_a}{n_i} \tag{3}$$

where $C_{max} = 3.18$ pF and $C_{min} = 0.45$ pF are maximum and minimum capacitances, respectively, and C_{sub} is a substrate capacitance. The area A of mesa structure can be found from Equation (3).[18]

$$t_{oxb} = \frac{\varepsilon_{ox}A}{C_{max}} - t_{oxf} - \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}} \tag{4}$$

as $A = C_{max}(t_{oxb} + t_{oxf}\varepsilon_{ox} + t_S/\varepsilon_{Si})\ \ (\varepsilon_0\varepsilon_{ox})^{-1} = 1.1 \times 10^{-8}\ m^2$, taking into account the known parameters of SOI structures, $t_{oxb} = 40$ nm, $t_{oxf} = 2$ nm, and $t_{Si} = 200$ nm. The area $A = 1.1 \times 10^{-4}\ cm^{-2}$ corresponds to the effective diameter of SOI mesa structures $D_{eff} = 116$ μm. Then, from the substrate capacitance $C_{sub} = 48\ \mu F/m^2$ and Equation (1), it follows that the depth of the SCR layer under the buried silicon dioxide is $d_{max} = 2.15$ μm. According to Equation (2), the silicon layer under the BOX is depleted in the main charge carrier electrons to a depth of ≈2 μm and is filled with minority carrier holes with a low concentration of $N_a \approx 3 \times 10^{11}\ cm^{-3}$.

Using a p-type Si substrate can also increase the SCR due to a similar effect (Figure S1, Supporting Information). This means that the i-layer is preserved in the modified COII n-type Si substrate, even after high-temperature treatments. The proposed approach to the SCR formation is similar to the formation of the SCR region with vertically arranged p−n junctions under the BOX layer in the substrate,[19] but, unlike vertical junctions, it does not require matching the arrangement of active and passive RF IC elements in the SOI layer with the boundaries of these SCRs in the substrate. As layers with a COII getter are highly resistive, with respect to the substrate, and have a free charge carrier concentration of $<<1 \times 10^{15}\ cm^{-3}$, nonlinear effects will not be significant for RF ICs.[20]

The possible mechanisms of free carrier removal in a COII getter layer of both n- and p-type moderately doped silicon substrates are related to the carbon atom binding with phosphorous and to the oxygen atom binding with boron at high-temperature annealing, respectively.[21–24]

In addition, the local expansion under the mask along the surface and the SCR depth weakly depend on the substrate conductivity and are determined only by the implantation region and the energy of CO^+ molecular ions, reaching a depth of >1 μm for an ion energy value >500 keV. The large SCR depth is useful for the RF IC and flash applications, but the nature of the high-temperature stability of the SCR is still to be determined. Nevertheless, the local implantation of molecular CO^+ ions allows to isolate the areas suitable for placing RF ICs circuits on SOI wafers without using expensive HR-TR SOI wafers.

5. Conclusion

By the ion implantation of molecular gas ions with m/e = 28 a.u. into silicon substrates, it becomes possible to provide impurity gettering and binding inside the implantation layer. The formation of gettering layers in COII regions of n- and p-type type Cz-Si wafers and in SOI structures is first demonstrated by the SIMS after the processes of direct bonding and thermal cleavage/transfer of Si layers to a silicon substrate and layer-by-layer oxidation/etching at 1000–1100 °C.

The charge carrier mobility in SOI layers, measured by the Y-function method in pseudo-MOS transistors, turns out to be less than the mobility in SOI structures without getters even after high-temperature annealing at 1100 °C, and it is explained by the formation of an SCR under a UT BOX. The presence of this region is confirmed by the $C-V$ and $I-V$ measurements of the vertical mesa structures of SOI UT BOX. When transferring a

silicon layer, together with a thermal silicon dioxide layer (SmartCut) to a Si substrate implanted with CO^+ ions, the interface state value D_i decreases by more than an order of magnitude to $\approx 5 \times 10^{10}\,cm^{-2}$. A model for the formation of a few-micrometer SCR by oxygen- and carbon-containing precipitates is proposed.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Data available on request from the authors.

Keywords

CO^+-implanted Cz−silicon, high-resistivity−trap-reach silicon-on-insulator wafers, thermally robust high-resistance layers

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