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Transport of Charge Carriers along Dislocations in Si and Ge

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Experimental observations and quantum mechanical device simulations point to different electronic properties of dislocations in silicon and germanium. The experimental data suggest a supermetallic behavior of the dislocations in Si and thus the high strain in the dislocation core is thought to cause the confinement of the charge carriers, which leads to the formation of a 1D electron gas along a dislocation (quantum wire). The resulting significant increase in the electron concentration corresponds to a marked increase in the drain current of metal–oxide–semiconductor field-effect transistor (MOSFET). The specific resistance of an individual dislocation in Ge is about nine orders of magnitude higher than for a dislocation in Si. The experimental measurements of the strain in dislocation cores in Ge are still missing. Based on the band structure data, the generation of a strain equivalent to that of the dislocation cores in Si appears to be very challenging because of the transition from an indirect into a direct semiconductor with about tenfold lower strain levels. The lower strain in the dislocation core in germanium may not support the carrier confinement as proposed for the dislocation core of silicon, and consequently 1D electron gases are not expected to form along the dislocations in Ge.

1. Introduction

Dislocations in silicon and germanium were intensively studied over recent decades. Both elemental semiconductors have a diamond cubic crystal structure indicating the existence of the same type of perfect dislocations, that is, pure screw dislocations and pure edge dislocations, the so-called 60° dislocations.[1] The Burgers vector of perfect dislocations is $\boldsymbol{b} = a/2\langle 110\rangle$ with a as the lattice constant. Perfect dislocations frequently dissociate into 30° and 90° partial dislocations (60° dislocation) or two 30° partials (screw dislocation).

Based on the same crystal structure, the analogous models of the electrical properties of dislocations have been previously proposed for both elemental semiconductors.[2–4] Accordingly, it has been assumed that a charged dislocation acts as a strong perturbation for the energy levels of the valence and conduction band caused by the atomic structure of the defect (band-like states) and from the interaction with point defects (localized states).[5,6] However, more recent measurements suggested that the dislocations in silicon and germanium behave like 1D conductors, similar to the nanowires.[3,7,8] Based on this model, the electronic properties of the dislocations in Si and Ge could be explained by their band structure. The current article deals with the experimental measurements of the dislocations in both elemental semiconductors and explains their electronic properties using quantum mechanical calculations.

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2. Results and Discussion

2.1. Short Summary of Experimental Results

The electronic properties of dislocations have been intensively studied with various analytical techniques[4,9–11] that typically required high densities of dislocations for attaining the detection limits of the respective methods. The commonly used method for dislocation generation has been plastic deformation, which also introduces a large number of other defects and defect reactions making it sometimes difficult to interpret experimental data.[3,10]

To avoid such interactions between the defects, alternative methods have been applied to generate defined arrangements of dislocations in silicon and germanium. The measurements on the dislocations in germanium were carried out on p–n junctions prepared in thin Ge layers grown on silicon substrates.[12] If the layer thickness reaches the critical film thickness (above five

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monolayers for Ge on Si), threading dislocations (TD) appear to have densities ranging from 10^6 and 10^9 cm^{-2}. The typical current–voltage (I–V) characteristics of p–n junctions produced in such layers are shown in **Figure 1** at room temperature. In comparison with diodes prepared in dislocation-free bulk germanium (reference sample, Figure 1), Ge p–n junctions with dislocations exhibited a significant increase in the dark current, which suggests that the dislocations act as shunts. Low-temperature measurements showed a $T^{-1/4}$ dependence of the conductivity of the I–V forward region of dislocated Ge diodes (**Figure 2**). An analogous temperature dependence has also been reported for highly dislocated Si diodes such as solar cells.[13] The $T^{-1/4}$ dependence of the conductivity G refers to the 3D variable range hopping mechanism described by Mott's law[14]

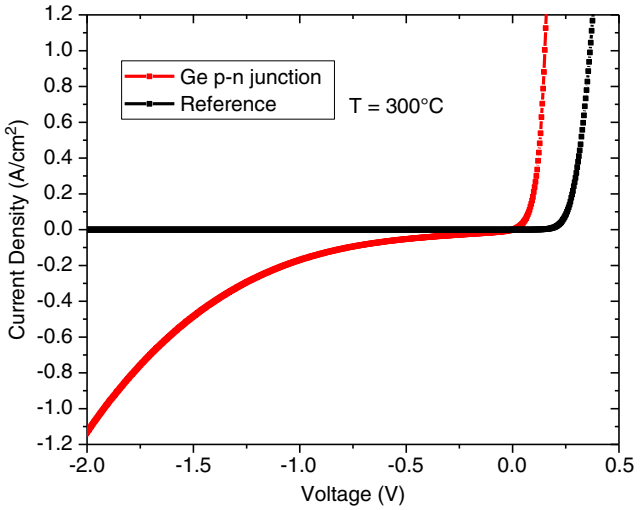

Figure 1. Current–voltage plot of an undoped Ge p–n junction with dislocations in comparison with a dislocation-free Ge photodiode acting as the reference. Measurements at room temperature.

$$G = G_0 \exp[-(T_M/T)^{-p}], \quad (1)$$

where $p = 1/(1+d)$, d is the dimensionality of the system. For a 3D dislocation arrangement, as in the case of the TDs in Ge p–n junctions or solar cells

$$p = 1/(1+3) = 1/4 \quad (2)$$

is valid. T_M in Equation (1) is the Mott characteristic temperature indicating the degree of disorder. It is approximately given by[15]

$$T_M \approx 18\lambda^3/(N(E_F)k_B) \quad (3)$$

with $N(E_F)$ as the electronic density of (localized) states per unit energy interval at the Fermi level, which is expected to be constant in Mott's model, λ^3 is the charge carrier wave function, $\exp(-\lambda r)$ decay length in the localized center, and G_0 is the conductivity prefactor[15,16]

$$G_0 = 3e^2\nu_{ph}N(E_F)/8\pi a k_B T \quad (4)$$

where e is the electronic charge, k_B the Boltzmann constant, and ν_{ph} the hopping frequency that may be related to the phonon frequency.

Reducing the dimensionality of the dislocation arrangement does not result in a similar temperature dependence of the conductivity. There are no indications for a $T^{-1/2}$ or $T^{-1/3}$ dependence of G in our experimental data expected for single dislocations ($d = 1$) and two-dimensional dislocation networks ($d = 2$), respectively. In addition, indications to other variable range hopping processes (Efros-Shklovskii mechanism, characterized by a $T^{1/2}$ dependence[17]) does also not exist suggesting that three-dimensional dislocation networks in Si and Ge consist of one-dimensional conductors (dislocations) with a strong interchange coupling. This conclusion is supported by our previous analyses of diodes without dislocations,[18] for which, band-to-band-tunneling was also observed but the current followed a $T^{-3/2}$ dependence referring to Shockley-Read-Hall (SRH) recombination as the dominant mechanism (**Figure 3**).

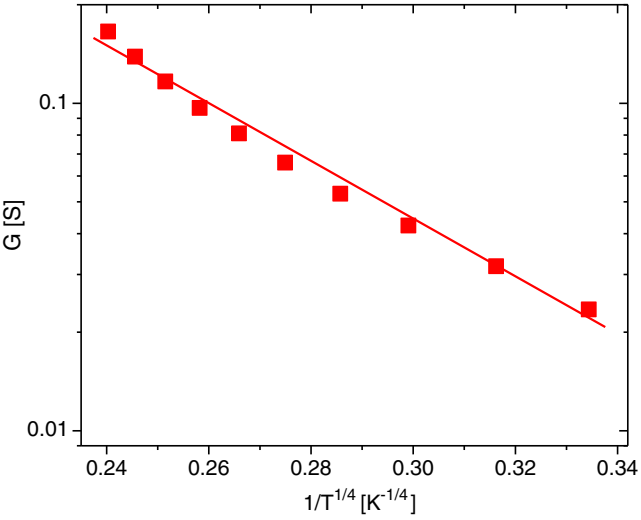

Figure 2. Dependence of the conductance G on the temperature of a dislocated Ge p–n junction ($V = 0.5$ V).

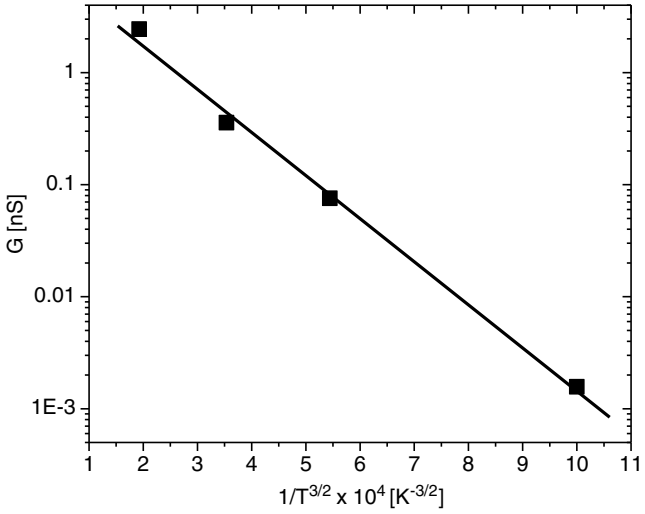

Figure 3. Dependence of the conductance of a Si diode without dislocations on the temperature. The bias is V = 0.2 V.

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Analyses on individual dislocations have been carried out previously for Ge[19] and Si[20,21] suggesting a diode character of these defects. In these studies, dislocations running through the whole wafer were directly contacted by metal tips for measurements. More recent studies showed additional details about the electronic properties of dislocations. For instance, the increase of the dark current of Ge diodes was modelled by shunt effects of threading dislocations.[12] The additional resistance was calculated from the slope of the linear reverse region of the I–V characteristics yielding a specific resistance of an individual TD of $\rho_{TD}^{Ge} \approx 10\,\Omega\,cm$.

The behavior of individual dislocations in silicon has been studied on defined dislocation networks produced by wafer direct bonding in thin device layers of silicon-on-insulator (SOI) substrates.[22] Typical transfer characteristics of n-channel metal–oxide–semiconductor field-effect transistors (nMOSFET's) with and without defined dislocations in the channel are shown in **Figure 4**. The thickness of the device layer was, in this specific case, about 80 nm and the channel length was 1 µm. Importantly, we found significantly higher drain currents (I_{DS}) obtained for devices with dislocations at the same gate (V_G) and drain (V_D) voltages compared with devices without dislocations. An increase in I_{DS} by a factor of 50 was found even at very low gate voltages (Figure 4). Similar results were previously reported by other authors[23] and ascribed to the presence of dislocations.

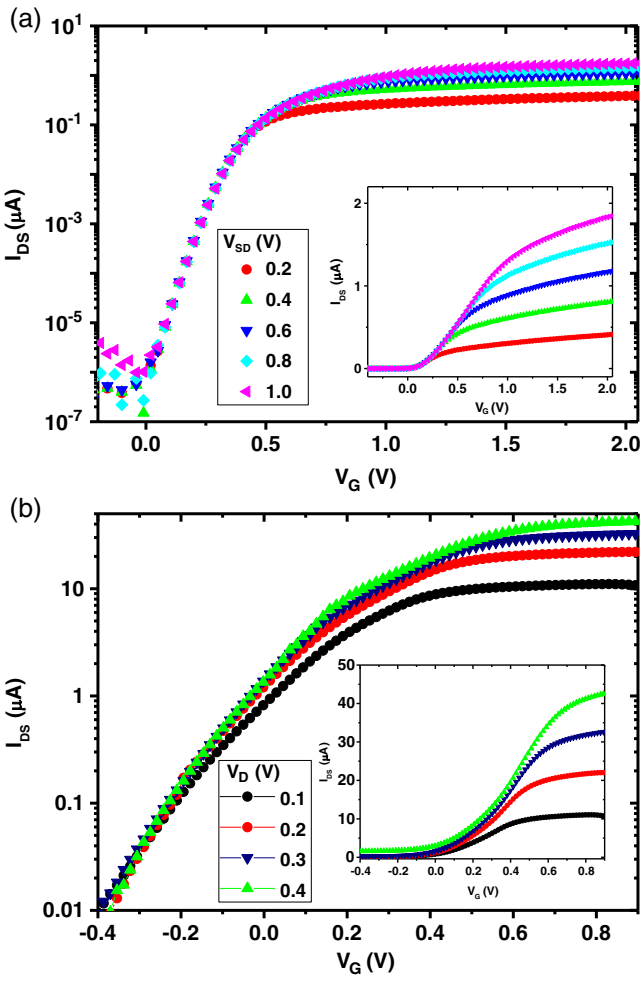

Figure 4. Transfer characteristics (I_D–V_G) of nMOSFETs a) without and b) with dislocations in the channel. The gate length L and width W are 1 µm. The insets in both figures represent the transfer characteristic in linear scale for a better current comparison.

A subthreshold swing of $SS = 100\,mV\,dec^{-1}$ and a threshold voltage $V_T \approx 0\,V$ are extracted for reference samples without dislocations. Devices with dislocations, on the other hand, are characterized by larger values of SS and V_T. Typical values of $SS = 120–370\,mV\,dec^{-1}$ and $-150\,mV < V_T < 400\,mV$ were measured depending on the number of dislocations in the channel. The shift of V_T may be caused by a higher carrier concentration on dislocations influencing the Fermi potential and depletion charge of SOI nMOSFETs.[24,25] We note that both high-resolution electron microscopy [high-angle annular dark field (HAADF)] and analytical electron microscopy [electron energy loss spectroscopy (EELS)] did not show a higher doping concentration on individual defects as a consequence of pipe diffusion or segregation described by other authors.[26–29]

Furthermore, MOSFETs with dislocations are characterized by a lower ratio of on-state to off-state current (I_{ON}/I_{OFF}) compared with reference devices without dislocations. This is mainly caused by higher values of I_{OFF} (Figure 4).

Measurements on nMOSFETs revealed an increase in the drain current (I_{DS}) with decreasing number of dislocations in the channel. The highest value of I_{DS} was expected if only one dislocation crosses the channel from source to drain. The highest increase was obtained if screw dislocations were present in the channel. Furthermore, an increase in I_{DS} was observed for p- and nMOSFET's, which suggests that dislocations transport either electrons or holes. Detailed measurements on only a few dislocations down to an individual defect were performed on n^+pn^+ structures fabricated on SOI wafers containing equivalent dislocation networks. Arrays of such devices were closely spaced to avoid any inconsistency in the dislocation network. The width of the devices (W) was subsequently reduced by electron beam lithography in combination with dry etching down to 30 nm[22] yielding a decreasing number of dislocations with decreasing W. These analyses demonstrated an increase in the current density (or decreasing resistivity ρ_{dis}^{Si}) as W was decreased. Electron microscopy showed only one dislocation at $W = 30$ nm. Assuming the cross section of the dislocation core of 1 nm^2, the current density of a single screw dislocation in silicon would be $J = 3.8{\cdot}10^{12}\,A\,cm^{-2}$ corresponding to a resistivity of $\rho_{dis}^{Si} \approx 1 \times 10^{-8}\,\Omega\,cm$, which is about eight orders of magnitude below that of the surrounding silicon. The resistivity of the dislocation was also significantly smaller than for most metals and suggests a supermetallic behavior of the dislocations in silicon. Moreover, the supermetallic behavior contrasts with the resistivity value extracted for an individual TD in germanium, which is more than nine orders of magnitude higher. The behavior found for the dislocations in Ge explain why Ge-light emitting diodes (LED) with high density of TDs up to $10^9\,cm^{-2}$, crossing the p–n junction, operate properly. These findings may suggest principal differences of the electronic properties of dislocations in silicon and germanium. Assuming a similar atomic structure (or disorder) in dislocations of both elements, the different

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electronic properties may be caused by the different band structures of silicon and germanium.

2.2. Simulation

The supermetallic behavior of the dislocations (screw dislocations) in silicon may be caused by high strain levels inside the dislocation cores.[22] The strain is uniaxial tensile along the dislocation line, that is, along <110>, and reaches about 10% or more ($\varepsilon \approx +0.1$), which is much higher than strain levels induced by the strained layers or other process-induced stressors. Calculations of the band structure result in significant alterations by such high strain levels.[30] A strain of $\varepsilon \approx +0.1$ cause shifts of the conduction and valence bands inducing smaller gaps but in different ways for tensile or compressive strain. Because of the small dimensions of dislocations (diameter of about 1 nm and lengths up to a few micrometers), the band shifts may make the dislocations act as quantum wires. This interpretation was also supported by low-temperature analyses indicating the existence of an electron gas on dislocations in silicon. The existence of Shubnikov–de Haas oscillations refers to a 2D electron gas for dislocation networks consisting of 1D electron gases on individual dislocations.[30]

Quantum mechanical device simulations support the effect of strain-induced bandgap narrowing on the carrier transport along the dislocations in silicon and the resulting interpretation of dislocations as quantum wires.[31] For simulations using the Global TCAD Solutions (GTC) Framework simulation package,[32] a 2D model of a nMOSFET with circular geometry was applied (**Figure 5**). A dislocation (core) in the center was embedded in an unstrained matrix and surrounded by a thin gate oxide and the gate electrode. Using the experimental data for silicon (p-type matrix), core n-type (electron concentration $1 \times 10^{18}\,\mathrm{cm}^{-3}$), uniaxial tensile strain of $\varepsilon = +0.1$ (corresponding to a stress $\sigma = 16$ GPa, measured by electron microscopy)) simulations showed the effect of confinement of carriers (electrons) at the dislocation (**Figure 6**a). The electron concentration increased as the strain in the core increased and reached $n_{el} = 3.5 \times 10^{19}\,\mathrm{cm}^{-3}$ at $\sigma = 16$ GPa and a gate voltage $V_G = 0.6$ V and was therefore 35 times larger than the initial electron concentration assumed to

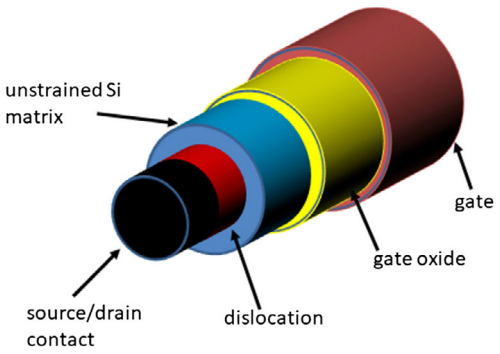

Figure 5. Model of a nMOSFET having a dislocation in the center. The dislocation (red, diameter 5 nm) is embedded in an unstrained silicon matrix (blue, diameter 20 nm) and surrounded by a thin gate oxide (yellow, 1 nm thick) and a gate electrode (brown). The source/drain contact on the dislocation is drawn in black.

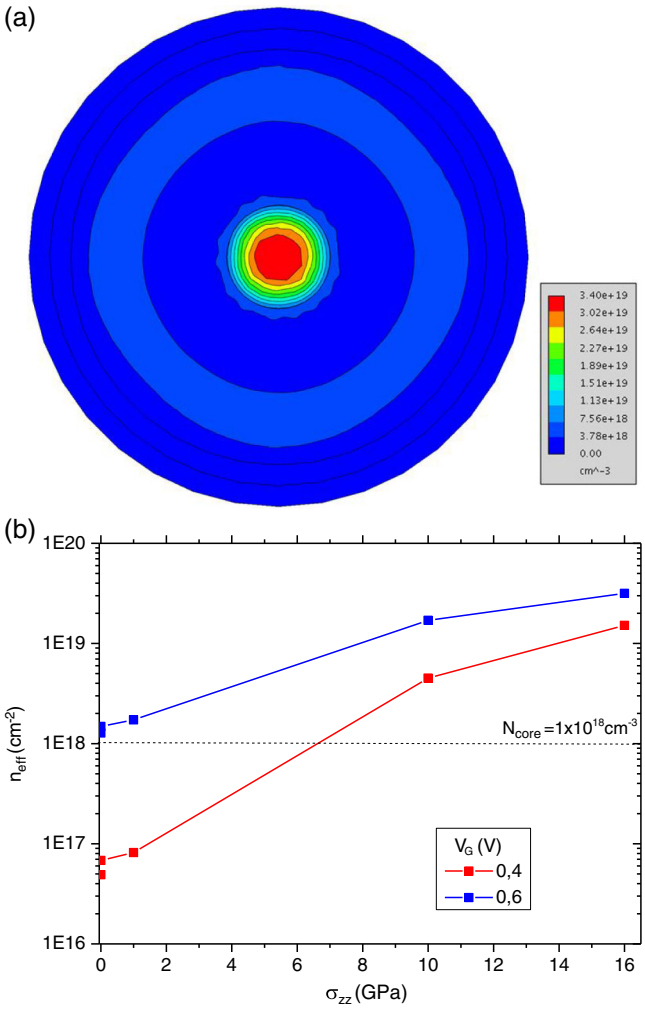

Figure 6. Cross section of a nMOSFET shown in Figure 5 with a dislocation in the center (core). a) The electron concentration at $V_G = 0.7$ V is shown. b) Dependence of the electron concentration on the uniaxial tensile stress (σ_{zz}) in the dislocation for $V_G = 0.4$ V and $V_G = 0.6$ V. The stress σ_{zz} is parallel to the dislocation line.

be $1 \times 10^{18}\,\mathrm{cm}^{-3}$ for the dislocation (Figure 6b). For the reference sample without a dislocation, the maximum electron concentration was about $1 \times 10^{18}\,\mathrm{cm}^{-3}$ and was observed close to the gate electrode. Increasing V_G increased the electron concentration for MOSFETs with and without (reference sample) a dislocation in the center. These simulations showed an increase by more than a factor of 10^4 for MOSFETs with a dislocation in the channel even at low gate voltages ($V_G < 0.5$ V, **Figure 7**c), which may result from the splitting into discrete energy levels in the quantum wire. This effect appears to depend on the diameter of the dislocation core representing the quantum wire. Increasing the diameter up to about 5 nm causes a significant increase in the electron concentration. A further increase in the diameter did not yield an increase in the quantization effects, and the electron concentration remained nearly constant. The strong increase even at low values of V_G suggests shifts of the band structure and therefore changes in the number of energy levels inside the quantum wire.

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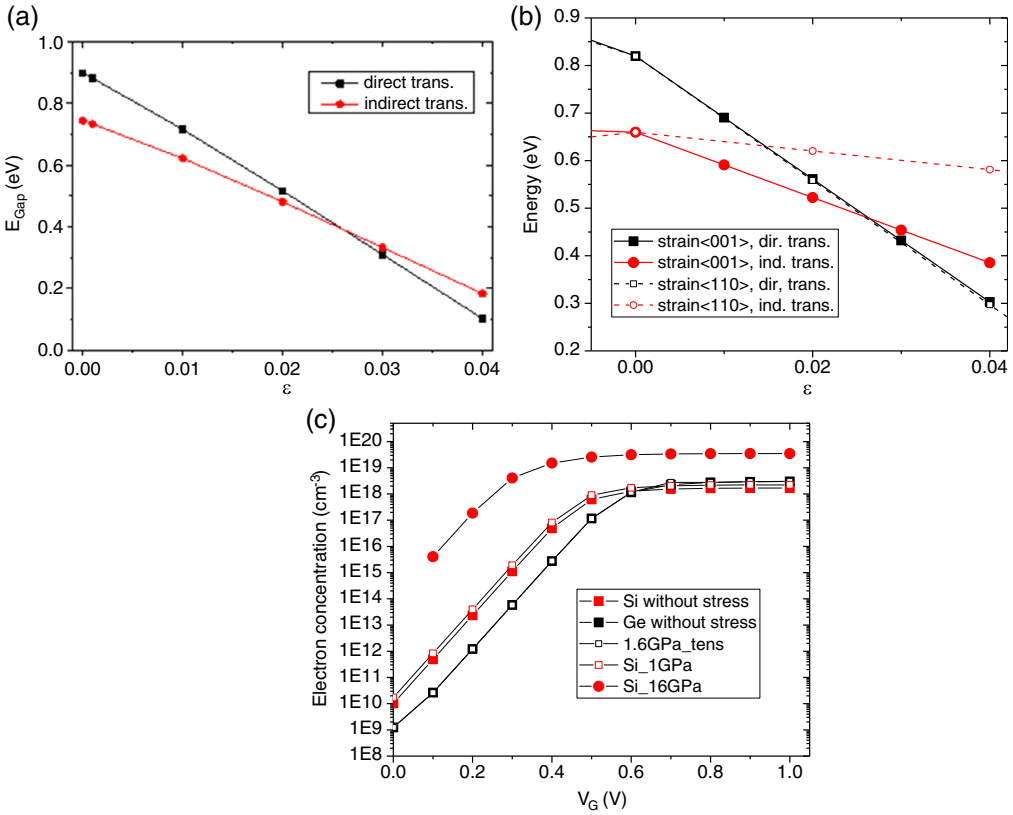

Figure 7. Calculated gap energies for Ge as a function of a) biaxial strain and b) uniaxial tensile strain parallel to <001>- and <110>-directions, respectively. Squares denote the direct transition, while circles characterize the indirect transition in (a) and (b). c) Calculated electron concentration as a function of the gate voltage V_G for Si- (red) and Ge- nMOSFETs (black) without stress (full squares) and with cores (dislocations) having stresses of 1 GPa (red open squares), 16 GPa (full red circles) for Si, and 1.6 GPa for Ge (black open squares), respectively. Note that the curves for the Ge devices without and with stress are superimposed. The uniaxial tensile strain (stress) is assumed to be parallel to <110>. Band structure calculations were carried out using a 6- and 8-band **k.p** model as well as an empiricial $sp^3d^5s^*$ tight binding model described elsewhere.[30]

The different behavior of the band structure of germanium may explain the different properties of dislocations in both elements. Tensile strain up to $\varepsilon = +0.1$ were reported to affect the bandgap at the Γ-point (direct transition) and lower the conduction bands at the Δ- and L-points for Si.[30] The bandgap between Γ- and L-points was smaller than between Γ- and Δ-points at $\varepsilon \geq 0.1$, suggesting the dominance of this new indirect transition at very high strain. Such behavior was not found for germanium. Biaxial as well as uniaxial tensile strain resulted in a downward shift of the conduction band at the Γ- as well as L-points for germanium (Figure 7a,b). Because the slope of both shifts was not equivalent with the increasing strain, both lines intersected. The intersection characterizes the transition of Ge from an indirect into a direct semiconductor. The transition appeared at a biaxial strain $\varepsilon \approx +0.025$. The same strain value was required for transition if a uniaxial tensile strain parallel to <001> was applied (Figure 7b). The uniaxial tensile strain parallel to <110> (characterizing the strain direction in a screw dislocation in elemental semiconductors) shifted the conduction band at the L-point considerably less resulting in the transition to a direct semiconductor already at lower strain rates ($\varepsilon \approx +0.015$).

The calculations showed that significantly lower strain is required for Ge to induce strong alterations of the band structure. The strain was about one order of magnitude lower than for silicon. Therefore, the different band structures had a significant impact on the device behavior. Assuming the same device as in the case of Si (nMOSFET), quantum mechanical simulations suggested lower electron concentrations in the case of MOSFETs prepared in unstressed Ge compared with unstressed Si. The electron concentration was about a factor of 15 lower for Ge-MOSFETs than for Si-MOSFETs even at low gate voltages (Figure 7c). Introducing a dislocation in the channel characterized by a strain of $\varepsilon \approx +0.016$ did not change the electron concentration compared with the unstrained device. This is also plotted in Figure 7c as stress $\sigma = E{\cdot}\varepsilon = 1.6$ GPa where E is the Young's modulus (E ≈ 100 GPa for Ge). We note that such stresses should initiate the transition into a direct semiconductor. Assuming an Si-MOSFET with a dislocation in the channel having nearly the same stress (about 1 GPa) would result in a slightly higher electron concentration as in the case of the unstrained device but would be more than one order of magnitude above the value attained for the Ge-MOSFET. The different electron concentrations obtained for MOSFETs in silicon and germanium may also indicate different recombination mechanisms especially at dislocations. The transition of Ge to a direct semiconductor even at low strain rates may favor radiative

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recombination mechanisms while non-radiative recombination processes may be preferred for Si. The radiative recombination on dislocations in Ge has already been reported in previous studies.[12,33,34]

3. Conclusion

Silicon and germanium possess the same crystal structure indicating analogies in the structure and electronic properties of crystal defects (dislocations). Numerous similarities between dislocations in Si and Ge have been found when a large number of the defects were analyzed, especially of plastically deformed samples,[2,3,35] solar silicon,[13] or TD in Ge layers grown on silicon substrates.[12] Despite this, a different behavior was described in the literature for the effect of dislocations in both elemental semiconductors on device properties. Results of the study by Claeys and Simoen (2009) have been published showing that a minimum number of dislocations was required for the functionality of different Ge devices.[3] For silicon, it has been assumed that only a single dislocation can destroy the functionality of most devices.

Experimental measurements of the individual dislocations in combination with quantum mechanical simulation appear as a useful approach for a better understanding of the electronic properties of dislocations in both semiconductors. The experimentally demonstrated high strain in the core of a (screw) dislocation in Si causes the confinement of carriers and results in the formation of a 1D electron gas along a dislocation. This may cause a significant increase in the electron concentration which, for instance, corresponds to the increase in the drain current of MOSFETs.

The experimental measurements of the strain in dislocation cores in Ge are still missing. Based on the band structure data alone, the generation of a strain equivalent to that of dislocation cores in Si remains very challenging because of the transition from an indirect into a direct semiconductor with about tenfold lower strain levels. An alternative may be the formation of high-pressure phases as described in the literature.[36] The lower strain in the dislocation core in germanium may not support the carrier confinement as proposed for silicon, which suggests that 1D electron gases may not form along dislocations in Ge.

4. Experimental Section

Semiconductor wafer direct bonding under hydrophobic surface conditions was applied to generate 2D dislocation networks.[37,38] Varying the angles of rotational and azimuthal misfit, respectively, resulted in different dislocation distances. The type of the dislocations forming the network was determined by the crystal symmetry of the bonded wafers. Using <100>-oriented silicon wafers, a screw dislocation network with square-like meshes resulted from the rotational misfit.

Silicon-on-insulator (SOI) wafers were applied to avoid the effect of bulk material and the possible defects therein. We utilized commercially available wafers with the following specifications: Czochralski-grown silicon, diameter 150 mm, p-type, resistivity $\rho = 1$–$10\,\Omega\,\mathrm{cm}$, <100>-orientation, buried oxide thickness (BOX) 60 nm. The initial device layer thickness of 260 or 600 nm was reduced to 30 nm by successive thermal oxidation. After removing all oxide layers from the surfaces (including the native oxide), two SOI wafers were bonded (hydrophobic conditions) in an atmospheric environment. Various twist angles between $0.01° < \vartheta_{\mathrm{twist}} < 0.4°$ were realized. After bonding, subsequent annealing at 1050 °C for 4 h in nitrogen resulted in the formation of the t2D dislocation network in the interface. Finally, one of the handle wafers was removed by a combination of mechanical grinding and chemical etching (spin etching) followed by chemical etching of the oxide layer. This procedure resulted in new SOI wafers with 2D dislocation networks in their 60 nm thick device layers.

SOI metal–oxide–semiconductor field-effect transistors (MOSFETs) and arrays of n^+pn^+-diode structures were prepared on such substrates using lithographic techniques and reactive-ion etching (RIE). To avoid the effects of the preparation steps on the properties of dislocations, reference samples without dislocations were prepared in the same process flow. The channel region was defined first, and the channel direction was chosen <110> - crystal directions coinciding with the dislocation direction in Si. To study the effects of the dislocation density, the channel width varied between 1 and 10 µm with a constant channel length ($L = 1$ µm). Source and drain contacts were formed by As^+ implantation (5 keV, $1 \times 10^{15}\,\mathrm{cm}^{-2}$) combined with a rapid thermal annealing (RTA) step (950 °C, 60 s).

Ge-LED structures were prepared by low-temperature molecular beam epitaxy (MBE) on Si substrate, as explained in the previous studies.[39,40] A virtual substrate (VS) technology was applied, using boron-doped (100)-oriented Si substrates with high specific resistance. The RTA oxide was removed by a 900 °C in situ cleaning step. The epitaxial growth started with a Si buffer, followed by an ultrathin VS consisting of a strain-relaxed Ge buffer grown at a very low temperature. An annealing step at 750 °C reduced the original density of threading dislocations from more than 10^{10} to less than $10^9\,\mathrm{cm}^{-2}$. In addition to this VS, the device layers forming the Ge-diode LED structure were deposited at a growth temperature below 400 °C. The 300 nm thick highly doped p-type Ge layer ($B \approx 10^{20}\,\mathrm{cm}^{-3}$) grown on top of the VS served as the buried contact. It is followed by the 300 nm thick Ge active region that was not intentionally doped. In addition, a Ge/Si structure is prepared serving as upper contact. It consists of 100 nm thick highly n-doped Ge and Si layers ($Sb \approx 10^{20}\,\mathrm{cm}^{-3}$), respectively.

The device measurements (output and transfer characteristics of MOSFETs) were carried out using either a 4156C or B1500A Precision Semiconductor Parameter Analyzer (Agilent). For measurements of the Ge diode *I*–*V* characteristics, an E5270B Precision IV Analyzer (Agilent) was applied. The diode temperature was regulated by a Cryostat Microstat N (Oxford Instruments) equipped with a temperature controller ITC 501.

All simulations of the band structure and device simulations were performed using the GTS Framework simulation package.[32] The simulation package enabled classical and quantum mechanical device simulations. For dislocations, the Vienna Schroedinger Poisson Solver (VPS) tool within the simulation package was used representing a general-purpose device simulator for arbitrary nanostructures operating on the Schrödinger–Poisson equation system.[41]

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

dislocation, electronic properties, germanium, silicon

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