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# Electronic characteristics of n-type nanocrystalline/p-type crystalline silicon heterostructure

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**Abstract**

A heterojunction of ultrathin phosphorus-doped hydrogenated nanocrystalline silicon with p-type crystalline silicon was fabricated to investigate carrier information and conduction behaviour. The temperature-dependent carrier information of holes and electrons as well as the two-dimensional electron gas were identified. The forward conduction can be ascribed to tunnelling-aided carrier emission recombination while the reverse transport can be divided into different mechanisms within different reverse bias ranges. The reverse current can be assigned to minority carrier tunnelling through the space charge region within the backward bias voltage from 0 to about −10 V. With decreasing negative applied voltage from −10 V to around −22 V, the reverse current can be attributed to the tunnelling-assisted Poole–Frenkel emission. With further reduction of the reverse bias voltage from −22 V to about −38 V under 100 K, the reverse current staircases can be allocated to sequential resonant tunnelling; otherwise it can be due to the thermic effect at higher temperature. The main origin of short transient time for the fabricated device can be due to the tunnelling mechanism.

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## 1. Introduction

Hydrogenated nanocrystalline silicon (nc-Si:H) films that are constituted by Si nanocrystals embedded in hydrogenated amorphous (a-Si:H) matrices [1] have attracted a large amount of attention owing to its potential nanoelectronic devices and photovoltaic applications. The nc-Si:H based heterojunction as a basic structure can be extensively applied in device fabrication such as solar cells [2], diodes [3] and other electronic devices such as field effect transistors [4]. Hence, identifying carrier characteristics and understanding carrier conduction in this kind of heterostructure is of great importance in developing applications and improving the performances for the deposited films. Hamma *et al* [2] indicated high potential of nc-Si:H as contact layers in p-i-n solar cells and hope to avoid a band discontinuity at the nc-Si:H/a-Si:H interface. A tunnel diode of the (n)nc-Si:H/($p^+$)c-Si structure was fabricated and sequential resonant tunnelling was presented in our previous paper [3]. In [5] the step-like current structures in current–voltage ($I$–$V$) curves due to tunnelling from the subband of the two-dimensional electron gas (2DEG) at the interface nc-Si:H/c-Si to the 0 dimension electronic states in Si nanocrystals were observed because no buffer layer existed between a thick nc-Si:H film and a c-Si substrate. These related progresses implied that the carrier characteristics and transport are determined by the nc-Si:H based heterojunctions.

In order to further develop device technology, in the present work, an ultrathin phosphorus-doped nc-Si:H film was deposited on a medium-doped (p)c-Si substrate to form a (n)nc-Si:H/(p)C-Si structure, while the carrier information and conduction were analysed. Compared to the previous

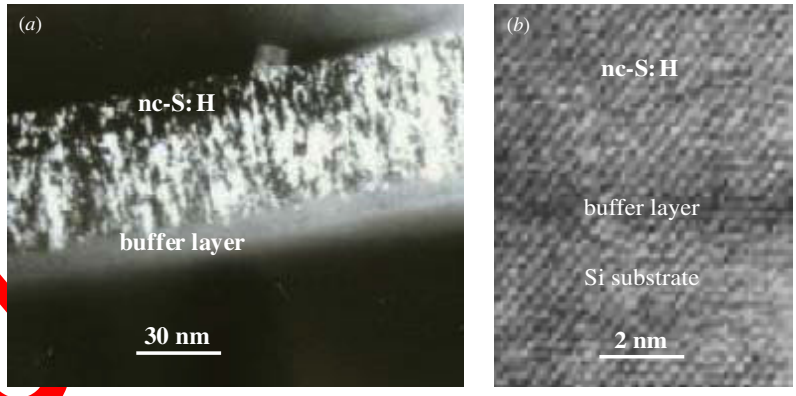


**Figure 1.** (*a*) A TEM image of the cross section (n)nc-Si:H/(p)c-Si, which shows columnar nanocrystalline growth along the direction of film growth on a buffer layer. (*b*) A HRTEM picture of the (n)nc-Si:H/(p)c-Si, which reflects Si nanocrystals embedded in very narrow grain boundaries (about 2–4 atomic spacings, much less than the mean size of Si nanocrystals).

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device [3], in the present structure, one can expect that the negative differential conductance will have vanished since medium-doped (p)c-Si was employed as a substrate. In the heterojunction nc-Si:H/c-Si [5], the buffer layer between nc-Si:H and c-Si did not exist. It can be comprehended as that the deposition of the thick nc-Si:H film (0.92 $\mu$m) needed a long time, each of Si atoms which derived from decomposition of reactive source gas silane $SiH_4$ had enough time to adjust their position and match with the atom array of the c-Si substrate in the deposition process. Hence, no buffer layer can be formed in that diode. However, in the present device, the deposition of the ultrathin nc-Si:H layer on c-Si needed a very short time, the incubated high resistivity amorphous buffer layer should be formed and it was actually demonstrated by a high resolution transmission electronic microscope (HRTEM) image. Therefore, one can imagine that the buffer layer between ultrathin nc-Si:H and c-Si will play a key role, which acts as a spike-shaped barrier in the bend conduction band of the (n)nc-Si:H/(p)c-Si junction to bring about the possible existence of 2DEG at the junction interface. In this paper, the device was created and its electrical properties were analysed. The carrier characteristics including the 2DEG at the interface of (n)nc-Si:H/(p)c-Si were indicated, while the transport behaviour and the main origin of the short transient time of the produced structure were elucidated.

## 2. Experimental details

A single-facet polished p-type (100) silicon wafer around 100 $\mu$m in thickness with an average resistivity of 1.2 Ω cm ($N_A \sim 10^{16}$ cm$^{-3}$) was adopted as the substrate. The (n)nc-Si:H/(p)c-Si structure was prepared by a planar process. First, an approximately 100 nm thick $SiO_2$ layer was made by thermal oxidation of the substrate wafer at 1293 K. Subsequently, the $SiO_2$ layer was etched and patterned by photolithography to make an array of square holes (50 × 50 $\mu$m$^2$). A strong hydrogen-diluted silane, i.e., $SiH_4$ diluted into 1.0 vol% (volume percentage) in $H_2$ and phosphine $PH_3$ was added into diluted silane with a doping ratio of $PH_3/SiH_4 = 0.50$ vol% to get the mixed reactant source gas. The fresh phosphorus-doped nc-Si:H film was deposited by a capacitively coupled radio-frequency (RF of 13.56 MHz)

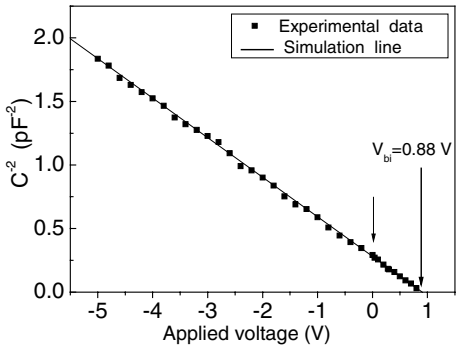


**Figure 2.** Relation between the reciprocal of capacitance squared and applied voltage ($C^{-2}$–$V$) for the electrode/(n)nc-Si:H/(p)c-Si/electrode at room temperature.

plasma-enhanced chemical vapour deposition system on the array configuration. The outer layer of the deposited film in the square holes was removed by etching and photolithography, leaving only about 50 nm thick phosphorus-doped nc-Si:H layers in the hole bottoms. The other process parameters were set as follows: the substrate temperature was 523 ± 1 K, the RF power density 0.60 ± 0.05 W cm$^{-2}$, reactant gas pressure 100 ± 5 Pa and a negative direct current voltage −200 ± 2 V applied to the substrate. Later, Au/Cr and Au/Ge alloy as the Ohm contact electrode was prepared by electron-beam evaporation on the side of the substrate and nc-Si:H film, respectively. For convenience of electric measurements, finally, the structure of electrode/(n)nc-Si:H/(p)c-Si/electrode was sealed in a ceramic shell with a metal contact pad.

The cross section of (n)nc-Si:H/(p)c-Si was checked by a TEM apparatus JEM-2010 operating with a voltage of 200 kV and resolution of 0.19 nm, as shown in figure 1(*a*). A HRTEM picture for the cross section was taken and displayed in figure 1(*b*), from which one can find that a buffer layer of some 2 nm thickness was incubated upon the substrate.

The capacitance–voltage ($C-V$) curve for electrode/(n)nc-Si:H/(p)c-Si/electrode was performed with a HP4280A precision LCR meter with an alternation signal of 1 MHz frequency and an amplitude voltage of 0.05 V at room temperature and the measurement data were transformed into the relation of $C^{-2}$ versus $V$ as exhibited in figure 2.

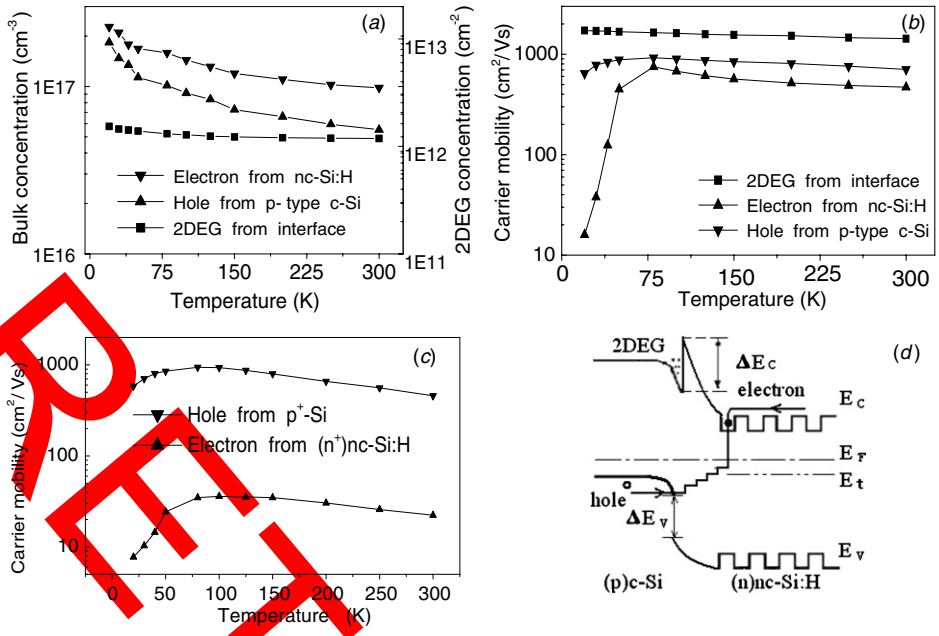


**Figure 3.** (*a*) Temperature dependence of concentrations of $h_{c\text{-Si}}$, $e_{nc\text{-Si:H}}$ and $e_{2DEG}$. (*b*) Temperature dependence of mobilities of $h_{c\text{-Si}}$, $e_{nc\text{-Si:H}}$ and $e_{2DEG}$. (*c*) Temperature dependence of mobilities of $h_{c\text{-Si}}$ and $e_{nc\text{-Si:H}}$ in (n$^+$)nc-Si:H/(p$^+$)c-Si prepared in [7]. The dots are experimental data and the connecting lines are guides to the eye. (*d*) The energy band diagram of (n)nc-Si:H/(p)c-Si.

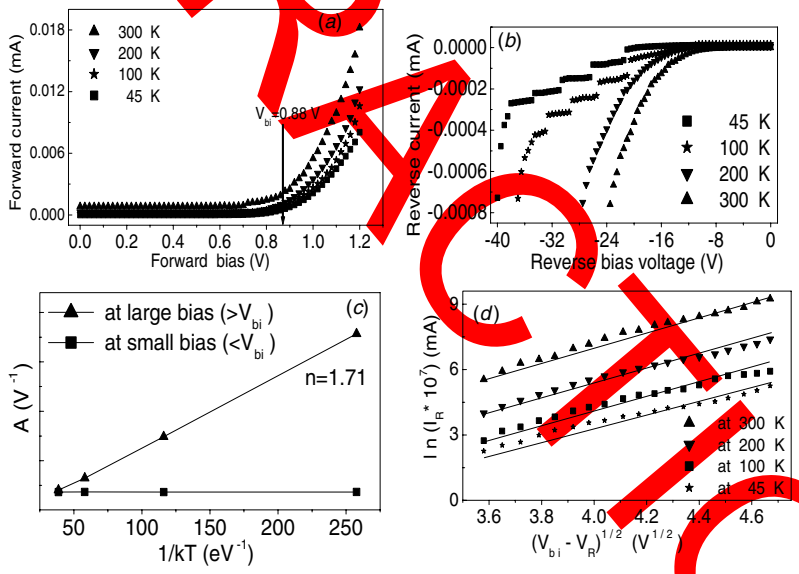


**Figure 4.** Current–voltage (*I*–*V*) experimental plots of the electrode/(n)nc-Si:H/(p)c-Si/electrode at different temperatures: (*a*) for forward *I*–*V* data and (*b*) for reverse *I*–*V* data, respectively. (c) Temperature dependence of *A* in expression (3) derived from the forward *I*–*V* experiment in (*a*). (*d*) The relation ln($I_R$) versus $(V_{bi} - V_R)^{1/2}$ derived from (*b*) within the reverse bias range from −10 V to around −22 V at different temperatures. In (*a*) and (*b*) the dots are experimental data while in (*c*) and (*d*) the dots are the calculated data, the connecting lines are guides to the eye.

In order to detect whether 2DEG occurs in the present device, a temperature- and magnetic field-dependent Hall-effect measurement in combination with mobility spectrum analysis can be adopted to check the carrier information including kinds, concentration and mobility [6]. Using van der Pauw configuration, the carrier parameters in (n)nc-Si:H/(p)c-Si were measured by an Oxford Instruments superconductive magnet system (temperature from 20 to 300 K and magnetic field intensity from 0 to 15 T), as presented in figures 3(*a*) and (*b*). As a comparison, in figure 3(*c*) the measurement of carrier characteristics in (n$^+$)nc-Si:H/(p$^+$)c-Si created in our recent paper [7] was taken.

The *I*–*V* data of electrode/(n)nc-Si:H/(p)c-Si/electrode were conducted by a computer-controlled system including HP4140B (PA meter/dc voltage source) within the temperature range from 20 K to room temperature, as depicted in figures 4(*a*) and (*b*).

Testing of a deep-level transient Fourier spectrum (DLTFS) with temperature sweeping from 77 to 450 K was performed by a high sensitivity DLTFS meter BIO-RAD-

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**Table 1.**The results of the deep-level transient Fourier spectrum (DLTFS).

| $V_R$ (V) | $(N_A - N_D)$ ($10^{17}$cm$^{-3}$) | Trap level location $E_t$ (eV) | Capture cross section $\Sigma$ ($10^{-15}$ cm$^{-2}$) | Trap concentration $N_t$ ($10^{12}$ cm$^{-3}$) | $[N_t/(N_A–N_D)]$ (%) |
|---|---|---|---|---|---|
| −1.0 | 2.36 | $E_1 = -0.51$ | 3.2 | 0.432 | $\sim 10^{-5}$ |
| −2.0 | | $E_1 = -0.51$ | 3.2 | 1.45 | |
| −3.0 | | $E_1 = -0.51$ | 3.2 | 3.52 | |

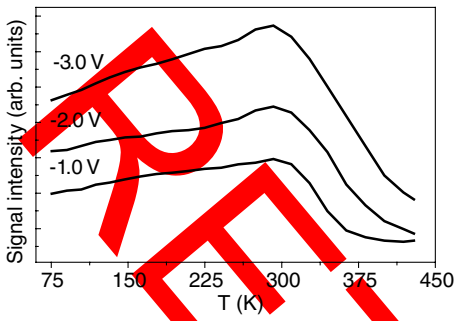


**Figure 5.** Deep-level transient Fourier spectra (DLTFS) of electrode/(n)nc-Si:H/(p)c-Si/electrode.

DL8000 at different reverse applied voltage $V_R$ and pulse amplitude voltage $V_P$ but held at $V_R + V_P = 0$ V. The spectra are shown in figure 5 and the results from DLTFS measurement are presented in table 1.

According to the measurement of transient time for the p–n junction [8], the transient time of electrode/(n)nc-Si:H/(p)c-Si/electrode was taken by a digital sampling oscillograph TDS8000B with forward current $I_F = 0.1$ mA and reverse current $I_R = 0.1$ mA under room temperature. The observation showed that the transient time of the studied device was only about 1.8 ns.

## 3. Results and discussion

### *3.1. Carrier characteristics of the (n)nc-Si:H/(p)c-Si structure*

From the *C–V* experiment in figure 2, one can find that the relation of $C^{-2}$ versus $V$ is almost linear, which indicates that electrode/(n)nc-Si:H/(p)c-Si/electrode is a single abrupt semiconductor p–n junction since no peak appears at zero applied voltage [9, 10]. In addition, the almost linear $C^{-2}$–$V$ characteristic further reveals reasonably that there is a discontinuity in the bend conduction band of the (n)nc-Si:H/(p)c-Si structure, as described in figure 3(*d*), from which one can presume the existence of 2DEG at the interface of the junction [11, 12]. Actually, three kinds of carriers including hole and electron as well as 2DEG, which are labelled as $h_{c\text{-}Si}$ and $e_{nc\text{-}Si:H}$ as well as $e_{2DEG}$ respectively within the (n)nc-Si:H/(p)c-Si system, are demonstrated in figures 3(*a*) and (*b*) according to the temperature- and magnetic field-dependent Hall-effect experiment in combination with mobility spectrum analysis, for which clear evidence for the 2DEG formation in the interface (n)nc-Si:H/(p)c-Si is exhibited. Herein, one can deduce that it is just the high resistivity amorphous buffer layer that plays a key role as a spike-shaped barrier in the bend conduction band of (n)nc-Si:H/(p)c-Si and induces the 2DEG formation. Otherwise, one can infer that the 2DEG would have disappeared since there is no discontinuity in the bend conduction band of the (n$^+$)nc-Si:H/(p$^+$)c-Si heterostructure with very high carrier concentrations on both sides [7], as demonstrated in figure 3(*c*). In figure 3(*b*), the holes indicating two kinds of classical scattering mechanisms of bulk carriers (i.e., ionized impurity scattering at low temperature and phonon scattering at high temperature) can be attributed to the 3D carriers from (p)c-Si [13]. With regard to the high mobility electrons, reflecting weak decrease with rising temperature due to limitation by longitudinal optical phonon scattering [14], can be assigned to 2DEG which emerges within the interface of (n)nc-Si:H/(p)c-Si. However, for the low mobility electrons, the temperature-dependent mobility indicates the variation in conductance from the band-tail state conductance (exponential temperature dependence under 50 K) to the extended state conductance (power-law temperature dependence at $T > 50$ K). Similar behaviour was observed in a-Si:H [15], which can be ascribed to the conduction of majority carriers. It should be noted that the observed high electron mobility up to about 500 cm$^2$ (V s)$^{-1}$ at room temperature implies the highly uniform distribution of Si nanocrystals, as depicted by HRTEM image in figure 1(*b*). The figure reveals that Si nanocrystals imbed in very narrow grain boundaries (about 2–4 atomic spacings in thickness, much less than the mean size of Si nanocrystals), which indicates that the crystalline volume fraction of the prepared film prevails over 50% in volume percentage. Accordingly, electron tunnelling occurs easily between nanocrystals. Hence, the diffusive mobility of electrons in nc-Si:H can be regarded as the same as that in c-Si. Furthermore, the boundary scattering in the ballistic transport of carriers through the barriers of the interfaces between nanocrystals is intensively related to doping concentration, electron mean free path and trapping states at the boundaries. It is demonstrated by the result in figure 3(*c*), from which the low electron mobility in the (n$^+$)nc-Si:H/(p$^+$)c-Si system produced in [7] can be assigned to heavy doping. It is just the uniform distribution of ordered Si nanocrystals that results in the latter step-like structures in *I–V* curves at low temperature. The observed high carrier mobility implies that the prepared heterojunction will be suitable for heterojunction field effect transistors [14].

According to the electron and hole concentrations in figure 3(*a*), one can presume the distribution of the depletion layer using the following expression [16]

$$\frac{V_{D1}}{V_{D2}} = \frac{\varepsilon_2 N_D}{\varepsilon_1 N_A}, \tag{1}$$

where $\varepsilon_1 = 11.9$ is the dielectric constant of c-Si, $\varepsilon_2 \approx 10.0$ is the dielectric constant of nc-Si:H according to the present mean size of Si nanocrystals [17]. $N_A$ and $N_D$ are

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the acceptor concentration on the (p)c-Si substrate side and the donor concentration in the (n)nc-Si:H layer, respectively. $V_{D1}$ and $V_{D2}$ are the diffusion voltages supported by c-Si and nc-Si:H, respectively. For the built-in potential $V_{bi} = V_{D1} + V_{D2}$, one can obtain the $V_{bi} = 0.88$ V from the relation of $C^{-2}$–$V$ in figure 2 or from the measured forward $I$–$V$ curve in figure 4(*a*) at room temperature. As a result, one can obtain $V_{D1} = 0.47$ V while $V_{D2} = 0.41$ V according to expression (1) and the values of $N_D$ and $N_A$ in figure 3(*a*). Hence, the depletion layer in the studied p–n junction should be located on both sides of c-Si and nc-Si:H. Both nc-Si:H and c-Si should be taken into account when the carrier transport of the heterostructure is considered. Particularly, the part of nc-Si:H, located in the space charge region, will play a crucial role. On the one hand, the defect traps originating from dangling bonds and disorder as well as impurities can provide gap states for carrier tunnelling through the heterojunction. On the other hand, the localized defect traps may supply recombination centres to induce carrier recombining.

### 3.2. *I–V characteristics of the (n)nc-Si:H/(p)c-Si junction*

The dark $I$–$V$ measurement curves of (n)nc-Si:H/(p)c-Si in figures 4(*a*) and (*b*) were measured at different temperatures. The experimental data indicate a typical $I$–$V$ characteristic for a semiconductor diode while exhibits good rectifying behaviour with a rectification ratio $I_F/I_R$ up to the order of magnitude $10^4$ at $\pm 1.0$ V at room temperature. One can also imply from figure 4(*a*) that the built-in potential $V_{bi}$ of about 0.88 V coincides with the speculated value from $C^{-2}$–$V$ data in figure 2. It is obvious from the forward $I$–$V$ curves in figure 4(*a*) that the slopes of the curves present weak temperature-dependent behaviour within the measurement temperature range. Really, the experimental $I$–$V$ curves can be described by the multitunnelling-assisted carrier capture-emission mechanism using the empirical expression [18]

$$I = I_0[\exp(AV) - 1] \tag{2a}$$

$$\begin{aligned} I_0 &= SB\exp(-E_{ac}/k_BT) \\ &= SB\{\sigma_p v_{th} N_V \exp[-(E_T - E_V)/k_BT] \\ &\quad + \sigma_n v_{th} N_C \exp[-(E_C - E_F)/k_BT]\}, \end{aligned} \tag{2b}$$

where $I_0$ is the saturation current, $S$ is the junction area, $B$ is the constant irrespective of applied voltage and temperature, $\sigma_p$ and $\sigma_n$ are the capture cross section of holes and electrons, $v_{th}$ is the thermal velocity, $N_C$ and $N_V$ are the effective densities of states in conduction band and valence band of nc-Si:H, $E_{ac}$ the activation energy, $E_C$, $E_V$, $E_F$ and $E_T$ are the energies of the conduction band, valence band, Fermi level and deep trapping level that originates mainly from midgap dangling bond states of nc-Si:H, respectively, $A$ is the coefficient, $k_B$ is Boltzmann's constant in units of eV K$^{-1}$ and $T$ is the measurement temperature in Kelvin. The first term in expression (2*b*) relates to electron capture while the second term correlates with hole emission. According to the relation of $\ln(I_0)$ versus $1/kT$ from formula (2*b*) and experimental data, one can indicate that the activation energy $E_{ac} \approx 0.80$ eV, which is larger than the diffusion potential $eV_{D2} \sim 0.41$ eV (where $V_{D2} = 0.41$ V is the diffusion voltage which is borne by the nc-Si:H layer as aforementioned). Therefore, the condition for tunnelling flux through the spike-shaped barrier cannot be satisfied [18]. Moreover, as exhibited in figure 1(*b*), the amorphous buffer layer is sandwiched by nc-Si:H and c-Si, which acts as a spike-shaped barrier and will prevent tunnelling from the subband of 2DEG in the nc-Si:H/n-Si interface to the 0D electronic states in Si nanocrystals in [5]. However, the film deposited by CVD usually has a high defect density. When the trap density is up to a certain degree, the mean distance between them is very small. As a consequence, the charged neighbouring traps interfere with each other, and the potential well for trap centres can be significantly decreased under the applied bias. Hence, the formed gap states in the forbidden band gap can provide tunnelling paths, while the localized traps can supply recombination centres. Accordingly, the forward conduction phenomenon can be regarded by electrons from the conduction band, which are trapped in localized states associated with the depletion region and are recombined with holes emitted from the valence band via multistep tunnelling sites existing within the band gap, as exhibited in figure 3(*d*).

As is well known, the coefficient $A$ in the expression (2*a*) depends on the dominant carrier transport mechanism. $A$ is temperature independent if the forward current is governed by tunnelling. When the forward current is dominated by other mechanisms, $A$ is generally temperature dependent and is expressed by [19]

$$A = \frac{q}{nk_BT}, \tag{3}$$

where $q$ is the elementary charge. If $I_F$ derives primarily from carrier diffusion or thermionic emission in the depletion region, the ideality factor $n$ is equal or close to 1. If $I_F$ comes chiefly from carrier recombination, then $n$ should be close to 2. Accordingly, a least-square fitting with the experimental data in figure 4(*a*) was performed using $I_0$ and $A$ as adjustable parameters. As a consequence, at small forward biases (lower than $V_{bi}$), the parameter $A$ is independent of $1/k_BT$ as exhibited in figure 4(*c*), which indicates that tunnelling plays a primary role in the forward current when the applied voltage is lower than $V_{bi}$ [18–20]. While at large forward biases (higher than $V_{bi}$), the coefficient $A$ agrees with expression (3) with $n = 1.71$ close to 2 as exhibited in figure 4(*c*), which indicates that the $I_F$ originates from carrier recombination, namely, a great number of defect traps in nc-Si:H induces the carrier recombination.

For the reverse current $I_R$, it shows weak electrical field and temperature dependence within the reverse bias from 0 to about $-10$ V for different measurement temperatures, as displayed in figure 4(*b*). The conduction behaviour within this negative applied voltage range should be attributed to tunnelling instead of electrical-field-enhanced electron emission. One can comprehend it according to the DLTFS results. As demonstrated in table 1 and figure 5, the trap concentration $N_t$ increases with reducing reverse bias voltage $V_R$, which indicates that $N_t$ increases with the depth inside nc-Si:H from the interface of (n)nc-Si:H/(p)c-Si. The depletion layer broadens and leads the observed trap concentration to increase with the decreasing reverse bias. The traps act as discrete bulk traps rather than continuous interface ones, because the measured signal peaks are fixed at the same temperature and independent of the reverse bias $V_R$ as depicted in figure 5. This can be explained

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by the bulk traps in the nc-Si:H film being far larger than the interfacial traps, since abundant defects (including dangling bonds, impurities, disorder, etc) are imbedded in the film. Therefore, few localized states coming from the discrete bulk traps participate in the transport. Consequently, little cumulative leakage current increases with a decrease in the backward reverse bias. As a result, one can deduce that the carrier transport within this negative applied voltage range is dominated by tunnelling behaviour, namely, the minority carriers tunnel across the depletion layer in (n)nc-Si:H/(p)c-Si rather than majority carriers.

With the reverse applied voltage decreasing from −10 V to around −22 V, the relations $I_R$ versus $(V_{bi}–V_R)^{1/2}$ are almost linear while the slopes have little difference for different experimental temperatures in figure 4(*d*), namely, $I_R$ is approximately linearly dependent on the applied electrical field. Similar characteristics had been found in the junction of nanocrystalline carbon with crystal silicon and the diode of polymorphous silicon with crystal silicon [21, 22], where $I_R$ can be reasonably assigned to the tunnelling-assisted Poole–Frenkel emission. It can be easily inferred that $I_R$ should be remarkably influenced by the carrier injection as well as the trap properties in the present junction. On the one hand, the limited injection of carriers through tunnelling into the trap states is a fundamentally different transport behaviour from the conventional Poole–Frenkel mechanism. On the other hand, with the help of the reverse applied electrical field, the tunnelling process was greatly enhanced by the Poole–Frenkel effect and the large increase in $I_R$ was obtained by increasing the applied voltage.

However, by further reducing the negative applied voltage from −22 to about −38 V, the plots of $I_R$ versus $V_R$ demonstrate current staircases under 100 K, as present in figure 4(*b*). A similar phenomenon was interpreted as an injection of electrons via sequential resonant tunnelling through the Si nanocrystal quantum dots into the substrate in [3]. In addition, in figure 4(*b*) the width of the current staircase reduces till it disappears with rising temperature, which indicates that the energy gap between quantized energy bands formed in Si nanocrystals decreases till it vanishes with rising temperature. In figure 4(*b*), with further decrease in the reverse applied voltage beyond −38 V, the sharp increase in $I_R$ can be assigned to the carrier avalanche multiplication to enhance the electron resonant tunnelling in the nc-Si:H layer at low temperatures. Comparing the breakdown voltage of the present junction with that of the (n)nc-Si:H/($p^+$)c-Si structure in [3] at low temperatures, the slight difference between them indicates that a majority of applied voltage is supported by the incubated buffer layer between the ultrathin nc-Si:H film and c-Si substrate. However, at high temperatures, e.g., at 200 K and 300 K, the value of $I_R$ increases fast and shows no staircase, which can be allocated to thermic effect [8, 23]. It can be understood as follows. In the present device, the active nc-Si:H layer was surrounded by the $SiO_2$ material while the junction was sealed in a ceramic shell. Hence, the heat that originates from reverse operating current can hardly be dissipated with the result of increasing temperature, which induces the increase of $I_R$. This leads to breaking down the junction.

### *3.3. Transient time of the (n)nc-Si:H/(p)c-Si device heterojunction*

At room temperature, the transient time of (n)nc-Si:H/(p)c-Si can be theoretically expressed by [8, 24]

$$t \approx \frac{\tau}{2}\left(\frac{I_R}{I_F}\right)^{-1} = \frac{1}{\sigma v_{th} N_t}\left(\frac{I_R}{I_F}\right)^{-1}, \tag{4}$$

where $\tau$ is the lifetime of minority carriers in the (n)nc-Si:H layer, $\sigma$ is the conductance, $v_{th}$ is the thermal velocity, $N_t$ is the trap concentration, $I_F$ and $I_R$ are the employed forward and reverse currents, respectively. In the experiment, $I_R/I_F$ was set as 1. As depicted in table 1, a deep trap level was formed in the present p–n junction and the trap concentration $N_t$ is near $10^{12}$ $cm^{-3}$. In addition, at room temperature the carrier concentration in (n)nc-Si:H is up to $10^{17}$ $cm^{-3}$ as shown in figure 3(*a*). Hence, the lifetime of minority carriers $\tau$ can be up to $2 \times 10^{-10}$ s according to [8]. Therefore, the transient time $t$ is around $10^{-10}$ s from expression (4) and close to the measured value of around 1.8 ns. The deviation may come from the neglect of the time for carrier transition from electrode to trap states. One can presume that it is just the high densities of trap states which make tunnelling the crucial role to result in carriers traversing rapidly through the junction [25]. However, the transient time cannot be described by the time for a carrier to traverse through the film or the substrate [26]:

$$t = \frac{d^2}{\mu_{eff} V}, \tag{5}$$

where $V$ is the applied voltage to the measurement structure, $d$ is the thickness of the nc-Si:H film or of the substrate and $\mu_{eff}$ is the effective mobility in the film or in the substrate. Herein, the value of $V$ was taken as 0.88 V in the experiment, $\mu_{eff}$ is achieved at around 500 $cm^2$ $(V\ s)^{-1}$ at room temperature from figure 3(*b*). The obtained value $\tau$ is only of the order of magnitude $10^{-15}$ s for the film or $10^{-6}$ s for the substrate according to description (5) and hence does not coincide with the experimental result.

## 4. Conclusion

In the produced heterostructure of (n)nc-Si:H/(p)c-Si, it is just the high resistivity amorphous buffer layer between ultrathin (n)nc-Si:H and (p)c-Si that induces the 2DEG formation at the interface. The forward current can be ascribed to tunnelling-aided carrier emission recombination. The reverse current $I_R$ can be assigned to minority carrier tunnelling through the space charge region within the reverse bias from 0 to about −10 V. On decreasing the backward bias from −10 to around −22 V, the $I_R$ can be attributed to tunnelling-assisted Poole–Frenkel emission. With further reduction of the negative applied voltage from −22 to about −38 V below 100 K, the $I_R$ staircases can be due to sequential resonant tunnelling; otherwise it can be owing to the thermic effect at higher temperatures. The main origin of the short transient time of the (n)nc-Si:H/(p)c-Si heterojunction can be attributed to tunnelling mechanism.

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