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Sources of error and methods to improve accuracy in interface state density analysis using quasi-static capacitance–voltage measurements in wide bandgap semiconductors

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ABSTRACT

Characterizing interface trap states in commercial wide bandgap devices using frequency-based measurements requires unconventionally high probing frequencies to account for both fast and slow traps associated with wide bandgap materials. The $C-\psi_S$ technique has been suggested as a viable quasi-static method for determining the interface trap state densities in wide bandgap systems, but the results are shown to be susceptible to errors in the analysis procedure. This work explores the primary sources of errors present in the $C-\psi_S$ technique using an analytical model that describes the apparent response for wide bandgap MOS capacitor devices. Measurement noise is shown to greatly impact the linear fitting routine of the $1/C_S^{*2}$ vs ψ_S plot to calibrate the additive constant in the surface potential/gate voltage relationship, and an inexact knowledge of the oxide capacitance is also shown to impede interface trap state analysis near the band edge. In addition, a slight nonlinearity that is typically present throughout the $1/C_S^{*2}$ vs ψ_S plot hinders the accurate estimation of interface trap densities, which is demonstrated for a fabricated n-SiC MOS capacitor device. Methods are suggested to improve quasi-static analysis, including a novel method to determine an approximate integration constant without relying on a linear fitting routine.

I. INTRODUCTION

The large breakdown electric field strength and high electron saturation velocity of wide bandgap (WBG) materials make them favorable candidates for high-power and high-frequency applications.[1–5] However, WBG-based structures are known to exhibit large charge trap densities at or near the dielectric/semiconductor interfaces,[6] introducing threshold–voltage instabilities in contemporary MIS (Metal-Insulator-Semiconductor) devices.[7,8] Interface trap states are also known to adversely alter the current response and channel transport dynamics in MISFET and MIS-HEMT devices.[8] Mitigating these charge traps requires reliable characterization techniques to better correlate processing methods with device performance and reliability. Furthermore, large-scale device fabrication processes would greatly benefit from simple and consistent defect characterization techniques that can be readily implemented into the manufacturing procedure. The typical techniques used to characterize the density of interface states in silicon-based systems, such as the high-low method[9] or the Terman method,[10] are not suitable for WBG-based devices because they require unconventionally high probing frequencies to account for fast trap states associated with WBG materials.[11–13] More rigorous techniques such as the conductance method[14] or deep-level transient spectroscopy[15,16] require more time-consuming measurements that hinder their adoption as a prescreening process in manufacturing.

A consistent and straightforward method for measuring interface trap densities, D_{IT}, in WBG material systems would prove invaluable in developing more robust high-power and high-frequency device technologies. The $C-\psi_S$ technique is a quasi-static capacitance–voltage characterization method used to evaluate D_{IT} distributions in WBG MOS structures and has been demonstrated extensively for SiC-based systems.[17–20] Nevertheless, Belanche *et al.* have demonstrated that the $C-\psi_S$ technique is susceptible to measurement errors.[21] Specifically, the fitting routine used for the $C-\psi_S$ technique to determine the surface potential/gate voltage calibration constant can be inconsistent and may lead to an incorrect evaluation of interface trap density distributions as a function of bandgap energy.

In this work, a SiO_2/n-SiC MOS capacitor is simulated to investigate errors in interface trap analysis using quasi-static data generated to mimic experimental measurements and demonstrate the validity of the $C-\psi_S$ technique under ideal conditions. The $C-\psi_S$ technique is then applied to simulated data generated under different measurement conditions, showing that the analysis is highly sensitive to measurement noise and an inaccurately approximated oxide capacitance. In addition, an unexplained nonlinearity present throughout the $1/C_S^{*2}(\psi_S)$ vs ψ_S plot, demonstrated on a fabricated *n*-SiC MOS capacitor device, shows a disagreement between theoretical analysis and real devices. This non-ideal behavior, most readily observed in deep depletion, hinders the accurate estimation of interface trap densities for WBG-based structures.

II. SIMULATING A WBG MOS CAPACITOR

The WBG-based MOS capacitor structure is simulated based on an *n*-type SiC substrate with a uniform doping concentration of $1.30\times10^{16}\,\mathrm{cm}^{-3}$ and a 40-nm SiO_2 gate dielectric ($\varepsilon_{SiO_2}=3.9$). The capacitance response for high-frequency measurements, C_{HF}, and quasi-static measurements, C_{QS}, are calculated as a function of surface potential, ψ_S, using the following relationships:

$$C_{QS}(\psi_S)=\left(\frac{1}{C_D(\psi_S)+C_{IT}(\psi_S)}+\frac{1}{C_{OX}}\right)^{-1}, \tag{1}$$

$$C_{HF}(\psi_S)=\left(\frac{1}{C_D(\psi_S)}+\frac{1}{C_{OX}}\right)^{-1}, \tag{2}$$

where C_D is the semiconductor depletion capacitance, C_{IT} is the interface trap state capacitance, and C_{OX} is the oxide capacitance. Equivalent circuit diagrams for each measurement configuration described by Eqs. (1) and (2) are concisely illustrated and described by Yoshioka *et al.*[17]

In a quasi-static measurement, the capacitance contribution from interface traps is determined in accordance with the time constants associated with the trap states opposite the Fermi level as a function of energy within the bandgap,

$$C_{IT}(\psi_S)=qD_{IT}(\psi_S)(1-e^{-t_0/\tau_{IT}(\psi_S)}), \tag{3}$$

where q is the fundamental charge, D_{IT} is the density of interface traps opposite the Fermi level at surface potential ψ_S, and t_0 is the integration time of the capacitance measurement. The time constant for interface trap states, τ_{IT}, is defined as

$$\tau_{IT}(\psi_S)=\frac{e^{-q\psi_S/kT}}{N_D\sigma_n(\psi_S)\nu_T}, \tag{4}$$

where N_D is the bulk equilibrium electron concentration ($N_D=1.30\times10^{16}\,\mathrm{cm}^{-3}$), ν_T is the electron thermal velocity $\left(\nu_T=1\times10^7\ \frac{\mathrm{cm}}{s}\right)$, k is Boltzmann's constant, and T is the device temperature. Reported capture cross-sectional values for the SiO_2/SiC system span a tremendous range (i.e., 10^{-12}–$10^{-23}\,\mathrm{cm}^2$), as investigated by many different techniques.[22–24] This work assumes an energy-independent capture cross section σ_n of $2\times10^{-18}\,\mathrm{cm}^2$, which agrees well with the work conducted by Yoshioka *et al.*[23]

The surface potential ψ_S is then associated with a corresponding gate voltage V_G to emulate a typical capacitance–voltage measurement using the following relationship:[25]

$$\begin{aligned}V_G=\Phi_{GS}&-\frac{Q_F}{C_{OX}}-\frac{Q_{IT}(\psi_S)}{C_{OX}}+\psi_S\\&+\mathrm{Sign}(\psi_S)\frac{kT}{q}\frac{\varepsilon_S\varepsilon_0}{C_{OX}L_D}\left[e^{\frac{q\psi_F}{kT}}\left(e^{-\frac{q\psi_S}{kT}}+\frac{q\psi_S}{kT}-1\right)\right.\\&\left.+e^{-\frac{q\psi_F}{kT}}\left(e^{\frac{q\psi_S}{kT}}-\frac{q\psi_S}{kT}-1\right)\right]^{\frac{1}{2}},\end{aligned} \tag{5}$$

where Φ_{GS} is the gate-to-semiconductor work function, Q_F is the fixed oxide charge at the interface, ϵ_S is the semiconductor dielectric constant, ψ_F is the Fermi potential of the bulk substrate, ε_0 is the permittivity of free space, and L_D is the intrinsic Debye length. In this work, Φ_{GS} and Q_F are both set equal to 0 to simplify the analysis.

Figure 1 shows the capacitance–voltage response for the simulated *n*-type MOS capacitor for various measurement configurations as a function of gate voltage. The simulated quasi-static curves utilize the D_{IT} distribution input shown in Fig. 2, while the high-frequency curve assumes no contribution from interface traps. Annotations above the plot refer to the major MOS capacitor bias regions for a WBG-based device (i.e., accumulation, depletion, and deep depletion).

For applied gate voltages that induce band bending beyond the flatband condition ($\psi_S>0$), the MOS capacitor is in weak accumulation and majority carriers collect near the dielectric/semiconductor interface. The Fermi level position at the semiconductor/dielectric interface is near the conduction band edge and can reside above the conduction band edge for sufficiently high gate voltages. In accumulation, the depletion capacitance is large, and the oxide capacitance dominates the measured capacitance of the device. As the gate voltage moves further into accumulation, the measured capacitance asymptotically approaches the oxide capacitance, as shown by the inset in Fig. 1. Continuing to increase the gate voltage will eventually induce oxide breakdown, limiting the maximum gate voltage in accumulation. Therefore, measuring a device in strong accumulation typically underestimates the true

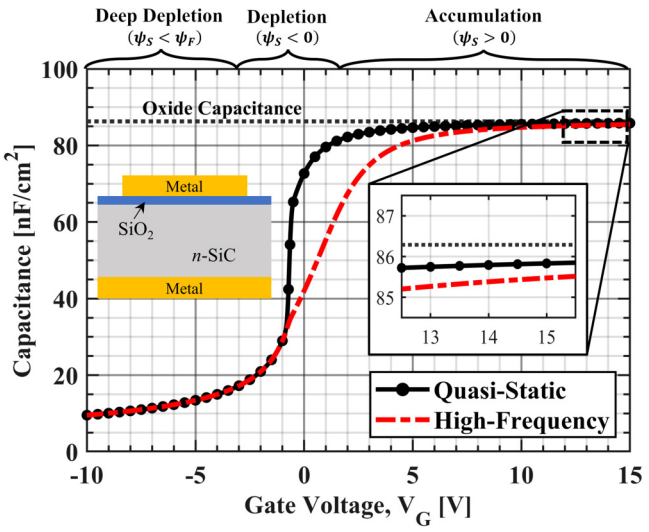

FIG. 1. An n-type (1.30×10^{16} cm^{-3}) SiC-based MOS capacitor with a 40-nm-thick SiO_2 gate dielectric is simulated to demonstrate the CV response for a quasi-static measurement and a high-frequency measurement. The quasi-static measurement includes the capacitance contribution of interface trap states, while the high-frequency measurement assumes a sufficiently fast signal that interface states cannot respond to. The inset shows how, gradually, the quasi-static and high-frequency measurements approach C_{OX} in strong accumulation. This is in part due to stretch-out of the capacitance–voltage curve along the voltage axis due to a high density of interface states near the conduction band. In WBG-based MOS capacitors, thermal generation is unable to supply holes at the interface to form an inversion layer.

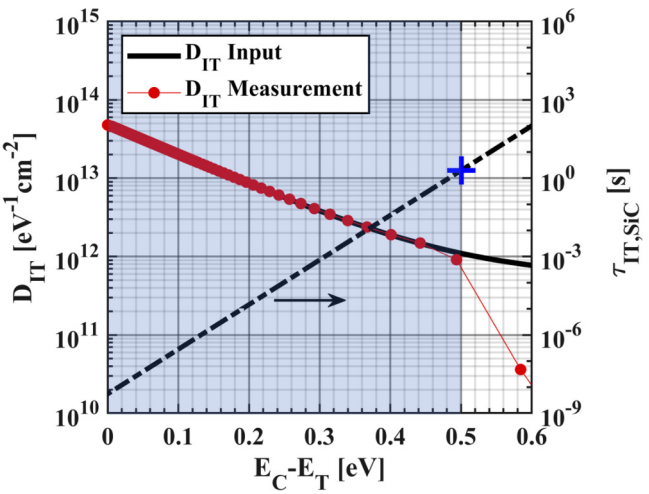

FIG. 2. The simulation D_{IT} (solid line) extends far into the bandgap. An accurate analysis (red circles) of the quasi-static capacitance–voltage curve only detects D_{IT} to about 0.5 eV below the band edge due to the exponentially increasing time constants (dashed line) of states deep in the bandgap. The blue cross symbol denotes the 2.0 s characteristic time used within the simulation. The shaded region refers to the range of energies within which interface traps can be efficiently measured.

oxide capacitance of a device. This will give rise to errors in the determination of $D_{IT}(E)$ near the conduction band, as will be shown below.

In either a high-frequency measurement or a quasi-static measurement, interface traps can exchange charge with the majority carrier band if the time constant of the states opposite the Fermi level is less than the period of the ac signal in a high-frequency measurement or less than the integration time of a quasi-static measurement. Figure 2 depicts a D_{IT} distribution that extends deep into the SiC bandgap and the corresponding $D_{IT}(E)$ detected by a simulated quasi-static measurement with integration time of 2 s and a 0.2 V step size. In addition, τ_{IT} is plotted as a function of trap energy with respect to the conduction band edge. With the assumed parameters, the simulated measurement detects interface traps up to 0.5 eV below the conduction band, below which the charge contribution precipitously dissipates.

For a large enough applied V_G, the Fermi level at the interface moves past the intrinsic Fermi level of the substrate and the device enters deep depletion. This is because in a wide-bandgap semiconductor, thermal generation is unable to supply holes to the interface to form an inversion layer. Without an external source of excitation such as photogeneration,[26] the MOS capacitor remains in deep depletion. Figure 3 illustrates the semiconductor band diagram for an n-type MOS capacitor in its various bias regions (i.e., accumulation, depletion, and inversion/deep depletion) and suggests how the distribution of interface traps are positioned relative to the Fermi level in each region. In this figure, ψ_F is the Fermi potential of the bulk substrate, E_g is the bandgap, E_F is the semiconductor Fermi energy, and E_i is the intrinsic semiconductor Fermi energy and is used as a reference energy.

III. CHARACTERIZING THE MOS CAPACITOR RESPONSE

The interface trap state density distribution as a function of bandgap energy is measured through analysis of capacitance–voltage data, from which the oxide capacitance, C_{OX}, and the gate voltage/surface potential relationship, $\psi_S(V_G)$ vs V_G, must also be determined. As previously mentioned, the oxide capacitance can be approximated by measuring the capacitance of the device in strong accumulation. The surface potential ψ_S and gate voltage V_G are found using the Berglund equation,[27]

$$\psi_{S,Berg.}(V_G) = \int \left(1 - \frac{C_{QS}}{C_{OX}}\right) dV_G + \Delta, \tag{6}$$

where Δ is an additive constant that must be determined. The D_{IT} distribution is calculated by

$$D_{IT}(\psi_S) = \frac{C_S^*(\psi_S) - C_{D,theory}(\psi_S)}{q^2}, \tag{7}$$

where $C_S^* = (C_D + C_{IT})_{QS}$ is the quasi-static semiconductor capacitance, which includes the interface trap capacitance, and $C_{D,theory}$ is

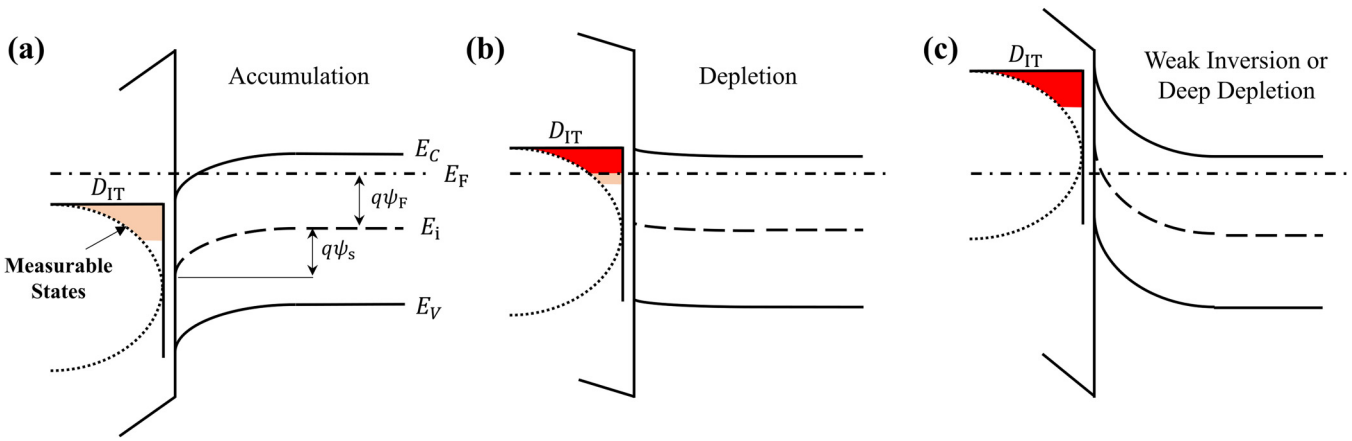

FIG. 3. (a) In accumulation mode, majority carriers (electrons) collect at the semiconductor–oxide interface, and interface trap states with energies within the bandgap are empty for sufficiently large gate voltages. (b) In depletion mode (i.e., beyond the flatband condition, $\psi_S < 0$), majority carriers move away from the interface. Interface trap states fill as the D_{IT} distribution moves across the Fermi level. For some arbitrary integration constant (e.g., 2 s), a quasi-static capacitance–voltage measurement can only detect interface states that have a time constant smaller than the integration time of the measurement. (c) In (weak) inversion mode, majority carriers have been completely depleted at the interface such that doping inversion occurs and minority carriers (holes) begin to collect at the interface. In WBG-based devices, thermal generation is unable to supply minority carriers to the interface to form an inversion layer, and the device remains in deep depletion mode.

the theoretical depletion capacitance. For an *n*-type MOS structure, the theoretical depletion capacitance is calculated by[28]

$$C_{D,\text{theory}}(\psi_S) = \frac{qN_D\left|\exp\left(\frac{q\psi_S}{kT}\right) - 1\right|}{\sqrt{\frac{2kTN_D}{\varepsilon_S}\left\{\exp\left(\frac{q\psi_S}{kT}\right) - \frac{q\psi_S}{kT} - 1\right\}}}. \quad (8)$$

The results determined by Eq. (7) are often expressed as a function of the trap energy, E_T, relative to the band edge, E_C,

$$E_C - E_T = \left(\frac{E_g}{2} - \psi_F\right) - \psi_S. \quad (9)$$

Determining the exact relationship between ψ_S and V_G from experimental data is a challenging task, given the inherent ambiguity of the integration constant Δ.[25,27] Some approaches to determine Δ rely on calculating the flatband voltage V_{FB}.[29] In the commonly used high-low method, a calculated flatband capacitance C_{FB} is compared to a high-frequency capacitance measurement that is assumed to contain no contributions from interface trap response.[9,25] While the high-low method is a common approach to determine D_{IT} in a MOS device, problems arise when the probe frequency is not sufficiently high to eliminate all interface trap responses for Fermi level positions in the range of the measurement. For WBG materials, the time constant associated with interface trap states close to the band edge becomes much smaller than the period of conventional high frequencies (~1 MHz) used in the high-low method.[12] These unaccounted-for traps lead to an inaccurate determination of V_{FB} and result in under-reporting the interface state density distribution. Accurately measuring interface trap densities using the high-low method in SiC-based devices, for example, requires unconventionally high probing frequencies (~100 MHz) to calibrate $\psi_S(V_G)$ vs V_G.[30]

Yoshioka *et al.* propose using the $C - \psi_S$ technique to account for fast trap states associated with WBG materials and remove the need for frequency-based measurements by comparing the theoretical high-frequency capacitance with a quasi-static capacitance measurement.[17] This technique recognizes that, in the linear portion of the $1/C_S^*(\psi_S(V_G))^2$ vs $\psi_S(V_G)$ relationship, the Fermi level is deep in the bandgap where interface states cannot respond during the integration time of the quasi-static measurement, and only the depletion capacitance responds. The $C - \psi_S$ technique then performs a linear fit to the $1/C_S^{*2}$ vs $\psi_S(V_G)$ plot and extrapolates to $1/C_S^{*2} = 0$ ($C_D = \infty$). Δ is then chosen so that this intercept occurs at $\psi_S = 0$. A similar technique for determining Δ is also suggested by Schroder.[25]

Here, we briefly describe a novel method to identify Δ, which first considers a $\psi_S(V_G)$ vs V_G relationship determined by[25]

$$\psi_{S,\text{Ext.}}(V_G) = -\left(\frac{q\varepsilon_S\varepsilon_0 N_D}{2C_S^{*2}(V_G)} + \frac{kT}{q}\right), \quad (10)$$

where N_D is the uniform *n*-type doping concentration. This relationship provides a viable approximation when C_S^* is measured so that interface traps do not contribute to the measurement (i.e., high-frequency capacitance–voltage measurements). As previously discussed, extracting C_S^* with minimal contribution from interface traps is difficult close to the band edge because of the extremely high frequencies needed to exclude an interface trap response. However, the approximation provided by Eq. (10) remains accurate in ideal deep depletion where interface trap time constants are longer than the time scale of the measurement process, even for quasi-static or low-frequency measurements as shown in Fig. 2.

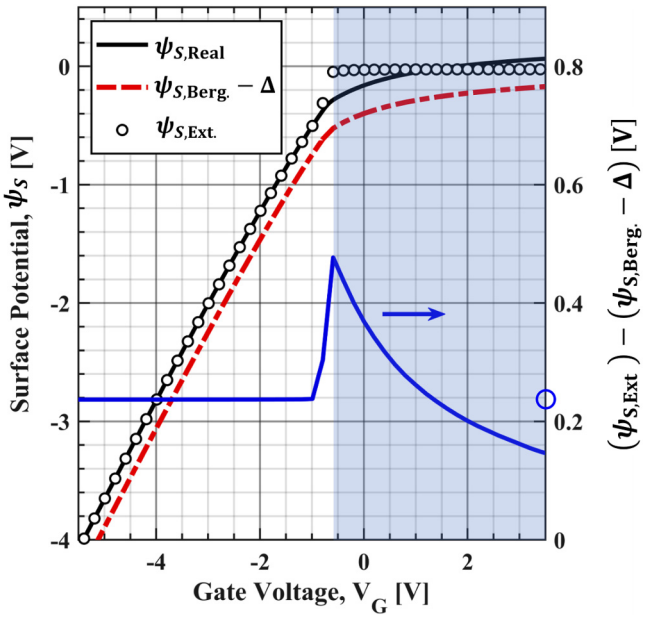

FIG. 4. The $\psi_{S,Real}(V_G)$ vs V_G relationship (solid line), calculated by Eq. (5), is accurately predicted using the Berglund equation, assuming the correct Δ value is used (dashed line). The shaded region refers to a range of gate voltages, wherein interface traps impact the measurement and corresponds to the shaded region shown in Fig. 2. In addition to the $C - \psi_S$ technique, Δ may be determined by comparing $\psi_{S,Ext.}(V_G)$ defined by Eq. (10) and $\psi_{S,Berg.}(V_G) - \Delta$ defined by Eq. (6) in deep depletion. The correct Δ value for the presently simulated structure is 240 mV, as given by the lower curve for $V_G < -1$.

Comparing $\psi_{S,Ext.}(V_G)$ and $\psi_{S,Berg.}(V_G) - \Delta$ in deep depletion and measuring the offset between the two calculations should, therefore, provide a solution for Δ. In Fig. 4, the calculated offset in deep depletion (i.e., $V_G < -1$) for the presently simulated device provides the correct Δ value of 240 mV. Additionally, the position of the maximum vertical offset observed at a gate voltage of −0.6 V directly corresponds to when the simulated interface traps would no longer efficiently exchange charge during the 2-second integration time of the quasi-static measurement (i.e., 0.5 eV below the conduction band edge).

IV. SOURCES OF ERRORS IN THE $C - \psi_S$ TECHNIQUE

Belanche *et al.* have shown that the $C - \psi_S$ technique is highly susceptible to measurement errors when determining the surface potential/gate voltage calibration constant Δ, and this may lead to an incorrect evaluation of interface trap density distributions.[21] The problem is demonstrated here on an *n*-type SiC MOS capacitor. The device is formed on a 4H-SiC (0001) epilayer with a nitrogen concentration of 1.5×10^{16} cm^{-3} as determined by high-frequency capacitance–voltage measurements. The substrate is cleaned and then oxidized in a pyrogenic furnace at 1100 °C for 130 min, followed by an 1175 °C anneal for 120 min in nitric oxide (NO). The resulting gate oxide is approximately 40-nm thick, as determined by profilometry. Circular-gate MOS capacitors are formed by thermal evaporation of a 100-nm Ni layer with a diameter of 600 μm. The backside contact is 200 nm of Al deposited by thermal evaporation.

Measurements are carried out at room temperature in a probe station connected to a Keysight B1505A power device analyzer. The quasi-static capacitance measurement with leakage compensation is recorded at gate voltage steps of 0.2 V and an integration time of 2.0 s per step and is shown in Fig. 5. The gate voltage is stepped from 20 to −20 V (accumulation to depletion) for both sets of devices. Point-to-point measurement noise is approximated by applying a Savitsky–Golay smoothing filter to the measured data,[31] then comparing the filtered result with the as-measured capacitance measurement and expressing the result as a relative percentage value. C_{OX} is estimated to be 85.88 nF/cm^2 by averaging the last five capacitance points in strong accumulation. The true C_{OX} is likely to be slightly larger than this value because the capacitance in strong accumulation never exactly reaches the oxide capacitance due to stretch-out along the voltage axis, as illustrated in the inset of Fig. 1.

Analysis of the capacitance–voltage measurement shown in Fig. 5 is conducted using the $C - \psi_S$ technique for various practical fitting scenarios to determine Δ. The linear fitting results for four different fitting scenarios of the $1/C_S^{*2}$ vs $(\psi_S - \Delta)$ plot are shown in Fig. 6(a), and all show reasonable agreement with the data. The Δ value for each linear extrapolation is the respective offset from the origin at the x-intercept, as shown in the inset of Fig. 6(a). The Δ solutions for the four fitting scenarios are 250, 190, 120, and 60 mV. The $\psi_S(V_G)$ vs V_G relationships for each fitting scenario, given by Eq. (6), are compared in Fig. 6(b). The flatband voltages are indicated by dots, with values of 4.53, 5.04, 6.02, and 8.25 V. While the differences between the Δ solutions in Fig. 6(a) seem

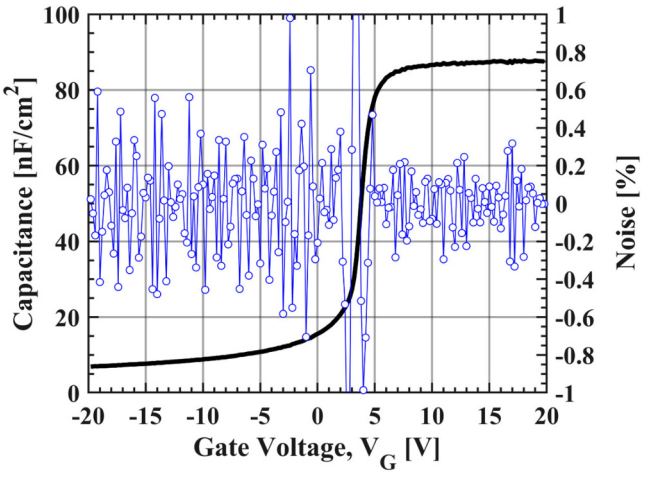

FIG. 5. Quasi-static capacitance measurement of the n-SiC device reveals an approximate C_{OX} value of 85.88 nF/cm^2. Filtering the capacitance response and comparing it with the as-measured curve demonstrates a non-negligible noise distribution (circles) present throughout the measurement.

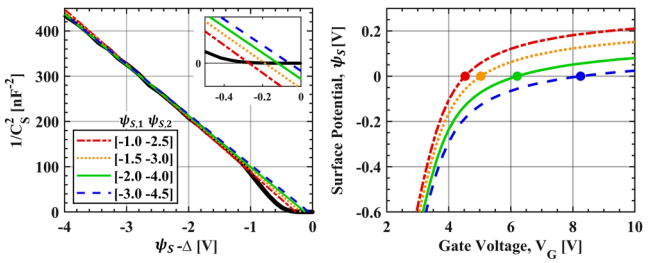

FIG. 6. The linear extrapolation of the $1/C_S^{*2}$ curve is strongly dependent on the choice of linear fitting bounds ψ_1 and ψ_2, as shown in (a). The Δ solutions for the four linear fits are 250 (double dashed), 190 (dotted), 120 (solid), and 60 mV (dashed). The $\psi_S(V_G)$ vs V_G relationships for each fitting scenario are vertically shifted from each other in accordance with their Δ solutions, as shown in (b). The respective V_{FB} values are 4.53, 5.04, 6.02, and 8.25 V, as indicated by the dots in (b).

relatively small, large shifts in V_{FB} highlight a critical issue when extrapolating a linear fit to calibrate the $\psi_S(V_G)$ vs V_G relationship.

The resulting interface trap distributions for each fitting scenario are plotted in Fig. 7, which shows that the variation in calculated D_{IT} distributions can span multiple orders of magnitude. In addition, D_{IT} values do not drop abruptly at trap energies well below the conduction band where trap response times are purportedly longer than the measurement integration time. The large inconsistencies possible using the $C-\psi_S$ technique are a cause for concern, and an analysis technique that minimizes the uncertainty

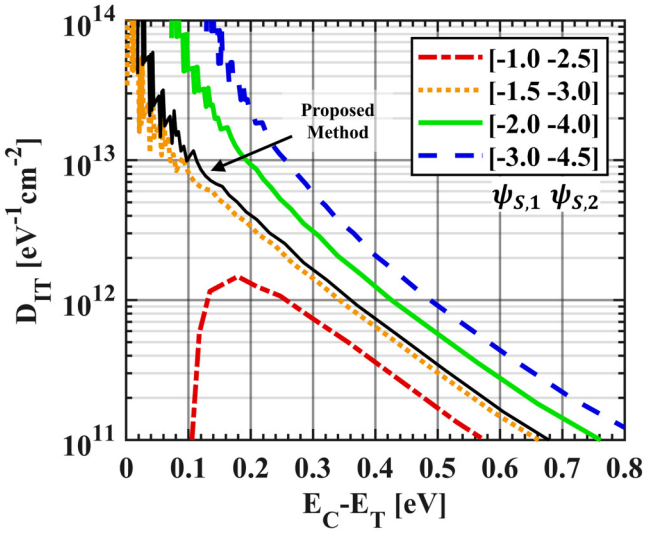

FIG. 7. The resulting distributions for each fitting-bound-dependent Δ show how D_{IT} can be over-estimated or underestimated. In addition, the inferred D_{IT} does not abruptly drop at some point below the conduction band, but rather extends deep into the bandgap. The solid black line reports the results using the proposed method discussion in Sec. IV C.

is urgently needed. In this work, the source errors in the $C-\psi_S$ technique are explored by studying the impact of random point-to-point measurement errors on an analytically modeled MOS capacitor and by comparing the simulated capacitance–voltage output with data collected from a fabricated device. Three primary sources of errors are identified and presently discussed: (1) random point-to-point measurement errors can introduce large uncertainties into the linear fitting routine, (2) an inaccurate estimation of oxide capacitance dramatically affects accuracy near the band edge, and (3) departure from ideal linearity of experimental $1/C_S^*(\psi_S(V_G))^2$ vs $\psi_S(V_G)$ plots make the linear extrapolations especially sensitive to the region of the plot chosen for the linear fit.

A. Random point-to-point measurement noise

Point-to-point measurement errors due to electrical noise (e.g., shot noise, thermal noise, and power line cycle noise) are present in any parametric test setup, though measurement strategies are typically implemented to mitigate their impact. The simulated quasi-static capacitance response influenced by point-to-point measurement errors due to electrical noise is defined by

$$C_{QS,\,Noise}(V) = C_{QS}(V)(1 + N_F\delta(V)), \tag{11}$$

where N_F is the noise factor expressed as a relative percentage value and $\delta(V)$ is a randomly generated value between −1 and +1 for each gate voltage step. The linear fitting routine considers ψ_S fitting bounds of −1 and −3 V to emulate a typical fitting range. A larger fitting range would reduce the impact of measurement noise on the linear fit, though a commonly reported nonlinearity in the measured $1/C_S^{*2}$ plot limits the range with which linear fitting can be conducted to within the depletion range of the device.[17,21]

The absolute error in the measured Δ value compared to the actual Δ is denoted as ξ_Δ. Figure 8(a) depicts the ξ_Δ probability distribution determined by the Monte Carlo method[32] for the calculated Δ value influenced by different values of N_F. The corresponding standard deviations, σ_Δ, are 5.27, 10.55, and 21.10 mV for N_F values of 0.25%, 0.50%, and 1.00%, respectively. Random point-to-point measurement noise can be mitigated by adjusting the voltage step size and quasi-static integration time.[21] However, too large of a step size reduces the number of points utilized by the linear fitting routine, and too short of an integration time limits the range from the band edge to detect interface traps.

Figure 8(b) demonstrates how the corresponding ξ_Δ distribution propagates through $C-\psi_S$ analysis and impacts the calculated D_{IT} distribution by illustrating the $\pm 3\sigma_\Delta$ bounds for each N_F value. Even for small N_F values, the uncertainty may mislead the analysis to arbitrarily suggest an increase or decrease of the semiconductor/dielectric interface quality relative to interfaces within identically fabricated devices. The wider $\pm 3\sigma_\Delta$ bound shows that the $C-\psi_S$ technique is unreliable when unmitigated point-to-point errors are present within the measurement. The noise approximation for the fabricated device shown in Fig. 5 suggests a noise factor N_F value in the range of 0.2% and 0.4%. Increasing the integration time or decreasing the voltage step size

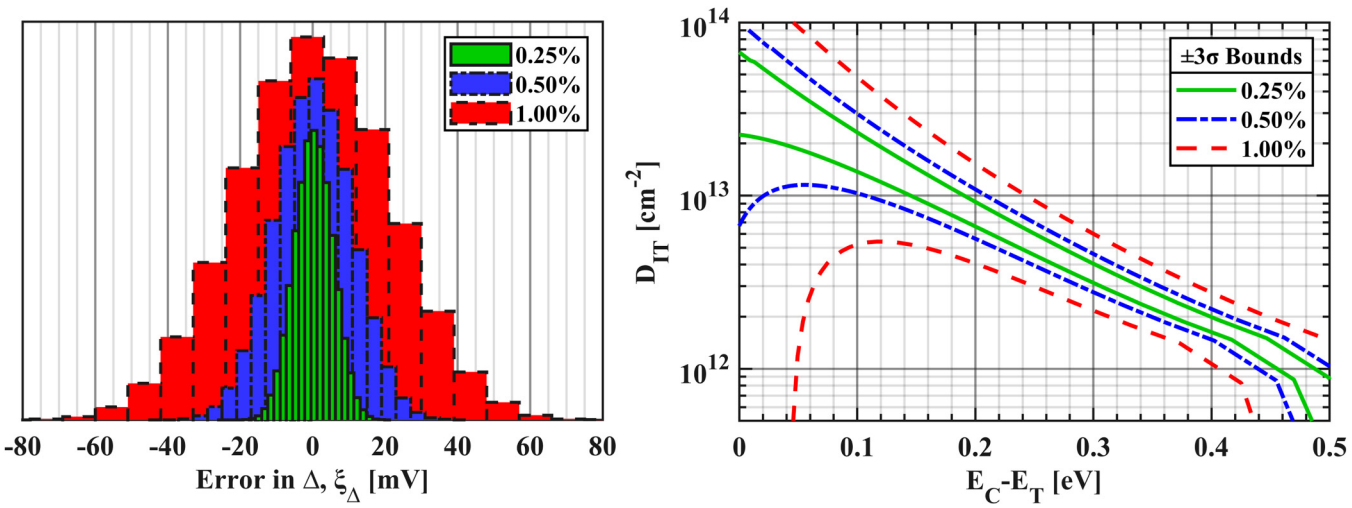

FIG. 8. (a) Each of the average N_F values imposed on the simulated signal is shown to directly impact the precision of the measured Δ and an increasing N_F value corresponds with an increasing standard deviation, σ_Δ. (b) The $\pm 3\sigma_\Delta$ bounds determined for each of the injected noise magnitudes demonstrate the wide range of D_{IT} distributions possible due to point-to-point measurement noise.

rapidly raises the approximate N_F to values higher than 1.0%. Under such conditions, the $C-\psi_S$ technique requires many repeated measurements of the same device to establish a sufficient confidence interval. In addition, quasi-static capacitance measurements may benefit from a data-filtering routine to reduce point-to-point measurement noise and increase the precision of the linear fitting routine.

B. An inaccurate approximation of C_{OX}

As discussed previously, the oxide capacitance C_{OX} value is experimentally determined by measuring the maximum quasi-static capacitance value observed in strong accumulation. The inset of Fig. 1 demonstrates how the measured C_{OX} value from the simulated quasi-static curve does not represent the actual C_{OX} value, but rather a slight under approximation. In addition, substantial oxide leakage in a real device may be incorrectly interpreted by the quasi-static measurement's leakage compensation routine to erroneously overestimate the quasi-static capacitance in strong accumulation. Measurement noise would also exacerbate the uncertainty in C_{OX}. In this work, the relative error in the measured C_{OX} value, $\bar{\xi}_{OX}$, is defined as a percentage value relative to the actual C_{OX} value used in this simulation. Due to the oxide breakdown limit or substantial oxide leakage restricting the maximum applied gate voltage and the impact of measurement noise, $\bar{\xi}_{OX}$ is reasonably expected to be in the range of ±0.5%.

Figure 9 depicts the calculated D_{IT} results from the MOS capacitor simulation, when using an exact knowledge of the integration constant Δ for a reasonable set of $\bar{\xi}_{OX}$ values, and shows a very large variation in D_{IT} results near the band edge. An inaccurate determination of C_{OX} directly alters the determination of $C_S^*(\psi_S)$, especially when the Fermi level is positioned near the band edge and, therefore, misguides the estimation of the D_{IT} distribution. For this reason, D_{IT} values reported near the band edge are unreliable and reported values should be restricted to ranges that exclude trap energies close to the band edge, unless an accurate estimation of C_{OX} is provided. This source of error in determining D_{IT} is not limited to the $C-\psi_S$ technique but extends to any capacitance-based analysis method

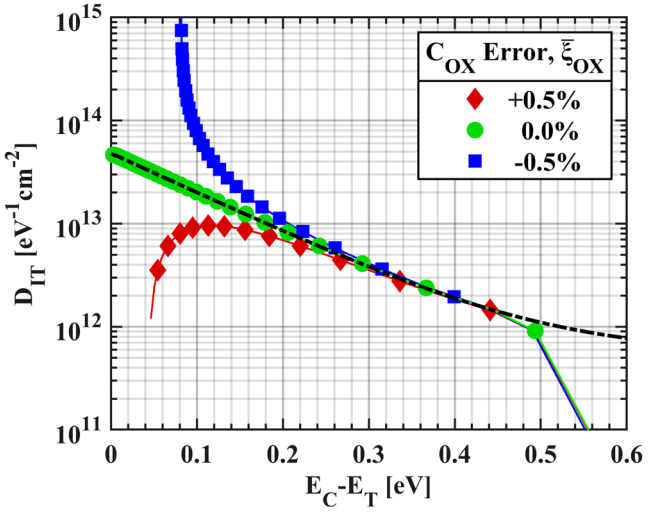

FIG. 9. Calculated D_{IT} distributions are shown to be inaccurate near the band edge for small $\bar{\xi}_{OX}$ values, which restricts the range of reliable energies for which D_{IT} values should be reported. The simulated $D_{IT}(E)$ input (double dash) is included for comparison.

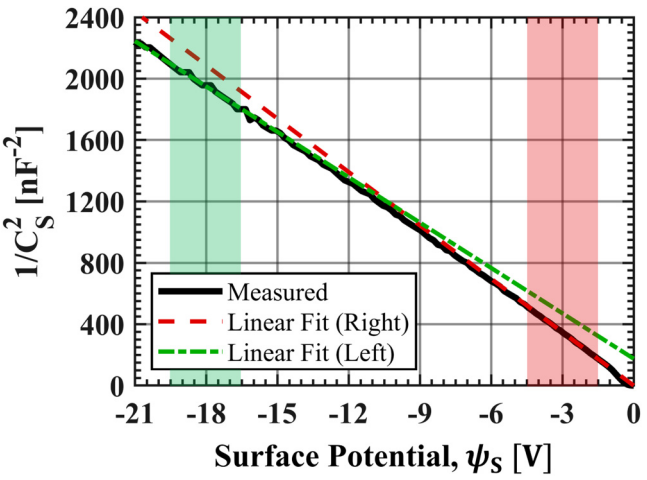

FIG. 10. The non-ideal curvature observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S plot complicates the determination of D_{IT} when using the $C-\psi_S$ technique. The shaded bands on the right and left of the figure define the fitting bounds in depletion and deep depletion, respectively.

of MOS capacitor devices, such as the high-low method or the Terman method. It is also worth noting that any technique that relies on Eq. (10) to define the $\psi_S(V_G)$ vs V_G relationship would be particularly impacted.

C. Nonlinearity in the $1/C_S^{*2}(\psi_S)$ plot deep in depletion

Figure 10 demonstrates a nonlinearity observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship for the fabricated device over a wide range of ψ_S that extends far into deep depletion. This non-ideal behavior impacts the linearity of the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship over the entire span of ψ_S and obfuscates the accurate determination of D_{IT} by the $C-\psi_S$ technique. Without an analytical description of nonlinearity as a function of an accurately calibrated ψ_S, determining a correct linear fitting range when calculating an accurate Δ is made unrealistic. Conversely, determining an accurately calibrated ψ_S to define such an analytical description requires prior knowledge of an accurate Δ. Furthermore, the additional semiconductor capacitance associated with this nonlinearity is unaccounted for in the theoretical depletion capacitance described by Eq. (8). As a result, the calculated D_{IT} distribution never permanently dissipates when measured deep in the bandgap. This is because the additional semiconductor capacitance is interpreted by the $C-\psi_S$ technique as due to an interface state contribution. In addition, this non-ideal behavior obscures the energy level within the bandgap where interface traps with time constants greater than the integration time of the measurement no longer contribute to the interface trap measurement.

The nonlinearity observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship could be attributed to slight variations in apparent doping within the depletion width of the MOS capacitor. The linear fits shown in Fig. 10 describe the apparent constant doping for the respective fitted regions by considering the following relationship:[25]

$$N_D = \frac{-2}{q\varepsilon_S\varepsilon_0 \dfrac{d(1/C_S^{*2})}{d\psi_S}}. \tag{12}$$

Assuming an average doping value over the entire range of ψ_S allows an approximate depletion depth to be calculated as a function of ψ_S. The doping observed close to the depletion region (dashed line) is calculated to be $1.52\times10^{16}\,\mathrm{cm}^{-3}$ at an approximate depth of $0.3\,\mu$m, while the doping observed far into deep depletion (double-dashed line) is calculated to be $1.70\times10^{16}\,\mathrm{cm}^{-3}$ at an approximate depth of $1.1\,\mu$m. However, the curvature observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship tends to be negative for all measured devices over many separately fabricated device sets, suggesting that doping profiles preferentially increase with increasing depth. On the contrary, epitaxial *n*-SiC grown by chemical vapor deposition techniques to form a constant doping distribution is unlikely to feature such large variations in doping over such short distances. Additional mechanisms are likely needed to explain the non-linearities observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship. In present, it is still unclear the exact cause of the nonlinearity, and additional research is required.

Figure 11 depicts the comparison of $\psi_{S,Ext.}(V_G)$ and $\psi_{S,Berg.}(V_G)-\Delta$ determined from measured data and shows that the two calculations notably diverge in deep depletion, contrary to theoretical expectations. While $\psi_{S,Ext.}$ remains accurate in deep depletion under ideal conditions, the nonlinearity observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship implies a non-ideal behavior in the C_S^* measurement and, therefore, negates the accuracy of Eq. (10) in deep depletion. However, comparing $\psi_{S,Ext.}(V_G)$ and $\psi_{S,Berg.}(V_G)-\Delta$ may still suggest an approximate Δ value by considering the region of minimum difference in deep depletion,

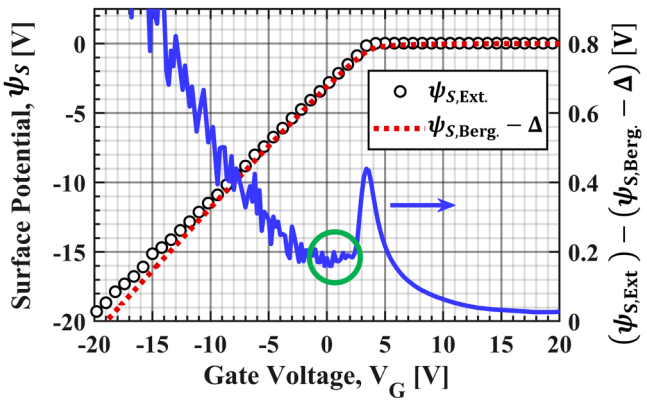

FIG. 11. Comparing $\psi_{S,Ext.}(V_G)$ and $\psi_{S,Berg.}(V_G)-\Delta$ reveals a diverging response in deep depletion, contrary to theoretical expectations. However, the circled range suggests an approximate Δ value of 180 mV without relying on a linear fit, though an exact value is still obscured by the non-ideal behavior. The position of the local maximum observed around a gate voltage of 3.4 V suggests the point when interface traps stop responding to the quasi-static capacitance measurement.

which is circled for reference, and does not rely on a linear fitting routine. Within this region, the non-ideal behavior only marginally impacts the determination of C_S^* relative to values in deep depletion. The average Δ value between gate voltages V_G of 0–2 V is 180 mV, which compares very well with the Δ values approximated by the $C-\psi_S$technique, as shown in Fig. 7. In addition, the position of the local maximum observed at a gate voltage of 3.4 V suggests the point when interface traps no longer respond to the quasi-static integration and corresponds to a $E_C - E_T$ value of 0.55 eV.

This approximation is still sensitive to the choice of C_{OX} which directly impacts the calculation of Eq. (10) by way of $C_S^{*2}(V_G)$, and special attention must be paid to ensure an accurate analysis and logical results. The non-ideal behaviors that induce a negative curvature in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship would still make this calculated value for Δ an over-approximation of the real Δ value with limited means to determine the approximate error. An over-approximation in Δ results in an under approximation of D_{IT} magnitudes. Therefore, the proposed technique would provide a lower bound for the correct D_{IT} distribution as a function of trap energy within the bandgap. In addition, without a correction for the nonlinearity observed in the $1/C_S^{*2}(\psi_S)$ vs ψ_S relationship, D_{IT} magnitudes measured deep in the bandgap, where interface trap time constants are greater than the integration time of quasi-static measurement, should not be reported.

V. CONCLUSION

In this work, a SiO_2/*n*-SiC MOS capacitor structure is modeled to investigate the accuracy of interface trap analysis using the $C-\psi_S$ technique. We find that D_{IT} distributions inferred from the $C-\psi_S$ technique are highly sensitive to measurement noise and an underestimated oxide capacitance. In addition, a small nonlinearity in experimental $1/C_S^{*2}$ vs ψ_S plots observed in most *n*-type SiC MOS capacitors deep in depletion can lead to significant errors in the determination of the additive constant in the Berglund equation, and therefore, in the energy position of the measured D_{IT}. In addition, a novel method for determining an approximate Δ value is demonstrated, which does not rely on a linear fitting routine. The discussed strategies for measuring interface traps in WBG-based systems may benefit other still-developing WBG material systems, especially those used in GaN- and Ga_2O_3-based devices. Further work will be conducted to verify the wide-ranging applicability of the proposed methods. The $C-\psi_S$ technique is a useful analytical tool for characterizing the MOS interface in wide-bandgap semiconductors, but care must be taken during both measurement and data analysis to avoid misleading and erroneous conclusions.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

B. D. Rummel: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (equal); Methodology (equal); Software (equal); Validation (lead); Writing – original draft (lead); Writing – review & editing (lead). **J. A. Cooper:** Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Software (equal); Visualization (equal); Writing – review & editing (equal). **D. T. Morisette:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (supporting); Methodology (equal); Software (supporting); Visualization (equal); Writing – review & editing (equal). **L. Yates:** Conceptualization (supporting); Supervision (lead); Writing – review & editing (equal). **C. Glaser:** Resources (supporting); Writing – review & editing (equal). **A. T. Binder:** Supervision (supporting); Writing – review & editing (equal). **K. Ramadoss:** Resources (equal); Writing – review & editing (equal). **R. J. Kaplar:** Funding acquisition (lead); Supervision (supporting); Writing – review & editing (equal).

NOMENCLATURE

C_D	Depletion capacitance
$C_{D,theory}$	Theoretical depletion capacitance
C_S^*	Quasi-static semiconductor capacitance
C_{FB}	Flatband capacitance
C_{HF}	High-frequency device capacitance
C_{IT}	Interface trap state capacitance
C_{OX}	Oxide capacitance
C_{QS}	Quasi-static device capacitance
D_{IT}	Density of interface traps
Δ	Integration constant for the Berglund equation
E_C	Conduction band edge energy
E_g	Semiconductor bandgap
E_F	Semiconductor Fermi energy
E_i	Intrinsic semiconductor Fermi energy
E_T	Interface trap energy
ε_S	Semiconductor dielectric constant
ε_{SiO_2}	Oxide dielectric constant
ε_0	Permittivity of free space
k	Boltzmann constant
L_D	Intrinsic Debye length
N_C	Effective density of states in the conduction band
N_D	Bulk equilibrium electron density
N_F	Noise factor
v_T	Electron thermal velocity
ξ_Δ	Relative capacitance measurement error

$\bar{\xi}_{OX}$	Relative oxide capacitance error
Q_F	Fixed oxide charge
Q_{IT}	Interface trap charge
q	Universal charge constant
σ_Δ	Standard deviation due to measurement noise
σ_n	Capture cross section
T	Device temperature
t_0	Integration time for the quasi-static measurement
τ_{IT}	Interface trap time constant
V_{FB}	Flatband voltage
V_G	Gate voltage
Φ_{GS}	Gate-to-semiconductor work function
ψ_F	Fermi potential of the bulk substrate
ψ_S	Fermi potential at the substrate surface
$\psi_{S,Berg.}$	Surface potential predicted by Eq. (6)
$\psi_{S,Ext.}$	Surface potential predicted by Eq. (10)

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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