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# Automatic full quantum analysis of *CV* measurements for bulk and SOI devices

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ABSTRACT

We propose a new automatic method for analysing capacitance versus voltage measurement of metal–oxide–semiconductor (MOS) devices. Based on a quantum simulation of the semiconductor capacitance, this method allows the extraction of the flat band voltage and equivalent oxide thickness even if only a small part of the measurement is relevant. This is a strong advantage for analysing different capacitances in one time, as well as dealing with high interface states densities. Moreover, this method can be applied in accumulation regime as well as in inversion regime. It is consequently a good solution to deal with SOI devices.



## 1. Introduction

The control of the equivalent oxide thickness (EOT) and flat band voltage ($V_{fb}$), is a key factor in the development and production of new MOS architectures. Indeed, during the production, time dependent process deviations can occur, they can be monitored by a continuous analysis of EOT and $V_{fb}$ variations. In the development of new materials, we need to evaluate their properties in the gate stack. High-$\kappa$ are a good example of such development, they are integrated in MOS devices to reduce the gate leakage currents as well as the EOT. However, the study of the $V_{fb}$ versus EOT dependency has shown a strong reduction of $V_{fb}$ induced by the High-$\kappa$ as the EOT is thinning (roll-off) [1]. More generally, $V_{fb}$ and EOT are of first importance for the study of new materials, especially for the extraction of the gate's effective work function, which cannot be performed if only the threshold voltage ($V_{th}$) is known [2]. The measurement of the capacitance versus voltage (*CV*) response of a MOS device is a simple way to obtain these parameters, but an automatic extraction can be tricky. Indeed, without human control, high leakage current or interface states densities (Dit) can lead respectively to a wrong evaluation of EOT or $V_{fb}$. Moreover, the extraction of these parameters is usually performed when the capacitor is in accumulation, which is not suitable for the study of SOI devices. For such devices only the inversion capacitance can be measured from $C_{gc}$ (gate to channel capacitance). Here, we present a new fast and reliable extraction method that deals with Dit's, leakage current and SOI devices.

## 2. Method

Among the various methods used to extract $V_{fb}$ from *CV*, a method dealing with *CV* curves deformed by high leakage current in strong accumulation already exists [3]. This method is based on the Maserjian function $Y$ ($Y = C'/C^3$) [4]. However, $Y$ is based on the $C(V)$ derivative, which is strongly inaccurate in case of stretched *CV* curves [5]. Moreover, as $Y$ is independent of the EOT, another method must be used to extract this parameter, usually based on the maximal accumulation capacitance ($C_{max}$). It leads to inaccuracies because the quantum effects are neglected as well as the $C_{max}$ reduction due to high leakage currents. In our previous work [5], we proposed an alternative method, which deals with both stretched capacitors and high leakage current *CV* alterations. It uses a Poisson–Schrödinger simulation of the capacitance to automatically fit the *CV* measurement at $V_{fb}$ and an other bias $V_{max}$ in the accumulation part of the measurement, non-affected by high leakage current *CV* alterations. This method is based on the assumption that a $V_{fb}$ condition exists. However when *CV* curves are affected by interface states, the capacitance $C$ at $V_{fb}$ is no longer relevant and both methods are almost equivalent, leading to erroneous $V_{fb}$ extraction (Fig. 1). In Fig. 1, one of the experimental *CV* curves (large dots) has been fitted (corresponding simulation is with dashed lines) through previous methodology [5] leading to large discrepancies. With our new method, we want to be able to extract $V_{fb}$ and EOT from any significant part of the *CV*

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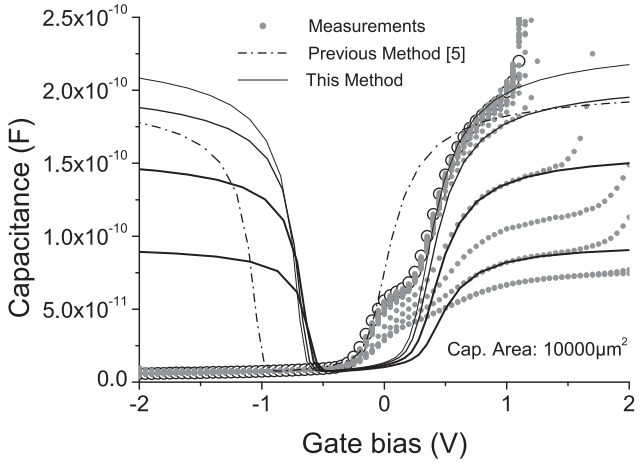


**Fig. 1.** Set of experimental *CV* curves obtained on a $SiO_2$ bevel on N silicon substrate, with upper $HfO_2$ layer and TiN gate (dots) compared to quantum simulation related either to previous extraction method [5] (dashed line) or this new extraction method (full lines).

curve, contrary to the previous ones for which we are limited to the region near $V_{fb}$.

The capacitance response of an ideal MOS device ($C_{MOS}$) results from the serial combination of three capacitances (Eq. (1)): $C_{ox}$, the dielectric capacitance; $C_S$ and $C_G$, respectively the substrate and gate capacitances

$$\frac{1}{C(V_G)} = \frac{1}{C_S} + \frac{1}{C_{ox}} + \frac{1}{C_G} \tag{1}$$

$C_S$ and $C_G$ (as well as the surface potentials $\psi_s$ and $\psi_g$) dependencies with the substrate charge $Q$ were previously calculated using our Poisson-Schrödinger simulator for different doping levels ($N_{dop}$). The results are stored in a database, which is used for *CV* analyses. The previous method which automatically extracts a simulation crossing experimental at $V_{fb}$ and $V_{max}$ is presented in Ref. [5]. In this new extraction method, for a certain measurement ($C_{Meas}$), we define two voltages ($V_{G1}$ and $V_{G2}$) between which the *CV* curve can be considered as non-distorded by interface states or leakage induced alterations (Fig. 1). In case of interface state parasites, $V_{G1}$ is the maximum accumulation bias non-altered by leakage current and $V_{G2}$ is the minimum accumulation bias non-altered by interface states. They can be determined from a fast visual analysis on a whole set of *CV* curves, as in Fig. 1. Once determined, simulations crossing experiment at $V_{G1}$ and $V_{G2}$ are then automatically extracted without any further operator intervention, identifying then $V_{fb}$ and EOT. In Eqs. (2a) and (2b), we express the relationship resulting from such conditions, the challenge is to find the substrate charge densities $Q_{S1}$ and $Q_{S2}$ that respectively correspond to the gate bias $V_{G1}$ and $V_{G2}$

$$\frac{\varepsilon_{ox}}{C_{Meas}(V_{G1})} - \frac{\varepsilon_{ox}}{C_S(Q_{S1})} = EOT = \frac{\varepsilon_{ox}}{C_{Meas}(V_{G2})} - \frac{\varepsilon_{ox}}{C_S(Q_{S2})} \tag{2a}$$

$$\frac{1}{C_{Meas}(V_{G1})} - \frac{1}{C_{Meas}(V_{G2})} + \frac{1}{C_S(Q_{S1})} - \frac{1}{C_S(Q_{S1} - \Delta Q_S)} = 0 \tag{2b}$$

$$\Delta Q_S = \int_{V_{G1}}^{V_{G2}} C_{Meas}(V_G) dV_G \tag{3}$$

This can be simplified since $\Delta Q_S$, the difference between $Q_{S2}$ and $Q_{S1}$, can be obtained by integrating $C_{Meas}$ from $V_{G1}$ and $V_{G2}$ (Eq. (3)). $Q_{S1}$ can be determined by solving Eq. (2b). Notice that Eqs. (2a) and (2b) correspond to gate with no depletion. EOT is then obtained from $Q_{S1}$ (Eq. (2a)) and $V_{fb}$ is calculated (Eq. (4)) using $\psi_S$ and $\psi_G$ (both reported in the database). Fig. 1 shows that this method allows a correct extraction of the flat band voltage even with a small part of the *CV* curve. As expected the simulation now correctly fits the measurement in accumulation. In term of $V_{fb}$ the difference between old and new method is huge and a 200 mV variation is often seen

$$V_{fb} = V_{G1} - \psi_S(Q_{S1}) + \psi_G(-Q_{S1}) + \frac{Q_{S1}}{C_{EOT}} \tag{4}$$

## 3. Bulk devices with Dit's

One major issue of the new material integration is the control of $V_{th}$. The main parameter involved in $V_{th}$ control is the Effective Metal gate Work Function ($EWF_M$). However, $EWF_M$ is influenced by many parameters such as stack materials and also process parameters [6]. Understanding $EWF_M$ variations requires a reliable determination of $EWF_M$, which can be obtained from $V_{fb}$. $V_{fb}$ is defined by three parameters: $EWF_M$, the interfacial charge densities and the substrate doping level. The study of $\Delta V_{fb}$(EOT) leads to a reliable extraction of $EWF_M$ [2] ($\Delta V_{fb}$ is the flat band voltage referenced to the silicon substrate mid-gap). However this study requires the analysis of many MOS devices, for this reason a reliable automatic extraction is much appreciated.

In the following example, we study the influence of the substrate doping type on $EWF_M$. To do this, we performed *CV* measurements on the same MOS stacks either on P-type or N-type substrates. These stacks consist of a bevelled $SiO_2$ layer covered by 2 nm thick $HfO_2$ layer, the gate is a 2 nm thick TaN layer. For Hf-based gate stacks, Interface states are mainly located in the upper part of the gap [7] explaining the hump on the experimental *CV* of Fig. 1, which corresponds to N-substrate capacitor. Same gate stacks processed on P-substrate do not exhibit such *CV* alterations due to interface states. Thanks to the bevelled $SiO_2$, layer we obtained several EOTs on a single wafer. Fig. 2 shows the $\Delta V_{fb}$(EOT) plot for N- and P-MOS capacitors extracted with the *Y* based method and our new method. We first notice that at the smallest EOT, $V_{fb}$ roll-off occurs. The phenomenon occurs only for the first 2 nm of interfacial $SiO_2$ dielectric [8] and $V_{fb}$ can be considered as relevant for $EWF_M$ extraction for EOT larger than 2.5–3 nm. Therefore, our $EWF_M$ extraction will be performed for EOT between 2.5 and 4 nm. For NMOS (P-substrate), all methods lead to the same extraction for $V_{fb}$ and EOT, and $EWF_M$ is around 0.05 eV below equivalent mid-gap. For PMOS (N-substrate), $V_{fb}$ and EOT extracted with the *Y* based method are significantly lower. Similar

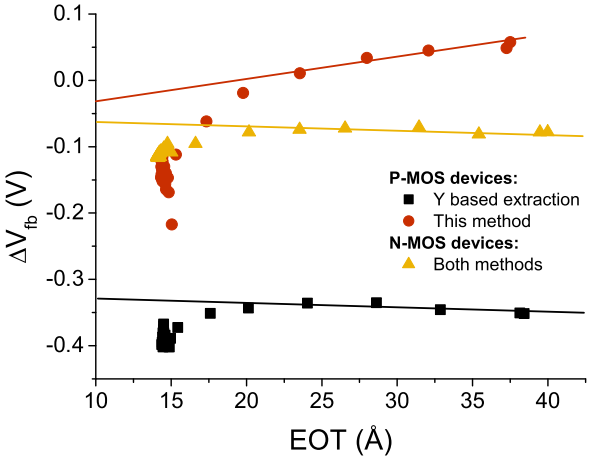


**Fig. 2.** Flat band voltage referenced at silicon mid-gap ($\Delta V_{fb}$) versus EOT for the gate stack identified in Fig. 1, two different substrate type and various extraction methods.

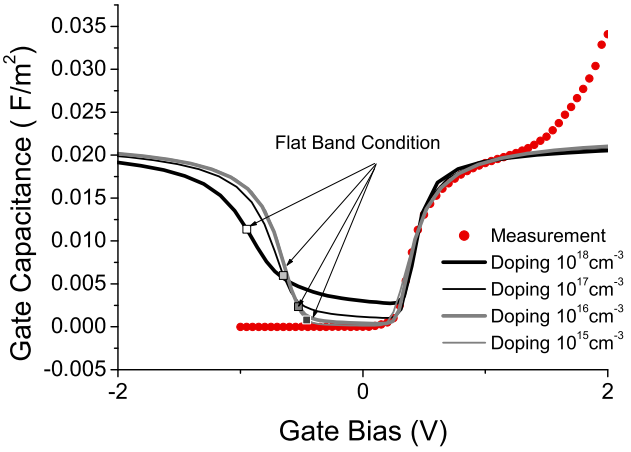


**Fig. 3.** Comparison of one NMOS fully depleted SOI device characteristic (dots) to quantum simulations at different substrate doping levels, allowing extraction of $\Delta V_{fb}$.

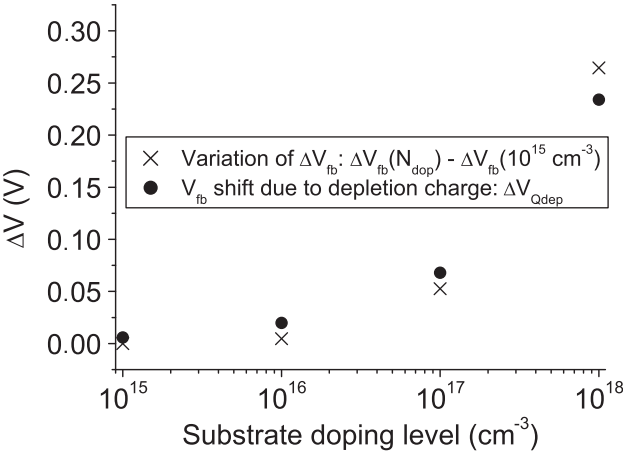


**Fig. 4.** $\Delta V_{fb}$ and $\Delta V_{Qdep}$ obtained for different doping levels, $\Delta V_{Qdep}$ is the $V_{fb}$ shift due to depletion charge ($\Delta V_{Qdep} = Q_{dep}/C_{ox}$).

results would also be obtained with our previous method [5] (see Fig. 1). All these more classical methods lead to a 250 meV smaller $EWF_M$ on an N-substrate, compared to the P-substrate results. The extraction with our new method is able to get rid of interface state parasites and we get a value similar to the one obtained on P-substrate. The difference in $\Delta V_{fb}$(EOT) slopes between N- and P-substrate also indicates interface state occurrence in upper part of silicon gap, leading to interface negative charges in case of N-substrate.

## 4. Study of SOI devices

This method can be easily applied in case of SOI devices. For such devices we work on the gate to channel *CV* measurement. It implies that $V_{G1}$ and $V_{G2}$ must be taken in the inversion regime of the *CV* curve. The main problem is the choice of $N_{dop}$. To study the impact of $N_{dop}$ choice on the extracted $V_{fb}$, we performed several extractions with different $N_{dop}$ on the same device. We found

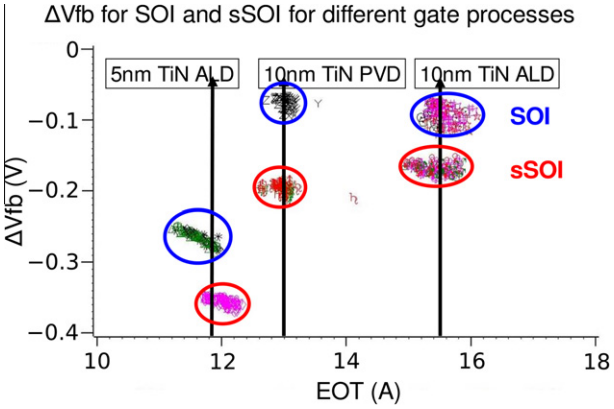


**Fig. 5.** $\Delta V_{fb}$ versus EOT for the study of TiN gate process and substrate SOI type on the effective gate stack work function.

that inversion can always be simulated even with a high $N_{dop}$ but $V_{fb}$ shows wide variations (Fig. 3). Indeed, since we fit in inversion, $V_{fb}$ does not only depend on the substrate Fermi level as in the bulk case, but also on the depletion charge influence ($\Delta V_{Qdep} = Q_{dep}/C_{ox}$). This dependency is highlighted on Fig. 4 where we observe that $\Delta V_{fb}$ and $\Delta V_{Qdep}$ have the same evolution with $N_{dop}$. However, the magnitude of this dependency decreases with $N_{dop}$, therefore, a good choice for extracting $\Delta V_{fb}$ is a low doping level of about $10^{15}$ cm$^{-3}$.

As an example, Fig. 5 shows the result of a study on SOI devices. The samples are Metal/High-$\kappa$ transistors performed on SOI and strained SOI (sSOI). The Metal is a 5 or 10 nm thick ALD or PVD TiN layer. The High-$\kappa$ is a 2.5 nm thick HfZrO layer. One can see that the reduction of the ALD TiN thickness induces a 0.2 eV $WF_M$ reduction and also reduces the $SiO_2$ bottom layer regrowth of about 4 Å. Compared to PVD, ALD seems to enhance the $SiO_2$ regrowth. To finish, one can see that the use of strained SOI induces a 0.1 eV $WF_M$ lowering which is independent of the gate process.

## 5. Conclusion

We have developed a new fast and reliable method to automatically analyse any *C*(*V*) measurements. This method uses a database obtained from PS simulations. It consequently accounts for quantum effects. The main advantage of this method is its capability of determining $V_{fb}$ and EOT from a small part of a *C*(*V*) measurement. We show that, in case of high interface states density, applying any method identifying $V_{fb}$ from its capacitance value can lead to errors in $V_{fb}$. Our new method can be successfully applied in the case of large Dit's and SOI devices to monitor $EWF_M$ variations.

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