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Study of Electron Traps Associated With Oxygen Superlattices in n-Type Silicon

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In this paper, the deep levels found by Deep-Level Transient Spectroscopy in Si-O superlattices (SLs) on n-type silicon are reported. Samples have been grown with one, two or five silicon-oxygen layers, separated by 3 nm of silicon. A Cr Schottky barrier (SB) is thermally evaporated on top of the SL. Similar as for p-type silicon, no deep levels have been found for a bias pulse in depletion, while a broad distribution of electron traps shows up when pulsing into forward bias. At the same time, these bands are absent in a zero SL reference sample. Similar as for the p-type results, the trap filling of the electron states exhibits a logarithmic capture. The possible origin of this slow filling will be discussed.

1. Introduction

Oxygen superlattices (SLs) in silicon have received quite some attention, related to the fact that they could enable the fabrication of a higher mobility silicon channel, without the need for implementing strain.[1–3] Electron mobility enhancement has been demonstrated experimentally, for nMOSFETs with an oxygen-inserted silicon channel.[3,4] This is based on the quantum confinement of the electron wave function in the (100) transport plane, yielding a reduction in the transport effective mass and a boost of the electron mobility.

While the presence of oxygen on a silicon surface is normally detrimental for good quality epitaxial deposition, the growth of crystalline oxygen SL in Molecular Beam Epitaxy (MBE)[1–4] and more recently, Chemical Vapor Deposition (CVD)[5] has been demonstrated. The elimination of extended defects (stacking faults) is important in order to obtain the mobility enhancement required for boosting the CMOS transistor performance [6]. This is related with the presence of defect-related deep level centers in the SL, which can trap and scatter free carriers.

It has been reported before that a broad distribution of near mid-gap hole traps is present in p-type Si containing a Si-O SL, as determined by Deep-Level Transient Spectroscopy (DLTS).[7,8] In addition, it has been shown that the parameters of the hole traps (activation energy, hole capture cross section and concentration) strongly depend on the number of periods and the thickness of the epitaxial silicon interlayer.[8] Several possible origins for the observed Density-of-States (DOS) have been considered. A first possibility is the formation of oxygen-clustering-related shallow thermal donors,[9–12] which has definitively been ruled out in previous work.[7,8] Other candidates are the dangling bond (P_b) defects present at the Si-SiO_2 interface and giving rise to a donor level at about 0.3 eV from the valence band maximum E_V.[13–19] However, the observed hole traps have usually a higher activation energy, particularly for a higher number of Si-O layers. In addition, a recent Electron Paramagnetic Resonance (EPR) study indicated no dangling bonds above the estimated detection limit of $\approx 10^{11}\,cm^{-2}$.[20] Finally, the results of[7,8] have been interpreted in terms of point-defect clusters, showing extended-defect-like behavior. This was based on the fact that the capture kinetics of the hole traps is logarithmic with the filling pulse duration t_p. In other words, the underlying deep-level defects are not independent of each other and obstruct the carrier trapping by other neighboring states as soon as they are filled. The progressive filling of the deep states with increasing capture time builds up a potential barrier, opposing further capture and resulting in a cross section which reduces with time.

It is the aim here to extend the study to n-type silicon containing oxygen atomic layers (ALs). In this case, Cr Schottky barriers have been fabricated in order to keep the thermal budget low, so not to change the as-grown defect levels in the SL layers. It is shown that, similar as for p-type material, a band of electron traps is formed, which also exhibits logarithmic filling. In this case, there is a tendency for the DOS to shift toward the conduction band minimum with increasing number of layers.

2. Experimental Details

The SLs have been deposited on 200 mm n-type Czochralski (CZ) silicon substrates after a high-temperature pre-epi bake,

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removing the residual native oxide. CVD of a silicon epi layer at ≈500 °C using SiH_4 is followed by the Atomic Layer Deposition (ALD) of oxygen atomic layers at 50 °C using O_3 as an oxygen precursor. It has been shown that both a H-termination of the silicon surface before ALD and a partial sub monolayer oxygen coverage are crucial for a good epitaxial continuation of the several periods SL.[5,6] Further processing details can be found elsewhere.[6,21]

Cr Schottky barriers have been thermally evaporated on the SLs with a different number of periods (1, 2, and 5), in order to enable DLTS analysis. Circular dots with a diameter of 0.5 mm have been selected. Aluminum was evaporated as ohmic contact to the n-type substrate. The device structure is schematically represented in **Figure 1**. Current-Voltage (*I*–*V*) and Capacitance-Voltage (*C*–*V*) measurements at a frequency f=1 MHz have been performed at room temperature and lower temperatures (**Figure 2**). From the *C*–*V* a doping density of $\approx 1\text{–}2 \times 10^{14}\,cm^{-3}$ has been derived typically. Similar results have been obtained for the SB containing a Si-O SL. This implies that the presence of a superlattice does not affect the doping density in the n-type substrate – it mainly has an impact on the barrier height $q\Phi_B$ and, hence, the current[8]: $q\Phi_B$ was found to reduce slightly from 0.75 eV for the 0, 1, and 2 period SL to 0.72 eV for the 5 period barrier. One can observe in Figure 2a that the forward current suffers from a rather high series resistance at lower temperatures, while the reverse current obviously reduces with T as well.

Fourier transform (FT-) DLTS[22] has been applied using several bias pulses from a reverse bias V_R to a pulse bias V_P, which probe either the depletion region of the near surface layer, containing the SL, or the silicon substrate. The pulse is applied with a period t_w and a duration t_p. The temperature of the SB is varied between 70 and 300 K using a liquid-nitrogen flow cryostat for temperature-scan (T-scan) DLTS.

3. Results

According to **Figure 3**, no electron traps are present above 70 K in the reference no SL sample for a bias pulse from −4 to −1 V. This means that the n-type silicon substrate is free of defects above the detection limit of the method, that is, with a concentration higher than about $2 \times 10^{10}\,cm^{-3}$.

When pulsing closer to the surface, approximately up to the flat-band condition from −1 to +0.5 V, a small peak appears at 80 K, whose origin is presently unknown. The estimated trap concentration is in the range of $1 \times 10^{12}\,cm^{-3}$. Compared with the 2-period SL of **Figure 4**, a different picture emerges. Again, no electron traps are present in the deep depletion region, a few μm from the silicon surface. At the same time, a broad peak is present for the 0 to +2 V spectrum around 180 K. It is broader than a typical point-defect peak so that it can correspond to a density of states, associated with an extended defect for example.

The spectra corresponding with a 5-period SL sample are shown in **Figure 5**, confirming the results for the 2-period sample. The main difference now is that the peak maximum occurs at lower temperature (≈130 K). At the same time, the peak

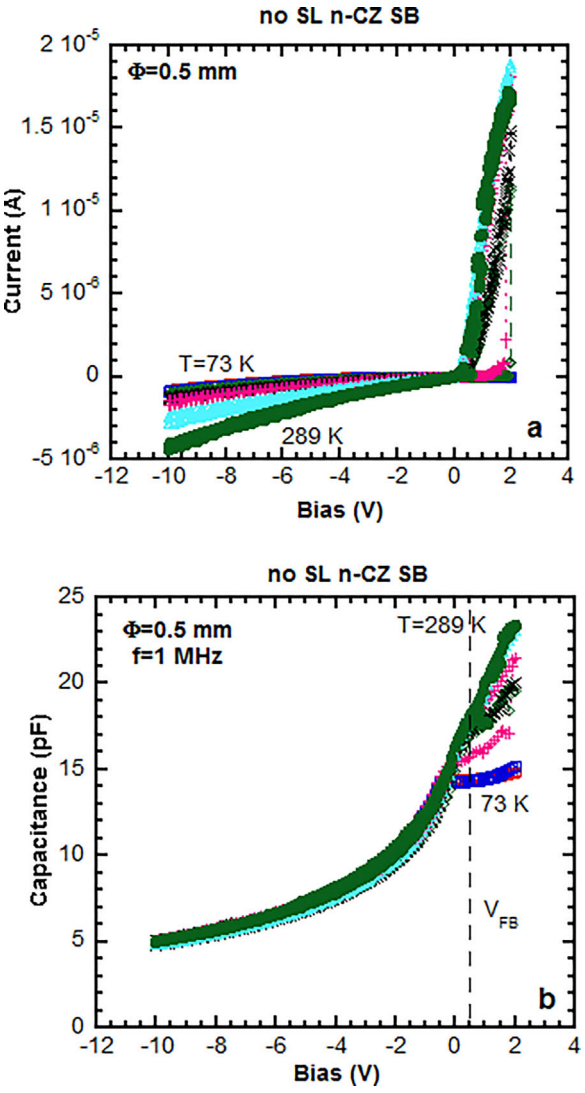

Figure 2. *I*–*V* (a) and *C*–*V* (b) characteristics at different temperatures between 73 K and RT of a 0.5 mm Cr SB on n-type silicon without SL. V_{FB} corresponds with the flat-band voltage condition.

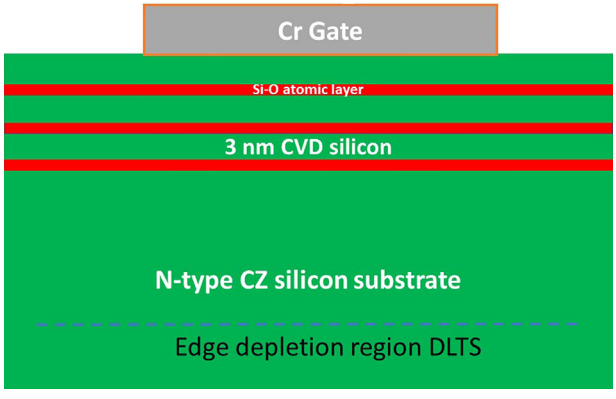

Figure 1. Schematic representation of a Cr Schottky barrier on a 3 period Si-O superlattice on n-type Czochralski silicon. Also indicated by the dashed line is the edge of the depletion region at reverse bias V_R during DLTS.

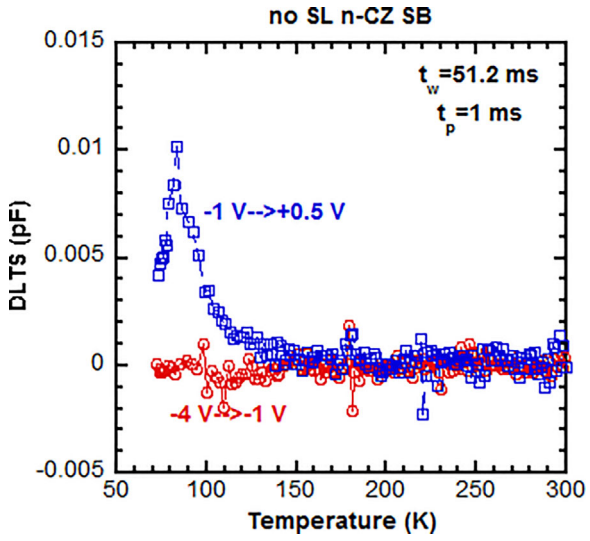

Figure 3. Temperature-scan DLTS for a Cr SB on a no SL n-type CZ silicon sample. A sampling period t_w of 51.2 ms and a pulse duration $t_p = 1$ ms have been used. Bias pulses were from −4 V–>−1 V (bulk) and from −1 V to +0.5 V (interface).

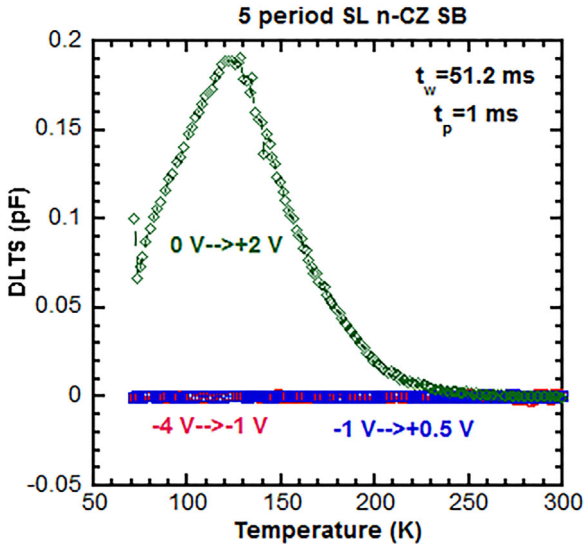

Figure 5. Temperature-scan DLTS for a Cr SB on a 5 period SL n-type CZ silicon sample. A sampling period t_w of 51.2 ms and a pulse duration $t_p = 1$ ms have been used. Bias pulses were from −4 V–>−1 V (bulk), −1 V to +0.5 V (interface) and 0 V–>+2 V.

is wider but with a two times smaller amplitude. The broadness of the peak is in fact further enhanced when measuring at a smaller t_w, for the same bias (**Figure 6**).

4. Discussion

Summarizing the previous observations, the presence of a Si-O SL in n-type CZ Si gives rise to a broad DLTS peak, corresponding with a distribution of electron traps. There is a tendency to shift toward the conduction band going from two to five periods, which is opposite to the trend for the hole traps in p-type material, where the average activation energy increases with increasing SL thickness.[8] In other words, the SL-related states move away from the valence band edge for an increasing number of periods. Although different n- and p-type SB samples have been used, it strongly indicates that the SL introduces a band of hole traps in the bottom half and a band of electron traps in the upper half of the band gap.

It has been concluded previously that the hole traps belong to extended defects (or clusters of point defects) induced by the SL growth.[8] However, an alternative explanation is that deep levels

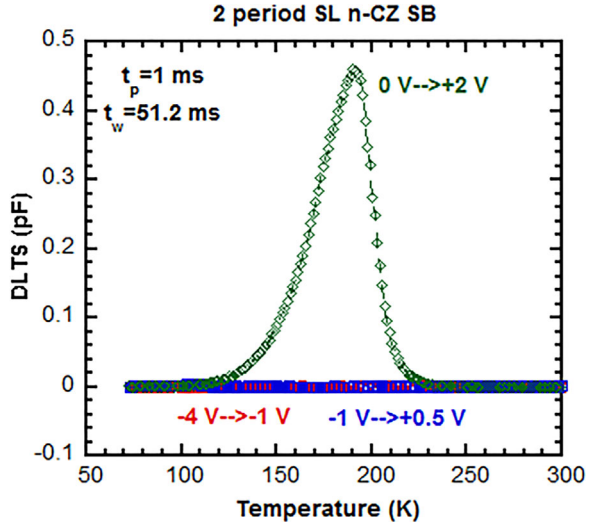

Figure 4. T-scan DLT-spectra at a sampling period $t_w = 51.2$ ms, a pulse duration $t_p = 1$ ms. The spectra correspond with three different bias pulses, from −4 V–>−1 V; −0.5 V–>+0.5 V and 0 V–>+2 V.

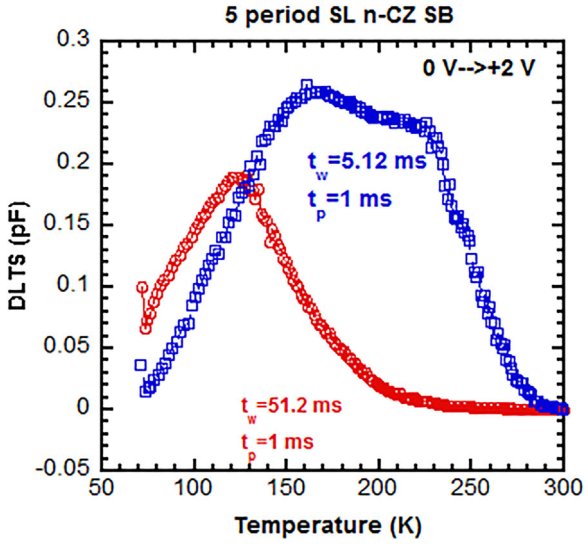

Figure 6. Temperature-scan DLTS for a Cr SB on a 5 period SL n-type CZ silicon sample at a pulse from 0 V to +2 V. The spectra correspond with a sampling period of 51.2 or 5.12 ms and a bias pulse of 1 ms, respectively.

in the SL layer are not independent of each other, which could explain the logarithmic capture kinetics. This has been suggested in the context of the deep levels associated with InAs quantum dots (QDs).[23] Charging of one QD with electrons creates a Coulomb blockade barrier for the capture by a neighboring dot, resulting in the observed behavior. A similar mechanism can be envisaged for the deep levels of the Si-O SL layer, which are in principle located at the oxygen atomic layer in the (100) plane of the wafer. It has been shown previously that a peak DOS in the range of $\approx 10^{12}\,cm^{-2}\,eV^{-1}$ can be reached in p-type Si,[7] which places a defect state every 10 nm on the average. This is much smaller than the extent of a possible Coulomb repulsive potential.

In order to investigate this hypothesis, a detailed study has been performed of a 1-period SL, which does not suffer from the impact of further Si-O layers. The resulting DLT-spectra are shown in **Figure 7**. Again, a broad peak of electron traps is found, with a maximum temperature T_m around 210 K. This confirms the trend of a downward shift of the activation energy of the peak maximum with increasing number of periods. This corresponds with a reduction of the average activation energy of the SL-related band of states in n-type Si, for an increasing number of periods. The peak height is comparable with the 2-period case of Figure 4.

The next step is to investigate the filling kinetics as a function of t_p, which is shown in **Figure 8**. One can clearly see that over the range from 10 µs to 10 ms the DLTS amplitude is not saturated and increases more or less in a logarithmic way. This is similar to the behavior of the hole traps in p-Si,[8] emphasizing the connection between the deep levels in the n- and p-type silicon.

For a further identification of the type of states, it has been suggested to compare the amplitude-normalized spectra,[23,24] as has been done in **Figure 9**. One can observe that in good approximation, the high-temperature side of the peaks overlaps for the different pulse durations, while there is a more or less parallel shift of the low-temperature flank with increasing t_p. The peak

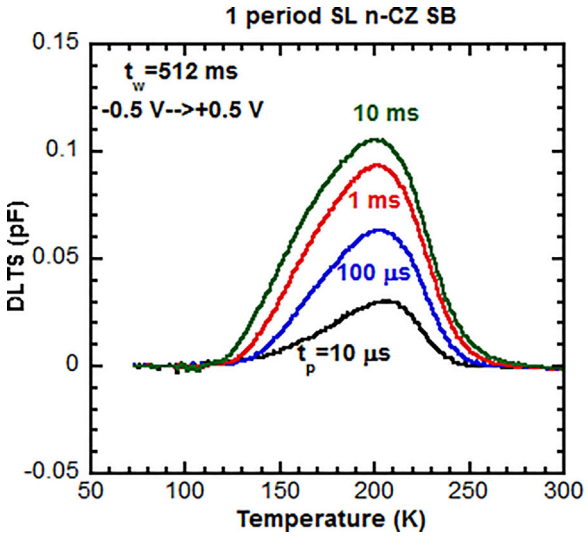

Figure 8. DLT-spectra corresponding with a Cr SB on n-type CZ Si, containing one Si-O layer. The spectra correspond with a $t_w = 512$ ms, a bias from −0.5 V to +0.5 V and different pulse durations.

maximum, however, remains at the same position. This is in good agreement with what has been found for extended defects, corresponding with a distribution of localized states.[24,25] These local states are thought to correspond with imperfections and local defects in the structure of an extended defect.

Based on this, it is concluded that the observed electron and hole states of Si-O SL layers in n-type CZ silicon are most likely associated with extended crystalline defects, rather than to intrinsic states. The fact that for MBE grown material mobility enhancement has been demonstrated in the past[3,4] supports the growth-related origin of the observed deep levels. Of course, this should be further investigated.

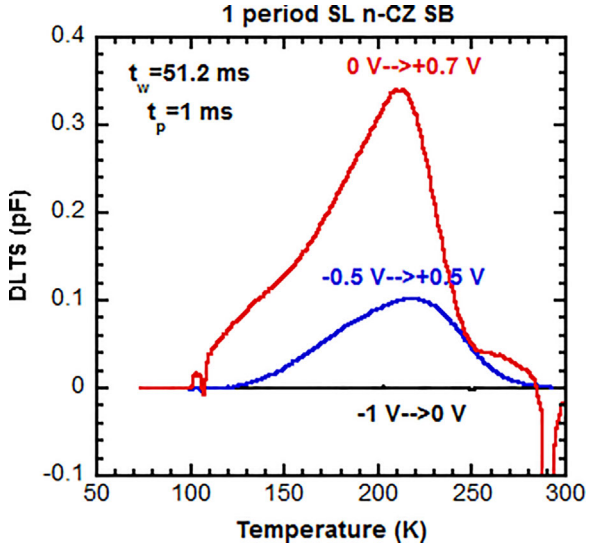

Figure 7. DLT-spectra corresponding with a Cr SB on n-type CZ Si, containing one Si-O layer. The spectra correspond with a $t_w = 51.2$ ms, a $t_p = 1$ ms and different bias pulses.

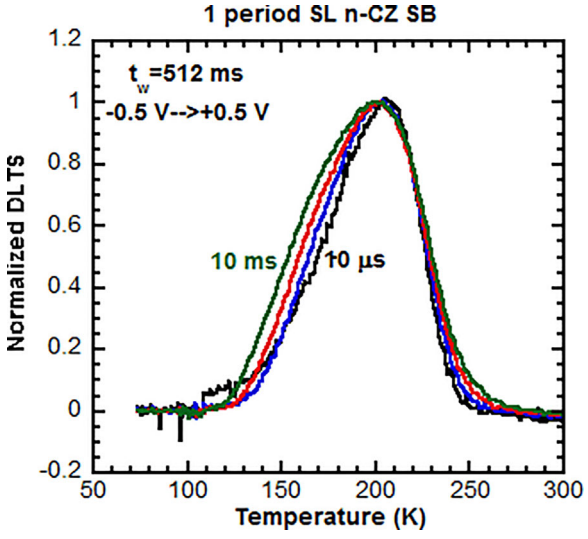

Figure 9. Amplitude normalized spectra, corresponding with **Figure 8**.

5. Conclusions

It has been shown that in Si-O superlattices fabricated on n-type CZ silicon wafers a band of deep electron traps can be found by DLTS. The peak maximum shifts toward the conduction band with increasing number of layers. The trap filling kinetics exhibits logarithmic behavior with pulse duration, similar as for the hole traps in p-type material. Therefore, both bands of states may have a similar type of defect at their origin. From the behavior of the amplitude-normalized peak in n-type material, it is concluded that it behaves like a density of localized states, as can be found for extended defects in silicon.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

dangling bonds, deep-level transient spectroscopy, interface states, silicon, silicon-oxygen superlattice

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