

Optimal design of a driver of interdigital transducers used to generate standing surface acoustic waves for cell sorting

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ABSTRACT

A compact driver based on current feedback amplifiers is designed to drive interdigital transducers (IDTs) that generate standing surface acoustic waves for cell sorting. Compared with commercial RF amplifiers, this driver can be used to drive a wider range of loads without impedance matching. Furthermore, the driver works in a switch mode triggered by target cells, which significantly reduces power consumption in the system. A Butterworth–Van Dyke equivalent circuit was fabricated to study the electrical characteristics of the IDTs, and the driver was designed and optimized by circuit simulations. A cell sorter was constructed and tested experimentally to demonstrate that the driver meets sorting requirements. The driver allows the cell sorter to extract rare cells while otherwise consuming low power.

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I. INTRODUCTION

Fluorescence-activated cell sorting (FACS) has become an efficient method for cell separation because of its sensitivity and accuracy.^{1,2} The present commercial fluorescence-activated cell sorters encapsulate cells in drops in air, and the sorting process is performed by charging target drops and applying biased electric fields. These sorters are capable of very high sorting rates but have intrinsic limitations. Dispersing samples into drops may cause contamination of samples via the air or create biohazardous aerosols, and frequent nozzle clogging and droplet aggregation can lead to poor performance.

Recently, FACS systems using **standing surface acoustic waves (SSAWs)** have been developed.^{3,4} In this approach, the target cells experience an acoustic force produced by a SSAW field and are moved away from their original path toward the collection outlet. The whole process is carried out inside a fluid channel, with no direct contact with the external environment.⁵ Combined with microfluidic technologies, systems can be manufactured at desktop scales, and sample chambers can be disposable with no need for complex cleaning and sterilization.

In previous studies, the sorting process using SSAWs was controlled by switching the output of an RF waveform generator on and off with the power amplifier in continuous wave (CW) mode, meaning the amplifier is working all the time.^{6–8} Because of push-pull architecture,⁹ the amplifier has high power output capacity, but power consumption by the driving system is large and unnecessary, especially for applications that require long processing times such as sorting of rare cells.

In this work, a power operational amplifier (Op-Amp) that uses components of current feedback amplifiers (CFA) was assembled to drive interdigitating transducers (IDTs) with a maximum power of 7 W at their resonant frequency of 38.4 MHz. The power amplifier remains disabled with little power consumption while no target cells are detected, but can apply power within 350 ns in response to a sorting pulse generated upon detection of a target cell, and then switch off again until the arrival of the next target cell. Accordingly, the frequency of the repetitive switching process, which limits the maximum sorting throughput, could be as high as 400 000 events per second. Using this switching mode, our driver offers advantages of power savings for extraction of rare cells. In addition, this driver can be used for a wider range of loads without impedance matching

because the internal resistance of the amplifier is very small compared with the load, and amplification is achieved through feedback with fixed voltage amplitude gain, regardless of load. In the following sections, a Butterworth–Van Dyke (BVD) equivalent circuit was first fabricated to study the electrical characteristics of the IDTs, and the driver was then designed and optimized by circuit simulations. Finally, the driver was integrated into a fluorescence-activated cell sorting system and tested on lymphocytes. The experimental results showed that target cells can successfully be extracted, which validated the performance of our design.

II. THEORIES AND DESIGNS

A. Working mechanism of SSAWs

SSAWs can be generated by a pair of IDTs patterned onto piezoelectric materials.^{10,11} When an AC signal is applied, the IDTs excite the piezoelectric material to generate two counter-propagating waves at the same resonant frequency. A standing acoustic field is established, which forms a periodic spatial distribution of acoustic energy. Objects in this field experience an acoustic force (F_r) that can be expressed as^{12–14}

$$F_r = -\left(\frac{\pi p_0^2 V_p \beta_f}{2\lambda}\right) \phi(\beta, \rho) \sin(2kx) \quad (1)$$

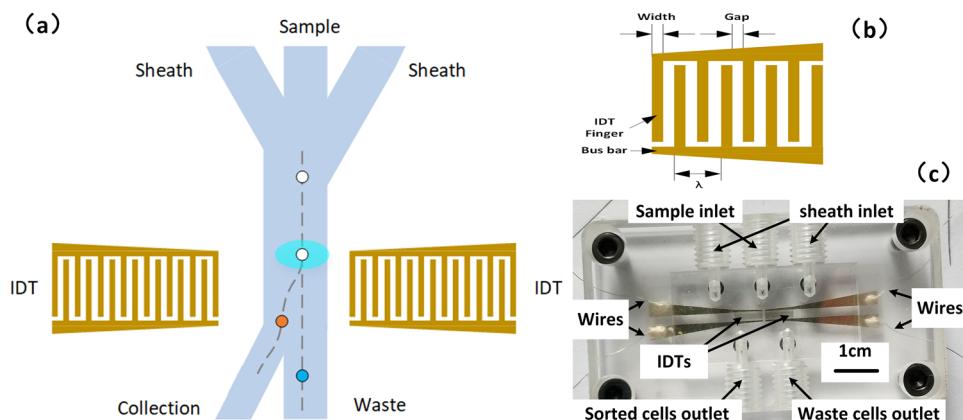


FIG. 1. The cell-sorting device used in the experiments. (a) Schematic diagram of the SSAW-based cell sorter excited by IDTs. The sample is focused by sheath flow, passing through the detection area one by one. If a target cell (red) is detected, the SSAW is switched on and moves the cell to the collection outlet, while others (blue) enter the waste outlet. (b) The comb-like pattern of an IDT. The width of the IDT fingers is equal to the gap between them. As periodicity of the finger pairs defines the wavelength of the resulting SAW, the IDTs should be driven by a corresponding single frequency signal. (c) Photo of our SSAW cell sorter.

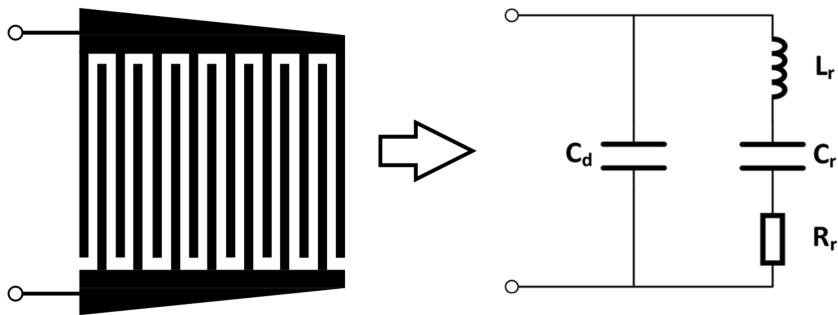


FIG. 2. Butterworth–Van Dyke equivalent circuit.

be $25 \mu\text{m}$, which was $\lambda_{\text{SAW}}/4$ and also the maximum moving distance of the target cells.

B. Butterworth–Van Dyke equivalent circuit

The conventional Butterworth–Van Dyke (BVD) equivalent circuit shown in Fig. 2 provides an adequate description of the electrical behavior of the IDTs and is helpful for designing the driving system, especially for determining the driving frequency and evaluating the load characteristics.^{16–19} In Fig. 2, C_d is the static capacitance of the IDT, and L_r , C_r , and R_r are, respectively, the mass inertia, elastic compliance, and the mechanical loss of the IDT in single mode. The parameters in the BVD equivalent circuit can be calculated from the impedance curve of the IDTs. The impedance curve measured with an impedance analyzer (E4991, Agilent) is shown in Fig. 3, and key parameters are listed in Table I. f_r and Z_r represent resonant frequency and the corresponding impedance, while f_a and Z_a are the anti-resonance frequency and corresponding impedance.¹⁸

Using parameters listed in Table I, C_d , R_r , C_r and L_r of the IDT can be calculated as follows,¹⁷ and the results are listed in Table II:

$$C_d = \sqrt{\frac{(f_A^2 - f_r^2)/Z_A^4 + \sqrt{4f_A^4/(Z_r^2 Z_A^2) + (f_A^2 - f_r^2)^2/Z_A^4}}{8\pi^2 f_A^4}} \quad (2)$$

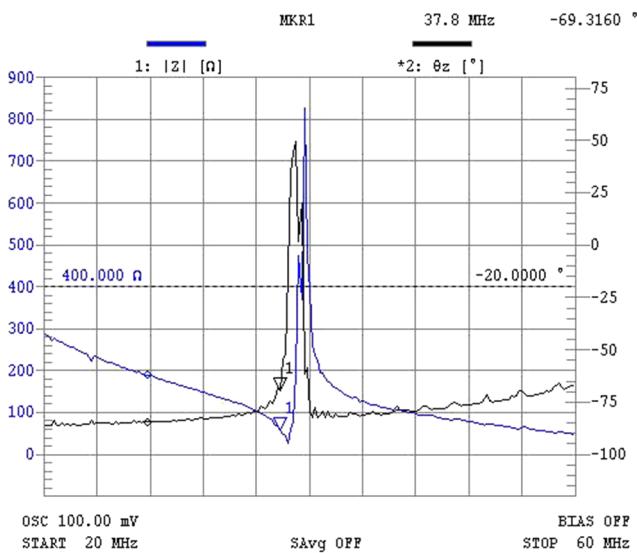


FIG. 3. Impedance of the IDT from 20 MHz to 60 MHz. The blue line represents the impedance ($|Z|$) and the black line is the phase angle (θ).

TABLE I. Resonance and anti-resonance parameters of the IDT.

f_r (MHz)	f_a (MHz)	Z_r (Ω)	Z_a (Ω)
38.4	39.6	26	614.6

TABLE II. Parameters in the BVD equivalent circuit derived from measurements.

C_d (pF)	R_r (Ω)	C_r (pF)	L_r (μH)
31.9	26.53	1.68	10.2

$$R_r = \sqrt{\frac{Z_r^2}{1 - (2\pi C_d f_r Z_r)^2}} \quad (3)$$

$$C_r = C_d \left[\left(\frac{f_A}{f_r} \right)^2 - 1 \right] \quad (4)$$

$$L_r = \frac{1}{4\pi^2 C_r f_r^2}. \quad (5)$$

The BVD equivalent circuit of the IDT was simulated with PSpice software (OrCAD 16.6 Lite, Cadence Design Systems). As shown in Fig. 4, the simulation results agree well with experiment. The parameters of the BVD equivalent circuit are sufficiently accurate to be used in the design of the driving circuit.

C. Design and simulation of the driver

To ensure cell viability during sorting, the driving signal input to IDTs should not be high power (200–1000 mW was sufficient in previous studies).^{8,20} The driving frequency is equal to the resonance frequency of 38.4 MHz, and the impedance of the IDTs at this frequency is $Z = 26 \Omega$. An integrated chip (ADA4870) produced by Analog Devices was chosen based on its bandwidth/slew rate (SR), output voltage and current.²¹ The key features of this component include: large signal bandwidth of 52 MHz (>2V_{p-p}), slew rate of 2500 V/ μs , output current of 1 A, and output voltage amplitude of 37 V_{p-p} with a 40 V power supply. A schematic diagram of the amplifier circuit using the selected components is shown in Fig. 5.

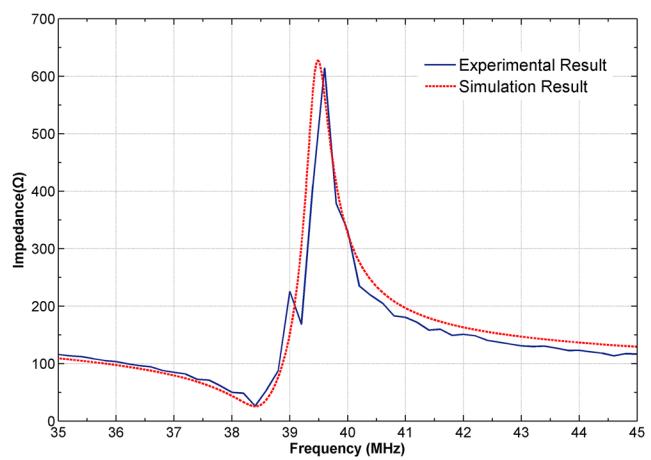


FIG. 4. Comparison of impedance curves from the simulation (red dotted line) and experiment (blue solid line). The two curves are very similar.

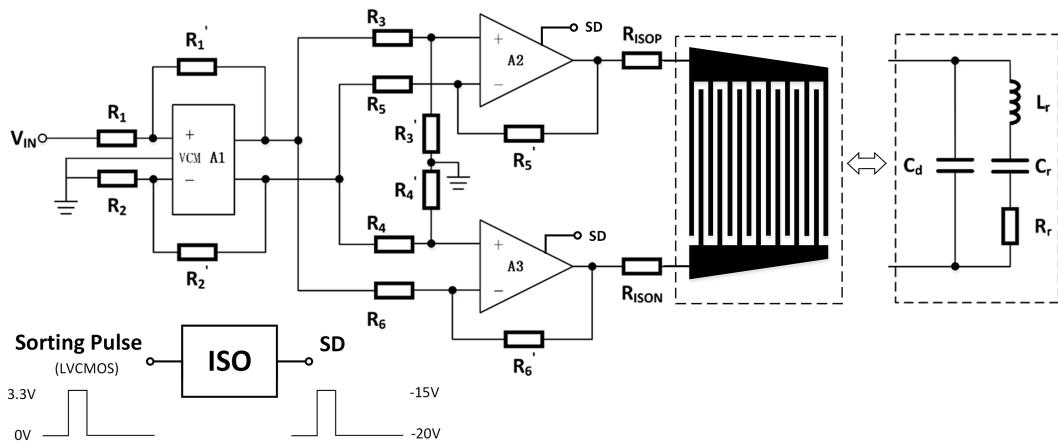


FIG. 5. Schematic of the power amplifier circuit. A1 is an amplifier circuit working as a buffer, changing the single-ended RF signal into differential mode. A2 and A3 are ADA4870s configured in the bridge connection with the IDT. The power amplifiers are switched by the sorting pulse through an isolation circuit.

Although the bandwidth of the amplifier is designed to be 52 MHz, the slew rate (SR) limits the actual output voltage amplitude. To output a sinusoidal signal without distortion at the required frequency, the highest slope of the wave, considered to be the maximum SR of the amplifier, can be expressed as²²

$$SR_{MAX} = \max\left(\frac{dv(t)}{dt}\right) = 2\pi f A_{MAX}. \quad (6)$$

With a typical slew rate of 2500 V/ μ s, the maximum voltage amplitude of the output signal at a frequency of 38.4 MHz is no more than 10.36 V. Therefore, the maximum current consumed (I_{MAX}) is only 0.4 A (10.36 V/26 Ω), which is far below the component's limit. To improve the performance, as shown in Fig. 5, two ADA4870 chips (A2, A3) were combined to drive the IDT in a bridge connection. In this way, the driving system could provide an output voltage of 40 V_{p-p} (± 20 V), which was twice that of a single power Op-Amp. The maximum current dissipation of the IDT can be ± 0.8 A, making the best use of the device. Another amplifier circuit (A1) working as a buffer was set in front of the bridge circuit, changing the single-ended signal into a differential output.

In the schematic diagram, R_1, R_1', R_2, R_2' were set to 1 k Ω to transform a single-ended signal into differential mode. R_5' and R_6' are feedback resistors with values of 1.21 k Ω , as recommended in the data sheet for a stable amplifier gain of 5 V/V. Correspondingly, the gain resistors (R_5, R_6) are configured to be 250 Ω . With parameters derived from the BVD equivalent circuit, the driving voltage and current of the IDTs were simulated using PSpice software to verify the design, as shown in Fig. 6.

The solid trace is the voltage output of the driver while the dotted trace represents the current. Although the BVD mode functions well, a slight phase deviation is still present, indicating a small capacitance, which has a slight effect on the IDT. The resulting power consumption should be calculated accordingly. This circuit design is capable of driving IDTs with an average power of 7 W.

D. Signal switching and response to the sorting pulse

The SSAW is switched on/off for cell sorting: when a cell of interest is detected, the SSAW is switched on to deflect the cell from its original path; otherwise, the SSAW stays off. The response time of the system determines the accuracy of the sorting action and hence the purity of the sorted cells. The response time is mainly determined by four factors: analysis time (t_a), delay time (t_d), recovery time of the driving signal (t_r), and rise time of the acoustic wave (t_b). In this design, we focused mainly on the latter two factors as they are related to the driving system.

With a surface wave velocity in the chosen LiNbO₃ substrate of 3992 m/s,¹⁶ and for a sorting device with an aperture between a pair of IDTs of 500 μ m, the rise time of the SSAW field can be estimated to be $t_b = 125$ ns, which is constant for the system.

The switching method of the driving signal and its period turn out to be the main considerations in our design. Usually there are two ways to switch an amplifier. The typical method is to use a fast MOSFET tube in the input signal chain to control output. However, an extra device has to be introduced into the signal chain that

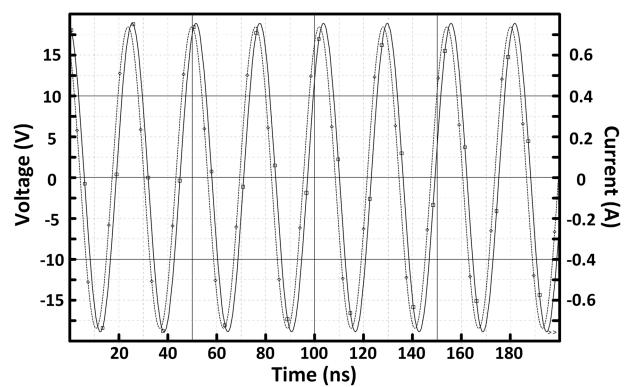


FIG. 6. Simulation results of the driver output. The solid trace represents voltage and the dotted trace represents current.

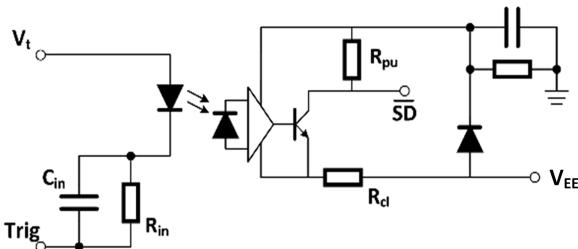


FIG. 7. Schematic of the trigger circuit. A high-speed optocoupler was employed to couple different voltage levels. When a sorting pulse arrives, the optocoupler shuts down quickly and SD pins of the power amplifiers are pulled up to a high voltage ($V_{EE} + 5\text{ V}$).

may cause signal distortion. In addition, the amplifiers keep working even when the input signal is switched off, which consumes energy and generates a lot of heat. Therefore, we adopted another method to switch the amplifiers directly. As mentioned in the device's data sheet, the ADA4870 can be rapidly switched by an external trigger signal. By pulling the shutdown (SD) pin of the device low to V_{EE} , the amplifier switches into a low power shutdown state, reducing the output current to $750\ \mu\text{A}$. When a cell of interest arrives, the SD pin is pulled high ($V_{EE} + 5\text{ V}$) and the amplifier switches back to a working state within 300 ns , which is fast enough for cell sorting. However, the trigger signal in the voltage mode of an LVCMOS transistor (0 to 3.3 V) sent by an FPGA could not be directly applied to the SD pin because the voltage range of the pin is V_{EE} to $V_{EE} + 5\text{ V}$, i.e., -20 to -15 V . An optocoupler can be used in this case, but the device should be designed carefully to ensure a fast response. A high-speed optocoupler (TLP118, Toshiba) was selected for its short propagation delay time of 60 ns and inverter logic type.²³ To achieve a fast response to the trigger signal, the optocoupler was used in an interdiction mode as shown schematically in Fig. 7.

The positive input of the optocoupler was supplied with 3.3 V (V_t), and the trigger signal was connected to the negative pole through a resistor (R_{IN}) in order to limit the input current of the LED to near its threshold. When a cell of interest is detected, the voltage level of the trigger signal goes high with a sharp rising edge, and the current input quickly falls below the lighting threshold of the optocoupler's LED. When the intensity of the optocoupler LED falls, the SD pin of the amplifier is pulled high ($V_{EE} + 5\text{ V}$), converting the amplifier into the working state. In this process, R_{IN} provides an offset to the input that shortens the response time. In addition to R_{IN} , a parallel capacitance (C_{IN}) was employed to balance the input capacitance of the optocoupler, reducing the delay in the response to the trigger signal. There is no need to consider the driving capacity of the trigger signal because of the interdiction mode of the optocoupler. As the central flow speed is designed to be 0.6 m/s , and the aperture of the IDTs is $500\ \mu\text{m}$, the switching process can be completed within $830\ \mu\text{s}$, which is sufficient for recovery of the driving system.

III. CHARACTERIZATION OF THE DRIVING SYSTEM

The printed circuit board (PCB) of the driver is shown in Fig. 8. The power Op-Amps are located on the lower side of the board, the trigger module is at the upper-left corner, and the power module is

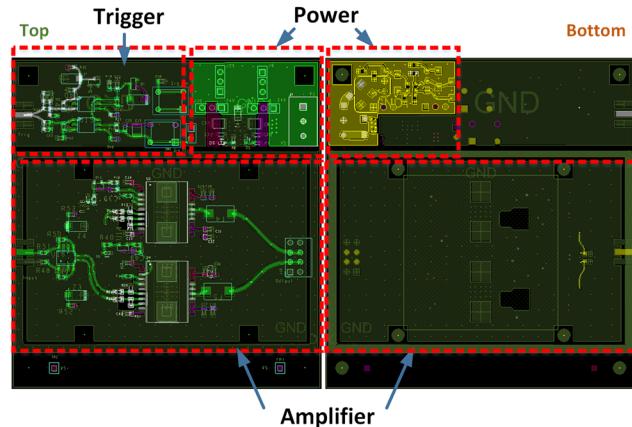


FIG. 8. PCB layout of the driver for the IDTs ($7.5 \times 6\text{ cm}^2$). A $4 \times 4\text{ cm}^2$ exposed copper ground plane is placed beneath the ADA4870s, and a passive heatsink is used for heat dissipation.

at the upper-right. A guard ring with via walls was used to reduce edge-fired emissions. The spaces between the via walls were set to be less than 5 mm , in accordance with the derivation of Armstrong *et al.*²⁴ An exposed copper ground plane ($4 \times 4\text{ cm}^2$) was placed on the bottom side of the board just beneath the ADA4870s. The thermal paddle of the power amplifiers was connected to this copper plane by the via arrays. A passive GPU heatsink was used to increase heat dissipation. The total cost of our device is currently no more than \$50.

A. Characterization of driver capabilities

A function generator (DG4202, Rigol) was employed to apply RF signals to the driver at 38.4 MHz with the desired voltage amplitudes. The outputs of the driver under load ($1\text{ M}\Omega$) were measured by a digital oscilloscope (MSO7034A, Agilent Technologies). The performance of the driver is shown in Fig. 9.

Figure 9(a) shows the measured relationship between SR and output amplitude of the system, where the black line is the output signal from the positive port and the gray line is the SR curve. The experimental results show that the maximum SR of the driver is $2443\text{ V}/\mu\text{s}$ when the output amplitude is 10.63 V , which is consistent with theoretical calculations and validates the output capability of the driver. Figure 9(b) shows measurements of the driver outputs with a load on the IDTs, where the black lines represent signals from the two ports of the output and the gray line is the difference of the two signals. Figure 9(c) is the fast Fourier transform (FFT, calculated with a Hanning window) of the signal input to the driver at a frequency of 38.4 MHz . Figure 9(d) is the FFT of the output signal of the driver with a load on the IDTs. The results of (c) and (d) indicate that the driver has good gain linearity, and the total harmonic distortion (THD) of the system is acceptable. These characteristics will be helpful in controlling the position of the SSAW PNs to achieve reliable cell sorting.

B. Response to the sorting pulse

To simulate the sorting process, a pulse signal generated by the function generator was applied to the trigger port of the driver with a

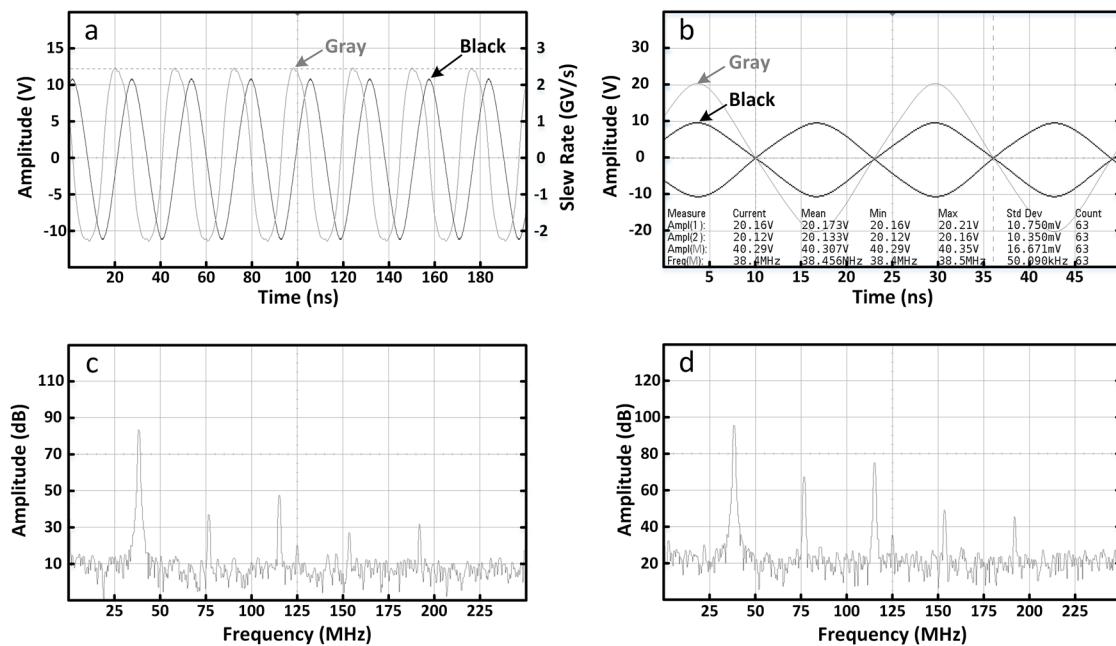


FIG. 9. Performance of the driver. (a) Measured relationship between SR and output amplitude of the system, where the black line is the output signal from the positive port and the gray line is the SR curve. (b) Measurements of the driver outputs with a load on the IDTs, where the black lines represent outputs of the driver and the gray line is the difference between the two signals. (c) Fast Fourier transform (FFT, calculated with a Hanning window) of the input signal to the driver at a frequency of 38.4 MHz. (d) FFT of the output signal of the driver with a load on the IDTs.

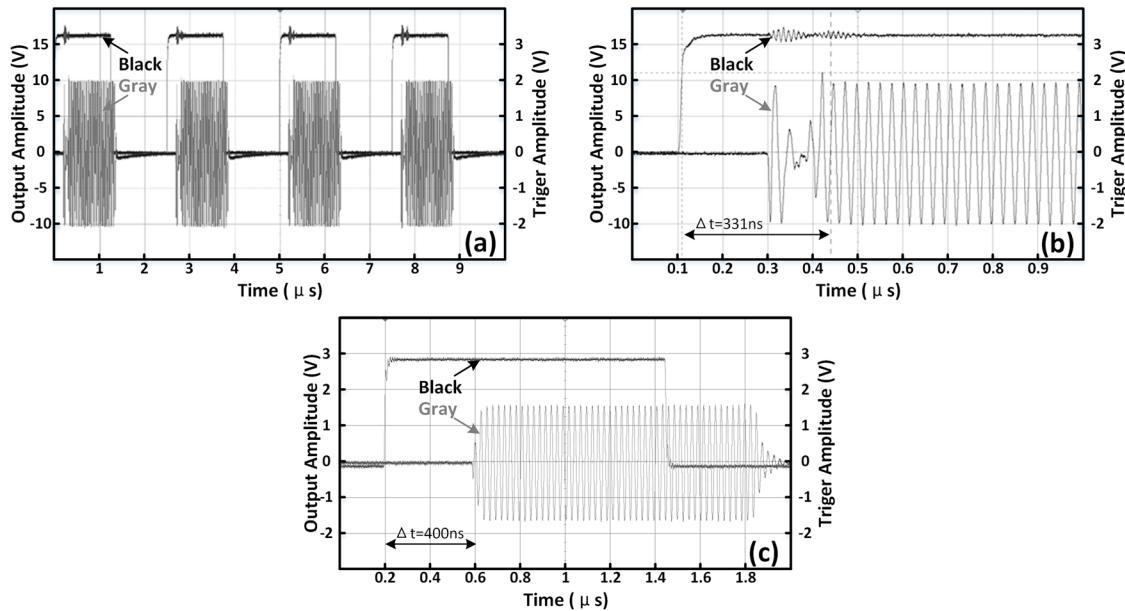


FIG. 10. Recovery of the driver in response to the trigger signal. (a) A pulse wave signal (black curve) generated by the function generator was applied to the trigger port of the driver with a frequency of 400 kHz, high-level voltage of 3.3 V, duty cycle of 50%, and rise time of 5 ns. The output of the driver (gray curve) is also shown. (b) Enlarged view of the beginning of a trigger-response cycle. The delay between the two signals was 331 ns. (c) The delay between the trigger pulse input (black curve) and the RF signal output (gray curve) of the waveform generator was 400 ns.

frequency of 400 kHz, high-level voltage of 3.3 V, duty cycle of 50%, and rise time of 5 ns. Figure 10 shows the recovery of the driver in response to the trigger signal. Figure 10(b) is an enlarged view of (a) at the beginning of a trigger-response cycle. The black curve is the trigger signal and the gray curve is the single-ended output of the driver. The test result shows that recovery can be complete within 330 ns. If the delay in the optocoupler caused by the oscilloscope probe capacitance is taken into account, recovery may be even faster.

We also compared the delay of our RF waveform generator to those reported in previous studies. Because the power amplifier adopted in previous methods operates in CW mode and can be regarded as delay-free, the delay between the trigger input and the RF signal output can be considered to be the response time of the driving system. A trigger signal with the same rising time of 5 ns was input to the pulse modulation port of the waveform generator, and an oscilloscope (DS1102U, Rigol) was used to measure the delay. As shown in Fig. 10(c), the delay was 400 ns, which is similar to that in

our system. Compared with the sorting process that lasts for hundreds of microseconds, the delay in the driving system is negligible. In conclusion, our driving system responds rapidly to the trigger signal of the cell sorter.

C. Sorting performance

A sorting system was assembled to assess the performance of our drivers. As can be seen in Fig. 11(a), the sorting device was mounted on the mechanical stage of an inverted microscope (DSZ2000, UOP, China). A pair of IDTs was connected to the driver described here, and a waveform generator sent identical RF signals to each driver. A beam-shaped 488 nm laser (LuxX 488-100, Omicron) was used to excite fluorescent labels on the cells. The fluorescence was collected by a 20× objective lens (Olympus), separated from the excitation and transmitted light by filters (Edmund), and detected by photomultiplier tubes (H10720-20, Hamamatsu). A custom main board was developed to analyze the fluorescence signals and trigger

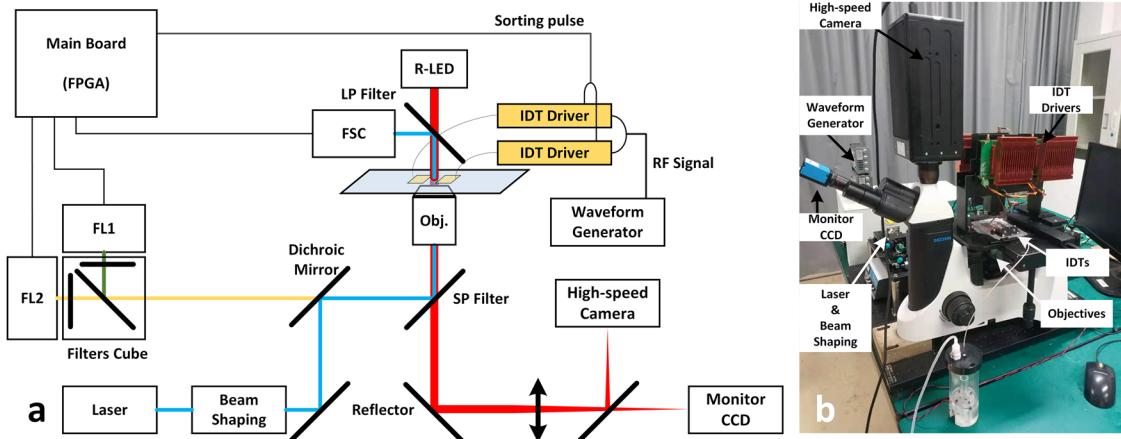


FIG. 11. Setup of the sorting system. (a) Schematic diagram of the sorter. The sorting device was mounted on the mechanical stage of an inverted microscope. Each pair of IDTs was connected to the driver described here and a waveform generator was used as an RF signal source. (b) A photograph of the prototype sorting system.

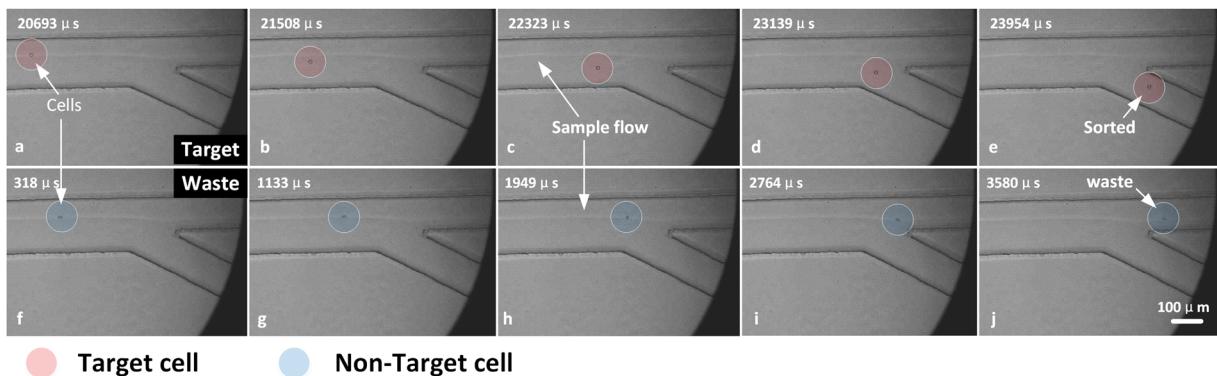


FIG. 12. Individual frames from a high-speed camera video (flow direction is from left to right). (a)–(e) When a fluorescently labeled lymphocyte cell was detected, the drivers were switched on. The target cell (red circle) was deflected by the SAW into the collection outlet. (f)–(j) When there was no target cell, the drivers remained switched off. All of the non-target cells (blue circle) were hydrodynamically guided into the waste outlet. Scale bar is 100 μm .

a sorting pulse when a target cell was detected. We used a red LED to illuminate the entire sorting area and recorded the movements of cells with a high-speed camera (5F01M, Revealer, China).

The capabilities of our drivers were examined using fluorescence-activated cell sorting. Fluorescently labeled lymphocytes were chosen as the target cells and mixed with unlabeled cells. As shown in Fig. 12, unlabeled cells (blue circle) were hydrodynamically guided into the upper waste outlet. When a target cell was detected, a sorting pulse triggered the IDT driver to switch into the working state in which the output power amplifier sent an RF signal to the IDTs, which then acted on the LiNbO₃ to generate an SSAW for sorting. The target cell (red circle) was deflected into the collection outlet by the acoustic field. The acoustic field only works in a small region and disappears instantaneously when the pulse signal is removed, so only the target cell is deflected.

With an actuation time of 500 μ s (controlled by the aperture of the IDT), an input power of 437.5 mW (26.4 dBm) from each driver is sufficient for operation of our sorting system. Higher driving power is helpful for providing stronger acoustic force and reducing the actuation time required. Our power Op-Amp can provide power up to 7 W to achieve a higher sorting rate.

IV. DISCUSSION AND CONCLUSIONS

In this paper, we present a bridge-connected power amplified driver of IDTs to generate SSAsWs for cell sorting. Instead of switching the output of RF waveform generator on/off to control the SSAsWs, we designed a quick switched power Op-Amp using CFAs. Compared with previous methods, shutting down the power amplifiers when no target is detected significantly reduces power consumption in the system, especially when sorting a low proportion of cells, such as in rare cell enrichment. Moreover, this driver can be used to drive a wider range of loads without impedance matching.

Taking advantage of the feedback loop, our driver worked as an Op-Amp: the amplitude of its output was consistent with the input at a certain rate, with little dependence on load. This could free users from having to consider batch-to-batch variation in IDT fabrication. However, it is important to be aware of the inverse proportional relationship between the driving frequency and the output amplitude, which is determined by the amplifier slew rate as discussed in Sec. II C.

In addition, for a given output voltage amplitude, driving in differential mode can produce four times as much power as that of single-ended mode. The position of a PN can be adjusted by changing the phase difference between outputs of the two drivers. The outstanding output capabilities and rapid response to the sorting pulse trigger were demonstrated through numerical simulations and experiments. Our device achieved a maximum output voltage amplitude of 40 V_{p-p} with output power calculated as 7 W at the frequency of 38.4 MHz. The recovery time of the driver in response to the sorting pulse was 331 ns, and the switching frequency can be higher than 400 kHz, which allows sorting at up to 400 000 events per second. Because of the low cost and small volume of our driver, parallel operation of them can further reduce the internal impedance, thus providing more power to the sorting device.

Generally, our device provides an effective, high switching-rate, low-power-consumption, low-cost, small-size driving system for integrated, high-performance, on-chip SSAW-actuated FACS.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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