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Thermal resistance optimization of GaN-on-Si materials for RF HEMTs based on structure function method and static-pulsed I–V measurements

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ABSTRACT

A major obstacle in the commercialization of GaN-on-Si RF HEMTs lies in the elevated thermal resistance introduced by the AlN/AlGaN multi-layer buffer, employed for stress management. This issue adversely impacts device performance and reliability. In this study, the structure function method was utilized to precisely determine the intrinsic thermal resistance of GaN-on-Si materials. Results reveal that a single-layer AlN buffer demonstrates a significantly enhanced heat dissipation capability compared to conventional AlN/AlGaN multi-layer or superlattice buffer. Additionally, the thermal performance of device under operation was quantitatively assessed using static-pulsed *I–V* measurements. Through theoretical simulations, the influence of GaN buffer structures on heat distribution within GaN-on-Si RF devices was explored, indicating that optimizing GaN buffer thickness can further enhance thermal performance. This research offers a thorough understanding of the relationship between material structures and RF device thermal behavior, providing crucial insights for the thermal management design of GaN-on-Si RF HEMTs.

As a representative of wide-bandgap semiconductor materials, GaN has superior properties, such as large bandgap, high electron mobility, and high electron saturation velocity, making it ideal for high-frequency and high-power RF applications.[1,2] GaN-based high-electron-mobility transistors (HEMTs) grown on SiC substrates have been commercialized for microwave and radio frequency (RF) applications. However, the high cost and limited wafer size of SiC substrates still hamper larger-scale deployment for cost-sensitive applications. Given the larger wafer size, lower cost, and potential integration potential with Si complementary metal–oxide–semiconductor field-effect transistors, high-performance AlGaN/GaN HEMTs grown on Si have progressed to be a powerful contender.[3,4] In practice, a carefully designed AlN/AlGaN multi-layer or superlattice (SL) buffer has been adopted to obtain crack-free high-quality GaN grown on low resistivity ($\rho < 20\,\Omega$ cm) Si substrates,[5,6] promoting the GaN-based HEMTs for power switching applications. For RF applications, high-resistivity Si (HR-Si, $\rho > 5\,\mathrm{k}\,\Omega$ cm) is used to mitigate the RF loss originating from the substrates.[7] There have been many reports on the growth of GaN-on-HR-Si HEMTs,[8] which mainly focus on strain management, dislocation control, and suppression of RF loss due to the parasitic channel at the AlN/HR-Si interface. As a matter of fact, another key limiting factor for high-frequency GaN HEMTs performance and reliability is

the operating junction temperature, which is in turn determined primarily by the thermal resistance of the overall structure. Recently, learning from the GaN-on-SiC epitaxial structure, a new way of stress control by using a single-layer AlN buffer has been developed for GaN-on-HR-Si epitaxial growth (see our previous work[9]) for RF device applications. It is expected to reduce thermal resistance, owing to the effective suppression of phonon-alloy and phonon-boundary scattering, compared with the conventional AlN/AlGaN multi-layer buffer.[10,11] To evaluate device thermal resistance, methods such as infrared thermography, double-pulsed electrical techniques, and micro-Raman thermometry are commonly used. Infrared thermography provides non-contact, high-resolution 2D temperature mapping but is limited by low emissivity and optical transparency.[12] Double-pulsed electrical methods offer a simple and accurate way to estimate channel temperature by comparing device behavior under DC and pulsed conditions.[13] Meanwhile, micro-Raman thermometry has been widely adopted for decades, offering sub-micrometer spatial resolution (0.5–0.7 μm), along with high temporal resolution (200 ns). It has been successfully applied in GaAs p-HEMTs and AlGaN/GaN HEMTs.[14–16]

In this work, the structure function method, in which heat conduction was constrained to one-dimensional pillar structures, was first applied for an accurate characterization of thermal resistance of various GaN-on-HR-Si buffers. Combined with static-pulsed I–V measurements based on a simple two-terminal (source–drain) test structure, the impact of GaN buffer structure on the working device was also revealed.

Figure 1 shows the epitaxial structures of various buffer types grown on high-resistivity Si(111) substrates using metalorganic chemical vapor deposition (MOCVD). A 300-nm-thick AlN nucleation layer was grown directly on Si(111) substrate, followed by the deposition of a 1-μm-thick GaN buffer layer (sample A). Sample B consisted of a 300-nm-thick AlN layer, a 300-nm-thick $Al_{0.18}Ga_{0.82}N$ layer, a 500-nm-thick $Al_{0.18}Ga_{0.82}N$/GaN SL with 35 periods (3/11.5 nm), and a 1-μm-thick GaN buffer layer. Sample C replaced the SL layers with Al-composition step-graded AlGaN layers, including approximately a 270-nm-thick $Al_{0.23}Ga_{0.77}N$ layer and a 300-nm-thick $Al_{0.17}Ga_{0.83}N$ layer. Considering that different transitional layers have distinct interface thermal resistance, our motivation is to quantitatively compare the thermal resistance from the material perspective, which comprises both the material properties and the interface.

Based on the well-known Cauer model, the structure function curve of the measured system (chip sensor, device, solder, and case) corresponds to an equivalent RC thermal network.[17] This allows the thermal resistance of the device to be identified and extracted through structure function analysis. This approach was employed in our study to quantitatively analyze the thermal characteristics of the buffer layers. A chip with the heat source separated from the temperature sensor was designed to obtain transient temperature response curves, which were processed using the structure function method.[18] The temperature measurement chip consisted of a heat source layer with metal wires, a SiO_2 isolation layer, a temperature sensor with Schottky diodes in a series connection, and a SiC substrate, as illustrated in Fig. 2(a). The chip area was approximately $1 \times 1\,mm^2$. During the measurement, the electrical signals can be converted into temperature signals owing to a linear relationship between the forward junction voltage drop of the Schottky diode at a constant current and the temperature rise. In this way, temperature variation can be recorded.[19] Figure 2(b) shows the measurement sequence, where constant heating power was applied, and the transient temperature response curves were obtained by collecting voltage change in the temperature sensor. In this method, the thermal resistance (R_{th}) of material can be used by Fourier's Law governing heat conduction

$$R_{th} = \frac{d}{\kappa \times S_{Heat\_flux}} = \frac{R_{value}}{S_{Heat\_flux}}, \quad (1)$$

where d is the thickness (m) of the material (measured on the path parallel to the heat flow), κ is the thermal conductivity [W/(K m)] of the material, S_{Heat_flux} is the cross-sectional area (m^2) perpendicular to the path of heat flow, and R_{value} (K m^2/W) is called thermal resistance for a unit area which describes an intrinsic thermal characteristic for material with a certain thickness.[20] According to Eq. (1), to make the extraction of R_{th_buffer} more reliable, magnifying its proportion accompanied by a reduction in heat capacity (proportional to the weight of the material) contained in the entire structure function curve is highly required. It should be mentioned that R_{th_buffer} includes the thermal resistance originating from the GaN buffer and underlying transitional layers (a single-layer AlN buffer, a AlGaN/GaN SL buffer, or a step-graded Al-composition AlGaN buffer). Thus, the GaN-on-Si sample was etched to form a pillar array of uniformly distributed square elements, reaching a depth of approximately 100 nm below the interface of AlN/Si substrate, as shown in Figs. 2(c) and 2(d). It is noteworthy that the pillar structure with small size helps constrain the heat conduction along one dimension. In addition, to verify the reliability of the measurement by R_{value}, which is theoretically independent of S_{Heat_flux}, two arrays with different geometric sizes were fabricated. Table I summarizes their structural parameters: S_{single} denotes the area of a single pillar, while N_{Array} and S_{Heat_flux} represent the pillar number

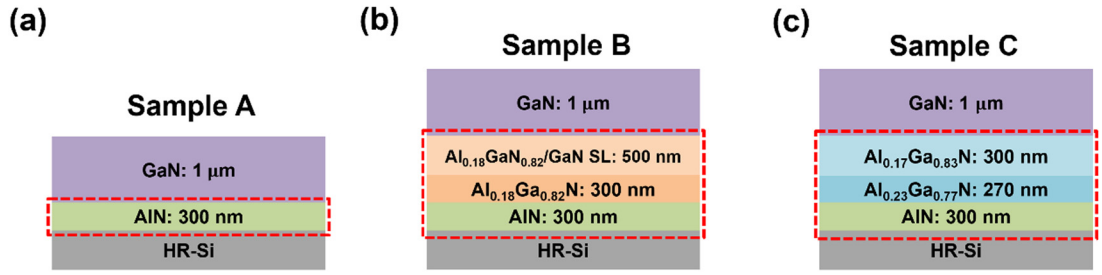

FIG. 1. Schematic illustration of the epitaxial structures. (a) Sample A with a single-layer AlN buffer; (b) sample B with a AlGaN/GaN SL buffer; and (c) sample C with a step-graded Al-composition AlGaN buffer.

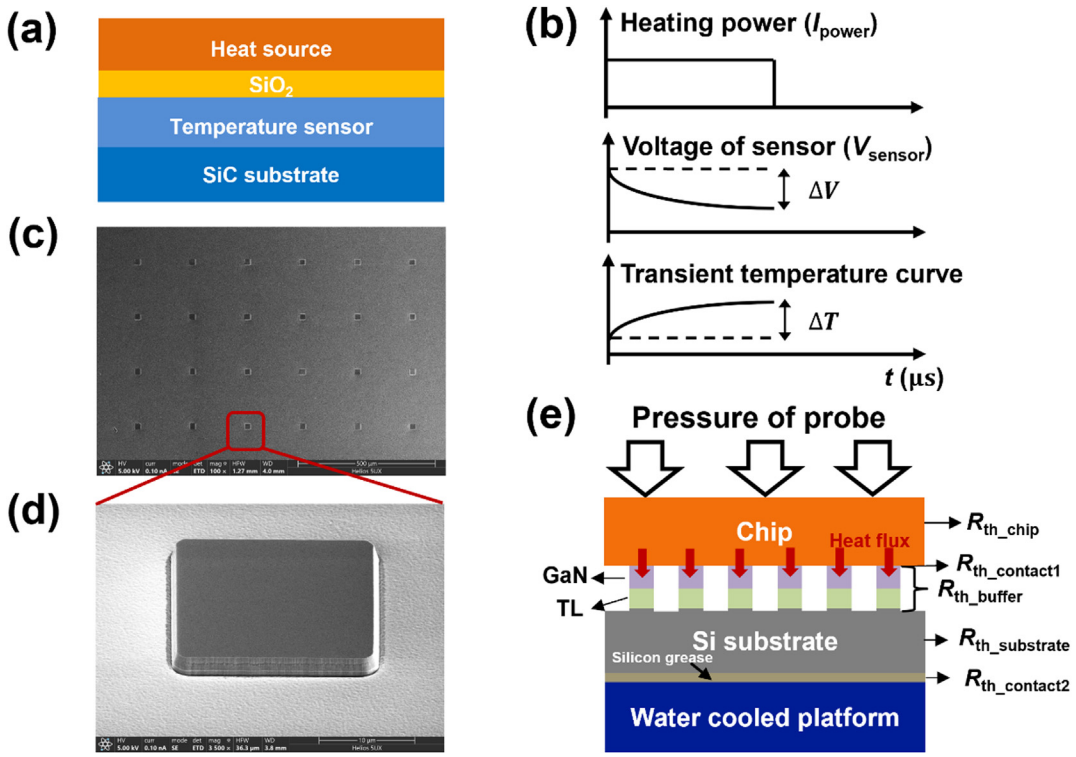

FIG. 2. (a) Schematic illustration of the temperature measurement chip. The heat source with metal wires and temperature sensor unit were grown on SiC substrate. (b) The measurement sequence. (c) and (d) SEM images of the surface topography of sample C ($S_{single} = 20 \times 20\ \mu m^2$). (e) Schematic illustration of the measurement system.

within the array and the effective contact area between the chip and the GaN-on-Si sample, respectively.

The whole measurement system, as presented in Fig. 2(e), shows that the chip was directly in contact with the as-fabricated arrays. The chip was connected with the external measurement circuit through eight probes. These probes provide sufficient pressure to reduce the contact thermal resistance between the chip and arrays. Basically, the total thermal resistance of the measurement system can be expressed as

$$R_{th\_total} = R_{th\_chip} + R_{th\_contact1} + R_{th\_buffer} + R_{th\_substrate} + R_{th\_contact2}, \quad (2)$$

where R_{th_chip} and $R_{th\_substrate}$ are, respectively, the thermal resistance of the chip and Si substrate of the GaN-on-Si sample, R_{th_buffer} is the entire thermal resistance of the columnar section, $R_{th\_contact1}$ is the contact thermal resistance between the chip and the sample, and $R_{th\_contact2}$ is the contact thermal resistance between the sample and the water-cooled platform as illustrated in Fig. 2(e). $R_{th\_contact1}$ was chosen as a controllable parameter during the measurement and was tuned by applying varied probe pressures on the chip. In this way, the thermal characteristics of the chip itself can be distinguished from that of the measured sample in the structure function curve.

TABLE I. Surface area parameters of the GaN-on-Si pillar arrays after fabrication.

	S_{single} (μm^2)	N_{Array}	S_{Heat_flux} (μm^2)
Array I	20×20	5×5	100×100
Array II	40×40	5×5	200×200

Figure 3(a) shows the transient thermal resistance (Z_{th}) curves of sample B, measured under varying probe pressures adjusted by the stroke depths of the probes. In the experiment, the downward stroke of the probe in contact with the chip electrode was 20 and 30 μm. The two curves overlapped closely until 10 ms but diverged significantly thereafter under higher probe pressures, indicating a reduction in $R_{th\_contact1}$. Therefore, the total thermal resistance at the steady state decreased from 21.30 to 20.75 K/W.

To establish a clear correspondence between transient thermal resistance curves and the actual measurement structure, cumulative structure curves were derived using the structure function method, as shown in Fig. 3(b). Part I of the curves overlapped completely, while part II showed an offset of approximately 0.55 K/W due to increased probe pressure. Based on the transient dual interface test method (TDIM) principle, this difference reflects the variation in the contact thermal resistance between the chip and the sample. Therefore, part I corresponds to R_{th_chip} and $R_{th\_contact1}$. According to the theory of the structure function method, the x-axis and y-axis in the cumulative structure curve represent the cumulative value of the thermal resistance and heat capacity along the direction of heat flux, respectively. For one-dimensional heat flux, the significant variation in heat capacity with the accumulation of thermal resistance is generally considered

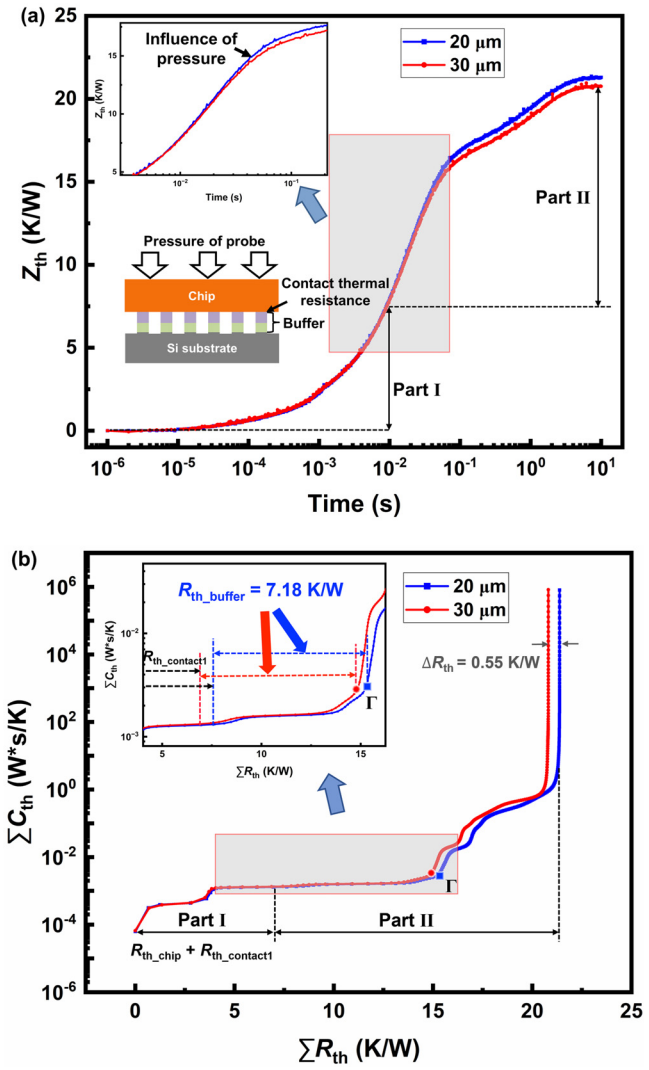

FIG. 3. (a) Transient thermal resistance curves of sample B (array I) with probe strokes of 20 (blue) and 30 μm (red), obtained by normalizing transient temperature response curves using the power of the heat source. The inset illustrates the impact of probe strokes depth on the curves beyond 10 ms. (b) Cumulative structure curves obtained from the transient thermal resistance curves using the structure function method. The inset reveals a reduction in $R_{th\_contact1}$ with increasing pressure, and a distinct separation of R_{th_buffer} in the cumulative curves.

to be heat flux conduction in the bulk material, whereas the negligible variation can be related to heat conduction at interface. Thus, $R_{th\_contact1}$ appears as a platform in the cumulative structure curve, where thermal resistance increases while heat capacity remains nearly constant. As the GaN-on-Si sample pillars lead to an increased proportion of R_{th_buffer} to R_{th_total} as well as a decrease in heat capacity, R_{th_buffer} exhibits a plateau characteristic similar to $R_{th\_contact1}$, but with a slight increase in heat capacity. A consequent plateau with a clear transition point Γ corresponding to R_{th_buffer} can be observed. As a result, R_{th_buffer} of sample B can be extracted to be 7.18 K/W shown in the inset of Fig. 3(b).

Measurements of the other two samples were performed under the same conditions. Using Eq. (1), R_{value_buffer} was calculated for the three samples. As shown in Table II, R_{value_buffer} values derived from different areas (array I and array II) are consistent, confirming the reliability of the measurement results. Sample A, equipped with a single-layer AlN buffer, exhibits superior heat dissipation in one-dimensional heat conduction compared to samples B and C, which is consistent with the reported work.[21] This is expected to improve the heat dissipation capacity and GaN RF device performance. Theoretically speaking, there is still room for improvement through optimizing the growth conditions of the AlN layer and the interface structure.[22] In addition, although the AlGaN/GaN SL in sample B introduces more interfaces, which might degrade thermal performance, it shows a lower thermal resistance than sample C. This is attributed to the thinner AlGaN thickness in SL ($35 \times 3 = 105$ nm) compared to sample C.

Moreover, the influence of GaN buffer thickness on the thermal performance of the operating device was systematically studied. Two-terminal test structures with varying source–drain spacings (d) were fabricated. These structures excluded the gate and utilized regrown highly n-doped GaN Ohmic contacts.[23] This design ensured that nearly all heat generation originated from the channel, thereby simplifying the heat dissipation process. As illustrated in Fig. 4(a), GaN buffer layers with various thicknesses ($t_{GaN} = 0.8$, 1.0, 1.3, and 1.8 μm) were grown on a 300-nm-thick AlN layer. All samples featured the same AlGaN/GaN heterostructure and a similar dislocation density of 3.0×10^9 cm^{-2}.

A static-pulsed I–V measurement technique, as described in Ref. 24, was employed across various temperatures to quantitatively evaluate the thermal dissipation capacity of GaN buffer layers and precisely extract their thermal resistance (R_{th}). The black curve in Fig. 4(b) represents the static measurement for the Device Under Test (DUT), where sufficient heating (pulse width = 100 μs) induced significantly self-heating and reached a steady junction temperature ($T_{junction}$). For the other curves, the device was first heated to reach various baseplate temperatures ($T_{ambient}$, from 50 to 150 °C). Subsequently, I–V data were quickly acquired using a short pulse (pulse width = 300 ns, duty cycle = 0.01%) to minimize self-heating, resulting in isothermal I–V curves. Both static and pulsed measurements used the same quiescent bias ($V_Q = 0$ V). The intersection points of the static curve (black) and the other pulse curves measured at various temperatures determined the dissipation power ($P_{diss} = V \cdot I$), which corresponds to the $T_{junction}$ obtained from the isothermal I–V curve in Fig. 4(b). The definition of device thermal resistance is

$$R_{th} = \frac{T_{junction} - T_{ambient}}{P_{diss}}, \tag{3}$$

where $T_{junction}$ is the junction temperature (K), $T_{ambient}$ is the ambient temperature (K), and P_{diss} is the dissipation power (W). This definition establishes a linear relationship between $T_{junction}$ and P_{diss}, enabling the

TABLE II. R_{value_buffer} ($\times 10^{-8}$ m^2 K/W) extracted from the cumulative curves.

	R_{v_buffer} (sample A)	R_{v_buffer} (sample B)	R_{v_buffer} (sample C)
Array I	5.83	7.18	9.36
Array II	6.16	7.20	9.28

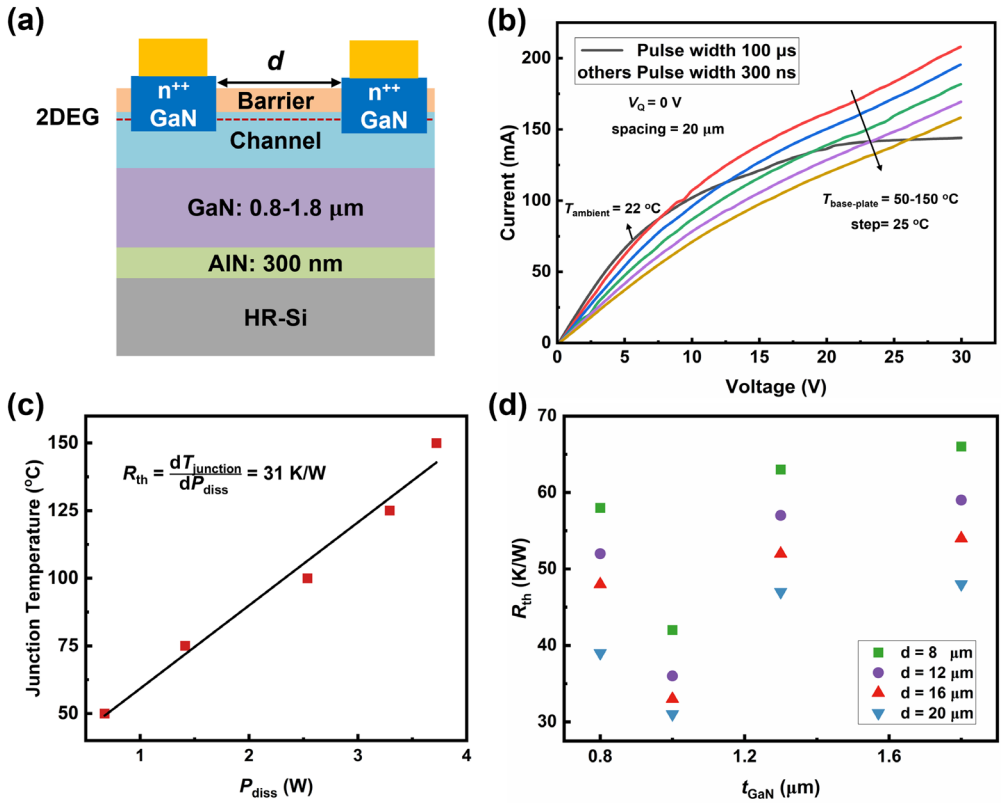

FIG. 4. (a) Cross-sectional schematic view of the fabricated two-terminal test structure, featuring a GaN buffer layer and a single-layer AlN layer. (b) Self-heating pulsed *I–V* (pulse width = 100 μ s) at ambient temperature and pulsed *I–V* (pulse width = 300 ns) at various baseplate temperatures (50–150 °C, step = 25 °C) of DUT ($t_{GaN} = 1\ \mu$m, $d = 20\ \mu$m). (c) The junction temperature of the device as a function of dissipation power, the slope of the data represents the thermal resistance of the device. (d) Thermal resistance distribution with various spacings of DUTs.

extraction of R_{th} as the slope of the fitted line, as described in Fig. 4(c). Figure 4(d) shows that R_{th} decreases with increasing d, suggesting that a larger heat source area facilitates heat dissipation. Notably, the DUT with a 1-μm-thick GaN buffer layer exhibits the lowest R_{th}. This observation deviates from the expected one-dimensional heat dissipation scenario, where a thicker GaN buffer is supposed to result in a larger R_{th}. This device-level observation suggests that both vertical and lateral heat dissipation, influenced by the GaN buffer thickness, must be considered.

Hence, three-dimensional thermal simulation based on a Finite Element Method (FEM) model was performed to study the integrated effects of GaN buffer layer thickness and heat source dimension on device thermal performance.[25] The schematics of the simulated device structure are shown in the inset of Fig. 5(a), designed to replicate the measured two-terminal test structure. Thermally insignificant components, such as source and drain contacts, were excluded for simplicity.[26] The device features a thickness varying GaN layer on a 100-μm-thick Si substrate, with fixed mesa sizes ($L_M = 20\ \mu$m, $W_M = 500\ \mu$m). The substrate was ideally heatsinked at 300 K. To ensure a fair comparison, a constant heat flux of 1 W was supplied through the heat source. Additionally, the thermal boundary resistance (TBR) between the GaN layer and the Si substrate was set to 40 m^2 K/GW, accounted for the AlN layer as part of the interface resistance.[22]

Figure 5(a) depicts the R_{th} of the device, determined by monitoring the junction temperature at the center of the heat source according to Eq. (3). Interestingly, the dependence of R_{th} on GaN buffer layer thickness exhibits distinct trends as the heat source length (L_{HEAT}) varies. In the case of $L_{HEAT} = L_M = 20\ \mu$m, a thinner GaN layer helps reduce R_{th}, resembling a one-dimensional heat conduction scenario where lateral heat dispersion is virtually absent. With limited lateral heat diffusion, heat generated in the channel primarily flows vertically through the GaN layer, which leads higher thermal resistance as the GaN layer thickness increases. However, for smaller heat source dimension, localized heat generation introduces additional complexity, as the two-dimensional spread angle must be considered. An appropriately thick GaN buffer achieves the lowest junction temperature for the structure with a certain L_{HEAT} as shown in Fig. 5(a). Alternatively, shrinking the GaN layer thickness beyond a certain value could lead to a significant increase in thermal resistance. The underlying mechanism stems from the effective cross-sectional area S_{Heat_flux} of the thermal path between the heat source and the heat sink, which has an intimate relation with GaN layer thickness. Figure 5(b) shows the transverse temperature distribution at the GaN/Si interface for different GaN layer thicknesses, allowing qualitatively estimation of S_{Heat_flux}. For thin GaN layer (0.1–0.5 μm), the concentrated heat flux coming out from the heat source passes through the interface almost without

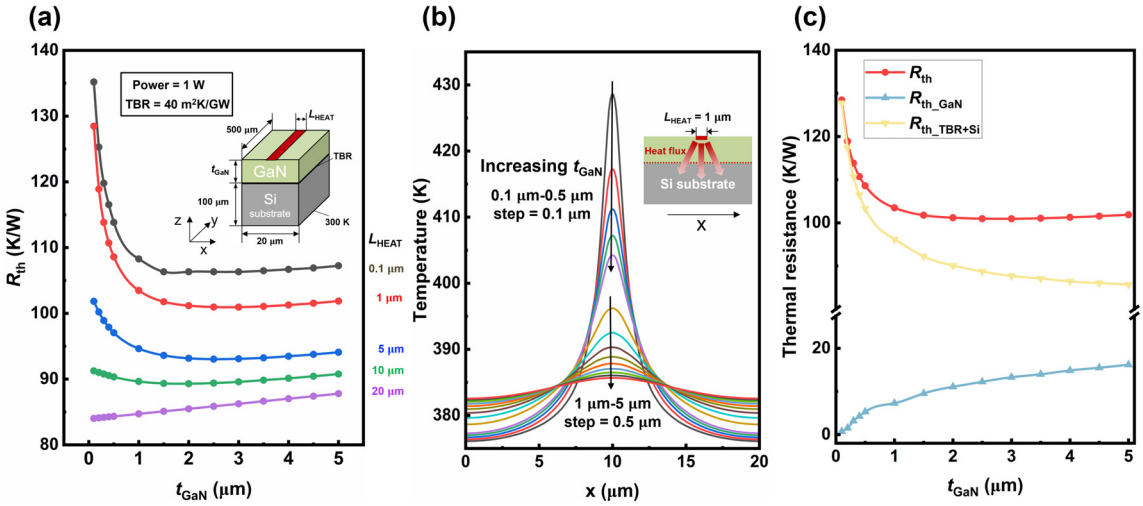

FIG. 5. (a) The effect of GaN buffer layer thickness (t_{GaN}) on the thermal resistance of device (R_{th}) for various heat source lengths (L_{HEAT}). (b) Transverse temperature distribution at the GaN/Si interface for various thicknesses of GaN buffer layer. (c) The effect of t_{GaN} on the thermal resistance of the device (R_{th}), the thermal resistance of the GaN layer (R_{th_GaN}), and the interface and Si substrate (R_{th_TBR+Si}) for $L_{HEAT} = 1\ \mu m$.

spreading, leading to a smaller S_{Heat_flux}. Conversely, thicker GaN layers (1–5 μm) mitigate thermal crowding and broaden S_{Heat_flux}. Figure 5(c) decomposes the overall thermal resistance (R_{th}) into the thermal resistance of the GaN layer (R_{th_GaN}) and the combined thermal resistance of the GaN/Si interface and Si substrate (R_{th_TBR+Si}). As the GaN layer thickens, S_{Heat_flux} increases, effectively reducing R_{th_TBR+Si}. However, an excessively thick GaN adds significant thermal resistance from the layer itself, making substantial contribution to the overall thermal resistance, as shown in Fig. 5(c). The simulation results provide a physical explanation for why the thermal resistance of the DUT, measured by the static-pulsed I–V method, deviates from one-dimensional heat conduction expectations.

In summary, the thermal performance of GaN-on-Si RF HEMTs with various buffers was comprehensively studied at the fundamental material level using the structure function method. A single-layer AlN buffer shows the best heat dissipation capability as expected. Additionally, the static-pulsed I–V measurement was used to precisely extract the thermal resistance of the working device. For devices at the micrometer scale with a 300-nm-thick AlN layer, the optimal heat dissipation performance is achieved with a 1-μm-thick GaN buffer layer. Combined with FEM-based simulations, the impact of GaN buffer thickness on device thermal performance has been clarified. This work provides useful guidance for thermal management design of GaN-on-Si RF HEMTs from the perspective of material stack structure.

See the supplementary material for the structure function method and details of the measurement process.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Qingru Wang: Conceptualization (lead); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Yu Zhou:** Conceptualization (equal); Formal analysis (supporting); Funding acquisition (equal); Investigation (equal); Methodology (equal); Resources (equal); Writing – review & editing (lead). **Xiaozhuang Lu:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal). **Xiaoning Zhan:** Formal analysis (equal); Investigation (equal); Resources (equal). **Quan Dai:** Formal analysis (equal); Funding acquisition (equal). **Jianxun Liu:** Conceptualization (equal); Resources (equal). **Qian Li:** Writing – review & editing (equal). **Xinkun Zhang:** Formal analysis (equal); Software (equal). **Yamin Zhang:** Methodology (equal); Software (equal). **Qian Sun:** Funding acquisition (equal); Resources (lead); Writing – review & editing (equal). **Shiwei Feng:** Resources (equal). **Zhihong Feng:** Funding acquisition (equal). **Meixin Feng:** Funding acquisition (equal). **Xin Chen:** Methodology (equal). **Hui Yang:** Funding acquisition (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

REFERENCES

[1]J. Ajayan, D. Nirmal, P. Mohankumar, B. Mounika, S. Bhattacharya, S. Tayal, and A. S. A. Fletcher, Mater. Sci. Semicond. Process. **151**, 106982 (2022).
[2]K. Harrouche and F. Medjdoub, *Nitride Semiconductor Technology: Power Electronics and Optoelectronic Devices* (Wiley, 2020), Vol. 99.
[3]K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, J. Appl. Phys. **130**(16), 160902 (2021).
[4]L. H. Hsu, Y. Y. Lai, P. T. Tu, C. Langpoklakpam, Y. T. Chang, Y. W. Huang, W. C. Lee, A. J. Tzou, Y. J. Cheng, C. H. Lin, H. C. Kuo, and E. Y. Chang, Micromachines **12**(10), 1159 (2021).
[5]X. Chen, Y. Zhong, S. Yan, X. Guo, H. Gao, X. Sun, H. Wang, F. Li, Y. Zhou, and M. Feng, J. Phys. D. **56**(35), 355101 (2023).
[6]F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere, and M. Kuball, IEEE Electron Device Lett. **41**(12), 1754 (2020).
[7]T. T. Luong, F. Lumbantoruan, Y.-Y. Chen, Y.-T Ho, Y.-C. Weng, Y.-C. Lin, S. Chang, and E-Y. Chang, Phys. Status Solidi A **214**(7), 1600944 (2017).
[8]J. He, W. Cheng, Q. Wang, K. Cheng, H. Yu, and Y. Chai, Adv. Electron. Mater. **7**(4), 2001045 (2021).
[9]X. Zhan, J. Liu, X. Sun, Y. Huang, H. Gao, Y. Zhou, Q. Li, Q. Sun, and H. Yang, J. Phys. D: Appl. Phys. **56**(1), 015104 (2022).
[10]D. Q. Tran, R. Delgado-Carrascon, J. F. Muth, T. Paskova, M. Nawaz, V. Darakchieva, and P. P. Paskov, Appl. Phys. Lett. **117**(25), 252102 (2020).
[11]C. Middleton, S. Dalcanale, J. W. Pomeroy, M. J. Uren, J. Chang, J. Parke, I. Wathuthanthri, K. Nagamatsu, S. Saluru, S. Gupta, R. Howell, and M. Kuball, IEEE Electron Device Lett. **40**(9), 1374 (2019).
[12]S. Kim, D. C. Shoemaker, A. Karim, H. Walwil, M. T. DeJarld, M. B. Tahhan, J. Vaillancourt, E. M. Chumbes, J. R. Laroche, G. Pavlidis, S. Graham, and S. Choi, IEEE Trans. Electron. Devices **72**(1), 162–168 (2025).
[13]S. Martin-Horcajo, A. Wang, M.-F. Romero, M. J. Tadjer, and F. Calle, IEEE Trans. Electron Devices **60**(12), 4105 (2013).
[14]M. Kuball, G. J. Riedel, J. W. Pomeroy, A. Sarua, M. J. Uren, T. Martin, K. P. Hilton, J. O. Maclean, and D. J. Wallis, IEEE Electron Device Lett. **28**(2), 86–89 (2007).
[15]S. Choi, E. R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans Electron Devices **60**(6), 1898–1904 (2013).
[16]A. Sarua, A. Bullen, M. Haynes, and M. Kuball, IEEE Trans Electron Devices **54**(8), 1838–1842 (2007).
[17]V. Székely, Microelectron. Reliab. **42**(4–5), 629 (2002).
[18]X. Li, S. Feng, Z. Feng, S. Pan, Y. Lv, K. Bai, X. Lu, J. Qin, and Y. Zhang, Appl. Phys. Lett. **122**(7), 073501 (2023).
[19]X. Li, T. Pu, L. Li, and J.-P. Ao, IEEE Electron Device Lett. **41**(4), 601 (2020).
[20]S. J. William, *Engineering Heat Transfer* (CRC Press, 2018).
[21]S. Ghosh, M. Frentrup, A. M. Hinz, J. W. Pomeroy, D. Field, D. J. Wallis, M. Kuball, and R. A. Oliver, Adv. Mater. **37**, 2413127 (2025).
[22]T. Zhan, M. Xu, Z. Cao, C. Zheng, H. Kurita, F. Narita, Y. J. Wu, Y. Xu, H. Wang, M. Song, W. Wang, Y. Zhou, X. Liu, Y. Shi, Y. Jia, S. Guan, T. Hanajiri, T. Maekawa, A. Okino, and T. Watanabe, Micromachines **14**(11), 2076 (2023).
[23]H. Qie, J. Liu, Q. Li, Q. Sun, H. Gao, X. Sun, Y. Zhou, and H. Yang, Appl. Phys. Lett. **121**(21), 212106 (2022).
[24]M. Rudolph, C. Fager, and D. E. Root, *Nonlinear Transistor Model Parameter Extraction Techniques* (Cambridge University Press, 2011).
[25]K. Park and C. Bayram, Appl. Phys. Lett. **109**(15), 151904 (2016).
[26]E. A. Douglas, F. Ren, and S. J. Pearton, J. Vac. Sci. Technol. B **29**(2), 020603 (2011).