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On the Generation and Recovery of Interface Traps in MOSFETs Subjected to NBTI, FN, and HCI Stress

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***Abstract*—A common framework for interface-trap (N_{IT}) generation involving broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds is developed for negative bias temperature instability (NBTI), Fowler–Nordheim (FN), and hot-carrier injection (HCI) stress. Holes (from inversion layer for pMOSFET NBTI, from channel due to impact ionization, and from gate poly due to anode–hole injection or valence-band hole tunneling for nMOSFET HCI) break $\equiv$Si$-$H bonds, whose time evolution is governed by either one-dimensional (NBTI or FN) or two-dimensional (HCI) reaction–diffusion models. Hot holes break $\equiv$Si$-$O bonds during both FN and HCI stress. Power-law time exponent of N_{IT} during stress and recovery of N_{IT} after stress are governed by relative contribution of broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds (determined by cold- and hot-hole densities) and have important implications for lifetime prediction under NBTI, FN, and HCI stress conditions.**

***Index Terms*—Anode–hole injection (AHI), charge pumping (CP), Fowler–Nordheim (FN), hot-carrier injection (HCI), interface traps (N_{IT}), negative bias temperature instability (NBTI), reaction–diffusion (R–D) model, stress-induced leakage current (SILC), valence-band hole tunneling (VBHT).**

I. Introduction

INTERFACE-TRAP (N_{IT}) generation is an important reliability concern in MOSFETs subjected to negative bias temperature instability (NBTI), Fowler–Nordheim (FN), and hot-carrier injection (HCI) stress [1]–[12]. It is generally believed that N_{IT} generation is due to breaking of $\equiv$Si$-$H bonds at the Si$-$SiO$_2$ interface and the resultant production of $\equiv$Si$-$(N_{IT}), which show up as P_b centers in electron spin resonance (ESR) studies [13]. The time evolution of N_{IT} shows power-law dependence, with larger value of exponent n for FN and HCI compared with NBTI stress. On the other hand, unlike HCI and FN stress, significant N_{IT} recovery has been observed after NBTI stress [14], [15]. The mechanism of N_{IT} generation during stress and any recovery of N_{IT} after stress must be properly understood and modeled for accurate prediction of device lifetime under actual operating conditions.

It is now believed that inversion-layer (cold) holes are responsible for the breaking of $\equiv$Si$-$H bonds during NBTI stress in pMOSFETs [4]. Classical one-dimensional (1-D) reaction–diffusion (R–D) model [16] can successfully explain N_{IT} generation and recovery characteristics for NBTI stress [17], [18]. R–D model suggests that N_{IT} generation is due to the breaking of interfacial $\equiv$Si$-$H bonds and subsequent diffusion of released H species into the oxide bulk. N_{IT} recovery is due to back diffusion of H species toward the Si$-$SiO$_2$ interface and repassivation of $\equiv$Si$-$. R–D model can explain the (relatively) lower n of N_{IT} generation during NBTI stress as due to release and diffusion of either or both neutral H^O and H_2 species [18].

Note that the crucial difference between NBTI and HCI or FN is the presence of hot electrons (HE) and hot holes (HH) for the latter stress conditions [4], [7], [10]. Significant efforts were made in the past to understand whether only electrons, or only holes, or both electrons and holes are responsible for breaking of $\equiv$Si$-$H bonds during HCI and FN stress [5]–[10], [12], [19], [20]. The higher n of N_{IT} generation during uniform FN stress can be explained within the 1-D R–D framework by assuming possible release and subsequent drift of H^+ species [18]. A two-dimensional (2-D) extension of the classical R–D model, which considers localized (near drain junction) breaking of interfacial $\equiv$Si$-$H bonds and subsequent 2-D diffusion of released H^O species, has been proposed to model HCI [21].[1] The model suggests that the spread of HCI degraded region (due to broken $\equiv$Si$-$H bonds) determines n during stress and recovery after stress. However, the above models need experimental validation, and much work is needed to develop a unified model for N_{IT} generation under all stress conditions.

Furthermore, whereas NBTI stress (negligible hot carriers) produce only N_{IT} [4], HCI and FN stress (hot carriers present) also produce bulk traps (N_{OT}) [7], [10]–[12], [23]–[26]. N_{OT} generation is believed to be due to broken $\equiv$Si$-$O bonds at the oxide bulk [24]–[26]. There has been significant debate on whether HH or H^+ diffusion (following breaking of $\equiv$Si$-$H bonds) break $\equiv$Si$-$O bonds during FN and HCI stress [24], [25], [27], [28]. Broken $\equiv$Si$-$O bonds at oxide bulk give rise to stress-induced leakage current (SILC) [7], [12], [24]–[26], [29], [30],[2] whereas those at (or near) Si$-$SiO$_2$ interface can contribute to overall measured N_{IT} [32]. However, unlike $\equiv$Si$-$H bonds, broken $\equiv$Si$-$O bonds are not known to recover at room temperature after the stress is removed. It is important to understand and quantify the nature and composition of N_{IT} buildup due to broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds [33], [34] (and check for the release of H^+, if any), as these scenarios lead to substantially different lifetime projections for NBTI, FN, and HCI stress. We know of no effort so far that has

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[1] Alternatively, the stretched-exponent model [22] also explains power-law dependence of N_{IT} generation.

[2] An alternative viewpoint [31] for the origin of SILC is the bridging of H^+ into an existing oxygen vacancy.

successfully differentiated between these two types of $N_{\rm IT}$ generation processes for a wide range of stress conditions.

This paper attempts to develop a common framework for $N_{\rm IT}$ generation and recovery under NBTI, FN, and HCI stress conditions. The contribution of broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds on $N_{\rm IT}$ is explored by varying HE and HH energies under different stress configurations and monitoring $N_{\rm IT}$ buildup and recovery for successive stress and poststress periods. For uniform (NBTI or FN) stress, various combinations of $\equiv$Si$-$H and $\equiv$Si$-$O related defects are created by stressing pMOSFETs at different gate (V_G) and substrate (V_B) voltages. It is shown that when stressed at low V_G $(V_B = 0)$ such that HH generation is negligible, $\Delta N_{\rm IT}$ is due to broken $\equiv$Si$-$H bonds, a fraction of which recovers after stress is removed. When HH generation is increased (by increasing V_B) for any stress V_G [4], enhanced $\Delta N_{\rm IT}$ is observed. HH-induced additional $\Delta N_{\rm IT}$ does not recover and shows a unique power law in time that matches well with that of SILC. It is conclusively shown that additional $\Delta N_{\rm IT}$ caused by $V_B > 0$ stress is due to HH-induced broken $\equiv$Si$-$O bonds at the Si$-$SiO$_2$ interface.

For nonuniform HCI stress in nMOSFETs, HE and HH densities were varied by carefully designed experiments on devices having different channel length L and oxide thickness $T_{\rm PHY}$, under different V_G, V_B, and drain (V_D) voltages. The localized HE and HH density distributions under different stress configurations were obtained from full-band Monte Carlo simulations. It is shown that 2-D R–D model (concerning spread of broken $\equiv$Si$-$H bonds) alone is insufficient; contribution due to broken $\equiv$Si$-$O bonds (due to HH) must also be taken into account to explain the generation and recovery of $N_{\rm IT}$ during HCI stress under a wide range of stress conditions. It is also shown that channel HE do not directly break $\equiv$Si$-$H bonds during HCI stress. Holes, originated from impact ionization (II), anode–hole injection (AHI) [25], as well as from valence-band hole tunneling (VBHT) [35] processes break $\equiv$Si$-$H bonds. Hole (not electron)-induced breaking of $\equiv$Si$-$H bonds during nMOSFET HCI stress is consistent with inversion-layer hole-induced breaking of $\equiv$Si$-$H bonds for pMOSFET NBTI stress [4]. Based on relative contribution of $\equiv$Si$-$H and $\equiv$Si$-$O bonds, HCI degradation of devices is explored as supply $V_{\rm DD}$ is scaled. Our results have important implications for selecting stress voltages, projection of device lifetime under variety of operating conditions, and modeling of $N_{\rm IT}$ generation and recovery by 1-D and 2-D R–D models.

II. Experimental Results

Experiments were performed at $T = 27$ °C on n- and p-channel MOSFETs having (nonnitrided) gate oxides with $T_{\rm PHY}$ of 22, 24, 26, and 48 Å and L of 0.20 and 0.28 μm (width $W = 10$ μm). Uniform FN (or NBTI) stress was applied in pMOSFETs at different V_G and V_B. Nonuniform HCI stress was applied in nMOSFETs under different V_G, V_B, and V_D. FN (or NBTI) and HCI stress were followed by poststress periods with all terminals grounded (unless specifically mentioned otherwise). Both the stress and poststress periods were periodically interrupted to estimate $N_{\rm IT}$ by measuring charge pumping (CP) current $I_{\rm CP}$ [36], using a single-level pulse at frequency

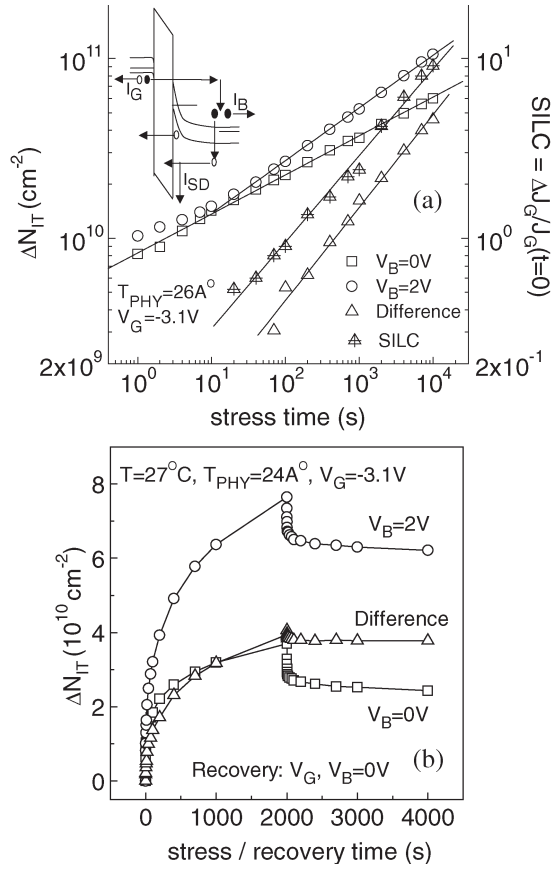

Fig. 1. (a) Time evolution of $N_{\rm IT}$ generation for uniform NBTI and FN stress at different V_B but fixed V_G. $V_B > 0$ stress-induced enhanced $N_{\rm IT}$ and SILC are also shown. SILC was measured at $V_G = -2.5$ V. Inset shows pMOSFET energy band under $V_B > 0$ stress. (b) Time evolution of $N_{\rm IT}$ generation and recovery during and after uniform stress at different V_B but fixed V_G.

$f = 800$ kHz. The delay (stress-off time) for measurement was fixed at 500 ms. Note that the value of n obtained in the presence of measurement delay is slightly higher than the true value due to unintentional recovery effects (where applicable) as explained in [14] and [15]. As degradation is uniform along the channel, $\Delta N_{\rm IT}$ $(= \Delta I_{\rm CP}/qfWL)$ can be easily determined for FN or NBTI stress. Determination of $\Delta N_{\rm IT}$ is difficult due to the nonuniform localized nature of HCI damage. Although it is possible to determine the spatial profile of HCI damage [11], [23], it is outside the scope of this work. Therefore, FN degradation is expressed in terms of $\Delta N_{\rm IT}$, whereas HCI degradation is expressed in terms of $\Delta I_{\rm CP}$. High V_G SILC was measured on "separate" identically stressed devices when required to monitor $N_{\rm OT}$. Multiple V_G sweeps were performed with delays (in-between sweeps) to nullify any charge-trapping-induced transient effects [37].

A. Uniform FN Stress Experiments in pMOSFETs

Fig. 1(a) shows the time evolution of $N_{\rm IT}$ for FN (or NBTI) stress under different V_B but constant V_G. Increasing V_B stress was used to generate increasing amount of HH in the channel by II, as depicted using the energy band diagram shown in the inset of Fig. 1(a). $\Delta N_{\rm IT}$ shows power-law time dependence, with lower n for stress at $V_B = 0$. $\Delta N_{\rm IT}$ increases with HH

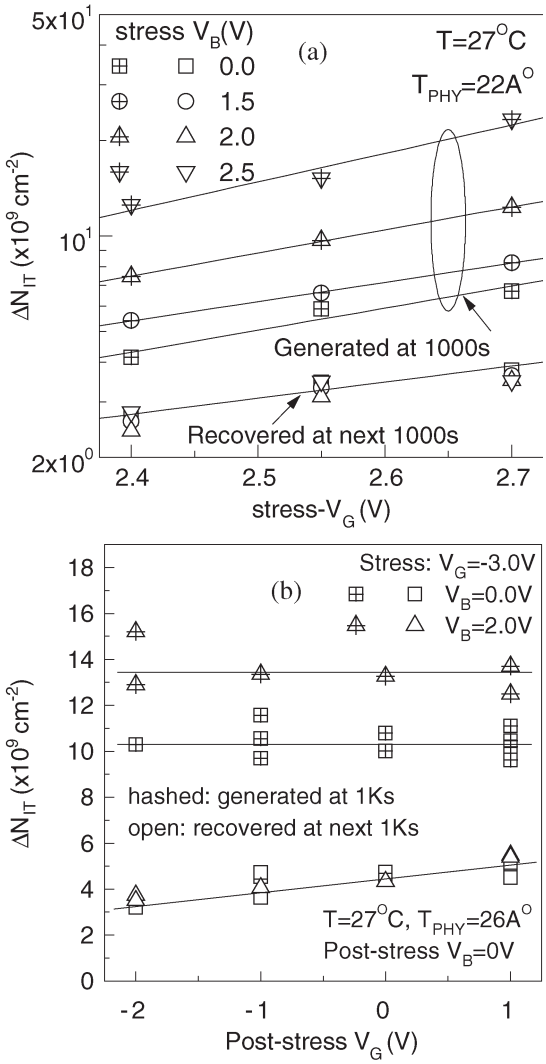

Fig. 2. $N_{\rm IT}$ generation after 1000-s uniform NBTI and FN stress and recovered after subsequent 1000-s poststress phase. (a) For different stress V_G and V_B but fixed (zero) poststress V_G. (b) For different stress V_B and poststress V_G but fixed stress V_G. Poststress $V_B = 0$.

energy as stress V_B is increased, and the power-law signature is maintained although with a higher value of n. Note that the time beyond which $V_B > 0$ stress-induced $\Delta N_{\rm IT}$ enhancement shows up reduces as V_B is increased. Time evolution of $V_B > 0$ stress-induced additional $\Delta N_{\rm IT}$ $\{\Delta^2 N_{\rm IT} = \Delta N_{\rm IT}(V_B > 0) - \Delta N_{\rm IT}(V_B = 0)\}$ together with measured high-V_G SILC are also shown in Fig. 1(a). Additional $\Delta N_{\rm IT}$ and SILC were observed only for $V_B > 0$ stress under significant HH generation; both show good correlation with quantum yield [38] of HH generation as V_B is increased (not shown) [4] and show power-law time dependence with very similar n. Fig. 1(b) shows the generation and recovery of $\Delta N_{\rm IT}$ after stress under different V_B but constant V_G. The absolute magnitude of $\Delta N_{\rm IT}$ recovery does not change with stress V_B, which implies that additional $\Delta N_{\rm IT}$ generated due to $V_B > 0$ stress is "permanent" and does not recover after removal of stress.

Fig. 2(a) shows $\Delta N_{\rm IT}$ generation and recovery for different V_G and V_B stress. It can be seen that $\Delta N_{\rm IT}$ generation increases with increase in both V_G and V_B during stress. However,

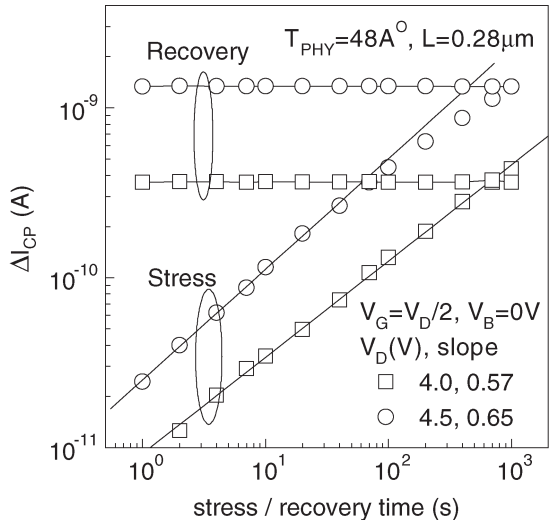

Fig. 3. Stress V_D dependence of time evolution of $\Delta I_{\rm CP}$ ($\sim \Delta N_{\rm IT}$) generation and recovery for 1000 s of HCI stress and poststress phases. Stress $V_G = V_D/2$, $V_B = 0$. All terminals were grounded during poststress.

increase in recovery is only seen following stress at increased stress V_G. Additional $\Delta N_{\rm IT}$ generated for $V_B > 0$ stress does not recover (identical recovery is seen for stress with different V_B for all stress V_G). Fig. 2(b) shows $\Delta N_{\rm IT}$ generation for $V_B = 0$ and $V_B > 0$ (fixed V_G) stress, and recovery for different poststress V_G. $\Delta N_{\rm IT}$ recovery is always identical for both $V_B = 0$ and $V_B > 0$ stress for all poststress V_G (once again, additional $\Delta N_{\rm IT}$ due to $V_B > 0$ stress does not recover) and is only "weakly" dependent on the sign and magnitude of poststress V_G.

B. Nonuniform HCI Stress Experiments in nMOSFETs

Fig. 3 shows the time evolution of $\Delta I_{\rm CP}$ ($\sim \Delta N_{\rm IT}$) generation and recovery for different V_D ($V_G = V_D/2$, $V_B = 0$, and fixed L and $T_{\rm PHY}$) stress. The usual power-law time dependence is seen but with much larger n compared with that for FN or NBTI stress (Fig. 1). Both the magnitude and n increase with increasing stress V_D. Long-time saturation seen at higher degradation level is due to reduction in drain current (and hence stress level). Unlike FN stress, $\Delta N_{\rm IT}$ does not recover (at all) after the removal of stress, which is true for all V_D (and all L, shown later) under these stress conditions.

Fig. 4(a) shows the time evolution of $\Delta I_{\rm CP}$ ($\sim \Delta N_{\rm IT}$) generation for $V_G = V_D/2$ stress under different V_B and on devices with different L (V_D and $T_{\rm PHY}$ fixed). Once again, power–law time dependence is seen for all stress conditions, and the saturation observed for higher degradation level is due to the reduction in stress level. The magnitude of $\Delta I_{\rm CP}$ increases with higher $|V_B|$ and lower L. However, n decreases with higher $|V_B|$ but is insensitive to reduction in L. Fig. 4(b) shows the time evolution of $\Delta I_{\rm CP}$ recovery after different stress conditions ($V_G = V_D/2$ and different V_B and L). Recovery is not seen after $V_B = 0$ stress, irrespective of L [similar to Fig. 3(b)]. Recovery is only seen after $V_B < 0$ stress, and both fractional and absolute recovery increase with increase in $|V_B|$. The fractional recovery remains the same, whereas the absolute recovery increases as L is scaled.

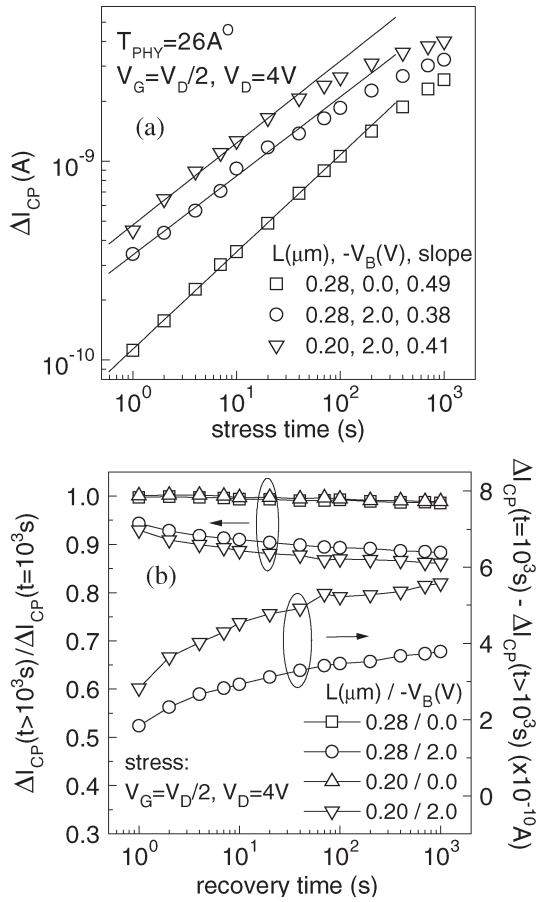

Fig. 4. Impact of L scaling on (a) time evolution of $\Delta N_{\rm IT}$ ($\sim \Delta I_{\rm CP}$) generation during HCI stress at different V_B (b) fractional and absolute recovery after stress. Stress $V_G = V_D/2$, V_D fixed. All terminals were grounded during poststress.

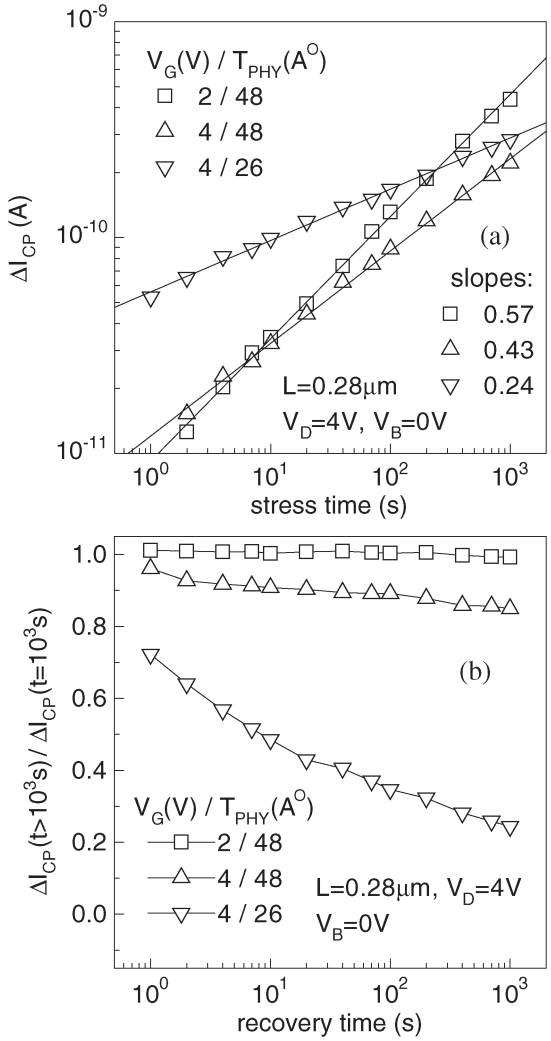

Fig. 5. (a) Time evolution of $\Delta N_{\rm IT}$ ($\sim \Delta I_{\rm CP}$) generation for HCI stress at different V_G, V_B, and $T_{\rm PHY}$. V_D constant for all stress configurations. (b) Fractional recovery of $\Delta I_{\rm CP}$ following stress at different V_G, V_B, and $T_{\rm PHY}$. All terminals were grounded during poststress.

Fig. 5(a) shows the time evolution of $\Delta I_{\rm CP}$ ($\sim \Delta N_{\rm IT}$) generation for different stress V_G and on devices having different $T_{\rm PHY}$ (V_D, V_B, and L fixed). Once again, power-law behavior is observed, with a reduction in n at higher V_G ($= V_D$). Moreover, although $\Delta I_{\rm CP}$ magnitude increases, n shows a drastic reduction for $V_G = V_D$ stress as $T_{\rm PHY}$ is scaled below the direct tunneling limit. Fig. 5(b) shows the time evolution of fractional $\Delta I_{\rm CP}$ recovery after different conditions of stress as Fig. 5(a). For $V_B = 0$, recovery is not observed after $V_G = V_D/2$ stress. Recovery is seen after $V_G = V_D$ ($V_B = 0$) stress, which drastically increases as $T_{\rm PHY}$ is scaled.

III. Simulation Results and Explanations

A. Uniform FN Stress Experiments in pMOSFETs

Note that FN stress with $V_B = 0$ (negligible HH) is the normal NBTI stress, where $\Delta N_{\rm IT}$ is known to be due to breaking of $\equiv$Si$-$H bonds at the Si$-$SiO$_2$ interface (the exact microscopic mechanism is unknown) and subsequent movement of released H into the oxide, which leaves behind $\equiv$Si$-(N_{\rm IT})$. As per the solution of 1-D R–D model for NBTI [16], $\Delta N_{\rm IT}$ would show a power-law behavior with time exponent $n \sim 0.165$ if the diffusing species is H_2 and $n \sim 0.25$ if it is H^O [18]. Any intermediate value ($n \sim 0.2$) can be explained by any of the following; 1) a mix of H_2 and H^O species; 2) H^O species plus dispersive transport; and 3) H_2 species plus recovery due to measurement delay [14], [15]. Independent measurements of the activation energy of diffusion points to the diffusion of H_2 species [4], [39] and, therefore, $n \sim 0.2$ is likely due to (3). The $n \sim 0.3$ time exponent of enhanced $\Delta N_{\rm IT}$ for $V_B > 0$ stress is due to the sum of two components: "normal" $\Delta N_{\rm IT}$ with $n \sim 0.2$ plus the "additional" $\Delta N_{\rm IT}$ with $n \sim 0.5$, as shown in Fig. 1(a). Depending on stress V_G and V_B, $\Delta N_{\rm IT}$ for $V_B > 0$ stress shows a wide range of n [40] based on the relative magnitude of normal and additional components (not shown).

The $n \sim 0.5$ time exponent of $\Delta^2 N_{\rm IT}$ can be due to 1) broken $\equiv$Si$-$H bonds followed by release and drift of H^+ as per the solution of 1-D R–D model [18], 2) broken $\equiv$Si$-$O bonds at or near the Si$-$SiO$_2$ interface [24]–[26], or 3) both. Note that SILC is always observed together with additional $\Delta N_{\rm IT}$ in the presence of HH, which clearly identifies that $\equiv$Si$-$O bonds are broken [26], [29]. Hence, at least a fraction of additional $\Delta N_{\rm IT}$ is due to broken $\equiv$Si$-$O bonds at Si$-$SiO$_2$ interface. It remains to be seen if additional $\equiv$Si$-$H bonds

are also broken with subsequent release of H^+, and whether H^+ diffusion plays some role in breaking $\equiv$Si$-$O bonds [27], [28], [30].

Note that 1-D R–D model also predicts that once stress is removed, some of the released H species come back to the interface and rapidly repassivate $\equiv$Si$-$ to form $\equiv$Si$-$H, thereby reducing $\Delta N_{\rm IT}$ [16]–[18]. However, any recovery of broken $\equiv$Si$-$O bonds at room temperature is not known. Fig. 1(b) shows that a fraction of $\Delta N_{\rm IT}$ generated during $V_B = 0$ and $V_B > 0$ stress recovers after stress. However, additional $\Delta N_{\rm IT}$ generated in the presence of HH for $V_B > 0$ stress does not recover after stress, and this is true for a wide range of stress V_G and V_B as shown in Fig. 2(a). Therefore, enhanced $\Delta N_{\rm IT}$ in the presence of HH for $V_B > 0$ stress is entirely due to additional contribution from broken $\equiv$Si$-$O bonds at the Si$-$SiO$_2$ interface. If H^+ ions were released and diffused from broken $\equiv$Si$-$H bonds, a fraction of them should have diffused back to the Si$-$SiO$_2$ interface and passivate at least a fraction of the additional $\equiv$Si$-$. This would have resulted in larger recovery after $V_B > 0$ stress, contrary to observed results. Identical post-V_G dependence of recovery as shown in Fig. 2(b) suggests similar diffusion species for both $V_B = 0$ and $V_B > 0$ stress. The time exponent of $n \sim 0.2$ during $V_B = 0$ stress and the insensitivity of $\Delta N_{\rm IT}$ recovery to poststress V_G can only be explained if the diffusing H species is always neutral.

Therefore, $N_{\rm IT}$ generation has two different origins due to broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds. When HH generation is insignificant, $N_{\rm IT}$ is due to broken $\equiv$Si$-$H bonds at the Si$-$SiO$_2$ interface and subsequent diffusion of H_2, a fraction of which recovers after stress. Additional $\equiv$Si$-$H bonds can get broken in the presence of HH. However, because HH density is much less than that of inversion-layer (cold) holes, HH-induced broken $\equiv$Si$-$H bonds would be insignificant compared with $\equiv$Si$-$H bonds broken by cold holes. No evidence is observed for diffusion of H^+ when HH is absent or present. In the presence of large HH generation, broken $\equiv$Si$-$O bonds at or very close to the Si$-$SiO$_2$ interface also makes an additional contribution and increases the overall magnitude and power-law time exponent n of measured $N_{\rm IT}$. Unlike broken $\equiv$Si$-$H bonds, broken $\equiv$Si$-$O bonds do not recover after stress. However, the exact microscopic mechanism of how inversion-layer cold holes break $\equiv$Si$-$H bonds and HH breaks $\equiv$Si$-$O bonds is not yet understood and calls for further (microscopic) modeling and analysis.

B. Nonuniform HCI Stress Experiments in nMOSFETs

As mentioned in Section I, the correlation of n and fractional recovery for HCI stress has been predicted by the 2-D R–D model [21]. It was proposed that larger spread of the degraded (broken $\equiv$Si$-$H bonds) region would produce lower n and larger recovery during stress and poststress phases, respectively. Note that the model does not comment on any $N_{\rm IT}$ contribution due to broken $\equiv$Si$-$O bonds at (or very close to) the Si$-$SiO$_2$ interface [32] and does not predict $n > 0.5$. To verify whether HCI results can be explained by 2-D R–D model, process, device, and full band Monte Carlo simulations were performed using well-calibrated DIOS, DESSIS [41], and SMC [42] simulators. Note that for the devices used in this study, CP measurement probes the drain half of the channel, from the center up to a fractional length (L_F) of about 0.4 [11], [23]. Therefore, HE and HH density distributions up to $L_F = 0.4$ should be used to interpret the experimental results.

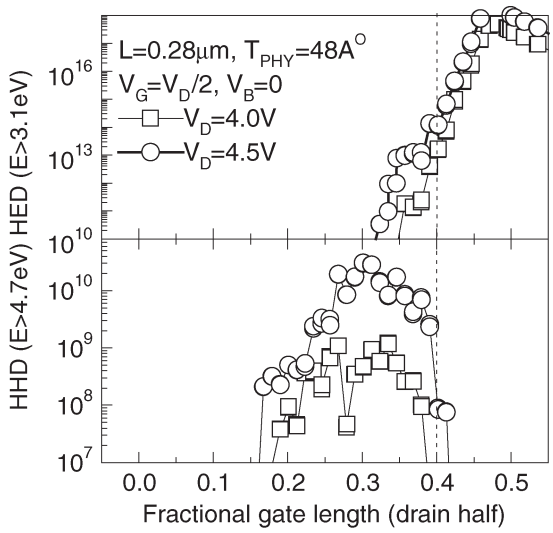

Fig. 6. Spatial distribution of simulated HE and HH densities along the channel and at the Si$-$SiO$_2$ interface under different V_D. All conditions similar to Fig. 3. $x = 0$ corresponds to the center of channel, whereas $x = 0.5$ corresponds to the gate edge on the drain side.

Fig. 6 shows simulated HE and HH profiles for different stress V_D ($V_G = V_D/2$, $V_B = 0$, and fixed $T_{\rm PHY}$ and L). The HE and HH spread shows very little increase, whereas HH peak increases by a large amount as V_D is increased. The observed $n > 0.5$ time exponent and increase in n with increase in V_D cannot be explained by 2-D R–D model based on localized broken $\equiv$Si$-$H bonds. These results can only be explained if increased contribution from broken $\equiv$Si$-$O bonds (due to increased HH density at higher V_D) is assumed. No recovery observed after the removal of stress also suggests that for $V_G = V_D/2$, $V_B = 0$ stress (on relatively thicker $T_{\rm PHY}$ devices), broken $\equiv$Si$-$O bonds dominate $N_{\rm IT}$ contribution. Any contribution due to $\equiv$Si$-$H bonds (by HE and/or by holes out of II) must be insignificant or highly localized to have zero recovery after stress. However, as mentioned before, the connection between HH density and breaking of $\equiv$Si$-$O bond is yet unclear and needs attention.

Fig. 7 shows HE and HH profiles for different stress V_B and L ($V_G = V_D/2$, and fixed V_D and $T_{\rm PHY}$). The spread of HE distribution increases with higher $|V_B|$ and lower L, whereas the peak and spread of HH distribution remain unaffected at higher $|V_B|$ and increases by a large amount at lower L. Inasmuch as $V_B < 0$ stress does not impact HH density, nonrecoverable $\equiv$Si$-$O contribution remains unchanged between $V_B = 0$ and $V_B < 0$ stress. However, the spread of II [42], [43] (not shown) and HE distribution (shown) increase as V_B is made negative and so is the spread of broken $\equiv$Si$-$H bonds (assuming impact ionized holes and/or HE breaks $\equiv$Si$-$H bonds). Therefore, 2-D R–D model in principle can explain lower n and larger fractional as well as absolute recovery observed for $V_B < 0$ stress.

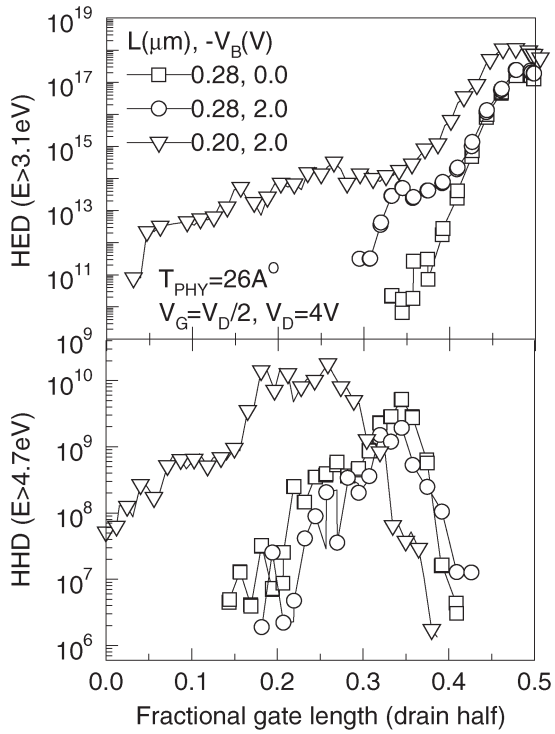

Fig. 7. Spatial distribution of simulated HE and HH densities along the channel and at the $Si-SiO_2$ interface under different L and V_B. All conditions similar to Fig. 4. $x = 0$ corresponds to the center of channel, whereas $x = 0.5$ corresponds to the gate edge on the drain side.

Note that both II (not shown) and HE spread also increase as L is scaled. A naive application of 2-D R–D model as above would suggest reduced n and larger recovery as L is scaled. This is contrary to the experimental result (no change in n as L is scaled, see Fig. 4). Therefore, additional contribution due to broken $\equiv$Si$-$O bonds must be considered. Both the peak and spread of HH distribution increase as L is scaled, which would suggest increased $\equiv$Si$-$O contribution. Increased II and HE spread at lower L would also imply increased $\equiv$Si$-$H contribution. In general, n can either reduce or increase as L is scaled, depending on the relative increase of $\equiv$Si$-$H and $\equiv$Si$-$O contributions. For the present case, no change in n implies similar increase in $\equiv$Si$-$H and $\equiv$Si$-$O contributions as L is scaled. Moreover, because higher $N_{\rm IT}$ generation at lower L is contributed by both $\equiv$Si$-$H (recoverable) and $\equiv$Si$-$O (nonrecoverable), fractional recovery remains almost the same, whereas absolute recovery increases (following a $V_B < 0$ stress) as L is scaled and can explain the observed results.

It is clear from the above discussion that HH breaks $\equiv$Si$-$O bonds and either HE and/or impact ionized (not necessarily hot) holes break $\equiv$Si$-$H bonds, both of which determine the time exponent and recovery fraction during and after stress, respectively. Although the role of HH behind broken $\equiv$Si$-$O bonds is clearly established (the exact mechanism that governs the power-law time exponent is yet unknown), it is not clear so far whether either or both HE and impact ionized holes break $\equiv$Si$-$H bonds.

Fig. 8 shows HE profile as V_G is increased and $T_{\rm PHY}$ is scaled (fixed V_D, V_B, and L). Note that HE spread does not increase at higher V_G and lower $T_{\rm PHY}$. Moreover, II and HH density become insignificant for $V_G = V_D$ stress (for all $T_{\rm PHY}$). Dominant HH generation can explain $n > 0.5$ slope and negligible recovery for $V_G = V_D/2, V_B = 0$ stress (thicker $T_{\rm PHY}$). The absence of recovery under such condition implies negligible or highly localized (HE or impact ionized hole induced) broken $\equiv$Si$-$H bonds. As HE spread does not significantly increase from $V_G = V_D/2$ to $V_G = V_D$ stress, absence of HH-induced broken $\equiv$Si$-$O bonds for $V_G = V_D$ stress alone cannot explain observed reduction in n and higher recovery. Furthermore, in spite of no change in HE spread, n reduces and recovery increases drastically as $T_{\rm PHY}$ is scaled. Therefore, the observed changes in n and fractional recovery for varying stress V_G and $T_{\rm PHY}$ cannot be explained by 2-D R–D model if one assumes HE breaks $\equiv$Si$-$H bonds and HE spread equals the spread of broken $\equiv$Si$-$H bonds.

Note that for nMOSFET HCI stress, holes can also reach $Si-SiO_2$ interface via AHI [25] and VBHT [35] processes (under favorable oxide field), as shown using the energy band diagram of Fig. 9(a). Fig. 9(b) plots the electron energy

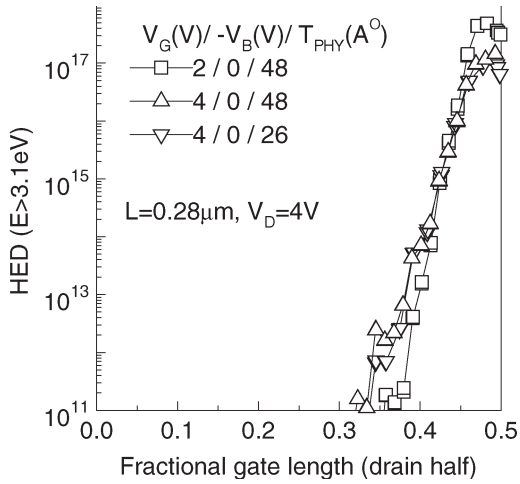

Fig. 8. Spatial distribution of simulated HE density along the channel and at the $Si-SiO_2$ interface under different stress V_G, V_B, and $T_{\rm PHY}$. All conditions similar to Fig. 5. $x = 0$ corresponds to the center of channel, whereas $x = 0.5$ corresponds to the gate edge on the drain side.

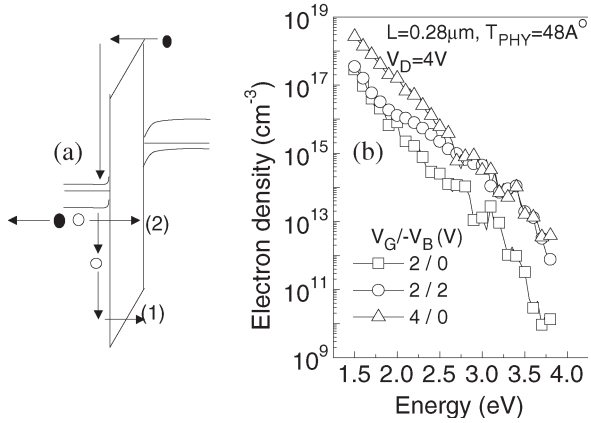

Fig. 9. (a) Energy band diagram for nMOSFET in inversion showing 1) AHI and 2) VBHT processes. (b) Simulated EED for different stress V_G and V_B. Data were extracted at the $Si-SiO_2$ interface and at the point of maximum electron injection.

distribution (EED) at the $Si-SiO_2$ interface and at a point of maximum electron injection for various stress conditions. Compared with $V_G = V_D/2$, $V_B = 0$, both $V_G = V_D/2$, $V_B < 0$ as well as $V_G = V_D$, $V_B = 0$ stress increase the population of high energy tail of EED. Higher HE spread and higher EED tail would increase gate current (I_G) for $V_G = V_D/2$, $V_B < 0$ stress [43]. Higher EED tail and higher spatial area of favorable oxide field would increase I_G for $V_G = V_D$, $V_B = 0$ stress. Increase in electron gate current would increase AHI for these conditions. By assuming lateral spreading of injected electrons inside the gate poly, back-injected holes due to AHI would reach the $Si-SiO_2$ interface over a wider area. Furthermore, as $T_{\rm PHY}$ is reduced below the direct tunneling limit, increased VBHT would cause holes to reach the $Si-SiO_2$ interface more uniformly over an even wider area.

We propose that even for HCI stress, $\equiv$Si−H bonds are broken by holes (and not by electrons), consistent with hole-induced mechanism observed for NBTI stress. For $V_G = V_D/2$ stress, broader II area [43] and larger AHI would produce larger spread of broken $\equiv$Si−H bonds for $V_B < 0$. Even if HE spread remains constant and II reduces with increase in $V_G\,(= V_D)$, increase in AHI over a wider area in the channel causes larger spread of broken $\equiv$Si−H bonds. As $T_{\rm PHY}$ is scaled below the direct tunneling limit, holes due to VBHT create a very wide spread of broken $\equiv$Si−H bonds. Now, it is possible to explain the reduction in n during stress and increase in fractional recovery after stress for higher stress $|V_B|$ and V_G and lower $T_{\rm PHY}$ within the 2-D R–D model framework.

Fig. 10 summarizes the parameter dependence of $\equiv$Si−H and $\equiv$Si−O contribution and its effect on n and recovery for HCI stress. For $V_G = V_D/2$, $V_B = 0$, increased n and no recovery as V_D is increased is due to increased $\equiv$Si−O contribution due to increased HH density. As V_G is increased to $V_G = V_D$, n reduces and recovery increases due to reduction in $\equiv$Si−O contribution (negligible HH) and increased $\equiv$Si−H contribution over a larger spread due to increased AHI. On the other hand, for $V_B < 0\,(V_G = V_D/2)$, increased II area and increase in AHI cause broken $\equiv$Si−H over a wider spread, resulting in further reduction in n and increased recovery. Increased VBHT as $T_{\rm PHY}$ is scaled reduces n and increases recovery by an even larger extent. Finally, II, HH generation, and AHI (due to HE) increase as L is scaled. Hence, relative increase of $\equiv$Si−H (due to holes from II and AHI) and $\equiv$Si−O (due to HH) contribution determines overall n and fractional recovery, whereas absolute recovery always increases as L is scaled. Fig. 10 also shows the prevalence of different physical mechanisms and their effect as V_G is switched from 0 to V_D. For $V_B = 0$, peak substrate current (I_B) stress breaks mostly $\equiv$Si−O bonds (HH), and any broken $\equiv$Si−H bonds must be negligible or highly localized. Therefore, large n and no recovery are seen. However, for $V_B < 0$, peak I_B stress breaks both $\equiv$Si−O and $\equiv$Si−H (II and AHI). Therefore, n reduces and some recovery is seen. As HH generation is negligible, peak gate current I_G stress generates only $\equiv$Si−H (AHI and VBHT), and lower n and higher recovery fraction are observed.

Fig. 11 shows peak HH density for $V_G = V_D/2$ stress and peak HE density for both $V_G = V_D/2$ and $V_G = V_D$ stress simulated for different stress V_D. It can be clearly seen that V_D scaling results in much larger relative reduction in peak HH density compared with peak HE density (hence AHI). Moreover, VBHT should also increase as $T_{\rm PHY}$ is scaled. Therefore,

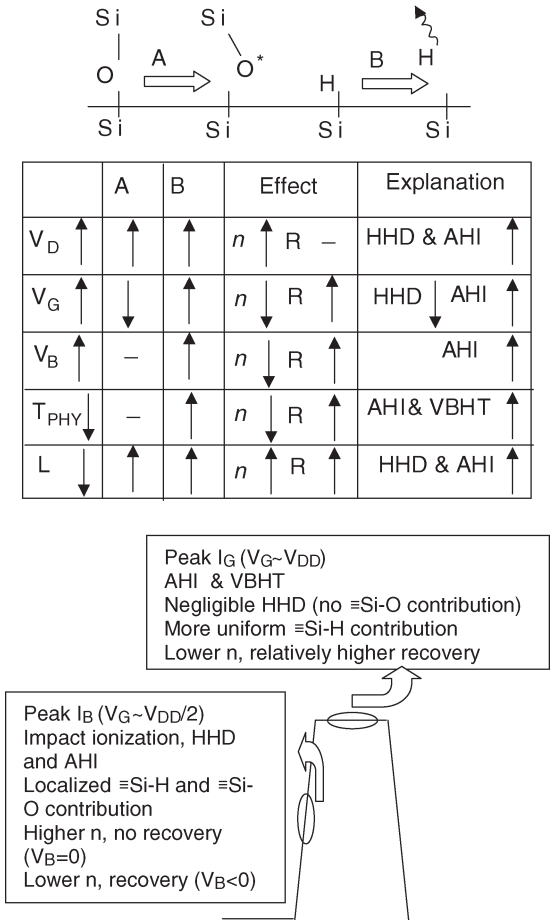

Fig. 10. Summary of HCI results and physical mechanisms that influence power-law time exponent of $N_{\rm IT}$ generation and $N_{\rm IT}$ recovery under different stress and device variables. Various degradation mechanisms operating at peak I_B and peak I_G stress conditions are also shown.

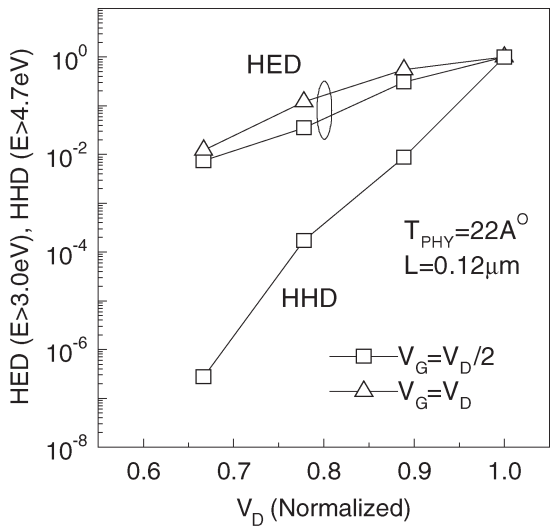

Fig. 11. Simulated peak HE density $(V_G = V_D/2, V_G = V_D)$ and peak HH density $(V_G = V_D/2)$ for different stress $V_D (V_B = 0)$. Data normalized for easy reference.

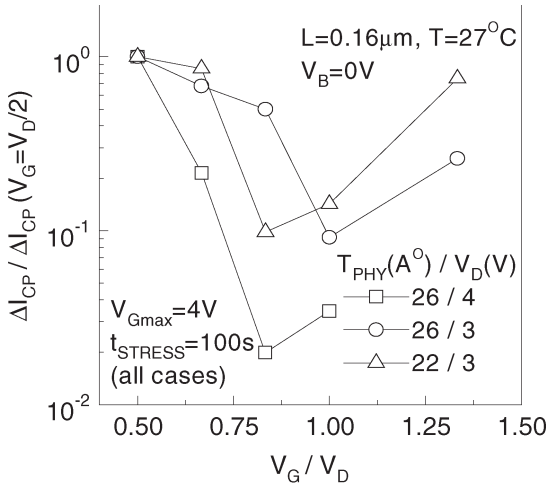

Fig. 12. Generated $\Delta I_{\rm CP}$ ($\sim \Delta N_{IT}$) as a function of stress V_G/V_D as V_G is varied for different V_D and $T_{\rm PHY}$. $\Delta I_{\rm CP}$ normalized to the $V_G = V_D/2$ value for easy reference.

as V_D and $T_{\rm PHY}$ are scaled (as a consequence of L scaling), it is expected that $\equiv$Si$-$O contribution at peak I_B stress would reduce more in comparison with $\equiv$Si$-$H contribution for peak I_G stress. Therefore, peak I_G stress would show significant $N_{\rm IT}$ compared with peak I_B stress. Fig. 12 shows normalized (to that at $V_G = V_D/2$ stress) $\Delta I_{\rm CP}$ as a function of stress V_G/V_D as V_G is varied for a given V_D and $T_{\rm PHY}$. As V_G is increased relative to $V_G = V_D/2$ stress, $\Delta I_{\rm CP}$ first reduces but then increases for larger V_G values due to larger AHI and VBHT. The relative increase of $\Delta I_{\rm CP}$ at higher V_G is more for lower stress V_D (more reduction in HH-induced broken $\equiv$Si$-$O bonds) and lower $T_{\rm PHY}$ (more increase in VBHT-induced broken $\equiv$Si$-$H). This is consistent with the above prediction.

IV. Conclusion

To summarize, this paper studies the composition of generated $N_{\rm IT}$ during NBTI, FN, and HCI stress. In the absence of HH for NBTI stress in pMOSFETs, inversion-layer (cold) holes cause $N_{\rm IT}$ generation by breaking $\equiv$Si$-$H bonds. Released H moves away from the Si$-$SiO$_2$ interface as neutral H$_2$ and governs the time evolution of $N_{\rm IT}$ buildup, which shows a power law with relatively lower value of time exponent n. A fraction of H$_2$ moves back to the interface and passivates broken $\equiv$Si$-$, causing some recovery of generated $N_{\rm IT}$ after stress. For uniform FN stress when HH generation and injection into the oxide is significant, broken $\equiv$Si$-$O bonds (via yet unknown mechanism) also contributes to $N_{\rm IT}$, which show a power law with larger n and does not recover after stress. The sum of broken $\equiv$Si$-$H and $\equiv$Si$-$O components governs the overall $N_{\rm IT}$ generation and recovery characteristics. No evidence has been found for the release of H$^+$ following breaking of $\equiv$Si$-$H bonds even in the presence of HH during stress.

For nonuniform HCI stress in nMOSFETs, relative contribution of broken $\equiv$Si$-$H and $\equiv$Si$-$O bonds also determines $N_{\rm IT}$ generation and recovery characteristics. Broken $\equiv$Si$-$O bonds exist mostly during peak I_B ($V_G = V_D/2$) stress, cause increase in n and do not recover after stress, depend on 2-D HH distribution (verified by full-band Monte Carlo simulations), increase at lower L and higher V_D, remain constant as V_B is varied, and disappear for peak I_G ($V_G = V_D$) stress. Broken $\equiv$Si$-$H bonds exist for both peak I_B (only for $V_B < 0$) and peak I_G stress, cause reduction in n and a fraction recover after stress (depends on spatial spread), and increase with higher $|V_B|$, V_G, and lower $T_{\rm PHY}$. Broken $\equiv$Si$-$H bonds do not directly depend on 2-D HE distribution, but rather on distribution of holes coming from II and AHI and VBHT for various stress conditions. Due to significant contribution of broken $\equiv$Si$-$O bonds, the lateral spread of broken $\equiv$Si$-$H bonds alone cannot explain all the observed HCI behavior as is expected by the 2-D R–D model. However, the exact mechanism of HH-induced breaking of $\equiv$Si$-$O bonds needs to be quantified. Moreover, the hole (not electron)-induced breaking of $\equiv$Si$-$H bonds during HCI stress is also consistent with that observed during NBTI stress.

As V_D and $T_{\rm PHY}$ are scaled (as a consequence of L scaling), it is shown that peak I_G stress and contribution due to broken $\equiv$Si$-$H bonds would show progressively significant contribution. Finally, we speculate that ultrathin $T_{\rm PHY}$ nMOSFETs in CMOS inverter configuration would show (pMOSFET NBTI-like) positive bias temperature instability (PBTI) phenomenon triggered by VBHT from gate poly, with time exponent similar to pMOSFET NBTI effect. This requires further investigation.

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References

[1] K. Uwasawa, T. Yamamoto, and T. Mogami, "A new degradation mode of scaled p$^+$ polysilicon gate p-MOSFETs induced by bias temperature instability," in *IEDM Tech. Dig.*, 1995, pp. 871–874.

[2] T. Yamamoto, K. Uwasawa, and T. Mogami, "Bias temperature instability in scaled p$^+$ polysilicon gate p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 921–926, May 1999.

[3] D. Schroder and J. F. Babcock, "Negative bias temperature instability: Road to cross in deep sub micron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, Jul. 2003.

[4] S. Mahapatra, P. Bharath Kumar, and M. A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability in p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1371–1379, Sep. 2004.

[5] S. Ogawa and N. Shiono, "Interface-trap generation induced by hot-hole injection at the Si$-$SiO$_2$ interface," *Appl. Phys. Lett.*, vol. 61, no. 7, pp. 807–809, Aug. 1992.

[6] J.-H. Shiue, J. Y. Lee, and T.-S. Chao, "A study of interface trap generation by Fowler–Nordheim and substrate-hot-carrier stresses for 4-nm thick gate oxides," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1705–1710, Aug. 1999.

[7] D. Esseni, J. D. Bude, and L. Selmi, "On interface and oxide degradation in VLSI MOSFETs—Part II: Fowler–Nordheim stress regime," *IEEE Trans. Electron Devices*, vol. 49, no. 2, pp. 254–263, Feb. 2002.

[8] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot electron induced MOSFET degradation—Model, monitor and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 375–385, Feb. 1985.

[9] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot carrier degradation in n-channel and p-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2194–2209, Dec. 1988.

[10] G. Groeseneken, R. Bellens, G. Van den bosch, and H. E. Maes, "Hot carrier degradation in submicrometer MOSFETs: From uniform injection towards the real operating conditions," *Semicond. Sci. Technol.*, vol. 10, no. 9, pp. 1208–1220, Sep. 1995.
[11] S. Mahapatra, C. D. Parikh, V. Ramgopal Rao, C. R. Viswanathan, and J. Vasi, "Device scaling effects on hot-carrier induced interface and oxide trapped charge distributions in MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 789–796, Apr. 2000.
[12] D. Esseni, J. D. Bude, and L. Selmi, "On interface and oxide degradation in VLSI MOSFETs—Part I: Deuterium effect in CHE stress regime," *IEEE Trans. Electron Devices*, vol. 49, no. 2, pp. 247–253, Feb. 2002.
[13] E. H. Poindexter and P. J. Caplan, "Characterization of Si/SiO_2 interface defects by electron spin resonance," *Prog. Surf. Sci.*, vol. 14, no. 3, pp. 201–294, 1983.
[14] M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, "Dynamic recovery of negative bias temperature instability in p-type metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 83, no. 8, pp. 1647–1649, Aug. 2003.
[15] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, 2003, pp. 341–344.
[16] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, May 1977.
[17] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for p-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 345–348.
[18] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, "A comprehensive framework for predictive modeling of negative bias temperature instability," in *Proc. Int. Reliab. Phys. Symp.*, 2004, pp. 273–282.
[19] K. R. Hofmann, C. Werner, W. Weber, and G. Dorda, "Hot electron and hole emission effects in short n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-32, no. 3, pp. 691–699, Mar. 1985.
[20] S. K. Lai, "Two-carrier nature in interface trap generation in hole trapping and radiation damage," *Appl. Phys. Lett.*, vol. 39, no. 1, pp. 58–60, Jul. 1981.
[21] H. Kufluoglu and M. A. Alam, "A geometrical unification of the theories of NBTI and HCI time exponents and its implications for ultra-scaled planer and surround gate MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 113–116.
[22] O. Penzin, A. Hagghag, W. McMahon, E. Lyumkis, and K. Hess, "MOSFET degradation kinetics and its simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1445–1450, Jun. 2003.
[23] S. Mahapatra, C. D. Parikh, V. R. Rao, C. R. Viswanathan, and J. Vasi, "A comprehensive study of hot-carrier induced interface and oxide trap distributions in MOSFETs using a novel charge pumping technique," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 171–177, Jan. 2000.
[24] J. D. Bude, B. E. Weir, and P. J. Silverman, "Explanation of stress-induced damage in thin oxides," in *IEDM Tech. Dig.*, 1998, pp. 179–182.
[25] M. Alam, J. Bude, and A. Ghetti, "Field acceleration for oxide breakdown—Can an accurate anode hole injection model resolve the E vs. $1/E$ controversy," in *Proc. Int. Reliab. Phys. Symp.*, 2000, pp. 21–26.
[26] T. C. Yang and K. C. Saraswat, "Effect of physical stress on the degradation of thin SiO_2 films under electrical stress," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 746–755, Apr. 2000.
[27] J. H. Stathis and D. J. DiMaria, "Reliability projection of ultra thin oxides at low voltage," in *IEDM Tech. Dig.*, 1998, pp. 167–170.
[28] D. J. DiMaria, "Explanation for the polarity-dependence of breakdown in ultrathin silicon dioxide films," *Appl. Phys. Lett.*, vol. 68, no. 21, pp. 3004–3006, May 1996.
[29] M. Alam, "SILC as a measure of trap generation and predictor of $T_{\rm BD}$ in ultrathin oxides," *IEEE Trans. Electron Devices*, vol. 49, no. 2, pp. 226–231, Feb. 2002.
[30] D. J. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," *J. Appl. Phys.*, vol. 78, no. 6, pp. 3883–3894, Sep. 1995.
[31] P. E. Blochl and J. H. Stathis, "Hydrogen electrochemistry and stress induced leakage current in silica," *Phys. Rev. Lett.*, vol. 83, no. 2, pp. 372–375, Jul. 1999.
[32] D. Varghese, S. Mahapatra, and M. A. Alam, "Hole energy dependent interface trap generation in MOSFET Si/SiO_2 interface," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 572–574, Aug. 2005.
[33] D. Saha, D. Varghese, and S. Mahapatra, "On the generation and recovery of hot carrier induced interface traps: A critical examination of the 2D reaction diffusion model," *IEEE Electron Device Lett.*, vol. 27, no. 3, pp. 188–190, Mar. 2006.
[34] ——, "The role of anode hole injection and valence band hole tunneling on interface trap generation during hot carrier injection stress," *IEEE Electron Device Lett.,* submitted for publication.
[35] W. C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction-and valence-band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366–1373, Jul. 2001.
[36] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.
[37] J. De Blauwe, J. V. Houdt, D. Wellekens, G. Groeseneken, and H. E. Maes, "SILC-related effects in flash E^2PROM's—Part I: A quantitative model for steady-state SILC," *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1745–1750, Aug. 1998.
[38] S. Takagi, N. Yasuda, and M. Toriumi, "Experimental evidence of inelastic tunneling in stress-induced leakage current," *IEEE Trans. Electron Devices*, vol. 46, no. 2, pp. 335–341, Feb. 1999.
[39] M. L. Reed and J. D. Plummer, "Chemistry of $Si-SiO_2$ interface trap annealing," *J. Appl. Phys.*, vol. 63, no. 12, pp. 5776–5793, Jun. 1988.
[40] P. Bharath Kumar, T. R. Dalei, D. Varghese, D. Saha, S. Mahapatra, and M. A. Alam, "Impact of substrate bias on p-MOSFET negative bias temperature instability," in *Proc. Int. Reliab. Phys. Symp.*, 2005, pp. 700–701.
[41] *Users Manual, ISE TCAD*, Synopsis Inc., Mountain View, CA, 2002.
[42] J. D. Bude, M. R. Pinto, and R. K. Smith, "Monte Carlo simulation of CHISEL flash memory cell," *IEEE Trans. Electron Devices*, vol. 47, no. 10, pp. 1873–1881, Oct. 2000.
[43] J. D. Bude, "Gate current by impact ionization feedback in sub-micron MOSFET technologies," in *VLSI Symp. Tech. Dig.*, 1995, pp. 101–102.

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