APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

Extreme ultraviolet lithography and three dimensional integrated circuit—A review

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Extreme ultraviolet lithography (EUVL) and three dimensional integrated circuit (3D IC) were thoroughly reviewed. Since proposed in 1988, EUVL obtained intensive studies globally and, after 2000, became the most promising next generation lithography method even though challenges were present in almost all aspects of EUVL technology. Commercial step-and-scan tools for preproduction are installed now with full field capability; however, EUV source power at intermediate focus (IF) has not yet met volume manufacturing requirements. Compared with the target of 200 W in-band power at IF, current tools can supply only approximately 40–55 W. EUVL resist has improved significantly in the last few years, with 13 nm line/space half-pitch resolution being produced with approximately 3–4 nm line width roughness (LWR), but LWR needs 2× improvement. Creating a defect-free EUVL mask is currently an obstacle. Actual adoption of EUVL for 22 nm and beyond technology nodes will depend on the extension of current optical lithography (193 nm immersion lithography, combined with multiple patterning techniques), as well as other methods such as 3D IC. Lithography has been the enabler for IC performance improvement by increasing device density, clock rate, and transistor rate. However, after the turn of the century, IC scaling resulted in short-channel effect, which decreases power efficiency dramatically, so clock frequency almost stopped increasing. Although further IC scaling by lithography reduces gate delay, interconnect delay and memory wall are dominant in determining the IC performance. 3D IC technology is a critical technology today because it offers a reasonable route to further improve IC performance. It increases device density, reduces the interconnect delay, and breaks memory wall with the application of 3D stacking using through silicon via. 3D IC also makes one chip package have more functional diversification than those enhanced only by shrinking the size of the features. The main advantages of 3D IC are the smaller form factor, low energy consumption, high speed, and functional diversification. EUVL, if adopted, will continue to enable IC performance improvement at a slower rate, but 3D IC provides an alternative way to improve the system performance. The best scenario is the adoption of both EUVL and 3D IC. However, the possible further delay of EUVL could enhance the realization of 3D IC for IC system improvement. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4863412]

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EXTREME ULTRAVIOLET LITHOGRAPHY (EUVL)

EUVL introduction

Lithography has been a key technology in the semiconductor industry for improving chip performance. The wavelength used for exposure plays an important role in determining the patterning resolution. Original lithography used visible g-line (436 nm) and ultraviolet i-line (365 nm) lights produced by mercury arc lamps. Later, deep ultraviolet 248 nm KrF and 193 nm ArF excimer lasers were used for better lithographic resolution. Now, state-of-art lithography is using a 193 nm wavelength, immersion method, and multiple patterning approaches. Compared with 193 nm wavelength, shorter wavelength lithography, known as next-generation lithography (NGL), was proposed in the 1980s using 157 nm wavelength, extreme ultraviolet (EUV) light (e.g., 13.5 nm wavelength), X-ray (0.4 nm), and even shorter wavelengths of electron and ion beams. In the late 1990s, EUVL became the most promising NGL due to the advantage of optical projection lithography, although reflective optics has been used in EUVL optical systems. Because all available materials are strong absorbers of EUV light, no materials are transparent enough to make use of refractive optics.

Resolution, R (half pitch), of projection lithography is expressed as

$$R = k_1 \frac{\lambda}{NA}, \tag{1}$$

where λ is wavelength, NA is numerical aperture, k_1 is constant. Obviously, R can be reduced by increasing NA (e.g., immersion), decreasing k_1 factor (e.g., multiple patterning), and λ (e.g., 13.5 nm EUV light).

In order to improve lithographic resolution, EUVL attenuated phase-shift photomask was recently investigated using an absorber stack as a phase-shift material. Phase shift stacks, consisting of 32.1-nm thick ITO (indium tin oxide) and molybdenum[1] or 40.5-nm thick tantalum nitride (24-nm-thick) and molybdenum (16.5-nm-thick),[2] show advantages compared to partially multilayer-etched phase shifters.

EUVL was introduced as a high k_1 (about 0.4) and low NA (currently about 0.33) approach; thus, it offers potential extendibility to smaller feature size nodes. By increasing NA to 0.6 or decreasing wavelength to about 6.7 nm, it is possible for EUVL to reach sub-10 nm resolution.

However, we should not be so optimistic about EUVL applications. EUVL technology includes resist, printers, masks, metrology, inspection, and defect controls. Till now, there are critical challenges in source power, resist line width roughness (LWR), and mask.

EUV exposure tools

EUVL as a concept and design was proposed in 1988[3] and examined experimentally in 1989[4] and 1990.[5] Schematics of EUVL are shown in Figure 1.

The first challenge to build a EUV exposure tool is the EUV optics fabrication. From late 1990 to 2001, EUV LLC developed the first EUV full field exposure tool, Engineering Test Stand (ETS), to demonstrate the feasibility and capability

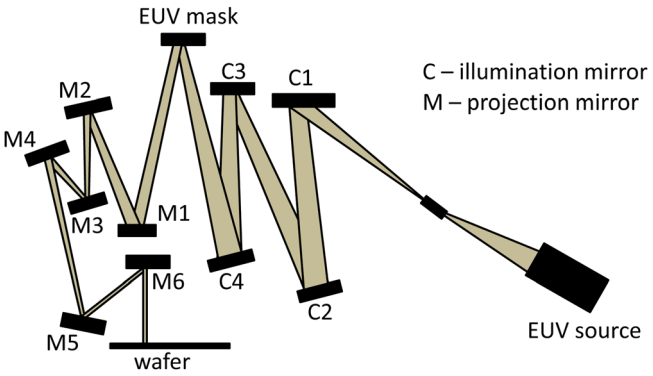

FIG. 1. Schematics of EUVL.

of a fully integrated EUVL exposure tool.[6] The ETS tool is the first full-field EUV exposure tool operated in a high vacuum condition. Although it could not meet the specifications of a EUV lithography production tool, it proves the feasibility of this new technology and shows a promising future, thereby convincing the industry to move forward on this technology.

In 2006, ASML installed alpha-demo (AD) EUVL exposure tools in Europe and the United States, showing that EUVL was advancing toward industrial production. The tools were full field size (26×33 mm^2), but EUV power at intermediate focus (IF) was only a few watts supplied by a tin-discharge-produced plasma (DPP) light source. The tool optics used six mirrors and 4× demagnification. The maximum NA was designed to be 0.25 with 50 nm resolution.[7]

In order to help EUV resist and mask development, small field EUV exposure tools with high NA and resolution such as micro-exposure tool (MET)[8] and micro-exposure stepper (MS-13) were developed.

From 2010, six pre-production tools, NXE 3100 made by ASML, were delivered to end users. The resolution of the tool is 28 nm with NA of 0.25. However, only about 10 W can be used for exposure, resulting in very low throughput.

A new exposure tool, NXE 3300B with NA of 0.33, began to be delivered to 11 end users since 2013. The tool's capability has improved to 13 nm resolution in a single exposure and is also capable of 9 nm resolution using spacer double patterning technology.[9] Its source power was improved to 55 W with adequate dose control, which corresponds to a throughput of 43 wafers per hour.

Today, all main integrated circuit (IC) manufacturing companies and industrial consortia are heavily involved with EUVL. The investment of ASML by Intel, Samsung, and TSMC, as well as acquisition of Cymer by ASML, shows the confidence of the semiconductor industry for the future of EUVL.

Single wavelength with narrow bandwidth is a basic requirement for projection lithography. A synchrotron source was used for the original pioneer studies,[4,5] but later it turned to DPP and laser-produced plasma (LPP) sources because of its high cost and large space requirement. Both DPP and LPP create several 100 000 K temperatures, which enable a 13.5 nm short wavelength emission.[10]

EUV source power is mainly determined by resist sensitivity. Resist with sensitivity of 10 mJ/cm^2 requires greater

than 180 W 2% bandwidth IF power.[11] However, collectable EUV power is very limited. For a DPP EUV source having 645 W at 2π sr solid angle within 2% bandwidth, only 42 W IF power were obtained.[12]

Both DPP and LPP sources (Figure 2) need emitting materials, among which tin and xenon are the most promising candidates. Xenon is cleaner than tin, but its emission spectra were not as strong as tin, making tin the current common emitting materials for EUV source.

DPP has high conversion efficiency, but collecting efficiency is low because EUV light can be collected only in a small solid angle. In addition, plasma electrode lifetime and debris mitigation could also be issues.

LPP was proposed as a EUV source in the first EUVL publication in 1988 and was used as source in the ETS tool later. The primary challenge is to obtain a high laser power (e.g., 10 kW) and pulse repetition rates of several kHz. Short laser pulses and high repetition rates tend to result in higher conversion efficiency.

High CE requires a fresh surface for the laser target, resulting in the use of tin droplets with small diameters of 20 μm. Recent progress on a pre-pulse approach plays an important role in the increase of EUV source power.[13]

In 2013, it was reported that LPP can continuously supply 40 W IF power for 6 h and 50 W for 1 h.[14] It is expected that obtaining 100 W EUV IF power is in the future. When this target is attained, EUVL will show a strong competitor to multiple patterning technology. Thus far, LPP is the leading candidate of EUV source.

EUV reflective optics requires a reflective mirror having a multilayer coating to reflect EUV light at a small incidence angle. The current multilayer mirror consists of 40 Mo/Si layer pairs.[15,16] Due to delays, the technology node of EUVL adoption is pushed to below 22 nm, or maybe even below 10 nm, so that the focus has been recently on 6.7 nm EUV source based on rare-earth emitters in order to improve the lithographic resolution.[17,18] However, the low source power and narrow reflective bandwidth of multilayering is a very critical challenge. For the same reason, EUVL with high NA and demagnification is also in consideration.[19]

Thermal stability is very important for Mo/Si multiplayer on the first multilayer mirror because the high heat load can cause inter-diffusion, change the d-space thickness, and shift the peak reflectance wavelength. A barrier layer is generally used between Mo and Si to prevent inter-diffusion and structural change.[20] A protective capping layer (e.g., silicon or ruthenium) covering the multilayer is also used to prevent the top molybdenum layer from oxidizing in atmospheric oxygen.

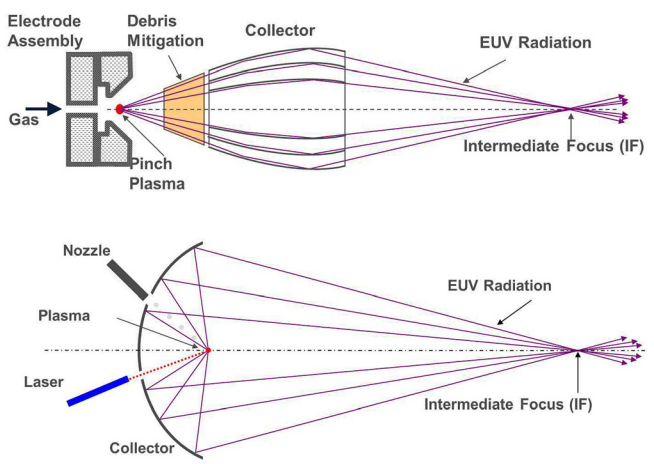

FIG. 2. DPP and LPP sources.

Projection-lithographic optics is composed of illumination (condenser) and projection optics, the former for light collection to illuminate a mask plane, and the latter to image the mask pattern onto the wafer. Field uniformity is a basic requirement for the illuminator.

Due to the limited EUV source power, collector optics should collect in-band light efficiently. Prevention or removal of contamination on collector optics created during EUV exposure is a challenge. Large size collectors favor solid angle, debris mitigation, and a long life, but make fabrication difficult.

In the EUVL projection optical system, six mirrors are currently used for an acceptable aberration control. Wavefront error (WFE) requirements for diffraction-limited imaging scale with wavelength, so that about 14× smaller allowable WFE for the EUVL system is required compared with 193 nm wavelength.[21] Three important parameters for the EUVL optical system are surface figure error (low spatial frequency roughness) for aberration control, mid-spatial frequency roughness (MSFR) for flare control, and high-spatial frequency roughness (HSFR) for scattering (reflectivity) control. After intensive studies in the 1990s and early 2000s, these optical challenges were overcome.

Resist

The basic requirements for EUVL resist are sensitivity, resolution, line width roughness (LWR) or line edge roughness (LER), outgassing, a pattern cross-sectional aspect ratio and profile, etch resistance, defect density, and reproducibility. Among them, it is a critical challenge to meet the requirements simultaneously on resolution, LWR, and sensitivity (RLS).

EUVL uses chemically amplified resist (CAR) due to the advantages of high sensitivity and resolution, but its LWR is relatively high, which becomes a significant issue. For the 22 nm feature, LWR should be controlled below 2 nm (3σ), which is about half of the current best available values.

The power limit of the EUV source necessitates a low exposure dose, requiring a high photoacid generator (PAG) loading and high sensitivity (e.g., 15 mJ/cm^2). The thinner photoresists (e.g., 50 nm) have to be used for EUV absorption and aspect ratio controls on small features, but thin resist requires a high etch resistance during pattern transfer.

Resist resolution depends on pattern collapse, mainly caused by the capillary force during the drying of the rinse liquid.[22–27] When the aspect ratio is higher than "critical aspect ratio," patterns will begin to collapse.[26,28] For a resist with a critical aspect ratio of three, 16 nm line patterns will require resist thickness of about 50 nm. EUV absorption in the resist and resulting profile also emphasize the use of thin

resist. For these reasons, current EUV resists have bilayer structure (about 50 nm thick sensitive layer plus underlayer) or sensitive layer combined with hard mask.

LWR is a very critical challenge for a EUVL resist. It is related with many parameters including dose, PAG properties, and process conditions. Shortening of exposure wavelength from 193 nm to 13.5 nm increases photon energy from 6 eV to 93 eV, which along with discrete photons, creates shot noise, and thus increases LWR.[29]

CAR properties are dependent mainly on PAG and polymer types. LWR is depending on PAG diffusion, so a popular method to reduce LWR is to use polymer-bound PAG. Small PAG size and high PAG concentrations have low LWR, and high quencher concentrations at good aerial image contrast also reduce LWR.[30]

Resist sensitivity is influenced by PAG properties and concentration. High PAG concentration gives high sensitivity. However, there is a conflict between resist sensitivity and outgassing, i.e., a highly sensitive PAG generates more decomposed products and thus more outgassing.

Currently, an approximate 13 nm line/space pattern was obtained at about 40 mJ/cm^2 dose, indicating the relaxation of a resolution challenge.[14] It is still a challenge to meet RLS simultaneously.

Mask

EUVL mask is the top challenge mainly due to defect control. The challenges exist in blank mask preparation and mask fabrication from raw stock. Displacement error control requires very flat (30 nm p-v) substrate with a low coefficient of thermal expansion (CTE) at less than 5 ppb/K. After decades of development, these challenges became non-critical except the defect control.

The EUVL mask should have defect density less than 0.0025 printable defects/cm^2 at a related technology node for both the mask substrate and the multilayer to obtain a mask blank yield of 60%,[31] which means an average 0.34 defect in the mask pattern area. Current defect control can reach about 40–50 defects per mask at 50 nm sensitivity. However, for current EUVL target technology nodes of 22 and 16 nm, final printable defect dimensions are 18 and 13 nm. That means that much more defects will be detected if the inspection tool with a higher sensitivity is available.

Phase defects, as shown in Figure 3, are special non-repairable defects for EUVL. They are located on the substrate surface or lower part of the multilayer and thus can distort most multilayers, and locally change the reflective property of the multilayer by changing the phase or amplitude. Most phase defects result from pits on the substrate surface. Due to the imperfection of substrate materials, it is extremely difficult to make the substrate surface without any pits or bumps in a few nanometer heights. Another defect is an amplitude defect. It is usually on top of the multilayer and repairable.

Allowable amplitude mask defect size is less than 80% of the technology node. With the EUVL target technology node shifting, tolerant defect size is scaling accordingly. In the near future, it will be impossible to produce real defect-free photomask, so several compromised approaches were examined, including pattern shift, pattern rotation, and design-aware defect-avoidance floorplanning of EUVL masks.[32–34]

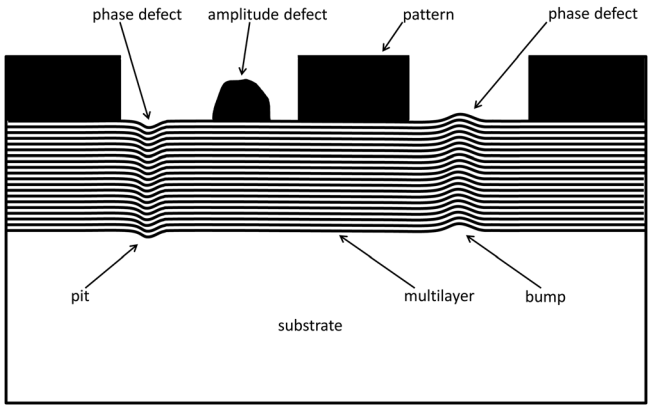

FIG. 3. Phase defects and multilayer distortion.

Production cost control requires that the EUVL mask blanks be inspected and repaired. Amplitude defects can be identified by using optical or electron-beam inspection; however, phase defects have to rely on at-wavelength light (actinic)[35–38] to carry out inspections. The actinic EUVL mask inspection tool is composed of a stable EUV source, optical system, and signal capture/processing system, with higher costs. Until now, there is no cost-effective actinic EUVL mask inspection tool available.

Because of the strong absorption of EUV light in any materials, the current EUVL system does not have a pellicle on the EUVL mask. It is very difficult to overcome this major challenge. Thermophoretic protection[39–42] and e-beam curtain methods were proposed, but the realizations are difficult due to the complexity. A 50-nm silicon membrane (with wire-grid) pellicles was proposed.[43] However, it is very challenging to make and use such a thin pellicle.

Due to three dimensional (3D) mask effects and the use of an off-axis incidence angle to the mask, a thinner absorber layer is expected to improve lithographic performance and reduce the pattern shift. The absorber stack thickness was reduced from original 150 nm down to the current 70–80 nm. Intentions for further reduction of the absorber layer lead studies on new absorber materials such as $TaTe_2O_7$ and ITO with an absorber stack thickness of about 45 nm.[44,45] However, these new absorber stacks need to be verified for etch properties, cleaning resistance, repairability, and optical properties before being acceptable.

EUVL mask fabrication is also challenge. It includes very tight control on the pattern cross section profile, cleaning resistance, sensitive inspection, and damage-free repairing.

Summary of EUVL

EUV lithography has gone through intensive global studies since proposed. Original critical technological challenges in EUVL reflective optics have been overcome; resist resolution was pushed down to 13 nm feature size; EUVL exposure tools now have better alignment accuracy, better optics, and 40–55 W EUV in-band light at the IF position.

The EUVL mask significantly improved the defect level with an advanced inspection tool. It is generally expected that volume production will soon come despite several delays in its adoption.

3D IC TECHNOLOGY

Introduction

The term 3D IC generally means an IC package having multiple device layers, which is different with 3D transistor structures such as the FinFET. 3D packaging and 3D integration are the common terms used for 3D ICs.

The real beauty of 3D IC technology is that it provides a revolutionary design methodology to allow improvements in both performance and power consumption. The IC designer can optimize the IC structure through functional partitioning using interconnection at both the transistor and functional block scales. The interconnect length between ICs on different device layers can be reduced from millimeters down to micrometers, which could make the interconnect signal propagation among ICs in different layers as fast as that of one IC. 3D IC also offers an alternate path to continue Moore's Law.

There is a strong demand for high-density heterogeneous chip packages suitable for small and lightweight mobile electronic products. Many CMOS image sensors using through silicon via (TSV) interconnection are used for today's mobile phone cameras.[46–48] TSV 3D IC stacking technology has great potential for all portable electronics because of the small form factor and low energy consumption.

3D ICs can have different die types stacked to add new functionality to a single package, something that has been called "More than Moore." This approach allows for non-digital functions, such as radio frequency (RF) communication, power control, passive components, and sensors, to migrate from separate chips into a single package.[49] Another special advantage is the ability to integrate die with different substrate types (e.g., Si and GaAs).

The genesis of the stacked IC concept is unclear, but the idea was already known in the 1970s. 3D integration using through vertical connections through each die using through-silicon vias, can be traced back to 1970s,[50] but intensive studies on wafer stacking and chip stacking started in the 1990s.[51] In the mid-1990s, 3D stacking technology using TSV became the subject of systematic investigation for CMOS devices.[52] For the first time, advances in deep silicon etch, wafer thinning, and bonding process technologies made it possible to achieve high-density packaging and high-speed signal transmission between chips.

The most promising application of TSV-based 3D IC technology may be the stacking of memory and logic devices. Several companies have asserted that stacking DRAM and NAND memories is technically viable.[53] At the end of 2011, a stacked DRAM device (hybrid memory cube) achieved a data rate as high as 128 GB/s, about 15 times faster than 2D devices.[54] Logic-on-memory devices combining field-programmable gate arrays (FPGAs) with memory are next in line for production.[55]

In addition to near term applications for mobile devices, the low energy consumption of 3D ICs enabled by short interconnects may drive adoption of the technology in stationary devices such as servers and desktop personal computers, with positive consequences for global energy consumption.

3D IC can be realized by monolithic approach, which fabricates devices layer by layer from bottom to top.[56–59] There is only one substrate, and all other layers are fabricated based on the substrate. After the devices on the substrate are fabricated, a second layer of silicon or other semiconductor film is grown on top of the first layer of devices by deposition or a thin layer may be attached using a method similar to that used in the silicon-on-insulator (SOI) process.[60]

Compared with other 3D IC approaches, monolithic 3D IC has the advantages of small interconnect via dimensions, high interconnect density, transistor-scale vertical interconnection lengths, relatively easy alignment between layers, and potentially low process cost. However, it is very challenging to create a sufficiently high quality upper film, make highly stable bottom field effect transistors (FETs), and find a process flow for making the upper layer of FETs with sufficiently low thermal budget so the bottom layer is not damaged. These challenges limit the application of monolithic 3D IC.

3D IC using TSV interconnect for stacked dies is the most promising way to pack multiple devices into a small form factor with ultra-fine pitch, short interconnects, and high I/O interfaces.

With increasing in IC speed and current, the distribution of stable power supply voltages and suppression of simultaneous switching noise (SSN) in the power supply network have become critical design issues. Conventional wire-bonding interconnections for power delivery networks can generate significant SSN above a frequency of a few hundred megahertz, due to large parasitic inductance.[61] A thorough comparison of bonding-wire and TSV interconnection showed that TSV interconnection for the 3D stacked chip package has significantly lower inductive interconnection impedance among chips, passives, and package substrates for signal, power, and return current path connections.[61]

There are three approaches to TSV die stacking: wafer-to-wafer, die-to-wafer, and die-to-die. Wafer to wafer has the highest throughput, but may have yield problems because a bad die may be attached to a good die, rendering the finished package useless. This problem worsens as more wafers are added to the stack. In contrast, the other two approaches (die-to-wafer and die-to-die) can test and discard bad die before stacking. Using only known good dies (KGD) increases yield and reliability. However, wafer-to-wafer is the prevalent technique currently owing to the higher throughput.[62]

3D IC design considerations

Design and tools

Designing an IC is an extremely complex process. At the die level, we can separate the design process into several key levels: electronic-system level design, logic design, circuit design, and physical design. To complete the device, we add the package and board design steps. All these designs are heavily dependent on electronic design aid (EDA) tools, making the availability of mature EDA tools determining factors in the commercialization of 3D ICs.

Currently available 3D IC design tools are "pseudo 3D" physical design tools, which are expected to be replaced in the near future by "native" 3D tools for maximizing the benefit from 3D IC. The key to 3D IC design is to develop tools for the complete hardware design flow, including high level logical design and verification, physical design and verification, and design for test (DFT).

The 3D IC design is new to semiconductor industry, but the design process can extrapolate best practices from current 2D IC design technologies to 3D IC design technologies: a set of specifications and a set of constraints. Many designs in development will take advantage of heterogeneous chip stacking, such as DRAM on logic IC, or analog on logic IC. The design for these types of products is similar to current 2D IC, but with the consideration of TSV alignment, heat dissipation, and stress management. Ultimately, the design of 3D ICs will be significantly different because a fully integrated and optimized multi-die 3D IC stack involves homogenous and/or heterogeneous partitioning.

Traditional IC system design includes critical steps such as logic design, circuit design, physical design, and packaging design with the help of EDA design tools and specific design methods. IC design begins with the creation of a functional specification, which can be described in variety of computer languages. The most difficulty is in the register-transfer level (RTL) design step, which converts the user specifications into a RTL description in hardware description languages (HDLs) to create a high-level representation of the circuit. Then, synthesis translates RTL description to the equivalent, lower-level, hardware implementation file. However, this does not involve 3D-specific requirements because the system partitioning is already completed at the system exploration level. All design components are instantiated with their geometric representations, so the new physical features and implementation of unconventional approaches in 3D stacking are quite disruptive, requiring new design tools for layout design, design for manufacturing (DFM), and DFT. Today, chip designers are forced to employ *ad hoc* methods for R&D.[55] In addition to 3D layout tools, 3D ICs need completely new tools to design and model power distribution network, clocks, I/Os, and electrostatic discharge (ESD) protection. Lastly, a new class of design management tools is required so that designers of each die are coordinating their efforts into a system design approach, i.e., chip-package-system co-design.

The 3D IC technology opens up multiple new degrees of freedom compared with 2D ICs. The communication between subsystems in 3D IC technologies is potentially "free" because of significant advantage provided by system partitioning. It will impact the architectural specification of every individual ICs used in the stack. These technologies have the capability to stack sub-systems fabricated by using different design nodes and substrate technologies. This new flexibility will ultimately reduce cost-per-function and raise performance.

System level exploration, also known as "path-finding," is a spatially aware design methodology to take a design concept from architecture level down to physical level. It involves the analysis of die sizes, wire length distributions, routing ability, and floor planning. These parameters affect feasibility, power, performance, and cost. Path-finding in 3D IC design will define the TSV process, stacking orientation, and stacking process. Gross thermal analysis is at the heart of system level exploration for 3D IC design, as discussed further in section "Temperature distribution and thermal stress."

Path-finding determines and optimizes primary 3D IC technology parameters such as TSV size, backside redistribution layer (BRDL) pitch and micro-bump size, based on die-to-die interconnect number, die sizes, interconnect levels, and placement restrictions. During path finding, the primary characteristics of the system (such as power, cost, and performance) are evaluated and determined.

For IC performance and stability, thermal and mechanical stress should be considered together. Silicon design, 3D stack and package designs, and process technologies are co-optimized in a simulation process known as "TechTuning." Thermo-mechanical considerations are new to the IC design practices, and thermal management is a key challenge that poses a significant barrier to integration of 3D ICs. Today, there is no commercial EDA tool that meets all of 3D IC design requirements.

Thermal and mechanical considerations must be included in the stack and chip design stage for 3D ICs as primary design parameters, compared with the current 2D IC approach that addresses them only at the package or board level of design. Managing thermal considerations is challenge for 3D IC designs because 3D integration results in a very intimate thermal interaction between multiple dies stacked in a single package.[63,64] Power dissipated on one die affects the temperature and the performance on the other die in the stack.

Similarly, mechanical stress is traditionally considered during a board or package level design for 2D ICs, but it becomes one of the principal considerations for 3D IC design.[65,66] Copper-filled TSV and die-to-die interactions introduce incremental and different sources of stress and stress interactions, which may affect stack mechanical integrity and cause cracking or fracturing. Therefore, the stress distribution for various stacking configurations should be included in the design analyses.

A primary 3D IC technology parameter is the diameter of the TSV because it determines the "keep-out zone," the area that the circuit board layout design cannot use due to thermal management, cooling, and mounting constraints. A small TSV is preferred due to the smaller keep-out zone and cost, but smaller diameter increases the aspect ratio and thus increases process cost. Thin wafers can decrease the TSV aspect ratio, but it is difficult to handle and thin wafers also cause challenges with stress management.

The 3D IC design has multiple choices for the interconnect process sequence: "via-first" means via formed before transistor device; "via-middle" after device before BEOL; and "via-last" after BOEL interconnect process (as shown in Figure 4). Other choices include face-to-face or face-to-back stacking; and Cu-to-Cu direct bonding or microbump bonding. These selections impact system performance and cost and should be explored during the high level design stage.

Size and pitch of the microbump is another important parameter for IC stacking using TSV. Small microbumps

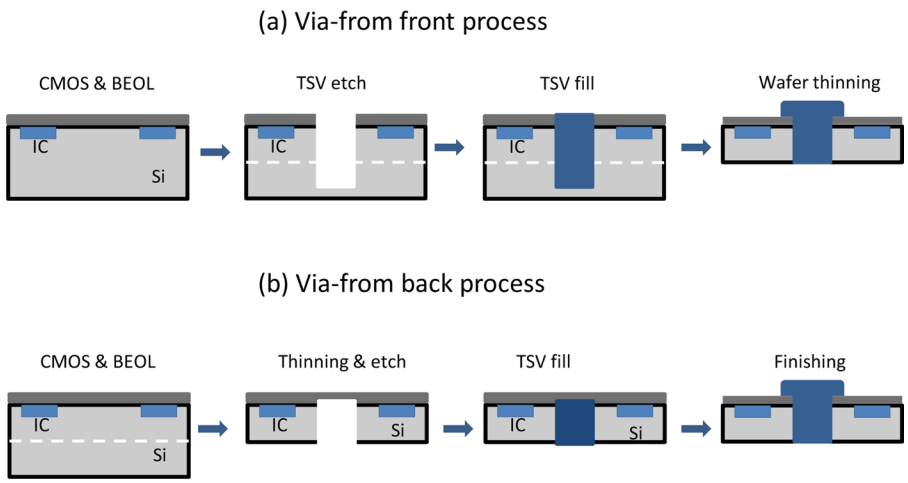

FIG. 4. Via-last integration approach.

allow high density die-to-die interconnects and enable short interconnects between the die, but small microbumps also need tight alignment and low warpage tolerances, resulting in high manufacturing cost and risk. BRDL pitch and the routing density obviously should be co-optimized with TSV and microbump size.

It should be mentioned that testing 3D IC stacks is a significant challenge because the functionality and various features of a given system may be distributed across multiple dies in different stacked layers and some die may not contain conventional test points for using traditional probe cards. Cost may be significantly high if testing is conducted on a finally completed 3D IC stack. Therefore, cost-effective test and associated DFT strategies need to be developed as part of the 3D IC design infrastructure.

Progress in design tools and strategies offered several approaches to test challenges recently. In order to effectively control the manufacturing costs, different levels of tests in fabrication processes should be conducted by using pre-bond test, mid-bond test, and post-bond test.[67,68] Pre-bond test targets classic logic of individual dies on the wafer level and unbounded TSVs; mid-bond targets partially assembled stacks; and post-bond test targets final circuit tests.

Among the different levels of tests, pre-test is difficult mainly due to the direct access to the not-connected tiny TSVs. In the last few years, several pre-bond test strategies were proposed such as built-in self test (BIST) structure,[67,69,70] scan switch network (SSN) structure,[71] and vertically addressed test structures (VATS).[72]

Design rules play a key role in the physical design of 3D ICs. The introduction of new design rules is necessary for 3D IC design.

Temperature distribution and thermal stresses

One of the biggest challenges in 3D IC stacking technology using TSV is thermal management owing to the high heat flux up to about 200 W/cm^2.[73] 3D IC structures have more heat flow paths and interfaces between die and heat sink than 2D IC, and heat must conduct through multiple layers in a 3D IC structure. The stacked structure adds insulating barriers impeding the removal of heat from the hottest die. As the power density levels increase, higher conductivity interconnect layers are required to remove dissipative heat.

For die-to-die interconnects, bumped die pads are usually used. The bonding method uses a solder bump and protective underfill layers between the two dies. The effective conductivity of the bump/underfill layer is much lower than silicon, which restricts the achievable power density for face-to-face TSV stacking applications to moderate levels.

Silicon normally acts as a good heat spreader when the wafer has moderate thickness, but thinned die decreases the ability of the die to dissipate heat laterally. Compounding the problem, the heat flux generated at hot spots is usually much higher than the average heat flux dissipated across the die. When the ratio of heat flux near hot spot to the average value across the die is higher than a threshold, thin die can no longer efficiently conduct the heat away from the hotspot due to large spreading resistance.

The separation distance between the hotspot and thermal via is critical for the hot spot and it must be considered in design. This distance and the TSV layout have a major impact on reducing junction temperatures. With the progress in EDA tools in the last few years, the temperature rise of 3D IC can be minimized by design path finding and partitioning.[74,75] It was proposed to manage dissipative heat using thermal aware floor plan and placement.[76]

However, thermal aware floorplan and placement may not be enough, which leads to the uses of signal and power network TSVs for thermal dissipation.[77] The thermal aware via farm technique, i.e., a cluster of TSVs used for signal bus connections between layers, was proposed to minimize the lateral thermal blockage effect due to the use of thinned wafers in 3D IC.[78]

Because of the challenges of thermal management, current 3D IC packages are limited to lower power applications such as memory devices and logic devices. For high power 3D IC packages, embedded thermal solutions were realized by circulating fluid inside the 3D IC package;[79] however, the realization may be very difficult. Integrated liquid cooling system for 3D IC stacked modules with high power dissipation was proposed for special applications such as small size, high power packages for defense systems.[80]

It was reported that independent interlayer microfluidic cooling for 3D IC is an effective way for thermal management due to the capability of power dissipation as high as 390 W.[81] However, current liquid cooling technology inevitably increases the stack thickness, resulting to the contrary of the TSV technology trend.[82] In addition, micro-channel based liquid cooling consumes a lot of extra power for pumping coolant through channels. Therefore, a hybrid 3D IC cooling system using micro-fluidic cooling and thermal TSVs was proposed to overcome the challenge.[83] This approach may solve the thermal management problem technologically, but increases the manufacturing complexity and costs, limiting the applications.

Because the TSVs make both mechanical and electrical connections between chips, thermal stress is a significant potential issue, and thus, thermo-mechanical analysis is necessary for evaluating the 3D IC stacking technologies.[84]

A major source of stress is from mismatches in CTE between via-filling materials and silicon. When it is used for filling via, the copper is attached to the next level die by means of thermo-compression bonding or other bonding methods. The thermo-compression bonding process applies force and temperature simultaneously on the copper-copper surface for bonding the metal together by inter-diffusion. After cooling down to room temperature, the large mismatch in CTE between copper ($17.5 \times 10^{-6}/°C$) and silicon ($2.5 \times 10^{-6}/°C$) makes copper contrast much faster than silicon, pulling the surrounding surface of silicon, and thus resulting in tensile stresses in the area.[85] The resulting stress may cause silicon fracture or delamination at the interface, resulting in electrical breakdown.

These mechanical loads also affect the carrier mobility, i.e., transistor performance through piezo-resistive effects, depending on temperature and the doping concentration.[65,66,86] Therefore, how far the active region (the transistors) is away from the copper vias is an important design consideration.[87] The size of this keep-out zone is proportional to the via diameter, and the bonding temperature is the main cause for the induced stresses during the thermo-compression bonding process. In this case, thinned die can reduce somewhat induced stresses,[87] but the stress introduced by lateral thermal blockage effect due to thinned silicon should be considered.

Detailed stress studies in recent years suggest that static (design-time) management of TSV thermal stress and load as mentioned above on keep-out zones be considered in thermal stress-aware TSV floorplan. In addition, run-time TSV stress analysis and management must be performed for effectively minimizing thermomechanical stress to neighbor devices.[88]

Signal integrity and power integrity

TSV interconnections have very small inductance, compared to long, within-die interconnects or wire bonds between die. This is very useful in a power distribution network (PDN) design because the impedance can be very low by sharing PDNs in 3D stacked chips.[89] This enhances both signal integrity (SI) and power integrity (PI) for TSV 3D IC compared with that of wire-bonded 3D chip. This effect is more pronounced in high frequency applications. However, if not designed properly, TSV capacitance could be a significant source of delay on 3D signal paths and add to the already deteriorating PDN. Ignoring TSV capacitance may lead to highly inaccurate estimation of wire length, delay, and power.[90,91]

As mentioned previously, heat flux density for TSV-based 3D IC increases dramatically because of stacked chips in z-direction, making electrical-thermal co-analysis essential for power delivery networks in 3D IC system integration, owing to the temperature-dependence of electrical resistivity of conductors.[92]

When using high clock frequencies and high transmission data rates, signal integrity is a concern in high speed designs used for TSV-based 3D IC integration.[93] In a 3D IC, the signal routing becomes much more complicated, and the high density interconnection increases the potential of signal integrity degradation, which may cause crosstalk and inter-symbol-interference (ISI).[94] Although small compared to wire-bonded packages, high frequency with short distance interconnections also has parasitic and transmission line effects, which may cause severe signal degradation due to reflection, distortion, and signal delays. All these possible issues should be considered during design.

TSV structure can be expressed using equivalent circuit for evaluation of electrical performance.[95–97] The equivalent TSV self-capacitance is an important parameter for RC delay, which needs to be considered during TSV design. The equivalent TSV inductance is also important for interconnect performance such as SSN that is determined by TSV length. Because they are frequency-dependent, DC and AC resistance should be considered separately for applications such as digital, RF, or power delivery.

Reduction of the parasitics associated with the TSV is critical to control signal propagation delay, which is reduced by using TSV dimension reduction, substrate thinning, and design optimization. Using a ground reference for the TSV can reduce self-capacitance and the noise induced on the signal propagation path and the inductive loop. Wafer thinning decreases the TSV length and then decreases RC delay.

3D IC process

TSV etch

TSV holes are formed by a high aspect ratio (HAR) silicon etch, also known as deep silicon etch, and high aspect ratio trench (HART) silicon etch. Plasma HAR silicon etch was developed for micro-electro-mechanical system (MEMS) in the late 1980s and 1990s. This technology has been improved for TSV etch for 3D IC stacking technology.

The time-multiplexed alternating process (shown in Figure 5), also known as the Botch process, is the most common method for TSV etch, which alternates sidewall passivation and etch steps.

Although etching completely through the silicon substrate is not required because a thinning step is used later, an etch depth of about 100 μm is generally required. TSV etch requires a high etch rate to enable high throughput, and smooth sidewalls ensure conformal depositions of insulator, barrier, and

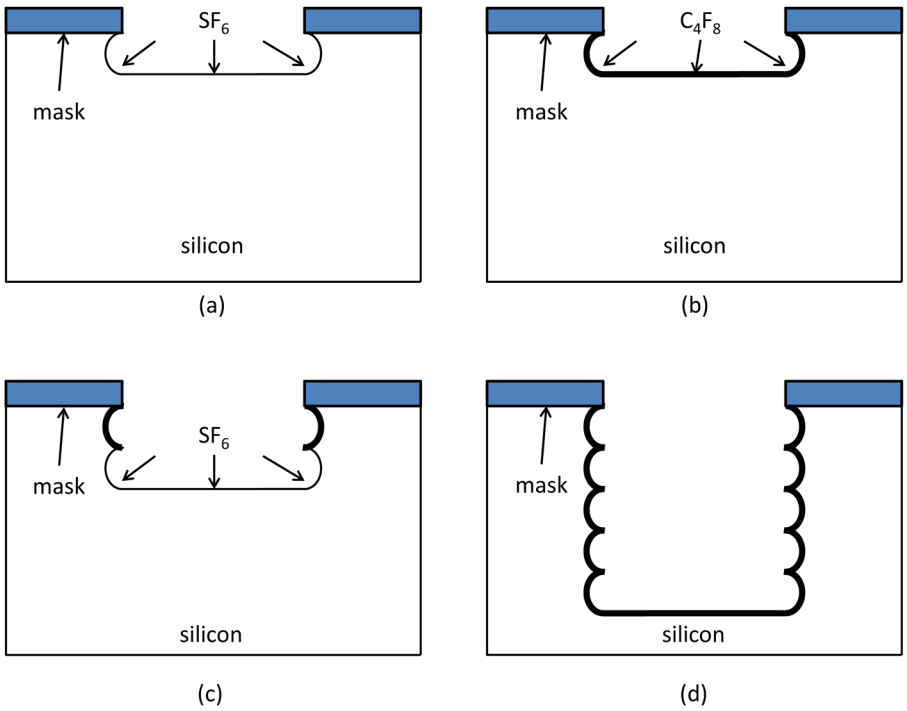

FIG. 5. TSV etch and profiles.

seed, as well as the optimal fill of conducting materials in conductor electro-deposition. For via-last process etching from the back side of a wafer after wafer thinning, placement error should be controlled well so that the via meets the conductor layer at the correct place on the front side.

The key challenges of TSV etch are to achieve high aspect ratio with smooth sidewall profiles, obtain high etch rate and selectivity, and control loading effects, aspect ratio dependent etching (ARDE), micrograss, tilting, and notching. Now, TSV etch technology can meet 3D IC process requirement.

TSV liner deposition

After TSV etch, the sidewalls are lined with dielectric film for electric insulation using chemical vapor deposition (CVD). This process is followed by barrier and seed layer deposition. The basic requirement of dielectric layering is good step coverage in a high aspect ratio via. Typical dielectric film thickness is in the range of 0.1–3.0 μm.

For the dominant via-middle and via-last processes, the dielectric film (e.g., silicon oxide) is deposited after the transistors are formed, which requires that the process temperature for dielectric film should be low enough to avoid damaging the structures. For the via-middle process, the temperature is in the range of 450 °C–550 °C or lower. However, for the via-last process, the completion of devices requires even lower temperature for dielectric deposition, 200–400 °C, in order to keep the required material properties of interconnect layers such as copper, low-k dielectric, and the adhesive used for bonding wafer to a support carrier. In contrast, the via-first process has virtually no temperature limit for dielectric deposition (e.g., up to 1000 °C). That means high temperature oxide or a silicon nitride CVD process can be used to form the dielectric layer.

Sub-atmospheric chemical vapor deposition (SACVD) and plasma enhanced chemical vapor deposition (PECVD) methods are the most suitable candidates for depositing TSV dielectric liner films because SACVD can be used at approximately 400 °C for the via-middle TSV process and PECVD at 200 °C or below for the via-last process.

The conductor seed material should be the same as that used for the final via fill. Common materials are copper, tungsten, and polysilicon. Because copper can diffuse easily into the underlying dielectric layer, a barrier layer must be used to prevent the diffusion. Due to its very low electric resistivity, copper is a very good TSV material.

Common for adhesion/barrier layers for copper are TaN/Ta and Ti/TiN bi-layer in order to prevent copper diffusion while TaN can improve the adhesion.

Barrier and seed layers for TSV applications can be formed by several methods, among which PVD is the most promising because of its high purity of deposition layer and low costs. A key challenge for PVD method for TSV applications is to achieve high conformality.

CVD processes may also be considered for barrier and seed layer deposition because the very low sticking coefficient leads to very good conformality. However, CVD films usually have more impurities than PVD films, resulting in higher resistivity. In addition, CVD films are less dense than those formed by the PVD process, because metal atoms arriving at the substrate have a higher energy in a PVD process than the precursor molecules in a CVD process. Besides the film properties, the cost of CVD processes is typically higher than PVD. The combination of film purity, resistance, density, and costs determines that the PVD method is preferred to CVD for the deposition of barrier and seed layers.

TSV filling

Electroplating, also known as electrodeposition or electrochemical deposition (ECD), is the preferred process for the bulk fill of TSVs because of the low costs.

Although several materials have been proposed, superior electrical properties, such as high conductivity and relatively low electromigration compared to aluminum make copper the most common material for TSV applications.[98,99] Copper electroplating requires a seed layer on the TSV bottom and sidewall to achieve a complete fill.

ECD in an aqueous system is a superconformal or bottom-up deposition process capable of void-free via fill for TSV applications.[100] Bottom-up deposition is a special property, as shown in Figure 6, which deposits material at the bottom of the features at higher rates than at via mouth or on the top field area of the wafer.[101]

A true bottom-up growth deposition technique is suitable for TSV filling.[101] This process uses organics additives to suppress the deposition at the top of the via, which makes the deposition faster at the bottom of the via due to the low concentration of the suppressive organics.

Plating solution composition plays a very critical role in deposition quality. Costs of ECD as well as the pre- and post-ECD steps are important process considerations. High barrier and seed layer quality is vital to prevent voids in copper plating, and copper overburden significantly influences the downstream planarization cost.

TSV chemical mechanical planarization

Wafer bonding requires a high flatness of a wafer surface, so chemical mechanical planarization, or polishing (CMP) is used for surface planarization.

Both performance and costs are related to CMP material removal rate.[102] That rate depends on pressure on the wafer, the wafer motion velocity relative to the pad, material properties, and slurry composition.

For TSV applications, topography on the wafer surface mainly results from the copper plating. Over polishing, where polishing continues even after some areas are clear, is necessary to clear copper residue completely, but it causes undesirable recessing of the copper at the barrier and dielectric interface, i.e., dishing. Dishing mainly results from different slurry wet-etching rates between different materials on the wafer, physical gouging from slurry particles, and pad deformation.

In addition to planarization, CMP is also used in the via-middle and via-last schemes to make the TSV tips, known as "studs" protrude above the silicon surface. This process is called "via reveal." For good electrical connection between TSVs when different die are stacked, it is vital that all the stud ends should lie in the same plane. Achieving the necessary uniformity is a particular challenge because the planarization rate of the studs is highly dependent on the via density.

CMP is a critical process for all TSV integration schemes. Cost of ownership is an important requirement. Backside via reveal requires CMP to remove silicon and copper to expose the copper vias. For the via-first or via-middle schemes, CMP is used to planarize the dielectric passivation film and copper pillars.

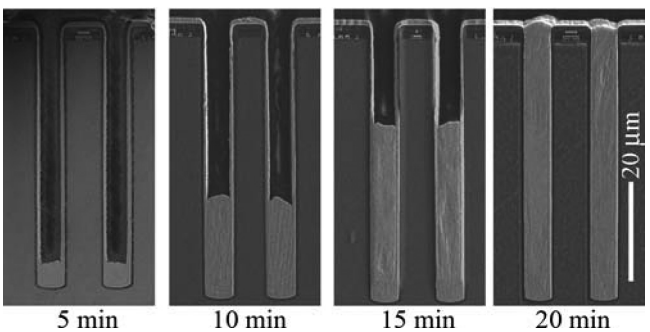

FIG. 6. Bottom-up copper electroplating. Reproduced by permission from T. P. Moffat and D. Josell, "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns," J. Electrochem. Soc. **159**, D208 (2012). Copyright 2012 by The Electrochemical Society.[101]

Wafer bonding and thinning

The main functions of wafer bonding in TSV processing are mechanical adhesion, electric conduction, heat transfer between chips, and to temporary hold wafers for processes such as film deposition, wafer thinning, and CMP. Common bonding techniques are thermo-compression metal bonding for electric and heat conductivity, low temperature direct fusion bonding, and polymer adhesive bonding (Figure 7).[103]

The high I/O count between chips requires the reduction of bump pitches and bump sizes, which influences the bonding method for TSV integration.

Direct copper-copper bonding is a promising candidate due to the good bonding strength and conductivity for wafer-to-wafer interconnection, but it requires a relatively long process time, high temperature, and high pressure. Compared with direct copper-copper bonding, molten solder bonding requires less time and low temperature, so it remains the most widely used for TSV interconnection. Cu–Sn eutectic bonding falls somewhere in between direct copper–copper bonding and solder bonding.

Recent progress on low-temperature copper–copper direct bonding shows that diamond-cut copper bumps can be bonded at temperatures of 150–200 °C and pressure of 200 MPa for 30 min.[104] The capability for low temperature bonding is very significant for relaxing the thermal stress introduced by a CTE mismatch of copper and silicon.

Temporary bonding and de-bonding technology is required for wafer handling and processing. When all the backside processes are completed, the device wafer will be released, or de-bonded, from the carrier wafer, for final packaging.

De-bonding of adhesives can be accomplished by chemical release, thermal release, and UV release mechanisms. A thermal de-bonding process is usually used to separate the wafer stack, followed by cleaning and unloading to the film frame, a specially designed thinned wafer holder.

A wafer thinning process reduces a full thickness (e.g., 775 μm) wafer down to 30–150 μm after it is bonded to a temporary carrier. The basic requirements of this process are to achieve thickness uniformity less than 1 μm and leave a smooth silicon surface less than 1 nm RMS, free of silicon residue and defects or contaminants without breakage or cracking the edge of the wafer.

The most common wafer thinning method is mechanical grinding using wet slurry. Other methods include CMP, wet

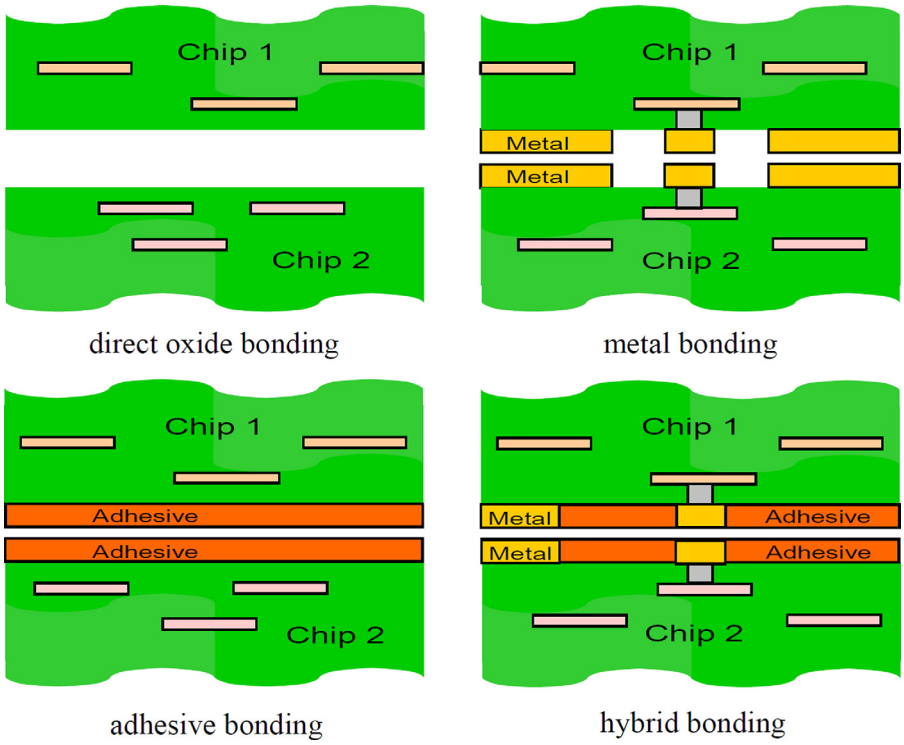

FIG. 7. Bonding methods suitable for TSV integration. Reproduced by permission from B. Kim *et al.*, "Advanced wafer bonding solutions for TSV integration with thin wafers," IEEE International Conference on 3D System Integration, San Francisco, California, USA, 28–30 September 2009, pp. 1–6. Copyright 2009 by IEEE.[103]

etching, and dry etch, but they are more expensive than grinding.

Once thinning is completed, a blanket silicon nitride film is deposited using a low-temperature CVD process to protect the back of the wafer.

Summary of 3D IC

3D IC devices will improve performance and enable new applications enabled by changing design strategy, IC structure and partitioning, form factor, functional diversification, and costs. 3D IC fabrication mostly relies on wafer fab technology rather than progress of a traditional packaging method. This infrastructure requirement change may cause consolidation among wafer fab and packaging houses.

Now, there are no critical challenges for IC stacking processes, but the realization of 3D IC depends on the availability of a design tool, management of heat and stress, and method of testing.

DISCUSSION

Processor performance and challenges

The geometric shrinking enabled by lithography reduces transistor gate length and hence transistor switching time. Before 2000, processor performance was improved by about 60% every year in terms of instruction throughput, which was enabled by the increase in transistor density and by linear scaling with a processor clock.[105]

When EUVL was proposed in 1988, the approach to improve IC performance was very straightforward. That process was to increase device density and clock rate, reduce gate delay, and thus increase instruction completion rate by using advanced lithography. By that time, lithography seemed the only way to improve IC performance. Since then, research and development were focused on the concept proving and realization of EUVL.

However, the chip performance and its determination factors have changed in last 25 years. Improvement on processor rate has been much faster than that on memory access rate in last several decades, which built up the memory wall and thus slowed down the rate of performance improvement.

When IC feature size shrank to below 45 nm, short-channel effect (SCE) became significant, which increased leaking current and power consumption significantly, causing the saturation of clock rate.

Scaling improved the IC performance, but also increased the complexity due to smaller interconnect lines, which, however, made interconnect delay pass the gate delay and thus become a critical delay after the turn of the century, as shown in Figure 8.[106]

In addition, market demands for functional diversification have changed dramatically. Revolutionary applications of mobile devices such as smartphone and tablet computer have driven the semiconductor industry towards low power consumption, small form factor, and more functions.

All these changes and new requirements have challenged lithographic ability to effectively improve performance. It has become questionable if conventional, two-dimensional, device shrinking alone will be able to enhance the performance further because of interconnect delay and latency issues. This "wiring crisis," as called by ITRS, is significant for 32 nm node and beyond.

Therefore, focus is turned to 3D IC technology using TSV stacking to solve these problems. 3D ICs can be realized by using TSV, edge wiring, silicon carrier, flip-chip-on-chip, and interposer. Among all these approaches, 3D stacking using wafer-to-wafer TSVs is the most promising method in the future for volume production.

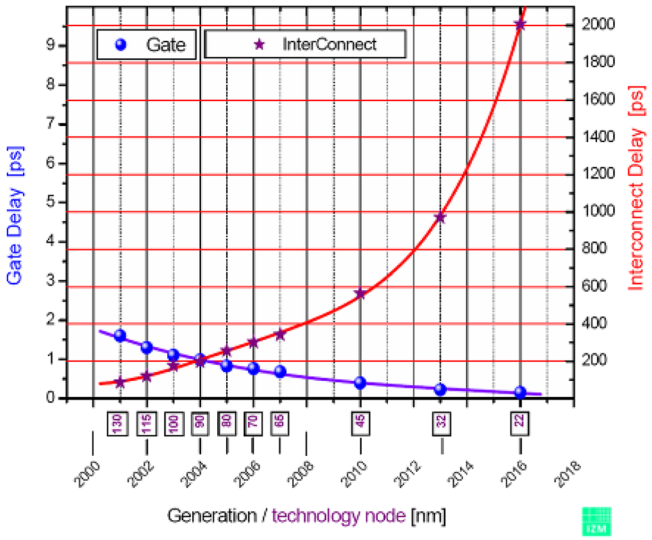

FIG. 8. Gate delay versus interconnect delay. Reproduced by permission from 3DIC & TSV Report—Cost, Technologies & Market, Yole Development, Lyon, France, November 2007. Copyright 2007 by Yole Development.[106]

The speed mismatch between the microprocessor unit (MPU) and discrete memory chips has resulted in the use of on-chip memory (cache) to improve the chip performance. On-chip cache memory is now a key determinant of processing speed and large on-chip caches have become commonplace. However, on-chip cache memory is no longer sufficient to achieve high performance because the resistance-capacitance (RC) delay of interconnects that communicate across a large fraction of the die is now a performance bottleneck.

One approach for relieving these interconnecting constraints is the use of wafer-level 3D IC stacking with TSVs to supply high density vertical interconnects. This technique reduces the length of many global interconnects without introducing any logic complexity. It also reduces the required number of repeaters—additional circuits which boost signal strength over long distances. This improves area efficiency and reduces the power consumed within the interconnect network. It also allows a large memory bandwidth with little chip area consumption.

Ultimately, 3D IC technology will improve IC performance from the fundamentals, i.e., changing of rules of design, by repartitioning IC into multiple chips for optimal system functionality.[53]

Multicore and multithreading

The fast microprocessor and slow memory access rate cause the mismatch of the rate, i.e., the memory wall. It causes complex MPU idle to wait for slow memory. In order to overcome this bottleneck, the multicore concept was proposed in 2001, which suggests using multiple simpler cores to replace one complicated core to improve IC performance.[107] For example, a two core processer doubles the computation capability of a chip. However, since the two core processer supports two programs running simultaneously, it needs nearly twice the off-chip bandwidth and twice the on-chip cache capacity of a single core chip.

Another technology to improve IC performance is the multithreading technology by which each core can run multiple programs (e.g., two programs) simultaneously, but it requires extra off-chip bandwidth and on-chip caches.

The applications of multicore and multithreading technologies significantly improved IC performance without increasing clock rate since 2001. However, these technologies introduced challenges on large cache memory, high off-chip bandwidth, and high interconnect delays. Fortunately, 3D IC technology is able to provide approaches to solve these problems.

EUVL applications

When EUVL was originally proposed, it was targeted as a total solution for IC performance improvement. The technological complexity and challenges let us think about the scaling of different devices using specific approaches. Three main devices are logic (e.g., MPU), DRAM, and flash memory (e.g., NAND).

According to ITRS 2011, NAND flash memory might be scaled down to 16 nm using extension of 193 nm ArF lithography combined with immersion and multiple patterning. Progress on 3D flash memory processing helped the performance improvement without using EUVL for 1× nm nodes.

Recently released Intel MPU is manufactured by 22 nm technology using extension of optical lithography. It is predicted that 16 nm MPU will be made using 193 nm exposure wavelength, too. The potential extensions of optical lithography down to 16 nm for MPU and NAND flash memory ICs strongly impact the applications and market size of EUVL, which may influence the resources and investment in EUVL.

Among these three types of devices, DRAM is the most difficult for scaling because of the dense patterns. Now, 32-nm technologies can be used for DRAM production using 193-nm lithography. It may have an extension to another half technology node, i.e., down to 28 nm. However, it is almost impossible to extend optical lithography to 1× nm node for DRAM manufacturing. Therefore, EUVL was believed to be the main candidate for further DRAM scaling in the last few years.

Recent progress in 3D IC technology resulted in the emergence of a hybrid memory cube.[54] HMC has much higher access rate than traditional DDR3 DRAMs, which determines in the near future that 3D IC technology will be the more effective method for DRAM performance improvement than EUVL.

3D IC technology increases both DRAM density and access rate, which makes EUVL not as important to DRAM as before, resulting in the possible loss of EUVL application in DRAM. It seems that EUVL has the risk to lose applications in the near future, although it might be an approach to improve IC performance for longer term considerations.

3D IC and its impact

3D IC enables improvements in form factor, interconnect rate, memory access rate, energy consumption, functional diversification, functional block partitioning, design strategy,

and IC system functions. It is a game-changing technology and will have a revolutionary impact on computer systems. Compared with influence of EUVL on IC system via device performance improvement, 3D IC technology impacts the IC system function by design and system integration.

After the turn of the century, multicores and multithreading technologies were applied to improve IC system performance by reducing the rate mismatch. However, memory wall still exists.

Progress in 3D IC provides a solution to break the memory wall by increasing the DRAM access rate enabled by stacking technology, and thus reducing cache memory.

The increase in DRAM access rate in 3D IC will result in the removal of some cache memories (e.g., L3, L2, and maybe L1.5), and/or rearrangement of cache memories in different dies. This capability makes us to reconsider the necessity of current 26×33 mm^2 die dimension. The die size shrinkage may cause a high production yield, which might compensate some of the costs introduced by 3D stacking processes.

3D IC technology stacks MPU and DRAM memory, resulting in removal of off-chip bus connection between them. Due to the slow rate and high energy consumption of the off-chip buses, the removal of them will save power, increase bandwidth, and improve reliability.

3D heterogeneous integration can stack silicon and compound semiconductor ICs together to make a special advantage, which, however, cannot be enabled by lithographic progress. In addition, 3D IC can be extended to the stacking of IC, passives, rf, image sensor, and even MEMS together, resulting in a very strong capability of a IC package.

The best scenario of the semiconductor industry is the realization of both EUVL and 3D IC in the next five years. If this dream comes true, 3D IC enhanced with EUVL will have a revolutionary improvement on system performance.

EUVL is expected to improve chip performance from the historical point of view in terms of device density and performance. However, 3D IC alternatively provides another approach, which not only increases transistor count and improves performance but also provides extra benefits such as reduction of interconnect and energy consumption, increases in functional diversification, and lots of design flexibility.

World economy will determine if the semiconductor industry and big companies will have enough resources and investments to continue developing both technologies simultaneously. It might be necessary to mark their priority levels and collaborate among EUVL and 3D IC teams, industrial consortia, and professional societies for improvement of the IC system performance.

CONCLUSIONS

Both EUVL and 3D IC technologies are important to the semiconductor industry because of their capability to improve chip performance. However, both technologies have multiple challenges for their realization in volume production.

There are three critical challenges on EUVL, i.e., EUV source power, resist RLS, and qualified photomask. Progresses on these challenges are reported every year, but several more years are needed to adopt this technology to overcome the challenges before volume production can be realized.

The main challenges of 3D ICs are the lack of a design tool, management of heat and stress, and control of yield and costs. Although the adoption schedule was postponed again, a volume production of 3D IC in the next few years is expected.

When EUVL was proposed in 1988, performance of ICs, especially MPUs, was improved every year by lithographic scaling. In 1990s, EUVL and other NGLs competed very intensively in order to technologically dominate the semiconductor industry. Device density and clock rate increased every year; however, performance improvement of MPU was much faster than that of DRAM access rate, resulting in memory wall. In addition, smaller interconnect dimension and complexity due to scaling made the interconnect delay much longer than gate delay now.

After 2000, IC scaling introduced a short channel effect and significant current leakage, which saturated the clock rate and thus slowed down performance improvement. Since then, chip performance improvement has been enabled by not only lithographic scaling, but also the adoption of multicore and multithreading approaches.

Now, immersion and multiple patterning approaches push optical lithography down to below 20 nm in the feature size of MPU and flash memory, reducing the manufacturers' dependence on EUVL. However, it is more difficult for DRAM scaling using an extension of optical lithography. Recent progress on 3D IC increased the DRAM access rate and density dramatically, relaxing the dependence of DRAM manufacturing on EUVL.

Progress on 3D IC technology enables performance improvement in terms of memory walls, interconnect delay, device density, form factor, energy consumption, and functional diversification, which open many channels for IC designers. All this progress makes EUVL lose momentum.

The best scenario is the adoption of both EUVL and 3D IC technologies in the next few years. However, the true reality will depend on technology progress, costs, and marketing needs.

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