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Characterisation of electrically active defects

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Defects may arise in the semiconductor substrate and at interfaces due to the processing used to fabricate transistors and circuits. The development of low-thermal-budget processes, which is advantageous in many ways, unfortunately reduces the likelihood of annealing out these electrically active defects. Electrical characterisation using simple diode structures yields valuable information; not only the absolute leakage current density value, but also carrier lifetimes, leakage activation energies, and diode ideality factor. Coupled with material analysis techniques, they can provide a detailed picture of the problems associated with process-induced defects, and supply insight that can target optimised processes. In this paper the technological relevance of electrically active defects, their impact on device performance and power supplies, as well as their electrical and material characterisation, will be discussed.

1 Introduction

1.1 Markets and applications

With the enormous modern-day increase in use of handheld electronic devices, power consumption and carbon-footprint concerns are escalating. With the worries over climate change, the next Information and Communication Technology (ICT) impact on society may be driven by environmental considerations and the need to reduce energy consumption.

One estimate has ICT consuming 5% of the world's energy resources [1], while another source has ICT estimated to consume about 6-10% of the world's energy resources and is responsible for 2-3% of worldwide greenhouse gas emissions, which is similar to the aviation industry emissions level [2].

So what is sucking up all that energy? The International Telecommunication Union has estimated that there are 6.8 billion mobile device subscriptions globally [3], equivalent to approximately 96% of the world population. To put that in perspective an average smartphone is ~10.5 cm long × 6.8×10^9 = 7.14×10^5 km, while the distance to moon = 385000 km = 3.85×10^5 km. In other words, if placed end-to-end, there are enough mobile personal devices to stretch to the moon and almost back. This market growth is largely being driven by demand in the developing world. With the escalating popularity and penetration of mobile electronic devices in the modern world, tomorrow's mobile applications will need to combine low cost, high performance, low power, and small carbon footprint.

Furthermore Gartner reports that more than 1 billion PCs are in use worldwide and headed to 2 billion PCs by 2014 [4]. Depending on the choice of Intel Core iX (most modern) microprocessor and clock speed, the power dissipation is as high as 130 W. Compare that to the original Intel Pentium from the early 1990s which had power dissipation in the 8-16 W range for desktop applications [5]. The importance of power scaling is also illustrated by the power demand of the high-end processors used in data centres and servers, as their worldwide power consumption increased ~56% between 2005 and 2010 [6].

Consequently, the potential impact of energy-efficient ICT solutions is huge. Power consumption control for handheld devices and other mobile ICT systems is the fastest, cheapest and cleanest way to address energy resource issues. Making these energy-thirsty devices more efficient through scaling transistor power consumption will directly reduce the global demand for energy.

A major portion of semiconductor device production is devoted to digital logic where the key considerations are speed, power and density requirements. Thermal power dissipation in a microprocessor is characterised by

$$P=C.V_{DD}^{2}.f \quad (1)$$

where P is power, C is capacitance, V_{DD} is power supply voltage, and f is clock frequency. Furthermore off-state leakage currents in metal-oxide-semiconductor (MOS) devices are undesirable as they drain power supply resources in integrated circuits and systems. Nobody wants a mobile device, such as a smartphone or tablet PC, that discharges it's battery too quickly, especially when it's in standby mode.

In summary identifying and characterising sources of leakage (i.e. power drain) are critical elements in the semiconductor device optimisation process.

1.2 So, what's the problem?

A highly challenging area of front-end processing is the optimisation of the thermal annealing and diffusion of dopants, and especially on electrical activation and deactivation. Due to the strongly reduced thermal budgets needed for scaled devices, these processes are highly transient and are governed by the diffusion and reaction of dopant atoms and defects, and especially by the cluster dynamics of these two. An additional aspect to be considered is the formation of defect clusters in the space charge regions of pn junctions. Such clusters, comprising intrinsic point defects, dopants and co-implanted species, may introduce levels in the band gap and cause detrimental leakage currents.

Ion implantation is the most common approach to introduce dopant impurities into a semiconductor material. These highly energetic ions damage the target semiconductor material as they strike it, impinging on target atoms and displacing many of them from lattice positions in the crystalline matrix. If the concentration of these events is high enough, the crystalline structure of the target is broken down, and it is amorphised. Amorphous silicon is considered to be a continuous random network with short range order (i.e. it appears to be crystalline), but it lacks the long range periodicity of a crystal.

Heating amorphous silicon via thermal annealing triggers a process known as recrystallisation. This tendency is related to the fact that the free energy of crystalline silicon is lower than the amorphous state, due to more disordered atom arrangements and distorted bonds in the latter. Distorted bonds, in terms of length and angle, are thermodynamically less stable than regularly arranged bonds, as a result there is a driving force for the atoms to rear-range themselves into the form of a regular crystal.

A significant factor to consider when operating under amorphisation and recrystallisation conditions is the region of damaged silicon just beyond the amorphous-crystalline (a/c) interface. This region was damaged during implant, but not to a high enough level to transform to amorphous material. As the recrystallised amorphous silicon region regrows essentially defect-free, there exists a buried layer of damaged silicon after recrystallisation is completed, rich in point defects. The annealing of such damaged regions proceeds with the formation of a hierarchy of defect structures. Simple point defects may agglomerate and form larger extended defects, typically rich in silicon interstitials, such as line defects known as {311}s, and agglomerate further to form larger disc-shaped defects known as dislocation loops. These {311}s and dislocation loops are problematic for technology applications as they act as reservoirs of interstitials and can locally enhance point defect populations and ultimately lead to unwanted effects such as transient-enhanced-diffusion and diode leakage. These defects do anneal out with high thermal budget anneals and with surface proximity.

Note the analysis of leakage in diodes and reverse biased junctions is often discussed with respect to advanced MOS technology. However much of the physics and dialogue are also applicable to other devices and technologies that may incorporate unintentional crystal defects, such as solar cells, image sensors, photonics, and photodetectors.

1.3 Characterisation of leakage mechanisms

Definitions of leakage mechanisms can be found in detail in many Si technology textbooks, and the summary here is intended to be a quick reference. Further details can be found in refs [7,8].

Generation mechanisms that lead to leakage currents are temperature and/or electric field (E_{FIELD}) dependent. To extract the dominant mechanisms we need to analyse: (a) the voltage dependence and (b) the temperature dependence of the leakage current. The temperature dependence of various leakage mechanisms is shown in Fig. 1. E_A signifies activation energy, and E_G signifies semiconductor band gap.

Current mechanism	Characterised by
Diffusion	$E_A \sim E_G$
SRH	$E_A \sim E_G/2$, Current is $V^{½}$ dependent
TAT	$E_A \sim E_G/2$, Current not $V^{½}$ dependent
BBT	$E_A \sim 0$

Figure 1 Temperature dependence characteristics of the important reverse bias leakage mechanisms.

Ideal diffusion current is proportional to n_i^2, where n_i is the intrinsic carrier concentration. Shockley Read Hall (SRH) generation is temperature dependent and relies on the presence of deep levels in the depletion region. SRH dominated current is proportional to the width of the depletion region and thus proportional to $V^{0.5}$, assuming a one-

sided step junction. Trap-Assisted Tunnelling (TAT) can be considered as SRH in the presence of an E_{FIELD}, or as a combination of electron capture and tunnelling through the barrier. TAT voltage dependence is V^x, where x is greater than 0.5. Band to Band Tunnelling (BBT) occurs when the E_{FIELD} across the junction is strong enough to propel a carrier from the valence band through the band gap, into the conduction band on the other side.

Note there is an entire field of work devoted to the study and characterisation of *interface defects* located at the gate dielectric-substrate and gate dielectric-gate electrode interfaces. Hurley *et al*. wrote a review of this area recently [9], and this is a good starting point for those readers interested in that topic.

2 Experimental

2.1 Methodology and process flow

The added value of our approach lies in the innovative way we link the experimental work with the simulations, as shown schematically in Fig. 2(a). Electrical measurements were first performed on fabricated diodes of different sizes and perimeters, with different doping profiles, and with different levels of process induced damage. After electrical characterisation, the fabricated diodes were subjected to a deprocessing step where the contact metallisation was removed, so that secondary ion mass spectrometry (SIMS) analysis could extract the doping profiles from the structures that were measured electrically. The resulting doping profiles were then used as input into a well-established simulation tool (MEDICI) to enable a closer evaluation of the measurements.

This body of work incorporated a large number of experiments over several years, but we will focus on a subset in this paper. The diodes fabricated consisted of

a) n+/p diodes with arsenic/boron doping,
b) n+/p diodes with arsenic/boron doping and with intentional end-of-range (EOR) defects located close to the metallurgical junction,
c) p+/n diodes with boron/arsenic doping,
d) p+/n diodes with boron/phosphorus doping.

In this paper we will concentrate on the subset (b).

A simple process was used to fabricate the diodes with relatively deep junctions. The diode cross-section is shown schematically in Fig. 2(b). During the metallisation removal, the silicon surface was expected to be roughened, which may lead to inaccuracies in the SIMS analysis close to the surface. To ensure accurate SIMS profiling at the metallurgical junction, a junction depth of >150 nm was targeted. The process flow consisted of standard processing to define the active area and poly-buffered LOCOS isolation on (100) oriented 200 mm Czochralski silicon wafers. A 5 nm screen oxide was deposited before the implants and anneals.

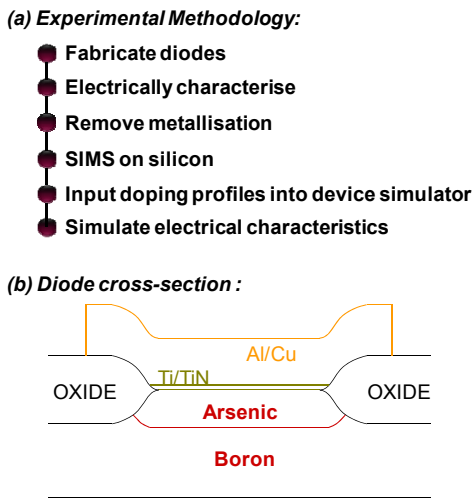

Figure 2 (a) Methodology of the diode study, and (b) a schematic cross-section of the diodes in this work. Note the choice of dopant was varied.

For the n+/p diodes with intentional EOR defects, high-concentrations of As (1×10^{15} cm^{-2} 10 keV and 4×10^{15} cm^{-2} 180 keV) and low-concentrations of B (2.0×10^{13} cm^{-2} 100 keV) were implanted into a preamorphised layer formed by high dose Si implants. The rest of the flow consisted of an 1100 °C 0 s spike anneal to activate the dopants, an etch step to remove the screen oxide, and the deposition of a Ti/TiN contact layer. Finally a 650 nm layer of AlCu metal was deposited and patterned.

Process details of the n+/p and p+/n diodes without intentional defects, can be found elsewhere [7, 8].

Current-voltage characteristics were measured using a HP4155 parameter analyzer. A thermochuck was used to investigate temperature dependency. For each structure and split, several die were measured. The within wafer reproducibility of the measurements was good, as there was little spread from die to die. Most of the measurements were done on large area square diodes. For completeness perimeter current was extracted from meander structures. In all square diodes the perimeter component was several orders of magnitude lower than the area contribution.

After electrical characterisation of the diodes, the contact metallisation was removed by using a standard Al etch followed by a standard Ti etch. Impurity profiles were then determined by SIMS analysis using 3 keV O_2+ primary ions. TEM cross-section and plan-view samples were prepared by mechanical polishing down to electron transparency. The TEM studies were performed on a FEI Tecnai F30ST TEM operated at 300 kV. Off-axis diffraction contrast imaging was performed with a tilt of 1.5º. The local thickness of the TEM sample was determined using energy filtered TEM.

On selected samples, transmission mode Fourier Transform Infra-Red (FTIR) spectra were obtained by averaging 64 scans taken on a Bio-Rad QS-300 FTIR system

equipped with a cesium iodide beam splitter and a compressed air purge. The spectral range is 220–4000 cm^{-1}, with a standard nominal spectral resolution of 2 cm^{-1}. Each spectrum has been corrected for baseline and background absorption.

2.2 Naming convention

As there are quite a number of different diodes in this work, it is worthwhile to explain the naming convention.

"*AB*" denotes a diode with Arsenic (high-concentration) and Boron (low-concentration) doping, thus is an n+/p diode. These diodes are numbered AB1-AB5 with the boron concentration as the only variable. AB1 has the highest B concentration, and AB5 has the lowest [7,8].

"*ABD*" denotes a diode Arsenic (high-concentration) and Boron (low-concentration) doping with intentional end-of-range Defects.

For simplicity, in some graphs diodes are labelled according to their doping type, e.g. "*As/B*" denotes a diode with Arsenic (high-concentration) and Boron (low-concentration) doping, while "*B/P*" denotes a diode with Boron (high-concentration) and Phosphorus (low-concentration) doping.

Note, the concept ''background concentration" discussed in our diode experiments, is analogous to the channel doping concentrations in a MOS device.

3 Results and discussion

3.1 The trouble with intentional (EOR) defects

Diodes with intentional EOR defects are characterised in this section to show the dependency of leakage on residual process induced defects. Leakage has been studied in the presence of intentional EOR defects by other groups in the past, and Ref. [7] has a literature summary of that.

The novelty in our study is that the doping profiles were extracted by SIMS analysis from the structures that were measured electrically. Studying the defect contribution is complicated if the doping profile of the junction is not extracted. Changing the type or position of an EOR defect band will inevitably change the shape and/or slope of the doping profile at the junction. By extracting the profile, the doping contribution to leakage can be filtered out to more accurately quantify the defect contribution. The experimental variable here is the location of the EOR defect band. This variation was achieved by changing the preamorphising Si implant energy. The arsenic and boron doping implants were kept constant in this investigation.

In our work we used amorphising implants to create EOR defects, however, it should be noted that extended defects can also be formed from non-amorphising conditions, which could affect leakage in a similar way

The diodes in this section are labelled ABD1, ABD2, and ABD3, according to the variation in position of the EOR defect band. Diode ABD1 has the defect band closest to the surface, diode ABD3 has the defect band farthest from the surface. Figure 3 shows the SIMS profiles for these diodes. The relatively bumpy nature of the boron profiles is related to the different positions of the silicon interstitial defects. Boron is known to collect in these defect bands.

In Fig. 4, two representative images of diode ABD1 are shown. One is XTEM, the other is plan-view TEM. A band of dislocations is visible at a depth of 236 nm. The width of this band is roughly 50 nm. The defect density in the plane perpendicular to the field of view of the plan-view TEM image was determined to be 2.5×10^{2} μm^{-2}. Also in Fig. 4 a representative image from diode ABD2 is shown. A band of dislocations is visible at a depth of 373 nm, with a width of roughly 80 nm. Comparing the images of diode ABD1 and ABD2 it seems that the EOR defect density is considerably higher for diode ABD2. However, this is due to the thickness in TEM sample. After correction for the sample thickness, the defect densities of the two diodes are comparable. The defect density at the projected range was determined from plan-view TEM to be 3.0×10^{2} μm^{-2} in ABD2. Additionally, threading dislocations (hairpin defects) are visible in the regrown layer. The density of these defects determined from XTEM is 3 ± 2 μm^{-1}. For diode ABD3 a band of dislocations is visible at a depth of 452 nm, the width of this band is roughly 90 nm. Threading dislocations are again visible in the regrown layer. The density of these defects is 6 ± 2 μm^{-1}. The defect density at the projected range could not be determined due to overlap of the two different defect types in the projected image.

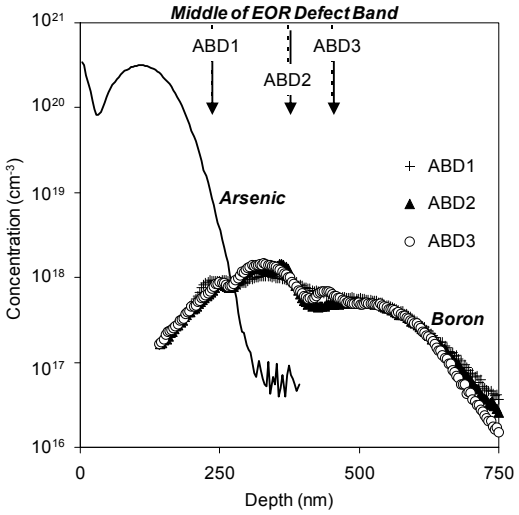

Figure 3 SIMS depth profiles of arsenic and boron for the diodes ABD1–ABD3, i.e. the diodes with intentional residual damage. The position of the middle of the EOR defect band is indicated.

Figure 5 shows the current density at 1 and 6 V reverse bias versus the distance between the junction and the dislocation defect band ($X_{DEFECTS}$–X_J) for diodes ABD1, ABD2, and ABD3, along with the corresponding case without defects, diode AB4, which has a similar boron concentration at the junction. A positive value for $X_{DEFECTS}$–X_J indicates that the defect band is deeper than the junction, and is

more likely to be located within the depletion region. In general the addition of defects has increased the leakage current density, which agrees with previous studies on leakage in p+/n diodes [10-12]. The increase appears to be greater at low E_{FIELD} (low biases) compared to at high E_{FIELD} (high biases). For diodes ABD2 and ABD3 the defect band is located deeper than the junction and at 1 V reverse bias the increase in leakage is more than 3 orders of magnitude. At higher E_{FIELD} (6 V) the defect band contribution is ~2 orders of magnitude. The thermal emission from traps may be field dependent [13] so the TAT contribution to the leakage current may change with bias. Also at higher biases BBT becomes more significant, the relative contribution of TAT to the total current may drop. For diode ABD1 the defects are slightly shallower than the junction and as a result are not all located in the depletion region. Thus the relative defect contribution to leakage is less.

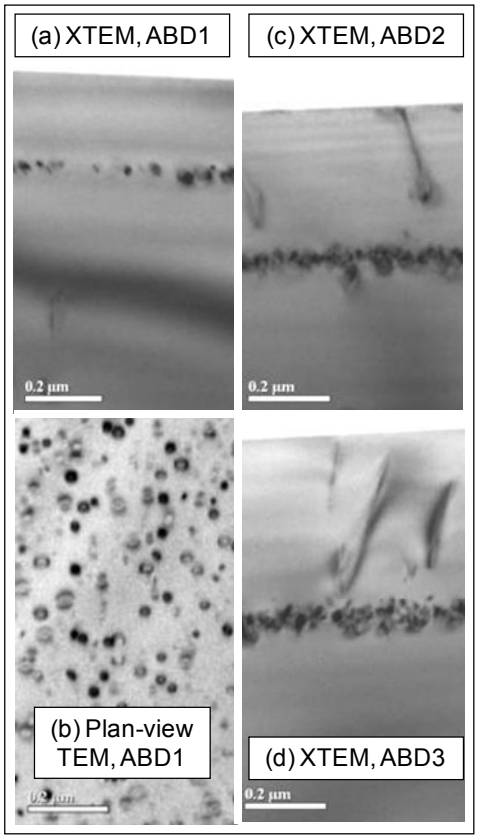

Figure 4 (a) XTEM image of diode ABD1 shows an EOR defect band at a depth of 236 nm, (b) a plan-view TEM image of the same diode showing the presence of large silicon interstitial defects, (c) XTEM image of diode ABD2 shows an EOR defect band at a depth of 373 nm, and (d) XTEM image of diode ABD3 shows an EOR defect band at a depth of 452 nm.

The elevated temperature measurements are shown in Fig. 6 for diode ABD2. There is an increase in leakage with temperature. The inset of Fig. 6 shows E_A versus reverse bias. The curves for ABD1, ABD2, and ABD3 overlap almost perfectly. With midgap E_A TAT is the dominant mechanism, but the same E_A for the different diodes indicates that the defect band depth has little qualitative impact on the generation mechanism. At increased reverse bias BBT becomes more significant and thus E_A drops. Also included are the data for diode AB4, which has a similar background doping level without the residual defects. At low biases the E_A without residual defects is higher (0.61 vs 0.39 eV at 1 V), but they converge at higher biases.

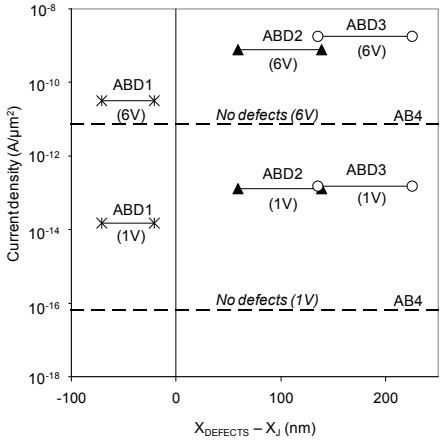

Figure 5 (a) Reverse current density at 1 V and 6 V reverse bias versus EOR defect band depth, for the diodes ABD1 – ABD3, corresponding to the SIMS depth profiles in Fig. 3, and the TEM images in Fig. 4. Diode AB4 is the "No defects" case.

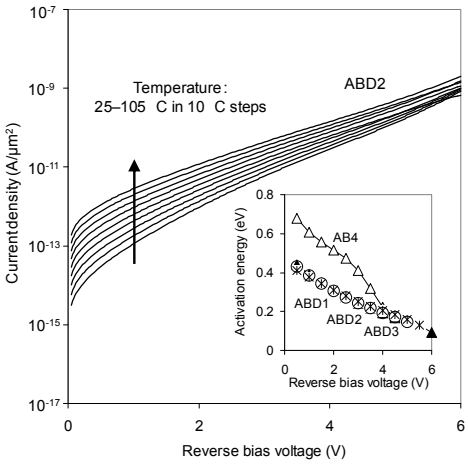

Figure 6 Reverse current density versus reverse bias, with temperature varied between 25 °C and 105 °C. For clarity only diode ABD2 is shown. The inset shows activation energy of the current density characteristics versus reverse bias for the diodes AB4 and ABD1–ABD3. The values for diodes ABD1 – ABD3 lie on each other.

The forward bias characteristics for diodes ABD1, ABD2, and ABD3 were measured at 25 °C. As expected due to the presence of large silicon-interstitial defects the ideality factors (n) are >1. Here we observe n values of 1.57, 1.79 and 1.75 respectively.

A summary of forward bias characteristics is shown in Fig. 7, for all the diodes in the larger body of work. The ideality factor is plotted versus background concentration. As expected the cases with residual EOR defects exhibit the worst ideality for a fixed background concentration. All diodes without intentional EOR defects follow a similar trend and across the concentration range of 1.5-4×10^{18} cm^{-3} where there is a sharp degradation. This is highly significant as minor changes in channel doping would lead to a large leakage variation.

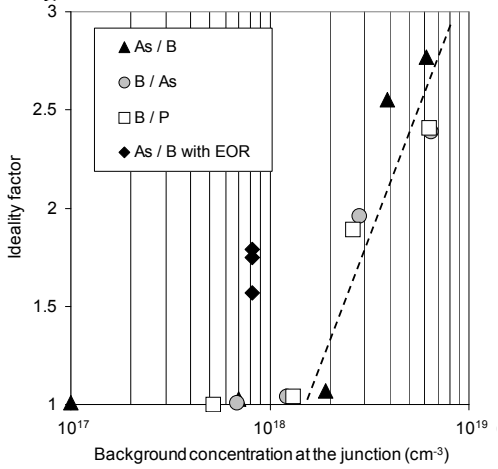

Figure 7 Forward bias ideality factor at 25 °C versus background concentration at the junction for all the diodes in this work. The diodes without intentional residual defects follow the same trend. The dashed line is added to guide the eye.

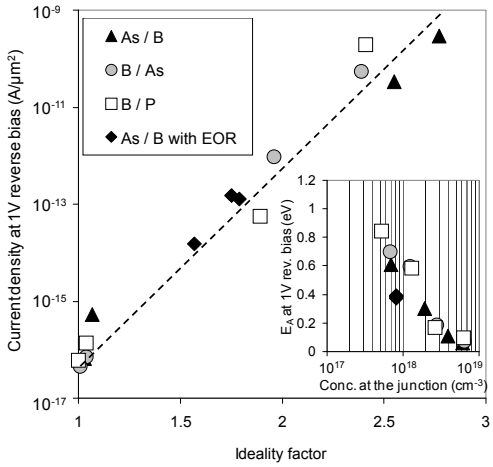

Figure 8 Reverse current density at 1 V versus forward bias ideality factor. All the diodes lie on the same trend-line. The dashed line is added to guide the eye. The inset shows activation energy of the current density at 1 V reverse bias versus background concentration at the junction. The diodes without intentional residual defects follow the same trend.

Figure 8 shows the correlation between reverse bias current density at 1 V and forward bias ideality factor. As n increases so does the reverse leakage. All data points, from the widely varying diodes in our work, lie on a straight line. Thus, diode behaviour in our experiments is linked regardless of dopant species on the high-concentration side (here arsenic and boron), regardless of dopant species on the low-concentration side (here boron, arsenic, and phosphorus), and also regardless of the presence or absence of identified and unidentified residual defects. The inset of Fig. 8 shows E_A of reverse leakage at 1 V as a function of background concentration for all the diodes in this work. Without residual EOR defects the characteristics fall on the same trendline. E_A falls as concentration increases, from ~0.8 eV at 7×10^{17} cm^{-3}, to ~0 eV at 6×10^{18} cm^{-3}. BBT will increase and start to dominate as background doping levels are increased. With residual EOR defects E_A is slightly lower.

3.2 Insight from modelling

As described in Fig. 2 SIMS analysis was used to extract the doping profiles from the structures that were measured electrically. The doping profiles were then used to define donor and acceptor profiles in the device simulator MEDICI to enable a closer evaluation of the electrical measurements and to validate the accuracy of the physical models available. Established models were used for doping concentration dependent SRH, Band Gap Narrowing (BGN), TAT, BBT, self-consistent impact ionisation, and Auger recombination.

To promote confidence in the modeling capabilities we first benchmarked the simulations against the extensive experimental work [7]. With only a slight alteration of default model parameters, established models could accurately predict the dominant leakage mechanism and quantify experimental current densities in diodes with ideality factors <2 without EOR defects. However, in diodes with EOR defects or ideality factors >2, the simulations underestimated the very high leakage levels, indicating that there is a source of leakage that the simulation code cannot account for. Note, Schenk has successfully modelled drain leakage SOI nFETs [14], so future simulation code may well be capable to account for these crystal anomalies.

We know that EOR defects increase leakage. The quantification of the EOR defect contribution to leakage may be complicated if processing is altered, say by changing the preamorphisation depth. In the simulations we can predict the leakage generated by the doping profile (i.e. E_{FIELD}), while in the experiment we have the combination of the doping profile and EOR defect contributions. Thus the "*measurement vs simulation*" comparison can quantify the EOR defect contribution.

Figure 9 shows the measured and simulated characteristics of n+/p diodes with EOR defects, ABD1, ABD2, and ABD3. As expected the simulated current densities are lower than the measurements. Note the defect contribution is dependent on the applied bias, and thus on the E_{FIELD}. In

this case at low E_{FIELD} (1 V) the EOR defects contribute 3 orders of magnitude to leakage, while at higher E_{FIELD} (6 V) they contribute 2 orders of magnitude.

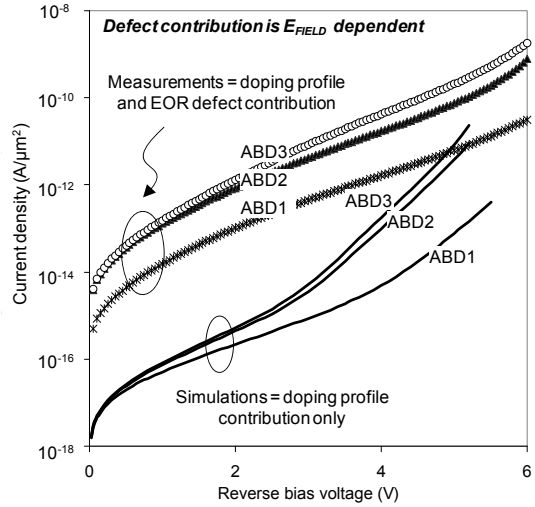

Figure 9 Experimental and simulated reverse current density versus reverse bias, for diodes ABD1 – ABD3. The difference between the experimental and simulated characteristics indicates the EOR defects contribution to leakage.

3.3 The trouble with unintentional defects

It was noted earlier that models could not reproduce the high leakage and high ideality factors (>2) in the diodes with high background doping concentrations, regardless of what dopant (arsenic, phosphorus, or boron) was used.

In [7] carrier lifetimes were used as a fitting parameter. For the diodes with background concentrations $>2\times10^{18}$ cm^{-3} the simulated lifetimes were reduced significantly. While this calibration approach was sufficient for the current density characteristics at 25 °C, the temperature dependence (E_A ~0 eV) was not well reproduced. This indicates that a severe local E_{FIELD} enhancement is present in those diodes that is not captured in the simulations. Furthermore it appears to be independent of dopant type and species.

This discrepancy is not considered to be a miscalibration of the BBT model, as fitting the current density characteristics would require a large, unphysical, change in the BBT model parameter set. Likewise it is not thought to be a miscalibration with the BGN model. BGN has a significant effect on tunnelling generation because if the band gap is smaller it is easier for carriers to tunnel through. This effect is associated with highly doped substrates. Using the model for BGN from Jain and Roulston [15], who showed their expression fits experimental data accurately, the highest BGN for our experiment is ~60 meV. If a forced calibration is applied in our simulations, BGN of >400 meV is required for the high background concentration diodes, which clearly is not physical.

To identify the source of this problem FTIR absorption measurements were undertaken on 3 structures, namely a non-ideal case (diode AB2 – background boron concentration at the junction = 3.9×10^{18} cm^{-3}, n=2.55), an ideal case (diode AB3 – background boron concentration at the junction = 1.9×10^{18} cm^{-3}, n=1.07), and a control of the arsenic profile without any boron.

As a non-destructive characterisation technique, FTIR spectroscopy has been used successfully in detecting interstitial oxygen, nitrogen, boron, and other impurities in silicon wafers. The strength of the absorption of a species is proportional to the concentration. Shown in Fig. 10 are all the absorbance traces extracted. We focused the spectroscopic study on the 1000–1300 cm^{-1} spectral range, where infrared absorption bands for SiO_2 and B_2O_3 precipitates can be detected [16]. The band around 1100 cm^{-1} confirms the presence of precipitates in the material from the non-ideal diode AB2. The low intensity collected does not allow us to address the contribution of each precipitate to the band observed.

Corresponding FTIR analysis was undertaken to investigate samples with high background concentrations of arsenic and phosphorus, but unfortunately proved inconclusive.

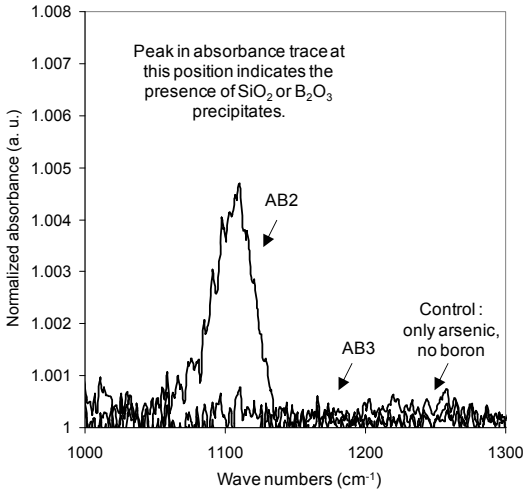

Figure 10 FTIR absorption traces for diodes AB2 and AB3, along with a control of arsenic without boron. A peak in the absorption trace indicates the presence of clusters or precipitates.

Generation/recombination centres that reduce carrier lifetimes can be induced by the presence of clusters or precipitates in the silicon. At high E_{FIELD} the barrier for thermal emission from traps may be reduced, due to the Poole-Frenkel effect, and would be consistent with our observations of E_A ~0 eV for the diodes with the highest background doping concentrations. But where do the supposed precipitates come from at high dopant concentrations? In their work on silicon emitters, Andersson and Engström reported that generation centres were formed due to a clustering process linked to high phosphorus concentrations [17]. Our FTIR analysis points to oxygen related precipitation at high boron concentrations. Bothe and Schmidt reported that carrier lifetime limiting centres form in boron-

doped oxygen-contaminated crystalline silicon [18]. Their concentrations are linearly dependent on substitutional boron concentration and quadratically dependent on interstitial oxygen concentration. Furthermore oxygen content in the starting wafer in the 10^{17} cm^{-3} range has been shown to increase leakage by Slotboom *et al*. [19], while Busta and Waggener studied generation currents induced by metal impurity precipitation. In their analysis they obtained deep energy levels through deep level transient spectroscopy for gold, iron, copper, nickel, tantalum, and tungsten [20].

Mitromara *et al*. performed Deep Level Transient Spectroscopy (DLTS) and Laplace DLTS (LDLTS) measurements on samples similar to those here with high background doping concentrations [21,22]. In control samples with just the shallow high-dose implant (i.e. the n+ of the n+/p diodes), no DLTS signals were observed. In the samples with a background doping implant the DLTS predominantly showed minority carrier emission, irrespective of the implanted species. LDLTS applied to these minority carrier traps, showed that the emission rate was temperature independent. This was interpreted as being due to carrier trapping in small quantum-well-like regions in the highly doped shallow junctions. Generally, LDLTS of all traps examined showed multiple emission rates, suggestive of complicated defect structures rather than isolated point defects.

Recently Nyamhere *et al*. performed DLTS on small interstitial clusters and {311} defects in n-type Si [23]. In samples with small clusters, deep levels at E_c-0.24 eV and E_c-0.54 eV dominated. In samples containing {311} defects, the E_c-0.54 eV level was still present while other electron traps E_c-0.26 eV and E_c-0.46 eV were introduced.

Finally, Hurkx and Agarwal reported that quantum-mechanical effects influence the generation-recombination rates and the carrier concentrations in the depletion layer [24]. At doping concentrations $>10^{18}$ cm^{-3} the carrier concentrations in the depletion layer are several orders of magnitude greater than in the semiclassical case. This indicates that for such high doping levels the classical drift-diffusion theory starts losing its validity for predicting diode currents and, hence, our simulations may be inaccurate at very high doping levels.

4 Conclusions

In this paper characterisation of electrically active defects was reviewed. The influence of doping levels and implant related damage on reverse biased leakage currents in n^+/p and p^+/n diodes was quantified. The EOR defect contribution to leakage was shown to be E_{FIELD} dependent.

In diodes with ideality factors ~2 and higher, the simulations underestimated the very high leakage levels, indicating that there was a source of leakage not captured by the simulation code. This behavior was independent of dopant species used as n+/p and p+/n diodes with boron, arsenic, and phosphorus all produced the same trend. The temperature independence of the high leakage levels point to an E_{FIELD} dependent tunneling related mechanism. The exact cause may be linked to quantum mechanical effects or a local E_{FIELD} enhancement due to precipitates or clusters.

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