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Single-electron counting statistics and its circuit application in nanoscale field-effect transistors at room temperature

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Abstract

A circuit utilizing single electrons is demonstrated at room temperature. Individual electrons randomly passing through the nanoscale silicon-on-insulator metal-oxide-semiconductor field-effect transistor (MOSFET) are monitored by an electrometer in real time. Such a random behavior of single electrons is used for high-quality random-number generation suitable for data processing which stochastically extracts the most preferable pattern among various ones. MOSFET-based random-number generation allows fast operation as well as high controllability, which leads to flexible extraction of the preferable pattern.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The continuously advancing miniaturization of Si metal-oxide-semiconductor field-effect transistors (MOSFETs) has enhanced the performance of various consumer electronics [1]. However, guaranteeing error-free operation of MOSFETs leads to increased current density and power consumption [2, 3]. In contrast, ultimate reduction of current can open up a fascinating field where a single electron plays a crucial role. Since applications using a single electron as one bit of information promise ultra-low power consumption, various kinds of circuits have been proposed [4–9]. Such applications increase the importance of analyzing the movement of a single electron, which can be done by monitoring it in real time. Since single-electron movement is also attracting huge attention from the academic viewpoint, real-time monitoring of single-electron transport through a solid-state device has been widely studied as single-electron counting statistics [10–13]. However, single-electron counting statistics in MOSFETs, one of the most familiar solid-state devices, has not been possible because single electrons travel through the MOSFET channel from the source to the drain too fast for an electrometer to detect individual electrons. Other reasons are that previously reported devices require a complicated device structure as well as a low-temperature measurement system and that a small leakage current flows even when a MOSFET is turned off due to inevitable imperfection of the channel quality especially at p–n junctions [14]. Actually, single-electron counting statistics deepen our understanding of shot noise in MOSFETs, which is one of three kinds of noise: thermal noise, flicker noise, and shot noise [15–18]. Shot noise originates from individual electrons passing through a MOSFET and is the most fundamental noise among the three types. However, it has only been possible to indirectly analyze shot noise from spectrum measurements because it is often masked by other noises.

In this paper we report single-electron counting statistics in Si MOSFETs at room temperature. Real-time monitoring of single-electron transport through a high-quality channel of the MOSFET by a high-charge-sensitivity electrometer reveals that single-electron transport or shot noise is dominated not by the single-electron tunneling effect, which had been studied in other reports, but by thermal activation, which allows high controllability based on the well-known FET theories [19]. Utilizing a stochastic behavior of single-electron transport for physical random-number generation, we demonstrate a stochastic data processing circuit for pattern recognition with high flexibility. In contrast to the previous report showing a basic demonstration of the stochastic circuit [9], simpler and more practical demonstrations are achieved because of

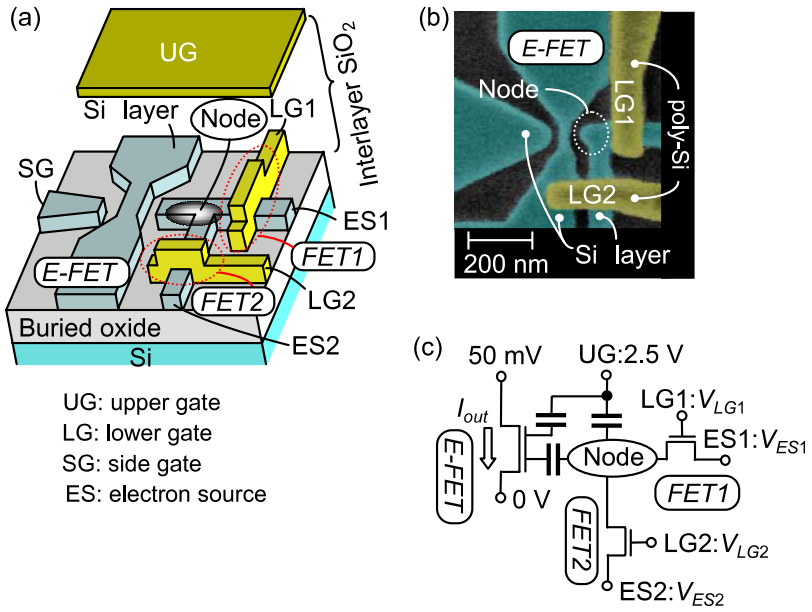

Figure 1. Device structure for single-electron counting. (a) A schematic view. (b) A scanning electron microscope image after the formation of the FET channels, LG1 and LG2. (c) An equivalent circuit. The voltage applied to the SG is 0 V.

improvement of the device structure and usage of additional pattern-reconstruction processes, respectively.

2. Device structure and its principle

Our device for single-electron counting statistics (figure 1) is composed of three nanoscale MOSFETs: one single-electron electrometer (E-FET) and two single-electron transfer FETs (FET1 and FET2). A T-shaped wire and a narrow constriction were patterned on an undoped silicon-on-insulator (SOI) layer. This was followed by thermal oxidation to convert the constriction into a tiny channel for the E-FET, which leads to high charge sensitivity for the detection of single electrons. Then, two lower gate electrodes (LG1 and LG2) made of a polycrystalline Si (poly-Si) were fabricated on the wire channel, which was followed by thermal oxidation. Finally, an interlayer SiO_2 and an upper gate (UG) were formed on the whole area. The final size of the SOI channel and poly-Si gate after oxidation to shrink them is estimated as follows: the thicknesses and width of channels of FET1 and FET2 are 30 nm, the length and oxide thickness of LG1 and LG2 are 20 and 35 nm, respectively, and the gap between the node and E-FET is 50 nm. The thickness of the interlayer SiO_2 is 50 nm.

The upper gate (UG) is used to invert the undoped channel of FET1 and FET2 so as to define source and drain regions electrically at both sides of the two lower gates (LG1 and LG2). LG1 and LG2 turn FET1 and FET2, respectively, on and off like a conventional FET. Since the two drains are connected and terminated at the tip, or node, of the wire channel, electrons are transferred one after another from the electron sources (ES1 and ES2) to the node. The transferred electrons are detected as a change in current I_{out} flowing through the E-FET, which is capacitively coupled to the node [20].

3. Experimental results and discussions

3.1. Single-electron transfer and detection

We first demonstrated multiple-electron transfer from ES1 (ES2) to the node, which was monitored as the change in I_{out} (figure 2(a)). When the voltage of LG1 (LG2), V_{LG1} (V_{LG2}), was changed from -4 V and reached -2.5 V, I_{out} abruptly decreased because FET1 (FET2) turned on and a lot of electrons from ES1 (ES2) entered the node. The subsequent reverse sweep of V_{LG1} (V_{LG2}) caused hysteresis in I_{out} because FET1 (FET2) turned off at a V_{LG1} (V_{LG2}) of -2.5 V and electrons were stored in the node.

Using a fixed V_{LG1}, which was a little lower than that causing the electron injection shown in figure 2(a), we performed a time-resolved measurement of single-electron transfer though FET1. As shown in figure 2(b), I_{out} decreased in steps with the same height. This is proof that a single electron, which entered the node from the ES1 through FET1, was detected as one step of I_{out} [7–9, 20]. From each step height of I_{out} and current characteristics (not shown here) of the E-FET when FET1 is on and V_{ES1} is changed [20], change in the node potential caused by the single-electron injection and self-capacitance of the node are evaluated to be 8.9 meV and 18 aF, respectively. Single-electron counting statistics can be achieved in the MOSFET because the E-FET has charge sensitivity, which is evaluated to be $0.051e$ $Hz^{-1/2}$ at 10 Hz from each step height and noise spectrum of I_{out} [20], high enough to detect individual electrons stored in the node, and because the time interval δt between the transfer of each electron through the MOSFET into the node becomes long enough for the E-FET to detect it in a time-resolved manner. The better charge sensitivity can be obtained by optimizing the side gate (SG) so that I_{out} has a larger transconductance [20] (not done in this paper).

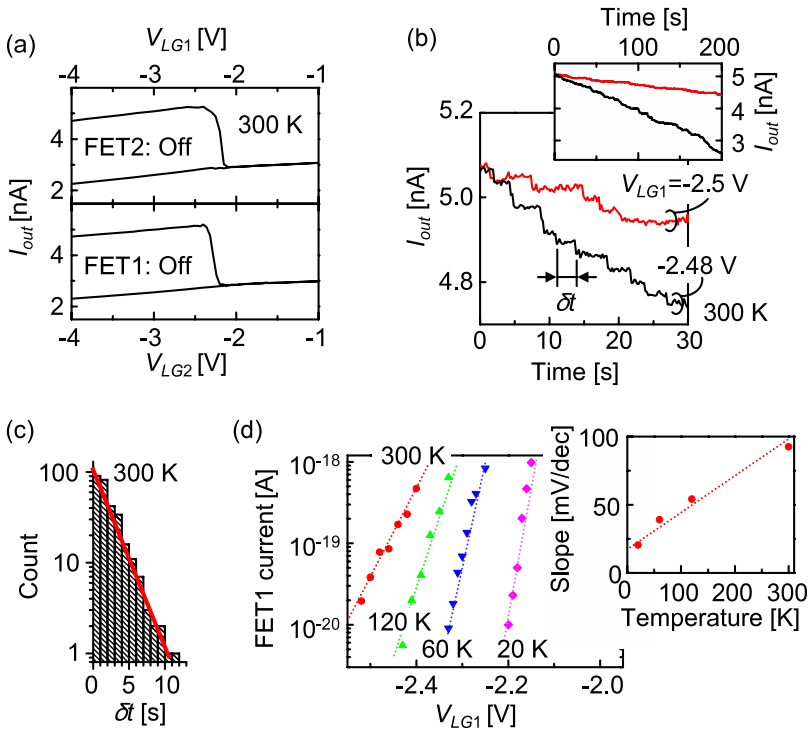

Figure 2. Electron transfer into the node. (a) A transfer of a huge number of electrons by turning FET1 (upper) and FET2 (lower) on and off. In the upper (lower) plot, FET2 (FET1) is kept off by adjusting $V_{\rm LG2}$ ($V_{\rm LG1}$) to be -4 V. Before the measurement, all electrons in the node were removed by opening FET1 and FET2 and setting both $V_{\rm ES1}$ and $V_{\rm ES2}$ to 2 V and, then, FET1 and FET2 turned off. The number of electrons in the node after electron transfer is estimated to be 140. (b) Counting of single-electron transfer through FET1. $V_{\rm ES1} = -1$ V. $V_{\rm ES2}$ and $V_{\rm LG2}$ were adjusted to the node, -4 to -1 V, respectively, so that no electrons enter through FET2. Electrons enter randomly though FET1 until the number of electrons in the node reaches around 100 as shown in the inset. The change in $I_{\rm out}$ from the beginning of measurements corresponds to the excess number of electrons in the node above charge neutrality after electron removal. (c) Histogram of the time interval, δt, in (b), at $V_{\rm LG1}$ of -2.48 V. (d) Sub-atto-ampere current characteristics as a function of $V_{\rm LG1}$ at various temperatures. $V_{\rm LG2}$ and $V_{\rm ES2}$ were -4 and -1 V, respectively. Current, which is the total charge transferred from the ES to the node for 1 s, is evaluated $e/\langle\delta t\rangle$, where e is the elementary charge, and $\langle\delta t\rangle$ the average of 100 samples of δt. For the clarity, plots at 20, 60, and 120 K are horizontally shifted by -0.6 V. Change in the slope of the dotted line, which is a guide of the eye, is plotted as a function of temperature in the inset.

From the viewpoint of single-electron counting statistics, it should be noted that δt is always random. The histogram of δt in figure 2(c) clearly shows an exponential decay and its Fano factors, defined as the ratio of deviation of δt to the average of δt, are close to 1, which means that single-electron transport though the MOSFET follows the Poisson process. In other words, the ideal Poissonian behavior of single-electron transport means that repulsive force from electrons in the node is negligible for subsequent single electrons entering there due to the sufficiently large size or small charging energy of the node explained before, which leads to continuous single-electron transport as shown in the inset of figure 2(b).

In contrast to random δt, its average, i.e. an extremely small current in the FET, can be fully controlled using $V_{\rm LG1}$ as shown in figure 2(d). This is because our device, whose electrical channels are formed by the UG instead of a p–n junction, eliminates undesired leakage current originating from electron–hole generation centers in p–n junctions [14, 20, 21]. More importantly, slopes of dotted lines in current characteristics shown in figure 2(d) have a linear dependence on temperature as shown in the inset of figure 2(d). This means that the single-electron transfer, or shot noise, follows the well-known theory of thermally–activated subthreshold current in conventional MOSFETs, which guarantees a highly controllable single-electron transfer according to the MOSFET theory [19].

3.2. Stochastic circuit for pattern recognition

Single-electron transfer based on the Poisson process and MOSFET theory allows high randomness of δt and high controllability of averaged δt, respectively. These features are useful for an elementary device for a stochastic data processing circuit, which is a stochastically working XNOR device (S-XNOR) [9, 22–24]. When both the input (i_j) and reference (r_j) signals are '1' ('0'), more electrons are injected through FET1 (FET2) into the node than when other combinations of signals are applied, as shown in figures 3(a) and (b), which corresponds to the XNOR function. What is important here is that because the number of electrons injected into the node always fluctuates as shown in figure 3(c), the device performs XNOR correctly in most cases but does so incorrectly with some possibility which corresponds to stochastic XNOR operation. Figure 3(c) also indicates high-speed operation (100 ns) due to the FET-based single-electron transfer. Since the demonstrated speed was limited by the various kinds of capacitors in the measurement system, optimization of the system will lead to much faster operation. Although the

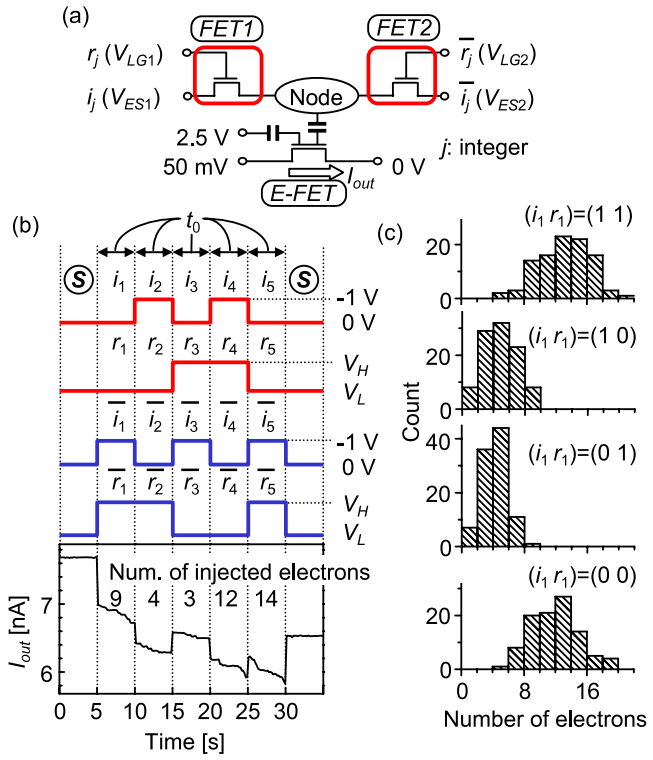

Figure 3. Demonstration of an S-XNOR circuit. (a) Equivalent circuit. (b) Waveforms of input/reference signals and experimental results when input and reference signals were (0 1 0 1 0) and (0 0 1 1 0), respectively. The signals are fed into the device sequentially. $V_H = -2.41$ V, $V_L = -2.46$ V, and $t_0 = 5$ s. In the experimental plot, the number of electrons injected at each binary signal is also shown. The abrupt change in I_{out} when input and reference signals were changed was due to the capacitive coupling between ES1/ES2 and the E-FET and between LG1/LG2 and the E-FET. Since voltage conditions during S at the beginning of the waveform are the same as those at the end, the difference between I_{out} at the beginning and the end corresponds to the number of electrons in the node above. (c) Histograms of the number of electrons for different (i_j, r_j) at high-speed operation. $V_H = -1.75$ V, $V_L = -1.8$ V, and $t_0 = 100$ ns.

XNOR function was demonstrated in a previous paper [9], FET1 and FET2 had the E-FETs individually. Therefore, we had to optimize voltages applied to the E-FETs separately so that they had the same step in I_{out}s caused by single-electron injection through FET1 and FET2, which led to the difficulty and complexity of XNOR operation. In contrast, since FET1 and EFT2 share the same E-FET and node in this paper, the XNOR function can be easily achieved.

Actually, this S-XNOR function can also be achieved by using a conventional XNOR circuit and physical random-number generation, whose randomness is high enough to avoid biased results of the S-XNOR function. However, physical random-number generation, which originates from nuclear radiation and white noise in solid-state devices, requires complex circuits, which make fast operation and high controllability difficult. In contrast, our device, which uses the natural behavior of single-electron transfer through the FET for physical random-number generation, offers a simple structure and fast operation, which are very useful for the circuit application demonstrated below.

Figure 4(a) shows schematics of pattern recognition using the S-XNOR. Input and reference patterns consist of 5 × 5 segments and represent alphabetic patterns, whose color is black or white, like the patterns 'N', 'M', and 'H' shown in figure 4(b). For the expression of patterns using binary signals, the black and white segments are replaced with the binary signal 1 and 0, respectively. The patterns are divided into five rows and each row is expressed by 5 bit input (i_1 i_2 i_3 i_4 i_5) and reference (r_1 r_2 r_3 r_4 r_5) signals, both of which are fed sequentially into the S-XNOR as shown in figure 3(b). After all rows are input, the numbers of electrons in the nodes of all S-XNORs are summed up, and the reference pattern giving the maximum sum of electrons is chosen as the pattern most resembling the input pattern and becomes the 'winner' among all reference patterns.

Figure 4(b) shows the number of chances of winning for each reference pattern when the input pattern was 'N'. For the demonstration, just one S-XNOR was used for the five rows composed of 5 bit signals as follows. When one row was fed into the S-XNOR, the number of electrons in the node was counted. Then, after all electrons were removed from the node, the next row was fed. These were repeated for five rows and the numbers of electrons transferred into the node at all rows were summed up. Although the reference pattern 'N' became the winner with high probability, other reference patterns also became winners with some probability because the numbers of electrons fluctuated every time as shown in figure 3(c). Note that the number of chances of winning increases with decreasing Hamming distance, which is defined as the number of different signals between the input and reference patterns to express the similarity between them. This feature means that the stochastic circuit can choose the preferable reference pattern with some flexibility.

Such flexible operation of the stochastic circuit is very useful when an input pattern is corrupt, as shown in figure 4(c). Although humans can recognize the corrupt pattern as 'N' owing to their flexible imagination, the deterministic computation based on the Hamming distance recognizes the corrupt pattern as 'H'. In contrast, the stochastic circuit can choose 'N' with some possibility, as shown in figure 4(c). Owing to this flexibility, human-brain-like recognition can be achieved by a pattern-reconstruction process (figure 4(d)). By repeating the pattern-reconstruction process, the corrupt pattern gradually comes to resemble the most preferable pattern 'N' as shown in figure 4(e). At the beginning, the winning probability of each reference pattern fluctuates because the reference patterns are chosen as winners with similar probability (open bars of figure 4(c)). However, by changing V_L to choose the preferable reference pattern with higher selectivity (closed bars), the winning probability is stabilized and 'N' is chosen as the winner with high probability. Such control of the winning probability is called 'simulated annealing' in software algorithms [25, 26]. The inset of figure 4(c) is a schematic energy diagram showing the system for a qualitative explanation of simulated annealing. The closed circle depicts the state of the system, and fluctuation of the winning probability of the device operation corresponds to fluctuation of the energy applied to the system. To

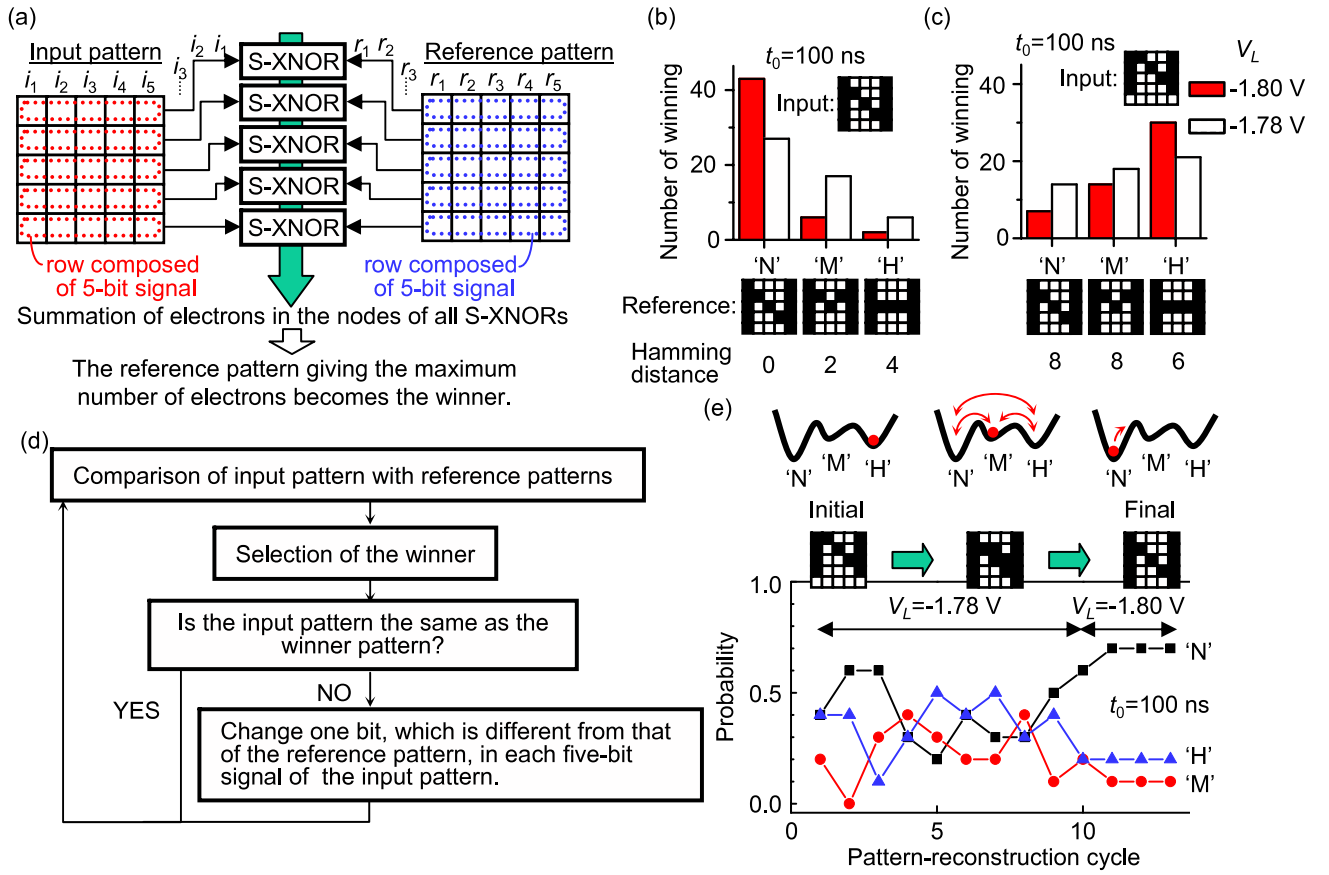

Figure 4. Demonstration of a stochastic single-electron circuit for a pattern recognition. (a) Schematics of the circuit. (b), (c) The number of chances of winning for each reference pattern at two input patterns. V_H was −1.75 V. The numbers beneath the reference patterns on the x-axis indicate the Hamming distance. (d) Sequence for pattern reconstruction. The input pattern is changed so that it becomes close to the reference pattern that becomes the winner. (e) Change in the probability of winning of each reference pattern when the pattern reconstruction was repeated. The probability was evaluated from an ensemble composed of 10 samples of learning cycles. After 10 pattern-reconstruction cycles, V_L was changed. The lower inset shows the change in pattern of one sample during the pattern-reconstruction cycle. The upper inset is a schematic energy diagram showing the system for a qualitative explanation of the simulated annealing.

provide the reference pattern resembling the input pattern, the system has two local energy minima ('H' and 'M') and one global minimum ('N') that corresponds to the most preferable state. At the initial stage, the system localizes the state of 'H', which has the smallest Hamming distance, having the local minima. When the pattern reconstruction is repeated at V_L of −1.78 V for larger energy fluctuation to the system, the system fluctuated randomly between other states, which corresponds to the annealing process. Then, when V_L is changed to −1.78 V for a smaller energy fluctuation, the system is stabilized at the global minimum 'N', which corresponds to the cooling process. In this circuit, such an annealing scheme is realized physically owing to the high controllability of the winning probability using the FET as shown in figure 4(b), promising fast and precise extraction of the preferable operation.

Stochastic circuits based on the same concept are expected to be useful for other applications, such as data clustering and vector quantization [25]. While conventional data processing circuits give deterministic results without error, the stochastic circuit gives one of the most favorable ones in a flexible manner. Therefore, although it is hard to compare their performance directly, the stochastic circuit can allow data processing treating a huge number of data with high time and high power efficiency like the human brain.

4. Conclusions

In summary, we have demonstrated single-electron counting statistics in FETs. It has been confirmed that shot noise comprises stochastic single-electron transport based on a Poisson process, which can be controlled by gate voltage. Using the excellent randomness of the electron transport, we demonstrated a circuit for pattern recognition with high flexibility, which is promising for achieving high performance, time efficiency, and low power consumption. We believe that the stochastic behavior of single electrons in shot noise can open another path to applications for MOSFETs.

References

[1] 2008 *International Technology Roadmap for Semiconductors* Available at http://www.itrs.net/
[2] Bourianoff G 2003 The future of nanocomputing *IEEE Comput.* **36** 44–53

[3] Bourianoff G I, Gargini P A and Nikonov D E 2007 Research directions in beyond CMOS computing *Solid-State Electron.* **51** 1426–31
[4] Likharev K K 1999 Single-electron devices and their applications *Proc. IEEE* **87** 606–32
[5] Asahi N, Akazawa M and Amemiya Y 1997 Single-electron logic device based on the binary decision diagram *IEEE Trans. Electron Devices* **44** 1109–16
[6] Lent C S, Tougaw P D and Porod W 1992 Bistable saturation in coupled quantum dots for quantum cellular automata *Appl. Phys. Lett.* **62** 714–6
[7] Nishiguchi K, Inokawa H, Ono Y, Fujiwara A and Takahashi Y 2004 Multilevel memory using an electrically formed single-electron box *Appl. Phys. Lett.* **85** 1277–9
[8] Nishiguchi K, Fujiwara A, Ono Y, Inokawa H and Takahashi Y 2006 Room-temperature-operating data processing circuit based on single-electron transfer and detection with metal-oxide-semiconductor field-effect transistor technology *Appl. Phys. Lett.* **88** 183101
[9] Nishiguchi K, Ono Y, Fujiwara A, Inokawa H and Takahashi Y 2008 Stochastic data processing circuit based on single electrons using nanoscale field-effect transistors *Appl. Phys. Lett.* **92** 062105
[10] Lu W, Ji Z, Pfeiffer L, West K W and Rimberg A J 2003 Real-time detection of electron tunneling in a quantum dot *Nature* **423** 422–5
[11] Fujisawa T, Hayashi T, Hirayama Y and Cheong H D 2004 Electron counting of single-electron tunneling current *Appl. Phys. Lett.* **84** 2343–5
[12] Bylander J, Duty T and Delsing P 2005 Current measurement by real-tme counting of single electrons *Nature* **434** 361–4
[13] Fujisawa T, Hayashi T, Tomita R and Hirayama Y 2006 Bidirectional counting of single electrons *Science* **312** 1634–6
[14] Nakajima H, Yanagi S, Komiya K and Omura Y 2002 Off-leakage and drive current characteristics of sub-100 nm SOI MOSFETs and impact of quantum tunnel current *IEEE Trans. Electron Devices* **49** 1775–82
[15] Das M B and Moore J M 1974 Measurement and interpretation of low-frequency noise in FET's *IEEE Trans. Electron Devices* **21** 247–57
[16] Jayaramans R and Sodini C G 1989 A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon *IEEE Trans. Electron Devices* **36** 1773–82
[17] Reimbold G 1984 Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion—influence of interface states *IEEE Trans. Electron Divices* **31** 1190–8
[18] Sarpeshkar R, Delbruck T and Mead C A 1993 White noise in MOS transistors and resistors *IEEE Circuits Devices Mag.* **9** 23–9
[19] Sze S M 2001 *Physics of Semiconductor Devices: Physics and Technology* 2nd edn (New York: Wiley)
[20] Nishiguchi K, Koechlin C, Ono Y, Fujiwara A, Inokawa H and Yamaguchi H 2008 Single-electron-resolution electrometer based on field-effect transistor *Japan. J. Appl. Phys.* **47** 8305–10
[21] Nishiguchi K, Fujiwara A, Ono Y, Inokawa H and Takahashi Y 2007 Long retention of gain-cell dynamic random-access memory with undoped memory node *IEEE Electron Device Lett.* **28** 48–50
[22] Saen M, Morie T, Nagata M and Iwata A 1998 A stochastic associative memory using single-electron tunneling devices *IEICE Trans. Electron.* **E81-C** 30–5
[23] Tamanaka T, Morie T, Nagata M and Iwata A 2000 A single-electron stochastic associative processing circuit robust to random background-charge effects and its structure using nanocrystal floating-gate transistors *Nanotechnology* **11** 154–60
[24] Yamanaka T, Morie T, Nagata M and Iwata A 2001 A CMOS stochastic associative processor using PWM chaotic signals *IEICE Trans. Electron.* **E84-C** 1723–9
[25] Morie T, Matsuura T, Nagata M and Iwata A 2002 An efficient clustering algorithm using stochastic association model and its implementation using nanostructures *Advances in Neural Information Processing Systems* vol 14, ed T G Dietterich, S Becker and Z Ghahramani (Cambridge, MA: MIT Press) pp 1115–22
[26] Kirkpatrick S, Gelat C D and Vecchi M P 1983 Optimization by simulated annealing *Science* **220** 671–80