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Current, voltage and temperature distribution modeling of light-emitting diodes based on electrical and thermal circuit analysis

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Abstract
We demonstrate a modeling method based on the three-dimensional electrical and thermal circuit analysis to extract current, voltage and temperature distributions of light-emitting diodes (LEDs). In our model, the electrical circuit analysis is performed first to extract the current and voltage distributions in the LED. Utilizing the result obtained from the electrical circuit analysis as distributed heat sources, the thermal circuit is set up by using the duality between Fourier's law and Ohm's law. From the analysis of the thermal circuit, the temperature distribution at each epitaxial film is successfully obtained. Comparisons of experimental and simulation results are made by employing an InGaN/GaN multiple-quantum-well blue LED. Validity of the electrical circuit analysis is confirmed by comparing the light distribution at the surface. Since the temperature distribution at each epitaxial film cannot be obtained experimentally, the apparent temperature distribution is compared at the surface of the LED chip. Also, experimentally obtained average junction temperature is compared with the value calculated from the modeling, yielding a very good agreement. The analysis method based on the circuit modeling has an advantage of taking distributed heat sources as inputs, which is essential for high-power devices with significant self-heating.

(Some figures may appear in colour only in the online journal)

1. Introduction

Typical high-power light-emitting diode (LED) package is composed of an LED chip, epoxy resins, a heat slug and a heat sink. The heat generated from an LED chip spreads out to surrounding materials mainly by the heat conduction process. Commercial thermal analysis software packages based on the finite element method (FEM) are adequate to calculate the temperature distribution and heat flow of a system with a small number of discrete heat sources. However, a high-power LED package, in which self-heating by the current crowding is the dominant heat source, should be simulated with distributed heat sources rather than discrete ones. The issue is that it is not easy to know the position and the quantity of heat sources due to the complicated flows of both current and heat in a multilayered three-dimensional LED package. Consequently, it is necessary to develop a method which is capable of calculating both heat sources and heat flows in a simultaneous manner.

Heat sources can be classified by their origins, i.e., Joule heating, nonradiative electron-hole recombination, Thomson effect and optical absorption. In recent nitride-based blue LEDs, heat sources due to Joule heating, nonradiative electron-hole recombination and optical absorption are the dominant ones. Of these sources, Joule heating and nonradiative

recombination are directly related to the current paths in an LED chip [1].

Typical nitride LEDs grown on the sapphire substrate have an etched mesa shape and a lateral contact configuration due to the insulating sapphire substrate. These diodes employ lateral as well as vertical current flows. In particular, the lateral current flow leads to nonuniform current spreading, the so-called current crowding effect with the corresponding Joule heating. Thus, uniform current density on the entire surface of an LED chip is essential to get high optical power and good reliability [2].

Heat is dissipated by three different processes, namely conduction, convection and radiation. Conduction is the dominant thermal dissipation process in an LED chip or package. Several techniques have been proposed to improve the thermal conduction process. Their basic idea is to remove partly or completely the low-thermal-conductivity sapphire substrate and to attach a high-thermal-conductivity material as near as possible to the self-heating area. LED performances related to temperature are characterized by the junction temperature of the intrinsic p–n diode that is locally balanced by the self-heat generation rate and the dissipation rate. Thus, it is very important to manage both the thermal and current distributions simultaneously in each epitaxial or metallic film constituting an LED chip.

Several approaches for the junction temperature measurement have been reported theoretically or experimentally. The forward voltage [3], threshold current [4], Raman spectroscopy [5] and/or the peak emission wavelength [6] have been utilized frequently for determining the junction temperature. Recently, methods using the reverse current [7] and luminous efficacy [8] were introduced to extract the average junction temperature. In these methods, the average junction temperatures can be known instead of the local temperatures. Infrared (IR) microscopes have often been used as well to measure a two-dimensional temperature distribution of an LED chip. The method is capable of measuring the IR intensity just at the surface. Moreover, it is not easy to analyze the local temperature accurately by this because the IR intensity distribution at the surface usually originates from different materials and each material has its own emissivity of energy radiation. Thus, the calibration of the radiation energy from each material is a mandatory procedure for the actual surface temperature measurement.

In this paper, we present an analysis method of the current, voltage and heat flows based on three-dimensional electrical and thermal equivalent circuits, utilizing a lateral-type InGaN/GaN multiple-quantum-well (MQW) LED grown on a sapphire substrate. The duality property between Fourier's law in heat transfer and Ohm's law in current flow allows us to use an electrical circuit simulator in both the thermal and electrical analyses [9–12]. We first calculate current and voltage distributions in space by analyzing the electrical equivalent circuit. Next, the results are used as distributed heat sources in a thermal equivalent circuit and finally the three-dimensional thermal distribution is obtained from the thermal circuit analysis. All the analyses of the equivalent circuits are implemented with a conventional circuit simulator (SPICE). Calculated current distribution is experimentally verified by measuring the light distribution at the surface and current–voltage characteristics. The temperature distribution is verified by measuring the junction temperature and IR distribution. In the following sections, theoretical formalisms for electrical and thermal equivalent circuits and their experimental verifications are described.

2. Circuit modeling and analysis

2.1. Electrical equivalent circuit

For direct-current operation, an LED can be electrically modeled by using only resistors and intrinsic diodes without considering the inductive and capacitive effects. The resistor circuit represents electrical properties of metallic, semiconductor, or dielectric materials. The intrinsic diodes describe those of the p–i–n diode region. An LED is spatially divided into small volumes (meshes) modeled by an electrical equivalent circuit as shown in figure 1(*a*) [13–15]. The maximum dimension of the mesh is determined by area, thickness and the number of epitaxial layer of a sample. In figure 1(*a*), V, I and R_E are voltage, current and electrical resistance, respectively, and suffixes i, j and k represent a discrete position denoted by the Cartesian coordinate system. Air adjacent to the LED surface is considered as a perfect insulator. The voltage or current sources are applied to the electrode surfaces. The active p–i–n region is modeled as a diode network distributed in two dimensions. The value of $R_{E,i,j,k}$ depends on both the conductivity and the dimension of a discretized volume. The material resistivity value of each epitaxial layer and the diode parameters can be experimentally extracted. Finally, the total equivalent circuit is solved by utilizing a circuit simulator like SPICE.

2.2. Thermal equivalent circuit

Spatial distributions of current and voltage can be used as the distributed heat sources in a high-power LED chip. The electrical circuit simulator can also be utilized to analyze the temperature distribution once the duality property between Fourier's law in thermal analysis and Ohm's law in electrical analysis is established.

Fourier's law represented in one dimension is

$$\dot{Q} = -A\kappa \frac{\mathrm{d}T}{\mathrm{d}x} \tag{1}$$

where $\dot{Q}$ is the heat transfer rate, A is the cross-sectional area, κ is the thermal conductivity, T is the temperature and x is the direction of heat transfer. This law means that the time rate of heat transfer through a material is proportional to the negative gradient of temperature and also to the area. On the other hand, Ohm's law is expressed in one dimension as

$$I = -A\sigma \frac{\mathrm{d}V}{\mathrm{d}x} \tag{2}$$

where I, σ and V are the current, the electrical conductivity and the electric potential, respectively. There exists an analogy between the heat transfer rate in (1) and the electrical current in (2). $\dot{Q}$, κ and T in the thermal circuit can be considered as

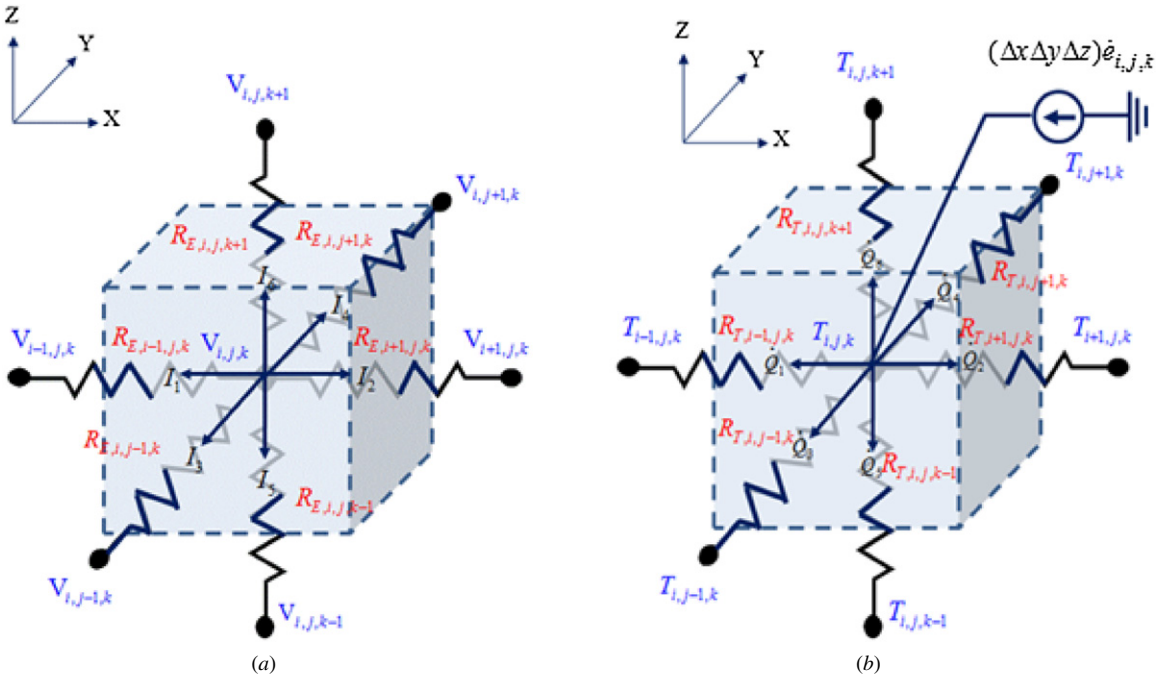

Figure 1. Mesh used for discretization of an LED: (*a*) an electrical equivalent circuit and (*b*) a thermal equivalent circuit.

I, σ and V in the electrical circuit, respectively. Therefore, the electric potential difference ΔV and the temperature difference ΔT between two adjacent positions are expressed by similar relationships of $\Delta V = IR_E$ in the electrical circuit and $\Delta T = \dot{Q}R_T$ in the thermal circuit, where R_E and R_T are electrical and thermal resistances, respectively.

The material is uniformly discretized with a volume of size Δx, Δy and Δz in x, y and z directions, respectively and the temperature $T(i\Delta x, j\Delta y, k\Delta z)$ at a node (i, j, k) is denoted as $T_{i,j,k}$. With the energy conservation law, we can represent one mesh in the steady state as

$$\dot{Q}_1 + \dot{Q}_2 + \dot{Q}_3 + \dot{Q}_4 + \dot{Q}_5 + \dot{Q}_6 = (\Delta x \Delta y \Delta z)\dot{e}_{i,j,k} \tag{3}$$

where $\dot{e}_{i,j,k}$ is the heat generation rate per unit volume inside a material. Since the term on the right-hand side of (3) represents the heat generation rate in a volume, each term on the left-hand side of (3) corresponds to a heat transfer rate. In this case, each heat transfer rate term can be represented as

$$\begin{aligned}
\dot{Q}_1 &= \kappa A_x (T_{i,j,k} - T_{i-1,j,k})/\Delta x \\
\dot{Q}_2 &= \kappa A_x (T_{i,j,k} - T_{i+1,j,k})/\Delta x \\
\dot{Q}_3 &= \kappa A_y (T_{i,j,k} - T_{i,j-1,k})/\Delta y \\
\dot{Q}_4 &= \kappa A_y (T_{i,j,k} - T_{i,j+1,k})/\Delta y \\
\dot{Q}_5 &= \kappa A_z (T_{i,j,k} - T_{i,j,k-1})/\Delta z \\
\dot{Q}_6 &= \kappa A_z (T_{i,j,k} - T_{i,j,k+1})/\Delta z
\end{aligned} \tag{4}$$

where A_x, A_y and A_z are $\Delta y \Delta z$, $\Delta x \Delta z$ and $\Delta x \Delta y$, respectively. Equation (4) can be rewritten as follows by using thermal resistances defined in (6):

$$\begin{aligned}
(\Delta x \Delta y \Delta z)\dot{e}_{i,j,k} = {} & \frac{T_{i-1,j,k} - T_{i,j,k}}{R_{T,i-1,j,k}} + \frac{T_{i+1,j,k} - T_{i,j,k}}{R_{T,i+1,j,k}} \\
& + \frac{T_{i,j-1,k} - T_{i,j,k}}{R_{T,i,j-1,k}} + \frac{T_{i,j+1,k} - T_{i,j,k}}{R_{T,i,j+1,k}} + \frac{T_{i,j,k-1} - T_{i,j,k}}{R_{T,i,j,k-1}} \\
& + \frac{T_{i,j,k+1} - T_{i,j,k}}{R_{T,i,j,k+1}}
\end{aligned} \tag{5}$$

where

$$\begin{aligned}
R_{T,i-1,j,k} &= \Delta x/(\kappa A_x) \\
R_{T,i+1,j,k} &= \Delta x/(\kappa A_x) \\
R_{T,i,j-1,k} &= \Delta y/(\kappa A_y) \\
R_{T,i,j+1,k} &= \Delta y/(\kappa A_y) \\
R_{T,i,j,k-1} &= \Delta z/(\kappa A_z) \\
R_{T,i,j,k+1} &= \Delta z/(\kappa A_z).
\end{aligned} \tag{6}$$

Then the heat transfer rate at a node (i, j, k) in (5) can be described by a thermal equivalent circuit as shown in figure 1(*b*). Next, we explain a calculation procedure for three-dimensional electrical and thermal distributions in an LED chip.

2.3. Analysis procedure for thermal distributions

Figures 2(*a*) and 3(*a*) schematically show the cross-sectional and top views of an InGaN/GaN MQW LED structure used in this study, respectively. Figures 2(*d*) and (*e*) are schematic representations of three-dimensional electrical and thermal equivalent circuits for the cross-sectional structure shown in figure 2(*a*), respectively. Different colors in figure 2 are introduced to identify different materials as indicated in figure 2(*c*). The layer representing air can be selectively changed to other materials to set up different boundary conditions if needed. In the electrical equivalent circuit, the active MQW layer is modeled by two-dimensionally distributed intrinsic diodes. Each epitaxial, metallic and dielectric layer consists of three-dimensional resistor networks as shown in figure 2(*d*). By analyzing the electrical equivalent circuit, we are able to find current and voltage distributions in the entire LED structure.

These current and voltage distributions are utilized to calculate the distributed heat transfer rate inside an LED structure except intrinsic diodes of the active MQW

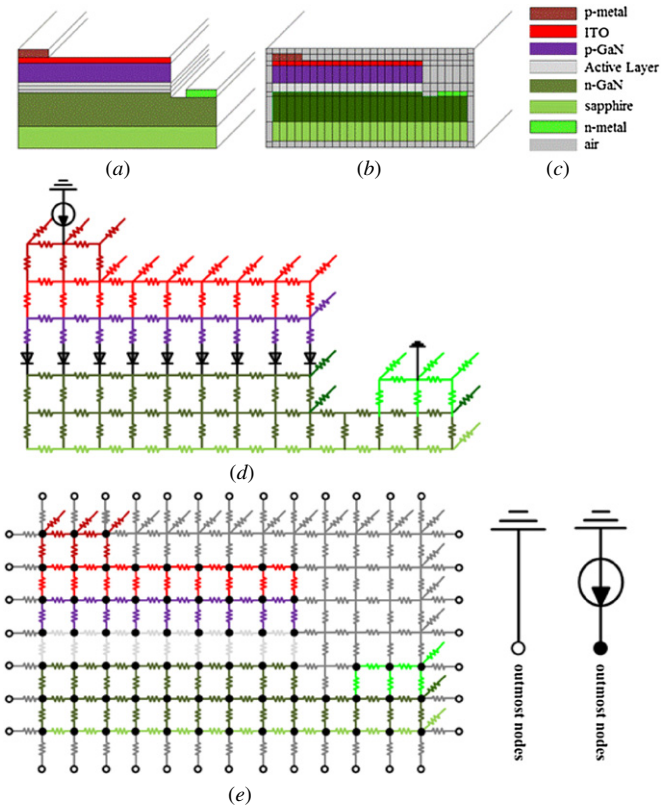

Figure 2. (*a*) A schematic cross-sectional view of an LED structure used in this study, (*b*) an LED divided into meshes, which is a first step for the thermal circuit modeling, (*c*) a color index representing different materials, (*d*) the electrical equivalent circuit model and (*e*) the thermal equivalent circuit model.

region. Total electric power applied to the intrinsic diode is converted to light and heat with the multiplication factors of $(h\nu/qV_d)\eta_{\text{internal}}$ and $(1 - (h\nu/qV_d)\eta_{\text{internal}})$, respectively, where η_{internal} is the internal quantum efficiency (IQE), $h\nu$ is the average photon energy and qV_d is the potential energy of the injected electrons. In other areas, almost all the electric power is consumed as Joule heat. The rate of Joule heat generation in a volume $\Delta x\Delta y\Delta z$ is $(\Delta x\Delta y\Delta z)\dot{e}_{i,j,k}$ in (3), which is expressed as a current source in the thermal network shown in figure 2(*e*). With these concepts, the value of $(\Delta x\Delta y\Delta z)\dot{e}_{i,j,k}$ is calculated as shown below except in the active MQW region:

$$(\Delta x\Delta y\Delta z)\dot{e}_{i,j,k} = I_1^2 R_{E,i-1,j,k} + I_2^2 R_{E,i+1,j,k} + I_3^2 R_{E,i,j-1,k} + I_4^2 R_{E,i,j+1,k} + I_5^2 R_{E,i,j,k-1} + I_6^2 R_{E,i,j,k+1}. \quad (7)$$

In the active MQW region, it is calculated by

$$(\Delta x\Delta y\Delta z)\,\dot{e}_{i,j,k} = \left[1 - \left(\frac{h\nu}{qV_d}\right)\eta_{\text{internal}}\right] I_{\text{d}} V_{\text{d}} \quad (8)$$

where I_d and V_d represent the current and the voltage applied to the intrinsic diode, respectively. In the thermal network representing the heat conduction and generation processes, resistors stand for thermal resistances. Also, terminations represented by small filled circles designate connections to heat sinks. Terminations represented by small open circles designate connections to current sources (shown as ground and current source in figure 2(*e*)). In practice, heat sources are set up at all nodes for our simulation.

Resistance values in the thermal network are determined by thermal conductivities of materials. Air or package materials surrounding the LED are taken into account in terms of thermal resistances by applying the boundary condition between the LED and the heat sink. Once the thermal network is established, we are able to analyze it with a conventional circuit simulator and obtain three-dimensional temperature distributions in an LED device.

3. Results and analysis

We prepared an InGaN/GaN MQW blue LED mounted on a TO-CAN package. The epitaxial layers were grown by the metal-organic chemical vapor deposition (MOCVD) on a sapphire substrate. The n-GaN, the active layer with five-period $In_{0.14}Ga_{0.86}N$/GaN MQWs and the p-GaN clad layer were grown in sequence. To deposit the metal as an n-electrode, etching process was performed until the n-GaN layer was exposed. The thin ITO film was used as a transparent metal electrode. Metallic films were used as p- and n-electrodes for wire bonding. The size of the LED chip designed was 1140 μm $\times$ 610 μm. Table 1 shows material and diode parameters extracted to model and analyze the electrical and thermal circuits. Diode parameters were extracted by measured current–voltage characteristics of the sample LED. Thermal conductivity, emissivity and transmittance values were obtained from relevant research papers and open data [16–18]. Low thermal conductivities of ITO and sapphire, negligible emissivities of ITO and gold, the high contact resistance between ITO and p-GaN are key numbers in table 1 because these parameters contribute to poor heat transfer via conduction or radiation. In this section, simulation and experimental results are shown and discussed when an injection current of 200 mA is supplied to the sample LED.

3.1. Verification of simulated current distribution

As a first step, we analyze the electrical equivalent circuit and obtain three-dimensional current and voltage distributions inside the LED chip. Since the two-dimensional light emission pattern measured from the surface is almost the same as the two-dimensional current distribution injected into the active MQW layer, the measured light emission pattern is compared with the calculated current distribution in order to verify our electrical circuit modeling and its analysis procedure [13–15].

Figure 3(*a*) shows a top view of the LED sample where the bright lines are p- and n-electrodes. The patterns shown in figures 3(*b*)–(*g*) are the top views of thin layers constituting the LED structure, i.e., the p-electrode pattern, the ITO layer, the p-GaN layer, the active layer and the n-electrode, the n-GaN layer and the sapphire substrate, respectively. Each layer is divided into meshes whose unit volume is 10 μm $\times$ 10 μm $\times$ thickness of each material. The total number of meshes created in this analysis is 41 724. Figure 3(*h*) shows the calculated current distribution on the active layer where both p- and n-electrode patterns are also displayed in order to compare it clearly with the experimental result. Current crowding is observed near the edge of the p-fingers.

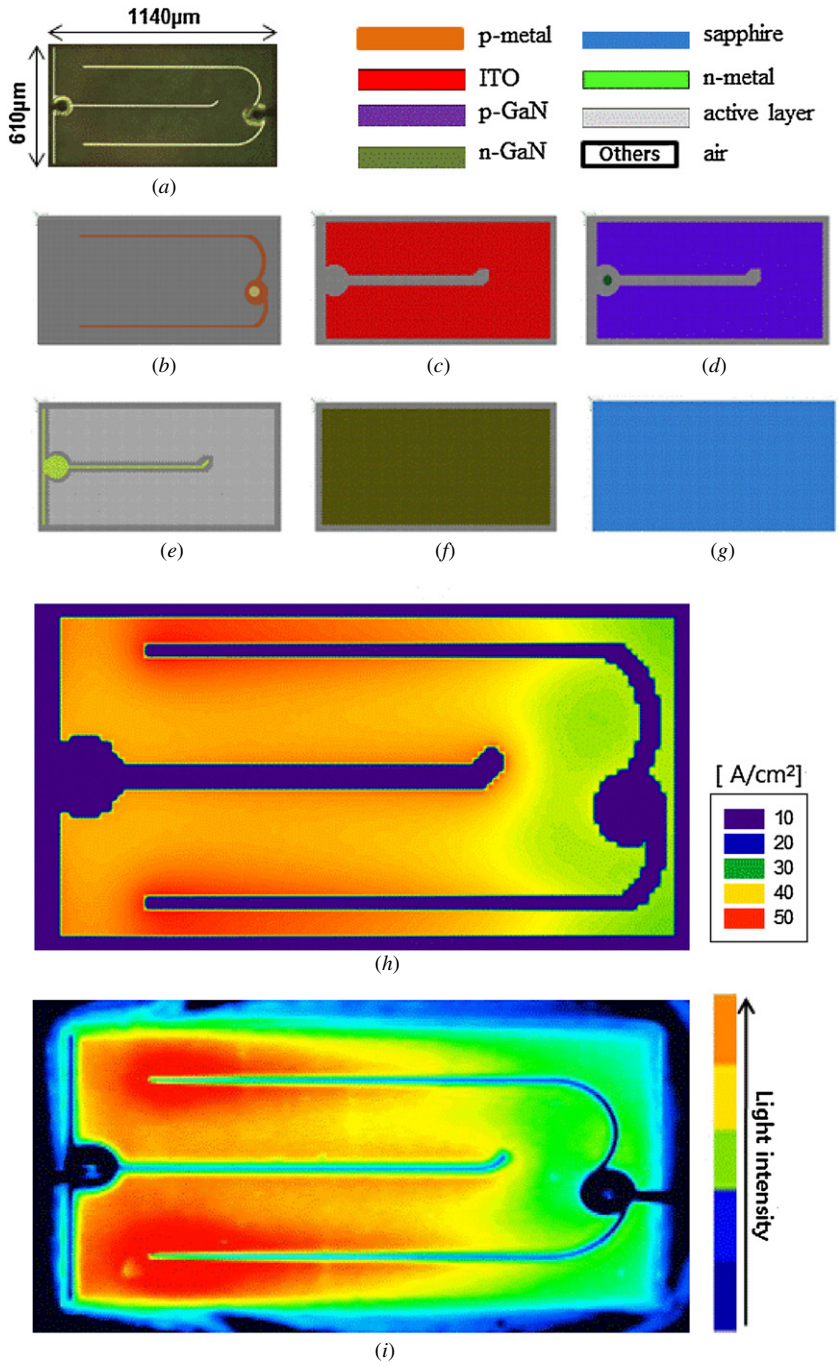

Figure 3. (*a*) A top view of the sample LED device with electrode patterns, used as a sample to test the modeling methodology. Top views of thin layers constituting the LED chip are shown sequentially, i.e., (*b*) the p-electrode, (*c*) ITO, (*d*) p-GaN, (*e*) the active layer/n-electrode, (*f*) n-GaN and (*g*) the sapphire substrate. Also shown are (*h*) calculated current distribution in the active layer when 200 mA is injected and (*i*) relative luminous intensity distribution observed by a CCD camera at the same injection current.

Table 1. Material parameters extracted and used in simulations. Ideality factor = 1.92. Reverse saturation current = 7×10^{-37} (A).

Material	Electrical resistivity (Ω cm)	Thermal conductivity (W/(°C cm))	Emissivity	Thickness (μm)	Transmittance of IR
Gold	1.0×10^{-7}	3.2	0.02	1	0.2
ITO	1.5×10^{-4}	1.1×10^{-1}	0.1	0.075	0.1
p-GaN	1.6	1.2	0.5	0.13	0.98
n-GaN	2.5×10^{-3}	1.2	0.5	4.5	0.98
Sapphire	–	4.2×10^{-1}	0.89	70	0.9
Air	–	2.5×10^{-4}	0.8	–	0.8
Contact	1.5×10^{-2} (Ω cm^2)		–	–	–

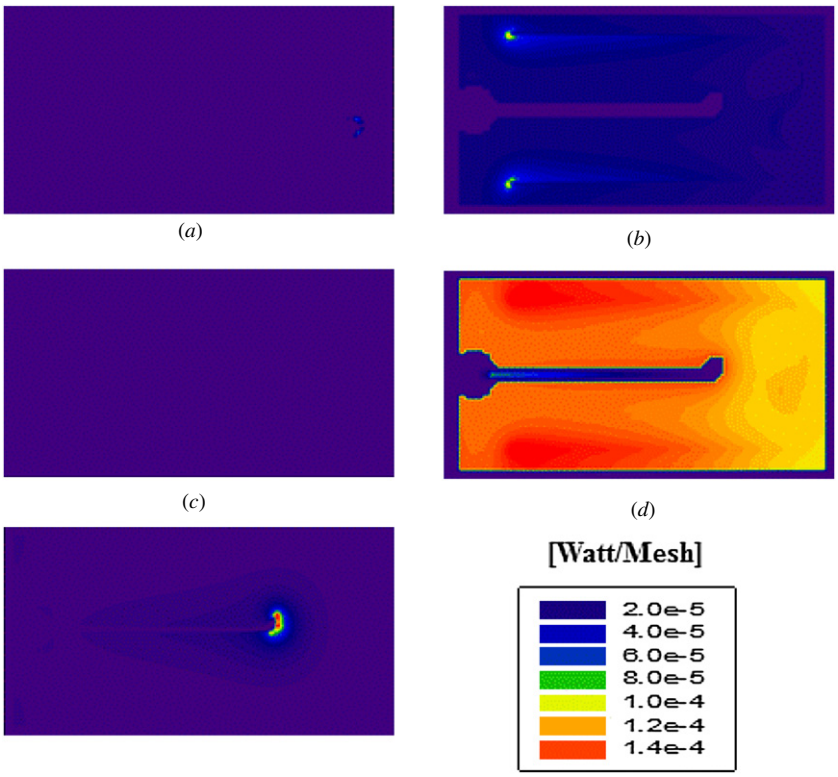

Figure 4. Calculated heat generation rate by Joule's law in (*a*) the p-metal, (*b*) ITO, (*c*) p-GaN, (*d*) the active layer/n-electrode and (*e*) n-GaN.

Figure 3(*i*) shows the relative luminous intensity distribution at the surface of the LED, which was measured by a charge-coupled-device (CCD) camera with a neutral-density (ND) filter. It is found that the calculated current distribution in the active layer shows a good agreement with the measured relative luminous intensity distribution.

3.2. Calculation of heat generation rate and its distribution

Figure 4 shows calculated distributions of heat generation rate at each epitaxial layer. Figure 4(*a*) shows the one at the p-metal layer. Due to the finite conductivity of the metallic film and a relatively large current density compared with the one at the other layers, the heat generation rate becomes large for the electrode area near the contact pad (still not so significant, though, as can be seen in figure 4(*a*)). Figure 4(*b*) shows the one at the ITO layer. When the sheet resistance of the ITO layer is larger than that of the n-GaN, most of the current flows in the vertical direction near the p-metal area than the mesa edge. The higher relative luminous intensity near the p-metal in figure 3(*i*) also indicates that this sample's lateral current flow in the ITO is not large. High localized heat generation rate near the end position of p-metal is a consequence of this current crowding near the p-metal shown in figures 3(*h*) and (*i*). Figure 4(*c*) shows the heat generation rate at the p-GaN layer. It is found that the heat generation rate is the smallest at the p-GaN layer. This is because the lateral current flow in the p-GaN layer is negligible and the vertical resistance is relatively smaller than those for other epitaxial layers due to its very small thickness. Figure 4(*d*) shows the heat generation rate at the active layer and the n-electrode. As the IQE can be defined as the ratio of the current contributing to the radiative recombination process to the total current injected into the active layer, the ratio of $(1 - \eta_{\text{internal}})$ among the total current is used as the heat generation there. In this calculation, a constant IQE of 40% is taken as a reasonable value for the simulation. This means that 60% of the total electric power delivered to the active layer is wasted as nonradiative recombination heat rather than light emission. The total electric power delivered to the active layer is calculated by the sum of the local electric power distribution. The heat generation at the active layer is the largest due to (i) a small IQE value, (ii) the voltage applied to the active layer being the largest and (iii) relatively small Joule heats at other layers. Lastly, figure 4(*e*) shows the heat generation rate at the n-GaN layer. Since the conductivity of n-GaN is finite and the lateral current is dominant, large Joule heating is observed especially at the current-crowded region. As the current is crowded the most near the end of the n-electrode, the heat generation rate there has the highest value in the calculated results of this sample.

3.3. Simulated temperature distribution

Heat generation rate values calculated in figures 4(*a*)–(*e*) are used as heat sources in the thermal circuit modeling based on the duality between Fourier's law and Ohm's law [19]. Heat generation by self-absorption of emitted blue light was omitted in this study with the following assumptions. First, if the self-absorption takes place near the active layer, which generates most of the heat, it should not affect the temperature

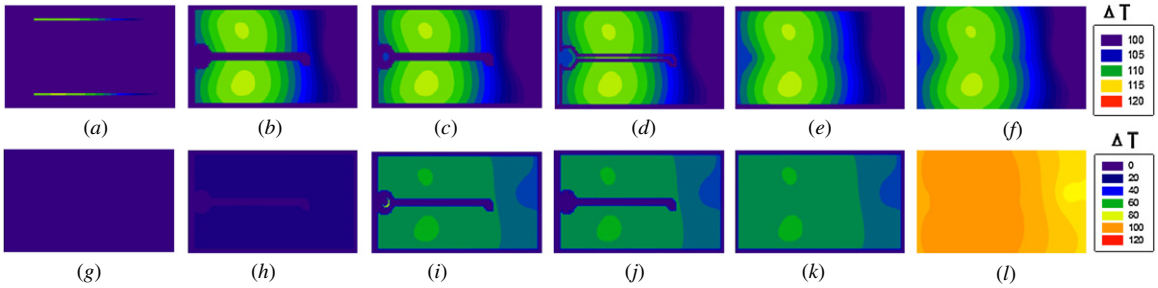

Figure 5. Temperature distributions at (*a*) the p-electrode, (*b*) ITO, (*c*) p-GaN, (*d*) the active layer/n-electrode, (*e*) n-GaN and (*f*) sapphire. Temperature distribution when the emissivity is applied to the results shown in (*a*)–(*f*): (*g*) the p-electrode, (*h*) ITO, (*i*) p-GaN, (*j*) the active layer/n-electrode, (*k*) n-GaN and (*l*) sapphire. All the results are drawn on the same temperature scale.

distribution much. Second, if the self-absorption takes place in random positions in an LED, it should not affect the temperature distribution much, either.

Since heat is nonuniformly generated in the whole LED structure due to the current crowding phenomenon, it is necessary to consider nonuniformly distributed heat sources in space. In fact, the temperature distribution is mostly determined by the large heat generating blocks and their heat spreading characteristics.

The results shown in figures 5(*a*)–(*f*) are temperature distributions at various layers. They show very similar distributions except for the p-metal and sapphire layers. There are two reasons for these phenomena. First, the thermal resistance of air is much larger than those of other materials. Second, the thickness of the LED chip is much smaller than its width and length and the vertical thermal resistance of the material is smaller compared to its lateral thermal resistance. Consequently, the temperature distribution at each layer is very similar and the heat is dissipated mainly through the sapphire substrate. By comparing the outer side in figure 5(*f*) with figures 5(*a*)–(*e*), one can see that the heat is flowing laterally at the sapphire substrate. A common feature in these results is the higher temperature on the left side than on the right side of the chip. This comes from the boundary condition for the p-contact pad, where a bonding wire to the package is attached (a dim outline of the bonding wire can be seen in figure 6(*a*)). This bonding wire provides an additional heat conduction path to the chip. The value used for the thermal resistance between the package heat sink and the p-pad was 8.8×10^4 °C W^{-1}. Also, the value of the thermal resistance between air and the chip was set up as 10^7 °C W^{-1}. The one between the sapphire substrate and the package was 8.8×10^5 °C W^{-1}.

Figures 5(*g*)–(*l*) are plots obtained after multiplying the emissivity values in table 1 to the temperature distributions of figures 5(*a*)–(*f*). The apparent temperature distribution obtained in this way is correlated with the IR intensity emitted by each epitaxial layer. The sapphire substrate seems to show higher temperature than the others because the emissivity values of metals and ITO are very low and that of sapphire is larger than those of GaN-based materials. These results with the emissivity values multiplied are used to obtain the apparent temperature distribution by the radiant heat at the LED surface after applying the transmittance values in table 1.

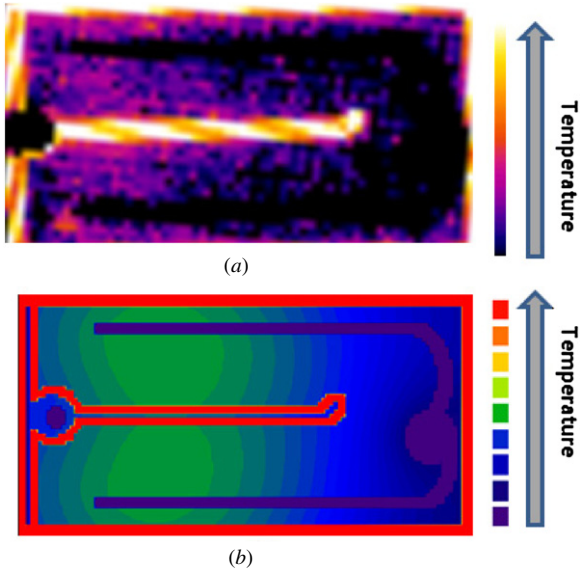

Figure 6. (*a*) Experimental result by an IR camera and (*b*) the simulated temperature distribution at the LED surface when emissivity and transmittance are applied.

3.4. Comparison of temperature distribution by radiated heat between simulation and experimental results

Figures 6(*a*) and (*b*) show the IR intensity distributions at the LED surface obtained by an FLIR A40 IR camera and from the simulation, respectively. The two results match quite well in the distribution tendency even though the image quality obtained by the IR camera is limited in resolution: It is seen that near the p-contact pad, both results show relatively low apparent temperature compared with the other areas. Although the etched mesa seems to show the highest apparent temperature from the experimental and simulation results, these results do not represent the actual temperature. The results mainly come from the ITO functioning as an IR radiation blocker, and the low emissivity and transmittance of metals.

3.5. Experimental and simulation results of current–voltage and junction temperature characteristics

Figure 7 shows experimental and simulated current–voltage characteristics of the LED sample under consideration. From

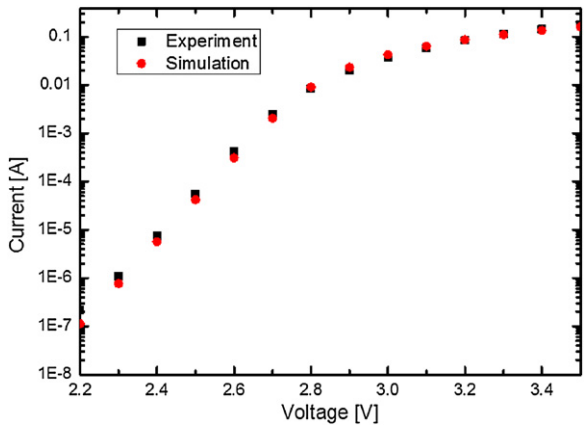

Figure 7. Current–voltage characteristics from the experimental and simulation results.

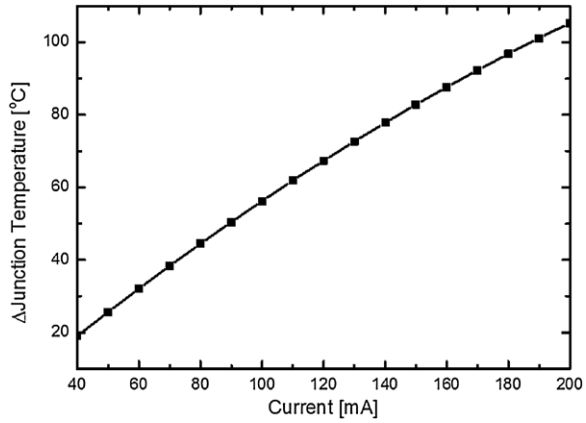

Figure 8. Junction temperature–current characteristics of the sample LED obtained from the diode forward voltage method.

these results as well as the ones shown in figures 3(*h*) and (*i*), we can confirm the effectiveness of the analysis based on the electrical circuit modeling. Figure 8 shows the experimental junction temperature–current characteristics of the sample LED obtained by using the conventional diode forward voltage method [6]. The junction temperature at an injection current of 200 mA is ∼105 °C in this experiment. The average temperature at the active layer calculated by our thermal circuit modeling is 104 °C with the boundary condition mentioned above. These results indicate that our thermal circuit modeling is valid and applicable to actual situations.

4. Conclusion

We have successfully obtained the current, voltage and temperature distributions by utilizing the electrical and thermal circuit modeling. Comparison of current and temperature distributions between the experimental and simulated results has shown a good agreement and demonstrated the effectiveness of our analysis method.

We believe that employing the methodology demonstrated in this paper can assist in designing the LED and package structures with better current spreading and heat dissipation. The techniques utilized in this paper can also be applied to other semiconductor devices with distributed heat sources caused by nonuniform current distribution.

Acknowledgments

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