Phys. Status Solidi A **208**, No. 6, 1433–1439 (2011) / **DOI** 10.1002/pssa.201000103

physica status solidi a
www.pss-a.com
applications and materials science

The use of porous silicon layers in thin-film silicon solar cells

Jan Van Hoeymissen*, Valerie Depauw, Izabela Kuzma-Filipek, Kris Van Nieuwenhuysen, Maria Recaman Payo, Yu Qiu, Ivan Gordon, and Jef Poortmans**

Solar Cell Technology Group, imec, Kapeldreef 75, 3001 Leuven, Belgium

Received 15 April 2010, revised 27 May 2010, accepted 28 May 2010
Published online 21 December 2010

Keywords bragg reflector, epifree, layer transfer process, porous silicon, silicon solar cells

* Corresponding author: e-mail vhoeymis@imec.be, Phone: +00 32(0)16 281 505, Fax: +00 32(0) 16 281 501
** e-mail vdepauw@imec.be, Phone: +00 32(0)16 288265

In the quest for lowering the manufacturing cost of silicon solar cells, imec has been working successfully on two crystalline Si 'thin-film' cell concepts. In a first concept, a 20 μm-thin Si solar cell is epitaxially grown on top of a porous Si-based Bragg-type reflector which is electrochemically etched in a low-cost UMG Si substrate. Large area solar cells with efficiencies of 15.2% have been made, using (semi-)industrial processing tools. This clearly demonstrates that this cell concept has almost reached the stage of industrial application. In a second, longer-term approach, a 1–5 μm-thin, stand-alone mono-crystalline film is created based on the controlled annealing of an ordered macroporous silicon layer (the 'Epi-free' process). With this very thin Si layer, a simple proof-of-concept solar cell has been made exhibiting an efficiency of 4%. By optimizing the cell process in terms of light trapping and passivation, efficiencies over 15% can be expected from this technology.

1 Porous silicon and thin-film silicon solar cells at imec

Today, one of the main objectives in the field of Si-based photovoltaics research is focused on lowering the consumption of high-quality silicon (g Si/W_p), since that would most efficiently reduce the cost of silicon solar modules. Therefore, many research labs are developing 'thin-film' (thickness active layer δ 50 μm) silicon solar cells, as alternative to standard wafer-based cells (thickness ≈200 μm).

At imec, two different thin-film approaches have been actively investigated the last few years, both based on the use of porous Si (PSi) layers. The latest results on these activities are presented here.

2 Embedded microporous Si reflectors for epitaxially grown solar cells

2.1 Introduction

Up to now, the majority of crystalline thin-film silicon cells are based on chemical vapour deposition (CVD) of silicon on a substrate. At imec, a process was developed to epitaxially deposit the active layer onto a cheap, low-quality silicon substrate. To limit the cost of epitaxial deposition, only 20 μm-thick active Si layers are grown. However, due to the low absorption coefficient of Si, this limited thickness introduces large optical losses, which can be reduced by implementation of an intermediate PSi-based reflector. The role of the porous reflector is to boost the low-energy photons trapping in the thin active layer, and therefore to increase the charge carrier generation and resulting efficiency of the solar cell device (Fig. 1). This cell concept and technology is already described elsewhere [1].

Due to the fact that the front surface of the cell is textured (using a fluorine-based plasma), the light entering the active layer is diffused in many angles causing both a Bragg reflection effect for the light impinging onto the reflector in a direction close to the normal, and a total internal reflection effect at angles above the critical angle.

At the same time, the porous Si structure also acts as a gettering site for impurities that originate from the low-quality substrate [1]. Studies showed that metallic contaminants react with Si dangling bonds, which are present on the internal surface of the nanometer-scale voids created within Si crystals. Contaminants are trapped by silicon dangling bonds during high thermal processes.

PSi multilayer reflectors were produced by electrochemical anodization of $10 \times 10\,cm^2$, highly B-doped silicon substrates (resistivity 0.005–0.02 Ω cm), using an electrolyte of 33 vol% hydrofluoric acid in water and ethanol. The PSi multilayer structures were obtained by changing the current

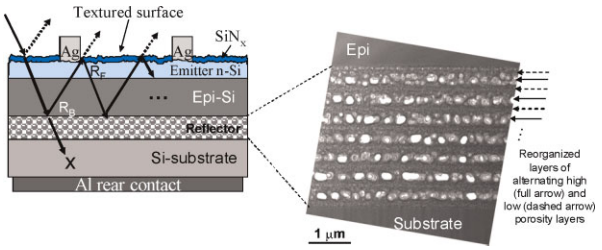

Figure 1 (online colour at: www.pss-a.com) Cross section of a thin-film epitaxial solar cell including the electrochemically etched, layered porous Si Bragg reflector after thermal reorganization.

density as a function of time during the electrochemical etching step. Typical values used during etching are: 6 mA cm^{-2} for about 10 s and 100 mA cm^{-2} for about 1 s. The multilayer stack produced in this way consisted of several PSi layers with alternating low/high/low porosities. The layer optical thicknesses were chosen according to the quarter-wavelength principle to promote constructive interference for the reflecting light at a target wavelength.

Electrochemically etched PSi is an optical active material which is easy to engineer, as well as compatible with the existing silicon solar cell technology. This multiple function of the porous silicon stack brings a significant added value to the industrial implementation of the porous silicon technology into thin-film Si solar cells.

2.2 Chirped porous Si reflectors As highly doped multicrystalline Si wafers are used as carrier substrate, sometimes the optical properties of the etched single mirror Bragg reflectors deviate from the designed properties, for they are sensitive resonant structures. This is due to the presence of various crystal grain orientations, surface roughness and variations in dopant concentrations. However, the resulting decrease in total reflection can be minimized and even avoided by using a linear or a 'segmented' type of chirped reflector [2], allowing a broader reflection bandwidth. In this concept the Bragg wavelength is designed not to be constant, but to intentionally vary within the porous stack. In this case, different wavelengths penetrate within the stack to different extents resulting in a wider reflection response than for the single wavelength Bragg reflector. This structure allows not only for reflection of lower energy photons that have reached deep sub-layers of the reflector stack, but also for less strict thickness preparation of the particular Bragg mirrors, making the technique more robust.

Up to now, most stable and best solar cell results have been obtained using a segmented chirped PSi reflector consisting of a total number of 36 PSi layers. The reflector is composed of nine subsequent wavelength mirrors or segments, each consisting of four layers (two periods). The total period thickness (summation of high and low porosity layer thicknesses) for each segment/mirror is increased from the previous one with a certain step size Δ. The theoretical response of the segmented chirped reflector with a step size

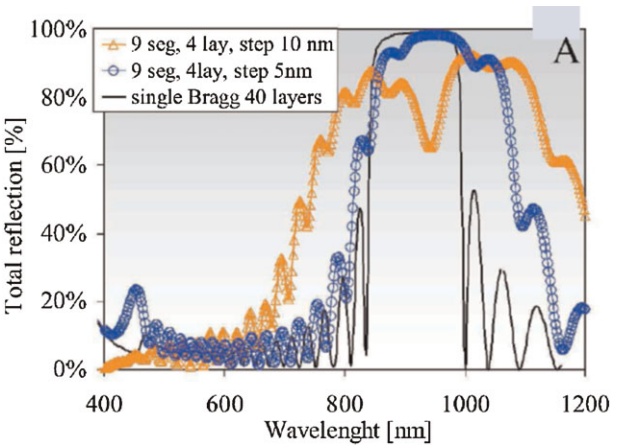

Figure 2 (online colour at: www.pss-a.com) Simulation of the total reflection for a segmented chirped PSi reflector of ~40 layers with 5 and 10 nm step size between each segment, in comparison with a conventional (single mirror) Bragg reflector of about the same amount of layers. (Calculated for normal incidence light).

Δ of 5 and 10 nm in comparison with the single mirror Bragg reflector consisting of a comparable amount of layers (40), is seen in Fig. 2.

The reflector with the nine segments and a step size Δ of 10 nm revealed also experimentally a much wider reflection bandwidth than the one with the step size of 5 nm, which was confirmed by measuring the reflector responses on solar cell level [2].

2.3 PSi reflector implementation and solar cell results After etching of the PSi stack into the substrate, a 30 min bake in H_2 atmosphere is applied at 1130 °C. During this baking step, PSi reorganizes into voids, preserving its multilayer structure and retaining the crystallographic information of the original substrate; at the same time the top PSi surface closes, creating an ideal surface for epitaxial silicon deposition. Then, an active silicon layer of about 20 μm is deposited using an epitaxial Si CVD process. This layer consists typically of a back surface field (BSF) (boron doping of around 10^{19} at. cm^{-3}) and a base (boron doping between 4 and 8 10^{16} at. cm^{-3}).

In the past, imec has reported on the use of linearly chirped reflectors boosting short-circuit current densities up to 2 mA/cm^2 in comparison to the cells with single mirror Bragg reflectors. Solar cell efficiencies were reached above 14% on large-area (78 cm^2) mc-Si offspec wafers with diffused emitters and screen-printed contacts [3].

More recently, cell were fabricated on comparable large-area mc-Si substrates, including the segmented chirped porous reflectors, using a stable and well established cell process at ISE (Fraunhofer Institute for Solar Energy Systems, Germany). This included emitter formation by $POCl_3$-based diffusion and metallization by photolithography and Ag electroplating. The best solar cell obtained had

Table 1 Best epitaxially grown solar cell results with an embedded segmented chirped porous Si reflector.

solar cell Si substrate	base thickness (μm)	J_{sc} (mA/cm^2)	Eff. (%)
multi-crystalline[a], large area (78 cm^2)	19	31.3	15.2
mono-crystalline, small area (4 cm^2)	25	34.6	16.9

[a]In collaboration with ISE.

an outstanding efficiency of 15.2% and a current density above 31 mA/cm^2 (see Table 1).

As a showcase, demonstrating the high potential of the epitaxially-grown thin-film solar cell concept, a 'rear emitter' epi cell was made at imec on a high quality mono-crystalline substrate including an embedded segmented chirped PSi reflector. The epitaxial stack on top of the reflector consists of a highly doped p-type BSF, a lowly doped emitter (doping concentration around 1×10^{18} at. cm^3 and a thickness of 2 μm), and a lowly doped n-type base (1×10^{16} at. cm^3). Random pyramids are used to texture the front surface. A front-surface field (FSF) is created by diffusion of phosphorus during the deposition of a $POCl_3$ oxide. The original base thickness was chosen to be 31 μm. The front surface random pyramid etching removed around 6 μm (average) of the base layer, ending up with an active base around 25 μm (Fig. 3).

This cell concept is designed to avoid low-quality epitaxial regions sometimes observed when growing on textured surfaces. Moreover, the thickness of the highly-doped region is minimized and a lowly doped emitter can be used. Furthermore, an n-type base will benefit from longer minority-carrier lifetime in comparison with its p-type sister. A FSF is made by $POCl_3$-based diffusion. Laboratory-type solar cells (2×2 cm^2) are made using high quality p$^+$ mono-crystalline substrates. Solar cell processing after texturing and emitter/FSF creation included passivation by thermal oxidation and metallization by lithography and evaporation.

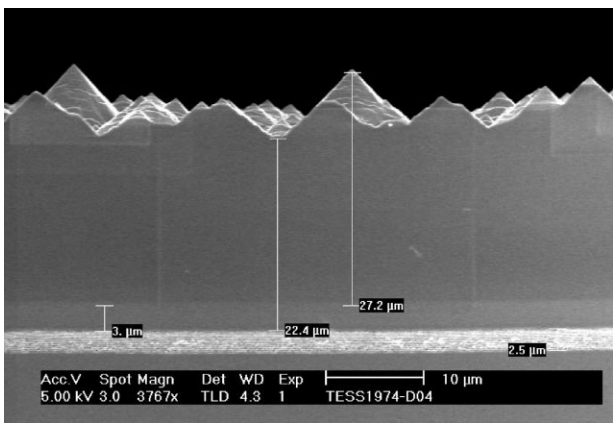

Figure 3 X-SEM image showing the cross-section of the full epitaxial stack for the high-efficiency rear-emitter solar cell. The porous Si Bragg reflector is visible at the bottom of the structure.

Very high current densities above 34 mA/cm^2 are obtained for this cell structure in combination with Voc's around 626 mV. A record cell with an efficiency of 16.9% is obtained (see Table 1). This illustrates the benefit of the n-type base and the exclusion of low-quality epi layers. Simulations show that, after optimization, cell efficiencies close to 18% are in reach, illustrating the high potential of epitaxially-grown solar cells including a PSi Bragg reflector.

2.4 Cost reduction potential The most recent discussion on economical aspects of the epitaxially grown Si thin film solar cell technology by Schmich et al. [15] predicts a total costs reduction advantage on cell level (including *in situ* grown emitters) of 0.24 €/W_p over the conventional industrial wafer cell technology. On the total module installation system, this difference was calculated to be of 0.12 €/W_p. The calculations show a significant advantage of crystalline thin film cell with *in situ* CVD emitters over the standard industrial mc-Si cell with a diffused emitter of 27%. The calculations also reveal that the energy payback time of the epitaxially grown Si thin film solar cell technology is almost 1 year shorter than the conventional Si cell technology.

2.5 Ageing study of as-etched PSi layers PSi in general is suffering from aging phenomena. The huge internal surface of the pores tends to be progressively oxidized or contaminated by impurities when in contact with air. The oxidation, in particular, leads to a lowering in the effective refractive index, with time, which is crucial for a photonic device [4]. The resonant nature of a PSi Bragg reflector is extremely sensitive to slight changes in n and is detuned easily due to oxidation. Moreover, adsorption and even capillary condensation of water can occur in nanopores with a hydrophilic surface, potentially affecting the Si epi CVD reactor hardware.

Since PSi ageing depends on specific storage conditions, porosity, substrate doping type and level, etc. [5]; it was decided to perform a PSi ageing assessment on our own p$^+$ mono-crystalline substrates, stored in the specific imec clean room conditions. The resulting information is useful to determine the best storage conditions and maximum storage time between PSi layer formation and further solar cell processing steps. PSi monolayers (porosities between 20 and 50%) were investigated as a function of storage time with ellipsometry, thermal desorption mass spectroscopy and ellipsometric porosimetry. The monitoring time frame was from minutes to months. Substrates were stored at room temperature in air and/or in a N_2-purged box.

While doing ellipsometry, it was ensured that always one and the same sample spot (0.1 mm accuracy) was investigated, in order to achieve comparable and consistent measurements. The variation of spectra obtained at the same time on different sample spots with a few mm distance can be as large as the ageing effects under consideration. For none

of the samples a significant change of the Δ and Ψ angles could be observed over a period of 5 months. The same observation was made during ellipsometric porosimetry on both fresh and aged samples: no adsorption or desorption of water vapour could be measured, nor any capillary condensation.

Thermal desorption mass spectroscopy confirmed the above observations. The desorption behaviour only changed to a very minor extent between fresh and old samples, independently of the storage conditions. This is illustrated in Fig. 4, showing the desorbed water vapour concentrations of both a one-week and six-month old sample. In both samples there is indeed some physisorbed water present; and there is slightly more in the oldest sample. But in absolute terms, the water concentration is still extremely low: about 0.007 monolayer in the fresh sample, and about 0.01 monolayer in the aged sample. On both samples, the Si–H and Si–H_2 signals (not shown on the graph) are clearly present and nearly identical, confirming that the –Si–H surface termination is still intact.

As a verification of the metrology used, the ageing process of a few PSi samples was accelerated by annealing the substrates at 700 °C for 4 h in an O_2 ambient. Measurements on these samples show that the Si pore surface is oxidized; no indications of the presence of a –Si–H terminated surface could be found.

As a conclusion, it is demonstrated that the mesoporous PSi layers etched in p^+ substrates have a hydrogen surface passivation which is stable for at least 5 months when stored at room temperature. Recently, similar findings have been observed by Ghulinyan et al. [4]. This information is essential for the industrial implementation of the PSi Bragg reflector in the thin-film Si solar cell technology.

3 Mono-crystalline epitaxy-free solar cells from macroporous silicon

3.1 Introduction The layer-transfer solar cell process under development at imec takes advantage on the properties of macroporous silicon to enable the transfer of a perfect ultra-thin layer of mono-crystalline silicon without resorting to epitaxial deposition. The empty-space-in-silicon concept on which it is based enables a unique combination of a high material quality with potentially very low fabrication costs. The concept, the current results and future developments are presented below.

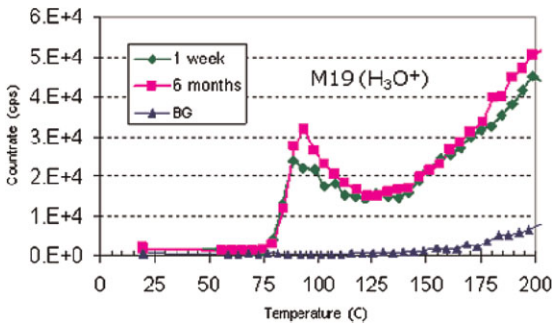

Figure 4 (online colour at: www.pss-a.com) Thermal desorption spectrum of mass 19 (proportional to the desorbed water vapour concentration) of both a 1 week and 6 month old PSi sample. In both samples the amount of physisorbed water is very low (see text).

3.2 The specific features of the Epifree process In typical layer-transfer processes, a thin sacrificial layer of micro or mesoporous silicon is detached from a thick wafer, transferred to a low-cost carrier substrate and used as a seed layer for the growth of a high-quality epitaxial silicon film grown by CVD [6]. High-efficiency solar cells, with a recent record of 17% [7], can be achieved with such method with less than 50 μm of material. Silicon epitaxy by CVD, which is necessary for growing a mono-crystalline material, is however, hindering the industrial development of these cells. The possibility to use microporous silicon itself as the active material of the cell, after a thermal treatment, was explored [8] but unfortunately the presence of pores strongly restrains the device efficiency. However, a perfect separation of pores and silicon is actually possible using the empty-space-in-silicon (ESS) concept developed by Toshiba [9]. In fact, macropores with specific dimensions close at high temperature, just as microporous silicon, and merge into a single void, leaving a micron-thin mono-crystalline silicon layer on top (Fig. 5a). With 'Epifree' we aim at using this mechanism for a new layer-transfer process that would enable to by-pass epitaxy and fabricate the cell directly inside the ultra-thin detachable overlayer.

Such a process can be divided into five main steps (Fig. 5b) and sets new challenges, amongst which the formation of centimeter-wide defect-free films, the handling

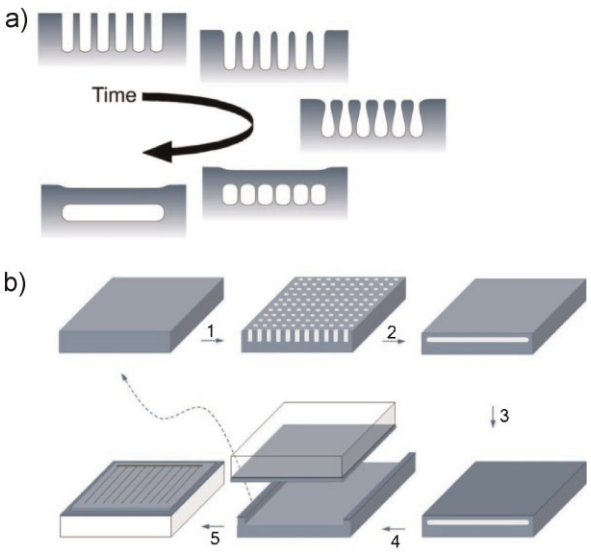

Figure 5 (online colour at: www.pss-a.com) (a) Pore reorganization and merging upon high-temperature annealing and (b) Epifree solar-cell process consisting of five steps of pore formation, annealing, processing of the first cell side, bonding to a low-cost substrate and processing of the second side of the cell.

of such ultra-thin film and the fabrication of highly efficient cells of a few microns only.

3.3 Current process and results The proof-of-concept of this process has been demonstrated by achieving simple solar cells of 2.6% first, and more recently 4.1%, energy-conversion efficiency with one micrometer of silicon only. The cornerstones of each of the five main process steps are described below.

3.3.1 Pore formation The creation of a uniform and detachable film requires etching of a perfectly uniform array of pores with specific dimensions. These dimensions of pore diameter d, length l, aspect ratio and pitch (distance between their centers) were studied in Ref. [10] and the way they influence the final void shape is illustrated in Fig. 6. For solar cells, a film with a thickness of a few micrometers is desirable and therefore we aim at large pores with a maximum pitch, about two times the diameter, so that the film thickness may be maximized. Since larger pores require longer annealing times, their diameter is limited by the thermal budget and should lie in the range of a few hundreds of nanometres.

In these first experiments to reach a proof of concept, the pore arrays were formed by deep-UV lithography followed by dry-etching in order to ensure a perfect control of the array (Fig. 7a). The hard-mask was formed in a 500-nm-thick thermal oxide capped with a 50-nm antireflective SiON coating. This mask was opened with a CF_4 plasma and the silicon pores were etched through it with a SF_6/O_2 plasma. After removal of the mask and cleaning, the wafers (20 Ωcm 200-mm Cz B-doped) were sent to the furnace.

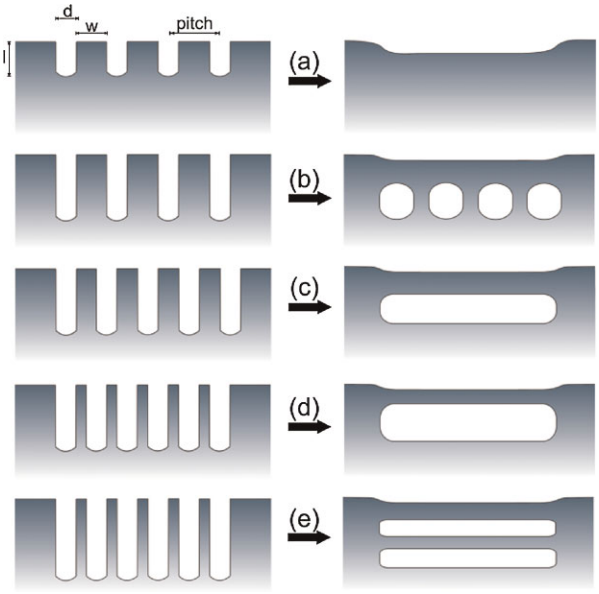

Figure 6 (online colour at: www.pss-a.com) Schematic of the influence of the initial pore morphology on the final ESS morphology: pore aspect ratio and pitch determine the shape of the void and the thickness of the silicon overlayer.

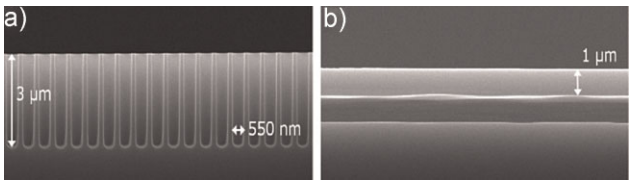

Figure 7 (a) Typical porous structure formed by DUV lithography and dry etching, with a diameter of 530 nm, and (b) its transformation into a floating 1-µm-thin film after annealing in hydrogen (10 Torr, 1150 °C, 60 min).

3.3.2 Annealing Reorganization of cylindrical pores into spheres requires conditions that enable self surface diffusion of silicon atoms, and should therefore take place over 1000 °C in a non-oxidizing ambient. A reducing hydrogen atmosphere or an inert atmosphere of argon can be used, provided that no traces of oxygen or water are present, which would lead to non-uniform etching and formation of defects (e.g. pits or holes in the film) [11]. In well-controlled atmospheres, perfect films as wide as 200-mm wafers were obtained. The film resulting from the reorganization of our pores was one micrometer-thin (Fig. 7b) and was formed by annealing in hydrogen at 1150 °C.

To ensure full wafer reorganization, the high temperature was kept for 45 to 60 min. The higher the temperature and the lower the pressure, the faster pores close. After closure, to avoid collapsing and resealing of the film onto its parent wafer, atmospheric pressure must be returned at a sufficiently low temperature. The film formed in this way is floating but sufficiently stable not to lift-off and can further be processed.

3.3.3 Front-side processing To develop high-efficiency cells, processing both sides of the film is necessary, and therefore the stability of the floating film on its parent was tested. The film proved to be sufficiently stable under certain process conditions that avoid strong pressure differences between the gas inside the void and the ambient. In practice the film was subjected to deposition of hydrogenated amorphous silicon in a plasma-enhanced CVD (PE-CVD) system and to e-beam evaporation of aluminium and could withstand a vacuum as low as 10^{-6} mbar (10^{-4} Pa) provided that it was reached sufficiently slowly, in 1 h. Wet etches, on the other hand, like piranha clean ($4\,H_2SO_4$:H_2O) or diluted-HF dips, should be kept very short, for the liquid might enter the void under the film and lift it off. The floating film can hence be processed under limited conditions but, to avoid any risk of lift-off, the development of a temporary bonding technique would be preferable.

3.3.4 Bonding After processing of its front side, the film can permanently be bonded to a foreign carrier substrate and detaches by itself from its parent wafer, revealing its rear side. The choices of bonding technique and carrier substrate determine the following process limitations. In the current

stage of development, the film is transferred to a glass substrate by anodic bonding. The latter technique has the advantages of providing bonds that resist high temperatures, a wide range of chemicals, and is direct, thus avoiding contamination problems that can arise from the presence of a gluing agent. A problem that is under investigation though is the creasing of the film, which often leads to formation of cracks during the following processes of the rear side.

3.3.5 Rear-side processing The use of a low-cost foreign carrier substrate, such as glass or plastic, limits the processes that follow bonding to low temperatures and, therefore, the solar cells are prepared with a hetero-junction emitter of hydrogenated amorphous silicon (aSi:H), instead of a standard diffused emitter (Fig. 8). The details of the proof-of-concept process can be found in Ref. [12] and the first basic cells reached 2.6% energy-conversion efficiency. These cells of only 1 μm, featured a good short-circuit current (Jsc) of almost 14 mA/cm^2 without light trapping, but suffered from a low open-circuit voltage (V_{oc}) of 340 mV, due most likely to the low material doping and to the absence of rear-surface passivation.

Therefore, in a later stage, a thin layer of i/p$^+$ aSi:H of 10 and 20 nm respectively, has now been applied to the film to passivate its top surface, before bonding (in step 3 of Fig. 5b), providing a rear-surface passivation to the cell.

The V_{oc} improved to 430 mV, increasing the efficiency to 4.1% (Fig. 9). This V_{oc}, although significantly improved, is still rather low for a hetero-junction cell and the reasons are being investigated. Direct contact of aSi with aluminium, which is known to induce crystallization of aSi at temperatures as low as 170 °C, and anodic bonding, which subjects the cell to 250 °C and 1000 V for 10 min, are two probable factors.

3.4 Present and future developments To go beyond the present achievement of proof-of-concept solar cells, additional demonstrations in terms of cost and cell efficiency will have to be achieved in the future. On the short term, the cell efficiency is being increased by developing efficient surface passivation and by increasing the material thickness to a theoretical maximum of 3 to 5 μm. In parallel, to demonstrate the low-cost potential of this process, the expensive deep-UV lithography, which is required to achieve sufficiently regular pore arrays, is being replaced by nano-imprint lithography (NIL) [13]. NIL could in fact be used in combination with anodization to form perfectly

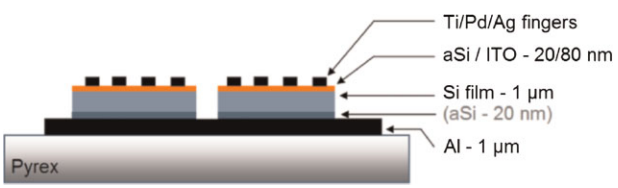

Figure 8 (online colour at: www.pss-a.com) The current simple cell structure with a hetero-junction emitter. The rear-side of the cell corresponds to the front-side of the film.

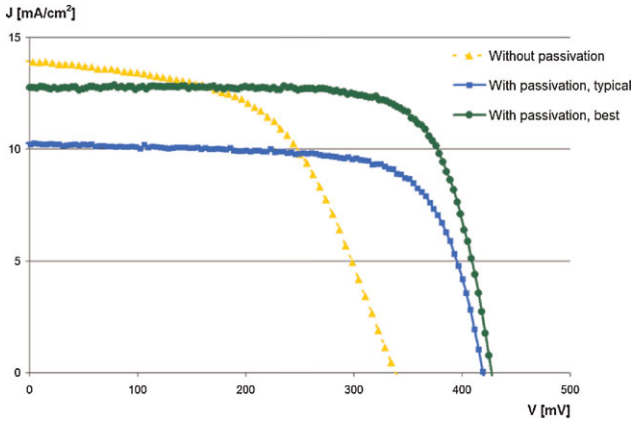

Figure 9 (online colour at: www.pss-a.com) Current density vs. voltage curves of a typical and best Epifree cells with rear-surface passivation compared to a typical cell without, displaying an increase in V_{oc}.

controlled and regular macro-pores by pre-patterning the surface and thus guiding pore nucleation [14]. Without pre-patterning, random pores lead to defected and non detachable films.

On a longer term, light-trapping schemes such as plasmonic structures or photonic crystals will have to be implemented inside more complex cells in order to push their efficiency towards 16%. Finally, the re-usability of the substrate will be essential and the effect of multiple annealings on the lifetime of the parent wafer will have to be investigated.

For all of these reasons, the maturity of the Epifree solar cell process is far from being reached. Therefore, it is currently not possible to give an estimation in terms of cost. In terms of silicon consumption however, it is possible to make a comparison with the current wafer-based technologies. If a cell efficiency of 16% could be reached, the Epifree process would present a radical reduction of the amount of used silicon per Watt-peak. In fact, current typical industrial cells of 16% are made using 200 μm-thick wafers. Each of these wafers generates 200 μm of Si loss due to wire sawing. Epifree, with an estimated silicon consumption of 10 μm would lead to a reduction by a factor 40, that is 0.2 g/W$_p$ instead of 8–9 g/W$_p$.

Acknowledgements The financial support from the European Community is acknowledged under the FP6 project SES6-CT 2003-502583 (Crystal Clear). ISE Freiburg for the help in processing the small-area epi solar cells. Dr. Guy Vereecke (imec) for performing the TDS-MS measurements on the PSi samples. Dr. Mikhail Baklanov for performing the ellipsometric porosimetry measurements on the PSi samples.

References

[1] I. Kuzma-Filipek, F. Duerinckx, K. Van Nieuwenhuysen, G. Beaucarne, J. Poortmans, and R. Mertens, Phys. Status Solidi C **6**(7), 1745–1749 (2009).

[2] I. Kuzma-Filipek, K. V. Nieuwenhuysen, J. Van Hoeymissen, M. R. Payo, E. V. Kerschaver, J. Poortmans, R. Mertens, G. Beaucarne, E. Schmich, S. Lindekugel, and S. Reber, Prog. Photovolt.: Res. Appl. **18**, 137–143 (2010).
[3] I. Kuzma-Filipek, K. Van Nieuwenhuysen, J. Van Hoeymissen, G. Beaucarne, J. Poortmans, and R. Mertens, IEEE Electron Device Lett. **30**(5), 499–501 (2009).
[4] M. Ghulinyan, B. Gelloz, T. Ohta, L. Pavesi, D. J. Lockwood, and N. Koshida, Appl. Phys. Lett. **93**, 061113 (2008).
[5] G. Amato, C. Delerue, and H. J. von Bardeleben (Eds.), Structural and Optical Properties of Porous Silicon Nanostructures (Optoelectronic Properties of Semiconductors and Superlattices, Vol. 5 (CRC Press, Amsterdam, 1998), p. 452.
[6] R. Brendel, Jpn. J. Appl. Phys. **40**, 4431–4439 (2001).
[7] M. Reuter, W. Brendle, O. Tobail, and J. H. Werner, Sol. Energy Mater. Sol. Cells **93**, 704–706 (2009).
[8] T. Rinke, R. Bergmann, and J. Werner, Appl. Phys. A **68**, 705–707 (1999).
[9] I. Mizushima, T. Sato, S. Taniguchi, and Y. Tsunashima, Appl. Phys. Lett **77**, 3290–3292 (2000).
[10] T. Sato, I. Mizushima, S. Taniguchi, K. Takenaka, S. Shimonishi, H. Hayashi, M. Hatano, K. Sugihara, and Y. Tsunashima, Jpn. J. Appl. Phys. **43**, 12–18 (2004).
[11] V. Depauw, I. Gordon, G. Beaucarne, J. Poortmans, and R. Mertens, J. Appl. Phys. **106**, 033516 (2009).
[12] V. Depauw, I. Gordon, G. Beaucarne, J. Poortmans, R. Mertens, and J.-P. Celis, Mater. Sci. Eng. B **159**, 286 (2009).
[13] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, J. Vac. Sci. Technol. B **14**, 4129 (1996).
[14] V. Lehmann and U. Grüning, Thin Solid Films **297**, 13–17 (1997).
[15] E. Schmich, H. Prigge, T. Friess, and S. Reber, 23rd EUPVSEC (WIP-Renewable Energies, Valencia, Spain, 2008).