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THE EFFECT OF Ti:W BARRIER METAL ON CHARACTERISTICS OF PALLADIUM-SILICIDE SCHOTTKY BARRIER DIODES

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The values of diode-quality factor and reverse-current leakage of Au/Pd/Ti:W/Pd_2Si/nSi unguarded Schottky barrier diodes are much higher than expected from silicide/silicon junction-radius induced high-field effects. Experimental Ti-, W-, and Ti:W-MIS structures were built and tested to show that Ti is responsible for the formation of a parasitic Ti-MIS structure around the unguarded-diode perimeter. This parasitic structure is responsible for excessive current leakage and also for an additional unguarded-diode degradation induced by annealing at 400°C.

Key words: palladium-silicide/titanium:tungsten metallization, palladium-silicide Schottky diodes, Schottky diode current leakage.

Introduction

A sandwich metallization composed of Au/Pd/Ti:W/Pd_2Si is one of the advanced schemes used in high-performance bipolar integrated circuits. The gold layer ensures high electrical conductivity. The Ti:W layer with 10 wt.% Ti provides for the adhesion of gold to the silicon dioxide and forms a barrier against the diffusion of gold into the silicon. The Pd_2Si layer makes a good rectifying contact to lightly doped n-type silicon. It also forms a good tunneling low-resistance contact

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to heavily doped silicon of either conductivity type. The thin Pd layer between Au and Ti:W is needed to further enhance the stability of the system and to provide an oxide-free surface for the Au plate-up process. The Pd_2Si layer is formed by dc magnetron sputtering of 100 Å Pd followed by a silicide formation at 400 °C in N_2/H_2 forming gas. Unreacted Pd is removed in an NH_4I/I_2 solution. The Ti:W and Pd layers are then deposited subsequently by dc planar magnetron sputtering in argon at 6 mtorr. The gold layer is electroplated in a potassium gold cyanide solution. The Au/Pd/Ti:W/Pd_2Si scheme offers moderate chemical stability, high electromigration resistance, and low electrical resistance. It is capable of handling current densities higher than 10^6 A/cm^2 without degradation and is stable up to 400 °C for long periods of time. This thermal stability is essential when NiCr or SiCr resistors are incorporated onto the same chip in bipolar analog circuits, since these resistor materials require 400 °C anneals in air for a period of a few hours to stabilize their properties. The 400 °C H_2/N_2 forming-gas anneals are also required to recover the gain of transistors damaged during various steps of the deposition processes. Figure 1 shows the cross-sectional diagram of the Au/Pd/Ti:W/Pd_2Si metallization scheme.

Although this metallization appears to be ideal, problems arise in fabricating unguarded Schottky barrier diodes (USBD). The quality factor of these diodes significantly exceeds unity, and their reverse-current leakage is much greater than expected from ideal Pd_2Si/nSi Schottky barrier diodes (SBD). It is shown that a parasitic low barrier-height titanium-silicide/oxide/nSi diode is responsible for this excessive current leakage. This metal/insulator/semiconductor (MIS) diode forms around the perimeter of the Ti:W/Pd_2Si/nSi USBD. The further degradation of USBDs observed after a thermal anneal at 400 °C is attributed to the reduction of the interfacial oxide thickness of the parasitic MIS diode. This thickness reduction is a result of the interaction between Ti and interfacial SiO_2.

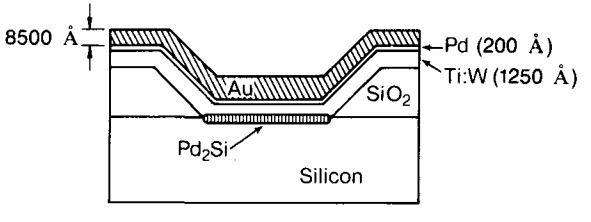

Fig. 1. Au/Pd/Ti:W/Pd_2Si metallization scheme.

Characteristics of Unguarded Au/Pd/Ti:W/Pd_2Si/nSi Schottky Barrier Diodes

All diode characteristics shown in this paper were measured under dark conditions using a Tektronix 4052 computer-based data-acquisition system. The measured diodes were biased using a Keithley 220 programmable current source. A Fluke 6502 multimeter was used to measure the device bias voltage via the Keithley 220. The forward and reverse currents were stepped from the lowest to highest values measured and, in all cases, the forward I-V characteristics were measured first.

Figure 2 shows typical experimental I-V curves of Au/Pd/Ti:W/Pd_2Si/nSi USBDs before and after a 4-hr anneal in forming gas as solid and broken lines, respectively. It also shows simulated I-V curves of ideal guarded and unguarded Pd_2Si Schottky barrier diodes for comparison. The I-V curves of the guarded diode (GSBD) were calculated from

$$I = SA^{**}T^2 \exp\left(\frac{-\phi_B}{kT}\right)\left[\exp\left(q\,\frac{V-IR_s}{kT}\right)-1\right] \tag{1}$$

where S is the diode area, A^{**} is the effective Richardson's constant, R_s is the diode series resistance, V is the applied voltage, ϕ_B is the barrier height corrected as in [1]

$$\phi_B = \phi_{Bo} - \alpha E_{\max} - \sqrt{\frac{qE_{\max}}{4\pi\varepsilon_s}} \tag{2}$$

where ϕ_{Bo} is the intrinsic barrier height of the Pd_2Si/nSi junction (0.745 eV), α is the field-penetration parameter [1], and $E_{\max}$ is the maximum junction field calculated from

$$E_{\max} = \left|\frac{-qN_d w}{\varepsilon_s}\right| \tag{3}$$

where N_d is the concentration of carriers and w is the depletion-layer width.

The first field-dependent term on the right side of (2) represents the barrier lowering due to penetration of the wave functions of the conduction electrons in the metal-silicide into the semiconductor [1].

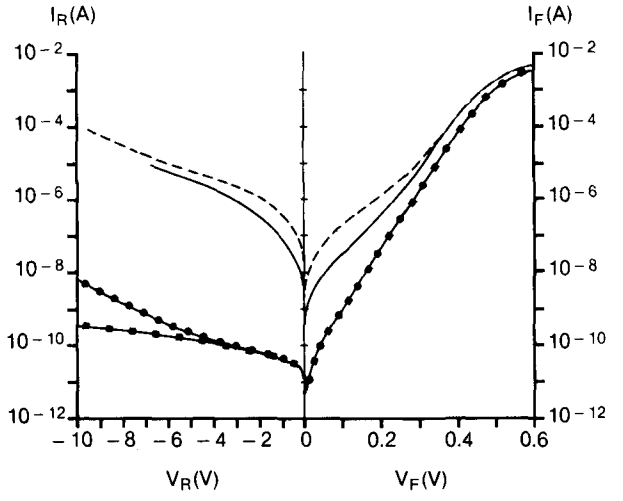

Fig. 2. Experimental and ideal I-V curves of Au/Pd/Ti:W/Pd_2Si/nSi Schottky barrier diodes: ——— experimental before anneal; — — — experimental after 4-hr anneal at 400 °C in H_2/N_2 forming gas: —●—●— simulated unguarded Pd_2Si/nSi and —■—■— simulated guarded Pd_2Si/nSi diodes using $\alpha = 2.45$ nm, $r_j = 34.2$ nm, $\phi_{Bo} = 0.743$ eV, $N_d = 2 \times 10^{16}$ cm^{-3}.

The second barrier-lowering term results from barrier lowering due to the image force [2].

In calculations of I-V curves of USBDs, the effect of silicide-junction radius has been taken into account [3]. The current enhancement due to the junction curvature is calculated from

$$I_e = \frac{\pi r_j}{2} LA^{**}T^2 \exp\left(\frac{-\phi_{Be}}{kT}\right)\left[\exp\left(q\,\frac{V - I_e R_e}{kT}\right) - 1\right] \tag{4}$$

where L is the diode perimeter, R_e is the spreading resistance of the perimeter portion of the diode, and

$$\phi_{Be} = \phi_{Bo} - \alpha \left| E(r_j) \right| - \sqrt{\frac{qE(r_j)}{4\pi\varepsilon_S}} \tag{5}$$

The value of the maximum field at the junction edge is calculated from

$$E(r_j) = -\frac{qN_d}{2\varepsilon_s}\frac{\Delta r(2r_j+\Delta r)}{r_j} \tag{6}$$

where r_j is the radius of the silicide edge and Δr is the depletion width near the diode perimeter. In the first approximation, the diode edge radius is considered to be equal to the depth of the silicide [3]. The characteristic shape of the I-V curve of the ideal unguarded silicide-silicon junction is seen in Fig. 2. Under reverse-bias conditions, the difference between the I-V curves of ideal guarded and unguarded diodes is large. Under forward-bias conditions, this difference is minimal.

The I-V curves of the ideal and experimental unannealed diodes deviate significantly. The diode-quality factor of the experimental diode significantly exceeds unity and, in the reverse-current direction, the diode is very leaky. Neither the high value of the diode-quality factor nor the excessive reverse-current leakage can be attributed to the silicide-junction curvature. The barrier height determined from the forward I-V curve is much lower than the 0.74 eV of the Pd_2Si/nSi junction. After a 4-hr anneal in N_2/H_2 forming gas at 400 °C, the diode degrades further, resulting in more leakage in both current directions.

Degradation Mechanism—Theory

The results from experimental diodes imply that, besides thermionic emission over the Pd_2Si/nSi barrier, some additional carrier-transport mechanism contributes to the current of the Ti:W/Pd_2Si/nSi USBD in both bias directions. Studies of the forward log(I) versus 1/T Arrhenius plots [4] obtained from experimental USBDs did not indicate any significant current contributions from recombination of the carriers within the depletion region or from quantum-mechanical tunneling across the Pd_2Si/nSi junction [5]. The low values of barrier height determined from these diodes suggest that some metal other than Pd_2Si forms a parasitic low barrier-height diode conducting in parallel with the main palladium-silicide SBD. The variability of this barrier height indicates that either the area of this parasitic diode or its barrier height, or perhaps both, are variable. The Ti component in particular is suspected to form a low barrier-

height MIS diode at the perimeter of the unguarded diode. This can also explain the variability of the barrier height of the parasitic diode, since the barrier height of the MIS diode depends on the thickness of the interfacial oxide. The thin oxide between the silicon and the metal has the ability to passivate the silicon surface and thus reduce the density of interfacial states. As a result, the barrier height of the Schottky barrier diode is determined strongly by the differences between the silicon and metal work functions [6]. For low work-function metals, such as titanium for example, the barrier height of the MIS diode can thus be lower than that of a Schottky diode that has no interfacial layer.

The MIS-diode formation results because the Pd_2Si forms only where the interfacial oxide between Pd and Si is thinner than 2 nm. At the diode perimeter, where the oxide thickness exceeds 2 nm, the Ti:W/SiO_2/nSi MIS structure forms. This is schematically represented in Fig. 3. The effect of the 400 °C thermal anneal on I-V curves can be explained in terms of a reaction between the thin SiO_2 and the Ti. Kräutle *et al.* report [7,8] that Ti reacts with SiO_2 to form a titanium-silicide layer having a ratio of Si:Ti = 0.62 and titanium oxide of unknown stoichiometry above 700 °C. This silicon-to-titanium ratio corresponds to Ti_5Si_3 [8,9], which is a known titanium-silicide phase. The evidence that a similar reaction also occurs at a much slower rate at 400 °C is presented by Drobny *et al.* in [10]. The same has also been observed by Ting *et al.* [11], who determined from leakage-current measurements of Ti-MOS capacitors that this reaction starts at 400 °C. For thermodynamic reasons, no reaction between the W component of Ti:W and SiO_2 is expected. By using the data and methods from Pretorius *et al.* [12], the following heats of formation for potential reactions between W and SiO_2 have been calculated and are given in Table I.

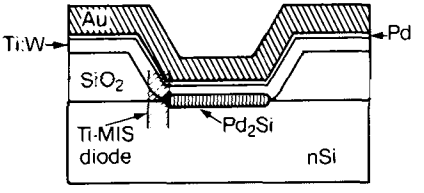

Fig. 3. Location of parasitic Ti-MIS diode.

Table I. Heats of formation values for a W-SiO_2 system.

$8W + 3SiO_2 \longrightarrow W_5Si_3 + 3WO_2 \ldots\ldots \Delta H° = +9.8$	kcal/gatom
$37W + 15SiO_2 \longrightarrow 5W_5Si_3 + 6W_2O_5 \ldots. \Delta H° = +10.4$	kcal/gatom
$7W + 3SiO_2 \longrightarrow W_5Si_3 + 2WO_3 \ldots\ldots \Delta H° = +10.9$	kcal/gatom
$3W + 2SiO_2 \longrightarrow WSi_2 + 2WO_2 \ldots\ldots \Delta H° = +12.9$	kcal/gatom
$13W + 10SiO_2 \longrightarrow 5WSi_2 + 4W_2O_5 \ldots\ldots \Delta H° = +13.7$	kcal/gatom
$7W + 6SiO_2 \longrightarrow 3WSi_2 + 4WO_3 \ldots\ldots \Delta H° = +14.5$	kcal/gatom

Since the values of the heat of formation for all the above reactions are positive, none of them are expected to occur. The last three reactions should not be considered, since there is sufficient evidence that a typical product of the reaction between reactive-transition metal and silicon dioxide is a metal-rich silicide, such as Ti_5Si_3 or V_3Si for example [8,12,13]. The reaction between Ti and SiO_2 is thermodynamically possible. The heats of formation for reactions between Ti and SiO_2, considering the metal-rich silicide Ti_5Si_3 as the product, were calculated to be $-10.5 < \Delta H° < -16.6$ kcal/gatom, depending on the final titanium-oxide composition. These theoretical results were found to be in perfect agreement with experiments described later and also in the literature [7,8,10–12].

Degradation Mechanism—Experiments

The Ti component of Ti:W diffusion-barrier metal is suspected to cause degradation of the Au/Pd/Ti:W/Pd_2Si/nSi USBD. It is blamed for the formation of a low barrier-height parasitic MIS diode and also for the diode degradation induced by a thermal anneal at 400 °C.

To confirm this, experimental discrete Pd_2Si/nSi diodes were made with the Ti:W replaced by a high work-function metal, such as Pd, which should eliminate the formation of the low barrier-height parasitic MIS diode. The experimental diodes were made using 0.25 ohm-cm (111) oriented wafers, thermally oxidized to grow ≈800 nm of oxide. Schottky barrier diode oxide windows 13 μm in diameter were defined using standard optical photolithography. Approximately 12 nm of palladium was then deposited on the wafers by dc-magnetron sputtering. The palladium-silicide layer was formed by heating the wafers at 400 °C for 15 min; the metal that remained unreacted on top of the

oxide was chemically removed. Approximately 120 nm of Pd was then sputtered and patterned to form overlapping contacts for device probing. Sputtered gold was used for the backside contacts. The device structure is shown in Fig. 4. The forward and reverse I-V characteristics of a typical $Pd/Pd_2Si/nSi$ diode are shown in Fig. 5. The I-V characteristics of an ideal 13-μm diameter Pd_2Si/nSi USBD, also displayed in Fig. 5, were simulated using (4–6) and [3] and assuming $\phi_{Bo}=0.743$ eV, $N_d=2\times10^{16}$ cm^{-3}, $\alpha=2.45$ nm, $r_j=34.2$ nm, and $T=300$ K. The I-V characteristics of the experimental Pd_2Si USBD are nearly ideal with a diode-quality factor of 1.012. This demonstrates that non-ideality of the $Ti:W/Pd_2Si/nSi$ USBDs is associated with the Ti:W barrier metal. When Pd, which is a high work-function metal, is used instead of Ti:W, the low barrier-height parasitic MIS diode does not form and the diode characteristics are identical to those of ideal simulated devices.

Now, to show that Ti is responsible for degradation of the $Au/Pd/Ti:W/Pd_2Si/nSi$ USBD, Ti- and W-MIS diodes were fabricated on top of 0.25 ohm-cm (111) oriented nSi wafers. The wafers were first thermally oxidized to grow 360 nm of oxide. Oxide windows, 13 μm in diameter, were defined using standard optical-lithography and wet-etching techniques to form openings for the MIS diodes. A 4-nm thick interfacial oxide was thermally grown at 800 °C for 10 min in dry oxygen. This was followed by deposition of 50 nm of Ti or W by dc planar magnetron sputtering to form Ti- or W-MIS diodes, respectively. The MIS contacts were protected by an overlapped Au/Pd/Ti:W contact. The contacts to the backside of the wafers were made using sputtered gold. The resulting structure is shown in Fig. 6.

The I-V characteristics of MIS diodes measured before and after the thermal anneal at 400 °C are shown in Fig. 7. The Ti-MIS diode is much more conductive than the W-MIS in both current directions. While the W-MIS I-V curves changed only slightly after annealing, the

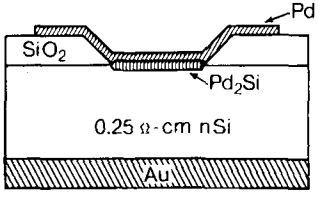

Fig. 4. Experimental $Pd/Pd_2Si/nSi$ Schottky barrier diode structure.

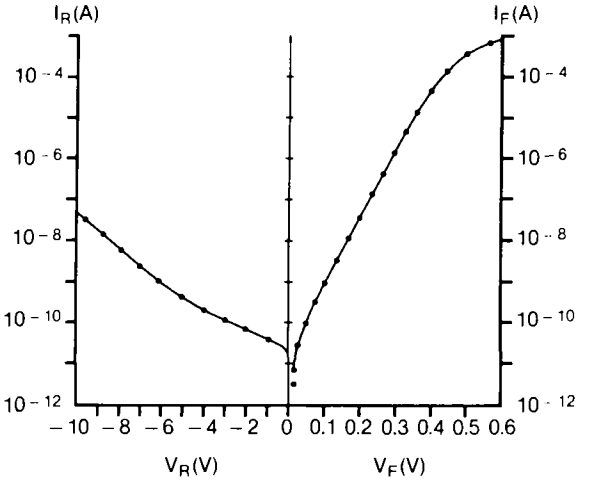

Fig. 5. I-V characteristics of $Pd/Pd_2Si/nSi$ Schottky barrier diodes: • • • experimental; ——— simulated using $\alpha = 2.45$ nm, $r_j = 34.2$ nm, $\phi_{Bo} = 0.743$ eV, $N_d = 2 \times 10^{16}$ cm^{-3}.

Ti-MIS I-V characteristics changed dramatically. The slight difference in the shape of the W-MIS I-V curves measured before and after the 400 °C anneal can be attributed to the change in the density of interfacial states at the oxide/metal interface. The dramatic current increase of the Ti-MIS diode after the thermal anneal can be explained in terms of an increased quantum-mechanical tunneling through the thin interfacial oxide due to the reduction of its thickness. This is in agreement with a theoretical prediction that titanium should react with SiO_2 and thus reduce its thickness, while the oxide thickness under the W remains constant. The current density of experimental W-MIS diodes suggests that the current contribution from a $W/SiO_2/nSi$ parasitic perimeter diode is sufficiently low to cause only little deviation of a

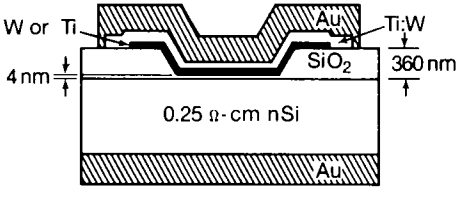

Fig. 6. Structure of experimental Ti- or W-MIS diode.

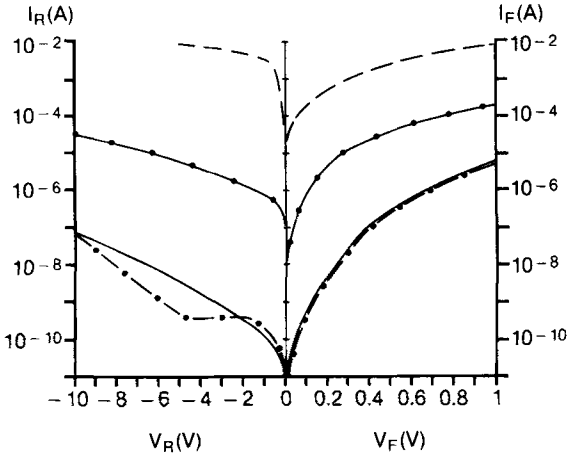

Fig. 7. Experimental I-V characteristics of Ti- and W-MIS diodes before and after 400°C, 2 hr anneal in H_2/N_2 forming gas: ——— W-MIS before anneal; —•—•— W-MIS after anneal; —•—•— Ti-MIS before anneal; ——— Ti-MIS after anneal.

Au/Pd/W/Pd_2Si/nSi USBD from ideality and no significant degradation after the thermal anneal. The I-V curves of a 15-μm diameter experimental Au/Pd/W/Pd_2Si/nSi USBD are shown in Fig. 8. In the forward-current direction, the experimental diode is nearly ideal. In the reverse-current direction, the difference between the experimental and simulated characteristics is much smaller than the corresponding difference shown in Fig. 2 for the Au/Pd/Ti:W/Pd_2Si/nSi USBD. After thermal anneal, the characteristics changed only slightly in contrast to the change in the characteristics of the Au/Pd/Ti:W/Pd_2Si/nSi diode shown in Fig. 2.

To show how much of the perimeter must be involved in the MIS conduction to cause a significant change in I-V characteristics, a 13-μm diameter Ti:W-MIS diode with ≈3 nm of interfacial oxide was made and then measured before and after a 2-hr anneal at 400°C in forming gas. A 15-μm diameter Pd_2Si USBD was then modeled assuming a 2.5-nm wide MIS perimeter region. The current contribution of the parasitic Ti:W-MIS diode was calculated as a product of the current density obtained from the experimental Ti:W-MIS diode and the area of the simulated diode perimeter—initially, 2.5-nm wide. The perimeter current was then added to the current calculated for an ideal Pd_2Si/nSi

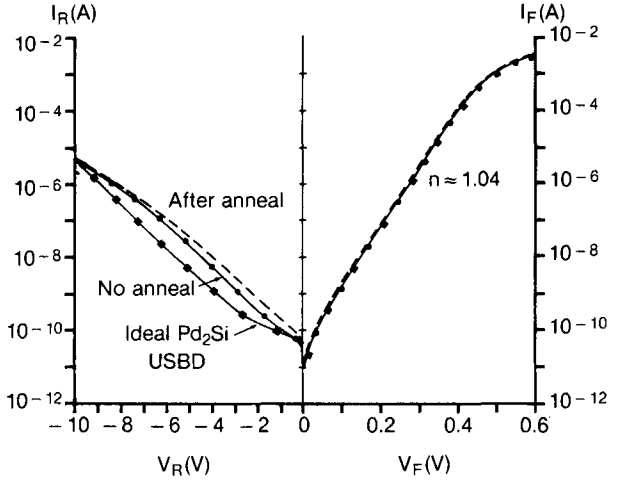

Fig. 8. I-V characteristics of Au/Pd/W/Pd_2Si/nSi Schottky barrier diodes: —●—● before anneal; ——— after 4-hr anneal at 400 °C in H_2/N_2 forming gas; —■—■— simulated ideal Pd_2Si/nSi diode.

USBD to simulate the characteristics of a Ti:W/Pd_2Si/nSi USBD. The I-V characteristics of annealed Ti:W/Pd_2Si/nSi USBDs were simulated in a similar manner, considering the current density from an annealed Ti:W-MIS diode and a diode perimeter of 5-nm width. The lateral spread of the perimeter of the parasitic MIS diode was allowed to compensate for the consumption of the oxide by Ti which, in the case of Ti:W, was found to be approximately 2 nm in the first 2 hr of the anneal. The magnitude of the lateral spreading depends on the geometrical profile of the oxide at the bottom of the oxide cut. Although this simulation does not fully reflect the real situation at the diode perimeter, where the oxide thickness is variable, the results shown in Fig. 9 resemble the characteristics of experimental Ti:W/Pd_2Si/nSi very well. The simulation demonstrates that a parasitic perimeter MIS diode only 2.5-nm wide can have a significant impact on the I-V characteristics of a Ti:W/Pd_2Si/nSi USBD.

Conclusions

The origin of excessive current leakage of Au/Pd/Ti:W/Pd_2Si/nSi unguarded Schottky barrier diodes has been identified. It was shown that this leakage cannot be attributed to the high-field effect present

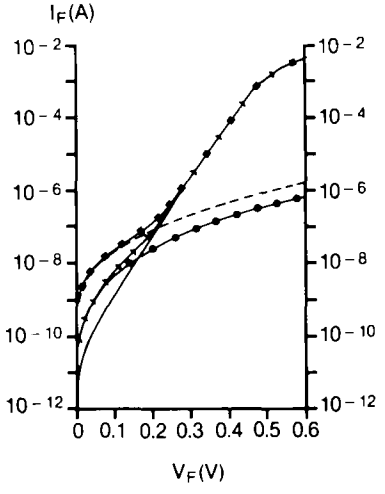

Fig. 9. Simulated forward I-V characteristics of Au/Pd/Ti:W/Pd_2Si/nSi Schottky barrier diodes: ——— ideal Pd_2Si/nSi SBD; —●—● current of 2.5-nm wide perimeter Ti:W-MIS diode before anneal; —►—► total Ti:W/Pd_2Si/nSi diode current before anneal; ——— current of perimeter Ti:W-MIS diode after 2-hr anneal at 400°C in H_2/N_2 forming gas; —■—■ total Ti:W/Pd_2Si/nSi diode current after anneal.

near the edges of an unguarded diode [3]. When the Ti:W diffusion-barrier metal was replaced by high work-function Pd, the current leakage disappeared. The excessive current is attributed to a parasitic low barrier-height Ti-MIS diode that forms at the USBD perimeter. The Ti component of Ti:W has also been shown to be responsible for a 400°C anneal-induced USBD degradation. This was confirmed experimentally from the characteristics of W- and Ti-MIS diodes. It was demonstrated that, when W was used as a diffusion-barrier metal, no major degradation of W/Pd_2Si/nSi USBDs resulted. A simulation of Ti:W/Pd_2Si/nSi USBD based on data from experimental Ti:W-MIS diodes and simulated Pd_2Si characteristics demonstrated that a parasitic MIS diode having a perimeter as small as 2.5-nm wide can have a significant impact on USBD properties.

Acknowledgments

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