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Characterization of defect states in Mg-doped GaN-on-Si p^+n diodes using Deep-Level Transient Fourier Spectroscopy (DLTFS)

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Mg-doped GaN-on-Si p^+n diodes have been fabricated and characterized by static electrical and Deep-Level Transient Fourier Spectroscopy (DLTFS) measurements. From static capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics, we estimated the diffusion barrier of the p^+n diode close to the GaN band gap at room temperature. The temperature dependence of the capacitance showed freeze-out effect of the Mg-dopants at 200 K. From DLTFS measurements for various reverse bias and pulse voltages, two peaks were found and are composed of different defect states. The first peak with two components was related to diffusion of Mg *p*-type dopants in the *n*-GaN and V_N-related defects. The two components have activation energies close to 0.25 eV, from valence band and conduction band with a capture cross-section of ~10^{-16} cm^2. The second peak with two components showed temperature shifts with the pulse height indicating a band-like behavior. This peak was commonly attributed to deep acceptor C_N-related defects with an activation energy of E_V+0.88 eV and a capture cross-section of 10^{-13} cm^2. A second acceptor level was found, with an activation energy of 0.70 eV and a capture cross-section of 10^{-15} cm^2. This second component was previously attributed to native point defects in GaN.

Keywords: GaN-on-Si, *pn* diodes, DLTFS, defect states

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1. Introduction

GaN is a promising material for numerous applications, from photonic devices such as blue Light Emitting Diodes (LED) [1] to high power and high frequency devices such as High Electron Mobility Transistors (HEMT) or Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET). The quality of GaN epitaxy required for these devices is achievable in heterostructures grown by Metal-Organic-Chemical Vapor Deposition (MOCVD) [2], Molecular Beam Epitaxy (MBE) [3,4] or Hybrid Vapor Phase Epitaxy (HVPE) [5,6]. Due to the lack of cost efficient bulk GaN substrates [3], GaN based devices are realized on silicon carbide (SiC) [7,8], sapphire (Al_2O_3) [9,10] or silicon (Si) [11] substrates. It has been shown that devices fabricated on SiC substrates can deliver higher performance in terms of power density [7] due to the high thermal conductivity of SiC. Nevertheless, GaN-on-Si devices allow the exploration of new technologies and potentially facilitates wider integration of GaN [12]. However, GaN based devices suffer from a high density of defects. These defects commonly occur in GaN in the form of native point defects (nitrogen anti-sites, nitrogen or gallium vacancies), impurities (oxygen and carbon substituted at nitrogen sites) or extended defects, with stress-induced threading dislocations as the most important ones [13]. Formation of dislocation allows for relaxation of highly mismatched GaN/substrate interface owing to strong difference in lattice constants and coefficient of thermal expansion. For example, GaN films grown on sapphire, silicon or SiC substrates suffer from compressive and tensile strains [14–16]. All these defects can degrade the device performance and reliability [17,18].

The defect states in GaN based HEMT have been studied with different techniques such as low frequency noise [19–21], drain current transient spectroscopy [22–25] and Deep-Level Transient Spectroscopy (DLTS) [22,25,26]. In the same time, with the development of GaN MOSFET, *p*-type and *n*-type doped GaN Schottky diodes grown on sapphire [27–30] or on SiC [31,32] substrates have also been studied. A few defect states were found but their origin is not completely understood and were attributed to nitrogen vacancies, Mg dopant or C impurities [13]. Besides, Mg-doped *p*-type GaN found a growth of interest because of the research on the development of blue LED [33]. Moreover, the use of Mg doping also turned out to play a crucial role in bringing HEMTs in the normally off/enhancement mode with a shift of the threshold voltage to positive values [34–36]. Also, many works about GaN *pn* diodes on sapphire [37], on GaN [38–41] and on silicon [42,43] substrates reported interesting electrical performance for power applications. Although the use of a silicon substrate is promising for power applications with reduced cost of fabrication, there is a strong dependence of the electrical characteristics, breakdown voltage or OFF-current, on defects in GaN-on-Si *pn* diodes [44,45]. So the understanding of GaN-on-Si *pn* diode defect properties is crucial for the development of GaN-on-Si based power devices [12].

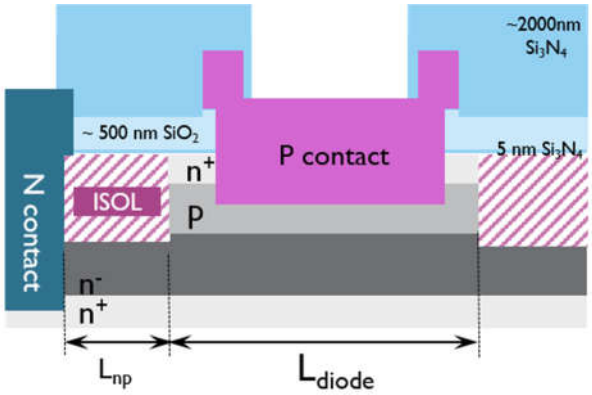
In this work we investigated the defect characteristics of Mg-doped GaN p^+n diodes on silicon substrates using a powerful technique, the Deep Level Transient Fourier Spectroscopy (DLTFS) in order to extract the defects parameters.

2. Experimental details

2.1 Epitaxial layer

In this work, GaN p^+n diodes were fabricated at IMEC. The diodes were grown by MOCVD on Si substrates. The p^+n structure was composed of a 400 nm thick Mg-doped p^+-GaN layer at a doping concentration of $6x10^{19}$ cm^{-3} and of a 750 nm thick Si-doped *n*-GaN layer at $3x10^{16}$ cm^{-3}. We can note that Mg dopants have a rather deep acceptor level and exhibit freeze-out behavior [34] due to the Fermi level shift towards the valence band for lower temperature. This phenomenon is seen as a drop reduction of in the steady-state capacitance with decreasing the temperature at a fixed reverse bias U_R. This phenomenon is weakened due to high Mg doping concentration. Here, the Mg activation percentage is about 60% evaluated with Secondary-Ion Mass Spectroscopy (SIMS) by measuring Mg/H ratio.

(a)



(b)

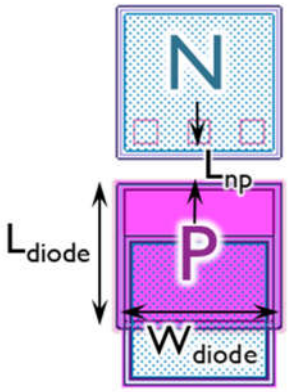


Figure 1. Schematic representation of the GaN-on-Si p^+n-diode under study, showing the diode in a cross-sectional view (a) and in top view (b). The diodes under study have an area of 100 x 112 µm^2 (L_{diode} x W_{diode}) and there is a 14 µm distance between the top N and P contact area (L_{np}).

A schematic representation of the diodes under study is depicted in cross-sectional view in **Figure 1(a)** and in top view in **Figure 1(b)**. In the fabricated diode, a top n^+-GaN layer is present because trench gate transistors are integrated in the same wafer. It is etched out prior to p metal contact, hence, the role of the top n^+-GaN layer in the diode electrical characteristic is neglected. For the diode fabrication, a Si_3N_4/SiO_2 layer is used as surface passivation. Ti/Al/TiN containing metal stacks are used to contact the p-GaN layer and the bottom n^+-GaN layer from the top. These metal contacts are annealed at 565°C. The top n^+-GaN and p-GaN layers are isolated towards the drain contact by using a N-implantation (see ISOL area in **figure 1(a)**). A 4 µm-thick Al is put on top of the n and p contacts and a 2 µm-thick Si_3N_4 layer is used as final surface passivation. The diodes under study have an active area of 100 x 112 µm^2 (L_{diode} x W_{diode}). Both the n and p metal contacts are made at the frontside of the wafers with an L_{np} of 14 µm. The threading disclocation density was estimated using the in-plan Transmission Electron Microscopy (TEM) at about 1~3·10^9 cm^{-3} while X-Ray Diffraction (XRD) gave similar readout.

2.2 The Deep-Level Transient Fourier Spectroscopy

In order to characterize the defect states of the Mg-doped GaN p^+n diodes, DLTFS measurements were carried out. These measurements are based on the observation of trap-dependent capacitance transients, originating from a depletion region in a semiconductor material [46–48]. One may visualize it in the following way: initially, the charges are trapped in those defect states at deep-level energy E_T (eV) that are lying below Fermi level. By applying a reverse bias voltage U_R (V) (**Figure 2(a)**), defect states emit their trapped charges (up to the depletion width x_R). Then, a pulse voltage U_P (V) (**Figure 2(b)**) is applied and the charges are trapped again in the deep-level centres (up to the depletion width x_P). After the pulse (**Figure 2(c)**), the defect states their trapped charges again with an emission time τ (s) and emission rate e (s^{-1}). The (**1** below defines the electron emission rate e [49], where σ (m^2) is the capture cross-section, the term γT^2 (m^{-2}·s^{-1}) corresponds to the product of the conduction band density of states and the thermal velocity of electrons, E_T is the defect state

activation energy, E_C is the conduction band energy (eV), q is the elementary charge, k_B is the Boltzmann constant and T is the temperature.

$$e = \frac{1}{\tau} = \sigma\gamma T^2 \cdot exp^{\frac{(E_C - E_T)}{qk_BT}} \qquad (1)$$

DLTS is based on measurements of capacitance transients that correspond to the response of the system a voltage pulse for different time window t_w (from t_1 to t_2) at varying temperature (**Figure 2(d)**). The difference ΔC (F) is extracted and converted into several coefficients (b_1 for example is used here) using Fourier transform in order to obtain the DLTFS signal (**Figure 2(e)**).

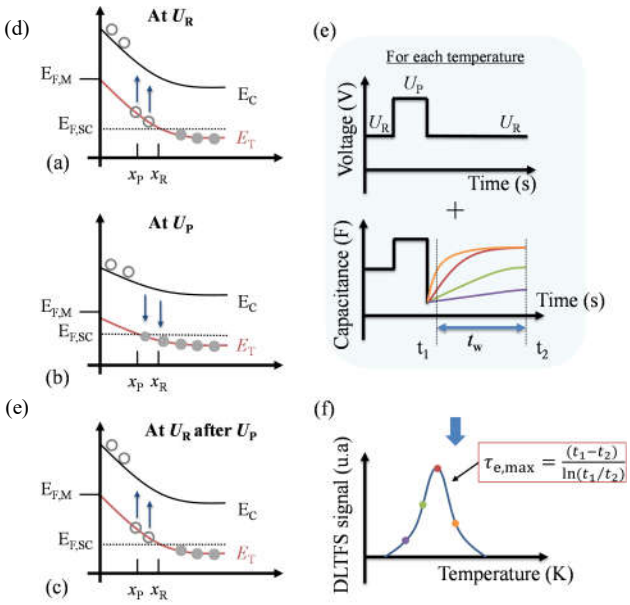


Figure 2. Principle of DLTFS. (a) First state at reverse bias voltage U_R with empty defect states within x_R, (b) a pulse voltage U_P is added to fill the defect states up to x_P, (c) after the pulse, the system goes back at reverse bias. (d) The capacitance transients are acquired at each temperature and the capacitance difference is calculated for several time windows t_w. (e) Then, the DLTFS signal is extracted from capacitance transients as a function of the temperature.

2.2 Electrical characterization setup

The measurements have been performed through a PhysTech GmbH FT-1230 HERA DLTS system for measurement and data acquisition. The setup is composed of a Boonton 7200 capacitance bridge to apply the reverse bias voltage and measure the capacitance or conductance and of a Keysight 33500B to generate the pulse voltage (**Figure 3**). Here the dynamic signal voltage and frequency are 100 mV and 1 MHz, respectively. The time windows used in this study were 100 ms, 300 ms, 600 ms, 1 s and 3 s. The sample is placed in a closed-loop Helium-cooled Janis cryostat and the temperature is controlled by a Lakeshore Model 336. The reverse bias and pulse voltage are applied between the p^+ and n contacts and are defined by U_R and U_P, respectively.

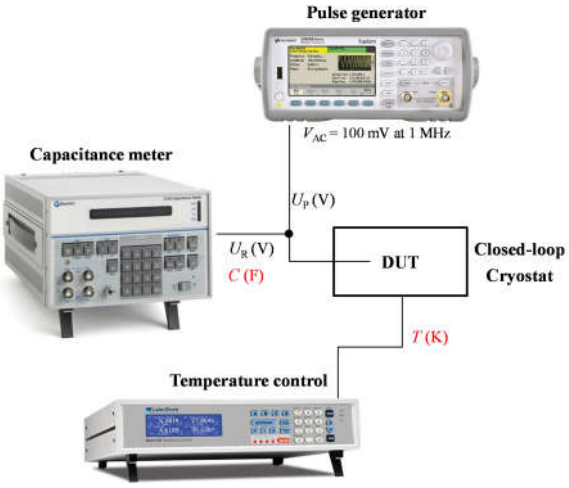


Figure 3. Schematic of the measurement setup composed of a capacitance meter (Boonton 7200), a pulse generator (Agilent 33500B), a temperature controller (Lakeshore Model 336) and a PhysTech FT-1230 HERA DLTS system (not shown). The sample is placed in a closed-loop He cooled cryostat.

3. DC Characterization

3.1 DC measurements at room temperature

In order to determine the structural type of the GaN p^+n diode, a capacitance-voltage (C-V) measurement performed at room temperature in the bias range between -5 V and 5 V and we extracted the power-law index [50]. *pn* junctions can be broadly categorized under three structural types, an abrupt junction, a linearly graded junction, and a non-abrupt and non-linear junction. From **(2**, we can identify the structural type from the power-law index k. In this equation, V (V) is the applied voltage, V_D (V) the barrier height, A a factor dependent on parameters such as diode surface S (m^2) and GaN dielectric constant ε_0 and C (F) the capacitance. It is known that if $k = 1/2$ the junction is abrupt, if $k = 1/3$ the junction is linearly graded and the junction is graded and non-linear in the other cases [51].

$$V = V_D + A\left(\frac{1}{C}\right)^{1/k} \qquad (2)$$

Using the procedure detailed by C.A. Wang *et al.* [50], we find the **(3** which is independent of A.

$$V = V_D + k \cdot \frac{dV}{d\left(\frac{1}{C}\right)}\left(\frac{1}{C}\right) \qquad (3)$$

Then from the plot of V against $\frac{dV}{d\left(\frac{1}{C}\right)}\left(\frac{1}{C}\right)$, we can extract V_D from the intercept of the fitting line with the y-axis and the power-law index k from the slope. **Figure 4** shows the C-V and $1/C^{1/k}$-V curves along with its linear fit using the extracted power-law index k. We found a hysteresis in the C-V curve, which is indicative of defect charging effects. Besides, we observed a linear $1/C^{1/k}$-V curve for $k \approx 0.17 \pm 0.01$ indicating a graded and non-linear p^+n junction at room temperature. The linear fit of the $1/C^{1/k}$-V curve allowed the extraction of the diffusion barrier of the junction, which is about 3.6±0.2 V at 295 K. This value is slightly larger than the theoretical value, of about 3.25 V at 295 K. It is possibly due to the series resistance with contribution from contact resistance and from resistance of the quasi-neutral region in the n-type GaN with a doping level of 10^{16} cm^{-3}.

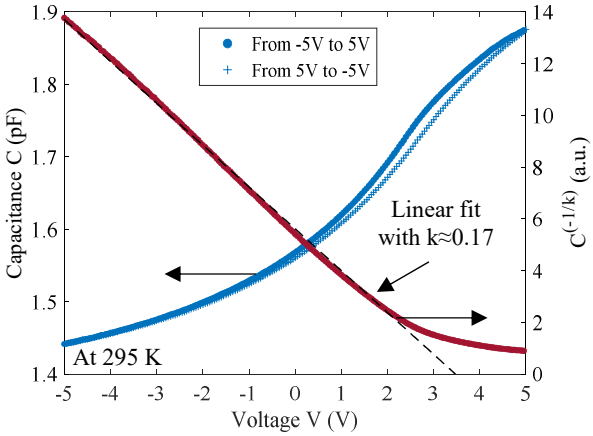


Figure 4. C-V characteristics at room temperature of the GaN p^+n diode showing a hysteresis for voltage between -5 V to 5 V (left y-axis) and the $C^{-1/k}$-V curve with a linear fit allowing to extract the diffusion barrier of about 3.6 V (right y-axis).

3.2 DC measurements - temperature dependence

Figure 5 shows the temperature dependence of the static characteristics (C-V and I-V) in the range 100 K - 410 K with 10 K steps. First in **Figure 5(a)**, we observed an increase of the capacitance with temperature because of the dependence of the active Mg concentration in the p-GaN layer with the temperature. It is in the C-T curve obtained at a reverse bias of -5 V (**Figure 5(b)**), where the Mg-dopants freeze-out occurs around 200 K. The freeze-out in this case is very low, which can be explained by the formation of an acceptor band instead of individual acceptor levels inhibiting the freeze-out phenomenon [52]. At higher temperatures, a decrease of the capacitance is observed for $V > 4$ V, which is related to the decrease of the fixed ionized charge density in the depletion region.

Then, in the I-V characteristic (**Figure 5(c)**), an increasing current with temperature is in agreement with the temperature dependence of p^+n diode behavior [51]. First at low forward voltage between 0 V and 3 V, the increase in current is related to enhanced generation-recombination current due to the increase of the intrinsic carrier density with the temperature.

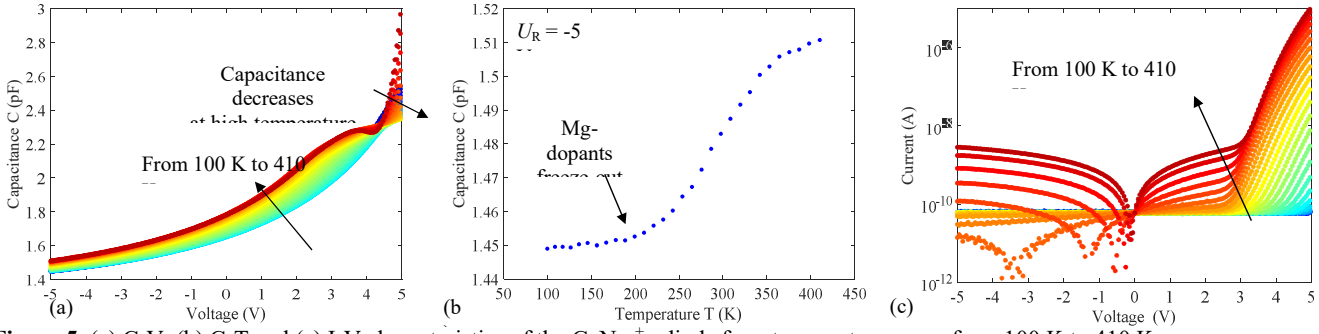


Figure 5. (a) C-V, (b) C-T and (c) I-V characteristics of the GaN p^+n diode for a temperature range from 100 K to 410 K.

Besides, a shift of the zero point of the I-V curve can be explained by the apparition of the non-ideal defect-assisted generation-recombination component in forward voltages and at high temperature values which is thermally activated and negligible around room temperature. At high forward voltage, above 3 V, we observed an increase of the diffusion current as carriers have more energy to pass the p^+n barrier.

4. DLTFS characterization

4.1 Effect of reverse bias and pulse voltage

In order to assess defects, and extract their parameters in terms of activation energy and capture cross-the DLTFS measurements were carried out in the temperature range 100 K - 400 K. Pulse time t_P = 100 ms and time window t_w = 600 ms were chosen to have a strong DLTFS signal strength. **Figure 6** shows the DLTFS spectra for different reverse bias U_R from -5 V to -3 V at a fixed U_P = -0.5 V (**Figure 6(a)**) and for different pulse pulse voltages U_P from -1.5 V to 0.5 V at a fixed U_R = -5 V (**Figure 6(b)**). The DLTFS spectra show two positive positive peaks (T_1 and T_2) around 130 K and at 330 K, respectively.

When increasing U_R from -3 V to -5 V, no temperature shift and an increase of magnitude of the first peak T_1 were observed indicating T_1 is related to bulk traps [53,54]. For the second peak T_2, an increase its magnitude and a shift towards higher temperatures implies that it could be related to a field-dependent emission rate [53,54]. This dependence can be explained by Poole-Frenkel effect, phonon assisted emission or band-like defects.

Now when increasing U_P from -1.5 V to 0.5 V, we found an increase of T_1 magnitude up to -0.5 V followed by the drop for positive value of the pulse voltage. So, carrier injection is lowering the peak magnitude. This effect can be explained by the overlapping of two states (electron and hole traps) as previously reported [55]. Also, no temperature shift was noted indicating again the T_1 peak is related to bulk or extended defects. Concerning T_2 peak, we observed a large increase of the magnitude when the pulse voltage becomes positive with a shift towards higher temperatures. This shift cannot be related to the Poole-Frenkel effect as the emission electric field did not change. One explanation could be that T_2 is related to several defects with different energy levels such as band-like defects.

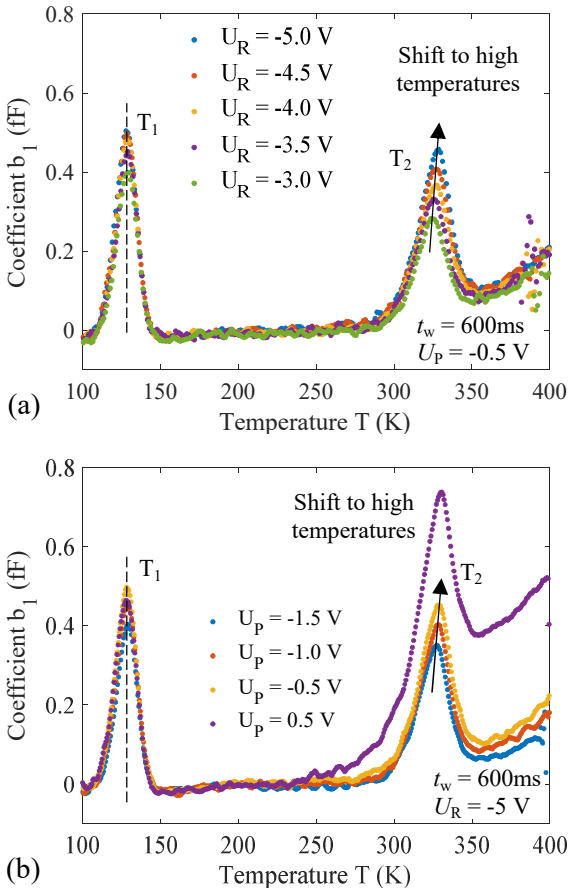


Figure 6. (a) DLTFS spectra for different reverse bias at U_P = -0.5 V and (b) for different pulse voltages at U_R = -5 V. Two peaks can be observed at 130 K and 330 K.

4.2 Discussion on defect states

In DLTFS spectra, the maximum of the peaks occurs when the emission time dependence on the time window satisfies $\tau_{max} = \frac{t_1 - t_2}{\ln(t_1/t_2)}$ (**Figure 2(e)**). The term τ_{max} is numerically extracted for each temperature knowing the time window in order to represent the Arrhenius plot, ($\ln(\tau.T^2)$-1000/T). Then, the capture cross-section σ is calculated from the intercept of the linear fitting curve with the y-axis and the activation energy E_C-E_T or E_T-E_V from the slope. **Figure 7(a)** and **Figure 7(b)** show the Arrhenius plot for both defect states at 130 K and 330 K, respectively, extracted for different values of U_R and for U_P = -0.5 V.

For the first defect state T_1, an activation energy of about 0.23±0.01 eV and a capture cross-section of about 10^{-16} cm^2 were extracted. This defect is commonly observed in MOCVD-grown GaN and is assigned to V_N-related defects or to V_N-V_{Ga} complexes in *n*-GaN [29,31,32,56]. Recently it was reported that Mg diffuses into the *n*-type GaN through the dislocations [57]. Because of diffusion of the Mg along the dislocations, the Mg doping level can be reduced to 10^{16} cm^{-3} [58]. Moreover, for this doping level of 10^{16} cm^{-3}, Mg dopants have an activation energy of about 0.25 eV [59], close to the one extracted from T_1 peak. The T_1 peak could be related to donor-type V_N-related defects and to acceptor-type diffused Mg dopants. So, the drop of the DLTFS signal can be explained by these defect states (donor and acceptor) in the *n*-GaN. It could also explain the graded and non-linear p^+n junction as identified from the $1/C^k$ (V) curves. Nevertheless, donor carbon-related defects C_N at E_V+0.25 eV as reported by Tokuda *et al.* [34,55] in *p*-GaN cannot be ruled out.

For the second defect state T_2, activation energies of about 0.89±0.03 eV and 0.86±0.03 eV above the valence band and a capture cross-section of about 10^{-13} cm^2 were extracted for U_P = -1.5 V and U_P = -0.5 V, respectively. This is alike to the deep acceptor level at the same energy level, at E_V+0.88 eV which has been reported and previously assigned to C_N in *n*-GaN [34,35,55]. The temperature shift suggests that the C_N deep acceptor state has a band-like behavior. As U_P is increased to a positive value of 0.5 V, the energy and capture cross-section lowered down to 0.70±0.02 eV and 10^{-15} cm^2, respectively. So, a second component is observed and was attributed to a native point defect in GaN [56,60]. The large increase of the amplitude indicates that both components come from the same type of defect (acceptor state). **Figure 7(c)** shows the DLTFS spectra at U_R = -5 V for U_P = -1.5 V (in blue) and U_P = 0.5 V (in violet). The fits of the experimental curves was performed using the PhysTech GmbH software with the extracted parameters. A strong agreement between the experimental curves and the corresponding fits (dashed line) is observed.

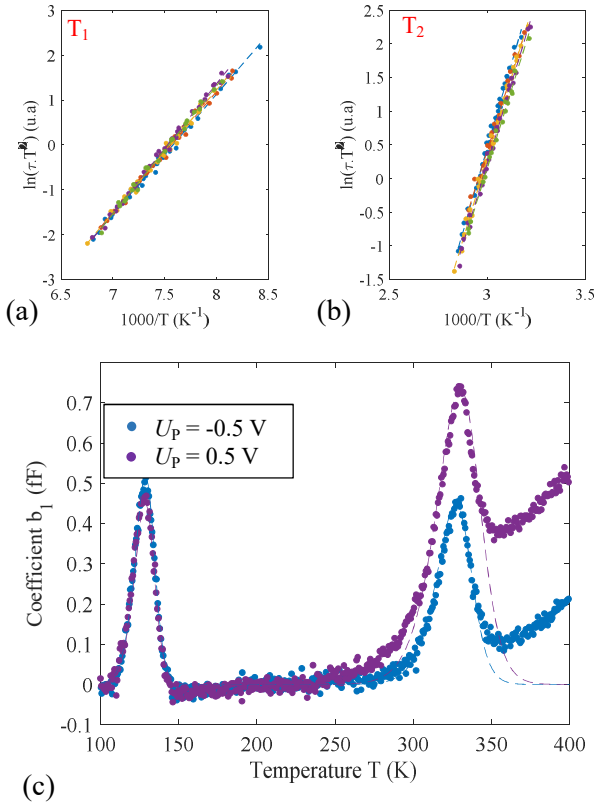


Figure 7. Arrhenius plots of the defect state (a) at 130 K and (b) at 330 K extracted for different values of U_R and for U_P = -0.5 V. (c) DLTFS spectra at U_R = -5 V for U_P = -0.5 V (in blue) and U_P = 0.5 V (in violet) and their fit using the extracted parameters.

5. Conclusion

The defect state properties of Mg-doped GaN-on-Si p^+n diodes have been studied by mean of DLTFS. The effect of the reverse bias and pulse voltage showed different defect states at low and high temperature. At low temperature, two defect states with the same energy of about 0.25 eV, one above the valence band and the other below the conduction band, were observed. These defect states were attributed to V_N-related defects and to Mg-dopants diffusion in the *n*-GaN. At high temperature, two defects states were observed at energies of about 0.88 eV and 0.70 eV above the valence band. The first was attributed to deep acceptor C_N-related defects with a band-like behavior, while the second was assigned to native point defects.

Acknowledgements

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