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Device Performance as a Metrology Tool to Detect Metals in Silicon

Cor Claeys and Eddy Simoen*

Herein, the impact of transition metals (TMs) on the electrical device performance, i.e., carrier lifetime, leakage current, low-frequency noise, photocurrent, and solar cell efficiency is reviewed. Defect information is obtained by using either simple device structures such as metal-oxide-semiconductor (MOS) capacitors and pn-diodes or transistors. The impact of metals on complementary MOS (CMOS) image sensors (CIS) and solar cells is also briefly addressed. Scaled devices are a power tool to detect small-sized defect clusters or even single metal atoms. Examples are given for a variety of both slow- and fast-diffusing metals. The final section outlines the power of density functional theory (DFT) ab initio calculations to support the experimental observations and to get a deeper physical insight into the defect structure.

1. Introduction

Metallic contamination in silicon has been investigated for more than half a century and is still today an extensive research topic as clearly outlined in a recent book by the authors.[1] While for photovoltaic (PV) applications relative high metal concentrations can be allowed, more stringent requirements are imposed for integrated circuits (IC). The electrical device performance is degraded by their impact on essential parameters such as carrier lifetime, leakage current, gate oxide integrity, and retention times of memories. The detrimental impact can be restricted or in some cases even eliminated by defect-control techniques such as ultraclean processing, gettering schemes, and defect passivation techniques by hydrogen annealing.[2]

A variety of techniques is available for the chemical and structural characterization of metal-related defect complexes, each with their resolution and detection limit. A combination of different techniques will be needed in case that the origin of the detrimental defect is unknown. However, due to the sensitivity limit of these techniques, the electrical performance evaluation of devices enables to show defect concentrations at a much lower detection level, as e.g., in the case of CMOS imager sensors (CIS) where even a single metal atom in a pixel can be detected. This review will mainly focus on the impact of metallic contamination on silicon devices and circuits.

For the detection of metals and also grown-in defects (precipitates, clusters, extended defects), one can use simple structures such as capacitors and diodes or more complexes components such as transistors and circuits. The aim is to obtain defect information using basic electrical parameters. Several of the analysis techniques will be briefly discussed and illustrated. Attention is also given to the impact of metals on the performance of CMOS imagers and solar cells, respectively. A brief discussion will also be given related to the use of ab initio calculations to achieve a better insight into the structure of the metal defects. The use of density functional theory (DFT) calculations to optimize metal gettering approaches will be outlined and illustrated.

2. Metal Contamination and Device Processing

Analyzing the semiconductor IC fabrication cycle from crystal growth to device packaging, there are ample places for picking up metallic contamination. This is discussed in detail in Chapter 3 of previous study.[1] Many fabrication modules such as wafer handling, wafer cleaning, lithography, wet/dry etching, and thermal processing (diffusion, layer deposition, annealing, rapid thermal processing, epitaxial growth, etc.) are nowadays well controlled.

Special attention has to be given to ion implantation where the effects such as sputtering,[3] cross contamination from previous implantation steps,[4] and mass interference (e.g., BF_2 and Mo[5]) are often the origin of metallic contamination. Examples of Al sputtering during P^+ implantation at 45 keV and As^+ at 25 keV,[6] respectively, and Fe sputtering during an As^+ implantation at 60 keV,[7] are illustrated in **Figure 1**. For a detailed analysis, one has to take into account the type of implanted species, the dose, and the energy and the metal that is sputtered away.

For advanced processing schemes, an important source of metallic contamination is the metal layer that is used for, e.g., silicidation or germanidation, back-end metallization (BEOL), via filling in damascene structures, through silicon vias (TSV) and ferroelectric layers for nonvolatile memories (NVMs). For TSV processing, the stress around the via influences the metal

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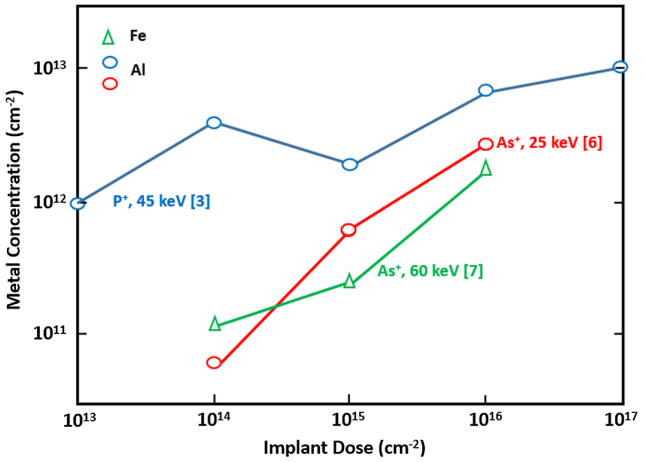

Figure 1. Al concentration due to sputtering during an ion implantation (P^+, 45 keV,[3] and As^+, 25 keV) and Fe concentration (As^+, 60 keV) versus implantation dose.

diffusion so that a Keep-Out Zone around the via has to be respected to avoid impact on the lifetime and the leakage current of the devices.[8,9]

3. Capacitance–Voltage Analysis

Since the early days of semiconductors, capacitance–voltage (C–V) analysis has been the workhorse to gain insight in the properties of dielectric layers by studying mobile, fixed, and interface charges (as shown in previous studies[10,11]).

Metal precipitates at the surface influence the oxidation rate resulting in a locally reduced oxide thickness, a lower breakdown voltage, and an increased leakage current due to tunnelling phenomena. Furthermore, metals can diffuse and segregate in the oxide creating fixed or mobile traps (charges) in the dielectric, thereby shifting the flat band voltage and distorting the C–V characteristics. A good insight into the diffusion, precipitation, and segregation of transition metals in dielectrics is crucial.

The Fe segregation coefficient k_{Fe}[12] is given as follows

$$k_{Fe} = \frac{N_{Fe(Si)}}{N_{Fe(SiO_2)}} = 3.76 \exp\left(\frac{-196(\text{eV})}{k_B T}\right) \quad (1)$$

with k_B the Boltzmann constant and T the temperature, leads to a strong Fe segregation in the oxide and limits the in-diffusion in the Si bulk.

The influence of Cu contamination on the oxide breakdown voltage is illustrated in **Figure 2**.[14] The n-type wafers received a backside Cu contamination in the 300–600 °C range. It can be clearly seen that the Cu threshold concentration for initiating degradation depends on the oxide thickness and reduces for thinner oxides. This can be explained by either the Cu precipitation at or near the interface creating a short or the local enhancement of the electric field.

The dependence of the critical Fe concentration for reducing the oxide breakdown voltage with the oxide thickness t_{ox} (in nm) obeys the formula $[Fe]_{crit} = 1.53 \times 10^{11} \cdot 10^{0.12 t_{ox}}$.[13]

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Metal-oxide-semiconductor (MOS) capacitors are also commonly used to determine the generation lifetime and the surface recombination velocity, based on the so-called Zerbst technique that analyzes the capacitance transient response after applying a bias pulse from accumulation to deep depletion.[15]

The Zerbst plot represents $-\mathrm{d}(C_{ox}/C(t)^2)/\mathrm{d}t$ versus $(C_f/C-1)$, with C_{ox} the oxide capacitance and C_f the final steady-state capacitance. This leads to the expression

$$-\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{C_{ox}}{C(t)}\right)^2 = \frac{2\varepsilon_{ox} n_i s_{g,eff}}{\varepsilon_s t_{ox} N_a} + \frac{2n_i}{\tau_{g,eff} N_a}\frac{C_{ox}}{C_f}\left(\frac{C_f}{C(t)} - 1\right) \quad (2)$$

with N_a the doping concentration, n_i the intrinsic carrier concentration, $s_{g,eff}$ the effective surface generation velocity, and $\tau_{g,eff}$ the effective generation lifetime. The slope $(2n_i C_{ox})/(\tau_{g,eff} N_a C_f)$

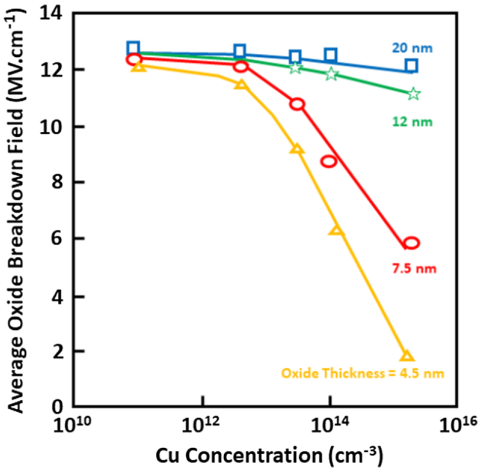

Figure 2. Average oxide breakdown electric field as a function of copper concentration for various oxide thickness. Reproduced with permission.[14] Copyright 1999, ECS-The Electrochemical Society.

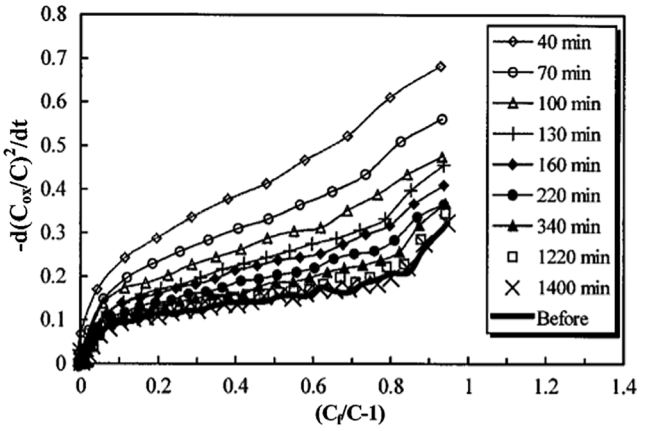

Figure 3. Zerbst plots of iron-doped p-type Si before and after a heat treatment at 200 °C for 5 min and remeasured after different times. Reproduced with permission.[16] Copyright 2000, IEEE.

enables to calculate the generation lifetime, and the intercept is proportional with the surface generation velocity.

The transient response will be influenced by the presence of metals both near the surface and in the semiconductor. The Zerbst technique has been used to study the Fe contamination in silicon and can show the impact of both Fe-B pairs and interstitial Fe_i as illustrated in **Figure 3**.[16] The figure shows the Zerbst plots of p-type Si wafers contaminated with $3.9 \times 10^{12}\,cm^{-3}$ Fe after a 5 min annealing at 200 °C and recorded after different waiting times. Initially, all the Fe is in FeB complexes. Due to the annealing step, these complexes dissociate into Fe_i^+. After a certain waiting time, part of the Fe_i^+ will again be transformed in FeB complexes, resulting in an increase in the generation lifetime. The pairing time t_p of Fe_i^+ and B_s^- to form a FeB complex is $t_p = 557T/[D_{Fe}.N_a]$, with D_{Fe} the Fe_i^+ diffusivity.[17] After 1400 min, all Fe_i^+ is again in the FeB state.

The MOS technique has also been used to characterize the TSV processing, which is schematically shown in **Figure 4**a. After the Si etching, a liner (e.g., TEOS/O_3 CVD) is deposited before depositing a barrier layer (e.g., Ta PVD) followed by the via filling with a metal (e.g., Cu). The process is completed by a chemical–mechanical polishing step (CMP).

The impact of TSV processing on the generation time is illustrated in Figure 4b.[18] The scalloping of the sidewalls is due to the repeated etching and passivation step. When the roughness of the scalloping increases, there is a poorer coverage of the sidewall by the barrier enabling more Cu atoms from the TSV to diffuse in the substrate during processing. The resistance of the Ta barrier during a 300 °C annealing step depends on its thickness. An increased thickness and/or a smoother profile are required for a high-generation lifetime.

4. Diode Analysis

Diode analysis is a simple and straightforward method to investigate the generation τ_g and recombination lifetime τ_r of the material.[19] For a lightly doped substrate with an uniform lifetime, the area current density J_{gen} in reverse operation for $V_R >> k_B T/q$, is given by

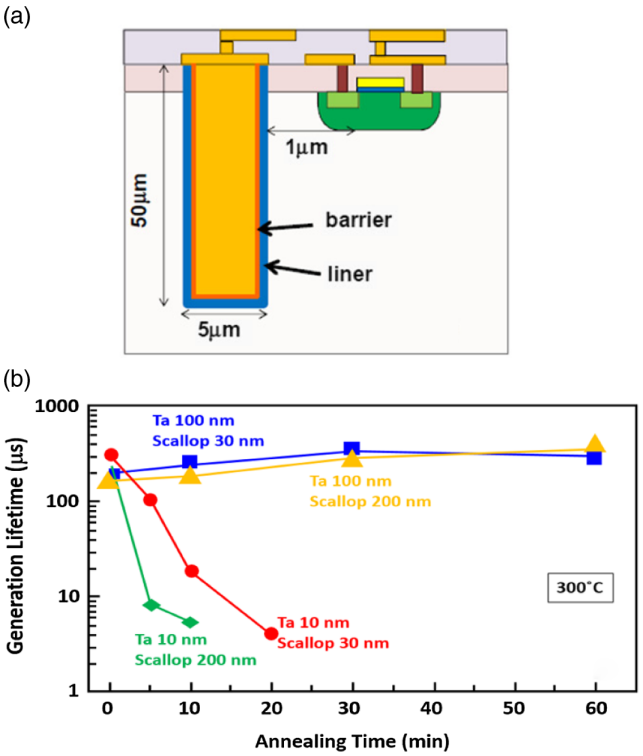

Figure 4. a) Schematic drawing of a TSV process. b) Generation lifetime (τ_g) of minority carriers measured from *C–t* analysis versus the annealing time at 300 °C. Reproduced with permission.[18] Copyright 2011, IEEE.

$$J_{gen} = \frac{q n_i W}{\tau_g} \tag{3}$$

with W the depletion region width at V_R, which can be obtained from a *C–V* plot. The generation lifetime depends on the position of the trap level E_T in relation to the intrinsic level E_i

$$\tau_g = \tau_r\, 2\cosh\left(\frac{E_T - E_i}{k_B T}\right) \tag{4}$$

The most efficient trapping levels are lying near midgap.

The impact of the surface concentration of metals on the leakage current of n^+p diodes is shown in **Figure 5** for Cu, Ni, and Fe.[20] While Ni has only a minor impact, there is an increased leakage current for concentrations above about $2 \times 10^{12}\,cm^{-2}$ for Fe and Cu. The Cu activity is caused by the Cu gettering in the n^+ layer forming precipitates with extended defects.

It is also possible to calculate the generation current per defect center, given by

$$I_{g,defect} = \frac{q n_i \sigma_{n,p} v_{thn,p}}{2\cosh\left(\frac{E_T - E_i}{k_B T}\right)} \tag{5}$$

This expression has been used to calculate the leakage current for a variety of metals in both silicon and germanium.[21] The graphical representation for Mn, Fe, Co, and Ni and Cu is given in **Figure 6**. The metals with an energy level close to

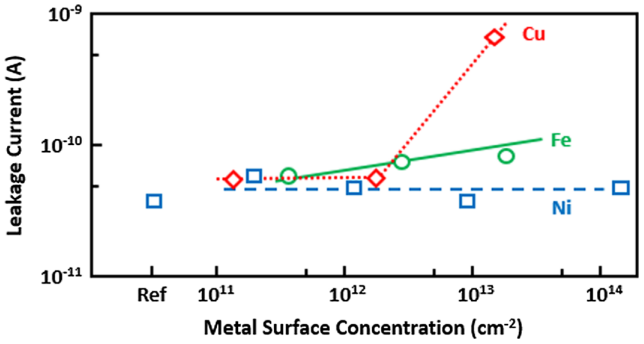

Figure 5. The relationship between leakage current and surface metal concentration before heat treatment (junction area of n^+p diode is 1 mm^2).[20]

midgap (Fe and Ni) and small capture cross sections are the most effective current generators. For the current generation, however, the dominant factor is the position of the energy level, yielding an exponential dependence on the temperature, while the capture cross sections are only influencing the prefactor. As the intrinsic carrier concentration depends exponentially on the band gap ($E_{g,Si} = 1.12$ eV, $E_{g,Ge} = 0.66$ eV), this means that at 222 K, Ge has the same intrinsic carrier concentration as Si at 300 K. As can be seen in Figure 6, metals have a larger impact in Ge than in Si.

In case that the metal precipitates are associated with dislocations, one has also to take into account the electrical activity of the dislocation, i.e., both the generation current caused by the metal atoms in the cluster and the dislocation-induced current are important.

It should also be mentioned that by using different diodes with different geometries (i.e., different area and perimeters), one can calculate both the physical (diffusion current and generation current) and the different geometrical components, i.e.[19]

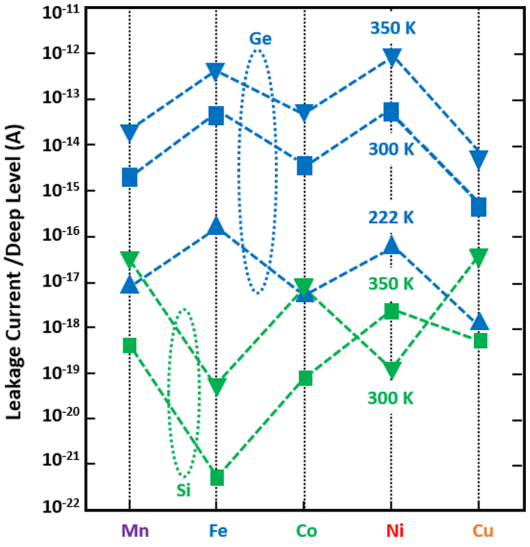

Figure 6. Leakage current per deep level in Ge and Si.

$$I = AJ_A + PJ_P + N_C I_C + I_{par} \quad (6)$$

with A the diode area, J_A the area current density (A m^{-2}), P the perimeter (m), J_P the perimeter current density (A m^{-1}), N_C the number of corners, I_C the corner current density (A/corner), and I_{par} the parasitic current related to the measurement system. The different parameters in Equation (6) can be obtained by solving a set of four equations for four nearby diodes with different area/perimeters ratio and design layout (e.g., finger or comb structure). If the corner and the parasitic components can be neglected, then a simple graphical technique can be used to determine the other components, as illustrated in **Figure 7** for a set of $Si_{0.8}Ge_{0.2}$ diodes. The slope of the graph gives J_A, whereas J_P is obtained from the intercept.

5. CMOS Image Sensors

Since the early days, much attention has been given to charge coupled devices (CCDs) for imaging applications. A defect in a pixel leads to a white spot in the image, making these devices very sensitive to metallic contamination and/or defects such as dislocations, stacking faults, and precipitates. Since the last decade, CMOS image sensors (CIS) to replace CCDs have gained enormous interest in the field as it is a low-cost manufacturing process with a good reproducibility and enabling high-volume production and yield.

Over the years, a good control has been obtained to avoid or even eliminate extended defects so that nowadays, the main concern is focused on metallic contaminants. Since the very high sensitivity of the imager, dedicated analytical techniques have been developed such as dark current spectroscopy.[22]

Also, for CIS applications, there is a great concern about metallic contamination during ion implantation, mainly caused by possible cross contamination. A systematic study resulted in a good model for the observed dark current histograms given by[23]

$$I_{dark} = AT^3 \exp\left(-\frac{E_g}{k_B T}\right) + BT^{3/2} \exp\left(-\frac{\frac{E_g}{2} + \Delta E}{k_B T}\right) \quad (7)$$

The first term is the diffusion current, which is a measure for the recombination lifetime, while the second term is the generation current. The relative contribution to the two currents is

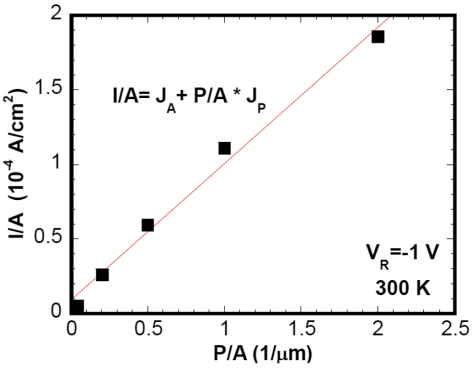

Figure 7. Current density versus P/A ration at $V_R = -1$ V and 300 K for a set of $Si_{0.8}Ge_{0.2}$ diodes.

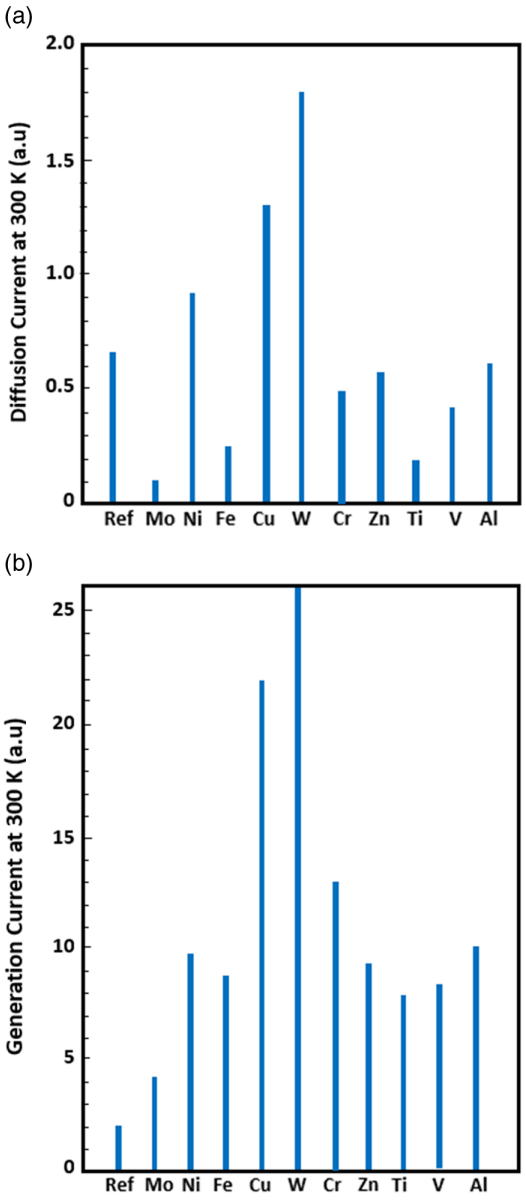

Figure 8. Impact of different metals on a) the diffusion and b) the generation current. The data are taken from Russo et al.[23]

shown in **Figure 8** for different metals. This allows to draw some conclusions:[23] 1) Mo is a slow diffusor and the number of white spots increases with the implant dose; 2) W is also a slow diffusor but a much stronger dark current generator; 3) Cu has also a rather strong impact on the dark current; 4) Ti mainly influences the generation current; and 5) the impact of Ni and Cr is rather limited.

Based on Equation (5), one can calculate how much metallic contamination can be allowed to keep the dark current below 10^{-8} A cm^{-3}, which corresponds to a space charge layer of 1 μm and a dark current of 1 pA cm^{-2}. As illustrated in **Figure 9** (based on Equation (5)), this corresponds with a Cu contamination level of 10^{9} cm^{-2}, which is much lower than the requirements for logic CMOS.[24] CIS are thus much more prone to

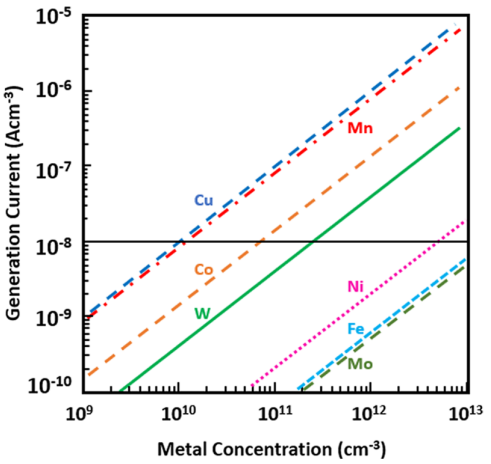

Figure 9. Calculated contribution of metal impurities to the trap-assisted dark current generated per unit volume as a function of the metal volume concentration.

metallic contamination. The present calculations are based on a simple Shockley–Read–Hall (SRH) expression, and as mentioned before, the electrical activity of the metals also strongly depends on their charge state so that additional effects (interactions with dopant atoms, extended defects, etc.) may have to be taken into account.

Because of the stringent contamination levels for CIS applications, much attention has been given to the implementation of appropriate gettering techniques. Good results have been obtained by implementing a proximity carbon-implantation which getters Fe, Ni and also slow diffusing metals such as W.[25] Besides optimizing the C implantation conditions, attention must also be given to the appropriate rapid thermal annealing (RTA) step, the post-treatments, and the design layout of the C-implantation mask, i.e., in the middle of the contact area, only on one side, or at both sides of the contact area. Some results are given as an illustration in **Figure 10**, clearly indicating the strong reduction of the white spots. The gettering of W is easier than the gettering of Fe or Ni, and the post treatment of the proximity getter process is very important for achieving an optimal reduction of the white spots.

Other approaches giving good results are based on the use of p/p^{++} epitaxial wafers and relaxation gettering-based hydrogen-ion-induced nanocavities created in the substrate underneath the depletion region of the photodiodes.[26] Some results are shown in **Figure 11**, giving for Fe, Cu, Ni, and Co the change in dark photocurrent

$$V_{\text{dark-photo}}(\%) = \frac{V_{\text{dark-photo (metal contamination)}}}{V_{\text{dark-photo (no contamination)}}} \quad (8)$$

for two different substrates, i.e., p-substrates with and without H^+ implantation (6×10^{16} cm^{-2} at 26 keV + 3 μm epitaxial layer) and p/p^{++} epitaxial wafers.

The figure allows to conclude that 1) Cu and Ni severely degrade the dark photocurrent performance; 2) H^+-cavities have a good gettering capability for all studied metals; and 3) a p/p^{++} epitaxial wafer can be used for gettering Fe but not for Cu and Ni.

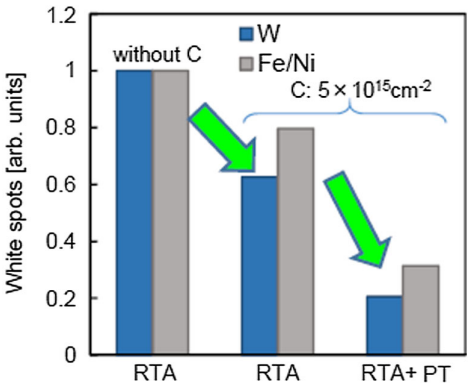

Figure 10. White spots reduction by the optimization of carbon gettering implantation and post treatment (PT). Reproduced with permission.[16] Copyright 2016, IEEE.

6. Transistor Performance

Due to the scaling of the device dimensions, the sensitivity of many analytical techniques is no longer sufficient. For dimensions below 100 nm, the device volume becomes smaller than 10^{-15} cm^{-3} making it a real challenge to detect defects. Therefore, investigation of the electrical device performance can be used to show the presence of small-size defects in low concentrations. A good example of a powerful tool for defect detection is low-frequency noise analysis, enabling to detect even single defects. Both defects in the dielectric and in the depletion layer can be detected by the investigation of the gate voltage dependence of the current noise power spectral density.[27,28]

A systematic low-frequency noise analysis in both the frequency and the time domain as a function of the operating parameters enables to determine the energy level, capture cross section and its activation energy, and the trap position with respect to the interface with the channel for individual defects.[29,30] The energy levels and capture cross sections can then be compared with, e.g., data obtained from deep-level transient spectroscopy (DLTS) studies to identify the origin of the defects. **Figure 12** illustrates the use of noise spectroscopy to show different defect levels in silicon-on-insulator (SOI) MOSFETs.[31] Four defect levels have been detected of which three could be identified by comparing with the DLTS data in the literature. The unidentified one is the most likely related to etching-induced defects.

Although the same approach can be used to study devices with metal contamination, not much information has been reported in the literature. An early report on Fe-contaminated wafers pointed out that for the studied devices, Fe had no impact on the low-frequency noise, although degradation of the lifetime and leakage were observed.[32] This may be caused by a too low contamination level and/or the dominance of possible other defects on the noise performance.

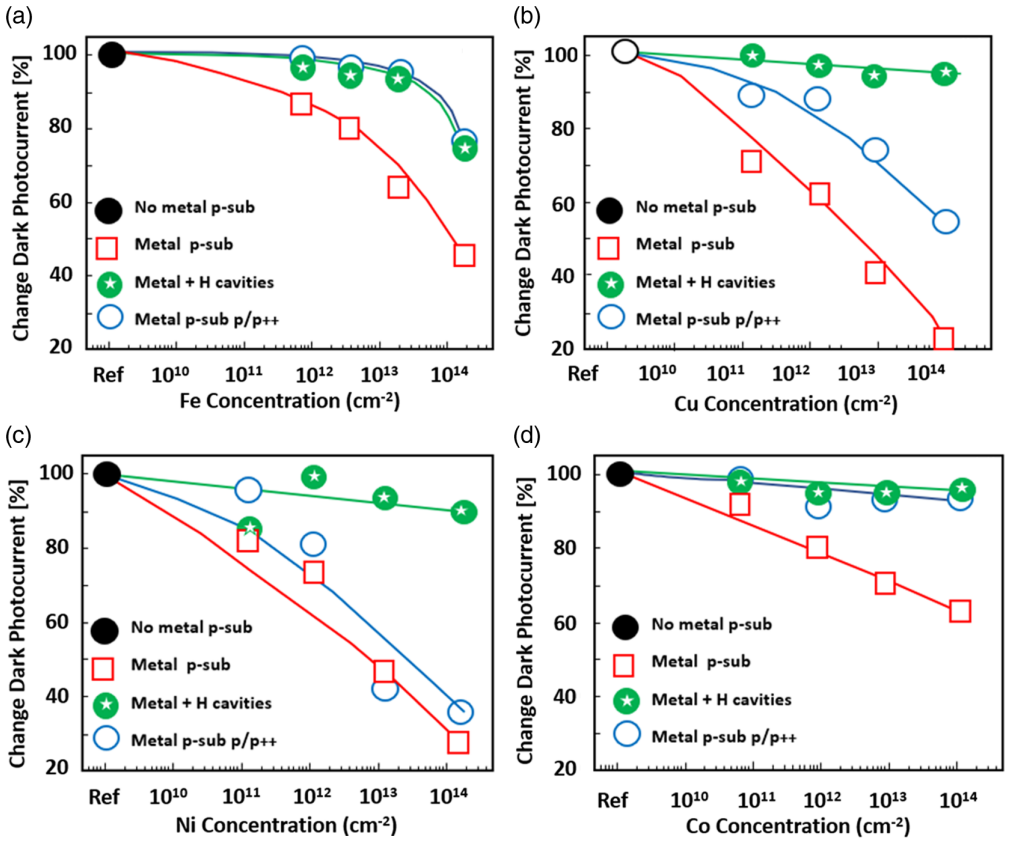

Figure 11. Change in dark photocurrent before and after contamination with a) Fe, b) Cu, c) Ni, and d) Co for different substrates and with or without hydrogen implantation (after Kim et al.[26]).

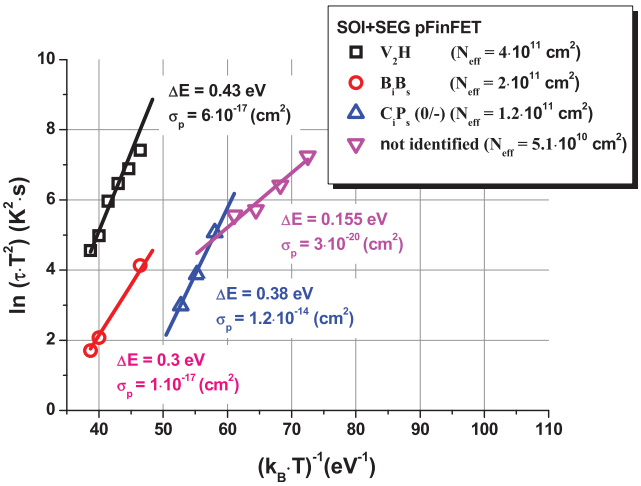

Figure 12. Arrhenius plot for a SOI MOSFET with a gate length of 1 µm, showing four different defect levels.

7. Solar Cells

Extensive studies have been reported on the impact of metallic contamination on the performance of solar cells as often metallurgical grade silicon is used as a low-cost starting material.

The metals have deep levels in the band gap, can form clusters and/or precipitates, and may decorate other extended defects present in the material, increasing their electrical activity. For multicrystalline (mc) Si metals can also precipitate at the grain boundaries increasing their electrical activity.[33] The main parameter that will be influenced is the recombination lifetime, and depending on the doping level (e.g., in the emitter region), the Auger recombination can become more dominant than

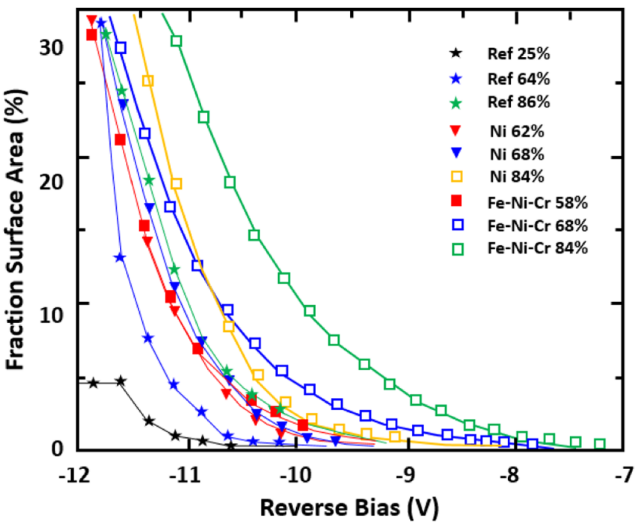

Figure 14. Fraction of the surface area which shows light emission due to breakdown. This graph shows measurements made on solar cells which were taken from the three ingots at different ingot heights (denoted by the percentage: 0% = bottom; 100% = top). Reproduced with permission.[36] Copyright 2009, AIP Publishing.

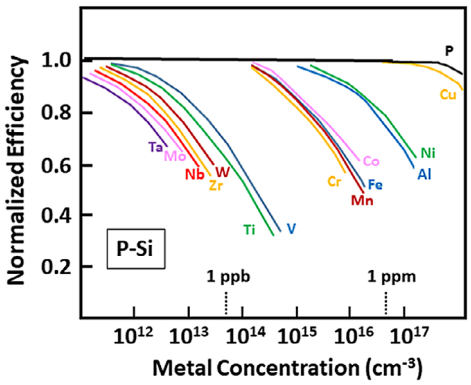

Figure 13. The effect of metallic contaminants on the solar cell efficiency. The indicated impurity concentration is that in the wafer prior to cell processing.[35]

the Shockley–Read–Hall component.[34] Besides the solar cell efficiency, metal-defects will have an impact on the open-circuit voltage V_{oc}, the short-circuit current I_{sc}, and the fill factor.

Figure 13, showing the impact of metals on the loss in solar cell efficiency, clearly indicates that a more pronounced impact is found for the slow-diffusing elements such as Mo, W, and Ti compared with the fast diffusers such as Fe, Ni, Cu, Co, and Cr.[35]

The presence of metal precipitates may also result in a local breakdown of the solar cell. This phenomenon can be observed by light emission in dedicated spots on the wafer surface. The spots can lead to a soft reverse diode behavior or a hard destructive breakdown. The origin is related to the increased electrical field at the precipitate/Si interface due to the Schottky barrier formation. This is clearly illustrated in **Figure 14**, giving for intentionally contaminated ingots the surface fraction showing light emission.[36]

In the literature, there are many reports available on the impact of specific metals such as Fe, Ti, and Au. For an in-depth review, the reader is referred to the study by Claeys and Simoen.[1]

Recently, a study has been reported on the use of a Cu/Ni contact scheme as a future viable and cost-effective contact technology for solar cells.[37] Although this leads to a high-conductivity and low-contact resistance, there is a risk that metal contamination may degrade the cell performance.

In the passivated emitter and rear cell (PERC) solar cell, the plated Ni layer acts as a diffusion barrier for Cu as shown in **Figure 15**.

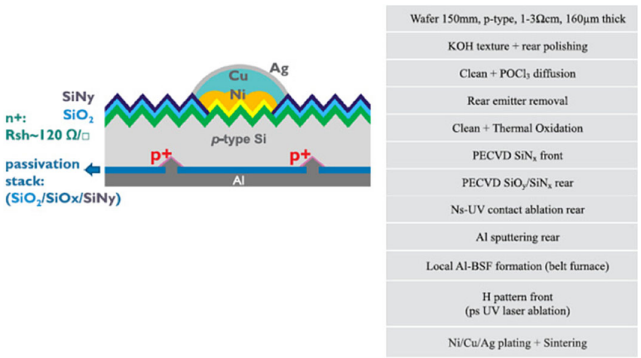

Figure 15. Schematic drawing and process sequence of a PERC solar cell. Reproduced with permission.[37] Copyright 2018, Elsevier.

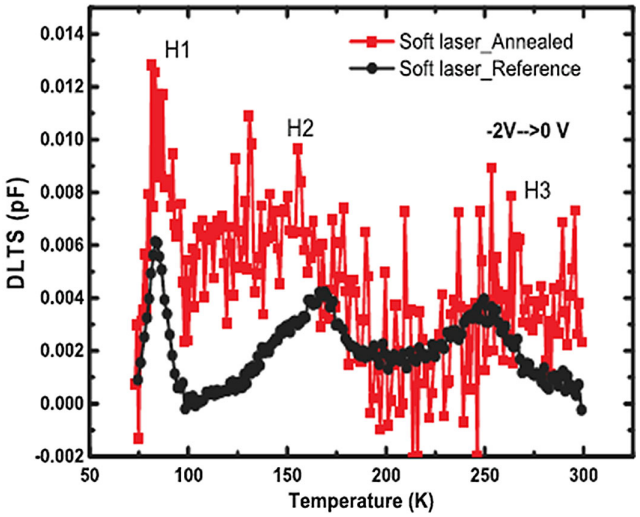

Figure 16. DLTS spectra before and after annealing for a PERC sample prepared by soft laser ablation. Reproduced with permission.[37] Copyright 2018, Elsevier B.V.

After the deposition of the backside Al layer, laser ablation is used to open the contact area before the Ni plating.

A DLTS study showed a hole trap H1 around 80 K, as shown in **Figure 16**.[37] Arrhenius plot analysis and comparison with the literature data pointed out that the trap corresponds with the substitutional Ni_s donor, and its concentration is not influenced by thermal annealing after the sintering step. The concentration of Ni is estimated at about 10^{11}–10^{12} cm^{-3}. The Ni may impact the recombination activity, especially when it interacts with the dislocations induced during the laser ablation step.

Normally, Ni is interstitially incorporated in the lattice but becomes substitutional by interacting with vacancies, which are released by dislocations.[38] Therefore, more Ni_s is found in samples with hard laser ablation because these samples have a higher dislocation density than soft laser ablated samples.[37] No migration of the Cu in the p-type Si base has been observed by DLTS.

8. Density Functional Calculations

To develop theoretical defect models, it is essential to have information on the different defect structures, to be able to define the lowest-energy state, and to get insight in the migration and diffusion properties of the metals. Electron paramagnetic resonance (EPR) is a powerful but also time-consuming analytical technique. Experimental observations of several transition metals have been explained based on both the Ludwig and Woodbury[39] model for the interstitial and substitutional T_d sites of the metal and the Watkins vacancy model[40] for the substitutional T_d site for heavy metals like Au, Ag, and Cu.

Over the last two decades, enormous progress has been achieved on the use of first-principle techniques for calculating deep levels and vibration spectra. The first total energy calculations were performed for Cu in Si, based on the Hartree–Fock theory, using 44 host Si atoms in the super cell.[41]

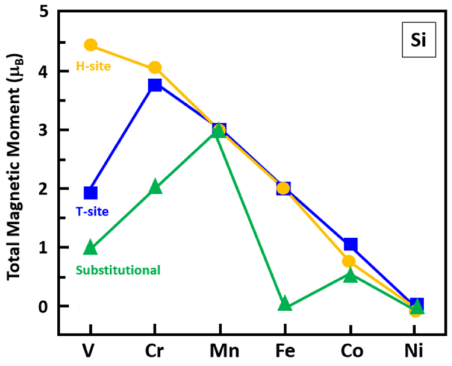

Figure 17. Total magnetic moments for a TM atom doped in Si at a substitutional site, an interstitial site with tetrahedral symmetry ,and an interstitial site with hexagonal symmetry. Reproduced with permission.[42] Copyright 2008, American Physical Society.

An illustration of the DFT calculations for the magnetic moment μ_B of the 3D series of metals is given in Figure 17.[42] The explanation is based on a simple filling scheme leading to the 5, 4, and 3 μ_B for vanadium, chromium, and manganese, respectively. Similar calculations have been done for the magnetic moments of these transition metals (TMs) in Ge.[43]

The DFT approach has also successfully been used to study radiation and implantation defects such as the divacancy (V_2), the oxygen-vacancy (VO), and the dioxygen-vacancy (VO_2). Additionally, the binding energy of TM with these defects can be calculated as shown in **Figure 18** for VO and VO_2 in silicon.[44] It can be noticed that some metals have a stronger binding energy than other. The gettering by VO_2 is smaller compared with the getter action of the VO complex. For the latter, the stable position of the Fe atom is at the interstitial site. As a reference, the binding energy of the BFe complex is also indicated.

These ab initio calculations turn out to be very helpful in the atomistic understanding and optimization of metal gettering approaches. It can also lead to new insights in the physics behind gettering schemes such as the phosphorus diffusion gettering (DFG). For a long time, it was believed that the P diffusion was dominant for the gettering by the injection of self-interstitials associated with the dissociation of the PI pairs.[45] However, ab initio calculations demonstrated that the Fe gettering occurs by the dominant P_4V site forming M-PV_4 complexes.[46]

A final example of ab initio calculations is related to the effectiveness of Fe and Ti gettering by a p/p^+ epitaxial wafer, as shown

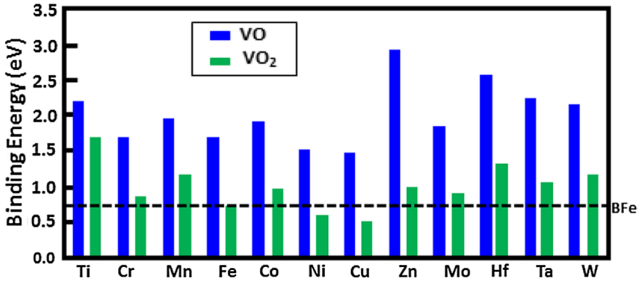

Figure 18. Binding energy for different metals to VO and VO_2 defects in silicon. Reproduced with permission.[44] Copyright 2016, Elsevier B.V.

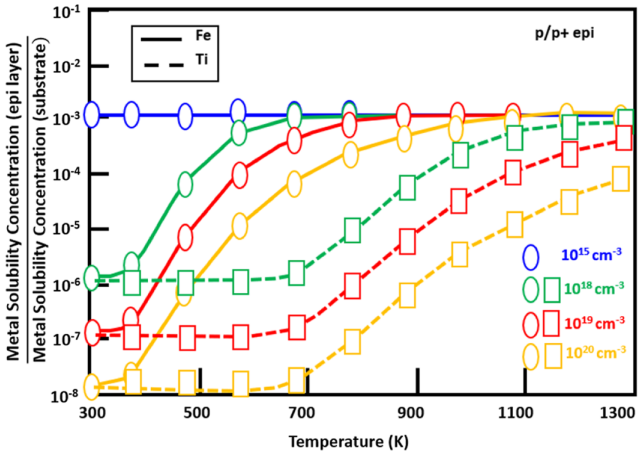

Figure 19. Temperature dependence of the ratio of the equilibrium metal solubility concentration in the epi-layer and in the substrate for Fe and Ni in p/p^+ epitaxial silicon wafers (based on data from Yamada and Sueoka[47]).

in **Figure 19** for DFT calculations in the 10^{15}–10^{20} cm^{-3} boron doping range.[47] In the case that the p-substrate has the same doping concentration as the epitaxial layer, no gettering occurs as the concentration ratio is then equal to the thickness ratio epi-layer and substrate. It can be noticed that Fe gettering works well for $T < 400$ K, while this is the case below 700 K for Ti. For Fe, one can notice that most of the Fe atoms are not gettered for $T > 700$ K (1100 K); for an epi B concentration of 10^{18} (10^{20}) cm^{-3} of the p^+ silicon substrate, Ni gettering starts at about 600 K and is very effective below 300 K.[44] For Hf atoms, the temperatures are 1300 and 700 K.

Besides getting fundamental insight by DFT calculations, the exercise can be extended by adding continuum modeling and device simulation enabling to use realistic process conditions and to predict the device performance.

9. Conclusion

Metal contamination control remains an important challenge for silicon processing both for logic technologies, CIS applications, and solar cells. Although many of the classical sources of metallic contamination have been suppressed or eliminated, one has to remain careful with ion implantation and the introduction of advanced metal-based process modules (ferroelectrics, BEOL, TSV, etc.).

The impact of metals on the device performance is directly linked to the basic metal properties such as solubility, diffusivity, defect configuration, precipitation, clustering, energy levels in the band gap, and defect signature. The metal configuration in the lattice (interstitial, substitutional or precipitate), which depends on the type of metal and the thermal history of the material, has a strong impact on the electrical activity of the metal.

Because of the stringent requirements put on allowable metal concentrations, the optimization of appropriate gettering schemes remains of crucial importance. Fundamental insight and modeling based on the DFT approaches are a very strong starting basis and can be linked to process and device modeling. Of all analytical techniques, the microelectronics device itself remains one of the most sensitive tools for showing the presence of defects and metallic contamination.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

complementary metal-oxide-semiconductor (CMOS) imagers, diode analysis, functional density theory, low-frequency noise, metal-oxide-semiconductor capacitors, solar cell efficiencies, transition metals

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