Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors

Ning Xu,[1,2,a)] Ronghui Hao,[2,3,a)] Fu Chen,[1,2] Xiaodong Zhang,[2] Hui Zhang,[2,4] Peipei Zhang,[2,4] Xiaoyu Ding,[2,3] Liang Song,[1,2] Guohao Yu,[2,b)] Kai Cheng,[5] Yong Cai,[2,b)] and Baoshun Zhang[2,6,b)]

[1]*School of Nano Technology and Nano Bionics, University of Science and Technology of China, Hefei 230026, China*
[2]*Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics, CAS, Suzhou 215123, China*
[3]*School of Materials Science and Engineering, Nanjing University of Science and Technology, Nanjing 210094, China*
[4]*The College of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China*
[5]*Enkris Semiconductor, Suzhou 215123, China*
[6]*Suzhou Powerhouse Electronics Co., Ltd, Suzhou 215123, China*

(Received 24 May 2018; accepted 26 September 2018; published online 11 October 2018)

In this letter, gate leakage mechanisms in different gate contact normally off p-GaN/AlGaN/GaN high electron mobility transistors (HEMTs) have been studied by the temperature-dependent current-voltage (I_G-V_G) measurement. It is found that two-dimensional variable range hopping is responsible for gate leakage current at the reverse gate bias and low forward gate bias in both high-leakage and low-leakage Schottky gate contact devices. At high forward gate bias, in the case of high-leakage Schottky contact, the dominant current conduction mechanism is found to be thermionic field emission while it is Poole–Frenkle emission (PFE) for the case of low-leakage Schottky contact and the activation energy of trap states for PFE current is derived as 0.6 eV. Besides, related models are also proposed to describe the gate leakage current in p-GaN gate HEMTs and they match well with the experimental gate leakage current within a wide range of temperatures and gate biases. *Published by AIP Publishing.* https://doi.org/10.1063/1.5041343

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) show tremendous potential for high power, high frequency, and high efficiency power switching applications due to the outstanding properties of the GaN material (e.g., wide bandgap, high-electron saturation velocity, and large breakdown electric field).[1,2] However, the inherent high density two dimensional electron gas (2DEG) existing in the gate region of the common AlGaN/GaN HEMTs can result in normally on operation.[3] For the consideration of fail-safe and simplifying the gate drive topology, normally off devices are preferred in the practical power switching applications. Among solutions,[4–6] normally off p-GaN gate HEMTs, which lift up the conduction band beyond the Fermi level by the p-n junction built-in electric field, have drawn a lot of attention and are now commercial available from a broad range of suppliers.[7]

Gate leakage current is an important parameter for GaN HEMTs, and it can affect device performance and reliability. For instance, the forward gate leakage current limits the gate voltage swing and causes drive losses, while the reverse one can lead to off-state power consumption and limit breakdown voltage.[8,9] Therefore, research studies on gate leakage mechanisms are necessary before we can take effective solutions. Nowadays, the mechanisms of the gate current transport in Schottky AlGaN/GaN HEMTs and metal insulator semiconductor HEMTs (MIS-HEMTs) have been thoroughly investigated and interpreted by different models.[10–14] However, so far, gate leakage mechanisms in p-GaN gate HEMTs are still unclear.[15] The gate contacts of p-GaN gate HEMTs can be divided into high-leakage (e.g., Pd) and low-leakage (e.g., W, WSiN, Ti/Al, and TiN) contacts according to the value of forward gate leakage current.[5,15–18] However, no matter what kind of gate contact, a Schottky barrier always exists at metal/p-GaN due to the high work function and low hole concentration of p-GaN, which makes it difficult to analyze the gate current transport mechanisms in p-GaN gate HEMTs.[19,20] In this work, we investigate the conduction mechanisms of gate leakage current in p-GaN gate HEMTs fabricated by hydrogen plasma treatment.

The p-GaN/AlGaN/AlN/GaN (70 nm/18 nm/1 nm/4.35 μm) epi-structure was grown on a 2-in. p-type Si (111) substrate by metal organic chemical vapor deposition (MOCVD). The p-GaN gate HEMTs in this work were fabricated by hydrogen plasma treatment, and their schematic cross-section is shown in Fig. 1(a).[21,22] The device fabrication flow is the same as the previous work expect for the gate metal.[23] Pd/Au and Ti/Au metal stacks with the same thickness of 50/150 nm were applied to form the gate electrodes for device A and device B, respectively. Device B was passivated by a 300 nm SiNx deposited using plasma enhanced chemical vapor deposition (PECVD). The measured devices in this work have the same dimensions of $L_{GS}/L_G/L_{GD}/W_G = 4/2/15/100$ μm. With a drain current criterion of $I_D = 10$ μA/mm, the threshold voltage is determined to be 1 V and 1.2 V for device A and device B, respectively. The forward gate

[a)]Ning Xu and Ronghui Hao contributed equally to this work.
[b)]Authors to whom correspondence should be addressed: ghyu2009@sinano.ac.cn; ycai2008@sinano.ac.cn; and bszhang2006@sinano.ac.cn

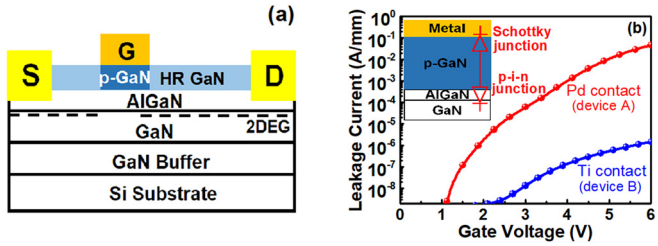

FIG. 1. (a) The schematic cross-section of the fabricated p-GaN gate HEMTs. (b) Forward I_G-V_G characteristics of Pd contact (red) and Ti contact (blue) devices at RT. The inset depicts the gate structure of the fabricated p-GaN gate HEMTs.

leakage currents of the two devices at room temperature (RT) are shown in Fig. 1(b) ($V_D = V_S = 0$ V). Due to the work function difference between Pd (5.12 eV) and Ti (4.33 eV), I_G of device A at $V_G = 6$ V is approximately four orders of magnitude higher than that of device B. Therefore, device A and device B are referred to as the high-leakage and low-leakage Schottky gate contact cases, respectively.[24]

I_G-V_G characteristics of device A and device B measured at elevated temperatures from 298 to 473 K in steps of 25 K are shown in Figs. 2(a) and 2(b) and they are used to analyze the gate leakage mechanisms in high-leakage and low-leakage Schottky gate contact cases, respectively. The I_G-V_G characteristics of both devices can be divided into three regions, namely, region-I (reverse gate bias), region-II (low forward gate bias), and region-III (high forward gate bias). The insets of Figs. 2(a) and 2(b) show I_G-V_G characteristics of both devices in the linear coordinate, respectively. As can be seen, the I_G of both device A and device B increases nearly linearly as the $|V_G|$ increases in region-I and region-II. Two-dimensional variable range hopping (2D-VRH) is one of the possible mechanisms and it can be described by the following simple expression:[25]

$$\sigma \propto \exp\left[-\left(\frac{1}{T}\right)^{\frac{1}{3}}\right], \tag{1}$$

where σ is the conductance, and T is the absolute temperature. The temperature dependences of I_G of device A and device B at $V_G = -4$ V (region-I) and $V_G = 0.6$ V (region-II) are shown in Fig. 3. The lnσ gives a straight line with $1/T^{1/3}$ at various temperatures from 298 K to 473 K, indicating that gate current is proportional to $\exp(-1/T^{1/3})$. Device A and device B are unpassivated and passivated (300 nm SiN_x), respectively. As illustrated in Fig. 3, the fitting curves of

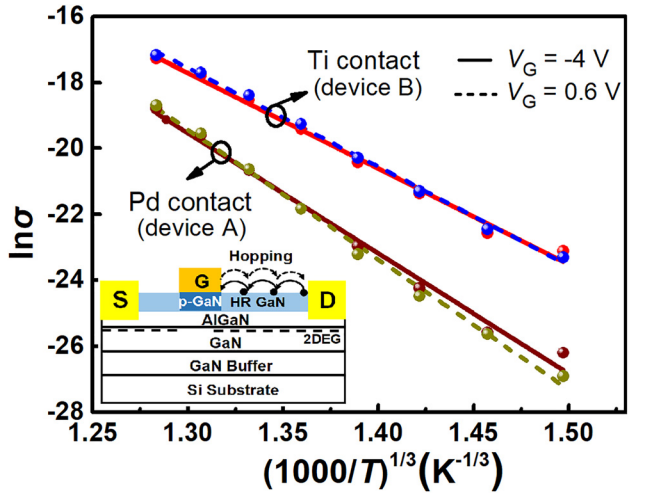

FIG. 3. lnσ of device A and device B at $V_G = -4$ V and $V_G = 0.6$ V as a function of $1/T^{1/3}$ showing straight lines. The inset shows the 2D-VRH along the HR-GaN surface in the p-GaN gate HEMTs.

device A and device B have different slopes, indicating that SiN_x passivation can affect the gate leakage current as well as the fitting slope. Therefore, it is believed that 2D-VRH is the main gate leakage current transport mechanism in region-I and region-II. As shown in the inset of Fig. 1(b), two back-to-back junctions, the Schottky metal/p-GaN junction (Schottky junction) and the p-GaN/AlGaN/GaN junction (p-i-n junction), are included in the gate structure of both devices. At reverse bias, vertical gate current is blocked due to the reverse bias of the p-i-n junction. The vertical gate current is also small when the forward bias is low since the voltage drop at the p-i-n junction is below the forward turn-on voltage. Thus, surface current can be responsible for I_G in region-I and region-II. The p-GaN gate HEMTs were fabricated by H plasma in our experiment, and the plasma could cause damage to the surface and form traps.[22] Therefore, these traps could form surface current along the high-resistivity GaN (HR-GaN). A similar conclusion has also been reported for p-GaN gate HEMTs fabricated by etching technology.[15] Also, the relationship between the H plasma power and the surface current needs further investigation.

The schematic band diagrams of devices A and B at high forward gate bias (region-III) are shown in Figs. 4(a) and 4(b), respectively, and the difference between them mainly depends on the gate metal work function. For device A, as shown in Fig. 4(a), the current is limited by the Pd/p-GaN Schottky junction. According to metal-semiconductor contact

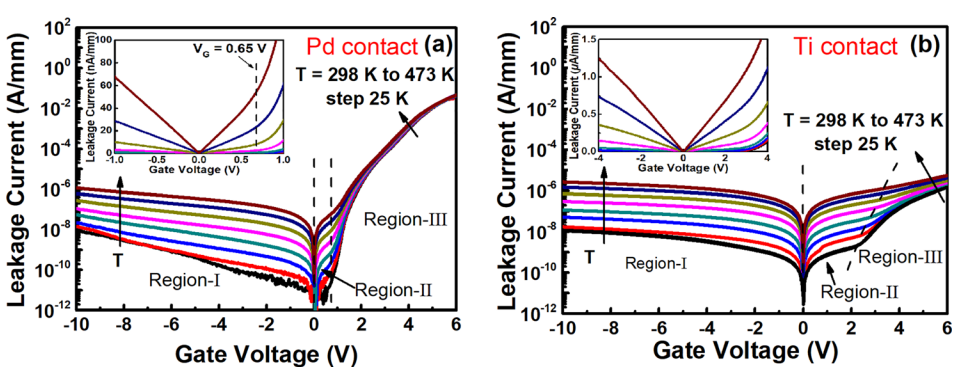

FIG. 2. Temperature-dependent I_G-V_G characteristics of (a) high-leakage (device A) and (b) low-leakage (device B) Schottky contact p-GaN gate HEMTs.

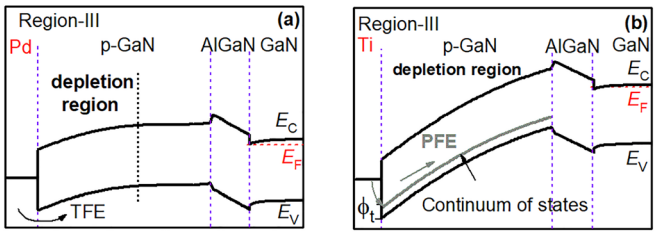

FIG. 4. The schematic band diagram in region-III of (a) device A and (b) device B.

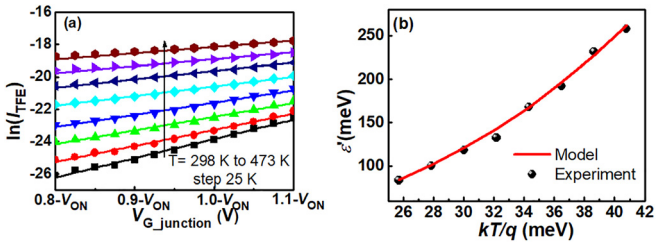

FIG. 5. (a) TFE plots [ln(J_{TFE}) vs. $V_{G\_junction}$] of device A. (b) Experimental and theoretical values of ε' as a function of kT/q for device A.

theory,[26] the current conduction mechanisms are related to the tunneling parameter (E_{00}). Taking the Mg doping concentration (N_A) of $2 \times 10^{19}\,\mathrm{cm}^{-3}$ into consideration, the value of E_{00}/kT is in the range between 0.85 and 1.20 in the examined temperature range. This implies that thermionic field emission (TFE) ($0.6 < E_{00}/kT < 1.4$) should be the dominant mechanism of current transport in region-III of device A.[20] Hence, the expression of the TFE reverse current is used to fit the experimental data[17,27]

$$I_{TFE} = I_s \cdot \exp\left[qV_{G\_junction}/\varepsilon'\right], \tag{2}$$

with

$$\varepsilon' = \frac{kT \cdot E_{00} \coth\left(\frac{E_{00}}{kT}\right)}{kT - E_{00} \coth\left(\frac{E_{00}}{kT}\right)} \quad \text{and} \quad E_{00} = qh/4\pi\sqrt{N_A/m^*\varepsilon}, \tag{3}$$

where I_s is the saturation current, q is the elementary charge, $V_{G\_junction}$ is the voltage across the Schottky junction, k is the Boltzmann constant, and h is Planck's constant. In the above expressions, ε and m^* represent the dielectric constant of p-GaN and the effective mass of holes in p-GaN, respectively. $\varepsilon = 8.9\varepsilon_0$, where ε_0 is the permittivity of free space, and $m^* = 0.81\,m_0$, with m_0 being the free electron mass, are adopted. Tallarico *et al.* found that the applied positive gate voltage drops almost at the p-GaN/AlGaN/GaN junction before its forward turn-on, while the additional applied gate voltage drops nearly across the depletion region of the gate metal/p-GaN Schottky junction after the p-GaN/AlGaN/GaN junction's forward turn-on.[28] As a result, $V_{G\_junction}$ in region-III can be estimated as $V_{G\_junction} \approx V_G - V_{ON}$, V_{ON} is the p-GaN/AlGaN/GaN junction forward turn-on voltage and it is less than 0.65 V in this paper, since the p-GaN/AlGaN/GaN junction is already forward turn-on in region-III ($V_G > 0.65$ V). From Eq. (2), the plot of ln (I_{TFE}) vs. $V_{G\_junction}$ should yield straight lines with slopes of q/ε'. Figure 5(a) shows that ln (I_{TFE}) indeed gives straight lines with $V_{G\_junction}$ for temperature from 298 K to 473 K. Also, the extracted ε' is in good agreement with the theoretical curve obtained by Eq. (3) [Fig. 5(b)], verifying that the TFE is the dominant mechanism in region-III for the high-leakage Schottky contact case (Pd contact).

The TFE model has also been attempted for the Ti contact case (device B) at the high forward gate bias. However, the fitting results are inconsistent with the experimental data (not shown here). This phenomenon could be related to the low work function of Ti, which causes a higher Schottky barrier and a wider depletion region in the Ti/p-GaN Schottky junction compared to the Pd contact case [Fig. 4(b)]. In this case, some other trap-related current conduction mechanisms could become the dominate gate leakage mechanism due to the high trap density in p-GaN and higher electric field in p-GaN compared to the Pd contact case.[12] As shown in Fig. 2(b), the measured I_G of device B in region-III depends on not only the electric field but also temperature, indicating that Poole–Frenkle emission (PFE) may be the more likely current conduction mechanism (PFE shows a dependence on both the electric field and temperature).[12] For the low-leakage Schottky contact case, a two-junction capacitor model has been proposed[29]

$$\frac{1}{C_{total}} = \frac{1}{C_{junction}} + \frac{1}{C_{AlGaN}}, \tag{4}$$

where C_{total}, $C_{junction}$, and C_{AlGaN} are the total capacitor, the capacitor of the Ti/p-GaN Schottky junction, and the capacitor of junction across the AlGaN barrier, respectively. C_{AlGaN} can be simply calculated by using the ideal dielectric constant of the $Al_{0.2}Ga_{0.8}N$ ($\varepsilon_{AlGaN} = 8.8\varepsilon_0$). $C_{junction}$ is given by[29]

$$C_{junction} = \sqrt{\frac{q\varepsilon N_A}{2(V_{bi} + V_{G\_junction})}}, \tag{5}$$

where V_{bi} is the built-in potential of the Ti/p-GaN junction [$V_{bi} = \Phi_s - \Phi_m = \chi + E_g/q - \eta_p/q - \Phi_m$, where Φ_s is the p-GaN work function and $\eta_p = kT\ln(N_v/p)$, where N_V is the valence band density of states]. Based on this two-junction capacitor model, $V_{G\_junction}$ at a given V_G can be calculated, since $C_{junction}V_{G\_junction} = C_{AlGaN}V_{AlGaN}$. Furthermore, the effective electric field across p-GaN can be estimated by

$$E \approx \frac{V_{G\_junction}}{t_d}, \tag{6}$$

where t_d is the thickness of the depletion region in p-GaN. J_{PFE} can be expressed as[12–14]

$$\ln\left(\frac{J_{PFE}}{E}\right) = \mathrm{m(T)}\sqrt{E} + c(\mathrm{T}), \tag{7}$$

with

$$\mathrm{m(T)} = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon}}, \quad c(\mathrm{T}) = -\frac{q\Phi_t}{kT} + \ln C, \tag{8}$$

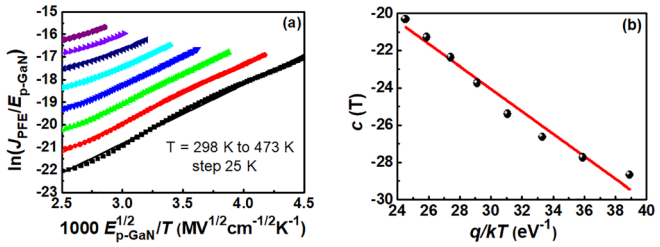

FIG. 6. (a) PFE plots [$\ln(J_{PFE}/E)$ vs. $1000E^{1/2}/T$] of device B. (b) The plot of c(T) versus q/kT of device B.

where Φ_t is the barrier height for the electron emission from the trap states, and C is a constant associated with PFE. Figure 6(a) shows that the plots of $[\ln(J_{PFE}/E)$ vs. $1000E^{1/2}/T]$ yield straight lines, indicating that PFE is the dominate mechanism. The plot of c(T) versus q/kT is shown in Fig. 6(b), and the Φ_t is estimated to be 0.6 eV.

The gate leakage current in p-GaN gate HEMTs can be modeled as a combination of voltage and temperature dependent current sources connected in parallel. The total gate leakage current (I_G) can be expressed by

$$I_G = I_{2D-VRH} + I_{TFE} \tag{9}$$

or

$$I_G = I_{2D-VRH} + I_{PFE} \tag{10}$$

where $I_{2D\text{-}VRH}$, I_{TFE}, and I_{PFE} are the current related to 2D-VRH, TFE, and PFE, respectively. The expressions for $I_{2D\text{-}VRH}$, I_{TFE}, and I_{PFE} are given by Eqs. (1), (2), and (7), respectively. Figures 7(a) and 7(b) compare the results from Eqs. (9) and (10) with experimental results at 298 K, 373 K and 473 K for high-leakage and low-leakage Schottky contact p-GaN gate HEMTs, respectively, and components of leakage currents are also exhibited for reference. Good agreement between the experimental data and model results within a wide range of temperatures and gate biases can be seen, which demonstrates the proposed models.

In summary, an investigation of the gate leakage current mechanisms in p-GaN gate HEMTs has been performed. At reverse gate bias or low forward gate bias, 2D-VRH is found to be the dominant mechanism of gate current for both high-leakage and low-leakage Schottky gate contact cases. At high forward bias, the gate leakage transport in the high-leakage Schottky contact case is dominated by TFE, while PFE becomes dominant in the case of low-leakage Schottky contact. According to the gate leakage current mechanisms, models to describe the gate leakage current in p-GaN gate HEMTs have been proposed and fit well with the experimental results over a wide range of biases and temperatures.

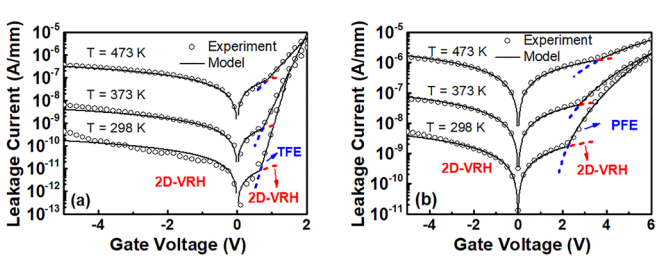

FIG. 7. I_G-V_G characteristics comparing the models with the experimental data of (a) high-leakage and (b) low-leakage Schottky contact p-GaN gate HEMTs.

This work was supported in part by the National Natural Science Foundation of China (Grant No. 61704185), the Key Research and Development Program of Jiangsu Province (Grant No. BE2016084), the Natural Science Foundation of Jiangsu Province (Grant No. BK20160400), and the National Natural Science Foundation of China (Grant No. 61774014). The authors would like to thank the Nano Fabrication Facility, Platform for Characterization and Test, Nano-X of Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, and Enkris Semiconductor for their technical support.

[1]K. J. Chen, O. Haberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. F. Wu, IEEE Trans. Electron Devices **64**, 779 (2017).
[2]L. Efthymiou, G. Longobardi, G. Camuso, T. Chien, M. Chen, and F. Udrea, Appl. Phys. Lett. **110**, 123502 (2017).
[3]O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, J. Appl. Phys. **87**, 334 (2000).
[4]Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, IEEE Electron Device Lett. **26**, 435 (2005).
[5]Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, and M. Yanagihara, IEEE Trans. Electron Devices **54**, 3393 (2007).
[6]H. Y. Wang, J. Y. Wang, J. Q. Liu, M. J. Li, Y. D. He, M. J. Wang, M. Yu, W. G. Wu, Y. Zhou, and G. Dai, Appl. Phys. Express **10**, 106502 (2017).
[7]E. A. Jones, F. F. Wang, and D. Costinett, IEEE J. Emerging Sel. Top. Power Electron. **4**, 707 (2016).
[8]M. Meneghini, I. Rossetto, M. Borga, E. Canato, C. D. Santi, F. Rampazzo, G. Meneghesso, and E. Zanoni, in *IEEE International Reliability Physics Symposium*, Monterey, USA, 2–6 April 2017, p. 4B-5.1.
[9]M. H. Mi, X. H. Ma, L. Yang, H. Bin, J. J. Zhu, Y. L. He, M. Zhang, S. Wu, and Y. Hao, Appl. Phys. Lett. **111**, 173502 (2017).
[10]Y. Li, G. I. Ng, S. Arulkumaran, G. Ye, Z. H. Liu, K. Ranjan, and K. S. Ang, J. Appl. Phys. **121**, 044504 (2017).
[11]S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta, and N. D. Gupta, IEEE Trans. Electron Devices **60**, 3157 (2013).
[12]G. Dutta, N. D. Gupta, and A. D. Gupta, IEEE Trans. Electron Devices **64**, 3609 (2017).
[13]M. Y. Hua, C. Liu, S. Yang, S. H. Liu, K. Fu, Z. H. Dong, Y. Cai, B. S. Zhang, and K. J. Chen, IEEE Trans. Electron Devices **62**, 3215 (2015).
[14]J. J. Zhu, X. H. Ma, B. Hou, W. W. Chen, and Y. Hao, Appl. Phys. Lett. **104**, 153510 (2014).
[15]J. H. Bae, S. Hwang, J. Shin, H. I. Kwon, C. H. Park, H. Choi, J. B. Park, J. Kim, J. B. Ha, K. Park, J. Oh, J. K. Shin, U. Chung, K. S. Seo, and J. H. Lee, in *IEEE Electron Devices Meeting*, Washington, USA, 9–11 December 2013, pp. 786–789.
[16]M. Meneghini, O. Hilt, J. Würfl, and G. Meneghesso, Energies **10**, 153 (2017).
[17]G. Greco, F. Iucolano, S. D. Franco, C. Bongiorno, A. Patti, and F. Roccaforte, IEEE Trans. Electron Devices **63**, 2735 (2016).
[18]T. L. Wu, D. Marcon, S. Z. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. V. Hove, G. Groeseneken, and S. Decoutere, IEEE Electron Device Lett. **36**, 1001 (2015).
[19]J. Simon, V. Protasenko, C. Lian, H. Xing, and D. Jena, Science **327**, 60 (2010).
[20]J. S. Jang and T. Y. Seong, Appl. Phys. Lett. **76**, 2743 (2000).
[21]R. H. Hao, K. Fu, G. H. Yu, W. Y. Li, J. Yuan, L. Song, Z. L. Zhang, S. C. Sun, X. J. Li, Y. Cai, X. P. Zhang, and B. S. Zhang, Appl. Phys. Lett. **109**, 152106 (2016).
[22]R. H. Hao, N. Xu, G. H. Yu, L. Song, F. Chen, J. Zhao, X. G. Deng, X. Li, K. Cheng, K. Fu, Y. Cai, X. P. Zhang, and B. S. Zhang, IEEE Trans. Electron Devices **65**, 1314 (2018).

[23]R. H. Hao, W. Y. Li, K. Fu, G. H. Yu, L. Song, J. Yuan, J. S. Li, X. G. Deng, X. D. Zhang, Q. Zhou, Y. M. Fan, W. H. Shi, Y. Cai, X. P. Zhang, and B. S. Zhang, IEEE Electron Device Lett. **38**, 1567 (2017).
[24]L. Sayadi, G. Iannaccone, S. Sicre, O. Haberlen, and G. Curatola, IEEE Trans. Electron Devices **65**, 2454 (2018).
[25]J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, Appl. Phys. Lett. **91**, 093501 (2007).
[26]A. Y. C. Yu, Solid-State Electron. **13**, 239 (1970).
[27]F. A. Padovani and R. Stratton, Solid State Electron. **9**, 695 (1966).
[28]A. N. Tallarico, S. Stoffels, P. Magnone, N. Posthuma, E. Sangiorgi, S. Decoutere, and C. Fiegna, IEEE Electron Device Lett. **38**, 99 (2017).
[29]T. L. Wu, B. Bakeroot, H. Liang, N. Posthuma, S. Z. You, N. Ronchi, S. Stoffels, D. Marcon, and S. Decoutere, IEEE Electron Device Lett. **38**, 1696 (2017).