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Effect of the charge state of traps on the transport current in the SiC/Si heterostructure

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Abstract. Forward and reverse currents in the heterostructure «amorphous SiC/*p*-Si» were studied in the temperature range 30 – 80 K. It has been found that in different ranges of the applied voltage the transport current is described by different mechanisms. Charging the electron traps situated in the SiC layer increases the forward current due to reduction of the potential barrier for holes. In the range of forward biases 0.5 – 0.8 V the current is controlled by variable-range hopping of holes in the amorphous SiC according to the Mott's mechanism. At higher voltages the dominant mechanism controlling the current becomes the hole tunneling across the triangular barrier in the amorphous-crystalline semiconductor interface.

Keywords: heterostructure, transport current, low temperature

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1. Introduction

Studies of amorphous SiC / crystalline Si heterojunctions are of interest from the viewpoint of potential application of silicon carbide to high-temperature microelectronics [1], and optoelectronics [2]. The use of amorphous silicon carbide is preferable, compared with use of the single-crystalline material, because the temperature of its formation is relatively low, which provides better compatibility of fabrication of silicon carbide with the current silicon technology. The physical properties of shallow electrically active centres in SiC and at the SiC/Si interface are less studied to date, although the presence of such centres, associated with structural defects, dramatically affects the parameters responsible for the operating efficiency of optoelectronic and microelectronic devices.

In our previous paper [3] the results were reported of investigations of electrophysical properties of the SiC-pSi heterostructure using thermally stimulated charge release (TSCR) technique. It has been shown that this heterostructure contains three systems of electrically active centres possessing levels near the edges of the band gap. In the silicon carbide layer the system of shallow electron levels was found located in the ranges from E_c - 0.08 to E_c - 0.22 eV near the bottom of the conduction band and spatially distributed over the whole layer thickness.

The aim of this paper is to clarify the transport mechanisms in «amorphous SiC – crystalline *p*-Si» heterojunctions. In the paper, results of measurements of forward and reverse current-voltage (*I–V*) and current-temperature (*I–T*) characteristics in the SiC/Si heterojunction in the temperature range from 30 to 80 K are presented, and the effect of the charge state of electron centres in the SiC layer on the transport current is studied. Based on experimental results, the possible transport mechanisms at various temperatures and electric fields are discussed.

2. Experimental

The SiC layer was deposited onto the silicon wafer using a low-pressure chemical vapour deposition (LPCVD) technique in an atmosphere of methyltrichlorosilane with hydrogen as carrier gas at temperature 1000 °C. The thickness of the SiC layer was 1.1 μm. Measurements were carried out on the Al-SiC-*p*-Si structure. The aluminium capacitor's area was 0.001 cm^2. Ohmic contact was cre-

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ated at the back side of the wafer. The character of the current transport was studied either by measuring the set of *I–V* characteristics at several values of temperature, or by measuring the set of temperature dependencies of the current (*I–T* characteristics) at a fixed bias voltage applied to the structure [4, 5]. I-V characteristics were measured at linear voltage sweep at the metal electrode with the rate 0.12 V/s.

Filling of the system of electron traps situated in the silicon carbide layer was performed by applying the positive bias to the aluminium electrode (reverse biased heterojunction) at some fixed temperature (about 120 K). Cooling the sample to a lower temperature and switching off the filling voltage turns the system into the non-equilibrium state with a fraction of charge being trapped in the centres of the SiC layer. Investigations of the TSCR currents from these centres [3] have shown that at temperatures below 80 K the major part of charge remains trapped unless a high negative voltage (forward biased heterojunction) is applied to the metal electrode.

3. Results and discussion

3.1. Capacitance-voltage characteristics

In [3] capacitance-voltage (*C–V*) characteristics of the investigated structure have been presented, and it was shown that at low temperatures and a high measuring frequency the silicon carbide layer behaves itself as an insulator so that concentration carrier profiling in silicon becomes possible. In [6] an approach to the treatment of *C–V* curves has been suggested for an «unimplanted a-Si:H/pSi» structure. This method allows one to determine an effective density of localized gap states in an amorphous material from results of *C–V* measurements, if an impurity density in a crystalline material is known. First, from the *C–V* data the square of the space charge region length in a crystalline material W_1^2 is calculated as a function of applied voltage. An intercept of this plot with the voltage axis gives the magnitude of the heterojunction diffusion potential V_D, and from the slope S the gap state density in the amorphous material N_I can be determined as follows:

$$N_I = \left(\frac{2\varepsilon_0 \varepsilon_s}{S q N_A^2} - \frac{1}{N_A} \right)^{-1}, \qquad (1)$$

where N_A is the concentration of impurities in a crystalline semiconductor.

Fig. 1 shows the W_1^2 vs. V dependence at temperature 60 K and empty electron centres. It can be seen in the figure that the diffusion voltage for this heterojunction is 0.58 V. The density of silicon carbide gap states N_I, determined from the equation (1) at $N_A = 1.2\times10^{15}$ cm^{-3} [3] and ε_S = 11 [7], is 1.5×10^{15} cm^{-3}, or, per energy unit, 2.9×10^{17} cm^{-3}eV^{-1}.

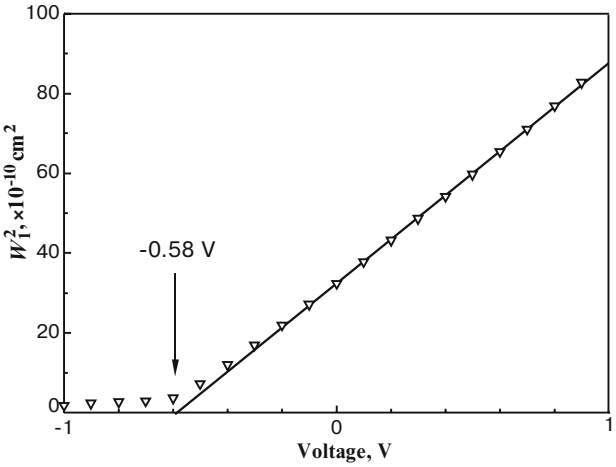

Fig. 1. Plot for determination of the bandgap state density in amorphous silicon carbide and of the diffusion voltage of the heterojunction.

3.2. Forward I-V characteristics

Fig. 2 shows the current-voltage characteristics of the structure measured at temperatures below 60 K. It can be seen that the heterojunction has distinct rectifying properties. It is worth noting that, at forward bias, the current onset takes place at some nonzero value of the negative gate voltage.

Fig. 3 shows, in the semi-logarithmic plot, current-voltage characteristics of the forward-biased heterostructure measured at 40 and 80 K with and without filling the electron system of centres in the SiC layer. Filling was performed by applying a 10 V bias at temperature 120 K. It can be seen in the figure that each curve consists of three sections with a substantially different character of the dependence of current on bias and temperature. In the

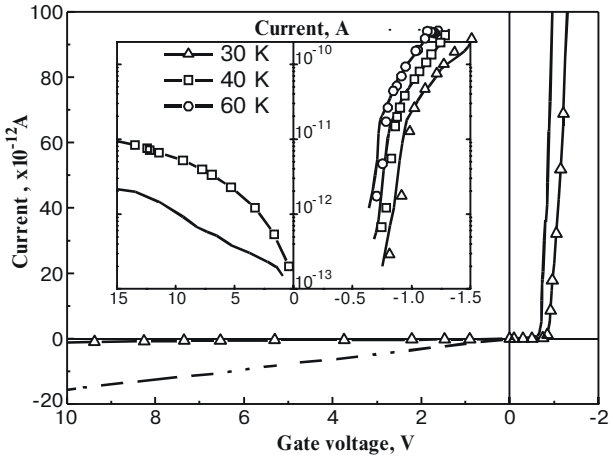

Fig. 2. Current-voltage characteristics of the SiC-Si heterojunction at different temperatures (semi-log plot is shown in the inset).

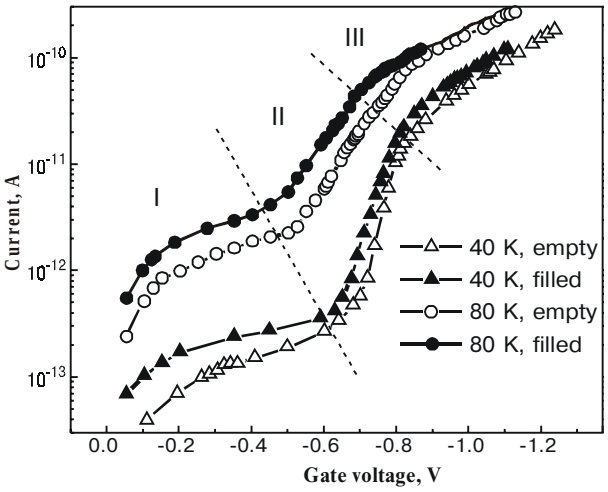

Fig. 3. Forward I–V characteristics at the temperatures 40 K (Δ) and 80 K (O) for empty (open symbols) and filled (full symbols) electron states.

low-voltage region the current rises rather slowly (section I), then the sharp increase of the current is observed (section II), and in the higher voltage region the section III with a lower slope of the log I vs. V dependence is registered. Such behaviour reflects the existence of different mechanisms of the transport current control as the forward bias increases.

Filling of the electron traps results in an increase of the current over the investigated voltage range. It was shown in [3] that application of a positive voltage to the gate at temperatures above 120 K leads to a capture of the electron charges in the electrically active centres in the silicon carbide layer. The fact that the forward current increases after filling the traps proves that the dominant component of the forward current is the hole current. In this case the negative charge of electrons trapped in the SiC layer lowers the potential barrier for the hole transport from the silicon substrate through the hetero-interface and the silicon carbide layer into the metal contact.

There exist a number of papers devoted to studies of transport current mechanisms in heterojunctions and, in particular, in the structures «amorphous semiconductor - single-crystalline semiconductor». The energy band diagram of the a-SiC/pSi heterojunction at temperatures close to room temperature is based on the classical Anderson approach for a sharp crystalline anisotype heterojunction and the basic transport mechanisms are the recombination current at temperatures below 250 K and tunnel-recombination current with involvement of interface states at higher temperatures [8]. The model of Perlman and Feight [9] is based on Schottky emission through the band discontinuity at the interface. Brodsky and Dohler [10] have shown that in the «amorphous-crystalline silicon» heterostructure the dominant transport mechanism in the amorphous Si film is the variable range hopping conductivity near the Fermi level (Mott's model). In papers by Hill the conduction of amorphous solids is described by the Poole-Frenkel model for thermal field-assisted emission of carriers from the Coulomb centers [11] or by the hopping conduction mechanism [12].

Fig. 4 shows energy band diagrams of the heterostructure under investigation, which help to illustrate the observed behaviour of the current-voltage characteristics. In Fig. 4(a) the classical Anderson energy band diagram is shown in thermal equilibrium and at zero gate bias. The sum of band bendings on both sides of the heterojunction is equal to the diffusion potential V_D.

If the absolute magnitude of the negative bias applied to the gate increases, the situations shown in the Figs 4(b-e) will eventually appear. At low forward bias the band diagram does not differ significantly from the conventional diagram for heterojunctions (see Fig. 4(b)). However, since doping of the wide-bandgap semiconductor is low, its resistivity is high at low temperatures, therefore an amorphous silicon carbide layer at temperatures below the liquid nitrogen temperatures can be considered as the dielectric with leakage. At a certain value of voltage $V=V_{FB}$ the negative voltage at the gate electrode compensates the built-in diffusion potential and the flat band conditions for the semiconductor are reached (Fig. 4(c)).

As the forward voltage is further increased, the voltage drop across the silicon side of the heterojunction remains unchanged, and the portion of the bias exceeding this value appears to be applied to the silicon carbide layer (Figs 4(c, d)). In this case the single-crystalline silicon plays a role of the source of charge carriers, and the current is determined mostly by transport processes through the heterointerface and in the amorphous material.

Thus, as the forward bias increases, different situations may occur in the investigated structure, so that different theoretical models developed for transport in anisotype heterojunctions, dielectrics with leakage, or amorphous semiconductors, should be drawn to explain the observed behaviour. It is seen in Fig. 4 that a characteristic point on the voltage axis separating the heterojunction model and the model of dielectric with leakage is the flat-band voltage V_{FB}.

3.2.1. Multi-step tunnelling in the bandgap localized states

The fact that the slope of logarithm of the current vs. voltage plot in the first section (see figure 3), i.e. at low forward biases, is practically independent of the temperature, can be considered as an evidence of the tunnelling mechanism of the transport current. As was shown in [7, 8, 13, 14], one of the most probable transport mechanism for anysotipe heterojunctions is the multi-step recombination-tunnelling process. According to this mechanism majority carriers for the narrow-bandgap semiconductor make subsequent trappings and emissions via the states in the bandgap of the wide-bandgap material. In the energy diagram (Fig. 4(b), arrows indicate schematically

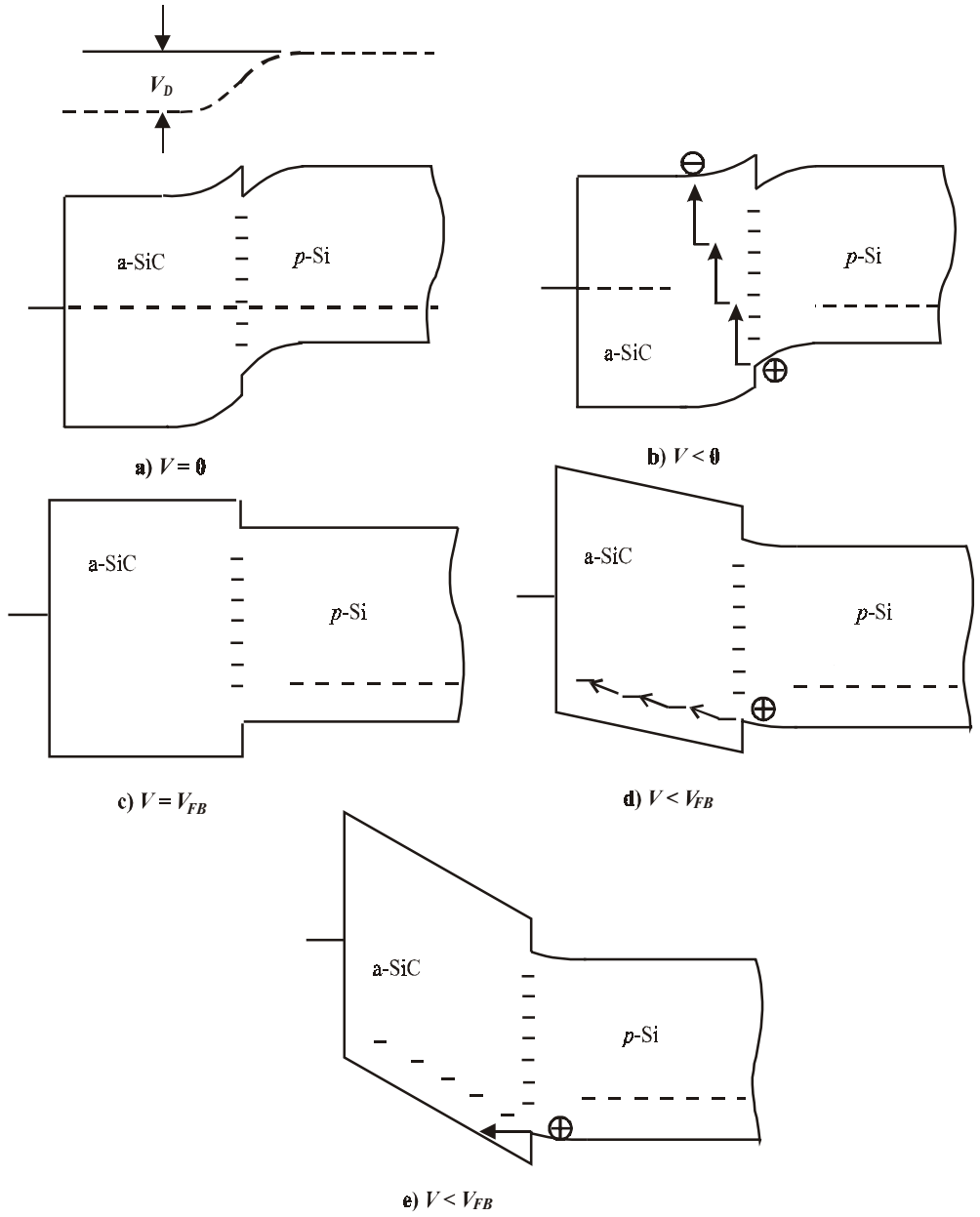

Fig. 4. Energy band diagrams of the structure at various conditions: thermal equilibrium, $V = 0$ (a); forward biased hetero-junction: $V > V_{FB}$ (b), $V = V_{FB}$ (c), $V < V_{FB}$ (d, e).

the charge carrier motion at such transport mechanism, when the hole passes the multi-step path in the silicon carbide space charge region until it is recombined with the electron. The current in this case is described by the relation:

$$J = J_0 \exp(V/V_0) \exp(T/T_0), \quad (2)$$

where V_0 and T_0 are independent of temperature and voltage parameters.

Fig. 5 shows the temperature dependencies of the current at low forward biases. One can notice that an exponential dependence of the current on temperature is really observed at voltages ranging from -0.1 to -0.3 V. The characteristic temperature T_0 lies in the range 13-16 K.

3.2.2. Tunneling of holes on localized states in the valence band tail

It can be seen in Fig. 3 that, as the value of the forward bias exceeds the flat-band voltage, V_{FB}, the current through the structure increases sharply, and its temperature dependence changes. Such an increase of the current is related to appearance of additional conduction channel associated with the transport of holes from crystal-

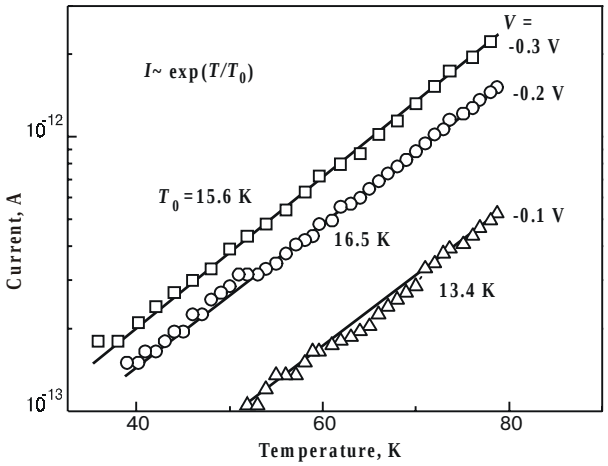

Fig. 5. Temperature dependencies of forward currents at small biases.

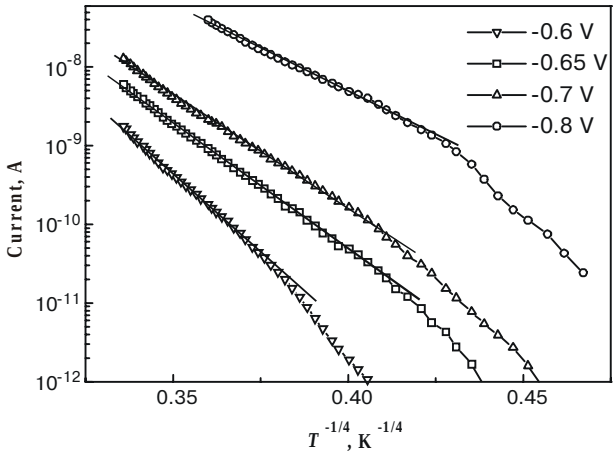

Fig. 6. Temperature dependencies of forward currents plotted in Mott's coordinates.

line silicon on states in the tail of the valence band of amorphous silicon carbide. At lower biases (p.3.2.1.) the current transport is mainly determined by the processes in space charge regions near the interface (see Fig. 4(b)). The current magnitude is very small in this case, because at multistep tunneling transport mechanism the transport processes are controlled by the presence of free electrons in the wide-bandgap intrinsic material, and at low temperatures the electron concentration is very small. Once the magnitude of applied voltage exceeds the flat-band voltage (see Figs 4(d, e)), the current through the structure is determined by the transport of holes in the amorphous silicon carbide layer.

Conduction of amorphous semiconductors was studied theoretically in [15], where three basic channels for conduction were distinguished: 1) extended state conduction above a mobility edge; 2) hopping conduction in localized states below a mobility edge; 3) hopping conduction in localized states at the Fermi level. In a review [16] hopping transport in ordered and disordered solid is studied, and it is shown that in amorphous intrinsic semiconductors conduction in localized states in the tails of conduction or valence bands may be realized. At low temperatures conductivity of amorphous semiconductors used to be described by the well-known Mott law for the variable range hopping transport and obeys the law [16]:

$$\sigma \propto \sigma_0 \times \exp[-(T_M/T)^{1/4}], \quad T_M = c_3^4 \alpha^3 / kN(\mu) \qquad (3)$$

where c_3 is a constant of order unity, α is the reciprocal of the Bohr radius of atomic wavefunction, $N(\mu)$ is the density of states at the Fermi level. The equation (3) is valid for the three-dimensional case, whereas in a general case [17] the critical exponent depends on dimensionality of space being equal to 1/3 for two- and 1/2 for the quasi-one-dimensional transport.

In Fig. 6 temperature dependencies of forward currents at biases exceeding V_{FB} are shown as a function of $T^{-1/4}$. It can be seen that conductivity obeys the $T^{-1/4}$ law, and the slope of the plot changes in dependence on the applied voltage. It follows from equation (3) that knowing the values of the constant c_3 and of the characteristic dimension of the wavefunction α^{-1} it is possible to determine the density of states at the level where hopping takes place, i.e. at the conduction level.

In Fig. 7 calculated values of density of localized states in the valence band tail of amorphous silicon carbide are shown in dependence on applied voltage. In calculation the values c_3=2 [16] and α^{-1} =1.5 nm [18] were used. The increase of the state density with increasing the forward bias reflects the displacement of the Fermi level to the edge of the valence band. Supposing that Fermi level position changes linearly with variation of the gate voltage, we can draw the conclusion from the Fig. 7, that the density of states in the tail of the valence band increases exponentially while approaching the edge of the bandgap. A good agreement of the obtained density of states values with the value calculated from the *C–V* measurements (see p.3.1) should be noted. For clarity this value is presented in the plot by solid square mark at the voltage V = - 0.58 V.

3.2.3. Tunneling through the potential barrier near the interface.

Consider the third part of the current-voltage characteristics. It can be seen in Fig. 3 that as some value of the forward bias is reached, the temperature dependence of the current becomes much weaker and the character of field dependence changes. The slope of *I–V* characteristic, in semi-log scale, is independent of temperature in this part of the curve. Therefore, we can suggest that the main mechanism controlling the transport current in this section is tunnelling.

Returning to the second section of *I-V* characteristic, within which the transport is determined by the Mott

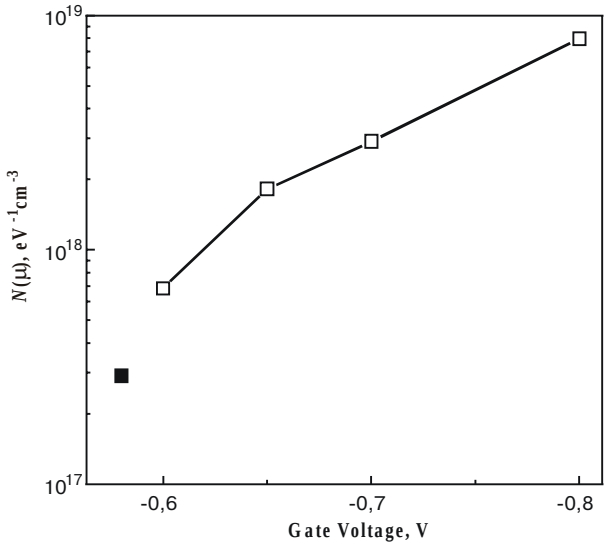

Fig. 7. Density of states in the valence band tail of amorphous silicon carbide in dependence on the voltage at the metal electrode.

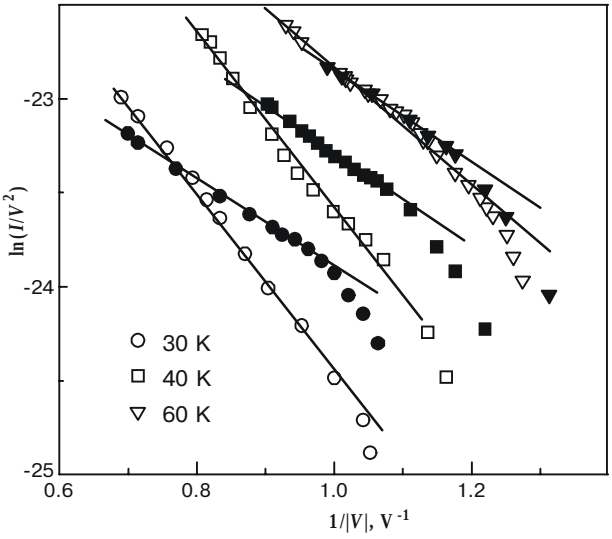

Fig. 8. Current-voltage dependences at high forward bias for filled (solid) and empty (open) centres.

mechanism, we should note that in this case holes enter the silicon carbide layer by resonant tunnelling from the silicon valence band to the level in the SiC bandgap near the top of the valence band. In Fig. 4(e) the situation is illustrated occurring during the increase of negative voltage at the metal electrode when the field in the amorphous semiconductor increases. In this case the probability of direct tunneling into the valence band of silicon carbide across the triangular barrier increases. This type of tunnelling process is known as Fowler-Nordheim tunnelling and the current in this case is described by the following equation [19]:

$$J \propto E^2 \exp\left(\frac{-4\sqrt{2m^*}(q\varphi_B)^{3/2}}{3q\hbar E}\right) \qquad (4)$$

Here, φ_B is the potential barrier height.

As is seen from the equation (4), Fowler-Nordheim tunnelling occurs if the plot of dependence of logarithm I/V^2 vs. $1/V$ is a straight line. In Fig. 8 current-voltage characteristics are shown plotted in $\ln(I/V^2)$ vs. $1/V$ coordinates for the third part of I-V characteristics at empty and filled electron centres. It can be seen in the figure that transport here can be described in frames of the Fowler-Nordheim tunnelling model. The temperature dependence of the current is related with the increase of free charge carrier concentration in crystalline silicon with increasing temperature.

Filling of electron centres in the silicon carbide layer results in the increase of electrical field strength near the interface, since the field induced by distributed electron charge is added to the external field. Because of this, the slope of the plots is different for cases of filled and empty electron centres.

It should be mentioned that at temperatures above 60 K the dependencies for empty and filled states coincide. At such temperatures and fields the electrons trapped in the SiC layer are released into the conduction band and are swept into the silicon substrate since a sufficiently large forward bias reduces the effective barrier for their release. As a result, the structure turns to its initial condition with empty electron states.

3.3. Reverse I-T characteristics

If a reverse bias is applied to the structure ($V_g > 0$), then, at low temperature, in the p-type silicon substrate the non-equilibrium depletion is formed and the major part of the applied voltage drops at the silicon substrate.

Measurements of reverse currents have shown that if the electron centres are initially empty, the magnitude of the current varies during the measurement, that is, at a constant temperature and reverse bias the current slowly (with a characteristic time of about several minutes) decreases approaching to some steady-state value. If trap filling is performed before the measurement, the change in the current is not observed. This effect was attributed to the fact that the negative charge of electron centres in silicon carbide creates a barrier for carrier transport and causes the reduction of the current. This reduction of current proves that the reverse current is the current of electrons from the silicon substrate to the silicon carbide layer and further to the metal electrode.

In order to clarify the effect of filling the electron traps on the magnitude of the reverse current two sets of measurements have been carried out. In the first set reverse currents were measured in dependence on temperature at different values of reverse bias, and after each measuring

cycle (during heating from 20 to 80 K) the sample was heated up to 160 K in shortened state. Such heating resulted in emptying the electron traps in the SiC layer. In the second set of measurements such a heating was not performed, the structure was cooled with the reverse bias applied, then, at low temperature, the new value of the bias was applied, and the following measuring cycle was done. The electron states may be conditionally considered as empty in the first set and as filled in the second set.

Fig. 9 shows the temperature dependencies of the reverse currents of the heterojunction measured at different reverse biases for empty traps. It is seen that the reverse currents can be described by the same relation (2) as the forward currents at low voltages (see Fig. 5). The characteristic temperature T_0 is practically the same as that obtained for the forward currents.

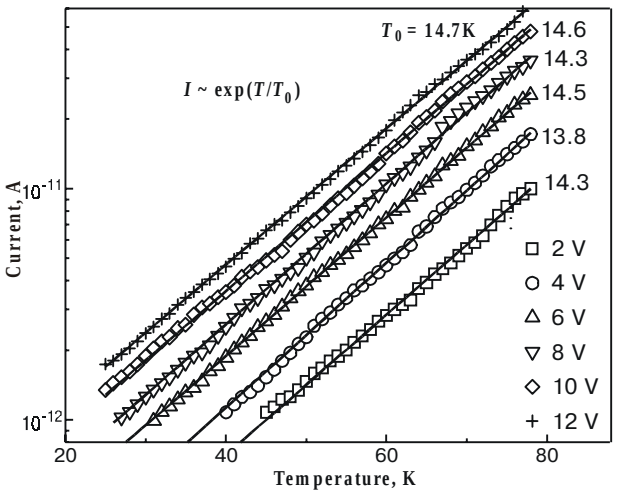

Fig. 9. Temperature dependences of the reverse current at different bias.

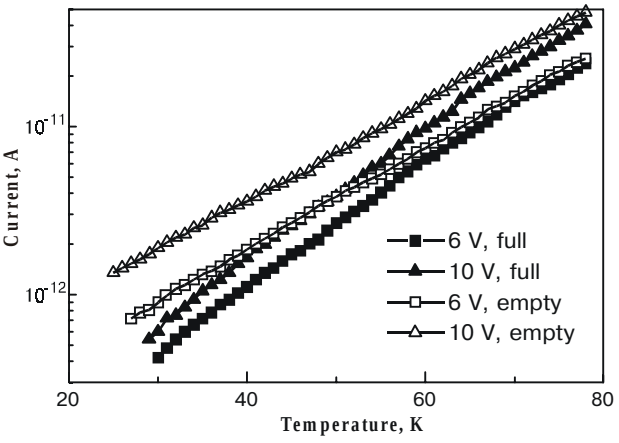

Fig. 10. Temperature dependences of the reverse current for filled (solid) and empty (open) electron centres.

Fig. 10 shows, for comparison, the temperature dependencies of reverse currents at empty and filled electron centres. It can be seen in the figure that filling results in a substantial reduction of the reverse current. It agrees with our assumption that the electrons trapped at the centres create an additional barrier for the electron current in the SiC layer.

Conclusions

From the study of the forward and reverse currents in the *a*-SiC/*p*-Si heterojunction in the temperature range from 30 to 80 K it was found that transport current mechanisms in this structure are different at different voltages at the metal electrode. At a reverse bias and a low (less than 0.3 V) forward bias the transport is determined by the process of multi-step tunnelling of electrons and holes, respectively, via states in the bandgap of amorphous silicon carbide. The transport current in the heterojunction at forward biases in the range 0.55-0.8 V is controlled by hopping of holes in the amorphous material according to Mott's mechanism. At higher voltages the dominant mechanism controlling the current becomes the hole tunneling across the triangular barrier in the amorphous-crystalline semiconductor interface.

Filling the system of electron traps situated in the silicon carbide layer causes the reduction of the potential barrier for holes and, as a result, leads to the increase of the forward current. The reverse current of electrons in this case decreases.

References

1. J. B. Casady, R. W. Johnson, Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review // *Solid State Electronics* **39**, pp. 1409-1422 (1996).
2. D. Kurangam, T. Endo, M. Deguchi, W. Guang-Pu, H. Okamoto and Y. Hamakawa, Amorphous silicon carbide thin film emitting diode // *Optoelectronics* **1**, pp. 67–84 (1986).
3. V. S. Lysenko, I. P. Tyagulski, Y. V. Gomeniuk, I. N. Osiyuk and I. I. Tkach, Thermally stimulated characterization of shallow traps in the SiC/Si heterojunction // *Journ. of Phys. D: Applied Physics* **31**, pp. 1499–1503 (1998).
4. H. Chaabane, J. C. Bourgoin, Irradiation effect on electron transport through GaAlAs barriers // *Applied Phys. Letters* **64**(8), pp. 1006–1008 (1994).
5. H. Chaabane, J. C. Bourgoin, Role of defects on electron transport through semiconductor barriers // *J. Appl. Phys.* **76**(1), pp. 315–318 (1994).
6. H. Matsuura, T. Okuno, H. Okushi, K. Tanaka, Electrical properties of *n*-amorphous/*p*-crystalline silicon heterojunctions // *J. Appl. Phys.* **55**(4), pp. 1012-1019 (1983).
7. I. Magafas, N. Georgoulas, A. Thanailakis, Electrical properties of a-SiC/c-Si(p) heterojunctions // *Semicond. Sci. Technol.* **7**, pp. 1363-1368 (1992).
8. J. R. Donnelly, A. G. Milnes, Current/voltage characteristics of p-n Ge-Si and Ge-GaAs heterojunctions // *Proc. IEE*, **113** (9), pp. 1468-1476 (1966).
9. S. S. Perlman, D. L. Feught, P-N heterojunctions // *Solid State Electronics* **7**(12), pp. 911-923 (1964).
10. M. H. Brodsky, G. H. Dohler, P. J. Steinhardt, On the measurement of the conductivity density of states of evaporated

amorphous silicon films // *Physica Status Solidi (b)* **72**, pp. 761-770 (1975).
11. R. M. Hill, Poole-Frenkel conduction in amorphous solids // *Philosophical Magazine* **23**, pp. 59-86 (1971).
12. R. M. Hill, Hopping conduction in amorphous solids // *Philosophical Magazine* **24**, pp. 1307-1325 (1971).
13. A. R. Riben, D. L. Feught, Electrical transport in *n*Ge-*p*GaAs heterojunctions // *Int. J. Electronics* **20**(6), pp. 583-599 (1966).
14. B. L. Sharma and R. K. Purohit, *Semiconductor Heterojunctions*, Oxford: Pergamon 1974.
15. A. J. Grant, E. A. Davis, Hopping conduction in amorphous semiconductors // *Solid State Comm*. **15**, pp. 563-566 (1974).
16. H.Bottger, V.V.Bryksin, Hopping conductivity in ordered and disordered solids (I) // *Physica Status Solidi* (*b*) **78**(1), pp. 9-56 (1976).
17. D. Redfield, Transport properties of electrons in band tails // *Advances in Physics* **24**, pp. 463-487 (1975).
18. N.F.Mott, E.A.Davis, *Electron Processes in Non-Crystalline Materials*, 2nd Ed., Clarendon Press: Oxford, 1979.
19. S. M. Sze, Physics of Semiconductor Devices, 2nd Ed., Wiley: New York 1981.