Characterization of hole traps in reverse-biased Schottky-type p-GaN gate HEMTs by current-transient method

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ABSTRACT

In this study, the current-transient method has been conducted to investigate the trap states in p-GaN gate high-electron-mobility transistors (HEMTs) under reverse gate stress. An irregular threshold voltage shift under reverse gate bias has been observed through the pulsed transfer measurements with different delay times. It suggests that both the hole insufficiency and hole trapping are generated during the reverse gate pulse bias. With proper selection of the delay time based on the pulsed characterizations, the hole detrapping can be effectively evaluated after the hole recovery is completed. In addition, by subtracting the trapping behavior caused by the measurement condition, the actual detrapping transient under reverse gate filling voltages can be obtained with the current-transient method. Three traps have been observed with the energy levels of 0.484, 0.390, and 0.235 eV. The identification of hole traps may provide a basis on the understanding of threshold voltage instability and further improvement of the reliability of p-GaN gate HEMTs.

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Normally off high-electron-mobility transistors (HEMTs) have recently demonstrated to be excellent devices for the power electronics applications owing to the low on-resistance,[1] simplified gate control scheme,[2] and fail-safe operation.[3] In particular, the Schottky type p-GaN gate HEMTs are commercially available because of the low switching loss[4] and reduced gate leakage current.[5,6] However, the p-GaN gate HEMTs still suffer from critical gate reliability concerns in practical operations,[4] and the gate bias induced threshold voltage (V_{TH}) instability requires further investigation.[7,8]

In recent years, a large number of studies have been dedicated to the understanding of the V_{TH} instability of p-GaN gate HEMTs.[3,5,9] The positive V_{TH} shift is usually ascribed to the electron trapping[1] or charge storage model,[3] while the negative shift is usually attributed to the hole accumulation[4] or hole trapping.[8] In addition, the V_{TH} shift may be related to the design and process of devices, which would result in the discrepancies between different reports.[10,11] Therefore, to distinguish and clarify the effect of different carrier behaviors on the V_{TH} shift is of great significance to the improvement of the device dynamic performance.[2]

Specifically, there are relatively few studies focused on the impact of reverse gate bias on V_{TH} shift. For the p-GaN gate HEMTs, the reverse gate voltage is often employed to avoid the false turn-on of the devices considering the relatively low V_{TH}[12,13] and, thus, more efforts should be devoted to the study of reverse gate bias induced V_{TH} shift. Wang *et al.* recently observed the positive V_{TH} shift under reverse gate stress, which was ascribed to the reduced positive charges in p-GaN layer.[12] Yang *et al.*, however, reported that the hole trapping occurred in the p-GaN layer apart from the hole insufficiency during the reverse gate pulse.[2] Nevertheless, the V_{TH} shift affected by different carrier behaviors under reverse gate stress has not directly been presented. Therefore, further study on the V_{TH} shift is necessary for understanding hole insufficiency and hole trapping mechanisms under reverse gate stress, which makes the identification of hole traps in p-GaN gate HEMTs important.

In this study, we investigated the reverse gate bias induced V_{TH} shift in the p-GaN gate HEMT through the pulsed transfer characterizations. The non-monotonic V_{TH} shift was observed after removing the reverse gate pulse with different delay time, from which the effect of hole recovery and hole detrapping behaviors can be discussed clearly. Three traps were identified based on the detrapping transients with the current-transient method, and the possible origins of the hole traps were also analyzed. It offers a distinct approach for the identification of

hole traps, which can be meaningful in further improvement of the gate reliability of the p-GaN gate HEMTs.

The device used in this study is a commercial 100 V/6 A p-GaN gate HEMT.[14] The pulsed transfer characterizations under reverse gate stress were performed using a Keysight B1505A power device analyzer along with a N1265A fast switch. As depicted in Fig. 1(a), the pulsed transfer measurements were employed to present the V_{TH} shift under reverse gate stress,[3,9] with the delay time (t_d) ranging from 0 to 30 ms after switching to a forward gate bias.[2] The stress time was set as 1 s and the measurement time was 10 ms, assuring that the self-heating effect could be adequately eliminated.[12] The threshold voltages of the device were extracted at a criterion of drain–source current (I_{DS}) of 1 mA, and the above-mentioned measurements were performed on three samples to verify the shift in V_{TH}. In addition, the device was kept in the unstressed situation for 10 min to confirm the full recovery of V_{TH} before the next measurement.[1]

Through the pulsed transfer characterizations with different delay times, a non-monotonic V_{TH} shift was observed with the gate–source quiescent voltage (V_{GSQ}) ranging from 0 to −4 V in Fig. 1(d), of which the V_{TH} shift with different delay time can be classified as the following types:

(i) a positive V_{TH} shift with $t_d = 0$ ms shown in Fig. 1(b);
(ii) an irregular V_{TH} shift within $t_d = 10$ ms; and
(iii) a negative V_{TH} shift with the delay time larger than 10 ms, and the pulsed transfer curves with $t_d = 30$ ms were shown in Fig. 1(c).

To demonstrate the mechanisms of the above-mentioned non-monotonic V_{TH} shift, the schematic and band diagrams of the gate stack were presented in Fig. 2. For the p-GaN gate HEMTs, the gate stack can be modeled as back-to-back series-connected metal/p-GaN

Schottky diode (J_s) along with the p-GaN/AlGaN/GaN diode (J_p),[2,8] and the equivalent circuit was presented in Fig. 2(a). With a reverse gate bias, the Schottky diode was forward biased and the holes flowed out toward the gate metal.[35] Among them, part of the holes may be emitted to the gate metal in Fig. 2(b),[12] and part of the holes may be trapped in the SCR in Fig. 2(c).[2] After switching to a forward gate bias, the hole recovery and hole detrapping behaviors were presented in Figs. 2(d) and 2(e), which corresponded to the hole insufficiency and hole trapping with a reverse gate bias, respectively. More details about the hole insufficiency and hole trapping with a reverse gate stress can be found in Refs. 2 and 12.

Based on the above-mentioned analysis, the hole insufficiency and hole trapping under reverse gate stress can result in the reduced positive and negative charges, respectively. Therefore, the V_{TH} shift was affected by the weight of the above-mentioned carrier behaviors. Specifically, it has been reported that the hole detrapping behavior was generated after hole recovery under the forward gate bias,[2] and, thus, the non-monotonic V_{TH} shift in Fig. 2(d) can be related to the different delay time after the switching event. For the pulsed measurements (i) without delay time, the effect of hole insufficiency dominated first and the reduced positive charges may not be restored instantly,[12] which resulted in the positive V_{TH} shift in Fig. 1(b). With increasing delay time after switching, the effect of hole trapping gradually became more significant and lead to the excessive positive charges. Therefore, the V_{TH} shift (ii) within the first 10 ms became irregular, and then the negative V_{TH} shift (iii) with the delay time larger than 10 ms can be observed. The above-mentioned results were also consistent with the analysis of hole detrapping generated after hole recovery with the change encountered at ∼10 ms in Ref. 2.

To further illustrate the hole trapping under reverse gate stress, the detrapping behavior was identified using the current-transient
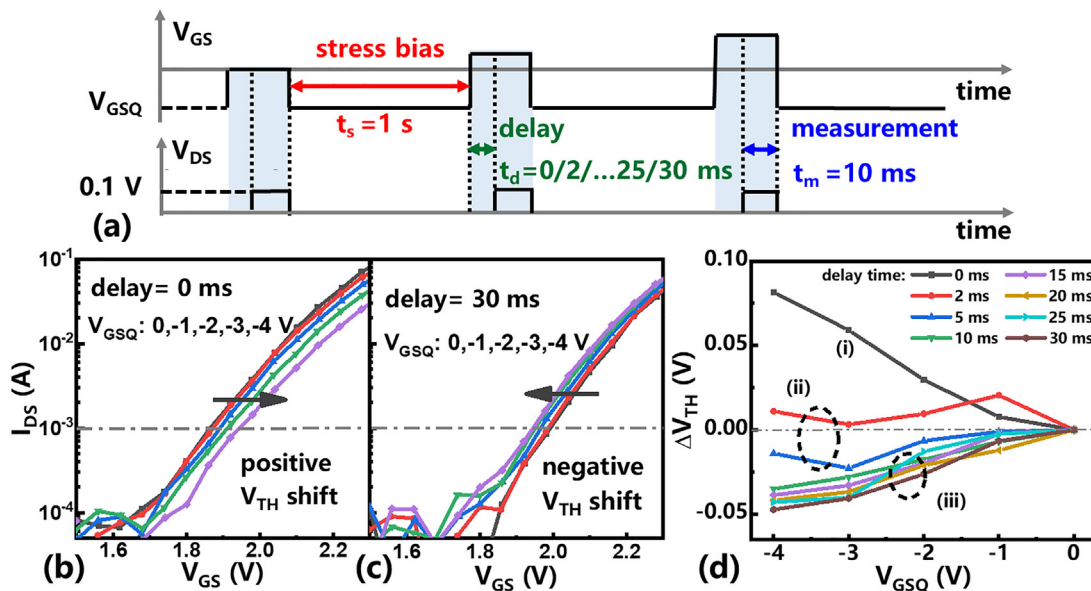

FIG. 1. (a) Sequence for the pulsed transfer characterizations with different delay times (t_d) after removing the reverse gate bias voltage. The stress and measurement time were 1 s and 100 ms, respectively. (b) The positive V_{TH} shift with $t_d = 0$ ms. (c) The negative V_{TH} shift with $t_d = 30$ ms. (d) The comparison of the V_{TH} shift with the t_d ranging from 0 to 30 ms.
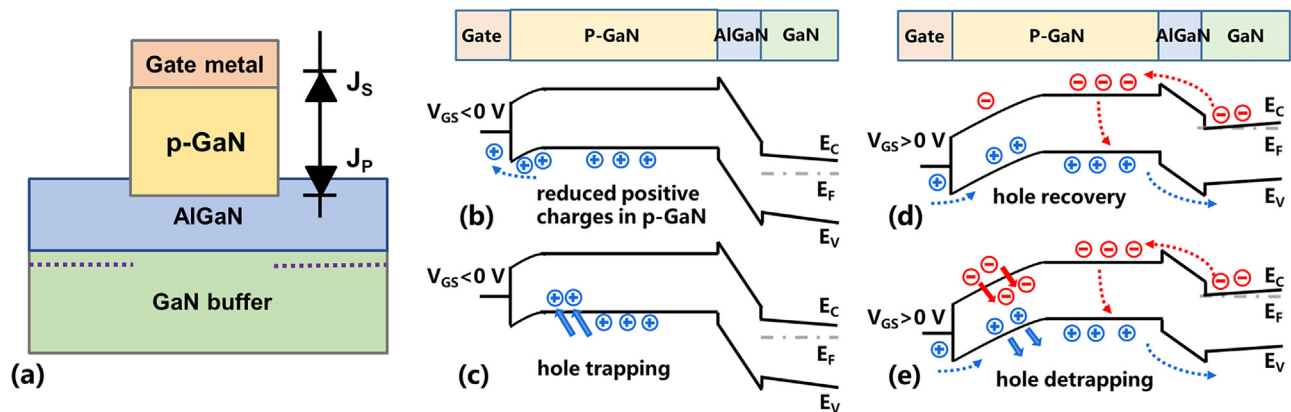
FIG. 2. (a) The schematic diagram of the gate metal/p-GaN/AlGaN/GaN gate stack. The band diagrams of the gate stack with (b) the hole insufficiency and (c) hole trapping under a reverse gate bias stress. The band diagrams in transient measurement dominated by (d) the hole recovery and (e) hole detrapping at a forward gate bias.

method, and the measurement sequence was presented in Fig. 3(a). The detrapping transient was obtained with the measurement conditions of $(V_{GS}; V_{DS}) = (2\,V; 0.1\,V)$ for 500 s, after a certain gate filling voltage applied on the device for 1 s. According to the results in Fig. 1(c), the effect of hole recovery can be avoided completely with delay time larger than 30 ms after the switching event, and, thus, the detrapping transient curves were obtained after switching to the measurement conditions with $t_d = 30$ ms. In addition, the measurement voltages applied during the detrapping process can lead to the additional trapping behavior,[15] which was included in the measured detrapping curves. To obtain the effect of this trapping behavior, the same voltages were applied on the device before the filling process, and the trapping transient was also monitored with $t_d = 30$ ms. To ensure that the device recovered to the initial condition before the filling process, the reverse gate stress was applied after 10 min rest time to obtain the detrapping transients.[10]

Figure 3(b) presented the measured detrapping curve (brown) with gate filling voltage (V_{GF}) of -3 V, and the trapping curve with the same measurement voltages (orange), of which the current variation

(ΔI_{DS}) was presented with respect to the steady state current value at the end of the transient.[16] Under the above-mentioned measurement conditions, the electrons injected from the two-dimensional electron gas (2DEG) may be captured by the traps in the p-GaN or at the p-GaN/AlGaN interface,[4,12] resulting in the decrease in the current (orange) in Fig. 3(b). Therefore, the actual detrapping curve (red) was obtained by subtracting the undetected part from the measured curve,[15] which presented a regular decreasing trend. It can be noticed that the release of holes can result in the decrease in I_{DS},[17] and, thus, the decreasing trend of the actual detrapping curve was consistent with the analysis of hole detrapping in Fig. 2(e). In addition, the above-mentioned results also verified the negative V_{TH} shift in Fig. 1(c), which can be attributed to the hole detrapping generated after hole recovery with $t_d = 30$ ms.

With this method, the actual hole detrapping under different V_{GF} was obtained in Fig. 4(a). As the detrapping transients may involve several independent detrapping processes and can be regarded as a sum of exponentials,[18,19] the measured transient curve I_{ds} (t) can be expressed as[20,21]
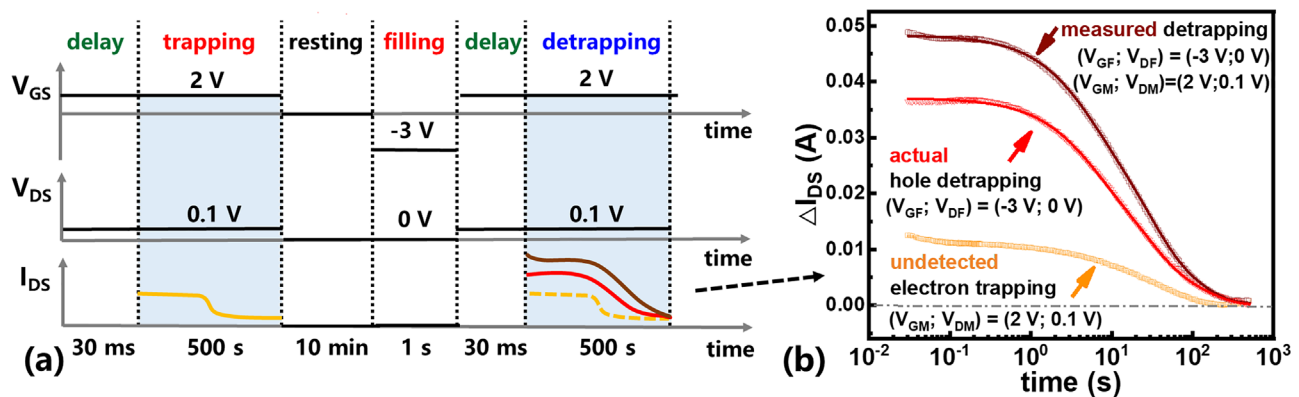

FIG. 3. (a) The sequence for the detrapping transient curves with the current-transient method. The effect of hole recovery generated within 30 ms after the switching event is excluded by the delay process, and the effect of trapping behavior caused by the measurement conditions is obtained with the trapping process. (b) The comparison of the measured (brown) and actual (red) detrapping curves with the filling voltages of $(V_{GF}; V_{DF}) = (-3\,V; 0\,V)$ and measurement conditions of $(V_{GM}; V_{DM}) = (2\,V; 0.1\,V)$. The current variation (ΔI_{DS}) is presented with respect to the steady state current value at the end of the transient.
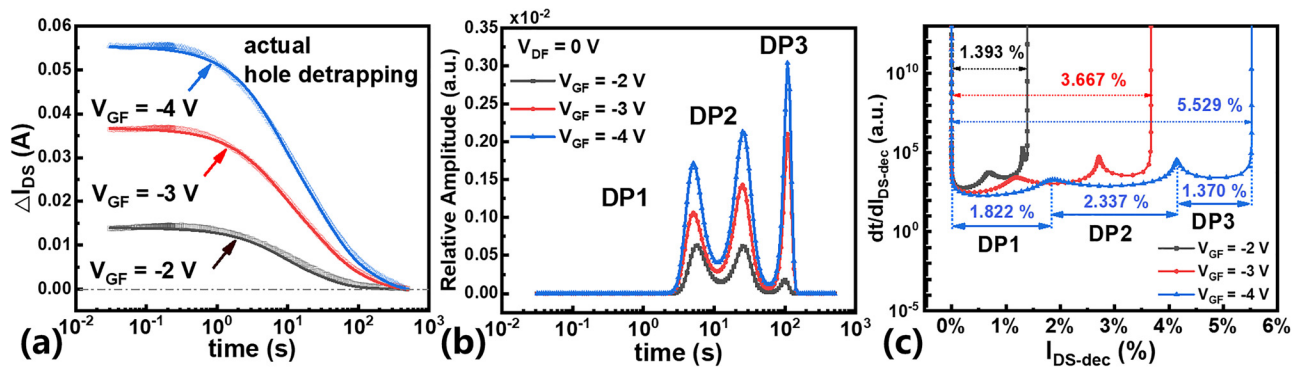
FIG. 4. (a) The actual detrapping transients at different gate filling voltages. The experimental data (dots) and reconstructed curves (lines) are agreed well with each other. (b) Time constant spectra based on the Bayesian deconvolution method. Three detrapping behaviors were identified and designated as DP1, DP2, and DP3. (c) Differential amplitude spectra.

$$I_{ds}(t) = \sum \Delta I_i \exp\left(-\frac{t}{\tau_i}\right) + I_\infty, \qquad (1)$$

where ΔI_i is the amplitude, τ_i is the time constant of trap, and I_∞ is the current at a steady state. Therefore, the time constant of traps can be obtained based on the Bayesian deconvolution method.[20] This method was also used to extract the trap time constant in the depletion GaN HEMTs,[18] which can perform well in avoiding the small ripples and distinguishing the close peaks in the time constant spectra (TCS).

As shown in Fig. 4(b), three traps were identified with the detrapping transients and designated as DP1, DP2, and DP3, which corresponded to the hole trap states with a reverse gate filling bias.[2,17] The time constants of three traps can be extracted from the values of x-axis in correspondence to the peaks and were unchanged with different V_{GF}. It suggested that the time constants of three traps were long, indicating that the release of holes may take longer time due to the low hole mobility.[5] Moreover, the transient curves in Fig. 4(a) were reconstructed from the TCS and agreed well with the experimental data (dots), indicating that the extracted time constants with the Bayesian deconvolution method were accurate.

In addition, it can be observed that the height of peaks increased with larger V_{GF} in the TCS in Fig. 4(b), suggesting that the relative

amplitudes of traps increased correspondingly. However, the peak distribution was not taken into consideration and thus the accurate amplitudes should be illustrated with the differential amplitude spectra (DAS) in Fig. 4(c), which was obtained with a differential calculation based on the sum of the relative amplitudes of traps in the TCS in Fig. 4(b).[18] It suggested that the total variation of I_{DS} at $V_{GF} = -2, -3,$ and -4 V were 1.393%, 3.667%, and 5.529%, respectively. The above-mentioned results were consistent with the ΔI_{DS} at the corresponding V_{GF} in Fig. 4(a). In addition, the exact amplitude of each trap can also be directly extracted from the difference in abscissa between the peaks in Fig. 4(c),[18] which included the information of the linewidth of the peak and corresponded to the contribution of each trap to the total variation of I_{DS}.[21] Moreover, it can be noticed that the accurate amplitudes of hole traps became larger with increasing V_{GF}, suggesting that the positive charges in p-GaN layer increased correspondingly due to the enhanced hole trapping under higher electric field. This result was also consistent with the larger V_{TH} shift with $t_d = 30$ ms in Fig. 1(c), which can be ascribed to the reduced negative charges in the SCR under higher reverse gate stress.

To obtain the energy levels of the above hole traps, the actual detrapping transients with $V_{GF} = -2$ V in the 303–343 K temperature range were presented in Fig. 5(a), which was also obtained with the
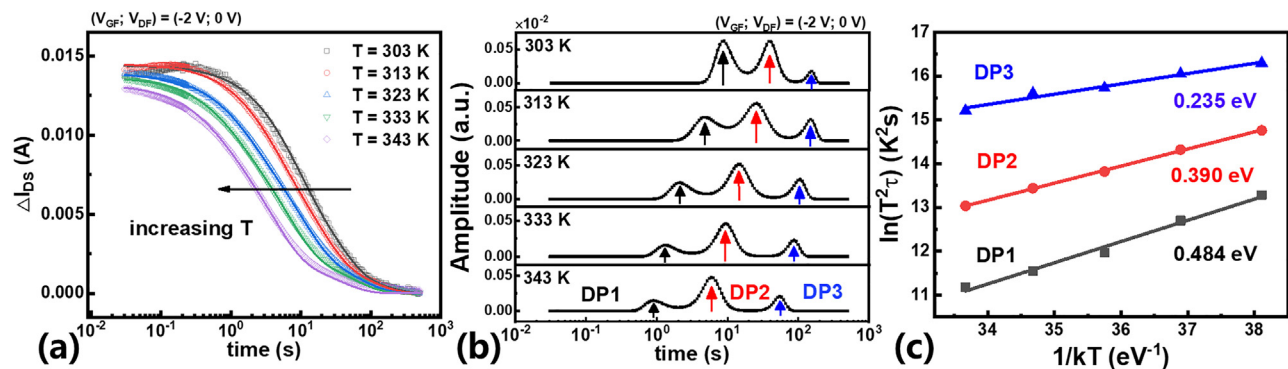

FIG. 5. (a) The actual detrapping transient curves with temperatures ranging from 303 to 343 K. The reconstructed curves (lines) agreed well with the experimental data (dots) at each temperature. (b) The time constant spectra at different temperatures with the gate filling voltage of -2 V. (c) The Arrhenius plots and the corresponding energy levels of the observed traps.

same sequence in Fig. 3(a). Moreover, the time constants of three traps at each temperature were presented in the TCSs in Fig. 5(b). Based on the TCSs, the Arrhenius plots of three traps can be depicted in Fig. 5(c). As the energy levels (E_A) and capture cross sections (σ) of traps can be directly identified with the linear fit of the points,[16] the detrapping transients only need to be monitored under several temperatures, which makes it easy to perform.

Specifically, DP1 was identified with energy level of 0.484 eV and capture cross section of 2.8×10^{-18} cm^2. The hole traps with E_A of 0.48–0.49 eV and σ of 10^{-17}–10^{-19} cm^2 have been observed in p-GaN HEMT[2,22] and p-GaN Schottky diodes,[23] which can be related to the transition level for nitrogen-vacancy or related complexes.[24,25]

DP2 was characterized with an energy level of 0.390 eV and capture cross section of 1.7×10^{-20} cm^2. The hole trap with E_A of 0.35 eV and σ of 1×10^{-21} cm^2 has also been reported in GaN layer.[26] It suggested that the hole traps with energy level close to 0.4 eV may be ascribed to the defect centers giving rise to the blue luminescence in p-GaN,[27,28] which has also been detected by DLTS[29] and admittance spectra.[30]

In addition, the energy level and capture cross section of DP3 were estimated to be 0.235 eV and 1.4×10^{-23} cm^2, respectively. The hole traps with the similar E_A may be associated with the Mg-related acceptors in previous studies,[17,31,32] and the hole traps with the cross sections of 10^{-20}–10^{-23} cm^2 have also been reported in GaN,[26,33,34] which deserves further works.

In this work, the hole insufficiency and trapping behavior in the p-GaN gate HEMT were discussed to analyze the V_{TH} shift under reverse gate stress. The pulsed transfer measurements were conducted after removing the reverse gate pulse with different delay times, and a non-monotonic V_{TH} shift was observed. A delay time of ~30 ms was identified to complete the hole recovery process thoroughly. The hole detrapping behavior generated after the hole recovery was obtained using the current-transient method. Three traps were identified based on the Bayesian deconvolution method and the possible origin of traps was analyzed with the obtained energy levels. The results can be useful for further understanding of the V_{TH} instability in the p-GaN gate HEMTs.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Shijie Pan: Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Shiwei Feng:** Methodology (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Xuan Li:** Formal analysis (equal); Investigation (equal); Resources (equal). **Kun Bai:** Software (equal); Visualization (supporting). **Xiaozhuang Lu:** Methodology (supporting); Resources (supporting). **Yanjie Li:** Data curation (supporting); Resources (supporting). **Yamin Zhang:** Methodology (supporting); Writing – review & editing (supporting). **Lixing Zhou:** Writing – review & editing (supporting). **Meng Zhang:** Investigation (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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