Electrical characterization of the temperature dependence in CdTe/CdS heterojunctions deposited *in-situ* by pulsed laser deposition

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(Received 9 October 2017; accepted 14 February 2018; published online 28 February 2018)

The I-V and C-V characteristics of CdTe/CdS heterojunctions deposited *in-situ* by Pulsed Laser Deposition (PLD) were evaluated. *In-situ* deposition enables the study of the CdTe/CdS interface by avoiding potential impurities at the surface and interface as a consequence of exposure to air. The I-V and C-V characteristics of the resulting junctions were obtained at different temperatures, ranging from room temperature to 150 °C, where the saturation current (from 10^{-8} to 10^{-4} A/cm^2), ideality factor (between 1 and 2), series resistance (from 10^2 to 10^5 Ω), built-in potential (0.66–0.7 V), rectification factor ($\sim 10^6$), and carrier concentration ($\sim 10^{16}$ cm^{-3}) were obtained. The current–voltage temperature dependence study indicates that thermionic emission is the main transport mechanism at the CdTe/CdS interface. This study also demonstrated that the built-in potential (V_{bi}) calculated using a thermionic emission model is more accurate than that calculated using C-V extrapolation since C-V plots showed a V_{bi} shift as a function of frequency. Although CdTe/CdS is widely used for photovoltaic applications, the parameters evaluated in this work indicate that CdTe/CdS heterojunctions could be used as rectifying diodes and junction field effect transistors (JFETs). JFETs require a low PN diode saturation current, as demonstrated for the CdTe/CdS junction studied here. *Published by AIP Publishing*. https://doi.org/10.1063/1.5008753

Cadmium telluride (CdTe) films have been widely studied as absorption layers for photovoltaic applications. Some of the advantages of CdTe films for these applications include a proper bandgap and a high absorption coefficient, which have been reported to be around 1.45 eV and 10^5 cm^{-1}, respectively.[1,2] Similarly, cadmium sulfide (CdS) films are usually reported as the window layer of choice for CdTe-based solar cells due to their adequate optical properties, which include their large bandgap (~2.4 eV)[3] and low absorption coefficient,[4] which allows most of the photons going across the CdS layer to reach the CdTe absorbing layer. In fact, heterojunctions based on CdTe/CdS have produced solar cells with efficiency as high as 20%.[5–7]

Additional advantages for both materials include deposition methods compatible with large area and low cost fabrication.[3,4,8–10] CdTe and CdS can be deposited by several methods, including solution methods,[11,12] thermal evaporation or sublimation,[13–15] metal-organic chemical vapor deposition (MOCVD),[16] close-spaced sublimation (CSS),[17,18] RF magnetron sputtering,[19,20] and pulsed laser deposition (PLD),[21–23] among others. The main advantage of films deposited by PLD is that the stoichiometry of the target is transferred directly to the substrate. In addition, substrate temperature, deposition pressure, target-substrate distance, and laser energy density are some other variables that can be used to tune the properties of the deposited film.[22,24,25] Another advantage of PLD is that it allows CdTe and CdS deposition *in-situ*, avoiding the exposure of the CdTe/CdS interface to the ambient, while many of the CdTe/CdS heterojunction devices reported use different deposition methods for CdTe and CdS.

Most CdTe/CdS heterojunction studies are focused on its application for solar cells and typically focus on parameters related to PV applications evaluated at room temperature, such as PV efficiency, fill factor, built-in potential, short circuit current, open circuit voltage, and optical properties, among others.[5,9,10] However, temperature analysis for diodes is extremely important to extract important diode parameters, such as transport mechanisms and built-in potential.[26,27]

Critical evaluation of CdTe/CdS structures could enable new applications for CdTe/CdS based devices. For instance, rectifier diodes and junction field-effect transistors (JFETs) could be fabricated with these materials if the transport mechanisms are properly understood. JFETs are devices where the channel is pinched-off by the depletion region in a PN junction. Therefore, understanding PN diode behavior is a key to investigate CdTe/CdS for potential JFET implementation.

In this work, the CdTe and CdS films were deposited *in-situ* using pulsed laser deposition (PLD). Since the PLD method allows for the introduction of multiple targets in the chamber, depositing different layers while avoiding the exposure of interface to air is possible. *In-situ* deposition minimizes the exposure of the interface to potential contaminants and potential oxidation after the first layer deposition but prior to deposition of the second layer. These contaminants can degrade the quality of PN interfaces, reducing the diode performance. The initial evaluation is shown in Fig. 1. The inset in Fig. 1 shows the I-V curves for CdTe/CdS diodes deposited *in-situ* and diodes where CdTe was deposited after exposing the CdS layer to the ambient (*ex-situ* deposition). The inset shows similar values of reverse and forward bias currents; however, different curve shapes for both methods are evident. Figure 1 shows the ideality factor calculated from the I-V curves shown in the inset. Figure 1 demonstrates that the behavior of samples deposited *in-situ*

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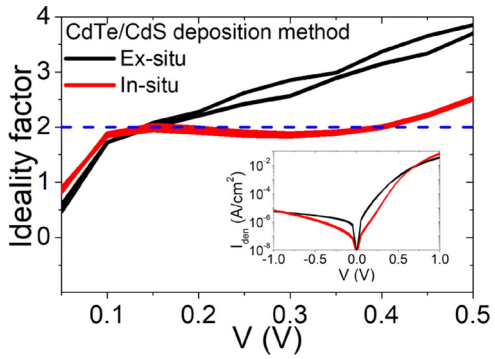

FIG. 1. Ideality factor for CdTe and CdS deposited *in-situ* and *ex-situ* for heterojunction fabrication. The sample deposited *in-situ* showed a flat region with a value of 2 from 0.1 V to 0.4 V. The sample deposited *ex-situ* showed a poorer ideality factor behavior compared to the sample deposited *in-situ*. The inset shows the I-V curves measured from heterojunction diodes used to calculate the ideality factor.

is closer to the ideality compared to that deposited *ex-situ*. This is due to a better quality of the interface.

The CdTe/CdS heterojunction was evaluated as a function of temperature to understand the transport mechanism in the PN heterojunction along with evaluation of the built-in potential, which is closely related to the operation voltage of JFETs.[28] Some reports demonstrate operational JFETs with a high $V_{bi} = 2.5$ V for epitaxially grown SiC JFET[28] but as low as 0.6 V for p-$ZnCo_2O_4$/n-ZnO thin-film heterojunctions deposited by PLD.[29,30] Based on the built-in potential extraction methodology implemented, the importance of properly selecting the method to evaluate these devices is critical. The built-in potential calculated by C-V measurements showed frequency dependence resulting in incorrect results since in this method, the calculated V_{bi} varied around 1 V instead of a fixed value. The built-in potential calculated using the temperature dependence led to a V_{bi} value much closer to the theoretical value ($\sim$0.7 V) for this heterojunction. The reverse bias current of the PN heterojunctions is also evaluated and related to the gate leakage current in a JFET since the current flowing to the gate is the current crossing the reverse biased PN junction formed between the drain-gate contacts. Some authors report operational JFETs with leakage current up to 100 nA.[31–33]

For the diode fabrication, a commercially available PLD Pioneer 180 from Neocera Inc. was used to deposit the CdTe/CdS heterojunctions. The system includes a 248 nm KrF excimer laser with energy density (J_e) adjusted optically to 1 J/cm^2. The laser frequency was maintained at 10 Hz. For all depositions, the background pressure was 1×10^{-6} Torr and a mass flow controller (MFC) was used to control the deposition pressure (varying Ar gas flow). The deposition starts by depositing the CdS layer on pre-cleaned ITO-glass substrates at a deposition pressure of 60 mTorr and 6500 laser pulses. This results in films with a thickness of 50 nm. Next, the CdTe layer was deposited *in-situ* at a deposition pressure of 20 mTorr and 20 000 laser pulses for a thickness of $\sim$100 nm. Both layers were deposited at 220 °C, this temperature was selected from our previous report.[21] After deposition, CdTe/CdS was annealed at 360 °C in a N_2 atmosphere for 30 min. This annealing improves the diode performance by passivating grain boundaries and increases the CdTe grain size.[1,34,35] Gold (Au) and copper (Cu) contacts were deposited using a shadow mask followed by N_2 annealing at 150 °C for 30 min.[35] This annealing diffuses copper into CdTe to reduce contact resistance, as previously reported.[21]

A Keithley 4200-SCS system and a HP 4284A precision LCR meter were used for current-voltage (I-V) and capacitance-voltage (C-V) measurements, respectively. A Cascade Microtech probe station with chuck temperature control was used for the I-V and C-V measurements at different temperatures. For these measurements, the temperature was increased in 10 °C increments up to 150 °C. At each temperature step, the I-V curves were measured, while the C-V curves were measured at 50 °C, 100 °C, and 150 °C. Two different device diameters, 100 μm and 200 μm, were measured. The diode analysis was carried out using the thermionic emission theory. Thermionic emission is the most common theory associated with a potential barrier for carrier transport. Due to the expected potential barrier height and the depletion width for these CdTe/CdS devices, the tunneling current should be negligible and only thermionic emission current should contribute to carrier transport. As a result, thermionic emission theory was used to calculate the diode parameters such as ideality factor, series resistance, saturation current, and built-in potential, V_{bi}. V_{bi} is the potential voltage across the depletion width formed in the PN junction. C-V analysis was used to calculate the carrier concentration, while the extrapolation of the linear fitting of $1/C^2$ vs. V plots was used to determine V_{bi}. V_{bi} obtained using this methodology was compared with V_{bi} obtained from the temperature dependence of I-V.

The forward bias current was used to calculate the saturation current using the formula[36–38]

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \tag{1}$$

where I_0 is the saturation current, q is the electron charge, V is the applied voltage across the junction, n is the ideality factor, k is the Boltzmann constant, and T is the temperature.

The ideality factor was calculated for different temperatures using[36,38]

$$n = \frac{q}{\ell n(10)\left(\frac{d\log I}{dV}\right)kT} = \frac{q}{2.3\left(\frac{d\log I}{dV}\right)kT}. \tag{2}$$

In Eq. (1), I_0 corresponds to the saturation current, and it is defined as[36–38]

$$I_0 = AA^*T^2\exp\left(-\frac{q\varphi_b}{kT}\right), \tag{3}$$

where A is the device area, A* is the Richardson constant, and φ_b is the potential barrier. Equation (3) was used to obtain the potential barrier for the CdTe/CdS junction. The series resistance (R_s) was calculated in the region for $V \gg V_{bi}$ using[38]

$$\frac{1}{g_d} = \frac{nkT}{q} + IR_s, \tag{4}$$

where $g_d = dI/dV$ is the diode conductance.

For the C-V analysis, the carrier concentration [p(W)] was calculated from a $1/C^2$ vs. V plot using the following equation:[36,38]

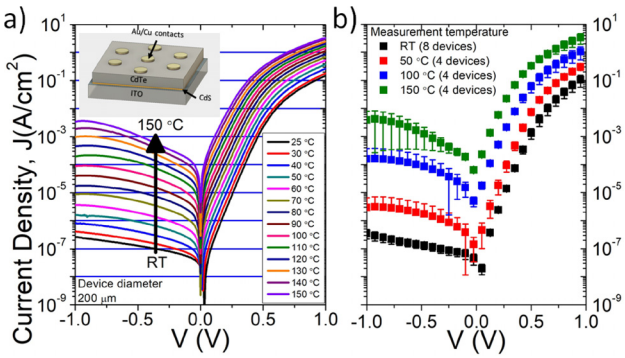

FIG. 2. (a) I-V curves measured at different temperatures (RT up to 150 °C). The current density increased for reverse and forward bias with increasing temperature. Higher temperature increases the energy of free carriers, allowing more carriers to cross the junction and contribute to current flow. (The inset shows the structure of CdTe/CdS diodes deposited on commercial ITO-glass substrates. CdTe and CdS were deposited *in-situ* by PLD.) (b) The temperature dependence of the current is evident even in the presence of some variability under reverse bias conditions at 150 °C.

$$p(W) = -\frac{C^3}{qK_s\varepsilon_0 A^2 \frac{dC}{dV}} = \frac{2}{qK_s\varepsilon_0 A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}}, \tag{5}$$

where K_s is the dielectric constant and ε_0 is the permittivity of free space. Using the same plot, the V_{bi} potential is calculated using[36–38]

$$C^{-2} = 2\left[\frac{\left(V_{bi} - V - \frac{kT}{q}\right)}{qA^2K_s\varepsilon_0 N_A}\right], \tag{6}$$

where N_A is the doping density.

Figure 2(a) shows typical I-V curves for a 200 μm device as a function of temperature; the inset in Fig. 2(a) shows the structure of the diodes fabricated. For reverse bias conditions, the main transport mechanism is the generation of charges in the depletion region. Here, electron–hole pairs produced in this region are separated by the electric field. When the temperature increases, more charges are produced due to the increasing kinetic energy; therefore, a higher temperature increases the reverse current at a higher rate than for forward bias. Figure 2(b) shows the current density with error bars for different measurement temperatures. All parameters under investigation were calculated using the forward bias current region. This region showed a small standard deviation, and the temperature dependence trend is not modified. The standard deviation for the reverse bias current region is more affected when temperature increased; however, a temperature dependence is clearly seen.

For the forward bias case, current increases with increasing temperature due to the increase of thermionic emission. The thermionic-emission model is described in Fig. 3. The PN junction forms a potential barrier due to mismatching in the band structure shown as $V_{bi} - V_A$. V_{bi} is the built-in potential formed at the interface under equilibrium conditions with no bias applied, and V_A is the potential applied across the PN junction. Electrons with enough kinetic energy to cross the potential barrier contribute to forward bias current. Fermi-Dirac statistics describe that the density of

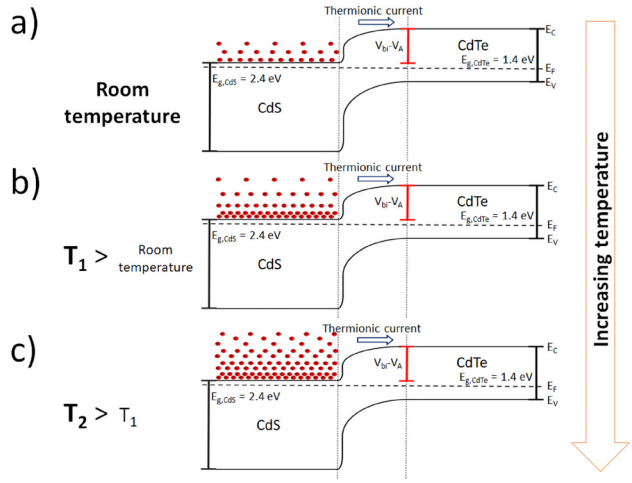

FIG. 3. Band diagram for heterojunction diodes and the thermionic emission effect. (a) At room temperature, the kinetic energy of electrons enables some electrons to have enough energy to surmount the potential barrier at the interface. (b) and (c) As the temperature increases, more energetic electrons are able to surmount the barrier and increase the current flowing at the interface, thereby contributing to the diode current.

electrons and energy of these electrons in the conduction band increase for higher temperature. Figure 3 shows that more electrons can contribute to forward current crossing a constant potential barrier when increasing temperature. Next, the rectification factor, saturation current, ideality factor, and series resistance were obtained using the model previously described as a function of temperature.

Figure 4(a) shows the rectification factor for different voltages and temperatures. In this figure, for low voltage (<0.3 V), the rectification is independent of temperature; however, for higher voltages, the rectification factor is inversely proportional to the temperature. For low voltage biased, forward current and reverse current are dominated by

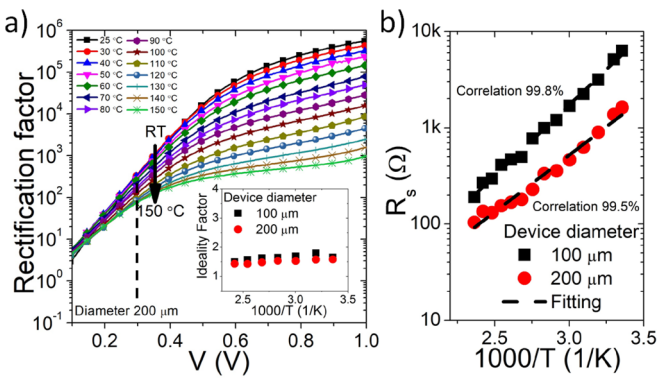

FIG. 4. (a) Rectification factor for different applied voltages. For applied voltage <0.3 V (dash line), the rectification factor is mostly temperature independent; however, for higher voltages, the rectification factor is lower as temperature increases. The increment of the rectification factor for higher temperatures and voltages is related to traps in the bulk and interface of the heterojunction. (Inset: The effect of the temperature measurement on the ideality factor calculated from I-V curves. As it was expected, the ideality factor is temperature independent and it is close to a constant value, between 1 and 2, for different temperatures.). (b) Effect of the temperature on series resistance. The log scale in series resistance demonstrates a linear behavior, with a correlation close to 100% with respect to 1000/T. The series resistance decreased when measurement temperature was increased. Free carriers with more energy can cross a barrier potential at the CdTe-metal interface decreasing the contact resistance.

thermionic emission current and generation current, respectively. Both transport mechanisms are affected proportionally by temperature. As a result, the rectification factor is constant for low voltage bias. In addition, for higher voltage bias, forward bias depends on the series resistance, while reverse current still depends on the generation current. The impact of the temperature on generation current is more dominant than that on the series resistance. For this reason, at higher negative voltages, the reverse bias current increases faster than the forward bias current, reducing the rectification factor for higher temperature.

The inset of Fig. 4(a) shows the ideality factor behavior at different temperatures. The ideality factor is related to the transport mechanism in a PN junction. For an ideality factor close to 1, the diffusion current dominates; similarly, for an ideality factor close to 2, the recombination current dominates. In this case, the ideality factor is between 1 and 2 at room temperature, and this indicates that both processes contribute to carrier transport. However, for higher temperature, the diffusion current increases due to the thermionic effect; this is why the ideality factor decreases slightly when increasing the temperature.

Figure 4(b) shows the log of series resistance vs. 1000/T for different temperatures. In this figure, the series resistance decreases with increasing temperature. CdTe-based devices are reported to have series resistance primarily due to the resistivity of CdTe bulk and high contact resistance. The CdTe bulk resistance decreases for higher temperature due to trapping and bond breaking in the bulk of the film, which produce additional free carriers that contribute to the reduction in series resistance.[36] Besides, CdTe contact resistance also decreases when temperature increases. This is due to the interface between the CdTe and metal contact, which is usually reported as non-Ohmic.[39,40] The non-ohmic behavior is related to a potential barrier at the CdTe–metal interface, leading to an increase in the series resistance. Similar to the CdTe/CdS interface, the thermionic effect increases the number of carriers crossing the potential barrier at the CdTe–metal interface, decreasing the contact resistance as temperature increases. The linear behavior of the log scale R_s vs. 1000/T shown in Fig. 4(b) is consistent with the thermionic effect model. As a result, R_s decreases for higher temperatures since CdTe bulk resistance and CdTe contact resistance are expected to decrease with increasing temperature. The series resistance for the smaller device (100 μm device diameter) varied from $\sim$6 kΩ to $\sim$200 Ω, and it was slightly higher compared to the 200 μm device diameter, which varied from $\sim$1.5 kΩ to $\sim$100 Ω. This reduction in R_s with respect to the device area is caused by larger area devices having more probability to find leakage paths through the films, which can increase the current.

The log saturation current density is shown in Fig. 5(a). The linearized fitting means that the current in the junction is dominated by the thermionic effect.[37] The log current vs. 1000/T shows a linear behavior for the two different area devices under test. The linear fitting in the semi-log plot was used to find the built-in potential which was calculated to be 0.66 V and 0.7 V for devices with 100 μm and 200 μm diameter, respectively. These V_{bi} values are similar to those reported by other authors ($\sim$0.6 V).[41,42]

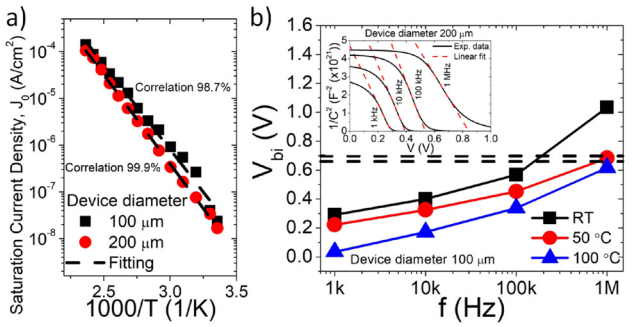

FIG. 5. (a) Effect of the temperature on saturation current calculated from I-V curves. The saturation current demonstrated a linear behavior on a log scale, with a correlation close to 100% with respect to 1000/T values. The linear behavior of the saturation current with respect to the temperature showed that the current across the junction is dominated by the thermionic effect. (b) The effect of frequency and temperature analysis on Vbi from C-V curves. Vbi increased from 0 to 1 V when frequency was increased. This is an inaccurate value due to parasitic effects. Vbi decreased for the higher temperature measurement due to more energetic carriers surmounting the effective barrier potential. The dashed line indicates Vbi calculated from I-V curves at different temperatures. (The inset illustrates the effect of the frequency on the C-V measurement. The linear fitting was used for Vbi extraction from C-V measurements. The linear fitting crossing the x-axis showed Vbi for each measurement. Different frequencies produced different values for Vbi calculation due to parasitic effects.

Figure 5(b) shows the extracted V_{bi} potential calculated from C-V analyses. Clearly, V_{bi} is frequency and temperature dependent. This variation makes it difficult to determine an accurate value for V_{bi} using this method. This effect is reported to be due to deep level traps at the CdTe/CdS interface, which do not respond at high frequencies.[43,44] This V_{bi} shift can be due to other effects including multiple trap states due to the polycrystalline materials and non-ideal interfaces.

The inset in Fig. 5(b) shows a typical $1/C^2$ vs. V plot. The extrapolation of the linear fitting is used to calculate V_{bi} directly from the plot. Although V_{bi} is expected to be around 0.7 V, the values extracted using this method vary substantially as calculated using the thermionic emission model. At lower frequencies, the $1/C^2$ curves drop when $V < V_{bi}$. This is due to traps being able to capture and emit carriers in the bandgap at the CdTe/CdS heterojunction at the lower measurement frequency, thereby contributing to carrier transport across the interface. At low frequency, the process of charge trapping and detrapping is more effective and traps contribute to carrier transport across the CdTe/CdS interface. This results in V_{bi} shifting to higher values for lower frequencies, which is consistent with Fig. 5(b). On the other hand, higher temperatures also contribute to trapping and detrapping charges faster, due to increased kinetic energy. For that reason, a larger V_{bi} shifting is expected for higher temperature, as shown in Fig. 5(b). The impact of frequency and temperature in the V_{bi} potential shift for $1/C^2$-V curves is consistent with the effect of traps on the CdTe/CdS interface.

In addition, the C-V measurements were used to calculate the carrier concentration at different frequencies and temperatures. Carrier concentration is not expected to change over this small temperature variation. The leakage current is very high for samples measured at 150 °C, and it was not possible to measure the capacitance. Thus, characteristic devices were measured at RT, 50 °C, and 100 °C. The carrier concentration was calculated to be $\sim 10^{16}$ cm^{-3} at different

frequencies and temperatures. This carrier concentration value is consistent with a previous report.[21] The carrier concentration is related to the sulfur diffusion in the CdTe layer due to the thickness of CdTe.

In summary, *in-situ* CdTe/CdS heterojunction diodes were electrically characterized and analyzed at different temperatures to evaluate this heterojunction as a prospect for possible application in JFET implementation. The temperature dependence of these devices was used to understand the transport mechanism at the interface and to calculate important diode parameters. The thermionic effect current was demonstrated to be the main transport mechanism at the interface due to the linear dependence of the saturation current with respect to the 1/T plot. The I-V curves at different temperatures demonstrated an effective method for built-in potential extraction where V_{bi} values for the CdTe/CdS heterojunction were calculated to be 0.66 and 0.7 V for different devices. These are expected values from a band diagram perspective. C-V analysis is shown to be an effective method for finding the carrier concentration; however, the frequency dependence showed that due to a large number of traps and parasitic effects, C-V curves produced a shift in V_{bi} calculation, and the value obtained using this method was not accurate. Also, as expected, the ideality factor and the carrier concentration of CdTe did not show a temperature dependence. Finally, the rectifier behavior was demonstrated for CdTe/CdS devices ($\sim 10^6$ rectification factor at 1 V), low saturation current density ($\sim 10^{-8}$ A/cm^2), and low reverse bias current density ($\sim 10^{-7}$ A/cm^2 at 1 V). The reverse bias current measured for these devices at different temperatures was at least 10× lower than other reported values.[42] The reverse bias current density for these diodes should produce a JFET leakage current in the order of nA due to expected JFET dimensions ($\ll 1$ cm^2). These parameters make CdTe and CdS prospective materials for implementation as rectification diodes as well as more complex devices based on heterojunction structures, such as JFETs.

This work was supported in part by the CONACYT Program and an NSF CAREER Award under the NSF Award ECCS-1653343.

[1]Z. Bai, L. Wan, Z. Hou, and D. Wang, Phys. Status Solidi C **8**(2), 628–630 (2011).
[2]F. de Moure-Flores, J. G. Quinones-Galvan, A. Guillen-Cervantes, J. S. Arias-Ceron, A. Hernandez-Hernandez, J. Santoyo-Salazar, J. Santos-Cruz, S. A. Mayen-Hernandez, M. de la, L. Olvera, J. G. Mendoza-Alvarez, M. Melendez-Lira, and G. Contreras-Puente, J. Crystal Growth **386**, 27 (2014).
[3]S. R. Ferrá-González, D. Berman-Mendoza, R. García-Gutiérrez, S. J. Castillo, R. Ramírez-Bon, B. E. Gnade, and M. A. Quevedo-López, Optik **125**(4), 1533 (2014).
[4]F. Atay, V. Bilgin, I. Akyuz, and S. Kose, Mater. Sci. Semicond. Process. **6**(4), 197 (2003).
[5]T. L. Chu, S. S. Chu, C. Ferekides, C. Q. Wu, J. Britt, and C. Wang, J. Appl. Phys. **70**(12), 7608 (1991).
[6]H. Lin, W. Xia, H. N. Wu, and C. W. Tang, Appl. Phys. Lett. **97**(12), 123504 (2010).
[7]J. Britt and C. Ferekides, Appl. Phys. Lett. **62**(22), 2851 (1993).
[8]M. Ristova, M. Ristov, P. Tosev, and M. Mitreski, Thin Solid Films **315**(1-2), 301 (1998).
[9]T. Aramoto, F. Adurodija, Y. Nishiyama, T. Arita, A. Hanafusa, K. Omura, and A. Morita, Sol. Energy Mater. Sol. Cells **75**(1-2), 211 (2003).
[10]H. Jun-feng, F. Gan-hua, V. Krishnakumar, L. Cheng, and W. Jaegermann, J. Mater. Sci.-Mater. Electron. **24**(8), 2695 (2013).
[11]A. L. Salas-Villasenor, I. Mejia, M. Sotelo-Lerma, Z. B. Guo, H. N. Alshareef, and M. A. Quevedo-Lopez, Semicond. Sci. Technol. **29**(8), 085001 (2014).
[12]S.-J. Ding, S. Liang, F. Nan, X.-L. Liu, J.-H. Wang, L. Zhou, X.-F. Yu, Z.-H. Hao, and Q.-Q. Wang, Nanoscale **7**(5), 1970 (2015).
[13]N. A. Shah, A. Nazir, W. Mahmood, W. A. A. Syed, S. Butt, Z. Ali, and A. Maqsood, J. Alloys Compd. **512**(1), 27 (2012).
[14]A. F. Mulla, A. S. Al-Shamrnari, A. M. Elnaggar, W. M. Al-Ayashi, and A. M. Al-Dhafiri, in *The Conference Record of the IEEE Photovoltaic Specialists Conference* (2009).
[15]C. Gretener, M. Wyss, J. Perrenoud, L. Kranz, S. Buecheler, and A. N. Tiwari, in *2014 IEEE 40th Photovoltaic Specialist Conference (Pvsc)* (2014), p. 3510.
[16]W. S. M. Brooks, S. J. C. Irvine, and D. M. Taylor, Semicond. Sci. Technol. **28**(10), 105024 (2013).
[17]S. Butt, N. A. Shah, A. Nazir, Z. Ali, and A. Maqsood, J. Alloys Compd. **587**, 582 (2014).
[18]T. Okamoto, R. Hayashi, S. Hara, and Y. Ogawa, Jpn. J. Appl. Phys. **52**(10), 102301 (2013).
[19]E. Hernández-Rodríguez, M. Loeza-Poot, I. Riech, V. Rejón, and J. L. Peña, J. Phys. D: Appl. Phys. **48**(25), 255102 (2015).
[20]M. Becerril, A. Picos-Vega, O. Zelaya-Angel, R. Ramirez-Bon, F. J. Espinoza-Beltran, J. Gonzcalez-Hernandez, and B. Chao, J. Phys. Chem. Solids **60**(2), 257 (1999).
[21]J. Avila-Avendano, I. Mejia, H. N. Alshareef, Z. Guo, C. Young, and M. Quevedo-Lopez, Thin Solid Films **608**, 1 (2016).
[22]N. Hernandez-Como, V. Martinez-Landeros, I. Mejia, F. S. Aguirre-Tostado, C. D. Nascimento, G. D. Azevedo, C. Krug, and M. A. Quevedo-Lopez, Thin Solid Films **550**, 665 (2014).
[23]F. de Moure-Flores, J. G. Quinones-Galvan, A. Guillen-Cervantes, J. Santoyo-Salazar, A. Hernandez-Hernandez, M. de la L. Olvera, M. Zapata-Torres, and M. Melendez-Lira, AIP Adv. **2**(2), 022131 (2012).
[24]C. Ding, Z. Ming, B. Li, L. Feng, and J. Wu, Mater. Sci. Eng., B **178**(11), 801 (2013).
[25]P. Hu, B. Li, L. Feng, J. Wu, H. Jiang, H. Yang, and X. Xiao, Surf. Coat. Technol. **213**, 84 (2012).
[26]J. M. Luther, S. W. Johnston, S. R. Kurtz, R. K. Ahrenkiel, and R. T. Collins, Appl. Phys. Lett. **88**(26), 263502 (2006).
[27]R. A. Minamisawa, A. Mihaila, I. Farkas, V. S. Teodorescu, V. V. Afanas'ev, C. W. Hsu, E. Janzén, and M. Rahimo, Appl. Phys. Lett. **108**(14), 143502 (2016).
[28]R. K. Malhan, M. Bakowski, Y. Takeuchi, N. Sugiyama, and A. Schöner, Phys. Status Solidi A **206**(10), 2308 (2009).
[29]F. J. Klupfel, A. Holtz, F. L. Schein, H. Von Wenckstern, and M. Grundmann, IEEE Trans. Electron Devices **62**(12), 4004 (2015).
[30]F. L. Schein, M. Winter, T. Böntgen, H. Von Wenckstern, and M. Grundmann, Appl. Phys. Lett. **104**(2), 022104 (2014).
[31]J. B. Boos, W. Kruppa, and B. Molnar, Proc. SPIE **1144**, 306 (1989).
[32]W. C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T. J. K. Liu, and A. P. Pisano, IEEE J. Electron Devices Soc. **2**(6), 164 (2014).
[33]R. Karsthof, H. Von Wenckstern, and M. Grundmann, IEEE Trans. Electron Devices **62**(12), 3999 (2015).
[34]B. Maniscalco, A. Abbas, J. W. Bowers, P. M. Kaminski, K. Bass, G. West, and J. M. Walls, Thin Solid Films **582**, 115 (2015).
[35]N. R. Paudel, A. D. Compaan, and Y. Yan, Sol. Energy Mater. Sol. Cells **113**, 26 (2013).
[36]E. Coskun, H. H. Gullu, I. Candan, O. Bayrakli, M. Parlak, and C. Ercelebi, Mater. Sci. Semicond. Process. **34**, 138 (2015).
[37]G. K. Rao, K. V. Bangera, and G. K. Shivakumar, Solid-State Electron. **56**(1), 100 (2011).
[38]D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, Hoboken, NJ, 2006).
[39]J. H. Yun, K. H. Kim, D. Y. Lee, and B. T. Ahn, Sol. Energy Mater. Sol. Cells **75**(1-2), 203 (2003).
[40]S. Uličná, P. J. M. Isherwood, P. M. Kaminski, J. M. Walls, J. Li, and C. A. Wolden, Vacuum **139**, 159 (2017).
[41]P. R. Kharangarh, G. E. Georgiou, and K. K. Chin, *The Materials Research Society Symposium Proceedings* (2013).
[42]T. L. Chu, S. S. Chu, and S. T. Ang, J. Appl. Phys. **64**(3), 1233 (1988).
[43]N. Taoka, T. Kubo, T. Yamada, T. Egawa, and M. Shimizu, Microelectron. Eng. **178**, 182 (2017).
[44]A. Tataroğlu and Ş. Altındal, Microelectron. Eng. **83**(3), 582 (2006).