An investigation of the electrical properties of the interface between pyrolytic carbon and silicon for Schottky diode applications

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An investigation of the electrical properties of the interface between nano-crystalline, pyrolytic carbon, and silicon is presented. We have deposited conductive carbon films on silicon substrates by the pyrolysis of ethene and structured them into Schottky diodes in order to evaluate the electrical properties of the interface. The results show that the Schottky barrier to n-doped silicon is 0.46 eV, whereas for p-doped silicon, it is 0.66 eV. The carbon to n-type silicon barrier height is comparable to the values for metal silicide contacts in commercial devices. The results imply that no interfacial layer is formed and show the absence of Fermi-level pinning. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4725429]

INTRODUCTION

The increasing speeds for data transfer and wireless applications requires continued improvement in the switching speeds and response times of semiconductor devices. One of these devices is the Schottky diode used in high frequency applications due to its low capacitance and high current density.

Schottky diodes are formed at the interface between a metal and a semiconductor. The metal chosen for the contact must be stable under the high current densities applied and also generate a small Schottky barrier. The barrier height depends in part on the metal as well as the interface quality.[1] However, the metals tend to form an alloy with the silicon at the interface known as a silicide. The silicide has an effective work-function closer to the silicon band center,[2] increasing the Schottky barrier height. This has an exponential effect on the current carrying capacity of the device leading to larger device areas and corresponding capacitances. Metal silicides often exhibit uneven interfaces with silicon,[3] leading to two main device variability issues: fluctuations in the active diode area and local barrier lowering at silicide protrusions.[4,5] Moreover, it has been shown that the interface trap density in silicide-silicon junctions can be considerable resulting in enhanced noise.[6] Barrier heights as low as 0.11 eV (Ref. 7) have been reported in the literature; however, the typical barrier height of a production diode is around 0.45 eV (Ref. 8) probably due to manufacturing constraints, such as compatibility of the materials with the semiconductor production line, and device reliability.

A stable metal-semiconductor interface is a prerequisite for applications at elevated temperatures. For metal contacts, the form of the interface, for example, the phase of the silicide, may change at higher temperatures leading to an irreversible barrier height change.[9] Hence, an electrode material with similar barrier characteristics but with a better thermal stability would be desirable for high temperature devices.

Investigations of diodes made from r.f. magnetron sputtered carbon on silicon have been reported.[10] The carbon films deposited using this method are either narrow gap semiconductors or insulators with high resistivities $\sim 10^4$–10^6 Ω cm due to their high sp^3 bond fraction.[11] The diode current was found to follow the classical rectification behavior with a built-in voltage of 0.35 V on n-Si substrates with the current strongly limited by the carbon film resistivity.[10] This built-in voltage corresponds to a Schottky barrier height of around 0.6 V.

Pulsed laser deposited carbon films on Si have also been investigated.[12] Small band-gap semiconducting carbon films with resistivities as low as 2 mΩ cm were reported. However, the films were not structured into diodes and a barrier was not reported.

Highly conductive, pyrolytic carbon (PC) deposited in a simple chemical vapor deposition (CVD) process in a hot-wall reactor has been investigated as a material for gate electrodes,[13] trench capacitors,[14] and memory elements.[15,16] The properties of PC in vias and wires with nanometer dimensions have also been evaluated and no size effect due to grain boundary scattering was found.[17] The films reported have low resistivities of several mΩ cm. More recently pyrolysed photoresist films and PC have been formed into Schottky diodes on n-type silicon with a barrier of 0.6 eV and an ideality factor of 1.44.[18]

There is a considerable body of work on the CVD of carbon from various precursors.[19–24] However, except for Ref. 18, there appears to have been no investigation of *CVD* carbon growth directly on oxide-free silicon below 900 °C and on the electrical properties of the interface. In this paper, we present evidence that PC carbon can be used to make Schottky diodes on silicon with barriers as low as 0.46 eV.

EXPERIMENTAL

The carbon films investigated in the present work were deposited in an 8 in. wafer, single zone, hot-wall, quartz tube reactor at 860 °C using a 10:3 mixture of nitrogen to ethene at a pressure of 80 mbar. The nitrogen flow was 200 sccm and the ethene flow was 60 sccm, as described elsewhere.[25]

Raman and TEM analysis of the films indicate a nanocrystalline sp^2 bonded carbon structure with average grain sizes around 1.7 nm, in line with previous investigations.[19–24]

The silicon substrates were obtained from 6 in. wafers with resistivities of 3.5 Ω cm for p-type and 2 Ω cm and 0.03 Ω cm for n-type. These resistivities correspond to doping levels of $4 \times 10^{15}\,cm^{-3}$, $3 \times 10^{15}\,cm^{-3}$, and $5 \times 10^{17}\,cm^{-3}$, respectively.[26] The silicon samples were first etched in 4% dilute hydrofluoric acid (DHF) for 10 min to remove the native oxide and other contaminants. After a de-ionized (DI) water rinse they were further cleaned using 0.3% dilute hydrochloric acid (HCl) to etch away any remaining metal contamination. After a further rinse for several minutes in flowing DI water they were dried in nitrogen and transferred into the reactor oven within several minutes. The substrates were heated up to 860 °C in the nitrogen-ethene mixture to minimize the risk of obtaining a thin oxide interface between the silicon and carbon. The deposition process was continued for 8 min at 860 °C after which the gases were evacuated and the oven cooled down to less than 100 °C for the samples to be removed.

The carbon films were subsequently annealed for 10 s at 1000 °C in flowing nitrogen in a rapid thermal process (RTP) run on separate equipment. This was found to improve the resistivity of the carbon film from 2.9 mΩ cm to 1.5 mΩ cm (Ref. 17) and harden the surface. No changes in the Raman spectra or TEM images of the films were found after annealing. We suggest that the conductivity improvement is the result of hydrogen desorption out of the film and the subsequent formation of additional conductive sp^2 bonds. Scanning electron microscope images of the cross-section show that the carbon layer has a thickness of around 45 nm using this process and a TEM analysis found no oxygen at the carbon-silicon interface or evidence of a significant silicon carbide layer.

In order to obtain a good contact to the substrate carbon residuals on the back side were removed with a short oxygen remote plasma etch run on an ATV SRO 706 lamp oven modified with a 2.45 GHz R^3T microwave radical generator. The back side was then sputtered with argon before being deposited with 20 nm titanium or 30 nm platinum in the same apparatus without an air-break.

The diode devices were generated using a metal dot array deposited on top of the carbon and remote plasma etching. The metal stack was composed of a 30 nm thick titanium layer for the devices on p-type substrates and 10 nm titanium and 40 nm gold on n-type silicon structured into dots with areas of 3050 μm^2. The additional gold on the n-type substrate components was required to reduce the series resistance of the device and the contacts to the measurement system. The exposed carbon between the pads was removed with a remote oxygen plasma using the metal dots as a mask.

Electrical evaluation of the diode I–V characteristics was carried out on a Süss PM5 probe station connected to a Keithley 2400 source measurement unit and a Keithley 2700 multi-meter. Automatic electrical measurements were enabled using in-house routines running under LabView. The capacitance measurements were carried out at frequencies between 10 kHz and 1 MHz at an AC voltage amplitude of 30 mV on a Cascade probe station with a Keithley 4200 parameter analyzer. Several tens of diodes were evaluated on different samples to ensure consistent results. All electrical measurements were carried out at an ambient temperature of 22 °C.

ELECTRICAL RESULTS AND DISCUSSION: I–V

The current-voltage (I–V) characteristics of carbon on p-type substrates were measured by biasing the metal pads in the voltage range ±0.5 V relative to the substrate. The devices were made with a 30 nm thick titanium top contact and 20 nm Ti back contact. Figure 1 shows the results from 3 separate devices indicating current rectification and typical Schottky diode behavior. In the forward direction (negative pad voltage), the devices show a distinct exponential current dependence up to about −0.3 V. For more negative voltages, the current levels off due to the series resistance. In the reverse bias direction (positive pad voltage), the current displays an exponential increase with a much lower slope than in the forward direction. Further, in the forward direction, the devices show a very little spread indicating a small device area distribution. There are small deviations between the devices for reverse biases which may be related to small differences in the pad edge roughness.

The equations used to describe the behavior of Schottky diodes are well known.[1] The forward current density J follows the form:

$$J_F = J_0(\exp((\beta(V_D - JAR))/n) - 1), \tag{1}$$

where $\beta = q/k_BT$, with q the electron charge, k_B the Boltzmann constant, and T the absolute temperature. V_D is the voltage across the whole device, A is the device area, R is the series resistance of the device, and n the ideality factor.

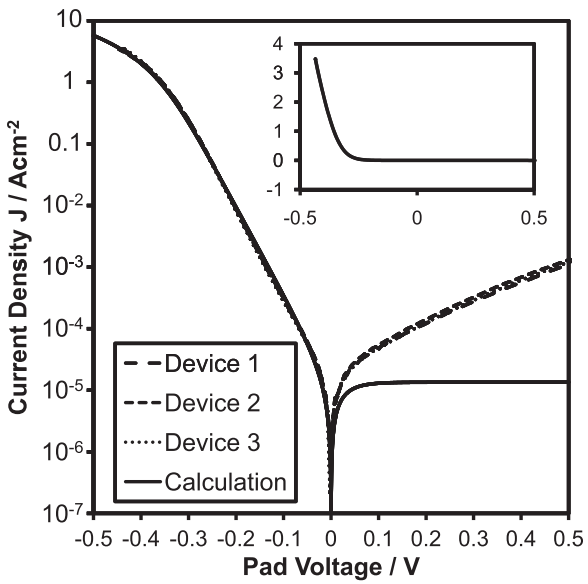

FIG. 1. Current-voltage characteristics of 3 diodes on p-type silicon substrates. The inset shows the current on a linear scale. The calculation shows a fit to the measured curves with a barrier height of $\phi_B = 0.66$ eV, an ideality of $n = 1.2$ and a series resistance of $R_s = 600\ \Omega$.

The prefactor J_0 depends on the temperature and the barrier height in the following way:

$$J_0 = A^{**}T^2\exp(-\beta\phi_B), \tag{2}$$

where A^{**} is the effective Richardson constant and ϕ_B is the barrier height. In the current work, values of $A^{**} = 110$ $\mathrm{A\,cm^{-2}\,K^{-2}}$ for electrons (n-type) and $A^{**} = 30$ $\mathrm{A\,cm^{-2}\,K^{-2}}$ for holes (p-type)[1] have been used to determine the barrier heights.

Fitting equation (1) to the results for C-Si diodes on p-type substrates yields $J_0 = 1.35 \times 10^{-5}$ $\mathrm{A\,cm^{-2}}$, $R = 600\ \Omega$ and $n = 1.2$. This value of J_0 corresponds to a barrier height of $\phi_B = 0.66 \pm 0.02$ eV using Eq. (2). The relatively high series resistance is due to the low substrate doping level of only 4×10^{15} $\mathrm{cm^{-3}}$ but this does not affect the interpretation of the curves since the diode resistance is much higher over much of the measured voltage range.

The measured I–V curves deviate significantly from the calculation for reverse biases. This is partly because of static and Schottky barrier lowering but mostly due to the edges of the carbon dots which are also directly on the substrate and produce high electrical fields in contrast to Eq. (1) which assumes a perfectly parallel field. In commercial components, the boundaries reside on isolation areas known as guard-rings which ensure more uniform electrical fields even at the device edges.[1]

The ideality factor $n = 1.2$ compares well with commercial devices where n is typically between 1.05 and 1.10. Here again, the edges of the devices can play an important role as well as the contact of the device to the measurement apparatus, particularly the back contact which in this case is itself a large reverse biased diode.

Figure 2 presents the I–V characteristics of carbon-silicon devices fabricated on n-type substrates with a doping concentration of 3×10^{15} $\mathrm{cm^{-3}}$. It is immediately clear that the current densities are several orders of magnitude higher than for the devices on p-type substrates, indicating a much lower barrier height. Due to the higher currents involved the backside was coated with 30 nm platinum and the metal dots on the carbon were 10 nm Ti and 40 nm Au in order to reduce the series resistance of the contacts. However, despite this, the series resistance of the substrate still has a significant impact on the forward bias current and there is no distinct exponential behavior as observed for the p-type diodes.

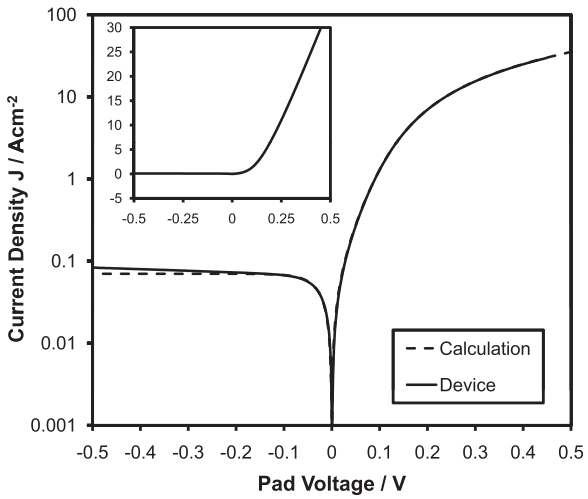

FIG. 2. Current-voltage characteristics of a diode on an n-type silicon substrate with a dopant concentration of 3×10^{15} $\mathrm{cm^{-3}}$. The calculation (dashed line) shows a fit to the measured curves with a barrier height of $\phi_B = 0.46$ eV, an ideality of $n = 1.17$ and a series resistance of $R_s = 294\ \Omega$. The upper left insert shows the current density on a linear scale.

A fit of Eq. (1) to the forward bias results yields $J_0 = 0.07$ $\mathrm{A\,cm^{-2}}$, $R = 294\ \Omega$, and $n = 1.17$. The higher value of J_0 corresponds to a barrier height of 0.46 eV. As for the p-type diodes, the reverse bias current is higher than calculated due to the poorly defined device edge potentials. The ideality factor is similar to the value obtained for the p-type silicon-carbon diodes.

Diodes were also made on n-type silicon substrates with a 100× higher doping level in order to reduce the series resistance of the substrate. The samples used have a dopant concentration of 5×10^{17} $\mathrm{cm^{-3}}$, which means that direct tunneling through the barrier becomes significant.[1] In order to minimize the impact of the substrate resistance, the voltage across the diode was measured to a neighboring device placed 100 μm away. The difference is shown between the solid line and dashed-dotted line curves in Figure 3, highlighting the impact of the substrate. In this case, the substrate resistance is reduced by the shorter distance between the neighboring devices (100 μm) compared with the substrate thickness (750 μm) and elimination of the contribution of the backside contact resistance.

The current densities for the higher doped substrate diodes are about 1–2 orders of magnitude higher than for the low doped diodes. In this case, an effective barrier height of $\phi_B = 0.41$ eV and an ideality of $n = 1.3$ are found. This suggests that the high substrate doping makes the barrier thinner increasing direct tunneling and contributing to barrier lowering.[1] At higher doping levels, the diodes also become less

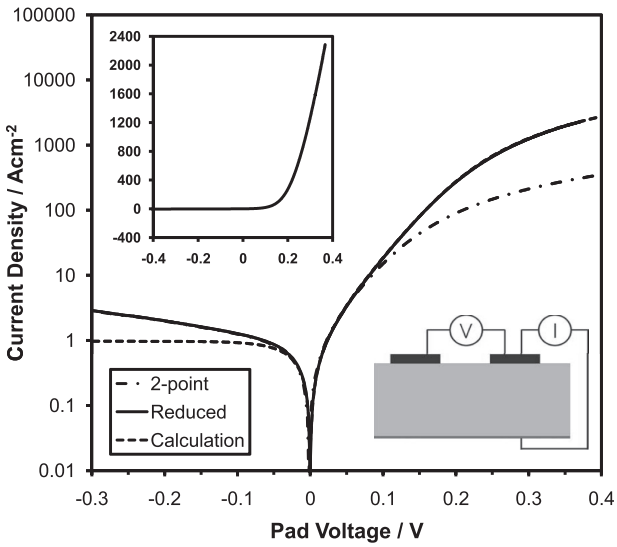

FIG. 3. Current-voltage characteristics of a diode on n-type silicon with a dopant concentration of 5×10^{17} $\mathrm{cm^{-3}}$ measured in 2-point (dotted-dashed line) and reduced series resistance (solid line) setup (lower right hand insert). The calculation (dashed line) shows the fit with a barrier height of $\phi_B = 0.41$ eV, ideality $n = 1.30$ and a series resistance of $R_s = 1.6\ \Omega$. The upper left insert shows the current density on a linear scale.

ideal, resulting in the higher ideality factor. The increase of $\delta n \approx 0.1$ is consistent with the theoretical increase for a doping level of $5 \times 10^{17}\,\mathrm{cm}^{-3}$.[27]

ELECTRICAL RESULTS AND DISCUSSION: C-V

The depletion capacitance per unit area of an abrupt junction between a metal and a semiconductor is given by[1]

$$C = \sqrt{\frac{q\varepsilon_s N_B}{2}}(V_{bi} \pm V - 2/\beta)^{-\frac{1}{2}}, \tag{3}$$

where ε_s is the permittivity of the silicon substrate, N_B is the silicon dopant concentration, V_{bi} is the built-in potential, and V is the voltage applied to the junction. The built-in potential V_{bi} for a metal to n-type silicon interface is given by the abrupt junction approximation

$$V_{bi} \cong \frac{1}{q} \cdot \left[\phi_B - \frac{\phi_{BG}}{2} + k_B T \ln\left(\frac{N_B}{n_i}\right)\right], \tag{4}$$

where ϕ_{BG} is the silicon band-gap and n_i is the intrinsic (thermal) dopant density. Thus, the barrier height ϕ_B can also be determined from the intercept of a plot of $1/C^2$ against V for $1/C^2 = 0$ at different measurement frequencies taking into account the substrate series resistance.[28]

The $1/C^2$ and conductance G behavior of a p-type silicon-carbon diode is shown in Figure 4 for four different frequencies. The conductance curves (bottom) show no significant frequency dependence and point to a maximum conductance of 80 Scm^{-2}. This corresponds to an AC series resistance of 415 Ω which is of the same order but somewhat lower than the DC resistance of 600 Ω determined from the I–V measurements. This value of the series resistance was used to correct the junction capacitance values.[28]

The $1/C^2$ behavior of, in particular, the 300 kHz curve follows the linear dependence expected for a pure depletion region driven capacitance. There is a small deviation at around −0.3 V due to the influence of interface states, which is discussed later. This strongly suggests that there is no significant insulating layer at the interface since this would result in a leveling off to a fixed $1/C^2$ value in the inversion region determined by the insulating layer capacitance.

The intercepts of the $1/C^2$ curves correspond to voltages of -0.37 ± 0.01 V, as shown in Figure 4 (top). This indicates a built-in voltage of $V_{bi} = 0.42 \pm 0.01$ V and a barrier height of 0.67 ± 0.01 eV using Eqs. (3) and (4) and the substrate doping level of $4 \times 10^{15}\,\mathrm{cm}^{-3}$. Thus, the barrier height determined from the AC C-V and DC I–V measurements are the same, to within the experimental errors.

The deviation of the $1/C^2$ data between −0.4 V and −0.1 V in Figure 4 from a linear behavior indicates the presence of interface states.[28,29] The characteristic relaxation time and density of the interface states can be determined from the frequency dependence of the capacitance in the depletion region.[30] At high frequencies, the states cannot react quickly enough and the capacitance is determined by the substrate dopant level. At low frequencies, the interface states can react and contribute to increase the measured capacitance.

Figure 5 shows the frequency dependence of the capacitance at four different pad voltages in the forward bias regime for the p-type substrate diodes. The additional capacitance per unit area from the interface states C_{SS} can be calculated from[31]

$$C_{SS} = qN_{SS}\frac{\tan^{-1}(\omega\tau)}{\omega\tau}, \tag{5}$$

where N_{SS} is the density of interface states accessable at a particular electrode bias, $\omega = 2\pi f$ is the angular frequncy and τ is the relaxation time of the states. The solid line curves in Figure 5 show fits to the frequency dependent capacitance curves at each pad voltage. The corresponding accessable density of states varies from about $2 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ at 0 V up to $1.2 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ at a bias of −0.25 V. The relaxation time of the states increases from 4 μs to 20 μs in the same voltage range. These values are comparable with those obtained for metal-silicon diodes.[29,30,32]

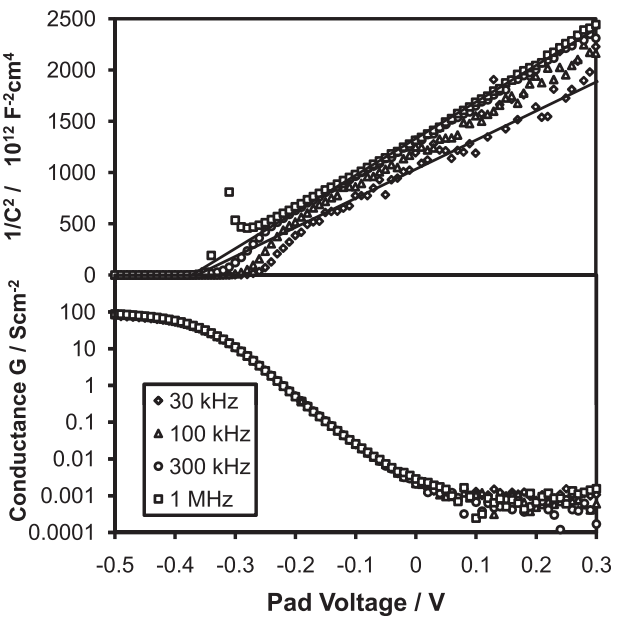

FIG. 4. (Top) $1/C^2$-V characteristics of a carbon p-type silicon diode at 4 different frequencies. (Bottom) conductance behavior of the diode.

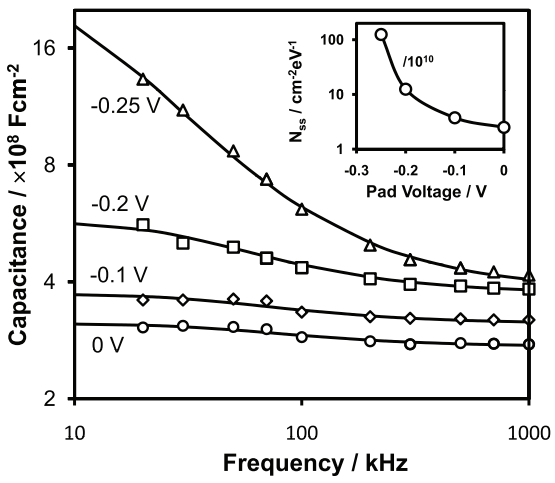

FIG. 5. Frequency dependence of the capacitance of p-type diodes at different pad voltages. The inset shows the extracted density of interface states.

The $1/C^2$ curves for the low doped n-type silicon carbon diodes are shown in Figure 6. The high current densities flowing through the n-type Si-C diodes under forward bias introduces considerable errors in the determination of the capacitance. Therefore, we have confined the measurements to the depletion region in order to extract the barrier height from the $1/C^2$-V characteristics for comparison with the IV behavior. This limitation also means that the density of interface states cannot be determined for the n-type diodes using the current experimental configuration. Further, the measurements for the low doped n-type silicon are limited to the range 200–500 kHz as a result of the low capacitance and the corresponding impact on the noise level at such high current densities.

As can be seen, the capacitance values follow a linear behavior in the intermediate frequency range with the intercept of 0.15 ± 0.01 V. This corresponds to a built-in voltage of $V_{bi} = 0.20 \pm 0.01$ V and a barrier height of 0.46 eV using Eqs. (3) and (4). This barrier height is the same as that determined from the IV measurements.

The intercept of the $1/C^2$-V curves for the $5 \times 10^{17}\,\mathrm{cm}^{-3}$ doped silicon diodes is 0.22 ± 0.02 V as shown in Figure 7. This indicates a built-in voltage of $V_{bi} = 0.27 \pm 0.02$ V and a barrier height of 0.40 ± 0.02 eV taking into account the higher substrate doping. As for the other two cases, the barrier determined from the CV measurements is the same to within experimental error as extracted from the IV measurements.

The barrier heights of $\phi_{Bn} = 0.46$ eV and $\phi_{Bp} = 0.66$ eV are consistent with the silicon band-gap of $\phi_{BG} = 1.12$ eV at room temperature. This implies that the low temperature deposition process at 860 °C does not form silicon carbide interfaces of considerable thickness. Further, these values indicate an effective work-function for the carbon electrode of 4.49 ± 0.01 eV assuming a silicon valence band edge energy of 5.15 eV.[33] This is the same, to within experimental error, as the work-function for highly oriented pyrolytic graphite (HOPG) of 4.48 eV (Ref. 34) and consistent with the Fowler-Nordheim barrier difference of about 0.4 eV determined for carbon electrode metal insulator semiconductor (MIS) capacitors.[25] These results together suggest that the carbon-silicon junction is determined by the work-function difference and is not pinned by (metal) electrode induced gap states.

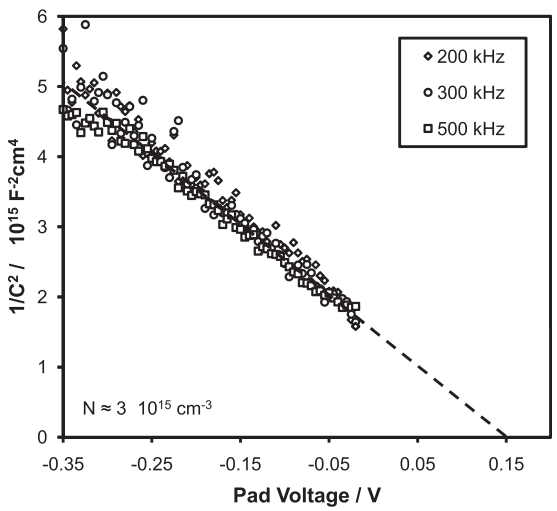

FIG. 6. The measured $1/C^2$-V characteristics of carbon n-type silicon diodes with a doping level of $3 \times 10^{15}\,\mathrm{cm}^{-3}$. The intercept is 0.15 V for all three frequencies.

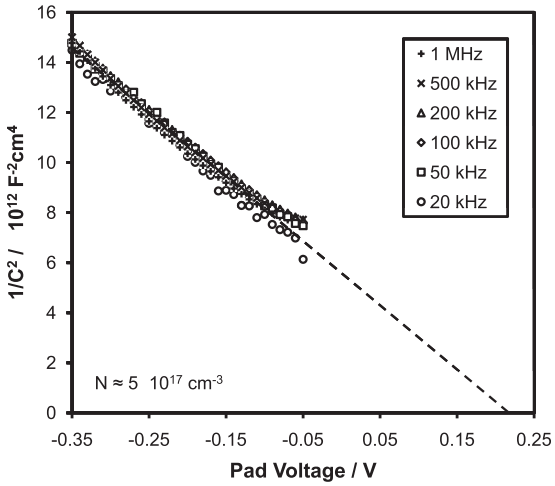

FIG. 7. The measured $1/C^2$-V characteristics of carbon n-type silicon diodes with a doping level of $5 \times 10^{17}\,\mathrm{cm}^{-3}$. The extrapolated intercept is 0.22 V.

CONCLUSIONS

In the present work, we have provided evidence that pyrolytic carbon deposited at 860 °C can be used as an electrode material for Schottky diode applications on silicon. Barrier heights of 0.66 eV and 0.46 eV were determined for low doped p-type and n-type substrates, respectively, and 0.41 eV for an n-substrate with two orders of magnitude higher doping. The diode ideality factors of around 1.2 are somewhat higher than for optimized commercial devices, but well within the range for simple structures with poorly defined boundaries.

Further, the capacitance-voltage measurements suggest that the carbon-silicon junctions do not have an insulating interface layer but an interface state density of about $10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. This is comparable with the values found for metal-semiconductor diodes. The interface states do not appear to pin the semiconductor Fermi energy, as indicated by the similarity of the carbon work-function determined from the IV and CV presented here and that of HOPG. Importantly, previous work has shown that the carbon deposition process and material are compatible with conventional semiconductor processing making carbon electrodes attractive for high stability and high temperature devices.[14]

ACKNOWLEDGMENTS

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