Progress with Defect Engineering in Silicon Heterojunction Solar Cells

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((Optional Dedication))

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Abstract:

((Abstract text. 12 point, double-spaced. Maximum length 200 words. Written in the present tense.))

Due to the constraint of low temperature processing in silicon heterojunction (SHJ) solar cells, no defect engineering to improve silicon wafer quality is typically incorporated during cell fabrication. This means that high quality n-type Cz wafers are required to produce high efficiency cells. In this review, we survey recent demonstrations of incorporating defect engineering approaches, such as gettering and hydrogenation, into the SHJ process flow for both n-type and p-type wafers. Defect engineering on wafers before cell fabrication can significantly improve the quality of low-lifetime p-type wafers (implied open-circuit voltage (iV_{OC}) increase of > 70 mV), making them much more suitable for SHJ cells. Interestingly, these same approaches are also very effective in improving the cell performance in the n-type wafers that are conventionally used in industry. Post-cell illuminated

annealing processes have been shown to eliminate boron-oxygen LID in p-type wafers, leading to stable V_{OC} exceeding 735 mV. New results indicate that the hydrogen naturally incorporated during SHJ processing is sufficient to passivate these defects. Similar illuminated annealing processes also lead to substantial improvements (of up to 0.7%$_{abs}$ efficiency gain) in n-type SHJ cells. With these findings considered, we demonstrate that a modified SHJ process flow, which includes defect engineering on a wafer level and post-cell hydrogen passivation, is beneficial for SHJ production, regardless of the wafer type.

1. Introduction

Silicon heterojunction (SHJ) solar cells are formed by the deposition of stacks of intrinsic and doped hydrogenated amorphous silicon layers (a-Si:H) on the surface of crystalline silicon (c-Si) wafers [1][2][3]. The doped a-Si:H layers determine the carrier selectivity of each contact, which defines the direction of current flow, and the intrinsic a-Si:H layers, which are deposited directly onto the crystalline silicon (c-Si) surface, provide excellent surface passivation [4][5]. The cells are completed by the deposition of a transparent conducting oxide (TCO) to aid lateral conduction and the formation of metal contacts, typically by screen printing of silver [6][7][8]. This technology was pioneered in the 1990s by Japanese company Sanyo [9][10][11]. The solar PV market is currently dominated by the passivated emitter and rear cell (PERC) design [12][13]. Compared to PERC, SHJ solar cells have multiple advantages. They have demonstrated higher open circuit voltages (V_{OC}), with V_{OC} values as high as 750 mV [9]. The high V_{OC} is related to the excellent surface passivation provided by the a-Si:H layers. The world record 1-sun efficiency of 26.7% for a single junction silicon solar cell was achieved using this approach [14], and cells with efficiency exceeding 25% have been fabricated in an industrial environment [15]. Another advantage of SHJ cells, which is linked to the high V_{OC}, is the lower temperature coefficient, meaning that power losses in SHJ cells operated at elevated temperatures are lower than other silicon-based technologies [16][2]. Therefore, under realistic cell operation conditions in the field, the actual power output of a SHJ module will be higher than that of a PERC module, even if they have the same power rating at room temperature. Additionally, the expected rise of tandem solar cells with silicon as the bottom cell has also increased interest in the SHJ technology, as it is well-suited as the bottom cell in a tandem device [17][18][19][20][21][22]. These advantages mean that industry is seriously looking into SHJ solar cells as a technology to compete with PERC in the future. The ITRPV 11th edition indicates that the market share for SHJ cells is expected to increase to 15% over the next ten years [23], which will represent a significant volume as we move towards terawatt-scale photovoltaics [24].

One unique aspect of SHJ cells is that all processing occurs in a low temperature regime, typically < 250 °C[4][16][25]. This is very different to most other cell architectures, such as Al-BSF, PERC, n-PERT and TOPCon, which all require high temperature thermal diffusions for junction formation and firing processes for metallization [13][26]. This temperature constraint in SHJ cells is related to the sensitivity of the a-Si:H passivation, whereby processing at elevated temperatures causes a deterioration of the surface passivation, which substantially reduces the efficiency [27][28]. The lack of high temperature processing can avoid the possibility of significantly reducing the bulk lifetime, which can occur in low quality silicon wafers [10].

The high temperature processes in the process flow of structures such as PERC also serve a secondary purpose, they provide defect engineering as a way to improve the quality of the silicon wafer [29]. These defect engineering approaches primarily come in two forms: gettering and hydrogenation [30]. The first is related to the thermal diffusion process. During the high temperature diffusion process, a very heavily doped region is formed at the surface. Mobile impurities in the bulk of the silicon are accumulated in this region, which is subsequently etched away. One common example of the use of gettering is the removal of interstitial iron from p-type silicon wafers during the phosphorus diffusion in PERC and Al-BSF solar cells [31][32]. This can cause the concentration of interstitial iron in the bulk to reduce by more than two orders of magnitude [29]. An additional impact of gettering, which is performed at temperatures of > 800 °C, is the impact of the thermal profile on the wafer. High temperature processing has been shown to anneal thermal donors in silicon [33]. However, the high temperature process can also, in some cases, lead to the activation of grown-in defects, such as oxygen precipitates, which can severely reduce the lifetime [34]. Thus, as the thermal load can modulate the material to either increase or decrease lifetime, it is very important to understand the interplay between these effects. The second defect engineering approach is hydrogen passivation of impurity-related and crystallographic defects in the bulk. Hydrogen is introduced into the silicon bulk via hydrogen-containing dielectrics. The application of

plasma enhanced chemical vapour deposition (PECVD) to deposit these layers, in particular hydrogenated silicon nitride (SiN_X:H) as a passivation layer and anti-reflection coating in PERC solar cells, has allowed for the incorporation of a large amount of atomic hydrogen into the cell. During the high temperature contact firing, hydrogen from these layers can diffuse from the dielectric layers into the bulk, where it can become available to passivate a range of defects. A subsequent low temperature hydrogen passivation process can then be used to passivate boron-oxygen defects, thereby eliminating light-induced degradation, one of the key arguments in heading to the use of n-type wafers and the SHJ technology [35][1][11]. Figure 1 shows a comparison of the process flow for SHJ and PERC solar cells, highlighting the natural incorporation of defect engineering in the PERC process flow.

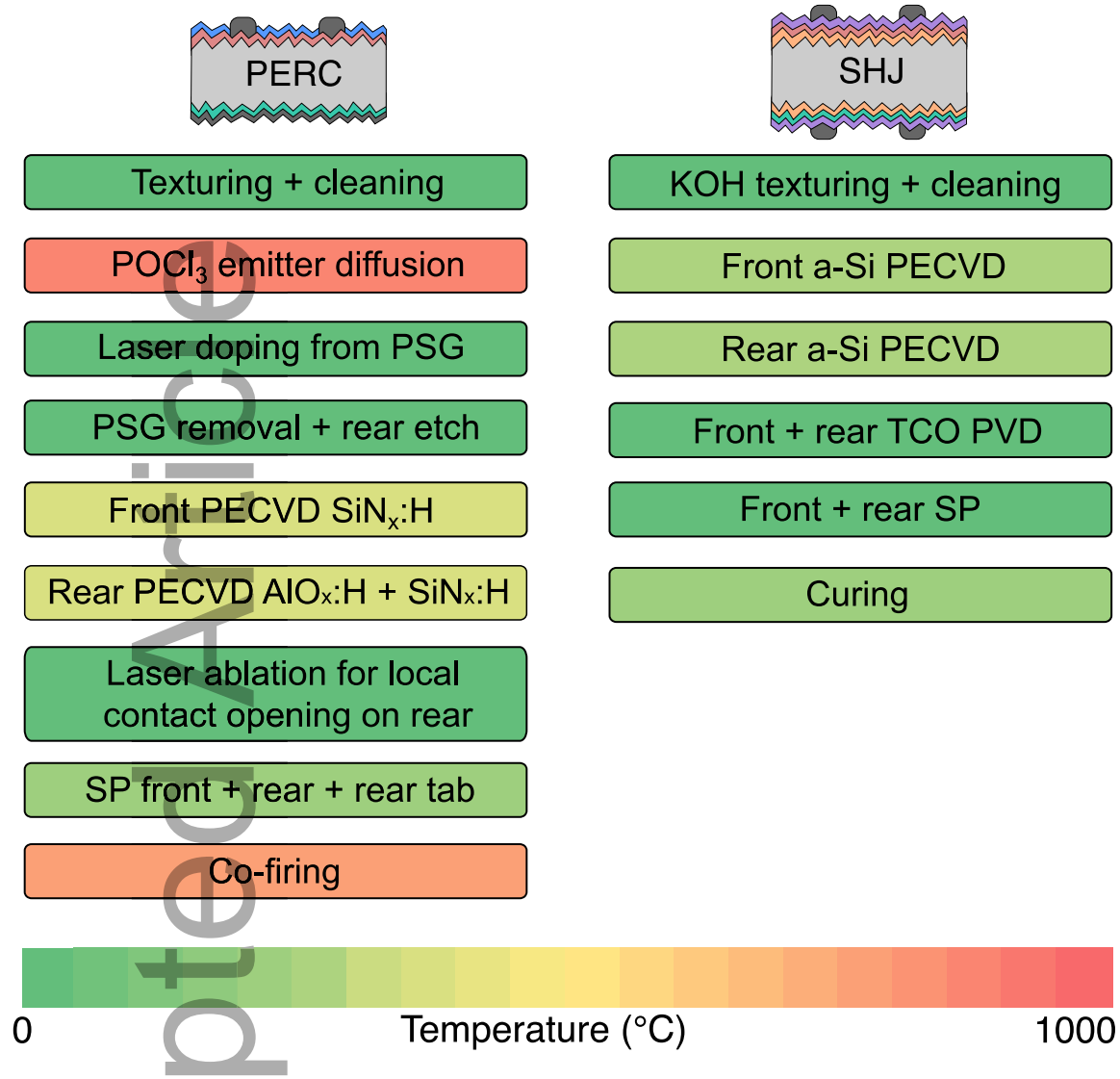

Figure 1. Comparison of process flow for PERC (left) and SHJ cells (right). The colour bar indicates the temperature of each process.

The fact that there is no provision for defect engineering in SHJ process flow means that to achieve a high efficiency cell, high quality n-type Cz wafers are required. LONGi estimates that the cost differential for n-type Cz wafers, compared to p-type Cz wafers used in PERC cells, is 10% [36]. This requirement for using expensive wafers adds an additional cost for SHJ cell manufacturers. It would therefore be ideal to incorporate defect engineering approaches into SHJ fabrication, to allow for the use of cheaper silicon wafers. Chang *et al.* performed a cost analysis using a Monte Carlo approach, which showed that it would be cost competitive to switch to cheaper p-type Cz wafers if

the cell efficiency could be kept within 0.4 – 0.5%$_{abs}$ of n-type Cz wafers [37]. This cost analysis was performed assuming a median wafer premium of 8% for n-type Cz wafers. According to LONGi, this has since increased to 10%, which may make the comparison even more favourable for p-type SHJ cells. Recent results from Descoeudres *et al.* indicate that the average efficiency for p-type SHJ cell can be comparable to that of n-type if a phosphorous diffusion gettering defect engineering approach is incorporated [38].

Over the past four years, the area of defect engineering in SHJ solar cells has been gaining research attention. The purpose of this manuscript is to survey the existing demonstrations of defect engineering for SHJ solar cells, as well as to present new results demonstrating the impact in industrial solar cells, and to provide direction for future research in this area. In particular, the review addresses three key research areas: i) pre-fabrication defect engineering on n-type and p-type wafers for SHJ cells; ii) post-cell illuminated annealing to improve n-type SHJ cells; and iii) hydrogen passivation of boron-oxygen light-induced degradation for p-type SHJ cells. By closely surveying existing literature, it becomes clear that defect engineering processes are not only beneficial to improve the properties of cheaper, low quality wafers, but that they can also be very beneficial for cells made using high lifetime n-type Cz wafers. As such, we believe that the defect engineering approaches outlined in this review should be considered more closely for industrial SHJ cells.

2. Defect Engineering Approaches

2.1. Defect Engineering on a Wafer Level

In order to facilitate the use of lower quality silicon wafers in SHJ solar cells, defect engineering approaches may be applied to the wafer prior to cell fabrication. This pre-fabrication defect engineering primarily consists of two approaches. The first is gettering, which leads to the removal of unwanted impurities in the bulk, namely mobile transition metals that are incorporated during wafer formation. In p-type silicon wafers, a significant metal of concern is iron [39],[40],[41],[42]. Gettering relies on the movement of highly mobile impurities towards heavily diffused sites at the surface, which are subsequently etched away. The second approach is hydrogenation, where hydrogen is introduced into the silicon bulk so that it may passivate a range of crystallographic or impurity-related defects.

Hallam *et al*. demonstrated the effectiveness of such pre-fabrication defect engineering approaches on commercial grade p-type Cz silicon wafers [43]. Due to the inherent defect engineering approaches integrated into the PERC process flow, the lifetime requirements on p-type Cz used for this technology are far less strict, commercial grade p-type Cz wafers can have lifetimes as low as ~20 µs. Even with such low-lifetime starting materials, efficiencies of > 23% and V_{OC} of almost 690 mV is achieved for PERC solar cells, as the material quality is improved due to the inherent defect engineering. In their report, Hallam *et al*. perform gettering and hydrogenation treatments on low-lifetime commercial grade p-type Cz wafers prior to SHJ cell fabrication. The study contained four different groups: i) Control (no defect engineering treatment); ii) H (hydrogenation treatment only); iii) G (gettering treatment only); and iv) G + H (both gettering and hydrogenation treatment). Gettering was performed by the application of a heavy n+ phosphorous emitter diffusion (35 Ω/□), with subsequent HF dip and alkaline texturing to remove the PSG layer and the diffused

emitter layer. For hydrogenation, the hydrogen was introduced via the deposition of a hydrogen rich silicon nitride film (SiN_X:H), deposited by plasma-enhanced chemical vapour deposition (PECVD). The wafers were then fired in a fast-firing furnace at 740 ± 6 °C to facilitate the release of hydrogen from the dielectric layer into the bulk of the silicon. The SiN_X:H films were then removed prior to SHJ cell fabrication. Following SiN_X:H removal, lifetime test structures were formed by the deposition of both intrinsic and doped a-Si:H films to form cell precursors.

The defect engineering approaches had a profound impact on the lifetime of the wafers. Figure 2 shows the effective lifetime (extracted at an injection level of 1×10^{15} cm^{-3}) and the 1-sun implied V_{OC} for wafers from the four groups. The control samples, which did not receive any treatments, had an effective lifetime of ~ 25 µs. This is significantly lower than the multi millisecond n-type Cz wafers typically used in the commercial production of SHJ solar cells. The application of the G or H treatments resulted in average lifetimes of 50 µs or 75 – 100 µs, respectively. The most significant improvement was observed for the G + H group, which demonstrated effective lifetimes of ~ 125 µs. This represents a 5-fold increase compared to the control. For all samples, the a-Si:H passivation led to J_0 values < 5 fA/cm^2, indicating that the changes in effective lifetime were related to changes in the bulk. Figure 2 also displays the 1-sun implied V_{OC} (iV_{OC}) of the wafers, which displays an identical trend. The average iV_{OC} increased from 615 mV for the control, to 689 mV for the G + H group, an improvement of more than 70 mV.

Another group of samples from the same wafer set were then fabricated into full p-type SHJ cells by the subsequent deposition of the TCO and low temperature silver screen printing. In control cells, fabricated using wafers that did not receive any defect engineering approaches, the V_{OC} was 621 mV. This is significantly lower than industrial PERC cells and is even lower Al-BSF solar cells, which exhibit V_{OC} of ~ 640 mV in industrial cells. This highlights the incompatibility with low

lifetime commercial grade p-type Cz wafers and the SHJ technology. The observed improvements in lifetime for the defect engineered wafers translated into the cell voltages. V_{OC} values of 628 mV and 643 mV were recorded for the H and G groups, respectively. Remarkably, the V_{OC} of the G + H group was 692 mV, which represents an increase of > 70 mV compared to the control. This significantly higher value for the G + H group highlights the complementary nature of gettering and hydrogenation. Additionally, the J_{SC} in the defect engineered cells was higher than the control. EQE measurements (not shown here) showed that the gettering and hydrogenation improved the long wavelength response, indicative of improvements in the bulk minority carrier lifetime.

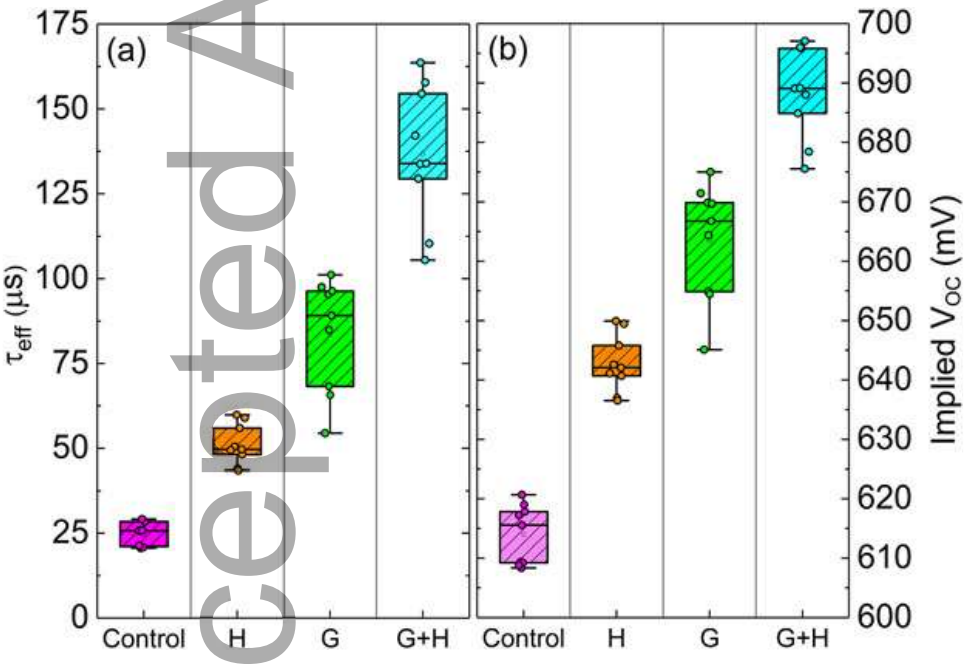

Figure 2. Impact of hydrogenation and gettering defect engineering approaches on (left) effective minority carrier lifetime (extracted at 1×10^{15} cm^{-3}) and (right) 1-sun implied open circuit voltage (iV_{OC}) for commercial grade p-type Cz wafers. Four groups are displayed, wafers that did not receive any pre-fabrication defect engineering (control), hydrogenated samples (H), gettered samples (G) and samples what underwent both gettering and hydrogenation (G+H). Reproduced with permission [43].

A similar methodology was adopted by Chen *et al*., who investigated the effectiveness of defect engineering approaches to improve the performance of both p-type Cz and high performance multi wafers [44]. In monocrystalline samples, the application of a phosphorous diffusion gettering led to a significant reduction in the interstitial iron concentration [Fe_i]. The [Fe_i] reduced by almost two orders of magnitude, from 3×10^{11} cm^{-3} to 5×10^{9} cm^{-3}. The application of the G + H approach led to an increase in iV_{OC} from 620 mV to 687 mV, which closely matches the observation of Hallam *et al*. Matching samples were again fabricated into SHJ cells. This improvement in the G + H group translated to an impressive V_{OC} of 693 mV in a SHJ device, however, after the application of an advanced hydrogenation process (AHP) following cell fabrication, the V_{OC} increased to as high as 707 mV. This indicates that the defect engineering used was able to increase the V_{OC} by > 80 mV, compared with the control cell. This V_{OC} exceeds that of the 25% world record PERL cell, which used hydrogen passivation of the surfaces to improve the V_{OC} by ~ 100 mV [45][46]. The application of these types of post-cell AHP approaches is discussed in the following section.

The same defect engineering approaches were applied to p-type high performance multi-crystalline (mc-Si) silicon wafers. mc-Si wafers have an inherently higher concentration of metallic impurities and have a higher density of crystallographic and structural defects. Thus, the use of defect engineering in these wafers is more crucial. Figure 3 shows calibrated iV_{OC} maps for mc-Si wafers in each of the four groups. The spatially averaged iV_{OC} in the control sample was 615 mV, the lifetime for this case is limited by the large amount of crystallographic defects and the presence of saw damage. The sample in the H group, which received only a hydrogenation treatment, displayed improved material quality, with an iV_{OC} of 625 mV. For this case, the change is largely observed in intra grain regions, while the grain boundaries remain highly defective. A similar behaviour is seen for the G sample, the gettering improves the intra grain regions. The most significant improvement

is seen for the G + H group, for which passivation occurs in both the intra-grain regions and at the grain boundaries. The corresponding iV_{OC} is ~ 700 mV, an increase of > 80 mV compared to the control. When fabricated into SHJ cells, the highest achieved V_{OC} was 702 mV. This is the highest reported V_{OC} for either n-type or p-type mc-Si, surpassing the previous value by approximately 30 mV [47]. This demonstrates the effectiveness of defect engineering approaches for improving the prospects of using cheaper wafer sources to form SHJ solar cells.

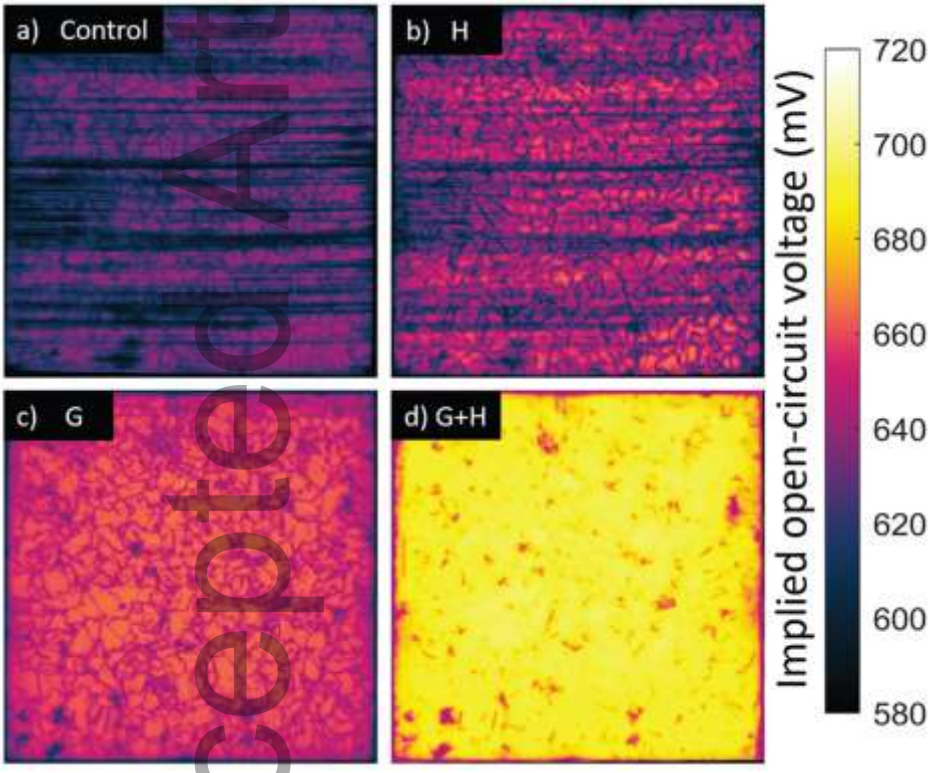

Figure 3. Calibrated 1-sun implied V_{OC} maps for p-type mc-Si samples with symmetrical SiNx:H passivation layers. Four groups are displayed, a) wafers that did not receive any pre-fabrication defect engineering (control), b) hydrogenated samples (H), c) gettered samples (G) and d) samples what underwent both gettering and hydrogenation (G+H). Reproduced with permission [44].

Author	Year	Material	Area [cm²]	Pre-fabrication wafer-treatment	Efficiency [%]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm²]	Reference
Park et al.	2012	n-type Cz-Si	1	-	11.9	577	73.9	27.8	[48]
				Gettering	13.4	598	75.3	29.8	
Jay et al.	2014	n-type QM-Si	156	Gettering	21.6	732	77.9	38.3	[49]
Basnet et al.	2018	n-type UMG Cz-Si	4	Gettering	21.2	715	78.0	37.0	[50]
Haschke et al.	2018	n-type QM-Si	4	Gettering	21.5	700	78.0	39.0	[51]
Chen et al.	2018	p-type Cz-Si	4	-	14.2	621	68.9	33.3	[44]
				Gettering + hydrogenation	16.6	693	69.6	34.5	
		p-type mc-Si	4	-	12.3	632	61.1	31.9	
				Gettering + hydrogenation	14.5	657	68.6	32.1	
Basnet et al.	2019	n-type UMG Cz-Si	4	-	18.0	678	73.4	36.2	[52]
				Tabula rasa + gettering	21.0	717	78.0	37.5	
				Gettering + hydrogenation	21.2	715	78.1	38.6	
		n-type Cz-Si	4	-	21.2	708	76.7	39.0q	
				Tabula rasa + gettering	22.4	720	78.4	39.8	
				Gettering + hydrogenation	22.7	721	79.2	39.6	
Kivambe et al.	2019	p-type QM-Si	4	Gettering	22.2	723	77.6	39.4	[35]
		n-type QM-Si	4	Gettering	22.6	725	79.1	39.4	
Descoeudres et al.	2020	p-type Cz-Si	244	-	22.6 ± 0.1	742.3 ± 1.5	79.2 ± 0.4	38.5 ± 0.1	[38]
			244	Gettering	22.8 ± 0.2	742.9 ± 2.0	79.9 ± 0.5	38.4 ± 0.1	
		n-type Cz-Si	244	-	22.78	738.3	80	38.6	
Vicari Stefani et al.	2020	p-type Cz-Si	244	Gettering	21.6 ± 0.1	735.4 ± 0.9	73.8 ± 0.3	39.7 ± 0	[53]
			244	Gettering + hydrogenation	21.2 ± 0.1	731.1 ± 1.4	73.1 ± 0.2	39.5 ± 0	
This work	2021	n-type Cz-Si	243.4	-	22.3 ± 0.2	735 ± 1.4	79.4 ± 1.0	38.1 ± 0.2	-
				Gettering	22.8 ± 0.1	737.5 ± 0.7	80.2 ± 0	38.6 ± 0.1	

Table 1. Overview of works describing pre-fabrication defect engineering on wafers in silicon heterojunction solar cells

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Upgraded metallurgical grade (UMG) silicon is substantially cheaper than the electronic grade silicon that is commonly used by industry. Compared to electronic grade silicon, UMG silicon does not go through a purification step in a Siemens reactor, which is the reason for the lower cost. However, the liquid phase purification process means that a higher concentration of both metallic and non-metallic impurities remain in the silicon, which would have otherwise been removed by the Siemens process. Vicari Stefani *et al.* presented a study on defect engineering in p-type UMG mc-Si wafers from the edge of the silicon cast [54]. These wafers, referred to as 'red zone' wafers, contain severe impurity contamination at the edges due to impurities that diffused from the crucible wall during crystallisation. Defect engineering approaches led to significant increases in the effective lifetime, which increased from 9 µs for the control to 39 µs in the G + H group. This was correlated with an order of magnitude reduction in $[Fe_i]$ concentration.

One of the interesting aspects of these red zone wafers is the significant variability in the quality across the wafer. It is expected that the red zone regions at the edge of the wafer contain significantly higher impurity concentrations and would thus benefit more from defect engineering. In order to illustrate the spatial non-uniformity of the influence of different defect engineering approaches, changes in PL counts on an inverse scale were compared. It was assumed that the PL counts were proportional to the effective lifetime and thus, an increase in PL counts is indicative of a reduction in relative defect density. In this way, a map of change in the relative defect density was produced by comparing the difference in inverse PL counts before / after the defect engineering.

Figure 4 a) shows the impact of the hydrogenation only treatment. This indicates that the most substantial improvement occurs at the wafer edge in the 'red zone'. However, there are some regions in the map at the interface of the red zone that are dark, which correlate with an increase in recombination activity, or reduction in lifetime. This implies that the hydrogenation treatment makes the material quality worse in some parts. Figure 4 b) shows the impact of the gettering only treatment. This shows that the red zone region is substantially improved, and there is much less reduction in lifetime at the interface regions compared to the hydrogenation treatment. However, there are significant portions in the intra grain regions that are negatively impacted by the gettering. Figure 4 c) shows the impact of the combined gettering and hydrogenation treatment. This highlights the significantly larger improvement in the edge red zone region; however, the combination of the two defect engineering approaches removes any areas where the lifetime is reduced. This highlights the important complementary nature of gettering and hydrogenation.

When fabricated into a full SHJ solar cell, one sample from the G + H group exhibited a V_{OC} of 691 mV. This V_{OC}, achieved using a wafer with a starting bulk lifetime of < 15 µs, is comparable to modern industrial p-type Cz PERC cells and is believed to be the highest for this p-type UMG mc-Si material.

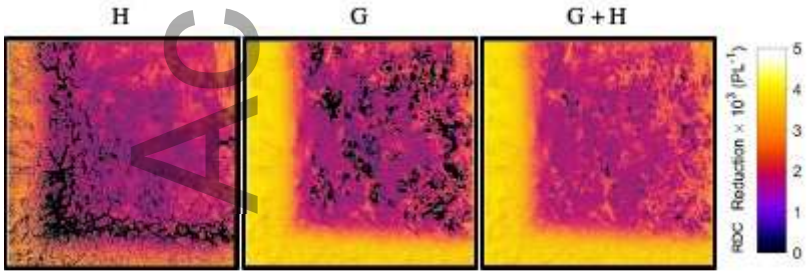

Figure 4. Inverse PL maps for UMG p-type mc-Si samples that underwent a) hydrogenation only (H), b) gettering only (G) and c) both gettering and hydrogenation (G+H). Each image displays the difference in inverse PL counts between that sample and the control sample,

which did not undergo any defect engineering process. Thus, each image represents the changes in inverse PL counts for that treatment. Changes in the PL counts are indicative of changes in the relative defect concentration, where bright regions on the map represent larger reductions in the relative defect concentration. Reproduced with permission [54].

Kivambe *et al.* demonstrated high efficiencies in both p-type and n-type cast mono wafers using a defect engineering approach prior to SHJ cell fabrication [35]. Cast mono or quasi mono wafers are formed via the solidification of molten silicon in a crucible with a partially melted silicon seed crystal. This approach produces wafers that are higher quality than standard multi-crystalline wafers formed via casting and has cost benefits compared to the conventional Cz growth process. When developed by BP Solar, it appeared this wafer growth technique would revolutionise the industry, however, significant dislocation clusters that form at the edges of the crucible reduce the material quality compared to mono Cz wafers formed using the Cz technique [55]. As such, these wafers are highly suitable for defect engineering approaches to improve wafer quality. Kivambe *et al.* investigated the diffusion temperature profile on the impact of phosphorous diffusion gettering on both p-type and n-type cast mono wafers. Figure 5 shows the effective lifetime of cast mono wafers for three different gettering diffusion profiles, i) peak temperature of 811 °C, ii) peak temperature of 900 °C and iii) peak temperature of 900 °C with slow temperature ramp down. The gettering process improves the lifetime for both p-type and n-type wafers. In p-type cast mono wafers, the largest improvement in lifetime is observed for the lower temperature gettering step. Interestingly, the opposite effect is seen in n-type wafers, where the higher temperature process leads to significantly larger improvements compared to the lower temperature gettering. A previous report has shown that the lifetime of p-type and n-type silicon behaves differently depending on the size of metallic precipitates [56]. In n-type silicon, it is more detrimental to have a smaller precipitate density, or larger precipitate size, whereas the reverse is true in p-type

silicon. As the temperature of the diffusion process modulates the density and size of metallic impurities, this is provided as an explanation for the very different response to the gettering step for p-type and n-type wafers. Gettered wafers using the optimal conditions where then fabricated into small area SHJ cells. A certified efficiency of 22.58% and 22.15% was achieved for n-type and p-type cast mono wafers, respectively. Control samples without defect engineering all displayed efficiencies of less than 20%. A summary of the efficiency data is shown in Table 1. The efficiency for the n-type cast mono is believed to be the highest efficiency for this material class. These results are promising; however, they highlight a very important point, both p-type and n-type wafers benefit from pre-fabrication defect engineering. However, the processing conditions required for optimal performance is not necessarily the same for both wafer types.

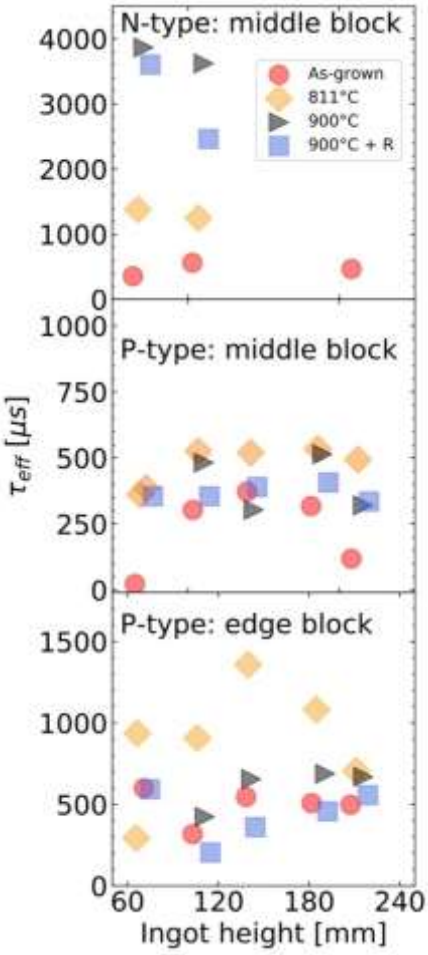

Figure 5. Effective minority carrier lifetime (extracted at 1×10^{15} cm^{-3}) of p-type and n-type cast mono wafers from different ingot cast positions, plotted as a function of ingot height. The scale for the vertical axis for p-type and n-type wafers is different. Reproduced with permission [35]. Copyright 2019, American Chemical Society.

The previously described reports demonstrated high V_{OC} on a variety of lower cost p-type substrates, however, the FF was significantly lower than for industrial n-type cells, and thus the efficiency was not comparable. In 2019, Descoeudres *et al*. demonstrated that high efficiency devices are achievable using p-type Cz substrates [38]. In their report, they investigate the impact of a gettering step on the performance of full area p-type Cz SHJ solar cells. The gettering on p-type Cz wafers was performed by a $POCl_3$ diffusion step with furnace temperature ranging from 810 °C – 900 °C. Following this, the PSG layer and n+ emitter were removed via a HF dip and alkaline texturing step, respectively. Prior to cell fabrication, lifetime test structures with *i-n* / *i-p* a-Si:H stacks were fabricated on both n-type and p-type Cz wafers, as well as a n-type FZ wafer. The gettering process impacted the lifetime of the p-type wafers. In control wafers that did not receive gettering, the lifetime varied significantly as a function of ingot position. The effective lifetime, extracted at a minority carrier density of 5×10^{14} cm^{-3}, reduced from ~ 9 ms at the top of the ingot to ~ 4 ms at the tail end of the ingot. Wafers that underwent gettering were much less sensitive to ingot position. It is thought that higher lifetimes achieved at the tail end of the gettered ingot was due to a suppression of metallic impurity defects in the bulk. Additionally, the high temperature gettering process also significantly alters the resistivity (reduces resistivity). This is thought to be related to the annihilation or de-activation of thermal donors. Very impressive lifetimes were observed on the p-type wafer. A highest effective lifetime (extracted at 5×10^{14} cm^{-3}) of 10.1 ms was observed on the gettered p-type Cz wafer, compared to 11.4 ms on the n-type Cz wafer. This indicates that the high lifetimes required to fabricate high efficiency

SHJ cells are not exclusively achievable with n-type wafers. Although, it is noted that these lifetimes are not directly comparable as the resistivity on the p-type wafer was higher (6 Ω·cm compared to 2.2 Ω·cm) and it was slightly thinner due to the additional etching step from the gettering. Another interesting point when comparing the effective minority carrier lifetime in n-type and p-type wafers is the difference in the mobility of carriers. The minority carriers in p-type silicon are electrons, which have a higher mobility than holes by approximately a factor of three. This higher mobility of minority carriers implies that the lifetime requirements for a p-type wafer will be relaxed when compared to n-type, further complicating the lifetime requirements for each wafer type. Finally, standard n-type SHJ solar cells are formed with the n+ doped a-Si layer at the front and the p+ doped a-Si layer at the rear, meaning they are rear junction cells. For p-type, the same architecture is used, meaning that the junction is at the front. This changes the current flow pattern and thus may modify the lifetime requirement to reach the same efficiency. No optimisation to account for this in p-type SHJ cells was reported in this work, however, it was noted that this may be important for the future. Regardless, it is a very promising result as the processing approach for the p-type was not modified from the standard n-type samples. This highlights the versatility of the SHJ fabrication approach, high efficiency cells can be fabricated on either n-type or p-type substrates with no modification of the processing sequence. Also, interestingly, no significant reduction in lifetime at low injection was observed on the p-type wafer. In previous reports, the lower FF in p-type devices was attributed to the low lifetime at low injection on p-type.

Full area (244 cm^2), front and back contacted p-type SHJ solar cells were fabricated using p-type Cz wafers that were gettered prior to cell fabrication using a variety of $POCl_3$ diffusion recipes. The structure of the cells in this study closely resembles that of a fully industrial SHJ solar cell. The impact of three different $POCl_3$ diffusion steps were explored, with peak temperature of 810 °C, 840 °C and 900 °C. As a reference, the efficiency results of the p-type gettered samples were compared with a batch of SHJ cells fabricated using n-type Cz wafers

using identical cell processing conditions. A summary of the efficiency data is displayed in Table 1. Compared to the n-type cell efficiency, the non-gettered p-type cells are ~ 0.2%$_{abs}$ lower. This is caused primarily by the lower FF in p-type cells. Interestingly, the V_{OC} in the p-type cells is actually slightly higher than the n-type reference. After the gettering step, the average efficiency of the p-type cells increases to a level that is comparable with the n-type reference. This is a very promising result as the cell processing here closely resembles that of an industrial cell, it is not just a study of a small area laboratory cell. Globally, the gettering tends to increase the performance of p-type Cz SHJ cells by ~ 0.2%$_{abs}$. This is related to an increase in the FF after the gettering step, which is more pronounced for higher gettering diffusion temperatures, however, the impact of temperature is marginal. The gettering process was shown to improve the effective lifetime of the p-type wafers, particularly for wafers from the tail end of the ingot where the concentration of impurities is expected to be highest. As the surface recombination velocity (SRV) is expected to be very low and the passivation scheme for all samples was identically processed, it is expected that changes in the lifetime are caused by improvements in the bulk. Further detailed studies on the impact of the gettering are required to pinpoint the exact cause of the improvements.

To delve deeper into the efficiency potential of p-type SHJ cells, monofacial cells were prepared on both p-type and n-type substrates. An efficiency as high as 23.6% was achieved on full area monofacial SHJ cells with p-type Cz wafers. This is the first demonstration of a p-type SHJ cell with such high efficiency and, in particular, with such high FFs (exceeding 80%). A small area device (4 cm^2) fabricated using a p-type float zone wafer achieved a remarkable certified efficiency of 23.76%. These results present a very positive case for the future development of p-type SHJ solar cells. One key aspect missing from this report is the stability of the p-type SHJ cells compared to n-type. This is addressed in section 2.3.

In an industrial setting, SHJ cell manufacturers exclusively use n-type Cz wafers. This is because they have inherently higher lifetimes and do not suffer from light induced degradation related to boron-oxygen defects. It is well known that p-type silicon is more susceptible to increased bulk recombination caused by the presence of transition metals such as interstitial iron [41][40]. However, n-type wafers are not immune to bulk defects. In addition, n-type Cz wafers can also suffer from light-induced degradation, as reported by Letty *et al*. for seed-end wafers [57]. N-type Cz wafers are also susceptible to reductions in lifetime due to thermal donors [58]. Thermal donors are recombination-active defects thought to be formed via the aggregation of silicon and interstitial oxygen atoms [59][60]. The formation of thermal donors varies as a function of thermal history, with peak formation rates reported to occur at ~ 470 °C [61], although, a wide window of temperatures can lead to the formation of these defects. The formation of thermal donors in n-type wafers can have a significant negative impact on efficiency. For example, the formation of thermal donors with a concentration of 1×10^{15} cm^{-3} (which is feasible in industrial n-type Cz ingots) can lead to a reduction in the efficiency of SHJ solar cells by $1\%_{abs}$ [62][63]. It was shown in the 1980s that annealing the wafers at temperatures > 600 °C can annihilate the thermal donors [33]. As such, the efficiency of Al-BSF, PERC and TOPCon solar cells, which all incorporate high temperature processes, are not significantly impacted by thermal donors. However, the low temperature processing regime in SHJ solar cells means there is no possible annihilation / de-activation of thermal donors during cell fabrication, meaning they can have a greater impact on cell efficiency in this architecture.

Therefore, it is feasible that the defect engineering approaches described above to improve the performance of p-type wafers are also applicable to the industry standard n-type wafers. Generally, a cut off for lifetime for solar cell manufacturers using n-type Cz wafers given to wafer producers is 1 ms [64]. However, simulations performed by Steinkemper *et al* [65], indicated that for a 1 Ω·cm n-type wafers with a 1 ms lifetime, the efficiency may be impacted by as much as 1% absolute (4.2% relative for a 24% efficient SHJ solar cell), highlighting a significant scope for improving the efficiency of SHJ solar cells fabricated even on high lifetime n-type wafers through defect engineering.

Basnet *et al*. investigated the impact of defect engineering approaches on the performance of n-type UMG Cz wafers [52]. These wafers have a higher density of contaminants, both metallic (e.g. Fe, Cu, Cr) and non-metallic (e.g. O and C), compared with the electronic grade silicon feedstocks currently used in industry. As such, the lifetime is more affected by grown-in oxygen precipitate ring defects and metallic impurities.

In a previous report, Basnet *et al*. demonstrated that three defect engineering approaches of *tabula rasa* (TR), phosphorous diffusion gettering (PDG) and hydrogenation (H) were very effective in addressing these issues [50]. In their 2020 report, Basnet *et al*. extended this approach to assess the effectiveness of defect engineering in SHJ cells fabricated using treated UMG n-type Cz wafers [52]. They used the defect engineering approaches in two complementary ways. The first group underwent a high temperature *tabula rasa*, followed by a phosphorus diffusion gettering (TR + PDG). In this approach, it is thought that the grown-in oxygen defects were dissolved during the *tabula rasa* and the metallic impurities were subsequently removed via the phosphorous diffusion gettering. An alternative approach combined the PDG with a hydrogenation step (PDG + H). In this approach, the PDG removes metallic impurities and the hydrogenation subsequently passivates the oxygen precipitates

formed during the high temperature process. The high temperature *tabula rasa* and PDG may also lead to the annihilation of thermal donors [33].

Both the TR + PDG and PDG + H approach led to significant improvements in the quality of lifetime test structures. The iV_{OC} of the as-grown UMG Cz wafer was 672 mV, which is too low to compete with commercial electronic grade n-type Cz wafers. However, the TR + PDG and PDG + H treatments led to an increase in iV_{OC} of 40 mV and 35 mV, respectively. Wafers that only received the PDG defect engineering did not improve, as the high temperature process alone leads to the activation of grown-in defects, highlighting the importance of complementary defect engineering treatments. Interestingly, the approaches also led to increases in the iV_{OC} of electronic grade (EG) n-type Cz wafers, which were included as a control. However, the amount of increase was much smaller (11 mV improvement in iV_{OC}), likely due to the lower amount of defects present in the EG silicon.

Both UMG and EG n-type wafers subject to TR + PDG and PDG + H treatments were then fabricated into SHJ solar cells. For UMG cells, the efficiency improved significantly from 18.0% for the as-grown wafer to 21.2% and 21.0% for the TR + PDG and PDG + H groups, respectively. These impressive efficiency enhancements of $3.0\%_{abs}$ are related to increases in all three parameters. A summary of the efficiency data is shown in Table 1. Both the FF and V_{OC} increase after the treatments, related to the significant improvements in the bulk properties. The V_{OC} increases by almost 40 mV for both defect engineering approaches, which closely correlates with the observed increases in iV_{OC} on lifetime structures. Interestingly, the J_{SC} also increases by > 1 mA / cm^2. EQE measurements indicate that both defect engineering routes lead to broadband improvements in the EQE compared to the as-grown case, which is again indicative of improvements in the bulk. Both approaches also led to an increase in efficiency in EG Cz n-type SHJ cells of $> 1\%_{abs}$, from 21.2% for the control

to 22.4% and 22.7% for the TR+PDG and PDG + H treatments, respectively. Although the EG Cz n-type wafers used in this study may not be directly comparable to those used in industry, it still presents a case that all n-type SHJ cells may benefit from defect engineering approaches to modify the bulk recombination.

We have recently extended the defect engineering approaches previously demonstrated on p-type wafers to commercial grade n-type Cz wafers. This work was done in conjunction with SHJ cell manufacturer Hevel Solar. Commercial grade n-type Cz wafers (resistivity 2.6 Ω·cm) underwent a series of modified defect engineering treatments at UNSW.

The wafers were then sent to Hevel Solar, where they were fabricated into full area SHJ cells in an industrial environment. Table 1 displays the I-V characteristics of SHJ cells made using both non-treated control n-type wafers and wafers that underwent defect engineering at UNSW. The efficiency for defect engineered wafers was > $0.5\%_{abs}$ higher than control wafers, increasing from 22.25% to 22.80%. This was related to an improvement in J_{SC}, V_{OC} and FF. This result showing improvements in n-type SHJ cells is consistent with the observations by Basnet *et al*. A comparison of lifetime curves from the control and gettered wafers indicated that the defect engineering caused the bulk lifetime to improve from 6 ms to 7.5 ms. The efficiency enhancement observed is significant, incorporating such defect engineering approaches in production could help to raise the power of SHJ modules. One factor that increases the cost of n-type Cz wafers, relative to p-type Cz wafers, is that there is no market for low quality wafers. During production, some n-type Cz wafers contain a higher concentration of metallic impurities, which reduce the lifetime. The fact that SHJ cell manufacturers conventionally do not include any defect engineering in the process flow

means that these defective wafers are not useful for SHJ cell production. If defect engineering approaches were incorporated, this may improve the utilization of n-type wafers by allowing for a larger number of pulls in an ingot and more recycling of scrap silicon, and also allow a relaxation of the lifetime restrictions given to wafer manufacturers, which would drive down the costs.

Some manufacturers are already beginning to explore the use of defect engineering treatments on n-type Cz silicon wafers for industrial SHJ cells. This is particularly relevant as impurity-related defects become more problematic for larger wafer sizes and the industry is rapidly shifting towards larger wafers. Variations in impurity content can lead to unwanted variations in cell efficiency. For example, SHJ manufacturer Jinergy, who were an early adopter of the M6 wafer size (166 mm × 166 mm), reported the use of 'wafer annealing' to improve the quality of commercial n-type Cz wafers [66]. This led to a reported cell efficiency increase in the range of $0.1\%_{abs} - 0.3\%_{abs}$. As manufacturers strive towards larger cell sizes to increase the power of modules, the use of defect engineering to improve wafer quality may become increasingly relevant for industry.

2.2. Post-Cell Illuminated Annealing

Thin film a-Si:H solar cells are prone to light induced degradation (LID). Illumination has been shown to lead to the formation of recombination active, deep-level dangling bond defects in the bulk of the a-Si:H [67]. This type of LID is generally referred to as the Staebler-Wronski effect (SWE) [68]. Crystalline silicon coated with intrinsic a-Si:H layers has also displayed SWE degradation behaviour when exposed to prolonged illumination [69]. These observations pose the question of whether SHJ cell structures with stacked intrinsic and doped a-Si:H layers as passivation schemes would suffer from the same LID.

In 2016, Kobayashi *et al*. investigated the stability of n-type SHJ solar cells under light soaking conditions [70]. The results are shown in Figure 6 and a summary of the change in efficiency is shown in Table 2. Remarkably, this indicates that the performance of the solar cells actually improves during the light soaking at 1-sun illumination. The efficiency gain saturates at ~ 0.3%$_{abs}$ after a light soaking time of ~ 15 hours. This gain is caused by increases in both the FF and V_{OC}. When the temperature during light soaking was varied from 25 °C to 75 °C, similar results were observed. As shown in Figure 6, the application of a forward bias in the dark (forward bias of 2.8 V with current of 41 mA / cm^2) yields very similar results to light soaking.

This indicates that the changes are induced by the generation of carriers.

To investigate the impact of light soaking on the interface, a series of lifetime test structures were formed containing surface layers of, i) symmetrical *i-i*, ii) symmetrical *i-n*, iii) symmetrical *i-p*, iv) *i-n* / *i-p* cell precursors. After light soaking, the layers coated with

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symmetrical *i-i* layers degraded. The degradation kinetics followed a power law, similar to that seen for SWE. This indicates that this interface undergoes similar degradation to the bulk degradation seen in bulk a-Si:H thin film solar cells. However, all other structures underwent significant increases in carrier lifetime after light soaking. This indicates that the improvement is dependent on changes in the surface passivation quality and that it requires the presence of the doped a-Si:H layers. Fitting of injection dependent lifetime curves from these test structures indicated that the improvements were directly related to a reduction in the density of recombination active interface states.

In 2017, the authors extended this study to one cell mini-modules [71]. The same magnitude of efficiency increase was observed in modules, indicating that these efficiency changes may occur under field operating conditions on non-light-soaked cells. The paper also studied the impact of the incident light spectrum and light intensity on this phenomenon. By illuminating the samples with a series of optical filters, they determined that incident photons in the UV and blue part of the spectrum, which can be absorbed in the a-Si:H itself, did not play a role in the performance improvement. This indicates that the improvement at the interface is related to electron-hole pairs generated in the c-Si absorber. The authors also varied the illumination intensity from 1 sun down to 0.02 suns. Performance enhancements were observed for illumination intensities as low as 0.02 suns.

Author	Year	Material	Area [cm²]	Pre-fabrication wafer-treatment	Post-fabrication process	Efficiency [%]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm2]	Reference
Kobayashi et al.	2016	n-type Cz-Si	243.4	-	-	21.9	731.2	81	-	[70]
					Light soaking	22.2	733.7	81.7	-	
Kobayashi et al.	2017	n-type Cz-Si	243.4	-	-	21.8	731.9	79.9	-	[71]
					Light soaking	22.1	734.5	80.7	-	
Chen et al.	2019	p-type Cz-Si	4	Gettering + hydrogenation	-	16.6	693	69.6	34.5	[44]
					Advanced hydrogenation process	18	707	74.1	34.3	
		p-type mc-Si	4	Gettering + hydrogenation	-	14.5	657	68.6	32.1	
					Advanced hydrogenation process	17.3	701	70.6	34.9	
	2019	p-type Cz-Si	4	Gettering + hydrogenation	-	18.8	694	68.8	39.3	[72]
					Advanced hydrogenation process	20.0	710	72.2	39.2	
					Advanced hydrogenation process + light soaking	19.8	707	71	39.5	
Vicari Stefani et al.	2019	p-type UMG mc-Si	4	Gettering + hydrogenation	-	17.8	680	72.9	35.8	[54]
					Advanced hydrogenation process	18.7	690	74.4	36.2	
Wright et al.	2019	n-type Cz-Si	243.4	-	-	22.0	730	80.1	37.7	[73]
					Illuminated annealing	22.7	737	81.9	37.7	
Vicari Stefani et al.	2020	p-type Cz-Si	244	Gettering	-	21.6 ± 0.1	735.4 ± 0.9	73.8 ± 0.3	39.7±0	[53]
					Advanced hydrogenation process	21.8 ± 0.3	736.7 ± 1.4	74.8 ± 0.8	39.6 ± 0	
					Advanced hydrogenation process + light soaking	21.6 ± 0.2	735.4 ± 0.1	74.1 ± 0.5	39.6 ± 0.1	
			244	Gettering + hydrogenation	-	21.2 ± 0.1	731.1 ± 1.4	73.1 ± 0.2	39.5 ± 0	[53]
					Advanced hydrogenation process	21.7 ± 0	733.3 ± 0.5	74.8 ± 0	39.5 ± 0	
					Advanced hydrogenation process + light soaking	21.3 ± 0.1	729.2 ± 1.2	73.8 ± 0.1	39.5 ± 0	
Cui et al.	2020	n-type Cz-Si	251.99	-	Light and elevated temperature process	+ 0.2 %rel	+ 0.4 %rel	+ 1.5 %rel	+ 0.0 %rel	[74]
Bao et al.	2021	n-type Cz-Si	243.4	-	-	23.1	79.8	738.3	39.4	[75]
					Light soaking	23.6	81.3	740.8	39.4	

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Table 2. Summary of impact of post-cell treatment on silicon heterojunction solar cells

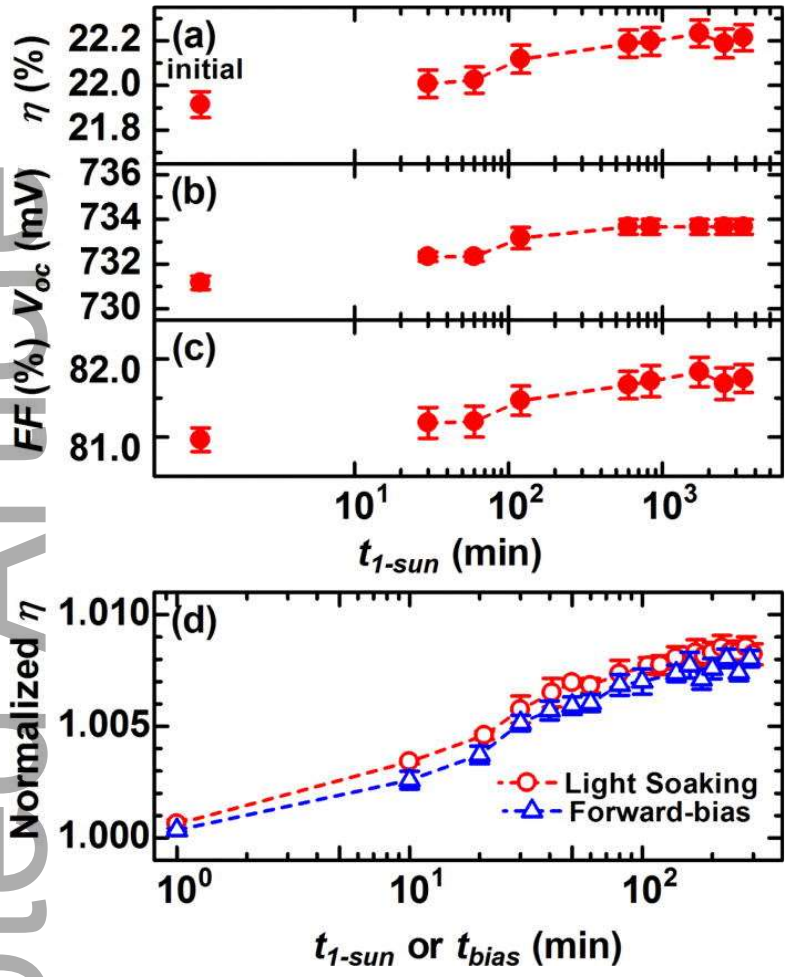

Figure 6. Measured values of a) efficiency, b) V_{OC} and c) FF for n-type silicon heterojunction solar cells under light soaking at 1-sun illumination temperature at 32 ± 2°C. The data points represent average values, the error bars show the standard deviation. d) comparison of normalised efficiency values for 1-sun light soaked and forward biased solar cells. The efficiency was normalised to the initial efficiency value. Reprinted from [70] with the permission of AIP publishing.

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In their conclusion, Kobayashi *et al*. discuss the potential economic ramifications of this 0.3%$_{abs}$ efficiency boost for SHJ modules. For a manufacturer with a 1 GW production capacity, they estimate that the excess production resulting from the increased efficiency could have an economic benefit in the range of 7 – 10 million US dollar per year [70]. This sounds promising, however, light soaking at 1-sun at low temperature requires > 10 hours to reach a stabilised efficiency enhancement. This time scale is far too long to be relevant for industrial applications. In order to receive the full benefit of this annealing, the process must be accelerated to significantly reduce the time of the process.

To accelerate the observed improvements under light soaking, Wright *et al*. investigated the use of high-intensity illuminated annealing [73]. Laser illumination under elevated temperature has been previously used to accelerate the kinetics of degradation and recovery in p-type cell architectures [76][77]. This can result in the passivation of defects in a matter of seconds that may otherwise take hours. In their report, Wright *et al*. used a similar approach. Industrial n-type SHJ cells were sourced from a company, CIE Power. The cells were bifacial, 156 mm × 156 mm and had 5 busbars. During illuminated annealing, the samples were heated to 200 °C on a hot plate and were illuminated with a continuous wave (λ = 960 nm) solid state diode laser with monochromatic illumination intensity of ~ 55 kW / m^2. Accounting for photon density, this is equivalent to approximately 100 suns. The illumination increased the actual cell temperature to ~ 230 °C. The treatment time was 30 s. Remarkably, the average efficiency after the treatment increased by 0.7%$_{abs}$, from 22.05% to 22.75%. A summary of the efficiency data is displayed in Table 2. No statistically significant change was seen in the J_{SC}, the enhancement was related to increased V_{OC} and FF, which increased by 7 mV and 2%$_{abs}$, respectively. It is likely that the improvements in V_{OC} are caused by increased surface passivation, as a reduction in J_0 was seen on lifetime test structures. An analysis of the exact mechanisms involved in the improvement is currently underway.

This high-intensity illuminated annealing approach was extended to a pilot study with Hevel Solar. A batch of 50 busbarless, 156 mm × 156 mm, bifacial SHJ cells were sourced from Hevel Solar and were subsequently treated with laser illumination. Results from 50 cells with a starting efficiency of 22.53 ± 0.12% are displayed in Figure 7. Figure 7 graphically displays the change in V_{OC}, FF and efficiency using box plots. Figure 7 displays a clear increase in efficiency after the post-cell processing. The efficiency improves by $0.58\%_{abs}$ ($2.58\%_{rel}$), this increased efficiency is related to changes in both V_{OC} and FF. The increased FF can be correlated with a reduction in series resistance (R_S). The R_S reduced by 0.13 $\Omega \cdot cm^2$ (11.8%). These results are very promising, they indicate that the illuminated annealing treatment is successful in improving the cell efficiency across a variety of manufacturers and with cells that display vastly different efficiency from the production line.

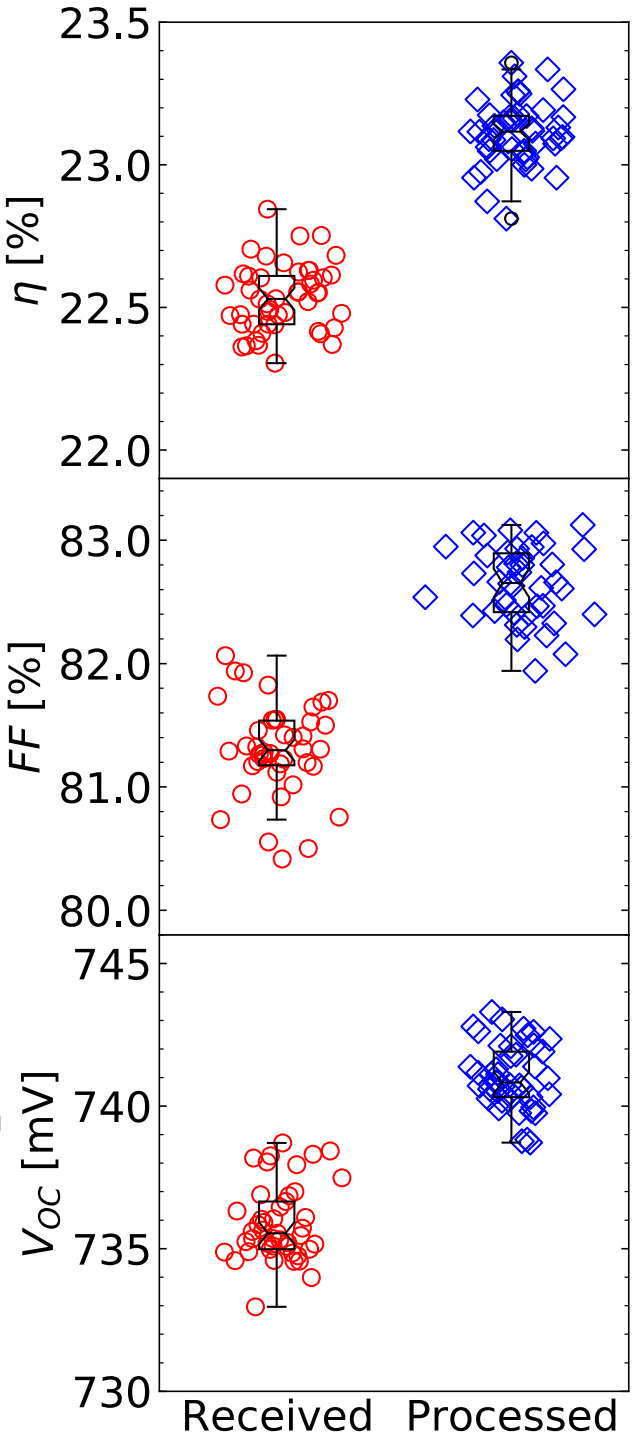

Figure 7. Impact of illuminated annealing on the FF, V_{OC} and efficiency for a batch of 50 n-type SHJ solar cells fabricated in an industrial environment at Hevel Solar.

We are now beginning to see companies adopt this approach in production. Risen presented data on a 'light and elevated temperature process' (LETP) to treat their industrial n-type SHJ cells at the 3rd International Workshop on Silicon Heterojunction Solar Cells [74]. Their

approach did not use laser illumination, instead, it used a belt furnace tool with irradiance provided by lamps. This approach may be more suitable for mass production, as samples can be passed through a belt furnace with a higher volume. The optimised conditions led to an efficiency improvement of ~ 2%$_{rel}$. As with previous reports, the J_{SC} was unchanged. A slight improvement in V_{OC} was seen, however, the majority of the improvement was attributed to increased FF. This was correlated with a significant reduction in R_S, up to approximately 17%$_{rel}$. This closely matches the UNSW observations on the Hevel cell pilot study. There are many components that make up the total R_S in a SHJ solar cell. Identifying the exact mechanism and location in the cell that is improving is an active area of research. Similar to the Kobayashi *et al*. paper [70], Risen reported increased lifetime in symmetrical test structures. A slight reduction in J_0 was observed, indicating that the V_{OC} improvements were related to improved surface passivation. Following the LETP treatment, cells were stored in a N_2 environment and measured periodically. After testing for up to 800 hours, the improved performance appeared to be very stable.

A recent report by Madumelu *et al*. shed some light on the intricacies of light-induced changes in SHJ cell performance [78][79]. By investigating a wide variety of illuminated annealing conditions on commercially produced n-type SHJ cells, they showed that, depending on the temperature and illumination intensity, the cells can undergo significant degradation. Dark annealing at 160 °C led to an efficiency improvement of 0.2%$_{abs}$ ± 0.1%$_{abs}$, however, annealing under 1-sun illumination caused a reduction in efficiency of 0.5%$_{abs}$ ± 0.3%$_{abs}$, with a maximum degradation of 0.8%$_{abs}$. Figure 8 displays the efficiency as a function of illuminated annealing time. The error bars represent the statistics for 5 cells in each group. The observed changes in efficiency were dominated by changes in V_{OC} and FF. Interestingly, the error bars for the illuminated and dark annealed samples are very large, indicating that the response of these commercial cells is very variable. The reduction in V_{OC}

and FF were linked to changes in J_{01} and R_S, respectively. These results were achieved using broadband halogen light sources to represent 1-sun illumination. In line with these observations, several previous reports have shown degradation on a module level for n-type SHJ modules in the field [80][81]. These reports indicate that the observed degradation in SHJ cells may be higher than that for PERC modules, however, the systems investigated employ SHJ cells that were fabricated up to ten years ago, before SHJ cells had a significant presence in PV manufacturing. As such, these results may not be representative of modern n-type SHJ modules. To better understand the influence of both illumination intensity and temperature on the degradation, similar experiments were performed under accelerated conditions using a commercial laser tool. Varying the temperature from 25 °C to 180 °C and the light intensity from 0 to 40 kW/m^2 indicated that both parameters play a large role in modulating the degradation and recovery kinetics. Under some conditions, the recovered cell efficiency was higher than the starting efficiency, while in other cases, it did not fully recover. This is an important study, as it highlights the idea that illuminated annealing can potentially have a negative impact on cell performance. This means that great care must be taken during the optimisation of illuminated annealing for commercial n-type cells.

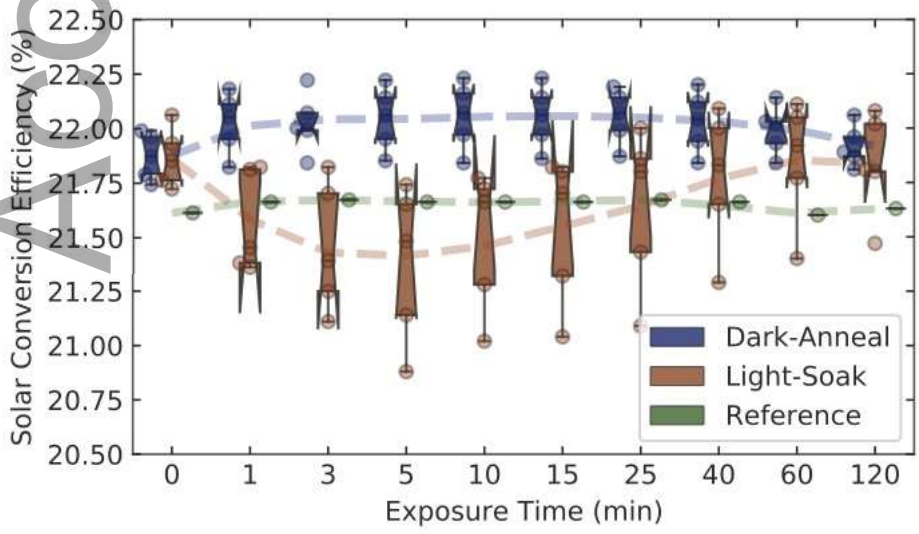

Figure 8. Comparison of efficiency for industrial n-type SHJ solar cells that were either light soaked under 1-sun illumination at 160 °C or dark annealed at 160 °C. A reference sample that was not exposed to light or heat is also shown. Reprinted from [78]. Copyright 2020, with permission from Elsevier.

Bao *et al.* investigated the reversibility of the improved passivation induced by light soaking [75]. They did this by subjecting the samples to repeated extensive light soaking and low temperature dark annealing treatments. The light soaking treatment was applied at a variety of temperatures under high intensity light using a laser, equivalent to approximately 80 suns. The dark anneal was performed at 200 °C under ambient conditions. In lifetime samples with symmetrical *i-i* or symmetrical *i-n* stacks, the lifetime increased significantly after exposure to the first light soaking treatment, which aligns with previous reports. However, the application of a dark annealing step at 200 °C returned the effective lifetime to almost the initial value. Repeated cycling of these two treatments led to a toggling of the lifetime between the two states, indicating the mechanism leading to light-activated improved surface passivation is reversible. A different trend was observed for lifetime structures with symmetrical *i-p* stacks. The different response in the *i-p* stacks was not fully understood, it was suggested this may be due to changes in the film microstructure. The lifetime reduced during dark annealing and improved after light soaking, however, the overall trend after several cycles was a reduction in lifetime compared to the initial value. On full SHJ cells, a similar reversibility was observed for the cell efficiency. After the application of the light soaking step, the efficiency improved by ~ 0.5%$_{abs}$, from ~ 23.2% to ~23.7%. This was caused by an increase in V_{OC} and FF, while J_{SC} was unchanged. However, the application of a subsequent dark-anneal returned the efficiency to the initial value, caused by a removal of the gains in V_{OC} and FF. Subsequent cycling of the two processes displayed a very clear trend, there appears to a direct toggling

between the activated and de-activated states. This report shows that more study is required to fully understand the nature of light-induced changes in the passivation of SHJ cells.

2.3. Hydrogen Passivation to Stabilise p-type SHJ Cells

Another key advantage of using n-type wafers for SHJ cell fabrication is that, unlike boron-doped p-type silicon wafers, n-type silicon is not susceptible to light-induced degradation caused by boron-oxygen related defects (except for n-type wafers compensated with boron dopants, such as in UMG silicon). If manufacturers were to switch to boron-doped p-type Cz wafers to save cost, boron-oxygen light-induced degradation (BO LID) will become a problem [72]. The formation of recombination-active defects in p-type boron-doped wafers under illumination has been known for several decades [82][83][84][85]. This degradation can cause significant power losses in p-type PERC modules [86], which has negative economic and environmental impacts.

BO LID exhibits a degradation and recovery cycle. It is possible that under field operating conditions cells will undergo recovery, however, this may occur over many years and is dependent on many factors. It is more desirable to solve the issue on a cell level before module formation. In 2006, a breakthrough report showed that annealing the cell at elevated temperature when subject to either illumination or current injection (both induce the generation of carriers), the defect could be de-activated [87]. Although there is still uncertainty regarding the exact nature of the defect, it is clear that hydrogen plays a role in passivating BO LID. This understanding has led to the development of high intensity illumination approaches that are able to rapidly stabilize cells susceptible to BO LID. Hallam *et al*. and Hamer *et al*. demonstrated approaches that allowed for the passivation of BO LID on industrial cells within ten seconds [88][89].

Vicari Stefani *et al*. investigated the impact of BO LID in p-type SHJ cells [53]. Commercial grade p-type Cz wafers, with resistivity of 1.6 Ω·cm, were used to ensure that the boron

concentration was similar to that used for industrial PERC solar cells. These wafers were fabricated into full area (244.32 cm^2) p-type SHJ cells in an industrial environment at Meyer Burger, Germany. Prior to cell fabrication, the wafers underwent defect engineering, similar to that described in section 2.1. Two groups were investigated, gettering only (G) and gettering and hydrogenation (G + H). For samples in the G group, cells were fabricated with an average efficiency of 21.6%. The average V_{OC} of cells in this group was 735 mV. This is an impressive result; however, it was shown that these cells were susceptible to BO LID. Light soaking stability testing was performed for 48 hours at room temperature with a white LED light source (< 0.02 suns). The average V_{OC} after light soaking reduced from 735 mV to 658 mV, a drop of more than 70 mV. The efficiency reduced by 3.1%$_{abs}$ to 18.5%, which represents a relative efficiency reduction of 14.3%. This indicates that p-type cells fabricated with passivating contacts, and thus exhibiting high V_{OC}, are even more prone to efficiency reductions from LID. A separate set of cells in the G group were subjected to an illuminated annealing approach, similar to that used for rapid stabilisation of PERC cells. This was referred to as an 'advanced hydrogenation process' (AHP). This led to a slight improvement in efficiency of 0.2%$_{abs}$. When the AHP treated cell underwent the same light soaking stability test, the V_{OC} was remarkably stable. Figure 9 displays in-situ monitoring of the V_{OC} for both the untreated and AHP treated cells. This illustrates the significant V_{OC} reduction due to BO LID in the untreated cell. However, no noticeable change in V_{OC} is seen for the treated cell.

The removal of this BO LID shown in Figure 9 is attributed to hydrogen passivation. These cells that underwent the gettering treatment were coated with hydrogen-containing SiN_X layers before cell fabrication for the purpose of material quality characterisation. These SiN_X:H layers were subsequently removed prior to cell fabrication. Although the wafers did not undergo a high temperature firing process to purposefully introduce hydrogen into the bulk, it is not possible to conclusively state that the

presence of the SiN_X:H layers were not involved in the source of hydrogen for BO passivation. For samples in the G + H group, which did undergo a dedicated high temperature hydrogenation process, the cell efficiency was slightly higher. The highest performing cell achieved a stable efficiency of 22%, with V_{OC} > 735 mV. This is thought to be the demonstration of the highest stable V_{OC} in a cell manufactured with a commercial grade p-type Cz wafer.

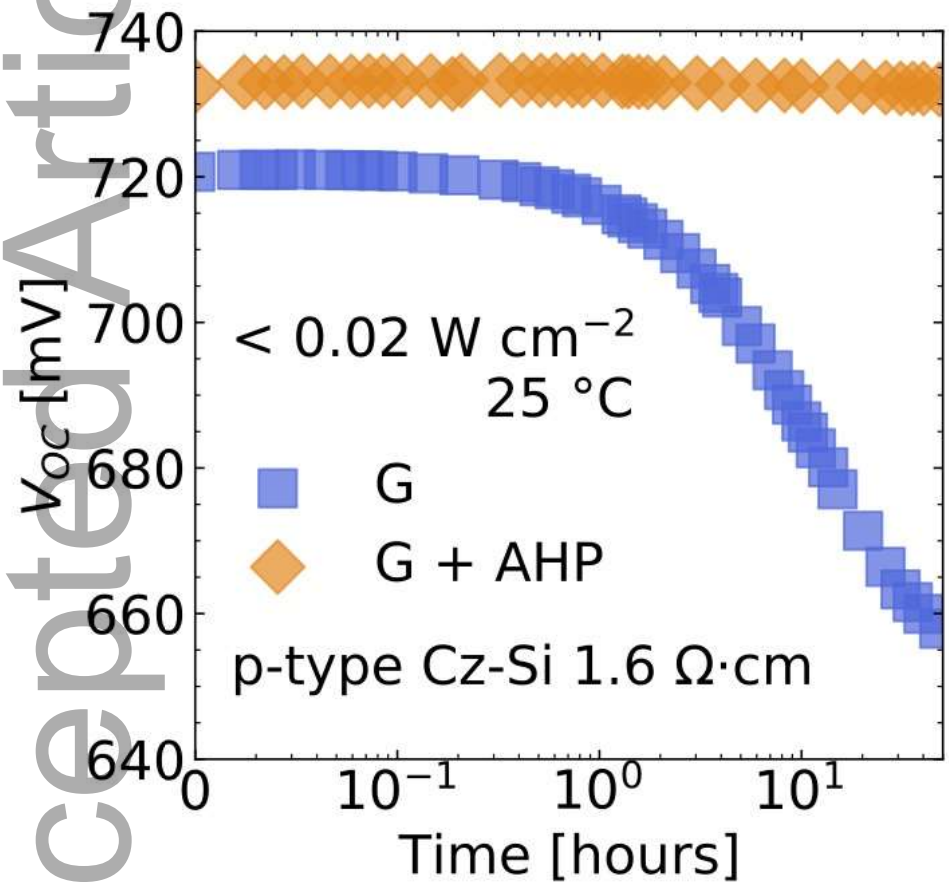

Figure 9. Open-circuit voltage as a function of light soaking time for p-type Cz SHJ solar cells fabricated in an industrial environment at Meyer Burger (Germany). The control sample (blue square), labelled as G, underwent a pre-fabrication gettering step, while the treated sample (orange diamond), labelled as G + AHP also underwent a post-cell hydrogenation process to passivate BO defects. Reproduced with permission [53].

This demonstration of stabilisation in p-type SHJ solar cells poses an important question; what is the source of hydrogen that is used to passivate the bulk defects causing BO LID? It is well known that in cell structures incorporating hydrogen-containing dielectric passivation layers, hydrogen is incorporated into the bulk during firing. This hydrogen is then used to passivate BO defects. However, in the SHJ processing flow there are no hydrogen containing dielectrics that are subsequently fired at high temperatures. In order to study the potential origin of bulk hydrogen in SHJ solar cells, Sun *et al.* studied UMG compensated n-type silicon wafers [90]. The authors used compensated n-type wafers that contained almost equal concentrations of both phosphorous and boron dopants. Due to the large concentration of boron atoms ($> 1\times10^{16}$ cm^{-3}), it is expected that SHJ cells made using these wafers will suffer from BO LID. To study whether the a-Si:H passivation alone was able to contribute sufficient hydrogen to the bulk to passivate these BO defects, half of the n-type compensated wafers underwent a pre-fabrication hydrogenation treatment, which involved the deposition of an 80 nm SiN_X:H film, followed by high temperature firing.

Light soaking under 1-sun illumination caused significant degradation in V_{OC} for all n-type compensated SHJ cell, while an uncompensated n-type control sample did not degrade. Once the cells reached the degraded state, a regeneration process was performed using a 938 nm laser with illumination intensity of approximately 93 suns. The samples were kept on a hot plate at 220 °C. This led to full regeneration of V_{OC} for all UMG samples on a timescale of 30 – 100 s. Following regeneration, the cells went through a second 1-sun light soaking stability test. This showed that all cells were stable, no further BO LID was observed. This rapid passivation of BO LID for both pre-hydrogenated and non pre-hydrogenated samples indicates that during the SHJ process sequence, a significant amount of hydrogen was incorporated into the bulk. However, the scope of this study was insufficient to pinpoint the origin of the hydrogen incorporated into the bulk.

In order to provide further insights into the origin of the source of hydrogen for bulk passivation in SHJ cells, Sun *et al*. investigated the degradation properties of a wide variety of lifetime precursor structures [91]. They used n-type UMG Cz wafers that were heavily compensated, with phosphorous concentration of 2.0×10^{16} cm^{-3} and boron concentration of 1.3×10^{16} cm^{-3}. Due to the high boron concentration, these wafers were susceptible to BO LID, as demonstrated in their previous study [90]. Multiple studies have shown that there is a close correlation between the concentration of hydrogen in the bulk and the regeneration rate of BO defects [92]. Because of this, the authors used the regeneration rate of BO defects as a proxy to compare the relative concentration of bulk hydrogen for a wide variety of passivation schemes. This included fired and non-fired SiN_X:H films as a reference point. Analysis of the injection-corrected regeneration rates indicated that the concentration of bulk hydrogen provided by ***i-n*** / *i-p* cell precursor sample was even higher than the fired SiN_X:H samples. This was independent of whether the ITO layer was present. However, the use of a H_2 plasma treatment to improve surface passivation in a-Si:H films was shown to be crucial in determining the bulk hydrogen concentration. This promising result indicates that the concentration of bulk hydrogen in SHJ cells may be higher than previously assumed.

To assess the relevance of these findings on the hydrogen passivation of BO LID in p-type SHJ cells, we fabricated cells with control wafers, that did not receive any defect engineering at all. Large-area SHJ cells were fabricated with non-treated p-type Cz wafers in an industrial environment at Hevel Solar. One sample was subjected to an AHP LID mitigation treatment, while another cell was left as a control. Figure 10 displays the result of the same BO LID light soaking test. The V_{OC} in the control, which is markedly lower than the defect engineered results displayed by Vicari Stefani [53], displays a similar degradation profile. However, the control cell that undergoes the post-cell AHP treatment is stable. This result implies that the

hydrogen naturally incorporated into the bulk during the industrial SHJ fabrication process is sufficient to successfully mitigate BO LID. This aligns with the findings of Sun *et al*., that suggest the hydrogen incorporated into the bulk is comparable to that introduced during high temperature firing of SiN_X:H films. Importantly, this suggests that a SiN_X:H deposition and firing process for bulk hydrogenation prior to SHJ cell fabrication process is not required to eliminate BO LID, but rather, the only addition to the conventional SHJ solar cell process is a short illuminated annealing process. Furthermore, the same process to treat BO LID may improve the efficiency of n-type SHJ solar cells, as well as p-type cells, through improved surface passivation and current transport properties.

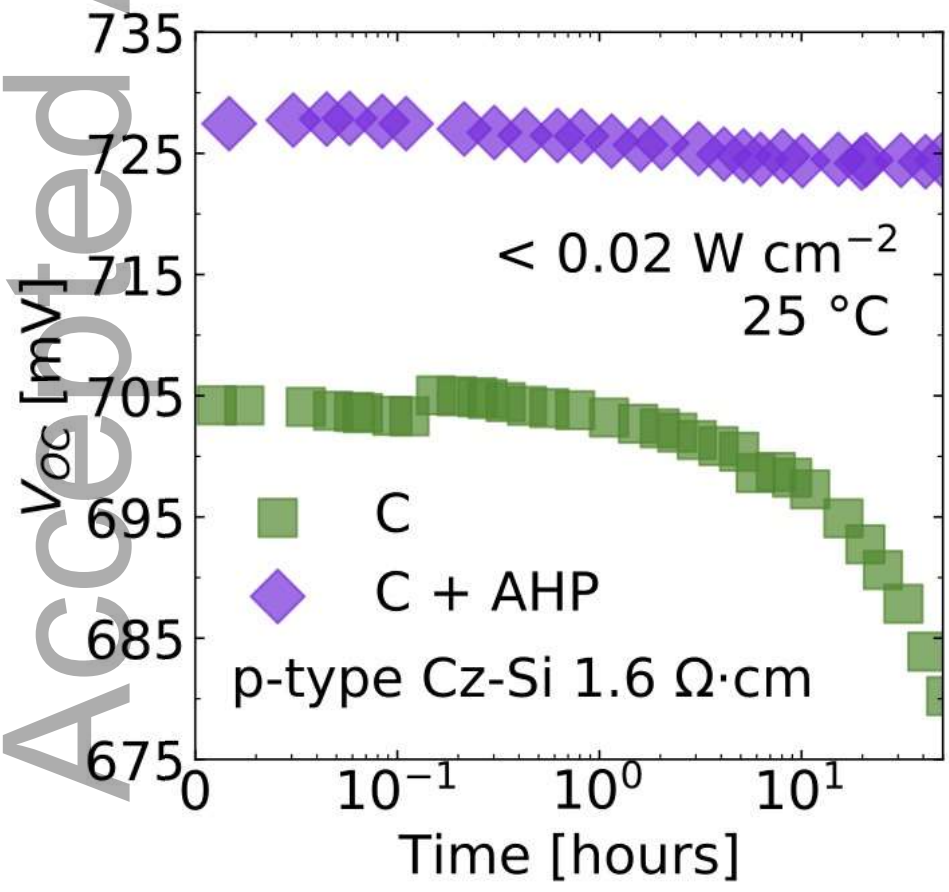

Figure 10. Open-circuit voltage as a function of light soaking time for p-type Cz SHJ solar cells fabricated in an industrial environment at Hevel Solar. Unlike with Figure 9, the control cell in this case, labelled as C, did not receive any pre-fabrication defect engineering

processing. The treated cell, labelled as C + AHP, also did not receive any pre-fabrication defect engineering, however, it received a post-cell hydrogenation stabilisation process.

3. Conclusion and Future Outlook

Silicon heterojunction solar cells have achieved world record efficiency values, which makes them very attractive for commercial production. Due to the low temperature processing regime used in the fabrication of SHJ solar cells, to achieve high efficiencies it is necessary to use high lifetime n-type Cz wafers. It would be attractive from a cost standpoint to use defect engineering approaches, which could significantly reduce the strict material requirements on silicon wafers. On the other hand, the processes are also beneficial for n-type Cz material with multi millisecond lifetimes. This review has surveyed recent efforts to incorporate defect engineering approaches, namely gettering and hydrogenation, to improve the performance of SHJ cells fabricated using a variety of p-type wafers. These approaches have proved successful, with V_{OC} exceeding 700 mV achieved on p-type mc-Si and 740 mV on p-type Cz wafers. Interestingly, these same defect engineering approaches used on p-type cells have also been very beneficial for n-type wafers, even those high lifetime n-type Cz wafers typically used in industry. As wafer sizes increase, meaning that controlling impurity-related defects becomes more difficult, consideration should be given to the integration of defect engineering into either p-type or n-type wafers. Defect engineering can also come in the form of post-cell illuminated annealing processes. Over the past few years, multiple demonstrations have shown the successful application of illuminated annealing to industrial n-type SHJ cells, with observed efficiency enhancements as high as $0.7\%_{abs}$. These approaches have been demonstrated using cells from a wide variety of manufacturers and we are beginning to see it incorporated into the processing sequence by at least one SHJ cell company. The very same approaches are crucial for both improving the performance and solving stability issues in p-type SHJ solar cells. We have recently demonstrated that the hydrogen naturally incorporated

in the a-Si:H layers is sufficient to passivate BO defects and thus stabilize p-type cells. This again indicates that approaches that are beneficial for p-type cells are also beneficial for n-type cells. By viewing the available literature together, it seems that many of the processes necessary to improve the performance of p-type cells are also beneficial for n-type systems. This could suggest that a paradigm shift in SHJ processing is required. The merging of defect engineering approaches used in p-type cells with current SHJ processing approaches may be required to fully realise the potential of the technology. Figure 11 details a proposed modified SHJ process flow that incorporates the discussed defect engineering approaches.

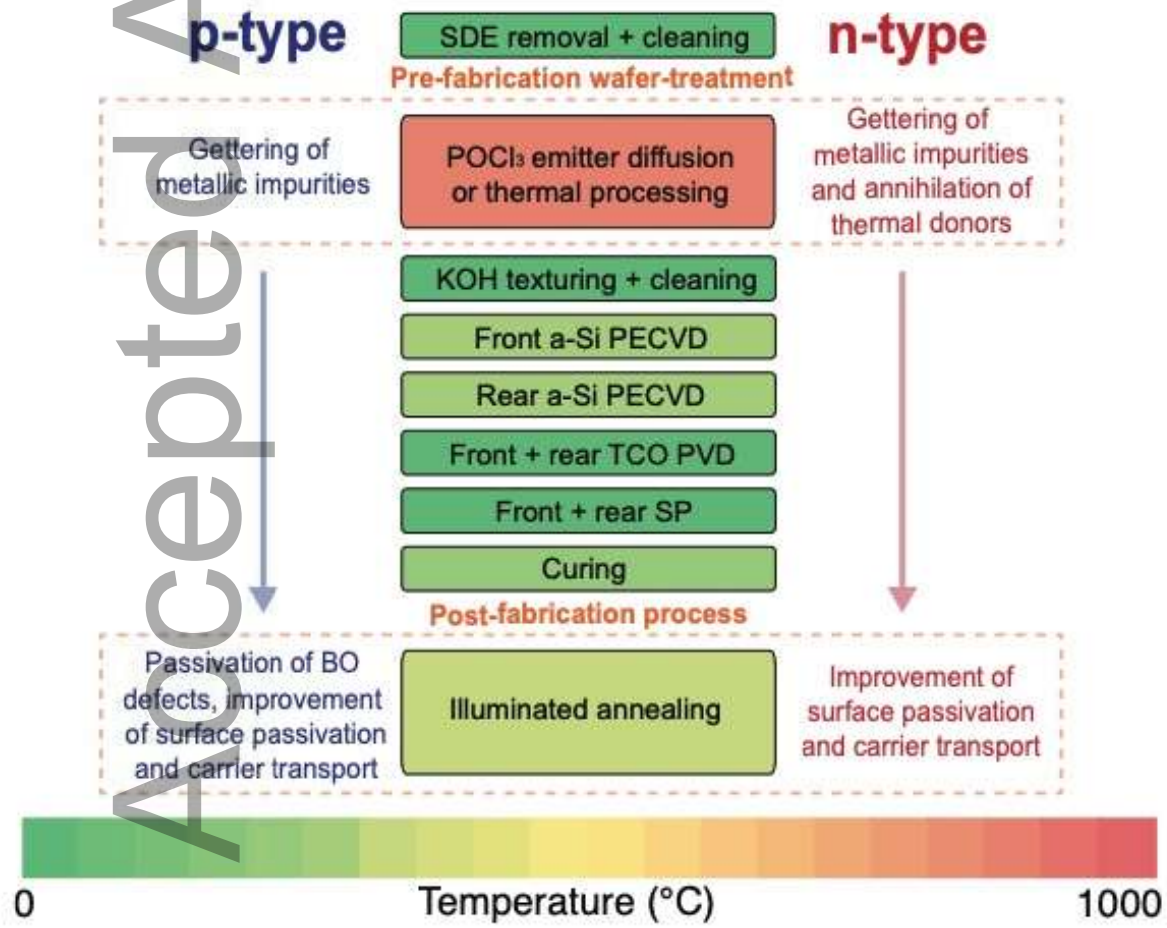

Figure 11. Proposed altered SHJ solar cell processing sequence.

In order to reap the benefits of defect engineering approaches in industrial SHJ cells, the additional processing must be cost effective. The cost of both the SHJ cell processing and defect engineering approaches are rapidly changing. As such, it is difficult to definitively quantify the cost benefits. Here, we provide a preliminary cost assessment of the impact of additional defect engineering processes on the cost of SHJ cells, in terms of $US / W. From here on, $US will be referred to as $. In 2021, the cost of a SHJ cell, including the wafer and processing, is ~ $0.15 / W [93]. For the calculation, we assume a cell efficiency of 24% and cell area of 244.3 cm^2. In 2018, Woodhouse *et al.* provided a detailed overview of processing costs. They show that the cost for gettering with a $POCl_3$ diffusion for a 21.5% efficient PERC cell is 3.0 c / cell [94]. In Chang *et al.*, the authors detail processing costs for illuminated annealing tools. They consider a range of approaches, including an inline furnace with LED illumination and an industrial laser approach. The authors suggest that the processing cost for these approaches is in the range of 0.2 to 1.0 c / cell [37][95]. These costs were also generated in 2018. As these values would have reduced over time, and will continue to reduce into the future, we have not used single values in our cost analysis. Instead, we use a contour plot showing a range of additional costs associated with defect engineering.

The potential efficiency gains realised by defect engineering is also variable and dependent on the type of silicon used and the starting base efficiency of the cell. The benefits of defect engineering on a wafer can be very large for lower quality materials. Increases in iV_{OC} of > 70 mV in p-type mc-Si samples and an efficiency gain of $3\%_{abs}$ for UMG n-type Cz wafers indicate the vast potential for defect engineering to improve lower quality silicon materials. Gains of $0.5\%_{abs}$ have also been achieved on commercial n-type Cz wafers with multi millisecond lifetime, indicating that these approaches are also applicable to improve standard Cz materials. These large gains contrast the findings of Descouedres et al., who showed that gettering p-type Cz wafers led to an efficiency improvement of only $0.2\%_{abs}$. Similar variance

is observed for illuminated annealing. Efficiency gains of > 2%$_{abs}$ are seen for p-type mc-Si materials, while the enhancement is in the range of 0.3%$_{abs}$ to 0.7%$_{abs}$ for n-type Cz materials.

As such, taking this available data into account, we investigate the impact of the defect engineering processes with an additional cost in the range from 0.0 c / cell to 3.0 c / cell and efficiency gains in the range from 0%$_{abs}$ to 1.0%$_{abs}$. These additional costs assume no changes in the incoming wafer costs. Figure 12 displays a contour plot that details the change in SHJ cell cost, in terms of $ / W, as a function of both the defect engineering cost and the associated efficiency gain. Focussing first on defect engineering on a wafer level, the 2018 cost of gettering was ~ 3.0 c / cell [94]. However, by taking into account the cost reductions over the past years, as reported in the 11th ITRPV report, this would reduce to 2.2 c / cell in 2020 [23]. According to Figure 12, this defect engineering cost would require an efficiency gain of 0.6%$_{abs}$ in order to break even and achieve an overall cost of $0.15 / W. This required efficiency gain is comparable to that observed for n-type Cz wafers shown in this work. However, for simplicity, Figure 12 displays the cost solely at a cell level. The required efficiency increase is substantially reduced when considering costs at the module level, due to the increased efficiency. According to the ITRPV, in January 2020, the cell-module conversion cost comprised 53% of the total module cost [23]. As such the required efficiency gain would approximately halve to 0.3%$_{abs}$. At the system level, assuming a cost of $0.63 / W, the required efficiency gain would again approximately halve to 0.15%$_{abs}$. Based on the efficiency gains demonstrated herein, this indicates that the addition of a gettering process is cost favourable.

The reported cost range of illuminated annealing processes is from 0.2 to 1.0 c / cell. For the upper cost bound of 1.0 c / cell, the efficiency gain required to achieve $0.15 / W is 0.25%$_{abs}$.

For the 0.2 c / cell case, this reduces to less than 0.1%$_{abs}$. As discussed above, moving to a module and system level, the required efficiency gains are even further reduced. As efficiency gains of > 0.5%$_{abs}$ have already been demonstrated on commercial n-type Cz wafers, it is highly likely that this approach will yield cost benefits. However, we note that a starting cell efficiency of 24% is used in this simulation. It is likely that the efficiency gains from defect engineering will be more difficult as the standard efficiency value increases to such high levels. To achieve an efficiency of 24% without defect engineering, it would require high lifetime n-type Cz wafers. However, as shown in this article, the use of defect engineering approaches may allow for cheaper wafers to be used. If the wafer cost was reduced by 5% or 10%, and the same efficiency maintained, the cost would reduce to \$0.147 / W and \$0.144 / W, respectively. For these scenarios, where the cost is reduced via lowering wafer costs, the efficiency gains afforded by defect engineering would be even more crucial.

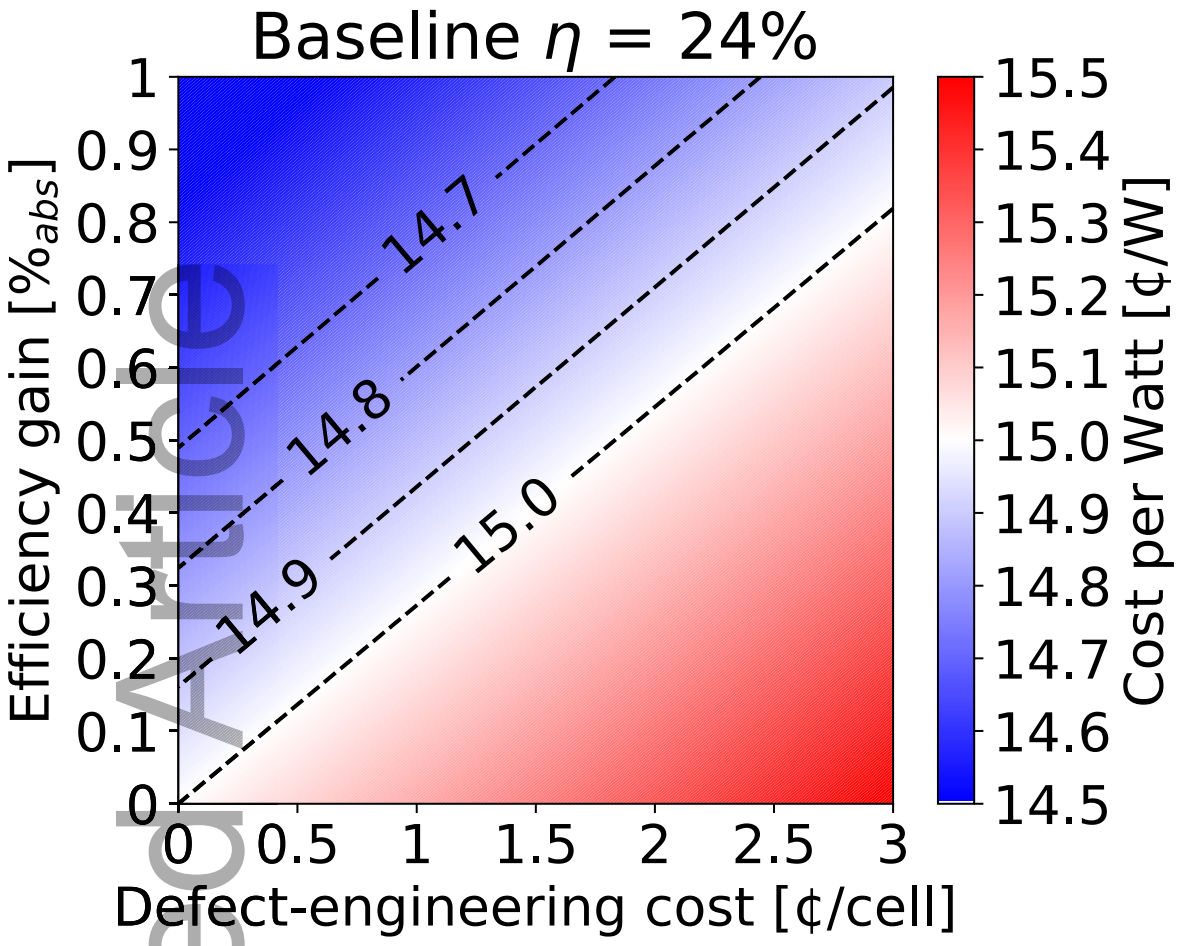

Figure 12. Contour plot displaying changes in the cost of a SHJ solar cell (in terms of $/W), as a function of both the additional defect engineering processing cost, shown on the x axis, and the associated efficiency gain, shown on the y axis. The costs are represented by a colour scale. The assumed value for cost with no defect engineering approaches ($0.15/W) is represented by a white line. Blue portions of the graph represent cost benefits, while red portions of the graph indicate conditions that would lead to increased cost.

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TOC text

Here, we review the benefits of including defect engineering processes, either via treatments on the silicon wafer level or post-cell annealing processes, into the fabrication approach for silicon heterojunction solar cells. Defect engineering can improve silicon heterojunction solar cells made using both cheap p-type wafers and the more expensive n-type CZ wafers currently used in industry.

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