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Temperature Dependent Vertical Conduction of GaN HEMT Structures on Silicon and Bulk GaN Substrates

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The vertical leakage current mechanisms of high electron mobility transistors (HEMT) grown by metalorganic chemical vapor deposition (MOCVD) on Si and GaN substrate under forward and reverse bias are analyzed at ambient temperatures from 25 °C to 200 °C. For the GaN/Si case, a thermally activated vertical conduction with two temperature regimes and activation energies of 0.06 eV and 0.43 eV is found. In contrast to that, the GaN/GaN case shows a single activation energy of 0.67 eV for the rate-limited vertical conduction. For forward vertical bias, Poole–Frenkel (PF) conduction is identified as the dominant conduction mechanism at higher fields for both substrates. In reverse bias, space charge limited and PF conduction are identified as dominant conduction mechanism for GaN/Si and GaN/GaN, respectively. The deviation in vertical conduction mechanism is related to a significant reduction in the dislocation density by three orders of magnitude and homoepitaxially lattice matched growth for the GaN/GaN HEMT.

1. Introduction

Advanced future applications like high-frequency amplification and power switching demand for transistor operation at elevated temperatures well above the limits established by conventional silicon (Si) transistor technology. The high electron mobility transistor (HEMT) has proven to be a future candidate to enable high frequency switching and high power switching at elevated temperatures above 200 °C.[1] The substrate widely used for GaN HEMT is Si and is established as the "workhorse"-substrate of the industry due to its low cost and large size availability.[2,3] In addition to that, Si is already well known and established in complementary metal-oxide-semiconductor (CMOS) fabrication sites entering the fast growing GaN market. This is despite to the challenges like lattice and thermal mismatches (−16.9% and 54%, respectively) and thermal management issues that arise when using Si as a substrate.[2,4] Recently, hydride vapor phase epitaxy (HVPE) grown bulk GaN is gaining interest as a substrate candidate for transistor applications, which is also driven and supported by the need for GaN substrates in the optoelectronics market.[5,6] Growing HEMT on native GaN substrates offers the benefits of no lattice and thermal mismatch along with the drawbacks of high-substrate cost and limitations in available substrate size for the desired insulating substrates. However, the lattice match of epitaxy and substrate allows the simplification of the epitaxial stack. Transition layers tailored for GaN buffer growth on Si can be eliminated. This direct lattice-matched epitaxy leads to a significant reduction in defect density and threading dislocations density. GaN on GaN HEMTs showing superior electrical performance have been reported recently.[7,8] This is pronounced in three orders lower off-state leakage and reduced current collapse when being compared to HEMT on Si and sapphire substrates which is correlated to a reduced dislocation density due to homoepitaxy.

In addition to transistor performance, which is mainly taking part between the three top terminals drain, source and gate, the bulk-dependent vertical conduction to the fourth terminal, the bottom bulk contact, cannot be neglected. To understand and enable the optimum choice of substrate and buffer to achieve vertical device isolation along with low vertical leakage and reliable transistor performance, the vertical conduction mechanisms across the different regions and junctions are analyzed in depth.

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Table 1. Sample overview specifying substrate type, buffer type, sheet resistance, 2DEG mobility and carrier concentration (N.A.: not available).

	Substrate	Buffer	Epi supplier	R_{sheet} [$\Omega\,\square^{-1}$]	Mobility [$cm^2\,Vs^{-1}$]	Carrier conc. [cm^{-2}]
Sample A	6″ Si	GaN:C	A	380	2250	7.2×10^{12}
Sample B	2″ GaN	GaN:Fe	B	231	N.A.	N.A.

2. Experimental Section

In this work, vertical currents are measured as a function of temperature on samples grown on Si (GaN/Si) and samples grown on GaN (GaN/GaN) and conduction mechanisms are evaluated and studied. AlGaN/GaN HEMT epi-layers were grown by metalorganic chemical vapor deposition (MOCVD) on 6-inch Si (111) and 2-inch GaN (c-plane) substrates using the conventional precursors and industrial type of equipment. An overview of the samples used in this work is summarized in **Table 1**.

The wafers were processed into test structures. Mesa isolation was achieved by 500 nm deep dry etching. Ti/Al/Ni/Au metal stack annealed at 830 °C was used to form the ohmic contacts without any surface treatment or ohmic contact recess etching. The samples were back-metallized using aluminum to enhance electrical and thermal contact to the measurement chuck. Layer stacks of samples A and B are shown in **Figure 1**a,b, respectively. The GaN substrate was grown on a sapphire template by HVPE. After growth the GaN layer is released from the template and polished from the front side. The GaN substrate is iron doped

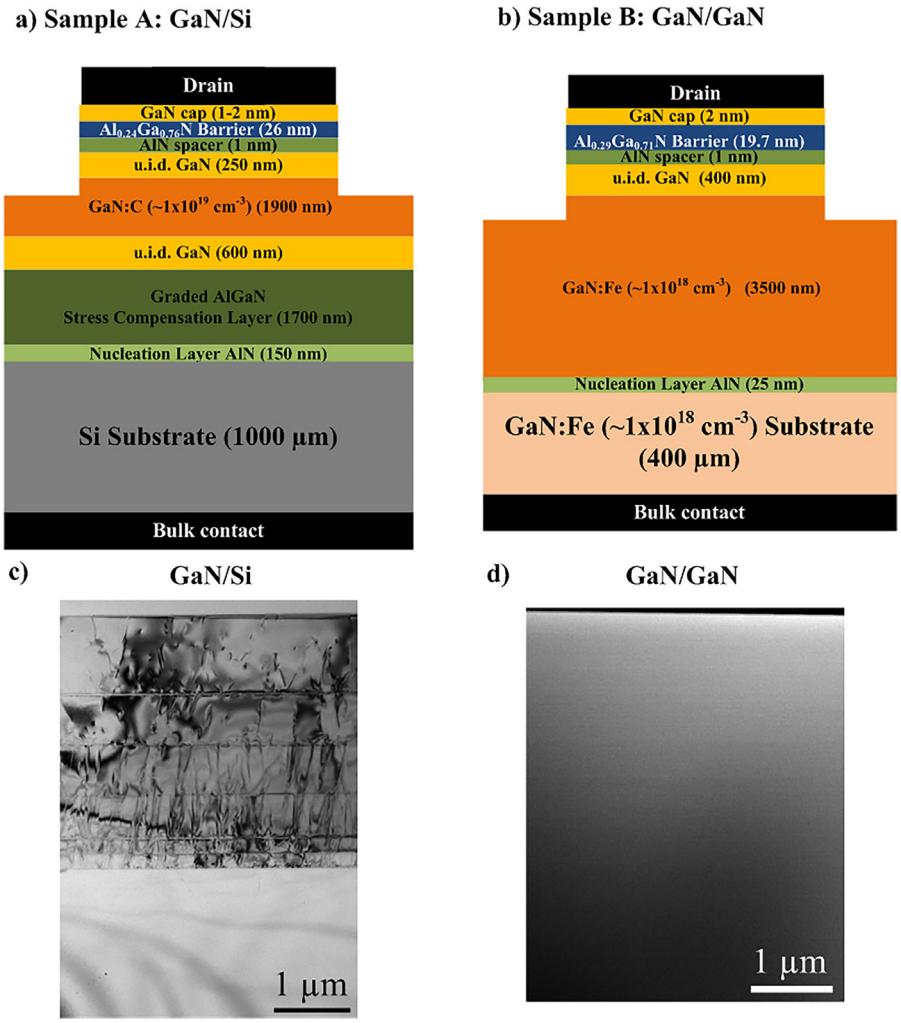

Figure 1. Schematic illustrations of the HEMT grown on Si (a) and GaN substrates (b), properties of AlGaN barrier and AlN spacer are confirmed by XRD. Drain and bulk contact used for vertical electrical analysis are indicated. TEM cross-sections of typical AlGaN/GaN HEMT grown on Si (c) and GaN (d) substrates.

with a doping concentration of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ and a resistivity of $>10^{6}\,\Omega\,\mathrm{cm}^{-1}$ was measured.

TEM cross-sections of a typical AlGaN/GaN HEMT grown on Si and GaN substrates are shown in Figure 1c,d, respectively. TEM analyses reveal dislocation densities of $10^{9}\,\mathrm{cm}^{-2}$ for a typical GaN/Si sample and below $10^{6}\,\mathrm{cm}^{-2}$ (which is the detection limit) for the GaN/GaN sample. This confirms the existence of threading dislocations for the case of GaN/Si heteroepitaxy and a significant reduction in defects with GaN/GaN homoepitaxy. This translates into a higher amount of potential trapping sites, leakage paths, and degradation of mobility and thermal conductivity for the GaN/Si case compared to the GaN/GaN case.[9,10]

Electrical measurements of the vertical current from drain to bulk (I_{DB}), biasing the layer stack in forward (drain potential high), and reverse direction (drain potential low) were performed by sweeping the vertical voltage (V_{DB}) by a Keithley 2410 source measure unit. All measurements in this work were performed biasing only drain and substrate contact, source and gate can always be considered floating due to the absence of electrical connection. Drain pad sizes were 150 µm × 400 µm and 150 µm × 200 µm. Measurements were conducted from 25 °C to 200 °C heating the measurement chuck. For each measurement, a previously unbiased location is used, which is enabled by excellent wafer uniformity (e.g., GaN/Si sample A: AlGaN thickness 0.7% std. dev.).

3. Results and Discussion

Vertical leakage currents of the GaN/Si sample A and the GaN/GaN sample B measured in forward and reverse bias at selected temperatures are shown in **Figure 2**a,b, respectively. For a power switching application the leakage in forward bias is of main interest. This is the case when the transistor operates in off-state and a high potential is at the drain, while the bulk is grounded. The average physical breakdown in forward bias is at 825 V and 280 V for the GaN/Si and GaN/GaN samples, respectively. This shows that the GaN/Si sample has superior vertical isolation properties, when being compared to the GaN/GaN sample, resulting from more advanced layer design and more effective buffer compensation doping. However, the physical leakage and breakdown mechanisms are of major interest for both substrates. When comparing the symmetry of the reverse- and forward-biased measurements of both samples a deviation of the forward conduction mechanism from the reverse mechanism is indicated by diverging slopes for the GaN/Si case.[11] This will be analyzed and discussed by fitting the behavior of different conduction mechanisms to the measurements later in this work.

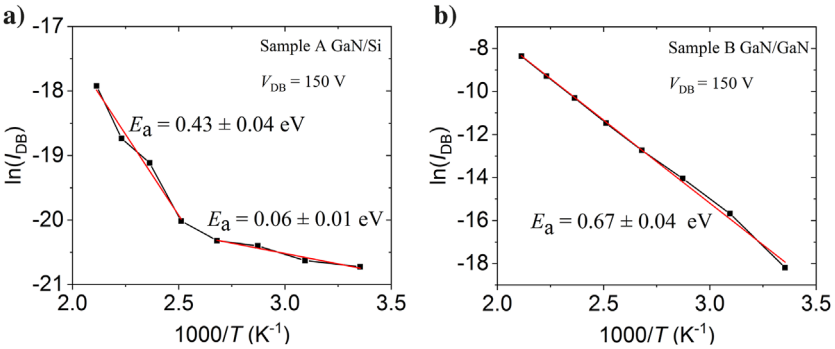

Figure 3. Arrhenius plots of the thermally activated vertical currents measured in forward direction of the GaN/Si sample A (a) and the GaN/GaN sample B (b) extracted at a forward bias of $V_{DB} = 150\,\mathrm{V}$.

Arrhenius plots of the thermally activated vertical currents measured in forward direction of the GaN/Si sample A and the GaN/GaN sample B extracted at a forward bias of $V_{DB} = 150\,\mathrm{V}$ are shown in **Figure 3**a,b, respectively. The bias level was chosen to enable comparison between the samples without influence of high fields and below the breakdown regime.

It can be assumed that the vertical conduction is a thermally activated process which is rate limited and follows the Arrhenius law: $I_{DB} = I_{DB,0} \exp(-E_a/k_b T)$, where E_a is the activation Energy and k_b is the Boltzmann constant.[12] For the GaN/GaN sample, the extracted vertical current linearly decreases with $1/T$ and one linear fit matches the measurement very well. From this, an activation energy (and fitting error) of $0.67 \pm 0.04\,\mathrm{eV}$ can be extracted. A single activation energy and therefore a good linear fit in the Arrhenius plot for GaN/GaN grown HEMT is also reported in the literature for molecular beam epitaxy (MBE) grown samples.[13] However, a lower activation energy of about 0.35 eV is reported. This difference in activation energy can be explained by a diverging layer stack and different trap properties introduced by a higher dislocation density of $6\text{–}8 \times 10^{8}\,\mathrm{cm}^{-2}$, which suggests lower material quality, a regrowth of HEMT layers by MBE on an MOCVD buffer template and a different GaN substrate supplier.

For the GaN/Si sample A two different temperature regimes can be observed. Currents measured at chuck temperatures from 25 °C to 100 °C and measured from 125 °C to

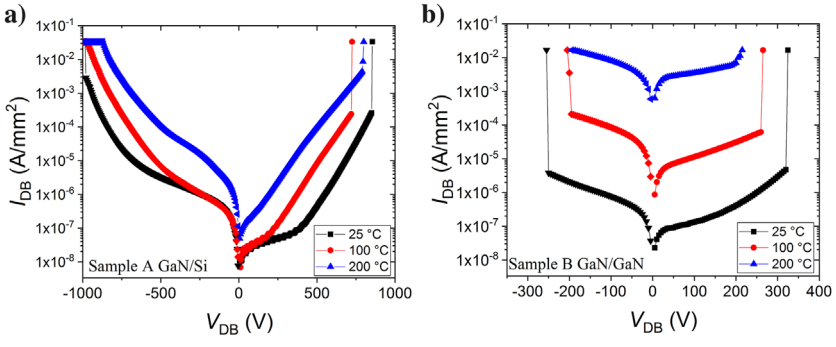

Figure 2. Vertical leakage measured in forward and reverse for GaN/Si sample A (a) and GaN/GaN sample B (b) shown for selected temperatures.

200 °C each form a temperature regime and show a linear increase with $1/T$. Activation energies of 0.06 ± 0.01 eV (25–100 °C) and 0.43 ± 0.04 eV (125–200 °C) were extracted. It can be concluded, in contrast to the GaN/GaN sample, that there exist two different trap species and related conduction mechanisms for the GaN/Si sample which both are dominant in the respective temperature regimes. Activation energies extracted at voltages from 60 V to 200 V (targeting comparable fields in the buffer for both samples) including their fitting errors are shown in **Figure 4**. From this, an average activation energy of $0.66 \text{ eV} \pm 0.02$ eV was extracted for the GaN/GaN sample B. For the GaN/Si sample A, average activation energies of $0.46 \text{ eV} \pm 0.09$ eV and $0.06 \text{ eV} \pm 0.02$ eV were extracted for the high- and low-temperature regimes, respectively.

Comparable temperature regimes with slight changes in activation energies (0.35 eV and 0.10 eV) are reported in literature for MBE grown GaN/Si HEMT.[13] The difference from the values reported in the literature and shown in this work may stem from the different applied growth technique resulting in different trap properties and therefore activation energies. There are many variables which govern the behavior of the vertical conduction of GaN on Si, such as the nucleation layer growth temperature, the type, and number of buffer interlayers and their respective compensation doping. These variables lead to different trap activation energies as observed extensively in the literature.[14] Arrhenius cross sections at $1/T = 0$ ($I_{DB,0}$) of 3.03 kA, 1.6 mA and 7.24 nA were extracted for the GaN/GaN sample, for the GaN/Si high-temperature regime and for the GaN/Si low-temperature regime, respectively. Comparing the Arrhenius cross section of the high-temperature regime of the GaN/Si sample to the $I_{DB,0}$ of the GaN/GaN sample reveals a higher leakage current at high temperature, which can be explained by non-effective buffer compensation of the GaN/GaN sample. When comparing the results obtained from GaN/Si and GaN/GaN HEMT, the highest sensitivity to temperature for the vertical leakage current is observed for the GaN/GaN case. For GaN/Si only very weak (25–100 °C) and weak (125–200 °C) activation of the vertical leakage by increasing temperature is observed.

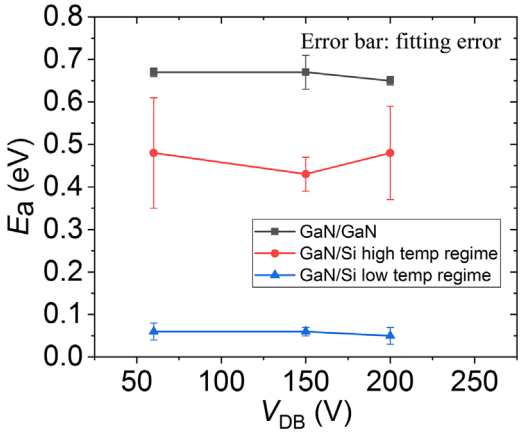

Figure 4. Activation energies as a function of vertical voltage, fitting errors from the Arrhenius plots are shown as error bars.

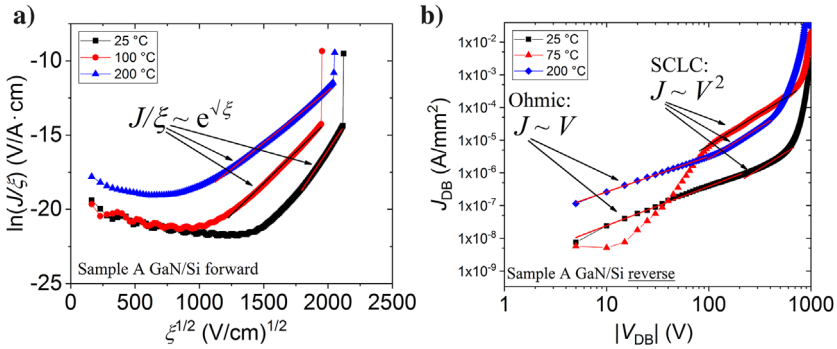

Figure 5. Electric field normalized current density versus square root of the electric field indicating Poole–Frenkel transport (PF) for vertical current measured at forward bias (a) and double logarithmic plot showing space charge limited current (SCLC) and ohmic conduction for vertical current measured at reverse bias of the GaN/Si sample A (b).

To further analyze the vertical current conduction mechanism of the GaN/Si sample A, the quotient of the vertical current density measured at selected temperatures and normalized electric field is plotted in a semi logarithmic plot as a function of the square root of the normalized electric field and is shown in **Figure 5**a.

For high electric fields (25 °C: from $\approx 1.5 \text{ kV}^{1/2}\text{cm}^{-1/2}$ ($\approx 2.25 \text{ MV cm}^{-1}$) equivalent of V_{DB} ≈430 V, 100 °C: $\approx 1.25 \text{ kV}^{1/2}\text{cm}^{-1/2}$ ($\approx 1.56 \text{ MV cm}^{-1}$) equivalent of V_{DB} ≈300 V, 200 °C: $\approx 1 \text{ kV}^{1/2}\text{cm}^{-1/2}$ ($\approx 1 \text{ MV cm}^{-1}$) equivalent of V_{DB} ≈190 V) a good agreement with a linear fit is observed, which indicates Poole–Frenkel conduction (PF).[18] The identified PF conduction follows:

$$J_{PF} = A\xi \exp\left(\frac{q}{k_b T}\sqrt{\frac{q\xi}{\Pi\varepsilon}}\right) \quad (1)$$

with

$$A = q n_t \mu \exp\left(-q\frac{\Phi_{PF}}{k_b T}\right) \quad (2)$$

where k_b is the Boltzmann constant, T is the temperature, q is the elementary charge, ξ is the effective electric field, μ is the effective mobility, n_t is the total trap density, and Φ_{PF} is the effective trap density. PF conduction occurs due to the lowering of a Coulombic potential barrier around a charged trap when it is exposed to an electric field as shown in the band diagram in **Figure 6**. With increasing temperature the measured leakage current increases. This can be explained by an increasing available amount of free carriers and increasing ionization of buffer traps.[15] The current shows PF characteristics until the physical breakdown. For lower electric fields, the diverging characteristics from the linear PF fit can be explained by mixed conduction with an ohmic component for the transition and

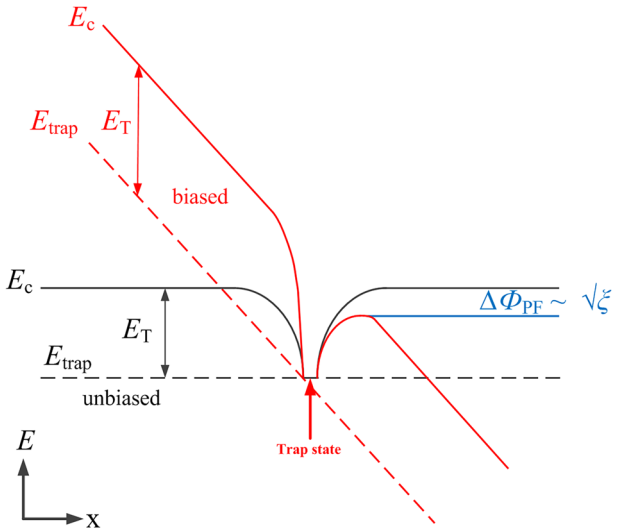

Figure 6. Schematic sketch of the band diagram during Poole–Frenkel conduction under biased (red) and unbiased (black) condition.[16]

pure ohmic conduction for low-electric fields. This is confirmed by a slope of about one in the double-logarithmic current–voltage (I–V) plot (Figure 5b).

The vertical current measured in reverse bias of the GaN/Si stack is plotted in a double logarithmic plot in Figure 5b. For high negative bias (100–700 V), a good agreement with a linear fit and a slope of about 2 in the log–log plot indicates space charge limited current (SCLC). The identified SCLC conduction is described by the equation: [17]

$$J_{SCLC} = \frac{9}{8}\varepsilon\mu_L\frac{V^2}{L^3} \quad (3)$$

where ε is the permittivity, μ_L is the effective mobility, and L is the space charge region length. This leads to the conclusion that in the negative bias case electrons are injected from the drain electrode and their conduction is limited by a space charge, e.g., formed in the nucleation layer.[18] Toward the negative physical breakdown, the current characteristic diverges from SCLC toward a mixed conduction with higher order dependency. As for the forward bias, a trend of increasing current for increasing temperature is observed.

For the case of the GaN/GaN sample, as shown in **Figure 7**a, the vertical current measured under forward bias shows an ohmic behavior for moderate fields up to about $700\,V^{1/2}\,cm^{-1/2}$ ($490\,kV\,cm^{-1}$) and PF behavior until the breakdown of the device. The reverse conduction, as shown in Figure 7b, reveals an ohmic onset up to about $250\,V^{1/2}\,cm^{-1/2}$ ($62.5\,kV\,cm^{-1}$) and is dominated by PF conduction up to the physical breakdown. A strong increase in current with increasing temperature is observed, which becomes also evident in the Arrhenius plot (Figure 3b). Having similar conduction mechanisms for the GaN/GaN sample in forward as well as in reverse direction can be related to the homoepitaxially grown layer stack only interrupted by a thin AlN nucleation layer (Figure 1b).

Band diagrams of the associated vertical conduction mechanisms are sketched in **Figure 8**. In the reverse bias for the GaN/Si case (Figure 8 top, left), electrons from the top ohmic contact are injected into the buffer layer and fill buffer traps. Excess electrons flow into the Si substrate and contribute to the leakage current. Threading dislocations and defects (Figure 1c) are assumed to provide additional leakage paths and trapping centers. For the forward-biased case of the GaN/Si (Figure 8 bottom, left), the conduction band in the Si substrate close to the AlN transition layer is assumed to bend below the Fermi level due to a voltage drop in this region and form a conductive inversion channel.[19,20] At higher forward bias, electric fields exceeding the critical value ($0.3\,MV\,cm^{-1}$) impact ionization may occur and cause electrons to be injected into the buffer, which fills buffer traps or contributes to the reverse current.[11]

For the GaN/GaN case (Figure 8, right), a relatively thin 25 nm AlN nucleation layer separates the GaN substrate from the GaN buffer. Due to the high bandgap of GaN, it is not assumed that an inversion channel is formed. The critical electric field of GaN ($3\,MV\,cm^{-1}$) is 10 times higher than the one of Si, which makes impact ionization less likely when comparing to the Si substrate. Charge carriers directly tunnel through the NL or overcome the barrier.

Under vertical bias the proposed current path for the GaN/Si case is through a dislocation-related path (e.g., screw/threading dislocations) mixed with bulk conductivity.[21] Vertical current paths through dislocations will allow fast charging and discharging of buffer traps which are created by compensation doping and threading dislocations and are expected to create a good dynamic behavior. Due to the significant reduction of dislocations for the GaN/GaN structure, the proposed conduction is bulk conductivity which is due to unintentional n-type doping species, which also becomes evident by low-breakdown voltages. This different dominant conduction path is also assumed to explain the higher thermal activation of the current conduction observed for the GaN/GaN layers. The reason for this is the simplification of the layer stack for the GaN/GaN case to consist only of a thin nucleation layer and no stress compensation layer, which is enabled by homoepitaxially grown

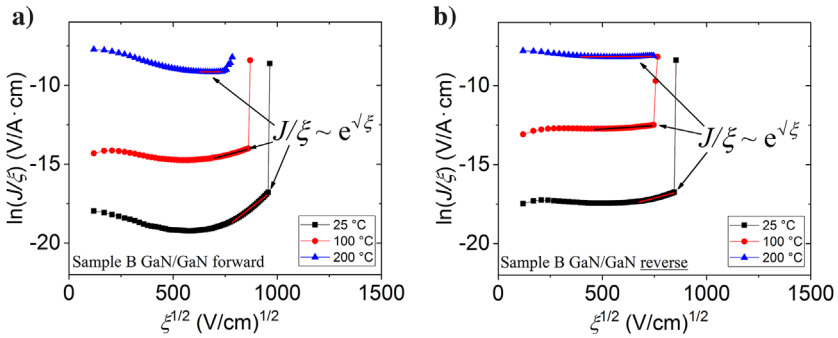

Figure 7. Electric field normalized current density versus square root of the electric field indicating Poole–Frenkel transport (PF) for GaN/GaN sample B measured at forward bias (a) and reverse bias (b).

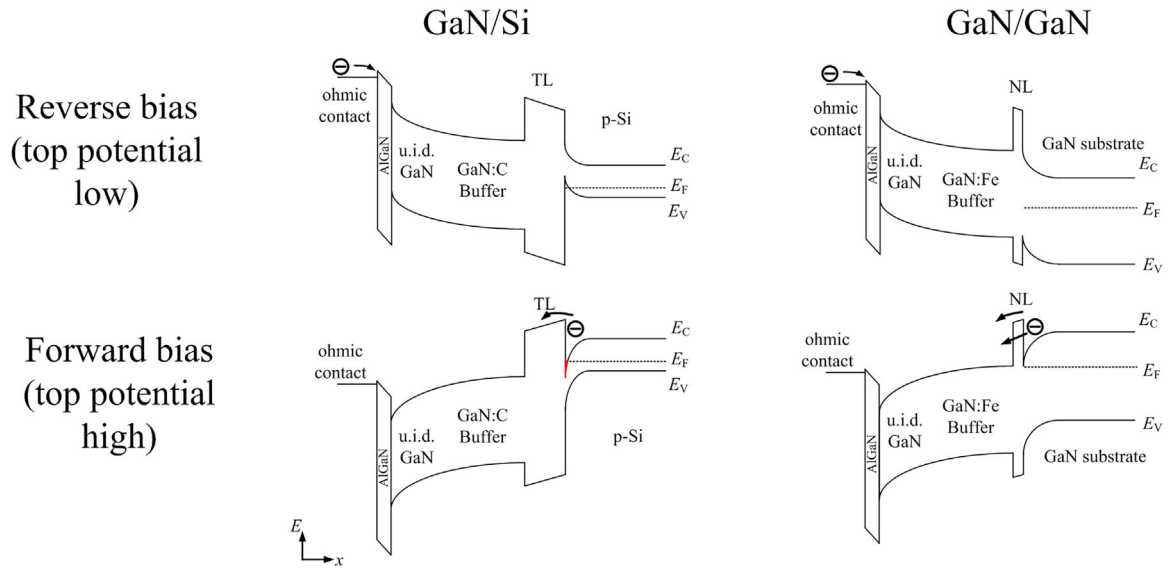

Figure 8. Band diagrams of the associated GaN/Si (left) and GaN/GaN (right) vertical conduction mechanisms at reverse (top) and forward bias (bottom) (TL: transition layer, NL: nucleation layer).

layers, which are lattice- and thermally matched to the GaN substrate. In this case, the disparity of vertical charging/discharging paths for buffer traps might lead to compromises in the dynamic performance. Charges that were trapped under a high-field condition (off-state of the device) cannot be released under a low-field condition (on-state of the device) due to significant reduction of current conduction paths. Considering a GaN Buffer with good insulating properties grown on an insulating GaN substrate this would spread the voltage drop across all layers and interfaces, which is expected to increase the breakdown voltage significantly. This is expected to be observed with optimized buffer compensation and resulting improved isolation properties.

4. Conclusion

The vertical leakage current mechanisms of HEMT grown by MOCVD on Si and GaN substrate in forward and reverse bias were analyzed at temperatures from 25 °C to 200 °C. For the GaN/Si case, a thermally activated vertical conduction with two temperature regimes and activation energies of 0.06 eV and 0.43 eV has been found. In contrast to that, the GaN/GaN case shows a single activation energy of 0.67 eV for the rate-limited vertical conduction, which leads to the conclusion of two trap species that are dominant at different temperature regimes for GaN/Si and only one for GaN/GaN. For a switching application, a single activation energy and therefore predictable behavior across the full temperature range like shown for the GaN/GaN device is beneficial. For forward vertical bias, PF conduction has been identified as the dominant conduction mechanism at higher fields for both substrates. In reverse bias, SCLC and PF conduction have been identified as dominant conduction mechanism for GaN/Si and GaN/GaN, respectively.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

GaN HEMT, GaN substrates, Poole–Frenkel conduction, space charge limited current, temperature dependent vertical current, vertical conduction mechanisms

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