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New determination method of arbitrary energy distribution of traps in metal-oxide-semiconductor field effect transistor

Yoshiki Yonamoto*, Naotoshi Akamatsu

Yokohama Research Laboratory, Hitachi Ltd., Yokohama, Kanagawa 244-0817, Japan

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ABSTRACT

We have developed a highly sensitive method, thermally stimulated voltage recovery (TSVR), to investigate traps responsible for the threshold voltage shift ($\Delta V_{\rm th}$) in gate oxides of metal–oxide–semiconductor field effect transistors (MOSFETs). TSVR provides the contribution of traps with energy level $E_{\rm t}$ to $\Delta V_{\rm th}$ just after trapping events [$\Delta V_{\rm thi}(E_{\rm t})$]. We applied TSVR to stressed MOSFETs with SiO $_2$ gate oxides. The traps with several $E_{\rm t}$ were observed and $\Delta V_{\rm thi}(E_{\rm t})$ showed significant dependence on the gate length, reflecting the influence of fabrication processes on traps.

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1. Introduction

Oxide traps in metal–oxide–semiconductor field effect transistors (MOSFETs) have been investigated extensively because they have significant impacts on the threshold voltage ($V_{\rm th}$) through their carrier trapping/detrapping events. In particular, the estimation of their density ($N_{\rm t}$) and energy ($E_{\rm t}$) has been an important issue for the understanding of device physics and the development of new fabrication processes as well as the improvement of device reliability.

Trap properties are frequently estimated by simple electrical measurements such as capacitance–voltage or discharge transient current measurements on MOS capacitors [1,2]. They are very easy and time-saving methods, while some models or assumptions, e.g., trap distributions inside films [1,2], are required to interpret their observations, making results only qualitative and insufficient for fully understanding of device and trap physics.

For these reasons, we focused on thermally stimulated current (TSC) since it is highly sensitive and provides more accurate $N_{\rm t}$ and $E_{\rm t}$ simultaneously without any models or assumptions. However, applying TSC to MOSFETs is difficult since they are generally too small to detect signals. Also, since $V_{\rm th}$ shift ($\Delta V_{\rm th}$) depends on both trap amounts and locations (see Eq. (1)), the direct relationship between $N_{\rm t}$ and $\Delta V_{\rm th}$ cannot be estimated. Thus, the conventional TSC seems to be inappropriate to examine traps

responsible for $\Delta V_{\rm th}$. Therefore, a new method to overcome these problems has been required.

In this paper, we introduced new method, thermally stimulated voltage recovery (TSVR). The principle of TSVR is similar with that of TSC, but is applicable to MOSFETs. Moreover, TSVR provides directly $E_{\rm t}$ and the contribution of traps with $E_{\rm t}$ to $\Delta V_{\rm th}$ just after trapping events $[\Delta V_{\rm thi}(E_{\rm t})]$. Below, we show the basic principle and application results of TSVR.

2. Theory of TSVR

In this section, we explain the principle of TSVR. Unlike TSC, TSVR measures the temperature dependent $\Delta V_{\rm th}$, i.e., $\Delta V_{\rm th}(T)$, of a MOSFET after charging sequences. $\Delta V_{\rm th}$ depending on $E_{\rm t}$ and T is expressed by the next equation [3]

$$\Delta V_{\rm th}(E_{\rm t},T) = \frac{q}{\epsilon} \int_0^{T_{\rm ox}} x \rho(E_{\rm t},T,x) dx, \tag{1}$$

here q, ϵ , x, $T_{\rm ox}$, and $\rho(E_{\rm t},T,x)$ are the charge quantity, the dielectric constant of a gate insulator film, the distance from a gate, a film thickness, and a trap density distribution. When the MOSFET is heated, trapped charges are emitted. By analogy with the conventional TSC equation [4], the detrapping current $I(E_{\rm t},T,x)$ can be written as

$$I(E_{t}, T, x) = \rho_{i}(E_{t}, x)qv \exp\left[-\frac{E_{t}}{kT} - \frac{v}{\beta} \int_{T_{i}}^{T} \exp\left(-\frac{E_{t}}{kT'}\right) dT'\right]$$

$$= \rho_{i}(E_{t}, x)\theta(E_{t}, T), \tag{2}$$

E-mail address: yoshiki.yonamoto.qh@hitachi.com (Y. Yonamoto).

st Corresponding author.

where β , v, T_i , and $\rho_i(E_t,x)$ represent the heating rate, the attempt-to-frequency, the initial temperature, and the initial trap density distribution just after the charging sequence, respectively. Therefore, $\rho(E_t,T,x)$ is expressed as

$$\rho(E_{\rm t},T,x) = \rho_{\rm i}(E_{\rm t},x) \left\{ 1 - \int_{T_{\rm i}}^{T} \frac{1}{q\beta} \theta(E_{\rm t},T') dT' \right\}. \tag{3}$$

Here we neglect retrapping events. Inserting this into Eq. (1), we obtain

$$\begin{split} \Delta V_{th}(E_t,T) &= \frac{q}{\epsilon} \int_0^{T_{ox}} x \rho_i(E_t,x) \bigg\{ 1 - \int_{T_i}^T \frac{1}{q\beta} \theta(E_t,T') dT' \bigg\} dx \\ &= \Delta V_{thi}(E_t) \bigg\{ 1 - \int_{T_i}^T \frac{1}{q\beta} \theta(E_t,T') dT' \bigg\}, \end{split} \tag{4}$$

where $\Delta V_{thi}(E_t)$ is the initial $\Delta V_{th}(E_t)$ just after the charging sequence. Differentiating by T gives

$$\frac{\partial \Delta V_{\text{th}}(E_{\text{t}}, T)}{\partial T} = \frac{-\Delta V_{\text{thi}}(E_{\text{t}}, T)}{q\beta} \theta(E_{\text{t}}, T). \tag{5}$$

For distributed E_t , this equation becomes

$$\sum_{E_{t}} \frac{\partial \Delta V_{th}(E_{t}, T)}{\partial T} = \frac{\partial \Delta V_{th}(T)}{\partial T} = \sum_{E_{t}} -\frac{\Delta V_{thi}(E_{t})}{q\beta} \theta(E_{t}, T)$$

$$= \sum_{E_{t}} -\Delta V'_{thi}(E_{t}) \theta(E_{t}, T). \tag{6}$$

This equation is very important because this means that the differentiated TSVR signal, $\partial \Delta V_{\rm th}(T)/\partial T$, can be treated in the same way as the conventional TSC (see also Eq. (2)). Referring to the past study, we can estimate $\Delta V_{\rm thi}(E_{\rm t})$ with highly energy resolution using the maximum entropy method (TSC-MEM) [5,6]. Here we describe its principle only briefly. Below, we denote $\partial \Delta V_{\rm th}(T)/\partial T$ as $\xi(T)$ for simplicity. In order to apply MEM to TSVR, we normalize $\xi(T)$ and $\Delta V'_{\rm thi}(E_{\rm t})$ by P as the following equation.

$$\xi'(T) = \frac{\xi(T)}{P} = \sum_{E_t} -\frac{\Delta V'_{thi}(E_t)}{P} \theta(E_t, T) = \sum_{E_t} -\Delta V''_{thi}(E_t) \theta(E_t, T). \quad (7)$$

P can be easily obtained from the next equation.

$$P = \sum_{E} \Delta V'_{\text{thi}}(E_{\text{t}}) = \sum_{T} \xi(T). \tag{8}$$

Using Eq. (7), the MEM basic equations can be expressed as

$$\chi^2 = \sum_{\tau} \frac{\left\{ \xi'(T) - \xi'(T)_{\text{MEM}} \right\}^2}{\sigma_{\ell}^2}, \tag{9}$$

$$S = -\sum_{E_t} \biggl\{ \Delta V_{thi}''(E_t) \, ln \left[\frac{\Delta V_{thi}''(E_t)}{D_t'(E_t)} \right] + D_t'(E_t) - \Delta V_{thi}''(E_t) \biggr\}, \eqno(10)$$

and

$$F = \frac{\chi^2}{2} - \alpha S,\tag{11}$$

where $\sigma_\ell^2, D_t'(E_t)$, and α correspond to experimental errors, a default function, and the Lagrange parameter determined by the theory described in Ref. [5]. The $\Delta V_{\text{thi}}''(E_t)$ minimizing F becomes the most probable $\Delta V_{\text{thi}}''(E_t)$. With Eq. (7) and P obtained by Eq. (8), $\Delta V_{\text{thi}}(E_t)$ can be determined. Note that $\Delta V_{\text{thi}}''(E_t)$ and $D_t'(E_t)$ satisfy next constraints required for using MEM [5].

$$\sum_{E_{t}} \Delta V_{thi}''(E_{t}) = \sum_{E_{t}} D_{t}'(E_{t}) = 1, \tag{12}$$

$$\Delta V_{thi}''(E_t) \geqslant 0, \ D_t'(E_t) \geqslant 0. \tag{13}$$

The default parameter $D_t'(E_t)$ in Eq. (10) is arbitrary as long as it satisfies Eqs. (12) and (13), i.e., this method requires no initial assumed model for $\Delta V_{\text{thi}}(E_t)$. Actually, we tested several $D_t'(E_t)$ such as constant, gauss, and exponential functions and confirmed that obtained $\Delta V_{\text{thi}}(E_t)$ are coincident within 2.5% (sufficiently smaller than experimental errors). While, the computing time considerably depends on the assumed $D_t'(E_t)$. Comparing with the constant function, the exponential (gauss) function takes about twice (1.5 times). Therefore, we used constant $D_t'(E_t)$ below.

A great care has to be taken to determine v in Eq. (2) since v is a very critical parameter to quantify E_t . According to Ref. [7], v is generally between 10¹⁰ and 10¹²/s. On the other hand, it was pointed out from the results of TSC and isochronal annealing experiments that it significantly depends on the bias imposed during measurements and can vary from 10⁵ to 10¹³/s due to the compensating carriers [8-11]. Also, the isothermal and isochronal annealing experiments under the zero bias condition provided relatively small v, $10^7/s$ [12]. These fact suggest that the experimental conditions, especially the bias, have to be taken into consideration for the determination of v. Therefore, v under our experimental conditions has to be determined carefully. For this reason, we performed additional isothermal experiments and obtained $v = 3 \times 10^{11}/s$. Though detailed explanations about the determination of v will be described in the last section, we use this value in the calculations below.

3. Experimental

Samples are n-type MOSFETs with 8 nm thickness SiO_2 gate insulators. Their gate length/width (W/L) are 40/40, 40/5 and 40/1 μ m. The reason for choosing them is that they are relatively large and can be regarded as the reference system. They seem to be suitable for demonstration of TSVR validity. Noted that though we tried the conventional TSC experiments, no signal was detected because of the poor sensitivity of it (figures not shown). Also, they are typical sizes for devices such as thin-film-transistors and power devices. Moreover, we are interested in the gate size dependence of traps reflecting influences of fabrication processes. If it is observed, it provides very critical information for the improvement of processes. Therefore, we prepared MOSFETs with various gate sizes.

Before TSVR measurements, the MOSFET was subjected to the Fowler–Norldheim stress (10 MV/cm, 300 K, and 30 s). To measure the background signal, unstressed MOSFET was also prepared. During $V_{\rm th}(T)$ measurements, the drain, source, and substrate voltages were fixed at 0.2, 0, and 0 V, respectively. Here we defined the temperature dependent gate voltage giving the constant drain current (1 \times 10⁻⁶ A) as $V_{\rm th}(T)$. To reduce noises, all the measurements were performed inside the closed chamber filled with He gas and all electrodes were connected to equipment with an Al wire bonding technique. $V_{\rm th}(T)$ were recorded from 300 to 573 K with β = 0.15 K/s.

The TSVR signal is the temperature dependent $\Delta V_{\rm th}$ ($\Delta V_{\rm th}(T)$) of a MOSFET after a charging sequence. The emission of trapped carriers by the thermal energy induces $\Delta V_{\rm th}$. Meanwhile, $V_{\rm th}(T)$ depends on temperature intrinsically. We therefore obtained $\Delta V_{\rm th}(T)$ by subtracting $V_{\rm th}(T)$ of unstressed MOSFETs from $V_{\rm th}(T)$ of stressed ones.

4. Results and discussions

Fig. 1 shows $V_{\rm th}(T)$ of stressed/unstressed MOSFETs W/L = 40/40 µm) and their difference, $\Delta V_{\rm th}(T)$ (TSVR signal). $\Delta V_{\rm th}(T)$ depending on L are plotted in Fig. 2. $\Delta V_{\rm th}(T)$ at 300 K ($\Delta V_{\rm thi}$) is about 150 mV. This originates from the initial trapped charges by the

stress. $\Delta V_{\rm th}(T)$ decreases with T due to detrapping events. One easily sees that four regions are present in $\Delta V_{\rm th}(T)$. In the A and C regions, the temperature dependences of $\Delta V_{\rm th}(T)$ is relatively small. Meanwhile, the B and D regions show large dependences. These mean that little (considerable) detrapping events occur in the former (latter) regions. $\Delta V_{\rm th}(T)$ becomes close to zero at 573 K. From this fact, we expect that most of the trapped carriers were emitted by 573 K.

The differentiated TSVR signal, $\partial \Delta V_{\rm th}(T)/\partial T$, calculated from $\Delta V_{\rm th}(T)$ is illustrated in Fig. 3. To improve the signal-to-noise ratio, we repeated same measurements by eight times and averaged them. $\partial \Delta V_{\rm th}(T)/\partial T$ shows two peaks at around 350 and 520 K. As described above, $\partial \Delta V_{\rm th}(T)/\partial T$ can be treated in the same way as the conventional TSC. Accordingly, our data can be compared with the previous TSC spectra of SiO₂. Our spectrum quite resembles TSC data of irradiated SiO₂ films [8,11,13]. They observed two traps and attributed them to E_δ and E_γ' [13]. Therefore, peaks in our spectrum could correspond to them.

We applied the TSC-MEM method to these $\partial \Delta V_{\rm th}(T)/\partial T$ in order to obtain $\Delta V_{\rm thi}(E_{\rm t})$. The reproduced curves by the TSC-MEM and obtained $\Delta V_{\rm thi}(E_{\rm t})$ are shown in Figs. 3 and 4a, respectively.

Here, the accuracy of these results should be mentioned. In the previous study, the TSC-MEM results of SiO_2 films showed much more complicated fine structures [6]. On the other hand, $\Delta V_{thi}(E_t)$ in the present study are relatively structureless. This is due to the noises in $\partial \Delta V_{th}(T)/\partial T$. Since $\partial \Delta V_{th}(T)/\partial T$ is obtained by differentiating $\Delta V_{th}(T)$ by T, it is very sensitive to noises in $\Delta V_{th}(T)$. The noises can mask fine structures in $\partial \Delta V_{th}(T)/\partial T$ even if they are present. This makes obtained $\Delta V_{thi}(E_t)$ from the TSC-MEM structureless. So, in this sense, our $\Delta V_{thi}(E_t)$ might be absolutely inaccurate, however, we think that they can reflect the differences in trap properties in each MOSFETs at least because the TSC-MEM method reproduces experimental $\partial \Delta V_{th}(T)/\partial T$ well as seen in Fig 3.

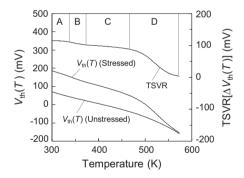


Fig. 1. $V_{th}(T)$ of FN stressed/unstressed MOSFETs ($W/L = 40/40 \ \mu m$) and its TSVR signal (their difference, $\Delta V_{th}(T)$).

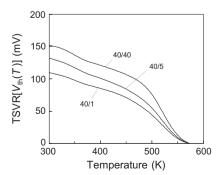


Fig. 2. L dependence of TSVR signals measured on MOSFETs. Their W/L are 40/40, 40/5, and 40/1 μm .

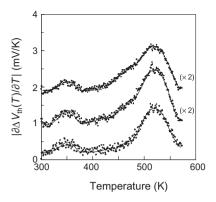


Fig. 3. Differentiated TSVR signals $(\partial \Delta V_{th}(T)/\partial T)$ of MOSFETs (circles) and curves reproduced using TSC-MEM method (solid lines). From bottom to top, their W/L are 40/40, 40/5, and 40/1 μ m, respectively. The data of W/L = 40/5 and 40/1 μ m are offset for clarity.

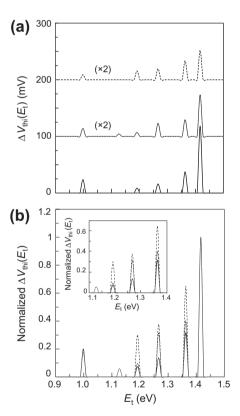


Fig. 4. (a) $\Delta V_{\rm thi}(E_{\rm t})$ of MOSFETs. Solid, dotted, and dashed lines correspond to W/L = 40/40, 40/5, and $40/1~\mu m$. Data of W/L = 40/5 and $40/1~\mu m$ are offset for clarity. (b) $\Delta V_{\rm thi}(E_{\rm t})$ normalized by 1.4 eV peak intensity. Solid, dotted, and dashed lines are the same as (a). Inset figure in (b) normalized $\Delta V_{\rm thi}(E_{\rm t})$ between 1.1 and 1.4 eV region

In Fig. 4a, some distinct peaks are seen. Peaks at around 1.0 and 1.4 eV correspond to ones centered at around 350 and 520 K in $\partial \Delta V_{\rm th}(T)/\partial T$. Furthermore, some additional peaks at around 1.2, 1.25, and 1.35 eV are observed. 1.12 eV peak present only in the $W/L=40/5~\mu m$ MOSFET could be due to the noises since it is absent in other MOSFETs. The presence of additional peaks is reflected in the peak widths in $\partial \Delta V_{\rm th}(T)/\partial T$. It should be also mentioned that our stresses might not full all traps. Accordingly, the absolute intensities of $\Delta V_{\rm thi}(E_{\rm t})$ peaks cannot be compared, however, we think that normalized peak intensities are comparable.

The normalized $\Delta V_{\text{thi}}(E_t)$ by 1.4 eV peak intensities are shown in Fig. 4b. There are some interesting features in this figure. Firstly, the negligible L dependence of 1.0 eV peak intensity is seen. This means that 1.0 eV and 1.4 eV traps have the same *L* dependence. Secondly, the additional peaks at 1.2, 1.25, and 1.35 eV significantly depend on L. For shorter L, they increase more and more. These characteristics give us some clues about the process effects on traps. We speculate that the implantation or etching process damages during the fabrication of drain/source regions cause the formation of the additional traps near the edges of SiO₂ films. With decreasing L, their relative contributions to $\Delta V_{\text{thi}}(E_{\text{t}})$ increase when 1.0 and 1.4 eV traps are present uniformly in the L direction, i.e., these traps are intrinsic and irrelevant to process damages. Although it is impossible to determine detailed formation mechanisms by TSVR alone and more studies are required, the appearance of the additional peaks is interesting phenomenon and can be a clue to improve $V_{\rm th}$ instability in MOSFETs. Note that we tried to detect traps by the TSC method, but failed because of its poor sensitivity, proving the high sensitivity of the TSVR method.

It also should be mentioned that besides bulk traps, the recovery of interface states could affect $\partial \Delta V_{th}(T)/\partial T$ [14,15]. The amount of interface states increased by $\approx 3 \times 10^{10} / \text{cm}^2$ after the stress and they recovered to undetectable level after the TSVR measurements. Therefore, the recovery component is involved in $\partial \Delta V_{th}(T)/\partial T$. Its contribution to ΔV_{th} can be approximately estimated to be 10 mV [11]. Because this is much smaller in comparison with $\Delta V_{\rm thi}$, we neglected it in this study for simplicity. Although main components dominating ΔV_{thi} are determined, more studies and improved theory are required to examine the influence of interface

Here, let us describe the details of the determination of v. We analyzed the TSVR spectrum ($W/L = 40/40 \,\mu\text{m}$) with various v. Fig. 5a shows E_t of the main peaks as a function of v. E_t depends on v ($\partial E_t/\partial \log(v) \cong 0.1$), which means that v is a very critical for $E_{\rm t}$. To determine reliable v, additional isothermal $\Delta V_{\rm th}(t)$ decay experiments were performed [9,12,16]. Results are shown in Fig. 5b. Symbols are experimental $\Delta V_{\rm th}(t)(\Delta V_{\rm th}^{\rm exp.}(t))$ as a function of the annealing times after stressing. Note that since v strongly depends on the bias during annealings as shown in Table 1 [9,12], the bias in our experiments was kept at the same conditions with TSVR experiments. Lines correspond to $\Delta V_{\rm th}(t) \left(\Delta V_{\rm th}^{\rm calc.}(t,v) \right)$ calculated using the next equations.

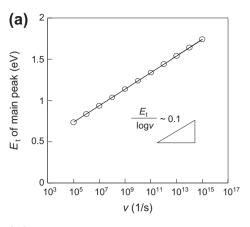
$$\Delta V_{\rm th}^{\rm calc.}(t,\nu) = \int_0^\infty \Delta V_{\rm thi}(E_{\rm t},\nu) \exp\{-e_{\rm p}(E_{\rm t},\nu)t\} dE_{\rm t}, \tag{14}$$

$$e_{\rm p}(E_{\rm t}, \nu) = \nu \exp\left(\frac{-E_{\rm t}}{kT}\right).$$
 (15)

v dependent $\Delta V_{\text{th}}^{\text{calc.}}(t,v)$ can be calculated from $V_{\text{thi}}(E_{\text{t}},v)$ determined by the TSVR curve and the assumed v. Although calculations were carried out with various v, only calculated curves with $v = 3 \times 10^{11}$ s are shown in Fig. 5b for clarity. The inset figure in Fig. 5b shows the differences between calculated and experimental $\Delta V_{
m th}(t)$ as a function of assumed $v\left(R = \sum \left[\Delta V_{\text{th}}^{\text{calc.}}(t, v) - \Delta V_{\text{th}}^{\text{exp.}}(t)\right]^2\right)$. Fitting

them with a quadratic function, we obtained $v \approx 3 \times 10^{11}/\text{s}$.

In principle, v can be expected to be $v \approx 10^{13}/\text{s}$ (SiO₂ phonon frequency). Our value is smaller, however, it is not surprising if one takes into consideration the fact that compensating carriers induced by the bias can stabilize the trapped carriers and make ν smaller as suggested previously [8-11]. Actually, they observed the significant dependence of v the bias and showed that v can vary from 10^5 to 10^{13} /s as seen in Table 1. In our case, the same stabilization can make v smaller than 10^{13} /s. In this sense, our results



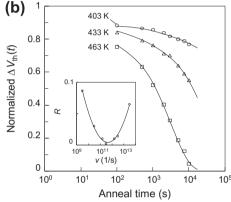


Fig. 5. (a) v dependent E_t of the main peak in TSVR of MOSFET ($W/L = 40/40 \mu m$). (b) Experimental $\Delta V_{\text{th}}^{\text{exp.}}(t)$ (symbols) and calculated $\Delta V_{\text{th}}^{\text{calc.}}(t, v)$ with $v = 3 \times 10^{11}/\text{s}$ (lines). The isothermal annealing temperatures are 403, 433, and 463 K. In the inset figure, circles show the differences between $\Delta V_{\rm th}^{\rm exp.}(t)$ and $\Delta V_{\rm th}^{\rm calc.}(t,\nu)$. The solid line is the result of the curve fitting using a quadratic function. For more details, see the

reflect not the "pure" detrapping phenomenon, but the "effective" one including the influence of the stabilization. However, the "effective" does not mean disadvantage because it reflects the instability of $\Delta V_{\rm th}$ under MOSFET operating conditions. Therefore, our experimental and analytical schemes can provide useful information from the technological view.

One more question is the validity of our v and energy scale. As seen in Table 1, Saigné's and our v are smaller than ones under the negative bias condition. It can be due to the compensating carriers and reasonable, however, they are different by four orders (1 \times 10⁷ and 3×10^{11} /s). This discrepancy cannot be explained only by the compensating carriers. Flament et al. commented that under the zero bias conditions, the electron tunneling processes play a key role in trapped hole detrappings [9]. If this is true in our case, our isothermal annealing curves in Fig. 5b include the contributions of the tunneling processes as well as the thermal detrappings. In other words, the decrease of $\Delta V_{\rm th}(t)$ becomes steeper than one determined by only thermal detrappings. Since Eq. (14) neglects

Table 1 The bias dependent v in previous papers and this study. Superscripts a and b are values in Refs. [9,12]. Values in "Net charges" and "Trapped carrier" mean the "effective" and the "pure" in the text, respectively.

| | υ(/s) | | | |
|-------------------------------|--------------------|------------------|---------------------|---------------------|
| Electric field (MV/cm) | -2.2 | -0.2 | 0 | +2.2 |
| Net charges ^{a,b} | $3\times10^{13,a}$ | | $1 \times 10^{7,b}$ | $3 \times 10^{5,a}$ |
| Trapped carriers ^a | $3\times10^{13,a}$ | _ | _a | _ ^a |
| This study | - | 3×10^{11} | - | - |

the tunneling contribution, the thermal detrapping probability can be overestimated, which makes v larger.

Unfortunately, though the gate SiO_2 thickness in the Saigné's MOSFET is unknown, it can be expected to be much more thicker than ours from their devices and experimental conditions (e.g., they imposed 9 V bias which is too large for our SiO_2 , only 8 nm thickness) [12]. In this case, ours can be much more susceptible to the tunneling processes since the tunneling probability considerably depends on the distance between the SiO_2/Si interface and trapped charge position. As a result, our v is estimated to be larger than Saigné's. To confirm this point, additional TSVR, TSC, isothermal, and isochronal experiments on MOSFETs with various SiO_2 thickness would be very helpful. We have a plan to perform these experiments and results will be published elsewhere.

Regarding the energy scale, the main peak energy in Fig. 4 (\approx 1.4 eV) are in good agreement with one in the previous report (Fig. 1 in Ref. [11]). 1.47 eV observed by Dusseau et al. is also almost coincidence with ours [16]. From these facts, we think that our energy scale is valid at least under our experimental condition. Note that in our analysis, the barrier lowering effect has been ignored since the bias is sufficiently small. If experiments are performed under the strong bias, one has to take it into consideration. However, even in that case, our method is valid and $\Delta V_{\rm thi}(E_{\rm t})$ can be estimated in the similar manner.

This method needs a great care, however, is very powerful tool. It allows one to determine $\Delta V_{\rm thi}(E_{\rm t})$ with highly energy resolution. Furthermore, it can be applied to any MOSFETs, even modern submicron-size MOSFETs, as long as $V_{\rm th}$ is observable. Although there have been some unsolved questions about its detailed principles, we expect that this method can shed light on the mechanism of $V_{\rm th}$ instability induced by various factors such as fabrication processes, stressing, or irradiation.

5. Conclusion

In conclusion, we have investigated traps responsible for $\Delta V_{\rm th}$ in MOSFETs using TSVR and MEM. It successfully provided $\Delta V_{\rm thi}(E_{\rm t})$ with high sensitivity. Main traps responsible for $\Delta V_{\rm thi}$ are determined to be 1.0 and 1.4 eV traps. Some additional traps are present and they show significant L dependences. This method was proven to be very useful for device characterizations, however, more investigations including the influence of interface states and tunneling processes are required.

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