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The analysis of lateral distribution of barrier height in identically prepared Co/*n*-Si Schottky diodes

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ABSTRACT

We have studied the experimental linear relationship between ideality factors and barrier heights (BHs) for Co/*n*-Si metal–semiconductor (MS) structures with a doping density of about 10^{15} cm^{-3}. The barrier heights for the Co/*n*-type Si metal–semiconductor structures from the current–voltage (*I–V*) characteristics varied from 0.64 to 0.70 eV, the ideality factor *n* varied from 1.18 to 1.26, and from reverse bias capacitance–voltage (C^{-2}–*V*) characteristics the barrier height varied from 0.68 to 0.81 eV. The experimental barrier height distributions obtained from the *I–V* and C^{-2}–*V* characteristics were fitted by a Gaussian distribution function, and their mean values were found to be 0.67 and 0.75 eV, respectively. Furthermore, the lateral homogeneous BH value of approximately 0.81 eV for Co/*n*-Si metal–semiconductor structures was obtained from the linear relationship between experimental effective BHs and ideality factors.

1. Introduction

Metal–semiconductor (MS) structures have been studied extensively because of their importance in direct current and microwave applications and as tools in the analysis of other fundamental physical parameters [1,2]. Although Schottky interfaces have been well studied for over 50 years, it is only in the past two decades that an inhomogeous contact has been considered as an explanation for a voltage-dependent barrier height (BH) [2–4]. Interface states and an interfacial oxide layer at a MS contact play an important role in the determination of the Schottky barrier height. The barrier height is likely to be a function of the interface atomic structure, and the atomic inhomogeneities at MS interface which are caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases, etc. [5,6]. Since the reliability and stability of all semiconductor devices are intimately related to their surface conditions, an understanding of the surface physics with the help of MIS diodes is of great importance to device operations [1–3]. The Si (1 0 0) surface is the particularly applied in semiconductor device technology [1,2,7].

MS structures are frequently used in integrated circuits, e.g. as gates in metal–semiconductor field-effect transistors (MESFETs) or the metal-oxide–semiconductor field-effect transistor (MOSFET), in light detectors and as solar cells. MS structures are among the simplest MS contact devices [1–9]. The popularity of such studies rooted in their importance to the insulator layer between metal and semiconductor. Because the existence of such an interfacial insulator layer converts the MS diodes to MIS type diodes and can have strong influence on the device characteristics as well as the interface states density, Schottky barrier height (SBH) and ideality factor [10–21]. The most important feature characterizing a MS is its barrier height. The electronic property of such structures (Schottky barrier diodes-MS) is characterized by its barrier height and ideality factor. In spite of the numerous applications of Schottky barriers, the factors controlling the BHs are not completely understood [1–10]. The barrier heights are important parameters that determine the electrical characteristics of MS diodes. At a metal/*n*-type semiconductor interface, the SBH is the difference between the highest point of conduction band edge and the Fermi level [1,2,17].

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Thus, provided the semiconductor substrate is well characterized then the homogeneous Schottky BH may be obtained even from the *I–V* characteristics of one contact.

Electrodeposition method has been used for the formation of Co/*n*-Si Schottky diodes (SD). Among the different methods available for metallization of Si surfaces, vacuum deposition is the usual metallization method, and electrodeposition also is an interesting method due to its valuable advantages such as the possibility of metal deposition at low temperature with low costs. Moreover, electrodeposition method provides the possibility of depositing film structures different from those being produced from the vapour phase. For example, the electrodeposition method does not require a pretreatment to activate the surface [22–25]. The electrodeposition is an advantageous alternative to the common expensive physical technologies for the metallization of semiconductors and it is useful to avoid passivation processes occurring during the deposition process [22–25]. In addition, this technique can be preferred for metals such as Ni, Co, etc. which are very difficult to be evaporated by the vacuum deposition.

Some authors have been able to account for much of the observed non-ideal behaviour by assuming certain distributions of microscopic barrier heights for the different diodes [4–8,10,26–28], and pointed out that the BH inhomogeneity model would also explained the linear relationship between effective BHs and ideality factors that is often observed on sets of the identically prepared diodes [27–35]. It has been developed the idea that non-ideal behaviour in the Schottky barrier diodes (SBD) could be quantitatively explained by assuming specific distribution of nanometer-scale interfacial patches (small regions) with lower BH than the junction's main BH [27,28]. In such cases, the current across the MS contact may be greatly influenced by the presence of the BH inhomogeneity [4,8,27,28]. Tung [27] and Sullivan et al. [28] have modelled imperfect Schottky structures by assuming lateral variations of the barrier height. They found larger ideality factors and smaller effective barrier heights when they increased the inhomogeneity of barriers.

In this study, our purpose is to experimentally investigate the relationship between the effective BHs and ideality factors obtained from the forward bias *I–V* and reverse bias *C–V* characteristics of the Co/*n*-Si Schottky diodes. The homogeneous barrier height value for the device was obtained from the linear relationship between the experimental effective barrier heights and ideality factors. This homogeneous BH value is important, which is the real meaningful value characteristic for the MS systems, which should be used to develop theories of physical mechanisms determining these BHs about Schottky contacts [34]. The statistical distribution of the characteristics parameters of the structures was made by means of the Gaussian function.

2. Experimental procedures

The MS Schottky diodes were prepared using one side polished (as received from the manufacturer) *n*-type Si wafers with (1 0 0) orientation and 1.26×10^{15} cm^{-3} carrier concentration from *C–V* measurements in this study. The wafers were chemically cleaned using the RCA cleaning procedure [i.e., a 10 min boil in $NH_4OH + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$]. The native oxide on the front surface of the substrate was removed in HF:H_2O (1:10) solution and finally the wafer was rinsed in de-ionized water for 30 s. Then, low resistivity ohmic back contact to *n*-type Si wafer was made by using Au-Sb alloy, followed by a temperature treatment at 420 °C for 3 min in N_2 atmosphere. The Schottky structures were formed on the front face of the *n*-Si as dots with diameter of about 1 mm (the diode area = 7.85×10^{-3} cm^2) by the galvanostatic electrodeposition of Co. An acid-resistant adhesive tape was used to mask off all the substrate except for the deposition area. The electrodeposition of Co films on *n*-type Si substrate has been carried out at room temperature from an aqueous electrolyte containing 1 M Co sulphate and 0.5 M boric acid. The *n*-Si substrate was used as cathode while a Pt plate was anode. A current density of 3 mA/cm^2 was maintained between the two electrodes. Film thickness was determined as 150 nm by deposition time. The current–voltage and capacitance–voltage characteristics were measured using a Keithley 487 Picoammeter/Voltage Source and a HP model 4192A LF Impedance analyser (5 Hz–13 MHz), respectively, at room temperature in dark conditions. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussion

Fig. 1 shows both forward and reverse bias *I–V* characteristics of the Co/*n*-type Si Schottky structure. It is assumed that the current in MS structures is due to thermionic emission current and it can be expressed by [1,2]

$$I = I_o \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

where I_o is the saturation current derived from the straight line intercept of ln *I* at *V* = 0 and is given by

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (2)$$

Φ_b is the zero bias effective Schottky barrier height, A^* is the effective Richardson constant and equals to 112 *A*/cm^2 K^2 for *n*-type Si [10], *A* is the diode area and *n* is an ideality factor which is a measure of conformity of the diode to pure thermionic emission. It is obtained from the slope of the straight line region of the forward bias ln *I–V* characteristics through the relation;

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

ideality factor, *n*, which is equal to 1 for an ideal diode has usually a value greater than unity. 10 dots (Schottky structures) for the Co/*n*-type Si were fabricated on the same *n*-type Si semiconductor substrate by electrodeposition of Co. From Eq. (2) the barrier height, Φ_b is given by;

$$\Phi_b = \frac{kT}{q}\ln\left(\frac{A^*AT^2}{I_0}\right) \quad (4)$$

Using the Eq. (3), the values of ideality factor (*n*) were determined between 1.18 and 1.26, and using the Eq. (4), the values of barrier height (Φ_b) were determined between 0.64 and 0.70 eV. As can be seen from the data, the effective BHs and ideality factors

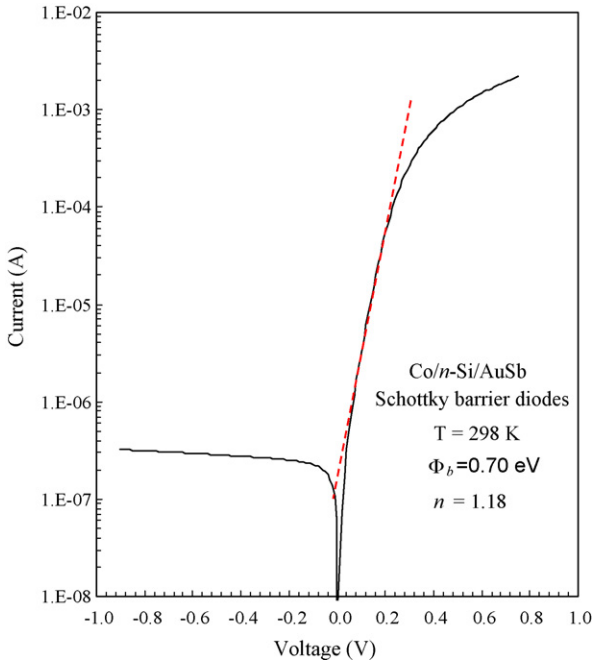

Fig. 1. The experimental forward and reverse bias current versus voltage characteristics of one of the Co/*n*-type Si Schottky structures at room temperature.

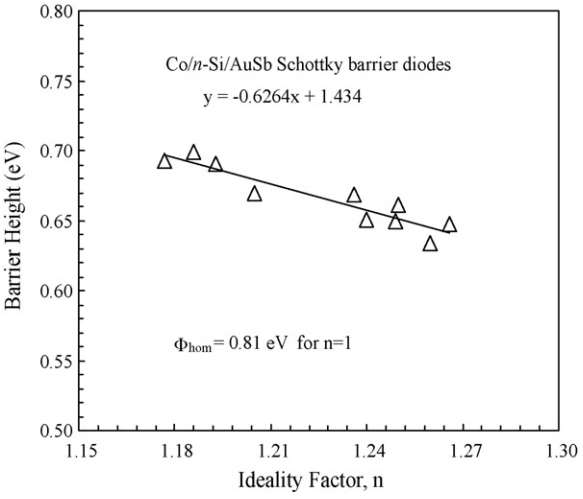

Fig. 2. The plot of experimental barrier height versus ideality factor of the Co/*n*-type Si Schottky structures at room temperature.

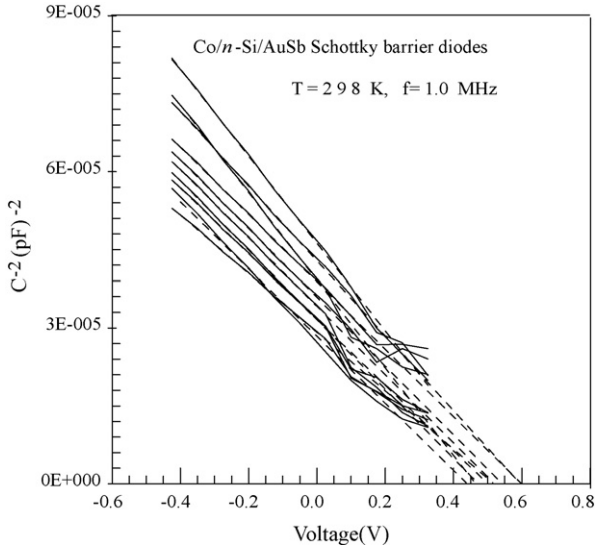

Fig. 3. Reverse bias C^{-2}–V characteristics of the Co/*n*-type Si Schottky structures at a frequency of 1.0 MHz and room temperature.

from I–V characteristics varied from diode to diode even if they are identically prepared. This finding indicates that the potential barriers at real MS interfaces depend much more strongly on the applied voltage than predicted by the image-force effect for ideal contacts. Therefore, it is common practice to take averages [29–33].

Fig. 2 shows the experimental barrier heights versus the ideality factors plot at room temperature. As can be seen from Fig. 2, there is a linear relationship between experimental effective BHs and ideality factors of Schottky structures. Therefore, there is a linear relationship between experimental effective BHs and ideality factors of the electrodeposited Co/*n*-Si Schottky barrier diodes. That is, the barrier heights become smaller as the ideality factors increase. This finding may be attributed to lateral barrier inhomogeneities of in Schottky diodes [28–36]. It has been mentioned that higher ideality factors among identically prepared diodes were often found to accompany lower observed barrier heights. A laterally homogeneous barrier height value of 0.81 eV for the electrodeposited Co/*n*-Si Schottky structures was obtained from the linear relationship between experimental effective BHs and ideality factors in Fig. 2. The homogeneous BH of 0.81 eV for the electrodeposited Co/*n*-Si MS formed by us is close to value of 0.82 eV by Sağlam et al. [37]. In addition, the homogeneous barrier height value of 0.81 eV is larger than value of 0.67 eV given for the vacuum-deposited *n*-Si MS in reference [2]. Forment et al. [22] reported that the barrier height was higher for the electrochemically deposited structures than for the vacuum evaporated ones. According to reference [22], the difference in barrier height between electrochemically deposited and evaporated structures can be explained by the presence of a dipole layer containing oxygen at the MS interface of the electrochemically formed structures.

As mentioned above, the lateral inhomogeneous distribution of barrier heights at the interface may be caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases, etc. [28–35]. Ideality factors between 1.01 and 1.02 can be expected due to image-force lowering of the Schottky barrier at the interface. Our data clearly show that the diodes have ideality factors that are considerably larger than the value determined by the image-force effect only. Therefore, these diodes are patchy [29,30,38]. The larger values of ideality factors are attributed to secondary mechanisms at the interface [1,2,6,26,27,31,38]. For example, interface defects may lead to a lateral inhomogenous distribution of barrier heights at the interface which results in larger ideality factors, and the charge transport across the interface only is no longer due to thermionic emission. As seen from the explanations above, the inhomogeneities may play an important role and have to be considered in the evaluation of experimental I–V characteristics. According to Tung [27], the high values of n can be attributed to the presence of a wide distribution of low-SBH patches caused by laterally barrier inhomogeneous.

In Schottky diodes, the depletion layer capacitance, capacitance (C) can be expressed as [1,2]:

$$\frac{1}{C^2} = \frac{2(V_0 - V)}{q\varepsilon_s\varepsilon_0 A^2 N_D} \quad (5)$$

where A is the area of the diode, V_0 is the diffusion potential at zero bias and is determined from the extrapolation of the linear C^{-2}–V plot to the V axis, ε_s is the dielectric constant of the semiconductor (=11.8 for Si) [1,2], ε_0 is the dielectric constant of vacuum (8.85×10^{-14} F/m), and N_D is the donor concentration of n-type semiconductor substrate. The plots of C^{-2}–V as a function of reverse bias voltage are linear that indicates the formation of SDs [25]. With the help of Eq. (5), the values of V_0 and N_D can be determined from the intercept and slope of the C^{-2}–V plot. Fig. 3 shows the room temperature reverse bias C^{-2}–V characteristics of the Co/*n*-Si Schottky structures (10 dots) at 1 MHz.

According to Eq. (5), and as can be seen from Fig. 3, the C^{-2}–V plot is a straight line whose intercept with the V axis gives the value of V_0. The value of the barrier height $\Phi_b(CV)$ can be calculated by the following well-known equation, using C–V measurements,

$$\Phi_b(CV) = \left(V_i + \frac{kT}{q}\right) + kT\ln\left(\frac{N_V}{N_A}\right) - \Delta\Phi_b = V_0 + E_F - \Delta\Phi_b \quad (6)$$

where E_F is the Fermi energy. The $\Phi_b(CV)$ for the Co/*n*-Si Schottky structures ranged from 0.68 to 0.81 eV, *Vi* is the intercept point of V axis from C^{-2}–V curve, and $\Delta\Phi_b$ is the image-force alone causes barrier lowering. As can be seen, the experimental effective BHs obtained from the C–V characteristics can differ from diode to diode. Therefore, as mentioned above, their averages should be taken [29–33,38].

Fig. 4 shows the statistical distribution of BHs from the forward bias I–V plots of the Co/*n*-Si MS structures (10 dots) and Fig. 5 shows the statistical distribution of BHs from the reverse bias C^{-2}–V plots of the same diodes. The experimental distributions of the effective BHs were fitted by the Gaussian function. At first, let us consider the I–V BHs. The statistical analysis yielded a mean BH value of 0.67 eV with a standard deviation of 0.02 eV. In the distribution of the BHs from the reverse bias C^{-2}–V characteristics of the Co/*n*-Si

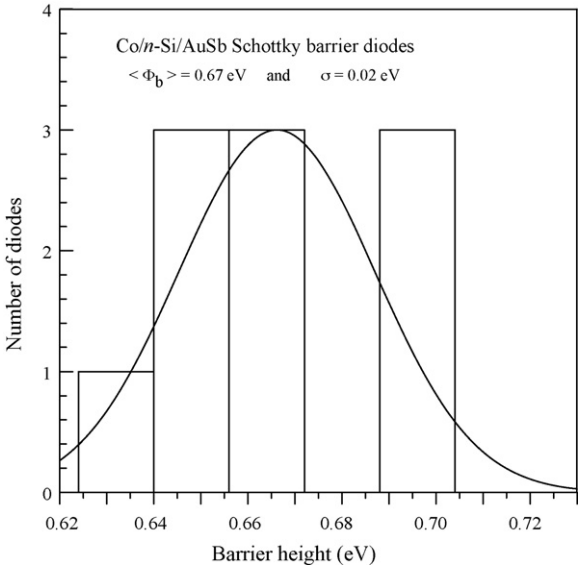

Fig. 4. Gaussian distribution of barrier heights from the forward bias *I–V* characteristics of the Co/*n*-type Si Schottky structures at room temperature. The Gaussian fits yields $\bar{\Phi}_b = 0.67$ eV and $\sigma = 0.02$ eV for the barrier heights.

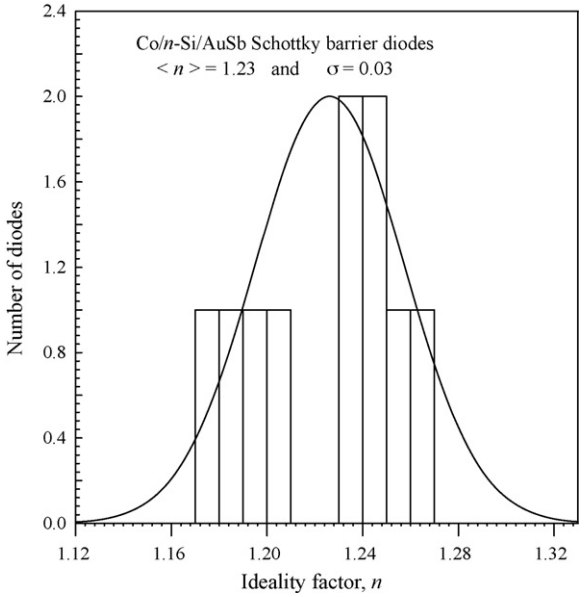

Fig. 6. Gaussian distribution of ideality factor from the forward bias *I–V* characteristics of the Co/*n*-type Si Schottky structures at room temperature. $\bar{n} = 1.23$ eV and $\sigma = 0.03$ for the ideality factors.

SDs at 1.0 MHz (Fig. 5), and the statistical analysis yielded a mean BH value of 0.75 eV with a standard deviation of 0.04 eV. The difference between the mean SBH values obtained from C^{-2}–*V* and *I–V* (0.08 eV) characteristics is larger than the image-force lowering value of 0.013 eV for this device. The image-force lowering value for the barrier height was determined by using Eq. (3.31) according to reference [1]. Due to the different nature of the C^{-2}–*V* and *I–V* measurement techniques, barrier heights deduced from them are not always the same. When the difference in SBH approaches zero, the potential profiles approach a uniform barrier height. In the distribution of the ideality factors from the forward bias *I–V* characteristics of the Co/*n*-Si Schottky structures (Fig. 6), the Gaussian fit yields a mean ideality factor value of 1.23 with a standard deviation of 0.03.

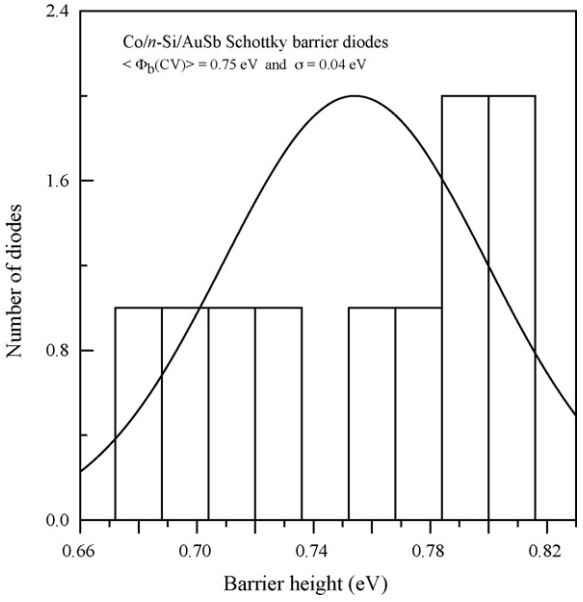

Fig. 5. Gaussian distribution of barrier heights from the reverse C^{-2}–*V* characteristics of the Co/*n*-type Si Schottky structures at room temperature. The Gaussian fits yields $\bar{\Phi}_b = 0.75$ and $\sigma = 0.04$ for the barrier heights.

4. Conclusions

In this study, we were attempted to study the electrical properties of the Co/*n*-Si Schottky diodes (10 dots) formed by electrodeposited method under experimentally identical conditions. The laterally homogeneous BH value of approximately 0.81 eV for the electrodeposited Co/n-Si Schottky structures was obtained from the linear relationship between experimental effective BHs and ideality factors that can be explained by lateral inhomogeneities. The statistical analysis yields the mean effective SBH = 0.67 ± 0.02 eV and the mean ideality factor = 1.23 ± 0.03 for these devices from the *I–V* characteristics. In addition, the statistical analysis yields the mean effective SBH = 0.75 ± 0.04 eV for these devices from the *C–V* characteristics.

References

[1] S.M. Sze, Physics of Semiconductor Devices, third ed., John Wiley & Sons, New York, 2007.
[2] E.H. Rhoderick, R.H. Williams, Metal–semiconductor structures, Clarendon Press, Oxford, 1988.
[3] R.T. Tung, Mater. Sci. Eng. R 35 (2001) 138.
[4] J.H. Werner, H.H. Guttler, J. Appl. Phys. 69 (1991) 1522.
[5] A.R. Saha, S. Chattopadhyay, R. Das, C. Bose, C.K. Maiti, Solid State Electron. 50 (2006) 1269.
[6] Ş. Karataş, Ş. Altindal, Mater. Sci. Eng. B 122 (2005) 133.
[7] H. Çetin, B. Şahin, E. Ayyildiz, A. Türüt, Physica B 364 (2005) 133.
[8] S. Chand, J. Kumar, Semicond. Sci. Technol. 11 (1996) 1203.
[9] Ş. Karataş, Solid State Commun. 135 (2005) 500.
[10] N.L. Dimitruk, O.Yu. Borkovskaya, I.N. Dimitruk, S.V. Mamykin, Zs.J. Horvath, I.B. Mamontova, Appl. Surf. Sci. 190 (2002) 455.
[11] E. Hökelek, G.Y. Robinson, Solid State Electron. 99 (1981) 24.
[12] G.A. Barti, M. Schlilter, Phys. Rev. B 33 (1986) 7346.
[13] R. van de Walle, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, J. Appl. Phys. 74 (1993) 1885.
[14] M.K. Hudait, S.B. Kruppanidhi, Solid State Electron. 44 (2000) 1089.
[15] A. Singh, K.C. Reinhardt, W.A. Anderson, J. Appl. Phys. 68 (1990) 3475.
[16] P. Chattopadhyay, A.N. Daw, Solid State Electron. 29 (1986) 555.
[17] H.C. Card, E.H. Rhoderick, J. Phys. D 4 (1971) 1589.
[18] K. Hatori, Y. Torii, Solid State Electron. 34 (1991) 531.
[19] Ş. Karataş, Ş. Altındal, A. Türüt, A. Özmen, Appl. Surf. Sci. 217 (2003) 250.
[20] B. Akkal, Z. Benamara, L. Bideux, B. Gruzza, Microelectron. J. 30 (1999) 673.
[21] V.W.L. Chin, M.A. Green, J.W.V. Storey, Solid State Electron. 33 (1990) 299.
[22] S. Forment, R.L. Van Meirhaeghe, A. De Vrieze, K. Strubbe, W.P. Gomes, Semicond. Sci. Technol. 16 (2001) 975.
[23] Z.L. Bao, K.L. Kavanagha, J. Vac. Sci. Technol. B 24 (2006) 2138.
[24] A. Eftekhari, Microelectron. Eng. 69 (2003) 17.

[25] V. Saxena, R. Prakash, Polym. Bull. 45 (2000) 267.
[26] Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, Solid State Electron. 29 (1986) 633.
[27] R.T. Tung, Phys. Rev. B 45 (1992) 13509.
[28] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. 70 (1991) 7403.
[29] W. Mönch, J. Vac. Sci. Technol. B 17 (1999) 1867.
[30] J. Ohdomari, K.N. Tu, J. Appl. Phys. 51 (1980) 3735.
[31] H.J. Im, Y. Ding, J.P. Pelz, W.J. Choyke, Phys. Rev. B 64 (2001) 075310.
[32] T.U. Kampen, W. Mönch, Surf. Sci. 331–333 (1995) 490.
[33] K. Akkilic, T. Kilicoglu, A. Turut, Physica B 337 (2003) 388.
[34] H. Çetin, B. Şahin, E. Ayyildiz, A. Türüt, Semicond. Sci. Technol. 19 (2004) 1113.
[35] W.P. Leroy, K. Opsomer, S. Forment, R.L. Van Meirhaeghe, Solid State. Electron. 49 (2005) 878.
[36] G. Güler, Ö. Güllü, Ö.F. Bakkaloglu, A. Türüt, Physica B 403 (2008) 221.
[37] M. Sağlam, F.E. Cimili, A. Türüt, Physica B 348 (2004) 397.
[38] H. Doğan, H. Korkut, N. Yıldırım, A. Türüt, Appl. Surf. Sci. 253 (2007) 7467.