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Direct detection of carrier traps in Si solar cells after light-induced degradation

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In solar cells fabricated from boron-doped Cz-Si wafers minority and majority carrier traps were detected by deep level transient spectroscopy (DLTS) after so-called "light-induced degradation" (LID). The DLTS signals were detected from mesa-diodes with the full structure of the solar cells preserved. Preliminary results indicate metastable traps with energy levels positioned at $E_V + 0.37$ eV and $E_C - 0.41$ eV and apparent carrier capture cross-sections in the 10^{-17}–10^{-18} cm^2 range. The concentration of the traps was in the range of 10^{12}–10^{13} cm^{-3}. The traps were eliminated by annealing of the mesa-diodes at 200 °C. No traps were detected in Ga-doped solar cells after the LID procedure or below the light protected bus bar locations in B-doped cells.

1 Introduction The "light-induced degradation" (LID) of Si solar cells is known for more than 40 years (see [1–8] and references therein). The degradation is leading up to $\Delta\eta/\eta_0 = 10\%$ gradual relative loss in the efficiency value of Si solar cells under working conditions. The effect of LID was clearly observed by carrier lifetime spectroscopy [2–7] and was interpreted in most cases as being due to the Shockley–Read–Hall (SRH) recombination at a centre containing boron and oxygen atoms. The analysis [2, 3] suggested that traps with energy level at $E_C - 0.41$ eV are responsible for the LID. Despite numerous attempts no LID-related traps have been observed until now by deep level transient spectroscopy (DLTS) or related techniques (see [8] and references therein).

An annealing step at 200 °C for several minutes cures the LID effect. However, subsequent illumination initiates LID again. Permanent passivation of the LID defects, so-called regeneration, occurs if annealing is accompanied by carrier injection. Recent investigations strongly suggest a crucial role of hydrogen in the regeneration (see [9, 10] and references therein). The role of hydrogen in the annealing process of LID defects has still to be clarified.

The aim of the present work was a direct detection of the LID defect by DLTS on mesa-diodes fabricated from high-quality Cz-Si solar cells.

2 Samples and experimental Two Cz-Si solar cells with passivated emitter rear contact (PERC), one doped with boron with resistivity 2 Ω cm and another one doped with Ga (1 Ω cm) were used in our investigations [11]. Several pieces, ~2 × 2 cm^2 in size, were cut out of the cells and subjected to illumination under AM1.5 conditions. The LID process was monitored by in-situ measurements of open-circuit voltage (V_{OC}) from the pieces. After saturation of the second drop of the V_{OC} value (>24 h, see Fig. 1), the pieces were cleaved to samples with sizes ~5 × 10 mm^2 and mesa-diodes with area ~1 mm^2 were fabricated on top of the samples (see insert in Fig. 1). Details of the mesa-diode fabrication procedure were presented earlier [12].

Some of the illuminated samples were annealed at 200 °C for 20 minutes in a light-tight furnace to check the annealing of LID defects. For some of the samples the back-side structure of the cells was removed by dry polishing or by etching in HF : H_2O and HF : HNO_3 : H_2O solutions for 35 min. The front side of the cells was protected by resist during the etching. The extended etching duration was

related to the complicated structure of the back-side contact in the PERC cells, with several layers to be removed. For samples with removed back-side structure ohmic contacts were formed by rubbing-in InGa eutectic solution.

In what follows, the labels of the investigated mesa-diodes (see example presented in the inset of Fig. 1) will start with the dopant symbol ("B" or "Ga"). The mesa-diodes completely protected from the illumination by bus bar lines (see image in Fig. 1) have "B" as subsequent letter in the label, while those with only thin contact finger on the top have letter "C" instead. The processing state of the material is reflected by: "(0)" the initial state, "(I)" – illuminated and "(A)" – annealed. In the case of back-contact removal the additional symbol "E" means etching and "P" – dry polishing. The symbol "#" is used as a wild-card.

DLTS measurements were performed by means of a standard lock-in system working at the capacitance testing frequency of 1 MHz. Principles of the method and the system were previously described [13]. Cooling of a sample was done by immersion in a dewar with liquid He and a temperature controller maintaining the necessary temperature in the range of 35–300 K.

3 Results and discussion Relative changes of V_{OC} with time during the LID for the B-doped cell and the reference curve for the Ga-doped cell are presented in Fig. 1. The difference in formation of LID-related defects in B- or Ga-doped cells is clearly visible in Fig. 1: no changes for V_{OC} were detected for the Ga-doped samples with illumination time. Relative loss in the B-doped cell efficiency value after LID procedure was $\Delta\eta/\eta_0 = 2.3\% \pm 0.3$, while in the limits of the error the efficiency remained the same for the Ga-doped cells.

Prominent DLTS peaks from majority and minority carrier traps were detected from the all BC(I) mesa-diodes subjected to the LID procedure in B-doped cells. An example of DLTS signals from such mesa-diodes is presented in Fig. 2.

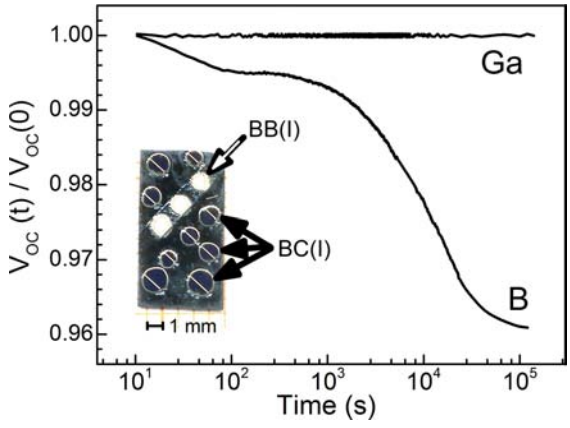

Figure 1 Relative changes of V_{OC} with time during the LID for the B-doped cell and the reference curve for the Ga-doped cell. Insert presents example image of B-doped sample with mesa-diodes.

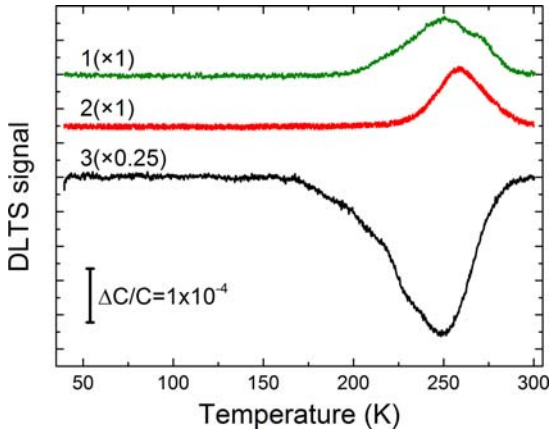

Figure 2 DLTS spectra detected from B-doped cells subjected to the LID procedure. The spectra are shifted vertically for ease of viewing. The intensity of spectrum 3 was divided by 4. Experimental conditions: sampling period 48 ms, pulse duration 250 µs, reverse bias 5 V, pulse voltage 1 V (curves 1, 2) and –1 V (curve 3). For an estimate of the signal amplitude the $\Delta C/C$ scale (see text) is presented in the lower left part of the figure.

For detection of majority carrier traps (Fig. 2, curve 1) diodes were cooled to low temperatures (<100 K) with shortened contacts and DLTS measurements were performed with $dT/dt > 0$. Measurement of the same diodes starting from 300 K (with $dT/dt < 0$) generated majority carrier DLTS signals similar to curve 2. The shape of the signals from the minority carrier traps was similar independent on the cooling conditions (curve 3 in Fig. 2).

Apparently the defects showed metastability: the shape and intensity of the majority peak depended on the sample cooling conditions. Therefore, the parameters of the traps will require further detailed investigations. Our preliminary measurements suggest an energy level position for the majority carrier trap at $E_t = E_V + (0.37 \pm 0.01)$ eV, with apparent carrier capture cross-section extrapolated from the Arrhenius plot (CCS) close to 10^{-18} cm^2. For the minority trap, $E_t = E_C - (0.41 \pm 0.01)$ eV and CCS ~ 10^{-17} cm^2. The majority trap concentration was ~2×10^{12} cm^{-3}. The estimated lower limit for the concentration of the minority traps was ~2.5×10^{13} cm^{-3}.

The intensities of the detected signals for various types of mesa-diodes in $\Delta C/C$ units, where ΔC is a capacitance change at the maximum of DLTS signal and C is the value of the capacitance at the reverse bias, are presented in Fig. 3. The signals were below the detection level (D.L.) for the B # (0) diodes prepared from the non-illuminated cell, from illuminated mesa-diodes located below the bus bars, BB(I), and for all mesa-diodes after the annealing B # (A). No signals were detected from Ga-doped diodes, Ga # (#), in whichever state.

The formation and annealing of the DLTS traps are in agreement with those of the LID defects [2–8]. The preliminary parameters of the traps well agree with those suggested by the reported carrier lifetime measurements [3–6]. The metastability of the defects and the overlay of the ma-

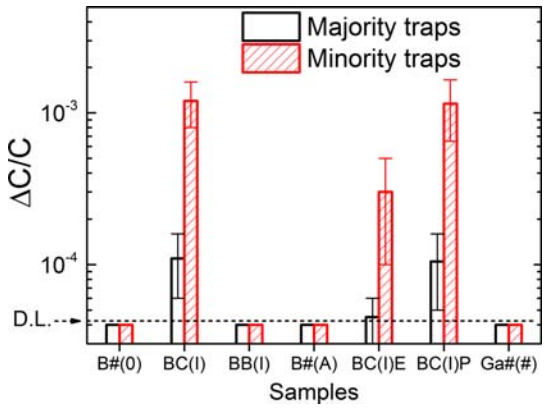

Figure 3 DLTS signal intensities for majority and minority traps in various mesa-diodes (see text) in $\Delta C/C$ units.

jority and minority DLTS peak positions require future minority carrier transient spectroscopy (MCTS) measurements for the precise determination of the trap parameters.

After the prolonged etching-off of the backside contacts of the cells, diodes BC(I)E in Fig. 3, the DLTS signal intensities dropped by a factor of 4. Removal of the backside contact by polishing, diodes BC(I)P, did not cause noticeable changes in the signals. Strong changes in the amplitude of the signals for the samples subjected to backside etching may suggest a strong influence of hydrogen on the traps. Strong influence of hydrogen on permanent suppression of LID defects was also observed previously [9, 10]. In our case, hydrogen was introduced to the bulk of the samples during the prolonged etching procedure. If the observed effect is indeed related to hydrogen introduced to the sample bulk during the etching, the previously reported problems with the DLTS detection of the traps [8] could be easily explained. All previous DLTS detection attempts were performed on the LID subjected bulk material. In these cases the preparation of Schottky diodes for DLTS measurements required wet chemical treatment of the samples which naturally introduce hydrogen in the near-to the surface volume. Therefore, all LID-related traps will be already passivated during the sample preparation procedures. In our case the investigated volume of the mesa-diode was safely protected by resist and therefore the LID-related defects could survive the sample preparation procedures.

At the present stage it is too early to discuss in-depth the possible structure of the traps. However, based on the present knowledge [2–10] and taking into account the possible strong influence of hydrogen (see [10] and our results) we would suggest a slightly different mechanism of LID. The previous models assumed that LID resulted from formation or activation of boron and oxygen containing complexes during carrier injection at $T < 100$ °C. Following [14], we would suggest that the complexes responsible for LID are formed during crystal growth and/or cooling but are initially passivated by hydrogen existing in the crystal. Carrier injection leads to the escape of hydrogen from the complexes and the residual part becomes electrically active leading to LID. Further, any treatment introducing hydrogen leads to re-passivation of the complexes and suppression of their electrical activity. The heat treatment also initiates redistribution of hydrogen atoms toward the complexes and their passivation. Such a mechanism could explain the sensitivity of the traps to the hydrogen content in the material and the ease of their activation at low temperatures.

In summary, we have directly detected the defect levels introduced during LID in B-doped Si by DLTS on mesa-diodes prepared from PERC solar cells. The majority as well as the minority carrier traps, formed during LID, were suppressed by annealing at 200 °C. Further measurements will help to unravel the nature of this defect.

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