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On Interface and Oxide Degradation in VLSI MOSFETs—Part I: Deuterium Effect in CHE Stress Regime

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***Abstract*—This paper analyzes in detail the generation of interface states (N_{it}) and stress-induced leakage current (SILC) during channel hot electron (CHE) stress experiments in the context of a possible hydrogen/deuterium (H/D) isotope effect.**

Our results show that N_{it} generation is related to the hydrogen release (HR) at the Si-SiO_2 interface at relatively high V_G where a large isotope effect is found. Instead, for gate voltages (V_G) favorable for hot hole injection (HHI) the N_{it} creation becomes a unique function of hole fluence and the isotope effect disappears.

In the studied stress conditions, we found no experimental evidence supporting a causal relation between SILC generation and HR because no isotope effect is observed even when the corresponding N_{it} measurements reveal a very different D/H release rate. Similar to N_{it} generation, we found that SILC becomes a unique function of hole fluence at low stress V_G.

Relevant implications and extensions of these results to the Fowler-Nordheim (FN) tunneling stress conditions are discussed in the companion paper [47].

***Index Terms*—Channel hot electron (CHE) degradation, hydrogen/deuterium (H/D) isotope effect, interface states, MOSFETs relibility, stress-induced leakage current (SILC).**

I. Introduction

THE reduction of the gate oxide thickness has been systematically used as an essential ingredient for device downscaling in the evolution of MOS technologies [1]–[3], and the amount of work directed to thin oxide reliability in recent years is very remarkable. When stressed at high electric fields, thin oxides develop a progressive low voltage stress-induced leakage current (SILC) [4], [5] which is a serious concern for data retention of nonvolatile memories and represents the main obstacle for oxide scaling in these devices [6]–[10]. At larger charge fluences, oxides eventually experience a breakdown and their insulating properties are suddenly compromised. It has been recently pointed out that oxide breakdown may impose a limit to its scaling and this fact might in turn prevent silicon technology from attaining the SIA roadmap [11].

The significant research effort has lead to a consensus on some important points concerning thin oxide reliability. It is quite generally accepted that the generation of the damage is correlated to electron energy at the anode [12]–[14] and it is thus governed by the gate voltage (V_G) rather than by the oxide field [15]–[18]. The conduction mechanism responsible for SILC is generally assumed to be a trap-assisted tunneling [19]–[21], [8], [22] that is most probably inelastic [23]–[27]; however, it is not completely clear yet whether oxide sites are mainly neutral or positively charged traps [28]. Furthermore, according to the percolation theory, breakdown occurs when oxide traps reach a critical density [29], [11], [30], [31] and SILC can thus be effectively used as a sensitive monitor of oxide degradation [8], [21].

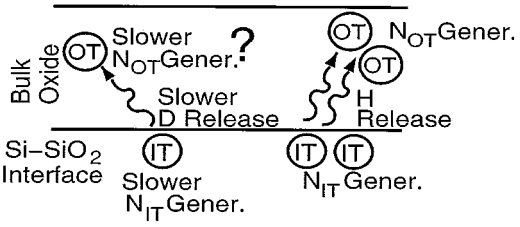

Fig. 1. Schematic representation of the process of interface states N_{it} generation related to the release of a H atom (right) from the Si-SiO_2 interface. In the HR model, the released H is involved in the subsequent generation of a bulk oxide trap N_{ot}. If the rate of release for deuterium (left) is slower than for hydrogen, then a slower creation of N_{ot} is expected in the HR model picture.

Although it is generally accepted that the damage generation is governed by the electron energy at the anode, as mentioned above, two different models have been proposed for the mechanism that links electron energy to degradation. According to the hydrogen release (HR) model [21], [32] hot electrons at the anode cause the release of hydrogen (H) atoms from Si-SiO_2 interface and the migration of H species within the oxide results in the creation of the bulk-oxide traps (N_{OT}) (see Fig. 1). The anode hole injection (AHI) model, instead, identifies the culprit in the injection of hot holes generated at the anode by energetic electrons [33], [14].

A tempting means to test the HR model is provided by recent experiments showing that using deuterium (D) instead of H for device passivation suppresses interface state (N_{it}) generation in channel hot electron (CHE) stress conditions because D exhibits a much slower desorption yield than H in the electronic excitation regime [34], [35]. According to the HR model the desorption of hydrogen is also responsible for N_{OT} generation so that a D/H isotope effect on SILC is expected (see Fig. 1). Consequently, whether or not D annealing is also effective to reduce SILC [36]–[38], besides the clear applicative interest, can remarkably help enlighten the dominant cause of SILC generation.

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Recent experiments [36] have reported that samples exhibiting a clear D/H isotope effect for $N_{\rm it}$ generation during CHE stress experiments show essentially no isotope effect for SILC produced by a Fowler-Nordheim (FN) stress. However, FN and CHE stress may not probe the same D concentration if the diffusion length of D from the spacers is small [34], [39], [36] because FN stress is spacially uniform along the channel whereas CHE damage is localized at the drain-end of the channel where the D concentration might be larger then elsewhere. Furthermore, since the isotope effect on $N_{\rm it}$ generation in FN stress conditions is much smaller than during CHE stress [40], [38], it is only using this latter stress regime that SILC generation can be studied in the context of a clearly different rate of D/H release at Si-SiO_2 interface.

In this paper, we systematically study the generation of $N_{\rm it}$ and SILC in CHE stress experiments in the context of a possible D/H isotope effect. Our results show that no isotope effect is observed on SILC even when a large effect is simultaneously observed on $N_{\rm it}$. By exploring a variety of electron and hole injection conditions, we discuss the possible correlation of $N_{\rm it}$ and SILC generation to the D/H release at the interface and to hot hole injection (HHI).

In the companion paper [47], we will first use these results to compare the efficiency of a HR mechanism with experimental data of SILC produced by conventional high field stress conditions and then investigate in depth a possible AHI mechanism at low stress gate voltages.

II. Device Technology and Experimental Techniques

The devices used in this work are n-MOS transistors fabricated with a 0.25-μm technology. The oxide thickness is $T_{\rm ox} = 5$ nm, the device width and length are $W = 39$ and $L = 0.32$ μm, respectively, and the threshold voltage is $V_T \approx 600$ mV. The use of transistors is obviously necessary for CHE stress experiments, however also in the companion paper [47] (dealing with the FN stress regime) we will make use of n- and p-MOS transistors instead of capacitors because they provide more experimental knobs and degradation monitors that prove useful for our analysis.

Two otherwise identical wafers were annealed either in a 10% H_2 ambient at 425 °C for 2 h (H_2 devices) or in a 10% D_2 ambient at 450 °C for 5 h (D_2 devices). The drain current and transconductance characteristics of the *virgin*, as fabricated devices were virtually indistinguishable despite the different temperature and duration of the anneal, thus indicating that the only relevant difference between H_2 and D_2 samples is the substitution of deuterium to hydrogen in the passivation of the Si-SiO_2 interface.

CHE stress experiments were performed in a variety of drain voltage (V_D) and V_G conditions and $N_{\rm it}$ generation was monitored using both linear drain current (I_D) versus V_G characteristics and charge pumping (CP) measurements [41] performed at a frequency of 160 kHz. The main experimental hurdle related to SILC measurements in CHE conditions is the detection of extremely small values of gate current (I_G). In fact, the extension of the damaged area during CHE conditions is confined to a small length close to the drain end of the channel which makes

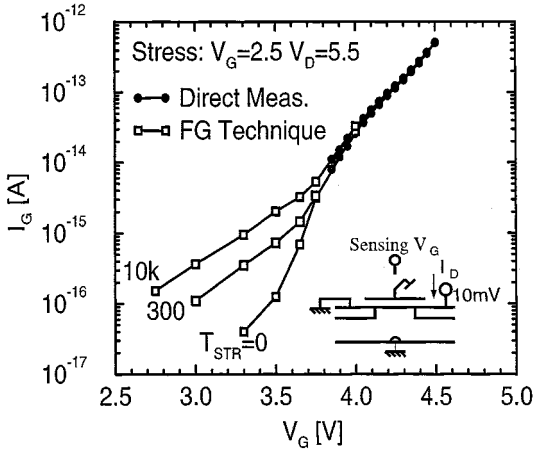

Fig. 2. Typical I_G measurements obtained with the FG technique and comparison with direct measurements. The working principle of the technique is sketched: I_G was calculated from I_D drop as $I_G \simeq [\Delta I_D/(G_m \cdot \Delta t)] \cdot C_G$. Very good agreement between FG (open symbols) and direct measurements (filled symbols) is obtained in the V_G range where both are possible.

SILC proportional to device width rather than to device area. It is also worth noting that, for the relatively short devices necessary for CHE stress experiments, the width cannot be arbitrarily increased because the very large drain currents drawn during the stress make it difficult to accurately control the *intrinsic V_D applied to the device* due to possible voltage drops on *nonscaling* parasitic resistances such as the contact resistance between the tips and the pads.

In order to greatly improve I_G sensitivity over conventional direct measurements, we made use of the floating-gate (FG) technique. This characterization procedure was initially conceived for small I_G measurements during CHE stress experiments [42], [43] and it has been more recently used for the measurement of low tunneling currents [44], [45]. The basic idea of this technique is to use the MOS device as a very sensitive electrometer to convert small gate currents in V_G variations that can be in turn detected as I_D change (see the the schematic description in the inset of Fig. 2).

In practice, after every stress step the I_D versus gate V_G characteristic was measured for a very small $V_D = 10$ mV and the transconductance G_m was determined in the V_G range of interest. Then the gate electrode was charged to a suitable V_G value (slightly above the sensing V_G value which is to be probed), and subsequently floated by lifting up the gate probe. The average I_G value is proportional to the variation of V_G and can be readily calculated from the I_D drop as

$$I_G \simeq C_G \times \left[\frac{\Delta I_D}{G_m \cdot W \Delta t}\right] \tag{1}$$

where C_G is the total gate capacitance. The capacitance C_G was measured to be approximately 0.5 pF (essentially the capacitance of the pad) and this value led to a very good agreement between FG and direct measurements when both were possible (see Fig. 2).

During all experiments a flux of dry nitrogen was present in the micro-chamber of the probe station [43] that suppressed any leakage current component at the surface of the wafer well below the minimum I_G that will be reported as a measurement

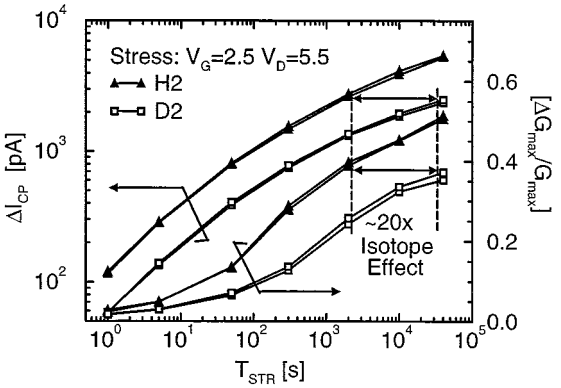

Fig. 3. $I_{\rm CP}$ and G_m variations versus $T_{\rm STR}$ for a stress $V_D = 5.5$ and $V_G = 2.5$ V corresponding to maximum substrate current. The results for two pairs of H_2 and D_2 devices are shown. Approximately the same 20 times isotope effect is observed for both monitors.

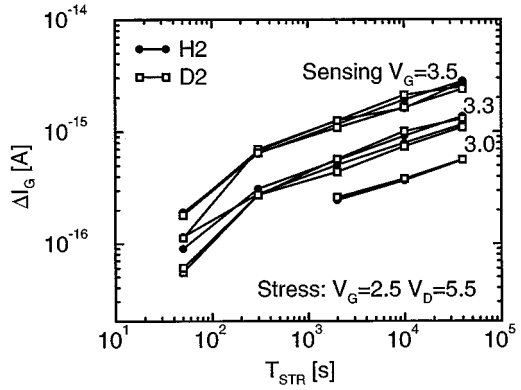

Fig. 4. SILC evolution corresponding to the same experiment of Fig. 3 and for three different sensing V_G values. The results for two pairs of H_2 and D_2 devices are shown. Essentially no isotope effect is observed.

result. To be conservative we can say that all data for I_G values above 10^{-16} A were stable and reliable.

Since SILC is known to have a transient component [46], [28], in all measurements we carefully isolated the steady state SILC by performing preliminary I_G versus V_G characteristics with a very slow sweep rate also when SILC was to be measured with the FG technique.

III. Measurement Results

Fig. 3 shows CP current $(I_{\rm CP})$ and G_m variations for stress $V_D = 5.5$ and $V_G = 2.5$ corresponding to maximum substrate current. Consistently with previous studies [34], [35], a large isotope effect on both $I_{\rm CP}$ and G_m is observed showing approximately a 20 times slower rate of $N_{\rm it}$ generation in D_2 devices. The corresponding SILC measurements are shown in Fig. 4 for three different sensing V_G and it is apparent that, in spite of the much slower rate of D desorption at the interface proved by $N_{\rm it}$ generation in Fig. 3, SILC measurements exhibit essentially no isotope effect. This comparison clearly points out that the generation of SILC cannot be causally related to H or D release in these stress conditions.

Fig. 5 shows I_G versus V_G characteristics of the devices used for our experiments: at large V_G a positive gate current due to hot electron injection is observed whereas for lower V_G values

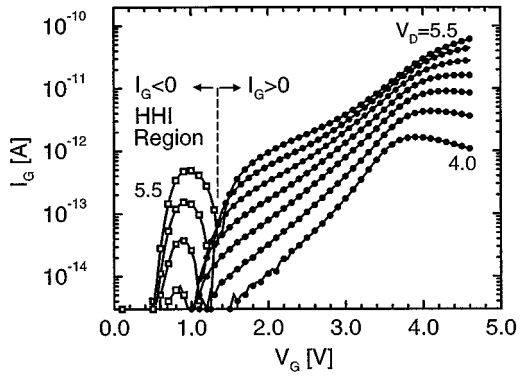

Fig. 5. Measured I_G characteristics as a function of V_G and for V_D from 4.0 to 5.5 V in step of 0.25 V. At low V_G a negative I_G (open symbols) corresponding to HHI is clearly observed.

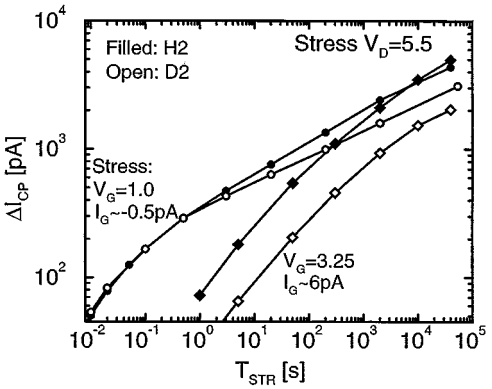

Fig. 6. $I_{\rm CP}$ variations for a stress $V_D = 5.5$ V and $V_G = 1$ V corresponding to the maximum HHI $(I_G < 0)$ or $V_G = 3.25$ corresponding to hot-electron injection $(I_G > 0)$ (see Fig. 5). No isotope effect is observed in the early stage of the stress in the HHI stress condition.

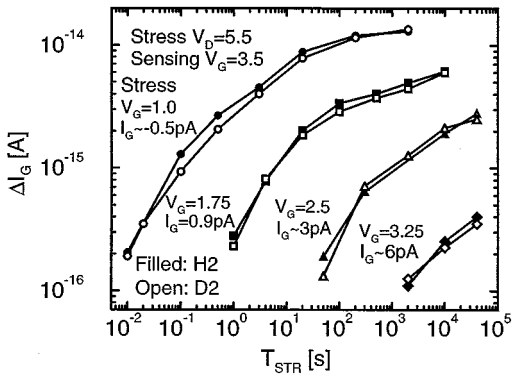

Fig. 7. SILC evolution for a stress $V_D = 5.5$ V and different V_G voltages corresponding to different I_G values (Fig. 5). SILC is dramatically increased when V_G is reduced and becomes progressively more favorable for HHI. No isotope effect is observed for any stress condition.

a negative I_G produced by HHI is found, consequently, the ratio between electron and hole injection during the stress can be changed by orders of magnitude adjusting the values of V_D and V_G.

The effect of the stress V_G is illustrated in Figs. 6 and 7 for $I_{\rm CP}$ and SILC, respectively. When V_G is reduced and becomes progressively more favorable for HHI, a very fast $N_{\rm it}$ creation is observed in Fig. 6, where the release of hydrogen from the

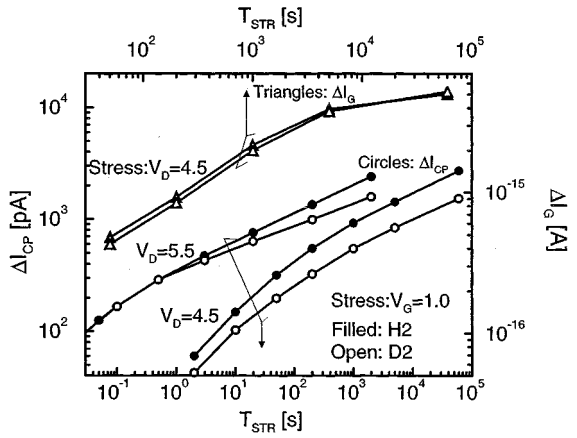

Fig. 8. $I_{\rm CP}$ evolution (circle, bottom and left axes) for a stress $V_G = 1$ V and $V_D = 5.5$ or 4.5 V. When V_D is reduced a clear isotope effect on $I_{\rm CP}$ emerges. SILC evolution (i.e., ΔI_G at a sensing $V_G = 3.5$ V) for stress $V_G = 1$ V and $V_D = 4.5$ V is also reported (triangles, top and right axes) where no isotope effect is found.

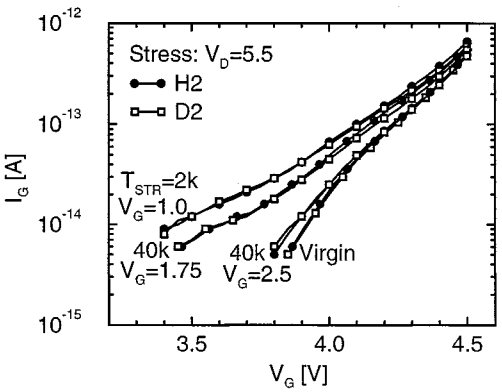

Fig. 9. Direct measurements (non-FG) of I_G versus V_G characteristics for virgin and stressed devices. Stress $V_D = 5.5$ while V_G is 1.0 (with a $T_{\rm STR} = 2000$), 1.75 and 2.5 (with $T_{\rm STR} = 40000$). No isotope effect on SILC is observed.

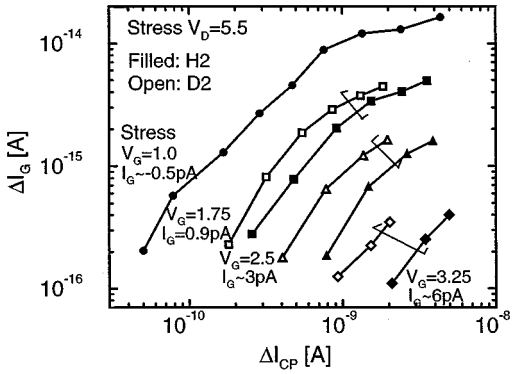

Fig. 10. Stress-induced I_G variations (sensing $V_G = 3.5$ V) plotted as a function of corresponding $I_{\rm CP}$ variations for stress $V_D = 5.5$ and different stress V_G values. For a given amount of $\Delta I_{\rm CP}$ SILC is greatly increased for decreasing V_G. For a given stress condition D_2 devices exhibit essentially the same ΔI_G for lower $\Delta I_{\rm CP}$.

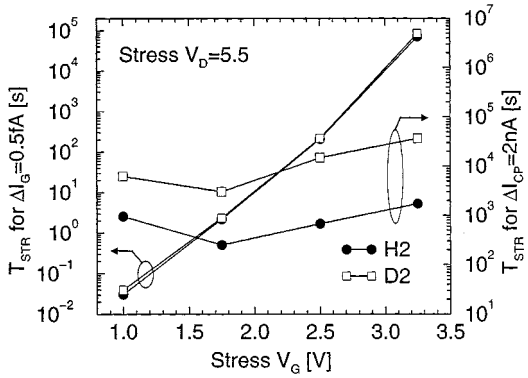

Fig. 11. Stress time to reach either an I_G increase of 0.5 fA (for a sensing $V_G = 3.5$ V) or an $I_{\rm CP}$ increase of 2 nA as a function of the stress V_G and for stress $V_D = 5.5$. A very different V_G dependence of SILC and $N_{\rm it}$ generation is found and, furthermore, in the case of $N_{\rm it}$ a 20 times isotope effect is observed whereas in the case of SILC it is not. We verified that the qualitative behavior of $T_{\rm STR}$ versus stress V_G does not significantly depend on the target values used for $\Delta I_{\rm CP}$ and ΔI_G.

interface is not presumably involved because no isotope effect is observed (at least in the early stage of the stress). The effect of stress V_G on SILC is much stronger than on interface states and Fig. 7 shows that oxide degradation is dramatically increased with decreasing V_G: the stress time $(T_{\rm STR})$ to reach a given ΔI_G varies by more than six orders of magnitude when V_G changes between 1.0 and 3.25 V and, furthermore, no isotope effect on SILC is observed in any stress condition. The data of Fig. 7 strongly suggest that HHI plays an important role in the degradation of the oxide.

As for the correlation between HHI and the isotope effect on $N_{\rm it}$, similar results as in Fig. 6 are obtained by varying V_D instead of V_G. In fact, Fig. 8 shows that if V_D is reduced from 5.5 to 4.5 V for $V_G = 1.0$ V (thus drastically suppressing HHI—Fig. 5), then $N_{\rm it}$ creation is slowed and an isotope effect appears. On the contrary SILC still exhibits no correlation to the different rate of D and H release from the interface.

Since most SILC measurements have been obtained with the indirect FG technique, we have double-checked the results using conventional direct measurements. In fact, depending on the stress conditions, a direct measurement of SILC (i.e., not obtained with the FG technique) was also possible at large stress times. The insensitivity of SILC to D annealing could thus be also confirmed by direct measurements of post-stress I_G characteristics, as shown in Fig. 9.

IV. Discussion

A. Possible Correlation Between $N_{\rm it}$ and SILC Generation

The results reported so far demonstrate that in the CHE stress conditions there is no correlation between $N_{\rm it}$ and SILC generation and this is best illustrated by Fig. 10 where ΔI_G is plotted as a function of the corresponding $\Delta I_{\rm CP}$ for different V_G and for both H_2 and D_2 devices. In fact, for a given amount of $\Delta I_{\rm CP}$ very different ΔI_G are observed and, furthermore, when the isotope effect reduces $N_{\rm it}$ generation in D_2 devices, yet essentially the same I_G variations are found.

Fig. 11 illustrates the stress time $T_{\rm STR}$ necessary to reach a given $I_{\rm CP}$ or I_G increase and indicates a very different dependence of the two degradation monitors on the stress V_G. In the case of SILC, $T_{\rm STR}$ decreases by orders of magnitudes when V_G is reduced and HHI is favored and, furthermore, no clear improvement is observed in D_2 with respect to H_2 devices. As for $\Delta I_{\rm CP}$, the V_G dependence of $T_{\rm STR}$ is much weaker and up to a 20 times lifetime increase is observed in D_2 devices.

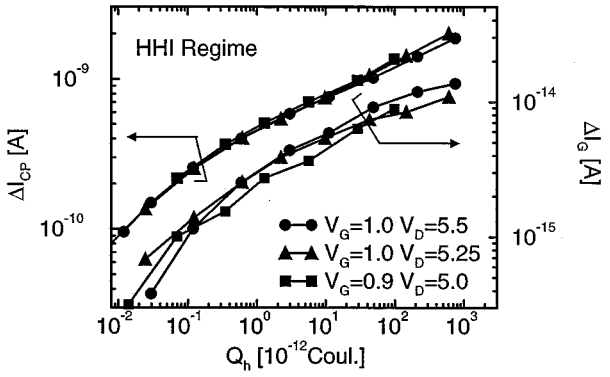

Fig. 12. Stress-induced $I_{\rm CP}$ and I_G variations (for a sensing $V_G = 3.5$ V) in the HHI regime versus hole fluence Q_h (i.e., the integral of I_G during the stress). Hot Hole gate current I_G is approximately 35, 115, and 550 fA for $V_D = 5.0, 5.25$. and 5.5 V, respectively (see Fig. 5).

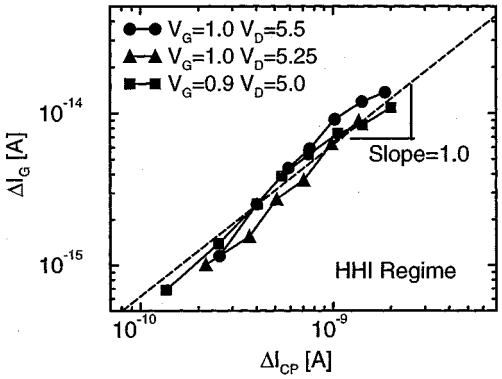

Fig. 13. Stress-induced I_G variations (for a sensing $V_G = 3.5$ V) versus $I_{\rm CP}$ variations in the HHI regime. Hot Hole gate current I_G is approximately 35, 115, and 550 fA for $V_D = 5.0, 5.25$, and 5.5 V, respectively (see Fig. 5).

The above results identify a clearly different behavior for SILC and $N_{\rm it}$ generation and, furthermore, two different mechanisms for $N_{\rm it}$ generation itself: at relatively large $V_G, N_{\rm it}$ is related to the HR caused by CHE and a clear isotope effect is observed, whereas for small V_G a different mechanism dominates which is largely insensitive to the different D or H desorption rates.

B. The Hot Hole Injection Regime

In order to investigate more quantitatively the possible role of HHI on $N_{\rm it}$ and SILC generation we performed experiments in the HHI stress regime varying the drain voltage and, consequently, the hot hole gate current. As can be seen in Fig. 5, I_G changes by more than one order of magnitude when V_D is varied between 5.0 and 5.5 V for a gate voltage of approximately 1.0 V. The corresponding stress experiments reveal that the generation of both $N_{\rm it}$ and SILC scale fairly well with the gate current so that, as shown in Fig. 12, both $\Delta I_{\rm CP}$ and ΔI_G are approximately unique functions of the hole fluence Q_h (i.e., the integral of I_G during the stress). The correlation between the damage generation and Q_h shown in Fig. 12 demonstrates that in this stress regime both interface and bulk oxide degradation are rate limited by HHI. The common origin of $\Delta I_{\rm CP}$ and ΔI_G is best illustrated by Fig. 13 showing a one to one proportionality between the two degradation monitors. This correlation between $N_{\rm it}$ and SILC generation is peculiar to the HHI stress regime and represents a clear difference with respect to CHE conditions as can be easily seen comparing Figs. 13 to 10.

As for the high V_G range, it is worth noting that when V_G increases (for a given V_D) hot electron injection increases by orders of magnitude as can be seen in Fig. 5. The dramatic reduction of SILC with increasing V_G (see Fig. 7) demonstrates that hot electrons cannot be the dominant cause of the oxide degradation. This latter fact is not completely surprising because in the CHE stress conditions the maximum of electron injection is most likely taking place in the region of the channel close to the inflection point of the oxide field $E_{\rm OX}$ (i.e., where $E_{\rm OX}$ changes its sign), so that electrons in the oxide typically experience a small field (with respect to values typical of the FN stress regime) and reach the poly electrode with only a small energy above SiO_2 conduction band minimum. Consequently, as long as the electron energy at the anode is the critical parameter for the oxide degradation, CHE injection is expected to induce a much smaller damage than FN tunneling for a given electron fluence.

As for holes, instead, for a given V_D, the injection into the oxide exponentially decreases with increasing V_G and the suppression of SILC with progressively larger V_G shown in Figs. 7 and 11 suggests that SILC generation might be rate limited by HHI also for relatively large V_G. This picture ascribing the generation of SILC to a mechanism which is not directly related to the HR could also explain why SILC never exhibits an isotope effect in the whole bias range explored in this work.

V. Conclusion

In the general framework of a possible assessment of the mechanisms responsible for thin oxide degradation, here quantified as SILC, in this paper we have exploited the recently pointed out D/H isotope effect [34], [35] to test the correlation between the desorption of hydrogen at Si-SiO_2 and the creation of $N_{\rm it}$ and SILC.

Our results show that $N_{\rm it}$ generation is evidently related to stress-induced leakage current (H/D) release at relatively large stress gate voltages where the well known isotope effect is unambiguously observed [34], [35], whereas at low stress V_G it is rate limited by HHI because $I_{\rm CP}$ variations become a unique function of hole fluence Q_h and, furthermore, the beneficial effect of D annealing almost disappears.

In the studied stress conditions, we found no experimental evidence supporting the causal relation between SILC generation and H release at the Si-SiO_2. Instead, at low V_G the generation of SILC seems to have the same origin as $N_{\rm it}$ and it is rate limited by hole injection. At relatively large V_G SILC is greatly suppressed but no isotope effect is observed even when the corresponding $N_{\rm it}$ generation measurements reveal a very different D/H desorption rate.

In the companion paper [47], we will show that using these results obtained for CHE conditions it is possible to establish a reasonable upper boundary for the efficiency of a possible HR mechanism for SILC generation in the conventional high oxide field stress configuration. The possible role of AHI in these FN stress conditions will be also investigated in details.

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