

Growth and Defects in Cast-Mono Silicon for Solar Cells: A Review

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Cast-mono silicon (CM-Si) is a promising substrate to fabricate cost-effective photovoltaic (PV) wafers used for solar cells with higher efficiency compared with conventional cast multicrystalline silicon (mc-Si) due to its high throughput and good ingot quality. However, the unavoidable appearance of defects like dislocation, subgrain boundaries, impurities, multicrystallization, and twins, seriously limits its mass-scale applications in the PV industry. In this review, the growth characteristics of the CM-Si method are introduced first. Then, the attention is focused on the defects in CM-Si. Other issues related to production costs that restrict the development of CM-Si are also addressed in detail, such as seed cost and recycled seeds, n-type CM-Si, and large-size CM-Si. Finally, a conclusion is made and the prospects are given about the CM-Si technique.

1. Introduction

With the increasingly severe environmental and energy issues, almost all of the countries around the world have begun to develop clean energy vigorously. Solar energy, being one of the most promising clean energy sources due to various advantages such as being resourceful, clean and safe, pollution free, and emission free, can be converted into electric energy directly by photovoltaic (PV) applications, that is, solar cells. Crystalline silicon remains the dominating substrate material used for solar cells in the PV industry, which accounts for more than 90% of the global PV market.^[1] Among them, single-crystalline silicon, grown by Czochralski (Cz) method, is mostly used for semiconductor industry and high-efficiency solar cells due to high purity and less crystal defects. However, the unavoidable high oxygen concentration in Cz-Si make the cells made of boron-doped Cz-Si wafers suffer serious light-induced degradation (LID) because of B–O complexes.^[2,3] In contrast, cast-mono silicon (CM-Si) has some advantages over Cz-Si such as low LID, cost-effectiveness, high throughput, and large scale, which has attracted much attention and made great progress over the decades. Nevertheless, CM-Si technique still faces several problems including dislocation generation, subgrain boundaries (sub-GBs),

multicrystalline grains, twins, and impurity contamination. These defects reduce the solar cell efficiency by 1–2% absolutely compared with Cz-Si cells, which hinders its mass-scale applications in PV industry. Therefore, it is very important to improve the cell performance by understanding its growth characteristic, the defects in physics, and finding the effective ways to suppress them.

In this review, we will first introduce the growth characteristic of CM-Si. Then, the attention is focused on the defects in CM-Si, and we will discuss various techniques to eliminate the defects. In addition, other issues related to production costs that restrict the development of CM-Si are also elaborated in detail, such as seed cost and recycled seeds, n-type growth, and large-size CM-Si. Finally, we will make a conclusion and give the prospects about CM-Si technique.

2. Growth of CM-Si

CM-Si, also called quasi-single-crystalline silicon, was first invented by BP Solar in 2006^[4] and then was developed by several PV companies and research institutes. It is well known that Cz-Si is grown by drawing and pulling seed crystals over the Si melt. Seeds are also used directly inside the crucible in the Bridgman method for getting high-performance multicrystalline silicon (mc-Si). Similarly, CM-Si method is basically the same as Bridgman method in terms of the following features: directional growth in a crucible from the bottom to the top and the use of single-crystalline seeds. These seeds prepared from Cz-Si ingots, usually <100> orientated when considering the actual solar cell applications, are used for CM-Si growth. The seed size is similar to that of cell wafers, that is, $\approx 15.6 \times 15.6 \times$ thickness cm³. During the practical casting process, all the feedstocks in the crucible are completely melted at a high temperature above the silicon melting point, except for the seeds that are partially melted. To keep the seeds preserved during the melting process, processing conditions and temperature profile require some modifications from those traditional furnaces used to fabricate mc-Si ingots. These modifications lead to a slight increase of the processing time, typically less than few hours. After that, the furnace is cooled down, and the molten silicon subsequently solidified directionally from the bottom to the top of the crucible and epitaxially inherits the initial grain structure. Finally, a CM-Si ingot is obtained. **Figure 1** shows the schematic illustration of one seed and the CM-Si growth.

Compared with the Cz method, CM-Si method could provide single-crystalline Si ingots with a high production throughput and low cost owing to the huge size of the ingots and the square

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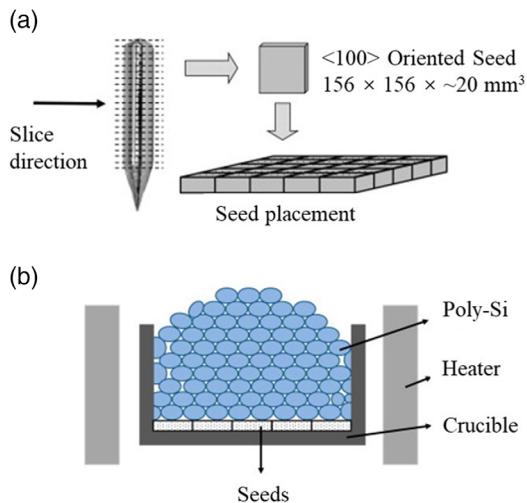


Figure 1. Schematic illustration of one seed and cast-mono silicon growth. Reproduced with permission.^[5] Copyright 2012, Elsevier.

shape of ingots, based on the same facilities as those used for growing mc-Si. As reported previously, the cost of CM-Si is currently 30–40% lower than that of Cz-Si,^[6] which is very important for the highly competitive PV industry. Furthermore, the similarity with the casting method also lowers the barrier to introducing this method on a practical manufacturing line. In addition, the crystal quality of CM-Si is usually high because of its single-crystalline feature. Single crystal means few GBs^[7–9] that could work as recombination sites for photogenerated carriers, especially when decorated with electrically active impurities. Another advantage of single crystals is the availability of alkaline texturing that can produce inverted pyramids due to the uniform {100} facet index of the wafer surface. Zhong et al.^[10] investigated the performance of solar cells made from CM-Si wafers with different area ratios of <100>-oriented single crystals in detail. They found that the main advantage of CM-Si solar cells lies in their low reflectance introduced by alkaline texturing. The difference in solar cell efficiency between alkaline and acidic texturing is up to an absolute value of about 1.05%. Moreover, this single-crystalline feature can be also adapted to cost-effective multiwire sawing by fixed diamond abrasive grains.

Casting methods have made great development and evolution in decades. As discussed earlier, CM-Si shares many of the advantages of Cz-Si and mc-Si; however, these advantages can become limitations in certain cases. CM-Si is slightly worse than Cz-Si in terms of crystal quality and has slightly higher cost than mc-Si. The crystal quality and cost issues are mainly related to several problems, that is, dislocation, sub-GBs, multicrystalline grains, twins, and impurities, etc. In the following sections, the defects in CM-Si will be discussed and advanced methods will be described to suppress them.

3. Defects in CM-Si and Methods to Suppress Them

3.1. Dislocation

Compared with Cz-Si, dislocations are easily introduced in CM-Si due to lacking of necking technique in directional

solidification. As one of the most detrimental defects in silicon, dislocation generally originates from thermal stress,^[11–16] mechanical damage stress,^[17–20] lattice mismatch around the seed junctions or metal precipitation,^[21] etc. Once formed, they tend to develop into extended defects as dislocation clusters by moving and propagating along with the preferred directions and exhibit cascade-like patterns in the minority carrier's lifetime maps.^[22,23] Dislocation clusters, especially when decorated with electrical active impurities, usually work as recombination sites for photogenerated carriers and shunts of p–n junctions in solar cells,^[24,25] which seriously lead to cell efficiency decrease and affect the development of CM-Si. Therefore, dislocation should be eliminated as much as possible.

Recently, various methods are reported to suppress dislocation generation, motion, and multiplication from seed junctions. Takahashi et al.^[26] proposed a new growth method named SMART for CM-Si, as illustrated in Figure 2. This method uses induced functional defects (i.e., GBs) located at ingot edges to achieve impurity gettering, dislocation-propagation limiting, and stress relaxing, which effectively hinder dislocation motion and propagation into the central area of the ingot. Similarly, Zhang et al.^[27] developed a novel <110>-oriented CM-Si by manipulating seeds pavement to control the dislocation glide and propagation, as shown in Figure 3a–c. As a result, cascade shape of the extended defects is absent, and dislocations only aggregate in the {100}/{100} boundary planes of <110>-oriented seeds (Figure 3f–g), because dislocations usually slip and propagate along the <110> directions in close-packed {111} planes (mentioned earlier), as shown in Figure 3d–e. In addition, they also designed functional Σ13 GBs at seed junctions for limiting dislocation clusters and sub-GBs and finally obtained high-quality CM-Si with low dislocation density.^[28]

Dislocations originating from seed junctions can be effectively controlled by defect engineering,^[21,27–33] while those caused by mechanical damage stress on seeds should be limited by other strategies. Huang et al.^[18] systematically studied the impacts of indentation morphology caused by feedstocks on seed surface on dislocation generation and mobilization. They applied buffer layers on Ga-doped seeds to release stress from feedstocks weight and thus to reduce dislocation density. Finally, they fabricated the CM-Si ingots with high quality. Several reports also focused on the dislocations induced by mechanic stress and carried out corresponding methods to control them.^[17–20] Another problem is the thermal stress that often occurs during growth or cooling. Jiptner et al.^[34] reported that dislocation density induced by thermal stress during cooling process is generally in the order of 10^3 cm^{-2} and that local dislocation density is as high as 10^4 cm^{-2} in the periphery of the ingot. To decrease the dislocation density, it is essential to reduce the amount of thermal stress. Li et al.^[35] studied the impact of thermal field on thermal stress and dislocation density distributions in the silicon ingot by transient global simulations. They found that melt flow structure and melt–crystal interface shape depend on thermal field simultaneously. During the cooling stage, proper decrease of temperature could reduce the thermal stress and dislocation density.

In summary, dislocation is the most common and detrimental defect in CM-Si. Its generation and motion are sensitive to stresses from mechanic damage, lattice mismatch, or thermal process. Many researches incorporated with functional defects

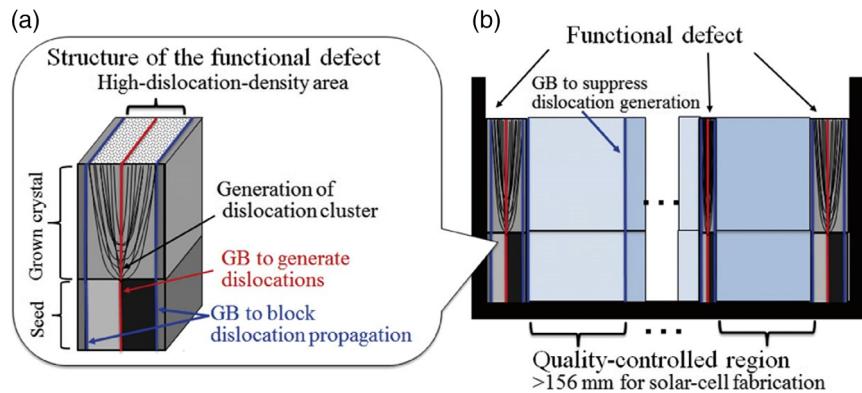


Figure 2. Concept of the SMART. a) Structure of the functional defects. b) Arrangement of seeds and grown crystals in a crucible. Reproduced with permission.^[26] Copyright 2015, The Japan Society of Applied Physics.

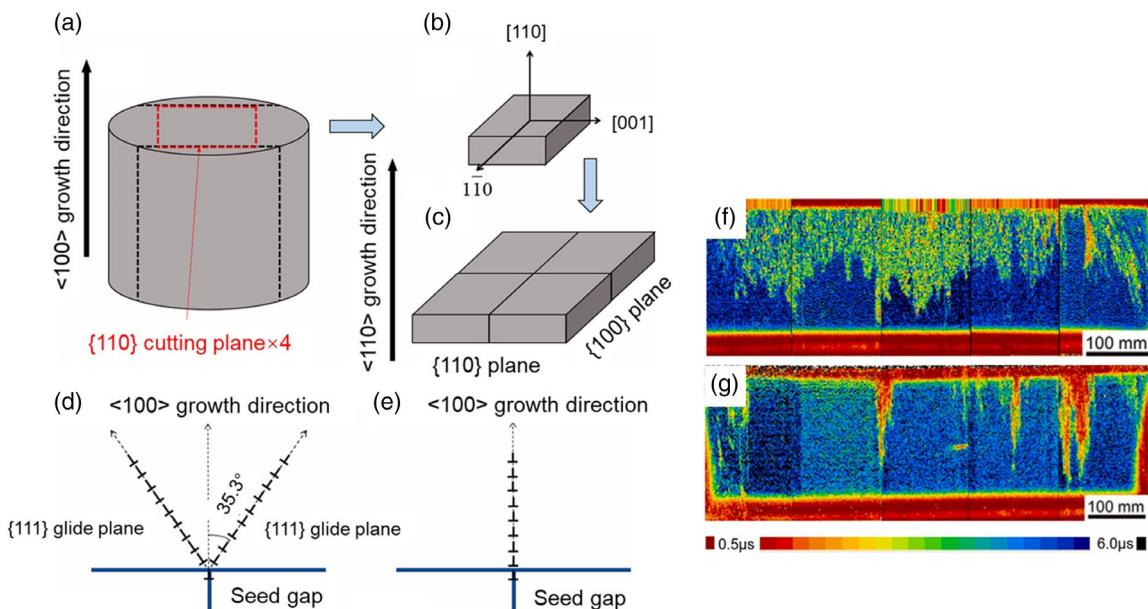


Figure 3. Schematic illustration of the $<110>$ -oriented seeds for growing CM-Si ingot: a) cutting method, b) the $<110>$ -oriented seed and its orientation index, and c) the way of the seed placement. Glide of dislocations in d) $<100>$ -oriented and e) $<110>$ -oriented CM-Si. Carrier lifetime mapping on the cross sections of CM-Si: f) $<100>$ -oriented and g) $<110>$ -oriented. Reproduced with permission.^[27] Copyright 2019, Elsevier.

like induced GBs or with designation of thermal field have been investigated and have succeeded in controlling dislocation and its extended defects.

3.2. Subgrain Boundaries

Sub-GB is another defect in CM-Si ingot, which is usually induced and generated by seed junctions or mechanic stress.^[36] Sub-GBs, though with a small deviation of crystalline lattice orientation, usually cause distorted regions^[13,21] which could attract impurity precipitating and result in dislocation generation, significantly decreasing the minority carrier lifetime because of their strong recombination activity.^[37–39] Lantreibecq et al.^[40] observed sub-GBs with TEM and SEM. They found that sub-GBs were constituted by a set of dense, perfectly organized

immobile dislocations aligned along the growing direction and having an edge character. Oriwol et al.^[41] studied the formation of dislocation pile-ups and related sub-GBs by use of white-beam X-ray topography (WB-XRT) technique. The analysis of lattice distortion induced by WB-XRT accounted for the formation of sub-GBs having small angles' mismatch between the growth direction. A model for explaining the formation of sub-GBs from dislocation pile-ups was proposed, as shown in Figure 4 (left). At first, continuous dislocation generation occurs at GBs (A) near the solid–liquid interface. Then, they produce dislocation walls (B). Finally, the dislocations build up small-angle sub-GBs (SAGBs) (C), resulting in slightly misoriented subgrains (D). Similarly, Chuang et al.^[42] directly observed the formation of SAGBs during solidification *in situ*. They thought the SAGBs derived from dislocations aggregation at solid–liquid interface.

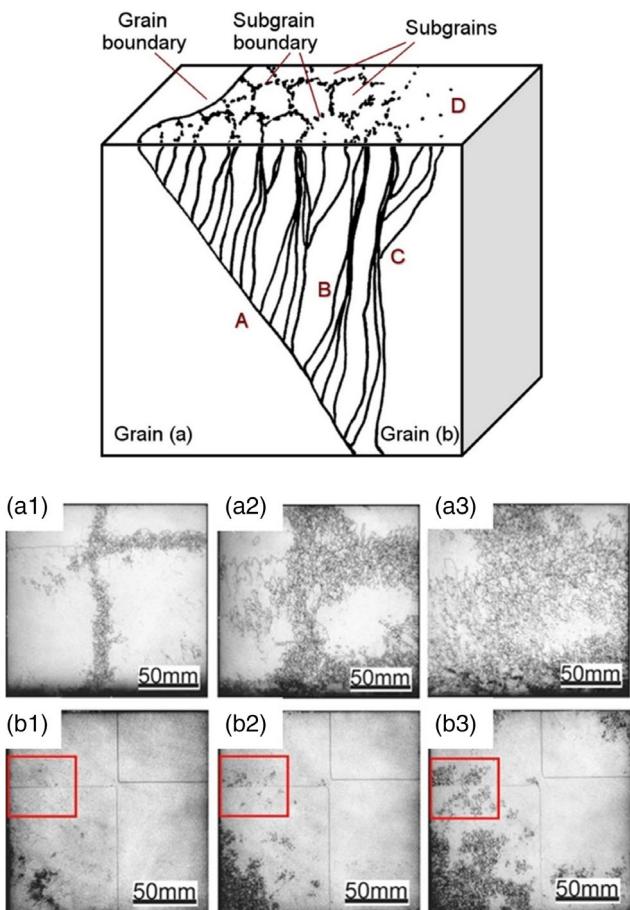


Figure 4. Left: simplified scheme of the formation of sub-GBs from dislocation pileups starting at a grain boundary. Reproduced with permission.^[41] Copyright 2013, Elsevier. Right: PL images of the wafers from the bottom (a1, b1), middle (a2, b2), and top (a3, b3) of the block of a) ingot with sub-GBs grown by a common process and b) ingot without sub-GBs grown by induced GBs. Reproduced with permission.^[23] Copyright 2015, Elsevier.

The GB misorientations would increase through the continual penetration of dislocations into the grains.

Sub-GBs and dislocations are both similar crystalline defects with strong recombination activity, so the methods to suppress dislocations can also be used to limit the generation of sub-GBs. Hu et al.^[23] reported a novel technique to grow CM-Si ingots by forming special GBs induced by controlling the pavement way of seeds at the crucible bottom, which completely suppressed sub-GBs and obtained increased minority carrier lifetime and higher internal quantum efficiency in corresponding solar cells. As shown in the red boxes of Figure 4b1–b3, the induced GBs suppress the multiplication of sub-GBs at junctions. Oliveira et al.^[43] studied the sub-GB sources and their effects on ingot quality. They found that damages on seeds caused by indentation of sharp feedstock and crystallographic mismatch between seeds were the main sources of sub-GBs nucleation. Therefore, careful alignment of seeds with minimized misorientation and preparation of the feedstock without sharp points is an efficient way to suppress sub-GB generation.

3.3. Multicrystalline Grains and Twins

During the growth of CM-Si, random nucleated grains with different crystallographic orientations occur on the inner surface of the crucible due to low formation energy there. Then, the area of these multicrystalline grains increases and finally occupies a large proportion of the single-crystal area, leading to a significant decrease in conversion efficiency of the cells fabricated by the ingot. There are mainly two ways to reduce the influence of multicrystallization on CM-Si quality. One is to suppress the nucleation on the sidewalls of the crucible as much as possible and the other is to constrict the multicrystalline area to a minimum.

Growth conditions like melt–crystal interface shape, temperature distribution, and growth rate can all affect nucleation and should be controlled carefully.^[44–46] Gao et al.^[47] numerically analyzed the generation of multicrystalline grains region near the crucible wall and found that the ratio of multicrystalline grains was mainly determined by a ratio of thermal flux along the crucible wall to thermal flux along the seed. Therefore, properly adjusting thermal flux along the crucible wall or the seeds can markedly suppress multicrystallization. Moreover, the seed preservation is also of great importance, because random nucleation from the crucible bottom will result in severe multicrystalline grains if the seeds are totally melted during growth.^[48] Li et al.^[49] investigated the key factors influencing seed preservation by carrying out transient global simulations of the feedstock melting process and found that radiant heat transfer in the furnace and downward heat flux under the crucible were main factors. Ding et al.^[50] designed movable partitions to optimize the thermal field in the hot zone and consequently obtained a suitable temperature gradient with a flat seed–melt interface. The seeds were well preserved, and CM-Si ingot with few multicrystalline grains was fabricated. A similar method could also be found in the study by Ma et al.^[45]

In contrast, multicrystalline area can be limited by defect engineering like using induced functional GBs, as mentioned in Section 3.1 and 3.2. Kutsukake et al.^[30,51] reported a method to limit multicrystalline GBs propagation in CM-Si utilizing $\Sigma 5$ GB introduced by multiseeds with specific orientations and demonstrated that functional $\Sigma 5$ GB can interact with common $\Sigma 3$ GB nucleated on crucible inner sidewalls and then form vertical $\Sigma 15$ GB to suppress multicrystallization during growth. **Figure 5** shows the suppression mechanism.

Twins are important defects, not because of their impact on electrical performance, which is very low due to their high degree of recombination, but because of their abundance,^[52] which affect the texturing process and do not fabricate high-efficiency solar cells. Twinning is closely linked to a faceted melt–crystal interface during growth. Fujiwara et al.^[53] showed the emergence of parallel twins on a faceted interface related to Si-faceted dendrite growth by *in situ* observations. Kutsukake et al.^[54] discussed the formation mechanism of twin boundaries by *in situ* observation. They found that the formation of twin boundaries was always accompanied by an obvious increase in the growth rate and twins were hardly formed when the growth rate was constant at a high value. Zhai et al.^[55] investigated the atomic mechanism of twin formation along (111), (112), (110), and (100) planes by molecular dynamics simulations. They found that twins must

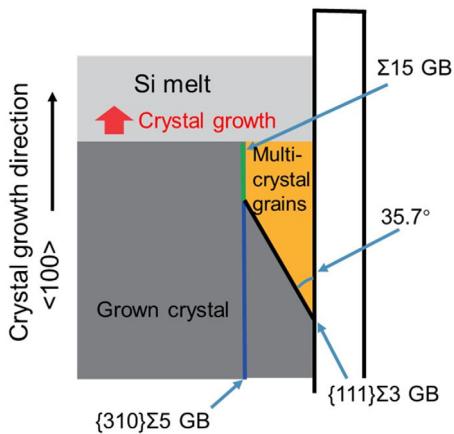


Figure 5. Schematic side view of crystal growth near the crucible wall. Reproduced with permission.^[30] Copyright 2013, The Japan Society of Applied Physics.

generate on Si {111} facets regardless of what the plane was, and the angle between the growth planes and {111} facets affected the morphology of the melt–crystal interface and further the formation of twins. They concluded that the formation probability on planes was $(111) > (112) > (110) > (100)$ from high to low, which was basically consistent with the previous reports.

Although twins are hardly electrically active, its existence still influences the fabrication process of solar cells because of different orientations from single-crystalline silicon substrate, which should also be paid attention to.

3.4. Impurities

3.4.1. Oxygen

Oxygen mainly exists in the form of interstitial oxygen (O_i) as the result of the partial dissolution of the crucible walls/coatings and further interaction with the molten silicon. The atomic concentration of oxygen is about $\approx 1.0 \times 10^{17} \text{ cm}^{-3}$, which is lower than that in Cz-Si.^[56] $[O_i]$ decreases from bottom to top in the ingots due to its segregation coefficient, ≈ 1.25 . In boron-doped silicon, O_i usually forms B–O complexes with boron,^[57–60] which significantly reduce the minority carrier lifetime and thereby reduce the cell efficiency. O_i can also form thermal donors (TDs) in the temperature range of $300\text{--}500^\circ\text{C}$,^[61–63] among which 450°C is the most effective temperature for the formation of TDs. Annealing at 650°C for 30 min can eliminate most of the TDs. In CM-Si, lower amount of oxygen than Cz-Si leads to few as-grown TDs and less boron–oxygen-related LID, which becomes an important advantage compared with Cz-Si. As another existence form of oxygen, oxygen precipitation generally occurs during the high-temperature process of CM-Si wafers. The recombination activity of oxygen precipitation mainly comes from the dangling bonds between the silicon interface and themselves,^[64–69] similar to those on silicon wafer surface. In addition, lattice distortion caused by oxygen precipitation in the silicon substrate can lead to the generation of crystallographic defects, such as stacking faults, dislocations, etc., which could act

as the main recombination centers.^[67–69] In summary, oxygen precipitates are severe defects, and therefore, they should be carefully avoided during the cell fabrication process.

3.4.2. Carbon

Carbon, existing as substitutional atoms (C_s), is mainly incorporated by CO vapor in the atmosphere, because the heaters and insulation blocks in the furnace are mainly based on carbon materials.^[70] The concentration of the substitutional carbon [C_s] is $\approx 3.0 \times 10^{17} \text{ cm}^{-3}$ in CM-Si, higher than that of $\approx 5.0 \times 10^{16} \text{ cm}^{-3}$ in Cz-Si.^[71] If the concentration of carbon exceeds its solubility limit in silicon, it will form SiC precipitates, which can cause severe ohmic shunts in solar cells. SiC precipitates also have a negative impact on the wire sawing process^[70] and result in multicrystallization,^[72] wafer warpage, and slip during processing.^[71] Therefore, it is vital to decrease the carbon impurity concentration in CM-Si for keeping the yield and improving performance of solar cells by use of feasible and convenient methods, such as using controlled atmosphere with a cap over the melt,^[73] improving the gas flow condition and SiN_x coating,^[74] or trapping it at functional defects.

3.4.3. Nitrogen

To prevent the crack of ingots and the sticking between ingots and quartz crucibles, silicon nitride has been selected as optimal coating material, and thus nitrogen is introduced in CM-Si with a concentration range of $4\text{--}6 \times 10^{15} \text{ cm}^{-3}$.^[75] Due to the weaker convection of molten silicon than Cz-Si, the segregation of nitrogen is weakened during solidification, and consequently, the distribution of nitrogen-related impurities in CM-Si ingots is more complicated. In CM-Si, nitrogen exists in the forms of monomer, dimer, complex, and precipitates, among which nitrogen dimer and N–O complex are the main forms of nitrogen in silicon under room temperature.^[76] The former is inactive, whereas the latter serves as TDs. Moreover, both of them are found to increase the mechanical strength of the wafers.^[76] The Si_3N_4 precipitates in CM-Si are in three forms: rods, fibers, and nets,^[77] whose classification and properties as well as SiC precipitates^[78] are specifically summarized in Figure 6. The Si_3N_4 rods typically grow within grain volume and have random orientations, while Si_3N_4 fibers and Si_3N_4 nets could grow in the direction of crystallization direction.^[77] All of them have high resistivity values and hence are not electrically active in most cases.^[78] However, they could introduce mechanical stress due to lattice mismatch and thus generate crystallographic defects like dislocation.

3.4.4. Iron

Iron is one of the most prominent metal impurities in CM-Si, as most equipment and devices related to ingot growth and wafer processing are mainly based on iron materials. Iron is also introduced by feedstocks and crucibles, distributing in the whole ingot. Figure 7a exhibits the graphical representation showing common origins of Fe contamination and final forms. Fe typically increases from the bottom of the ingot to the top due to very

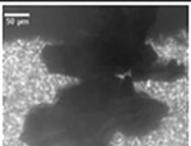
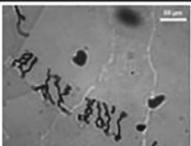
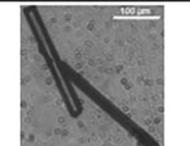
type	SiC particles	SiC filaments	Si ₃ N ₄ rods	Si ₃ N ₄ fibers	Si ₃ N ₄ nets
IR microscopy					
size	1–600 µm in diameter	<5 µm in diameter, up to 3 mm in length	<30 µm in diameter, up to 2 mm in length	<500 nm in diameter, up to 8 mm in length	<500 nm in diameter, up to 3 mm in length
morphology	compact particles, frequently in clusters showing irregular surface and consisting of monocrystalline particles showing vicinal faces	irregular diameter, rough surface, multicrystalline	polygonal diameter, smooth surface, monocrystalline	steady diameter, smooth surface, monocrystalline	irregular diameter, smooth surface, multicrystalline
local growth preference	within grain volume, often at Si ₃ N ₄ rods	mostly in grain boundaries, growing in crystallization direction	within grain volume, random orientation	within grain volume, growing in crystallization direction, branching	in grain boundaries, growing in crystallization direction
crystal structure	cubic, β-SiC	cubic, β-SiC	hexagonal, β-Si ₃ N ₄	trigonal, α-Si ₃ N ₄	trigonal, α-Si ₃ N ₄
space group	F43m (216)	F43m (216)	P63 (173)	P31c (159)	P31c (159)
lattice constants	$a = 0.436 \text{ nm}$	$a = 0.436 \text{ nm}$	$a = 0.760 \text{ nm}$, $c = 0.291 \text{ nm}$	$a = 0.775 \text{ nm}$, $c = 0.562 \text{ nm}$	$a = 0.775 \text{ nm}$, $c = 0.562 \text{ nm}$
impurities	N, Al	N, O	Li, C, O, Mg, Ca	C, O, Ca	C, O, Al, Ca
electrical resistance	$8.17 \times 10^{-5} \Omega \text{ cm}$ (4PP)	$2 \times 10^{-3} \Omega \text{ cm}$ (4PP) [28]	$>4.7 \times 10^7 \Omega \text{ cm}$ (4PP) [28]	$(5 \pm 4) \times 10^8 \Omega \text{ cm}$ (2PP)	$(1.44 \pm 0.26) \times 10^{10} \Omega \text{ cm}$ (2PP)

Figure 6. Classification of carbon- and nitrogen-correlated precipitates in crystalline solar silicon. Reproduced with permission.^[77] Copyright 2017, John Wiley and Sons.

small segregation coefficient ($\approx 8 \times 10^{-6}$). However, in CM-Si, Fe is also high at the ingot bottom due to solid diffusion from the crucible, which causes “red zone” with low minority carrier lifetime because of strong recombination related to Fe and thus significantly reduces the yield of CM-Si. Gao et al.^[79] reported a low-high-low nonmonotonic distribution of Fe at the ingot bottom, to which they attributed the back diffusion of Fe from molten silicon into the seed before solidification. Nevertheless, Yu et al.^[80] reported the similar two-peak characteristic distribution of iron impurities at the ingot bottom of CM-Si. They thought the first peak occurring at the inner face of the crucible bottom was due to iron diffusion from the quartz crucible and the second peak occurring at a height of $\approx 2 \text{ cm}$ above the initial solid–liquid interface resulted from the formation of an iron-rich layer at the initial stage of the crystallization process. The existence form of Fe in silicon is related to its solubility and diffusion coefficient, mainly including interstitial state ([Fe_i]), Fe-related complex, and precipitates.^[81–84] Fe_i could introduce deep donor levels that act as effective recombination centers and thus decrease minority carrier lifetime.^[85–88] Fe-related complexes including many species, such as Fe–acceptor pairs, Fe–point defects complexes, Fe–carbon/oxygen complexes, Fe–other metals complexes, are mostly electrically active.^[89] When Fe is supersaturated, it usually aggregates to structural defects and nucleates and grows into Fe precipitates. In addition, Fe also interacts with other defects,

such as sub-GBs, dislocations, etc., which severely enhance recombination activity and thus affect the quality of CM-Si.

3.4.5. Copper

Apart from Fe, other metal impurities from the crucible,^[91] coatings,^[91] gas phase,^[92,93] and feedstock^[93] are also able to decrease the minority carrier lifetime due to the introduction of deep-level recombination centers. For example, Cu, as the second common metal impurity in silicon, is always decorated at the structural defects, such as dislocations and GBs,^[94,95] and then forms Cu₃Si precipitates,^[96,97] which interact together with defects and become strong carrier recombination centers. In addition, Cu can also cause LID,^[98–102] of which the degree depends on the contamination amount of Cu. Schmidt et al.^[103] applied 2D device simulation to assess the impact of impurities on the performance of next-generation industrial silicon solar cells. The simulation results show that the most detrimental metal impurities in p-type silicon are Cr, Co, and Fe, whereas in n-type silicon, they are Co, Cr, and Ni. Accordingly, they thought that the other metal impurities like Co, Cr, and Ni instead of Fe might be a major reason why no higher efficiencies for cells that are based on n-type wafers have been achieved so far, compared with cells made of p-type material.^[103]

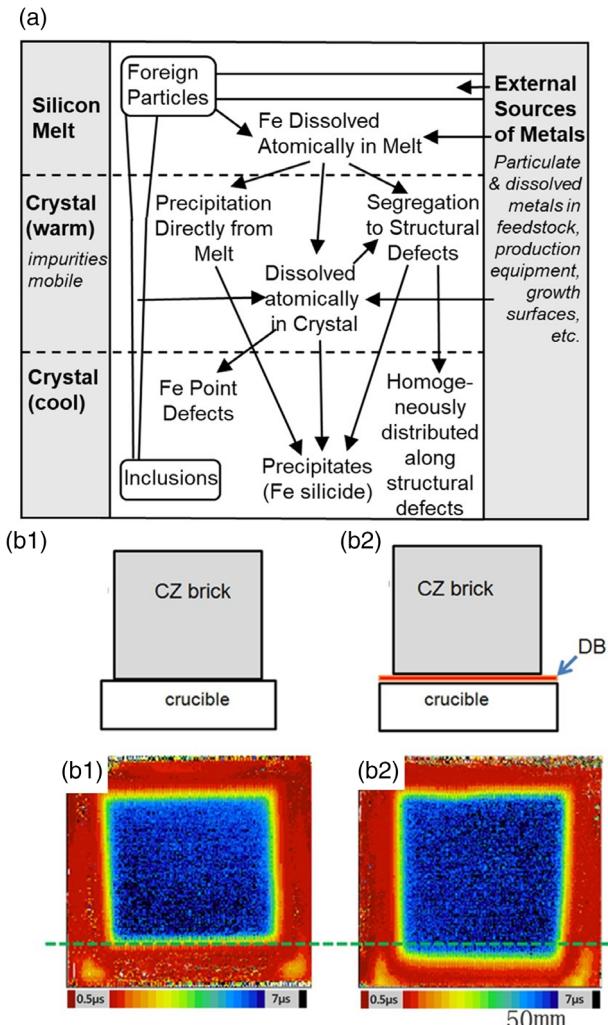


Figure 7. a) Common origins of Fe contamination and its possible final forms. Reproduced with permission.^[84] Copyright 2005, AIP Publishing. b) Illustration of annealing experiment of two monocrystalline bricks machined from one Cz rod placed on the crucible without diffusion barrier (b1) and with diffusion barrier (b2), respectively. Reproduced with permission.^[90] Copyright 2020, Elsevier.

In order to ensure the quality of CM-Si ingots, the contamination of metal impurities of all kinds should be avoided as much as possible in the whole process of feeding, growing, and processing. Hu et al.^[22] utilized GB engineering to control Fe contamination at the ingot edges, based on the grain nucleation enhanced by silicon powder coating at the crucible walls. The induced GBs paralleling to the growth direction can getter Fe and meanwhile hinder its diffusion, which significantly reduced the low lifetime area at the ingot edges. Another method is to use diffusion barrier. Zhang et al.^[90] introduced diffusion barrier fabricated by alternatively brushing silica and silicon nitride coatings with high purity on the inner bottom of the crucible to reduce the height of bottom low lifetime region. The annealing results exhibited that the diffusion barrier could effectively decrease the red zone height, as shown in Figure 7b.

Gettering is also an effective method to remove the metal impurities out of silicon substrate, which could significantly improve the quality of wafers, especially for CM-Si. Generally, gettering contains three processes: 1) dissolution of metal precipitates or other immovable states to release impurity atoms; 2) fast diffusion of impurity atoms to gettering sites; and 3) capture of impurity atoms at gettering sites. Rinio et al.^[104] investigated the influence of low-temperature p-gettering on the solar cells fabricated from the wafers near the crucible wall and the dependence on the annealing temperature and time. They found that the best improvement is obtained at about 600 °C with duration of 120 min, because the low temperature could enhance driving force of impurity motion.^[104] Internal gettering at dislocation clusters or other intrinsic defects can also enhance the electronic properties of CM-Si, because impurities are easily captured at defects due to lower energy needed.^[105] After gettering, hydrogenation is usually performed to form the H-defect complex with the impurities having shallow energy levels, which can further improve the wafer performance due to the decreased recombination activity of impurities.

4. Cost Factors

4.1. Seed Cost and Recycled Seed

The single-crystalline seeds are mainly made from Cz-Si ingots, which raises the cost of CM-Si. Therefore, the recycled ones should be focused on to decrease the cost. Zhong et al.^[106] investigated the effects of new seeds and recycled seeds on the length of the low minority carrier lifetime zone (red zone) at the bottom of CM-Si ingots. Although the recycled seed crystals obviously have higher initial impurity concentrations than the new seeds, however, there is little difference in the average length of the bottom red zone of the bricks. They inferred that the main source of impurities in the red zone is from the quartz crucible rather than the seeds, because the concentration of iron in the recycled seeds was significantly smaller than that in the crucible. He et al.^[107] compared new seeds and a large-scale recycled seed cut from a G6 CM-Si ingot bottom in the same growth. Although the recycled seed could generate extra initial defects, however, it becomes influential for solar cell performance only when defect concentration reaches a certain level, that is, the influence of dislocation clusters induced by initial defects is neglectable when the wafer height is below 55% and becomes severe at higher positions.^[107] Lei et al.^[108] used split recycled seeds to grow CM-Si. They found that the defect density in the recycled seeds increased significantly but decreased greatly during the seeding and growth. Furthermore, the average cell efficiency of the solar cells fabricated by the wafers grown with recycled seeds was only 0.1% different from that of the wafers grown with new seeds.^[108] Therefore, this low-cost seed recycling method is of great significance for reducing the cost of CM-Si.

4.2. n-type Growth of CM-Si

Due to the higher tolerance of n-type silicon to impurities than p-type silicon, n-type silicon generally has higher minority carrier lifetime and is more suitable for fabricating novel solar cells with

high power efficiency conversion like heterojunction with intrinsic thin layer (HT) and tunnel oxide-passivated contact (TOPCon). However, the wide axial distribution of resistivity owing to the small segregation coefficient of phosphorus in CM-Si ingot leads to huge production waste and incidental cost increase, because the resistivity needs to be controlled within an appropriate range to avoid large series resistance and severe Auger recombination. Increasing the resistivity of the ingot top in n-type CM-Si appears to be a good choice to promote yield and reduce the cost. Forster et al.^[109] proposed to use compensation engineering, by gallium codoping, and demonstrated its potential to control the net doping along the height of n-type ingot grown using upgraded metallurgical grade silicon feedstock that contained boron and phosphorus. In the resultant compensated material, they found an increase in the minority carrier lifetime, but the minority carrier mobility was reduced and largely counterbalanced the gain. To increase the resistivity at the ingot top, Huang et al.^[110] grew and compared n-type CM-Si ingots under different pressures to control phosphorus evaporation because of its much higher saturated vapor pressure than silicon. The results exhibited that the physical mass transfer process of phosphorus in CM-Si was a coupling result of evaporation and segregation, as shown in Figure 8a. The obtained minimum mass transfer coefficient K_G , meaning the transport of phosphorus through the gas phase to the external environment, was the controlling step, which contributed to the slight increase of resistivity under reduced pressure (≈ 300 mbar), as shown in the inset of Figure 8b.

4.3. Large-Sized Growth of CM-Si

Another method to reduce the cost of CM-Si is to improve the production capacity of single ingot by increasing the ingot size. However, larger size of the ingots means more complex thermal fields, which could lead to detrimental defects to the ingot quality. To improve the uniformity of the 3D solid–liquid (S/L) interface at the periphery of the G8 ingots that have a more complex thermal field than conventional ingots with smaller sizes, Zhang et al.^[111] developed a new structure for side heater that installs six electrodes and increased space occupancy of heaters compared with three electrodes in convectional AC heaters. The resultant interface shapes and contour plots of the 3D S/L height of the ingots demonstrated that the 3D S/L interface presented a distorted shape at the periphery of G8 ingot with traditional side heaters, while a nearly flat and highly symmetrical structure was achieved in the improved ones due to the greatly reduced Lorentz force density in the silicon melt.^[111] He et al.^[112] designed an octagonal thermal field to improve the quality of ingots with larger loading capacity. Finally, they obtained a more uniform temperature distribution and lower-temperature gradients in the octagonal furnace compared with that in the conventional furnace. Because the octagonal silicon ingot was rounder and had better effect of releasing stress, dislocation defects near the crucible wall of the ingot were reduced. Moreover, the charging weight of a single ingot was increased from 860 to 1150 kg after being modified from conventional furnace to the octagonal one.^[112] The production capacity was 24.62% higher than before, and the unit energy consumption

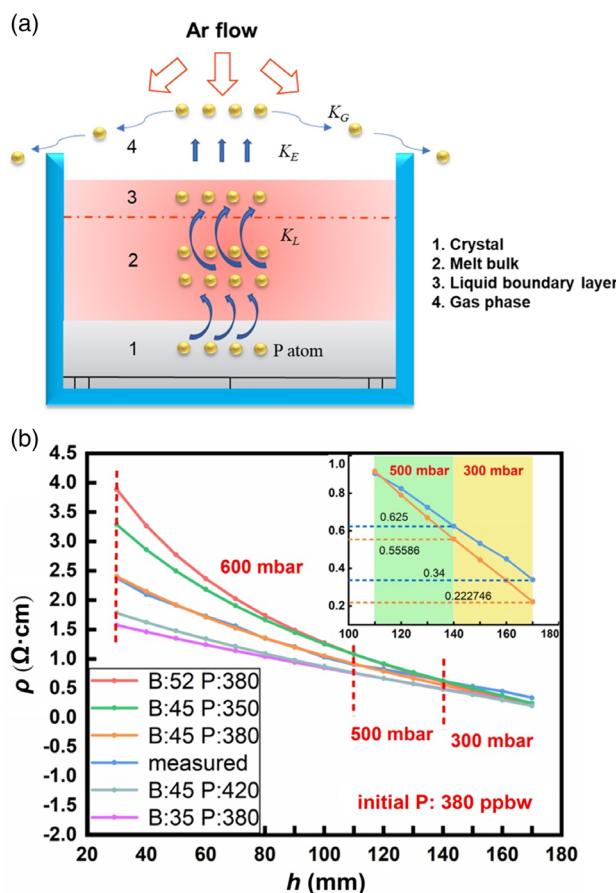


Figure 8. a) Schematic diagram of mass transfer process of phosphorus in CM-Si. b) Distribution of the measured resistivity with fitting curves at different heights in the CM-Si ingot. The inset shows a partially enlarged resistivity distribution of measured curve and fitting curve. Reproduced with permission.^[110] Copyright 2022, Elsevier.

was reduced by 14.62% than before, which exhibited great potential in reducing manufacturing costs because of the better use of furnace space, as illustrated in Figure 9.

5. Conclusion and Outlook

The CM-Si technique can provide quasi-single-crystalline silicon ingots using the same production line currently used for mc-Si ingots, which has advantages of mc-Si in terms of low cost, high production yield, uniform crystal orientation, and high crystalline quality similar to Cz-Si. However, many defects affecting crystalline quality are related to the growth process of CM-Si ingots, such as dislocation, sub-GBs, multicrystalline grains, twins, and impurity contaminants. In contrast, seed cost apart from crystalline defects also plays a vital role in limiting the development of CM-Si.

To solve these problems, advanced growth methods have been proposed on the base of fundamental studies of crystal growth and defect generation in CM-Si. For example, functional defects like SMART method and induced special GBs show promise for

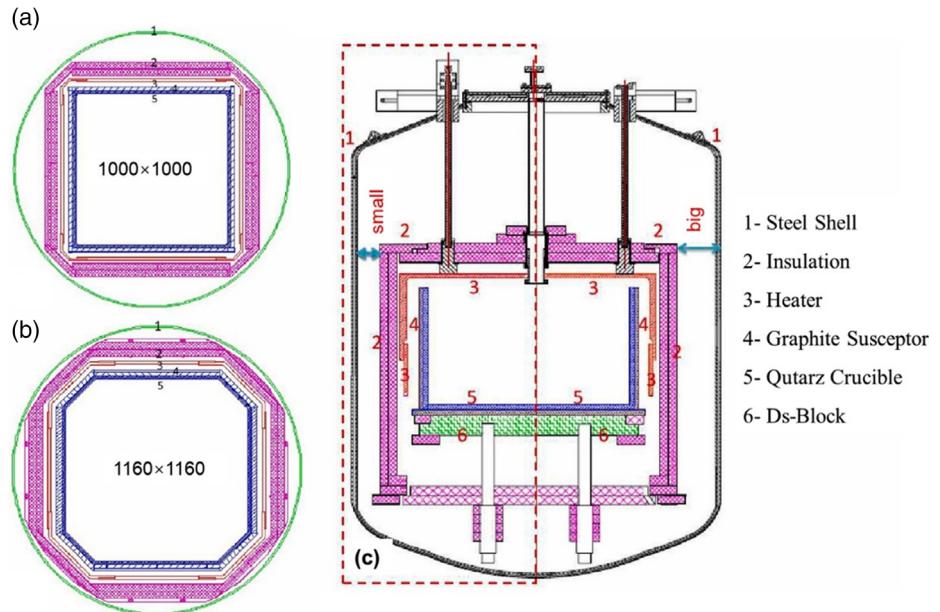


Figure 9. Schematic of the furnace of a) top view of the conventional furnace, b) top view of the modified furnace, and c) longitudinal section view of modified furnace (left) and conventional furnace (right). Reproduced with permission.^[112] Copyright 2021, Elsevier.

relieving the influence of dislocation, sub-GBs, and multicrystallization, by limiting them in the ingot edge. Designation of proper thermal field and control of seed arrangement can impede their generation to some extent as well, by decreasing the thermal and mechanical stress. In terms of impurities, using GB engineering to control impurity contamination at the ingot edges and using pure crucibles with improved coatings to obstruct impurity diffusion seem to be good choices. In addition to these methods to suppress the crystalline defects, considerable research has been reported to reduce the cost of CM-Si by recycling seeds, growing CM-Si ingots with a large size, and fabricating n-type ingots with narrow resistivity distribution to decrease production waste.

Although these methods reviewed in this paper seem promising, the development of CM-Si is still restricted due to a poorer quality and higher cost than Cz-Si. Therefore, further investigations of CM-Si will be still necessary to understand the mechanisms of the defect generation and propagation in order to grow CM-Si ingots with high quality. In addition, it has to be carefully considered if the cost of additional process steps overcompensates the potential savings on production cost. With the prolonged efforts on improving the CM-Si technique, it is feasible that the CM-Si will become the dominant material for crystalline silicon solar cells and occupy a large market share as ever.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

J.H. took care of conceptualization, data curation, formal analysis, investigation, writing the original draft, and writing the review and editing. S.Y. took care of conceptualization, data curation, supervision, funding acquisition, and resources. X.Y. took care of conceptualization, formal analysis, resources, supervision, funding acquisition, and writing the review and editing. D.Y. took care of conceptualization, resources, supervision, and funding acquisition.

Keywords

cast-mono silicon, crystal growth, defect engineering, dislocations, grain boundaries, solar cells

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