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Gold Schottky contacts on (002) CdSe films growing on p-type silicon wafer

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ABSTRACT

The thermal evaporation technique has been successfully used for depositing CdSe on p-Si (001) substrates. X-ray diffraction analysis indicated the hexagonal structure for the growing film along the (002) plane with *c*-axis perpendicular to Si-substrates. The average particle size was calculated to be ~40 nm with a dislocation density at the film surface of 6.25×10^{10} cm^{-2}. The temperature dependent electrical properties of Au Schottky contacts to *a*-plane CdSe thin films growing on p-Si (001) were investigated over the temperature range of 160–360 K, which show a rectification behavior. The barrier height (φ_b), and ideality factor (n), values were found to be 0.863 eV at 360 K to 0.451 eV at 160 K, and 2.48 ± 0.11 at 360 K to 5.18 ± 0.19 at 160 K, respectively. The increasing of φ_b while decreasing n with the increase of temperature was described by a double Gaussian distribution with two different regions in the temperature range of 240–360 and 160–240 K. Moreover, it was observed that Au/CdSe/Si/Al heterostructure exhibit space charge limited current (SCLC) at all temperatures. The transition voltage (V_x) from ohmic to SCLC is found to be quite dependent on temperature. The defect levels were estimated from the slope of ln$J$ versus $1/T$ plots, which yield two values of activation energies $\Delta E_{d1} = 0.227 \pm 0.011$ eV in the 240–360 K range and $\Delta E_{d2} = 0.128 \pm 0.003$ eV in the 160–240 K range, respectively.

1. Introduction

Among the II–VI compound semiconductors, cadmium selenide (CdSe), with a direct band gap of 1.74 eV at room-temperature (RT), has gained a great deal of attention for its potential applications

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in the fields of light amplification, gamma-detectors [1], thin film transistors [2], solar cells [3], and acousto-optic devices [4]. Different deposition techniques have been carried out to prepare CdSe; these include: chemical deposition, vacuum evaporation, molecular beam epitaxy, metal oxide molecular beam epitaxy, and Laser ablation (*c.f.* [5,6] and references cited therein). Here, the quality of a device strongly depends on both structure and electronic properties of the CdSe films which, in turn, depends on the experimental conditions [7]. In order to achieve high performance CdSe devices, it is essential to develop reliable and reproducible Ohmic and Schottky contacts. Along with Schottky barriers, ohmic contacts represent the two basic metallization technologies for semiconductor device fabrication. Ideally, a metal-semiconductor (MS), junction results in an ohmic behavior if the barrier formed by the contact is zero. In both cases, however, it is necessary for the electrical contacts to be steady with time and to operate at various temperatures and in various ambient without degradation. Nevertheless, many cases have significant deviations from the ideal Schottky barrier contacts behavior; i.e., increase in ideality factor and decrease in barrier height with temperature decrease. All specified deviations are known for some decades; however, their nature is still a subject for discussion up to date [8]. In fact, the interfacial states of the MS contacts have a dominant influence on the device performance, reliability and stability [8,9] as well as the current across the MS contact that may be greatly influenced by the presence of barrier height inhomogeneities. It is therefore necessary to understand the electrical properties of such diodes, in particular, the current–voltage (I–V) characteristics and relevant diodes parameters such as ideality factor (n), and barrier height (φ_b).

Nevertheless, a complete description of the charge carrier transport through a MS junction still remains a challenging problem [7,10–14]. An investigation of the I–V characteristics of the MS as well as homo- and heterojunction diodes that measured only at RT does not provide detailed information about the current-conduction process and the formed nature of the interface barrier. There is a barely number of studies that checked up the Au/CdSe configuration viewing spread in φ_b values [13–15], suggesting that the interface structure significantly modifies the electronic environment at the contact.

In the present study, the fabrication of Au/CdSe/p-Si/Al configuration is considered to scrutinize the forward bias I–V characteristics over a temperature range of 160–360 K, aiming to provide some detailed knowledge about the electrical properties, surface morphological evolution and the temperature dependence of Au/CdSe/p-Si/Al heterostructure parameters.

2. Experimental

Thin films of CdSe were deposited from CdSe powder (Balzers, 99·999%) by the thermal evaporation technique using Edwards vacuum coating system (model: E306A) from tungsten boat. The deposition made onto cleaned mirror polished p-Si (0 0 1) wafers at a substrate temperature of 300 K under a vacuum of 10^{-6} Torr. The used substrates were initially cleaned chemically in acetone and isopropyl alcohol ultrasonic bath and then dried using dry nitrogen, followed by a submersion of the Si wafers into an aqueous solution of hydrofluoric acid and hydrogen peroxide with a volume ratio of HF 50%:H_2O_2 30%:H_2O = 1:5:10. This solution etches wafer surfaces to eliminate the native oxide layer at the surface. Aluminum (Al) and gold (Au) electrodes were deposited from tungsten filaments. The deposition rates showed$\sim$2 nm s^{-1} (CdSe), 1 nm s^{-1} (Au), and 1 nm s^{-1} (Al), which continuously monitored using a quartz-crystal monitoring system. Ohmic contact was created at the back side of the wafer by Al (Fluka, 99.999%) electrodes. For the temperature-dependent I–V measurements, the top contact is prepared by evaporating chemically pure Au (Loba, 99.99%) with a thickness of $\sim$250 nm and diameter of 5 mm over a contact area of 0.196 cm^2. The obtained film was found to have a thickness of 792 nm, as measured by transmission spectra in the far-infrared region. After fabrication, the samples were removed to a subsidiary vacuum system maintained at RT under a pressure below 10^{-3} Torr.

The chemical composition as well as the homogeneity of the deposited semiconductor films were checked at several positions using a virtual standard analysis package on a scanning electron microscope (SEM), model: JEOL-5400, equipped with an energy dispersive analysis of X-rays (EDAX) unit comprising a Si(Li) detector. The quantification analysis was calibrated with highly pure constituent elements as standard.

The structural nature of the deposited CdSe films on both glass substrates and p-Si (100) wafers have been investigated by means of X-ray diffraction (XRD) using Phillip's computerized diffractometer (type: XPERT-MPDUC PW 3040) with Cu Kα radiation source ($\lambda = 0.15406$ nm), at a power of 1600 W (40 kV and 40 mA). The diffraction pattern was automatically recorded with a step size of 0.02° in the range $10° \leqslant 2\theta° \leqslant 80°$, where θ is the diffraction angle. The time spent for collecting the data per step was 2s.

The temperature dependent *I–V* characteristics of the Au/CdSe/p-Si diodes have been performed in the range of 160–360 K at 40 K intervals, using a temperature controlled cryostat (model: Oxford DN1714) at a chamber pressure of 10^{-5} Torr, connected to a temperature controller (type: ITC 503) with an accuracy of 0.01°. DC voltage source of type Keithley 228A is used in the 1 V range, with a resolution of 1 mV. Such resolution enables the selection of the discrimination step to be 10 mV in recording the *I–V* data. The electric current was measured using an electronic digital electrometer of type Keithley-616. The reproducibility of the recorded electrical measurements for various devices of the considered configuration was quite satisfactory and the percentage error was within acceptable limits (3%).

3. Results and discussion

3.1. Composition and structure characterization

EDXA spectrum analysis showed the composition as well as the homogeneity of the evaporated semiconductor thin film where the respective percentage of the constituent elements Cd and Se are found to be: 53.93 ± 0.22 at.% and 46.07 ± 0.22 at.% (Fig. 1).

Fig. 2 shows the experimental XRD pattern of the as-deposited CdSe/p-Si substrate which illustrates the presence of two intensive diffraction peaks, at $2\theta_{obs} = 25.425°$ and 69.285°. The first peak has been established by various authors for synthesized CdSe thin films at $2\theta_{obs} = 25.4°$ using different evaporation techniques [16–19]. Hence, the detectable peak located at 25.425° is indexed as the (002) lattice plane of the hexagonal wurtzite phase of CdSe that consistent with the value in the standard card ([JCPDS: 77-2307], with lattice parameters $a = 0.4299$ nm and $c = 0.7010$ nm).

Moreover, it is often reported that the obtained CdSe films are of a hexagonal structure which is highly oriented along the (002) plane with a *c*-axis perpendicular to the substrate. However, when $2\theta_{obs} = 69.285°$, this indicates a relation to the 4th order reflection of the (001) plane representing

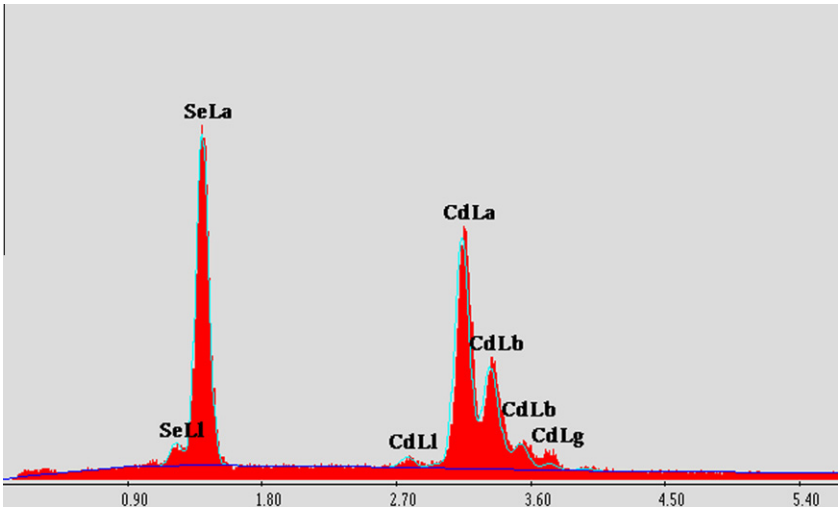

Fig. 1. Typical EDXA spectrum of CdSe Films grown on Si (100).

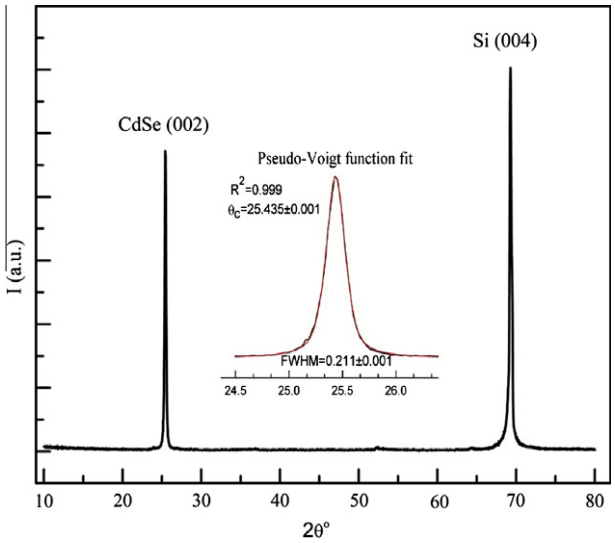

Fig. 2. XRD scans for CdSe/Si (100) with CdSe (002) reflection peak at $2\theta_{obs} = 25.425°$ and Si (400) at $2\theta_{obs} = 69.285°$. The inset shows profile fitting results for CdSe (002) peak using Pseudo-Voigt function.

the (400) feature of the Si substrate. This brought about the fact that the substrate orientation Si (001) has no effect on the formation of the hexagonal phase of the deposited CdSe films [20,21].

The peak position, (2θ) and the full width at half maximum (β_{hkl}) of the peak (002) were determined by profile fitting technique using Pseudo-Voigt function. The best-fit results were chosen taking into account the minimum error as well as the realistic values for the fitting parameters. The average crystallite size (D) of the film is estimated from the broadening of the diffraction peak using Scherrer's relation [22]:

$$D = \frac{0.94\lambda}{\beta_{hkl}\cos\theta} \tag{1}$$

where λ is the wavelength of the X-rays used. The CdSe (002) peak position at $2\theta_c = 25.453° \pm 0.001$ and the corrected peak width at half maximum (β_{hkl}) corresponding to the diffraction peak (002) is estimated to be $\beta_{002} = 0.211° \pm 0.001$ that yields an average crystallite size of ~40 nm as shown in Fig. 2.

The Si (001) plane is of a square profile that is unmatched with the hexagonal lattice in CdSe (002) plane. Therefore, the lattice mismatches ($\Delta a/a_{sub}$) between CdSe film in the hexagonal phase and Si (001)-oriented substrate, resulted to be ~21%. Due to the large lattice mismatch, there is a relatively high prediction for the possibility of a weak bonding strength between CdSe/Si. This result is in good conformity with the analysis of the XRD spectra of CdSe films grown on Si (001) reported by Perna et al. [21]. Similarly, the lattice mismatch between Au and CdSe was found to be ~8.5. In such a way, the produced interface must generate structural defects and dislocations on the CdSe film in the short range. The dislocation density (δ) has been evaluated using Williamson and Smallman formula [23]:

$$\delta = \frac{l_f}{D^2} \tag{2}$$

where l_f is the number of dislocations along each face. Assuming $l_f = 1$, as a minimum estimated dislocation density in the considered CdSe film, δ is found to be $6.25 \times 10^{10}\ \mathrm{cm}^{-2}$. Fig. 3 shows the dislocations network of CdSe (002) film grown on Si (001) substrate. The average dislocation density, δ, was estimated to be $9.77 \times 10^{10}\ \mathrm{cm}^{-2}$ from SEM image (Fig. 3). Ponce et al. [24] mentioned an

interesting conclusion; i.e., that is large lattice mismatch leads to high dislocation densities of 10^7–10^{11} cm^{-2}.

3.2. Current–voltage–temperature (I–V–T) analysis

Fig. 4 dedicated a set of semi-logarithmic plots for the *I–V* characteristics of the investigated Au/CdSe/p-Si/Al heterostructural configuration in both forward and reverse biasing as measured in the temperature range of 160–360 K. This figure declares three features during the considered temperature range: (I) strong temperature dependence of both forward and reverse currents; (II) the current increases nonlinearly with the biased increase due to the effect of some parameters such as the series resistance (R_s), interfacial layer and interface state [25]; and (III) near-symmetrical *I–V* characteristics. By using the thermionic emission model, the parameters that describe a current flow can be represented by the equation [26]:

$$I = AA^{*}T^{2}\exp\left(-\frac{q\varphi_b}{kT}\right)\left(\exp\left(\frac{q(V-IR_S)}{nkT}\right)-1\right) \tag{3}$$

where $I_s = AA^{*}T^{2}\exp\left(-\frac{q\varphi_b}{kT}\right)$, is the reverse saturation current, q is the elementary charge, k is the Boltzmann constant, T is the absolute temperature, n is the ideality factor. The IR_S term represents the voltage drop across the series resistance (R_S) of the configuration, $A^{*} = 4\pi qm^{*}k^2/h^3 = 120(m^{*}/m_o)$ is the Richardson constant of 15.6 $cm^{-2}K^{-2}$ for CdSe, where $m^{*} = 0.13\ m_o$ [27], A is the geometric diode area and φ_b is the apparent barrier height of the diode which is the energy necessary to transport a metal electron into the semiconductor conduction band. The change in temperature has essential effects on determination of the main diode parameters, such as φ_b, n, and R_s, to provide detailed information about the current-conduction process as well as the nature of the formed interface barrier.

Nevertheless, the *I–V* characteristics of a real diode are modeled by a series combination of a diode and a resistance through which the current flows. Here, a linear region can be found by plotting $\ln(I)$ versus V at $V \geqslant 3kT/q$, as shown in Fig. 5. The values of both n and I_s can thus be determined from the experimentally obtained forward *I–V* characteristics at a given T. The value of I_s can be evaluated by extrapolating the linear region of the function $\ln(I) = f(V)$ to $V = 0$; and n can be determined from

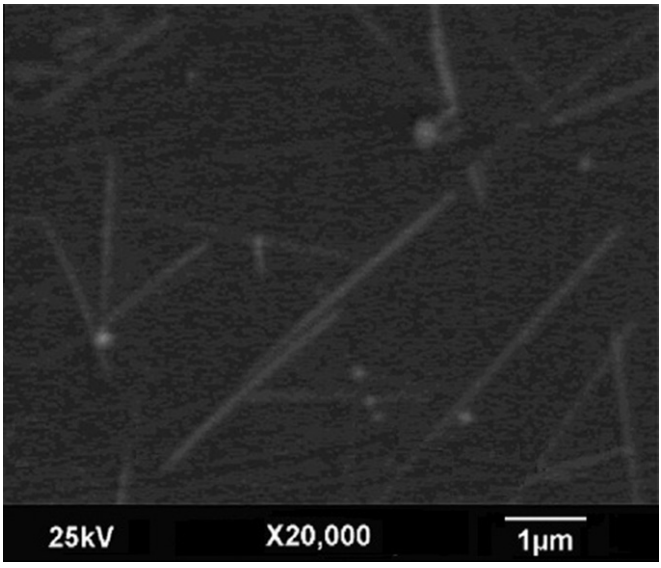

Fig. 3. SEM plan-view micrograph of CdSe/Si (100) interface showing the dislocation network.

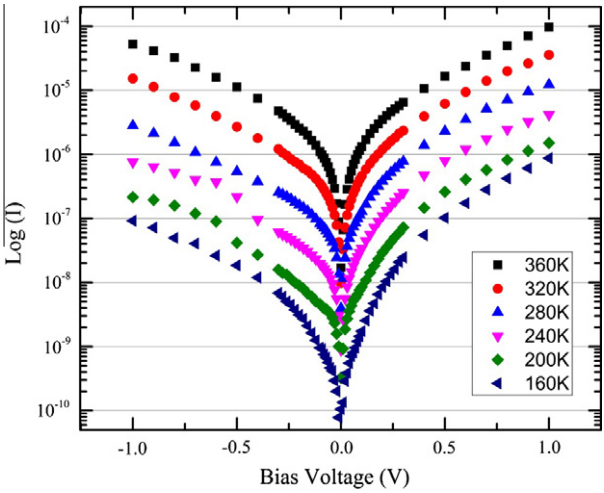

Fig. 4. *I–V* characteristic curves of Au/n-CdSe/p-Si/Al at different temperatures.

$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right)$ that is based on neglecting the series resistance of the diode. The series resistances of the diode were calculated by applying the following equation:

$$\left(\frac{dV}{d\ln I}\right) = IR_S + \frac{nkT}{q} \tag{4}$$

$$H(I) = IR_S + n\frac{\varphi_b}{q} \tag{5}$$

Plotting $dV/dln(I)$ versus I yields a straight line whose slope gives the specific series resistance, R_s; also, the y-axis intercept gives the ideality factor, n, according to Eq.(5). The slope of plot of $H(I)$ versus I, also, provides an alternative determination of R_s by which the consistency of Cheung's approach [28] can be checked. It is obvious from Fig. 5 that the concavity of the curve in the forward bias *I–V* characteristics increased with increasing the series resistance, which decreased with increasing the

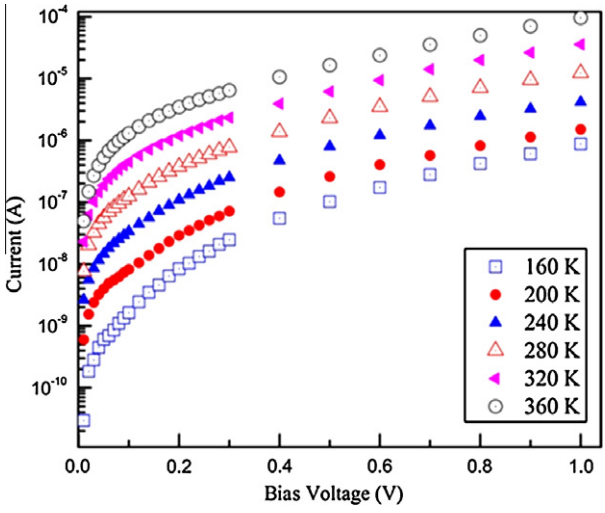

Fig. 5. Semi-logarithmic plots of *I–V* characteristic for Au/CdSe/p-Si heterostructure diodes at different temperatures.

temperature. Using the ideality factor value extracted from the $dV/d\ln(I)$ versus I plot, the value of φ_b can be determined from Eq. (4). Table 1 summarizes the quantitative determined values of the diode parameters (φ_b, n, I_s and R_s) for the considered temperature range of 160–360 K. As can be seen from the results of Table 1, the values of R_s obtained from the H(I) versus I plots are approximately equal to those obtained from the $dV/d\ln(I)$ versus I plots, which confirm the consistency of the technique of Cheung and Cheung as well as the values of the other two parameters φ_b and n. In addition, the change of the reverse saturation current of the diode with temperature indicates a change in the barrier height while increasing temperature; i.e., $n = 2.48 \pm 0.11$ at 360 K to 5.18 ± 0.19 at 160 K; whereas φ_b decreases from 0.863 eV at 360 K to 0.451 eV at 160 K. A higher value of n corresponds to an effectively lowered barrier height. On other hand, the increase in R_s with decreasing T is one of the factors responsible for the increase in n and, consequently, the decrease in φ_b [28]. This means that the current is not limited by drift and diffusion or by recombination in the space charge region. On other hand, it could result from the presence of nonlinear MS contact [29].

Previous researches have shown proven the existence of analogous behavior of Au/CdSe without taking into consideration the structure of the films, where the variation in the values of φ_b and n, are observed as being 0.465–0.515 eV and 4.6–3.5 in the temperature 280–330 K range [30], and 0.632–0.666 eV and 4.7–2.2 in the temperature range of 300–350 K [31], respectively.

Clearly, the variation in the values of φ_b and n demonstrates that both decrease in n and increase in φ_b while increasing T refer to a deviation from the pure thermionic emission–diffusion theory. Such an unusual behavior of both φ_b and n, cannot be explained on the basis of thermionic emission–diffusion model. But, incorporation of the concept of inhomogeneities into thermionic emission–diffusion theory can be a satisfactory account for such observed changes [32]. As described earlier, inhomogeneities are imperfections at the interface between two materials. The results and analysis of the XRD reveal such kind of disordered interface between CdSe/Si and Au/CdSe, primarily because of the value of the lattice mismatch. Other possible reasons for this behavior could be the dislocation density of CdSe films (δ) that could act on both interfaces Au/CdSe and CdSe/Si. According to previous studies, dislocations create a potential well at their cores and the electrical barriers besides the well, which reduce the electron mobility, especially at near interface-region [33,34]. In return, this could explain the high values of R_s. In this context, Werner et al. [35] reported that the atomic structure of the interface itself, i.e. coordination of the metal atoms and structural defects in the interface, is expected to strongly influence the barrier heights. The deviation from stoichiometry determined by EDXA involves native point defects in the deposited CdSe films, such as Se vacancies and/or Cd interstitials. Therefore, a growing body of literature on SBDs is dedicated towards understanding the deviation from ideality and effects of barrier height inhomogeneities on transport properties [36].

3.3. Inhomogeneities barrier analysis

Fig. 6 shows that the value of φ_b increases with increasing T, whereas the value of n decreases with increasing T. The high values of n, depend, however, on the diode temperature, shows that the transport properties of the diode are not only well-modeled by thermionic emission but there is a current

Table 1
Temperature dependent values of the parameters determined from the forward bias I–V characteristics of Au/CdSe/p-Si/Al diode in the temperature range of 160–360 K.

T (K)	I_s (A)	n		R_s (KΩ)		φ_b (eV)	φ_b (eV)
	$\ln(I)$ versus V	$\ln(I)$ versus V	$\frac{dV}{d\ln(I)}$ versus I	$H(I)$ versus I	$\frac{dV}{d\ln(I)}$ versus I	$\ln(I)$ versus V	$H(I)$ versus I
160	4.85×10^{-10}	5.18 ± 0.19	5.35 ± 0.11	1300 ± 60	1250 ± 59	0.451	0.448
200	2.56×10^{-09}	4.95 ± 0.11	4.92 ± 0.12	527 ± 10	667 ± 17	0.543	0.542
240	1.25×10^{-08}	4.58 ± 0.14	4.56 ± 0.30	188 ± 10	222 ± 23	0.627	0.631
280	3.98×10^{-08}	3.57 ± 0.01	3.51 ± 0.18	92 ± 1	99 ± 8	0.711	0.703
320	1.38×10^{-07}	3.12 ± 0.12	2.90 ± 0.15	41 ± 1	49 ± 4	0.785	0.777
360	3.37×10^{-07}	2.48 ± 0.11	2.35 ± 0.23	18 ± 0.2	21 ± 1.5	0.863	0.845

flow parameter through the lower barrier height when it builds up with increasing both T and bias voltage.

From a microscopic point of view, and according to the model proposed by Tung [37] and Sullivan et al. [38], an inhomogeneous Schottky contact can be depicted as a distribution of nanometer-size "patches" with lower barrier height embedded within a high barrier background [28]. On the other hand, many authors developed analytical expressions to describe the effects of barrier heights inhomogenties (BHI) on the I–V–T characteristics of a Schottky diode. Here, Chand and Kumar [32] pointed out that the temperature dependence of barrier height and the ideality factor from the vast majority of MS interface are consistent with the presence of Schottky barrier height inhomogeneity referring to the Werner–Gütler's potential fluctuation model [35]. This model proposed that the observation of non-ideal diode behavior can be explained by assuming a Gaussian distribution of Schottky barrier heights with a mean barrier height, φ_{bm}, and a standard deviation σ_s, according to the following expression [39,40]:

$$\rho(\varphi_b) = \frac{1}{\sigma_s\sqrt{2\pi}}\exp\left(-\frac{(\varphi_b - \varphi_{bm})^2}{2\sigma_s^2}\right), \tag{6}$$

where φ_b is the apparent barrier height, φ_{bm} is the mean barrier height, σ_S is the standard deviation and $\frac{1}{\sigma_s\sqrt{2\pi}}$ is a normalization constant. The Gaussian distribution of the barrier heights with a mean value φ_{bm} and a standard deviation yields the following expression:

$$\varphi_b = \varphi_{bm} - \left(\frac{q\sigma_S^2}{2kT}\right) \tag{7}$$

The observed variation of the ideality factor n with temperature in the above model is given by:

$$\frac{1}{n} = 1 - \gamma + \frac{\sigma_S q\xi}{kT} \tag{8}$$

where the coefficients γ and ξ measure the voltage deformation of the barrier height distribution; while φ_{bm} and the barrier distribution width are given by coefficients γ and ξ, respectively.

Conspicuously, the data fitting show two straight lines with different slopes over the investigated temperature ranges of 240–360 K and 160–240 K, according to Eqs. (7) and (8). This confirms the presence of two Gaussian distributions of barrier heights in the contact area over the temperature range

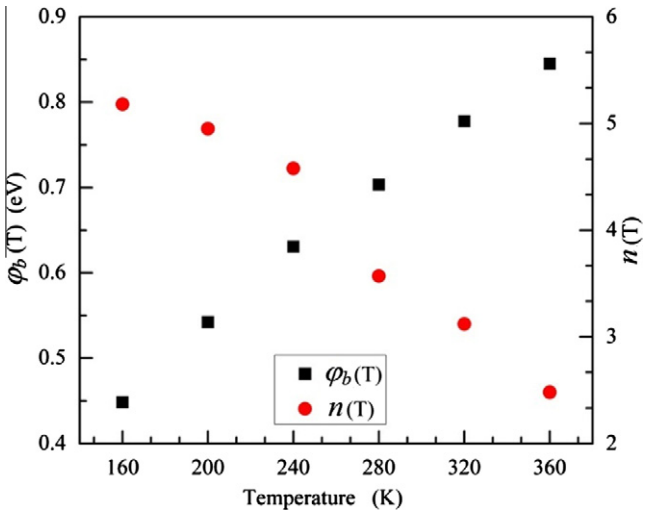

Fig. 6. Temperature dependence of barrier height (φ_b) and ideality factor (n) of Au/CdSe/p-Si heterostructure diodes.

investigated. The second Gaussian distribution is barely different from the first one but pertinent only to the lower temperature region. Therefore, the double Gaussian model is applied to the temperature dependent distribution of the barrier height values in the temperature ranges 240–360 and 160–240 K. The intercepts and slopes of these straight lines yield two values sets for φ_{bm} and σ_S as: 1.26 ± 0.04 eV and 0.162 ± 0.013 V in the 240–360 K range and 0.98 ± 0.04 eV and 0.122 ± 0.011 V in the 160–240 K range, respectively. Accordingly, the percentage of σ_S/φ_{bm} is found to be ∼12% in both temperature ranges. Interestingly, Chand and Kumar [39] mentioned that the standard deviation always lies within 7–12% of the mean barrier height. Here, the standard deviation is a measure of the barrier homogeneity. These values of σ_S are not small compared to their respective φ_{bm} values, and this indicates the existence of larger inhomogeneities at the interface of Au/CdSe. Similarly, the temperature dependence of n can be understood on the basis of Eq. (8). It indicates that $1/n$ versus $1/T$ plot should yield a straight line with slope giving $\frac{q\xi}{2k}$ and intercept $(1-\gamma)$. As a result, $1/n$ versus $1/T$ plot shows two temperature ranges due to the contact referring to two barrier height distributions. This is obviously the present case (see Fig. 7) as the data clearly fit with two straight lines for the temperature ranges: 240–360 K and 160–240 K. The corresponding respective values of ξ are -0.0509 ± 0.006 and -0.1019 ± 0.012 for the two temperature ranges, as obtained from the lines slopes. Whereas, the values of γ obtained from the intercepts are 0.72 ± 0.04 and 0.19 ± 0.01 in the respective temperature ranges. The negative value of ξ coupled with the positive value of γ disclosed that the increase of n with fall in temperature arises due to the third term containing ξ in Eq. (8). As can be seen easily, Fig. 8 shows the excellent fitting of the experimental φ_b and n with the calculated by using parameters given by Eqs. (7) and (8), two straight lines over the investigated temperature ranges of 240–360 K and 160–240 K, respectively.

3.4. Space charge limited current model

Temperature measurements allow the determination of extra information concerning the thin film material. In Fig. 9, *I–V* characteristics are shown for Au/CdSe/p-Si/Al; two distinct regimes exist in each of the characteristics. A properly well-defined transition voltage V_x, derived from each characteristic by obtaining the intersection point of the two linear sections of the logarithmic characteristics. *I–V* characteristics at low voltages, $V < V_x$, I is proportional to V (the slopes of the log I-log V curves are approximately unity, region I) specifying an Ohmic transport, which indicates that the density of thermally generated free carriers inside the films is larger than the injected carriers. The injected carrier

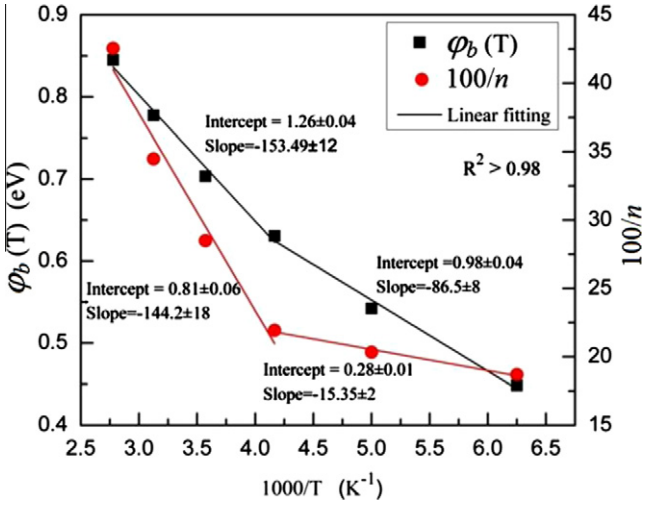

Fig. 7. Plot of the experimental values of φ_b and $1/n$ versus $1/T$ for Au/CdSe/p-Si diode.

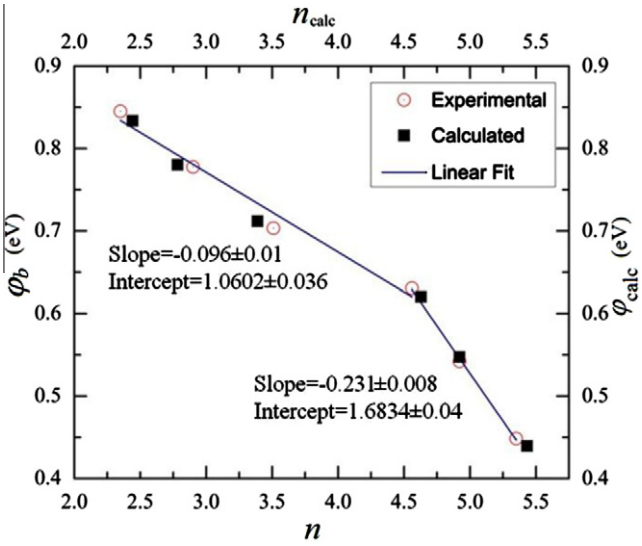

Fig. 8. Least-squares fit of φ_b versus n in the temperature ranges of 160–240 and 240–360 K.

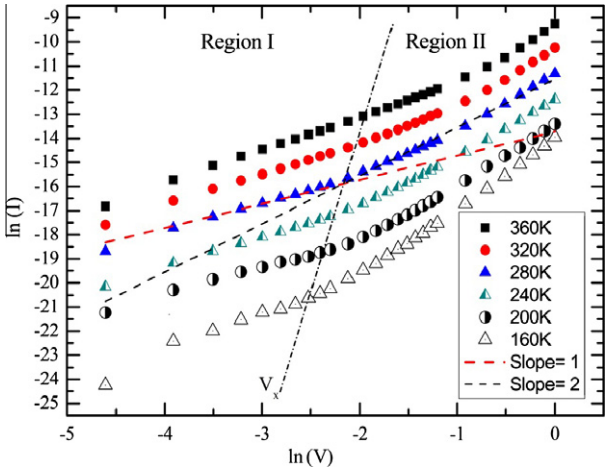

Fig. 9. Plots of $\ln(I)$ versus $\ln(V)$ of the Au/CdSe/p-Si heterostructure at various temperatures.

would thus undergo dielectric relaxation to maintain the charge neutrality rather than transport across the sample. This Ohmic mode takes place in the electrically quasi-neutral state corresponding to the situation when partial trap centers are filled at weak injection. As the applied voltage is larger than V_x, the injected carrier dominates over the thermally generated carrier. The increase of the applied voltage also shifts the quasi-Fermi level towards the conduction band and the effect would be the filling up of the trap at the energy level of $(E_C - E_t)$. As the applied voltage further increases to the extent that all the traps are filled i.e., the conduction would become SCLC and the current fit to the power-law of type $I \propto V^m$. Concerning temperature dependence, the determined exponent (m), varies from $m = 2.02$ at $T = 360$ K to $m = 2.86$ at $T = 160$ K. As is well known, the deviation from stoichiometry in II–VI semiconductors creates principally a large number of localized defect states in their forbidden gap [41]. These localized defect states act as carrier trapping centers; when carriers injected

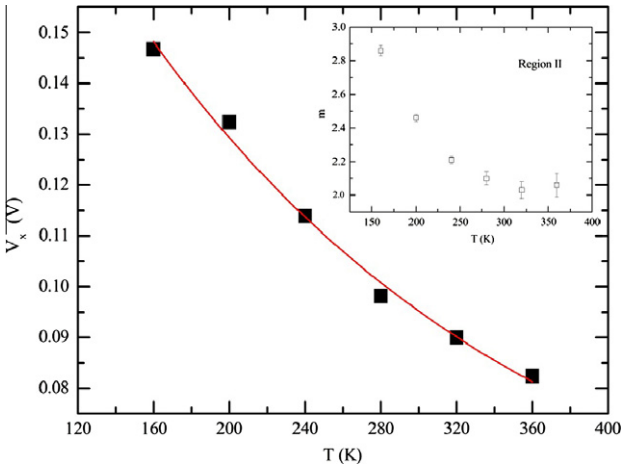

Fig. 10. Variation of V_X values with temperature for Au/CdSe/p-Si heterostructure, and the inset shows the variation of m against the temperature.

Table 2
Temperature dependent values of SCLC parameters.

T (K)	m	l	T_t (K)	V_x (V)
160	2.82 ± 0.03	1.82	291.2	0.147
200	2.45 ± 0.02	1.45	290.0	0.132
240	2.23 ± 0.02	1.23	295.2	0.114
280	2.12 ± 0.04	1.12	336.0	0.098
320	2.06 ± 0.05	1.06	339.2	0.090
360	2.26 ± 0.09	1.26	453.6	0.082

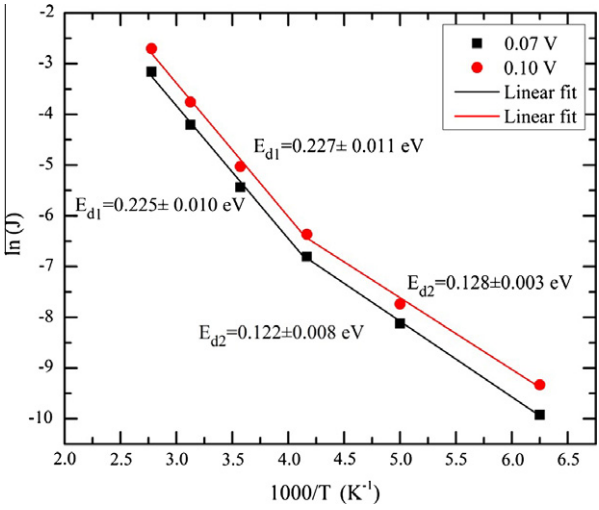

Fig. 11. Arrhenius plots of ln(J) versus 1000/T for Au/CdSe/p-Si heterostructure.

from the electrodes, they are trapped in these centers, so this localized states become charged. Consequently, Space-charge regions may originate from traps in the band gap induced by structural defects often presented in CdSe thin films. In addition, the absence of any near vertical regime in the $\ln(I)$ versus $\ln(V)$ plots indicates the traps are continuously distributed rather than discrete [42]. Noticeably, V_x goes down as the temperature increasing and the inset graph of Fig. 10 shows the variation of the m of the second region going to be about 2 as the temperature increasing. There is another form of the power-law, which can be given by:

$$J = \frac{q\mu N_c}{d^{2l+1}}\left(\frac{\varepsilon\varepsilon_0}{P_0 T_t}\right)^l V^{l+1} \tag{9}$$

where μ is the mobility of carrier charge, N_c is the effective density of states in conduction band, d is the thickness of sample, ε is the dielectric constant of semiconductor, ε_0 is the permittivity of free space, P_0 is the trap density per unit energy range at the conduction band, and l is a parameter given as $l = m - 1 = \frac{T_t}{T}$. T_t is a characteristic temperature of the exponential distribution of traps. Consequently, using the obtained m values; the T_t characteristic temperatures for trap distributions for Au/CdSe/p-Si/Al heterostructure have been calculated and listed in Table 2 together with the corresponding l values at various temperatures.

In the region I (Ohmic), activation energy (E_d) can be calculated from the temperature dependence of the I–V curves at $V = 0.07$ V and $V = 0.1$ V by plotting $\ln(J)$ versus $1/T$, the slope of which is $(E_d - E_c)/k$. Undoubtedly, Fig. 11 shows the data revealing that there are two fitting straight lines with different slopes over the investigated temperature ranges of 240–360 K and 160–240 K. The slopes of these straight lines yield two values of activation energies $\Delta E_{d1} = 0.227 \pm 0.011$ eV in the 240–360 K range and $\Delta E_{d2} = 0.128 \pm 0.003$ eV in the 160–240 K range, respectively. The small activation energy was attributed to the shallow traps, existing near the conduction of the CdSe thin films. Since the thermal generation of the carriers increases with temperature, relatively lower voltage is required to fill all the trap levels at higher temperature.

4. Conclusion

CdSe films of 792 nm thick have been successfully grown on a p-Si (100) by thermal evaporation technique with excellent adherence and good crystallinity. The structural characteristics of the CdSe films were composed of a single hexagonal phase with highly intensive peak (002) plane. The silicon orientation has no effect on both phase growth and crystalline qualities. In conclusion, the temperature-dependent forward-bias I–V characteristics of the Au/CdSe/p-Si/Al heterostructure were measured in the temperature range of 160–360 K. It was observed that there exists the variation in barrier heights with a double Gaussian distribution, one is for high temperature region 240–360 K and the other is for low temperature region 160–240 K, that explained the temperature dependent of the ideality factor and barrier heights. The increase of series resistance R_s as the temperature decreases is believed to be resulted due to factors responsible for increasing n and/or lack of free-charge carriers concentration at low temperatures. Space-charge regions may originate from traps in the band gap induced by structural defects often presented in CdSe thin films. The estimated localized defect states were found to be $\Delta E_{d1} = 0.227 \pm 0.011$ eV in the 240–360 K range and $\Delta E_{d2} = 0.128 \pm 0.003$ eV in the 160–240 K range, respectively.

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