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On the temperature dependent forward bias current–voltage (I–V) characteristics in Au/2% graphene–cobalt doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure

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ABSTRACT

In order to good interpret of temperature dependent main electrical parameters in Au/2% graphene–cobalt (GC) doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure, forward bias current–voltage (I–V) characteristics have been investigated in the temperature range of 80–340 K. The possible current-conduction mechanisms (CCMs) in this structure was also investigate in detail. The ideality factor (n), reverse saturation current (I_o), and zero-bias barrier height (Φ_{Bo}) values were found as 14.5, 7.2×10^{-6} A, 0.141 eV at 80 K and 3.18, 1.7×10^{-3} A, and 0.526 eV at 340 K, respectively. It is clear that both the value of n and Φ_{Bo} are strong function of temperature. While the value of n decreases with increasing temperature, Φ_{Bo} increases. In order to explain such behavior of BH the Φ_{Bo} and n, Φ_{Bo} vs $q/2kT$, Φ_{Bo} vs n, and $(n^{-1}-1)$ vs $q/2kT$ plots were drawn to obtain an evidence of a Gaussian distribution (GD) of the BHs and it shows a straight line. The mean value of BH ($\overline{\Phi}_{Bo}$) and standard deviation (σ_s) were found from the slope and intercept of this plot as 0.614 eV and 0.088 V, respectively. By using the modified Richardson plot, the $\overline{\Phi}_{Bo}$ and Richardson constant (A^*) values were obtained from the slope and intercept of this plot as 0.604 eV and 108.23 A cm^{-2} K^{-2}, respectively. It is clear that this value of A^* ($=$108.23 A cm^{-2} K^{-2}) is very close to the theoretical value 112 A cm^{-2} K^{-2} for n-Si. In conclusion, the temperature dependence of the forward bias I–V characteristics of the structure can be successfully explained on the basis of a thermionic emission (TE) mechanism with GD of the BHs.

1. Introduction

Metal-semiconductor (MS), metal-insulator/polymer-semiconductor (MIS or MPS) type Schottky barrier diodes (SBDs) play an important in the semiconductor industry and also the formation Schottky barrier height (SBH) at M/S interface and conduction mechanisms in these devices are very sensitive to the thermal treatment. The performance and reliability of these devices are also dependent on various parameters such as the processing of surface, interface traps (D_{it}), impurity or dislocation level of the semiconductor, sample temperature, the concentration of doping atoms, applied bias voltage, BH and interfacial layer inhomogeneity and series and shunt resistances (R_s and R_{sh}) of the device. Therefore, the fabrication of thermal stable such devices with high BH, high rectifier rate, low series resistance, low leakage current, and barrier homogeneity still up till presents a challenge problem. Due to

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these reasons, the electrical characteristics of these devices have been extensively studied both experimentally and theoretically, [1–11], but most of these studies were limited to the determination BH, ideality factor (n), R_s and D_{it} at room temperature or above temperatures and applied bias voltage by using current–voltage (I–V) and capacitance–voltage (C–V) measurements. On the other hand, the measurements at only room temperature does not give detailed information to us about their CCMs or nature of BH at M/S interface. In other word, if we want to get more information both on CCMs and the nature of BH, these measurements must be performed in the wide temperature and applied bias voltage ranges.

The analysis of the I–V characteristics of these devices based on thermionic emission (TE), usually reveals an abnormal increase in BH and a decrease in the ideality factor with an increase in temperature [12–17]. Such behavior of BH especially at low temperatures leads to a deviation from linearity in the activation energy or Richardson, $\mathrm{Ln}(I_o/T^2)$ vs q/kT, plot. There are a lot of studies in the literature on such behavior of BH and n with temperature in the last three decades [12–20]. They have been successfully explained on the bases of TE theory with GD of the BHs. In addition, BH and n are the fundamental parameters of these devices and strongly effect the quality of devices performance. The high value of n especially at low temperatures can be raised from five different sources: (1) Interface traps and interfacial layer native or deposited between metal and semiconductor [1,21–23]; (2) tunneling current in high doped semiconductor and at low temperatures [24–26]; (3) image force lowering of the BH in the high electric field at M/S interface [1]; (4) generation–recombination (GR) current with the space charge [27]; and (5) inhomogeneous BH with a distribution of low BHs at around mean BH. Also the use of high dielectric materials at M/S interface as an interfacial layer such as insulator or oxide, polymer and ferroelectric materials play an important role on the performance of these devices. Their main advantages are low density of D_{it}, R_s, leakage current and high R_{sh}, rectifier rate ($\mathrm{RR}=\pm I_F/I_R$). Because, such an interfacial layer not only prevents inter-diffusion between metal and semiconductor, but also alleviate the electric field reduction issue in these devices. However, the formation of such interfacial layer on the semiconductor by traditional ways cannot completely passive the active dangling bonds at the semiconductor surface. There are many experimental and theoretical studies in the literature on MPS type SBDs in two decades [3,5–9,18], but in detail information on the nature of BH and CCMs are also not available especially at low temperatures. Because, the temperature dependent of the forward bias I–V characteristics allows the identification of the various conduction mechanisms and nature of BH at M/S interface. For example, while thermionic-field emission (TFE) and field emission (FE) mechanisms become dominate at low temperatures and high doped semiconductors, TE become dominate at room and above temperatures. That is why, the investigation of conduction mechanisms especially in high doped semiconductors and low temperatures is very important subject. Due to the technological importance, graphene–Si contact devices and their full understanding of the nature of electrical characteristics is also great interest in recent years [28]. Because, it is a zero-gap semiconductor and has very large intrinsic carry mobility.

In light of the above description, the analysis of the I–V characteristics only at room temperature does not give detailed information about their conduction process/mechanisms or the nature of current conduction mechanisms (CCMs) and barrier formation at the M/S interface [2,12–18]. On the other hand, the temperature dependence of the I–V measurements in a wide temperature ranges allows us to understand different aspects of the current conduction process. Therefore, in this study, in order to good interpret of temperature and voltage dependence main electrical parameters in Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure, forward bias I–V characteristics have been investigated in the wide temperature range of 80–340 K. The 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer was grown on the front of Si wafer after the formation of ohmic contact because of its easy of processing, cost and compatibility with Si.

2. Experimental details

The Au/n-Si (MS) type Schottky barrier diodes (SBDs) with interfacial 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer were fabricated on P-doped (n-Si) single crystal with 0.001–0.005 Ω cm resistivity from the manufacturer, (100) orientation and ~250 μm thickness. Firstly, n-Si wafers were ultrasonically cleaned in trichloroethylene and ethanol, etched by CP4 (HNO_3:HF:$COOHC_2H_5$:H_2O=3:1:2:2 weight ratio) solutions at about 30 s and they were rinsed by propylene glycol and blown dry with nitrogen gas (N_2). After that wafers were etched in a sequence of H_2SO_4 and H_2O_2 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally rinsed in the de-ionized water with 18 MΩ cm resistivity. All cleaning processes were carried out in the ultrasonic bath. After cleaning processes, immediately n-Si wafers were transferred into the high vacuum metal evaporation system and then high purity Au (99.999%) with 1500 Å thickness was thermally evaporated onto the whole back side of n-Si wafer at about 10^{-6} Torr. In order to perform low resistivity back ohmic contact, wafers were annealed at 500 °C in the nitrogen ambient at about 5 min. This annealing process serves metal collapse into the semiconductor. After formation of ohmic contact, 2% graphene–cobalt doped ($Ca3Co4Ga0.001O_x$) interfacial layer was prepared in PVA solution on the n-Si wafers using the electro-spinning technique. Because, if we use the electro-spinning technique instead of the spin coating technique, we produce nanofibers and these nanofibers coated in the substrate increase the electrical conductivity even more than 20 times with respect to the spin coating technique. That is why we choose nanofibers technology. The scheme of the electro-spinning system can be seen in previous study [28] in Fig. 1. The growth processes of 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer on the front of the n-Si wafer is given as follows:

Polyvinyl alcohol (PVA-Mw 85.000–124.000 g/mol) was used as the polymeric precursor and it was supplied from Sigma-Aldrich. Calcium acetate hydrate (ReagentPlus®, ≥99%

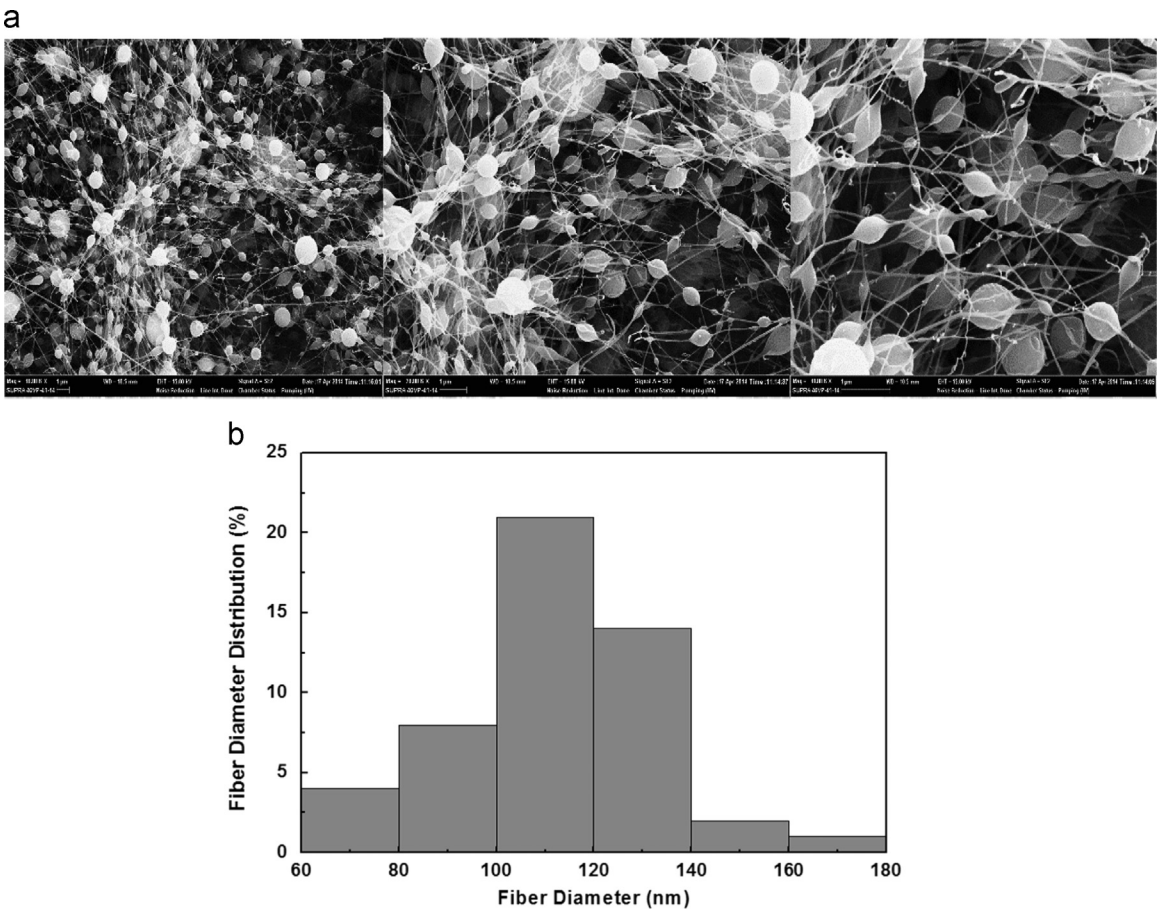

Fig. 1. (a) The SEM images for nano-fibers onto 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer structure. (b) The histogram of the fiber diameter distribution vs the fiber diameter for nano-fibers of 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer structure.

(titration), powder), and gallium nitrate hydrate (crystalline, 99.9% trace metals basis) were also supplied from Sigma-Aldrich, cobalt acetate tetra-hydrate (for analysis EMSURE® ACS) was provided from Merck. Ultrapure deionized water which was produced by Millipore water and acetic acid (100%, Merck) was used as a solvent. Firstly, the PVA solution (10% w/w) with de-ionized water was prepared by dissolving the PVA powder in ultrapure distilled and deionized water and heating it at 80 °C while stirring for 3 h, then it was cooled to the room temperature. Then, the metal acetates and nitrate were solved into the ultrapure water and acetic acid and a solution was produced. Then, PVA (10% w/w) was added into this solution, so the solution which will be used the electro-spinning process was produced. The percent (w/w) of the materials are cobalt (100%), calcium (75%), gallium (2.5%), and polyvinyl alcohol powder (50%). Lastly, the n-Si wafers were pasted upon metal collector and the solution of the PVA/metal compounds was transferred upon the wafers as nano-size during 10 min via electro-spinning, respectively. The distance between the wafer and the syringe (polymer hybrid solution) was adjusted to 15 cm and the voltage of 17 kV was applied to the solution at a flow rate of 0.5 ml/h. Thus, the nano-fibers were placed on the wafers. The electro-spinning system consisted of a direct current (DC) high-voltage power supply (Gamma High Voltage Research, Inc., Ormond Beach, FL, USA; ES 30P-20 W/DAM), a dosing pump (New Era Syringe Pump), a plastic capillary tube (syringe), and a metal collector. The syringe was filled with polymer solutions before the copper pins were connected to the power supply.

The surface morphology of nano-fibers was also examined by SEM (Field Emission SEM ZEISS, SUPRA 40 VP) on samples sputtered with platinum (Qourum Q 150R ES DC Sputter) and observed at an accelerating voltage of 10 kV. Fig. 1(a) shows the SEM images for nano-fibers onto 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer structure at 20,000 magnification (i) and 40,000 magnification (ii). As can be seen in Fig. 1(a), there is a nanosized structure on the n-Si wafer. The beady, bendy, and linear structures are seen in this figure. The viscosity, the conductivity, and the surface tension are effective at these formations.

Fig. 1(b) shows the histogram of the fiber diameter distribution versus the fiber diameter for nano-fibers of 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer structure. It is clear that the diameters of nano-fibers change from 60 nm to 180 nm and the average diameter of nano-fibers is about 112 nm.

After grown of 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer, the high purity of Au dots with 1 mm diameter and at about 1500 Å thickness were deposited on the front of interfacial layer in same metal evaporation system. Thus

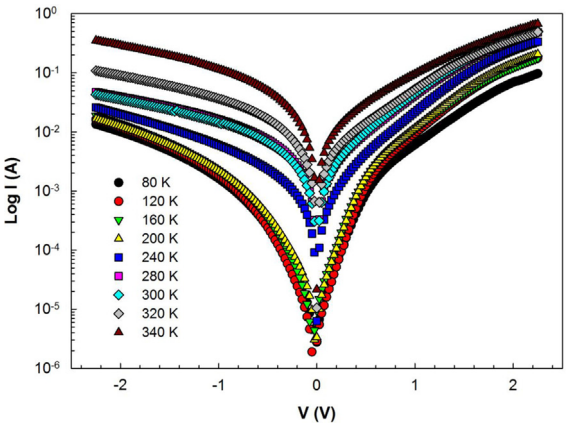

Fig. 2. The semi-logarithmic forward and reverse *I–V* characteristics of Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

the fabrication processes of Au/n-Si SDs with interfacial 2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$) interfacial layer were completed. For the electrical measurements, the samples were placed on the Cu-holder with the help of silver paste and the electrical contacts were also made to the upper electrodes by the use of thin silver coated wires with silver paste. Both the forward and reverse bias *I–V* measurements of these structures were performed at room temperature by using Keithley 2400 source meter.

3. Results and discussions

Fig. 2 shows the semi-logarithmic *I–V* characteristics of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure in the temperature range of 80–340 K. As shown in Fig. 2, the reverse current (I_r) increases as exponentially with increasing voltage and exhibits strong dependence of temperature. Such increase in reverse current with temperature can be attributed the tunneling throw/via the surface and bulk states/traps [3,28–30]. According to Refs. [1,2], these experimental results of the I_r–V_r characteristics of the sample may be well described by the electric field dependence so the effective conduction mechanisms are either Frenkel–Poole emission (FPE) or Schottky emission (SE) [3,28,29]. The total reverse or leakage current of the MS, MIS or MPS structures consist of leakage current from the defective low-barrier regions (patches or pinch-off) as well as of leakage current from the dislocation-free high barrier regions. In addition, there is not any "soft" or slightly non-saturation behavior in this reverse bias region, which may be explained in terms of the image force lowering of the sample [17,23] and the existence of interfacial layer at M/S interface. For a SBD with uniform interface polymer or insulator layer, relation between the applied forward biases ($V \geq 3kT/q$) and current is due to TE theory and it can be expressed as [22,23].

$$I_{TE} = I_o \left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)\right]\left\{1-\exp\left[\frac{q(V-IR_s)}{kT}\right]\right\}+\left(\frac{V-IR_s}{R_{sh}}\right) \quad (1a)$$

where I_o is the reverse saturation current and can be extracted from the straight line intercept of Ln*I* vs *V* plot at zero bias is given by

$$I_o = A^*A\,T^2\exp(-q\Phi_{Bo}/kT) \quad (1b)$$

where the quantities *A*, A^*, *T*, IR_s and Φ_{Bo} are the diode area, the effective Richardson constant and is equal to 112 A/cm^2 K^2 (for *n*-type Si), the absolute temperature in *K*, Boltzmann's constant, voltage drop across R_s of structure and the apparent or zero-bias BH, respectively. This model considers the voltage dependence of the BH by the *n* and the series and parallel resistances (R_s and R_{sh}) of the structure. Firstly, the value of I_o was obtained from the intercept of ln*I* vs *V* plot at $V=0$ for each temperature. Subsequently, I_o determined and using the value of *A*, the value of Φ_{Bo} was obtained from Eq. (1b) for each temperature as

$$\Phi_{Bo} = \frac{kT}{q}\ln\left[\frac{AA^*T^2}{I_o}\right] \quad (1c)$$

The other important diode parameter is the ideality factor and it was obtained from the slope of the Ln *I–V* plot for each temperature in the linear region ($0.075 \ll V \ll 0.425$ V) and can be written using Eq. (1) as

$$n = \frac{q}{kT}\left(\frac{d(V-IR_s)}{d(\ln(I))}\right) \quad (2)$$

The changes in I_o, *n* and Φ_{Bo} values with temperature were tabulated in Table 1 and they were found to be strongly temperature dependent. The experimentally values of I_o, *n* and Φ_{Bo} for the structure range from 7.2×10^{-6} A, 14.5, and 0.141 eV (at 80 K) to 1.7×10^{-3} A, 3.18, and 0.526 eV (at 340 K). Such high value of *n* cannot be explained only the base of particular density distribution of D_{it} and interfacial layer at M/S interface [28]. In the other words, the high value of *n* especially at low temperatures in our samples cannot be also explained the existence of interfacial layer and particular distribution of interface states at metal/semiconductor (M/S) interface. It is clear that the *nT* values seems to remain almost constant between 160 and 340 K and it means that the CCM should be dominated tunneling via traps or FE theory [2,25,26,31]. The increase in *n* with decreasing temperature is known as T_o effect or anomaly in the literature [24–26] and may be originated from D_{it} [12], tunneling [23] and image force lowering [23]. In addition, as can be seen in Fig. 3, the value of *n* was found to change linearly with the inverse

Table 1
The values of various electrical parameters for the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure in the temperature range of 80–340 K.

T (K)	I_o (A)	*n*	Φ_{Bo} (eV)	$\Phi_{Bef.}$ (eV)	*nT* (K)
80	7.2×10^{-6}	14.50	0.141	1.149	1160
120	1.5×10^{-5}	9.00	0.213	1.077	1080
160	3.1×10^{-5}	6.63	0.282	1.044	1060
200	6.6×10^{-5}	5.30	0.347	1.015	1061
240	1.7×10^{-4}	4.42	0.404	0.961	1061
280	2.9×10^{-4}	3.79	0.466	0.941	1061
300	5.3×10^{-4}	3.54	0.487	0.899	1061
320	1.1×10^{-3}	3.31	0.503	0.842	1061
340	1.7×10^{-3}	3.18	0.526	0.833	1081

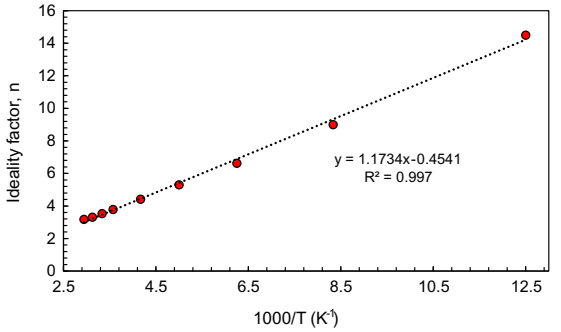

Fig. 3. The plot of n vs 1000/T of Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

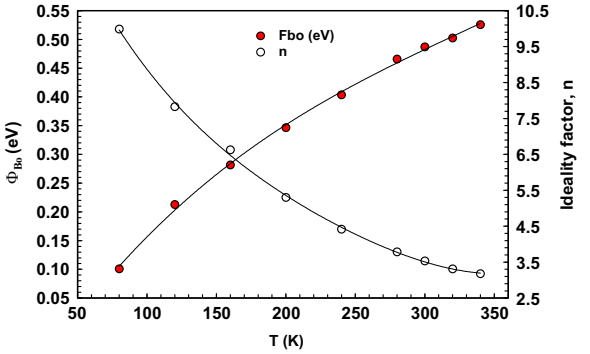

Fig. 4. The Φ_{Bo} and n of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure obtained from the forward bias I–V data at various temperatures.

temperature as

$$n(T) = \alpha + \beta/T \equiv n_o + T_o/T \tag{3}$$

where α and β which are equal to n_o and T_o are constant which were found to be 0.454 and 1173 K from the intercept and slope of $n(T)$ vs $1/T$ plot, respectively.

The values of Φ_{Bo} obtained from the forward bias I–V plots in the linear region have also shown an unusual behavior such that it increases with increasing temperature. Such behavior of Φ_{Bo} and n with temperature were shown a deviation from pure TE in the whole temperature range. As can be seen in Table 1 and Fig. 4 both Φ_{Bo} and n values strongly dependent on temperature especially at low temperature. While Φ_{Bo} increases, n decreases with increasing temperature. It is clear that there is a positive temperature coefficient in Φ_{Bo} that is in contrast to the negative temperature dependence measurements by Crowell and Rideout [32] in Si based SBDs and Mead and Spitzer [33] in InAs, which closely follows the charge in the band gap of Si with temperature [22,23].

As can be seen, in Table 1, T product by n (nT) is almost constant due to the same slope of Ln I vs V plots. Therefore, FE and TFE mechanisms may be effective in the whole temperature range (80–340 K). On the other hand, the TFE mechanism requires the characteristic tunneling energy (E_{oo}) should be close thermal energy (kT/q) and in the FE mechanism E_{oo} must be very larger than thermal energy. According to tunneling mechanisms, the tunneling ideality

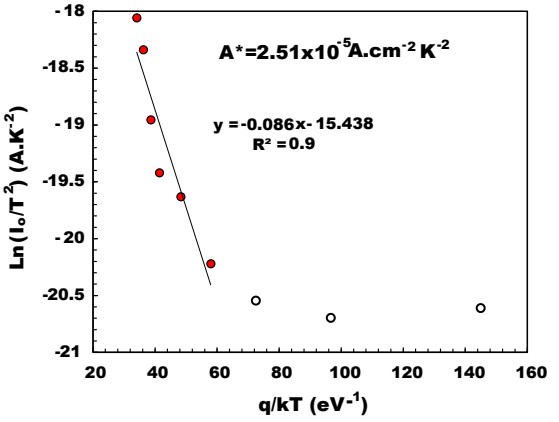

Fig. 5. The Ln(I_o/T^2) vs q/kT plot of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

factor n_{tun} can be expressed as [24–26]:

$$n_{tun} = \frac{E_{oo}}{kT}\coth\left(\frac{E_{oo}}{kT}\right) = \frac{E_o}{kT} \tag{4.a}$$

with

$$E_{oo} = \frac{h}{4\pi}\left(\frac{N_D}{m_e^*\varepsilon_s}\right)^{1/2} \tag{4.b}$$

where $m_e^* = 0.98\ m_o$ is effective mass of electrons and ε_s is the permittivity of Si (=11.8), N_D is the concentration of donor atoms ($=8.6\times10^{17}$ cm^{-3} from the manufacturer) and the other symbol are of usual meaning [22]. The value of E_{oo} was obtained from Eq. (4.b) as 5.06 meV at room temperature and this value is lower than kT/q (25 meV). The theoretical value of E_{oo} confirmed that tunneling mechanisms are not dominating in the whole temperature range.

Thus, in light of the above explanations, in the in the expression of I_o should be including both the probably tunneling factor ($\chi^{0.5}\delta$) and values following relation as [1,34,35]. Thus, the expression for the reverse saturation current can be written as

$$I_o = AA^*\exp\left(-\alpha\chi^{1/2}\delta\right)\exp\left(-\frac{q\Phi_{Bef}}{n(T)kT}\right) \tag{5a}$$

Here, $n(T)$ is temperature dependent ideality factor, $\Phi_{Bef.}$ is the effective barrier height, δ is the thickness of the interfacial layer in which electrons move through tunnel, $\alpha = (4\pi/h)(2m_e^*)^{0.5}$ is a constant that depends on the tunneling effective mass of electron and Planck's constant, and χ is the mean tunneling barrier presented by the δ. The value of ($\chi^{0.5}\delta$) was found to be as 9 from the linear part of Ln(I_o/T^2) vs q/kT plot. Thus, the modified value of BH ($=\Phi_{Bef.}$) can be expressed as [1,34]

$$\Phi_{Bef} = n(T)\left[\frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right) - (kT/q)\cdot(-\alpha\chi^{0.5}\delta)\right]$$
$$= n(T)\cdot[\Phi_{Bo} - (kT/q)(\alpha\chi^{0.5}\delta)] \tag{5b}$$

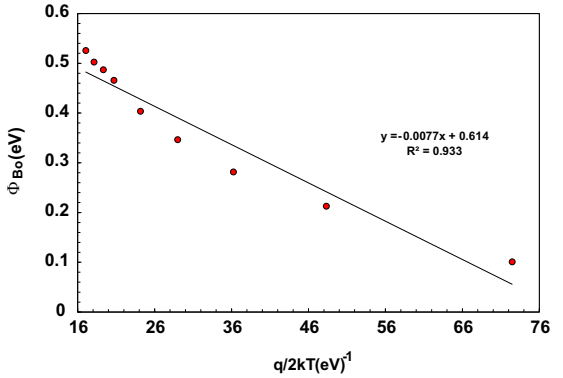

Fig. 6. The Φ_{Bo} vs $q/2kT$ plot of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

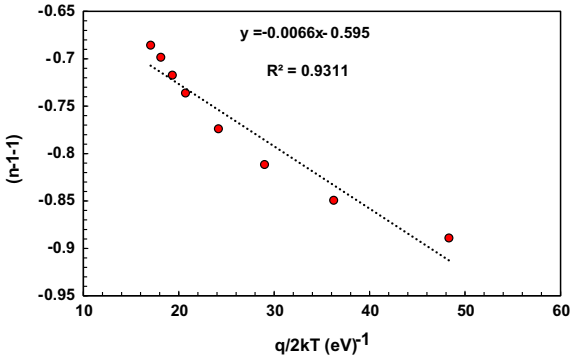

Fig. 7. The $(n^{-1}-1)$ vs $q/2kT$ plot of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

After this modification, as can be seen in Table 1, the modified value of Φ_{Bef}. decreases almost linearly with the temperature as

$$\Phi_{Bef} = \Phi_B(0\ K) + \alpha\, T \tag{6}$$

Here, Φ_{Bo} (0 K) is the BH at zero temperature and α is the negative temperature coefficient of the BH and they are found as 1.23 eV and -11.5×10^{-4} eV K^{-1} respectively. It is clear that this value of α for Φ_{Bef}. is closer to the value of α (-4.73×10^{-4} eV K^{-1}) for forbidden band gap of Si.

In order to evaluation of the BH, one may also make use of the conventional Richardson plot/ activation energy plot ($Ln(I_o/T^2)$ vs q/kT). $Ln(I_o/T^2)$ vs q/kT plot of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure was shown in Fig. 5. As shown in Fig. 5, Richardson plot shows a linear behavior in the temperature range of 200–340 K, but it deviated from linearity at low temperatures (80–160 K). The E_a and A^* values were found from the slope and intercept of this plot as 0.086 eV and 2.5 times; 10^{-5} A cm^{-2} K^{-2}, respectively. This experimental value of A^* is quite small compared to their theoretical value of n-Si (A^*=112 A/cm^2 K^2). In addition, the obtained value of E_a is also very low of forbidden band gap of Si. These results confirmed that the deviation in Richardson plots may be due to the spatial inhomogeneous BHs and potential fluctuations at the interface that consists of low and high barriers or patches [12–18]. On the other hand, Horvath et al. [36] explained the low value A^* may be affected by lateral inhomogeneity of the BH at M/S interface.

The decrease in Φ_{Bo} and increase in n with decreasing temperature can be also explained by the lateral distribution of BH and it has a GD of the BH values at around mean value BH ($\overline{\Phi}_{Bo}$) with standard deviation (σ_{so}). According to single GD theory, the measured or apparent BH (Φ_{ap}) and the ideality factor ($n=n_{ap}$) with temperature can be expressed by the following relations [14–18]:

$$\Phi_{ap} = \overline{\Phi}_{Bo}(0\ K) - \frac{q\sigma_{so}^2}{2kT} \tag{7}$$

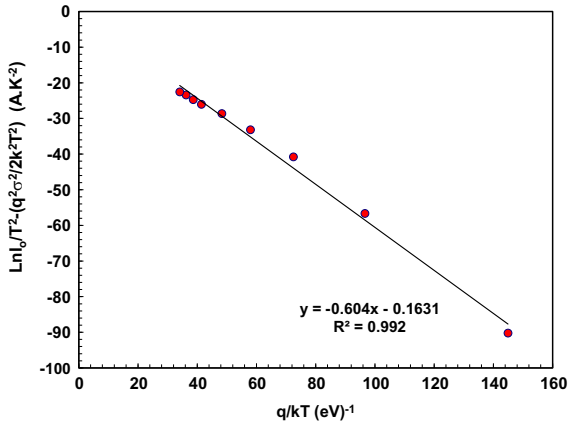

Fig. 8. The $Ln(I_o/T^2)-(q^2\sigma_s^2/2k^2T^2)$ vs q/kT plot of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure.

$$\frac{1}{n_{ap}(T)} - 1 = -\rho_1(T) = -\rho_2 - \frac{q\rho_3}{2kT} \tag{8}$$

where ρ_1, ρ_2 and ρ_3 are the voltage deformation coefficients. $\overline{\Phi}_{Bo}$, σ_{so} and voltage coefficients. Both the Φ_{Bo} vs q/kT and $(n^{-1}-1)$ vs $q/2kT$ plots are shown in Figs. 6 and 7, respectively. $\overline{\Phi}_{Bo}$ and σ_{so}^2 values were found from the intercept and slope of the Fig. 6 as 0.614 eV and 0.088 V, respectively. This low value of σ_{so} shows that the existence of a homogeneous distribution of BHs or patches at around $\overline{\Phi}_{Bo}$. As can be seen in Table 1, the value of Φ_{Bo} from the forward bias I–V data is always smaller than the average of the BH for each temperatures. In addition, $(n^{-1}-1)$ vs $q/2kT$ was also shown in Fig. 7 and the voltage deformation coefficients ρ_2 and ρ_3 values were obtained from the intercept and slope of the this plot as 0.595 and 0.0066 V, respectively.

Thus, the Richardson plot was modified using following relation (Eq. 9) and it was given in Fig. 8

$$Ln\left(\frac{I_o}{T^2}\right) - \left(\frac{q^2\sigma_{so}^2}{2k^2T^2}\right) = Ln(AA^*) - \frac{q\overline{\Phi}_{Bo}}{kT} \tag{9}$$

$\overline{\Phi}_{Bo}$ and A^* values were obtained from the slope and intercept of the modified Richardson plot as 0.604 eV

and 108.23 A cm^{-2} K^{-2} respectively. This obtained experimental value of A^* is in close agreement with the theoretical value of n-Si (112 A cm^{-2} K^{-2}). Analysis of the forward bias *I–V–T* characteristics of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure can be explained with GD of BHs.

4. Conclusions

The current conduction mechanisms in the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure have been investigated in the temperature range of 80–340 K using the forward bias current–voltage (*I–V*) characteristics. Experimental results show that the main electrical parameters such as n, I_o, and Φ_{Bo} values were found a strong function of temperature and they were found as 14.5, 7.2×10^{-6} A, 0.141 eV at 80 K and 3.18, 1.7×10^{-3} A, and 0.526 eV at 340 K, respectively. While the value of n increases with decreasing temperature, Φ_{Bo} decreases. In order to interpret such behavior of Φ_{Bo} and n, both the Φ_{Bo} vs $q/2kT$, Φ_{Bo} vs n, and $(n^{-1}-1)$ vs $q/2kT$ plots were drawn to obtain an evidence of a Gaussian distribution (GD) of the BHs and they show a linear behavior. Thus, the $\overline{\Phi}_{bo}$ and σ_s values were found from the slope and intercept of this plot as 0.614 eV and 0.088 V, respectively. Consequently, the $\overline{\Phi}_{Bo}$ and A^* values were obtained from the slope and intercept of the modified Richardson plot as 0.604 eV and 108.23 A cm^{-2} K^{-2} respectively. This obtained experimental value of A^* is in close agreement with the theoretical value of n-Si (112 A cm^{-2} K^{-2}). It has been concluded that the analysis of the forward bias *I–V–T* characteristics of the Au/2% GC-doped ($Ca_3Co_4Ga_{0.001}O_x$)/n-Si structure can be successfully explained with GD of BHs.

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