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Characteristics of an oxidation-induced inversion layer in compensated p-type crystalline silicon

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Abstract
We report on the formation of a lightly doped p–n junction at the surface of compensated p-type silicon wafers, caused by dopant segregation during thermal oxidation. Experimental evidence and characterization of the junction is obtained by secondary ion mass spectrometry and hot probe measurements. For the first time the impact of the unexpected junction on the characterization of metal-oxide-semiconductor structures with capacitance–voltage measurements is measured and explained via simulation.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The photovoltaic industry is rapidly moving towards silicon purification processes that are less energy intensive such as upgraded metallurgical grade silicon. The material produced by such techniques is cheaper and has a lower embodied energy than conventional silicon materials. Nevertheless, they tend to be less pure (containing more metallic impurities) and compensated (containing both boron and phosphorus). Therefore, the properties of compensated silicon wafers, and their behaviour during device fabrication, are of considerable interest. An important characterization tool is the measurement of the capacitance–voltage (CV) characteristics of metal insulator semiconductor (MIS) structures constructed on the silicon. This allows important properties of the insulator semiconductor interface to be derived. However, when attempting to apply CV methods to characterize thermally grown SiO_2 on compensated Si, an unexpected problem arises. In this work we demonstrate that thermal oxidation of compensated p-type silicon wafers can lead to the creation of an unwanted n-type layer at the surfaces, caused by dopant segregation during the oxide growth. We also show how this parasitic n-layer can interfere with device performance and material characterization.

Dopant redistribution during oxide growth is affected by several mechanisms: diffusion in Si, diffusion in SiO_2 and segregation at the Si/SiO_2 interface. The equilibrium segregation coefficient m is expressed as the ratio of the concentration of impurity in the silicon over the concentration of impurity in the oxide at equilibrium, $m = C_{\text{silicon}}/C_{\text{oxide}}$. The equilibrium segregation coefficient of boron at the Si/SiO_2 interface is approximately $m_{\text{boron}} = 0.3$ [1], meaning that the oxide accepts boron. On the other hand the segregation coefficient of phosphorus at the Si/SiO_2 interface is approximately $m_{\text{phosphorus}} = 10$ [1], meaning that the oxide rejects phosphorus. As a result of their different segregation properties, boron tends to become depleted from the silicon during oxide growth, while phosphorus tends to pile up just below the surface. In non-compensated p-type material this effect leads to a depletion of boron in the Si near the interface. But in compensated p-type material, it also leads to an accumulation of phosphorous. After sufficient time the effect may be so great that the dominant species near the interface is no longer boron, but phosphorus. The semiconductor has thus changed from p- to n-type near the interface. It should be noted that this inversion of conductivity type can only occur in p-type compensated silicon. In n-type compensated silicon the depletion of boron and accumulation of phosphorus will only increase the concentration of n-type dopants. Phosphorous,

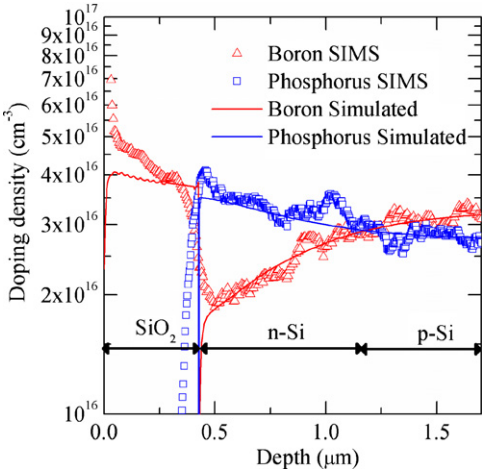

Figure 1. Measured (SIMS) and simulated dopant profiles after a 1 h 1100 °C wet oxidation in a strongly compensated p-type sample ($N_A = 3.25 \times 10^{16}$ cm^{-3}, $N_D = 2.75 \times 10^{16}$ cm^{-3}).

antimony or arsenic doped samples will act in a similar way as their segregation coefficients are very similar [1].

2. Experimental method

The samples used in this study were the cleaved sections of 155 × 155 mm pseudo square, p-type, ⟨1 0 0⟩-oriented Czochralski-grown silicon wafers. There were wafers from two control ingots (non-compensated), which were boron doped and had resistivities of 1.20 ± 0.08 Ω cm and 0.40 ± 0.08 Ω cm, and also two compensated ingots, doped with both boron and phosphorus, with resistivities of 1.6 ± 0.1 Ω cm and 0.50 ± 0.08 Ω cm. More details of these samples have been published elsewhere [2]. After surface etching and cleaning, samples for secondary ion mass spectrometry (SIMS) measurements were thermally oxidized at 1100 °C for 1 h in steam (wet oxidation). In addition, a simulation of the oxidation and dopant redistribution processes during this thermal step was made using the 2D process simulator silvaco-ATHENA [3]. The impact of the unwanted junction on capacitance–voltage (CV) measurements was then demonstrated by high frequency (1 MHz) CV measurements on metal oxide semiconductor structures (MOS) with a mercury probe (775 μm diameter Hg dots). Four control and four compensated samples were fabricated. These wafers had been first submitted to a wet oxidation at 1050 °C for 15 min, 30 min, 1 h and 2 h. The charge density within the device was simulated using silvaco-ATLAS [4]. In addition, hot probe measurements were made after etching of the oxide.

3. Results and discussion

To experimentally demonstrate the formation of the junction, a SIMS dopant profile was performed. Figure 1 presents the SIMS profile within the first 1.7 μm of both boron and phosphorus in the strongly compensated (1.6 Ω cm) sample after a 1 h wet oxidation at 1100 °C. This sample was expected to have dopant concentrations of around $N_A = 4 \times 10^{16}$ cm^{-3} and $N_D = 3 \times 10^{16}$ cm^{-3}, based on previous studies [2]. The secondary ion intensity dropped after ∼0.4 μm showing that the oxidation grew a 0.4 μm thick oxide. The figure shows that this oxide caused a large change in dopant concentration near the interface. Deep in the material the doping density is constant with $N_A > N_D$, making it p-type. Closer to the Si/SiO$_2$ interface the concentration of boron decreases while the concentration of phosphorus increases. At 0.8 μm from the interface, the semiconductor becomes perfectly compensated ($N_A = N_D$), and then switches to n-type ($N_D > N_A$). In this sample an n-layer of approximately 0.7 μm depth and with a peak net doping density of 2×10^{16} cm^{-3} has formed after oxidation.

Table 1. Accumulation capacitance C_{acc} (pF) and corresponding oxide thickness t_{ox} (μm) for different oxidation time.

	Control		Compensated	
Oxidation time	C_{acc} (pF)	t_{ox} (μm)	C_{acc} (pF)	t_{ox} (μm)
15 min	85	0.24	86	0.24
30 min	58	0.36	59	0.35
1 h	40	0.52	40	0.52
2 h	28	0.74	28	0.74

To further study the formation of the junction, a numerical simulation of the process was made using the 2D process simulator silvaco-ATHENA [3]. Figure 1 plots the results from a 1 h 1100 °C wet oxidation in a strongly compensated p-type sample with an acceptor concentration of $N_A = 3.25 \times 10^{16}$ cm^{-3} and a donor concentration of $N_D = 2.75 \times 10^{16}$ cm^{-3}. These dopant concentrations were chosen based on the SIMS measurements deep in the wafer, and vary only slightly from those reported previously for similar wafers ($N_A = 4 \times 10^{16}$ cm^{-3}, $N_D = 3 \times 10^{16}$ cm^{-3}) [2]. The simulated dopant distributions in the silicon and the junction depth after oxidation are in good agreement with the SIMS data.

Simulation shows that several parameters can be adjusted to reduce the junction depth and doping density, such as reducing the oxidation temperature and time, and using dry oxidation. At a constant net doping density ($N_A - N_D$), simulations indicate that as N_A and N_D increase, the junction becomes deeper and more heavily doped.

Following the experimental demonstration of the junction formation, its influence on characterization techniques was studied. High frequency (1 MHz) CV measurements were conducted on MOS fabricated on four control and four compensated samples. Table 1 shows that the accumulation capacitances C_{acc} are similar in the compensated and control wafers, indicating that the oxide thicknesses were similar for each oxidation time. The oxide thickness t_{ox} was calculated using the capacitance in accumulation ($t_{ox} = \varepsilon_{ox} \times A/C_{acc}$).

Figure 2 plots the measured CV curves, showing qualitatively different curves for (*a*) the control and (*b*) the compensated samples. In contrast to the control samples, the CV curves of the compensated samples have a distinct minimum and are increasingly shifted to more negative voltages. Such minimums have been found to occur when

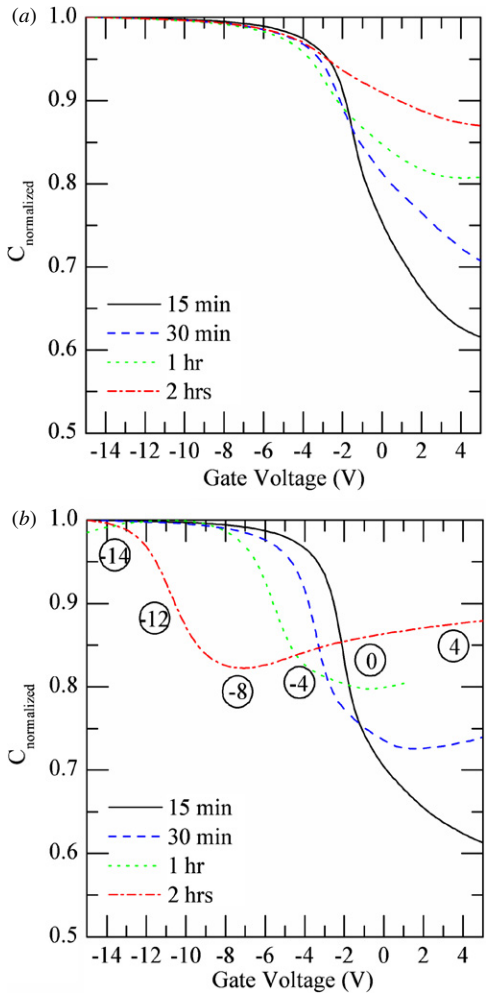

Figure 2. Measured normalized high frequency capacitance–voltage curves on metal oxide semiconductor devices after different oxidation times (15 min, 30 min, 1 h, 2 h): (*a*) CV curves for a 1.2 Ω cm non-compensated bulk ($N_A = 1.7 \times 10^{16}$ cm^{-3}), (*b*) CV curves for a 1.6 Ω cm compensated bulk ($N_A = 4 \times 10^{16}$ cm^{-3}, $N_D = 3 \times 10^{16}$ cm^{-3}).

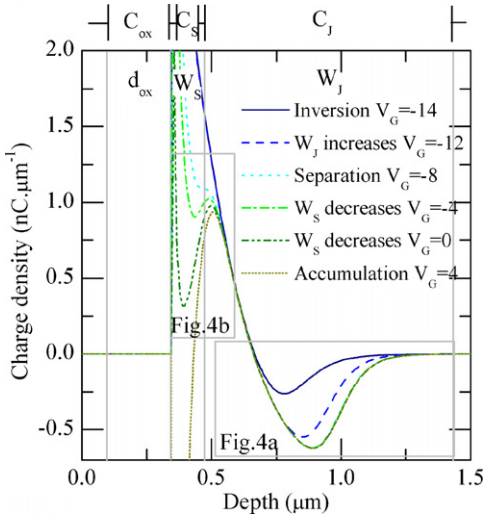

Figure 3. Simulated charge density in the device for different applied gate voltage, the oxide (d_{ox}), the surface depletion (W_S) and junction depletion (W_J) regions lead to the oxide capacitance (C_{ox}), surface capacitance (C_S) and the junction capacitance (C_J) represented at the top; the different gate voltages (1–6) represent the different sections of the CV curve, numbered in figure 2(*b*).

the entire surface of the semiconductor was inverted either by charge in the oxide near the p-type silicon [5], or by an implanted layer under the oxide [6]. Since these minimums do not occur in our control samples, any charge in the oxide is negligible in terms of inducing an inversion layer below the surface, and so should not affect the compensated samples either.

Sigmond *et al* [6] have examined the case of a p-type implanted layer between an n-type bulk and an oxide. In their study a model with an oxide capacitance in series with one surface and one junction depletion capacitance was used. In our case the situation is similar. To analyse precisely the junction coupled with the MOS, the dopant profiles obtained using the process simulator silvaco-ATHENA [3] were entered into the semiconductor characterization simulator silvaco-ATLAS [4]. In the simulation, a voltage ramp was then applied to the gate (−15–5 V) at high frequency (1 MHz). The simulated curves are less stretched out than the experimental ones. This is due to the simplification in the modelling with zero density of interface states, and means that experimental and simulated gate voltages differ. For simplification purposes the values of experimental voltages corresponding to the accumulation minimum and inversion are used in the explanation of the simulation. There is a clear qualitative agreement between the simulated and experimental curves with the characteristic minimum being present in both simulated and experimental CV curves. The simulation allowed for the extraction of the potential, electric field and charge density in the device for different gate voltage (figures 3 and 4).

Due to the presence of the n-layer in compensated samples, inversion for a control p-type sample becomes accumulation for a compensated p-type sample. For the following analysis the terms inversion, depletion and accumulation will refer to the voltage-induced charged density in the n-layer and not the p-type bulk. This means that positive gate voltage induces accumulation (of electrons) and negative voltage induces inversion (appearance of holes at the surface). Large negative gate voltage not only attracts holes to the surface but also repels electrons on the p-side of the junction (figures 3 and 4(*a*), $V_G = -14$ V). Variations in the gate voltage exclusively induce changes in the charge density of the inversion layer. Hence the surface-junction depletion region (W_{S+J}) neither expands nor shrinks. The total capacitance is therefore constant (figure 2(*b*), $V_G = -14$ V). As the gate voltage increases, the inversion layer disappears and electrons starts to flow back to the p-side of the p–n junction (figure 3, $V_G = -14$ V to -8 V). This results in an increase of the surface-junction depletion region (figure 4(*a*), $V_G = -14$ V to -8 V). Consequently the total capacitance decreases as seen in figure 2(*b*). ($V_G = -14$ V to -8 V). The depletion region increases with increasing gate voltage till the surface depletion region (W_S) separates itself from the junction depletion region

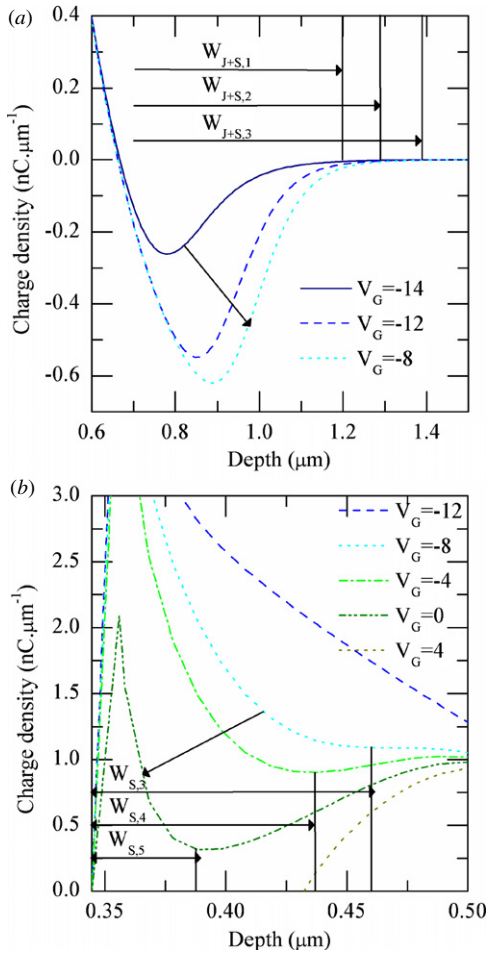

Figure 4. Simulated charge density profile in the p-side of the junction (*a*) and in the n-side of the junction near the silicon/oxide interface (*b*). The increase of the junction depletion width W_{S+J} with increasing gate voltage is evident in (*a*), and the decrease of the surface depletion width W_S with increasing gate voltage is shown in (*b*).

(W_J) (figures 3 and 4(*b*), $V_G = -8$ V). After this point of separation, the surface becomes less and less depleted with increasing voltage and thus the surface depletion shrinks (figure 4(*b*), $V_G = -8$–0 V). This in turn leads to an increase of the total capacitance as seen in figure 2(*b*) ($V_G = -8$–0 V). Further increase in the gate voltage results in an accumulation of electron at the surface (figure 4(*b*), $V_G = 4$ V). The junction depletion does not vary much with gate voltage leading to the stabilization of the total capacitance seen in figure 2(*b*), ($V_G = 4$ V).

It is interesting to note that for longer oxidation times, thus more heavily doped n-layers, the point of separation occurs at larger negative voltage (figure 2(*b*)). For more heavily doped n-regions the junction and surface depletion regions are smaller. Not only are these depletion regions more distant from each other, but also the surface depletion region expands more slowly with negatively increasing gate voltage. Therefore, larger negative gate voltages are required for the surface depletion region to reach the junction depletion region.

Table 2. Surface polarity after oxidation of p-type samples after oxidation using the hot probe method compared with the ideality of the CV curve obtained.

ρ (Ωcm)	R_C	Surface polarity after oxidation	Ideality of CV curve
		Uncompensated	
0.4	1	P	Ideal
1.2	1	p	Ideal
		Compensated	
0.5	3.5	Not detectable	Non-ideal
1.6	7	n	Non-ideal

At similar resistivity, samples that have a higher compensation ratio will have a higher n-layer doping. By looking at the shift of the CV curve one can deduce which sample has a higher compensation ratio. This cannot be done by traditional methods such as four point probe where compensated samples with similar resistivities cannot be discriminated. Nevertheless, the fact that the main region affected by the applied gate voltage is the n-region implies that no quantitative data concerning the net doping of the bulk can be obtained using CV on thermally oxidized compensated samples. The fact that the junction induces a shift of the CV curve also makes it difficult to extract information about the density of interface states using the CV method.

Finally, a relatively quick and easy way to detect the presence of an oxide-induced junction is to measure the conductivity type of the sample's surface by removing the oxide and using the hot probe method [7]. In this measurement, one hot probe and one cold probe are contacted with the sample. The thermal gradient generates a majority carrier current in the semiconductor, and depending on whether the semiconductor is n-type or p-type, the current will be negative or positive.

Table 2 shows the results of the hot probe method on our wafers after a 1 h 1100 °C wet oxidation step (the compensation ratio is defined as $R_C = (N_A + N_D)/(N_A - N_D)$). While the surface of the non-compensated samples ($R_C = 1$) remains p-type after oxidation, the surface changes to n-type for the highly compensated sample ($R_C = 7$). Due to a lower compensation ratio ($R_C = 3.5$), and therefore insufficient surface inversion, the less compensated sample shows no detectable current. The hot probe method is thus useful to quickly determine whether a relatively heavy inversion layer has been formed. Combined with an oxidation the hot probe method can be used to identify strongly compensated samples.

4. Conclusion

In conclusion, SIMS, hot probe measurements and numerical simulations, are in agreement and reveal the formation of a surface n-type layer after thermal oxidation in highly compensated p-type silicon. This n-layer interferes with characterization techniques that require a thermal oxidation such as CV measurements on MOS structures. In a high

frequency CV curve the surface n-layer introduces a dip in the CV curve that is due to the separation of the junction and surface depletion regions. This prevents the determination of the bulk doping density or the density of interface defects from such CV measurements. It is thus preferable to use electrochemical CV to obtain bulk doping densities, since the requirement for an oxidation is avoided. Nevertheless, the CV curve on MOS structures cannot only be used to determine whether a sample is compensated or not but also to discriminate two compensated samples with similar resistivity but different compensation ratios. This oxidation-induced n-layer could also create significant problems in compensated silicon solar cells involving thermal oxidation. Due to the segregation mechanisms involved, this inversion layer can only occur when $N_A > N_D$ (p-type material). It is also more likely to occur in heavily doped and highly compensated material. The low doping of the resulting n-layer on our samples means that it is unlikely to be useful as an emitter in a solar cell device. Nevertheless, it could potentially act as a non-contacted floating junction, repelling minority carriers from the surface, and thus decreasing surface recombination. More generally, this effect could have potential applications in devices requiring a low-doped diffused layer (n-) with an oxide on top, such as CCDs or buried-channel MOSFETs, the simple oxidation process potentially making phosphorus implantation unnecessary.

Acknowledgments

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