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Microelectronic Engineering 85 (2008) 646–653
MICROELECTRONIC ENGINEERING
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Analysis of interface states and series resistance of Ag/SiO_2/n-Si MIS Schottky diode using current–voltage and impedance spectroscopy methods

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Received 4 September 2007; received in revised form 31 October 2007; accepted 30 November 2007
Available online 8 December 2007

Abstract

The electrical characteristics and interface state density properties of Ag/SiO_2/n-Si metal–insulator–semiconductor diode have been analyzed by current–voltage and impedance spectroscopy techniques. The electronic parameters such as barrier height, ideality factor and average series resistance were determined and were found to be 0.62 eV, 1.91 and 975.8 Ω, respectively. The calculated ideality factor shows that Ag/SiO_2/n-Si structure obeys a metal–interfacial layer–semiconductor configuration rather than ideal Schottky barrier diode. The interface state density of the diode is of order of $\sim 10^{11}$ eV^{-1} cm^{-2}. The dielectrical relaxation mechanism of the diode is analyzed by Cole–Cole plots, indicating the presence of single relaxation mechanism. It is evaluated that the interfacial oxide layer modifies electrical parameters such as interface state density, series resistance and barrier height of Ag/SiO_2/n-Si diode.

Keywords: Metal–insulator–semiconductor diode; Interfacial state density; AC conductance

1. Introduction

The semiconductor devices of metal–semiconductor (MS) and metal–insulator–semiconductor (MIS) types technology have been still investigated and have attracted much attention during recent years [1–3]. MISs play a crucial role in constructing some useful devices in electronic technology. The interface quality between metal and semiconductor affects the performance and reliability of a Schottky diode. A MIS structure is the also most useful device in the study of semiconductor surfaces. Since the reliability and stability of all semiconductor devices are intimately related to their surface conditions, an understanding of the surface physics with the help of MIS diodes is of great importance to device operations [4–7]. Unless specially fabricated, a Schottky barrier diode possesses a native oxide layer between metal and semiconductor. The existence of such an insulating layer converts metal–semiconductor (MS) devices into metal–insulator–semiconductor (MIS) diodes and can have a strong influence on the diode characteristics as well as the interface states and series resistance [8–13] and can modify the electrical properties of MIS structure. The insulator layer between metal and semiconductor, interface state (D_{it}), series resistance (R_s) parameters cause the electrical characteristics of MIS Schottky diodes to be non-ideal [14–18]. Therefore, the frequency-dependent electrical characteristics are very significant to get accurate and reliable results about fabricated semiconductor devices. Recently, the capacitance and conductance measurements for semiconductor investigation have been used to obtain valuable information about the parameters of interface states [14,19,16,20].

This work is an attempt to investigate the detailed electrical transport properties of Ag/SiO_2/n-Si diode with an interfacial oxide layer using forward bias *I–V* characteristics and impedance spectroscopy measurements. Here, we show

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doi:10.1016/j.mee.2007.11.011

some evidence of non-ideal behavior of the $Ag/SiO_2/n$-Si due to the oxide layer, series resistance and interface states, modifying the electrical characteristics of the diode.

2. Experimental details

n-Type silicon with a doping concentration of 0.5–1.5×10^{15} cm^{-3} substrate used in this study is n-Si(1 0 0) with resistivity of 5–10 Ω cm. In order to remove the native oxide on surface on n-Si, the substrate was etched by HF and then was rinsed in deionised water using an ultrasonic bath for 10–15 min and finally was chemically cleaned according to method based on successive baths of methanol and acetone. Then, substrate was immediately placed in vacuum system for the processes [21]. High purity (99.999%) Al with a thickness of 500 nm was thermally evaporated from the tungsten filament onto the whole backside of the substrate at pressure of 3.3×10^{-6} mbar in vacuum pump system and ohmic contact was prepared by sintering evaporated Al at 450 °C for 15 min. Schottky contact was formed by vacuum thermal evaporation of Ag at pressure of approximately 3.3×10^{-6} mbar. The thickness of the metal was determined to be 1 μm. The current–voltage (I–V) measurements were performed by a 2400 KEITHLEY sourcemeter and GPIB data transfer card for current–voltage measurements are used and data are recorded by an interface. The impedance spectroscopy measurements were performed by use of HP 4194A impedance/Gain-phase analyzer.

3. Results and discussion

Fig. 1 shows the forward and reserve bias current–voltage characteristics of the $Ag/SiO_2/n$-Si diode. The current–voltage characteristics of a metal–insulator–semiconductor (MIS) diode can be analyzed by the following relation [1,2],

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(-\frac{q(V - IR_s)}{kT}\right)\right] \quad (1)$$

where q is the electronic charge, n is the ideality factor, R_s is the series resistance, k is the Boltzmann constant and I_o is the saturation current defined by [1,2]

$$I_0 = AA^*T^2 \exp\left(-\alpha\chi^{0.5}\delta\right) \exp\left(-\frac{q\phi_{b0}}{kT}\right) \quad (2)$$

where A is the contact area, A^* is the Richardson constant and equals to 112 A/cm^2 K^2, T is the temperature and φ_{b0} is the zero barrier height, $\exp(-\alpha\chi^{0.5}\delta)$ is transmission coefficient across the thin interfacial layer, $\alpha = (4\pi/h)(2m^*)^{1/2}$ is a constant, h is the Planck constant, m^* is the effective mass of the electrons ($0.98m_0$), δ is the thickness of the interfacial layer, χ is the effective tunneling barrier of the oxide layer. The ideality factor of the diode can be calculated by the following relation:

$$n = \frac{q}{kT}\frac{d\ln(V - IR_s)}{d\ln I} \quad (3)$$

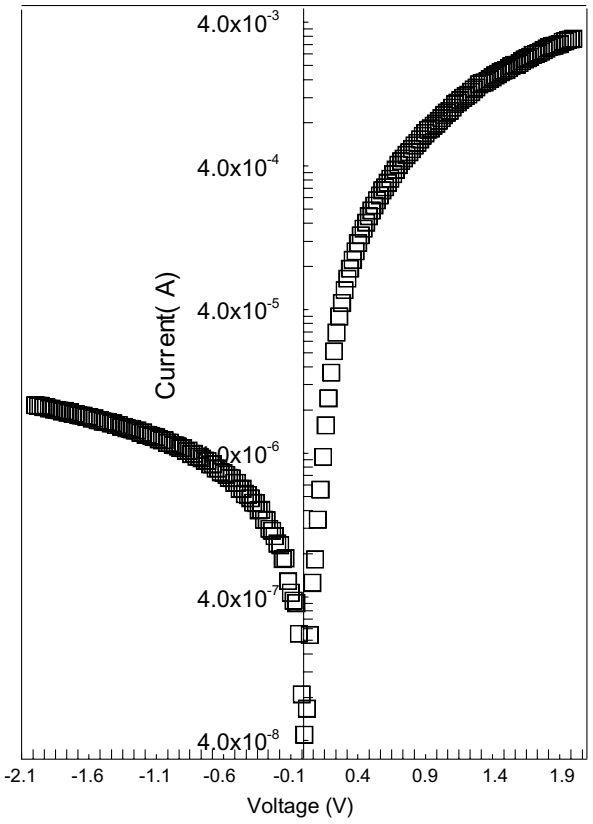

Fig. 1. The forward and reserve bias current vs. voltage characteristics of the $Ag/SiO_2/n$-Si diode.

The n and φ_b were calculated from slope and intercept of the Fig. 1 and were found to be 1.65 and 0.73 eV, respectively. The obtained ideality factor shows that Ag/n-Si structure obeys a metal–interfacial layer–semiconductor configuration rather than ideal Schottky barrier diode. Fig. 2 shows schematically the presence of surface and interface states in a MIS device [22]. At higher biases, the non-linearity of I–V characteristic of the diode indicates a continuum of interface states, in which interface states are at equilibrium with the semiconductor. Nevertheless,

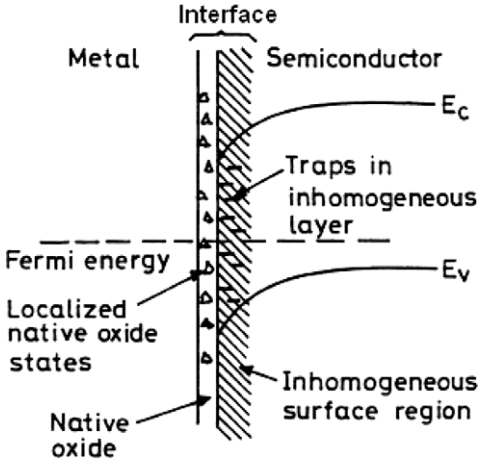

Fig. 2. Surface and interface states in a MIS device [22].

$Ag/SiO_2/n$-Si diode exhibits good rectifying behavior with a relatively low leakage current density. There are several effects, which cause deviations of the ideal behavior and must be taken into account. These effects can be interface states and series resistance and these are important parameters for the diode performance. These parameters cause a downward curvature in the I–V characteristics at higher forward bias values. In such a case, Cheung's method can be used to obtain the barrier height, ideality factor and series resistance. Cheung's functions are expressed by [23]

$$\frac{dV}{d\ln I} = n\frac{kT}{q} + IR_s \tag{4}$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) \tag{5}$$

where $H(I)$ is written as

$$H(I) = n\phi_B + IR_s \tag{6}$$

In order to obtain φ_b and R_s values, the plots of $dV/d\ln I$ and $H(I)$ vs. I were plotted (Fig. 3a and b). The n and R_s values were determined from Fig. 3a and were found to be 1.91 and 974.6 Ω, respectively. Using obtained value of n, the barrier height and series resistance values were calculated from the plot of $H(I)$ vs. I. The obtained φ_b and R_s values are 0.62 eV and 977 Ω, respectively. The difference in the values of ideality factor and barrier height obtained from the $dV/d\ln I$–I and $H(I)$–I plots is due to the presence of series resistance, interfacial layer and existence of interface states. The interfacial layer causes a voltage drop across the interface. The ideality factor (1.91) of the $Ag/SiO_2/n$-Si studied is lower than that of $Au/SnO_2/n$-Si diode (3.10) [24] and difference between these ideality factors is due to interface inhomogeneities of the diodes.

The ideality factor of $Ag/SiO_2/n$-Si leads to layer interfacial thickness of 36.05 Å [1,2]. The obtained insulator layer thickness is less than 50 Å, this suggests that direct tunneling is taking place in this MIS diode. The tunneling barrier height for the diode was calculated using tunneling factor via Eq. (2) and was found to be 0.34 eV. This indicates that the interface oxide affect the barrier height of the diode. The n value obtained from I–V characteristics of the diode is attributed to the presence of a thin interfacial insulator layer between the metal and semiconductor. The downward curvature at sufficiently higher voltages is caused by the effect of series resistance R_s, apart from the presence of the interface states [25]. The $Ag/SiO_2/n$-Si diode can be further characterized using capacitance–voltage (C–V) characteristics. The C–V characteristics of the $Ag/SiO_2/n$-Si diode at 10 kHz and 1 MHz frequencies are shown in Fig. 4. The shape of the C–V curve under 1 MHz indicates n-type behaviour. The capacitance increases with increasing positive voltage until accumulation steady state. The accumulation capacitance for the device was found to be 3.25 nF. This capacitance results from the native oxide layer between Si and metal. The voltage dependence on capacitance allows us to use the relation between capacitance and voltage given by [1]

$$\frac{1}{C^2} = \frac{2(V_{bi} + V)}{A^2\varepsilon_s q N_D} \tag{7}$$

where V_{bi} is the built-in potential, ε_s is the dielectric constant of semiconductor and N_D is the donor concentration. The barrier height can be obtained using the relation above. For this, we use the following relation [1]:

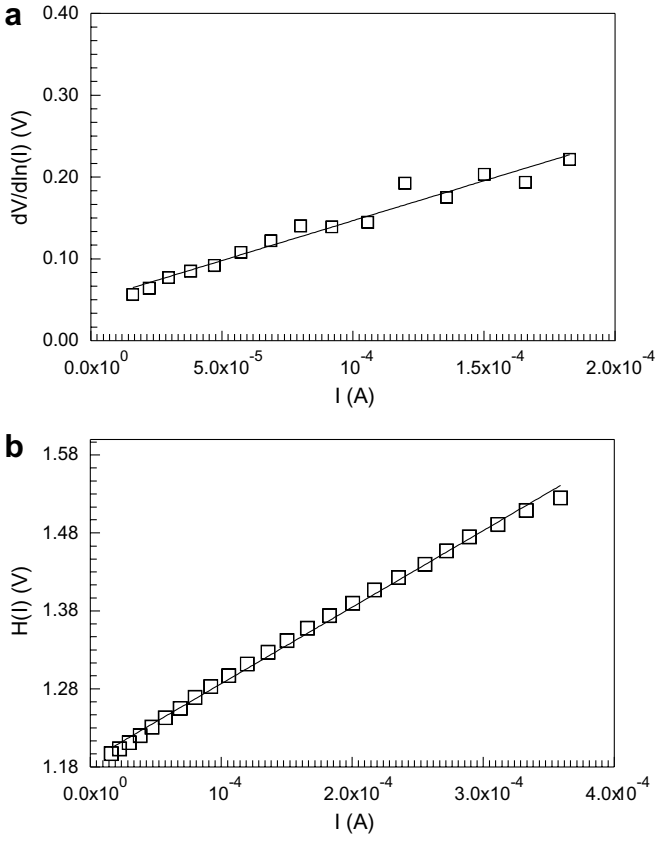

Fig. 3. Plots of $dV/d\ln I$ and $H(I)$ vs. I of the $Ag/SiO_2/n$-Si diode.

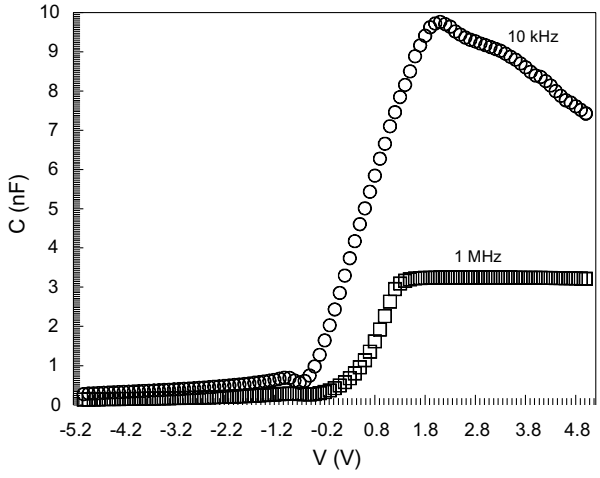

Fig. 4. C–V plots of the $Ag/SiO_2/n$-Si diode at 10 kHz and 1 MHz frequencies.

$$q\phi_{b(C-V)} = qV_{bi} + kT\ln\left(\frac{N_c}{N_D}\right) \quad (8)$$

where N_c is the effective density of state in the band conduction of silicon ($N_c = 2.8 \times 10^{19}\,cm^{-3}$). N_D was calculated from the slope of C^{-2}–V plot, as shown in Fig. 5 and was found to be $1.17 \times 10^{14}\,cm^{-3}$. The value of $V_{bi} = 0.17$ V was calculated from the intercept of Fig. 5. The barrier height can be obtained from the C–V measurements using Eq. (8). The $\varphi_{b(C-V)}$ value was calculated using V_{bi} and was found to be 0.50 eV. The $\varphi_{b(C-V)}$ value is lower than the $\varphi_{b(I-V)}$ value. This is probably due to the barrier inhomogeneities. It is seen that the barrier heights deduced from two techniques are not always the same. The discrepancy between $\varphi_{b(C-V)}$ and $\varphi_{b(I-V)}$ can be explained by distribution of Schottky barrier height due the inhomogeneities such as non-uniformity of the interfacial layer thickness and distributions of the interfacial charges [26,27]. The inhomogeneities affect apparent Schottky barrier height as current across interface depends exponentially on Schottky barrier height and the current is sensitive to barrier distribution at the interface. The barrier height obtained from C–V method includes an average value of Schottky barrier heights of patches available in the contact. The determination of Schottky barrier height from I–V characteristics is only reliable if one can be confident that the current is determined by thermionic emission (TE) theory [28]. According to TE, forward current–voltage characteristic gives a good straight line and in turn, one obtains a reliable value of barrier height. We can evaluate that the value of barrier height obtained from C–V measurement for the diode studied is reliable.

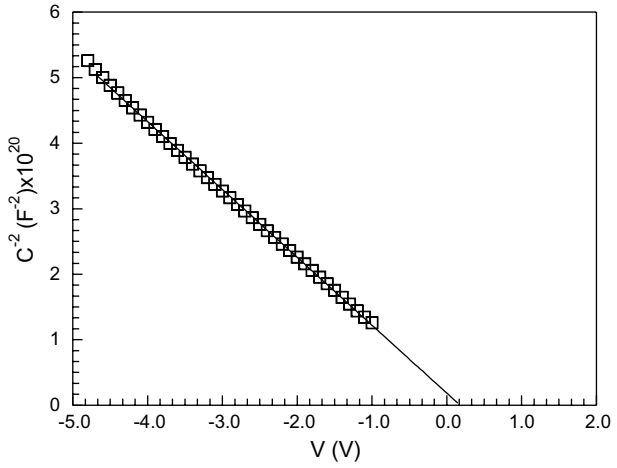

Fig. 5. Plot of C^{-2}–V of the Ag/SiO_2/n-Si diode.

The alternating current (AC) conductance can be expressed as [29]

$$G(f) = G_{dc} + Df^s \quad (9)$$

where G_{dc} is the direct current conductance, D is a constant and s is the exponent which lies $0 < s < 1$. Fig. 6 shows the conductance dependence on frequency for Ag/n-Si diode at different biases. The curves observed in figures exhibit two regions corresponding to different conduction mechanisms. In the first region, conductance does not change by frequency, i.e., direct current conductivity. Whereas in the second region the conductance increases with increasing frequency. The AC conductance of the Ag/n-Si diode is consistent with typical of hopping conduction in polycrystalline and amorphous materials. The s values at different biases were determined by fitting the Fig. 6 and s values were found as 0.45–0.55. The calculated s values confirm that hopping is the dominant mechanism of electron transport in the Ag/n-Si diode. These values suggest that empty probability of the traps changes with electric field applied. The s values suggest that 45–55% of traps are empty. Fig. 7 shows plots of C_p–f at different bias voltages. The capacitance of the diode decreases with increasing frequency. This suggests the presence of interface state traps inside

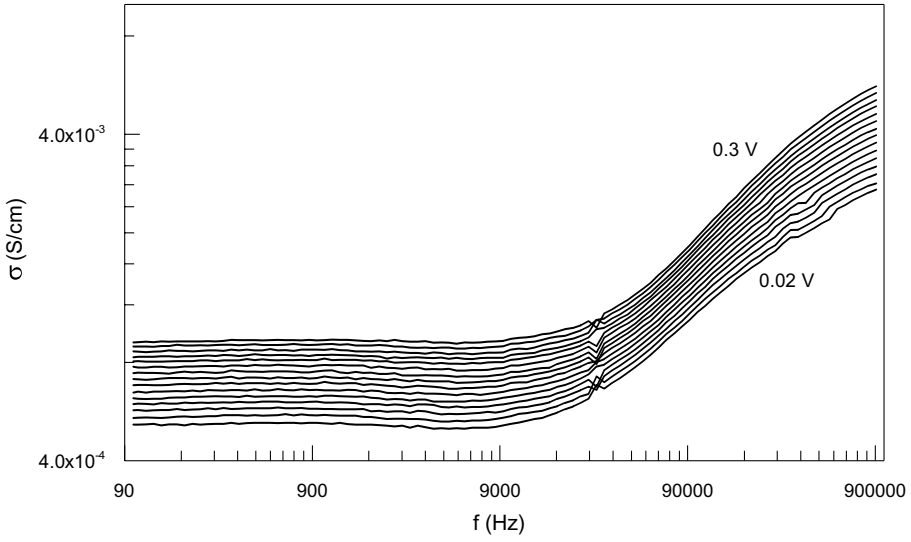

Fig. 6. The conductance vs. frequency plots of the Ag/SiO_2/n-Si diode (0.0–0.30 V with steps of 0.02 V) at room temperature.

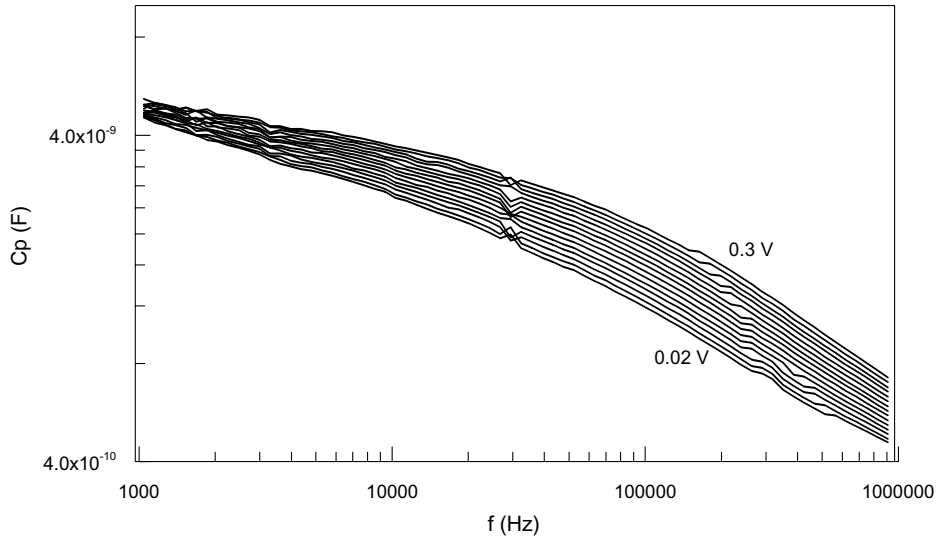

Fig. 7. The capacitance vs. frequency plots of the Ag/SiO_2/n-Si diode (0.0–0.30 V with steps of 0.02 V) at room temperature.

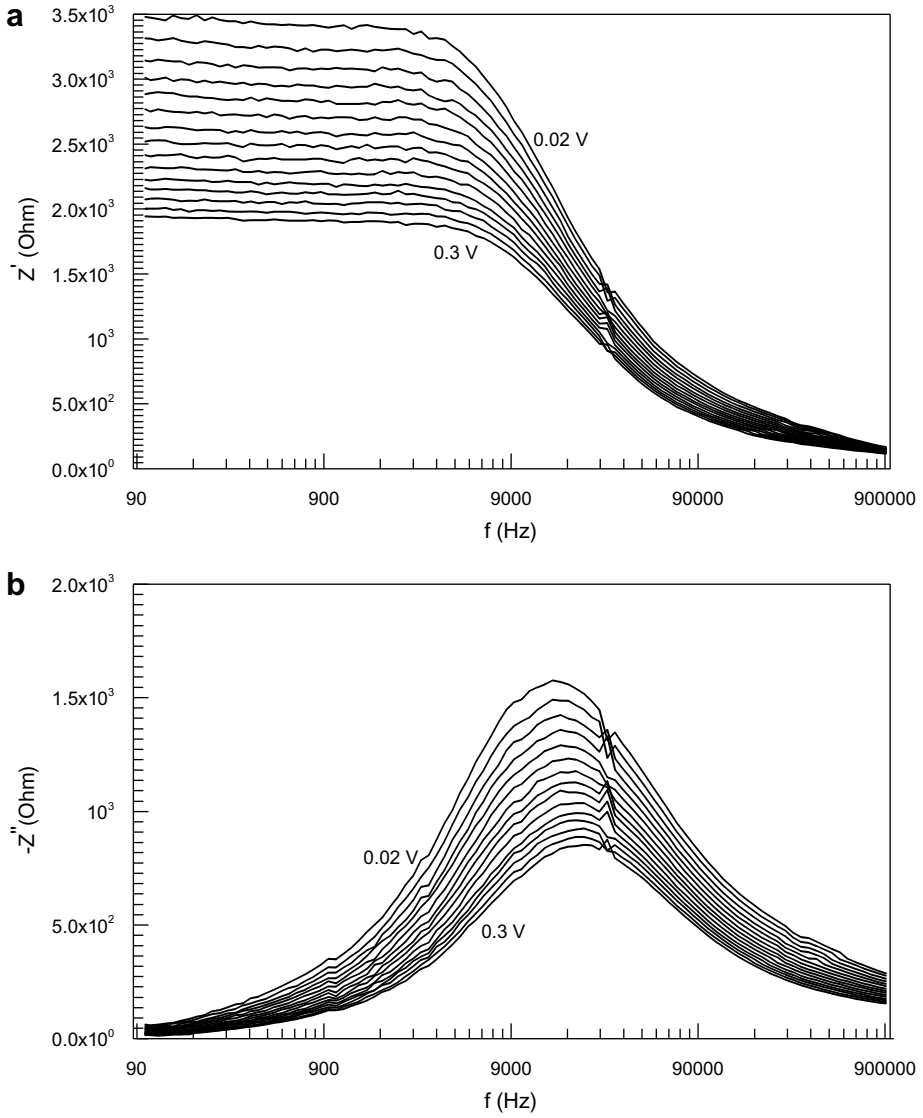

Fig. 8. The real and imaginary parts of impedance vs. frequency plots of the Ag/SiO_2/n-Si diode (0.0–0.30 V with steps of 0.02 V) at room temperature.

the diode. Fig. 8a and b show the real and imaginary parts of the complex impedance at different bias voltages. It is well known that the complex impedance for the diode is expressed as

$$Z^* = \mathrm{Re}(Z) + \mathrm{jIm} \tag{10}$$

where $\mathrm{Re}(Z)$ and $\mathrm{Im}(Z)$ are real and imaginary parts of the complex impedance, respectively.

In literature, the real and imaginary parts of the complex impedance are expressed as

$$\mathrm{Re}(Z) = R_s + \frac{R_p}{1 + (\omega/\omega_0)^2} \tag{11}$$

and

$$-\mathrm{Im}(Z) = \frac{R_p(\omega/\omega_0)}{1 + (\omega/\omega_0)^2} \tag{12}$$

where $\omega_0 = 1/R_pC_p$. At lower frequency, the real part of impedance for the diode indicates a plateau region. In this region, the complex impedance results from interface properties of the diode and the impedance decreases as bias voltage increases. After the plateau region, the impedance decreases drastically with increasing frequency. The imaginary part of the impedance shows a peak maximum, suggesting a relaxation mechanism. The position of this peak shifts to higher frequencies. This suggests that the relaxation frequency is shifted to increasing bias voltages. The relaxation time dependence of bias voltage is shown in Fig. 9 and τ values decreases with bias voltage. This suggests that the orientation of electrical charges in the interface is facilitated by bias voltage. The relaxation mechanism for the diode can be analyzed by Cole and Cole curves. Fig. 10 shows Cole–Cole plots at different voltages. Cole–Cole plot indicates a single semicircle for various voltages. In the complex plane, radius of semicircle is decreasing with increasing bias voltages. The parallel resistance R_p and capacitance C_p values were determined from

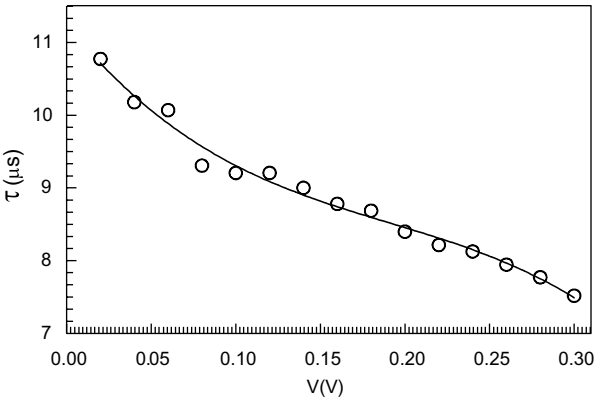

Fig. 9. Plot of τ–V of the Ag/SiO_2/n-Si diode.

the Cole–Cole plots and plots of R_p–C_p vs. V are shown in Fig. 11. The C_p values are almost constant with bias voltage. The R_p values decreases with increasing bias voltages.

As seen in Fig. 4, the curve at low frequency (10 kHz) shows a peak at around 2.08 V. This peak is due to the contribution from the interface states present at the Schottky interface and also due to the injected minority carriers from the back contact [30]. It is evident from the Fig. 4 that the low frequency characteristics are more sensitive to the interface states [31]. Considering that the interface states are continuously distributed in the energy gap and the expression for the effective capacitance is expressed as

$$\frac{1}{C_{\mathrm{total}}} = \frac{1}{C_d} + \frac{1}{qD_{it} + \frac{\varepsilon_i/\delta}{1+\omega^2R_t^2(\varepsilon_i/\delta)^2}} \tag{13}$$

where R_t is the resistance due to tunneling of carrier through the interface, C_d is the depletion capacitance, D_{it} is the interface state density, δ and ε_i are thickness and permittivity of the interfacial layer, respectively. It is evaluated that the interface states respond to the alternating current signal especially at low frequency (<10 kHz) and it has

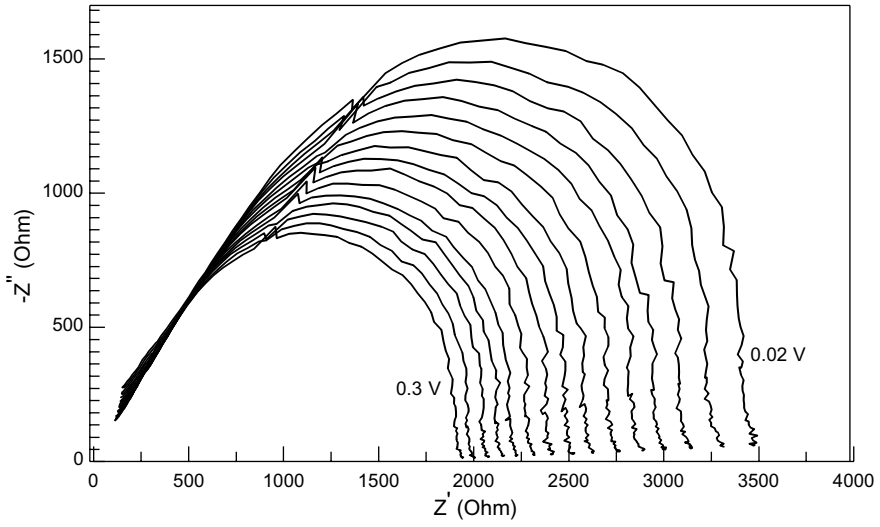

Fig. 10. Cole–Cole plots of the Ag/SiO_2/n-Si diode (0.0–0.30 V with steps of 0.02 V) at room temperature.

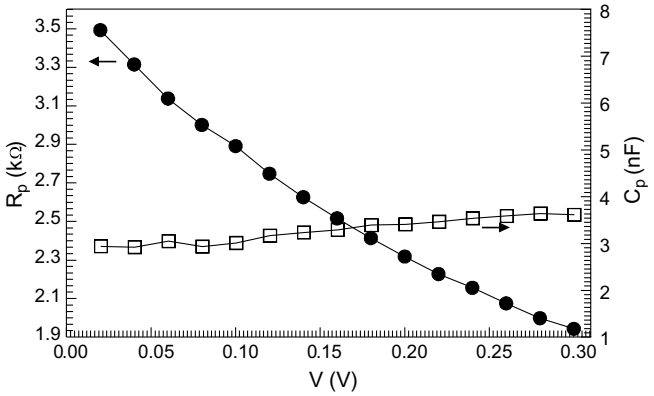

Fig. 11. Plots of R_p–C_p vs. V of the Ag/SiO_2/n-Si diode.

been shown in Eq. (13) that the capacitance contribution from the D_{it} at a low frequency is nearly qD_{it} [32]. In the literature, the density of the interface states can be calculated from the capacitance–voltage measurements, in which capacitance–voltage measurements were performed at 10 kHz and 1 MHZ frequencies to determine interface states [33,34]. The capacitance of the interfacial layer is effectively in series in with capacitance of the depletion region. For the MIS diode having interfaces, the ideality factor is higher than unity. The density of the interface states at equilibrium with semiconductor for a MIS structure can be determined by the following relation [35]:

$$D_{it} = \frac{\varepsilon_i/\delta}{qC_{HF}} \frac{C_{HF} - C_{LF}}{C_{LF} - \varepsilon_i/\delta} \sqrt{q\varepsilon_s N_a / 2\psi_s} \tag{14}$$

where C_{HF} and C_{LF} are high and low frequency capacitances given by the relations

$$C_{LF} = \frac{\left(qD_{it} + \sqrt{\frac{q\varepsilon_s N_D}{2\psi_s}}\right)}{\left(1 + (qIR_s/kT) + \frac{\delta}{\varepsilon_i}\left(q^2 D_{it} + \sqrt{\frac{q\varepsilon_s N_D}{2\psi_s}}\right)\right)} \tag{15}$$

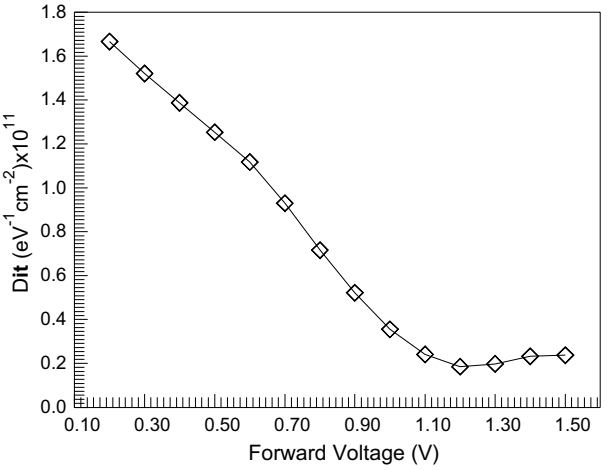

Fig. 12. Variation of D_{it} values with forward applied voltage for the Ag/SiO_2/n-Si diode.

and

$$C_{HF} = \frac{\sqrt{\frac{q\varepsilon_s N_D}{2\psi_s}}}{\left(1 + (qIR_s/kT) + \frac{\delta}{\varepsilon_i}\left(\sqrt{\frac{q\varepsilon_s N_D}{2\psi_s}}\right)\right)} \tag{16}$$

where ψ_s is the surface potential. The interface density D_{it} was calculated from the C–V curves and is shown in Fig. 12. The interface density D_{it} ranges from 1.66×10^{11} eV^{-1} cm^{-2} to 0.18×10^{11} eV^{-1} cm^{-2}. The interface density D_{it} of the Ag/SiO_2/n-Si studied is lower than that of Au/SnO_2/n-Si diode. This suggests that the interface oxide layer between metal and semiconductor modifies the interface state properties of the diode.

4. Conclusions

The current–voltage and capacitance voltage characteristics of Ag/SiO_2/n-Si Schottky diode have been investigated. The obtained results suggest that Ag/n-Si structure obeys a metal–interface layer–semiconductor configuration rather than the ideal Schottky barrier diode. The interfacial oxide layer modifies the electronic parameters of Ag/n-Si/Schottky diode. The interface state density was found to vary from 1.66×10^{11} eV^{-1} cm^{-2} to 0.18×10^{11} eV^{-1} cm^{-2}.

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