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Effects of measurement temperature and metal thickness on Schottky diode characteristics

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ABSTRACT

Ti Schottky contact (SC) metal with 50 nm and 100 nm thickness on *n*-GaAs substrate was sputtered by DC magnetron into vacuum unite. It was checked whether the diode parameters changed with SC metal thickness and measurement temperature. As a result of measurements, the potential barrier values decreased while ideality factors remained unchanged with the increasing metal thickness. The results showed that the Ti film thickness has a considerable effect on the barrier potential value. The potential barrier value of the device with thickness of 50 nm was found to be 0.92 and 0.63 eV, and that of 100 nm thickness to be 0.80 and 0.56 eV at 300 and 60 K, respectively. That is, a different of 0.12 eV for the barrier potential was obtained depending on metal thickness at 300 K.

1. Introduction

Ohmic and rectifier contacts are always need in fabrication of the opto-electronic and integrated circuits. That is, the metal/GaAs rectifier or ohmic contacts are usually used MESFETs (Metal–semiconductor field-effect transistors), high-speed microelectronic applications and microwave communication device fabrication [1–10]. However, researchers are still far from a complete understanding of the Schottky rectifier contact components [11–22]. Therefore, more information must be available about semiconductor/metal contacts. Schottky contact metal/semiconductor (MS) interface quality in device fabrication plays an important role in the determining their characteristics. Schottky rectifier contact parameters such as potential barrier height and diode resistance highly depend on stability and reliability of the MS interface properties [3,4,11–28].

The barrier height which controls the current conduction across the MS interface is one of the most important diode parameters of the Schottky barrier diode (SBD). In the MS contacts, Schottky contact (SC) metal interacts with the semiconductor substrate depending on metal coverage change. The effect of the SC metal thickness on the diode parameters was investigated by some researchers [11–18]. Their results showed that the SC metal thickness has an important role on the MS interfacial performance and potential barrier modification, ideality factor, diode resistance and reverse saturation current [11–14,20,22,27]. The potential barrier increase in Schottky contacts can improve rectification behavior and potential barrier decrease can reduce the voltage drop in forward bias. The electrical characteristics such as switching speed and voltage drop in the Schottky diodes can be directly improved by controlling potential barrier and its stabilization [11–16,29,30]. Sometimes, the metal/insulator/semiconductor (MIS) structures [30–32] and the metal/semiconductor/semiconductor heterojunctions [33–35] and semiconductor surface treatment [36–39] were also used for the barrier height (BH) modification of the SBDs. That is, the BH modification can be formed using an insulator or semiconductor layer at the MS interface. Investigating temperature dependent properties of MS contacts with different metal thicknesses may route to find relation between them.

We have investigated effects of Schottky contact metal thickness on diode parameters as a function of measurement temperature (MT). For this purpose, Ti/*n*-GaAs/In diodes with different metal thicknesses (50 and 100 nm) were fabricated. The Schottky metallization of Ti was sputtered by DC magnetron. The device with 50 nm Schottky metal thickness was named Ti(50 nm) and the other device with 100 nm thickness was named Ti(100 nm). The *I-V* data of these SBDs were

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measured in the temperature range of 60–320 K by the steps of 20 K. The experimental procedure was detailed in a previous study [25]. The samples were prepared using cleaned and polished *n*-GaAs (as received from the manufacturer) with (100) orientation and 2.3×10^{15}–3.2×10^{15} cm^{-3} carrier concentrations.

2. Results and discussion

The experimental *I–V* data can be analyzed by means of the thermionic emission (TE) equation. The *I-V* characteristic, when $V \geq 3kT/q$ predicted by the TE equation, is stated as follows [1–5]:

$$I = I_0\left[\exp\left(\frac{eV}{nkT}\right)\right] \tag{1}$$

where I_0

$$I_0 = AA^*T^2 exp\left(\frac{-e\Phi_{b0}}{kT}\right) \tag{2}$$

is saturation current. The quantities *A, A*, T, k, q* and Φ_{b0} are the diode area, the effective Richardson constant of 8.16 $cm^{-2}K^{-2}$ for *n*-type GaAs, temperature in Kelvin, Boltzmann constant, electronic charge and the barrier height (BH), respectively. The *n* is ideality factor and it considers the deviation of the ideal current flow mechanism, and from eqn. (1) it is given as

$$n = \frac{e}{kT}\left(\frac{dV}{dlnI}\right) \tag{3}$$

The forward-bias *I–V* measurements in 60–320 K range for both Schottky diodes were given in Fig. 1(A) and (B). The *I-V* curve at each temperature in Fig. 1 has a large linear region, in contrast to higher current region that departures from linearity by effect of the device series resistance. Fig. 2 displays the comparison of the current characteristics as a function voltage for both diodes at 100, 200 and 300 K. Effect on the current data of the barrier metal thickness can be clearly seen. In Fig. 2, when considered the current curves up to region that the series resistance affects, the current across the Ti(50 nm) diode at a given bias voltage makes the difference by approximately two order of magnitude of current than that of the Ti(100 nm) at each temperature. The slope of the linear portion of the *I-V* curve at each temperature for both diodes has been given Table 1. The slope increases with decreasing temperature, this clearly seems in especially Fig. 2. As can be seen from Figs. 1 and 2, the linear current regions obey Eqs. (1)–(3) quite well with reasonable Φ_{b0} and *n* values.

As seen from Fig. 1(A) and (B), the both diodes have similar *I–V* characteristics. The *I–V* curves for 120 K and lower temperatures in Fig. 1 look like *I–V* curves for higher temperatures (approximately the same slope and voltage shift between the curves), this does not seem that some other current mechanism transport over the barrier starts to be prevalent for lower temperatures. In lower temperatures below 120 K, the relation between temperature and current flow can be explained by the current flow across inhomogeneous MS contact [7,8,11,39–53]. The presence of the charge tunneling across the barrier may not be present due to the low doping level of the GaAs substrate, 2.3×10^{15}–3.2×10^{15} cm^{-3} carrier concentrations [46,51,54–57]. That is, the carriers may surmount the patches of lower barrier heights across the MS interface even though tunneling do not dominate in the carrier conduction at lightly doped MS contacts [46,51,52,54–57]. The current preferentially flows through the low BH with the temperature due to the BH inhomogeneity. Atomic structure of the interface, the atomic inhomogeneities, non-uniform interface charges, defects, multiple phases, grain boundaries and facets all probably have an important role in the function and modification of BH [7,8,11,39–47,52,53].

The appearing values of the BH Φ_{b0} and the ideality factor *n* for both devices were determined from the linear part of the forward-bias *I-V* curves, respectively, using eqns. (2) and (3). The values of these

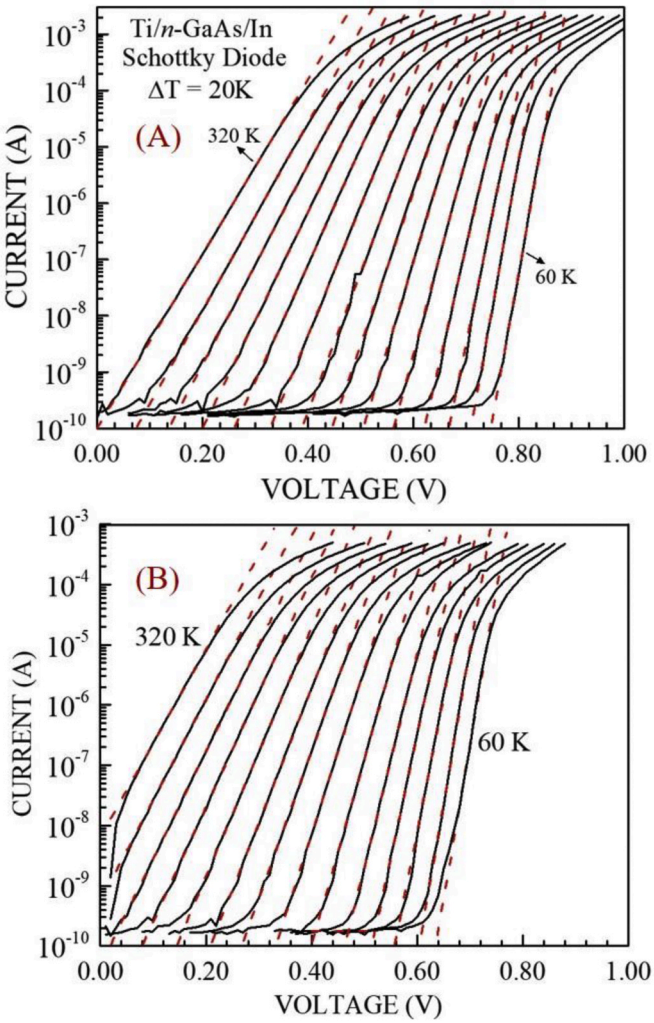

Fig. 1. Current-Voltage-temperature characteristics for both Schottky diodes with (A) 50 nm (B) 100 nm Schottky metal (Ti) thickness. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

parameters obtained by the standard TE equations above as a function of measurement temperature are given in Table 1 and Fig. 3(A) and (B), respectively. The *n* versus temperature curves and *n* values at each temperature for both devices overlap each other over the whole temperature range. The value of *n* remains approximately unchanged down to 120 K, and then increases with decreasing temperature. That is, the ideality factor values are almost independent on temperature above about 120 K. The corresponding values are between 1.00 and 1.02. The Φ_{b0} value changes from 0.63 eV at 60 K to 0.91 eV at 320 K for the Ti(50 nm) diode and from 0.56 eV at 60 K to 0.81 eV at 320 K for the Ti(100 nm) diode. Furthermore, The Φ_{b0} value for both diodes decreases with a decrease in temperature from 60 K to 120 K. Ideality factor values for both change from 1.00 to 1.04 between 140 K and 320 K, and increased with the decrease in temperature below 120 K.

The barrier height value increased with decreasing Schottky contact metal thickness. Biber et al. [11] obtained similar results and reported that the SBH value for the Au(5 nm) and Au(65 nm)/*n*-GaAs diodes have ranged from 0.84 to 0.94 eV and from 0.83 to 0.85 eV at 300K, respectively. They [11] determined the lateral homogeneous SBH values of 0.94 eV and 0.87eV for the Au(5 nm) and the Au(65 nm)/*n*-GaAs diodes from the linear relationship in the SBH versus the ideality factor plots. Jang and Lee [12] revealed the result that the barrier height decreased from 0.6 eV to 0.49 eV at 300 K when they the barrier metal

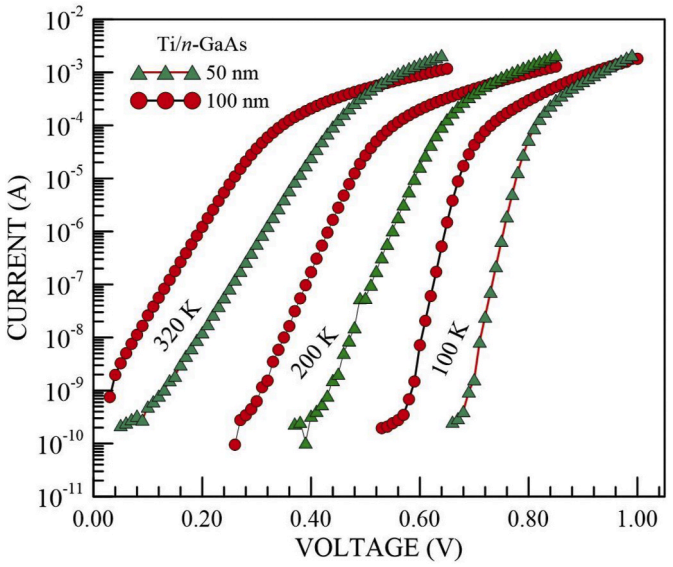

Fig. 2. Comparison of the current characteristics as a function of bias voltage for both devices at 100, 200 and 300 K. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Table 1
Diode parameters obtained from temperature-dependent *I-V* characteristics.

T (K)	Barrier Height (eV)		Ideality Factor		The Slopes for IVT curves	
	50 nm	100 nm	50 nm	100 nm	50 nm	100 nm
60	0.63	0.56	1.56	1.57	120.00	117.71
100	0.88	0.77	1.09	1.10	105.23	102.21
140	0.93	0.84	1.02	1.00	50.58	81.43
180	0.93	0.82	1.01	1.02	62.41	63.10
220	0.94	0.81	1.01	1.02	52.00	51.21
280	0.92	0.80	1.01	1.00	41.00	41.00
300	0.92	0.80	1.00	1.00	38.16	38.54
320	0.91	0.81	1.02	1.00	35.71	36.00

thickness increased from 50 to 90 nm in Ti/*p*-type Si diodes. They [12] ascribed the barrier height decrease with increase of the metal thickness to the impurity concentration change at the contact interface, with their results supported by SIMS measurement. Wang et al. [13] introduced the *I–V* measurements of Au/*n*-GaN MS contacts with different metal film thickness up to130 nm. Their *I–V* measurement results showed a steady decrease in the quality of the SBDs for increasing Au film thickness, and indicated that thin (<50 nm) film Schottky diodes showed significantly better rectification characteristics than those of thick Au films (>50 nm) [13]. It was emphasized that there is a BH reduction from about 0.78 eV for the thinnest films to about 0.69 eV for the thickest films from the *I-V* curves and that the thickness of the Au film should be kept below 50 nm for the performance and reliability of these contacts [13]. Their Auger electron spectroscopy (AES) depth profile studies demonstrated that V_{Ga} defects produced on the GaN by the out-diffusion of Ga into the Au layer could be responsible for the BH modification in the Au/GaN contacts. Again, Wang et al. [13] showed by depth profiling AES that the Au/GaN junction interface width increases with increasing Au thickness, suggesting considerable inter-mixing of Au, Ga and N. Gullu et al. [14] reported that the BH ranges from 0.855 eV (for 5 nm) to and 0.794 eV (for 100 nm) for the un-annealed Au/*n*-GaAs diodes, and ranges from 0.920 eV (for 5 nm) to 0.774 eV (for 100 nm) for the H2 pre-annealed Au/*n*-GaAs diodes, respectively, from the *I-V* curves at 300K. Wu et al. [15] demonstrated experimentally that the effective SBH in the SBH of metal/TaN/*n*-Ge junctions pinned from 0.53–0.61 eV–0.44 eV with an increase in the TaN thickness from 0 to 10 nm. They [15] ascribed the

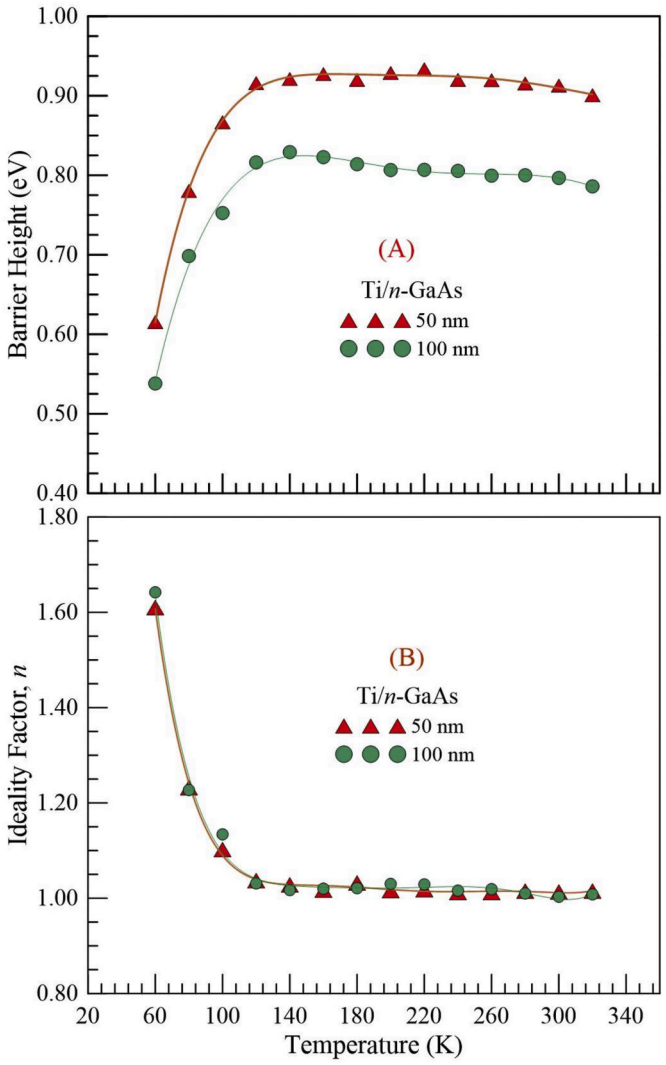

Fig. 3. Measurement temperature plots of (a) ideality factor and (b) barrier height. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

modulation of the SBH to the interdiffusion between the cap metals (Al, Fe, and Ni) and TaN. Masri and Langlade [16] presented that the metal-induced interface states in the semiconductor forbidden gap forced towards higher energies by increase in the Schottky contact metal thickness and that there are very sensitive to metal thickness changes. Furthermore, Ahmadi [51] revealed from the experimental forward bias *I-V-T* curves that the barrier height was decreased with increasing thickness of the epitaxial layer in Ti/Au/Si:$Al_{0.33}Ga_{0.67}As$/*n*-GaAs Schottky diodes.

It was reported [58–61] that the deposition of thin metal layers to a semiconductor substrate leads to band bending with the Fermi level (FL) shifting towards the mid-gap of the *n*- or *p*-type semiconductors. The position of the FL at a metal-*n* type semiconductor (*p*-type) interface relative to the conduction band (to the valence band) is accepted to be constant across the semiconductor band gap. Such a pattern can also be understood in terms of the different pinning mechanisms. The sufficiently high density of the defect energy levels inside the semiconductor band gap can pin the FL. These defects may be generated when the metal atoms condense on the semiconductor surface. They are the so-called metal induced gap states (MIGS) originating from metal wave function tailing into the semiconductor [58,59]. Ludeke [60] have studied this possibility further for silver deposited on *n*- and *p*-type GaAs surfaces. Silver is a relatively unreactive metal, and the position of the FL as a

function of the metal thickness was investigated. The experimental points for *n*- and *p*-type samples did not meet but remained separated by around 0.2 eV for silver coverages, as seen in their Fig. 5 [60]. Spicer et al. [62,63] experimentally found that the thin metal deposition layers leads to band bending with the FL shifting towards the mid-gap, for both *n*- and *p*-type crystals, and reported that the FL reaches its final position very rapidly when Al, Ga, and In are deposited on GaAs cleaved surfaces due to interaction between the metal adatom and substrate, and that the final pinning position is obtained with a low coverage, as can be seen in their Fig. 2 [62] and Fig. 1 [63]. They concluded that the Schottky barrier height was determined not by levels directly induced by the orbitals of the adatoms but by defect levels induced indirectly by the metal adatoms [62,63].

Again, Ludeke et al. [60] discussed the applicability of other generalized Schottky barrier models to the Ag/GaAs contact, and observed variation of the surface FL with coverage necessitates an interface level of variable energy; that is, for each increment in deposited metal thickness or cluster size, a new level is responsible for stabilizing the FL at that coverage. If this defect level was the consequence of a specific interaction of the Ag with the surface, and in a position deeper in the gap, then for an increasing number of levels proportional to the coverage, the FL position would shift towards the mid-gap, as can be seen in their Fig. 5 [60]. More recently, Newman et al. [64] presented the results of a more complete study for a wider range of metals on GaAs surfaces. They [64] measured the pinning energies for ultra-thin coverages of thick metal coverages on clean cleaved *n*-GaAs surfaces and ultra-thin coverages of adatoms on *n*- and *p*-type GaAs surfaces. They [64] showed that the FL pinning positions shifted towards the mid-gap for ultra-thin layers of metals on *n*- and *p*-type crystals.

Fig. 4 displays *nT* versus temperature dependence for both Ti/*n*-GaAs Schottky diodes. This plot is the "T_0 anomaly plot", where T_0 is a constant called the excess temperature and is a direct consequence of a real Schottky contact with the inhomogeneous barrier distribution [47,51,54,56,65–69]. As seen from Fig. 4, it can be said that the current across the devices obeys the TE current eqn. (1) with the values of $T_0 = 3.43$ for Ti(50 nm) device and $T_0 = 5.00$ for Ti(100 nm) device down to 120 K. The current flow across the devices may be attributed to the increase in charge tunneling effect at temperatures below 120 K, that is, may be said that the current transport dominates by the thermionic field emission (TFE) current [46,54–56], or that the current preferentially flows through the low BH with the temperature due to the barrier height inhomogeneity [7,8,11,39–54,59].

We can find effective BHs for both diodes from Fig. 5 which represents the Richardson or Arrhenius plots by the saturation I_0 values of the *I-V-T* characteristics. The effective BHs values of 0.93 eV for Ti(50 nm) device and 0.84 eV for Ti(100 nm) were determined from the slope of the linear part of the *I-V-T* curves in Fig. 5. The BH values are in close agreement with the BH values at the room temperatures given above for both devices, and thereby, say that the current transport is dominated by TE. The deviation of the linearity in the curves of this plot below 120 K mentions the deviation of the TE current.

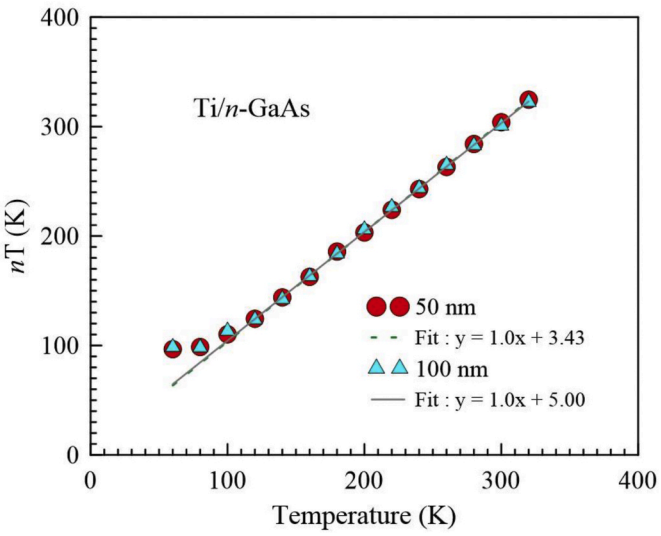

Fig. 4. *nT* versus temperature plots for both diodes. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

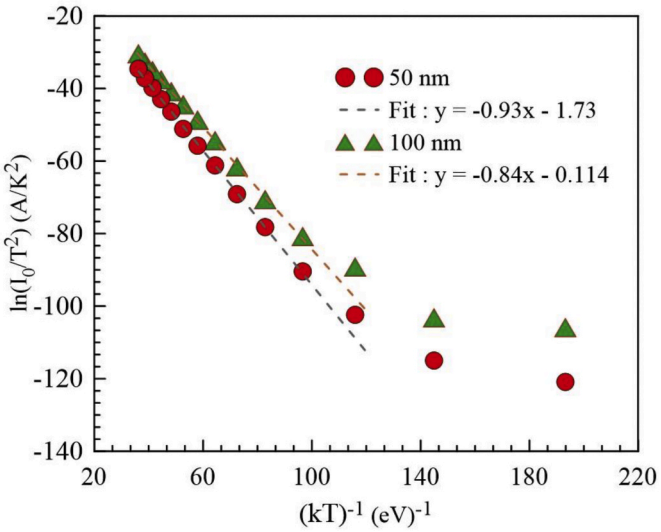

Fig. 5. Richardson or Arrhenius plots by the saturation I_0 values obtained from temperature dependent *I-V* characteristics for both Ti/*n*-GaAs Schottky diodes. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

3. Conclusion

It was that the device parameters become almost independent of temperature and nearly ideal in the temperature range of 120–320 K. The results obtained for the Ti/*n*-GaAs diodes in the temperature range of 60–320 K have indicated that the barrier height decreases with the increasing Schottky metal thickness. Therefore, Schottky metal thickness can be used for achieving the desired SBH value. We have found that SBDs with thicker Schottky metal thickness are slightly less sensitive to temperature changes.

Credit author statement

Sample Preparation: Nezir Yıldırım and Tuna Göksu. Taking measurements: Tuna Göksu, Nezir Yıldırım and Ahmet Özdemir. Evaluation of data: Abdulmecit Turut, Ahmet Özdemir, Tuna Göksu. Writing the article: Abdulmecit Turut.

Declaration of competing interest

The authors announce that they have no conflict of interest.

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