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Device physics underlying silicon heterojunction and passivating-contact solar cells: A topical review

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Abstract

The device physics of commercially dominant diffused-junction silicon solar cells is well understood, allowing sophisticated optimization of this class of devices. Recently, so-called passivating-contact solar cell technologies have become prominent, with Kaneka setting the world's silicon solar cell efficiency record of 26.63% using silicon heterojunction contacts in an interdigitated configuration. Although passivating-contact solar cells are remarkably efficient, their underlying device physics is not yet completely understood, not in the least because they are constructed from diverse materials that may introduce electronic barriers in the current flow. To bridge this gap in understanding, we explore the device physics of passivating contact silicon heterojunction (SHJ) solar cells. Here, we identify the key properties of heterojunctions that affect cell efficiency, analyze the dependence of key heterojunction properties on carrier transport under light and dark conditions, provide a self-consistent multiprobe approach to extract heterojunction parameters using several characterization techniques (including dark J-V, light J-V, C-V, admittance spectroscopy, and Suns-Voc), propose design guidelines to address bottlenecks in energy production in SHJ cells, and develop a process-to-module modeling framework to establish the module's performance limits. We expect that our proposed guidelines resulting from this multiscale and self-consistent framework will improve the performance of future SHJ cells as well as other passivating contact-based solar cells.

KEYWORDS

amorphous semiconductors, current-voltage characteristics, heterojunctions, passivating contacts, process control, silicon, modeling and simulation

1 | INTRODUCTION

With a newly installed capacity of over 100 MW per day on average, photovoltaic (PV) solar cells have become the fastest growing class of solar energy–harvesting technologies.[1] The large-scale deployment of PV has so far been mainly based on diffused-junction silicon solar cells. The increased electronic quality of crystalline silicon (c-Si) wafers at acceptable cost, dielectric surface passivation schemes, and the possibility of making direct metal-silicon contacts on relatively lightly doped surfaces have been important factors—in addition to economies of scale—in driving down the cost per Watt of generating solar power during the last two decades. The device physics underlying such solar cells is well understood, and this knowledge—coupled with device and material characterization —has been an important contributing factor to the increasing sophistication of solar energy technologies.

In recent years, tremendous progress has been made in the conversion efficiency of silicon solar cells, now at a record[2] of 26.63%, largely thanks to the application of so-called passivating contacts. Key to high performance of passivating-contact technology is that the metal contacts are displaced from the semiconductor by insertion of an ultrathin (few nm) buffer layer, aimed at passivating the silicon surface states. In addition, these contacts feature a material that provides carrier selectivity, inducing a potential at the c-Si surface. As such, passivating contacts render diffused junctions—along with a large part of the well-known device physics describing the precise working principles of diffused-junction technologies—obsolete.

Large-scale deployment of passivating contacts solar devices requires accurate and physically sound modeling and characterization efforts to identify losses and enable further process sophistication. This

is because even a small improvement in efficiency has significant impact on the levelized cost of energy (LCOE) of a PV technology. For example, a 10% relative increase in performance of a 17.2% efficient module can result in a 7.5% decrease in its LCOE.[3] Here, we review the device physics of passivating contact silicon heterojunction (SHJ) solar cells to establish a multiscale and self-consistent framework to improve the performance of future SHJ PV technology.

1.1 | Solar cell classification based on carrier collection: theory of ideal vs practical cells

In an "ideal" solar cell (see Figure 1A), the photo-generated carriers reside for a sufficiently long time in the absorber so that they can diffuse/drift to the appropriate contacts where they are collected without incurring carrier loss through recombination in the absorber's bulk or at its surfaces. In this context, *carrier-selective* contacts create asymmetric potential barriers so that the majority carriers are collected without any hindrance, while the minority carriers are rejected fully (see Figure 1B).

In practice, solar cells are designed to approximate this idealized configuration to achieve efficient extraction of photogenerated carriers. Depending on the specific approach to charge extraction, solar cells may be broadly divided into 3 categories:

1. *diffused homojunction* solar cells, such as those used in commercial diffused junction silicon solar cells;

2. *p-i-n homojunction* solar cells, such as a-Si:H thin-film solar cells; and

3. *heterojunction* solar cells, such as CdTe, CIGS and CZTS thin-film solar cells, and SHJ Si wafer-based solar cells.

Briefly, in a typical *diffused homojunction* solar cell, the photogenerated carriers reach their respective contacts mainly through diffusion in the quasi-neutral bulk of the absorber; to be efficient, this process requires long carrier diffusion lengths and thus a high electronic quality of the PV absorber. The contact regions are heavily doped with the respective doping type to achieve carrier selectivity (n-type doping for electron collection, p-type doping for hole collection) but also to achieve low-resistivity contacts (see Figure 1C for a schematic of the energy band diagram). Despite the fact that such contacts have enabled almost all electronic devices, problems in the doping process lead to important electronic losses, such as Auger recombination and bandgap narrowing, as well as to optical losses, such as free carrier absorption of infrared light.

The *p-i-n homojunction* solar cell concept is usually applied to low-cost PV absorbers, which are extremely defective, resulting in very short carrier diffusion lengths, compared to the absorber thickness. In such a case, photogenerated charge-carrier pairs (ie, electrons and holes) are almost instantaneously separated upon generation in the intrinsic absorber layer, under the influence of a built-in electric field. They are then effectively be collected by drift to the appropriate contacts. Due to the poor quality of the absorber, recombination at the contacts is usually not a limiting factor (see Figure 1D).

Diffused[4-6] and p-i-n homojunctions[7] have been studied in great detail, and the properties of these solar cells are reasonably well understood. The classical characterization methods, such as current-voltage (J-V) and capacitance based techniques and protocols, are well developed for these categories of solar cells. However, their cell designs, relying either on impurity doping or defective absorber materials, lead to fundamental limitations in the achievable efficiencies of solar cells based on these structures.[8]
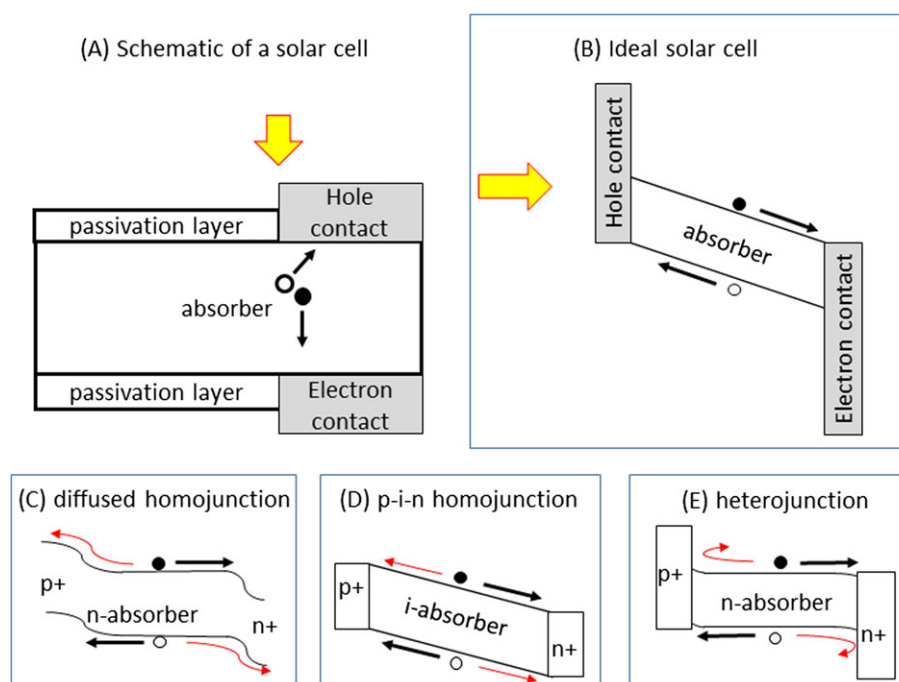
FIGURE 1 A, A schematic of a solar cell structure with the yellow arrow indicating the direction of illumination. Energy band diagrams of: B, an ideal solar cell with photogenerated carriers flowing to respective contacts; C, a diffused homojunction; D, a p-i-n homojunction; and E, a heterojunction. Black arrows indicate majority carrier flow path for collection by appropriate contacts, while the red arrows indicate minority carriers traveling towards and recombining/reflecting at the wrong contacts [Colour figure can be viewed at wileyonlinelibrary.com]

The emerging *heterojunction solar cell* technology inherently involves two or more different materials (see Figure 1E). In these solar cells, carrier selectivity is achieved by depositing films that provide a workfunction that is sufficiently different from the Fermi level in the absorber to induce a potential at the aborber surface, enabling charge collection. Such films are often referred to as electron and hole transport layers (ETL and HTL). In the case of c-Si solar cells, the contacts contain in addition a very thin buffer layer inserted underneath the ETL and HTL, providing chemical surface state passivation, unpinning the Fermi level. Unless carefully optimized, and depending on the materials used, the heterojunction may create an unintended barrier to charge collection. Historically, SHJ was the first passivating-contact technology.[9] Sustained process improvement allowed Panasonic, Japan[10] to claim the world record in 2014. Recently, Kaneka has further improved the performance to 26.6.3%.

Silicon heterojunction solar cells are currently the most successful passivating-contact structures (see Figure 2). The key reasons for the success of this structure are that intrinsic hydrogenated amorphous silicon (a-Si:H) enables excellent chemical passivation of the Si absorber and a-Si:H can be doped as either p- or n-type,[17] which can induce a sufficiently large c-Si surface potential to achieve carrier selectivity (hole collection for a-Si:H(p) overlayers and electron collection for a-Si:H(n) overlayers). As such, a-Si:H is an ideal choice in creating carrier-selective passivating contacts that passivate well. In addition, as described in detail below, there is a significant inversion charge at the a-Si:H/c-Si interface in a fully formed SHJ solar cell that aids in field-effect passivation of the c-Si surface. These intrinsic features are however somewhat counterbalanced by the relatively high parasitic optical absorption and the challenge of controlling the heterojunction barrier between the a-Si:H/c-Si interface, prompting continued search for new passivating contact materials.

Traditionally, SHJ solar cells use intrinsic and doped hydrogenated amorphous silicon stacks for passivating contact formation.[11] In recent years, several new material systems have been reported that as well enable such passivating contacts for c-Si.[12,13] An increasingly important development criterion for such material system—aside from reduced contact recombination and lower material and process costs —is the absence of optical losses.[14] This has motivated the search for dopant-free passivating contacts.[15,16] Ideally, such contacts should also

FIGURE 2 A schematic of a silicon heterojunction (SHJ) solar cell. Here, hole collection occurs at the front side, while electrons are collected at the rear side. Opposite polarities are also possible [Colour figure can be viewed at wileyonlinelibrary.com]

be able to withstand industrial contact firing, as this would lower the metalization cost.

In general, such passivating-contact systems are more complex than their classical homojunction counterparts, involve diverse material systems, and are generally not as well understood. Thus far, classical p-n homojunction theory and models, including the superposition principle for light J-V, ideality factors for the dark J-V, Mott-Schottky analysis of C-V for built-in voltage extraction, and the slope of Suns-V_{OC}, have been used in the analysis of passivating-contact solar cells. However, the direct application of these theories and models to the heterojunction device structure may not be warranted and could lead to misinterpretation of experimental data. Hence, there is a clear need to redefine/reinterpret the theory and models of heterojunction solar cells and to establish an independent and self-consistent framework that explains their performance. Such efforts will provide useful guidelines for improving the process-to-module fabrication cycle for SHJ solar cells. In the following section, we describe the history, technology, and physics of passivating contacts in more detail.

1.2 | The inception of the SHJ technology

The inception of the SHJ technology can be traced back to the development of traditional diffused junction and p-i-n homojunction cells. The earliest silicon-based PV energy conversion system was patented[18] in 1941, while the first p-n diffused junction diode-based solar cell was demonstrated on the same material[19] in 1954. Within a few years, the efficiency of c-Si–based solar cells improved to 11%. With the rise in fossil fuel prices in the early 1970s, there was a growing need for alternative energy sources, such as terrestrial PVs. Ever since, the c-Si PV market has grown steadily, with a current share of more than 90% of the PV market.[11,20] Historically, some of the major design concepts that proved to be vital in improving the c-Si technology and several subsequent technologies were (1) back surface fields below the rear contacts, (2) surface texturing for effective light trapping,[21] (3) passivation of surfaces for noncontacted surfaces, and (4) contacting structures (traditional vs interdigitated back contacts [IBCs][22]), in addition to a constantly increasing electronic quality of the c-Si wafer at affordable price. Currently, the best diffused-junction c-Si cells are based on the passivated emitter rear locally diffused (PERL) design with efficiency[23] of 25% and the IBC design[22] with efficiency of 25.3%.[24-27] Trina solar and Sunpower are some of the leading PV companies actively developing these designs. Moreover, several of these design principles (e.g., back surface field and interdigitated contacts) have influenced the designs of SHJ cells as well.

Meanwhile, in the late 1960s, the discovery of hydrogen-alloyed amorphous silicon (denoted here as a-Si:H)[28] initiated a lot of interest in developing the electronic properties of a-Si:H with reasonable carrier mobilities[29] as a potential PV material.[30] Its semiconducting properties, such as the existence of a bandgap and the presence of Urbach tail states (as a consequence of its atomic structural disorder), were observed around the same time.[31,32] The role of hydrogen in satisfying the valency of Si atoms and the formation of a stable interconnected Si-H ring structure was explained by Lewis et al[33] in 1974.
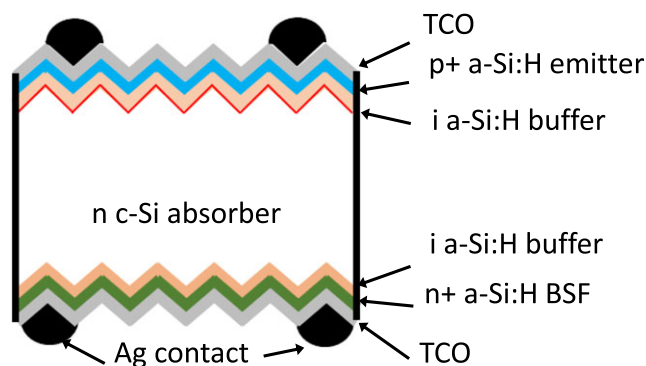
The photoconductivity of a-Si:H, as a consequence of its relatively low defect density, was also studied during this time.[34] A major milestone in the development of a-Si:H was the discovery of substitutional doping[35] in 1975. The n-doped (p-doped) a-Si:H was developed by the addition of phosphine (diborane) to the silane gas. Research on a-Si:H for PV device applications was started by RCA laboratories with initial solar cell efficiencies of 2% to 3%, which reached 11% to 12% by[36] 1989. The first commercial application of a-Si:H solar cells was developed by Sanyo in 1979 for hand-held calculator applications.[37] The limited efficiency gains over the years for a-Si:H p-i-n cell stunted the growth of this technology. Nevertheless, the development of doped a-Si:H technology was proven to be crucial to the development of SHJ cells.

The first proof of passivation of silicon wafers with atomic hydrogen, contained in a-Si:H, was reported[38] in 1978. The first solar cell using an SHJ consisted of a-Si:H/poly-Si heterojunction bottom cell in a tandem junction solar cell; this Honeymoon cell was patented[39] in 1985. In the late 1980s, Sanyo's research division (now owned by Panasonic Inc) incorporated a-Si:H as a junction-formation material for c-Si wafers. They patented their hybrid design of a-Si/c-Si heterojunction (SHJ) solar cells under the trademark HIT (Hetero Intrinsic Thin layer)[9] in 1991. The schematic of a bifacial SHJ cell is shown in Figure 2. It contains a c-Si wafer sandwiched between a-Si:H layers. The a-Si:H layers consist of a stack of intrinsic and doped a-Si:H material. The intrinsic a-Si:H layers (5 nm) are used to passivate the c-Si surfaces. The p^+ layer forms the hole contact (7-12 nm) and the n + a-Si:H layer (10-20 nm) forms the electron contact. Typically, SHJ cells with n-type wafers have higher efficiencies than those fabricated using p-type wafers due to the better chemical passivation of n-type c-Si surfaces with a-Si:H,[40] compared to p-type c-Si, and to the better inherent electronic bulk quality of n-type materials, compared to that of p-type materials.

Sanyo and other groups have reported several advantages of the SHJ design over the traditional c-Si design, including the following: (1) The deposited a-Si:H layers require processing temperatures of less than 200°C, compared to up to ~1000°C for the traditional diffused c-Si technology; (2) SHJ devices have a lower temperature coefficient compared to c-Si cell technology, which is of extreme importance in actual operating conditions[41]; (3) the record cell efficiencies for SHJ cells are higher than for diffused junction c-Si cells; and (4) due to symmetry of the cell design, the SHJ technology offers potential to be used in the bifacial mode.[42-45] In addition, the fabrication of SHJ cells takes advantage of well established, industrially scalable, thin-film deposition technologies.[46] Owing to all these advantages, SHJ solar cells are an attractive, high-efficiency alternative to traditional c-Si based solar cells, which typically have lower efficiencies.

There are, however, several challenges that the SHJ technology faces in comparison to the traditional c-Si–based homojunction technology, including the following: (1) SHJ are built on n-type c-Si wafers, although n-type silicon ingots have greater spread in their resistivity, compared to p-type ingots; (2) the need for a transparent conductive oxide (TCO) (typically indium tin oxide [ITO]) on both the front and back surface of the SHJ solar cell to collect the carriers increases the material cost—alternative transparent electrodes are actively being explored[47]; (3) the deposition of the very thin a-Si:H layers make the

technology sensitive to process variation; and (4) due to the limited annealing resilience of a-Si:H, sintering of the contacting metals is not possible, possibly requiring higher metal consumption per generated Watt of PV power in the case of screen-printed metallization,[48] unless alternative methods are developed such as multiwire approaches.

By the mid-2000s, Sanyo had improved the efficiencies of SHJ solar cells, reaching 20%, and developed the first commercial SHJ solar cell module.[42,49-55] Following the expiration of the patent in 2011, research activity on understanding the electronic and photoconductive properties of a-Si:H/c-Si SHJ solar cells by groups around the world increased markedly.[56] With the standard and IBC designs exceeding 25% efficiency in large-area devices[46-48] and the relative insensitivity of the output power to actual operating conditions, such as temperature,[51,57] SHJ technology indeed appears to be on the right trajectory for large-scale adoption by the PV industry. In addition, improvements, such as the use of new electron and hole transport layers,[15,16] TCO materials,[58] c-Si surface engineering,[59] bifacial configuration,[42,43] IBC configuration,[2,10,60,61] local SHJ contacts,[62] SHJ-based tandems,[63-66] and bifacial tandem configurations,[44] have all been proposed, attesting for the design flexibility of this device platform. In fact, the current efficiency record stands at 26.63%, achieved by Kaneka, Japan, with the IBC configuration.[2] Exploiting thin-film deposition properties, simplifications to such relatively complex design have been proposed.[67] As of today, this technology is poised to be one of the few commercially viable silicon-based solar cell technologies[68] and is actively being developed by several companies, including Panasonic, Sharp, Kaneka, CIC, Neo Solar Power, Hyundai, Meyer Burger, Sunpreme, and Silevo (now owned by Solar City, Tesla).

2 | STATUS OF HIGH EFFICIENCY SHJ CELLS

2.1 | Processing of modern SHJ cells

2.1.1 | Wafer preparation

Good quality, CZ/FZ-grown c-Si wafers with at least ~1-millisecond carrier lifetimes are used in the manufacturing of SHJ cells. Alkaline etchants, such as NaOH, KOH, or $(CH_3)_4NOH$, texture the (100) surface of the wafer to form so-called random pyramids of 3 to 7 micrometers height.[69] This is followed by wafer cleaning using sequential silicon-surface oxidation and oxide stripping with dilute HF solutions.

2.1.2 | Amorphous silicon deposition

The next step is to deposit an intrinsic a-Si:H passivation layer, typically through Plasma enhanced chemical vapor deposition (PECVD) or hot-wire chemical vapor deposition (CVD).[53,70-72] To this end, silane (SiH_4) gas, often diluted with H_2, is used as a precursor. The deposition temperature and pressure are maintained at about 200°C and 0.1 to 1 Torr, respectively. Precise control over this step is mandatory to avoid the formation of defective epitaxial Si.[71,73,74] Cycles of deposition and annealing and/or intermittent H_2 plasma treatments have been shown to provide excellent surface passivation, which may also improve light-induced degradation (LID) of such *intrinsic* buffer

layers.[75-78] Furthermore, studies of LID of intrinsic a-Si:H layers on c-Si wafers indicate that the annealed samples may exhibit a reversible Staebler-Wronski effect.[79,80] Next, diborane or trimethylboron gas mixed with SiH_4 is used to deposit a p-type a-Si:H layer while phosphine gas mixed with SiH_4 is used to deposit an n-type a-Si:H layer. It should be noted that direct deposition of doped a-Si:H layers on c-Si wafers has been shown to have very poor passivation properties.[9] This is most likely due to dopant-induced defect generation in a-Si:H layers.[81] Remarkably, such stacked films, featuring a doped layer, lead to improved passivation upon extended light soaking,[82] resulting in improved efficiencies of finalized devices.[83]

2.1.3 | Contact formation

Sputtered ITO is commonly used as a TCO layer on top of the front and back a-Si:H layers in bifacial designs because the lateral resistance of doped a-Si:H is too high. In more recent years, new transparent electrodes, aimed at an improved transparency-conductivity trade-off and replacement of indium by less scarce materials, have been actively studied.[47] Even in monofacial designs, TCO is generally deposited on the back side to avoid diffusion/spiking of the back metal through the contact stack and for improved light coupling in the wafer.[84-86] A silver grid with 50- to 100-micrometer-wide fingers is deposited through screen printing for the front and back contact in bifacial design. A detailed description of the fabrication process can be found in Ballif et al.[56]

2.2 | Bottlenecks in energy production of SHJ cells: a qualitative discussion

2.2.1 | Optical losses in the passivation layers—impact on J_{SC}

An important design requirement in heterojunction solar cells is to find a wide-band-gap carrier-collecting contact at the front side to minimize parasitic absorption. Towards this goal, a CdS layer is used in CIGS, CZTS, and CdTe solar cells. In SHJ cells, thin a-Si:H layers are used, which, despite having a slightly wider bandgap than the c-Si absorber underneath, can lead to significant parasitic light absorption and to reduced J_{SC} in the cells (see Figure 3). An important reason for this is the highly defective nature of the p^+ a-Si:H layer. Figure 4A shows that the a-Si:H layer absorbs a significant fraction of short wavelength photons, which are mostly lost to recombination and accounting for J_{SC} loss[87] of up to 2.1 mA·cm^{-2}. An additional 0.5 mA·cm^{-2} at higher wavelengths is lost to parasitic absorption in the overlying ITO layer. Moreover, achieving sufficiently low contact resistivity between the transparent electrode and the underlying a-Si:H layer has been a significant process challenge, mainly because of the limited dopant activation in a-Si:H, which can be remedied by using doped nano-crystalline Si films, also deposited by PECVD.[88] Recent design/material development efforts to alleviate the J_{SC} bottleneck are discussed in Section 6.

2.2.2 | Charge collection losses in the absorption layers—impact on V_{OC} and FF

Photo-generated carriers must be collected at the appropriate contacts to contribute to the photo-current (J_{Pho}). Before the charges are collected by the contacts, however, a fraction of the photo-
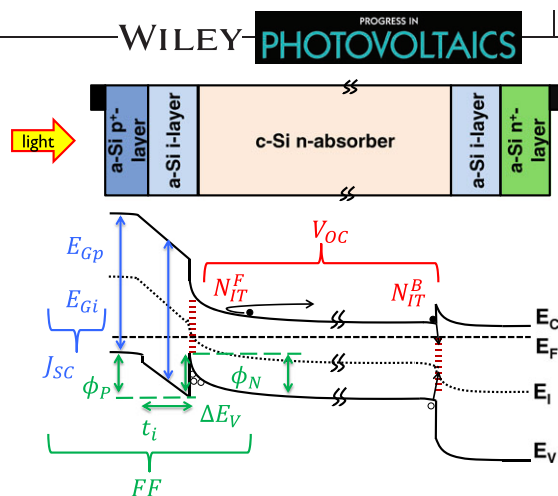

FIGURE 3 An equilibrium energy band diagram illustrating the device parameters necessary for accurately predicting the performance of SHJ cells. E_{Gp}, E_{Gi} are bandgaps of p- and i- a-Si:H layers, ϕ_P and ϕ_N are the band-bendings in the front a-Si:H layer and the absorber regions of the junction, ΔE_V is valence band offset at a-Si/c-Si interface, t_i is i-layer thickness, N_{IT}^F and N_{IT}^B are interface defect densities at front and back a-Si/c-Si interfaces [Colour figure can be viewed at wileyonlinelibrary.com]

generated carriers may be lost through radiative and nonradiative recombination processes, which in turn significantly reduce V_{OC}. Hence, it is important to quantify these collection loss mechanisms for design and process optimization. As shown in Figure 3, there are 5 process-specific parameters that dictate carrier loss in SHJ cells: (1) the thickness of the intrinsic a-Si:H layer (t_i); (2) p-layer doping (N_A); (3) intrinsic a-Si:H/n-doped c-Si valence band discontinuity (ΔE_V); (4) interface defect density (N_{IT}^F); and (5) absorber doping (N_D). The corresponding collection losses can be divided into two groups: (1) *recombination losses* (related to N_{IT}), which impact the operating voltage and V_{OC} and (b) *heterojunction losses* (influenced by ΔE_V, t_i, ϕ_P, and ϕ_N), which impact the FF. We briefly discuss these two types of losses below.

2.2.3 | Bulk and interface recombination losses impact V_{OC}

The dominant recombination mechanism in most c-Si cells is through deep level defects (usually called Shockley-Read-Hall [SRH] recombination). Radiative recombination is negligible because c-Si is an indirect band-gap material. As a consequence, in thin and high-quality wafers with good interface passivation, Auger recombination can become significant even at the 1-sun condition.[11] The SRH recombination loss in the device can occur in (1) the distinct bulk regions present in the device, which are doped a-Si:H, intrinsic a-Si:H regions, and the c-Si absorber, (2) the a-Si:H/c-Si interface regions, and/or (3) the transparent electrodes.

Under V_{OC} conditions, for the photogenerated carriers in c-Si, the recombination in the a-Si:H regions and the contacts contribute[89] to less than 1% of the total recombination loss within the entire device. This is because the a-Si:H layers at the front and back act as effective minority carrier reflectors, thereby significantly reducing the recombination at the contacts. As high-quality c-Si wafers produced through CZ or FZ processes have very long bulk lifetimes (τ) of about ~ 1 to
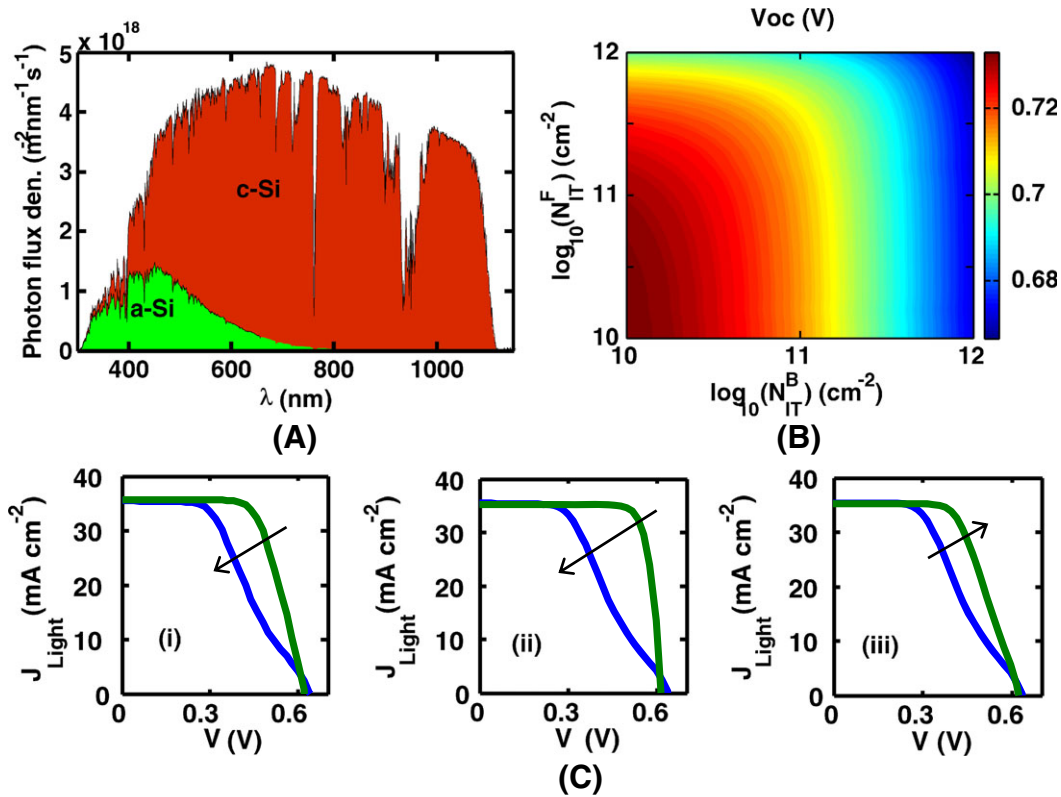
FIGURE 4 A, The photon flux density in the AM1.5G spectrum absorbed in a-Si:H regions at the front and the c-Si absorber. B, Simulated V_{OC} contour plot as a function of front (N_{IT}^F) and back (N_{IT}^B) interface defect densities. C, The influence of (i) t_i, varied from 5 to 20 nm (ii) ΔE_V, varied from 0.37 to 0.47 eV (iii) ϕ_P, where p-layer doping (N_A) is varied from 2 × 10^{18} to 10^{19}, on FF of typical SHJ cell light J-V characteristics[107] [Colour figure can be viewed at wileyonlinelibrary.com]

10 milliseconds, thus the major recombination losses in SHJ devices are limited to the front and back interface regions.

Very low V_{OC} values of devices can often be attributed to the undesired presence of a defective epitaxial layer formed during the deposition of intrinsic a-Si:H layers.[71,73,74] This can be remedied by developing a-Si:H deposition procedures aimed at an atomically sharp a-Si:H/c-Si interface.[90,91]

In theory, for the standard SHJ design with hole collection at the front, V_{OC} should be more sensitive to the back interface as compared to the front interface (see Figure 4B) (N_{IT}^F vs. N_{IT}^B). This is because the (p) a-Si:H/(i)a-Si:H/(n)c-Si junction electric field at the front interface repels one type of carrier (electrons in this case) thus creating field-effect passivation (see Figure 3). However, at the back interface, the (n)c-Si/(i)a-Si:H/(n)a-Si:H junction electric field is typically not strong enough to repel the carriers as effectively, which could lead to higher interface recombination.[89] In practice, however, p-type a-Si:H is always much more defective than n-type a-Si:H. This is because the (intrinsic) defect-formation energy is much lower when the Fermi-level shifts towards the valence band. This effect is so strong that it can even induce defects into the buffer layer and the front interface.[92,93] As a result, despite the electrostatic passivation, the front interface may still have higher recombination compared to the back interface. It is of note that the overlaying TCO layers can further alter the passivation of the contact stacks.[94]

In solar cells, a higher open circuit voltage (V_{OC}) can be obtained by confining the active carrier generation region (absorber) to smaller volumes, provided the surface recombination is negligible. Although this is true with any solar cell technology, it is a particularly attractive technique for increasing the V_{OC} of SHJ cells due to very effective surface passivation. With effective light trapping techniques, it is possible to minimize the loss of photon absorption (especially the in red part of the spectrum) and avoid any significant reduction in J_{SC}.[50] Thus, for a given base lifetime and interface trap density, reducing the base thickness is an effective way to boost the efficiency of SHJ solar cells. For very small absorber thicknesses (<60 μm), however, it is observed that Auger recombination starts to dominate over the other recombination mechanisms.[95]

2.2.4 | Front side, blocking layer losses impact the fill-factor

The presence of a heterojunction in a solar cell can affect the collection efficiency and thus the fill-factor (FF) in a significant way: Under operating conditions, the hetero-interface can act as a barrier for the photo-generated carriers (holes) to be collected at the front contact. The influence of key device parameters that affect the carrier collection and hence the FF are presented (Figure 4C). In Section 3.1, we discuss transport across the heterojunction to understand the origin of S-shaped J-V characteristics in greater detail; for now, we discuss the effects qualitatively.

In n-type SHJ cells, a large ΔE_V supports significant hole inversion charges close to the interface, resulting in field effect a-Si:H/c-Si passivation and thus improving V_{OC}. On the other hand, a large ΔE_V

impedes carrier collection and reduces FF. There is an optimum band offset of ~ 0.45 eV that provides an optimum V_{OC} and FF. On the other hand, in p-type SHJ cells, relatively smaller ΔE_C cannot support significant electron inversion charges close to the interface, resulting in poor field-effect a-Si:H/c-Si passivation and thus lower V_{OC}.

To summarize, the device parameter-dependent bottlenecks in SHJ cell include (1) the front a-Si:H properties, especially the bandgap and absorption coefficients that control the J_{SC}; (2) The interface defect densities and absorber lifetime that control the V_{OC}; and (3) the heterojunction ΔE_V, t_i, ϕ_P, and ϕ_N that control the FF.

Given the complex process of charge collection, optimizing industrial-grade SHJ cells is nontrivial because even small variations in these device-related parameters may lead to dramatic differences in performance. A detailed study of the influence of these variables is essential to pinpoint the origin of the efficiency gap and optimize the design and process cycles. Such a study could involve significant resources if approached on a trial-and-error basis. For this reason, an alternative, physically grounded approach is necessary to address this issue and propose design and manufacturing guidelines to achieve the highest possible power output from a given SHJ cell. Therefore, we offer a quantitative discussion of the physics of charge collection, and capture the mechanisms through a compact model formulation in the following section.

3 | THE PHYSICS OF CARRIER COLLECTION ENCAPSULATED IN A COMPACT MODEL

As discussed in Section 2, an SHJ cell is a complex multilayer device. Improving the performance of SHJ cells first requires understanding of the various layers before bottlenecks are identified and the technology limits can be resolved. Towards this goal, it is instructive to model a solar cell using simple circuit elements and then to see how an SHJ cell differs from diffused homojunction solar cells.

3.1 | Validity of superposition principle

A typical circuit representation of a solar cell is presented in (Figure 5 A). The circuit can be divided into *intrinsic* and *extrinsic* components as shown. The *intrinsic* total current under illumination (J_{Tot}) is given by the algebraic sum of two currents given by J_{Pho} and J_{Diode}. J_{Pho} is the current density due to the photo-generated carriers, and J_{Diode} is the total current density due to diode-injected carriers. In general, J_{Pho}

and J_{Diode} are functions of the photo-generation rate (G), bias (V), and temperature (T). Thus, we can write

$$J_{Tot}(G, V, T) = J_{Pho}(G, V, T) - J_{Diode}(G, V, T). \quad (1)$$

For a typical diffused homojunction (c-Si) solar cell, which usually does not feature any carrier-transport barrier, it is possible to simplify (1) by using the "principle of superposition,"[96,97] which states that the total current of a solar cell can be obtained as a superposition of the photocurrent measured under short-circuit condition [$J_{Pho} = J_{SC}(G)$] and the dark J-V characteristics [$J_{Diode}=J_{Dark}(V, T)$] (see Figure 5B). Thus, (1) simplifies to a more familiar expression, namely,

$$J_{Tot}(G, V, T) = J_{SC}(G) - J_{Dark}(V, T). \quad (2)$$

Using the diode equation for dark current, we can rewrite (2) as

$$J_{Tot}(G, V, T) = J_{SC}(G) - J_0(T)\left(e^{qV/k_B T} - 1\right), \quad (3)$$

where the symbols have their usual meaning.

Notably, the assumptions that lead to (2) and (3) are generally not valid for SHJ solar cells. Hence, it is not possible to model a SHJ solar cell using (2) or, equivalently, the compact model in Figure 5B. To overcome this challenge, a numerical approach to study J_{Dark} and J_{Tot} must be adopted. Furthermore, J_{Tot} involves two components, J_{Pho} and J_{Diode} (see (1)), which need to be analyzed separately.[98] Detailed analysis of these current components was carried out in.[98-100] In the following section, we see that the circuit in Figure 5C works very well to explain SHJ cell transport. In addition, we quantify the components of the current using physical and intuitive analytical models.

3.2 | The physics of dark and light J-V

3.2.1 | High ideality factors in dark J-V

Once the shunt and series resistances have been accounted for,[99,101-103] the dark J-V of a typical SHJ cell is characterized by the current-saturation voltage, which occurs at the bias $V = V_1^{Dark}$ (see Figure 6A, C). In an experimental dark J-V, V_1^{Dark} is defined by the maximum of $d^2 \log(J_{Dark})/dV^2$ (see Figure 6A).[99] The origin of *dark current saturation* and *very high ideality factors* above $V = V_1^{Dark}$ is discussed in previous works.[99,105] Briefly, at $V = V_1^{Dark}$, the top of the a-Si:H valence band at the interface aligns with the c-Si valence band at the depletion edge (see Figure 6E). Under this condition, the magnitude of the diode current injected from the front contact into the c-Si region is

FIGURE 5 A, A typical circuit representation of a solar cell. B, A simplified circuit representation of the intrinsic components of a p-n homojunction solar cell. C, An accurate circuit representation of an SHJ solar cell.[111] SHJ, silicon heterojunction [Colour figure can be viewed at wileyonlinelibrary.com]
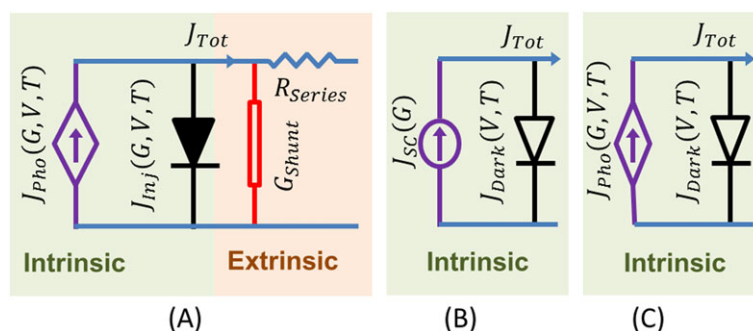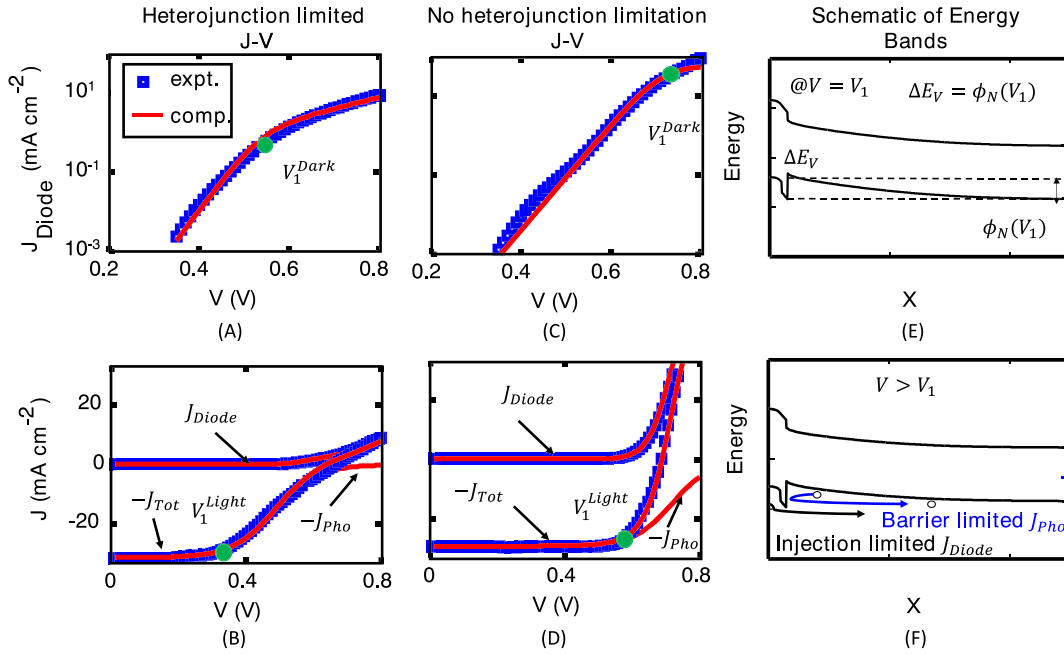
FIGURE 6 The J_{Diode} obtained from experiments ($\square$) and the compact model ($-$), indicating the current saturation at V_1^{Dark} (marked in green) for A, voltages>0.5V for low-quality samples and C, >0.7V for high-quality samples.[104,107] The corresponding J_{Pho} also indicates the expected shift in the rollover voltage at V_1^{Light} (marked in green) for B, low- and D, high-quality samples. E, At $V = V_1$, the energy band diagram shows that the top of the valence band in a-Si aligns with that of the c-Si valence band. F, For $V > V_1$, J_{Diode} is injection limited and hence saturates and J_{Pho} is barrier limited and hence drops. See Chavali et al[99] for details [Colour figure can be viewed at wileyonlinelibrary.com]

dictated by the height of the a-Si:H valence band spike observed from the front contact (see Figure 6F). As the bending in a-Si:H does not change significantly with applied bias (due to the presence of the inversion charge at the interface[106,107]), the carrier injection also does not change significantly. Hence, the injected diode (dark) current saturates with respect to the applied bias. However, in *good* devices with higher p-layer doping, V_1^{Dark} occurs at much higher applied bias (see Figure 6C), and the J-V behaves as if the heterojunction were absent.

One can capture the essential physics of heterojunction transport under dark conditions using a simple analytical model developed from thermionic emission-diffusion theory (see [107] for a full analysis). Assuming that the generation dependence of the diode current is negligible [$J_{Diode}(V) = J_{Dark}$],[99] the diode current is given by the following:

$$J_{Diode} = q \frac{n_{ic}^2}{N_D} \left(\frac{1}{s_{fd}^{-1} + s_D^{-1}} \right) \left(e^{qV/k_BT} - 1 \right). \quad (4)$$

Here, n_{ic} is the intrinsic carrier concentration in the absorber layer, $s_{fd} = s_o e^{-(\Delta E_V - \phi_{Nd})/k_bT}$ is the emission-diffusion velocity in a-Si:H under dark, where $\phi_{Nd} = (\phi_{Nd}(V = 0) - \beta_d V)$, β_d is a fraction of the voltage drop in the c-Si depletion region under dark conditions, and ϕ_{Nd} is the electrostatic potential in the c-Si depletion region under dark conditions (the subscript "d" stands for dark) and s_D is minority carrier bulk diffusion velocity. Intuitively, (4) indicates that the smaller of the two velocities (s_{fd}, s_D) defines the rate-limiting factor and dictates the magnitude of J_{Diode}. The analytical model fits to experimental data are reproduced from Chavali et al[108] and are shown in Figure 6A-D.

3.2.2 | The physical origin of S-shaped light J-V characteristics

The superposition principle does not always hold for heterojunction cells.[99] Under the light J-V conditions in Figure 6B, we observe that the *S-type rollover close to the maximum power point* is correlated with the *current saturation under dark J-V conditions*.[99] Briefly, this is due to rollover of J_{Pho}, which occurs at $V_{Bias} = V_1^{Light}$, when the top of the a-Si:H valence band at the interface aligns with the c-Si valence band at the depletion edge *under illumination conditions* (see Figure 6D). The rollover starts to occur when the photo-generated holes observe a barrier due to ΔE_V above V_1^{Light} (see Figure 6F). However, in *good* devices with higher p-layer doping, V_1^{Light} occurs at much higher voltage (see Figure 6D) and does not limit the light J-V response.

These V_1^{light} in light J-V and V_1^{Dark} in dark J-V and C-V (discussed later in Section 4.2) may occur at the same bias *if* the photo-generated carriers do not significantly change the electrostatic potential under illumination as compared to under dark conditions.[99] However, these values can be significantly different and the correlations between V_1^{light} and V_1^{Dark} and thus the light and dark J-V need to be analyzed using the "frozen potential technique" (see other works[99,100] for details).

One can use the thermionic emission-diffusion theory[109,110] to capture carrier transport across the heterojunction under illumination in an analytical form as follows:

$$J_{pho} \cong q N_{cSi} \left(\frac{s_D^{-1} + s_b^{-1}}{s_{fl}^{-1} + s_D^{-1} + s_b^{-1}} \right), \quad (5)$$

where N_{cSi} is the effective rate of carriers generated per unit area inside the quasi-neutral region of c-Si, dependent on the p-doped and intrinsic a-Si:H layer thicknesses (t_p, t_i), the c-Si quasi-neutral region width (W_c) and the corresponding attenuation coefficients (k); s_b is the surface recombination velocity at the back interface; and s_D is the diffusion velocity in the c-Si quasi-neutral region given by $s_D = D_h \left(\frac{1}{W_c} + \frac{1}{L_h} \right)$, where D_h is the diffusion coefficient for holes and L_h is the hole diffusion length in c-Si. The s_{fl} is the emission-diffusion velocity in a-Si:H under light, given by $s_{fl} = s_o e^{-(\Delta E_V - \phi_{Nl})/k_b T}$ and $\phi_{Nl} = (\phi_{Nl}(V = 0) - \beta_l V)$, β_l is the fraction of the voltage drop in the c-Si region under illumination and ϕ_{Nl} is the electrostatic potential in the c-Si depletion region under illumination (subscript "l" stands for light) (see ϕ_N in Figure 3). Intuitively, (5) indicates that the smallest of s_{fl}, s_D, or s_b is the rate-limiting factor, dictating the magnitude of J_{Pho}. The total current (J_{Tot}) is given by the sum of the diode and photo current, as shown in (1).

3.3 | Impact of temperature and intensity on collection of photogenerated carriers

The experimental normalized light J-V curves under different intensity (I, suns) and temperature (T) conditions obtained from Chavali et al[111] are presented in Figure 7A,B. Firstly, at a given T (say 101 K; see Figure 7A), increasing I causes early onset of the S-shaped curve. Secondly, for a given I (say 0.4 Sun, Figure 7B), increasing T eliminates the S-shaped curve. These trends indicate the opposite effects of T and I.

Once again, we can understand these curves from the energy barrier perspective (Figure 6E-F) discussed earlier in Section 3.2. Increasing the intensity increases the carrier concentration, reducing the surface potential, introducing a hole collection barrier, and causing

S-shaped J-V. At lower temperatures, a larger fraction of the photo-generated carriers cannot cross the heterojunction barrier, causing a "carrier pile-up" near the junction, reducing ϕ_N, introducing a hole collection barrier, and, consequently, causing an S-shaped J-V characteristics. To summarize, we find that early onset of the S-shaped J-V may be triggered by higher I, lower T, or both.

3.3.1 | Suns-V$_{oc}$ vs suns-photovoltage characteristics

Using the J-V characteristics, we can construct Suns-photovoltage curves for different T and at different current densities (see Figure 7 C-F). For example, to obtain the blue curve in Figure 7C (at $T = 101$ K), we read the voltage (V) at $J = -0.9J_{SC}$ for each I from Figure 7A (for $T = 101$ K) and plot it against the corresponding I. Here, the Suns-photovoltage curves at $J = -0.9J_{SC}$, $J = -0.5J_{SC}$, $J = -0.1J_{SC}$, $J = 0$ (ie, at V_{oc}) in Figure 7C-F are systematically analyzed. The effects of I, V, and T on the Suns-photovoltage curves elucidate the operating conditions under which the superposition principle fails.

In Figure 7C (plotted at $J = -0.9J_{SC}$) for low intensities, the photovoltage is dictated by the splitting of the quasi Fermi-levels, and the device obeys the superposition principle (ie, Equation 1) and the photovoltage increases logarithmically with intensity, as expected. However, for higher intensities, the photovoltage begins to reduce, and the curve turns around unexpectedly. Under these conditions, junction electrostatics and thus ϕ_N dictate the device characteristics.[111] In addition, considering the full data set given in Figure 7C-F, we see that the turnaround is stronger at higher current densities ($J = -0.9J_{SC}$, Figure 7C), while it becomes weaker close to open circuit conditions (see Figure 7F).[94]

In essence, the experimental observation of the turnaround in Suns-V$_{oc}$ is a direct consequence of the carrier emission over the heterojunction barrier, which is strongly influenced by the illumination
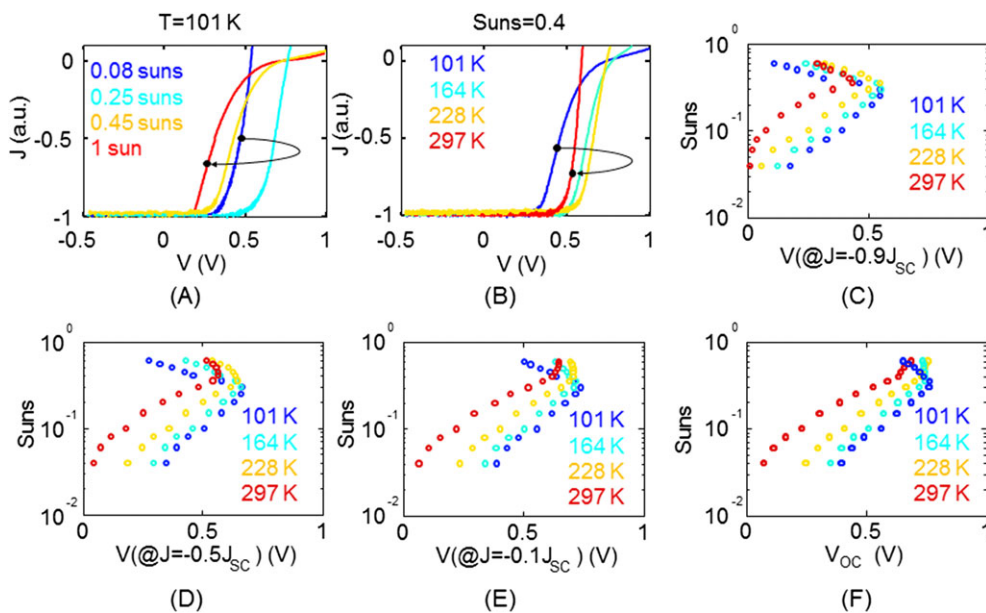
FIGURE 7 The experimental normalized J-V characteristics of an SHJ cell for different A, intensity conditions at $T = 101$ K and B, temperature conditions at Suns = 0.4. Experimental Suns-photovoltage curves for a standard SHJ cell at different temperatures and $J = -0.9J_{SC}$, $J = -0.5J_{SC}$, $J = -0.1J_{SC}$, and V_{OC} conditions ($J = 0$) are plotted in C, D, E, and F, respectively[111] [Colour figure can be viewed at wileyonlinelibrary.com]

intensity, temperature and bias conditions. Thus, in a good SHJ device, while the turnaround may be present at lower temperatures, it will disappear under actual operation conditions.

In addition to the influence of a-Si:H/c-Si heterobarrier, Schottky contacts[112] can also contribute to the turnaround in Suns-V_{oc} curves. Hence, one needs to be cautious about inferring the presence/absence of a Schottky barrier or a heterojunction simply based on Suns-V_{oc} measurement. When analyzed self-consistently with other techniques, such as dark J-V-T,[99,113] C-V,[107] admittance spectroscopy[107,114] (discussed next in Section 4], and surface-photovoltage,[115] we can infer the presence/absence of Schottky contacts for a specific process technology and recommend effective strategies for process improvement. In the following section, we describe such a self-consistent approach known as a "multiprobe approach" to *parameterize* the influence of the heterojunction on these SHJ cells.

4 | MULTIPROBE CHARACTERIZATION

In the previous sections, we demonstrated that the performance of SHJ cells can be predicted once the physical parameters are specified. It is therefore important to define the parameters through self-consistent characterization.

4.1 | Need for multiprobe characterization

In Section 2.2, we discussed that a heterojunction significantly affects the charge-collection efficiency of the cell and this heterojunction-limited charge collection depends on five device parameters (see Figure 3). Furthermore, Equations 4 and 5 in Section 3 allow us to deduce the 5 heterojunction-related parameters that affect the collection efficiency, including (1) the thickness of the intrinsic a-Si:H layer (t_i) through N_{cSi}, s_o; (2) p-layer doping (N_A) through β; (3) intrinsic a-Si:H/n-doped 7c-Si valence band discontinuity (ΔE_V) through s_{fd} and s_{fi}; (4) interface defect density (N_{IT}^F) through s_o, s_b; and (5) absorber doping (N_D) through ϕ_{NI}.

It is important to evaluate these parameters individually because each parameter is controlled by different processing steps, and the failure to optimize them collectively could reduce cell efficiency. For example, the deposition times of the a-Si:H layers control the p-layer thickness (t_p) and the i-layer thickness (t_i).[9,116,117] ΔE_V and N_{IT}^F are controlled by precisely controlling the a-Si:H process parameters[42,73,118,119] and the post-deposition treatment.[75-78]

If we use only traditional single-temperature dark J-V or single-intensity light J-V to characterize a SHJ cell,[107] it would be impossible to uniquely extract the 5 parameters listed above. This is because many of these parameters affect the terminal characteristics in a similar way (eg, changing any of t_i, ΔE_V, and N_A produce a very similar S-type light J-V in Figure 5B). In other words, we observe many-to-many mapping between a measured quantity (J-V) and a key heterojunction parameter that makes the parameter extraction process impossible. Hence, independent characterization of the 5 key parameters is crucial for process optimization of SHJ solar cells. In this section, we describe a set of quasi-orthogonal capacitance-based characterization techniques that can extract the parameters self-consistently[88]

(see Figure 8). Specifically, the goal of this section is to explain the following equations needed for key parameter extraction:

$$t_i^* \cong \epsilon \left(C_{hf}^{-1} - C_{lf}^{-1} \right), \tag{6a}$$

$$\phi_P \cong E_A^{eff}, \tag{6b}$$

$$\Delta E_V = V_{bi}^{hf} - V_1^{Dark}, \tag{6c}$$

$$\phi_N^0 = V_{bi}^{hf}, \tag{6d}$$

$$N_D \sim \frac{1}{d\left(1/C_{hf}^2 \right)/dV}. \tag{6e}$$

The physics and extraction process are provided in Chavali et al.[107]

4.2 | Response of inversion charge (Q_{Inv})

Analysis of the small signal frequency, temperature, and applied bias response of the charge present at the inversion layer (Q_{Inv} at the a-Si:H/c-Si interface within the junction) can provide useful insights into the parameter extraction procedure. Consequently, we see that Q_{Inv} is responsible for several distinctive features observed in the charge and transport measurements. Using the response of Q_{Inv}, we can connect the junction-related parameters to the observed features in the characterization methods in a self-consistent manner, as summarized in (6).

4.2.1 | Frequency response of Q_{Inv} at the heterojunction

At low frequency (<f_c), the Q_{Inv} can respond to v_{ac} via transfer of holes from the hole contact to the inversion layer and vice versa.[107] Under these conditions, the differential inversion charge (ΔQ_{Inv}) responds with the differential space charge in c-Si (ΔQ_{c-Si}), at the c-Si depletion edge, as shown at the top Figure 9A. This effect can be measured as the low-frequency capacitance (C_{lf}) (see Figure 9A, bottom). However, at high frequency (>f_c), this transfer of holes between the hole contact and the inversion region is not fast enough to follow v_{ac}; hence, Q_{Inv} cannot respond (see Maslova et al[106] for details). Therefore, ΔQ_{c-Si} responds in the differential space charge region in the doped a-Si:H layer (ΔQ_{a-Si}). As shown in the top of Figure 9A, this effect can be measured as the high-frequency capacitance (C_{hf}).

Thus, C_{lf} (C_{hf}) is due to the low (high) frequency response of differential charges that are separated by W_{lf} (W_{hf}). The distance between W_{lf} and W_{hf} provides an estimate for intrinsic a-Si:H thickness (t_i^*) as given by $t_i^* = W_{hf} - W_{lf} = \epsilon \left(C_{hf}^{-1} - C_{lf}^{-1} \right)$, Equation 6a.

4.2.2 | Temperature response of Q_{Inv} at heterojunction

To understand the origin of the temperature-activated response of the fluxes that support Q_{Inv}, Chavali et al[107] studied J_{Int}, the response of interface defects; J_{c-Si}, the response of holes in the c-Si base; and J_{a-Si}, the response of holes in the a-Si:H. They found that the emission of holes from the p-doped a-Si:H into the inversion layer ($J_{a-Si}^{e \rightarrow i}$) is the
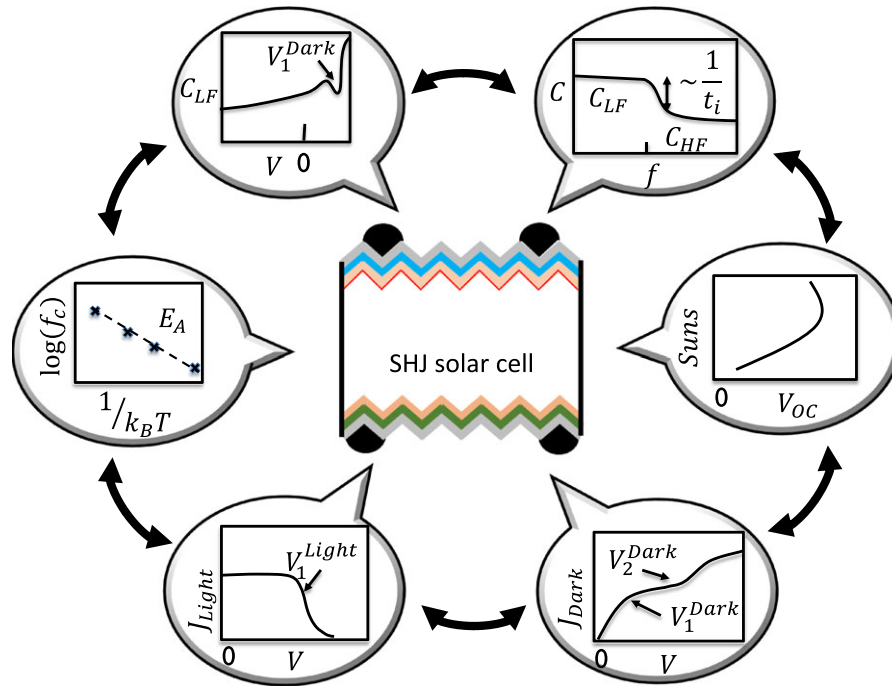
FIGURE 8 An array of quasi-orthogonal characterization methods are used to study the SHJ solar cell. SHJ, silicon heterojunction [Colour figure can be viewed at wileyonlinelibrary.com]

rate-limiting factor and dictates the activation energy observed through admittance spectroscopy (E_A^{eff}). This activation energy is strongly correlated with the total band bending in the a-Si:H region (ϕ_P) (see Figure 9B, top). Further, this observation also explains the anomalous voltage dependence of E_A^{eff}, which is consistent with the voltage dependence of ϕ_P (see Figure 9B, bottom).[114]

4.2.3 | Voltage response of Q_{Inv} at the heterojunction

In a classical p-n homojunction, as the applied bias increases, the voltage drop occurs partially across both p and n sides. In response to this voltage drop, most carriers on either side of the junction reach the corresponding depletion edge, thereby reducing the depletion widths on both side. This change in depletion with applied bias defines
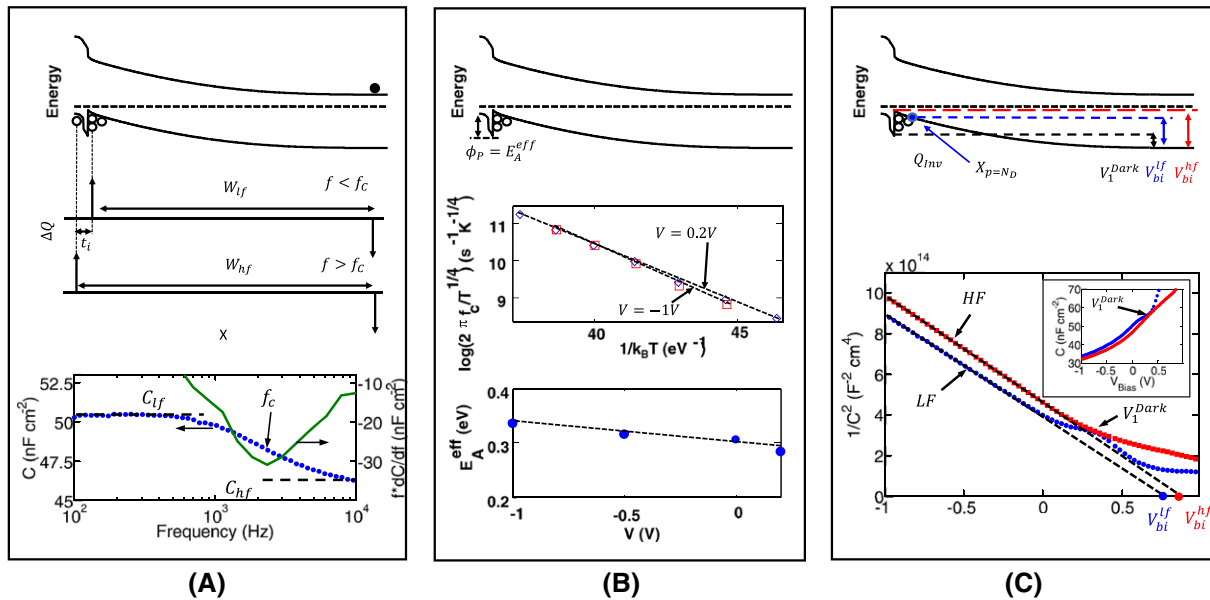
FIGURE 9 A, An equilibrium energy band diagram indicating the estimated t_i. The C-f characteristics indicate C_{lf} and C_{hf} and the cut-off frequency (f_C). B, The band diagram indicates that the activation energy from admittance spectroscopy measurements (E_A^{eff}) equals ϕ_P. The voltage-dependent admittance spectroscopy measurement indicates the voltage-dependent E_A^{eff}, consistent with the voltage dependence of ϕ_P. C, The Mott-Schottky analysis ($1/C^2$ vs V) provides an estimate for band-bending in the device useful for extracting ΔE_V. $X_{p=N_D}$ is the point in c-Si base where $p = N_D$. See Chavali et al[107] for a detailed discussion of these analyses [Colour figure can be viewed at wileyonlinelibrary.com]

the shape of the reverse bias C-V characteristics in the p-n junction. Traditionally, the reverse bias C-V characteristics are used in a Mott-Schottky analysis to calculate the intercept and slope of the *frequency-independent* $1/C^2$ vs V (Equation 6e). They are, respectively, correlated to V_{bi} and base doping (N_D).

However, in SHJ cells, the presence of Q_{Inv} at the heterojunction interface complicates the junction electrostatics. Indeed, the reverse bias C-V characteristics and hence the Mott-Schottky theory of the p-n junction cannot be directly applied to SHJ cell analysis.[107]

4.2.4 | Low-frequency C-V

Through detailed analysis of the electrostatic response of Q_{Inv}, it is found that the V_{bi}^{lf} estimated from the reverse-bias low-frequency $1/C^2$-V (for $f < f_C$) is essentially equal to the equilibrium band bending from the quasi-neutral c-Si base region to a point defined by $X_{p=N_D}$ in the c-Si region, where the hole concentration (p) is equal to base doping (N_D) (see Figure 9C).[107] Next, at $V = V_1^{Dark}$ (see the dark J-V discussion in Section 3.2), a "knee" is observed in the low-frequency ($f < f_C$) C-V (see Figure 9C, top). In other words, the saturation of dark J-V at V_1^{Dark} manifests as a knee in the low-frequency C-V. This correlated feature of dark J-V and C-V demonstrates the self-consistency of these two measurements.

4.2.5 | High frequency C-V

Furthermore, V_{bi}^{hf} estimated from the reverse bias high-frequency $1/C^2$-V (for $f > f_C$) is approximately equal to the equilibrium band bending in c-Si ($\phi_N^0 \approx V_{bi}^{hf}$), as shown in Figure 9C and Equation 6b. Also, the effective doping estimated from the high-frequency $1/C^2$-V curve using the Mott-Schottky analysis is N_D.

Once V_1^{Dark} and ϕ_N^0 are known from the low and high frequency C-V characteristics, we can estimate the band offset as follows (see Figure 9C, top): $\Delta E_V = \phi_N^0 - V_1^{Dark} = V_{bi}^{hf} - V_1^{Dark}$, see Equation 6c.

Thus, the multiprobe approach determines the 5 key parameters of an SHJ cell, provides deep insights into the device physics of SHJ cells, and is self-consistent with prior discussions on J-V characteristics. Once the cell performance is optimized by optimizing these parameters, we must ensure that the cell-level efficiency gain *translates to the module-level performance improvement*. This is the topic of discussion in the next section.

5 | CELL-TO-MODULE TRANSITION

Up to this point, our focus has been to understand cell-level performance. Now, we take a closer look at the implication of cell-level performance on the module power output. After all, the ultimate issue for commercial success of this technology is module performance, which involves careful considerations of all factors that can lead to potential losses at various stages of module production. This section is geared towards highlighting a comprehensive yet portable modeling framework for industry that can be useful for design optimization of the fabrication process flow of SHJ modules.

5.1 | Process-to-module modeling framework

The connection between key process, device, and module parameters can help to establish the ultimate performance limit and long-term commercial viability of a PV technology. Indeed, careful and self-consistent modeling and optimization at the process, device, and module levels can help to reduce the *cell-to-module efficiency gap* (Δ). Here, we define the idealized cell-to-module efficiency gap (Δ) as the *absolute* efficiency loss between two quantities: the idealized cell efficiency that can be achieved for optimized process conditions (excluding the series resistance and the shunt losses) vs the ultimate module efficiency (including the dead-area loss, etc) ready for deployment. With several SHJ companies ramping up their module production, a systematic approach to analyze the contributions to Δ is crucial to improving the module efficiencies to better than 20%.

Ideally, a compact modeling approach that captures the essential features of the process conditions, transport across the heterojunction, and module configuration offers an efficient way to establish the connection among the process, device, and module parameters, and thereby helps to specify the origin of Δ. A key contributor to Δ may be possible variations in a-Si:H film properties within/among the manufactured SHJ solar cells. The variation in a-Si:H film properties can be due to process variations in deposition pressure (P_p), temperature (T_p), plasma power density (W), $[B_2H_6]/[SiH_4]$ (R_g), and/or deposition time (t_{dep}) (see Figure 10A). These process variations lead to variation in material properties, such as the bandgap (E_G), average Fermi-level in doped a-Si:H ($\langle E_{fp} - E_V \rangle$), film thickness of i-layer (t_i) and p-layer (t_p), and attenuation coefficient (k). These variations in the material parameters dictate the variation in the diode (J_{Diode}) and photocurrent (J_{Pho}) characteristics of an individual cell (see (4) and (5)) and ultimately may affect the module efficiency (η).[108]

Specifically, in this section, we highlight the impact of correlations among (1) the key a-Si:H deposition parameters (P_p, T_p, W, R_g, t_{dep});(2) the *front* a-Si:H film parameters (E_G, E_{fp}, t_i, t_p, k); (3) the SHJ device characteristics (J_{Diode}, J_{Pho}); and (4) the module parameters (η, Δ). (4) The modeling approach involves (1) a semi-empirical process model along with its influence on the a-Si:H film properties; (2) establishing the influences of process parameters on the device performance using the physics-based SHJ device model presented in Section 3; and (3) using a SPICE-based circuit simulator to create a full module (Figure 10B) and study the influence of process/shunt parameters, resistance, dead area loss, and cell sorting on the cell-to-module efficiency gap. The detailed procedure followed in developing this framework is described in Chavali et al.[108] Here, we present the electrical aspects of the module; however, the module optics also requires careful attention to maximize the module efficiency.[2,120-122] Some of the optical aspects will be considered later in Section 5.3.

5.2 | The variation-induced cell-to-module efficiency gap (Δ)

An end-to-end framework allows us to predict Δ. Here, we summarize the capabilities of the framework using an example that highlights the importance of various factors, such as the dead area, a-Si:H process variation, shunt, and series resistance losses.[108]
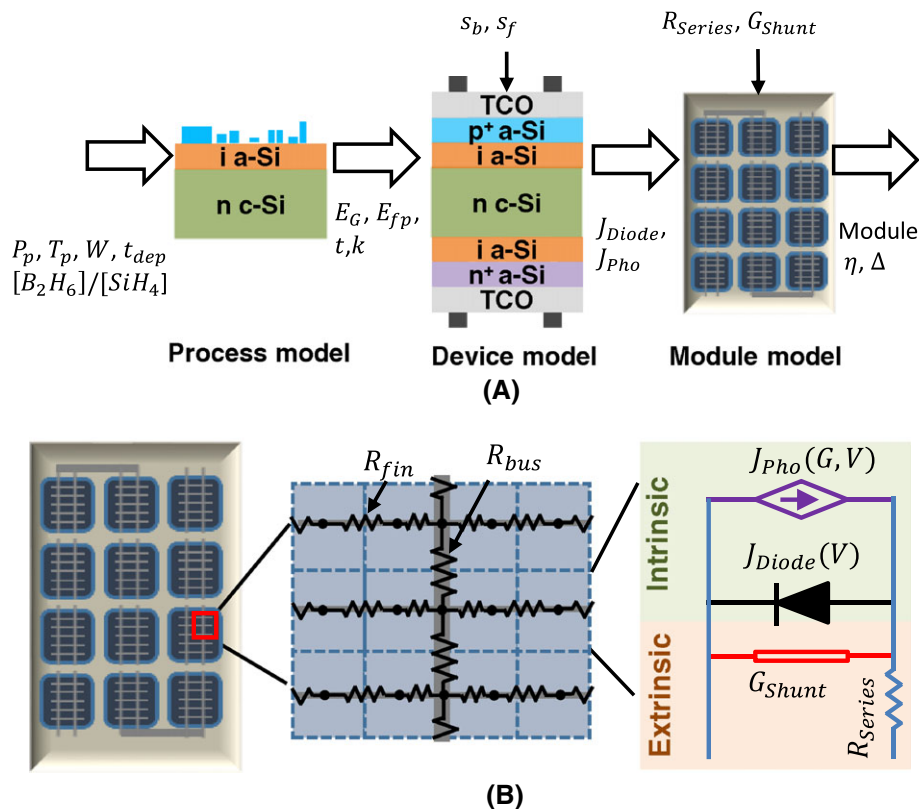
FIGURE 10 A, The end-to-end modeling framework for SHJ cells. B, Schematic of series-connected cells in the module. Subcells within a cell are connected with resistor elements to model the bus-bar (R_{bus}) and the finger (R_{fin}) resistances, whereas the subcell circuit within a cell models the intrinsic and extrinsic components.[108] SHJ, silicon heterojunction [Colour figure can be viewed at wileyonlinelibrary.com]

In this example, the idealized module efficiency is 22.6%. Once the dead area loss in included, the efficiency drops to 21.1%. Including series and shunt resistances further reduces the efficiency to 20.3%.

We can now study the additional losses due to process variations. The process variations are captured by σ, which is the percentage of deviation of each of the process parameters from its nominal value. A smaller σ indicates tighter process control. Figure 11A shows an example of cell-to-cell variation in the output power density of a module (with $\sigma = 10\%$) at its operating point ($V_{module} = 53$ V). The process parameter variation occurs at the cell level, and the microscopic shunt variation occurs at the subcell level. Furthermore, Figure 11B shows the contribution to Δ of various values of σ. As expected, with an increase in σ, the loss due to process variation becomes important. Around $\sigma \sim 12\%$, this loss starts to dominate over others. Binning/cell sorting/current matching strategies can effectively mitigate these variation-induced losses.[108]

This analysis indicates the obvious importance of process control in a large-scale industrial process line for fabrication of SHJ cells. Indeed, for the state-of-the-art commercial modules from Panasonic Inc, the typical cell efficiency[123] is ~22%, while the overall module efficiency is 18.5% for the 88-cell configuration[124] and 19.4% for the 72-cell configuration,[123] indicating that Δ is ~2.6% and ~3.5%, respectively. This suggests close-to-ideal process control for the 72-cell configuration. Similar performance characteristics were also observed in Meyer-Burger modules.[125] The framework discussed in this work can therefore

be useful to several other SHJ manufacturers attempting to quantify such losses to optimize their process flow and reduce Δ to ~2%.

## 5.3 | Other optimizations for a reduced cell-to-module gap

Innovation in module design has resulted in several promising approaches to reduce the cell-to-module efficiency gap.[126,127] Here, we briefly discuss some of the important module design approaches.

5.3.1 | Optimization of the module stack

Optical management through optimization of glass and cell encapsulant properties can significantly enhance the module's power gain. For example, improvements, such as the use of 2-mm anti-reflective coated solar glass rather than the typical 3.2-mm solar glass and/or the use of PVB (Polyvinyl butyral) polymer with better UV transmittance characteristics instead of EVA (Ethylene-vinyl acetate) for the cell encapsulant, reduce the relative module power loss by 4%.[120] Bifacial glass-glass modules may also be an approach to lower Δ.

5.3.2 | Optimization of inter-cell spaces and module borders

In a typical module, the dead area accounts for 7% of the total module area. As we have seen in Figure 11B, the dead area can cause significant power loss in a module. Strategies such as partial redirection of light that is reflected off the dead areas onto the solar cells can help
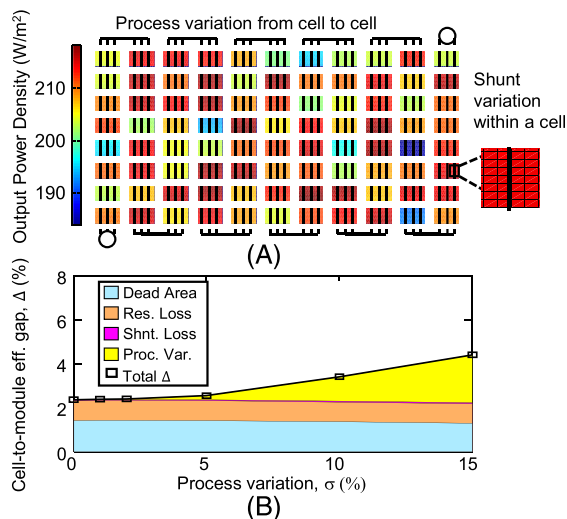
FIGURE 11 A, Module simulation (for σ = 10%) shows the output power density in each cell connected in a series configuration. The variation in cell-to-cell power output is due to process variations and variation within a cell (see the magnified cell) is due to shunt variation. B, The stack plot shows the contributions to the cell-to-module efficiency gap (Δ, absolute value)[108] [Colour figure can be viewed at wileyonlinelibrary.com]

improve J_{SC} and thus the output power. In fact, state-of-the-art white back sheets have demonstrated a power gain of 3% over the baseline case.[128] Strategies such as shingling of cells can dramatically reduce the dead-area between cells.

5.3.3 | Optimization of metal contact designs

Increasing the grid aspect ratio can reduce the front metal shading loss without introducing any additional series resistance losses. However, the use of high-aspect ratio grids can introduce significant mechanical stresses in the cells, increasing their susceptibility for breakage. A potential solution could be the use of circular cross section wires as contact grids. These wires reflect a significant portion of normally incident light into larger angles, causing a total internal reflection at the glass/encapsulant interface (see Meyer-Burger, smart-wire connection technology[129] for details). This reflected light can be absorbed by nearby cells, thereby improving the current densities. Cells with these wires are also less susceptible to breakage.[129] Such grid designs are currently being commercialized by Meyer-Burger. Finally, recent use of back-contacted cell technologies eliminates grid shading loss and may be responsible for the highest efficiency reported to date.[2,121]

5.3.4 | Optimization of electrical resistance

Reduction of I^2R losses can be achieved by either reducing R or I. Half-cell designs obtained through laser scribing and cleaving of full cells are proposed as an approach to reduce I by half and I^2R by three-quarters.[130] Two half cells connected in series replace every full cell in the proposed module design. Although there is some material loss due to laser scribing, the overall power gains through the use of half cells is found to be ~5%. It is significant that the reduction in the module-associated series resistance also favorably impacts the temperature coefficient of modules.[41]

6 | DISCUSSION AND OUTLOOK

6.1 | Reliability considerations for SHJ cells

As a c-Si-based technology, SHJ cells inherit a number of characteristic degradation mechanisms that possibly may affect all solar cell technologies. For example, corrosion, delamination, and discoloration can be concerns even in SHJ cells.

Unlike c-Si technologies that predominantly use p-type wafers, SHJ cells with n-type wafers do not exhibit significant LID. This contrasts with p-type wafers, where light-catalyzed boron-oxygen complexes act as recombination centers and reduce V_{OC}. The absence of boron in n-type wafer-based SHJ cell helps to eliminate the V_{OC} degradation with light exposure.[3] Furthermore, a-Si:H cells are well known to undergo LID through the Staebler-Wronski effect. Notably, whereas it has been shown that LID can cause some degradation of intrinsic a-Si/c-Si interface passivation structures,[131] it was recently found that, on the device level, SHJ cells actually improve their efficiency under light exposure.[82,83]

In addition, the option to use a bifacial design for SHJ cells introduces a significant constraint on the size of the junction box electronics to avoid any shading loss on the back-side insolation.[132] However, the small size of the junction box is subject to significant self-heating and is becoming a major concern in adopting bifacial SHJ cell designs.

Finally, a recent reliability study[133] based on 10-year-old field modules indicates that the efficiency degrades at a linearized rate of (0.67 ± 0.18) %/year, similar to that of classic silicon systems. A careful theoretical study ascribes the atypical V_{oc} loss to increased recombination at the front a-Si/c-Si interface, and the series resistance increase to TCO layer degradation and/or change in the a-Si/c-Si heterojunction discontinuity. Most likely, these trends can be traced back to early technology imperfections. We need more field data, especially of modules that benefitted from more recent processing sophistications, to definitively conclude that these degradation mechanisms are characteristics features of SHJ/passivated-contact solar cells or just typical early-technology imperfections of modules fabricated now already more than a decade ago.

6.2 | Emerging trends in passivation

We have seen in Section 2.2 that the maximum possible J_{SC} for a SHJ cell is about 43 mAcm^{-2}. For a realistic device, part of this potential current is lost due to parasitic absorption in the a-Si:H front layers and transparent electrode. In fact, these a-Si:H layers, if not well optimized, may reduce J_{SC} by 2.1 mAcm^{-2} through the absorption of sub-600 nm photons (see Figure 4A).[87] This J_{SC} loss can be avoided by using higher bandgap window layers that are transparent to the sub-600 nm part of the AM1.5G spectrum. Towards this goal, materials such as MoO_x and SiO_x are being developed to replace the doped and intrinsic a-Si:H layers, respectively.

Early reports on MoO_x-based SHJ cells in which the p-doped a-Si:H layer is replaced with a higher bandgap (3.3 eV) MoO_x layer show J_{SC} improvement of 1.9 mAcm^{-2}, suggesting a near complete recovery of the sub-600 nm (blue) spectrum.[15] However, this cell suffered from a nonideal S-shaped light J-V and exhibited a turnaround in the Suns-

V_{OC} measurement, similar to an a-Si:H SHJ cell (see discussion in Sections 3.2 and 3.3). Once the contacts were optimized, the S-shapes nonideality disappeared from the J-V and the cell efficiency[134] reached 22.5%. However, the long-term reliability of these materials must be determined to assess the commercial potential.

In the case of SiO_x-based SHJ cells, a larger bandgap SiO_x layer (instead of an intrinsic a-Si:H layer) is used for passivation of the c-Si wafer. Excellent effective lifetimes ($\tau_{eff} > 5$ ms) have been reported with SiO_x passivation, and J_{SC} improvement of 0.4 mAcm^{-2} (over SHJ cells) has been reported.[16] Indeed, Solar-City (owned by Tesla Inc), which has commercialized SiO_x-based heterojunction cells, has obtained efficiencies greater than 23%.[43]

6.3 | Emerging contact topology−IBCs

Interdigitated back-contact (IBC) design has been proposed to eliminate grid shadow loss in traditional c-Si solar cells. In SHJ cells, the IBC design has been particularly attractive because it eliminates the need to have a functional contact stack on the front side of the device, which liberates design space for high-transparency materials. In general, however, IBC designs introduce greater fabrication complexity into an otherwise simple SHJ cell process flow, an issue that is now actively being studied.[67] Furthermore, current crowding effects close to the back contacts can increase the overall resistance.[135] Nevertheless, the highest reported efficiencies (>25%), including the current world record for the SHJ technology, belong to devices based on the IBC architecture.[2,10,60]

6.4 | Emerging directions for device structures—bifacial and tandem SHJ solar cells

Another approach to improve the J_{SC} is through designing devices with better optical absorption. By exploiting the symmetry of SHJ cells, several groups are considering bifacial designs in which light can enter through both sides of the cell. With the front side receiving the direct illumination from the sun and the back side receiving ground-reflected light (characterized by the albedo, ie, the ratio of incident to reflected light), the annual output power for bifacial modules can be up to 34% higher than that for traditional designs.[42,136] Several companies including Panasonic,[42] Solar-city,[43] Sunpreme, and Meyer-Burger[137] have demonstrated capabilities for mass production of bifacial modules of SHJ cells.

Furthermore, absorption properties can be improved through the use of a tandem cell design. Here, two or more cells are connected optically in series to reduce the free-carrier thermalization losses associated with short wavelength light.[138] When SHJ cells are used as bottom cells, several top cells, such as Perovskite[63,66] and GaInP[64,65] can be used. A hybrid design with the advantages of both bifacial and tandem designs of Perovskite/SHJ cell has been proposed.[44,45] This hybrid design not only provides significant gains in power output but is also predicted to be tolerant to cell thickness variations, thereby relaxing the stringent optical absorption length requirements of tandem solar cells.

6.5 | Cost analysis and projections for SHJ cells

In 1997, SHJ technology appeared in the PV market with the start of a production line by Sanyo's PV division (now owned by Panasonic Inc[139]). Ever since, there has been a lot of work on efficiency improvements, and SHJ cells have systematically broken every record for maximum conversion efficiency. Based on LCOE calculations, this technology has become an attractive option for utility-scale PV deployment and a potential replacement for a significant portion of the c-Si market.[46,140] A waterfall chart of LCOE comparisons between c-Si technology and SHJ cells is reproduced from Hauser et al[3] and presented in Figure 12. This waterfall chart can be understood by separating the LCOE advantages of SHJ cells into module- and cell-level advantages.

6.5.1 | LCOE reduction at the module level

The major contributors to the drop in LCOE in SHJ cells are the high module efficiency (~19.6%), better temperature coefficient (−0.258%/K)[141] and longer life span (40 y, with glass-glass modules). Note that, with every ~1% improvement in module efficiency, the balance of system costs reduces by ~6% to 7%. With a better temperature coefficient, SHJ cells can harvest higher overall solar energy throughout the day and year, which makes this technology especially attractive for the hot-climate market. Thanks to their higher conversion efficiencies and good infrared-reflecting properties at the rear contact, this technology will also lead to significantly less device heating compared to diffused-junction approaches.[142,143]

Unlike c-Si technology, which uses p-type wafers, SHJ cells with n-type wafers do not exhibit LID. Thus, the difference in LCOE between current c-Si and SHJ cell technologies is ~2.5 c/kWh (representative number; exact price can vary dramatically)[3] (see Figure 12). Further reduction in LCOE of SHJ cells can be achieved by exploiting the inherent bifacial module design, where lower-priced solar glass replaces the more expensive plastic backsheet.[46] In addition, frameless designs are also being explored to further improve the cost effectiveness of SHJ cells.
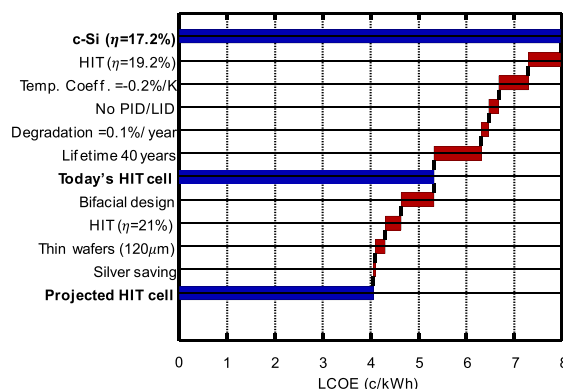
FIGURE 12 This waterfall chart shows the drop in LCOE with technology improvements in SHJ cells. This figure was reproduced from Hauser et al[3] with permission. LCOE, levelized cost of energy [Colour figure can be viewed at wileyonlinelibrary.com]

6.5.2 | LCOE reduction at the cell level

Significant cell cost reductions can be achieved by improving PECVD process control, which is anticipated to increase the overall module efficiency to 21%, as shown in Figure 12. Further analysis suggests that there are two other major components for cell production cost: wafer costs and silver metallization costs.[46] Traditionally, p-type wafers, which have lower production costs compared to n-type wafers, are used in c-Si technology. This is because phosphorous-doped wafers (n-type) are more prone to dopant segregation, which results in a nonuniform electrical resistivity throughout the ingot compared to boron-doped p-type wafers. In addition, p-type ingots can be melted and used in p-type poly silicon wafer feedstock. On the contrary, there are no recycling components in n-type poly wafers.[144]

Although SHJ technology uses more expensive n-type wafers, the two main advantages for n-type wafers are the absence of LID and the lower sensitivity to interstitial transition metal defects present in the feedstock, which reduces the refining costs.[144] The lower sensitivity of defects in n-type wafers is because acceptor-type defects remain filled in n-type wafers and do not participate in recombination processes.[145]

Furthermore, the wafer cost for next-generation SHJ cells can be reduced by moving from current slurry-based wafer sawing (producing >180-μm-thick wafers) to diamond-wire-based sawing (producing 120-μm-thick wafers). Alternatively, kerfless approaches are also actively pursued by combining epitaxially grown silicon substrates with a lift-off process. Excellent electronic material quality on large surfaces can be achieved as evidenced by the fabrication of 22.5% efficient SHJ cells that are 243.4 cm^2 in size.[146]

The silver costs can also be reduced by moving from screen printing (which uses 12 g of Ag per module) to a smart-wire adhesion process (which uses ~3 g of Ag per module) or even to a copper-based smart-wire adhesion process.[88] Interestingly, replacing ITO with zinc oxide (ZnO) does not improve the TCO costs in any significant way (see Louwen et al[46] for details). Finally, we note that although the current and projected production costs of SHJ technology are comparable to those of traditional c-Si technologies, the real advantage of the SHJ technology is in its much lower lifetime costs and thus the LCOE.

6.6 | Concluding remarks

1. SHJ is a technology of immense promise, in particular because structurally it resembles the ideal PV configuration and it allows bifacial light absorption.

2. Thanks to ideal passivation in SHJ solar cells, voltages close to the theoretical limit are possible, enabling record device performance with very small temperature dependencies.

3. Design and optimization of SHJ solar cells involve a subtle interplay of several factors. However, we have identified 5 key parameters, developed a multiprobe approach to characterize the parameters, and established the process correlations between the parameters.

4. A strict control of process parameters (especially the ultrathin a-Si:H layers) is crucial in developing practical SHJ solar cells. The loss of several percent of absolute efficiency can be due to process variation. However, nanometer deposition control over multiple square-meter areas is well established thanks to the flat-panel industry.

5. Significant innovations in module design (eg, bifacial design), contact topology (eg, IBC architecture) and passivation (eg, MoO_x/a-Si) continue to improve cell performance. It is clear that the efficiency will continue to approach the theoretical limit with further process, device, and module innovations.

Apart from determining the device physics, the key challenge is the cost of SHJ solar cells (partly because of the use of n-type substrates and Ag consumption). Once the cost question is addressed satisfactorily, SHJ cells are expected to find widespread adoption as the dominant PV technology in the world.

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