

# Design of a simple and low-cost solid-state ultra-fast high-voltage switch

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## ABSTRACT

Ultra-fast high-voltage switches (UFHVSs) are a core component of time-of-flight mass spectrometers for realizing high accuracy ion acceleration, deceleration, and temporal focusing. The desirable features of high performance UFHVSs include a large range of adjustability of pulse width, a high maximum output amplitude, and minute rising and falling times. Besides the simplicity of the driver circuit, the total cost of the whole device is also critical to its practical applications. In this work, we present a low-cost and easy-fabrication 5000 V bipolar solid-state UFHVS for a high-resolution mass spectrometer. A double-pulse transformer isolates the circuit's high- and low-voltage sides and synchronously drives series-connected cascode SiC FETs to form its push–pull topology. This scheme allows transmitting drive signals with long widths but without the magnetic saturation of the transformer. Testing results show that output pulses reach a maximum voltage of 5000 V and a width of 150  $\mu$ s, with rising and falling times of 8.5 and 18.3 ns, respectively. More importantly, they have nearly no voltage decay.

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## I. INTRODUCTION

Ultra-fast high-voltage switches play a significant role in a variety of applications, particularly in time-of-flight mass spectrometers, where they serve as a central component for ion acceleration and deceleration and temporal focusing. The resolution and ion transfer efficiency are highly affected by the amplitude, voltage decay, and the rising and falling edges of the output high-voltage pulses.<sup>1–3</sup>

The most prevalent topology of UFHVS circuits is the serial connection of high voltage transistors, which is the simplest but most effective design for application to mass spectrometers that need high voltages and weak currents. The key to success in such a methodology is the high-voltage isolated drive circuit, which can adopt either an active or a passive mode.

In an active mode, the driver is typically arranged on the low voltage side with an isolated power supply.<sup>4</sup> Although the conventional active drive circuit design exhibits high controllability and synchronization,<sup>5,6</sup> it usually needs a rather complex circuit and has a high cost.<sup>7</sup> In addition, the maximum output is limited by

the voltage of the signal isolation device. In contrast, no extra isolation power supplies are needed for passive mode drive circuits. Capacitive<sup>8–11</sup> and transformer coupling<sup>11–14</sup> are the two main passive modes. The capacitive coupling has a low cost, but it suffers from the overvoltage of the first transistors that turn-on faster than the others that are serially connected. However, for transformer coupling, although it has inherent synchronicity and fast response, pulse width adjustment is difficult as only one-side edge can reach the nanosecond regime.

Taking advantage of the extremely low on-resistance of SiC JFETs and high breakdown electric fields,<sup>15–17</sup> normally on SiC JFETs are often utilized as core transistors in high-voltage switches.<sup>18</sup> However, these JFETs need rather complex driving, starting, and protective circuits<sup>19</sup> and can only be turned off by applying negative voltages. Therefore, a normally on high-voltage SiC JFET is always coupled with a low-voltage Si MOSFET. This combination is the so-called cascode SiC FET (CSFET),<sup>20</sup> which has a faster switching speed, lower switching losses, a smaller on-resistance, and improved gate reliability than the conventional SiC MOSFET,<sup>19,21–24</sup> which makes it appropriate for high-voltage pulsed applications.

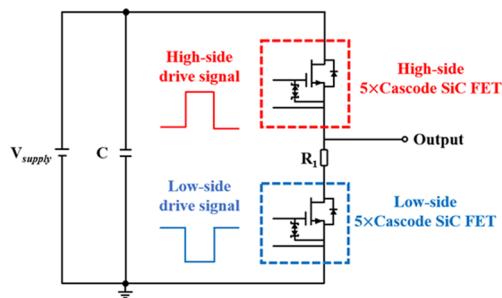


FIG. 1. Schematic of the 5 kV high-voltage switch circuit.

In this work, we present a design that has an isolated high-voltage drive based on dual-pulse transformer coupling, using serially connected 1200 V CSFETs as switch units to realize a 5000 V bipolar, ultra-fast, low-cost, and high-voltage switch.

## II. HIGH-VOLTAGE PULSE CIRCUIT

The 5000 V switch circuit is shown in Fig. 1, where the half-bridge high-voltage side is composed of five Series-Connected CSFETs (SC CSFETs) (model: UF3C120150B7S). The drive signals for the upper and lower arms come from the same source but are inverted, as shown in Fig. 2. The functions of the circuit are described as follows: When the upper arm driving signal arrives,

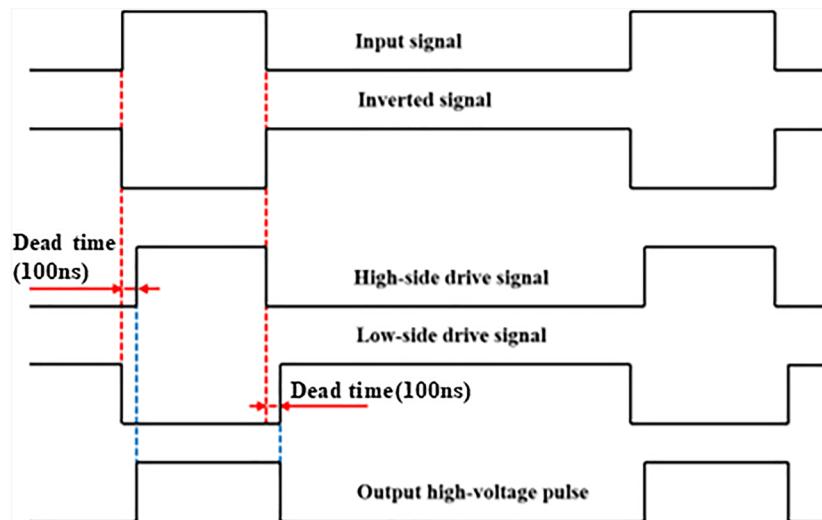


FIG. 2. Timing sequence diagram of the 5 kV high-voltage switch circuit.

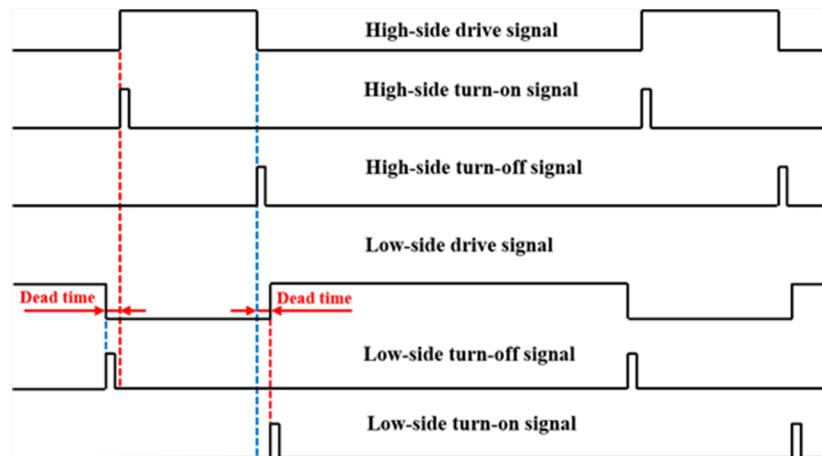
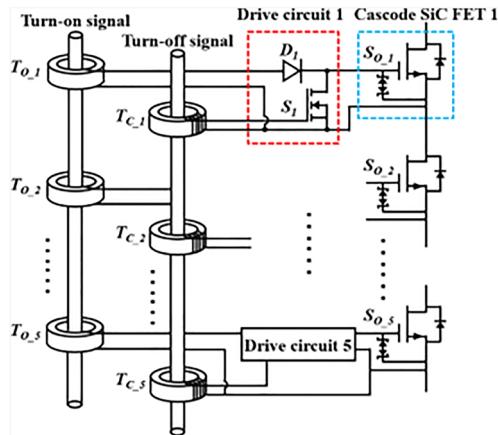
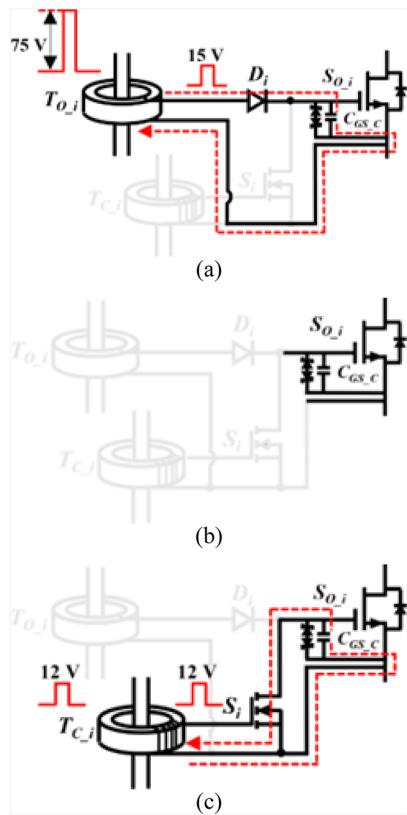


FIG. 3. Timing diagram of the isolated driving signals.



**FIG. 4.** Schematic diagram of the high-voltage isolated drive for the one-sided bridge arm.

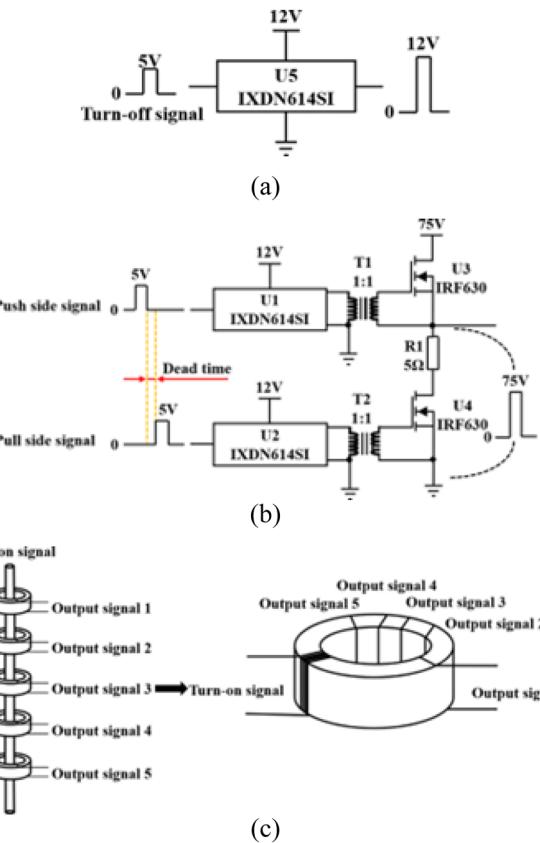
the series-connected high-side CSFETs will turn on simultaneously. After passing the high-voltage DC to the load, the output pulse reaches its maximum amplitude. It stays at that voltage until the lower arm drive signal comes, when the series-connected low-side



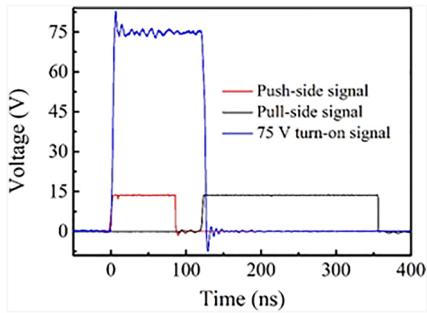
**FIG. 5.** Schematic diagram of the switching sequence of the isolated driving circuit.  
(a) Turn-on. (b) On-hold. (c) Turn-off.

CSFETs turn on simultaneously, shorting the load to the ground, so the output voltage falls to zero. Although the MOSFETs are connected in series, multiple MOSFETs are turned on simultaneously due to their parallel gating configuration. They are working as a series connected resistor chain, and the on-state resistance differences between different MOSFETs are small enough to avoid overloading of any of them. Therefore, working as a switch at on-state does not need extra actions to keep all transistors bear the same voltage. Due to the switching delay caused by the parasitic capacitance of the CSFET, the dead time between the two drive signals must be taken into account to guarantee the switching process.

When the lower arm is turned off and the upper arm is on, the busbar voltage will be loaded on the lower arm SC CSFETs, resulting in both a large voltage ( $dV/dt$ ) and a large current change ( $di/dt$ ). A large  $dV/dt$  will generate a noticeable displacement current between the gate and drain through the parasitic capacitance  $C_{GD,C}$  of the lower arm SC CSFETs, while a large  $di/dt$  can lead to a transient voltage across the source parasitic inductance  $L_S$ . All in all, it will rise the gate-to-source voltage  $V_{GS}$  and possibly surpass the threshold voltage  $V_{th}$ , thereby needing the resistor  $R_1$  to diminish the effect and crosstalk-induced false triggering.  $R_1$  has a resistance of  $300\ \Omega$ .



**FIG. 6.** Diagram of pulse amplification circuits. (a) Turn-off pulse amplification circuit with an output of 12 V pulses. (b) Turn-on pulse amplification circuit with an output of 75 V pulses. (c) Turn-on pulse transmission.



**FIG. 7.** The red line is the 12 V push-side drive signal, the black line is the 12 V pull-side drive signal, and the blue line is the 75 V output turn-on signal, which has a rise time of 3.2 ns and a fall time of 8.1 ns.

Besides providing isolation between the high- and low-voltage sides, the isolation drive also provides the necessary current and voltage to the gates of the SC CSFETs, which synchronizes and balances the voltage between them. The signal delay and separation circuit at the low-voltage side provides the primary turn-on and turn-off signals to the drive circuit. These two parts are described in detail in Secs. II A and II B.

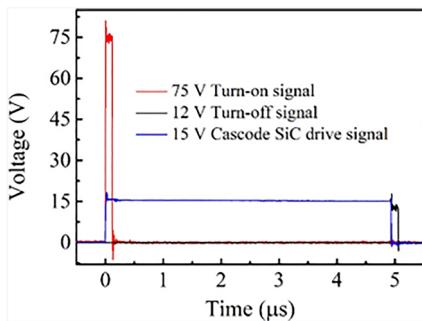
### A. High-voltage isolated drive circuit

#### 1. High-voltage pulse isolation

For a passive drive circuit, long pulse signals cannot be transmitted due to the magnetic saturation of the pulse transformer. To circumvent this issue, only the rising and falling edges of the low-voltage side output pulse are used as turn-on and turn-off signals, as shown in Fig. 3.

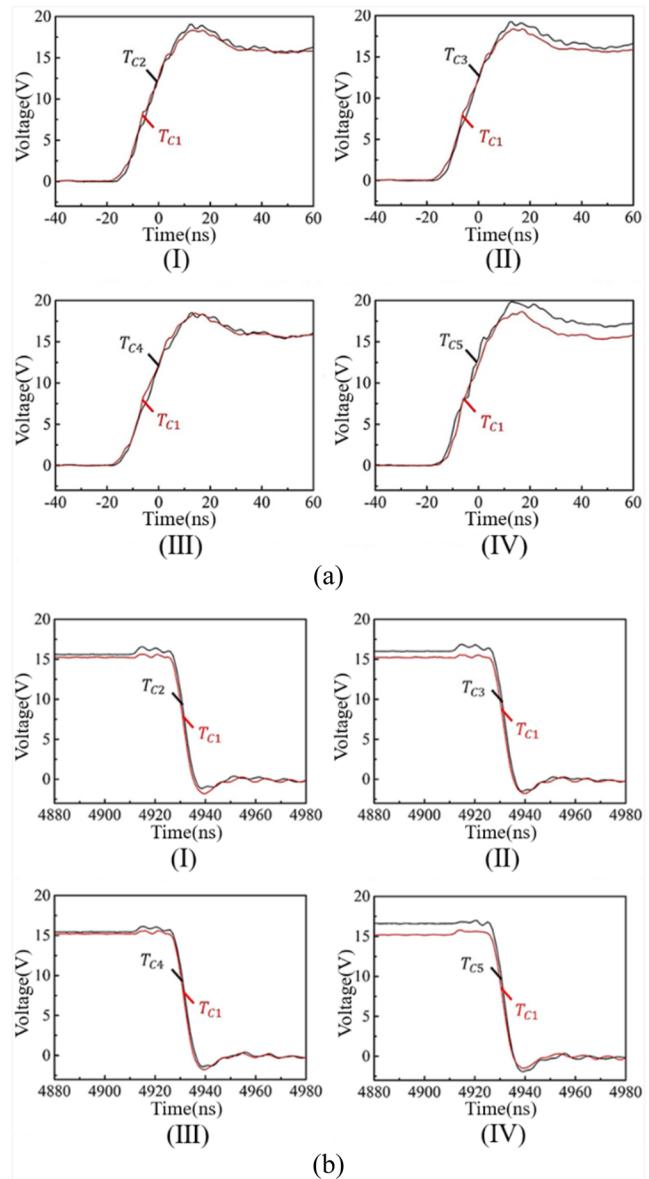
The two pulse transformers are designed to transmit the turn-on and turn-off pulses, which, combined with the passive components of the high-voltage side, restore the long pulse.

The isolated drive circuits used in the upper and lower arms are identical, as shown in Fig. 4. There,  $S_{O-i}$  is one of the SC CSFETs.  $T_{O-i}$  and  $T_{C-i}$  are the magnetic rings for transmitting the turn-on pulse.



**FIG. 8.** Pulse transformer coupling transmission signals and the gate drive signal of the CSFET. The red line is the 75 V turn-on signal, the black line is the 12 V turn-off signal, and the blue line is the drive signal of the CSFET with an amplitude of 15 V, a rise time of 9.1 ns, and a fall time of 5.9 ns.

and turn-off signals;  $D_i$  is the high-conductivity ultra-high speed diode (IN4454) with a maximum reverse voltage of 50 V and a forward conduction voltage of only 0.575 V, which is used to prevent the reverse discharge of the parasitic capacitance between gate and source.  $S_i$  is an N-MOSFET (AO3422). It is used to control the discharge of the parasitic capacitance gate to the source of the CSFET.



**FIG. 9.** Push-side MOSFET gate drive signals. (a) Rising edge of the gate drive signal on the CSFETs (I)  $T_{c2}$ , (II)  $T_{c3}$ , (III)  $T_{c4}$ , and (IV)  $T_{c5}$  (black curve) at the high-voltage push end compared with the one for  $T_{c1}$  (red curve). (b) Falling edge of the gate drive signal on CSFETs (I)  $T_{c2}$ , (II)  $T_{c3}$ , (III)  $T_{c4}$ , and (IV)  $T_{c5}$  (black curve) at the high-voltage push end compared with the one for  $T_{c1}$  (red curve).

As shown in Fig. 5(a), the turn-on signal is coupled to the electrically isolated high-voltage side through  $T_{O,i}$  to drive  $S_{O,i}$  by charging  $C_{GS,C}$ . When the turn-on signal runs from high to low, as shown in Fig. 5(b), there is no route to discharge the parasitic capacitor  $C_{GS,C}$  since the low-voltage Si MOSFET  $S_i$  is turned off and the diode  $D_i$  is reversed, so  $S_{O,i}$  will remain on. Only when the turn-off signal arrives through  $T_{C,i}$ , the low-voltage Si MOSFET  $S_i$  will turn on and  $C_{GS,C}$  can discharge to the floating ground, thus turning off  $S_{O,i}$  as shown in Fig. 5(c). Here,  $T_{O,i}$  and  $T_{C,i}$  have outer and inner diameters of 8.5 and 3.5 mm, respectively, and a height of 3.5 mm. They are made of an iron-based amorphous alloy, which is superior to normal ferrite in many aspects.

Since the same primary winding is used to produce the induced current for the secondary of each of the magnetic rings, it enables synchronous driving of all the SC CSFETs. In this coupling configuration, the maximum pulse width is not limited by the saturation time of the transformer but only by the discharge time of the gate to source parasitic capacitance of the high-voltage circuit. It resolves a long-standing difficulty in using a pulse transformer coupling in the application of long pulses. Additionally, the isolation voltage between the high and low sides can be adjusted by simply changing the air gap between the primary winding and the inner wall of the magnetic ring.

## 2. Pulse transformer coupling

Considering the balance between performance and cost, IXDN614SI is chosen as the drive unit; see Fig. 6(a). IRF630 power MOSFETs are used to build a push-pull pulse amplification circuit, as shown in Fig. 6(b). In order to provide a high enough driving power to the secondary winding of the transformer, two IXDN614SI

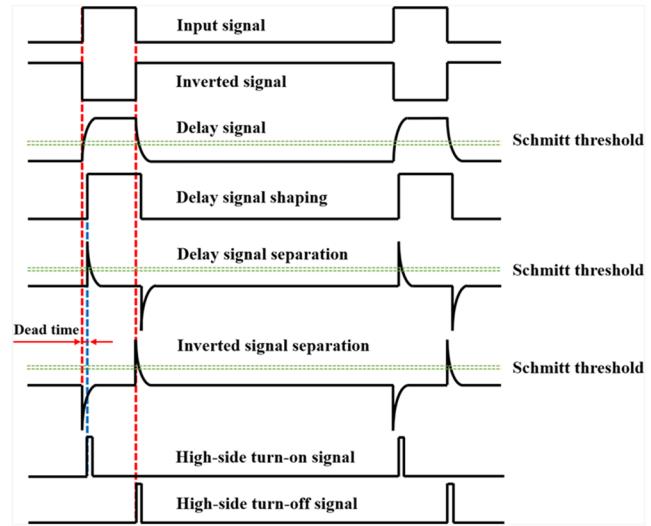


FIG. 11. Timing sequence diagram of the separated turn-on and turn-off signals of the upper arm at the low-voltage side.

chips, U1 and U2, are used as the driver chips for the high and low sides of the circuit on the low voltage side. The same design is also applied to the primary winding. The equivalent model is shown in Fig. 6(c). Therefore, with a 1 turn secondary winding, in order to achieve 15 V gate voltage on the CSFETs, the primary winding needs to be applied at 75 V. The output results are shown in Figs. 7–9.

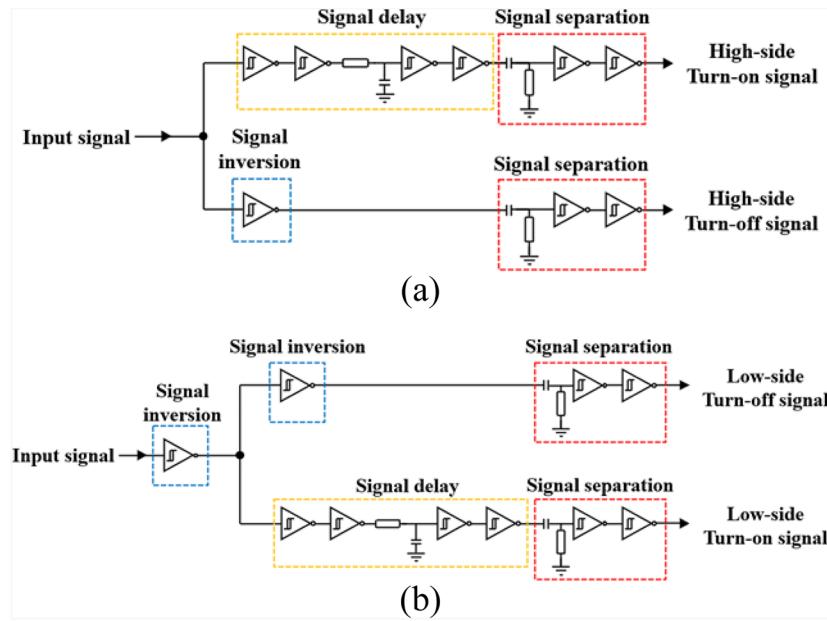


FIG. 10. Diagram of the separation of the turn-on and turn-off pulses at the low-voltage side. (a) High-side input signal delay and separation circuit. (b) Low-side input signal delay and separation circuit.



FIG. 12. Photograph of a high-voltage switch.

### B. Low-voltage end signal delay separation circuit

The low-voltage signal delay and separation circuit is used to provide 75 V turn-on pulses and 12 V turn-off pulses to the high-voltage drive, which can be divided into an input delay circuit, a rising and falling edge separation circuit, and a pulse amplification circuit.

As shown in Fig. 10, the low-voltage side signal is split into two mutually inverted signals to serve as the inputs to the low-voltage push and pull sides. The delay is obtained with a low-pass RC circuit and a SN74HC14 Schmitt trigger chip, whose function is to shape the slow rising and falling edges after the delay.

The input signal delay circuit of the upper and lower arms is shown in the yellow dashed box in Fig. 10. After delay shaping, the rising and falling edges of the input signal on the push side form the upper arm drive signal, while the falling and rising edges of the inverted delay output signal on the pull side form the lower arm

drive signal, as shown in Fig. 3. There is a dead time between the upper arm and lower arm drive signals.

As indicated in the red dashed box in Fig. 10, signal separation consists of a high-pass RC filter and an SN74HC14. Through this, the rising and falling edges of the input signal are extracted to serve as the turn-on and turn-off triggers, while the rising and falling edges of the inverted signal form the on and off edges for the lower arm. The timing diagram is shown in Fig. 11.

Since the circuit uses a pulse transformer for high- and low-voltage isolation and direct drive of the CSFETs, the pulse width of the separated short pulse should be less than 100 ns. However, as long as the turn-on time at the pull side is long enough for discharging, it will work properly. This design achieves accurate signal delay and separation and has the advantages of simple adjustment and strong anti-interference.

### III. EXPERIMENTAL TESTING

The photograph of the high-voltage switch is shown in Fig. 12. The 5000 V bipolar high-voltage switch was tested with pulses generated by a DG645 digital delay generator. The output high-voltage pulse was captured by a Tektronix MD03104 oscilloscope with a P6015A  $\times 1000$  high-voltage attenuation probe. As shown in Fig. 13, the 5000 V pulse has 8.5 and 18.3 ns rising and falling edges and a pulse width of 30  $\mu$ s at a repetition rate of 20 Hz (the rise and fall time are defined as the time required for the output voltage to rise from 10% to 90% and to fall from 90% to 10% of the total voltage, respectively). Further tests indicate that with a pulse width of 150  $\mu$ s, there is no observable output decay, as shown in Fig. 14. In addition, we also tested the minimum pulse duration and the maximum pulse duration. The minimum pulse duration is 300 ns, which is mainly limited by pulse amplification circuits. If the input pulse is too short, the push-side drive signal and pull-side signal will overlap, causing the 75 V turn-on signal to fail to output normally. Due to the

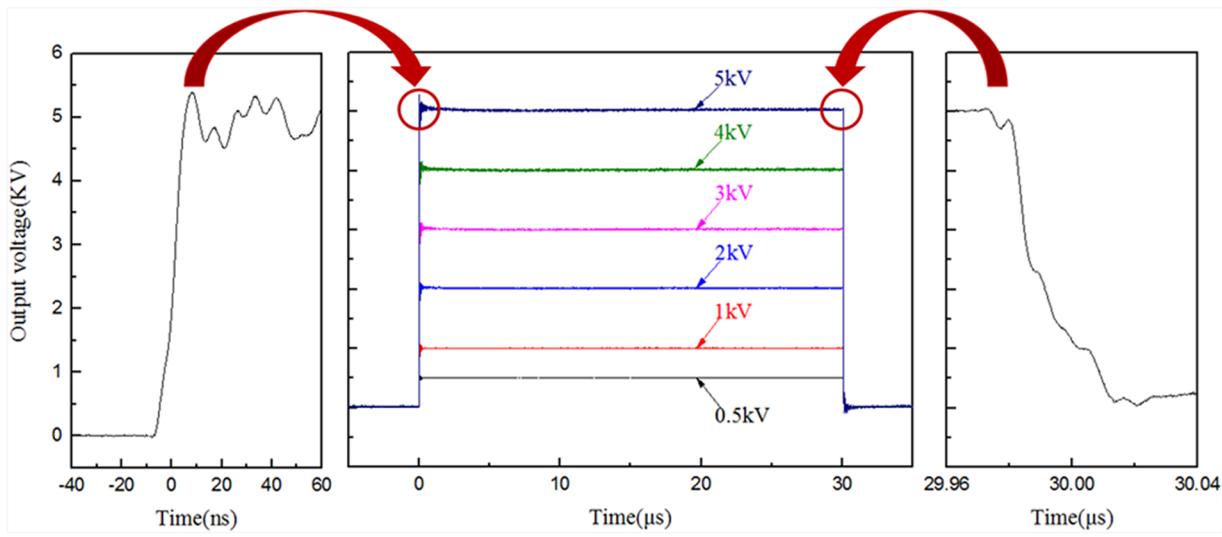


FIG. 13. Output of pulses up to 5000 V. The close-up shows the rising and falling times of 8.5 and 18.3 ns for the 5000 V output pulse.

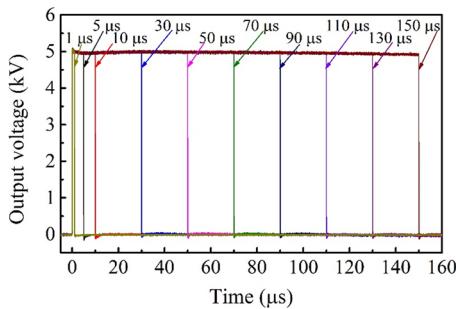


FIG. 14. Output pulse with a width of 1–150  $\mu$ s at an amplitude of 5000 V.

limitations of high-voltage power supplies and the maximum current of CSFETs, we cannot test the maximum pulse duration under high-voltage conditions, so we conduct experiments under the condition of adding a voltage of 100 V. In the case of a frequency of 10 Hz, when the input signal duty cycle is 90% (pulse width 90 ms), the high-voltage pulse switch can still output the waveform normally.

#### IV. CONCLUSION

We present a design of a 5000 V all-solid-state ultra-fast bipolar high-voltage switch for high-resolution mass spectrometry. The adoption of passive drive circuits for the high-voltage secondary terminals enables the coupled turn-on and turn-off pulses to actively control the series-connected CSFETs, achieving both long pulse drive signal transmission and high-voltage isolation. This scheme resolves the difficulty due to the magnetic saturation of the transformer while synchronously driving the series-connected topology. Testing results demonstrate that output pulses have rising and falling times of 8.5 and 18.3 ns at 5000 V with a duration of 30  $\mu$ s and nearly no voltage decay for pulse durations from 1 to 150  $\mu$ s.

#### SUPPLEMENTARY MATERIAL

See the supplementary material for the design and algebraic analysis of the pulse amplification circuit and the schematic and timing sequence diagrams of the input signal separation of the 75 V push-pull amplification circuit.

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#### AUTHOR DECLARATIONS

##### Conflict of Interest

The authors have no conflicts to disclose.

#### Author Contributions

Ziwen Zhou and Yifan Li are contribute equally.

**Ziwen Zhou:** Data curation (lead); Investigation (lead); Methodology (lead); Writing – original draft (lead). **Yifan Li:** Investigation (equal); Methodology (equal); Writing – original draft (equal). **Zhaojun Liu:** Investigation (supporting); Methodology (supporting). **Runyu Wang:** Investigation (supporting); Methodology (supporting). **Tianjie Ma:** Investigation (supporting); Methodology (supporting). **Zezhao Jia:** Methodology (supporting). **Guangjia Yin:** Methodology (supporting). **Ramiro Moro:** Writing – review & editing (supporting). **Lei Ma:** Investigation (lead); Methodology (lead); Supervision (lead); Writing – review & editing (lead).

#### DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

#### REFERENCES

- <sup>1</sup>Y.-H. Cai, C.-H. Lin, and Y.-S. Wang, “Theoretical study of the impact of ion acceleration parameters on the mass resolving power in linear MALDI time-of-flight mass spectrometry,” *Int. J. Mass Spectrom.* **471**, 116756 (2022).
- <sup>2</sup>Z. Ren, M. Guo, Y. Cheng, W. Sun, M. Dong, G. Li, X. Pei, and C. Wu, “Simulated and developed an electron impact ionization source for space miniature time-of-flight mass spectrometer,” *Vacuum* **174**, 109207 (2020).
- <sup>3</sup>Y. Zhu, L. He, J. R. Srinivasan, and D. M. Lubman, “Improved resolution in the detection of oligonucleotides up to 60-mers in matrix-assisted laser desorption/ionization time-of-flight mass spectrometry using pulsed-delayed extraction with a simple high voltage transistor switch,” *Rapid Commun. Mass Spectrom.* **11**, 987–992 (1997).
- <sup>4</sup>T. Okuda, Y. Nishimura, K. Nishioka, S. Kishimoto, Y. Kikuchi, and T. Nakamura, “A 5-kV pulse generator with a 100-kV/ s slew rate based on series-connected 1700-V SiC MOSFETs for electrical insulation tests,” *Rev. Sci. Instrum.* **92**, 114705 (2021).
- <sup>5</sup>Y. Sukhatme, V. K. Miryala, P. Ganesan, and K. Hatua, “Digitally controlled gate current source-based active gate driver for silicon carbide MOSFETs,” *IEEE Trans. Ind. Electron.* **67**, 10121–10133 (2020).
- <sup>6</sup>C. Dimarino, J. Wang, R. Burgos, and D. Boroyevich, “A high-power-density, high-speed gate driver for a 10 kV SiC MOSFET module,” in *2017 IEEE Electric Ship Technologies Symposium (ESTS)* (IEEE, 2017), pp. 629–634.
- <sup>7</sup>P. Wang, F. Gao, Y. Jing, Q. Hao, K. Li, and H. Zhao, in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)* (IEEE, 2018).
- <sup>8</sup>R. Yu, Y. Xu, Z. Fan, and W. Chen, “Analysis of series SiC MOSFETs stack using a single standard gate driver,” in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)* (IEEE, 2016), pp. 1664–1668.
- <sup>9</sup>L. Pang, T. Long, C. Zhou, F. Cai, K. He, and Q. Zhang, “An overvoltage driver with inductive adder pulse for fast switching of series-connected MOSFETs module,” *AIP Adv.* **9**, 095052 (2019).
- <sup>10</sup>L. Pang, T. Long, K. He, Y. Huang, and Q. Zhang, “A compact series-connected SiC MOSFETs module and its application in high voltage nanosecond pulse generator,” *IEEE Trans. Ind. Electron.* **66**, 9238–9247 (2019).
- <sup>11</sup>X.-W. Feng, X.-W. Long, and Z.-Q. Tan, “Nanosecond square high voltage pulse generator for electro-optic switch,” *Rev. Sci. Instrum.* **82**, 075102 (2011).
- <sup>12</sup>C. Batard, N. Ginot, and C. Bouquet, “Design of a gate driver for SiC MOSFET module for applications up to 1200 V,” *IET Power Electron.* **13**, 1364–1373 (2020).

- <sup>13</sup>J. Upadhyay, M. L. Sharma, A. B. Ahuja, and C. P. Navathe, "Development of high-voltage pulse generator with variable amplitude and duration," *Rev. Sci. Instrum.* **85**, 064704 (2014).
- <sup>14</sup>X. Chen, W. Chen, X. Yang, Y. Han, X. Hao, and T. Xiao, "Research on a 4000-V-ultrahigh-input-switched-mode power supply using series-connected MOSFETs," *IEEE Trans. Power Electron.* **33**, 5995–6011 (2018).
- <sup>15</sup>H. Shimizu, H. Okino, S. Akiyama, K. Katoh, N. Yokoyama, and K. Ishikawa, "600-V 27-mΩ normally off SiC junction field effect transistors for high-efficiency power supply," *Jpn. J. Appl. Phys.* **53**, 031303 (2014).
- <sup>16</sup>H. Shimizu, S. Akiyama, N. Yokoyama, H. Imomata, H. Kobayashi, A. Fukuiji, T. Iijima, K. Tomiyama, Y. Sasaki, and S. Ibori, "Controllability of switching speed and loss for SiC JFET/Si MOSFET cascode with external gate resistor," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)* (IEEE, 2014), p. 221.
- <sup>17</sup>D. C. Sheridan, A. Ritenour, V. Bondarenko, P. Burks, and J. B. Casady, "Record 2.8 mΩ·cm<sup>2</sup> 1.9 kV enhancement-mode SiC VJFETs," in *Proceedings of the 2009 21st International Symposium on Power Semiconductor Devices and IC's* (IEEE, 2009), pp. 335–338.
- <sup>18</sup>A. Mihaila, F. Udrea, S. J. Rashid, P. Godignon, P. Brosselard, D. Tournier, J. Millan, G. Amaralunga, and G. Brezeanu, "High temperature characterization of 41-SiC normally-on vertical JFETs with buried gate and buried field rings," in *2006 International Semiconductor Conference* (IEEE, 2006), pp. 1–4.
- <sup>19</sup>C. Zhao, L. Wang, X. Yang, F. Zhang, and Y. Gan, "Comparative investigation on paralleling suitability for SiC MOSFETs and SiC/Si Cascode devices," *IEEE Trans. Ind. Electron.* **69**, 3503–3514 (2022).
- <sup>20</sup>Z. Li and A. Bhalla, "USCI SiC JFET cascode and super cascode technologies," in *PCIM Asia 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management* (IEEE, 2018), pp. 1–6.
- <sup>21</sup>R. Wu, J. O. Gonzalez, Z. Davletzhanova, P. Mawby, and O. Alatise, "Fast switching SiC cascode JFETs for EV traction inverters," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)* (IEEE, 2020).
- <sup>22</sup>Y. Gunaydin, S. Jahdi, O. Alatise, J. O. Gonzalez, M. Hedayati, B. Stark, J. Wang, X. Yuan, and P. Mellor, "Impact of temperature and switching rate on forward and reverse conduction of GaN and SiC cascode devices: A technology evaluation," in *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)* (IET, 2020), pp. 782–787.
- <sup>23</sup>X. Song, A. Q. Huang, L. Zhang, P. Liu, and X. Ni, "15kV/40A FREEDM supercascode: A cost effective SiC high voltage and high frequency power switch," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)* (IEEE, 2016).
- <sup>24</sup>B. Hu, Z. Wei, H. Li, X. Lyu, D. Xing, R. Na, and J. Wang, "Characterization and evaluation of 4.5 kV 40 A SiC super-cascode device," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)* (IEEE, 2017), pp. 321–326.