2D Materials Nanoelectronics: New Concepts, Fabrication, Characterization From Microwaves up to Optical Spectrum

Mircea Dragoman, Adrian Dinescu, and Daniela Dragoman*

The paper presents the state-of-the art of nanoelectronic devices based on 2D materials related to the cutting edge of Moore's law. Ballistic electron devices, ferroelectric, and atomically thin heterostructures are analyzed to show the benefits of 2D materials applications in nanoelectronics. It is shown that these new devices fulfill the basic requirements for further developments of new materials and circuits architectures envisaged beyond the Moore law. However, in many aspects, these new devices, concepts, as well as their implementations, are at the very beginning, so that the main obstacles to be overcome and the inherent difficulties to design and fabricate nanoelectronic devices based on single-atom- or few-atoms-thick materials are also presented.

1. Introduction

Moore's law[1] is not a physical law, but a development trend that has worked well for more than 50 years, stating that the number of transistors on the same chip area will double each 18 months, so that the dimensions of transistors will reduce with 50% in the above-mentioned duration of time. Later, the initial duration of time was decreased. This law has deep implications in many areas of sciences, such as electronics, communications, and physics, especially solid-state physics, optics, chemistry, and material science. The reason is that Moore's law is in fact the road-map of the development of electronic, computer, and communication industries, that is, the most advanced industries to date, having a very strong influence on all other existing industries. Therefore, the Moore's law approaching its end could be a dramatic event, because the performances of many equipments and services will stall for an undefined period of time. This happens because the gate length of Si transistors is reaching very soon the dimensions of few atoms, and short channel effects will disturb very much the functioning of tiny field effect transistors (FETs). Moreover, due to the high degree of integration, implying few billions of transistors integrated on a single chip and requiring tens of billions of metallic interconnects, the produced dissipated heat is so large that it cannot be evacuated with standard and non-expensive cooling systems. Thus, to avoid thermal runaway, the speed of microprocessors was stalled below 3 GHz since two decades.

The state of the art in CMOS VLSI circuits is now at 14 nm node, but 10 nm node based on FinFETs[2] is already in fabrication, while some companies use 7 nm node: TMSC/AMD for Vega-20-GPU and Huawei for the Kunpeng 920 7 nm ARM Processor.

To overcome the difficulties to push further Moore's law, solutions can be found in the history of electronic circuits. The development of FETs with gate lengths less than 100 nm was possible by finding new materials, such that now more than 60 materials from the Mendeleev table are used, rather than the starting 11 materials at the beginning of the integrated circuits era.[3] At the same time, the optical photolithography breakthrough has allowed the systematic reduction of transistor dimensions, so both discoveries in materials and optics have contributed to impressive reduction of circuits in CMOS technology. Since large scale integrated circuits are using optical lithography (in the extreme-ultraviolet (EUV) range), when the features are scaling down below 10 nm the costs of such equipments soar at very high prices. In a recent report, the McKinsey company considers that reaching the 10–11 nm node will imply an increase of the capital costs by 40%, while the R&D investments will rise by 150%.[4]

All these limitations suggest that 2D materials or atomically-thick materials should be considered as having a leading role in the future development of electronics. New circuits architectures for developing new ways of computation, such as neuromorphic computation or quantum computing, are envisaged, as well as reconfigurable high frequency circuits for 5G communications, which are the backbone of the internet of things (IoT).

How will 2D materials devices respond to the above challenges beyond Moore's law? The response we know now is sketched in the remaining of the paper. In what follows, we present first a brief review of 2D materials' physical properties.

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DOI: 10.1002/pssa.201800724

Then, we discuss about graphene – the best known 2D material – and the ballistic devices based on it. 2D materials showing ferroelectricity are presented next, since they are very interesting for many future applications, followed by 2D materials heterostructures, which are the source of inspiration of many new innovative devices.

2. Physical Properties of 2D Materials

This section is a very short review of 2D materials relevant to nanoelectronics. A detailed account of the physics of 2D materials is found in ref. [5] and will not be repeated here, except the main issues about growth, electrical, and mechanical parameters related to nanoelectronic devices based on atomically thin materials. In all following considerations, one-atom-thick materials will be referred to as monolayers, two-atom-thick materials as bilayers, and thicker materials, but not exceeding 10 nm, as multilayers or few-atom thick materials. Today, there are more than 1000 materials which can be obtained as monolayers or few-atoms thick.[6] The large majority of them originate from a category of materials termed van der Waals materials, which are layered structures formed from billions of monolayers held together in the vertical plane by weak van der Waals forces, while in the horizontal plane, that is, in the monolayers' plane, there are strong bonds between atoms (**Figure 1**).

Due to the above properties of van der Waals materials, the simple method to obtain a monolayer is to detach monolayers and multilayers using an adhesive tape. This method is famous after using it for years to get graphene monolayers and later transition-metal-dichalcogenides (TMDs). This is still today the main method to obtain 2D materials for studying their physical properties. However, this method cannot be applied for nanoelectronic devices due to the low yield and lack of reproducilibility. The single 2D material grown today at the 4 inch and 6 inch Si wafer scale is graphene, grown by CVD (chemical vapor deposition) methods, and such wafers are commercially available. The rest of 2D materials are only occasionally grown on Si wafers, due to the inherent difficulties to grow monolayers with a low rate of defects.

In the case of graphene, we have two main methods to grow monolayers, described in **Table 1**. A good review about these methods is found in ref. [7]. The most used approach is graphene growth via CVD on Cu substrates, followed by the transfer on the Si/SiO_2 wafer of 4 or even 6 inches. The thickness of SiO_2 is 300 nm, since at this thickness the graphene monolayer is visible at a microscope.[8] More recent methods are proposing the growth of graphene without any transfer process, directly on dielectric.[9]

Regarding the other 2D materials, the wafer scale growth is not so advanced, although promising results are obtained using various methods such as ALD (atomic layer deposition), CVD, MOCVD (metal-organic chemical vapor deposition) or direct methods such as sputtering, pulsed-laser deposition (PLD) or e-beam methods.[10] The number of papers reporting wafer scale nanoelectronic devices based on MoS_2 monolayer are increasing. The first results on MoS_2 FETs made on three-atomic layers of MoS_2 grown on Si/SiO_2 by MOVCD were reported in ref. [11], and few-layers of MoS_2 grown on GaN were reported recently.[12]

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Intensive efforts are underway to grow other 2D materials at the wafer scale for various applications.[13]

Very often, 2D materials nanoelectronic devices are compared with Si devices. However, it is usually neglected to be mentioned that the growth techniques at the wafer level are primitive in comparison to that for the Si monocrystalline wafer, which has now the dimensions of 300 mm (12 inch) with a thickness of 775 μm. On these Si wafers billions of nanoelectronic devices are integrated, the whole fabrication process being automatized and controlled by computers.

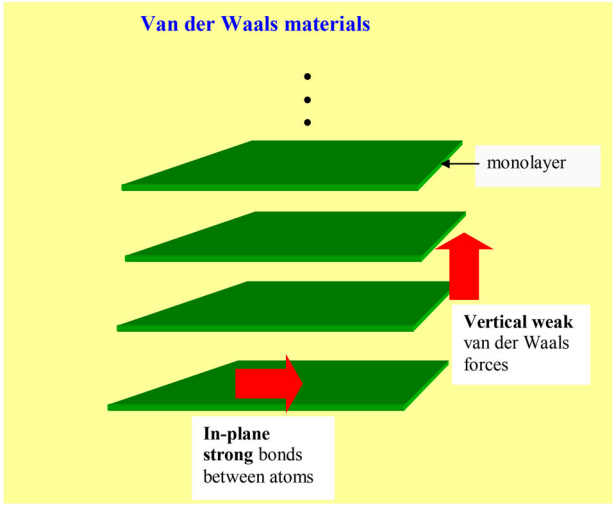

Figure 1. Van der Waals materials.

On the other hand, processing and integration of graphene grown by CVD in a 200 mm wafer Si technology is now available at the pilot line level.[14] Also graphene growth on SiC based on the thermal decomposition of Si atoms near the surface due to the different partial pressures of C and Si has advanced, and presently wafers up to 200 mm are available. The quality of the graphene on SiC is the same or even better compared to that grown by CVD methods due to the higher fabrication temperature.[15]

Although the nanoelectronic devices based on 2D materials benefit from all these advanced fabrications techniques, the quality of 2D materials wafers is very low in comparison to Si. This is the research area where we need to focus in the next years if we want to see mature 2D nanoelectronic devices in few years.

The main difference between graphene and other 2D materials is that the carriers' transport in graphene is described by a Dirac-like equation,[5] graphene being a gapless material, while in the case of all other 2D materials the transport of carriers is described by the Schrödinger equation. Therefore, graphene, TMD and other 2D materials will be described separately.

2.1. Physical Properties of Graphene

Graphene monolayers are native 2D electron gas materials where the transport of carriers is described by the Dirac equation. As a result, the density n in graphene monolayers is electrical modulated by a back gate (usually doped Si), according to the relation $n(V_G) = \varepsilon_0\varepsilon_d V_G/te$,[16] where ε_0 and ε_d are the dielectric permittivities of air and isolation dielectric of the backgate on which graphene is transferred (SiO_2, HfO_2), respectively, and V_G is the backgate voltage. The Fermi level (E_F) in graphene is initially placed at the Dirac point when $n = 0$, and the backgate voltage shifts the Fermi energy level, defining the transport carrier type (n or p) in graphene devices via this unique electrical doping (**Figure 2**). Therefore, the carrier transport in graphene is always ambipolar. Figure 2 shows that graphene has metallic behavior, since it has no bandgap. In deep contrast to semiconductors, electrons and holes in graphene have an identical role, and identical physical properties, at least at low energies and in high quality graphene with a reduced number of defects.

The main physical properties of graphene are found in **Table 2**.

Graphene monolayers show the highest mean-free-path length at room temperature among all known materials, and therefore their main application in electronics are ballistic devices working up to THz frequencies, as will be shown later. The main challenge of graphene electronics for digital applications is to have simultaneously a high mobility and a large on/off ratio, issue that can be solved using nanopatterned graphene FET channels.

2.2. Physical Properties of 2D Materials

The most studied 2D materials for nanoelectronics are TMDs, having the formula MX_2, where M is a transition metal and X is a chalcogen, such as S, Te, and Se. All TMDs are known to be semiconductors, MoS_2 and WS_2 being the most studied. There are many reviews where TMD are discussed in detail.[5,25–27] We

Table 1. Graphene growth methods at the Si wafer level.

Material	Method	Yield	Graphene surface
SiC	Thermal decompostion of Si atoms at high temperature	Moderate	Moderate (3–4 inches up to wafers of 200 mm)[14,15]
CVD	Gas mixture (CH_4 and H_2)	Very high	Very large (4–6 inces)[7–9]

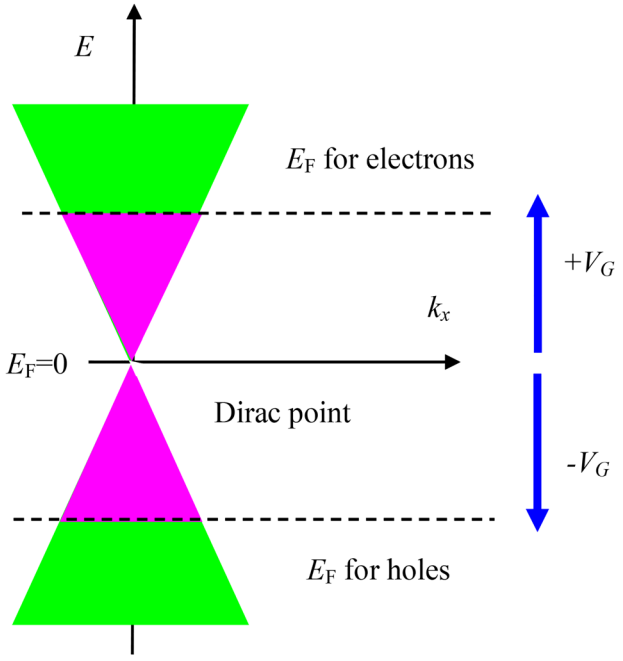

Figure 2. Electrical doping in graphene.

will present here only the main physical parameters for electronic applications.

The bandgap (see **Table 3**), which is one of the most important parameters in electronic devices, is varying as a function of the material thickness, that is, as a function of the number of monolayers. In the case of MoS_2, the bandgap is of 2.4 eV for a monolayer, 2.1 eV for a bilayer, and 1.6 eV for few-layers.[29] The mobility of several TMDs, mostly obtained from numerical simulations, is displayed in **Table 4**.[30]

From this table we see that, except Hf-based TMDs, all other TMDs have mobilities lower than Si. So, we cannot expect to use these materials in digital or high-frequency devices, since these nanoelectronic devices will underperform the existing ones on Si. The single 2D material with very high mobility is germanene (18000 $cm^2 Vs^{-1}$), but it is unstable in air, as is silicene (10^3–10^5 $cm^2 Vs^{-1}$). Both are atomically-thin versions of Ge and Si, respectively, but are, in addition, very difficult to grow. Few examples illustrate this situation. Recently, a 1 bit microprocessor based on 115 MoS_2 FETs was reported.[31] However, despite the impressive progress in the integration of MoS_2 transistors, even if this microprocessor will be extended at 8 bits or 16 bits, it will never compete with a Si microprocessor since the mobility of MoS_2 is lower than Si, and its clock will not exceed 40–60 kHz. In another example, a FET having silicene as channel and capped with Al_2O_3 loses its electrical signal in air in about 2 min.[32]

The physical properties of materials tell us always which are those that can be used in nanoelectronic devices and circuits, and what are the expectations. As will be seen later, 2D materials have impressive applications in many areas of nanoelectronics.

3. Graphene Devices and Circuits at the Waferscale

3.1. Ballistic Graphene Devices

At the macroscopic scale, in semiconductors electrons are moving randomly due to the high scattering rates with impurities and phonons. An applied electric field induces a diffusive electron transport, with a limited mobility, and heat dissipation due to scattering mechanisms. In deep contrast, the ballistic transport is defined as the collisionless transport regime, valid when the dimensions of the sample are smaller than the mean free path L_{fp}. In the ballistic transport, the carriers become matter waves, which is a direct manifestation of quantum mechanics,[33] and they have the highest possible

Table 2. Main physical properties of graphene.[17]

Parameter	Room temperature values
Mobility	44 000 $cm^2 Vs^{-1}$ (intrinsic)[18] 100 000 $cm^2 Vs^{-1}$ in suspended graphene or in graphene over h-BN[19]
Mean free path (ballistic transport at room temperature)	400 nm in good quality graphene monolayer[20] >1 mm for graphene encapsulated in BN monolayers[19] >10 mm in graphene nanoribbons[21]
Thermal conductivity	5000 $W mK^{-1}$, better than in many metals[22]
Bandgap	0 eV in graphene monolayers >0.1–0.3 eV in graphene nanoribbons[23] or nanopatterned graphene[24]

Table 3. Bandgap of 2D materials.[17,28]

2D material	E_v [eV]	E_c [eV]	E_g [eV]	Type of gap	Workfunction (eV)
HfS_2[28]	−6.30	−5.1	1.23	Indirect	−5.7
$HfSe_2$[28]	−5.4	−4.95	0.45	Indirect	−5.17
MoS_2[17,28]	−5.9	−4.3	1.6	Direct	−5.07
$MoSe_2$[28]	−5.2	−3.9	1.31	Direct	−4.6
WS_2[28]	−5.5	−3.95	1.54	Direct	−4.70
WSe_2[28]	−4.9	−3.55	1.32	Direct	−4.2

mobility, reaching the speed of $c/300$ in the case of graphene. In consequence, the Ohm law in ballistic devices connected by ideal metallic contacts is no longer valid, and should be replaced by the Landauer law.

The Landauer law states that:

$$I = \frac{2e}{h}\int M(E)T(E)[f_l(E) - f_r(E)]dE \quad (1)$$

where I is the current, E is the energy of electrons, $f_l(E)$ and $f_r(E)$ are the Fermi-Dirac quasi-distribution functions in the left and right contacts between which a bias voltage V is applied, M is the number of transverse modes and T is the quantum probability of an electron injected in one contact to be transmitted to the other. The presence of $T(E)$ in the above law shows the quantum nature of ballistic transport, while I – the current – is a macroscopic manifestation of the quantum nature of ballistic transport. The mean free path is a measure of the distance between successive electron collisions with impurities or phonons and is about tens of nanometers in polycrystalline metallic films and about tens of micrometers in high-mobility semiconductors at low temperatures ($T < 4$ K). Thus, due to the high mobility and very reduced heat dissipation, ballistic electron devices are appealing for the post-Moore era, but, however, they must work at room temperature. Graphene monolayer has a very large L_{fp} at room temperature (see above Table 2), while L_{fp} in Si is only 2 nm. Other semiconductor nanostructures show high mean-free paths at room-temperature, such as InAs nanowires ($L_{fp} = 150$ nm), or InSb/AlInSb quantum wells ($L_{fp} = 589$ nm). We have displayed in **Figure 3** a schematic representation of diffusive and ballistic transport in a FET, for comparison.

Ballistic transistors at room temperature are a longstanding expectation of nanoelectronics, especially in THz signal emission and detection, where transistors based on drift-diffusive transport cannot work. The first attempts of ballistic transistors involving semiconductor heterostructures working in THz were based on carrier plasma instabilities.[34,35] Ballistic devices such as the ballistic rectifier (BR), which is an asymmetric four-terminal cross-junction based on ballistic carrier transport is able to rectify alternative currents. Such BRs were implemented as a junctionless diode used as an InGaAs/InAlAs/ InP deflection transistor[36] or in graphene.[37]

We have developed the first ballistic graphene FET working at room temperature trying to solve two basic issues: i) to obtain a nonlinear drain current–drain voltage ($I_D - V_D$) characteristic knowing that the non-ballistic graphene monolayers FETs have a linear $I_D - V_D$ dependence, acting as voltage-controlled resistances and ii) to obtain amplification knowing that non-ballistic graphene monolayer FETs show no amplification, the ratio between transconductance g_m and drain conductance being less than 1. Equation (1) is a strongly nonlinear dependence between current and voltage in the ballistic regime, so it was expected that $I_D - V_D$ will become strongly nonlinear at certain gate voltages V_G.

However, there is a very detrimental effect in graphene ballistic transport, not encountered anywhere in other 2D materials, due to the Dirac transport equation of carriers. The effect is called Klein paradox, and it states that the transmission coefficient T (see Equation (1)) cannot be modulated by electrostatic gates at normal incidence because in this case, always, $T = 1$. Therefore, our ballistic graphene FETs geometry have oblique gates at an inclination of 45° with respect to the drain (D)-source (S) axis. This allows the modulation of $T(E)$ between 0 and 1 at various drain voltages. There is an energy region where $T(E)$ is abruptly decreasing to zero, meaning that the current decreases when the energy/voltage is increasing and, as a result, a negative differential resistance (NDR) region is occurring.[38] Thus, the ballistic transport is accompanied by NDR regions in graphene ballistic transistors (see **Figure 4**).

The above ballistic graphene FET having an oblique gate was fabricated on a 4 inch wafer of graphene monolayer transferred on a Si/SiO_2 wafer. The gate insulation was HSQ, with a thickness of 50 nm, and the distance between D and S was 400 nm. The gate length was 40 nm.[39]

NDR regions in the dependence $I_D - V_D$ at room temperature, showing a peak-to-valley-ratio (PVR) of 9, were measured in the ballistic FET with a tilted top gate at 45° mentioned above. The top and the back gates were able to change the NDR, modifying the PVR in the range 7–9 (see **Figure 5**).

We have further fabricated, at the 4 inch wafer scale, a ballistic graphene FET working at room temperature, using a double-gate configuration, with both gates tilted at 45°.[40] In this situation, the gate lengths are 30 nm and are separated by 40 nm, while the distance between D and S is only 190 nm. The isolation gate oxide is also HSQ, with a 40 nm thickness (see **Figure 6**a). In Figure 6a, we have displayed the SEM photo of the double-gate graphene FET. The dark rectangle is the HSQ deposited over the graphene channel, and the two gates are located over HSQ. Both graphene ballistic FET transistors, with single and double tilted gates, are working at very high frequencies since their cutoff frequency exceeds 3 THz.

The $I_D - V_D$ dependence at various gate voltages is strongly nonlinear, showing saturation regions and, at some gate

Table 4. The mobility of the few TMDs.[17,30]

2D material	Mobility [$cm^2 Vs^{-1}$]	m_{eff} (Γ–K) × m_e	m_{eff} (K–M) × m_e
HfS_2[30]	1833	3.30	0.24
$HfSe_2$[30]	3579	3.10	0.18
MoS_2[17,30]	340	0.45	0.45
$MoSe_2$[30]	240	0.52	0.52
WSe_2[30]	0.33	0.31	705
WS_2[30]	1130	0.24	0.26

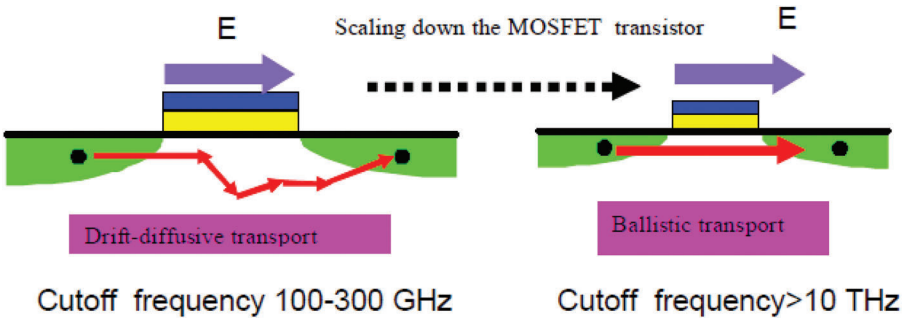

Figure 3. The drift-difussive transport and the ballistic transport in a FET.

voltages, and an NDR behavior (Figure 6b). The maximum transconductance g_m is 1.42 mS μm^{-1} at $V_D = 3$ V and $V_{TG} = -0.5$ V, being among the largest in graphene FETs. The NDR is manifested in the drain conductance g_D behavior, which is decreasing very much, and the ratio g_m/g_d becomes >50 in the gain range corresponding to a drain voltage range of 1.5–2.5 V, so we have amplification. Further, we have illuminated the D-S region with a red laser having a power of $P = 0.5$ mW and a spot diameter of 1.5 mm. The responsivity was 2.8×10^5 A/W, which is an unprecedented large value for graphene, because the generated photo-carriers have almost no time for recombination, being transported ballistic between D and S.

We have recently designed and fabricated at wafer scale quantum gates working at room temperature based on ballistic transport in graphene.[41] There is an increased interest for quantum computing, and very large companies offer cloud access at the first quantum computers built with superconducting circuits. These computers have very large dimensions and work in the mK temperature range.

The paradigm of quantum computers is the vanishing of the coherence of wave functions, termed decoherence. A quantum computation could last few ms, during which billions of operations take place, but after this short time decoherence destroys all quantum operations and the computer must be reset. A solution is the computation with ballistic devices, where in the absence of large variations of temperature and due to low imperfections at the edges of ballistic devices the coherence is not lost. Using e-beam lithography we have fabricated and measured one-qubit Hadamard or NOT gates and a one-qubit modified Deutsch-Jozsa (DJ) quantum algorithm circuit on 4 inch wafer of graphene monolayer transferred on Si/SiO_2 wafer by Graphenea. The electrical measurements have shown that the quantum coherence is present in these devices. For more details, see ref. [41] and the references herein. In **Figure 7**, we show the SEM photo of the Hadamard gate.

The above quantum gate is formed from an Y-shaped junction designed to support one mode, which is creating a superposition of $|0\rangle$ and $|1\rangle$ quantum logic states, defined as the wavefunctions of the upper and lower branches of the Y-junction. After the Y-junction the output is $(|0\rangle + |1\rangle)/\sqrt{2}$. The interference junction of length L is designed to support two modes. The two output currents measured at the end of the interference region are depending on the phase difference between the propagating modes in the interference region, given by

$$\Delta\phi(E, U_G, L) = L\left[\sqrt{(E-U_G)^2/(\hbar v_F)^2 - (2\pi/W)^2} - \sqrt{(E-U_G)^2/(\hbar v_F)^2 - (\pi/W)^2}\right] \quad (2)$$

Thus, the ratio between the two output currents is dependent on the backgate voltage. This fact was experimentally demonstrated by measuring the output currents as a function of the backgate voltage, and it was observed that their ratio strongly depends on the backgate voltage.[41] As such, the quantum coherence is evidenced. We note that if the transport is not ballistic, the ratio between the two currents is independent of the backgate voltage and no coherence is present.

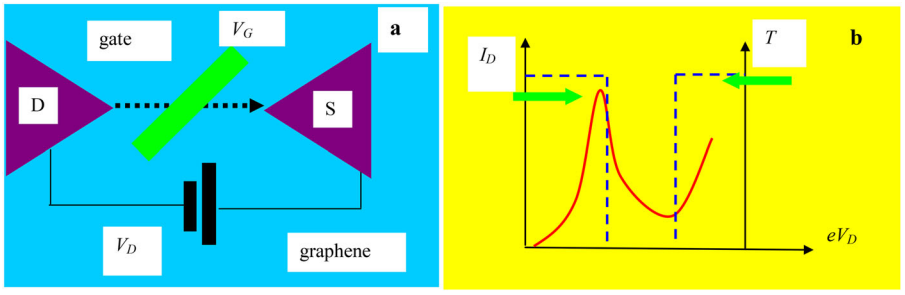

Figure 4. The principle of ballistic FETs based on graphene monolayers working at room temperature: (a) inclined gate graphene FET, and (b) transmission and current of ballistic graphene FET.

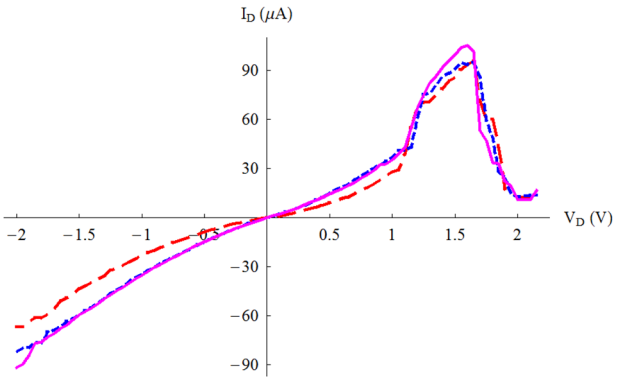

Figure 5. The NDR of the ballistic graphene FET with inclined gate at $V_{TG} = 0$ V (red dashed line), 0.5 V (blue dotted line) and 1 V (solid red line). Reproduced with permission.[59] Copyright 2017, Institute of Physics, UK.

The actual quantum computers are based on superconducting Josephson junctions (JJs). Ballistic superconducting JJs based on graphene were recently reported as the most advanced superconducting devices. JJs are SIS structures, an insulator (I) being sandwiched between two superconducting (S) metals. We know that in each superconductor the carriers can be described by a single wavefunction and the Josephson coupling is determined by the phase difference between the two superconductors Φ. Thus, in JJs, the carriers are tunneling the insulator, and the current is dependent on Φ, which is the prerequisite for quantum computing, as seen above in the case of ballistic quantum gates. The JJ can be made not only in the SIS configuration, but in a weak link configuration, in which in the proximity of superconductors are placed nanoconstrictions, 2D

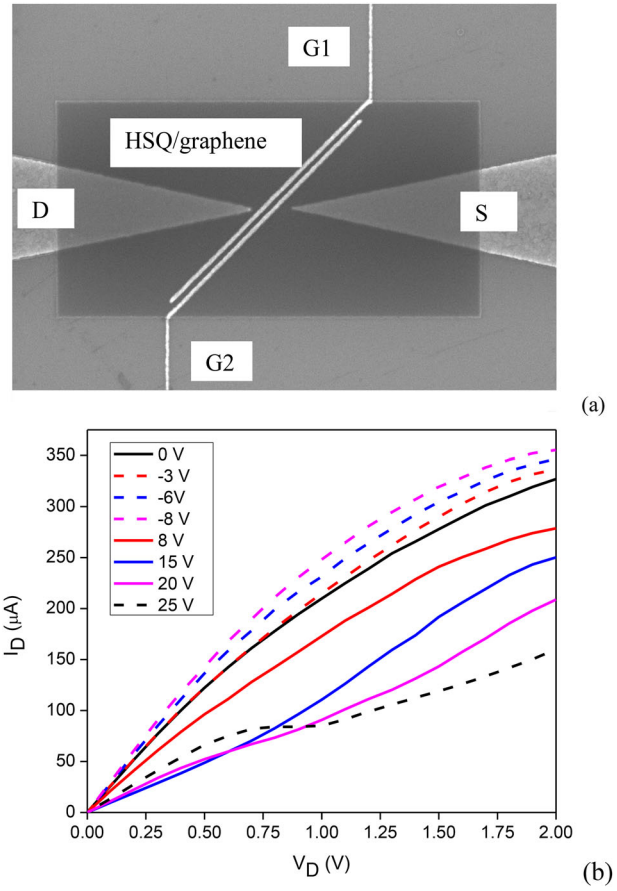

Figure 6. a) The double gate ballistic graphene FET working at room temperature. b) The I_D–V_D dependence at various gate voltages when when both gates have the same values written in the inset. Reproduced with permission.[40] Copyright 2016, AIP Publishing.

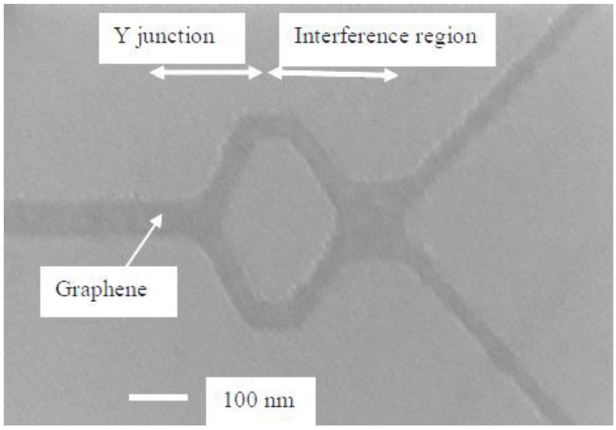

Figure 7. The graphene Hadamard gate.

electron gas semiconductors, carbon nanotubes, or nanowires having a dimension L less than the coherence length of the superconductors, ξ. All devices are based on the superconducting proximity effect.[42] Additionally, if the JJ is ballistic, the dimension L should be smaller than L_{fp} – the mean free path.[43]

There are two types of ballistic graphene JJs: i) with in-plane electrodes and ii) with vertical electrodes (see **Figure 8**). Considering that these graphene JJs must be fabricated at the wafer scale since in a quantum computer there are thousands of JJ junctions inside superconducting circuits,[44] both configurations have some drawbacks. In the first graphene JJ configuration, the roughness of the electrode edges must be small; otherwise the ballistic transport of carriers is deteriorated, this problem being the same as in the case of ballistic quantum gates reported above.[45] This configuration is fully compatible with CMOS technology. The second configuration,[43] with graphene placed between two metals, eventually with graphene sandwiched between two hexagonal boron nitride (h-BN) layers to reduce the scattering between graphene and electrodes, is more difficult to fabricate at the wafer scale, being actually beyond the state of the art of graphene fabrication processes.

3.2. Graphene Nanoelectronic Devices with Induced Bandgap

We have pointed out in section 3.1 that in graphene monolayers, the charge carriers attain unprecedented high mobilities. However, these mobilities are measured in special conditions and in special structures, such as graphene suspended structures, which cannot survive in air. Any FET needs to be based on a material with bandgap, this allowing the switching between an off and an on state, the key concept of any digital integrated circuit. Since graphene monolayers have no bandgap, there are various methods to induce it, but the mobility is downgraded at values which are often lower than in Si.

One way to improve the actual state of the art of graphene FETs is to pattern the graphene channel with nanosized holes of different forms, the most widespread being circular holes,[46] which could show ballistic transport.[47] We have reported that encapsulated graphene FETs, fabricated at the wafer scale and having a nanoperforated channel made by e-beam lithography, show saturation and blocking regions (on and off states), which are tunable via the top gate voltage. The on/off ratio is 2×10^3 at room temperature and the mobility is of 2200 $cm^2\,Vs^{-1}$, which is higher than in many TMDs monolayers and even Si.[48] Continuing along this path, we have solved recently the graphene electronic conundrum, that is, high mobility and high on-off ratio at the wafer level. In this respect, we have fabricated nanopatterned graphene FETs at the wafer level, having all the width $W = 2\,\mu m$, and nanopatterned holes with diameters of 20 nm, distanced at 100 nm on horizontal and vertical directions, inducing a bandgap of 0.3 eV.[49] We have varied the length of the transistors and measured all FET parameters, observing that the mobility of nanopatterned FETs varies significantly with the channel length, as displayed in the table below at the gate voltage of 0.5 V. The on/off ratio was at least 10^3 in all the measured range of drain voltage, between 1 mV and 2 V, irrespective of the length. The dielectric gate is HSQ.

So, depending on the nanopatterned graphene channel length we can obtain mobilities comparable to that of semiconductors such as InP, GaAs, GaN, or Si.

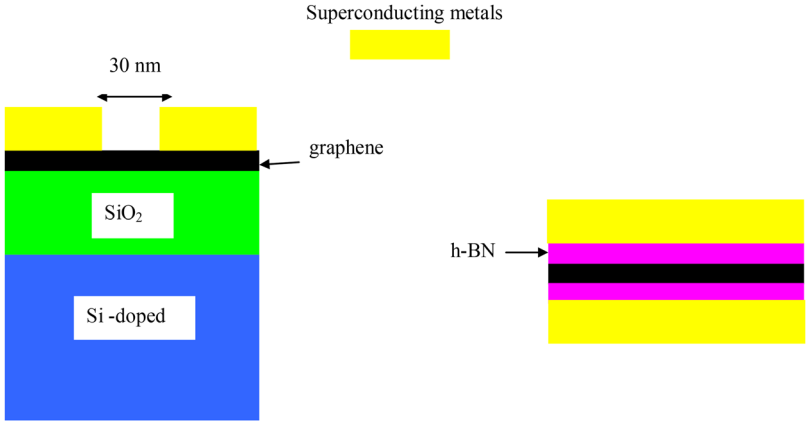

Figure 8. Ballistic Josephson graphene junctions with in-plane electrodes (left) and vertical electrodes (right).

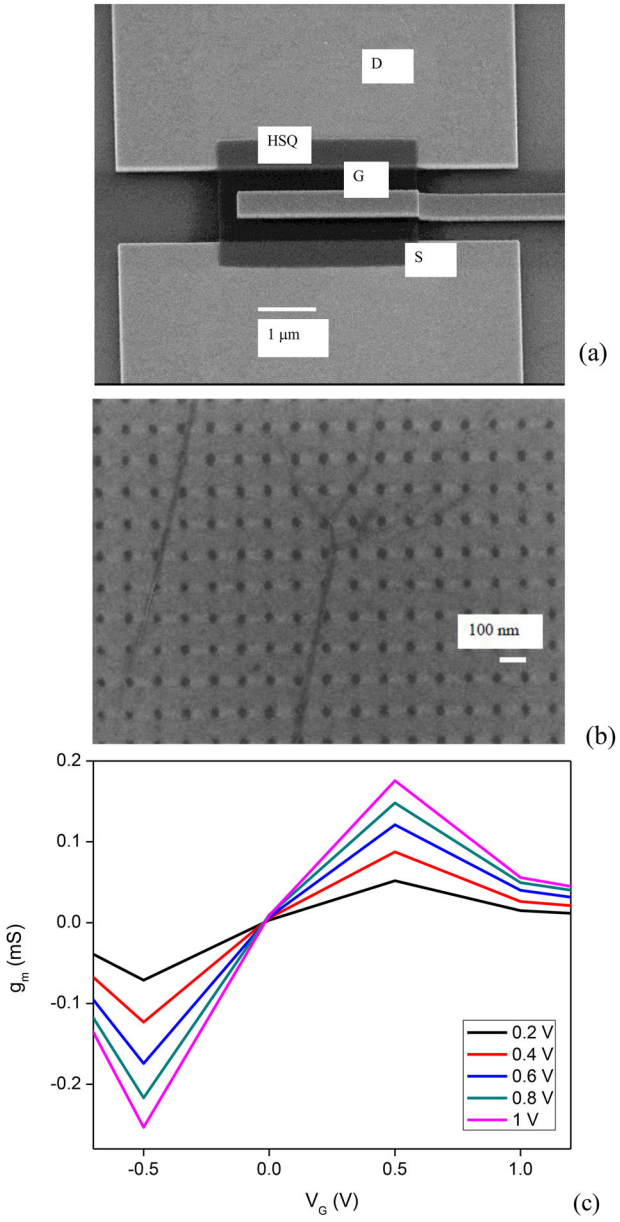

Figure 9. a) The nanopatterned graphene FET. b) The nanopatterned channel of 2 μm length. c) The transconductance at various drain voltages indicated in the inset. Reproduced with permission.[49] Copyright 2018, Elsevier.

Table 5. Mobility versus length in nanopatterned graphene monolayers FETs.[49]

Nanopatterned channel length (mm)	Mobility [$cm^2 Vs^{-1}$]
1	10 400
2	5500
3	4000
4	2500
7	1000
8	550

The above mobility was calculated from experimental data based on the formula $\mu = g_m L/WC_g|V_D| = g_m Lt/\varepsilon W|V_D|$ in which $g_m = \partial I_D/\partial V_G$ (see **Figure 9**c) is the transconductance, L (see the **Table 5** above) and $W = 2\,\mu m$ are the length and the

Table 6. Dependence of ferroelectric parameters on dopant (values from ref. [57]).

Dopant	Concentration [%]	P_r [$mC\,cm^{-2}$]	E_c [$MV\,cm^{-1}$]
Zr	50	17	1
Y	5.2	24	1.2–1.5
Al	4.8	16	1.3

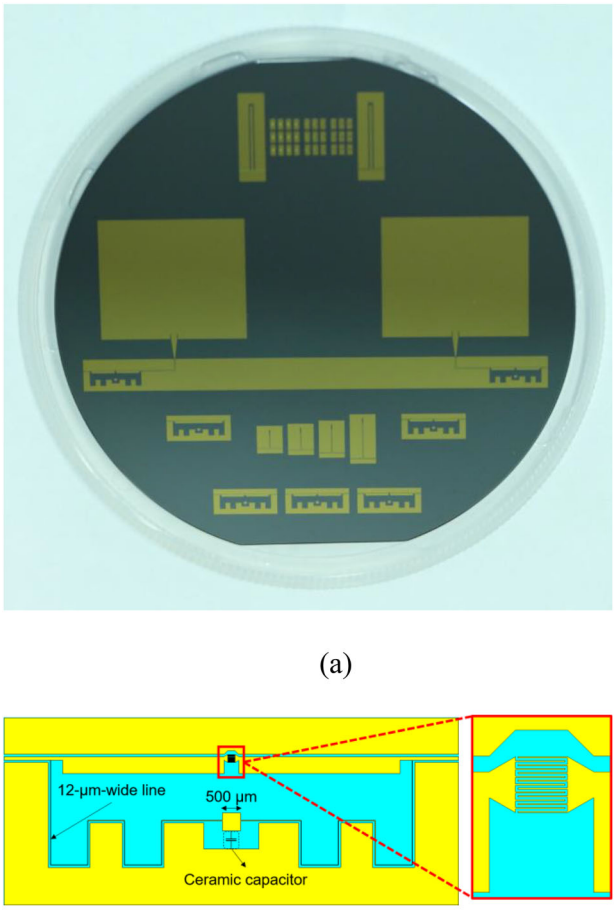

Figure 10. a) The phased array antenna, and b) detail of the antenna array to show HfZrO phase shifter. Part (b) reproduced with permission.[61] Copyright 2018, IET.

width of the GFET channel. Further, C_g is the gate capacitance per unit area, $t = 40$ nm is the thickness of the gate dielectric, and $\varepsilon = \varepsilon_0 \varepsilon_r$, with ε_0 the vacuum permittivity and $\varepsilon_r = 3.3$ the relative dielectric permittivity.

An optical image of the graphene nanopatterned FETs can be seen in Figure 9a,b.

There is another recent way to obtain high mobility and high on/off ratio: by nanopatterning the SiO_2 substrate and not the

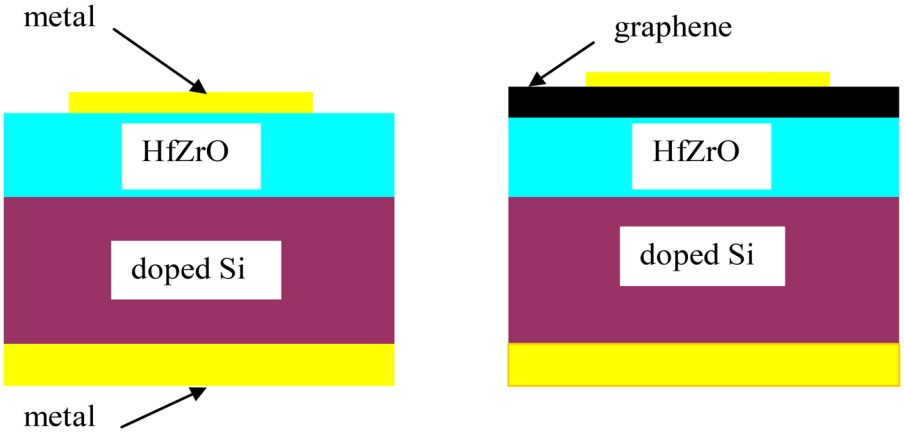

Figure 11. HfZrO/Si and graphene/HfZrO/Si memories.

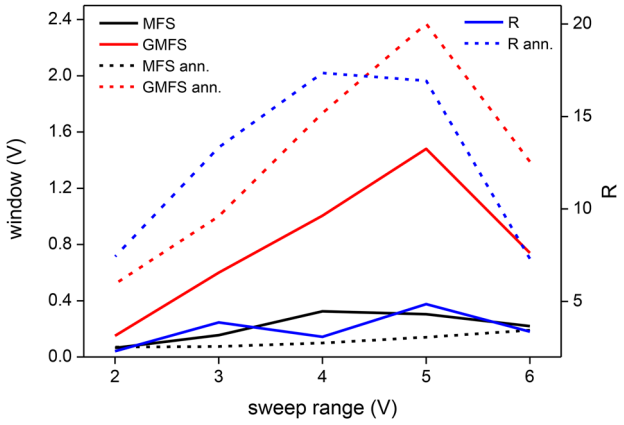

Figure 12. The memory window for MFS and GMFS (left axis) and the enhancement factor R (right axis). Reproduced with permission.[62] Copyright 2018, Institute of Physics, UK.

graphene.[50] A huge mobility of 300 000 $cm^2 Vs^{-1}$ of a graphene monolayer encapsuled in h-BN monolayers was obtained in this way, but at 250 mK. It remains to be seen if the technological processes are fully compatible at the wafer level, and to determine the mobility at room temperature, and only afterwards to build a graphene FET based on these findings.

4. 2D Ferroelectrics and Their Applications

We assist now at the rise of 2D ferroelectrics.[51] Intercorrelated in-plane and out-of-plane ferroelectricity, as well as in-plane ferroelectricity, were observed in few layers of the van der Waals semiconductor In_2Se_3 (see ref. [52] and references therein), and in-plane ferroelectricity was found in few-layers and monolayers of the semiconductor SnTe grown on graphene on SiC.[53]

The applications of 2D ferroelectrics mentioned above are targeting FeRAM (ferroelectric random access memory memories), but researches are at the very beginning since ferroelectricity was evidenced using piezo force microscopy (PFM) and other advanced methods of characterization, without any further application.

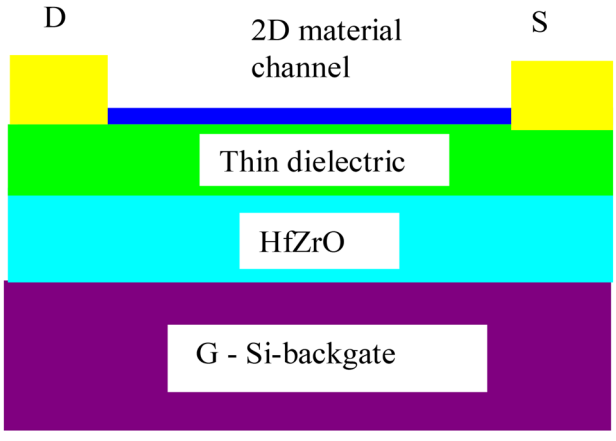

Figure 13. A 2D HfZrO transistor in backgate configuration.

However, by far, the most advanced 2D ferroelectrics are doped HfO_2, with a thickness within the range of few atomic layers, not exceeding 5–6 nm. The ferroelectricity in HfO_2 originates from an orthorhombic crystalline structure as a result of doping.[54–56]

There is a direct link between the doping material and the HfO_2-based ferroelectric parameters, as can be seen from **Table 6**.

The most used HfO_2-based ferroelectric is that doped with Zr, termed further as HfZrO. The advantage of HfZrO is that it is fully CMOS compatible, in deep contrast with other ferroelectrics, and can be grown at the Si wafer scale.

The tunability of high-frequency circuits is a prerequisite for developing further the future communications systems such as 5G or Internet of Things (IoT). Ferroelectrics are the best choice in this respect, since their electrical permittivity is dependent on the applied DC voltage. Thus, amplifiers, filters, and antenna arrays can be tuned by ferroelectrics,[58] but this approach is almost abandoned today due to the fact that the applied DC voltages attain tens of volts. However, we have demonstrated that extraordinary tunability of microwave devices can be obtained at very low DC voltages, not exceeding ± 3 V.[59] In this respect, we have demonstrated that the phase shift of an interdigitated phase shifter in coplanar technology, fabricated at the wafer scale on HfZrO/high resistivity Si, is 60^0 at 1 GHz and 13^0 at 10 GHz, if the applied DC voltage is within the range ± 3 V. The DC voltage is so low that it can be provided by a battery.[60] Moreover, by integrating two such phase shifters in the arm of an antenna array consisting of two patch antennas we have shown that the HfZrO phased antenna array is able to steer the radiation pattern at 2.55 GHz with 25^0 for very low bias voltages, of ± 1 V.[61] (see **Figure 10**a,b).

Very recently, we have designed and fabricated HfZrO memories based on the graphene monolayer/ferroelectric (HfZrO)/semiconductor/metal configuration[62] depicted in **Figure 11**. The memory windows of graphene-based HfZrO memories are 3–4 times larger than those of ferroelectric memories without graphene; the ratio is increasing after annealing. This enhancement of the memory is produced due to the additional electric field applied by the graphene monolayer on the HfZrO ferroelectric, as well as due to the negative thermal expansion coefficient of the graphene monolayer.

In **Figure 12** we have depicted the memory windows on the left axis for MFS (metal-ferroelectric metal) and GMFS (graphene-MFS) capacitors), and their ratio R (right axis) before (solid line) and after (dashed line) thermal annealing (at 80 °C for 24 h). We can see that R attains the record value of about 17.35 in the range (−4,4) V, when a graphene monolayer is inserting in the MFS.

Another important application is in low-power transistors for which the subthreshold swing (SS) must be lowered than the 60 mV/decade value, typical for CMOS transistors, using ferroelectric negative capacitance FETs.[63] This approach is of outmost importance for electronics beyond Moore law, being a vector in the era of hyper-scaling electronics.[64]

The thermal limitation is visible in the SS given by:

$$SS = \partial V_G/\partial(\log I_D) = (\partial V_G/\partial \varphi_S)(\partial \varphi_S/\partial(\log I_D)) = (\partial V_G/\partial \varphi_S)(k_B T \ln 10/q) \quad (3)$$

Table 7. The SS of FETs based on the negative capacitance of HfZrO.

Transistor type	Gate length [nm]	I_D–V_G hysteresis	SS at room temperature [mV dec^{-1}]	Ref.
FET MoS_2 channel (back-gate)	1000	Yes	6	[66]
FET MoS_2 monolayer channel (back-gate)	2000	No	20	[67]

We see from the above formula that $k_BT\ln 10/q$ is 60 mV/decade at room temperature, and this is the main obstacle of CMOS transistors in switching faster and reducing power consumption.

However, any ferroelectric could decrease the SS below 60 mV/decade by noting that SS is $(\partial V_G/\partial \phi_S)k_BT\ \ln 10/q = m \times 60$ mV/decade where

$$m = 1 + C_G/C_S \tag{4}$$

In the above formula, C_G is the gate capacitance, while C_S is the semiconductor capacitance, both capacitances being connected in series.

If C_G originates from a ferroelectric, it is a negative capacitance, so that the total capacitance of the transistor $1/C = (1/C_G + 1/C_S)$ while m is less than 1.

Such a negative capacitance can be achieved in a 2D HfZrO transistor in the backgate configuration, as that depicted in **Figure 13**. The thin dielectric layer has the role of isolating the charges in the 2D material channel from the charges in the ferroelectric.

The main transistor characteristics must show no hysteresis for low-power logical applications. There are several methods to achieve this goal.[65] In **Table 7**, we find some data regarding ferroelectric transistors where the channel is a MoS_2 monolayer and the ferroelectric is HfZrO.

Both results are very new; the SS is indeed much smaller than 60 mV/decade, and it remains to be seen if this solution will extend at the level of complex circuits.

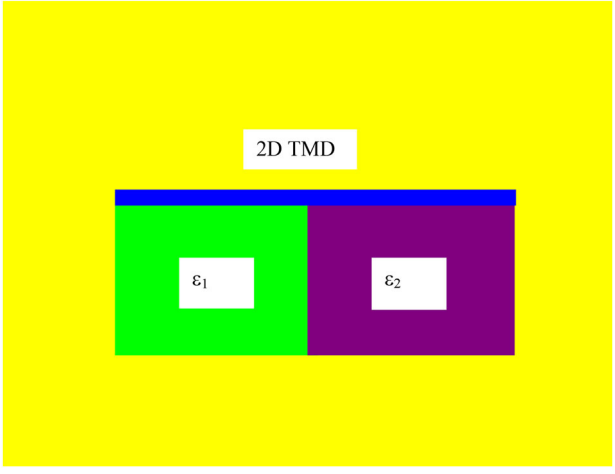

Figure 14. The induced heterostructure via screening.

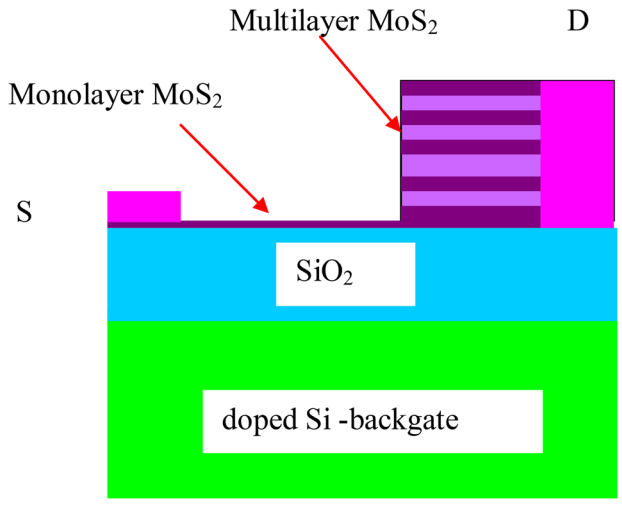

Figure 15. The 2D hetrostructure formed by different layers thicknesses.

5. 2D Heterostructures

The most promising device applications of 2D materials are 2D heterostructures. The reason is that band engineering is the key physical concept, which is at the foundation of many modern electronic devices such as resonant FETs, tunneling diodes, lasers, and photodetectors. Initially, band engineering was used for AIII-BV semiconductor compounds, such as GaAs/AlGaAs,[68] but now an entire part of semiconductor industry is relies on it. However, van der Waals epitaxy of 2D materials was able to produce up to now devices similar to heterostructure semiconductor devices, such as tunneling devices, or even heterostructure lasers. However, the growth methods of such 2D heterostructures are much less developed compared with those for semiconductor compounds, which are based on molecular beam epitaxy (MBE) and MOCVD and CVD growth.

Typically, semiconductor heterostructures are based on epitaxial methods where between an overlayer and a substrate there are strong chemical bonds originating from interface dangling bonds. On the contrary, in the case of van der Waals epitaxy there are no chemical bonds between monolayers, these

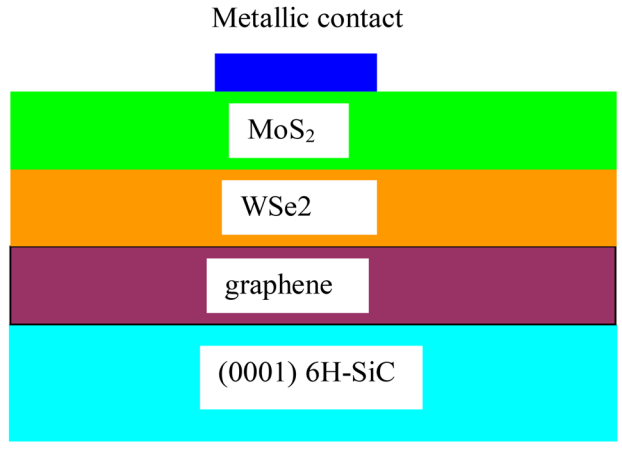

Figure 16. RTD based on a heterostructure formed from two TMDs.

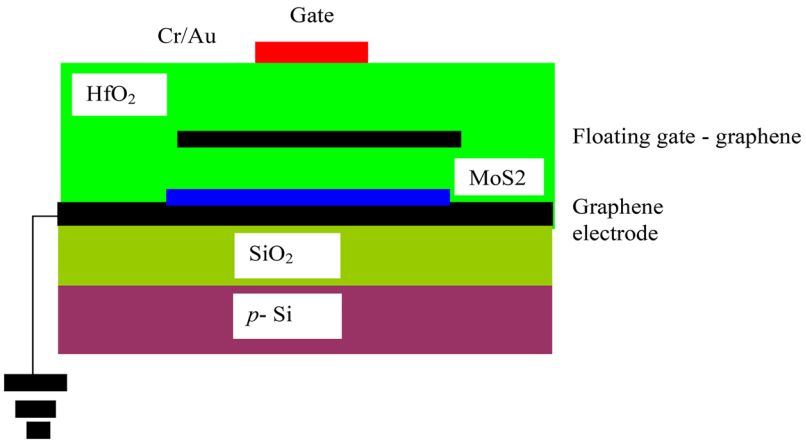

Figure 17. Nonvolatile memory based on MoS2/graphene.

bonds being found only in in-plane monolayers. The absence of dangling bonds between monolayers allows the fabrication of quality heterostructures with 40% lattice mismatch,[69] which is impossible in the case of semiconductor heterostructures where lattice matching is a fundamental prerequisite. We note that graphene and TMDs are dangling bonds-free monolayers and van der Waals epitaxy is possible due to this unique property of van der Waals materials.

Although the van der Waals epitaxy is 50 years old, it was rediscovered in the context of 2D materials.[70] There are other methods to grow 2D heterostructures, such as mechanical transfer, CVD, electrostatic assembly of monolayers, and Langmuir-Blodgett assembly. Two very recent review papers are explaining these methods in detail.[71,72]

There are also new approaches to build heterostructures using 2D materials. This is the case of lateral heterostructures. In the first example, such a heterostructure is based on the fact that in 2D materials the screening is reduced as a result of strong Coulomb interactions (see **Figure 14**). The screening can be engineered via the dielectric permittivity, and so the bandgap is changing its common meaning, of intrinsic parameter, since it depends of the dielectric permittivity of the surrounding medium. The bandgap is decreasing when the electrical permittivity is increasing.

This effect is named dielectric-induced bandgap renormalization[73] and this effect is opening a new way of bandgap engineering. Very recently, this concept was experimentally tested via a lateral heterotructure based on two dielectrics[74]: cytop, having $\varepsilon_r = 2$, and hBN, with $\varepsilon_r = 6$, which induce a type I heterostructure with a bandgap offset of 90 meV.

As a second example, another heterostructure of type I could be generated by varying the thickness of TMD, as in ref. [75]. TMD monolayers have a direct bandgap, which becomes indirect when the number of layers is increased. The heterostructure is presented in **Figure 15**.

Few examples of 2D heterostructures are given below. The first example is a resonant tunneling diode (RTD) based on MoS_2/WSe_2/graphene and WSe_2/MoS_2/graphene,[76] depicted in **Figure 16**. The two dissimilar TMDs are grown on graphene multilayer, which is epitaxially grown, in turn, on 6H-SiC.

Although the negative differential resistance (NDR) region in the current-voltage dependence is obtained, the currents are rather weak, around 0.1 nA at room temperature, while the peak-valley ratio of the NDR is 2–3.

In another example, nonvolatile memories could be implemented using MoS_2/graphene heterostructures with resistive electrodes. Four orders of magnitudes are found between program and erase states.[77] This memory is schematically represented in **Figure 17** and is based on a floating gate isolated by various dielectrics from MoS_2 and the metallic electrodes. The drain current versus gate voltage dependence has a hysteretic behavior, and at the drain voltage of 50 mV there is a 8 V wide memory window. When the top gate voltage is positive, the electrons are tunneling from the MoS_2 channel to the graphene floating gate and remain trapped in graphene. On the contrary, when a negative top gate voltage is applied, the trapped electrons are released from the graphene floating gate and the device is reset.

The memristor is another modern device where atomically-thin heterostructures could play an important role. The memristor is a nonlinear circuit element having a pinched hysteretic voltage-current dependence. Thus, the resistance of the memristor depends on the history of the applied voltage, being the electrical analogue of a brain synapse.[78] Recently, a 2D

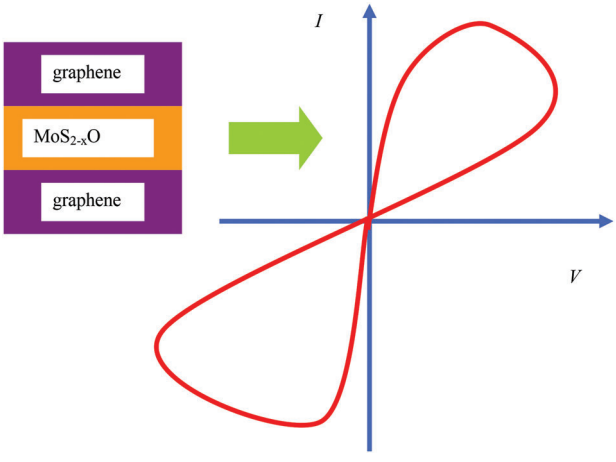

Figure 18. The graphene/$MoS_{2-x}O$/graphene memristor.

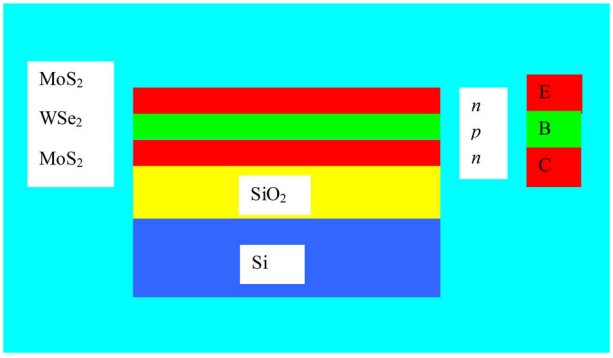

Figure 19. The 2D HBT transistor.

heterostructure graphene/$MoS_{2-x}O$/graphene was used as a memristor with impressive performances.[79] The device consists of a graphene/$MoS_{2-x}O$/graphene heterostructure on Si/SiO_2 wafer and displays an on/off ratio of 10^7 with maximum currents exceeding 1 mA, and is able to work at 340 °C. The device is represented in **Figure 18**.

Vertical transistors, such as tunneling transistors and heterobipolar transistors (HBTs) are another promising application of vdW heterostructures. A very recent review regarding these issues is ref. [80]. These vertical transistors are especially appealing for low power applications and high frequency applications. Although research on this subject is just starting, some important results were already obtained. For example, a vertical heterostructure bipolar transistor was recently reported having a high current amplification. [81] The 2D material HBT is depicted in **Figure 19**. The transistor consists of *p*-WSe_2 multilayers with the thickness of 8 nm sandwiched between two *n*-MoS_2 multilayers (10 nm thickness). This is an *n*-*p*-*n* transistor where the emitter E and collector C are MoS_2 while the base B is WSe_2. This HBT shows a current density of 1.3 A cm^{-2} and a current amplification factor $\beta = 150$, values which are comparable with HBT based on semiconductors.

6. Conclusions

Nanoelectronics nowadays is at crossroads since the Moore law is announcing its end. The atomic scale electronics is a main vector of research today, but it is at the very beginning. We have presented in this paper a state of art of various devices and circuits fabricated all at the wafer scale, and able to be developed in the future, that is, ballistic electronics, including quantum computing, 2D ferroelectrics compatible with CMOS technology high-frequency devices, memories, and low-power transistors.

Acknowledgements

The authors acknowledge the financial support of project GRAPHENEFERRO grant of Ministry of Research and Innovation, CNCS-UEFISCDI, number PN-III-P4-ID-PCCF-2016-0033.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D materials, ballistic devices, ferroelectrics, piezoelectrics, thermoelectrics

Received: September 16, 2018
Revised: March 2, 2019
Published online:

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