

Capacitance–voltage characteristics of perovskite light-emitting diodes: Modeling and implementing on the analysis of carrier behaviors

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ABSTRACT

Analyzing and optimizing carrier behaviors are essential to achieve high electroluminescence performance in perovskite light-emitting diodes (PeLEDs). In this work, a capacitance–voltage (C–V) model for PeLEDs is established to describe carrier behaviors. Four distinct regions in this typical C–V model, including a neutrality region, a barrier region, a carrier diffusion region, and a carrier recombination region, were analyzed. Importantly, the C–V model is implemented to guide the electroluminescence (EL) performance improvement in PeLEDs. By studying the measured C–V characteristics of a typical PeLED, issues of a high hole injection barrier and insufficient recombination are revealed. To address them, one MoO₃ interface layer with deep conduction band minimum is designed between a hole transport layer and a hole injection layer to enhance the hole injection. The C–V characteristics for the optimized PeLED confirm the reduced injection barrier and strengthened recombination rate. The optimized PeLED shows an improved external quantum efficiency from 8.34% to 15.82%. The C–V model helps us to quantitatively understand the essential carrier behaviors in PeLEDs and can serve as an efficient method to improve the EL performance of PeLEDs.

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Recently, perovskite light-emitting diodes (PeLEDs) have developed rapidly and attracted worldwide attention. Due to their excellent optical properties such as an easily tunable bandgap and narrow-band emissions, PeLEDs show potential in lighting and display fields.^{1–4} The basic carrier behaviors of PeLEDs include carrier injection, transportation, and recombination.^{5,6} To improve the electroluminescence (EL) performance of PeLEDs, analyzing and optimizing carrier behaviors (e.g., enhancing the rate of carrier injection, transporting, and recombination) are widely implemented strategies.^{7–10}

However, some mechanisms for essential carrier behaviors in PeLEDs are not very clear. For instance, quantitative evaluation of carrier accumulation is difficult. Meanwhile, a detailed analysis of carrier injection and transport is arduous. Since carrier behaviors directly dominate the EL performance, further understanding of them

becomes a vital issue for the optimization of PeLEDs.¹¹ Impedance spectroscopy is a powerful method to characterize electrical properties of materials and their interfaces.^{12–15} As a key parameter of impedance spectroscopy, a capacitance–voltage (C–V) characteristic can quantitatively measure the change of space charges in devices and describe carrier behaviors, indicating an efficient method to help understanding carrier behaviors and further improving EL performance.^{16–18} C–V analysis has been implemented in some semiconductor devices.^{19–21} However, for PeLEDs, related modeling and further measurement of C–V characteristics are lacking, which limit their further application.

In this work, a C–V model for PeLEDs is established to connect capacitances with carrier behaviors. First, the four distinct regions of the C–V model, including a neutrality region, a barrier region, a carrier diffusion region, and a carrier recombination region, were analyzed.

Then, carrier behaviors in PeLEDs, including carrier injection, transportation, and recombination, are clearly analyzed by the model. Furthermore, the C-V model is implemented to guide the optimizations of EL performance in PeLEDs. By studying the measured C-V characteristics of a typical PeLED, we show the issues of the high hole injection barrier and insufficient recombination. In order to address them, one MoO₃ interface layer with deep conduction band minimum is designed between the hole injection layer (HIL) and hole transport layer (HTL) to enhance the hole injection. The C-V characteristics of the optimized PeLED confirm the reduced injection barrier, enhanced hole injection, and strengthened recombination. As a result, the optimized PeLED shows an improved external quantum efficiency (EQE) from 8.34% to 15.82%, indicating the C-V characteristics can be an efficient method to evaluate the carrier behaviors and to improve the EL performance of PeLEDs.

A standard PeLED is first investigated to find its C-V characteristics. As shown in Fig. 1(a), the typical PeLED is structured as anode/hole injection layer (HIL)/hole transport layer (HTL)/perovskite/electron transport layer (ETL)/cathode. With sufficient forward bias, electrons are injected from the cathode into the conduction band (CB) of perovskite nanocrystals (NCs), while holes are injected from the anode into the valence band (VB) of perovskite NCs, followed by radiative recombination inside the perovskite layer. For this standard PeLED, its capacitance can be defined as $C = dQ/dV$, where dV is a small change in voltage and dQ is the corresponding quantity changes of charge in the device.

For C-V characteristics measurement, a small alternating current (AC) signal with an amplitude of 500 mV and a modulation frequency of 1 KHz is applied. This frequency is lower than the response frequency of carriers. (The order of magnitude for the transport and recombination time of carriers are μs ,^{9,11} corresponding to the response frequency of MHz.) Therefore, it can confirm that all carriers have enough time to response the signal changes and reveal the capacitance changes in detail.

Assuming that the emission of this PeLED is strong enough, and the injection barrier is relatively low, then an ideal C-V curve can be described in Fig. 1(b). There are four regions which can be divided. For region 1, when the applied voltage is close to 0 V, carriers that are injected into the PeLED can be ignored, and the capacitance C_1 of the

PeLED can be regarded as its geometric capacitance C_1 , which is calculated by

$$\frac{1}{C_1} = \frac{1}{\epsilon_0 S} \left(\frac{d_{ETL}}{\epsilon_{ETL}} + \frac{d_{Perovskite}}{\epsilon_{Perovskite}} + \frac{d_{HTL}}{\epsilon_{HTL}} + \frac{d_{HIL}}{\epsilon_{HIL}} \right), \quad (1)$$

where ϵ , S , and d are the relative permittivity, area, and thickness for each layer, respectively, and ϵ_0 is the permittivity of vacuum (supplementary material, Note 1). In this case, the capacitance of PeLEDs is a constant value.

In regions 2–4, carriers are injected into the PeLED with the increase in the applied voltage. Under forward voltage, carriers are injected into the device, and the hole/electron concentration in the HTL/ETL becomes higher. Therefore, the HTL and ETL in PeLEDs trend to become a p-region and an n-region. In this case, the basic equation to describe the capacitance C of the PeLED is given as

$$C = \frac{dQ}{dV} = \frac{dQ_{in} + dQ_{trap} - dQ_r}{dV}, \quad (2)$$

where Q_{in} , Q_{trap} , and Q_r are the total charge quantity of injected carriers, trapped carriers, and recombined (including radiative and nonradiative components) carriers due to the small AC signal, respectively.

For region 2, the applied voltage is relatively small. Since there are energy barriers between two different materials (e.g., barriers between the HIL/HTL interfaces), it is difficult for injected carriers to overcome them. Therefore, in region 2, carriers will be accumulated at the interface between two materials, and the corresponding capacitance C_2 of PeLEDs can be regarded as its barrier capacitance

$$C_2 = S \left| \frac{dQ}{dV} \right| = S \sqrt{\frac{\epsilon_r \epsilon_0 q N_{p-HIL} N_n}{2(N_{p-HIL} + N_n)(V_D - V)}}, \quad (3)$$

where q is the charge quantity, N_{p-HIL} is the hole concentration in the HIL, N_n is the electron concentration in the ETL, and V_D is the built-in voltage, which is determined by the energy levels of the materials and the work function of the electrodes (supplementary material, Note 2). In this region, with the injection of carriers, carriers accumulated in the device are slowly increased. Therefore, C_2 shows a slight rise with the increase in the applied voltage.

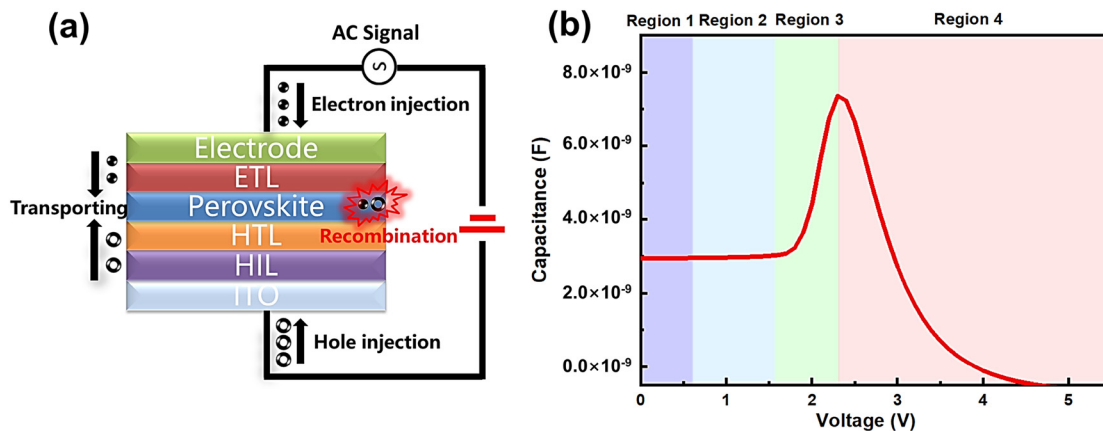


FIG. 1. (a) Schematic of the PeLED structure. (b) Typical C-V curve of a PeLED.

Once the applied voltage is high enough, Eq. (3) will be invalid, and the C-V curve needs to be analyzed in region 3. Here, the increase in voltage helps more and more carriers overcome energy barriers in the device and leads to the carrier diffusion and transport in PeLEDs. Capacitance C_3 of PeLEDs can be regarded as the diffusion capacitance

$$C_3 = S \frac{dQ_{total}}{dV} = \frac{d(Q_n + Q_p)}{dV} = Sq^2 \frac{[n_{p0}(L_n + L_{perovskite}) + p_{n0}L_p]}{k_0T} \exp\left(\frac{q(V - V_D)}{k_0T}\right), \quad (4)$$

where p_{n0} is the hole concentration in the ETL and n_{p0} is the electron concentration in the HTL. L_n and L_p are the length of the ETL and HTL, respectively, and $L_{perovskite}$ is the length of the perovskite layer. k_0 is the Boltzmann constant, and T is the temperature (supplementary material, Note 3). In this case, the carrier is injected into the transport layer and transported to the perovskite layer mainly by carrier diffusion. The rise rate of C_3 presents the carrier transporting capability. Importantly, for PeLEDs, majority carriers are believed to be injected first, and then minority carriers are injected and recombined with majority carriers. Therefore, C_3 describes the strong influence of majority carriers transported on capacitance, followed by the significant injection of minority carriers and recombination in region 4.

For region 4, the applied voltage reaches the turn-on voltage of PeLEDs, and minority carriers are injected into the perovskite layer and recombined with majority carriers. According to the definition, carrier recombination and consumption happen since the start point of region 4, while charges keep being accumulated during region 3. Therefore, the maximal rate of charge increase will exist at the start point of region 4. Based on Eq. (1), a peak capacitance value C_p will, hence, occur at the start point of region 4. Meanwhile, the start points of region 4 correspond to the turn-on voltage of PeLEDs. (Here, the turn-on voltage is defined as the applied voltage when the recombination begins.) Therefore, the corresponding voltage of the location of C_p should be the turn-on voltage of PeLEDs. Furthermore, capacitance tendency in region 4 simultaneously depends on the charge injection and consumption. To better analyze this issue, C_r is defined here as the capacitance change due to recombination (including radiative and nonradiative components)

$$C_r = \frac{dQ_r}{dV}. \quad (5)$$

C_r can be calculated according to the optical power spectrum and external quantum efficiency (EQE)

$$C_r = \frac{Aq}{h} \frac{\partial \left[\frac{\eta_{extraction}\eta_{injection}}{EQE(V)} \int_{\lambda_1}^{\lambda_2} \frac{P(\lambda, V)}{v(\lambda)} d\lambda \right]}{\partial V}, \quad (6)$$

where $P(\lambda, V)$ is the light power, h is the Planck constant, $\eta_{extraction}$ is the extraction efficiency, $\eta_{injection}$ is the injection efficiency, $v(\lambda)$ is the frequency of light with wavelength λ , and A is a constant (supplementary material, Note 4). Then, capacitance C_4 of PeLEDs can be regarded as the summation of the diffusion capacitance C_d (for charges injected and accumulation) and C_r by

$$C_4 = C_d - C_r. \quad (7)$$

According to the definition of C_d , it has the similar expression like Eq. (4), and C_4 can be further described in detail by

$$C_4 = Sq^2 \frac{n_{p0}(L_n + L_{perovskite}) + p_{n0}L_p}{k_0T} \exp\left[\frac{q(V - V_D)}{k_0T}\right] - \frac{Ae}{h} \frac{\partial \left[\frac{\eta_{extraction}\eta_{injection}}{EQE(V)} \int_{\lambda_1}^{\lambda_2} \frac{P(\lambda, V)}{hv(\lambda)} d\lambda \right]}{\partial V}. \quad (8)$$

Based on Eq. (7), it can be easily found the increment part (C_3) and decrement part (C_r) jointly control the position and magnitude of C_p as well as the capacitance tendency in region 4. For PeLEDs with a relative high injection barrier and low mobility of the transport layer, they will have relatively weak emission and high turn-on voltage. In this case, charge accumulation at the barrier and slow transport rate leads to relatively high value C_3 and low value C_r . Therefore, C_p will be high and C_4 would continue increasing due to $C_3 > C_r$. In contrast, PeLEDs with the lower injection barrier and enhanced carrier injection show lower C_p as well as decreased C_4 . Furthermore, once the emission of the PeLED is strong enough, C_4 even can be a negative value due to $C_r > C_3$.

Based on discussions about C-V models, we find that the low frequency C-V analysis can be an effective strategy to evaluate EL performance (e.g., injection barrier, injection rate, and emission). Therefore, it was implemented here to guide the design and optimization of the PeLEDs to improve their EL performance.

First, a typical PeLED was fabricated and analyzed here. The device structure is demonstrated in Fig. 2. The typical PeLED was fabricated using the FAPb_{0.7}Sn_{0.3}Br₃ perovskite nanocrystal²² (20 nm) with the device structure of indium tin oxide (ITO, 80 nm)/poly (3, 4-ethylene-dioxythiophene): poly (styrenesulfonate) (PEDOT: PSS, 40 nm)/poly(9-vinylcarbazole) (PVK, 30 nm)/FAPb_{0.7}Sn_{0.3}Br₃ perovskite (20 nm)/1,3,5-Tris (1-phenyl-1H-benzimidazol-2-yl)benzene (TPBi, 40 nm)/lithium fluoride (LiF, 1 nm)/Al (100 nm).

To verify the C-V modeling and evaluate the EL performance of this typical PeLED, the C-V and L-V characteristics of as-fabricated PeLEDs were measured first. As shown in Fig. 3, the C-V curve shows relatively good agreement with our model before its peak capacitance. When the applied voltage is small (<0.5 V), there are only few carriers injected into the device, so the capacitance is almost a constant. The measured capacitance of this PeLED was 1.58 nF, while the calculated result based on Eq. (1) was 1.55 nF. With the increase in the applied voltage (0.5–2 V), majority carriers are slightly injected into the device, and the capacitance keeps increasing slowly, which corresponds to region 2 [barrier capacitance, described in Eq. (3)]. During the higher applied voltage (2–3.9 V), the capacitance shows a rapid increase due to the strong injection of majority carriers, which corresponds to region 3. This process is described in Eq. (4).

Then, a peak capacitance occurs at the turn-on voltage (the applied voltage when the luminance of the device reaches 0.1 cd/m²) of the PeLED ($V_{th} = 3.9$ V). Interestingly, after this peak capacitance, the capacitance decreases from 3.9 to 4.75 V, then it increases again. These performances can be well explained by our C-V modeling.

During 3.9–4.75 V, once the voltage reached 3.9 V (turn-on voltage), carriers in the HTL and ETL are reduced because they are transported into the perovskite layer and start to be recombined. This reduction of carriers in the HTL and ETL leads to the slower

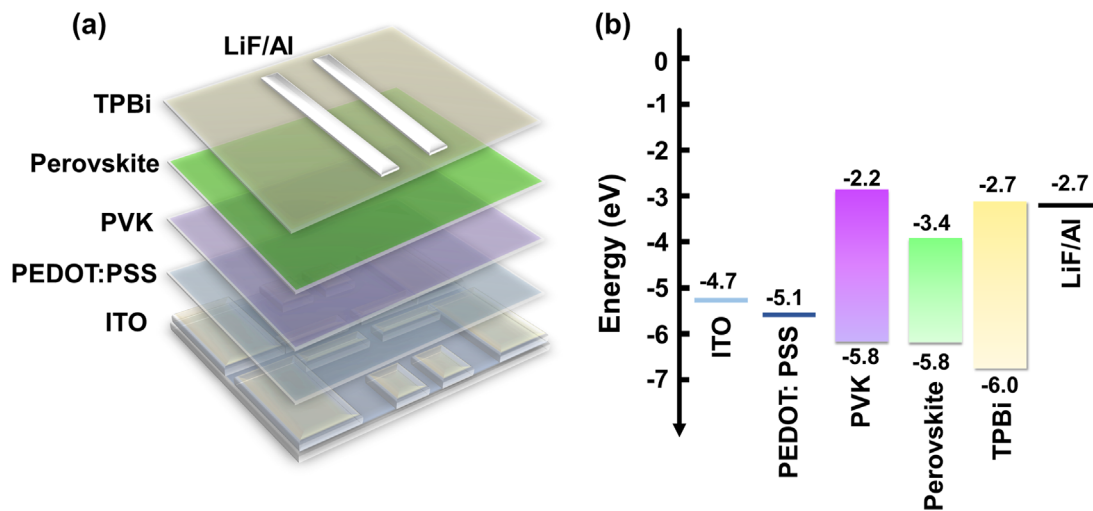


FIG. 2. (a) Device structure of a typical PeLED. (b) Energy levels of the as-fabricated LED.

increase in C_3 . Meanwhile, high increase rate of recombination leads to high C_r . According to Eq. (7), the capacitance will decrease from 3.9 V. There is a trough at around 4.75 V. After 4.75 V, the capacitance increases again. Two problems would lead to this result: (1) The increase rate of recombination is low, so C_r was not high enough; (2) the carrier accumulation in the device becomes serious so C_3 shows rapid growth.

For these PeLEDs, the injection of electrons is stronger than holes due to the negligible electron injection barrier and high mobility of the ETL (around $10^{-4} \text{ cm}^2/(\text{Vs})$). As discussed above, the measured C-V curve not only certifies our modeling but also reveals the key issues in this device: a high hole injection barrier between PEDOT:PSS and PVK (0.7 eV) and a low hole mobility of PVK [$10^{-6} \text{ cm}^2/(\text{Vs})$] lead to relatively low hole injection rate. Therefore, the increase rate of recombination in the perovskite layer is relatively weak, and Q_r is low.

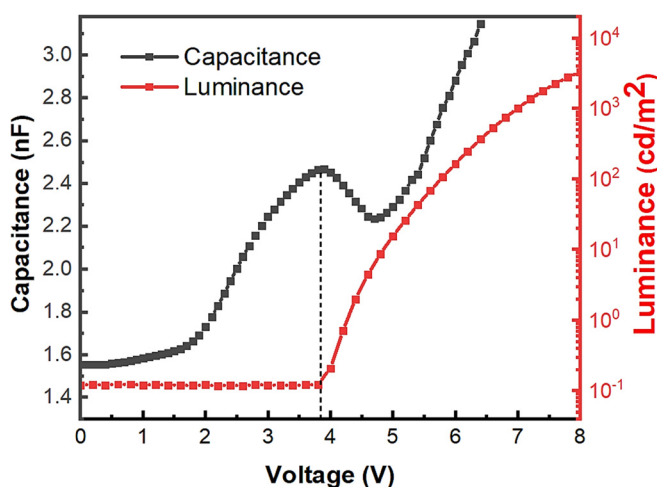


FIG. 3. C-V and luminance vs voltage (L-V) characteristics of the as-fabricated PeLED.

On the contrary, under high applied voltage, uncombined carriers continually accumulate at the interface between the perovskite layer and transport layers. As described in Eq. (2), Q_{in} as well as Q_{trap} kept increasing, and Q_r kept at a low level. Therefore, after 4.75 V, the capacitance increased again.

Based on issues presented by the C-V curve, the optimization for this device should include two parts: (1) The hole injection barrier needs to be reduced, so that the hole injection will be enhanced, and the accumulation of holes at the interface will be reduced; and (2) the hole concentration in HTL needs to be increased, then the hole and electron in the device can be more balanced (confirmed in Fig. S5), and the rate of radiation recombination will be increased. An optimization strategy is proposed as shown in Fig. 4(a). One MoO_3 interface layer is designed between PEDOT:PSS and PVK (the optimized thickness of MoO_3 was determined as 1.5 nm, analyzed in Fig. S2). Due to the deep conduction band minimum (CBM) of MoO_3 (-6.7 eV), some electrons in PVK are transferred to MoO_3 and trapped here. Every transported electron in MoO_3 has a corresponding hole in PEDOT:PSS or PVK, and electric dipoles are, thus, formed at the interfaces due to the electron-hole pairs, which leads to a stronger electrical field at PEDOT:PSS/ MoO_3 and PVK/ MoO_3 interfaces. This interfacial electrical field facilitates holes transporting from the HIL to HTL. Meanwhile, due to the transfer of electrons, hole concentrations in PVK will increase, which further facilitate the transport of holes to the perovskite layer. Moreover, the modification of MoO_3 on PEDOT:PSS dramatically reduces the hole injection barrier between PEDOT:PSS and PVK. Therefore, the designed MoO_3 interface layer enhances the hole injection, increases the hole concentration in PVK as well as PEDOT:PSS, and reduces the hole injection barrier. Aside from this, other materials (e.g., HAT-CN) with deep CBM (or LUMO) can also enhance hole injection like MoO_3 .

C-V curves of PeLEDs are shown in Fig. 4(b), where the red/black curve represents the PeLED with/without MoO_3 , respectively. Under a very small voltage ($<0.5 \text{ V}$), the geometric capacitances of two devices are almost same. As described in Eq. (1), this capacitance value is depended on materials themselves. The introduction of the

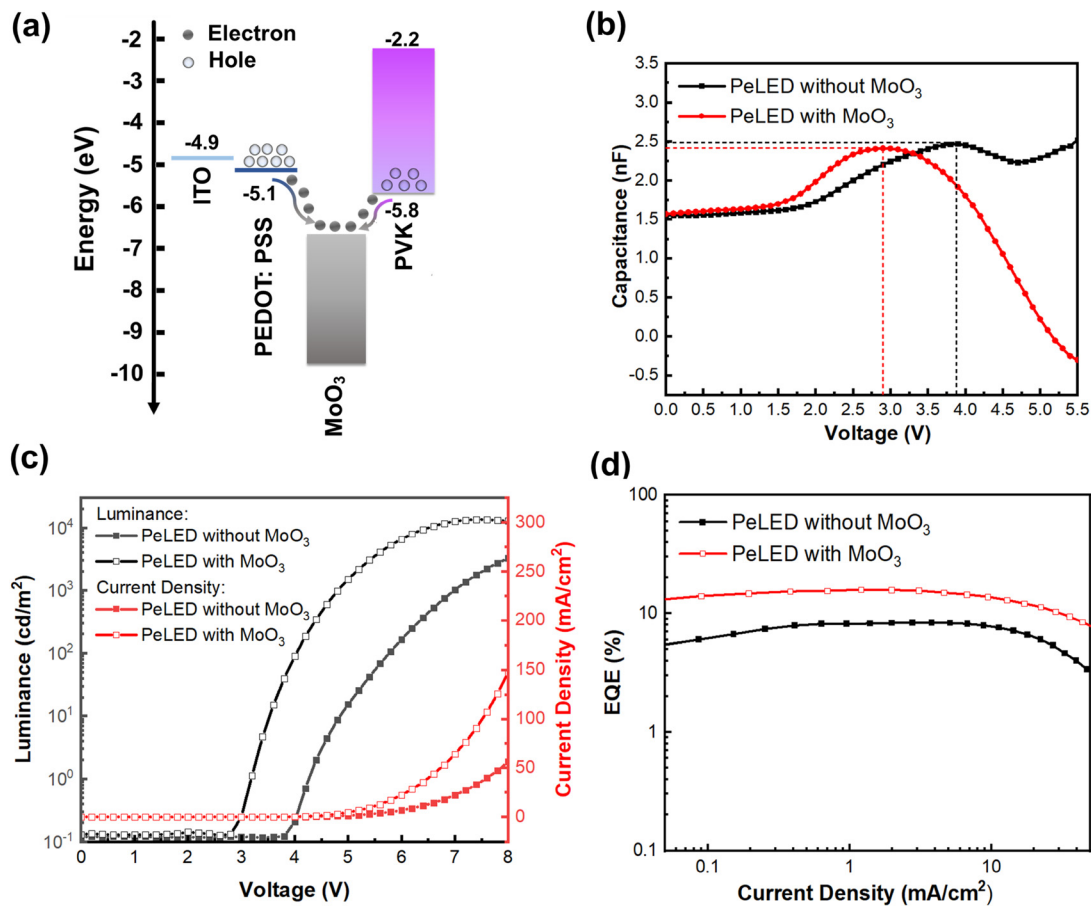


FIG. 4. (a) Energy levels of PeLEDs with the MoO₃ interface layer, (b) C–V curves, (c) J–L–V curves, and (d) EQE curves of devices with and without the MoO₃ interface layer.

MoO₃ interface layer does not bring significant difference in geometric capacitances due to its extremely thin thickness. When the voltage is higher than 0.5 V, both of two devices show increasing capacitance. Particularly, the red curve rises faster than the black curve. As described in Eqs. (3) and (4), carriers are injected in devices, and a larger number of injected carriers lead to the faster rise rate. Since there are the same device structure for electron injection, the electron injection with and without MoO₃ keep unchanged. Therefore, faster rise of the red curve can only be explained by the enhanced hole injection. Meanwhile, the C_p of the red curve (≈ 2.85 V) is obviously lower than that of the black curve (≈ 3.85 V). Also, the voltage corresponding to C_p of the red curve (≈ 2.42 nF) is lower than that of the black curve (≈ 2.50 nF). As discussed in Eqs. (7) and (8), this lower C_p and the corresponding voltage in the red line indicate the lower hole injection barrier and stronger recombination rate. After the C_p , the black curve drops and then rises again due to the serious accumulation of carriers (Fig. S4). However, the red curve keeps declining, and finally, its capacitance becomes a negative value. According to Eq. (7), this negative capacitance indicates a relatively low C_3 and high C_r . In detail, relatively low C_3 means MoO₃ alleviate the hole accumulation at the

PEDOT:PSS/PVK interface. While relatively high C_r means MoO₃ help enhancing the hole injection, realizing stronger recombination in perovskites.

EL performance of devices further confirms the analysis of C–V curves. Figure 4(c) shows the current density–voltage and luminance–voltage characteristics. The MoO₃ based PeLED shows much higher current density (triple times increase at 8 V), and the maximum luminance increases from 5129 to 13610 cd/m², showing a 2.65 times improvement. Meanwhile, the turn on voltage (V_{on}) decreased from 3.8 to 2.8 V due to the reduced hole injection barrier and improved hole injection. As demonstrated in Fig. 4(d), with the implementation of the MoO₃ interface layer, the EQE increases from 8.34% to 15.82%. The PL, EL spectra of the proposed PeLEDs are shown in Fig. S3. In addition, the T_{50} operation lifetime is also improved from 8.39 to 16.02 min, showing the better stability (Fig. S1). As analyzed by C–V curves, these improvements mainly attributed to the enhanced hole injection and efficient recombination. Therefore, the optimization for PeLEDs by introducing MoO₃ has been theoretically predicted, analyzed, and experimentally proved by the C–V analysis.

In summary, a C–V model for PeLEDs is built to establish the relationship between capacitances with carrier behaviors. The carrier behaviors in PeLEDs, including carrier injection, transportation, and recombination, are clearly analyzed by the model. Aside from that, the C–V model is used to guide the optimizations of EL performance of PeLEDs. The measured C–V characteristics of a typical PeLED show the issues of the high hole injection barrier and insufficient recombination. For addressing these issues, a MoO₃ interface layer is inserted between the HTL and HIL to enhance the hole injection. The C–V characteristics of the optimized PeLED confirm the reduced injection barrier, enhanced hole injection, and strengthened recombination. As a result, the optimized PeLED shows an improved EQE from 8.34% to 15.82%, indicating the C–V characteristics can serve as an efficient method to evaluate the carrier behaviors and improve the EL performance of PeLEDs.

See the [supplementary material](#) for more details of experimental procedures and other information.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

X.X. and T.Y. contributed equally to this work.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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