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Electrical conduction mechanisms of CdTe quantum dots/p-si heterojunction

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ABSTRACT

CdTe quantum dots (QDs) are prepared on p-Si substrates using thermal evaporation technique. Current–voltage (I–V) characteristics of Au/CdTe QDs/p-Si/Al heterojunction are measured in a temperature range 304–368 K. The results show that the device has a rectification behavior with a rectification ratio being 275 at ± 1.5 V. We determine the electrical conduction mechanisms of the heterojunction. At forward voltages $V < 0.3$ V, the thermionic emission becomes the main mechanism, where in this voltage range, it is possible to estimate the barrier height and the ideality factor. At a forward voltage range $0.5 < V < 0.9$ V, the conduction mechanism turns into the space charge limited conduction which is dominated by an exponential trap distribution (TSCLC). Within this voltage range $0.5 < V < 0.9$, the total density of the trap states is calculated. At forward voltages $0.95 < V < 1.5$ V, Poole-Frenkel conduction mechanism fits well with the experimental data. It is found that there are two trap levels with zero fields of the activation energy which have values 0.16 and 0.46 eV. At the reverse applied voltages, it is also found that the main source of the reverse current is the generation-recombination through p-Si rather than through the interface of the thin film itself.

1. Introduction

Cadmium telluride (CdTe) is an essential material in solar cell technologies because it has a direct band gap, which has a value 1.44 eV [1]. This direct band gap can be tuned by quantum confinement. CdTe is also a significant in solar cell applications due to the reported value of the electrical conversion efficiency 16.5% [4]. For this purpose polycrystalline CdTe thin films have been prepared by different methods such as closed-space sublimation [2] and chemical vapor deposition [3]. Recently, an extensive attention has been paid to the development of solar cells based on nano-crystals or quantum dots (QDs) [5]. An advantage of the use of (QDs) comes due to the fact that a control of particles' size and shape can optimize the properties of the resultant semiconductors. Quantum dots (QDs) also show a high efficiency multiple exciton generation [6]. CdTe quantum dots is a good candidate for solar cell applications, which has been investigated in a previous work [5]. CdTe (QDs) also attracted much attention due to their unique properties, where the effective optical path for absorption is much greater than the actual film thickness. Thus, light generated electrons and holes needs to travel a short path and the recombination losses are greatly reduced. As a result, the absorber layer thickness in nanostructure solar cells can be as thin as 150 nm instead of several micrometers in microstructure thin film solar cells [7,8]. Previous studies show that the conduction mechanisms in CdTe junctions can be thermionic emission type [9] or a space charge limited conduction (SCLC),

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which is normally dominated either by traps located at a discrete energy level [10,11] or by traps distributed exponentially within the band gap [11–13]. Additionally, it is seen that both traps types belong to the space charge limited conduction can be presented but each one becomes a dominant in a certain voltage range [14]. Investigations of the conduction mechanisms of CdTe device also show a field lowering conductivity of the Poole-Frenkel type [15,16]. Several studies on evaporated nano-particles are found to maintain their structural properties [5,17]. CdTe/p-Si heterojuction has been reported in several studies which demonstrate that this device acts as a photo sensor in visible and near infrared regions [18]. This result confirms that CdTe is a promising material for silicon optoelectronic devices [18].

In this paper Au/CdTe QDs/p-Si/Al heterojunction, which is seldom found in literature, is fabricated. The junction properties and the electrical conduction mechanisms are investigated by facile current–voltage (*I–V*) characteristics in a temperature range (304–368 K).

2. Experimental

CdTe quantum dots powder have been synthesized in Nano-Tech Egypt laboratories *via* the hot-injection technique which is the pioneering work of Murray et al. [19]. The silicon samples used in this study were [100] oriented P-type CZ wafers with resistivity ranging from 2 up to 5 Ω. cm with a thickness of 450 μm. The samples were textured for 30 min in HF: HNO_3: CH_3COOH texturing solution in ratio of 1:6:1. Silicon substrates were rinsed in de-ionized water and dried in the presence of nitrogen gas. The preparation of the heterojunction has been done in the next procedures. The back electrode has been evaporated on one side of Si wafer by high vacuum coating unit (Edwards, E306A). The vacuum chamber was pumped down to vacuum of 5×10–5 Torr. CdTe quantum dots have been evaporated using molybdenum boat heater onto glass and p-Si substrates, where the temperature is fixed at room temperature. Structural and optical properties of the investigated CdTe(QDs) thin film have been studied in a previous work [5]. The film thickness was controlled by using quartz crystal thickness monitor (Edwards FTM4). The deposition rate was adjusted at 2 Å/s. CdTe quantum dots film has been coated with gold (Au) to be used as a top electrode. Fig. 1 indicates the schematic diagram of Au/CdTe QDs/p-Si/Al heterojunction.

The dark (current-volt) characteristics of Au/CdTe QDs/p-Si/Al heterojunction have been carried out in a compact furnace at temperature rang 304–368 K using a high impedance electrometer (Keithley 617) as a voltage source and a current meter.

3. Results and discussion

3.1. Dark electrical properties

The dark (current–volt) characteristics of Au/CdTe QDs/p-Si/Al heterojunction device have been measured at different temperatures (304–368 K) as shown in Fig. 2. The curves exhibit diode-like behavior, which can be recognized by the formation of a barrier at the interface that limits the flowing of the forward and reverse carriers across the junction where the built in potential barrier could be investigated. At a fixed bias potential, the current increases with increasing temperature indicating that CdTe QDs's behave as a semiconductor material. The weak voltage dependence of the reverse bias current as well as the strong voltage dependence of the forward bias current is characteristics of good rectification performance for a junction interface.

3.2. Dark current parameters

3.2.1. Rectification ratio

The rectification ratio (*RR*) for the junction is defined as the ratio of the forward current to reverse current at a certain value of the applied voltage ($RR=(I_F/I_R)$ $V=const$). Fig. 3 indicates that this parameter is an important parameter that points out how the junction is good enough to rectify the current. The calculated value of *RR* for Au/CdTe QDs/p-Si/Al equal 275at $V=\pm 1.5$ V, which is similar to that observed by A.A. El-Gamdi *et al.* [20].

3.2.2. Series resistance

At sufficiently high forward bias, the junction resistance approaches a constant value which is the series resistance, R_s. The series resistance is known as the voltage independent resistance, which is determined by the sum of the resistances of the quasi neutral region, the back contact as well the contacting wires [21]. The total junction resistance is the sum of the resistance of space charge region (R_d) plus series resistance (R_s) plus CdTe QDs resistance($R_{CdTe\ QDs}$). The voltage dependence of the junction resistance is shown in Fig. 4 (where $R_j=(\delta V/\delta I)$) in a forward direction. At low forward bias the resistance of the depletion region is the dominating one. It is seen by the exponential decrease in the differential resistance with the increasing forward bias. As the applied forward bias becomes higher than the built-in voltage the width of the depletion region R_d turns out to be negligible and it does not limit the forward current under these conditions the series resistance is the dominant. As indicated in Fig. 4, the junction resistance does not become saturated at high forward bias. Also the inset of Fig. 4 shows that the series resistance decreases in the

Fig. 1. A schematic diagram of Au/CdTe QDs/p -Si/Al device.

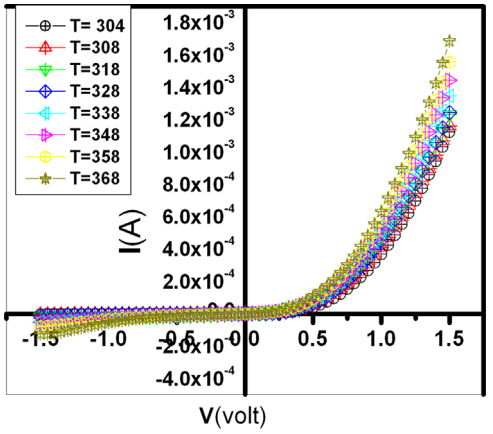

Fig. 2. (*I, V*) characteristics at the temperature range (304–368 K).

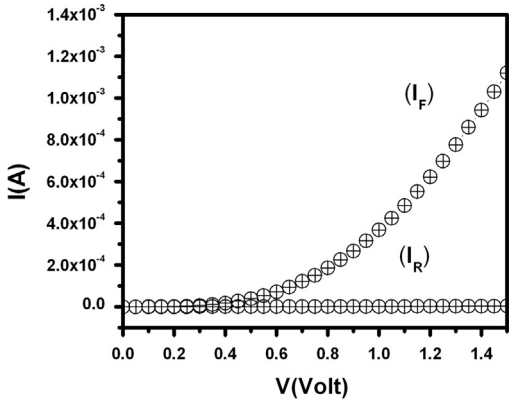

Fig. 3. *I* (*A*) (forward and reverse) versus the applied voltage (Volt).

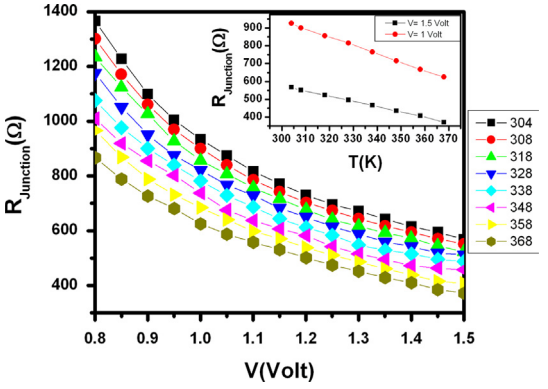

Fig. 4. The junction resistance ($R_{Junction}$) versus the applied voltage at forward bias. (The inset Fig.4. The relation between the obtained series resistance and temperatures).

temperature range at fixed values of the voltage at 1and 1.5 V. This behavior provides evidence that the series resistance R_s is not a dominating one.

3.2.3. Shunt resistance

On the other hand, the shunt resistance (R_{sh}) or dynamic resistance at zero voltage [22] can be determined by applying small voltage to the junction. Shunt resistance is a voltage dependent and it depends on the active area of the diode. Mechanisms related to shunt resistance are comprised of a multistep tunneling and thermal trapping-detrapping of carriers within the defect states in the space-charge region [23]. Shunt resistance can also calculated from junction resistance at a reverse small applied voltage, where $R_j=(\delta V/\delta I)$. Fig. 5 shows that the junction resistance decreases as the applied voltage and the temperature increase. The calculated value of shunt resistance at low applied reverse voltage equal (R_{sh}=685 k Ω at 0.05 V *at* $T=304$ K).

3.3. Dark conduction mechanisms

The information about conduction mechanisms can be obtained from Fig. 6 which indicates a presence of three distinct regions characterizing three different conduction mechanisms.

3.3.1. At low voltage region I [$V \leq 0.3$ V]:

The current varies exponentially with the applied voltage, which can be given by a standard diode equation [24]:

$$I_{F1} = I_{S1}\left[\exp\frac{qV}{n_1 k_B T} - 1\right] \quad (1)$$

where I_{F1} is the forward current in the region *I*, n_1 is the ideality factor in the region *I*, k_B is the Boltzmann constant, I_{S1} is the reverse saturation current, q is the electron charge and V is applied voltage. According to Eq. (1) the parameters (I_{S1} and n_1) can be determined from intercepts and slopes of straight lines in Fig. 6 in the region I. The calculated value of the ideality factor (n_1) at room temperature equals 2.6.The deviation of the value of the ideality factor from unity maybe attributed to the recombination of electrons and holes in the depletion region [25]. In order to identify the dominant current transport mechanism through the device in this region of the applied voltage the following relations $ln(I_{S1})$, $ln(I_{S1}/T^2)$, $ln(I_{S1}/T^{3/2})$ and $ln(I_{S1}/T^3)$ as a function of reciprocal temperature were examined. Only, $ln\ (I_{S1}/T^2)$ versus $1000/T$ gives a straight line as shown in Fig. 7. This result indicates that thermionic emission is the dominant mechanism of charge transport [26] and can be represented by the

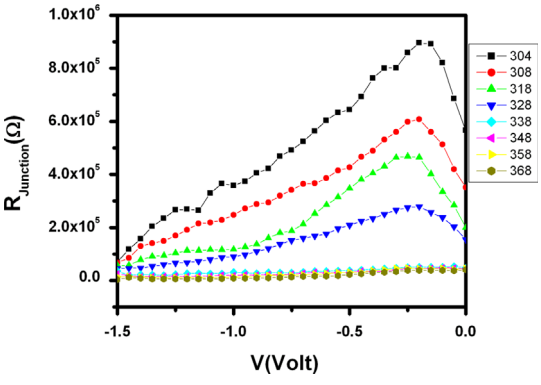

Fig. 5. The junction resistance versus *V* at a reverse direction.

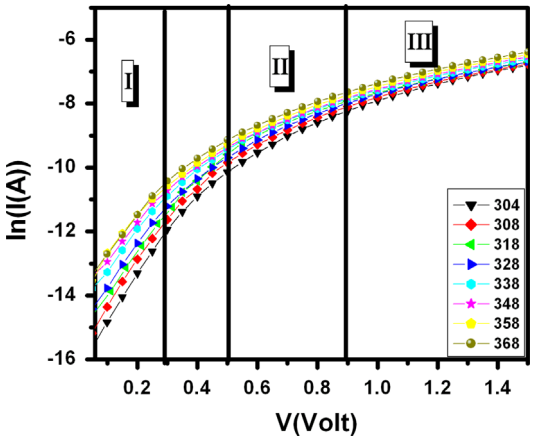

Fig. 6. The relation between $ln(I)$ and applied voltage in forward bias at the temperature range (304–368 K).

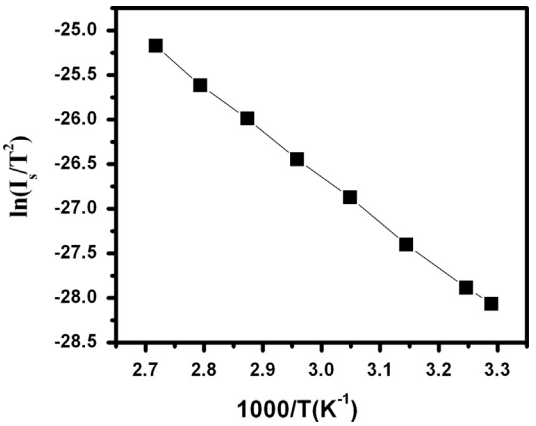

Fig. 7. Plot of $ln(I_{S1}/T^2)$ versus $1000/T$.

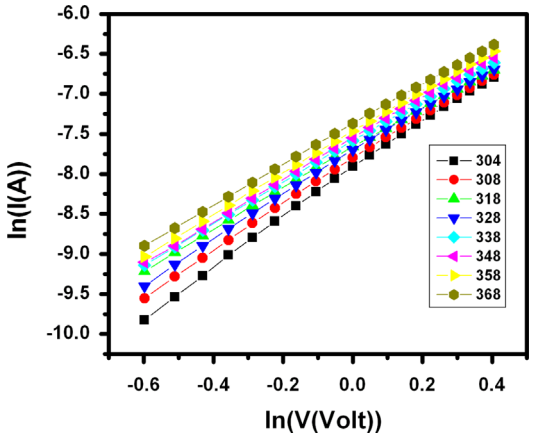

Fig. 8. The Power law exponent of the junction at $(0.5 \le V \le 0.9$ volt).

following relation [27]:

$$I_{S1} = AA^*T^2 \exp\left[\frac{-q\phi_B}{k_B T}\right], \quad (2)$$

where A is junction area, A^* is Richardson constant and ϕ_B is the barrier height. The barrier height is determined from the slope of the straight line that is given in Fig. 7. It is found that the barrier height equals 0.44 eV.

Table 1
The obtained values of exponent m, characteristic temperature of the exponential trap distribution T_c, n_t traps level per unit energy and total traps concentration N_t.

T (K)	m	T_c	$\alpha_\circ$ ($m^2\,KV^{-1}$)	n_t($J^{-1}\,m^{-3}$)	N_t(cm^{-3})
304	3	608	3.9×10^{-11}	2.99×10^{41}	2.5×10^{15}
308	2.78	547	3.4×10^{-11}	3.4×10^{41}	2.6×10^{15}
318	2.51	479.86	3.6×10^{-11}	3.26×10^{41}	1.9×10^{15}
328	2.69	553.66	3.5×10^{-11}	3.33×10^{41}	2.5×10^{15}
338	2.54	518.83	3.16×10^{-11}	3.7×10^{41}	2.6×10^{15}
348	2.58	549.84	3.2×10^{-11}	3.6×10^{41}	1.9×10^{15}
358	2.56	558.48	2.3×10^{-11}	3.5×10^{41}	2.69×10^{15}
368	2.5	556.05	2.3×10^{-11}	3.6×10^{41}	2.7×10^{15}

3.3.2. At region II ($0.5 \le V \le 0.9$ V)

Another mechanism is supposed to be the dominant in the voltage range $0.5 \le V \le 0.9$ V. The current shows power law behavior of the form of $I \sim V^m$ *as indicated in* Fig. 8. The calculated values of the exponent (m) are listed in Table 1. It is noticed from Table 1 that the carrier transport is controlled by a set of traps known by space charge limited conduction dominated by exponential trap distribution (TSCLC). The traps originate during the growth of the films or may be from grain boundaries that do not have the benefit of passivation which are from ligands of capping material (TOP). The increase in density of the unpassivated long-range crystalline defects results in an increase in the mid-gap trap density acting as trapping centers for the carriers. The variation of the number of traps (n_t) per unit energy range is given by

$$n_t = (n_{\circ t}/k_B T_c)\exp[-(E_v - E)/k_B T_c, \quad (3)$$

where T_c is the characteristic temperature of the exponential trap distribution for which $m = L + 1 with\ L = T_c/T$, n_{ot} is the initial value and E_v valance band energy.

Assuming that the Fermi level lies in the middle of the uniform distribution of traps states per unit energy rang, n_t. The carrier density (p) at the valance band at an applied voltage V is given by [28]:

$$P = P_0 \exp(\alpha_0 V/Td^2), \quad (4)$$

where P_0 is the equilibrium carrier concentration within the valance band and d is thickness of the active layer and the parameter α_0 is expressed as:

$$\alpha_\circ = \varepsilon\varepsilon_0/qn_t k_B \quad (5)$$

where $\varepsilon = 2.93$ is dielectric constant which is calculated from optical measurement [5] and ε_0 is permittivity of a free space. Now, following Rose [29], the modified expression of the space charge limited current is given by:

$$I = 9/8(\mu P_0 qV)/d[\exp(\alpha_0 V/Td^2)]. \quad (6)$$

Where μ is the hole mobility. The value of α_0 can be calculated from the slope of the variation of $ln(I/V)$ with V as indicated in Fig. 9. The values of α_0 at different temperatures are given in Table 1. Thus, upon substituting the value of α_0 in Eq. (5), the values of n_t can be calculated. These calculated values of n_t are given in Table 1. It should

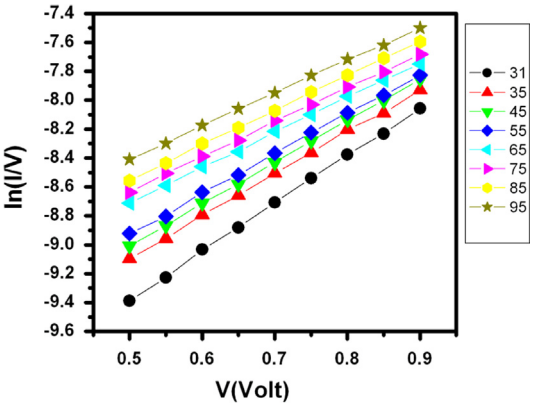

Fig. 9. Variation of $ln(I/V)$ with the voltage.

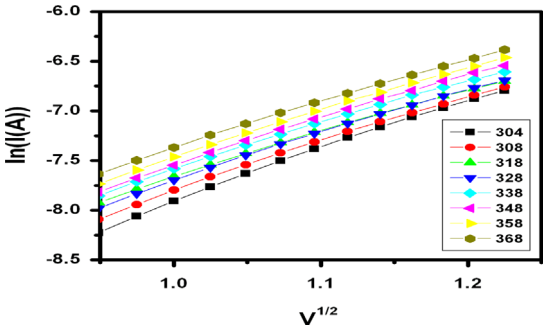

Fig. 10. Variation of $ln(I)$ with square root of the applied voltage showing the fit to Schottky conduction mechanism in region III.

be mentioned that although Eq. (6) suggests a strong dependence of the space charge limited current on the temperature, it is observed that relative high values of trap states n_t makes the value of α_0 sufficiently small so the TSCLC show much less dependence on temperature. The total density of trap state is given by:

$$N_t = n_t k_B T_c \tag{7}$$

The calculated values of N_t, which are given in Table 1, show less dependence on temperature. The obtained value of N_t is less than the obtained value for microstructure CdTe by Basol *et al.* [30] which equal to 7×10^{15} cm^{-3}and the obtained by A Pal. J Dtta *et al.* [28] which equal 5×10^{15} cm^{-3}. Similar observation by A. Bezryadina, *et al.* [30] for nanostructure CdTe. Bezryadina, *et al.* [31] stated that the low trap density in the nanoparticle films shows that the ligands are effective at electrically passivating the surface of the nanoparticles and the nanoparticles themselves have a low mid gap trap density. The very large surface area of the nanoparticle films does not appear to introduce more trap states relative to microstructure so Ligands in nanoparticle based films are very effective at reducing the number of mid-gap trap states in photodetectors devices.

3.3.3. *The third region ($0.95 \leq V \leq 1.5$ V)*

Among all the possible mechanisms, it was observed that the data fit well both Schottky (Fig. 10) and Poole-Frenkel conduction (Fig. 11). It is often difficult to

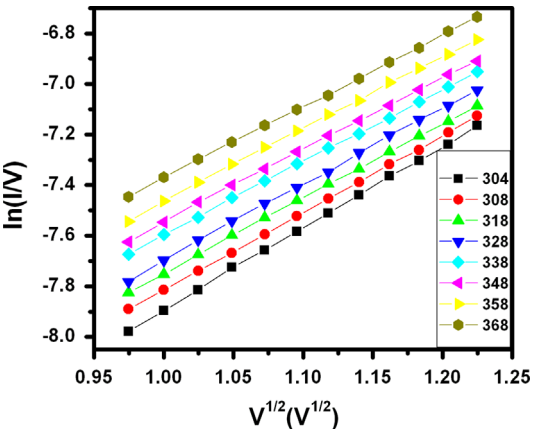

Fig. 11. Variation of ln(I/V) with square root of the applied voltage showing the fit to Poole-Frenkel conduction mechanism in region III.

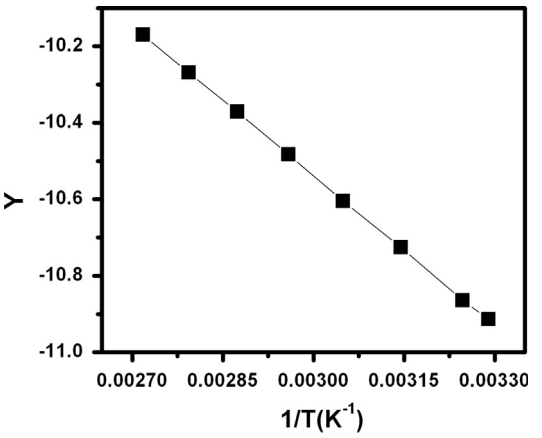

Fig. 12. Variation of Y against $1/T$.

distinguish between Poole-Frenkel and Schottky conduction in several works [24,25,32–36].

In case for Schottky conduction [36]:

$$I = AA^*T^2 e^{(-E_s/K_BT)} e^{(n/k_BT)(e^3\eta/4\pi\varepsilon\varepsilon_s d)^{1/2}V^{1/2}} \tag{8}$$

Where A is the device area, A^* is Richardson constant and n, η are parameters depending on the type of transport E_0 is the zero field of the activation energy which given by the bias assisted lowering of the trap energy equation [36]:

$$E = E_0 - n\left(\frac{e^3\eta}{4\pi\varepsilon\varepsilon_0 d}\right)^{1/2} V^{1/2} \tag{9}$$

In the case of Poole-Frenkel conduction [36], the current is given by:

$$I = G_0 V e^{(-E_0/k_BT)} e^{(n/k_BT)(e^3\eta/4\pi\varepsilon\varepsilon_s d)^{1/2}V^{1/2}} \tag{10}$$

where G_0 is the conductance of the sample so Eq. (7) can be simplified as:

$$\ln(I/V) = Y + ZV^{1/2} \tag{11}$$

Where Y is the intercept and equal:

$$Y = \ln(G_0) - \frac{E_0}{k_BT} \tag{12}$$

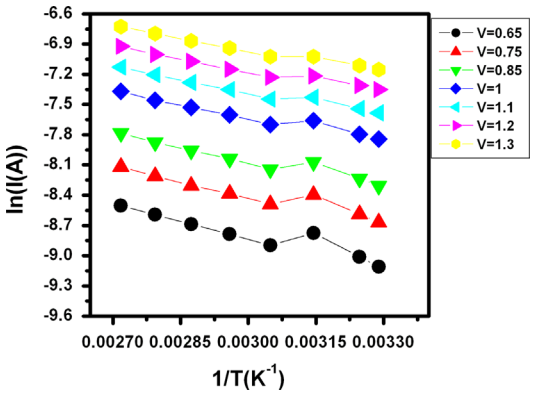

Fig. 13. Variation of $ln(I)$ against $1/T$ for different biases voltage.

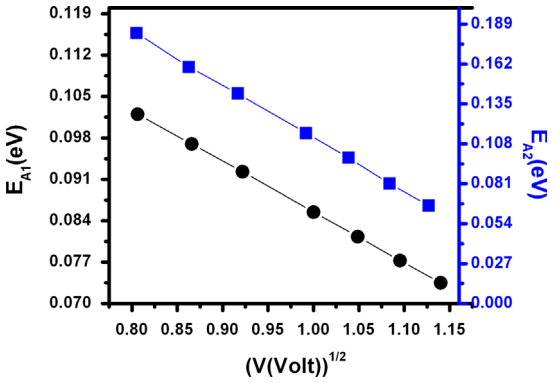

Fig. 14. The activation energies against square root of the corresponding voltage.

Table 2
Activation energies of the two trap levels ($E_{A1} \geq 358$ K *and* $E_{A2} \leq 348$ K) dependence on the voltage.

V(V)	E_{A1}(eV)	E_{A2}(eV)
0.65	0.102	0.2
0.75	0.096	0.16
0.85	0.0918	0.14
1	0.083	0.11
1.1	0.0814	0.092
1.2	0.0795	0.081
1.3	0.077	0.076

And Z is the slope:

$$Z = n/k_B T\left(\frac{e^3\eta}{4\pi\varepsilon\varepsilon_\circ d}\right) \tag{13}$$

The closer examination of the Fig. 10 and Fig. 11 reveal that $ln(I/V)$ against $V^{1/2}$ plot gives better linear fit as compared to $ln(I)$ against $V^{1/2}$. Following that, plotting Y against $1/T$ according to Eq. (12) at Fig. 12 gives the value of E_0 which found to equal 0.1 eV.

3.3.4. Activation energy

The current–voltage dependence of the device can be expressed as:

$$I\alpha e^{(-E_A/k_B T)}, \tag{14}$$

where E_A is the activation energy. Fig. 13 shows the relation between $ln(I)$ and reciprocal of temperature at different voltage to evaluate the activation energy E_o. As shown from Fig. 13 that the curves exhibits two slopes ($T \geq 358$ K and $T \leq 348$ K) which attributed to the presence of two traps level with activation energies are listed in Table 2 for different bias voltages. It is clear that the activation energy decreases with the applied biasing voltage. As sequences, plot of E_A against $V^{1/2}$ should be a straight line and the intercept gives the value of the zero field value E_0 of the activation energy which indicated in Fig. 14. The zero fields E_0 of the two trap levels are 0.16 and 0.46 eV.

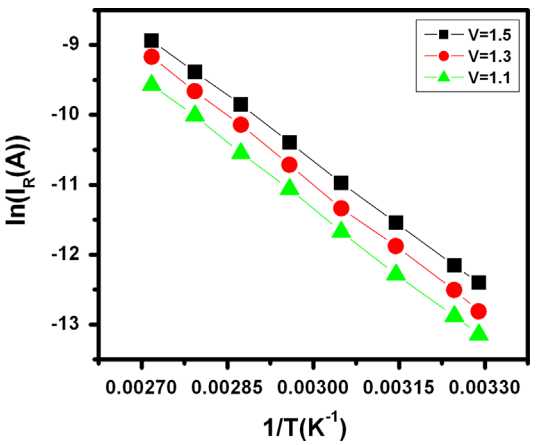

Fig. 15. Plotting of $ln(I_R(A))$ against $1/T$.

3.3.5. The dark reverse characteristics of Au/CdTe QDs/p-si/Al heterojunction device

Fig. 2 shows small dependence on voltage assuming that the generation-recombination current is the dominant source of the reverse current [37]. The reverse current can be represented by the following equation [38]:

$$I_R\alpha \exp\left(E_g/rk_B T\right) \tag{15}$$

where E_g is the energy band gap of the base material and $r=2$ if the generation-recombination process dominating. Fig. 15 represents $ln(I_R)$ against $1/T$ at different voltages. The obtained slopes in Fig. 15 are nearly constant with average value equals 0.54 eV (half the band gap of Si). In this case we conclude that the main source of the reverse current is the generation-recombination through p-Si rather than through the interface of the thin film itself [39].

4. Conclusion

Au/CdTe QDs/p-Si/Al heterojunction have been fabricated using thermal evaporation techniques. Au/CdTe QDs/p-Si/Al heterojunction have been studied by (I–V–T) measurements. The rectification ratio shows that the junction

is good to rectifier the current which equal 275 at $V = \pm 1.5$ V. Also shunt resistance and series resistance are determined. The junction I–V curves in the temperature range exhibited as a diode like behavior. In the forward bias, there are three distinct regions corresponding to three conduction mechanisms. In the first region ($V \leq 0.3$ V), thermionic emission conduction is the dominant mechanism with barrier height of 0.44 eV. In the second region ($0.5 \leq V \leq 0.9$ V), the dominant mechanism is the space charge limited current with trap distribution (TSCLC) which showes a small dependence on temperature range. The density of the trap states are calculated and they are found to be less than the values of microstructure CdTe in literature. The very large surface area of the nanoparticle films does not appear to introduce more trap states relative to microstructure so Ligands in nanoparticles based films are very effective at reducing the number of mid-gap trap states in the junction. This result affects on the optoelectronic devices based on silicon where it cause high photo-response. Finally, in the reverse biased voltage, the generation-recombination through p-Si is the main source of the conduction in which the activation energy is the half of the optical band gap of silicon.

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