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A comparison study regarding Al/p-Si and Al/(carbon nanofiber–PVP)/p-Si diodes: current/impedance–voltage (*I*/*Z*–*V*) characteristics

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Abstract
Al/p-Si and Al/(carbon nanofiber–PVP)/p-Si diodes were produced using a p-type silicon wafer with 10 Ω cm resistivity to determine the polymer interlayer effects on device characteristics. To assess whether carbon nanofiber–PVP interlayer is beneficial for electrical performance, the current–voltage (*I*–*V*) and the impedance–voltage (*Z*–*V*) measurements were performed in wide range of voltage. Thus, electrical parameters such as series resistance, barrier height, and ideality factor were derived from the forward bias Ln (I_F)–V_F and Cheung's functions, so that they are compared and voltage dependence of them is explored. Later, the values of intercept voltage, width of depletion layer, doping acceptor atom concentration, and barrier height were also extracted from C^{-2}–*V* data at 1 MHz and then results were compared with each other. The surface states and their energy profile were also extracted from the I_F–V_F characteristics by considering barrier height (BH) and n is voltage dependent as well. Experimental results indicate that the carbon nanofiber–PVP interlayer decreases surface states (N_{ss}), series resistance (R_s) and leakage current, whereas it increases rectifying ratio and shunt resistance. Hence, such polymeric interlayer material forms an interesting alternative to conventional oxide layer due to some advantages of polymers such as desirably low values of cost, weight, and energy consumption.

Keywords Al/p-Si and Al/(polymer)/p-Si diodes · Current/impedance–voltage (*I*/*Z*–*V*) characteristics · Polyvinylpyrrolidone (PVP) interlayer · Surface states (N_{ss}) · Series resistance (R_s) effects on the performance

1 Introduction

Lately, tremendous effort was put on the production of high-performance electronic devices to find budget-friendly alternatives to typical metal–semiconductor (MS) or metal–insulator–semiconductor (MIS) structures. That is why scientists have pointed their focus on the improvement of MS type structures or Schottky diodes (SDs) performance by means of growing some oxide, polymer or ferroelectric interlayer with and without metal or metal-oxide materials [1–8]. Compared to conventional oxide layer materials, growing a polymer interlayer between metal and semiconductor is usually easier and cheaper. Low molecular weight, low cost, large area of production and flexibility lightness are other features that make polymeric interlayers are advantageous [9–11]. Moreover, the existence of high-dielectric interlayer between metal (*M*) and semiconductor (*S*) layers can be more effective on the formation of barrier height (BH). Also it could decrease surface states (N_{ss}), series resistance (R_s) and the leakage current (I_R), whereas it can cause an increase in shunt resistance (R_{sh}), thus in rectifying ratio ($RR = I_F/I_R$) [12–15]. Usually, the technical significance of polymers such as polyvinyl-alcohol (PVA) and polyvinylpyrrolidone (PVP) is that they are flexible, low consumption, easy production, lower molecular weight, low cost, and water soluble. Upon dispersing with metals, metal oxides and graphene, these polymers reveal interesting electrical and dielectric properties such as higher dielectric strength

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and electronic charge storage capability due to their OH groups and hydrogen bonding formation [16, 17].

In general, the forward bias Ln (I_F)–V_F plots of the MS with and without an interfacial layer (native or deposited) at intermediate bias voltage yield a linear region since the effect of R_s in this region is quite insignificant, but the linearity is broken towards high forward biases because of R_s and interlayer [18–22]. Therefore, the applied bias voltage on the device is shared by the depletion layer, R_s and interlayer. Several techniques were suggested for extraction of N_{ss} and R_s from the *I–V*, and *C*/*G–V* characteristics. When *I–V* characteristics are available, Ohm's law [12, 13], Norde [23], Cheung [24], and modified Norde function by Bohlin [25] are the mostly preferred methods for R_s, yet it needs to be noted that there exists some differences such as different voltage range and calculation method. The existence of N_{ss} can also affect the *C*/*G–V* characteristics particularly in depletion region depending on the value of c_2 (~ 1/*n*) which is ratio of the experimental value of doping donor/acceptor level to its theoretical value (~ $N_{exp.}/N_{teor.}$) [12, 13].

The high value of n usually stems from the existence of interlayer, its thickness (d_i) and permittivity (ε_i), barrier inhomogeneity at *M*/*S* interface, N_{ss}, and doping concentration atoms in semiconductor or depletion layer width (W_d) as *n* is given by $1 + d_i/\varepsilon_i\ (\varepsilon_i/W_d - qN_{ss})$. The tunneling through the barrier via surface states or dislocations, recombination generation, and image force lowering also affect ideality factor and conduction mechanism (CM). Moreover, high value of R_s could be due to the resistivity of metal contacts, the wires which are used during measurements, the bulk resistance of the semiconductor, and the semiconductor's being non-uniformly doped [12–15].

It is well known that defects can be formed during the fabrication of semiconductor diodes and these defects which lead to N_{ss} having energies localized in forbidden band gap. Thus, the performance of MS and MIS/MPS type SDs is significantly altered. These states usually reveal themselves as a result of dangling bonds between interfacial layer and semiconductor, chemical composition of the interface, and some contaminating organic impurities in the laboratory environment [12–15].

The first purpose of this study is to produce both the Al/p-Si and Al/(carbon nanofiber–PVP)/p-Si diodes on the same p-type silicon wafer to the explore the effects of polymer interlayer on the electrical characteristics. Furthermore, the second purpose is to assess and explore whether the carbon nanofiber–PVP interlayer is beneficial or not using the *I–V* and *Z–V* data taken in wide bias range. The results of this work show that N_{ss}, R_s and leakage current are decreased, and RR and R_{sh} are increased by the use of carbon nanofiber–PVP interlayer. Thus, it was shown that carbon nanofiber–PVP forms a preferable alternative interlayer material to conventional oxide interlayers due to its advantages regarding the cost, weight, energy consumption and production methods.

2 Experimental details

The Al/p-Si (MS) and Al/(carbon nanofiber–PVP)/p-Si (MPS) diodes were produced using the same B-doped p-type silicon wafer with doping concentration of 1.39×10^{15} cm^{-3}, orientation of < 100 >, and thickness of ~ 300 µm. First, wafer was rinsed in ammonium peroxide for ~ 1 min to obtain a wafer that is free of the native oxide and some organic impurities on the surface and then it was rinsed in a solution of H_2SO_4:H_2O_2:H_2O (3:1:1) and then a solution of HCl:H_2O (1:1) for ~ 1 min for etching the wafer. Later, it was dipped into deionized water (DW) with high resistivity (18 MΩ cm) and cleaning process was finalized through drying the wafer using highly pure dry-nitrogen gas. Once the wafer is cleaned, the fabrication process was started with evaporating highly pure Al (99.999%) on the back side of wafer at 10^{-6} Torr. Thus, Al layer with 150 nm thickness was achieved and later the substrate was annealed at 500 °C for 5 min in a N_2 atmosphere to perform low resistivity ohmic contact and then, the p-Si wafer was divided two pieces to be used for production of two different diode types (MS and MPS). After the same these stages, previously the carbon–PVP solution was grown on the front of first piece of p-Si wafer by electro-spinning method. Immediately, two p-Si wafers (with and without (carbon nanofiber–PVP) interfacial layer) were taken into thermal evaporation system for growing rectifier contacts under same conditions as ohmic contact. After that, circular Al dots with radius of 0.5 mm (7.85×10^{-3} cm^2) and thickness of 150 nm were achieved on the front side of the p-Si wafer (MS) and on the (carbon nanofiber–PVP) interfacial layer at same time. Thus, both the fabrication of MS and MPS type diodes were completed. Both the thickness native insulator layer (SiO_2) and deposited (carbon nanofiber–PVP) polymer layer were estimated to be 3 nm and 23.2 nm from the interfacial layer capacitance ($C_i = \varepsilon_i\varepsilon_o A/d_i$) at 1 MHz. The schematic diagrams of the Al/p-Si (MS) and Al/(carbon nanofiber–PVP)/p-Si (MPS) type diodes were illustrated in Fig. 1. To perform electrical measurements, silver (Ag) coated thin Cu wires were connected to the contacts using Ag paste. A Keithley-2400 source meter was used for *I–V* measurements between − 3 and 3 V, and a HP4192A impedance analyzer was used for $C - V/G/\omega - V$ measurements between − 1 and 3 V. All measurements were performed in dark condition at room temperature using a software program via an ac/dc converter card.

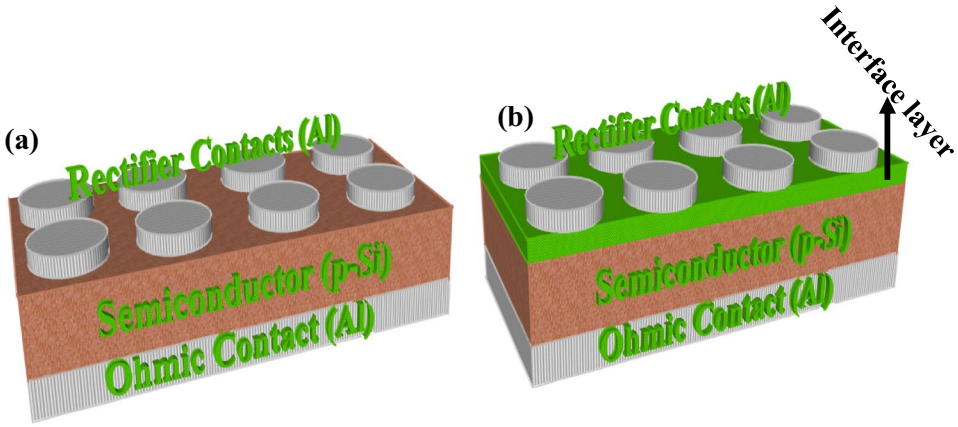

Fig. 1 The illustrative schematic diagram of the **a** MS and **b** MPS type diodes

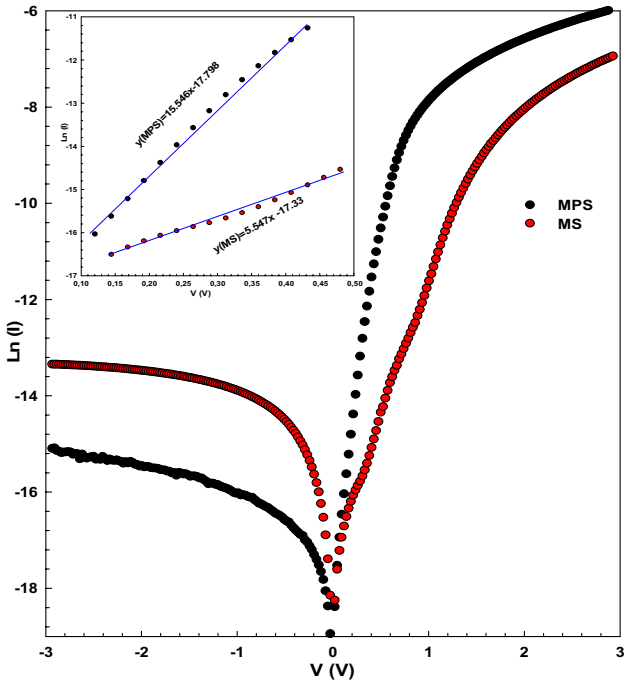

Fig. 2 Ln (*I*)–*V* plots of the MS- and MPS-type diodes

3 Results and discussion

3.1 The forward and reverse bias *I–V* characteristics

It is well known that the current–voltage (*I–V*) profile taken in wide range of bias voltage provide detailed information. Since the Al/p-Si (MS) and Al/(carbon nanofiber–PVP)/p-Si (MPS) type diodes were produced using the same p-type silicon wafer, such detailed information allows comparison of performance of these devices, so that benefits of this interlayer is revealed. Figure 2 shows the Ln *I* vs *V* plots of the MS and MPS diodes. As shown in the figure, the value of current in the reverse bias regime becomes saturated by showing weak dependence on bias; however in the forward bias regime, it rises up increasing voltage almost linearly for intermediate voltage and then deviates from the linearity because of R_s and interlayer effect. In other words, both diodes have good rectifying ratio ($RR = I_F/I_R$ at ± 2.5 V), however that of MPS diode is larger so this clearly shows the improvement in RR thanks to carbon nanofiber–PVP interlayer. In the case that MS, MIS, MPS and similar type diodes have unignorable series resistance, the theory of thermionic emission (TE) considers the relationship of current and voltage as below for $V \geq 3$ kT/q [12–14]:

$$I = AA^{*}T^{2}\exp\left(-\frac{q}{kT}\Phi_{B_0}\right)\left[\exp\left(\frac{q\left(V-\mathrm{IR_s}\right)}{nkT}\right)-1\right]. \tag{1a}$$

Here, A^{*}, I_o, Φ_{B0} and n are the effective Richardson constant, which is equal to 32 A cm^{-2} K^{-2} for *p*-type silicon, reverse saturation current, zero-bias barrier height and ideality factor, respectively, and the other parameters are well known in the literature. Once I_o is obtained from the *y*-intercept linear part of Ln (*I*) vs *V* plot, the value of zero-bias barrier height, Φ_{B0}, can be also obtained by [12]:

$$\Phi_{B_0} = \frac{kT}{q}\mathrm{Ln}\left(\frac{AA^{*}T^{2}}{I_0}\right). \tag{1b}$$

The value of the ideality factory (n) is a quantity that reflects the quality of diode, it is expected to be equal to 1 in the ideal case. Nevertheless, n values extracted from the slope of linear regime of Ln (*I*) vs *V* plot could be larger than unity in applications. Even it could be considerably higher than unity, i.e. 1, because of the interlayer depending on its thickness (δ_i) and permittivity (ε_i), semiconductor's permittivity (ε_s), surface states (N_{ss}), width of depletion layer (W_D) which depends on concentration of doping atoms, and barrier inhomogeneity as follows [14]:

$$n = \frac{q}{kT}\left(\frac{\mathrm{d}V}{\mathrm{d}(\ln(I))}\right) = 1 + \left(\frac{\delta_i}{\varepsilon_i}\right)\left\{\frac{\varepsilon_s}{W_D} + qN_{ss}\right\}. \quad (1c)$$

Utilizing Eqs. (1a–1c), the values of I_o, n, Φ_{Bo}, and RR were found as 2.97×10^{-8} A, 6.967, 0.684 eV, 6.44×10^{2} for MS diode, and 1.84×10^{-8} A, 2.486, 0.696 eV, 8.24×10^{3} for MPS diode, respectively. Clearly, carbon nanofiber–PVP interlayer decreased n value significantly while yielding 13 times higher RR value than MS diode.

Resistance (R_i) of the diode is another parameter which determines the diode quality. It is well known that R_i at high applied biases voltages corresponds to R_s, whereas R_i at enough low applied bias voltages corresponds to R_{sh}. For better performance, R_s of the diode needs to be as low as possible whilst R_{sh} needs to be as high as possible. R_i–V plots of the diodes are given in Fig. 3. R_s and R_{sh} at ± 3 V were found as 2944.06 Ω and 1.90×10^{6} Ω for MS diode, and 1137.23 Ω and 9.36×10^{6} Ω for MPS diode, respectively. These values were given in Ohm's law column of Table 1 for comparison with the values of other methods that will be mentioned in proceeding paragraphs of the paper.

Alternatively, modified Norde functions (Eqs. 2a–2c) were utilized for calculation of the BH and R_s of the diodes [23, 25]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left\{\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right)\right\}, \quad (2a)$$

$$\Phi_B = F(V_o) + \frac{V}{\gamma} - \frac{kT}{q}, \quad (2b)$$

$$R_s = \frac{kT(\gamma - n)}{qI_o}. \quad (2c)$$

In Eqs. (2a–2c); γ is the smallest integer greater than the n obtained from TE, V_o is the voltage value that coincides with the local minimum of F (V)–V and I_o is the current value corresponding to V_o. Figure 4 shows F (V)–V plots of the diodes. The F (V)–V plots for both diodes exhibit a local minimum point in the intermediate forward bias regime. Using Eqs. (2a–2c), the values of barrier height and R_s are obtained as 0.74 eV and 763.89 Ω for MS, 0.77 eV and 2424.53 Ω for MPS, respectively, and given in Norde's method column in Table 1.

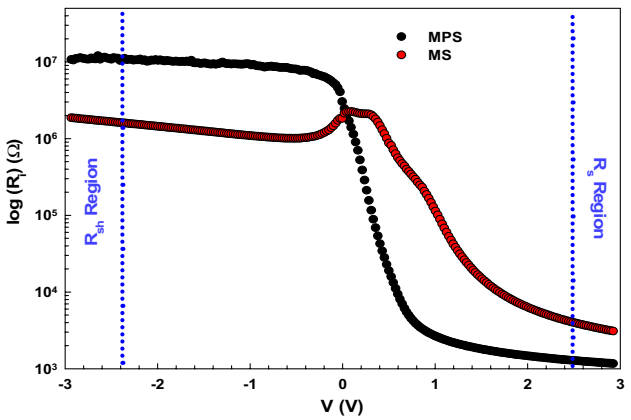

Fig. 3 R_i–V plots of the MS and MPS type diodes

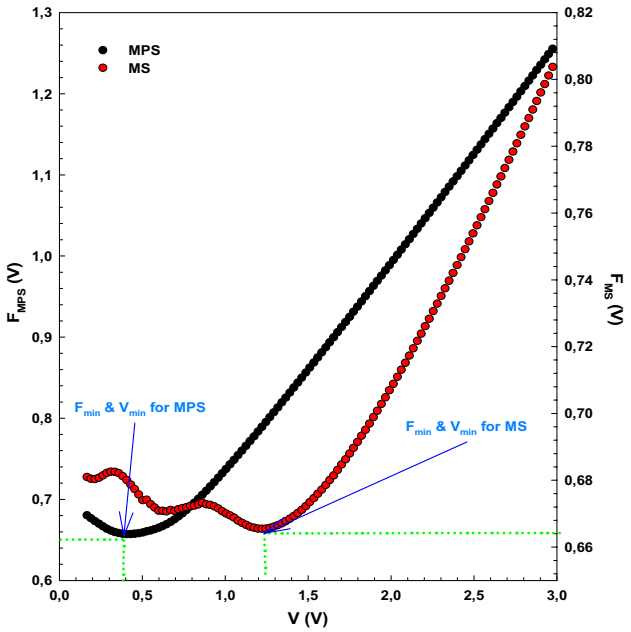

Fig. 4 F (V)–V plots of the MS- and MPS-type diodes

Table 1 Electrical parameter values obtained from different theories using I–V data

Diode:	TE theory			Ohm's law		Norde's method		Cheung's method			
								dV/d ln (I)		H (I)	
	n	I_o (A)	Φ_{Bo} (eV)	R_s (Ω) (3 V)	R_{sh} (MΩ) (− 3 V)	Φ_B (eV)	R_s (Ω)	n	R_s (Ω)	Φ_B (eV)	R_s (kΩ)
MS	6.97	2.97×10^{-8}	0.68	2944	1.90	0.74	764	7.58	1455	0.63	1.33
MPS	2.49	1.84×10^{-8}	0.70	1137	9.36	0.77	2425	3.48	1046	0.56	0.96

Another method for extracting n, BH, and R_s values from I–V data is to use Cheung's functions [24]:

$$\frac{dV}{d(\ln(I))} = IR_s + \left(\frac{nkT}{q}\right), \tag{3a}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_B. \tag{3b}$$

The n and R_s values are obtained from Eq. (3a) while BH and R_s values are obtained from Eq. (3b). Figure 5a, b show the current dependent plots of dV/d (ln (I)) and H (I) for MS and MPS diodes, respectively. Thus, dV/d (ln (I))–I plots revealed n and R_s values as 7.58 and 1454.80 Ω for MS, and 3.48 and 1046.20 Ω for MPS, respectively, and these values are given in dV/d (ln (I))–I part of Cheung's method column in Table 1. Also, H (I)–I plots revealed the values of Φ_B and R_s as 0.63 eV and 1335.60 Ω for MS, and 0.56 eV and 959.60 Ω for MPS, respectively, and these values are given in H (I)–I part of Cheung's method column in Table 1. While the values obtained for n and BH are in agreement for these three different methods, R_s values of these methods are not. This is considered to be a result of using I–V data of different bias regions during the extraction of these parameters by Chueng's method, Norde's method and Ohm's law [9, 23, 24].

For the purpose of exploring the CMs of the diodes, the forward bias ln (I_F)–ln (V_F) plots were given in Fig. 6 and these plots exhibit several linear parts corresponding to different bias regions. These linear parts were referred as Regimes I, II, III and IV for MS diode and named as Regimes I, II and III for MPS diode. Such a linearity in Fig. 6 indicates the power law behavior, which is $I \sim V^m$ relationship between current and applied voltage. The m value is indeed the slope of ln (I_F)–ln (V) and it is calculated separately for each linear regime so that it is revealed if the dominant CM is ohmic or space/trap-charge limited current, which are abbreviated as SCLC and TCLC. Thus, the m values were obtained as 3.423, 6.233, 3.999, and 1.081 for Regime I, II, III and IV of MS diode whereas it was found as 1.828, 4.743 and 2.182 for Regime I, II and III of MPS diode, respectively.

For the MS diode;

- In Regimes I, II and III; its CM has been interpreted as TCLC since the m value is larger than two.
- In Regime IV; its CM has ohmic behavior since the m value is close to the 1.

For the MPS diode;

- In Regime I; dominant CM is SCLC since the m value is close 2.
- In Regime II; its CM has been interpreted as TCLC since the m value is larger than two.
- In Regime III; dominant CM is SCLC since the m value is close 2.

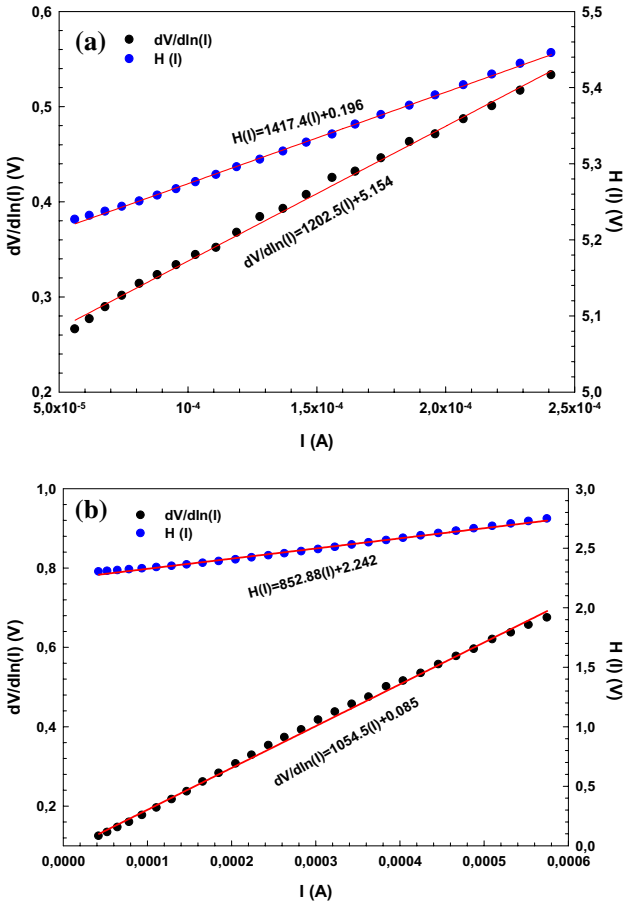

Fig. 5 dV/d (ln I)–I and H (I)–I plots of the **a** MS- and **b** MPS-type diodes

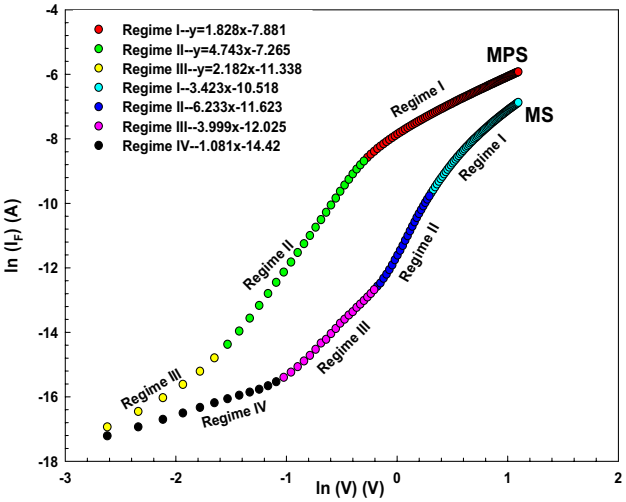

Fig. 6 Ln I_F–Ln V_F plots of the MS and MPS type diodes

Additionally, ln (I_R)–ln ($V^{1/2}$) plots were given in Fig. 7 for the purpose of investigating the CMs of MS and MPS diodes in the reverse bias voltage. There may be two CMs in the reverse bias voltage. These are Poole–Frenkel mechanism (PF) and Schottky emission mechanism (SE). Reverse bias current, I_R, for PF and SE are written as follows, respectively [8, 26–29]:

$$I_R = I_o \exp\left(\frac{\beta_{PF} V^{1/2}}{kTd^{1/2}}\right) \tag{4a}$$

$$I_R = I_o \exp\left(\frac{\beta_{SC} V^{1/2}}{kTd^{1/2}}\right), \tag{4b}$$

where d is the thickness of interlayer. As to β_{PF} and β_{SC}, they are PF field-lowering and SE field-lowering coefficients, respectively, and the relationship between these two coefficients is given by [27–29]:

$$\beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_o\varepsilon_r}\right)^{\frac{1}{2}} = 2\beta_{SC}, \tag{4c}$$

where ε_r is the dielectric constant of interlayer. Equation (4c) shows that β_{SC} is half of β_{PF}. Thus, using this equation, theoretical values of β_{PF} and β_{SC} were calculated as 5.69×10^{-7} eV^{-1} $m^{1/2}$ $V^{1/2}$ and 1.14×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$ for MS, and 4.41×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$ and 8.82×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$ for MPS, respectively. The field-lowering coefficient of a diode can be experimentally calculated from the slope of ln (I_R)–ln ($V_R^{1/2}$) plots. These plots of MS and MPS diodes are given in Fig. 7, and they have a good linear behavior. Thus, the field-lowering coefficients of MS and MPS diodes were obtained as 1.24×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$ and 4.09×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$, respectively. The dominant CM for the MS diode is SE because the experimental field-lowering coefficient of the MS diode indeed approaches to the theoretical value obtained for β_{SC}. However, the CM for the MPS diode is considered as PF because of the experimental field-lowering coefficient is closer to the theoretical value obtained for β_{PF}.

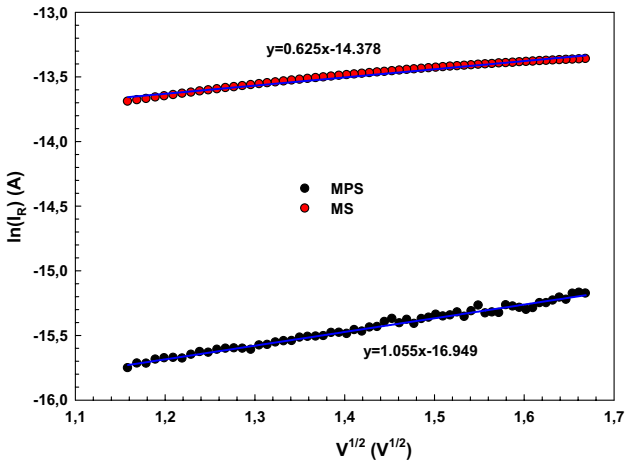

Fig. 7 ln (I_R)–$V^{1/2}$ plots of the MS- and MPS-type diodes

Interface states (N_{ss}) have also an important role in a diode because they can cause a diode to behave non-ideally. The voltage-dependent profile of N_{ss} equilibrium with semiconductor can be calculated using I–V data with the help of Eqs. (5a–5d) [14]:

$$n(V) = \left(\frac{q}{kT}\right)\left(\frac{V - IR_s}{\ln(I/I_o)}\right) \tag{5a}$$

$$\Phi_e = \Phi_{B_o} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{5b}$$

$$E_{ss} - E_v = q(\Phi_e - V) \tag{5c}$$

$$N_{ss}(V) = \left(\frac{1}{q}\right)\left(\frac{\varepsilon_i}{\delta_i}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right). \tag{5d}$$

Here Φ_e is the effective barrier height, E_{ss} is interface states energy, E_v is valance band energy, and (V) notation in n (V) indicates its dependence on voltage. δ_i values for MS diode with the native interlayer, i.e. SiO_2, and MPS diode with carbon nanofiber–PVP interlayer were calculated as 60 Å and 232 Å from the interlayer capacitance ($C_i = \varepsilon_i\varepsilon_o A/\delta$) at 1 MHz, respectively [15]. Moreover, W_D values of MS and MPS diodes were calculated as 4.42×10^{-4} cm and 4.71×10^{-4} cm from slope of the C^{-2}–V at 1 MHz, respectively. Thus, N_{ss} values were obtained for both MS and MPS diodes and energy distribution profiles of N_{ss} are given in Fig. 8. As shown the figure, the N_{ss} values of MPS diode are lower in the given region of energy owing to passivation of dangling bonds through the carbon nanofiber–PVP interlayer [9, 18].

3.2 The forward and reverse bias *Z*–*V* characteristics

For the investigation of Z–V characteristics, the experimental data was given in the form of voltage-dependent capacitance (C) and conductance (G/ω) plots in Fig. 9 for the MS and MPS diodes at room temperature and 1 MHz. The figure shows that the C–V and G/ω–V plots for the diodes have three regions as accumulation, depletion and inversion which are approximately corresponding to the voltage regions of (1.5 V/3 V), (0.5 V/1.5 V), (− 1 V/0.5 V), respectively, just like a typical MIS diode. C–V and G/ω–V plots almost reaches to a constant value particularly in the inversion and accumulation regions. As the applied bias is varies, there occur changes in C and G/ω values due to the passivation effect of interlayers (native or

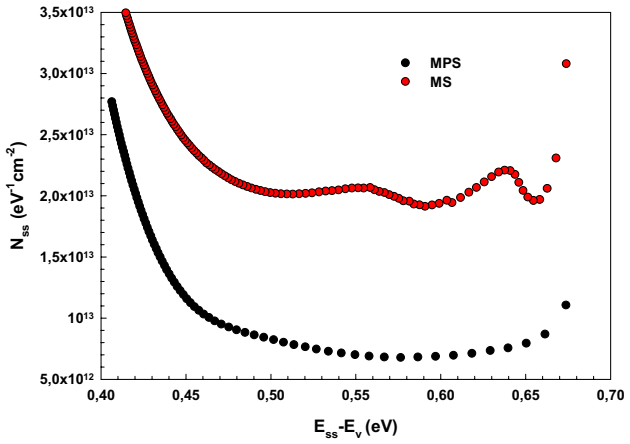

Fig. 8 ($E_{ss} - E_v$)–N_{ss} plots of the MS- and MPS-type diodes

carbon nanofiber–PVP) at *M*/*S* interface and R_s [4, 30]. Comparing the two diodes, *C* and G/ω values of MPS diode for a given bias is lower. This is partly because MPS diode has a thicker interlayer. A bending behavior of the plots of *C*–*V* and G/ω–*V* happen due to effect of R_i value is in the forward biases. Therefore, it is very important to consider the resistance of the structures.

According to Nicollian and Brews [15], the voltage evolution of the R_i value of a structure is calculated using the *C* and *G* data in Eq. (6):

$$R_i = \left(\frac{G_m}{G_m^2 + (\omega C_m)^2} \right). \tag{6}$$

Thus R_i values were calculated for both diodes and R_i–*V* plots were given in Fig. 10. The figure clearly shows that R_i have a nearly constant value at the inversion and accumulation regions, particularly for MPS diode. The series resistance (R_s) of the structure corresponds to R_i at sufficiently high voltages and frequency. The R_s values of the diodes at + 3 V are given in Table 2 along with other electrical parameters which will be mentioned in proceeding paragraphs of the paper.

To extract electrical parameters from depletion capacitance data of the diodes, C^{-2}–*V* plots were given in Fig. 11. As shown in this figure, these plots reveal linearity for both diodes. Although it seems linear fit lines are nearly parallel to each other, their slopes are different.

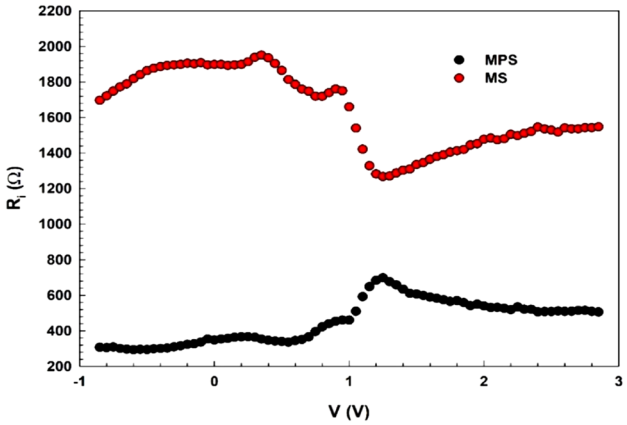

Fig. 10 R_i–*V* plots of the MS and MPS type diodes at 1 MHz

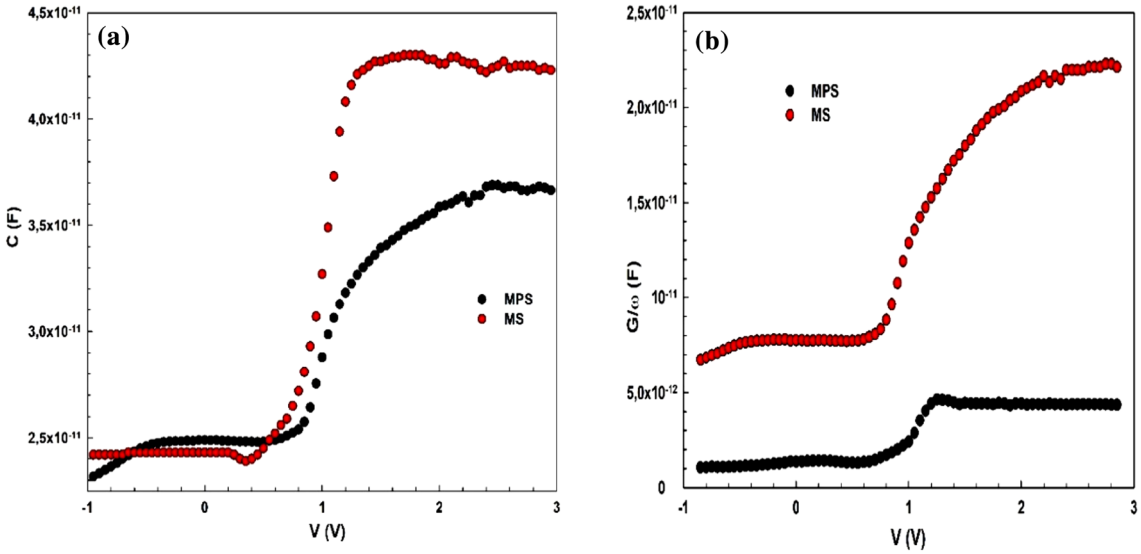

Fig. 9 **a** *C*–*V* and **b** G/ω–*V* plots of the MS and MPS diodes at 1 MHz

Table 2 Various electrical parameters obtained from the C^{-2}–V plot at 1 MHz

Diode	V_D (eV)	$N_A \times 10^{14}$ (cm^{-3})	E_F (eV)	$W_D \times 10^{-4}$ (cm)	Φ_B (C–V) (eV)	R_s (Ω) (at + 3 V)
MS	2.22	2.383	0.267	4.42	0.669	1541.25
MPS	2.52	2.298	0.268	4.71	0.705	506.73

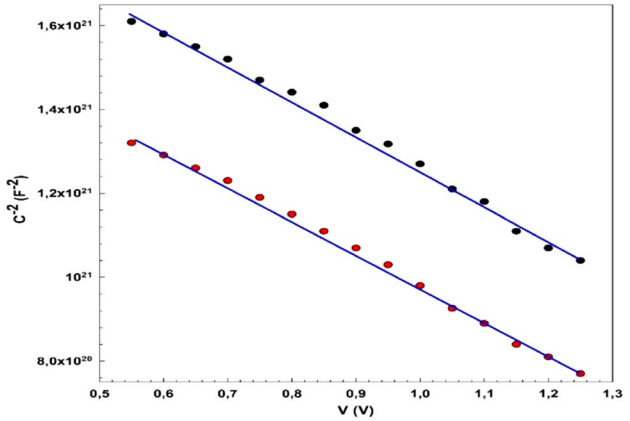

Fig. 11 C^{-2}–V plots of the MS- and MPS-type diodes at 1 MHz

The x-intercept and slope values of Fig. 11 are useful for extracting some parameters such as diffusion potential (V_D), acceptor atom concentration (N_A), the Fermi energy (E_F) and W_D. Thus, Φ_B (C–V) of the diodes at 1 MHz is obtained using these parameters in equation below [12, 31]:

$$\Phi_B(C-V) = V_D + E_F. \tag{7a}$$

Here V_D is equal to $V_o + kT/q$ where V_o is the x-intercept of C^{-2}–V plot. As to E_F, it is calculated by [12, 31]:

$$E_F = \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right). \tag{7b}$$

Here N_V is used for denoting the effective density of states for valance band of Si ($=1.04\times10^{19}$ cm^{-3}) [12]. N_A ($=2/(q\varepsilon_s\varepsilon_o A^2$ (dC^{-2}/dV))) is acceptor atom concentration and was obtained as 2.383×10^{14} cm^{-3} and 2.298×10^{14} cm^{-3} for MS and MPS diodes, respectively, using the slope values of C^{-2}–V. Thus, W_D was calculated using the equation below [12, 31]:

$$W_D = \sqrt{\frac{2\varepsilon_s\varepsilon_o V_D}{qN_A}}. \tag{7c}$$

The experimental values of V_D, N_A, E_F, W_D and Φ_B (C–V) obtained for MS and MPS diodes at 1 MHz using Eqs. (7a–7c) are given in Table 2.

As shown in the Table 2, the MPS diode has higher Φ_B (C–V) value than the MS diode owing to the carbon nanofiber–PVP interlayer. All experimental results reveal that SiO_2 may be good dielectric due to its suitability with silicon; however, it has low dielectric permittivity (~3.8 ε_o) and hence it tends to yield larger leakage current, N_{ss}, and R_s. But, this problem can be overcome using high dielectric film at M/S interface such as $BaTiO_3$ [8], $SrTiO_3$ [32], (Gr–PVA) [4], (Fe_2O_4–PVP) [33], (Fe_3O_4) [34], Sm_2O_3 [35], and (Cu–PVA) [36] by various researchers in recently.

4 Conclusion

For the purpose of exploring the effects of the carbon nanofiber–PVP polymeric interlayer, Al/p-Si type diodes with and without carbon nanofiber–PVP interlayer were produced using same silicon wafer and their voltage-dependent current and impedance measurements were performed in wide bias range at room temperature. First, I–V data were utilized for the extraction of some parameters; such as Φ_B (I–V), R_s, n, using TE theory, Ohm's law, Cheung's, and Norde functions and comparisons were made between these methods' results. Second, C–V data of depletion region at 1 MHz were utilized for the extraction of Φ_B (C–V), W_D, E_F, N_D and V_D. Both characteristics (I–V and C–V) revealed larger Φ_B for MPS diode because of the polymeric carbon nanofiber–PVP interlayer as well as the nature of measurement method, voltage, and calculation method. For MPS diode, the obtained level of N_{ss} is considerably lower than that for the MS diode. Also, obtained RR value for MPS diode is also 13 times larger than that for the MS diode. Experimental findings of this study clearly show that the usage of polymeric carbon nanofiber–PVP interlayer leads to some enhancement in diode's performance in terms of its electrical parameters. Considering some advantages of polymers such as desirably low values of cost, weight, and energy consumption, this polymeric interlayer material would form a preferable alternative to conventional interlayer materials.

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