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Electrical and interfacial properties of Au/P3HT:PCBM/n-Si Schottky barrier diodes at room temperature

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ABSTRACT

In this study, a gold/poly(3-hexylthiophene):[6,6]-phenyl C61 butyric acid methyl ester/n-type silicon (Au/P3HT:PCBM/n-Si) metal-polymer-semiconductor (MPS) Schottky barrier diode (SBD) was fabricated. To accomplish this, a spin-coating system and a thermal evaporation were used for preparation of a P3HT/PCBM layer system and for deposition of metal contacts, respectively. The forward- and reverse-bias current–voltage (*I–V*) characteristics of the MPS SBD at room temperature were studied to investigate its main electrical parameters such as ideality factor (n), barrier height (Φ_B), series resistance (R_s), shunt resistance (R_{sh}), and density of interface states (N_{ss}). The *I–V* characteristics have nonlinear behavior due to the effect of R_s, resulting in an n value (3.09) larger than unity. Additionally, it was found that n, Φ_B, R_s, R_{sh}, and N_{ss} have strong correlation with the applied bias. All results suggest that the P3HT/PCBM interfacial organic layer affects the Au/P3HT:PCBM/n-Si MPS SBD, and that R_s and N_{ss} are the main electrical parameters that affect the Au/P3HT:PCBM/n-Si MPS SBD. Furthermore, a lower N_{ss} compared with that of other types of MPS SBDs in the literature was achieved by using the P3HT/PCBM layer. This lowering shows that high-quality electronic and optoelectronic devices may be fabricated by using the Au/P3HT:PCBM/n-Si MPS SBD.

1. Introduction

Organic semiconductors used in electronic and photonic devices have many advantages over inorganic semiconductors, such as easy fabrication, low cost, and applicability to rigid and flexible substrates. All of these advantages make organic semiconductors very attractive active components for organic light-emitting diodes, transistors, organic lasers, organic field-effect transistors, organic photodiodes, solar cells, and other solid-state electronic devices such as Schottky diodes [1,2].

The Schottky barrier diode (SBD) consists of a metal–semiconductor (M/S) junction whose properties depend on the work function of the metal, the band gap of the intrinsic semiconductor, and the type and concentration of dopants in the semiconductor. Additionally, the presence of a thin interfacial polymer layer between the metal and semiconductor, referred to as metal–polymer–semiconductor (MPS) sandwich configuration, shows the main characteristics of SBDs. MPS structures have become more popular compared with other types of SBD structures because of their industrial applications [3,4].

Heterojunctions and SBDs fabricated and tested using different semiconducting organic and inorganic compounds have gained considerable importance in terms of the characteristics of electronic devices [5,6]. The electrical and dielectric properties of electronic devices strongly depend on the interface states and on the polymeric interfacial layer in MPS structures [7].

Among the organic semiconductors, the mixture of poly(3-hexylthiophene) (P3HT) and [6,6]-phenyl C61

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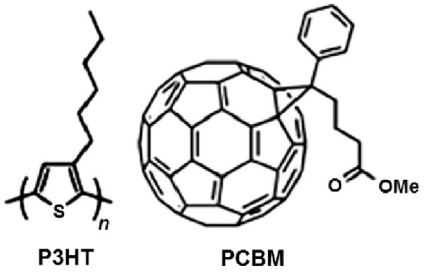

Fig. 1. Chemical structures of P3HT and PCBM.

butyric acid methyl ester (PCBM) is a promising material for industrial applications [8,9]. This blend is generally used for photovoltaic devices because of its efficiency (as high as 5%) [10]. The structures of P3HT and PCBM are shown in Fig. 1. P3HT, a conjugated polymer (Fig. 1), is commonly used for hole transport in organic solar cells because of the high mobility of charge carriers in the material (0.1 cm^2/V s) [11]. PCBM, an n-type soluble molecule based on fullerene (Fig. 1), is used for electron transport because of the high mobility of electrons in the material (μ_e = 0.21 cm^2/V s) [8]. Another advantage of using the P3HT/PCBM blend as a polymeric interfacial layer in MPS SBDs is its easy processing.

Previous studies examined the enhancement of MPS device performance by using organic interfacial layers in SBDs with new organic materials such as polyvinyl alcohol [12], perylene [13], rhodamine-101 [14], and chitin [15] inserted at the (M/S) interface. In addition to enhancement in device performance, improvement in rectification behavior of the diode can be achieved by using an organic interfacial layer instead of an inorganic interfacial layer. To improve the device performance of MPS SBDs, understanding the electrical properties of MPS SBDs is important. For instance, the density of interface states (N_{ss}) at the metal/polymer (M/P) interfacial layer and at the polymer/semiconductor interface, the series resistance (R_s) of MPS diodes, and the barrier height (Φ_B) of the M/S interface affect the performance of MPS diodes. These properties can be deduced from current–voltage (*I–V*) analysis.

In the present study, *I–V* measurements were performed on a Au/P3HT:PCBM/n-type silicon (n-Si) MPS SBD in the dark at room temperature. Essential electrical parameters such as ideality factor (n), Φ_B, R_s, shunt resistance (R_{sh}), μ_e, and N_{ss} were obtained from *I–V* analysis and then investigated to determine the effects of the P3HT/PCBM interfacial layer.

2. Experimental

Prior to cleaning of the Si wafer and evaporation of the back metal contact, a mixture of P3HT/PCBM (20 wt% PCBM) was prepared for spinning on n-Si wafer. P3HT and PCBM were procured from Sigma-Aldrich Company Ltd. P3HT and PCBM were dissolved in 1,2-dichlorobenzene to a concentration of 10 g/L at 60 °C.

Phosphorus-doped single-crystalline n-Si wafer with a $<100>$ orientation was used as a substrate. The thickness and resistivity of one side of the polished Si wafer were 350 ± 25 μm and 4.8 Ω cm, respectively. The Si wafer was cleaned by using the RCA cleaning procedure [16]. Immediately, silver (Ag) metal was then evaporated onto the entire back-side of the n-Si wafer to a thickness of ~2500 Å by use of a thermal evaporation system (~1×10^{-6} mbar pressure). This formed a low-resistivity ohmic back contact. Subsequently, the wafer was thermally annealed at 450 °C for 30 min under N_2 flow to achieve good ohmic contact. During formation of the back-side ohmic contact, a thin native oxide layer formed on the front side of the n-Si wafer. Therefore, the front side of the n-Si wafer was cleaned with 50% HF solution.

The P3HT/PCBM mixture (20 wt% PCBM) was immediately spun onto the front surface of the Si wafer for 30 s at an acceleration of 1500 rpm/s to form a continuous film with 100 nm thickness. Afterward, the film was dried at 150 °C for 15 min on a hot plate to evaporate the solvent.

To fabricate the Au/P3HT:PCBM/n-Si SBDs, Au rectifying contacts were formed on the P3HT:PCBM film on the front of the n-Si wafer. A metal shadow mask with circular dots (1 mm diameter) was used to deposit the Au metal by using a thermal evaporator system at a pressure of ~1×10^{-6} mbar. The thickness of the circular Au contacts and the deposition rate of Au were 1500 Å and 3 Å/s, respectively, as determined from observations through a quartz crystal thickness monitor.

The *I–V* characteristics of the Au/P3HT:PCBM/n-Si SBD in the dark at room temperature were measured on a Keithley 4200 SCS. *I–V* measurements using an IEEE-488 AC/DC converter card connected to a computer were performed, while a GPIB data transfer card was used to record data from *I–V* measurements to a computer.

3. Results and discussion

An overview of the forward- and reverse-bias *I–V* characteristics of the Au/P3HT:PCBM/n-Si MPS SBD in the dark at room temperature is shown on a semilogarithmic scale in Fig. 2. The difference in the work functions of the electrodes implies different barriers at the M/P interface that give rise to the asymmetrical nature of the curve, and thus the high rectification characteristic of the diode. The effects of R_s and of the interface states as well as the value of n ($n \geq 1$) led to this nonlinear *I–V* behavior. By considering these effects, we could express the *I–V* characteristics of the Au/P3HT:PCBM/n-Si MPS SBD according to the thermionic emission (TE) theory through the following relation [17,18]:

$$I = I_0 \left[\exp\left(\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \quad (1)$$

where V is the applied voltage, IR_s is the voltage drop across the R_s of the diode, n is the ideality factor, k is the Boltzmann constant, T is the absolute temperature in Kelvin, q is the electronic charge, and I_0 is the reverse saturation current derived from the straight-line intercept of the ln *I–V* plot at zero bias. I_0 is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{B0}}{kT} \right) \quad (2)$$

where A, A^*, Φ_{B0} are the rectifier contact area, the effective Richardson constant (equal to 120 A/cm^2 K^2 for n-Si

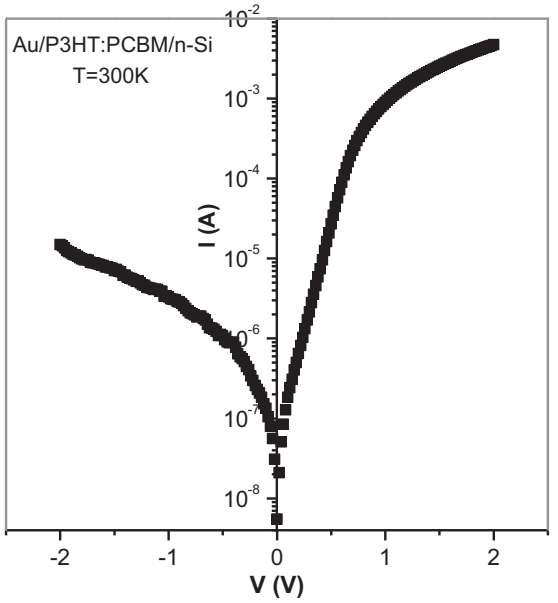

Fig. 2. Semilogarithmic ln *I–V* plot of the Au/P3HT:PCBM/n-Si MPS SBD in the dark at room temperature.

[17,18]), and the zero-bias barrier height, respectively. The value of n is a measure of the deviation of the diode from the ideal TE theory. It determines the slope of the exponential regime of the dark *I–V* characteristics on a semilogarithmic plot through the following relation [18]:

$$n = \frac{q}{kT}\frac{d(V - IR_s)}{d(\ln I)} \tag{3}$$

The value of Φ_{B0} may be extracted from the extrapolated I_0, and it may be expressed as follows:

$$\Phi_{B0} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \tag{4}$$

The semilogarithmic *I–V* curve of the device in the dark at room temperature is shown in Fig. 2. The curve gives information regarding the rectifying behavior of the diode, the leakage current, the interface states, as well as the R_s and R_{sh} of the device. The *I–V* characteristics of the Au/P3HT:PCBM/n-Si MPS SBD show its rectification behavior (Fig. 2). This behavior is due to formation of a space charge layer at the Au/P3HT:PCBM/n-Si MPS SBD interfaces. The rectification behavior may be analyzed from the rectification ratio (RR). The value of RR may be defined as the ratio of the forward- to the reverse-bias current at a fixed voltage (± 5 V); it is equal to 3.17×10^2 for the Au/P3HT:PCBM/n-Si MPS SBD. This value of RR is similar to results from other studies on MPS SBDs [5,7]. Additionally, Fig. 2 indicates that there is a linear relationship at low applied voltages (< 0.8V); in contrast, there is a deviation from linearity at high applied voltages (≥ 0.8V), which may be a result of IR_s in the natural region of the semiconductor.

Values of I_0, n, and Φ_{B0} of the Au/P3HT:PCBM/n-Si MPS SBD derived from the slope of the linear region of the forward-bias ln *I–V* plot (Fig. 2) based on Eqs. (2), (3), and (4) are 5.11×10^{-8} A, 3.09 eV, and 0.73 eV, respectively. The calculated value of n is higher than unity, indicating deviation from ideal *I–V* behavior in the semiconductor devices. This deviation may be attributed to the high N_{ss} localized at the M/P interface, the high value of R_s, the effect of barrier inhomogeneities, and the tunneling effect [17–19]. On the other hand, the Φ_{B0} value of Au/P3HT:PCBM/n-Si MPS SBD increased relative to that of the conventional Au/n-Si diode [7]. The P3HT/PCBM blend, which modifies the interfacial electrical parameters of Au/n-Si diodes and the effective Φ_B by affecting the space charge region of the n-Si, might cause this increase.

R_s and R_{sh} are important parameters of the performance of the SBDs and affect the *I–V* characteristics of the diodes. Because of this, determination of R_s and R_{sh} values is very useful for understanding the mechanism of diodes. In ideal diodes, the values of R_s are low while R_{sh} is high (on the order of megaohms). The voltage across the Schottky barrier is equal to the applied voltage minus the value of IR_s, that is, $V_d = V - IR_s$. SBD resistance (R_i) under forward bias and under reverse bias can be expressed as R_s and R_{sh}, respectively, which is the derivative of voltage with respect to current ($R_i = dV_i/dI_i$). Fig. 3 shows a plot of R_i versus V for the Au/P3HT:PCBM/n-Si MPS SBD, which determines the R_s and R_{sh} values. The values of R_s and R_{sh} of the Au/P3HT:PCBM/n-Si MPS SBD were found to be 642 and $0.77 \times 10^6\ \Omega$, respectively. The low R_s and high R_{sh} values show that the Au/P3HT:PCBM/n-Si MPS SBD behaved as a near-ideal diode.

The *I–V* characteristics at room temperature is shown in a double logarithmic scale (Fig. 4), which was constructed to determine the dominant mechanism of current conduction in the Au/P3HT:PCBM/n-Si MPS SBD in the forward-bias region. As depicted in Fig. 4, three distinct linear regions (viz., I, II, and III) representing different mechanisms of current conduction in the diode can be identified. These regions have different slopes. In each region, the current depends on the voltage (i.e., $I \propto V^m$, where m is the slope of the ln *I*–ln *V* plot for each phase. m defines the conduction mechanism) [12,20,21]. The values of m for regions I, II, and III were found to be 1.34, 3.29, and 2.36, respectively. These are similar to reported values in the literature [22,23]. Ohmic behavior is the mechanism of

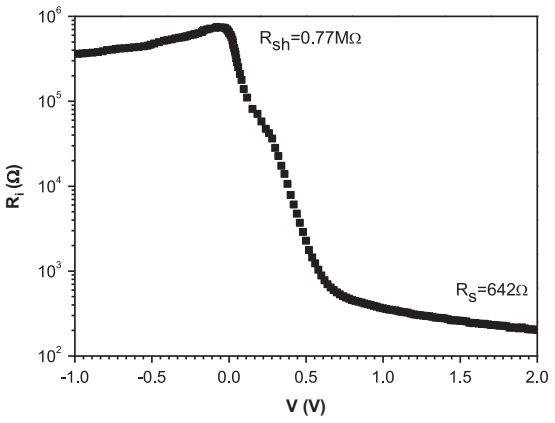

Fig. 3. SBD resistance (R_i) of the Au/P3HT:PCBM/n-Si MPS structure as a function of voltage at room temperature.

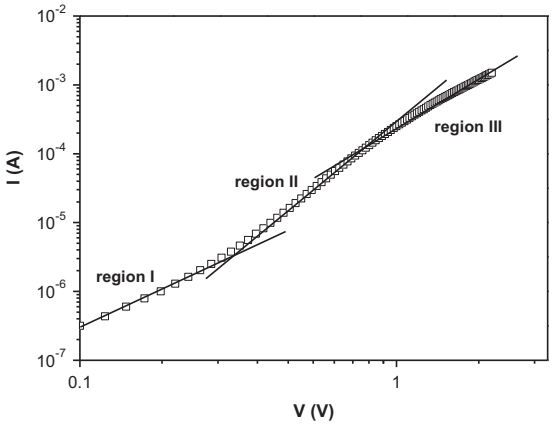

Fig. 4. Double logarithmic *I–V* plot of the Au/P3HT:PCBM/n-Si MPS SBD in the forward-bias region at room temperature.

current conduction in region I, where voltage is low and the slope of the curve is approximately unity ($m \approx 1$). At higher voltages, that is, in regions II and III, the current is proportional to the voltage, with $m \geq 2$ (power law), corresponding to space-charge limited current (SCLC) as the dominant mechanism of current conduction. The SCLC region starts at a particular voltage (V_x), which is the end of the ohmic region. Thus, the conduction mechanisms are both ohmic and SCLC conduction at V_x. At low voltages ($V_{bias} \leq 0.3$ V), the number of thermally excited carriers, the conductive components in the ohmic region, is inadequate, and the trap levels are nearly empty [24]. With the rise in voltage ($V_{bias} \geq 0.3$ V), the density of carriers injected from electrodes increase, dominating the charge-carrier transport capacity of the blended layer and filling the traps [25]. The mechanism of SCLC conduction is the result of current, which is limited when the field due to space charge dominates the applied electric field. A bulk relaxation time exceeding the transit time of any excess injected carrier gives rise to SCLC [26]. Interaction of the carriers with localized defects state may depend on the magnitude of the current response and on the actual *I–V* characteristics. The energy distribution of the trapping levels affects the transition from an ohmic region to an SCLC region, which happens when the injected carrier density exceeds the volume-generated free carrier density [27,28]. In organic semiconductors, charge-carrier mobility is insufficient to sweep additionally injected charges to the receiving electrode [26]. Under such conditions, the SCLC can be expressed as given below:

$$I = \frac{9}{8}\varepsilon_0\varepsilon_s\mu_e\frac{A}{d^3}V^2 \tag{5}$$

where ε_0 and ε_s are the permittivities of free space and of the semiconductor, respectively; d is the thickness of the interfacial organic layer (determined to be ~100 nm by use of a Dektak step profilometer); and μ_e is the mobility of the electron in the interfacial organic layer. In Eq. (5), the effect of traps on charge transport is ignored since all the traps are filled [29]. The value of μ_e calculated from Eq. (5) was found to be 3.25×10^{-7} cm^2/V s. This value is comparable to the result of another study on such organic film used SBDs [30,31].

As shown in Fig. 2, the nonlinear *I–V* curve shows a downward curvature obtained at high forward-bias voltages. This curvature results in two linear regions in the forward-bias ln *I–V* plot, namely, a region in the low-bias region with large slope and another in the high-bias region with a smaller slope. Such behavior of the *I–V* characteristics of the Au/P3HT:PCBM/n-Si MPS SBD in the forward-bias region at room temperature may be attributed the effects of R_s, N_{ss}, and interfacial states at the M/S interface. In the present study, the values of R_s, Φ_B, and n in the nonlinear region of the curve were evaluated by using a method developed by Cheung and Cheung [32]. The parameters of this method may be determined through the following relations:

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \tag{6}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{7}$$

and

$$H(I) = IR_s + n\Phi_B \tag{8}$$

Plots of $dV/d(\ln I)$ versus I and of $H(I)$ versus I for the Au/P3HT:PCBM/n-Si MPS SBD at room temperature are shown in Fig. 5. Eq. (6) gives a straight line from data for the downward curvature region in the forward-bias ln *I–V* curve. The slope of the $dV/d(\ln I)$–I plot is equal to R_s, and the y-axis intercept of the $dV/d(\ln I)$–I plot, $n(kT/q)$, determines the value of n. The values of R_s and n are 1.24 kΩ and 3.33, respectively. Additionally, the value of n determined from the $dV/d(\ln I)$–I plot is slightly higher than that obtained from the forward-bias ln *I–V* plot. The higher values of n than unity ($n > 1$) for both cases might be due to interface dipoles and to fabrication-induced defects at the interface, as well as to the presence of the P3HT/PCBM layer [33,34]. On the other hand, the $H(I)$–I plot constructed based on Eq. (8) is linear, with its y-axis intercept equal to $n\Phi_B$. The slope of this plot also provides a second determination of R_s which can be used to check the consistency of Cheung's method. By using the value of n determined from Eq. (6), the value of Φ_B is obtained from

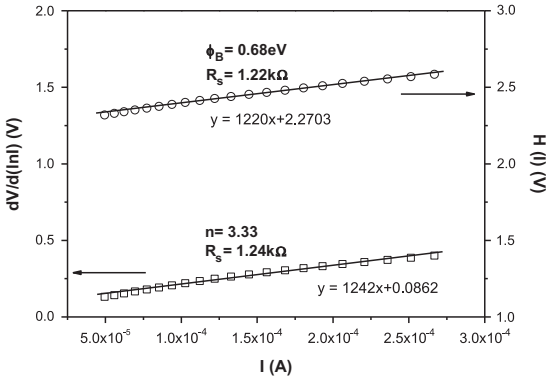

Fig. 5. Plots of the experimental $dV/d(\ln I)$ versus I and of $H(I)$ versus I for the Au/P3HT:PCBM/n-Si MPS SBD at room temperature.

the y-axis intercept of the $H(I)$–I curve plotted according to Eq. (7). Thus, the value of Φ_B may be calculated from Eq. (8). The values of Φ_B and R_s were found to be 0.68 eV and 1.22 kΩ, respectively. It can be seen that the R_s values obtained from the functions proposed by Cheung and Cheung are almost the same. This similarity may be attributed to the consistency of these functions. On the other hand, these values of R_s are higher than those obtained from the I–V plot. This difference suggests that R_s is a current-limiting factor for the Au/P3HT:PCBM/n-Si MPS SBD. Moreover, the value of Φ_B deduced from the method of Cheung and Cheung is in good agreement with the values of Φ_B determined by applying the TE theory to the I–V characteristics.

The junction parameters of the MPS diodes, such as Φ_B and R_s, were also determined by using an alternative method proposed by Norde [35]. The Norde function is described below:

$$F(V)=\frac{V}{\gamma}-\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) \tag{9}$$

where γ is a dimensionless arbitrary integer greater than the value of n deduced from the I–V characteristics. First, Norde function $F(V)$ is plotted against V by using Eq. (9) (Fig. 6). The value of Φ_B can then be deduced from the following equation:

$$\Phi_B=F(V_0)+\frac{V_0}{\gamma}-\frac{kT}{q} \tag{10}$$

where $F(V_0)$ is the minimum point of $F(V)$, and V_0 is the corresponding voltage. The value of R_s determined from Norde's method may be expressed as follows:

$$R_s=\frac{kT(\gamma-n)}{qI_0} \tag{11}$$

where I_0 is the current corresponding the minimum point of $F(V_0)$. The approach in Eq. (11) is valid only for high values of R_s [36]. By using the plot of $F(V)$ versus V, values of Φ_B and R_s for the Au/P3HT:PCBM/n-Si MPS SBD at room temperature were found to be 0.76 eV and 3.44 kΩ, respectively. These values are in good agreement with those obtained from the functions of Cheung and Cheung and from the Norde method. Additionally, Φ_B is higher (0.76 eV) than that of the conventional Au/n-Si diode [7]. This difference may be due to the P3HT/PCBM layer, which modifies the Φ_B by influencing the space charge region of the n-Si inorganic substrate [32,37].

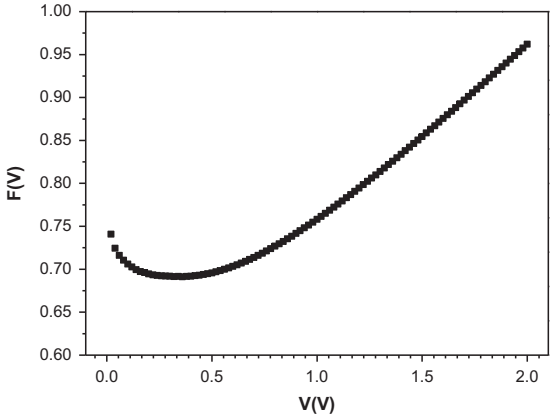

Fig. 6. A plot $F(V)$ versus V for the Au/P3HT:PCBM/n-Si MPS SBD.

One of the most important properties of SBDs, besides Φ_B, n, and R_s, is the interface states which causes the higher value of n than unity. There are very few studies on the interface states of MPS SBDs [7,12,38]. The density distribution curves of the interface states (N_{ss}) in equilibrium with the semiconductor may be determined from the forward-bias ln I–V characteristics. Nonlinear I–V characteristics of the MPS diode lead to the voltage-dependent ideality factor, $n(V)$. The effective barrier height (Φ_e) also depends on the voltage because of either the nonlinear behavior of the I–V curve or the presence of the P3HT/PCBM layer and R_s. $n(V)$ and Φ_e may be expressed through the following equations [19,39]:

$$n(V)=\frac{q\,(V-IR_s)}{kT\ln\,(I/I_0)} \tag{12}$$

$$\Phi_e=\Phi_{B0}+\beta(V-IR_s)=\Phi_{B0}+\left(1-\frac{1}{n(V)}\right)(V-IR_s) \tag{13}$$

where β is the voltage coefficient of Φ_e. It combines the effects of N_{ss} and R_s. By considering the nonideal I–V characteristics of the MPS diode, we find that n becomes N_{ss} dependent and greater than unity, as deduced by Card and Rhoderick [19,40]:

$$n(V)=1+\frac{d}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D}+qN_{ss}(V)\right] \tag{14}$$

where d is the thickness of the interfacial organic layer; W_D is the width of the space charge region calculated from the experimental C^{-2} versus V plot at 1 MHz [12]; $\varepsilon_i = 3.8\varepsilon_0$ and $\varepsilon_s = 11.8\varepsilon_0$ are permittivities of the interfacial and semiconductor layers [41], respectively; and N_{ss} is the density of the interface states in equilibrium with the semiconductor.

In n-type semiconductors, the energy of the interface states (E_{ss}) can be defined in terms of the conduction band edge at the semiconductor surface (E_c), as follows [42]:

$$E_c-E_{ss}=q(\Phi_e-V) \tag{15}$$

Fig. 7 shows the energy distribution profile of N_{ss} determined from the experimental data of the forward-bias I–V characteristics of the Au/P3HT:PCBM/n-Si MPS SBD at room temperature. As shown in this figure, N_{ss} exponentially increases with the applied bias from the midgap toward the bottom of the conduction band. In the Au/P3HT:PCBM/n-Si MPS SBD, formation of the P3HT/PCBM layer on the inorganic n-Si semiconductor could generate a high N_{ss} at the semiconductor surface. Hence, the presence of the P3HT/PCBM layer influences the properties of the SBD. N_{ss} varies from 2.09×10^{11} to 9.94×10^{11} cm^2/eV. These results show that the value of N_{ss} strongly depends on the bias and changes with the applied bias according to the position in the Si gap. Additionally, variation of N_{ss} might be due to the presence of the P3HT/PCBM layer, which could prevent diffusion between the Au contact and the n-Si surface, and thereby

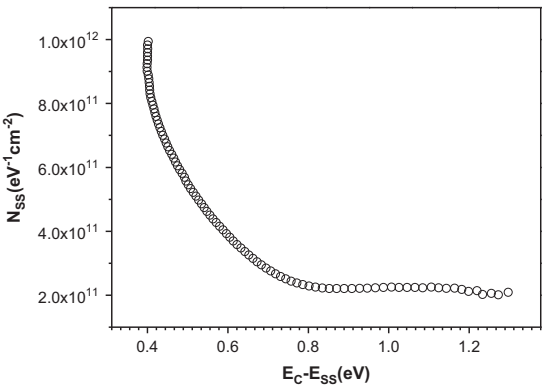

Fig. 7. Profile of the density of interface states (N_{ss}) as a function of $E_c - E_{ss}$ for the Au/P3HT:PCBM/n-Si MPS SBD at room temperature.

reduce the high gate current. Therefore, the P3HT/PCBM interfacial layer used in the SBD considerably lowered the value of N_{ss} compared with those observed in other studies on SBDs [7,12,43,44].

4. Conclusion

The forward- and reverse-bias *I–V* characteristics of a Au/P3HT:PCBM/n-Si MPS SBD at room temperature were studied. The *I–V* characteristics show nonlinear behavior due to the effect of R_s, as evidenced by the n value of 3.09 ($n > 1$). By considering the experimental results, we believe that main electrical parameters such as n, Φ_B, R_s, R_{sh}, and N_{ss} have a strong correlation with the applied bias. R_i was plotted as a function of voltage by using *I–V* characteristics to determine the effect of R_s on the electrical characteristics. The profile of the R_i–*V* plot obtained under forward bias shows a plateau in the high-bias region corresponding to the R_s value of the MPS diode. On the other hand, the Φ_B value of the Au/P3HT:PCBM/n-Si MPS SBD is higher than that of the conventional Au/n-Si diode because of the presence of the P3HT/PCBM layer. The *I–V* characteristics plot on a double logarithmic scale has three distinct linear regions (I, II, and III) with different slopes. These regions represent different mechanisms of current conduction. Characteristics of region I, which has a slope of ~1, correspond to ohmic conductivity at low voltages; regions II and III, which have slopes of ≥ 2 correspond to SCLC conductivity at high voltages. The values of n, Φ_B, and R_s were also examined by use of functions proposed by Cheung and Cheung and through the Norde method. There is good agreement between the results determined from these techniques. The forward-bias *I–V* data were also used to determine the energy profile of N_{ss}. A high value of n (3.09) at equilibrium with the semiconductor was obtained when the voltage dependence of Φ_e and R_s were considered. N_{ss} exponentially increases with bias from the midgap toward the bottom of the conduction band because of the increase in R_s due to reduction of the applied bias. The results show that the P3HT/PCBM interfacial layer considerably lowers the value of N_{ss} relative to that of the conventional Au/n-Si diode, while the R_s values of the Au/P3HT:PCBM/n-Si MPS SBD are higher than those of the conventional Au/n-Si diode because of the presence of the P3HT/PCBM interfacial layer. All of the results show that the electrical parameters of the Au/P3HT:PCBM/n-Si MPS SBD are mainly affected by the P3HT/PCBM interfacial organic layer and by R_s and N_{ss}. Moreover, a lower value of N_{ss} compared with that of other types of MPS SBDs in the literature was observed when P3HT/PCBM film was used as organic interfacial layer.

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