

Electrical and Temperature Behavior of the Forward DC Resistance With Potential Induced Degradation of the Shunting Type in Crystalline Silicon Photovoltaic Cells and Modules

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Abstract—Potential-induced degradation (PID) is an unsolved and major power degradation mechanism that affects photovoltaic (PV) cells, and the tendency to increase the operating voltage of PV systems will render it worse, affecting their reliability. A method, which can detect PID at an early stage, can alleviate reliability issues, safeguarding high energy output. The measurement of the forward dc resistance (FDCR) provides promising results for the early PID detection (<2% power loss). The FDCR method is tested on single-cell and multi-cell PV modules and it is the pathway for the development of a detection method at the system level. This work examines the effect of PID degradation rate and temperature on the detection sensitivity (electrical behavior) of the FDCR method. Additionally, the effect of temperature (temperature behavior) on the FDCR as PID progresses is studied. The electrical behavior demonstrates that the detection sensitivity is robust to PID degradation rate and temperature and that the degradation rate is not related to the initial shunt resistance of the PV cell. The temperature behavior indicates that the temperature coefficient of the FDCR is initially negative and increases toward more positive values as PID progresses. Furthermore, the electrical variation of the FDCR with PID progression is much higher (74%) than the variation of the FDCR due to temperature (19%) and this favors PID detection.

Index Terms—Early detection, electrical behavior, forward dc resistance (FdcR), photovoltaic (PV), potential-induced degradation (PID), shunt resistance, temperature behavior.

I. INTRODUCTION

POTENTIAL-INDUCED degradation (PID) is a major performance loss issue for photovoltaic (PV) systems [1], [2]. Laboratory tests on PV modules from 13 manufacturers have revealed that more than 50% of them are prone to PID under various test conditions [3]. This can affect the performance

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and the reliability of high-voltage PV systems due to their increased degradation rate. A low-cost sensor, which would warn the user for the early development of PID, could alleviate the problem. In this work, a method, which can be implemented in a low-cost sensor, for detecting PID of the shunting type (PID-s) is presented.

The first method used to detect PID is electroluminescence [4]–[6]. Although 1% detection accuracy could be achieved, its main disadvantage is that PV modules have to be dismantled for indoor testing. Other methods, which avoid module dismantling are outdoor electroluminescence [7], [8], outdoor photoluminescence [9], [10], and drone copter thermography [11]. The main disadvantage of outdoor methods is the high equipment and labor cost. The cost can be reduced by using detection methods which measure electrical parameters. The PV module leakage current was proposed; however, the results in the literature are not consistent. On one hand, it was demonstrated that it correlates with the power loss caused by PID [12], whereas other researchers have demonstrated that this is not valid [13], [14]. Nevertheless, measuring the leakage current in a PV system is not practical since the aluminum frame of the PV modules is grounded for safety reasons. Another method, based on current-voltage (*IV*) curves was proposed [15]–[17]. This method can estimate the maximum power output of a PV module with PID progression with an accuracy of 3%. Another approach is the use of the *IV* slope near the short-circuit current to estimate the shunt resistance (R_{sh}) of a PV cell. The shunt resistance changes steeply with PID progression [18]–[22] before any significant power loss, and could be used to monitor PID. The use of the aforementioned *IV* methods is not an optimum choice for two reasons. First, the current during the measurement is relatively high (~8 A) and does not enable the use of a low-cost sensor (high-power electronics are required). Second, the use of high-current signals (>10 mA) decreases the detection sensitivity and do not allow for the early detection of PID. Impedance spectroscopy was also proposed as another detection method [23]–[25]. Impedance spectroscopy uses low-current signals; however, the cost of the electronic circuit is not adequately low due to the use of high-frequency ac signals.

The cost can be reduced even more by using partial *IV* curves which use low-current dc signals. In the literature [19],

[20], [26], [27], it was shown that dark *IV* curves are a good indicator for PID progression. However, this was shown only qualitatively. In this work, it is demonstrated quantitatively as well, i.e., at what current values the detection of PID is more sensitive. Furthermore, the effect of the PID degradation rate and temperature on the detection sensitivity is presented.

Our target is to develop a method for the early and reliable detection of PID and exploit this for the development of a low-cost sensor. We have demonstrated [28] that the measurement of the forward dc resistance (FdcR) in single-cell PV modules at low forward bias conditions can be used for the early detection (< 2% power loss) of PID-s that affects p-type crystalline PV cells [29] which dominate the market. Because of the low-current dc signals applied, the FDCR method can be embedded in a low-cost sensor. The low-cost sensor advantage stems from the fact that the FDCR is measured at low bias currents (<10 mA). This allows for low power and, hence, low-cost electronics to be used for the implementation of such a sensor. It was shown that the FDCR exhibits a steep change with PID progression. In addition, it was shown that the detection sensitivity of the FDCR method is independent of the PID history of the PV cells. In this work, the effect of the PID degradation rate (i.e., how fast the output power of a PV cell decreases) and temperature on the detection sensitivity (electrical behavior) of the FDCR method for PID detection are examined. What is more, the effect of temperature (temperature behavior) on the FDCR as PID progresses is studied. It is important to analyze the temperature behavior in order to deduce the degree to which it affects the electrical behavior of the FdcR. This study is based on single-cell and multi-cell PV modules and is the pathway for the development of a PID detection method at system level.

A number of authors have considered the temperature behavior of the crystalline silicon technology in the presence of PID. Desharnais [30] demonstrated the effect of different temperature values (25–65 °C) on the power loss because of PID under different irradiance values. Spataru *et al.* [16] presented a temperature correction method for a proposed *in situ* power-loss estimation method from 25 to 60 °C. Luo *et al.* [17] presented a different temperature correction method for the same *in situ* power-loss estimation method from 25 to 50 °C. The aforementioned work describes results on multi-cell PV modules. This cannot reflect the temperature behavior of a single PV cell with PID progression. Because of the uneven PID degradation of the PV cells in a multi-cell PV module, it is not possible to accurately extract the temperature behavior of a single PV cell from the average temperature behavior of the whole PV module. A more recent study by Kasu *et al.* [31] examined the temperature behavior of monocrystalline single-cell PV modules; however, the study was only at standard test conditions (STC). Consequently, the available data in the literature are not adequate to extract the temperature behavior of the FDCR method for PID detection. Therefore, in this work, the temperature behavior of the FDCR is examined in single-cell PV modules under various forward bias currents as PID progresses.

The novelty of this work is that new data are provided regarding the temperature behavior of multicrystalline silicon PV cells with PID progression (i.e., at different PID stages)

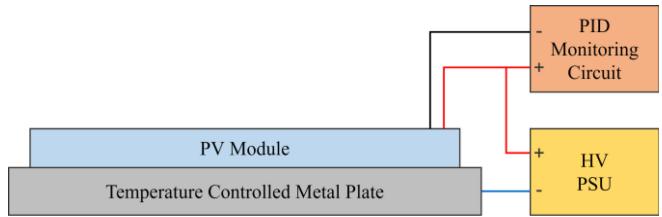


Fig. 1. Indoor PID test setup for inducing PID and monitoring its progression in single-cell PV modules.

from 0 to 60 °C. From the data, the effect of temperature on the FDCR method for PID detection is analyzed. Although the FDCR method is based on the measurement of the FDCR at low forward bias currents, the temperature behavior analysis is performed on a wider range of forward bias currents to provide an insight into the nature of the PID shunting. Furthermore, the detection sensitivity of the FDCR method is examined for different PID degradation rates and temperatures. Finally, the FDCR method for PID detection is demonstrated for the first time on multi-cell PV modules.

II. EXPERIMENTAL SETUP

The experiments were conducted by using single-cell and multi-cell crystalline silicon (c-Si) PV modules as test samples.

A. Single-Cell Module

The single-cell PV module samples were made of multicrystalline p-doped base and n-doped emitter (emitter pointing toward the front glass), 3 mm thick glass, 15505P/UF EVA encapsulant, and TPT Akasol PV1000V back-sheet. The refractive index of the antireflective coating varied from 2.05 to 2.08 (measured with ellipsometry). The cell area was 243.4 cm² and the total surface area of the module was approximately 400 cm².

To induce PID to the PV samples, an indoor test setup was implemented that allowed the temperature of the sample under test to be controlled, while a high-voltage (HV) bias was applied at the same time under dark conditions by using a power supply unit (PSU), as shown in Fig. 1. The glass facing side of the sample was placed on the temperature-controlled metal plate which was connected to the negative (−ve) terminal of the HV PSU. The power terminals of the sample were connected to the positive (+ve) terminal of the HV PSU via the PID monitoring circuit (PMC). The PMC was controlled to measure the dc resistance (4-wire measurement) at various forward/reverse bias conditions in order to monitor the progression of PID.

The setup was placed in a dark room and a source-meter device was used to acquire dark *IV* curves (4-wire measurement). The dark *IV* curves were used to analyze the FDCR variation with PID progression and temperature at various forward bias conditions.

B. Multi-cell Module

The multi-cell PV module samples were standard 60-cell PV modules (1640 × 992 × 40 mm) made of 60 p-doped base



Fig. 2. Outdoor test setup for inducing PID and monitoring its progression in multi-cell PV modules.

and n-doped emitter (emitter pointing toward the front glass) polycrystalline cells, high-transmission low iron tempered glass (AR coated), EVA encapsulant, and composite film back-sheet. The modules were rated for a system voltage of 1000 V dc and were protected by three diodes in the junction box.

To induce PID to the PV samples, an outdoor test setup was implemented that allowed the application of an HV bias under light and dark conditions by using a HV PSU (see Fig. 2). The aluminum frame of the samples was connected to the negative (−ve) terminal of the HV PSU. The power terminals of the sample were connected to the positive (+ve) terminal of the HV PSU via the PMC (similar to that in Fig. 1). One of the modules (right) was kept as a reference (no HV bias). The other module (left) was covered with black aluminum foil (to accelerate PID and to achieve as even degradation as possible in all cells). The foil was electrically connected to the aluminum frame of the module. The samples were operating at open-circuit condition.

The PMC was measuring the FDCR at night with a 2-wire measurement (4-wire was not necessary because of the low bias currents, <10 mA, during the measurement).

C. Equipment

In addition to the aforementioned equipment, a solar simulator was used to determine the maximum power of the PV samples at STC. The measurement error of the equipment used is shown in Table I.

TABLE I
EQUIPMENT AND MEASUREMENT ERROR

Equipment	Measurement Error
HV PSU	< 1.0%
Source-Meter (Keithley 2430)	< 0.1%
Temperature sensors (RTD)	< 0.5%
PID monitoring circuit (PMC)	< 1.0%
Solar Simulator (Pasan A+A+A+)	< 1.0%*

* For the single-cell PV samples, the combined error was < 0.5%. The combined error is < 1% (temporal instability < 0.15%, irradiance uniformity < 0.51% and maximum power measurement < 0.23%). However, the single-cell sample under test was always placed at the same location in the solar simulator and, hence, the irradiance uniformity error was insignificant.

III. METHODOLOGY

The methodology followed to obtain the results includes the experimental PID progression and the electrical and temperature behavior stages for single-cell and multi-cell PV samples.

A. Potential-Induced Degradation Progression (Single-Cell)

For the single-cell PV samples, PID was induced by continuously applying a voltage of -1000 V dc under dark conditions (indoor dark room). During the HV bias, the PV sample temperature was kept constant at 60°C ($+/- 1^\circ\text{C}$) to accelerate the test time.

The PID progression was monitored by measuring the shunt resistance (R_{sh}) of the PV samples by using the PMC. The shunt resistance was approximated by measuring the reverse dc resistance of the sample. Although the reverse dc resistance does not vary linearly with voltage, it provides a good approximation of the shunt resistance when measured at low reverse bias conditions [32]. The shunt resistance can be measured at forward bias as well but it requires very low bias conditions (<100 mV) [33] in order for the PV cell to be in a linear region and, hence, this was not implemented on the single-cell samples because of the limitations of the PMC. The shunt resistance was measured at a reverse bias voltage of 0.5 V. The voltage was applied to the electrical terminals of the PV sample and the shunt resistance was calculated based on the measured current. The measurement was conducted with a sampling rate of 10 s for a short period of time, i.e., every 10 s, a measurement was acquired for a duration of 75 ms. This was performed in order not to bias the sample continuously and possibly affect its PID progression.

The PMC was able to measure the shunt resistance while the HV bias was being applied in order to avoid any capacitive currents, which could affect PID progression, if the HV was switched ON/OFF every 10 s.

B. Potential-Induced Degradation Progression (Multi-Cell)

For the multi-cell PV samples, PID was induced by continuously applying a voltage of -1000 V dc under light and dark conditions (outdoor setup). The temperature of the samples was

TABLE II
RELATION OF PID DEGRADATION LEVEL TO SHUNT RESISTANCE VALUES AND RELATIVE POWER LOSS AT EACH LEVEL

PID Degradation Level	R_{sh} (Ω)	Sample (S) Power Loss (%)				
		S1	S2	S3	S4	Mean
L1	R_i	0	0	0	0	0
L2	10	2.03	2.71	0	1.81	1.64
L3	5	3.72	15.8	0.83	3.49	5.96
L4	2.5	7.31	19.8	8.34	8.68	11.0
L5	1	13.8	29.7	17.9	16.1	19.4
L6	0.5	30.1	38.6	25.5	29.0	30.8
L7	0.25	54.2	48.9	50.2	49.0	50.6

The shunt resistance (R_{sh}) was measured at -0.5 V and 60 °C.
 R_{sh} before PID (R_i) was 50, 60, 40 and 126 Ω for S1, S2, S3 and S4.
The maximum power (STC) before PID was 3.20, 2.87*, 2.78* and 3.10 W for S1, S2, S3 and S4.
* The power measured by the solar simulator for S2 and S3 was lower than S1 and S4, mainly, because the electrical terminals of S2 and S3 were 100 cm longer than S1 and S4. The terminals were made of 6 mm² solar cable (PV1-F) which has an electrical resistivity of 3.39 m Ω /m at 20 °C.

not controlled but it was determined by the ambient temperature and the solar irradiance.

The PID progression was monitored by measuring the FDCR at low forward bias conditions (<10 mA) by using the PMC. It was demonstrated (on single-cell PV modules) that measuring the FDCR at low bias conditions provides high sensitivity to PID progression [28]. In this work, this concept is tested on multi-cell PV modules. An electrical current was applied to the electrical terminals of the PV sample and the FDCR was calculated based on the measured voltage. The measurement was conducted with a sampling rate of 10 s for a short period of time, i.e., every 10 s, a measurement was acquired for a duration lower than 150 ms. This was performed in order not to bias the sample continuously and possibly affect its PID progression.

The PMC was able to measure the FDCR while the HV bias was being applied in order to avoid any capacitive currents, which could affect PID progression, if the HV was switched ON/OFF every 10 s.

C. Electrical and Temperature Behavior (Single-Cell)

The electrical and temperature behavior of the single-cell PV samples was deduced by acquiring and analyzing dark IV curves at various temperatures.

Dark FDCR curves were calculated from the dark IV curves to analyze the FDCR behavior with PID progression under a wide range of forward bias conditions, as well as, to estimate the shunt resistance with higher accuracy. Typical dark FDCR curves were previously published in [34]. Dark FDCR curves were recorded before starting the PID test (i.e., before applying the high voltage), and then, every time the shunt resistance (R_{sh}) was reaching certain PID degradation levels (L), as defined in Table II.

At each of those PID levels, the temperature was changed from 60 to 0 °C and dark IV curves were acquired every 10 °C. The temperature of the PV sample (T_s) during each IV curve

acquisition was kept within +/- 0.5 °C of its target value. During the temperature sweep, the temperature of the sample was reduced from 60 to 40 °C within less than 5 min in order to minimize PID recovery effects. The total temperature sweep time was less than 30 min. Furthermore, each dark IV curve was performed in less than 5 s to keep the temperature change of the sample lower than 0.25 °C (verified by a thermal simulation).

D. Electrical and Temperature Behavior (Multi-Cell)

The electrical and temperature behavior of the multi-cell PV samples was deduced by measuring the FDCR and sample temperature at night (between 22:00 and 04:00). The FDCR was measured at forward bias currents lower than 10 mA. The FDCR change and the temperature coefficient of the FDCR were analysed with PID progression.

E. Power Loss Measurement

The output power (P_{out}) of the PV samples was measured at STC by using a solar simulator.

For the single-cell PV samples, the output power was measured before the PID test and after each temperature sweep as PID was progressing (see before). The maximum power measurement was performed in less than 15 min after the temperature sweep in order to minimize PID recovery effects.

For the multi-cell PV samples, the output power was measured before the PID test and at various PID stages as PID was progressing. The progression was based on the measured FDCR value, and at each stage, the FDCR was approximately half of the previous stage. It was not possible to define PID degradation levels and perform a measurement at each level (similar to the single-cell samples) because the FDCR was measured only at night. The maximum power measurement was performed in less than 30 min after the HV bias was removed in order to minimize PID recovery effects.

F. Electroluminescence Imaging

Electroluminescence images were captured for the multi-cell PV samples after each output power measurement (see before). The sample was biased at a current of 1 A. The measurement was conducted in less than 30 min after the output power measurement in order to minimize PID recovery effects.

IV. RESULTS

A. Potential-Induced Degradation Progression (Single-Cell)

The progression of PID induced in the single-cell PV samples was monitored by measuring the shunt resistance (R_{sh}) of the PV samples, as shown in Fig. 3. It can be observed that samples 1 and 4 degrade within a few hours, whereas the degradation time for samples 2 and 3 is orders of magnitude longer. As will be shown later, the different degradation times are useful to prove that the sensitivity of the FDCR method for PID detection is not affected by the PID degradation rate. Furthermore, no relation between the initial shunt resistance and the degradation time can be observed.

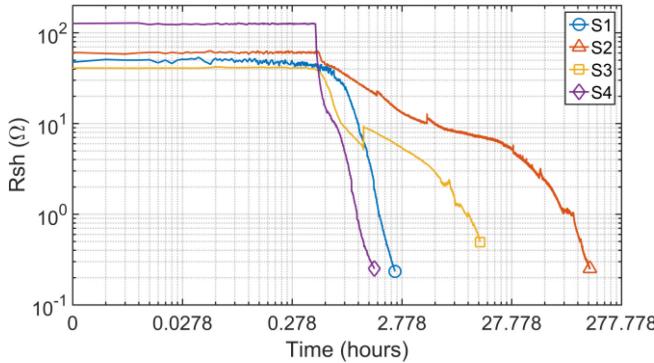


Fig. 3. Shunt resistance (R_{sh}) measurement against time (PID progression) for each PV sample (S).

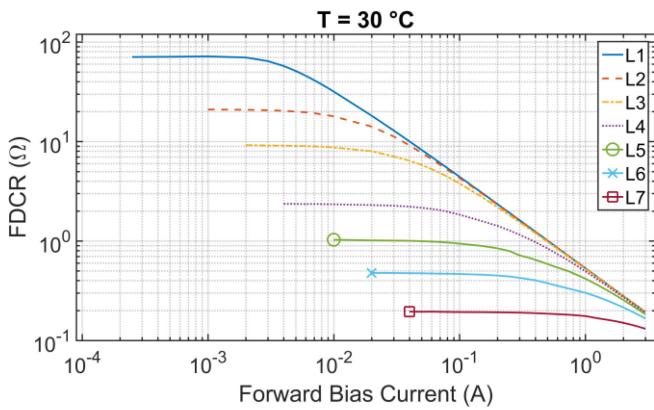


Fig. 4. FDCR against forward bias current (for sample 3) at different PID levels (L) for a PV sample temperature (T) of 30°C .

As mentioned earlier, dark *IV* and maximum power measurements were performed each time PID progression was reaching a certain degradation level. The PID progression was monitored by measuring the shunt resistance (R_{sh}); hence, the degradation levels were defined on a shunt resistance basis, as shown in Table II. The electrical and temperature behavior of the FDCR with PID progression was studied at those levels, as presented later. The relative power loss of the samples is presented as well.

B. Electrical Behavior (Single Cell)

The FDCR variation with PID progression (electrical behavior) in single-cell PV samples was deduced from dark *IV* (dark FdcR) curves. To derive the electrical behavior of the FdcR, the FDCR was plotted against the forward bias current for the different PID levels (L1–L7) at the same temperature, as shown in Fig. 4. This allows the observation of the FDCR variation (sensitivity) with PID progression (from PID L1 to L7) for the various forward bias currents at which the FDCR is measured. From the results, it is observed that the FDCR variation is higher as the forward bias current decreases. The reason for this behavior is explained in [28].

Since our interest is to detect PID before 1% power loss occurs, the percentage FDCR change from PID level 1 (L1) to PID level 2 (L2) was calculated using (1). PID L2 was selected

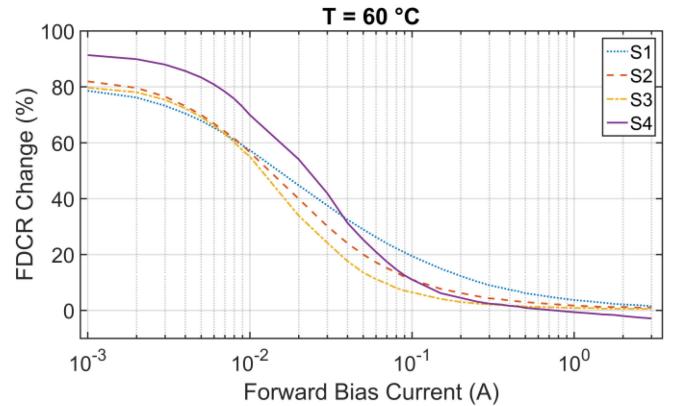
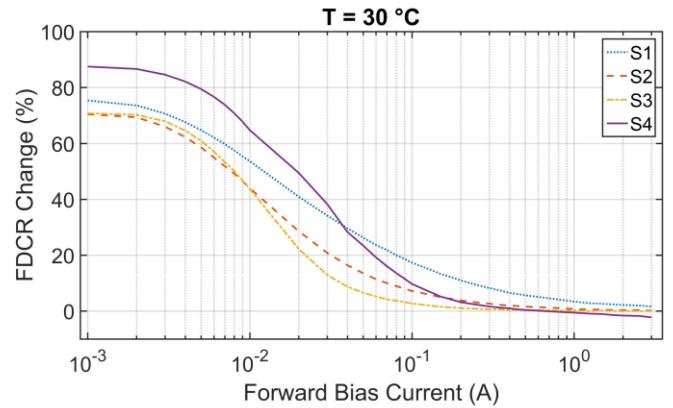
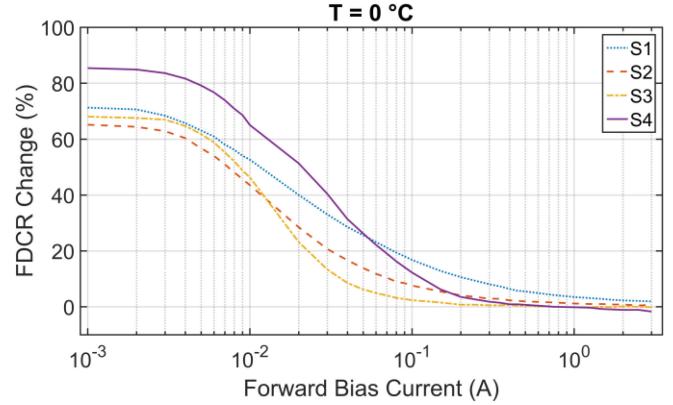


Fig. 5. FDCR change (from PID L1 to L2) against forward bias current for each PV sample (S) at PV sample temperatures (T) of 0, 30, and 60°C . The FDCR change was calculated from PID L1 to L2 using (1).

since the average power loss is lower than 2% (see Table II). Although it is theoretically possible to detect PID before 1% power loss, it was not possible to test it experimentally because of practical limitations

$$FDCR_{\text{change}} = \frac{FDCR_{L1} - FDCR_{L2}}{FDCR_{L1}} * 100\%. \quad (1)$$

As it can be seen (see Fig. 5), the FDCR change (sensitivity to PID progression) increases as the forward bias current decreases; the maximum FDCR change occurs at 1 mA (available equipment limits for PID $L > 1$). The results are presented in more detail in Table III. It can be observed that the FDCR

TABLE III
 Δ FDCR CHANGE FROM, PID L1, TO L2, AT DIFFERENT TEMPERATURES

Temperature (°C)	Sample (S) FDCR Change at 1 mA (%)				
	S1	S2	S3	S4	Mean
0	71.3	65.1	68.0	85.4	72.5
30	75.4	70.4	70.8	87.5	76.0
60	78.6	81.9	79.7	91.3	82.9
Δ Change, 60 °C to 0 °C	7.3	16.8	11.7	5.9	10.4

The FDCR change was calculated from PID L1 to L2 using (1).

For reference, at PID L1 R_{sh} was 76, 78.8, 64 and 134 Ω for S1, S2, S3 and S4. At PID L2 R_{sh} was 11.9, 13.3, 12.6 and 10.2 Ω for S1, S2, S3 and S4. The PV samples shunt resistance (R_{sh}) was estimated from the dark FDCR curves at 60 °C.

change depends on temperature; however, its average (mean) value remains high (>72%) for the whole temperature range. For each sample, the minimum (72.5%) and maximum (82.9%) FDCR change occurs at 0 and 60 °C, respectively. Its average variation from 0 to 60 °C is 10.4%. This means that the FDCR method for PID detection poses high detection sensitivity in a wide temperature range.

As was indicated earlier (see Fig. 3), the samples degraded with a different rate (time to degrade from PID L1 to L7). In addition, as can be seen from Table III, the FDCR change with PID progression (from PID L1 to L2) for each sample is higher than 65%, 70%, and 78% at 0, 30, and 60 °C, respectively. This leads to the important outcome that the sensitivity of the proposed FDCR method for PID detection remains high and it is not significantly affected by the PID degradation rate. The difference in the FDCR change values among the samples is due to the different initial (PID L1) shunt resistance (R_{sh}) values of each sample. The results provide convincing evidence that the sensitivity of the FDCR method for PID detection is robust to the degradation rate and temperature conditions.

C. Temperature Behavior (Single-Cell)

The FDCR variation with temperature (temperature behavior) in single-cell PV samples was deduced from dark IV (dark FdcR) curves. The results present the effect of temperature on the FDCR at the different PID levels (L1–L7) for various forward bias current values (at which the FDCR was measured).

From the results, it was deduced that the FDCR exhibits a nonlinear TC; therefore, the TC was calculated for two temperature ranges. The first range is from 0 to 30 °C and the second one was from 30 to 60 °C. In each temperature range, the FDCR is assumed to change linearly with temperature and the TC was calculated by using (2) and (3). The FDCR values at 30 °C, which were used to calculate the TC, are shown in Table IV

$$TC_{0-30} = \frac{FDCR_{30} - FDCR_0}{FDCR_{30} * 30} * 100\% / ^\circ C \quad (2)$$

$$TC_{30-60} = \frac{FDCR_{60} - FDCR_{30}}{FDCR_{30} * 30} * 100\% / ^\circ C. \quad (3)$$

The TC of the FDCR of each sample was analyzed at each PID level (L1–L7) for various forward bias currents, as presented in Fig. 6. At each PID level (L1–L7), the FDCR TC was calculated

TABLE IV
FDCR AGAINST FORWARD BIAS CURRENT AT DIFFERENT PID LEVELS (L)

Current	FDCR (Ω) at 30 °C						
	L1	L2	L3	L4	L5	L6	L7
3 A	0.194	0.194	0.19	0.186	0.180	0.168	0.147
1 A	0.532	0.528	0.497	0.465	0.401	0.303	0.198
100mA	4.37	4.00	3.04	1.85	0.858	0.435	0.226
10 mA	29.83	15.65	7.40	2.76	0.96	-	-
1 mA	74.38	20.98	8.53	-	-	-	-
100 μA	75.40	-	-	-	-	-	-

for each sample (S), as well as, the average (mean) FDCR TC of all the samples.

From the results, the overall temperature behavior for forward bias currents higher than 10 mA is that the FDCR TC is initially (PID L1) negative and remains about the same until PID reaches a level (the level is current dependent, the higher the current the higher the PID level the TC remains constant) after which the TC starts to increase. In some cases, the TC changes from negative to positive. This is assumed to be due to the positive TC of sodium metallic paths [35] that form in the PV cell junction [36] and counterbalance the negative TC of the forward conduction of crystalline PV cells. A more thorough explanation for this behavior can be realized by considering the single-diode model of a PV cell [28]. The higher the forward bias current, the more the diode dominates the conduction path. Therefore, the TC is dominated by the negative TC of the diode and more sodium accumulation is required (i.e., PID has to progress more) to affect the TC. Another hypothesis for the increase of the TC with PID progression is the effect of the TC of the series resistance of the PV cell. This is because the shunts because of PID are highly localized and lateral currents flow through the metallic grid contacts and bulk silicon [37], [38]. The series resistance might affect the TC at currents higher than 100 mA. At lower currents, the dominant factor for the change in the TC is the accumulation of sodium in the junction. At the forward bias current of 1 mA, the FDCR TC did not change from negative to positive because the equipment used was not able to measure the FDCR at higher PID degradation levels.

In [16], [17], and [30], it was presented that the TC of the maximum power of a PV module is negative and increases toward a more positive value as PID progresses (i.e., the temperature effect on the maximum power is lower as PID progresses). This is in agreement with the calculated TC of the FdcR, which also increases from a negative value toward a more positive value. If the FDRC TC is converted to a forward voltage TC, the forward voltage is affected to a lower degree by temperature as PID progresses. Therefore, the PV module power is affected in a similar way since it depends on the voltage.

From a more careful examination of the results, for forward bias currents higher than 100 mA, the FDCR TC value increases monotonically as PID progresses from L1 to L7. On the other hand, for forward bias currents lower than 100 mA, the FDCR TC decreases first, and then, increases as PID progresses. The

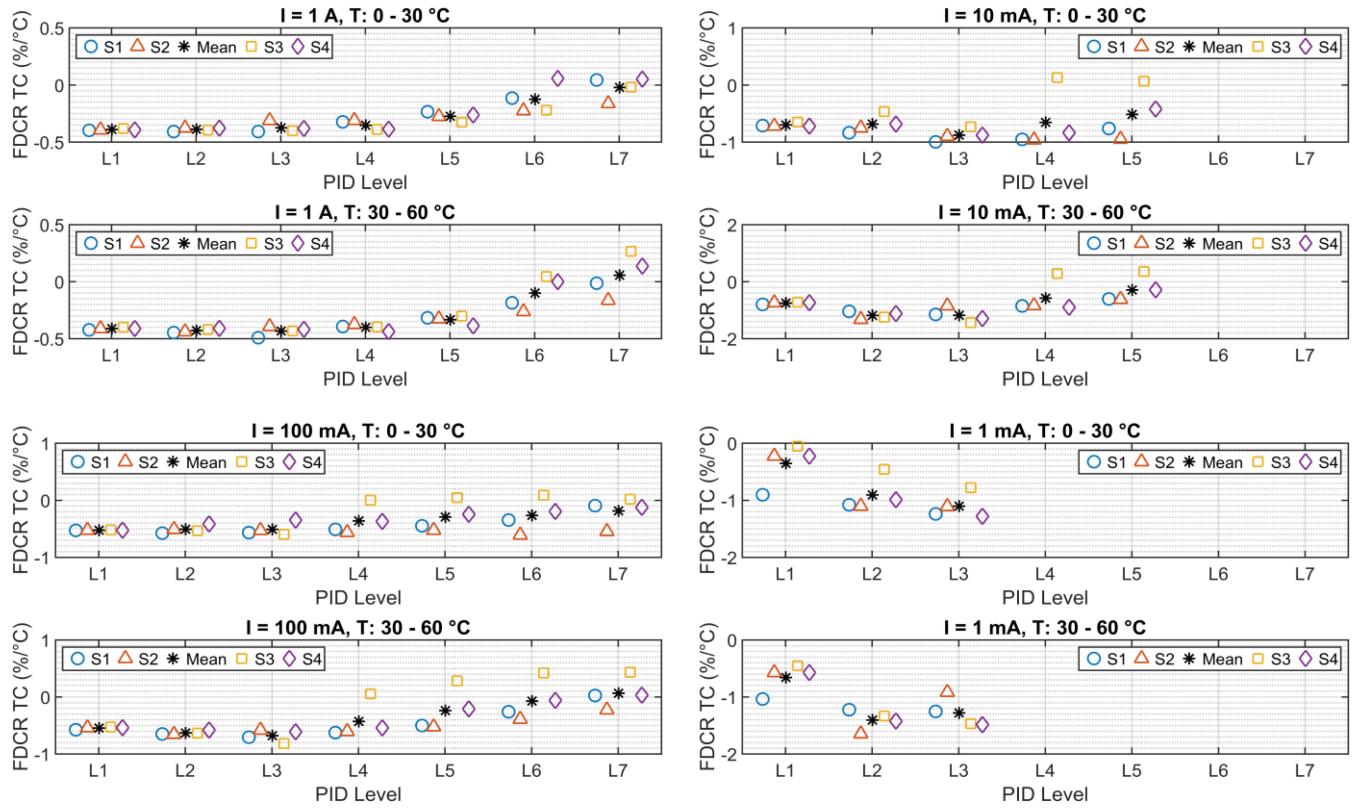


Fig. 6. FDCR TC against different PID levels at forward bias currents of 1 A, 100 mA, 10 mA, and 1 mA. The TC was calculated for two temperature ranges (0–30 °C and 30–60 °C) for each of the PV samples (S) and their average TC (mean).

possible reasons for the overall increase of the TC were explained earlier. The reason for the initial decrease of the TC might be because of the low number of sodium atoms in the junction, which act as donors [39] and, hence, more electrons are released when the temperature increases (negative TC). As the number of sodium atoms increases, sodium metallic paths (which exhibit positive TC) form across the PV cell junction and dominate the overall TC of the FdcR.

What is more, the FDCR TC values for all samples at PID L1 for forward bias currents higher than 10 mA are almost equal. If the average forward voltage TC is calculated, its value is –2.00, –2.14, and –2.34 mV/°C for 3 A (not shown in Fig. 6), 1 A and 100 mA, respectively. This is very close to the –2 mV/°C TC of a typical p-n junction.

In addition, for forward bias currents lower than 10 mA, the FDCR TC has significant variation (i.e., the values are spread out) at PID L1. This is because, at L1, the intrinsic shunt resistance dominates the conduction path and its TC varies from sample to sample because of the many nonlinear components which comprise the total shunt resistance [40]. A similar spread out of the TC values can be seen for the other PID levels, as well as, at forward bias currents higher than 100 mA for high PID levels at which the shunt resistance dominates the conduction path. This means that the temperature behavior of the shunt resistance formed across the PV cell junction because of sodium accumulation with PID progression varies from sample to sample and does not exhibit a stable behavior like the temperature behavior of the forward conduction of a healthy PV cell.

TABLE V
COMPARISON OF THE FDCR ELECTRICAL AND TEMPERATURE CHANGE

Temperature range	FDCR change due to PID (electrical) (%)	FDCR change due to temperature (%)
Low: 0 – 30 °C	74.25	19
High: 30 – 60 °C	79.45	31

The FDCR change was calculated at 1 mA from PID L1 to L2. The electrical change was calculated based on the average FDCR change in the electrical behaviour section for the respective temperature range. The temperature change was calculated based on the average FDCR TC in the temperature behaviour section for the respective temperature range.

A very important result that stems from Fig. 6 is that for forward bias currents higher than 10 mA, the FDCR TC has similar values in both temperature ranges (0–30 °C and 30–60 °C). On the other hand, at a forward bias of 1 mA, the TC of the low-temperature range is about half of the high-temperature range at PID levels of L1 and L2. This favors the proposed FDCR method for PID detection since it was demonstrated earlier that measuring the FDCR at 1 mA (available equipment limits for PID $L > 1$), offers the most sensitive condition for PID detection.

In order to evaluate the effect of temperature on PID detection, the electrical and temperature behavior of the FDCR had to be considered together. Therefore, the electrical and temperature change of the FDCR with PID progression are compared in Table V at 1 mA in both temperature ranges since the FDCR detection sensitivity and TC are different in each range (see before). Only the FDCR change from PID L1 to L2 was considered since

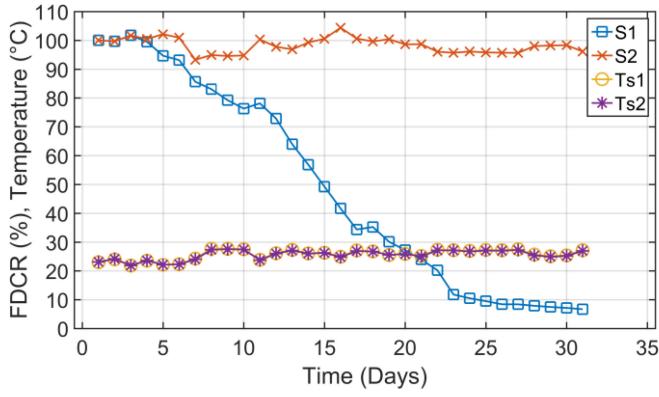


Fig. 7. Average FDCR and average sample temperature (T) against time (PID progression) for the induced fault sample (S1) and the reference sample (S2). The FDCR was measured between 10:00 P.M. and 04:00 A.M. each day. The FDCR on day 1 is 79.5 and $73.4\text{k}\Omega$ for S1 and S2 respectively. The FDCR is not temperature corrected. No HV bias on days 1 and 2.

TABLE VI
FDCR CHANGE AND RELATIVE CHANGE IN THE MAXIMUM OUTPUT POWER
OF THE SAMPLES WITH PID PROGRESSION

Time (Day)	FDCR (Ω)				Reference sample (S2)		
	Induced fault sample (S1)		Δ FDCR (%)	Δ Power (%)	FDCR (Ω)	Δ FDCR (%)	Δ Power (%)
1	79.5	0.00	0.00	73.4	0.00	0.00	0.00
12	58.0	-27.1	-0.90	71.8	-2.23	-0.25	
17	27.3	-65.6	-0.93	73.9	0.62	0.05	
31	5.32	-93.3	-2.00	70.6	3.87	0.59	

The initial (day 1) power is 256.9 and 253.0 W for S1 and S2 respectively.

the PV sample power loss was lower than 2% at L2 (see Table II). It can be observed that in the high-temperature range, the FDCR electrical change (79%) is higher than the temperature change (31%). A similar electrical change (74%) is observed in the low-temperature range; however, the temperature change (19%) is 12% lower than in the high-temperature range. This suggests that the FDCR should be measured at low temperatures since it offers the maximum differentiation between the electrical and temperature variation of the FDCR with PID progression.

D. Electrical Behavior (Multi-Cell)

The variation of the FDCR with PID progression (electrical behavior) in multi-cell PV samples was examined.

As mentioned earlier, the FDCR was measured only at night between 22:00 and 04:00. The average FDCR values and average sample temperature during that period are presented in Fig. 7. It can be observed that the FDCR of the induced fault sample (S1) reduces with PID progression, whereas the FDCR of the reference sample (S2) does not change with PID (it only changes with the temperature).

To evaluate the effectiveness of the FDCR for PID detection, the maximum power of the samples was measured as PID was progressing. Table VI shows the percentage FDCR change and

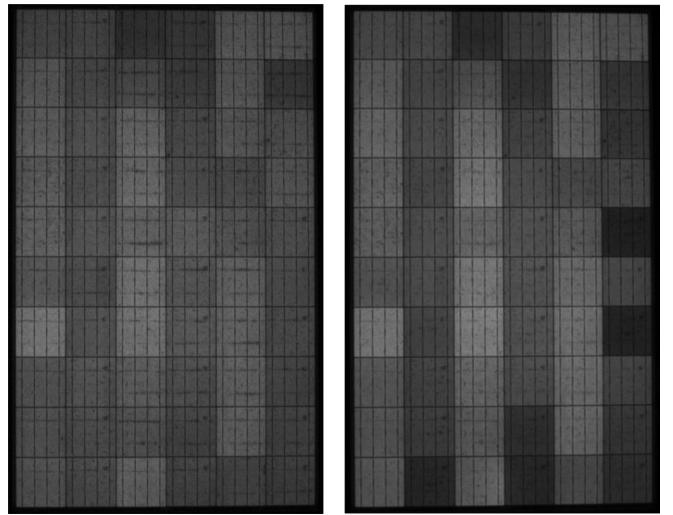


Fig. 8. Electroluminescence images of the multi-cell PV samples at 1 A on day 12 (left) and on day 31 (right) of the PID test.

the relative change in power of the samples. From the results, it is demonstrated that the FDCR of S1 changes by 93.3% before the output power of the sample decreases by 2%. On the other hand, the FDCR change of S2 is lower than 4%, while the change in its output power is lower than 0.6% (within the measurement uncertainty of the equipment). The results on the multi-cell PV samples verify that PID can be detected at an early stage (before 2% power loss) as predicted by the single-cell PV samples results presented in this article and in [28]. It is theoretically possible to detect PID before 1% power loss; however, it was not possible to test it experimentally because of practical limitations.

In addition to the maximum power measurement, the development of PID in the multi-cell PV samples was verified by electroluminescence images (see Fig. 8). It can be observed that on day 12, only a few PV cells demonstrated reduced luminosity, whereas on day 31, several cells demonstrated reduced luminosity. This is in agreement with the increased power loss on day 31. The overall FDCR decrease cannot be attributed only to the darker PV cells since the initial FDCR of each cell was approximately $1\text{k}\Omega$. The advantage of the FDCR method is that PV cells contribute to the decrease of the overall FDCR even before they appear to degrade in the electroluminescence images.

E. Temperature Behavior (Multi-Cell)

The variation of the FDCR with temperature (temperature behavior) in multi-cell PV samples was examined.

The TC of the PV samples was calculated based on the measured FDCR and sample temperature at night between 22:00 and 04:00 as PID was progressing (see Fig. 9). The TC of the induced fault sample (S1) is initially negative and increases toward more positive values with PID progression, as expected from the results on single-cell PV samples earlier. Despite the small variation, the TC of the reference sample (S2) remains close to its initial value.

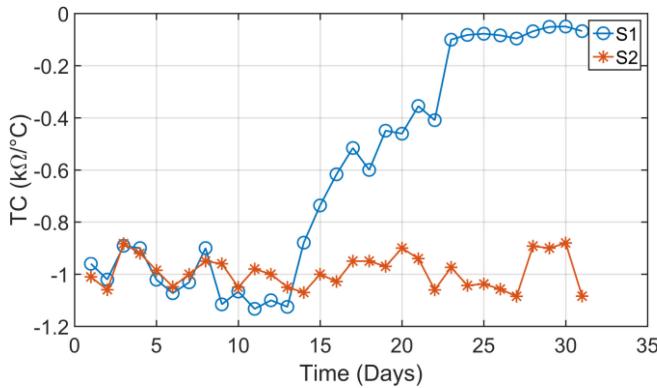


Fig. 9. TC against time (PID progression) for the induced fault sample (S1) and the reference sample (S2).

V. CONCLUSION

PID is a major degradation mechanism in PV systems that affects their performance and reliability. A method, which can detect PID at an early stage, can improve the reliability of PV systems and ensure high energy output. The measurement of the FDCR provides promising results for the early detection of PID (< 2% power loss). The FDCR method was tested on single-cell and multi-cell PV modules and it is the pathway for the development of a detection method at system level. To achieve this, the electrical and temperature behavior of the FDCR were studied. This article provided experimental data and analysis to examine the effect of PID degradation rate and temperature on the detection sensitivity (electrical behavior) of the FDCR method. Additionally, the effect of temperature (temperature behavior) on the FDCR as PID progresses was studied. The electrical behavior demonstrated that the FDCR change (detection sensitivity) with PID progression is robust to the PID degradation rate and temperature and that the degradation rate is not related to the initial shunt resistance of the PV cell. The FDCR change was examined at various forward bias currents and it was found that the maximum sensitivity to PID detection occurs if the FDCR is measured at 1 mA. Theoretically, the sensitivity increases at lower currents but it was not possible to test it with the available equipment. The temperature behavior indicated that the FDCR exhibits a negative TC, which increases toward a more positive value as PID progresses. In some cases of severe PID degradation, the TC changes from negative to positive. A possible reason is the positive TC of sodium metallic paths that form in the PV cell junction and counterbalance the negative TC of the forward conduction of crystalline PV cells. A comparison between the electrical and temperature behavior of the FDCR showed that the electrical change (>74%) is higher than the temperature change (<31%), and this favors PID detection. The FDCR should be measured at low temperatures since it offers maximum differentiation between the electrical and temperature change of the FDCR with PID progression.

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REFERENCES

- [1] J. Huang, Y. Sun, H. Wang, and J. Zhang, "Regular and irregular performance variation of module string and occurred conditions for potential induced degradation-affected crystalline silicon photovoltaic power plants," *Energies*, vol. 12, no. 22, 2019, Art. no. 4230.
- [2] J. Huang, H. Li, Y. Sun, H. Wang, and H. Yang, "Investigation on potential-induced degradation in a 50 MWp crystalline silicon photovoltaic power plant," *Int. J. Photoenergy*, vol. 2018, pp. 1–7, 2018.
- [3] M. Ebert, "Research group 'Reliability of solar modules and systems'- R&D competencies," 2015, doi: [10.13140/RG.2.1.1328.3280](https://doi.org/10.13140/RG.2.1.1328.3280).
- [4] T. Kropf, M. Schubert, and J. H. Werner, "Quantitative prediction of power loss for damaged photovoltaic modules using electroluminescence," *Energies*, vol. 11, 2018, Art. no. 1172.
- [5] K. G. Bedrich *et al.*, "Quantitative electroluminescence imaging analysis for performance estimation of PID-Influenced PV modules," *IEEE J. Photovolt.*, vol. 8, no. 5, pp. 1281–1288, Sep. 2018.
- [6] I. M. Kwembur, J. L. C. McCleland, E. E. van Dyk, and F. J. Vorster, "Detection of potential induced degradation in mono and multi-crystalline silicon photovoltaic modules," *Physica B, Condens. Matter*, vol. 581, 2020, Art. no. 411938.
- [7] L. Stoicescu, M. Reuter, and J. H. Werner, "DaySy: Luminescence imaging of PV modules in daylight," in *Proc. 29th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2014, pp. 2553–2554.
- [8] S. Koch *et al.*, "Outdoor electroluminescence imaging of crystalline photovoltaic modules: Comparative study between manual ground-level inspections and drone-based aerial surveys," in *Proc. 32nd Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2016, pp. 1736–1740.
- [9] R. Bhoopathy, O. Kunz, M. Juhl, T. Trupke, and Z. Hameiri, "Outdoor photoluminescence imaging of photovoltaic modules with sunlight excitation," *Prog. Photovolt.*, vol. 26, no. 1, pp. 69–73, 2017.
- [10] G. A. R. Benatto *et al.*, "Photoluminescence imaging induced by laser line scan: Study for outdoor field inspections," in *Proc. 7th IEEE World Conf. Photovolt. Energy Convers.*, 2018, pp. 395–399.
- [11] T. Kaden, K. Lammers, and H. J. Moller, "Power loss prognosis from thermographic images of PID affected silicon solar modules," *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 24–28, 2015.
- [12] T. Kawamura, Y. S. Khoo, T. Zhao, Y. Wang, and A. G. Aberle, "Quantitative analysis of relationship between leakage current and power loss of multi-crystalline silicon photovoltaic module during potential-induced degradation test," *Jpn. J. Appl. Phys.*, vol. 56, no. 12, 2017, Art. no. 122301.
- [13] M. Schwark *et al.*, "Investigation of potential induced degradation (PID) of solar modules from different manufacturers," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, 2013, pp. 8090–8097.
- [14] M. Florides, G. Konstantinou, V. Venizelou, G. Makrides, and G. E. Georgiou, "Potential induced degradation (PID) power loss correlation to leakage and reverse bias currents," in *Proc. 44th IEEE Photovolt. Spec. Conf.*, 2017, pp. 1941–1945.
- [15] P. Hacke, K. Terwilliger, and S. Kurtz, "In-situ measurement of crystalline silicon modules undergoing potential-induced degradation in damp heat stress testing for estimation of low-light power performance," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-5200-60044, 2013.
- [16] S. Spataru *et al.*, "Temperature-dependency analysis and correction methods of in situ power-loss estimation for crystalline silicon modules undergoing potential-induced degradation stress testing," *Prog. Photovolt. Res. Appl.*, vol. 23, no. 11, pp. 1536–1549, 2015.
- [17] W. Luo *et al.*, "In-situ characterization of potential-induced degradation in crystalline silicon photovoltaic modules through dark I-V measurements," *IEEE J. Photovolt.*, vol. 7, no. 1, pp. 104–109, Jan. 2017.
- [18] M. Bahr and K. Lauer, "Analysis of activation energies and decay-time constants of potential-induced degraded crystalline silicon solar cells," *Energy Procedia*, vol. 77, pp. 2–7, 2015.
- [19] A. Masuda, Y. Hara, and S. Jonai, "Consideration on Na diffusion and recovery phenomena in potential-induced degradation for crystalline Si photovoltaic modules," *Jpn. J. Appl. Phys.*, vol. 55, no. 2S, 2016, Art. no. 02BF10.
- [20] D. Lausch *et al.*, "Potential-Induced degradation (PID): Introduction of a novel test approach and explanation of increased depletion region recombination," *IEEE J. Photovolt.*, vol. 4, no. 3, pp. 834–840, May 2014.
- [21] M. B. Koentopp, M. Krober, and C. Taubitz, "Toward a PID test standard: Understanding and modeling of laboratory tests and field progression," *IEEE J. Photovolt.*, vol. 6, no. 1, pp. 252–257, Jan. 2016.
- [22] C. Taubitz, M. Schutze, and M. B. Koentopp, "Towards a kinetic model of potential-induced shunting," in *Proc. 27th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2012, pp. 3172–3176.

- [23] M. I. Oprea *et al.*, "Detection of potential induced degradation in c-Si PV panels using electrical impedance spectroscopy," in *Proc. 43rd IEEE Photovolt. Spec. Conf.*, 2016, pp. 1575–1579.
- [24] N. Katayama, S. Osawa, S. Matsumoto, T. Nakano, and M. Sugiyama, "Degradation and fault diagnosis of photovoltaic cells using impedance spectroscopy," *Sol. Energy Mater. Sol. Cells*, vol. 194, pp. 130–136, 2019.
- [25] T. Yeow, J. Sun, Z. Yao, J.-N. Jaubert, and K. P. Musselman, "Evaluation of impedance spectroscopy as a tool to characterize degradation mechanisms in silicon photovoltaics," *Sol. Energy*, vol. 184, pp. 52–58, 2019.
- [26] S. Spataru, D. Sera, P. Hacke, T. Kerekes, and R. Teodorescu, "Fault identification in crystalline silicon PV modules by complementary analysis of the light and dark current–voltage characteristics," *Prog. Photovolt. Res. Appl.*, vol. 24, no. 4, pp. 517–532, 2016.
- [27] P. Hacke *et al.*, "Testing and analysis for lifetime prediction of crystalline silicon PV modules undergoing degradation by system voltage stress," in *Proc. 38th IEEE Photovolt. Spec. Conf.*, 2012, pp. 1750–1755.
- [28] M. Florides, G. Makrides, and G. E. Georghiou, "Early detection of potential induced degradation by measurement of the forward DC resistance in crystalline PV cells," *IEEE J. Photovolt.*, vol. 9, no. 4, pp. 942–950, Jul. 2019.
- [29] W. Luo *et al.*, "Potential-induced degradation in photovoltaic modules: A critical review," *Energy Environ. Sci.*, vol. 10, pp. 43–68, 2017.
- [30] R. A. Desharnais, "Characterizing the impact of potential-induced degradation and recovery on the irradiance and temperature dependence of photovoltaic modules," in *Proc. 29th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2014, pp. 2346–2350.
- [31] M. Kasu *et al.*, "Temperature dependence of potential-induced degraded p-type mono-crystalline silicon cell characteristics," *Jpn. J. Appl. Phys.*, vol. 58, 2019, Art. no. 101005.
- [32] M. Florides, A. Livera, G. Makrides, and G. E. Georghiou, "Characterisation of the reverse DC resistance due to potential induced degradation (PID) in crystalline PV cells," in *Proc. 36th Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2019, pp. 1050–1053.
- [33] M. Florides, G. Makrides, and G. E. Georghiou, "Early potential induced degradation (PID) detection in the field: Voltage measurement methods," in *Proc. 33rd Eur. Photovolt. Sol. Energy Conf. Exhib.*, 2017, pp. 1677–1681.
- [34] M. Florides, G. Makrides, and G. E. Georghiou, "Characterisation of the shunt resistance due to potential induced degradation (PID) in crystalline solar cells," in *Proc. 7th IEEE World Conf. Photovolt. Energy Convers.*, 2018, pp. 695–699.
- [35] F. J. Bradshaw and S. Pearson, "The electrical resistivity of sodium between 78°K and 372°K," *Proc. Phys. Soc.*, vol. 69, pp. 441–448, 1956.
- [36] S. P. Harvey *et al.*, "Sodium accumulation at potential-induced degradation shunted areas in polycrystalline silicon modules," *IEEE J. Photovolt.*, vol. 6, no. 6, pp. 1440–1445, Nov. 2016.
- [37] M. Kasemann *et al.*, "Luminescence imaging for the detection of shunts on silicon solar cells," *Prog. Photovolt. Res. Appl.*, vol. 16, pp. 297–305, 2008.
- [38] O. Breitenstein, J. Bauer, T. Trupke, and R. A. Bardos, "On the detection of shunts in silicon solar cells by photo- and electroluminescence imaging," *Prog. Photovolt. Res. Appl.*, vol. 16, pp. 325–330, 2008.
- [39] P. Doubrava, "The electrical properties of silicon with sodium donors," *Solid State Phys.*, vol. 40, pp. 483–492, 1970.
- [40] O. Breitenstein, J. P. Rakotonaina, M. H. Al Rifai, and M. Werner, "Shunt types in crystalline silicon solar cells," *Prog. Photovolt. Res. Appl.*, vol. 12, pp. 529–538, 2004.