



# Determining the potential barrier presented by the interfacial layer from the temperature induced *I–V* characteristics in Al/p-Si Structure with native oxide layer

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## ABSTRACT

The temperature induced current-voltage (*I–V–T*) characteristics of the Al/SiO<sub>2</sub>/p-Si diodes with the interfacial native oxide layer were experimentally investigated in present our study. The values of 24.35 and 1.02 eV for the tunneling factor ( $a\delta\sqrt{\chi}$ ) and the potential barrier presented by the interfacial layer ( $\chi$ ) were determined for the Al/SiO<sub>2</sub>/p-Si metal-insulator-semiconductor (MIS) diode. The  $\chi$  value obtained from the forward bias *I–V–T* characteristics of the SiO<sub>2</sub>/p-Si diode is a crucial result according to those from only room temperature *I–V* curves in literature studies. Furthermore, the temperature dependence of the apparent barrier heights of the forward bias *I–V–T* characteristics displayed a Gaussian distribution (GD) of inhomogeneous barrier heights (BHs). Thus, the standard deviation values of  $\sigma_{1,s0} = 147.65$  mV for high temperature range and  $\sigma_{2,s0} = 83.66$  mV for low temperature range were obtained from the GD plot of the BHs (the apparent BH versus  $(2kT)^{-1}$  plot). Again, for the mean barrier height  $\bar{\Phi}_{b0}$  from the GD plot of the BHs, the values of 1.16 eV and 0.70 eV were obtained from the high temperature region and low temperature region, respectively. Furthermore, the Richardson constant values of 54.66 and 58.42 A/K<sup>2</sup>cm<sup>2</sup> from these temperature regions are approximately 1.70 times higher than the theoretical value of 32 A/K<sup>2</sup>cm<sup>2</sup> of the p-type Si semiconductor.

## 1. Introduction

Metal-semiconductor (MS) contact is one of the most widely used rectifying contacts in the electronics industry. Due to the SiO<sub>2</sub> thin layer on the Si surface, Si semiconductor is commonly used in the electrical and electronics device industry. Unless the MS contacts are fabricated by cleaving the semiconductor in an ultrahigh vacuum or by molecular beam epitaxy, there always is a thin native oxide layer between MS contact. This native interfacial layer may be considered to be an insulator [1–7]. Therefore, the nonideal behaviors observed in electrical characteristics of the MS contacts can be generally attributed to the presence of interface layer, a full understanding the nature of their electrical characteristics is of greater interest [8–13]. It can be saturated the dangling bonds (unsaturation bonds) on the Si surface by the SiO<sub>2</sub> native oxide layer. The termination with SiO<sub>2</sub> thin layer causes variety of crucial properties of the silicon substrate after exposing to clean room

air. The dangling bonds on the surface of the semiconductor substrate can be stabilized with native oxidation process [1,8–10,14–18]. So, the deposition of an oxide layer on the semiconductor is more important process step in the MIS or MOS device fabrications [14,19–24]. The formation of ohmic contacts is also important because of the reaction between metal and semiconductors depending on the interfacial native oxide layer and the different metal used [17,18,23].

The purpose of this article is to determine the temperature-dependent behaviors of the interfacial parameters of the Al/SiO<sub>2</sub>/p-Si MIS diodes with the interfacial native oxide layer by means of the forward and reverse bias *I–V* characteristics in the temperature range 120–320 K with steps of 20 K. The analyzes and observations related to the devices at a given temperature alone not enough for us to perfectly understand the current transport mechanism across the device. Therefore, it is very important to determine the carrier tunneling factor and the transmission coefficient of the interfacial thin film and potential

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barrier presented by the interfacial layer for the Al/SiO<sub>2</sub>/p-Si MIS diodes by means of the temperature induced forward bias *I*-V-T characteristics. These interfacial parameters for the SiO<sub>2</sub>/p-Si MIS diodes were determined from only room temperature *I*-V data in literature studies. Therefore, the determining the  $\chi$  value from the temperature dependence of the forward bias *I*-V characteristics of the diode is a crucial result according to those from only room temperature *I*-V curves in literature studies. We calculated the values of  $(a\delta\sqrt{\chi}) = 24.35$  for hole tunneling factor and  $\chi = 1.02$  eV potential barrier presented by the interfacial native oxide layer. Furthermore, we explained the forward bias *I*-V-T characteristics of the device by means of the modified thermionic emission (TE) mechanism with Gaussian distribution (GD) of the barrier heights (BHs) because the temperature dependent zero bias apparent BHs of displayed a GD of inhomogeneous BHs [25–33].

## 2. Experimental details

It has been fabricated the Al/SiO<sub>2</sub>/p-Si/Al diodes using *p*-type Si (100) with resistivity of 1–10 Ω-cm. The *p*-type Si semiconductor has free carrier concentration of  $2.28 \times 10^{15} \text{ cm}^{-3}$ . The ohmic contact to *p*-type Si(100) wafers was evaporated using ultra-pure Al(%99,999), obtained p-Si/Al was annealed in N<sub>2</sub> atmosphere for 3 min at 550 °C. The native oxide layer on the clean front surface of the substrate was formed by exposing to clean room air before evaporating Schottky Al gate metal [34]. The front surface of pieces cut from the wafer with ohmic contact has been chemically cleaned using the RCA1 procedure and finally has been rinsed in ultra-pure water for 60 s. The Schottky gate metal contacts [34] were formed as dots of 1.75 mm diameter with evaporation of Al onto the SiO<sub>2</sub>/p-Si in vacuum chamber at  $10^{-6}$  Torr. A symbolic drawing of the Al/SiO<sub>2</sub>/p-Si/Al structure is given in Fig. 1. The capacitance-voltage (*C*-V) characteristics were measured by a HP model 4192A LF impedance analyzer; and the *I*-V-T characteristics at different temperatures by Keithley 2400 Picoammeter/Voltage Source.

## 3. Results and discussion

### 3.1. Capacitance and conductance-voltage characteristics

Fig. 2 shows the energy band diagram of a MIS diode under the forward bias, where  $\Phi_m$  is the metal work function,  $\chi_s$  is the electron affinity of semiconductor,  $\delta$  is the thickness of the interfacial layer,  $V_p$  is the potential difference between Fermi Level and the valence band edge in the neutral region, band,  $V_D = V_{D0} - V$  is the surface potential as a function of the applied forward bias,  $V_{D0}$  is the zero-bias value of the surface potential (diffusion potential),  $V$  is the voltage drop across the depletion region  $\Phi_{b0} = (V_{D0} + V_p)$  is the zero bias barrier height.

Fig. 3 (A) and (B) represent the forward and reverse bias *C*-V and *G*-V curves at 1000 kHz and room temperature. For the forward bias, a negative voltage was to the Al Schottky gate contact side (Al/SiO<sub>2</sub> side).

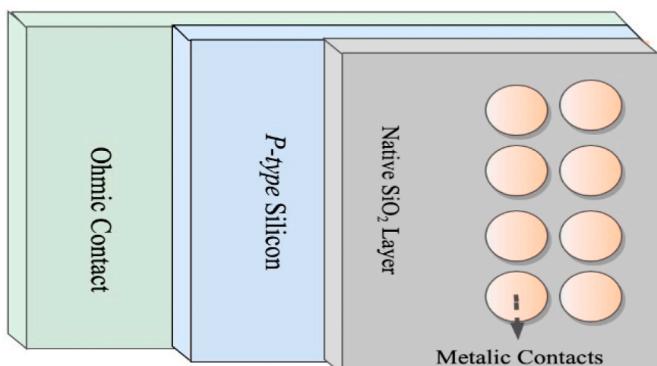


Fig. 1. The symbolic Al/SiO<sub>2</sub>/p-Si/Al structure.

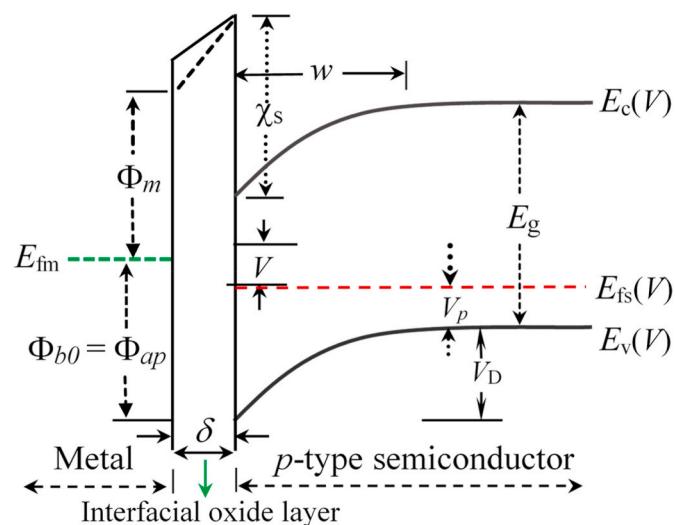


Fig. 2. Energy-band diagram for a metal/insulating layer/p-Semiconductor MIS structure under the forward bias condition.

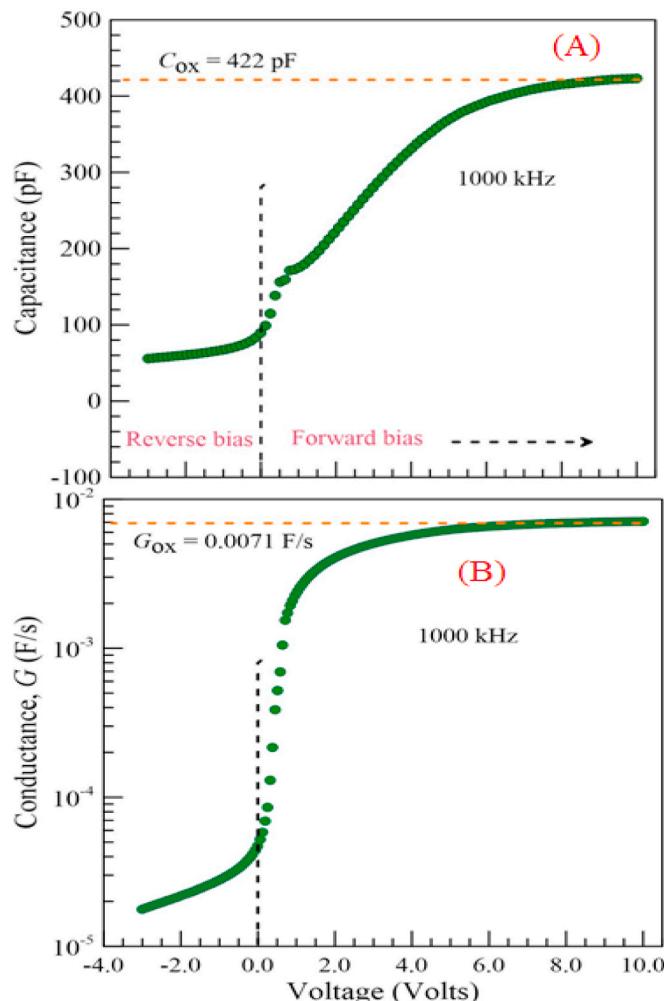


Fig. 3. Capacitance-conductance curves at 1000 kHz and 300 K.

Thus, the majority carrier holes will be pushed toward the native oxide layer/semiconductor interface and an accumulation layer of holes corresponds to the positive charge on the bottom Al Schottky gate contact of the MIS capacitor. When a small positive voltage was applied to the Al

Schottky gate contact side, the majority carriers are depleted. This is the “depletion case”. When a larger positive voltage was applied to the Al Schottky gate contact side, the number of electrons (minority carriers) at the surface is larger than that of the majority carrier holes. Thus, the *p*-Si surface is inverted. This is the “inversion case”. The depletion and inversion cases in the *p*-type MIS diode correspond to the reverse branch.

The accumulation region corresponds to the saturation region at about 7.5–10 V range at forward branch in Fig. 3(A). The capacitance value of  $C_{ox} = 422 \text{ pF}$  from accumulation region is the capacitance of the native oxide layer. Thus, the oxide layer thickness can be calculated using the expression below [18,20,24]:

$$C_{0x} = \frac{\epsilon_{ox}\epsilon_0 A}{\delta} \quad (1)$$

where  $\epsilon_{ox} = 3.9$  [35] is the permittivity of  $\text{SiO}_2$ , and  $A$  is the Schottky gate contact area,  $\epsilon_0$  is the permittivity of free space and  $\delta$  is native oxide thickness, respectively. A value of about 65.80 nm for the thickness of interfacial layer  $\delta$  is calculated using eqn. (1). But, we cannot obtain the actual value of the thickness of interfacial due to the effect of the series resistance ( $R_s$ ).  $R_s$  is the series resistance of the thickness of interfacial plus the neutral region of the semiconductor substrate. The neutral region is the part between the depletion region and ohmic contact. The  $R_s$  can cause some error in revealing of the interfacial layer properties. To prevent this, the desired information can be obtained after a correction is applied to the measured capacitance data. The  $R_s$  and interfacial layer capacitance  $C_{0x2}$  for the MIS structure can be defined as [36–39]:

$$R_s = \left[ \frac{G_{ma}}{(wC_{ma})^2 + G_{ma}^2} \right] \quad (2)$$

$$C_{ma} = \frac{C_{0x}}{1 + (wR_s C_{0x})^2} \quad (3)$$

$$C_{0x2} = C_{ma} \left[ 1 + \frac{C_{ma}^2}{(wC_{ma})^2} \right] \quad (4)$$

where  $C_{ma} = 422 \text{ pF}$  and  $G_{ma} = 7.10 \times 10^{-3} \text{ F/s}$  are the measured  $C$  and  $G$  in the strong accumulation region in Fig. 3(A) and (B). Eqn. (4) was obtained from eqns. (2) and (3). The  $C_{0x2}$  and  $R_s$  values were obtained as 3448 pF and  $123 \Omega$  using eqns. (2) and (4) for the accumulation region, respectively. This corrected capacitance value of  $C_{0x2} = 3448 \text{ pF}$  is eight higher than value of  $C_{0x} = 422 \text{ pF}$ . A corrected value of 8.06 nm for the thickness of the interfacial layer  $\text{SiO}_2$  was obtained using value of  $C_{0x2} = 3448 \text{ pF}$  in eqn. (1). As can be seen from explained above, the  $R_s$  entirely prevents interface trap loss, and particularly the equivalent parallel  $G$  is much more susceptible to the  $R_s$  rather than  $C$ . Therefore, the correction by taking account the  $R_s$  is especially crucial in  $G$  measurements [36,37].

Again, let us deal with the  $C$ -V and  $G$ -V curves in Fig. 3(A) and (B), the reverse branch case of the MIS diode, when a small positive voltage is applied to the  $\text{Al}/\text{SiO}_2$  side, with respect to the *p*-Si/Al; a positive charge will exist on the top Al Schottky contact (gate metal), some carrier holes will have electrical force away from the native oxide layer. When the holes are pushed away from the metal/native oxide layer, a negative space charge induced depletion region is formed owing to the ionized acceptor atoms. The free carrier density was calculated from the slopes of the  $C^{-2}$ -V curve in Fig. 4 using the following equation [1,18,40]:

$$N_A = \frac{2}{q \mathcal{E}_s \mathcal{E}_0 (dC^{-2}/dV) A^2} \quad (5)$$

The portion from 0.0 V to −3.0 V of the  $C^{-2}$ -V curve in Fig. 4 corresponds the reverse bias branch. As seen from Fig. 4, the  $C^{-2}$ -V curve shows two linear regions divided by a transition part. One them corresponds the depletion region of the device that the majority carriers are depleted which ranges about from 0.0 V to −0.6 V in Fig. 4, the other to

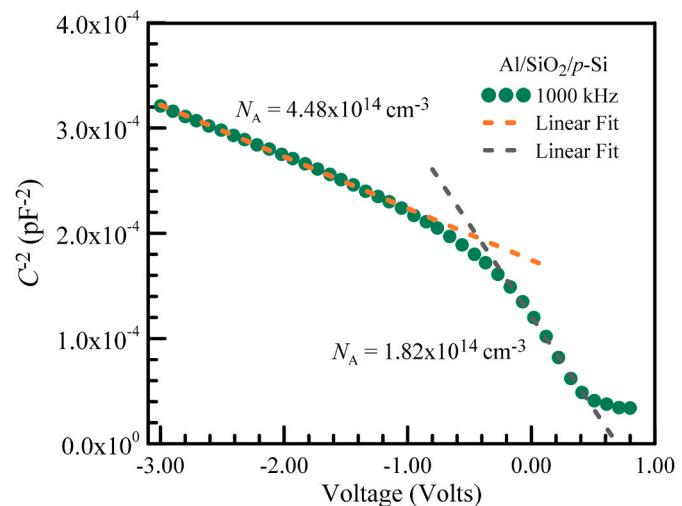


Fig. 4.  $C^{-2}$  versus voltage curve at 1000 kHz and 300 K.

the inversion region which approximately ranges from −1.0 V to −3.0 V in Fig. 4. At this case, the number of minority carriers at the surface is larger than the number of the holes and thus the surface of the *p*-type Si is inverted from a *p*-type to an *n*-type semiconductor and causes a larger induced space charge region. A majority carrier hole density of  $1.82 \times 10^{14} \text{ cm}^{-3}$  for the *p*-Si was calculated from the depletion part in the  $C^{-2}$ -V curve. A carrier density of  $4.48 \times 10^{14} \text{ cm}^{-3}$  was calculated from the inversion part of the  $C^{-2}$ -V curve.

Furthermore, the BH  $\Phi_{CV}$  from the  $C^{-2}$ -V curves can be determined by Refs. [1,18,40,41]:

$$C^{-2} = \frac{2(V_{D0} + V_0)}{q \mathcal{E}_s \mathcal{E}_0 N_A A^2} \quad (6)$$

As can be seen from Fig. 2, the diffusion potential is given by  $V_{D0} = (\Phi_{CV} - V_p)$ ,  $V_p$  is the potential difference between Fermi level and valence band maximum in the neutral region of *p*-type semiconductor, and it is stated by

$$V_p = kT \ln \left( \frac{N_V}{N_A} \right) \quad (7)$$

where  $N_V = 1.04 \times 10^{19} \text{ cm}^{-3}$  is the state density in the valance band [18]. A value of 0.25 V for  $V_p$  was obtained from the equation above. The value of  $\Phi_{CV}$  can be determined from the fit to linear depletion region in (0.0 V) – (−0.6 V) range of the  $C^{-2}$ -V curve in Fig. 4. That is, the intercept of the linear  $C^{-2}$  versus  $V$  plot with  $V$  axis is obtained as  $V_0 = V_{D0} = 0.70 \text{ V}$ . Thus, the  $\Phi_{CV} = (V_p + V_{D0}) = 0.95 \text{ V}$ .

### 3.2. Measurement temperature induced current-voltage characteristics

#### 3.2.1. Forward bias current-voltage characteristics

It is assumed that the total current flowing in a rectifying metal-semiconductor (MS) contact under bias is usually described within the thermionic emission (TE) theory and can be given as [42–44].

$$I = AA^* T^2 \exp \left( -\frac{e\Phi_{b0}}{kT} \right) \left[ \exp \left( \frac{eV - IR_s}{nkT} \right) - 1 \right] \quad (8)$$

where  $I_{s0}$  saturation current is given by

$$I_{s0} = AA^* T^2 \exp \left( -\frac{e\Phi_{b0}}{kT} \right) \quad (9)$$

$\Phi_{b0}$  is the barrier height at zero bias. This is maximum height of the valance band top in the semiconductor substrate relative to the metal Fermi level, and is distinct from the potential barrier presented by the native oxide layer at the MS interface.  $A^*$  is the effective Richardson

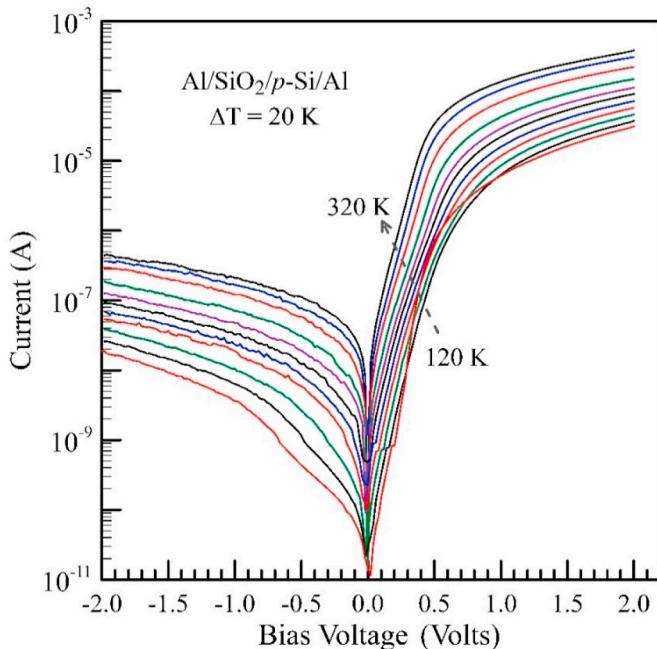
constant and equals  $32 \text{ A/cm}^2\text{K}^2$  for *p*-type Si, respectively, and  $n$  is an ideality factor stated with

$$n = \frac{q}{kT} \frac{dV}{d(\ell nI)} \quad (10)$$

**Fig. 5** shows the *I-V-T* characteristics of the MIS diode. The  $\Phi_{b0}$ ,  $n$  and other some parameters calculated for the MIS diode are given in **Table 1**. The  $\Phi_{b0}$  and ideality factor  $n$  take the values of 0.76 eV and 0.37 eV, and 2.36 and 4.01 for 300 and 120 K, respectively. The ideality factor of 2.36 being greater than unity at 300 K is an evidence of the existence of the native oxide layer at the Al/*p*-Si interface [1,17,20,22, 45–50]. Duman et al. [45] and Yıldız et al. [47] and Kumar et al. [50] obtained values of 0.81 and 0.63 and 0.67 eV at 300 K for Al/SiO<sub>2</sub>/*p*-Si diode, respectively.

In **Fig. 5**, the downward curvature above voltage region 0.50 V in the forward bias *I-V* curve of 300 K comes from the series resistance  $R_s$  of the MIS diode, which is caused by the SiO<sub>2</sub> thin layer and *p*-Si substrate thicknesses. The starting point of the downward curvature part of the curve at 300 K is 0.50 V, and the starting point of the other forward bias *I-V* curves shifts to high voltages with decreasing temperature. There are the series resistance  $R_s$  and shunt resistance,  $R_{sh}$ , effects on the current characteristics and performance of MIS diode at sufficiently high forward and reverse bias voltages, respectively [1,17,20,45,51–55]. In an ideal device,  $R_s$  value must be as low as possible, whereas  $R_{sh}$  should be as high as possible. Furthermore, the forward bias *I-V* curve exhibits a non-ideal behavior as if there is an excess current when  $R_{sh}$  affects in low forward bias voltage range in contrast to the series resistance which generally influences the forward bias *I-V* curves in large bias range [47, 54–57]. The voltage-dependent  $R_s$  values of the MIS diode can be determined by applying Ohm's law ( $dV/dI$ ) to the current-voltage data of both branches in **Fig. 5**. This plot is given in **Fig. 6**. For example, the resistance values from **Fig. 6** were determined as  $R_s = 6.5 \text{ k}\Omega$  at the forward bias of 2.0 V and  $R_{sh} = 5.4 \text{ M}\Omega$  at the reverse bias of -2.0 V at 300 K.

The curve in **Fig. 7** [1,58] was drawn using the values of the ideality factor and corresponding the native oxide layer thickness given in **Table 1** in Ref. [1]. The linear fit to data in **Fig. 7** given  $\delta = (33.81n - 28.69)x10^{-8} \text{ cm}$  equation. The native oxide layer thickness for the diode fabricated by us was calculated as 5.8 nm using the value of

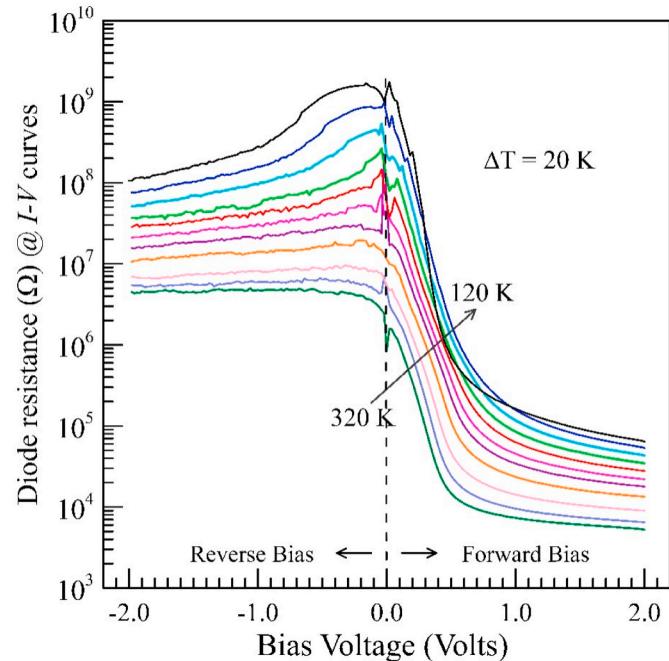


**Fig. 5.** Current versus voltage curve at various temperature.

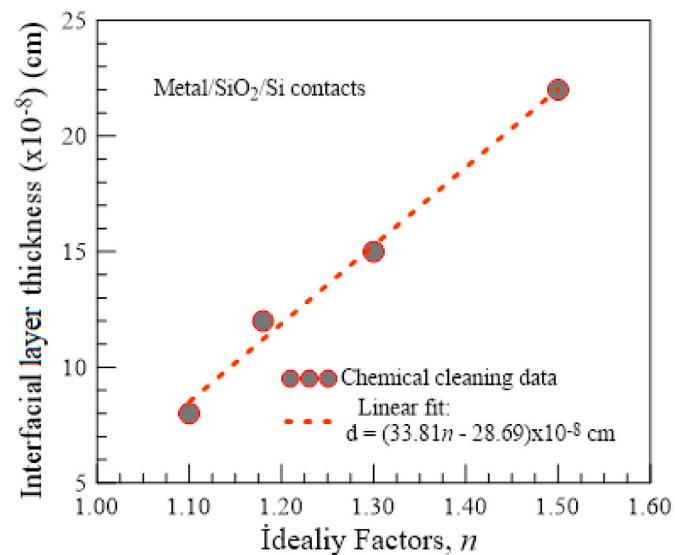
**Table 1**

Temperature dependence value of some diode parameters obtained from the forward branch *I-V* curves of the MIS diode.

T(K)	$\Phi_{b0}$ (eV)	$n$	$I_0$ (A)	$\ln(I_0/T^2)$	$(kT)^{-1}$ (eV) <sup>-1</sup>
320	0.80	2.15	$2.10 \times 10^{-8}$	-29.26	36.23
300	0.76	2.36	$1.06 \times 10^{-8}$	-29.77	38.65
280	0.72	2.74	$7.78 \times 10^{-9}$	-29.94	41.41
260	0.68	2.91	$3.60 \times 10^{-9}$	-30.56	44.59
220	0.59	2.98	$9.63 \times 10^{-10}$	-31.74	52.70
200	0.55	3.07	$3.90 \times 10^{-10}$	-32.39	57.97
160	0.45	3.45	$1.81 \times 10^{-10}$	-33.64	72.46
120	0.37	4.01	$2.62 \times 10^{-12}$	-34.66	96.62



**Fig. 6.** Plot of the resistance versus voltage from the temperature induced *I-V* curves.



**Fig. 7.** Experimental ideality factor versus interfacial layer (SiO<sub>2</sub>) thickness plot [1].

the ideality factor of 2.36 (300 K) in the fit equation above. It can be said that the thickness value of 5.8 nm is in close agreement with the value 8.06 nm from the strong accumulation region, given in the C-G-V characteristics in section above. Fig. 8 represents the BH and ideality factor versus temperature determined from the forward bias I-V curves in Fig. 5. The ideality factor value increased with decreasing temperature in the measurement temperature range.

In Fig. 8, the barrier height exhibits a linear behavior decreasing with decrease in temperature. This behavior is a property of the forward bias I-V characteristics of MIS diodes. This linear straight line in Fig. 8 gives a fit equation such as equation  $\Phi(0, T) = 0.0104 + 0.0021T$  eV to the data of the diode. Considering the temperature dependent behavior of the barrier height, some researchers [1,14,52,59,60] have determined the transmission coefficient of the interfacial native oxide thin film and an effective barrier height presented by that interfacial thin layer in MIS diodes. This evaluation can be realized by [1,14,52].

$$q\Phi(T) = q\Phi(0) + (ak\delta\sqrt{\chi})T \quad (11a)$$

where  $a\delta\sqrt{\chi}$  is the hole tunneling factor,  $a = \frac{4\pi}{\hbar}\sqrt{2m^*}$  is a constant depending on effective mass,  $m^* = 0.16m_0$  [18] is the effective tunneling hole mass,  $\chi$  is the effective potential barrier presented by the interfacial layer or the energy difference between the valance band edges of the p-Si and insulating layer, and  $\delta$  is the insulating layer thickness. The slope of the fit equation  $\Phi(0, T) = 0.0104 + 0.0021T$  eV corresponds to  $ak\delta\sqrt{\chi}$  in eqn. (11a), where Boltzmann constant  $k$  equals  $8.625 \times 10^{-5}$  eV/K,  $\delta \approx 58$  Å and  $a = 0.41$  eV $^{1/2}$ Å $^{-1}$ . Thus, the hole tunneling factor ( $a\delta\sqrt{\chi}$ ) = 24.35 and  $\chi = 1.02$  eV values were obtained for the MIS diode. Card and Rhoderick et al. [1] given a value of about  $\chi = 1.89$  eV for Au/SiO<sub>2</sub>/n-Si diode with film thickness of 28 Å, and a value of about  $\chi = 1.65$  eV for Au/SiO<sub>2</sub>/n-Si diode with film thickness of 15 Å fabricated by another chemical cleaning method. The value of  $\chi = 1.02$  eV that we found from the temperature dependent barrier height or corresponding saturation current values for the MIS diode is in close agreement with those obtained from the room temperature saturation current value for the Si MIS diode by Card and Rhoderick et al. [1]. The value of  $\chi = 1.02$  eV is an important result because it is determined considering the temperature induced forward bias I-V characteristics.

Let us go back to the barrier height values in Fig. 8. The I-V characteristics of real MS contacts generally deviate from the standard TE. Some Scientists [14,25,28,44,50,61–73] have mentioned that the major reasons behind the origin of the lateral inhomogeneity of the barrier heights over the diode area in Schottky contacts can arise as a result of inhomogeneity in the interfacial layer composition, distributions of interfacial charges, non-uniformity of the thickness, and so it is more

accurate to present a distribution for barrier heights. In addition to, the oxide layer and Si substrate interface inhomogeneity can be due to atomically roughness which gives rise to the fermi level to vary locally, and thus to potential barrier inhomogeneity. The surface traps, dislocations, interface states, vacancy defects, gap states can be caused different inhomogeneities [61,62].

Fig. 9 represents the energy band diagram of a MS rectifying contact with the lateral inhomogeneous barrier height. The commonly observed deviation from the standard TE can be explained by means of the modified TE current expression according Gaussian distribution (GD) characterized by a spatial distribution of barrier heights [26,50,61,62,72,73]. The total forward bias and reverse current  $I_M$  in the modified TE relationship can be stated as [61,73,74].

$$I_M = AA^* T^2 \exp \left[ -\frac{q}{kT} \left( \overline{\Phi}_{b0} - \frac{q\sigma_{s0}}{2kT} \right) \right] \left[ \exp \left( \frac{eV - IR_s}{nkT} \right) - 1 \right] \quad (11b)$$

$$I_{Ms0} = AA^* T^2 \exp \left[ -\frac{q}{kT} \left( \overline{\Phi}_{b0} - \frac{q\sigma_{s0}^2}{2kT} \right) \right] \quad (12)$$

$$\Phi_{b0}(0, T) = \overline{\Phi}_{b0} - \frac{q\sigma_{s0}^2}{2kT} \quad (13)$$

where,  $I_{Ms0}$  is the modified saturation current,  $\Phi_{b0}(0, T) = \Phi_{ap}$  is the experimental zero bias apparent BH given in Table 1 and Fig. 8, and it is stated as the apparent BH in terms of the GD,  $\overline{\Phi}_{b0}$  is the mean value of the Gaussian BH distribution and  $\sigma_{s0}$  is its standard deviation. The model with the GD of the apparent barrier heights due to barrier height inhomogeneities or the potential fluctuations explains the current transport across the Schottky potential barrier [14,25,28,44,50,61–73].

Fig. 10 reflects the apparent barrier height versus  $(2kT)^{-1}$  plot. This is called the GD plot of the inhomogeneous barrier heights from the forward bias I-V curves in Fig. 5. This plot has given two GDs regions. One of the them has occurred in the high temperature region and the other in the low temperature region with the values of  $\overline{\Phi}_1 = 1.15$  eV,  $\sigma_1 = 147.65$  mV and  $\overline{\Phi}_2 = 0.74$  eV,  $\sigma_2 = 83.66$  mV, respectively.

Fig. 11 shows the Richardson plots. These graphs should result in a straight line with a slope proportional to the effective BH  $\Phi_b$ . The  $\Phi_b$  value of 0.60 eV was obtained from the fit to the linear  $\ln(I_0 / T^2)$  versus  $(nkT)^{-1}$  plot. The non-linearity of curve may be caused by an abnormal decrease in the BH value with a decrease in temperature, as can be seen from the BH versus temperature curve in Fig. 8. As stated above, the nature and origin of the decrease in the BH with a decrease in temperature can be successfully defined by the GD depend on spatially inhomogeneous BHs using eqn. (12). This equation can be written as

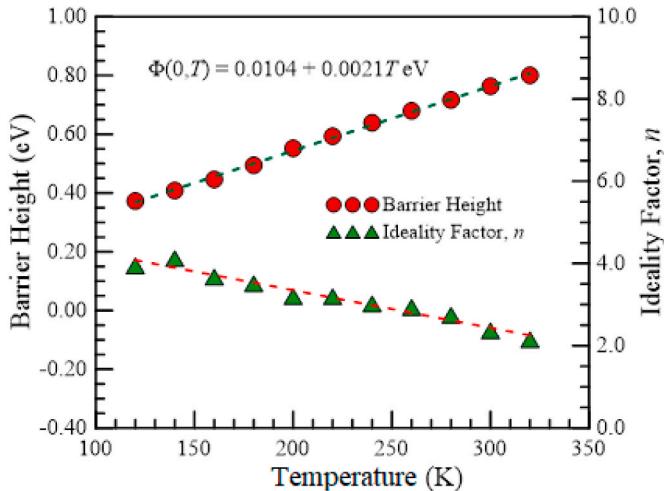


Fig. 8. MIS diode parameters from the forward bias I-V curves in Fig. 4

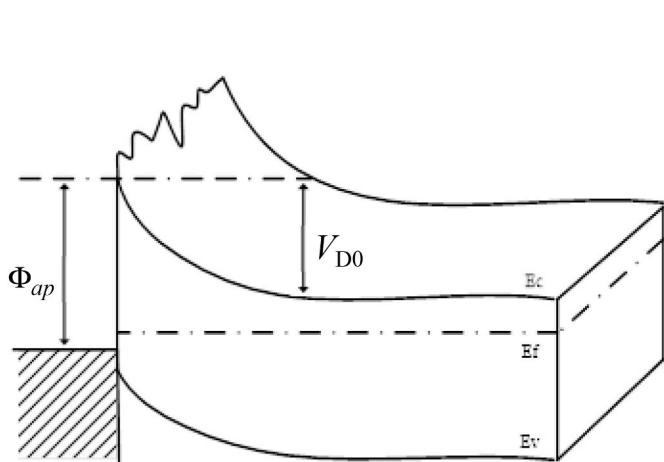


Fig. 9. The energy band diagram of a metal-semiconductor rectifying with lateral inhomogeneous barrier height.

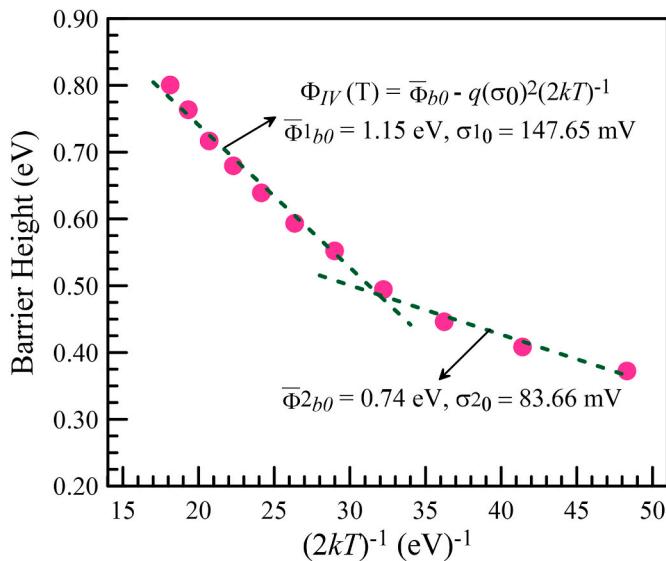


Fig. 10. Forward bias  $I$ - $V$  barrier height versus  $(2kT)^{-1}$  plot.

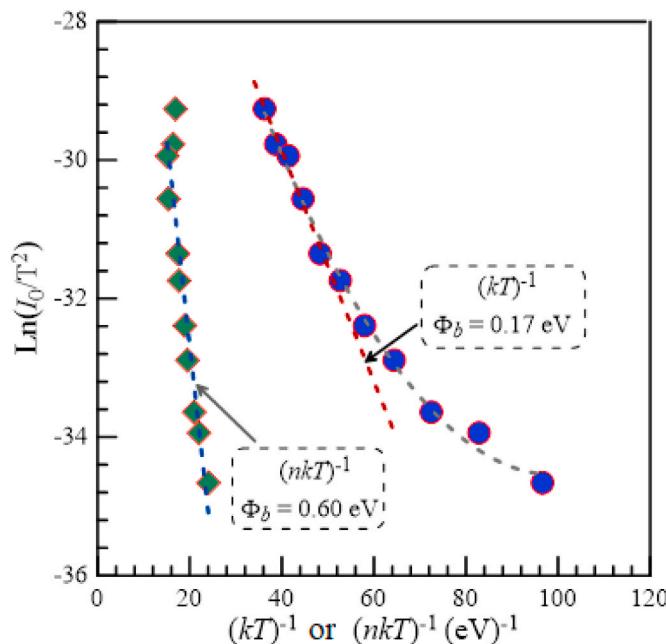


Fig. 11. Richardson Plots plot using the saturation current values.

$$\ell n\left(\frac{I_{M0}}{T^2}\right) - \frac{q^2\sigma_{s0}^2}{2(kT)^2} = \ell n(AA^*) - \frac{q\Phi_{b0}}{kT} \quad (14)$$

Eqn. (14) is the modified Richardson equation according to GD. When comparing eqn. (14) to eqn. (9), it has been seen that eqn. (14) has been modified with the term  $(q^2\sigma_{s0}^2/2(kT)^2)$ . Now, let us see if we can approach the expected values of the diode parameters by modifying the experimental values.

Fig. 12 shows the Richardson plot modified with the term  $q^2\sigma_{s0}^2/2(kT)^2$  according to GD of the inhomogeneous barrier heights. This plot was drawn using  $\sigma_{1s0} = 147.65$  mV and  $\sigma_{2s0} = 83.66$  mV values in eqn. (14), respectively. Thus,  $\bar{\Phi}_{1b0} = 1.16$  eV value was obtained from the curve 1 in high temperature region, and  $\bar{\Phi}_{2b0} = 0.70$  eV value from the curve 2 in low temperature region. These mean BH values for both regions are in close agreement with the values of  $\bar{\Phi}_{1b0} = 1.15$  eV and

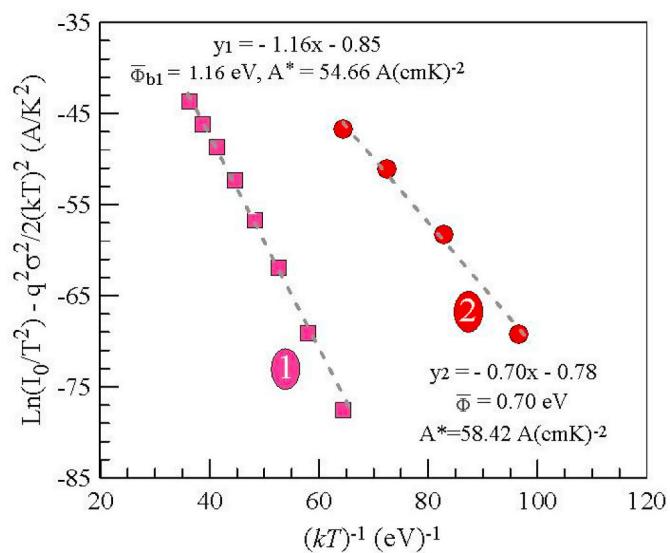


Fig. 12. Modified Richardson plot with the term  $q^2\sigma_{s0}^2/2(kT)^2$  considering GD model of the inhomogeneous barrier heights.

$\bar{\Phi}_{2b0} = 0.74$  eV obtained in Fig. 10. Furthermore, the Richardson constant values of 54.66 and 58.42  $A/K^2\text{cm}^2$  from the curve 1 and curve 2 are approximately 1.70 times higher than the known value of  $32 A/K^2\text{cm}^2$  of holes in p-type Si.

### 3.2.2. Reverse bias current-voltage characteristics

Fig. 13 displays the semilog-reverse branch  $I$ - $V$  characteristics at some temperatures. As seen from the Figure, the current arises with arising voltage at each temperature, indicating non-saturation of the current. The reverse bias current should be saturate after a given voltage. The non-saturation behavior arises due to the presence of the native oxide layer and potential barrier inhomogeneity. The determination of the potential barrier  $\Phi_{b0}(IV)$  from these curves does not give correct and expected results. As seen in Fig. 14, a normalized semi-log graphic of the  $\{I/[1-\exp(-qV/kT)]\}$  versus reverse applied bias allows us to determine the values of  $I_0$  and thus  $\Phi_{b0}(IV)$  from the intercepts

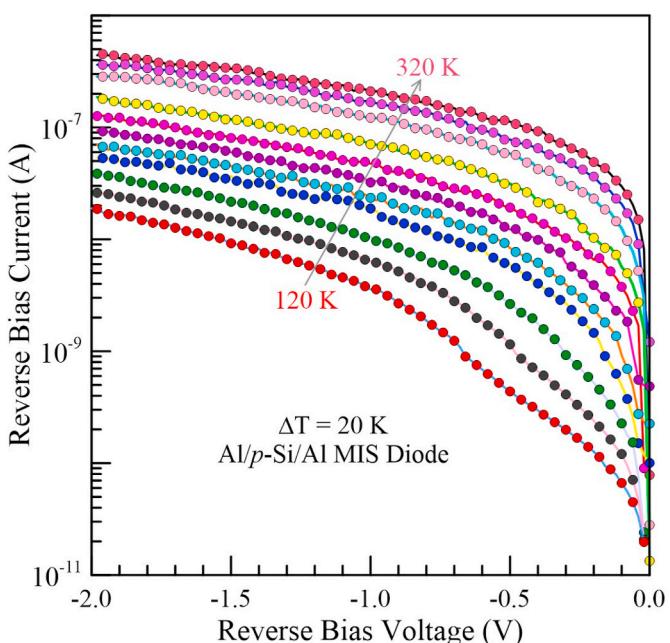
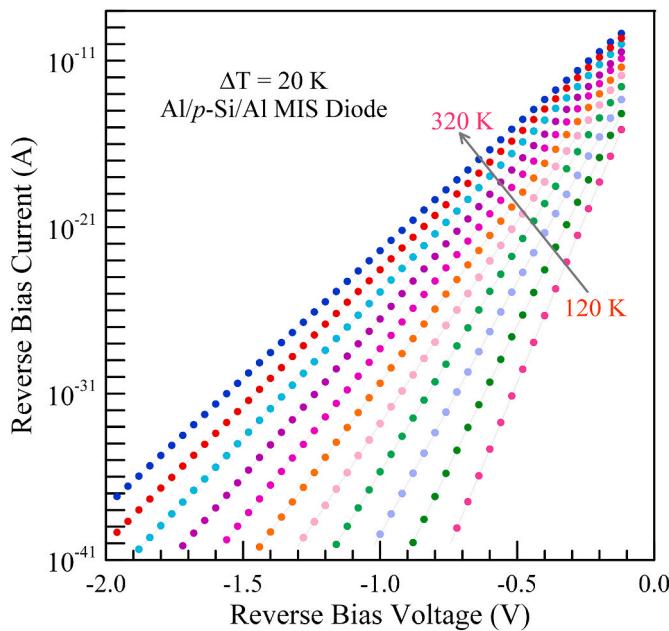


Fig. 13. Semilog-reverse bias  $I$ - $V$  characteristics at some temperatures.



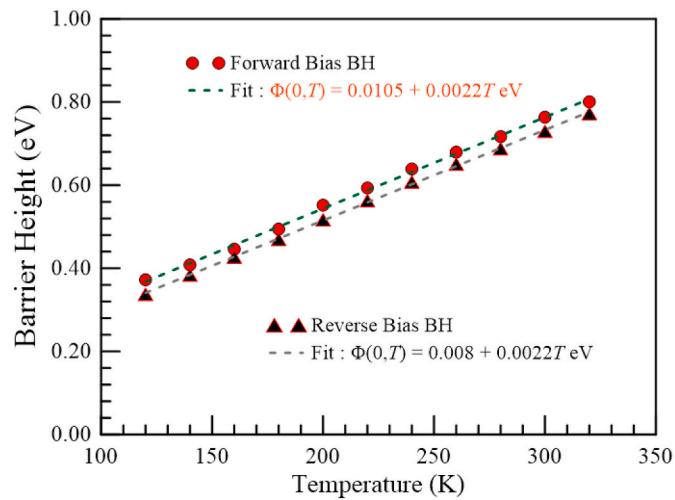
**Fig. 14.** (Color online) Semi-logarithmic  $\{\mathbf{I}/[1-\exp(-qV/kT)]\}$  versus  $V$  plots from the experimental reverse bias  $I$ - $V$  data in Fig. 13.

[75–79]. Thereby, as can be seen from Fig. 15, the  $\phi_{b0}(IV)$  values from the forward and reverse bias  $I$ - $V$  characteristics in Figs. 5 and 14, respectively, run in parallel to each other from 120 K to 320 K. The zero bias forward  $\phi_{b0}(IV)$  is larger than the reverse  $\phi_{b0}(IV)$  each temperature. In addition, the reverse bias BH will gradually decrease while the forward bias BH increases with increase of the bias that decreases (increases) the current transport with the applied voltage. The bias dependence of the BH can be evaluated according to the pinch off effect appearing from interactions of the neighboring patches with low barrier-height. That is, the rise (decrease) in the saddle point potential at forward (reverse) applied bias leads to an increase (decrease) in the effective BH [11,79–83].

Therefore, Ru et al. [83] have suggested that the pinch-off effect at forward bias is stronger than that at reverse bias. Thus, it has been concluded that the effective BH under forward bias should be higher than that under reverse bias when considering Tung's model [11, 79–83]. They have mentioned that this effect technologically seems to do no good for Schottky rectifying diode because a Schottky diode ideally requires a low-barrier diode for forward branch and a high-barrier diode for reverse branch. According to Tung's pinch-off model [79], a Schottky diode with inhomogeneous barrier may behave as a high-barrier rectifier at forward branch and a low-barrier rectifier at reverse branch. Nevertheless, it is important to refer if the low barrier is more to be pinched off under forward or reverse branch.

#### 4. Conclusion

We have systematically analyzed the temperature induced carrier transport in Al/p-Si/Al diodes with the interfacial native oxide layer. A hole tunneling factor of  $(a\delta\sqrt{\chi}) = 24.35$  was determined from the temperature-induced BH graph of the MIS device fabricated by us and thus a value of  $\chi = 1.02$  eV for the effective potential barrier presented by the interfacial layer or the energy difference between the valence band edges of the *p*-Si and oxide layer. The  $\chi$  value is an important result because it has been determined considering the temperature induced forward bias  $I$ - $V$  characteristics rather than the results from only room temperature  $I$ - $V$  curve for SiO<sub>2</sub>/p-Si diodes in the literature. The GD plot of inhomogeneous BHs has given drawn using  $\sigma 1_{s0} = 147.65$  mV for high temperature range and  $\sigma 2_{s0} = 83.66$  mV for low temperature



**Fig. 15.** (Color online)  $\phi_{b0}(IV)$  values from the forward and reverse bias  $I$ - $V$  characteristics in Figs. 5 and 14, respectively.

range. Thus,  $\overline{\Phi}1_{b0} = 1.16$  eV value was obtained from the curve 1 in high temperature region, and  $\overline{\Phi}2_{b0} = 0.70$  eV value from the curve 2 in low temperature region. These mean BH values for both regions are in close agreement with the values of  $\overline{\Phi}1_{b0} = 1.15$  eV and  $\overline{\Phi}2_{b0} = 0.74$  eV from the modified Richardson plot. Furthermore, the Richardson constant values of 54.66 and 58.42 A/K<sup>2</sup>cm<sup>2</sup> from the curve 1 and curve 2 are approximately 1.70 times higher than the known value of 32 A/K<sup>2</sup>cm<sup>2</sup> of holes in *p*-type Si.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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