Characterization of a-Si:H/c-Si interface by admittance spectroscopy

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The capabilities of admittance spectroscopy for the investigation of a-Si:H/c-Si heterojunctions are presented. The simulation and experimental results, which compare very well, show that the admittance technique is sensitive to parameters of both the a-Si:H layer and the a-Si:H/c-Si interface quality. In particular, the capacitance versus temperature curves have two steps, accompanied by two bumps in the temperature dependence of the conductance. The first step occurring in the low temperature range (100−200 K) is related to the transport and response of gap states in the a-Si:H layer. The second step occurring at higher temperature (> 200 K) is caused by a carrier exchange with interface states and appears when the interface defect density exceeds 5×10^{12} cm^{-2}. Then, the interface defects affect the band bending, and thus the activation energy of de-trapping, which favours the exchange with electrons from the a-Si:H and holes from the c-Si, respectively, for increasing defect density.

1. Introduction

(Hydrogenated amorphous silicon)–(crystalline silicon) heterojunctions, a-Si:H/c-Si, are of great interest for practical applications and theoretical studies. One of the attractive practical usage of such heterostructures is high efficiency solar cells (up to 21%) fabricated at completely low temperature process thus reducing the cost [1]. The theoretical interest is caused by the fact that a-Si:H/c-Si heterojunctions may be used as a modelling structure for amorphous/crystalline semiconductor heterojunctions, because c-Si is a well known material and properties of a-Si:H have also been enough studied to be used as an amorphous modelling material. But in both cases the properties of the a-Si:H/c-Si interface are the critical point for the photovoltaic application as well as for modelling. For photovoltaic applications the recombination at interface states may significantly decrease the solar cells efficiency, and uncertainty at the interface brings a lot of difficulties in the modelling. Thus, efficient methods of interface characterisation are needed to study interface properties and to optimise the fabrication process.

It is known that the frequency and temperature dependence of the junction admittance is very sensitive to exchanges with trap levels and its variations with applied dc bias are strongly dependent on interface properties [2,3]. Recently, admittance spectroscopy has been successfully applied to study the interface properties of a-Si:H/c-Si heterostructures [4–6]. It was shown that, generally, in the experimental temperature dependence of the capacitance (C-T) two steps may be observed that are shifted to higher temperature with increasing the measure frequency. The first step occurring in the low temperature range (100−200 K) was attributed to the activation of the transport in the a-Si:H layer, and the second step occurring at higher temperature (> 200 K) was explained by the response of the interface states. However, in order to assess the admittance spectroscopy as a method of characterisation of silicon heterostructures, it is important to get more insight into these two capacitance steps by studying the influence of different heterojunction parameters. We have persent both the results of simulations of admittance spectra and the results of experimental measurements for different a-Si:H/c-Si heterojunctions. Comparison of the modelling results with experimental data allows us to determine and verify the effect of the a-Si:H and c-Si parameters as well as of the defect density at the a-Si:H/c-Si interface on admittance properties.

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2. Simulation details and experiment

The modelling of the heterostructure admittance and its dependence on temperature, frequency and bias was made using a numerical PC program, AFORS-HET, developed at Hahn-Meitner-Institut in Berlin (HMI) [7]. We considered a single heterojunction between n-type a-Si:H and p-type c-Si, with two front and back ohmin contacts. The band diagram of the simulated structures is presented in Fig. 1. The material parameters used in calculations for the c-Si and a-Si:H layers and given in the Table. The value of the conduction band offset equal to 0.15 eV and the distribution of the density of states (DOS) in a-Si:H were taken according to UV-excited photoemission experiments [8]. In particular, the DOS in a-Si:H was taken as consisting of two exponential band tails with characteristic energies, kT_c and kT_v, of 0.106 and 0.068 eV for the valence and conduction band respectively, and with a pre-exponential factor of 2×10^{21} cm^{-3}eV^{-1}, and two Gaussian deep defect distributions of donor and acceptor nature being, respectively, at 0.46 and 0.66 eV above the

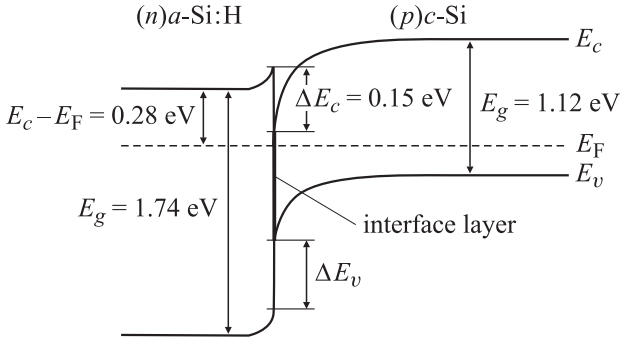

Figure 1. Band diagram used in simulation.

valence band maximum, with a pre-exponential factor of 1.8×10^{20} cm^{-3}eV^{-1}. The interface was described by introducing between c-Si and a-Si:H an additional interface layer with a thickness of 1 nm. The defect distribution in this interface layer was assumed to be constant within the bandgap, assuming donor(acceptor)-like defects in the lower(upper) part of the bandgap. In the following N_{ss} (in cm^{-2}) will denote the interface defect density, which is determined as the product $d_{\text{int}} N_{\text{it}}$ where d_{int} is the thickness of the interface layer (1 nm) and N_{it} (in cm^{-3}) is the defect density in this layer, which is the integral over the band gap of the DOS, g_{it} (in cm^{-3}eV^{-1}).

Main parameters of heterojunction layers used in calculations

Parameter	c-Si	Interface layer	a-Si:H
Band gap, eV	1.12	1.12	1.74
Doping density, cm^{-3}	$10^{15}-2\times10^{18}$	$10^{15}-2\times10^{18}$	10^{20}
Electron affinity, eV	4.05	4.05	3.9
Thickness, nm	300 000	1	10–80

Two series of numerical calculations of the admittance as a function of temperature and frequency were performed.

1. To study the admittance features in the low temperature range (100–200 K) we varied the a-Si:H layer thickness $d_{a\text{-Si:H}}$, characteristic energy of the exponential conduction band tail in a-Si:H, kT_c, and c-Si doping density, N_a, while N_{ss} was set at 10^{11} cm^{-2}.

2. To investigate the admittance behaviour in the „high" temperature range (200–350 K) we varied the interface defect density, N_{ss}, the capture cross section of electrons and holes of the interface states, σ_n and σ_p, respectively, while the parameters of the c-Si and a-Si:H layers were kept constant.

The results of simulations are supplied by experimental measurements obtained on various a-Si:H/c-Si heterostructures. Samples with various a-Si:H layer thickness and c-Si doping density were provided by Hahn-Meitner-Institut, Berlin, while another series of samples with various c-Si surface treatments was provided in the framework of the French national project SiNERGIES. The admittance measurements as a function of temperature and frequency (C-T-ω and G-T-ω) were performed in a liquid nitrogen cryostat in the temperature range 93–333 K using a HP4284A impedance meter at frequencies in the range 20–1 MHz at a reverse bias of 0.1 V.

3. Results

3.1. Low temperature region

The simulated C-T-ω and G/ω-T-ω curves for the heterojunctions with a-Si:H layer thickness of 10, 40 and 80 nm and c-Si doping density of 10^{16} cm^{-3} are shown in Fig. 2, *a*. The experimental curves for two structures with a-Si:H

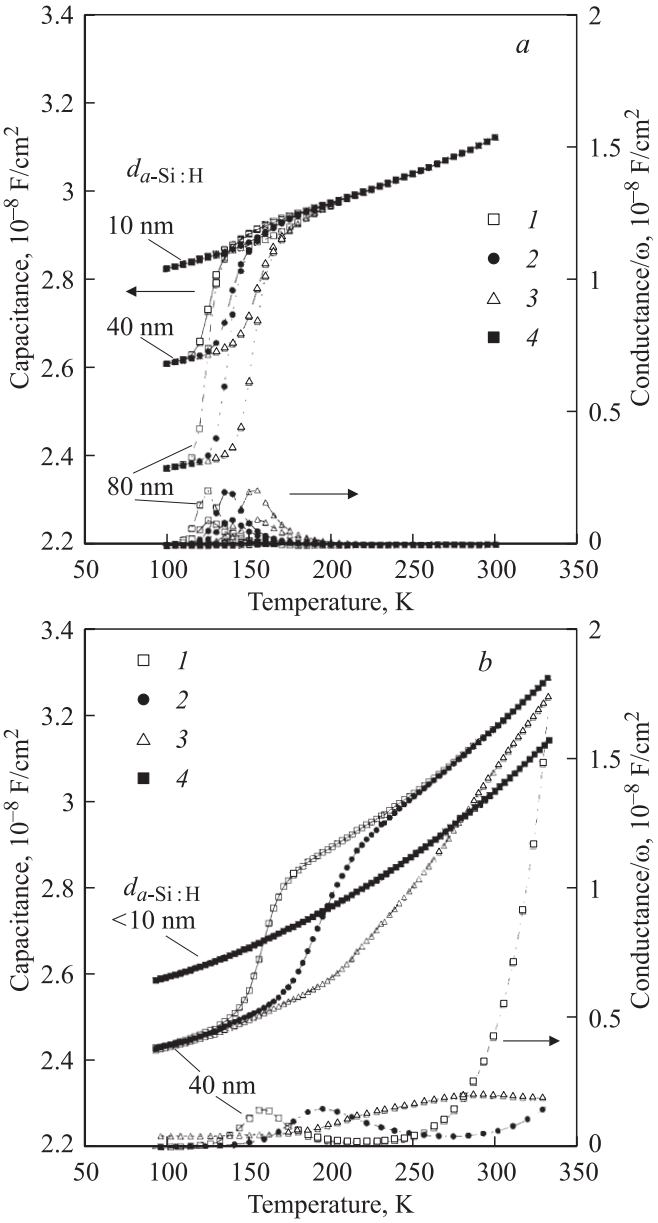

Figure 2. Calculated (*a*) and experimental (*b*) C-T and G/ω-T curves for different thickness of a-Si:H layer, $d_{a\text{-Si:H}}$, measured at frequencies of 100 Hz (*1*), 1 kHz (*2*), 10 kHz (*3*) and at a reverse bias of 0.1 V; *4* — c-Si.

thickness $d_{a\text{-Si:H}} < 10$ nm and $d_{a\text{-Si:H}} = 40$ nm and with the same c-Si doping density are presented in Fig. 2, *b*. One can observed the similar tendencies and similar absolute values of simulated and measured results. A small monotonic increase of the capacitance with temperature is due to the statistical shift of the Fermi level in both c-Si and a-Si:H, reducing the built-in potential and thus the width of the space charge region with increasing temperature. The characteristic features of the curves is the presence of a step in the capacitance in a temperature range of 100–200 K. This step is accompanied by a maximum in the conductance, and both the capacitance step and the conductance maximum are shifted to higher temperatures with increasing frequencies [5]. This shift in the temperature versus frequency may be used to obtain the activation energy of the underlying process. For the simulated curves the activation energy is equal to 0.28 eV and for the experimental curves this parameter is approximately equal

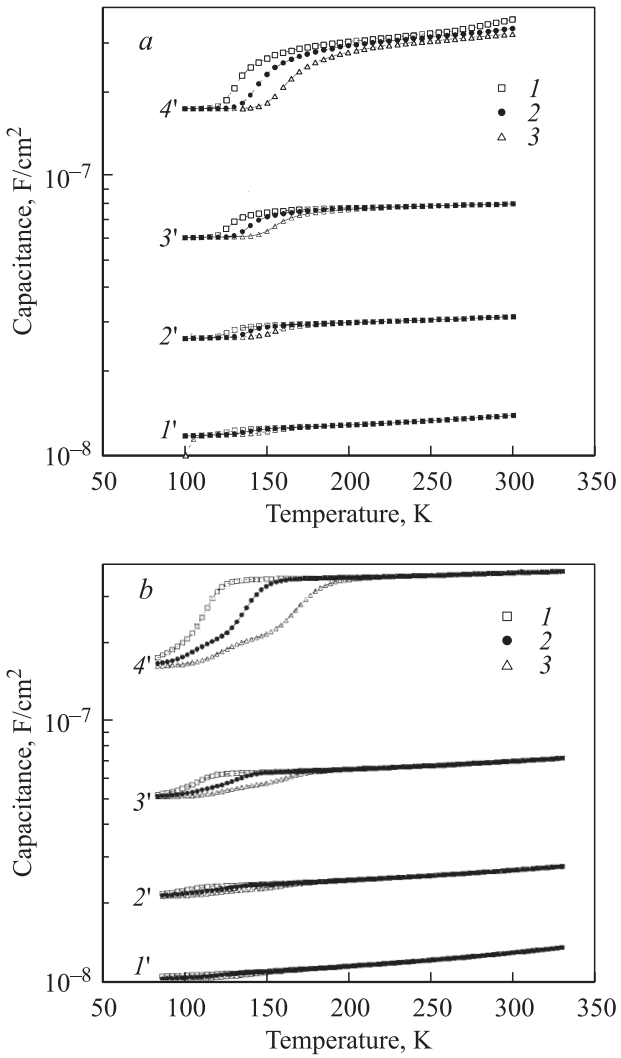

Figure 3. Calculated (*a*) and experimental (*b*) C-T curves for different values of c-Si doping density, N_a, measured at frequencies of 100 Hz (*1*), 1 kHz (*2*) and 10 kHz (*3*) and at a reverse bias of 0.1 V. N_a, cm^{-3}: *1′* — 1.8×10^{15}, *2′* — 10^{16}, *3′* — 7×10^{16}, *4′* — 2×10^{18}.

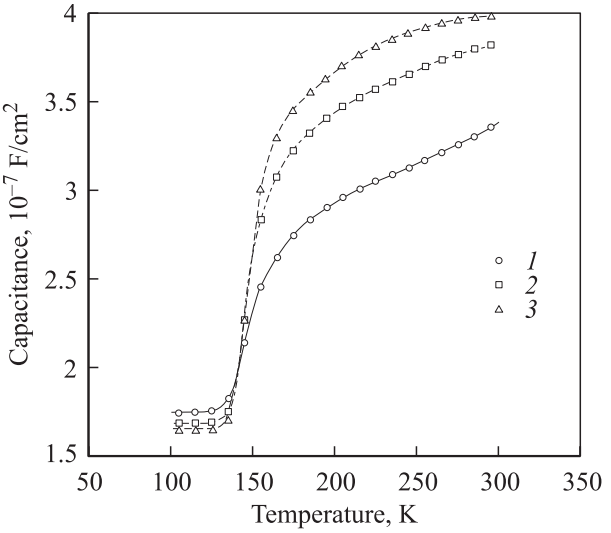

Figure 4. Calculated C-T curves for different values of characteristic energy of conduction band tail in a-Si:H, kT_c, at a frequency of 1 kHz and at a reverse bias of 0.1 V. kT_c, eV; *1* — 0.68, *2* — 0.1, *3* — 0.15.

to 0.2 eV. The amplitude of the capacitance step increases with increasing the a-Si:H layer thickness.

To study the influence of the c-Si substrate doping density, N_a, on the capacitance properties in this temperature region we simulated and measured C-T-ω curves for different values of N_a: 1.8×10^{15}, 10^{16}, 7×10^{16} and 2×10^{18} cm^{-3}, which are presented in Fig. 3. Again, there is a very good correlation between calculated and measured curves. The amplitude of the capacitance step increases with increasing doping density.

Finally, the effect of the DOS in a-Si:H was studied by simulation by varying kT_c while keeping the same position of Fermi level in a-Si:H at 0.28 eV below the conduction band minimum. This simulation was made for $N_a = 2 \times 10^{18}$ cm^{-3} because the effect at this doping density is more pronounced. Three calculated curves for kT_c equal to 0.068, 0.1 and 0.15 eV are shown in Fig. 4. The amplitude of the step is changed in different ways: the top limit of the step significantly rises with increasing kT_c while the bottom limit slightly decreases.

3.2. High temperature region

In the second series of the simulations the interface parameters were varied. The influence of interface defect density, N_{ss}, on the behaviour of the C-T-ω curves is shown in Fig. 5, *a*, where N_{ss} changed from 10^{10} to 10^{14} cm^{-2} for N_a equal to 10^{15} cm^{-3}. For N_{ss} varying from 0 to 10^{10} cm^{-2} no difference in the C-T-ω and G-T-ω curves was observed. When N_{ss} increases to 10^{12} cm^{-2} a slight rise of the capacitance value was observed without any visible deviation of the dependence on temperature and frequency. While N_{ss} reaches 5×10^{12} cm^{-2} the capacitance value significantly increases and a character

of the curves is changed. The second capacitance step appears at higher temperature (200–250 K), accompanied by a second conductance peak, which is not presented in the figure for clarity reason. An activation energy of 0.43 eV can be deduced from this step. For N_{ss} equal to 5×10^{13} cm^{-2} the capacitance level further increases and the second step is shifted to higher temperature (250–300 K) with significantly larger amplitude and activation energy of 0.48 eV. Finally, for N_{ss} equal to 10^{14} cm^{-2} the capacitance absolute value further increases and the amplitude of the second step drastically rises with a slight decrease of activation energy to 0.47 eV. The positon of this step is shifted to higher temperature with decreasing capture cross section of interface states, $\sigma = \sigma_n = \sigma_p$, as shown in Fig. 6 where C-T curves calculated for three different values of σ are presented, N_{ss} is set at 5×10^{13} cm^{-2}. It should be noted that, from a practical point of view the appearance of the second capacitance step is a well defined feature for a rough estimation of the interface quality.

In Fig. 5, *b* we present experimental C-T-ω curves for two structures with different interface treatment. Sample 1, which has an efficiency of 9–10% exhibits a step at high temperature, while the second sample with an efficiency of 12–14% does not have any step in this temperature region. It means that the low efficiency of sample 1 is caused by the poor interface quality, and an estimation of N_{ss} gives a value in the order of 5×10^{13} cm^{-2}. On the contrary, N_{ss} for the sample 2 is less than 10^{12} cm^{-2}.

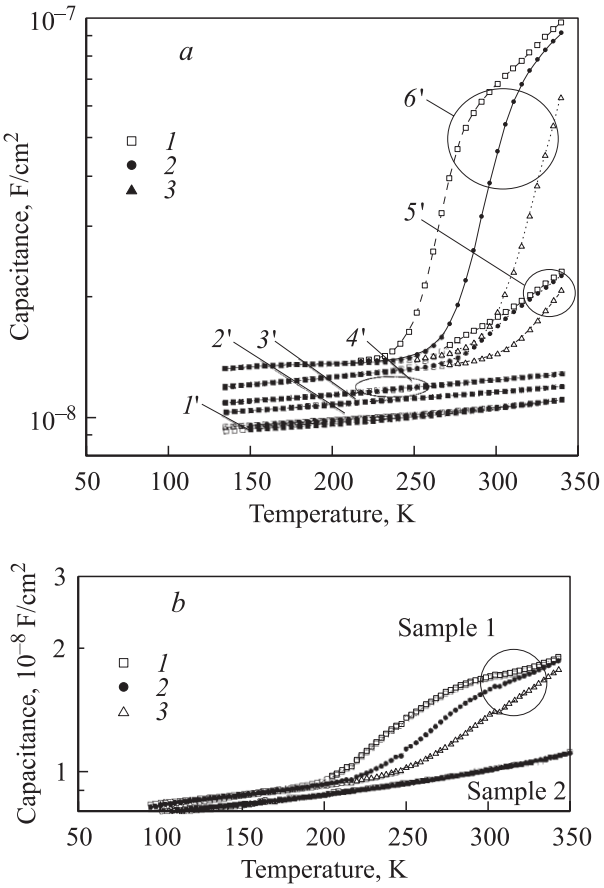

Figure 5. C-T curves: *a* — calculated for values of interface defect density N_{ss} cm^{-2}: *1′* — 10^{10}–10^{11}, *2′* — 10^{12}, *3′* — 5×10^{12}, *4′* — 10^{13}, *5′* — 5×10^{13}, *6′* — 10^{14}, *b* — measured for 2 samples with different interface treatment at frequencies of 100 Hz (*1*), 1 kHz (*2*) and 10 kHz (*3*) and at a reverse bias 0.1 V.

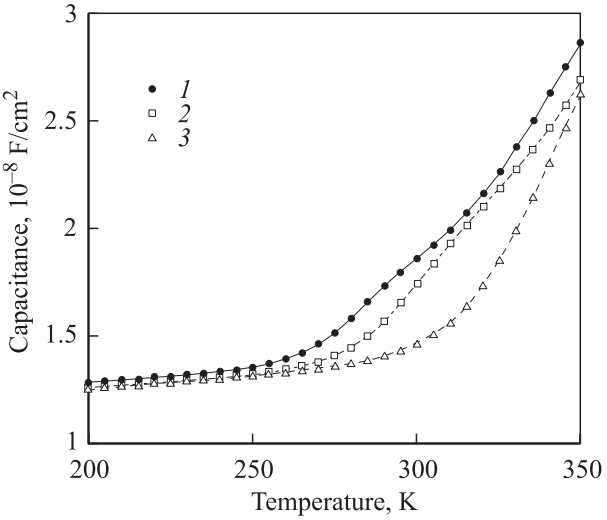

Figure 6. Calculated C-T curves for different values of capture cross section, σ, measured at frequency of 1 kHz and at a reverse bias of 0.1 V. σ, cm^{-2}: *1* — 10^{-13}, *2* — 10^{-14}, *3* — 10^{-15}.

Analysis of the sensitivity of the C-T-ω curves to N_{ss} shows that the limit of sensitivity i.e. the minimum value of N_{ss} for the second capacitance step to appear does not depend significantly on the doping density of *c*-Si.

4. Discussion

The presence of the step in the C-T curves at low temperature is attributed to the onset of the transport or of the response of gap states at the Fermi level in the *a*-Si:H emitter [5]. At very low temperatures, below the step, the capacitance is given by $\varepsilon A/(d_{a\text{-Si:H}} + W_{c\text{-Si}})$, where ε is the dielectric permittivity, A is the diode area, $d_{a\text{-Si:H}}$ is the *a*-Si:H thickness and $W_{c\text{-Si}}$ is the width of the depletion layer in *c*-Si. Above onset, the capacitance changes to $\varepsilon A/(l_{\text{eff}} + W_{c\text{-Si}})$, determined by the sum of the depletion region, $W_{c\text{-Si}}$, in *c*-Si and the effective depletion length, l_{eff}, in *a*-Si:H. This effective depletion length is a kind of Debye length related to the density of gap states responsible for the change in capacitance. From the step in capacitance, we can thus determine the difference between the whole *a*-Si:H layer thickness and the effective depletion length, $d_{a\text{-Si:H}} - l_{\text{eff}}$. So, for the structure with *a*-Si:H thickness of 40 nm presented in Fig. 2, *b*, we obtain $d_{a\text{-Si:H}} - l_{\text{eff}} = 36$ nm. This value approximately corresponds to the total thickness of the *a*-Si:H layer. The activation energy of this process corresponds to the difference between conduction band and Fermi level in *a*-Si:H ($E_c^{a\text{-Si:H}} - E_{\text{F}}^{a\text{-Si:H}}$).

Increasing the doping density of c-Si, N_a, leads to decrease of $W_{c\text{-Si}}$ and therefore the capacitance becomes more sensitive to the variation of effective thickness from $d_{a\text{-Si:H}} + W_{c\text{-Si}}$ to $l_{\text{eff}} + W_{c\text{-Si}}$, and also the absolute value of the capacitance increases. For high values of $N_a \approx 10^{18}\,\text{cm}^{-3}$, which are comparable with the a-Si:H effective doping density, the depletion length l_{eff} in a-Si:H is no longer negligible compared to with $W_{c\text{-Si}}$. It means that the capacitance is more sensitive to the DOS in a-Si:H. It is illustrated by simulations in Fig. 3 where the increase of conduction tail characteristic energy, which corresponds to increase of the DOS, leads to a decrease of l_{eff} that increases the capacitance value above the step. In contrary, the decrease of capacitance below the step with increasing kT_c is caused by increase of $W_{c\text{-Si}}$ due to the more propounced band bending in c-Si when the DOS in a-Si:H is increased.

The second step at high temperature is caused by trapping and emission of charge carriers at interface states. Before analysis of the simulation results we should remind that the calculation was made assuming a constant distribution of interface defect density and with capture cross sections for those interface states equal for electron and holes ($\sigma = \sigma_n = \sigma_p$).

Firstly, increasing N_{ss} up to $10^{12}\,\text{cm}^{-2}$ leads to slightly decrease the band bending in c-Si and therefore the depletion region width $W_{c\text{-Si}}$. Thus, in C-T-ω curves one can observe a slight increase of the capacitance level with no step since the contribution of interface states to the capacitance is negligible. When N_{ss} is in the range of $5 \times 10^{12} - 10^{13}\,\text{cm}^{-2}$ the step at higher temperature occurs due to the exchange of electrons between interface states near the Fermi level and the conduction band of a-Si:H. The activation energy of this process corresponds to the difference between the conduction band in a-Si:H and the quasi Fermi level for electrons E_{Fn} at the interface $(E_c^{a\text{-Si:H}} - E_{Fn})_{\text{it}}$. The value of activation energy increases with increasing N_{ss} because of the rise of band bending in a-Si:H and the step is shifted towards higher temperature. Further increasing N_{ss} ($N_{ss} \geq 5 \times 10^{13}\,\text{cm}^{-2}$) leads to a case where $(E_c^{a\text{-Si:H}} - E_{Fn})_{\text{it}}$ is greater than the difference between the quasi Fermi level for the holes E_{Fp} and the valence band in c-Si at the interface $(E_{Fp} - E_v^{c\text{-Si}})_{\text{it}}$. In this case the exchange of holes between interface states and the valence band in c-Si prevails. The amplitude of the step becomes larger, and the activation energy corresponds to $(E_{Fp} - E_v^{c\text{-Si}})_{\text{it}}$. Increasing N_{ss} to $10^{14}\,\text{cm}^{-2}$ leads to a slight decrease of the activation energy and therefore to a shift of the step to lower temperature.

5. Conclusion

The low temperature step in C-T curves (and the corresponding bump in G-T curves) is related to the transport and response of gap states in the a-Si:H layer. From the activation energy of this step one can determine the position of the Fermi level in a-Si:H, and from the absolute values of the capacitance below and above the step the difference $d_{a\text{-Si:H}} - l_{\text{eff}}$ can be obtained. If one knows the thickness of the a-Si:H layer $d_{a\text{-Si:H}}$, the effective depletion length l_{eff} in a-Si:H can be found, which is related to the band bending in a-Si:H.

The high temperature step in C-T curves is caused by a carrier exchange with interface states and appears when N_{ss} exceeds $5 \times 10^{12}\,\text{cm}^{-2}$. It can be used for a rapid estimation of the interface quality. We have shown that, when N_{ss} is increased above $5 \times 10^{12}\,\text{cm}^{-2}$, first the exchange of electrons with a-Si:H takes place, which leads to only a limited step in the capacitance as a function of temperature. Then, for higher values of N_{ss}, the exchange of holes with the c-Si prevails and the step in C-T curves is much more pronounced.

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