Materials Science in Semiconductor Processing 39 (2015) 390–399

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Current–voltage and capacitance–voltage characteristics of Al Schottky contacts to strained Si-on-insulator in the wide temperature range

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ARTICLE INFO

Available online 6 June 2015

Keywords:
SSOI
Schottky contact
Barrier height
Ideality factor
Double Gaussian distribution
Barrier inhomogeneities

ABSTRACT

The electrical characteristics of Al/strained Si-on-insulator (sSOI) Schottky diode have been investigated using current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements in the wide temperature range of 200–400 K in steps of 25 K. It was found that the barrier height (0.57–0.80 eV) calculated from the *I–V* characteristics increased and the ideality factor (1.97–1.28) decreased with increasing temperature. The barrier heights determined from the *C–V* measurements were higher than those extracted from the *I–V* measurements, associated with the formation of an inhomogeneous Schottky barrier at the interface. The series resistance estimated from the forward *I–V* characteristics using Cheung and Norde methods decreased with increasing temperature, implying its strong temperature dependence. The observed variation in barrier height and ideality factor could be attributed to the inhomogeneities in Schottky barrier, explained by assuming Gaussian distribution of barrier heights. The temperature-dependent *I–V* characteristics showed a double Gaussian distribution with mean barrier heights of 0.83 and 1.19 eV and standard deviations of 0.10 and 0.16 eV at 200–275 and 300–400 K, respectively. From the modified Richardson plot, the modified Richardson constant were calculated to be 21.8 and 29.4 A cm^{-2} K^{-2} at 200–275 and 300–400 K, respectively, which were comparable to the theoretical value for p-type sSOI (31.6 A cm^{-2} K^{-2}).

1. Introduction

The downscaling of the complementary metal oxide semiconductor (CMOS) devices over the past few decades has been the foundation for revolution in the information technology [1,2]. One of the main driving forces of the technological advances has been the scaling of gate oxides. With the gate length of the transistor entering the nanometer-scale regime and the gate oxide becoming thinner, it will be very challenging to sustain these past trends. Once the scaling of CMOS devices slows down due to physical limits, new materials systems such as high-k gate dielectrics or the high mobility channel materials are required to continue the shrinkage of device dimension [3,4]. Strained Si has been considered as alternative channel material for further improvement of device performance beyond device scaling owing to strain induced carrier mobility enhancement over bulk-Si. Similarly, strained Si-on-insulator (sSOI) has received a considerable attention due to the combined advantages of enhancement in carrier mobility from strained Si layer and the benefits of silicon-on-insulator (SOI) such as reduced

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http://dx.doi.org/10.1016/j.mssp.2015.05.043
1369-8001/

parasitic capacitance, low leakage current, and suppressed short channel effects [5–7]. Such a prominent feature of sSOI stimulates demand for employing sSOI on CMOS devices. For instance, Fenouillet-Beranger et al. [8] reported that the use of sSOI substrate led to a gain in performance of 20% on the n-channel devices with a gate length of 30 nm, as compared to the standard SOI one.

The Schottky barrier diodes have been widely employed in the electronics industry finding many uses as a rectifier. Their unique properties include low turn on voltage, fast recovery time, and low junction capacitance, which enables them to be used in a number of applications where other diodes would not be able to provide the same level of performance [9,10]. Despite a wide range of industrial applications of Schottky barrier diodes, the attempt for the implementation of sSOI into Schottky barrier diodes is rather scarce, though sSOI-based Schottky devices are expected to show further enhanced device performance in many areas. Due to the technological importance of Schottky barrier diodes in the electronics industry, their electrical characteristics have been extensively studied both experimentally and theoretically in order to improve their performance and reliability [11–14]. Most of these studies were limited to the determination of the Schottky barrier height at room temperature by measuring either the current–voltage (I–V) characteristics or the capacitance–voltage (C–V) characteristics of these diodes. However, such an analysis performed at room temperature is insufficient to give detailed information about carrier transport through Schottky barrier. Infact, it neglects many possible effects that cause non-ideality in the I–V characteristics of the Schottky diode with the reduction of the barrier height. The temperature dependence of the I–V and C–V characteristics gives a better insight of details for the nature of Schottky barrier formed in the interface between metal and semiconductor. In this work, Al Schottky structures were fabricated on p-type sSOI and their electrical characteristics were investigated using I–V and C–V characteristics in the temperature range of 200–400 K. It will be shown that the barrier inhomogeneity prevailing in Al/sSOI Schottky contact could be responsible for the strong temperature dependence of barrier height and ideality factor. It will be further shown that there exists the double Gaussian distribution of barrier heights in Al/sSOI Schottky contact.

2. Experimental details

In this work, sSOI wafers were fabricated by bonding a strained Si layer directly to the buried oxide (BOX) using SMARTCUT technology [15]. A strained p-type Si layer with a resistivity of 10 Ω cm epitaxially grown on a relaxed $Si_{0.8}Ge_{0.2}$ film was transferred to an oxidized p-type (100) Si wafer using a hydrogen-induced layer transfer method, followed by chemical–mechanical polishing. The thicknesses of the strained Si and BOX layers were 40 and 140 nm, respectively. Initially, the sSOI wafers were cleaned in an ultrasonic bath of acetone and methanol, immersed in a diluted HF solution (H_2O:HF=100:1) to remove the native oxide, and were finally rinsed with deionized (DI) water. The circular Schottky electrodes were formed by the evaporation of Al film (30 nm) using thermal evaporation. The circular Al Schottky contacts were defined with a diameter of 200 μm around which Ohmic contacts were formed by the sputter deposition of Pt film (30 nm) separated by a distance of 100 μm. Temperature dependent I–V and C–V measurements were performed using a precision semiconductor parameter analyzer (Agilent 4156 C) and precision LCR meter (Agilent 4284 A), respectively.

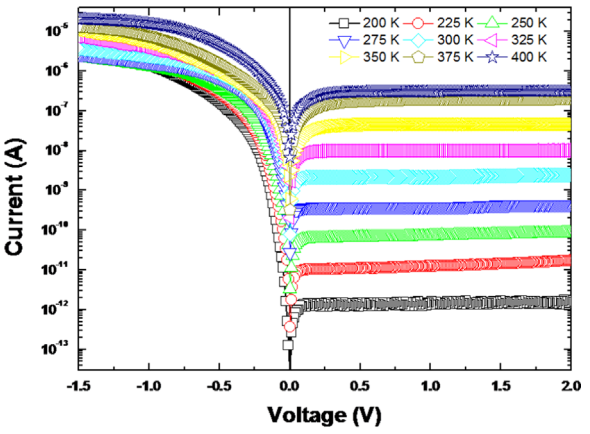

Fig. 1. The semi-log reverse and forward bias current–voltage plots of the Al/sSOI Schottky barrier diode in the temperature range of 200–400 K.

3. Results and discussion

Fig. 1 shows the I–V characteristics of Al/p-type sSOI Schottky diodes measured at temperatures in the range of 200–400 K. It is clear that the current through the diode increased with increasing temperature. Obviously, the diodes showed good rectifying behavior at all temperatures with the current showing an exponential increase in the forward bias and a weaker voltage dependence in the reverse bias. According to thermionic emission (TE) theory, the I–V characteristics of the Schottky diode are given by [16]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{-qV}{kT}\right)\right] \quad (1)$$

where q is the elementary charge, V is the applied voltage, n is the ideality factor, k is the Boltzmann constant and T is the absolute temperature, I_0 is the saturation current derived from the y-axis intercept of the straight line portion of ln (I) versus V at V=0 and is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \quad (2)$$

where Φ_{b0} is the Schottky barrier height, $A^*$is the effective Richardson constant and equals to 31.6 A cm^{-2} K^{-2} [16] and A is the diode area. Once I_0 is determined, the barrier height can be evaluated using

$$\Phi_{b0} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (3)$$

The ideality factor is obtained from the slope of straight line portion of the forward bias ln (I)–V characteristics from

Table 1
The experimentally obtained characteristic parameters of Al/p-sSOI Schottky diodes at different temperatures in the range of 200–400 K.

T (K)	Schottky barrier height (eV)						Ideality factor		Series resistance (kΩ)		
	I–V	Φ_{bf}	$n\Phi_b$	Norde	$H(I)$	C–V	I–V	Cheung	$dV/d(\ln I)$	$H(I)$	Norde
200	0.57	0.96	1.12	0.57	0.45	1.01	1.97	4.41	480	435	406
225	0.58	0.93	1.09	0.60	0.50	1.01	1.88	3.64	437	387	401
250	0.62	0.92	1.07	0.63	0.54	1.00	1.73	3.17	387	327	398
275	0.64	0.91	1.06	0.66	0.57	1.01	1.64	2.66	349	260	287
300	0.67	0.90	1.04	0.69	0.62	1.01	1.55	2.36	303	245	247
325	0.70	0.90	1.04	0.72	0.67	1.00	1.47	2.07	272	236	238
350	0.75	0.92	1.03	0.77	0.72	0.99	1.38	1.87	263	223	231
375	0.77	0.92	1.02	0.78	0.74	0.98	1.32	1.69	219	208	222
400	0.80	0.92	1.02	0.82	0.77	0.97	1.28	1.50	92	84	71

Eq. (1) and can be written as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{4}$$

The values of barrier heights and ideality factor obtained using Eqs. (3) and (4) are represented in Table 1. The experimental values of barrier height and ideality factor for the device varied from 0.57 eV and 1.97 at 200 K to 0.80 eV and 1.28 at 400 K, respectively. The ideality factors were obtained from the ln(I)–V plot in the voltage range of 0.01–0.1 V. The barrier height and ideality factor showed a strong temperature dependency. For instance, as decreasing temperature, the barrier height decreased and the ideality factor increased. This decrease in barrier height and the increase in ideality factor with decrease in temperature are indicative of the deviation from the pure TE theory, in which the barrier height and the ideality factor are independent of temperature. This anomalous temperature dependence of the barrier height and ideality factor could be associated with the existence of spatially inhomogeneous Schottky barrier consisting of low and high barrier patches with individual cross-sectional areas [17]. The barrier inhomogeneities may occur as a result of the poor interface quality, which, in turn, depends on several factors such as the surface and bulk defect density distribution, the inhomogeneities in the interfacial thin layer stoichiometry, compositional changes at the near surface region, non-uniformity of the interfacial charge distribution, and interfacial layer thickness. The existence of laterally extended barrier inhomogeneities at the metal–semiconductor interface allows for carrier transport to be treated by the parallel conduction model [18,19]. According to this model, since the current transport across the metal–semiconductor interface is a temperature activated process, at lower temperatures, the carriers do not have sufficient energy to surmount the high barrier [19]. Thus, the current transport is dominated by current flowing through the patches of lower Schottky barrier height, resulting in higher ideality factor. As increasing the temperature, more carriers gain sufficient energy to cross over the higher Schottky barriers. Therefore, the current transport is dominated by the current that flows over the higher barrier, and hence the barrier height increases and ideality factor decreases at higher temperatures. In addition, the ideality factor greater than unity in the present device could be associated with the particular distribution of interface states, the image force effect, recombination–generation, and minority carrier injection [20].

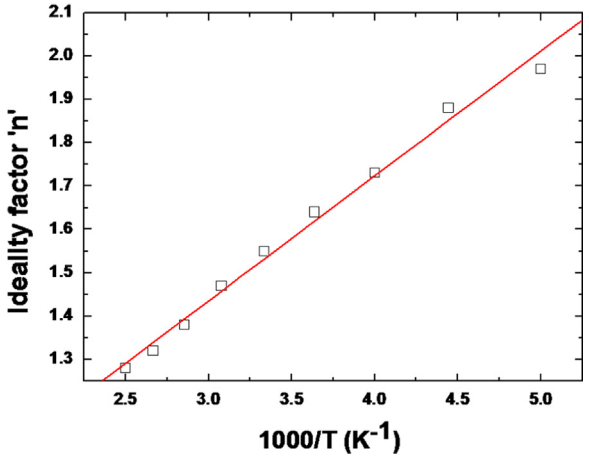

Fig. 2. Temperature dependence of the ideality factor for Al/sSOI Schottky diode in the temperature range of 200–400 K.

Al/p-type sSOI Schottky diodes exhibited an ideality factor deviating from the value of unity, indicating the current transport deviated from thermionic emission mechanism. An increase in ideality factor with decreasing temperature is known as T_0 effect (measure of the temperature dependence of the ideality factor) [21,22]. Such a phenomenon may be due to the interface state density at the metal/semiconductor interface, image force lowering and tunneling of the carrier through the barrier [21,22]. As can be seen in Fig. 2, the change in ideality factor with temperature was found to change linearly with inverse temperature as

$$n(T) = n_0 + \frac{T_0}{T} \tag{5}$$

where n_0 and T_0 are constants, and can be obtained from the linear fitting of the plot of ideality factor versus inverse temperature (Fig. 2) according to Eq. (5). The values of n_0 and T_0 were obtained as 0.5718 and 287.9 K, respectively. For example, by using the n_0 (=0.5718) and T_0 (=289.9) constants, the ideality factor was calculated to be 1.72, 1.53, and 1.39 at T=250, 300 and 350 K, respectively. These

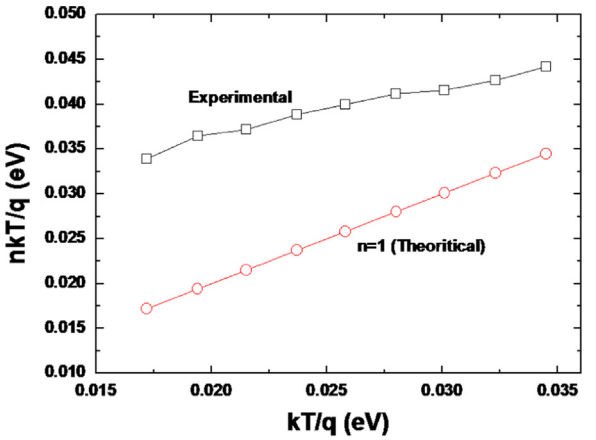

Fig. 3. The plot of nkT/q versus kT/q for Al/sSOI Schottky diode.

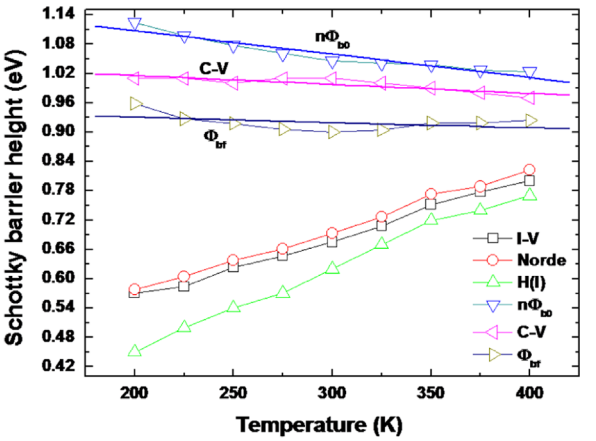

Fig. 4. Comparision of barrier height versus temperature obtained by Cheung's method, Norde method, Φ_{b0},$n\Phi_{b0}$, C–V and Φ_{bf} for Al/sSOI Schottky diode.

values were very close to the obtained experimental values of 1.73 (at 250 K), 1.55 (at 300 K) and 1.38 (at 350 K).

Also, nkT/q versus kT/q plot was drawn to obtain the evidence of T_0 effect, as shown in Fig. 3. As can be seen from Fig. 3, there was a linear behavior with the value of ideality factor being closer to unity at high temperature. Such a behavior could be attributed to the presence of barrier inhomogeneity having mean barrier height along with a small number of low barrier height regions. At low temperatures, the ideality factor is characterized by the current flowing through the distribution of low Schottky barrier height patches, while the ideality factor is defined as carrier transport through Schottky barrier having large uniform region by approaching unity value at high temperatures. In other words, when increasing temperature, lower effective Schottky barrier height of the patches is offset by much greater area of the uniform region.

It should be noted that the ideality factor is included in the expression for the saturation current. This is due to the effect that causes deviation from $n=1$ at higher bias voltage being also present at zero bias voltage [23]. Particularly, in addition to the effect of the interfacial layer that is strongest on ideality factor, the image force and surface charges will be present at zero voltage. The mere reduction of the applied voltage to zero does not result in the elimination of these effects. The expression for the current can now be written as [23]

$$I = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{n(T)kT}\right)\left[\exp\left(\frac{-qV}{kT}\right)-1\right] \tag{6}$$

$n(T)$ is temperature dependent. The corresponding barrier height Φ_{b0} can be calculated from the modified saturation current given by

$$\Phi_{b0} = \frac{n(T)kT}{q}\ln\left[\frac{AA^*T^2}{I_0}\right] \tag{7}$$

After this modification, as can be seen in Table 1 and Fig. 4, the value of Φ_{b0} decreases almost linearly with the temperature as

$$\Phi_{b0} = \Phi_{b0}(0\ K) + \alpha T \tag{8}$$

Here, Φ_{b0} (0 K) and α are the barrier height at zero temperature and the temperature coefficient of the barrier height, respectively. From the fit to the data of plot, the value of Φ_{b0} (0 K) and α were found to be 1.20 eV and -4.78×10^{-4} eV K^{-1} respectively. These values were close to the theoretical values calculated from the forbidden band gap of Si (Φ_{b0} (0 K): 1.17 eV, α: -4.73×10^{-4} eV K^{-1}) [17]. Also, these results were in good agreement with the previous studies [24,25]. Namely, assuming that variation of the barrier height with temperature is entirely due to the variation in the band gap, discrepancy between experimental and theoretical values of Φ_{b0} (0 K) and α was insignificant [26,27].

The series resistance (R_s) is one of the most important parameters that influence the electrical properties of metal–semiconductor contacts. The presence of R_s in the Schottky structure is responsible for the deviation of I–V characteristics from linearity. The downward concave curvature of the forward-bias I–V plot at sufficiently large voltages is caused by the effect of R_s value [28]. In order to determine the value of R_s, we analyzed the forward bias I–V data using the method developed by Cheung [29]. According to TE theory, the forward bias I–V characteristics of the metal–semiconductor contact with R_s can be expressed using Cheung's function as

$$\frac{dV}{d\ln(I)} = \frac{nkT}{q} + IR_S \tag{9}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_S + n\Phi_b \tag{10}$$

Fig. 5(a) shows the plot of $dV/d\ln(I)$ versus I for different temperatures in a wide range from 200 to 400 K. From Eq. (9), a plot of $dV/d\ln(I)$ versus I will be linear and its slope and y-axis intercept give R_s and nkT/q, respectively. As seen from Fig. 5(a), the curves exhibited very good linearity for whole temperature range. When the temperature decreased, the corresponding curve was shifted upward, as would be estimated by Eq. (9). In addition, Fig. 5(b) shows the plot of $H(I)$ versus I for the device at the same temperature with the slope and y-axis intercept giving R_s and barrier height, respectively. The barrier height, ideality factor and series resistance values obtained from Cheung's method at

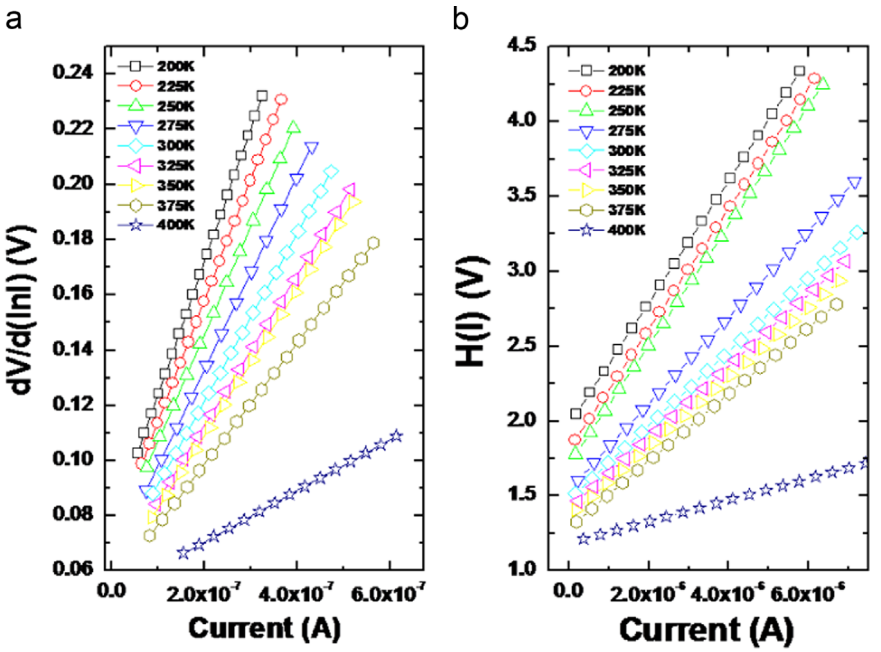

Fig. 5. Pot of Cheung's method (a) $dV/d(\ln I)$ versus I (b) $H(I)$ versus I for Al/sSOI Schottky barrier diode in the temperature range of 200–400 K.

different temperatures were summarized in Table 1, together with the values of the barrier height and ideality factor calculated from the I–V characteristics. As seen from Table 1, the values obtained from different methods were in good agreement with each other. The R_s decreased with increasing temperature. It seems that an increase in R_s with the fall of temperature could be associated with the factors responsible for the increase in ideality factor and/or the lack of free carrier concentration at low temperatures [20].

Norde proposed an alternative method to determine the R_s and barrier height based on TE theory. Norde's function $F(V)$ is defined as [30]

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left[\frac{I(V)}{AA^*T^2}\right] \tag{11}$$

where $I(V)$ is the current obtained from the I–V curve. A plot of $F(V)$ versus V of the diode is shown in Fig. 6. From the $F(V)$–V plot, the barrier height can be determined as follows:

$$\Phi_{b0} = F(V_{min}) - \left(\frac{1}{2} - \frac{1}{n}\right)V_{min} - \frac{(2-n)}{n}\frac{kT}{q} \tag{12}$$

where $F(V_{min})$ is the minimum value of $F(V)$ and V_{min} is the corresponding voltage. The R_s can be expressed as

$$R_s = \frac{kT(2-n)}{qI_{min}} \tag{13}$$

where I_{min} is the forward current corresponding to the V_{min}, where the function $F(V)$ exhibits a minimum. The barrier height and R_s calculated from Eqs. (12) and (13) were found to be 0.57 eV and 435 kΩ at 200 K and 0.82 eV and 84 kΩ at 400 K, respectively. It should be noted, however, that the barrier heights calculated from Norde's method differ from those obtained from the forward I–V characteristics. Generally, Norde's method may not be a suitable method for the rectifying junctions with high ideality factor which are not compatible with pure TE model. Therefore, there was a discrepancy between barrier heights obtained from Norde and I–V methods.

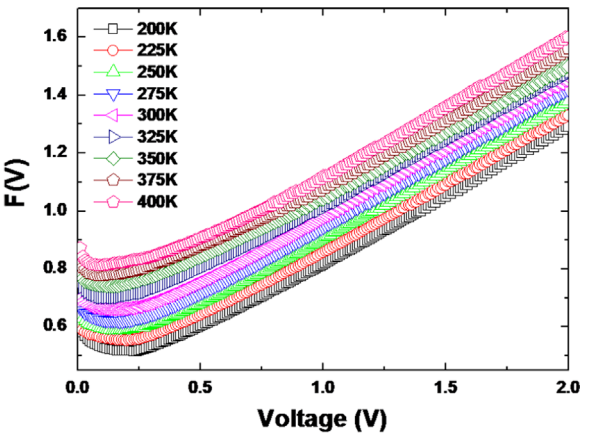

Fig. 6. $F(V)$ versus V for Al/sSOI Schottky diode at various temperatures in the case where thermionic emission dominates.

The C–V measurements were carried out for the Al/p-type sSOI Schottky diode to determine the interface quality as well as barrier height. Fig. 7 represents the experimental reverse bias C^{-2}–V characteristics of the Al/p-type sSOI Schottky contacts over the temperature range of 200–400 K in steps of 25 K. The junction capacitance was measured at a frequency of 1 MHz. In Schottky diodes, the depletion layer capacitance is expressed as [16]

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_s q N_A A^2}\right)\left(V_{bi} - \frac{kT}{q} - V\right) \tag{14}$$

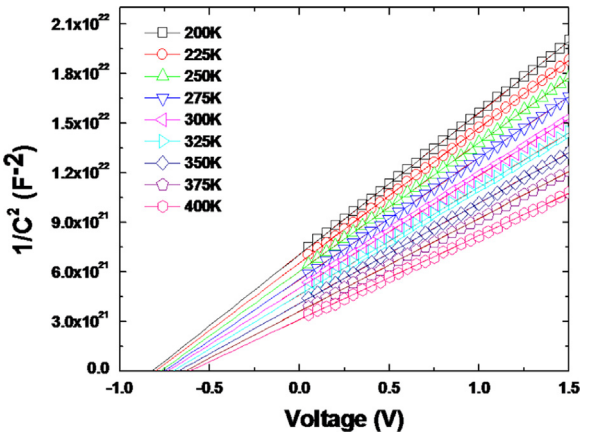

Fig. 7. $1/C^2$–V characteristics of the Al/sSOI Schottky diode in the temperature range of 200–400 K.

where N^A, A, and ε_s are carrier concentration, area of the Schottky contact, and the permittivity of the semiconductor ($\varepsilon_s = 12.5\varepsilon_0$), respectively. The x-axis intercept of the plot of C^{-2} versus V gives the diffusion potential V_0 and it is related to the built-in potential V_{bi} by the equation $V_{bi} = V_0 + kT/q$, where T is the absolute temperature. The barrier height $\Phi_{C\text{-}V}$ is given by the equation $\Phi_{C\text{-}V} = V_0 + V_n + kT/q$, where $V_n = (kT/q)\ln(N_V/N_A)$. The density of states in the valence band edge is given by $N_V = 2(2\pi m^* kT/h^2)^{3/2}$, where $m^* = 0.16m_0$ and its value is 1.603×10^{18} cm^{-3} for Si at room temperature [16]. The temperature dependence of N_A was calculated from the slope of reverse bias C^{-2}–V characteristics shown in Fig. 7. The N_A and N_V were calculated to be $(1.39\text{–}2.34) \times 10^{15}$ cm^{-3}and $(2.76\text{–}7.81) \times 10^{17}$ cm^{-3} in the temperature range of 200–400 K, respectively. The variation of N_A and V_{bi} depending on the temperature could be attributed to the modulation of space charge region caused by the emission of more carriers from the deep-level impurities at higher temperatures [31]. Based on the temperature dependent N_V and N_A values, the barrier heights of Al/p-type sSOI Schottky contacts extracted from C–V characteristics were calculated to be 1.01–0.97 eV at the temperatures in the range of 200–400 K. The temperature dependence of barrier heights ($\Phi_{C\text{-}V}$) is given in Table 1 and Fig. 4. Due to the square dependence of $\Phi_{C\text{-}V}$ on $1/C$, compared to the logarithmic dependence of Φ_{b0} on the current, $\Phi_{C\text{-}V}$ is more sensitive to the experimental errors of the measured data than Φ_{b0} [32]. From Fig. 4, it was also observed that the $\Phi_{C\text{-}V}$ slightly decreases with increasing temperature. The temperature dependence of $\Phi_{C\text{-}V}$ is expressed as

$$\Phi_{C\text{-}V} = \Phi_{C\text{-}V}(0\ \text{K}) + \alpha T \tag{15}$$

where $\Phi_{C\text{-}V}(0\ \text{K})$ is the barrier height extrapolated to 0 K and α is the temperature coefficient of the barrier height. From the fitting of experimental $\Phi_{C\text{-}V}$ data shown in Fig. 4, the $\Phi_{C\text{-}V}(0\ \text{K})$ and α were found to be 1.05 eV and -1.86×10^{-4} eV/K, respectively. Generally, the temperature dependence of the barrier height should follow the temperature dependence of the band gap with a coefficient, which is almost identical to that of the band gap [33,34]. This is due to the decrease in barrier height with increasing temperature associated with the shrinking of the band gap at higher temperature [34]. Moreover, the barrier heights extracted from C–V measurements was higher than those obtained from I–V measurements, regardless of temperature. Such a discrepancy between barrier heights obtained from I–V and C–V measurements could be attributed to the spatial inhomogeneity of the barrier height at the Al/p-type sSOI interface [35,36].

The barrier height estimated under flat-band condition is called flat-band barrier height (Φ_{bf}) and is considered to be real fundamental quantity. Unlike the zero-bias barrier height obtained from Eq. (3), the electrical field in the semiconductor is zero under the flat-band condition and semiconductor bands are flat, which eliminates the effect of tunneling and image force lowering that would affect the I–V characteristics and removes the influence of lateral inhomogeneity [33,37]. The Φ_{bf} can be calculated from the experimental ideality factor and zero-bias barrier height using [38,39]

$$\Phi_{bf} = n\Phi_{b0} - (n-1)\left(\frac{kT}{q}\right)\ln\left(\frac{N_V}{N_A}\right) \tag{16}$$

A plot of the Φ_{bf} as a function of temperature is shown in Fig. 4. The temperature dependence of the flat-band barrier height is described as [38,39]

$$\Phi_{bf}(T) = \Phi_{bf}(0\ \text{K}) + \alpha T \tag{17}$$

where $\Phi_{bf}(0\ \text{K})$ is the zero-temperature flat-band barrier height and α is the temperature coefficient of Φ_{bf}. Based on Eq. (17), the linear fitting of the experimental $\Phi_{bf}(T)$ data shown in Fig. 4 yielded $\Phi_{bf}\ (0\ \text{K}) = 0.95$ eV and $\alpha = -1.08 \times 10^{-4}$ eV/K. It should be noted that Φ_{bf} was always larger than zero-bias barrier height. This is possibly due to extremely high values of the ideality factor, which increased with decreasing temperature. Furthermore, the values of α obtained from the flat-band barrier height were in close agreement with those from C–V characteristics.

The non-ideal behavior of the forward bias I–V characteristics of the Al/p-type sSOI Schottky barrier diode can be explained by the Richardson plot of $\ln(I_0/T^2)$ versus $10^3/T$, obtained by rewriting Eq. (2) as

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{q\Phi_{b0}}{kT} \tag{18}$$

Fig. 8 shows the plot of $\ln(I_0/T^2)$ versus $10^3/T$ and $10^3/nt$ taken from Al/p-type sSOI Schottky diode. According to Eq. (18), the plot $\ln(I_0/T^2)$ versus $10^3/T$ yields a straight line with the slope and y-axis intercept corresponding to the activation energy (E_a) and the Richardson constant (A^*), respectively. The $\ln(I_0/T^2) - 10^3/T$ plot was nonlinear in the measured temperature range and exhibited two linear regions (region I (350–400 K) and region II (200–325 K)) with different slopes. Deviation from the linearity of the plot of $\ln(I_0/T^2)$ versus $10^3/T$ was caused by the temperature dependence of the barrier height and ideality factor associated with the existence of the inhomogeneities at the interface consisting of high and low barrier areas. For region I (350–400 K), the values of E_a and A^* were obtained as 0.43 eV and 7.32×10^{-4} A cm^{-2} K^{-2}, respectively. As for region II (200–325 K), the values of E_a and A^* were found

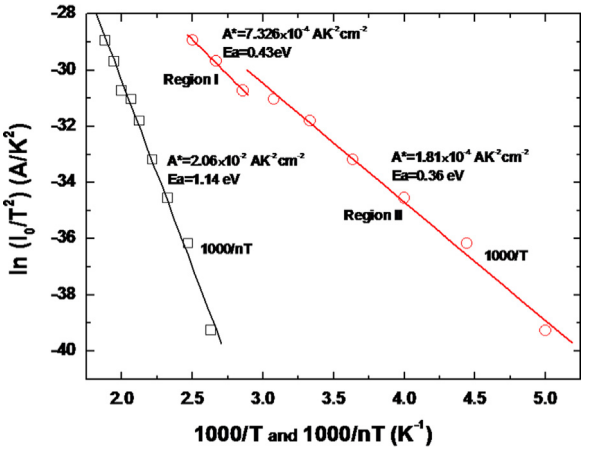

Fig. 8. Richardson plot of $\ln(I_0/T^2)$ against $10^3/T$ or $10^3/nT$ for Al/sSOI Schottky diode.

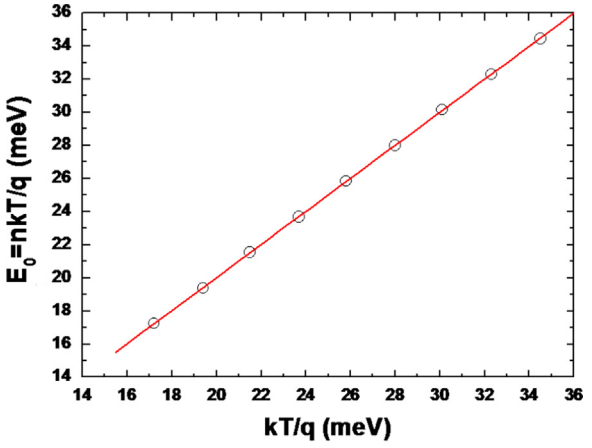

Fig. 9. Experimentally found tunneling current parameter nkT/q versus kT/q assuming thermionic emission theory for Al/sSOI Schottky diode.

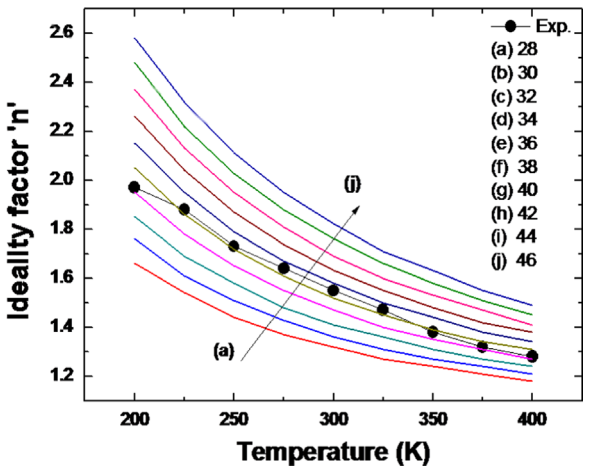

Fig. 10. Experimentally and theoretically found n_{tun} values for the Al/sSOI Schottky diode in the temperature range of 200–400 K.

to be 0.36 eV and 1.81×10^{-4} A cm^{-2} K^{-2}, respectively. The values of A^* extracted from both linear regions were much lower than the theoretical value of p-type sSOI (31.6 A K^{-2} cm^{-2}). Such a large discrepancy between the experimental and the theoretical values of A^* could be associated with a spatially inhomogeneous barrier height and potential fluctuations at the metal–semiconductor interface. Generally, current preferentially flows through the lower barriers in the potential distribution. According to Horvath [40], the A^* obtained from the temperature dependence of I–V characteristics may be affected by the lateral inhomogeneity of the barrier, and the fact that it is different from the theoretical value may be connected to a value of the real effective mass which is different from the calculated one. Also, the nonlinear behavior of $\ln(I_0/T^2) - 10^3/T$ plot in the measured temperature range could be attributed to the extra current contribution caused by apparent reduction in the barrier height. On the other hand, the plot of $\ln(I_0/T^2)$ versus$10^3/nT$ obtained from the Al/p-type sSOI Schottky diode was found to be linear in the whole measured temperature range. This essentially implies that Φ_{b0} reduces to Φ_{b0}/n, when increasing ideality factor with decreasing temperature. The replacement of T by nT or $(T+T_0)$ (since $nT=T+T_0$) in Eq. (2) for understanding the deviation of the Arrhenius plot from linearity was popularly referred to as "T_0 effect". The E_a and A^* corresponding to the slope and y-axis intercept of fitted line to the data of $\ln(I_0/T^2) - 10^3/nT$ plot, respectively, were found to be 1.14 eV and 2.06×10^2 A cm^{-2} K^{-2}, respectively.

The dominant current transport mechanism in Schottky barrier diode is especially dependent on ambient/sample temperature, applied bias voltage, surface preparation, formation of a native/deposited interfacial layer and the form of barrier heights at metal–semiconductor interface. As can be seen in Table 1, the decrease in barrier height and increase in ideality factor with decreasing temperatures indicates a deviation from the pure TE theory, suggesting that the tunneling current mechanisms such as thermionic field emission (TFE) and field emission (FE) are possible current transport mechanisms. If the current transport is controlled by the TFE or FE theory, the relationship between the forward bias voltage and current can be expressed as [17,41]

$$I = I_{tun}\left[\exp\left(\frac{q(V)}{E_0}\right) - 1\right] \tag{19}$$

with

$$n_{tun} = \frac{qE_{00}}{kT}\coth\left(\frac{E_{00}}{kT}\right) = \frac{qE_0}{kT} \tag{20}$$

where E_{00} is the characteristic tunneling energy that is related to the tunnel effect transmission probability:

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_A}{m_e^* \varepsilon_s}\right)^{\frac{1}{2}} \tag{21}$$

where h is Plank's constant. Based on Eq. (21), E_{00} was obtained as 0.427 meV at room temperature. It is well known that TFE should be valid when $E_{00} \approx kT/q$, whereas TE dominates when $E_{00} \ll kT/q$ and the FE becomes important when $E_{00} \gg kT/q$. Fig. 9 shows $E_0(=nkT/q) - kT/q$ plot taken from the Al/p-type sSOI Schottky barrier diode in temperature range of 200–400 K. The E_0 was calculated to be 52 meV corresponding to a doping concentration of 1.52×10^{19} cm^{-3}. The obtained experimental value of E_0

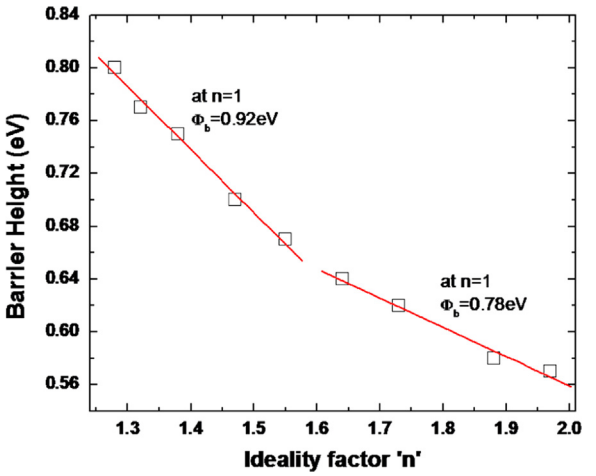

Fig. 11. The zero-bias barrier height versus ideality factor for the Al/sSOI Schottky barrier diode as a function of temperature.

was not close to the theoretical value of 0.427 meV calculated from the initial hole concentration of p-type sSOI. From the experimental values, the increase in ideality factor was further analyzed by considering the tunneling current as the cause for the variation of the ideality factor. When considering the bias coefficient of the barrier height, β, Eq. (20) can be written as [21,41]

$$n_{tun} = \frac{qE_0}{kT(1-\beta)} \tag{22}$$

where $\beta = d\Phi_b/dV$. Fig. 10 represents the theoretical temperature dependence of the ideality factor for the case when the current through Schottky junction is dominated by the TFE. The solid lines in Fig. 10 were obtained by fitting Eq. (22) to the experimental temperature dependence values of ideality factor for different values of the characteristic energy E_{00} without considering the bias coefficient of the barrier height, $\beta = 0$, for the Al/p-type sSOI Schottky barrier diode. The filled circles in Fig. 10 shows the temperature dependence values of ideality factor obtained from the experimental *I–V* characteristics. The experimental temperature dependence of ideality factor was in agreement with the curve (e) obtained with $E_{00} = 36$ meV for the Al/p-type sSOI Schottky barrier diode studied in the temperature range 200–400 K. The E_{00} of 36 meV was much larger than the theoretical value of 0.427 meV for Al/p-type sSOI Schottky barrier diode. To understand the possible origin of the high E_{00}, it should be underlined that E_{00} is connected with the transmission probability [42,43]. The high E_{00} is related to several effects such as the electric field present on the surface of the semiconductor, the existence of interfacial insulating layer between the deposited metal and semiconductor and the density of states [40,44]. Therefore, any mechanism which enhances the electric field or the density of states at the semiconductor surface will increase the TFE, resulting in high E_{00}.

According to Tung's theoretical approach, experimental zero-bias barrier heights are linearly correlated with ideality factors. As shown in the plot of experimental zero-bias barrier height as a function of ideality factor obtained from Al/p-type sSOI Schottky diode structure (Fig. 11), the experimental zero-bias barrier height decreased with increasing ideality factor. The plot clearly revealed that there were two linear regions. This could be associated with the lateral inhomogeneities of the barrier heights [45,46]. In the region I (300–400 K), from the extrapolation of the plot to $n = 1$ a homogeneous barrier height was found to be 0.92 eV, which was close to the band gap of Si. In the region II (200–275 K), homogeneous barrier height extracted using same calculation approach was estimated to be 0.78 eV, approximately corresponding to half of the band gap of Si. This indicates that under forward bias the current transport for $T \geq 300$ K is controlled by TE and for $T \leq 300$ K by the TFE [16,47]. These results also confirm the presence of double Gaussian distribution of barrier height in present devices. Thus, the significant decrease in the zero-bias barrier height and the increase in the ideality factor especially at low temperature were possibly caused by the barrier inhomogeneities.

From the above observations, it should be noted that the barrier height in the contact area can be modeled with double Gaussian distribution of barrier height. A spatial distribution of the barrier height at the metal–semiconductor interface of Schottky contacts by Gaussian distribution $P(\Phi_{b0})$ with a standard deviation σ_o around a mean Schottky barrier height $\overline{\Phi_{b0}}$ value was suggested by Werner and Guttler [38,39] which can be given as

$$P(\Phi_{b0}) = \frac{1}{\sigma_0\sqrt{2\pi}}\exp\left[-\frac{(\Phi_{b0}-\overline{\Phi_{b0}})^2}{2\sigma_o^2}\right] \tag{23}$$

where the pre-exponential term is the normalization constant of the Gaussian barrier height distribution. The total current across a Schottky contact at a forward bias is given by

$$I(V) = \int_{-\infty}^{+\infty} I(\Phi_{b0}, V)P(\Phi_{b0})d\Phi_{b0} \tag{24}$$

where $I(\Phi_{b0},V)$ is the current for a barrier of height Φ_{b0} at voltage *V*. By introducing $I(\Phi_{b0},V)$ and $P(\Phi_{b0})$ from Eqs. (1) and (23) in Eq. (24), the current of the Schottky barrier diode with the modified barrier is given by

$$I(V) = AA^*T^2\exp\left[-\frac{q}{kT}\left(\overline{\Phi_{b0}}-\frac{q\sigma_o^2}{2kT}\right)\right]\exp\left(\frac{qV}{n_{ap}kT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{25}$$

with

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_{ap}}{kT}\right) \tag{26}$$

where Φ_{ap} and n_{ap} are the apparent barrier height and apparent ideality factor, respectively. The Φ_{ap} is expressed by [35,38]:

$$\Phi_{ap} = \overline{\Phi_{bo}} - \frac{q\sigma_o^2}{2kT} \tag{27}$$

The above expression for the extraction of apparent barrier height has been already used by Duman et al. [48], Song et al. [35], and Werner and Guttler [38]. The observed variation in the ideality factor with temperature in the

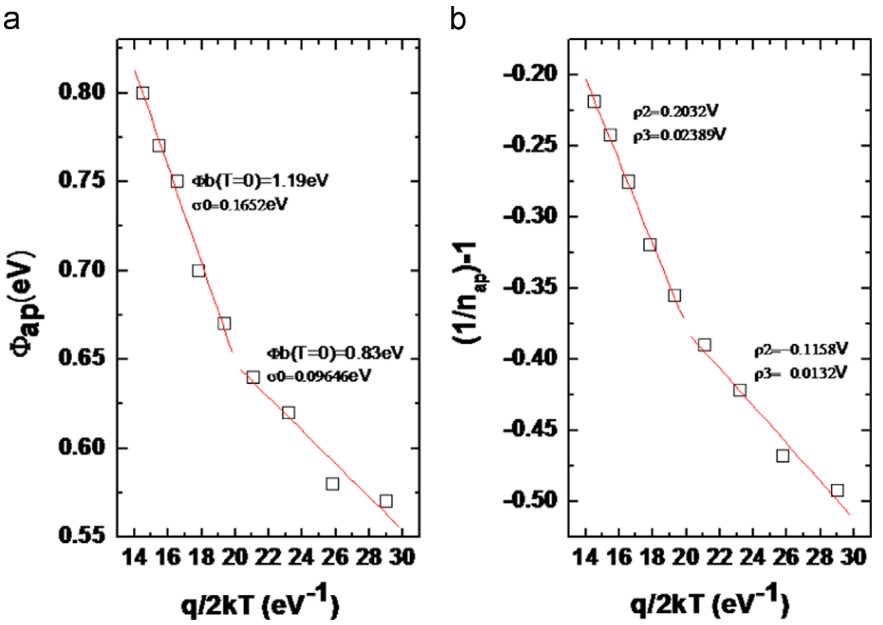

Fig. 12. (a) Zero-bias barrier height and (b) ideality factor versus $1/2kT$ curves and their linear fits for the Al/sSOI Schottky barrier diode according to Gaussian distribution of the barrier heights.

model is given by [35,38]

$$\left(\frac{1}{n_{ap}}-1\right)=-\rho_2+\frac{q\rho_3}{2kT} \tag{28}$$

where ρ_2 and $\rho_3$are voltage coefficients depending on the temperature which are used to quantify the voltage deformation of the barrier height distribution [32,37]. Based on Eqs. (27) and (28), the experimental $\Phi_{ap}-q/2kT$ and $(1/n_{ap})^{-1}-q/2kT$ plots (Fig. 12) were drawn to obtain the evidence of double Gaussian distribution of the barrier heights. The both plots clearly revealed that there were two straight lines with the transition occurring at 300 K rather than single one. This indicates the presence of double Gaussian distribution of barrier heights in the rectifier contact area. The intercept and slopes of these straight lines in Fig. 12(a) gave two sets of values of $\overline{\Phi_{b0}}$ and σ_0 as 1.19 and 0.16 eV in the temperature range of 300–400 K and 0.83 and 0.10 eV in the temperature range of 200–275 K, respectively. Since the σ_0 is a measure of the barrier homogeneity; lower σ_0 corresponds to more homogeneous barrier height. Obviously, the Schottky barrier diode with the best rectifying performance presents the best barrier homogeneity with the minimum σ_0. It was seen that the values of $\sigma_0=0.16$ and 0.10 eV are not small compared to the mean values of $\overline{\Phi_{bo}}=1.19$ and 0.83 eV in the temperature range of 300–400 K and 200–275 K respectively, indicates the presence of the interface inhomogeneities. Nevertheless, this inhomogeneity dramatically affects the *I–V* characteristics, particularly at low temperatures. Moreover, the plot of $(1/n_{ap})^{-1}$ versus $q/2kT$ (Fig. 12(b)) should also possess different characteristics in the two temperature ranges because the structure contains two barrier height distributions. The values of ρ_2 and ρ_3 obtained from the *y*-axis intercept and the slope of the $(1/n_{ap})^{-1}-q/2kT$ plot were -0.2032 and -0.0289 V in the temperature range of 300–400 K, and 0.1158 and -0.0132 V in the temperature range of 200–275 K, respectively.

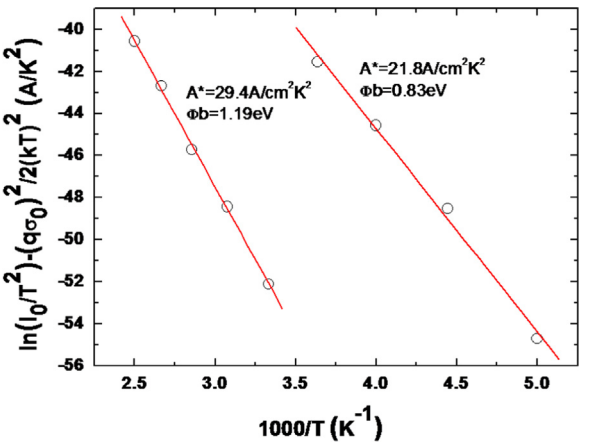

Fig. 13. The modified Richardson plot of $\ln(I_0/T^2)-q^2\sigma_0^2/2k^2T^2$ versus $q/2kT$ for Al/sSOI Schottky barrier diode according to Gaussian distribution of the barrier heights.

As indicated earlier, the Richardson constant extracted from the conventional Richardson plot of $\ln(I_0/T^2)$ versus $10^3/T$ (Fig. 8) was much lower than the theoretical value of sSOI. To obtain more reliable values of the Richardson constant by minimizing the effect of barrier inhomogeneity on the *I–V* characteristics of the Al/p-type sSOI Schottky diode, we employed a modified Richardson plot (Fig. 13) using Eq. (29) combined with Eqs. (26) and (27) as follows:

$$\ln\left(\frac{I_0}{T^2}\right)-\left(\frac{q^2\sigma_0{}^2}{2k^2T^2}\right)=\ln(AA^*)-\frac{q\overline{\Phi_{b0}}}{kT} \tag{29}$$

A fit to the modified Richardson plot of $\ln(I_0/T^2)-(q^2\sigma_0{}^2 2k^2T^2)$ versus $10^3/T$ (Fig. 13) should be a straight line of which slope and y-axis intercept correspond to $\overline{\Phi_{bo}}$ and modified Richardson constant A^* for a given diode area A, respectively. The values of the modified Richardson constant were calculated to be 29.4 and 21.8 A cm^{-2} K^{-2}, in the temperature range of 300–400 K and 200–275 K, respectively. These values were comparable to the theoretical value for p-type sSOI (31.6 A cm^{-2} K^{-2}) [49].

4. Conclusion

Temperature dependence of Schottky barrier parameters of Al/p-type sSOI Schottky barrier diodes was investigated using I–V and C–V in the wide temperature range of 200–400 K in steps of 25 K. Calculations showed that with increasing temperature, the barrier height and ideality factor increased and decreased, respectively. This anomalous temperature dependence of the barrier height and ideality factor could be associated with the nature of inhomogeneous Schottky barrier consisting of a combination of low and high barrier patches. Homogeneous barrier heights, extracted from the linear relationship between barrier height and ideality factor, were found to be 0.78 and 0.92 eV in the temperature ranges of 200–275 K and 300–400 K, respectively. The temperature-dependent I–V characteristics demonstrated the presence of a double Gaussian distribution with mean barrier heights of 0.83 and 1.19 eV and standard deviations of 0.10 and 0.16 eV at 200–275 and 300–400 K, respectively. From $\ln(I_0/T^2)-(q^2\sigma_0{}^2 2k^2T^2)-10^3/T$ plot, the modified Richardson constant was estimated to be 29.4 and 21.8 A cm^{-2} K^{-2} at 200–275 and 300–400 K, respectively, of which values were comparable to theoretical value for p-type sSOI (31.6 A cm^{-2} K^{-2}).

Acknowledgment

This research was supported by a grant from the R&D Program (Grant No. 10045216) for Industrial Core Technology funded by the Ministry of Trade, Industry and Energy (MOTIE), Republic of Korea, and by research support project of the ETRI (Grant No. B0132-15-1001) by the Ministry of Science, ICT and Future Republic of Korea. It was also financially supported by Basic Science Research Program (NRF-2015R1A6A1A04020421) through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Republic of Korea.

References

[1] Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, S.H. Lo G. Sai-Halasz, R. Viswanathan, H.J.C. Wann, S. Wind, H.-S. Wong, Proc. IEEE 85 (1997) 486–504.
[2] S. Asai, Y. Wada, Proc. IEEE 85 (1997) 505–520.
[3] R. Choi, K. Onishi, C.S. Kang, S. Gopalan, R. Nieh, Y.H. Kim, J.H. Han, S. Krishnan, H.-J. Cho, A. Shahriar, J.C. Lee, IEDM Technical Digest 2002, pp.613–616.
[4] G. Lucovsky, B. Rayner, Y. Zhang, J. Whitten, IEDM Technical Digest 2002, pp. 617–620.
[5] I. Lauer, T.A. Langdo, Z.-Y. Cheng, J.G. Fiorenza, G. Braithwaite M.T. Currie, C.W. Leitz, A. Lochtefeld, H. Badawi, M.T. Bulsara, M. Somerville, D.A. Antoniadis, IEEE Electron Device Lett. 25 (2004) 83–85.
[6] S. Takagi, N. Sugiyama, T. Mizuno, T. Tezuka, A. Kurobe, Mater. Sci. Eng. B 89 (2002) 426–434.
[7] T. Mizuno, S. Takagi, N. Sugiyama, H. Satake, A. Kurobe, A. Toriumi, IEEE Electron Device Lett. 21 (2000) 230–232.
[8] C.F. Beranger, P. Perreau, O. Weber, I. Ben-Akkez, A. Cros, A. Bajolet, S. Haendler, P. Fonteneau, P. Gouraud, E. Richard, F. Abbate, D. Barge, D.P. Tanon, B. Dumont, F. Andrieu, J. Passieux, R. Bon, V. Barral, D. Golanski, D. Petit, N. Planes, O. Bonin, W. Schwarzenbach, T. Poiroux, O. Faynot, M. Haond, F. Boeuf, Symposium on VLSI Technology Digest of Technical Papers 2012, pp. 115–116.
[9] W. Ruming, S. Hao, T. Teng, L. Lingyun, S. Xiaowei, J. Semicond. 33 (2012) 104001-1–104001-4.
[10] F. Mohammed, M.F. Bain, F.H. Ruddell, D. Linton, H.S. Gamble V.F. Fusco, IEEE Trans. Electron Devices 52 (2005) 1384–1391.
[11] E. Hokelek, G.Y. Robinson, Appl. Phys. Lett. 40 (1982) 426.
[12] K. Hattori, Y. Izumi, J. Appl. Phys. 53 (1982) 6906.
[13] F.E. Jones, C.D. Hafer, B.P. Wood, R.G. Danner, M.C. Lonergan, J. Appl. Phys. 90(2001) 1001.
[14] O. Gullu, A. Turut, Sol. Energy Mater. Sol. Cells 92 (2008) 1205.
[15] M. Bruel, Nucl. Instrum. Methods B 108 (1996) 313–319.
[16] E.H. Rhoderick, R.H. Williams, Metal–Semiconductor Contacts, second ed. Clarendon Press, Oxford, 1988.
[17] H.C. Card, E.H. Rhoderick, J. Phys. D: Appl. Phys. 4 (1971) 1589–1601.
[18] F.Z. Pur, A. Tataroglu, Phys. Scr. 86 (2012) 035802-1–035802-7.
[19] V. Janardhanam, I. Jyothi, K.S. Ahn, C.J. Choi, Thin Solid Films 546 (2013) 63–68.
[20] S. Chand, J. Kumar, Appl. Phys. A 63 (1996) 171–178.
[21] F.A. Padovani, G. Sumner, J. Appl. Phys. 36 (1965) 3744–3747.
[22] N. Tugluoglu, S. Karadeniz, M. Sahin, H. Safak, Appl. Surf. Sci. 233 (2004) 320–327.
[23] R. Hackam, P. Harrop, IEEE Trans. Electron Devices 19 (1972) 1231–1238.
[24] S. Altındal, I. Dokme, M.M. Bulbul, N. Yalcın, T. Serin, Microelectron. Eng. 83 (2006) 499–505.
[25] M.O. Aboelfotoh, K.N. Tu, Phys. Rev. B 34 (1986) 2311–2318.
[26] I. Vurgaftman, J.R. Meyer, L.R. Ram-Mohan, J. Appl. Phys. 89 (2001) 5815–5875.
[27] R. Passler, Phys. Rev. B 66 (2002). 085201-1 – 085201-18.
[28] S. Aydogan, M. Saglam, A. Turut, Microelectron. Eng. 85 (2008) 278–283.
[29] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. 49 (1986) 85–87.
[30] H. Norde, J. Appl. Phys. 50 (1979) 5052–5053.
[31] N. Yıldırım, K. Ejderha, A. Turut, J. Appl. Phys 108 (2010) 114506–114508.
[32] S.Y. Zhu, R.L. Van Meirhaeghe, C. Detavernier, F. Cardon, G.P. Ru X.P. Qu, B.Z. Li, Solid-State Electron 44 (2000) 663–671.
[33] M.O. Aboelfotoh, J. Appl. Phys. 66 (1989) 262–272.
[34] C. Lu, S.N. Mohammad, Appl. Phys. Lett. 89 (2006) 162111-1–162111-3.
[35] Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, Solid-State Electron. 29 (1986) 633–638.
[36] I. Jyothi, V. Janardhanam, Y.R. Lim, V. Rajagopal Reddy, K.S. Ahn C.J. Choi, Mater. Sci. Semicond. Process. 30 (2015) 420–428.
[37] A. Gümüs, A. Türüt, N. Yalçin, J. Appl. Phys. 91 (2002) 245–250.
[38] J.H. Werner, H.H. Guttler, J. Appl. Phys. 69 (1991) 1522–1533.
[39] J.H. Werner, H.H. Guttler, J. Appl. Phys. 73 (1993) 1315–1319.
[40] Z.s.J. Horvath, Solid-State Electron. 39 (1996) 176–178.
[41] F.A. Padovani, J. Appl. Phys. 37 (1966) 921–922.
[42] F.E. Jones, B.P. Wood, J.A. Myers, C.H. Daniels, M.C. Lonergan, J. Appl. Phys. 86 (1999) 6431–6441.
[43] J. Osvald, Semicond. Sci. Technol. 18 (2003) L24–L26.
[44] M.K. Hudait, P.V. Venkateswaralu, S.B. Krupanidhi, Solid-State Electron. 45 (2001) 133–141.
[45] S. Karataş, S. Altındal, A. Turut, A. Ozmen, Appl. Surf. Sci. 217 (2003) 250–260.
[46] R.F. Schmitsdorf, T.U. Kampen, W. Mönch, Surf. Sci. 324 (1995) 249–256.
[47] S.M. Sze, K. Ng Kwok, Physics of Semiconductor Devices, 3rd ed. Wiley, New Jersey, 2007.
[48] S. Duman, B. Gurbulak, A. Türüt, Appl. Surf. Sci. 253 (2007) 3899–3905.
[49] S. Chattopadhyay, L.K. Bera, S.K. Ray, C.K. Maiti, Appl. Phys. Lett. 71 (1997) 942–944.