Misfit dislocation–related deep levels in InGaAs/GaAs and GaAsSb/GaAs p–i–n heterostructures and the effect of these on the relaxation time of nonequilibrium carriers

M. M. Sobolev,[a] F. Yu. Soldatenkov,[b] and I. L. Shul'pina
Ioffe Institute, 194021 St. Petersburg, Russia

(Received 31 October 2017; accepted 22 January 2018; published online 7 February 2018)

A study of deep levels in InGaAs/GaAs and GaAsSb/GaAs p^0–i–n^0 heterostructures with misfit dislocations and identification of the effective defects responsible for the significant (by up to a factor of 100) decrease in the relaxation time of nonequilibrium carriers in the base layers (and in the related reverse recovery time) of InGaAs/GaAs and GaAsSb/GaAs high-voltage power p-i-n diodes is reported. Experimental capacitance–voltage characteristics and deep-level transient spectroscopy spectra of p^+–p^0–i–n^0–n^+ homostructures based on undoped GaAs layers without misfit dislocations and InGaAs/GaAs and GaAsSb/GaAs heterostructures with a homogeneous network of misfit dislocations, all grown by liquid-phase epitaxy, are analyzed. Acceptor defects with deep levels HL2 and HL5 are identified in GaAs epitaxial p^0 and n^0 layers. Dislocation-related electron and hole deep traps designated as ED1 and HD3 are detected in InGaAs/GaAs and GaAsSb/GaAs heterostructures. The effective recombination centers in the heterostructure layers, to which we attribute the substantial decrease in the relaxation time of nonequilibrium carriers in the base layers of p-i-n diodes, are dislocation-related hole traps that are similar to HD3 and have the following parameters: thermal activation energy $E_t = 845$ meV, carrier capture cross-section $\sigma_p = 1.33 \times 10^{-12}$ cm^2, concentration $N_t = 3.80 \times 10^{14}$ cm^{-3} for InGaAs/GaAs and $E_t = 848$ meV, $\sigma_p = 2.73 \times 10^{-12}$ cm^2, and $N_t = 2.40 \times 10^{14}$ cm^{-3} for the GaAsSb/GaAs heterostructure. The relaxation time of the concentration of nonequilibrium carriers in the presence of dislocation-related deep acceptor traps similar to HD3 was estimated to be 1.1×10^{-10} and 8.5×10^{-11} s for, respectively, the InGaAs/GaAs and GaAsSb/GaAs heterostructures and 8.9×10^{-7} s for the GaAs homostructure. These data correspond to the relaxation times of nonequilibrium carriers in the base layers of GaAs, InGaAs/GaAs, and GaAsSb/GaAs high-voltage power p-i-n diodes. *Published by AIP Publishing.*
https://doi.org/10.1063/1.5011297

I. INTRODUCTION

The interest in high-voltage GaAs structures is due to the search for alternative (to silicon) materials for pulse power electronics, capable of working at higher pulse repetition rates and higher temperatures. Compared with silicon, GaAs has a wider energy gap, substantially higher electron mobility (which also exceeds that in SiC and GaN), higher dielectric strength, shorter carrier lifetimes, and better radiation hardness. One more advantage of GaAs is that it is a direct-band semiconductor material for which solid solutions can be obtained, so that the optical and electrical parameters of device layers in GaAs–III–V heteroepitaxial structures and the electrical characteristics of devices based on these structures can be widely varied. At present, the method of liquid-phase epitaxy (LPE) is mostly used to fabricate high-voltage (hundreds of volts) GaAs p–i–n structures.[1–4] These structures can be used to manufacture semiconductor devices for pulse power and high-frequency applications.[1–6]

As noted in Refs. 1, 3, 5, and 7, the temporal characteristics of gallium arsenide diodes (lifetime of nonequilibrium carriers and voltage rise time), as well as the voltage blocked by the diode structures, must be strongly affected by defects and deep-level (DL) interfacial states formed in the course of the epitaxial growth of p–i–n structures. The following ways to control the ensemble of intrinsic defects in LPE-grown epitaxial GaAs layers are presently known: (i) by changing the crystallization onset temperatures T_b[8] and (ii) by varying the atomic fraction of the isovalent bismuth impurity concentration in the solvent (Ga + Bi), which must lead to a change in the relative concentrations of Ga and As.[9] In GaAs p^+–p^0–i–n^0 structures are grown at crystallization onset temperatures $T_b = 650$–$800\,^\circ$C; deep-level transient spectroscopy (DLTS) revealed HL5 and HL2 trap levels[10] characteristic of GaAs layers produced by the LPE method in the atmosphere of hydrogen.[8,11] After the crystallization onset temperature was raised to $T_b \geq 850\,^\circ$C, a defect similar to EL2 was formed in epitaxial GaAs layers in addition to HL5 and HL2 defects.[8,12] With increasing Bi content in the solution-melt, the concentration of the DL HL5 and HL2 defects decreased due to the change in the relative concentrations of Ga and As.[9] For $In_xGa_{1-x}As$ and $GaAs_{1-x}Sb_x$ ($x < 0.012$ mol. %) epitaxial layers grown on a GaAs substrate, a similar suppression of hole traps was observed at a simultaneous decrease in the dislocation density.[13,14] Based on the experimental results they obtained, the authors of Ref. 15 concluded that the observed suppression effects are associated with local stresses appearing

[a]Electronic mail: m.sobolev@mail.ioffe.ru
[b]Electronic mail: f.soldatenkov@mail.ioffe.ru

around In and Sb atoms in $In_xGa_{1-x}As$ and $GaAs_{1-x}Sb_x$ solid solutions. It was noted in Refs. 16 and 17 that, with the content of isovalent impurities in the solid solutions raised to $x \approx (0.2–3)$ mol. %, a 2D network of 60° misfit dislocations is formed due to the lattice mismatch between the substrate and the layer at the substrate–layer interface as the layer thickness exceeds the critical value. The appearance of these dislocations may be accompanied by the formation of dislocations threading across the epitaxial layer. In Refs. 17 and 18, the DLTS technique was used to find in LPE-grown $In_xGa_{1-x}As$ and $GaAs_{1-x}Sb_x$heterostructures DLs with energies $(E_V + 0.67\,\text{eV})$ and $(E_C - 0.64\,\text{eV})$ in the energy gap. These levels were attributed to, respectively, misfit dislocations and threading dislocations and could serve as recombination centers or traps for free carriers.

Previously, it was shown in Ref. 3 that the appearance of a homogeneous network of dislocations is typical of $In_xGa_{1-x}As$ layers with thicknesses of 50 to 65 μm and compositions x in the range from 1.5 to 3 mol. %. The typical dislocation density of these networks was on the order of $100\,\text{cm}^{-1}$. To the appearance and development of the structural defects of this kind were attributed the observed effects in which the relaxation time of nonequilibrium carriers substantially (by up to a factor of 100) decreased and the voltages blocked by high-voltage InGaAs/GaAs diode heterostructures became somewhat (by up to a factor of 2) lower, which was due to the gradual rise in the dislocation network density upon an increase in x to ~3 mol. %.[3] Thus, there appeared a natural desire to study the ensemble of DLs in $In_xGa_{1-x}As$/GaAs and $GaAs_{1-x}Sb_x$/GaAs heterostructures with misfit dislocations and to identify the effective defects predetermining the considerable (by up to a factor of 100) decrease in the relaxation time of nonequilibrium carriers in the base layers and in the related reverse recovery time of InGaAs/GaAs and GaAsSb/GaAs high-voltage power p–i–n diodes.

In this communication, we report on a comparative study of the DLs related to point defects and dislocations in LPE-fabricated homoepitaxial GaAs and heteroepitaxial layers of InGaAs/GaAs and GaAsSb/GaAs p^0–i–n^0 diodes by the following methods of capacitance spectroscopy: capacitance–voltage (C–V) technique and DLTS, and present estimates of the influence exerted by acceptor-type dislocation traps on the relaxation times of the concentration of nonequilibrium carriers in the p^0–i–n^0 diodes.

II. EXPERIMENTAL SAMPLES

The GaAs homoepitaxial and $In_xGa_{1-x}As$, and $GaAs_{1-y}Sb_y$ heteroepitaxial p^+–p^0–i–n^0–n^+ diode structures were fabricated in two stages by the LPE method. The epitaxial growth of high-voltage lightly doped GaAs, $In_xGa_{1-x}As$, and $GaAs_{1-y}Sb_y$ graded p^0–i–n^0 junctions was performed by a modified LPE method[1,3,19] on p^+-GaAs (111)A substrates doped with zinc to $(2–5) \times 10^{18}\,\text{cm}^{-3}$ from a limited Ga–As, In–Ga–As, or Sb–Ga–As melt in a quartz boat-cassette in a flow of hydrogen in the range from 850 °C to room temperature. In the second stage, n^+-GaAs emitter layers of the diode structures, doped to $\sim 10^{18}\,\text{cm}^{-3}$, were additionally grown in a graphite piston cassette. Diode samples (chips) had the form of mesa structures produced by chemical etching of the active layers down to the substrate. A multilayer AgMn–Ni–Au contact was deposited onto a p^+-GaAs substrate, and AuGe–Ni–Au, onto the n^+-GaAs emitter.

With this method, lightly doped p^0–i–n^0 structures are obtained from a single solution-melt in the course of the same technological process. The content of electrically active defects in the epitaxial layers and their distribution across the layer thickness depend on the content of residual impurities in the melt and growth system, temperature, duration of the preliminary annealing of the solution-melt, flow rate of hydrogen and its moisture content, and film crystallization mode under forced cooling of the system. Solution-melts of required composition were prepared from metallic Ga (99.9999%), In (99.9995%), and Sb (99.9995%), with undoped polycrystalline GaAs produced by zone melting serving as the source of arsenic. The growth processes were carried out in a quartz tube in a flow of Pd-diffused hydrogen gas with a moisture content of about 1 ppm and an oxygen content of less than 1 ppm. To obtain high-voltage structures under study, the temperature-and-time mode and the hydrogen flow rate in the course of growth were selected so that the epitaxial layer had the form of a graded p^0–i–n^0 junction with free-carrier concentration in the i-type layer on the order of 10^{13}–$10^{14}\,\text{cm}^{-3}$, which makes it possible to reach voltages U_b blocked by the diodes of up to 1000 V and more.[2] Figure 1 shows a typical distribution of the free-carrier concentration in a p^+–p^0–i–n^0–n^+ structure of a high-voltage diode, obtained via its layer-by-layer etching from the C–V dependences for a reverse-biased Schottky barrier with a mercury probe.

The composition of the liquid phase used to deposit InGaAs or GaAsSb solid solution layers of required composition was determined by calculations in terms of the quasi-regular approximation model with consideration for the elastic strains appearing due to the lattice mismatch between the layer and the substrate.[1,3,20] The content of InAs (see Ref. 3) and GaSb in the epitaxial layers of the solid solutions was found from the results of an X-ray fluorescence microanalysis on a Camebax installation.

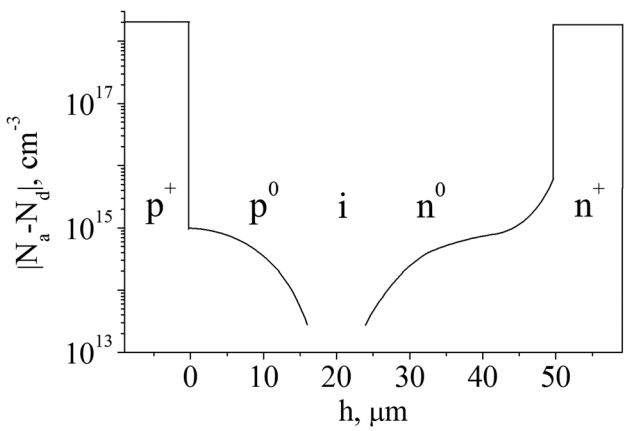

FIG. 1. Typical free carrier distribution across the thickness of GaAs, InGaAs, or GaAsSb high-voltage p^0–i–n^0 layers grown on p^+-GaAs substrates with a subsequently grown n^+-GaAs emitter.

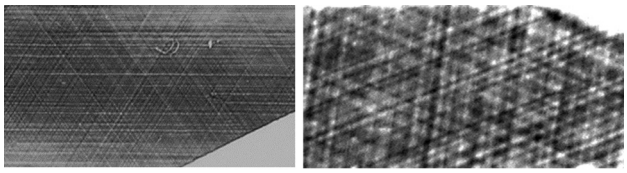

FIG. 2. X-ray back reflection topographs of (a) $In_xGa_{1-x}As/GaAs$ and (b) $GaAs_{1-y}Sb_y/GaAs$ heterostructures. CuK_α-radiation with reflection: (a) 422 and (b) 333.

The thickness and composition of the heteroepitaxial layers were chosen so as to exceed the critical thicknesses at which relaxation defects start to be formed in pseudomorphic films[1,3] and provide generation of misfit dislocations with density not exceeding 300 cm^{-1}. We studied diodes with the following thicknesses and chemical composition of the p^0–i–n^0 layers: (i) GaAs layers with a thickness of about 50 μm, (ii) $In_xGa_{1-x}As$ layers with a thickness of 56 μm and the maximum InAs content x of about 2.9 mol. %, and (iii) $GaAs_{1-y}Sb_y$ layers with a thickness of 42 μm and the maximum GaSb content y of about 2.7 mol. %.

The real structure of the samples was studied by back reflection X-ray diffraction topography[21] with CuK_α–radiation and a set of reflections to provide the best conditions for revealing defects in strongly absorbing materials at a large thickness of the information layer and narrow width of the diffraction peak. The reflected X-ray beam was passed through a slit in the nontransparent screen mounted between the sample and detector and recorded by using a photosensitive element, with scanning over this element and the sample, as it is done in the Lang method.[22,23] A set of misfit dislocations with different densities was observed in samples of $In_xGa_{1-x}As/GaAs$ and $GaAs_{1-y}Sb_y/GaAs$ heterostructures [Figs. 2(a) and 2(b)]. The dislocation density in the network of linear misfit dislocations was about 150 cm^{-1} for $In_xGa_{1-x}As/GaAs$ and about 15 cm^{-1} for the $GaAs_{1-y}Sb_y/GaAs$ heterostructure. The samples with a homoepitaxial GaAs layer had no ordered dislocation network, with only the dislocations characteristic of the substrate and those threading from the substrate into the layer observed in this case.

III. RESULTS AND DISCUSSION

C–V characteristics and DLTS spectra of chips of p^+–p^0–i–n^0–n^+ structures based on homoepitaxial GaAs and heteroepitaxial $In_xGa_{1-x}As/GaAs$ and $GaAs_{1-y}Sb_y/GaAs$ layers were studied with a BIORAD DL4600 DLTS spectrometer (UK) equipped with a Boxcar integrator.

A. *C–V* characteristics of p^+–p^0–i–n^0–n^+ diodes

The *C–V* characteristics of the diodes were examined at various temperatures and measurement conditions: (i) in the dark and (ii) under illumination of a sample in the course of measurements of the characteristics. For convenience of presentation of the results obtained in these measurements and their further interpretation, we calculated from the *C–V* characteristics, by using the differential capacitance method,[24] the distribution profiles of the free-carrier concentration (n^*) across the thickness (W) of the space-charge region (SCR).

Studies of p^+–p^0–i–n^0–n^+ structures based on epitaxial GaAs demonstrated that the changes observed in the *C–V* characteristics are associated with the temperature behavior of the diffusion potential. The optical recharging of deep acceptor traps in the i-type layer and in the adjacent p^0 and n^0 layers did not lead to any significant change in the effective carrier concentration in the conduction band of the epitaxial layers (n^*). The thickness W of the space charge layer at a measurement temperature of 300 K was about 3.5 μm.

The $n^*(W)$ distribution profiles of p^+–p^0–i–n^0–n^+ structures based on $In_xGa_{1-x}As/GaAs$ and $GaAs_{1-y}Sb_y/GaAs$ layers revealed strong differences between these structures and those based on GaAs [see Figs. 3(a) and 3(b)]. The results presented for both the heterostructures in Figs. 3(a) and 3(b) demonstrate that the SCR thickness grows as the sample measurement temperature is lowered to 86 K. It was found that, for these structures, the gains in the SCR thickness on changing the temperature from 300 to 86 K substantially exceed the values calculated on the assumption of being associated with

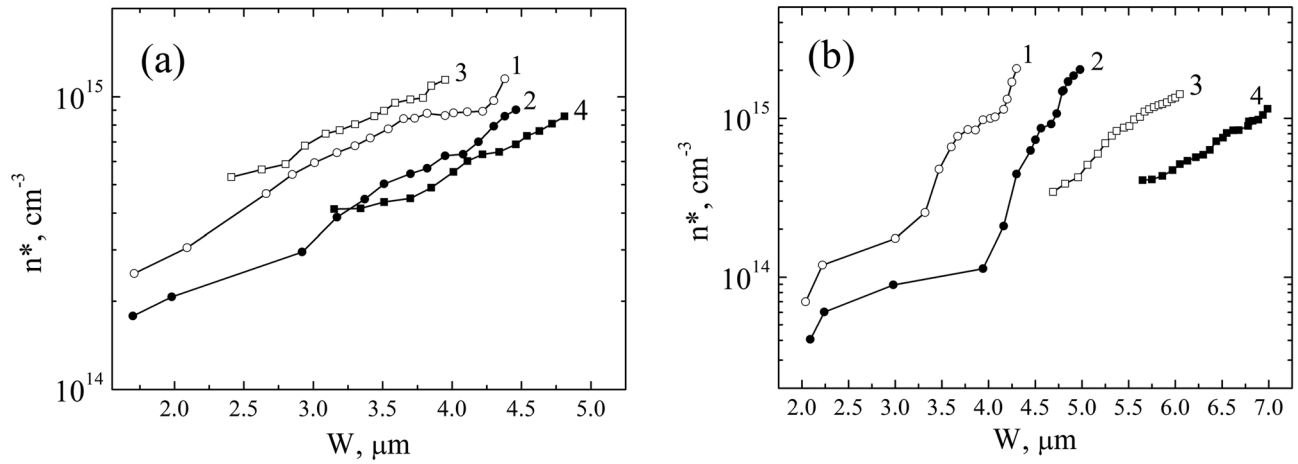

FIG. 3. Distribution profiles of the effective free-carrier concentration n^* across the thickness W of the space-charge layer in p^+–p^0–i–n^0–n^+ diodes based on heteroepitaxial layers: (a) $In_xGa_{1-x}As/GaAs$ and (b) $GaAs_{1-y}Sb_y/GaAs$, measured at various temperatures T, K: (1, 2) 300 and (3, 4) 80, measured (2, 4) in the dark and (1, 3) under illumination.

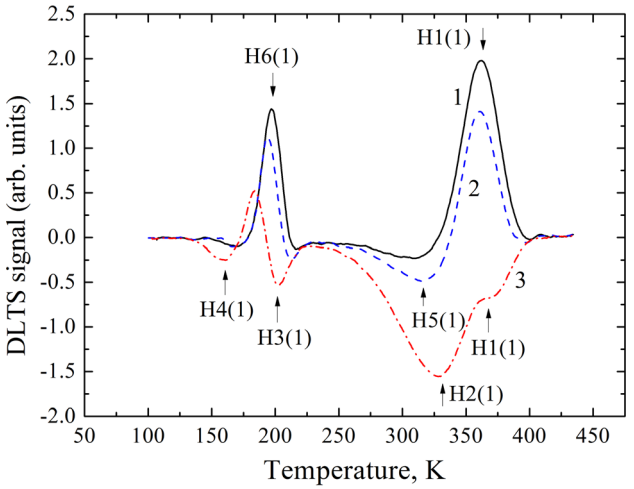

FIG. 4. DLTS spectra of a GaAs p^+–p^0–i–n^0–n^+ diode, measured at a window rate of 200 s^{-1}, filling pulse voltage $V_f = +0.96$ V, and reverse bias voltages V_r, V: (1) –1.01, (2) –0.48, and (3) + 0.12.

the temperature behavior of the diffusion potential. Also, the dependence of $n^*(W)$ on whether there is an optical illumination of a sample being measured was revealed for both the p^+–p^0–i–n^0–n^+ heterostructures [Figs. 3(a) and 3(b)]. The illumination of the structures led to a decrease in the SCR thickness at both 86 and 300 K. The most probable reason for these changes in the SCR thickness with temperature and illumination is deep interfacial states of donor and acceptor types at the heterointerfaces of the p^+–p^0–i–n^0–n^+ structures. The influence exerted by the density N_{ss} of the interfacial states on the C–V characteristic of a p–n junction was studied in detail in Refs. 25–28. In Ref. 26, the Poisson equation was solved to give the following relation with two terms:

$$\frac{1}{C^2} = -\frac{2(\varepsilon_n N_d + \varepsilon_p N_a)}{q\varepsilon_n\varepsilon_p N_d N_a}(V - V_o) - \frac{N_{ss}^2}{\varepsilon_n\varepsilon_p N_d N_a}, \qquad (1)$$

where V_0 is the diffusion potential, V is the reverse bias, ε_n and ε_p are the dielectric constants of the n and p layers, and N_d and N_a are the concentration of donors and acceptors in the n and p layers, respectively. The first term is associated with the capacitance of the SCR of the p–n junction, which varies with the applied bias voltage and with the distribution of the concentrations N_d and N_a in the n and p layers and the second is related to the density of interfacial states whose occupancy may vary with the measurement temperature and with the position of the Fermi level in the structure. The optical illumination of the p^+–p^0–i–n^0–n^+ heterostructure may lead, in the presence in the epitaxial layers of deep-level defects of the donor and acceptor type in concentrations comparable with those of shallow levels, to a change in the position of the Fermi level and, accordingly, to a change in the occupancy of localized interfacial states by carriers.

Therefore, the presence of the interfacial states is attributed to the formation of misfit dislocations at the heterointerfaces of the structures under study.

B. DLTS measurements of p^+–p^0–i–n^0–n^+ diode structures

For all three types of p^+–p^0–i–n^0–n^+ diode structures, we measured DLTS spectra at various bias (V_r) and filling pulse (V_f) voltages (Figs. 4, 6, and 8). The parameters of the DLs were determined and their identification (see Table I) was made by using the Arrhenius dependences in Figs. 5, 7, 9, and 10. It has been noted previously that epitaxial layers of a solid solution have the form of a graded p–i–n junction with free-carrier concentration in the i-type layer on the order of 10^{13}–10^{14} cm^{-3}. That is why the DLTS spectra were measured at both negative and positive bias voltages V_r. The filling pulse voltages V_f were positive, which made it possible to find deep levels for majority and minority carriers in the p^0 and n^0 layers of the structures under study.

TABLE I. Identification of electron and hole traps in LPE-grown GaAs, InGaAs/GaAs, and GaAsSb/GaAs p^+–p^0–i–n^0–n^+ diodes.

Deep level designation	Activation energy, meV	Capture cross-section, cm^2	Deep level concentration, cm^{-3}	Identity and nature of a deep level	References
GaAs					
H1(1)	695	3.89×10^{-15}	1.60×10^{13}	HL2 [V_{Ga}+]	8–10
H2(1)	499	4.69×10^{-17}	8.84×10^{15}	HS3 [Fe]	10
H4(1)	302	1.05×10^{-14}	2.0×10^{12}	HL6	10
H5(1)	643	2.06×10^{-14}	4.0×10^{12}	HL9	10
H6(1)	447	5.38×10^{-13}	3.8×10^{13}	HL5 [V_{Ga}+]	8–10
InGaAs					
E1(2)	653	1.06×10^{-13}	3.35×10^{14}	ED1	17, 18
H0(2)	709	2.56×10^{-15}	7.2×10^{13}	HB1 [Cr]	10
H1(2)	774	1.73×10^{-12}	3.8×10^{14}	HD3	17, 18
H1*(2)	845	1.33×10^{-12}	3.8×10^{14}	HD3	17, 18
H2(2)	696	4.69×10^{-15}	7.2×10^{13}	HL2 [V_{Ga}+]	8–10
H6(2)	409	6.35×10^{-14}	3.2×10^{13}	HL5 [V_{Ga}+]	8–10
GaAsSb					
E1(3)	683	1.16×10^{-14}	1.60×10^{14}	ED1	17, 18
H1(3)	848	2.73×10^{-12}	2.39×10^{14}	HD3	17, 18
H5(3)	627	1.69×10^{-15}	3.8×10^{13}	HL9	10
H6(3)	385	3.95×10^{-14}	1.98×10^{13}	HL5 [V_{Ga}+]	8–10

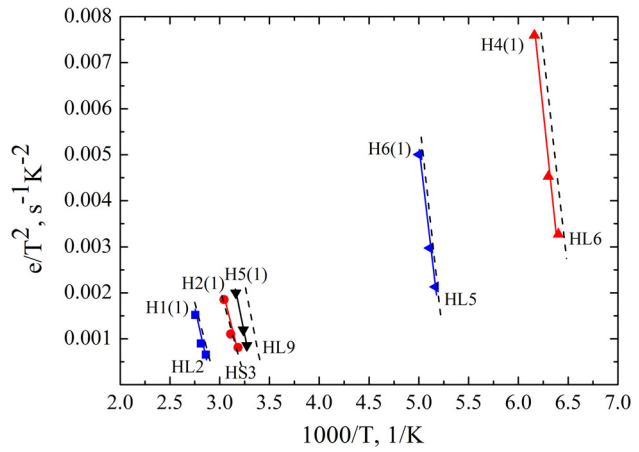

FIG. 5. Arrhenius temperature dependences of the thermal emission rates e of holes and electrons from deep traps in p^+–p^0–i–n^0–n^+ structures based on homoepitaxial GaAs layers. The dashed lines show the Arrhenius dependences for traps identified in Ref. 10.

Figure 4 shows DLTS spectra of a GaAs p^+–p^0–i–n^0–n^+ structure, measured at three values of V_r: –1.01 V (spectrum 1), –0.48 V (spectrum 2), and +0.12 V (spectrum 3) at a filling pulse voltage $V_f = +0.96$ V. It can be seen that four negative DLTS peaks, related to traps for majority carriers, are observed at $V_r = +0.12$ V. The filling pulse and the voltage at which the DLTS signal is measured are applied in the forward direction, and, therefore, the trap filling by carriers and their emission must mostly occur from the p^0 layer. In this layer, holes are majority carriers and their capture and emission are determined by acceptors with DLs. The DLTS spectra demonstrated, in addition to the four negative peaks, one DLTS peak with positive sign, the appearance of which in the DLTS spectrum is due to the emission of holes from the DLs in the n^0 layer. At reverse bias voltages $V_r = -0.48$ and –1.01 V, the amplitudes of negative-sign DLTS peaks either became substantially lower or completely disappeared, but there appeared two DLTS peaks with a positive sign and large amplitude: low-temperature and high-temperature (Fig. 4), which represent traps for minority carriers. At $V_r = -0.48$ and –1.01 V, the voltage at which the DLTS signal is measured was applied in the reverse direction, and therefore, the emission of minority carriers occurred from the n^0 layer and was attributed to holes that were captured to deep acceptor states. These measurements demonstrated that applying V_r with two different values and a forward or reverse bias voltage enabled us to identify the DLs in the p^0 and n^0 layers and to show that these DLs are related to the same defects, well known[8–10] for LPE-grown GaAs: HL2 and HL5 (Fig. 5). The same defects [H2(2) and H6(2) from Table I and Figs. 6(b) and 7] were observed in DLTS spectra of the InGaAs/GaAs layer, measured at $V_r = -2.42$ V and $V_f = -0.4$ V [Fig. 6(a), curve 1]. HL5 defect designated in Fig. 8 (curve 1) and Fig. 9 as H6(3) was also observed in the DLTS spectra of the GaAsSb/GaAs layer, measured at $V_r = -2.70$ V and $V_f = +0.50$ V. Instead of the HL2 defect, the H5(3) level appeared in DLTS spectra, which is attributed[10] to the known trap HL9. The HL5 level was not observed in our measurement conditions in the DLTS spectra of the GaAsSb/GaAs layer. Other levels were also observed in the DLTS spectra of the p^+–p^0–i–n^0–n^+ structures under study (Figs. 4, 6, and 8). These levels were identified with the well-known traps previously found in GaAs layers. For example, H2(1), H4(1), and H5(1) levels observed in GaAs layers were similar according to Arrhenius dependences in Ref. 10 to HS3, HL6, and HL9 traps (Fig. 5). The H0(2) level related to Cr impurity (HB1) was observed in InGaAs/GaAs layers [Figs. 6(a) and 7].[10]

The approach employed above to reveal defects with DLs in the GaAs p^+–p^0–i–n^0–n^+ structure on the basis of DLTS spectra was used to examine diodes of the InGaAs/GaAs and GaAsSb/GaAs p^+–p^0–i–n^0–n^+ heterostructures also grown at $T_b = 850$ °C (Figs. 6 and 8). The DLTS spectra shown in Figs. 6 and 8 were measured in the dark. When DLTS spectra were measured with illumination, the amplitudes of the DLTS peaks changed, which is a characteristic indication of spatially localized deep states: interfacial, quantum dots, etc. As shown in Refs. 29 and 30 for the DLTS spectra of localized states, the amplitude of the DLTS

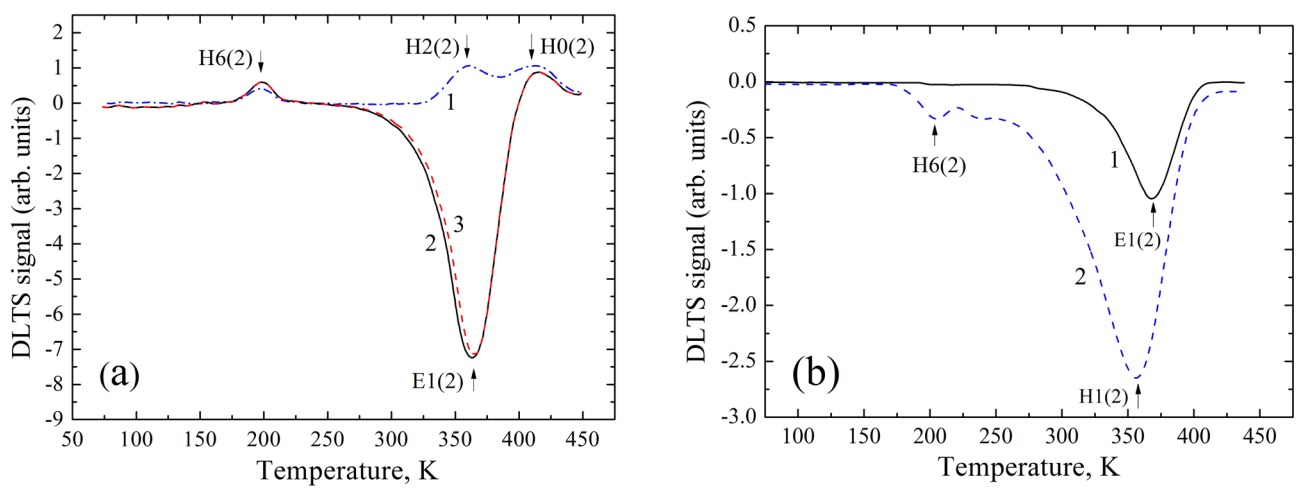

FIG. 6. DLTS spectra of an InGaAs/GaAs p^+–p^0–i–n^0–n^+ diode, measured at a window rate of 200^{-1} s: (a) at a reverse bias voltage $V_r = -2.42$ V and filling pulse voltages V_f, V: (1) –0.4, (2) +0.54, in the dark; (3) +0.54, under illumination; (b) at a filling pulse voltage $V_f = +0.50$ V and reverse bias voltages V_r, V: (1) –2.70 and (2) +0.01.

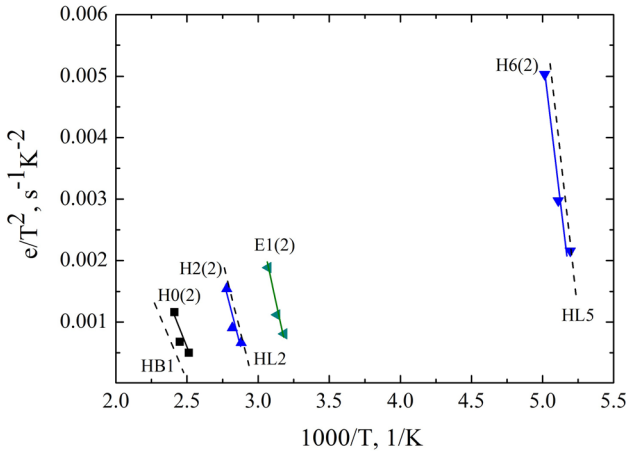

FIG. 7. Arrhenius temperature dependences of the thermal emission rates e of holes and electrons from deep traps in p^+–p^0–i–n^0–n^+ structures based on $In_xGa_{1-x}As/GaAs$. The dashed lines show the Arrhenius dependences for the traps identified in Ref. 10.

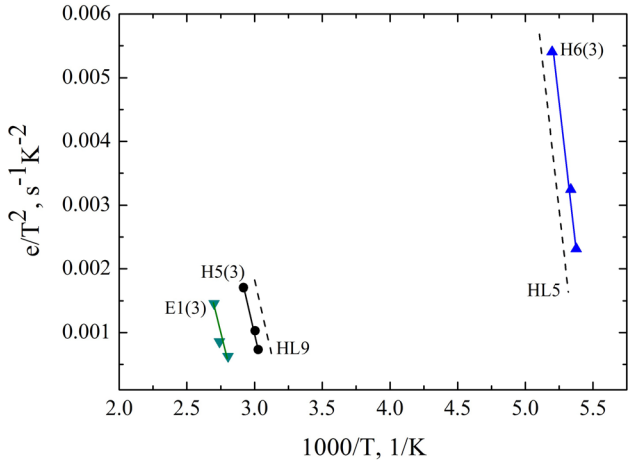

FIG. 9. Arrhenius temperature dependences of the thermal emission rates e of holes and electrons from deep traps in p^+–p^0–i–n^0–n^+ structures based on $GaAs_{1-y}Sb_y/GaAs$ layers. The dashed line shows the Arrhenius dependences for the traps identified in Ref. 10.

signal is given by the expression $\Delta C/C \approx (n_1L)/(2N_dW)$ for the n–type layer, and $\Delta C/C \approx (p_1L)/(2N_aW)$ for the p–type layer, where C is the capacitance of the SCR at a pulse voltage V_r at which the DLTS signal is measured, n_1 and p_1 are the surface densities of electrons or holes captured into localized states, L is the depth at which the spatial localization layer lies, and N_d and N_a are the concentrations of shallow donors and acceptors. Optical illumination may change the position of the Fermi level due to the recharging of deep-level defects in the nearest vicinity of these spatially localized states E1(2), E1(3), H1(2), and H1(3), which may favor a controlled metastable rise in their occupancy (n_1). The change in the amplitudes of E1(2), E1(3), H1(2), and H1(3) peaks in measurements of DLTS spectra of the InGaAs/GaAs and GaAsSb/GaAs p^+–p^0–i–n^0–n^+ heterostructures under optical illumination was observed experimentally. The changes in the amplitudes E1(2), E1(3) and H1(3) peaks in measurements of DLTS spectra under optical illumination

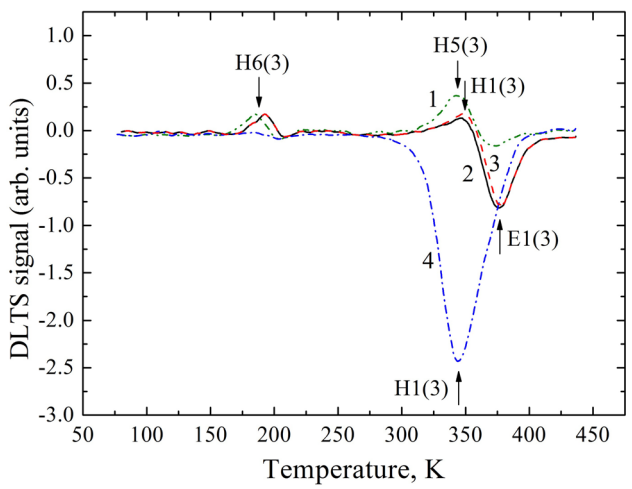

FIG. 8. DLTS spectra of a GaAsSb/GaAs p^+–p^0–i–n^0–n^+ diode, measured at a window rate of 200^{-1} s at (1) reverse bias voltage $V_r = -2.70$ V and filling pulse voltage $V_f = +0.50$ V, (2) $V_r = -2.70$ V and $V_f = -0.07$ V, in the dark, (3) $V_r = -2.70$ V and $V_f = -0.07$ V, under illumination, and (4) $V_r = +0.01$ V and $V_f = +0.5$ V.

are shown in Fig. 6(a) (curve 3) and Fig. 8 (curve 3). At the same time, the DLTS signal for defects distributed across the whole thickness of the semiconductor layer is determined by $\Delta C/C \approx N_t/(2N_d)$ and its amplitude grows with increasing concentration N_t of deep levels of the defect and with decreasing concentration N_d of shallow donors and is independent of illumination.[29,30] Thus, the change in DLTS spectra under illumination indicates that E1(2), E1(3), H1(2), and H1(3) peaks are related to spatially localized states. The DLTS spectra obtained at $V_r = -2.70$ V and $V_f = +0.50$ V for InGaAs/GaAs and GaAsSb/GaAs heterostructures [Fig. 6(b), curve 1, and Fig. 8, curve 1] demonstrated for each of the n^0 layers a single negative high-temperature DLTS peak associated with the electron emission from a deep donor trap. The thermal activation energies (E_t) and capture cross-sections (σ_n) of this DL trap were found from the Arrhenius dependences in Figs. 7 and 9 to be $E_t = 653$ meV and $\sigma_n = 1.06 \times 10^{-14}$ cm^2 for InGaAs/GaAs and $E_t = 683$ meV and $\sigma_n = 1.16 \times 10^{-14}$ cm^2 for GaAsSb/GaAs [E1(2) and E1(3) DLs from Table I]. The electron trap concentrations were, respectively, 3.35×10^{14} and 1.60×10^{14} cm^{-3}. These electron traps are close in parameters to ED1 DL observed in Refs. 17 and 18 and attributed to threading dislocations formed near the interfaces of InGaAs/GaAs and GaAsSb/GaAs heterostructures. No electron traps were manifested in the GaAs p^+–p^0–i–n^0–n^+ structure.

To reveal DL defects in the p^0 layers of the InGaAs/GaAs and GaAsSb/GaAs heterostructures, we measured DLTS spectra with $V_r = +0.01$ V and $V_f = +0.50$ V. For both the heterostructures, the DLTS spectra of the p^0 layer demonstrated a negative high-temperature peak, which was now associated with the emission of holes from a deep acceptor trap [Fig. 6(b), curve 2, and Fig. 8, curve 4]. This DL trap had the following parameters: $E_t = 774$ meV and $\sigma_p = 1.23 \times 10^{-13}$ cm^2 for InGaAs/GaAs and $E_t = 848$ meV and $\sigma_p = 2.73 \times 10^{-12}$ cm^2 for GaAsSb/GaAs [H1(2) and H1(3) DLs from Table I and Fig. 10]. The hole trap concentrations were, respectively, 3.80×10^{14} and 2.40×10^{14} cm^{-3}. When the DLTS spectrum of the InGaAs/GaAs heterostructure was

measured with $V_r = +0.01$ V and $V_f = +1.00$ V, the parameters of the high-temperature hole trap were found to be different at its unchanged concentration: $E_t = 845$ meV and $\sigma_p = 1.33 \times 10^{-12}$ cm^2 [H1*(2) from Table I and Fig. 10]. These parameters were found to be similar to the values determined for the hole trap in the GaAsSb/GaAs heterostructure. Comparison of the Arrhenius dependences for the DL hole traps (Fig. 10) found in the p^0 layers of three types of p^+–p^0–i–n^0–n^+ structures under study by the DLTS method shows that these defects are strongly different from those similar to HL2 formed in GaAs homoepitaxial layers. The hole traps H1(2), H1*(2), and H1(3) from Table I and Fig. 10 are similar to the HD3 trap described in Refs. 17 and 18. It was reported[17,18] that a hole trap HD3 with an activation energy of about 0.74 eV was observed in LPE-grown $GaAs_{1-x}Sb_x$ epitaxial layers, together with an ED1 electron trap. When DLTS spectra of the GaAsSb/GaAs p^+–p^0–i–n^0–n^+ heterostructure were measured with $V_r = +0.01$ V and $V_f = +0.5$ V under illumination, as this was also done for the E1(3) peak, we observed changes in the amplitude of H1(3) (Fig. 8, curve 3). It has been shown previously that this effect, associated with the optical illumination, is a characteristic indication of spatially localized deep states, represented in the given case by a deep state related to hole traps. Thus, this hole trap can be attributed to the interfacial states of misfit dislocations.

In our DLTS measurements of InGaAs/GaAs heterostructures, we observed a dependence of the thermal activation energy and capture cross-section of the acceptor-type dislocation traps on the filling pulse. This dependence may be associated with the existence of an energy band in the forbidden gap. The possibility that a band of this kind may exist was noted in Refs. 31–33 in which it was suggested to consider a dislocation as a 1D crystal. In addition, dislocations are characterized, as noted in Ref. 34, by large hole capture cross-sections, and just this we observed in a DLTS study of both the InGaAs/GaAs and GaAsSb/GaAs heterostructures.

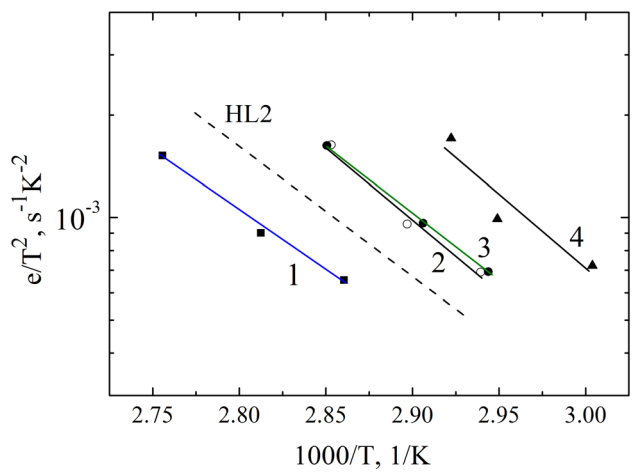

FIG. 10. Arrhenius temperature dependencies of the thermal emission rates e of holes from deep acceptor traps: (1) H1(1), (2) H1(2), (3) H1*(2), and (4) H1(3) in p^+–p^0–i–n^0–n^+ structures based on (1) homoepitaxial GaAs layers and heteroepitaxial (2 and 3) $In_xGa_{1-x}As$/GaAs, and (4) $GaAs_{1-y}Sb_y$/GaAs layers. The dashed line shows the Arrhenius dependence for the HL2 trap identified in Ref. 10.

For dislocation centers, the phonon coupling with the lattice becomes weaker, compared with point defects. Centers of this kind, with midgap levels, may be effective recombination centers with the equal number of partners from the valence and conduction bands.[34] If we assume in this case that the cross-section of electron capture to a neutral dislocation center differs only slightly from that of hole capture to a negatively charged center, it becomes possible to estimate the relaxation times of the nonequilibrium carrier concentration. It should be noted that the values of the basic parameters of the DL dislocation traps (thermal activation energies and concentrations) were determined above.

C. Estimated relaxation time of the nonequilibrium carrier concentration in diode structures

In the general form, the expressions relating the relaxation times of nonequilibrium carriers depend in a complicated way on the coefficients of electron and hole capture by the traps ($C_n = \sigma_n \times v_n$ and $C_p = \sigma_p \times v_p$, where v_n and v_p are the thermal velocity of electrons and holes) and on the level energies.[33,35] The effective recombination centers in the InGaAs/GaAs and GaAsSb/GaAs heterostructure layers are dislocation-related hole traps similar to HD3: H1(2) and H1(3) from Table I and Fig. 10. Therefore, we assume that the recombination rate of nonequilibrium carriers in the heteroepitaxial layers is determined by just these defects. If the conditions $N_t^0 \gg n_0 + n_1$ and $N_t^- \gg p_0 + p_1$ are satisfied (where N_t^0 is the equilibrium concentration of empty deep acceptor-type traps; N_t^-, equilibrium concentration deep acceptor traps filled by electrons; n_1 and p_1, electron and hole concentrations in, respectively, conduction and valence bands at which the Fermi level coincides with the DL energies (E_t); and n_0 and p_0, equilibrium electron and hole concentrations), the expressions for C_n and C_p can be simplified for deep acceptor levels at a low excitation level, high trap concentration, and low temperature of the crystal.[33,35] In this case, the expressions for the relaxation time of nonequilibrium carriers (τ_1 and τ_2) in the cases in which empty deep acceptor-type traps (τ_1) and those filled by electrons are involved (τ_2) are simplified to become[33,35]

$$\frac{1}{\tau_1} \cong C_n \times N_t^o, \quad \frac{1}{\tau_2} \cong C_p \times N_t^-. \tag{2}$$

Because it is quite probable that a double carrier injection occurs in the p^+–p^0–i–n^0–n^+ structures under study on applying a bias to the samples, we estimate the relaxation time of nonequilibrium carriers for both of these cases.

(i) Estimate of the relaxation time of nonequilibrium holes for an acceptor trap with a level situated in the upper half of the forbidden gap in the p^0 layer on the assumption that it is filled by electrons. For the InGaAs/GaAs heterostructure, we have the relaxation time $\tau_2 = 1.1 \times 10^{-10}$ s on taking into account that $E_t = 845$ meV, $\sigma_p = 1.33 \times 10^{-12}$ cm^2, $N_t^- = 3.80 \times 10^{14}$ cm^{-3}, and the average thermal velocity of holes in GaAs $v_p = 1.8 \times 10^7$ cm/s.[36] For the GaAsSb/GaAs heterostructure with $E_t = 848$ meV, $\sigma_p = 2.73 \times 10^{-12}$ cm^2, and $N_t^- = 2.40 \times 10^{14}$ cm^{-3}, the relaxation time $\tau_2 = 8.5 \times 10^{-11}$ s. Similar estimates made for the GaAs p^+–p^0–i–n^0–n^+ structure

in which a hole trap with $E_t = 695$ meV, $\sigma_p = 3.89 \times 10^{-15}$ cm^2, and $N_t^- = 1.60 \times 10^{13}$ cm^{-3} is an effective recombination center for the p^0 layer yielded a relaxation time $\tau_2 = 8.9 \times 10^{-7}$ s, which substantially exceeds the values for the InGaAs/GaAs and GaAsSb/GaAs heterostructures.

(ii) Estimate of the relaxation time of nonequilibrium electrons for the case in which empty deep acceptor-type traps situated in the upper half of the forbidden gap in the p^0 layer are involved. Assuming (on the basis of the arguments presented in Ref. 34) that the cross-section of electron capture to a neutral dislocation center, σ_n, may have a value of $\sim 10^{-13}$ cm^2 and taking into account that the electron thermal velocity in GaAs, $v_n = 4.4 \times 10^7$ cm/s,[36] we have that, according to Eq. (2), the relaxation time, τ_1, is $\sim 10^{-9}$ s (0.6×10^{-9} s and 0.95×10^{-9} s for the InGaAs and GaAsSb layers, respectively).

The effective lifetimes of nonequilibrium carriers in the base regions of the InGaAs/GaAs and GaAsSb/GaAs heterostructures were determined by the Lax[37] or Gossik[38] methods to be on the order of several nanoseconds,[1–3] in agreement with our estimates made on the assumption that the relaxation of nonequilibrium carriers is governed by acceptor-type dislocation centers.

IV. CONCLUSIONS

The C–V characteristics and DLTS spectra of p^+–p^0–i–n^0–n^+ diode structures based on lightly doped homoepitaxial GaAs layers having no misfit dislocations and heteroepitaxial InGaAs/GaAs and GaAsSb/GaAs layers with homogeneous networks of misfit dislocations, all grown by the LPE method at crystallization onset temperatures of 850 °C, were studied. It was found that the base regions of all three structures had the form of a graded p^0–i–n^0 junction with a free-carrier concentration in the i-type layer of $\sim 10^{13}$–10^{14} cm^{-3}. This made it possible to study the DLTS spectra for the p^0 and n^0 layers of p^0–i–n^0 structures at both negative and positive bias voltages V_r with different amplitudes. These measurements enabled the authors to identify HL2 and HL5 DL defects in the p^0 and n^0 GaAs epitaxial layers, which are well known for the LPE-grown GaAs.

Deep interfacial states were observed at the heterointerfaces of the p^+–p^0–i–n^0–n^+ InGaAs/GaAs and GaAsSb/GaAs heterostructures. These states are manifested under optical illumination at various measurement temperatures of the C–V characteristics of DLTS spectra. Measurements of DLTS spectra performed for these p^+–p^0–i–n^0–n^+ heterostructures revealed in the n^0 and p^0 layers electron (ED1) and hole (HD3) spatially localized traps attributed to, respectively, misfit dislocations and threading dislocations.

A dependence of the thermal activation energies and capture cross-sections of acceptor-type dislocation traps on the filling pulse was observed for InGaAs/GaAs heterostructures. This dependence can be attributed to the existence of an energy band in the forbidden gap.

The relaxation times of the nonequilibrium carrier concentration were estimated with the involvement of deep acceptor-type dislocation traps similar to HD3 (effective recombination centers in the samples under study) taken into account. These times were 1.1×10^{-10} s for InGaAs/GaAs heterostructures and 8.5×10^{-11} s for GaAsSb/GaAs heterostructures, which are substantially shorter than that for GaAs homostructures (8.9×10^{-7} s). These data correspond to the relaxation times of nonequilibrium carriers in the base layers of GaAs, InGaAs/GaAs, and GaAsSb/GaAs high-voltage power p-i-n diodes. This enables us to conclude that just deep acceptor-type dislocation traps similar to HD3 are responsible for the significant decrease in the relaxation time of nonequilibrium carriers in the base layers of InGaAs/GaAs and in GaAsSb/GaAs heterostructures with a network of misfit dislocations.

ACKNOWLEDGMENTS

This study was supported in part by the Russian Foundation for Basic Research (Research Project No. 16-08-00954-a).

[1]F. Y. Soldatenkov, V. G. Danilchenko, and V. I. Korolkov, Semiconductors **41**, 211 (2007).
[2]V. G. Danilchenko, V. I. Korolkov, and F. Y. Soldatenkov, Semiconductors **43**, 1055 (2009).
[3]V. A. Kozlov, F. Y. Soldatenkov, V. G. Danilchenko, V. I. Korolkov, and I. L. Shulpina, in *Proceedings of the 25th Advanced Semiconductor Manufacturing Conference (ASMC-2014), Saratoga Springs, USA, 19–21 May 2014*, pp. 139–144.
[4]V. Dudek, J. Kowalsky, and J. Lutz, in *Proceedings of the International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH), Denver, USA, 19–22 May 2014*, pp. 397–400.
[5]V. I. Brylevskiy, I. A. Smirnova, A. V. Rozhkov, P. N. Brunkov, P. B. Rodin, and I. V. Grekhov, IEEE Trans. Plasma Sci. **44**, 1941 (2016).
[6]V. G. Danilchenko, V. I. Korolkov, S. I. Ponomarev, and F. Y. Soldatenkov, Semiconductors **45**, 515 (2011).
[7]M. M. Sobolev, F. Y. Soldatenkov, and V. A. Kozlov, Semiconductors **50**, 924 (2016).
[8]M. M. Sobolev, P. N. Brunkov, S. G. Konnikov, M. N. Stepanova, V. G. Nikitin, V. P. Ulin, A. S. Dolbaya, T. D. Kamushadze, and R. Maisuradze, Sov. Phys. Semicond. **23**, 660 (1989).
[9]P. N. Brunkov, S. Gaibullaev, S. G. Konnikov, V. G. Nikitin, M. I. Papentsev, and M. M. Sobolev, Sov. Phys. Semicond. **25**, 205 (1991).
[10]A. Mitonneau, G. M. Martin, and A. Mircea, Electron. Lett. **13**, 666 (1977).
[11]L. S. Berman, V. G. Danilchenko, V. I. Korolkov, and F. Y. Soldatenkov, Semiconductors **34**, 541 (2000).
[12]G. M. Martin, A. Mitonneau, and A. Mircea, Electron. Lett. **13**, 191 (1977).
[13]V. A. Kaluchov and S. I. Chikichev, Phys. Status Solidi **88**, K59 (1985).
[14]A. Z. Li, H. K. Kim, J. C. Jeong, D. Wong, T. E. Schlesinger, and A. G. Milnes, J. Appl. Phys. **64**, 3497 (1988).
[15]K. Yamada and K. Wada, Inst. Phys. Conf. Ser. **106**, 153 (1989).
[16]B. H. Yang, Z. G. Wang, H. J. He, and L. Y. Lin, J. Cryst. Growth **103**, 371 (1990).
[17]O. Yastrubchak, T. Wosinski, A. Makosa, T. Figielski, S. Porowski, I. Grzegory, R. Czernecki, and P. Perlin, Eur. Phys. J.: Appl. Phys. **27**, 201 (2004).
[18]T. Wosiński, A. Makosa, and J. Raczyńska, Acta Phys. Pol. A **87**, 369 (1995).
[19]Z. I. Alferov, V. I. Korolkov, V. G. Nikitin, M. N. Stepanova, and D. N. Tret'yakov, Sov. Tech. Phys. Lett. **2**, 76 (1976).
[20]F. Y. Soldatenkov, V. P. Ulin, A. A. Yakovenko, O. M. Fedorova, S. G. Konnikov, and V. I. Korolkov, Tech. Phys. Lett. **25**, 852 (1999).
[21]D. K. Bowen and B. K. Tanner, *High Resolution X-Ray Diffractometry and Topography* (Taylor and Francis Ltd., London, 1998).
[22]I. L. Shul'pina and T. S. Argunova, J. Phys. D: Appl. Phys. **28**, A47 (1995).
[23]I. L. Shul'pina, V. V. Ratnikov, V. A. Kozlov, F. Y. Soldatenkov, and V. E. Voitovich, Tech. Phys. **59**, 1556 (2014).
[24]C. O. Thomas, D. Kahng, and R. C. Manz, J. Electrochem. Soc. **109**, 1055 (1962).

[25]E. S. Yang, J. Appl. Phys. **45**, 3801 (1974).
[26]J. P. Donnelly and A. G. Milnes, IEEE Trans. Electron Devices **14**, 63 (1967).
[27]M. M. Sobolev, A. V. Gittsovich, M. I. Papentsev, I. V. Kochnev, and B. S. Yavich, Sov. Phys. - Semicond. **26**, 985 (1992).
[28]D. V. Davydov, A. L. Zakgeim, F. M. Snegov, M. M. Sobolev, A. E. Chernyakov, A. S. Usikov, and N. M. Shmidt, Tech. Phys. Lett. **33**, 143 (2007).
[29]M. M. Sobolev, A. R. Kovsh, V. M. Ustinov, A. Y. Egorov, A. E. Zhukov, and Y. G. Musikhin, Semiconductors **33**, 157 (1999).
[30]M. M. Sobolev, A. R. Kovsh, V. V. Ustinov, A. Y. Egorov, A. E. Zhukov, and Y. G. Musikhin, J. Electron. Mater. **28**, 491 (1999).
[31]V. Kveder, M. Kittler, and W. Schröter, Phys. Rev. B **63**, 115208 (2001).
[32]Ł. Gelczuk, M. Dąbrowska-Szata, G. Jóźwiak, and D. Radziewicz, Phys. B: Condens. Matter **388**, 195 (2007).
[33]V. L. Bonch-Bruevich and S. G. Kalashnikov, *Physics of Semiconductors* (Nauka, Moscow, 1977).
[34]H. F. Matare, *Defect Electronics in Semiconductors* (Wiley-Interscience, NY, London, Sydney, Toronto, 1971).
[35]A. G. Milnes, *Deep Impurities in Semiconductors* (Wiley-Interscience Publication, John Wiley and Sons Inc., NY, London, Sydney, Toronto, 1973).
[36]*Handbook Series on Semiconductor Parameters Vol. 1*, edited by M. Levinstein, S. Rumyantsev, and M. Shur (World Scientific, 1996).
[37]B. Lax and S. F. Neustadter, J. Appl. Phys. **25**, 1148 (1954).
[38]B. R. Gossik, J. Appl. Phys. **27**, 905 (1956).