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Correlation between barrier inhomogeneities of 4H-SiC 1 A/600 V Schottky rectifiers and deep-level defects revealed by DLTS and Laplace DLTS

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ABSTRACT

Electrical properties of commercial silicon carbide (SiC) Schottky rectifiers are investigated through the measurement and analysis of the forward current–voltage (*I–V*) and reverse capacitance–voltage (*C–V*) characteristics in a large temperature range. Some of devices show distinct discrepancies in specific ranges of their electrical characteristics, especially the excess current dominates at voltage <1 V and temperature <300 K. Standard deep level transient spectroscopy (DLTS) revealed the presence of a single deep-level defect with activation energy of about 0.3 eV, exhibiting the features characteristic for extended defects (e.g. dislocations), such as logarithmic capture kinetics. Furthermore, high-resolution Laplace DLTS showed that this deep level consists actually of three closely spaced levels with activation energies ranging from about 0.26 eV to 0.29 eV. A strong correlation between these two techniques implies that the revealed trap level is due to extended defects surrounded by point traps or clusters of defects. On the basis of obtained specific features of the deep-level defect, it was proposed that this defect is arguably responsible for the observed Schottky barrier inhomogeneities.

1. Introduction

Silicon carbide (SiC) is a well-known wide bandgap semiconductor material due to its extraordinary properties such as high reverse breakdown voltage, high electron velocity, high thermal conductivity and small dielectric constant [1]. As a result of these properties the most attractive applications of SiC-based devices are in the area of high power, high frequency and high temperature conditions [1,2], under which conventional semiconductors (Si, GaAs) cannot adequately work. The SiC Schottky barrier diodes (SBDs) are easy to fabricate and show high-switching-speed capabilities due to the absence of minority carrier injection effects observed in p–n junction devices [2]. Furthermore, wide bandgap and high breakdown field permit the operation of SiC Schottky diodes at much higher voltages (kV) and current densities (kA/cm^2) than it is possible with Si-based Schottky diodes.

There are many polytypes of SiC, but the technologically important ones are 3C-, 6H- and 4H-SiC, with the bandgap of 2.3 eV, 3.0 eV and 3.2 eV, respectively. 3C-SiC is the only form of SiC with a cubic crystal structure, while 4H- and 6H-SiC are only two of many possible SiC polytypes with hexagonal crystal structure [1]. In general, 3C-SiC is known as a low-temperature polytype, while 4H- and 6H-SiC are high temperature polytypes.

Despite the fact that in the last decade the SiC market is developing rapidly, there are still unresolved problems, especially dealing with the influence of electrically active defects on the performance and electrical characteristics of SiC-based devices. Besides the shallow dopants like nitrogen (N), aluminum (Al), phosphorus (P) or boron (B), which mainly govern the conductivity of SiC material, many intrinsic and extrinsic defect centers are usually present in SiC giving rise to energetically deep levels in the bandgap. These deep-level defects can act either as trapping centers for electrons and holes or recombination-generation centers limiting a lifetime of free charge carriers.

Since the early stage of SiC Schottky rectifier development, it has been observed that reverse leakage current density of large area diodes was always much higher (typically about 2 orders of magnitude) than expected by the thermionic emission theory [3,4] and the excess current was often observed in the forward characteristics at a low voltage, showing the anomalous behavior [5,6]. Non-ideal Schottky characteristics described above can be

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well explained using a Schottky barrier height (SBH) inhomogeneity concept, considered as two SBDs with different SBHs combined in parallel, according to the model given in [5,7]. In this model, the excess current at a low forward voltage results from low Schottky barrier height patches in localized regions, surrounded by a large area contact with higher SBH. It was also shown that lowering of SBH can lead to increasing of the reverse leakage current [3,7]. In order to eliminate the SBH inhomogeneities, many explanations were given so far, but most of them indicated the presence of defects, which result in lowering of the SBH in localized regions and thus indirectly influence on direct and reverse characteristics of SiC diodes [3–13]. The investigated defects include crystallographic defects (dislocations, micropipes, grain boundaries, stacking faults, etc.) and surface defects (carrots, comets, half-moons, growth pits, scratches, etc.) [4,7,10–12]. The micropipes are well documented defects in the literature that severely degrade the performance of SiC power devices [1,2]. It is also known that high density of screw dislocations can significantly deteriorate reverse characteristics at a critical value of the electric field limiting the breakdown voltage [4]. Until now, a great deal of efforts have been made to identify the source defects of SBH inhomogeneities. None of the known defects were claimed as a main factor controlling electrical properties of SiC. Therefore, the study of electrically active defects is of fundamental interest for the design and development of high quality modern SiC devices.

The deep level transient spectroscopy (DLTS) is widely used and sensitive method for studying deep-level defects in semiconductors [14]. It provides many electrical parameters of deep levels, such as activation energy (i.e. deep energy level position in the bandgap), capture cross section and defect concentration. Moreover, high-resolution Laplace DLTS technique (LDLTS) [15] is used for studying closely spaced deep levels with similar properties, because of its significantly improved spectral resolution compared to the standard DLTS.

In this paper, commercially available SiC Schottky rectifiers were studied by means of current–voltage (I–V) and capacitance–voltage (C–V) characteristics as well as DLTS and Laplace DLTS techniques. The motivation of this work were results reported in Ref. [13]. It was discovered that some of the commercially available SiC Schottky rectifiers exhibit distinct discrepancies in specific ranges of the forward and reverse I–V characteristics. Especially, different values of reverse leakage currents occurred in most of the tested diodes, although these values were within the range guaranteed by a producer. According to literature data and own considerations, it was initially proposed [12] that such an extraordinary behavior may be evoked by the presence of electrically active deep-level defects in the bandgap. In order to verify this hypothesis we performed thorough I–V and C–V measurements in a wide range of temperature and tried to relate the observed discrepancies with deep-level defects existing in these devices.

2. Experiment

In this work, 4H-SiC Schottky barrier rectifiers produced by Cree Inc. were studied. The rectifiers CSD01060 (1 A, 600 V) have typical packages TO-220 and are used in switch mode power supplies, power factor correction and motor drives [16]. Current–voltage (I–V) and capacitance–voltage (C–V) characteristics were measured within 80–380 K range by means of Keithley 2601A I–V sourcemeter and Boonton 7200 capacitance bridge, respectively. Standard DLTS measurements were performed within 77–400 K range with the use of DLS-82E spectrometer (SemiTrap), equipped with 1 MHz capacitance bridge meter and lock-in type integrator. For the high-resolution LDLTS measurements, samples were mounted in liquid nitrogen Janis VPF-475 cryostat, equipped with Lakeshore 331 temperature controller. Next, Boonton 7200 C–V meter was used for recording the capacitance transients, which were than analyzed by special numerical algorithms [15].

It is worth noting that the most confusing problem of this research is the fact that we do not know practically the area and kind of metallization used for preparation of the Schottky contact, as well as the type and doping level of the SiC material that are essential for proper analysis of electrical characteristics and calculation of diode parameters. The only true information is that 4H-SiC polytype was used for preparation of the investigated Schottky rectifiers (information received from personal communication with CREE Inc. representatives). Nevertheless, assuming a diameter of the contact area equal to 0.5 mm^2, which in our opinion is close to the typical values for SiC Schottky diodes, we obtained electrical parameters (especially SBHs) close to the observed typically for many 4H-SiC Schottky barrier rectifiers with different metallization's [4–7,9,10,17].

3. Results and discussion

3.1. I–V–T and C–V–T measurements

Rectifying properties of four commercial 4H-SiC Schottky barrier diodes were studied by means of I–V method [13]. Standard approach, based on the thermionic emission theory was used to describe a current flow across the Schottky barrier interface [18]:

$$I = I_S\left[\exp\left(\frac{q(V - IR_S)}{nkT}\right) - 1\right], \tag{1}$$

with the saturation current I_S defined by

$$I_S = AA^*T^2\exp\left(-\frac{q\Phi_{b0}}{kT}\right), \tag{2}$$

where n denotes the ideality factor, R_S is the series resistance, q is the elementary electron charge, k is the Boltzmann constant, T is the temperature, A denotes the diode area, Φ_{b0} is the Schottky barrier height and A^* is the Richardson's constant, previously calculated and equal to about 146 A/cm^2 K^2 for 4H-SiC [17].

The investigated diodes are intended to work with a maximum forward current of 1 A and maximum reverse voltage of 600 V. Measured characteristics of four diodes at a room temperature were generally in accordance with the characteristics presented in product data sheets [16]. In a forward current range, where the diodes are intended to work, that is for current from 1 mA to 1 A, the I–V characteristics of all measured diodes were almost identical. The calculated series resistance at a nominal current of 1 A is about of 0.45 Ω and the ideality factor ranges from about 1.12 to about 1.17. However, there were very different values of reverse leakage currents, although these values were within the range guaranteed by the producer. On the other hand, the room temperature forward I–V characteristics below the voltage of 0.75 V and the reverse I–V characteristics below the voltage of 600 V showed large discrepancies, as reported in [13]. Fig. 1 shows representative I–V characteristics in a semi-logarithmic plot for one of the studied diodes at several temperatures within the range from 80 K up to 380 K and with the step of 20 K. As one can recognize, the presented characteristics are not ideal, because they show one or even two distinct "knees". At higher temperatures (>300 K) the characteristics are similar as those for ideal Schottky rectifiers, yielding the value of the ideality factor (extracted from the linear part of the plot) close to one, indicating that thermionic emission mechanism is responsible for the current transport through the Schottky junction. According to the thermionic emission theory [18] of Schottky barrier diode for a forward bias, the log(I)–lin(V) plot should be a straight line extending over many orders up to a

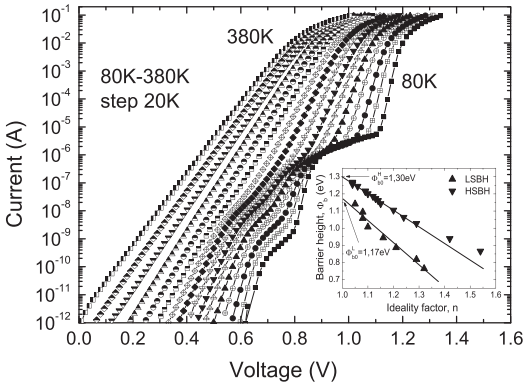

Fig. 1. Temperature dependence of forward *I–V* characteristics for 4H-SiC rectifier (CSD1060, CREE), showing barrier height inhomogeneities at lower temperatures, with the so-called "two SBH" behavior. The inset shows the plots of LSBH and HSBH as a function of ideality factor determined at various temperatures.

high current density where the series resistance causes its bending. However, at lower temperatures (<300 K) some excess current (i.e. an additional current over the typical current of Schottky junction yielding linear log(I)–lin(V) region) is observed below a forward bias voltage of about 1 V (Fig. 1). Furthermore, for only a few characteristics measured at even lower temperatures (<200 K) another "knee" is observed, what can indicate that some additional excess current can flow at very low temperatures and for very low forward voltage (<0.7 V) in the studied Schottky diodes.

As reported previously for 4H-SiC, the diodes which display the excess current at low voltages can be still analysed using thermionic emission theory as two independent Schottky barriers in parallel [3,5,7], according to the equation:

$$I = I_S^L\left[\exp\left(\frac{q(V-IR_S^L)}{n^L kT}\right)-1\right]+I_S^H\left[\exp\left(\frac{q(V-IR_S^H)}{n^H kT}\right)-1\right], \qquad (3)$$

where the superscripts L and H account for low and high Schottky barrier height (SBH) regions. In this model local low-barrier regions distributed within the diode area are surrounded by a high-barrier region. At low forward voltages (<1 V), the current flows primarily over the low SBH (LSBH) region, whereas at higher forward voltages the current flow over the high SBH (HSBH) becomes dominating, since the current flow through the low-barrier patches is limited by their area (due to the higher current density and very high series resistance). Therefore, the HSBH is responsible for a linear region of the *I–V* characteristics observed in Fig. 1 for the near-ideal Schottky rectifier, i.e. above 300 K in the range of 10^{-12}–10^{-2} A, and below 300 K in the range above 10^{-5} A. On the other hand, the LSBH is responsible for a linear region observed at a low voltage and at lower temperatures (<300 K). The additional excess current observed for lower temperatures is presumably related to the effect of shunt resistance [19], which is also considered to be another evidence for the inhomogeneities of SBH due to the presence of defects at biased metal–semiconductor interface. Similar behavior of anomalous *I–V* characteristics, i.e. different mechanisms of current flow in the forward direction was recently observed in non-commercial 4H-SiC Schottky diodes [20].

The calculated SBHs as a function of the ideality factors for different temperatures obtained by *I–V* technique were shown additionally in the inset of Fig. 1. The SBH values were obtained assuming that a contact area is equal to about 0.5 mm^2. A linear trend is observed over a wide temperature range which is regarded as the indication of laterally nonuniform SBHs [21]. Similar linear correlations have been observed in the past for 4H-SiC [5,7,22] and other materials [21]. Finally, the extrapolation of experimental barrier heights vs ideality factors plot to n = 1 (as expected for ideal case) gives an effective HSBH value of about 1.30 eV and LSBH value of about 1.17 eV, respectively.

It is worth noting that temperature dependence of SBHs and ideality factors can be also interpreted in the framework of the common model proposed by Tung et al. [23,24] who presented a general theory on the real metal–semiconductor (MS) interface explaining most of the experimentally observed anomalies of Schottky rectifiers, such as greater-than-one ideality factor as well as temperature dependence of the SBH and the ideality factor. The model considers a barrier at a metal–semiconductor interface as consisting of locally nonuniform but interacting patches of different barrier heights embedded in a background of a uniform barrier height. According to this model, local neighboring regions of lower SBH are considered as interacting patches with Gaussian distribution surrounded by regions of higher SBH, for which internal interactions and especially modifications in the potential profile at the boundary between these two regions cannot be neglected. In fact, since a small region of LSBH is surrounded by a large area contact with HSBH, it is expected that potential distribution beneath a region of LSBH would be influenced by the region of HSBH and this would result in a pinch-off of the potential for the LSBH region [23]. However, application of this model to the studied diodes did not provide a good fit to the experimental data in this case. It could result from different formation mechanisms of SB, which are dependent on the local specifics of the MS interface in the studied diodes. As an alternative, the above mentioned model of two non-interacting, independent diodes of discrete barrier height was assumed.

Furthermore, *C–V* characteristics were measured for the studied diodes in the same temperature range. Typical *C–V* results of the same SiC rectifier measured within the same temperature range are shown in Fig. 2. Capacitance–voltage data were also used to extract the Schottky barrier height and doping concentration by fitting a straight line to C^{-2} plotted as a function of voltage, using the standard equation [17]:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s\varepsilon_0 N_D A^2}(V_i - V_R), \qquad (4)$$

and the barrier height is given by:

$$\Phi_{b0} = V_{bi} + V_n; \quad V_{bi} = V_i + \frac{kT}{q}, \quad V_n = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \qquad (5)$$

where N_D denotes the doping concentration, V_i is the diffusion potential (the intercept along a voltage axis), V_{bi} is the built-in volt-

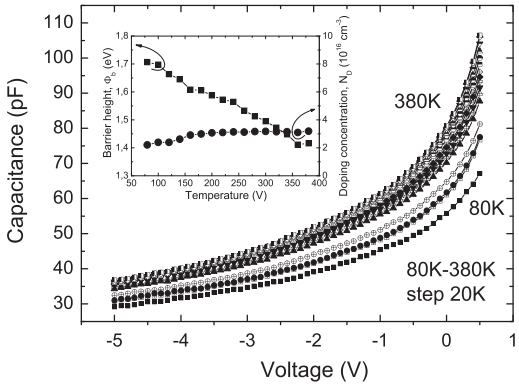

Fig. 2. Temperature dependence of reverse *C–V* characteristics for 4H-SiC Schottky rectifier (CSD1060, CREE). The inset shows variation of barrier heights and doping concentrations measured by *C–V* at different temperatures.

age, V_R is the reverse voltage, V_n is the potential difference between the Fermi level position and conduction band edge, N_C is the effective density of states in the conduction band, ε_s is the static dielectric constant and ε_0 is the permittivity of free space.

The semiconductor doping concentration and built-in voltage (and then the value of the barrier height, determined from Eq. (5)) can be calculated from the slope and intercept of $1/C^2$ vs V_R plot, respectively. In the inset of Fig. 2 the two plots of extracted SBHs and effective doping concentrations as a function of temperature are shown. Assuming a contact area value equal to about 0.5 mm^2 the doping concentration was estimated at the level of about 3.0×10^{16} cm^{-3}, which was almost uniform for the whole measured temperature range. The small drop of the doping concentration profile was only observed for the lowest temperatures (below 150 K). On the other hand, the values of the extracted SBH by means of *C–V* technique increase significantly with decreasing the temperature. The observed changes in the SBH and doping density are evidently related to the effect of defects, existing around the contact area near the metal–semiconductor interface. Finally, extrapolation of the *C–V* derived values of the SBH vs the ideality factors obtained from *I–V* measurements to $n = 1$ gives an effective SBH value of about 1.4 eV.

The value of SBH obtained from *C–V* measurements is remarkable higher than the extrapolated HSBH derived from the forward *I–V* characteristics (1.3 eV). There are many studies showing discrepancies between the barrier height values obtained by *I–V* and *C–V* measurements, the latter being typically larger of about 0.1–0.3 eV for e.g. 4H-SiC [25]. It follows from the fact, that *I–V* characteristics depend strongly on the homogeneity of the interface and are affected by a slight field-induced barrier lowering (the zero-bias SBH). On the other hand, the *C–V* extracted values approach the flat-band SBH and are not significantly affected by interfacial lateral non-homogeneities in SBH [23,24]. Furthermore, the effect of acceptor-like interfacial defects on the SBH extracted from CV measurements is also generally known. The presence of interfacial region with such defects can increase the built-in voltage and result in an apparently higher value of SBH (if the influence of defects in such an interfacial region is neglected) [18]. The discrepancy between *C–V* and *I–V* derived SBH may be also explained by the presence of Schottky barrier height inhomogeneities [26]. By using a model with the presence of two Schottky barriers in parallel it can be shown also that the barrier height obtained by the *C–V* method is in general close to the highest barrier height, whereas a barrier height obtained by the *I–V* method is in general close to the lowest one [26]. Finally, the *C–V* derived barrier heights are generally virtually independent on the ideality factor and local barrier height inhomogeneities and therefore they are much more consistent for the individual diode [7].

As it was mentioned before, considerable evidences exist for defect-driven Schottky barrier inhomogeneities in SiC materials [3–12]. Discrete surface defects localized at local barrier patches of metal–semiconductor interface are generally regarded to be responsible for the observed non-ideal Schottky diode characteristics. A locally reduced barrier height can result from the excess current flowing through local defective paths instead of evenly distributed over the entire Schottky area. Therefore, individual extended defects, such as dislocations, micropipes, stacking faults, extended defects decorated with point defects or clusters of defects concentrated near the metal–semiconductor interface are predominatingly taken into consideration [3–12]. In order to clarify, which of these defects are responsible for the observed barrier height inhomogeneities and to obtain their fine characterization (i.e. electrical parameters, localization in the structure, point or extended character, etc.) DLTS and Laplace DLTS measurements were performed.

3.2. DLTS and LDLTS measurements

The existence of local defective current paths, causing the observed distortion of the *I–V–T* characteristics at lower temperatures and low voltage (Fig. 1) can be attributed to electrically active deep-level defects located at its neighborhood, which should be observed by means of standard DLTS technique. Indeed, Fig. 3 presents DLTS temperature spectra of the studied diode, measured for a quiescent reverse bias voltage (U_R) of −6 V, forward filling-pulse height (U_P) of 0 V, filling-pulse width (t_p) of 50 μs and different lock-in frequencies (f_0), ranging from 2.5 Hz up to 1 kHz. Only one, single dominant deep-level trap, called by us T1, was revealed at around 150 K on the DLTS spectra. It is worth noting that a similar trap was also observed for all studied diodes and the detail results can be found in our previous paper [27].

The electrical parameters of the T1 trap, i.e. thermal activation energy ($E_a = E_{C,V} \pm E_T$, denoting a deep-level position in the band-gap) and apparent capture cross section ($\sigma_{n,p}$) were determined by measuring the evolution of the DLTS-peak position with the temperature for several lock-in frequencies. The temperature dependence of thermal emission rates (so-called the Arrhenius plot) made possible to calculate the parameters of the T1 trap. The activation energy and the apparent capture cross sections were then deduced from the least-square fitting procedure of the data presented in the inset of Fig. 3. They are equal to about 0.3 eV and 7.4×10^{-15} cm^2, respectively.

The next step of our investigations was to distinguish the point or extended character of the observed deep-level trap T1. The important feature of DLTS-line that is commonly considered as a fingerprint of the extended defect (e.g. dislocation), is the so-called logarithmic capture law [28], i.e. a logarithmic dependence of the kinetics for majority charge carriers captured in trap states. This phenomenon is usually explained in terms of a barrier model of recombination processes via dislocations. In this model, the capture rate of free charge carriers, limited by the Coulombic barrier of a repulsive electrostatic potential built up at the defect, is proportional to a number of electrons already captured at the dislocation line [28,29]. Such a dependence can occur when the trap levels are arranged in a linear array, interacting between themselves, and not randomly distributed in the whole crystal. In DLTS, logarithmic capture law is exploited as a principal argument for discriminating between isolated point defects and extended ones, which can be expressed as a linear dependence of the DLTS-peak amplitude on the logarithm of the filling-pulse duration time. This effect has been already observed for dislocations themselves or dislocations decorated with point defects in many semiconductors, for example

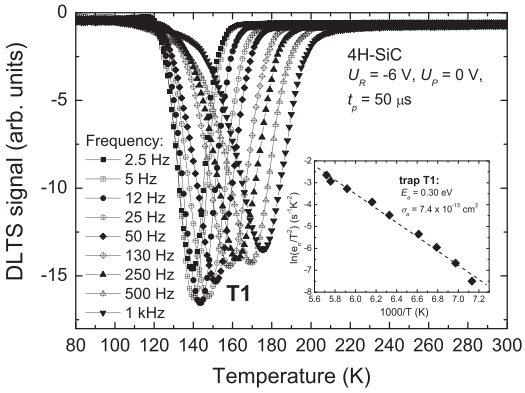

Fig. 3. Standard DLTS spectra measured for different lock-in frequencies (f_0) and for quiescent other parameters: $U_R = -6$ V, $U_p = 0$ V, and $t_p = 50$ μs. The inset shows the Arrhenius plot for a deep-level trap T1 revealed in the 4H-SiC rectifier (CSD1060, CREE).

Si [30], SiGe [31], GaAs [32] and also SiC [8]. On the contrary, isolated point defects or impurities typically reveal exponential capture kinetics (the exponential capture law). This dependence can be also investigated by DLTS. In this case, a characteristic distinct saturation of the DLTS peak amplitude for long filling-pulse durations is observed [29]. Such a behavior is typical of non-interacting point defects. As the DLTS amplitude is proportional to the defect concentration, the time at which saturation is reached describes the situation when no more free charge carriers are captured in defect states. Therefore, it determines the trap concentration (N_T).

In Fig. 4, the DLTS spectra collected at 2.5 Hz and bias conditions: $U_R = -6$ V, $U_P = 0$ V, are shown for different widths of filling-pulse times ranging from 20 μs to 20 ms (the highest value is limited by technical limitations of our DLTS system). It is noticeable that for the trap T1, the DLTS signal increases consistently with increasing filling-pulse width. As it is shown in the inset of Fig. 5, a linear trend is observed in semi-logarithmic plot of DLTS-peak vs filling-pulse time, indicating logarithmic capture kinetics for the trap T1. On the basis of these results we can confirm the presence of interacting trap levels characteristic for extended defects.

In order to investigate, where the observed deep-level trap T1 is primarily located, a depth concentration profile was measured exploiting the Double Correlation DLTS (DDLTS) technique [33], with the use of two filling pulses differing by 0.5 V and quiescent reverse voltage of −16 V. The obtained results, i.e. deep-level trap concentration vs distance from the surface is presented in Fig. 5. As one can see, the concentration profile of T1 trap, obtained for a lock-in frequency of 10 Hz and fixed filling-pulse time equal to 5 ms, increases monotonically up to the surface, indicating that the revealed deep-level defect should be evidently concentrated near the surface, i.e. at metal–semiconductor interface. Determination of the maximum concentration of the trap was not possible, because of the lack of saturation of the corresponding DLTS-peak amplitude due to logarithmic capture kinetics (see in the inset of Fig. 4), as it was minutely mentioned above. Nevertheless, the maximum concentration of the trap T1, measured at about 180 nm below the surface, i.e. for the filling pulse bias of 0 V (which was limited by the width of the depletion region) is equal to about 1.3×10^{14} cm^{-3}.

It is known, that spatially extended defects (e.g. dislocations) are associated with a large number of deep electronic states in the bandgap whose properties can vary depending upon the level of their decoration by point defects (e.g. impurities) [34]. They usually form deep-lying one-dimensional energy bands rather than isolated energy levels, typically attributed to point defects. The

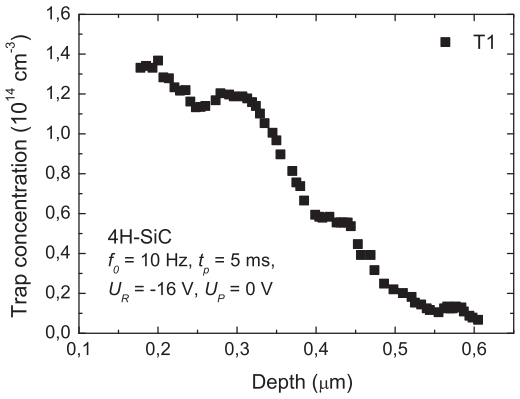

Fig. 5. The concentration depth profile of the trap T1 as a function of the distance from the surface, i.e. metal–semiconductor interface.

Laplace transform DLTS technique (LDLTS) [15], due to its significantly improved spectral resolution compared to a standard DLTS technique, enable us to resolve closely spaced deep energy levels of defects. This technique is relayed on the measurements of capacitance transients due to carrier emission at a fixed temperature and their analysis by special mathematical algorithms to extract the emission rates of the transient [15]. The temperature is chosen on the basis of the standard DLTS temperature spectrum where the deep-level defect-related peak is observed. If the transient is fully exponential (as for a single point defect), only one peak will be visible in the LDLTS spectrum. On the other hand, if the transient is non-exponential (as typical for extended defects) or multi-exponential (as for few closely spaced point traps) the spectra will usually show several peaks, as it was shown for extended defects in silicon [34].

The representative high-resolution LDLTS spectrum, recorded at 164 K, for the trap T1 is presented in Fig. 6. This spectrum, taken for similar experimental conditions as those used for standard DLTS measurements, consists of three sharp peaks, labeled T1A, T1B and T1C, with different emission rates. It confirms that the peak attributed to the trap T1 observed by standard DLTS is not caused by the isolated point defect, because it has more than one closely spaced energy level contributing to the overall carrier emission, observed by standard DLTS [34]. At least three different trap levels, with activation energies of about 0.265 eV, 0.281 eV and 0.291 eV (according to the Arrhenius plots shown in the inset of Fig. 6) were revealed in the LDLTS spectrum, respectively. In LDLTS analysis, the Arrhenius plots were obtained by measuring the emission rate

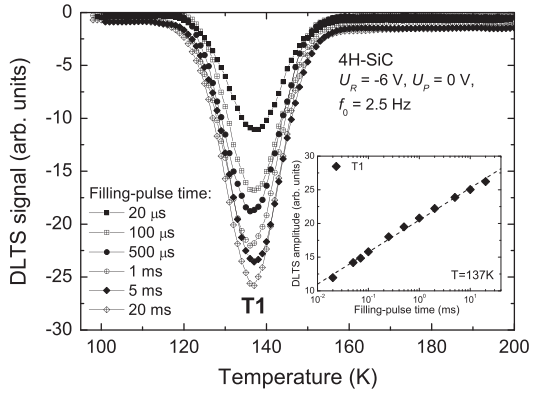

Fig. 4. DLTS spectra measured for different durations of the filling-pulse. The other parameters were: $f_0 = 25$ Hz, $U_R = -6$ V, $U_P = 0$ V. The inset shows DLTS peak amplitude of the trap T1 vs filling-pulse time showing logarithmic dependence characteristic for extended defects.

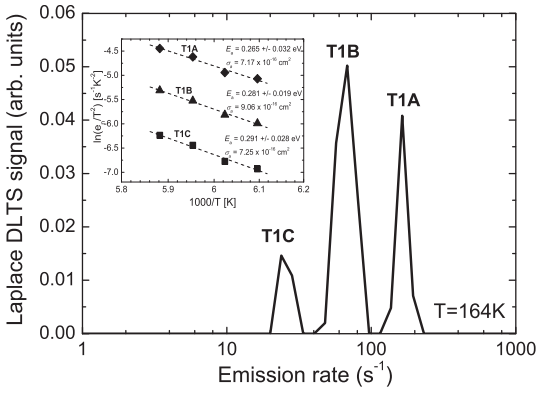

Fig. 6. High-resolution Laplace DLTS spectrum of 4H-SiC Schottky rectifier recorded at 164 K for similar experimental parameters as those of standard DLTS. The inset shows Arrhenius plots of three closely-spaced deep levels T1A, T1B and T1C revealed for the trap T1.

peak position at various fixed temperatures around the position of trap T1 in the standard DLTS spectrum, shown in Fig. 3.

The results obtained from DLTS and LDLTS suggest that the single trap T1 is due to either continuous distributions of states or to group of closely spaced discrete energy levels. Thus we can attribute this trap to the emission from extended defects (e.g. dislocations) probably decorated with point defects [7,8]. However, there is another explanation related to clusters of point defects with similar activation energies and high local concentrations. According to [35], such defects can locally "pin" the Fermi level at lower than ideal values and result in the excess current at low forward voltages. Moreover, the observed LSBH values should be at least of the same magnitude as activation energy of the defect causing such barrier height inhomogeneities. Our investigations are somewhat in contradiction with this model, because the mean activation energy of the trap T1 equal to about 0.3 eV is far lower than LSBH value of 1.17 eV as obtained from *I–V* measurements. Nevertheless, all the revealed features, such as logarithmic kinetics of carrier capture process, near surface location and multi-level character of the deep trap T1 indicate that this defect can be partially responsible for the observed barrier height inhomogeneities in 4H-SiC Schottky rectifiers. The more, so that only this trap was revealed in the studied commercial diodes. The possible existence of another defect with activation energy close to the LSBH value which can contribute to the observed inhomogeneities and thus can be in agreement with the Fermi level pinning model, requires DLTS measurements at higher temperatures >450 K that is beyond technical capabilities of our DLTS system.

4. Conclusions

In summary, some of the tested commercially available 4H-SiC Schottky rectifiers show distinct discrepancies of the forward *I–V* characteristics for low voltage (<1 V) at different temperatures. The discrepancies involve the excess current in a low forward voltage, ideality factors greater than one and anomalously low *I–V* barrier heights, which decrease linearly with increasing of ideality factor. These non-idealities of Schottky rectifiers were related to Schottky barrier height (SBH) inhomogeneities due to the existence of local defective patches with low SBH, surrounded by large area contact regions with high SBH. The calculated low and high SBHs from *I–V* measurements were equal to about 1.17 eV and 1.3 eV, respectively. Moreover, the effective SBH value of about 1.4 eV, as obtained from *C–V* measurements, was remarkably higher than those obtained from *I–V* measurements. The discrepancy between *C–V* and *I–V* analysis was also related to the presence of SBH inhomogeneities.

In order to verify the existence of electrically active defects under the Schottky contact which can be responsible for the observed SBH inhomogeneities DLTS measurements were performed. Only one deep-level defect was revealed with an activation energy of about 0.3 eV in the measured temperature range. The measurements of capture kinetics for the related trap, revealed a linear increase of the DLTS-peak amplitude on increasing of the filling pulse time in a semi-logarithmic plot. Moreover, according to the depth concentration profile of this trap, it appears evident that the trap T1 should be located near the surface, i.e. metal–semiconductor interface. Finally, high-resolution Laplace DLTS measurements showed additionally that trap T1 is due to either continuous distributions of states or to group of closely spaced discrete energy levels with different activation energies, varying from about 0.265 eV to 0.291 eV. The revealed specific features indicate together that this trap can be attributed to extended defects (e.g. dislocations) probably decorated with point defects or clusters of point defects with similar activation energies, which are partially responsible for the observed barrier height inhomogeneities in 4H-SiC Schottky rectifiers.

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