The Influence of Parasitic Effects on Injection-Level-Dependent Lifetime Data

Florence W. Chen, Jeffrey E. Cotter, Malcolm D. Abbott, Tsu-Tsung A. Li, and Kate C. Fisher

***Abstract*—A circuit simulation approach is employed to investigate the influence of various parasitic effects on injection-level-dependent lifetime data of samples containing p-n junctions. Simulations of the influence of shunts, localized recombination, edge recombination, and a combination of these on lifetime data are presented. The simulation shows that the nature of the parasitic effects can be qualitatively identified due to their different lifetime behaviors at various injection levels. It is demonstrated that the parasitic effects start to dominate the lifetime data at injection levels $< 10^{15}$ cm^{-3}, and the lifetime behavior can look similar to Shockley–Read–Hall recombination in some cases. A range of case studies with experimental data and data fitting are presented. The case studies show that parasitic effects can interfere with lifetime-based experiments. In some cases, the understanding of the influence of parasitic effects leads to a reinterpretation of the lifetime behavior of the test devices.**

***Index Terms*—Circuit simulation, photoconductivity, photoluminescence (PL), photovoltaic cells.**

I. Introduction

ANALYSIS of injection-level-dependent lifetime (IDL) data is an important characterization technique for the development and manufacture of crystalline silicon solar cells. IDL data provide information about recombination in the bulk, emitter, and surface regions of silicon wafers [1]–[3] and are used in numerous applications. For example, IDL data have been used to study carrier trapping by defects in Czochralski silicon and multicrystalline silicon [4]–[6], to characterize process-induced dislocations from laser damage [7], to understand diffusion-induced and stress-induced misfit dislocations [8], [9], and to optimize surface passivation techniques [10]–[16]. By relating the excess carrier concentration to the junction voltage, it is possible to convert IDL data into implied voltage curves [4]. This allows the terminal voltage of devices to be predicted without requiring a finished solar cell structure.

Traditionally, IDL data have been measured using techniques based on the measurement of photoconductance (PC), such as transient PC decay [17] or quasi-steady-state PC [4], [18], [19]. Since the techniques are contactless, they can be applied to partially finished solar cells, allowing process monitoring at most stages of fabrication. However, the range of injection levels over which the effective lifetime can be accurately determined is limited due to artifacts in the measurements caused by depletion region modulation (DRM) [20], [21] and trapping [22]. These effects limit the range of available injection levels in IDL data. For example, for 1-$\Omega \cdot$ cm wafers with a diffused junction, the IDL data are limited to injection levels $> 10^{14}$ cm^{-3}. Recently, a technique based on quasi-steady-state photoluminescence (PL) was introduced as an alternative to measure the IDL of silicon wafers [23]. The PL technique is able to measure reliable IDL data to injection levels as low as $> 10^{9}$ cm^{-3} [23], without the influence of DRM or trapping [24]. At these low injection levels, a variety of complex lifetime behaviors caused by various parasitic effects dominates the data. The analysis of such IDL data is the subject of this paper.

To model IDL data at injection levels below $\sim 10^{15}$ cm^{-3}, it is necessary to take a circuit-based approach due to the complex nature of the IDL curves. We use a freeware student version of PSPICE9.1 [25] to provide quick numerical solutions to complex nonlinear circuits that model the IDL data of samples with p-n junctions, which exhibit parasitic effects. An equivalent circuit model of such samples is developed to generate simulated IDL data. By adding components to this model, it is possible to investigate the influence of a range of parasitic effects such as junction shunting and isolated points of high recombination. We show that different parasitic effects dominate at different injection levels and result in different characteristic shapes in IDL data. This allows detection and identification of the nature of the parasitic effects present in partially finished solar cells. Furthermore, it is shown that the IDL curves of samples dominated by parasitic effects such as localized recombination and edge recombination have a similar characteristic shape as the ones dominated by Shockley–Read–Hall (SRH) recombination.

II. Theory

Most parasitic effects have complex and nonlinear lifetime behaviors that require numerical solutions. To address this, we use a circuit simulator, namely PSPICE, as a tool to simulate the IDL curves. The equivalent circuit model comprises a main diode that simulates the idealized case, a current source to simulate the optical generation, and additional circuit elements to simulate the parasitic effects.

For single-sided test structures that have a p-n junction on one side only, the recombination current of the main diode,

Manuscript received June 19, 2007; revised August 1, 2007. This work was supported by the Australian Research Council under the Centre of Excellence Scheme. The review of this paper was arranged by Editor M. J. Kumar.

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Digital Object Identifier 10.1109/TED.2007.906970

which is expressed in terms of the commonly used diode parameters, is given by (assuming an n-type base layer)

$$J_r = \frac{q \cdot W}{\tau_h} \cdot \Delta p + \frac{J_{0d}}{n_i^2} \cdot \Delta p \cdot (\Delta p + N_D) \tag{1}$$

where q is the electron charge, τ_h is the minority carrier lifetime in the base layer, W is the base width (and essentially the wafer thickness), J_{0d} is the total recombination current density flowing into the diffused regions, n_i is the intrinsic carrier concentration, N_D is the base layer doping level, and Δp is the minority carrier concentration in the base layer.

The voltage V across the main diode is related to the excess minority carrier population Δp at the respective depletion region edge by the standard expression that accounts for the possibility of high injection conditions in the base region, i.e.,

$$\Delta p = \frac{N_D}{2}\left[\sqrt{1 + 4 \cdot \frac{n_i^2}{N_D^2} \cdot \left(\exp\left(\frac{qV}{kT}\right) - 1\right)} - 1\right]. \tag{2}$$

Together, (1) and (2) comprise a model of a single-sided sample with narrow base and a p-n junction that remains in low injection in the emitter, a structure that is typical of many lifetime test structures, but in a form that is convenient for a PSPICE simulation. The parameters of the test device are modeled in PSPICE using (1) and (2), which are programmed into a PSPICE "GVALUE" transconductance circuit element.

The generation current density is given by

$$J_g = q \cdot W \cdot G$$

where G is the optical generation rate. In a typical simulation, the generation current J_g is varied over several orders of magnitude to simulate the conditions of a PC or PL test, and voltage data V are collected.

Parasitic effects are modeled by adding additional circuit elements to the main circuit at the appropriate location. A deep scratch on the front surface, for example, might be modeled with a resistor, diode, or other circuit elements or combinations of elements, across the main diode terminals.

Data from a circuit simulation (specifically V and J_g) are converted into an IDL plot using (2) to determine Δp. The standard PC/PL assumption that optical generation G is equal to the total recombination in the main diode R is also used, allowing the inverse effective lifetime $1/\tau_{\text{eff}}$ to be calculated, i.e.,

$$\frac{1}{\tau_{\text{eff}}} \equiv \frac{R}{\Delta p} = \frac{J_g}{\Delta p \cdot q \cdot W}. \tag{3}$$

This assumption implies that all of the recombination occurs in the main diode. However, this is a poor assumption in cases where the parasitic effects dominate the test device's PC/PL response, because there is an appreciable number of carriers flowing through the parasitic elements. Nevertheless, making the assumption here allows us to replicate the IDL behavior resulting from standard PC/PL computations. Also, in the case of simulated PC IDL curves, the DRM effect is included in the calculations according to the equations outlined in [20].

In test devices where there is a p-n junction on both sides of the sample, the Ebers–Moll equivalent circuit [26] can be used to describe the total recombination current density of the front junction and the rear junction. The point of developing the Ebers–Moll model and deploying a circuit-based analysis is to emulate the asymmetrical case of minority carrier population at the front and rear p-n junction ($\Delta p_f \neq \Delta p_r$), which can occur, for example, when a sample is illuminated or diffused differently on one side compared to the other, and to emulate complex nonlinear parasitic effects, which can also affect the test device asymmetrically.

Since the base layer is now connected to a p-n junction on either side, J_r is now composed of two equations, each containing three current density components describing each of the junctions. These can be written as

$$J_{r\_\text{front}} \approx \left(\frac{q \cdot D_h}{W} + \frac{1}{3} \cdot \frac{q \cdot W}{\tau_h}\right) \cdot \Delta p_f + \frac{J_{0d}}{n_i^2} \cdot \Delta p_f \cdot (\Delta p_f + N_D) - \left(\frac{q \cdot D_h}{W} - \frac{1}{6} \cdot \frac{q \cdot W}{\tau_h}\right) \cdot \Delta p_r \tag{4.1}$$

$$J_{r\_\text{rear}} \approx \left(\frac{q \cdot D_h}{W} + \frac{1}{3} \cdot \frac{q \cdot W}{\tau_h}\right) \cdot \Delta p_r + \frac{J_{0d}}{n_i^2} \cdot \Delta p_r (\Delta p_r + N_D) - \left(\frac{q \cdot D_h}{W} - \frac{1}{6} \cdot \frac{q \cdot W}{\tau_h}\right) \cdot \Delta p_f \tag{4.2}$$

where D_h is the minority carrier hole diffusivity in the base layer, and Δp_f and Δp_r are the minority carrier hole populations at the edges of the front and rear p-n junctions, respectively.

The first term in each of (4.1) and (4.2) represents recombination current density in the base layer. The second term represents recombination in the diffused layer, and the third term represents current injected by the adjacent p-n junction that is transported across the base layer and collected by the p-n junction.

Together, (4.1) and (4.2) describe the implied current density–voltage (J–V) characteristics of the device containing a p-n junction at the front and at the rear in a form that is convenient for PSPICE simulation. In the general case of $\Delta p_f \neq \Delta p_r$, the excess minority carrier concentration is not uniform in the base. The narrow-base assumption, however, implies that the excess carrier populations Δp_f and Δp_r decrease linearly away from their respective depletion region edges to zero at the opposite depletion region edges, as they are collected by the opposite junction. Superimposing the minority carrier populations associated with the front and rear junctions and integrating the recombination over the width of the base region lead to the following expression for the effective lifetime:

$$\frac{1}{\tau_{\text{eff}}} = \frac{R_{\text{tot}}}{\overline{\Delta p}} = \frac{J_{r\_\text{front}} + J_{r\_\text{rear}}}{\overline{\Delta p} \cdot q \cdot W} = \frac{J_{g\_\text{front}} + J_{g\_\text{rear}}}{\overline{\Delta p} \cdot q \cdot W} \tag{5}$$

where $\overline{\Delta p} = (\Delta p_f + \Delta p_r)/2$.

Incidentally, summing equations for J_{r_front} and J_{r_rear} for the symmetrical case of $\Delta p_f = \Delta p_r$ and transforming using (5) lead to the familiar inverse lifetime expression of Kane and Swanson [17], i.e.,

$$\frac{1}{\tau_{\mathrm{eff}}} = \frac{1}{\tau_{\mathrm{bulk}}} + \frac{2 \cdot J_{0d}}{q \cdot W \cdot n_i^2} \cdot (\Delta p_n + N_D)\,. \tag{6}$$

III. Influence of Parasitic Effects on Lifetime Curves

We have observed a wide variety of physical defects and their influence on PC and PL lifetime data, including scratched surfaces, cracked wafers, chipped edges, and edge–junction and edge–bulk recombinations. Such parasitic effects can interfere with lifetime-based experiments and, in some cases, degrade the performance of high-efficiency solar cells. In most cases, these parasitic effects can be detected by PC and PL techniques in the low injection region of the IDL data. Since different parasitic effects result in different characteristic shapes in the IDL data, the nature of the parasitic effect can be identified.

A. Influence of Junction Shunt

Junction shunting of solar cells occurs when there is a conductive path across the p-n junction, providing an alternative path for carriers that would otherwise be injected through the main diode. The minority carriers collected by the junction return through this conductor as majority carriers, instead of being reinjected as minority carriers through the main diode. Therefore, the minority carrier population is effectively reduced, and this can be detected by lifetime measurements.

Junction shunting can be modeled in circuit simulations by adding a resistor R_{sh} in parallel to the main diode, as shown in Fig. 1. The simulated IDL data obtained from this circuit for various values of R_{sh} are shown in Fig. 2. At injection levels $< 10^{14}$ cm^{-3}, the shunt current becomes significant when compared to the recombination current of the main diode and dominates the IDL data depending on the magnitude of the shunt resistor.

B. Influence of Localized Recombination

Localized recombination is a common parasitic effect in solar cells. It occurs when local regions of high recombination are present in parallel with the main diode. Sometimes, these localized recombination centers are partially resistively isolated from the main diode. Several physical effects have been shown to cause resistively isolated localized recombination [27], including edge recombination, damaged pyramid tips, and Schottky contacts, for example. A test device affected by localized recombination can be modeled using the circuit shown in Fig. 3. In this case, the localized recombination is modeled by a series-connected resistor R_L and a diode that has an ideality factor n_L of 1.0. The severity of the localized recombination can be modeled by varying the saturation current density of the parasitic diode, i.e., J_{0L}.

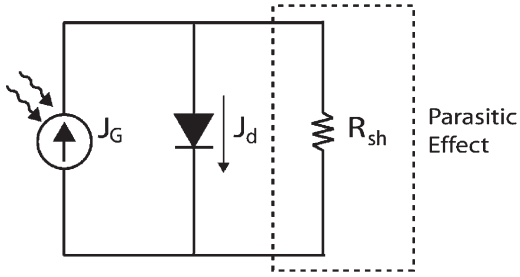

Fig. 1. Equivalent circuit model for junction shunt.

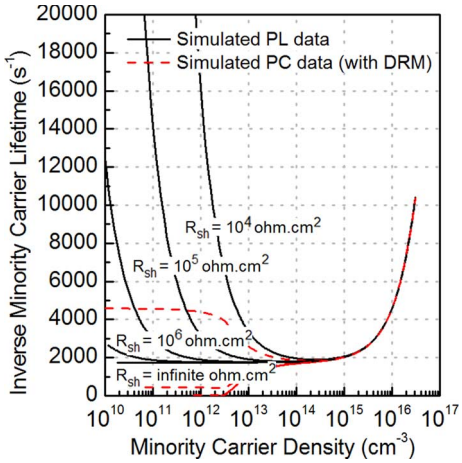

Fig. 2. Simulations of the influence of a junction shunt on IDL curves. The solid and dashed lines represent simulated PL and PC IDL data, respectively.

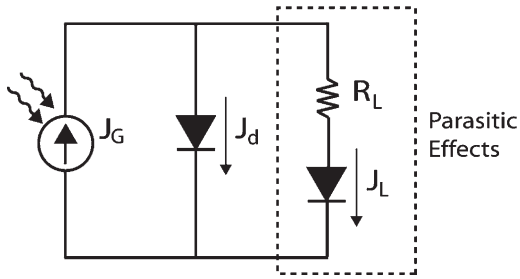

Fig. 3. Equivalent circuit to represent a test device affected by localized recombination.

Simulations of the influence of J_{0L} and R_L on IDL data are shown in Figs. 4 and 5, respectively. The other model parameters are fixed at $J_{0d} = 100$ fA/cm^2, $\tau_{\mathrm{bulk}} = 300$ μs, $R_L = 100\ \Omega \cdot \mathrm{cm}^2$ (for Fig. 4), and $J_{0L} = 500$ fA/cm^2 (for Fig. 5). Again, the parasitic localized recombination dominates the IDL data at injection levels below 10^{14} cm^{-3}. Notably, the shapes of the IDL curves look very similar to those affected by SRH recombination; however, no reasonable parameters of the SRH recombination provide an equivalent shape. In our experience, test samples dominated by localized recombination cannot be satisfactorily fitted with SRH parameters alone.

C. Influence of Edge Recombination

Another common parasitic effect that can affect lifetime test device, particularly small-area test structures, as well as completed solar cells, is edge recombination. Two types

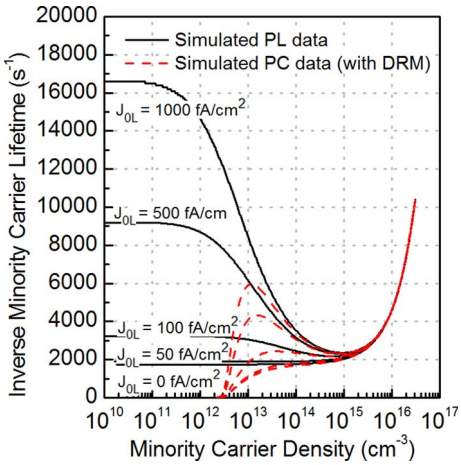

Fig. 4. Simulations of the influence of localized recombination on IDL curves (influence of J_{0L}). The solid and dashed lines represent simulated PL and PC IDL data, respectively.

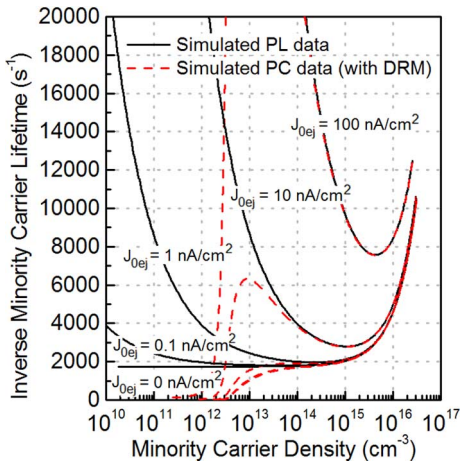

Fig. 6. Simulations of the influence of edge–junction recombination on IDL curves (influence of J_{0ej}). The solid and dashed lines represent simulated PL and PC IDL data, respectively.

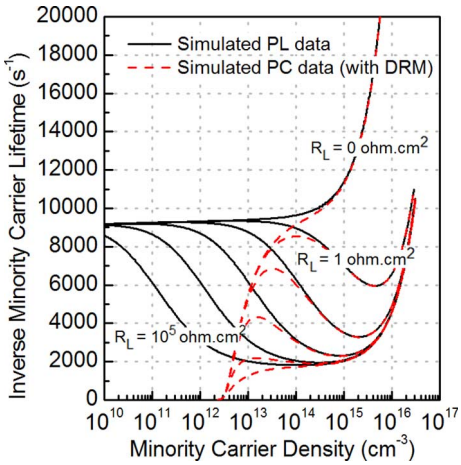

Fig. 5. Simulations of the influence of R_L (10^5, 10^4, 10^3, 10^2, 1, and 0 $\Omega \cdot$ cm^2). The solid and dashed lines represent simulated PL and PC IDL data, respectively.

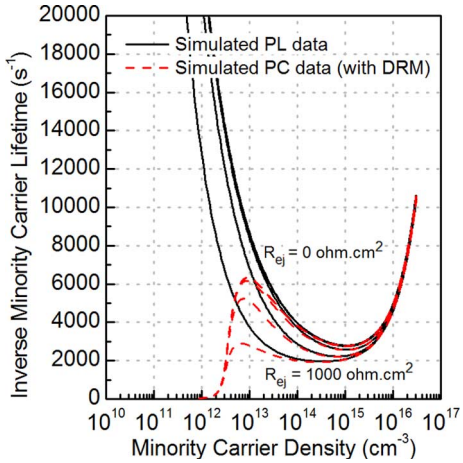

Fig. 7. Simulations of the influence of R_{ej} (10^3, 10^2, 1, and 0 $\Omega \cdot$ cm^2). The solid and dashed lines represent simulated PL and PC IDL data, respectively.

of edge recombination can dominate IDL data. Edge–bulk recombination J_{0eb} denotes recombination where the quasi-neutral regions of the device intersect the solar cell's edge, and edge–junction recombination J_{0ej} denotes recombination where the space–charge regions intersect the solar cell's edge. Edge–bulk and edge–junction recombinations can be modeled using the same equivalent circuit that models localized recombination, but with different circuit element parameters. For example, an ideality factor of 1.0 and 2.0 for the parasitic diode should be used to model edge–bulk and edge–junction recombinations, respectively. A resistor R_{ej} that is series connected with the parasitic diode may be added to represent the internal resistive path along the emitter [27]. As both edge–bulk recombination and localized recombination can be represented by the same circuit/circuit components, other analysis methods or characterization techniques are required to separate the two parasitic effects.

The influence of edge–junction recombination on IDL data is illustrated in Figs. 6 and 7. The severity of recombination at the edge is simulated by varying the saturation current density of the parasitic diode. The other parameters are fixed at $J_{0d} =$ 100 fA/cm^2, $\tau_{\rm bulk} = 300$ μs, $R_{0ej} = 0$ $\Omega \cdot$ cm^2 (for Fig. 6), and $J_{0ej} = 0.1$ nA/cm^2 (for Fig. 7). It should be noted that the influence of R_{ej} on IDL data is dependent on the magnitude of J_{0ej}—it only becomes significant if the edge–junction recombination is severe.

D. Combination of Parasitic Effects

In practice, it is rare for only one type of parasitic effect to be present in test device structures. Simulated IDL data of a test device that is affected by a combination of localized recombination and edge–junction recombination are shown in Fig. 8. The equivalent circuit used for the simulation is shown in Fig. 9. The influence of the two effects on IDL data is evident in the plot. Since different parasitic effects dominate at different injection levels, a qualitative analysis can be performed to determine the nature of the various parasitic effects when more than one is present. For data sets such as

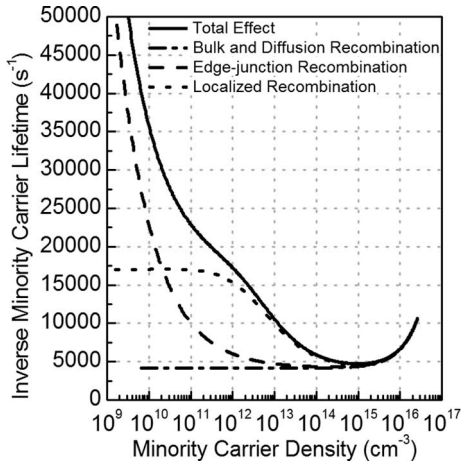

Fig. 8. Simulated PL data showing the influence of a combination of parasitic effects. $J_{0d} = 100$ fA/cm^2, $\tau_{\text{bulk}} = 0.3$ ms, $J_{0L} = 1000$ fA/cm^2, $R_L = 100\,\Omega \cdot \text{cm}^2$, and $J_{0ej} = 1$ nA/cm^2.

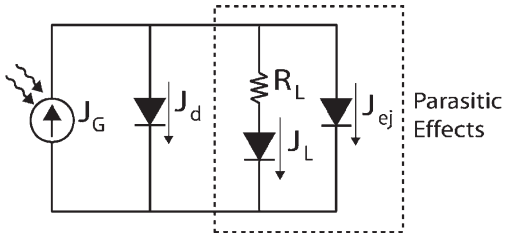

Fig. 9. Equivalent circuit used to model a combination of various parasitic effects.

these, it is necessary to use circuit simulation, which is fast and flexible, whereas an analytical solution is not possible.

IV. Case Studies With Experimental Results

A range of case studies where parasitic effects can interfere with lifetime-based process development is presented here. In cases where the experimental test structure is well designed and carefully constructed, lumped parameters quantifying the parasitic effects can be extracted, as demonstrated in [28]. This quantification can be useful for process design and optimization. In other cases, qualitative information can provide insight into the nature of parasitic effects dominating device performance.

Unless otherwise stated, all the wafers used in the experiments presented in this paper are high-lifetime, n-type, float-zoned (FZ), 1-$\Omega \cdot$ cm silicon that have been etched in sodium hydroxide (NaOH) to remove the saw-damaged surface layer. A combination of quasi-steady-state PL and PC measurements is carried out to obtain IDL data over a wide range of injection levels. For PL measurements, the test device is placed on top of a PL sensor, which detects and converts the PL emission into an excess carrier concentration and, combined with the generation rate, into an effective lifetime [23]. PC measurements are performed using a Sinton bridge that measures excess sheet conductance, which is converted into excess carrier concentration and effective lifetime [18]. In both cases, an 810-nm light-emitting diode array is used as the light excitation source to

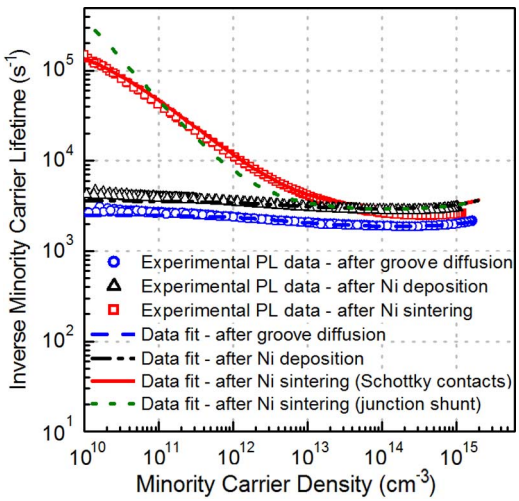

Fig. 10. Log–log graph of the experimental and circuit simulation fit of IDL data of the sample after each processing step. The experimental data are obtained by the PL technique.

generate carriers. The reflectance at 810 nm of all test devices, which is required to calibrate the absolute generation rate, is measured with a Cary 500 spectrophotometer. Self-consistent calibration [29] was employed for all measurements. The PL and PC measurements presented here were done separately but immediately after each other.

A. Schottky Contact Electrodes

Metallization is one of the most important steps in solar cell fabrication. In some cases, Schottky contacts may form if the metal–semiconductor contacts are not properly designed or constructed (e.g., if the underlying semiconductor is too lowly doped or if the metal contacts are not sintered at the correct temperature). These factors can cause the metal to spike through the emitter diffusion and contact the base of the solar cell, resulting in Schottky contacts [30]. In this situation, the equivalent circuit shown in Fig. 3 with a large J_{0L} can be used to describe the behavior of the Schottky contacts, as proposed in [27].

Several samples with an oxide-passivated, 100-Ω/sq boron emitter at the front and an oxide-passivated, 100-Ω/sq phosphorus diffusion at the rear of the samples were prepared. A well-passivated isolation trench was formed to isolate the emitter from the physical edges. A set of groove lines approximately 30 μm deep and approximately 2.7 cm long was then scribed inside the passivated square isolation trench, followed by a weak NaOH etch to remove the slag and laser damage in the grooves. A light phosphorus diffusion was performed in the groove lines, resulting in a diffusion profile that is known to produce Schottky contacts. A layer of nickel was deposited in the groove lines by electroless plating at 90 °C to 92 °C for 10 min and sintered at 300 °C for 10 min in N_2 ambient. PL measurements were made after each processing step. The IDL curves of a sample after each step are shown in Fig. 10.

Circuit simulation was performed to fit the IDL curves after each processing step, and the parameters used are summarized in Table I. In all cases, the data could be fitted with

TABLE I
PARAMETERS USED FOR THE SIMULATION FOR EACH STEP

Step	τ_{bulk} (ms)	J_{0d} (fA/cm^2)	R_L (Ω.cm^2)	J_{0L} (fA/cm^2)
Groove diffusion	1.20	50	2500	40
Ni deposition	1.20	100	2500	40
Ni sintering	1.20	100	2500	11500

the equivalent circuit that represents localized recombination (see Fig. 3), with a relatively small J_{0L} (40 fA/cm^2), up until the metal sintering step. This indicates that some small localized recombination is already present in our test structure before the metal was sintered. After the metal was sintered, the effective lifetime at injection level $> 10^{14}$ cm^{-3} decreased slightly, whereas the effective lifetime at lower injection levels decreased dramatically. A large value for J_{0L} was needed in the circuit simulation to fit the IDL data, indicating the presence of Schottky contacts.

It is worth noting that the data could not be modeled satisfactorily when the equivalent circuit of junction shunt was used. The best data fit using the junction shunt model is also shown in Fig. 10, with $R_{\rm sh} = 25$ kΩ, $\tau_{\rm bulk} = 1.2$ ms, and $J_{0d} = 100$ fA/cm^2. This experiment highlights the importance of analyzing a wide range of injection levels to obtain a more complete understanding of the nature of the parasitic effect. In this case, Schottky contact formation may not be obvious if the lifetime of the sample is only monitored at a single injection level, e.g., at 10^{15} cm^{-3}. It also demonstrates how circuit simulation can be useful in differentiating the nature of parasitic effect that is present in the test device.

B. Silicon Nitride Passivation

Silicon nitride (SiN) is widely used as a passivation layer and for antireflection coating in both industrial and laboratory solar cells. IDL measurements are commonly used to determine the surface passivation quality of SiN film. Typically, a SiN film is deposited on both sides of a high-quality silicon wafer, and the surface recombination velocity (SRV) can be extracted from the IDL data made on this device. It is common to report and compare the passivation quality based on the effective lifetime or the SRV extracted from a single injection level, often at one injection level in the range of $\sim 10^{14}$–10^{15} cm^{-3} of the IDL data. We demonstrate that parasitic effects can interfere with lifetime-based experiments of this nature, and in some cases, the IDL data at injection level $\sim 10^{14}$–10^{15} cm^{-3} are influenced by the parasitic effects. Furthermore, we show that parasitic effects can also have an influence on the lifetime behavior of charge-induced p-n junctions.

1) SiN-Passivated Boron-Diffused Surfaces: Boron-diffused surfaces play an important role as the emitter in n-type solar cells. Traditionally, boron emitters are passivated by thermal oxide. Recently, there is an increasing interest in using SiN to passivate boron emitters. This is because SiN can be deposited at low temperature and has optical properties that are well suited for antireflection coating purposes.

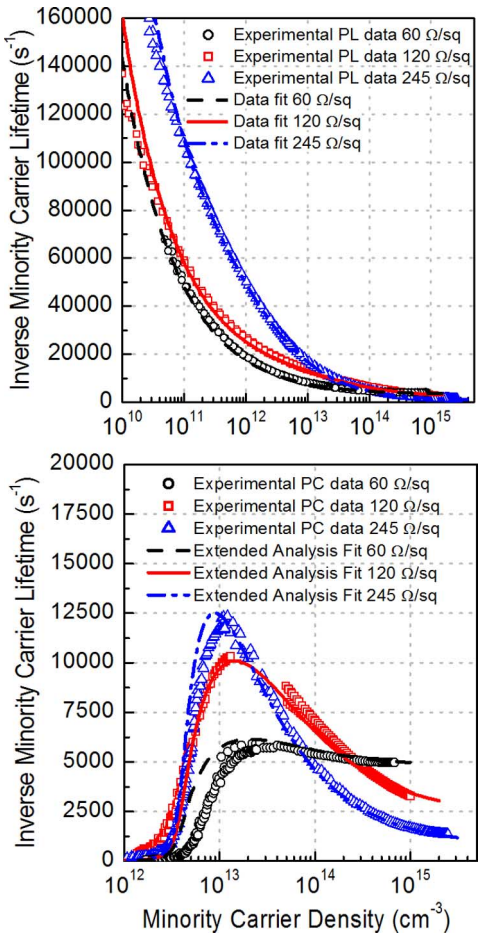

Fig. 11. Experimental IDL data and the extended analysis fit of three different SiN-passivated boron-diffused samples measured by (top) PL and (bottom) PC.

The IDL data obtained from PL and PC measurements made on three test devices that have SiN-passivated boron-diffused surfaces are shown in Fig. 11. The samples are identical, including the type of silicon nitride film ($n = 2.35$, 70 nm thick) used for passivation and the annealing environment, with the exception of the boron diffusion strengths (60, 120, and 245 Ω/sq). However, the IDL data of the three samples are strikingly different because they are affected by different parasitic effects.

Circuit simulations using the circuit shown in Fig. 9 and the parameters listed in Table II were performed for each sample, and a good fit of the measured IDL data was achieved for all three samples. The simulations suggest that various degrees of localized recombination and edge–junction recombination are present in all three samples. It is worth noting that the influence of parasitic effects on IDL data obtained from PC measurements is not always obvious. For example, J_{0d} is proportionally high when compared to J_{0L} in the sample that has a 60-Ω/sq boron emitter. As a result, the characteristic shape of localized recombination in the inverse lifetime curve is not as obvious as the other two samples.

TABLE II
PARAMETERS USED FOR THE SIMULATION FOR EACH CASE

Sample	τ_{bulk} (ms)	J_{0d} per side (fA/cm^2)	R_L (Ω.cm^2)	J_{0L} (fA/cm^2)	J_{0ej} (nA/cm^2)
60 Ω/□	0.5	150	100	10	0.10
120 Ω/□	0.5	8	35	8	0.10
245 Ω/□	2.2	5	120	50	0.16

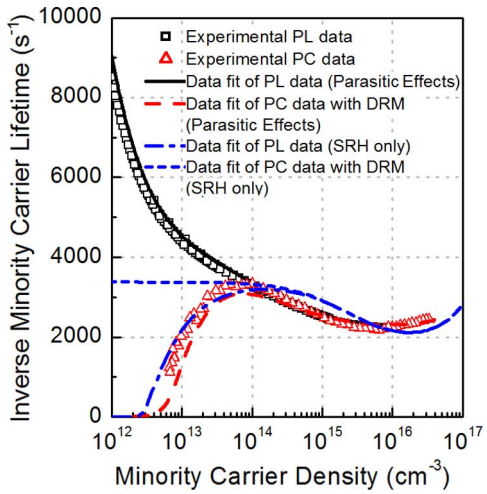

Fig. 12. Experimental IDL data of a sample containing SiN on both sides of a p-type silicon wafer. The modeled IDL data are also included ($J_{0d} = 4.75$ fA/cm^2, $\tau_{\rm bulk} = 0.48$ ms, $J_{0L} = 65$ fA/cm^2, $R_L = 30\ \Omega \cdot$ cm^2, and $J_{0ej} = 0.1$ nA/cm^2).

2) SiN-Induced p-n Junction: When SiN is deposited on a p-type wafer, the positive fixed charges in the film induce an n-type inversion layer at the Si–SiN interface, forming an induced p-n junction. The IDL data of a p-type, 1-Ω · cm, FZ silicon wafer coated on both sides with a typical plasma-enhanced chemical vapor deposition SiN film is shown in Fig. 12. The shape of the curve obtained by PC measurements suggests that the sample is affected by SRH recombination; however, no fit could be achieved for any reasonable combination of SRH parameters alone. A much better fit of the IDL data is achieved using a combination of circuit elements that represent localized recombination and edge–junction recombination, as shown in Fig. 12. This is plausible because it is known that SiN has many pinholes that can act like sources of localized recombination. The component of edge–junction recombination is not entirely expected due to the use of a poorly designed substrate holder design in the SiN deposition system [31]. However, we do not completely rule out the presence of SRH recombination in the sample. Instead, the circuit simulation merely suggests that the sample is dominated by the presence of the parasitic effects.

C. Furnace Cleanliness Monitoring

Furnace cleanliness is crucial to fabricating high-efficiency solar cells. One common method to monitor the cleanliness of a furnace is to perform diffusion and oxidation on test samples in the furnace of interest and analyze the IDL data to determine if there is any degradation in the bulk.

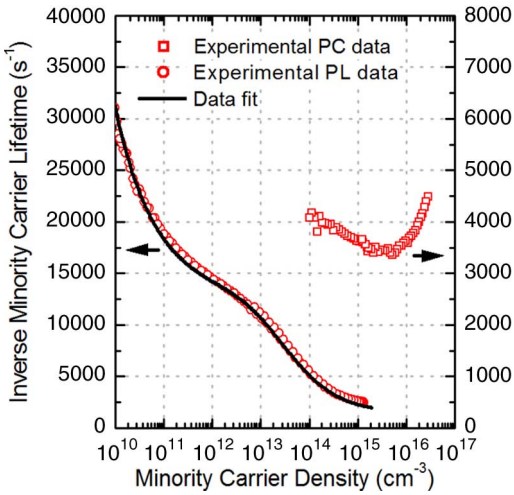

Fig. 13. PL and PC IDL data of a test device used to monitor the cleanliness of a furnace, showing the complex lifetime behavior at low injection levels. The circuit simulation fit of the data is also included in the graph ($\tau_{\rm bulk} = 1$ ms, $J_{0d} = 20$ fA/cm^2, $R_L = 25\ \Omega \cdot$ cm^2, $J_{0L} = 430$ fA/cm^2, and $J_{0ej} = 0.7$ nA/cm^2).

The IDL data of an FZ, 1-Ω · cm, p-type sample used for furnace cleanliness monitoring is shown in Fig. 13. Phosphorus diffusion and oxidation were performed, and the IDL data were measured by the PC method, as shown in Fig. 13. The low injection lifetime behavior in the PC IDL data is often attributed to SRH recombination, which leads to the conclusion of bulk contamination by impurities in the furnace. However, a PL lifetime measurement of the same sample shows a more complex lifetime behavior at injection levels $< 10^{14}$ cm^{-3}, where the SRH theory alone cannot explain the complex behavior.

The shape of the complex lifetime behavior looks similar to the simulated IDL curve presented in Section III-D, and hence, a qualitative conclusion can be drawn on the nature of the parasitic effects: a combination of localized recombination and edge–junction recombination. Curve fitting confirms the nature of the parasitic effects, with a good fit being achieved across a wide range of injection levels using the equivalent circuit for a combination of parasitic effects shown in Fig. 9.

The results reiterate the benefits of using a circuit simulator to analyze IDL data: it is a quick and flexible method to explain complex nonlinear lifetime behavior where an analytical solution is not possible. In this case, the circuit simulation leads to a reinterpretation of the IDL results, which otherwise would lead to the conclusion that the sample is dominated by SRH recombination in the bulk.

V. CONCLUSION

IDL data are one of the most important characterization tools for solar cell process development and monitoring. With the recently developed PL lifetime measurement technique, reliable low injection level data can be obtained for the first time.

We have observed a wide variety of defects associated with p-n junctions that can influence PC and PL IDL data, including scratched surfaces, cracked wafers, and edge–junction and edge–bulk recombinations.

Circuit-based simulation techniques allow complex IDL curves to be accurately modeled, leading to a better understanding of the defects affecting the devices. Circuit simulators are easy to use and provide fast numerical solutions to complex transcendental equivalent circuits. We emulated a typical single-sided lifetime test structure, as well as double-side passivated and diffused lifetime test structures with an Ebers–Moll equivalent circuit, which is suitable to describe many types of solar-cell-related device structures.

Equivalent circuits for some common parasitic effects are presented in this paper—localized recombination, edge recombination, and shunting—in a variety of device configurations—single-sided, double-sided, and induced p-n junction devices. Circuit simulations are used to demonstrate the influence of these common parasitic effects on IDL data. A wide range of case studies was presented to illustrate the applicability and versatility of the technique. Interestingly, junction shunting is not experimentally observed in any of the cases that we studied in this paper. Instead, many parasitic effects that we observed in our experiments are localized recombination, edge recombination, or a combination of both. The case studies show that such parasitic effects can interfere with lifetime-based experiments. In some cases, the understanding of the influence of parasitic effects results in a reinterpretation of the IDL data and experiment conclusions.

ACKNOWLEDGMENT

The authors would like to thank A. Cuevas for the valuable comments on the manuscript, T. Trupke and R. Bardos for the discussion on topics related to the PL technique, and B. Hallam for his assistance on sample preparation.

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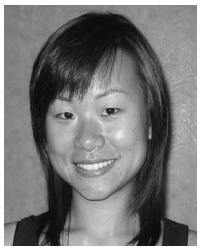

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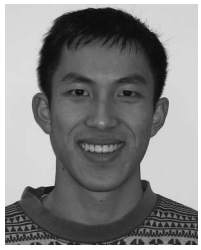

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