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Defect-assisted tunneling current-transport mechanism for Schottky diodes of Pt thin film on *p*-SiNWs tips

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ABSTRACT

The Schottky diodes of a Platinum (Pt) thin film on *p*-silicon nanowires (*p*-SiNWs) tips were fabricated. The current-transport mechanism of Pt/*p*-SiNWs Schottky diodes was defect-assisted tunneling (TU). Each silicon nanowire could be seen as a core/shell structure with a monocrystalline silicon core wrapped by a thin natural amorphous silicon oxide shell, which induced a large number of defects and enhanced the defect-assisted tunneling probability. The experimental *I–V* data were fitted to the theoretical mode of the thermionic emission (TE), generation–recombination (GR), TU, and leakage (RL) current-transport mechanisms in the temperature range of 300–370 K and voltage range of −1 to 1 V. The TU fitting data were in excellent agreement with the experimental data. Meanwhile, the tunneling parameter (E_0) was independent of the temperature, which closely followed the TU current-transport mechanism. Defect-assisted tunneling mechanism of Pt/*p*-SiNWs Schottky diodes could be applied to many other Schottky junction devices, especially, for low-dimensional nanostructures.

1. Introduction

Silicon nanowires (SiNWs) had drawn significant attention in the past decades. Various potential applications including optoelectronics, photovoltaics, thermoelectrics, battery electrodes, biological, and chemical sensors had been explored [1–8]. In all applications, the contact property between metal and SiNWs was an inevitable and essential topic. In recent years, studies of metal/SiNWs contact properties had been reported [9–11]. However, the current-transport mechanisms of metal/SiNWs contact were not clearly demonstrated in those studies. It was well known that SiNWs displayed unique small-size effects, electrical properties, and large specific surface characteristics that were not displayed by their bulk counterparts. Meanwhile, a lot of papers had been published [12,13] that each silicon nanowire could be seen as a core/shell structure and a thin natural amorphous silicon oxide shell was loosely bound to a monocrystalline silicon core, which induced a large number of defects and greatly enhanced the tunneling probability. However, for the contact between metal and bulk silicon with a doping concentration of $\sim 10^{16}$ cm^{-3}, tunneling did not play a role in the current-transport mechanisms [14].

In this work, Pt thin film was deposited on the tips of *p*-SiNWs to form Schottky diodes. The current-transport mechanisms in Pt/*p*-SiNWs Schottky diodes were investigated. In room ambient light, the forward *I–V* characteristics of the devices were measured at various ambient temperatures ranging between 300 and 370 K. The experimental data were fitted with various current-transport mechanisms, such as the thermionic emission (TE), generation–recombination (GR), tunneling (TU), and leakage (RL) currents. The results indicated that current-transport mechanism of Pt/*p*-SiNWs Schottky diodes was defect-assisted tunneling.

2. Experimental

The process for Schottky diodes with Pt thin film on *p*-SiNWs tips was summarized in Fig. 1. The double-sided polished p-type silicon-wafer (with (100) orientation and ~0.1–10 cm resistivity) was cleaned via standard RCA process (Fig. 1a). For protection purpose, photoresist was spin-coated on one side of silicon-wafer (Fig. 1b). Then, the wafer was immersed in a mixture of 5.6 mol/l HF aqueous solution and 0.025 mol/l silver nitrate ($AgNO_3$) with equal volume at room temperature for 1 h. *p*-SiNWs were fabricated (Fig. 1c), which had been reported in our previous work [15,16]. The technique was based on the galvanic displacement of Si by $Ag^+ \rightarrow Ag^0$ reduction on the wafer surface. Briefly, Ag^+ reduced onto the Si wafer surface by injecting holes into the Si valence band and oxidizing the surrounding lattice, which was subsequently etched by HF. The initial reduction of Ag^+ formed Ag nanoparticles on the wafer surface, thus delimiting the spatial

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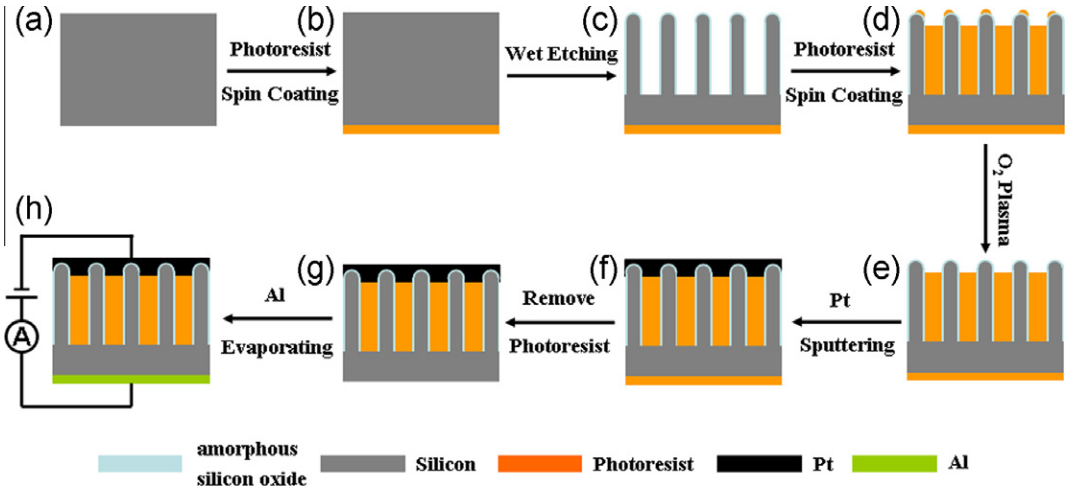

Fig. 1. Schematic illustration of the fabrication of Pt/*p*-SiNWs Schottky diodes. (a) The double-sided polished p-type silicon-wafer was cleaned via standard RCA process. (b) Photoresist was spin-coated on one side of silicon-wafer. (c) Formation of SiNWs by silver-assisted electroless wet chemical etching. (d) Spin coating of photoresist with the speed of 3500 rpm and the coating time of 20 s in order to ensure that the tips of *p*-SiNWs took out. (e) O_2 plasma was employed to remove the remaining photoresist to expose the tips of SiNWs. (f) Pt was deposited on the tips of *p*-SiNWs by electron beam evaporation. (g) Photoresist on backside of wafer was removed by acetone. (h) The wafer was sliced into chips for the measurement.

extent of the oxidation and etching process. Further reduction of Ag^+ occurred on the nanoparticles, not the Si wafer, which became the active cathode by electron transfer from the underlying wafer [9].

Fig. 2a showed the scanning electron microscopy (SEM) image of *p*-SiNWs with a length about 8 μm. Fig. 2b displayed the high resolution transmission electron microscopy (HRTEM) images of single silicon nanowire with a diameter of ~50 nm. In addition, the core–shell structure of SiNWs was obvious. A thin natural amorphous silicon oxide shell typically ~5 nm was visible. The upper and lower left insets in Fig. 2b were the selected area electrical diffraction (SAED) of the natural amorphous silicon oxide shell and silicon nanowire core, respectively. It was indicated that the natural amorphous silicon oxide shell was amorphous while the silicon nanowire core was single crystalline. A top SEM image of *p*-SiNWs was exhibited in Fig. 2c.

After *p*-SiNWs growth, photoresist was spin-coated (Fig. 1d). The spin-coating speed was 3500 rpm and the coating time was 20 s in order to ensure photoresist to fill into the gaps among *p*-SiNWs and make the tips of *p*-SiNWs take out. Similar methods

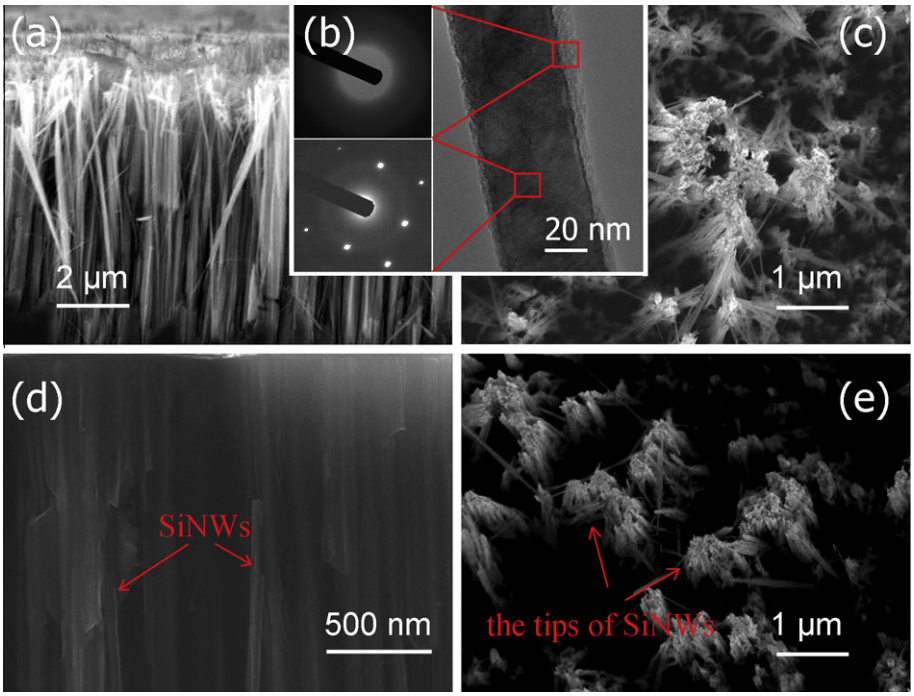

Fig. 2. Structural characterization of SiNWs. (a) The scanning electron microscopy (SEM) image of a cross-sectional view of *p*-SiNWs with a length about 8 μm. (b) The high resolution transmission electron microscopy (HRTEM) images of single silicon nanowire with a diameter of ~50 nm. A thin natural amorphous silicon oxide shell typically ~5 nm was visible. The upper and lower left insets were the selected area electrical diffraction (SAED) of the natural amorphous silicon oxide shell and silicon nanowire core, respectively. (c) The top SEM image of *p*-SiNWs. (d) The cross sectional image of *p*-SiNWs after photoresist spin coating. (e) The top morphology of *p*-SiNWs after photoresist spin coating. The length of SiNWs exposed for contacting with Pt was more than several hundred nanometers.

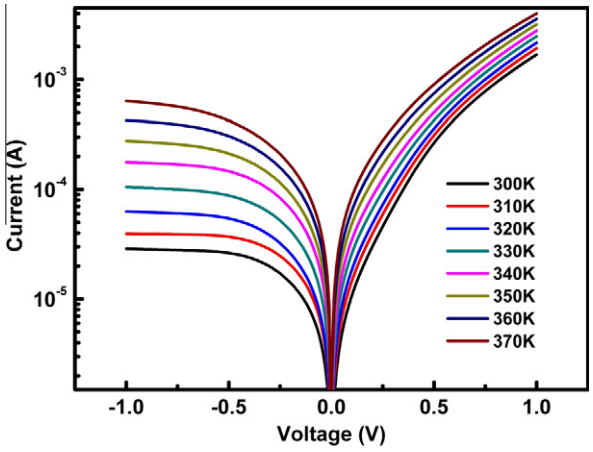

Fig. 3. ln(I)–V–T characteristics of Pt/p-SiNWs in the temperature range from 300 to 370 K and voltage range of −1 to 1 V.

had been reported in the literatures [17–20]. A little photoresist might remain on p-SiNWs tips, O_2 plasma was then employed to remove the remaining photoresist to expose the tips of SiNWs (Fig. 1e). The cross sectional and top morphology of p-SiNWs after photoresist spin coating were shown in Fig. 2d and e, respectively. The length of SiNWs exposed for contacting with Pt was more than several hundred nanometers. Then, Pt was deposited on the tips of p-SiNWs by electron beam evaporation through the metal shadow mask (Fig. 1f). The Pt electrodes with 0.5×0.5 cm^2 square geometry were then formed. For Al/bulk p-Si ohmic contact fabrication, acetone was used to remove the photoresist on backside of wafer (Fig. 1g). Next, Al thin film was thermally evaporated on the backside of p-Si wafer and annealed at 450 °C for 5 min in nitrogen atmosphere in order to establish a large area backside ohmic contact. Finally, the wafer was sliced into chips for the measurement (Fig. 1h).

The I–V–T measurements were performed by Keithley 6487 Picoammeter to detect electrical properties and drying cabinet on forced convection to build the ambient temperature range of 300–370 K in room ambient light. The morphologies of prepared samples were observed by scanning electron microscopy (FE-SEM, Philips XL30FEG) and high resolution transmission electron microscopy (HRTEM, JEM-2100). O_2 plasma treatment was performed by plasma etcher (ICP-98A).

3. Results and discussion

In order to correctly prove the current-transport mechanisms of Pt/p-SiNWs, thermionic emission (TE), generation–recombination (GR), tunneling (TU) and leakage (RL) current-transport mechanisms were all considered. In general, the relationship between the applied-bias voltage ($V \geqslant 3kT/q$) and the current of the Schottky diodes was given by [21]

$$I_{tot} = I_{TE} + I_{GR} + I_{TU} + I_{RL} \tag{1}$$

and the individual current contributions were

$$I_{TE} = I_{TE(0)}\left\{\exp\left[\frac{q(V - IR_S)}{nkT}\right] - 1\right\} \tag{2}$$

$$I_{TE(0)} = AA^*T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{3}$$

$$I_{GR} = I_{GR(0)}\left\{\exp\left[\frac{q(V - IR_S)}{2kT}\right] - 1\right\} \tag{4}$$

$$I_{TU} = I_{TU(0)}\left\{\exp\left[\frac{q(V - IR_S)}{E_0}\right] - 1\right\} \tag{5}$$

$$I_{RL} = (V - IR_S)/R_L \tag{6}$$

According the literatures [22,23], E_0 and E_{00} could be defined as

$$E_0 = E_{00}\coth(E_{00}/kT) \tag{7}$$

$$E_{00} = (qk/4\pi)(N/m^*\varepsilon)^{0.5} \tag{8}$$

where $I_{TE(0)}$ was the reverse saturation current, $I_{GR(0)}$ the generation–recombination saturation current, $I_{TU(0)}$ the tunneling saturation current, R_S the series resistance, n the ideality factor, T the absolute temperature, A the rectifier contact area, A^* the effective Richardson constant (32 A/cm^2 K^2 for p-Si), Φ_{b0} the zero-bias barrier height, E_0 the tunneling parameter, E_{00} the characteristic tunneling energy, m^* ($m^* = 0.6m_0$ for (100) Si [24], m_0 the electron rest mass) the hole effective mass, ε the dielectric constant of Silicon, N the doping concentration and R_L the resistance corresponding to the leakage current. From Eq. (2), the value of n was calculated from the slope of the linear region of the forward bias ln(I)–V plot and could be written as [11]

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \tag{9}$$

Meanwhile, Φ_{b0} could be obtained from Eq. (3)

$$\Phi_{b0} = \frac{kT}{q}\left[\ln\left(\frac{AA^*T^2}{I_{TE(0)}}\right)\right] \tag{10}$$

In our previous work [11], by taking the natural logarithm of Eq. (3), we could obtain the equation

$$\ln\left(I_{TE(0)}/T^2\right) = \ln(AA^*) - q\Phi_{b0}/kT \tag{11}$$

According to Eq. (11), the value of AA^* could be obtained from the plots of $\ln(I_{TE(0)}/T^2)$ vs. q/kT.

Fig. 3 showed the ln(I)–V–T characteristics of Pt/p-SiNWs Schottky diodes, which were measured in the temperature range from 300 to 370 K. For all the experimental temperatures, the Pt/p-SiNWs Schottky diodes exhibited clear Schottky rectifying behavior. From Fig. 3, the maximum linear region was found in the intermediate forward bias voltage range ($0.1 \leqslant V \leqslant 0.5$ V) at

Table 1
Temperature dependent values of various parameters determined from the forward bias I–V characteristics are listed. The value of tunneling parameters E_0 and the tunneling saturation current $I_{TU(0)}$ was obtained by least-squares fitting of Eq. (5).

T (K)	I_0 (A) $\times 10^{-5}$	Slope (A V^{-1})	n	nT (K)	Φ_{b0} (eV)	E_0 (eV)	$I_{TU(0)}$(A) $\times 10^{-5}$
300	4.38	8.37	4.62	1386	0.519	0.130	1.97
310	6.62	8.26	4.53	1404	0.527	0.132	2.75
320	10.13	8.16	4.44	1421	0.534	0.133	3.62
330	14.11	8.49	4.14	1366	0.543	0.130	5.05
340	19.99	8.55	3.99	1357	0.551	0.131	7.02
350	28.73	8.63	3.84	1344	0.558	0.132	10.70
360	47.63	8.97	3.59	1292	0.560	0.131	15.10
370	59.88	8.93	3.51	1299	0.570	0.134	22.20

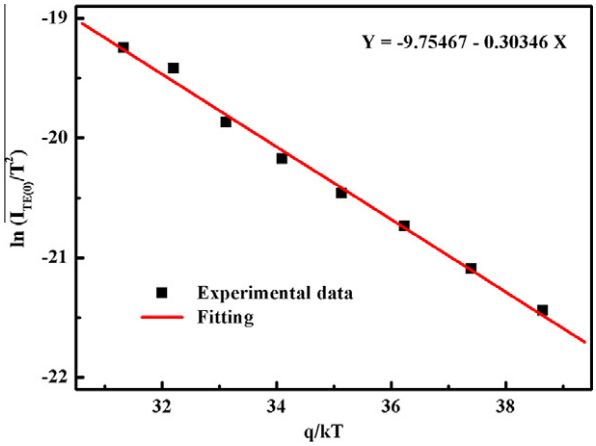

Fig. 4. The plots of $\ln(I_{TE}(0)/T^2)$ vs. q/kT for Pt/p-SiNWs Schottky diodes.

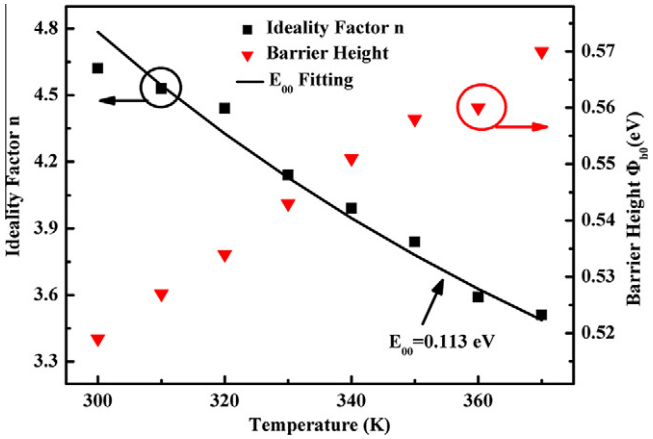

Fig. 5. The zero-bias barrier height Φ_{b0} and the ideality factor n obtained from the forward bias I–V data in the temperature range from 300 to 370 K. E_{00} could be obtained by fitting Eq. (12) to the n (T) data and the fitting value of E_{00} was 0.113 eV.

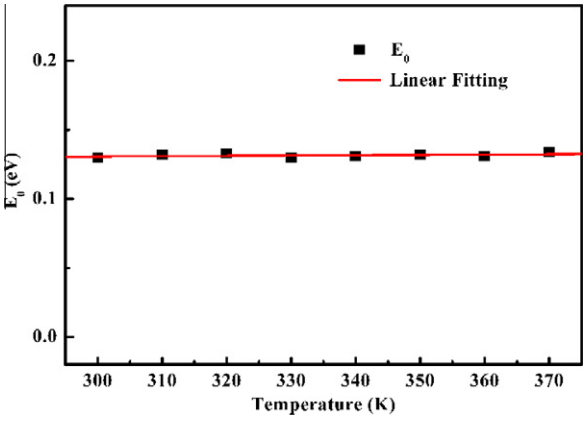

Fig. 6. The plots of E_0 vs. kT/q for Pt/p-SiNWs Schottky diodes.

300 K. With the increasing temperature, according to Eq. (5), the series resistance (R_S) had a great influence on the electrical characteristics of our investigated Schottky diodes and induced the curves nonlinear [11]. Hence, at 370 K, the linear region was only in the range of $0.2 \leqslant V \leqslant 0.4$ V. The ideality factor (n), the zero-bias barrier height (Φ_{b0}) and the reverse saturation current ($I_{TE(0)}$) could be calculated from this linear slope and y-axis intercept, which were all listed in Table 1. According to Eq. (11), the plots of $\ln(I_{TE(0)}/T^2)$ vs. q/kT were shown in Fig. 4 and the value of AA^* was 5.80×10^{-5} A/K^2. If the theoretical A^* value of 32 A/cm^2 K^2 for p-Si was used to estimate the rectifier contact area A for Schottky diodes based on the p-SiNWs, the estimated area was 1.81×10^{-6} cm^2, which was significantly lower than the square geometry sample area of 0.5×0.5 cm^2. It was well known that SiNWs had the vast surface-to-bulk ratio. Hence, the actual geometry area was so much larger than 0.5×0.5 cm^2. The contradictory result indicated that the TE current-transport mechanism was not applicable to the experimental data.

Fig. 5 showed the temperature dependent values of the zero-bias barrier height (Φ_{b0}) and the ideality factor (n). From Fig. 5, we could see that the values of n decreased with increased temperature and were greater than 1.0, which indicated that the main transport mechanism was associated with carrier tunneling rather than thermal diffusion [25,26]. As per the Sah–Noyce–Shockley theory [27], the forward current in a p–n junction was dominated by recombination of minority carriers injected into the neutral regions of the junction. This type of current gave an ideality factor of 1.0. Recombination of carriers in the space charge region, mediated by recombination centers located near the intrinsic Fermi level, resulted in an ideality factor of 2.0. If the ideality factors were greater than 2.0, the literatures reported earlier [25,26] were attributed to deep-level-assisted tunneling. Tunneling enhanced bulk recombination in which electrons/holes first tunneled to a trap and then fell in the valence/conductance band, or first fell into a trap and then tunnel to the appropriate band. In other words, the high ideality factors ($n > 2.0$) was the characteristic of tunneling mechanism [28].

As shown in Fig. 5, the values of Φ_{b0} increased with increasing temperature. At room temperature, Φ_{b0} was 0.519 eV, which was larger than the values of 0.23 and 0.18 eV reported by Li et al. [29] and by Lyu et al. [30] for PtSi/p-Si (1 0 0) contacts, respectively. The reason was attributed to the size effect [11]. When the bulk silicon was etched to form SiNWs, the energy band structure would be changed. The forbidden gap of the SiNWs was larger than that of the bulk silicon [31]. The Schottky barrier could be expressed by $\Phi_B = \Phi_M - \chi_S$. Hence, given the metal work function (Φ_M), the Schottky barrier became larger while the electron affinity (χ_S) decreased. Hence, the Schottky barrier increased. However, the variation of Φ_{b0} with temperature was opposite to that of the experimental plots by Mohammad [31] for Schottky contacts to SiNWs. This contradiction was possible due to Eq. (3), which was not representative of the reverse saturation current of our samples implying that the current transport mechanism was not the TE [14].

For the TU current-transport mechanism, Eq. (5), the slope of the $\ln(I)$ versus V plot was essentially temperature independent. In Table 1, n values changed from 4.62 (at 300 K) to 3.51 (at 370 K). However, the slope and nT values remained almost unchanged over the same temperature range with an average of 8.54 A/V and 1359 K, respectively. Meanwhile, as could be seen in Fig. 6, E_0 were located on a straight line, which indicated E_0 was independent of the temperature. It was evident that the mechanism of current-transport was tunneling [14].

According to the literatures [22,23], Eq. (7) could also be defined as

$$E_0 = E_{00}\coth(E_{00}/kT) = nkT \tag{12}$$

Therefore, E_{00} could be obtained by fitting Eq. (12) to the n (T) data. As shown in Fig. 5, the fitting value of E_{00} was 0.113 eV, which was far more than kT/q. Thus, E_0 was nearly independent of the temperature. According to the reports [22,23], TU became important when $E_{00} >> kT/q$, whereas GR dominated when $E_{00} \sim$ kT/q, and TE was crucial if $E_{00} << kT/q$. On this basis, we also calculated

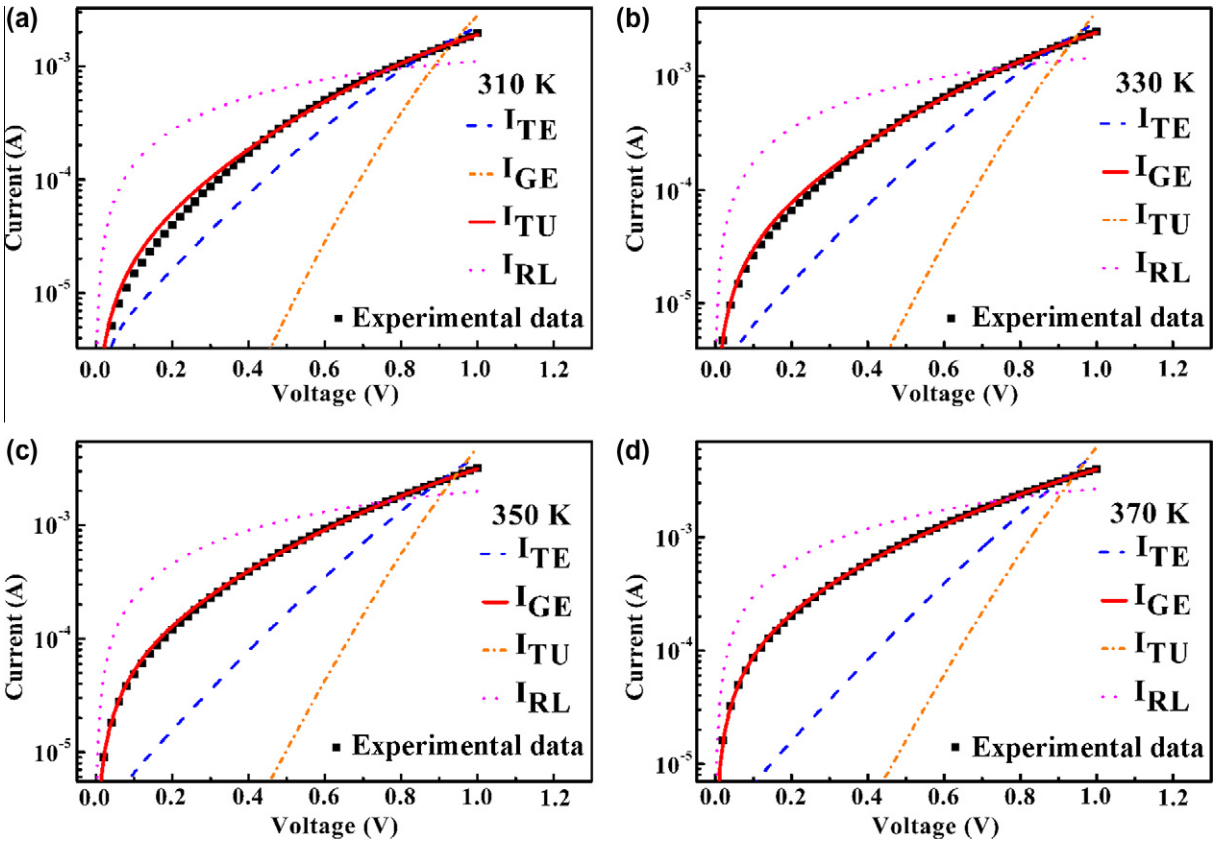

Fig. 7. The least-squares fits of the thermal emission (TE) [Eq. (2)], generation–recombination (GE) [Eq. (4)], tunneling (TU) [Eq. (5)] and leakage (RL) [Eq. (6)] equations to the experimental *I–V* data measured at (a) 310, (b) 330, (c) 350, and (d) 370 K.

the doping concentration *N* induced by the defects of *p*-SiNWs with Eq. (7) and Eq. (8). The value of *N* was $\sim 4.84 \times 10^{19}$ cm^{-3}. This concentration was high enough to generate defect-assisted tunneling effect [32,33].

In order to determine that the true current-transport mechanism was defect-assisted tunneling current-transport mechanism, we fitted the experimental *I–V* data to the theoretical mode. As shown in Fig. 7, the experimental *I–V* data were in excellent agreement with defect-assisted tunneling current-transport mechanism at the whole temperature range. $I_{TU(0)}$ and E_0, which were determined from the fit of Eq. (5) to the experimental *I–V* data, were summarized in the seventh and eighth columns of Table 1.

As well known, Bardeen proposed a theory that the Fermi level was pinned by surface states and the rectification characteristics of a metal–semiconductor contact were practically independent of the metal work function [34]. Cowley et al. [35] also explained the discrepancy between Schottky model and experimentally measured Schottky barrier height by introducing interface state and

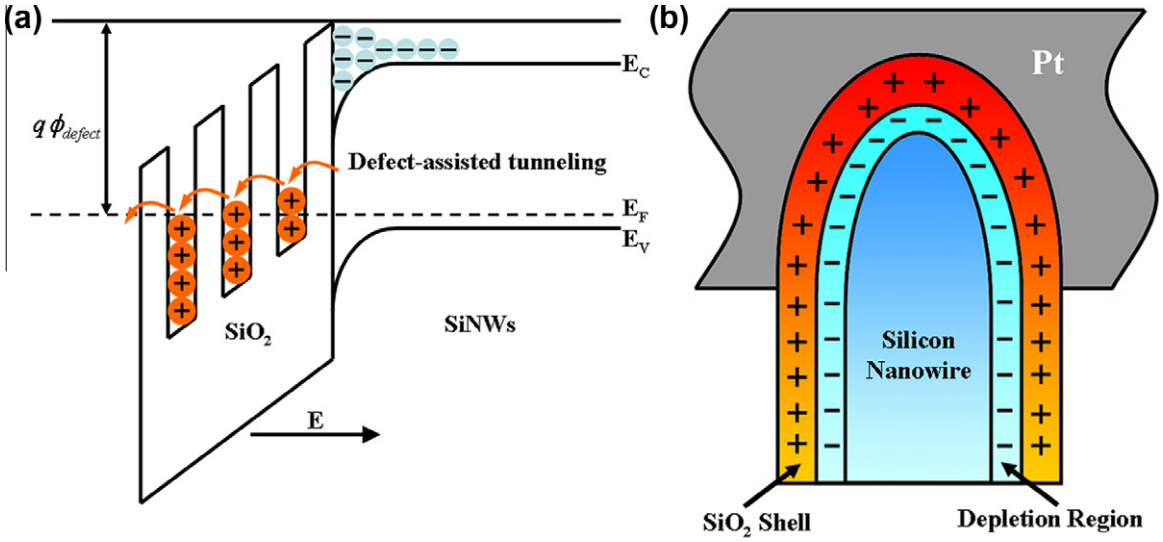

Fig. 8. (a) The energy band diagram at crystalline/amorphous interface of *p*-SiNWs. (b) The schematic of depleted region at crystalline/amorphous interface of *p*-SiNWs.

concluded that the surface states density was a property of the semiconductor and independent of the metal.

For SiNWs wrapped with thin natural amorphous silicon oxide, a large number of defects were located at the crystalline/amorphous interface [12,13] and formed high surface states. According to Bardeen theory [34], the Fermi level of SiNWs was pinned by the surface states. Fig. 8a showed the schematic energy band diagram of the Si/SiO_2 interface of SiNWs. Fig. 8b displayed the schematic of depleted region at the Si/SiO_2 interface. In general, the interface position of the Fermi level was pinned by surface states slightly below the center of the gap for silicon [23,36–38]. Therefore, the interface defect-level of *p*-SiNWs was higher than the intrinsic Fermi level and the energy band bended downward. Defects at the Si/SiO_2 interface absorbed positive charge from the underlying bulk, creating a narrow space charge region, and a corresponding build-in electric field *E* that pointed into the bulk and repelled positive charge [39,40]. In Fig. 8a, Φ_{defect} was the barrier height induced by the defects of *p*-SiNWs and *E* was build-in electric field, which was opposite to Pt/*p*-SiNWs Schottky diodes forward voltage. By applied forward voltage, the build-in electric field was decreased and the holes were more readily able to tunnel in the direction of the arrows to the neighboring trap, then the further trap, and finally out of the insulator.

4. Conclusion

In summary, the current-transport mechanisms for Schottky diodes of Pt/*p*-SiNWs were carried out by using $\ln(I)$–*V*–*T* characteristics in the temperature range of 300–370 K and voltage range of −1 to 1 V. The results demonstrated the current-transport mechanism of Pt/*p*-SiNWs Schottky diodes was defect-assisted tunneling. The thin natural amorphous silicon oxide layer with positive charges could accelerate the tunneling transport of electrons. We believed that the approach presented here could be applied to many other Schottky junction devices, especially, for low-dimensional nanostructures.

Acknowledgments

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