Effect of dry etching and subsequent annealing of Si/SiGe/Si heterostructure

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Exposure to dry etching can deleteriously affect strained SiGe films by initiation of misfit strain discontinuity in the film as well as at the interface. In this paper annealing behavior of defects generated as a consequence of dry etching of Si/SiGe/Si heterostructure metal–oxide–semiconductor capacitors have been reported. Some samples were wet etched for comparison. Samples were annealed at four different temperatures after being etched, namely, 650, 700, 750, and 800 °C. Results of the investigations using deep-level transient spectroscopy reveal defect levels at 0.62, 0.57, 0.56, and 0.44 eV for the dry-etched samples and at 0.31, 0.43, 0.56, and 0.44 eV for the wet-etched samples annealed at the aforetold temperatures. The results could be explained on the basis of appearance of point defects condensing into dislocation loops which eventually shrink and disappear as the annealing temperature is increased. The estimated size of the dislocation loops agrees quite well with the experimentally measured values obtained for identically processed samples. © *1996 American Institute of Physics.* [S0021-8979(96)08708-2]

I. INTRODUCTION

The fact that the fundamental band gap (indirect) of strained Ge_xSi_{1-x} layer covers a fairly large range between 1300 and 1550 nm[1,2] makes this alloy very attractive for applications involving long-wavelength integrated optoelectronics using silicon substrate. Advanced epitaxial techniques like molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) have made it possible to grow pseudomorphic Ge_xSi_{1-x} layers on silicon substrate.[3] Tunability of band gap in these films has made them important for heterostructure electronic devices. Several devices using SiGe like heterojunction bipolar transistors (HBTs),[4,5] *p*-metal–oxide–semiconductor field-effect transistors (MOSFETs)[6,7] have been demonstrated to have significant performance leverage over the conventional bipolar transistors and *p*-MOSFETs. This is made possible because of the enhanced mobility that is achieved due to selective doping. Schottky-barrier long-wavelength IR detector has also been fabricated using strained SiGe films.[8] All these have stimulated much interest among researchers to obtain a thorough understanding of this alloy.

Reactive ion etching appears to be the most promising technique which is required to transform the submicron patterns for very large scale integrated (VLSI) circuits. Reactive ion etching (RIE) is known to have a disadvantage of being a low-density plasma source utilizing high-energy ions. Energetic ion and deep UV radiation are likely to create lattice damage due to physical defects by ions and charge release/relaxation by photons which in turn produce trapping centers for electrons and holes at interfaces as well as in the bulk. It may also create strain-relieving misfit dislocations and/or threading dislocations. Presence of these dislocations will greatly affect the performance of the devices and hence should be kept away from the active device region. Thorough knowledge of the defects induced during device processing thus becomes necessary. Though reactive ion etching of Si has been studied in detail,[9,10] not much is known about SiGe at present. Wet etching, on the other hand, is known to be a rather nondestructive method and hence retains the characteristics of the starting materials after the processing is done. In bulk semiconductors annealing causes condensation of point defects into dislocation loops which then shrink and disappear after further annealing. The driving force behind the eventual shrinking is the reduction in self energy of the dislocation loops. Hence, it is important to be fully aware of various defects generated during processing and the effect of annealing on those defects. Deep-level transient spectroscopy (DLTS) has been established as a potential technique[11,12] for semiconductor characterization that reveals information about several characteristics of the electrically active defects present in such materials. With these considerations the authors have performed a comparative study of the annealing behavior of the defects generated as a result of dry and wet etching.

II. EXPERIMENT

The enhanced mobility achieved in Ge_xSi_{1-x} strained layers containing about 20% or less Ge has made these materials important for various electronic applications. Undoped Ge_xSi_{1-x} ($x=0.20$) layers with thickness of 500 Å were grown on *p*-Si substrates by conventional CVD at atmospheric pressure. Si cap layers 1500–1900 Å thick were deposited on the Ge_xSi_{1-x} layer. SiH_4 and GeH_4 were used as Si and Ge sources, respectively. Dry etching was performed in a DRYTECH-100 plasma reactor at a chamber pressure of 150 mTorr with a flow rate of 50 sccm SF_6 and Freon 115 each. The rf power was 400 W. The etch rate was 40 Å/s and etching was continued for 28 s to remove about 1100 Å of Si cap. On the other hand, wet etching was carried out in a solution of 25 mg KOH, 1 mg $K_2Cr_2O_7$, 25 ml

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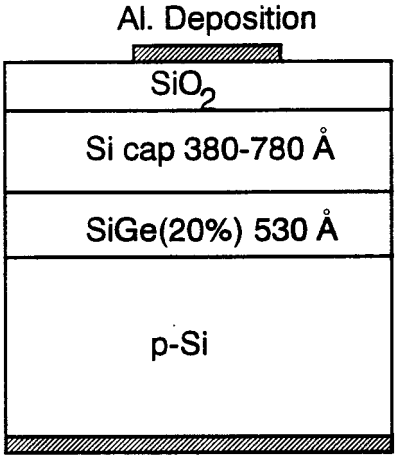

FIG. 1. Schematic drawing of the MOS device structure used for the investigations.

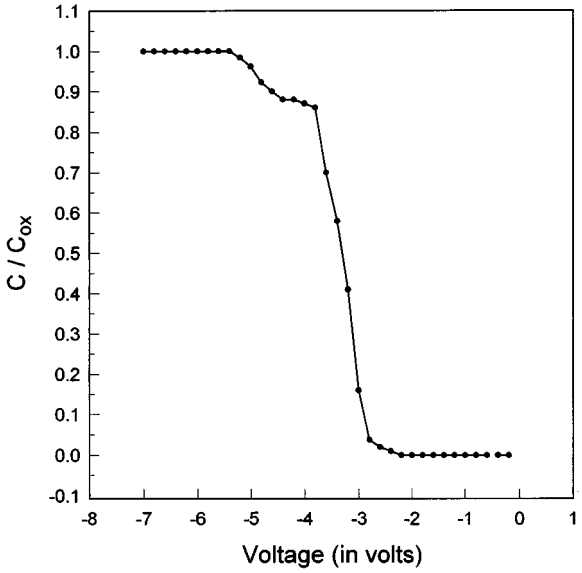

FIG. 2. Typical *CV* plot obtained for a MOS capacitor.

propanol in 100 ml of water at 26 °C. The etch rate was 160 Å/min and etching was continued for 7 min. Samples were annealed at temperatures of 650, 700, 750, and 800 °C for 60 s in a rapid thermal process (RTP) reactor under vacuum. SiO_2 was then grown by liquid phase chemical vapor deposition (LPCVD) at 450 °C. The thickness of SiO_2 was 400 Å. Al dots were then evaporated through a metal mask by thermal evaporation to make MOS capacitors. Back contact was made with Al deposition on the Si substrate. A completed sample structure is shown in Fig. 1.

Deep-level transient spectroscopy was performed to obtain information about the deep levels. The DLTS measurement system consisted of a PC, a Boonton 7200 capacitance meter, programmable temperature controller, and a HP 8013 pulse generator. The temperature of the sample was varied between 80 and 370 K by a MMR Technologies compressed liquid nitrogen and heating arrangement in a specially designed sample holder inside a low-temperature microprobe. The filling pulse time was 2 ms. A differential capacitor was employed to scale the capacitance values to the measurable range. Transient response was recorded in the computer with the help of an analog–digital converter. The MOS devices were biased to 3 V by a dc supply into depletion. The superimposed majority carrier pulse drove the silicon surface into accumulation to populate the trap centers. Transient response was measured both while cooling and heating in the aforesaid temperature range in steps of 2 K. DLTS measurements were performed on both the dry- and wet-etched samples.

III. RESULTS AND DISCUSSIONS

CV measurements carried out on the MOS capacitors show a deep depletion. A typical *CV* plot for a dry-etched unannealed sample is shown in Fig. 2. As may be seen from this plot a small kink (indicated by arrow) is observed here. A similar plot was obtained for the wet-etched unannealed samples. However, no such kink was noticed in any of the samples after the annealing was performed. This could be due to the relaxation of the lattice, that results in a broadening of the band gap. Pulse height of 2 V (from -3.2 to -5.2 V) which makes the depletion region pass through the SiGe layer, was applied to drive the device to accumulation for the DLTS measurement. Figures 3 and 4 demonstrate the DLTS spectra of the dry- and wet-etched samples respectively, annealed at different temperatures, recorded during cooling of the sample from 370 to 80 K in steps of 2 K. As may be seen from these figures there exists a peak for each sample and temperature. Defect levels were calculated using Arrhenius plots with four rate windows. A typical Arrhenius plot employed for the dry etched samples is shown in Fig. 5. The calculated trap levels and the corresponding trap concentrations are summarized in Table I.

However, no DLTS peak was observed for the wet-etched, unannealed samples, indicating the samples to be

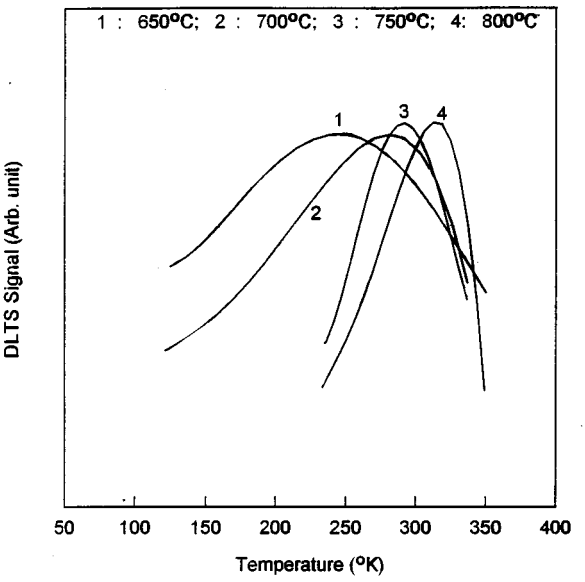

FIG. 3. DLTS signal obtained for the dry-etched sample annealed at different temperatures.

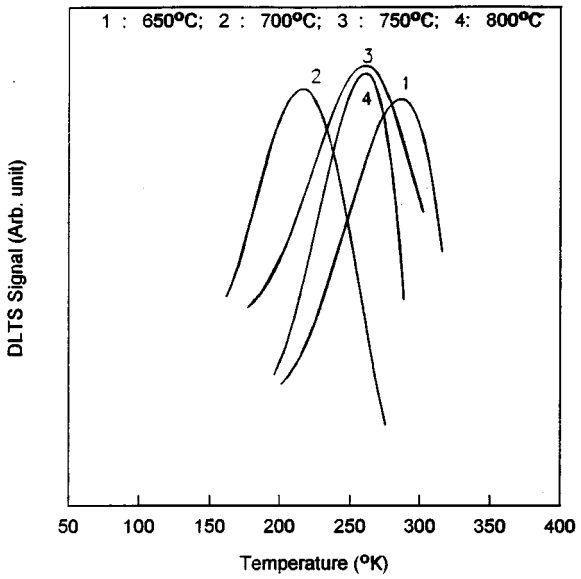

FIG. 4. DLTS signal obtained for the wet-etched samples annealed at different temperatures.

stained and free of defects in the SiGe layer. No significant difference was observed in the DLTS spectra during heating as compared to that of cooling.

The presence of the defect level at 0.31 eV for the wet-etched 650 °C annealed sample could be due to small point defects. It is known that in bulk semiconductors annealing causes condensation of point defects into dislocation loops, which then eventually shrink and disappear after further annealing. Reduction in self energy of the dislocation loops is the driving force behind their shrinking. But if a dislocation is present in Ge_xSi_{1-x} and intends to expand, it will impinge on the epilayer/substrate interface. If the films are strained, the self energy of the loops will be balanced by the strain

TABLE I. Observed defect levels and defect concentrations for the dry- and wet-etched samples.

Annealing temperature (°C)		650	700	750	800
Dry etched	E_c-E_t (eV)	0.62	0.57	0.56	0.44
	Defect conc.(cm^{-3})	8.15×10^{15}	7.72×10^{15}	7.36×10^{15}	7.07×10^{15}
Wet etched	E_c-E_t (eV)	0.31	0.43	0.56	0.44
	Defect conc. (cm^{-3})	3.10×10^{15}	2.55×10^{15}	2.22×10^{15}	1.87×10^{15}

energy that is relaxed within the loop. The total energy is thus given by the algebraic sum of the two, i.e.,

$$E_{\text{total}}=E_{\text{loop}}-E_{\text{strain}}. \tag{1}$$

Energy associated with any interface step, if created, has been ignored here, which looks reasonable for small Ge concentration in the alloy, since it has an almost similar elastic constant as that of Si. Formulation and discussion of Eq. (1) has been done by many authors.[13–15] Most general behavior of Eq. (1) is an initial increase of total energy with increase in the radius of the circular loop r, which passes through a maximum activation barrier ΔE at a critical radius r_0 and then decreases as r is further increased. It becomes zero at r_1 and then becomes negative. This is illustrated in Fig. 6.

As the annealing temperature increases in a wet-etched sample from 650 to 700 °C, the mobility of the point defects also increases. These point defects form dislocation loops of increased radius. However, their radius is smaller than the critical radius r_0. Hence from the discussions above (Fig. 6) their energy will be increased and thus we observe a defect level at 0.43 eV. A similar mechanism increases the

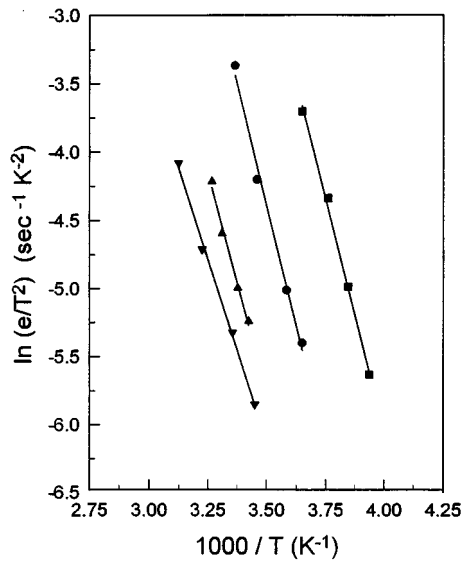

FIG. 5. A typical Arrhenius plot used to calculate the trap levels for the dry etched samples.

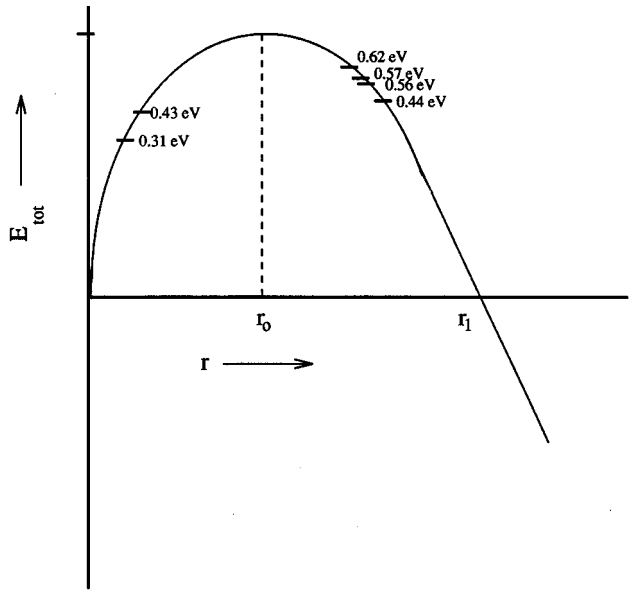

FIG. 6. Variation of total energy of the dislocation loops as a function of loop radius.

trap level to 0.56 eV after annealing at higher temperature, i.e., 750 °C. But a further annealing at 800 °C increases the radius of the condensing loops beyond the critical radius r_0 and thus from Fig. 6 the total energy decreases, so the defect level moves to 0.44 eV.

It is well established that RIE creates dislocation loops either by high-energy ion bombardment or by electron stress which are able to create misfit dislocation due to their energies. So it is apparent that a dry-etched sample will be less strained as compared to its wet-etched counterpart. Hence, in our case we may assume that the dry-etched 650 °C sample is relatively more relaxed with respect to the 650 °C wet-etched one. It is obvious that a point defect/dislocation loop will move more freely (i.e., have higher mobility) in the dry-etched sample than the wet etched. So, the dry-etched 650 °C annealed sample will contain dislocation loops having bigger radius which from Fig. 6 will correspond to a higher energy. This may be the reason behind the trap level at 0.62 eV calculated for this sample. With increase in the annealing temperature dislocation loops condense and form bigger loops. However, it is observed that the energy of the defect levels decreases from 0.62 to 0.57, 0.56, and 0.44 eV for annealing at 700, 750, and 800 °C, respectively. This clearly indicates that the radius of dislocation loops present in the relatively relaxed 650 °C annealed film is already beyond the critical radius r_0. As may be clearly seen from Fig. 6 any further increase in radius will decrease the total energy. Thus a dry-etched sample is relaxed at a lower temperature as compared to a wet-etched one prepared under similar conditions. Decreasing trap density with increasing annealing temperature in the dry as well as wet-etched samples is in line with the observed increase in the loop radius as per our model (Table I). When the radius of the loops increases, they merge to form loops of bigger radius and hence this results in a decrease in their density.

The appearance of same defect level for the 750 and 800 °C annealed, dry- as well as wet-etched sample, according to our model indicates similar lattice mechanism. This strongly suggests that the lattice is getting completely relaxed at 750 °C and further annealing on the samples manifests the same behavior irrespective of the fact that they were dry etched or wet etched. Our results are in agreement with that of Hull *et al.*[16] which indicates that at low Ge concentration, annealing between 550 and 750 °C causes significant stain relaxation.

An estimate of size of the dislocation loops can be obtained by using Eq. (1) and the expressions for E_{loop} and E_{strain} given by Bacon and Crocker.[17] According to them

$$E_{\text{loop}}=\frac{\mu b^2 r}{4(1-\nu)}\left[\frac{b_z^2}{b^2}+\left(1-\frac{\nu}{2}\right)\left(1-\frac{b_z^2}{b^2}\right)\right]\left[\ln\left(\frac{\pi r\alpha}{b}\right)-1.758\right]+\frac{\mu b^2 r}{32(1-\nu)^2}\left[(6-4\nu)\left(\frac{b_z^2}{b^2}\right)-(1-2\nu)\left(1-\frac{b_z^2}{b^2}\right)\right], \tag{2}$$

$$E_{\text{strain}}=\frac{\pi r^2\mu(1+\nu)\epsilon}{(1-\nu)}(b_g\cos\chi\cos\psi+b_e\cos^2\chi). \tag{3}$$

Here, b is the dislocation Burgers vector, b_z is the component of the Burger vector normal to the dislocation loop, ν the Poisson's ratio, r the loop radius, μ is the shear modulus, α the dislocation core parameter, ϵ is the strain (lattice mismatch) between Ge_xSi_{1-x} and Si, b_g and b_e are the glide and climb components respectively, χ is the angle between the loop normal and the free surface, and ψ the angle between b_g and the line in the free surface which is normal to the intersection of the dislocation loop with the epilayer-substrate interface.

Hull and Beam have reported[15] the presence of only 60° type of dislocations in the $Ge_{0.15}Si_{0.85}$/Si(100) samples in the temperature range 550–850 °C, while in the $Ge_{0.25}Si_{0.75}$ samples the proportion of 90° type of dislocations are increased. So, our sample [$Ge_{0.2}Si_{0.8}$/Si(100)] annealed in the temperature range 650–800 °C can be assumed to have a majority of 60° type of dislocations which will move by pure glide rather than climb. From Eq. (1) it is observed that E_{total} will be zero when the loop and strain energy as given above are equal; i.e.,

$$\frac{\mu b^2 r}{4(1-\nu)}\left[\left(1-\frac{\nu}{2}\right)\right]\left[\ln\left(\frac{\pi r\alpha}{b}\right)-1.758\right]=\frac{\pi r^2\mu(1+\nu)\epsilon}{(1-\nu)}(b\cos\chi\cos\psi). \tag{4}$$

Here, we have neglected the second term in the expression for E_{loop} (as done by many authors) because inclusion of the ''surface traction'' effect would serve to reduce the activation barrier for 60° dislocations. However, a major unknown quantity in this expression is the dislocation core energy α. Hirth and Lothe[18] have suggested a value <1 for metal and ~ 4 for covalent fcc structure. The magnitude of α is related to the dislocation cutoff radius R by the relation: $R=b/\alpha$, which gives a value of $R\sim b$ in metals and $\sim b/4$ in semiconductors. But Eaglesham *et al.*[14] have mentioned the dependence of loop energy upon the core parameter which is very crucial in determining the energetics of dislocation nucleation. Hull *et al.*, however, have proposed the inappropriateness of such a large value of α for alloys. Making use of Hooke's law[15] a rather appropriate value for $\alpha=2$ may be obtained for the present situation. Since the dislocations move by glide only, the climb component of the burger vector has been omitted from the expression for E_{strain}. Simplification of Eq. (4) gives

$$(0.85)[\ln(\pi r/2)]=0.06\ r,$$

where the following numerical substitutions have been made: $b=4$ Å, $\nu=0.3$, $\alpha=2$, $\epsilon=0.04$, $\cos\chi=0.5$, and $\cos\psi=0.742$.

Solving the above equation gives a value of $r_1\sim 6$ Å (i.e., $r_0=3$ Å). From the discussions above it is known that the radii of the dry etched samples (r) lie in the range $r_0<r<r_1$; i.e., they lie between 3 and 6 Å. Hence their diameter (~their size) varies between 6 and 12 Å. Transmission electron microscope (TEM) investigations carried out on identically processed samples indicate[19] the loops to have size in the range 10–12 Å which matches quite closely to our estimated value.

IV. CONCLUSION

The above investigations reveal that reactive ion etching induces dislocation loops whose size increases with increase in annealing temperature that eventually changes the trap levels. The Si/SiGe/Si heterostructures examined are found to relax at 750 °C. DLTS has successfully been employed to provide information about the defect and their annealing behaviors. However, this technique alone is not adequate to provide all the required information to understand the mechanism thoroughly. Cross-sectional TEM and optical band-gap measurements will add credence to our model. Investigations guided by the above considerations are in progress in our laboratory in order to obtain concrete understanding of the problem.

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