

Engineering of defects in resistive random access memory devices



Cite as: J. Appl. Phys. **127**, 051101 (2020); doi: [10.1063/1.5136264](https://doi.org/10.1063/1.5136264)

Submitted: 13 November 2019 · Accepted: 14 January 2020 ·

Published Online: 3 February 2020



View Online



Export Citation



CrossMark

Writam Banerjee,^{1,a)} Qi Liu,² and Hyunsang Hwang¹

AFFILIATIONS

¹Center for Single Atom-based Semiconductor Device, Department of Material Science and Engineering, Pohang University of Science and Technology (POSTECH), Pohang 790-784, South Korea

²Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, No. 3, BeiTuCheng West Road, ChaoYang District, Beijing 100029, China

^{a)}Author to whom correspondence should be addressed: writam@postech.ac.kr

ABSTRACT

Defects are essential to switch the resistance states in resistive random-access memory (RRAM) devices. Controlled defects in such devices can lead to the stabilization of the switching performance, which is useful for high-density memory and neuromorphic computing applications. In contrast, uncontrolled defects in RRAM can generate randomness and increase intrinsic entropy, which are useful for security applications. In this tutorial, we explain how to engineer defects in RRAM devices. More specifically, we focus on defect engineering of the oxide layer and how the defects can affect the switching mechanism. Defect engineering processes include the doping effect, nanocrystal-based switching layer design, embedded metals in switching oxide, defective electrode design, etc. We explain how defects can improve the electrical performance of RRAM devices and the recent development of applications using defect-based RRAM devices.

Published under license by AIP Publishing. <https://doi.org/10.1063/1.5136264>

I. INTRODUCTION

Over the past few decades, the computing capability of digital computers has enhanced at a faster rate due to continuous miniaturization of transistors' dimension. In the era of the Internet of things (IoT), because of an intrinsic bottleneck of energy efficient data processing speed, recently, Von Neumann computers have encountered serious challenges. Advanced brain-inspired computing demands time. Synaptic abilities are researched in hardware implemented neural networks.^{1–11} High-density memory with analog type switching is the basic need for neuromorphic computing. Various analog-programmable emerging nonvolatile memory (NVM) devices such as phase change memory (PCM), spin-transfer torque magnetic random-access memory (STT-MRAM or STT-RAM), and resistive random-access memory (RRAM) are cutting edge technologies. Modern high-speed in-memory computing systems have been developed on the shoulders of these emerging NVMs.^{12–20} Comparison among different emerging NVMs is shown in Fig. 1(a). Because of the simple two-terminal design, cost effective ultrahigh density vertical three-dimensional (3D) stacking, high-speed operation, etc. RRAM has become a noticeable candidate among the rest.^{21,22}

RRAM, also known as memristor or resistive switches, is an electronic device based on a metal–insulator–metal (MIM) structure, in which the internal resistance state is the recorded history of the applied stimuli in the form of current or voltage, and the switching is the change of such state from a high resistance state (HRS) to a low resistance state (LRS) and vice versa.^{23–32} Digitally, two states can be represented as “0” and “1” for HRS and LRS, respectively (the other way is also possible). The process to change HRS to LRS is known as SET and the process to change LRS to HRS is known as RESET. Depending on the transistor size, the one transistor one resistor (1T1R)-based device can be scaled closer to 8F²; however, the stackable one selector one resistor (1S1R) structure can be scaled down to 4F². In such extremely small (~2 nm) devices,³³ high-speed resistive switching (RS) (~1 ns)³⁴ costs only minimal energy with 6-bit/cell storage capacity.²⁵ For a standard memristor array, several laws are employed to define the current in the system. Generally, Ohm's law defines the current at each cross-point and Kirchhoff's current law is the total column current, i.e., collective current originated at each cross-point. Due to the unique design, array structure, and working ability, RRAM has a wide range of applications such as storage class memory, low-power

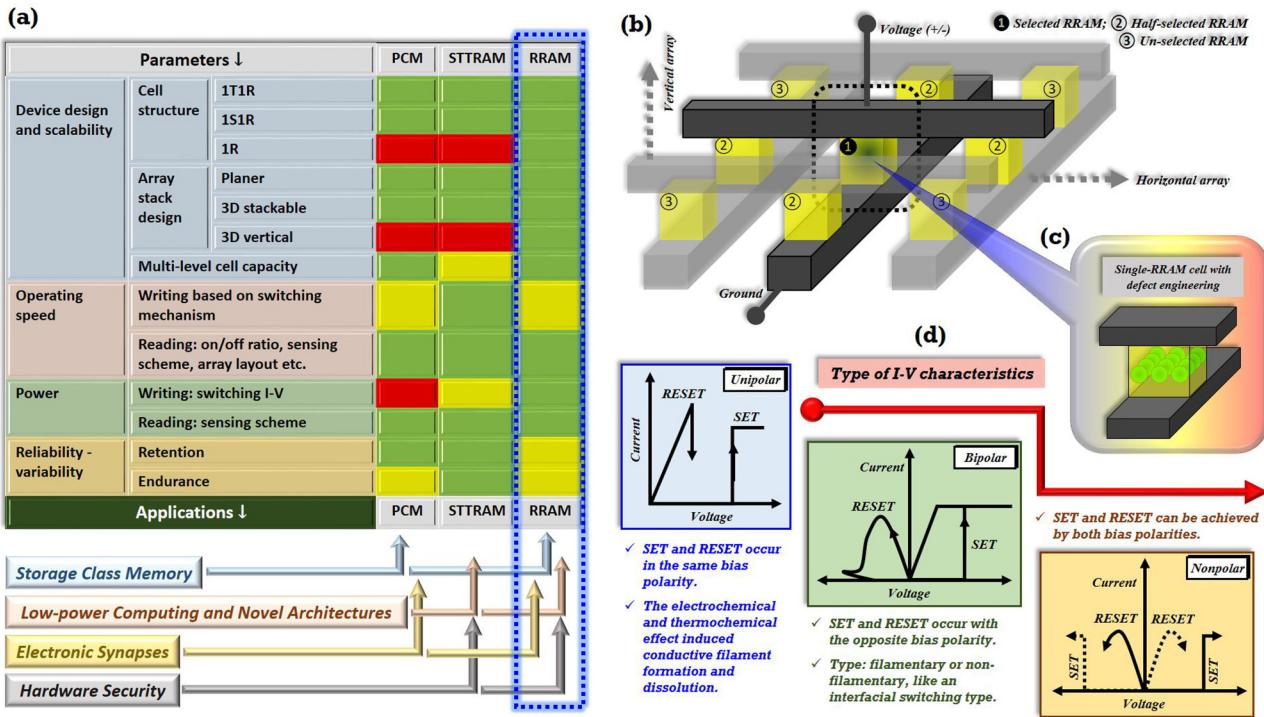


FIG. 1. (a) Schematic illustration of major emerging nonvolatile memory devices and their applications. Major emerging NVM devices are PCM, STT-RAM, and RRAM. All of them have their advantages and disadvantages.¹⁵⁶ From the application point of view, RRAM is a promising candidate in the field of memory, novel architecture, neuromorphic computing, and in security. (b) Illustration of a 3×3 array of crossbar RRAM devices. Under biasing condition, only ① device is the selected one, ② devices are half-selected cells, and ③ devices are unselected cells. (c) A single RRAM cell can be constructed with a single-oxide layer or a multiple-oxide layer or by defect engineering. (d) Generally, RRAM cells have three types of I - V characteristics. Based on the SET/RESET direction, those types are unipolar, bipolar, and nonpolar. Among them, unipolar and bipolar are the most common types.

computing, electronic synapses, and so on. Scaling of devices within the vicinity of the nanoscale regime demands innovation in the device structure, stack materials, technology, and state variables such as electron spin for STT-RAM or resistance for RRAM.

A simple MIM-based RRAM array is shown in Fig. 1(b). The key feature of the development of RRAM technology is its simple structure in which a memory element is placed in the crossing of horizontal and vertical lines; those lines in array are defined as a word line (WL) and a bit line (BL) and for a single cross-point as the top electrode (TE) and the bottom electrode (BE). The insulating layer can be a single-oxide layer, a multiple-oxide layer, or a layer with defect engineering as shown in Fig. 1(c). The materials, design of the stack, and process conditions have a great impact on switching operations. The current–voltage (I – V) characteristics can classify resistive switching (RS) into three categories as illustrated in Fig. 1(d): unipolar, bipolar, and nonpolar types. In RRAM array technology, there are mainly five types of building blocks.^{35–40} They are one resistor (1R), one selector one resistor (1S1R), one transistor one resistor (1T1R), 1TnR, and complementary metal oxide semiconductor + molecular (CMOL) cross-point memory. In the form of a three-dimensional (3D) memory array, two common types are the 3D horizontal array and the 3D vertical array. Stored

information in those devices is in the form of resistance, which can be engineered in several ways such as multilayer stack design, incorporation of nanocrystals, gradation of oxygen vacancies, and doping of switching layer. In general, every material contains some amount of defects. It is very difficult to design a device with an ideal defect free structure. Interestingly, the controlled defects are beneficial to improve the performance of RRAM devices and control the variability, but uncontrolled defects can produce randomness in behavior. Such material engineering has a great influence in new applications such as neuromorphic computing^{41–48} and the design of security systems.^{49,50}

The present tutorial concerns the engineering of defects in the insulating layer of RRAM devices, improvements of electrical performance using defect engineering, and the applications of defect-based RRAM arrays. Section II gives a general background, materials, structures of RRAM devices, and different switching mechanisms. Section III discusses about defect engineering of RRAM devices. Section IV represents the improvement of electrical performance of RRAM devices due to defect engineering and specific applications. To end this, Sec. V discusses the challenges and open scope of this research and will conclude this tutorial.

II. MATERIALS AND STRUCTURES OF RRAM

In 1884, more than a century ago, ancient conductivity was discussed by Calzecchi-Onesti.⁵¹ After a long break, in 1962, Hickmott⁵² experimentally discussed about the large negative resistance in five anodic oxide materials, i.e., SiO_2 , Al_2O_3 , Ta_2O_5 , ZrO_2 , and TiO_2 . In 1970, the concept of memristor, as a fourth fundamental element, was introduced by Chua.⁵³ After a few decades, in 2008, HP laboratories experimentally demonstrated the operation of a memristor.⁵⁴ Afterward, RRAMs or memristors have received much attention in the research community. So far, this particular technology has experienced vast structural modifications using different material systems. Based on the materials and structural changes, RS mechanisms are different.

A. Resistive switching mechanisms

In general, RRAM devices can be categorized into several forms.⁵⁵ Among them, mostly researched RRAM devices are the electrochemical metallization (ECM) type and the valence change memory (VCM) type because of their low power consumption, superior scalability up to the atomic level, and simple fabrication process. The switching event in ECM devices is dominated by the metal ion migration process, and in VCM devices, the switching events are dominated by the oxygen vacancy/oxygen migration process. According to the ECM theory, the growth of metallic filament depends on ① oxidation at the active electrode, i.e., the anode, ② electromigration of cations from the anode to the cathode, ③ reduction of cations to metal atoms to initiate nucleation at the cathode, and finally ④ the growth of the filament. As active electrode materials, Cu and Ag are the mostly used candidates. However, several other materials are also reported such as Ni,⁵⁶ Al,⁵⁷ Ti,⁵⁸ Zn,⁵⁹ Nb,⁶⁰ and Au.⁶¹ The filament formation and switching process in the VCM devices is shown in Fig. 2(b). In this case, oxygen ions and vacancies dominate the process. Hence, the core idea of RS is based on the formation or movement of internal defect states, which can be deposited and/or generated by material engineering and/or operation control. Based on that, the RS mechanism is divided into several types such as switching at the electronic scale, atomic scale defect migration, phase transition, and thermochemical reaction.

1. Switching at the electronic scale

At the electronic scale, charge trapping/detrapping is one of the basic concepts in semiconductors, which are the core mechanisms of flash memory devices. The same idea is also followed in RS. The charge carrier can be trapped by the internal defect sites in the insulating layer or at the oxide/electrode interface. The charge trapping or detrapping process leads to detect different states in the RRAM devices. The trapping/detrapping process can be enhanced by material engineering with doping or by depositing nanocrystals inside the insulating layer. Many groups have reported on nanocrystal-based devices using inorganic materials, such as ZnO ,⁶² Al_2O_3 ,⁶³ and TiO_2 , or the organic form, such as Alq_3 .⁶⁴ The presence of point defects such as vacancies in the insulator is the natural resources of trap sites. Generally, the I - V behavior in such devices follows Ohm's law ($I \sim V$) at a low voltage and Child's law ($I \sim V^2$)

at a high voltage region. In such cases, the conduction mechanism is dominated by space charge limited current (SCLC) or by trap controlled SCLC injection. Under suitable bias conditions, charge can be trapped during the SET process and detrapped during the RESET process. In general, trapping/detrapping processes are the effect of opposite bias polarities, which lead to a bipolar switching operation of the RRAM device.

In another way, charge can also be trapped in the oxide/electrode interface. When the defects in RRAM devices accumulated at the interface region, a Schottky barrier is generally formed. The application of an external bias can change the height of the barrier at the interface. For an Au/Nb:STO junction, the device can be SET with a positive bias on Au and can be RESET (HRS) with a negative bias on the same.⁶⁵

2. Atomic scale defect migration

Atomic scale defect generation is the key reason for the resistive switching in ECM and VCM type devices. In ECM devices, it is a very much electrode material dependent behavior. As compared to the electrode potentials for Pt^{2+} (1.19 V), Au^+ (1.83 V), etc., the potential for Ag^+ (0.8 V) and Cu^{2+} (0.34 V) is much smaller. In addition, Ag and Cu required a low Gibbs free energy of formation of oxides than other metals such as Ir, Pt, and Ni. Hence, Ag^+ and Cu^{2+} can easily be electrochemically dissolved and are obvious choices for ECM devices. The growth of the metallic filament also depends on the type of the insulating material, solid electrolyte based, oxide electrolyte based, or organic electrolyte based. Solid electrolyte-based ECM systems based on H_2O ,⁶⁶ Ag-Ge-Se,⁶⁷ Ag_2S ,⁶⁸ GeTe,⁶⁹ GeS,⁷⁰ etc., are dominated by ionic conductivity. In those systems, with applying positive bias on active electrodes such as Ag or Cu, cations (Ag^+ or Cu^+) can be generated from those electrodes by the oxidation process. Generated defects can be migrated through the solid electrolyte layer and reduced at the inert electrode layer such as TiN and Pt. In solid electrolyte-based systems, a metallic filament is usually developed from the inert electrode side to the active electrode side. The following RS process is the effect of the oxidation/reduction process of a tiny region of the metallic filament.

Compared to the conventional solid electrolyte-based ECM devices, cations have low solubility and diffusion coefficients in the oxide electrolyte system; hence, the mechanism is different than conventional. For any given electrolyte system, ionic conductivity depends on the metal ion flux within that system, such as in an oxide electrolyte-based system, the Cu ion flux is 10 orders of magnitude lower than that in solid electrolyte systems (i.e., $\text{Cu}/\text{CuS}/\text{Pt}$); hence, lower ionic conductivity is present in oxide electrolyte-based ECM devices. Therefore, in an oxide electrolyte-based system ($\text{Cu}/\text{ZrO}_2/\text{Pt}$),⁷¹ the mobile metal ions can combine with electrons in the oxide layer and reduce at any place inside the layer, which leads to the formation of the metallic filament from the active electrode to the inert electrode side. In an organic electrolyte-based system, such as Ag/WPF-BT-FEO/heavily doped p-type poly Si (WPF-BT-FEO stands for poly[(9,9-bis(6'-(*N,N,N*-trimethylammonium) hexyl)-2,7-fluorene]-co-(9,9-bis(2-(2-methoxyethoxy)ethyl)-fluorene)-co-(2,1,3-benzothiadiazole)] dibromide),⁷² the filament growth direction is similar to oxide-based ECM.

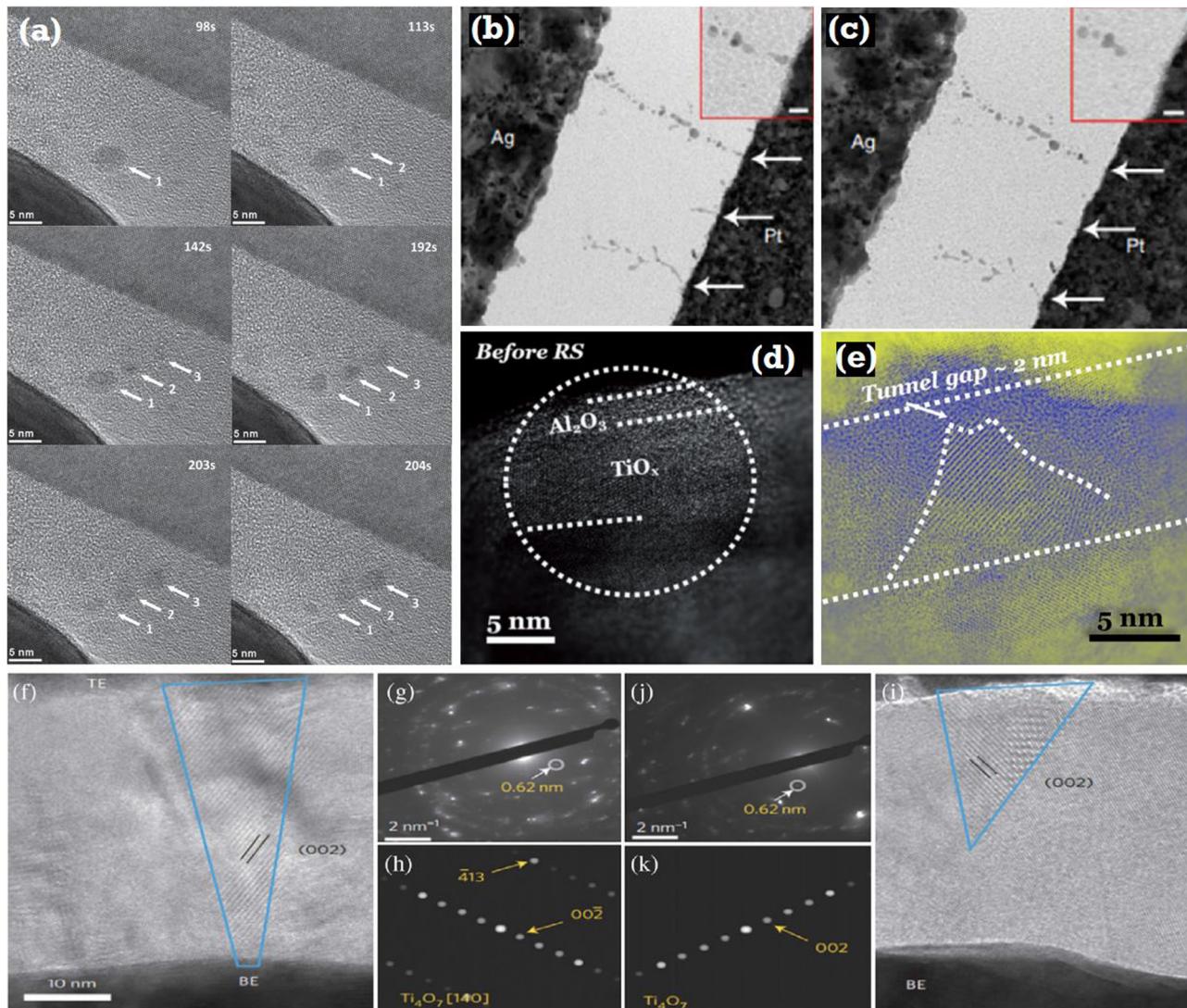


FIG. 2. (a) The HRTEM serial images of the mass transfer process in Au/Ag:SiO₂/p⁺-Si RRAM devices. Arrows represent the origin and the movements of the Ag nanoparticles. Reproduced with permission from Tian *et al.*, *Adv. Funct. Mater.* **26**, 3649–3654 (2014). Copyright 2014 John Wiley and Sons Publishing. (b) and (c) The HRTEM images of Ag-filament formation and rupture process in SiO₂-based RRAM devices, respectively. (d) and (e) The HRTEM images of TiO_x/Al₂O₃-based RRAM device before and after LRS, respectively. The filament is based on the phase transition process. Reproduced with permission from Banerjee *et al.*, *Adv. Electron. Mater.* **3** (12), 1700287 (2017). Copyright 2017 John Wiley and Sons Publishing. (f)–(j) The HRTEM images of phase transition process dominated Ti₄O₇ filament formation and rupture process during SET and RESET switching (Figures (b), (c), and (f)–(j) are reproduced with permission from Wang and Yan, *Phys. Status Solidi RRL* **13**, 1900073 (2019). Copyright 2019 John Wiley and Sons Publishing).

In another approach, active metals can be deposited or generated in the form of nanocrystals under biased conditions. The formation of an ionic electronic conductive channel by both the Ag₂S argenteite phase and Ag nanocrystals was reported by Xu *et al.*⁷³ Initially, Ag₂S was maintained at an acanthite nonconductive phase, which under positively biased conditions transformed to a conducting argenteite phase, and Ag⁺ cations started to migrate toward the cathode interface. The process leads to the formation of

Ag nanocrystals from the cathode. Figure 2(a) shows the ECM device fabricated with Ag nanocrystals in the Ag/SiO₂/p⁺-Si structure, as already shown by Tian *et al.*⁷⁴ The switching is based on the Ag mass transfer process. The time-dependent measurement shows a size modification of the Ag cluster by maintaining a nanogap between the neighboring clusters. Initially at 98s, the Ag cluster near to the Ag electrode was bigger, which changes slowly over time, and at 204s, it grew bigger near the p⁺-Si side. The

movement of the Ag cluster was in the direction of the applied electric field. In organic RRAM devices, based on the Ag/poly(3,4-ethylene-dioxythiophene):poly(styrene-sulfonate)/Pt structure, similar movement of defects in the form of Ag nanocrystals is also reported by Gao *et al.*⁷⁵ Interestingly, the nucleation of Ag nanocrystals starts from a capricious region of the organic layer. With the increasing voltage stress time, an increasing amount of nanocrystals agglomerated together and increased the size of the chain, which leads to the formation of the metallic filament in the device. Figures 2(b) and 2(c) show the formation and rupture process of the Ag filament on SiO₂-based RRAM devices, respectively.

In VCM devices, the switching process is mainly dominated by the migration of oxygen ions or oxygen vacancies. Such a system can be designed with inert metals at one side, which are not easily oxidized, such as Pt, Au, and Ir, and oxidized metals in the other side, such as Al, Ti, Nb, etc.; after oxidation, the oxidized metal cannot easily come back to its original form. Among many insulating materials, TiO_x,⁷⁶ NiO_x,⁷⁷ HfO_x,⁷⁸ TaO_x,⁷⁹ AlO_x,⁸⁰ and WO_x,⁸¹ along with nitrides such as AlN⁸² and NiN⁸³ have been studied rigorously. In such systems, the valence of oxides or nitrides will be changed due to the migration of positively charged oxygen vacancies or nitrogen vacancies under an external electric field. In VCM devices, the oxygen ions drift toward the top interface with the application of positive bias on TE. The nonlattice oxygen ions will accumulate or form an oxygen rich interfacial layer if the TE material is inert or oxidizable, respectively. In this condition, the TE-insulator interface will behave like an oxygen reservoir and the created point defects in the oxide layer will lead to the electric field-dependent soft breakdown of the dielectric film. Generally, the SET/RESET switching voltage is lower compared to the forming voltage. Voltage and current are very crucial for RRAM devices. During SET, the size and thickness of the conductive filament are very much related to the applied current level, resulting in multiple resistance levels in LRS. During RESET, the operating stop voltage limits the rupture of the filament, which provides multilevel cell storage capability in HRS.

3. Phase transition of oxides

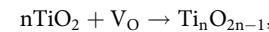
Phase transition of oxides especially metal-insulator transition is a promising resource of RS, in which the resistance changes due to the transition of the phase from metallic to insulator or vice versa. Several materials have been reported in this class such as group VB elements: VO₂,⁸⁴ NbO₂,⁸⁵ and Ca₂RuO₄⁸⁶ exhibit metal-insulator transition. Mott memory is a special type of emerging NVM, which is based on the principle of metal-to-insulator transitions.⁸⁷ The electronic-structural phase changes in the complex oxide thin films can develop this type of memory, where the change in Gibbs free energy can define the memory. The initial phase can go through a phase transition to the metastable phase by the application of external bias and the change of resistivity can be detected. The stability of the states is dominated by the kinetics of the phase transition.

Joule heating due to an applied electric field can increase the internal temperature of RRAM devices and can change the internal chemical conditions for phase transition. Generally, RS caused by this process is unipolar due to the strong thermal effect. The PCM is a prominent example of this category. In addition, several

transition metal oxides can show this type of switching. Materials such as NiO, CoO, and Nb₂O₅ based on thermochemical reaction-based RRAM devices were summarized in a previous work.⁸⁸ In the Pt/ZnO/Pt structure,⁸⁹ RESET operation was dominated by the Joule heating process, which provides a sufficient amount of energy to thermochemically break the Zn rich CF and switch the device.

Figures 2(d) and 2(e) show examples of metal-insulator transitions in Al₂O₃/TiO_x-based bilayer RRAM devices.³⁸ In general, for TiO₂ films, the oxygen-deficient Magnéli phases can be chemically formulated as Ti_nO_{2n-1}. With n = 5, Ti₅O₉ is a substoichiometric composition of metallic TiO_x, which is a conducting type, and can be obtained due to oxygen loss from the TiO₂ and Ti₂O₃. The Magnéli phase is a stable one as compared to the rutile phase. Atomic rearrangement is caused due to the bias driven localized thermal enhancement. In that condition, formation of the oxygen-deficient Magnéli phase is possible in two ways:

- ① By the removal of oxygen ions, i.e., the formation of oxygen vacancies in the lattice site,



- ② By the formation of titanium interstitial Ti_{interstitial} in an ordered way



The Magnéli phase is able to go through a temperature-dependent metal-insulator-transition process because of the mixed-valance compound. However, the conductivity of Ti₅O₉ is lower than that of the Ti₄O₇ phase. Phase transition is a very much localized phenomenon, which leads to the formation of the Ti₄O₇ filament as shown in Figs. 2(f)-2(k).

So far, plenty of materials as insulating layers have been researched for a potential candidate in RRAM. A wide range of material systems are available such as chalcogenides, perovskites, solid-state electrolytes, transition metal oxides, and organic compounds. In a collective way, the materials can be classified into two groups, i.e., inorganic and organic insulating layers. For stable RRAM operations, inorganic materials are the best option. However, cost effective simple fabrication processes and flexible device fabrication capabilities are the key advantages of organic RRAM (generally polymers and small molecule systems). RRAM devices with AlO_x, SiO_x, TiO_x, CoO_x, NiO_x, CuO_x, ZnO_x, ZrO_x, HfO_x, TaO_x, Ti_{interstitial}, and WO_x and complex oxides such as SrTiO₃,⁹⁰ La_{0.7}Sr_{0.3}MnO₃,⁹¹ and BiFeO₃⁹² are extensively investigated. As insulating layers, both single and bilayer devices are investigated. Along with several materials, the application of carbon as an electrode material, a switching layer, and also as a barrier layer in RRAM devices has been investigated.⁹³⁻⁹⁸

III. DEFECT ENGINEERING OF RRAM

Stack engineering has a great influence in determining the performance of RRAM devices. Engineering of RRAMs is summarized in Fig. 3. RRAM has a simple two-terminal design, and thus there is ample scope for structure engineering. Engineering can be done in

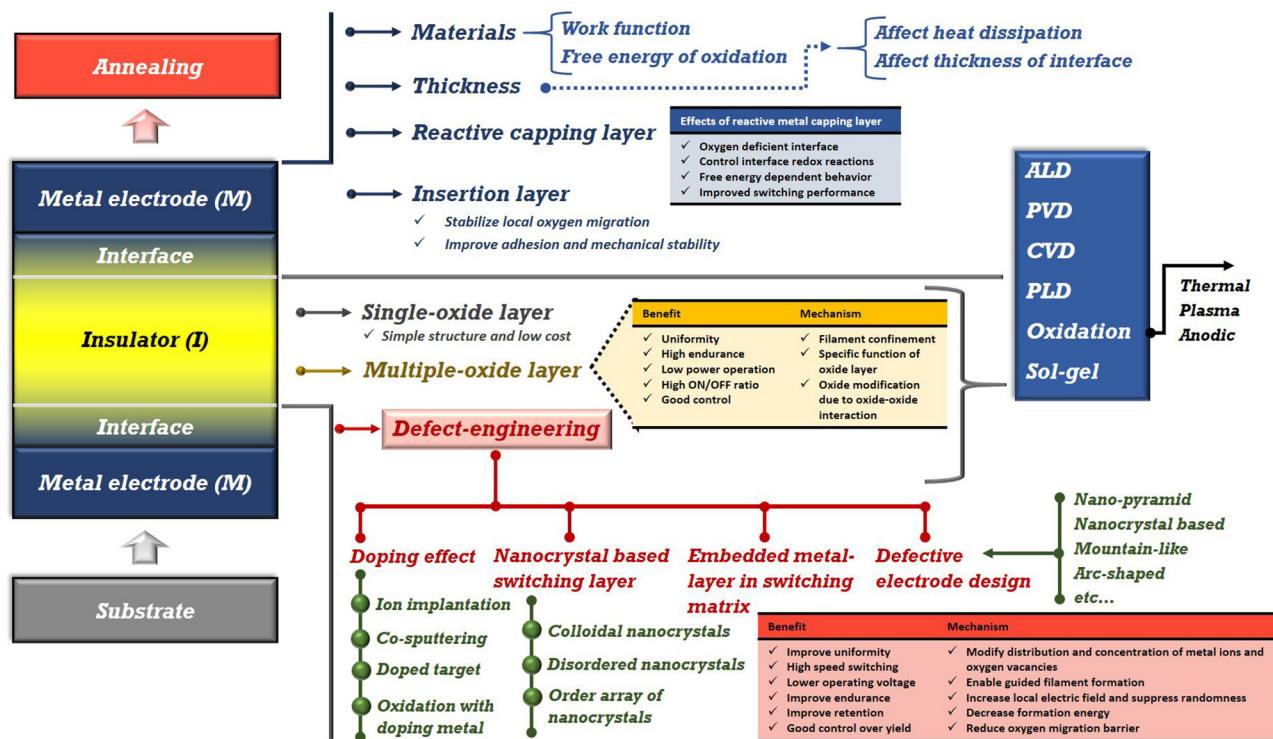


FIG. 3. Schematic representation of material engineering of RRAM devices. Defect engineering is playing a major role.

the metal layers, interfacial layers, and in the insulating layer, and the device can be fabricated using systems such as atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD). The metal work function and free energy of oxidation are the two major parameters for selecting the metal layer. At the same time, the thickness of the layer is also important as it can affect the heat dissipation and also affect the thickness of the interfacial layer formation. In some cases, deposition of the interfacial layer is important as it can stabilize local oxygen migration and improve adhesion and mechanical stability of the metal layer. In addition, in some cases, the interfacial layer can act as the barrier layer for ion diffusion, leading to the improvement in the switching stability of RRAM devices. There are several types of insulating layers. In general, for oxide-based RRAM devices, they are in the form of single-oxide layers, multiple-oxide layers, or defect engineering layers. Defect engineering can be done in several ways such as doping of the oxide layer, nanocrystal-based switching layer (NC-RRAM), embedded metal layer in switching matrix, and also with the design of a defective bottom electrode layer. Generally, defect engineering RRAM devices improved switching uniformity, lowering the operating conditions, and provided high speed, long endurance, good data retention, and improved device yield.

A. Doping in RRAM

Doping of the insulating layer can be done using several ways such as ion implantation process, cosputtering of doping material

with an oxide layer, deposition of the oxide layer using the doped target, and oxidation with doping metals. Doping engineering is an effective process for defining the performance of RRAM technology. Previously, it was reported that the doping of Cu,⁹⁹ N,¹⁰⁰ and Au¹⁰¹ can be influential for the improvement of electrical properties of RS devices. Misha *et al.*¹⁰² had reported a nitrogen-doped Ta/TaO_x/Pt RRAM device with improved switching uniformity as compared to nondoped devices. Excess nitrogen in the oxide layer can confine the oxygen migration by making a strong bond with them. By this process, localization of the filament and improvement of the switching stability are possible. In general, doping can modify the concentration distribution of the metal ions and oxygen vacancies and guide the filament formation process.

B. Incorporation of nanocrystals

Incorporating nanocrystals in the oxide layer (Fig. 4) is an efficient way to improve the electrical performances in NC-RRAM devices. Several NCs such as Ru,¹⁰³ IrO_x,¹⁰⁴ TiO₂,¹⁰⁵ Cu,¹⁰⁶ and Au were researched in RRAM devices. The NCs can cover the oxide layer completely or they can be distributed in an ordered or a disordered form in the oxide layer. In any form, NCs play several roles in RRAM devices, e.g., they can enhance the electric field and guide the filament forming process, they can migrate and form conductive filaments, and it is also possible to trap charges using NCs. Based on the structure design and NC formation process, NCs in RRAMs can be in colloidal (used to form a complete oxide

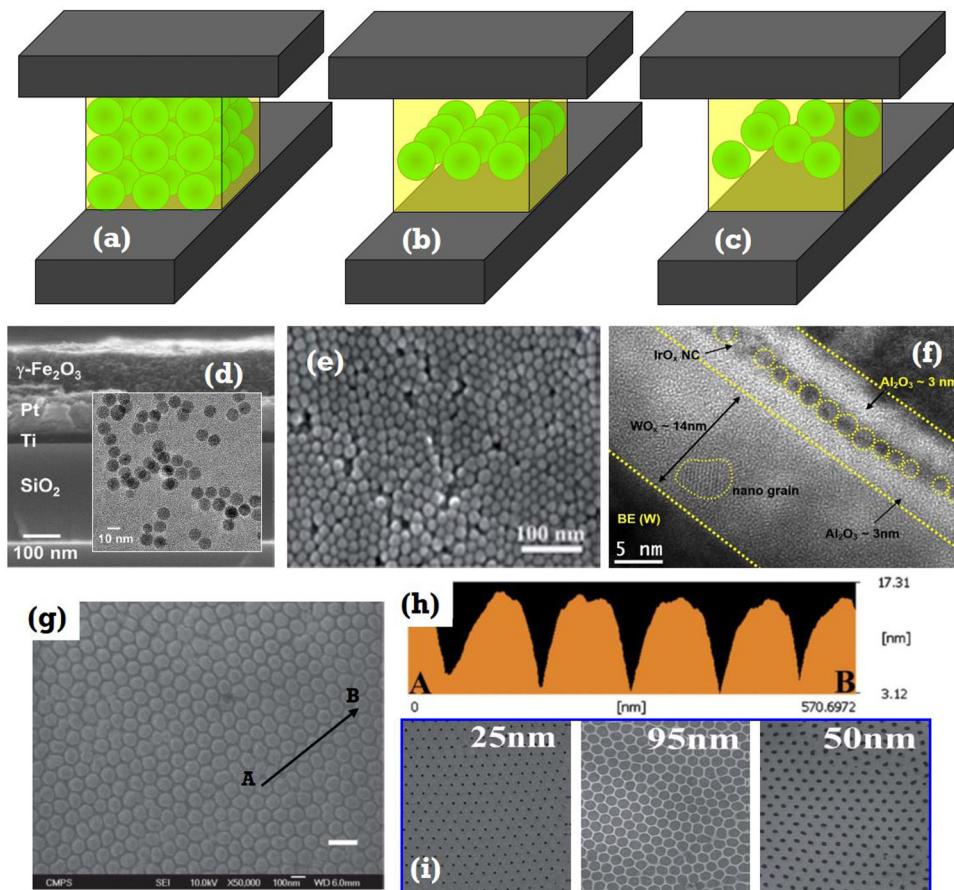


FIG. 4. Schematic illustration of (a) colloidal NC-based RRAM and (b) and (c) distributed NCs in RRAM. The HRTEM image of (d) chemical processed $\gamma\text{-Fe}_2\text{O}_3$ -NCs. Reproduced with permission from Kim *et al.*, J. Appl. Phys. 114, 224505 (2013). Copyright 2013 AIP Publishing LLC. (e) Planar view of Ni-Au-NCs layer in RRAM [Reproduced with permission from Zhong *et al.*, RSC Adv. 4, 40924 (2014). Copyright 2014 The Royal Society of Chemistry Publishing] and (f) sputtered IrO_x -NCs in Al_2O_3 matrix [Reproduced with permission from Banerjee *et al.*, Nanoscale Res. Lett. 7, 194 (2012). Copyright 2012 Springer Open Publishing], for RRAM applications. (g) The SEM image of the isolated HfO_2 nanodots, prepared by nanoporous AAO template, (h) the AFM image with thickness profile along A → B. (i) The size of the HfO_2 nanodots can be varied according to the size of the AAO templates. Reproduced with permission from Lyu and Lee, J. Mater. Chem. 22, 1852 (2011). Copyright 2011 The Royal Society of Chemistry Publishing.

layer), disordered (formed by the reduction process from an ultra-thin layer), or in ordered form (homogeneous NCs can be formed using the template).

1. Colloidal nanocrystals as complete resistive switching layers

Figure 4(a) shows a schematic colloidal NC-based RRAM design. Previously, colloidal CdS-NCs¹⁰⁷ and $\gamma\text{-Fe}_2\text{O}_3$ -NCs¹⁰⁸ were reported as complete oxide layers. A cost effective chemical solution-based fabrication process using a chemical drop-dry method is the major advantage of colloidal NC-RRAM. The NC size, NC density, and the thickness of the film can be controlled by modifying the concentration of NCs in the chemical solution. A high-resolution transmission electron microscopy (HRTEM) image of colloidal $\gamma\text{-Fe}_2\text{O}_3$ -NC-based RRAM structure is shown in Fig. 4(d). In general, the solution process colloidal NC-based oxide layer has a porous structure with a large interface area between neighboring NCs. The structure acts as a reservoir of the atoms (ions) and vacancies. In such devices, several parameters such as stoichiometry, microstructure, vacancy concentration, and defect state can change RS properties. Hence, the switching mechanism of these types of structures is not generalized. Along with the

oxide material, the performance of colloidal NC-based RRAM devices was also affected by the selection of electrode materials, as reported by Zhong *et al.*¹⁰⁹ The scanning electron microscopic (SEM) images of Ni-Au-NCs in Au/Ni-Au-NCs/ITO, and Au/Ni-Au-NCs/NSTO RRAM devices are shown in Fig. 4(e). Generally, the Ni-based RS layer can be easily oxidized and can form an interface of the NiO_x layer. Moreover, depending on the oxidation kinetics, the metallic film of Ni could easily produce NiO_x as reported by Courtade *et al.*¹¹⁰ Due to the presence of Ni^{2+} vacancies, NiO_x is an intrinsic p-type semiconductor with a bandgap of 3.6 eV. As the work function for both the Ni and Au is ~ 5 eV, the Au/ NiO_x interface is Ohmic. In Au/Ni-Au-NCs/ITO and Au/Ni-Au-NCs/NSTO RRAM devices, ITO and NSTO have work functions of 4.7 eV and 4.2 eV, respectively. Different work functions play different roles in devices. A higher diffusion potential in the NCs/NSTO interface will introduce a rectifying property and a lower diffusion potential in the NCs/ITO interface will help in the formation of the conductive filament. Therefore, using different electrode materials, it is possible to alter the interface properties with defects that will effectively change the electrical behavior of an RRAM device. Solution-processed colloidal NC-RRAM is one of the best candidates in the field of flexible electronics.

2. Randomly distributed nanocrystals in the oxide layer of RRAM

RRAM devices based on randomly distributed NCs are reported by several groups. In this type of structure, the NCs are distributed in the oxide layer or sandwiched in the form of M-I-NCs-I-M, as shown in Figs. 4(b) and 4(c). Depending on the reduction process from a thin layer of NC material, this type of structure can be formed. Point to be noted, only a few nanometer (<3 nm)-thick layer can form as-deposited NCs depending on the top and bottom oxide layer thicknesses. NCs' size and density are interrelated. Generally, for larger NCs, the density is smaller, whereas smaller NCs are usually highly dense.¹¹¹ Figure 4(f) shows the HRTEM image of randomly distributed sputtered deposited IrO_x -NC in $\text{IrO}_x/\text{Al}_2\text{O}_3/\text{IrO}_x$ -NCs/ $\text{Al}_2\text{O}_3/\text{WO}_x/\text{W}$ -based RRAM devices.⁶³ The ultrasmall ~ 1 nm IrO_x -NCs were formed from a 1.5 nm thick IrO_x metal layer during the fabrication of the complete RRAM stack. The as-deposited IrO_x -NCs with a diameter of ~ 1 nm and a density of $1 \times 10^{13} \text{ cm}^{-2}$ were formed in RRAM devices. The major advantage of this type of structure is the improvement of electric field distribution in the localized position. The high electric field can decrease the filament formation energy, which leads to a soft breakdown in NC-RRAM devices at a smaller voltage. It is always recommended to reduce the forming voltage of RRAM devices, as it can control the initial defect formation and the current overshoot effect. Generally, in NC-RRAM devices, the conductive filament can form at a lower voltage and suppress the randomness during the switching process as compared to the normal RRAM devices. Proper care must be taken during the fabrication process as a good balance between size and density is needed. Chang *et al.*¹¹² reported that in the thicker Pt NC-RRAM, the electrical properties are degraded as compared to thinner Pt-NCs. The major advantage of this type of design is operation voltage lowering thereby improving RS stability.

3. Ordered array of nanocrystals using a template

In randomly distributed NC-RRAM devices, the size, shape, and density variation of NCs can leave a strong footprint on the device-to-device performance instability and device yield, which can be improved with the controlled distribution of NCs, as shown in Figs. 4(g)–4(i). One of the effective ways is bio-nano-processed homogeneous NC-based RRAM devices. Using the cavity of cage-shaped ferritin protein, Uenuma *et al.*¹¹³ had fabricated NC-RRAM devices based on the ordered array of Pt-NCs. The core diameter of 7 nm can define the size of the NCs and the outer diameter of 12 nm can define the gap between two adjacent NCs. Using a slow chemical reaction-based biomimetic process, several materials such as Fe-oxide,¹¹⁴ Co-oxide,¹¹⁵ and Ni-oxide¹¹⁶ can be crystallized within the cavity of ferritin protein. As the ferritin protein cavity size and shape can define the NCs, the distribution of NC size on the wafer area is uniform. There are several advantages of the bio-nano-process, e.g., it has atomic scale uniformity, this method is a promising bottom-up process that can overcome the miniaturization limitations of the top-down approach, self-assembly is easy to control, and selective adsorption to the designated area.

Apart from the bio-nano-process NC array, it is also possible to design the NC array using the self-organized nanoporous

anodized aluminum oxide (AAO) template. Lyu and Lee¹¹⁷ reported a controlled distribution of the HfO_2 nanodots using the nanoporous AAO template for RRAM applications. The SEM image of the controlled distribution of HfO_2 nanodots with uniform distribution, size, and thickness is shown in Figs. 4(g) and 4(h). The size of the nanopores is one of the key players in this type of fabrication process as the size and shape of the NCs are very much dependent on that. In this case, the pore size is varied from 25 nm to 95 nm, as shown in Fig. 4(i). Hence, the design of the template with various pore sizes, pore densities, and the lengths is an important factor. As the density of the nanodots is very much dependent on the nanoporous template, the controllability of the NCs or nanodots is much better as compared to nontemplate devices. Due to this reason, the yield of this type of devices is better as compared to other NC-based designs.

C. Embedded metal in the insulating layer

Instead of embedded NCs in the oxide layer, it is also possible to engineer the device with a thin metal layer. Several metal layers, such as Cr, Cu, and Pt, are reported in the embedded form to improve the performance of the RRAM devices.^{118–120} Lim *et al.*³¹ have reported a Ta metal layer-based $\text{Cu}/\text{HfO}_2/\text{Ta}/\text{Cu}_2\text{S}/\text{W}$ structure for the improvement of the multilevel operation of the RRAM devices. In devices without a Ta metal layer, the uncontrolled injection of Cu ions created unwanted resistance fluctuations. In the Ta metal layer-based RRAM structure, Ta acts as a diffusion barrier and controls the overinjection of Cu ions; hence, there is an improvement of resistance states resulting in a stable multilevel operation. It is also possible to design such an ultrathin metal layer at the top or bottom oxide/metal interface in RRAM devices. Banerjee and Hwang²⁵ have reported a 2 nm thick Ti metal layer in Cu/HfO_2 -based RRAM devices. The ultrathin Ti layer acts as the barrier layer for Cu diffusion. The limited source can form a very stable thin Cu-based filament that can improve the quantized conduction behavior and a stable 6-bit/cell storage capacity. Therefore, depending on the location in the oxide layer, the embedded ultrathin metal layers in RRAM devices can serve in many ways such as they can enhance the stability of filament, control ion migration, and improve the adhesion.

D. Defective electrode design

The location of the NCs in the oxide layers also affects the switching of the devices. Instead of having a NC layer in the middle of the oxide layer, it is also possible to design a structure with NCs on the top of the bottom electrode or on the bottom of the top electrode. In any form, the enhancement of the electric field on the surface of the NCs is one of the major reasons in designing NCs for ECM, VCM, and also molecular memory applications.^{121,122} To control the localized formation of the conductive filament, Liu *et al.*¹²¹ had reported a Cu-NC designed BE in an $\text{Ag}/\text{ZrO}_2/\text{Cu}-\text{NCs}/\text{Pt}$ RRAM device, which is shown in Figs. 5(j) and 5(k). This process not only improves the electrical behavior but also leads to a deeper understanding of the microscopic mechanisms of the filament formation process guided by Cu-NC. A 20 nm thick conductive filament on top of Cu-NC can be observed clearly in the HRTEM image. SET and RESET processes were dominated by the

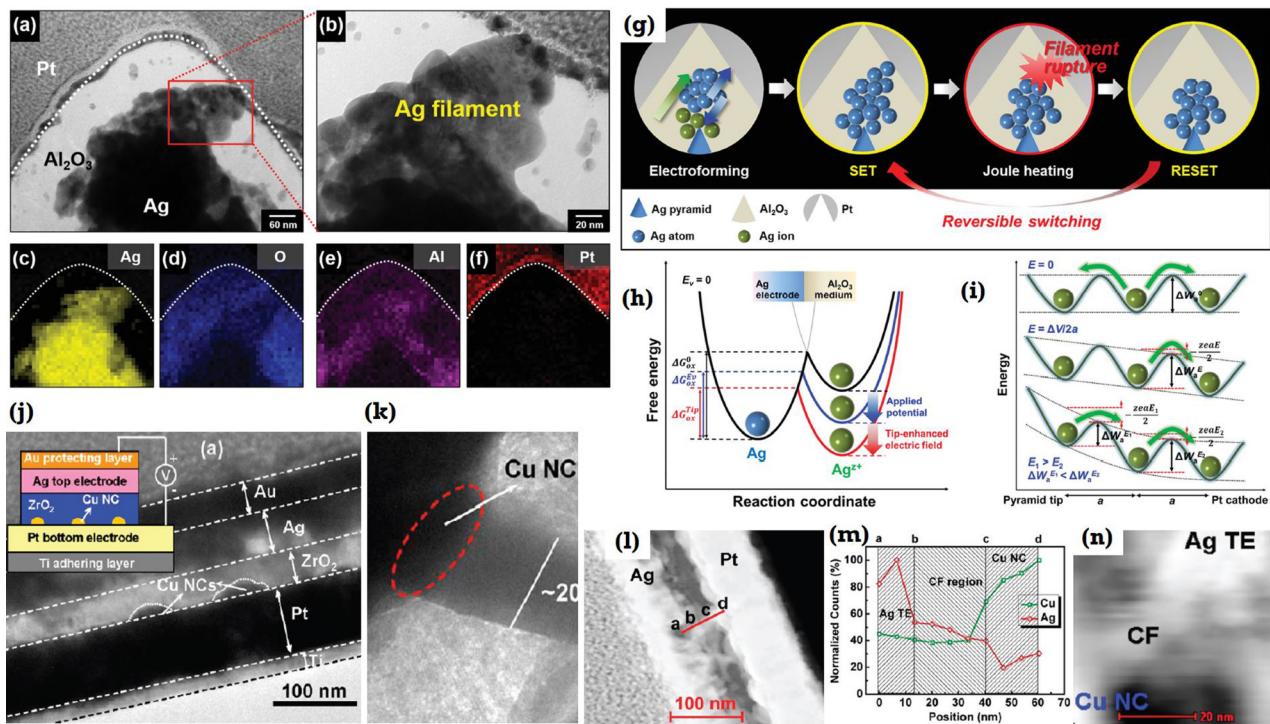


FIG. 5. (a)–(f) The HRTEM and elemental mapping of the defect engineering of electrode with the formation of Ag-nanopyramid and filament structure. (g)–(i) The tip-enhanced electric field plays a key role to form the localized filament improve the switching uniformity. Reproduced with permission from Shin et al., *Adv. Electron. Mater.* **2**, 1600233 (2016). Copyright 2016 John Wiley and Sons Publishing. (j)–(n) The Cu-NC-based bottom electrode is affecting the performance in Ag/ZrO₂/Cu-NC/Pt-based RRAM devices. The high electric field on top of the Cu-NC is beneficial for the easy formation of Ag-filament in the devices. Reproduced with permission from Liu et al., *ACS Nano* **4**(10), 6162 (2010). Copyright 2010 American Chemical Society Publishing.

formation and rupture of the conductive filament. Further physical analysis [Figs. 5(l)–5(n)] of the filament confirms that Ag is more concentrated only in the filament region. Depending on the curvature of the Cu-NC-based bottom electrode, a stronger electric field can be achieved around the NC in the oxide layer. It was reported that, for a given NC radius of 8 nm within a 40 nm thick ZrO₂ layer, the electric field intensity on the tip of the Cu-NC is almost double as compared to the flat bottomed electrode devices. Therefore, higher field on top of Cu-NCs attracts more Ag⁺ ions and the nucleation probability of Ag atoms is very high at the NC sites.

Apart from NCs, other nanostructures such as nanopyramid,^{123,124} nanopeak,¹²⁵ arc-shaped,¹²⁶ nanorod,¹²⁷ and nanowire nanostructures,¹²⁸ are also capable of improving the performance. In any form, enhancement of the localized electric field is the main objective. Huang *et al.*¹²⁴ designed a nanopyramid-based structured bottom electrode for the application of Pt/TiO₂/Cu RRAM devices. Recently, Shin *et al.*¹²⁹ reported a controllable formation of the filament using the tip-enhanced electric field in Ag-pyramid-based Ag/Al₂O₃/Pt RRAM devices. The pyramid structures were prepared using a photolithographic technique on the Si substrate. A patterned SiN layer was used as a template to design nanopyramids on the Si wafer surface using a reactive-ion etching process. On top of the Si-nanopyramids, a thick ~190 nm Ag layer was deposited.

After that, this design acts as the Ag-nanopyramid bottom electrode. The HRTEM image of the Ag-filament on top of the Ag-nanopyramid bottom electrode is shown in Figs. 5(a) and 5(b). The cone-shaped Ag-filament is because of the rapid decrease of the tip-enhanced electric field with the increasing distance from the tip. In this case, high ion migration was near the Ag tip and slow ion migration was near the Pt electrode. The material of the filament was further confirmed by elemental mapping, as shown in Figs. 5(c)–5(f). The switching mechanism in such defect-engineered bottom electrode-based RRAM devices is shown in Fig. 5(g). With the application of electrical potential to the Ag electrode, Ag ions are generated and migrated to the Pt electrode following the electric field and reduced to Ag atoms, resulting in the formation of the conductive Ag-filament. After filament rupture during RESET operation, the remaining Ag-virtual source controls the next operation and localized switching is likely to occur. The energy diagram [Fig. 5(h)] of the Ag-nanopyramid-based RRAM cell shows that under the zero bias condition or the initial condition, the activation energy of oxidation is high. Under the applied bias condition, the energy barrier decreases, and hence shows improvement. Figure 5(i) shows the impact of the Ag-pyramids on the ion hopping process. The designed electrode provides highly enhanced electric field near the tip, leading to the faster formation of the localized conductive filament.

A similar type of improvement is also possible with other defect-engineered electrodes. It is more likely due to the fact that for the nanostructured BE RRAM devices, the ionic conductivity is higher on top of the structure and the enhanced electric field helps in the faster growth of the conductive filament. The controlled localized filament takes an active part in performance improvement in terms of reliability, narrowing distributions of operating parameters, as well as good cycling and retention properties, as compared to the conventional flat electrode-based RRAM devices.

IV. ELECTRICAL PERFORMANCES OF DEFECT-ENGINEERED RRAM DEVICES AND APPLICATIONS

Two-terminal cell structures of RRAM devices provide this technology enough scope for several architectural developments in 2D and 3D space. Along with the device-level investigation, array-level RRAM also received significant attention in the past decade, which helped in developing new applications in the direction of neuromorphic computing and security. Several array designs have been proposed including 1R, 1S1R, 1T1R, 1TnR, CMOL, and 3D crossbar type.

A. Design of an RRAM array

In a simple form, 1R type RRAM can be designed in a planer structure, both in the form of via-holes and crossbars. In via-hole 1R devices, the insulating RS layer is located inside the via-hole, which connects the top and bottom electrodes. In the crossbar structure, the switching layer is located at each cross-point of the perpendicularly placed top and bottom electrode lines usually denoted as word line and bit line for arrays. Following the switching process in a single device, digital states in an array can be defined using tunable resistance, which allows multilevel storage in RRAM devices. A 1R RRAM device in the crossbar form has a minimum cell area of $4 \cdot F^2$, providing ground for the increase in the array size. Generally, the crossbar design is suitable for RRAM and PCM type devices. The structure is not very useful for STT-RAM as the small measurement window complicated the read margin. As the small cell size 1R crossbar RRAM devices are very attractive, the large sneak path current is one of the major hindrances restricting the large array size. The sneak path problem can be overcome using several types of selection devices such as self-selection process, self-rectifying, and complementary resistive switching. Experimentally, it is very difficult to fabricate a 1R device with a highly nonlinear $I-V$ performance to obtain a large array size. However, the simple two-terminal 1R design provides enough ground to engineer the selector device in a stackable form with each cross-point.

Having the similar structure and mechanism with 1R, selector devices can be placed vertically without losing additional area, and the array stands for 1S1R. A highly nonlinear selector can efficiently suppress the leakage current through the unselected cells and reduce the line resistances of the array to a greater extend. For unipolar 1R devices rectifying diodes and for bipolar 1R bidirectional selector, devices are suitable as 1S component. Depending on the shape of the $I-V$ characteristics, different types of selector devices are available such as exponential selectors, field-assisted

superlinear threshold selectors, metal-insulator-transition-based selectors, and ovonic threshold selectors. Each of them has their own advantages and disadvantages, which can be found in detail in other literature studies.^{130–134}

In the absence of selector devices, it is essential to integrate 1R devices with transistors in the form of 1T1R, and the array can be either a NAND type or a NOR type. In NAND type devices, each 1R structure is placed parallel to 1T, whereas they are placed in series with 1T for NOR type devices. In any case, 1R devices can be integrated with the source or drain side of 1T. An additional 1T device limits the current flow through the 1R; hence, a large array can be designed. Due to the presence of the transistor, 1T1R cell size increases. In addition, new 1T structures such as FinFET, gate-all-around FET, carbon nanotube FET, etc., can improve 1T1R scalability; however, several difficult challenges still need to be addressed. A minimum of $4 \cdot F^2$ cell area can be realized by using FinFET devices.^{135,136} Following the similar structure of 1T devices, recently, gate controlled three-terminal RRAM devices also have been explored;¹³⁷ however, cell structure, array design, device performance, and applications need to be addressed properly. Instead of having 1T at each cross-point 1R device, when a column of crossbar (a series connection of cross-point 1R devices) is connected with a 1T device, then the combination form is referred to as 1TnR, which can maintain a small footprint of $4 \cdot F^2$. Although this structure can reduce the sneak leakage current and internal resistance drop, this system consumes power.

In CMOL structures, there are five essential layers, i.e., 2D CMOS address decoder, segmented word-lines, memory cells, segmented bit-lines, and the bottom 2D CMOS address decoder. The CMOL structure is suitable for multilayer 3D integration.^{138,139} The structure can reduce the interconnect resistance, sneak current, parasitic capacitance, etc., but processing this type of devices and random accessibility are complicated.

Emerging applications of NVM devices are based on two major factors, one is the lower bit expense and other is the higher density of the memory devices. Monolithic 3D integrated memory arrays can fulfill both these requirements; in addition, the vertical stack enables us to maintain the smallest feature size. As compared to the 1T1R structure, crossbar is mostly suitable for this type of engineering with two different designs, i.e., 3D horizontal arrays and 3D vertical arrays. Previously, the fabrication process and usefulness of 3D RRAM arrays have been reviewed.^{35,36} All designs have their own advantages and disadvantages and can change the electrical performance of the device.

B. Improvement of electrical performance of RRAM devices using defect engineering

In any form of RRAM device, the basic operation is based on the detection of history of the resistance state created by the applied current and voltage. Generally, a stress dependent forming process is a basic step to create the conduction path in the switching layer to conduct further RS process. As discussed earlier, there are several possible mechanisms to create such a type of defective path. Usually, a virgin HRS can be broken due to the forming process. After the initial forming and 1st RESET step, an intermediate HRS will take the lead for the next RS cycle. The forming process can be

affected by device and material engineering. Defect engineering can effectively control the forming process. Banerjee *et al.*¹⁰⁴ reported the improvement in the device forming condition with lowering the forming voltage by incorporating IrO_x -NCs in $\text{Al}_2\text{O}_3/\text{WO}_x$ bilayer via-patterned RRAM devices. Chen *et al.*¹⁰³ had reported a similar phenomenon with a lower voltage forming process by incorporating Ru-NCs in Al_2O_3 RRAM. In addition, highly amorphous insulating layer-based devices need larger forming voltage as compared to the less amorphous devices. Therefore, a forming process can be affected by material engineering, material deposition methods, operating conditions, temperatures, device area scaling, and also switching layer thickness scaling. Particularly, for sub-nm scaled RRAM devices, only a single filament may dominate the switching event and the geometry of the filament can control the repeatable operation. It is also possible to eliminate the forming step with ultrathin oxide layer-based RRAM devices.

Switching process is the successful transition between HRS and LRS with an applied voltage or current.¹⁴⁰ Device internal resistance can change from HRS to LRS during the SET process and from LRS to HRS during RESET. Usually 2-bits can be produced in the device, which can be digitally defined as "1" and "0." The operating voltage is also very much dependent on several factors similar to the forming process; however, the SET voltage is always lower than the forming voltage. So far, rigorous investigation identifies the improvement of device operation by various methods. Depending on the structure design and materials of the particular RRAM, in defect-engineered devices, incorporating NCs in the oxide layer may or may not influence the SET/RESET voltage and also the resistance ratio of the particular RRAM. But the presence of the NCs must improve the variability in switching cycles of the RRAM devices. Figure 6(a) shows a very stable switching for $>10^3$ dc cycles in IrO_x -NC-based Al_2O_3 RRAM devices, with a high resistance ratio of $>10^2$. Even at a high temperature of 85 °C, the resistance ratio is remarkably stable in IrO_x -NC-based RRAM devices as compared to normal Al_2O_3 RRAM devices¹⁴¹ as shown in Fig. 6(b). Wu *et al.*¹⁴² reported that the presence of NCs in the oxide layer improved the speed of the switching. A SET switching speed of 100 ns [Fig. 6(d)] was achieved for NC-RRAM devices as compared to without NCs devices [Fig. 6(c)]. Doping of the oxide layer is also effective to control the switching variation of the RRAM devices. Both the RESET voltage and RESET current can be well controlled by N-doing in TaO_x -based RRAM devices [Fig. 6(e)]. As RESET is the critical method to achieve well controlled switching in any RRAM device, the defect engineering process is very much suitable to achieve stable switching in such devices by stabilizing RESET operation. Along with the defect engineering of the oxide layer, it is also beneficial to use the thin metal layer as a barrier of ion migration in RRAM devices. Figure 6(i) shows a typical forming free I-V switching of in $\text{Cu}/\text{Ti}/\text{HfO}_2/\text{TiN}$ RRAM devices²⁵ at a low RESET power level of several hundreds of fW. Apart from the 2-bit/cell storage, RRAM devices have shown a 6-bit/cell storage potential [Fig. 6(j)] with a long retention time for all levels [Fig. 6(k)]. The quality of the nonvolatile resistance states can be measured by retention and endurance properties, which defines whether the particular RRAM device is useful or not.

Data in standard NVMs must be retained for 10 years at 85 °C. Although several groups have reported such retention behavior,

the process is still not fully reliable as retention failure is a completely stochastic process in RRAM devices. Several effects can dominate the retention properties such as the relaxation effect, oxygen vacancy diffusion effect, and metal ion diffusion effect. The failure mechanism was modeled by many researchers.^{143,144} Material engineering is a potential tool to improve the retention performance of RRAM devices.¹⁴⁵ Device endurance, i.e., the sufferance ability, is another major issue of RRAM devices,¹⁴⁶ based on which a RRAM can be implemented as a storage class memory between storage and memory applications. The failure of endurance happens when the resistance state is stuck at the LRS or HRS. For VCM type devices, failure is mainly due to the generation/recombination of oxygen vacancies, whereas for ECM, it can be due to the excess amount of metal ions. Therefore, the HRS is mostly prone to stuck to LRS. It is also possible that the failure state can stuck to some of the mezzanine resistance states. Hence, multilevel cell storage accuracy is still in debate. Summarizing all factors, one can say that the length and width of the filament and the defect density in it are the key parameters to control the reliability properties. In engineering of filament materials, size and shape will have a direct effect to enhance such controllability.

C. Variability improvement with defect engineering

For commercialization of RRAM devices, the improvement in switching variability is one of the major concerns. Although emerging devices show the potential to overcome the energy efficient scalability challenges, cell-to-cell and device-to-device variability are significantly degrading the accuracy of resistance read processes.^{147–149} For a large scale RRAM array integration, a minimal fluctuation of resistance and voltage is desirable to maintain the uniformity of the array. In a cell-level statistical investigation, it is noted that a significant performance variation exists in the tail bits, resulting in read error in RRAM devices. The stochastic generation of defects and variation in generation of energy are two typical reasons behind this. Previous studies show that the fluctuation of a number of defects within the filament is one of the major reasons of the physical origin of resistance fluctuation in RRAMs. Recently, Tao *et al.*¹⁵⁰ reported a HfO_x -based RRAM device with a mountainlike surface-graphited carbon layer to improve the variability, as shown in Figs. 6(f)–6(h). The devices on the top of the mountain surface can surely improve the voltage and resistance variability from the cell-level to the device-level. However, in general, the cell-level local defect arrangement can change the internal band structure for each cycle and change the transport properties. The cell-level variation can affect the device-level variability, and hence the array-level. This is one of the open areas in RRAM research.

D. Applications of defect-based RRAM devices

In the traditional form, RRAM can be used for memory and storage purposes. The performance of RRAM devices is in-between NAND flash memory and DRAM; hence, it can be used as storage class memory. The switching of RRAM can be abrupt or analog type. Analog switching is very useful for neuromorphic computing, where a precise change of conductance is essential. Such computing technology will be able to learn and perform by its own. Combining such devices with CMOS can

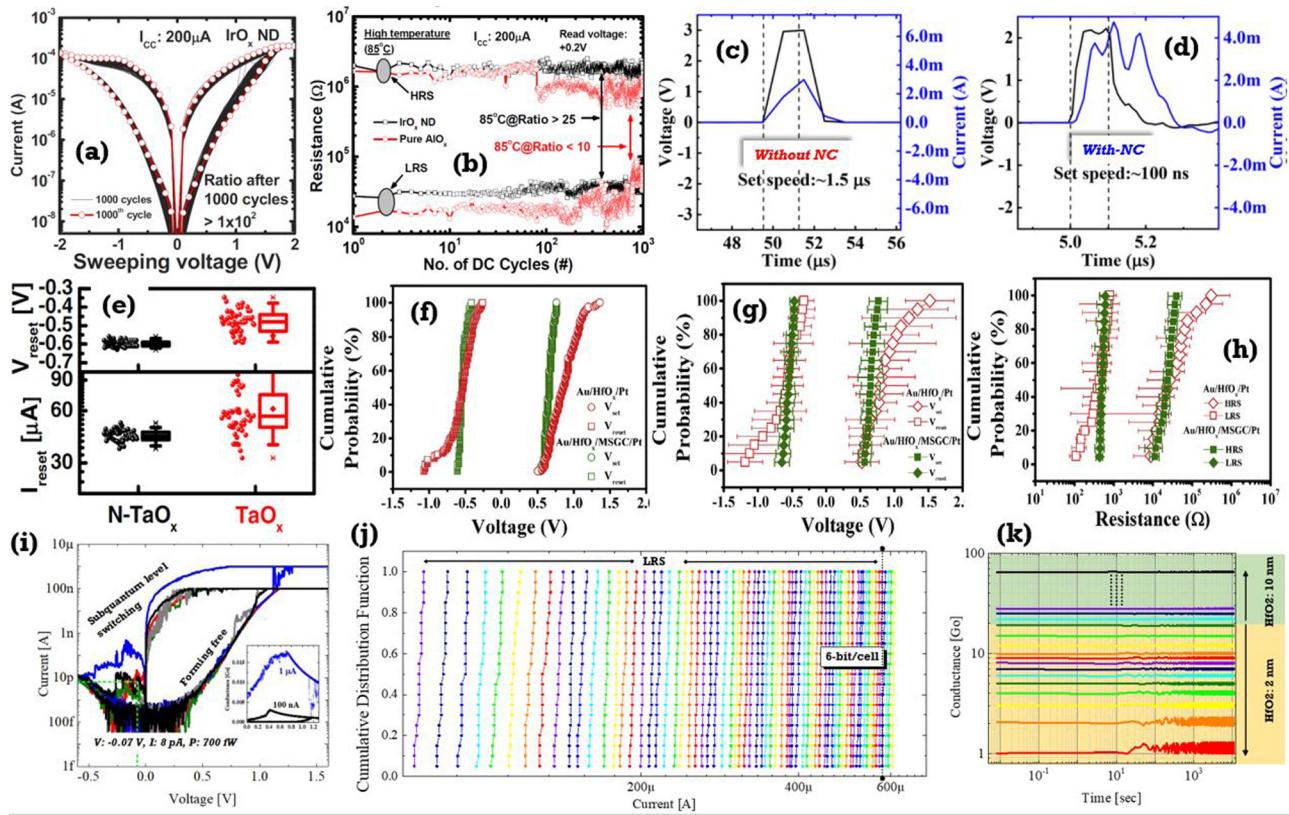


FIG. 6. (a) and (b) Highly improved electrical performance by using $\text{Al}_2\text{O}_3/\text{IrO}_x$ -NCs/ Al_2O_3 -based RRAM devices compared to Al_2O_3 -based RRAM devices. Even high temperature behavior with NCs can show very stable performance. Reproduced with permission from Banerjee and Maikap, *Proceedings of Technical Program of VLSI Technology, System and Application* (IEEE, 2012), pp. 493–496. Copyright 2012 IEEE Publishing. (c) and (d) High-speed switching can be observed for the NC-based HfO_2 -RRAM devices. Because of the improved electric field as compared to without NCs, the NC-RRAM devices can be used for high-speed operation. Reproduced with permission from Wu *et al.*, *Appl. Phys. Lett.* **113**(2), 023105 (2018). Copyright 2018 AIP Publishing LLC. (e) Improvement of device operation conditions with nitrogen doping in TaO_x RRAM devices. Reproduced with permission from Misha *et al.*, *ECS Solid State Lett.* **4**(3), P25–P28 (2015). Copyright 2015 Author(s), licensed under CC. (f)–(h) Improvement of electrical performance of $\text{Au/HfO}_x/\text{Pt}$ -based RRAM devices with a mountainlike electrode design. The method can improve the cycle-to-cycle and device-to-device performance. Reproduced with permission from Tao *et al.*, *Appl. Surf. Sci.* **440**, 107–112 (2018). Copyright 2018 Elsevier Publishing. (i)–(k) Forming free $I-V$ switching at a current level of 100nA with Ti-interfacial barrier layer engineering in $\text{Cu/Ti}/\text{HfO}_2/\text{TiN}$ RRAM and 6-bit/cell storage capability of the same device. Reproduced with permission from Banerjee and Hwang, *Adv. Electron. Mater.* **5**, 1900744 (2019). Copyright 2019 John Wiley and Sons Publishing.

solve several problems associated with artificial intelligence. Prior to the successful implementation of a neuromorphic device on hardware, it is essential to design an electronic neuron that mimics bioneurons' capability and electronic synapse that emulates the behavior of biosynapse. For that, a high-density low-power device with at-least 5-bits/cell storage is necessary. RRAM is an obvious choice in that category. A prototype of such a memristive neural network of 8×8 1T1R array based on a defect-engineered Ag-doped SiO_xN_y layer is shown in Figs. 7(a)–7(c).¹⁵¹ With a special learning protocol and a peripheral circuit design, the synaptic weight update was demonstrated [Figs. 7(d)–7(f)]. It is possible to emulate both the short-term and long-term synaptic plasticity using Ag-doped RRAM devices based on MgO_x , SiO_xN_y , and HfO_x .²⁰ Figure 7(g) shows the paired-pulse measurement of such devices. Additionally, spike-timing-dependent plasticity (STDP) has

been demonstrated in Fig. 7(h). Previously, many research works have identified the application of such RRAM devices for neuromorphic computing. Several groups have reviewed such applications.

Hardware security has become extremely important in the era of IoT. So far, the randomness of RRAM devices have extended their applications in the security domain such as physical unclonable functions (PUFs) and true random number generators (TRNGs). In such devices, intrinsic stochasticity is the major source of entropy changes or randomness. Random numbers are extremely useful for generating cryptographic keys. In the last decade, RRAM technology has been established as a most promising robust, low-power emerging NVM with a broad range of applications. Though RRAM devices have attractive properties, the reliability and variability issues are still among the major challenges for memory type applications. However, the grass is still greener on

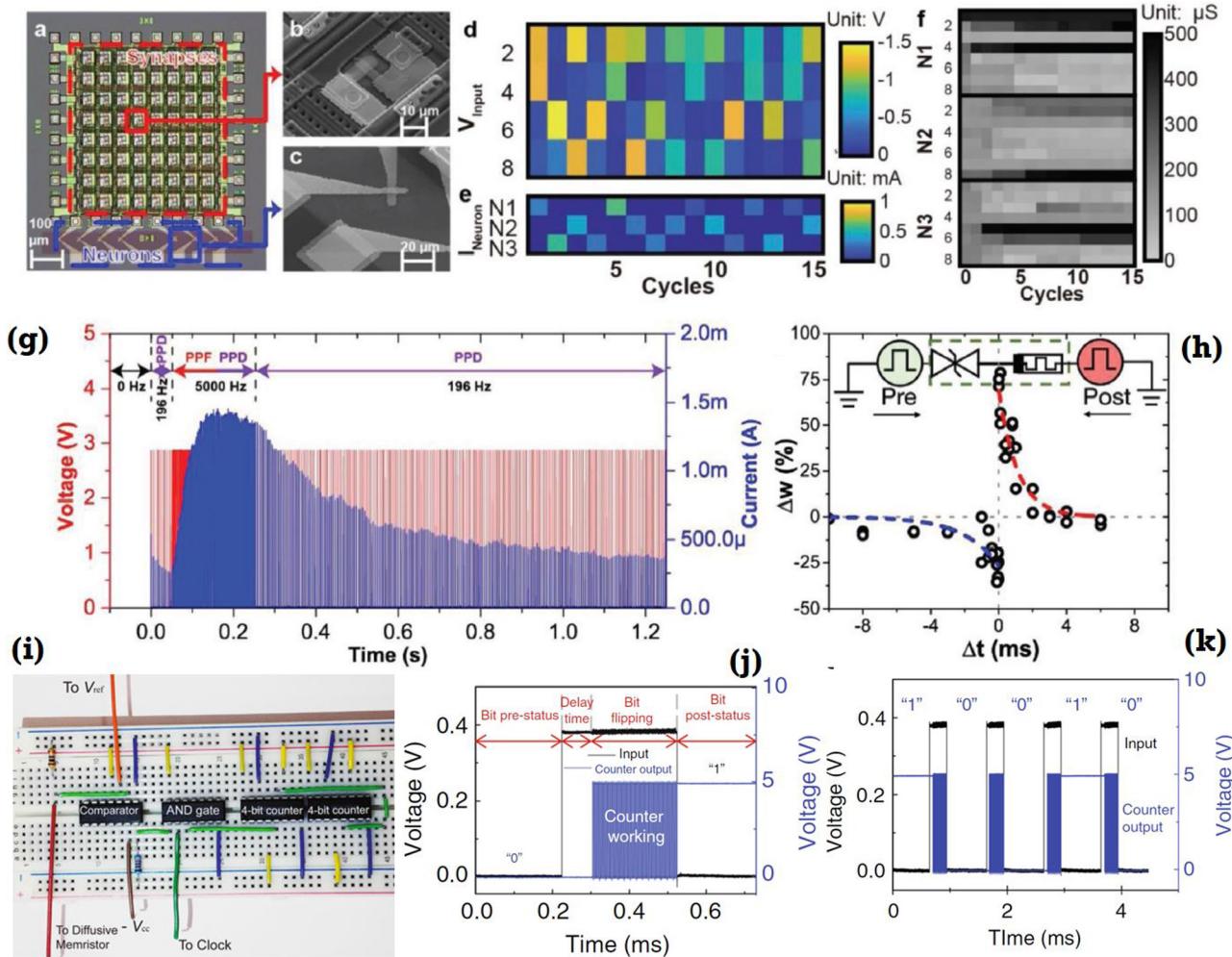


FIG. 7. (a) Optical image of a typical 8×8 1T1R memristive neural network. The scanning electron microscope image of (b) 1T1R cell and (c) a single 1R. (d)–(f) the input pattern, peak neural current, and synaptic weight at each training cycle, respectively. Reproduced with permission from Upadhyay *et al.*, *Adv. Mater. Technol.* **4**, 1800589 (2019). Copyright 2019 John Wiley and Sons Publishing. (i) Image of circuital arrangement of a volatile diffusive memristor device. (j) One counter output in response to 1 kHz input voltage pulse. (k) Random binary out flipping states over continuous switching cycles. Reproduced with permission from Jiang *et al.*, *Nat. Commun.* **8**, 882 (2017). Copyright 2015 Author(s), licensed under CC.

the other side, and this random behavior is extremely useful in stochastic computing and hardware security applications.^{152–154} A TRNG can be realized using cycle-to-cycle variations of LRS or HRS and also using device-to-device variations. Along with the simple oxide-based RRAM devices, defect-engineered RRAM devices are also studied for TRNG applications. Jiang *et al.*¹⁵⁵ demonstrated a TRNG using volatile type diffusive RRAM devices, which relies on the diffusion dynamics of metal atoms in an Ag-doped SiO₂-based RRAM structure. Figures 7(i)–7(k) show a typical circuital arrangement of such a system consisting of only a Ag-doped diffusive memristor, a comparator, an AND-gate, and a counter. The intrinsic stochasticity of the delay time has been used as the source of entropy to build a TRNG that can pass all 15 NIST

Special Publication 800-22 randomness tests. There are a variety of analog and digital circuits that harness the physical processes, and, therefore, natural entropy, for generating randomness.

V. CONCLUDING REMARKS

In conclusion, RRAM is an emerging technology that has plenty of opportunities to enable useful nonvolatile memory devices in the near future.^{156–158} The attractive defect-physics is very suitable to improve the performance of ECM, VCM, and molecular RRAM devices. Defect engineering can be done in several ways such as doping of the oxide layer, nanocrystal-based switching layer design, embedded metals in switching oxide, and

defective electrode design. Defects in RRAM can play an important role in several ways such as improving the localization of the electric field, increasing the charge trapping ability, and also it can serve for different purposes based on the structure design.

Defect engineering can be influenced by the material, size, shape, and configuration. Moreover, it is difficult to control defect distribution from device to device. For example, although the cycle-to-cycle switching reliability for a single NC-based RRAM device can improve, the device-to-device variation of NCs' size, shape, and density can lead to device-level fluctuations of resistive switching parameters. Scalability is one of the major advantages of RRAM, which has a potential to hit the atomic level. Hence, controlling the size of NCs in such an atomic scale is another vital challenge. In the sandwich form, it can improve the performance; however, realization of the physics behind the switching process of such devices is complicated.

One of the major advantages of defect engineering of RRAM devices is the improvement of the localized electric field, which is also possible with a nanostructure electrode design. As the device size of RRAM is scaled down to several nanometer ranges, controlling the size and shape of the nanostructure electrode is very critical. However, depending on the requirements and applications, defects in the RRAM devices can be engineered. *In a controlled manner, defects are tremendous possibilities for memory and neuromorphic applications, as they can provide stable and controlled switching. In an uncontrolled way, defects are essential to introduce randomness and entropy change during switching and are useful for hardware security applications.*

ACKNOWLEDGMENTS

The authors are thankful to Dr. An Chen for fruitful discussion. This work was supported by the National Research Foundation of Korea funded by the Korea government (MSIT) (Grant No. NRF-2018R1A3B1052693).

REFERENCES

- ¹Q. Xia and J. J. Yang, *Nat. Mater.* **18**, 309–323 (2019).
- ²M. A. Zidan, J. P. Strachan, and W. D. Lu, *Nat. Electron.* **1**, 22–29 (2018).
- ³C. Sung, H. Hwang, and I. K. Yoo, *J. Appl. Phys.* **124**, 151903 (2018).
- ⁴C. Du, W. Ma, T. Chang, P. Sheridan, and W. D. Lu, *Adv. Funct. Mater.* **25**(27), 4290–4299 (2015).
- ⁵S. Park, J. Noh, M. Choo, A. M. Sheri, M. Chang, Y.-B. Kim, C. J. Kim, M. Jeon, B.-G. Lee, and B. H. Lee, *Nanotechnology* **24**, 384009 (2013).
- ⁶Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, and X. J. Zhu, *Adv. Funct. Mater.* **22**, 2759–2765 (2012).
- ⁷C. Mead, *Proc. IEEE* **78**, 1629–1636 (1990).
- ⁸G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis, and T. Prodromakis, *Nanotechnology* **24**, 384010 (2013).
- ⁹J. Kim, A. J. Hong, S. M. Kim, K.-S. Shin, E. B. Song, Y. Hwang, F. Xiu, K. Galatsis, C. O. Chui, and R. N. Candler, *Nanotechnology* **22**, 254006 (2011).
- ¹⁰P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, *Science* **345**(6197), 668–673 (2014).
- ¹¹T. M. Wong, R. Preissl, P. Datta, M. Flickner, R. Singh, S. K. Esser, E. McQuinn, R. Appuswamy, W. P. Risk, H. D. Simon, and D. S. Modha, IBM Research Report RJ10502 (November 13, 2012), [https://domino.research.ibm.com/library/cyberdig.nsf/papers/19B9020D53E753DB85257AB7005FFA18/\\$File/RJ10502.pdf](https://domino.research.ibm.com/library/cyberdig.nsf/papers/19B9020D53E753DB85257AB7005FFA18/$File/RJ10502.pdf).
- ¹²R. Waser and M. Aono, *Nat. Mater.* **6**, 833–840 (2007).
- ¹³H. Lv, X. Xu, H. Liu, R. Liu, Q. Liu, W. Banerjee, H. Sun, S. Long, and M. Liu, *Sci. Rep.* **5**, 7764 (2015).
- ¹⁴W. Banerjee, Q. Liu, S. Long, H. Lv, and M. Liu, *J. Phys. D Appl. Phys.* **50**, 303002 (2017).
- ¹⁵Y. Li, Y. Zhong, L. Xu, J. Zhang, X. Xu, H. Sun, and X. Miao, *Sci. Rep.* **3**, 1619 (2013).
- ¹⁶T. Chang, S.-H. Jo, and W. Lu, *ACS Nano* **5**(9), 7669–7676 (2011).
- ¹⁷L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, and Q. Wan, *Nat. Commun.* **5**, 3158 (2014).
- ¹⁸Y. Li, L. Xu, Y.-P. Zhong, Y.-X. Zhou, S.-J. Zhong, Y.-Z. Hu, L. O. Chua, and X.-S. Miao, *Adv. Electron. Mater.* **1**, 1500125 (2015).
- ¹⁹P. M. Sheridan, F. Cai, C. Du, W. Ma, Z. Zhang, and W. D. Lu, *Nat. Nanotechnol.* **12**, 784–789 (2017).
- ²⁰Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, and J. J. Yang, *Nat. Mater.* **16**, 101–108 (2017).
- ²¹W. Banerjee, X. Xu, H. Liu, H. Lv, Q. Liu, H. Sun, S. Long, and M. Liu, *IEEE Electron Device Lett.* **36**(4), 333–335 (2015).
- ²²J. J. Yang, D. B. Strukov, and D. R. Stewart, *Nat. Nanotechnol.* **8**, 13–24 (2013).
- ²³C. Wang, H. Wu, B. Gao, T. Zhang, Y. Yang, and H. Qian, *Microelectron. Eng.* **187–188**, 121–133 (2018).
- ²⁴T.-C. Chang, K.-C. Chang, T.-M. Tsai, T.-J. Chu, and S. M. Sze, *Mater. Today* **19**, 254–264 (2016).
- ²⁵W. Banerjee and H. Hwang, *Adv. Electron. Mater.* **5**, 1900744 (2019).
- ²⁶W. Banerjee, X. Zhang, Q. Luo, H. Lv, Q. Liu, S. Long, and M. Liu, *Adv. Electron. Mater.* **4**(2), 1700561 (2018).
- ²⁷B. C. Jang, S. Kim, S. Y. Yang, J. Park, J.-H. Cha, J. Oh, J. Choi, S. G. Im, V. P. Dravid, and S.-Y. Choi, *Nano Lett.* **19**, 839 (2019).
- ²⁸H. Lv, X. Xu, P. Sun, H. Liu, Q. Luo, Q. Liu, W. Banerjee, H. Sun, S. Long, L. Li, and M. Liu, *Sci. Rep.* **5**, 13311 (2015).
- ²⁹W. Banerjee, F. Wu, Y. Hu, Q. Wu, Z. Wu, Q. Liu, and M. Liu, *Appl. Phys. Lett.* **112**(13), 133108 (2018).
- ³⁰X. Xu, L. Tai, T. Gong, J. Yin, P. Huang, J. Yu, D. N. Dong, Q. Luo, J. Liu, Z. Yu, X. Zhu, X. L. Wu, Q. Liu, H. Lv, and M. Liu, in *IEEE International Electron Device Meeting* (IEEE, 2018), p. 464.
- ³¹S. Lim, C. Sung, H. Kim, T. Kim, J. Song, J.-J. Kim, and H. Hwang, *IEEE Electron Device Lett.* **39**, 312 (2018).
- ³²L. Zhu, J. Zhou, Z. Guo, and Z. Sun, *J. Materomics* **1**, 285–295 (2015).
- ³³S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, and Q. Xia, *Nat. Nanotechnol.* **14**, 35–39 (2019).
- ³⁴B. J. Choi, A. C. Torrezan, J. P. Strachan, P. G. Kotula, A. J. Lohn, M. J. Marinella, Z. Li, R. S. Williams, and J. J. Yang, *Adv. Funct. Mater.* **26**, 5290–5296 (2016).
- ³⁵J. Y. Seok, S. J. Song, J. H. Yoon, K. J. Yoon, T. H. Park, D. E. Kwon, H. Lim, G. H. Kim, D. S. Jeong, and C. S. Hwang, *Adv. Funct. Mater.* **24**, 5316–5339 (2014).
- ³⁶C. Wang, D. Feng, W. Tong, J. Liu, Z. Li, J. Chang, Y. Zhang, B. Wu, J. Xu, W. Zhao, Y. Li, and R. Ren, *ACM Trans. Des. Autom. Electron. Syst.* **24**, 46 (2019).
- ³⁷W. Banerjee, N. Lu, Y. Yang, L. Li, H. Lv, Q. Liu, S. Long, and M. Liu, *IEEE Trans. Electron Dev.* **65**(3), 957–962 (2018).
- ³⁸W. Banerjee, X. Xu, H. Lv, Q. Liu, S. Long, and M. Liu, *Adv. Electron. Mater.* **3**(12), 1700287 (2017).
- ³⁹Q. Luo, X. Xin, H. Liu, H. Lv, T. Gong, S. Long, Q. Liu, H. Sun, W. Banerjee, L. Li, H. Gao, N. Lu, and M. Liu, *Nanoscale* **8**, 15629 (2016).
- ⁴⁰S. Kim, J. Zhou, and W. D. Lu, *IEEE Trans. Electron Dev.* **61**, 2820–2826 (2014).
- ⁴¹K. Moon, S. Lim, J. Park, C. Sung, S. Oh, J. Woo, J. Lee, and H. Hwang, *Faraday Discuss.* **213**, 421 (2019).
- ⁴²W. Banerjee, Q. Liu, H. Lv, S. Long, and M. Liu, *Nanoscale* **9**(38), 14442–14450 (2017).

- ⁴³D. Ielmini, *Microelectron. Eng.* **190**, 44–53 (2018).
- ⁴⁴Y. Li, Z. Wang, R. Midya, Q. Xia, and J. J. Yang, *J. Phys. D Appl. Phys.* **51**, 503002 (2018).
- ⁴⁵D. Lee, M. Kwak, K. Moon, W. Choi, J. Park, J. Yoo, J. Song, S. Lim, C. Sung, W. Banerjee, and H. Hwang, *Adv. Electron. Mater.* **5**, 1800866 (2019).
- ⁴⁶G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. Le Gallo, K. Moon, J. Woo, H. Hwang, and Y. Leblebici, *Adv. Phys. X* **2**, 89–124 (2017).
- ⁴⁷M. K. F. Lee, Y. Cui, T. Somu, T. Luo, J. Zhou, W. T. Tang, W.-F. Wong, and R. S. M. Goh, *ACM Trans. Archit. Code Optim.* **15**, 64 (2019).
- ⁴⁸Q. Wu, H. Wang, Q. Luo, W. Banerjee, J. Cao, X. Zhang, F. Wu, Q. Liu, L. Li, and M. Liu, *Nanoscale* **10**(13), 5875–5881 (2018).
- ⁴⁹A. Burg, A. Chattopadhyay, and K.-Y. Lam, *Proc. IEEE* **106**, 38–60 (2018).
- ⁵⁰J. Rajendran, R. Karri, J. B. Wendt, M. Potkonjak, N. McDonald, G. S. Rose, and B. Wysocki, *Proc. IEEE* **103**, 829–849 (2015).
- ⁵¹T. Calzecchi-Onesti, *Il Nuovo Cimento* **16**, 58–64 (1884).
- ⁵²T. W. Hickmott, *J. Appl. Phys.* **33**, 2669–2682 (1962).
- ⁵³L. O. Chua, *IEEE Trans. Circuit Theory* **18**, 507–519 (1971).
- ⁵⁴D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, *Nature* **453**, 80–83 (2008).
- ⁵⁵W. Banerjee and Q. Liu, in *Nanocrystals in Nonvolatile Memory*, edited by W. Banerjee (Pan Stanford Publishing, 2018), pp. 389–468.
- ⁵⁶J. Sun, Q. Liu, H. Xie, X. Wu, F. Xu, T. Xu, S. Long, H. Lv, Y. Li, L. Sun, and M. Liu, *Appl. Phys. Lett.* **102**, 053502 (2013).
- ⁵⁷C. Pearson, L. Bowen, M.-W. Lee, A. L. Fisher, K. E. Linton, M. R. Bryce, and M. C. Petty, *Appl. Phys. Lett.* **102**, 213301 (2013).
- ⁵⁸P. Peng, D. Xie, Y. Yang, Y. Zang, X. Gao, C. Zhou, T. Feng, H. Tian, T. Ren, and X. Zhang, *J. Appl. Phys.* **111**, 084501 (2012).
- ⁵⁹Z. Wang, P. B. Griffin, J. McVittie, S. Wong, P. C. McIntyre, and Y. Nishi, *IEEE Electron Dev. Lett.* **28**, 14 (2007).
- ⁶⁰X. Zhu, W. Su, Y. Liu, B. Hu, L. Pan, W. Lu, J. Zhang, and R.-W. Li, *Adv. Mater.* **24**, 3941 (2012).
- ⁶¹C. N. Peng, C. W. Wang, T. C. Chan, W. Y. Chang, Y. C. Wang, H. W. Tsai, W. W. Wu, L. J. Chen, and Y. L. Chueh, *Nanoscale Res. Lett.* **7**, 559 (2012).
- ⁶²Y. C. Yang, F. Pan, F. Zeng, and M. Liu, *J. Appl. Phys.* **106**, 123705 (2009).
- ⁶³W. Banerjee, S. Maikap, C. S. Lai, Y. Y. Chen, T. C. Tien, H. Y. Lee, W. S. Chen, F. T. Chen, M. J. Kao, M. J. Tsai, and J.-R. Yang, *Nanoscale Res. Lett.* **7**, 194 (2012).
- ⁶⁴L. D. Bozano, B. W. Kean, V. R. Deline, J. R. Salem, and J. C. Scott, *Appl. Phys. Lett.* **84**, 607 (2004).
- ⁶⁵Z. B. Yan and J.-M. Liu, *Sci. Rep.* **3**, 2482 (2013).
- ⁶⁶X. Guo, C. Schindler, S. Menzel, and R. Waser, *Appl. Phys. Lett.* **91**, 133513 (2007).
- ⁶⁷M. N. Kozicki and M. Mitkova, *J. Non Cryst. Solids* **352**, 567 (2006).
- ⁶⁸A. Gubicza, D. Z. Manrique, L. Posa, C. J. Lambert, G. Mihaly, M. Csontos, and A. Halbritter, *Sci. Rep.* **6**, 30775 (2016).
- ⁶⁹S. J. Choi, G. S. Park, K. H. Kim, S. Cho, W. Y. Yang, X. S. Li, J. H. Moon, K. J. Lee, and K. Kim, *Adv. Mater.* **23**, 3272 (2011).
- ⁷⁰T. Fujii, M. Arita, Y. Takahashi, and I. Fujiwara, *Appl. Phys. Lett.* **98**, 212104 (2011).
- ⁷¹Q. Liu, J. Sun, H. Lv, S. Long, K. Yin, N. Wan, Y. Li, L. Sun, and M. Liu, *Adv. Mater.* **24**, 1844–1849 (2012).
- ⁷²B. Cho, J.-M. Yun, S. Song, Y. Ji, D.-Y. Kim, and T. Lee, *Adv. Funct. Mater.* **21**(20), 3976–3981 (2011).
- ⁷³Z. Xu, Y. Bando, W. Wang, X. Bai, and D. Golberg, *ACS Nano* **4**, 2515 (2010).
- ⁷⁴X. Tian, S. Yang, M. Zeng, L. Wang, J. Wei, Z. Xu, W. Wang, and X. Bai, *Adv. Funct. Mater.* **26**, 3649–3654 (2014).
- ⁷⁵S. Gao, C. Song, C. Chen, F. Zeng, and F. Pan, *Appl. Phys. Lett.* **102**, 141606 (2013).
- ⁷⁶J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, and R. S. Williams, *Nat. Nanotechnol.* **3**, 429 (2008).
- ⁷⁷C. Yoshida, K. Kinoshita, T. Yamasaki, and Y. Sugiyama, *Appl. Phys. Lett.* **93**, 042106 (2008).
- ⁷⁸W. Banerjee, W. F. Cai, X. Zhao, Q. Liu, H. Lv, S. Long, and M. Liu, *Nanoscale* **9**(47), 18908–18917 (2017).
- ⁷⁹C. Chen, C. Song, J. Yang, F. Zeng, and F. Pan, *Appl. Phys. Lett.* **100**, 253509 (2012).
- ⁸⁰W. Banerjee, S. Z. Rahaman, A. Prakash, and S. Maikap, *Jpn. J. Appl. Phys.* **50**, 10PH01 (2011).
- ⁸¹S. Won, S. Y. Lee, J. Park, and H. Seo, *Sci. Rep.* **7**, 10186 (2017).
- ⁸²C. Chen, Y. C. Yang, F. Zeng, and F. Pan, *Appl. Phys. Lett.* **97**, 083502 (2010).
- ⁸³H.-D. Kim, H.-M. An, and T. G. Kim, *IEEE Trans. Electron Dev.* **59**, 2302 (2012).
- ⁸⁴J. Kim, C. Ko, A. Frenzel, S. Ramanathan, and J. E. Hoffman, *Appl. Phys. Lett.* **96**, 213106 (2010).
- ⁸⁵X. Liu, S. M. Sadaf, M. Son, J. Shin, J. Park, J. Lee, S. Park, and H. Hwang, *Nanotechnology* **22**(47), 475702 (2011).
- ⁸⁶F. Nakamura, M. Sakaki, Y. Yamanaka, S. Tamaru, T. Suzuki, and Y. Maeno, *Sci. Rep.* **3**, 2536 (2013).
- ⁸⁷Y. Zhou and S. Ramanathan, *Proc. IEEE* **103**(8), 1289–1310 (2015).
- ⁸⁸K. M. Kim, D. S. Jeong, and C. S. Hwang, *Nanotechnology* **22**(25), 254002 (2011).
- ⁸⁹J.-Y. Chen, C.-L. Hsin, C.-W. Huang, C.-H. Chiu, Y.-T. Huang, S.-J. Lin, W.-W. Wu, and L.-J. Chen, *Nano Lett.* **13**, 3671–3677 (2013).
- ⁹⁰X. T. Zhang, Q. X. Yu, Y. P. Yao, and X. G. Li, *Appl. Phys. Lett.* **97**, 222117 (2010).
- ⁹¹M. Hasan, R. Dong, H. Choi, D. Lee, D.-J. Seong, M. Pyun, and H. Hwang, *Appl. Phys. Lett.* **92**, 202102 (2008).
- ⁹²L. Liu, S. Zhang, Y. Luo, G. Yuan, J. Liu, J. Yin, and Z. Liu, *J. Appl. Phys.* **111**, 104103 (2012).
- ⁹³X. Zhao, S. Liu, J. Niu, L. Liao, Q. Liu, X. Xiao, H. Lv, S. Long, W. Banerjee, W. Li, S. Si, and M. Liu, *Small* **13**(35), 1603948 (2017).
- ⁹⁴S. Liu, N. Lu, X. Zhao, H. Xu, W. Banerjee, H. Lv, S. Long, Q. Li, Q. Liu, and M. Liu, *Adv. Mater.* **28**(48), 10623–10629 (2016).
- ⁹⁵F. Hui, E. Grustan-Gutierrez, S. Long, Q. Liu, A. K. Ott, A. C. Ferrari, and M. Lanza, *Adv. Electron. Mater.* **3**, 1600195 (2017).
- ⁹⁶C. Pan, E. Miranda, M. A. Villena, N. Xiao, X. Jing, X. Xie, T. Wu, F. Hui, Y. Shi, and M. Lanza, *2D Mater.* **4**(2), 025099 (2017).
- ⁹⁷Z. Wu, X. Zhao, Y. Yang, W. Wang, X. Zhang, R. Wang, R. Cao, Q. Liu, and W. Banerjee, *Nanoscale Adv.* **1**(9), 3753–3760 (2019).
- ⁹⁸Y. Bai, H. Wu, K. Wang, R. Wu, L. Song, T. Li, J. Wang, Z. Yu, and H. Qian, *Sci. Rep.* **5**, 13785 (2015).
- ⁹⁹D. Lee, D.-J. Seong, H. J. Choi, I. Jo, R. Dong, W. Xiang, S. Oh, M. Pyun, S.-O. Seo, S. Heo, M. Jo, D.-K. Hwang, H. K. Park, M. Chang, M. Hasan, and H. Hwang, in *Technical Digest—International Electron Devices Meeting (IEDM)* (IEEE, 2006).
- ¹⁰⁰W. Kim, S. I. Park, Z. Zhang, Y. Y. Liauw, D. Sekar, H.-S. P. Wong, and S. S. Wong, in *Symposium on VLSI Technology—Digest of Technical Papers* (IEEE, 2011), pp. 22–23.
- ¹⁰¹Q. Liu, S. Long, W. Wang, Q. Zuo, S. Zhang, J. Chen, and M. Liu, *IEEE Electron Device Lett.* **30**(12), 1335–1337 (2009).
- ¹⁰²S. H. Misha, N. Tamanna, J. Woo, S. Lee, J. Song, J. Park, S. Lim, J. Park, and H. Hwang, *ECS Solid State Lett.* **4**(3), P25–P28 (2015).
- ¹⁰³L. Chen, H.-Y. Gou, Q.-Q. Sun, P. Zhou, H.-L. Lu, P.-F. Wang, S.-J. Ding, and D. W. Zhang, *IEEE Electron Device Lett.* **32**(6), 794 (2011).
- ¹⁰⁴W. Banerjee, S. Maikap, S. Z. Rahaman, A. Prakash, T.-C. Tien, W.-C. Li, and J.-R. Yang, *J. Electrochem. Soc.* **159**, H177–H182 (2012).
- ¹⁰⁵C. H. Cheng, P. C. Chen, Y. H. Wu, F. S. Yeh, and A. Chin, *IEEE Electron Device Lett.* **32**, 1749–1751 (2011).
- ¹⁰⁶Y. Wang, Q. Liu, H. Lü, S. Long, W. Wang, Y. T. Li, S. Zhang, W. T. Lian, J. H. Yang, and M. Liu, *Chin. Sci. Bull.* **57**, 1235 (2012).
- ¹⁰⁷Y. C. Ju, S. Kim, T.-G. Seong, S. Nahm, H. Chung, K. Hong, and W. Kim, *Small* **8**(18), 2849–2855 (2012).
- ¹⁰⁸J.-D. Kim, Y.-J. Baek, Y. J. Choi, C. J. Kang, H. H. Lee, H.-M. Kim, K.-B. Kim, and T.-S. Yoon, *J. Appl. Phys.* **114**, 224505 (2013).
- ¹⁰⁹S. Zhong, S. Duan, and Y. Cui, *RSC Adv.* **4**, 40924 (2014).

- ¹¹⁰L. Courtade, C. Turquat, C. Muller, J. G. Lisoni, L. Goux, D. J. Wouters, D. Goguenheim, P. Roussel, and L. Ortega, *Thin Solid Films* **516**(12), 4083–4092 (2007).
- ¹¹¹W. Banerjee, S. Maikap, T.-C. Tien, W.-C. Li, and J.-R. Yang, *J. Appl. Phys.* **110**, 074309 (2011).
- ¹¹²W.-Y. Chang, K.-J. Cheng, J.-M. Tsai, H.-J. Chen, F. Chen, M.-J. Tsai, and T.-B. Wu, *Appl. Phys. Lett.* **95**, 042104 (2009).
- ¹¹³M. Uenuma, K. Kawano, B. Zheng, N. Okamoto, M. Horita, S. Yoshii, I. Yamashita, and Y. Uraoka, *Nanotechnol.* **22**, 215201 (2011).
- ¹¹⁴J. Volatron, F. Carn, J. Kolosnjaj-Tabi, Y. Javed, Q. L. Vuong, Y. Gossuin, C. Ménager, N. Luciani, G. Charron, M. Hémadi, D. Alloyeau, and F. Gazeau, *Small* **13**, 1602030 (2016).
- ¹¹⁵H.-A. Hosein, D. R. Strongin, M. Allen, and T. Douglas, *Langmuir* **20**(23), 10283–10287 (2004).
- ¹¹⁶M. Okuda, K. Iwahori, I. Yamashita, and H. Yoshimura, *Biotechnol. Bioeng.* **84**, 187–194 (2003).
- ¹¹⁷S.-H. Lyu and J.-S. Lee, *J. Mater. Chem.* **22**, 1852 (2011).
- ¹¹⁸C.-Y. Lin, M.-H. Lin, M.-C. Wu, C.-H. Lin, and T. Y. Tseng, *IEEE Electron Device Lett.* **29**(10), 1108–1111 (2008).
- ¹¹⁹Y. Wang, Q. Liu, S. Long, W. Wang, Q. Wang, M. Zhang, S. Zhang, Y. Li, Q. Zuo, J. Yang, and M. Liu, *Nanotechnology* **21**, 045202 (2010).
- ¹²⁰M.-H. Lin, M.-C. Wu, C.-H. Lin, and T.-Y. Tseng, *Appl. Phys. Lett.* **107**, 124117 (2010).
- ¹²¹Q. Liu, S. Long, H. Lv, W. Wang, J. Niu, Z. Huo, J. Chen, and M. Liu, *ACS Nano* **4**(10), 6162 (2010).
- ¹²²S.-C. Qin, R.-X. Dong, and X.-L. Yan, *Appl. Phys. A* **118**(2), 605–612 (2015).
- ¹²³H.-D. Kim, M. J. Yun, S. M. Hong, and T. G. Kim, *Nanotechnology* **25**, 125201 (2014).
- ¹²⁴Y.-C. Huang, W.-L. Tsai, C.-H. Chou, C.-Y. Wan, C. Hsiao, and H.-C. Cheng, *IEEE Electron Device Lett.* **34**, 1244–1246 (2013).
- ¹²⁵S. Otsuka, T. Shimizu, S. Shingubara, K. Makihara, S. Miyazaki, A. Yamasaki, Y. Tanimoto, and K. Takase, *AIP Adv.* **4**, 087110 (2014).
- ¹²⁶Z. Wang, K. Zhao, H. Xu, L. Zhang, J. Ma, and Y. Liu, *Appl. Phys. Express* **8**, 014101 (2015).
- ¹²⁷H. W. Shin, J. H. Park, H. Y. Chung, K. H. Kim, H.-D. Kim, and T. G. Kim, *Appl. Phys. Express* **7**, 024202 (2014).
- ¹²⁸S. Park, K. Cho, and S. Kim, *Semicond. Sci. Technol.* **30**, 055019 (2015).
- ¹²⁹K.-Y. Shin, Y. Kim, F. V. Antolinez, J. S. Ha, S.-S. Lee, and J. H. Park, *Adv. Electron. Mater.* **2**, 1600233 (2016).
- ¹³⁰P.-K. Yang, C.-H. Ho, D.-H. Lien, J. R. D. Retamal, C.-F. Kang, K.-M. Chen, T.-H. Hua, Y.-C. Yu, C.-I. Wu, and J.-H. He, *Sci. Rep.* **5**, 15087 (2015).
- ¹³¹J. Lee, B. Yoo, H. Lee, G. D. Cha, H.-S. Lee, Y. Cho, S. Y. Kim, H. Seo, W. Lee, D. Son, M. Kang, H. M. Kim, Y. I. Park, T. Hyeon, and D.-H. Kim, *Adv. Mater.* **29**, 1603169 (2017).
- ¹³²Q. Hua, H. Wu, B. Gao, M. Zhao, Y. Li, X. Li, X. Hou, M.-F. Chang, P. Zhou, and H. Qian, *Adv. Sci.* **6**, 1900024 (2019).
- ¹³³R. S. Shenoy, G. W. Burr, K. Virwani, B. Jackson, A. Padilla, P. Narayanan, C. T. Rettner, R. M. Shelby, D. S. Bethune, K. V. Raman, M. BrightSky, E. Joseph, P. M. Rice, T. Topuria, A. J. Kellock, B. Kurdi, and K. Gopalakrishnan, *Semicond. Sci. Technol.* **29**(10), 104005 (2014).
- ¹³⁴W. Banerjee, X. Xu, H. Lv, Q. Liu, S. Long, and M. Liu, *ACS Omega* **2**, 6888–6895 (2017).
- ¹³⁵M. Zackriya, H. M. Kittur, and A. Chin, *Sci. Rep.* **7**, 42375 (2017).
- ¹³⁶Z. Wang, M. Rao, R. Midya, S. Joshi, H. Jiang, P. Lin, W. Song, S. Asapu, Y. Zhou, C. Li, H. Wu, Q. Xia, and J. J. Yang, *Adv. Funct. Mater.* **28**, 1704862 (2018).
- ¹³⁷X. P. Wang, Z. Fang, X. Li, B. Chen, B. Gao, J. F. Kang, Z. X. Chen, A. Kamath, N. S. Shen, N. Singh, G. Q. Lo, and D. L. Kwong, in *Proceedings of the IEEE International Electron Devices Meeting* (IEEE, 2012), pp. 493–496.
- ¹³⁸Z. Fang, X. P. Wang, X. Li, Z. X. Chen, A. Kamath, G. Q. Lo, and D. L. Kwong, *IEEE Trans. Electron Devices* **60**(3), 1108–1113 (2013).
- ¹³⁹E. Herrmann, A. Rush, T. Bailey, and R. Jha, *IEEE Trans. Electron Devices* **39**, 500–503 (2018).
- ¹⁴⁰T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, *Nat. Mater.* **10**, 591–595 (2011).
- ¹⁴¹W. Banerjee and S. Maikap, in *Proceedings of Technical Program of VLSI Technology, System and Application* (IEEE, 2012), pp. 493–496.
- ¹⁴²Q. Wu, W. Banerjee, J. Cao, Z. Ji, L. Li, and M. Liu, *Appl. Phys. Lett.* **113**(2), 023105 (2018).
- ¹⁴³B. Chakrabarti, M. A. Lastras-Montano, G. Adam, M. Prezioso, B. Hoskins, M. Payvand, A. Madhavan, A. Ghofrani, L. Theogarajan, K.-T. Cheng, and D. B. Strukov, *Sci. Rep.* **7**, 42429 (2017).
- ¹⁴⁴D. B. Strukov and R. S. Williams, *Proc. Natl. Acad. Sci. U.S.A.* **106**, 20155–20158 (2009).
- ¹⁴⁵N. Raghavan, D. D. Frey, M. Bosman, and K. L. Pey, *Microelectron. Reliab.* **55**, 1422–1426 (2015).
- ¹⁴⁶F. G. Aga, J. Woo, S. Lee, J. Song, J. Park, J. Park, S. Lim, C. Sung, and H. Hwang, *AIP Adv.* **6**, 025203 (2016).
- ¹⁴⁷B. Traoré, P. Blaise, E. Viabello, H. Grampeix, S. Jeannot, L. Perniola, B. D. Salvo, and Y. Nishi, *IEEE Trans. Electron Devices* **62**, 4029–4036 (2015).
- ¹⁴⁸M. Lanza, H.-S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. M. Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T.-H. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. C. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui, and Y. Shi, *Adv. Electron. Mater.* **5**, 1800143 (2019).
- ¹⁴⁹G. Molas, G. Sasseine, C. Nail, D. Alfaro Robayo, J.-F. Nodin, C. Cagli, J. Coignus, P. Blaise, and E. Nowak, *ECS Trans.* **86**(3), 35–47 (2018).
- ¹⁵⁰Y. Tao, W. Ding, Z. Wang, H. Xu, X. Zhao, X. Li, W. Liu, J. Ma, and Y. Liu, *Appl. Surf. Sci.* **440**, 107–112 (2018).
- ¹⁵¹N. K. Upadhyay, H. Jiang, Z. Wang, S. Asapu, Q. Xia, and J. J. Yang, *Adv. Mater. Technol.* **4**, 1800589 (2019).
- ¹⁵²A. Chen, *Proceedings of the IEEE International Electron Devices Meeting* (IEEE, 2015), pp. 265–268.
- ¹⁵³R. Liu, H. Wu, Y. Pang, H. Qian, and S. Yu, *IEEE Electron Devices Lett.* **36**, 1380–1383 (2015).
- ¹⁵⁴C. Y. Huang, W. C. Shen, Y. H. Tseng, Y. C. King, and C. J. Lin, *IEEE Electron Devices Lett.* **33**, 1108–1110 (2012).
- ¹⁵⁵H. Jiang, D. Belkin, S. E. Savel'ev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao, M. Barnell, Q. Wu, J. J. Yang, and Q. Xia, *Nat. Commun.* **8**, 882 (2017).
- ¹⁵⁶A. Chen, *Solid State Electron.* **125**, 25–38 (2016).
- ¹⁵⁷A. Chen, *J. Comput. Electron.* **16**, 1186–1200 (2017).
- ¹⁵⁸H. Wang and X. Yan, *Phys. Status Solidi RRL* **13**, 1900073 (2019).