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How Thin Practical Silicon Heterojunction Solar Cells Could Be? Experimental Study under 1 Sun and under Indoor Illumination

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The transition toward thinner microcrystalline silicon wafers for their potential performance gain has been of interest in recent years. Theoretical predictions have estimated a maximum efficiency for silicon wafers to be at about 100−110 µm thickness. The potential and losses in silicon heterojunction solar cells prepared on wafers with thickness in the range of 60−170 µm with focus on open-circuit voltage (V_{OC}) and fill factor (FF) are studied experimentally. The applicability of thinner wafers for low light and indoor applications using light emitting diode (LED) lighting is also studied. The implied V_{OC} (iV_{OC}) is observed to increase with a decrease in wafer thickness according to theoretical predictions with absolute values approaching the theoretical limit. Unlike the iV_{OC}, the implied FF is observed to decrease with wafer thickness reduction opposite to the theoretical predictions which are related to the effect of surface recombination. A combination of gains and losses results in a broad range of high efficiency under 1 sun for wafer thicknesses ranging from 75 to 170 µm with maximum of 22.3% obtained at 75 µm. As for indoor performance, thinner wafers show slightly better efficiency at lower light intensity under sun and LED illumination, promising improved performance for even thinner devices.

1. Introduction

Solar cells based on crystalline silicon have been largely improved over the past decades and represent the dominating technology in the current photovoltaic industry. Drastic cost reduction along with performance improvements[1] over the past decades has pushed the technology closer to its limitations[2–4] and consequently, makes further technical and economic progress on the solar cell level very challenging yet highly desirable. One of viable routes for improvement is a reduction of the wafer thickness which is related to several advantages. First of all, reduction in material usage per solar cell area is highly relevant for global mass production. Utilization of thinner-cut,[1,5] exfoliated,[6] or prepared-in-kerfless-ways[7,8] wafers leads to the production of a larger active solar cell area per kg of Si and therefore the potential reduction of cost and improvement of energy return on investment (ERoI).[1] At the same time, solar cells gain mechanical flexibility and suit better, for instance, the emerging building-integrated[9] or vehicle-integrated[10] applications. Solar cells based on thinner wafers require shorter diffusion lengths,[11] which make them less sensitive to bulk defect recombination, and with ideal surface passivation, their performance is more likely to approach the intrinsic limits.[12] This enhanced tolerance to bulk imperfections gives rise to the opportunity of producing higher efficiencies from low-cost materials such as the upgraded metallurgical-grade silicon.[13]

From the solar cell physics point of view, wafer thickness (W) is one of the key parameters for determining the limit of a crystalline silicon solar cell efficiency. The recent detailed studies on solar cell efficiency limits indicate that the reduction of the solar cell thickness below the modern standard of 170−180 µm can potentially increase the power conversion efficiency. Considering n-type wafers in the theoretical estimation of Richter et al., a maximum efficiency of 29.43% with an optimal thickness of ≈110 µm is reported.[2] In a later work, Veith-Wolf et al.[3] based on the calculations of Richter et al.[2] included

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deeper analyses of light trapping and concluded that even thinner, $W = 78.7\,\mu m$, wafers are expected to have maximum efficiency of 29.47% or n-doped c-Si. It has been demonstrated that reduction in wafer thickness is beneficial for the temperature coefficient of silicon heterojunction (SHJ) solar cells.[14] Departing from the standard 1 sun illumination, once indoor applications are addressed, it is predicted that significant reduction of thickness is beneficial.[15]

Reduction of wafer thickness, which is associated with optical loss, is compensated by increase in V_{OC} and fill factor (FF) due to the increase in excess carrier density.[2,3,11,16] As the thickness of the solar cell is reduced, the quasi-Fermi-level splitting of the electrons and holes increases, leading to the increase in V_{OC}. The increase in FF with decreasing thickness has two contributions. First is a straightforward rather geometrical dependence of FF on the V_{OC} estimated by Green[17] and revised by Leilaeioun et al.[18] The second effect is related to the Auger recombination limit. The thin c-Si solar cells with proper surface passivation approach the Auger limit of the V_{OC}. This implies that in the vicinity of V_{OC}, the local ideality factor (n_{id}) of the current–voltage ($I-V$) curve will approach the value of 2/3, steepening the $I-V$ curve, and therefore the limit of FF can surpass the usual FF of "ideal diode" with $n_{id} = 1$. The Auger recombination-limited lifetime leads to extraordinary FF values in simulations of Richter et al.,[2] Andreani et al.,[11] and Kowalczewski et al.,[16] which, depending on wafer thickness, exceeds the value expected from the ideal diode with ideality factor of 1 by 3–4 absolute percent. This potential has been demonstrated experimentally by Yoshikawa et al., where Suns–Voc data show pseudo-FF (pFF) of 85.6%,[19] which is greater than 85.4% predicted for an ideal diode at equivalent V_{OC} values. In other words, the thin solar cells with a high-quality passivation approach enter the Auger limit regime under 1 sun, which was usually just the case of concentrator devices.[20–22] Taking into account that SHJ solar cell technology provides a very high degree of surface passivation, this technology is of interest to explore how far the predicted efficiency gains with reduction in wafer thickness are attainable in practice.

In our work, we study the effect of wafer thickness on the performance of SHJ solar cells with a focus on the open-circuit voltage and FF. The potential and losses in experimental SHJ solar cells prepared on wafer with thickness in the range from 60 to 170 μm are investigated. To isolate or identify losses, the solar cells are investigated at different stages of preparation. In view of the promising predictions for thinner solar cells operating at 1 sun[2,3,11,16] and under low indoor irradiance,[15] the SHJ solar cells with different wafer thickness were studied under standard test conditions as well as under indoor LED illumination. Our results show a broad range of high efficiency under 1 sun for thicknesses ranging from 75 to 170 μm. Under reduced irradiance and especially under realistic indoor LED lighting, the thinner wafers show more promise for better performance.

2. Results and Discussion

2.1. Wafer Thickness Effect on Lifetime

The net sum of all losses due to recombination that takes place in a silicon wafer is described by the effective lifetime (τ_{eff}) of the wafer. In the context of this work, isolation of the bulk and surface contributions to the effective lifetime is of interest. A common expression for the effective lifetime with bulk and surface lifetime components is[23]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_B} + \frac{2S}{W} \tag{1}$$

where τ_B is the bulk lifetime, S is the surface recombination velocity, and W is the thickness of the wafer. The second part of the equation represents the inverse of the surface recombination lifetime. Although this conditional "spatial" separation of recombination channels does not describe types or mechanisms of recombination, it is typical that surface recombination is dominated by Shockley–Read–Hall (SRH) or trap-assisted mechanism[24,25] due to the high density of trap states at the surfaces and interfaces.[26,27] Recombination in the bulk of high-quality Si wafer is dominated by SRH or Auger mechanism depending on the injection level.[22] Although the surface recombination on the front and back surfaces can be different due to the different actions of n- and p-type layers, here, we assume an identical value for the sake of simplicity.

Figure 1 shows a plot of the inverse effective lifetime, $1/\tau_{eff}$, against the inverse wafer thickness of our prepared samples. It is evident that a decrease in wafer thickness leads to a decrease in the effective lifetime of the wafer. With a linear fit to the data shown in Figure 1, a bulk lifetime τ_B of ≈7.2 ms and a surface recombination velocity of ≈1.4 cm s^{-1} were determined from the intercept on $1/\tau_{eff}$ axis and the slope of the fitted red line. The increasing effect of surface recombination with reducing wafer thickness is clearly observed. Together with bulk lifetime which is factor 2–3 higher than the total effective lifetime, we can conclude that at the injection level of maximum power point the recombination in SHJ solar cells is dominated by surface SRH recombination. The influence of surface recombination is clearly visible at low injection levels in the dependencies of effective carrier lifetime on carrier density reconstructed from quasi-steady-state-photoconductance (QSSPC) measurements in **Figure 2**.

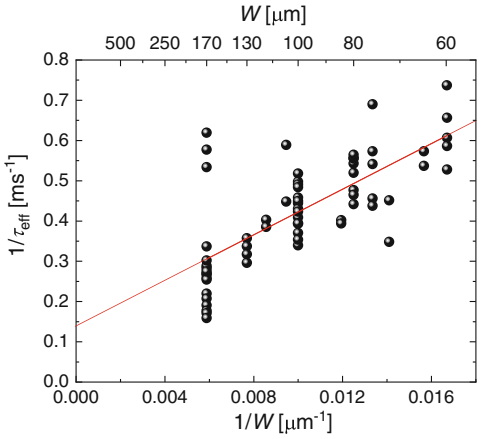

Figure 1. Inverse effective lifetime versus inverse wafer thickness. The bulk lifetime and the surface recombination velocity are determined from the intercept on $1/\tau_{eff}$ axis and the slope of the fitted red line, respectively.

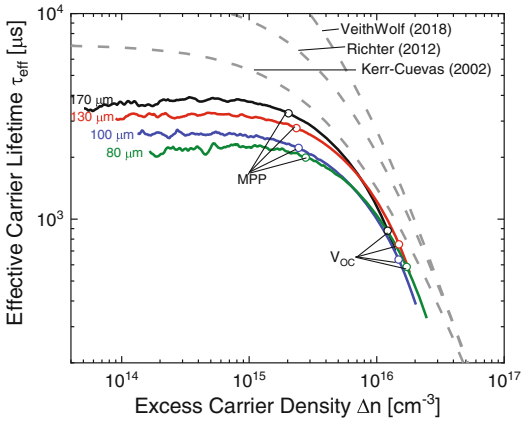

Figure 2. Effective carrier lifetime τ_{eff} versus excess carrier density at different thicknesses (80–170 µm with resistivity of ≈1 Ωcm). The dashed lines represent the Auger lifetime limit from different models at 1 Ωcm.[3,4,32]

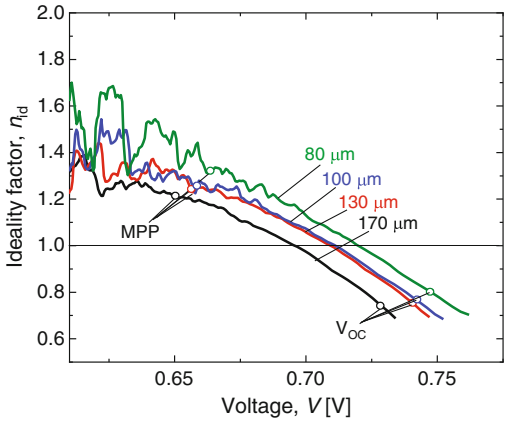

Figure 3. Differential ideality factor, n_{id}, as a function of voltage, V, for different wafer thicknesses W (80−170 µm), as indicated in the graph.

Here, the effective carrier lifetime reduces with decreased thickness for a broad range of excess carrier density, Δn, which is most pronounced at Δn below 5×10^{15} cm^{-3}. At low injection levels, τ_{eff} is limited by SRH recombination mostly at the surfaces. With reduction of wafer thickness, the surface recombination gains significance, thereby reducing τ_{eff} as the volume of Si bulk is reduced and imperfect surfaces get closer to each other. At higher injection conditions and at Δn above 10^{16} cm^{-3}, the effect of Auger recombination takes over and the influence of the wafer thickness becomes less significant. Auger recombination is governed by fundamental material properties and carrier density. We conducted simulations of the Auger-limited lifetime with PV lighthouse recombination calculator[28] using the bandgap narrowing parametrization by Schenk,[29] dopant ionization model by Altermatt et al.,[30] and radiative recombination model by Trupke et al.[31] The results of simulations are shown in Figure 2 for models by Kerr−Cuevas,[4] Richter,[32] and Veith-Wolf.[3] As it can be expected, the experimental lifetime is well below the Auger limit at low carrier density, where SRH recombination dominates. The simulated values of the τ_{eff} approach the experimental values at higher carrier density; however, there are still noticeable differences in values and slopes between the experimental data and simulation. The current device apparently requires a more detailed modeling to account for, for example, the carrier density distribution. In all four lifetime curves, the points of 1 sun-implied V_{OC} are deep in the "Auger regime"—the high-carrier-density region, where Auger recombination plays a dominating role. Here, it is expected that the theoretical predictions[2,3,11,16] based on Auger recombination limit are most relevant for the experimental data. At the same time, we can see in Figure 2 that the implied FF (*i*FF) points of all thicknesses are deep in the carrier density range dominated by SRH recombination; therefore, the predictions made with Auger limit are less relevant for the FF. In other words, the implied V_{OC} in high-quality SHJ solar cell precursors is very close to the fundamental Auger limit, whereas the *i*FF is to a large extent limited by the quality of the wafer passivation. An alternative way to present the transition between SRH and Auger recombination regimes is to calculate the differential ideality factor n_{id} using QSSPC data.

The differential ideality factor at different voltages was calculated from QSSPC measurements for the different wafer thicknesses and is shown in **Figure 3**. The $I-V$ characteristics dominated by SRH recombination have ideality factor ranging from 1 for low-injection to 2 for high-injection regimes, whereas a significantly lower value of 2/3 is characteristic for Auger recombination.[33] It is typical for real solar cell $I-V$s to have a dependence of the ideality factor on the voltage (on carrier density); therefore, it is instructive to examine the dependence of ideality factor on the carrier density for different wafer thicknesses.

The results in Figure 3 show a clear transition from $n > 1$ for low voltage (low carrier density) to $n_{id} = 1$ at 0.7−0.72 V with further reduction of n below 1 at higher voltage. For all implied V_{OC} points, an ideality factor of ≈0.7−0.8 is recorded, which indicates the dominating role of Auger recombination. At the same time, at the *i*FF points, n_{id} is ≈1.2−1.4, characteristic for SRH recombination regime.[18,33] The plot in Figure 3 clearly shows one of the key outcomes of the study. The iV_{OC} of the high-quality SHJ solar cell precursors is indeed far enough in the Auger-limited regime to be governed by the fundamental mechanism presented in the theoretical works,[2,3,11,16,32] whereas the *i*FF in the solar cell precursor is far from being governed by the fundamental limit.

There is another notable feature of the data shown in Figure 2, 3. From the pure Auger limit perspective, only the carrier density determines carrier lifetime, which implies that approaching the Auger region, the lifetime curves should converge into the same dependence on the carrier density. Even though dependencies in Figure 2 approach each other at the highest carrier density, they do not converge into the same dependence, which has also been observed for the numerous measurements during the present study. This is even more apparent in the differential ideality factor in Figure 3, where wafer thickness leads to a shift of dependence. The curves do not tend to converge into the same dependence at high voltage. These observations indicate that there is an additional effect, which has to be further investigated, to approach practical limits

of the SHJ solar cells even when Auger recombination dominates. It is likely that 0D predictions of Auger limit are not sufficient to describe the realistic SHJ device.

So far, the analysis was based on QSSPC lifetime measurements on the solar cell precursors. We explore the evolution of the solar cell parameters at major preparation steps up to the ready solar cell in the next sections

2.2. Open-Circuit Voltage

To obtain a high V_{OC}, it is important to first provide high excess charge carrier density, providing high quasi-Fermi-level splitting of the electrons and holes. Second, a high contact selectivity which is the ability of the contact to accept one type of charge carrier over the other is needed to extract these charge carriers at their corresponding terminals. The implied open-circuit voltage iV_{OC} gives the upper limit of the expected open-circuit voltage of the manufactured solar cell. The values of iV_{OC} calculated out of QSSPC effective lifetime data under 1 sun conditions are shown in **Figure 4**a, together with the theoretical predictions by Richter et al.[2] Here, a series of wafers with thicknesses ranging between 60 and 170 µm and resistivities between 1 and 3 Ωcm were studied. The iV_{OC} points shown were obtained after the deposition of the amorphous intrinsic and doped layers but before the deposition of ITO. The implied V_{OC} trend follows the theoretical predictions and increases with reduction in wafer thickness. Not only the trend but also the absolute values of iV_{OC} are very close to the theoretical limit. A high iV_{OC} value of 766 mV was obtained for a 60 µm wafer with resistivity of 2.2 Ωcm. This high value is very close to the V_{OC} limit modeled at 3 Ωcm by Richter et al.[2] After ITO depositions, very little losses in the iV_{OC} values were observed (not shown). However, a substantial voltage drop was observed for the actual V_{OC} values obtained after the solar cells were finalized with screen-printed contacts. This drop was especially significant at wafer thicknesses lower than 64 µm. Even though certain degradation of carrier lifetime after screen printing cannot be excluded, we believe that the difference between iV_{OC} and V_{OC} is related to imperfect operation of carrier-selective contacts. Among several mechanisms reported in the literature as listed by Dumbrell et al.,[34] the most relevant for SHJ solar cell technology is related to contact shadowing.[34–36] Light shadowing from the front contact leads to inhomogeneous generation of photocurrent, which results in internal currents from the open regions with high generation to the shadowed regions under metal contacts. The related voltage drop then is observed as the difference between iV_{OC} and externally measured V_{OC}. This shadowing effect is reported to be of particular significance in front-junction solar cells.[34–37] In the rear-junction solar cells studied in this work the significance of this effect needs additional confirmation. Finally, part of the difference between iV_{OC} and V_{OC} can be explained by imperfect selective function of doped layers—carrier selectivity of the contacts[38–40]—especially in the high-voltage case of thinned wafers. We argue that the reduction of externally measured V_{OC} compared with the iV_{OC}, that is, the internal chemical potential of electron–hole pairs, naturally

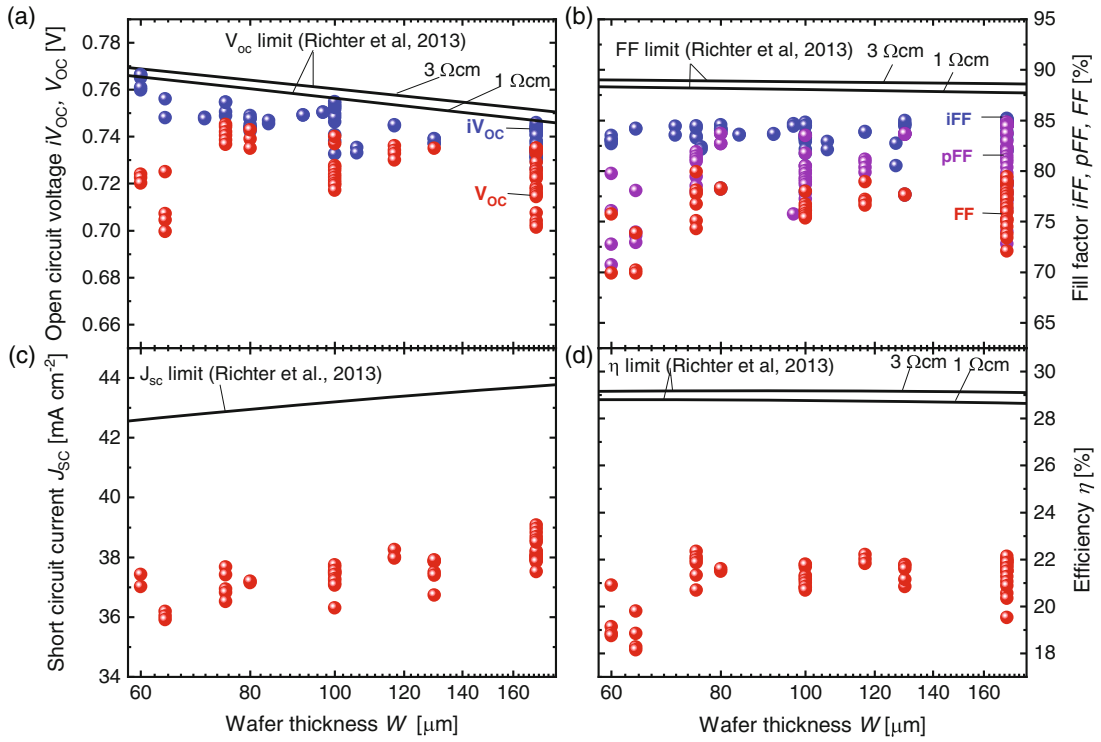

Figure 4. a) Implied open circuit iV_{OC} and open-circuit voltage V_{OC}; b) *i*FF, *p*FF, and FF; c) short-circuit current density J_{SC}; and d) efficiency η plotted with respect to the wafer thickness *W*. The measured samples have resistivities ranging from 1 to 3 Ωcm. The solid black lines represent theoretical limits for Si wafers with 1 and 3 Ωcm resistivities according to parametrization by Richter et al.[2]

becomes more significant as the wafers get thinner and that therefore issues with carrier selectivity of the contacts must be settled to preserve the gain in quasi-Fermi-level splitting in thinner wafers. A similar voltage loss behavior was obtained by Sai et al. for wafer thicknesses less than 70 μm.[41]

An alternative explanation is that at such low thicknesses, there is a higher possibility of wafer damage during the metallization process, which may also result in this drop on V_{OC}.[42,43]

2.3. Fill Factor

In predictions by Richter et al., a slight increase in FF with reduced thickness is expected for the studied wafer thickness range.[2] However, as shown in the "lifetime" section earlier, the *i*FF is predominately governed by SRH recombination at the interfaces, and theoretical predictions[2,3,16] are of little relevance here. Not surprisingly, results in Figure 4b show a trend opposite to the theoretical predictions—*i*FF decreases with the wafer thickness reduction. Unlike iV_{OC}, the implied FF is limited by the SRH recombination dominated by the surface defects and not Auger recombination. This result is consistent with the experimental results obtained by Richter et al.[44] To approach intrinsic limits especially for thinner wafers, significant improvements of passivation of wafer surfaces are needed. Similar to the iV_{OC} after ITO depositions, very little change in *i*FF values was observed for all wafers (not shown). After the finalization of solar cells, the *p*FF out of $I_{SC}-V_{OC}$ measurement and final FF from $I-V$ measurements are estimated. The *p*FF represents the diode FF without the effect of series and shunt resistance. The drop from *i*FF to *p*FF is smaller in the case of the reference wafer thickness and increases as the wafer thickness is reduced. Similar to V_{OC}, this increased drop from *i*FF to *p*FF for thinner wafers could be as a result of increased effect of contact shadowing,[34–36] carrier selectivity of contacts,[38–40] and possibly defects caused during the metallization process.[42,43] The final FF values for all wafer thicknesses drop from the *p*FF due to the effect of series resistance.

2.4. Short-Circuit Current Density and Efficiency

There is a significant difference between the theoretical limit and the measured short-circuit current densities in Figure 4c. This is related to the rather optimistic Lambertian scattering usually implied in the models as well as reflection and shadowing caused by the front metal contact in real solar cells. Noticeable J_{SC} losses related to the functional layers of SHJ show up here as well. However, the measured short-circuit current density shows a trend comparable with the theoretical predictions. The decrease at lower thicknesses is a direct result of reduced absorption in the long light wavelength region due to reduced optical path length in the solar cells. This absorption loss is shown in **Figure 5**, which shows the external quantum efficiency (EQE) spectra of some of the solar cells of different thicknesses. There is a trade-off between this decrease in J_{SC} values and the increase in V_{OC} with reduced wafer thickness, which results in a broad maximum of efficiency. Richter et al. predicted a maximum efficiency at about 110 μm thickness with minimal loss between

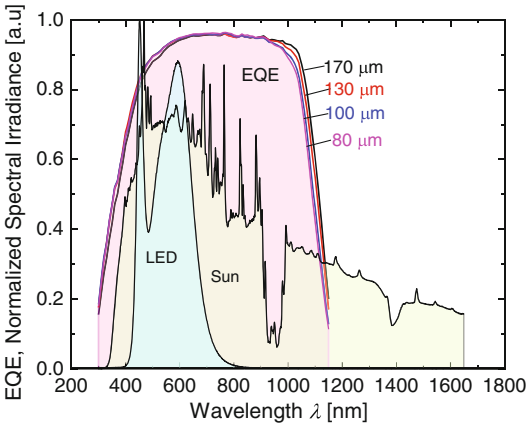

Figure 5. Normalized spectral irradiance of solar simulator and LED in comparison with the normalized EQE of SHJ solar cells at different thicknesses.

60 and 170 μm.[2] Our results in Figure 4d show a similar range of efficiency values between 75 and 170 μm with the best cell efficiency of 22.3% ($V_{OC} = 745$ mV, $J_{SC} = 37.43$ mA cm^{-1}, and FF = 80%) obtained at 75 μm, although there is no direct link between the work of Richter and the present results due to the significant influence of SRH recombination on the FF of the experimental solar cells. Note that considering scatter in the data and flat trends, no optimum of the thickness can be identified. Instead, it can be seen that wafer thickness can be varied over a significant range without compromising efficiency. Harrison et al., also reported a broad range of high efficiency for solar cell thicknesses between 90 and 160 μm.[42] At lower thicknesses, the decrease in J_{SC} and the possibility of higher defectivity dominate the increased V_{OC}, which results in a decrease in efficiency. With improved surface passivation and higher carrier selectivity of the contacts, there is potential for even higher efficiency in thinner wafers. However, with our existing passivation technology, it is clear that it is possible to reduce by half the thickness of the standard wafers majorly used in the manufacturing of silicon solar cells with no loss and possibly gain in efficiency values.

2.5. Indoor Performance

Solar cells can be used as indoor light harvesters for low–power-intensive standalone devices such as the internet of things, wireless sensors, etc. Light intensity in a well-lit classroom or office usually lies between 250 and 500 lux, which is by several orders less than the typical outdoor conditions.[45] Also, the spectrum of artificial lighting is more concentrated in the visible light region than the solar spectrum, which is spread out from the UV to the IR region. The different light properties result in significantly different requirements to solar cell absorber material. For Si, it means that much thinner wafers are required to absorb the available spectrum efficiently. In Figure 5, we show the effect of the thickness of silicon wafers on the EQE of the solar cell and also with respect to normalized LED and sun irradiance. There is a slight shift in the IR to lower wavelengths as the

thickness of the solar cell is reduced. This leads to a reduction of the short-circuit current density under solar illumination, as shown in Figure 3c. There is also a slight difference in the short-wavelength region between the reference 170 μm cells and the thinner cells, which is likely related to the difference in surface texture between the reference and thinned wafers. Under LED illumination, there is no expected loss in current at high wavelengths because no photons are produced by the LED at the infrared region. In fact, from the EQE and J_{SC} point of view, much thinner wafers can be used without any optical loss under LEDs. Hence, as reduction in wafer thickness leads to an increase in voltage, it is possible to improve the solar cell efficiency under LEDs by producing ultrathin silicon solar cells with no incurred optical losses. Bahrami-Yekta et al. predicted an optimum thickness of 1.8 μm for LED light harvesting as opposed to 109 μm under solar illumination.[15]

The performance of one-solar-cell silicon heterojunction modules at different light intensities under the solar and LED spectra was studied. Studies have shown that irrespective of the light source, there is a linear relationship between illumination intensity and short-circuit current.[46] Therefore, for a more uniform comparison, we represent our light intensity in terms of short-circuit current density J_{SC}.

There is an expected general decrease in photovoltaic parameters as the intensity of light is reduced, as shown in **Figure 6**. At higher light intensity, very little difference in V_{OC} is observed between the different wafer thicknesses under sun and LED illumination. However, toward lower intensities, a slightly steeper drop in V_{OC} is noticed for thicker wafers. The FF values obtained at 1 sun in Figure 6c are low compared with values shown in Figure 4b, likely due to perimeter recombination losses, which increase for smaller-sized solar cells.[47] Under sun illumination, an initial decrease in intensity leads to a slight increase in FF due to reduced effects of series resistance. A further decrease in intensity results in a sharp decrease in the FF values, which is likely due to shunt resistance effects for small-scale solar cells. Also, the reduced FF values at higher solar cell thickness at reduced intensity correlates with the measured shunt resistance values of the solar cells, which are lower for thicker solar cells. Similarly, under LED illumination, at indoor conditions, better

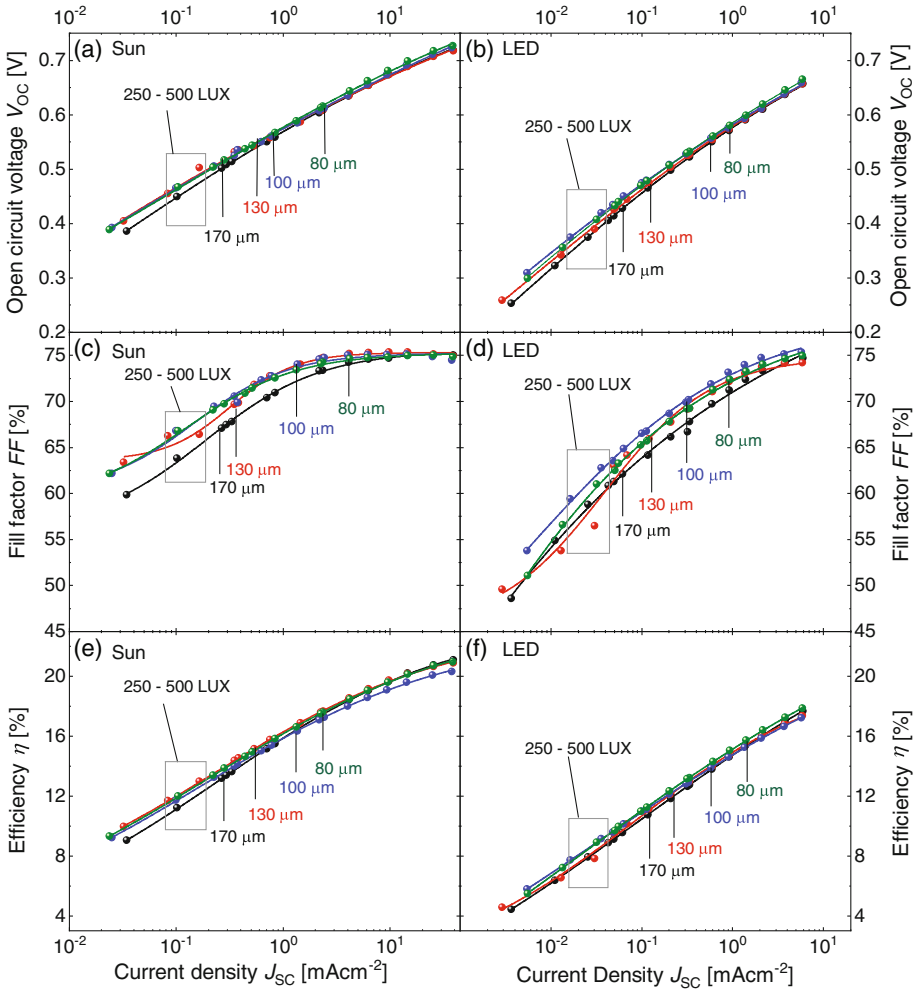

Figure 6. a,b) The open-circuit voltage V_{OC}; c,d) FF; and e,f) efficiency η for one-solar-cell SHJ solar modules of different thicknesses in different illumination intensities under the simulated sun and LED light sources. The solid lines represent the fit for data points for each wafer thickness. The rectangular boxes indicate the regions for typical indoor lighting.

FF values are observed for the 100 and 80 μm solar cells. There is a slight increase in the overall efficiency values at lower solar cell thicknesses, especially in low-light conditions. This suggests that further decrease in solar cell thickness could lead to better performance for indoor applications.

3. Conclusion

In this article, we investigated experimentally the effect of Si wafer thickness on the performance of silicon heterojunction solar cells. The effect has been studied for 1 sun standard irradiance and indoor LED illumination. Experimental trends were compared with the recent theoretical predictions of the efficiency limit in Si solar cells determined by Auger recombination. Lifetime measurements revealed that despite high-quality passivation in SHJ solar cells, the carrier lifetime at carrier density below $5 \times 10^{15}\,\mathrm{cm}^{-3}$ is dominated by surface recombination which gains importance as the wafer gets thinner. A reduction in wafer thickness leads to reduction of the effective carrier lifetime. The points of 1 sun *i*FF for all studied solar cell precursors are dominated by surface passivation; thus, reduction of wafer thickness leads to gradual reduction of *i*FF as opposed to the Auger limit predictions.

At higher excess carrier density, all solar cell precursors show transition to the Auger-dominated regime, which is supported by the differential ideality factor approaching characteristic value of 2/3. The 1 sun *i*Voc for all studied solar cells belongs to the Auger-dominated region. Therefore, experimental *i*Voc closely reproduces theoretical trends and best values are very close to the theoretical Auger limit. Overall, solar cell precursors show that maximum power point of modern SHJ solar cells is still strongly affected by the surface recombination and this effect is stronger in thinner wafers, which is in good agreement with recent report of Sai et al.[41] Approaching fundamental limits of *i*FF will take even further passivation improvement. In contrast, iV_{OC} is to a large extent Auger limited in highly passivated SHJ solar cells and is very close to the theoretical limit.

As the solar cells are finalized, both FF and V_{OC} show noticeable loss, which increases with thickness reduction, even excluding effects of parasitic resistances. We attribute the loss to contact shadowing and imperfect selectivity of the contacts, which is critical in high-voltage SHJ solar cells on thin wafers. Short-circuit current predictably reduces with thickness reduction due to weaker absorption in the long-wavelength region. The short-circuit current density J_{SC} follows the theoretically predicted trend, while absolute values are significantly lower than the limit based on Lambertian scattering, which leaves significant space for optimization.

Even though some challenging improvements have to be made to attain fundamental limits, the solar cells of various thicknesses show high efficiency. A broad range of high efficiency was observed for thicknesses ranging from 75 to 170 μm with a maximum of 22.3% obtained at 75 μm. This result shows the opportunity to reduce wafer thickness down to ≈75 μm without noticeable reduction in efficiency. A further reduction of the wafer thickness would take additional improvement in passivation quality, contact selectivity, and eventually light trapping.

For indoor performance, thinner wafers show slightly better efficiency at lower light intensity under sun and LED illumination. For higher efficiency under LED, a further decrease in wafer thickness is clearly recommended.

4. Experimental Section

Monocrystalline czochralski-grown M2 ($156.75 \times 156.75\,\mathrm{mm}^2$) n-type ⟨100⟩ silicon wafers of 170 μm standard thickness and resistivities ranging from 1 to 3 Ωcm were thinned and textured using a wet-bench chemical process, which involved first dipping the wafers in a mixture of HCl, O_3, and H_2O in appropriate proportions and then thinning the wafers down using deionized H_2O and dilute KOH, also known as the saw damage removal (SDR) process. To obtain wafers of different thicknesses, the SDR time was varied. The etching rate during thinning was evaluated from the weight loss of the wafers. At the development stage of the wafer thinning experiment, three methods were used to measure the wafer thickness: calculation out of the wafer weight, cross-section scanning electron microscopy (SEM), and mechanical thickness measurement at the LOANA solar simulator. The homogeneity of wafer etching was verified with cross-section SEM. The thinning process appeared to be highly homogeneous with variation of thickness of ±2 μm for the thinnest wafers. After calibration, the thickness of the wafer was routinely estimated with calculation out of the wafer weight. For textured wafers, this method resulted in the thickness values averaged over the texture. After thinning, the wafers were textured via anisotropic etching using KOH and an organic additive (monoTEX-F). Then, the wafers were cleaned in a mixture of HF, HCl, O_3, and H_2O and then rinsed and left to dry for 3 min at 50 °C. Using the plasma-enhanced chemical vapor deposition (PECVD) technique, a stack of intrinsic (i) and n-type-hydrogenated amorphous silicon (a-Si:H) was deposited on the front side, whereas an i/p-type a-Si:H stack was deposited on the rear side. The indium tin oxide (ITO) layers were deposited using the magnetron sputtering process and then silver grid contacts were screen printed on both sides of the wafers. Approximately one-third of the studied cells were finalized with full metal back contacts. Finally, the samples were annealed at 200 °C for 35 min for better conductivity and adhesion of the silver contacts and better passivation. More detailed descriptions of the deposition process are reported in other studies.[48,49] Two sizes of solar cells were used in the study. For the first part of the study related to 1 sun performance, the wafers were laser cut into four equal pieces of $\approx 78 \times 78\,\mathrm{mm}^2$. Four cells with aperture area of $19 \times 19\,\mathrm{mm}^2$ were formed by screen printing on each of the $78 \times 78\,\mathrm{mm}^2$ quarters. For the measurements under LED light, the measurement setup required devices with external contacts. In this case, the cells with aperture area of $17 \times 21\,\mathrm{mm}^2$ were laser cut out of the wafer and equipped with copper ribbon contacts soldered to the front and back busbars of the cell.

The effective lifetime measurements were done using the QSSPC technique. The EQE spectra were measured using a Grating Monochromator Quantum Efficiency (GM.QE) setup. A double-source AM1.5 Class A solar simulator was used at standard test conditions. A white LED light bulb was also used for simulating indoor performance of the solar cells. Measurements at different illumination intensities were done using neutral density filters.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding authors. The data are not publicly available due to privacy or ethical restrictions.

Keywords

effective carrier lifetimes, indoor performances, silicon heterojunction solar cells, silicon surface passivation, silicon wafer thicknesses

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