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Perspective on oxide-based three-terminal artificial synapses in physical neural networks

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ABSTRACT

The physical implementation of artificial neural networks, also known as "neuromorphic engineering" as advocated by Carver Mead in the late 1980s, has become urgent because of the increasing demand on massive and unstructured data processing. complementary metal-oxide-semiconductor-based hardware suffers from high power consumption due to the von Neumann bottleneck; therefore, alternative hardware architectures and devices meeting the energy efficiency requirements are being extensively investigated for neuromorphic computing. Among the emerging neuromorphic electronics, oxide-based three-terminal artificial synapses merit the features of scalability and compatibility with the silicon technology as well as the concurrent signal transmitting-and-learning. In this Perspective, we survey four types of three-terminal artificial synapses classified by their operation mechanisms, including the oxide electrolyte-gated transistor, ion-doped oxide electrolyte-gated transistor, ferroelectric-gated transistor, and charge trapping-gated transistor. The synaptic functions mimicked by these devices are analyzed based on the tunability of the channel conductance correlated with the charge relocation and polarization in gate dielectrics. Finally, the opportunities and challenges of implementing oxide-based three-terminal artificial synapses in physical neural networks are delineated for future prospects.

I. INTRODUCTION

A. Overview of neuromorphic computing and physical neural networks

Owing to the swift evolution of Internet of Things (IoTs), the capability of processing vast and unstructured data is an ever-increasing challenge for the present computing systems, either on the centralized cloud servers and edge servers or on the mobile devices.[1–3] Logically, the human brain is a superlative data processor because it executes parallel and multifaceted tasks such as coordinated judgment and concurrent physical actions or perceptions based on its neural network.[4] The neural network of the human brain contains about 10^{11} neurons interconnected by 10^{15} synaptic nodes.[5] This network empowers the brain to realize an efficient information transmitting. To imitate the function of the biological nervous system of the human brain, algorithms based on artificial neural networks (ANNs) have been developed for gigantic and complex computation.[6–8] Nevertheless, the data shuttling between the physically separated memory and central processing units in conventional von Neumann architecture leads to an insurmountable speed barrier, known as the von Neumann bottleneck.[9] It also results in massive energy consumption.[10,11]

Consequently, it is imperative to emulate neural networks with new physical hardware architectures, as opposed to software-based approaches, to overcome the barrier of the von Neumann bottleneck. As analogously illustrated in Fig. 1(a), the neuromorphic hardware system can be exemplified with a helicopter which travels much faster and overcomes the geographic obstacles as compared to a truck (representing the traditional von-Neumann computer). The hardware implementation of ANNs is also referring to neuromorphic engineering or "physical neural networks," which were developed by Carver Mead in the late 1980s when he pointed to the parallels between charges moving in MOS transistors operating in the subthreshold regime and charges transmitting across the membranes of neurons.[12–15] A neural network is typically represented by a three-layer perceptron model, as shown in Fig. 1(b). The nodes imitate the biological neurons of the human brain and connect to others by "artificial synapses." In 1996, the Mead group demonstrated single-transistor silicon synapses based on a floating-gate MOS transistor and operated at subthreshold current levels for analog learning applications. The synapse transistor allowed simultaneous memory reading and writing. As a result, the synapse arrays can compute both the array output and local memory updates, in parallel.[16]

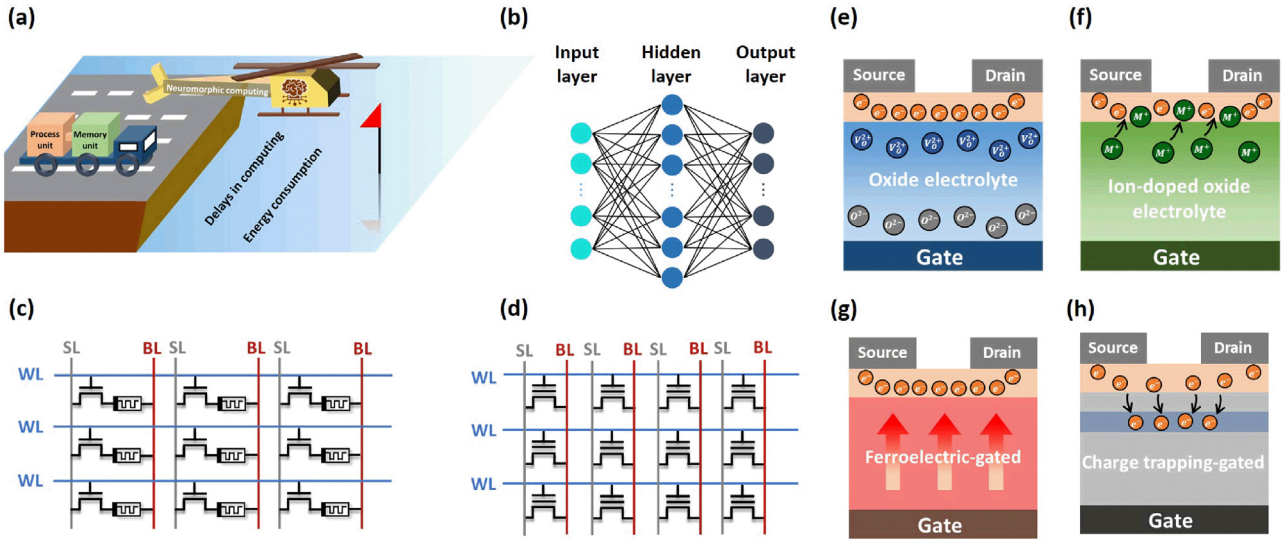

FIG. 1. (a) The race for computing efficacy in the future. Traditional von-Neumann architecture encounters the obstacles in computing efficiency which can be solved by the neuromorphic hardware system. (b) Schematic configuration of a three-layered artificial neural network. The crossbar array of artificial synapses based on (c) 1T1R and (d) single synaptic transistor as computing unit cell. Schematic diagram of three-terminal synaptic devices with different working principles: (e) oxide electrolyte-gated transistor, (f) ion-doped oxide electrolyte-gated transistor, (g) ferroelectric-gated transistor, and (h) charge trapping-gated transistor.

B. Analog switching devices as artificial synapses

However, the main difficulty of implementing ANNs using conventional complementary metal-oxide-semiconductor (CMOS) technology is the device scaling ability for accommodating large numbers of neurons and synapses in the networks.[17–19] Several promising novel devices for enabling easier hardware implementation of the neural networks have been investigated in recent years.[20–22] The main attention focuses are the synaptic functions mimicked by emerging nonvolatile memory devices, such as resistive random access memory (RRAM),[23–25] phase-change memory (PCM),[26–28] ferroelectric random access memory (FeRAM),[29–31] and magnetic random access memory (MRAM).[32–34] Among these, significant advances have been made in artificial synapses with a large variety of two-terminal RRAMs, also named memristors.[35–37] If a memristor presents analog switching, the multiple conductance states adjusted by consecutive identical voltage pulses are compatible with the tunable connection strengths (synaptic weight) of the biological synapse according to the neural activities. The conductance of the memristor can then be applied to encode the synaptic weight without requiring heavy additional digital circuitry.[38] Therefore, there are many papers in the literature discussing the implementation of artificial synapses and neurons using memristors for brain-inspired computing.[39–42]

C. Figures of merit for three-terminal synaptic devices

Two-terminal memristor-based synaptic devices are practical for a high density cross-point array architecture.[43] Nevertheless, the memristors are often afflicted by abrupt and stochastic switching characteristics, resulting in nonlinear and asymmetrical conductance modulation, as well as large device variations, subsequently limiting their performance as artificial synapses.[44] Furthermore, in many cases, an associated transistor selector is needed to prevent sneak current paths flowing through the unselected cells in the memristor array, making the one-transistor one-resistor (1T1R) cell essential.[45,46] Practically, a large number of memristors are deployed in the crossbar array to integrate the synaptic weights and transmit to the neuron devices. However, the undesired sneak path current flows through the unselected cells, causing crosstalk inference between the adjacent memory cells and inducing high energy consumption. With a transistor connected to a memristor in series, when the series transistor is in the on-state, the voltage across the memristor facilitates the resistance state switching. When the series transistor is in the off-state, no voltage drops across the memristor.[47] Therefore, the sneak path current can be effectively suppressed and the precise selection of a specific memristor can be realized. Yet, the additional transistor may complicate the device structure and increase the footprint as displayed in Fig. 1(c).

Without linking with memristors, three-terminal transistor-based devices are also developed for the application of artificial synapses.[44] The array architecture is illustrated in Fig. 1(d). In three-terminal transistor-based synaptic devices, the gate electrode is typically treated as presynaptic terminal for applying the action potential, and the channel conductance can be regulated such that the drain current is equivalent to the postsynaptic signal. Although the three-terminal synaptic transistors need more complex layer stacks than memristors, the artificial synaptic transistors are reported to prevent the sneak path issue and the removal of memristors will facilitate footprint scalability. Additionally, the separation of programming and reading terminals (at the gate and drain, respectively) allows a parallel and selective weight update,[48,49] guaranteeing a robust reversible change and compatibility with CMOS technology. Moreover, they can be extended to multiple gates to receive signals from several inputs jointly and, thus, can experience spatiotemporal effects, which two-terminal devices cannot.[50,51] In terms of the operation mechanism, the two-terminal memristor exhibits the feature of a pinched I–V hysteresis loop. The devices discussed in this Perspective are the three-terminal transistors,

where the source-to-drain current (I_D) depends on the gate voltage (V_G). Similar to the variable resistive states in the two-terminal memristor, the presence of an I_D–V_G hysteresis loop is critical for modulating the channel conductance states (related to I_D) to emulate the synaptic weight updating process.[52,53] The mechanism of channel conductance modulation may arise from the capacitance change in the gate dielectrics while applying different polarity of electrical stimulation on the gate electrode. Nevertheless, it is the channel conductance, not the capacitance, which dominates the synaptic functions. Therefore, the synaptic behavior performance can be mimicked well in both two-terminal memristors and three-terminal transistors due to the hysteretic loops in the I–V and I_D–V_G curves, respectively.

D. Oxide-based devices for neuromorphic implementation

Three-terminal transistor-based artificial synapses have been demonstrated with organic and inorganic semiconductors as the channel materials.[54–59] In the three-terminal artificial synapses, there exist two fundamental components: the semiconducting channel and gate dielectric layer. For semiconducting channels, the most common organic semiconductors include pentacene,[60] benzothiophene (C_8-BTBT),[61] and poly(3-hexylthiophene) (P3HT),[62] beneficial for their process maturity and continuity of large-scale film formation. As for 2D materials, such as graphene,[63] MoS_2,[64] and WSe_2,[65] can also be employed as the semiconducting channel materials in diverse fields due to their larger atomic utilization, large specific surface, and high charge transport ability. When considering the oxide materials, post-transition metal oxides, for instance, IGZO,[66] In_2O_3,[67] and ZnO,[68] are the main materials for semiconducting oxide channels because their conductivity can be modulated by controlling the stoichiometry or defect states.

Regarding the electrolyte layers (i.e., the "gate dielectrics"), hexagonal boron nitride[69,70] is an appealing dielectric 2D material with a large bandgap. For the oxide-based dielectrics, high dielectric constant (high-k) binary oxides, such as TaO_x,[68] HfO_x,[71] and ZrO_x,[72] are the proper materials because they generally possess large bandgaps and the conduction band offsets for minimizing the leakage current. Moreover, these high-k dielectrics can be grown thicker while maintaining the Equivalent Oxide Thickness (EOT) as SiO_2, enabling the gate leakage reduction for CMOS technology compatibility.[73,74]

Compared to organic semiconductors, inorganic semiconductors have the advantages of good stability, high carrier mobility, and compatibility with the current silicon process technology. Two groups of inorganic semiconductors are investigated as synaptic transistors: metal oxides and 2D layered materials. The 2D layered materials generally function as the semiconducting channels and they intrinsically possess dangling-bond-free and lattice-mismatch-free properties.[75,76] Also, 2D layered materials have advantages in several aspects, such as high mobility, fast operation speed, and lower switching energy.[77,78] Therefore, in terms of the synaptic characteristics, 2D materials may preferably demonstrate the heterosynaptic plasticity and mimicry of multi-terminal synaptic networks.[79–82] Similar to oxide semiconductors, by polarity combinations of the gate and drain voltage inputs, 2D materials-based synaptic devices can achieve diverse field-effect characteristics to reconfigurable multifunctional logic and neuromorphic capabilities.[83] However, the large-scale deposition, doping process, and inferior controllability over interface width are still the challenging issues for the practical application of 2D materials.[84–86]

There have been significant advancements made in metal oxide semiconductor thin-film transistors (TFTs) since Hosono first introduced high-mobility oxide TFTs based on amorphous InGaZnO (a-IGZO).[87] In addition to IGZO, some other post-transition metal oxides are the popular candidates to act as the channel layer in the oxide-based synaptic transistors, such as In_2O_3,[67] ZnO,[68] IZTO,[58] and so on. Most oxide semiconductors have been found to be n-type.[88] Moreover, the off-current in oxide TFT is ultralow because of the wide bandgap and low density of state in the forbidden band. This attribute is indispensable to diminish the leakage current for low power and low voltage operation.[89]

Therefore, in this Perspective, we mainly focus on the oxide-based three-terminal artificial synapses for physical neural network applications. We survey the recent research progresses of emerging synaptic transistors fabricated with both an oxide semiconductor channel and oxide dielectrics from the material and device performance perceptions. Based on the charge relocation in dielectrics for gating the channel conductance, four types of devices [Figs. 1(e)–1(h)] are classified and discussed, including oxide electrolyte-gated transistors, ion-doped oxide electrolyte-gated transistors, ferroelectric-gated transistors, and charge trapping-gated transistors. The fundamental physical mechanisms enabling these four types of transistors to be artificial synapses are first discussed, followed by presenting their synaptic performances for neuromorphic computation application. Finally, the prospects and challenges of implementing the three-terminal synaptic transistors in physical neural networks will be evaluated.

II. OPERATION MECHANISM OF THREE-TERMINAL SYNAPTIC DEVICES

A. Oxide electrolyte-gated transistors

Among various synaptic transistors, the electrolyte-gated transistor is favorable in attaining the synaptic properties because the development of the electric double layer (EDL)[90,91] brings the transistor to realize the memory and imitation. The non-equilibrium interface oxide charge state has been considered in two-terminal resistive switching devices based on the electrochemical process.[92,93] The charge storage in the dielectric/channel interface induces high carrier density in the channel and presents superior memory retention and transconductance. A schematic cross-sectional illustration of the ZnO/Ta_2O_5 transistor[68] is shown in the inset of Fig. 2(a). It was found the peak current during the cyclic voltammetry (CV) measurement strongly depends on the voltage scan rate, suggesting the accumulation of charged oxygen vacancies toward the channel under positive gate bias. A power law relationship[94] of $i_{peak} = av^b$ between the voltage scan rate and the extracted peak current is fitted shown in Fig. 2(b) and the parameter b is approximately 0.5. This indicates that the Faradaic process-induced diffusion-controlled current involves the diffusion of oxygen vacancies into the channel layer ZnO. A further measurement in Fig. 2(c) depicts the drain current is further while applying a constant drain voltage (2 V) with a scan rate of 0.05 V/s in gate voltage sweep. Notably, the drain current increases abruptly at a gate voltage of 2.4 V, suggesting the electrochemical doping of the ZnO channel by the drifted oxygen vacancies, which is analogous to the case in proton-doped devices.[95] This three-terminal device based

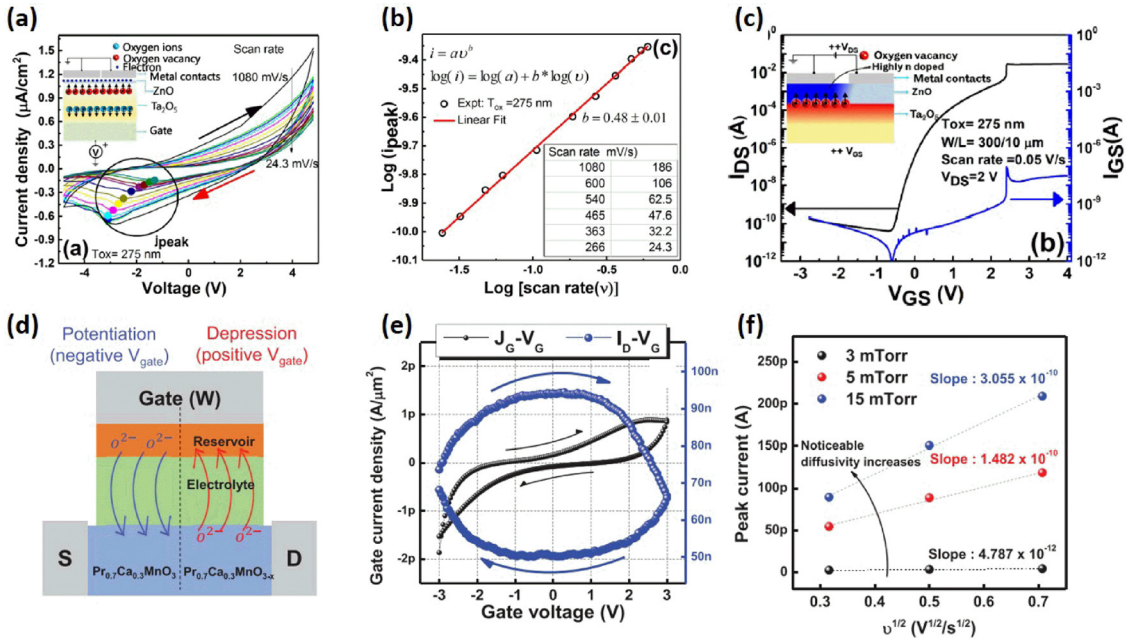

FIG. 2. (a) Cyclic voltammetry (CV) data revealing the electrochemical kinetics of the ZnO devices measured in the gate/insulator/semiconductor/metal geometry. I−V characteristics are acquired at different scan rates for Ta_2O_5 gated ZnO TFT with a W/L of 200/2.5 μm. (b) A power law relationship between the peak current (I_{peak}) of the reduction reaction and the scan rate (v), where b ∼ 0.5 implies the current is mainly controlled by solid-state diffusion of the mobile ions in the gate insulator. (c) The transfer characteristic captured at a drain bias of 2 V and using a scan rate of 0.05 V/s revealing an abrupt increase in the on-state conductance around $V_{GS} = 2.4$ V. Reprinted with permission from Pillai *et al.*, ACS Appl. Mater. Interfaces **10**, 9782–9791 (2018). Copyright 2018 American Chemical Society.[68] (d) Schematic of the operating mechanism of PCMO-based O-IST. (e) I_D–V_G (blue color) and J_G–V_G (black color) characteristics of the PCMO O-IST. Read voltage (V_{SD}) is set to 0.5 V. (f) Peak current (I_{peak})–sweep rate ($v^{1/2}$) fitting curve for various v. Reproduced with permission from Lee *et al.*, Appl. Phys. Lett. **119**, 103503 (2021). Copyright 2021 AIP Publishing.[59]

on reversible charge storage is predicted to have promising potential in neuromorphic application.

Since the ionic mobility in the electrolyte plays a critical role in the ion transportation to the active channel, Lee *et al.* demonstrated how the density of the HfO_x electrolyte dielectric layer affects the ion mobility.[59] Figure 2(d) illustrates the schematics of the cross-sectional image of the $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)-based oxygen-ion synaptic transistor as well as the simplified operating mechanism. The gate stack deposition of HfO_x (electrolyte)/GdO_x (reservoir)/W (gate electrode) was conducted by RF sputtering onto the PCMO semiconductor channel. When the negative gate pulse is applied, the oxygen ions in GdO_x can migrate through HfO_x and penetrate the PCMO channel, escalating the channel conductance, called potentiation. Conversely, the positive gate pulse extracts the oxygen ions from the channel and causes the depression. This conductance increase and reduction can be illustrated in the I_D–V_G characteristic plotted in Fig. 2(e). Compared with the channel resistance, the high resistance of the gate stack is justified by the cyclic voltammogram-based J_G–V_G curve, implying that the electrochemical reaction in the PCMO channel incorporated with oxygen ions provides the switching of channel conductance. By altering the working pressure (3, 5, and 15 mTorr) of the sputtered HfO_x electrolyte, the electrolyte density can be precisely controlled. According to the scan-rate-dependent cyclic voltammetry results for the devices with HfO_x deposited under working pressure from 3, 5, to 15 mTorr, the $I_{peak} - v^{1/2}$ fitted curves are shown in Fig. 2(f). The diffusivity of the oxygen ions in the transistors with HfO_x sputtered at 5 and 15 mTorr can be remarkably improved by more than ∼900 and ∼4000 times as opposed to that of transistor with HfO_x sputtered at 3 mTorr. Therefore, the ion mobility can be significantly elevated and provide a wider dynamic range in the potentiation and depression properties.

B. Ion-doped oxide electrolyte-gated transistors

To augment the synaptic characteristics, ion-doped oxide electrolyte-gated transistors are being studied with interest. Ions (e.g., H^+, Li^+, Na^+, and K^+)[91,96,98,99] in the electrolyte are introduced into the oxide electrolyte to accumulate at the electrolyte/channel interface by gate bias, forming an EDL to modulate the current in the channel layer. Additionally, the penetration of ions from the dielectric electrolyte into the channel may take place while applying a relatively high voltage, further enhancing the channel conductance level based on the electrochemical doping. Li *et al.*[96] prepared Li-ion doped Al_2O_3 (AlLiO) thin film as the solid electrolyte in the synaptic transistor. Fig. 3(a) compares the transfer characteristics between Al_2O_3 with and without Li-ion doping. With the application of backward gate voltage sweep from +4 to −2 V, a clockwise and a counterclockwise hysteresis are observed in In_2O_3/Al_2O_3 TFT and In_2O_3/AlLiO TFT, respectively. This can be attributed to the EDL developed due to the accumulation of Li-ion at the In_2O_3/AlLiO interface. As the gate voltage sweeps back, the accumulated electrons in the channel layer are retained because of the compensation for the external electric field caused by

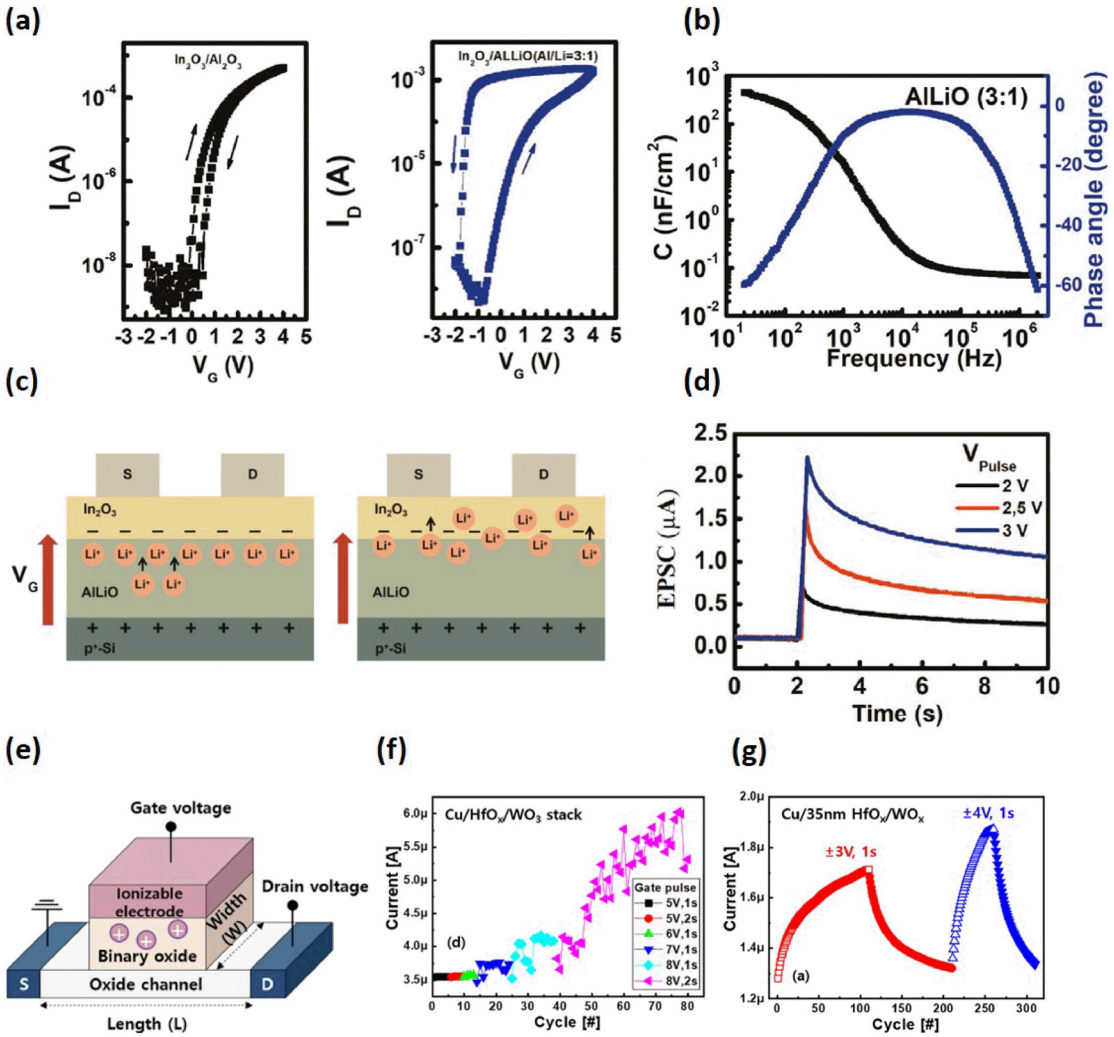

FIG. 3. (a) The transfer curves of In_2O_3/Al_2O_3 TFT and In_2O_3/AlLiO (Al:Li=3:1) TFT with V_G sweeping. (b) The capacitance–frequency curves and phase angle of AlLiO (Al:Li=3:1) films. (c) Schematic diagram of electrochemical doping in TFT. (d) The EPSC of In_2O_3/AlLiO TFT response to one presynaptic pulse with different pulse amplitudes ($V_D = 0.3$ V and pulse width = 30 ms). Reproduced with permission from Li *et al.*, Adv. Electron. Mater. **6**, 1901363 (2020). Copyright 2020 Wiley-VCH.[96] (e) Schematic diagram of the fabricated Cu-ion-actuated three-terminal synaptic device. (f) The read current measured at 0.5 V from the source to the drain of the Cu/HfO_x/WO_3 stack as a function of the gate pulse. (g) The read current measured at 0.5 V from the source to the drain of the Cu/HfO_x/WO_x stack as a function of the gate pulse. Reproduced with permission from Kang *et al.*, Appl. Phys. Lett. **119**, 072103 (2021). Copyright 2021 AIP Publishing.[97]

the slow relaxation of Li ions at the dielectric/channel interface. To explore the electrical response of AlLiO, the frequency dependence of the capacitance and phase angle is shown in Fig. 3(b) with ITO/AlLiO/p^+-Si capacitor. In the low frequency region ($f < 100$ Hz), the capacitance exhibits a large value (400–500 nF/cm^2) and weak dependence on the frequency. In terms of the phase angle, $|\theta| > 45°$ represents the capacitive behavior and correlates with the EDL formation. In the medium frequency ($100\ \text{Hz} < f < 10^4$ Hz), the capacitance is strongly affected by the frequency and $|\theta| < 45°$, implying the resistive behavior owing to the migration of dissociated lithium ions. At high frequency ($f > 10^4$ Hz), the capacitance gradually decreases and $|\theta| > 45°$. This refers to the dipolar relaxation in AlLiO oxide electrolyte.[100] The schematic in Fig. 3(c) displays the Li-ion migration toward the In_2O_3/AlLiO interface under the gate bias. With a stronger stimulus, the Li ions penetrate into the channel and lead to the long-term intensification of conductance. As shown in Fig. 3(d), the EPSC (excitatory post-synaptic current) slowly recovers to a constant value higher than the initial conductance. With the increased gate pulse amplitude, the EPSC peak value increases and the change in synaptic weight augments from 302% to 1210%. This specifies that the greater pulse amplitude gives rise to a stronger electrochemical doping and strengthens the potentiation effect.

In addition to the alkali mobile ions and oxygen vacancies (or oxygen ions), active ions, including Cu or Ag, can also be regarded as alternative ionic species in the transistor.[97,101] Figure 3(e) shows the schematic illustration of the Cu-ion-driven three-terminal artificial

synapse composed of simple binary oxides in the electrolyte dielectric and channel layer.[97] The WO_3 channel current, serving as the synaptic weight, can be modulated by the voltage exerted on the Cu top gate supplying ions through HfO_x electrolyte to the channel interface. By sequentially altering the gate voltage pulse amplitude, there is no distinguishable current change until the gate voltage pulse amplitude is higher than 7 V. The higher gate voltage pulse of 8 V is set as the threshold voltage required to actuate the Cu ions against the channel because of the effectively increased current shown in Fig. 3(f). As the injected Cu ions reach the WO_3 channel layer, the valence state of W will be changed at the interface, causing an enhanced channel current. However, to improve the controllability, the WO_3 sputtered from a W metal target in the Ar/O_2 mixed atmosphere is replaced with the WO_x deposited by sputtering a WO_x target with inert Ar gas only. The WO_x channel shows ten times lower resistance than the WO_3 channel and thereby improves the analog synaptic behavior. Figure 3(g) displays the weight updating process with relatively low voltage pulse amplitude of ±3 V in the $Cu/HfO_x/WO_x$ stack. Also, as the gate voltage is elevated, the dynamic range of the current is widened with a lower number of input pulses.

C. Ferroelectric-gated transistors

The ferroelectric-based transistor can achieve multilevel conductance states by applying various amplitude of the bias to control the degree of polarization in the ferroelectric dielectric layer.[102,103] When the electric field is removed, the polarization maintains and each state corresponds to the different conductance level in the channel. Compared to the ferroelectric perovskite oxides and polymers, hafnium oxide (HfO_x)-based ferroelectric materials, such as aluminum-doped HfO_x (Al:HfO_x),[71] zirconium-doped HfO_x (Zr:HfO_x),[104] and silicon-doped HfO_x (Si:HfO_x),[105] are preferable because of the compatibility with CMOS technology. In addition, an oxide semiconductor as the channel has more advantages than the Si-based channel because the unstable interface between HfO_x and Si causes the allocation of traps and requires high operating voltage.[106,107] Kim *et al.*[71] proposed an IGZO-based synaptic transistor using 10 nm thick Al:HfO_x film as the gate insulator shown in Fig. 4(a). Part of Hf in the orthorhombic phase (o-phase) of HfO_x is replaced with Al. The upward/downward polarization switching depends on the movement of negatively charged oxygen ions, inducing the accumulation or depletion of electrons in the IGZO channel. To confirm the ferroelectric characteristics, the polarization–voltage (P–V) measurements are carried out in the ITO/Al:HfO_x/W structure. Figure 4(b) shows the remnant polarization and coercive voltage increase with the increased sweep range. There are multiple domains in the Al:HfO_x layer and only when the applied voltage is higher than the coercive voltage in the domain will the polarization switching takes place. Moreover, the capacitance–voltage (C–V) curve in Fig. 4(c) reveals the charge response according to the applied voltage and displays a symmetric curve in forward and reverse sweep. For the artificial synapse, symmetric and linear weight updates during potentiation and depression are decisive to the learning accuracy. To examine the accuracy, two types of voltage waveform are examined in the study of Kim *et al.*[58] First, in Scheme A, 16 positive (+3.5 V, 10 μs) and 16 negative (−4 V, 10 μs) gate pulses are applied successively for conductance increase and decrease (not shown here). The other gate voltage waveform, Scheme B, contains a pulse train of positive incremental amplitude (2.5–4.075 V with step of 25 mV, and 64 pulses) and negative decreasing amplitude (−3 to −4.575 V with a step of (−25 mV and 64 pulses) with a fixed pulse width of 100 μs. A more linear analog conductance change and larger dynamic range are found in the pulse applied with Scheme B, as shown in Fig. 4(d). Consequently, Fig. 4(e) shows the image recognition accuracy in the experimental data of Scheme B (93.1%) is much closer to the ideal neural network (94.1%) than Scheme A (10.1%) is.

D. Charge trapping-gated transistors

In contrast to the excitatory synapse, the inhibitory synaptic functions were realized by the carrier trapping event under gate bias stimuli. Figure 5(a) shows the transfer characteristics of a floating-gate-type IGZO synaptic transistor with $Al_2O_3/ITO/Al_2O_3$ stack.[66] The forward sweep was conducted from $-V_{G,max}$ to $+V_{G,max}$ followed by the reverse sweep. A clockwise hysteresis was observed and the hysteresis window tended to be greater with an increase in the gate voltage sweep range. These results can be ascribed to the ITO trapping layer in the floating gate. The 10 nm-thick ITO with narrower bandgap compared with the Al_2O_3 forms a quantum well where electrons can be trapped easily. The Al_2O_3 of 6 nm between the ITO and channel layer IGZO was designed to get the electrons tunneling into the ITO, while the bottom blocking oxide Al_2O_3 of 30 nm served as the blocking layer to suppress the trapped electrons from emitting into the gate electrode. Figure 5(c) shows the current response to a positive gate voltage. After the stimulus, the current gets smaller than the initial one because of the electrons trapped in the ITO layer as shown graphically in Fig. 5(b).

Another sandwich-stack (SS) structure similar to the floating-gate-type transistor was proposed by the study of Yang *et al.*[108] The IGZO synaptic transistors are fabricated using the oxygen-deficient HfO_2 (OD-HfO_2) as the gate dielectric enwrapped with an HfO_xN_y ultrathin layer. With the assistance of a ferroelectric OD-HfO_2 layer, the electron trapping/releasing process can be enhanced and lead to the carrier concentration difference in the IGZO layer when applying gate bias pulse. The working mechanism is shown in Fig. 5(d). When a negative voltage pulse is applied to the gate electrode, the electrons are released into the IGZO. Simultaneously, coupled with the assistance of ferroelectric polarization, the movement of released electrons further increases the channel conductance. On the contrary, the positive gate pulse enables the accumulated electrons to be trapped at the interface or injected into the OD-HfO_2 layer. In addition, the reverse polarization direction in the OD-HfO_2 layer attracts more electrons toward the interface and causes them to be trapped more. Therefore, the channel current decreases.

III. SYNAPTIC FUNCTIONS AND NEUROMORPHIC COMPUTING

A. Short-term synaptic plasticity

In chemical biological synapses, the connection strength between two adjacent neurons is called synaptic plasticity. Synaptic plasticity refers to the activity-dependent modification and plays a central role in incorporating the immediate memory to persistent memory.[109] Short-term plasticity (STP), short-term memory (STM) to long-term memory (LTM) transition, long-term plasticity (LTP), and potentiation/depression (P/D) weight-updating are the fundamental and important synaptic functions. The electrolyte-gated transistors can realize STP (PPF and high-pass filter), while the ion-doped oxide electrolyte-gated

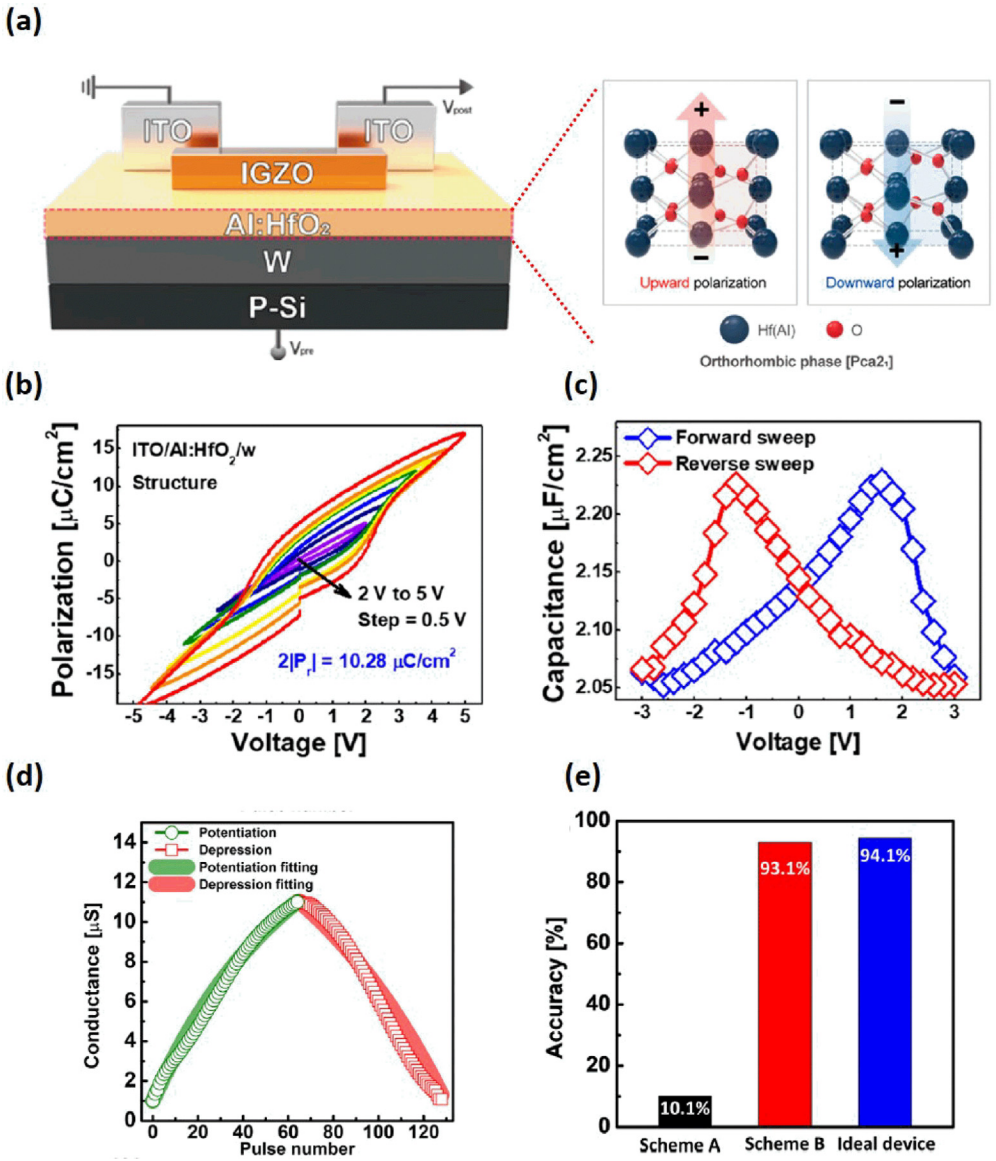

FIG. 4. (a) Schematic illustrations of FeTFT for the synaptic devices and mechanism of polarization switching in terms of the lattice structure. (b) P_V hysteresis curve of the MFM capacitors with a sweep voltage ranging from ±2to ±5 V. (c) C–V curve of the MFM capacitors. Reprinted with permission from Kim *et al.*, ACS Appl. Mater. Interfaces. **13**, 52743–52753 (2021). Copyright 2021 American Chemical Society.[71] (d) Potentiation and depression characteristics of the FeTFT using incremental pulses (Scheme B). (e) Simulated recognition accuracy of the neural network using an ideal device and the FeTFT with Scheme A/B. Reproduced with permission from Kim *et al.*, Appl. Phys. Lett. **118**, 032902 (2021). Copyright 2021 AIP Publishing.[58]

transistors are suitable to reveal STM-to-LTM transition. The ferroelectric-gated transistors and charge trapping-gated transistors are feasible to emulate LTP. Finally, to achieve the P/D weight-updating process in the neural network, the charge trapping-gated transistors are considered due to the fast carrier injection governed by Fowler–Nordheim tunneling and the conductance state can be continually modified and last for a long time.

Figure 6(a) presents the schematic illustration for the resemblance of the synapse and In_2O_3/Gd_2O_3 TFT.[67] To emulate the synaptic signal transmission, the gate electrode and drain electrode are considered as pre-synapse and post-synapse, respectively. The response of the drain current while applying the V_G pulse can be analogous to the EPSC. To demonstrate the short-term synaptic plasticity (STP), paired-pulse facilitation (PPF) is a typical character to be examined.[110] In a biological nerve system, PPF is an essential feature for decoding the temporal information, which is manifested as an enhancement of the post-synaptic potential. When two identical stimuli are applied to the device, the second current response will be larger

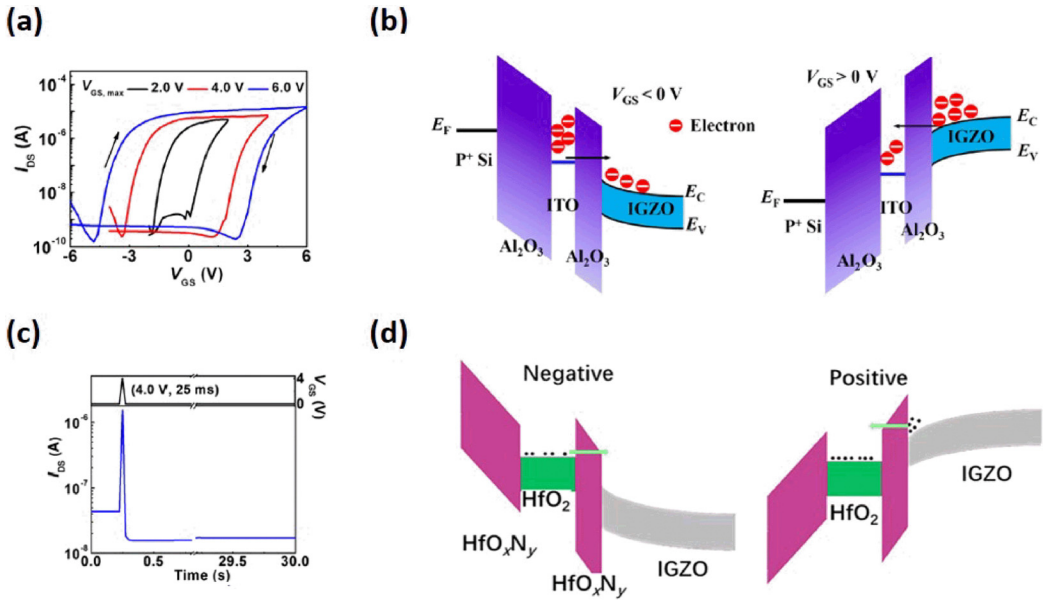

FIG. 5. (a) Transfer characteristics of the synaptic transistor measured under different V_{GS} sweeping ranges (from $-V_{GS,max}$ to $V_{GS,max}$ and then back) at $V_{DS} = 2.0$ V. (b) Band diagrams of the floating-gate synaptic transistor under negative and positive V_{GS}, respectively. Reproduced with permission from He *et al.*, J. Phys. D: Appl. Phys. **53**, 215106 (2020). Copyright 2020 IOP Publishing.[66] (c) The spike response to a high positive gate electrical pulse (4.0 V, 25 ms). (d) Band diagrams of the devices at negative and positive gate voltages, respectively. Reproduced with permission from Yang *et al.*, Appl. Phys. Lett. **115**, 022902 (2019). Copyright 2019 AIP Publishing.[108]

than the first one. As shown in Fig. 6(b), the second response of EPSC ($A_2 = 0.35$ μA) is apparently higher than the first response ($A_1 = 0.24$ μA) and the ratio of A_2 to A_1 is defined as the PPF index. As the interval time between the two spikes is shortened varying from 1000 to 50 ms, the PPF index will increase due to the enhancement of the second EPSC. This facilitation shown in Fig. 6(c) can be fitted with a double exponential decay function:[111]

$$\text{PPF index} = 1 + C_1 \exp\left(\frac{-\Delta t}{\tau_1}\right) + C_2 \exp\left(\frac{-\Delta t}{\tau_2}\right), \quad (1)$$

where the time decay constants τ_1 and τ_2 are of about 6 and 125.7 ms, respectively, it corresponds to the decay timescale in biological synapses. In addition to the PPF, STP can also be elicited by different temporal patterns of activity at particular synapses. Therefore, this differential frequency dependence gives rise to differing post-synaptic responses.[112] The EPSC response in Fig. 6(d) displays the final current increases with the frequency and the plot of EPSC gain (A_6/A_1) is gradually enhanced when the frequency rises as shown in Fig. 6(e). This result correlates with the frequency-dependent synaptic performance and makes the In_2O_3/Gd_2O_3 TFT feasible as a dynamic synaptic high-pass filter for information transmission.[113]

B. Long-term synaptic plasticity

Long-term synaptic plasticity (LTP) is the primary mechanism for learning and memory in the nervous system.[109,117] The experiment by Bliss *et al.* reported enhanced activation of excitatory synapses on the hippocampus led to increased synaptic strength and could last for hours or days.[118] This concept can be embodied in the synaptic devices to realize the emulation of the neural system. Figure 7(a) shows the PSC of the proton-doped SiO_2 insulator gated IGZO-based synaptic transistor after applying various numbers of gate pulses (1 V and 10 ms).[114] After the voltage pulse stimuli, the protons are driven toward the IGZO/SiO_2 interface and slowly return to equilibrium. The peak value of PSC increases and the decay process extends further while raising the pulse number. Figure 7(b) shows the PSC peak value and retention time (ΔI_p and τ) as a function of the pulse number, demonstrateing the short-term memory (STM) and long-term memory (LTM) consolidation. When the pulse height is strengthened to 7 V, the current is significantly elevated, as shown in Fig. 7(c). In addition to an evidently higher PSC peak value, the longer retention in current is observed. Some protons intercalated into the channel IGZO cause the current increase and remain for a longer time compared to the situation with a gate voltage pulse of 1 V. The transition from short-term memory to long-term memory can be manifested in Fig. 7(d), where τ increases from 30 to 3.1×10^4 ms with the increasing pulse number from 1 to 100. Based on the above-mentioned experiments, the IGZO/SiO_2 synaptic transistors are configured in a 3×3 array. Figure 7(e) illustrates the memory retention behavior encoded by a single pulse (1 V and 500 ms) to write the "T" pattern into the synaptic array. The "T" pattern at $t = 0$ s is represented in pure purple. Nevertheless, the purple color is gradually faded to white within 5 s due to the poor retention. To obtain a longer retention, the encoded single pulse is enhanced to 8 V height with 500 ms. In Fig. 7(f), despite the purple "T" pattern gently fading away after the writing process, it lasts much longer than the 1 V pulse does. This is well recognizable even after 500 s.

In terms of the charge trapping-gated device, the STM-to-LTM transition, for example, can be also realized in the Al nanoparticle-embedded-IGZO synaptic transistor. Consecutive gate pulses (−5 V

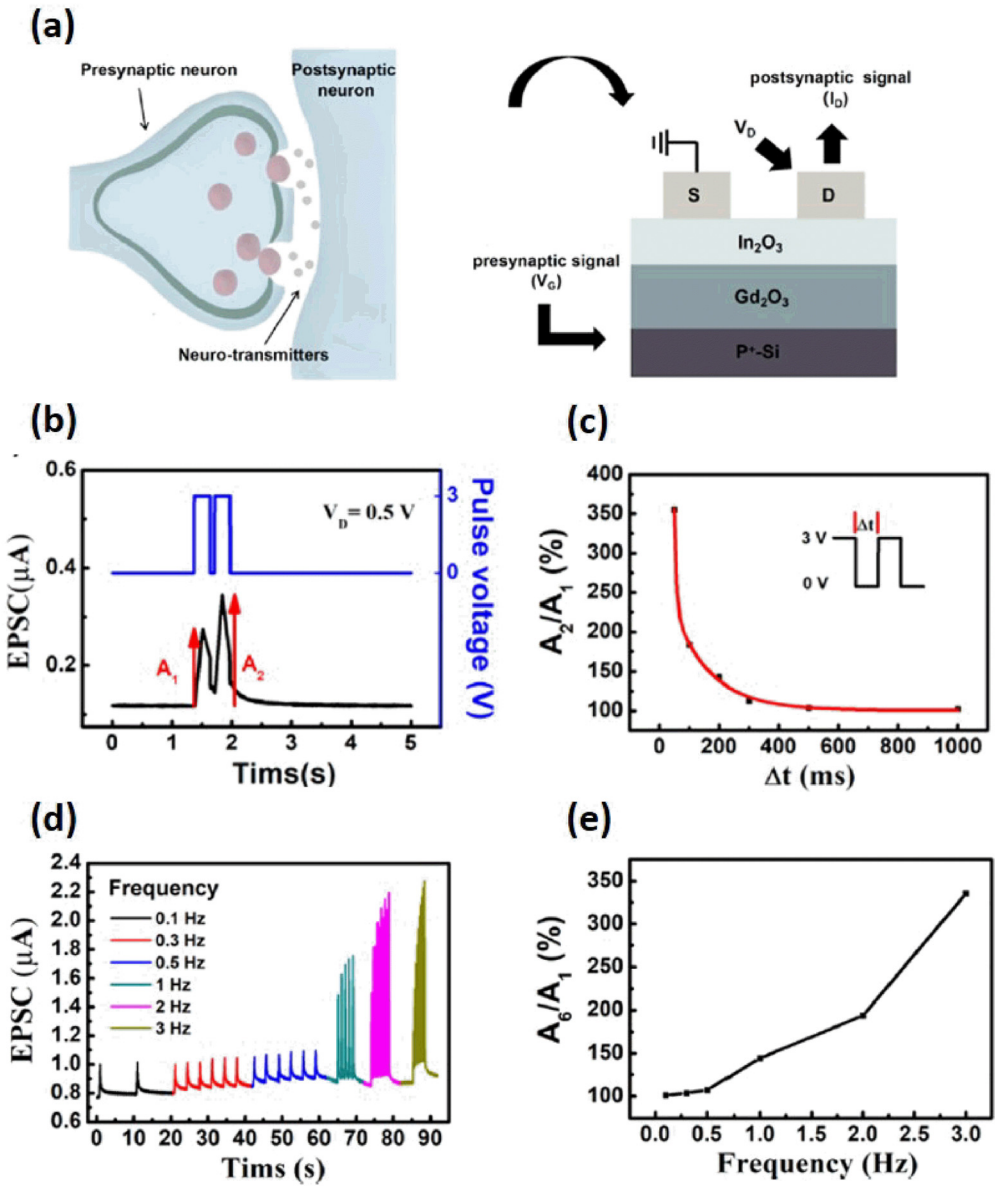

FIG. 6. (a) Schematic diagram of the neural synapse and In_2O_3/Gd_2O_3 TFT. (b) Paired-pulse facilitation (PPF) property of the excitatory postsynaptic current triggered by two presynaptic pulses ($V_{Pulse} = 3$ and $V_D = 0.5$ V). (c) Plots of PPF with a presynaptic interval time (Δt) varying from 50 to 1000 ms. (d) The EPSC of the In_2O_3/Gd_2O_3 TFT response to the six presynaptic pulses with different pulse frequencies. (e) Plots of A_6/A_1 of EPSC response to the different stimulus ($V_{Pulse} = 3$, $V_D = 0.5$ V, pulse width = 200 ms). Reprinted with permission from Zhou *et al.*, ACS Appl. Mater. Interfaces. **12**, 980–988 (2020). Copyright 2020 American Chemical Society.[67]

with 10 ms pulse width and 90 ms time interval) are applied to the synaptic transistor and the EPSC peak values grow continuously as the input pulse number increases as shown in Fig. 7(g).[115] Meanwhile, the long-term retention characteristics are achieved and indicated in the finally monitored currents triggered by the increasing pulse number. Also, in the ferroelectric-based device, the IGZO-based synaptic transistor gated by the $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) ferroelectric layer is proposed to examine the effect of polarization on LTP behavior.[116] Figures 7(h) and 7(i) show that the synaptic weight (i.e., the channel conductance) can be modulated by controlling the pulse amplitude applied to the gate terminal. A narrow pulse width of 50 μs with smaller voltage pulse leads to a sharp current increase but is not maintained. With the enhanced pulse amplitude and extension of pulse width to 500 μs, a higher current peak is obtained and results in a sustained conductance change lasting much longer. These time-dependent learning mechanisms are essential for matrix multiplication in ANNs because they are required to keep the weight constant until the next update occurs.

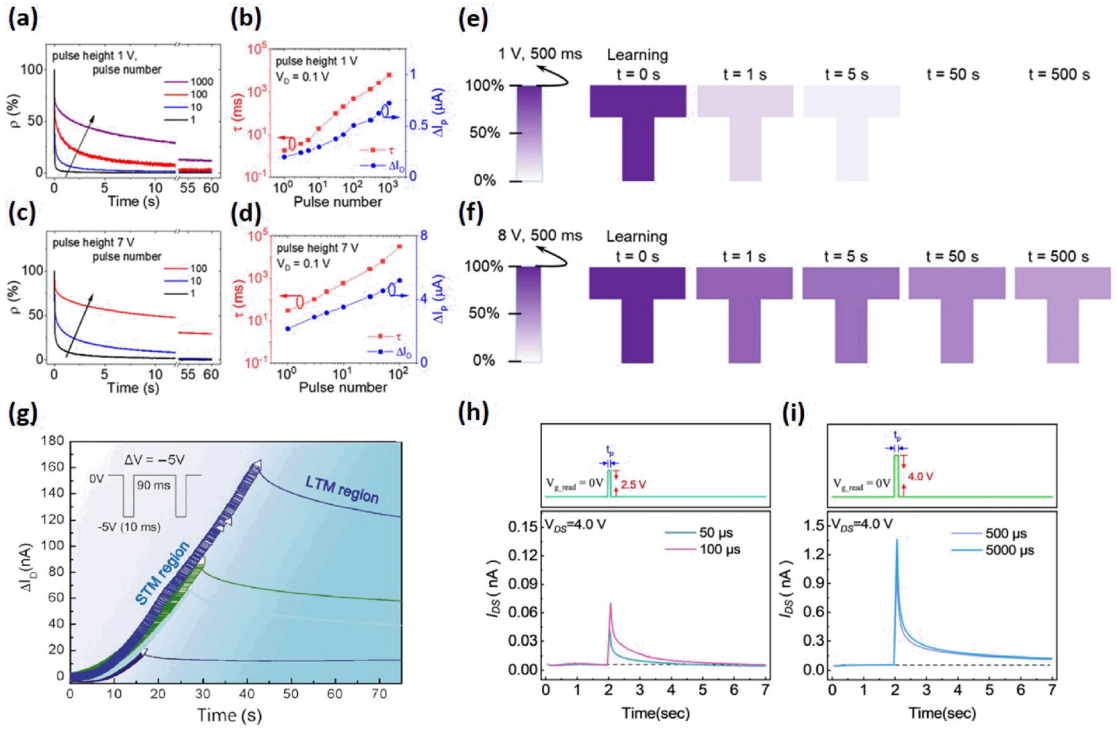

FIG. 7. (a)–(d) Memory behavior under different spiking numbers. (a) and (c) memory retention curves with varied pulse numbers (1, 10, and 100). (b) and (d) PSC peak value and memory retention time as a function of the applied gate pulse number. The pulse height is 1 V for (a) and (b) and 7 V for (c) and (d). (e) and (f) Pattern learning and memorizing behaviors. The pattern is represented in color from pure white to pure purple, which is encoded by the conductance value. The value is normalized by the PSC peak value under a single pulse of 500 ms with pulse heights of (e) 1 and (f) 8 V. Reproduced with permission from Fu *et al.*, Appl. Phys. Lett. **120**, 252903 (2022). Copyright 2022 AIP Publishing.[114] (g) Transition behavior from STM to LTM regimes. Reproduced with permission from Kim *et al.*, Adv. Electron. Mater. **6**, 1901072 (2020). Copyright 2020 Wiley-VCH.[115] (h) Tunable short-term plasticity with different spike widths. (i) Tunable long-term plasticity with different spike widths. Reproduced with permission from Zhong *et al.*, Appl. Phys. Lett. **117**, 092903 (2020). Copyright 2020 AIP Publishing.[116]

C. Neuromorphic computing

Realization of multi-states in synaptic strength on the basis of long-term potentiation (LTP) and long-term depression (LTD) is a requisite condition for the artificial neuromorphic computing.[109,120] Figure 8(a) shows the conductance modulation properties of IGZO/$HfZrO_x$-based ferroelectric synaptic TFT (FeTFT).[119] A series of pulses with incremental amplitude (from 2.7 to 4.3 V with 25 mV/step and 10 ms pulse width), and successive pulses of decreasing amplitude (from −2 to −3.6 V with 25 mV/step and 10 ms pulse width) are applied to the gate for potentiation and depression, respectively. The conductance (G) of FeTFT is read at V_G of -1 V and V_D of 1 V after the stimulation of each pulse with G_{max}/G_{min} ratio of 14.4. The linearity is evaluated by the following equation:[121]

$$G_p = B\left(1 - e^{-\frac{P}{A_p}}\right) + G_{\min}, \tag{2}$$

$$G_d = -B\left(1 - e^{-\frac{P - P_{max}}{A_d}}\right) + G_{\max}, \tag{3}$$

$$B = \frac{G_{\max} - G_{\min}}{1 - e^{\frac{-P_{\max}}{A_{p,d}}}}, \tag{4}$$

where G_p and G_d are the conductance states at the P^{th} pulse during potentiation and depression, respectively. The P_{max} is the pulse number corresponding to G_{max}, and A represents the linearity factor of the potentiation and depression processes. The fitted values are $A_p = -0.8028$ and $A_d = -0.6979$, indicating that the FeTFT possesses good linearity in weight update measurement.

An ANN is constructed according to the experimentally measured LTP/LTD of this FeTFT to demonstrate the supervised learning. A 20×20 image pixels of handwritten digits from the "Modified National Institute of Standards and Technology (MNIST)" dataset is the input dataset for training.[122] For simulation, the neural network consists of two-layer multilayer perceptron (MLP)[123] There are 400 input neuron nodes, 100 hidden neuron nodes, and ten output nodes as shown in Fig. 8(b). The 20×20 MNIST data correspond to the 400 input neurons and the ten output neurons classify the digits (0–9) from the input layer. At each epoch, 8000 patterns are selected randomly from 60 000 images during the training process followed by another 10 000 tested images to acquire sufficient accuracy. The accuracy after 125 training epochs displayed in Fig. 8(c) achieves 91.1% which is comparable to the ideal neural network of 94.1%. This high accuracy stems from the 64-level separated conductance states, good weight tuning linearity, low cycle-to-cycle variation, and practicable G_{max}/G_{min} ratio (14.4).

Generally, ANN only considers the static synaptic weight without temporal properties. In contrast, the spike neural network (SNN) exhibits low power consumption based on the dynamic binary spiking

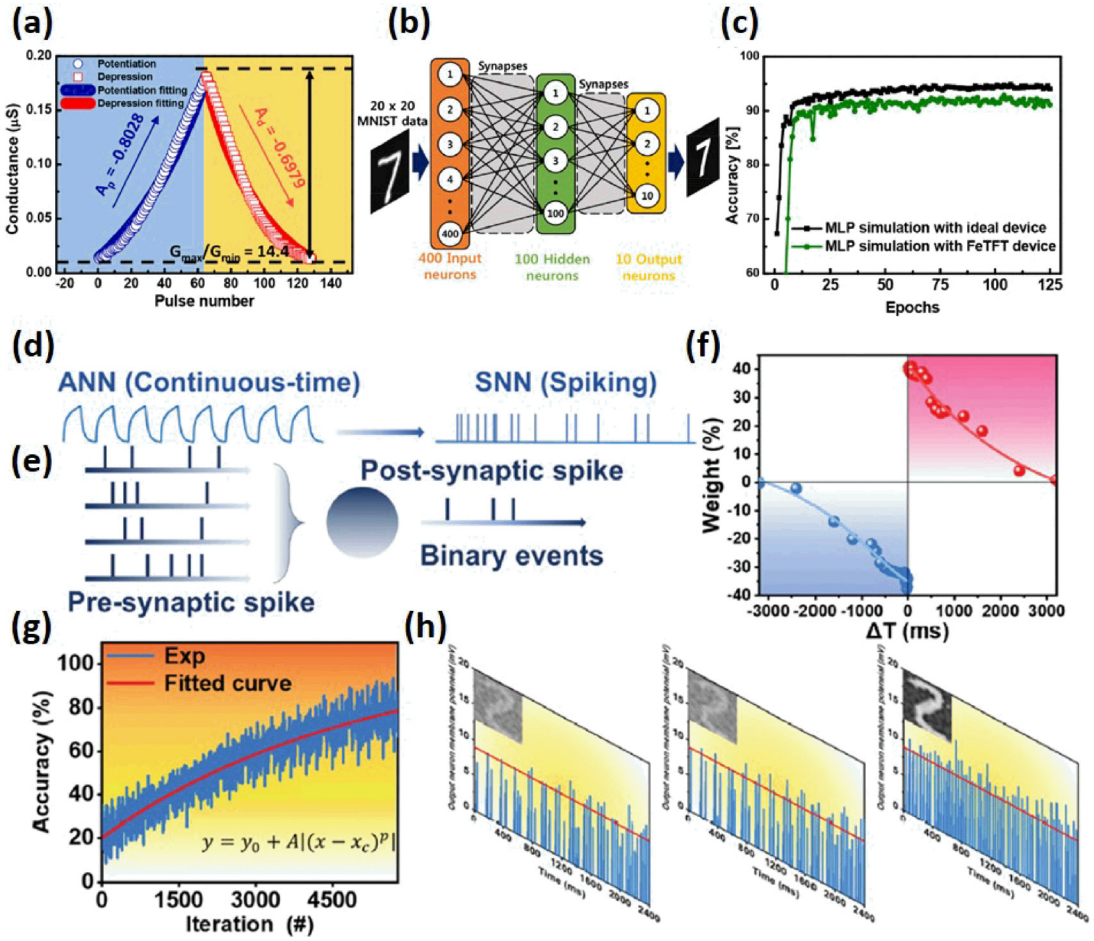

FIG. 8. (a) Potentiation and depression properties of the ferroelectric thin-film transistor with incremental pulse scheme. (b) Schematic illustration of the two-layer multilayer perceptron neural network. (c) Simulated pattern recognition accuracy of the two-layer multilayer perceptron neural network based on the ferroelectric thin-film transistors compared to an ideal neuromorphic device. Reprinted with permission from Kim *et al.*, Nano Lett. **19**, 2044–2050 (2019). Copyright 2019 American Chemical Society.[119] (d) ANN algorithm and SNN algorithm function diagram. (e) SNN algorithm weight update diagram. (f) STDP response based on K^+ doped AlO_x synaptic devices. (g) Image recognition rate of SNN algorithm. (h) Results of training the SNN at different stages using the MNIST dataset. Via the generation characteristics of the SNN, the image is reconstructed using the training weights connected to each output neuron to view the learning situation of the network. Reproduced with permission from Cao *et al.*, J. Mater. Chem. C **10**, 3196 (2022). Copyright 2022 Royal Society Chemistry.[91]

inputs as a function of time.[124] The neural nodes in SNN transmit spatiotemporal information to update the synaptic weight and correlates with the formation of associative memory.[125] The distinction between ANN and SNN is illustrated in Figs. 8(d) and 8(e).[91] Compared with the non-linear activation function in ANN, the information in SNN is encoded as sparse binary signals and abides by the all-or-nothing rule in reply to the input signal. SNN often refers to as the "third-generation" neural network owing to its potential for noise resiliency, computing energy efficiency, and more biologically realistic implementation.[126,127] To employ the SNN simulator, the spike timing dependent plasticity (STDP) behavior serves as the critical learning rule and could be emulated in the InO_x/K^+ doped AlO_x synaptic transistor, which resembles the strength of neural connections in biological process. The change in the synaptic weight ($\Delta\omega$) is defined as $(G_{Post}-G_{Pre})/G_{Pre}$, where G_{Pre} and G_{Post} are the conductance level after the pre- and post-synaptic stimuli, respectively. $\Delta\omega$ depends on the relative timing of the pre-synaptic and post-synaptic input action potential. If the pre-synaptic pulse precedes the post-synaptic pulse ($\Delta t > 0$), the connection strength could be strengthened; in contrast, the connection weakens as the sequence is reversed and causes the depression. The STDP ruled weight change at different timings and sequences is shown in Fig. 8(f). From the SNN algorithm, the result of the image recognition rate reaches 86% [shown in Fig. 8(g)] through the experimental LTP/LTD characteristics in STDP. In Fig. 8(h), after training by the MNIST dataset, all synaptic weights are associated with a particular neuron. The variable threshold is calculated through the number of involved activations and denoted as the red line in the figure. It can be observed that the inset diagram becomes distinct and reveals the success in the image recognition by the trained weight matrix.

IV. PERSPECTIVE DIRECTION AND CHALLENGE

To fully realize the hardware implementation of neuromorphic computing and perceptron devices, a host of challenges must be overcome in both scientific and engineering aspects. Building a brain-like computing paradigm still has a long way to go. The fundamental breakthrough lies in the joint efforts from the materials science, chemical/physical dynamics, mathematic model, circuit design, and other disciplines.

We reviewed the recent progress of oxide-based synaptic transistors based on different working principles. The oxide electrolyte-gated and ion-doped oxide electrolyte-gated transistors are prone to reveal the STP, including the PPF and high-pass filter. Oxide electrolyte-gated transistors have low operating voltage, linear conductance modulation characteristics, and demonstrate multiple synaptic functions. However, the dynamic range in weight updating and retention is limited, restricting their further application. Ion-doped oxide electrolyte-gated transistors enlarge the dynamic range and retention time. Due to the doped ions (i.e., alkali ions) in the oxide electrolyte-gated dielectrics, the formation of the electric double layer and the electrochemical doping process occur between the channel and dielectric layers, contributing to the transition from STM to LTM. Yet, the reactive alkali ions such as Li^+ are not compatible with the CMOS processes. On the other hand, the emulation of long-term synaptic plasticity (LTP) is an advantage of the ferroelectric-gated and charge trapping-gated synaptic transistors based on the polarization of ferroelectric dielectrics and floating gate, respectively. Ferroelectric-gated transistors have an edge on gradual conductance modulation, fast operation speed, and long-term retention time. Nevertheless, because of the nonvolatile memory characteristics, the emulation of STP is difficult. Additionally, the fabrication of a high-quality ferroelectric layer with multi-domain features is challenging in a large-scale array. Another complex matter is the application of an incremental pulse scheme to obtain a linear and wide conductance modulation complicates the peripheral circuit. The charge trapping-gated transistor exhibits good retention and reliability, but the voltage required for Write/Erase is high and consumes more power in the system. In addition, the floating-gate-type transistors take up a larger area and increase the manufacturing complexity due to the sandwich structure.

The synaptic transistors discussed in this Perspective have their own opportunities and obstacles in various synaptic functionalities. First, the tradeoffs are found in all four types of the transistors for emulating both STP and LTP. In view of the CMOS technology compatibility, the ferroelectric-gated transistors are the promising artificial synapses; however, they have difficulty in demonstrating STP because of the nonvolatile memory characteristics. To combine the STP and LTP characteristics, the gate dielectric with the mixed mechanism of ferroelectric and ion-doped oxide electrolyte is worthy of future exploration because it will enable the transistor to demonstrate the synaptic functions more comprehensively.

Overall, the fundamental mechanism requiring more attention is the ferroelectric-gated transistor. FeFETs feature a wide dynamic range of conductance modulation with high bit resolution, fast operation speed and low programming power. More importantly, the CMOS-compatible processes endow FeFET with promising potential for hardware implantation. Recently, FinFET (or tri-gate) technology has replaced planar CMOS technology for down-scaling purposes. The FinFeFET has been reported and the overall footprint is scaled down to 0.002 μm^2 area.[128] Therefore, the ferroelectric-gated synaptic transistors are the favorable synaptic element for large-scale integrated neuromorphic hardware implementation.

The pulse duration for modulating the synaptic transistor channel conductance falls in the range of milliseconds to microseconds,[129] while it is microseconds or even lower to nanoseconds for the memristors.[130] Two factors account for this difference. First, in most reports, the transistor channel lengths are greater than a few micrometers. On the contrary, the active layer thicknesses of the memristors are in a nanometer scale. Second, the conductance variation in synaptic transistors arises from the channel carrier concentration modulation induced by the field-effect through the electrolyte-gated dielectric layer. For the two-terminal memristors, the conductance of the active layer is immediately affected by the electric field applied to it. Therefore, the modulation response of the electrical conductance to the stimulating pulses is indeed slower in synaptic transistors as compared to the memristors. To improve the operation speed of the three-terminal artificial synapses, the down-scaling of the transistor dimensions, especially decreasing the channel length and dielectric thickness, will be immediately effective (if the leakage current is properly restricted). Additionally, to increase the gate control on the channel, multi-gate transistors[51] and ultimately the GAA[131] (gate-all-around) field effect transistors have high potential to improve the speed of the three terminal synaptic transistors. These complex structures may not be easily realized in academic laboratories but can be feasibly implemented in the IC fabs once the functionalities of three-terminal artificial synapses are matured.

Apart from the pros and cons, the development of multi-terminal devices to increase the synaptic functionality per unit area has also been regarded as a scaling issue for efficiency. However, multi-terminal synaptic transistors are rarely found in oxide-based devices. Compared to the ionic liquid or polymer electrolyte, oxide dielectrics suffer from poor ionic conductivity, contributing to a lower specific capacitance.[132] This might be the reason why few lateral-gate or multi-gate devices are demonstrated in oxide-based synaptic transistors. Consequently, improving the device functionality by virtue of the advantages in multi-terminal synaptic transistors should be an issue of attention for future research. Also, it is expected synaptic devices will be implemented in the field of wearable smart chips and health monitoring components, so the properties of flexibility, stretchability, and biocompatibility must be considered. Nevertheless, unlike organic synaptic transistors, studies regarding the flexible devices based on oxide materials are still limited.[116]

In addition, although essential synaptic functions are taken into account in numerous types of transistors, the biological neuron information processing functions based on the computational LIF (leaky-integrate and fire) model have scarcely been reported in oxide-based transistors. The "fire" action of LIF may be difficult to achieve by pulsing gate voltage and it will rely on the two-terminal threshold-switching memristors.[133–135] Moreover, since the number of synaptic connections is around 10^{15}, the arrangement of the devices is a huge task. Each type of artificial synapses has their own opportunities but also faces obstacles in the realization of brain-like computing hardware. A further comprehension of the physical mechanisms of these emerging oxide-based synaptic transistors will benefit their device uniformity and reliability. Together with the 3D integration technique, the brain-inspired chips packaged with high-density neuromorphic

devices will be more process-efficient on a larger scale and reveal the significance for long-term development.

Exploitation of neuromorphic computing and engineering involves multiple disciplinary studies. In aspects of the materials and device performance, the channel conductance regulation in response to the electrical pulse reveals analog modulation and complex switching dynamics, enabling the emulation of brain-inspired learning rules. We have summarized these in the manuscript and the above-mentioned discussion.

For the hardware circuit design, the key element lies in the non-von Neumann architecture. The synaptic module consists of densely packed crossbar array, where the cross point between each column and row sets up an artificial synapse. All the regulative synaptic weights in the matrix are integrated by multiply accumulate operation and transmit to neuronal module, performing the in-parallel computing efficiently. This significant research effort targets the attainment of large-scale neural network circuit deployment.[43] Regardless of spiking or non-spiking networks, the matrix-vector multiplication (MNM) utilizes Ohm's and Kirchhoff's laws and allows high real-time processing speed.[136] However, the challenge should be the mixed analog and digital computation, which might require a large number of analog-digital converters to carry out the hybrid integration of front-end CMOS technology and synaptic devices.

In addition, the neuromorphic algorithms are the core of training the neural network. With the evolution of neural network models, the third-generation spiking neural network (SNN) model employs spiking data and time as a computational resource.[137,138] This algorithm is bio-plausible and emulates how biology acquires knowledge efficiently, which needs investigation in neuroscience. The fundamental issue arises in understanding the information encoding and process through the spatiotemporal signal propagation. The device response to the assorted spatiotemporal signals is a fundamental material dynamic issue at the atomic scale that is yet to be explored.

Based on the above-mentioned discussion, to advance the field of neuromorphic hardware, the integration of multiple disciplines, including materials science, peripheral circuitry, computation science, and neuroscience, must be investigated.

V. SUMMARY

In summary, brain-inspired computing based on neuromorphic devices utilizing oxide materials has made great stride. For implementing in-memory computing, three-terminal synaptic devices feature the recommended metrics, including the size for integration, number of states, linearity and symmetry, switching energy, write/read speed, state retention, etc. These desired characteristics need to be further explored for faithful biomimetic dynamic computing. Accordingly, the priority efforts will be devoted to developing the materials and understanding the working principle of artificial synapses. In this Perspective, we review the recent progress of oxide-based three-terminal artificial synapses for physical neural network application. Four types of transistors classified by their gating mechanisms are discussed: oxide electrolyte-gated transistor, ion-doped oxide electrolyte-gated transistor, ferroelectric-gated transistor, and charge trapping-gated transistor. One type of transistors can take precedence over other types of transistors, determined by the particular demand for the application. Although some challenges remain, the combination of the interdisciplinary field such as materials engineering, chemical/physical science, computer science, and peripheral circuit design will achieve the breakthroughs in the scope of brain-inspired computing as well as in the biomimetic design, such as robotics and prosthetics.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Kuan-Ting Chen: Conceptualization (equal); Investigation (lead); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Jen-Sue Chen:** Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Resources (lead); Supervision (lead); Validation (equal); Writing – original draft (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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