MOS Capacitance–Voltage Characteristics from Electron-Trapping at Dopant Donor Impurity*

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Abstract: The capacitance versus DC-voltage formula from electron trapping at dopant impurity centers is derived for MOS capacitors by the charge-storage method. Fermi–Dirac distribution and impurity deionization are included in the DC-voltage scale. The low-frequency and high-frequency capacitances, and their differences and derivatives, are computed in the presence of an unlimited source of minority and majority carriers. The results show that their difference and their DC-voltage derivatives, are large and readily measurable, hence suitable as a method for characterizing the electronic trapping parameters at dopant impurity centers and for a number of lower power signal processing and device technology monitoring applications.

Key words: MOS capacitance; trapping capacitance; impurity deionization; spintronics
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1. Introduction

The effect of dopant impurity deionization, due to trapping of electrons on donors and holes on acceptors, on the DC current–voltage (DCIV) characteristics from electron–hole recombination (R-DCIV) at SiO_2/Si interface traps in MOS transistor was recently reported by us[1]. One of us (CTS) proposed potential device applications of the distortion of the voltage-scale of the R-DCIV curves from impurity deionization, such as memory or bit storage on the spin-orbit states of trapped electrons at the donor impurity atoms (centers) or trapped holes at acceptor impurity atoms (centers). In this paper, we present the results of the DC-voltage dependence of the capacitance from trapping electrons and holes ($C_{\rm nt}$ and $C_{\rm pt}$ versus DC-gate-to-body voltage $V_{\rm GB}$, $C_{\rm nt}V_{\rm GB}$ and $C_{\rm pt}V_{\rm GB}$) at the dopant donor and acceptor impurity centers or traps, including its DC-voltage distortions from the trapped charges, because the direct-result trapping-capacitance at the dopant impurities should be much more sensitive than the indirect-result recombination-current at the interface traps, aside from the fact that the dopant impurity concentration is usually high and can be made very high, while the interface traps are to be avoided at all costs. Furthermore, three applications are evident: (1) the use of the trap capacitance as information storage at the spin and configuration (orbit) states of the trapped electron or hole, and by the capacitance–voltage (CV) line-shape (lineshape) which is influenced by the charge state of the impurity center from the presence and absence of a trapped electron or hole, (2) the use of the trap capacitance versus DC gate voltage variation, and its first and higher DC-voltage derivatives, to give the dopant impurity concentration profile, at a resolution exceeding the conventional minority-majority carrier storage capacitance method, and (3) an easy method to measure the quantum mechanical transition properties of the trapped electrons and holes at the impurity centers, and their chemical dependence, of both the impurity and the host, that provide these missing fundamental electronic kinetic constants or quantum mechanical transition rates in the modeling of the solid state.

In this first report on this new trapping-capacitance-DC-voltage method, we shall demonstrate the feasibility, using a simple model which is the one of small-signal sinusoidal steady-state at the two limits of the measurement signal frequency $f = \omega/2\pi$, namely much higher and much lower than the trapping frequency $\omega_{\rm t}$ or the reciprocal trapping rate $1/\tau_{\rm t}$, that is, $\omega \gg \omega_{\rm t} = 1/\tau_{\rm t}$ and $\omega \ll \omega_{\rm t} = 1/\tau_{\rm t}$ which are determined by the emission and capture rates of the electrons at the shallow-level donor dopant impurities and of the holes at the shallow-level acceptor dopant impurities[2]. For electrons trapped at the donor impurity centers, this is[2,3] $1/\tau_{\rm t} = c_{\rm n}N + e_{\rm n}$ where N is the electron concentration in the conduction band. The three mechanisms of electron capture by the donor-impurity electron trap are given by $c_{\rm n} = c_{\rm nt}+c_{\rm no}+c_{\rm na}$ from the three capture transitions, Thermal, Optical, and Auger-Impact[2] which gives the carrier concentration dependence of $\tau_{\rm t}$. Similarly, the three mechanisms of electron emission or detrapping from the donor-impurity electron trap, are given by $e_{\rm n} = e_{\rm nt} + e_{\rm no} + e_{\rm na}$. Recombination of hole with the trapped electron and capture of a valence band electron by donor-impurity electron trap not occupied by trapped electron, are the additional two transitions[2].

We shall also assume an unlimited source of minority and majority carriers so that the low-frequency limit is not unduly long due to the delayed supply of the minority and majority carriers at the their contacts or a common ohmic or infinite recombination-generation-velocity contact. The physics of the mathematical limiting condition is that the measurement signal frequency must be small compared with the reciprocal rate or the frequency of supply of the majority and minority car-

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riers by these contacts[3], $(2\pi f) = 1/\tau = \omega \ll \omega_c = 1/(\tau_n+\tau_p) = \omega_n\omega_p/(\omega_n+\omega_p)$ where by definition, $\omega_n = 1/\tau_n$ and $\omega_p = 1/\tau_n$, or the measurement signal time constant, τ, must be large compared with the sum of the rates of supplying the majority and minority carriers, $\tau \gg \tau_n + \tau_p$, that is, both the majority and the minority carriers must be supplied and extracted by the contacts, fast enough to follow the change of the measurement signal.

In this first report, on feasibility, we shall also ignore the fine structures (excited states and spin-orbit or spin and space-configuration degeneracies) of the bound states of the electrons or holes trapped at the impurity centers. These details are described in the second report to be published in this journal soon.

2. Electron Trapping Capacitance in MOS Capacitor

We follow the textbook derivation of the charge-control capacitance[2] for the semiconductor capacitance, C_s, with extension from Boltzmann distribution and impurity full ionization (no trapping) to Fermi–Dirac distribution and impurity deionization (with trapping). The semiconductor capacitance now consists of three parts, including trapping at the dopant impurities, C_{nt} and/or C_{pt}, instead of just two parts, the electron and hole storage capacitances, C_n and C_p. Thus, the capacitance of the 2-terminal MOS capacitance between the metal gate and the semiconductor substrate, body or bulk, C_{gb}, is a capacity network consisting of the oxide capacitance, C_{ox}, in series with the parallel combination of the electron and hole and trapped electron or/and hole capacitances, C_s = electron capacitance C_n + hole capacitance C_p + trapping capacitance C_t. The latter is measurement-signal-frequency dependent ($\omega = 2\pi f$ where frequency f is in Hertz unit or cycle per second, and capacitances, in Farad per unit area). C_t approaches C_{nt} or C_{pt} or their sum at low frequencies and it approaches zero at high frequencies when trapping is too slow to following the signal, or the trapping frequency is too small compared with the signal frequency, $\omega_t \ll \omega$[2]. Writing $C_s(\omega) = C_n(\omega) + C_p(\omega) + C_t(\omega)$ and using the series-parallel capacitance model just described,

$$\begin{aligned} C_{gb} &= (C_{ox}C_s)/(C_{ox} + C_s) \\ &= C_{ox}(C_n + C_p + C_t)/(C_{ox} + C_n + C_p + C_t), \end{aligned}$$

we have the following general and frequency-limit results:

$$\begin{aligned} C_{gb}(\omega) &= C_{ox}[C_n(\omega) + C_p(\omega) + C_t(\omega)] \\ &\quad \div [C_{ox} + C_n(\omega) + C_p(\omega) + C_t(\omega)] \qquad (1) \\ &= C_{ox}[C_n(\omega_s) + C_p(\omega_s) + C_t(\omega)] \\ &\quad \div [C_{ox} + C_n(\omega_s) + C_p(\omega_s) + C_t(\omega)]. \qquad (2) \end{aligned}$$

Unlimited Source of Minority and Majority Carriers ($1/\tau_c = \omega_c \gg \omega_s \approx 0$)

$$\begin{aligned} C_{gb}(\omega) &= C_{ox}[C_n(0) + C_p(0) + C_t(\omega)] \\ &\quad \div [C_{ox} + C_n(0) + C_p(0) + C_t(\omega)]. \qquad (3) \end{aligned}$$

We drop the (ω) and use the appropriate charge-controlled values, then:

Electron Trap at Shallow-Level Donor Dopant Impurity Center

$$C_{gb\_lf} = C_{ox}(C_n + C_p + C_{nt})/(C_{ox} + C_n + C_p + C_{nt}), \quad \text{Low Frequency,} \qquad (4)$$

$$C_{gb\_hf} = C_{ox}(C_n + C_p + 0)/(C_{ox} + C_n + C_p + 0), \quad \text{High Frequency.} \qquad (5)$$

Hole Trap at Shallow-Level Acceptor Dopant Impurity Center

$$C_{gb\_lf} = C_{ox}(C_n + C_p + C_{pt})/(C_{ox} + C_n + C_p + C_{pt}), \quad \text{Low Frequency,} \qquad (6)$$

$$C_{gb\_hf} = C_{ox}(C_n + C_p + 0)/(C_{ox} + C_n + C_p + 0), \quad \text{High Frequency.} \qquad (7)$$

The asymptotic expressions given in Eqs. (3) to (7) are readily obtained by the stated frequency limits already described in the preceding paragraph and the conditions stated at the end of each equation.

Based on the charge control method, the capacitance is given by $\partial Q/\partial V$[2,3] where V is the potential between the two surfaces of a layer and Q is the stored charge per unit area in the layer, from both the mobile electrons and holes in the conduction and valence bands and the trapped electrons at the donor impurity centers and trapped holes at the acceptor impurity centers. The stored charge, Q, is obtained by the integration of the space-charge density (volume). The dependence of the local potential, $V(x)$, on the applied voltage to the two terminals (Gate and Body, V_{GB}) is obtained by integration of the Poisson Equation using the boundary conditions at the four interfaces: conductor-wire/Gate-metal, Gate-Metal/SiO_2, SiO_2/Si-Body and Si-Body/Metal-Contact. We extend the textbook description[2] to include the trapping and deionization at the dopant impurity centers and the Fermi–Dirac statistics for high carrier concentration in strong accumulation and inversion gate-voltage ranges. For this first report, on feasibility, we consider only n-Si with a donor dopant impurity, such as Phosphorus or Arsenic, of a total N_{DD} neutral atoms per unit volume (commonly symboled by chemists as $N_{DD}^{\times}$ but less ambiguously as N_{DD}^{0}, however, we shall just use N_{DD} to represent its two meanings, the total atom density and the also the total neutral atom density which is electrically neutral in a free space environment) each with five valence electrons, hence positively charged when the fifth valence electron is released from the donor impurity center to the silicon conduction to satisfy the crystalline silicon's covalent bond, leaving a singly positively charge donor atomic core, to be denoted by the volume density $N_D^+(x)$, hence, denoting the density of trapped electrons at the donor impurity center as $N_D(x)$, which is also the density of the neutral donor impurity. Thus, the total donor impurity concentration (density) is given by

$$N_{DD}(x) = N_D^+(x) + N_D(x), \qquad (8)$$

or the density (concentration) of the charged donor impurity is given by

$$N_{\rm D}^{+}(x) = N_{\rm DD}(x) - N_{\rm D}(x). \tag{9}$$

The volume density of the space charge in silicon body or bulk is then given by

$$\begin{aligned}\rho(x) &= q[P(x) - N(x) + N_{\rm D}^{+}(x)] \\ &= q[P(x) - N(x) + N_{\rm DD}(x) - N_{\rm D}(x)].\end{aligned} \tag{10}$$

Using the reference at $x = \infty$ where the electrical neutrality is assumed,

$$\begin{aligned}\rho(x=\infty) &= q[P(x=\infty) - N(x=\infty) \\ &\quad + N_{\rm DD}(x=\infty) - N_{\rm D}(x=\infty)] \\ &= 0,\end{aligned} \tag{11}$$

then,

$$\begin{aligned}\rho(x) &= \rho(x) - \rho(x=\infty) \\ &= q\{[P(x) - P(x=\infty)] - [N(x) - N(x=\infty)] + \\ &\quad [N_{\rm DD}(x) - N_{\rm DD}(x=\infty)] - [N_{\rm D}(x) - N_{\rm D}(x=\infty)]\}.\end{aligned} \tag{12}$$

Using the homogeneous sample condition, $N_{\rm DD}(x) = N_{\rm DD}$ = independent of x, so $N_{\rm DD}(x) = N_{\rm DD}(x = \infty)$, then, Equation (12) is further simplified to just three groups of terms, from valence band holes, conduction band electrons, and trapped electrons on the donor impurities:

$$\begin{aligned}\rho(x) = q\{&[P(x) - P(x=\infty)] - [N(x) - N(x=\infty)] \\ &- [N_{\rm D}(x) - N_{\rm D}(x=\infty)]\}.\end{aligned} \tag{13}$$

Integrating Eq. (13) over the entire thickness of the semiconductor body-or-bulk, from $x = 0$ to $x = \infty$, writing the electric potential at the SiO_2/Si interface $x = 0$ as $V(x = 0) = V_{\rm S}$, using the electrical potential $x = \infty$ as the reference, $V(x = \infty) = 0$, and writing $P(x = \infty) = P_{\rm B}$ and $N(x = \infty) = N_{\rm B}$, then, the areal density of the three stored charges are

$$\begin{aligned}Q_{\rm S} &= \int_0^\infty \rho(x){\rm d}x = \int_0^\infty [\rho(x) - \rho(x=\infty)]{\rm d}x \\ &= \int_0^\infty {\rm d}x\{q[P(x) - P_{\rm B}] - q[N(x) - N_{\rm B}] \\ &\qquad - q[N_{\rm D}(x) - N_{\rm D}(x=\infty)]\} \\ &\equiv +Q_{\rm P} + Q_{\rm N} + Q_{\rm NT},\end{aligned} \tag{14}$$

where the stored hole charge density per unit area is

$$Q_{\rm P} \equiv +q\int_0^\infty [P(x) - P_{\rm B}]{\rm d}x, \tag{15}$$

the stored electron charge density per unit area is

$$Q_{\rm N} \equiv -q\int_0^\infty [N(x) - N_{\rm B}]{\rm d}x, \tag{16}$$

and the stored trapped electron charge density trapped at the positively charged donor impurities or stored trapped electron charge density is:

$$Q_{\rm NT} \equiv -q\int_0^\infty [N_{\rm D}(x) - N_{\rm D}(x=\infty)]{\rm d}x. \tag{17}$$

With the positive charge flowing into the node or terminal as the positive direction, the semiconductor charge-control capacitance is then:

$$C_{\rm s} \equiv -{\rm d}Q_{\rm S}/{\rm d}V_{\rm S} = C_{\rm p} + C_{\rm n} + C_{\rm nt}, \tag{18}$$

where the hole charge-control capacitance is

$$C_{\rm p} \equiv -{\rm d}Q_{\rm P}/{\rm d}V_{\rm S}, \tag{19}$$

the electron charge-control capacitance is

$$C_{\rm n} \equiv -{\rm d}Q_{\rm N}/{\rm d}V_{\rm S}, \tag{20}$$

and the trapped electron charge-control capacitance of the electrons trapped at the donor impurities:

$$C_{\rm nt} \equiv -{\rm d}Q_{\rm NT}/{\rm d}V_{\rm S}. \tag{21}$$

The steady-state Fermi–Dirac occupation function of the conduction band states occupied by electrons and valence band states occupied by holes, and the steady-state fraction of the donor impurities occupied by trapped electrons, $f_{\rm D} = N_{\rm D}/N_{\rm DD}$, were given in Ref. [2] which are listed below:

$$P(x) = N_{\rm V} \times F_{1/2}\{[-qV(x) + E_{\rm V} - E_{\rm F}]/kT\}, \tag{22}$$

$$N(x) = N_{\rm C} \times F_{1/2}\{[E_{\rm F} - E_{\rm C} + qV(x)]/kT\}, \tag{23}$$

$$\begin{aligned}N_{\rm D}(x) &= f_{\rm D}(x) \times N_{\rm DD} \\ &= N_{\rm DD} \div \{1 + (1/g_{\rm D})\exp[(E_{\rm D} - qV(x) - E_{\rm F})/kT]\},\end{aligned} \tag{24}$$

where $N_{\rm C}$ and $N_{\rm V}$ are respectively the effective densities of electronic (electron and hole) states in the conduction and valence bands; $V(x)$ is the electric potential which characterizes the silicon energy band bending at the position x, and $-qV(x)$ measures the energy difference between the conduction band edges at the position x and at the far-away position $x = \infty$ where $V(x = \infty) = 0$. The potential is normalized to the thermal voltage $k_{\rm B}T/q$, given by $U(x) \equiv qV(x)/k_{\rm B}T$. Recall that $V(x = \infty) = 0$ is the reference potential and $V(x = 0) = V_{\rm S}$ is the surface potential. The conduction band edge at the far-away position $x = \infty$ is taken as the reference energy level in this paper, namely, $E_{\rm C} = 0$, so $E_{\rm V} = -E_{\rm G}$ where $E_{\rm G}$ is the silicon energy gap ($\sim$ 1.12 eV and precise temperature dependence is used in our computations). Thus, all energies and energy levels, and electric potentials are properly referenced, with two subscripts, the second of which is the reference. The Fermi energy level is denoted by $E_{\rm FC}$, the donor trap energy level by $E_{\rm DC}$, and the corresponding not-normalized and normalized (to thermal voltage, $k_{\rm B}T/q$) potentials of the Fermi energy are $V_{\rm FC} = -E_{\rm FC}/q$ and $U_{\rm FC} = qV_{\rm FC}/kT$; and

the potentials of donor trap energy-level are $V_{DC} = -E_{DC}/q$ and $U_{DC} = qV_{DC}/kT$. Using these normalized potentials and energy-level-potentials, the hole, electron, and trapped electron densities given by Eqs. (22)–(24) are now:

$$P(x) = N_V \times F_{1/2}(U_{FC} - E_G/kT - U(x)), \tag{25}$$

$$N(x) = N_C \times F_{1/2}(U(x) - U_{FC}), \tag{26}$$

$$N_D(x) = N_{DD} \div \{1 + (1/g_D)\exp[U_{FC} - U_{DC} - U(x)]\}. \tag{27}$$

We have used the consensus Fermi–Dirac integral of the order j , defined by Dingle in 1957[4] and employed universally in the first 40 years (1957 to 1997), as[2, 4]:

$$F_j(\eta) = [\Gamma(j+1)]^{-1}\int_0^\infty \varepsilon^j[1+\exp(\varepsilon-\eta)]^{-1}\mathrm{d}\varepsilon. \tag{28}$$

Using the rational Chebyshev approximation, the Fermi–Dirac integrals of the order of $j = 3/2,\ 1/2,\ -1/2$ and $-3/2$ have been evaluated to high precision by Cody and Thacher 10 years later in 1967[5] and by Trellakis, Galick and Ravaioli another 30 years later in 1997[6], in a span of 55 years to today (1957 to 2011). We have used their approximation formulas in calculations at high concentrations and are continuing to use their approximation formulas in our capacitance calculations reported here.

To obtain the equation between the surface potential, V_S (and its normalized value, U_S) and the DC voltage V_{GB} (and its normalized value, U_{GB}) applied between the Gate and the Body contacts of the 1-D MOS capacitor, we integrate the DC steady-state Poisson equation from the Gate contact to the Body contact and apply the boundary conditions at the four interfaces mentioned in the initial part of this section[2]. In the bulk-body silicon region, $x = 0$ to $x = \infty$, the Poisson Equation can be expressed in the following normalized form (normalized to k_BT/q).

$$\varepsilon_S(\mathrm{d}E/\mathrm{d}x) = -\varepsilon_S\mathrm{d}^2V(x)/\mathrm{d}x^2 = -\varepsilon_S(kT/q)\mathrm{d}^2U(x)/\mathrm{d}x^2 \tag{29}$$

$$= \rho(x) = q[P(x) - N(x) + N_{DD} - N_D(x)] \tag{30}$$

$$= q\{N_V \times F_{1/2}(U_{FC} - E_G/kT - U(x)) - N_C \times F_{1/2}(U(x) - U_{FC}) + N_{DD} \div [1 + g_D\exp(U(x) - U_{FC} + U_{DC})]\}. \tag{31}$$

Integrating the above by quadrature using $E(x) = -\mathrm{d}V(x)/\mathrm{d}x$, the electric field at any location x in the silicon substrate of body is then given by[7, 8]:

$$E^2 = (2kT/\varepsilon_s) \times \{N_V \times [F_{3/2}(U_{FC} - E_G/kT - U(x)) - F_{3/2}(U_{FC} - E_G/kT)] + N_C \times [F_{3/2}(U(x) - U_{FC}) - F_{3/2}(-U_{FC})] + N_{DD} \times [-U(x) + \log_e(1 + g_D\exp(U(x) + U_{DC} - U_{FC})) - \log_e(1 + g_D\exp(U_{DC} - U_{FC}))]\}. \tag{32}$$

The surface electric field at the SiO_2/Si interface, $x = 0$, $E(x = 0) = E_S$ is then given by

$$E_S^2 = (2kT/\varepsilon_s) \times \{N_V \times [F_{3/2}(U_{FC} - E_G/kT - U_S) - F_{3/2}(U_{FC} - E_G/kT)] + N_C \times [F_{3/2}(U_S - U_{FC}) - F_{3/2}(-U_{FC})] + N_{DD} \times [-U_S + \log_e(1 + g_D\exp(U_S + U_{DC} - U_{FC})) - \log_e(1 + g_D\exp(U_{DC} - U_{FC}))]\}. \tag{33}$$

Substituting Eqs. (25)–(27) and $N_{DD}(x = \infty) = N_{DD}$ into Eq. (11), the charge neutrality condition at $x = \infty$ reads:

$$N_V \times F_{1/2}(U_{FC} - E_G/kT) - N_C \times F_{1/2}(-U_{FC}) + N_{DD} \div \{1 + g_D\exp[U_{DC} - U_{FC}]\} = 0. \tag{34}$$

The Fermi potential V_{FC} can then be solved from the above equation using Newton–Raphson method.

Using the Gauss theorem, $Q_G = \varepsilon_O E_O = \varepsilon_O V_O/x_O = C_{ox}V_O$ at the gate-conductor/oxide interface and $Q_S = -\varepsilon_S E_S$ at the oxide/silicon interface, or just the straight-forward integration from $x = -x_O$ to $x = 0$ to $x = \infty$ using the three boundary conditions at these three interfaces, the gate-voltage surface-potential relationship can be obtained[2]:

$$C_{ox}V_O = \varepsilon_S E_S - Q_{OT} - Q_{IT}, \tag{35}$$

$$V_{GB} = [\phi_{MS}/q - (Q_{OT} + Q_{IT})/C_{ox}] + V_S + \varepsilon_S E_S/C_{ox} = V_{FB} + V_S + \varepsilon_S E_S/C_{ox}, \tag{36}$$

where Q_{OT} is the areal density of the oxide trapped charge and Q_{IT}, the interface trapped charge; ϕ_{MS} is the work function difference between the metal and the silicon; V_{FB} the flatband voltage, C_{ox} is the oxide capacitance per unit area and V_O is the potential drop through the oxide layer. Since we wish to focus on the trapped charges on the dopant impurity center, therefore, we discard the oxide trapped charge and the interface trapped charge: $Q_{OT} = 0$ and $Q_{IT} = 0$. The metal is assumed to be Aluminum. From Table 413.1 in Ref. [2], $\phi_M = 4.679$ eV, $\phi_S = 4.029\ \mathrm{eV} + E_C - E_F = 4.029\ \mathrm{eV} - E_{FC}$. The flatband voltage is then:

$$V_{FB} = \phi_{MS}/q = 0.65 + V_{FC}\ \ (\mathrm{V}). \tag{37}$$

Using the definition of the threshold voltage condition for the MOS transistor defined by one of us (CTS) in 1964, which is the energy band bending amount which corresponds to the minority (hole) concentration at the surface equaling the equilibrium majority (electron) concentration, $P(x = 0) = N(x = \infty)$, then the surface potential at the threshold, U_{Sth}, can be obtained by solving the following equation:

$$N_V \times F_{1/2}(U_{FC} - E_G/kT - U_{Sth}) = N_C \times F_{1/2}(-U_{FC}). \tag{38}$$

Then, the threshold voltage (at strong surface inversion) is given by

$$V_{TH} = V_{FB} + V_{Sth} + \varepsilon_S \times E(U = U_{Sth}) \div C_{ox}. \tag{39}$$

Substituting Eqs. (27) and (32) into Eq. (17) and noting $dx = -(kT/qE) \times dU$, we obtain the explicit single integral to compute the areal charge density of electrons trapped at the donor impurity:

$$\begin{aligned} Q_{NT} &= \int_{U_S}^{0} q[N_D(x) - N_D(x=\infty)](kT/q)E^{-1}dU \\ &= \text{sign}(U_S) \times kTN_{DD} \int_0^{U_S} dU\{[1 + g_D \exp(U + U_{DC} - U_{FC})]^{-1} - [1 + g_D \exp(U_{DC} - U_{FC})]^{-1}\} \\ &\quad \times (2kT/\varepsilon_S)^{-1/2}\{N_V[F_{3/2}(U_{FC} - E_G/kT - U) - F_{3/2}(U_{FC} - E_G/kT)] + N_C[F_{3/2}(U - U_{FC}) - F_{3/2}(-U_{FC})] \\ &\quad + N_{DD}[-U + \log_e([1 + g_D \exp(U + U_{DC} - U_{FC})]/[1 + g_D \exp(U_{DC} - U_{FC})])]\}^{-1/2}. \end{aligned} \tag{40}$$

Using the definition Eq. (21), the analytic expression of the electron trapping capacitance or trapped electron charge storage capacitance is obtained and given by

$$C_{nt} = -qN_{DD}\{[1 + g_D \exp(U_S + U_{DC} - U_{FC})]^{-1} - [1 + g_D \exp(U_{DC} - U_{FC})]^{-1}\}E_S^{-1}. \tag{41}$$

Similarly, the analytic expressions of the electron and hole charge-control or charge-storage capacitances are obtained:

$$C_n = qN_C[F_{1/2}(U_S - U_{FC}) - F_{1/2}(-U_{FC})]E_S^{-1}, \tag{42}$$

$$C_p = -qN_V[F_{1/2}(U_{FC} - E_G/kT - U_S) - F_{1/2}(U_{FC} - E_G/kT)]E_S^{-1}. \tag{43}$$

The first derivative and second derivative of the electron and hole charge-storage capacitances and the electron trapping capacitance with respect to the surface potential can be readily obtained from Eqs. (41)–(43). These are useful in distortion and noise analyses.

Taking phosphorus as the donor impurity, whose measured trapped electron ground state energy in Si is $E_C - E_D = 45.5$ meV, or $V_{DC} = 45.5$ mV. The ground state degeneracy is the product of the spin degeneracy and the configuration (or space) degeneracy from the six conduction band valleys, $g_D = g_S \times g_C = 2 \times 6 = 12$. {See page 204 and Fig. 252.2 of Ref. [2].} We defer the effects of excited states to our next and second report. A more general case of trapping capacitance of a two-energy-level and three-charge-state impurity center in semiconductor, such as the sulfur double donor and the zinc double acceptor in silicon, was computed and discussed in Ref. [3].

3. Low-Frequency and High-Frequency Gate Capacitances

Low-frequency and high-frequency gate capacitances of the n-Si MOS capacitors with an unlimited hole and electron source connected to the n-type substrate is our example model for this feasibility study. Considering the gate oxide capacitance C_{ox} is in series with the semiconductor capacitance, the two limiting-frequency gate capacitances were derived and listed in Eqs. (4) and (5) in Section 2, which are repeated below:

$$C_{gb\text{-}hf} = C_{ox} \times (C_{nt} + C_n + C_p)/(C_{ox} + C_{nt} + C_n + C_p), \tag{4}$$

$$C_{gb\text{-}hf} = C_{ox} \times (C_n + C_p)/(C_{ox} + C_n + C_p). \tag{5}$$

Since C_{ox} can be accurately extracted from the low-frequency gate capacitance versus dc gate voltage curve, it is treated as a known parameter. Solving Eqs. (4) and (5), we obtain the following:

$$C_{nt} = C_{ox}^2 \times (C_{gb\text{-}lf} - C_{gb\text{-}lf}) \div (C_{ox} - C_{gb\text{-}lf}) \div (C_{ox} - C_{gb\text{-}lf}). \tag{44}$$

The above formula can be used to extract C_{nt} from the two experimental gate capacitances at low and high frequencies, which are directly measured.

The first derivative and second derivative of the two gate capacitances with respect to the dc gate voltage can also be measured from the MOS capacitors under test. The theoretical computations of these derivatives can be performed using the following equations:

$$dV_S/dV_{GB} = [1 + (C_{nt} + C_n + C_p)/C_{ox}]^{-1}, \tag{45}$$

$$\begin{aligned} d^2V_S/dV_{GB}^2 = &-[1 + (C_{nt} + C_n + C_p)/C_{ox}]^{-2} \div C_{ox} \\ &\times (dC_{nt}/dV_S + dC_n/dV_S + dC_p/dV_S) \times dV_S/dV_{GB}, \end{aligned} \tag{46}$$

$$d^2C_{nt}/dV_{GB}^2 = d^2C_{nt}/dV_S^2 \times (dV_S/dV_{GB})^2 + dC_{nt}/dV_S \times d^2V_S/dV_{GB}^2, \quad (47)$$

$$d^2C_n/dV_{GB}^2 = d^2C_n/dV_S^2 \times (dV_S/dV_{GB})^2 + dC_n/dV_S \times d^2V_S/dV_{GB}^2, \quad (48)$$

$$d^2C_p/dV_{GB}^2 = d^2C_p/dV_S^2 \times (dV_S/dV_{GB})^2 + dC_p/dV_S \times d^2V_S/dV_{GB}^2, \quad (49)$$

$$dC_{gb\_lf}/dV_{GB} = C_{ox}^2/(C_{ox} + C_{nt} + C_n + C_p)^2 \times (dC_{nt}/dV_S + dC_n/dV_S + dC_p/dV_S) \times dV_S/dV_{GB}, \quad (50)$$

$$d^2C_{gb\_lf}/dV_{GB}^2 = C_{ox}^2/(C_{ox} + C_{nt} + C_n + C_p)^3 \times (dC_{nt}/dV_S + dC_n/dV_S + dC_p/dV_S)^2 \times (dV_S/dV_{GB})^2 + C_{ox}^2/(C_{ox} + C_{nt} + C_n + C_p)^2 \times (d^2C_{nt}/dV_{GB}^2 + d^2C_n/dV_{GB}^2 + d^2C_p/dV_{GB}^2), \quad (51)$$

$$dC_{gb\_hf}/dV_{GB} = C_{ox}^2/(C_{ox} + C_n + C_p)^2 \times (dC_n/dV_S + dC_p/dV_S) \times dV_S/dV_{GB}, \quad (52)$$

$$d^2C_{gb\_hf}/dV_{GB}^2 = C_{ox}^2/(C_{ox} + C_n + C_p)^3 \times (dC_n/dV_S + dC_p/dV_S)^2 \times (dV_S/dV_{GB})^2 + C_{ox}^2/(C_{ox} + C_n + C_p)^2 \times (d^2C_n/dV_{GB}^2 + d^2C_p/dV_{GB}^2). \quad (53)$$

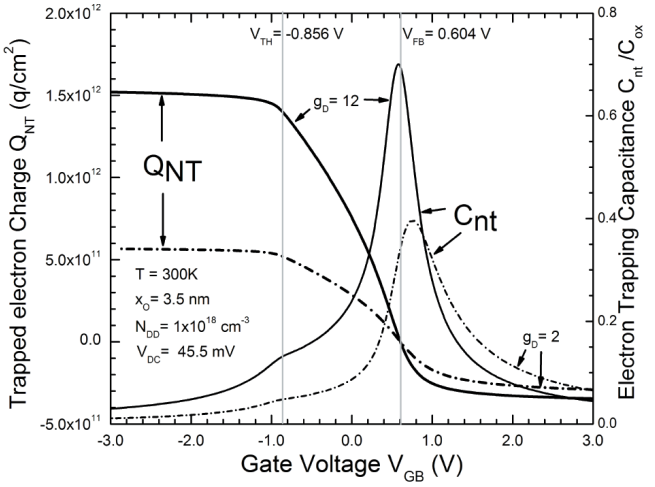

Fig. 1. Stored trapped electron charge areal density Q_{NT} and electron trapping capacitance C_{nt} of a n-Si MOS capacitor versus the applied gate voltage. The capacitor has a temperature T of 300 K, a gate oxide thickness x_O of 3.5 nm, and the donor (phosphorus) impurity volume density N_{DD} of 10^{18} cm^{-3}. Two vertical lines label the flatband voltage $V_{FB} = 0.604$ V and the threshold voltage $V_{TH} = -0.856$ V when $g_D = 12$. The two $g_D = 2$ curves show the degeneracy effect.

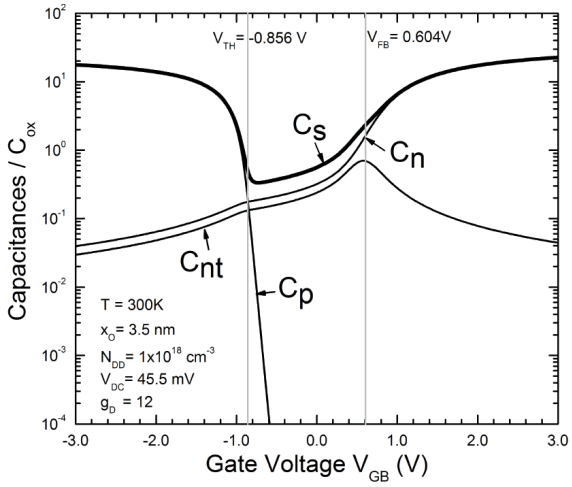

Fig. 2. Semiconductor capacitance C_s and its three components, electron trapping capacitance, electron and hole charge-control capacitances C_{nt}, C_n and C_p, of a n-Si MOS capacitor versus the applied gate voltage. The capacitor parameters: $T = 300$ K, $x_O = 3.5$ nm, $N_{DD} = 10^{18}$ cm^{-3}, $V_{FB} = 0.604$ V, and $V_{TH} = -0.856$ V.

4. Computation Results

To illustrate the typical characteristics of MOS capacitors with trapping at the dopant impurity centers, we wrote the formulae in Sections 2 and 3 into an Intel Visual Fortran program, and run this program on an Lenovo ThinkPad T60 notebook computer with Windows XP PRO and the Intel Visual Fortran Compiler 10.0. We then used Origin Pro 8.5 to plot all curves in the figures presented in this report.

Figure 1 shows the trapped electron charge density Q_{NT} and electron trapping capacitance C_{nt} of an n-Si MOS capacitor versus the DC voltage applied to the gate relative to the body or bulk, V_{GB}. As mentioned in Section 2, there are only donor (phosphorus) impurity atoms in the substrate of the capacitor, and their volume density is taken to be $N_{DD} = 10^{18}$ cm^{-3} for this example. Its gate electrode is made of Aluminum, its gate oxide thickness $x_O = 3.5$ nm, and the temperature is $T = 300$ K. The flatband and surface inversion threshold (or strong hole channel on the n-Si surface) gate voltages when $g_D = 12$ are computed to be $V_{FB} = +0.604$ V and $V_{TH} = -0.856$ V, which are indicated by two vertical solid lines. In the strong surface inversion range, $V_{GB} < -1.0$ V, and in the strong surface accumulation range, $V_{GB} > +1.8$ V, the gate voltage drops almost all through the gate oxide due to the thin silicon layer of huge hole concentration (the hole inversion layer) and electron concentration (the electron accumulation layer). These high concentrations also result in the saturation or almost constant Q_{NT} versus V_{GB} shown in Fig. 1, hence the small values of the C_{nt}. In contrast, in the weak inversion and depletion ranges, and the weak accumulation range, -1.0 V $< V_{GB} < 1.8$ V, the energy band bending in the silicon surface space charge layer strongly depends on the gate voltage, hence the electron and hole concentrations at the interface, $x = 0$, nearly exponentially on the gate voltage, which results in sharp rise of the trapped charge Q_{NT} with decreasing V_{GB} and a large peak of the electron trapping C_{nt}, almost 70% of C_{ox} near flat-band when $g_D = 12$.

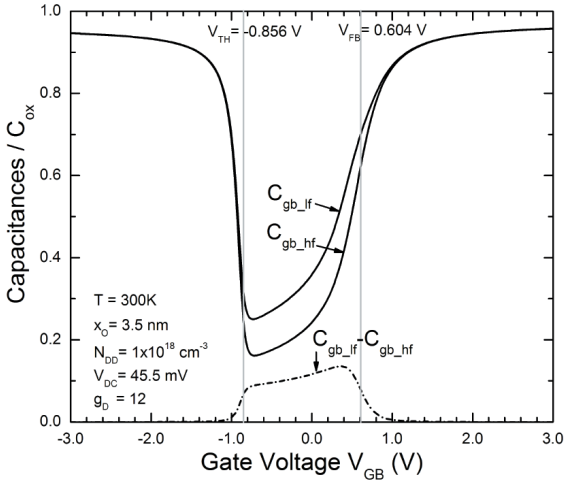

Fig. 3. Low-frequency and high-frequency gate capacitances, $C_{\rm gb\_lf}$ and $C_{\rm gb\_hf}$, and their difference ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) in a MOS capacitor versus the applied gate voltage. The capacitor parameters: $T = 300$ K, $x_{\rm O} = 3.5$ nm, $N_{\rm DD} = 10^{18}$ cm^{-3}, $V_{\rm FB} = 0.604$ V, and $V_{\rm TH} = -0.856$ V.

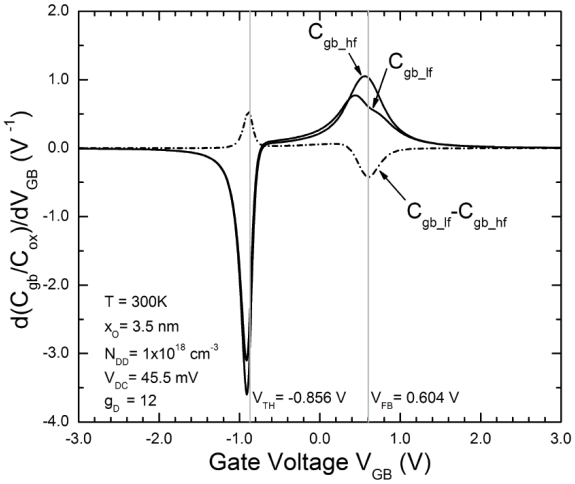

Fig. 4. First derivatives of low-frequency and high-frequency gate capacitances, $\mathrm{d}C_{\rm gb\_lf}/\mathrm{d}V_{\rm GB}$ labeled by $C_{\rm gb\_lf}$ and $\mathrm{d}C_{\rm gb\_hf}/\mathrm{d}V_{\rm GB}$ labeled by $C_{\rm gb\_hf}$, and their difference $\mathrm{d}(C_{\rm gb\_lf} - C_{\rm gb\_hf})/\mathrm{d}V_{\rm GB}$ labeled by ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) in a MOS capacitor versus the applied gate voltage. The capacitor parameters: $T = 300$ K, $x_{\rm O} = 3.5$ nm, $N_{\rm DD} = 10^{18}$ cm^{-3}, $V_{\rm FB} = 0.604$ V, and $V_{\rm TH} = -0.856$ V.

Note also a small structure in $C_{\rm nt}$ at $V_{\rm GB} = -0.9$ V, slightly beyond the surface inversion point.

Figure 2 shows semiconductor capacitance $C_{\rm s}$ and its three components: the electron trapping capacitance, and the electron and hole charge-storage (or charge-control) capacitances, $C_{\rm nt}$, $C_{\rm n}$ and $C_{\rm p}$. In the strong inversion range, hole charge-storage capacitance $C_{\rm p}$ is dominant due to the hole inversion layer; in the strong accumulation range, electron charge-storage capacitance $C_{\rm n}$ is dominant due to the electron accumulation layer. Since holes are the minority carriers, when the absolute value of the gate voltage is less than the absolute value of threshold voltage, hole surface concentration decreases exponentially with increasing $V_{\rm GB}$, thus, $C_{\rm p}$ decreases exponentially as show in the figure. From the weak inversion range to the weak accumulate range, $C_{\rm s}$ is actually mainly the sum of $C_{\rm nt}$ and $C_{\rm n}$.

Figure 3 shows low-frequency and high-frequency gate capacitances, $C_{\rm gb\_lf}$ and $C_{\rm gb\_hf}$, and their difference ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$), all normalized to $C_{\rm ox}$. From Eq. (44), the charge storage capacitance from electron trapping at the donor impurity or the electron trapping capacitance $C_{\rm nt}$ is directly related to the difference ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$). Thus the difference can be readily measured experimentally to characterize the impurity deionization or electron trapping at the dopant impurity centers in the n-Si MOS capacitor. The difference has significant values only from the weak accumulation range to the weak inversion range. This is expected from the fact observed in Fig. 2 that the $C_{\rm nt}$ contributes significantly to the $C_{\rm s}$ only from the weak accumulation range to the weak inversion range. Figures 4 and 5 show, respectively, the first and second derivatives of the low-frequency and high-frequency gate capacitances, $C_{\rm gb\_lf}$ and $C_{\rm gb\_hf}$, and their difference ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$). The cardinal feature is that the positive and negative peaks and zeroths pin point the flat band and surface inversion conditions, not unlike the many fundamental measurements in the physics and chemistry of materials.

Figures 6–8 show the dependences of the gate capacitance

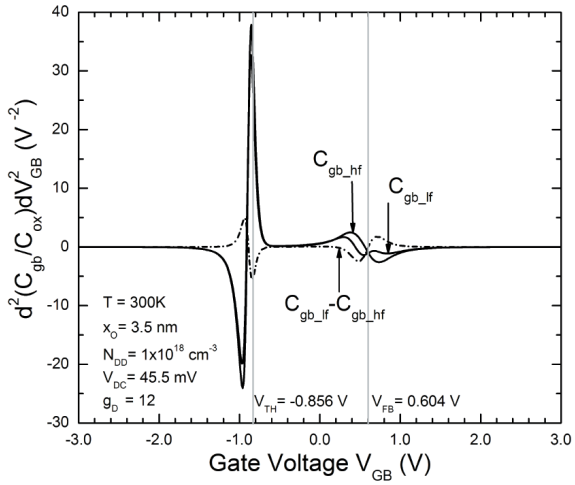

Fig. 5. Second derivatives of low-frequency and high-frequency gate capacitances, $\mathrm{d}^2C_{\rm gb\_lf}/\mathrm{d}V_{\rm GB}^2$ labeled by $C_{\rm gb\_lf}$ and $\mathrm{d}^2C_{\rm gb\_hf}/\mathrm{d}V_{\rm GB}^2$ labeled by $C_{\rm gb\_hf}$, and their difference $\mathrm{d}^2(C_{\rm gb\_lf} - C_{\rm gb\_hf})/\mathrm{d}V_{\rm GB}^2$ labeled by ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) in a MOS capacitor versus the applied gate voltage. The capacitor parameters: $T = 300$ K, $x_{\rm O} = 3.5$ nm, $N_{\rm DD} = 10^{18}$ cm^{-3}, $V_{\rm FB} = 0.604$ V, and $V_{\rm TH} = -0.856$ V.

difference ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) respectively on the impurity volume density $N_{\rm DD}$, temperature T, and gate oxide thickness $x_{\rm O}$. The temperature dependence comes through the material parameters $N_{\rm C}$, $N_{\rm V}$, and $E_{\rm G}$. {see Eqs. (233.8B), (233.10B), and (241.3A) of Ref. [9]}. When impurity volume density $N_{\rm DD}$ increases and when temperature T decreases, fewer electrons are detrapped or more electrons are trapped, thus, the electron trapping capacitance increases, resulting in the larger difference of ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$). Since the increasing $N_{\rm DD}$ increases the threshold voltage more significantly than the decreasing T, the line-shape in Fig. 6 stretches out to the left (inversion) while the line-shape in Fig. 7 stretches vertically. Since the gate oxide

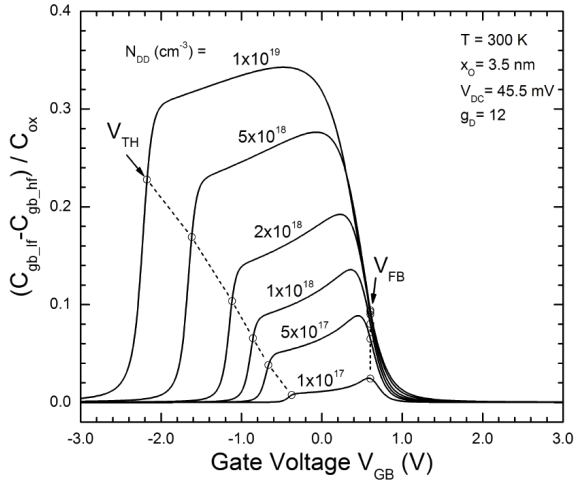

Fig. 6. Donor impurity concentration dependence of the difference of low-frequency and high-frequency gate capacitances ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) of n-Si MOS capacitors. The flatband and threshold voltages are indicated by the open circles. The capacitor parameters: $T = 300$ K, $x_{\rm O} = 3.5$ nm, $N_{\rm DD} = 1 \times 10^{17}$, 5×10^{17}, 1×10^{18}, 2×10^{18}, 5×10^{18}, 1×10^{19} $\rm cm^{-3}$.

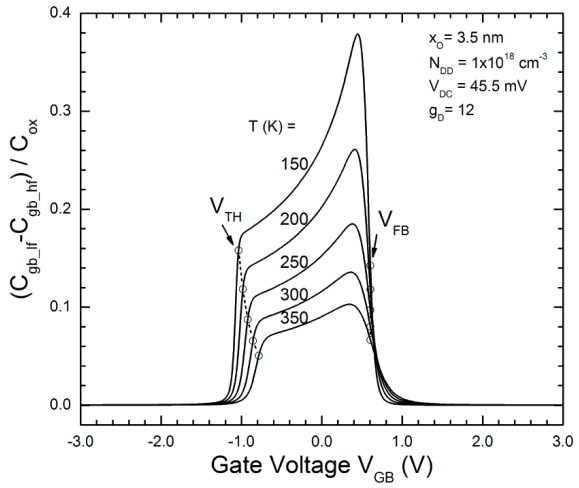

Fig. 7. Temperature dependence of the difference of low-frequency and high-frequency gate capacitances ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) of n-Si MOS capacitors. The flatband and threshold voltages are indicated by the open circles. The capacitor parameters: $T = 150$, 200, 250, 300, 350 K, $x_{\rm O} = 3.5$ nm, $N_{\rm DD} = 10^{18}$ $\rm cm^{-3}$.

thickness is not directly related to the impurity deionization, the change of the shape in Fig. 8 is significantly less than those in Figs. 6 and 7. However, the thinner oxide sharpens the peak near flat-band.

5. Summary

Theoretical calculations presented in this paper show that the frequency dependence of the capacitance due to carrier trapping at the dopant impurity center provides, as previously anticipated, a highly sensitive means of characterization of the properties of the dopant impurity centers in semiconductors. The numerical examples at 300 K and 3.5 nm oxide,

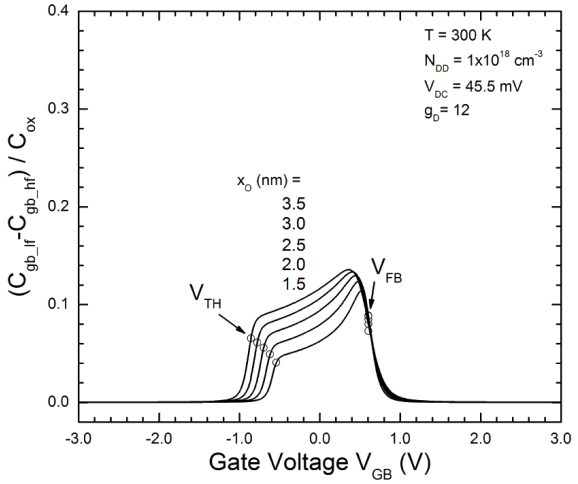

Fig. 8. Gate oxide thickness dependence of the difference of low-frequency and high-frequency gate capacitances ($C_{\rm gb\_lf} - C_{\rm gb\_hf}$) of n-Si MOS capacitors. The flatband and threshold voltages are indicated by the open circles. The capacitor parameters: $T = 300$ K, $x_{\rm O} = 1.5$, 2.0, 2.5, 3.0, 3.5 nm, $N_{\rm DD} = 10^{18}$ $\rm cm^{-3}$.

with ground state degeneracy $g_{\rm D} = 12$, neglecting the excited states, such as those of phosphorus donor in silicon, show large differences between the high and low frequency capacitances in the subthreshold gate voltage range, between flat-band and strong-inversion threshold gate voltages, from about 2% of the oxide capacitance at a phosphorus donor dopant impurity concentration of 10^{17} $\rm cm^{-3}$, rising to 35% of the oxide capacitance at a phosphorus donor impurity concentration of 10^{19} $\rm cm^{-3}$. Therefore, the use of the trapping capacitance, at the dopant impurity centers in a MOS capacitance are feasible as a high speed random access storage, which can be further integrated with the MOS gate of the signal processing MOS transistor. In addition, the large trapping capacitance provides a means for measurement of the fundamental parameters of the dopant impurities, in addition to its applications in the profiling the impurity concentrations in technology development and monitoring.

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