Effect of CdS Processing Conditions on the Properties of CdS/Si Diodes and CdS/CdTe Thin-Film Solar Cells

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***Abstract*—Thermally evaporated n-type CdS thin films were studied to determine the influence of substrate deposition temperature and postdeposition thermal annealing on their electrical, optical, and structural properties. It is shown that although increasing substrate temperature during deposition from room temperature to 200 °C results in CdS films exhibiting high optical transmittance as well as large grain size, deposition temperatures above 50 °C lead to significant degradation in carrier concentration and mobility. Postdeposition thermal annealing of CdS films deposited at room temperature is shown to yield CdS films with superior electrical and optical characteristics, resulting in an electron mobility of 17.45 cm^2/Vs for films annealed at 200 °C. The electrical characteristic of n-CdS/p-Si heterojunction diodes indicated that postdeposition thermal annealing reduced parasitic series resistance and decreased the diode ideality factor to a value of 1.384 for films annealed at 300 °C, suggesting a reduction in recombination centers in the vicinity of the CdS/Si interface. In n-CdS/p-CdTe heterojunction solar cells, the photovoltaic cell parameters indicated that the deposition of CdS films at room temperature produces better performing cells with the substrate temperature required during the thermal deposition of CdTe acting as postdeposition annealing for the underlying CdS thin film.**

***Index Terms*—CdS, CdS/CdTe solar cell, CdS/Si heterojunction, thermal annealing, thermal evaporation.**

I. Introduction

CADMIUM sulfide (CdS) is a direct bandgap II–VI compound semiconductor which has a number of attractive features for electronic and optoelectronic applications [1], [2]. CdS is best known for its application in thin-film heterojunction photovoltaic cells as an n-type contact and window layer on p-type CdTe or CuIn(Ga)Se absorber layers [3]–[7], since solar radiation is minimally absorbed within the wide bandgap n-type CdS layer and is, thus, efficiently absorbed within the narrower bandgap p-type absorber layer [8]. CdS has also been investigated as a window and contact layer for Si-based photovoltaic applications [9], [10] and as an electronic and optoelectronic material for nanowire [11] and quantum-dot-based devices [12]. Many techniques have been employed to deposit CdS thin films, such as sputtering [13], [14], close-spaced sublimation [15], and chemical-bath deposition [16]–[18]. Previous studies have noted that the properties of CdS thin films are strongly influenced by the deposition method and the specific conditions employed during the deposition process [19], [20]. Thermal evaporation, which is a thin-film deposition technique that is widely used in the semiconductor industry because of its relative simplicity, allows for the optimization of the deposited CdS films through the control of substrate temperature and deposition rate [19], [21], [22]. In our previous study [23], substrate temperature effects during the deposition of CdS films were investigated regarding film properties and device characteristics. However, photovoltaic properties were not able to be explained clearly because of postdeposition temperature effects during the CdTe deposition. In this study, postdeposition thermal annealing was found to have a greater effect than the substrate deposition temperature in improving the electrical and optical properties of the CdS thin films. Heterojunction n-CdS/p-Si diodes were fabricated by depositing CdS thin films on p-silicon at room temperature, which were subsequently annealed at various temperatures to investigate the influence of annealing temperature on device performance. Finally, the effects of substrate temperature and postdeposition annealing of CdS thin films in n-CdS/p-CdTe heterojunction solar cells were characterized in terms of photovoltaic cell parameters.

II. Experimental Techniques

The properties of CdS were initially investigated using thin films thermally evaporated onto glass slides. The glass substrates were cleaned in consecutive baths of acetone, methanol, and isopropyl alcohol, and then washed in a warm deionized water ultrasonic bath. The CdS thin films were deposited by a thermal evaporation technique using a 99.99% purity evaporation source at a base pressure of $< 1 \times 10^{-6}$ mbar, with a substrate to evaporation source distance of 19 cm. The 1-μm-thick CdS films were deposited at different substrate temperatures from room temperature to 200 °C at deposition rates varied from 7 to 6 Å/s owing to the increase in substrate temperature. The optical and structural properties of the films were investigated via optical spectroscopy, X-ray diffraction (XRD), and scanning electron microscopy (SEM). Hall effect measurements were employed

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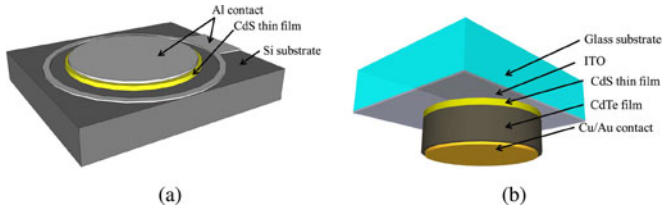

Fig. 1. Schematics of fabricated devices. (a) n-CdS/p-Si heterojunction with Si wafer in substrate configuration and (b) n-CdS/CdTe heterojunction with ITO coated glass in superstrate configuration.

to characterize the carrier concentration and mobility in the deposited films. In order to investigate the effect of postdeposition thermal treatment, the samples were annealed for 1 h at temperatures of 100, 200, and 300 °C, in a quartz tube furnace under flowing N_2 ambient conditions. All the above detailed measurements and analysis procedures were also performed on the postdeposition annealed samples.

Heterostructure n-CdS/p-Si junctions were formed by the thermal evaporation of 200-nm-thick CdS on boron-doped p-type (100) silicon substrates (100–150 Ω· cm), with the substrate held at room temperature. Prior to CdS deposition, any native oxide on the Si substrate was removed in 30% diluted HF solution. The as-deposited n-CdS/p-Si heterojunctions were then annealed at temperatures in the range of 100 to 300 °C for 1 h. Prior to forming ohmic contacts using thermally evaporated Al, device structures were defined by mesa etch to separate p-type Si and n-type CdS contact regions [see Fig. 1(a)]. Diode electrical characteristics were investigated employing room temperature current–voltage (*I–V*) measurements performed using a HP 4156A precision semiconductor parameter analyzer.

The n-CdS/p-CdTe heterojunction solar cells were fabricated by the thermal deposition of CdS and CdTe thin films on commercial ITO-coated glass substrates (ITO properties: 9–15 Ω/sq, 180 nm thick). Prior to thin-film deposition, the ITO substrates were cleaned in conventional solvents and subsequently annealed at 500 °C for 10 min in an N_2 ambient. This step was found to be necessary in order to prevent delamination of the CdS thin films, which had been observed in previous experiments, and found to occur after high temperature annealing following the $CdCl_2$ treatment. The 150-nm-thick CdS films were thermally deposited at substrate temperatures ranging from room temperature to 200 °C, and some of the films deposited at room temperature also underwent a postdeposition annealing at either 200 or 300 °C. The CdTe films (3.5 μm thick) were thermally deposited at a substrate temperature of 330 °C, at a deposition rate of ∼7 Å/s. To improve the electrical characteristics of the as-deposited CdTe films, a $CdCl_2$ treatment was performed by dipping the samples in a boiling $CdCl_2$-methanol solution, followed by an N_2 blow-dry and subsequent annealing at 420 °C in air for 7 min. The devices were electrically isolated by defining mesa structures by etching in a Br_2:HBr:H_2O (1:20:20) solution. Prior to the formation of ohmic contacts, the CdTe thin-film contact surface area was lightly etched in a bromine–methanol solution to remove any $CdCl_2$ residue, and to form a Te-rich surface. Ohmic contacts were formed by thermal evaporation of 5 nm Cu and 80 nm Au, which were then annealed at 250 °C in an N_2 ambient for 3 min in order to achieve low-resistance ohmic contacts to the CdTe. The fabricated n-CdS/p-CdTe thin-film heterojunction solar cell is depicted in Fig. 1(b). All photovoltaic cell parameters were extracted under AM 1.5G illumination.

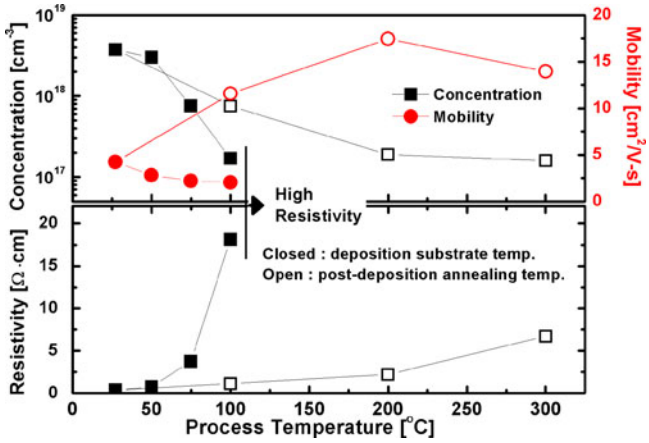

Fig. 2. Results of Hall effect measurements (carrier concentration, mobility and resistivity) on n-CdS thin films deposited on glass substrates as a function of substrate temperature during deposition (closed symbols) and postdeposition annealing temperature (open symbols).

III. Results and Discussion

A. *Effect of Annealing on CdS Film Properties*

The effect of process temperature during deposition and after deposition on the electronic transport parameters of CdS thin films deposited on glass is illustrated in Fig. 2; the carrier concentration N, mobility μ, and resistivity ρ were extracted from Hall effect measurements performed at room temperature under dark conditions. Although CdS thin films were deposited at substrate temperatures up to 200 °C, it was not possible to perform reliable Hall effect measurements on the thin films deposited above 100 °C because of their extremely high resistivity as shown in Fig. 2 (closed symbols). In contrast, CdS films deposited on glass at room temperature exhibited low resistivity (0.39 Ω · cm), and were found to be n-type with a free electron concentration of 3.74×10^{18} cm^{-3} and an electron mobility of 4.24 cm^2/Vs. Native defects, such as sulfur vacancies and cadmium interstitials, are likely to be the dominant donor-like defects responsible for the observed n-type character [24], [25]. Increasing the substrate temperature resulted in degradation in electron mobility, and a decrease in the electron concentration, with CdS films deposited at 100 °C exhibiting an electron mobility of 2.03 cm^2/Vs and a carrier concentration of 1.7×10^{17} cm^{-3}, resulting in an increased resistivity of 18.13 Ω · cm. The observed influence of deposition substrate temperature on the electrical properties of CdS thin films indicates that substrate temperature has a significant impact on film stoichiometry. Increasing the substrate temperature changes the sticking coefficients of both Cd and S species; thus, acting to affect the Cd/S ratio during deposition. The sticking coefficient of Cd has been

found to decrease with increasing substrate temperature [21], [22], and sulfur reevaporation has been found to be important at high substrate temperature [21]. In this context, it is important to note that the Cd/S ratio has a significant influence on both the optical and electrical properties of CdS thin films. Typically, Cd-rich thin films show low resistivity and low transmittance, whereas the opposite has been reported for CdS films deposited under sulfur-rich conditions [21], [22], [26]–[28]. It is noted that the low resistivity and high carrier concentration exhibited by CdS films deposited at room temperature renders them suitable for application in photovoltaic devices, since a low resistivity is important to decrease the device sheet resistance and to obtain a high open-circuit voltage [29]. Postdeposition thermal annealing for 1 h was then employed to attempt further optimization of the properties of CdS films deposited at room temperature. The effect of postdeposition annealing temperature on the room temperature carrier concentration, mobility, and resistivity is shown in Fig. 2 (open symbols), where it is evident that thermal annealing has resulted in a significant increase in electron mobility for all annealing temperatures, monotonically increasing with temperature up to 200 °C and decreasing thereafter. At 200 °C, the electron mobility was measured to be 17.45 cm^2/Vs. In contrast, the free electron concentration was found to monotonically decrease with increasing annealing temperature. As evident from Fig. 2, the rate at which the carrier concentration decreases with increasing annealing temperature was significantly lower than the rate at which the carrier concentration decreased with increasing substrate temperature during deposition. This suggests, together with the observed increase in electron mobility, that the dominant physical mechanisms responsible for the observed temperature dependence during deposition and during postdeposition annealing are significantly different. In the case of increasing substrate temperature during deposition, the formation of defects is determined by the resulting effective Cd/S ratio, whereas increasing the postdeposition annealing temperature induces defect migration and annihilation [27], [28]. The annihilation of defects present in the as-deposited films during thermal annealing effectively reduces the density of scattering centers; thus, resulting in a significant increase in electron mobility. The concomitant decrease in carrier concentration suggests the possible participation of native donor-like centers in the defect annihilation process that leads to higher electron mobility.

SEM revealed that the surface morphology of the CdS films was influenced by deposition temperature. As illustrated in Fig. 3(a), CdS films deposited at room temperature exhibited a granular surface morphology which was moderately influenced by substrate temperature during deposition up to 150 °C [as can be seen in Fig. 3(b)]. Significant grain growth was evident for temperatures above 150 °C, as shown in Fig. 3(c). Interestingly, CdS films postdeposition annealed at 300 °C showed small-grain surface morphology, as illustrated in Fig. 3(d).

The XRD spectra for CdS thin films deposited or postannealed at different substrate temperatures are shown in Fig. 4, which were obtained by scanning 2θ in the 20°–70° range. The significant overlap and/or close proximity of the H(002), H(112), and H(004) peaks of the hexagonal phase and the C(111), C(311), and C(222) peaks of the cubic phase made it difficult to

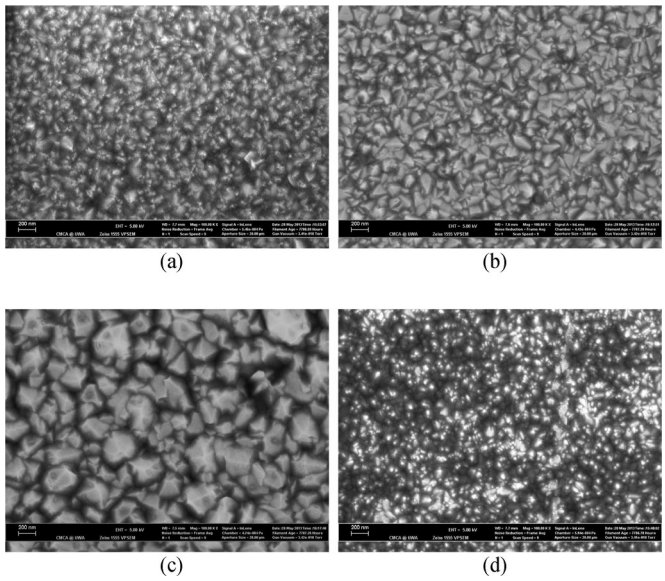

Fig. 3. SEM surface images. (a)–(c) CdS films deposited at different substrate temperature, (d) CdS film deposited at room temperature and post-deposition annealed at 300 °C for 1 h. (a) Deposited at room temperature. (b) Deposited at 150 °C. (c) Deposited at 200 °C. (d) Postannealed at 300 °C.

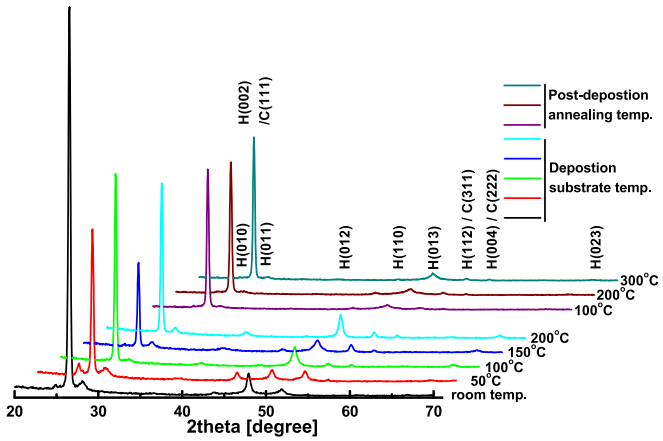

Fig. 4. XRD spectra of CdS thin films as a function of deposition substrate temperatures and postdeposition annealing temperatures.

unambiguously distinguish between cubic and hexagonal structure. It was found that distinct diffraction peaks appeared at around $2\theta = 26.53°$, 28.21°, 47.89°, and 51.89°, which were assigned to the (h k l) = H(002) or C(111), H(011), H(013), and H(112), or C(311) planes, respectively, with the H(002)/C(111) being the dominant XRD peak. Other peaks that became distinguishable in samples deposited at higher substrate temperatures were found at 36.85°, assigned to H(012); and 54.64° assigned to either H(004) or C(222). However, the peaks at 24.92°, assigned to H(010), and 43.73°, corresponding to H(110), were found not to be present in samples deposited at higher substrate temperatures. The above results suggest that phase transitions within the mixed (cubic and hexagonal) structure of the CdS films occurred as the substrate deposition temperature was increased. In CdS films, which were thermally annealed after deposition,

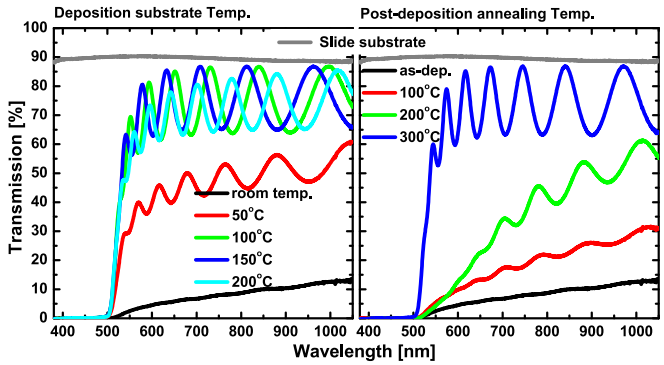

Fig. 5. Transmission spectra of 1-μm-thick CdS thin films on glass slides. (a) CdS films deposited at different substrate temperatures. (b) CdS film deposited at room temperature and postdeposition annealed for 1 h at different temperature.

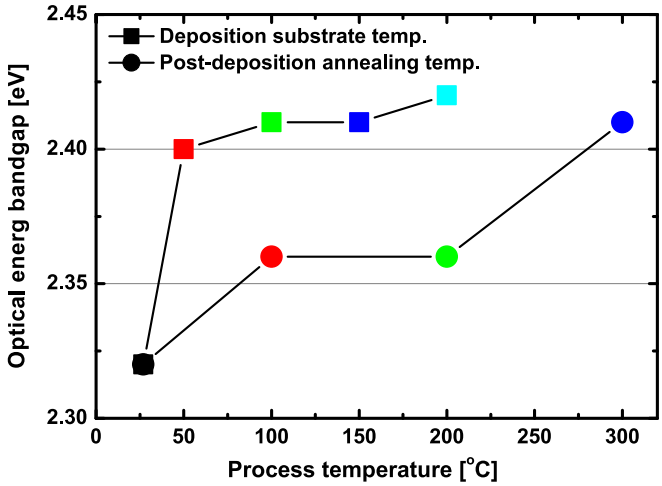

Fig. 6. Extracted energy bandgap of CdS thin films as a function of different deposition substrate temperatures and postdeposition annealing temperatures.

the H(002)/C(111) was found to remain the dominant XRD peak, even after annealing for 1 h, suggesting that postdeposition annealing induced no significant phase transitions. These observations are consistent with the electrical characterization results discussed previously.

A particularly important parameter in photovoltaic-cell applications is the optical transmittance of the deposited CdS films, since they are usually employed as a wide bandgap n-type window layer in solar cells. The optical transmittance spectra of CdS films prepared at different temperatures measured over the 380–1050 nm wavelength range are presented in Fig. 5, where the interference fringes associated with multiple reflections within the deposited layer are clearly evident [30]. The transmittance of the CdS thin films was found to increase as the temperature of the substrate was increased during deposition, with films deposited at above 100 °C exhibiting >73% transmittance for wavelengths above 600 nm, which was limited by the 89% transmittance of the glass substrate. Although the increase in optical transmittance achievable at deposition temperatures near and above 100 °C is desirable for CdS films as window layers, the relatively high resistivity of such films impacts negatively on solar-cell efficiency. Postdeposition annealing for 1 h was also found to lead to a significant increase in optical transmittance with increasing annealing temperature. Films annealed at 300 °C exhibited optical transmittance >73% for wavelengths above 600 nm, whereas annealing at lower temperatures resulted in films with poor optical transmittance characteristics. It is important to note that the above results indicate that the CdS films deposited at room temperature and postdeposition annealed at 300 °C for 1 h exhibit excellent optical and electrical characteristics for solar cell and optoelectronic device applications.

The optical energy bandgap E_g of the samples was extracted following the method of Tauc *et al.* [31], i.e., from the intercept of the extrapolated linear region of the $(\alpha E)^2$ versus photon energy E characteristics, since

$$\alpha = \frac{B(E - E_g)^{1/2}}{E} \tag{1}$$

where α is the absorption coefficient, E is the photon energy, and B is a form factor that depends on the transition probability, which is assumed to be constant within the optical frequency range [30], [31]. The absorption coefficient of each sample was extracted from the transmittance data using [32]

$$\alpha = \frac{1}{d} \ln \left[\frac{(1-R)^2}{2T} + \sqrt{\frac{(1-R)^4}{4T^2} + R^2} \right] \tag{2}$$

where T is the transmittance, R is the reflectance, and d is the thickness of the CdS film.

The optical energy bandgap values extracted employing the above approach are presented in Fig. 6. The bandgap of CdS films was found to marginally increase from 2.32 up to 2.42 eV with increasing deposition temperature, and up to 2.41 eV with increasing postdeposition annealing temperature. These observations are in agreement with previously reported values [33], [34].

B. Heterojunction Diodes

1) CdS/Si Heterojunction Diodes: The n-CdS/p-Si heterojunction diodes were fabricated by depositing 200-nm-thick layers of n-type CdS on p-type silicon substrates at room temperature, followed by postdeposition annealing for 1 h at temperatures from 100 to 300 °C. The resultant device structures are shown in Fig. 1(a). *I–V* characteristics of the fabricated diodes are shown in Fig. 7, where it can be clearly seen that all devices exhibited good rectifying characteristics. The diode ideality factor, which is a key current transport parameter in p-n junction devices [35], was extracted from the *I–V* characteristics using the ideal diode equation, including series resistance r_s and shunt resistance r_{sh}

$$J = J_0 \left[\exp\left(\frac{q}{nkT_s}(V_a - r_s J) \right) - 1 \right] + \frac{V_a}{r_{\text{sh}}} \tag{3}$$

where J_0 is the diode saturation current density, V_a is applied bias, k is Boltzmann's constant, and T_s is the sample temperature. The ideality factor n was extracted from the *I–V* characteristics for $V_a > 3kT_s$, whereas the series resistance was

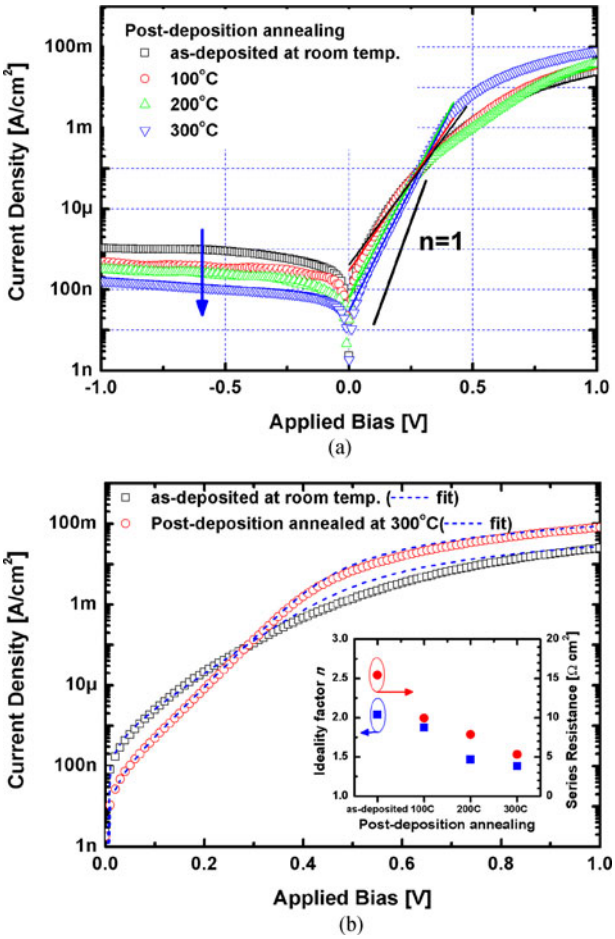

Fig. 7. (a) Experimental *I–V* characteristics of n-CdS/p-Si heterojunction diodes as a function of CdS postdeposition annealing temperature for 1 h, indicating the bias regions from which the diode ideality factors and series resistances were extracted. (b) Experimental and calculated forward *I–V* characteristics. The calculated characteristic employs a simple homogeneous p-n junction model (3). (Inset) Extracted diode ideality factors and series resistances.

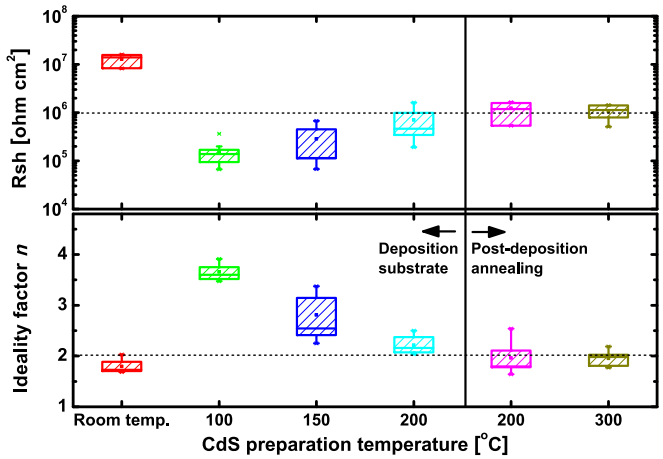

Fig. 8. Shunt resistance and ideality factor extracted from dark *I–V* curves for n-CdS/p-CdTe solar cells.

extracted from the linear region for $V_a > 0.8$ V. As evident from Fig. 7(b), the as-deposited samples exhibited a relatively high ideality factor (2.04 ± 0.04), a series resistance of 15.45 ± 0.13 $\Omega{\cdot}\text{cm}^2$, and diode *I–V* characteristics that departed significantly from those modeled by (3) for $V_a > 0.4$ V. This suggests that current transport across the n-CdS/p-Si junction is likely to be nonhomogenous, and that there is a relatively high density of recombination centers in the vicinity of the heterojunction interface, which are likely to be associated with grain boundaries in the as-deposited CdS film at or near the CdS/Si heterojunction. As illustrated in Fig. 7, postdeposition annealing was found to significantly reduce the reverse leakage current, series resistance, and ideality factor. CdS films annealed at 300 °C were characterized by an ideality factor n of 1.384 ± 0.002, a series resistance r_s of 5.32 ± 0.03 $\Omega \cdot \text{cm}^2$, and a diode saturation current J_0 of 3.4×10^{-8} A $\cdot$ cm^{-2}. The analysis of the reverse *I–V* characteristics indicated that, for all devices, reverse leakage current was dominated by diode shunt resistance. The extracted shunt resistance was 1×10^6 $\Omega{\cdot}\text{cm}^2$ for diodes with as-deposited CdS and $8 \times 10^6 \Omega \cdot \text{cm}^2$ for devices annealed at 300 °C. Thus, the n-CdS/p-Si diode characteristics indicate that postdeposition thermal annealing leads to a significant improvement in the electrical characteristics of the CdS/Si interface, as well as of the "bulk" CdS films.

2) CdS/CdTe Heterojunction Photovoltaic Cells: The n-CdS/p-CdTe heterojunction photovoltaic cells were fabricated employing CdS films deposited at different substrate temperatures, as well as employing CdS films thermally annealed for 1 h after deposition. Ten devices were defined on each substrate with areas varying from 4.9 to 9 mm^2, as well as different shapes, including both square and round devices. The resultant device structures are shown in Fig. 1(b). All *I–V* characteristics were measured in the dark, and shunt resistance (at 0 ± 0.05 V) and ideality factor (at 0.4 ± 0.05 V) were extracted using (3), and are depicted in Fig. 8. The extracted shunt resistance was $> 1 \times 10^6 \Omega \cdot \text{cm}^2$ for devices in which the CdS was deposited at room temperature, as well as for all annealed CdS films. In contrast, the shunt resistance was found to be $< 1 \times 10^6 \Omega \cdot \text{cm}^2$ for all devices in which the CdS films were deposited at elevated temperature. Since shunt resistance is related to recombination mechanisms arising from defects close to the heterojunction interface, it is strongly correlated with the extracted value for the ideality factor, which indicated a high value for low values of shunt resistance. Although a slight rollover of the *I–V* curves at high applied voltage made it difficult to extract the series resistance, it is evident that the higher resistivity of the p-CdTe films results in higher values of series resistance, since it is much thicker and more resistive than the corresponding n-CdS layers.

All devices were characterized using conventional photovoltaic cell parameters extracted under AM 1.5 G illumination. As shown in Fig. 9, the efficiency of n-CdS/p-CdTe solar cells was found to decrease as the substrate temperature during deposition was increased, resulting also in a marginal decrease in fill factor, which is likely to be due to increasing CdS film resistance with increasing deposition temperature. In contrast,

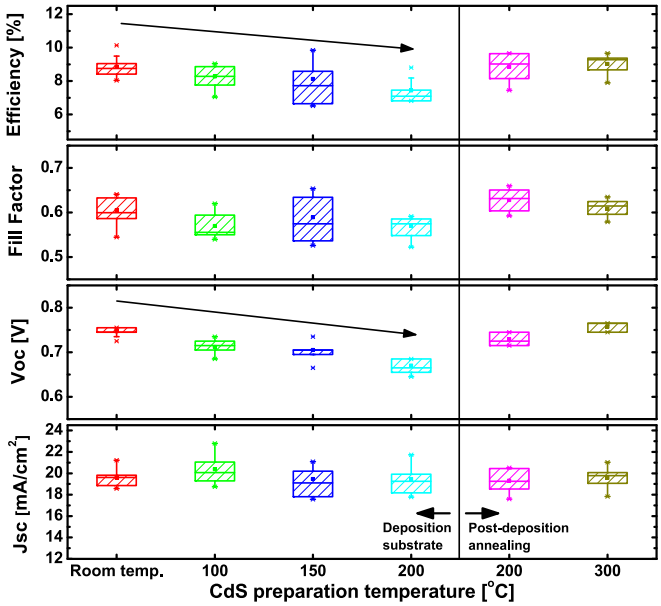

Fig. 9. n-CdS/p-CdTe solar cell parameters (efficiency, fill factor, open-circuit voltage, and short-circuit current) under AM 1.5 G illumination.

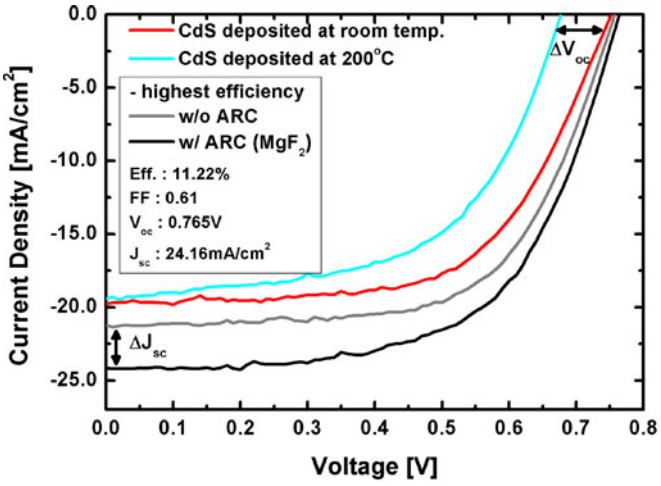

Fig. 10. *I–V* characteristics of fabricated solar cells measured under AM 1.5 G illumination, showing typical cells and those demonstrating the highest efficiency.

postdeposition thermal annealing lead to no significant change in solar cell efficiency or fill factor in comparison to CdS films deposited at room temperature without postdeposition thermal annealing prior to CdTe film deposition. It is important to note, however, that all CdS films were effectively annealed during the deposition of the CdTe film, which was undertaken at a substrate temperature of 330 °C for more than 1 h. It is noted that the postdeposition annealed thin film CdS/CdTe photovoltaic cells achieved an efficiency of $>11\%$, which compares very favorably with other thermally evaporated CdS/CdTe thin-film solar cell technologies [36].

The thermal annealing of the CdS films, which occurs during CdTe deposition, explains the observation that despite the low optical transmission of CdS films deposited at low substrate temperatures (see Fig. 5), the n-CdS/p-CdTe thin-film solar cells with CdS deposited at room temperature exhibited similar open-circuit voltage and short-circuit current levels, regardless of whether a preCdTe deposition thermal annealing step was performed, as evident from Fig. 9. The open-circuit voltage V_{oc} was found to be affected by both the CdS film deposition temperature and the postdeposition annealing temperature, confirming once again that the electrical properties of CdS thin films are influenced by thermal processes during both the deposition and postdeposition processes. Since optimization of the CdS/CdTe solar cells requires carrier concentration levels above 1×10^{17} cm^{-3} in the CdS films in addition to high optical transmittance through the CdS window layer [37], thermally evaporated CdS films deposited at room temperature can be considered to be suitable for photovoltaic cell applications if the subsequent CdTe deposition process involves a relatively high temperature for an extended period of time.

Fig. 10 compares *I–V* characteristics of n-CdS/p-CdTe solar cell devices fabricated using CdS films deposited at room temperature and at 200 °C to show V_{oc} improvement for CdS depostioned at room temperature. In addition, the measured *I–V* characteristics for the highest efficiency cell achieved using CdS films deposited at room temperature with MgF_2 antireflection coating for J_{sc} improvement are shown. The fabricated solar cells achieved an efficiency of $>11\%$, a short-circuit current of 24.16 mA/cm^2, and an open-circuit voltage of 0.765 V.

IV. Summary and Conclusion

In this study, we have presented detailed results of a study on the effects of substrate deposition temperature and postdeposition thermal annealing on the structural, electrical, and optical properties of thermally evaporated n-CdS thin films. It has been shown that increasing the substrate temperature during CdS deposition leads to a significant increase in the CdS film resistivity due to a reduction in carrier concentration and a degradation in the carrier mobility. It has been shown, however, that CdS films thermally deposited at higher substrate temperatures exhibit large grain size and higher optical transmission. It has been demonstrated that postdeposition thermal annealing of CdS films deposited at room temperature yields CdS films with significantly superior electrical and optical characteristics. In such films, it was found that although the grain size was not affected by postdeposition annealing temperature, the electron mobility increased significantly, thus indicating that thermal annealing effectively reduces the density of electron scattering defect centers. Similarly, the electrical characteristic of CdS/Si heterojunction diodes indicated that postdeposition thermal annealing decreased the diode ideality factor, thus suggesting a reduction in recombination at the CdS/Si interface and reduced parasitic series resistance. In CdS/CdTe heterojunction solar cells, photovoltaic cell parameters indicated that the deposition of CdS film at room temperature produces better performing cells with the substrate temperature required during thermal deposition of the CdTe acting to effectively anneal the underlying CdS film.

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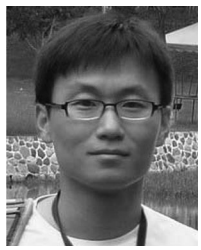

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