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THE NATURE OF THE TRAPPED HOLE ANNEALING PROCESS

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Abstract

Post-irradiation positive-bias annealing and negative-bias reverse-annealing of trapped positive charge in metal-oxide-semiconductor (MOS) oxides were studied as a function of temperature. Below 125°C, only a slight increase in the positive annealing response was observed, consistent with a tunneling process to a trap level below the Si valence band edge. A much larger increase in the trapped hole annealing rate was observed above this temperature. This change is discussed in terms of two possible mechanisms: (1) tunneling to an excited state above the Si conduction band and (2) thermal detrapping of holes to the oxide valence band. The annealing of positive oxide trapped charge appears to proceed at least partly by a compensation process where an electron tunnels to an electron trap associated with the trapped hole, restoring net electrical neutrality without removing the trapped hole. This compensating electron can tunnel back to the Si substrate if a negative bias is applied. This effect, which we call negative-bias reverse-annealing, is only slightly increased at elevated temperatures in hardened oxides, where it is significant even at room temperature. However, in a soft oxide which did not exhibit significant negative bias reverse annealing at room temperature, the effect was observed at elevated temperatures. We also discuss two unexpected results related to the interface trap density. First, the late-time saturation value of the radiation-induced interface trap density appears to increase with annealing temperature if positive bias is maintained. Second, the interface trap density appears to oscillate with alternating bias at elevated temperatures.

Introduction

In recent years there has been a growing recognition that MOS devices have a very complex time-dependent response to ionizing radiation. Hole trapping in the oxide near the Si substrate interface, along with its neutralization, is a fundamental component of this response. Previous studies at HDL have discussed the spatial distribution of hole traps [1] and the time and field dependence of the so-called negative bias reverse annealing [2], an effect previously observed elsewhere [3,4]. In this work we study these processes at different temperatures in an attempt to determine the energy level(s) of the traps as well as the activation energies for these processes. The oxide trapped charge annealing process appears to proceed at least partly by a compensation process. An electron tunnels to an electron trap associated with a trapped hole, restoring net electrical neutrality without removing the trapped hole (see Fig. 1). If a negative bias is applied, the compensating electron can tunnel back to the Si substrate, leaving a trapped hole again. This apparent compensation process has been observed independently now by five different groups [1-6].

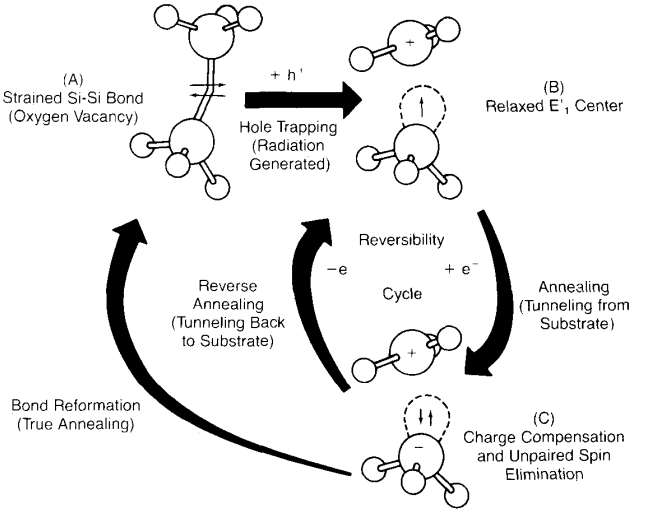

Fig. 1 A model of the hole trapping [(a) to (b)] and detrapping [(c) to (a)] processes are indicated, along with the intermediate compensation/reverse-annealing phenomenon [(b) to (c) and (c) to (b)].

In our earlier work, we used a trap level 3.1 eV above the SiO_2 valence band edge, following results by Manzini and Modelli [7]. Various other groups have agreed [8,9] or disagreed [3,5] with this trap level assignment. The groups who favored a level above the Si conduction band did so based on their annealing experiments at elevated temperatures [3,5], whereas our previous work was done primarily at room temperature. In an attempt to resolve these differences, we have also performed annealing measurements as a

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function of temperature, and have monitored the negative-bias reverse-annealing as well as the normal positive bias annealing. Using these new results along with results from the literature, we propose to explain the discrepancy in trap levels by suggesting a two-level trap model.

Background

Based on a large body of work by other researchers (see bibliography of reference 1), the following picture has emerged. Under positive gate bias, radiation-induced holes transport towards the Si/SiO_2 interface by polaron hopping [10,11]. A polaron is a localized lattice distortion carried along with the hole as it moves through the oxide. There is considerable lattice strain in the oxide near the interface [8], with numerous strained Si-Si bonds due to oxygen vacancies (see Fig. 1(a)). When the hole, with its associated lattice distortion, reaches a strained bond, it strains it further, often leading to bond breaking and a trapping event. As illustrated in Fig. 1(b), the hole is trapped on one of the Si atoms (thus leaving it positively charged), which then relaxes back into a planar configuration. The other Si remains neutral, with a dangling orbital containing one unpaired electron. These two trivalent Si atoms together constitute an E′ center, which was first identified by Feigl *et al.* [12] in unirradiated quartz, and was later associated with the MOS radiation-induced trapped hole by Lenahan and Dressendorfer [13]. Their electron spin resonance (ESR) studies have shown that the positive charge density during annealing correlates very well with the E′ signal, where the E′ signal is actually obtained by resonant flipping of the spin of the unpaired electron on the neutral Si. It is a crucial point that the process (presumably an electron tunneling into the oxide) which removes the unpaired spin also neutralizes the trapped hole, even though they are located on different atoms. Since this neutralization is partially reversible with a change of bias [1-5], electron compensation must be a part of the response along with the possible annihilation of the trapped hole and subsequent reformation of the Si-Si bond.

We believe the simplest model which accounts for these observations [2,14] is that the electron tunnels to the neutral Si where it joins the unpaired dangling electron, forming a spin pair (one spin up and one down), and leaving the Si negatively charged. Then, depending on the degree of relaxation of the lattice, the broken bond may or may not reform. If a negative bias is applied before the broken bond reforms, the extra electron can tunnel back to the Si substrate leaving a net positive charge in the oxide again (see Fig. 1(b) and 1(c)). A second possibility is that the compensating electron tunnels from the Si conduction band to the positively charged Si atom (an excited state), and then decays to the neutral Si atom (the ground state). This possibility will be discussed in detail later.

Experimental Procedure

As in our previous work [1,2], we studied an array of n-channel MOS field-effect transistors (MOSFETs) and p-type MOS capacitors produced from a variety of processes: process A produced a moderately hard oxide (19 percent trapping efficiency), process B produced a hardened oxide (8 percent), and process C produced a soft oxide (38 percent). Their gate oxides were grown to thicknesses of 97.0, 34.9, and 23.9 nm, respectively, with channel lengths ranging from 2- to 3-μm.

The MOSFETs were irradiated with a 10-keV x-ray bench-top tester at room temperature. Because of differences in the oxides, process A, B, and C samples were irradiated to different total doses (20 krad (SiO_2), 625 krad, and 125 krad, respectively). Each total dose was delivered in 2-1/2 min and produced a threshold voltage shift (ΔV_{TH}) between 0.5 and 1.0 V. These shifts were calculated from subthreshold current-voltage (I-V) curves measured with an HP 4145B semiconductor parameter analyzer. During irradiation and all subsequent stressing, the desired voltage was applied to the gate, and the other three terminals were grounded. The samples were all irradiated at room temperature with a +1.25 MV/cm electric field across the gate oxide. Following the irradiations, half of the samples were held under bias at room temperature, and the other half were stressed at elevated temperatures in a heating chamber which was evacuated for thermal stability. The I-V and charge-pumping measurements were made twice per decade of time, and were made at room temperature with a Keithley 619 electrometer. The chamber was cooled and reheated each time, with each half cycle lasting 30 to 40 min. The samples stressed at room temperature were measured with an HP 4145B. The oxide trapped charge component, ΔV_{OT}, was calculated with the assumption that the interface traps are all uncharged when the surface potential is at mid-gap [15]. Unirradiated controls were stressed as well and they exhibited shifts less than 10 percent of those observed in irradiated samples.

The MOS capacitors were irradiated in a temperature-controlled sample holder with a linear accelerator (LINAC) operated by the Armed Forces Radiobiology Research Institute (AFRRI), which delivered a 4-μs 13-MeV electron-beam pulse with a nominal dose of 100 krad (SiO_2). Switching to capacitors enabled us to do charge separation analysis on the data collected with a fast capacitance-voltage (C-V) system [16]. C-V data were taken (from 2×10^{-4} s following the pulse out to 10^3 s, with three measurements made per decade of time) by momentarily interrupting the gate bias, applying a 100-μs voltage ramp, and measuring the sample capacitance during the ramp with a 6-MHz probe signal. As with the x-ray exposures, the applied field was +1.25 MV/cm, except for the process A capacitors, for which it was limited to +1 MV/cm.

Both the pre- and post-irradiation measurements were taken at temperature. Once again, unirradiated controls were also stressed and did not show any significant shift.

Results and Discussion

Oxide Trapped Charge Response

Previous work by Oldham *et al.* [1] addressed the annealing of a particular oxide as a function of applied field. They noted that the slight differences in the annealing slope could be partly explained by the slight modification of the tunneling barrier height that their model predicted. In the present work, we study the annealing as a function of temperature, and again our results are consistent (up to 125°C) with that tunneling model.

In Fig. 2 we show results for MOS capacitors from process A that were exposed to an e-beam pulse while biased with an applied electric field of +1 MV/cm. The annealing of ΔV_{MG}, normalized to the same initial shift, $\Delta V_{MG}(0)$, is shown as a function of temperature. Almost no difference exists between the T=25°C and T=75°C curves (where the percentage of annealing/compensation for both is about 55 percent at 10^3 s). At T=125°C, slightly more annealing (or compensation) is observed (65 percent). However, at T=150°C, nearly all (95 percent) the initial charge has been neutralized. Fig. 3 shows the annealing results for capacitors from process B. Again, no significant temperature dependence is observed below 125°C. Similar annealing/compensation results were obtained for capacitors from process C. These results are summarized in Fig. 4, where we plot the fraction of unannealed charge remaining at 10^3 s following the radiation versus $1/T$. It is apparent that a different detrapping mechanism is present above 125°C for process A. Below this temperature the data fit well with the weak temperature dependence expected in a tunneling process from the Si substrate to traps in the oxide located below the top of the Si valence band. Above this temperature, a different mechanism becomes dominant. Two possibilities are discussed in the next section: (1) tunneling to an excited state above the Si conduction band and (2) thermal detrapping from the SiO_2 valence band. These results are confirmed by our MOSFET x-ray data (Figs. 5-7).

The other focus of our study is the negative-bias reverse-annealing effect, which illustrates that electron compensation is at least partly responsible for the apparent annealing of trapped holes. This effect was also studied as a function of temperature. Figs. 5 through 7 exhibit the results of MOSFETs from processes A through C, respectively, that were irradiated with a bench-top x-ray machine under positive applied field and allowed to anneal under positive field for 10^5 s at both room and elevated

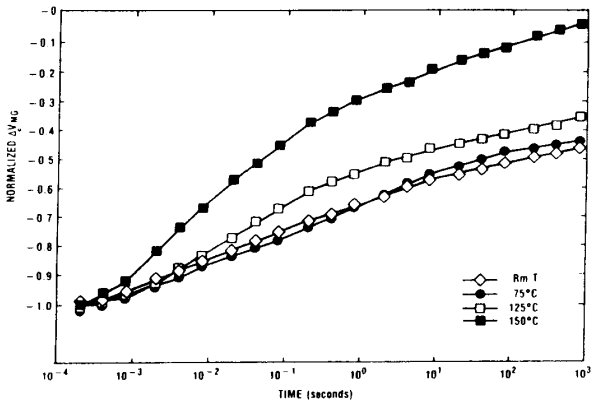

Fig. 2 Normalized positive-bias annealing of the oxide trapped charge as a function of temperature of a process A capacitor exposed to 100-krad (SiO_2) LINAC pulse.

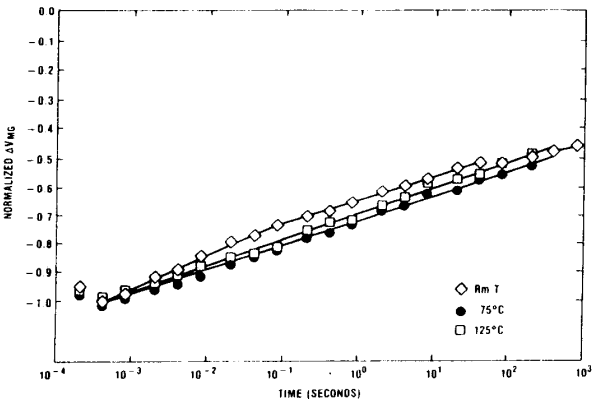

Fig. 3 Normalized positive-bias annealing of the oxide trapped charge as a function of temperature of a process B capacitor exposed to 100-krad (SiO_2) LINAC pulse.

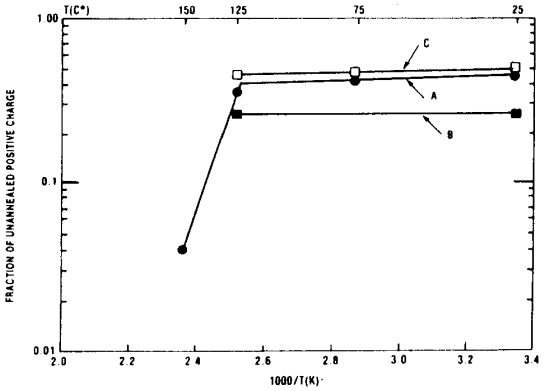

Fig. 4 The unannealed fraction of the oxide trapped charge after 10^3 s versus $1/T$. No temperature dependence is seen below 125°C. A second mechanism is apparent above 125°C.

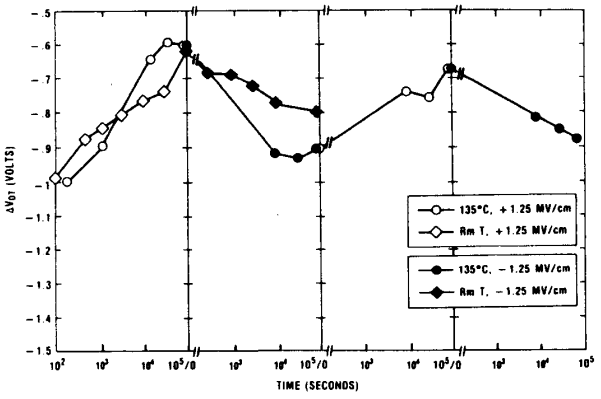

Fig. 5 Process A n-channel MOSFET exposure to 20 krad (SiO_2) from 10-keV x-rays. Alternate positive-and negative-bias annealing of the oxide trapped charge is shown as a function of temperature.

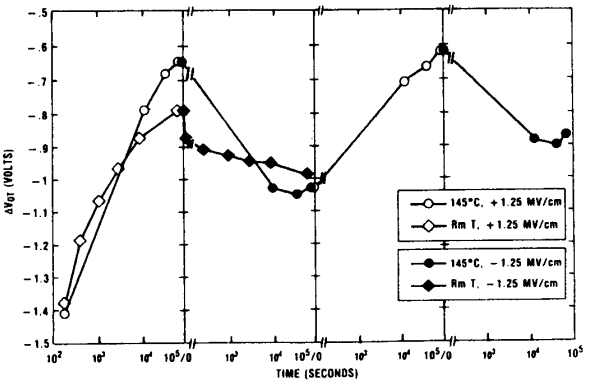

Fig. 6 Process B n-channel MOSFET exposure to 250 krad (SiO_2) from 10-keV x-rays. Alternate positive- and negative-bias annealing of the oxide trapped charge is shown as a function of temperature.

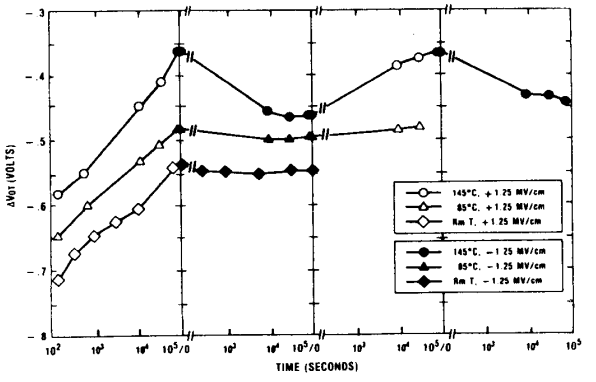

Fig. 7 Process C n-channel MOSFET exposure to 125 krad (SiO_2) from 10-keV x-rays. Alternate positive- and negative-bias annealing of the oxide trapped charge is shown as a function of temperature.

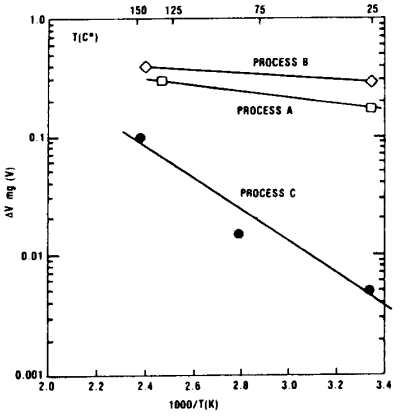

Fig. 8 The magnitude of the negative-bias reverse annealing in volts for 10^5 s is plotted versus $1/T$. The soft process C oxides have an activation energy of 0.27 eV.

temperature. In each case, after 10^5 s the applied field was switched negative and held for an additional 10^5 s. This field switching sequence was repeated several times, and the time interval from 10^2 to 10^5 s is shown for each cycle in Figs. 5 through 7. During the initial positive annealing sequence, there is a noticeable difference between the samples annealed at room temperature and those that were annealed at 135 or 145°C. This difference is less for the sample annealed at 135°C. This is consistent with the capacitor results shown in Fig. 4.

When the applied electric field was switched negative and held for an additional 10^5 s, we observed an increase in the magnitude of the elevated temperature negative-bias reverse-annealing response in comparison to the room temperature result. For MOSFETs from process A, ΔV_{OT} changed from 0.18 V at room temperature to 0.3 V at 135°C. The negative-bias reverse-annealing response for the hard process B MOSFETs increased by 33 percent, from 0.3 V at T=25°C to 0.4 V at T=145°C. For the soft process C MOSFETs on the other hand, even though the absolute increase in the negative bias reverse annealing was about the same as for the harder processes, the relative increase was by more than an order of magnitude, from about 5 mV at T=25°C to 100 mV at T=145°C. If we plot the magnitude of the reverse annealing on a log axis as a function of $1/T$ (see Fig. 8), we can obtain activation energies for all three process oxides. The soft process oxide is by far the most strongly activated by temperature. For process C

we calculate an activation energy of 0.27 eV, whereas the thermal activation energy is nearly zero for the other two processes. It must be remembered, however, that some positive annealing is occurring as well during the negative-bias reverse-annealing, and so the activation energy only provides information regarding the *net* tunneling process.

Previous results [2] at room temperature showed a difference in the negative-bias reverse-annealing response between hard and soft oxides. Whereas a sizable percentage of the neutralized charge reappeared in the hard oxides, no significant reversal was observed in the soft oxides. We explained this result by proposing that the two trivalent Si atoms of an E′ center move farther apart following hole capture in a hard oxide since hard oxides experience a greater bond strain gradient, a result suggested by Grunthaner *et al.* [8]. This in turn would decrease the likelihood of bond reformation.

This picture can easily be reconciled with the elevated temperature results which we have presented here. In the two harder oxides (processes A and B), the two trivalent Si atoms are pulled far enough apart by the stress in the oxide even at room temperature that many broken bonds do not reform when an electron is captured by tunneling. Raising the temperature does not cause a significant increase in the number of Si atoms which move far enough apart. On the other hand, the high temperature results in the soft oxide (process C) can be explained if the elevated temperature causes more pairs of trivalent Si atoms to move farther apart in this case, so that the broken bonds are less likely to reform when an electron tunnels in. Precisely this effect has been reported independently by Griscom [17] when annealing amorphous silica at 300°C. He observed changes in the ESR signature of the E′ center which he attributed to "a structural relaxation which causes the 'second silicon' to draw away even farther from the silicon of the unpaired spin." We note that Griscom did not perform his experiment as a function of temperature, so he did not determine the minimum temperature necessary to produce this effect. We believe that our elevated temperature negative-bias reverse-annealing results can be explained in a like manner.

Interface Trap Response

In the course of studying oxide trapped hole annealing/compensation, we have necessarily looked at the number of interface traps (N_{IT})--primarily because we have used the mid-gap neutrality assumption for calculating ΔV_{OT}, which requires that all or nearly all the interface traps are uncharged at this surface potential [15]. What we have observed is unexpected. N_{IT} oscillates with a change in bias at elevated temperatures, an effect not seen at room temperature. In addition, the magnitude of N_{IT} increases noticeably at late times when held under positive bias at elevated temperature following irradiation. (Two different groups [18,19] have previously reported that, although temperature does not change the final value of ΔN_{IT}, it does increase the rate of formation. A third group [20] has reported ΔN_{IT} to increase with temperature in a low dose rate experiment. However, this result appears to depend on the total dose.)

In Fig. 9 we show a hardened process B MOSFET which was irradiated with x-rays and annealed under positive bias at 145°C for 10^5 s. A considerable increase in ΔV_{IT} from its initial post-irradiation value is observed, along with the expected annealing/compensation of ΔV_{OT}, together inducing rebound in this device. When the bias is switched negative, three things occur. First, ΔV_{OT} reverse anneals as we have seen over and over again (and now routinely expect to see in a hard oxide--at any temperature). Second, ΔV_{IT} anneals to nearly its initial post-irradiation value at 10^2 s, and finally, ΔV_{TH} is observed going negative. ΔV_{IT} and ΔV_{OT} are in the same direction and they are of the same order of magnitude; each accounts for about half of ΔV_{TH}.

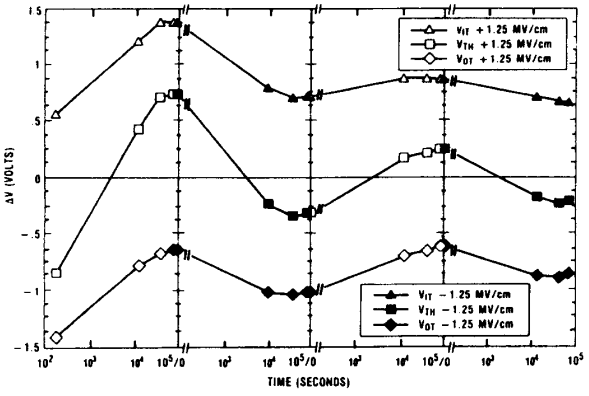

Fig. 9 A hard process B n-channel MOSFET was exposed to 250 krad (SiO_2) from 10-keV x-rays. Charge separation shows the effect of alternate positive- and negative-bias annealing at 145°C on both ΔV_{OT} and ΔV_{IT}.

In addition, we have used charge-pumping measurements to check the ΔN_{IT} values determined by sub-threshold I-V measurements. In Fig. 10 we show a process A MOSFET that was irradiated with x-rays and annealed under positive bias at 135°C out to 10^5 s, at which time the bias was switched negative for 10^5 s, etc. The interface trap density increases under positive bias and decreases under negative bias regardless of which method is used to make the measurement. The agreement is especially good with subsequent bias switches. Similar samples were irradiated and annealed except that positive bias was maintained for 2 x 10^5 s (positive bias control, also shown in Fig. 10). Here we see no annealing of ΔN_{IT}, but rather an

apparent saturation. Therefore we conclude that the apparent annealing of interface traps is bias dependent.

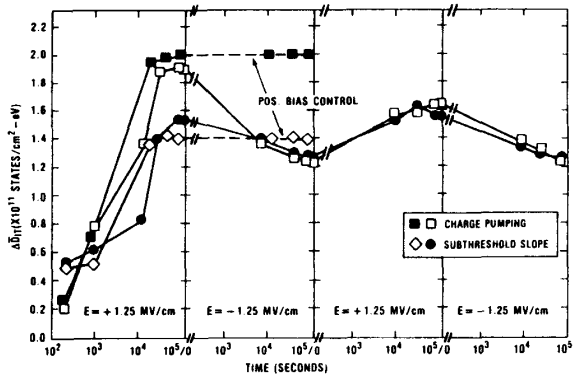

Fig. 10 The interface trap density of n-channel process A oxides at 145°C calculated using both subthreshold slope and charge pumping techniques. The oscillation observed is bias dependent.

In Fig. 11 we show the oscillation of ΔV_{IT} in process C MOSFETs as a function of temperature. At room temperature the final saturation value of ΔN_{IT} is observed at the end of the irradiation, and only a small increase is observed during annealing at 85°C. On the other hand, at 145°C, not only is there a large buildup under positive bias, but the increase is partly reversible under negative bias.

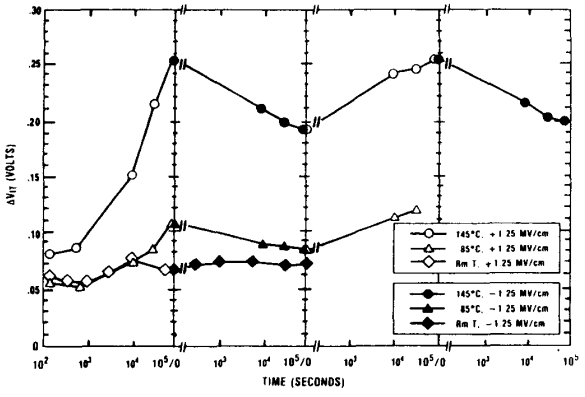

Fig. 11 Process C n-channel MOSFET exposure to 125 krad (SiO_2) from 10-keV x-rays. Alternate positive- and negative-bias annealing of the oxide trapped charge is shown as a function of temperature.

In summary, we see these N_{IT} results in samples from all three processes using both charge separation and charge-pumping methods, but only at elevated temperatures (greater than 125°C). In addition, we have seen similar results with capacitors exposed to e-beam pulses at elevated temperatures. We dismiss lateral non-uniformities (LNUs) as a culprit for two reasons: (1) charge-pumping measurements would not be affected by LNUs and (2) we have measured samples at liquid nitrogen temperature and have observed a virtual elimination of any sub-threshold stretch-out. Finally, we note that data by Dozier *et al.* [4] show a small reversal of ΔV_{IT} at 100°C. They dismissed this effect as insignificant since the reverse annealing of ΔV_{OT} dominated the ΔV_{TH} response, which was their focus of study. However, a small change is all that we would expect at 100°C, judging from our own data.

Discussion of the Energy Level of the Hole Traps

One of our main goals in studying oxide trapped charge annealing as a function of temperature was to determine the energy level(s) of the traps. In Fig. 12, we illustrate our current understanding of the trap levels. As we have already noted, several groups have reported trap levels below the Si valence band edge. Specifically, Grunthaner *et al.* [8] postulated a trap level 3.8 eV above the SiO2 valence band edge, assuming a 9.0-eV band gap. Harari and Royce [9] suggested a trap level 2.9 eV above the SiO_2 valence band. Manzini and Modelli [7] proposed a temperature-dependent trap level at 3.6 eV - αT, where $\alpha = 2$ meV/K, or a trap level of 3.1 eV at room temperature. We have used this result in our previous work [1,2]. In addition, Weber *et al.* [21] have recently reported that photons with energy in the range $5.5 < E < 6.4$ eV can excite electrons from a neutral state to the SiO_2 conduction band, leaving a positively charged center. This result suggests an energy level between 2.6 and 3.5 eV for the trapped hole. All these trap levels fall in the lower shaded band in Fig. 12. In addition, Schwank *et al.* [3] discussed their temperature dependent results in terms of a trap level 1.35 eV above the Si conduction band. Lakshmanna and Vengurlekar [5] also proposed a trap level 0.8 eV above the Si conduction band. These two results are indicated by the upper shaded band in Fig. 12.

The issue of the temperature dependence of the trapped charge annealing/compensation is central here. The probability of one particle tunneling through a barrier of a given height in a given time is, to a first order approximation (neglecting phonon assisted tunneling), independent of temperature. But the number of particles attempting to tunnel can be a strong function of temperature, and the barrier height can also depend on temperature. In particular, for a tunneling transition of an electron to the upper trapped hole level in Fig. 12, the density of electrons attempting to tunnel would be a strong function of temperature. Both groups reporting a trap level above the Si conduction band observed a strong temperature dependence in the annealing rate [3,5]. On the other

hand, at most a weak temperature dependence in the annealing rate would be expected for trap levels in the lower band in Fig. 12 because the electron density of states in the valence band is not a function of temperature. Other groups [7,22] have also reported such a weak temperature dependence in the annealing/compensation of trapped oxide charge.

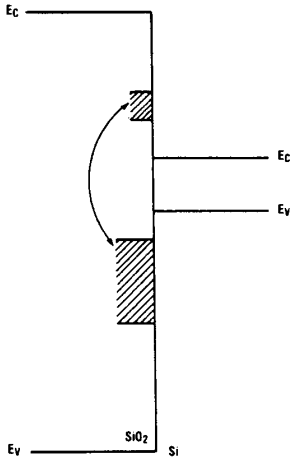

Fig. 12 The two spatially equivalent trap levels that electrons can tunnel to. These correspond to the ground state and an excited state of the E′ center complex.

Two other results in the literature suggest a way of unifying these apparently conflicting results. First, to explain some of his experimental results on the negative bias instability, Breed [23] proposed a model in which a neutral center in the oxide has a ground state below the Si valence band edge. An electron that is thermally excited to a higher energy level of the center, located above the Si conduction band edge, can then tunnel to the Si conduction band, leaving a positively charged center in the oxide. He determined the thermal activation energy for the transition to the excited state to be 1.3 ± 0.2 eV.

Second, Tohmon *et al.* [24] have recently reported optical measurements on oxygen-deficient glass. They propose a strained Si-Si bond (oxygen vacancy) as the ground state of the defect which is excited with 5 eV light. The singlet ground state is excited to a triplet state along with a lattice relaxation--an increase in the separation between the two Si atoms. Later, the excited triplet state decays back to the singlet ground state with the emission of a 2.7-eV photon. The 2.7-eV luminescence was detected by Tohmon *et al.* [24], even in unirradiated glasses, and by Hayes *et al.* [25] in heavily irradiated glasses.

The models proposed by Breed [23] and Tohmon *et al.* [24] are basically consistent with each other, if one equates a thermal activation energy of 1.3 eV with an optical excitation of 2.7 eV. An optical transition energy will always be greater than a thermal activation energy because an optical process is controlled by the peak in the density of states. On the other hand, thermal activation is controlled by the high energy tail of the density of states, which occurs at a higher energy than the peak, thus requiring less additional energy to make the transition.

These two works [23,24] suggest a model for reconciling the conflicting energy levels attributed to the trapped hole. The charged E′ center may have two energy levels to which an electron can tunnel: (1) the ground state (a singlet, because the two electrons are anti-parallel in the same orbital), which is also illustrated in Fig. 1(c) (where the electron tunnels to the neutral Si), and (2) an excited triplet state. The triplet state results from tunneling to the positively charged Si, allowing the two unpaired spins to be in a parallel alignment. This result is only temporary, since the electron in the excited state is unstable and decays to the ground state, probably in much less than 1 s. The ESR experiments by Lenahan [13] take much longer to complete, and therefore are sensitive only to the stable (final) ground state. For this reason, there is no real experimental inconsistency between a tunneling process to the excited triplet state (and subsequent decay to the singlet ground state) and our previous results.

Our previous experimental results at room temperature, and those we present here (up to 125°C), seem to be controlled primarily by tunneling directly from the Si valence band to the ground state of the E′ center (lower trap level in Fig. 12). The same conclusion is true in any other work where the tunnel annealing process is only weakly temperature dependent [7,22]. However, the other results we have discussed [23,24] indicate clearly that the excited level in Fig. 12 is a real state, which can also be reached by tunneling from the Si conduction band [3,5]. In this case the temperature dependence of the tunneling process is much stronger. The temperature at which tunneling to the excited state becomes an important effect will no doubt depend on oxide processing. It is likely that annealing studies in the literature which show a strong temperature dependence [3,5] were measuring significant tunneling to the excited triplet state of the E′ defect--the same defect involved in our measurements of tunneling to the ground state.

In general, one must also consider thermal detrapping, a process other than tunneling, when high temperature annealing experiments are performed. For example, Shanfield and Moriwaki [26-29] have performed thermally stimulated current (TSC) measurements where trapped holes were excited to the SiO_2 valence band and pushed by a negative field to the gate. The currents were measured as a function of temperature, and thermal activation energies ranging between 0.9 and 1.6 eV were calculated for the trapped holes. Shanfield performed TSC measurements

on a large number of oxides over the years, and many of them showed significant thermal detrapping in the temperature range of 125 to 150°C. In general, then, we would expect that if a high temperature annealing experiment shows accelerated annealing (compared to, say, room temperature), then both tunneling to the excited state in Fig. 12 and thermal detrapping could be contributing to the observed response. Then some care must be taken to resolve these two processes.

Conclusions

Only a weak temperature dependence is observed below 125°C for the annealing of the oxide trapped charge under positive bias following irradiation. This result, obtained in both hard and soft oxides, is consistent with the weak temperature dependence predicted by our tunneling model [1]. A strong temperature dependence was observed above 125°C, indicating a second detrapping mechanism. Two possibilities have been discussed: (1) thermal detrapping to the SiO_2 valence band and (2) electron tunneling to an unstable excited state opposite the Si conduction band. This second possibility suggests a way to reconcile the differences in the temperature dependence of trapped hole annealing in our work with that of others [3,5]. Whereas they explain their results with a hole trap that has an energy level opposite the conduction band of the Si substrate, we explain our results with an energy level that is below the Si valence band. We suggest, citing evidence from the literature, that these two energy levels are spatially equivalent, that they are the excited and ground states, respectively, of the same hole trapping complex (the E′ center).

The temperature dependence on the negative-bias reverse annealing of the oxide trapped charge was strongest for soft oxides. Even though both hard and soft oxides experienced similar absolute increases in the amount of reversibility, because soft oxides had exhibited no reverse annealing at room temperature, the increase for soft oxides was much larger in proportion. We explain this change by comparing the relative bond strains in soft and hard oxides. The greater the strain, the greater the chance the lattice will relax following hole capture (increasing the separation between the Si atoms of the E′ center). This effect in turn leads to a lesser chance of bond reformation following the capture of a tunneling electron in harder, more strained, oxides. We suggest, following the work of Griscom [17], that an increase in temperature will induce a greater separation to the point where bond reformation will be inhibited (to an extent) in soft oxides as well.

Two unexpected results relating to the interface trap density were observed at elevated temperature. First, the late-time saturation value of the radiation-induced interface trap density increased with annealing temperature when positive bias was maintained. Second, the interface trap density appeared to oscillate with alternating bias. These effects were seen in all three oxides studied using three different measuring techniques, and unirradiated controls showed no instability. These results suggest that proposals to use elevated temperature to accelerate annealing for rebound testing could overestimate the amount of rebound that would be observed at room temperature.

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