Optically enhanced trap assisted hysteretic I-V characteristics of nanocrystalline silicon based p-i-n heterostructure

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ABSTRACT

A p-i-n heterostructure containing electrochemically synthesized silicon (Si) nanorods embedded in a nonstoichiometric silicon oxide matrix sandwiched as i-layer between p-Si and n-type hydrogeneted amorphous Si shows hysteresis in both forward and reverse biases with an additional switching in forward bias. Conductivity in the trace path is lesser than the retrace path. Hysteresis in the reverse bias has been found to get enhanced up to three orders of magnitude under illumination by laser sources of different intensities and wavelengths showing the potential of the structure as an effective memory device. Hysteresis area and conductivity become maximum for red light and gradually decrease for green and violet light for fixed intensity. It is well known that the Si nanocrystal–silicon oxide interface contains a lot of electron and hole trap levels within the bandgap. Trapping and detrapping of photogenerated carriers at the trap/defect states are expected to affect the band bending at the junctions. The observed optically enhanced hysteresis has been explained through formation and destruction of the potential barrier at junctions during trace and retrace paths, respectively. The potential has been estimated by solving Poisson's equation, and the current–voltage (I–V) relation for trace and retrace paths has been derived where the rate of trapping and detrapping becomes different resulting in the observed hysteresis. Theoretically obtained I–V characteristics match well with the experimentally obtained results. The trap density in the i-layer estimated to be $\sim 10^{11}/\text{cm}^2$ is in good agreement for the trap density in similar systems.

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I. INTRODUCTION

Demand for different high performance memory devices makes the area of nonvolatile memory a very significant research topic in the current era dominated by electronic gadgets. Great attention is being paid to fabrication of high performance, low cost, and low power consuming resistive random access memory (RRAM) devices with reliable storage capacity. Plays a key role in such devices. The switching phenomenon is largely governed by the thickness And stoichiometry of the chemical composition of the resistive material, along with the presence of defect states, And to the chemical composition of the resistive material, along with the presence of defect states, And to the chemical composition of the resistive material, along with the presence of defect states, And to the chemical composition of the resistive material, And the chemical composition of the resistive material composition of the chemical composition of th

presence of interfacial or surface defects is usually considered to be damaging and detrimental for charge transport in optoelectronic applications. However, these so-called "defective" features may be utilized advantageously to obtain hysteretic charge transport, which in turn opens the scope for their application as memory devices. ^{13,18–20} Many groups along with ours have already reported that the interface traps play a crucial role in producing switching in silicon nanostructure based devices. ^{10,11,17,20–22} Particularly in nanostructures, where the surface to volume ratio becomes very high along with large density of interfacial traps, ^{11,23,24} hysteresis in I–V or C–V characteristics is an expected behavior and has

been observed in several nanostructure based heterojunctions. ^{13,25,26} Based on the hysteretic characteristics of the charge transport, a range of applications has also been demonstrated. ^{10,13,26–29} However, there are very few reports and consequently very little understanding of the hysteretic I–V property of nanostructured silicon based devices or heterostructures. ^{25,30}

Although not always explicitly stated, silicon nanocrystals almost always have a core-shell structure due to spontaneous, rapid surface oxidation of silicon nanostructures under ambient conditions. 11,31,32 The ubiquitous interfaces of such core-shell structures with nanocrystalline silicon at the core and the surrounding oxide shell act as charge trapping zones. 17,31,33-36 Consequently, nanostructured silicon covered with an oxide layer has the potential to be an active unit for fabrication of a memory device owing to the large concentration of oxide related hole and electron traps at the interface.³⁷ In this work, we have explored the effect of light irradiation on the hysteretic I-V characteristics of nanostructured silicon based p-i-n heterostructures. The heterostructured device under consideration consists of a layer of silicon nanorods embedded in a nonstoichiometric silicon oxide matrix^{22,31,38} sandwiched between p-Si and n-type amorphous Si (a-Si:H). In such a device structure, we have encountered current controlled switching under forward bias, which has been reported elsewhere. 17 Interestingly, we see that the same heterostructure exhibits hysteretic charge transport characteristics under reverse bias, and the hysteresis gets enhanced under visible illumination. A transport mechanism based on charge trapping and detrapping at the interfacial defect states satisfactorily explains the observed features. By explicitly solving Poisson's equation in the presence of trap states capable of capturing thermally and optically generated minority carriers, we have described the charge transport behavior of the device. Under this framework, we have obtained the hysteretic I-V characteristics of the device with illumination that match very well with the experimental ones. Moreover, the amount of the hysteresis being dependent on the intensity and color of the light irradiated on the device provides additional controls over the potential memory device that can be made with this structure.

II. EXPERIMENTAL

Standard anodic etching of a p-type (B-doped), electropolished (100) silicon wafer (resistivity $5-8\Omega$ cm) having previously established metallic contact on the back side through thermal evaporation of Aluminum (Al) in HF based ethanoic electrolyte [24% HF and Ethanol (Merck) in 1:1 volumetric ratio] was carried out that produces a porous, non-stoichiometric, silicon oxide layer containing silicon nano-rods. 32,39 The structure of the Si nanorods present in the porous Si layer was examined by high resolution Transmission Electron Microscopy (HRTEM, using JEOL JEM-3010). X-ray diffraction (Rigaku UltimaIV) has been performed to find the crystallite size of the nanocrystals present in the porous silicon layer. Photoluminescence (PL) [using Avantes (Avaspec-3648) spectrometer] and UV-VIS (Jasco: V-750) of the porous silicon have been performed to get an estimate about the optical bandgap of the layer. The chemical bonds present in the porous silicon layer were explored by Fourier transformed infrared spectroscopy (FTIR: Jasco FT/IR-4700).

On the electrochemically etched porous Si layer, an n-type hydrogenated a-Si layer has been deposited through plasma enhanced chemical vapor deposition (PECVD) technique. Raman spectroscopy (Lab RAM HR) has been performed on an a-Si:H layer deposited using same parameter in the same environment but on a glass substrate. Then, an ITO layer is sputtered on the a-Si:H layer (Milman India: MM196) with an optimized thickness of $\sim\!100$ nm to establish the metallic contact and to maintain the optical transparency. The area of the metallic contact is 3.14 mm². The structural hierarchy of the device was examined through Field Emission Scanning Electron Microscopy (FESEM) (Σ igma Zeiss) micrograph of the cross section of the device.

ITO and Aluminum (Al) layers were used to establish the top and bottom contacts, respectively. I-V measurements have been performed using an HP-source meter (Keysight U3606B) connecting in top-bottom configuration. To study the effect of illumination on transport through this hetero-structure, the measurements have been performed both in dark and under illumination. For illumination of different colors and intensities, three different lasers have been used. Violet and green light diode lasers (VDL-405 nm 500 mW ADJ and SDL-532-100 T, respectively) were employed. A He-Ne laser (Uniphase:1125P) is used as a source of monochromatic red light. Incident power and wavelength of the light used for this study have been measured by an Optical multimeter (ILX Lightwave: OMM-6810B). The I-V measurements have been performed on all the samples, but the hysteretic behavior was most prominent for the device containing a porous Si layer synthesized for 10 min at a current density of 10 mA/cm² on the bulk Si substrate. This particular porous Si layer is henceforth addressed as P10.

III. RESULTS AND DISCUSSIONS

Si nanorods are collected from the porous Si layer by the well-known exfoliation process reported elsewhere and are suspended in ethanol. Figure 1(a) shows the HRTEM micrograph of the colloidal Si nanorods exfoliated from the porous Si layer with inset showing the SAED pattern for the nanorods. The distinct circular rings with bright spots in the SAED pattern are associated with different crystalline planes of the Si nanorods. Random orientation of the nanorods is perceptible through the nearly continuous bright rings. The oxide shell surrounding the crystalline core is missing in the TEM micrograph due to amorphous nature of the oxide shell. This oxide shell gets merged with the background matrix of the TEM grid, and hence, the oxide shell of Si does not show any contrast variation in the TEM micrograph. 32

Figure 1(b) shows the XRD pattern of the Si nanorods present in the P10 layer for 2θ varying between 50° and 80° . In nanocrystalline material, the linewidth of the XRD pattern gets broadened due to the disruption of the long range crystallinity. This fact is prominent when the XRD pattern of P10 is compared with that of crystalline silicon as shown in Fig. 1(b). The average crystallite size measured from this peak broadening by using the Scherrer equation 40 is \sim 10 nm. It is well known that the Scherrer equation provides accurate size estimation for strain-free systems. The omnipresence of micro-strain in the porous Si layer makes it difficult to accurately estimate the actual crystallite size using Voigt analysis. Additionally, the presence of the crystalline substrate beneath the thin nanostructured porous layer affects the

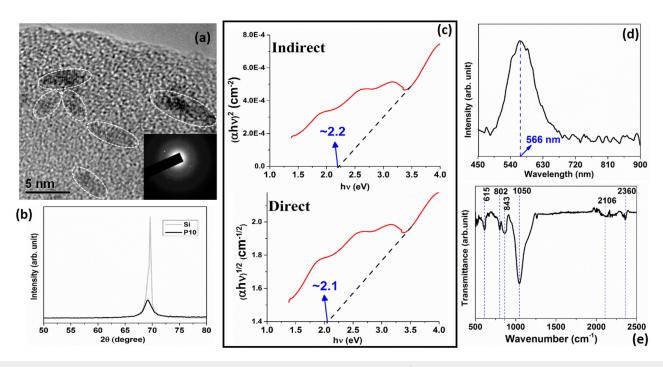


FIG. 1. Characterizations of a porous Si layer P10 etched for 10 min at a current density of 10 mA/cm²: (a) HRTEM micrograph of the Si nanorods (marked by dotted lines) with inset showing the SAED pattern with distinct circular rings and bright spots revealing different crystalline planes of randomly oriented Si nanorods; (b) XRD pattern of the porous Si layer showing peak broadening in comparison with crystalline silicon; (c) Tauc plot for the measurement of indirect ($(\alpha h v)^2 \text{ vs } h v$) and direct ($(\alpha h v)^2 \text{ vs } h v$) bandgap measurements estimating peaks at 2.2 and 2.1 eV, respectively; (d) PL spectrum showing a peak at 566 nm for the excitation of 405 nm; (e) FTIR spectrum in the transmission mode showing absorption peaks at ~615 cm⁻¹, and ~802 cm⁻¹ for Si-H_x deformation, ~843 cm⁻¹ for O-SiH_x; ~1050 cm⁻¹ convoluted with ~1155 cm⁻¹, indicating highly stressed SiO_x-Si bonds or defective silicon oxide; and ~2106 cm⁻¹ convoluted with 2087 cm⁻¹ and 2360 cm⁻¹ indicating Si-H bond vibrations.

final width of the diffracted peaks, which incorporate the convoluted effects of the nanostructured Si and the bulk Si substrate. Nevertheless, the Scherrer equation and Voigt analysis or any XRD based measurement provides an average order of magnitude estimation of the crystallite size, which although not accurate, and gives an idea of the size regime of the nanostructures present in the layer. 41,42,44,45

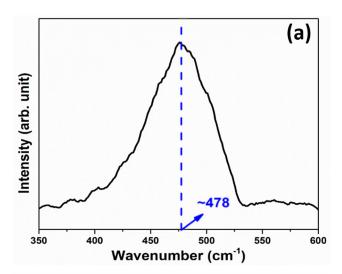
Figure 1(c) shows the well-known Tauc plot³⁶ related to the absorption^{36,46} under UV-visible excitation for the porous Si layer. Silicon is an indirect bandgap material in bulk form, but in nanocrystalline silicon, it behaves like a pseudo-direct bandgap material due to relaxation in the k-selection rule when the size becomes comparable with the electronic De Broglie wavelength. Moreover, the bandgap increases with decreasing size due to the quantum confinement effect. Due to the creation of trap states, the optical bandgap may also change for interfacial trap assisted transitions of charge carriers.³⁷ In this background, we have estimated the bandgap using two different Tauc plots applicable for direct and indirect materials. The values of the estimated bandgap obtained from $(\alpha h v)^2$ vs h v for indirect and $(\alpha h v)^{\frac{1}{2}}$ vs h v plots for direct are ~2.2 eV and ~2.1 eV, respectively. Figure 1(d) shows the PL spectrum of the P10 layer where the excitation wavelength of the laser source was 405 nm. The emission peak is obtained at ~566 nm. Although PL of Si nanocrystals is an active area of research from the discovery of luminescent

properties of porous Si in 1990, 47 the exact mechanism behind the light emission from these nanostructures is not convincingly understood until date. 17,48 From more than a few conflicting proposals, it is now believed that quantum confinement as well as oxide related surface/interface states are the main factors for luminescence from silicon nanocrystals, 37,49 but quantitative isolation of the specific contributions of quantum confinement and oxide interface states still remains an issue of concern. Consequently, an accurate estimation of the average electronic bandgap of the nanostructures or particle size directly from PL measurements is still not possible. Only a rough estimation of the optical bandgap of the porous Si layer has been obtained to be $\sim 2.2 \,\mathrm{eV}^{17}$ and is in good agreement with the results obtained from Tauc plots in Fig. 1(c). FTIR absorption spectra of the P10 layer are shown in Fig. 1(e). The lines at ~615 cm ~802 cm⁻¹, and ~843 cm⁻¹ indicate the presence of Si-H_x deformation and O-SiH_x bond in the porous layer. ⁵⁰ The sample is showing peaks near ~2106 cm⁻¹ convoluted with 2087 cm⁻¹ and 2360 cm⁻¹, which indicate the trace of different Si-H bonds.^{51,52} The peak at $\sim 1050 \,\mathrm{cm}^{-1}$ has been found to be convoluted with $\sim 1155 \,\mathrm{cm}^{-1}$. These two peaks indicate the presence of highly stressed SiO_x-Si bonds or defective silicon oxide in the porous Si layer. 5

Figure 2(a) is a Raman spectrum of the a-Si:H layer deposited through PECVD process on the porous layer containing Si nano-

rods. The excitation wavenumber was $\sim 514\,\mathrm{cm}^{-1}$ (using Argon Laser), and the main peak is obtained at $\sim 478\,\mathrm{cm}^{-1}$, which is the signature of the transverse optical mode in a-Si:H. $^{53-55}$ Another important feature is the absence of peak around $520\,\mathrm{cm}^{-1}$, which signifies the transverse optical mode for crystalline Si, 54 hence proves the absence of any crystalline phase in the a-Si:H layer. Figure 2(b) shows the cross-sectional FESEM image of one of the heterostructured devices named as PIN10. This device contains the P10 layer sandwiched between n-type a-Si:H layer and p-type bulk silicon as prominently visible in the FESEM image. The thickness of the P10 layer is $\sim 530\,\mathrm{nm}$. The porosity of this layer was obtained from the gravimetric method 52,56 and was found to be $\sim 70\%$.

Cyclic current-voltage (I-V) measurements have been performed in the dark environment as well as under illumination to study the transport of charge carriers through the device and to investigate the role of shining light on the charge transport as shown in Fig. 3. The characteristics obtained in dark as shown in



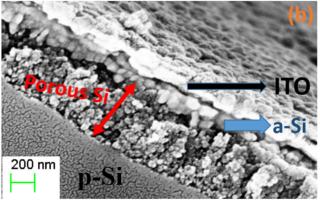


FIG. 2. (a) Raman spectrum of the top n-layer showing a broad peak at 478 cm⁻¹ revealing the presence of a-Si:H; (b) FESEM image of the cross section of the device depicting the porous layer sandwiched between the p-silicon substrate and the a-Si:H layer.

inset (a) of Fig. 3 represent the leaky rectifying nature of the device as the current obtained under dark in the forward bias is in the mA range, whereas that in the reverse bias is in the μ A scale. Resistive switching is obtained under forward bias in dark as shown in inset (b) of Fig. 3. Analysis of the switching characteristics observed in similar p-i-n heterostructures had already revealed the role of traps present in the porous Si layer. Therefore, in this paper, we are discussing about the hysteresis obtained in the reverse bias. From the sweeping direction, it is clear that the conductivity is less in case of the trace path (0 V to -6 V) in comparison to the retrace path (-6 V to 0 V). Both the conductivity and area of hysteresis in the reverse bias have been found to be enhanced under illumination. As in the forward bias the observed switching and conductivity do not show noticeable change under light, we have done the subsequent studies under the reverse bias only.

Three different light of different wavelengths but same incident power (1.1 mW) from three laser sources are used during I–V measurements as shown in Fig. 4(a). In dark, the area under the hysteresis loop in I–V characteristics is $\sim\!2.2\,\mu\text{W}$, whereas the loop area and the maximum current have been increased when the device is illuminated by three different sources of different wavelengths as given in Table I. Maximum current and hysteresis area have been increased gradually from violet to red light. This is due to the fact that the penetration depth through the material increases with increasing incident wavelength. With increasing depth of penetration of incident light, more and more electron–hole pairs are expected to be generated throughout the porous Si layer and in the bulk silicon substrate. As the effect of shining is maximum in the red laser, we have used the red laser for subsequent studies.

Using the red laser I–V measurements have been performed for different incident power as shown in Fig. 4(b). Corresponding hysteresis area and maximum reverse current are noted in Table II. It is clear that the area of the hysteresis loop increases with increasing incident power.

The salient features of the above study at a glance are as follows: (i) under reverse bias hysteresis is obtained in I–V characteristics in dark. The hysteresis and the conductivity get enhanced in the presence of light; (ii) the conductivity is more in the retrace path than that in the trace path, (iii) the area of hysteresis increases with increasing wavelength in the visible region and is maximum under red laser in comparison with green and violet lasers of same incident power and (iv) loop area increases for increasing incident power of the laser.

We have tried to explain the obtained hysteresis in I–V characteristics of the device on the basis of transport properties of a p-i-n diode. The role of i-layer is played by the porous Si layer that contains nanostructures having high surface to volume ratio. Consequently, there are numerous surface defects/traps present in this layer. These charge traps are expected to play a vital role in charge transport as reported elsewhere for several systems including similar structures. We have explained the charge transport through this device on the basis of charge trapping and detrapping in the porous Si layer. It is clear from the experimentally obtained graphs shown in inset (a) of Fig. 3 that under illumination there is no prominent photovoltaic effect as no open circuit voltage has been observed. Capturing of photogenerated carriers at the interface trap states present in the Si—SiO_x core—shell nanostructure

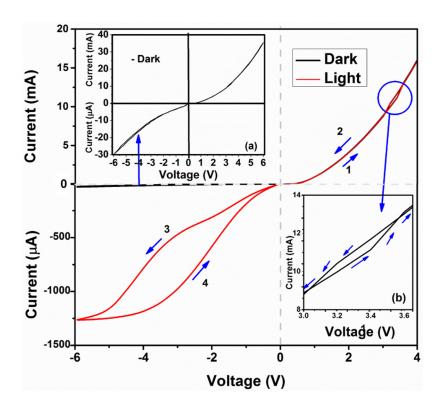
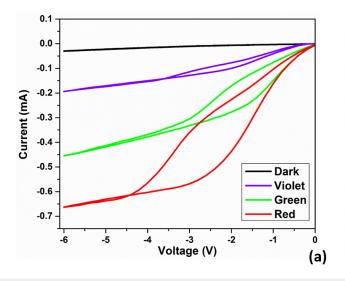


FIG. 3. I–V characteristics of the p-i-n device under dark and under illumination by a red laser (632 nm, 3.2 mW) showing large hysteresis in the reverse bias under illumination; with inset (a) I–V characteristics in dark only showing the maximum current obtained in forward bias in mA order whereas that in the reverse bias in μ A and (b) the magnified view of the switching in the forward bias.

inhibits the generation of free carriers that can produce a photovoltaic effect. ^{17,31} Under illumination, a fraction of the photogenerated carriers are expected to be trapped at the defect states. Application of reverse bias enhances the trapping rate that depends on the amount

of current flowing through the device and density of empty trap states. On the other hand, during withdrawal of the reverse bias, the detrapping rate is dependent on the current value as well as the density of filled states and hence different from trapping rate, in



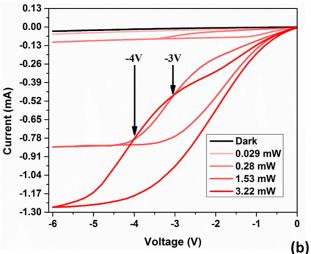


FIG. 4. (a) Hysteresis in I–V characteristics under dark and illumination of different laser sources with same incident optical power (1.1 mW) showing a gradual increase in the loop area and maximum photocurrent with increasing wavelength; (b) hysteresis in I–V characteristics for dark and different incident power of the red laser depicting increasing hysteresis, photocurrent, and saturation voltage with increasing optical power.

TABLE I. Maximum current obtained and hysteresis area for different wavelengths (1.1 mW).

Wavelength (nm)	Maximum reverse current (mA)	Hysteretic area (mW)
Dark	0.003	0.002
405	0.19	0.04
532	0.45	0.23
632	0.66	0.50

general. This difference between the trapping and detrapping rates for trace and retrace paths accounts for the hysteresis.

Due to diffusion of holes from p-Si and electrons from n-type a-Si:H, there are some uncompensated donor and acceptor ions in n and p materials, respectively, near the junctions. 46,58 Hence, the density of electron traps in the porous i-layer is likely to be higher near the p-Si/porous Si junction and that of the hole traps is higher near the porous Si/n-type a-Si:H junction. Under illumination, electron-hole pairs are generated everywhere including the n-type a-Si:H, p-type crystalline Si substrate, and the porous i-layer. Photocurrent is generated due to the crossing of excess minority carriers. Hence, a large number of minority electrons cross the p-Si/porous Si interface and get trapped near that interface. Similarly, holes get trapped primarily at the a-Si:H/porous Si interface during crossing that interface. This results in the fact that photogenerated electrons are more likely to be trapped near the interface of p-Si and porous Si layers, whereas holes are more likely to be trapped near the interface of porous Si and n-type a-Si:H. Therefore, under illumination, a potential barrier (V₀) is likely to be formed against the built-in potential [say φ_B^0 , as marked in Fig. 5(a)] due to capturing of the photogenerated carriers. This barrier opposes further crossing of minority carriers through the junction and nullifies the open circuit voltage that is otherwise expected to show up in a normal p-n junction solar cell.5 voltage (V)-current (i) relation for this device will be different from an ideal diode under illumination and can be expressed as

$$V = iR + \frac{\eta KT}{q} \ln \left(1 + \frac{i + i_{ph}}{i_0} \right) - \frac{\eta KT}{q} \ln \left(1 + \frac{i_{ph}}{i_0} \right). \tag{1}$$

The first term in Eq. (1) represents the drop across the effective series resistance of the porous Si layer. ⁶³ The second term corresponds

TABLE II. Maximum current obtained and hysteresis area for different incident power of the red laser.

Incident power (mW)	Maximum reverse current (mA)	Hysteretic area (mW)
Dark	0.03	0.002
0.03	0.05	0.009
0.28	0.11	0.100
1.53	0.84	0.663
3.22	1.27	1.330

to the drop across a normal p-n junction under illumination and the third term represents the potential barrier developed due to trapping of photogenerated carriers, which acts to decrease the band bending leading to no open circuit voltage under illumination. η , K, T, i_{ph} , and i_0 have their usual meaning and significance.

Figure 5(a) shows a schematic energy band diagram of the device indicating the empty charge traps present in the porous Si layer. Under illumination, due to trapping of the photogenerated carriers and consequent development of the potential barrier V_0 , the band bending $(\varphi_B^L = \varphi_B^0 - qV_0)$ will decrease as indicated in Fig. 5(b).

When the junction is under reverse bias, more electrons from the p-side and more holes from the n-side are being pushed into the porous silicon i-layer. This will, in general, lead to further trapping of injected minority carriers leading to an increase in barrier height opposing further drift of minority carriers at the interfaces. Another possibility is the detrapping of the trapped photogenerated carriers through collisions with the bias driven carriers. Actually, both in trace and in retrace paths, trapping and detrapping are expected to occur simultaneously as a dynamic process. But in the trace path, trapping will be dominant due to availability of more empty traps, whereas in the retrace path, detrapping will dominate as most of the traps are already filled due to trapping in the trace path. Because of the presence of the traps, the bending of the energy band will be less in comparison with the scenario when there is no trap present in the i-layer sandwiched between p-type and n-type layers as shown in Figs. 5(a) and 5(b). This will lead to lesser drift current than that is expected to flow in the absence of traps. The applied reverse bias in the direction of the built-in potential will increase the band bending $[\varphi_B^R = \varphi_B^0 + qV_R]$, as indicated in Fig. 5(c) where V_R is the applied reverse bias] leading to drift of more minority carriers and hence more reverse current. At the same time, the increase in the number of minority carriers trying to cross the junction results in trapping of more number of charge carriers. But again, this increase in the rate of trapping will lead to decrease in band bending $[\varphi_B^{RL}=\varphi_B^0+qV_R-qV_0]$ as indicated in Fig. 5(c)] resulting in lowering of the current through the device. This can be understood by noting the counter intuitive nature of current-voltage characteristics in the trace paths for illumination of 1.53 mW and 3.22 mW on the sample in the range of 3-4 V reverse bias marked in Fig. 4(b). It is expected in the normal case (without trapping) that high reverse current should flow for higher incident power at the same applied bias. However, in this case, initially, high current is flowing for higher illumination, but after a certain range of the applied voltage (approximately −3 V in this case), current flowing for lower illumination is more through the specified range of voltage (up to approximately -4 V). This apparently counter intuitive phenomena can be explained by considering trapping in the trace path. As the number of photogenerated carrier is higher for higher illumination, more of them are expected to be trapped leading to the increase of the barrier height and consequent lowering of the reverse current in that voltage range. Hence, a competition between the effect of the applied reverse bias trying to increase the reverse current and the trapping of charge carriers leading to the lowering of current is expected to be continued until most of the traps get filled. When all of the traps are filled, the reverse current reaches to a saturation value

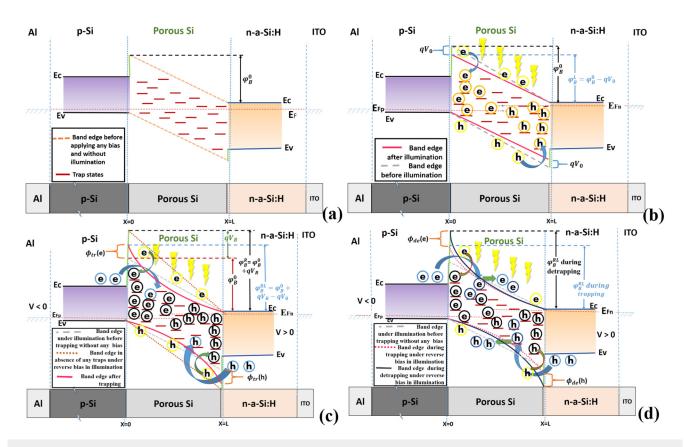


FIG. 5. Schematic energy band diagram of the heterostructure (a) under dark showing empty traps distributed throughout the porous Si layer and the built in potential φ_B^0 ; (b) under illumination showing trapping of photo-generated carriers leading to lowering in band bending ($\varphi_B^L = \varphi_B^0 - qV_0$) before applying any bias; (c) during trace path showing an increase in band bending (φ_B^R) due to applied reverse bias without illumination in the absence of traps along with a decrease in the bending (φ_B^R) under illumination due to trapping of photo-generated and injected carriers; and (d) during retrace path showing detrapping of captured carriers that leads to increase in the band bending.

equal to the maximum photocurrent achievable for a particular incident power.

Let the density of the vacant traps be n_t^0 under dark before application of any bias. The rate of trapping during trace is expected to be proportional to the rate of carrier flow (*i*) and density of vacant traps.⁶⁴

If n_t be the filled trap density, then

$$\frac{dn_t}{dt} \propto i(n_t^0 - n_t). \tag{2}$$

Corresponding expression for filled trap density at a particular current in the trace path can be expressed as

$$n_t = n_t^0 (1 - e^{-i/i_{tr}}),$$
 (3)

where $\frac{1}{l_{tr}}$ is a quantity related to the rate constant for trapping. Assuming the trapped charge density ρ is a linear function of distance(x)¹⁷ from the junction (p-Si/porous Si junction for holes and porous Si/a-Si:H junction for electrons), it can be written for the

porous Si layer of thickness L that

$$\rho(x) = \frac{\rho_{\text{max}} x}{I}.$$
 (4)

Solving Poisson's equation within the porous Si layer with suitable boundary condition that the development of barrier for holes is nearly zero at the p-Si/porous Si interface and maximum at the porous Si/a-Si:H interface, whereas the scenario is just opposite for electrons at those junctions, ¹⁷ we have the expression for the extra potential developed in the porous Si layer due to trapping of charge carriers as a function of reverse current as

$$\phi_t(x) = \frac{qn_t^0}{6\varepsilon}x^2(1 - e^{-i/i_{tr}}),\tag{5}$$

which leads to the value of the barrier potential at the interfaces

$$\phi_{tr} = \frac{qn_t^0}{6\epsilon} L^2 (1 - e^{-i/i_{tr}}). \tag{6}$$

This extra potential barrier will be formed at the porous Si/a-Si:H interface (x=L) for holes and at the p-Si/porous Si interface (x=0) for electrons as indicated in Fig. 5(c). Corresponding voltage drop is given as

$$V_{tr} = \frac{n_t^0}{6c} L^2 (1 - e^{-i/i_{tr}}) . (7)$$

This V_{tr} has to be subtracted from the right hand side of Eq. (1) as it is acting against the built-in field. Replacing $\frac{n_t^0}{6\varepsilon}L^2$ by V_t , the expression for voltage drop will be

$$V_{tr} = V_t (1 - e^{-i/i_{tr}}), (8)$$

where $V_t \left(= \frac{n_t^0}{6\varepsilon} L^2 \right)$ depends on the thickness, trap density, and effective dielectric constant of the porous Si layer. V_{tr} is the voltage developed due to trapping of the carriers at a given reverse current, and V_t is the maximum value of V_{tr} achievable at saturation reverse current.

When the reverse bias is reduced, in the retrace path, it is expected that the bias driven carriers will knock the trapped carriers out and these detrapped carriers will also take part in transport.¹⁷ This detrapping will lead to an increase in band bending due to lowering of the potential barrier already formed due to trapping in the trace path as indicated in Fig. 5(d) followed by drift of more minority charge carriers resulting in higher conductivity in the retrace path. Trapping depends on the density of available vacant traps, whereas detrapping depends on the density of filled traps. Hence, the current voltage relation for the trace and the retrace paths will be different from each other, in general, for the difference in trapping and detrapping rates. We have considered that before applying any bias some of the traps remain already filled by the photogenerated carriers. n_f^0 be the density of those filled traps. Considering that the rate of detrapping is proportional to the rate of carrier flow(i) and the density of occupied traps, 17 it can be expressed as

$$\frac{dn_t}{dt} \propto -i(n_f^0 + n_t). \tag{9}$$

The expression for filled trap density in the retrace path can be enumerated as

$$n_t = n_f^0 (e^{i/i_{rt}} - 1),$$
 (10)

where $\frac{1}{i_{rt}}$ is a quantity related to the rate constant for detrapping. In this case, also we get the expression for the potential developed at the interfaces during retrace as a function of reverse current as

$$\phi_{de} = \frac{q n_f^0}{2\varepsilon} L^2(e^{i/i_{rt}} - 1). \tag{11}$$

In the retrace path, minority carriers have to overcome the extra potential ϕ_{de} different from that in the trace path as indicated in Fig. 5(d). Corresponding voltage drop is given as

$$V_{de} = V_r(e^{i/i_{rl}} - 1), (12)$$

where $V_r = \frac{n_f^0}{2e}L^2$. It can be noted that V_r depends on initially filled trap density unlike V_t that depends on empty trap density along with the thickness and the effective dielectric constant of the porous Si layer. It can also be understood that the filled trap density is not fully independent of the total empty trap density. In the reverse bias, if the current reaches the saturation value i_m , i.e., all the traps are filled, then there should not be any difference between the voltage developed during the trace or the retrace path. This means $V_{tr} = V_{de}$ at $i = i_m$. Using Eqs. (8) and (12), we readily get

$$V_r = \frac{V_t(1 - e^{-i_m/i_{tr}})}{(e^{i_m/i_{rt}} - 1)}.$$
 (13)

Therefore, the current–voltage relation in Eq. (1) will be modified in trace and retrace paths through the incorporation of V_{tr} and V_{de} , respectively, and can be expressed as given in Eq. (14) below.

Hysteresis is obtained due to the difference in the rate of trapping and detrapping in trace and retrace paths, respectively. We have calculated the area (Δ) of hysteresis by integrating the difference of voltage in trace and retrace paths as mentioned in Eq. (14) in the range i=0 to $i=i_m$, where $\Delta=\oint V\ di=\int_{i_m}^0 V_{de}\ di-\int_{0}^{i_m} V_{tr}\ di$ leading to the expression for the area of hysteresis as shown in Eq. (15),

$$V = iR + \frac{\eta KT}{q} \ln\left(1 + \frac{i + i_{ph}}{i_0}\right) - \frac{\eta KT}{q} \ln\left(1 + \frac{i_{ph}}{i_0}\right) - V_t(1 - e^{-i/i_{tr}}) \qquad \text{for trace path}$$

$$iR + \frac{\eta KT}{q} \ln\left(1 + \frac{i + i_{ph}}{i_0}\right) - \frac{\eta KT}{q} \ln\left(1 + \frac{i_{ph}}{i_0}\right) - V_r(e^{i/i_{rt}} - 1) \qquad \text{for retrace path}$$
(14)

$$\Delta = V_t(i_m(\exp(i_m/i_{rt}) - \exp(-i_m/i_{tr}))/(1 - \exp(i_m/i_{rt})) + (i_{tr} + i_{rt})(1 - \exp(-i_m/i_{tr})). \tag{15}$$

Cyclic I–V measurements have been performed using the red laser (632 nm, 1.5 mW) for different voltage sweep ranges, and the obtained result is shown in Fig. 6(a). The maximum current i_m obtained for a particular sweep is noted from the experimental graphs for six different sweeping ranges. These experimentally obtained I–V

curves under illumination for different sweeping voltage ranges have been fitted to Eq. (14) for trace and retrace paths. Photocurrent i_{ph} has been estimated for this incident power (1.5 mW) as 0.88 mA and marked on Fig. 6(a). This is the maximum saturation current value under -6 V sweep. Reverse saturation current without illumination i_0

has also been estimated from the experimental data of I–V characteristics as shown in Fig. 3(a). The rate constants i_{tr} and i_{rt} for trapping and detrapping, respectively, along with the ideality factor η and V_t have been used as fitting parameters. The best fit I–V curves are shown in Fig. 6(b), and corresponding values for the fitting parameters are also summarized in Table III.

The same set of values for the fitting parameters $(V_t, i_{tr} \text{ and } i_{rt})$ has led to an excellent matching between the experimentally obtained hysteresis area and the theoretical Eq. (15) as shown in Fig. 6(c) that shows the hysteresis area increasing with increasing i_m with a super-linear trend within the range of experimental data as suggested in Eq. (15).

The above parameters listed in Table III have also been used to estimate the area of hysteresis for different wavelengths and

power of incident light and are compared with experimental data listed in Tables I and II, respectively. Here, also a reasonable agreement between the experimental and calculated results has been observed as evident in Fig. 6(d).

Here, the ideality factor η comes out to be ~32, which is used as a parameter for the best qualitative and quantitative matching of the calculated I–V characteristics and the hysteresis area with the experimentally obtained results. For an ideal diode, η should be between 1 and 2, but higher values of this parameter have also been reported by many other authors for different heterostructures. The many have value of ~10 to ~60 for porous Si based systems containing porous Si/ITO and porous Si/Au heterostructures. We have estimated the value of trap density $n_t^0 \sim 3.03 \times 10^{21}/m^3$ from the best fit value (3.7 V) of $V_t \left(= \frac{n_t^0}{6e} L^2 \right)$.

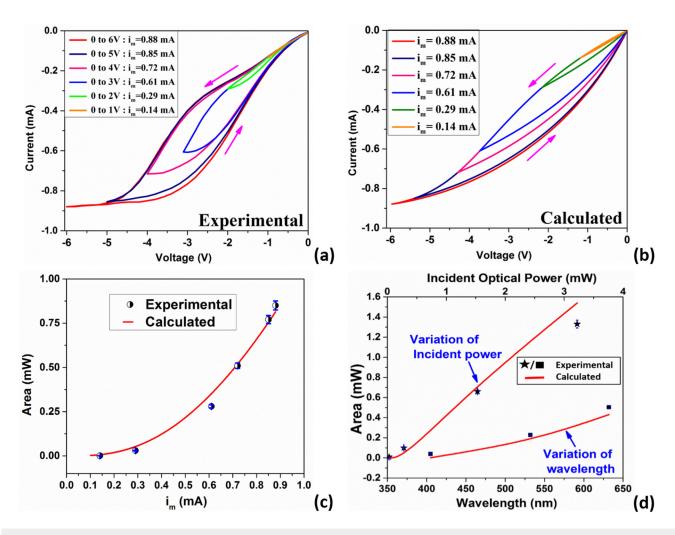


FIG. 6. (a) Experimentally obtained cyclic I–V characteristics under illumination by red laser (1.5 mW). (b) Theoretically obtained I–V characteristics for same incident power used in the experiment. (c) Area of hysteresis obtained experimentally (points) and calculated (solid line) for different i_m in different voltage sweep ranges depicting nice agreement between the theory and experiment. (d) Hysteresis area obtained experimentally (rectangular points and stars) and calculated (solid line) for different wavelengths and incident optical power representing a reasonable matching between the calculation and experiment.

TABLE III. List of best fit values of the fitting parameters.

$\overline{i_{tr}}$	i_{rt}	η	V_t
0.41 mA	0.58 mA	32	3.7 V

Here, we have used the value of $\varepsilon=1.63\times 10^{-11} F/m$ estimated using effective medium approximation for the porous Si layer of porosity ~70%. The thickness value of 530 nm has been used as L. Considering a linear distribution of trap density [Eq. (4)] and integrating this in the range of the thickness of the porous Si layer, the value of surface trap density at the junctions comes out to be ~1.6 $\times 10^{11}/cm^2$ that matches with the results we have obtained for a similar system as well as obtained by many other groups for the systems having similar interfaces reported elsewhere. 68

However, there is a small mismatch between I-V characteristics obtained experimentally and calculated theoretically as shown in Figs. 6(a) and 6(b), respectively, for low reverse bias region. In the theoretically calculated graphs, there is an over-estimation showing a bulge in the low reverse bias (below ~1 V reverse voltage), whereas this bulgy pattern becomes prominent above this voltage regime in the experimental graphs. We have approximated the charge transport in a simpler way that the transport in trace and retrace paths is dominated by only trapping and only detrapping of different rates, respectively, for any reverse bias. Another point to remember is that the trap density has been approximated with a linear distribution in the porous Si layer. Owing to these two approximations, the mismatch may have been arisen in the calculated plots. Exact qualitative and quantitative matching requires detail information about the distribution of traps in the active layer as well as more microscopic details about the transport of individual charge carriers.

IV. CONCLUSION

In conclusion, a p-i-n device consisting of electrochemically synthesized Si nano-rods in nonstoichiometric silicon oxide matrix sandwiched between n-type a-Si:H layer and p-Si substrate has been fabricated. ITO layer has been deposited on the top a-Si:H layer for optically transparent metallic contact. I-V characteristics of the devices show rectifying property along with a current controlled switching in the forward bias. A prominent hysteresis is obtained in the reverse bias, which is enhanced in the presence of light with suitable wavelength and intensity. This optically enhanced hysteresis has been explained in terms of raising and lowering of barrier leading to modification in band bending due to trapping and detrapping of injected carriers in trace and retrace sweeps, respectively. Theoretically simulated I-V plot qualitatively matches with the experimentally obtained graph for a suitable choice of a set of fitting parameters that have been used to estimate the trap density in the active layer leading to a plausible value of ~10¹¹/cm², which is in good agreement with previously reported results in similar systems. 17,68 The enhancement of hysteresis under illumination shows the potential of this p-i-n heterostructure as an optically controlled memory unit.

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