Improving the Accuracy of Capacitance-to-Frequency Converter by Accumulating Residual Charges

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***Abstract*—Recently, capacitive sensors, which consist of a sense capacitor and a reference capacitor, have been considered for a sensor array for monitoring biomolecular reactions. Although a capacitance-to-frequency converter (CFC) may be a simple and effective solution for reading a capacitive difference between the sensor capacitors, prior versions lack sufficient accuracy. In this paper, we present a more accurate CFC, which produces a single pulse stream in a wide range of frequencies. This circuit saves residual charges and accumulates them when discharging an integrator capacitor. Implemented in 0.35-μm CMOS technology, our circuit improves the accuracy from about 6% to 0.13%.**

***Index Terms*—Capacitance-to-frequency converter (CFC), capacitive sensor, integrator, residual charge.**

I. Introduction

PRODUCING and measuring a capacitive difference is a fundamental method of sensing, which has many applications such as pressure and humidity measurements, and hazardous gas detection. The same technique can also be used in a microelectromechanical system (MEMS) to monitor various concurrent biomolecular reactions, which change the stress on the surface of a mechanical element and, thus, the capacitance of a sense capacitor [1], [2]. By monolithically integrating readout circuits into the MEMS and having them handle a group of capacitive sensors, a high-density and low-noise monitoring system is attainable. In this system, an array of capacitive sensors is divided into multiple groups, so that the sensors in a group may share a common reference capacitor. Furthermore, the sensor array elements in a group can be accessed by a single readout circuit, and the area cost of the system can be reduced. In this case, the corresponding output rate is approximately divided by the number of array elements due to time multiplexing and additional switches.

Several circuits to read out the capacitive difference have already been published, which consist of a capacitance-to-voltage converter (CVC) and an analog-to-digital converter (ADC) [3]–[6]. However, this form of circuit is too large and complicated to be integrated in such a high-density sensor system previously described. An alternative candidate is the capacitance-to-frequency converter (CFC) proposed by Chiang *et al.*, which produces a single pulse stream and thus enables simple communication with the outside [7]. Although it produces a pulse stream without requiring the complexity of an ADC, the hardware cost can be further reduced by merging a CVC and a voltage-to-frequency converter into a direct CFC that only requires a single op-amp in its core, as proposed by Lee *et al.* [8]. However, the CFC due to Lee *et al.* suffers from nonlinearity that causes poor accuracy at higher frequencies. Chiang *et al.* addressed this nonlinearity by adding an automatic compensation circuit that observes an integrator output and controls a counter operating at a frequency that is four times higher than the operating clock frequency. Their compensation circuit was able to achieve an accuracy of about 5% at the cost of a circuit area comparable to the CFC. In this paper, we present a compact direct CFC in which accuracy is enhanced by utilizing the residual charges at the end of each output cycle, instead of allowing them to drain away. Additionally, the dynamic frequency range of our CFC has been widened to match the operating clock frequency. This circuit can measure both large and small differences in capacitance and, hence, in the quantity being sensed, with higher accuracy than previous circuits of this type.

II. Proposed CFC

A. Circuit Operation

Fig. 1 shows a schematic diagram of the proposed CFC, which converts the difference in capacitance between a sense capacitor $C_{\rm S}$ and a reference capacitor $C_{\rm R}$ into the output frequency $f_{\rm OUT}$ of an output pulse stream. The op-amp OP and switched capacitors in Fig. 1(a) constitute an integrator that produces a staircase signal at $V_{\rm int}$ during low MAG. The height of each step in this signal is proportional to the capacitive difference and is negative if $C_{\rm S}$ is smaller than $C_{\rm R}$. When the staircase signal reaches a predetermined level $V_{\rm refp}$ or $V_{\rm refn}$, one of comparators COMP1 or COMP2 produces a high level, and the MAG signal goes high and passes a delayed version of $\Phi 3$ to the output. Therefore, the output frequency $f_{\rm OUT}$ of the high-level pulse stream is also proportional to the difference between $C_{\rm S}$ and $C_{\rm R}$, and can be as high as the frequency of the operating

Manuscript received June 22, 2010; revised March 12, 2011; accepted March 21, 2011. Date of publication May 27, 2011; date of current version November 9, 2011. This research was supported in part by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (2011-0002126), and in part by the IT R&D program of the Ministry of Knowledge Economy/Korea Evaluation Institute of Industrial Technology (10030573, Development of Photonic CMOS-based Intelligent Silicon Bead). The Associate Editor coordinating the review process for this paper was Dr. Gerd Vandersteen.

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Digital Object Identifier 10.1109/TIM.2011.2147650

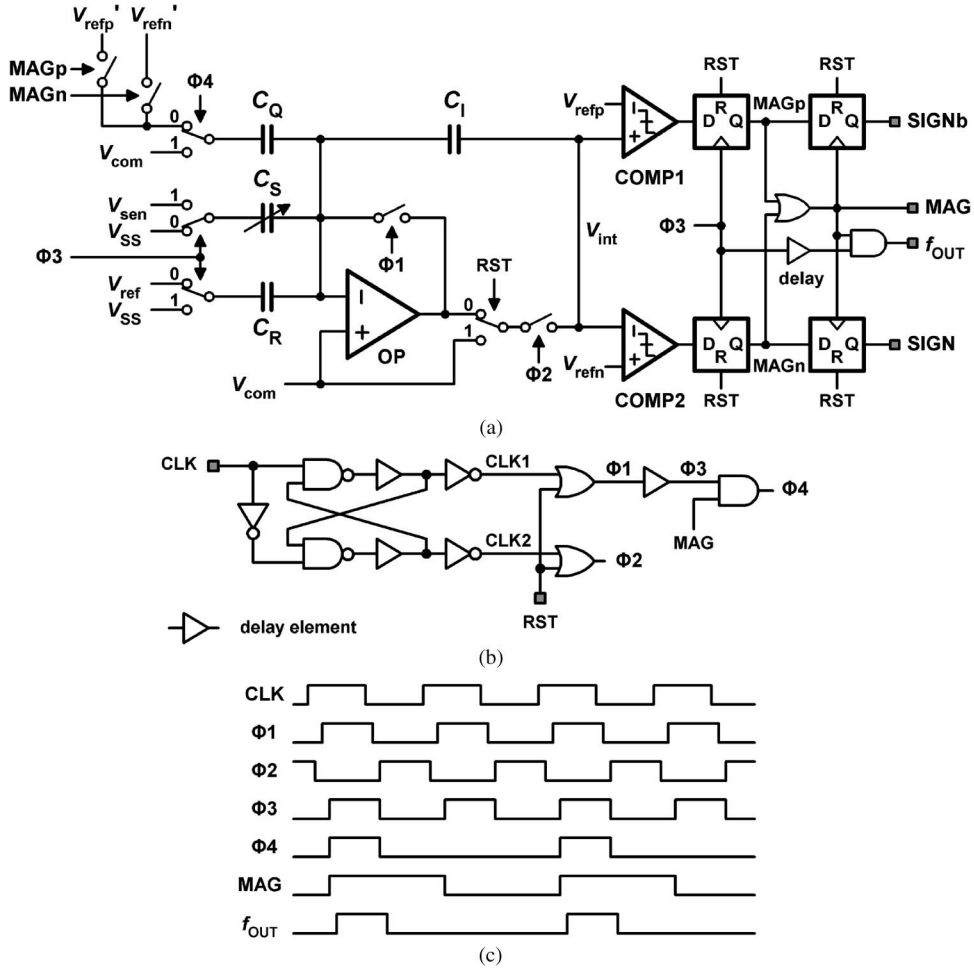


Fig. 1. Schematic diagram of (a) the proposed CFC and (b) its switch signal generator. (c) Timing diagram of the CFC.

clock CLK. If $C_{\rm S}$ is larger than $C_{\rm R}$, then the staircase signal approaches $V_{\rm refp}$ with a positive step, and COMP1 determines the value of MAG; however, COMP2 determines it if $C_{\rm S}$ is smaller than $C_{\rm R}$. The direction of the difference between $C_{\rm S}$ and $C_{\rm R}$ is reported by SIGN or SIGNb. Waveforms from the simulated operation of the CFC are shown in Fig. 2.

In the earlier CFCs, integrator capacitor $C_{\rm I}$ is fully discharged when MAG becomes high; then, it is charged during the subsequent integrating operations until MAG becomes high again [7], [8]. This is how the output frequency $f_{\rm OUT}$ is made to reflect the difference between $C_{\rm S}$ and $C_{\rm R}$. However, some of the charge integrated into $C_{\rm I}$, which is called the residual charge, is also discharged. Its magnitude is proportional to the voltage by which $V_{\rm int}$ exceeds a predetermined level and thus reflects the difference between $C_{\rm S}$ and $C_{\rm R}$. If we save these residual charges in successive discharging steps, they are also integrated over multiple charging-and-discharging cycles. If these residual charges have significant magnitude, then accounting for them clearly improves the accuracy of the CFC. Our CFC, as shown in Fig. 1, utilizes a constant-quantity capacitor $C_{\rm Q}$ to discharge $C_{\rm I}$ by a constant amount and saves the residual charge.

Four signals $\Phi1-\Phi4$ are internally generated from a single clock CLK and used for controlling charge transfer through the switches. Signals $\Phi1$ and $\Phi2$ are nonoverlapping clocks, and

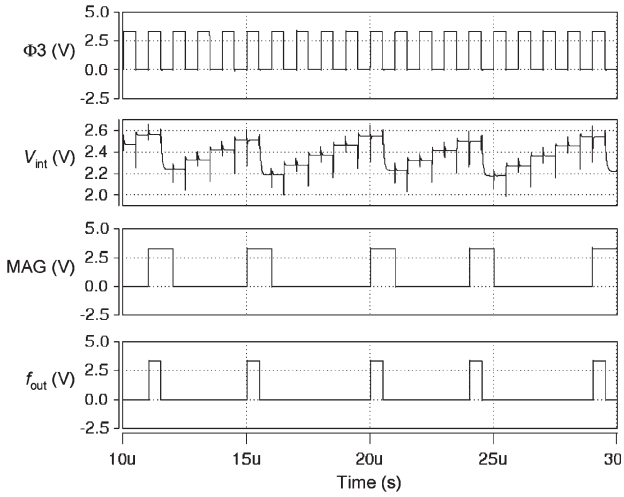


Fig. 2. Simulated waveforms from the proposed CFC. After $\Phi3$ changes, there are spikes on $V_{\rm int}$ and on the negative-input voltage of OP. They reflect the feedback operation of OP, which makes its two input voltages meet. The outputs of COMP1 and COMP2 are sampled by rising $\Phi3$ before the spikes occur and change those outputs.

$\Phi3$ is a delayed version of $\Phi1$. According to these signals, the integrator operates in two steps as follows:

1) Charge set: When $\Phi3$ is high, the output of OP is directly connected to the negative input of OP by high $\Phi1$.

Therefore, OP supplies charge when $C_{\rm S}$ and $C_{\rm R}$ are charged to $V_{\rm sen}-(V_{\rm com}+V_{\rm OS})$ and $V_{\rm SS}-(V_{\rm com}+V_{\rm OS})$, respectively. $V_{\rm OS}$ is the input offset voltage of OP.

2) Charge transfer: Since $\Phi 1$ goes low before $\Phi 3$, the negative input of OP is floated before the capacitors are switched. This ensures charge conservation at that input when $C_{\rm S}$ and $C_{\rm R}$ are charged to $V_{\rm SS}-(V_{\rm com}+V_{\rm OS})$ and $V_{\rm ref}-(V_{\rm com}+V_{\rm OS})$, respectively, by low $\Phi 3$. At this time, the output of OP is connected to the negative input through $C_{\rm I}$ by high $\Phi 2$, and extra charges at $C_{\rm S}$ and $C_{\rm R}$ are transferred to $C_{\rm I}$. Since capacitors $C_{\rm S}$ and $C_{\rm R}$ are switched in the opposite direction, the charges transferred to $C_{\rm I}$ are proportional to the difference in capacitance.

When MAG is high, $C_{\rm Q}$ is also involved in the two-step operation. If MAGp is high, the law of charge conservation gives

$$\begin{aligned}&C_{\rm S}\left[V_{\rm sen}-(V_{\rm com}+V_{\rm OS})\right]+C_{\rm R}\left[V_{\rm SS}-(V_{\rm com}+V_{\rm OS})\right]\\&\quad+C_{\rm I}\left[V_{\rm int1}-(V_{\rm com}+V_{\rm OS})\right]+C_{\rm Q}\left[V_{\rm com}-(V_{\rm com}+V_{\rm OS})\right]\\&=C_{\rm S}\left[V_{\rm SS}-(V_{\rm com}+V_{\rm OS})\right]+C_{\rm R}\left[V_{\rm ref}-(V_{\rm com}+V_{\rm OS})\right]\\&\quad+C_{\rm I}\left[V_{\rm int2}-(V_{\rm com}+V_{\rm OS})\right]+C_{\rm Q}\left[V'_{\rm refp}-(V_{\rm com}+V_{\rm OS})\right]\end{aligned}\tag{1}$$

where $V_{\rm int1}$ and $V_{\rm int2}$ are the $V_{\rm int}$ before and after charge transfer, respectively. Thus, we obtain

$$V_{\rm int2}-V_{\rm int1}=\frac{C_{\rm S}}{C_{\rm I}}V_{\rm S}-\frac{C_{\rm R}}{C_{\rm I}}V_{\rm R}-\frac{C_{\rm Q}}{C_{\rm I}}V'_{\rm Q}\tag{2}$$

where $V_{\rm S}=V_{\rm sen}-V_{\rm SS}$, $V_{\rm R}=V_{\rm ref}-V_{\rm SS}$, and $V'_{\rm Q}=V'_{\rm refp}-V_{\rm com}$. By setting $V_{\rm S}$ and $V_{\rm R}$ to the same value, we can process the capacitive difference with the CFC. When MAG is low, $C_{\rm Q}$ stays connected to the supply voltage and the ground through parasitic capacitors of metal–oxide–semiconductor (MOS) switches without being involved in the two-step operation, and $V'_{\rm Q}$ in (2) reduces to zero. Equation (2) shows that the operation of the integrator is not affected by $V_{\rm OS}$. The switches are implemented as a CMOS switch, which has an n-channel MOS and a p-channel MOS of the same size and does not cause severe charge injection [9]–[11].

B. Mathematical Analysis

For simplicity, we only consider the situation in which $C_{\rm S}$ is larger than $C_{\rm R}$. However, a similar treatment applies when $C_{\rm S}$ is smaller than $C_{\rm R}$.

Fig. 3 shows two input signals of a comparator COMP1, which are a staircase signal at $V_{\rm int}$ and a constant voltage of $V_{\rm refp}$. If we were to use the same discharging method as previous circuits [7], [8], the staircase signal would exhibit the following relationship, as shown in Fig. 3(a):

$$q=nx-r\tag{3}$$

where $q=V_{\rm Q}=V_{\rm refp}-V_{\rm com}$, $x=(C_{\rm S}V_{\rm S}-C_{\rm R}V_{\rm R})/C_{\rm I}$, and $0\le r<x$. Therefore, the actual value to be measured is

$$\frac{x}{q}=\frac{C_{\rm S}V_{\rm S}-C_{\rm R}V_{\rm R}}{C_{\rm I}V_{\rm Q}}=\frac{1+\frac{r}{q}}{n}.\tag{4}$$

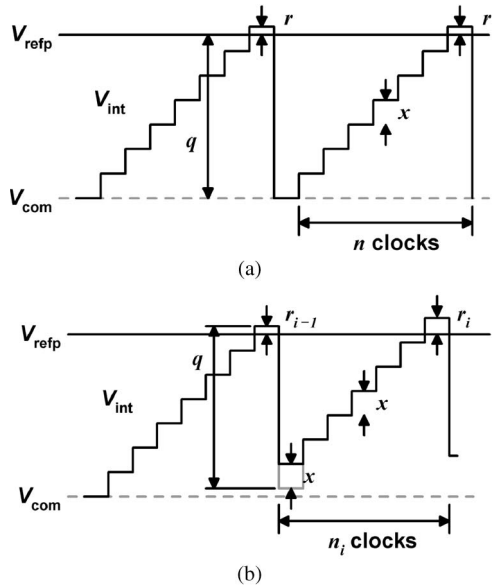


Fig. 3. Integrator operation and error calculation. (a) Previous method. (b) Proposed method.

When an error of r/q is allowed, the value measured by the CFC is

$$\frac{\hat{x}}{q}=\frac{1}{n}=\frac{1}{1+\frac{r}{q}}\cdot\frac{x}{q}\tag{5}$$

for the output frequency

$$f=\frac{1}{n}f_{\rm op}.\tag{6}$$

Because n is a positive integer, the measured value $\hat{x}$ is less than or equal to q, and the accuracy is limited if n is near 1.

However, when our method is applied, the following equation is obtained from the staircase signal shown in Fig. 3(b):

$$q-r_{i-1}=n_ix-r_i\tag{7}$$

where $q=C_{\rm Q}V'_{\rm Q}/C_{\rm I}$, $x=(C_{\rm S}V_{\rm S}-C_{\rm R}V_{\rm R})/C_{\rm I}$, and $0\le r_i<x$ for a nonnegative integer i. After m iterations, we obtain

$$\frac{x}{q}=\frac{C_{\rm S}V_{\rm S}-C_{\rm R}V_{\rm R}}{C_{\rm Q}V'_{\rm Q}}=\frac{1+\frac{r_m-r_0}{mq}}{n_{\rm eq}}\tag{8}$$

where

$$n_{\rm eq}=\frac{n_1+n_2+\cdots+n_m}{m}\tag{9}$$

and $n_{\rm eq}$ is equivalent to n of (4).

The value measured by the CFC is now

$$\frac{\hat{x}_{\rm eq}}{q}=\frac{1}{n_{\rm eq}}=\frac{1}{1+\frac{r_m-r_0}{mq}}\cdot\frac{x}{q}.\tag{10}$$

The error is $(r_m-r_0)/mq$, for the output frequency

$$f_{\rm eq}=\frac{1}{n_{\rm eq}}f_{\rm op}\tag{11}$$

where $0\le f_{\rm eq}<f_{\rm op}$. This output frequency $f_{\rm eq}$ is a harmonic mean of the frequencies, each of which corresponds to n_i of

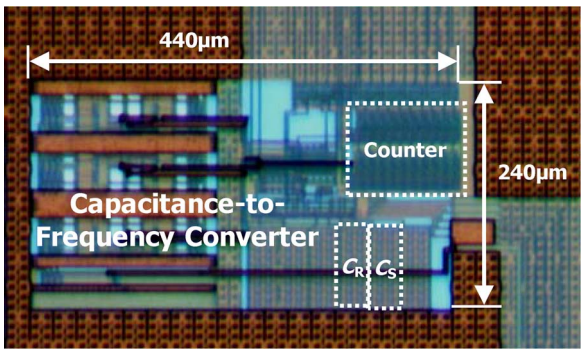


Fig. 4. Microphotograph of the proposed CFC equipped with a 10-bit counter.

(7). From (5) and (10), we can express the extent to which our method enhances accuracy with the following factor:

$$\eta = \frac{\hat{x} - x}{\hat{x}_{\text{eq}} - x} = \frac{\frac{mr}{r_m - r_0} + \frac{r}{q}}{1 + \frac{r}{q}} > \frac{mr}{2(r_m - r_0)} \tag{12}$$

where $0 \le r$, r_0, $r_m < x$. If we assume $r_0 = 0$ and $r_m = r$, then (12) reduces to $\eta > m/2$. For our method, m should not be less than 2, and therefore, η is always larger than 1. If m is 1, our method reduces to the previous method. When the output is observed over some fixed time interval N, a smaller n yields a larger m, which improves the accuracy at higher frequencies. To detect a small x, N should be large, and this limits the dynamic response of a measurement system employing a CFC. Equation (7) also shows that q is not affected by the input offset voltage of COMP1, which is not the case in previous circuits.

If the compensation technique due to Chiang *et al.* were to be applied to our CFC over the complete range of the output frequency, n in (3)–(6) would be replaced by $n + k/4$, where k is a nonnegative integer that is less than 4. Equation (12) would still be valid, even though r is less than $x/4$. Their technique changes the output frequency for smaller n by means of an additional fast clock, with a frequency that is four times higher than that of the operating clock, and requires analog-to-digital conversion. Therefore, the circuit is complicated [7].

III. Experimental Results

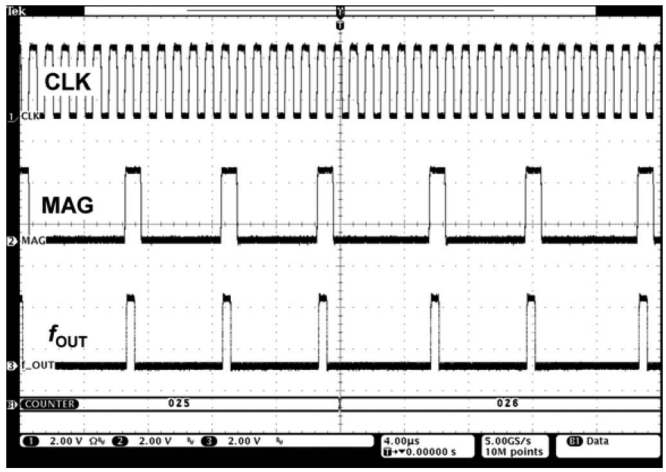
Our CFC has been designed and fabricated in a 0.35-μm double-poly four-metal (2P4M) CMOS process. It occupies an area of only 240×440 μm^2, as shown in Fig. 4, including capacitors C_{S} and C_{R} of 2 pF for experimental purposes. In addition, its op-amp is designed in a two-stage folded cascode structure to achieve a gain of 77 dB over a bandwidth of 18 MHz at the cost of 0.5 mW.

The circuit performance is summarized in Table I. Equations (4) and (8) show that the CFC measures a charge difference in a ratio to a constant charge. Therefore, the CFC can be used in two modes: 1) to measure a difference in capacitance, when V_{S}, V_{R}, and V_{Q} are constant, or 2) a difference in voltage, when C_{S}, C_{R}, and C_{Q} are constant. The characteristics of the CFC are assessed in voltage measurement mode with V_{R} set to 1.65 V. During measurement, no specific technique was applied to protect the circuit from external electromagnetic interference. In that condition, a difference between V_{S} and V_{R} of as small as 2 mV, which corresponds to 2.4 fF, could be measured with an accuracy of 1.2 mV.

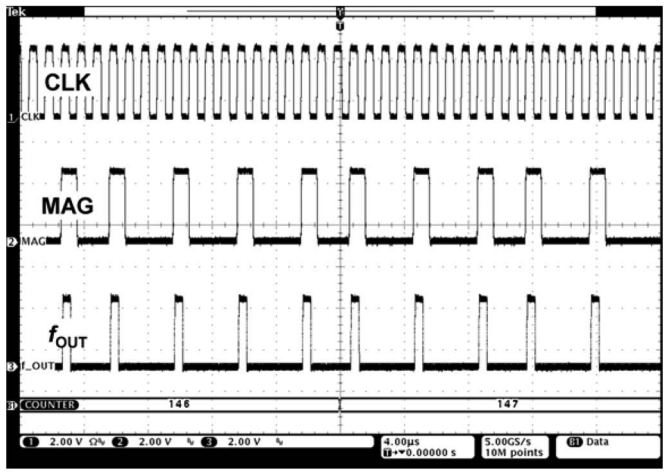
TABLE I
Performance Summary of the CFC

	[7]	This work
Technology	0.35μm 2P4M CMOS	0.35μm 2P4M CMOS
Power supply	3.2V	3.3V
Operating clock	2MHz	1MHz
Input capacitance	4-24pF	1.5-2.5pF [a]
Output frequency	0.5-500kHz	0-1MHz
Accuracy	±5.14%	±0.13%
Physical area	1.015mm^2	0.056mm^2

[a]This value is estimated from using the relative deviation of voltage-mode measurements.



(a)



(b)

Fig. 5. Oscilloscope display when the proposed CFC measured (a) V_{S} of 1.7 V and (b) that of 1.4 V.

The oscilloscope display during measurement is shown in Fig. 5, and the measured output frequencies of the CFC are

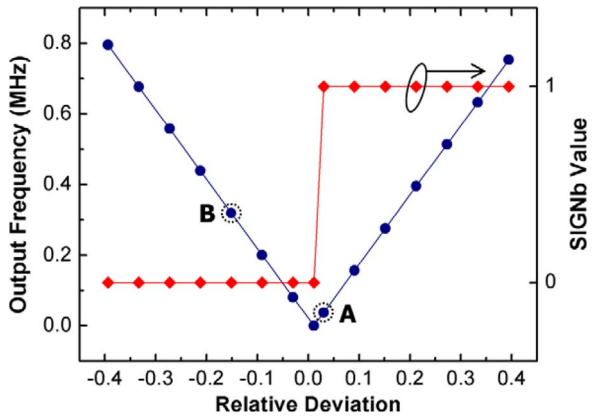


Fig. 6. Measured output frequency versus relative deviation for the CFC. [A: Fig. 5(a), B: Fig. 5(b)]

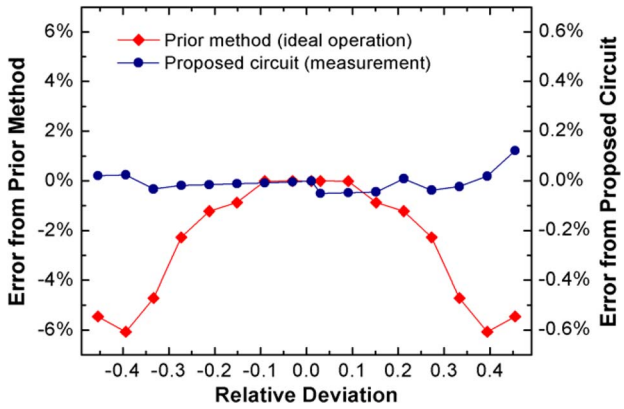


Fig. 7. Comparison between the simulated error of the prior compensation technique under ideal operating conditions and the experimentally measured error of the proposed circuit.

summarized in Fig. 6 with reference to the relative deviation of $V_{\rm S}$ from $V_{\rm R}$. For example, the measured outputs shown in Fig. 5(a) and (b) are when $V_{\rm S}$ is 1.7 and 1.4 V, which correspond to relative deviations of 0.03 and -0.15 in Fig. 6, respectively. These output frequencies were measured by using a 10-bit counter operating at the same clock frequency as the CFC. The counter counts the number of clock cycles during which MAG is high and a high-level pulse is seen at the output. When estimated for a given number of cycles, the output of the counter corresponds to $1/n_{\rm eq}$ in (11).

The sensing accuracy has been highly enhanced by the proposed CFC, as shown in Fig. 7. In this graph, errors are obtained for each measured point as the deviation of the measured output frequency from the expected output frequency. The errors are given in ratios to $V_{\rm R}$, and worst-case errors of both prior and proposed methods correspond to accuracies in Table I. When estimating errors from the prior compensation technique [7], we applied a behavioral model and obtained the following relationship assuming ideal operation of circuit components: if

$$\frac{1}{a+\frac{b+1}{4}} < \frac{x}{q} < \frac{1}{a+\frac{b}{4}} \tag{13}$$

for nonnegative integers a and b, then

$$\frac{\hat{x}}{q} = \frac{1}{a+\frac{b+1}{4}} = \frac{4}{\left\lceil 4\cdot\frac{q}{x}\right\rceil} \tag{14}$$

when (4) and (5) are referred to. The offset between $C_{\rm S}$ and $C_{\rm R}$ and that of $C_{\rm Q}$ were measured using (8), and their effect has been canceled in Fig. 7.

IV. Conclusion

We have described an enhanced-accuracy CFC for the capacitive sensors aimed at monitoring biomolecular reactions. Our CFC directly converts a capacitive difference of the sensor into a pulse frequency of a single pulse stream. By selecting pulses from a clock signal, a wide dynamic range of output frequencies has been achieved. Compared to about 6% with the prior compensation technique, the accumulation of residual charges achieves a sensing accuracy of as good as 0.13%. The CFC has a simple structure and only requires an active area of 0.056 mm^2 in 0.35-μm 2P4M CMOS technology.

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