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Letter

Direct extraction of semiconductor device parameters using lateral optimization method

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1. Introduction

Extraction and optimization of semiconductor device parameters is an important area in device modeling and simulation.[1–13] Regardless how sophisticated a semiconductor device model is, the model is useless and inaccurate if a viable parameter extraction method is not in place. The most widely used methods for extracting the semiconductor device parameters from the I–V measurements, using a junction diode as an example, can be classified into the following groups:

1. Extrapolation for the linear part of the plot of ln(I) versus V.[1] It is known that the presence of a large R can significantly obscure the linear characteristic of the ln(I) vs. V plot to such an extent that the parameters extracted from this method become unreliable.
2. Sophisticated algebraic manipulations[2,13] of the I–V data to generate plots which allow the separation of the effects of R. Norde[2] was the first to use this approach.
3. Use of the small-signal conductance,[4] or derivative of the current with respect to voltage. This method is highly sensitive to measurement errors because the derivative is equivalent to a high-pass filter.[1]
4. Use of integration of the current with respect to voltage.[10,11] This method is immune to measurement errors because the integration is equivalent to a low-pass filter.[10,11]
5. Addition of an external resistance in series with the device in I–V measurements.[9] This method requires further experimental work.
6. Direct vertical optimization of the parameters[12] from the I–V data by minimizing the vertical quadratic error:

$$\text{Vertical Error} = \sum_{j=1}^{n} \left(\frac{I_{\text{expj}} - I_{\text{simj}}}{I_{\text{simj}}} \right)^2 \tag{1}$$

where n is the number of experimental points, I_{expj} the jth measured current and I_{simj} the jth simulated current. It is called 'vertical optimization' because the error is minimized on the vertical axis (i.e. the current). However, as will be shown later, the direct vertical optimization method is quite computationally intensive. Nonetheless, such a method has become very popular because of its simplicity in concept and the availability of powerful computers and software.

In this paper, we will focus on a less known, yet powerful, extraction method called the 'direct lateral optimization' method based on the approach of minimizing the error on the lateral axis (i.e., the voltage). This method was first proposed by Bennet in 1987,[3] but its applications, robustness, and advantages have never been properly studied and documented. The main purpose of this work is to compare the efficiency (i.e., CPU time) and robustness (i.e., effects of the resistance and measurement errors on the accuracy of

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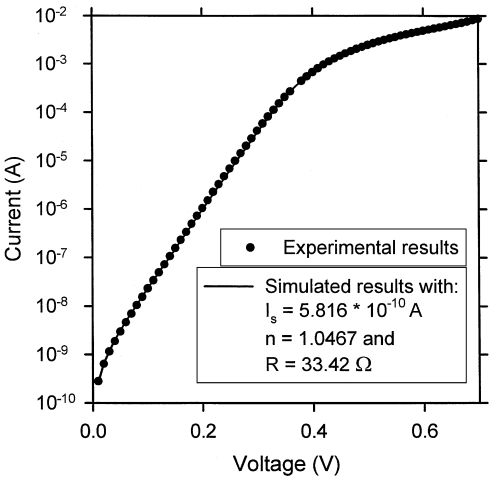

Fig. 1. I–V characteristics obtained from measurements (symbols) and from simulations (line) using the extracted parameters of $I_s = 5.81 \times 10^{-10}$ A, $n = 1.0467$ and $R = 33.4\ \Omega$.

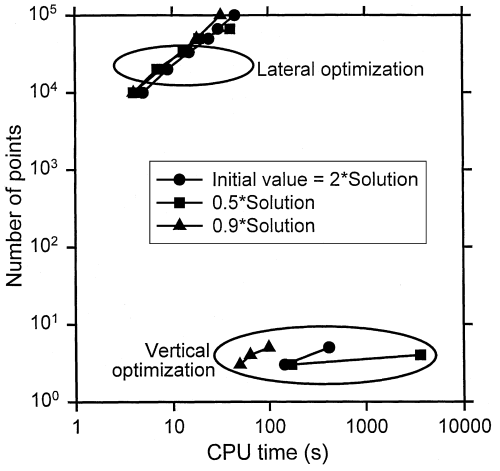

Fig. 2. Number of simulated points versus CPU time for the lateral and the vertical optimization methods using a PC with 300 MHz Pentium II microprocessor and 64 MB RAM. Three different initial values (i.e., $2\times$, $0.5\times$ and $0.9\times$ of the correction solution) were considered.

parameters extracted) of the widely used vertical optimization and the present lateral optimization methods under the environment of an industry standard statistical language called S-plus.[14]

2. Method development

For the purpose of this discussion, a junction diode will be considered here, but the approach generally applies to other semiconductor devices. The I–V characteristics of a p–n junction diode, or a Schottky diode, is frequently modeled by an ideal diode together with a parasitic resistance R:[1]

$$I = I_S \left(\exp\left(\frac{V - IR}{nV_{th}} \right) - 1 \right) \tag{2}$$

where I is the current passing through the diode, V the voltage applied to the junction, I_S the saturation current, n the ideality factor, and $V_{th} = kT/q$ the thermal voltage. Eq. (2) can be rewritten as

$$V = nV_{th} \log\left(\frac{I}{I_S} + 1 \right) + IR \tag{3}$$

which allows the evaluation for directing the voltage for a given current. Then by minimizing the errors on the voltage, the lateral quadratic error is

$$\text{Lateral Error} = \sum_{j=1}^{n} \left(\frac{V_{expj} - V_{simj}}{V_{simj}} \right)^2 \tag{4}$$

where n is the number of data points, V_{expj} the experimental voltage and V_{simj} the simulated voltage. The motivation for doing this is that V_{simj} can be directly evaluated from Eq. (3) without requiring any iterative solution. On the contrary, for the vertical optimization, an iterative solution is needed to calculate I_{simj}.

To illustrate this approach, we have applied the method to a diode from Motorola. Fig. 1 presents the experimental and the simulated I–V characteristics with the parameters of $I_s = 5.81 \times 10^{-10}$ A, $n = 1.0467$, and $R = 33.4\ \Omega$ extracted from the direct lateral optimization method and using S-plus software tool with a nonlinear optimization routine called 'nlregb' available in S-plus.[14] Our results also indicate that the same degree of accuracy for the fitting would be obtained if the direct vertical optimization were used.

To compare the speed of the lateral and vertical optimization methods, we generated data from AIM-SPICE[15] for several numbers of points, a voltage range from 0 to 1 V, and the extracted parameters of $I_s = 5.81 \times 10^{-10}$ A, $n = 1.0467$ and $R = 33.4\ \Omega$. Fig. 2 shows the required CPU time versus the number of points for the lateral and vertical optimization methods using a PC with 300 MHz Pentium II microprocessor and 64 MB RAM. In the figure, we have also tested the effects of different initial values on the CPU times for the two methods. The following three initial conditions are used: $2\times$, $0.5\times$, and $0.9\times$ of the correct solution. We find that for the same CPU time, the lateral optimization method allows for four more orders of magnitude data points to be calculated than with the vertical optimization counterpart. Therefore, the lateral optimization is much more efficient than the vertical optimization. We also see in this figure that the CPU time decreases quickly once the initial value

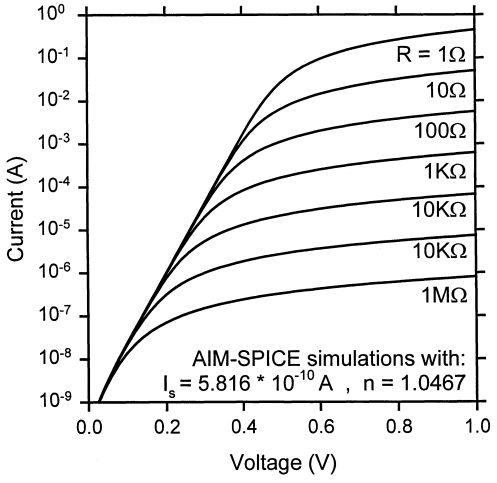

Fig. 3. Simulated I–V characteristics using the extracted parameters $I_s = 5.81 \times 10^{-10}$ A, $n = 1.0467$ and several different values of R.

used approaches the solution; a trend which is logical and expected.

Since large values of R can often obscure the extraction of device parameters, we now test the robustness of the present direct lateral optimization method with different values of R. Fig. 3 shows the I–V characteristics simulated using SPICE with $n = 1.0467$, $R = 33.4$ Ω and several different values of R. In addition, to account for possible errors in measurements (i.e., noise), the current is expressed as

$$I_{\text{with noise}} = I_{\text{without noise}} * (1 + \text{percent} * \text{random}) \quad (5)$$

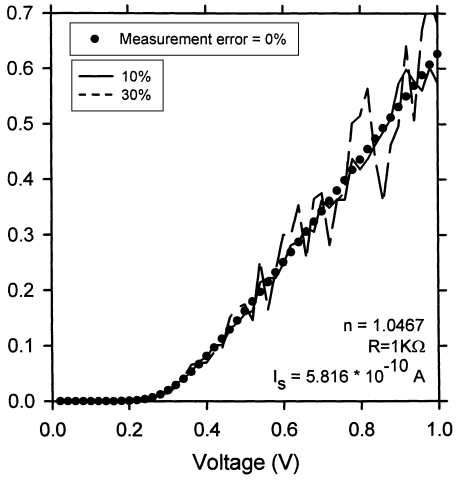

Fig. 4. I–V data with and without measurement errors (i.e., noise). For this particular plot, $I_s = 5.81 \times 10^{-10}$ A, $n = 1.0467$, $R = 1$ Ω, and noises of 0%, 10% and 30% are used.

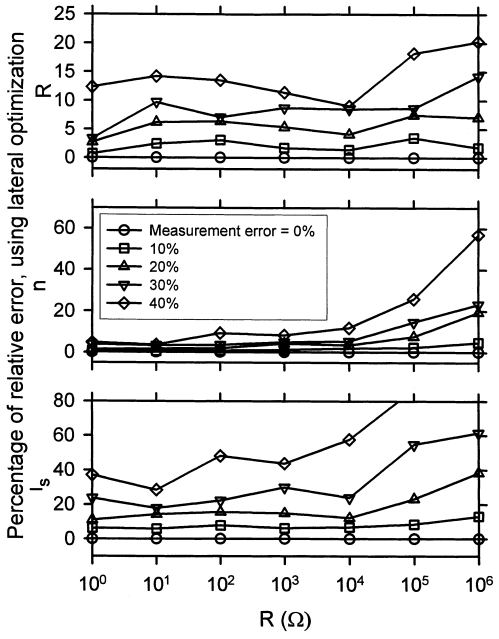

Fig. 5. The relative errors of R, n and I_s extracted from the lateral optimization method for various levels of measurement errors. The procedure of adding noise to the simulated data and then extracting the parameters was that the simulations were done 10 times for each case and that the largest value of errors was selected.

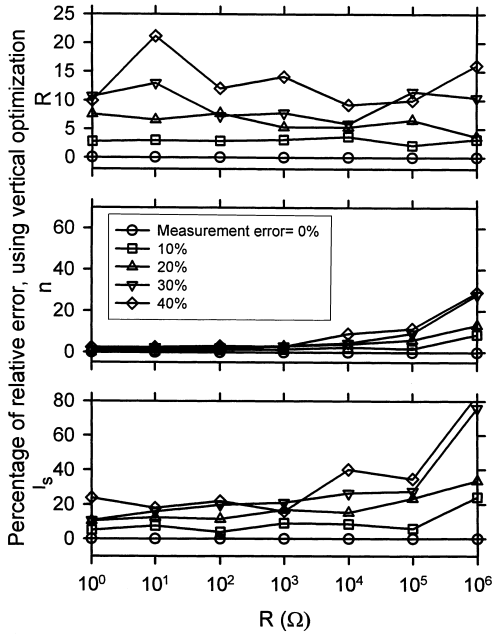

Fig. 6. The relative errors of R, n and I_s extracted from the vertical optimization method for various levels of measurement errors.

where $I_{\text{without noise}}$ is the AIM-SPICE simulated current, $I_{\text{with noise}}$ is the current with noise to be used in the parameter extraction, random is a randomly generated number between -1 and $+1$, and percent is the relative percentage of error to be added. A typical plot of the I–V data with and without noise is presented in Fig. 4. Fig. 5 presents the relative error in R, n and I_s versus R for various levels of noise. The parameter extraction with added noise was repeated 10 times for each case. We observe in Fig. 5 that the extracted parameters (R, n, and I_s) have very small relative errors when the noise level is below 20%, which is well within the tolerance of a typical experimental setup. The accuracy of the extracted parameters becomes questionable only when the noise is increased beyond 20% and/or the resistance value is approaching 1 MΩ. This demonstrates the robustness of the direct lateral optimization method. The same degree of robustness, however, is also found when using the direct vertical optimization method, as evidenced by the relative errors of the parameters extracted from this method shown in Fig. 6. Thus, it can be concluded that both the lateral and vertical optimization methods are equally insensitive to the errors associated with measurements.

In conclusion, by using a junction diode as an example, we have illustrated that the direct lateral optimization is an accurate, efficient, and robust method for extracting semiconductor device parameters. The widely used direct vertical optimization method, on the other hand, has the same degree of accuracy and robustness but the disadvantage of being much less efficient.

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