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Low-Leakage Ultra-Scaled Junctions in MOS Devices ; from Fundamentals to Improved Device Performance

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The aim of this work is to design ultra-scaled low-leakage junctions suitable for metal-oxide-semiconductor device scaling in bulk silicon. We begin with fundamental diode characterization analysis. Electrical behavior of fabricated diodes is then used to validate our device simulation modeling methodology, where established models are used to gain further insight and understanding in the junction leakage problem. Based on that effort, innovative junction scaling solutions are generated and realized in a silicon device experiment. Finally improved transistor performance is demonstrated.

Introduction

Leakage currents in metal-oxide-semiconductor (MOS) devices are undesirable as they drain power supply resources in integrated circuits and systems. Junction leakage is growing due to increased ultrashallow junction steepness, increased channel and pocket concentrations, increased junction curvature, and reduced annealing thermal budget which promotes the presence of residual defects. Literature on reversed biased junction leakage in diodes has been available for many decades now, however there are a number of aspects of modern MOS device processing and design that necessitate an updated study of junction leakage. Specifically it is necessary to determine which physical mechanisms are most responsible, and what should be done to alleviate the problems.

Furthermore, previous studies of leakage are almost exclusively devoted to investigations in one-dimension (1D). If the device operation is primarily 1D, such as in a bipolar transistor for example, that is sufficient. This approach is not always reliable if you consider a two-dimensional (2D) problem, namely the junction in a MOS transistor, where the curvature of the junction significantly affects the electric field (E_{FIELD}). As devices scale electric fields are increasing at a dramatic rate, and in the presence of high electric fields tunneling becomes the dominant current generation mechanism under reverse bias conditions.

Both doping profiles and damage/defects contribute significantly to junction leakage. In simple terms, in an ideal junction we have no defects and thus the junction leakage is determined by the doping profile. In a non-ideal junction where we have residual defects, junction leakage is a combination of the doping profile contribution and the damage contribution. End-of-range (EOR) damage, dopant precipitates, and dopant-defect precipitates are common sources of non-ideal currents in modern device technologies.

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We quantify the contribution of the key elements through a combination of experiment and device simulation. Thereafter, using predictive simulations and evaluation in a MOS device experiment, high tilt implants and lowly-doped junctions are shown to improve short channel effect control without significantly degrading drive or leakage. These concepts are thus attractive for future generation bulk silicon devices.

Understanding Junction Leakage

Theory

Generation mechanisms that lead to leakage currents are temperature and/or electric field dependent. To extract what mechanisms are dominating we need to analyze (i) the voltage dependence and (ii) the temperature dependence of the leakage current. The most relevant mechanisms to our study are diffusion current, Shockley Read Hall (SRH) generation, trap assisted tunneling (TAT), and band to band tunneling (BBT). An effective method for determining the different physical components in reverse leakage currents is to perform measurements at elevated temperatures [1,2], in order to extract the activation energy (E_A).

Diffusion current occurs when carriers, which are at a higher energy than the potential barrier, diffuse across from one side of the junction to the other. Ideal diffusion current is proportional to n_i^2, where n_i is the intrinsic carrier concentration. The temperature dependence behavior is related to the temperature dependence of n_i, which is $\propto \exp(-E_G/2kT)$, where E_G is the bandgap of silicon. Thus $I_{ideal} \propto \exp(-E_G/kT)$, and E_A is expected to be close to E_G.

SRH generation is temperature dependent, electric field dependent, and relies on the presence of deep levels in the depletion region. SRH generation occurs when an electron that is trapped in a deep level, gains energy, and climbs out of the Coulombic well. SRH dominated current is proportional to $V^{0.5}$. SRH generation is proportional to n_i. The temperature dependence is thus related to the temperature dependence of n_i, so $I_{SRH} \propto \exp(-E_G/2kT)$, and E_A is expected to be $E_G/2$.

TAT can be considered as SRH in the presence of an electric field, or as a combination of electron capture and tunneling through the barrier. In this case the tunneling electron uses a deep level trap in the depletion region as a stepping stone to make the transition. TAT is also temperature dependent and the extracted E_A of the current characteristics will indicate a trap level within the band gap. Usually this value is close to $E_G/2$.

BBT occurs when the electric field across the pn junction is strong enough to propel an electron from the valence band on the p-side through the potential barrier and forbidden band gap, into the conduction band on the n-side. Hurkx [3] showed that BBT $\propto \exp(-E_G^{0.5}/E_{FIELD}^{\max})$, where $E_{FIELD}^{\max}$ is the maximum electric field. The probability of BBT increases if the electric field increases or if the tunneling distance decreases. BBT becomes important above a local electrical field strength of 7×10^5 V/cm [4]. In general the temperature dependence of BBT is related to the temperature dependence of E_G. As a

rule of thumb, BBT increases approximately ×2 for a 100 °C increase above room temperature [3], so E_A is quite close to 0 eV.

A summary of the important leakage mechanisms is listed in Fig. 1.

Current mechanism	Characterised by
Diffusion	$E_A \sim E_G$
SRH	$E_A \sim E_G/2$, Current is $V^{½}$ dependent
TAT	$E_A \sim E_G/2$, Current not $V^{½}$ dependent
BBT	$E_A \sim 0$

Figure 1. Characteristics of different reverse bias leakage mechanisms. E_G is the bandgap of silicon = 1.12 eV.

Finally, at low forward biases the ideality of the junction can be determined from the slope of the current-voltage curve. In the ideal case the slope is q/kT, but in the non-ideal case in the presence of recombination centers in the depletion region, the slope is q/nkT, with n>1. This parameter n is known as the ideality factor.

Experiment

Diodes were fabricated with different doping profiles to quantify how each of these factors contribute to reverse bias leakage. The key to this study was that after electrical characterization the fabricated diodes were subjected to a deprocessing step where the contact metallization was removed, so that secondary ion mass spectrometry (SIMS) analysis could extract the doping profiles from the structures that were measured electrically. The resulting doping profiles were then used as input in the device simulator MEDICI [5] to enable a closer evaluation of the electrical measurements and to validate the accuracy of device simulation models. The ultimate aim of the experiment was to use the validated models for predictive device simulations on future generation MOS device performance.

In summary the process flow consisted of standard processing to define the active area and isolation. A 5 nm screen oxide was deposited, and subsequently boron and phosphorus implants were performed. Process conditions were chosen to create a junction depth at ~300 nm. During the metallization removal, the silicon surface may be roughened, which may lead to inaccuracies in the SIMS analysis close to the surface. To ensure accurate SIMS profiling at the metallurgical junction, a deep junction depth was targeted. The activation anneal was 1050 °C 60 s. This high thermal budget was chosen so the boron profile was diffused in, and thus the metallurgical junction was moved away from the damaged region of that high dose implant. The rest of the flow consisted of a clean step to remove the screen oxide, and the deposition of a Ti/TiN contact layer. Finally a 650 nm layer of AlCu metal was deposited and patterned.

Current-voltage characteristics of the diodes were measured using a HP4155 parameter analyzer. A thermochuck was used to investigate temperature dependency. For each structure and split several die were measured. In general, the within wafer

reproducibility of the measurements was good, as there was little significant spread from die to die. Most of the measurements were done on square diodes, consisting of a rectangular active area with a high area to perimeter ratio.

After electrical characterization of the diodes, the contact metallization was removed by using a standard Al etch followed by a standard Ti etch. Impurity profiles were then determined by SIMS analysis using 3 keV O_2^+ primary ions. The concentration scales were determined using a known calibration standard in silicon.

The diodes in this section are labeled D1, D2, D3, D4, and D5, according to the variation in phosphorus concentration. Diode D1 has the highest phosphorus concentration, diode D5 has the lowest phosphorus concentration. Shown in Fig. 2 are SIMS depth profiles for the 5 different diodes. The boron profile is the same for all cases. The phosphorus concentrations at the junction are 6.3×10^{18}, 2.6×10^{18}, 1.3×10^{18}, 5×10^{17}, and 5×10^{16} cm^{-3} for diodes D1 – D5 respectively.

Fig. 3 shows the corresponding reverse bias leakage current density as a function of reverse bias voltage. Current density increases with reverse bias and background concentration. For approximately 2 orders of magnitude increase in phosphorus concentration, the current density at 1 V increases by approximately 8 orders of magnitude. At high phosphorus concentrations the electrical characteristics are dominated by high electric fields. Diodes D1 and D2 are dominated by BBT. The flat-topped nature of the D1 characteristics at high biases indicates that the current density is limited by the substrate resistance. BBT dominates diode D3 at high biases. At low biases TAT is more significant. For diode D4 the TAT regime is larger and it requires higher biases in this case to generate BBT. Finally, diode D5 has relatively low electric fields, and there is no BBT regime evident at the measured biases. In diode D5 the current is proportional to $V^{0.5}$, so SRH is the dominant mechanism.

The temperature was then stepped between 25 °C and 105 °C, in 10 °C increments. An example of this measurement is shown in Fig. 4 for diode D3. Clearly there is a temperature dependent regime at low biases (TAT), and a temperature independent regime at high biases (BBT). Using the temperature dependency measurements, the leakage current was plotted as a function of 1/kT. These results are shown in Fig. 5 for diodes D1, D3, and D5. In diode D1 characteristics there is voltage dependence but not much temperature dependence. For diode D3 there is major voltage dependence and a transition from temperature dependence to temperature independence. Diode D5 shows the greatest temperature dependence with the lowest voltage dependence. From these plots E_A was extracted at selected voltages. For diodes D1 – D4 only one E_A was extracted as the current versus 1/kT produced a straight-line, but for diode D5 there were different E_A values at high and at low temperatures.

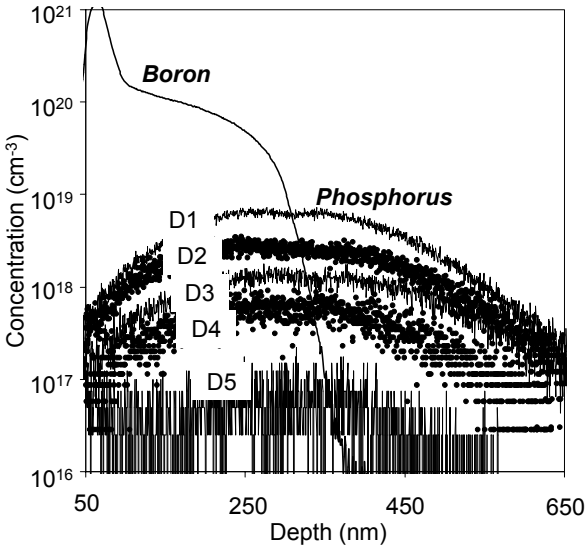

Figure 2. SIMS depth profiles of boron and phosphorus for the diodes D1-D5.

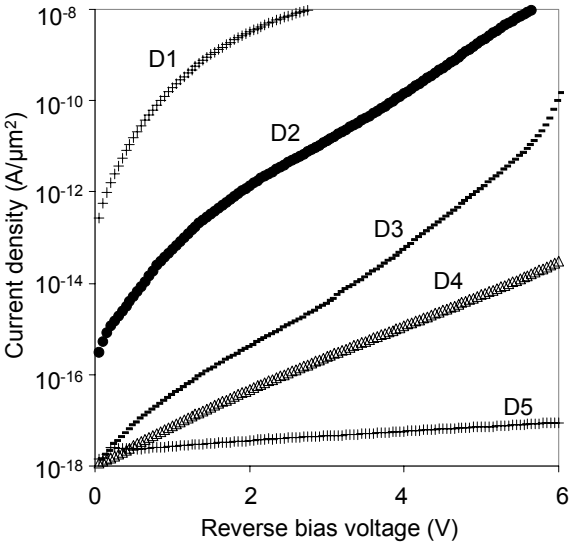

Figure 3. Reverse biased current density versus reverse bias, for the diodes D1-D5, corresponding to the SIMS depth profiles in Fig. 2.

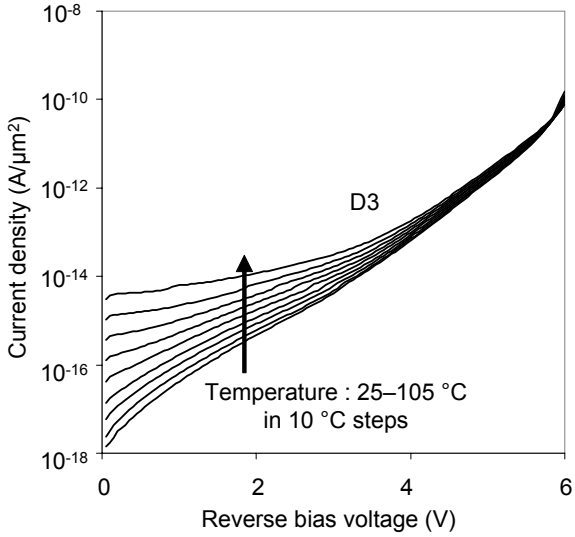

Figure 4. Reverse biased current density versus reverse bias, for the diode D3, as temperature is varied between 25 °C and 105 °C.

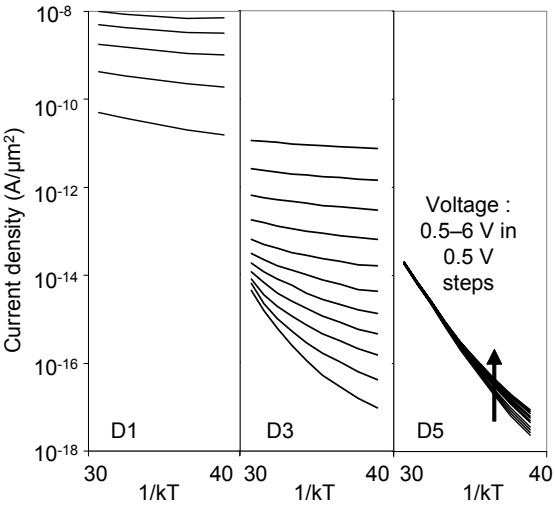

Figure 5. Reverse biased current density versus 1/kT. Voltage is sampled in 0.5 V steps between 0.5 and 6.0 V. For clarity only diodes D1, D3, D5 are shown.

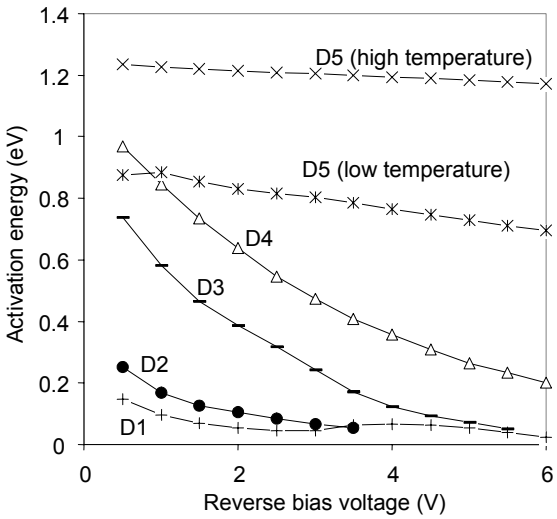

Figure 6. Activation energy of the current density characteristics, as a function of reverse bias, extracted from Fig. 5.

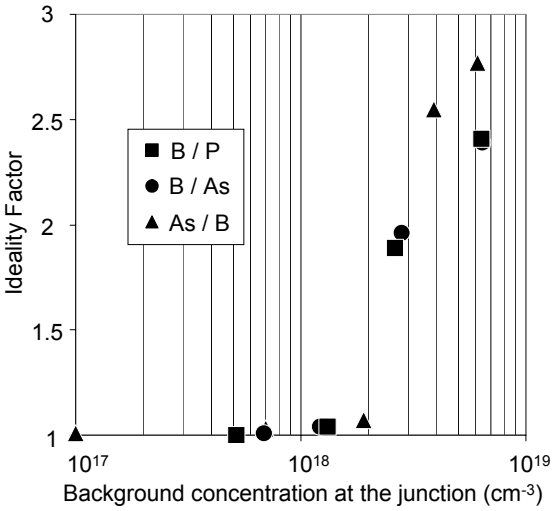

Figure 7. Forward bias ideality factor versus background concentration at the junction for all the diodes in this work. The behavior becomes non-ideal above concentrations of 2×10^{18} cm^{-3}.

E_A versus reverse bias voltage is plotted in Fig. 6. Where E_{FIELD} mechanisms dominate $E_A \sim 0$ eV, where thermally driven mechanisms dominate $E_A > 0$ eV. For diodes D1 and D2 $E_A \sim 0$ eV which is an indication that the leakage currents are dominated by E_{FIELD} mechanisms. For diode D3, $E_A \sim 0.8$ eV at reverse bias = 0.5 V and drops toward 0 eV as bias increases. This indicates that the E_{FIELD} mechanisms don't fully dominate at low biases, but become more significant as the voltage is increased. The trend is similar for diode D4, $E_A \sim 1.0$ eV at reverse bias = 0.5 V and drops toward 0 eV as bias increases. For diode D5 at high temperatures diffusion current is evident as $E_A = 1.2$ eV. At low temperatures SRH generation is confirmed from the midgap E_A.

A summary of forward bias characteristics is shown in Fig. 7. Ideality factor is plotted versus background concentration. Also included are data from boron-arsenic p^+n diodes and arsenic-boron n^+p diodes. As background doping concentration increases, the diodes become less ideal. At 2×10^{18} cm^{-3} there is a sharp change. Despite the difference in background doping species the 3 sets of diodes follow the same trend line.

Figure 8 shows current density at 1 V versus background concentration for the 3 sets of diodes. There is an 8 order of magnitude increase in leakage across the concentration range of $1.5 - 4\times10^{18}$ cm^{-3}. This is highly significant as modern MOS bulk-technology devices now use channel/pocket concentrations in this range [6]. Thus minor changes in pocket concentration would lead to a large leakage change. Again the 3 sets of diodes follow the same trend, independent of background doping species.

Simulations

The SIMS doping profiles were then used as input in the device simulator MEDICI to enable a closer evaluation of the electrical measurements and to validate the accuracy of the physical models. Established models were used throughout [5,7]. Models were included for SRH, Auger recombination, TAT, BBT, and self-consistent impact ionization. Some minor calibration to BBT prefactor and carrier lifetimes were undertaken to improve the fit between simulated and experimental current versus voltage characteristics.

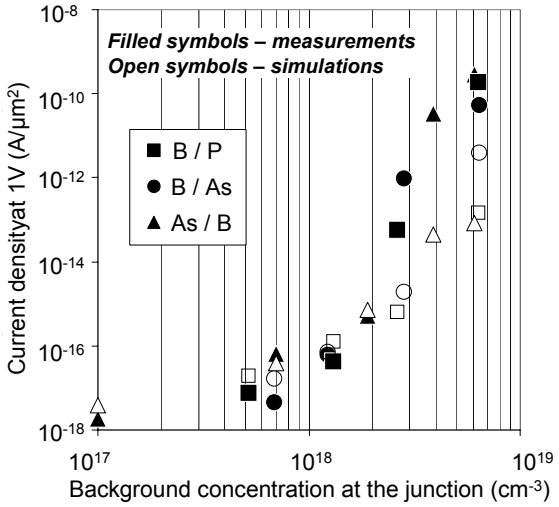

Figure 8. Current density at 1 V reverse bias versus background concentration at the junction for all the diodes in this work. Also included are simulated characteristics from the device simulator MEDICI.

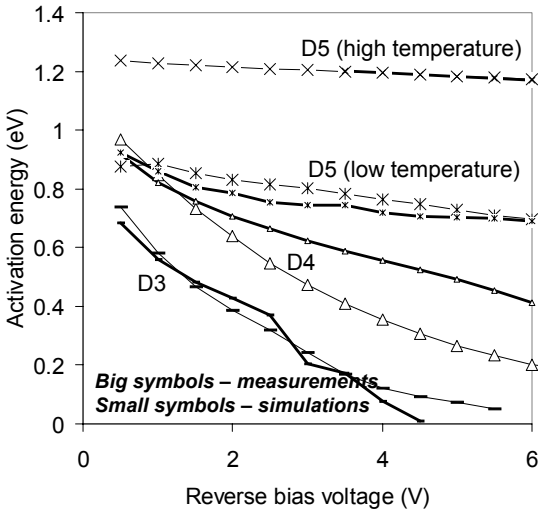

Figure 9. Activation energy of the current density characteristics for diodes D3-D5, as in Fig. 6. Also included are the simulated characteristics.

In Fig. 8 is a comparison between the simulated and experimental diode leakage at 1 V reverse bias. The measurements and simulations diverge at background concentrations above 2×10^{18} cm^{-3}. Note this divergence corresponds to the transition to non-ideal diode behavior (c.f. Fig. 7), and is independent of background dopant type as boron, arsenic, and phosphorus all produce this phenomenon. The physical reason for the failure of established models to reproduce the non-ideal behavior is still under investigation. The temperature independence of the high leakage levels point to an E_{FIELD} dominated mechanism, and may be linked to a local electric field enhancement due to precipitates or clusters.

Shown in Fig. 9, for ideally behaved diodes D3, D4 and D5, the experimental E_A values are reproduced very well by the simulations.

In conclusion, MEDICI can accurately quantify leakage in ideal junctions and predict the dominant physical mechanisms responsible.

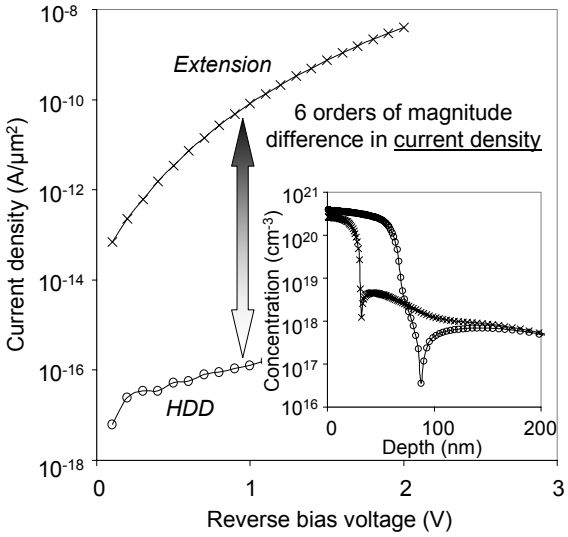

Figure 10. Simulated reverse biased current density versus reverse bias, highlighting the difference of the local electric field at the extension and HDD junctions. The inset shows doping profiles generated by 1D process simulation for both junctions.

ITRS specs for technology production in 2007 :	LSTP
V_{dd} (V)	1.1
I_{OFF} (A/μm)	2.5×10^{-11}
Physical gate length (nm)	**37**
Extension abruptness (nm/dec)	4.1
X_J (nm)	20.3
L_{EXT} (nm)	32
J_{OFF} (A/μm²)	7.8×10^{-10}
J_{OFF} for doping effects, assuming the presence of defects (A/μm²)	7.8×10^{-12}

Figure 11. ITRS roadmap targets from the hp65 technology node for Low Standby Power (LSTP) devices. Values for L_{EXT} and J_{OFF} are calculated here.

The first step in evaluating junction leakage in a MOS device is to establish which part of the junction leaks the most; the extension or the deep highly doped drain (HDD). In terms of *current density* it is expected that the extension will leak more as that junction is significantly more abrupt, and the background concentration is much higher.

As an illustration of this point, 1D process simulations were performed using TSUPREM4 using standard process parameters and models. Implant doses and energies are representative of a modern NMOS process, and a standard high-temperature spike anneal was simulated for activation. In the inset of Fig. 10 are net doping profiles of the simulated NMOS extension and HDD junctions. Note that the p-type doping at the junction is higher in the extension case. As the HDD profile is so deep, it covers most of the pocket profile and thus the p-type doping there is determined by the threshold voltage adjust (anti-punchthrough) implant. In the main part of Fig. 10 the reverse bias current densities for these doping profiles are plotted. At 1 V reverse bias, the current density is 6 orders of magnitude higher at the extension. BBT is the dominant mechanism in the extension case. At the HDD there is no significant BBT.

In the case of a real device however, the area of each junction must be considered. If the widths of both junctions are the same, the length of the extension (L_{EXT}) and of the HDD (L_{HDD}) are the important parameters. In a simplified way L_{EXT} can be considered one quarter of the circumference of a circle, with a radius equal to the junction depth (X_J). Here we take $X_J = 20$ nm to be typical, then $L_{EXT} = ¼ \times 2\pi r \approx 32$ nm. L_{HDD} is defined as 3× the DRAM half pitch, or 3× the technology node. For 45 nm technologies, $L_{HDD} =$ 135 nm. Thus the area of the HDD junction is larger, but by less than 1 order of

magnitude, and so the leakage current (current density × area) is far greater at the extension junction.

Figure 11 shows ITRS roadmap [6] targets from the *hp65* technology node for Low Standby Power (LSTP) devices. Target specs for V_{dd}, off-state current (I_{OFF}), physical gate length, extension abruptness and X_J are listed. The extension abruptness and X_J values are functions of the physical gate length. The extension abruptness = 0.11 × the physical gate length. The extension X_J = 0.55 × the physical gate length. Values for L_{EXT}, J_{OFF}, and J_{JUNC} are calculated here.

Before we can compare junction leakage characteristics to the spec, I_{OFF} needs to be converted to current density (J_{OFF}) for the purposes of our discussion. The length of the extension is again calculated according to the equation $L_{EXT} = ¼ \times 2\pi \times X_J$, = 32 nm. The I_{OFF} spec converted to J_{OFF} becomes 7.8×10^{-10} A/μm^2. The ITRS roadmap assumes that junction leakage is only a minor component of the off-state leakage. For simplicity in this analysis we consider the best case scenario for junction integration, where I_{OFF} is allowed to be 100 % junction leakage dominated. So the junction leakage current density (J_{JUNC}) spec is thus 7.8×10^{-10} A/μm^2.

From our work quantifying the contribution of defects, which will be presented elsewhere, current density in the presence of EOR defects is increased by approximately 2 orders of magnitude. If our junctions have EOR defects, the J_{JUNC} spec for the doping profile contribution must be lowered by 2 orders of magnitude, and thus becomes 7.8×10^{-12} A/μm^2.

These doping profile leakage limitations, along with the abruptness requirements, define target regions within which the reverse bias junction leakage current densities need to be. These will now be evaluated, using our validated device simulation methodology.

Shown in Fig. 12 are simulations of ideal diode behavior at 1.1 V reverse bias. There are 2 variables, namely the steepness of the extension profile, and the background concentration which represents the pocket profile. The peak activation of the extension is assumed to be 2×10^{20} cm^{-3}. As both extension steepness and background concentration increase, the current density increases. Also included in the graph is a guideline for where BBT dominates the leakage current. Typically for junctions that produce low local electric fields BBT is not significant, while for junctions that generate high electric fields BBT dominates.

With defects remaining after junction formation the 3×10^{18} cm^{-3} background concentration curve cannot penetrate the target box. With curvature enhancement included (2D simulations) the story is even worse. Fig. 13 shows the corresponding analysis with curvature included. The curvature enhancement is most significant for steep extensions, and now the 2×10^{18} cm^{-3} background concentration curve cannot penetrate the target if there are EOR defects present.

All of this analysis poses serious concerns that steep shallow junctions with defects can be used in the fabrication of future LSTP MOS devices with acceptable I_{OFF} control.

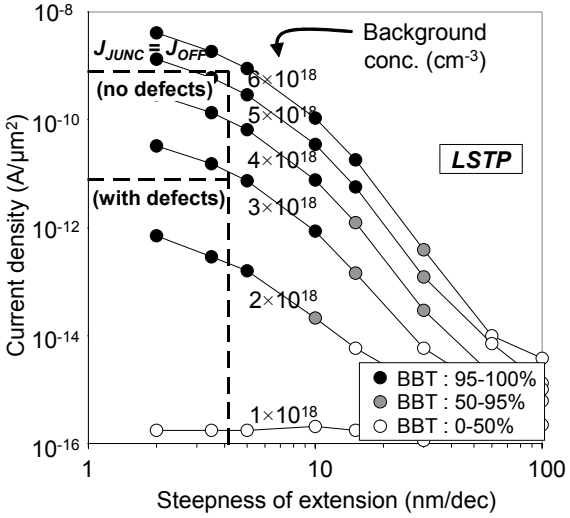

Figure 12. Simulated current density at 1.1 V reverse bias versus extension profile steepness and background concentration. The boxes indicate LSTP technology targets (with or without EOR defects) when I_{OFF} is dominated by junction leakage.

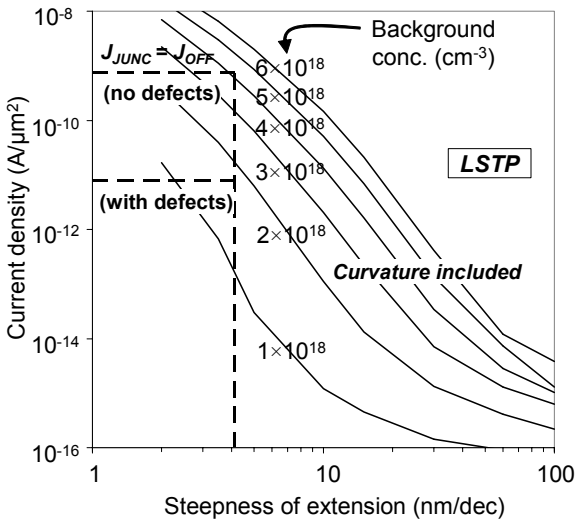

Figure 13. The same analysis of Fig. 12, but with curvature enhancement effects included in the simulations.

Low Leakage MOS Scaling Solutions

Simulations

So we know we have problems making scaled junctions in bulk MOS devices. In this section we identify potential solutions. Primarily we would like to scale the junction without increasing the local E_{FIELD} and possibly reduce it.

Previously, in Fig. 13 the curvature of the junction was shown as a source of increased leakage, so if this could be reduced, then leakage would follow. In Fig. 14 is an illustration of this fact. If the curvature of the junction is tailored, as shown in our 2D simulations, the peak E_{FIELD} and thus the junction leakage, can be reduced.

Figs. 15 and 16 show E_{FIELD} for more realistic junction solutions. In Fig. 15(a) is E_{FIELD} at 1 V reverse bias for our reference NMOS junction ; arsenic high-dose low-energy implant followed by conventional high-temperature spike anneal. The standard MOS scaling trends over the past few decades would require an increase of the pocket concentration, so as to prevent an increase of short channel effects (SCE) as the gate length is reduced. However as shown in Fig. 15(b) a 40% increase in pocket implant dose causes a large increase in E_{FIELD} at the junction.

Fig. 15(c) shows a *high tilted (HT)* implant scaling solution [8]. Conventional extension implants are typically done at 0 or 7° tilt, while 45° tilt implants are used for HT junctions. This high tilt ensures good junction to gate underlap. Thereafter a 0° tilt secondary implant is performed to maintain low junction sheet resistance.

Fig. 15(d) shows the *lowly doped (LD)* extension scaling solution [9,10,11]. This requires a low dose (10^{14} cm^{-2}) implant, followed by spacer processing, and then a high dose implant. It is somewhat counter-intuitive to purposely create a lowly doped region which will have high resistance. However, with modern spacer dimensions the high resistance region is quite short, and thus the contribution to the total resistance path is insignificant. Clearly both Fig. 15(c) and (d) show these alternative scaling approaches reduce the E_{FIELD} at the junction.

Fig. 16 shows cutlines through the plots of Fig. 15, quantifying the reduction of E_{FIELD}. The HT and LD concepts reduce the peak E_{FIELD} by ~25% over the conventional pocket concentration increase approach.

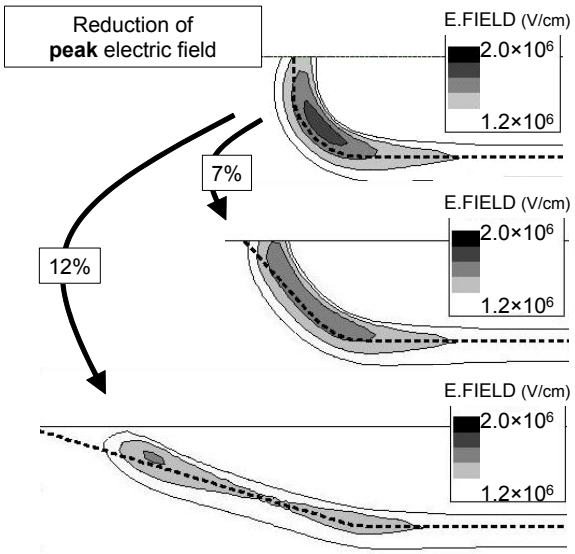

Figure 14. Simulated 2D electric field contours showing that lateral junction profile engineering can significantly lower the peak local electric field and thus reduce junction leakage. The values shown are for extension steepness=3.5 nm/dec, and background concentration=4×10^{18} cm^{-3}.

Extra simulations were undertaken to gain further insight into the benefits of the lowly doped extension. User-specified NMOS devices were defined in the device simulator with a 30 nm gate length, and 1.2 nm oxide thickness. Gaussian doping profiles for extension regions had a fixed abruptness and variable peak active concentration. The workfunction of the gate electrode is altered to counteract I_{OFF} changes with extension variation. This technique is also known as *workfunction engineering*. In this case I_{OFF} is fixed at 100 pA/μm.

Shown in Fig. 17 is a plot of extension peak concentration versus change in on-state current (I_{ON}). With the peak concentration in the range of 5×10^{19} - 1×10^{20} cm^{-3} I_{ON} is maintained at a constant level. Below 5×10^{19} cm^{-3} there is a drop in drive due to increased series resistance. Above 1×10^{20} cm^{-3} there is a drop in I_{ON} as SCE control becomes difficult through workfunction engineering. In summary the extension peak concentration can be reduced below what is conventionally thought to be needed (>10^{20} cm^{-3}) and drive can be maintained. The benefit of doing this is shown in Fig. 18, where the reduction of extension peak concentration produces better SCE control in terms of improved subthreshold slope and drain induced barrier lowering (DIBL) characteristics.

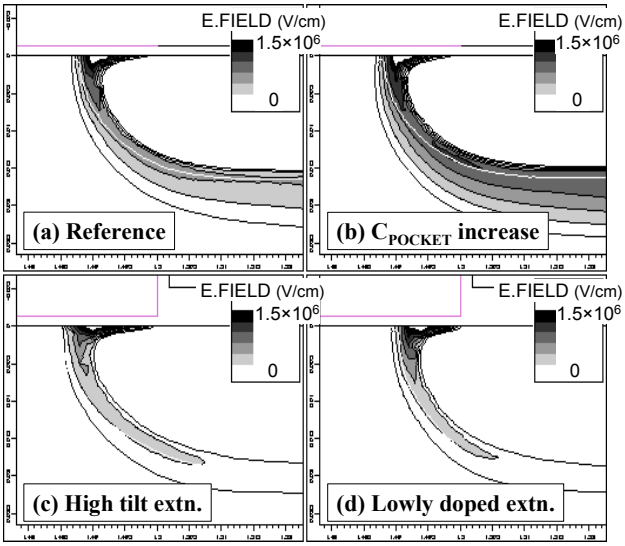

Figure 15. Simulated electric field contours at the drain junction in off-state. (a) is the reference NMOS junction, (b)-(d) are different scaling schemes.

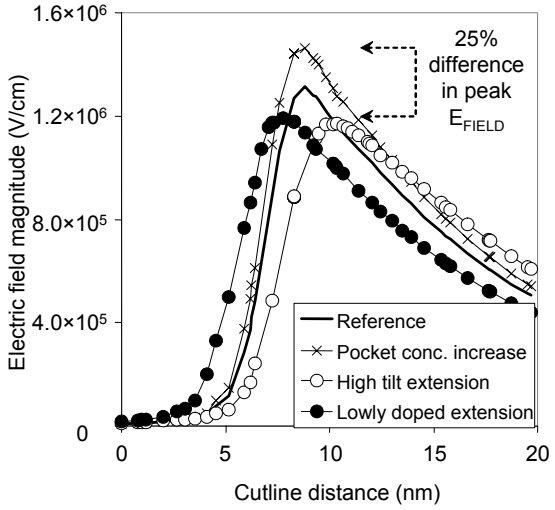

Figure 16. Cutlines at 45° through the junction simulations of Fig. 15. The conventional scheme leads to a significant increase in the peak electric field.

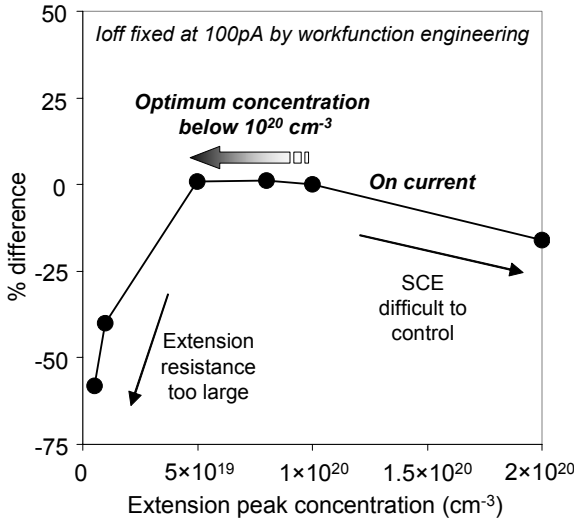

Figure 17. Simulated % difference in I_{ON} as a function of extension peak concentration. I_{OFF} is fixed by work function engineering of the gate electrode.

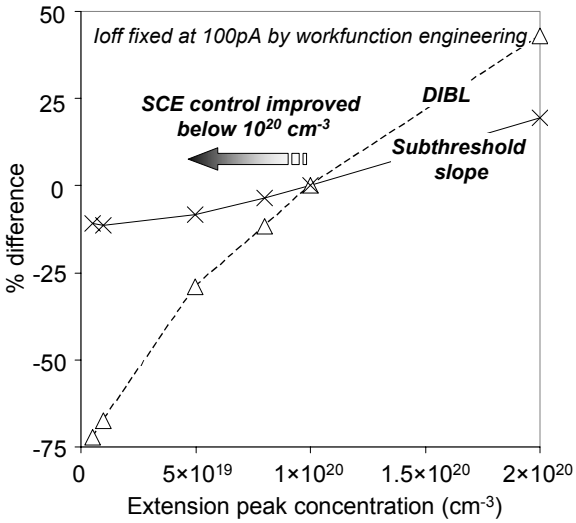

Figure 18. Simulations correlated with Fig. 17, extension peak concentrations < 10^{20} cm^{-3} provide a benefit in terms of SCE control.

Experiment

We evaluated the HT and LD junction concepts in NMOS devices. The baseline flow consisted of shallow trench isolation, boron well doping, silicon oxynitride (SiON) as gate dielectric with equivalent thickness = 1.5 nm, and 100 nm polysilicon as gate material. After gate re-oxidation, arsenic extensions and boron pockets were implanted. The high tilt implants were carried out at 5 keV through a 5 nm PECVD oxide liner that was deposited to limit the lateral and vertical extent of the implanted profile. In the deposition conditions, this layer is about 2.5 nm thick on gate sidewalls while it is 5 nm thick on horizontal surfaces. Spacer processing for LD extensions involved a 5 nm PECVD oxide liner and a 20 nm RTCVD nitride layer, leading to approximately 15 nm sidewall thickness after etch and strip. The extension processing is summarized in Fig. 19. Some LD cases had an intermediate spike anneal between the low dose and high dose implants. After extension processing, standard offset spacer and HDD processing was performed. All implants were activated with a 1050 ºC spike anneal. While a conventional zero stress contact-etch liner was deposited on most wafers, one wafer with the baseline conditions for extension processing received 100 nm of a moderately strained nitride liner. Conventional nickel silicide and single level copper/oxide back-end processing completed the flow.

Baseline	High tilt	Lowly doped
7×10^{14} cm^{-2} 1 keV	***T1*** : 7×10^{14} cm^{-2} 5 keV 45° + 1×10^{15} cm^{-2} 2 keV	***L1*** : 1×10^{14} cm^{-2} 1 keV + spike + 15 nm spacer + 7×10^{14} cm^{-2} 1 keV
	T2 : 1×10^{15} cm^{-2} 5 keV 45° + 1×10^{15} cm^{-2} 2 keV	***L2*** : same as L1, but with 30 nm spacer
	T3 : same as T2, but with optimized pocket	***L3*** : 1×10^{14} cm^{-2} 2 keV + 5 nm oxide liner + 1×10^{15} cm^{-2} 1 keV

Figure 19. Processing for the baseline, high tilt, and lowly doped extensions. All implants were arsenic at 0° tilt, unless otherwise mentioned.

For a fixed I_{OFF} of 10^{-7} A/μm, physical gate length (L_{PHYS}) and I_{ON} were extracted for a supply voltage of 1 V. These results were normalized to the baseline performance, and are plotted as relative L_{PHYS} and relative I_{ON} in Fig. 20. The median value of several measured die is shown. As expected strain engineering gives a boost in drive, but no enhancement in scalability. For the HT cases, T1 is similar to the baseline, and T2 is worse, yielding a larger L_{PHYS} for fixed I_{OFF}. With an optimized pocket implant T3 has much better SCE control, and L_{PHYS} can be scaled by ~25 nm compared to the baseline. The I_{ON} increase is correlated to an improvement in subthreshold slope. For the LD cases, all 3 variants here have better SCE control than the baseline. However the series resistance becomes significant if the lowly doped region is long, as with the 30 nm spacer in L2. For aggressive scaling L1 produced ~40 nm L_{PHYS} reduction at a ~5 % cost in I_{ON}. L3 is an attractive solution as the processing is most straight-forward.

Figure 21 shows off-state gate and bulk current at 1 V for long channel devices (L_{PHYS} ~200 nm). Again we plot the median value of several measured die. The gate current is gate-to-drain tunneling current. The bulk current is a mix of junction leakage and gate-induced-drain-leakage (GIDL). Note that the gate current is several orders of magnitude higher than the bulk current due to the thin SiON dielectric used in this

experiment. Compared to the baseline the LD junctions reduce gate leakage due to a reduced junction underlap and a voltage drop across the resistive region. The HT junctions show gate leakage slightly higher than the baseline, which again is related to the underlap. The junction and GIDL leakage have not been compromised by the LD and HT concepts.

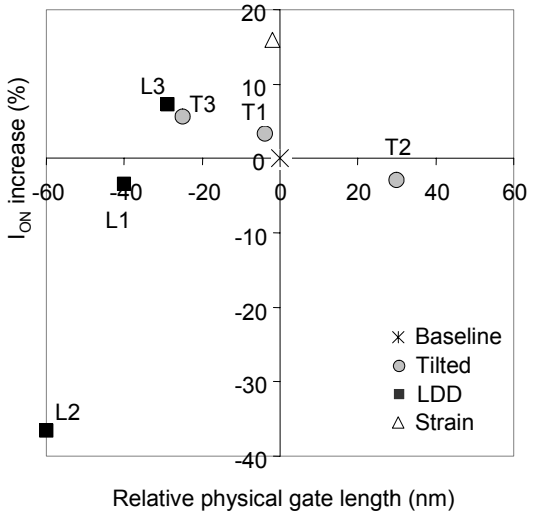

Figure 20. Experimental I_{ON} versus L_{PHYS} extracted at fixed I_{OFF} = 10^{-7} A/µm, normalized to the baseline performance.

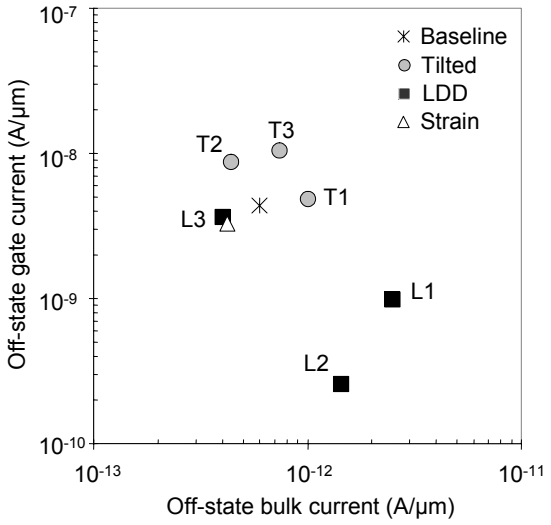

Figure 21. Experimental off-state gate leakage versus off-state bulk leakage for long channel devices (L_{PHYS} = 200 nm).

Conclusions

Through the initial work on fundamental diode analysis, insight and understanding was gained in the problem of MOS device junction leakage. Using the electrical behavior of fabricated diodes we validated our modeling methodology. Following that, innovative scaling solutions were proposed and realized in a silicon device experiment. Finally improved MOS transistor performance was demonstrated in terms of better SCE control without trading off leakage or drive behavior.

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