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Operation voltage and illumination intensity dependent space-charge limited current conductions in vertical organic phototransistors based on CuPc/C_{60} heterojunction and graphene

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ABSTRACT

For a trap-free single layer single carrier (hole-only or electron-only) organic device of thickness d, dielectric constant ε_r, and mobility μ, the relation of current density j with voltage V is described by the well-known Mott–Gurney equation, $j = 9\varepsilon_0\varepsilon_r\mu V^2/8d^3$, which can be rewritten as $\sqrt{j} = GV$, where $G = \sqrt{9\varepsilon_0\varepsilon_r\mu/8d^3}$ can be called space-charge limited (SCL) conductance. We investigated the current– voltage characteristics of vertical organic heterojunction phototransistors based on graphene as the source and C_{60}/copper phthalocyanine (CuPc) heterojunction as the photoactive layer. We found that the drain current vs drain voltage (I_d-V_d) characteristic is composed of two distinct SCL conductions with SCL-conductance being strongly dependent on the gate voltage and illumination intensity. At low gate voltages, the I_d-V_d curve can be divided into two sections of SCL current conduction with different SCL-conductance: the lower conductance in the lower drain voltage range and the higher conductance in the higher drain voltage range. Both low and high SCL-conductance increase with the gate voltage and illumination intensity. However, as the gate voltage increases to a certain threshold, the two SCL sections unify to only one with the conductance being between them. Our findings implicate that the current conduction of an ideal vertical organic phototransistor (VOPT), whose source/organic interface contact is Ohmic and organic semiconductor is trap free, can be well modeled by the SCL conduction theory with carrier density dependent mobility, which is strongly related to the gate voltage and illumination intensity, and that the mobility of VOPTs at a certain gate voltage can be extracted by the Mott–Gurney equation.

Organic phototransistors (OPTs) received great attention in recent years owing to their amplification capability for optical signals, noise reduction, and multiple functionalities.[1–3] In contrast to the conventional lateral structure OPTs, vertical organic phototransistors (VOPTs) stack the gate electrode, gate dielectric, source electrode, channel layer, and drain electrode vertically. In VOPTs, the charge carriers are transported in the vertical direction with the channel length equal to the thickness of the organic layer. In particular, due to small channel length, photogenerated excitons in VOPTs can be effectively separated and collected by source and drain electrodes resulting in efficient photoelectric conversion or fast response time.[4] At present, the cutting edge of VOPT research focuses on the preparation of source electrode films and organic material synthesis[5] for applications including but not limited to memory,[6] artificial synapses,[7,8] and arrays for image processing.[9] For example, patterned or structured conducting films,[10,11] metal nanowire films,[12,13] and graphene[14–17] are demonstrated as the source electrode for VOPTs. Among them, VOPTs based on graphene as the source electrode, termed as graphene based VOPTs hereafter, have arisen great interest due to fast charge transportation and inherent flexibility.[18–20] In graphene based VOPTs, the control of the gate voltage on the channel current conduction is manifested in two aspects. At first, the gate electric field partially penetrates into and through the graphene layer due to that graphene has a limited intrinsic dielectric constant of ~ 6.0[21] and controls the transport of charge carriers in the channel; second, as the work function of graphene can be tuned by the electric field due to limited density of states

(DOS),[22,23] the energy barrier at the graphene/organic interface can be effectively modulated by the gate electric field penetrating into the graphene,[24] thereby affecting the injection current from the graphene into the organic channel; for the case of Ohmic contact at the graphene/organic interface, the first one will become the dominant effect.

Space-charge limited (SCL) currents have played an important role in electronic devices, especially in solid-state electronic devices including organic electronic devices.[25] For an Ohmic contacted single carrier device of structure "metal/insulator/metal," the current density–voltage (J–V) characteristic is described by the Mott–Gurney equation[26]

$$j = \frac{9}{8}\varepsilon_0\varepsilon_r\mu\frac{V^2}{d^3}, \tag{1}$$

where ε_0 is the permittivity of vacuum and ε_r, μ, and d are the relative dielectric constant, carrier mobility, and the thickness of the organic layer, respectively. Equation (1) can be rewritten as $\sqrt{j} = GV$, where $G = \sqrt{9\varepsilon_0\varepsilon_r\mu/8d^3}$, which we call SCL-conductance. It is worth noting that the unit of SCL-conductance is $A^{1/2}\ m^{-1}\ V^{-1}$, which is different from that of common electric conductance.

It is known that for an ideal OPT of conventional lateral structure,[27] the output curves ($I_d \sim V_d$ dependences) can be expressed by the equation of the standard metal-oxide-semiconductor field effect transistor (FET) model,[28,29] and the linear region mobility can be extracted by the corresponding equation.[30] However, that equation is not valid for VOPTs. The question arising is what is the current conduction mechanisms and how to quantitatively describe the output characteristic curves of an ideal VOPT that has Ohmic contact at source/organic interface? In the present communication, we investigate the current conductions in graphene based VOPTs with C_{60}/copper phthalocyanine (CuPc) heterojunction as the photoactive layer and try to provide an answer for this question. We found that the drain current vs drain voltage (I_d-V_d) characteristic is composed of two distinct SCL conductions with SCL-conductance being strongly dependent on the gate voltage and illumination intensity. Moreover, the two SCL conductions unify to one at high gate voltages. The results implicate that the current conduction of an ideal VOPTs with Ohmic source/organic contact and trap free organic semiconductor can be well modeled by the SCL conduction theory with carrier density dependent mobility, which is strongly related to the gate voltage and illumination intensity.

The schematic structure of the VOPT is shown in Fig. 1, where n^+-Si/SiO_2 functions as the gate electrode and gate dielectric; graphene, C_{60}/CuPc bilayer, and Au are the source electrode, photoactive layer, and the semitransparent drain electrode, respectively. The device fabrication process is given in the supplementary material. Figures 2(a) and 2(c) show the output characteristics of the device in the dark and under light illumination with the intensity of 0.4 mW/cm^2, respectively. The transfer characteristics of the VOPT are shown in Fig. S2. In general, in the dark, the magnitude of drain current increases with drain voltage and gate voltage. Under light illumination, significant photocurrents are observed as shown in Fig. 2(b), demonstrating reasonable photodetection ability. The extracted photoresponsivity (R) and specific detectivity (D^*) show monotonic decreasing trends with increasing light intensity as displayed in Fig. S3 in the supplementary material.

In order to obtain further insight into the charge transport, $\sqrt{I_d} \sim V_d$ dependences in the dark for different gate voltages were plotted in Fig. 2(c). At lower gate voltages ($|V_g| \leq 80$ V), the $\sqrt{I_d} \sim V_d$ curves are folding lines with folding points at $|V_{tr}| = 2.1$ V.

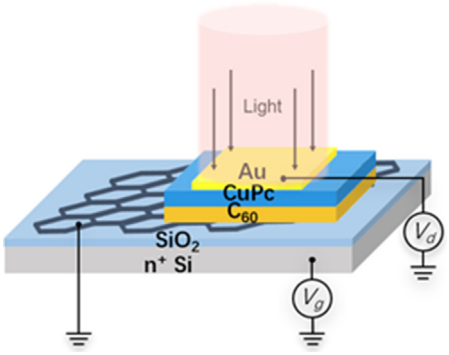

FIG. 1. Demonstration diagram of the VOPT structure.

According to Eq. (1), if $\sqrt{I_d} \sim V_d$ is a straight line, its slope is proportional to the square root of the mobility μ, from which the carrier mobility can be determined. As illustrated in Fig. 2(c), the current conduction of the device transits from a lower mobility state (1.104×10^{-6} cm^2/V·s) to a higher mobility state (6.616×10^{-6} cm^2/V·s) as V_d surpasses V_{tr}. With the gate voltage increasing, the slope of both line sections increases, indicating the increasing of carrier mobility with the gate voltage. For inorganic semiconductors, carrier mobility decreases generally with carrier concentration due to increased scattering.[31–33] Contrary to inorganic semiconductors, the increase in carrier mobility in organic semiconductors with carrier concentration was demonstrated both theoretically[34–36] and experimentally.[37] Therefore, the observed increase in carrier mobility with gate voltage is attributed to the increase in carrier concentration in VOPTs. As the gate voltage increases to a certain threshold ($|V_g| \sim 80$ V), a transition to a new conduction state occurs: the two sections unified to a new one with the SCL conductance being in the between of the two sections.

The observed SCL current conduction can be analyzed with the assistance of an energy level diagram of the device. At zero gate voltage, the work function of graphene is in a similar range to that of graphite, ~4.6 eV.[38–40] Considering that the LUMO and HOMO levels of C_{60} being 4.5 and 6.2 eV,[41] and that of CuPc being 3.5 and 5.2 eV, respectively,[42] the energy level diagrams for the charge transport in the device could be constructed as Fig. 3(a).

We first analyze the cases of low gate voltages. In this case, the work function of graphene is expected not far from 4.6 eV. Therefore, there is almost no energy barrier for electron injection at graphene/C_{60} interface considering the LUMO of C_{60} around ~4.5 eV. As Au/CuPc interface forming nearly Ohmic hole contact, therefore, at positive drain voltage bias, electrons will be injected into C_{60} from graphene, and holes into CuPc from Au free of energy barriers, resulting in SCL current conduction. This case is similar to that studied by Koehler and da Luz,[43] and the $j_d - V_d$ curve can be described by $\sqrt{j_d} = G_1 V_d$, with $G_1 = \sqrt{9\varepsilon_0\varepsilon_{r,CuPc}\mu_{p,eff1}/8d_{CuPc}^3}$, where $\mu_{p,eff} = \mu_{p,CuPc}/(1+\gamma)^2$ and $\gamma = \sqrt{\varepsilon_{r,CuPc}\mu_{p,CuPc}d_{C_{60}}^3/\varepsilon_{r,C_{60}}\mu_{n,C_{60}}d_{CuPc}^3}$. Considering that $d_{CuPc} = d_{C_{60}}$, $\varepsilon_{r,CuPc} = \sim 3$,[44] $\varepsilon_{r,C_{60}} =$ 3.33–3.63,[45] and $\mu_{p,CuPc} < \mu_{n,C_{60}}$, one has $\gamma > 1$, which indicates that $\mu_{p,eff} < \mu_{p,CuPc}$. When V_d further increases and surpasses V_{tr}, the applied voltage is mainly dropped on the CuPc layer as the conductance of the C_{60} layer is much larger than that of the CuPc layer. The larger conductance

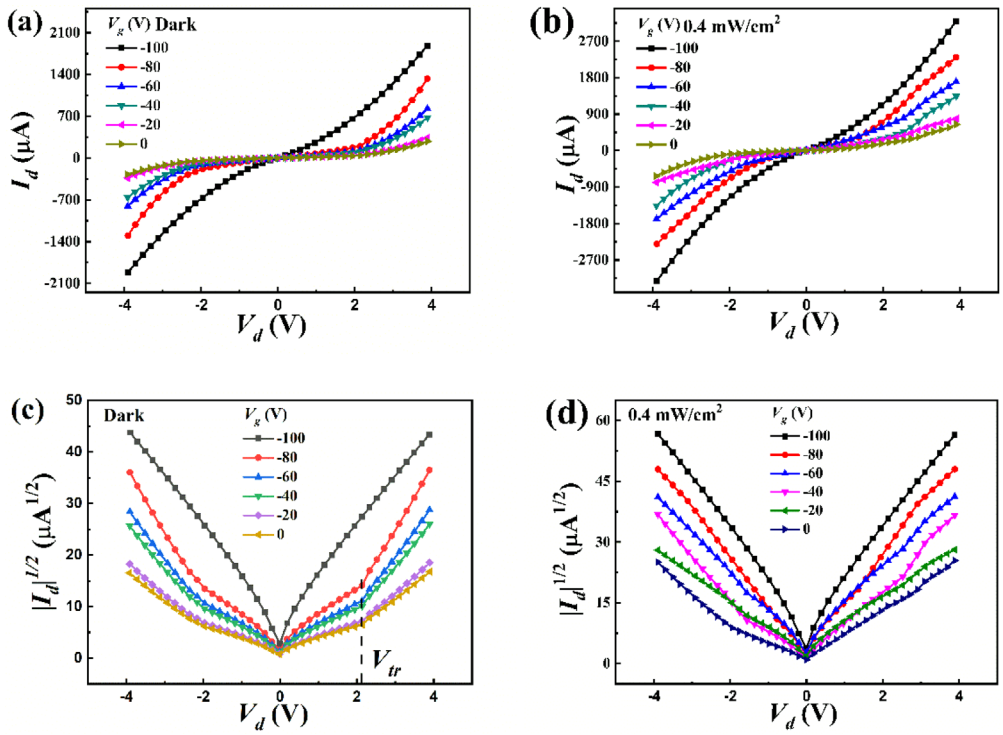

FIG. 2. The output characteristics of VOPT at various gate voltages (a) in the dark and (b) under illumination (power density = 0.4 mW/cm^2). The square root of drain current at various gate voltages (c) in the dark and (d) under illumination (power density = 0.4 mW/cm^2) at different gate voltages.

of C_{60} is mainly due to the large electron concentration of C_{60}. Therefore, the SCL-conductance of section 2, G_2, is described by $G_2 = \sqrt{9\varepsilon_0\varepsilon_{r,CuPc}\mu_{p,CuPc}/8d^3_{CuPc}}$. Because of $\mu_{p,CuPc} > \mu_{p,eff}$, therefore, one has $G_2 > G_1$, that is, the slope of section 2 is larger than that of section 1.

At high gate voltages, the work function of graphene reaches a level that is so high that almost no electrons can be injected into the C_{60} layer. Therefore, the current in the C_{60} layer is hole-only SCL transport with a characteristic SCL conductance of $G_{SCL3} = \sqrt{\varepsilon_{r,C_{60}}\mu_{p,C_{60}}/d^3_{C_{60}}}$. Because $\mu_{p,eff} < \mu_{p,C_{60}} < \mu_{p,CuPc}$, therefore $G_1 < G_3 < G_2$, that is, the slope of the red imaginary line 3 is less than green line 2 while larger than that of blue line 1 [Fig. 3(b)].

A quantitative modeling of the device will be helpful for a comprehensive understanding of the curves in Fig. 2, which is certainly beyond the scope of the present paper. Hence, in order to get deeper understanding, we fabricated a simplified device of the structure "p$^+$-Si/SiO$_2$/graphene/CuPc (50 nm)/Au" and developed a model for this simplified device based on carrier concentration dependent mobility. Considering that a negative gate voltage will induce accumulation of holes in CuPc, greatly enhancing the hole concentration, which results in increase in carrier mobility. Assuming Gauss distribution of transport density of states (DOS), the mobility can be expressed as[34]

$$\mu(p) = \mu_0 \exp\left[\frac{1}{2}(s^2 - s)\left(\frac{2p}{N_{DOS}}\right)^{\delta}\right], \quad (2)$$

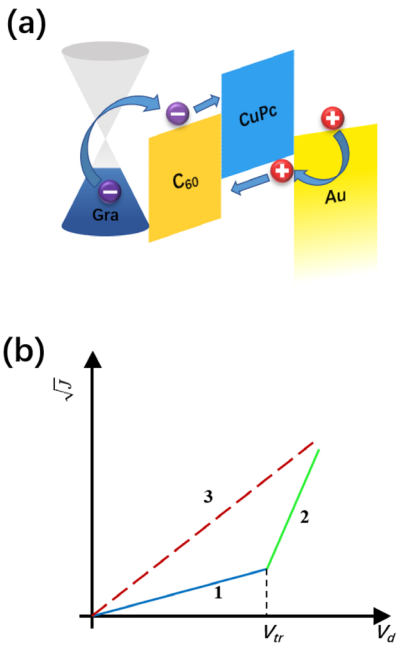

FIG. 3. $\sqrt{J} \sim V_d$ characteristic of the device and schematic energy level diagram in the case of positive drain voltage. (a) Photo-excitons generation and dissociation, charge injection, transport, and accumulation under on state, and (b) the slope of different drain voltages.

$$\delta = 2\frac{\ln(s^2 - s) - \ln(\ln 4)}{s^2}, \tag{3}$$

where μ_0 is the mobility prefactor that equals the carrier mobility at zero carrier density and $s = \sigma/(k_BT)$ is the reduced Gauss width; σ, k_B, and T are the width of Gauss DOS, Boltzmann constant, and temperature, respectively. N_{DOS} and p are the total DOS and average hole density in the organic semiconductor, respectively. The injection from the source electrode and induction by the gate voltage are the two contributions to the hole density in the channel. Assuming the later being the dominant one and proportional to the gate voltage (V_g), then the hole concentration p can be expressed as

$$p = p_d + \frac{k_p c_i}{qd} V_g, \tag{4}$$

where k_p, c_i, q, and d are dimensionless proportional coefficient, capacitor per unit area, elementary charge, and CuPc layer thickness, respectively. p_d is a gate voltage independent constant. Substituting Eqs. (2)–(4) into Eq. (1), the measured $j^{0.5} \sim V_d$ curves can be simulated with parameters summarized in Table I. In Fig. 4, the simulated $j^{0.5} \sim V_d$ curves are compared with the experimental one (symbols), demonstrating excellent agreement with each other except in the region with low drain voltages of $|V_d| < 1$ V.

The SCL conductance increases with illumination and tends to saturate at high intensities, as shown in Fig. 5. As the photocurrent is proportional to the product of the exciton density and exciton dissociation probability that increases sharply with the local electric field,[48] the observed slow increase in photocurrent at high light intensities as shown in the inset of Fig. 5(a) may originate from the exciton annihilation by interactions between excitons and charges;[49] the reduced exciton dissociation probability due to the reduced local electric field resulted from the photoholes accumulated there, and we thought the latter being the dominant one. As schematically shown in Fig. 6, the photogenerated electrons in C_{60} quickly drift toward the source, while the photoholes in CuPc slowly drift and diffusion toward the drain. Due to the fact that the hole mobility of CuPc is much lower than the electron mobility of C_{60}, the photoholes accumulate near the position where the exciton dissociation occurs, which weakens the electric field there. Therefore, the higher the light intensity, the weaker the electric field, and the smaller the exciton dissociation probability, thus resulting in slowly increase and even saturation of photocurrent with increasing illumination intensity.

In conclusion, we observed SCL conductions in graphene based VOPTs with a C_{60}/CuPc heterojunction as the photoactive

TABLE I. Parameters used for the fitting lines in Fig. 4.

Parameter	Symbol	Numerical value	Reference
Relative dielectric constant	ε_r	3.0	44
Total DOS	N_{DOS}	2.50×10^{19} cm^{-3}	46
Width of Gauss DOS	σ	0.20 eV	47
Proportional coefficient	k_p	2.60×10^{-5}	Fitting
Mobility prefactor	μ_0	8.35×10^{-9} cm^2/V·s	Fitting
Capacitor per unit area	c_i	3.19 nF/cm	···
Film thickness	d	75 nm	···

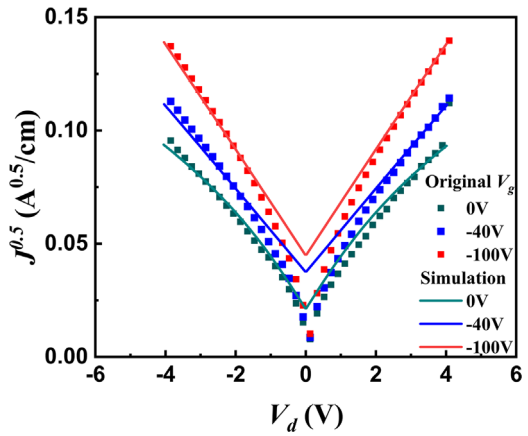

FIG. 4. The measured (filled squares) $j^{0.5} \sim V_d$ curves of the device p$^+$-Si/SiO$_2$/graphene/CuPc (50 nm)/Au at different gate voltages and the simulation with fitting parameters of $\mu_0 = 8.35 \times 10^{-9}$ cm^2/V·s and $k_p = 2.60 \times 10^{-5}$.

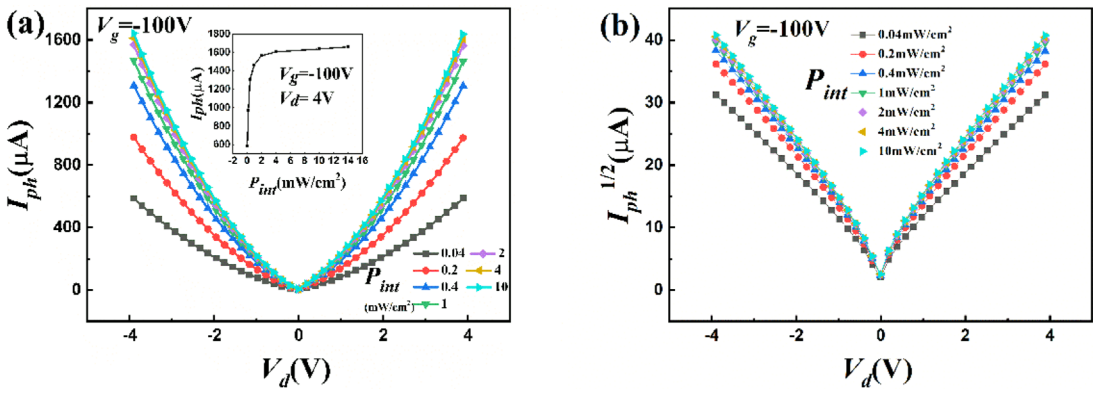

FIG. 5. (a) The photocurrent and (b) the square root of photocurrent of the VOPT were measured under V_d bias of −4–4 V and under an illumination of wavelength of 650 nm at different P_{int} at gate voltage (V_g) of −100 V. In (a), the inset shows an $I_{ph} - P_{int}$ curve of the VOPT at gate voltage (V_g) of −100 V and drain voltage (V_d) of 4 V.

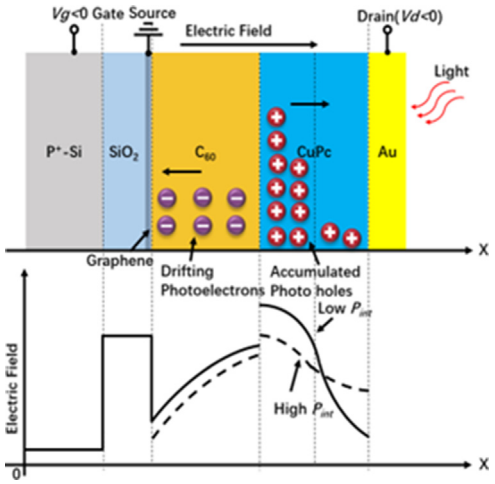

FIG. 6. Schematic expression of reduction of the electric field due to the accumulation of slowly moving photogenerated electrons.

layer. In the dark and at low gate voltages, a full *I*–*V* curve can be perfectly described by two SCL conductions of different conductance: the lower conductance in the low drain voltage range, and the higher conductance in the higher drain voltage range. However, at high gate voltages, the full *I*–*V* curve is described by only one SCL conduction with conductance being in between the two under low gate voltages. For both cases, the conductance increases with illumination intensity. Our findings have two implications regarding to conduction mechanism and device characterization: (1) different from the current conduction in ideal lateral OPTs, which is expressed by the equation of the standard metal-oxide-semiconductor FET model, the current conduction of an ideal VOPT, whose source/organic interface contact is Ohmic, and the organic semiconductor being trap free can be well modeled by SCL conduction theory with carrier density dependent channel mobility, which is strongly related to the gate voltage and illumination intensity; (2) the mobility of an ideal VOPT at a certain gate voltage could be extracted by Eq. (1) and the gate voltage dependent mobility from Eqs. (2)–(4), instead of the equations usually used by lateral OPTs, which are derived from the standard metal-oxide-semiconductor FET model.

See the supplementary material for additional data, materials, and optoelectronic measurement about the device.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Gang Hu: Data curation (lead); Writing – original draft (lead). **Grégory F. Schneider:** Resources (supporting). **Huabiao Zhu:** Investigation (supporting). **Qinyong Dai:** Investigation (supporting). **Chaoqun Jiang:** Supervision (supporting). **Yingquan Peng:** Writing – review & editing (supporting). **Wenli Lv:** Resources (equal); Supervision (equal); Writing – review & editing (supporting). **Sunan Xu:** Resources (supporting). **Lei Sun:** Resources (supporting). **Lin Jiang:** Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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