Differential ultra low noise amplifier for low frequency noise measurements

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Almost all low noise voltage preamplifier suitable for application in the field of Low Frequency Noise Measurements (either commercially available or proposed in the literature) are single ended input amplifiers. This means that one end of the measuring port of the Device Under Test (DUT) must be connected to common ground. This may be a severe limitation in many interesting measurement configurations, such as the case in which Kelvin connections to the DUT must be employed. In this paper we propose a simple design of a fully differential input ultra low noise amplifier with noise performances, in term of equivalent input voltage noise, comparable to those of the best single ended input amplifiers for low frequency noise measurements reported in the literature. Indeed, the amplifier we propose is characterized by a voltage gain of 80 dB, in the bandwidth from a few tens of mHz up to a few kHz, and by an equivalent input voltage noise as low as 14 nV/$\sqrt{}$Hz (100 mHz), 2 nV/$\sqrt{}$Hz (1 Hz), 1.2 nV/$\sqrt{}$Hz (10 Hz) and 1 nV/$\sqrt{}$Hz (1 kHz). Such an amplifier can also be employed as a single ended input amplifier by simply shorting to ground one of the two differential input ports. [doi:10.1063/1.3605716]

I. INTRODUCTION

The study of the quality and the reliability of semiconductor materials and devices is a crucial aspect of microelectronics. Among the several techniques that are employed within this context it is generally recognized that Low Frequency Noise Measurements (LFNM) is among the most sensitive tools that are available for the investigation of almost all the degradation mechanisms affecting passive and active integrated devices.[1–3] Apart from the applications in the field of reliability, noise measurements can be useful for the investigation of the conduction mechanisms in advanced devices.[4] Noise measurements can also be used for the design of primary thermometers (Johnson Noise Thermometry)[5] or for developing advanced sensing techniques (Noise Enhanced Sensing).[6] However, because of the extremely low levels of voltage or current fluctuations that have to be detected, performing sensible noise measurements, especially at very low frequencies ($f<1$ Hz), often results in a quite challenging task. Indeed, in every low frequency noise measurement system several sources of noise and disturbances are present that contribute to set the lowest detectable noise level at any given frequency. Such sources of disturbances may be classified as external, that is disturbances caused by interferences from the environment, and internal, that is those due to the noise introduced by the very instrumentation employed for setting up the noise measurement chain. Since external interferences can be completely eliminated, at least in principle, by resorting to proper shielding, the residual background noise of the system is set by noise introduced by the device biasing system and the low noise preamplifier coupled to the Device Under Test (DUT). The noise contribution of the bias network can be made negligible by using high capacity batteries as power supply. In this situation, the ultimate sensitivity of the noise measurement system is set by the equivalent input voltage and current noise sources of the preamplifiers. The availability of preamplifier with very low equivalent input noise is therefore a crucial requirement in any low frequency noise measurement system. Notwithstanding this, particularly in the field of low frequency noise voltage measurements,

no significant improvement have been observed in commercial instrumentation over the past years and indeed relatively old pieces of instrumentation, such as the SR560 by Stanford Research or the EG&G PAR113 are still the preferred choice for many research groups interested in the application of low frequency noise measurements.[7–9] Typical values of the SR560 equivalent input voltage noise are 300, 40 and 13 nV/$\sqrt{}$Hz at f=100 mHz, 1 Hz and 10 Hz respectively, and for the EG&G PAR113 130, 40 and 18 nV/$\sqrt{}$Hz at the same frequencies. Much better noise performances can be obtained with purposely designed preamplifiers,[10–12] an still, possibly because of the complexity of their design, they are often employed only by the very research group that have developed them. In an attempt to remove this obstacle, we have recently proposed a new ultra low noise voltage preamplifier that is characterized, at the same time, by excellent noise performances and by an extremely simple design.[13] Most of the design that have been proposed in the literature, including our own, are however characterized by a single ended input port. This fact implies that voltage noise measurements can only be performed between one node and the common ground of the system, if a single supply system is employed for biasing both the DUT and the amplifier. If independent batteries for biasing the device and the amplifier are employed, noise measurements across the voltages terminations of a DUT provided with Kelvin connections[14–16] can be performed. It is however obvious that the availability of a differential input preamplifier would greatly simplify the measurement set up as, among other advantages, it would not be necessary to employ a different set of batteries for the biasing circuit and for the preamplifier. Finally, there are cases in which the availability of differential input preamplifiers would allow measuring configurations that would be otherwise extremely difficult, if not impossible, to achieve. Suppose, with reference to Fig. 1, that a DUT supplied by a constant current be placed some distance away from the noise measurement amplifiers. This might be due, for instance, to the fact that the sample must be maintained at cryogenic temperature while the noise preamplifier must operate at room temperature. Suppose, moreover, that the wires used for connecting the DUT to the noise preamplifier are characterized by a not negligible resistance. By using a single pair of wires, the noise introduced by the wires (because of the wire resistance) would be indistinguishable from the noise produced by the DUT. If a pair of differential input low noise amplifiers is available, than two pair of wires can be used for connecting the ends of the DUT to each one of the two differential inputs of the amplifiers. In this way, by performing cross correlation at the outputs of the amplifier, the noise introduced by the wires can be completely eliminated. Moreover, both the two amplifiers and the biasing circuit could be supplied by a single set of batteries, thus considerably reducing the size of the entire system. In view of all these potential advantages, we have specifically addressed the problem of the design of a differential input ultra low noise amplifier. The target of the design was that of obtaining an equivalent input noise comparable to that of a single ended amplifier with a reduced circuit complexity.

II. DIFFERENTIAL INPUT LOW NOISE AMPLIFIER

The schematic of the proposed differential input low noise amplifier is shown in Fig. 2. The complete component list, together with their relevant characteristics, is reported in Table I. The amplifier consists of two cascaded gain stages. The first stage is a fully differential amplifier with a differential voltage gain of 100. The second stage receives as input the differential output of the first stage and produces a single ended output with an additional gain of 100. In this way, the resulting overall differential gain is 80 dB. Because of the symmetry in the design, in the following we will employ the subscript x when we will make reference to a component that is present, with the same value, in both the left and the right section of the circuit. Therefore, for instance, R_{1x} will be used in order to make reference to either R_{1L} or R_{1R}. The second stage consists of an AC coupled (C_O, R_O) low input bias current instrumentation amplifier (INA 131 by Texas Instruments) with a fixed gain of 100. This stage has the role of rising the level of the signal prior to digitization for spectral analysis. The high pass filters at its input are characterized by a low corner frequency of about 24 mHz and provide for removing the large DC offset at the output of the first stage that, as we shall discuss in the following, is the result of the large input offset introduced by the discrete JFET differential amplifier. The selection of the values for C_O and R_O, is relevant as far as the contribution of the equivalent input current noise source of $IA3$ to the total noise is concerned, as it will be discussed in more detail at a

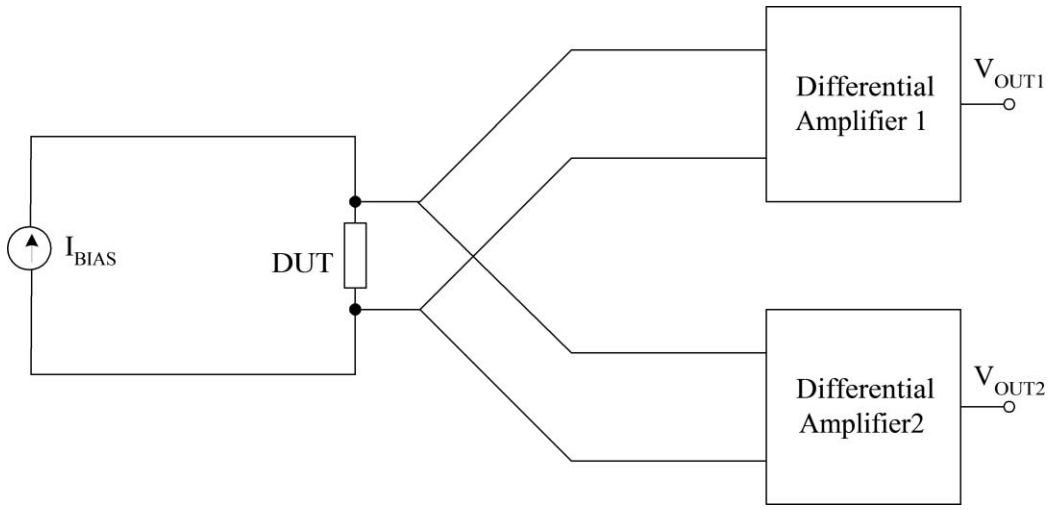

FIG. 1. Measurement configuration employing two differential amplifiers for rejecting cable noise by means of cross-correlation.

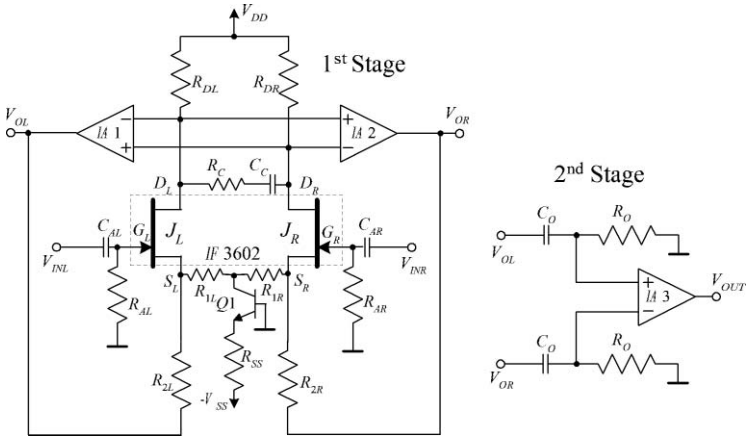

FIG. 2. Complete schematic of the proposed differential low noise voltage amplifier. Component type and values are reported in Table I. V_{DD} and V_{SS} are 12 V (lead acid batteries).

later time. As far as the contribution of the equivalent input voltage sources of *IA*3 to the equivalent input noise of the entire amplifier is concerned, because of the large gain of the first stage (40 dB), we can easily verify that it is negligible. Indeed, the power spectrum of the Equivalent Input Voltage Noise (EIVN) of *IA*3 is about 30 nV/$\sqrt{}$Hz at f=1 Hz and 12 nV/$\sqrt{}$Hz for f>30 Hz. Therefore, taking into account the gain of the first stage, the contribution to the EIVN of the entire amplifier is in the order of 300 pV/$\sqrt{}$Hz and 120 pV/$\sqrt{}$Hz at f=1 Hz and for f>30 Hz, respectively. In order to obtain a very low EIVN for the first stage, we resort to the very large area JFET transistors pair IF3602 by Interfet as the first stage of an AC coupled differential input-differential output voltage amplifier. A gain of 100 is set, as it will be shown in the following, by the ratio R_{2x}/R_{1x}. The JFETs IF3602 are characterized by a very low EIVN (0.4 nV/$\sqrt{}$Hz and below 0.3 nV/$\sqrt{}$Hz at f=10 Hz and for f>100 Hz, respectively, according to the manufacturer datasheet) and a high transconductance gain (g_m=70 mA/V for a drain current I_D=4 mA). Typical pinch off voltages for the IF3602 fall in the range between -1.5 V and -0.5 V and the reverse gate current in the active region of operation at room temperature is below 10 pA provided that the drain to source voltage is maintained below 4 V. We will start the analysis of the circuit in Fig. 2 by discussing the polarization of the JFETs. In ideal conditions (perfect symmetry between the JFETs) and in the absence of any signal at the inputs of the amplifier, the output voltages V_{Ox} are 0 and, therefore, the current I_{Dx} biasing each JFET can be

TABLE I. Component list for the circuit in Fig. 2

Component	Component type	Component value
J_L,J_R	Low noise JFET differential pair	Interfet IF3602
IAx	Instrumentation Amplifier	INA131 (Gain=100)
R_{1L}, R_{1R}	0.1%, 1/4 W, Wirewound	10 Ω
R_{2L}, R_{2R}	0.1%, 1/4 W, Wirewound	1 kΩ
R_{DL},R_{DR}	5 × 10 kΩ, 0.1%, 1/8 W, in parallel, metallic film	2 kΩ
R_{SS}	metallic film	1.5 kΩ
R_{Ax},R_O	—	3.3 MΩ, 680 kΩ
C_{Ax},C_O	Polyester	22 μF, 10 μF
$Q1$	Bipolar Transistor	2N1711
R_C,C_C	—	68 Ω, 33 nF

calculated as follows:

$$I_{Dx} = \frac{I_C}{2} - \frac{V_{GSx}}{R_{2x}}; I_C = \frac{V_{SS} - V_{BE}}{R_{SS}} \tag{1}$$

where I_C is the collector current of Q1. With R_{SS}=1.5 kΩ, V_{SS}=V_{DD}=12 V, R_{2x}=1 kΩ, V_{BE}≈ 0.7 V and assuming a typical V_{GS} value of about -1 V, we can estimate a biasing current I_{Dx} of about 4.5 mA. With this biasing current, the JFETs drain voltage is about 3 V (V_{DS}≈2 V). When we take into consideration the JFET pair offset that, according to the manufacturer, may be in the order of a few tens of mV (with a maximum of 100 mV), the DC bias feedback from the outputs V_{Ox} to the sources of the JFETs provides for offset compensation. The differential feedback loop is designed in order to maintain the drain voltages quite close to one another, so that I_{DL}≈I_{DR} even in the presence of large offsets. Indeed, let us assume that I_{DL}≈I_{DR} can be obtained with V_{GSL}=V_{GS}+ΔV_{GS} and V_{GSR}=V_{GS}-ΔV_{GS}. Since, as far as the calculation of the bias point is concerned, we may assume V_{GL}=V_{GR}=0, this means that the values of V_{SL} and V_{SR} should be changed, with respect to the ideal value in the case of symmetrical JFETs, by -ΔV_{GS} and ΔV_{GS}, respectively. We can now refer to the equivalent small signal circuit in Fig. 3 in order to evaluate the voltage changes ΔV_{OL} and ΔV_{OR} that are needed in order to obtain ΔV_{SL}=- ΔV_{SR}=-ΔV_{GS}. Since:

$$\Delta V_{SL} = \Delta V_{OL} \frac{R_{1L} || (1/g_m)}{R_{2L} + R_{1L} || (1/g_m)}; \Delta V_{SR} = \Delta V_{OR} \frac{R_{1R} || (1/g_m)}{R_{2R} + R_{1R} || (1/g_m)} \tag{2}$$

and since R_{1x}=10 Ω and, for bias currents in the order of 4-5 mA, the transconductance g_m of the IF3602 is in the order of 70 mA/V, it can be easily estimated that the maximum required offset (100 mV=|ΔV_{SL}- ΔV_{SR}|) can be compensated with |ΔV_{OL}|=|ΔV_{OR}|≈ 8 V, which is well within the output voltage range (±10 V) of the INA131 instrumentation amplifiers *IA*1 e *IA*2. Even with such large V_{Ox} values, the difference |V_{DL}-V_{DR}| between the drains of the JFETs would be of just 80 mV (|ΔV_{OL}|/G, G=100 being the gain of *IA*1 and *IA*2), thus confirming the initial assumption of operating with I_{DL}≈I_{DR} even in the presence of the largest possible offset between the JFETs. Note that, as it will be shown in the following, the ratio R_{2x}/R_{1x} sets the differential gain of the first stage. With R_{2x}=1 kΩ and R_{1x}=10Ω we obtain a gain of 100. A larger gain could be desirable for reducing the noise contribution of the following stage. However, because of the constraints outlined above, a larger R_{2x}/R_{1x} ratio would not insure that offset compensation be achieved with *IA*1 and *IA*2 remaining in the linear region of operation. It will also be shown that at frequencies above a few Hz, the most important noise contribution, besides that due to the equivalent input voltage noise of the JFETs, comes from the resistances R_{1x}. Once again, the offset compensation network poses a limit to the lowest value of R_{1x}. Indeed, the current that can be output by *IA*1 and *IA*2 is limited to about 10 mA, and therefore, with lower values for R_{1x} (for the same ratio R_{2x}/R_{1x}) we would risk of overcoming the maximum output current limitations of the INA131 in the case of large offset JFETs.

As far as the discussion of the gain and the noise of the first stage is concerned, we may refer to the small signal equivalent circuit in Fig. 4. In order to simplify the discussion, in Fig. 4 we assume

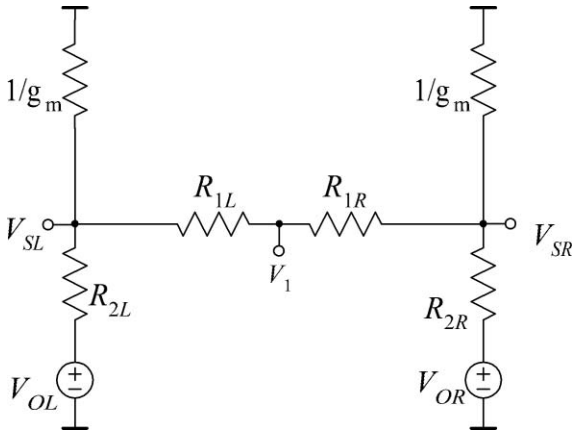

FIG. 3. Equivalent circuit of the first stage for offset modeling and compensation.

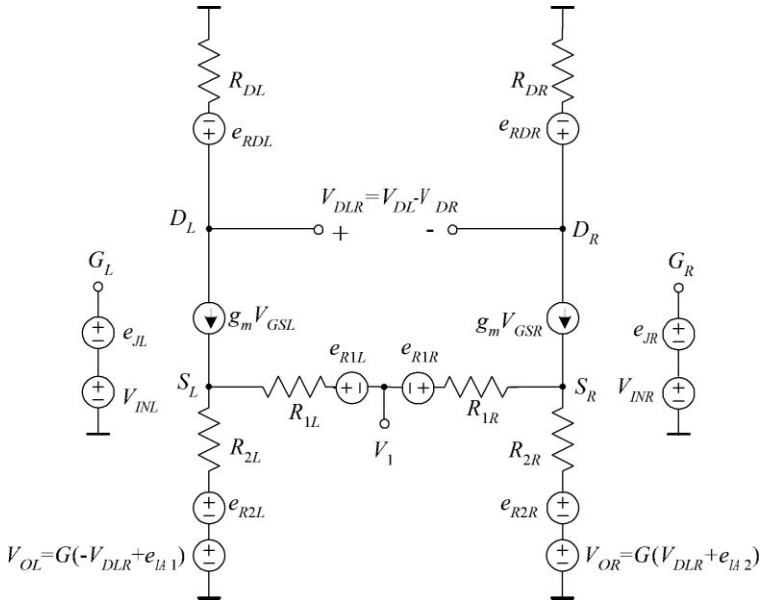

FIG. 4. Small signal equivalent circuit of the first stage for gain and noise calculation.

that, in the low to medium frequencies range, we can neglect the effect of the input high pass filters C_{Ax}-R_{Ax} and the effect of the series $R_C C_C$ that is used for frequency compensation. The role and the effects of these components on the performances of the amplifier will be however discussed in the following.

All the noise sources in Fig. 4 are assumed to be uncorrelated. The noise sources e_{Rx} represent the noise produced by each resistance R_x. The noise sources e_{IAx} represent the equivalent input noise sources of IAx. The effect of the equivalent input current noise sources of the instrumentation amplifiers is assumed to be negligible because of the relatively low value of the source impedance (in the order of R_{Dx} for both $IA1$ and $IA2$). Finally, e_{Jx} represent the equivalent input voltage noise sources of the JFETs. The effect of the instrumentation amplifiers $IA1$ and $IA2$ is completely accounted for by means of the two voltage controlled voltage sources V_{Ox} at the bottom of the drawing in Fig. 4. It must be noted that the INA131 are characterized by a bandwidth of about 70 kHz, and therefore the gain G should actually be written as:

$$G = G_0 \frac{1}{1 + s\tau_{PINA}}; \quad G_0 = 100; \frac{1}{2\pi\,\tau_{PINA}} = 70\ \text{kHz} \tag{3}$$

We can write the differential voltage V_{DLR}=V_{DL}-V_{DR} as follows:

$$V_{DLR} = V_{DL} - V_{DR} = e_{RDL} - e_{RDR} - g_m R_D (V_{GL} - V_{GR}) + g_m R_D (V_{SL} - V_{SR}) \tag{4}$$

with

$$(V_{GL} - V_{GR}) = V_{INL} - V_{INR} + e_{JL} - e_{JR} \quad R_D = R_{DL} = R_{DR} \tag{5}$$

From the equilibrium at nodes S_L and S_R (1st KCL) we have:

$$\begin{aligned} \frac{G(V_{DR} - V_{DL} + e_{IA1}) + e_{R2L} - V_{SL}}{R_2} &= \frac{V_{SL} - e_{R1L} - V_1}{R_1} - g_m (V_{GL} - V_{SL}) \\ \frac{G(V_{DL} - V_{DR} + e_{IA2}) + e_{R2R} - V_{SR}}{R_2} &= \frac{V_{SR} - e_{R1R} - V_1}{R_1} - g_m (V_{GR} - V_{SR}) \end{aligned} \tag{6}$$

with R_1=R_{1L}=R_{1R} and R_2=R_{2R}=R_{2L}.

From (6) the expression of the difference V_{SL}-V_{SR} can be obtained (the contribution of the voltage V_1 cancels out):

$$\begin{aligned} &V_{SL} - V_{SR} \\ &= \frac{G[-2(V_{DL} - V_{DR}) + e_{IA1} - e_{IA2}] + e_{R2L} - e_{R2R} + \frac{R_{2x}}{R_{1x}}(e_{R1L} - e_{R1R}) + g_m R_{2x}(V_{GL} - V_{GR})}{1 + \frac{R_{2x}}{R_{1x}} + g_m R_{2x}} \end{aligned} \tag{7}$$

Substituting (7) in (4), the expression of the differential voltage V_{DLR}=V_{DL}-V_{DR} as a function of the noise sources and of the gate voltages V_{GL} and V_{GR} can be obtained.

The equivalent circuit in Fig.4 and the equations derived so far can be employed for estimating the differential loop gain T_D of the system, by calculating the differential voltage V_{DLR} across the drains of the JFET in the hypothesis that an independent differential source V_P is used instead of V_{DLR} in the expression of the voltage sources V_{OL} and V_{OR}. With only V_P active, we have:

$$T_D = \frac{V_{DLR}}{V_P} = -\frac{2 g_m R_D G}{1 + \frac{R_2}{R_1} + g_m R_2} = T_{D0} \frac{1}{1 + s\tau_{PINA}} \tag{8}$$

Using the values of the component list reported in Table I and with g_m=70 mA/V we can estimate $|T_{D0}|$ to be in the order of 165. In (8) we have not taken into account the presence of parasitic capacitances that introduce other poles in the loop gain. Indeed, without proper compensation, the system would not be stable, as confirmed by SPICE simulations. In order to obtain stability, we employ the series $R_C C_C$ for obtaining a pole-zero compensation. The frequency of the zero is chosen equal to that of the pole of the INA131, while the pole frequency f_{pc} is set to about 1.2 kHz ($\tau_{pc} \approx 2 C_C R_D$=132 μs). The actual expression of the open loop gain T_{DC} with compensation is therefore:

$$T_{DC} = T_{D0} \frac{1}{1 + s\tau_{PINA}} \times \frac{1 + s\tau_{PINA}}{1 + s\tau_{PC}} = T_{D0} \frac{1}{1 + s\tau_{PC}} \tag{9}$$

The frequency at which $|T_{DC}|$ is close to 0 dB provides us with an estimate of the bandwidth of the system, that, in our case, is in excess of 10 kHz, more than sufficient for low frequency noise measurements applications. In the following, in order not to complicate the discussion and unless otherwise noted, we will assume that we are working at frequencies much lower than the bandwidth limit of the system, so that we can assume G=G_0, T_{DC}=T_{D0} and we can neglect the presence of the compensation network ($R_C C_C$) as far as the noise analysis is concerned. However, as we shall discuss in the following, we will need to take into account the effect of the compensation in order to correctly evaluate the noise contribution of *IA*1 and *IA*2 at frequencies near and above 1 kHz.

In order to evaluate the differential gain with respect to the differential input, let us assume that all noise sources be 0 in Fig.4. In this situation, with $Vd = V_{GL}$-V_{GR}, we have:

$$\frac{V_{DLR}}{V_d} = A_{DLR} = \frac{-g_m R_D \left(1 + \frac{R_2}{R_1}\right)}{1 + \frac{R_2}{R_1} + g_m R_2 + 2G g_m R_D} = -\frac{-T_{D0}}{1 - T_{D0}} \frac{1 + \frac{R_2}{R_1}}{2G} \approx -\frac{1 + \frac{R_2}{R_1}}{2G} \tag{10}$$

since $|T_{D0}| >> 1$.

The differential gain V_{OX}/V_d at the output of $IA1$ and $IA2$ is therefore:

$$\frac{V_{OL}}{V_d} = -\frac{V_{OR}}{V_d} = -G\frac{V_{DLR}}{V_d} = \frac{1 + \frac{R_2}{R_1}}{2} \approx 50 \tag{11}$$

The total differential gain of the first stage A_{DO1}=(V_{OL}-V_{OR})/V_d=V_{O1D}/V_d is therefore two times that reported in (11) and is very close to R_2/R_1=100.

In order to estimate the equivalent input differential voltage noise spectrum of the first stage we can employ (4) and (7) for calculating the total noise at the output V_{DLR} in the hypothesis of uncorrelated noise sources in Fig.4 and then divide the obtained power spectrum by the gain A_{DLR} squared. Note, however, that the calculation of the contribution by the equivalent input voltage noise of the instrumentation amplifiers will require a different approach. We can simplify the calculation by taking into consideration a few noise sources at the time. We will start with contribution $S^J{}_{in}$ of the JFET equivalent input noise sources e_{JL} and e_{JR} to the equivalent input noise. This calculation is readily done since the voltage difference e_{JL}-e_{JR} has obviously the same effect of a differential voltage at the input of the amplifier. Therefore we have:

$$S^J_{in} = S_{eJL} + S_{eJR} = 2S_{enJ} \tag{12}$$

where S_{enJ} is the power spectrum of the equivalent input voltage noise source of each JFET.

As far as the contribution $S^{RD}{}_{in}$ due to the resistances R_{Dx} (that is with e_{RDL} and e_{RDR} "on" and all other sources "off") we have:

$$S^{RD}_{in} = (S_{eRDL} + S_{eRDL}) \frac{1}{(1 - T_{D0})^2} \left(\frac{2G}{1 + \frac{R_2}{R_1}}\right)^2 \tag{13}$$

Since:

$$G \approx 1 + \frac{R_2}{R_1}; S_{eRDL} = S_{eRDR} = 4KTR_D; |T_{D0}| >> 1 \tag{14}$$

we have:

$$S^{RD}_{in} = 2\frac{4KTR_D}{(T_{D0})^2} \approx 7 \times 10^{-5} \times 4KTR_D \approx 2.4 \times 10^{-21} \mathrm{V^2/Hz} = 50\ \mathrm{pV}/\sqrt{\mathrm{Hz}} \tag{15}$$

We can therefore conclude that the contribution of the noise introduced by the resistances R_{Dx} is negligible with respect to the noise introduced by the JFETs.

Let us now take into consideration the effect of the noise introduced by the resistances R_{1x} and R_{2x}. With the very same approximations used so far we obtain, for the contribution $S^{R12}{}_{in}$ to the equivalent input voltage noise spectrum:

$$S^{R12}_{in} = 2 \times \left(4KTR_1 + 4KTR_2\frac{R_1^2}{R_2^2}\right) \approx 8KTR_1 = 0.33 \times 10^{-18} \mathrm{V^2/Hz} \approx 0.6\ \mathrm{nV}/\sqrt{\mathrm{Hz}} \tag{16}$$

Finally, we must take into consideration the contribution of the equivalent input voltage noise sources of the instrumentation amplifiers. In this case, it must be noted that at the (differential) output of the first stage we have:

$$V_{OL} - V_{OR} = G\left(-2V_{DLR} + e_{IA1} - e_{IA2}\right) \tag{17}$$

In the case in which only e_{IA1} and e_{IA2} are active, from (4) and (7) we have:

$$V_{DLR} = \frac{-T_{D0}}{1 - T_{D0}} \frac{e_{IA1} - e_{IA2}}{2} \tag{18}$$

and, when substituting in (17):

$$V_{OL} - V_{OR} = \frac{G}{1 - T_{D0}} (e_{IA1} - e_{IA2}) \tag{19}$$

Therefore, for the contribution to the equivalent input noise spectrum, we have:

$$S_{in}^{IA} = \frac{1}{\left(1 + \frac{R_2}{R_1}\right)^2} \frac{|G|^2}{|1 - T_{D0}|^2} 2S_{INA} \approx 7 \times 10^{-5} S_{INA} (f << f_{pc}) \tag{20}$$

At frequencies well below f_{pc} it can be easily demonstrated that the contribution of the instrumentation amplifiers to the equivalent input noise of the amplifier is negligible with respect to the noise introduced by the JFETs and by the resistances R_{1x}. For instance, at f=100 Hz the spectrum of the equivalent input voltage source of the INA131 is S_{INA}=144×10^{-18} V^2/Hz, corresponding to $S^{IA}{}_{in}$=11×10^{-21} V^2/Hz, while we have $S^{R12}{}_{in}$=330×10^{-21} V^2/Hz. However, as we approach and overcome the pole frequency of T_D, the expression (20) is no longer correct and the complete expression (8) should be used. Indeed, at frequencies above f_{pc}, the contribution $S^{IA}{}_{in}$, because of the frequency dependence of T_D, increases proportionally to f^2. For instance, at 10 kHz (still within the bandwidth of the amplifier) $S^{IA}{}_{in}$ is about 0.8×10^{-18} V^2/Hz, thus becoming the most important noise contribution to the background noise of the system.

We can summarize the discussion on the equivalent input noise of the amplifier as follows:

- at frequencies below a few Hz, the most important contribution to the equivalent input noise of the amplifier comes from the flicker noise of the JFETs. Indeed, at frequencies below 1 Hz, we expect the equivalent input noise to be coincident to $S^{J}{}_{in}$=$2S_{enJ}$;
- at frequencies above a few Hz and up to about 4 kHz, the noise contribution from the JFETs and from the resistances R_{1x} are of the same order, while the other sources of noise can be neglected. We expect a flat noise level in the order of 1 nV/$\sqrt{}$Hz;
- at frequencies above f_{pc}, because of the reduction of the loop gain, the noise introduced by the instrumentation amplifiers increases, until, at frequencies above 10 kHz, it becomes the most important source of noise, with the noise spectrum increasing proportionally to f^2.

In the previous discussion, we have assumed that the input filters and the second amplifier stage do not contribute to the equivalent input noise of the entire amplifier. Because of the need for AC coupling at the input and between the first and the second stage, this can only be obtained above a certain minimum frequency f_l that we take as the lowest frequency of interest for the measurements. For the design of such filters, we selected f_l=100 mHz as the minimum frequency of interest. As far as the input filters are concerned, we must therefore obtain a high pass frequency corner much lower that f_l. Moreover, we must insure a high input impedance in the pass band of the amplifier. The input impedance at low frequencies is indeed set by R_{Ax}. The capacitors C_{Ax} must insure that the noise generated by the large R_{Ax} resistances is filtered in such a way as to give a negligible contribution to the equivalent input noise starting from the minimum frequency of interest f_l. As it was observed in Ref.13, we expect the contribution of the equivalent input noise of the JFETs to be in the order 2×10^{-16} V^2/Hz at 100 mHz. With R_{Ax}=3.3MΩ and C_{Ax}=22 μF, we can estimate that, when both inputs are shorted to ground, the noise contribution to the equivalent input noise of the amplifier is in the order of 5×10^{-17} V^2/Hz, that is about four times below the noise introduced by the JFETs. Larger resistors and/or larger capacitors could be used to further reduce this contribution at the cost, however, of a longer settling time for the first stage.

As far as the design of the high pass filter between the first an the second stage is concerned, as we have observed before, because of the large gain (100) of the first stage, we do not need to worry about the noise introduced by the resistances and the equivalent input voltage noise of the instrumentation amplifier, as long as the frequency corner of the filter is below 100 mHz. However, in this case,

we must take into account the effect of the equivalent input current noise of the instrumentation amplifier. The impedance seen by each input of the instrumentation amplifier *IA*3, at frequencies above the pole frequency set by R_0 and C_0 is set by C_0. From the few data reported in the data-sheet of the INA131 regarding the equivalent input noise sources, we can estimate that, in the very low frequency range (f<1 Hz) their power spectrum S_{iin} can be written as:

$$S_{iin} = \frac{A_I}{f}; \quad A_I = 1.2 \times 10^{-24}\mathrm{A}^2 \tag{21}$$

Assuming the current noise sources at each input to be uncorrelated, from (21) we can estimate that their contribution to the equivalent input voltage noise of the entire amplifier at the lowest frequency of interest f_l is:

$$S_{in}^{IA3} = 2\frac{A_I}{f_l} \times \frac{1}{(2\pi f_l C_O)^2} \times \frac{1}{A_{DO1}^2} \tag{22}$$

where A_{DO1}=100 is the gain of the first stage. From (22) and from the condition of $S^{IA3}{}_{in}$ to be negligible with respect to the noise introduced by the JFETs, we obtain that we should employ capacitances much larger than 5 μF. With C_O=33 μF the contribution of the equivalent input current sources of *IA*3 is indeed negligible with respect to the other sources of noise at the lowest frequency of interest.

III. EXPERIMENTAL RESULTS AN DISCUSSION

The amplifier in Fig. 2 has been built with the components listed in Table I that have been selected according to the general guidelines reported in the previous paragraph.

For signal acquisition and spectra estimation, we used a spectrum analyzer that employs a National Instruments PCI-4451 two channels DSA board.

In a first experiment, we shorted to ground both inputs of the amplifier in order to evaluate the equivalent input noise. The acquired spectra at the output were divided by the gain of the amplifier squared (80 dB). The results of such measurements are reported in Fig.5 and Fig.6 for two different frequency ranges. As it is apparent from Fig.5, in the low frequency range (0.1 to 20 Hz) the noise spectrum S_{BN} is dominated by the noise introduced by the JFETs. In the frequency range between 10 Hz and about 2 kHz (Fig.6), the spectrum is flat and essentially coincides with the thermal noise introduced by the JFETs and by the resistances R_{1x}, as expected. Above 2 kHz, we notice that the noise spectrum rises, as expected because of the effect of frequency compensation.

In a second set of experiments, we employed a 10 kΩ resistor as a DUT. The measurements configurations are reported in Fig. 7. The results of these measurements confirm that the gain of the amplifier is 80 dB (with an error less than 1% in the entire bandwidth of the amplifier). When we connect the DUT between the two inputs, in a fully differential configuration, we obtain the thermal noise generated by the 10 kΩ resistor (Fig.5, (a) spectrum). When one input is shorted to ground and the DUT is connected from the other input and ground we still obtain the noise of the DUT(Fig.5, (b) spectrum). In a third experiment, we connected two 10 kΩ resistances from each input to ground. In this case, as expected, because of the uncorrelation in the noise produced by the two DUTs, we obtain, at the output, the noise corresponding to a 20 kΩ resistor (Fig.5, (c) spectrum).

Finally, we tied together the two inputs and connected a 100 kΩ resistor between the inputs and ground. In this case the noise produced by the DUT is a common mode signal and indeed we only obtain the background noise of the system. This means that, in the bandwidth in which the background noise is flat, we can estimate the common mode rejection ration to be in excess of 40 dB.

In Fig.6 we report the result of the measurements of a 10 kΩ resistance connected between the inputs in order to estimate the bandwidth of the system. As expected, the bandwidth is in excess of 30 kHz. For larger DUT impedances, however, the bandwidth is set by the equivalent input differential capacitance. Indeed, when a 100 kΩ is used as a DUT in differential measurements, the bandwidth is about 20 kHz that allows us to estimate a differential input capacitance in the order of 80 pF that is consistent with the value that can be estimated from the parasitic capacitances of the JFET

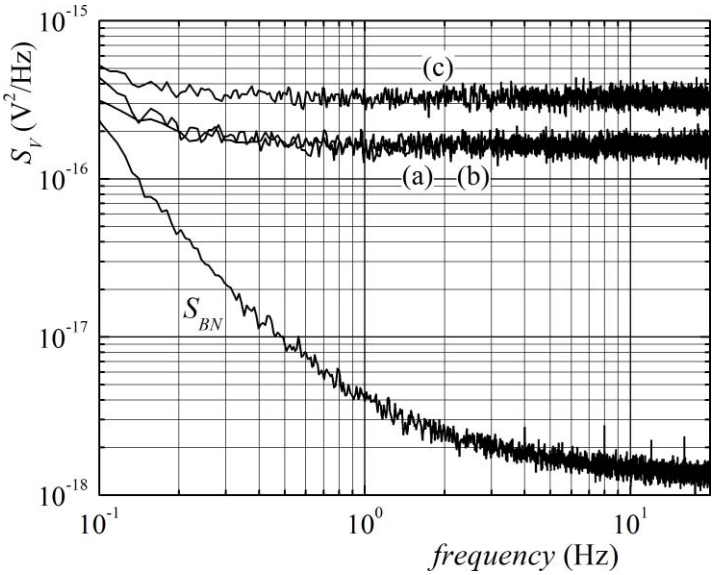

FIG. 5. Equivalent input voltage noise spectra. S_{BN} is the EIVN of the amplifier (both inputs shorted to ground); the other spectra (a), (b) and (c) are obtained using 10 kΩ resistors as DUTs in the corresponding configurations shown in Fig. 7.

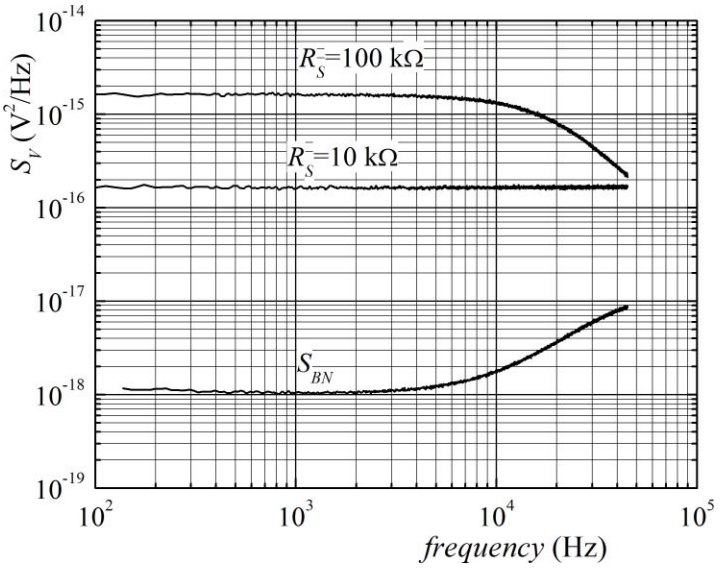

FIG. 6. Equivalent input voltage noise spectra in the frequency range from 100 Hz to 100 kHz. The resistances employed as DUTs are connected as in Fig. 7(a).

in the circuit configuration employed for the first stage of the amplifier. We can therefore conclude that the differential input impedance Z_{in} of the amplifier, for frequencies above f_l, is the series of the two R_{Ax} resistances in parallel to a capacitance C_{IN}=80 pF as shown in the equivalent circuit in Fig. 8, where also the equivalent input noise sources e_{BN} and i_{in} are shown together with a generic input source resistance R_S. The power spectrum S_{BN} of e_{BN} has already been reported in the previous measurements. With the help of the equivalent circuit in Fig. 8 and from the knowledge of the input impedance we can also estimate the power spectrum S_{Iin} of the equivalent input current noise source i_{in}. Indeed, we can evaluate the equivalent input voltage noise S_{VIOP} when the input is open ($R_S \to \infty$)

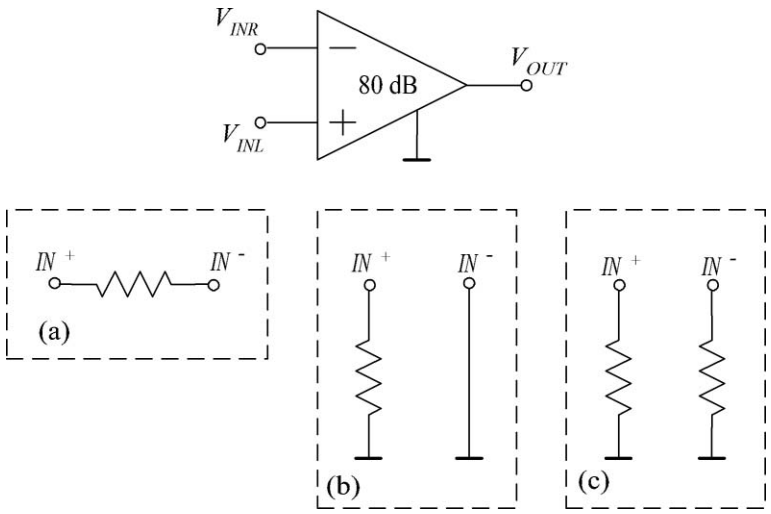

FIG. 7. Input DUTs connection used to test the performances of the amplifier. Configurations (a), (b) and (c) correspond to the spectra (a), (b) and (c) relatively in the plot of Fig. 5.

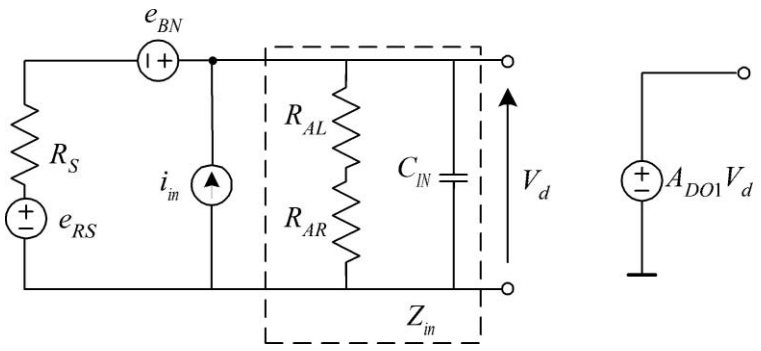

FIG. 8. Equivalent circuit for the estimation of the equivalent input current noise.

and obtain S_{Iin} as:

$$S_{Iin} = \frac{S_{VIOP}}{|Z_{in}|^2} \tag{23}$$

The result of the measurement of S_{VIOP} and the corresponding S_{Iin} estimated according to (23) are reported in Fig. 9. Note that, in order to cover the entire frequency range of interest from 100 mHz up to 30 kHz (more than 5 decades) with sufficient resolution at any frequency range, we had to perform two separate measurements, one with a sampling frequency of about 200 Hz (frequency range below 80 Hz) and another one with a sampling frequency of 100 kHz (frequency range above 80 Hz). As it can be noted from Fig. 9, up to a few kHz, S_{Iin} coincides with the thermal noise introduced by the resistances R_{AL} and R_{AR} (R_{AL}+R_{AR}=6.6 MΩ, with a thermal current noise, at room temperature, of about 2.5×10^{-27} A^2/Hz or 50 fA/$\sqrt{}$Hz). Above 10 kHz, S_{Iin} increases proportionally to f^2, possibly because of a significant contribution from the equivalent input current noise sources at the gate of the input JFETs.[17] In the hypothesis of uncorrelation between the equivalent input voltage noise source and the equivalent input noise source, we can also estimate the noise figure F as a function of the frequency and of the source resistance R_S in Fig. 8 as follows:

$$F = \frac{(S_{BN} + 4KTR_S)\left|\frac{Z_{in}}{Z_{in}+R_S}\right|^2 + S_{Iin}\,|Z_{in}||R_S|^2}{4KTR_S\left|\frac{Z_{in}}{Z_{in}+R_S}\right|^2} \tag{24}$$

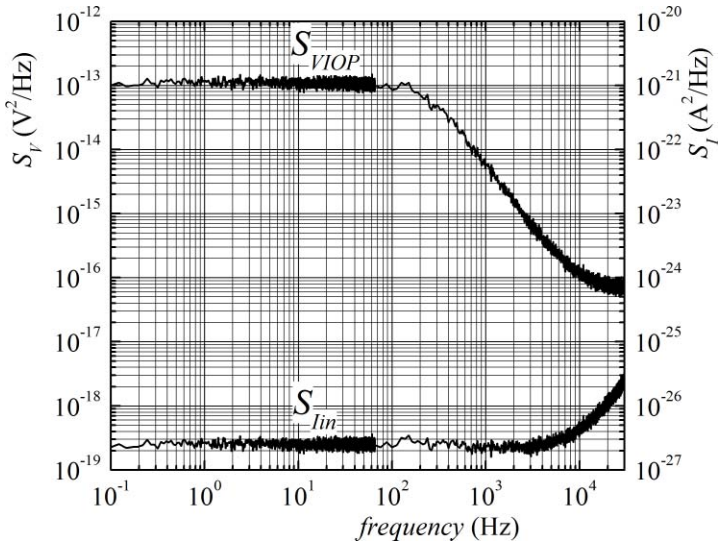

FIG. 9. Result of the measurement of the equivalent input voltage noise S_{VIOP} when the input is open ($R_S \rightarrow \infty$) and estimated equivalent input current noise spectrum S_{Iin}.

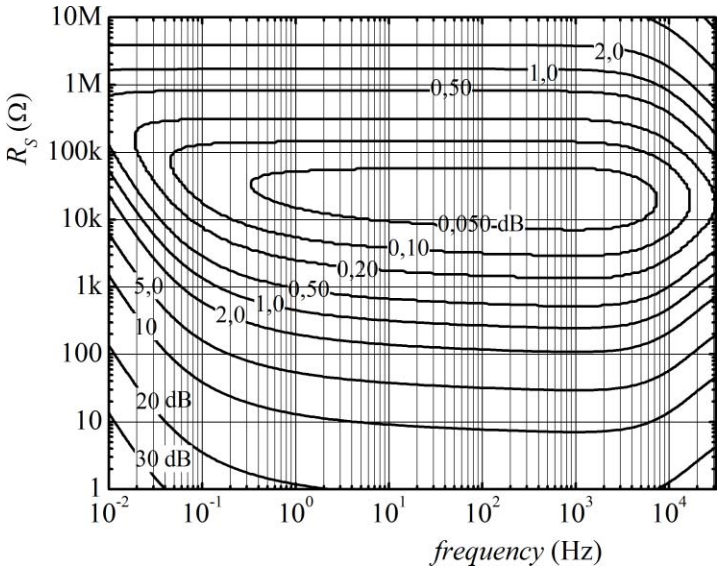

FIG. 10. Contour plots of the noise figure F as a function of the frequency and of the source resistance R_S.

Contour plots of the noise figure F are reported in Fig. 10 that may help to appreciate the overall noise performances of the proposed amplifier.

IV. CONCLUSIONS

In this paper we have discussed the design of a differential input ultra low noise preamplifier for application in the field of high sensitivity low frequency noise measurements. Both inputs are AC coupled with a low frequency corner of 2.2 mHz. The design has been optimized, as far as the equivalent input voltage noise is concerned, in the assumption that the lowest frequency of interest is 100 mHz. Indeed, in the bandwidth from 100 mHz and 10 Hz, the equivalent input noise coincides with that introduced by the very low noise discrete JFETs IF3602 employed in the design of the first stage. The equivalent input voltage noise, as measured on a prototype of the system, is

14 nV/$\sqrt{}$Hz (100 mHz), 2 nV/$\sqrt{}$Hz (1 Hz), 1.2 nV/$\sqrt{}$Hz (10 Hz) and 1 nV/$\sqrt{}$Hz (f>100 Hz) in excellent agreement with that predicted in the design. At frequencies higher than 2 kHz the equivalent voltage noise increases because of the effect of the compensation needed for insuring stability but it remains, however, below 3 nV/$\sqrt{}$Hz up to 40 kHz. Because of the AC coupling, there is no limitation to the common mode and differential DC voltage values that can be present at the inputs of the amplifier. The bandwidth of the system extends above 10 kHz for low input impedances ($|Z_{in}|<$ 10 kΩ). For high DUT impedances, the bandwidth of the amplifier is limited by the differential input capacitance. The differential input impedance of the amplifier at frequencies above a few tens of mHz can be regarded as the parallel of a 6.6 MΩ resistance in parallel to an 80 pF capacitance, that is due to the effect of the parasitic capacitances of the JFETs in the circuit configuration used in the first stage. As far as the equivalent input current noise is concerned, proper measurements have demonstrated that, from 100 mHz up to a few kHz, its power spectrum is about 2.5×10^{-27} A^2/Hz (50 fA/$\sqrt{}$Hz) and it is mainly due to the thermal noise introduced by the resistances R_{AL} and R_{AR} that are part of the AC input coupling network. It must be noted that these excellent performances are guaranteed by design and no calibration or trimming step is required. We believe that this fact, together with the very simple topology that has been devised, should allow anyone interested in the field of low frequency noise measurements to easily reproduce the amplifier we have described.

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