MOS Capacitance–Voltage Characteristics: V. Methods to Enhance the Trapping Capacitance*

Jie Binbin(揭斌斌)[1,2,†] and Sah Chihtang(薩支唐)[1,2]

[1]Department of Physics, Xiamen University, Xiamen 361005, China
[2]CTSAH Associates, Gainesville, Florida 32605, USA

Abstract: Low-frequency and High-frequency Capacitance–Voltage (C–V) curves of Silicon Metal–Oxide–Semiconductor Capacitors, showing electron and hole trapping at shallow-level dopant and deep-level generation-recombination-trapping impurities, are presented to illustrate the enhancement of the giant trapping capacitances by physical means via device and circuit designs, in contrast to chemical means via impurity characteristics previously reported. Enhancement is realized by masking the electron or/and hole storage capacitances to make the trapping capacitances dominant at the terminals. Device and materials properties used in the computed CV curves are selected to illustrate experimental realizations for fundamental trapping parameter characterizations and for electrical and optical signal processing applications.

Key words: MOS; silicon; trapping capacitance; dopant impurities; donors; acceptors
DOI: 10.1088/1674-4926/33/2/021001 **PACC:** 7340Q **EEACC:** 2560R

1. Introduction

We recently reported an investigation[1−4] (referred also as I, II, III and IV) of the capacitance–voltage (CV) characteristics of silicon and germanium Metal–Oxide–Semiconductor (MOS) capacitors (MOSCs) including the capacitance arisen from electron and hole trapping at the shallow-energy-level donor and acceptor dopant impurities and at the deep-energy-level donor, acceptor and amphoteric generation–recombination–trapping (g–r–t or grt or GRT) chemical impurities. These included all possible impurities, thus, they can be generalized with the acronym of d–g–r–t, dgrt or DGRT impurities. The results also apply to shallow and deep energy levels from physical defects, such as the point-defect-vacancies (missing a host atom at its lattice site, such as V_{Si}, V_{Ge} and V_C in the monoatomic semiconductors Si, Ge and C; V_{Ga} and V_{As} in GaAs and other binary III–V, II–VI, ternary and many-atom-species compound semiconductors), the pair defects-divancies ($V_{Si}V_{Si}$, $V_{Ge}V_{Ge}$, $V_{Ga}V_{As}$), and self-interstitials (I_{Si}, I_{Ge}, and I_{Ga} and I_{As} in GaAs). The results also apply to impurity-defect pairs, such as $O_{Si}V_{Si}$ which involves only one lattice point with the impurity displaced from the lattice site and other physical configurations that are favored from the high-temperature processing steps or from displacement radiation damage (A host atom is displaced by an energetic ion during the exposure to an energetic ion beam, such as ion implantation used in the silicon integrated circuit fabrication and production processes.) See Chapter 2 of Ref. [5] for a more detailed discussion of these imperfections (chemical impurities and physical defects) in crystalline solids.

The trapping capacitance can show a large presence in the capacitance–voltage (CV) characteristics at the two measurement or application terminals of the MOSC, because the trapping capacitance can be made very large, to many times the oxide capacitance, by increasing the concentration of the d–g–r–t impurities. The large trapping capacitance can provide unprecedented sensitivity, for the characterization of the fundamental electrical and optical properties of these electronic or electron and hole traps at the dopant and generation-recombination-trapping impurities and at the physical defects, as well as for new electrical and optical signal processing applications. In the first four reports[1−4], we described the results of enhancing the trapping capacitance at the two electrical signal terminals, solely by chemical means, namely, by the selection of the impurity species, which have large electron or hole binding energies, and by the use of two impurity species to bring out the large trapping capacitance of the second species in the gate voltage range of low masking from electron and hole storage capacitances. In this fifth report V, we describe the CV curves at the two signal terminals that avoid and eliminate the charge storage capacitance of the majority or minority carriers, or both, which masks the trapping capacitances, in order to bring out to the two terminals of the MOSCs, the full magnitude of the trapping capacitances.

2. Computed Capacitance–Voltage Characteristics with Trapping Capacitance

The equations used in this report V, are those employed in I–II–III–IV[1−4].

The terminal capacitance of an MOS capacitor is the series connection of the oxide capacitance, C_{ox}, with the semiconductor surface space-charge layer capacitance, C_{sz}, given by $C_{gz} = C_{ox}C_{sz}/(C_{ox} + C_{sz})$. The semiconductor surface space-

* This investigation is supported by the Xiamen University, China, and the CTSAH Associates (CTSA), founded by the late Linda Su-Nan Chang Sah.
† Corresponding author. Email: bb_jie@msn.com
Received 27 September 2011, revised manuscript received 23 October 2011

charge layer capacitance, referenced to terminal z denoted by C_{sz}, generally contains three charge storage capacitances in parallel which are due to: the electrons and holes stored in the conduction and valence bands in the semiconductor surface space-charge layer, C_n and C_p; and the electrons stored at the electron traps, C_{nt}, and the holes stored at the hole traps, C_{pt}. We shall denote all the trapping capacitances as a sum with the symbol $C_t = C_{nt}+C_{pt}$ while for a specific electron or hole trap, such as $C_{n\text{-}P}$ for the electron trapping capacitance at the phosphorus donor impurity, $C_{p\text{-}B}$ for the hole trapping capacitance at the boron acceptor impurity, and $C_{n\text{-}Au}$ and $C_{p\text{-}Au}$ for the amphoteric gold impurity in silicon that can trap one electron at one energy level and one hole at another energy level in the silicon energy gap. The filling and emptying of these storage sites, or the charging and discharging of these sites, are the kinetic transition processes of the electrons and holes which give rise to the charging-discharging rate or frequency-dependent capacitances. Therefore, the surface space-charge layer capacitance is given by $C_{sz} = C_n + C_p + C_t$. Thus, it is obvious that to make the trapping capacitances prominent or dominant between the two signal terminals, g (g for gate) and z (to be discovered or designed in this paper-V), the electron and hole charge storage capacitances, C_n and C_p need to be minimized or eliminated when measured from the two terminals, g and z, for integrated circuit applications via metal–conductor-lines to connect the terminals.

To streamline illustrating many examples, we follow the presentation scheme employed in the previous three reports[2−4], modified for the present objective of showing the trapping capacitances, minimally masked or not masked by the mobile electron and hole charge storage capacitances. Thus, each of the twelve figures, one for each of twelve chemical impurity selections, consists of four parts, (a), (b), (c) and (d), to demonstrate the physical schemes of eliminating the electron or/and hole charge storage capacitances. The terminal capacitance between the gate and z terminals, in the presence of all the semiconductor capacitances (electron and hole storage and trapping), is given by the gate oxide capacitance in series with the semiconductor capacitance which consists of all the charge storage capacitances of band and trap electrons and holes, $C_{gz} = C_{ox}C_{sz}/(C_{ox} + C_{sz})$. Figure (a) is the physical and terminal configuration in which the contact of the z-terminal to the semiconductor is an infinite source and drain of electrons and holes, that is, a contact whose generation and recombination rate of electrons and holes are infinite relative to the rate of change of the measuring voltage or current, or the sinusoidal frequency of the small-signal that is measuring the capacitance current through the two terminals, which is known as the ohmic contact with zero resistance. This is usually denoted by b for base or body, and z = b and $C_{sz} = C_{sb}$ where $C_{sz} = C_{sb} = C_n+C_p+C_t = C_n+C_p+C_{nt}+C_{pt}$. This is given by the CV curves in Figures (a) of the twelve figures. They are the same as the Figure (a) of the figures given the previous three reports[2−4]. Thus, Figure (a) shows the total measurable capacitance between the two terminals g and b given by $C_{gb} = C_{ox}C_{sb}/(C_{ox} + C_{sb}) = C_{ox}(C_n + C_p + C_t)/(C_{ox} + C_n + C_p + C_t) = C_{ox}(C_n + C_p + C_{nt} + C_{pt})/(C_{ox} + C_n + C_p + C_{nt} + C_{pt})$. Figure (b) is the terminal capacitance between the gate and a contact z to the body which can source and sink (drain) only electrons such as the n+layer or n+region on the n-type or p-type body, thus, z = n, and the semiconductor capacitance is denoted by $C_{sz} = C_{sn} = C_n + C_t = C_n + C_{nt} + C_{pt}$. Figure (c) has the hole source and drain, $C_{sz} = C_{sp} = C_p + C_t = C_p + C_{pt} + C_{nt}$. Figure (d) has a body contact z which is neither the hole nor the electron source and drain, such as a capacitive or electrical displacement current contact from a second insulated gate with a much larger gate area and thinner equivalent gate oxide. Thus, $C_{sz} = C_t = C_{pt} + C_{nt}$. It is noted that the carrier trapping capacitance can still appear in the absence of a contact that sources and drains the trapping carrier, on account of the equilibrium concentration of the carrier and via the recombination transition of the trapped majority carrier with a band minority carrier.

Figures 1(a) to 1(d) show the CV curves of MOSCs on an n-type silicon with a 50 meV shallow energy level donor dopant impurity such as phosphorus. Figures 2(a) to 2(d) show the CV curves for a deeper dopant impurity in Si. Figures 3(a) to 3(d) contain two impurity species consisting of a shallow donor and a shallow acceptor while Figures 4(a) to 4(d) contain two impurity species consisting of a shallow donor and a deep acceptor. Figures 5(a) to 5(d) contain two donor species, one shallow and one deep, while Figs. 6(a) to 6(d), two acceptor species. Figures 7(a) to 7(d) model the double-donor or two-electron trap such as Sulfur, in phosphorus doped n-type Si, while Figs. 8(a) to 8(d), in boron doped p-type silicon. Similarly, Figs. 9(a) to 9(d) are those for the double acceptor or two-hole trap zinc in p-Si, while Figs. 10(a) to 10(d), in n-Si. Figures 11(a) to 11(d), and 12(a) to 12(d) are those for the amphoteric gold generation-recombination-trapping center in n-Si and p-Si respectively.

In the next and sixth report, we shall show another method for enhancing and modulating the trapping capacitance, and describe the application details using the giant trapping capacitance. Using the present analyses and formulas, CV curves for other combinations of dgrt impurities and defects, and their complexes, are readily obtained for application-specific purposes at signal terminals of a variety of electrical and optical frequency ranges, as illustrated by the prophetic nomogram, Energy Conversion Chart, given by Shockley 62 years ago[7]. In detector applications, using an impurity in Germanium with energy level from 0.01 eV to 0.33 eV[3], the corresponding range of the lower cut-off frequency is from 2.4 THz to 80 THz, while using an impurity in Silicon with energy level from 0.05 eV to 0.60 eV[3], the corresponding range of the lower cut-off frequency is from 12 THz to 145 THz. Signal can also be generated by radiative capture of an electron or a hole by the trap, and the rate can be calculated directly or from the inverse of photo-ionization cross-section such as that made for the double-donor sulfur in silicon[8]. It should be obvious that the giant trapping capacitance in MOSC is infinitely easier to implement than the methods described by the articles in the latest issue on Terahertz electronics in Science China Information Sciences[9] and their references, for examples, Terahertz detectors based on superconducting hot electron bolometers[10], and Terahertz radiation sources based on free electron lasers and their applications[11] and Terahertz source based on optical Cherenkov radiation[12]. And its circuit integration for signal processing is easily implemented, monolithically by the silicon MOS integrated circuit technology on the same silicon chip, much easier than those recently described[13].

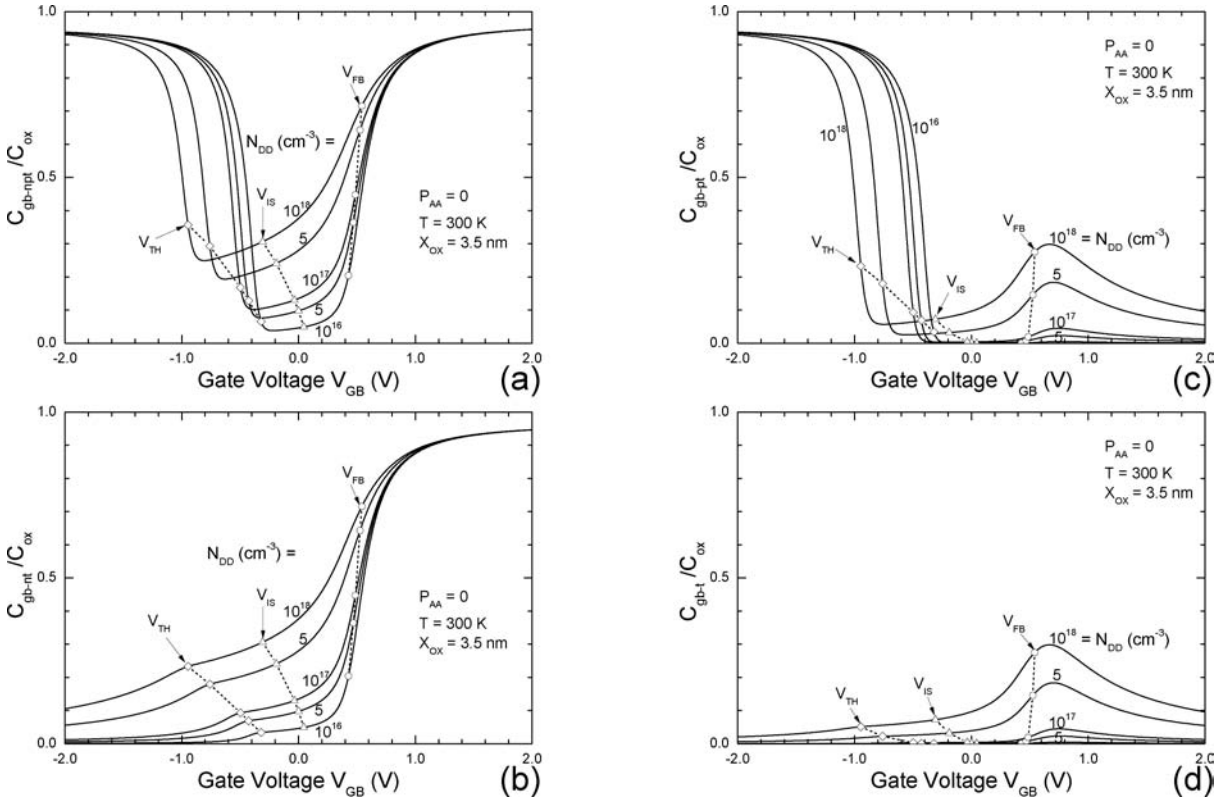

Fig. 1. Signal terminal capacitance of MOSCs on n-Si with a 50 meV donor impurity such as Phosphorus at $N_{DD} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

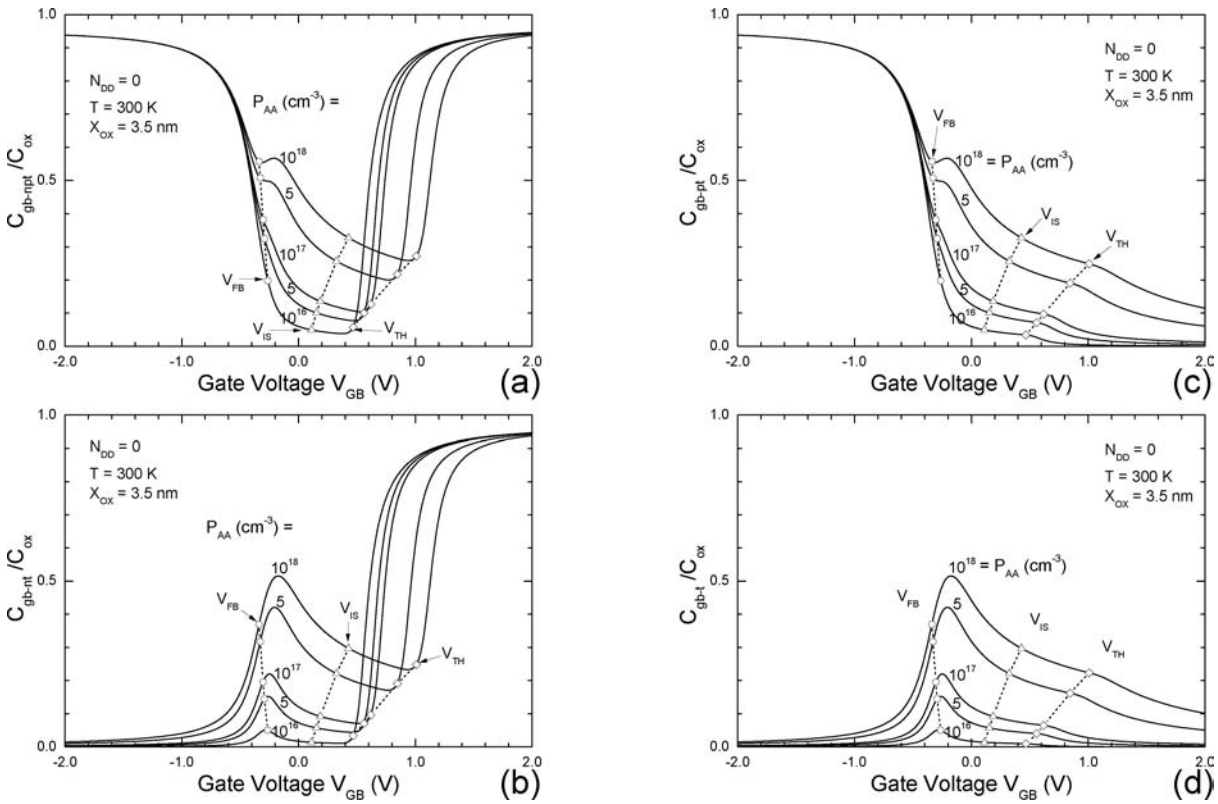

Fig. 2. Signal terminal capacitance of MOSCs on p-Si with a 150 meV acceptor impurity such as Indium at $P_{AA} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

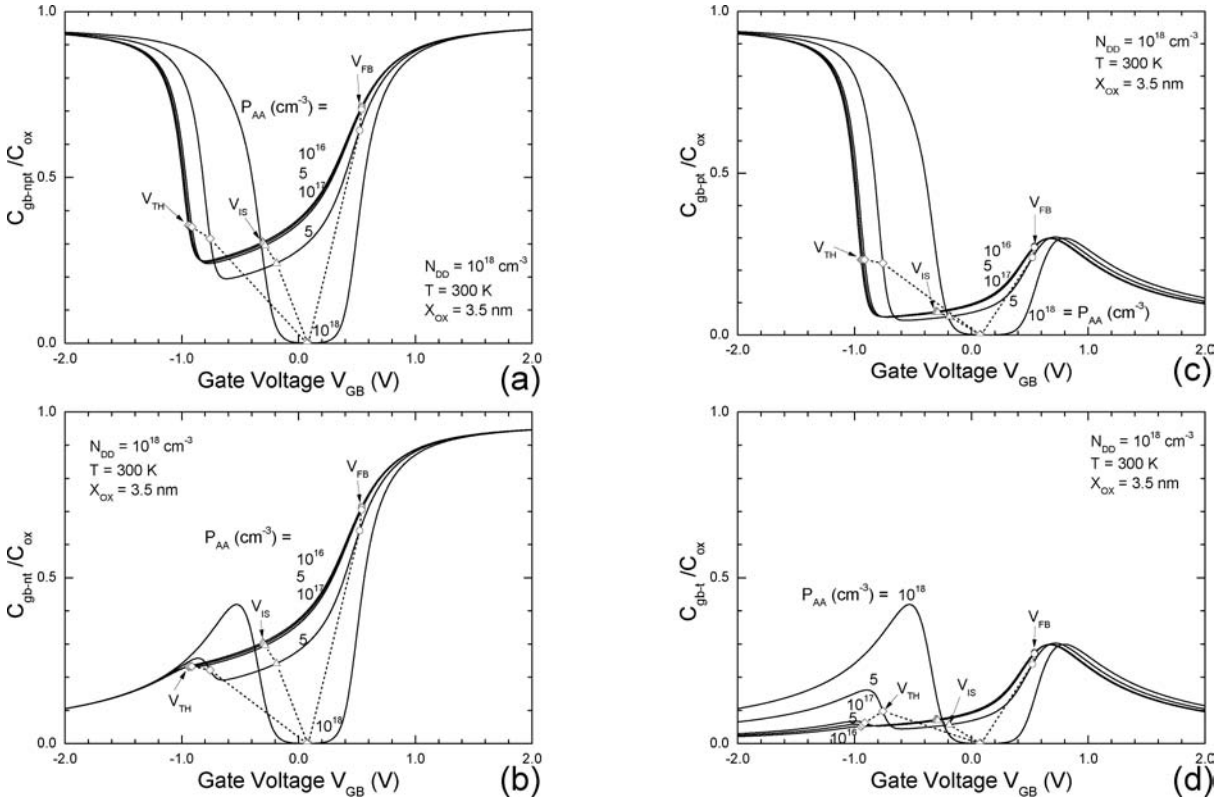

Fig. 3. Signal terminal capacitance of MOSCs on Si with a 50 meV donor (Phosphorus) at $N_{\mathrm{DD}} = 10^{18}$ cm^{-3} and a 50 meV acceptor (Boron) at $P_{\mathrm{AA}} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_{\mathrm{n}} + C_{\mathrm{p}} + C_{\mathrm{t}}$, (b) $C_{\mathrm{n}} + C_{\mathrm{t}}$, (c) $C_{\mathrm{p}} + C_{\mathrm{t}}$ and (d) C_{t}.

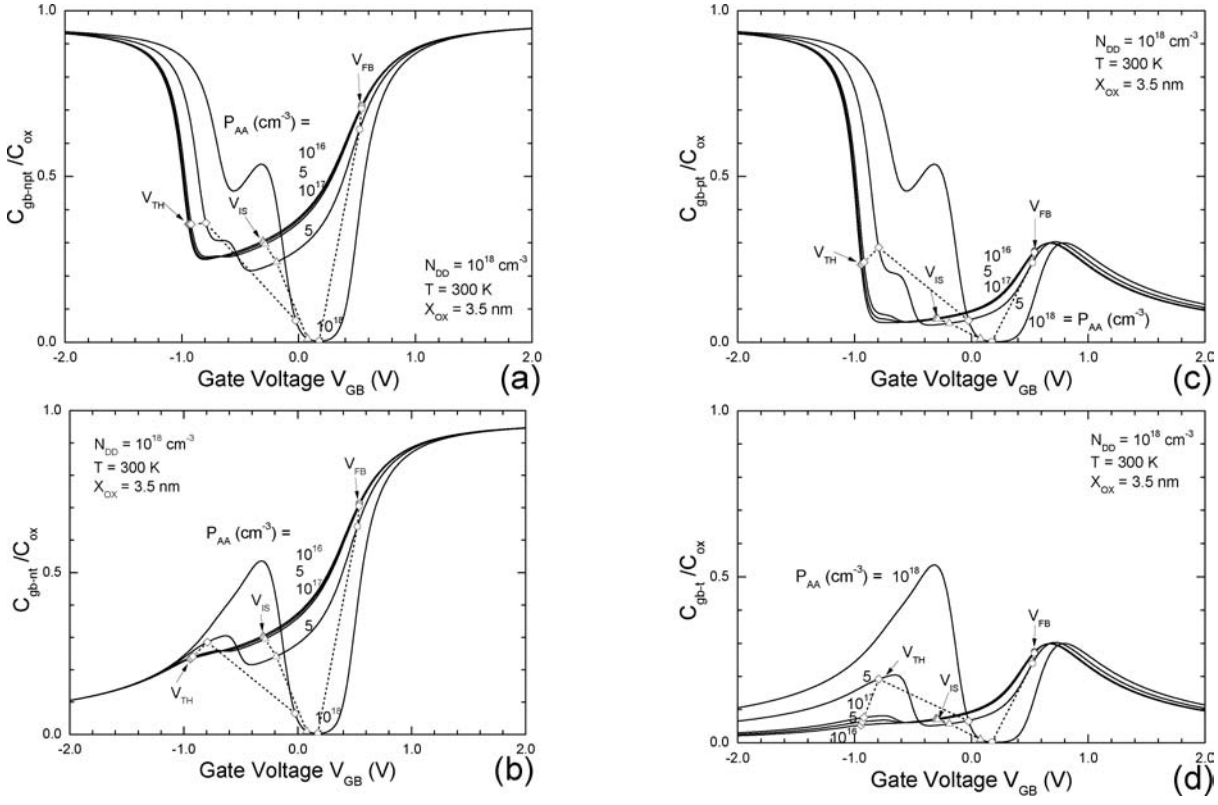

Fig. 4. Signal terminal capacitance of MOSCs on Si with a 50 meV donor (Phosphorus) at $N_{\mathrm{DD}} = 10^{18}$ cm^{-3} and a 250 meV acceptor (Thallium) at $P_{\mathrm{AA}} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_{\mathrm{n}} + C_{\mathrm{p}} + C_{\mathrm{t}}$, (b) $C_{\mathrm{n}} + C_{\mathrm{t}}$, (c) $C_{\mathrm{p}} + C_{\mathrm{t}}$ and (d) C_{t}.

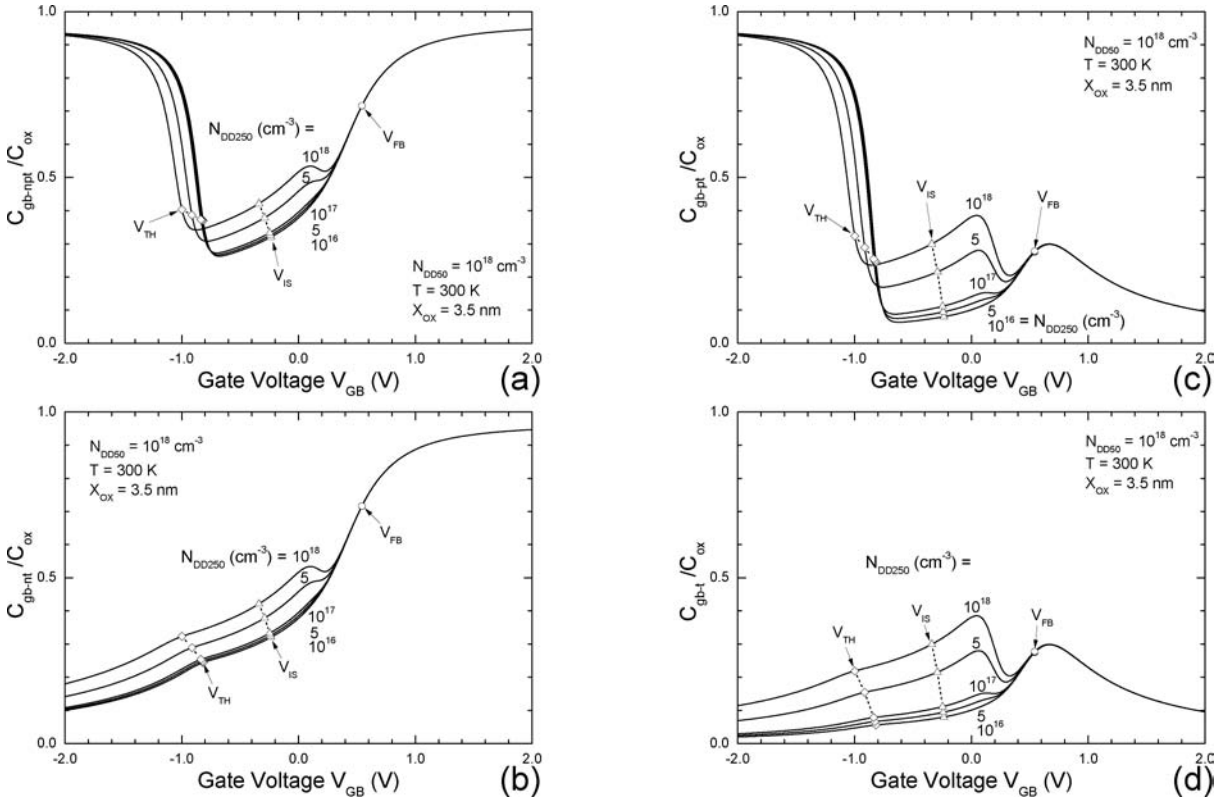

Fig. 5. Signal terminal capacitance of MOSCs on Si with a 50 meV donor at $N_{\mathrm{DD50}} = 10^{18}$ cm^{-3} and a 250 meV donor at $N_{\mathrm{DD250}} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_{\mathrm{n}} + C_{\mathrm{p}} + C_{\mathrm{t}}$, (b) $C_{\mathrm{n}} + C_{\mathrm{t}}$, (c) $C_{\mathrm{p}} + C_{\mathrm{t}}$ and (d) C_{t}.

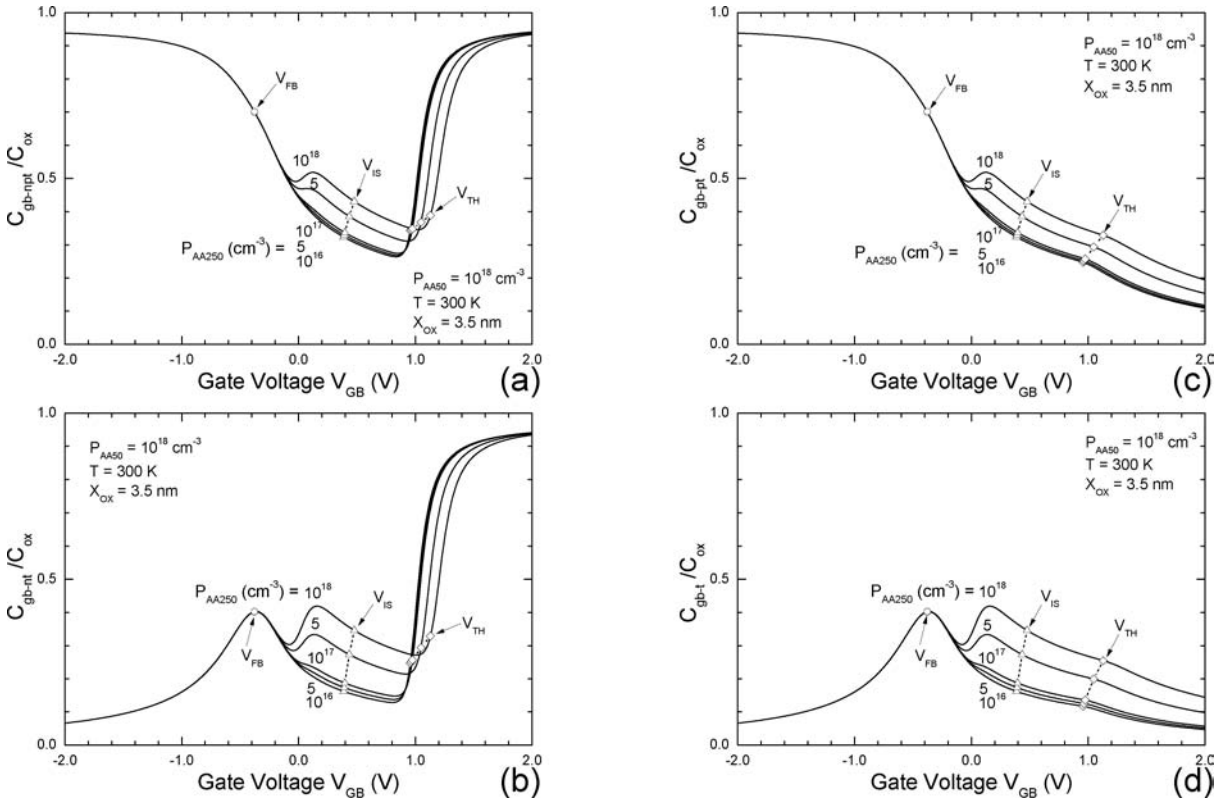

Fig. 6. Signal terminal capacitance of MOSCs on Si with a 50 meV acceptor at $P_{\mathrm{AA50}} = 10^{18}$ cm^{-3} and a 250 meV acceptor at $P_{\mathrm{AA250}} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_{\mathrm{n}} + C_{\mathrm{p}} + C_{\mathrm{t}}$, (b) $C_{\mathrm{n}} + C_{\mathrm{t}}$, (c) $C_{\mathrm{p}} + C_{\mathrm{t}}$ and (d) C_{t}.

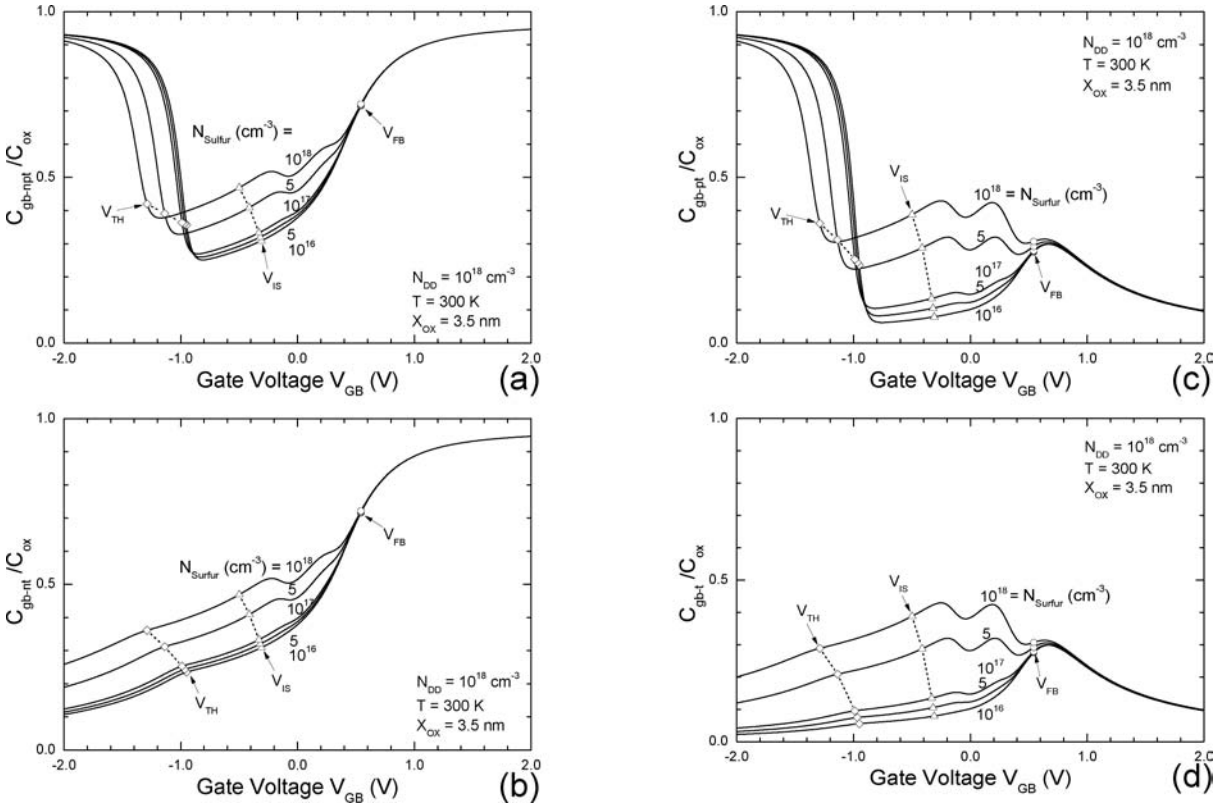

Fig. 7. Signal terminal capacitance of MOSCs on Si with a 50 meV donor at $N_{DD} = 10^{18}$ cm^{-3} and a Sulfur double-donor, $E_C - 180$ meV and $E_C - 380$ meV, at $N_{Sulfur} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

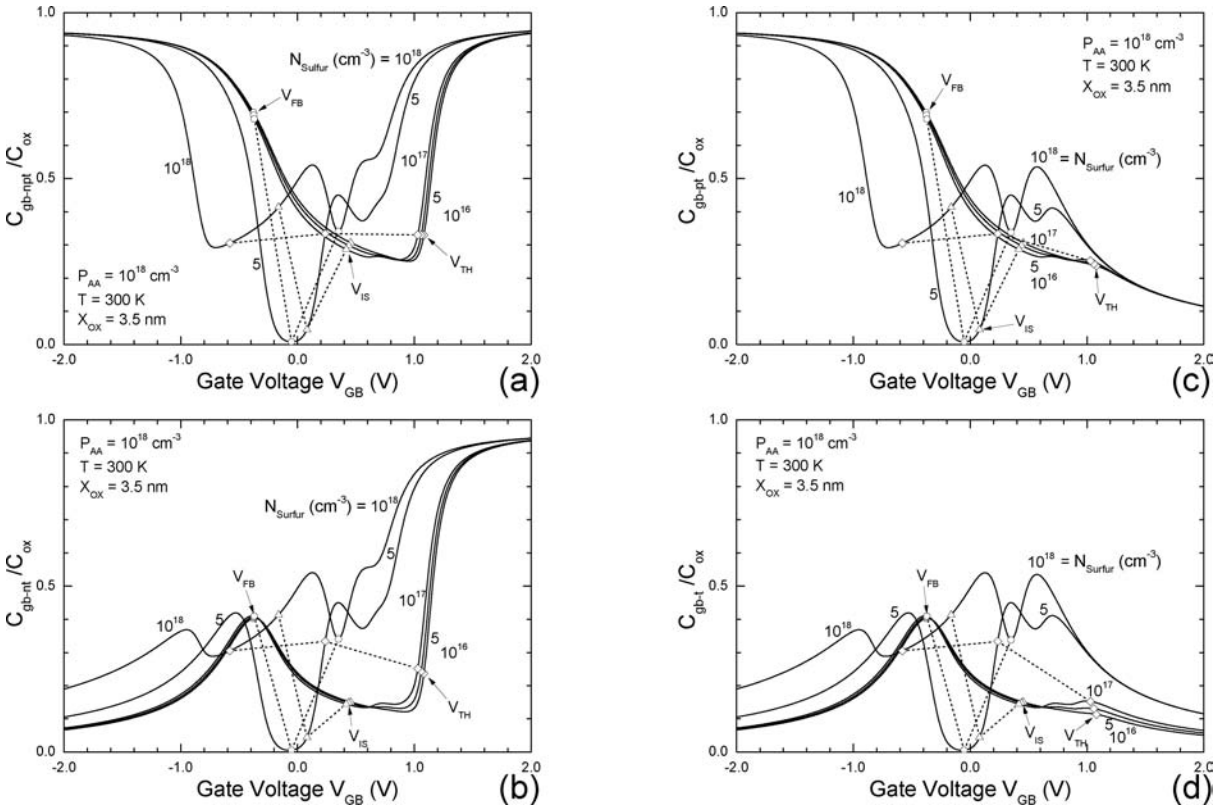

Fig. 8. Signal terminal capacitance of MOSCs on Si with a 50 meV acceptor at $P_{AA} = 10^{18}$ cm^{-3} and a sulfur double-donor, $E_C - 180$ meV and $E_C - 380$ meV, at $N_{Sulfur} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

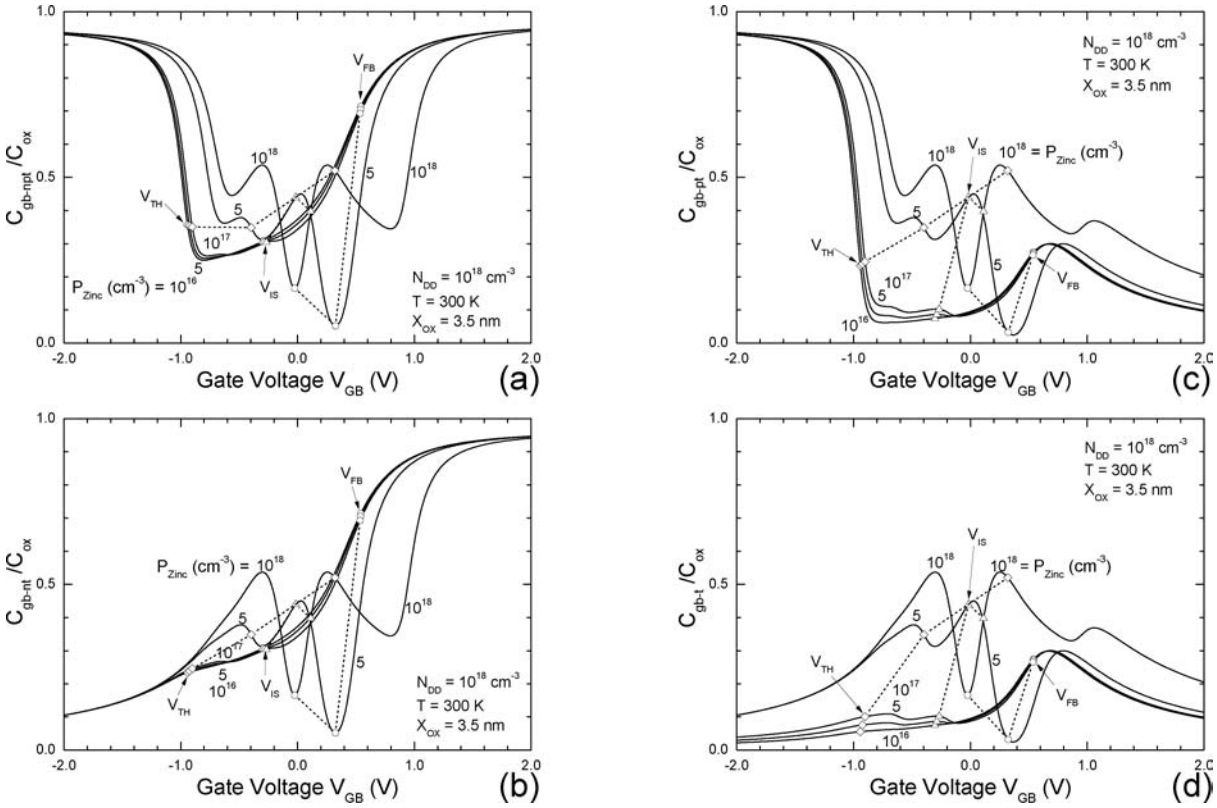

Fig. 9. Signal terminal capacitance of MOSCs on Si with a 50 meV donor at $N_{DD} = 10^{18}$ cm^{-3} and a Zinc double-acceptor, $E_V + 660$ meV and $E_V + 310$ meV, at $P_{Zinc} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

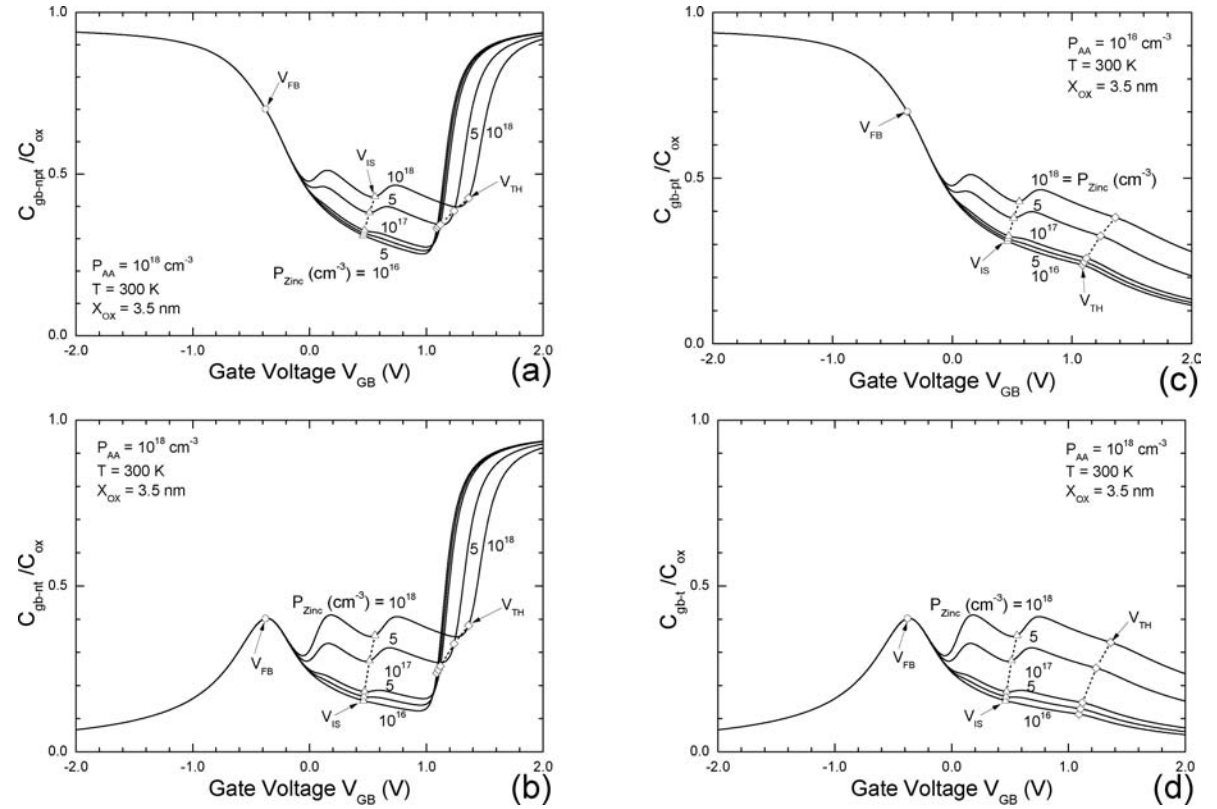

Fig. 10. Signal terminal capacitance of MOSCs on Si with a 50 meV acceptor at $P_{AA} = 10^{18}$ cm^{-3} and a Zinc double-acceptor, $E_V + 660$ meV and $E_V + 310$ meV, at $P_{Zinc} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

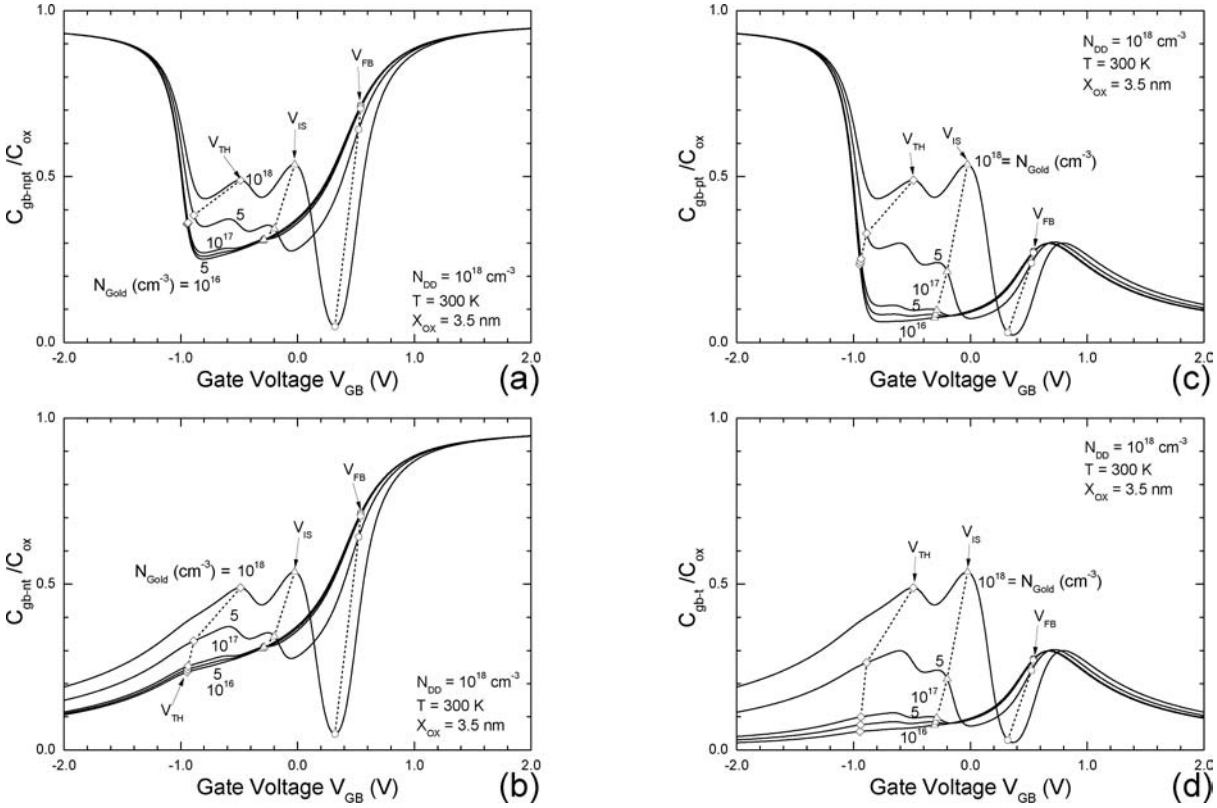

Fig. 11. Signal terminal capacitance of MOSCs on Si with a 50 meV donor at $N_{DD} = 10^{18}$ cm^{-3} and an amphoteric Gold, $E_C - 540$ meV and $E_V + 350$ meV, at $N_{Gold} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

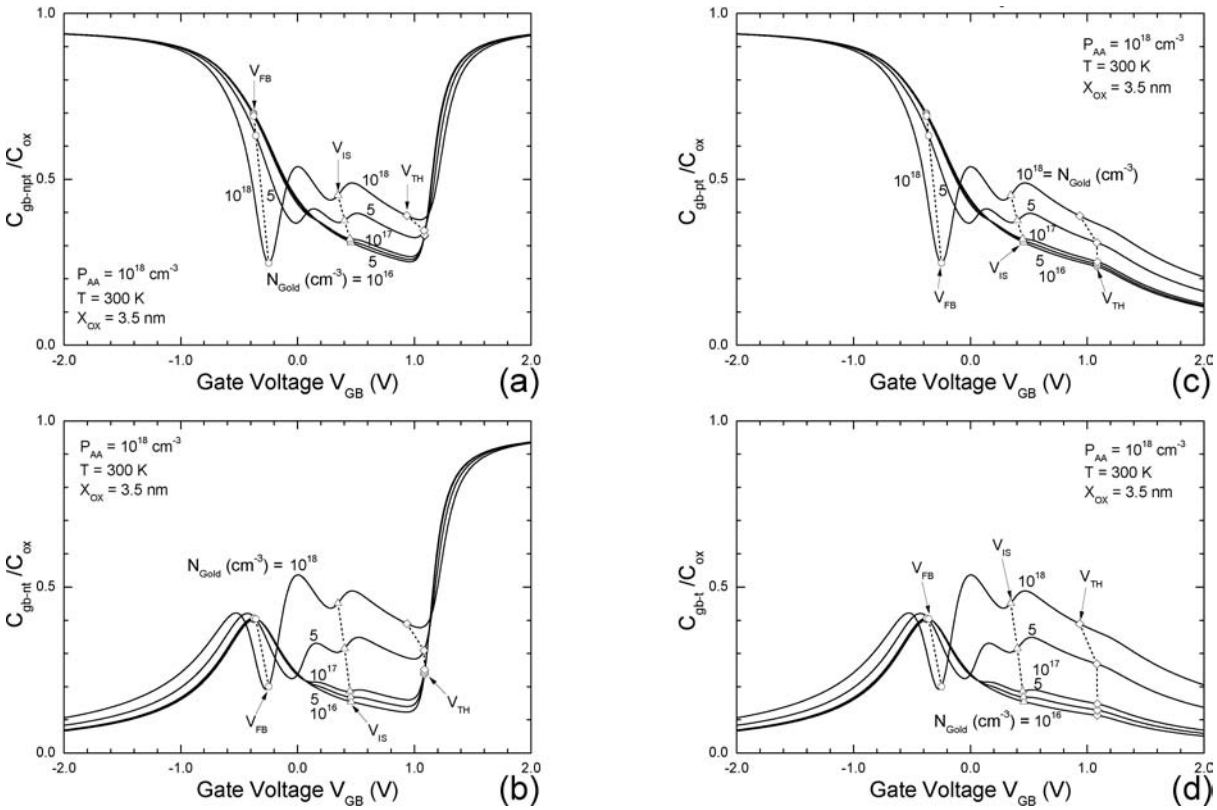

Fig. 12. Signal terminal capacitance of MOSCs on Si with a 50 meV acceptor at $P_{AA} = 10^{18}$ cm^{-3} and an amphoteric Gold, $E_C - 540$ meV and $E_V + 350$ meV, at $N_{Gold} = 10^{16}$ to 10^{18} cm^{-3}. C_{sz} is (a) $C_n + C_p + C_t$, (b) $C_n + C_t$, (c) $C_p + C_t$ and (d) C_t.

3. Summary and Acknowledgment

The main purpose of this survey-calculation report is to demonstrate the elimination of the majority and minority carrier storage capacitances in order to make the trapping capacitance dominating the signal terminal capacitance. Instead of the chemical method of selecting the impurities in the previous four reports, I, II, III and IV[1−4], this fifth report presented the physical method, or the device structure method, of providing a specific contact to the base or bulk of the semiconductor as the second signal terminal to complement the first signal terminal, the MOS metal gate. These second signal terminals can be the terminal to the electron or n+ contact, the hole or p+ contact, and the dielectric or displacement current contact from a second insulated-gate Metal/Oxide contact to the MOS capacitor structure. We thank Xiamen University President, Dr. Zhu Chongshi, and Dean of Physics, Dr. Wu Chenxu, for support of this work.

References

[1] Jie Binbin and Sah Chihtang, "MOS Capacitance–Voltage Characteristics from Electron-Trapping at Dopant Donor Impurity," Journal of Semiconductors, 32(4), 041001, 1–9, April 2011. This is referred to as Paper I in this series on trapping capacitances.

[2] Jie Binbin and Sah Chihtang, "MOS Capacitance–Voltage Characteristics II. Sensitivity of Electronic Trapping at Dopant Impurity from Parameter Variations," Journal of Semiconductors, 32(12), 121001, 1–11, December 2011.

[3] Jie Binbin and Sah Chihtang, "MOS Capacitance–Voltage Characteristics III. Trapping Capacitance from 2-Charge-State Impurities," Journal of Semiconductors, 32(12), 121002, 1–16, December 2011.

[4] Jie Binbin and Sah Chihtang, "MOS Capacitance–Voltage Characteristics IV. Trapping Capacitance from 3-Charge-State Impurities," Journal of Semiconductors, 33(1), 011001, January 2012.

[5] Chih-Tang Sah, Fundamentals of Solid-State Electronics, 1001pp. World Scientific Publishing Company, 1991. See Chapter 2 on the classifications of imperfections, both chemical and physical, in semiconductors and crystalline solids.

[6] Jie Binbin and Sah Chihtang, "MOS Capacitance–Voltage Characteristics VI. Applications of the Trapping Capacitance," Journal of Semiconductors, 33(3), 031001, March 2012.

[7] William Shockley, Electrons and Holes in Semiconductors, 558pp. D. Van Nostrand Company, Inc. New York. 1950. Third edition, reprinted January 1953. See his prophetic nomogram given in Appendix D on the inside of the back cover, titled Energy Conversion Chart.

[8] Ning Tak H and Sah Chih-Tang, "Photoionization Cross Section of a Two-electron Donor Center in Silicon," Physical Review B, 14(6), 2528–2533, September 15, 1976.

[9] Liu Shenggang and Xie Weixin, editor's note, Science China Information Sciences, 55(1), January 2012.

[10] Jiang Yi, Jin Biaobing, Xu Weiwei, Kang Lin, Chen Jian, and Wu Peiheng, "Terahertz detectors based on superconducting hot electron bolometers," Science China Information Sciences, 55(1), 64–71, January 2012.

[11] Tan Ping, Huang Jiang, Liu KaiFeng, Xiong YoungQian, and Fan MingWu, "Terahertz radiation sources based on free electron lasers and their applications," Science China Information Sciences, 55(1), 1–15, January 2012.

[12] Yao JianQuan, Liu PengXiang, Xu DeGang, LV YingJin and LV Da, "THz source based on optical Cherenkov radiation," Science China Information Sciences, 55(1), 37–24, January 2012.

[13] See the circuit application articles in the January 2012 issue of Science China Information Science cited in [9]–[12].