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# A review: wafer bonding of Si-based semiconductors

Shaoying Ke<sup>a,d,e</sup>, Dongke Li<sup>b,d</sup>, Songyan Chen<sup>c,e</sup>

<sup>a</sup> College of Physics and Information Engineering, Minnan Normal University, Zhangzhou, 363000, China

<sup>b</sup> School of Physics and Electrical Engineering, Jiangsu Key Laboratory for Modern Measurement of Technology and Intelligent System, Huaiyin Normal University, Huai'an, 223300, China

<sup>c</sup> Fujian Provincial Key Laboratory of Semiconductors and Applications, Collaborative Innovation Center for Optoelectronic Semiconductors and Efficient Devices, Department of Physics, Xiamen University, Xiamen, 361005, China

<sup>d</sup>The authors contributed equally to this work.

<sup>e</sup>[keshaojing2005@163.com](mailto:keshaojing2005@163.com) and [sychen@xmu.edu.cn](mailto:sychen@xmu.edu.cn)

**Abstract.** Wafer bonding techniques, which are very different from epitaxial growth techniques, not only can be used for the fabrication of micro-electromechanical systems (MEMS), silicon on insulator (SOI), and Si-based device integration, but recently were applied for the achievement of high-quality homojunction and heterojunction in the photoelectric field. That is, carrier transport at the interface of the wafer-bonded junction should be unimpeded and carrier recombination at the bonded interface should be restrained. For Si/Si wafer bonding, although high bonding strength and bubble-free bonded interface are needed for the fabrication of the MEMS and SOI, a perfect Si/Si bonded interface which is expected to be bubble-free, oxide-layer-free, and dislocation-free is needed for the achievement of high-performance photoelectric devices, such as Ge/Si single-photon avalanche photodiodes. On the other hand, for Ge/Si heterogeneous hybrid integration (high lattice mismatch), threading dislocations (TDs) in the Ge film can be eliminated by low-temperature heterogeneous wafer bonding due to the lower diffusion rate of misfit dislocations (MDs) at the Ge/Si bonded interface. This is very different from that in epitaxial growth, in which high-density TDs form in the integrated Ge layer due to the threading of MDs at high-temperature. In this paper, we review on the wafer bonding of Si-based semiconductors based on different bonding methods. The advantages and disadvantages of different bonding methods are pointed out for comparisons. We focus on the illustration of the fabrication of Si/Si and Ge/Si wafer pairs with TD-free, bubble-free, and oxide-layer-free bonded interfaces. Finally, the outlook for the development of Si/Si and Ge/Si wafer bonding and devices based on the wafer bonding technique is carried out. We trust that this work may provide guidance for low-temperature heterogeneous hybrid integration of different group materials with ultrahigh lattice mismatch, such as GeSn on Si and III-V materials on Si.

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2  
3 **Keywords:** Wafer bonding, hydrophilic reaction, oxide layer, bonding strength, bubbles, on/off ratio  
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## 1.1 Introduction

9 With the development of microelectronics [1-5] and optoelectronics [6-10], the  
10 information era and the big data era have been arrived successively on schedule. It is worth  
11 mentioning that the Moore's law [11-15] has been proposed for over 50 years. Although many  
12 people attempted to predict the end date of this amazing law in these years for many times, new  
13 revolutionary techniques, such as the fin field-effect transistor (FinFET) technique [16-18],  
14 fully-depleted silicon-on-insulator (FD-SOI) technique [19-21], and gate-all-around (GAA)  
15 technique [22-24], were proposed to continue this law as expected. However, the number of  
16 transistors on chip is impossible to increase indefinitely due to the fact that the size of the  
17 transistor is impossible to decrease indefinitely. The main factor limits the decrease of the size  
18 of the transistor is suggested to be the physical difficulty in the Si-based fabrication process  
19 [25-27]. When the channel length of the transistor decreases to several nanometers, the  
20 thickness of the gate oxide decreases to several atomic layers. The electrical characteristics of  
21 the small transistor is difficult to control due to the increase of the leakage current induced by  
22 the quantum tunneling effect [28-30]. However, further decrease in the size of the transistor is  
23 an important issue for the development of the integrated circuit.

38 The development of the Si complementary metal oxide semiconductor (CMOS) circuit  
39 triggers the investigation of Micro-Electro-Mechanical Systems (MEMS) [31-33]. MEMS is  
40 the micro-system which contains several micromodule (micro-device), such as power source,  
41 sensor, control circuit, and processor. At present, MEMS has a wide range of applications in the  
42 field of material science, energy science, biomedicine etc [34-37]. The development of MEMS  
43 is accompanied by the rise of the study of MEMS packaging techniques. The packaging of  
44 MEMS not only can protect the micro-device from mechanical damages and environmental  
45 damages, but can also solve the problem of the heat dissipation of the chip. Many MEMS  
46 packaging techniques have been proposed to package the micro-system, such as the flip chip  
47 packaging technique [38,39], multichip component technique [40,41], multichip packaging  
48 technique [42,43], wafer level packaging technique [44,45], and three-dimensional (3D)  
49 integration packaging technique [46,47].

The wafer level packaging technique based on the Si/Si wafer bonding, and the 3D integration packaging technique based on the Si/Si wafer bonding and through silicon via (TSV) technique [48-50] are two popular and important packaging techniques for the application of MEMS. Wafer level packaging is commonly used in the vacuum packaging of the MEMS [51-55]. The vacuum packaging based on the Si/Si wafer bonding provides a vacuum cavity for the MEMS device to protect the movable structures in some specific MEMS devices, such as the accelerometer [56,57], gyroscope [58,59], and pressure sensor [60,61]. With the development of the integration of MEMS, the 2D packaging based on the photolithography is unable to meet the market demands due to the fact that the feature size of semiconductor devices reaches its physical limits gradually. That is, the number of the integrated device cannot be further increased in the future. Although some emerging techniques, such as the interposer technique [62-64] to achieve 2.5D packaging and the wire-bonding interconnect technique [65] to achieve quasi-3D packaging, have been proposed to increase the number of the integrated devices, the integration level and the reliability of these techniques need to be further considered. The 3D integration of the MEMS device based on the wafer bonding and TSV technique can achieve a real sense of the device integration in the vertical direction. Overall, the Si/Si wafer bonding plays an important role in the integration of MEMS.

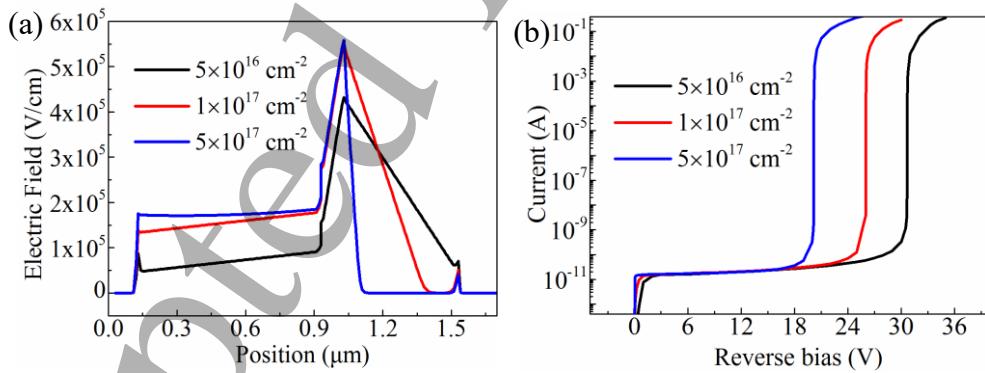


Figure 1. (a) I-V curves and (b) electric fields of the Ge/Si APDs with different doping concentrations of Si avalanche layer.

Furthermore, Si/Si wafer bonding has potential application prospect in the fabrication of photoelectric devices. At present, the fabrication of the Si avalanche layer of Ge/Si avalanche photodiodes (APD) is based on traditional Si/Si homoepitaxy technique [66-69]. Due to the

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existence of lattice vacancies during Si/Si homoepitaxy, the Si avalanche layer commonly exhibits weak n-type doping ( $10^{15}$ - $10^{16}$  cm $^{-3}$ ). In addition, the residual P atom in the pipeline and on the chamber wall (or heater strip) from a previous run can diffuse into the epitaxial intrinsic Si layer during homoepitaxy of intrinsic Si. This leads to high concentration of P atoms ( $10^{17}$  cm $^{-3}$  [70]) in the epitaxial intrinsic Si layer. On the other hand, the Si/Si homoepitaxy commonly carried out at high temperature ( $>850$  °C), thus the P atoms in the heavily-doped Si substrate also can diffuse into the epitaxial intrinsic Si layer due to the high diffusion rate of P atoms in Si [71-73]. When the P concentration in the Si avalanche layer increases, the electric field in the Si avalanche layer decreases and that in the Ge layer increases, as shown in figure 1(a), leading to the pre-breakdown of the device, as shown in figure 1(b). Thus, the fabrication of impurity-free and vacancy-free Si avalanche layer is very important for the achievement of high-performance Ge/Si APD. The potential method for the fabrication of high-quality Si avalanche layer is the low-temperature Si/Si wafer bonding technique and Smart-Cut technique. Based on these two techniques, the quasi-bulk-Si layer can be transferred to the heavily-doped Si substrate at low temperature. Thus, the achievement of the Si/Si bonded interface which shows perfect electrical properties is also very important.

On the other hand, in the past few years, Ge/Si photoelectric devices drew researcher's attentions due to the fact that these devices not only can respond to infrared light, but they can be directly integrated with the CMOS circuit. As we all know that the fabrication of Ge/Si photoelectric devices is based on the traditional and mature epitaxial technique, such as the reduced pressure chemical vapor deposition (RPCVD) [74,75], ultra-high vacuum chemical vapor deposition (UHV-CVD) [76,77], and molecular beam epitaxy (MBE) [78,79]. However, epitaxial growth of Ge film by these devices commonly requires ultrahigh vacuum ( $10^{-8}$  Pa) and high temperature (600-800 °C). In addition, the Ge/Si heterogeneous epitaxial growth produces high-density threading dislocations (TDs) ( $10^8$ - $10^9$  cm $^{-2}$  [80,81]) in Ge film due to 4.2% lattice mismatch between Ge and Si. Furthermore, after Ge growth, high-temperature cyclic annealing (700-900 °C) should be carried out to decrease the TD density (TDD) to  $10^6$ - $10^7$  cm $^{-2}$  [82-84]. This may lead to serious Ge/Si intermixing at the Ge/Si interface and the blue shift of the absorption wavelength of the photoelectric devices. It was reported that the TDs in Ge film act as acceptor-like defects at the middle of bandgap [85,86], leading to the increase of the

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4 dark current of the device.  
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6 Many modified Ge/Si epitaxial methods were proposed to decrease the TDD, such as the  
7 two-step Ge layer growth [87], Ge/SiGe multiple quantum well segregation [88,89], graded  
8 SiGe buffer layer growth [90], and selective growth [91,92]. It was reported that each method  
9 can lead to the decrease of the TDD to  $10^6 \text{ cm}^{-2}$ . However, the dark current density of the Ge/Si  
10 photoelectric devices based on these epitaxial methods is still too high ( $10\text{-}50 \text{ mA/cm}^2$  [93-100])  
11 due to the fact that the distribution of the TDs is nonuniform in the epitaxial Ge film. It was  
12 reported in our previous works [80] that the TDD near the Ge/Si interface (within 100 nm) is  
13 as high as  $>10^8 \text{ cm}^{-2}$ . With the increase of Ge film thickness, the TDD decreases. Thus, further  
14 lowering the epitaxial growth temperature to  $<400^\circ\text{C}$  and the TD density to  $<10^5 \text{ cm}^{-2}$  are two  
15 challenges for heterogeneous Ge/Si epitaxial growth. However, it is obvious that these two  
16 indicators are too difficult to be achieved for Ge/Si epitaxial growth due to the fact that the  
17 quality of epitaxial Ge film is low when lower epitaxial temperature was applied and the  
18 epitaxial growth process cannot avoid the 4.2% lattice mismatch. One potential method for  
19 further decreasing the TDD is the heterogeneous Ge/Si wafer bonding and Smart Cut™  
20 technique. It was reported that low-temperature Ge/Si wafer bonding can eliminate the TDs in  
21 Si-based Ge film. The Ge/Si wafer bonding and Smart Cut™ technique are considered to be an  
22 alternative for the Ge/Si epitaxial growth and the fabrication of Ge/Si photoelectric devices.  
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25 As described above, the Si/Si wafer bonding and Ge/Si wafer bonding are two important  
26 techniques for improving of the quality of the Si avalanche layer and the elimination of TDs in  
27 Si-based Ge film, respectively. In this paper, we review the progress of Si/Si wafer bonding and  
28 Ge/Si wafer bonding to provide guidance for further understanding the importance of Si-based  
29 wafer bonding techniques in microelectronics and optoelectronics.  
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## 32 **1.2 Progress of Si/Si wafer bonding**

33 The investigation of Si/Si wafer bonding starts from the direct bonding technique proposed  
34 by Shimbo et al. in 1986 [101]. Comparing to the epitaxial growth technique and ion  
35 implantation technique in the semiconductor fabrication process, the Si/Si wafer bonding  
36 technique was receiving more and more attentions in the field of MEMS and photoelectric  
37 devices because of its unique advantages. The most popular and common Si/Si wafer bonding  
38 method is the direct wafer bonding. Two Si wafers with the root-mean-square (RMS) below 0.5  
39

nm can direct contact to each other in the atmosphere or in the vacuum without the bonder or metal transition layer after cleaning of the wafers. Then post-annealing of the contacted wafers was conducted to enhance the bonding strength. The popular methods for Si/Si wafer bonding can be concluded into the wet chemical surface-activated bonding, plasma-activated bonding, high-vacuum surface-activated bonding, ultraviolet-activated bonding, and semiconductor interlayer bonding.

### 1.2.1 Wet chemical surface-activated method

The wet chemical surface-activated method contains two techniques. The one is the wet chemical hydrophilic bonding and the other is the wet chemical hydrophobic bonding. For wet chemical hydrophilic bonding, during the RCA cleaning of Si wafers, each cleaning step can activate the Si surface due to the introduction of  $\text{H}_2\text{O}_2$ , leading to the formation of a thin  $\text{SiO}_2$  layer on the Si surface. The existence of the  $\text{SiO}_2$  layer represents the hydrophilicity of the Si surface. For wet chemical hydrophobic bonding, H bonds should be introduced to passivate the Si surface. Commonly, the treatment of the HF solution of cleaned Si surface can achieve the H bond passivation.

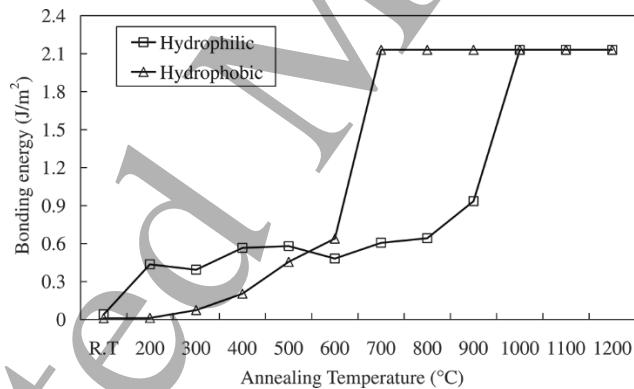


Figure 2. Bonding energy as a function of annealing temperature for hydrophilic and hydrophobic direct Si wafer bonding. Reprinted figure from [102], with the permission of IOP Publishing.

Toyoda et al. [102] and Plach et al. [103] systematically investigate the wet chemical surface-activated method for Si/Si wafer bonding. For hydrophilic and hydrophobic bonding, the  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:10:60$  solution and the 5% HF solution were used to activate the Si surface, respectively. The effect of the annealing temperature on the bonding energy of bonded

Si wafers in these two methods is shown in figure 2. One can see that the bonding energy of Si wafer pairs increases with the increase of the annealing temperature. The annealing of the wafer pairs at 1000 °C should be carried out for the achievement of high bonding energy of 2.1 J/m<sup>2</sup> for hydrophilic bonding, while that was achieved when the annealing temperature of 700 °C was carried out for hydrophobic bonding. Note that the bond energy of -OH groups is stronger than that of -H groups, thus hydrophilic bonding is easier to achieve than hydrophobic bonding.

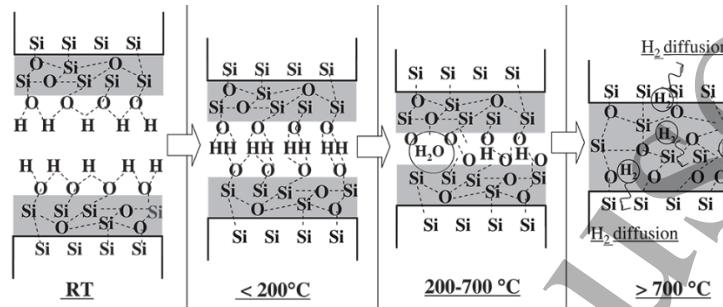


Figure 3. Bonding mechanism of hydrophilic direct Si wafer bonding. Reprinted figure from [102], with the permission of IOP Publishing.

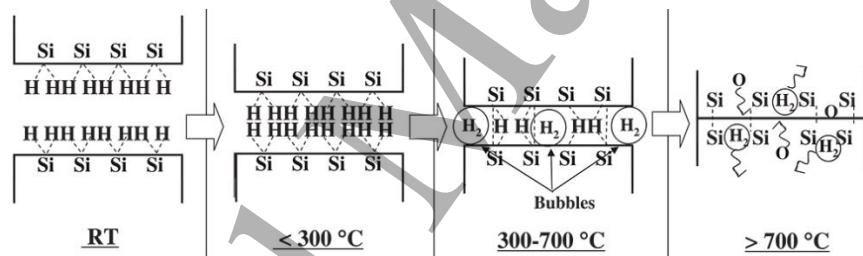


Figure 4. Bonding mechanism of hydrophobic direct Si wafer bonding. Reprinted figure from [102], with the permission of IOP Publishing.

The bonding mechanism of hydrophilic bonding is shown in figure 3. One can see that H bonding occurs at the interface when the temperature is below 200 °C. In addition, the S-O-Si bonds and H<sub>2</sub>O bubbles begin to form at the bonded interface when the temperature is above 200 °C. Note that when the temperature was increased to >700 °C, the hydrophilic reaction ( $\text{Si}+2\text{H}_2\text{O}=\text{SiO}_2+2\text{H}_2$ ) occurs, the H<sub>2</sub>O bubbles at the bonded interface turn into H<sub>2</sub> bubbles. Finally, H<sub>2</sub> gas diffuses into the Si wafer when the temperature was increased to >900 °C, leading to the disappearance of H<sub>2</sub> bubbles.

For hydrophobic bonding, as shown in figure 4, when the wafer pairs were annealed at

<300 °C, the wafers were weakly held by van der waals force. When the temperature was increased to >300 °C, the Si-H<sub>2</sub> bond converts into Si-H bond and H<sub>2</sub>, and the Si-Si bond begins to form. When rising the temperature to >700 °C, the H<sub>2</sub> begins to diffuse into Si wafers, resulting in the disappearance of H<sub>2</sub> bubbles. TEM images of bonding interfaces are shown in figure 5. One can see that an obvious oxide layer appears at the bonded interface for hydrophilic direct bonding due to the hydrophilic reaction at the bonded interface. However, the oxide clusters appear at the bonding interface due to the aggregation of O atoms in the Si wafer at the bonded interface.

Overall, hydrophilic and hydrophobic direct wafer bonding are two easy methods for Si/Si wafer bonding. Both methods can achieve high bonding strength of Si wafer pairs and bubble-free bonded interfaces. However, the annealing temperature of wafer pairs should be high enough. In addition, the oxide layer originates from the hydrophilic reaction and the oxide clusters originate from the aggregation of O atoms are difficult to be eliminated.

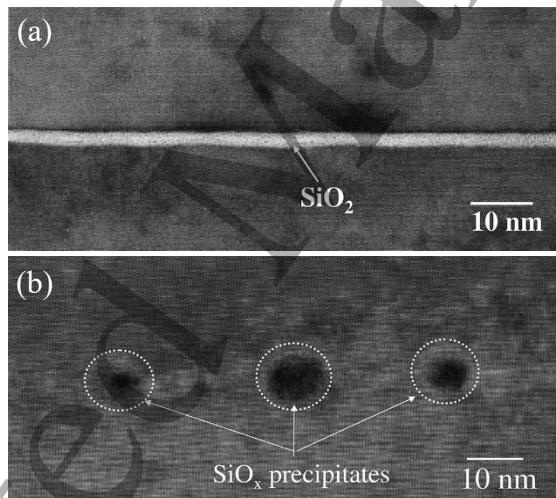


Figure 5. TEM images of the bonding interfaces. Reprinted figure from [102], with the permission of IOP Publishing. (a) Hydrophilic direct wafer bonding and (b) hydrophobic direct wafer bonding.

### 1.2.2 Plasma-activated bonding

As described above, the annealing temperature of Si/Si wafer pairs should be increased to at least 700 °C to enhance the Si/Si bonding strength which is close to the fracture strength of the bulk Si for wet chemical surface-activated bonding. However, for the packaging of MEMS

and the prevention of the diffusion of impurities in the substrate into the intrinsic layer, the bonding temperature of Si wafer pairs should be decreased to  $\leq 400$  °C. In order to decrease the annealing temperature of Si wafer pairs, some researchers propose to introduce plasmas for the activation of the Si surface. Howlader et al. and Suga et al. [104-110] systematically studied the effect of sequential plasma activation on the bonding strength, bubble density, bonded interface, and electrical properties of Si bonded wafer pairs. The plasmas used in the experiment are the O plasma in the RIE system and the N microwave plasma radicals. The surface treatment process is shown in figure 6. Firstly, the Si wafer surface was exposed to the O plasma, and then the wafers were treated with N microwave plasma radicals. After that, the treated Si wafers were contacted to achieve the pre-bonding of the wafer pairs.

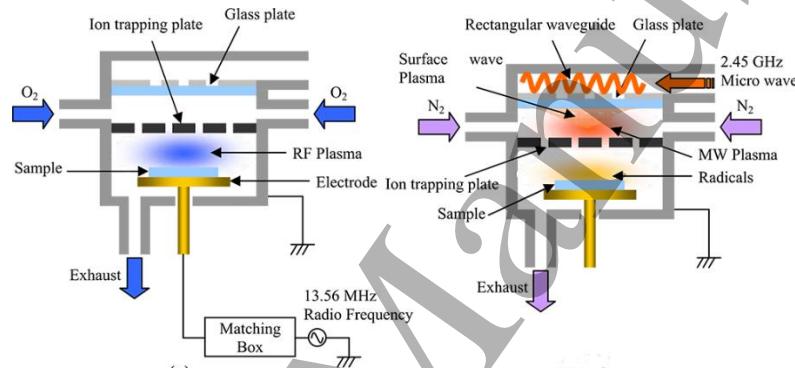


Figure 6. Schematic diagram of the sequential plasma-activated bonding. Reprinted figure from [104], with the permission of IOP Publishing.

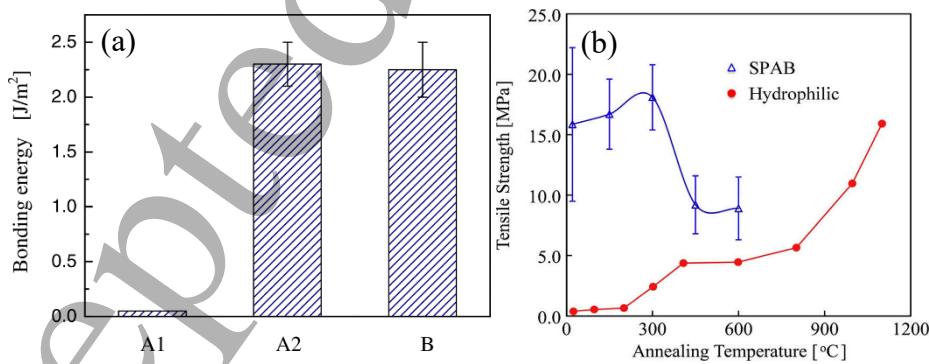


Figure 7. (a) Bonding energy versus stored time of the bonded wafer pairs. Reprinted figure from [104], with the permission of IOP Publishing. (b) Bonding strength versus annealing temperature for sequential plasma-activated bonding and hydrophilic direct bonding.

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Note that, as shown in figure 7(a), when the wafers were just contacted to each other, the low bonding energy of  $\sim 0.2 \text{ J/m}^2$  was achieved. However, when the wafer pairs were stored in air for 24 h, the bonding energy increases to  $\sim 2.2 \text{ J/m}^2$ . This is attributed to the formation of Si-O-Si bonds at the Si/Si bonding interface during the storing of the wafer pairs. The bonding mechanism of the sequential plasma activation method can be concluded as follow. Firstly, the O plasma treatment in the RIE system, which is similar to the O ion bombardment process, can remove the contaminations on the Si surface and forms a porous oxide layer on the Si surface. These porous structures are beneficial to the migration of  $\text{H}_2\text{O}$  and  $\text{H}_2$ . After that, the Si surface was treated by energy-free N microwave plasma radicals to produce a chemical-metastable oxynitride thin film on the Si surface. Thus, the Si surface after the O and N plasma treatment becomes extremely hydrophilic. Some  $\text{H}_2\text{O}$  molecules can diffuse into this oxynitride to form the Si-O-Si bonds, resulting in the increase of the bonding strength at room temperature.

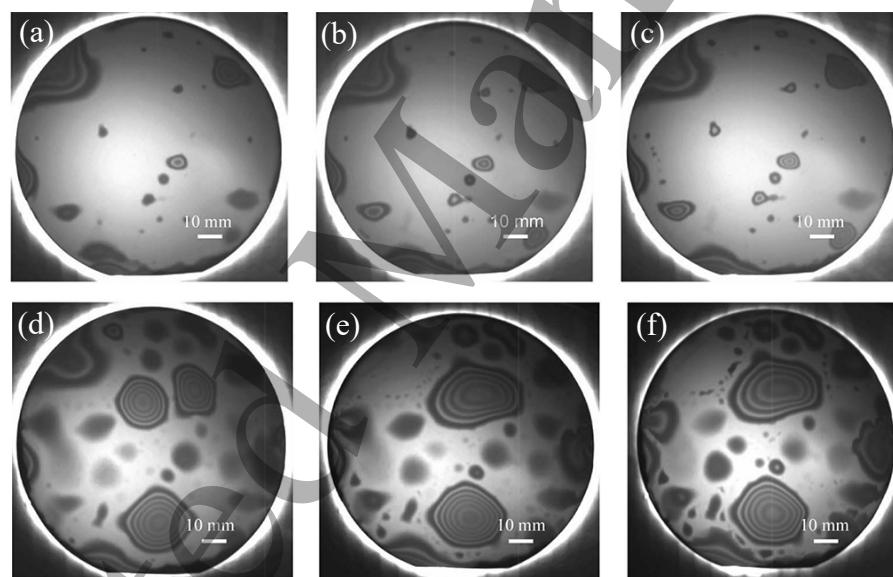


Figure 8. (a)-(f) Infrared images of the Si/Si bonded interfaces annealed at 100 °C, 200 °C, 300 °C, 400 °C, 500 °C, and 600 °C. Reprinted from [105], with the permission of IEEE Xplore Digital Library.

The temperature dependence of the bonding strength of the wafer pairs is shown in figure 7(b). One can see that for wet chemical hydrophilic bonding, the bonding strength of  $\sim 16 \text{ MPa}$  was achieved when the temperature reaches 1100 °C. However, for sequential plasma activation method, the bonding strength of  $\sim 16 \text{ MPa}$  was achieved at room temperature. However, with

the increase in annealing temperature, the bonding strength slightly increases at first, and then decreases. This feature can be explained by the increase of the bubble density at the bonded interface, as shown in figure 8.

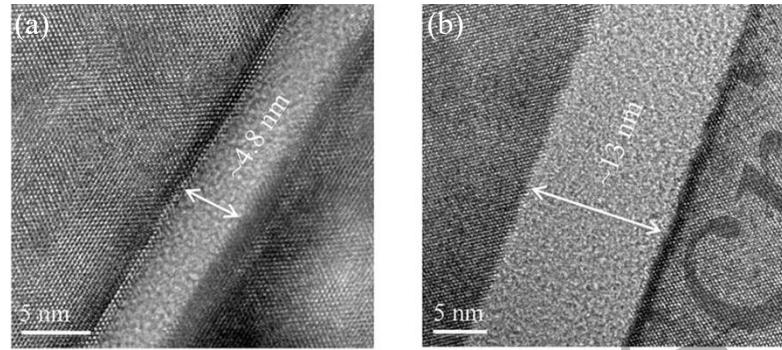


Figure 9. TEM images of Si/Si bonded interfaces (a) before annealed and (b) after annealed at 600 °C. Reprinted figure from [106], with the permission of IOP Publishing.

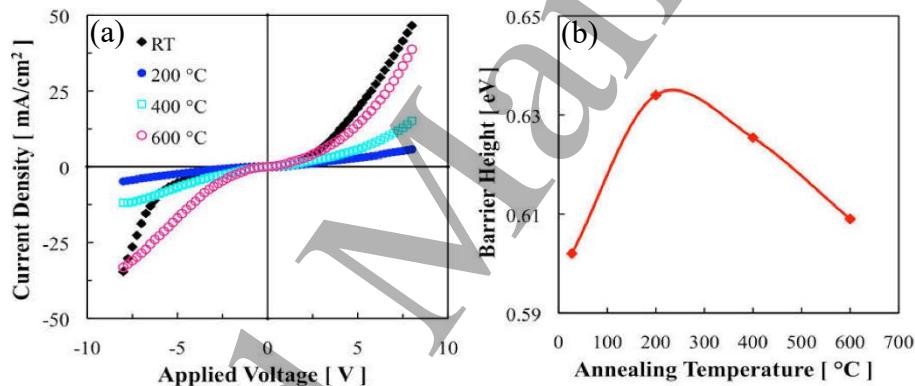


Figure 10. (a) I-V curves of the bonded wafer pairs annealed at different temperatures. Reprinted figure from [106], with the permission of IOP Publishing. (b) Barrier height at the bonded interface verse annealing temperature. Reprinted figure from [106], with the permission of IOP Publishing.

This is a common phenomenon for hydrophilic wafer bonding and due to the increase of hydrophilic reactions at the bonded interface when higher annealing temperature was applied, leading to the decrease of the bonding strength of the wafer pairs. In other words, the Si/Si wafer pairs produced by sequential plasma-activated bonding cannot suffer from high-temperature annealing. On the other hand, with the increase of the annealing temperature, the oxide layer thickness at the bonded interface increases, as shown in figure 9. When the

temperature increases to 600 °C, the oxide layer thickness reaches ~13 nm. This is also attributed to the serious hydrophilic reaction at the bonded interface. The existence of the oxide layer at the bonded interface produce a high barrier at the bonded interface, leading to the nonlinearity of the I-V curves, as shown in figure 10.

Overall, the sequential plasma-activated bonding can achieve a high bonding strength of the Si/Si wafer pairs and a near-bubble-free bonded interface at room temperature due to the appearance of the chemical bonds at the bonded interface after storing. However, with the increase of the annealing temperature, the bubble density increases, leading to the decrease of the bonding strength. In addition, with the increase of the annealing temperature, the oxide layer thickness at the bonded interface increases, leading to the nonlinearity of the I-V curves. That is, the transport of the carriers at the bonded interface is restrained by the interface barrier.

### 1.2.3 High-vacuum surface-activated bonding

As illustrated above, chemical reactions occur at the Si/Si bonded interface in the wet chemical surface activation and plasma surface activation due to the introduction of -OH and -H groups on the Si surface to enhance the bonding strength. The bonding of the wafers in these two methods are in the atmosphere. The absorption of -OH groups in the atmosphere cannot be avoided. In order to eliminate the -OH groups on the Si surface completely, high-vacuum surface-activated bonding was proposed. The surface-activated bonding was conducted in high vacuum. Thus, the molecules in the atmosphere cannot absorb on the Si surface after the surface activation. The surface-activated bonding process is shown in figure 11. Firstly, Si wafers were loaded into the vacuum chamber after cleaning. Note that an oxide layer and adsorbed molecules exist on the Si surface after cleaning. Ar atom beam etching was carried out when the pressure of the vacuum chamber decreases to  $<5\times10^{-5}$  Pa to activate the Si surface. The surface oxide layer and adsorbed molecules can be totally removed after Ar atom beam treatment, leaving Si dangling bonds on the Si surface. The Si surface is difficult to be reoxidized in high-vacuum atmosphere. Thus, the Si surface can maintain high activity to achieve bonding of Si dangling bonds. Finally, the treated Si wafers were directly bonded by the Si-Si bonds, achieving high bonding strength.

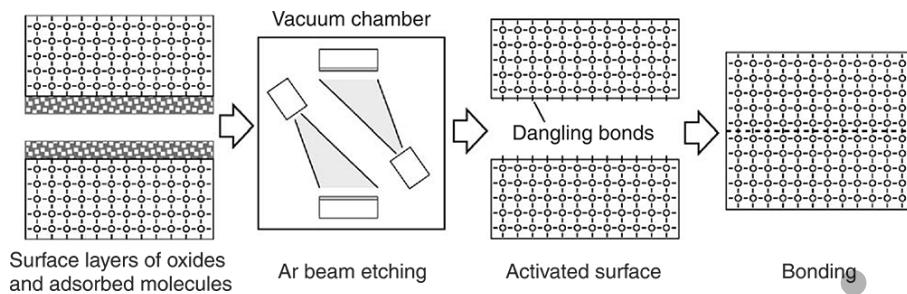


Figure 11. Bonding process of the high-vacuum surface-activated bonding. Reprinted figure from [111], with the permission of Elsevier.

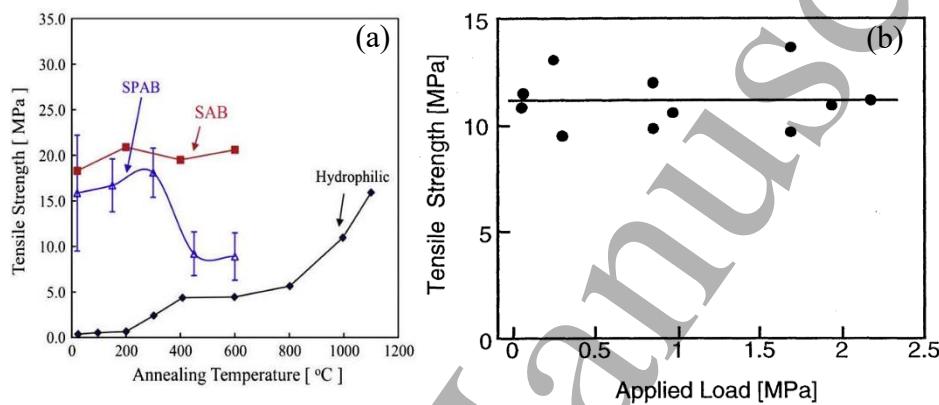


Figure 12. (a) Bonding strength versus annealing temperature. Reprinted figure from [112], with the permission of Elsevier. (b) Bonding strength versus applied load. Reprinted figure from [113], with the permission of IOP Publishing.

Suga et al. [111-117] started to investigate Si/Si wafer bonding using high-vacuum surface-activated bonding from 1990s. They not only studied the effect of different conditions, such as the annealing temperature, processing time of the Ar atom, and vacuum degree, on the bonding quality of Si/Si wafer pairs, but also achieved Ge/Ge [118] and GaAs/Si wafer bonding [119] by this method. For Si/Si wafer bonding, they revealed the dependence of bonding strength on the annealing temperature, as shown in figure 12(a). One can see that the bonding strength of the wafer pairs fabricated by this method is larger than that fabricated by wet chemical surface-activated bonding and plasma surface-activated bonding. This indicates that the bond energy of the Si-Si bond is higher than that of the Si-O-Si bond. With the increase in annealing temperature, the decrease of the bonding strength was not observed. The bonding strength can reach ~18 Mpa when the treated wafers were direct contacted at room temperature. This is

ascribed to the fact that only Si-Si bonds form at the Si/Si bonded interface, other elements were not introduced. Thus, with the increase of the temperature, chemical reactions are absent at the bonded interface, leading to the stabilization of the bonding strength.

They also studied the effect of the pressure applied on the wafer pairs on the bonding strength, as shown in figure 12(b). One can see that the bonding strength of the wafer pairs is almost unchanged with the increase in applied load. This implies that once the activated Si wafers were contacted together, high bonding strength can be achieved without the applied load. Figure 13(a) shows the effect of the etching time of the Ar beam on the bonding strength of the wafer pairs. It is shown that the bonding strength increases at first, then stabilizes at  $\sim 12$  MPa, and finally decreases with the increase in etching time. The increase of the bonding strength is due to the activation of the Si surface, while the decrease of the bonding strength results from the increase of the RMS of the Si surface with the increase of the etching time, as shown in figure 13(b).

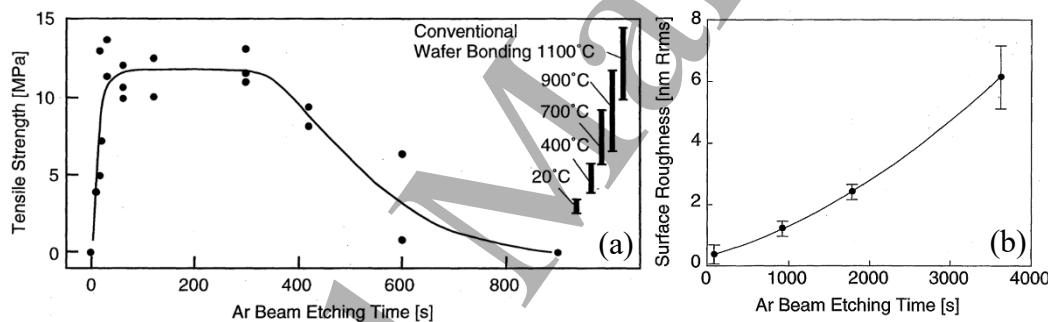


Figure 13. (a) Bonding strength verse Ar beam etching time. Reprinted figure from [113], with the permission of IOP Publishing. (b) Surface roughness verse Ar beam etching time.

Reprinted figure from [113], with the permission of IOP Publishing.

It is known that the vacuum level is an important factor in this method. They also investigated the effect of the vacuum level on the bonding strength and the bubble density. As shown in figure 14(a), the bonding strength increases with the increase of the vacuum level. When the pressure decreases to  $5 \times 10^{-5}$  Pa, the bonding energy of  $2.5 \text{ J/m}^2$  can be achieved. Figure 14 (b) and (c) show infrared images of the wafer pairs bonded in vacuum chamber with a pressure of  $2 \times 10^{-5}$  and  $5 \times 10^{-4}$  Pa, respectively. One can see that no bubbles can be observed at the bonded interface when the pressure was set to  $2 \times 10^{-5}$  Pa, while some bubbles appear at

the bonded interface when the pressure was increased to  $5 \times 10^{-4}$  Pa. This is ascribed to the fact that the particles and molecules were adsorbed on the activated Si surface when the pressure was set to higher value, leading to the appearance of hydrophilic reactions at the bonded interface. Thus, the bubbles appear at the bonded interface. In order to achieve a satisfied Si/Si bonded interface, the pressure of as low as  $10^{-7}$  Pa should be applied.

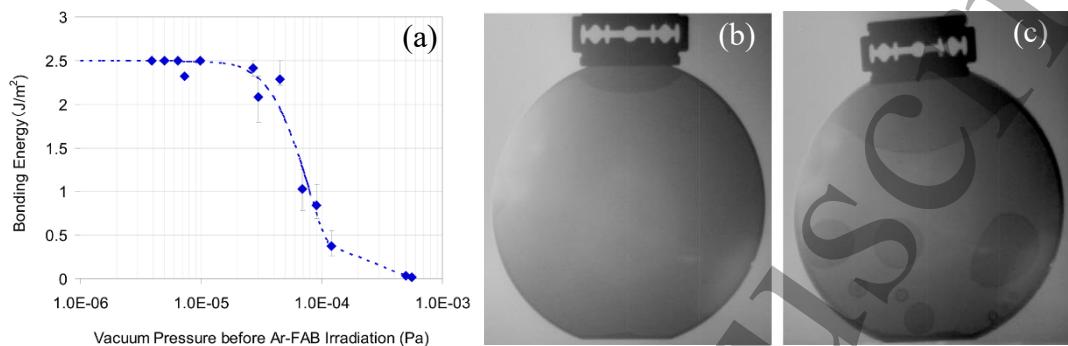


Figure 14. (a) Bonding energy verse vacuum pressure. Reprinted from [114], with the permission of IEEE Xplore Digital Library.. Infrared images of the samples bonded at a pressure of (b)  $2 \times 10^{-5}$  Pa and (c)  $5 \times 10^{-4}$  Pa. Reprinted from [114], with the permission of IEEE Xplore Digital Library.

Note that a thin amorphous Si (a-Si) layer appears at the Si/Si bonded interface after the wafer bonding by this method due to the bombardment effect of the Ar atom beam, as shown in figure 15(a). This is similar to the ion implantation effect. The thin a-Si layer can be totally repaired after annealing at 700 °C for 3 h, as shown in figure 15(b). On the other hand, the n-Si/n-Si junction fabricated by this method can achieve linear electrical property at room temperature, as shown in figure 15(c). However, the current densities of the n-Si/n-Si and p-Si/p-Si junctions irregularly change with the increase of the annealing temperature, as shown in figure 15(d) and (e). The potential barrier at the bonded interface is shown in figure 15(f). One can see that the potential barrier of the n-Si/n-Si junction is smaller than that of the p-Si/p-Si junction. In addition, the potential barrier at the bonded interface fabricated by this method is smaller than that fabricated by the plasma-activated method.

Overall, due to the absence of -OH groups adsorbed on the activated Si surface, the oxide layer and the interface bubbles at the bonded interface can be eliminated and high bonding strength can be achieved. However, a thin a-Si layer appears at the bonded interface. High-

temperature annealing ( $700\text{ }^{\circ}\text{C}$ ) should be conducted to repair this layer. In addition, although the linear I-V curve can be achieved for the sample bonded at room temperature, the I-V curve is still sensitive to the annealing temperature. High-temperature annealing should be conducted for achieving low potential barrier height at the bonded interface.

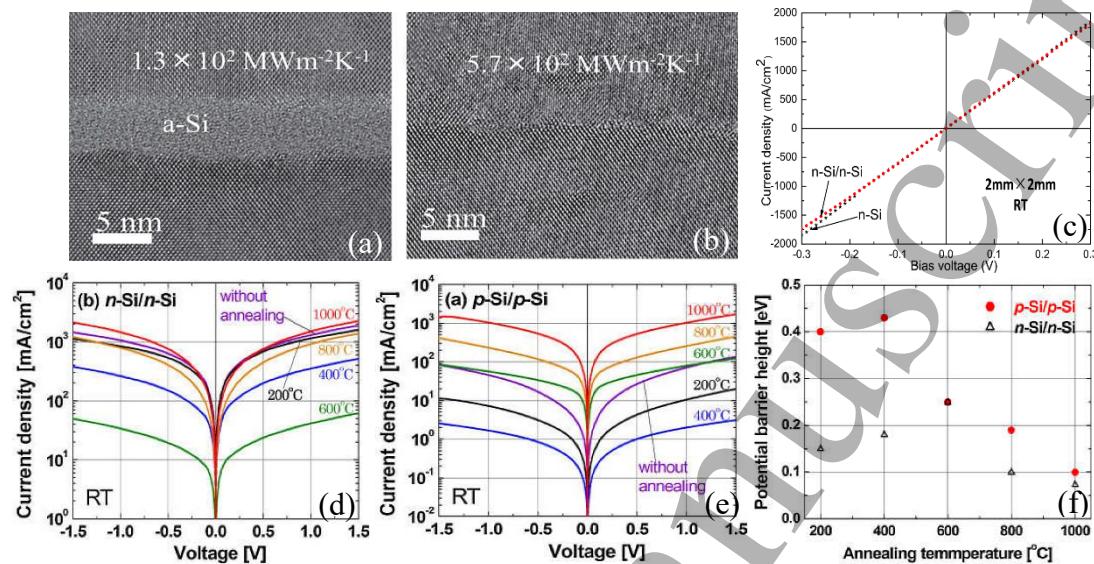


Figure 15. TEM images of the bonded interfaces (a) before annealing and (b) annealed at  $700\text{ }^{\circ}\text{C}$  for 3 h. Reprinted from [115], with the permission of AIP Publishing. I-V curves of (c) the n-Si/n-Si wafer pairs bonded at room temperature. Reprinted from [116], with the permission of AIP Publishing, (d) the n-Si/n-Si wafer pairs annealed at different temperature. Reprinted figure from [117], with the permission of IOP Publishing, and (e) p-Si/p-Si wafer pairs annealed at different temperature. Reprinted figure from [117], with the permission of IOP Publishing. (f) Potential barrier height verse annealing temperature. Reprinted figure from [117], with the permission of IOP Publishing.

#### 1.2.4 Ultraviolet-activated bonding

The dry activation, such as plasma activation and Ar atom beam activation, can lower the annealing temperature of bonded Si wafer pairs. However, as described above, the mechanism for low-temperature Si/Si wafer bonding is different. The ultraviolet (UV)-activated bonding is another low-temperature Si/Si wafer bonding technique. Before Si/Si wafer bonding, the Si wafers were exposed to the UV light to activate the Si surface. The Si surface is extremely hydrophilic after activation. The mechanism for the UV-activated bonding can be concluded

into two parts, surface cleaning and surface activation. The UV irradiation can further clean the Si surface, as shown in figure 16. Some organic molecules may absorb on the Si surface after wet cleaning. When the UV irradiation with the wavelength of 185 nm was conducted on the Si surface, the C-C bonds and C=C bonds in hydrocarbon break to form ions, free atoms, and active molecules. On the other hand, the UV irradiation (185 nm) can decompose O<sub>2</sub> into O<sub>3</sub> and O (2O<sub>2</sub>=O<sub>3</sub>+O). The O<sub>3</sub> can be absorbed again by UV irradiation with the wavelength of 254 nm to form the O<sub>2</sub> and O. This continuous photosensitized reaction leads to the increase of active O atoms on the Si surface. The O atoms bond with the C atoms to form CO<sub>2</sub> and CO, leading to cleaning of the Si surface.

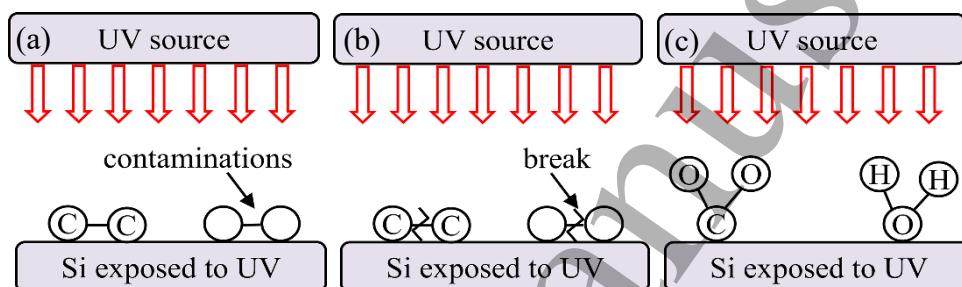


Figure 16. Mechanism of UV surface cleaning. (a) UV radiation forms active O atoms. (b) UV radiation breaks down hydrocarbon contaminations on wafer surface. (c) Gaseous byproducts form and escape from the surface. Reprinted figure from [120], with the permission of Springer.

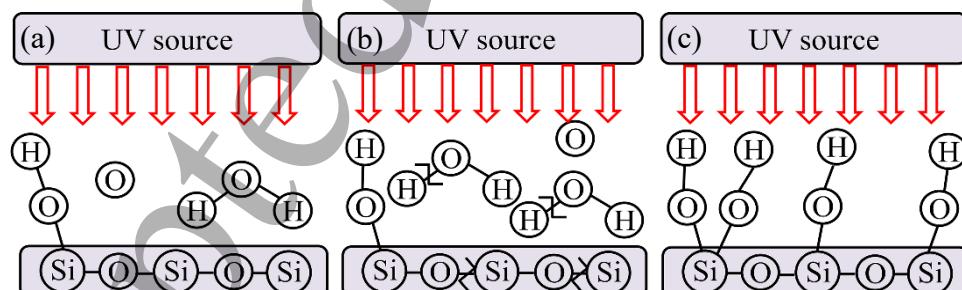


Figure 17. Mechanism of UV surface modification. (a) UV exposure on the silicon surface. (b) UV radiation breaks down H<sub>2</sub>O and Si-O-Si, then forms H-, -OH, Si- and Si-O-. (c) Silicon surface acquires considerable Si-OH and becomes hydrophilic. Reprinted figure from [120], with the permission of Springer.

The UV irradiation can activate the Si surface, as shown in figure 17. High-energy UV

irradiation can break the bonds of water molecules to form -OH and -H bonds on the Si surface. The -H bonds can further bond with the surrounding O atoms to form -OH bonds. In addition, the UV irradiation can break the Si-O bonds in the Si oxide to form Si- and Si-O-bonds, then the Si- bonds can bond with the -OH bands to form Si-OH bonds and the Si-O- bonds can bond with the -H bonds to form Si-OH bonds, leading to the increase of the hydrophilia of the Si surface.

Shi et al. and Kub et al. [120-124] systematically studied the effect of UV irradiation on the Si/Si wafer bonding. The effect of UV irradiation time on the RMS of the Si surface and the bonding strength was investigated, as shown in figure 18. One can see that when the UV irradiation time of 5 min was applied, the RMS of the Si surface reaches lowest value and the bonding strength reaches highest value (~15 MPa). With the increase of UV irradiation time, the RMS increases and the bonding strength decreases. This is similar to that in high-vacuum surface-activated bonding. They also studied the dependence of bubble density on the UV irradiation time, as shown in figure 19. It is shown that no bubbles were observed in the infrared image when the UV irradiation time of 5 min was applied. When increasing the irradiation time to 10 min, some bubbles appear at the bonded interface. This may be due to the increase of the RMS, as shown in figure 18(a).

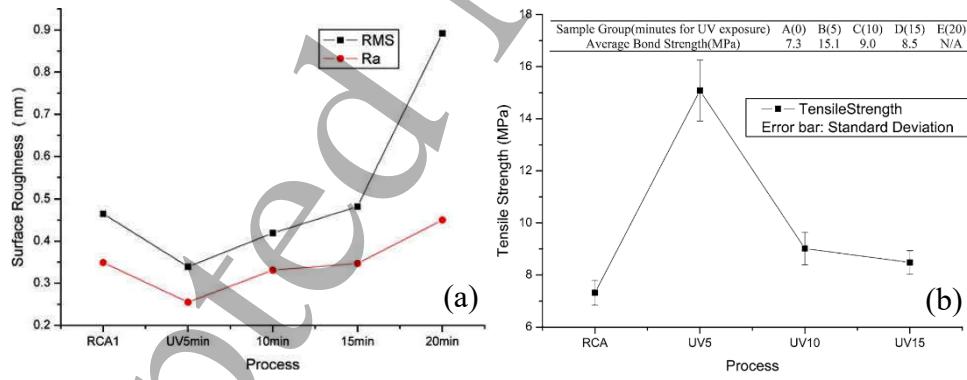


Figure 18. (a) Surface roughness verse UV exposure time. Reprinted figure from [120], with the permission of Springer. (b) Bonding strength verse UV exposure time. Reprinted figure from [120], with the permission of Springer.

The bonding strength as a function of the annealing temperature and the annealing time is shown in figure 20. One can see that the bonding strength increases with the increase of the annealing temperature. This is explained by the increase of the Si-O-Si bonds formed by the

hydrophilic reaction at the bonding interface when higher temperature was applied. In addition, the bonding strength increases at first, and then tends to be stable with the increase of the annealing time. The increase of the bonding strength at first is attributed to the increase of the hydrophilic reaction when short-time annealing was conducted, while the stabilization of the bonding strength is due to the absence of the hydrophilic reaction when long-time annealing was conducted.

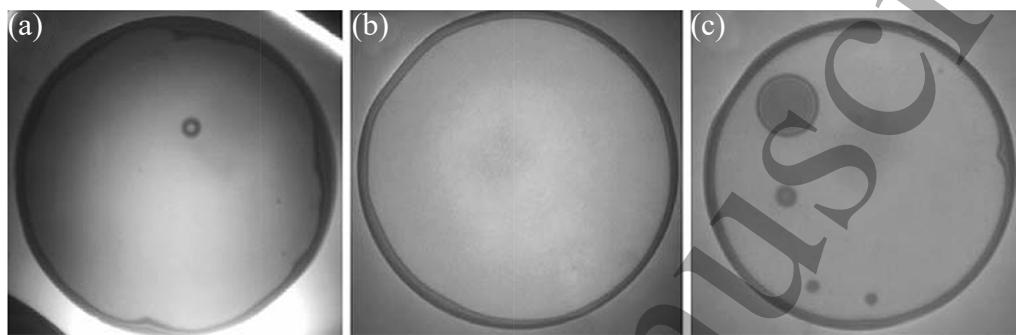


Figure 19. Infrared images of the bonded samples (a) without UV irradiation, (b) with UV irradiation for 5 min, and (c) with UV irradiation for 10 min. Reprinted figure from [120], with the permission of Springer.

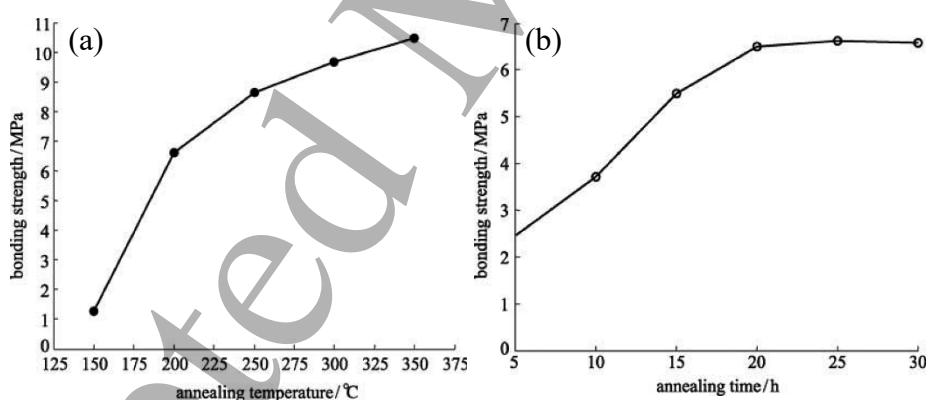


Figure 20. (a) Bonding strength versus annealing temperature. Reprinted figure from [121], with the permission of Springer. (b) Bonding strength versus annealing time. Reprinted figure from [121], with the permission of Springer.

Figure 21(a) and (b) show scanning acoustic microscope (SAM) images of bonded interfaces with and without UV irradiation for 5 min, respectively. It is important to note that although the infrared images show that no bubbles were observed at the bonded interface when

the UV irradiation time of 5 min was applied, the SAM images show that some small bubbles still exist at the bonded interface. This indicates that the resolution of SAM is higher than that of infrared transmission. It is more suitable to evaluate interface bubbles using SAM. One can see that the bubbles in the sample with UV irradiation are smaller than that in the sample without UV irradiation. On the other hand, although the authors did not show the TEM image of the bonded interface, we can speculate that the bonding interface contains oxide layer due to the fact that the UV-activated method is a hydrophilic bonding method, the Si-O-Si always exists at the bonded interface.

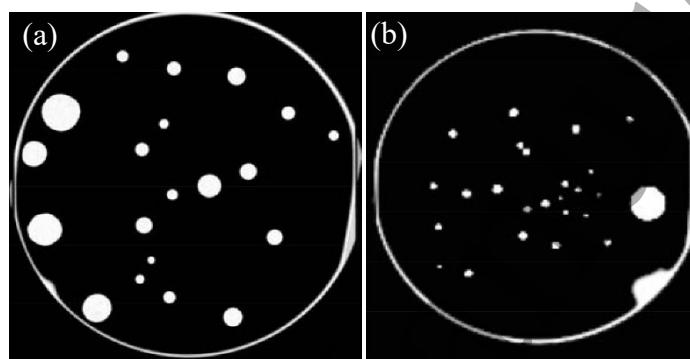


Figure 21. Scanning acoustic microscopy images of the bonded interfaces (a) without UV radiation and (b) with UV radiation for 5 min. Reprinted figure from [122], with the permission of IOP Publishing.

### 1.2.5 Semiconductor interlayer bonding

In order to achieve a real bubble-free bonded interface, some researchers try to construct a porous semiconductor interlayer between two Si wafers to exhaust by-products produced at the bonded interface. This is so-called semiconductor interlayer bonding. In this method, a smooth semiconductor interlayer, which is formed by the film deposition, ion implantation, or ion etching, was inserted between two Si wafers to achieve interlayer bonding. Tong et al. [125] and our colleagues [126-130] systematically studied Si/Si wafer bonding based on the a-Si layer and amorphous Ge (a-Ge), respectively. Tong et al. studied the effect of the a-Si interlayer fabricated by sputtering, ion implantation, RIE etching, and  $\text{B}_2\text{H}_6$  plasma treatment on the bonding strength and interface characteristics of Si/Si wafer pairs. The HF solution was used to achieve hydrophobic bonding. As described above, the annealing temperature for hydrophobic bonding should be increased to  $>700$  °C for the achievement of high bonding strength. Thus,

in order to lower the annealing temperature of Si/Si hydrophobic bonding, the dehydrogenation of the Si surface was carried out at low temperature. Ref. [131,132] reported that the H atoms on the a-Si surface can be released at a lower temperature ( $200\text{ }^{\circ}\text{C}$ ) than that on the bulk Si surface ( $300\text{ }^{\circ}\text{C}$ ). Thus, the Si wafer bonding based on a-Si can be achieved at a lower temperature. On the other hand, the a-Si exhibits porous structure, it can absorb and release H atoms when post-annealing was conducted.

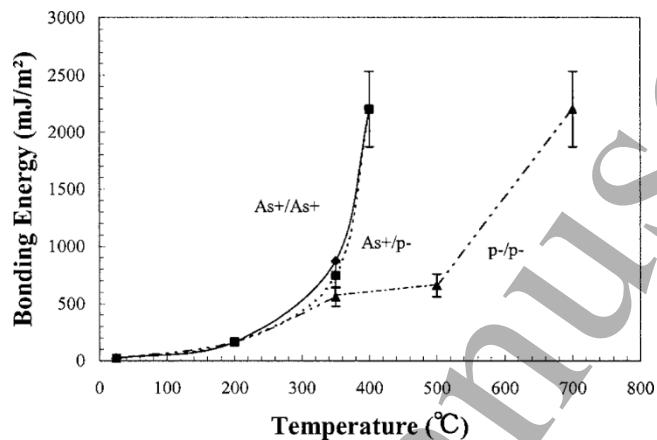


Figure 22. Bonding energy verse annealing temperature. Reprinted from [125], with the permission of AIP Publishing.

Firstly, the  $\text{As}^{+}$  implantation was applied to form 150 nm thick a-Si layer on the Si surface. The ion implantation of one wafer and two wafers were both conducted for wafer bonding. The bonding energy as a function of the annealing temperature is shown in figure 22. One can see that for direct wafer bonding, the wafer pairs should be annealed at  $700\text{ }^{\circ}\text{C}$  to achieve bonding energy of  $\sim 2.2\text{ J/m}^2$ . However, for the sample with  $\text{As}^{+}$  implantation, only  $400\text{ }^{\circ}\text{C}$ -annealing needs to be applied for the achievement of the bonding energy of  $\sim 2.2\text{ J/m}^2$ . Figure 23(a) shows the TEM image of the bonded interface for the as-bonded sample. The a-Si/a-Si bonded interface can be clearly observed and  $\sim 300$  nm thick a-Si layer exists at the bonded interface. After annealing at  $450\text{ }^{\circ}\text{C}$  for 24 h, as shown in figure 23(b), most of the a-Si has crystallized, leaving  $\sim 10$  nm thick a-Si at the bonded interface. After annealing at  $450\text{ }^{\circ}\text{C}$  for 28 h, the a-Si totally crystallizes (not shown here).

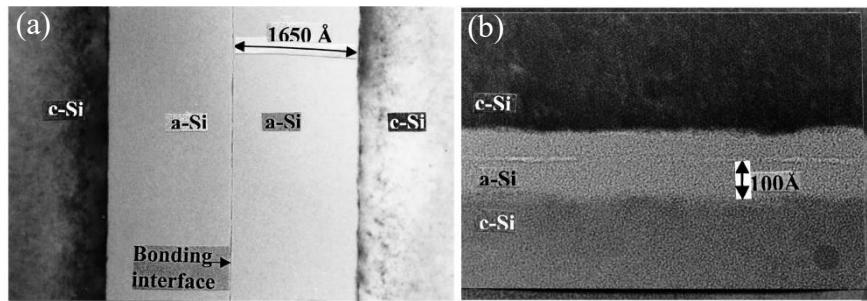


Figure 23. TEM images of the bonded interfaces for (a) the as-bonded sample and (b) the sample further annealed at 450 °C for 24 h. Reprinted from [125], with the permission of AIP Publishing.

They also fabricated a 1  $\mu\text{m}$  thick a-Si layer on the Si wafer by sputtering and CMP technique for wafer bonding. The bonding strength of the Si wafer pairs reaches the fracture strength of bulk Si when the annealing temperature was set to 300 °C. In addition, the bubbles were not observed at the bonded interface due to the absorption of H by a-Si film. This indicates that thick a-Si layer can further decrease the bonding temperature. They also fabricated a 1-3 nm thick a-Si layer on Si by RIE etching for wafer bonding. The annealing temperature of 400 °C needs to be applied to achieve high bonding strength. Finally, the  $\text{B}_2\text{H}_6$  plasma was used to form a 2 nm thick a-Si layer on the Si wafer surface. The effect of the annealing temperature on the bonding strength is shown in figure 24. One can see that the bulk fracture strength can be achieved when the temperature was increased to 350 °C. The lower annealing temperature of the wafer pairs results from the fact that after the treatment of the  $\text{B}_2\text{H}_6$  plasma, the B in Si weaken Si-H<sub>x</sub> bonds, leading to the break of the Si-H<sub>x</sub> bonds at lower temperature.

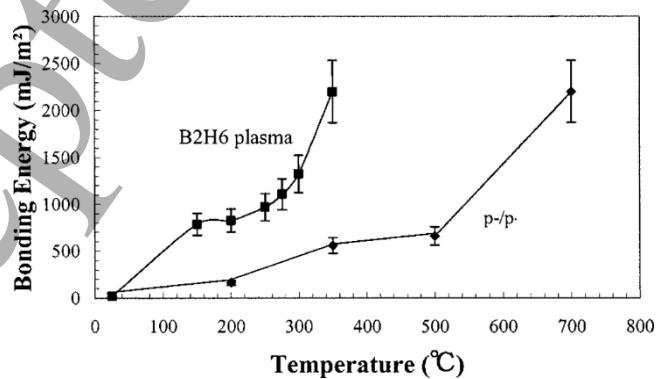


Figure 24. Bonding energy verse annealing temperature. Reprinted from [125], with the permission of AIP Publishing.

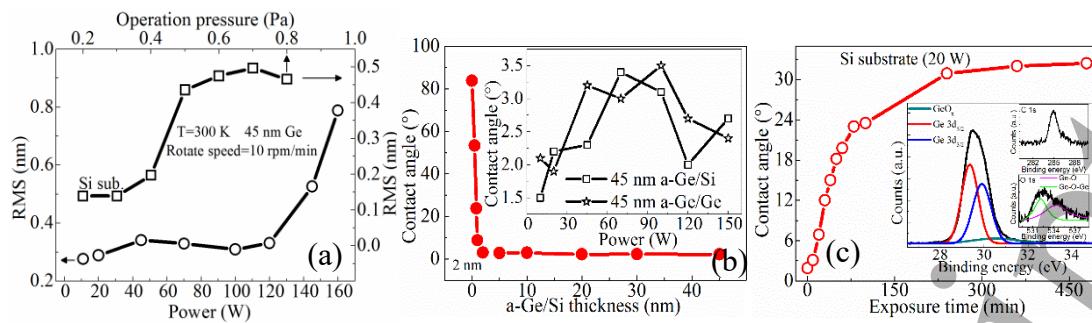
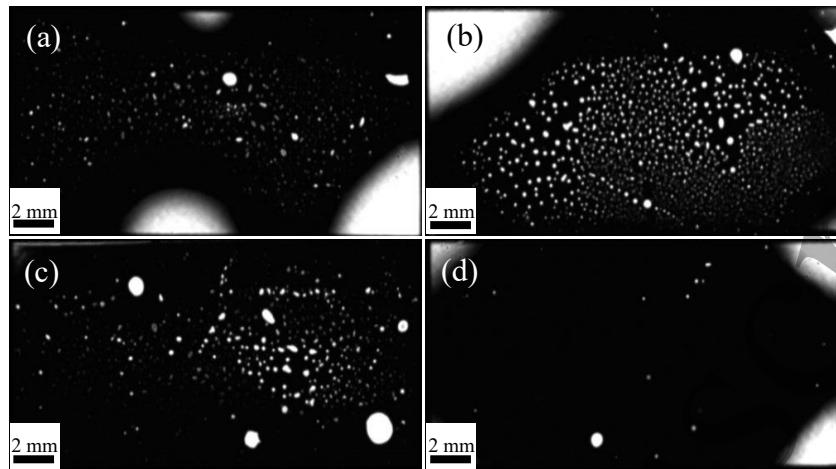


Figure 25. (a) RMS of a-Ge layer verse sputtering power and operation pressure. Reprinted from [126], with the permission of AIP Publishing. (b) Contact angle verse a-Ge layer thickness. Inset shows the contact angle verse sputtering power. Reprinted from [126], with the permission of AIP Publishing. (c) Contact angle verse exposure time. Inset shows the X-ray photoelectron spectroscopy (XPS) curves of the a-Ge surface. Reprinted from [126], with the permission of AIP Publishing.

Our colleagues introduced a thin a-Ge layer between two Si wafers to achieve Si/Si wafer bonding with high bonding strength and bubble-free bonded interface. Firstly, we investigated the RMS of sputtered a-Ge layer on the Si substrate versus input power and operation pressure, as shown in figure 25(a). One can see that the RMS of the a-Ge film is small (<0.4 nm) and is almost changeless at lower power (3-120 W), while it sharply increases at higher power (>120 W). In addition, the RMS of the a-Ge film also shows little change at low pressure, while it sharply increases when the pressure exceeds 0.4 Pa. Finally, the a-Ge film with the RMS of 0.28 nm (power=20 W and pressure=0.3 Pa) was selected for bonding experiments. Before a-Ge wafer bonding, we studied the effect of a-Ge layer thickness on the hydrophilicity of the Ge film, as shown in figure 25(b). One can see that with the increase of a-Ge layer thickness, the contact angle decreases at first, and then trends to be stable (~3°). This indicates that the sputtered a-Ge film (>2 nm) exhibits extremely hydrophilic. The inset shows the effect of sputtering power on contact angle. It can find that the contact angle is changeless with the increase of the sputtering power. We also investigated the contact angle of the a-Ge versus exposure time, as shown in figure 25(c). One can see that with the increase of the exposure time, the contact angle increases, indicating the decrease of the hydrophilicity. This is due to the

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2  
3 oxidation and carbonization of the a-Ge surface when the a-Ge film exposes to the air, as shown  
4 in the inset of figure 25(c).  
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23 Figure 26. SAM images of the Si bonded wafer pairs annealed at (a) 350 °C for 10 h, (b)  
24 350 °C for 10 h/300 °C for 10 h, (c) 350 °C for 10 h/350 °C for 10 h, and (d) 350 °C for 10  
25 h/400 °C for 10 h. Reprinted figure from [127], with the permission of IOP Publishing.  
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31 We also investigated the effect of the secondary annealing temperature on the bubble  
32 density and the bonding strength, as shown in figure 26 and figure 27(a). One can see that with  
33 the increase in secondary annealing temperature, the bubble density increases at first, and then  
34 decreases. In addition, the bonding strength increases with the increase of the annealing  
35 temperature. The increase of the bubble density at first results from residual hydrophilic  
36 reactions at the bonded interface and the decrease of the bubble density is attributed to the  
37 crystallization of the a-Ge film at the bubble position when higher annealing temperature was  
38 applied (discuss next).  
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46 Figure 27(b)-(e) show metalloscope images of Si surfaces of the samples with secondary  
47 annealing after pulling test of the bonded wafers. One can see that the Ge pit position is the  
48 bubble position. When the sample is annealed at higher temperature, the color of the bubble  
49 position (the color is yellow at lower annealing temperature) turns into black. This is due to the  
50 crystallization of the a-Ge film at the bubble position, as shown in figure 28. When the sample  
51 was annealed at 350 °C, the a-Ge at the bubble position starts to crystallize and the a-Ge film  
52 out of the bubble position still shows amorphous phase. When the annealing temperature  
53 increases to 400 °C, the total Ge film at the bonded interface has crystallized.  
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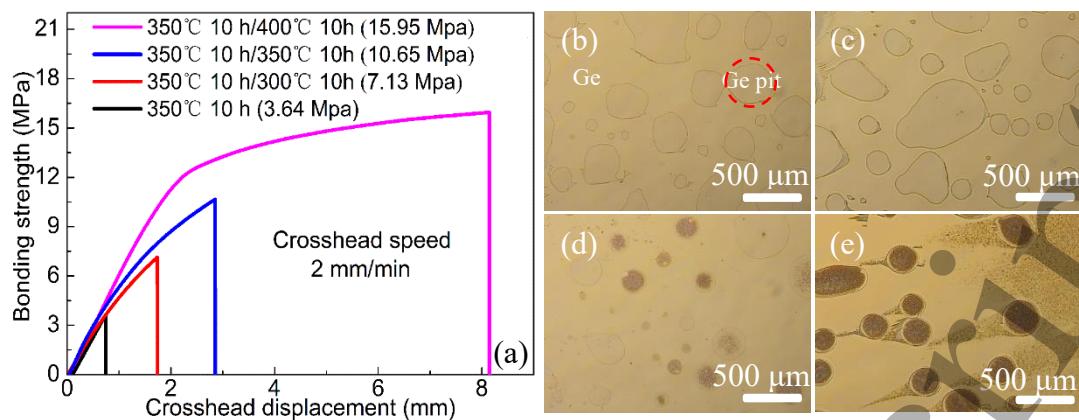


Figure 27. (a) Bonding strength of the Si bonded wafer pairs annealed at different temperatures. Reprinted figure from [127], with the permission of IOP Publishing.

Metalloscope images of the bonded interfaces of the samples annealed at (b) 350 °C for 10 h, (c) 350 °C for 10 h/300 °C for 10 h, (d) 350 °C for 10 h/350 °C for 10 h, and (e) 350 °C for 10 h/400 °C for 10 h after the pull test. Reprinted figure from [127], with the permission of IOP Publishing.

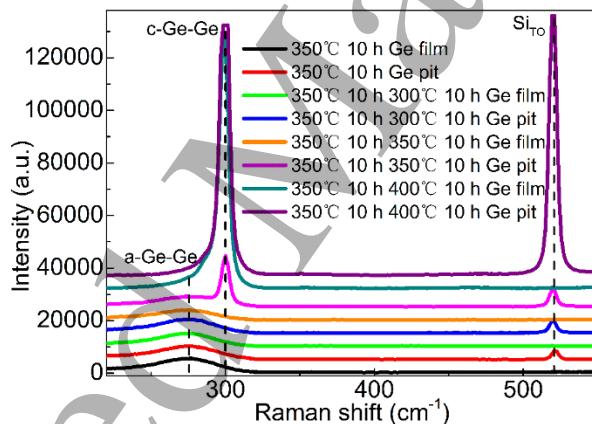


Figure 28. Raman spectrum of the bonded interfaces of the Si bonded wafer pairs annealed at different temperatures. Reprinted figure from [127], with the permission of IOP Publishing.

Figure 29 shows the TEM images of the Si bonded interface with 90 nm thick Ge layer annealed at 400 °C for 20 h. One can see that the a-Ge at the a-Ge/a-Ge bonded interface crystallizes to poly-Ge and the a-Ge at the a-Ge/Si interface still shows amorphous phase. This indicates that the poly-Ge film at the Si/Si bonded interface can absorb the by-products (H<sub>2</sub> and H<sub>2</sub>O) in the bubbles, leading to the disappearance of the bubbles at higher annealing temperature (figure 26). We also simulated the stress in the bonded wafer pairs, as shown in

figure 30(a). One can see that the stress symmetrically distributes in the wafer pairs and the largest stress appears at the a-Ge/a-Ge interface. This reveals that the crystallization of the a-Ge starts from the a-Ge/a-Ge interface and extends to the a-Ge/Si interface, as shown in the inset of figure 30(a), due to the stress-induced crystallization of the a-Ge.

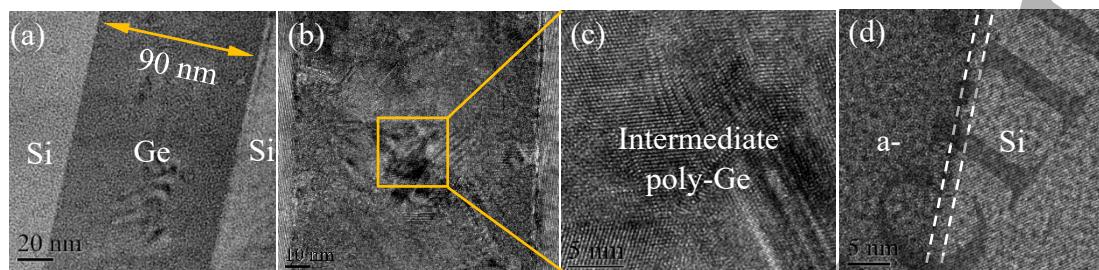


Figure 29. TEM images of the Si/Si bonded interfaces with 45 nm a-Ge layer. Reprinted from [126], with the permission of AIP Publishing.

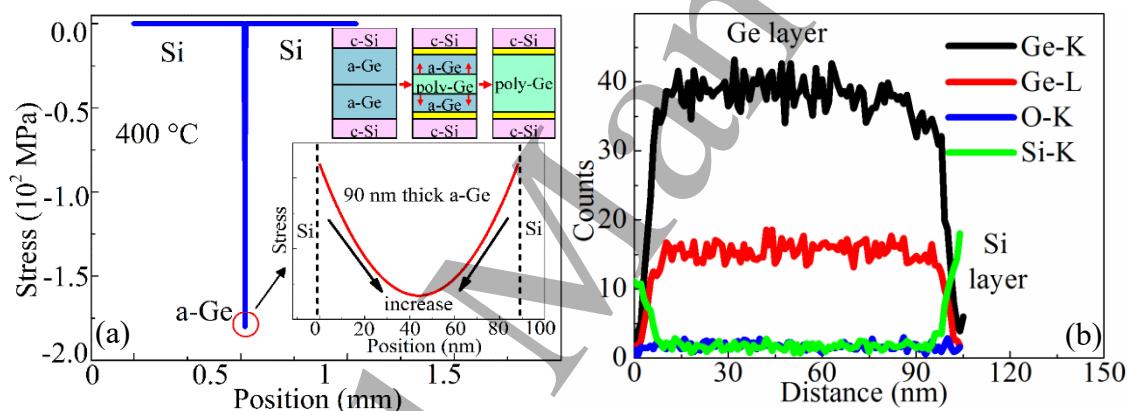


Figure 30. (a) Simulation results of the stress distribution in the Si/Si bonded wafers annealed at 400 °C. Reprinted from [126], with the permission of AIP Publishing. (b) EDS curves of the Si/Si bonded interface. Reprinted from [126], with the permission of AIP Publishing.

On the other hand, we cannot observe oxide layer at the bonded interface, as shown in figure 29(b). The O element cannot be detected by TEM energy dispersion spectrum (EDS), as shown in figure 30(b). This suggests that the bonded interface is an oxide-layer-free interface. The mechanism for the absence of the oxide layer at the bonded interface is shown in figure 31. Firstly, the oxide layer forms at the bonded interface due to the hydrophilic reaction. When the crystallization of the a-Ge occurs at the bonded interface, the atom migration becomes serious, the Ge atoms migrate into the oxide layer and the O atoms migrate into the Ge film, leading to

the decomposition of the oxide layer.

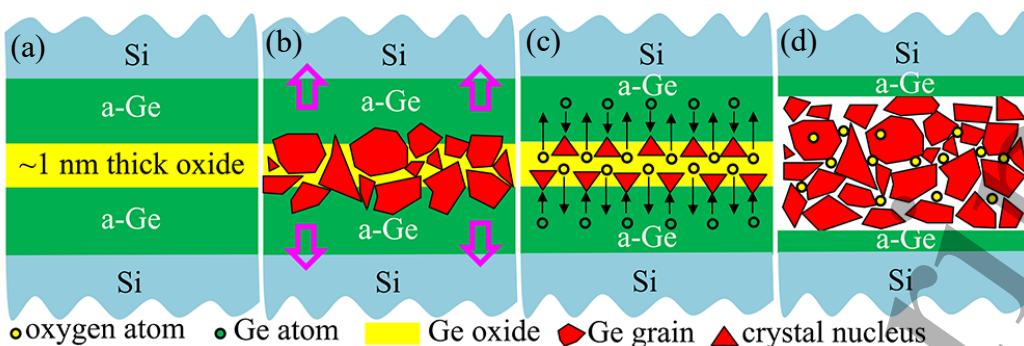


Figure 31. (a) and (b) Crystallization process of the a-Ge at the Si/Si bonded interface.

Reprinted from [128], with the permission of Springer. (c) and (d) Kinetic process of the Ge and oxygen atoms at the Si/Si bonded interface. Reprinted from [128], with the permission of Springer.

We also investigated the bubble density as a function of a-Ge layer thickness at 350 °C and 400 °C, as shown in figure 32 and figure 33. One can see that when the samples were annealed at 350 °C for 20 h, the bubbles density slightly decreases with the increase of the a-Ge layer thickness. However, the bubbles still exist at the bonded interface, even for the sample with 100 nm thick a-Ge layer. Only small bubbles ( $0\text{-}0.01 \text{ mm}^2$  and  $0.01\text{-}0.1 \text{ mm}^2$ ) were observed at 350 °C with the increase of a-Ge layer thickness, as shown in figure 34(a). In addition, as shown in figure 34(b), the bonding strength (7-8 Mpa) is almost changeless with the increase in a-Ge layer thickness. This is due to the fact that the crystallization of the a-Ge film is insufficient at 350 °C, the bubbles cannot be totally absorbed, leading to the lower bonding strength of the Si wafer pairs. For the samples annealed at 400 °C for 20 h, the bubble density decreases with the increase in a-Ge layer thickness. The bubbles almost disappear when the a-Ge layer thickness reaches 30 nm. Not only the small bubbles, but also the large bubbles ( $> 0.1 \text{ mm}^2$ ), as shown in figure 34(a), can be totally absorbed at 400 °C with the increase in a-Ge layer thickness due to the sufficient crystallization of the a-Ge at 400 °C. The crystallization of the a-Ge also leads to the increase of the bonding strength (16-18 Mpa).

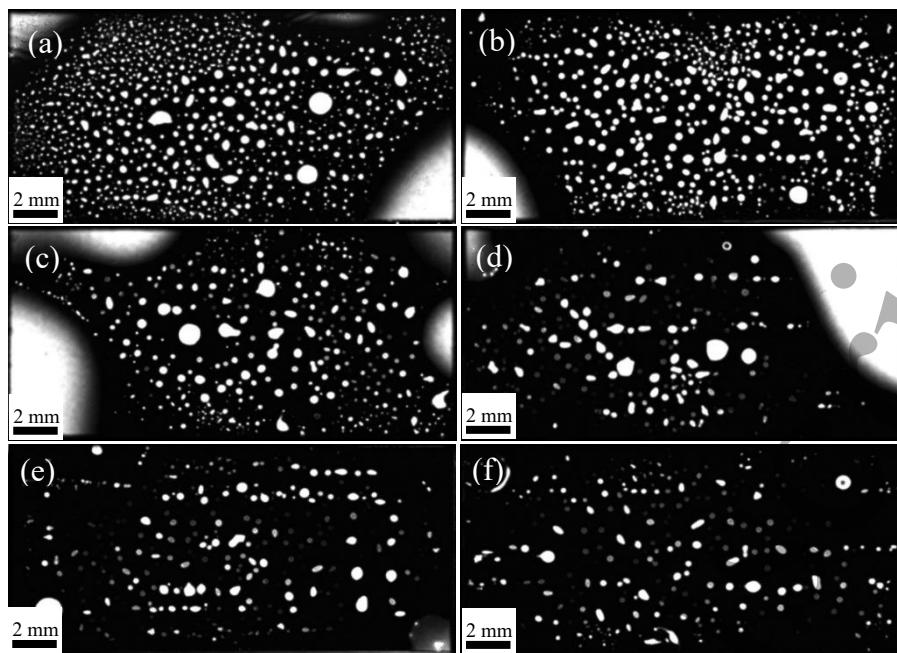


Figure 32. SAM images of the Si bonded wafer pairs with (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 30 nm, (e) 45 nm, and (f) 70 nm thick a-Ge layer annealed at 350 °C for 20 h. Reprinted figure from [127], with the permission of IOP Publishing.

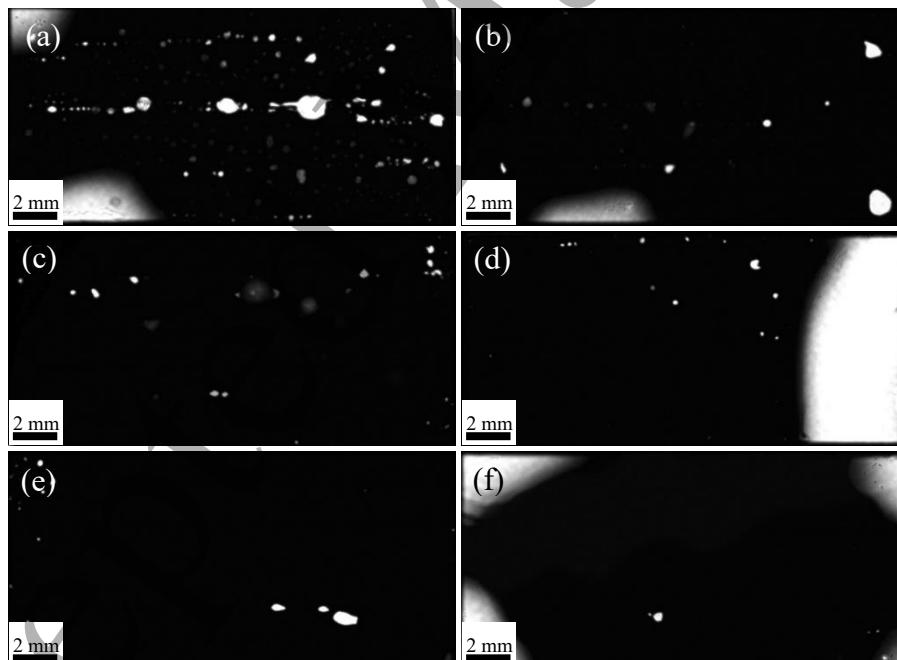


Figure 33. SAM images of the Si bonded wafer pairs with (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 30 nm, (e) 45 nm, and (f) 70 nm thick a-Ge layer annealed at 350 °C for 20 h. Reprinted figure from [127], with the permission of IOP Publishing.

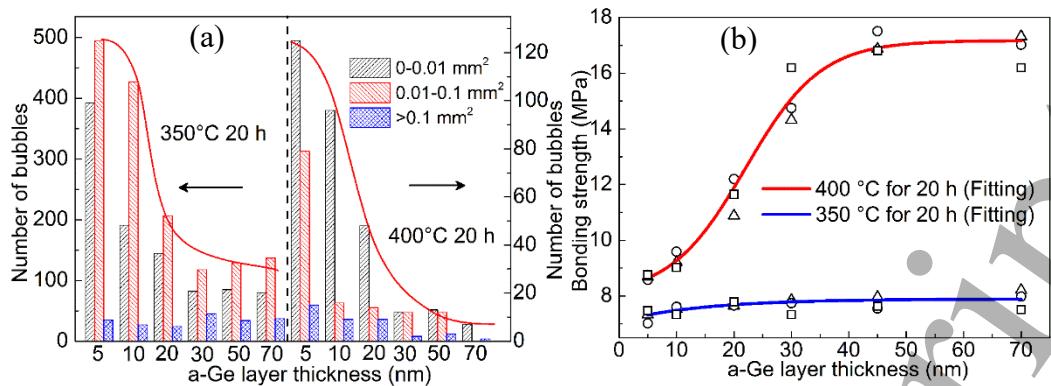


Figure 34. (a) Statistical histogram of the area of all the bubbles annealed at different temperatures. Reprinted figure from [127], with the permission of IOP Publishing. (b) Bonding strength of three sets of wafer pairs with different a-Ge layer thickness annealed at 350 °C and 400 °C for 20 h. Reprinted figure from [127], with the permission of IOP Publishing.

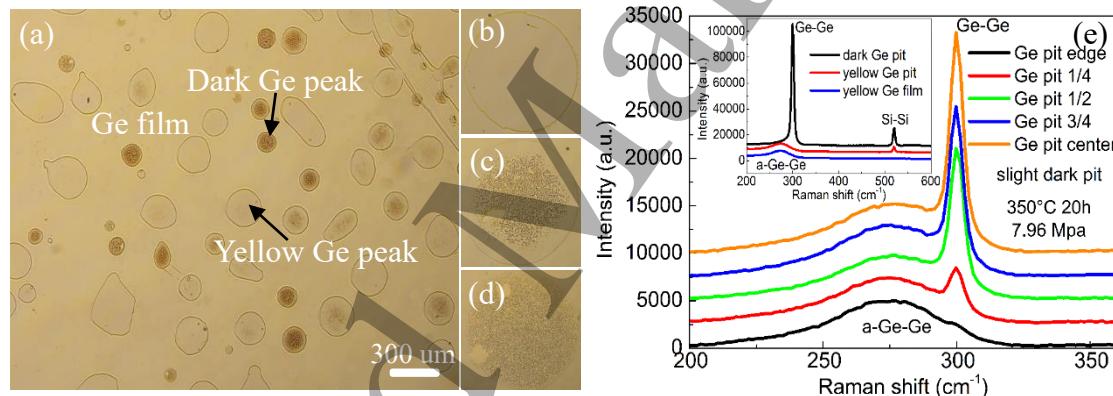


Figure 35. (a) Optical microscope image of the bonded interface of the sample annealed at 350 °C for 20 h. Reprinted figure from [129], with the permission of Elsevier. (b)-(d) Enlarged drawing of Figure 35(a). Reprinted figure from [129], with the permission of Elsevier. (e) Raman spectrum of the Ge pit at different place shown in Figure 35(d). Reprinted figure from [129], with the permission of Elsevier. Inset shows the Raman spectrum of the Ge film and Ge pit shown in Figure 35. Reprinted figure from [129], with the permission of Elsevier.

In order to reveal the repair process of bubbles during annealing. The pulling test was conducted for the sample annealed at 350 °C for 20h, as shown in figure 35(a). One can see

that some bubbles have crystallized and some bubbles still show amorphous phase. The Raman shift of the bubble in figure 35(c) is shown in figure 35(e). It can see that the crystallization of the a-Ge film starts from the center of the bubbles and expends to the edge of the bubble. This is consistent with the bubble evolution shown in figure 36. The bubbles start to turn into dark from the center of the bubbles in the SAM image and finally the total bubbles become bonded region.

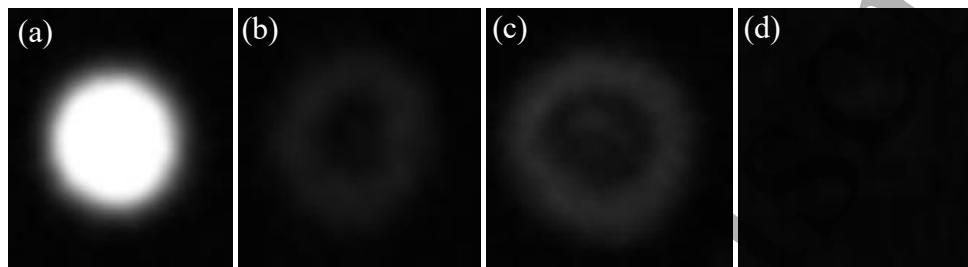


Figure 36. SAM image of the single bubble at different crystalline stages. Reprinted figure from [129], with the permission of Elsevier.

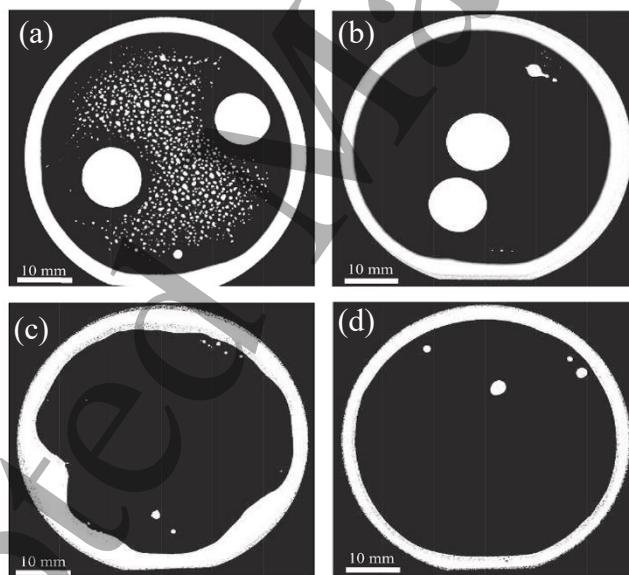


Figure 37. SAM images of the bonded wafer pairs annealed at (a) 350 °C for 20 h with the DI water immersion, (b) 400 °C for 20 h with the DI water immersion, (c) 350 °C for 20 h without the DI water immersion, and (d) 400 °C for 20h without the DI water immersion. Reprinted figure from [130], with the permission of IOP Publishing.

The sputtered a-Ge film was immersed into DI water and then was spin-dried before bonding in the experiments shown above. We also fabricate bonded Si/Si samples using the

direct contact method in which the sputtered a-Ge was not immersed into the DI water, as shown in figure 37. One can see that after annealing at 350 °C for 20 h, lots of bubbles appear at the bonded interface in the sample whose a-Ge film was immersed into the DI water, while no bubbles appear at the bonded interface for the sample whose a-Ge film was not immersed into the DI water. This is attributed to the fact that the a-Ge surface absorbs few -OH groups when the a-Ge film was not immersed into the DI water, leading to the decrease of the hydrophilic reactions at the bonded interface and the disappearance of bubbles.

We also studied the effect of the annealing temperature on the I-V curves of n-Si/n-Si bonded wafer pairs, as shown in figure 38(a). One can see that the I-V curves of the wafer pairs are all linear. This indicates that the barrier at the bonded interface is low enough for carrier transport. With the increase of the annealing temperature, the current increases, indicating the decrease of the resistance at the bonded interface. When the annealing temperature reaches 400 °C, the current of the bonded wafer pairs is close to that of bulk n-Si. This is attributed to the crystallization of the a-Ge film with the increase of the annealing temperature. This suggests the low resistance at the n-Si/n-Si bonded interface.

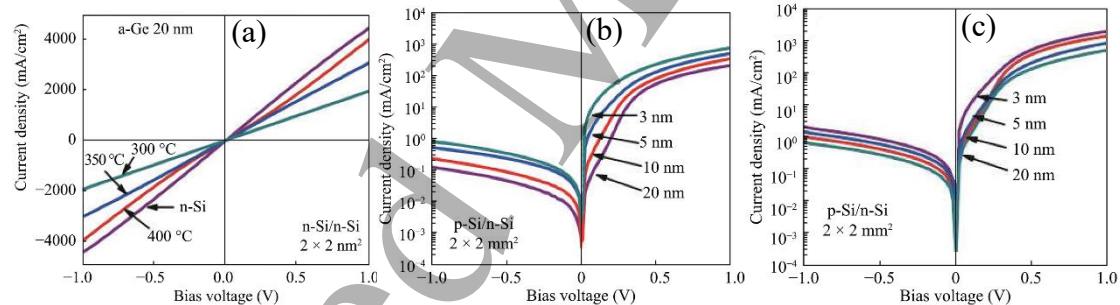


Figure 38. (a) I-V characteristics of the n-Si/n-Si bonded wafers (20 nm) annealed at different temperatures. Reprinted figure from [130], with the permission of IOP Publishing. I-V curves of the Si-based PN junction with different a-Ge interlayer thickness annealed at (a) 350 °C for 20 h and (b) 400 °C for 20 h. Reprinted figure from [130], with the permission of IOP Publishing.

We also study the effect of a-Ge layer thickness on the I-V curves of p-Si/n-Si junction annealed at 350 °C for 20 h and 400 °C for 20 h, as shown in figure 38(b) and (c), respectively. One can see that the I-V curves all exhibit rectification characteristic. This indicates that the

carriers at the bonded interface can transport well at the bonded interface. With the increase of the a-Ge layer thickness, the reverse current and the forward current both decrease. This is attributed to the increase of the resistance at the bonded interface due to the insertion of the thick a-Ge layer. On the other hand, the reverse current for the sample annealed at 400 °C for 20 h is higher than that annealed at 350 °C for 20 h. This can be ascribed to the increase of the electrical conductivity induced by the crystallization of the a-Ge film.

Overall, the semiconductor interlayer bonding technique can achieve Si/Si wafer bonding with high bonding strength and bubble-free bonded interface. This method is low-cost and is easy to be conducted. In addition, the interface oxide layer formed by the hydrophilic reaction can be totally decomposed due to the crystallization of the semiconductor interlayer. The bonded homojunction can achieve a linear I-V curve which can be comparable to that of bulk material. However, due to the insertion of the semiconductor interlayer, the resistance at the bonded interface increases, leading to the decrease of the reversed current and forward current of the device. Although the crystallization of the semiconductor interlayer may lead to the decrease of the interface resistance, the thickness of the semiconductor interlayer should be as low as possible.

## 1.2 Progress of Ge/Si wafer bonding

Compared to homogeneous Si/Si wafer bonding, the investigation of heterogeneous Ge/Si wafer bonding starts relatively late and few groups focus on the study of the Ge/Si wafer bonding and its applications in the photoelectric field. The Si-based Ge film fabrication is mainly based on the epitaxial growth. Thus, the wafer bonding technique is not widely used in the semiconductor technology. The reason for the less work on the Ge/Si wafer bonding can be concluded as following five reasons. (1) There is 4.2% lattice mismatch between Ge and Si materials. If Si and Ge wafer surfaces are not treated well before bonding, misfit dislocations may diffuse into the Ge wafer. (2) There is thermal expansion coefficient mismatch between Ge and Si materials (Ge [133]: $5.5 \times 10^{-6}$  K<sup>-1</sup> and Si [134]: $2.6 \times 10^{-6}$  K<sup>-1</sup>). If the annealing temperature is not well controlled, the thermal stress may be large enough to trigger the separation or crack of the bonded sample during annealing due to the thick bulk wafer (hundreds of micrometers). (3) The unstable oxides of the Ge material, such as GeO and Ge<sub>2</sub>O, easily form on the clean Ge surface, leading to the instability of the Ge/Si bonded interface. Although

the HF solution can remove most stable Ge oxide ( $\text{GeO}_2$ ) on the Ge surface, the unstable oxide is difficult to be removed cleanly. The unstable oxide can evaporate and break the existing Ge/Si bonds during higher temperature annealing ( $\geq 400$  °C), resulting in the formation of interface bubbles. (4) Although the bonding strength can increase when high-temperature annealing was conducted, the wafers may separate or creak during the annealing and the Ge/Si interdiffusion is serious at high temperature. Thus, it is difficult to obtain a desired Ge/Si bonding interface at higher annealing temperature. However, the bonding strength of the Ge/Si wafer pairs annealed at lower temperature is relatively lower than that annealed at higher temperature. This leads to the unsatisfied electrical properties at the bonded interface. (5) The most important reason is that an oxide layer formed by the hydrophilic or hydrophobic reactions exists at the Ge/Si interface in most Ge/Si wafer bonding techniques. The existence of the oxide layer at the bonded interface restrain the carrier transport at the bonded interface and lead to the increase of the RC time constant. Thus, the 3dB-bandwidth may decrease. This factor limits the use of wafer bonding technique in the optoelectronic field.

Although lots of challenges need to be overcame for Ge/Si wafer bonding at present, there are four distinct advantages of this technique which is hopeful to be an alternative of the traditional epitaxy technique. (1) Ge/Si wafer bonding can be carried out at a low temperature of  $\leq 300$  °C. This is much lower than that in the epitaxy technique (deoxygenation of the Si substrate at  $> 850$  °C and epitaxial growth of the Ge film at  $\sim 600$  °C). (2) Low-temperature Ge/Si wafer bonding can achieve a TD-free Ge/Si bonded interface due to the restraint of the nucleation and the diffusion of the misfit dislocations at low temperature. (3) Ge/Si wafer bonding can retain the crystalline quality and photoelectric characteristic of bulk Ge. (4) Ge/Si wafer bonding cooperates with the Smart-Cut technique can fabricate a Si-based Ge film whose quality can be comparable with bulk Ge.

The proposed Ge/Si wafer bonding at present can be concluded as wet wafer bonding which is divided into hydrophilic wet wafer bonding and hydrophobic wafer bonding, plasma-activated bonding, dry wafer bonding, high-vacuum surface-activated bonding, and semiconductor interlayer bonding.

### 1.3.1 Hydrophilic wet wafer bonding

For hydrophilic wet wafer bonding, after cleaning of Ge and Si wafers, they were bonded

in DI water and post-annealed for wafer bonding. Similar to Si/Si wafer bonding, high-temperature annealing of Ge/Si wafer pairs was investigated by Kanbe et al. [135-138] firstly. After cleaning of Si and Ge wafers in the organic solution, the wafer surfaces were deoxidized by the HF solution. Then, the wafers were further cleaned by  $H_2SO_4:H_2O_2:H_2O$  and  $HCl:H_2O$  solutions, respectively. After cleaning, the Si and Ge wafer surfaces both exhibits hydrophilic. Subsequently, the wafers were contacted to each other in the DI water and annealed at  $880\text{ }^\circ\text{C}$  in  $H_2$  atmosphere for 90 min to enhance the bonding strength. The TEM images of the Ge/Si bonded interface are shown in figure 39(a) and (b).

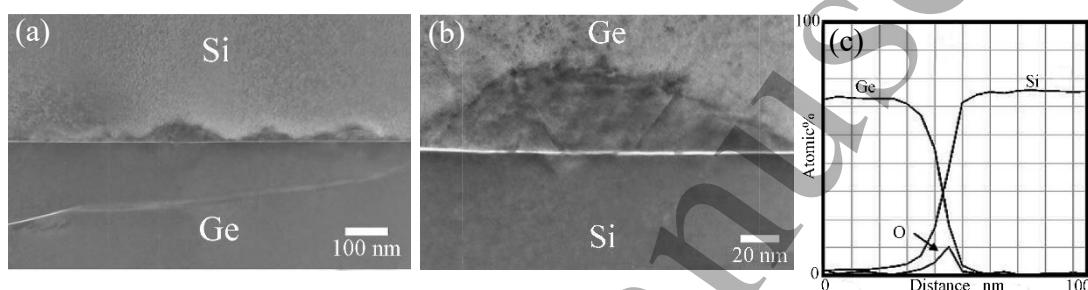


Figure 39. (a) and (b) TEM images of the Ge/Si bonded interface annealed at high temperature. Reprinted figure from [135], with the permission of AIP Publishing. (c) EDS curves of the Ge/Si bonded interface. Reprinted figure from [135], with the permission of AIP Publishing.

One can see that a transition layer with the thickness of several tens of nanometers appears at the Ge/Si bonded interface and some island-like structures appear in transition layer. This island-like structures result from the interdiffusion of the Ge and Si atoms at the bonded interface when high-temperature annealing was conducted. In addition, the dislocation lines along the [111] direction exist in the island-like structures and the distortion of the lattice at some positions of the bonded interface was observed. These abnormal features are attributed to the lattice mismatch and the thermal mismatch between Ge and Si. On the other hand, an obvious oxide layer appears at the Ge/Si bonded interface, as shown in figure 39(b) and (c). Moreover, a serious interdiffusion exists at the bonded interface, the diffusion depth of  $\sim 50\text{ nm}$  was detected. The EDS curve presents the O atom distribution at the Ge/Si bonded interface, indicating the existence of the Si and Ge oxide layer at the bonded interface.

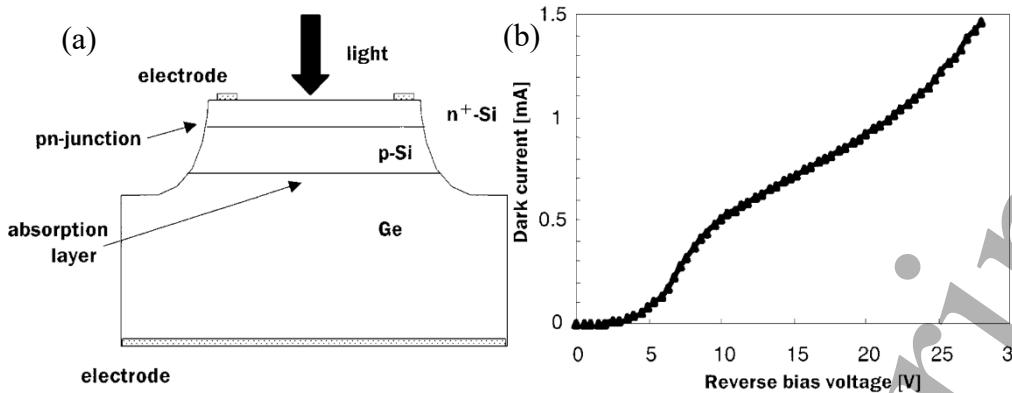


Figure 40. (a) Ge/Si device fabricated based on the Ge/Si wafer pairs annealed at high temperature. Reprinted figure from [136], with the permission of IOP Publishing. (b) I-V curve of this device. Reprinted figure from [136], with the permission of IOP Publishing.

Kanbe et al. fabricated a Ge/Si device based on this Ge/Si bonding method, as shown in figure 40(a). Although the device achieves a quantum efficiency of 40% at near-infrared wave range, the dark current of the device is too large, as shown in figure 40(b). The dark current reaches 0.5 mA when the reverse bias increases to 10 V. The large dark current of the device may be attributed to the interdiffusion and the formation of dislocations at the bonded interface.

After the study of high-temperature Ge/Si wet wafer bonding, Kanbe et al. also study the low-temperature annealing of the wet-bonded Ge/Si wafer pairs at 250 °C and 350 °C for 12-48 h. TEM images of the Ge/Si bonded interface are shown in figure 41(a). One can see that compared to the Ge/Si interface annealed at high temperature, the quality of the bonded interface annealed at low-temperature was improved. The misfit dislocations and TDs cannot be observed clearly at the bonded interface. Only 3-5 nm thick amorphous transition layer appears at the bonded interface. In addition, this layer is non-uniform. This may be due to the introduction of excessive H<sub>2</sub>O at the bonded interface. The C and O atoms were detected at the bonded interface, as shown in figure 41(b), indicating the existence of the contaminants and oxide layer at the bonded interface. In addition, the interdiffusion was observed at the bonded interface. The Ge/Si device based on this wafer bonding method also exhibits large dark current, as shown in figure 41(c). This may be due to the low bonding strength annealed at low temperature and the existence of the contaminants at the bonded interface.

Overall, whether high-temperature annealing or low-temperature annealing, the

hydrophilic Ge/Si wet wafer bonding cannot obtain a good Ge/Si bonded interface. A thick oxide layer appears at the Ge/Si bonded interface due to the bonding in the DI water and the excessive hydrophilic reactions at the Ge/Si bonded interface. High-temperature annealing triggers the formation of TDs and the Ge/Si intermixing at the bonded interface, while low-temperature annealing suffers from low bonding strength, resulting in the large dark current of the Ge/Si device.

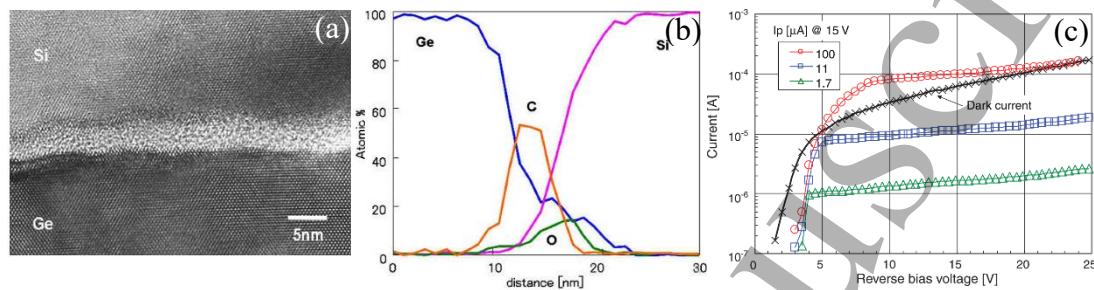


Figure 41. (a) TEM image of the Ge/Si wafer pairs annealed at low temperature. Reprinted figure from [137], with the permission of Springer. (b) EDS curves of the bonded interface. Reprinted figure from [137], with the permission of Springer. (c) I-V curves of the Ge/Si device. Reprinted figure from [138], with the permission of IOP Publishing.

### 1.3.2 Hydrophobic wet wafer bonding

In recent years, Lee et al. [139-140] investigated the crystallization of the a-Ge film on a  $\text{SiO}_2$  isolation layer induced by the Si window to achieve Ge/Si wafer bonding in the BOE solution. The induction process of the a-Ge film and the Ge/Si wafer bonding process are shown in figure 42. Firstly, a  $\text{SiO}_2$  isolation layer was deposited on the Si substrate. Then, a seed Si window for the crystallization of the a-Ge was opened on the  $\text{SiO}_2$  isolation layer. After that, a 300 nm thick a-Ge layer was deposited on the Si substrate and then a  $\text{SiO}_2$  capping layer was deposited on the a-Ge layer. Finally, the Si substrate was annealed at 950 °C for 4s using rapid thermal annealing to trigger the crystallization of the a-Ge film.

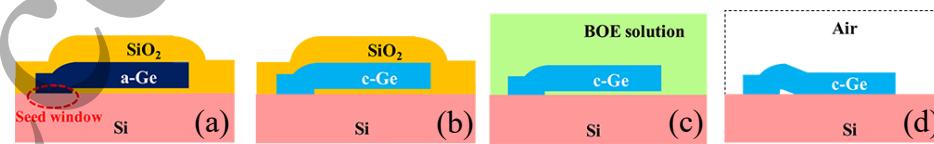


Figure 42. Process of the Ge/Si hydrophobic wet wafer bonding. Reprinted figure from [140], with the permission of OSA Publishing.

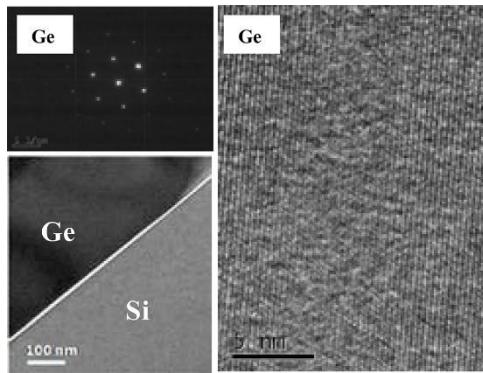


Figure 43. TEM images of the Ge/Si bonded interface fabricated by the hydrophobic wet wafer bonding. Reprinted figure from [140], with the permission of OSA Publishing.

After annealing, the Si substrate was immersed into the BOE solution to remove all the  $\text{SiO}_2$  on the substrate. The Ge film was attached to the Si substrate by Van der Waals force in the BOE solution. Finally, the Si substrate was taken out of the BOE solution and annealed at 400 °C for 1 h to achieve Ge/Si bonding. Figure 43 shows TEM images of the Ge/Si bonded interface. One can see that a 7 nm thick amorphous transition layer appears at the bonded interface. The element distribution in transition layer is Si:54%, Ge:14%, and O:32%. This indicates that the transition layer is an oxide layer. In addition, the a-Ge indeed turns into single-crystal Ge after annealing. Note that the crystallization of the a-Ge film not only appears at the Si window, but appears in the Ge film on the  $\text{SiO}_2$  layer. The Ge film on the  $\text{SiO}_2$  layer is demonstrated to be TD-free, the misfit dislocations and the TDs only exist at the Si window.

Lee et al. fabricated a waveguide Ge/Si p-i-n photodiode based on this bonding method, as shown in figure 44(a). The dark current of this photodiode is shown in figure 44(b). One can see that the I-V curve shows the rectification characteristic. However, the dark current sharply increases with the increase of the reverse bias, the saturation characteristic is not so satisfied. In addition, the forward current is lower, indicating the existence of large series resistance. This may be due to the poor quality of the Ge layer and the unsatisfied Ge/Si bonded interface. The responsivity of the photodiode is shown in figure 44(c). At -2 V reverse bias, the responsivity of the device at the wavelength of 1310 nm is only 0.3 A/W. In addition, the Ge film thickness is 300 nm, the calculated 3dB-bandwidth is dozens of GHz [142]. However, the 3dB-bandwidth of this device is only 16 GHz, as shown in figure 44(d), which is much lower than that of the epitaxial waveguide Ge/Si p-i-n photodiode [143].

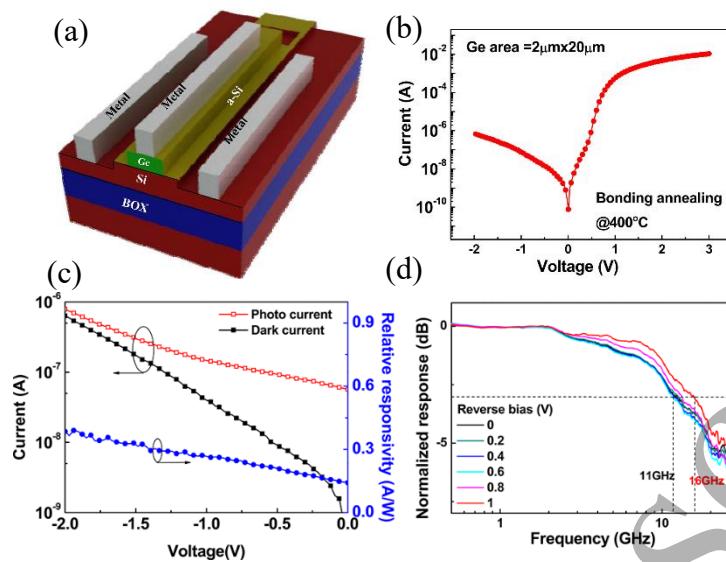


Figure 44. (a) Schematic diagram of the Ge/Si p-i-n photodiode based on the hydrophobic wet wafer bonding. Reprinted figure from [140], with the permission of OSA Publishing. (b) Dark current of the device. Reprinted figure from [140], with the permission of OSA Publishing. (c) Photocurrent of the device. (d) 3dB-bandwidth of the device. Reprinted figure from [140], with the permission of OSA Publishing.

Overall, although hydrophobic wet wafer bonding can restrict the TDs in the Si window, the point defects in the re-crystalline Ge layer on the  $\text{SiO}_2$  isolation layer cannot be eliminated, leading to the deterioration of the device performance.

### 1.3.3 Plasma-activated bonding

Byun et al. [144-146] and Gity et al. [147-149] systematically investigated low-temperature Ge/Si wafer bonding based on the free radical surface treatment. The O and N free radicals were used to activate wafer surfaces to be hydrophilic. The wafer bonder for the hot-pressed treatment of contacted wafer pairs was used to enhance the bonding strength and achieve pre-bonding. Firstly, after the cleaning of Si and Ge wafers, the wafer surfaces were activated by the O or N free radicals. Then, the wafers were contacted to each other and put into the wafer bonder for the hot-pressed treatment. The wafers were firstly bonded under a force of 1 kN (5 min) at a chamber pressure of  $10^{-5}$  mbar, then they were annealed in situ at 100 °C for 1 h under a force of 500 N. Finally, an ex situ annealing at 200 °C and 300 °C for 24 h was conducted to achieve Ge/Si wafer bonding with high bond strength. The O and N free

radical surface treatment can form a stable  $\text{GeO}_2$  on the Ge wafer due to the oxidation of the Ge surface and enhance the hydrophilic, respectively, as shown in figure 45.

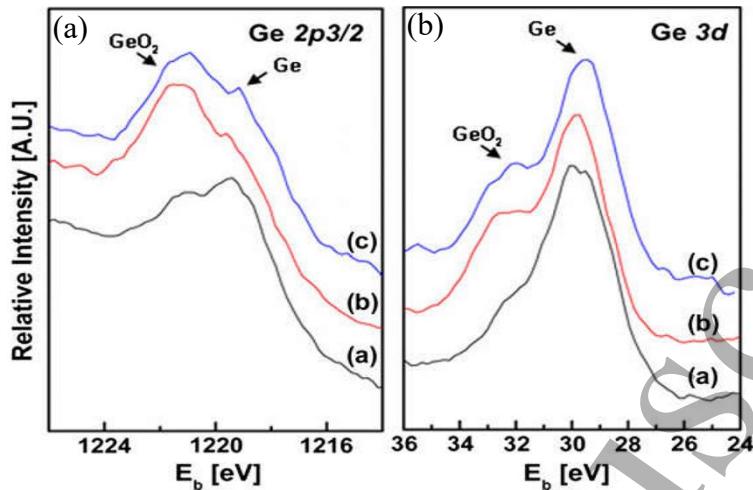


Figure 45. XPS curves of the Ge surfaces treated by the (a) O and (b) N free radicals.

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The SAM images of the Ge/Si wafer pairs treated by different free radicals are shown in figure 46. One can see that lots of bubbles appear at the Ge/Si bonded interface in the sample without free radical treatment, while an obvious decrease of the bubble density was observed at the Ge/Si bonded interface with the O and N free radical treatment. In addition, the bubble density at the Ge/Si bonded interface treated by the N free radicals is lower than that treated by the O free radicals. As we all know that, the oxide layer at the bonded interface can transfer the by-products out of the wafer pairs, that is, the thicker the oxide layer at the bonded interface, the lesser the by-products trapped at the bonded interface. Figure 47 shows the TEM images of the Ge/Si bonded interface treated by different free radicals. One can see that the oxide layer thickness at the bonded interface without the plasma treatment is 1.3 nm, and that treated by the O and N free radical is 1.6 and 2.2 nm, respectively. Thus, the bubble density at the Ge/Si bonded interface in the sample treated by the N free radical is least. This is consistent with the SAM images.

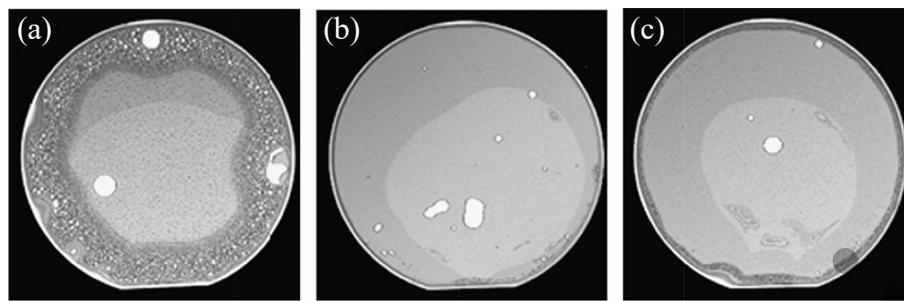


Figure 46. SAM images of the Ge/Si bonded interfaces (a) without free radical treatment, (b) with O free radical treatment, and (c) with N free radical treatment. Reprinted figure from [144], with the permission of Elsevier.

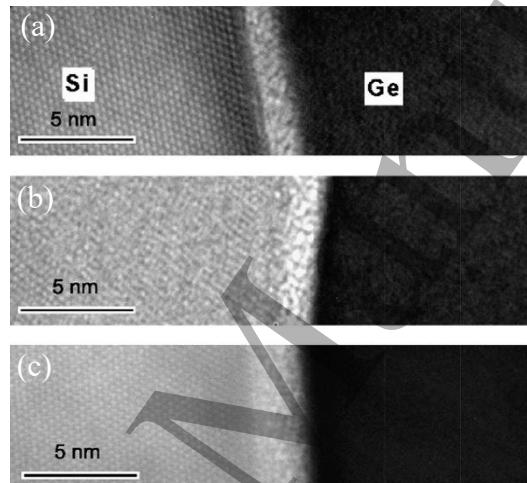


Figure 47. TEM images of the Ge/Si bonded interfaces (a) without free radical treatment, (b) with O free radical treatment, and (c) with N free radical treatment. Reprinted figure from [144], with the permission of Elsevier.

Gity et al. exfoliated a 700 nm thick Si-based Ge film by plasma-activated Ge/Si wafer bonding and the Smart-Cut technique. They also fabricated a p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction based on this exfoliated Ge film, as shown in figure 48(a). The dark current of this p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction is shown in figure 48(b). One can see that although the p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction shows the rectification characteristic, the forward current is lower, indicating the existence of high resistance at the bonded interface. In order to enhance the forward current, the heterojunction was annealed at 400 °C for 30 min. As shown in figure 48(b), the forward current increases after post-annealing, while the dark current slightly increases. The on/off

current ratio of the p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction with 100 μm diameter mesa at -0.5 V reaches  $5 \times 10^4$ , and the ideality factors of 5.48 and 2.28 were achieved before and after post-annealing.

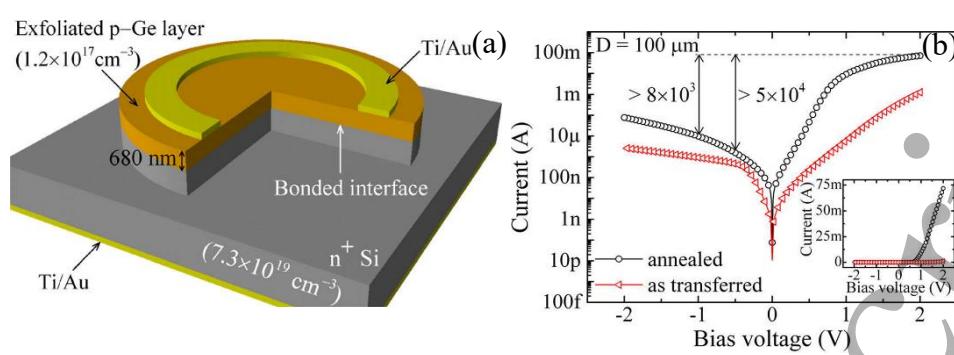


Figure 48. (a) p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction fabricated by the plasma-activated Ge/Si wafer bonding. Reprinted figure from [147], with the permission of AIP Publishing. (b) I-V curves of the p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction. Reprinted figure from [147], with the permission of AIP Publishing.

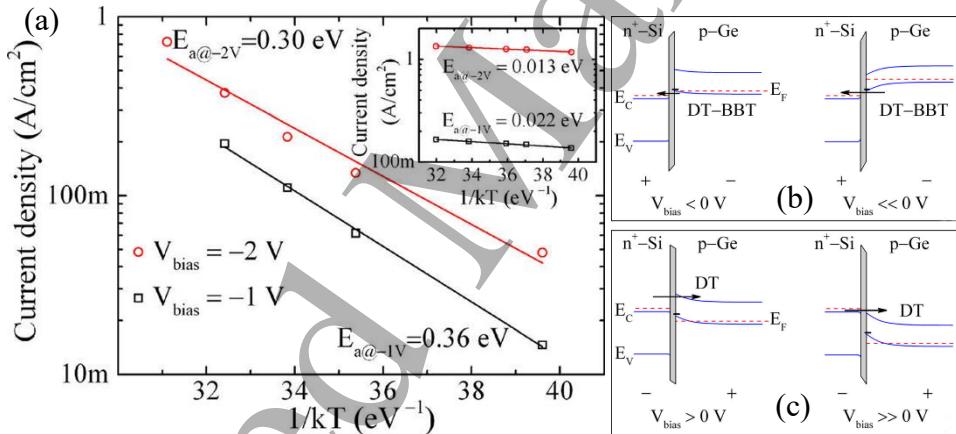


Figure 49. (a) Activation energies of the p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction before and after post-annealing. Reprinted figure from [147], with the permission of AIP Publishing. Carrier transport mechanisms at the Ge/Si bonded interface (b) under reverse bias and (c) forward bias. Reprinted figure from [147], with the permission of AIP Publishing.

The activation energies before and after post-annealing are shown in figure 49(a). One can see that the activation energy of 0.33 eV of the heterojunction was obtained before post-annealing. This value is close to the half of the Ge band gap. Thus, the mechanism of the generation and recombination of the carriers is dominated in the p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction

before post-annealing. However, the activation energy of the heterojunction is  $\sim 0.013\text{eV}$  after post-annealing. This is much lower than that of the Ge band gap. Thus, the band-to-band tunneling (BBT) mechanism can be responsible for the carrier transport at the heterojunction after post-annealing, as shown in figure 49(b) and (c).

Overall, the bubble density at the Ge/Si bonded interface can be decreased using plasma-activated Ge/Si wafer bonding, while the bubbles cannot be totally eliminated due to the hydrophilic reaction at the bonded interface. More importantly, the oxide layer still exists at the bonded interface even if the surface activation was applied. The carriers at the bonded interface can only transport by tunneling. This is not a good thing for the fabrication of high-performance Ge/Si device.

### 1.3.4 Dry wafer bonding

The Ge and Si wafers were contacted in the BOE solution in the wet wafer bonding method described above, in other word, the bonded Si wafer is original Si substrate after the corrosion of the  $\text{SiO}_2$ . However, in dry wafer bonding, after the corrosion of the  $\text{SiO}_2$ , the thermal release tape was used to transfer the thin film on original Si substrate to another new substrate. The dry wafer bonding can be divided into two parts. The one is the direct thin film transfer, and the other is the aligned thin film transfer. Kiefer et al. [150] investigated the direct thin film transfer for Ge/Si wafer bonding. They tended to transfer a 200 nm thick Si thin film in SOI substrate to a Ge wafer surface. Firstly, the Si thin film was defined and etched, and then the SOI wafer was immersed into the HF solution to corrode the BOX layer. After the corrosion, the Si thin film attaches to the Si substrate by weak Van der Waals force. After that the Si thin film was peeled off from the Si substrate by thermal release tape and transferred to the Ge substrate after the wafer was taken out of the HF solution. Finally, the Ge wafer was annealed at  $400\text{ }^\circ\text{C}$  for 30 min to enhance the bonding strength.

This bonding method is also one type of the hydrophobic bonding due to the fact that the Si thin film surface was passivated by H bonds before bonding. The optical microscope image of the transferred Si thin film is shown in figure 50(a). The TEM image of the Ge/Si bonded interface is shown in figure 50(b). One can see that no TDs were observed at the Ge/Si bonded interface. Only a thin amorphous transition layer (1.2 nm) appears at the bonded interface. The absence of the TDs can be attributed to the thin Si film and the low temperature annealing.

However, the 1.2 nm thick amorphous transition layer introduces a barrier at the Ge/Si bonded interface, restraining the transport of the carriers, as shown in figure 51. One can see that the carrier transport mechanism at the bonded interface is the barrier tunneling mechanism. This is similar to that at the Ge/Si bonded interface fabricated by plasma-activated bonding.

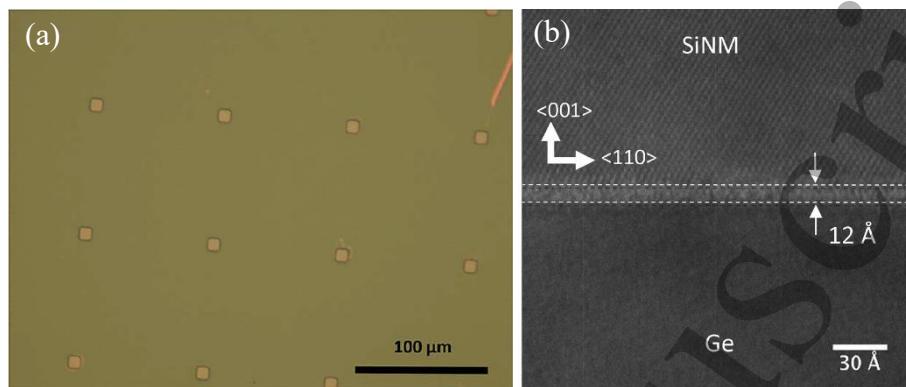


Figure 50. (a) Optical microscope image of the transferred Si thin film. Reprinted figure from [150], with the permission of ACS Publications. (b) TEM image of the Ge/Si bonded interface fabricated by the direct thin film transfer. Reprinted figure from [150], with the permission of ACS Publications.

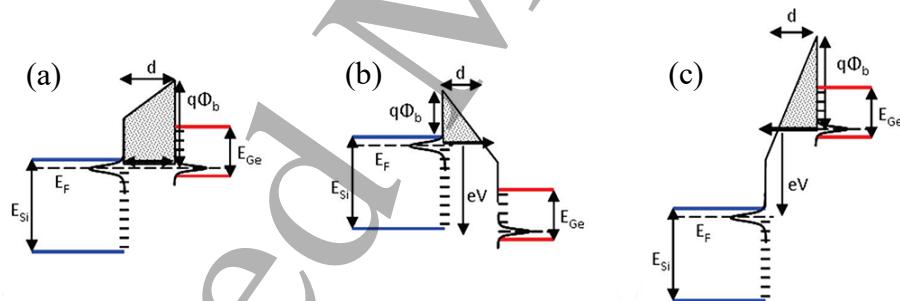


Figure 51. Carrier transport at the Ge/Si bonded interface fabricated by direct thin film transfer. Reprinted figure from [150], with the permission of ACS Publications. (a) At equilibrium. (b) At high forward bias. (c) At high reverse bias.

Liu et al. [151,152] achieved the Ge/Si micro-ribbon bonding by the aligned thin film transfer recently. The bonding process is shown in figure 52. Firstly, the SOI substrate with 70 nm thick n<sup>+</sup>-top Si and the GOI with 60 nm thick p<sup>+</sup>-top Ge were defined and etched to form Si and Ge ribbons on the SiO<sub>2</sub>, respectively. After that, the SOI and GOI were put into the HF solution to remove all the SiO<sub>2</sub> to form the Si and Ge ribbons on the Si substrate. Then, the

thermal release tape was used to transfer the Si ribbons onto the Ge ribbons to achieve the Ge/Si micro-ribbon bonding. This micro-ribbon alignment was conducted for this bonded method. This bonding method is also considered to be a hydrophobic bonding.

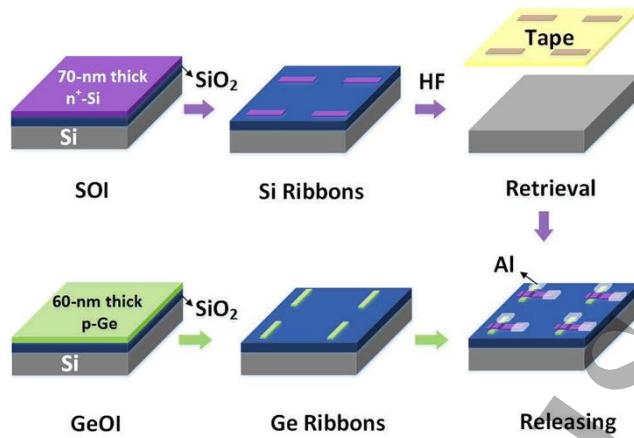


Figure 52. Fabrication process of the Ge/Si micro-ribbon bonding. Reprinted figure from [151], with the permission of IEEE Xplore Digital Library.

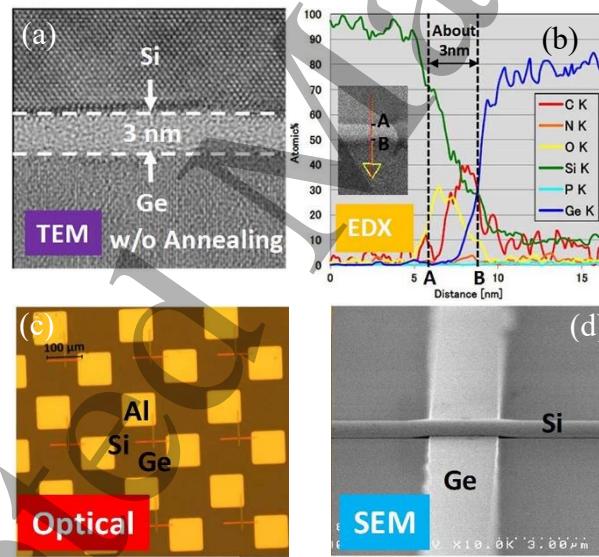


Figure 53. (a) TEM image of the Ge/Si bonded interface fabricated by the Ge/Si micro-ribbon bonding. Reprinted figure from [151], with the permission of IEEE Xplore Digital Library. (b) EDS curves of the Ge/Si bonded interface. Reprinted figure from [151], with the permission of IEEE Xplore Digital Library. (c) Optical microscope image of the p-Ge/n<sup>+</sup>-Si heterojunction. Reprinted figure from [151], with the permission of IEEE Xplore Digital Library. (d) SEM image of the Ge/Si micro-ribbon. Reprinted figure from [151], with the permission of IEEE Xplore Digital Library.

The TEM image of the Ge/Si bonded interface is shown in figure 53(a). One can see that the TDs were also not observed in the Ge or Si thin film, while an oxide layer with the thickness of 3 nm was clearly observed at the Ge/Si bonded interface. This also can be identified by the EDS curves shown in figure 53(b). Liu et al. fabricated a p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction using this bonding method, as shown in figure 53(c) and (d). The dark current of this p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction is shown in figure 54(a) and (b). One can see that the threshold voltage of this heterojunction is only 0.3 V which is much lower than that for the Ge/Si heterojunction fabricated by the plasma-activated bonding. The ideality factor of 2.15 was achieved for this ribbon heterojunction, which is also much smaller than that of the wafer-bonded heterojunction (5.48). However, the forward current of this device does not improve effectively. Due to the existence of the oxide layer at the bonded interface, the tunneling effect is dominated at the bonded interface, as shown in figure 54(c).

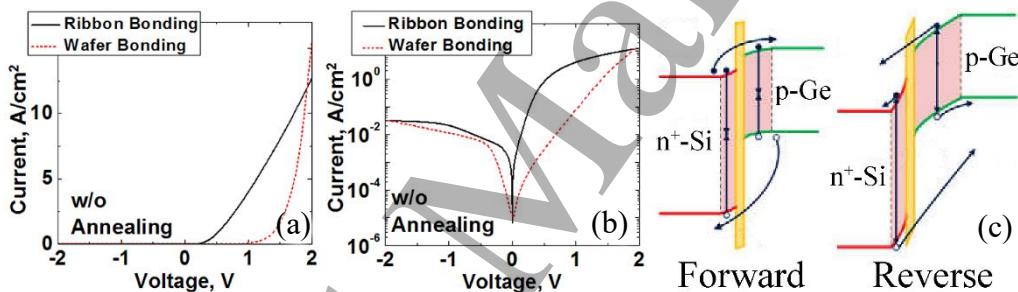


Figure 54. (a) and (b) I-V curves of the Ge/Si heterojunction fabricated by the Ge/Si micro-ribbon bonding. Reprinted figure from [152], with the permission of IEEE Xplore Digital Library. (c) Carrier transport mechanism at the Ge/Si bonded interface. Reprinted figure from [152], with the permission of IEEE Xplore Digital Library.

### 1.3.5 high-vacuum surface-activated bonding

High-vacuum surface-activated bonding method was used in Si/Si wafer bonding described above. The Ar atom beam was emitted to clean and activate the Si surface. However, for high-vacuum surface-activated Ge/Si wafer bonding, the Ar ion beam was applied to activate the Si and Ge surface. The fabrication process is shown in figure 55. The surface activation of Ge and Si surfaces in high-vacuum was conducted after cleaning of the wafers.

After that, the wafers were aligned and bonded together in high vacuum ( $\sim 10^{-6}$  Pa). Finally, the

bonded wafer pairs were post-annealed to enhance the bonding strength.

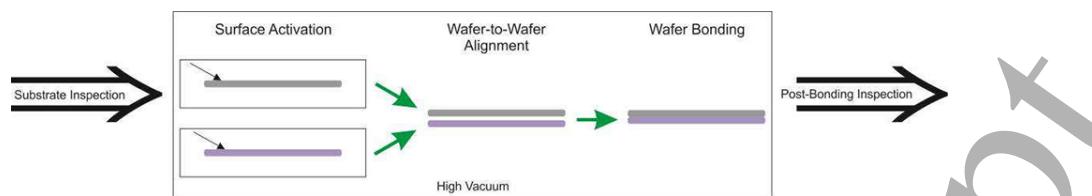


Figure 55. Fabrication process of the Ge/Si wafer pairs by high-vacuum surface-activated bonding. Reprinted figure from [153], with the permission of IOP Publishing.

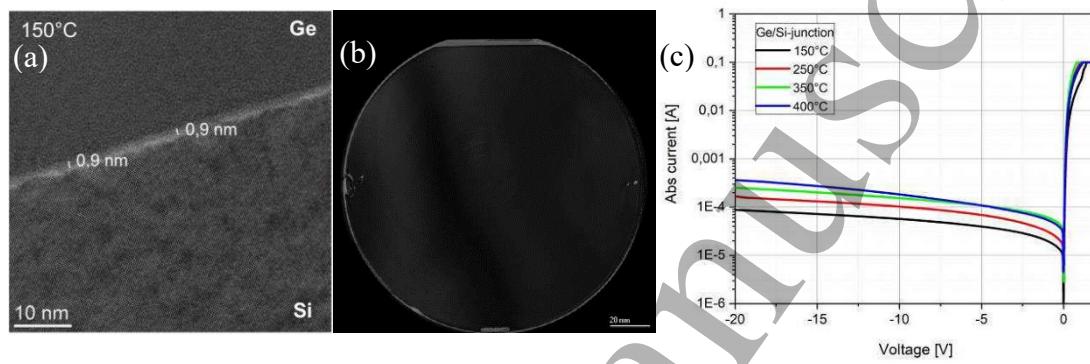


Figure 56. (a) TEM image of the Ge/Si bonded interface fabricated by the high-vacuum surface-activated bonding annealed at 150 °C for 2 h. Reprinted figure from [153], with the permission of IOP Publishing. (b) SAM image of the Ge/Si bonded interface annealed at 150 °C for 2 h. Reprinted figure from [153], with the permission of IOP Publishing. (c) I-V curves of the Ge/Si heterojunction. Reprinted figure from [153], with the permission of IOP Publishing.

The TEM image of the Ge/Si bonded interface in the sample annealed at 150 °C for 2 h is shown in figure 56(a). One can see that the TDs are also absent at the Ge/Si bonded interface. Only 0.9 nm thick amorphous transition layer appears at the Ge/Si bonded interface. The amorphous transition layer at the Ge/Si bonded interface is thinner than that in the Si/Si wafer bonding. This may be due to the fact that the damage of the surface bombarded by the Ar ion beam is smaller than that bombarded by the Ar atom beam. The SAM image of the Ge/Si bonded interface annealed at 150 °C for 2 h is shown in figure 56(b). One can see that few bubbles appear at the bonded interface when low-temperature annealing was conducted. Razek et al. also study the effect of the annealing temperature on the I-V curve of the Ge/Si

heterojunction, as shown in figure 56(c). One can see that the threshold voltage of this heterojunction is only 0.3 V and the ideality factor of 1.1 of the heterojunction was achieved after post-annealing, indicating the excellent performance of the Ge/Si heterojunction.

### 1.3.6 Semiconductor interlayer bonding

Our group focused on the investigation of the Ge/Si wafer bonding and Ge/Si layer exfoliation based on an a-Ge interlayer between Ge and Si wafers [126,128,154,155]. Before bonding, we investigated the RMS of the a-Ge on the Ge substrate as a function of input power, as shown in figure 57(a). One can see that the variation trend of the curve is similar to that for the a-Ge film on the Si substrate. Finally, the a-Ge with RMS of 0.46 nm is selected for Ge/Si wafer bonding. In addition, the contact angles versus the thickness and the exposure time of the a-Ge layer on the Ge substrate were also investigated, as shown in figure 57(b) and (c), respectively. One can see that the a-Ge layer on the Ge substrate, whose thickness is larger than 2 nm, exhibits extremely hydrophilic. In addition, the hydrophilia also increases with the increase of the exposure time.

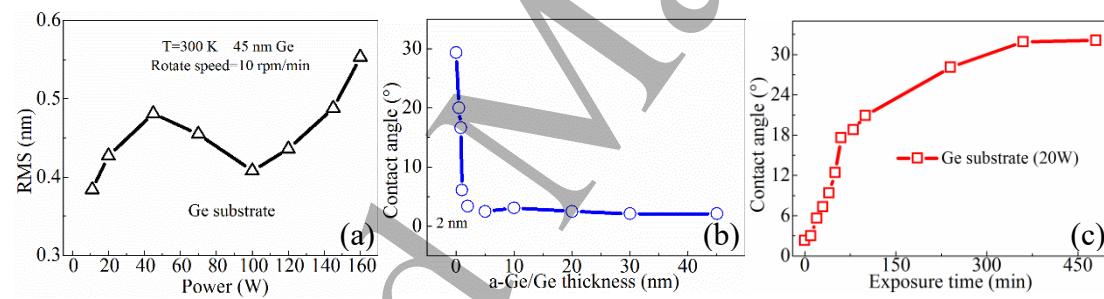


Figure 57. (a) RMS of the a-Ge film on the Ge substrate verse input power. Reprinted from [126], with the permission of AIP Publishing. (b) Contact angle verse a-Ge layer thickness.

Reprinted from [126], with the permission of AIP Publishing. (c) Contact angle verse exposure time. Reprinted from [126], with the permission of AIP Publishing.

For Ge/Si wafer bonding, we firstly studied the effect of the a-Ge layer thickness on the bubble density. After deposition of the a-Ge layer, the Ge and Si wafers were taken out of the chamber and directly bonded ( $\sim 1$  min). After that, the contacted wafers were annealed at  $300\text{ }^{\circ}\text{C}$  for 20 h. The CSAM images of the Ge/Si bonded interface are shown in figure 58. One can see that with the increase of the a-Ge layer thickness, the bubble density slightly increases. This is

attributed to the increase of the -OH groups absorbed on the a-Ge layer with the increase of the a-Ge layer thickness.

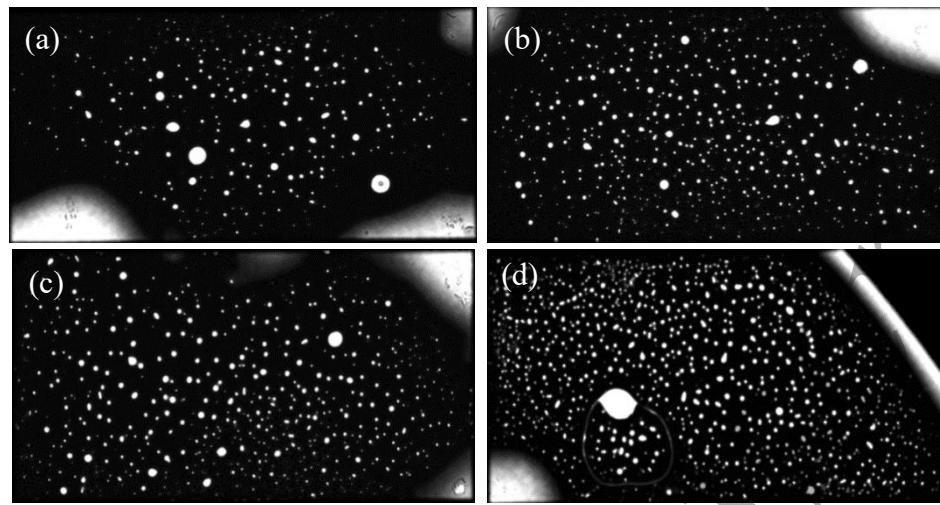


Figure 58. SAM images of the Ge/Si bonded interface with different a-Ge layer thickness. (a) 2 nm. (b) 5 nm. (c) 10 nm. (d) 20 nm.

We also studied the dependence of the bubble density of Ge/Si bonded wafers on the annealing time, as shown in figure 59(a) and (b). One can see that with the increase of the annealing time, the bubble density shows no change. This indicates that the by-products at the bonded interface is difficult to be transferred outside the wafer. In addition, when the temperature increases to 350 °C, as shown in figure 59(c), the bubble density slightly decreases and some small bubbles turn dark and dim. This may be due to the enhanced absorption of the by-products by the a-Ge film before crystallization when the annealing temperature was increased. However, the bubbles still exist at the bonded interface. In order to investigate the bubble density when the sample was annealed at 400 °C, we decreased the thickness of the Ge wafer to 20 μm before annealing due to the fact that if the contacted wafers were directly annealed at 400 °C, the wafers may separate due to the large thermal mismatch between Ge and Si. The SAM image of the Ge/Si bonded interface after annealing at 400 °C is shown in figure 59(d). One can see that the bubbles still exist at the bonded interface. High-temperature annealing still cannot significantly decrease the bubble density.

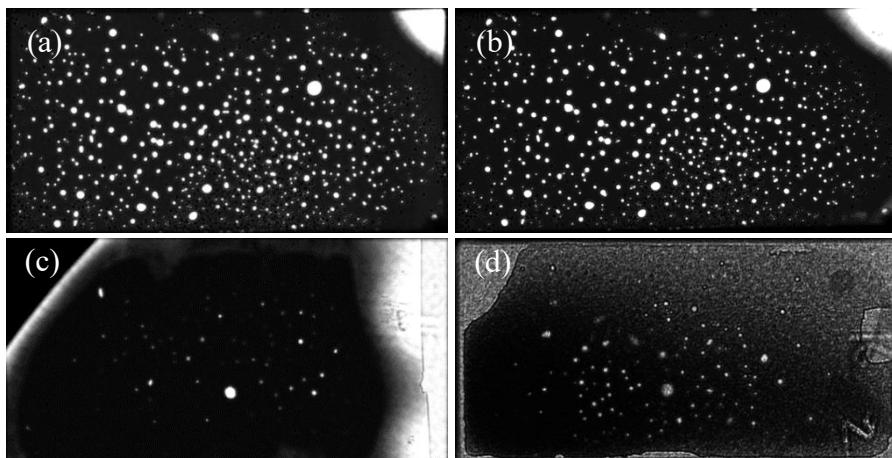


Figure 59. SAM images of the Ge/Si bonded interface annealed at 300 °C for (a) 20 h and (b) 60 h. Reprinted from [154], with the permission of IOP Publishing. SAM images of the Ge/Si bonded interface annealed at (c) 350 °C for 20 h and (d) 400 °C 20 h. Reprinted from [154], with the permission of IOP Publishing.

In order to further decrease the bubble density, we studied the bubble density as a function of exposure time (the time that the a-Ge layer was exposed to the air after sputtering and being taken out of the chamber), as shown in figure 60. One can see that with the decrease of the exposure time, the bubble density decreases. This is due to the fact that with the decrease of the exposure time, the -OH absorbed on the a-Ge layer decreases, leading to the decrease of the hydrophilic reaction (decrease of H<sub>2</sub>) at the bonded interface. When the exposure time was set to 3 s, a near-bubble-free Ge/Si bonded interface was achieved.

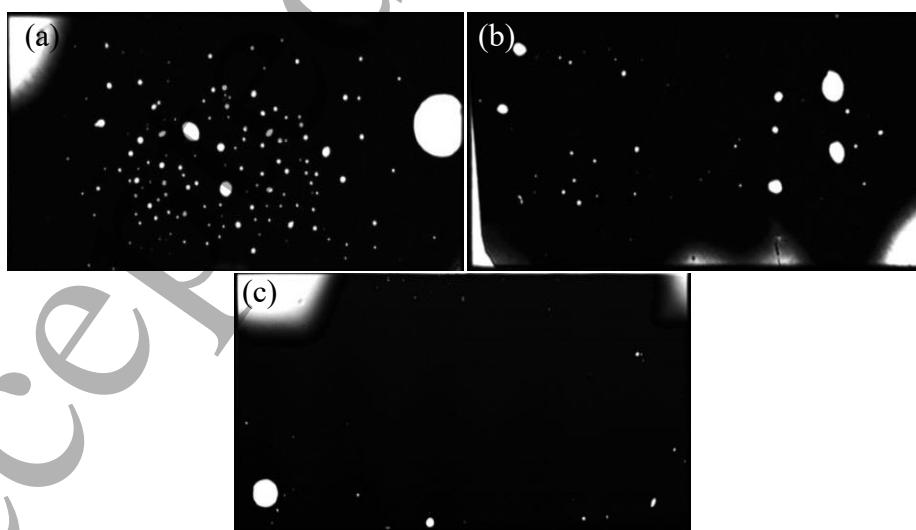


Figure 60. SAM images of the Ge/Si bonded interface bonded with the exposure time of (a) 20 s, (b) 10 s, and (c) 3 s. Reprinted from [154], with the permission of IOP Publishing.

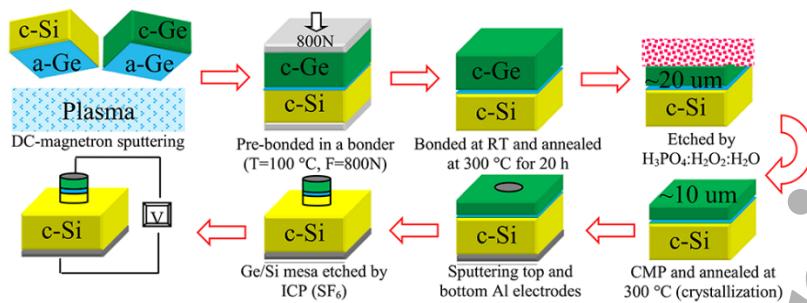


Figure 61. Fabrication process of the p<sup>-</sup>Ge/n<sup>+</sup>-Si heterojunction diode based on the Ge/Si interlayer wafer bonding. Reprinted from [154], with the permission of IOP Publishing.

We fabricated a p<sup>-</sup>Ge/n<sup>+</sup>-Si heterojunction diode based on the Ge/Si interlayer wafer bonding method, as shown in figure 61. The Ge wafer was chemical thinned and polished to 10 μm before the fabrication of the heterojunction diode. The effect of the annealing condition on the diode performance was investigated. The annealing condition of diode A is 300 °C for 20 h, that of diode B is 300 °C for 20 h and further 300 °C for 10 h, and that of diode C is 300 °C for 20 h and further 400 °C for 10 h. The IV curves of the heterojunction diodes are shown in figure 62(a). One can see that these three diodes all show the rectification characteristic and high on/off ratio of  $3.4 \times 10^5$  was achieved for diode B. This is higher than that of the p<sup>-</sup>Ge/n<sup>+</sup>-Si heterojunction diode fabricated by the plasma-activated bonding and dry bonding. This indicates that the quality of the Ge/Si bonded interface fabricated by the interlayer bonding is higher. The dependence of the I-V curve of the heterojunction diode is shown in figure 62(b). One can see that when the temperature decreases to 250 K, the dark current decreases sharply. This indicates that most of the recombination mechanism is restrained at near-room temperature. This is very important for the fabrication of the sensitive detectors (such as single-photon avalanche photodiode) operated at near-room temperature. On the other hand, a lower ideality factor was achieved for diode B (1.75 at 300 K and 1.02 at 150 K), as shown in figure 62(c).

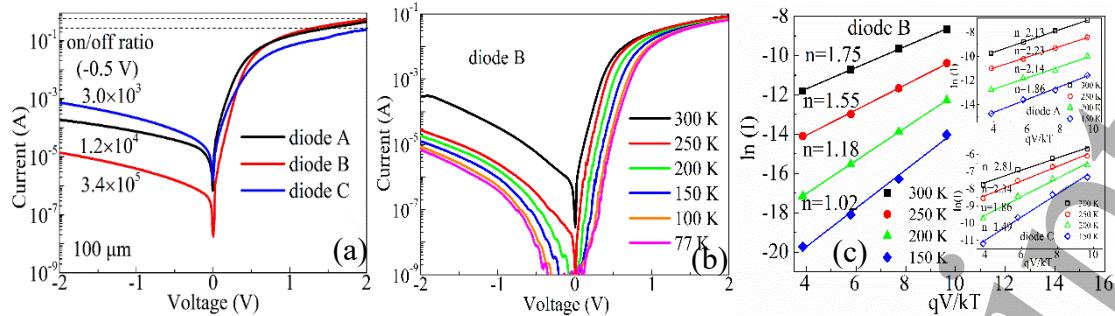


Figure 62. (a) I-V curves of the  $p^-$ -Ge/ $n^+$ -Si heterojunction diode ( $100\ \mu m$ ) based on the Ge/Si interlayer wafer bonding. Reprinted from [154], with the permission of IOP Publishing. (b) Temperature dependence of the I-V curve of diode B ( $200\ \mu m$ ). Reprinted from [154], with the permission of IOP Publishing. (c) Ideality factors of the heterojunction diodes. Reprinted from [154], with the permission of IOP Publishing.

In order to reveal the different electrical properties of the different diodes, the TEM examination of the Ge/Si bonded interface was conducted, as shown in figure 63. One can see that after annealing at  $300\ ^\circ C$  for 20 h, as shown in figure 63(a)-(d), the a-Ge at the Ge side has turned into single-crystal Ge (c-Ge) and that at the Si side still exhibits amorphous phase. In addition, an oxide layer appears at the Ge/Si bonded interface. More importantly, the TDs were not observed in the Ge wafer at the bonded interface. After further annealing at  $300\ ^\circ C$  for 10 h, as shown in figure 63(e)-(h), almost all of the a-Ge has turned into c-Ge, leaving 1-2 ML amorphous layer at the bonded interface. Note that the oxide layer disappears at the bonded interface and the TDs also cannot be observed after annealing. After further annealing at  $400\ ^\circ C$  for 10 h, as shown in figure 63(i)-(l), the a-Ge has totally turned into c-Ge, some distorted atoms appear at the bonded interface. Similarly, the oxide layer also cannot be observed at the bonded interface.

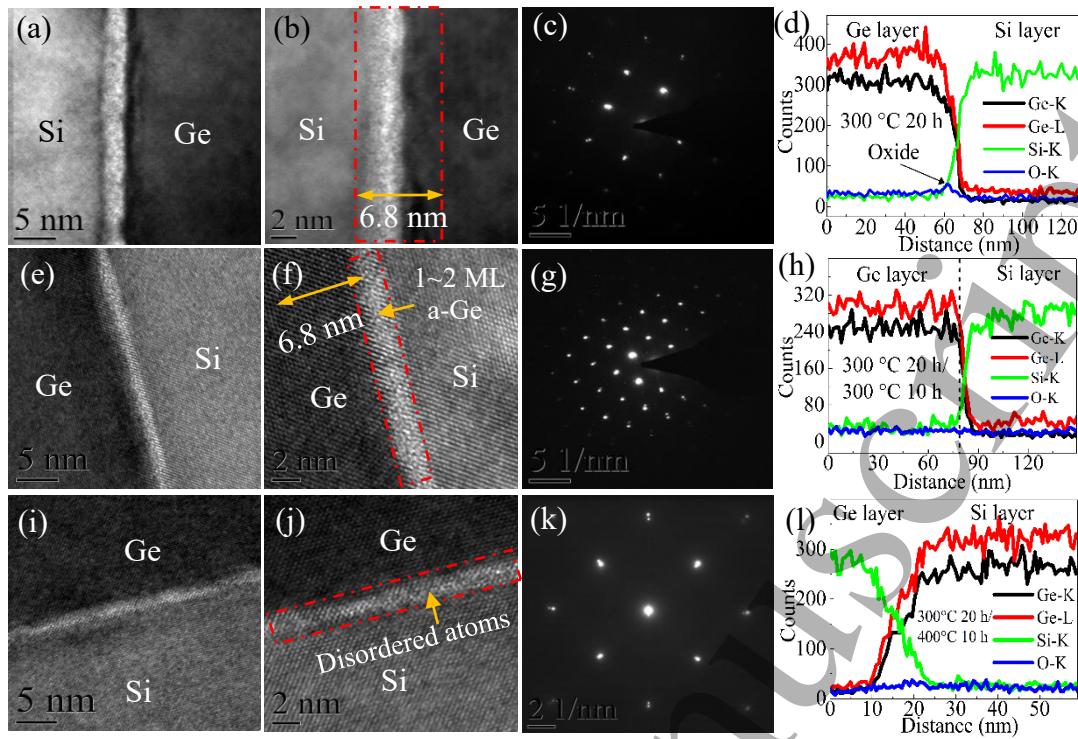


Figure 63. TEM images, electron diffraction, and EDS curves of (a)-(d) diode A, (b) diode (b), and diode (c). Reprinted from [154], with the permission of IOP Publishing.

In order to investigate the TDs in the Ge layer, the etch pit method was applied, as shown in figure 64. The TDs in diode B was extracted to be  $2.8 \times 10^3 \text{ cm}^{-2}$ , as shown in figure 64(a), and that in the diode C was extracted to be  $2.1 \times 10^5 \text{ cm}^{-2}$ , as shown in figure 64(b). Thus, the deterioration of the performance of diode C is due to the increase of the TDs in the Ge layer. In order to investigate the carrier mechanism at the bonded interface, the activation energy of the heterojunction diode was extracted, as shown in figure 64(c). One can see that the activation energy of diode B is 0.32 eV, thus the generation and recombination mechanism is dominated in diode B. The activation energy of diode C is 0.05, thus the BBT mechanism can be responsible for the carrier transport. The activation energy of diode A is 0.19 eV, thus the carrier migration at the bonded interface is the mixed mechanism of both the recombination mechanism and the BBT mechanism. The schematic diagrams of the carrier transport at the Ge/Si bonded interface are shown in figure 65.

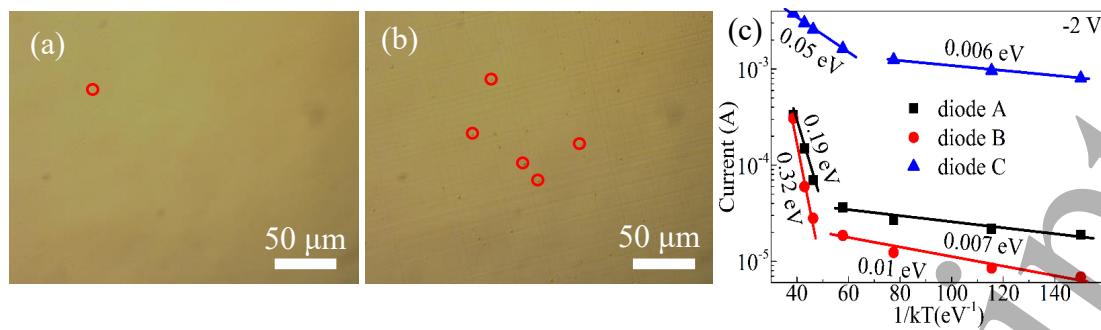


Figure 64. Optical microscope image of the Ge surface in the (a) diode B and (b) diode C etched in secoo solution for 60 s. Reprinted from [154], with the permission of IOP Publishing. (c) Activation energies of the three diodes at -2 V. Reprinted from [154], with the permission of IOP Publishing.

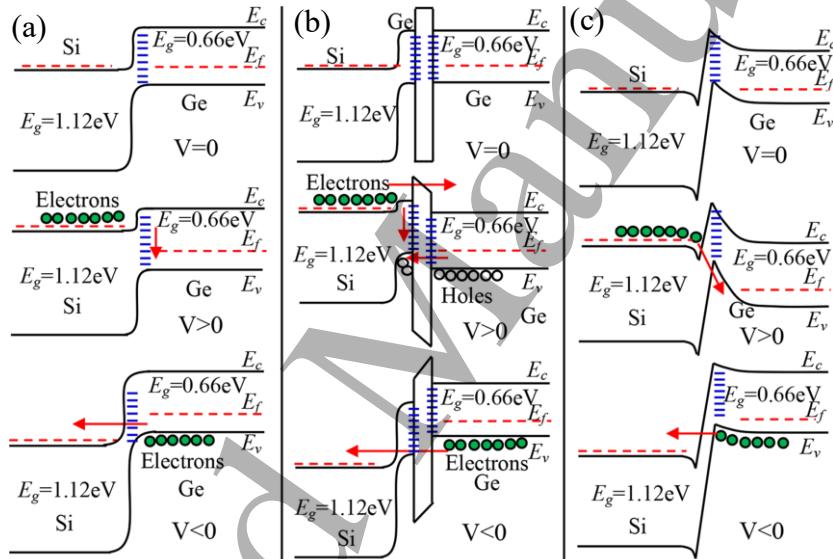


Figure 65. Schematic diagram of the carrier transport in (a) diode B, (b) diode A, and (c) diode C. Reprinted from [154], with the permission of IOP Publishing.

We also investigated the crystallization mechanism of the a-Ge film and the oxide layer evolution at the bonded interface. When the Ge/Si wafer pairs were annealed at 300 °C for 20 h, the a-Ge layer at the unbonded region still shows amorphous phase, as shown in figure 66(a)-(c), while that at the bonded region has crystallized, as shown in figure 66(d)-(f). We believe that the stress-induced crystallization of the a-Ge film at the bonded region can be responsible for this phenomenon. In order to reveal the crystallization process of the a-Ge film at the bonded interface, the Ge/SiO<sub>2</sub> wafer bonding with the a-Ge interlayer was also investigated. The TEM

image of the Ge/SiO<sub>2</sub> bonded interface is shown in figure 66(g)-(i). One can see that the a-Ge crystallizes from the Ge substrate. This is consistent with the Ge/Si wafer bonding.

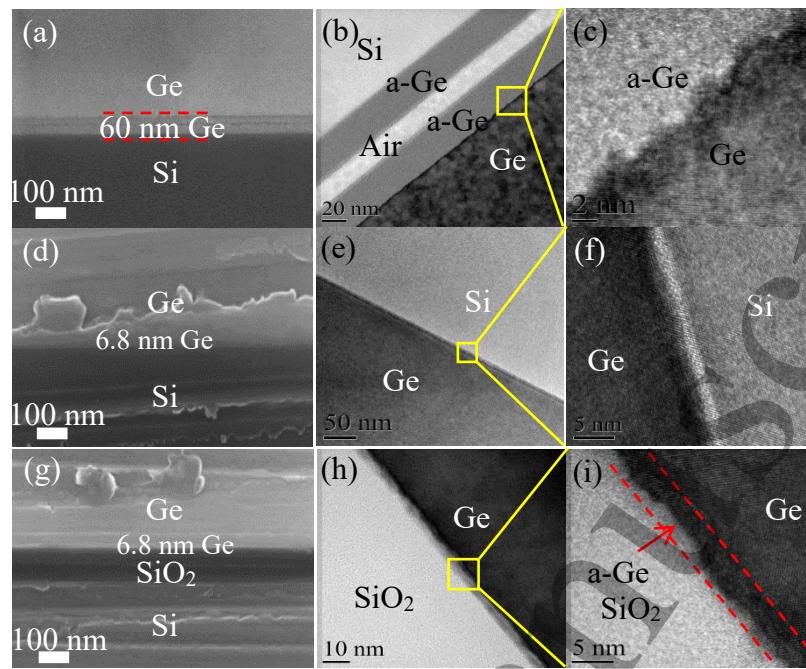


Figure 66. SEM images of the (a) unbonded region of the Ge/Si bonded interface, (d) bonded region of the Ge/Si bonded interface, and (g) bonded region of the Ge/SiO<sub>2</sub> bonded interface. TEM images of the (b)-(c) unbonded region of the Ge/Si bonded interface, (e)-(f) bonded region of the Ge/Si bonded interface, and (h)-(i) bonded region of the Ge/SiO<sub>2</sub> bonded interface. Reprinted from [128], with the permission of Springer.

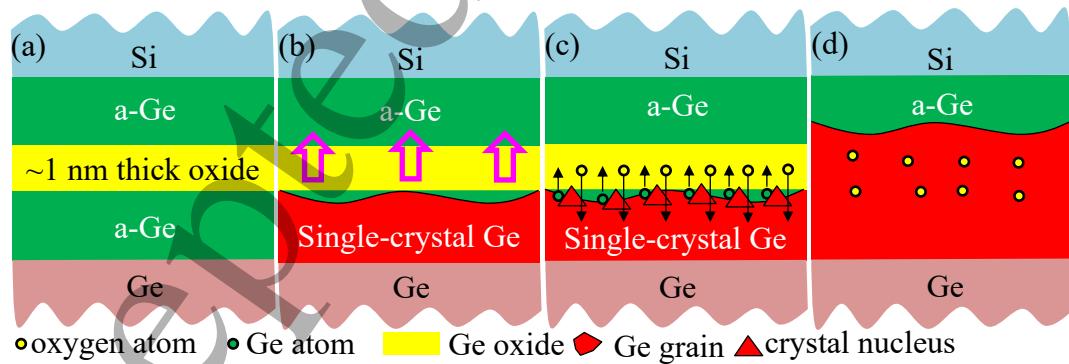


Figure 67. (a) and (b) Crystallization process of the a-Ge at the Ge/Si bonded interface. Reprinted from [128], with the permission of Springer. (c) and (d) Kinetic process of the Ge and oxygen atoms at the Ge/Si bonded interface. Reprinted from [128], with the permission of Springer.

In addition, no oxide layer was observed at the a-Ge/a-Ge bonded interface. Thus, the crystallization of the a-Ge film and the oxide layer evolution were drawn, as shown in figure 67. One can see that when the a-Ge shows amorphous phase, a thin oxide layer formed by the hydrophilic reaction appears at the a-Ge/a-Ge bonded interface. When the Ge/Si wafer pairs were annealed at 300 °C for 20 h, the a-Ge starts to crystallize from the Ge substrate and turns into the c-Ge induced by the Ge substrate. Due to the crystallization of the a-Ge, the atom migration becomes serious at the bonded interface, the Ge atoms migrate into the oxide layer and the O atoms migrate into the Ge layer, leading to the decomposition of the oxide layer at the bonded interface. Finally, the a-Ge totally crystallizes when 400 °C-annealing was conducted.

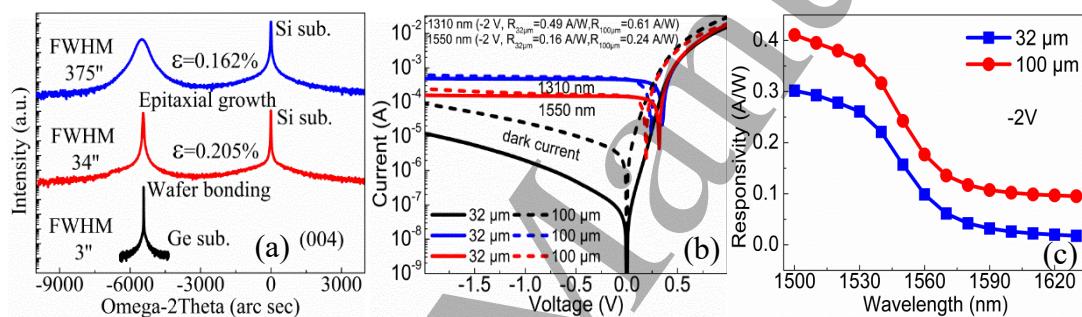


Figure 68. (a) XRD examination of the Ge(004) peak. Reprinted from [128], with the permission of Springer. (b) Photocurrent of the heterojunction diode. Reprinted from [128], with the permission of Springer. (c) Responsivity of the heterojunction diode verse wavelength. Reprinted from [128], with the permission of Springer.

We also fabricated a p<sup>-</sup>-Ge/n<sup>+</sup>-Si heterojunction diode with 1 μm thick Ge layer, the XRD examination of the Ge(004) peak is shown in figure 68(a). One can see that the FWHM of the wafer-bonded Ge film is only 34" which is much smaller than that of the epitaxial Ge film (375"). This indicates that the quality of the wafer-bonded Ge film is higher than that of the epitaxial Ge film. Figure 68(b) shows the I-V curve of the wafer-bonded Ge/Si photodetectors with the diameters of 32 and 100 μm. It can find that all the devices show good rectification characteristic. The responsivities of 0.49 and 0.61 A/W were achieved for the photodiodes with the diameter of 32 and 100 μm, respectively, at 1310 nm. In addition, the responsivity of 0.16

and 0.24 A/W was obtained at 1550 nm for these two devices, respectively. Figure 68(c) shows the responsivity of the heterojunction diode as a function of the wavelength. One can see that the responsivity of both photodiodes extends to 1560-1630 nm, which is beyond the absorption edge of the bulk Ge. This results from the Ge bandgap narrowing induced by the 0.205% tensile strain. The responsivity at 1630 nm is 94 and 17 mA/W for these two devices, respectively. This indicates that the wafer-bonded Ge/Si heterojunction photodiode is suitable for optical communication in all WDM bands, including the L-band and entire C band.

We also attempted to fabricate the Si-based Ge film by the interlayer wafer bonding and Smart-Cut technique. The H<sup>+</sup> implantation (dose of  $5 \times 10^{16}$  cm<sup>2</sup> and energy of 150 keV) was applied to create a defective blistered region below the Ge surface. Before Ge/Si wafer bonding, a 2 nm thick a-Ge layer was deposited on the substrate. The exposure time of 3 s was set for near-bubble-free wafer bonding. After contact, the wafer pairs were successively annealed at 150 °C under a force of 2 MPa for 1 h, 250 °C under a force of 0.5 MPa for 1 h, 350 °C without force for 1 h, and 400 °C without force for 1 h to trigger the exfoliation of Ge film. The whole bonding process was under a chamber pressure of 10<sup>-5</sup> mbar.

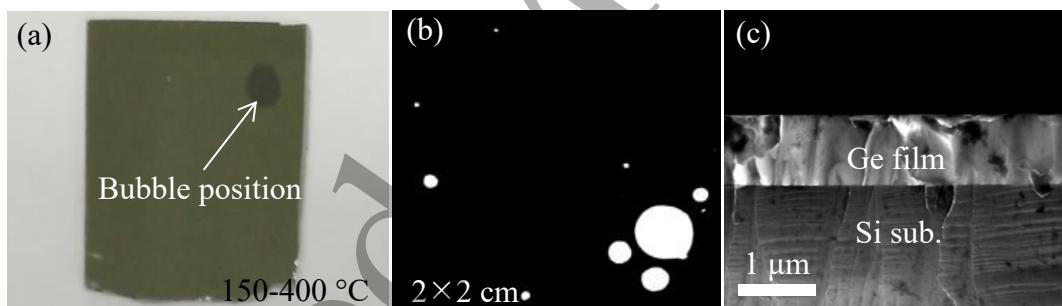


Figure 69. (a) Camera image of the exfoliated Ge film. Reprinted from [155], with the permission of IEEE Xplore Digital Library. (b) SAM image of the Ge/Si bonded interface. Reprinted from [155], with the permission of IEEE Xplore Digital Library. (c) SEM image of the Ge/Si bonded interface. Reprinted from [155], with the permission of IEEE Xplore Digital Library.

The camera image of the exfoliated Ge film is shown in figure 69(a). One can see that most of the Ge film was transferred onto the Si substrate. Only one bubble bursts on the Si substrate. The SAM image and SEM image of the Ge/Si bonded interface are shown in figure 69(b) and

(c), respectively. One can see that few bubbles appear at the Ge/Si bonded interface, indicating that less hydrophilic reactions appear at the bonded interface due to the short exposure time of a-Ge. The Ge film is uniformly located on the Si substrate and no creaks were observed at the bonded interface.

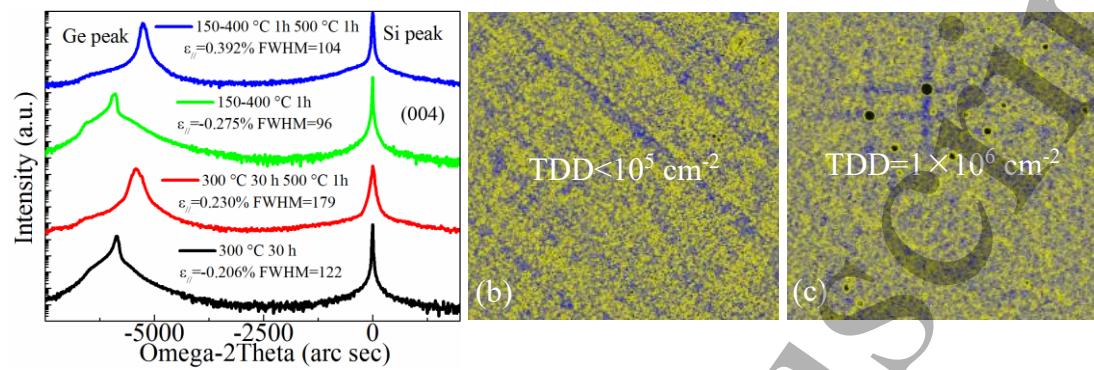


Figure 70. (a) XRD curves of the exfoliated Ge film annealed at different temperature.

Reprinted from [155], with the permission of IEEE Xplore Digital Library. AFM images of (b) the as-exfoliated Ge film and (c) the exfoliated Ge film post-annealed at 500 °C for 1 h etched in secco solution for 10 s. Reprinted from [155], with the permission of IEEE Xplore Digital Library.

The XRD peak of the Ge film is shown in figure 70(a). One can see that the exfoliated Ge film exhibits 0.275% compression strain and the FWHM of the exfoliated Ge film is 96" which is also smaller than that of the epitaxial one, while it is slightly larger than that of the thinning one shown above. There is a shoulder peak at the left side of the Ge(004) peak which results from the interference effects between the substrate and the strained layers created by the H<sup>+</sup> implantation [156-158]. This indicates that the strain in the Ge film is nonuniform. In addition, the shape of the Ge peak of the as-exfoliated Ge film is unusual. The upper half of the Ge peak is sharp, while the bottom half is broad. This is due to the point defects in the as-exfoliated Ge film induced by the H<sup>+</sup> implantation. In order to eliminate the point defects, high-temperature annealing (500 °C) was conducted for 1 h. The XRD peak is shown in figure 70(a). One can see that after post-annealing, the shape of the Ge peak becomes symmetrical and the bottom half of the Ge peak becomes narrow, indicating the relaxation of the nonuniform strain and the repair of the point defects in the Ge film. However, the FWHM of the Ge film (104") slightly increases. This is due to the increase of the TDs when high-temperature

annealing was conducted, as shown in figure 70(b) and (c). One can see that the number of the TDs in the as-exfoliated Ge film is less than  $10^5 \text{ cm}^{-2}$ , and that in the post-annealed Ge film increases to  $10^6 \text{ cm}^{-2}$ . More importantly, the peak position shows right-shift after post-annealing, the compression strain turns into tensile strain (0.392%) after post-annealing.

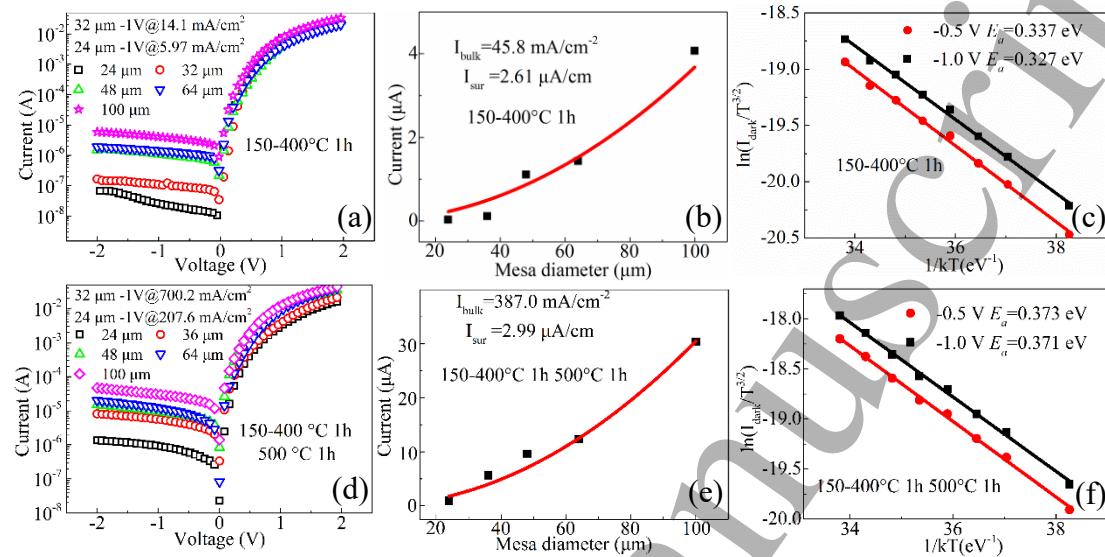


Figure 71. (a) IV-curves, (b) current verse mesa diameter, and (c) activation energy of the Ge/Si p-i-n photodiode based on the as-exfoliated Ge film. Reprinted from [155], with the permission of IEEE Xplore Digital Library. (d) IV-curves, (e) current verse mesa diameter, and (f) activation energy of the Ge/Si p-i-n photodiode based on the exfoliated Ge film annealed at 500 °C for 1 h. Reprinted from [155], with the permission of IEEE Xplore Digital Library.

We fabricate two wafer-bonded Ge/Si p-i-n photodiodes by the exfoliated Ge film. The dark current of the p-i-n photodiode based on the as-exfoliated Ge film is shown in figure 71(a). One can see that low dark current of  $5.97 \text{ mA/cm}^2$  was achieved for the 24 μm-diameter mesa at -1 V and that of  $14.1 \text{ mA/cm}^2$  was achieved for the 32 μm-diameter mesa. These values can be comparable with that of the epitaxial Ge/Si p-i-n photodiode. The dark current of  $207.6 \text{ mA/cm}^2$  was achieved for the p-i-n photodiode based on the exfoliated Ge film annealed at 500 °C for 1h with the 24 μm-diameter mesas. The increase of the dark current of the post-annealed p-i-n photodiode is attributed to the increase of the TDs in the Ge film. The increase of the TDs leads to the increase of the bulk current density, as shown in figure 71(b) and (e).

The activation energy of the photodiode was also extracted, as shown in figure 71(c) and (f). One can see that the activation energies of both photodiodes are close to 0.33 eV, indicating that the recombination mechanism is dominated in both photodiodes.

The photocurrents of the photodiodes are shown in figure 72(a) and (b). One can see that the responsivities of the photodiode based on the as-exfoliated Ge film at 1310 and 1550 nm were obtained to be 0.304 and 0.221 A/W, respectively, and that based on the exfoliated Ge film annealed at 500 °C for 1 h increases to 0.475 and 0.381 A/W, respectively. The increase of the responsivity is ascribed to the 0.392% tensile strain in the Ge film after post-annealing. The ideality factors of these two devices are shown in figure 72(c). It is shown that the ideality factor of 1.19 of the device without post-annealing was achieved, while that increases to 1.56 after post-annealing. The deterioration of the performance of the device is due to the increase of the TDs in the Ge film after post-annealing.

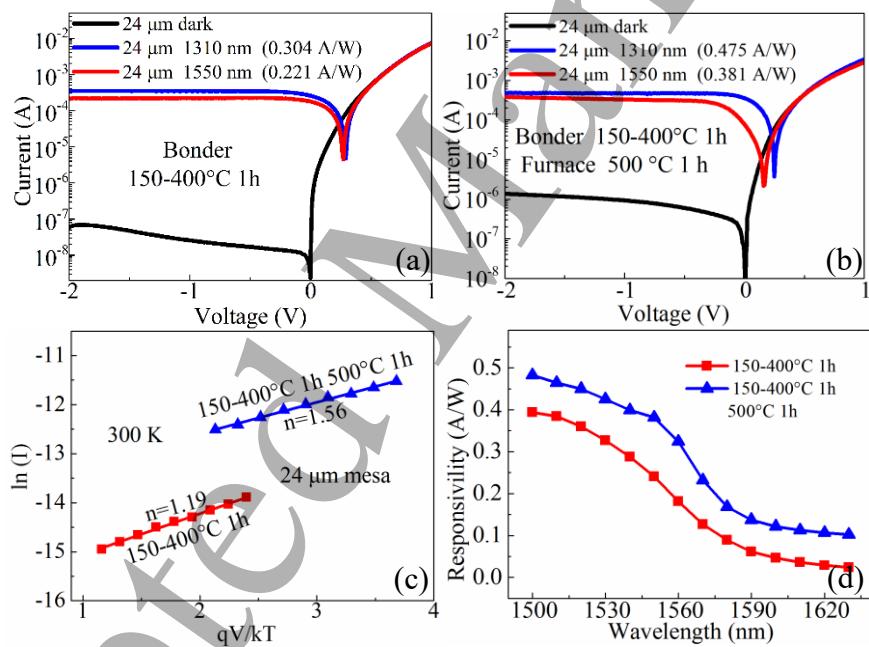


Figure 72. (a) and (b) Photocurrent of the Ge/Si p-i-n photodiode based on the as-exfoliated Ge film and the exfoliated Ge film annealed at 500 °C for 1h, respectively. Reprinted from [155], with the permission of IEEE Xplore Digital Library. (c) Ideality factor and (d) responsivity verse wavelength of the photodiode. Reprinted from [155], with the permission of IEEE Xplore Digital Library.

#### 1.4 Outlook of Si/Si wafer bonding and Ge/Si wafer bonding

The investigation of Si/Si wafer bonding is mature at present. We can easily achieve the Si/Si bonded wafer pairs with high bonding strength, low bonded temperature, bubble-free bonded interface. These features are basic requirements in MEMS. However, it is difficult to apply Si/Si wafer bonding technique to the photoelectric field at present. Due to the fact that the carriers should transport through the Si/Si bonded interface for the photoelectric devices, it is satisfied to lower the potential barrier at the bonded interface for the carrier transport and to restrain the carrier recombination. The difficulty for the application of the Si/Si wafer bonding in the photoelectric field can be concluded as follow. (1) The oxide layer at the Si/Si bonded interface should be totally eliminated at the bonded interface. (2) The Si/Si bonded interface should exhibit the electrical properties of bulk Si. (3) Small bubbles (several nanometers), which are difficult to be detected by the IR transmission technique or the CSAM technique, should be eliminated. These small bubbles may lead to the leakage current at the Si/Si bonded interface. The research direction for Si/Si wafer bonding in the future should focus on the replacement of the epitaxial Si layer with wafer-bonded (exfoliated) Si layer. For example, the epitaxial Si multiplication layer in the Ge/Si avalanche photodiode can be replaced by wafer-bonded Si layer. This may lead to the decrease of the dark current of the device and the decrease of the dark count rate and afterpulsing probability of the related Ge/Si single-photon avalanche photodiodes.

The study of Ge/Si wafer bonding and the photoelectronic device based on this technique is still insufficient. Using this technique, we can fabricate a Si-based Ge film without TDs at low temperature. The quality of wafer-bonded Ge film is hopeful to be higher than that of epitaxial one. This is due to the low-temperature achievement of the covalent bond at the bonded interface. Low-temperature annealing can eliminate the TD nucleation and diffusion at the bonded interface. However, many problems still need to be solved in the bonded process, such as how to further lower the bonding temperature, how to totally eliminate the small bubbles at the bonded interface, how to fundamentally eliminate the misfit dislocation, how to exfoliate the whole Ge film on the Si substrate, and how to effectively repair the point defects in the Ge film without introduction of the TDs.

The research direction of Ge/Si wafer bonding can be concluded as follow. (1) Some

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3 porous materials can be introduced at the Ge/Si bonded interface to absorb the by-product at  
4 the bonded interface. (2) Increasing the implantation dose of the H<sup>+</sup> to further decrease the  
5 exfoliation temperature of the Si-based Ge film. (3) Introduction of amorphous material or  
6 polycrystalline material at the Ge/Si bonded interface to eliminate the misfit dislocations. (4)  
7 Etching the implantation damage in Ge film to further enhance the Ge film quality. (5) Short-  
8 time high-temperature annealing method can be applied to improve the Ge film quality, such as  
9 nanosecond-pulsed laser annealing.

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