Surface plasmons and breakdown in thin silicon dioxide films on silicon

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The anode hole injection model is based on a surface plasmon model in which the positive charge is generated by hole injection from the anode, where it is generated via a surface plasmon mechanism resulting finally in oxide breakdown. Attempts to detect the surface plasmons can rely only on indirect observations, such as electron-energy loss, the radiative decay of the surface plasmons, or d^2I/dV^2 measurements. These measurements show that the emission of surface plasmons is both a strong energy-loss mechanism and an electron-hole pair generation mechanism, particularly in poly-Si/SiO_2 or poly-Si/vacuum interfaces. Calculation of the surface plasmon excitation threshold energy is shown to decrease with increasing temperature and is also confirmed by experiments. Thus, the positive charge density increases and the charge to breakdown decreases with increasing temperature. We have also measured and observed the surface plasmon excitation threshold energy at the poly-Si/SiO_2 interface from the electron energy loss spectrum for the first time. The surface plasmon mechanism explains the oxide thickness and gate thickness dependence of the positive charge density and temperature dependence of the charge to breakdown. The calculated electron threshold energy to generate a positive oxide charge by the surface plasmon mechanism is $E_{C-Si}+2.24$ eV. Also, the origin of substrate hole current can be explained by this proposed mechanism. Therefore, the anode hole injection model based upon surface plasmons is a reasonable thin oxide breakdown model that explains measured observations. © *1998 American Institute of Physics.* [S0021-8979(98)01714-9]

I. INTRODUCTION

Dielectric breakdown, one of the major failure mechanisms for metal-oxide-semiconductor (MOS)-very large scale integrate (VLSI) integrated circuits, has become more important as the gate oxide thickness is continually reduced. The wearout and breakdown of thin SiO_2 films has been extensively studied. A model involving local hole trapping and oxide field buildup during Fowler–Nordheim electron tunneling[1,2] has been proposed to explain oxide breakdown. The positive oxide charge (hole trapping) causes a reduced Fowler–Nordheim tunneling path and a lower effective barrier height for electrons due to the image charge effect.[2,3] However, because of a lack of a physics-based model, there has been persistent concern over the severity and even the existence of positive oxide charge buildup when the power supply voltage decreases from 5 to 3.3 V [soon to be 2.5 V in future generations of sub-0.5-μm Si complementary MOS (CMOS) integrated circuits].

Several mechanisms have been presented to explain positive charge generation by electron fluence.[3–6] For thick oxides, the impact ionization model for electron-hole pair generation in the oxide bulk shows reasonable agreement with experiments when the breakdown voltage is larger than the band gap energy of SiO_2.[3] For thin oxides, even though the apparent breakdown field is somewhat higher than that of thick oxides, the breakdown voltage is less than the threshold energy of impact ionization. Although the surface plasmon model for the generation of positive charge for thin oxides has been suggested,[4–6] this model has not been verified experimentally for poly-Si gate MOS capacitors with thin SiO_2.

Attempts to detect the surface plasmons must rely only on indirect observations, such as electron-energy loss,[7–9] radiative decay of the surface plasmons,[10–14] or d^2I/dV^2 measurements.[15–20] Measurements of this kind have been performed[7–20] in the past and actually show that the emission of surface plasmons is a strong energy-loss mechanism, particularly in thin metal films. Among the possible experiments, the electron energy loss spectrum (EELS) and the second derivative current–voltage $(I-V)(d^2I/dV^2)$ measurements are presented in this research.

Previous results showed that the surface plasmon excitation threshold energy of Si is nearly equal to the theoretical value[21–23] and the quantum efficiency was enhanced up to 30% for MOS junctions by the surface plasmons.[24–26] Tsui[16,17] has observed a broad peak in d^2I/dV^2 curves which corresponds to an increase in conductance at bias voltages near the surface-plasmon energy in GaAs. These measure-

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ments led Tsui to explain his observations as due to the excitation of surface plasmons in GaAs by tunneling electrons. The square-root dependence on electron concentration in the GaAs electrode is consistent with his interpretation. Duke *et al.*[19] have also reported the observation of a broad doping-dependent structure in the d^2I/dV^2 characteristic very similar to that of Tsui.

It has been observed that the surface plasmon excitation threshold energy is dependent on the temperature and its value lies in the range expected by theoretical calculations. The surface plasmon excitation threshold energy decreases with increasing temperature. Thus, the positive charge density increases and charge to breakdown decreases with increasing temperature, which is in agreement with previous published results.[27] We have observed that the surface plasmon is a strong energy loss mechanism and a source of electron-hole pair generation. We have also observed that the surface plasmon excitation threshold energy is about 8 or 11 eV at the poly-Si/SiO_2 interface or poly-Si/vacuum interface, respectively. These observations were obtained from the d^2I/dV^2 measurement. Furthermore, we have measured the surface plasmon excitation threshold energy of 7.5 eV at the poly-Si/SiO_2 interface from the EELS measurement for the first time. This value is close to the theoretical value. The surface plasmon mechanism well explains the oxide thickness and gate thickness dependences of the positive charge density and the temperature dependence of the charge to breakdown. The electron threshold energy to generate a positive charge by the surface plasmon mechanism accounts for the lower power supply voltage for ultrathin oxides and the origin of substrate hole current.

In this article, we propose that the positive charges are injected holes from the anode[28] which are generated by the decay of the surface plasmons to electron-hole pairs in the anode for the thin SiO_2 samples. The locally trapped holes increase the positive charge (and thus the cathode field) at such points in the oxide, causing the tunneling current density to increase in those locations (a positive feedback effect). When the density of trapped-oxide positive charge at one of such locations reaches a certain critical value, the local tunneling current is increased to the point that breakdown occurs.

II. EXPERIMENTAL PROCEDURES

Poly-silicon gate MOS capacitors were fabricated on 4 in. diameter, (100) oriented p-type wafers with a resistivity of 4–7Ω cm. A p-type epitaxial layer grown on the substrate formed the basis for either the n- or p-well capacitors. A 5×10^{13} cm^{-2}, 170 keV phosphorus implant formed the n-well and a 2.3×10^{13} cm^{-2}, 170 keV boron implant formed the p well. Silicon dioxide was then grown with a thickness of 73 Å and a phosphorus or boron-doped 3500 Å polysilicon layer deposited on top of the oxide as the gate electrode. The active sizes of the n^+ poly-Si gate with p well and the p^+ poly-Si gate with n-well capacitors were 1.03×10^{-3} and 9.47×10^{-4} cm^2, respectively. These samples were then used for the second derivative $I-V$ measurement.

The second derivative (d^2I/dV^2) experiments have been performed by Tsui[16,17] (in n-type GaAs–Pb surface-barrier tunnel junctions) and by Duke *et al.*[18,19] (in n-type GaAs–In contacts). Tsui has observed a broad peak in d^2I/dV^2 curve which corresponds to an increase in conductance at bias voltages near the surface-plasmon energy in GaAs. These measurements led Tsui to explain his observations as due to the excitation of surface plasmons in GaAs by tunneling electrons. Its square-root dependence on electron concentration in the GaAs electrode is consistent with his interpretation. Duke, Rice, and Steinrisser[19] have also reported the observation of a broad doping-dependent structure in the d^2I/dV^2 characteristic very similar to that of Tsui. They associate this structure with electron–bulk–plasmon interaction in the GaAs electrode. However, the position and the shape of the structure in d^2I/dV^2 resulting from their theoretical calculation do not agree with the experimental results.[19] We believe that the origin of the aforementioned tunneling anomaly is not due to (BP),[20] and that the strong structure calculated by Duke *et al.*[19] is spurious arising from an overestimation of the electron-BP interaction.[20]

Other samples with different process parameters were used for the electron energy loss spectrum measurement. The silicon substrates were (100)-oriented, 7 Ω cm, p-type silicon of 0.15 mm thickness. A 1.6 μm, 12 Ω cm, p-type epitaxial layer grown on the substrate formed the basis for either n- or p-well capacitors. A 4×10^{12} cm^{-2} phosphorus implant formed the n well and a 3.5×10^{12} cm^{-2} boron implant formed the p well. The wells were isolated by a modified localized oxidation of silicon (LOCOS) process. Silicon dioxide was then grown with a thickness of 175 Å and 5×10^{13} cm^{-2} phosphorus or boron-doped polysilicon layer deposited on top of the oxide as the gate electrode. The active sizes of the p- and n-well capacitors were 7.42×10^{-5} and 7.67×10^{-5} cm^2, respectively.

An HP4142B DC/Source Monitor and a Micromanipulator Model HSM temperature controller with a temperature range of 27–200 °C were used for the second derivative $I-V$ measurement. During voltage ramp determination, the current was limited to 10 mA and the voltage was limited to 10 V in order not to overstress the devices. An HP4145B Semiconductor Parameter Analyzer was used for the second derivative $I-V$ measurement. The capacitors were biased into accumulation mode tunneling by applying negative bias to the poly-Si gates of the p-well capacitor. The first derivative $I-V$ data were obtained using the HP4145B Semiconductor Parameter Analyzer and HSM temperature controller with a temperature range of 27–200 °C. The second derivative $I-V$ data were then extracted using computer software (Kalieda Graph).

The electron energy loss spectrum of the devices were taken with a Philips 400 FEG transmission electron microscope (TEM) with a field emission gun operating at 80 and 100 keV.

III. ANODE HOLE INJECTION: THIN OXIDE BREAKDOWN MODEL

Figures 1 through 3 display the hole generation efficiency (I_p/I_g), Q_{BD}, and the positive charge density as a

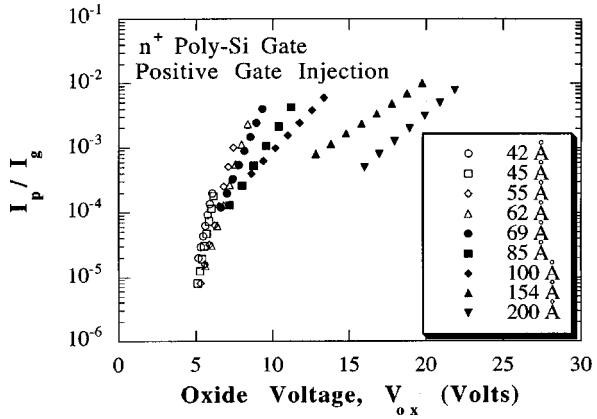

FIG. 1. The ratio of substrate hole current to gate tunneling current vs oxide voltage of n^+ poly-Si gate samples with different oxide thicknesses. The points are taken from Refs. 36 and 46.

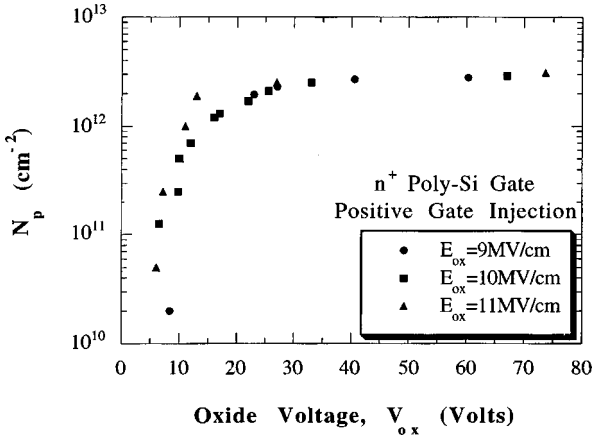

FIG. 3. Positive charge density vs oxide voltage of n^+ poly-Si gate samples with oxide electric field as a parameter. The experimental points are taken from references in Ref. 38.

function of the total voltage applied to the insulator V_{ox} for n^+ poly-Si gate samples. This procedure emphasizes the dependence on V_{ox} itself. Figure 4 displays the charge to breakdown as a function of the total voltage applied to the insulator V_{ox} for n^+ poly-Si gate samples. As can be seen in these figures, the threshold V_{ox} for I_p/I_g, Q_{BD}, and the positive charge density is around 5 or 2.6 V for the oxide thickness of 50 or 25 Å, respectively. These values are well below the threshold for the previously published models. Therefore, a reasonable model should be developed to explain these observations.

The anode hole injection model is based on the heating of electrons in the SiO_2 and their energy losses at the SiO_2/anode interface.[4–6] The electrons do heat up in SiO_2 and their transport can be understood, to first order, without invoking collision events in the bulk SiO_2 in which several eV are released. However, as soon as the electrons enter the anode electrode, their energy must be somehow lost. Low-energy electrons in a solid can lose energy mainly to phonons, electron-hole pairs, or plasmons. The phonons are ignored, since their energy is too low. Electron-hole pairs are usually generated with a relatively low efficiency, because the electrons are screened in a conductor (or semiconductor) and the strength of the Coulomb interaction is reduced.[5] Bulk-plasmon generation is less affected by the Coulomb screening,[5] but the high energy of the plasmons should inhibit this process in thin MOS structures. But *plasmons at the interface between a conductor and a dielectric*—called *surface plasmons* (SP)—are generated when the electrons are still unscreened in the insulator and they occur at much lower energies.

The proposed model is schematically illustrated in Fig. 5. At sufficiently large fields, electrons are injected into the conduction band of the oxide by Fowler–Nordheim tunneling. The injected electrons gain energy during their transport in the oxide. A significant fraction of the accelerated electrons lose energy at the anode/SiO_2 interface by emitting surface plasmons. Once excited, the surface plasmons decay quickly into electron-hole pairs. A small fraction of these holes can be injected into the SiO_2 and are trapped at localized areas. Hole traps are thought to be caused by oxygen vacancies in the bulk and/or dangling bonds at the surface. Locations with such a propensity to trap positive charge are postulated to make up only $\sim 10^{-6}$ of the total oxide area.[1] The locally trapped holes increase the positive charge (and thus the cathode field) at such points in the oxide, causing the tunneling current density to increase there (a positive feedback effect). When the density of trapped-oxide hole

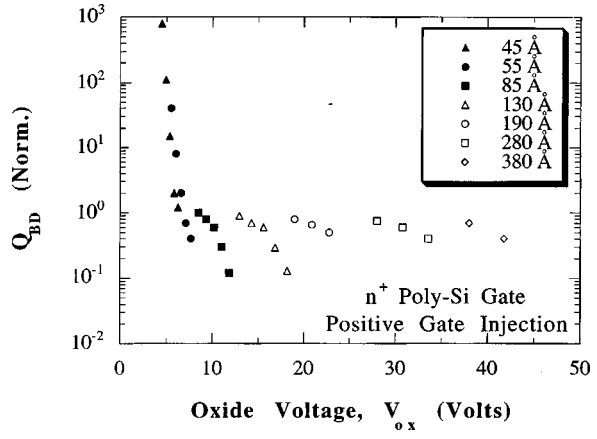

FIG. 2. Charge to breakdown vs oxide voltage of n^+ poly-Si gate samples with different oxide thicknesses. The points are taken from Refs. 44 and 46–48.

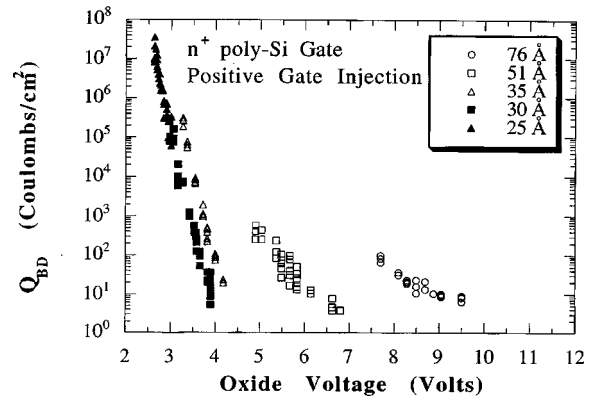

FIG. 4. Charge to breakdown as a function of oxide voltage (Ref. 38).

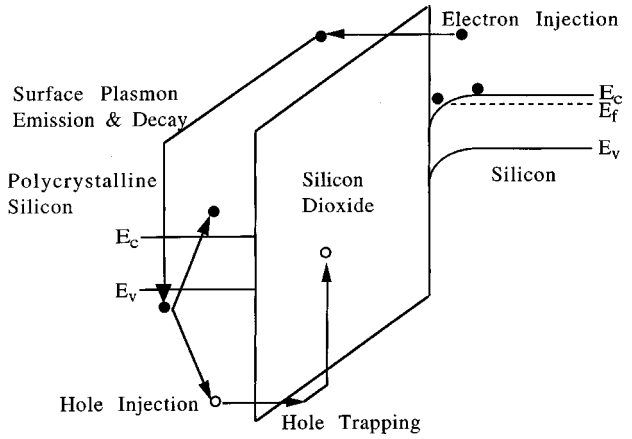

FIG. 5. Schematic diagram of positive charge generation and hole trapping.

charge at one of such locations reaches some critical value, the local tunneling current is increased to the point that breakdown occurs.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Second derivative *I–V* measurement

Recent observation of carrier-concentration-dependent broad peak in d^2I/dV^2 curves in n-type GaAs-metal tunnel junctions[16,17] has been interpreted as resulting from emission of surface plasmons in the GaAs electrode by tunneling electrons. The expression for the second derivative of the excess tunneling current due to electron–surface plasmon interactions corresponds to the broad peak in d^2I/dV^2 curves. The broad peak in the d^2I/dV^2 represents an increase in conductance at bias voltages near the surface plasmon excitation threshold energy in the semiconductor.[15–20]

The broad peaks in d^2I/dV^2 curves are also observed in poly-Si gate MOS structures. Figures 6 and 7 display these broad peaks for n^+ and p^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å versus temperature. The bias voltage of the peaks in the second derivative curves are dependent on the temperature. In Fig. 6, for n^+ poly-silicon

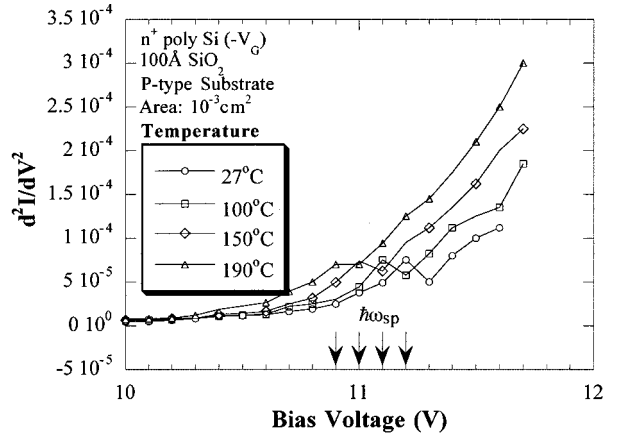

FIG. 6. The second derivative $I-V$ vs gate bias voltage curves of the n^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å with different temperatures as the parameter.

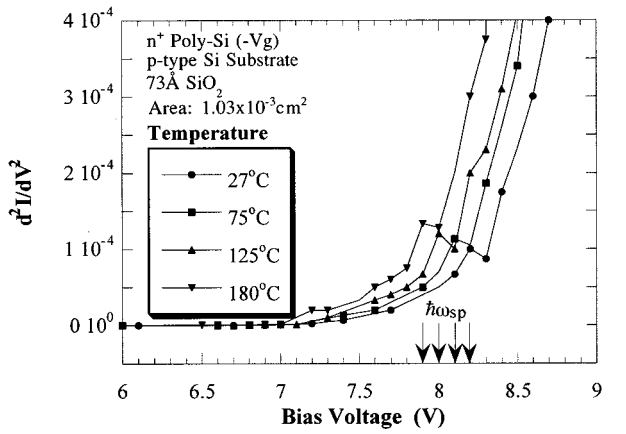

FIG. 7. The second derivative $I-V$ vs gate bias voltage curves of the n^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å with different temperatures as the parameter.

gate, the peaks move from 8.2 V at 27 °C to 7.9 V at 180 °C. This variation is due to the surface plasmon excitation at the poly-Si/vacuum interface for p-well capacitors. In Fig. 7, for n^+ poly-silicon gate, the peaks also move from right to left with increasing temperature. These peaks are due to surface plasmon excitations at the poly-Si/SiO_2 interface for p-well capacitors. The peaks correspond to an increase in conductance at bias voltages equivalent to the excitation threshold energy at the Si or the poly-Si/SiO_2 interface. These slight conductance increases are also observable in curves of dV/dI versus bias voltage.[16]

Theoretically, the volume plasmon energy $\hbar\omega_P$ of Si is calculated from the following equation:

$$\hbar\omega_P=\hbar\left(\frac{nq^2}{m_0\epsilon_0}\right)^{1/2}, \tag{1}$$

where n is the density of valence electrons, q is the electron charge, m_0 is the free electron mass, and ϵ_0 is the dielectric constant of the free space.[21–23] Referring to the above equation, we know that the value of $\hbar\omega_P$ depends upon the valence band electron density and thus it is a function of temperature due to lattice thermal expansion.[29–31] Note that the energy ($\hbar\omega_P$) of such a wave is greater than the binding energy of the electrons so that the valence electrons hardly feel the effect of the periodic crystal potential and behave as if they were ''free.'' [32]

Figure 8 shows the upper and lower bounds (solid lines) of the theoretical values calculated for the surface plasmon excitation threshold energy at the SiO_2/anode interface as a function of temperature. These theoretical values are obtained from the following equation:[22,26]

$$\hbar\omega_{SP}=\frac{\hbar\omega_p}{\sqrt{1+\epsilon}}, \tag{2}$$

where ϵ is the dielectric constant of SiO_2. In this equation, the variations of the valence band electron density and the dielectric constant due to the change of temperature should also be considered. Upper and lower bounds represent the range of reported data and are obtained by substituting the lattice thermal expansion coefficients reported in Refs. 29,

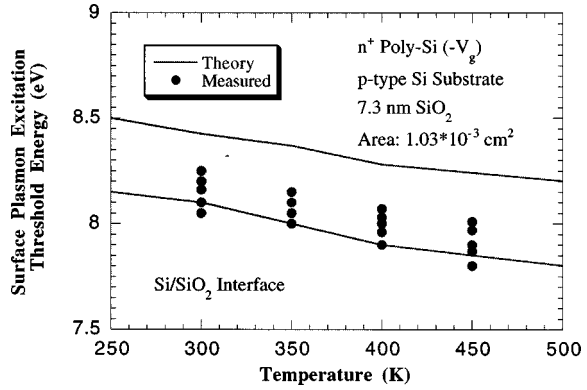

FIG. 8. Measured and theoretical values of the surface plasmon excitation threshold energy plotted as a function of temperature for the n^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å. Upper theoretical bound calculated using data from Refs. 27, 29, and 30. Lower bound calculated from Refs. 29, 31, 33, and 34.

and 30, or 31 into Eq. (1) and the dielectric constant presented in Refs. 27, or 33 and 34 into Eq. (2), respectively.

Detailed data on the measured surface plasmon excitation threshold energy, $\hbar w_{SP}$, together with the theoretical values on the investigated n^+ or p^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å are shown in Figs. 8 and 9. These figures show excellent agreement between the theoretical values and measured data. The surface plasmon excitation threshold energy decreases with increasing temperature. Thus, the positive charge density increases and charge to breakdown decreases with increasing temperature. This is in good agreement with previously published results which showed the temperature dependence of the charge to breakdown.[27]

B. Electron energy loss spectrum (EELS)

The characteristic energy losses of electrons in solids have been studied experimentally by many workers.[7–9] The electron energy loss spectrum gives an important insight into the variety of excitations of solids. The information is obtained by measuring the energy losses ΔE which the electrons, fast or slow, suffer by transmission through a thin film of a solid or by reflection at its boundary. The transmission is

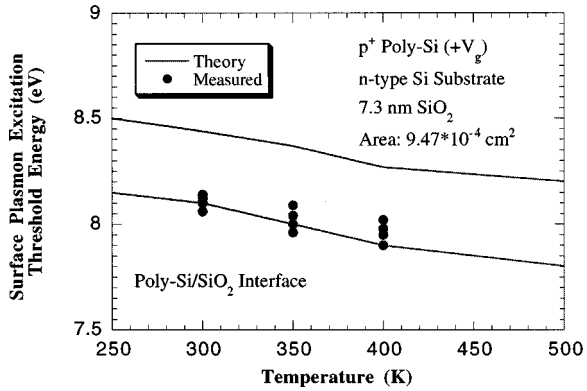

FIG. 9. Measured and theoretical values of the surface plasmon excitation threshold energy plotted as a function of temperature for the p^+ poly-Si gate MOS capacitors with an oxide thickness of 73 Å.

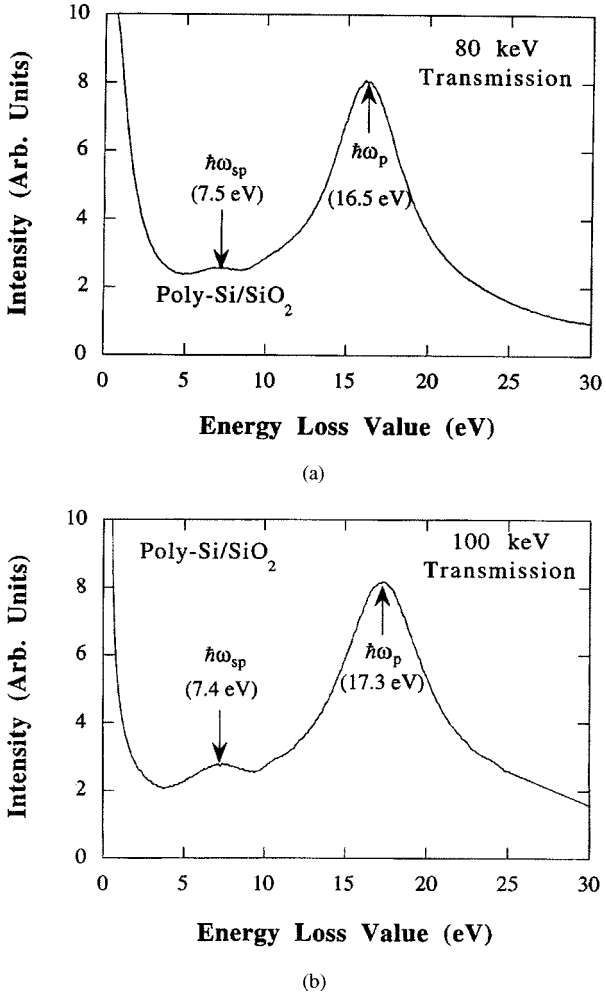

FIG. 10. Characteristic electron energy loss spectrum of poly-Si/SiO_2/Si (CMOS) structure with measuring at: (a) 80 and (b) 100 keV. $\hbar w_{SP}$ is the surface plasmon energy at poly-Si/SiO_2 interface and $\hbar w_p$ is the bulk plasmon energy of poly-Si.

mainly used in experiments with fast electrons of some 10 keV or more, whereas the reflection method is well adapted for low energy electrons of about 100 eV or less which cannot penetrate thin films in general. In the experiments, the Philips 400 FEG transmission electron microscope (TEM) was used with field emission gun operating at 80 and 100 keV.

Figures 10(a) and 10(b) show the characteristic electron energy loss spectrum of poly-Si/SiO_2/Si (CMOS) structure. The surface plasmon energy at the poly-Si/SiO_2 interface is $\hbar w_{SP}$ and the bulk plasmon energy of poly-Si is $\hbar w_p$. The peak at 0 eV is due to the primary unscattered electron beam. The surface plasmon energy at the poly-Si/SiO_2 interface is observed as approximately 7.45 ± 0.05 eV. This is the first time that the surface plasmon energy at the poly-Si/SiO_2 interface has been observed in the electron energy loss spectrum. A large peak located at 16.9 ± 0.4 eV is related to the bulk plasmon energy of the poly-Si. Figures 11(a) and 11(b) also show the characteristic electron energy loss spectrum of the poly-Si/SiO_2/Si (CMOS) structure. However, $\hbar w_{SP}$ for this case is the surface plasmon energy at the poly-Si/vacuum interface. The surface plasmon energy at the poly-

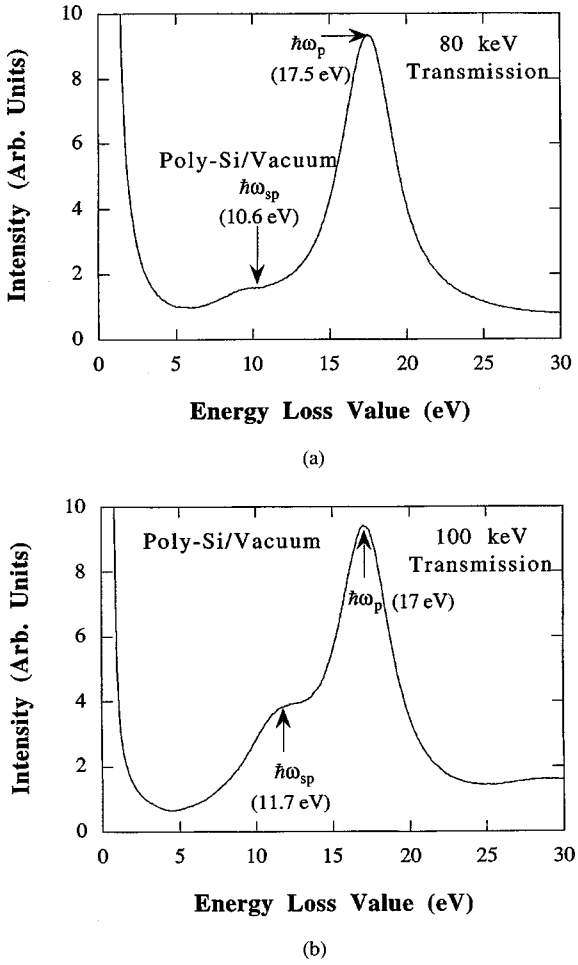

FIG. 11. Characteristic electron energy loss spectrum of poly-Si/SiO_2/Si (CMOS) structure with measuring at: (a) 80 and 100 keV. $\hbar w_{SP}$ is the surface plasmon energy of poly-Si vacuum interface.

Si/vacuum interface is about 11.1 ± 0.6 eV which is close to the theoretical value,

$$\hbar\omega_{SP} = \frac{\hbar\omega_p}{\sqrt{1+\epsilon_0}} \approx 11.2 \text{ eV}.$$

In many solids, the electron energy loss value agrees well with the energy value of the plasma oscillation calculated by the free electron theory as we described earlier. The characteristic energy loss of electrons in silicon has been studied experimentally by many workers[21–23] yielding excellent agreement with theoretical values.

V. THE ROLE OF SURFACE PLASMONS ON THIN OXIDE BREAKDOWN

A. Electron threshold energy

The theoretical threshold oxide voltage drop to generate the positive charge due to surface plasmon mechanism for ultrathin oxide samples will now be developed. Figure 12 shows the transition energy diagram of n^+ poly-Si gate MOS structures for positive oxide charge generation by the surface plasmon mechanism. Some incident tunneling electron arrives at the anode with energy, E_e, which is elastically transferred to a valence band electron, thereby exciting it to the

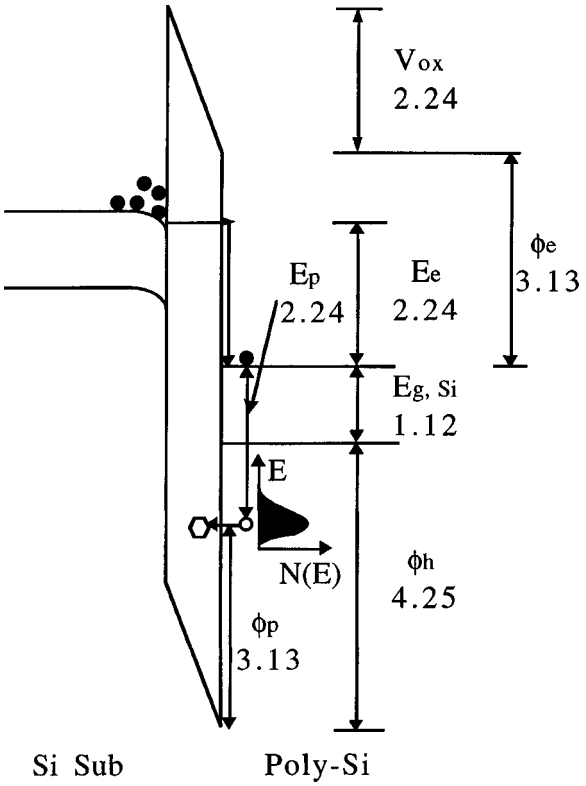

FIG. 12. The transition energy diagram of poly-Si gate MOS structures for positive charge generation.

lowest available energy state, that is, the anode conduction band via decay of surface plasmons. This excitation creates a ''hot'' hole capable of tunneling back into the oxide. E_e is simply V_{ox} for direct tunneling. An inspection of Fig. 12 shows that the threshold oxide voltage drop is

$$\begin{aligned} V_{\text{O threshold}} &= E_{g,\text{SiO}_2} - \phi_e - \phi_p \\ &= E_{g,\text{SiO}_2} - \phi_e - (\phi_h + E_{g,\text{Si}} - E_p) \\ &= E_p \\ &= 2(E_{g,\text{Si}}) = 2(1.12) = 2.24 \text{ V}. \end{aligned}$$

Figure 13 displays the charge to breakdown as a function of incident electron energy into the anode electrode for n^+

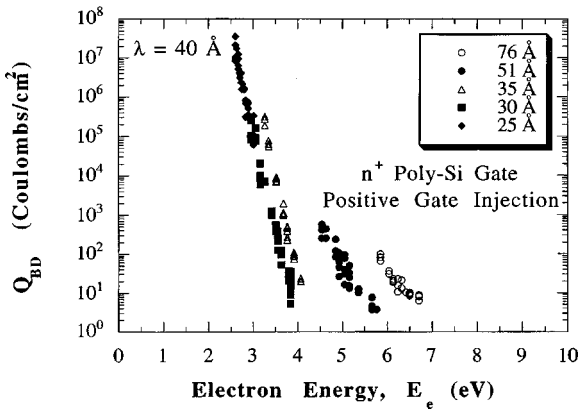

FIG. 13. Charge to breakdown as a function of the incident electron energy into anode electrode (Ref. 38).

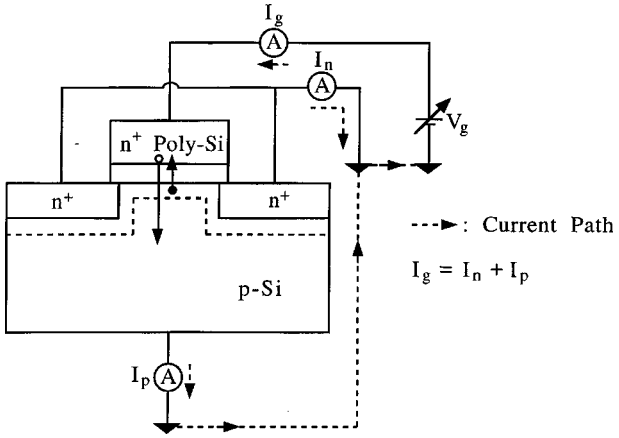

FIG. 14. Schematic illustration of the substrate hole current measurement circuit (Refs. 36 and 37).

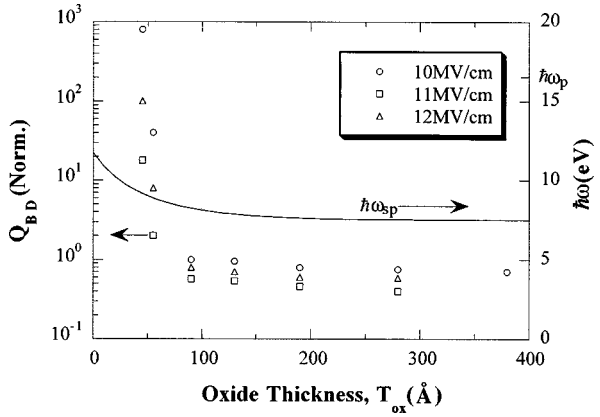

FIG. 15. Charge to breakdown and surface plasmon threshold energy vs SiO_2 thickness.

poly-Si gate samples. As can be seen in this figure, the threshold electron energy is around 2.6 eV for the oxide thickness of 25 Å. As the maximum energy the electrons can gain drops below the energy required to generate a surface plasmon at the anode/SiO_2 interface, no more charge to breakdown is observed. This value is well below the threshold for interband impact ionization in Si (5.37 eV) and interband Auger recombination (4.25 eV) by Lu and Sah.[35]

If holes are injected from the anode, carrier-separation structures [such as *n*-channel field-effect transistor (FETs)] should allow the observation of the hole-current in the substrate. Figure 14 displays the schematic illustration of the substrate hole current measurement circuit. When the gate of a large-area *n*-channel MOSFET is positively biased with source and drain grounded, the gate current I_g is almost entirely due to the electron F–N tunneling current I_n flowing between the surface inversion layer and the gate. However, a small ($\sim 1\%$ I_g) but easily measurable hole current, I_p, also flows out of the substrate.[36,37] This also has been observed, even below the threshold for interband impact ionization. From this discussion, we can conclude that the surface plasmon mechanism is a hole generation mechanism for thinner gate oxides.

B. Oxide thickness dependence

The electron mean free path in SiO_2 is about 15–40 Å.[36,37] If the silicon dioxide thickness is larger than the electron mean free path, the impact ionization coefficient a is only a function of the oxide electric field. Also, the impact ionization in Si is not related to the oxide thickness. If the silicon dioxide thickness is smaller than the electron mean free path, the impact ionization coefficient a is a function of oxide electric field and thickness, however the oxide voltage V_{ox} is too low for impact ionization in SiO_2. Note that, the surface plasmon threshold energy is a function of t_{ox} for thin SiO_2.[38] In addition, the total energy the electron gains as it travels to the gate is a function of t_{ox}. Therefore, we can explain the SiO_2 thickness dependence of Q_{BD}, N_p, and I_p/I_n or I_p/I_g for thin SiO_2 as shown in Figs. 1–4.

The electron tunneling current, I_n, is not a function of the SiO_2 thickness, t_{ox}, because F–N tunneling theory shows only an oxide electric field dependence. However, the substrate hole current, I_p, is a function of t_{ox} because the source of holes is the decay of the surface plasmons for thin silicon dioxide samples.[38] The total gate current is equal to the sum of I_n and I_p as shown in Fig. 14. Since the electron tunneling current is much higher than the hole current, the gate current is almost equal to the electron tunneling current. Therefore, the gate current is not a function of oxide thickness. However, the ratio of the substrate hole current to gate or electron current is a function of oxide thickness as shown in previous work.[38] These results are also shown in Fig. 1. For thick SiO_2 samples, I_p/I_g and I_p are not a function of t_{ox} because the source of holes is the impact ionization in SiO_2.

Figure 15 shows the charge to breakdown and surface plasmon threshold energy versus SiO_2 thickness with different oxide electric field as a parameter. Observe that the charge to breakdown increases with decreasing oxide thicknesses because the surface plasmon threshold energy increases and the total energy of electron decreases with decreasing oxide thickness.

C. Temperature dependence

Recently published results showed that the charge to breakdown decreases with increasing temperature.[27,38–41] Since impact ionization is predicted to decrease with increasing temperature, it would imply that the charge to breakdown should also increase with temperature.[39] Lu and Sah[35] also noted temperature independence of interband impact ionization in Si. However, the surface plasmon excitation threshold energy decreases with increasing temperature as shown in Figs. 6–9. Since the surface plasmon excitation threshold energy shows a decrease with temperature above 100 K, the regime where breakdown is controlled by surface plasmons should show a similarly strong temperature dependence. Increasing the lattice temperature should lower the charge to breakdown. Figures 16 and 17 display theoretical values of the surface plasmon excitation threshold energy and experimental Q_{BD} data plotted as a function of temperature. In these figures, some of the charge to breakdown data from Refs. 41–43 for Fig. 16 and Refs. 44 and 45 for Fig. 17 have been replotted as a function of temperature and compared to

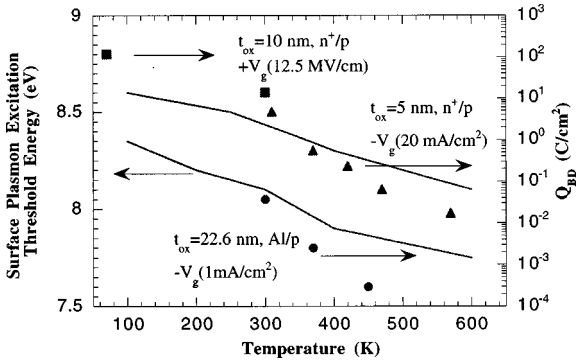

FIG. 16. Theoretical value of the surface plasmon excitation threshold energy and experimental Q_{BD} data (Refs. 41–43) plotted as a function of temperature.

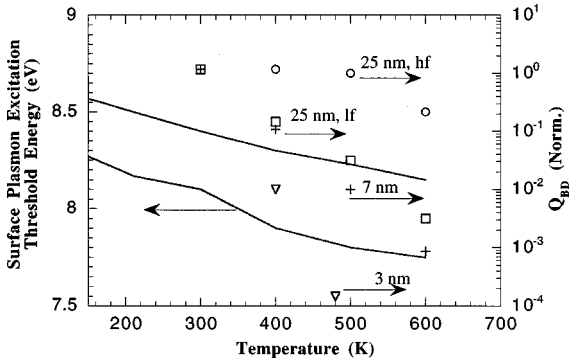

FIG. 17. Comparison of normalized charge to breakdown from Refs. 44 and 45 and surface plasmon excitation threshold energy as a function of temperature.

data for the temperature dependence of surface plasmon excitation threshold energy. In Fig. 17, each data set has been normalized to its corresponding value at room temperature. Average oxide fields determined from reported current densities are 11.8, 11.0, and 10.5 MV/cm on the 30, 70, and 250-Å-thick oxides, respectively, at low fields (lf). The high field (hf) data on the 250-Å-thick oxide were obtained at 12.8 MV/cm. The two different regimes of surface plasmons and impact ionization are apparent in these data. The high field (hf) Q_{BD} for the 250 Å oxides is dominated by positive charge production from impact ionization and shows the weak temperature dependence as expected. All other data in Figs. 16 and 17 are dominated by positive charge produced by the surface plasmon mechanism which has a stronger temperature dependence. Also, the low field (lf) Q_{BD} for the 250 Å oxides (see Fig. 17) and 226 Å oxides (see Fig. 16) are dominated by positive charge production from the surface plasmon mechanism and show the strong temperature dependence as discussed. The 30-Å-thick oxide structures are in the range of applied voltages near the 3 eV threshold for positive charge generation where a greater sensitivity to temperature variations would be expected. Furthermore, the surface plasmon mechanism (therefore, Q_{BD}) of these very thin oxides would reflect the added temperature sensitivity of the electron source in the contacting electrodes because most of the electrons traverse the film in a near ballistic manner.[45] Both of these factors would explain the stronger temperature dependence observed in Fig. 17 on the 30-Å-thick films. From the above results and discussion, we can rule out the interband impact ionization in SiO_2 and Si as the positive charge generation mechanism and the origin of the substrate hole current for thin oxides.

VI. CONCLUSIONS

It has been observed that the surface plasmon excitation threshold energy is dependent on the temperature and its value lies in the range expected by theoretical calculations. The surface plasmon excitation threshold energy decreases with increasing temperature. Thus, the positive charge density increases and charge to breakdown decreases with increasing temperature. This is in good agreement with previously published results. We have observed that the surface plasmon is a strong energy loss mechanism and a source of electron-hole pair generation. We have also observed that the surface plasmon excitation threshold energy is about 7.9 eV or 11.1 ± 0.6 eV at the poly-Si/SiO_2 or poly-Si/vacuum interface, respectively. These observations were obtained from the d^2I/dV^2 measurements. Furthermore, we have observed that the surface plasmon excitation threshold energy is around 7.5 or 11.1 eV(average) at the poly-Si/SiO_2 or poly-Si/vacuum interface from the EELS measurements for the first time, respectively. These values are in good agreement with the theoretical values. The surface plasmon mechanism explains quite well the oxide thickness dependence of the positive charge density and temperature dependence of the charge to breakdown. The electron threshold energy to generate a positive charge by the surface plasmon mechanism also accounts for the lower power supply voltage for ultrathin oxides and the origin of substrate hole current.

Finally, we conclude that the positive charges are injected holes from the anode which are generated by decay of the surface plasmons to electron-hole pairs in the anode for the thin SiO_2 samples. The locally trapped holes increase the positive charge (and thus the cathode field) at such points in the oxide, causing the tunneling current density to increase there and provide a positive feedback effect. When the density of trapped-oxide positive charge at one of these locations reaches some critical value, the local tunneling current is increased to the point that breakdown occurs.

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