Correlated Nonideal Effects of Dark and Light *I–V* Characteristics in a-Si/c-Si Heterojunction Solar Cells

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Abstract—a-Si/c-Si (amorphous Silcon/crystalline Silicon) heterojunction solar cells exhibit several distinctive dark and light I-V nonideal features. The dark I-V of these cells exhibits unusually high ideality factors at low forward-bias and the occurrence of a "knee" at medium forward-bias. Nonidealities under illumination, such as the failure of superposition and the occurrence of an "S-type" curve, are also reported in these cells. However, the origin of these nonidealities and how the dark I-V nonidealities manifest themselves under illumination, and vice versa, have not been clearly and consistently explained in the current literature. In this study, a numerical framework is used to interpret the origin of the dark I-V nonidealities, and a novel simulation technique is developed to separate the photo-current and the contact injection current components of the light *I–V*. Using this technique, the voltage dependence of photo-current is studied to explain the failure of the superposition principle and the origin of the S-type light I-V characteristics. The analysis provides a number of insights into the correlations between the dark I-V and the light I-V. Finally, using the experimental results from this study and from the current literature, it is shown that these nonideal effects indeed affect the dark I-V and the light I-V in a predictable manner.

Index Terms—Amorphous Silicon, current-voltage (*I-V*) characteristics, heterojunctions, modeling, simulation, process control, Silicon.

I. INTRODUCTION

INDING a cost-effective alternative to traditional c-Si solar cells has been a major driving force in the development of a-Si/c-Si (amorphous Silcon/crystalline Silicon) heterojunction solar cell technology [1], [2]. These so-called "HITTM" cells have demonstrated efficiencies exceeding 24% [3], comparable with those of the champion c-Si solar cells [4]. However, the

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complex heterojunction structure makes optimization of these cells more challenging.

An important step towards designing high-quality solar cells is to understand the nonidealities in carrier transport that can degrade the solar cell performance. An analysis of the dark *I–V* and the light I-V provides insights into the nonidealities of carrier transport that affect a-Si/c-Si solar cell efficiency. In the literature, the *low forward-bias transport* (in the dark) is generally attributed to two mechanisms—namely, multi-tunneling capture emission across the a-Si region [5] or diffusion flux across the barrier [6]. The two mechanisms are distinguished by the temperature dependence of the slopes of the dark *I–V* characteristics plotted in a semilog plot. Under *high forward-bias*, carrier transport appears to be dominated by diffusion [7], [8]. In the medium forward-bias range, however, it is frequently observed that there are a number of the nonideal features in the dark I-V, such as unusually high ideality factors (\gg 2), occurrence of a "knee" etc. [5], [6], [8]–[12], irrespective of the low-bias transport mechanism. The physical origins of these features are not fully understood. A consistent explanation of these features in the dark I-V may provide a renewed perspective in the analysis and optimization of these cells.

Likewise, several studies in the literature discuss the distinctive features of the light I–V characteristics of a-Si/c-Si heterojunction solar cells. In these solar cells, it is known that superposition may or may not hold upto the $V_{\rm OC}$ point. This failure of superposition appears to be correlated to the process details in fabricating the cell [13]–[15]. Indeed, several experimental reports (e.g., [16]–[19]) have suggested a link between the properties of a-Si and the occurrence of a nonideal "S-type" curve under certain circumstances. Furthermore, numerical modeling was used to understand the transport mechanism under light, using tunneling across the a-Si/c-Si interface and drift-diffusion-based transport [20], as well as hot-carrier-based transport [21]. These studies were mainly confined to understanding the light I–V properties, with no specific effort to correlate the features to the dark I–V.

Das *et al.* [17] reported a comprehensive set of both experimental dark I–V and light I–V characteristics obtained by varying the a-Si process conditions [22]. Based on the shape of the light I–V characteristics, the authors summarize their dark and light I–V observations into three categories, labeled here as: "Type-1", "Type-2", and "Type-3" responses, as shown in Fig. 2(b)–(d). Using the Suns-V_{OC} measurement under white, blue, and infrared light, they postulated that the presence of a barrier to minority carrier (hole) conduction may cause the

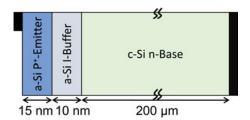


Fig. 1. Diagram of P⁺/I/n a-Si/c-Si heterojunction solar cell.

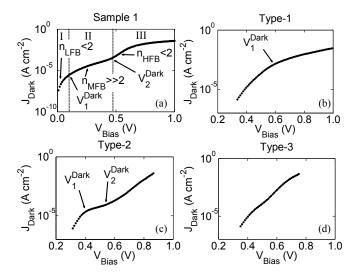


Fig. 2. (a) Shunt corrected dark I–V of Sample A used in this study is plotted. The bias where the ideality factor crosses 2 $(V_{\rm Bias} = V_1^{\rm Dark})$ and bias where the ideality factor drops below 2 $(V_{\rm Bias} = V_2^{\rm Dark})$ are marked. The vertical lines separate the different bias regions. (b) The measured dark I–V of a Type-1 sample is plotted [17]. The $V_1^{\rm Dark}$ is also indicated for this sample. (c) The measured dark I–V of a Type-2 sample is plotted [17]. The $V_1^{\rm Dark}$ and $V_2^{\rm Dark}$ are also indicated. (d) The measured dark I–V of a type-3 sample, which is referred to as "good fill-factor" device in [17] is plotted. There is no unusually high ideality region observed for this sample in the plotted bias range.

S-type curve in some of the samples. However, this study was mainly focused on understanding the light I-V behavior, and the authors did not correlate the dark and the light I-V characteristics from a device physics perspective. In this paper, we will use the same dark and light I-V dataset (along with our own measurements) to establish the physical origin of the correlation between the dark and light I-V characteristics.

In Section II, we explore the origin of the nonideal features in the dark I–V characteristics. In Section III, we use a novel simulation technique to isolate the photo-current and the contact injection current components of the light I–V characteristics. In Section IV, the nonideal effects of the dark I–V and light I–V characteristics are correlated, and the experimental data are interpreted based on the theory developed in Sections II and III. Finally, in Section V, we discuss the effects of interface defects on the analysis of the dark I–V characteristics.

II. PHYSICS OF CARRIER TRANSPORT IN THE DARK

A. Experimental Observations

Industrial-grade $P^+/I/n$ solar cell samples were used in this study. The P^+ a-Si emitter and an intrinsic a-Si buffer layer

TABLE I SUMMARY OF MEASURED DARK I–V RESULTS

	Shunt Parameters			Forward Bias Parameters			
Sample	G_{Sh}	J_{0Sh}	γ	n_{MFB}	V_2^{Dark}	J_0	n_{HFB}
Identifier	S cm ⁻²				V	A cm ⁻²	
	x10 ⁻⁵	x10 ⁻⁸				$x10^{-10}$	
A	1.7	1.8	1.0	3.7	0.48	0.4	1.2
В	1.6	1.7	2.0	4.1	0.49	8.0	1.5
C	1.9	1.8	1.0	3.9	0.47	2.1	1.3
D	3.9	1.6	0.9	3.7	0.47	93	1.7
E	1.6	0.6	2.0	3.0	0.42	11	1.4

The shunt parameters are extracted from the measured dark I-V data using the method developed in [24]. The n_{MFB} indicate abnormally high ideality factors ($n_{MFB} >> 2$).

were deposited on the front side of a c-Si wafer, while the back side was coated with aluminum to act as the back surface field and the back contact. The diagram of the solar cell is provided in Fig. 1. The dark and the light *I–V* for five samples were measured using a Keithley 4200 SCS measurement setup.

The dark *I–V* characteristics are first analyzed for parasitic shunt conduction, as follows. From the reverse-bias characteristics (not shown in figure), it is easy to obtain the nonlinear shunt resistance of the solar cell, i.e.,

$$J_{\rm Sh} = G_{\rm Sh}V + J_{\rm 0Sh}V^{\gamma}. \tag{1}$$

The equation (1) captures the ohmic conduction at the low reverse-bias $(G_{\rm Sh}V)$ and the non-linear space charge limited transport at high reverse-bias $(J_{\rm OSh}V^{\gamma})$. The range of γ was found to be $1<\gamma<2$, reflecting the space charge limited transport [23], [24]. The excellent uniformity of the prefactors $(G_{\rm Sh},\,J_{\rm OSh})$ for the measured samples, as summarized in Table I, indicates the process uniformity. The slight difference in the parameters reflects inevitable variations in the fabrication process.

Next, the forward-bias dark I-V is "cleaned" by subtracting the effects of the parasitic shunt current by using the "reflection" method suggested in [24] and [25]; this allows consideration of the intrinsic I-V features uncontaminated by shunt conduction. A typical shunt-corrected forward-bias dark I-V characteristics (of sample A) is shown in Fig. 2(a). The shunt corrected experimental dark I-V was fitted with a phenomenological single diode model

$$J_{\text{Dark}}^{\text{Fit}} = J_0 e^{q(V_{\text{Bias}} - J_{\text{Dark}}^{\text{Fit}} R_{\text{Series}})/nk_B T}, \tag{2}$$

where, J_0 is reverse saturation current, $R_{\rm Series}$ is the series resistance, and n is the ideality factor. We will define $n_{\rm LFB}$, $n_{\rm MFB}$, and $n_{\rm HFB}$ as being the ideality factors at low ($V_{\rm Bias} < V_1^{\rm Dark} \approx 0.1$ to 0.3 V, Region I), medium ($V_{\rm Bias} \approx 0.4$ V), and high forward-bias ($V_{\rm Bias} \approx 0.6$ V), respectively. The parameters obtained from these fits are summarized in Table I. Note that the ideality factors are obtained from the local derivative of the log ($J_{\rm Dark}$)– $V_{\rm Bias}$ curve. However, these ideality factors do not imply an exponential log ($J_{\rm Dark}$)– $V_{\rm Bias}$ relationship; rather, they indicate the degree of complexity of the $J_{\rm Dark}$ – $V_{\rm Bias}$ characteristics in these solar cells.

Under low forward-bias (at $V_{\rm Bias} < V_{\rm I}^{\rm Dark} \approx 0.1$ to 0.3 V), marked as region I in Fig. 2(a), $n_{\rm LFB}$ is below 2 for all of the samples. On increasing the bias $(V_{\rm I}^{\rm Dark} < V_{\rm Bias} < V_{\rm 2}^{\rm Dark} \approx 0.5$ V; region II), $n_{\rm MFB}$ exceeded 3 for all of the samples; this result is consistent with other studies, as reported in Section I. It is difficult to interpret such a high $n_{\rm MFB}$ in terms of classical transport mechanisms associated with p-n or p-i-n junctions, where the ideality factors generally do not exceed 2. Moreover, at the intermediate voltage $(V_{\rm Bias} = V_{\rm 2}^{\rm Dark} \approx 0.5$ V), a knee appears in the dark $I\!-\!V$ characteristics, see Fig. 2(a). Finally, at high forward-bias, the dark current increases exponentially (with $n_{\rm HFB} < 2$), until it is saturated by the $R_{\rm Series}$, see region III of Fig. 2(a).

The nonidealities in the dark *I–V* characteristics, such as the high ideality factors ($n_{\rm MFB} > 2$) above $V_{\rm Bias} = V_1^{\rm Dark}$ and the occurrence of "knee" were also observed by Das et al. [17]. As mentioned in the introduction, these authors classified their cells into three categories (labeled here as: Type-1, Type-2, and Type-3), depending on the shape of the light *I–V* characteristics. The corresponding dark I–V characteristics for each of these types are plotted in Fig. 2(b)–(d). It can be observed that the Type-1 and Type-2 samples also show regions of unusually high ideality factors ($n_{\rm MFB} > 2$) in certain bias ranges. Different from Type-1 (but similar to sample A), the Type-2 sample features a "knee" above which the ideality factor falls below 2. However, these nonidealities are not observed in the Type-3 sample, see Fig. 2(d). In the following subsection, we will use detailed numerical simulations to explore the physical origin of these nonideal effects and explain why they occur in some cells but not in others.

B. Numerical Simulation of the Dark Current

In order to understand the carrier transport and to explain the observed dark I-V behavior, ADEPT 2.0 [26] numerical simulator is used. The simulations are based on the standard material parameters for c-Si and a-Si layer obtained from [20], [27]. The minority carrier surface recombination velocities at the front (s_f) and the back (s_b) are set to 100 cm/s. The effect of the a-Si back surface field that may exist in some of these solar cell designs is thus lumped into the s_b .

In Fig. 3, the dark current $(J_{\rm Dark})$ along with its components, namely, the hole diffusion current (J_P) and the electron diffusion current (J_N) at the front contact, are plotted. The characteristic voltage features of a typical measured dark I–V curve in Fig. 2(a)–(c) are captured by the simulated dark I–V characteristics in Fig. 3. In order to understand the different features, energy band diagrams at different applied biases (regions) are plotted in Fig. 4. The $V_{\rm JN}$ and $V_{\rm JP}$ represent the band bending in the c-Si and the a-Si regions, respectively. The change in the band bending from the equilibrium value between the a-Si and c-Si layer is given by

$$V_m = \left(V_{\rm Jm}^0 - V_{\rm Jm}\right),\tag{3}$$

where, m=P for p-type (and intrinsic) a-Si, m=N for n-type c-Si and $V_{\rm Jm}^0$ is the equilibrium band bending. The band

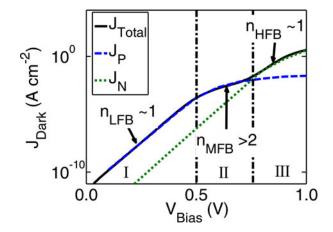


Fig. 3. Numerical dark I–V, $J_{\rm Dark}$, along with the J_N and J_P at the front contact, is plotted for an ideal a-Si/c-Si interface device. The vertical lines separate the different bias regions.

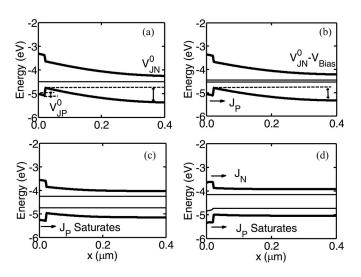


Fig. 4. Schematic of energy band diagram in (a) equilibrium, indicating the band bending in a-Si side $(V_{\rm JP}^0)$ and c-Si side $(V_{\rm JN}^0)$ of the interface, (b) region I $(0 < V_{\rm Bias} < V_{\rm I}^{\rm Dark})$, where J_P is the dominant current component, (c) region II $(V_{\rm I}^{\rm Dark} < V_{\rm Bias} < V_{\rm Z}^{\rm Dark})$, where J_P saturates, and (d) region III $(V_{\rm Bias} > V_{\rm Z}^{\rm Dark})$ J_N becomes dominant.

bending (V_m) across the a-Si and c-Si layers as a function of applied bias is plotted in Fig. 5.

It can be observed from Fig. 5 that nearly the entire voltage drop occurs across the n-type c-Si layer (V_N) for low-voltage bias (region I). This occurs because of the screening effect of an inversion hole charge at the a-Si/c-Si interface. As a result, the energy band in the a-Si region remains pinned with respect to the hole quasi-Fermi level [see Fig. 4(b)]. Hence, the hole concentration at the top of the valence band barrier is essentially voltage independent. Under these conditions, the dominant current transport mechanism is the J_P in the c-Si layer, as observed in Fig. 3.

As the bias voltage increases (region II), the voltage drop continues to increase across the c-Si, until the valence band on the c-Si neutral region aligns with the top of the hole barrier at the interface, as shown in Fig. 4(c). At this bias voltage $(V_{\rm Bias}=V_{\rm I}^{\rm Dark})$, the J_P saturates as it is limited by the hole

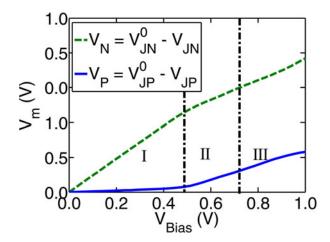


Fig. 5. Change in the band bending V_m across the a-Si and c-Si layers as a function of applied bias. The vertical lines separate the different bias regions.

concentration at the top of the hole barrier at the interface: This saturation is reflected by $n_{\rm MFB}$ exceeding 2 [28]. At even higher bias voltages (region III), the inversion charge, which was present at the interface at lower bias voltages, begins to disappear, causing an almost equal partitioning of the applied voltage across the n-type c-Si and the p-type a-Si layers, as shown in Fig. 5. Under these conditions, the dominant current component is dictated by the relative barrier heights for the electrons and holes. In this particular simulation, it is observed that, the dominant transport mechanism is J_N into the a-Si [see Fig. 3] and $n_{\rm HFB}$ falls below 2. The "knee" in the dark $I\!-\!V$ at $V_{\rm Bias}=V_2^{\rm Dark}$ is a consequence of the change from hole dominated current to electron dominated current. Increasing the bias further introduces bulk series resistance effects.

The change in ideality factor—from $n_{\rm LFB} < 2$ to $n_{\rm MFB} > 2$ and back to $n_{\rm HFB} < 2$ —with increasing applied bias is observed even in an ideal interface heterojunction and is a key signature for carrier transport in these devices. After introducing interface defects, these features are either enhanced or diminished due to changes in the electrostatics and carrier recombination rates dictated by the type of defect states. However, the essential features discussed in this section are still observed. The effects of defect states on the dark I-V will be analyzed later in Section V.

III. PHYSICS OF CARRIER TRANSPORT UNDER ILLUMINATION

Using the dark I-V analysis, one might expect that the light I-V features can be explained by applying the classical superposition principle. However, using a novel simulation approach, we will show that the light I-V components (the contact injection current and the photo-current) have strong generation and voltage dependences. Since, the superposition principle fails under these circumstances, a systematic understanding of individual light I-V features is essential.

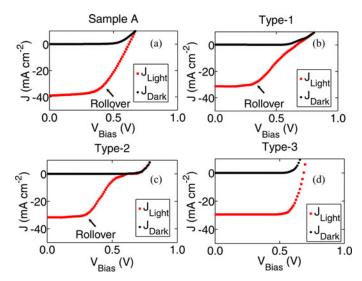


Fig. 6. Light *I–V* characteristics of sample A and those reported in [17] are plotted and labeled here as: Type-1, Type-2 and Type-3. Superposition principle does not hold for *I–V* plotted in (a)–(c). Light *I–V* of Type-1 and 2 indicate rollover in light *I–V* referred to as the S-type curve.

A. Experimental Observations

Fig. 6(a) shows the measured light and the dark I-V characteristics of sample A. It can be observed that the light I-V does not follow the principle of superposition due to rollover of the light I-V close to the maximum power point. Furthermore, in Fig. 6(b), (c), and (d), the dark I-V and the light I-V characteristics obtained from [17] are plotted. In Fig. 6(b) and (c), the light I-V exhibits a strong voltage dependence as Type-1 and Type-2 S-type curves, respectively. The light I-V in Fig. 6(b) and (c) also do not obey the superposition principle due to rollover of the light I-V close to the maximum power point.

However, in Fig. 6(d), the light I-V of Type-3 sample (obtained from [17]) does exhibit adherence to superposition, at least up to $V_{\rm OC}$ and was referred to as a "good fill-factor," FF sample in [17]. Furthermore, there are other studies in the literature that also do not report the occurrence of the S-type curve in the light I-V [15].

Using a novel modeling approach, important insights into carrier transport under light I–V can be realized. This approach allows the injection current to be directly computed for a given illumination condition and is described in the following section.

B. Numerical Simulation of the Light Current

Analyzing the light I–V inherently involves isolating two bias dependent and generation dependent current components of the total current under light (J_{Light}), as follows:

$$J_{\text{Light}}(V,G) = J_{\text{Inj}}(V,G) + J_{\text{Photo}}(V,G) \tag{4}$$

where, $J_{\rm Inj}$ is the contact injection current, and $J_{\rm Photo}$ is the photo-current due to photo-generation. A fundamental problem of analyzing the light I-V of measured devices is that these two components cannot be evaluated accurately using closed-form expressions.

¹Note that it is possible to have hole dominant current in high bias region as well. This depends on the exact a-Si process parameters, such as electron affinity. Suppression of electron current into a-Si region in possible by higher conduction band barrier. Under this scenario hole current from a-Si region is dominant and can exhibit exponential bias dependence.

In order to overcome this challenge, we have developed a novel numerical method to deconvolve $J_{\rm Light}$ into its components $J_{\rm Inj}$ and $J_{\rm Photo}$. The implementation procedure for the numerical method is as follows.

A modification to the ADEPT 2.0 [26] simulation tool was used in this study to separate the $J_{\rm Light}$ into the $J_{\rm Inj}$ and the $J_{\rm Photo}$. This modified drift-diffusion solver uses the following algorithm to determine the $J_{\rm Light}$ and $J_{\rm Inj}$ under illumination for a given generation rate profile (G(x)) and applied bias $(V_{\rm Bias})$.

- 1) The solver calculates the hole density $(p_{\rm Light}(x))$, the electron density $(n_{\rm Light}(x))$, and the potential profile $(\phi(x))$ under illumination using the full drift-diffusion formalism. The $J_{\rm Light}$ can be calculated from the obtained $p_{\rm Light}(x)$ and $n_{\rm Light}(x)$.
- 2) The simulated $\phi(x)$ under illumination was *frozen* and the G(x) is set to zero. The solver once again solves the continuity equations using the frozen $\phi(x)$ obtained from step 1 to calculate a new set of hole density $(p_{\rm Inj}(x))$ and electron density $(n_{\rm Inj}(x))$ profiles. The $J_{\rm Inj}$ was then calculated using the $p_{\rm Inj}(x)$ and $n_{\rm Inj}(x)$.
- 3) The J_{Photo} can be obtained from the J_{Light} and J_{Inj} using (4).

Note that steps 2 and 3 fix the energy band and resolve the carrier density profiles for the contact-injected-carrier components of the total carrier density profiles.

Next, the analysis of these individual components is carried out using test structures to provide insights into the carrier transport under illumination. In order to analyze the $J_{\rm Light}$, in terms of its individual components $J_{\rm Photo}$ and $J_{\rm Inj}$, two a-Si/c-Si heterojunction test structures with different emitter doping ($N_A = 5 \times 10^{17}~{\rm cm}^{-3}$ and $N_A = 5 \times 10^{18}~{\rm cm}^{-3}$) were simulated. It should be noted that the dark and the light I–V features are also affected by other emitter properties such as the valence band offset, a-Si band gap, etc., as discussed in [12] and [16], respectively. However, the essential features of individual components remain the same; hence, only the emitter doping is used as a variable in this analysis. The simulations under illumination are carried out using the AM 1.5 G solar spectrum.

First, the behavior of J_{Photo} is analyzed to study the origin of nonideal features, such as the S-type curve. $J_{\rm Photo}$, along with $J_{\rm Dark}, J_{\rm Inj}$, and $J_{\rm Light}$, are plotted in Figs. 7 and 8 for the lowand heavily doped emitter devices, respectively. It is clear from Fig. 7 that the $J_{\rm Photo}$ for the moderately doped emitter device has a strong bias dependence even below $V_{\rm OC}$ and, thus, the superposition principle does not hold. This significant rollover in $J_{\rm photo}$ at $V_{\rm Bias} \equiv V_{\rm l}^{\rm Light} \sim 0.4$ V, as shown in Fig. 7, can be explained by considering the corresponding energy band diagram at $V_{\rm Bias}=0.4$ V, shown in Fig. 9. It is observed that the valence band offset at the a-Si/c-Si interface acts as a barrier to the collection of photo-generated carriers at the front contact. This observation can be quantified by plotting the positionresolved collection efficiency at different biases, as shown in Fig. 10. This simulation involves counting the number of carriers that are collected at the front contact in response to an impulse of photo-generated carriers at each position along the length of the device. Fig. 10 indicates \sim 40% reduction in the collection efficiency from the c-Si absorber region at $V_{\rm Bias} = 0.4~{
m V}$ when

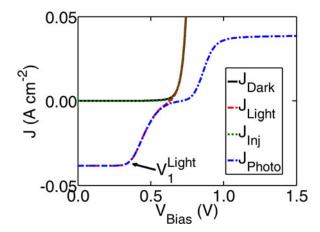


Fig. 7. J_{Dark} , J_{Light} , J_{Inj} , and J_{Photo} are plotted for a moderately doped emitter device ($N_A = 5 \times 10^{17} \ \mathrm{cm}^{-3}$). S-type curve in J_{Light} because of voltage dependence of J_{Photo} . Note that the J_{Dark} , J_{Inj} overlap in the plotted region and that J_{Light} , J_{Photo} overlap up to V_{OC} . The rollover in J_{Photo} starts to occur at $V_{\mathrm{Bias}} = V_1^{\mathrm{Light}}$.

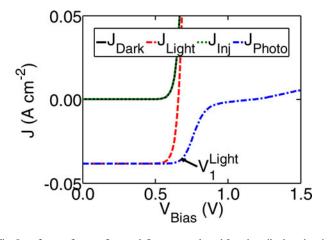


Fig. 8. $J_{\rm D\,ark}$, $J_{\rm Light}$, $J_{\rm Inj}$, and $J_{\rm P\,hoto}$ are plotted for a heavily doped emitter device $(N_A=5\times10^{18}~{\rm cm^{-3}})$. The $J_{\rm P\,hoto}$ is bias independent at least up to $V_{\rm O\,C}$. Note that the $J_{\rm D\,ark}$, $J_{\rm Inj}$ overlap in the plotted region. The rollover in $J_{\rm P\,hoto}$ starts to occur at $V_{\rm B\,ias}=V_1^{\rm Light}$.

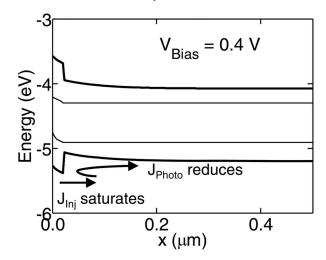


Fig. 9. Energy band diagram for moderately doped emitter device under illumination at $V_{\rm Bias} = 0.4 \text{ V} \sim V_{\rm 1}^{\rm Light}$. At this bias, the valence band offset acts as a barrier for collection of photo generated carriers. In addition, at this bias, loss of the c-Si barrier causes saturation of $J_{\rm Inj}$, which is hole current dominant.

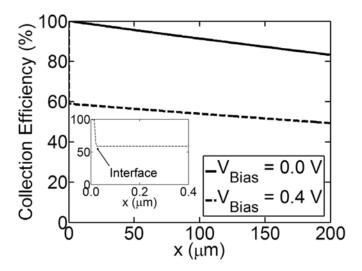


Fig. 10. Position-dependent collection efficiency plot for a moderately doped emitter device under short-circuit condition and at $V_{\rm Bias} = 0.4$ V. This shows a 40% reduction in collection efficiency for carriers generated in Si. The inset shows the reduction of the collection efficiency at the interface because of the a-Si/c-Si valence band offset which acts as a barrier for hole collection.

compared to the short circuit condition. For high forward-bias $(V_{\rm Bias}>0.9~{\rm V},{\rm Fig.~7})$, the reversal of the $J_{\rm Photo}$ polarity is due to a change in the direction of photo-generated carriers above the built-in voltage.

For a heavily-doped emitter device, however, Fig. 8 indicates the $J_{\rm Photo}$ starts to rollover well above $V_{\rm OC}$, at $V_{\rm Bias} = V_{\rm I}^{\rm Light} \sim 0.7$ V, indicating that superposition can be safely assumed for this device. Here, the magnitude of $J_{\rm Inj}$, which is equal to $J_{\rm Dark}$, dictates the shape of the $I\!-\!V$ characteristic up to $V_{\rm OC}$. The suppressed $J_{\rm Photo}$ at very high forward-bias indicates a very high built-in voltage for this device.

IV. CORRELATION OF DARK AND LIGHT I-V

A. Analysis of Simulation Results

The preceding discussion suggests a possible correlation between the dark I–V and the light I–V because both are controlled by the a-Si/c-Si potential barrier. In order to establish this correlation quantitatively, the behavior of $J_{\rm Inj}$ must be analyzed. $J_{\rm Inj}$, which is essentially the "effective dark current under illumination," will have the same features as those of the $J_{\rm Dark}$. Thus, the insights developed in Section II on the features of the dark I–V characteristics will be useful in analyzing the features of $J_{\rm Inj}$. Next, it will be shown that $J_{\rm Inj}$, which is obtained from light I–V simulations, can be correlated to the $J_{\rm Photo}$ discussed in Section III. This correlation provides insights into the operation of these solar cells.

We will use the same test structures discussed in Section III to analyze the essential features of $J_{\rm Dark}$ and $J_{\rm Inj}$. $J_{\rm Inj}$ and $J_{\rm Dark}$, for both moderately and heavily doped emitter structures, are plotted on a semilog plot in Figs. 11 and 12, respectively. Observe that both $J_{\rm Dark}$ and $J_{\rm Inj}$ have the same essential features discussed in Section II; indeed, $V_1^{\rm Light}$ and $V_2^{\rm Light}$ of $J_{\rm Inj}$ can be viewed as counterparts of $V_1^{\rm Dark}$ and $V_2^{\rm Dark}$ observed in $J_{\rm Dark}$. In addition, note that the $V_1^{\rm Light}$, which represented the rollover

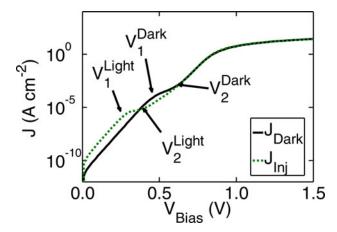


Fig. 11. J_{Dark} and J_{Inj} are plotted for a low-doped emitter device. The shift in V_{1}^{Light} from V_{1}^{Dark} indicate significant change in the c-Si band bending because of photo-generated carriers that results in the early saturation of low bias dominant hole current from the front contact.

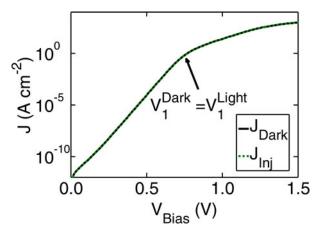


Fig. 12. $J_{\mathrm{D\,ar\,k}}$ and $J_{\mathrm{In\,j}}$ are plotted for a high-doped emitter device (overlap throughout the plotted bias range). There is no shift between $V_{\mathrm{I}}^{\mathrm{L\,ig}\,\mathrm{ht}}$ and $V_{\mathrm{I}}^{\mathrm{D\,ar\,k}}$, indicating a negligible impact of c-Si band bending due to photo-generated carriers.

of $J_{\rm Photo}$ [see Figs. 7 and 8], is the same as the one used here in Figs. 11 and 12. The justification for this will be provided once $J_{\rm Dark}$ and $J_{\rm Inj}$ are correlated.

For the moderately-doped emitter device, the $V_1^{\rm Light}$ occurs at a lower bias voltage compared with that of $V_1^{\rm Dark}$. As discussed in Section II (for $J_{\rm Dark}$), the saturation in $J_{\rm Inj}$ occurs when the valence band in the c-Si neutral region aligns with the top of the a-Si hole barrier as pointed out in Fig. 9. There is a considerable change in electrostatic potential profile under the illumination when compared with the dark, due to the presence of photogenerated carriers. This causes the early saturation of $J_{\rm Inj}$ when compared with $J_{\rm Dark}$. However, this shift in $V_1^{\rm Dark}$ and $V_1^{\rm Light}$ is not observed in the heavily doped emitter device, indicating a negligible change in the potential profile under illumination when compared to the dark conditions. It is important to note that the photo-generated carriers in the device with low $V_1^{\rm Dark}$ have a larger impact on the electrostatics of the device, thus causing a greater shift in $V_1^{\rm Light}$.

The correlation between $J_{\rm Photo}$ and $J_{\rm Inj}$ is based on an important observation that the valence band at the top of the a-Si barrier aligns with that of the neutral c-Si region at $V_{\rm Bias} = V_{\rm 1}^{\rm Light}$. At this bias, both the saturation of $J_{\rm Inj}$ and the rollover of $J_{\rm Photo}$ occur [see Fig. 9 for a low emitter case]. It can be observed for the moderately-doped emitter device in Figs. 7 and 11 that the rollover of $J_{\rm Photo}$ and saturation of $J_{\rm Inj}$ occur at the same voltage bias. Furthermore, this is also true for the heavily doped emitter device, as shown in Figs. 8 and 12.

B. Analysis of Experimental Results

Several distinctive features of the dark I-V and the light I-V, such as, the occurrence of high $n_{\rm MFB}$ above $V_1^{\rm Dark}$, the occurrence of knee under dark conditions, the failure of superposition, and the occurrence of S-type light I-V curve are explained using the numerical simulation framework in Sections II and III. Here, the dark I-V and the light I-V data measured during this study as well as those obtained from [17] are analyzed based on the theory developed in the preceding sections. It should be noted that, there may be significant processing differences among the samples considered. Despite these differences, it is possible to understand the general features of the experimental results based on the theoretical model discussed in the previous section.

Fig. 2(a) shows that the low forward-bias part of the dark I-V characteristics of sample A changes continuously over the bias voltage, which could be due to the presence of interface defect states (discussed in Section V). Hence, it is not possible to accurately estimate the $V_1^{\rm Dark}$. However, the $V_2^{\rm Dark}$ can be estimated from the local maxima in the $d^2\log(J)/dV^2$ versus $V_{\rm Bias}$ plot and was found to be around $V_2^{\rm Dark} \sim 0.48$ V.

From the light $I\!-\!V$ characteristics of sample A [see Fig. 6a], it can be observed that the light $I\!-\!V$ has a weak bias dependence at very low biases ($V_{\rm Bias} \sim 0.1$ V). However, a strong rollover starts to occur above $V_{\rm Bias} \sim 0.3$ V, which suggests that the $V_1^{\rm Light}$ may be around the same voltage range based on the discussion in the earlier subsection which correlated the $J_{\rm Photo}$ and $J_{\rm Inj}$.

From the dark I–V reported in [17], it can be observed that Type-1 [see Fig. 2(b)] and Type-2 [see Fig. 2(c)] samples exhibit a distinctive $V_1^{\rm Dark}$, followed by a region with a very high ideality factor ($n_{\rm MFB} > 2$) that can be attributed to J_P saturation. Furthermore, the Type-2 sample also exhibits a knee above which the ideality factor eventually returns to a value less than 2. This can be attributed to the change in the type of dominant minority carrier current (J_P to J_N), as expected from the analysis of dark I–V characteristics in Section III. This knee is not observed in Type-1 and Type-3 [see Fig. 2(d)], presumably because of the high-quality emitter and front contact properties that suppress J_N .

The light $I\!-\!V$ characteristic of the Type-1 sample [see Fig. 6(b)] exhibits a rollover at relatively low bias and a strong S-type behavior $(V_1^{\rm Light})$ which is correlated to the low $V_1^{\rm Dark}$ observed in the dark $I\!-\!V$ [see Fig. 2(b)] for this sample. The Type-2 sample, which has $V_1^{\rm Dark}$ in the medium bias range in the dark $I\!-\!V$ [see Fig. 2(c)], also has a light $I\!-\!V$ rollover [see Fig. 6(c)] at around the same voltage range $(V_1^{\rm Light})$. Finally, the

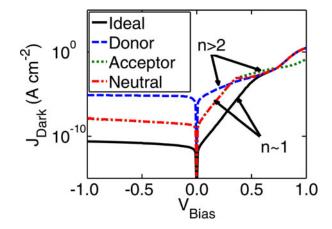


Fig. 13. Numerical dark I–V for an ideal structure along with nonideal structure with defective a-Si/c-Si interface containing donor, acceptor, and neutral traps with $D_{\rm IT}=10^{12}~{\rm cm}^{-2}$ (Gaussian energy distribution around the mid-gap with $\sigma=0.3~{\rm eV}$).

Type-3 sample, which has a near ideal dark I–V [see Fig. 2(d)] with no $V_1^{\rm Dark}$ within the plotted range, exhibits no rollover (no $V_1^{\rm Light}$ observed) of light I–V [see Fig. 6(d)] as well. Observably, the FF is very high for this case.

Now, it is also possible to correlate some of the other sets of measurements present in the literature, such as, those reported in [15]. These samples indicate no sign of nonideal features in the dark I-V and the light I-V, most likely because of excellent process control, closely resembling the device with higher emitter doping discussed in Section III.

V. DISCUSSION

At very low forward-bias, apart from the multi-tunneling capture emission phenomena [5], the dark I–V can be effected by the presence of interface defects. When defects are present in the a-Si/c-Si interface, there are two reasons for deviation of the dark I–V, namely, carrier recombination at the interface and change in electrostatics because of trapped charges. These two components can be studied separately using numerical simulation by first considering neutral traps ($D_{\rm IT}=10^{12}~{\rm cm}^{-2}$) to see the effect of recombination current ($J_{\rm Rec}$) and, second, using donor/acceptor like traps ($D_{\rm IT}=10^{12}~{\rm cm}^{-2}$) to capture the effects of change in electrostatics. The traps considered in this paper have a Gaussian energy distribution around the mid-gap with $\sigma=0.3~{\rm eV}$.

Upon introducing neutral defects, the reverse-bias and low forward-bias currents increase due to additional $J_{\rm Rec}$ [see Fig. 13]. The ideality factor, however, remains below 2 for the low forward-bias region and the high forward-bias region. In the medium bias range, the saturation of J_P causes the ideality factor to increase beyond 2, as observed in an idealized defect-free device discussed in Section II.

Donor traps at the a-Si/c-Si interface cause high currents in the reverse-bias and low forward-bias regions due to high $J_{\rm Rec}$. It should be noted that the ideality factors in low forward-bias in this case are *now considerably higher than* 2. This high ideality factor can be understood from the energy band diagram in

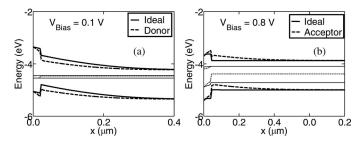


Fig. 14. Energy band diagram near the junction of an ideal structure along with a nonideal structure with (a) donor-like traps at a-Si/c-Si interface at $V_{\rm Bias}=0.1$ V. (b) Acceptor-like traps at a-Si/c-Si interface at $V_{\rm Bias}=0.8$ V.

Fig. 14(a). At low forward-bias ($V_{\rm Bias} \sim 0.1~\rm V$), on capturing the holes from the "inversion region" at the interface, the positively charged donor states push the band downward. However, the hole carrier concentration at the top of the barrier on the a-Si side remains the same (notice the hole quasi-Fermi level shifts along with the a-Si bands). This causes the early saturation of J_P , as explained in Section II. Hence, the twofold effect of charged defects, namely, increased low-bias dark current and high ideality factor, is due to high $J_{\rm Rec}$ and the change in c-Si barrier height in the presence of positively charged donor traps. Under high forward-bias ($V_{\rm Bias} > V_2^{\rm Dark}$), the detrapping of donor traps causes them to behave like neutral traps, and the dominant J_N makes the impact of $J_{\rm Rec}$ negligible.

On the other hand, acceptor-like traps are neutral in the reverse-bias and low forward-bias region $(V_{\rm Bias} < V_1^{\rm Dark})$, as there are few electrons to capture at the interface. The low bias ideality factor is less than 2 before it increases due to the saturation of J_P . However, at high forward-bias $(V_{\rm Bias} > V_2^{\rm Dark})$, the ideality factor is above 2, and the current deviates significantly from the ideal case. This can be understood from the energy band diagram at high forward-bias, shown in Fig. 14(b). At high forward-bias, the filled acceptor traps (which are negatively charged) push the bands upward. This causes an additional barrier to electrons from the c-Si to reach the a-Si layer, and thus, the J_N into the a-Si side is suppressed. Hence, at high-forward bias, the $J_{\rm Rec}$ and the saturated J_P continue to dominate over the J_N .

VI. CONCLUSION

The nonideal effects of the dark $I\!-\!V$ and the light $I\!-\!V$ characteristics of (P+/I/n) a-Si/c-Si heterojunction solar cell are discussed. In the dark $I\!-\!V$, the unusually high ideality factors in the medium-bias regions, even in an otherwise ideal interface heterostructure, is attributed to J_P saturation. The $V_2^{\rm Dark}$ is observed when the dominant current transport shifts from J_P to J_N . High densities of defects at the a-Si/c-Si interface can introduce additional current because of interface recombination and shift the position of $V_1^{\rm Dark}$ and $V_2^{\rm Dark}$ by affecting the electrostatics.

A novel simulation method using a detailed numerical model to separate $J_{\rm Light}$ into its component parts $J_{\rm Inj}$ and $J_{\rm Photo}$ has been developed. The rollover in $J_{\rm Photo}$ in the moderately doped emitter devices is due to the presence of a hole barrier at the

a-Si/Si interface. It is shown that $J_{\rm Dark}, J_{\rm Inj}$, and $J_{\rm Photo}$ are correlated in a fundamental way. The consequence of this correlation is that a device with a higher $V_1^{\rm Dark}$ has no shift in $V_1^{\rm Light}$ and has a voltage-independent $J_{\rm Photo}$ up to $V_1^{\rm Light}$. This avoids the rollover of the light $I\!-\!V$ before $V_{\rm OC}$ and yields in a better FF.

Finally, based on the interpretation of the experimental results, it is shown that the dark I-V and the light I-V nonidealities indeed follow the theory presented in this paper. This correlation offers a fundamental insight regarding the importance of the heterojunction interface in designing highly efficient HITTM cells.

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REFERENCES

- [1] M. Tanaka, M. Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, and Y. Kuwano, "Development of new a-Si/c-Si heterojunction solar cells: ACJ-HIT (artificially constructed junction-heterojunction with intrinsic thin-layer)," *Jpn. J. Appl. Phys.*, vol. 31, no. 11, pp. 3518– 3522, Nov. 1992.
- [2] K. Maki, D. Fujishima, H. Inoue, Y. Tsunomura, T. Asaumi, S. Taira, T. Kinoshita, M. Taguchi, H. Sakata, H. Kanno, and E. Maruyama, "Highefficiency HIT solar cells with a very thin structure enabling a high voc," in *Proc. 37th IEEE Photovoltaic Spec. Conf.*, 2011, pp. 57–61.
- [3] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, "24.7% record efficiency HIT solar cell on thin-silicon wafer," *IEEE J. Photovoltaics*, vol. 4, no. 1, pp. 1–4, Jan. 2014.
- [4] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (version 40)," *Prog. Photovoltaics Res. Appl.*, vol. 20, no. 5, pp. 606–614, 2012.
- [5] H. Matsuura, T. Okuno, H. Okushi, and K. Tanaka, "Electrical properties of n-amorphous/p-crystalline silicon heterojunctions," *J. Appl. Phys.*, vol. 55, no. 4, pp. 1012–1019, Feb. 1984.
- [6] L. F. Marsal, J. Pallarés, X. Correig, J. Calderer, and R. Alcubilla, "Electrical characterization of n-amorphous/p-crystalline silicon heterojunctions," J. Appl. Phys., vol. 79, no. 11, p. 8493, 1996.
- [7] N. Jensen, U. Rau, R. M. Hausner, S. Uppal, L. Oberbeck, R. B. Bergmann, and J. H. Werner, "Recombination mechanisms in amorphous silicon/crystalline silicon heterojunction solar cells," *J. Appl. Phys.*, vol. 87, no. 5, pp. 2639–2645, Mar. 2000.
- [8] M. Taguchi, E. Maruyama, and M. Tanaka, "Temperature dependence of amorphous/crystalline silicon heterojunction solar cells," *Jpn. J. Appl. Phys.*, vol. 47, no. 2, pp. 814–818, Feb. 2008.
- [9] B. Jagannathan, W. A. Anderson, and J. Coleman, "Amorphous silicon/ptype crystalline silicon heterojunction solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 46, no. 4, pp. 289–310, Jul. 1997.
- [10] T. H. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, H. M. Branz, and Q. Wang, "Effect of emitter deposition temperature on surface passivation in hot-wire chemical vapor deposited silicon heterojunction solar cells," *Thin Solid Films*, vol. 501, no. 1–2, pp. 284–287, Apr. 2006.
- [11] Y. J. Song, M. R. Park, E. Guliants, and W. A. Anderson, "Influence of defects and band offsets on carrier transport mechanisms in amorphous silicon/crystalline silicon heterojunction solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 64, no. 3, pp. 225–240, Oct. 2000.
- [12] R. V. K. Chavali, J. R. Wilcox, B. Ray, J. L. Gray, and M. A. Alam, "A diagnostic tool for analyzing the current-voltage characteristics in a-Si / c-Si heterojunction solar cells," in *Proc. 39th IEEE Photovoltaic Spec. Conf.*, 2013, vol. 1, pp. 652–657.
- [13] U. Das, S. Bowden, M. Burrows, S. Hegedus, and R. Birkmire, "Effect of process parameter variation in deposited emitter and buffer layers on

- the performance of silicon heterojunction solar cells," in *Proc. IEEE 4th World Conf. Photovoltaic Energy Convers.*, 2006, vol. 2, pp. 1283–1286.
- [14] T. F. Schulze, L. Korte, E. Conrad, M. Schmidt, and B. Rech, "High-forward-bias transport mechanism in a-Si:H/c-Si heterojunction solar cells," *Phys. Status Solidi*, vol. 207, no. 3, pp. 657–660, 2010.
- [15] T. F. Schulze, L. Korte, E. Conrad, M. Schmidt, and B. Rech, "Electrical transport mechanisms in a-Si:H/c-Si heterojunction solar cells," *J. Appl. Phys.*, vol. 107, no. 2, p. 023711, 2010.
- [16] M. Lu, U. Das, S. Bowden, S. Hegedus, and R. Birkmire, "Optimization of interdigitated back contact silicon heterojunction solar cells: Tailoring hetero-interface band structures while maintaining surface passivation," *Prog. Photovoltaics Res. Appl.*, vol. 19, no. 3, pp. 326–338, May 2011.
- [17] U. Das, S. Hegedus, L. Zhang, J. Appel, J. Rand, and R. Birkmire, "Investigation of hetero-interface and junction properties in silicon heterojunction solar cells," in *Proc. 35th IEEE Photovoltaic Spec. Conf.*, 2010, pp. 1358–1362.
- [18] Q. Wang, "High-efficiency hydrogenated amorphous/crystalline Si heterojunction solar cells," *Philos. Mag.*, vol. 89, no. 28–30, pp. 2587–2598, Oct. 2009.
- [19] Z. Shu, U. Das, J. Allen, R. Birkmire, and S. Hegedus, "Experimental and simulated analysis of front versus all-back-contact silicon heterojunction solar cells: Effect of interface and doped a-Si:H layer defects," *Prog. Photovoltaics Res. Appl.*, Jun. 2013.
- [20] A. Kanevce and W. K. Metzger, "The role of amorphous silicon and tunneling in heterojunction with intrinsic thin layer (HIT) solar cells," *J. Appl. Phys.*, vol. 105, no. 9, p. 094507, 2009.
- [21] K. Ghosh, S. Bowden, and C. Tracy, "Role of hot carriers in the interfacial transport in amorphous silicon/crystalline silicon heterostructure solar cells," *Phys. Status Solidi*, vol. 210, no. 2, pp. 413–419, 2013.
- [22] U. K. Das, M. Z. Burrows, M. Lu, S. Bowden, and R. W. Birkmire, "Surface passivation and heterojunction cells on Si (100) and (111) wafers using dc and rf plasma deposited Si:H thin films," *Appl. Phys. Lett.*, vol. 92, no. 6, p. 063504, 2008.
- [23] S. Dongaonkar, J. D. Servaites, G. M. Ford, S. Loser, J. Moore, R. M. Gelfand, H. Mohseni, H. W. Hillhouse, R. Agrawal, M. A. Ratner, T. J. Marks, M. S. Lundstrom, and M. A. Alam, "Universality of nonohmic shunt leakage in thin-film solar cells," *J. Appl. Phys.*, vol. 108, no. 12, p. 124509, 2010.
- [24] S. Dongaonkar, K. Y, D. Wang, M. Frei, S. Mahapatra, and M. A. Alam, "On the nature of shunt leakage in amorphous silicon p-i-n solar cells," *IEEE Electron. Device Lett.*, vol. 31, no. 11, pp. 1266–1268, Nov. 2010.
- [25] S. Dongaonkar and M. A. Alam, (2011, Mar.). PV Analyzer. [Online]. Available: https://nanohub.org/resources/11073
- [26] J. L. Gray, X. Wang, X. Sun, and J. R. Wilcox, (2011, Mar.). ADEPT 2.0. [Online]. Available: http://nanohub.org/resources/10913
- [27] (2012). Material Data-Silicon Materials. [Online]. Available: http://www.ampsmodeling.org/materialData_silicon.html
- [28] R. L. Anderson, "Experiments on Ge–GaAs heterojunctions," Solid State Electron., vol. 5, no. 5, pp. 341–351, Sep. 1962.



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