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Impedance spectroscopy of crystalline silicon solar cell: Observation of negative capacitance

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ABSTRACT

The knowledge of ac parameters of solar cells/arrays is important for designing of high performance power conditioning circuits to match the input at operating conditions. A systematic study of crystalline silicon solar cells is done using impedance spectroscopy under forward bias conditions and at different illumination levels. A "*negative capacitance*" behaviour is observed in the low frequency region under forward bias voltages and at low illumination levels. An electrical equivalent circuit with inductive component is used to fit the experimental data and the pseudo-capacitance behaviour is explained on the basis of an equivalent circuit model.

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1. Introduction

The load which is connected to the solar panel array in a solar photovoltaic power generating system, draws continuous power from it. The solar panel array and the battery are interfaced through a charge controller which switches between on and off states. The switching ripple of the charge controller contributes to the power loss which depends on the solar array capacitance (Kim et al., 2013; Kumar et al., 2006). Solar cell is a dc device, which exhibits complex impedance and is affected by ambient condition. Therefore, the knowledge of ac parameters of a solar cell, their variation with respect to illumination and bias is important as these parameters change with the duration of the day and ambient temperature. The requirement of high power necessitates the design of high performance power conditioning circuits to match with the input at the operating condition as a mismatch in impedances may lead to poor output. Therefore, knowledge of solar cell impedance is essential to develop an efficient system.

Impedance spectroscopy (IS) is an important technique which is, generally, used for characterisation of solid-electrolyte systems. With this technique, dynamic behaviour of a device with a small amplitude ac signal superimposed on a suitable dc voltage, can be studied. The response of the system to the sinusoidal perturbation is used to calculate the impedance (Z, a complex number) as a function of frequency (f). Thus, different processes in the system manifest themselves on different time scales. From the number and dimensions of the semicircles observed in the complex plane as Z'-Z'' plot, one can visualise the nature of physical phenomena occurring in the device. In the case of solar cells, IS is generally used for the study of surface transport, diffusion and recombination processes within the bulk and at the interface (Garland et al., 2011a,b; Kumar, 2001; Kumar et al., 2009, 2010; Nagaraju et al., 2005; Garcia-Belmonte et al., 2006). Normally, IS spectrum (Nyquist plot) consists of a number of semicircles depending on materials/layers and interfaces. Each semicircle is associated with a combination (series or parallel) of Voigt elements; where a single Voigt element is a parallel combination of a resistor (R) and capacitor (C) or an inductor (L). The impedance data can then be fitted into a circuit consisting a number of Voigt elements combination which can be used further to describe the physical processes.

It is known that a semiconductor device with a single p-n junction has two types of capacitances, namely the chemical (C_μ) and depletion (C_{dl}) capacitances (Kumar et al., 2009; Mora-Sero et al., 2009). The former, often termed as diffusion capacitance (C_d) which indicates the accumulation of minority carriers, is used to study the dynamic behaviour of photovoltaic devices (Bisquert, 2003; Mora-Seró et al., 2006; Mora-Sero et al., 2009). In addition, "*negative capacitance*" has also been observed in various types of

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solar cells (Mora-Seró et al., 2006), heterostructures (Perný et al., 2014), organic semiconductor devices (Ehrenfreund et al., 2007; Lungenschmied et al., 2009) and metal-semiconductor interfaces (Wu et al., 1990).

In this paper, the ac behaviour of crystalline silicon (c-Si) solar cells fabricated in an industrial environment is studied using impedance spectroscopy. The n^+-p-p^+ structure based cells have a p-n junction (n^+-p) and Al back surface field (BSF, with p-p^+ structure) at the rear side along with an antireflection layer on the front besides front and back metal contacts. Impedance spectra are measured at forward bias (V_b) condition (in dark) and at different illumination (P_{in}) levels (at zero electrical bias). The noticeable observation is the "*negative capacitance*" in the impedance data in low frequency regime. To explain this, separate passive element having inductive nature is added to the conventional equivalent circuit having Voigt elements consisting of resistance and capacitance (in parallel). The origin of low frequency inductance behaviour is discussed in terms of "*negative capacitance*".

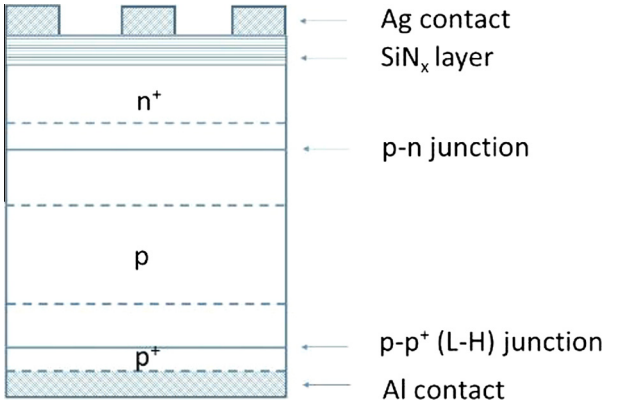

Fig. 1. Schematic of the silicon solar cell having n^+-p-p^+ structure. The cells have screen printed Ag front contact, an antireflection coating of silicon nitride and Al back surface field and back contact.

2. Experimental

The cells are fabricated on $125 \times 125\ mm^2$ pseudo square wafers obtained from single crystalline p-type Cz Si ingot. Prior to device fabrication, the wafers are textured using aqueous alkaline solution using the protocol described elsewhere (Singh et al., 2001). The textured wafers are subjected to phosphorus diffusion to make n^+ emitter and after phosphorous-silicate glass (PSG) removal, the diffused wafers are subjected to Si_xN_y layer deposition on the front as an anti-reflection coating using PECVD. Front metal grid is screen printed using Ag paste and on the back a layer of Al is applied; which on subsequent firing step forms the back surface field (BSF) in the form of p-p^+ junction. Finally two Al–Ag busbars are screen printed on the rear for electrical contact for current extraction. The finished cells ($125 \times 125\ mm^2$) are diced into smaller pieces ($20 \times 20\ mm^2$) from the backside using a laser scriber (M/s ARGUS YAG, China). These cells are used in the present study and the cell structure schematic is shown in Fig. 1. Due care is taken during dicing to avoid deleterious effect of shunting and associated "edge effect". For this the laser power is adjusted to scribe half of cell thickness and the laser marked pieces are separated manually. Impedance spectroscopy measurements are performed using a potentiostat (Model: Reference 600, M/s Gamry). The working electrode cable of the potentiostat terminal is connected to the rear metal contact. The counter and reference electrode are connected to the front metal contact of solar cell using shielded BNC cables. The length of the cables is taken as short as possible to minimize inductive component associated with wires and external noise. The excitation voltage is kept at 10 mV which is less than the thermal voltage (kT/q ~ 25 mV at 25 °C) to maintain the linearity of the response. The real and imaginary components of the impedance (Z' and Z'') are measured in 1 MHz to 1 Hz frequency range. The current density-voltage (*J-V*) characteristics (using a system from M/s Newport Corporation, USA, Model: J80036) of the $125 \times 125\ mm^2$ and the diced cells ($20 \times 20\ mm^2$) are measured using a Class AAA solar simulator (Model: Oriel Sol 3A, M/s *Oriel* Instruments, USA) under standard test conditions (STC; AM1.5G solar spectrum, 25 °C, 100 mW/cm^2 power). The solar simulator is equipped with 1600 W Xe lamp and AM 1.5G filter. IS measurements are carried out (under dark) at different dc bias voltages varying between zero to the open circuit voltage (V_{oc}), the value of which is pre-determined by *J-V* characteristics. The effect of illumination is studied at zero bias voltage where illumination level (P_{in}) is varied from 0.05 to 0.6 suns by adjusting the distance between the light source and the device. The illumination level is determined using Suns-V_{oc} system (M/s Sinton Instruments, USA; equipped with a 60 W Xe flash lamp) that has a provision to generate open circuit voltage (V_{oc}) at different illumination levels ranging from 0.06 to 6 suns. Subsequently the *J-V* characteristics are measured in the linear sweep voltammetry (LSV) analysis mode. The value of V_{oc} so determined is used to identify illumination levels (P_{in}). It is to be noted here that all the IS measurements are carried out on the diced $20 \times 20\ mm^2$ solar cells but *J-V* (and *I-V*) characteristics (shown in Fig. 2) are measured on both large (full cells) and diced small cells. During all the measurements the cell temperature is maintained at 25 °C.

3. Results & discussion

In silicon solar cells, the space charge region of n^+-p junction is the sum of depletion region widths on emitter and base sides and the built-in potential (V_{bi}) across junction is equal to $(kT/q)\ln(N_aN_d/n_i^2)$ where N_a and N_d are acceptor and donor concentrations and n_i is the intrinsic carrier concentration. Similarly at back surface field region a junction (p-p^+) is formed as the holes from p^+ side diffuse into the p-region and sets up a built-in voltage (V_{p0}). Under positive bias, both the junctions are forward biased due to the same polarity.

Fig. 2 shows the *J-V* characteristics of a representative $125 \times 125\ mm^2$ (non-diced) solar cell prior to the dicing and that of diced $20 \times 20\ mm^2$ pieces measured using solar simulator under standard test conditions. The open circuit voltage (V_{oc}) and the short circuit current density (J_{sc}) are 0.628 ± 0.002 V and 37.0 ± 0.2 mA/cm^2 respectively in both large and small cells. The inset of the figure gives *I-V* characteristics of the two cells ($125 \times 125\ mm^2$ and $20 \times 20\ mm^2$) which has same V_{oc} but different I_{sc}. The difference in two I_{sc} values are in the same ratio as that of the area of the two cells within measurement uncertainties. The same value of J_{sc} in the larger and the smaller cells clearly show that the dicing step has not introduced "edge-effects" which otherwise arises due to shunting. The knee voltage which is the voltage at the maximum power point, occurs at 0.46 V and cell efficiency (η) is $14.8 \pm 0.02\%$. The J_{sc} value is used to generate V_{oc} vs P_{in} curve using Suns-V_{oc} system and the result is shown in Fig. 3. In Suns-V_{oc} mode, the cells are illuminated by a short light pulse from a flash-lamp and decay of both, the illumination and open-circuit voltage, are recorded. The decay time of the illumination is such that V_{oc} remains in quasi-steady state (QSS) with P_{in}. Therefore, this method is also referred as QSS-V_{oc} (Sinton and Cuevas, 2000). Fig. 3 is then used to define P_{in} for recording impedance spectra under varying illuminations. Also from the Suns-V_{oc} curve, a pseudo *J-V* curve can be constructed (as shown in Fig. 4) which is

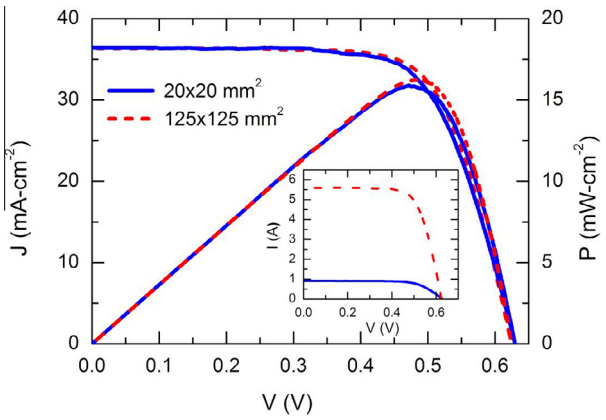

Fig. 2. Experimental current density-voltage (*J-V*) and power density-voltage (P-V) characteristics of large (125 × 125 mm^2) and diced (20 × 20 mm^2) solar cells under AM1.5G spectrum irradiation (1 sun) at 25 °C. The inset shows current-voltage (*I-V*) characteristics of both the cells under the same condition.

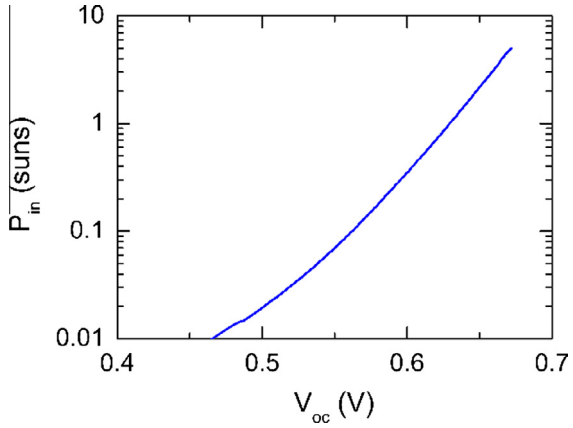

Fig. 3. Open circuit voltage (V_{oc}) vs illumination level (P_{in}) of a representative 20 × 20 mm^2 cell measured by the Suns-V_{oc} tester.

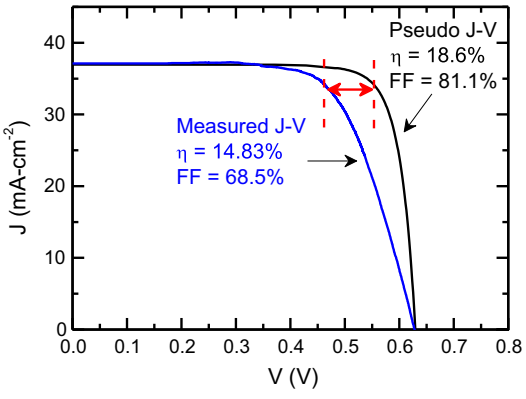

Fig. 4. One-sun pseudo *J-V* curve (continuous line) implied from the Suns-V_{oc} data along with the measured *J-V* characteristics of 20 × 20 mm^2 cell under standard test conditions (STC; AM1.5G solar spectrum, 100 mW cm^{-2} illumination, 25 °C). The dashed vertical lines show the knee voltages (maximum power point voltages) of the two curves. The double sided arrow shows the contribution of series resistance. The corresponding efficiency (η) and fill factor (FF) values are also given.

compared with the *J-V* curve measured under solar simulator (shown in Fig. 2). In the former, the contribution of series resistance is ignored and thus provides the upper bound for the device efficiency. From the difference of voltage values at the knee voltages (or the maximum power point voltage, V_{mp}) of the two curves, the effect of series resistance can be visualized, which plays a vital role in deciding the fill factor. The difference of values between the pseudo-FF and FF can be used to find the series resistance of the actual cell according to the formula (Pysch et al., 2007; Feldman et al., 2013); $R_{S,Suns\text{-}Voc} = (PFF - FF)V_{oc}J_{sc}/J_{mp}^2$ and is found to be 2.45 Ω cm^2.

Fig. 5 shows the *J-V* characteristics at different illumination levels measured using the LSV mode whereas Fig. 6 shows the impedance data of the cell in the complex plane, with varying bias voltage from 0.1 V to 0.6 V under dark (without illumination). The maximum value of the bias is kept close to V_{oc} which has been predetermined from *I-V* characteristics under 1 sun illumination. The displacement of the curves along the Z' axis provides the series resistance of the device. The negative values on Z''-axis in the high frequency side is generally attributed to the parasitic inductances associated with connecting wires. It can be seen from the figure that the radii of the semicircles decrease with increase in forward bias voltage (V_b) and after a certain bias ($V_b > 0.3$ V), the nature of the curve deviates from semi-circular shape particularly at high frequency (f) end. This can be attributed to the lower energy barrier resulted by the increasing V_b. In this condition, the current easily flows across the junction and consequently, the total impedance is lowered. The deviation in the original shape of the measured impedance spectra becomes more and more prominent with the increase in bias voltage. Generally the shape of the spectra deviates from the semi-circular nature due to the superposition of two or more semicircles. Therefore, different ac response is seen in low and high frequency regions. In the low frequency region the device behaves more like an n$^+$-p junction. At higher frequencies the response may be associated with the formation of second loop. This is, generally, assigned to the low-high junction created during BSF formation (Crain et al., 2012; Garland et al., 2011a,b) which can be accounted by additional RC circuits. For very large forward bias voltages ($V_b \simeq V_{oc}$), this loop is suppressed by the high frequency inductive tail. Further in the low frequency region, a separate loop in the lower (i.e., 4th) quadrant is observed and a significant number of data points lie in this region which cannot be ignored as a simple noise. This is, generally defined as "*negative capacitance*" or pseudo-capacitance in the literature (Ershov et al., 1998; Mora-Seró et al., 2006).

The "*negative capacitance*" behaviour can be seen with more clarity in the voltage dependence of C' (i.e., the real component of complex capacitance C) vs. f from Fig. 7 where the measured values are plotted for different electrical biases. From these curves following observations can be made; (i) the capacitance is positive showing a plateau in high to mid frequency (10^2–10^5 Hz) range; (ii) the capacitance becomes negative at low frequencies when the transition in capacitance (which is seen as a dip) occurs from positive to negative quadrant and the transition frequency (f_t^l) shifts with increasing bias voltage; and (iii) another transition from positive to negative sign at higher frequency side (f_t^h). The behaviour in the vicinity of f_t^h can be attributed to the external connecting wires, stray currents, noise etc (and generally shielded short wire mitigates these effects).

The conventional equivalent circuit used for silicon solar cells (n$^+$-p-p$^+$ structure) with resistance (R_x) and capacitance (C_x) (where x = LH and j corresponds to low-high junction and p-n junction respectively; Garland et al., 2011a) is shown in Fig. 8a. To explain the observed "*negative capacitance*" behaviour at f_t^l, a parallel combination of R_L and L is added to Fig. 8a as shown in Fig. 8b. The silicon solar cell used in the present study have two junctions, i.e., n$^+$-p and p-p$^+$. Generally, the magnitudes of R and C at the former junction is larger compared to the later (Garland et al., 2011a, b). In the present case, the values of R_x are two orders of magnitude different at the two junctions and corresponding C_x is of one order

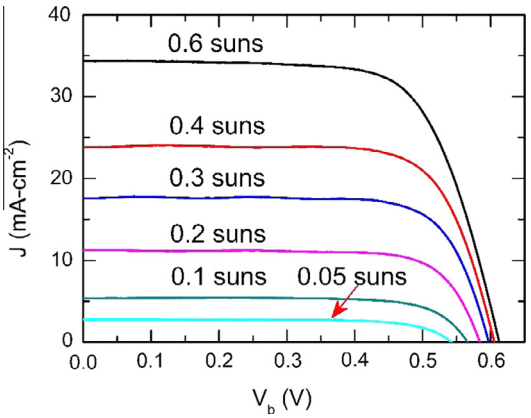

Fig. 5. Experimental current density-voltage (*J-V*) characteristics measured under different illumination levels (P_{in} = 0.05–0.6 suns) of a 20 × 20 mm^2 solar cell using the "Linear Sweep Voltammetry" mode.

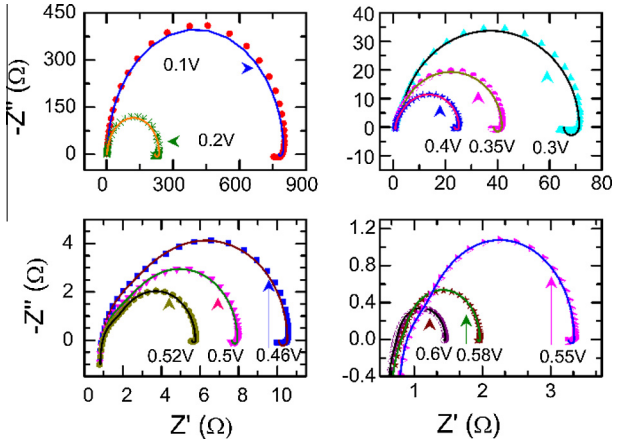

Fig. 6. Impedance spectra (symbols) of the 20 × 20 mm^2 cell measured under different forward bias voltages (V_b = 0.1–0.6 V) in dark. Solid lines are the best fit curves to the measured spectra using the modified equivalent circuit of Fig. 8b. The radii of the semi-circle associated with n$^+$-p junction decrease successively with increasing bias (V_b). Above V_b > 0.3 V the signatures of the p-p$^+$ junction could be seen as a change in the shape at high frequencies. In addition, an arc in the fourth quadrant at forward bias condition can be seen which is attributed to "*negative capacitance*".

(Table 1). However, the trend of two parameters is different and the difference in the respective value of R_x or C_x narrows down with increase in bias voltage. Therefore, following the observation of Garland et al., the larger combination of RC is designated to n$^+$-p junction and smaller combination to p-p$^+$ (Garland et al., 2011a). The inductor L can be considered as a negative or pseudo-capacitance that results in an additional loop at low frequencies in the Nyquist plot (or a dip in the *C′-f* plot at f_t^l). Similar observations are also made by others (Agarwal et al., 1992; Mora-Seró et al., 2006). On the other hand, the inductive tail at high frequency side, which is more prominent at higher forward bias, is taken care by the inductor (L_S) lumped in series with R_S which gives a dip at f_t^h in *C′-f* curve. Further, details for silicon solar cell with BSF using the conventional circuit elements has been discussed in literature (Garland et al., 2011a,b). The simulated curve using the conventional equivalent circuit (8a) is shown in Fig. 9 along with the curve generated using modified circuit (8b). It is evident from the figure that no signature of so called "*negative capacitance*" is observed in the former whereas its presence can be seen in the later case. It is also clear from the simulated spectra (Fig. 9a) that the low frequency loop in the fourth quadrant is entirely due to the inductive component *L*. The resistance (R_L) associated with this additional Voigt element can be considered as a recombination resistance and apparently its role is to reduce the total parallel resistance of the cell. The inductor *L* is reflected as a peak below the abscissa (positive component) in the imaginary part of the impedance (not shown here). The simulated *C′* vs. *f* curve, shown in Fig. 9b, manifests the transition from positive to negative capacitance at the low frequencies (f_t^l). The transition (a dip at f_t^h) on the higher frequency side owes its existence to the inductor (L_S) connected in series, and the presence of which could be attributed to stray effects associated with wires, noise etc. (Ershov et al., 1998; Kumar et al., 2006; Mora-Sero et al., 2009). A comparison of Fig. 9b (simulated) and Fig. 7 (experimental data deduced from Fig. 6) shows the similar features. Therefore, the proposed circuit is deemed fit for the analysis of crystalline silicon solar cell impedance data. Using the modified equivalent circuit, the data shown in Fig. 7 is fitted and the best fits are plotted (solid lines) in the same figure. In general, the fitted curves are in qualitative agreement with the experimental data at all bias conditions (as reflected in low values of goodness of fit, χ^2, which is of the order of 10^{-3}–10^{-5} shown in Table 1). The values of other parameters extracted from the simulations are compiled in Table 1. However, the fitting is superior in high frequency regime as compared to low frequency data, particularly the two f_t positions. It is to be remarked here that rather a poor fitting is obtained with the equivalent circuits reported in the literature (Garland et al., 2011a,b) in comparison to the proposed model (as is shown in Fig. 11). From the above discussion, it can be concluded that c-Si solar cells used in the present study show "negative" or "pseudo-capacitive" behaviour.

The measured impedance spectra and the *C′* vs. *f* data under different illumination without biasing are shown in Figs. 10 and 11 respectively along with the best fit simulated curves using the modified model and the extracted parameter values are compiled in the Table 2. It can be seen that the feature observed at higher frequency under different bias are also largely seen under illumination but with a difference of lowered impedance values. But the low frequency data shows marked difference and no clear transition at f_t^l is observed. The data in this region is scattered and noisy whereas at higher frequencies it is well defined with the increase in P_{in}. For the sake of comparison, the simulated curves using conventional equivalent circuit (Fig. 8a) is also plotted with the best fit curves with the modified circuit (Fig. 8b) for P_{in} = 0.4 and 0.6 suns (Fig. 11) which also fails in providing a good match with the experimental data. A similar effect in low frequency region is reported in time dependent QWIP devices (Ershov et al., 1998) where the *C′-f* data shows both qualitative and quantitative mismatch in capacitance values with simulated results (Figs. 7b and 8b of Ershov et al., 1998) based on Fourier transformation of the transient current can be seen.

The difference in the capacitance values are more than one order of magnitude higher for V_b > 0.55 V vis-à-vis at low V_b (<0.5 V) as can be seen from Table 1. The values begin to increase sharply in the vicinity of the maximum power point or at the knee voltage. This indicates that the device is governed by the depletion capacitance (C_{dl}) at low V_b and the chemical capacitance (C_μ) at higher V_b in the two different bias regimes. The origin of the chemical capacitance is the incremental change in the minority carriers whereas the C_{dl} is associated with depletion region that itself acts as a capacitor and whose magnitude changes with bias. At higher forward bias voltages, the chemical capacitance dominates and $C_j = C_\mu$ which increases exponentially with bias voltage. For reverse and low forward bias, the capacitance is governed by the depletion width of the junction and C_j is governed by C_{dl}. The magnitude of C_j under illumination (Table 2) explains how photo-generation of carriers affect the junction voltage and thereby affect the overall impedance of the device (Yahia et al., 2011). In addition to these

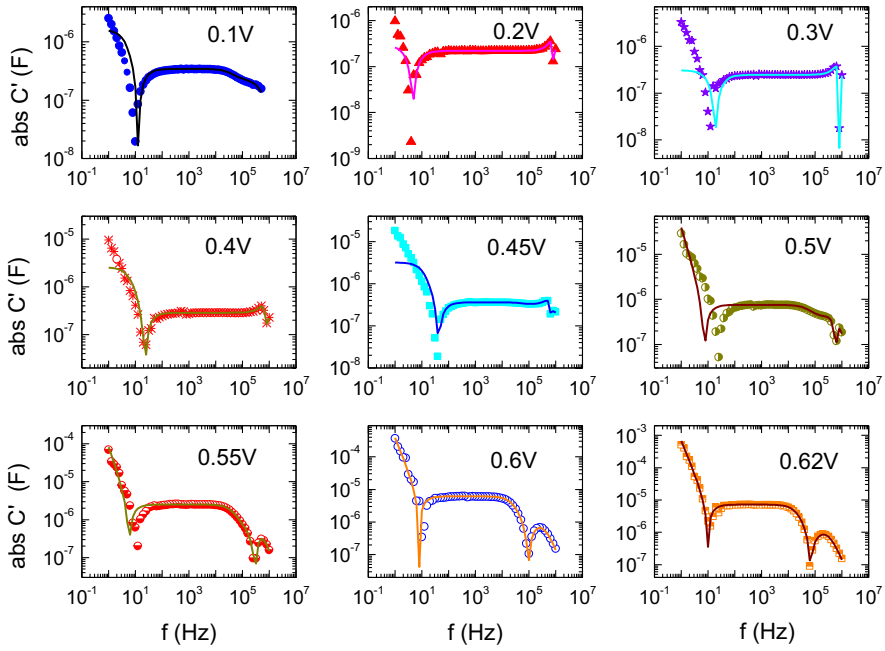

Fig. 7. Capacitance (C) as a function of frequency (f) of the cells under different applied forward bias (V_b = 0.1–0.6 V) conditions. The symbols are measured values whereas the solid lines are the theoretical fit using the modified equivalent circuit shown in Fig. 8b. The two dips at low and high frequency (at f_t^l and f_t^h respectively) manifest the transition of capacitance from positive to negative values having inductive behaviour.

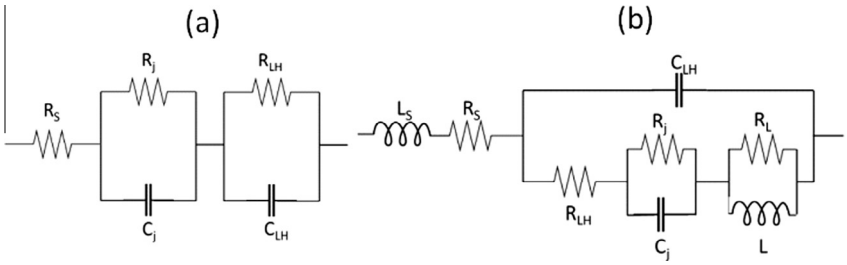

Fig. 8. Electrical equivalent circuit for (a) a crystalline silicon cell with back surface field, and (b) the modified circuit where an inductive Voigt element ($R_L - L$) is introduced along with an inductor (L_S) in series. The modified circuit is used to fit the expenimental data and the corresponding extracted parameters are given in Table 1 and 2 respectively for different forward electrical biases (V_b) and illumination levels (P_{in}).

Table 1
Values of the parameters within measurement uncertainty; series resistance (R_s), inductor (L_s) in series associated with the stray inductances, resistance (R_x) and capacitance (C_x) where x = LH and j corresponds to low-high junction and built-in junction respectively, resistance (R_L), and the inductor (L) that scales with voltage in the same way as R_L, along with the goodness of fit (χ^2) extracted from fitting the impedance plot with modified electrical equivalent circuit at different bias voltage (V_b).

V_b (V)	0.1	0.2	0.3	0.4	0.46	0.5	0.55	0.58	0.6
R_S (Ω)	1.09	0.83	0.81	0.79	0.79	0.8	0.73	0.62	0.57
R_{LH} (Ω)	0.0012	0.003	9.75	9.28	4.1	2.68	0.7	0.3	0.22
C_{LH} (μF)	0.24	0.22	0.24	0.27	0.38	0.48	1.37	2.21	2.9
R_j (Ω)	769.3	218.2	54.88	13.48	5.181	4.17	1.83	0.99	0.65
C_j (μF)	0.115	0.17	0.21	0.35	1.04	1.55	5.44	13	22.8
R_L (Ω)	36.41	18.62	5.896	1.64	0.45	0.29	0.084	0.032	0.018
L (H)	0.95	0.34	0.1	0.034	0.015	0.014	0.01	0.005	0.004
L_S ($\times 10^{-7}$ H)	1.92	1.92	1.94	1.96	1.94	1.94	1.88	2.13	2.16
χ^2	1.66e−3	3.60e−4	3.26e−4	1.99e−4	1.38e−4	1.09e−4	4.71e−5	7.21e−5	7.40e−5

two capacitances, a "*negative capacitance*" also plays a part in deciding the total capacitance under forward bias voltages.

The three combinations of R and C (or L) correspond to three time constants out of which two are capacitive and the third is inductive in nature. One capacitive time constant represents the bulk of the device, i.e., typical of a n^+-p junction. The second capacitive time constant is assigned to low-high (p-p^+) junction in the BSF region. It is noticed that the signature of the low-high junction is seen after certain forward bias voltages ($\geqslant$0.3 V, as shown in Fig. 6) and also at low illuminations (P_{in} < 0.2 suns; Fig. 10). It is known that the built in potential associated with the low-high junction is small as compared to the thermal voltage (~25 mV) particularly across the depletion layer (Garland et al., 2011a,b; Singh and Singh, 1991) and the hole depletion layer on the p^+ side is very thin (e.g., 6.4 nm is reported by Singh and Singh, 1991) as compared to the hole accumulation layer on the p-side. The capacitance associated with the increase in minority carriers in this region is small and hence chemical capacitance associated with it

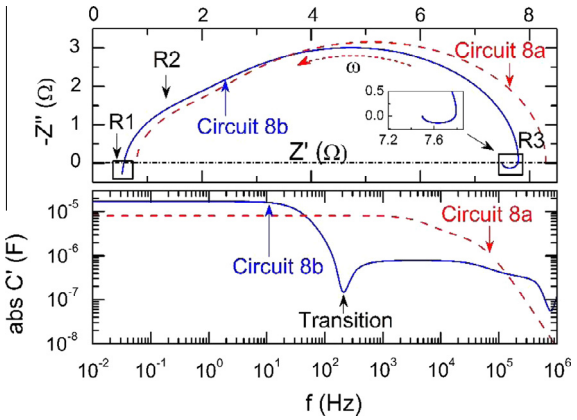

Fig. 9. Simulated impedance spectra (top) and capacitance-frequency (bottom) plots using conventional and modified electrical equivalent circuits shown in Fig. 8. Values of parameters are: R_S = 0.8 Ω, R_{LH} = 1.500 Ω, C_{LH} = 7.000 μF, R_j = 6 Ω, C_j = 15 - μF (for the circuit in Fig. 8a); and R_s = 0.5 Ω, $L_s = 10^{-7}$ H, R_{LH} = 3 Ω, C_{LH} = 0.45 μF, R_j = 4 Ω, C_j = 1.5 μF, R_L = 0.3 Ω, $L = 10^{-3}$ H (for that in Fig. 8b). The areas marked as R_1, R_2 and R_3 represent the high frequency inductive tail, the additional high frequency loop and the low frequency pseudo-capacitive loop respectively. The area R_3 is enlarged in the inset for the sake of clarity. Without inductive component (8a), the curve does not show the dip corresponding to transition from positive to negative capacitance.

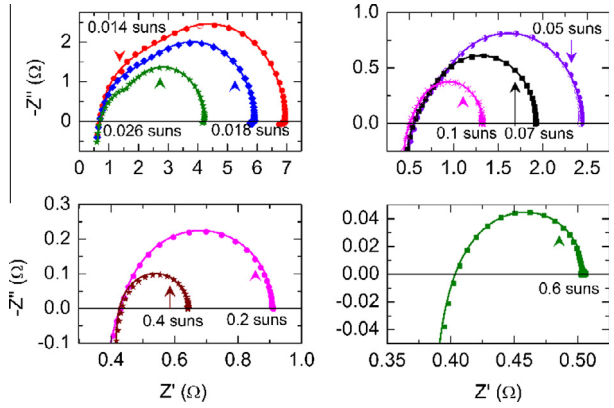

Fig. 10. Impedance spectra (symbols) of a $20 \times 20\ mm^2$ cell under different illumination levels (P_{in} = 0.014–0.6 suns) at STC. The best fit (solid lines) curves to the data using the modified equivalent circuit is also given which gives good fit in the high inductive tail region (which emanates from the inductor connected in series; L_S).

is small. It is only at the higher forward bias, the electrical response of n^+-p junction shifts to low impedance diffusion mode from high impedance charge depletion mode (Garland et al., 2011a,b). Under this condition (V_b > 0.3 V), impedance associated with low-high junction sets-in and the size of second loop grows. As a result ac characteristics deviate from semi-circular nature. Under $Z_j' > Z_{LH}'$ and $Z_j'' > Z_{LH}''$ conditions (absolute values), the arc associated with low-high junction will remain undetected. R_{LH} is always smaller than R_j, however, the difference between the two reduces with rise in V_b. Similar trend is seen in corresponding capacitance values also but their values increase with V_b. The effect of these two parameters is reflected in the relaxation times associated with low-high junction (τ_{LH}) which is below 2 μs and for p-n junction (τ_j) that is less than 100 μs. In the case of illumination, the parameters R_{LH} and R_j are comparable to each other as can be seen from Table 2. In this case the two values are respectively ~1.5 μs and ~10 μs. These τ values are in the vicinity of knee voltage. The magnitude as well as trend observed in τ_j and τ_{LH} are consistent with the values reported in the literature (Garland et al., 2011a,b). Garland et al., 2011a,b has attributed τ_j and τ_{LH} respectively to the lifetime of electrons and relaxation time of holes at the low-high interface. L_S remains unaffected with V_b and P_{in} as it is associated with stray wire and external noises if any. The value of R_L decreases with V_b, a trend observed in R_j (Table 1). Under illumination both R_L and L are orders of magnitude lower compared to the values under bias. The occurrence of "*negative capacitance*" effectively reduces the cell resistance R_{eff} (=$R_j + R_{LH} - R_L$) which represents the effective recombination resistance. The "*negative capacitance*" is observed for $V_b > 0$ V and under very low P_{in} (<0.02 suns). For higher P_{in}, this capacitance starts disappearing which may be attributed to the photoinduced positive capacitance due to linear rise in the excess carrier density. (Kumar et al., 2009; Lungenschmied et al., 2009; Yahia et al., 2011).

As described earlier, a "*negative capacitance*" represents the inductive behaviour of a device which is expected to have capacitive response (Ershov et al., 1998). Generally, the inductive behaviour is associated with magnetic field and dominates at higher frequency regime. As the semiconductor devices display positive capacitance at higher frequencies and a negative tail capacitance in this frequency regime indicates the presence of the parasitic inductance and the overall contribution is taken care by a series inductor L_S. Therefore, the inductive behaviour at lower frequencies cannot be ascribed to the parasitic or to the stray inductance. Further when the conduction current is zero, the total current is the displacement current related to the charge redistribution within the structure which leads to a finite positive capacitance.

The results discussed so far can be summarised as following:

1. The larger loop of impedance data (semi-circular in nature) is due to the n^+-p junction.
2. The deviation of the impedance data from semi-circular nature at higher forward bias (under dark) or under illumination (zero bias) in the high frequency region is ascribed to the LH (p-p^+) junction. This is manifested as a second loop which is only detected when V_b approaches the knee voltage under dark.
3. The inductive tail extended in 4th quadrant also at high frequencies is attributed to the stray effects emanating from wires, etc.
4. The occurrence of an additional loop at lower frequencies in the 4th quadrant represents "*negative capacitance*".

As mentioned earlier that above features are observed in variety of electronic devices that include p-n junction, Schottky diodes, MIS devices, etc., the physical mechanism of which may be different in different devices. In the past the fourth feature is often referred as "anomalous" or attributed to parasitic inductance or to measurement errors (Ershov et al., 1998) and in many cases it is not reported. However, the "*negative capacitance*" (or low frequency inductive behaviour) is reported in devices such as Schottky diodes (Wu et al., 1990), short based p-n junctions (Lindmayer and Wrigley, 1965; van den Biesen, 1990; Laux and Hess, 1999), light-emitting diodes (Hulea et al., 2003; Gommans et al., 2004), and DSSC. (Kron et al., 2003). For example, in the short-base p-n junction, the minority carrier depopulation at high forward bias induces a change in the capacitance sign (van den Biesen, 1990) whereas in quantum well infrared photodetectors, the "*negative capacitance*" effect has been explained on the basis of the non-equilibrium transient injection from the emitter by the injecting contact and inertia of the quantum well recharging process (Ershov et al., 1998). The "*negative capacitance*" is attributed to the existence of defect states at the interfaces between crystalline semiconductor and amorphous carbide layer also (Perný et al., 2014). In the past, the "*negative capacitance*" is observed in the devices where electrical contacts (metal-semiconductor interface) strongly influence the small signal characteristics (Wu

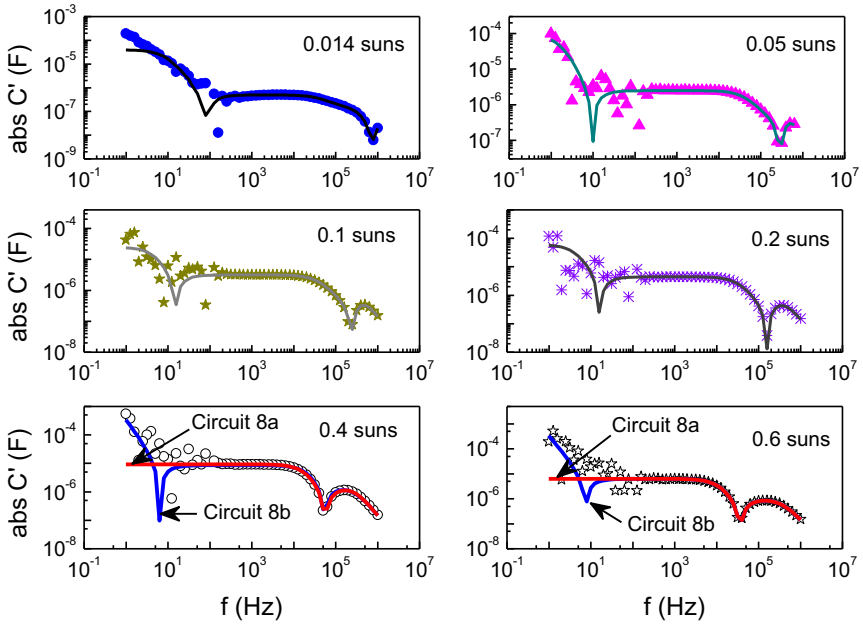

Fig. 11. Capacitance (C) as a function of frequency (f) (experimental and simulated best fit) of the 20 × 20 mm^2 cell under different illumination levels (P_{in} = 0.014–0.6 suns). The symbols represent the measured data whereas the solid lines are the corresponding fits using the modified electrical equivalent circuit shown in Fig. 8b. In the plots corresponding to 0.4 and 0.6 suns the theoretical fits using the conventional equivalent circuit (Fig. 8a) is also shown for the sake of comparison. On the increase in P_{in}, the dip at lower frequency (f_t^l) starts disappearing, whereas high frequency dip (f_t^h) is very well defined. The decreasing trend of C with f at low frequencies (1–10 Hz) is better represented by the modified model. This nature is not even shown by the model based on the more advanced fourier transform of the transient current measured in quantum well infrared photodetectors (QWIP) as can be seen from Figs. 7 and 8 of Ershov et al., 1998.

Table 2
Values of the parameters within measurement uncertainty extracted from fitting the impedance plots with modified electrical equivalent circuit under different illumination (P_{in}).

P_{in} (suns)	0.014	0.018	0.05	0.1	0.2	0.4	0.6
R_S (Ω)	0.56	0.55	0.5	0.5	0.4	0.4	0.38
R_{LH} (Ω)	3.25	2.52	0.72	0.52	0.30	0.25	0.23
C_{LH} (μF)	0.39	0.45	1.48	2.15	3.94	0.29	0.21
R_j (Ω)	2.92	2.66	1.29	0.98	0.61	0.22	0.11
C_j (μF)	1.84	2.31	5.41	7.37	12.3	53.7	124
R_L (mΩ)	163	123	7.19	4.31	3.94	14	15.1
L (mH)	2.42	1.71	0.59	0.10	0.11	28.20	57.50
L_S (×10^{-7} H)	1.18	1.18	1.60	1.53	1.55	1.73	1.63
χ^2	5.28e−5	4.48e−5	3.76e−5	3.23e−5	2.84e−5	2.67e−5	2.38e−5

et al., 1990). So far as the silicon solar cells are concerned, although IS is widely used (Kumar et al., 2009, 2010; Garland et al., 2010, 2011a,b; Crain et al., 2012; Mora-Sero et al., 2009) to study the ac response of the device and the first three features associated with positive capacitance have been discussed but the observation of "*negative capacitance*" is scantly reported (Mora-Seró et al., 2006). In the present study, all the features discussed above except the fourth are in agreement and follows the reported trends. The fourth feature is not well reported and the origin of which is not very clear.

The "*negative capacitance*" observed in silicon solar cells used in the present study is explained in the following section.

It is known that the width of the depletion region drops with increased doping of the semiconductor and according to Schottky theory, Ohmic contacts are represented by low barrier height or small width. The charge carriers tunnel through the depletion region below a certain barrier width. In a solar cell particularly silicon based cells, two metal-semiconductor junctions are in direct contact to the cell structures. For example, in high efficiency n^+-p-p^+ solar cell the two contacts are made by photolithography (front contact patterning) of thermally evaporated front metal layers where Ti/Pd/Ag layers on front and aluminium layer at the back is commonly used (Green, 1982). The contact layers are finally sintered which results in stable Ohmic contacts (Glunz, 2006). On the other hand, industrial solar cell employs screen printing where at the front, silver particles contact the emitter and at the rear, an aluminium-silicon eutectic forms the contact. Low-resistance Ohmic contacts at the rear side of such cell structures are a result of the inter-diffusion of Al into Si, where at times the dopant (Al) is not homogeneously distributed at the interface over the entire contact area. Further, Al forms a low-barrier Schottky diode on p-Si and tunnelling through such a barrier is a function of voltage drop across the diode (Adegboyega et al., 1989). In this scenario, back contact may be non-ideal Ohmic contacts and has tendency of Schottky contact. Similar situation may exist on the front contact also.

Now we would like to discuss why "*negative capacitance*" is seen in some Si-solar cell and is absent in others. It is known that any charge accumulation at an interface (e.g., p-n junction or metal-semiconductor junction) give rise to a positive capacitance. Conversely, its depletion may lead to "*negative capacitance*". For example, "*negative capacitance*" has been observed by Wu et al. (1990) in metal-semiconductor (n-Si) Schottky diode who proposed a charge delocalisation mechanism involving the concept of impact ionisation process which elucidate occurrence of "*negative capacitance*" at forward bias. Under forward bias condition,

electrons fill up empty states at the interface surmounting the Schottky barrier (qV_{SB}). If the electrons possess excess energy, these electrons knock trapped electrons out after collision provided the trap binding energy is smaller than the qV_{SB} (and is also insufficient to create e-h pair in the bulk). Consequently, the overall charge at the interface will decrease with the increase in V_b leading to equivalent capacitance of negative in nature. Further at higher temperatures the disturbance in local distribution of electrons is predominantly unaffected as the empty states created by the ionisation process are quickly refilled by the electrons from metal. Consequently, "*negative capacitance*" is suppressed.

As discussed above the cells used in the present study have screen printed contact which may have non-ideal ohmic contacts. The observed "*negative capacitance*" may be ascribed to such contact having Schottky tendency. The measurements carried out at different intensity levels show disappearance of "*negative capacitance*" under increased P_{in} is a direct manifestation of our believe because large population of charge carriers under high illumination instantaneously fill the trap states or reduces the barrier height. This is an evidence of non-ideal contacts. To reconfirm further our presumption about the origin of "*negative capacitance*", the impedance measurements are carried out on the sample (reported above) at different temperatures (T). It was observed that the contribution of "*negative capacitance*" decreases with the increase in T and disappears completely at $T > 75$ °C. Further, the impedance measurements are carried out on a high efficiency Si solar cell where the contacts were made by photolithography. In this sample, "*negative capacitance*" is not observed at different bias as well as under illumination.

4. Conclusion

Screen printed n^+-p-p^+ structure based silicon solar cells are studied under different forward bias and under illumination levels using impedance spectroscopy technique. Common features like the signatures of n^+-p and p-p^+ junction are seen respectively in the form of a major semi-circular arc extending from low to high frequency region and the deviation from semi-circular nature at high frequency end at large forward bias ($V_b > 0.3$ V) besides the extension of data to fourth quadrant. It has been observed that the transition between n^+-p (diode) and p-p^+ (BSF) cell impedances depend on the biasing condition and the contribution of the later comes more prominent with increase in forward bias. A distinct arc at lower frequency is observed that extends in the negative Z'' direction of the complex Z' vs. Z'' plot. The arc is attributed to pseudo-capacitance or more commonly known as "*negative capacitance*". The equivalent circuit of the solar cell is modified with the introduction of an inductive (L_S) component in series and an inductive Voigt element R_L-L in the circuit. Statistically good fitting of the measured data with the modified equivalent circuit is obtained. The origin of "*negative capacitance*" is attributed to non-ideal metal-semiconductor contacts/interface. This attribution is further verified by measuring the impedance spectra on high efficiency silicon cells where "*negative capacitance*" is not seen. However, more detailed understanding is needed to know the physical processes associated with the "*negative capacitance*". The impedance spectroscopy can be used to assess the performance of solar cell particularly the quality of contacts.

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