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Interpreting the nonideal reverse bias C–V characteristics and importance of the dependence of Schottky barrier height on applied voltage

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Abstract

This work presents an attempt related to the charging behaviour of interface states to the nonideal forward bias current–voltage (I–V) and the reverse bias capacitance–voltage (C–V) characteristics of Al–nSi Schottky barrier diodes. The diode showed nonideal I–V behaviour with an ideality factor of 1.50 and was thought to have a metal–interface layer–semiconductor configuration. Considering that the interface states localized at the interfacial layer–semiconductor interface are in equilibrium with the semiconductor, the energy distribution of the interface states was exactly determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height, Φ_e. The determination of the intercept voltage and interface state density was made by means of a simple interface charge model which has been developed in detail. The I–V characteristics were used for determining the voltage dependence of the barrier height. Although the change in barrier height with applied bias is small, it is important for exactly determining the shape of the interface state density distribution curve. At a frequency of 500 kHz, the nonlinear reverse bias C^{-2}–V plot with the curvature concave downward has been only thought of to be due to the contribution of the capacitance of the interface state charges. It is concluded that the nonlinear nature of C^{-2}–V plots in the frequency range 50–200 kHz has been caused by the interface state charges as well as inversion layer and inversion layer charges. It has been understood by means of the interface state charge model that the C^{-2}–V plots cannot only be interpreted in terms of the contribution of the interface state charges to the device capacitance.

1. Introduction

The metal–semiconductor (MS) contact is one of the most widely used rectifying contacts in the electronics industry [1, 2]. Due to the technological importance of Schottky barrier diodes (SBDs) which are of the most simple of the MS contact devices, a full understanding of the nature of the electrical characteristics of these diodes is of greater interest. Many Schottky diodes are not intimate MS contacts but are, instead, metal–interfacial layer–semiconductor(MIS) structures. Therefore, the nonideal behavior observed in Schottky barrier diodes has been generally attributed to the effect of

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interface states and the interfacial layer, which are present between metal contact and semiconductor interface by many authors [1–28] aside from that of the image force lowering. Thereby, the performance and reliability of SBDs generally depend on interface state density and their energy distribution [3–6, 16–38]. The effect of the interfacial layer properties such as interfacial layer thickness and the interface states in the MS contacts have long been of interest during recent years. Barden [7] discussed how semiconductor surface states or the interface states could make a rectifying barrier height independent of the ork function of the metal contact. Barden [7], and Cowley and Sze [8] also, showed that in the presence of sufficiently small interface states the barrier height should be a linear function of the metal work function. The first work in the determination of the energy distribution of the surface states was made by Crowell and Roberts [9] who used the capacitance–voltage (C–V) characteristics of Au–Si diodes reported by Archer and Atalla [10] but did not regard if the distribution was consistent with that of current–voltage (I–V) characteristics of diodes. They indicated [10] the voltage dependence of the barrier height is a parameter which combines effects of both the surface states and the interfacial layer thickness. Levine [11] suggested that the Schottky barrier height was controlled by the energy distribution of the interface states and the applied potential, and obtained the exponential surface state distribution from the I–V characteristics of Au–nGaAs diodes reported by Padovani [12]. Later, A. Deneuville [13] made a direct comparison of the energy distribution of the interface states obtained from the capacitance and conductance measurement under forward bias by following previously the methods used in MOS structures [14] with that extracted from photoelectric emission at the metal–semiconductor interface. Later on, Borrego et al. [15] presented a method for determining the interface state distribution in SBDs taking into account both I–V and C–V data of Au–nGaAs guarded diodes while considering any deep traps which may be present in the semiconductor depletion layer; his model assumes that the interface states are not in equilibrium with the semiconductor but instead with the metal so that an interfacial layer is neglected.

Furthermore, some researchers used admittance (capacitance) and conductance spectroscopy to obtain the energy distribution of the interface states in nearly ideal SBDs [16–20] and the diodes accepted the same as MIS diodes due to the presence of a thin undesired interfacial layer at the metal–semiconductor interface either during surface preparation, metal evaporation or post-deposition during thermal anneal for ohmic contact forming. Hovarth [21] extended the analysis of Card and Rhoderick [22] to the reverse I–V characteristics and evaluated the energy distribution of the interface states from the reverse and the forward I–V characteristics of SBDs by making special assumptions on the interface states. Wu and Yang [23] presented a model in which the measured diode capacitance is attributed to the modulation of the effective barrier height by the interface charge and formulated relations between the measured capacitance and the physical properties of the interface states by Shockley–Hall–Read statistics and applied this theory to $NiSi_2$–nSi diodes. Recently, Meada et al. [24] developed a new theory based on the model that nonideal I–V characteristics of the SBDs are due to changes of population in the interface states under applied bias, accompanying changes of the barrier height.

While important progress has been made towards the understanding of barrier formation and carrier transport mechanism across the device, there still exists further scope for research, particularly, on the capacitance of MIS structures. Although the experimental C–V characteristics can be fitted using a parameter C_0 called excess capacitance, the origin of this parameter is still not well understood [25]. The experimental results and C–V characteristics have shown that the nonlinear nature of C^{-2}–V characteristics have not been only interpreted introducing the parameter C_0, excess capacitance due to the interface state charges. The purpose of this paper is to show how the bias dependence of the barrier height affects the interface state density distribution and the interfacial layer. A simple method, which has been considered in detail by us, extended by Szatkowsk and Sieranski [26] for the interfacial layer theory (developed by Cowley and Sze [8]) to include the interface charge, has been used for determination of

the effective barrier height and the interface state density from the C–V characteristics at various frequencies. However, it is necessary to show that a nonlinearity or curvature in reverse bias C^{-2}–V plots can arise not only due to the interface states but also due to other effects.

2. Theoretical background

2.1. The surface potential expression as a function of applied bias

The energy band diagram of a metal and n-type semiconductor Schottky diode under bias is shown in Fig. 1, where Φ_m is the metal work function, χ the electron affinity of the semiconductor, δ the thickness of the interfacial layer, V_i the voltage drop across the interfacial layer, Φ_0 the neutral level of the interface states measured from the top of the valance band. The surface potential ψ_s can be obtained as a function of applied forward bias V from Refs. [25–29].

The interface state charge density, Q_s (C/cm^2), resulting from the occupied states between the Fermi level of the semiconductor and the neutral level is given by

$$Q_s(V) = -q\int_{\phi_0}^{E_g - q\psi_s(V) - qV_n} N_s(E)\,dE, \tag{1}$$

in the general case and only for constant N_s by

$$Q_s(V) = -qN_s[E_g - q\Phi_0 - q\psi_s(V) - qV_n], \tag{2}$$

where N_s is the density of the interface states which are in equilibrium with the semiconductor, q is the electronic charge. Using Gauss' Law, from the energy band diagram the potential drop across the interfacial layer under nonequilibrium conditions is represented by

$$V_i(V) = [\Phi_m - \chi - \psi_s(V) - V_n - V] = -\frac{\delta}{\varepsilon}Q_m = \frac{\delta}{\varepsilon}(Q_s + Q_{sc}), \tag{3}$$

where V_n is the potential difference between Fermi Level and the conduction band edge in the neutral region, ε_i the permittivity of interfacial layer and

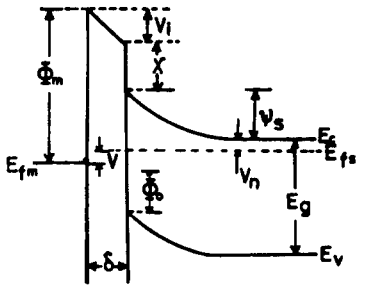

Fig. 1. Energy band diagram of a Schottky diode with the interfacial layer fabricated on an n-type semiconductor under nonequilibrium conditions.

δ its thickness and Q_{sc} the semiconductor depletion layer charge density. Q_{sc} is given by

$$Q_{sc}(V) = -[2q\varepsilon_s N_d \psi_s(V)]^{1/2}, \tag{4}$$

where N_d is the doping concentration of the n-type semiconductor, ε_s the permittivity of the semiconductor. Q_{sc} in Eq. (4) for simplicity in determining the surface potential expression can be neglected because it is quite small compared with the interface charge density in the interface states. An estimation of the relative magnitude of the Q_{sc} and Q_s can be made as follows. The potential differences and the charge are related by

$$V_i = \frac{\delta}{\varepsilon_i}Q_s, \tag{5a}$$

$$\psi_s(V) = \frac{qN_d d^2}{2\varepsilon_s} = \frac{Q_{sc}d}{2\varepsilon_s}. \tag{5b}$$

The ratio of both charges is roughly given by

$$\frac{Q_{sc}(V)}{Q_s(V)} = \frac{2\varepsilon_s\delta}{\varepsilon_i d}\frac{\psi_s(V)}{V_i(V)}, \tag{6}$$

where $\delta \simeq 20$ Å and d (thickness of the depletion region) $\simeq$ several thousands of Å, i.e. δ and d are different by more than two orders of magnitude; ε_s and ε_i are of the same order of magnitude. Therefore, the space charge density Q_{sc} can be neglected compared to the interface state charge density Q_s.

From Eqs. (2) and (3), the following expressions arise:

$$\psi_s(V) = c_2(\Phi_m - \chi) + (1 - c_2)[E_g/q - \Phi_0] - c_2 V - V_n, \tag{7}$$

$$\alpha = \frac{q^2 \delta N_s}{\varepsilon_i}, \tag{8}$$

$$c_2 = \frac{1}{1+\alpha} = \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta N_s}, \tag{9}$$

$$\Phi_B = c_2(\Phi_m - \chi) + (1 - c_2)(E_g/q - \Phi_0). \tag{10}$$

Here Eq. (8) is approximately the expression for the barrier height of a metal–n-type semiconductor SBD. Thus, Eq. (5) can be written as

$$\psi_s(V) = \Phi_B - c_2 V - V_n. \tag{11}$$

The surface potential expression given as a function of applied bias in Eq. (7) was first derived by Chattopadhya et al. [28] following Fonash [29], but we have considered that the approximation done in obtaining this equation was equivalent to neglecting the space charge Q_{sc} in the depletion region.

If measurements are carried out at very high frequency, w (such that the lifetime, τ, is much larger than w^{-1}), the charge at the interface states cannot follow an AC signal, that is, at high frequencies the equivalent circuit of the device will be just the oxide and depletion capacitance in series. This will occur when the time constant is too long to permit the charge to move in and out of the interface states in response to an applied signal. In this case the capacitance per unit area of the MIS diode is represented by

$$C = \frac{dQ_{sc}(V)}{d\psi_s(V)} \frac{d\psi_s(V)}{dV}. \tag{12}$$

Using Eqs. (4), (11) and (12), C can be expressed as

$$C = c_2 \left[\frac{q\varepsilon_s N_d}{2(\Phi_B - c_2 V - V_n)} \right]^{1/2} \tag{13}$$

or

$$C^{-2} = \left[\frac{2(\Phi_B - c_2 V - V_n)}{q\varepsilon_s c_2^2 N_d} \right]. \tag{14}$$

Furthermore, as can be seen from this expression the C^{-2} vs V plot is a straight line whose intercept with the V axis gives the value of V_0 and the slope the value of c_2. Thus Φ_B and c_2, respectively, can be given as follows:

$$\Phi_B = c_2 V_0 + V_n, \tag{15}$$

$$c_2 = \frac{2}{q\varepsilon_s N_d [d(C^{-2})/dV]}. \tag{16}$$

Since we know the values of the Fermi energy and c_2, the barrier height Φ_B for the MIS diode can be calculated from Eq. (15).

Usually, at the semiconductor–interfacial layer interface there are various kinds of states with different lifetimes. At low frequencies where $w\tau \ll 1$, all the interface states affected by the applied signal are able to give up and accept charge in response to this signal. The interface state capacitance appears directly in parallel with the depletion capacitance resulting in a higher total value of the capacitance for the Schottky diodes than if no interface states were present. At intermediate frequencies where $w\tau \simeq 1$, some, but not all, of the interface state charge will participate in small-signal measurements, and values of the capacitance observed will be between the low and high frequency values [1–3, 16–25]. A parameter λ which is a function of frequency ($\lambda(0) = 1$ and $\lambda(\infty) = 0$) should be described by considering the realistic assumption that for intermediate frequency some of them (λQ_s) follow an AC signal [16–26].

In this case the capacitance can be written [26] as

$$C = \frac{d[Q_{sc}(V) + \lambda Q_s(V)]}{d\psi_s(V)} \frac{d\psi_s(V)}{dV}. \tag{17}$$

Substituting Eqs. (2), (4), (11), (15) and in Eq. (17) one can obtain the expressions for the capacitance as follows [26]:

$$C = a(\lambda)(V_0 - V)^{-1/2} + b(\lambda), \tag{18}$$

$$a(\lambda) = [1 - \lambda(1 - c_2)] \left(\frac{q c_2 \varepsilon_s N_d}{2} \right)^{1/2}, \tag{19}$$

$$b(\lambda) = \lambda c_2 q^2 N_s. \tag{20}$$

As it is seen from Eq. (18), the capacitance measured C vs $(V_0 - V)^{-1/2}$ plot is a straight line for any

capacitance vs $(V_0 - V)^{-1/2}$ plot is shown in Fig. 4 for six different frequencies. According to Eqs. (18)–(22), $a(\lambda)$, $b(\lambda)$ and λ were calculated from the plot of C vs $(V_0 - V)^{-1/2}$ for each frequency, but N_s for only 500 kHz and 1 MHz frequencies. The values of these parameters are shown in Table 1. A value of 3.6×10^{15}/eV m^2 for N_s was obtained at 500 kHz, which is an intermediate frequency, because at this frequency some, but not all, of the interface state charge will contribute to AC small-signal measurements. As can be seen in Table 1, the values of $b(\lambda)$ and N_s calculated from the C–$(V_0 - V)^{-1/2}$ plot for 1 MHz are negligibly small. We cannot calculate the value of N_s in the frequency range 50–200 kHz for our sample because the slopes of C–$(V_0 - V)^{-1/2}$ curves belonging to these frequencies, that is, the values of $a(\lambda)$, are much greater than the value of 2.77×10^{-12} for $a(0)$ for the sample. According to Eq. (21), the value of $a(\lambda)$ must be lower than the value of $a(0)$, or the ratio $a(\lambda)/a(0)$ must be very close to one. For example, to obtain a value of the order of 10^{16}–10^{17}/eV m^2 for N_s, the ratio $a(\lambda)/a(0)$ must be in the range 1–0.99. As can be seen in Fig. 4, the slopes are larger for lower values of the frequency. As a result of the above explanations, it is evident that the dependence of the capacitance of our Schottky diode upon frequency (therefore excess capacitance) cannot be only interpreted by considering the effect of the interface state charge. According to Chattopadhya [25], one may think of two possible effects, namely, the interface state charge effect and the inversion layer charge effect for the anomalous behaviour of C^{-2}–V plots. There is the effect of the inversion layer charge on the capacitance of our device, since the shape of C^{-2}–V plots in the frequency range 50–200 kHz for our sample is similar to that given in Fig. 2 of Ref. [25]. Likewise, because our measurement frequencies (50–200 kHz) are not high, both inversion layer charges in the semiconductor and the interface state charges follow the AC signal and contribute to the capacitance of the device. The value of $a(\lambda)$ to be greater than that of $a(0)$ indicates that the capacitance of the device is composed of not only capacitances due to space charges and interface state charges but also capacitances due to these charges and inversion layer charges.

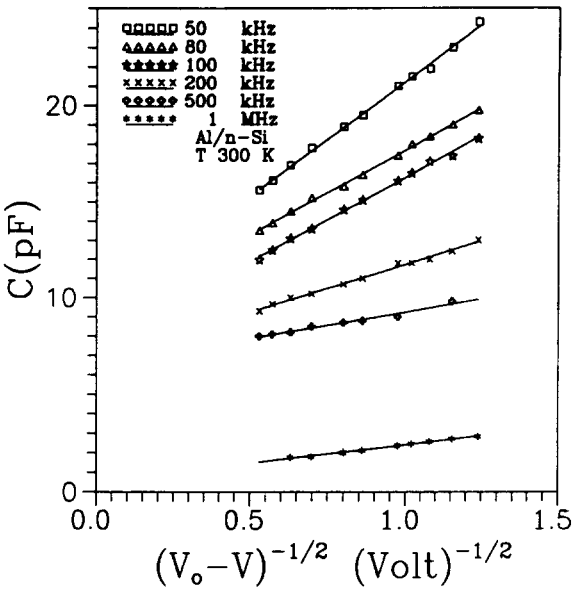

Fig. 4. Capacitance vs $(V_0 - V)^{-1/2}$ curves of an Al/n-Si Schottky diode.

Table 1
The experimental parameters of the reverse bias C–$(V_0 - V)^{-1/2}$ characteristics at five frequencies. $a(0) = 2.77 \times 10^{12}$, $A = 7.85 \times 10^{-3}$ cm^2

f(kHz)	$b(\lambda)$ (pF)	$a(\lambda) \times 10^{-12}$ (C V$^{-1/2}$)	$a(\lambda)/a(0)$	λ	N_s/eV m^2
50	9.35	11.87	4.285	−6.57	–
80	8.92	8.74	3.155	−4.31	–
100	7.52	8.74	3.155	−4.31	–
200	6.77	4.95	1.787	−1.57	–
500	6.53	2.73	0.986	0.029	3.6×10^{15}
1000	0.54	1.86	0.671	0.657	1.3×10^{13}

The value of 1.50 for n was calculated from the linear region of the semilog forward bias I–V characteristics shown in Fig. 5 indicating that the effect of series resistance in this region was not important. This value of n indicates that the devices obey a metal–interface layer–semiconductor (MIS) configuration rather than an ideal Schottky diode. The interface oxide layer may be formed either during surface preparation and metal evaporation or post-deposition thermal annealing [3–5, 25–29]. At high currents there is always a deviation which has

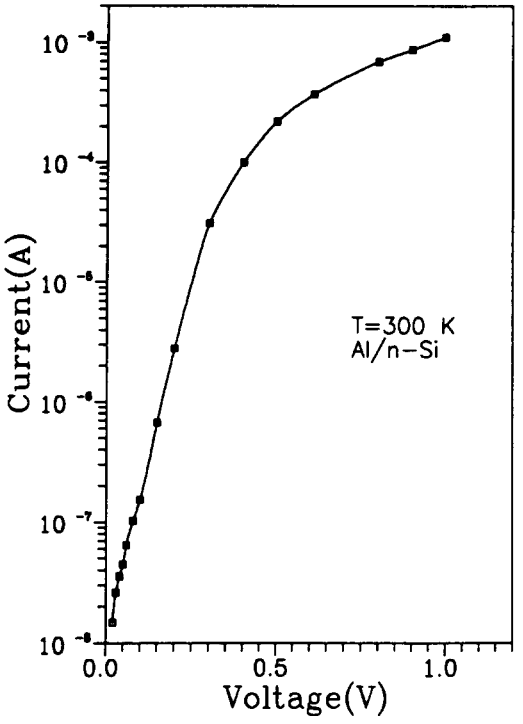

Fig. 5. Forward bias current vs voltage characteristics of an Al/n-Si Schottky diode.

been clearly shown to depend on the interface state density and bulk series resistance, as one would expect. The lower the interface density and the series resistance, the greater the range over which $\ln I$–V does in fact yield a straight line. As the linear part of $\ln I$–V plots is reduced, the accuracy of determination of Φ_b and n are poor. The barrier height, as well as other Schottky diode parameters as the ideality factor n and the series resistance R_s were achieved using a method developed by Cheung [34]. Cheung's functions

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right), \tag{32}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right), \tag{33}$$

and

$$H(I) = IR_s + n\Phi_b \tag{34}$$

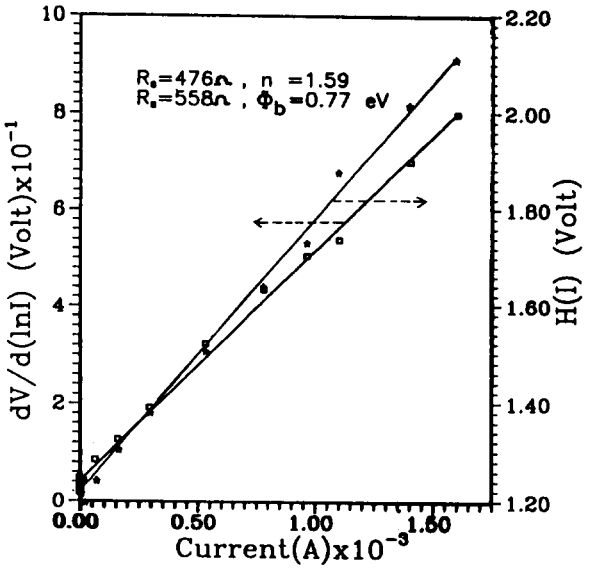

Fig. 6. Experimental $dV/d(\ln I)$ vs I and $H(I)$ vs I curves.

should give a straight line for the data of downward curvature region in the forward bias I–V characteristics. Schottky contact parameters were obtained from the vertical axis intercepts ($n = 1.59$, $\Phi_b = 0.77$ eV) and from the slopes of the functions ($R_s = 517\,\Omega$ as average). The plot associated with these functions is given in Fig. 6. Thus, it is clearly seen that the value of 1.59 for n from the downward curvature region which results from the series resistance and interface effects is greater than the value of 1.50 obtained from the linear region of the same characteristics.

Furthermore, these also is the effect of the interface states, which are in equilibrium with the semiconductor, on the I–V characteristics at high forward bias values, the curvature downward region. In this region the ideality factor n is rather controlled by the interface states. Therefore, the I–V data shown in Fig. 5 fitted well to the equation

$$I = 1.25 \times 10^{-8} \exp\left\{\frac{qV}{nkT}\right\}, \tag{35}$$

with the n values given in Table 2, where $I_0 = 1.25 \times 10^{-8}$ A is the saturation current. Substuting the values of the voltage dependence on n from

frequency. When capacitance measurements are carried out at different frequencies, the parameters of interface states can be calculated from the formula below:

$$\lambda = \frac{[1 - a(\lambda)/a(0)]}{(1 - c_2)}, \tag{21}$$

$$N_s = \frac{b(\lambda)}{q^2 c_2 \lambda}. \tag{22}$$

In these equations, parameters $a(0)$, $a(\lambda)$ and $b(\lambda)$ can be evaluated from the C vs $(V_0 - V)^{-1/2}$ plot for each frequency.

2.2. Current–voltage characteristics

When a metal–semiconductor contact with interfacial layer (MIS) is considered, it is assumed that the forward bias current in a Schottky barrier is due to thermionic emission current corrected by tunneling and is expressed [22, 28, 30] as

$$I = A^* A T^2 \exp(-\Phi^{1/2}\delta) \exp\left\{\frac{-q[\psi_s(V) + V_n]}{kT}\right\}, \tag{23}$$

where A^* is the Richardson constant, A the diode area, and Φ the mean barrier height presented by the thin interfacial layer. The term $\exp(-\Phi^{1/2}\delta)$ is commonly known as the transmission coefficient across the thin interfacial layer.

Now, from Eqs. (9), (11) and (23), the expression for current in a MIS diode can be given as

$$I = A^* A T^2 \exp(-\Phi^{1/2}\delta) \exp\left(\frac{-q\Phi_B}{kT}\right) \times \exp\left(\frac{c_2 q V}{kT}\right), \tag{24}$$

$$I = I_0 \exp\left\{\frac{qV}{[1 + (q^2 \delta N_s/\varepsilon_i)]kT}\right\}, \tag{25}$$

where

$$I_0 = A^* A T^2 \exp(-\Phi^{1/2}\delta) \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{26}$$

is the saturation current and

$$\frac{1}{c_2} = \left[1 + \frac{q^2 \delta N_s}{\varepsilon_i}\right] \tag{27}$$

is the ideality factor of the device and the fact that this parameter has a value greater than unity suggests that the voltage applied is not dropped entirely across the depletion layer. n or $1/c_2$ can be found from the linear portion of the forward bias $\ln I$ vs V plot.

In Eq. (24), the voltage dependence of the effective height Φ_e is contained in the factor n through the relation

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n}, \tag{28}$$

where β is the voltage coefficient of Φ_e. The effective barrier height is given by

$$\Phi_e = \Phi_B + \beta V. \tag{29}$$

Furthermore, for an MIS diode the ideality n becomes greater than unity as proposed by Card and Rhoderick [22] and given by

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{d} + q^2 N_s\right). \tag{30}$$

The terms used in Eq. (30) are the same as those used in other equations.

In an n-type semiconductor, the energy of the interface states E_s with respect to the bottom of the conduction band at the surface of the semiconductor is given [16, 20] by

$$E_c - E_s = q\Phi_e - qV. \tag{31}$$

3. Experimental procedure

The Al/nSi Schottky diodes used in this study were fabricated by evaporation of 99.99% pure Al as rectifying contact on the (111) face of Si wafers. Si was obtained from Wacker and it had a resistivity of 1400 Ω cm. An Au–Sb alloy was used for the ohmic contact to nSi. The doping concentration was measured using the van der Pauw technique and was found to be $2.79 \times 10^{18}\,m^{-3}$ [31]. Evaporation was carried out at about 10^{-5} Torr. Samples

were first mechanically polished and then chemically etched in CP-4 ($HF:CH_3COOH:HNO_3$; 1:1:2) solution for 3 min. They were then dipped in $HF:H_2O$ (1:15) solution to remove the native oxide layer on the surface. However, it is generally known that there is an oxide layer with thickness of about 10–20 Å on a Si surface irrespective of surface preparation conditions even after etching with diluted HF [3–9, 25–29]. But not always, it is possible to produce a hydrogen-terminated surface in diluted HF.

4. Results and discussion

The reverse C^{-2}–V characteristics of the Al/nSi Schottky diode are shown in Fig. 2 for five different frequencies. A downward curvature was observed in the 0.0–0.5 V region of the data for all frequencies. This region continues up to about 0.25 V for 50 kHz and up to about 0.5 V for 500 kHz. That is, the position that the curve is ended shifts towards a higher voltage with increasing frequency. This behavior has been attributed to either only bias-dependent charges in the interface states or the inversion layer charge in the semiconductor together with the interface state charge. The reverse C^{-2}–V plot for 1 MHz is linear with an intercept voltage of $V_0 = 0.55\ V$ (Fig. 3). The fact that the C^{-2}–V plot at this frequency is linear indicates that the interface states and the inversion layer charge cannot follow the AC signal at this high frequency and consequently do not contribute appreciably to the diode capacitance. From the slope of the 1 MHz, C^{-2}–V plot using Eq. (16), a value of $c_2 = 0.50$ was obtained. Then, using Eq. (15) the barrier height value equal to 0.67 eV was determined. The fact that at high frequency, 1 MHz, the value of the intercept voltage and the doping concentration are greater than that expected can be explained as follows. The presence of the interface states will alter the shape of a C^{-2}–V plot even if the measurements are made at a high frequency that the interface state charges do not contribute to the capacitance measurements. At a given bias, if the Fermi level does not coincide with the neutral level, there will be a net interface state charge at the surface due to the interface states, and these charges

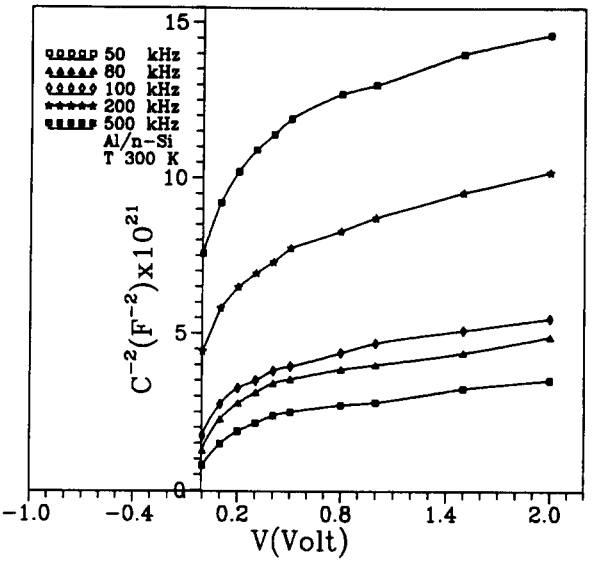

Fig. 2. Reverse bias C^{-2} vs V curves at five different frequencies of an Al/n-Si Schottky diode.

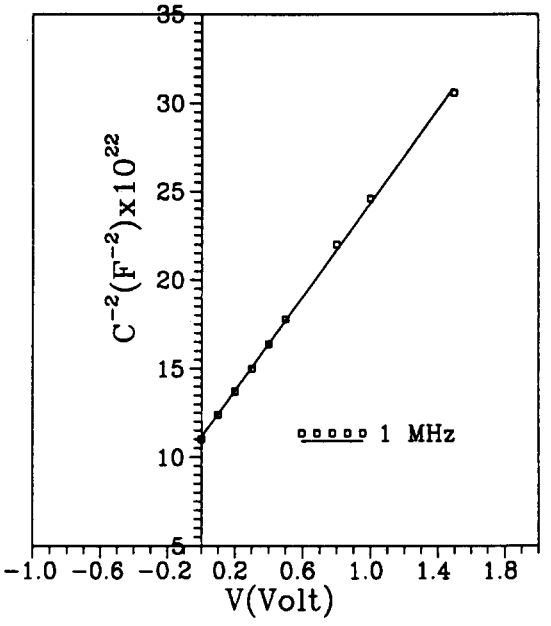

Fig. 3. Reverse bias C^{-2} vs V curves at 1 MHz of an Al/n-Si Schottky diode.

will give rise to an additional field in the oxide layer. This will result in a larger voltage drop across the oxide layer than would be experienced if no interface states were present [32, 33]. The

Table 2
Interface state energy distribution obtained from the forward I–V characteristics at 300 K, $\Phi_b(C$–$V) = 0.67$ V

Voltage (V)	$n = 1/c_2$	Φ_e (V)	$(E_c - E_s)$ (V)	$N_s \times 10^{16}$/eV m^2
0.200	1.50	0.737	0.537	4.25
0.225	1.50	0.745	0.520	4.25
0.250	1.50	0.753	0.503	4.25
0.275	1.50	0.762	0.487	4.25
0.300	1.50	0.770	0.470	4.25
0.325	1.55	0.785	0.460	4.65
0.350	1.63	0.805	0.455	5.36
0.375	1.68	0.822	0.447	5.78
0.400	1.73	0.839	0.439	6.21
0.425	1.80	0.859	0.434	6.81
0.450	1.86	0.878	0.428	7.32
0.475	1.94	0.900	0.425	8.00
0.500	2.00	0.920	0.420	8.51
0.525	2.07	0.941	0.416	9.11
0.550	2.15	0.964	0.414	9.79

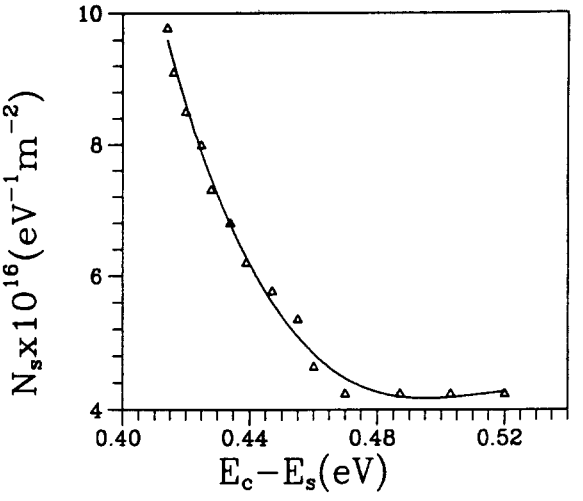

Fig. 7. Interface state energy distribution plot of an Al/n-Si Schottky diode.

Table 2 in Eq. (27), using $\delta = 26$ Å for $n = 1.50$ [22], $\varepsilon_i = 4\varepsilon_0$ [32], the values of N_s as function of V were obtained. These values of N_s were converted to a function of $E_c - E_s$ using Eq. (31). N_s vs $E_c - E_s$ is also shown in Table 2 and Fig. 7. Furthermore, the values of the bias dependence of Φ_e were calculated form Eqs. (28) and (29) and are listed in Table 1. The value of Φ_b (= 0.67 eV) used in Eq. (29) was evaluated from the C^{-2}–V characteristics at 1 MHz (Fig. 3) using Eq. (15). In the forward bias case, the increase of the effective barrier height of the diode Φ_e with bias can be understood as follows: When the diode biased in the forward direction, the quasi-Fermi (imref) for the majority carriers rises on the semiconductor side. Thus, most of the electrons will be injected directly into the metal forming a thermionic emission current, while some of them are trapped by the interface states. This charge capture process results in an increase of the effective barrier height, thereby reducing the diode current [23, 32]. As was seen in Fig. 7, a slow exponential increase of the interface state density exists from midgap towards the bottom of the conduction band. This case indicates the continuum of the interface states. Such a high density of the interface states can be related to the existence of a thin native oxide layer and to its growth during etching [3–5, 25–29]. The values obtained for the interface states are of the same order 10^{16}/m^2 eV, as those reported by some authors for metal/Si Schottky diodes [35–38]. The shape of the density distribution of the interface states in the range $E_c - 0.40$ eV to $E_c - 0.537$ eV is in close agreement with those obtained for n-type Si Schottky diodes of different metallization by Schottky capacitance spectroscopy [35–38] and the Schottky I–V characteristics [19, 20].

In conclusion, the nonideal forward bias I–V behaviour observed in the Al–nSi Schottky diode has been attributed to a change in the metal–semiconductor barrier height due to the interface states and the interfacial layer, and even if the change in barrier height with bias is therefore small, it is important to consider this effect in determining the interface state density distribution from the forward bias ln I–V characteristics. Furthermore, the C–$(V_0 - V)^{-1/2}$ plots with large slope from the measurements in the low frequency range 50–200 kHz suggested that the nonlinear nature of C^{-2}–V plots having the shape of particularly our C^{-2}–V plots has not only been interpreted by introducing the capacitance due to the interface state charges. Therefore, the C–V characteristics of the device are studied to be interpreted by considering the presence of the interface states, the inversion layer and the inversion layer charges. But, it can be

concluded that nonlinearity of C^{-2}–V characteristics being nearly ideal as in Ref. [26] can be interpreted by the capacitance due to the interface state charges.

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