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Characterization of defects in mono-like silicon wafers and their effects on solar cell efficiency

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ABSTRACT

Cell efficiency distribution of mono-like silicon ingot was investigated. And a long low-efficiency tail was found in the efficiency distribution chart, which degraded the cost-effectiveness of this material. Highly spatial resolved photoluminescence and electron back-scattered diffraction characterizations of the mono-like silicon wafers were performed to investigate the low-efficiency reasons. In the experiments, we found that lots of sub-grains, invisible with naked eyes, formed by low angle grain boundaries and high density of dislocations. Relationship of low angle grain boundaries, dislocations and cell efficiency were also investigated and calculated. It is found that the density of dislocations and low angle grain boundaries increase rapidly in the directional solidification of mono-like silicon ingot. Wafers from the top side of the ingot had high density of dislocations and low angle grain boundaries, which led to low-efficiency cell performance and long low-efficiency tail distribution.

1. Introduction

Silicon is the main material for the expanding photovoltaic (PV) products. In PV field, solar cells are mainly manufactured on multi-crystalline silicon (mc-Si) wafers and single crystalline silicon wafers. Compared with the single crystalline silicon wafers, mc-Si wafers are limited in lower conversion efficiency since there are much more crystal defects such as dislocations, grain boundaries and metallic impurities [1]. These defects can act as the recombination center for minority carriers, degrading the bulk lifetime of silicon wafers and solar cell performance.

To improve the solar cell performance of mc-Si, effect of micro-structures of grain and grain boundary, dislocation density and impurity content on cell efficiency are widely and intensively investigated [2,3,4–8]. Micro-structures of mc-Si could be improved by controlling the initial growth conditions and cooling rate of silicon dendrites. So, some larger grain silicon ingot with lower density of defects will be obtained in high efficiency solar cell applications. By cast technology with seeds covering the crucible, some obtain an ingot with one large dominating grain in the center and small grains surrounded. These ingots are called mono-like silicon or quasi-single crystalline (QSC) silicon. It is reported that mono-like silicon solar cell could give much higher cell efficiency performance than mc-silicon solar cell, which is even closed to the efficiency behavior of the single-crystal solar cell [1,9].

Compared with random grain boundary defects in mc-Si wafers, Low angle boundaries have been reported as serious defects to deteriorate solar cell performance [2,6].

For further investigation of the effect of defects on solar cell performance, photo-luminescence (PL) spectroscopy was used to observe the characterization of defects in mono-like wafers, which was proved to be a useful non-contacting and non-destructive technique in characterizing the distribution of defects and harmful impurities in semiconductor or solar wafer materials [10,11]. Electron back-scattered diffraction (EBSD) technology was also introduced in the experiments and used to characterize the grain angle, grain orientation and other grain parameters. Our investigation showed that large quantity of low angle grain boundaries with relative angle of less than 10° were found in mono-like silicon wafers, on which no grains or grain boundaries could be observed with naked eye.

In this work, we gave the defect distribution chart from bottom side to top side of one silicon block. We also showed the relationship of these defects and solar cell efficiency performance. We hope these results will help to understand the reasons of low-efficiency in mono-like silicon materials and enhance the application of the mono-like silicon in industry.

2. Materials and methods

A mono-like Si ingot was casted by directional solidification technology, boron-doped with the resistivity of 1.0–3.0 Ω-cm and the growth direction of ⟨100⟩. 16 blocks from the center part of the

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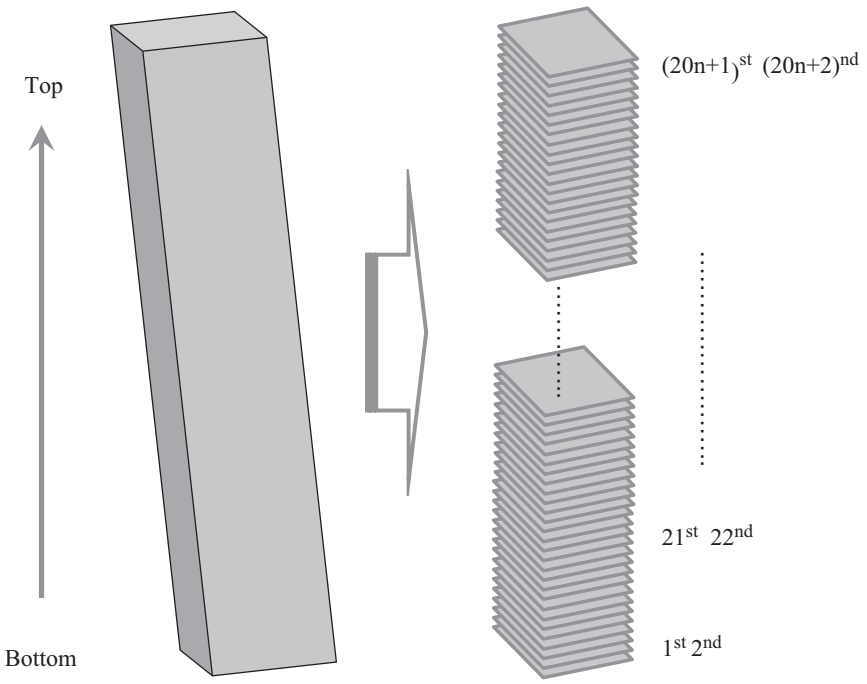

Fig. 1. Sketch showing the selection of wafers from the mono-like silicon block.

ingot are mono-like silicon and the 20 blocks from the edge part of the ingot are partly mono-like silicon or multi-Si. In the experiments, 16 blocks from the center part of the ingot were used. Wafers were sliced with the thickness of 200 μm and the dimension of 156 mm × 156 mm. As shown in Figs. 1 and 2 sample wafers were selected every 20 wafers by sequence from bottom side to top side of the block. One of the two wafers is used for PL test and some destructive experiments, such as dislocation etch and EBSD investigation. The other one is made into solar cell for cell efficiency performance investigation. It can be concluded that the characters of the two neighboring wafer are nearly the same.

PL images of as-cut wafer and finished solar cell made by the neighboring wafer have been acquired using the commercially available PL system equipped with a laser of 808 nm and a silicon CCD camera with a resolution of approximately 1 mega pixel [10]. For PL imaging of as-cut wafers, 5 V laser voltage and 20 s acquisition time were used, and for solar cell test, PL image was recorded by using 5 V and 3 s acquisition time.

For EBSD test, samples are chemically polished for about 3.5 min in HNO_3–HF mixture solutions (HNO_3: HF=6:1) to remove the damaged layer, and then cleaned in DI water to remove the contaminations. EBSD images are investigated by Zeiss Sigma FESEM and Oxford HKL Nordlys S detector with voltage 20 KV and step length 50 μm. Large samples with area up to 156 mm × 15 mm, are scanned in EBSD test experiment for statistically significant of the measured data.

Dislocations and grain boundaries are observed by optical microscope, after the wafers were mirror-polished by chemical-mechanical polishing machine, cleaned by DI water and etched for 5 min in sirtl etchant solution (HF(49%): CrO_3(5 M/L)=1:1). The fraction of dark line and defect networks on as-cut wafers' PL image was calculated by area, in which the wafer PL image was divided into 100 parts to estimate and calculate the fractions of dark line networks areas.

All the other wafers from the center 16 blocks of the ingot were made into solar cell to investigate the cell efficiency distribution. In the solar cell process, alkali solution was used to form 'inverted pyramid' texture.

3. Results and discussion

Fig. 2 shows the optical photograph and the PL image of mono-like wafer used in this study. In Fig. 2(a), no grains or grain boundaries could be observed in naked eyes on the wafer and the wafer has only one grain. In Fig. 2(c), EBSD test results also showed that only one grain orientation was found and the orientation is ⟨100⟩, which was the same as seed crystal silicon orientation. Fig. 2 (a) and (c) can tell that mono-like silicon has only one large silicon crystal grain, and the grain orientation inherits from the original seed orientation like CZ-Si. Fig. 2(b) is PL image of the wafer, on which we found some dark line and network pattern in the image. It is reported that dark contrast means strong recombination centers of minority carries [11] in PL image, and the recombination centers are always induced by heave metal impurities or defects. In the paper, these dark lines and network defects in PL images are named *R*ecombination *A*ctive *N*etwork defects (RAN defects).

To study the solar cell efficiency distribution of the whole mono-like ingot, we made all the wafers from the ingot into solar cells, in which alkali solution was used to form 'inverted pyramid' texture and a SiN_x layer was used to form a uniform antireflection film by PECVD.

Fig. 3 showed the cell efficiency distribution of the whole 16 sample blocks in the experiment. We found that it was a non-normal distribution and there exists a long tail on the low efficiency side. There must be something with strong recombination electrically centers do harmful effect on the cell efficiency performance of the wafers. To investigate the low-efficiency tail details reasons and location of the low efficiency wafers in the ingot, we investigate the detail trends of cell efficiency from bottom side to top side of the ingot. One mono-like silicon block was chosen and the wafers from the block were laser marked in sequence. And then, we made them into solar cells. Efficiency trend chart of the solar cells was showed in Fig. 4.

It could be found that the cell efficiency decreased rapidly as the cell wafers approach to the top of the ingot. In other words, the cell efficiency decreased along with the crystal ingot growth direction quickly. The cell efficiency difference of the top wafer

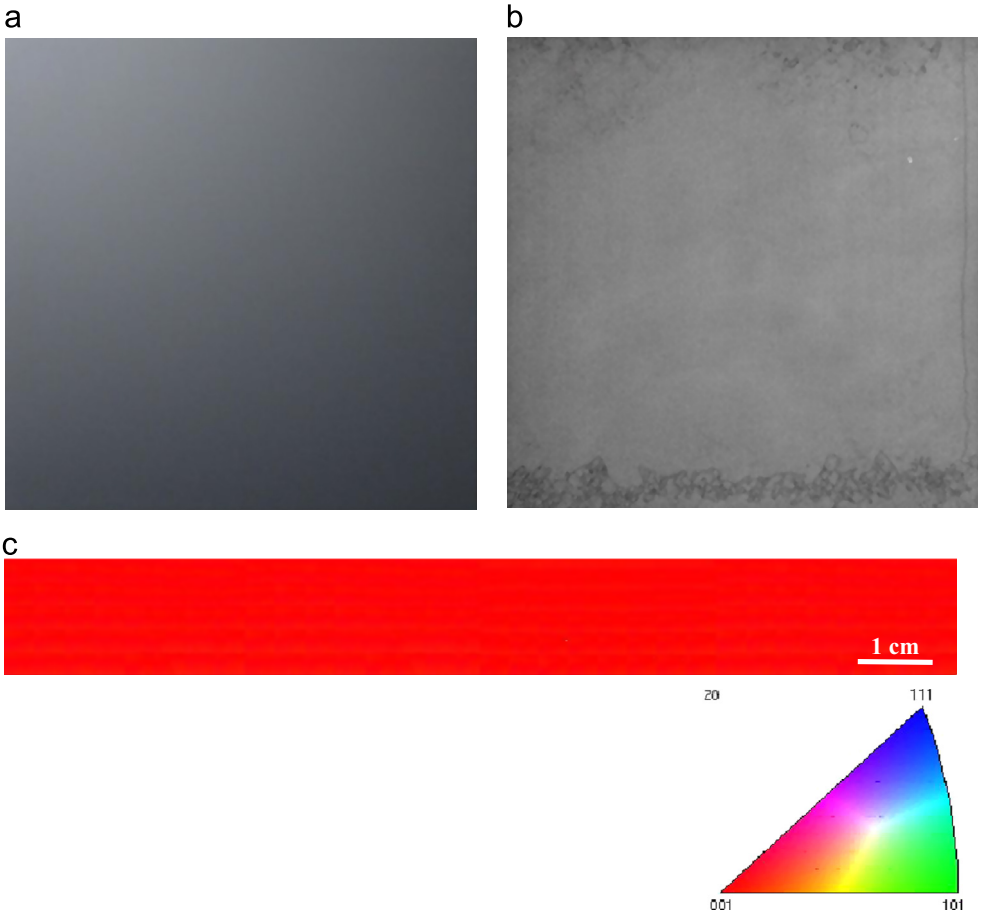

Fig. 2. Optical photograph (a), PL image (b) and EBSD mapping (c) of mono-like silicon wafer.

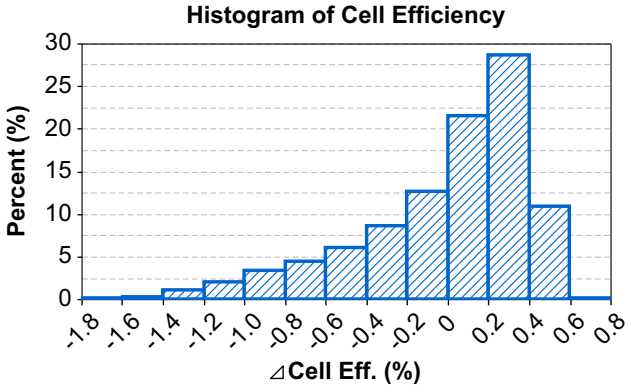

Fig. 3. Cell efficiency distribution of whole wafers from one mono-like ingot.

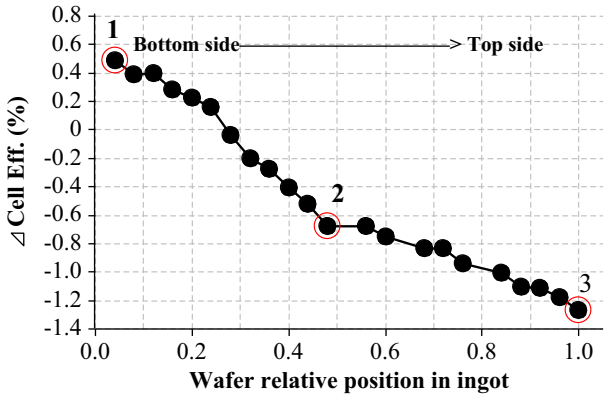

Fig. 4. Cell efficiency trend chart of one mono-like silicon block (from bottom to top).

and bottom wafer was nearly 2%. We can conclude that low-efficiency solar cells (in Fig. 3) are mainly made by wafers from the top side of the ingot from the efficiency trend chart.

Generally speaking, the performance of multi-poly silicon solar cell was affected significantly by the grain boundaries and the dislocation defects of the wafers compared with CZ silicon wafers. In order to trace the low-efficiency tail in the ingot efficiency distribution and to investigate what have degraded mono-like silicon's cell efficiency performance along the crystal growth direction, some experiments of detailed PL imaging and dislocation etching of the mono-like silicon wafers from bottom, middle and top side of one block were performed and EBSD characterization of the grain boundary and grain boundary angle of the bottom and top wafers were also investigated.

Fig. 5 showed the PL images of the as-cut wafers neighboring to cells marked with “1”, “2” and “3” in Fig. 4, which were respectively from the bottom, middle and top side of one mono-like silicon block. Fig. 6 showed the PL images of the cells marked with “1”, “2” and “3” in Fig. 4.

From these PL images, we can find that the pattern of RAN defects nearly do not change in the wafers after they are made into solar cells. That means RAN defects are still strong recombination active after the thermal annealing in solar cell processing. And the trend of RAN defects pattern in wafers and cells were same from bottom to top side of the block. It could also be found that the fraction of RAN defects increased visibly along the mono-like silicon crystal growth direction, and the fraction of RAN defects

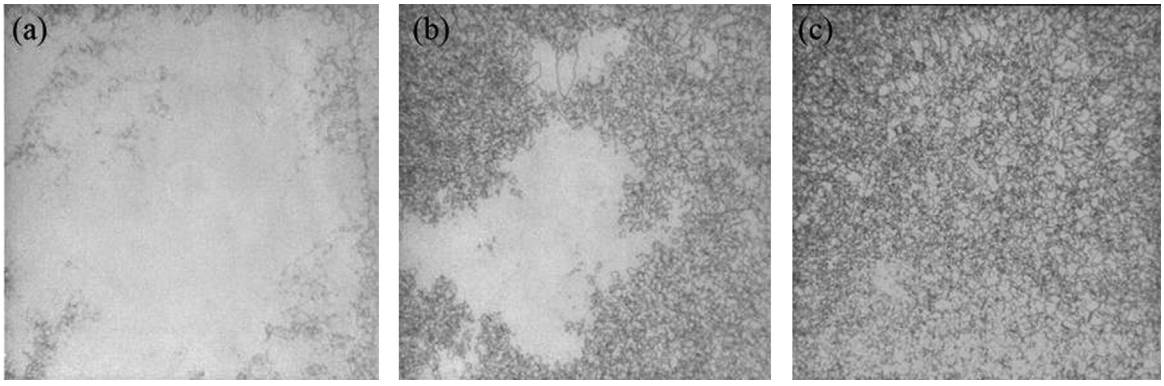

Fig. 5. PL images of as-cut wafers from the bottom to the top of one brick: (a) bottom Wafer 1, (b) middle wafer 2 and (c) top wafer 3, (Wafer 1, 2 and 3 are marked in Fig. 4).

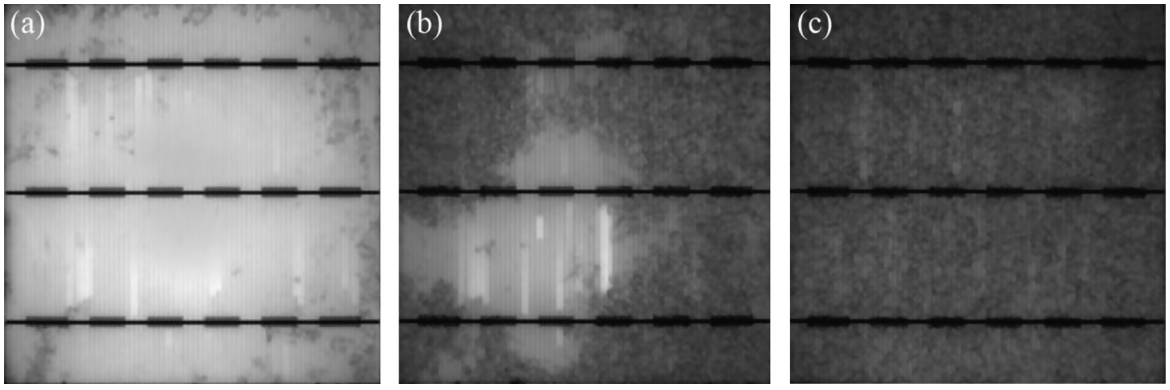

Fig. 6. PL images of solar cells from the bottom to the top of one brick: (a) bottom Wafer 1, (b) middle wafer 2 and (c) top wafer 3, (Wafer 1, 2 and 3 are marked in Fig. 4).

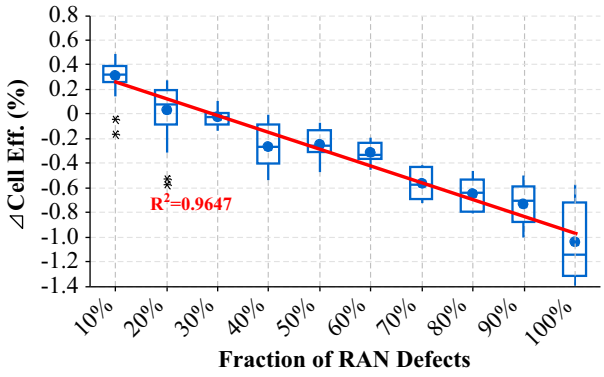

Fig. 7. Relationship between cell efficiency and the fraction of RAN defects.

of the bottom wafer in Fig. 5(a) was less than 10% area while the fraction of RAN defects in top wafer (Fig. 5(c)) was nearly 100% area. This means that density of RAN defects in wafers increases rapidly from bottom to top side of the silicon block. In Fig. 7, we calculated the fraction or density of RAN defects in all the wafers, and gave a correlation of RAN defects density in as-cut wafers and their average cell efficiency. The analysis revealed a good linear correlation of the fraction of RAN defects versus the average cell efficiency with a high correlation coefficient of $R^2=0.9647$. The density of RAN defects became higher and higher along the crystal growth direction of the block. And the average cell efficiency became lower and lower along the crystal growth direction. That means higher density RAN defects will degrade the solar cell efficiency performance. The good consistency of the correlation between the fraction of RAN defects and the average conversion efficiency tell that higher recombination active defects' density will lead to lower cell efficiency.

To investigate the detail of RAN defects, EBSD and dislocation etching were applied in the experiments. In EBSD investigation, we found a large amount of low angle grain boundaries in the top wafer and the length density of grain boundaries is about 2.0×10^3 mm/mm^2. It is also shown that all the detected grain boundary angles are less than 10°. Little density of low angle grain boundary is detected in the bottom wafers. From those facts, we concluded that the detected grain boundaries in the mono-like wafers were low angle grain boundaries and there are much more low angle boundaries in the top wafers than in bottom wafers.

Dislocations slipped and multiplied rapidly in the ingot casting thermal process once they formed. Movement and aggregation of large density of dislocations formed large density of low angle grain boundaries. These low angle grain boundaries formed some sub-grains in the wafers, which are not visible with naked eyes. To investigate the relationship of dislocations, low angle grain boundaries and RAN defects found in PL images, we make a detailed defect etching analysis and investigation. Firstly, high-solution images for top and bottom wafers were taken by PL machine. Secondly, RAN defect regions in the top wafer and non-RAN defect regions in the bottom wafer were sliced into small pieces for selective etching examination. Finally, their defects mapping were constructed after etching in sirtl solution and photographing by optical microscope.

In Fig. 8, we showed a relationship of dislocation etch pits and RAN defects in PL images. Fig. 8(a) gave a PL image which contained the distribution of RAN defects in the top wafer of the silicon block. In Fig. 8(b), etched dislocation mapping was shown, which pattern matched well with mapping of RAN defects in Fig. 8 (a). Fig. 8(c) and (d) were detailed pattern of RAN defects by etching and microscopy. As shown in Fig. 8(c) and (d), we found that distribution of low angle grain boundaries corresponded very well to RAN defects in Fig. 8(a) PL images. Also, there were lots of

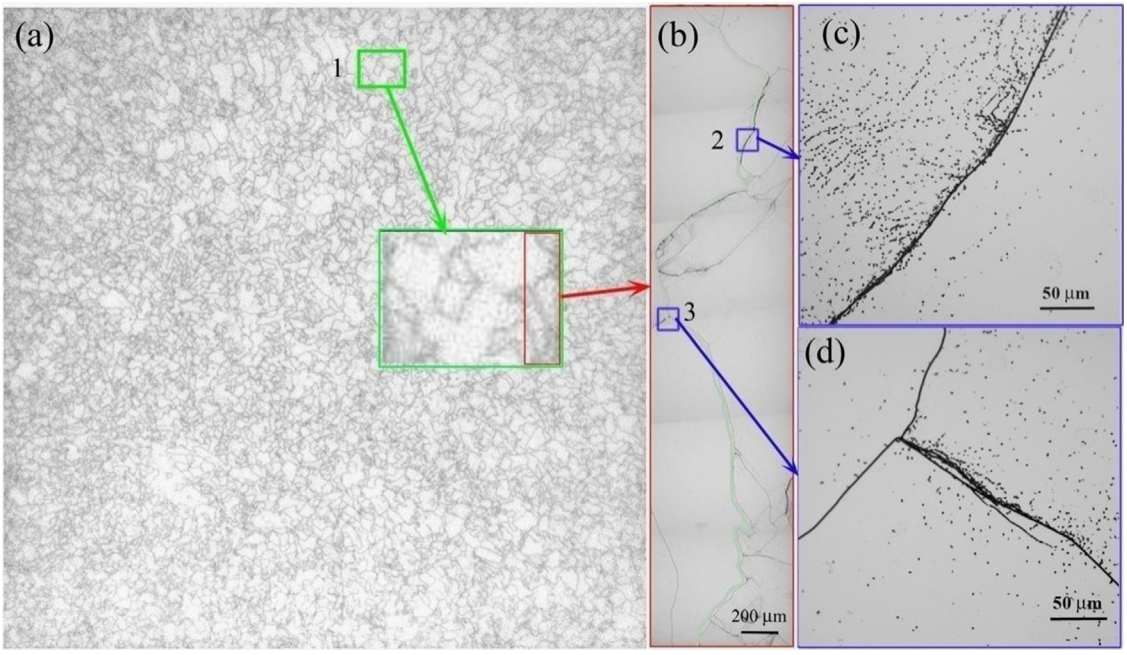

Fig. 8. (a) PL image and (b) grain boundary etch profile of top wafer (c), (d) Dislocation etch pits of top wafer.

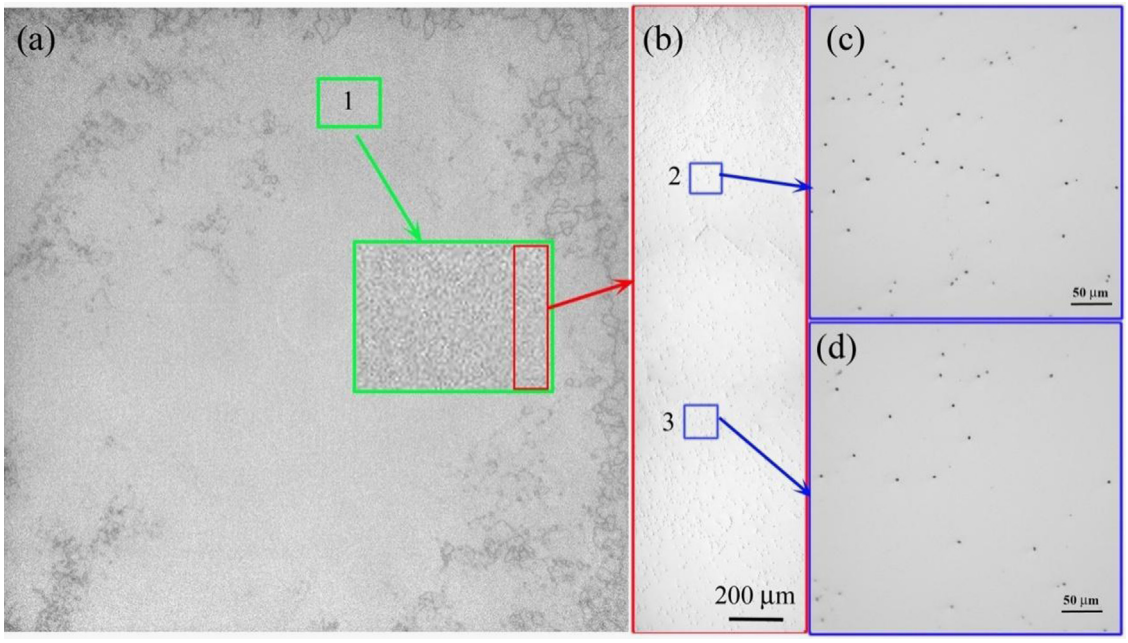

Fig. 9. (a) PL image and (b) grain boundary etch profile of bottom wafer (c), (d) Grain boundary and dislocation etch pits of bottom wafer.

dislocation etch pits detected in Fig. 8(c) and (d). It meant that lots of dislocation clusters aggregated around the low angle grain boundaries. Compared with the top wafer's dislocation distribution, the dislocation map of the bottom wafer shown in Fig. 9 were obviously different. We found that there were only several dislocation etch-pits existed in the “clean” area of bottom wafer, where there were no RAN defects found.

Then, it can be concluded that the RAN defects in PL images of the as-cut wafers were mainly caused by high density low angle boundaries and dislocations. And top wafers had much denser low angle grain boundaries and dislocations than bottom wafers in one ingot.

From above experiment results, we found that little dislocations form in the early phase of grains growth. Slip, increment and interaction of dislocations happen and go quickly during the directional solidification process. Then, a mess of defects network form in the latter duration of ingot growth process. Some dislocations aggregate together and form lots of low angle grain boundaries, which are shown in etching and microscope images. For large density of dislocations do great harm to cell performance, especially for cell electrical parameters, then, for mono-like top wafers, large density of low angle grain boundaries and dislocations degrade their cell performance. The long low-efficiency tail in Fig. 3 is mainly caused by the top wafers' low efficiency

performance of the mono-like silicon ingot. To control the increment and growth speed of dislocations and low angle grain boundaries, will eliminate the low-efficiency long tail in mono-like silicon ingot, optimize the cell efficiency distribution and do great favors to elevate the average cell efficiency performance of the whole mono-like silicon ingot.

4. Conclusions

In this paper, we have examined the efficiency distribution of mono-like ingot and gave an explanation for the long low-efficiency tail in mono-like silicon ingot. Several experiments have applied to prove that cell efficiency performance decreased along the ingot growth direction, and low efficiency wafers are mainly from top-side of each block in the ingot. It was also found that a special denser dark-line pattern, named RAN defects, appeared with the growth of the mono-like silicon crystal ingot. In addition, the relationship of RAN defects density and cell efficiency was calculated, and higher density of RAN defects will lead to much lower cell efficiency.

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