

Review article

Detailed review on c-Si/a-Si:H heterojunction solar cells in perspective of experimental and simulation



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ABSTRACT

The crystalline silicon (c-Si) based photovoltaic (PV) technology is most dominated among other PV technologies. The world record highest efficiency of 26.7% and 26.1% on n & p-type c-Si have been reported with interdigitated back contact- Si heterojunction (IBC-SHJ) design respectively. The c-Si PV technology has potential to reach the theoretical single junction limit of 29.4%. This paper presents the detailed review on experimental and simulation evolutions of high-efficiency c-Si/a-Si:H heterojunction solar cells (HJSCs). Different Si based PV technologies like IBC-SHJ, passivated emitted rear contact, passivated emitted rear local and total diffused contact, aluminum-back surface field, tunnel oxide passivating contacts and finally dopant free carrier selective contact solar cells (SCs) have also been reviewed. Later, developments on simulation studies of HJSCs have been discussed. Several simulation tools have been developed to design SHJ SC structures and understand the performance of different parameters on SHJ SCs. Simulated high efficiency of 27% was reported by modifying thickness of various layers of bifacial SHJ SCs. An efficiency of 27.2%, 24% and 25% obtained for IBC-SHJ, TOPCon and hole selective (MoO_x) SCs using simulation respectively. These results are closely comparable with experimental values. Finally, challenges and future directions to improve the performance of the SHJ SCs are discussed.

1. Introduction

Solar photovoltaic energy is most important power source in coming years due to forceful, extreme and rigorous transformations in geographical and environmental circumstances. Solar renewable energy is expected to address the human need of electricity because of detrimental of the resources for other energy technologies. A solar cell (SC) is a simple p-n junction diode, which converts the optical energy directly into electrical energy by photovoltaic effect. In 1839, Edmund Bequerel has reported the photovoltaic effect [1]. The main operating principle of SCs is (i) generation of electron–hole pairs, that is generating the free charge carriers by absorbing the photons in the semiconductor materials, (ii) these generated electron-hole pairs were separated by internal electric field and (iii) finally, collection of the free charge carriers in order to produce electricity.

Photovoltaic (PV) technology is classified into two categories mainly wafer based and thin film SCs. In the wafer based SCs, crystalline/poly silicon wafers are used for fabrication of SCs. Thin film SCs divided into Cadmium Telluride (CdTe), Copper Indium Gallium Selenide (CIGS) and

thin film silicon SCs. Other new technologies like Dye sensitized solar cell (DSSC), Organic photovoltaic (OPV) and Perovskite SCs are being developed. The main drawback of these new technologies are material instability, difficulties in fabrication of SCs in large area and processing of different layers. Limited availability of material and toxicity are main issues in CdTe and CIGS SCs. The silicon based SCs have tremendous advantages over other PV technologies due to stability, durability, abundance, low fabrication temperature and large area with high efficiency.

Fig. 1 shows the reported world best efficiencies of SCs with different materials and technology by various research groups. Many research groups are focused on increasing the efficiency of different type of SCs and decreasing the cost, time and utilization of raw material. Development of solar cell efficiency of mono and multi c-Si SCs shown in Fig. 2. It is observed that the growth of silicon SCs is increasing constantly. Fig. 3 shows the annual production of PV power by different regions in the last ten years. The global annual PV production is dominated by China about 70% share of market in 2020 and PV technology and production is growing steadily in other countries as well in recent years [4].

Abbreviations: c-Si, Crystalline Silicon; a-Si:H, Hydrogenated amorphous silicon; SCs, Solar Cells; HJSCs, Heterojunction solar cells; PV, Photovoltaics.

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Fig. 4 shows the annual cumulative installation of PV capacity by different regions in the last ten years. (See Table 1.)

For decades, crystalline silicon SCs have dominated the solar photovoltaic market. The reasonable explanation for this supremacy is because c-Si modules have experienced a cost digression of around 24% each year for over 30 years [3]. This significant cost reduction is based on the lowering of material costs, silicon wafer processing and module manufacturing and steady state rise in throughput of production tools. The increase in solar cell efficiency is another aspect that has contributed to a drop in module prices and system costs. Because of many system expenses are related to area, mounting and cabling. Modules with more power result in reduced system costs which results in a lower levelized cost of electricity (LCOE) [3]. In addition to financial concerns, the sustainable use of resources is a crucial reason for higher-efficiency SCs. More efficient SCs make better utilization of available space like roof tops areas, on sea or stable water, on vehicles and on the components system.

The silicon heterojunction (SHJ) SCs were produced by using hydrogenated amorphous Si (a-Si:H) and the crystalline silicon (c-Si) absorber provides and gives the best efficiency for silicon wafer-based photovoltaics [5,6]. Si wafer-based solar cell technology, which clearly dominates photovoltaic (PV) markets and high-volume manufacturing such as wafer texturing and cleaning, metallization, and module integration. The silicon thin film solar cell technology offers expertise for high-volume thin film deposition and in-depth knowledge regarding engineering of the transparent, conductive metal oxides, and Si thin film stacks, which forms the passivating contacts of the wafer-based SHJ SCs. Efficiency limitations of silicon thin film SCs are frequently attributed to the quality of the silicon thin film absorber [7].

The silicon heterojunction (SHJ) SCs shown tremendous results to get rid of the efficiency restrictions of the SCs developed by homojunction methods and thus further pushed silicon solar cell efficiency to its maximum theoretical limits [6–9]. However, several parameters gating silicon heterojunction SCs such as optical and electrical properties of the few nano-meter thick doped and un-doped silicon thin films and the anti-reflective, transparent and conductive metal oxide layers and also metal contact layers. Since the SHJ cells were processed around

200 °C, the electrical quality of the c-Si absorber was improved and deteriorated by the dependence of un-doped a-Si:H layer and also cleaning of c-Si wafers [10]. There are several restrictions on screen printing metal contacts and curing at high temperatures. Furthermore, surface of the c-Si, interface qualities and the opto-electronic contact qualities must be taken into consideration for large area fabrication. SHJ devices with incorporated ITO may be threatened by the production scarcity, potential supply shocks, and the relative scarcity of indium in the earth's crust in order to meet the challenges faced by the increasing expansion of the PV industry towards higher scale production [11,12]. To address the anticipated future market demand for PV, indium-free SHJ and comparable cell topologies are consequently having significant interest. Additionally, it is a general requirement for the c-Si community as a whole to significantly reduce or completely eliminate Ag use in PV manufacture[13]. In order to decrease of Ag usage, development of bifacial and interdigitated designs is required, which also gather light from both sides of the absorber and may increase energy yield while decreasing leveled cost of energy for a particular installation [11,12,14]. In addition to these possible limitations, wide bandgap metal oxides can be used in place of the doped silicon layers to further reduce parasitic absorption in passivating contact devices. Process and patterning simplification is crucial for becoming an industrial reality of IBC-SHJ SCs. Interesting new approaches can be developed to this aim, enabling bottom-up concepts like the tunnel-junction IBC cell.

Indium-tin oxide (ITO) is the most commonly employed as a transparent conductive oxide layer (TCO) for SHJ SCs. Another use of ITO is conduction of charge carriers in lateral direction through the ITO layer. These ITO layers also act as an anti-reflection coating on top of amorphous silicon layers, particularly on the front surface of the SHJ SCs. ITO layers may also be used as transport interlayers between the top and bottom cells in tandem devices for some newly developed solar cell technologies [13]. These layers enable necessary lateral conduction and the formation of high-quality ohmic contacts with metal electrodes at both the front and rear metal contacts. Some of commercial Si-based SCs like Al-BSF, PERC, and TOPCon SCs don't require much of ITO layers since the lateral conductivity of the doped silicon layers or bulk with boron or phosphorus as dopants is adequate [11,13]. Therefore, indium

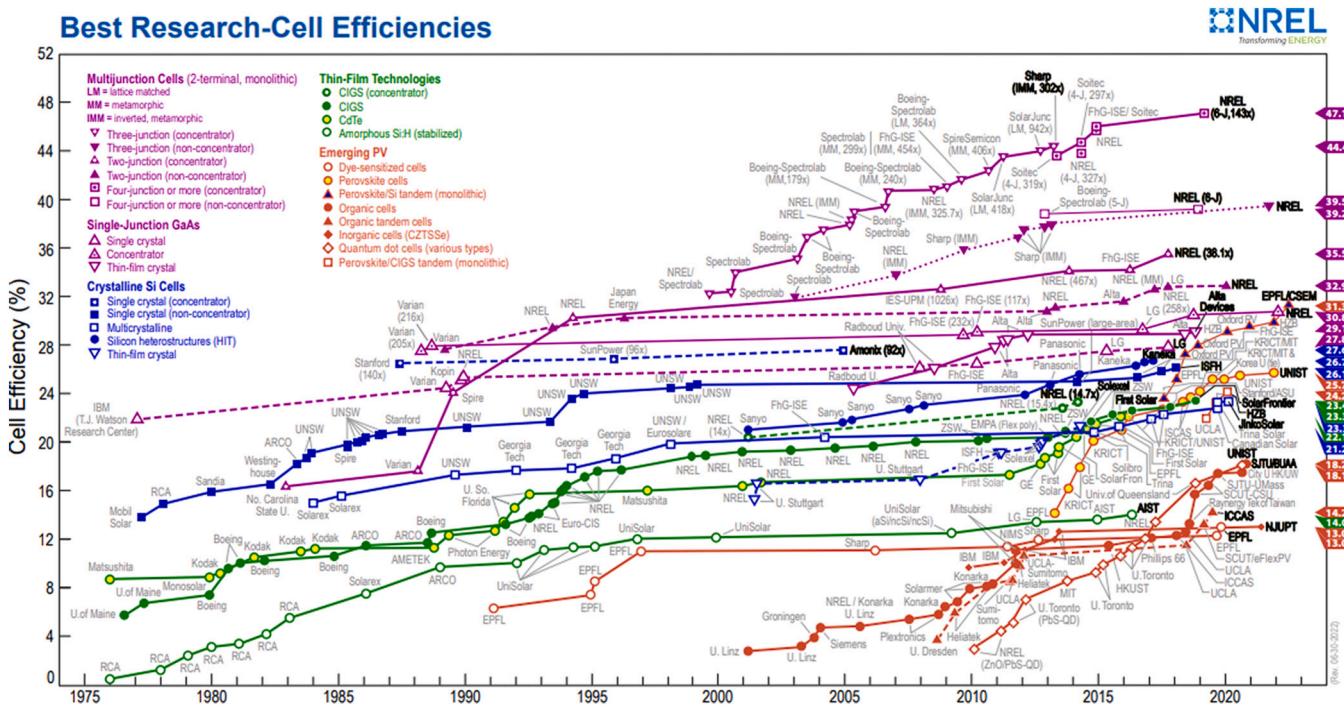


Fig. 1. Best solar cell efficiency with different materials and technology by different groups [2].

is not much important for either the established PERC or the TOPCon solar cell technologies and SiN_x layers have been using instead of ITO layers. Indium based alloys have also been utilized for connecting technologies like Smart-Wire and low-temperature soldering. However, Indium was slowly replaced by Bismuth because of the latter's high cost and scarcity [11,13]. In SHJ SCs, thin TCO layers are generally formed with ITO layer (80-100 nm) thick by sputtering. Generally, 5.7 mg/W of ITO and 4.2 mg/W of Indium is consuming for anticipated cell efficiency of 25%, considering density of ITO with 90% of In_2O_3 weight content [11,12]. The function of ITO as lateral transport and anti-reflection coating layers would be significantly impacted by the limitations of the allowable thickness of ITO layers for the terawatt scale [15]. In order to maintain the same lateral conductivity of thick ITO layer for thinner ITO layers, the sheet resistance should be decreased for several orders. Conductivity of the ITO layers can be enhanced by raising the carrier density. However, this will have a negative impact on optical characteristics due to an increase in parasitic IR light absorption [16,17]. In addition, in some circumstances where a reduced parasitic absorption of IR light is also observed due to the improved carrier mobility, indium oxide layers doped with tungsten (IWO), cerium (ICO), or hydrogen (IO: H) could be used for improved sheet resistance of those layers compared to conventional ITO layers, leading to improvements in the IR light management and increases in short-circuit current density [16]. Utilizing multi-layered anti-reflection coatings such as SiO_x , SiNx , or MgF_2 on top of very thin ITO layers for anti-reflection purpose might boost the sustainable production capacity [11]. The cost and complexity of the cell production process might be rise with the addition of any new layers and procedures. The usage of indium-free TCO layers must be further investigated in order to entirely overcome the constraints imposed by the indium supply in order to allow sustainable manufacture of SHJ SCs and future tandem devices at the terawatt scale [11]. Aluminum doped zinc oxide (AZO) is one of the considerable materials, due to its low cost, abundant supply of raw materials, and capacity to achieve efficiencies equal to those of ITO-based SHJ SCs. However, the relatively low conductivity and long-term stability of AZO layers still require a great amount of work to combat. In order to replace interlayers in future tandem devices as well as for SHJ SCs, it is crucial to speed the development and implementation of indium-free TCO layers. The lower soldering temperature also has the benefit of minimizing busbar and ribbon thermal mismatch damage, which is especially advantageous for SCs with bigger and thinner silicon wafers. Aluminum-doped ZnO (AZO) has been gaining interest as TCO layer for SCs due outstanding properties like high chemical stability in hydrogen plasma process than ITO and

good electrical properties and high bandgap of 3.4 eV [18]. These AZO films were deposited by variety of methods such as sputtering, atomic layer deposition (ALD), pulsed laser deposition (PLD), spray pyrolysis, sol-gel, electro-deposition and chemical vapor deposition (CVD) [12,19,20]. Among all these techniques, sputtering is most commonly used for deposition of AZO films. Better transmission properties of AZO films were obtained due to the formation of crater-like structures by self-texturing mechanism without any external thermal/chemical processes were obtained by deposition with suitable conditions [18]. Multilayers of AZO/Cu/AZO were deposited by sputtering studied varying thickness of Cu and annealing temperature and observed that this structures could be suitable as TCO for SCs in the range of visible and NIR at low temperature [21]. Multilayer of AZO/Cu/Ag/AZO were deposited at room temperature to develop indium-free TCO layer by sputtering. The best Fig. of merit of $3.8 \times 10^{-2} \Omega^{-1}$, sheet resistance of $9.9 \Omega/\text{sq}$ and transmission of 90% (400–800 nm) was obtained for the AZO/Cu/Ag/ AZO films with the 0.1 and 7 nm-thick Cu and Ag layer respectively [22]. The AZO capping layer of the silver nanowires has enhanced the optical transmittance in the visible-near IR range and reported that suitable TCO layer for solar photovoltaics[23]. Transmission, electron mobility and bandgap of ZnO and AZO films has increased as increase in hydrogen dilution of the films, which results in suitable opto-electronic properties as TCO layer [24]. An alternatively, Mg and F co-doped ZnO (MFZO) thin films deposited by sputtering techniques and obtained crater-like texture by etching of MFZO films with HCl to get TCO properties [25].

Silver has been using in industrial silicon solar cell technologies to form metal connections to collect photo-generated electron-hole pairs from the SCs. Screen-printing of silver paste is standard metallization method, which used to make the metal contacts in all major PV technologies. However, the price of SCs is increasing due to huge consumption of Ag to make metal contacts. The rear side of PERC and Al-BSF SCs' fingers and busbars are made of less expensive, more readily available aluminum. In this case, aluminum-silicon interactions are exploited to create an advantageous aluminum back-surface field (Al-BSF) at the contacted areas [26–28]. The limitations of the metal covering area for optical shading are relaxed as a result of a decreased incoming illumination intensity on the back surface. Consequently, to make up for aluminum's weaker conductivity (35-50 Ωcm) than silver (5-10 Ωcm), significantly larger and closer-spaced aluminum fingers may be utilized with bi-facial PERC SCs have an aluminum consumption of 200 mg [3,16]. However, more silver is needed to build soldering pads on the back side for connectivity since it is difficult to solder to

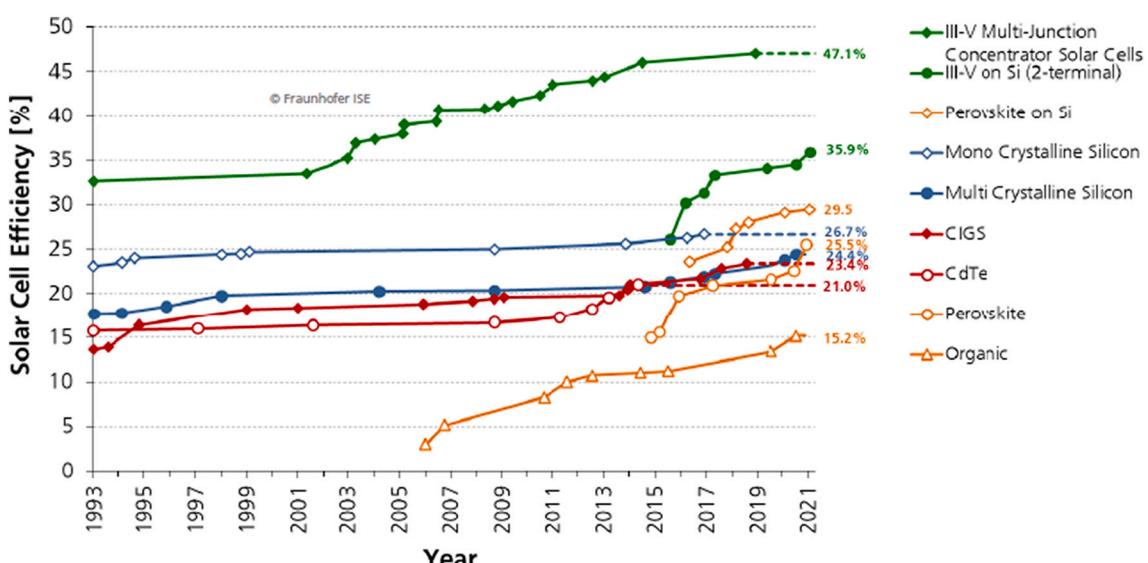


Fig. 2. Development of solar cell efficiency of c-Si SCs [2,3]

aluminum [11]. Silver pastes are applied to the front and back surfaces of industrial n-type TOPCon, PERL/PERT, SHJ and carrier selective SHJ SCs, resulting in a significantly greater silver consumption than PERC and Al-BSF. On the front, an Ag/Al paste is used to ensure the formation of high-quality ohmic contacts with the p-type emitters while also enabling sufficient conductivity in fingers and busbars with a line resistivity of 5–10 Ω·cm to avoid excessive shading and resistive losses [11]. Processing for SHJ SCs is normally restricted to temperatures below 200 °C to prevent a substantial degradation of surface passivation quality that can occur at higher temperatures [11]. As a result, the front and rear contacts of SHJ SCs need to be coated with a low-temperature silver paste that cures around 150–200 °C. In order to assure the appropriate creation and curing of contacts at low temperatures, SHJ silver pastes contain more silver particles and various solvents, additives, and curing agents than standard silver pastes due to low curing temperatures [29–31]. Low-temperature silver pastes for SHJ SCs typically have line resistivity in the range of 10–20 Ω·cm, which is about two times higher than the line resistivity of the high-temperature silver pastes that are typically used for PERC and TOPCon SCs [28,32–34].

To enable sustainable manufacturing at the terawatt scale, novel screen-printing methods to reduce silver consumption as well as alternative silver-free metallization and interconnection technologies must be developed and deployed as early as possible. When silver consumption is carefully controlled, fewer busbars will be needed to construct fingers, which might actually result in reduced finger resistance. Additionally, by lowering the number of busbars, the maximum permitted finger cross-sectional area will also be raised, which enhances the dependability and printability of such fingers in the context of mass production [11,16]. When moving toward more environmental friendly solar cell production techniques for screen-printed SCs, the physical limits on the finger dimension and shape must be taken into consideration to enable a workable and practical reduction in the consumption of silver in fingers. In order to decrease the amount of silver used in traditional busbar and tabbing zones, non-silver busbars (like Al or Cu) or busbar-less technologies need to be developed and used [35]. To speed the reduction of silver consumption in fingers and enable a total silver consumption below 5 mg/W or even 2 mg/W, alternative materials or finger geometry and pattern must be created [36]. One option is to create metal-silicon interface sections using a print-on-print technique with a seed layer of a silver paste, topped by a non-silver conductor. Copper plating is a different way to reduce silver consumption that the PV industry has to take seriously for both present and future technologies [35,37]. It is particularly significant for today's growing industrial SCs with passivated contacts, such as TOPCon and SHJ, that

plating has also been effectively used for SCs with such connections. Along with improvement in PV technologies, the industry is also paying more attention to innovative connectivity strategies and module technologies like SmartWire, half-cells, and shingled modules, which have been created to increase the efficiency and output power at the module level [38–40]. A reduced finger silver consumption or an increase in finger resistivity for the use of alternative materials (such Al or Cu) may be more tolerable thanks to the additional wires that are frequently included in the SmartWire configuration, without significantly increasing finger resistance losses [11,16]. Other than Ag screen printing technology, Cu plating, roll to roll printing, inkjet printing, direct printing, sputtering and Ni/Cu electroplating techniques have been developing for busbars and finger contacts of SCs. Al, Ni, Cu, Pt and their alloys like Ag/Al, Cu/Ni and Ag/Al/Pt are also using in screen printing.

2. Fabrication details of c-Si/a-Si:H HJSCs and materials

In this session, deposition of intrinsic/doped films, TCO and metals, fabrication techniques of different PV technologies and characterization techniques are discussed.

2.1. Deposition of thin films and SCs

Several deposition techniques have been developed to prepare amorphous silicon films and its alloys such as Pulsed laser deposition (PLD), Remote plasma chemical vapor deposition (RPCVD), Very high frequency PECVD (VHFPECVD), Hot wire CVD (HWCVD) and Radio frequency PECVD (RFPECVD), LPCVD [41,42]. Among all, RFPECVD is the most promising and widely used for the preparation of amorphous silicon films as well as SCs. The scientific community has adapted a standard RF frequency of 13.56 MHz for this technique which is also used for industrial applications. The advantage of this technique is that high quality films are deposited uniformly over a large area at low substrate temperature. The transparent conducting oxides i.e Indium tin oxide (ITO), Zinc oxide (ZnO) and Aluminium doped zinc oxide (AZO) thin films were deposited by RF sputtering technique [43,44]. Finally, metal electrodes are deposited on front and back by evaporation/screen printing techniques and then fired for reducing resistance losses.

2.1.1. Growth mechanism of a-Si:H thin films

Fig. 5. show the schematic diagram and main possible chemical reactions of growth mechanism of a-Si:H films. A number of gas species like SiH₃, SiH₂, SiH, Si, H₂ and H are released during the deposition of a-Si:H films, which undergo secondary reactions mainly with SiH₄

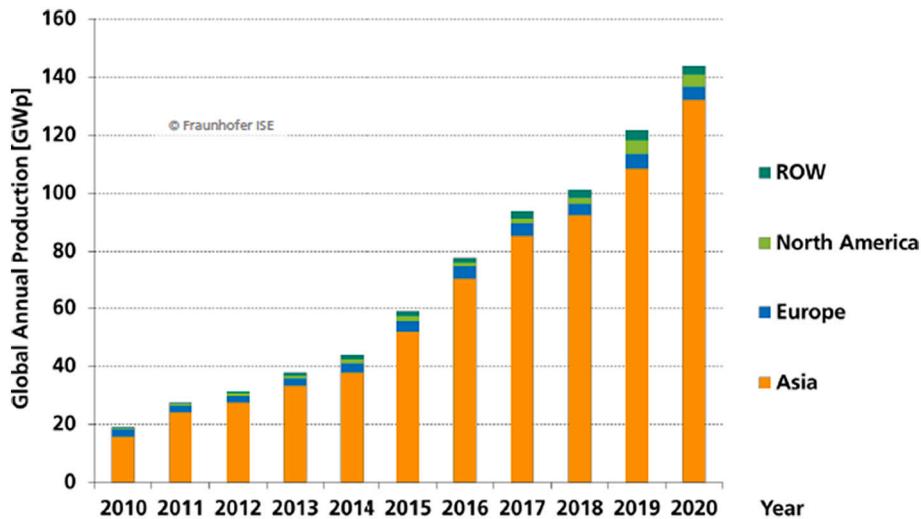


Fig. 3. PV industry global annual production by different region in recent years [3].

molecules, forming a steady state [45,46]. The grown film contains the strongly bonded Si-Si and Si-H as well as weak Si-H₂ bonds, trap centres and also defect density of states (dangling bonds) [45]. SiH₃ is the main precursor for deposition of a-Si:H films. It has sticking coefficient of 0.1 and these precursors experience many reactions during film growth, such as desorption of SiH₃ radicals, recombination with another SiH₃ radical and abstraction of hydrogen atom [47,48]. This SiH₃ radical abstracts one hydrogen atom and produces a SiH₄ molecules and leaves surface dangling bonds, which interacts with next SiH₃ radical. This results in growth of a-Si:H films.

2.1.2. Fabrication of SCs

Czochralski (CZ) and Float Zone (FZ) c-Si wafers with good quality and minority carrier lifetimes have been used for the fabrication of c-Si/a-Si:H HJSCs. Alkaline etchants, such as NaOH, KOH, or (CH₃)₄NOH, are used to texture the wafers. After texturing, wafers were cleaned by standard RCA-1 and RCA-2 processes and sequentially removed Si surface oxides with HF solution [49,50]. After cleaning, wafers were dried and then immediately loaded in deposition chamber. Fig. 6 (a, b) shows the schematic diagram of fabrication process steps and schematic structure of SHJ-HIT SCs with approximate thickness of each layer.

2.2. Characterization techniques

Raman spectroscopy is widely practiced to explore the microstructure and bonding modes in a-Si:H thin films. Medium and short range order of Si network, bond angle-deviations, crystalline, nano crystalline, grain boundary volume fractions and mean crystallite size were estimated by analyzing Raman spectra of Si films [51–54]. Transmission electron microscopy (TEM/ HRTEM) measurements were carried out to evaluate the structure, crystallinity, lattice spacing of planes of the films [44]. The X-ray diffraction system is used for determination of structure, size of crystallites and micro-strain of the TCO materials [55–57].

Spectroscopic ellipsometry (SE) is a highly accurate, non-destructive and optical technique to investigate the optical, structural properties, and to estimate the thickness, band gap, refractive index and surface roughness of the thin films. The main feature of SE is that it measures the change in polarization state of light upon reflection from the sample [58]. The dielectric constants, thickness and optical band gap of the films are deduced from measured (ψ , Δ) values as a function of energy or wavelength applying suitable optical models using single or multi-layer structures. Several models like Tauc-Lorentz (TL) [58–60], Cody-Lorentz (CL) [61], Lorentz, Gauss [62], Forouhi-Bloomer (FB), Modified Forouhi-Bloomer [63,64], Harmonic oscillator [62], Tetrahedral model [65] and Bruggeman effective medium approximation (BEMA) [62] etc. are available for evaluation of a-Si:H films. Combination of

Tauc-Lorentz model, Gauss and BEMA methods have been applied for estimation of the optical constants, thickness and fraction of voids, amorphous and crystalline parts of the films [62,66–69].

Fourier transform infrared spectroscopy (FTIR) is used to estimate nature of chemical bonding and compositional analysis of material. FTIR has been practiced to estimation of the hydrogen contents and micro-structure of the a-Si:H films [41,44,70–78]. The UV-Vis-NIR spectroscopy was employed to calculate thickness, bandgap and refractive index of thin films with swanepoel's method for reasonable thick samples [79] and optical band gap is incurred from the Tauc's graph [80–82]. The field emission scanning electron microscope (FESEM) and Atomic force microscope (AFM) techniques were employed on films to study the morphology and surface roughness [83].

The conductivity, photosensitivity of a-Si:H films, sheet resistance and resistivity of ITO thin films were determined using *I-V* measurements [41]. The SC parameters were measured by *I-V* curve under AM1.5 conditions with 100 mW/cm² of incident power density [42,84,85]. Spectral response, passivation quality of interfaces and reflection losses of SCs were studied by external quantum efficiency (EQE) and internal quantum efficiency (IQE) measurements with and without external reverse bias conditions [42,84]. The incident light intensity- V_{oc} (Suns- V_{oc}), Photo conductance decay (PCD) and Quasi-steady-state photo conductance (QSSPC) are very important measurement for Si based SCs. Junction properties, passivation quality can be estimated by finding minority lifetime using Suns- V_{oc} , PCD and QSSPC techniques [86,87].

3. Developments on c-Si/a-Si:H HJSCs

3.1. Development of silicon photovoltaic technology

Silicon based SCs (SCs) are mainly carved up into two categories: crystalline silicon (c-Si) and thin film silicon based SCs. The c-Si SCs are further divided into subcategories as per crystallinity and crystal size resulting in single crystalline wafers, multi-crystalline wafers, ribbons based SCs. Thin film silicon SCs are divided into two categories based on different active absorber material, which are hydrogenated amorphous silicon (a-Si:H), hydrogenated microcrystalline silicon (μ c-Si:H) and Si alloy materials. In 1954, Bell laboratory announced first c-Si SCs were fabricated by Bell laboratory and achieved an efficiency of 6% [88,89]. Since then there is a steady increase in efficiency, current highest efficiency is 26.7% [90–92]. The c-Si based PV technology is ruling the world with market share of 95% in the nowadays and potential to dominate in the upcoming years also due to remarkable properties of Si such as long enduringness, stabilization, abundant, environmental friendly and high efficiencies, whereas, other thin films PV technology is

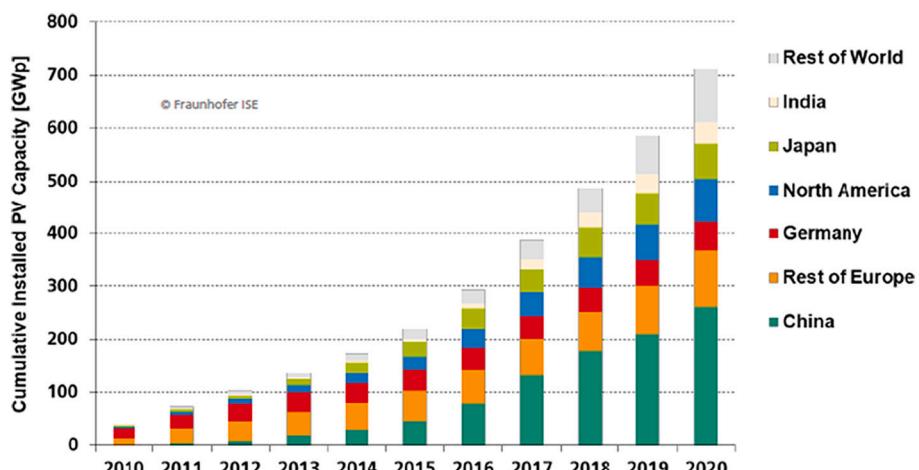
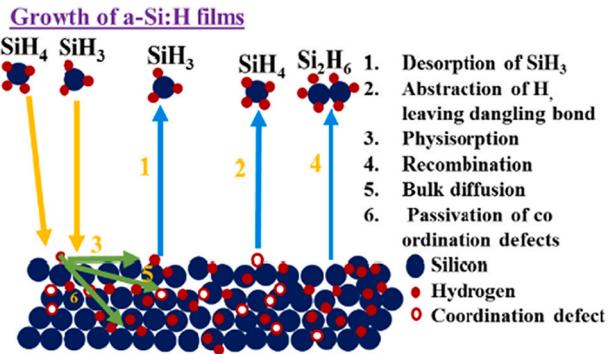


Fig. 4. PV industry global cumulative installed PV capacity by different region in the recent years [3].

Table 1

Reported few results of c-Si/a-Si:H HJSCs on c-Si wafers.

Research group	η (%)	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF	Area (cm ²) (description)	Year	Ref.
1 Kaneka, Japan	26.7	738	42.6	0.85	79(IBC-SHJ)	2018	[8]
2 Kaneka, Japan	26.6	738	42.6	0.85	180 (IBC-SHJ)	2018	[8]
3 ISFH, Germany	26.1	726	42.6	0.84	4 (IBC-POLO)(p-type)	2018	[174]
4 FhG-ISE, Germany	26.0	732	42.1	0.82	4(top/rear contacts)(p-type)	2021	[188]
5 FhG-ISE, Germany	26.0	732	42.0	0.84	4 (TOPCoRE)(p-type)	2022	[12]
6 FhG-ISE, Germany	25.8	724	42.8	0.83	4 (Top/Rear contact)	2017	[189,190]
7 Sanyo, Japan	25.6	740	41.8	0.83	143 (HIT(SHJ))	2014	[98]
8 Hanergy, China	25.1	747	39.6	0.85	244(n-type top/rear contacts)	2020	[162]
9 FhG-ISE, Germany	24.0	714	42.4	0.81	100 (TOPCon)	2017	[141]
10 Sanyo, Japan	24.7	750	39.5	0.83	100 (HIT(SHJ))	2014	[6]

**Fig. 5.** Schematic diagram and possible reactions of growth mechanism of a-Si:H films [45].

around 5% of market share [4] and in this (5%), 0.3% is accounted for a-Si:H thin films based SCs [4] because of high defects density, unstability of materials [41] and low power conversing efficiency of SCs [91].

3.2. Formation and structure of c-Si/a-Si:H HJSCs

Semiconductor heterojunction (HJ) and homo-junction were formed by adding two separate and equal band gap materials respectively [93]. Transport of the electrons from the n-type (light absorbing material) into the p-type material could be minimized by choosing p-type materials with a large bandgap than that of the n-type, which form the band offset at the CB. Due to this band discontinuity, heterojunction allows only e⁻s to n-type and holes to p-type material for transportation and avoids recombination losses [94,95]. This results in effective using of photo-generated carriers and therefore high photo currents from the SCs [10]. Fig. 7 and 8 shows the schematics of band bending and structure of c-Si/a-Si:H HJSCs respectively.

The c-Si/a-Si:H HJSCs offers captivated alternate to homo-junction c-Si based SCs. Fabrication of c-Si/a-Si:H HJSCs were completed at temp. of below 200°C, whereas, conventional c-Si SCs were fabricated by a thermally diffused process around 800-1000 °C [90]. This low temperature processing reduces the wafer size and thermal budgets during the heterojunction formation. This results in reduced wafer bowing and also feasibility of symmetric structures [96]. Less time duration is needed for formation of the HJ and for deposition of contacting layers compared conventional c-Si SCs. The silicon heterojunction (SHJ) SCs exhibit low temperature coefficient than conventional c-Si SCs [97]. In SHJ SCs, improved surface passivation and reduced recombination losses results in high V_{oc} values can be realised as compared to c-Si SCs. The conversion efficiency of c-Si/a-Si:H HJSCs is comparable with c-Si SCs [90,98,99].

3.2.1. Role of intrinsic and doped a-Si:H Layers

Higher quality thin typically around 5 nm a-Si:H(i) films were deposited on c-Si wafer. This thin a-Si:H(i) layer passivates the c-Si

surfaces and forms a high quality interface layer between c-Si and doped a-Si:H layers, which significantly reduces recombination losses at the interfaces [6,100]. The a-Si:H(i) passivating layers shoud have high quantity hydrogen content, epitaxial free grown and good opto-electrical properties. This high quality i-layer can be achieved by higher hydrogen flow rate during the deposition, pre/post hydrogen plasma treatment and hydrogen rich subsequent layer on poor hydrogen content layer. The microstructure and opto-electrical properties of the doped as well intrinsic a-Si:H layers plays a significant role in the performance of these SCs. However, formation of voids and epitaxial layers deteriorate the performance of the SHJ SCs [101,102]. Number of research groups have elaborated the significance of hydrogen in the preparation of a-Si:H and nc-Si:H/ μ c-Si:H networks [45,65,103–106]. Highly stable and lesser defective a-Si:H films can be prepared by adding hydrogen to silane during deposition for SCs. Some of the research groups also passivated c-Si substrate by hydrogen plasma treatment (HPT) before deposition of doped layer to reduce defects/recombination centres/dangling bonds [107–111]. This HPT has not only passivated the defects at the interface but also improved the microstructure of the a-Si:H layers. This improved quality of a-Si:H certainly show better optoelectronic properties and better open circuit voltages (V_{oc}) [108,112–114]. The a-Si:H films have been made shift to near modulation regions of amorphous and nano crystalline phase by HPT, which results in better microstructural properties and also improved performance of SCs [115–119]. It was observed that V_{oc} was significantly improved by HPT on i-layer before deposition of doped layer by breaking weakly bonded Si-Si and Si-H₂ and reforming strongly bonded Si-Si and Si-H [45,65,119]. The Si-H₂ and higher hydride bonds were significantly reduced by incorporation of hydrogen into the silicon network and improves the microstructure of the a-Si:H films [45,120,121]. Hitoshi Sai et.al deposited very thin a-Si:H(i) double layer on c-Si for passivating defected centers, however, lifetime of minority carriers has improved, i.e defect centers/recombination states have been reduced but the performance of SCs was deteriorated due to parasitic absorption and resistance losses due to double intrinsic layer [122]. Liu et studied the tailoring of Si-H bonds by varying optical bandgap and passivation quality [123]. It was also reported that atomic hydrogen widens the optical bandgap and results in superior surface passivation and enhanced performance of the SCs [124,125]. Intrinsic a-Si:H films fabricated near the onset of nano crystalline phase has significantly enhanced the interface quality and suppressed the interface recombination defect centers. This further improves the charge carrier transportation through interfaces [126–129].

The doped a-Si:H(p/n) layers create required band bending for c-Si/a-Si:H HJSCs. These layers reduce re-combination losses by creating sufficient electric field at interface [112,130,131]. The sufficient band bending offers a free transport for one type of charge carriers and blockage for opposite charge carriers. The thickness of the these layers is about 5-6 nm are deposited with sufficient doping by suitable gases (B₂H₆, B(CH₃)₃, PH₃, etc.). The superior properties of a-Si:H(p/n) layers are highly important for enhancing the efficiencies of c-Si/a-Si:H HJSCs, which are showed substantial prognosticating performances

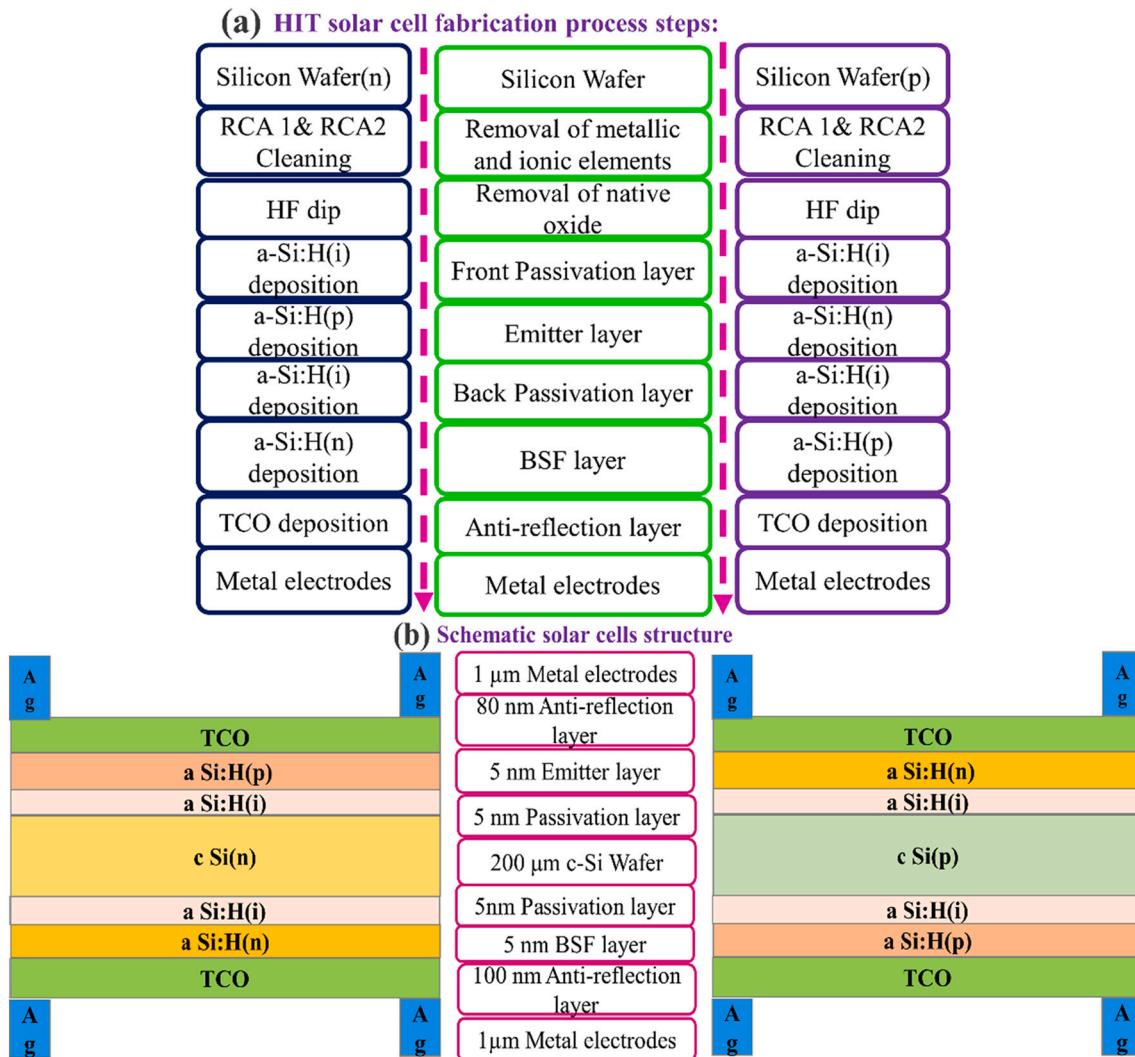


Fig. 6. a) Schematic diagram of process flow: wafers, cleaning, Si layer deposition, ITO and silver contact, b) schematic structure and approximate thickness of each layer of SHJ-HIT SCs.

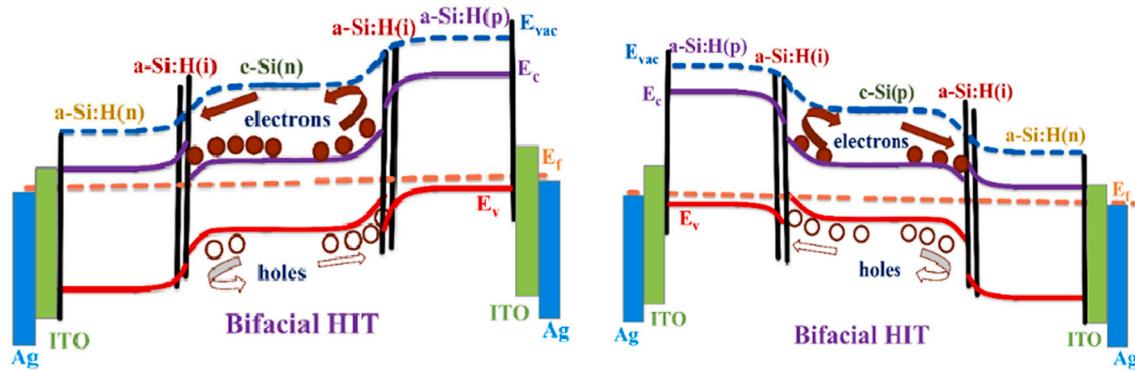


Fig. 7. Schematic band bending diagrams of bifacial c-Si/a-Si:H HJSCs.

[6,96,98,99]. The deposition parameters like process temperature, process pressure, and H_2 & SiH_4 gas flow rate have change the opto-electrical properties of a-Si:H(p/n) films remarkably [97,124,132–135]. There is growing interest in doped mixed phase or nanocrystalline Si and nc-Si_xO_y films as a replacement of doped a-Si:H layers in SHJ SCs [136–138]. These layers are showing beneficial interface properties and opto-electrical properties [139,140]. High band

gap hydrogenated silicon carbide (a-SiC:H) films were prepared by adding carbon atoms in silicon network [125]. These films have also been using to improve the short current density by widening absorption spectra [125]. Few research groups have also demonstrated nc-Si:H/μc-Si:H as emitter layer for HJSCs [140–142].

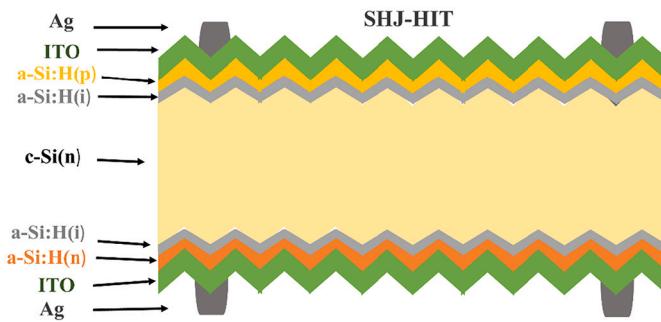


Fig. 8. Schematic diagram of the different layers of SHJ(HIT) SCs.

3.2.2. Role of TCO layers and metal contacts

The transparent conductive oxide (TCO) layers are critical layers to amend the efficiency of SCs. Indium tin oxide (ITO), Zinc oxide (ZnO), Alumina doped zinc oxide (ZnO:Al) are most commonly used TCO layers in SCs [6,7,97]. The TCO layers have significant importance in SCs as antireflection layer and also protect from diffusion of metal particles in to a-Si:H layers and also light transparent layer, conducting layer for charge carries [66,97,98,109]. To improve performances of SC, the primary prerequisites of TCO films are higher bandgap, higher transparency, high conductivity and lower sheet resistance values [7,143–145]. Few researchers incorporated hydrogen into ITO and ZnO network during deposition process for better properties [146,147]. However, properties of TCO layers are affected by deposition conditions [148,149]. These TCO layers were deposited on front emitter and BSF layer by sputtering and thickness is about 80 nm and 120 nm respectively [10]. Finally, metal grid electrodes were made on ITO layers for collection of charge carriers by screen printing method and annealed/fired for reducing resistance losses. Usually, Silver (Ag), Aluminum (Al), Platinum (Pt), Copper (Cu), Gold (Au), Palladium (Pd) and combination of these metals were used for c-Si/a-Si:H HJSCs [7,10,97]. The narrow and less height metal contacts are required to reduce resistance losses and shadowing losses in the SCs [7].

3.2.3. Surface, bulk and interface properties

Surface, bulk and interface layer properties are very crucial for improvement of the performance of the c-Si/a-Si:H HJSCs. Many researchers reported number of studies on interface quality and interface properties by different method/processes, however, till date it is very hot topic to further improve the interface and then performance of the c-Si/a-Si:H HJSCs. The c-Si is main absorber layer in SHJ SCs, so it is very important to use high quality c-Si wafer, which reduce bulk defect density and improve the bulk minority carrier lifetime. Surface defects/dangling bonds were mitigated by superior cleaning process before loading into the deposition chamber [136,137]. Many researchers observed that post deposition annealing around 200 °C has improved the passivation quality. Hydrogen atoms were redistributed into the films as well as the c-Si/a-Si:H interface by annealing. Annealing of the films facilitates breakage of weak bonds and reconstruction of the Si network. Furthermore, annealing in the H₂ atmosphere is improve chemical passivation of surface/bulk and also interfaces. Surface cleaning is very important processing step to suppress surface defects and to deposit higher quality a-Si:H layers. This cleaning process further help to suppress the interface defects after depositing intrinsic and doped a-Si:H layers also. Many researchers have used hydrogen plasma treatment prior and later on deposition of a-Si:H layer to passivate surface, bulk and interfacial defects/dangling bonds [109,150]. Prolonged light exposure induces metastable states (Staebler-Wronski effect) [41], however, this effect is less pronounced for c-Si /a-Si:H SCs due to less thick a-Si:H layers. Abrupt junctions of c-Si/a-Si:H can significantly enhance the charge carrier transport and therefore efficiency of the SHJ SCs. It was reported that interface treatments on a-Si:H(i) layer have

induced nucleation of nano-crystals as well as improved the quality of c-Si passivation [151]. It is highly recommended to reduce interface defect density, control of hetero interface, abrupt junctions, low plasma damage, required band offset for improving V_{oc} and then performance of the c-Si/a-Si:H SHJ SCs.

In 1941, at Bell laboratories, the first SCs have been fabricated by R. S. Ohl based on multi-crystalline silicon formed by directional solidification and obtained less than 1% efficiency [152]. Later, Bell laboratory fabricated the SCs with an efficiency of 4.5% in 1953 [153] and 6% in 1954 [154]. In 1974, at first, Fuhs et.al reported a-Si/c-Si heterojunction [155] and later in 1983, Okuda et.al reported a-Si/poly c-Si HJSC with an efficiency of 12% [156]. In 1992, researcher group at Sanyo have launched new PV technology of c-Si/a-Si:H HJSCs and realised high efficiency of 18.1% [5]. In this PV technology, the HJ with intrinsic thin layer (HIT) SHJ SCs were made by integrating a very thin a-Si:H(i) films in between the c-Si wafer and doped emitter layers, where main use of a-Si:H(i) layer is to passivate the c-Si surfaces and also defect density at interfaces [5]. The configuration is registered as HIT by Sanyo in 1992. After Sanyo's record efficiency with breakthrough technology in Si photovoltaics, this c-Si/a-Si:H HJSCs PV technology was gained lots of attention by research groups throughout the globe [97,157]. In 2014, the Sanyo has published highest efficiency of 24.7% (100 cm²) with both side contacts (bifacial structure) and 25.6% (43 cm²) with using interdigitated back contacts [98] and V_{oc} of 750 mV on (n)c-Si wafer with HIT SCs architecture [6]. This efficiency surpassed the efficiency of c-Si based homo-junction SCs and gained huge attention in this technology [158]. This SHJ technology significantly decreased thermal budget and wafer use compared to c-Si homo-junction SCs. The fabrication procedure, deposition parameters are still confidential to global researchers, however most of the research work is going on and this c-Si/a-Si:H heterojunction concepts are adopting to other photovoltaic technologies. This SHJ technology increasing significantly due to it is compatible, industrial feasibility and large scale manufacturing of the SCs [159]. Interdigitated back-contact (IBC) design was developed in order to reduce parasitic absorption of light in the a-Si:H layers, which results in remarkable improvement in the J_{sc} of SHJ SCs [8,158,160]. Later, in 2015, Kaneka has overcome HIT record efficiency and achieved 25.1% (151.9 cm²) with both sided contacts and then reported world highest recorded efficiency of 26.7% (180 cm²) with IBC-SHJ design [8,158,160]. The highest reported efficiency is 26.1% on c-Si(p)-wafer with IBC-SHJ SCs architecture [92]. Duy Phong Pham et. al. have reported the high efficiency of 21.8% with V_{oc} of 727 mV, J_{sc} of 39 mA/cm² by using μc-Si:H(n) and μc-SiO_xH(n) as a seed and front contact layer respectively [161]. It was found that Si seed layer subsequently improve the microstructure of the emitter/BSF contact layer. Xiaoning Ru et. al reported efficiency of 25.11% for SHJ SCs on a full size monocrystalline-silicon (c-Si) (n-type M2) wafer (total area, 244.5 cm²) by adding an extreme thin a-Si:H(i) buffer layer. The deposition rate, high microstructure and H-rich layer have shown superior surface passivation quality and then improved V_{oc} and efficiency of SHJ SCs [162]. The nc-SiO_x:H layer exhibits bright opto-electrical properties for carrier selective contacts (CSCs) in SHJ SCs and obtained high efficiency of 22% with J_{sc} of 39.3, V_{oc} of 712 mV and FF of 78.6% [151]. Daniel Meza et. al also used nc-Si:H films as emitter layer and obtained efficiency of 22.8% [163]. The bi-layers of nc-SiO_x:H(p) and nc-Si:H(p) have been incorporated into SHJ SCs as hole collector/ (p) contact stack and observed 22.47% efficiency with J_{sc} of ~38.8 mA/cm², V_{oc} of 719 and FF of 80.4% [164]. Depeng Qiu et.al obtained efficiency (η) of 23.1% with V_{oc} of 738 mV, FF of 80.4%, J_{sc} of 39.0 mA/cm² on M2 wafer with 5 nm of nc-SiO_x:H (n) and nc-Si:H (n) contact layer [165]. The efficiency of multi crystalline Si SCs is low compared to pure c-Si as well as c-Si/a-Si:H HJSCs and reported highest efficiency is 22% [157]. Many research groups are achieved high efficiency over the 22-23% with SHJ SCs [166,167]. From the literature, it is observed that nc-Si:H thin films are better alternate to a-Si:H emitter layers in SHJ SCs due to higher bandgap, good electrical and microstructural properties. High bandgap and high conductivity

emitter layer allows the more no. of photons to c-Si wafer for generation of e⁻h pairs as well as drive the separated free charge carriers to metal contacts, which leads to ultimate progress in the performance of SCs. Amorphous silicon based SCs having efficiency of 8-10% is reported with a-Si:H emitter [91]. The efficiency of 11.9%, 12.7% and 14% has been obtained for μc-Si, a-Si/ nc -Si and a-Si/nc-Si/nc-Si thin film SCs [91], whereas 12.3% is reported for a-Si/ nc -Si tandem SCs [91]. In order to reduce wafer cost of SCs, thinner and multi crystalline wafer can be used for preparation of SCs. The SHJ SCs offer symmetrical structure and highly suitable for bifacial designing of SCs, which enables high bifaciality factor and high energy yield [6,7].

SHJ technology having significant advantages in terms of power conversion efficiency, however, the market share is slowly increasing and present efforts on developments of SHJ are proven the feasibility of industrial manufacturing and competitiveness. This SHJ based PV technology accommodated the assure of lower LCOE and high energy-yield [29] credits to the ameliorate temp. coefficients, bifaciality and very less deterioration over period of time [168].

This HIT technology scheme has been applied to passivated rear and emitter contact (PERC) Si [169,170], passivated emitter rear totally diffused (PERT) [28], tunnel oxide passivated contact (TOPCon) Si [141], point contact Si and interdigititated back contact (IBC) Si SCs etc [9,142,170,171], aluminum back surface field (Al-BSF) [172], polycrystalline silicon (poly-Si) on oxide (POLO) SCs [92,173,174], poly-Si carrier-selective passivating contact (CSPC) [14,175,176], hole and electron selective contact (HSC and ESC) or dopant free carrier selective SCs [142,177-179].

It is evident from the ITRPV data (Fig. 9), PERX and TOPCon SCs have shared 90% in 2022, back and SHJ solar technology shared 2% in 2022 and expected greater than 20% in 2032 [15]. The BSF SCs shared about 15% in 2020 and expected to disappear after 2025. Bifacial SCs gaining market share in present and coming years as compared to monofacial SCs due to reduced thermal and mechanical strain, improved performance, reduced metal paste usage and double side usage of SCs (Fig. 10) [15]. Wafer thickness for c-Si based SCs has been reducing every year, which results in reduced usage of Si material, presently less than 4g Si is using for generating a watt power [3].

3.3. Interdigitated back contact- silicon heterojunction (IBC-SHJ) SCs

High V_{oc} is the main feature of SHJ (HIT) solar cell, whereas high J_{sc} is the main feature of interdigitated back contact (IBC) SCs. Fig. 11a shows schematic diagram of fabrication process steps of IBC-SHJ SCs on

p/n-type c-Si wafer. The high efficiency can be realized for crystalline silicon by combination of SHJ and IBC architecture shown in Fig. 11b. Both metal contacts (positive and negative) were deposited on rear side of Si wafer, this design significantly reduce optical, shading losses and also recombination losses at front side of the SCs. This design offer most of the light is utilized and generate electron-holes pairs, which results in improvement in J_{sc} of the SCs. Researchers at Panasonic company have reported high efficiency of 25.6%, J_{sc} of 41.8% on area of 143.7 cm² by combining interdigitated back contacts to silicon heterojunction technology [98]. Later, Kanenka group has overcome the record efficiency. The highest world record efficiency of 26.7% was reported on n-type by Kaneka group [8,160] and 26.1% on p-type c-Si wafer with IBC-SHJ SCs technology [92]. An efficiency of 26.1% was achieved on c-Si(p) wafer by implementing poly-Si(i) region b/w p & n-type poly-Si regions by employing an inter-digitated back contacted SC designs with poly-Si on oxide passivation contacts (IBC-SHJ SCs architecture) [92]. The hydrogen was incorporated through Si:H-rich SiN layers and a subsequently annealed at 425 °C for 30 min, which results in superior passivation by suppressing the recombination active defects at poly-Si (p&n) interface as well as in the poly-Si [174]. Shivram et.al proposed new process sequences to simplifying the back sided designing of the SHJ- IBC SCs. Interdigitated layers of a-Si:H (i&p⁺) and a-Si:H (i&n⁺) were fabricated by partially etched blanket a-Si:H (i/p⁺) through a hard mask to extract only the a-Si:H(p⁺) layer and replaced with a-Si:H (n⁺) layer. This approach has eliminated the ex-situ wet cleaning after dry etching and also preventing re-illumination of the c-Si surfaces during deposition of rear layer. With this process, reported an efficiency of 23% and V_{oc} of 730 mV [180]. Gianluca L. et. al achieved efficiency of 20% for selected emitter architecture known as PeRFeCT and 21% of efficiency with poly-Si and a-Si:H CSPCs at rear and front respectively [175]. Robby Peibst et.al obtained 23% of efficiency and J_{sc} of 42.2 mA/cm² by employing double ARC of SiN_x and textured SiO₂ obtained with IBC with poly-Si CSPC SCs [123,173]. B. Paviet-Salomon et.al tried to simplify the IBC-SHJ design and proposed tunnel-IBC structure featuring inter-band tunnel junction. Hydrogenated nano-crystalline silicon layers were integrated in the structure and reported a conversion efficiency of 23.9% [181]. Guangtao Yang et. al achieved 22.5% and 23% of efficiency for IBC SCs with poly-Si CSPCs prepared by self-alignment and etch-back processes respectively [176]. However, it is very risky, time taking and ambitious to get such high performance SCs due to poor quality of Si wafers, high quality cleaning of surface before the a-Si:H deposition, precisely control of deposition, superior passivation quality and need of advanced techniques and no. of complex processing steps

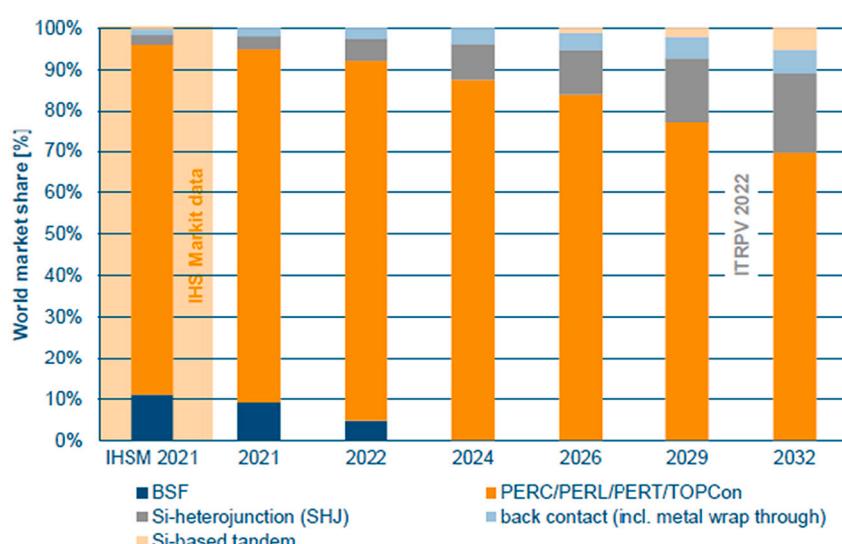


Fig. 9. Market share of different PV technologies [15].

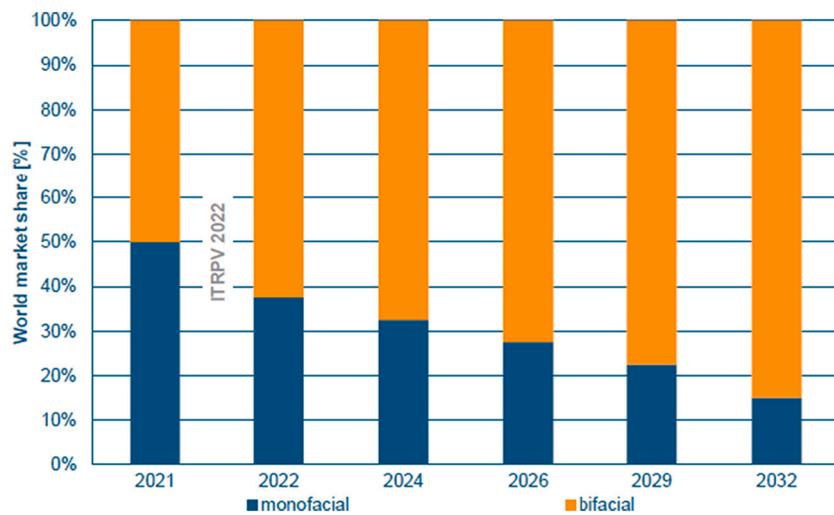


Fig. 10. Market share of monofacial and bifacial PV technologies [15].

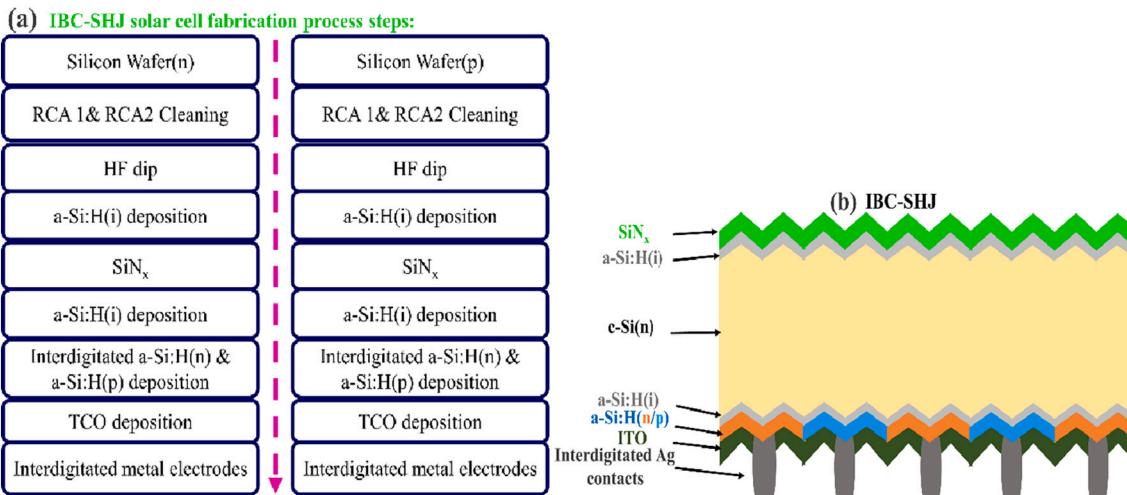


Fig. 11. a) schematic diagram of fabrication process steps of IBC-SHJ SCs on p/n-type c-Si wafer and b) schematic structure of IBC-SHJ SCs.

and contamination issues. In order to get expected performance of the SCs, one should full fill above requirements, which results in higher cost and difficulties involved. This is the one of the reasons for few groups are

realised high efficiency. There are lots of complicated problems are involved for industrial manufacturing and mass production of the IBC-SHJ structured SCs.

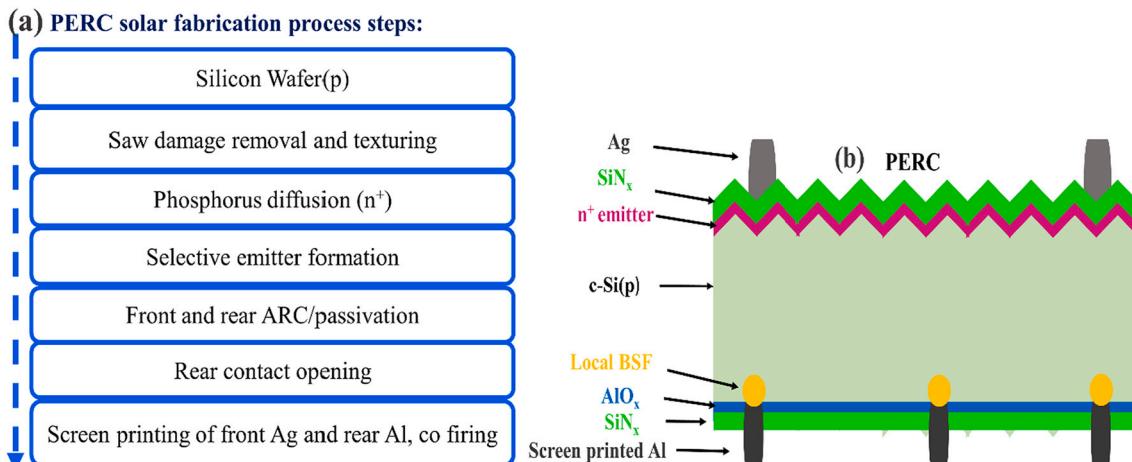


Fig. 12. (a, b). Schematic diagram of fabrication process steps of PERC SCs and Structure of Passivated Emitter Rear Contact (PERC) (layers are not in scale).

3.4. Passivated emitter rear (PERx) ($x=$ Contact, locally and totally diffused) (PERC, PERL and PERT) SCs

PERC devices have been fabricated similarly like Al-BSF SCs but rear surface passivation (generally, AlO_x) and local aluminum BSF contact layers were deposited by laser ablation. Fig. 12(a, b) show schematic diagram of fabrication process steps of PERC SCs and structure of Passivated Emitter Rear Contact (PERC) [182]. The rear passivation layer further reduces recombination defects and improve the V_{oc} . This results in PERC SCs show high potential for efficiency and suitable for fabrication on higher bulk life time mono-crystalline silicon wafers.

It is reported that the PERC SCs have surpassed the efficiency of the Al-BSF SCs by employing a dielectric layer between Si and Al that passivates the surfaces betterly compared to the Al-BSF and, also enables mirror reflection greater than 90% [183]. Ohmic contacts were deposited by evaporation method in PERC cells, whereas, evaporated Al was annealed for Al-BSF SCs to forming a locally alloyed BSF [14,159]. Schematic diagram of fabrication process steps of PERT and PERL SCs and Structure of Passivated Emitter Rear Totally Diffused (PERT) and Passivated Emitter Rear Locally Diffused (PERL) SCs shown in Fig. 13 (a, b & c) respectively. An efficiency of 22.7% was achieved with a fully ion implanted boron emitter and phosphorus BSF of PERT (Fig. 13b) SCs [14,142,184,185]. The highest reported efficiency of PERL (Fig. 13c) solar cell by locally diffused boron BSFs was 25% on 4 cm^2 [186], it was highest efficiency until the reported efficiency of Sanyo's HIT SCs in 2014. The present highest efficiency of PERC SCs is around 22.9% [14,123]. An industrial process for PERC cells on multi-crystalline p-type Si wafer, and gained efficiencies of SC up to 21.25% with a V_{oc} of 667.8 mV [242.74 cm^2] [184]. The efficiency of this technology can be improved as already known processes of selecting emitter layers, thinner metal contacts, improved quality of materials and quality of surface passivation. However, it is found that the parameters of these SCs are

restricted by recombination losses due to metal-semiconductors contacts. To further boost the efficiencies of PERC/PERL/PERT SCs, it is required to minimize metallized regions, reduce recombination losses between semiconductor-metal contacts, improve the existing technology or develop a new technology is necessary.

3.5. Aluminum doped-back surface field (Al-BSF) SCs

Al-BSF SCs have been processed by (i) cleaning the surface of c-Si wafer and removing saw damage and texturing, (ii) diffusion of phosphorus/boron on front side as emitter layer, (iii) deposition of SiN_x , which act as an anti-reflection and passivation layer, (iv) screen printing and burning of the front and rear metal contacts [14,139,159,172,185]. Fig. 14 (a, b) shows the schematic diagram of fabrication process steps of Al-BSF SCs and schematic diagrams of Al-BSF SCs. Phosphorus diffusion keeps a lower contact resistance at the interface of Si & metal, surface recombination defects and also opens lateral carrier transportation between the front metallic contacts. Further, the bulk defects have been passivated by hydrogenation. The design of Al-BSF SCs limit the manufacturing cost and offer the higher performance. The disadvantage of this SCs is recombination losses at rear metal contacts, which limit the efficiency around 23% [136,137,187]. Generally, these Al-BSF SCs were fabricated on low quality mc-Si wafers to reduce production cost.

3.6. Tunnel oxide passivated contact (TOPCon) SCs

Fig. 14 (a, b & c) show schematic diagram of fabrication process steps of TOPCon SCs and schematic diagrams of TOPCon and TOPCoRE SCs respectively. TOPCon SCs constructed with a stack of very thin interfacial SiO_2 ($\sim 1-3 \text{ nm}$) and heavily doped poly-Si layer shown in Fig. 14. The main role of very thin oxide layer is effectively passivating dangling bonds and interface defects sites at the c-Si surfaces. It acts as a tunneling

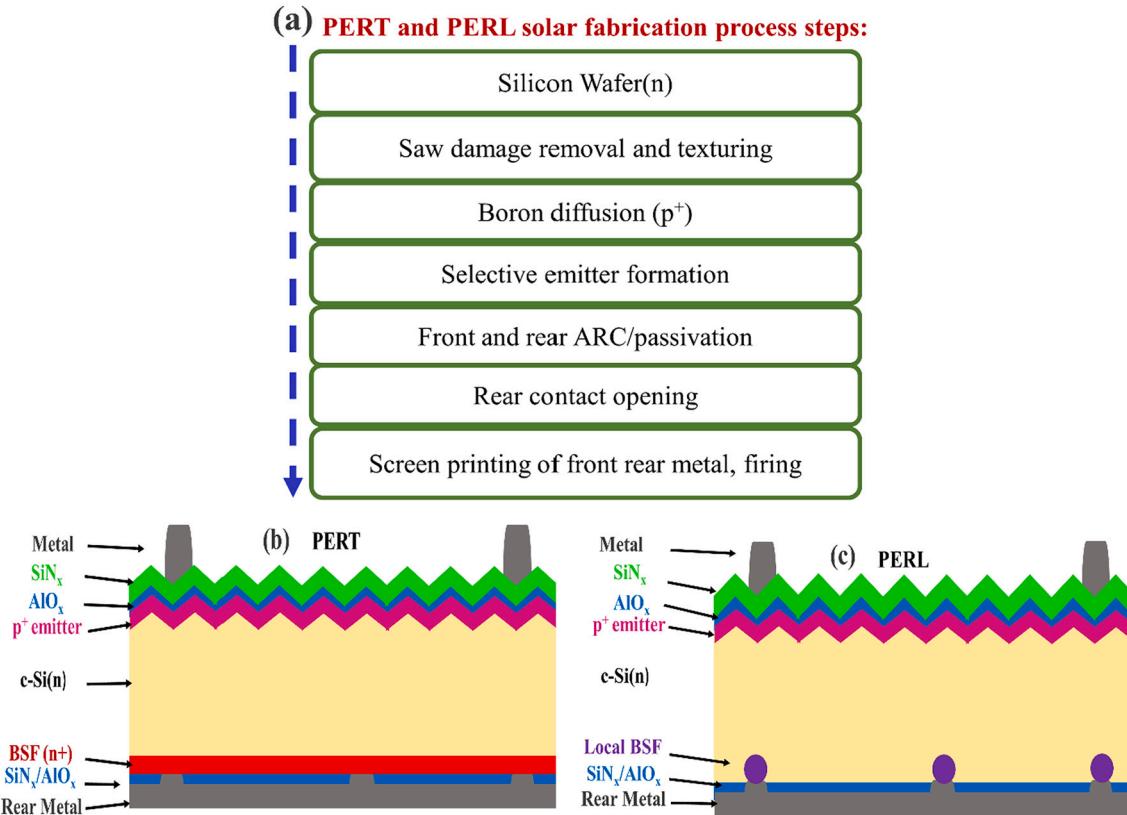


Fig. 13. (a, b & c). Schematic diagram of fabrication process steps of PERT and PERL SCs and Structure of Passivated Emitter Rear Totally Diffused (PERT) and Passivated Emitter Rear Locally Diffused (PERL) SCs (layers are not in scale).

(a) Al-BSF solar fabrication process steps:

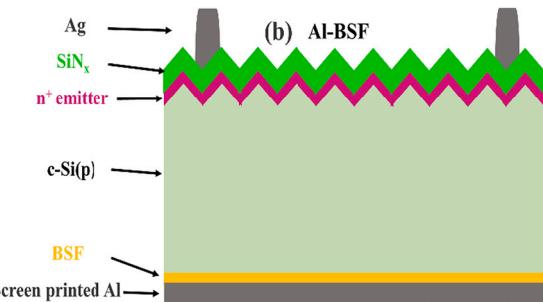
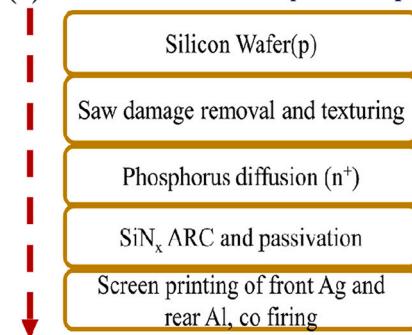


Fig. 14a. (a, b). Schematic diagram of fabrication process steps of Al-BSF SCs and schematic diagrams of Al-BSF SCs.

(a) TOPCon solar cell fabrication process steps:

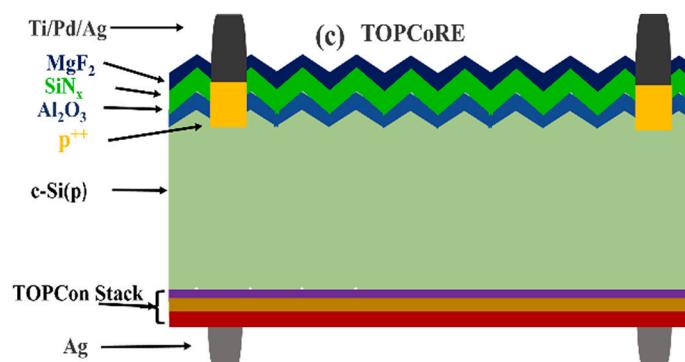
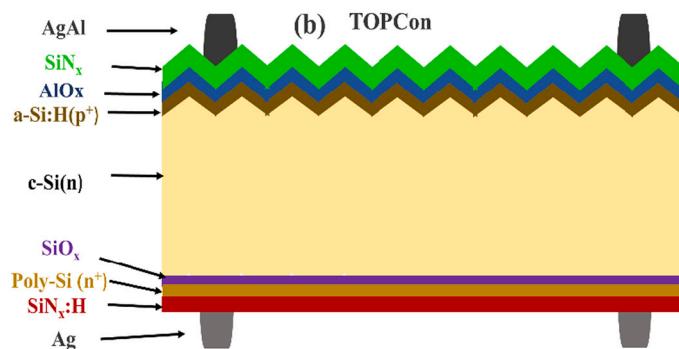
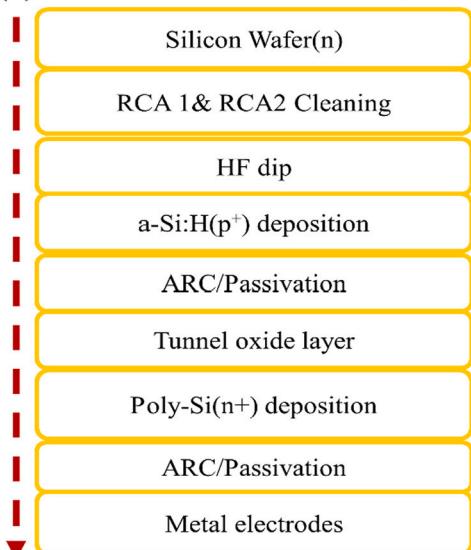


Fig. 14b. (a, b & c). Schematic diagram of fabrication process steps of TOPCon SCs and schematic diagrams of TOPCon and TOPCoRE SCs.

barrier for minority charge carriers and thus reduces recombination losses [141,191,192]. This PV technology was started in 1980 [141,192,193]. In, 2013 both-side contacted TOPCon (tunnel oxide passivating contact) SCs have been introduced by Feldmann et. al [141]. The record high efficiency of 25.8% [189]and 26.1% have been demonstrated for both side and single side contacted SCs respectively [92,174]. Tunnel oxide passivated contact PV technology has explored as a promising for high-efficiency SCs. TOPCon Technology offers lower re-combination current density ($\sim 1 \text{ fA/cm}^2$) and reasonable low

contacts resistivity ($\sim 1 \text{ m}\Omega\text{-cm}^2$) [194]. The surface passivation quality has been significantly improved by incorporation of H_2 into Si network by supplying as HPT or hydrogen contained dielectric materials (SiN_x [195–197] and Al_2O_3 [198] etc.), whereby hydrogen passivates electrically activated defect centers at the c-Si/ SiO_x interface [198] and also within the poly silicon layers [199]. Young-Woo Ok et. al reported poly-Si(p)/ SiO_x passivation contacts with a capped layer of SiN_x establish superior surface passivation with a very low J_0 of $\sim 5 \text{ fA/cm}^2$ and reported efficiency of 21% on larger area (239 cm^2) [200]. The historical

developments, fabrication processes, the working principles, charge carriers transport, main challenges like formation of metal contacts and integration into industrial-feasible and manufacturing process steps are more elaborately discussed in the review papers [14,28,137,201]. TOPCon structure eliminates the requirement of diffusion or implantation doping of the wafers and also complicated designing of emitter and BSF layer. Production of this technology is started for industrially large-scale.

TOPCon Rear Emitter (TOPCoRE) SCs were fabricated as TOPCon stack at rear side and P⁺⁺ emitter, passivation and ARC at front side of p-type c-Si (Fig. 14 c). The boron-doped P⁺⁺ emitter was deposited by BBr₃ diffusion at 870 °C in a tube-furnace and the oxidation at 1,050 °C. This was passivated with a 10-nm-thick Al₂O₃ layer deposited with ALD at 180 °C. The front side was coated with a double ARC layer of 50 nm SiN_x and 90 nm of MgF₂ and then evaporation of Ti/Pd/Ag front metal contacts. The full-area TOPCon stack was deposited as similar way of TOPCon SCs. In order to decrease the surface recombination losses near top contacts, P⁺⁺ emitter layers were deposited underneath of the front contacts [12]. The high efficiency of 26% and FF of 84.3% were obtained for TOPCoRE SCs on p-type c-Si wafer and 25.8% of efficiency with TOPCon (front junction) on n-type c-Si [12]. These values are obtained without TCO layers at the front surface, results in effective way of charge carrier transportation from c-Si to front contacts. These results were reported as highest efficiency for both side contacted TOPCon c-Si SCs [12]. These results may show a way to high performance both sided contact TOPCon c-Si SCs.

3.7. Hole and electron selective contact (HSC and ESC) or dopant free carrier selective SCs

Carrier selective contacts play very significant role in SCs as an efficient emitter, back surface field and excellent passivation layers to achieve high power conversion efficiencies [202–204]. Fundamentally, selective contacts establish potential gradient with light absorbing semiconductor, which allows one type of carriers and blocks opposite type of charge carriers. These contacts passivate surface, interface and bulk defects in the SCs [202,205]. Schematic diagram of fabrication process steps, SHJ based SCs with MoO_x hole and TiO_x electron collector layer shown in Fig. 15(a, b & c) respectively.

In order to reduce complicated process steps, toxic dopants, parasitic absorption and resistive losses, fabrication temperature and manufacturing cost and improve the efficiency of SCs, transition metal oxides (TMOs) have been applied as carrier-selective passivation contacts for Si SCs [179,202,206]. Generally, the materials with wider bandgap or lower work function with silicon material offer smaller conduction band offset, which are useful for electron selective contacts and materials with smaller bandgap or higher work function offer smaller valence band offset, which are applied as hole selective contacts for SHJ SCs [207–209]. Due to smaller conduction and valence band offset, ESCs allows only electrons, whereas HSCs allow only holes and blocks opposite charge carriers respectively. The molybdenum trioxide (MoO₃) [17,210], tungsten trioxide (WO₃) [207,211], vanadium pentoxide (V₂O₅) [212] and rhenium trioxide (ReO₃) [213] have been demonstrated as HSCs. Titanium dioxide (TiO₂) [214] and cesium

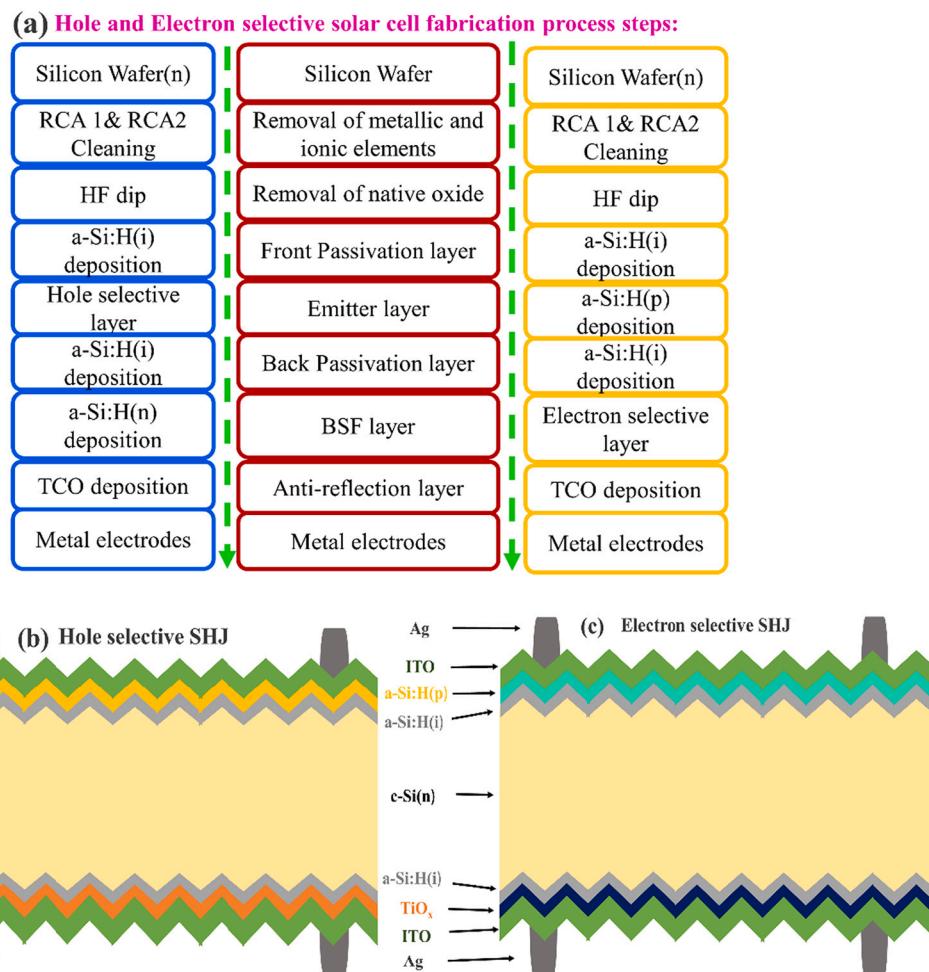


Fig. 15. (a, b & c): Schematic diagram of fabrication process steps, SHJ based SCs with MoO_x hole and TiO_x electron collector layer.

carbonate (Cs_2CO_3) [215] have also been demonstrated as ESCs. Conversely, the work function difference with p-type c-Si is small resulting in a quasi-ohmic contact. In case of MoO_x hole transport layer, mainly depending on the wafer type, the large work function difference between MoO_x and n-Si and the develops upward band bending and results in depletion of majority carriers at interface by forming Schottky junction, while, it forms semi-ohmic contact due to small difference of work function [216,217]. Similarly, TiO_x makes wider bandgap difference with silicon material and offers smaller conduction band offset, which results in TiO_x act as an electron transport layer [216]. Few groups have concentrated on TMOs as selective carrier passivation contacts in SHJ SCs [177,202,218–221]. These films were deposited by evaporation, sputtering, e-beam evaporation, solution process (spin coating technique) and atomic layer deposition (ALD)[219,222,223]. However, most of the researchers have deposited these films by thermal evaporation and ALD [221,223–226], which offers the soft and good material selectivity.

In 2011, Park et.al reported that a-Si:H based thin film SCs with 6.26% efficiency was fabricated with thermally evaporated MoO_3 film as a window layer in place of a-SiC:H(p) films [206]. In 2014, Battaglia et. al have employed MoO_x films into SHJ SCs for replacing the a-Si:H(p), results in significant optical gains [205]. This improved optical gain has improved the total photocurrent by 2.4 mA/cm² and obtained high efficiency of 18.8%, V_{oc} of 711 mV and J_{sc} of 39.4 mA/cm² [177,205]. Geissbuhler et.al achieved SHJ solar cell efficiency of 22.5% and FF of 80% with MoO_3 window layer [218]. Cho et al. studied the interface properties and thermal stability of MoO_3 films and obtained efficiency of 19.3% and V_{oc} of 724 mV and FF of 0.74 [225]. Carrier selective contact SCs were fabricated by 10 nm thick MoO_x film and achieved efficiency of 20% and effective minority carrier lifetime of 2.3 ms [223]. Jinhun et.al reported high V_{oc} of 730 mV, FF of 0.78 and efficiency of 21.3% with a 3 nm thick MoO_3 buffer layer [220]. Kumar et.al also reported high efficiency of 20%, V_{oc} of 695, FF of 0.74 and J_{sc} of 38.9 mA/cm² [221,223]. It is observed that from literature, SHJ SCs with titanium oxide (TiO_x) and MoO_x as ESC and HSC are shown highest efficiency of 23.1% and 23.5% respectively [187,227].

The TMOs based ESCs are studied extensively which include mainly, TiO_x [187,228–230], magnesium oxide (MgO_x) [231,232], tantalum oxide (TaO_x) [159,233], ZnO [233], and niobium oxide (NbO_x) [222]. The TiO_x ESCs are widely used due to smaller CB offset of 0.05 eV and larger VB offset of about 2 eV with Si material [228]. Thin TiO_x layer was serve as a ESCs and also passivate c-Si surface, this could be due to creation of the Si-O-Ti covalent bonds at interface of Si/ TiO_x [232,234]. Reported low efficiency of 7.1%, with TiO_x as an ESC layer at first, this low performance of the device is due to carrier recombination and conductivity losses of TiO_x layer [230]. Later, TiO_x applied at the back side of n-Si/ front PEDOT: PSS SCs and improved the efficiency to 13.9% [235]. Yang et al., deposited TiO_x -based contacts by ALD technique and observed that the films have good surface passivation as well as lower contact resistivity [228]. Further, the efficiency was boosted to 19.8% on n-Si/ boron-diffused p+ emitter as front with TiO_x rear contacts. Tunnel oxide (SiO_2) interface passivation layer was added in between Si (n) & TiO_x , which results in furthermore enhancement of the efficiency to 22.1% [187,228]. However, lower V_{oc} of about 675 mV was observed for SHJ and which is lower comparable to other silicon PV devices. It was seen that high efficiency of 23.1% and 21.8% was achieved by incorporating the TiO_x/LiF and TiO_x/Ca passivation contacts on Si(n) respectively [233] and 19.2% was achieved with Yb capping [236]. Other metal oxides such as MgO , NbO_x and ZnO films were deposited by thermal evaporation/ALD with a required band offset with Si have been studied as ESCs for c-Si/a-Si:H HJSCs [231,232]. The reasonable efficiency of 20% and V_{oc} of 629 mV has been achieved with MgO contacts deposited by thermal evaporation [231]. SHJ SCs with CSCs have a lot of scope to improve the solar cell performance by reducing parasitic absorption and resistive losses, defects, simplifying process steps and improving stability.

Fig. 16 shows the development of laboratory and commercial solar cell efficiencies of different type of silicon SCs over period. It will be expecting that very soon efficiency of lab cell will reach the physical limit of the SCs. **Fig. 17** shows the current efficiencies and power of selected commercial PV modules as per bulk material, cell concept and efficiency [3]. It is evident that from **Fig. 18**, mono and multi -crystalline Si module efficiency is 2.3% and 4% lower than the cell efficiency of mono and multi -crystalline Si cell respectively and also this trend is similar for other PV technology [3]. The efficiency of 22.7% and 20.4% was reported for PERC and multi crystalline Si based SHJ SCs respectively [158,237]. It is observed that module efficiencies are lower than the reported laboratory scale SCs due to different challenges in large scale, feasibility in PV technology and mass production of SCs.

4. Simulation developments on SHJ SCs

Simulation studies literally help researchers to optimize the intrinsic/doped layers, TCO layers and metal contacts and also useful for designing the different structures, fabrication of the optoelectronic devices and improvement of the performance of these devices without spending lots of time, risk and money in it. Presently, many researcher groups are concentrated on simulation/analytical studies of c-Si/a-Si:H HJSCs to uplift the performances by resolving several issues which are accountable for worsening of the performance of the SCs [91,238].

Numerical simulation techniques are practicable methods for evaluating and understanding the functioning of devices by creating the several SC structures and modifying the thickness, doping density, recombination sites at surface, bulk and interfaces of layers, bandgaps, various TCO layers, work function of the different layers [164,239–246]. Some of the research groups have developed few simulation tools for studying the functioning of SCs like AFORS-HET [242,246,247], AMPS [248], Sentaurus [249], Scaps [250], Silvano [251], Asa [252], Lumerical FDTD [253,254], Amorphous Semiconductor Device Modelling Program (ASDMP) [242,255,256]. Many groups have modeled different structured SC devices and analyzed by modifying thickness of layers, bandgap, interface defect states, doping concentration [257–259]. These simulated results are mostly matched with the properties/performance of the films/SCs prepared by experimental techniques [165,243,258,260]. The high bandgap of 1.65–1.7 eV of a-Si:H (p/n) and a-Si:H (/i) layers used for SHJ SCs. Thickness of the a-Si:H layers has varied from 2–10 nm for both layers and found that the optimum thickness is about 4–5 nm for high efficiency SCs, these results are comparable with experimentally fabricated SCs.

Zhuopeng Wu et.al studied the interface passivation and band alignment for silicon HJSCs by manipulating hydrogen flow rate and compared results with varying bandgap of emitter layer by simulation. Simulation results describe that the charge carrier transportation in HJSCs depends on the alignment and the nature of energy gap states at hetero interfaces [261]. The effect different TCO layers such as ITO, $\text{ZnO}: \text{Al}$ and $\text{IO}: \text{H}$ on the functioning of the SHJ SCs have been studied extensively. Louis O. Antwi et.al obtained simulated efficiency of 29.19% by optimized the defect sites and defined charge density of interfacial layers [262]. Dwivedi et.al reported 27% of efficiency by modifying thickness of various layers of different structured SHJ SCs [263]. Arti. R et. al reported higher efficiency of 24.14% for c-Si/ $\mu\text{-Si:H}$ HJSCs [264]. The efficiency of 9.35% and 17% has been observed for a-Si:H/nc-Si:H and $\mu\text{-Si:H}$ thin films based SCs respectively [245,265]. This efficiency was slightly boosted with a-Si:H/ $\mu\text{-Si:H}$ (15%) and a-SiCH/a-SiGe:H/ $\mu\text{-Si:H}$ (17%) thin film SCs respectively [266,267]. H. Bencherifa et.al enhanced light trapping by triangular texturing and double ARC layer, which results in betterment of J_{sc} (47.9 mA/cm²) and also efficiency of 20.06% for planar structure (a-Si:H(n)/a-Si:H(i)/c-Si (p)/c-Si (p⁺)) [268]. The emitter layer properties were explored by varying doping density and observed that density of recombination states decreased by increased electric field strength. Achieved an efficiency of 19.8 % by optimizing energy gap and doping density of SHJ

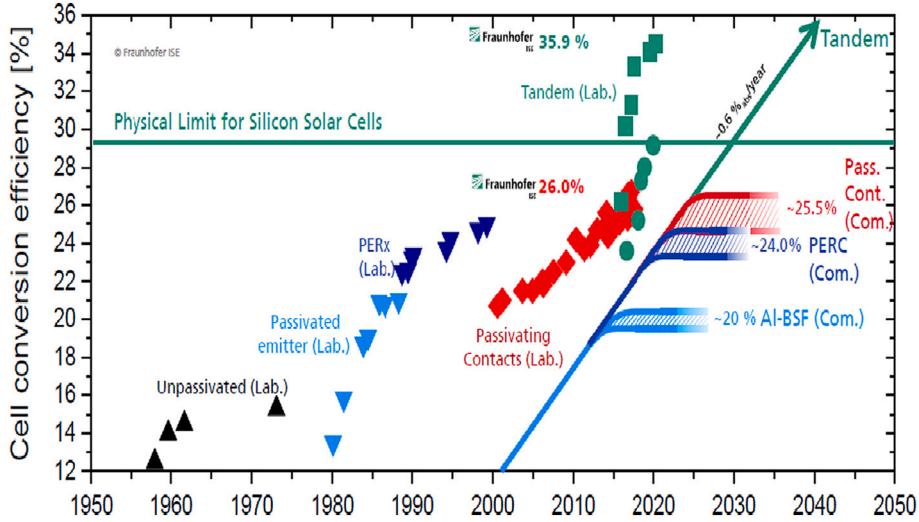


Fig. 16. Development of laboratory and commercial solar cell efficiencies [3].

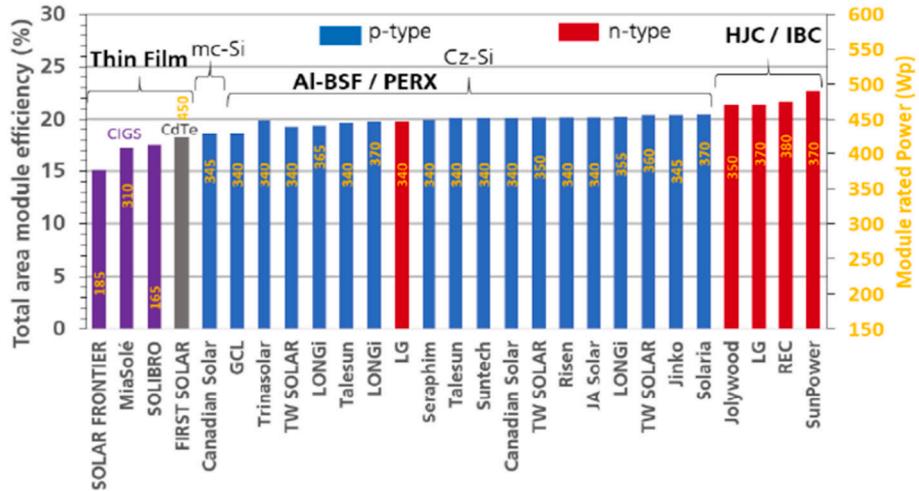


Fig. 17. Current efficiencies and power of selected commercial PV modules as per bulk material, cell concept and efficiency [3].

SCs with rear diffused n⁺ layer [269]. D. Muchahary et. al used double a-SiC emitter and μc-Si:OH as BSF layer obtained efficiency of 20.56 with low J_{sc} of 37.86 mA/cm² and V_{oc} of 673.5 mV. This could be due to increased parasitic absorption losses and poor interface passivation [270]. Depeng Qiu et.al fabricated the bifacial SCs with nc-SiO_x:H (n) (5 nm) and nc-Si:H (n) (5 nm) contact layer and shown V_{oc} of 738 mV, FF of 80.4%, J_{sc} of 39.0 mA/cm² and efficiency of 23.1%. Same device structure is simulated by AFORS-HET and Quokka 3 tools, found that comparable results with experimental results [165]. Peng Dong et.al demonstrated that the front floating emitter structure in IBC-SHJ cells has a higher flexibility for SC fabrication, BSF and emitter width, this results in simple fabrication process steps and less production cost [271]. For p-type contacts, the hole transport is primarily limited by activation energy and band gap of the p-layer and work function of the TCO. Whereas for n-type contacts, transport of electrons was limited by the activation energy and work function of the doping layer [272]. Zhenhai Yang et.al studied the IBC-SHJ SCs by adding the built-in fixed charges in the front side dielectric passivation layer by numerical simulations [273]. Carrier transport inside the bulk Si has promoted by the front-surface charges by suppressing the recombination losses at the interfaces [273]. Paul Procel et.al analyzed the carrier transportation formulism in IBC-SHJ SCs through the band bending at c-Si interface using TCAD Sentaurus and obtained simulated efficiency of 27.2%, FF of

86.8% and V_{oc} of 754 mV [272].

Ajeet Rohatgi et.al have used simple methodology to model the TOPCon SCs, Extended 2-D Sentaurus shown that the efficiency of 23.8% and expected to be boosted to 26% by better quality wafers, vertical plating contacts having externally aligned bus bars and reducing re-combinations in the TOPCon structured SCs [274]. Suchismita. M et. al expected V_{oc} = 766 mV for J_{oe} = 2 fA/cm² for doping density of poly-Si is greater than 10²¹ cm⁻³ in a c-Si/SiO₂/poly-Si contact for a 50-μm-thick wafer and V_{oc} values decreased to 750 mV for a 180-μm-thick wafer [275]. However, it is very difficult task to get such a high V_{oc} values for TOPCon SCs experimentally. The influence of the front surface field (FSF), lateral conductivity on the working of TOPCon cells has studied by simulation as well as experimentally and obtained efficiencies of 24.3% and 23.9% with and without the full-area FSF [33]. Junsin group has investigated the effects of CSFCs layer and defect states of SHJ SCs by AFORS-HET simulation tool. Cell efficiency of 22.77%, V_{oc} of 729 mV, J_{sc} of 39.99 mA/cm², FF of 78.06% with nc-SiO_x:H (n) as CFSC layer was achieved and found that close values of efficiency of 24.04%, V_{oc} of 733, J_{sc} of 40.03 mA/cm², FF of 81.97% by simulation [166]. The nc-SiO_x:H CSFCs have shown superior properties than the a-Si:H CSFCs layer due to the effect of tunneling and field effect passivation by the nc-SiO_x:H CSFCs [166]. Material related efficiency losses of mc-Si layers due to bulk recombination defects were demonstrated by PC1D

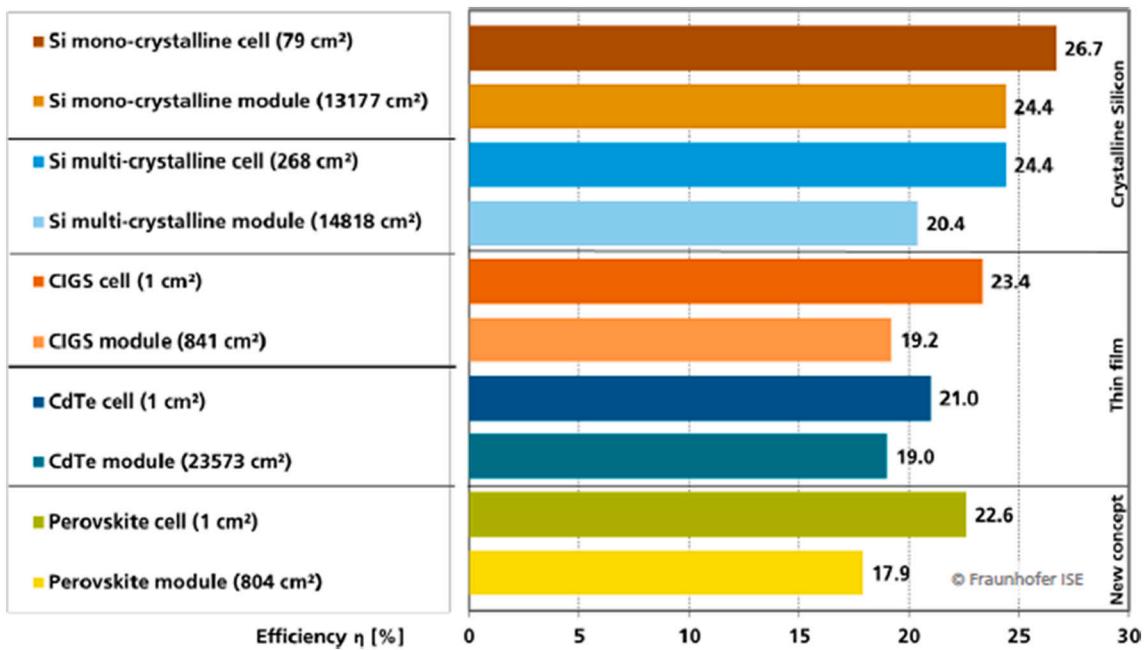


Fig. 18. Comparison of best efficiencies of SCs and solar modules [3].

simulation tool for TOPCon SCs [276]. Observed opto-electrical losses of mc-Si SCs are due to recombination sites at grain boundaries and in the emitter [277]. Reported high efficiency of 25.6%, V_{oc} of 752 mV, J_{sc} of 38.8 mA/cm², and FF of 79.0% by work function of 6.9 eV of MoO_x and decreasing rear recombination velocity [278]. However, more advanced simulations tools with flexible handling, accuracy, high response are required for studying already developed SCs, creating new designs and innovative PV technologies.

5. Challenges and future directions for the c-Si/a-Si:H HJSCs

Several parameters gating silicon heterojunction SCs such as optical and electrical properties of the few nano-meter thick doped and undoped silicon thin films and the anti-reflective, interface passivation layers, transparent and conductive metal oxide layers and also metal contact layers. Surface cleaning and passivation is one of the main challenges to reduce the surface recombination losses. Precise control of thickness of all layers and deposition conditions is required. Doped a-Si:H(p/n) layers have required sufficiently doping to generate sufficient electric field and also better interfacial properties between intrinsic and doped-layers as well as doped and indium tin oxide (ITO)(TCO) layers. Formation of abrupt hetero junctions with less interface defect density to be addressed to reduce recombination states at the interface. Since, interfacial layers are very critical for c-Si/a-Si:H HJSCs for reducing recombination losses and improving charge carrier transport. Optimization and cost effective deposition of transparent conducting oxide (TCO) layer and metal contacts are important to reduce resistance, optical losses and budget. Achieving high efficiency of c-Si/a-Si:H HJSCs is still a challenge due to complicate processing steps and contamination issues. Different cost effective processing methods to be developed with industrial feasibility. In order to reduce material cost, achieving high efficiency with multi-crystalline and thinner wafers is one of the main challenges. Complicated process steps should be reduced, simple designing and cost effective deposition of different layers of SCs are required for industrial up taking and mass production of SCs on large area. SHJ devices with incorporated ITO may be threatened by the production scarcity, potential supply shocks, and the relative scarcity of indium in the earth's crust in order to meet the challenges faced by the increasing expansion of the PV industry towards higher scale

production. In order to maintain the same lateral conductivity of thick ITO layer for thinner ITO layers, the sheet resistance should be decreased for several orders by raising the carrier density. However, this will have a negative impact on optical characteristics due to an increase in parasitic IR light absorption. To overcome parasitic absorption of IR light, indium oxide layers doped with tungsten (IWO), cerium (ICO) and hydrogen (IO:H) could be used for improving the sheet resistance and the IR light management and then increase the short-circuit current density. The usage of indium-free TCO layers must be further investigated in order to entirely overcome the constraints imposed by the indium supply in order to allow sustainable manufacture of SHJ SCs and future tandem devices at the terawatt scale. Several other TCO layers like ZnO, ZnO:Al, FTO, AZO and IZO can be developed. Aluminum doped zinc oxide (AZO) is one of the considerable materials, due to its low cost, abundant supply of raw materials, and capacity to achieve efficiencies equal to those of ITO-based SHJ SCs. However, the relatively low conductivity and long-term stability of AZO layers still require a great amount of work to combat. The price of SCs is increasing due to huge consumption of Ag to make metal contacts. To enable sustainable manufacturing at the terawatt scale, novel screen-printing methods to reduce silver consumption as well as alternative silver-free metallization and interconnection technologies must be developed and deployed as early as possible. Additionally, by lowering the number of busbars, the maximum permitted finger cross-sectional area will also be raised, which enhances the dependability and printability of such fingers in the context of mass production. In order to decrease the amount of silver used in traditional busbar and tabbing zones, non-silver busbars (like Al or Cu) or busbar-less technologies need to be developed. To speed the reduction of silver consumption in fingers alternative materials or finger geometry and pattern must be created. In place of Ag screen printing technology, Cu plating, roll to roll printing, inkjet printing, direct printing, sputtering and Ni/Cu electroplating techniques should be developed for busbars and finger contacts of SCs. Al, Ni, Cu, Ti, Pd, Pt and their alloys like Ag/Al, Cu/Ni, Pd/Pt/Ag and Ag/Al/Pt also can be tested for using in screen printing.

6. Conclusions

In this paper, detailed review on the deposition, characterization and

developments of high-efficiency c-Si/a-Si:H heterojunction SCs by experimental and simulations has been presented. Different c-Si based PV technologies like HIT, IBC-SHJ, PERC, PERL & PERT, Al-BSF, TOPCon and dopant free carrier selective contact SCs are discussed. Developments on simulation studies of c-Si/a-Si:H SCs have been also discussed, which produce realization of output of SCs with different structures before starting fabrication of SCs by experimentally. SHJ technology has capability of high power conversion efficiency and feasibility of industrial manufacturing and competitiveness. This SHJ based PV technology accommodated the assure of lower LCOE and high energy-yield, credits to the ameliorate temp. coefficients, bifaciality and very less deterioration over period of time. The highest of 26.7% was realised on n-type and 26.1% on p-type c-Si wafer with IBC-SHJ solar cell technology. However, there are lots of complicated issues like high quality cleaning of surface before the a-Si:H/poly-Si deposition, precisely control of deposition, superior passivation quality and need of advanced techniques and no. of complex processing steps and contamination issues are involved for industrial manufacturing and mass production of the IBC-SHJ structured SCs. The disadvantage of this Al-BSF SCs is recombination losses at rear metal contacts, which limit the efficiency around ~22-23%. To further boost the efficiencies of PERC/PERL/PERT SCs, it is required to minimize metallized regions, reduce recombination losses between semiconductor-metal contacts, improve the existing technology or develop a new technology is necessary. TOPCon technology has capable of high efficiency and production of SCs has started industrially on large-scale. This TOPCon structured SCs eliminate the diffusion or implantation doping steps and also complicated designing of emitter and BSF layer. Recombination sites on surface, in bulk and interfaces of SCs severely deteriorate the performance of the HJSCs. It is highly recommended to choose high quality metallization, TCO, Si layers, interfaces and HJ engineering, band bending alignments for high efficiency HJSCs. Dopant free carrier selective SCs reduce complicated process steps, toxic dopants, parasitic absorption and resistive losses, fabrication temperature and manufacturing cost. However, degradation effects and less throughput are observed compared to other SCs. Several simulation tools have been used to design SHJ SC structures and understand the function of different parameters on SHJ SCs. Simulated high efficiency of 27% was reported for bifacial SHJ SCs and efficiency of 27.2%, 24% and 25% obtained for IBC-SHJ, TOPCon and hole selective (MoO_x) SCs respectively. These results are closely comparable with experimental values. However, more advanced simulations tools with flexible handling, accuracy, high response are required for studying already developed SCs, creating new designs and innovative PV technologies.

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Availability of data and material

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Compliance with ethical standards

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Consent to participate

Not applicable

Consent to publication

The Author hereby confirms the consent to publication of the work in Journal of Microelectronic Engineering.

CRediT authorship contribution statement

Venkanna Kanneboina: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Software, Writing - original draft, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no conflict of interest.

Data availability

Data will be made available on request.

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