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An optimal low power digital controller for portable solar applications

N. Vijayalakshmi[1,a)] and P. Maruthupandi[2,b)]
[1]*Department of Electronics and Communication Engineering, Kathir College of Engineering, Coimbatore, India*
[2]*Department of Electrical Engineering, Government College of Technology, Coimbatore, India*

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The design of controllers for solar energy harvesting systems plays the key role in deciding the efficiency of the energy utilized. In applications of energy scavenging, the harvested power is consumed for about 70% in the operation of the converter and controller blocks before being supplied to the load. The proposed optimal Field Programmable Gate Array based Load Predictive Maximum Power Point Tracking (LP_MPPT) Digital Controller is used for low power, speedy, and decisive energy scavenging systems for a long run in applications of wireless or remote sensing or portable. LP_MPPT helps to predict the need of the load and generate the converter output as buck/boost/buck_boost mode power in comparison to the input from solar panels for every clock cycle. The power consumption of the controller section is comparatively reduced as the buck_boost mode of operation utilizes the no operation state. The proposed methodology is simulated and implemented using Xilinx ISE Design Suite 12.1 which is supported by the family SPARTAN 3E. The simulation results thus obtained show an increase in efficiency (94.3%) with trade off factors, namely, speed and area. *Published by AIP Publishing.*
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I. INTRODUCTION

The most inevitable topic in the present day globalization scenario is energy conservation and energy harvesting through nonconventional methods. The extremity in usage of fossil fuels has led the engineers and researchers to march forward towards hybrid energy generation methodologies such as wind, solar, geo thermal, biomass, and tidal. Generally, among the above methods, solar and wind energy generation methods prove to be easier and efficient methods, and hence, they are being used vastly in all sectors of energy needs where ever possible.[1] In the case of solar energy generation, its application varies from grid connected systems with some thousands of watts to wireless/remote electronics of few milli-watts.[2] Hence, it proves to be important to design optimal conversion and storage methodologies for low power operation in solar energy harvesting and scavenging systems. When the harvesting system consumes less power for its operation, then the produced photovoltaic (PV)–solar power is used efficiently for longer periods of non-illumination and lesser irradiance.[3] The power consumption by the solar energy production system is utilized among the converter block, controller block, and battery management systems and finally supplied to meet the load.[4] Maximum Power Point Tracking (MPPT) plays the key role in an effective operation of solar powered systems apart from geographical structures and irradiance and illumination parameters of the panels.[5] Numerous MPPT algorithms were designed and implemented by researchers all over the world successfully for effective generation of solar energy.[6]

[a)]viji365@gmail.com and vijayalakshmi_ece@kathir.ac.in
[b)]pandi@gct.ac.in

II. LITERATURE SURVEY

The perturbation and observation (P&O) algorithm[7,8] is most recurrently used due to its simplicity in structural design, lesser parameter consideration, and efficient decision making. This algorithm tracks the maximum power point by continuous iterations, perturbation, observations, and comparison with the obtained results of iteration for generating MPPT. The incremental conductance (Ic) algorithm[9] finds out MPPT by comparing and matching the incremental conductance (Ic) and instantaneous conductance (Inc). The hill climbing (HC) algorithm[10] is similar to that of the P&O algorithm in the decision making logics of comparing the present cycle with the previous cycle of power generated, and the former differs from the later by considering the duty cycle (D) as the parameter to determine the slope of P-V characteristics. The fractional open circuit voltage (FOCV) algorithm and the fractional closed circuit current (FCCI) algorithm[11] and MPPT have a linear relationship with OC-V and CC-I, respectively, under various geographical parameters. Other algorithms, such as Curve Fitting method, Differential Method, and soft computing, are also used as per their parametric necessity in some areas of solar energy harvesting.[12] In all the above-mentioned algorithms, the system generated power depends upon the voltage (Vpp) and current peak points (Ipp) of the photovoltaic array (PV-VPP and PV_Ipp). In contrast to other algorithms, the proposed algorithms not only depend upon PV-VPP and PV_Ipp but also the output from the converter (C_Vpp and C_Ipp) and the requirement of the load (L_Vpp and L_Ipp).

III. SYSTEM DESCRIPTION

The proposed field programmable gate array (FPGA) based load predictive maximum power point tracking (LP_MPPT) can be implemented with any type of DC/DC converter such as Buck, Boost, Buck_boost, and Inductor-less working with discontinuous mode of operation. The proposed block diagram (Fig. 1) consists of a PV array connected to a buck boost DC-DC converter. The converter in the proposed system works in buck/boost/buck_boost modes to fulfill the need of the varying DC load. The entire system operation is controlled by XC6SLX45 SPARTAN 3E FPGA. The mode of operation is decided by the proposed LP_MPPT controller based upon the feedback signals S1, C1, and L1.[25]

The parameters PV-VPP and PV_Ipp, _Vpp and C_Ipp, and L_Vpp and L_Ipp are analog quantities which are converted into digital before applying into the FPGA controller using ADC 0804. The digital control unit establishes a low cost unit when compared to the analog control unit and provides more accuracy comparatively.

The control signals of the LP_MPPT controller are applied to the MOSFET switches of the DC-DC converter section shown in Fig. 2, with a variable duty cycle Pulse Width Modulation (PWM) pulse to choose the operation of the converter as step up or step down of the input solar source.

Most of the MPPT controllers in energy scavenging use microcontrollers or digital signal processors (DSP). The proposed LP_MPPT controller enjoys the robustness, flexibility,

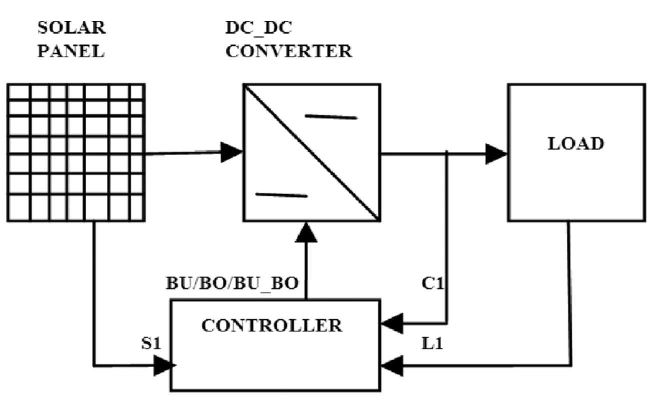

FIG. 1. Proposed block diagram.

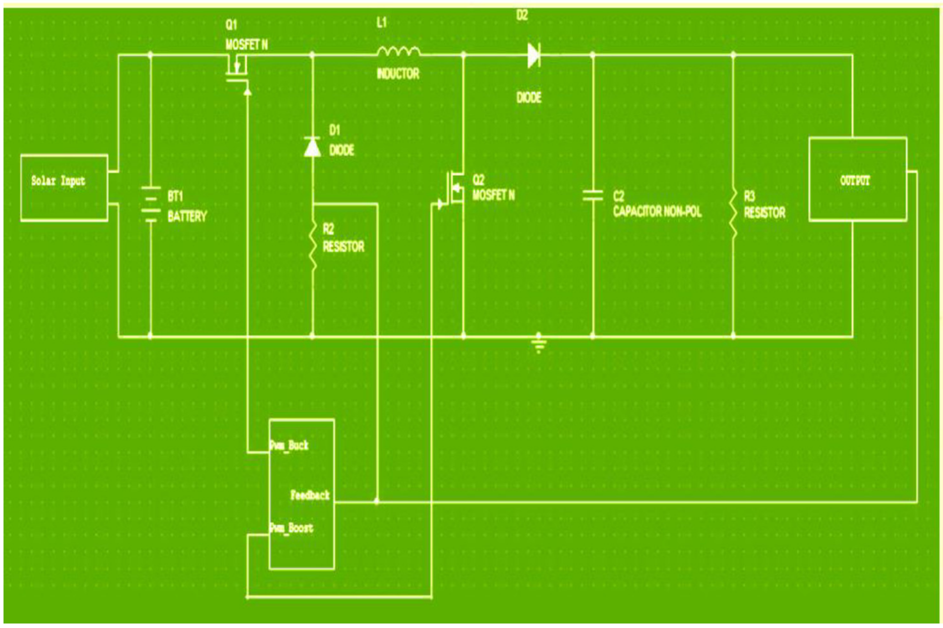

FIG. 2. Simulink model of the DC-DC converter section.

expandability, and testability along with offering the basic gate level designing that cannot be matched by any of the other DSP Microcontrollers.

Figure 3 depicts the algorithmic flow chart of the proposed LP_MPPT controller. In contrast to the available MPPT algorithms, the proposed methodology compares the system power requirements of the present clock cycle and previous clock cycle as per the load needs. The algorithm proves to be efficient in applications of energy scavenging and wireless remote devices, where low power operation plays the key role than the other trade off parameters.

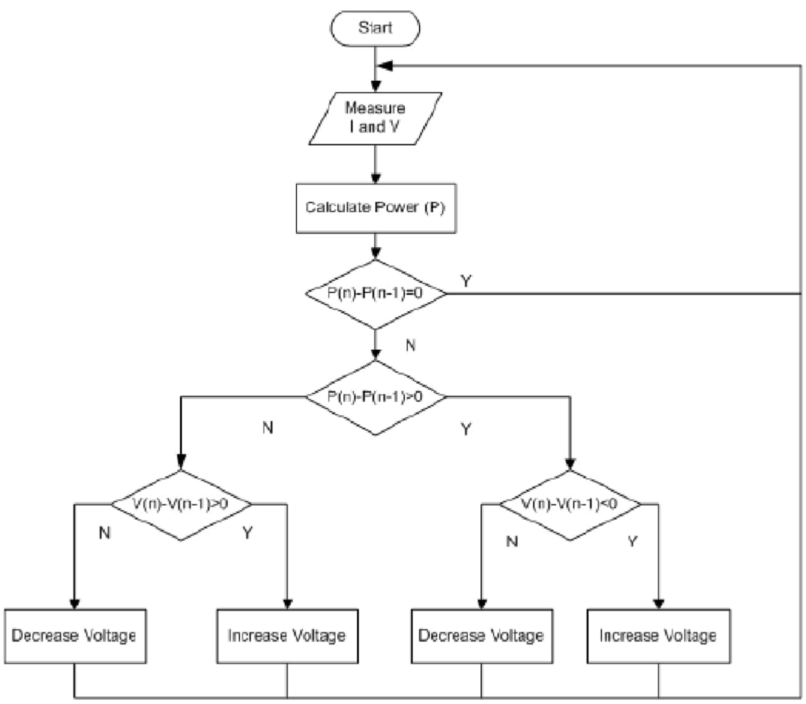

FIG. 3. Algorithmic flow chart for the proposed LP_MPPT controller.

IV. CONTROLLER OPERATION

The controller design is the heart of this work. The proposed LP-MPPT algorithm is developed in the Verilog VHDL coding module. The generated module is synthesized, implemented, and tested using ISE 12.1 of XILINX and family of SPARTAN 3E. The designed model acquires the input control signals from the PV array [S(0:3)], converter output [C(0:3)], and load [L(0:3)] and generates the gate control signal to the switches of the Buck boost converter through a varied duty cycle DPWM (Digital Pulse Width Modulation) pulse generator as shown in Fig. 4.

Modes of operation:

The proposed LP_MPPT controller helps to control the operation of the DC-DC converter in three basic modes as follows:

(a) Buck Mode (bu):

The buck mode of operation is carried out when both S (0:3) and C (0:3) are lesser than the L (0:3). The following conditional equation gives the buck mode of operation:

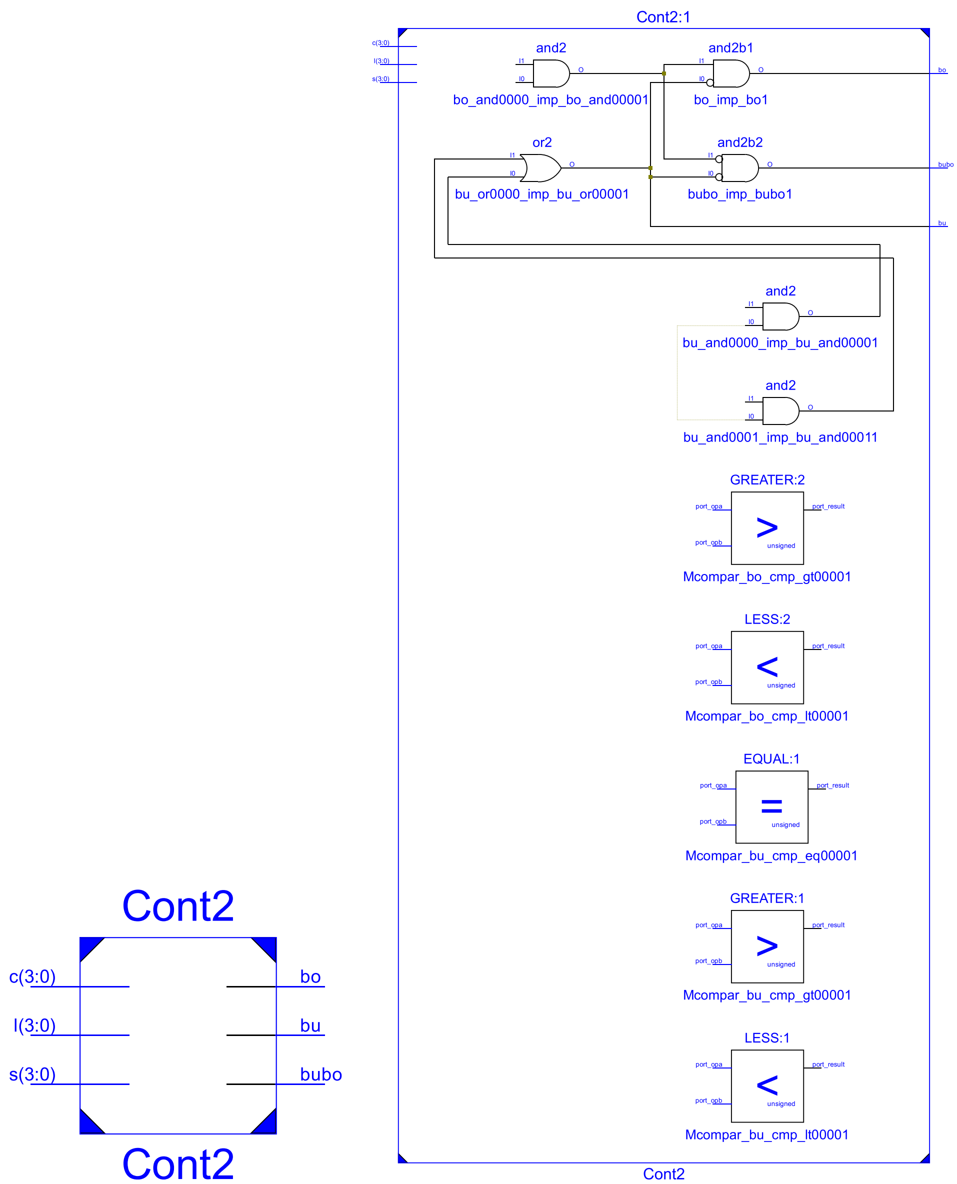

FIG. 4. (i) LP_MPPT controller design outline. (ii) RTL schematic of the LP_MPPT controller.

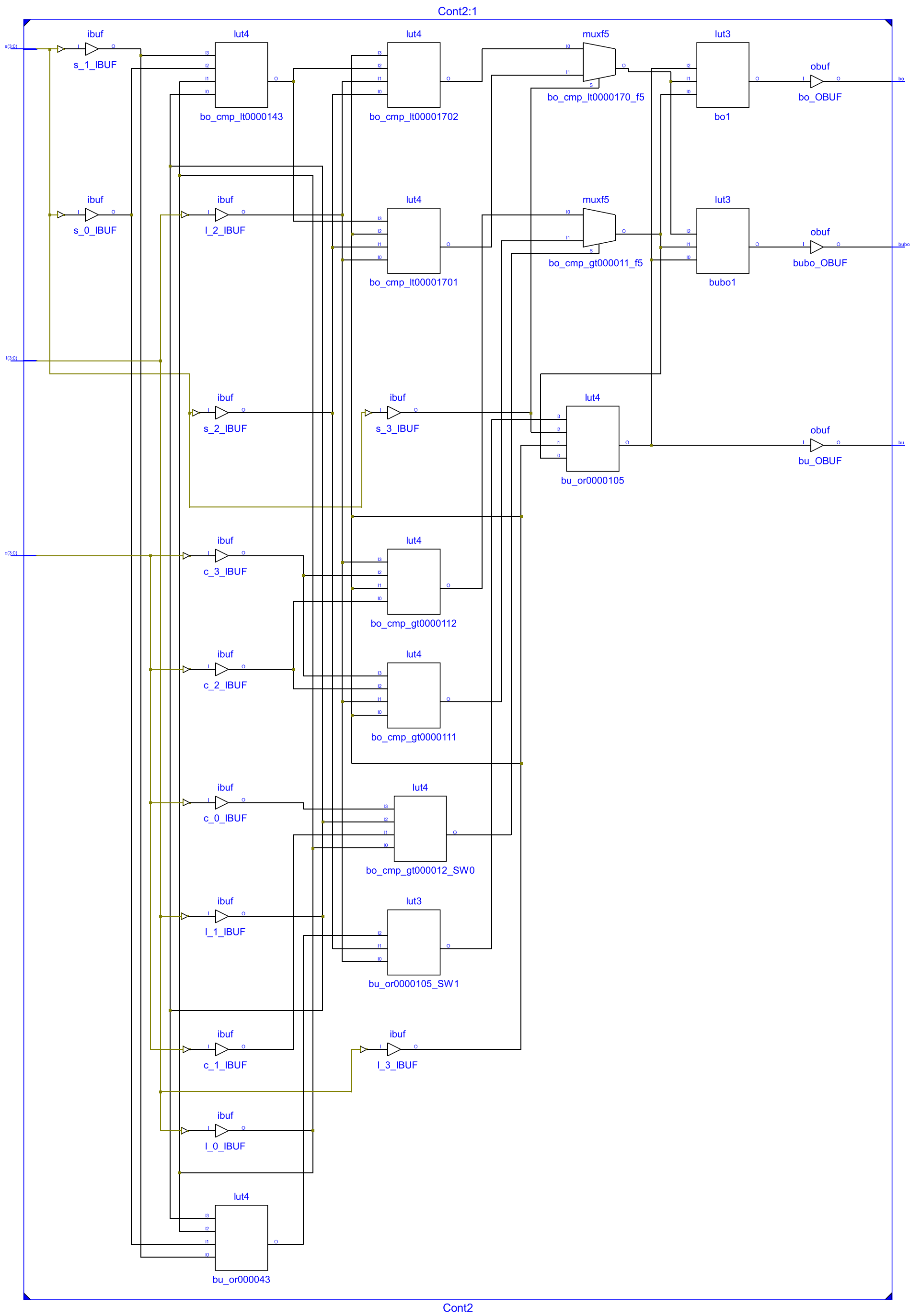

FIG. 5. Technical RTL model of the LP_MPPT controller.

TABLE I. Device utilization summary.

	Device utilization summary (proposed)			Device utilization summary[1]		
Logic utilization	Used	Available	Utilization (%)	Used	Available	Utilization (%)
Number of slices	6	2448	0.1	132	1536	8
Number of 4 input LUTs	11	4896	0.1	172	3072	5
Number of bonded IOBs	15	158	9	53	200	26

TABLE II. Critical review of the proposed system with existing works.

Work publication year	Converter type	Switching frequency	Cell power	MPPT	Hardware platform	Tracking speed
Proposed	Buck boost converter	200 kHz	59 W	LP_MPPT	FPGA XCS35250E	10.299 ns
2006[17]	DC/AC inverter	15 kHz	2 kW	INC	Microcontroller Intel 87196	500 ms
2006[21]	Boost converter	100 kHz	10 W	P&O	FPGA XC2C384	85 ms
2006[26]	Boost converter	500 kHz	85 W	Extremum-seeking	Analogue circuitry	20 ms
2008[18]	Push–pull converter	20 kHz	120 W	INC	DSP TMS320LF2407	250 ms
2011[16]	Boost converter	50 kHz	110 W	INR	Microcontroller C515C	500 ms
2011[20]	Buck converter	…	87 W	Voltage approximation line	Analogue circuitry	88 ms
2011[22]	Buck converter	100 kHz	20 W	Load current-based MPPT	DSP TMSF28335	80 ms
2011[30]	Boost converter	…	87 W	INC	PC Pentium-IV 2.4 GHz	16 ms
2012[14]	Buck converter	…	150 W	FLC-based P&O MPPT	DSP TMS320F28335	1.5 s
2012[15]	Boost converter	5 kHz	80 W	P&O	FPGA Quartus II	564 ms
2012[23]	DC/AC inverter	100 kHz	80 W	Distributed MPPT	Analogue circuitry	70 ms
2012[24]	Boost converter	…	55 W	Neuro-fuzzy (NFC)	FPGA Virtex II	30 ms
2012[27]	Two stage DC/DC converter	…	220 W	FLC	DSP TMS320F2812	20 ms
2012[29]	Boost converter	300 kHz	100 W	Extremum-seeking	Analogue circuitry	20 ms
2013[12]	Flyback converter	40 kHz	250 W	INC	Embedded controller dsPIC33FJ06GS202	5 s
2013[13]	Buck converter	…	50 W	INC	Microcontroller PIC18F4520	2 s
2013[19]	Boost converter	50–100 kHz	1.5 kW	P&O	FPGA XC4VLX60	100 ms
2013[28]	Boost converter	50 kHz	200 W	P&O-based PI	DSP TMS320F240	20 ms
2014[30]	Buck converter	100 kHz	80 W	INC	FPGA XC3S400	2.5 ms

$$\left(\left((s > l)\&(l == c)\right)||\left((s > 1)\&\&(l < c)\right)\right). \tag{1}$$

(b) Boost Mode (bo):
The boost mode of operation is carried out when both S (0:3) and C (0:3) are greater than the L (0:3). The following conditional equation gives the boost mode of operation:

$$\left((s < l)\&\&(l > c)\right). \tag{2}$$

(c) Buck_boost Mode (bubo)
The buck_boost mode of operation is carried out when the S (0:3) and C (0:3) are either greater or lesser than the L (0:3). The following conditional equation gives the Buck_buck mode of operation:

$$\left((s == l == c)\,||(s\&\&l < c)\,||\,(s < l\&\&\,c)\,||\,(s\&\&l > c)\right). \tag{3}$$

The Register Transfer Level (RTL) model of the proposed LP_MPPT controller is given in Fig. 5. Table I provides the resource summary of the LP_MPPT controller. It is evident from the summary that the power utilized for the controller is as low as **21%** and the speed of operation of the controller is **10.299 ns.**

The construction of Table II proves the comparison and literature review of the proposed LP_MPPT method with previous works with all necessary parameters to show the efficiency of the system generated.

V. SIMULATION RESULTS

The simulation waveforms of the LP_MPPT controller are shown in Fig. 6. From the simulation results, it is explicitly identified that the controller operates in the bubo mode for most of the clock cycles which in turn denotes the impedance state (z) or no operation (nop) state of the system till next clock cycle comparisons.

The power analysis of the proposed method from the snap shot of the XPOWER Analyser in Fig. 7 is evident to show the consumed power of the system, and Fig. 8 shows the buck and boost mode of operation. Table III gives the efficiency of the proposed system with a reduction in the ripple.

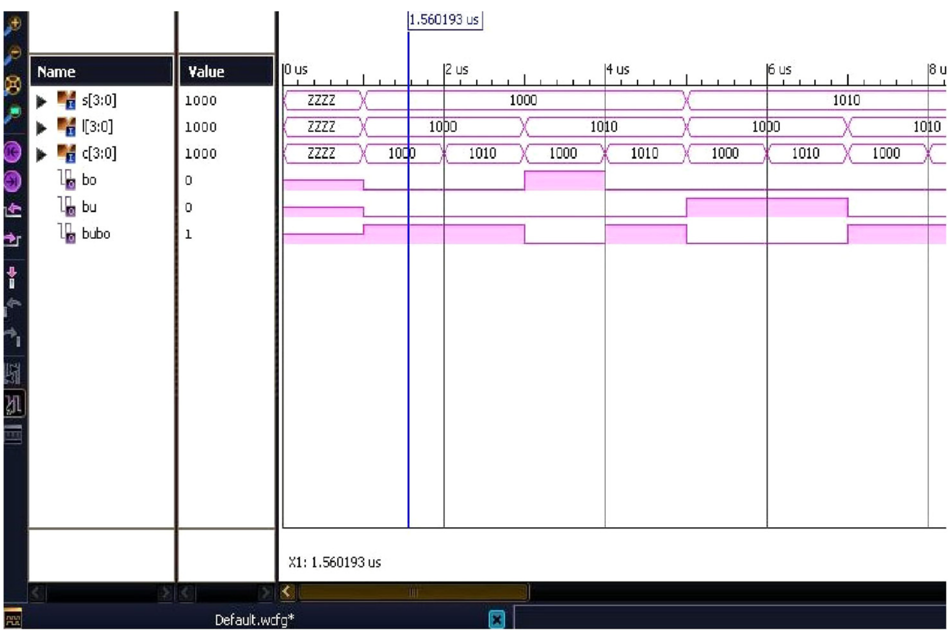

FIG. 6. Simulation results of the LP_MPPT controller.

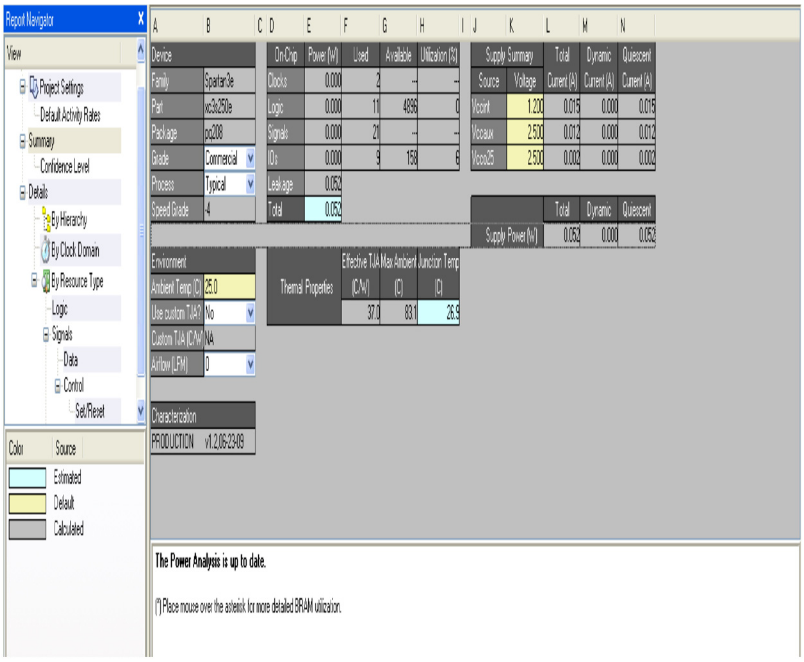

FIG. 7. Power Analysis of the LP_MPPT controller.

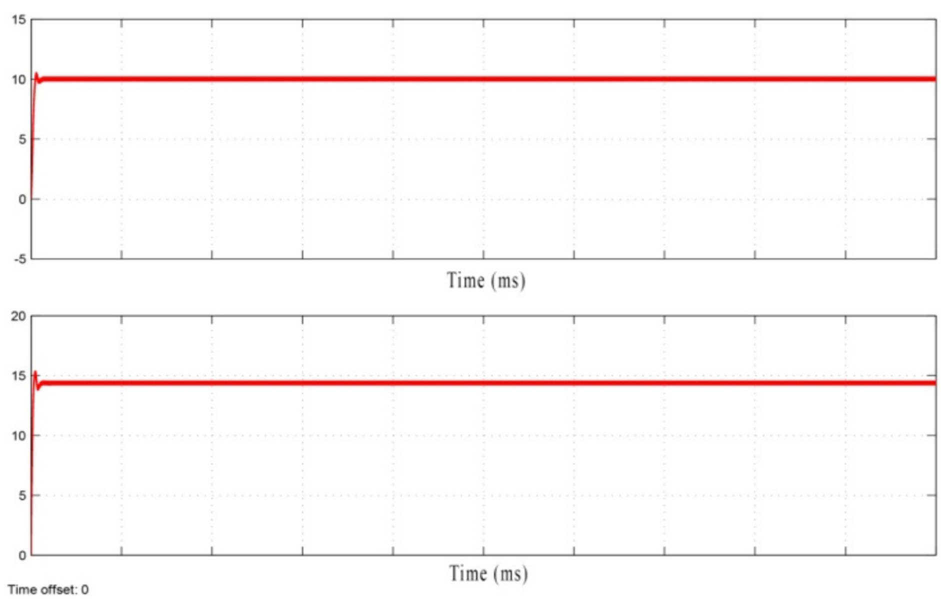

FIG. 8. (i) Boost mode V_{in} (ii) buck mode V_{in}.

TABLE III. Performance comparison of the converter after addition of the LP_MPPT FPGA based controller.

Parameters	Buck/boost	SEPIC/ZETA	Proposed system
Output voltage	Non-inverted	Non-inverted	Non-inverted
Settling time	0.2	0.9	0.2
Ripple current in load	1.82	1.56	0.45
Rise time	0.06	0.4	0.04
Transients in output	68%	52%	>50%
Efficiency	74%	82%	94.3%

VI. CONCLUSION

The proposed FPGA based LP_MPPT controller helps in real time application of tracking the Peak power point of the PV array output so as to make use of the maximum power without wasting them in the internal circuitry of the controller itself. The proposed method is most suited in areas of energy scavenging and remote applications as the proposal of the idle state (nop) for the converter helps in a very low operation strategy. The efficiency of the proposed LP_MPPT controller is 94.3%. A compromise has to be made in the case of fast changing climatic conditions which may demand an increase in the switching speed of the modes which in turn reduces the efficiency. In the near future, a suitable FPGA based controller coping up the rapid environment changes will be designed.

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