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# Effect of oxide thickness on the capacitance and conductance characteristics of MOS structures

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**Abstract**

In this work, the investigation of the interface states density and series resistance from capacitance–voltage ($C$–$V$) and conductance–voltage ($G$–$V$) characteristics in Au/$SnO_2$/n-Si (MOS) structures prepared at various $SnO_2$ layer thicknesses by spray deposition technique have been reported. It is fabricated five samples depending on deposition time. The thicknesses of $SnO_2$ films obtained from the measurement of the oxide capacitance in the strong accumulation region for MOS Schottky diodes are 37, 79, 274, 401, and 446 Å, for D1, D2, D3, D4, and D5 samples, respectively. The $C$–$V$ and $G$–$V$ measurements of Au/$SnO_2$/n-Si MOS structures are performed in the voltage range from −6 to +10 V and the frequency range from 500 Hz to 10 MHz at room temperature. It is observed that peaks in the forward $C$–$V$ characteristics appeared because of the series resistance. It has been seen that the value of the series resistance $R_s$ of samples D1 (47 Ω), D2 (64 Ω), D3 (98 Ω), D4 (151 Ω), and D5 (163 Ω) increases with increasing the oxide layer thickness. The interface state density $D_{it}$ ranges from $2.40 \times 10^{13}\,cm^{-2}\,eV^{-1}$ for D1 sample to $2.73 \times 10^{12}\,cm^{-2}\,eV^{-1}$ for D5 sample and increases with increasing the oxide layer thickness.
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*Keywords:* MOS schottky diodes; $SnO_2$; $C$–$V$; $G$–$V$; Series resistance; Interface states

## 1. Introduction

Tin oxide thin films ($SnO_2$) are technologically important materials and found application in areas such as gas sensors [1], heat reflectors [2], flat display devices [3], photovoltaic cells [4], dye-based solar cells [5], thin film transistors, computer touch screens, and opto-electronic devices and so on. Since the properties of the material are strongly dependent on the procedure of preparation, different techniques have been employed to obtain $SnO_2$ thin films. These include electron beam evaporation, reactive thermal evaporation, dip coating, chemical vapor deposition, r.f. magnetron sputtering, sol–gel, spray deposition. Among these, the spray deposition process presents an easy way to integrate $SnO_2$ devices into the Si technology, since it offers the possibility of good control of the deposition parameters, low processing temperatures and low production costs. The metal–semiconductor (MS) contact is one of the most widely used rectifying contacts in device technology [6,7]. The existence of such an oxide layer ($SnO_2$) converts the device to a metal–oxide–semiconductor (MOS) diode [8–10] and may have a strong influence on the diode characteristics as well as a change of the interface state charge with bias which will give rise to an additional field in the interfacial layer [11]. Interface states at the Si–$SiO_2$ interface have been studied in detail because of their effects on the reliability and quality of MOS diodes [11–26]. Especially, the formation and characterization of $SnO_2$ insulator layers on Si still remains a basic problem. In the case of $SnO_2$/Si interface, it is proposed that the structure behaves like a Schottky barrier diode [8–10].

Various measurement techniques [13,27–31] for determining the interface state density traps have been developed and among them the important one is Hill–Coleman technique [31]. This technique proposed by Hill and Coleman [31] is a powerful tool to deduce interface state density $D_{it}$, which is useful in estimating the interface charge and has been used by some authors [20,32,33]. The forward bias capacitance–voltage ($C$–$V$) and conductance–voltage

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($G$–$V$) measurements give the important information about the density or energy distribution of the interface states of the structure. In general, the $C$–$V$ and $G$–$V$ plots in the idealized case are frequency independent [6,7,18–21]. However, this idealized case is often disturbed due to the presence of an interfacial layer between the contact materials and interface states at the oxide layer/semiconductor interface [7,18–21]. Chattopadhyay and Daw [22] studied the capacitance of Schottky barrier diodes (Cu–$SiO_2$–p-Si) and observed an anomalous peak in the forward bias $C$–$V$ characteristics. The peak values of capacitance depend on a number of parameters such as the interface states density, series resistance and the thickness of the interfacial insulator layer. Ho et al. [23] studied the capacitance of Pd–Si Schottky contacts and observed an anomalous peak in the forward $C$–$V$ characteristics. They attributed this anomalous feature to interface states. Chattopadhyay and Raychaudhuri [24–26] investigated the $C$–$V$ characteristics of Schottky barrier diodes considering the series resistance effect. It has been shown that, in the presence of a series resistance, the $C$–$V$ characteristics should exhibit a peak. The peak value of the capacitance depends on a number of parameters such as the interfacial oxide layer thickness, interface state density and doping. Based on the above work, a technique has been developed which estimates the series resistance of the device [25]. The model proposed in Ref. [24], however, investigates only the $C$–$V$ plot in the high-frequency limit when interface states cannot follow the a.c. signal.

In our previous studies [8,9,34], we studied substrate temperature dependence of series resistance and energy distribution of the interface states density from current–voltage ($I$–$V$) characteristics in Al/$SnO_2$/p-Si Schottky diodes and electrical, structural and optical properties of $SnO_2$ films prepared by spray deposition method. In this paper, in order to achieve a better understand of the effects of surface states and series resistance on Au/$SnO_2$/n-Si Schottky diodes prepared at different oxide layer ($SnO_2$) thicknesses (37–446 Å) by spray deposition method, the $C$–$V$ and $G$–$V$ characteristics for a wide frequency range (500 Hz–10 MHz) at room temperature in dark have been measured and reported the first investigation of the interface states density and series resistance from capacitance and conductance characteristics in Au/$SnO_2$/n-Si (MOS) structures prepared at different $SnO_2$ layer thicknesses by spray deposition technique. Also, the aim of this research was to establish a relationship between the oxide ($SnO_2$) layer thickness and the characteristics parameters determined from the admittance-based measured methods ($C$–$V$ and $G/\omega$–$V$). In order to realize this goal, tin oxide films on n-Si were prepared by a spraying method at different oxide layer thicknesses.

## 2. Experimental procedure

The MOS (Au/$SnO_2$/n-Si) structures used in this work were fabricated using n-type (P-doped) single crystals silicon wafer with (1 1 1) surface orientation, 300 μm thick, and 5–10 Ω cm resistivity. The Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of $H_2SO_4$ an $H_2O_2$, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20%HF. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of resistivity of 18 MΩ cm. Before ohmic contact formed on the n-type Si substrate, the samples were dipped in dilute HF:$H_2O$ (1:10) about 20 s to remove any native thin oxide layer on the surface, finally the wafer was rinsed by ultrasonic vibration in deionized water. After surface cleaning, gold (Au, 99.999%) metal with a thickness of 2500 Å for ohmic contacts was thermally evaporated on the back of the wafer in a vacuum-coating unit of $1\times10^{-6}$ Torr. Low-resistance ohmic contacts were formed by thermal annealing at 450 °C for 5 min in flowing $N_2$ in a quartz tube furnace and then the wafer was cut into five pieces of about $5\times5\,mm^2$. After ohmic contact, a layer of $SnO_2$ was grown on the Si substrate by spraying a solution consisting of 32.21 wt% of ethyl alcohol ($C_2H_5OH$), 40.35 wt% of deionized water ($H_2O$) and 27.44 wt% of stannic chloride ($SnCl_4\cdot5H_2O$) on the substrate, which was maintained at a constant temperature of 400 °C. The $SnO_2$ films prepared on Si wafer at 5, 10, 15, 20, and 25 s deposition times are denoted by D1, D2, D3, D4, and D5 samples, respectively. The temperature of the substrates was monitored by chromel–alumel thermocouple fixed on top surface of the substrate. The variation of the substrate temperature during spray was maintained within ±5 °C with the help of a temperature controller. The rate of spraying was kept at about $30\,cm^3\,min^{-1}$ by controlling the carrier gas flow meter. $N_2$ was used as the carrier gas. $SnO_2$ dots were 3 mm in diameter. After spraying process, circular dots of 1 mm in diameter and 2500 Å thick Au rectifying contacts were deposited onto the $SnO_2$ surface of the wafer through a metal shadow mask in liquid nitrogen trapped ultra-high vacuum system in the pressure of $1\times10^{-6}$ Torr. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The deposition rates were about 5–10 Å $s^{-1}$. The thicknesses of $SnO_2$ films obtained from the measurement of the oxide capacitance in the strong accumulation region for MOS Schottky diodes were 37, 79, 274, 401, and 446 Å, for D1, D2, D3, D4, and D5 samples, respectively. The $C$–$V$ and $G$–$V$ measurements were performed at wide frequency range (500 Hz–10 MHz) by using HP 4192A LF impedance analyzer at the room temperature in dark and the test signal of 40 $mV_{rms}$ [13].

## 3. Results and discussion

Fig. 1(a) and (b) show the voltage dependence of the measured $C$–$V$ and $G/\omega$–$V$ characteristics for D1, D2, D3, D4, and D5 Au/$SnO_2$/n-Si MOS diodes fabricated at different oxide layer thicknesses at 1 MHz at room temperature. The bias voltage was varied between −6

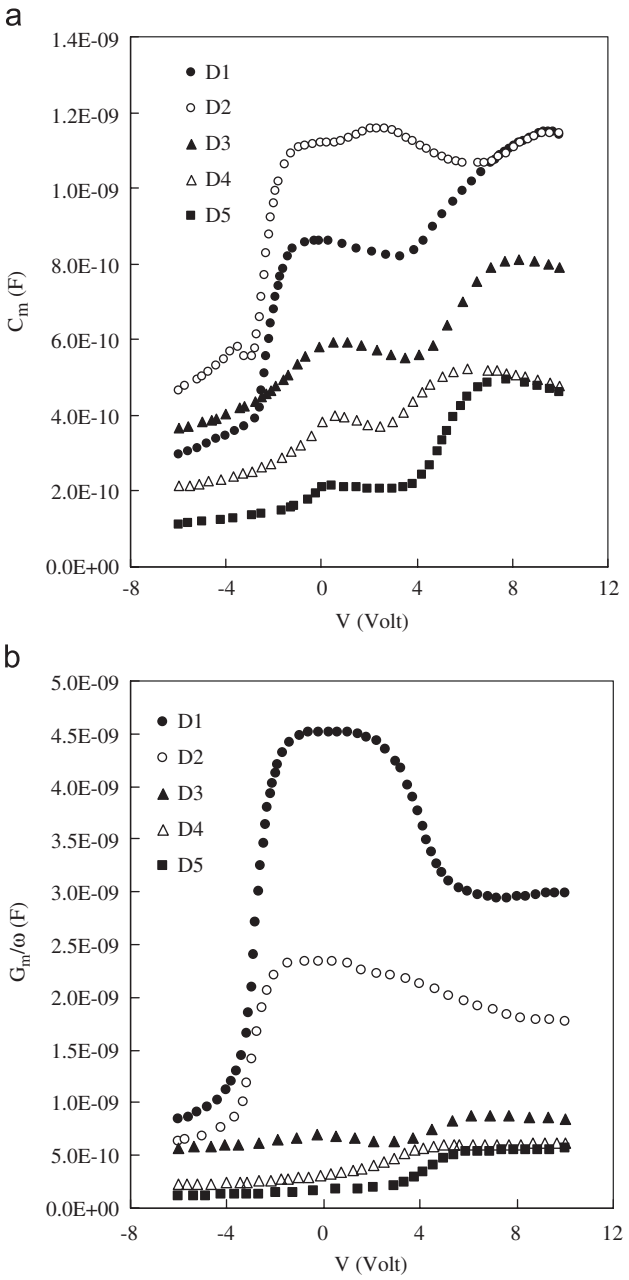


Fig. 1. (a) The measured capacitance ($C$) and (b) conductance ($G/\omega$) characteristics versus gate bias at frequency of 1 MHz at room temperature for (the samples D1–D5) Au/$SnO_2$/n-Si MOS structures prepared at different oxide ($SnO_2$) layer thicknesses by spray deposition technique.

and +10 VDC for all samples. It is seen from Fig. 1(a) that the values of the capacitance increase with increasing voltage for all samples and decrease with increasing oxide layer thickness (except D2 sample). As shown in Fig. 1(a) and (b), both $C$–$V$ and $G/\omega$–$V$ curves have three regimes of accumulation–depletion–inversion region. Also, the $C$–$V$ curves have two peaks in the depletion region for all samples. Such behavior of the capacitance peaks is attributed to particular distribution of surface states between $SnO_2$/Si interfaces. Therefore, there may be a capacitance due to interface states in excess to depletion layer capacitance. It is also shown in Fig. 1(a) that the change in the oxide layer thickness has effects on the values and positions of these anomalous peaks. The value of the capacitance at peak decreases with increasing oxide layer thickness and the first peak position shifts towards a lower voltage. The presence of the capacitance peak in the forward $C$–$V$ plot is investigated by a number of experimental results on MOS structures [22–26,35,36]. The origin of such a peak has been ascribed to the interface states by Ho et al. [23], and Chattopadhyay and Raychaudhuri [24–26] to the series resistance effect. The values of the capacitance and conductance depend on a number of parameters such as the thickness and formation of the oxide layer, series resistance and energy distribution or density of interface states. The effect of interface state density can be eliminated when the $C$–$V$ and $G/\omega$–$V$ curves are measured at sufficiently high frequency ($f \geqslant 500$ kHz) [6–9,11], since the charges at the interface states cannot follow an a.c. signal [11]. In this case, the interface states are in equilibrium with the semiconductor. From the above discussion the series resistance ($R_s$) seems the most important parameter, which causes the electrical characteristics of MOS structures to be non-ideal [11,35].

Fig. 2(a) and (b) depicts the capacitance ($C$) and conductance ($G/\omega$) as a function of frequency in 9.5, 9.5, 8, 6 and 7.5 V for D1, D2, D3, D4 and D5 samples, respectively. The values of voltage are determined from the second peak position in the strong accumulation. As seen from Fig. 2(a) and (b), the measured $C$ and $G/\omega$ for all samples decrease with increasing frequency in the frequency range from 500 Hz to 10 MHz and also remains almost constant after 100 kHz in the $G/\omega$ curves for all samples. This occurs because at lower frequencies the interface states can follow the a.c. signal and yield an excess capacitance, which depends on the frequency. In the high-frequency limit, however, the interface states cannot follow the a.c. signal. This makes the contribution of interface state capacitance to the total capacitance negligibly small. This behavior is also attributed to the presence of a continuous distribution of $D_{it}$, which leads to a progressive decrease of the response of the $D_{it}$ to the applied a.c. voltage [11,22–26]. Besides the higher values of $C$ and $G/\omega$ at low frequency are due to excess capacitance and conductance resulting from the $D_{it}$ in equilibrium with the semiconductor that can follow the a.c. signal. It can be concluded that under reverse bias the interface states are responsible for the observed frequency dispersion in $C(V)$ and $G/\omega(V)$ curves.

The real series resistance of MOS Schottky diodes can be determined from the measured capacitance ($C_{ma}$) and conductance ($G_{ma}$) in strong accumulation region at high frequency (500 kHz$\leqslant f$) [8,9,11,13,18,30]. At sufficiently high frequency, to determine series resistance, when the MOS structure is biased into strong accumulation, the admittance ($Y_{ma}$) is given by [11]

$$Y_{ma} = G_{ma} + j\omega C_{ma}. \quad (1)$$

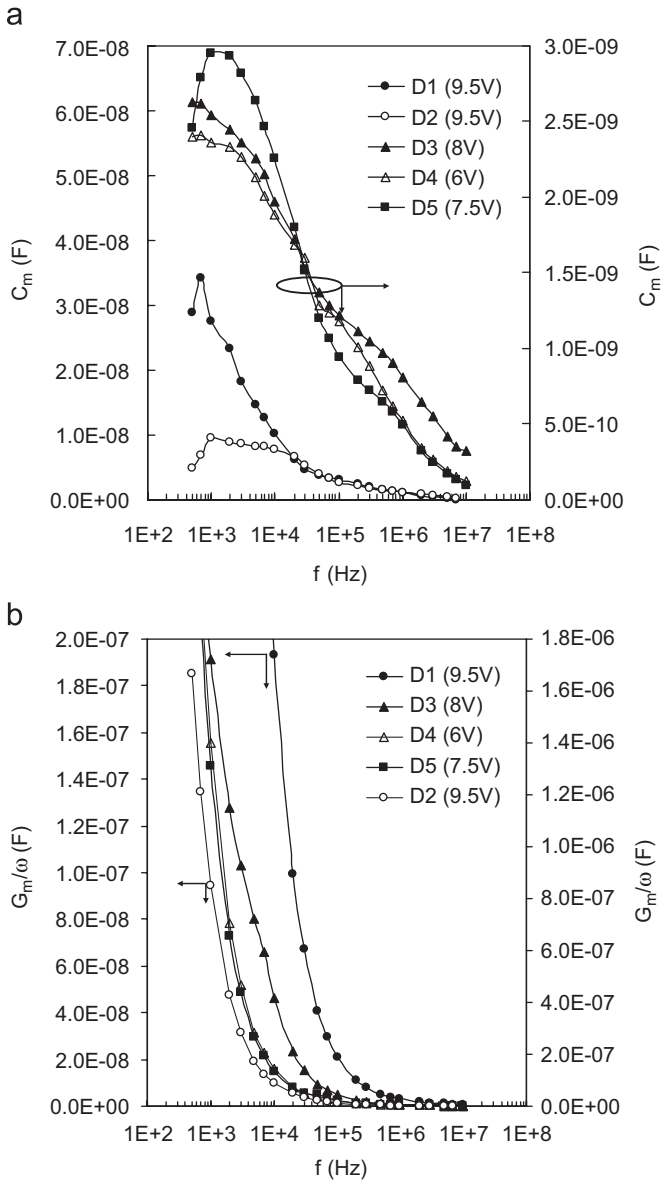


Fig. 2. (a) The $C(V)$–$f$ and (b) $G/\omega(V)$–$f$ characteristics for different forward bias at room temperature for all samples.

Comparing the real and imaginary parts of admittance, the series resistance of MOS structure is given by [11]

$$R_s = \frac{G_{acc}}{G_{acc}^2 + \omega^2 C_{acc}^2}, \quad (2)$$

where $C_{acc}$ and $G_{acc}$ are defined as the measured capacitance and conductance in strong accumulation region. The series resistance is estimated according to Eq. (2) and the voltage dependence of $R_s$ at 1 MHz for all samples is plotted in Fig. 3(a). These very significant values demanded that special attention be given to effects of the series resistance in the application of the admittance-based measured methods ($C$–$V$ and $G/\omega$–$V$). It is clearly seen in Fig. 3(a) that the series resistance is independent of voltage at positive voltage for D1 and D2 samples and gives a peak for D3–D5 samples and also remains almost constant after

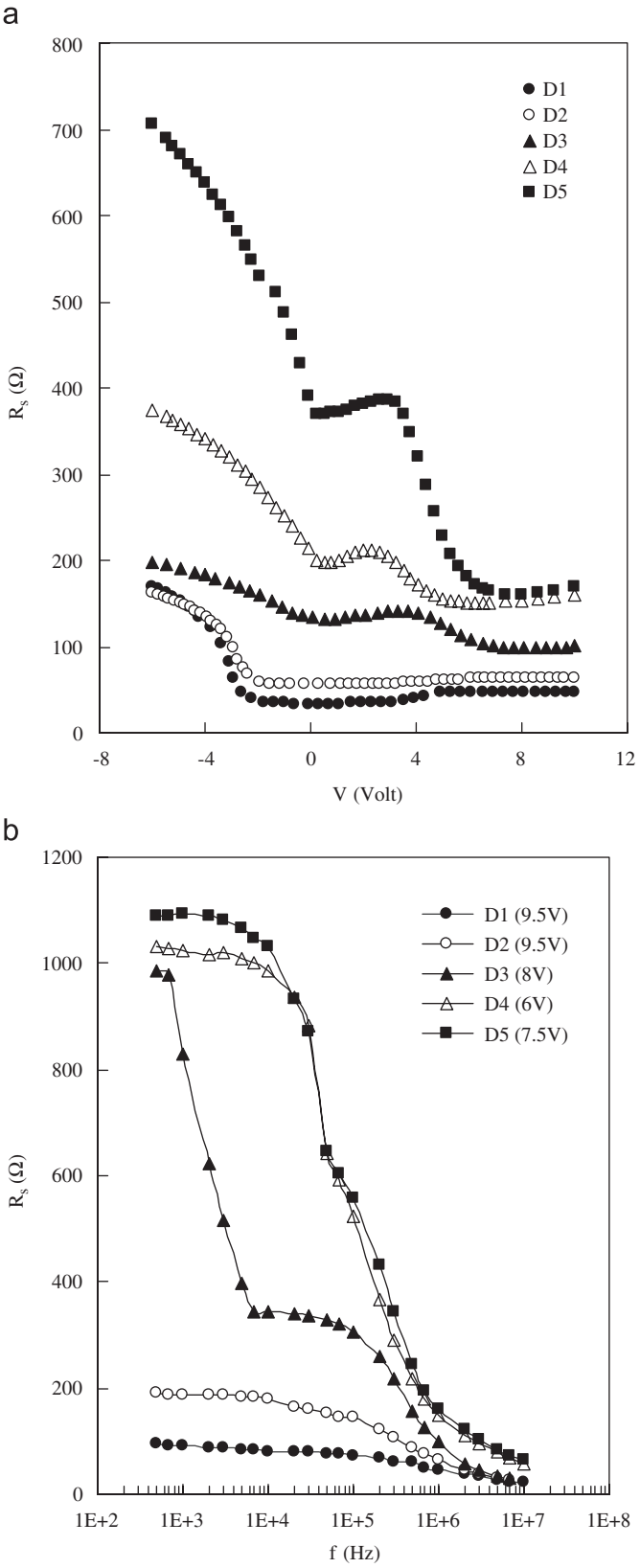


Fig. 3. (a) The voltage and (b) frequency dependence of the series resistance for all samples at frequency of 1 MHz at room temperature.

7 V for all samples. It is seen from Fig. 3(a) that the values of the series resistance increase with increasing oxide layer thickness. The series resistance values of Au/$SnO_2$/n-Si

MOS structure are calculated at strong accumulation region at 1 MHz and varied to be about 47, 64, 98, 151 and 163 Ω for D1, D2, D3, D4 and D5 samples, respectively, and plotted as a function of oxide layer thickness in Fig. 4. As seen in Fig. 4, the series resistance value of the samples D1–D5 increase with increasing oxide layer thickness. Fig. 3(b) depicts the series resistance ($R_s$) curves of Au/$SnO_2$/n-Si MOS structure in the frequency range of 500 kHz to 10 MHz at room temperature. From Fig. 3(b), it is clearly seen that the series resistance $R_s$ for all samples decrease with increasing frequency in the frequency range form 500 Hz to 10 MHz.

The corrected capacitance ($C_c$) and corrected equivalent parallel conductance ($G_c$) values of the MOS Schottky diodes corrected for series resistance are obtained as a function of angular frequency from the direct measured $C_m$ and $G_m$ according to

$$C_c = \frac{[G_m^2 + \omega^2 C_m^2]C_m}{a^2 + \omega^2 C_m^2} \tag{3}$$

and

$$G_c = \frac{[G_m^2 + \omega^2 C_m^2]a}{a^2 + \omega^2 C_m^2}, \tag{4}$$

where $a = G_m - [G_m^2 + \omega^2 C_m^2]R_s$.

The oxide layer capacitance ($C_{ox}$) values of 13, 6.16, 1.78, 1.21 and 1.09 nF for samples D1, D2, D3, D4 and D5, respectively, are obtained by substituting $R_s$ from Eq. (2) into the relation $C_{acc} = C_{ox}/(1 + \omega^2 R_s^2 C_{ox}^2)$ and solved for $C_{ox}$ which yields $C_{ox} = C_{acc}[1 + ((G_{acc})/\omega C_{acc})^2]$. The oxide ($SnO_2$) thickness $\delta$ is calculated from high frequency (1 MHz) $C$–$V$ data in strong accumulation using the equation for oxide layer capacitance ($C_{ox} = \varepsilon_i \varepsilon_0 A/\delta$), where $\varepsilon_i = 7\varepsilon_0$ [8,9] and $\varepsilon_0$ are the permittivity of the interfacial insulator layer and free space, has been determined to be about 37, 79, 274, 401, and 446 Å, for D1, D2, D3, D4, and D5 samples, respectively.

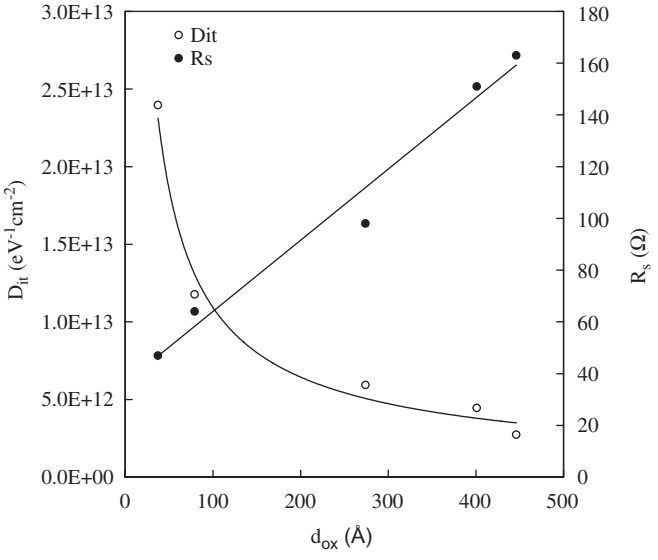


Fig. 4. The interface state density and series resistance versus oxide layer thickness curves of Au/$SnO_2$/n-Si MOS structure.

From Figs. 1 and 2, it is clearly seen that in the depletion and inversion region measured $C$–$V$ and $G/\omega$–$V$ are dependent on voltage and frequency, respectively. Therefore, to obtain the real diode capacitance $C_c$ and conductance $G_c/\omega$, the high-frequency (1 MHz) capacitance measured under forward and reverse bias is corrected for the effect of series resistance using Eqs. (3) and (4), respectively. Fig. 5(a) and (b) depicts the voltage dependence of the corrected capacitance $C_c$ and conductance $G_c/\omega$ characteristics for D3 sample at 1 MHz at room temperature. As seen from Fig. 5(b), it is clearly seen that the $G_c/\omega$–$V$ characteristic of D3 sample consists of a peak. The value of interface states density ($D_{it}$) is determined from this peak value. This peak is observed for all samples.

The application of a single-frequency approximation method [31] allows estimation of the density of interface states from the $G$–$V$ measurements. A fast and reliable way to determine the density of interface states ($D_{it}$) is the Hill–Coleman method [31] and confirmed by Konofaos [32] and Dakhel [33]. According to this method, $D_{it}$ can be calculated using the following formula:

$$D_{it} = \frac{2}{qA}\frac{G_{m,max}/\omega}{[(G_{m,max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]}, \tag{5}$$

where $q$ is the elementary electrical charge, $A$ is the area of the diode, $\omega$ is the angular frequency, $C_{ox}$ is the capacitance of oxide layer in strong accumulation region, $G_{m,max}$ conforms to maximum measured $G$–$V$ curve, and $C_m$ is the capacitance of the diodes corresponding to $G_{m,max}$.

This method is applied on $G$–$V$ curves of the frequency of 1 MHz. Fig. 5(b) depicts the $G$–$V$ curves of sample D3. The curve shown is for the as-measured data with the effects of series resistance being corrected for and this is the one used for the $D_{it}$ calculation via the Hill–Coleman equation. The peaks correspond to the depletion area of the device and its existence verifies the presence of interface traps [11,31–33]. Similar curves are obtained for all samples, verifying the MOS behavior with interface states. This method is very useful in understanding the electrical quality of the interface and the obtained values of the interface states are shown in Fig. 4. As seen from Fig. 4, the interface state density value of the samples D1–D5 decreased with increasing oxide layer thickness. The interface state density ($D_{it}$) values of 24.0, 11.8, 5.94, 4.46 and $2.73 \times 10^{12}\,eV^{-1}\,cm^{-2}$ for samples D1, D2, D3, D4 and D5, respectively, are obtained. However, the calculated values of $D_{it}$ ($\approx 10^{12}\,eV^{-1}\,cm^{-2}$) is not high enough to pin the Fermi level of the Si substrate disrupting the device operation [32,33]. Consequently, the interface traps and defects cannot prevent the construction of an MOS device. The values obtained for $D_{it}$ are of the same order as those reported by some authors for Schottky diodes [9,26,32,33,37,38].

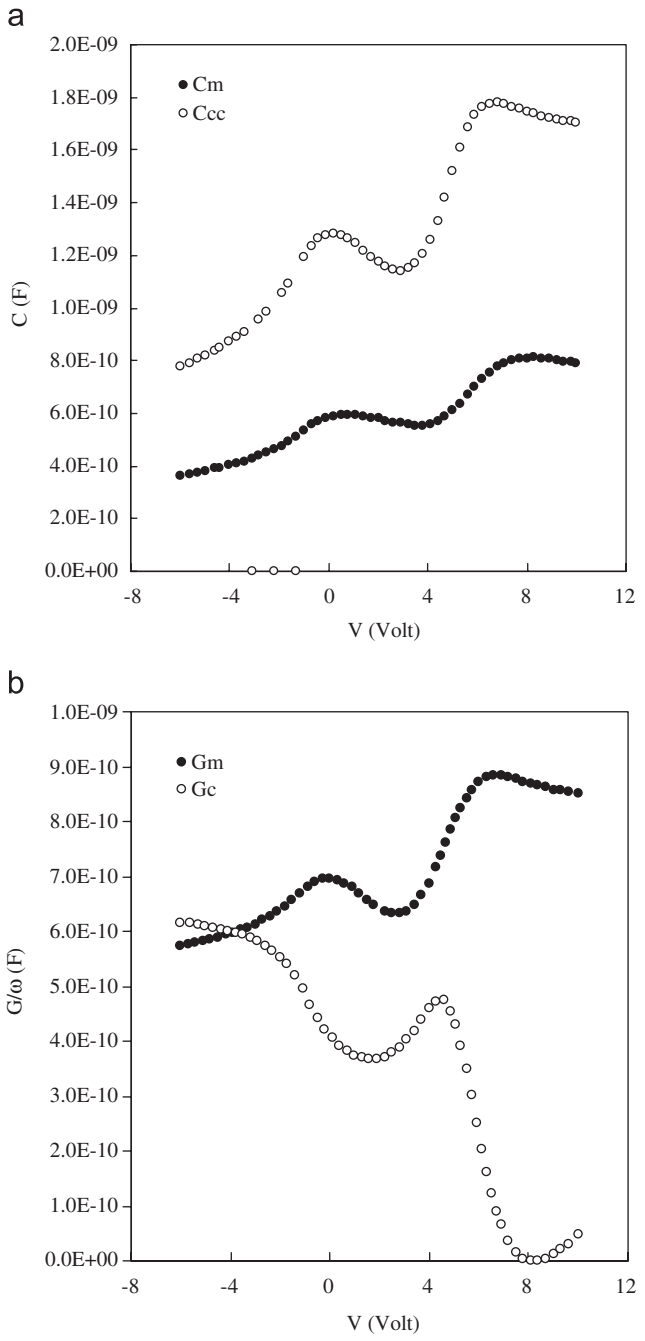


Fig. 5. The voltage-dependent plots of the corrected: (a) high-frequency (1 MHz) capacitance ($C$) and (b) conductance ($G/\omega$) curves at room temperature for one of the samples (D3).

## 4. Conclusions

The forward and reverse bias capacitance–voltage ($C$–$V$) and conductance–voltage ($G/\omega$–$V$) characteristics of Au/$SnO_2$/n-Si MOS diodes prepared at five different oxide ($SnO_2$) layer thicknesses by spray deposition method were measured in the frequency range of 500 Hz–10 MHz. The effects of the series resistance ($R_s$) and interface state density ($D_{it}$) of Au/$SnO_2$/n-Si MOS diodes on $C$–$V$ and $G$–$V$ characteristics are investigated. The series resistance values of Au/$SnO_2$/n-Si MOS structure calculated at strong accumulation region at 1 MHz and varied to be about 47, 64, 98, 151 and 163 Ω for D1, D2, D3, D4 and D5 samples, respectively, and increased with increasing oxide layer thickness. It is found that both capacitance and conductance were quite sensitive to frequency, especially at relatively low frequency, and the capacitance, conductance, and series resistance decrease with increasing frequency. The higher values of capacitance at low frequencies were attributed to the excess capacitance resulting from the $D_{it}$, which are in equilibrium with the semiconductor that can follow the a.c. signal. The values of the interface state density located in the n-Si band gap at the $SnO_2$/n-Si interface prepared in the different oxide layer thicknesses, 24.00, 11.80, 5.94, 4.46 and $2.73\times10^{12}\,eV^{-1}\,cm^{-2}$ for samples D1 (37 Å), D2 (79 Å), D3 (274 Å), D4 (401 Å) and D5 (446 Å), respectively, has been determined. It is found that the calculated values of $D_{it}$ ($\approx10^{12}\,eV^{-1}\,cm^{-2}$) is not high enough to pin the Fermi level of the Si substrate disrupting the device operation and also the density of interface states for Au/$SnO_2$/n-Si diodes is high when compared to insulators such as $SiO_2$.

We conclude that prepared Au/$SnO_2$/n-Si MOS Schottky diodes have been controlled by the insulator layer and interface states, which are responsible for the non-ideal behavior of $C$–$V$ characteristics and can also conclude a correlation between the interface layer in the contact metal–silicon and series resistance effect. The oxide ($SnO_2$) layer thickness reduces the interface state density and consequently the series resistance increases.

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