ISSN 1063-7826, Semiconductors, 2020, Vol. 54, No. 10, pp. 1296–1303. © Pleiades Publishing, Ltd., 2020.

PHYSICS OF SEMICONDUCTOR DEVICES

Characterization of Deep Levels in AlGaN|GaN HEMT by FT-DLTS and Current DLTS

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Received May 3, 2020; revised May 3, 2020; accepted June 17, 2020

Abstract—In this work, GaN|AlGaN high electron mobility transistor (HEMT) structures are investigated, grown on semi-insulating SiC substrates by molecular beam epitaxy and metal–organic chemical-vapor deposition techniques. This paper reports on the kink effect and hysteresis effect observed in AlGaN|GaN high electron mobility transistors (HEMTs) on SiC substrate. It is well known that trapping effects can limit the output power performance of microwave HEMTs, which is particularly true for the wide band gap devices. A detailed study is presented of FT-DLTS and CDLTS measurements performed on AlGaN|GaN HEMTs. It is demonstrated that the kink effect is directly correlated to shallow traps, and a remarkable correlation exists between deep levels observed by CDLTS and FT-DLTS and the presence of parasitic effects such as kink and hysteresis effects.

Keywords: AlGaN, GaN (HEMT), kink effect, hysteresis effect, FT-DLTS, CDLTS, traps

DOI: 10.1134/S1063782620100127

1. INTRODUCTION

One of the key issues that limit the efficiency of AlGaN|GaN field effect transistors (HFETs) for high-power and high-frequency applications is the existence of traps on the AlGaN surface and in the GaN buffer layers [1, 2]. The structures of the III-nitrides, produced through either metal-organic chemical-vapour deposition (MOCVD) or molecular beam epitaxy (MBE), can behave as shallow or deep traps influencing the channel density of the two-dimensional electron gas (2D-EG) and causing consequences such as current collapse [1], transconductance frequency dispersion [3], and low-power output during switching behavior [4].

GaN is typically grown hetero-epitaxially on foreign substrates such as sapphire (Al_2O_3), silicon carbide (SiC), and silicon (Si). The substrate, on which the nitride layers are grown, determines the crystalline quality of the entire buffer-layer stack. In particular, the large lattice and thermal mismatch between the AlN nucleation layer and the Si substrate leads to a severe amount of defects and, in particular, of threading dislocations starting from the substrate and propagating through the entire buffer-layer stack. In previous works [5–7], the fact is discussed that at high voltage (HV) the leakage current flows from the ohmic contacts into the substrate and along the Si interface. Electrically-active threading dislocations can assist the vertical leakage path between the ohmic contacts and the Si substrate. The high conductivity at the AlN|Si interface is due to several defects that create a conductive path, causing a degradation of the RF performance [8] and a premature breakdown [9]. Therefore, we proposed the Si removal technique [10] for enhancing the breakdown voltage. However, we have so far not presented the behavior under a high-electrical-field condition of defects that are induced by the growth of the nitride buffer layer on top of Si.

Still needs to be improved: a large number of studies have addressed the main different roots provoking degradation of RF, DC, or thermal performances of transistors dedicated to high-frequency applications. Experiencing reliability studied mechanisms on a given technology cannot be carried out to another one, depending on changes of the doping, passivation layer thickness or material, content of Al or In in the ternary composition of the channel. Among the more problematic causes of degradation for high electron mobility transistors (HEMT), traps need to be accurately identified.

In this paper, we investigate by Fourier transform deep-level transient spectroscopy (FT-DLTS) the nature and location of the traps, which may account for observed anomalies in static characteristics of nitride-based HEMT such as kink effect in the drain current or small hysteresis in capacitance-voltage characteristics.

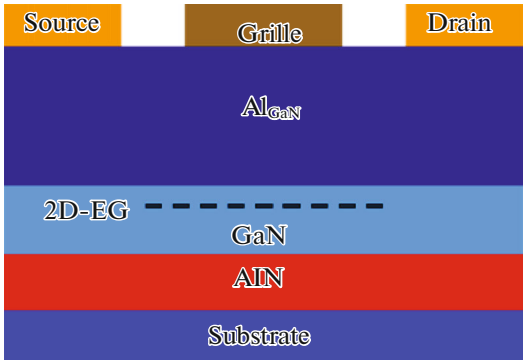

Fig. 1. A schematic cross-section of an AlGaN|GaN|SiC HEMT.

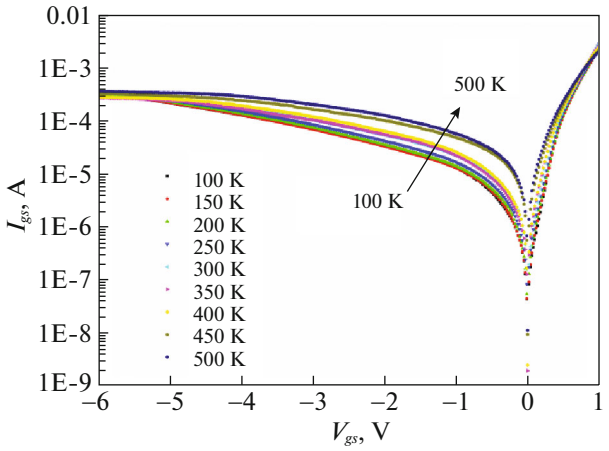

Fig. 2. Current–voltage transfer characteristic $I_{gs}(V_{gs})$ of AlGaN|GaN HEMTs with temperature in the range of 100 to 500 K.

2. SAMPLE DESCRIPTION AND EXPERIMENTAL DETAILS

The layer used in this study was grown by metal-organic chemical-vapour deposition (MOCVD) on SiC 2-inch thick substrate. The epitaxial layer structure contains an AlN. Intentionally undoped structures consisted of a 50-Å undoped AlGaN and a 1.2-μm undoped GaN cap grown on top of a GaN buffer. Doped structures consisted of a 200-Å undoped AlGaN spacer, a Si-doped AlGaN carrier-supply layer, a 50-Å undoped AlGaN barrier layer and a 30-Å undoped GaN cap, grown on top of GaN buffer. The Al mole fraction in all AlGaN layers was nominally 25%. The device processing consisted of mesa isolation using ECR-RIE followed by ohmic and Schottky metallization. Ohmic contacts were prepared by evaporating Ti|Al|Ni|Au multilayer and rapid thermal annealing at 850°C in an N_2 atmosphere for 30 s. The ohmic contact resistance of 0.4 Ω mm was measured on TLM patterns. The Schottky contacts consisted of a thick Ni layer covered by Au layer and patterned by e-beam lithography. The gate length is $L_G = 0.25$ μm, the gate width is $L_W = 100$ μm, and the separation between contacts were $L_{SG} = 1$ μm and $L_{GD} = 2.75$ μm (Fig. 1).

The reverse current-voltage characteristics as a function of the temperature $I(V, T)$ were measured using an HP4156. A liquid N_2-cooled cryostat was used for temperature-dependent measurement.

3. RESULTS AND DISCUSSION

3.1. Gate Current Measurements

The current–voltage characteristics are used widely to study the performance of the Schottky contacts since they offer many important device parameters. Figure 2 shows the typical semi-logarithmic reverse and forward bias $I(V)$ characteristics of the Au|Ni|SiC| GaN HEMT diodes measured in the temperature range of 100 to 500 K at steps of 25 K by applying gate-bias voltage V_{gs} from −5 to 1 V.

The integration time of the measurement is 320 ms per step. It is observed that the gate leakage current increases with increase in temperature. Then, in this study, the temperature dependence of current transport mechanisms at both reverse and forward bias voltage of Au|Ni|SiC|GaN HEMT diode have been investigated. This is performed to determine the mechanisms dominating the current transport.

We see that:

• The reverse currents are not strongly temperature-dependent, indicating the dominancy of tunneling conduction;

• The reverse currents are quite high and nearly constant at breakdown voltage $|V_b| > 4$ (below 10^{-4} A at 400 K) due to complete depletion of the 2D-EG;

• The forward currents show a kink structure, which may be due to tunneling currents at low biases. Many models have been proposed to explain the excess leakage currents in HEMTs on AlGaN|GaN, including the thin surface barrier model, and the field-emission/trap-assisted tunneling model. This may be explained by the degradation of the contact of the gate given the relatively large leakage current.

Furthermore, since the Schottky gate contact is still in the reverse-biased region, this leakage current could not be due to fluctuation of the potential but could possibly be caused by changes in the channel temperature due to the self-heating of the device. The origin of leakage current is probably due to deep level impurity or edge leakage currents [11, 12]. Zhang et al. [11] investigated leakage current mechanisms in GaN film grown by MBE and suggested that reverse leakage current is dominated by the emission of an electron from a trap state near the metal-semiconductor interface into a continuum of states associated with each conductive dislocation. Hsu et al. [12] reported that

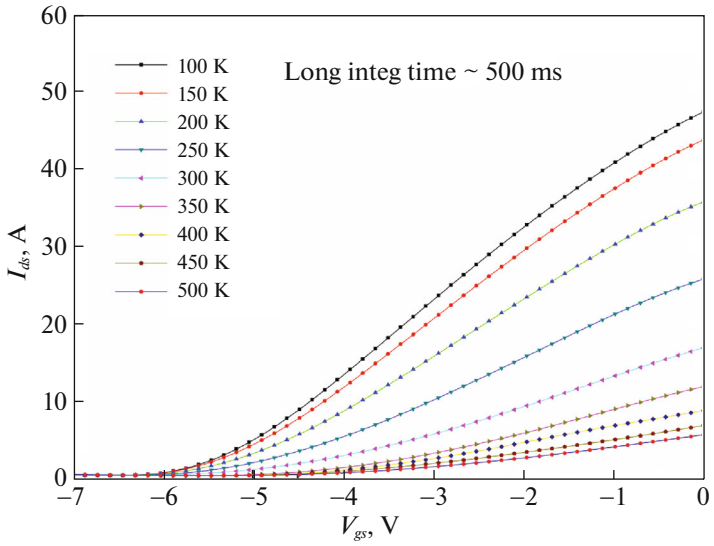

Fig. 3. Current–voltage transfer characteristic $I_{ds}(V_{gs})$ of AlGaN|GaN|SiC HEMTs.

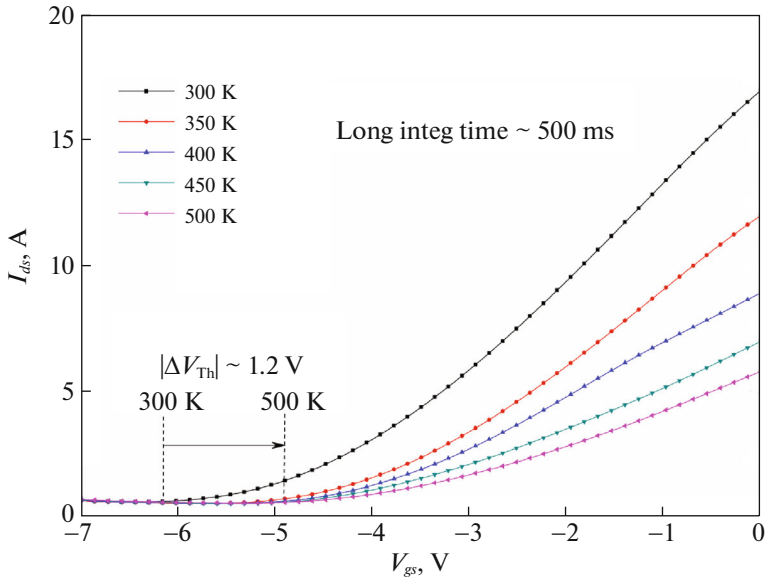

Fig. 4. Current–voltage transfer characteristic $I_{ds}(V_{gs})$ of AlGaN|GaN HEMTs between 300 and 500 K.

screw dislocations act as a passageway of excess leakage current in GaN film grown by MBE.

Another parasitic effect is the threshold voltage shift with temperature. As displayed in Fig. 3, the threshold voltage V_{Th} is defined by a linear extrapolation of the drain current I_{ds} versus gate voltage to zero value.

We see a 1.2-V offset from the threshold voltage to positive voltages from 350 K. This temperature coincides well with the kink effect of the $I_{ds}(V_{gs})$ measurements. It's made clear in Fig. 4.

This shift is thought to be caused by deep levels associated with electrically active defects in the GaN|SiC HEMT.

3.2. Drain-Source Current–Voltage Characteristic

Drain-source current–voltage $I_{ds}(V_{ds})$ measurements as a function of gate voltage have been performed at 400 K for HEMT AlGaN|GaN|SiC. Output characteristics show several parasitic effects. The gate negative voltage V_{gs} was increased in order to pinch-off the channel, the measurement is then taken; we noticed a large decrease of the drain current. An exam-

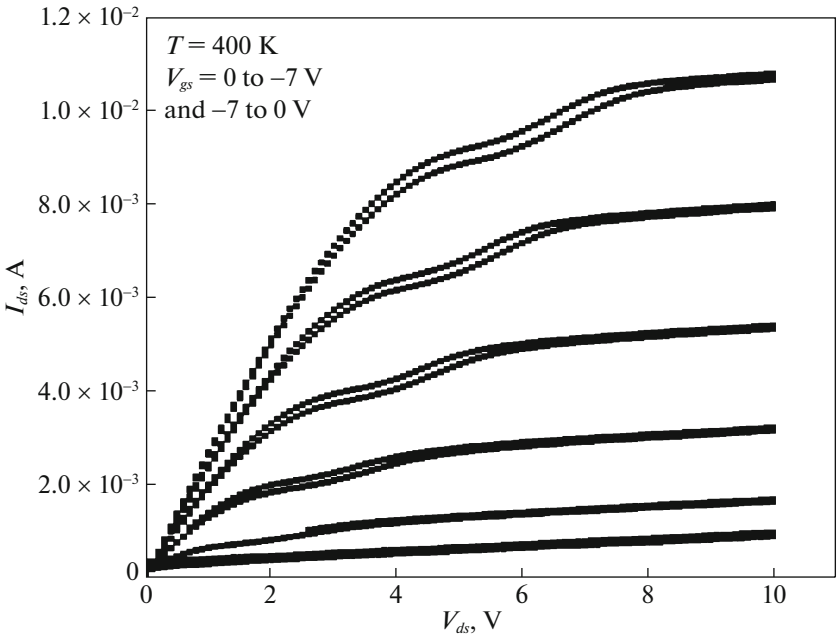

Fig. 5. Typical DC (I_{ds} versus V_{ds}) characteristics at $T = 400$ K, the gate-bias voltage V_{gs} has been first increased from 0 to -7 V and then decreased from -7 to 0 V.

ple of this degradation of drain current is given in Fig. 5.

This behavior confirms that we have the case of a thermally activated effect. A possible explanation of this decrease of the current is the presence of deep levels in the barrier layer under the gate metal, or the presence of deep levels in the interface in the buffer layer, and/or the surface states. In some other output characteristics obtained in the case of samples with SiC substrates, a spectacular variation of the output conductance, known as kink effect, is observed in Fig. 5. Some studies have established a link between the kink effect and the impact ionization phenomena [13–15], while other studies have correlated this effect with the presence of traps in the structure. Details of this effect are presented elsewhere [16, 17]. Another parasitic effect known as hysteresis phenomenon is observed in the output characteristics at 450 K. This effect represents an increase of the gate negative voltage V_{gs} in order to pinch-off the channel. The measurement is then taken again; we observe a decrease of the drain current. This Hysteresis effect may be explained by the presence of deep levels and the presence of surface states. The origin of the different parasitic effects in output characteristics is investigated in the following using FT-DLTS and CDLTS.

Because of the behavior of $I(V)$ characteristics, it seems difficult to compare the observed kink effect with deep levels in the structure for different temperatures; thus, a thorough analysis of the deep levels in our structure has been carried out to examine their potential influence on kink effect.

4. FT-DLTS AND CDLTS

From $I(V)$ measurements, we notice that a drain current anomaly appears for HEMT AlGaN|GaN|SiC. The voltage, at which the kink effect is observed, depends on the temperature. When the temperature increases, the kink voltage shifts to higher values. The drain current depends on both the direction and the speed of the voltage variation. Hysteresis effect is also observed for same sample at different temperatures. In order to understand the nature of these two parasite effects (kink and Hysteresis effects), CDLTS and FT-DLTS has been realized.

4.1. Conductance Deep Level Transient Spectroscopy Measurements

To characterize deep levels in HEMT GaN, conductance deep-level transient spectroscopy (CDLTS) is used. CDLTS is more suitable for study of the HEMT GaN structure than capacitance DLTS when the gate area of such structures is too small for capacitance DLTS. In addition, in CDLTS, the device can be reverse biased closer to the threshold voltage allowing investigation of deep levels in the buffer; this can be achieved by modifying the Fermi level position in the buffer region near the channel. In this type of structure, capacitance DLTS is not possible, because the high series resistance near the threshold voltage induces a distortion of the capacitance measurement; a correction procedure is needed to obtain the correct signal related to the traps. Moreover, CDLTS under drain pulse allows investigation in the buffer layer and

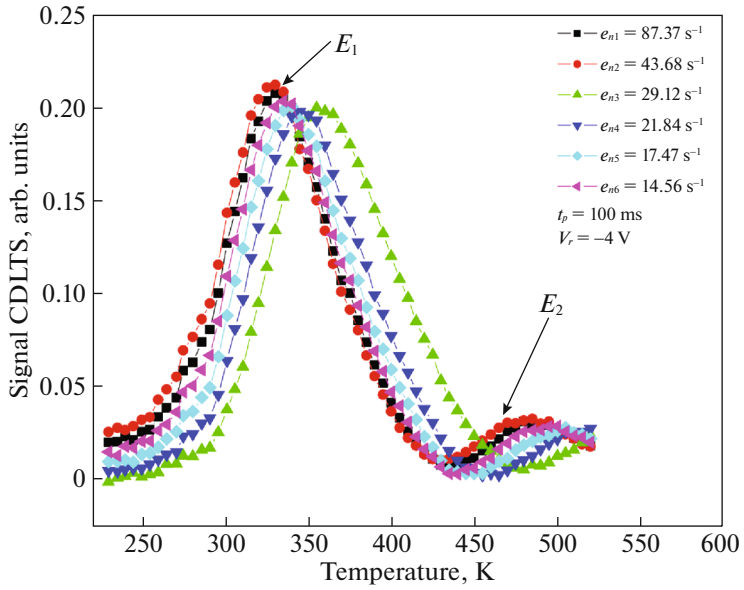

Fig. 6. A typical CDLTS spectrum showing the presence of two levels E_1 and E_2 under a gate pulse from 0 to –4 V and pulse time t_p = 100 ms. The reverse bias V_r = –4 V.

near the 2D-EG channel [17]. The CDLTS spectra (Fig. 6) under a gate pulse (V_{gs} switching from 0 to –4 V at V_{ds} = 5 V), reveal the presence of two positive peaks, corresponding to various electron emission e_n from different traps called E_1 and E_2.

For electron traps labelled by an activation energy E_{an}, the emission probability e_n per trap and per unit time is given by

$$e_n = \nu(T)\sigma_n(T)N_c(T)\exp\left(-\frac{E_{an}}{k_B T}\right),$$

where $\nu(T)$ is the thermal electron velocity, $\sigma_n(T)$ is the trap cross-section, and $N_c(T)$ is the conduction band state density.

Trap signatures related to emission kinetics are identified from the evolution of emission probability or emission time constant $\tau = (1/e_n)$ into a given temperature range.

The apparent activation energies and capture cross-sections are deduced from the Arrhenius plot of $\mathrm{Ln}(T^2/e_n)$ versus $1000/T$ (Fig. 7).

In order to compare the obtained activation energies with the ones reported in the literature, we notice the origin of the trap E_1. The trap E_1 is found to have an energy level of 0.62 eV, a capture cross-section of 5×10^{-13} cm^2, and a concentration of 2.5×10^{15} cm^{-3}. The electron trap is similar to the trap reported by H. Moasbahi et al. [18] using DLTS measurements on GaN layers grown by metal–organic chemical-vapor deposition (MOCVD). It is also observed by [19, 20] on *n*-GaN grown by MOCVD with DLTS measurement. This defect appears at the same temperature where the kink effect appears in the $I(V)$ characteristics; so this shows that the kink effect has a great relationship with deep levels. Despite the exact microscopic nature of level B_1 which cannot be undoubtedly established, the interesting point is that we can conclude that this level is located either in the interface state between Si|buffer and channel|buffer, near the 2D-EG or in the volume.

The trap E_2 with activation energy 0.40 eV was observed, to the best of our knowledge, only in our CDLTS measurements after gate pulse. This level can be attributed to interface states [23]. Indeed, Polyakov et al. [21] have shown that in AlGaN|GaN heterostructures, some levels exhibit an energy dependence on the AlGaN composition, and they suggested that such traps could be located at the interface. The energy value 0.45 eV does correspond to 0.24 Al concentrations as it is the case in our samples. This trap was also reported in AlGaN|GaN HEMTs by drain leakage current measurements at different temperatures [22].

4.2. Fourier Transform Deep-Level Transient Spectroscopy

A novel isothermal method of analyzing the deep impurity levels in semiconductors is proposed. In this method, named Fourier transform deep-level transient spectroscopy (FTDLTS), the transient junction capacitance, whose waveform is considered as a multi-exponential, is decomposed using two Fourier transforms.

Without doing the entire temperature ramp, this study consists in seeing the amplitude of the DLTS

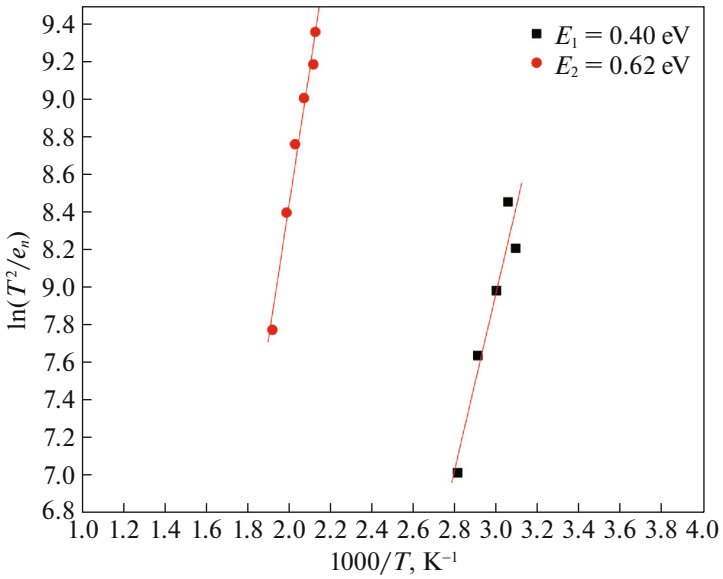

Fig. 7. Arrhenius plots for E_1 and E_2 deep levels observed in the AlGaN|GaN|SiC HEMTs under a gate pulse.

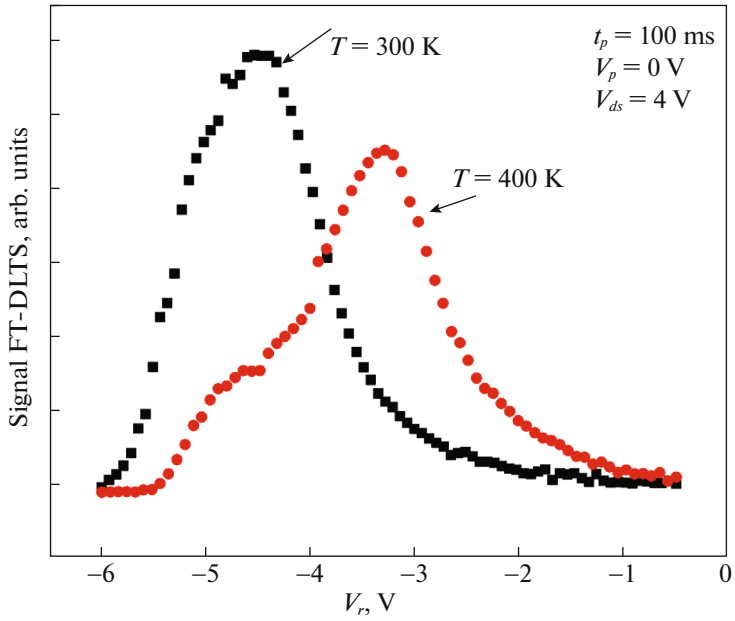

Fig. 8. Signal FT-DLTS versus V_r at $T = 300$ K and $T = 400$ K. V_p is the pulse voltage.

signal; among other things, the response of a trap if we know its emission temperature. Since we noticed anomalies at 400 K we wanted to do this additional study to see what is the trap that responds to this temperature. We compared with the response of signal CDLTS at room temperature (300 K). We measured the response as a function of the reverse voltage V_r to locate the defect and we found the result shown in Fig. 8.

We kept the same pulse time (100 ms) and the pulse voltage (0 V) for the two measurements as well as the voltage V_{ds} at 4 V where the kink should normally respond. We have observed that at 300 K you have a defect that responds when you polarize to –4.5 V (max signal) and when the sample is heated to 500 K this fault partially disappears and you have another defect that appears when you polarize at –3.5 V. This last defect can be the cause of the kink effect and the threshold shift during $I_{ds}(V_{gs})$ measurements. So to verify that this traps is the cause of the kink we carried out isothermal measurements to see the evolution of the signal as a function of the voltage V_{ds} (Fig. 9).

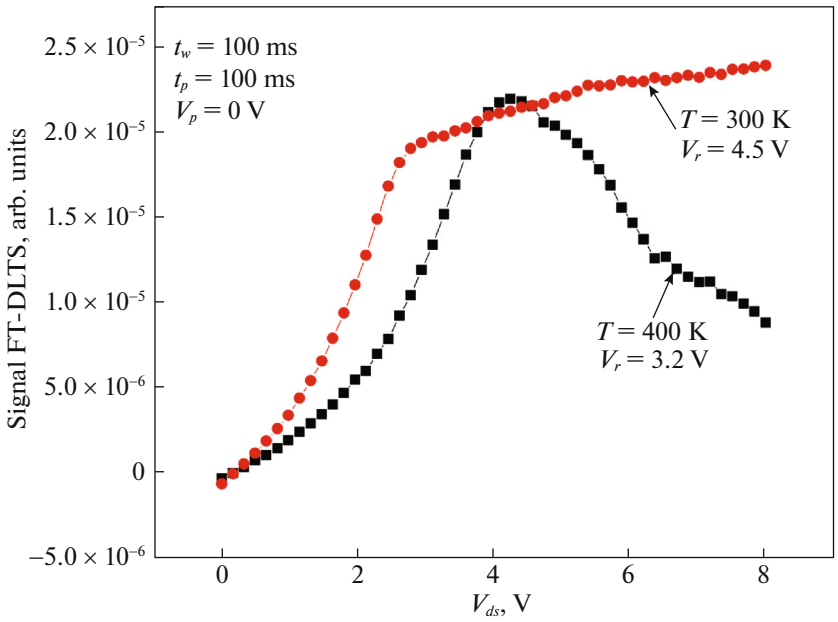

Fig. 9. Signal FT-DLTS versus V_{ds} at $T = 300$ K and $T = 400$ K. t_w is the window time.

For the first defect, which appears at 330 K, its response is abrupt from 2.5 V, then the signal remains almost constant, which shows that it does not depend too much on the strong values of V_{ds}. The second deep level that appears around 420 K depends on V_{ds} since it appears precisely when the kink effect appears (see the current–voltage characteristic $I_{ds}(V_{ds})$ measurements, the kink effect appears around 4 V) then this effect disappears when the V_{ds} voltage becomes very large. Then this effect indicates that the emission of the traps is maximum at the kink voltage (4 V); then, when V_{ds} is large enough, all the traps end up intermingling, probably because of the strong electric field in structure (classic explanation of the kink effect). In this case, the defect response decreases until canceled. This confirms the results found by the CDLTS.

5. CONCLUSIONS

In summary, static measurements and defect analysis of AlGaN|GaN|SiC HEMTs have been investigated. In fact, current-voltage characteristics show a number of anomalies attributed to trap centers and deep levels.

Deep levels in AlGaN|GaN|SiC HEMT's were directly measured by means of Fourier transform deep-level transient spectroscopy and Conductance DLTS technique. Two defects were labelled E_1 and E_2 with activation energies of 0.62 and 0.41 eV, respectively. These centers are responsible for trapping/detrapping phenomena.

FT-DLTS were also performed; they demonstrated that the defect at $T = 420$ K can be the source of the kink effect and the threshold shifting during $I_{ds}(V_{gs})$ measurements. The kink effect was associated with the E_2 defect observed at 0.62 eV. These results are in a good agreement with the hypothesis, which confirms the influence of deep levels, present in AlGaN|GaN|SiC HEMT transistor, on the kink, and the hysteresis effects observed in all $I_{ds}(V_{ds})$ characteristics.

ACKNOWLEDGMENTS

The author want to thank Dr W. Chikhaoui from L'INL of Lyon-France for providing the FT-DLTS and $I(V)$ measurements, and Prof. C. Gaquiere from 1'IEMN Lillel for his support and encouragement.

CONFLICT OF INTEREST

The author declare that they have no conflict of interest.

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