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Properties of sputtered CdS and CdTe films and performance of CdTe solar cells as a function of annealing temperature

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ABSTRACT

Thin film PV devices were fabricated in FTO/CdS/CdTe/Cu/Au superstrate configuration by RF sputtering of CdS and CdTe films, and $CdCl_2$ activation process was performed at 370, 380 and 390 °C, respectively. Morphological studies indicated for the first time that there were numerous holes randomly distributed at the as-deposited CdS/CdTe interface; although the holes were reduced after $CdCl_2$ annealing, the p–n junction was greatly improved. Further, the new concept of solar spectrum window width (ΔE_g) for the solar cells was demonstrated, and the ΔE_g of CdTe solar cells was found to be extended with increasing annealing temperature. Moreover, the efficiency of CdTe solar cells was dramatically improved from 0.02% to 12.02% as a function of annealing temperature, and the values of J_0 and A were reduced with the optimal values (7.2×10^{-7} mA/cm^2 and 1.87), indicating the primary carrier recombination of the best device was Shockley–Real–Hall mechanism in the space charge region.

1. Introduction

Due to their high-performance and large-area module production, thin-film cadmium telluride (CdTe) solar cells have currently held the second largest market share after crystalline silicon solar cells [1]. Meanwhile, CdTe solar cells have the shortest energy payback time among terrestrial PV devices and their energy return on investment exceeds that of fossil fuels in power generation [2,3]. Therefore, CdTe is an ideal candidate for PV energy conversion with a high absorption coefficient ($\sim 10^5$ cm^{-1}) and a direct optical band gap (1.45 eV) optimally matched to the solar spectrum, and its theoretical efficiency is expected to be about 29% [4]. In recent years, the preparation technologies of CdTe solar cells have achieved rapid development [5–8], and various high-efficiency CdTe solar cells ($>10\%$) have been successfully fabricated by several techniques, including close spaced sublimation [9], vapor transport deposition [10], magnetron sputtering [11] and screen printing [12]. To date, First Solar Inc. has reported the best efficiency of 20.4% (0.4778 cm^2) for a small area CdTe solar cell and a module efficiency of 17.5% (7021 cm^2) by high-temperature fabrication process [13]. In the case of sputtering technology, it is feasible to produce large-area CdS and CdTe films uniformly at low temperature (<400 °C), and the sputtered CdTe solar cell with the highest efficiency of 14.5% has been obtained for the CdS:O window layer [14].

In fact, thermal treatment is an important technology to improve material properties and interface quality [15–17]. In the case of CdTe solar cells, $CdCl_2$ post-annealing is a key process for fabricating high-efficiency CdTe solar cells. It can promote recrystallization and grain growth of CdS and CdTe films [18,19], accelerate the inter-diffusion of S and Te at the CdS/CdTe junction to reduce the concentration of interface defects by forming $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ alloys [20,21], and optimize the electronic properties of CdTe films by Cl incorporation and formation of an acceptor complex with vacancy [22,23]. Furthermore, in order to correlate the film properties with the final performance of the devices, it is necessary to carry out a systematic study on the properties of CdS and CdTe films and the performance of CdTe solar cells at different $CdCl_2$ annealing temperatures. In this study, according to the annealing temperature (387 °C) reported in literature [14], the $CdCl_2$ annealing process is performed at 370, 380 and 390 °C, respectively. The microstructure and optical properties of the sputtered CdS and CdTe films, and the performance of CdTe solar cells are investigated. In addition, the influences of the properties of CdS and CdTe films on the diode parameters and the performance of CdTe devices are also studied.

2. Experimental

2.1. Fabrication of CdS films, CdTe films and CdS/CdTe solar cells

Commercial FTO coated soda lime glass (TEC-7) with a sheet resistance of 6.795 Ω/sq and a transparency of 82% was used as

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Table 1
Sputtering conditions for CdS and CdTe films.

Parameters	Deposition conditions
Target material	Sintered ceramic disks of CdS and CdTe (99.999% purity, 2 in. in diameter)
Substrate–target distance	6 cm for CdS and 5 cm for CdTe
Substrate temperature	250 °C for CdS and 300 °C for CdTe
Base pressure	6.0×10^{-5} Pa
Sputtering pressure	2.0 Pa
Sputtering gas	Ar
Power	35 W for CdS and 30 W for CdTe

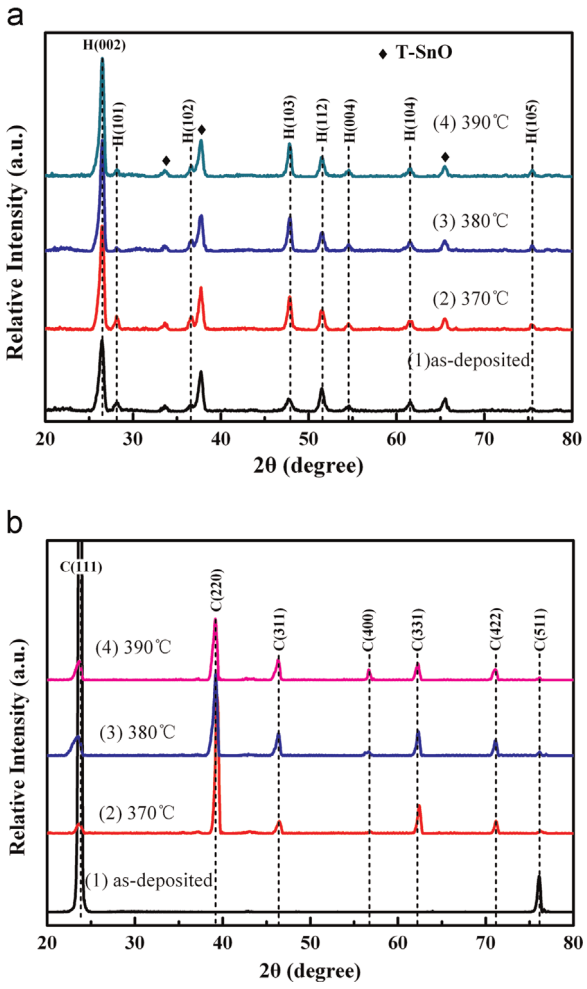

Fig. 1. XRD patterns for (a) CdS films deposited on FTO/glass substrates, and (b) CdTe films deposited on CdS/FTO/glass substrates before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

the front contact. All CdS and CdTe films were deposited by RF sputtering, and the sputtering conditions are listed in Table 1. The samples of CdS and CdTe films were deposited on FTO/glass substrates, and the thickness of CdS and CdTe films was about 200 and 2500 nm, respectively. The CdTe solar cell was fabricated in glass/FTO/CdS/CdTe/Cu/Au superstrate configuration in the present study. The $CdCl_2$ annealing was performed in a mixed atmosphere of $CdCl_2$ vapor and dry air at 370, 380 and 390 °C for 15 min, respectively. The $CdCl_2$ evaporator source was $CdCl_2$ power (99.999% purity) coated quartz glass at a distance of 3 mm from the sample surface. After $CdCl_2$ annealing, pseudo ohmic contact was obtained by etching the CdTe film surface with bromine methanol solution followed by vacuum evaporating Cu (3 nm) and Au (150 nm) layers through an aperture metal mask with an area of 0.25 cm^2 in

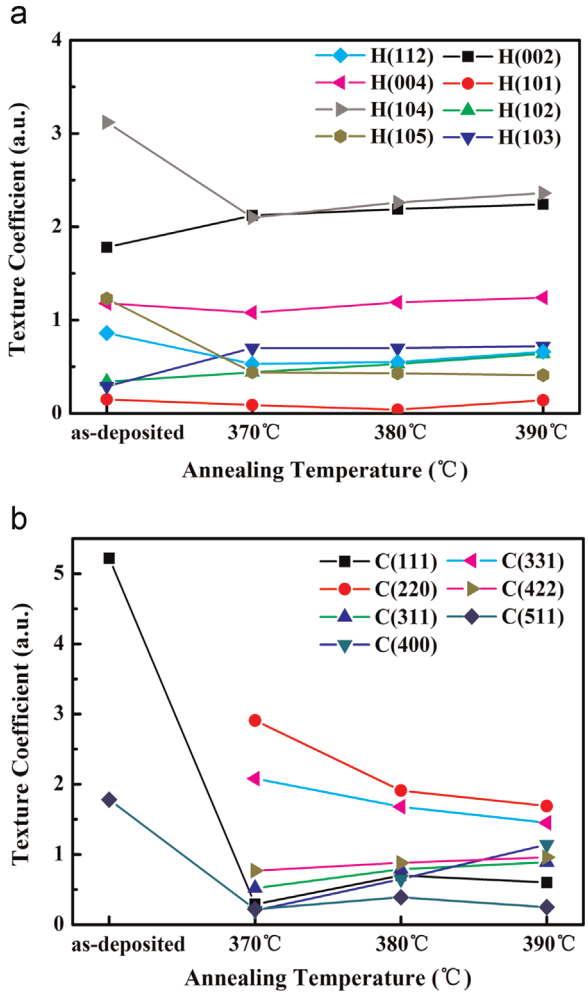

Fig. 2. Texture coefficient for (a) CdS films deposited on FTO/glass substrates, and (b) CdTe films deposited on CdS/FTO/glass substrates before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

Table 2
Preferential orientation factor (k) and lattice constant (d) for CdS and CdTe films before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

Sample/condition		k	d (Å)
CdS	(PDF# 41-1049)	–	4.141
	As-deposited	0.874	4.153
	370 °C	0.750	4.141
	380 °C	0.731	4.143
	390 °C	0.706	4.142
CdTe	(PDF# 15-0770)	–	6.481
	As-deposited	1.622	6.495
	370 °C	0.989	6.481
	380 °C	0.526	6.483
	390 °C	0.453	6.484

succession. Cu diffusion was achieved by annealing in room air at 150 °C for 45 min.

2.2. XRD, SEM, transmittance spectra, J–V and EQE measurements

The surface morphology of the CdS and CdTe films, and the cross-sectional morphology of CdTe/CdS/FTO/glass junction were observed by scanning electron microscope (SEM; Siren 2001615,

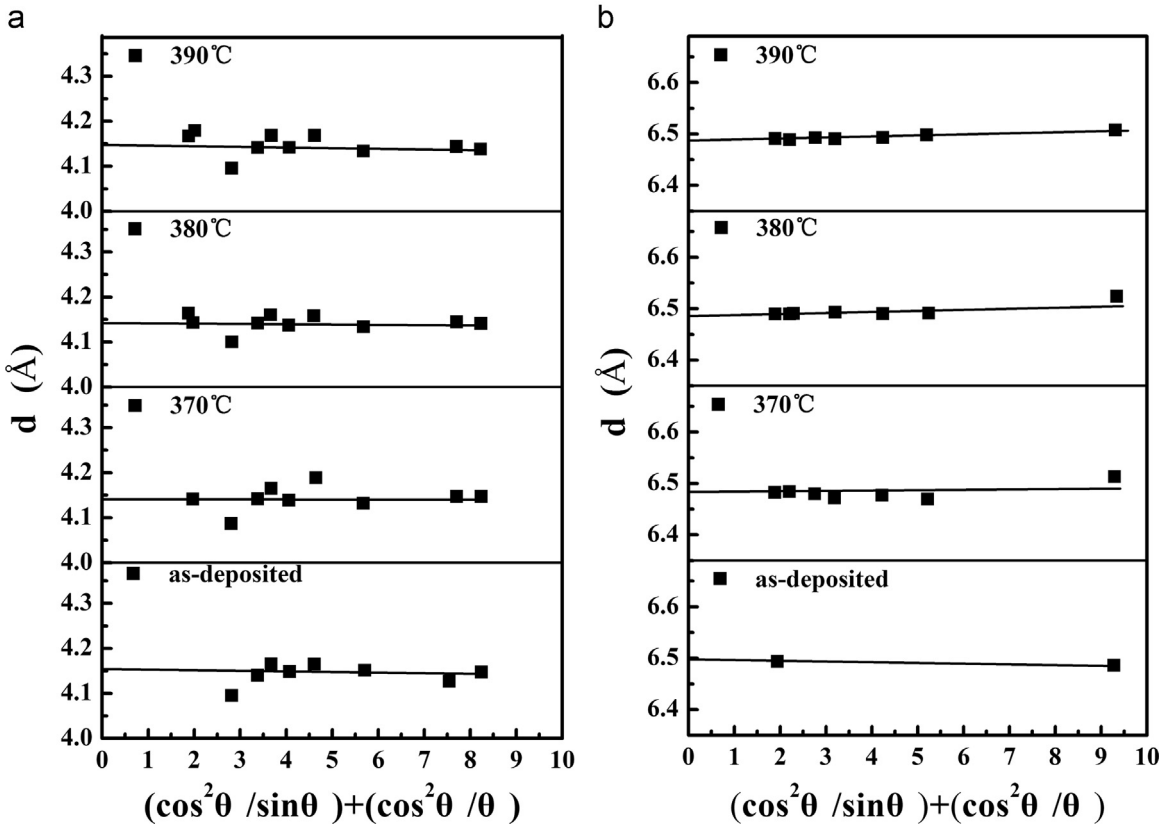

Fig. 3. Lattice constant for (a) CdS films deposited on FTO/glass substrates, and (b) CdTe films deposited on CdS/FTO/glass substrates before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

FEI Company, Hillsboro, OR, USA). The structure of the CdS and CdTe films was analyzed using X-ray diffraction (XRD; Bruker D8 DISCOVER) with 1.5418 Å Cu Kα radiation. Optical transmittance spectra were recorded with a UV–vis spectrophotometer (Cary 5000) in the wavelength range of 300–1100 nm. Before observation, the annealed samples were rinsed with deionized water and etched with dilute hydrochloric acid (1:6) for 6 s in order to remove $CdCl_2$ residue and chlorine oxides. The light and dark current density–voltage (J–V) characteristics of the CdTe solar cells were measured using a continuous light solar cell performance tester system (Xe lamp, Newport) under simulated AM1.5G (1000 W/m^2) and in the dark at 25 °C, respectively. External quantum efficiency (EQE) measurements were performed using a spectral response measurement system (Crowntech, QTest Station 1000AD). A calibrated Si-cell was used as reference for the $J(V)$ as well as for the EQE measurements.

3. Results and discussion

3.1. Structure, preferential orientation and stress

Fig. 1 shows the XRD patterns for the CdS and CdTe films before and after $CdCl_2$ annealing. As can be seen, all CdS samples exhibit polycrystalline diffraction peaks corresponding to hexagonal (002), (101), (102), (103), (112), (004), (104) and (105) planes (Fig. 1a), indicating that the CdS films are polycrystalline with hexagonal structure. The as-deposited CdTe sample exhibits two polycrystalline diffraction peaks corresponding to cubic (111) and (511) planes. After $CdCl_2$ annealing, some new peaks corresponding to cubic (220), (311), (400), (331) and (422) planes can be observed between the two peaks of cubic (111) and (511) planes (Fig. 1b). These suggest that all CdTe films are polycrystalline with cubic structures.

The degree of preferred orientation of CdS and CdTe films before and after $CdCl_2$ annealing can be estimated from the relative peak intensity. The values of preferred orientation factor (k) can be quantified by Refs. [24,25]

$$C_i = \frac{I_i/I_{0i}}{(1/N)\sum_{i=1}^{N} I_i/I_{0i}} \quad (1)$$

where C_i is the texture coefficient, I_i is the intensity of a generic peak in the XRD, I_{0i} is the intensity of a generic peak for a completely random sample [Joint Committee for Power Diffraction Standard], and N is the number of diffraction peaks considered in the analysis.

C_i gives the degree of preferred orientation of a certain crystal plane with respect to a reference sample. A value of 1 represents random orientation, while a value above 1 means preferential orientation in that direction. To analyze the preferred orientation of each sample as a whole, the standard deviation of all C_i values relative to randomly oriented samples can be calculated using

$$k = \sqrt{\frac{\sum_{i=1}^{N}(C_i - 1)^2}{N}} \quad (2)$$

where k is the preferential orientation factor used to compare the degree of orientation among different samples, and $k=0$ indicates a completely random sample.

Fig. 2 shows the C_i values for the selected diffracting planes of CdS and CdTe films. The as-deposited CdS film exhibits the larger C_i values corresponding to hexagonal (002) and (104) planes than those corresponding to other planes. After $CdCl_2$ annealing at 370, 380 and 390 °C, the CdS films show a little loss of preferred orientation along (104) orientation yet still maintain preferred

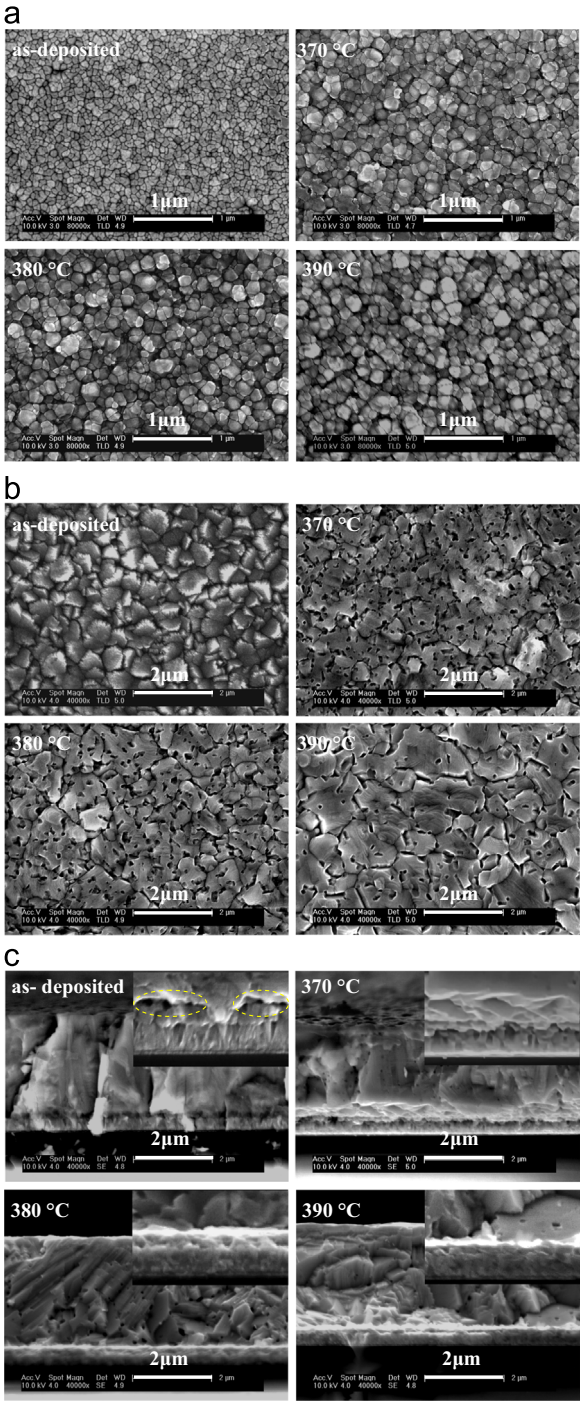

Fig. 4. SEM images for (a) CdS films deposited on FTO/glass substrates, (b) CdTe films deposited on CdS/FTO/glass substrates and (c) cross-sectional structure of glass/FTO/CdS/CdTe junction before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

orientation along (002) and (104) directions. The as-deposited CdTe film exhibits a strong peak corresponding to cubic (111) plane. However, after $CdCl_2$ annealing, the C_i value of cubic (111) plane is decreased, and the peak is replaced by that corresponding to cubic (220) plane. The changes can be attributed to the crystallography rearrangement caused by recrystallization and grain growth during $CdCl_2$ annealing. In the process, the decrease of C_i values of (104) plane in the CdS films and (111) plane in the CdTe films is associated with the decreased grain number in CdS films oriented along (104) direction and that in the CdTe films oriented along (111) direction, respectively. The recrystallized grains may coalesce and grow in the direction with minimized surface energy, which is responsible for the observed change of C_i values of different planes in the films. As seen from Table 2, the as-deposited CdS and CdTe films have higher k values (0.874 and 1.622,) than those of the annealed films. After $CdCl_2$ annealing, the k values of the films are gradually decreased, and the CdS and CdTe films annealed at 390 °C become randomly oriented with k values of 0.706 and 0.453. These results match well with the reported literatures [26]. Besides, it is also noted that the change of k values is closely related to the microstructure of the samples. When annealing temperature increases, the crystallinity of the samples is improved, and the preferential orientation is changed randomly. Accordingly, the k values are decreased.

Crystallographic rearrangement is related to the stress relaxation in these films, which can be calculated by the deviation of lattice constant (d). Fig. 3 shows the lattice constants of CdS and CdTe films according to the method described by Taylor [27] and Nelson [28]. The lattice constants of the as-deposited CdS film (4.153 Å) and CdTe film (6.495 Å) are larger than those of powder samples of CdS (4.141 Å, (PDF# 41-1049)) and CdTe (6.481 Å, (PDF# 15-0770)), respectively (Table 2). This indicates that the as-deposited CdS and CdTe films are subjected to a residual compressive stress. After $CdCl_2$ annealing, lattice constants of the CdS and CdTe films decrease and reach the values of powder samples of CdS ((PDF# 41-1049) and CdTe (PDF# 15-0770)), respectively. These results suggest that during $CdCl_2$ annealing process, the residual compressive stress is relaxed due to recrystallization and grain growth in the CdS and CdTe films, as observed in Section 3.2.

3.2. Morphology

The influences of $CdCl_2$ annealing on the morphology evolution of CdS and CdTe films are analyzed by SEM. Fig. 4a shows that all CdS films on FTO/glass substrates are compact, uniform and without pin-holes. The grain size of the as-deposited CdS film is about 70 nm. After $CdCl_2$ annealing, the crystallinity of the CdS films is improved, and the films have the same morphology, with the grain size in the range of 150–300 nm. Similarly, the as-deposited CdTe films on CdS/FTO/glass substrate are also compact, uniform and free of pin-holes. The grain size of the as-deposited CdTe film is about 500 nm. By increasing annealing temperature, the grain size of the CdTe films gradually increases, and reaches up to 2000 nm at 390 °C (shown in Fig. 4b). These results can be explained by the role of $CdCl_2$ as a fluxing agent during annealing process, which can promote recrystallization of the CdS and CdTe films at low annealing temperatures. As we all know, larger grain size of the CdTe films is beneficial to improving the transport properties of carriers by reducing the carrier trapping effects in grain boundaries [27,29]. By the way, the corrosion pits on the film surface are originated from etching effect with dilute hydrochloric acid to remove $CdCl_2$ residue and chlorine oxides.

Fig. 4c shows the cross-sectional structure of glass/FTO/CdS/CdTe junction before and after $CdCl_2$ annealing. The as-deposited CdTe film shows a columnar structure growing perpendicular to the substrate. As annealing temperature increases from 370 to 390 °C, the original columnar crystals gradually disappear and are finally replaced by granular crystals. There are numerous holes randomly distributed at the as-deposited CdS/CdTe interface region. These pores are produced by structural and/or compositional inhomogeneity, as well as the formation of slowly-growing facets in the island nucleation and directional growth process [31]. Furthermore, the misfit strain at the CdS/CdTe hetero-interface may facilitate the formation of holes, and the increase of numerous pores can lead to strain relief to some degree [32]. As these holes can act as carrier recombination centers, the p–n junction will be

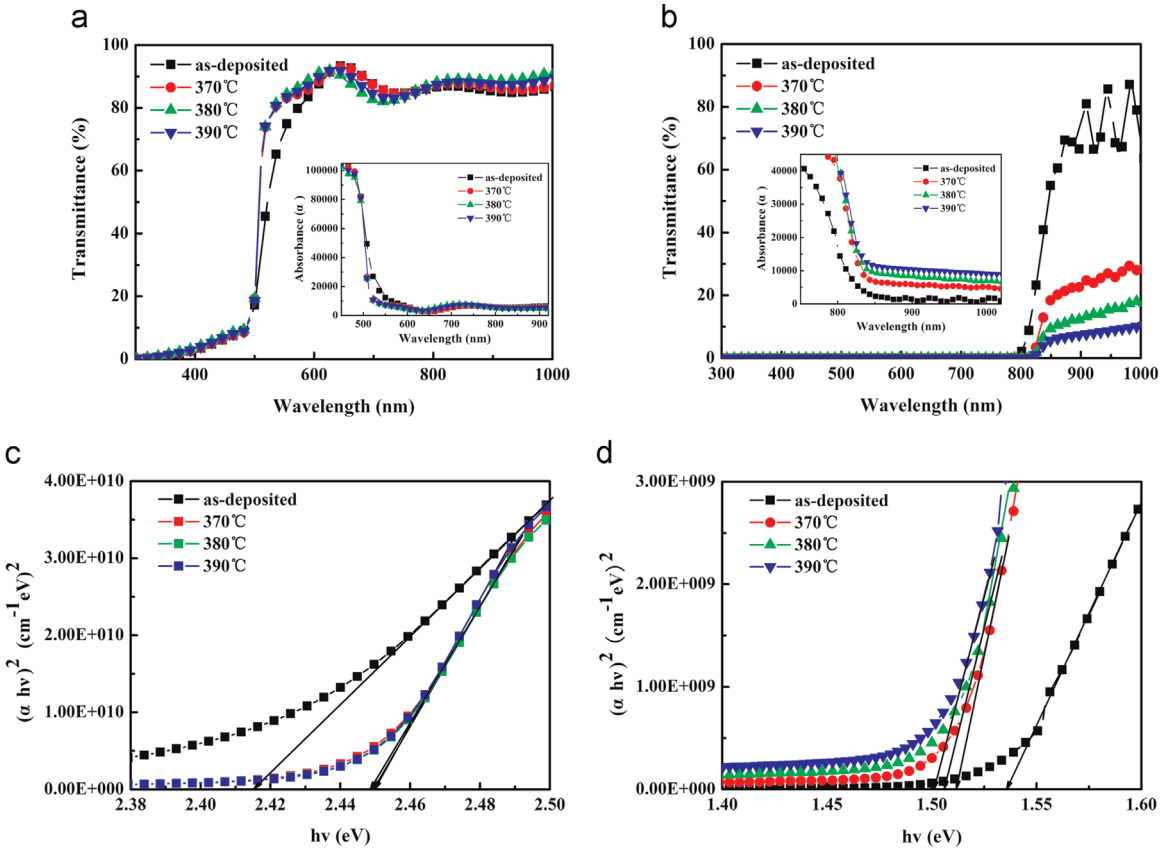

Fig. 5. Optical transmittance characteristics: (a) and (b) optical transmittance spectra for the CdS and CdTe films; (c) and (d) $(\alpha h\nu)^2$ vs. $h\nu$, fitted to determine band gaps for the CdS and CdTe films deposited on FTO/glass substrates before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

Table 3
Band gaps (E_g, eV) of the CdS and CdTe films and surface roughness (R_a) of the CdTe films.

Samples ID	CdS film	CdTe film	CdS, CdTe film	CdTe film	CdTe film
	E_g (T%, eV)	E_g (T%, eV)	ΔE_g (T%, eV)	$E_g^{'}$ (EQE, eV)	(R_a, nm)
As-deposited	2.415	1.536	0.879	1.502	2.3
370 °C	2.448	1.512	0.936	1.439	11.3
380 °C	2.449	1.506	0.943	1.409	17.6
390 °C	2.450	1.501	0.949	1.396	26.9

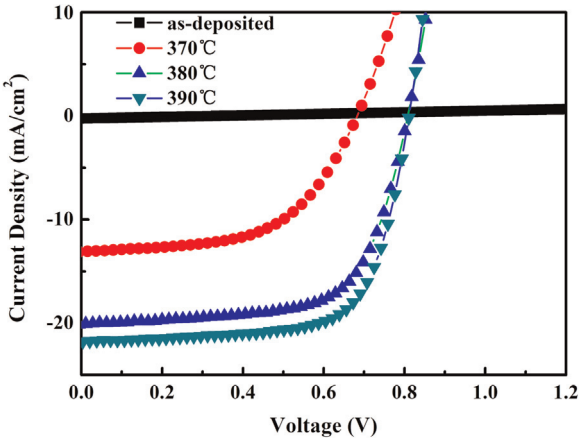

Fig. 6. Light *J–V* curves for CdTe solar cells before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

degraded due to the higher interface recombination [33]. However, these holes can be reduced after $CdCl_2$ annealing, which is beneficial to the p–n junction quality and the performance of CdTe solar cells. To the best of our knowledge, it is the first observation that the holes distributed at the as-sputtered CdS/CdTe interface region are reduced after $CdCl_2$ annealing. Holes healing during $CdCl_2$ annealing process can be explained by the inter-diffusion of S and Te at CdS/CdTe interface. As observed by secondary ion mass spectrometry (SIMS) in previous studies, inter-diffusion of S and Te occurs at the CdS/CdTe junction after $CdCl_2$ annealing, which causes the formation of $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ ternary compound at CdS/CdTe interface [34]. Consequently, it is considered in this study that inter-diffusion of S and Te at the CdS/CdTe interface and the stress relaxation in the CdS and CdTe films are the main reasons for the disappearance of these holes.

In addition, further studies show that extended $CdCl_2$ annealing can degrade the CdS film due to S loss. The nonuniform CdS consumption can result in lateral junction discontinuity [35], but this can be mitigated by heat treatment of the CdS layer prior to CdTe deposition to increase CdS grain size and density [36] or by deposition of CdS and CdTe films in an oxygen-containing ambient. Interestingly, the presence of oxygen in CdS and CdTe films can help optimize the inter-diffusion at CdS/CdTe interface and therefore improve the cell performance [37,38]. Further work in these topics is in progress in our lab.

3.3. Optical transmittance spectra

Fig. 5a shows the optical transmittance spectra for CdS films on FTO/glass substrates before and after $CdCl_2$ annealing. All CdS films exhibit an average transmittance of $>85\%$ in the wavelength range of 630–850 nm. Moreover, the annealed CdS films exhibit a

Table 4
Performance of CdTe solar cells before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

Device conditions	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	G (mS/cm^2)	R_s (Ω cm^2)	A	J_0 (mA/cm^2)
As-deposited	328	0.24	25	0.02	0.01	190.79	8.10	8.3×10^{-4}
370 °C	682	13.07	56	5.02	0	11.67	2.51	1.4×10^{-5}
380 °C	808	20.00	67	10.81	0	2.25	1.92	9.7×10^{-7}
390 °C	811	21.76	68	12.02	0	1.40	1.87	7.2×10^{-7}

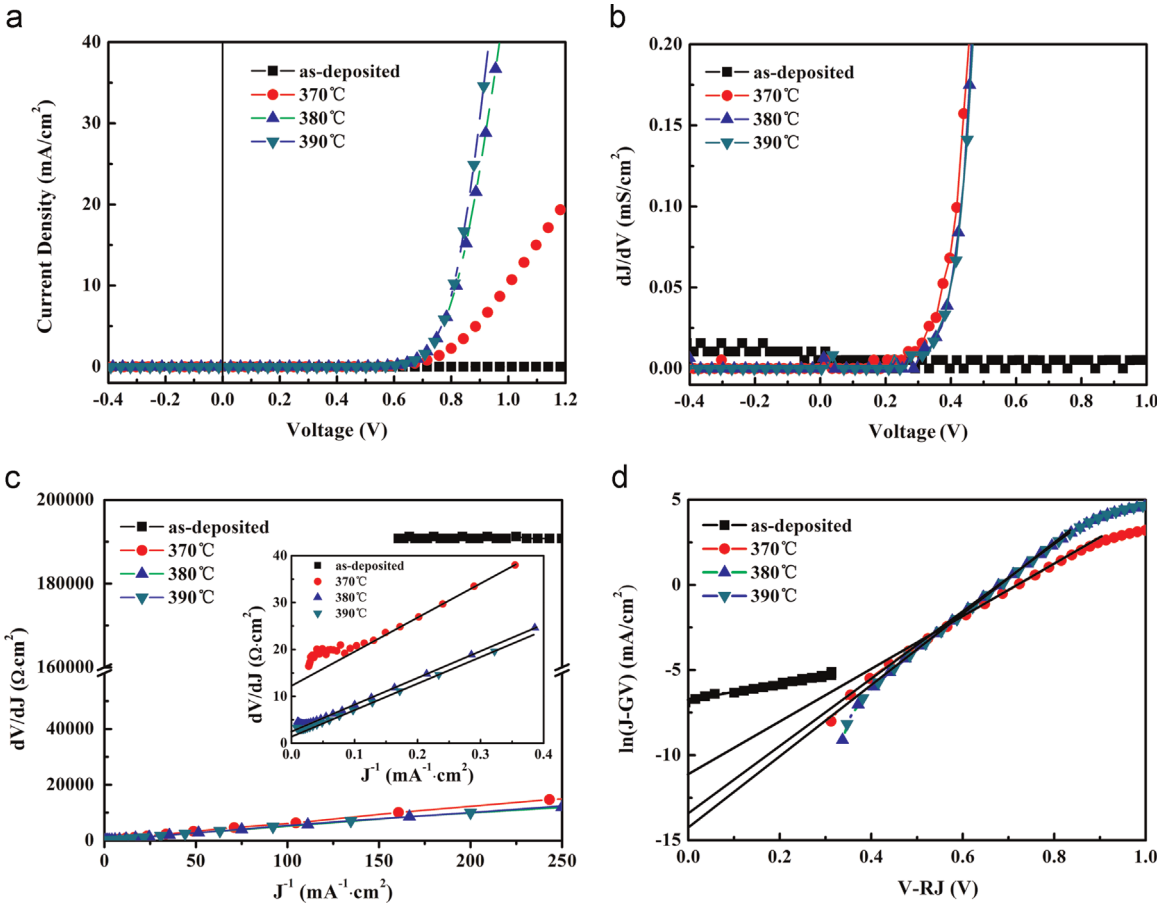

Fig. 7. Dark *J–V* characteristics: (a) dark *J–V* curves; (b) d*J*/d*V* vs. *V*, fitted to determine shunt conductance *G*; (c) d*V*/d*J* vs. 1/*J*, fitted to determine series resistance *R*; (d) ln (*J*–GV) vs. *V*–*RJ*, fitted to determine diode quality factor *A* and diode current J_0 for the CdTe solar cells before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

higher optical transmittance and a lower optical absorbance compared with the as-deposited CdS film in the wavelength range below 630 nm. The enhancement of optical transmittance of the annealed CdS films is beneficial to the improvement of J_{sc} for CdTe solar cells. As for CdTe films, they all have high optical absorbance in the wavelength range below λ_g (hc/E_g), and the optical transmittance is almost equal to zero, as shown in Fig. 5b. In the wavelength range above λ_g, all the annealed CdTe films have lower transmittance than the as-deposited CdTe film, and optical transmittance of the annealed CdTe films is reduced as annealing temperature increases. The lower transmission can be attributed to the scattering effect by the rough surface of annealed CdTe films. With increasing annealing temperature, the surface roughness of the CdTe thin films is gradually improved as shown in Table 3.

Figs. 5c and d show $(\alpha h\nu)^2$ vs. photon energy $h\nu$, which can be used to determine band gaps for CdS and CdTe films before and after $CdCl_2$ annealing, respectively. After $CdCl_2$ annealing at 370, 380 and 390 °C, band gaps of the CdS films are improved steadily, yet those of the CdTe films are reduced gradually. In order to study the actual range of the incident solar spectrum utilized by solar cells, the new concept of the solar spectrum window width is introduced for solar cells in this paper. ΔE_g is the difference of band gaps between the window layer (CdS) and the absorber layer (CdTe). The ΔE_g value of the as-deposited CdS /CdTe solar cell is 0.879 eV. As annealing temperature increases from 370 to 390 °C, the value increases from 0.936 to 0.949 eV (Table 3). This result reveals that the utilizable energy range of incident sunlight for CdTe solar cells is extended after $CdCl_2$ annealing, which can also improve J_{sc} of CdTe solar cells.

3.4. Current–voltage analysis

J–V measurement is the most common tool to evaluate the performance of solar cells. The *J–V* behavior of solar cells can be generally described by a single exponential diode equation as follows:

$$J = J_0 \exp[\frac{q(V - RJ)}{AkT}] + GV - J_L \quad (3)$$

where J_0 is the diode current, J_L is the light generated current, A is the diode quality factor, R is the series resistance, and G is the shunt conductance.

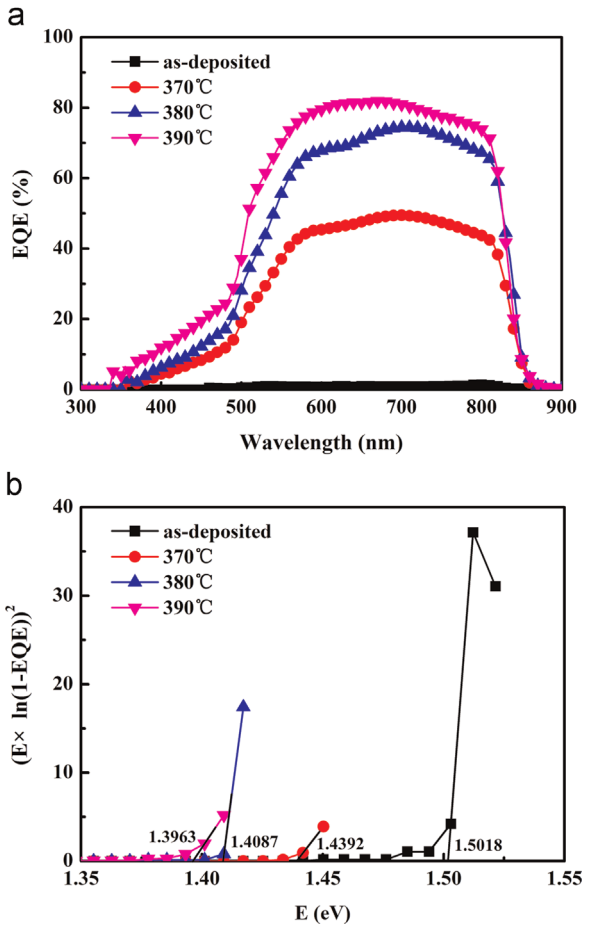

Fig. 8. External quantum efficiency measurement: (a) EQE vs. wavelength λ; (b) $[E \cdot \ln(1-EQE)]^2$ vs. E, fitted to determine the band gap of CdTe absorber layers for CdTe solar cells before and after $CdCl_2$ annealing at 370, 380 and 390 °C.

Fig. 6 shows the light *J–V* characteristics for the CdTe solar cells before and after $CdCl_2$ annealing. The as-deposited CdTe solar cell exhibits the lowest efficiency of 0.02% (V_{oc}=328 mV, J_{sc}=0.24 mA/cm^2, FF=25%). As annealing temperature increases from 370 to 390 °C, the device performance improves significantly with the best efficiency of 12.02% (V_{oc}=811 mV, J_{sc}=21.76 mA/cm^2, FF=68%) as listed in Table 4. Since J_L can be a function of voltage due to field-dependent drift collection, only the dark *J–V* curves with J_L=0 is analyzed as shown in Fig. 7, and the values of *G*, *R*, *A* and J_0 are listed in Table 4 [39,40].

(1) Fig. 7a shows the dark *J–V* curves. The as-deposited CdTe device appears no obvious diode characteristics. As annealing temperature increases from 370 to 390 °C, the diode characteristics of the CdTe devices are improved significantly.
(2) Fig. 7b shows the curves of derivative d*J*/d*V* vs. *V* for the CdTe solar cells. The plots of shunt conductance, $G(V)$=d*J*/d*V*, are flat in reverse bias. The $G(V)$ value of the as-deposited CdTe solar cell is 0.01 mS/cm^2. In addition, the curves of the annealed CdTe solar cells are coincided with the horizontal axis, and the *G* values are approximately equal to zero after $CdCl_2$ annealing at 370, 380 and 390 °C.
(3) The derivative d*V*/d*J* vs. 1/*J* can be plotted according to Eq. (3). For $G \leq 0.01$ mS/cm^2, the *RG* value is ignored. Then, a linear fitting to the plots gives an intercept of *R* with ordinate (Fig. 7c), and the *R* value of the as-deposited CdTe solar cell is determined to be 190.79 Ω cm^2. As annealing temperature increases from 370 to 390 °C, the *R* value decreases from 11.67 to 1.4 Ω cm^2.
(4) Using the *R* values obtained from Fig. 7c, the curves of ln (*J–GV*) vs. *V–RJ* can be plotted as Fig. 7d shows. The values of J_0 and *A* can be deduced from the slope intercepted with ordinate. For the as-deposited CdTe solar cell, the values of J_0 and *A* are 8.3×10^{-4} mA/cm^2 and 8.1, respectively. As annealing temperature increases, the values of J_0 and *A* both decline, and the best values are $J_0 = 7.2 \times 10^{-7}$ mA/cm^2 and *A*=1.87. These results indicate the primary carrier recombination of the best device is Shockley–Real–Hall mechanism in the space-charge region (SCR).

In fact, the performance of the CdTe solar cells is directly associated with the properties of the CdS and CdTe films and the quality of the CdS/CdTe junction. As annealing temperature increases from 370 to 390 °C, the values of *G* and *R* both decrease for better crystallinity of the CdTe films and more optimized quality of the CdS/CdTe junction, which can increase the values of J_{sc} and V_{oc}. The inter-diffusion of S and Te reduces the defect concentration at the CdS/CdTe interface by forming $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ alloys, which can decrease the values of *A* and J_0. The more the incident photons through the CdS film, the bigger the ΔE_g value, and the higher the J_{sc} value.

3.5. External quantum efficiency analysis

Fig. 8a shows the EQE spectrum as a function of photon wavelength for the CdTe solar cells before and after $CdCl_2$ annealing. The as-deposited CdTe solar cell shows the lowest EQE. After $CdCl_2$ annealing at 370, 380 and 390 °C, the EQEs of the CdTe solar cells are improved successively. As annealing temperature increases, the increase of sulfur loss can decrease the thickness of the CdS film, thus increasing the optical transmittance and enhancing the EQEs in short-wavelength range ($<$500 nm), as previously reported in Refs. [41,42]. In the long-wavelength side, the EQEs are restricted by the value of cutoff wavelength (λ_g) corresponding to the band gap ($\lambda_g = hc/E_g$) of the CdTe absorber layer, which can be determined from a plot of $[E \cdot \ln(1-EQE)]^2$ vs. E for the CdTe solar cells (Fig. 8b) [43]. A linear fitting to the plots can give an intercept of E_g' with abscissa, and the values are listed in Table 3. The E_g' values of the CdTe films before and after $CdCl_2$ annealing at 370, 380 and 390 °C are 1.502, 1.439, 1.409 and 1.396 eV, respectively. With the band gap of CdTe films decreasing from 1.502 to 1.396 eV, the J_{sc} value increases correspondingly. As estimated from the EQE curve, the E_g' values of CdTe absorber before and after $CdCl_2$ annealing at 370, 380 and 390 °C are around 1.502, 1.439, 1.409 and 1.396 eV, respectively. These values are significantly lower than those calculated from optical transmittance spectra. However, the variation trend is similar. This deviation may be attributed to the formation of $CdTe_{1-x}S_x$ ternary compound in the absorber layer by S diffusion into CdTe absorber [44,45].

4. Conclusions

In summary, effects of $CdCl_2$ post-annealing on the properties of sputtered CdS and CdTe films and the performance of CdTe solar cells are investigated in this paper. With $CdCl_2$ annealing temperature increasing from 370 to 390 °C, some findings can be summarized as follows:

(1) The grain size is increased, the preferential orientation of the films is more randomized, and the residual compressive stress is relaxed due to recrystallization and grain growth.

(2) The holes distributed at the as-deposited CdS/CdTe interface are reduced due to the inter-diffusion of S and Te at CdS/CdTe interface and the stress relaxation in CdS and CdTe films.
(3) The value of solar spectrum window width ΔE_g of the CdTe solar cells is increased.
(4) The performance of the CdTe solar cells is improved significantly from 0.02% to 12.02%.

In order to further improve the performance of the CdTe solar cells, the future optimization on annealing strategy will be focused on improving the crystallinity of the CdS and CdTe films and reducing the inter-diffusion of S and Te at the CdS/CdTe interface.

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