Physica B 700 (2025) 416949

Contents lists available at ScienceDirect

Physica B: Condensed Matter

journal homepage: www.elsevier.com/locate/physb

Detailed analysis of possible current-transport mechanisms (CTMs) in Au/(P3DMTFT)/n-GaAs Schottky diodes (SDs) in a wide range of temperature

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ARTICLE INFO

Keywords:
Au/(P3DMTFT)/n-GaAs diodes
Current transport mechanisms (CTMs)
Double Gaussian distribution of BH
Energy-dependent distribution of surface states

ABSTRACT

In this study, Au/Poly[3-(2,5-dimethyl-4-thienyl)phenylthiophene](P3DMTFT)/n-GaAs Schottky diodes were produced, and their CTMs were evaluated between 80 and 320 K using current/voltage (*I-V*) characteristics. Using the standard thermionic emission (TE) theory/model, basic electrical parameters were extracted from the forward bias voltages at each temperature. Fluctuations in the barrier height (*BH,* Φ_{B0}), and ideality factor (*n*) were attributed to BH inhomogeneity, which was assumed to follow a Gaussian distribution (GD) across the metal-semiconductor contact. The Richardson-Arrhenius curve deviated from linearity at lower temperatures. The Φ_{B0} and n against q/2 kT graphs exhibited two distinct linear regions with differing slopes. These are two key indicators that there is a double Gaussian distribution between metal and semiconductor. To improve the analysis, a modified Richardson plot was created utilizing the standard deviation (σ_{s0}) values from the slopes of the two linear sections of Φ_{B0}-$q/2$ kT. The energy-dependent profiles of the surface states (N_{ss}) were also derived using the forward-bias I-V data.

1. Introduction

The electrical properties of metal/semiconductor (MS) structures with/without an interlayer have been extensively investigated for their applications in integrated circuits, photodetectors, temperature sensors, and solar cells. Gallium arsenide (GaAs), a promising III - V compound semiconductor, is widely used in optoelectronics and high-speed electronic devices due to its direct band gap and high electron mobility. Metal/GaAs SDs are essential components in high-speed microelectronic applications, microwave communication structures, and metal-semiconductor field-effect transistors (FETs). A thorough understanding of their electrical characteristics is crucial since most contacts are not strictly MS unless meticulously fabricated [1–6]. Metal-polymer-semiconductor connections, which allow for continuous adjustment of the diode barrier height and other diode parameters, have garnered significant attention [7–11]. These investigations were carried out to create metal-polymer-semiconductor connections and improve their electrical characteristics.

However, experimental data often lack precise information regarding the Schottky diode characteristics and possible current transport mechanisms (CTMs), particularly at room temperature (RT) or within a narrow range of temperatures. As a result, the experimental I-V characteristics of such devices should be employed to investigate the interfacial layer and carrier transport mechanism, particularly over a wide low-temperature range. Analyzing the I-V characteristics of MS contacts using the TE model frequently reveals an unusual increase in Schottky BH and a drop in n with rising temperature. These findings have recently been addressed by adding the concept of barrier-inhomogeneities and proposing a TE model with a GD function in several research [12–18].

In this study, we planned to construct Au/(P3DMTFT)/n-GaAs SDs and then analyze their CTMs and fundamental electrical properties using forward-bias I-V measurements between of 80–320 K. These electrical characteristics and CTMs were found to strongly correlate with the applied electric field and temperature. The lateral SBH inhomogeneity model effectively accounts for the observed higher ideality factor values, deviation from the linearity in the conventional Richardson curve, the lower-than-expected A* value from the plot's intercept, and an increase

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https://doi.org/10.1016/j.physb.2025.416949
Received 26 November 2024; Received in revised form 11 January 2025; Accepted 19 January 2025
Available online 20 January 2025

of Φ_{B0} with an increase in temperature.

2. Experimental procedure

The n-GaAs chip with a (100) surface orientation and carrier density of (2–5)x10^{15}/cm^3 underwent cleaning and polishing. To eliminate contaminants, the n-type GaAs chip was soaked in a ($5H_2SO_4$+H_2O_2+H_2O) solution for 1 min, followed by immersion in an H_2O + HCl solution, and then rinsed with 18 MΩ-cm deionized water. It was dried using high-purity nitrogen. In a high-vacuum coating device at approximately 10 μT pressure, high-purity Au was evaporated onto the chip's reverse side. The n-GaAs chip was subjected to a high vacuum thermal-evaporation system, where high-quality (99.999 %) Au (200 nm) metal was thermally coated on the whole back of the wafer under 0.1 μT. The n-GaAs/Au chip was then sintered/annealed at 500 °C to produce a low-resistance ohmic contact. Afterward, the polymer Poly[3-(2,5-dimethyl-4-thienyl) phenylthiophene] (P3DMTFT) was applied to the front of the n-GaAs. Finally, Schottky contacts were created by evaporating Au dots with a 1.35 mm diameter on the front surface of the n-GaAs wafer. Thus, the manufacturing methods for Au/polymer (P3DMTFT)/n-GaAs SBDs have been accomplished, and a schematic of them is shown in Fig. 1 I-V measurements were taken using a Keithley 2400 I-V source meter and a Janes VPF-475 temperature-controlled cryostat between 80 and 320 K.

3. Results-discussion

Fig. 2 depicts the semi-logarithmic *I-V* plots of Au/(P3DMTFT)/n-GaAs (SDs) measured between 80 K and 320 K in 20 K increments. The forward-bias (V > 0) *I-V* plot includes two unique linear areas with varying slopes and intercepts at each temperature, identified as Region-I (0 ≤ V ≤ 0.75) and Region-II (0.75 ≤ V ≤ 1.5). These plots start to diverge from linearity at sufficiently higher bias voltages due to the existence of series resistance (R_s) and the interlayer (P3DMTFT). The unsaturated or "soft saturation" seen in the reverse-bias ln(I)-V curve is attributed to generation/recombination currents, a drop in image strength in the BH, the interface polymer layer (P3DMTFT), and low shunt resistance (R_{sh}) [19]. Schottky-type diodes' CTMs can involve multiple charge transport mechanisms, like TE, thermionic-field/field-emission (TFE and FE) theory, generation and recombination (GR), and the To-anomaly, particularly at lower temperatures and acceptor/donor atoms with higher doping into the semiconductor [12–16].

The I-V relationship in a Schottky diode can be investigated using the TE model. The slope and intercept values of the forward bias *I-V* plot, combined with the equations [1], can be used to calculate the values of ideality factor (n), zero-bias barrier height (Φ_{B0}), and the reverse saturation current (I_0) [20,21]:

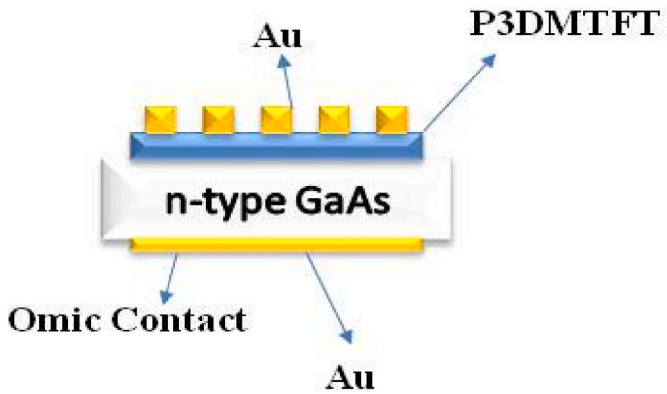

Fig. 1. The structure of Au/(P3DMTFT)/n-GaAs SDs.

$$I = I_{01}\left[exp\left(\frac{q(V-IR_s)}{n_1 kT}\right)-1\right]+I_{02}\left[exp\left(\frac{q(V-IR_s)}{n_2 kT}\right)-1\right] \quad (1)$$

$$I_{01} = AA^{*}T^{2}\ exp\left(-\frac{q}{kT}\Phi_{B01}\right) \quad (2)$$

$$I_{02} = AA^{*}T^{2}\ exp\left(-\frac{q}{kT}\Phi_{B02}\right) \quad (3)$$

$$\Phi_{B0} = \frac{kT}{q}ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \quad (4)$$

$$n = \frac{q}{kT}\left(\frac{dV}{d(ln(I))}\right) \quad (5)$$

In these equations, n_1 and n_2 are ideality factors, while I_{01} and I_{02} are the reverse-saturation currents for Regions I and II, respectively. In addition, A, A^*, and k refer to the diode area, the A^* (8.16 A $cm^{-2}K^{-2}$ for n-GaAs [22]), and the Boltzmann constant. Table 1 shows the computed values of n, I_0, and Φ_{B0} for the two regions of the Au/(P3DMTFT)/n-GaAs SDs. As demonstrated in the table, all parameters are strongly temperature-dependent: n decreases, while Φ_{B0} increases with rising temperature in both Region I and Region II. The presence of a GD at the interface accounts for the association between n and Φ_{B0} with temperature [22,23]. Furthermore, even at ambient temperature, n exceeds the ideal value (=1). This phenomenon can be explained by a variety of reasons, including the density of interface states, a high probability of electrons/holes recombination in the depletion zone, the presence of tunneling current, and the interface layer [24]. However, such high n values, particularly at low temperatures, cannot be attributed only to these factors [25–27]. Instead, the large n values observed in both regions at room and low temperatures are primarily attributed to barrier inhomogeneity. The current transmission through the MIS-type SBD is temperature-enabled, allowing electrons at low temperatures to overcome lower barriers or patches, resulting in high ideality factor values. However, at sufficiently high temperatures, more electrons gain enough energy to pass the higher barrier [25–27].

To identify the primary conduction mechanism in both Region I and Region II, theoretical (for n is equal to unity) and experimental $n.kT/q$ - kT/q curves were created, as shown in Fig. 3. As seen in Table 1, the value of n declines with increasing temperature in Region I, while the ($n.kT/q$) values stay relatively constant throughout temperatures. This data indicates that Field Emission (FE) is the dominant mechanism in Region I.

In addition, in Region II, the ($n.kT/q$) values remain constant at low temperatures but increase linearly with increasing temperature. The E_{00} value is compared with kT to determine whether the TFE or FE emission theory prevails. TE is dominant if qE_{00}/kT is much less than 1, TFE is dominant if it is roughly equal to 1, and FE is dominant as CTM if it is much greater than 1. As shown in Fig. 3, the value of E_{00} was found to be higher than the thermal energy (kT/q) for each temperature for Region-I and II. These results indicate that, in addition to TE theory, the FE mechanism may also dominate in Region I, while TFE dominates in Region II.

To learn more about BH and the Richardson constant (A^*), the ln(I_0/T^2) - q/kT relationship was plotted using Equation (6) and is shown in Fig. 4. Fig. 4 depicts the usual Richardson plot of Au/(P3DMTFT)/n-GaAs SDs, which displays a linear trend between 140K and 320K.

$$ln\left(\frac{I_0}{T^2}\right) = ln(AA^{*}) - \frac{q\Phi_{B0}}{kT} \quad (6)$$

Table 2 shows the A^* values for regions I and II of Au/(P3DMTFT)/n-GaAs SDs, which were obtained from equation (6) to be 5.63×10^{-8} A cm^{-2} K^{-2} and 5.82×10^{-7} A cm^{-2} K^{-2}, respectively. These computed A^* values are significantly lower than the theoretical value of 8.16 A/(cm^2. K^2) [22]. The theoretical and actual values differ significantly due to a

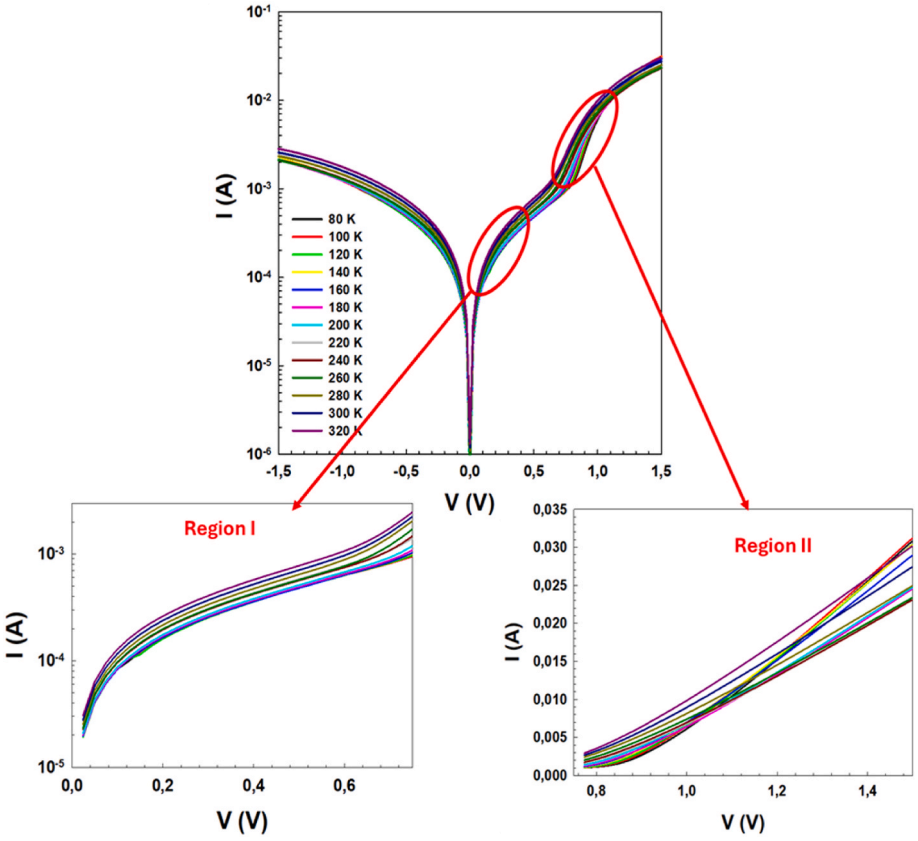

Fig. 2. The I-V plot for Au/(P3DMTFT)/n-GaAs SD at various temperature.

Table 1
The calculated values of n, I_o, and Φ_{B0} for Au/(P3DMTFT)/n-GaAs SDs at various temperatures.

T (K)	Region I				Region II			
	n_1	I_{01} (A)	Φ_{B01} (eV)	$n_1.T$ (K)	n_2	I_{02} (A)	Φ_{B02} (eV)	$n_2.T$ (K)
80	41.49	8.27×10^{-5}	0.111	3319.27	15.94	5.91×10^{-7}	0.145	5100.95
100	33.35	8.13×10^{-5}	0.142	3335.89	12.58	5.72×10^{-7}	0.185	4028.26
120	27.73	8.02×10^{-5}	0.174	3328.03	10.74	7.40×10^{-7}	0.223	3437.61
140	24.44	8.40×10^{-5}	0.207	3422.34	9.42	1.10×10^{-6}	0.259	3015.14
160	21.35	8.36×10^{-5}	0.240	3416.59	8.73	1.89×10^{-6}	0.292	2793.6
180	19.03	8.62×10^{-5}	0.273	3425.98	8.38	3.32×10^{-6}	0.324	2681.6
200	16.99	8.80×10^{-5}	0.307	3398.56	8.31	6.00×10^{-6}	0.353	2660.06
220	15.24	8.80×10^{-5}	0.341	3353.45	8.13	1.00×10^{-5}	0.382	2601.6
240	13.97	9.89×10^{-5}	0.373	3353.45	7.92	1.49×10^{-5}	0.413	2537.41
260	12.89	1.01×10^{-4}	0.408	3353.45	7.81	2.30×10^{-5}	0.441	2499.2
280	11.97	1.08×10^{-4}	0.441	3353.45	7.57	3.28×10^{-5}	0.470	2422.4
300	11.17	1.18×10^{-4}	0.474	3353.45	7.29	4.40×10^{-5}	0.499	2335.36
320	10.48	1.23×10^{-4}	0.508	3353.45	6.98	6.01×10^{-5}	0.527	2233.6

spatial inhomogeneity of the BH and patches at the M/S interface [24]. Furthermore, the experimentally obtained values deviate from the predictions of the standard TE theory.

As previously indicated, increasing temperature decreases the n value and increases Φ_{B0}. To understand the relationship between these two factors and the shape of BH, the Φ_{B0}–n diagram should be examined. Fig. 5 shows the Φ_{B0}–n plot for Au/(P3DMTFT)/n-GaAs SDs. The Φ_{B0}–n plot exhibits a linear trend from 140 to 320 K, as depicted in the figure above. This figure's intercept can be used to calculate the average value of BH ($\overline{\phi_{B0}}$). Therefore, ($\overline{\phi_{B0}}$) is calculated to be 0.731 eV in Region I and 1.542 eV in Region II.

The abnormal behavior of the I-V plot is attributed to the spatial variation of the BH. The spatial barrier-inhomogeneities in Schottky diodes are mostly defined by the GD function in equation [25,28].

$$P(\Phi_{B0}) = C_{\Phi_{B0}} . exp\left(\frac{(\Phi_{B0} - \overline{\phi_{B0}})^2}{2\sigma_{s0}^2}\right) \tag{7}$$

where $C_{\Phi_{B0}}$ $\left(= 1/(\sigma_{s0}\sqrt{2\pi}) \right)$ is the normalization constant for the Gaussian barrier-distribution. The barrier inhomogeneity replaces the total current $I(V)$ function, which is stated as follows:

$$I(\mathrm{V}) = \int_{-\infty}^{+\infty} I(\Phi_{B0}, V).P(\Phi_{B0}).d(\Phi_{B0}) \tag{8}$$

where $P(\Phi_{B0})$ denotes the normalized distribution function that calculates the probability of correctness given BH.

The $I\ (\Phi_{B0}, V)$ reflects the current in forward bias V for Φ_{B0} and is

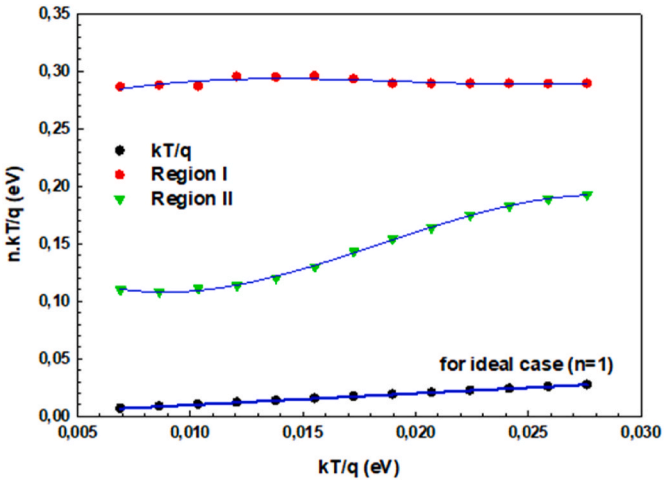

Fig. 3. The (n.kT/q) vs (kT/q) plot for Au/(P3DMTFT)/n-GaAs SD.

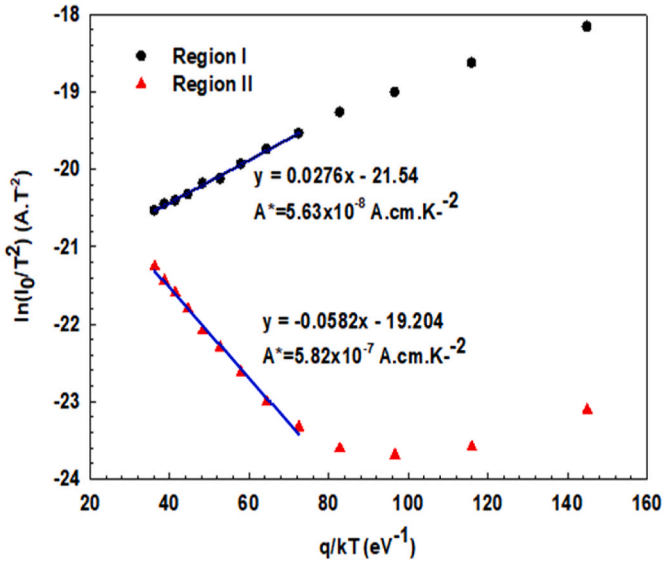

Fig. 4. The conventional Richardson plot for Au/(P3DMTFT)/n-GaAs SD.

given by the equation below.

$$I(V) = AA^{*}T^{2}\, exp\left[-\frac{q}{kT}\left(\overline{\phi_{B0}} - \frac{q\sigma_{s0}^{2}}{2kT}\right)\right] exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - exp\left(-\frac{qV}{kT}\right)\right] \tag{9}$$

The apparent n (n_{ap}) and apparent BH (Φ_{ap}) are stated as follows:

$$\Phi_{ap} = \overline{\phi_{B0}} - \frac{q\sigma_{s0}^{2}}{2kT} \tag{10}$$

$$\frac{1}{n_{ap}} - 1 = -\rho_{2} - \frac{q\rho_{3}}{2kT} \tag{11}$$

The standard deviation (σ_{s0}) is temperature-independent, while the voltage coefficients (ρ_2 and ρ_3) may vary with temperature. To better understand the link between n and Φ_{B0}, Fig. 6 shows the Φ_{B0} - $q/2$ kT plot for Au/(P3DMTFT)/n-GaAs SDs. This chart depicts two unique regimes for Region I and Region II: the high-temperature (HT) region, ranging from 200 to 320 K, and the low-temperature (LT) region, spanning from 80 to 180 K. The average $\overline{\phi_{B0}}$ values are 0.826 eV, 0.381 eV, 0.805 eV, and 0.449 eV for HTs and LTs in Region I and Region II, respectively. Similarly, σ_{s0} is found to be 0.826 eV, 0.381 eV, 0.805 eV, and 0.449 eV for HTs and LTs in Region I and Region II, respectively. All these values are summarized in Table 2. The temperature range represented by each line indicates the region in which the relevant distribution is effective. It is worth noting that the DGD function is applicable across the entire experimental temperature range.

Fig. 7 shows the (n^{-1}-1) vs $q/2$ kT plot for Au/(P3DMTFT)/n-GaAs SDs, which was used to calculate ρ_2 and ρ_3. The plot in Fig. 7 reveals two unique linear regimes for each location. The ρ_2 values were determined to be 0.847, 0.8929, 0.825, and 0.835 for HTs and LTs in Region I and Region II, respectively. The ρ_3 values were 0.0033 eV, 0.0007 eV, 0.002 eV, and 0.0014 eV for HTs and LTs in Region I and Region II, respectively. All obtained values are summarized in Table 2. Figs. 6 and 7 show two separate linear regimes, due to the double GD of BHs in the N_{ss} and Au/(P3DMTFT)/n-GaAs SDs. Similar findings have been published in the literature in recent years [24,28–32].

The Richardson curve was changed by combining Equations (6) and (10) as follows:

$$ln\left(\frac{I_0}{T^2}\right) - (0.5)\left(\frac{q\sigma_{s0}}{kT}\right)^{2} = ln(AA^{*}) - \left(\frac{q\overline{\phi_{B0}}}{kT}\right) \tag{12}$$

The standard Richardson plot has been changed by combining

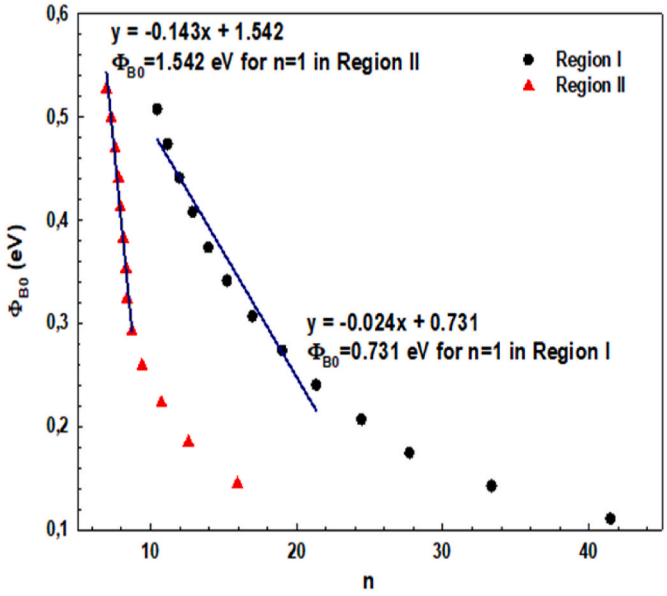

Fig. 5. The Φ_{B0} - n plot for Au/(P3DMTFT)/n-GaAs SD.

Table 2
Some of the obtained critical parameters for Au/(P3DMTFT)/n-GaAs SDs from various figures.

Region	σ_{s0} (eV)	ρ_2	ρ_3 (eV)	$\overline{\Phi_{B0}}$ (eV)		A* (A/cm^{2}K^2)	
	(from Fig-6)	(from Fig-7)	(from Fig-7)	(from Fig-6)	(from Fig-8)	(from Fig-4)	(from Fig. 8)
I	0.134 for HT	0.847 for HT	0.0033 for HT	0.826 for HT	0.817 eV for HT	5.63×10^{-8}	7.913 for HT
	0.062 for LT	0.8929 for LT	0.0007 for LT	0.381 for LT	0.382 eV for LT		15.542 for LT
II	0.126 for HT	0.825 for HT	0.002 for HT	0.805 for HT	0.808 eV for HT	5.82×10^{-7}	10.211 for HT
	0.066 for LT	0.835 for LT	0.0014 for LT	0.449 for LT	0.456 eV for LT		18.238 for LT

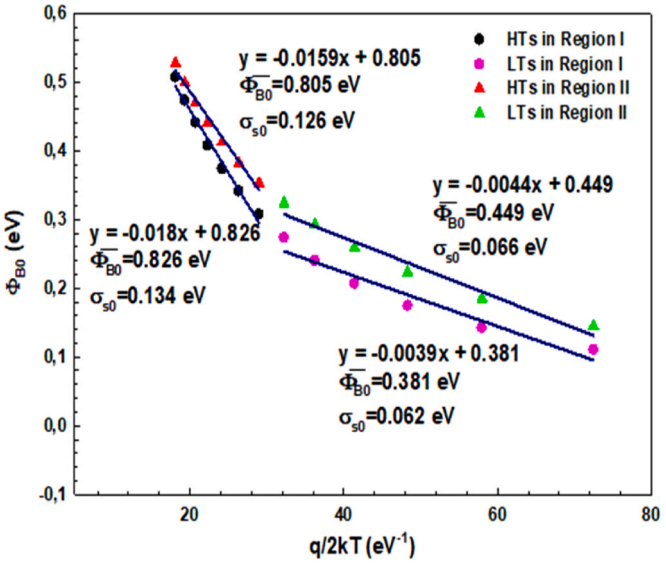

Fig. 6. The Φ_{B0} - (q/2 kT) plot for Au/(P3DMTFT)/n-GaAs SD.

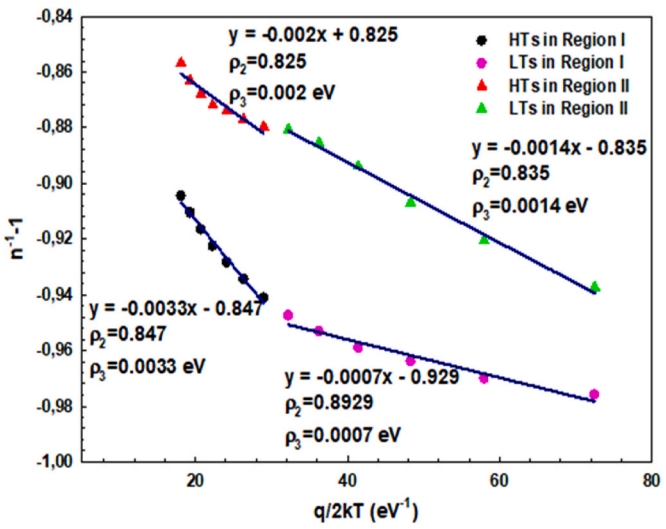

Fig. 7. The (n^{-1}-1) vs (q/2 kT) plot for Au/(P3DMTFT)/n-GaAs SD.

Equations (6) and (10) as follows: In Fig. 8, the $\ln(I_0/T^2)-(0.5).(q\sigma_{s0}/kT)^{0.5}$ vs. (q/kT) plot for Au/(P3DMTFT)/n-GaAs SDs exhibits two distinct linear regimes in each region. The graphic presents the values of $\overline{\phi_{B0}}$ and A^*. The ($\overline{\phi_{B0}}$) values for HTs and LTs in Regions I and II are 0.817 eV, 0.382 eV, 0.808 eV, and 0.456 eV, respectively. The A^* values for HTs and LTs in Region I are 7.913 A cm^{-2}K^{-2}, 15.542 A cm^{-2}K^{-2}, 10.211 A cm^{-2}K^{-2}, and 18.238 A cm^{-2}K^{-2}, respectively, whereas in Region II, they are 7.913 A cm^{-2}K^{-2}, 15.542 A cm^{-2}K^{-2}, 10.211 A cm^{-2}K^{-2}, and 18.238 A cm^{-2}K^{-2}. Table 2 shows all of the values acquired. Table 2 shows good agreement between the average values of $\overline{\phi_{B0}}$ derived from Figs. 6 and 8. The experimental A^* value for Au/(P3DMTFT)/n-GaAs SDs is close to the theoretical value. Consistency in A^* and $\overline{\phi_{B0}}$ values is crucial for ensuring accurate findings across multiple calculations.

As discussed in earlier sections, N_{ss} significantly impacts the functionality of electronic devices, making its analysis essential. The energy density distribution of *Nss* vs. (*Ess-Ev*) was also investigated using forward-bias I-V characteristics [23,33,34]. The voltage-dependent n, *n (V)*, is defined as follows;

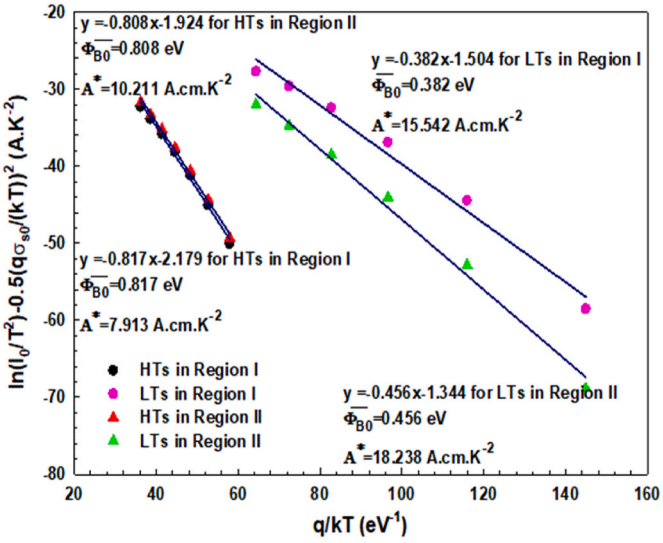

Fig. 8. The modified Richardson plot for Au/(P3DMTFT)/n-GaAs SD.

$$n(V)=\frac{qV}{kTln\left(\frac{I}{I_0}\right)}=\frac{\delta_i}{\varepsilon_i}\left[\left(\frac{\varepsilon_s}{W_d}+qN_{ss}\right)+1\right] \tag{13}$$

To account for the bias voltage, the effective BH, Φ_e, is calculated as follows:

$$\phi_e=\phi_{B0}+(1-1/n(V)).V \tag{14}$$

E_{ss} is the energy of the surface states relative to the bottom of the conduction band (E_c) at the semiconductor surface.

$$E_c-E_{ss}=q(\phi_e-V) \tag{15}$$

Thus, the density distribution of the N_{ss} depends on energy (E_c-E_{ss}) given by; [34,35],

$$N_{ss}=\frac{1}{q}\left[\frac{\varepsilon_i}{\delta_i}(n(V)-1)-\frac{\varepsilon_s}{W_d}\right] \tag{16}$$

As illustrated in Fig. 9, the E_c-E_{ss} value changes from 0.061 eV to 0.491 eV, whereas the N_{ss} value ranges from 1.28 × 10^{14}/(eV.cm^2) to 1.54 × 10^{13}/(eV.cm^2). The N_{ss} value increases exponentially from the mid-gap of Si to the bottom of the conduction band (E_c) at each temperature. As the temperature increases, charges rearrange and reorder, shifting closer to the *Ec* edge. Furthermore, the N_{ss} value drops with

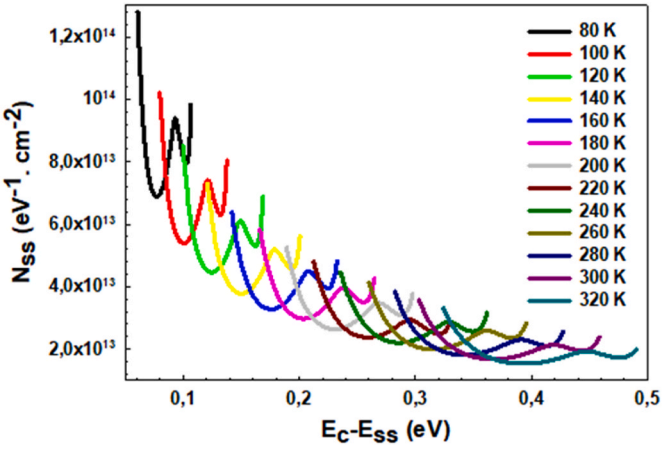

Fig. 9. The N_{ss} vs (E_c-E_{ss}) plot at various temperatures for Au/(P3DMTFT)/n-GaAs SD.

increasing temperature. Similar findings for Schottky-type diodes have been reported recently in the literature [36–40].

4. Conclusion

Au/(P3DMTFT)/n-GaAs SDs were examined throughout a temperature range of 80-32K, with 20 K increments. The temperature was found to affect key parameters, such as Φ_{B0} and n, in Au/(P3DMTFT)/n-GaAs SDs. Experimental results demonstrate that as the temperature rises, the Φ_{B0} value rises while the n value decreases. The A^* values obtained from standard Richardson plots were also found to be much lower than their theoretical values. These findings also suggest a significant departure from classic TE theory, particularly at low temperatures. Plotting nkT/q vs. kT/q, Φ_{bo} vs. n, and Φ_{bo} vs. $q/2$ kT curves revealed additional CTMs that could explain the anomaly. These graphs demonstrate tunneling (FE, TFE) and DGD of BH distribution are more effective conduction processes than TE. Additionally, N_{ss} and (E_c-E_{ss}) curves were produced from forward bias I-V data using the Card-Roderick approach, which takes into account the voltage dependence of n and BH values. It has been discovered that the N_{ss} value lowers with rising temperature and shifts towards the semiconductor's mid-gap energy as a result of rearrangement-reconfiguration caused by temperature and electric fields.

CRediT authorship contribution statement

Yılmaz Kansız: Resources, Methodology, Funding acquisition. **Ömer Sevgili:** Writing – original draft, Data curation. **Ahmet Faruk Özdemir:** Writing – review & editing, Writing – original draft, Supervision. **Durmuş Ali Aldemir:** Methodology, Investigation. **Maryam Abdolahpour Salari:** Formal analysis, Conceptualization. **Şemsettin Altındal:** Writing – review & editing, Writing – original draft, Supervision, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This research was funded by the Suleyman Demirel University Scientific Research Projects Management Unit (SDUBAP) under project number 3498-YL2-13. The semiconductor polymer (P3DMTFT) employed in the interface was produced in the TUBITAK 105T382 project.

Data availability

Data will be made available on request.

References

[1] E.H. Rhoderick, R.H. Williams, Metal-Semiconductor Contacts, second ed., Clarendon Press, Oxford, 1988.
[2] J.C.W. Song, K.E.J. Goh, N. Chandrasekhar, C. Troadec, Electrostatic effects of nanoscale dielectric patches in the modification of Schottky contacts, Phys. Rev. B 79 (2009) 165313, https://doi.org/10.1103/PhysRevB.79.165313.
[3] R.T. Tung, Recent advances in Schottky barrier concepts, Mater. Sci. Eng. R Reports 35 (2001) 1–138, https://doi.org/10.1016/S0927-796X(01)00037-7.
[4] T. Göksu, N. Yıldırım, H. Korkut, A.F. Özdemir, A. Turut, A. Kökce, Barrier height temperature coefficient in ideal Ti/n-GaAs Schottky contacts, Microelectron. Eng. 87 (2010) 1781–1784, https://doi.org/10.1016/j.mee.2009.10.012.
[5] R. Gupta, S.C.K. Misra, B.D. Malhotra, N.N. Beladakere, S. Chandra, Metal/semiconductive polymer Schottky device, Appl. Phys. Lett. 58 (1991) 51–52, https://doi.org/10.1063/1.104441.
[6] A. Turut, F. Köleli, Semiconductive polymer-based Schottky diode, J. Appl. Phys. 72 (1992) 818–819, https://doi.org/10.1063/1.351822.
[7] A. Usha Rani, V. Rajagopal Reddy, C. Venkata Prasad, A. Ashok Kumar, Chemical states, structural, electrical and current phenomenon properties of an Au/cobalt phthalocyanine/undoped-InP MPS-type diode with a CoPc interlayer, J. Inorg. Organomet. Polym. Mater. (2024), https://doi.org/10.1007/s10904-024-03087-3.
[8] Ş. Özden, N. Avcı, O. Pakma, İ.A. Kariper, Temperature dependent current transport mechanism of photopolymer based Al/NOA60/p-Si MPS device, J. Inorg. Organomet. Polym. Mater. 32 (2022) 1810–1818, https://doi.org/10.1007/s10904-021-02221-9.
[9] H. Altan, M. Özer, H. Ezgin, Investigation of electrical parameters of Au/P3HT: PCBM/n-6H–SiC/Ag Schottky barrier diode with different current conduction models, Superlattices Microstruct 146 (2020) 106658, https://doi.org/10.1016/j.spmi.2020.106658.
[10] H.H. Gullu, D.E. Yıldız, D.A. Kose, M. Yıldırım, Si-based photosensitive diode with novel Zn-doped nicotinate/nicotinamide mixed complex interlayer, Mater. Sci. Semicond. Process. 147 (2022) 106750, https://doi.org/10.1016/j.mssp.2022.106750.
[11] E. Marıl, The effect of (PVP-Cu2Te) organic interlayer on the electrical parameters of Al/p-Si Schottky barrier diodes (SBDs) at room temperature, Phys. B Condens. Matter 604 (2021) 412732, https://doi.org/10.1016/J.PHYSB.2020.412732.
[12] Y. Badali, H. Altan, S. Altındal, Thermal dependence on electrical characteristics of Au/(PVC: Sm2O3)/n-Si structure, J. Mater. Sci. Mater. Electron. 35 (2024) 228, https://doi.org/10.1007/s10854-023-11898-2.
[13] E. Evcin Baydilli, The effect of Cu-doping to the DLC interlayer on the temperature-dependent current-conduction mechanisms and barrier shape of the Schottky devices, Mater. Sci. Semicond. Process. 184 (2024) 108828, https://doi.org/10.1016/j.mssp.2024.108828.
[14] A. Kaymaz, Multi-Gaussian distribution of barrier height in diamond-like carbon interfacial-layered Schottky devices, Mater. Sci. Semicond. Process. 177 (2024) 108380, https://doi.org/10.1016/j.mssp.2024.108380.
[15] A. Turut, Analysis of temperature-dependent current-voltage characteristics of Schottky diodes by the modified thermionic emission current model, J. Vac. Sci. Technol. B 42 (2024) 32201, https://doi.org/10.1116/6.0003463.
[16] M. Mamor, K. Bouziane, H. Chakir, P. Ruterana, On the temperature dependence of the current conduction mode in non-homogeneous Pt/n-GaN Schottky barrier diode, Phys. B Condens. Matter 684 (2024) 415965, https://doi.org/10.1016/j.physb.2024.415965.
[17] Y.-H. Cho, S.-H. Chung, S.-R. Park, J.-S. Choi, S.-Y. Moon, H.-J. Lee, G.-H. Lee, S.-M. Koo, Effects of post-deposition annealing on temperature-dependent electrical characteristics of Ni/(Al0.1Ga0.9)2O3/4H-SiC Schottky barrier diodes, J. Mater. Sci. Mater. Electron. 35 (2024) 977, https://doi.org/10.1007/s10854-024-12551-2.
[18] S. Paul, R. Lopez, A.T. Neal, S. Mou, J. V Li, Low-temperature electrical properties and barrier inhomogeneities in ITO/β-Ga2O3 Schottky diode, J. Vac. Sci. Technol. B 42 (2024) 24004, https://doi.org/10.1116/6.0003401.
[19] E. Evcin Baydilli, Ş. Altındal, H. Tecimer, A. Kaymaz, H. Uslu Tecimer, The determination of the temperature and voltage dependence of the main device parameters of Au/7%Gr-doped PVA/n-GaAs-type Schottky Diode (SD), J. Mater. Sci. Mater. Electron. 31 (2020) 17147–17157, https://doi.org/10.1007/s10854-020-03799-5.
[20] Ş. Altındal, Ö. Sevgili, Y. Azizian-Kalandaragh, A comparison of electrical parameters of Au/n-Si and Au/(CoSO4–PVP)/n-Si structures (SBDs) to determine the effect of (CoSO4–PVP) organic interlayer at room temperature, J. Mater. Sci. Mater. Electron. 30 (2019) 9273–9280.
[21] A. Eroğlu, S. Demirezen, Y. Azizian-Kalandaragh, Ş. Altındal, A comparative study on the electrical properties and conduction mechanisms of Au/n-Si Schottky diodes with/without an organic İnterlayer, J Mater Sci, Mater Electron 31 (2020) 14466–14477, 2020.
[22] H. Durmuş, A. Tataroğlu, Ş. Altındal, M. Yıldırım, The effect of temperature on the electrical characteristics of Ti/n-GaAs Schottky diodes, Curr. Appl. Phys. 44 (2022) 85–89, https://doi.org/10.1016/j.cap.2022.09.015.
[23] J.H. Werner, G.H. H., Barrier inhomogeneities at Schottky contacts, J. Appl. Phys. 69 (1991) 1522–1533, https://doi.org/10.1063/1.347243.
[24] Ö. Sevgili, On the examination of temperature-dependent possible current-conduction mechanisms of Au/(nanocarbon-PVP)/n-Si Schottky barrier diodes in a wide range of voltage, J. Mater. Sci. Mater. Electron. 32 (2021) 10112–10122, https://doi.org/10.1007/S10854-021-05669-0/FIGURES/13.
[25] O. Çiçek, Ş. Altındal, Y. Azizian-Kalandaragh, A highly sensitive temperature sensor based on Au/Graphene-PVP/n-Si type Schottky diodes and the possible conduction mechanisms in the wide range temperatures, IEE Sensors Journal 20 (2020) 14081–14089. https://www.ieee.org/publications/rights/index.html.
[26] A. Buyukbas-Ulusan, A. Tataroglu, S. Altındal-Yerişkin, Analysis of the current transport characteristics (CTCs) in the Au/n-Si Schottky diodes (SDs) with Al2O3 interfacial layer over wide temperature range, ECS Journal of Solid State Science and Technology 12 (2023) 083010, 12.
[27] S. Altindal Yerişkin, K. Yildiz, A. Dere, Y. Orman, F. Yakuphanoğlu, Quaternary functional semiconductor device-based temperature sensors for low and high temperatures (LTs, HTs), Phys. Scripta 99 (2024) 125947, https://doi.org/10.1088/1402-4896/ad8d38.
[28] A.F. Özdemir, A. Turut, A. Kökçe, The double Gaussian distribution of barrier heights in Au/n-GaAs Schottky diodes from I–V–T characteristics, Semicond. Sci. Technol. 21 (2006) 298, https://doi.org/10.1088/0268-1242/21/3/016.
[29] Ö. Sevgili, S. Yılmaz, Ş. Altındal, E. Bacaksız, Ç. Bilkan, The investigation of current-conduction mechanisms of Te/NaF: CdS/SnO2 structure in wide temperature range of 80–400 K, Proc. Natl. Acad. Sci. India Sect. A Phys. Sci. 87 (2017) 409–417, https://doi.org/10.1007/s40010-017-0366-5.

[30] Ş. Altındal, A.F. Özdemir, Ş. Aydoğan, A. Türüt, Discrepancies in barrier heights obtained from current-voltage (IV) and capacitance-voltage (CV) of Au/PNoMPhPPy/n-GaAs structures in a wide range of temperature, J. Mater. Sci. Mater. Electron. (2022) 1–14, https://doi.org/10.1007/s10854-022-08181-1.
[31] Ö.F. Bakkaloğlu, K. Ejderha, H. Efeoğlu, Ş. Karataş, A. Türüt, The Temperature dependence of electrical parameters of the Cu/n-Si metal-semiconductor Schottky structures, J. Mol. Struct. 1224 (2021) 129057, https://doi.org/10.1016/j.molstruc.2020.129057.
[32] Ö. Sevgili, İ. Orak, The investigation of current condition mechanism of Al/Y2O3/p-Si Schottky barrier diodes in wide range temperature and illuminate, Microelectron. Reliab. 117 (2021) 114040, https://doi.org/10.1016/J.MICROREL.2021.114040.
[33] S.M. Sze, Physics of Semiconductor Devices, second ed., Willey, New York, 1981.
[34] H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes, J. Phys. D Appl. Phys. 4 (1971) 1589, https://doi.org/10.1088/0022-3727/4/10/319.
[35] A. Tataroğlu, Ş. Altındal, Y. Azizian-Kalandaragh, Comparison of electrical properties of MS and MPS type diode in respect of (In2O3-PVP) interlayer, Phys. B Condens. Matter 576 (2020) 411733.
[36] V. Rajagopal Reddy, V. Manjunath, V. Janardhanam, Y.H. Kil, C.J. Choi, Electrical properties and current transport mechanisms of the Au/n-GaN Schottky structure with solution-processed high-k $BaTiO_3$ interlayer, J. Electron. Mater. 43 (9) (2014) 3499–3507.
[37] A. Büyükbaş Uluşan, A. Tataroğlu, Y. Azizian-Kalandaragh, Ş. Altındal, On the conduction mechanisms of Au/(Cu2O-CuO-PVA)/n-Si (MPS) Schottky barrier diodes (SBDs) using current-voltage–temperature (I-V-T) characteristics, J. Mater. Sci. Mater. Electron. 29 (2018) 159–170.
[38] A.A. Alsaç, T. Serin, S.O. Tan, Ş. Altındal, Identification of current transport mechanisms and temperature sensing qualifications for Al/(ZnS-PVA)/p-Si structures at low and moderate temperatures, IEEE Sensor. J. 22 (2021) 99–106.
[39] M.K. Hudait, K.P. Venkateswarlu, S.B. Krupanidhi, Electrical transport characteristics of Au/n-GaAs Schottky diodes on n-Ge at low temperatures, Solid State Electron. 45 (2001) 133.
[40] İ. Taşçıoğlu, G. Pirgholi-Givi, S. Altındal Yerişkin, Y Azizian-Kalandaragh Examination on the current conduction mechanisms of Au/n-Si diodes with ZnO-PVP and ZnO/Ag2WO4-PVP interfacial layers, J. Sol. Gel Sci. Technol. 107 (2023) 536–547.