Increase in current density for metal contacts to n-germanium by inserting TiO_2 interfacial layer to reduce Schottky barrier height

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Metal contacts to n-type Ge have poor performance due to the Fermi level pinning near the Ge valence band at metal/Ge interfaces. The electron barrier height can be reduced by inserting ultrathin dielectrics at the metal-semiconductor interface. However, this technique introduces tunneling resistance from the large conduction band offset (CBO) between the insulator and Ge. In this work, the CBO between TiO_2 and Ge is estimated to range from -0.06 to -0.26 eV so tunneling resistance can be reduced. By inserting 7.1 nm TiO_2 between Al and n-Ge, current densities increased by about 900× at 0.1 V and 1200× at -0.1 V compared to contacts without TiO_2. © *2011 American Institute of Physics*. [doi:10.1063/1.3562305]

Germanium is a promising material to replace silicon as the channel material in metal oxide semiconductor field effect transistors (MOSFETs) due to its high electron and hole mobility. While p-channel MOSFETs have been demonstrated with superior performance, n-channel MOSFETs have suffered from poor drive current. One reason for this has been the high contact resistance to the n+ source/drain (S/D) regions due to the high electron Schottky barrier height (Φ_{BN}) as a result of Fermi level pinning close to the Ge valence band (VB) at metal/Ge junctions.[1,2]

Recent experiments have demonstrated Fermi level depinning by inserting thin tunnel barriers such as Si_3N_4,[3,4] Ge_3N_4,[5] and Al_2O_3 (Refs. 6 and 7) at the metal-semiconductor interface. Using a low work function metal can, therefore, result in lower Φ_{BN}. However, these insulators introduce a large tunneling resistance due to significant conduction band offset (CBO) to Ge. Simulations performed by Roy *et al.*[8] have shown that low specific contact resistivity to n-type Ge can only be achieved if the insulating layer is kept sufficiently thin, typically less than 1 nm, so as not to introduce a large tunneling resistance. It was identified that TiO_2 may be a good candidate since it has a nearly zero CBO to Ge for lower tunneling resistance.

In this work, we use TiO_2 as the insulating layer in a metal-insulator-semiconductor (MIS) structure to evaluate the suitability of using TiO_2 for contacts to n+ S/D regions for application in n-channel Ge MOSFETs. The MIS device cross-section is depicted in Fig. 1.

n-type Ge doped with electrically active concentration of $\sim 10^{19}$ cm^{-3} was heteroepitaxially deposited by chemical vapor deposition (CVD) on n-type Si wafers. This relatively high level of doping was used since our aim is to achieve high currents to n+ S/D. 400 nm SiO_2 was then deposited by CVD at 400 °C for device isolation. Standard lithography techniques were used to pattern contact holes. Atomic layer deposition (ALD) of TiO_2 at 150 °C was done using tetrakis(dimethylamido)titanium and water as the precursors. Control samples using ALD of Al_2O_3 at 200 °C were also made using trimethylaluminum and water as the precursors. Various thicknesses of TiO_2 and Al_2O_3 were deposited by changing the number of ALD cycles. Samples without a dielectric layer were also fabricated to observe the contact characteristics of metal directly on Ge. 100 nm of Al was deposited by e-beam evaporation onto the sample surface. Standard lithography techniques were used to pattern the Al. An argon sputter etch was performed to completely etch exposed TiO_2 using the Al contact as the mask. Due to the low band gap of TiO_2, electrical conduction has been observed in some TiO_2 films;[9] this etch, therefore, ensures complete isolation between adjacent devices. Finally, 300 nm of Al was deposited by e-beam evaporation onto the backside of the samples to get a good contact.

The VB offsets (VBO) of TiO_2/Ge and Al_2O_3/Ge were measured using synchrotron radiation photoelectron spectroscopy (SRPES). Low energy ($h\nu$=120–160 eV) photons from the Stanford Synchrotron Radiation Lightsource beam line 8-1 allows precise measurement of the VBO by taking the difference between the VB spectrum of TiO_2 or Al_2O_3 and the VB spectrum of bulk Ge, using the Ge 3d peak for alignment. Figure 2(a) shows the VB spectra of TiO_2 on Ge and bulk Ge, indicating a VBO of 2.9 eV. The band gap of amorphous TiO_2 has been reported to be 3.3–3.5 eV,[10] while the crystalline phases of TiO_2 have smaller band gaps.[11] We

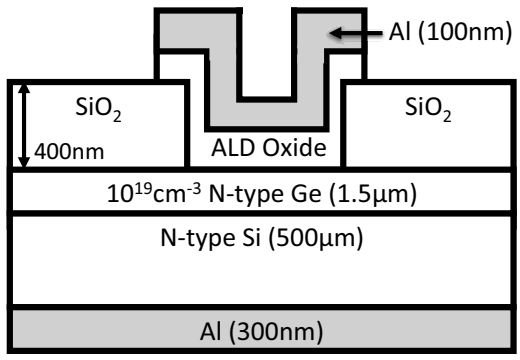

FIG. 1. Schematic cross-section of the MIS device. ALD of both TiO_2 and Al_2O_3 were used.

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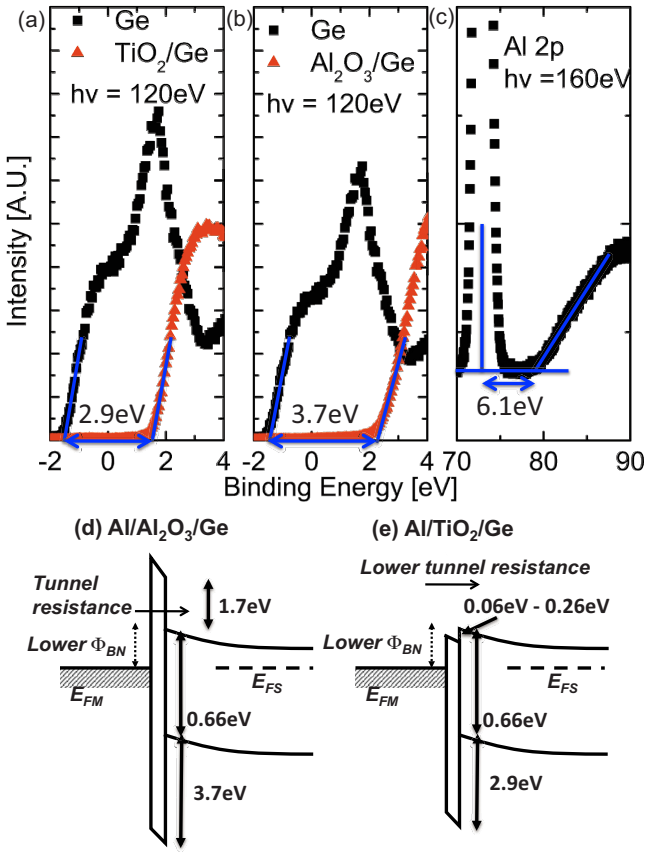

FIG. 2. (Color online) SRPES spectra for (a) TiO_2 and Ge VBs, (b) Al_2O_3 and Ge VBs, and (c) Al $2p$ peak. The photon energy used is indicated for each plot. The TiO_2/Ge and Al_2O_3/Ge VBO was determined to be 2.9 eV and 3.7 eV, respectively. The band gap of Al_2O_3 was confirmed to be 6.1 eV. Parts (d) and (e) are band diagrams summarizing the VBO and CBO data from SRPES. The metal Fermi level is drawn close to the conduction band, which assumes Φ_{BN} can be reduced.

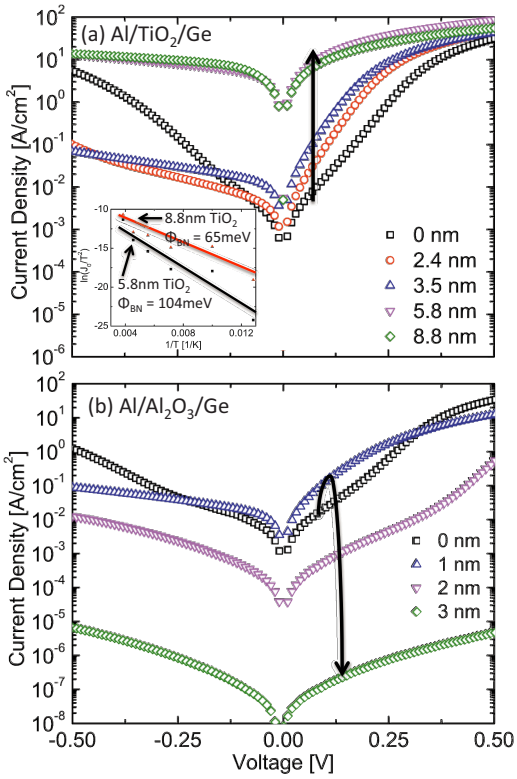

FIG. 3. (Color online) I-V characteristics of (a) Al/TiO_2/Ge and (b) Al/Al_2O_3/Ge MIS devices. With TiO_2, the forward current increases up to 5.8 nm, with no significant current degradation even up to 8.8 nm. With Al_2O_3, the forward current increases only up to 1 nm then starts decreasing rapidly. The inset of (a) shows temperature-dependent I-V measurements of the 5.8 nm and 8.8 nm TiO_2 devices, which show electron barrier heights of 104 meV and 65 meV, respectively.

expect our ALD-deposited TiO_2 films to be amorphous, although this was not confirmed. Since we use the band gap data only to calculate CBO, the larger band gap of amorphous TiO_2 represents a worst-case since it leads to a larger CBO. Using the range of band gaps for amorphous TiO_2, we obtain a CBO between -0.26 and -0.06 eV at the TiO_2/Ge interface. This low CBO value confirms the possibility that inserting TiO_2 at the metal/Ge interface may be able to achieve high current as long as Φ_{BN} can be reduced. Figure 2(b) shows the VB spectra of Al_2O_3 on Ge and bulk Ge, indicating a VBO of 3.7 eV. This is slightly larger than the typical value of ~3.3 eV obtained for Al_2O_3/Ge VBO.[12] Since our goal is to study TiO_2, we did not examine this further, but it is likely that different deposition conditions may give slightly different VBO. The ALD Al_2O_3 band gap was found to be 6.1 eV as determined from the energy loss spectrum of the Al $2p$ peak shown in Fig. 2(c), which is consistent with published results for ALD Al_2O_3.[12] We could not use this technique to determine the band gap of TiO_2 since the Ti $3p$ peak was too wide and therefore masked the energy loss onset. The VBO and CBO results are summarized in Figs. 2(d) and 2(e). Based on these band diagrams, it appears that TiO_2 MIS devices should be able to achieve higher currents than Al_2O_3 devices on the basis of CBO values, as long as the insertion of TiO_2 can also reduce Φ_{BN}. We, therefore, examine Φ_{BN} next.

The current-voltage (I-V) characteristics of Al/TiO_2/Ge and Al/Al_2O_3/Ge MIS devices were measured, using the backside as the second contact. Figure 3(a) shows the I-V characteristics of the TiO_2 devices. Without TiO_2 (0 nm curve) we observe low current as expected due to the large Φ_{BN}. The I-V characteristics are Ohmic-like due to the relatively high semiconductor doping used. As the TiO_2 thickness was increased to 2.4 and 3.5 nm, a noticeable increase in current was seen at forward and low reverse biases. This is evidence of a slight decrease in Φ_{BN}, which increases thermionic emission. At larger reverse bias, however, electron tunneling from the metal to the semiconductor through the semiconductor barrier becomes dominant. Although Φ_{BN} has been decreased, it is likely still a significant fraction of the band gap; the added TiO_2 reduces tunneling and results in current lower than the 0 nm case. With 5.8 nm TiO_2, the current saturates at values significantly higher compared to the 0 nm sample. This high current is due to a significant reduction in Φ_{BN}, which we verified later using temperature-dependent measurements. The fact that the I-V characteristics of the 5.8 and 8.8 nm samples look similar is an indication that thicker TiO_2 does not increase tunneling resistance significantly, as was predicted by our CBO estimation using SRPES.

Temperature-dependent I-V measurements were made between 78 and 260 K for the 5.8 and 8.8 nm TiO_2 devices. The inset of Fig. 3(a) is a Richardson plot of $\ln(J_0/T^2)$ versus $1/T$, where J_0 is the reverse saturation current and T is the temperature. The slope of such a plot is $-q\Phi_{BN}/k$, where q is

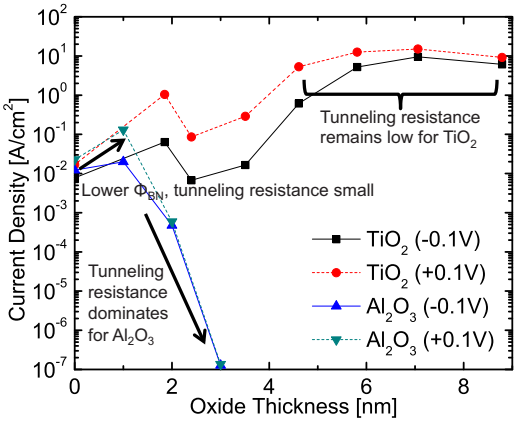

FIG. 4. (Color online) Current density of TiO_2 and Al_2O_3 devices as a function of oxide thickness at ± 0.1 V. TiO_2 devices show a substantial increase in current from reduction in Φ_{BN}. Al_2O_3 devices show an initial increase in current for the same reason but tunneling resistance with thicker Al_2O_3 quickly begins to dominate and reduces current density.

the electronic charge and k is the Boltzmann constant. The extracted Φ_{BN} was 0.104 eV (5.8 nm) and 0.065 eV (8.8 nm). This is a substantial reduction in Φ_{BN} from the 0 nm case, where $\Phi_{BN} \approx 0.58$ eV.[2] The reduction in Φ_{BN} combined with the low CBO explains the high current of the 5.8 and 8.8 nm TiO_2 devices.

In Fig. 3(b), the I-V characteristics of $Al/Al_2O_3/Ge$ devices are shown. There is a slight current increase with 1 nm of Al_2O_3 at low biases, which can be attributed to reduction in Φ_{BN}. However, with 2 nm Al_2O_3 or more, the resistance due to tunneling through Al_2O_3 starts to become significant and the current drops markedly. In a very large scale integration (VLSI) application, it would be difficult to achieve the optimum Al_2O_3 thickness uniformly across a 300 mm wafer since the current depends exponentially on thickness. This illustrates an advantage of using TiO_2 to relax the uniformity requirements, since a wide range of thicknesses still yielded high currents.

Figure 4 shows the current densities at ± 0.1 V for the TiO_2 and Al_2O_3 devices as a function of oxide thickness. Both positive and negative voltages were plotted since in a MOSFET, one contact will be forward biased while the other will be reverse biased. The trend is similar for both voltages. We focus on low biases since the high current levels at high biases causes large potential drop across the lightly doped Si substrate. The TiO_2 devices show an increase in current density due to reduction in Φ_{BN}, until about 5.8 nm TiO_2. With thicker TiO_2, the current remains roughly constant. The highest current achieved was with 7.1 nm of TiO_2, where the current increased by about 900× at 0.1 V (1.7×10^{-2} to 15.1 A/cm^2) and 1200× at −0.1 V (7.8×10^{-3} to 9.6 A/cm^2) compared to the 0 nm sample. In contrast, the Al_2O_3 devices show only a small initial increase in current up to 1 nm, again due to Φ_{BN} reduction. Tunneling resistance dominates with thicker Al_2O_3, and the current drops significantly. These results illustrate the advantage of using a low CBO material such as TiO_2 in MIS contacts.

In summary, the TiO_2/Ge interface was estimated to have a nearly zero CBO using SRPES, which makes it an excellent candidate material in an MIS contact due to its lower tunneling resistance. An ALD TiO_2 interfacial layer was used to decrease Φ_{BN}, as verified through temperature-dependent I-V measurements. We experimentally demonstrate that a TiO_2 interfacial layer is effective at significantly increasing current density for contacts to n-type Ge. This is, therefore, a promising method to increase the performance of n-channel Ge MOSFETs.

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