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p-n Junction Diagnostics to Determine Surface and Bulk Generation/Recombination Properties of Silicon Substrates

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An improved analysis of the p-n junction current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics is proposed and applied to diodes fabricated in a variety of silicon substrates. It is shown that for state-of-the-art processing conditions the diffusion current at room temperature dominates the volume leakage current. The peripheral component, on the other hand, is governed by the surface generation in the bird's-beak region surrounding the complementary metal oxide semiconductor compatible diodes. Nevertheless, a small substrate effect is observed, which can only be resolved by the proposed optimized analysis. For epitaxial wafers, the presence of the highly doped substrate can significantly reduce the volume diffusion current, while for internally gettered Czochralski material the presence of a highly defective bulk region under the denuded zone enhances this current. This complicates the recombination lifetime extraction from *I-V* characteristics.

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The strategic technology development of the semiconductor industry is closely linked to the Semiconductor Industry Association (SIA) roadmap.[1] The scaling of the feature size in ultralarge scale integrated (ULSI) technologies leads to stringent demands for defect and contamination control during processing. This implies that the tolerable amounts and concentrations are scaling along and push the limits of state-of-the-art analytical techniques. However, there is not only the question of sensitivity and detection limits, but at the same time, a large spatial resolution (in-depth and laterally) is required for a meaningful characterization of the bulk silicon and its $Si-SiO_2$ interface. There has, for example, been a significant improvement and (r)evolution over the last years with respect to "lifetime" monitoring techniques on wafer scale. However, for device operation and yield assessment it is of key importance to be able to extract the "local" values in the vicinity of the device active region, i.e., in the 2 to 3 μm near-surface layer. This requirement will only gain importance with the expected emphasis on the use of epitaxial substrates when semiconductor manufacturing lines are starting up 300 mm diam wafers for future sub-0.25 μm technologies.

It is demonstrated that by a proper combination of p-n junction diodes with different area/perimeter ratio and of gated diodes, a detailed analysis both of the interface (or surface) generation/recombination (GR) and of the bulk GR parameters can be achieved. The first part of this paper presents an improved methodology, whereby in an initial step the bulk component of the reverse current is separated from the peripheral leakage current. Subsequently, by combining these data with an improved capacitance-voltage (*C-V*) measurement procedure, the physical current components are determined, i.e., the diffusion part is separated from the generation part. The bulk recombination lifetime is extracted from the volume diffusion current component by analyzing either the forward or the reverse characteristics. The bulk generation lifetime and surface generation velocity can be derived from the respective generation components.

In the second part of this paper, this improved method is applied to diodes fabricated in different silicon substrates: Czochralski (CZ) material with different initial oxygen content, float zone (FZ) silicon, and epitaxial wafers with different epitaxial layer thickness. Based on the newly proposed analysis, some clear substrate effects can be observed for the different leakage current components. One of the major outcomes is the observation that the reverse volume current of near-ideal p-n junctions at room temperature is dominated by the diffusion current. Although this current, I_{diff}, is in the first instance determined by the dopant concentrations close to the junction at both the n- and p-side, it is demonstrated that there is still a pronounced substrate effect. While epitaxial wafers can show a strong suppression of I_{diff}, the opposite is true for internally gettered (IG) CZ material.

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Optimized Diode Analysis

Recently, considerable progress has been made in optimizing the analysis of p-n junction characteristics in order to use them as a probe of the electrical substrate and interface parameters.[2-4] The measurement and analysis strategy can be summarized as follows.[4] In a first step, the reverse and forward currents of a set of diodes with different geometries are measured, as well as the high-frequency (100 kHz-1 MHz) reverse capacitance-voltage characteristic. The resulting data can be combined to separate the different geometrical components, i.e., the volume capacitance C_A and current I_A, which scale with the diode area A, and the peripheral capacitance C_P and current I_P, which are proportional to the diode perimeter P. In the simplest case, one can combine a large-area junction with a large-perimeter (meander) diode, to separate the geometrical components, using the following linear set of equations

$$I_1 = A_1 J_A + P_1 J_P \quad [1a]$$

$$I_2 = A_2 J_A + P_2 J_P \quad [1b]$$

which is applicable to the forward (I_F) and the reverse current (I_R). Hereby are J_A the volume leakage current density (in nA/cm^2) and J_P the perimeter leakage current density (in pA/cm). After replacing currents by capacitances, a similar set of equations is applicable to the reverse capacitance. Details of the practical extraction procedure can be found in Ref. 5. Figures 1 and 2 illustrate this simple extraction technique for a 4 × 2.5 mm shallow n^+p junction fabricated on either a p-type internally gettered (IG) CZ or a 3 μm p/p^+ epitaxial wafer. The internal gettering is achieved by a high-low temperature cycle (6 h at 1100°C + 8 h at 750°C) on medium oxygen 150 mm CZ wafers. The growth of the oxygen precipitates deeper in the bulk occurs during the field oxidation. The shallow (≈0.17 μm deep) n^+p junctions, fabricated by a 3×10^{15} cm^{-2} As implantation at 70 keV followed by a rapid thermal anneal step at 1100°C, are compatible with a 0.35 μm complementary metal oxide semiconductor (CMOS) technology.[6] For Fig. 1 and 2, a rectangular diode (A_1 = 10 mm^2 and P_1 = 13 mm) is combined with a meander diode (A_2 = 0.1 mm^2 and P_2 = 80.4 mm).

Comparing the figures one can already draw some clear conclusions. First, for sufficiently large-area devices the peripheral capaci-

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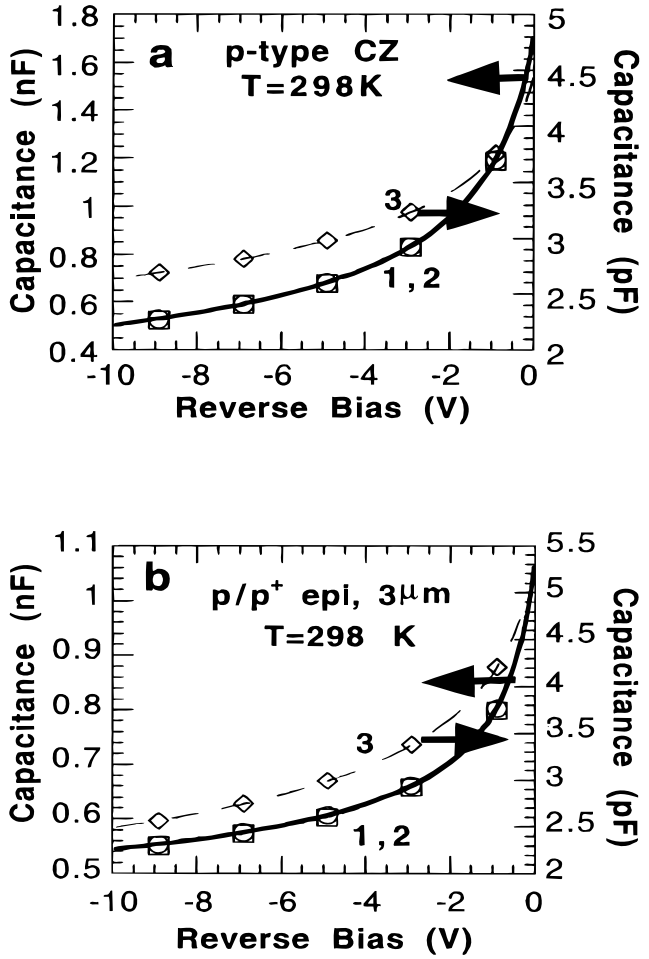

Figure 1. Total capacitance C (1) and areal (2) or peripheral component (3) for a 10 mm^2 area shallow n^+p junction fabricated on a p-type IG CZ substrate (a) and on a 3 μm p/p^+ epi substrate (b).

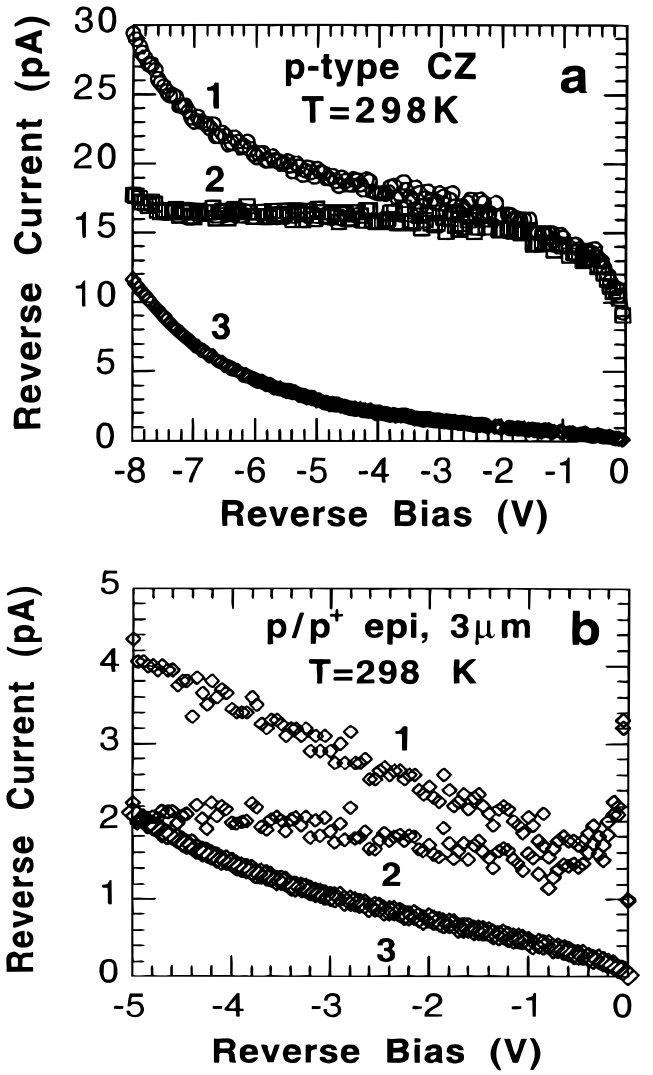

Figure 2. Total reverse current I_R (1) and areal (2) or peripheral component (3) for a 10 mm^2 area shallow n^+p junction fabricated on a p-type IG CZ substrate (a) and on a 3 μm p/p^+ epi substrate (b).

tance contribution will only be marginal (Fig. 1). This is, however, not the case if small-area junctions and/or in combination with lowly doped substrates are used for the measurements.[7] Second, it is clear that the diode formed on the epitaxial substrate has a superior leakage current behavior, compared with the one processed on the IG-CZ substrate (Fig. 2). In general, even for this large-area diode, the peripheral leakage starts to dominate at a reverse bias exceeding 5 V. Such a dominance of I_p for diodes on epitaxial wafers has also been observed on a previous set of diodes[4] and is discussed in more detail below.

To obtain a higher accuracy, the measurement results of more than two different geometry diodes can be combined in a least-squares fitting scheme.[4-6] In that case more components can be separated, like the contribution of the corner leakage J_C or capacitance C_C and a possible parasitic leakage current I_{par} and capacitance C_{par}. Four diodes are required to determine the four different current components.

In a second step, the different physical components of the reverse current are separated. Generally, one can write for the volume or peripheral current density[8,9]

$$J_A = J_{Agen} + J_{Adiff} \quad [2a]$$

$$J_P = J_{Pgen} + J_{Pdiff} \quad [2b]$$

whereby in first instance the diffusion part (subscript diff) is bias independent while the generation term increases with increasing reverse bias (or depletion width W_A). The peripheral generation current can be further split up into a substrate generation and a surface generation component, although this is not straightforward.[8,9]

The basic idea for the separation of the physical components is the use of the J_A vs. W_A plot, as shown in Fig. 3.[2,4,5,7] Hereby is W_A derived from the extracted volume capacitance C_{vol}, according to the simple relation

$$W_A = \frac{\epsilon_{si} A}{C_{vol}} \quad [3]$$

with ϵ_{si} the permittivity of silicon. For sufficiently large-area diodes, one can replace C_{vol} by C_{meas}, the measured capacitance, as was originally proposed by Murakami and Shingyouji,[2] although this will lead to erroneous results for smaller areas.[7]

In this so-called J_A-W_A method, the diffusion part is obtained from a linear extrapolation to zero depletion width. However, as seen in Fig. 3, this may not always be straightforward, if the volume current density shows a stronger than linear W_A dependence. The latter could be caused by electric-field-assisted thermal generation. As is shown elsewhere, a more general approach that can also handle field-assisted generation is based on a $\partial J_A/\partial W_A$ vs. W_A plot,[10] yielding acceptable J_{Adiff} values. The different depletion width in Fig. 3a and b is due to the difference in doping level, as can be seen in Fig. 4 and discussed below. Finally, it must be remarked that it has tacitly been assumed here that in the first instance the generation width equals the depletion width. A more accurate approach requires the

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replacement of the depletion width W_A, by the generation width W_G, as originally proposed by Calzolari and Graffi.[11] As the generation width is smaller than the depletion width, this leads to larger values for the generation lifetime. The impact of using the real generation width is important for high resistivity material, as, e.g., typically used for detector applications.[12] For ULSI compatible substrates the difference is less pronounced and typically ranges to about 20%.[7,10]

For the separation of the peripheral components, the same approach is used, i.e., plotting J_p vs. W_A and extrapolating to zero depletion width. By doing so, it is assumed that the lateral depletion width shows the same bias dependence as the vertical depletion width.[7,9] Although this is a rather crude assumption for the complex situation at the diode local oxidation of silicon (LOCOS) isolation edge, acceptable J_{pdiff} values have been obtained so far.[7] The improved two-dimensional carrier and doping profiling techniques under development will allow a quantification of the maximum error associated with more advanced isolation schemes based on, e.g., polysilicon buffered LOCOS and shallow trench.

Based on the analysis, one can also define validity criteria for the proposed numerical capacitance and current separation method.[4,5] For the capacitance extraction the validation is based on the determination of C_{par}, which is in principle bias independent. Another criterion is the built-in potential V_{bi} derived from a fit to the C_{vol}^{-2}-V_R plot, which should be close to the theoretically expected value. The validity criterion for the leakage current separation is more complex and is based on the temperature dependence of the diffusion component, which should be close to the silicon bandgap energy E_g of $\approx$1.12 eV at 300 K. [7] The activation energy of the generation current should be close to half of the bandgap energy. Another cross check is the comparison of J_{Adiff} derived from the reverse and from the forward *I-V*. This is an independent method, which therefore provides strong evidence for the overall validity of the approach used. When

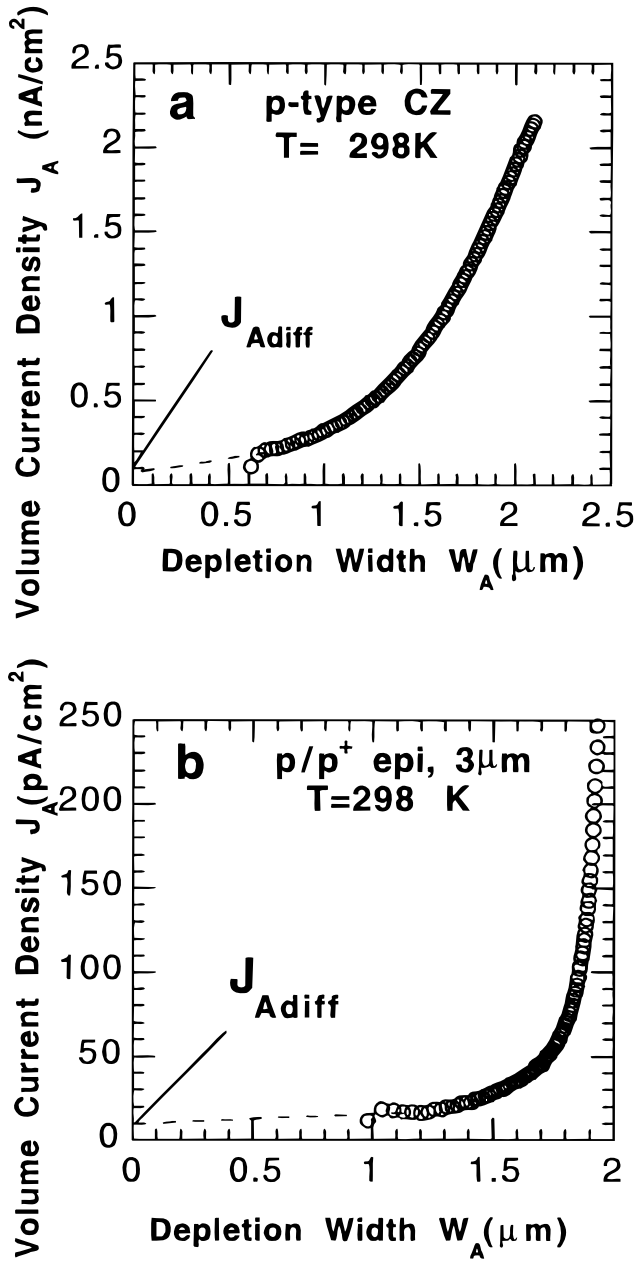

Figure 3. Volume current density vs. volume depletion width for a 10 mm^2 area shallow n^+p junction fabricated on a p-type IG CZ substrate (a) and on a 3 μm p/p^+ epi substrate (b).

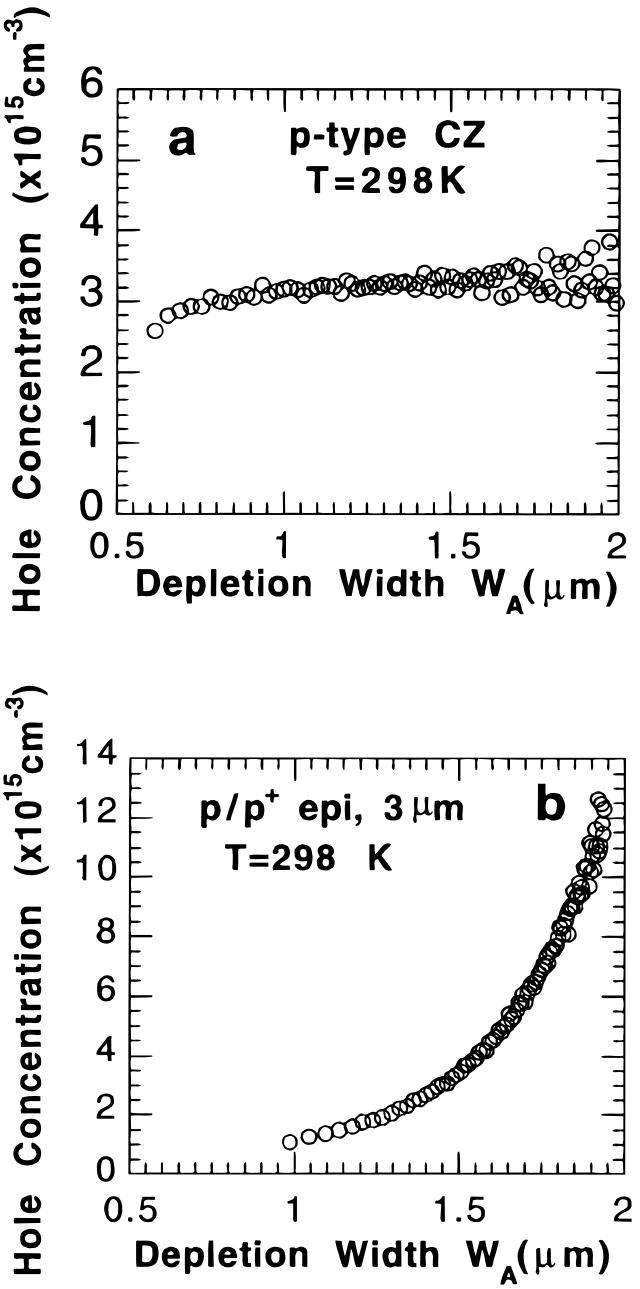

Figure 4. Hole concentration profile of a shallow n^+p junction fabricated on a p-type IG CZ substrate (a) and on a 3 μm p/p^+ epi substrate (b).

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comparing lifetime data determined from different techniques, it is important to check that the parameters have been obtained under similar injection conditions.

The correct determination of the volume depletion width W_A is not only important for the extraction of the diffusion current density, as outlined above, but also for the derivation of the substrate doping density N_A and its profile from a high-frequency C-V plot.[4,5,7] The doping profile can be calculated from

$$N_A(x) = \frac{-C_{vol}^3}{q\epsilon_{si}A^2(dC_{vol}/dV_R)} \quad [4]$$

with q the electron charge in absolute value. However, the capacitance technique probes the distribution of the majority carriers, rather than the distribution of the impurity atoms.[13] This is particularly important for thin epitaxial layers. Hereby is the depth position x below the junction given by the depletion width corresponding to the reverse bias V_R, i.e., $W_A(V_R)$. As shown by Fig. 4a for the p-CZ substrate a quite uniform profile is obtained, with a hole concentration $p = N_A \approx 3 \times 10^{15}$ cm^{-3}, while the corresponding junction is approximately abrupt. For the diode in epitaxial material, shown in Fig. 4b, on the other hand, an increasing majority carrier density is observed toward the epitaxial interface, at ≈3 μm below the shallow junction. This points toward a possible in-diffusion of B from the highly doped p$^+$-region in the epitaxial layer during the processing. This case also illustrates the usefulness of the J_A-W_A (or maybe better: J_A-1/C_{vol}) approach; by using the measured and corrected C_{vol}-V_R characteristics, one can derive the correct depletion depth below the junction, without any assumption or a priori knowledge of the doping density and profile or about V_{bi}.

Finally one can remark that the knowledge of the correct depletion width is of general interest, whenever the profile of an electrical property is derived from the reverse *I-V* or *C-V* characteristics. This is, for instance, the case for the generation lifetime profile.[5] Additionally, to calculate the maximum field at the junction F_{max}, needed to derive field-assisted carrier generation, W_A is an essential parameter[4,5] as are also V_{bi} and N_A.

Substrate Generation/Recombination Properties

The analysis presented above has been extensively applied to another set of n$^+$p junction diodes, with a junction depth of 0.5 μm, obtained by a combined As and P ion implantation, fabricated in different substrate types and corresponding to three thermal pretreatments. A two-step high-low (6 h at 1100°C + 8 h at 750°C) IG is compared with a low-temperature nucleation step (nucl) of 8 h at 750°C and with no pretreatment (no) as a reference. For the high oxygen wafers, the full diode processing on nonpretreated wafers results in a denuded zone width (DZW) of 3 μm. For the IG wafers a DZW of 10 μm is obtained, as derived from structural transmission electron microscopy (TEM) studies. Full details of the substrate characteristics and of the diode processing have been reported previously.[14] The outcome of using the improved diode analysis on these diodes is summarized in Fig. 5, showing the different reverse current components as a function of the initial interstitial oxygen concentration [O_i]. The latter is determined by measuring at 300 K the height of the infrared absorption peak at 1107 cm^{-1} using the IOC88 standard calibration with a conversion factor of 3.14 × 10^{17} cm^{-2}.

The following conclusions can be drawn from Fig. 5, on which the FZ and epitaxial material have been given an arbitrary low [O_i] value to enable to plot their data on the same figure.

The volume generation current.—The volume generation current is inversely proportional to the generation lifetime τ_g

$$J_{Agen} = \frac{qn_iW_A}{\tau_g} \quad [5]$$

with n_i the intrinsic carrier concentration, for which the expression (in cm^{-3}) of Sproul and Green is used[15]

$$n_i = 1.640 \times 10^{15}T^{1.706}\exp(-E_g/2kT) \quad [6]$$

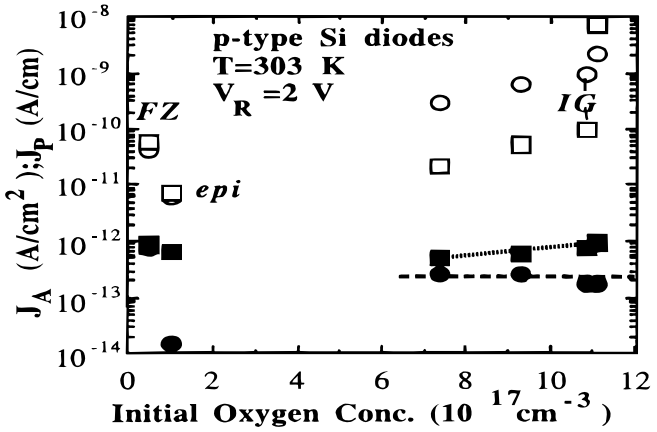

Figure 5. Generation (squares) and diffusion current components (circles) for n$^+$p diodes processed on different starting materials. The filled symbols correspond to the peripheral (lateral) components; the open symbols correspond to the volume components. The broken lines are drawn to guide the eye.

with k the Boltzmann constant and T the absolute temperature. As already noted earlier, for a more accurate determination of the generation lifetime, one has to use the generation width W_G.[10,12] It is seen from Fig. 5 that there is a pronounced dependence of the generation lifetime on [O_i]. The lowest values are observed for the epitaxial wafer (10 μm epitaxial layer here) and for the low-oxygen material. Within the same range of [O_i], the IG diodes have the lowest volume generation current. Based on structural and electrical/ spectroscopic analysis it is concluded that this generation current in p-CZ diodes is due to the presence of oxygen-precipitation induced extended defects in the depletion region.[14] The main results are in line with data reported by other groups.[2,16,17] These defects may be associated with the presence of two electron traps at 0.23 and 0.43 eV below the conduction band, observed as electron traps in the p-substrates by deep level transient spectroscopy (DLTS).[4,14] Note that the current levels for the FZ wafer are still very good, although they are somewhat higher than expected. This might be due to the fact that this wafer is coming from a different batch and/or to the higher sensitivity of these wafers to uncontrolled contamination.

The volume diffusion current.—The same conclusion is derived for the volume diffusion current. In this case (and to a first approximation) it is the recombination lifetime τ_r which shows a clear substrate dependence. This follows from the relationship

$$J_{diff} \approx q\sqrt{\frac{D_n}{\tau_r}}\frac{n_i^2}{N_A} \quad [7]$$

with D_n the electron diffusion coefficient (about 35 cm^2/s at 300 K for the doping concentrations in Fig. 5). The resulting recombination lifetime is represented in Fig. 6, using the doping densities derived from the calculated volume capacitance.[4,5,7] In fact, J_{diff} can also be determined from the intercept of the forward *I-V*, as outlined recently[3] and should theoretically yield similar values.[7] Within the accuracy of the methods this is also found in Fig. 6, which therefore can be considered as a validation of the consistency of the proposed separation procedure.[7] Again, the epitaxial diode yields the best effective recombination lifetime, derived from Eq. 7. The meaning of the effective τ_r is discussed in the next part. It has to be remarked that since the recombination lifetime is determined from *I-V* measurement, by extrapolating the experimental curves to 0 V, the obtained τ_r corresponds with the low injection value.

Since both lifetimes are known, one can calculate their ratio, which in good approximation corresponds to[8]

$$\frac{\tau_g}{\tau_r} = \exp\frac{|E_T - E_i|}{kT} \quad [8]$$

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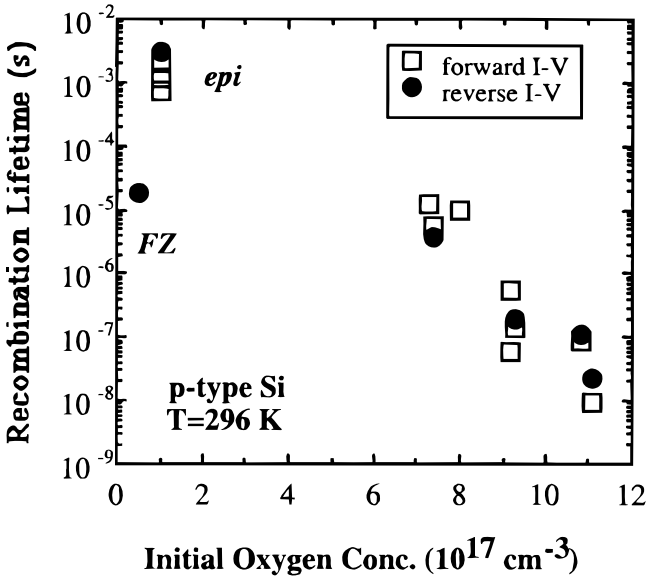

Figure 6. Recombination lifetime as a function of the initial oxygen concentration for p-type Si, derived from the forward current (squares) and from the reverse current (filled circles).

whereby $|E_T\text{-}E_i|$ gives the position of the effective generation/recombination (GR) level E_T with respect to the intrinsic Fermi level E_i. For a system with a single trap, the obtained E_T value corresponds with the real trap position. In the case of multiple trap levels, the calculated E_T value is called an effective trap level, and can be considered as a kind of average value corresponding with the weighted mean of the different traps. Although strictly speaking the Shockley-Read-Hall theory is no longer valid in this case, such an approach is often used. A more rigorous analysis of the problem also has to take into account the difference between the majority and minority carrier cross sections. As shown in Fig. 7 there is a clear contrast between the value typically found for the epi and FZ diodes and for the CZ diodes. A value of ≈0.1 eV has been quoted for "good lifetime" material,[8] which is obviously the case for the epitaxial and FZ substrates reported here. The larger value (>0.2 eV) found for the p-CZ devices first of all indicates that the carrier generation in that material occurs far less efficiently than the recombination processes. Since τ_r is rather insensitive to the exact E_T position, while an exponential τ_g dependence on E_T is expected in the Shockley-Read-Hall framework,[8] this suggests that the active GR centers in the p-CZ material have a position further away from midgap. It is then tempting to assign, for example, the ≈0.3 eV effective level to the E_c-0.23 eV shallow electron trap predominantly observed by DLTS in the IG high oxygen (HO) diodes.[4,14] In this case the effective level coincides with the microscopic trap level. The value of this electron trap, observed under minority carrier injection conditions, closely matches the activation energy of 0.87 eV, derived from an Arrhenius plot of the reverse current for not too large reverse biases.[4,16,17]

For the nongettered HO-Cz substrate, a lower value of ≈0.22 eV is found, placing the effective GR level closer to midgap. Consequently, it is expected that the deeper electron trap at E_c-0.43 eV also plays a role in the electrical activity of the oxygen-precipitation induced extended defects. In that case, the effective level is to be considered as a weighed mean between the two active GR centers present in the nongettered material. From an Arrhenius plot, an activation energy of ≈0.63 eV is derived for the HO-no diodes,[4] emphasizing the dominant role of the deeper level in the generation process. This is in line with previous reports for nongettered CZ material.[16,17] The recombination activity, on the other hand, will be dominated by the shallow(er) level at E_c-0.23 eV, as confirmed by the temperature dependence observed by using other more sophisticated lifetime techniques.[18]

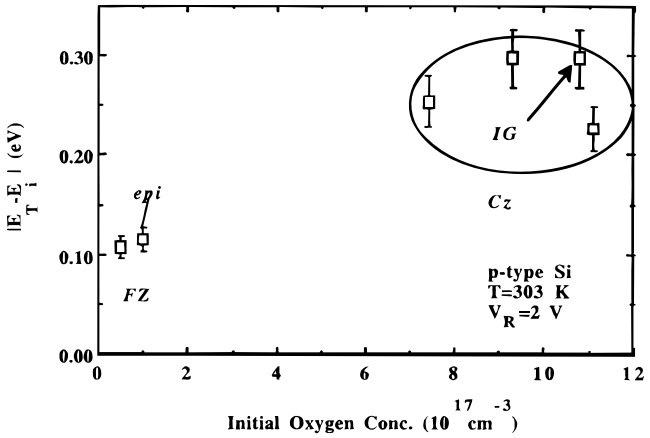

Figure 7. The effective GR level as a function of the initial oxygen concentration, for a number of p-type Si substrates.

The peripheral generation current.—The peripheral generation current density in Fig. 5 shows a subtle substrate dependence, which only has been revealed by the present separation procedure. As remarked above, the peripheral generation current originates from both the surface generation, through the interface states in the bird's-beak region of the LOCOS isolation and from the bulk generation in the lateral depletion region. A substrate dependence could point to an effect of the latter component. However, one can roughly estimate the lateral depletion generation per perimeter length unit by J_A times d_j, [9] with d_j the depth of the junction, i.e., 0.5 μm for the diodes corresponding to Fig. 5. It turns out that the corresponding peripheral density is in the range ≈0.1 pA/cm, which is at most 10% of the measured value (the case of HO-no). This suggests that the peripheral generation current is caused mainly by surface generation. Further evidence is provided by gated diode measurements, which show a close to linear correlation between the measured J_{Pgen} and the measured surface generation below the bird's-beak region of the field oxide, using a different approach than what is classically applied.[4,19] In addition, Arrhenius measurements reveal an activation energy in the range of ≈0.7 eV, which is close to the values reported for generation through interface states.[20,21] One can finally remark that the values for J_p found here in the range 1 pA/cm, indicate low residual stress levels at the LOCOS interface.[22] In more advanced isolation schemes, higher stress levels and J_ps are observed, which could rise up to about 10 pA/cm. [6,22] Above that, the stress is high enough to relax through the formation of dislocations at the edges of the device.[22] Efforts are currently underway to further improve on the separation procedure for a more accurate determination of the lateral component.

The peripheral diffusion current.—The peripheral diffusion current density in Fig. 5 is relatively constant for the CZ substrates, which is in line with what could be expected from a lateral current flow in a near-surface defect-lean zone (DLZ). Irrespective of the pretreatment, oxygen out-diffusion of the near-surface layer will inevitably take place during the diode processing, resulting in the formation of a defect-lean zone. A DLZ of 3 μm has been found from TEM observations in the HO-no diodes.[14] Interestingly, the epitaxial diodes show the lowest peripheral diffusion current as well, although no physical explanation exists for the moment. Arrhenius plots of the lateral diffusion component show an activation energy close to the expected theoretical value of 1.12 eV at 300 K. This supports the validity of the extraction procedure.[7]

Summary.—Summarizing, the best overall leakage current behavior is observed for the diodes fabricated on the epitaxial wafers. Furthermore, for good quality diodes, the volume diffusion current is larger than the volume generation current. This is already observed at or slightly above room temperature. The opposite is true for the peripheral component, which is dominated by the surface generation in the bird's-beak region. Although there is still a substrate effect, it

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will be determined mainly by other, processing (stress) related factors. This means in practice that for the downscaled source-drain diodes, this factor will be of extreme importance.[6,9]

Discussion: The Diffusion Current in Epitaxial and IG Cz Wafers

In Fig. 5, some other interesting observations can be made with respect to the volume diffusion current density. Since the early eighties, it has been pointed out that at higher operation temperatures, as typical, e.g., for DRAM circuits, the diffusion current will be the main source of leakage and therefore will determine the retention and refresh times.[23,24] By using epitaxial substrates, this component can be drastically reduced, as also evidenced by Fig. 5. Compared with the FZ and CZ substrates, a reduction by one or two decades can be obtained. This can be quantitatively explained as follows. For epitaxial wafers, Eq. 7 has to be modified in order to take into account the presence of a highly doped substrate underneath the epitaxial layer. According to Murakami and Shinyouji[2] the diffusion current density for zero bias is in a first approximation modeled by

$$J_{diff} = q\sqrt{\frac{D_n}{\tau_r}}\frac{n_i^2}{N_A}F \qquad [9a]$$

with

$$F = \frac{(1+\Phi)\exp(\beta) + (1-\Phi)\exp(-\beta)}{(1+\Phi)\exp(\beta) - (1-\Phi)\exp(-\beta)} \qquad [9b]$$

whereby $\beta = D/L_n$ and $\Phi = \exp(q\phi/kT) \approx N_A/N_A'$ with N_A' the substrate doping. Furthermore, ϕ is the Fermi potential difference between the highly doped substrate and the epitaxial layer, in the absence of an external electric field. L_n is the minority carrier diffusion length ($=\sqrt{D_n\tau_r}$) in the epi layer and D the distance between the edge of the depletion region and the epi interface, i.e. equal to the epi layer thickness (e.g., 10 μm in Fig. 8) minus $d_j + W_A(V_R)$. Equation 9 is a simplified model, valid if the difference in lifetime and mobility between the epitaxial layer and the substrate can be neglected and in the absence of recombination at the p-p$^+$ interface.[2] However, a good qualitative picture of what could be expected is obtained. In essence, the reduction of J_{diff} for an epitaxial wafer is due to the presence of the highly doped region with N_A'. A more detailed study of the experimental determination of the recombination and generation lifetime in expitaxial substrates has recently been presented by the authors,[26] discussing a graphical technique to determine the correction factor F. For a high potential difference or a high doping density ratio ($\Phi >> 1$) F simplifies to

$$F \approx \tanh(\beta) = \tanh\left(\frac{D}{L_n}\right) \qquad [10]$$

In the limiting case that the recombination lifetime becomes very small so that $D >> L_n$, $F \approx 1$, and the effect of having a highly doped substrate is lost. The diffusion current then approaches the value of a bulk wafer. Also in the case of a thick epitaxial layer $D >> L_n$ and $F \approx 1$.

Calculations based on Eq. 9 allow one to get insight into some parameters of direct importance for process development of submicron CMOS technologies. As shown in Fig. 8, for epitaxial substrates F is mostly smaller than 1. This implies that calculations based on Eq. 7 are overestimating the recombination lifetime. A more correct analysis yields a τ_r in the range of 5-10 μs, [26] which is in good agreement with the value obtained by using a cross-sectional optical measurement technique.[27]

Figure 8 clearly illustrates the impact of the epitaxial layer thickness and doping and of the supply voltage on the correction factor. This figure is calculated by using $N_A' = 10^{19}$ cm^{-3}, $L_n = 100$ μm, and $D_n = 30$ cm^2/s. Although more exact L_n and D_n values are required for a qualitative determination of the correction factor, the general trends reflected in Fig. 8 remain unchanged. An increase of F is found when the supply voltage (depletion width) is reduced, while keeping the same epi thickness. This could be an argument in favor of reducing the epi layer thickness for future generations of technologies for which one wants to reduce the supply voltage without penalizing the F factor. In principle, a very low F factor can be achieved there, as evidenced by Fig. 8, particularly if full depletion is reached, i.e., when D is approaching zero. Of course, one should then take into account other factors, neglected so far in this analysis (the generation in the substrate, the activity of the interface, the inhomogeneous doping density...).

The same improvement is obtained for a thick epitaxial layer with a lower doping concentration, although the "autodoping effect" (see Fig. 4) should become more pronounced in that case and maybe prevents the occurrence of full depletion of the epi layer. The above considerations imply that the diffusion current for epi diodes is bias dependent, especially for thin layers. It is believed that in such a case, the extraction of J_{diff} from I_R measurements should be carefully re-examined and, if needed, be fine tuned. On the other hand, the forward extraction procedure in first instance remains unaffected as it is based on the extrapolation of I_F to 0 V.

The fact that for the standard approach based on Eq. 7 the calculated recombination lifetime is overestimated also has its consequences for the calculation of the effective trap level by using Eq. 8. If the recombination lifetime is reduced, the trap level will shift toward higher values. No correction has been performed for the epi diode in Fig. 7, so that the difference between epitaxial and CZ material becomes somewhat smaller.

In the case of an internally gettered substrate, the introduction of a correction factor for the diffusion current has an opposite effect.[2,23-25] There an enhancement is expected due to the minority carrier generation in the quasi-neutral highly defective bulk region, having the same doping density. In first order, the diffusion current density is given by Eq. 9a,[2] but now with

$$F = \frac{(1+\alpha)\exp(\beta) + (1-\alpha)\exp(-\beta)}{(1+\alpha)\exp(\beta) - (1-\alpha)\exp(-\beta)} \qquad [11a]$$

whereby

$$\alpha = \frac{L_n' D_n}{L_n D_n'} \qquad [11b]$$

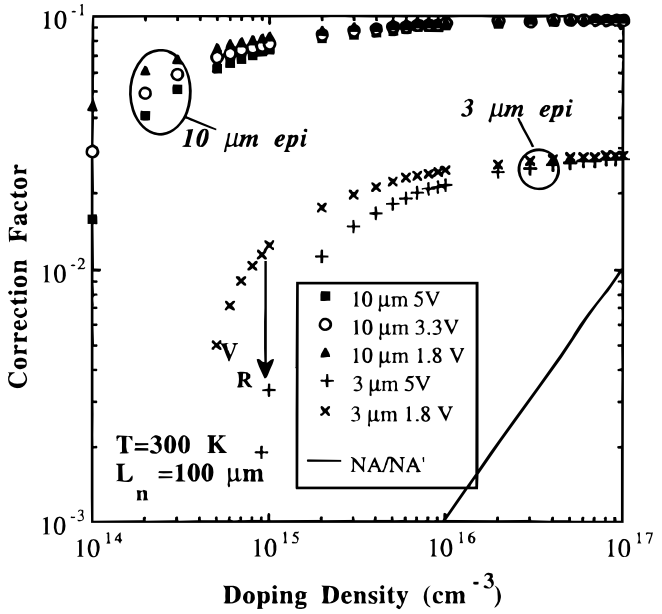

Figure 8. Calculated correction factor, given by Eq. 9b, for the diffusion current in an epitaxial wafer, with substrate doping density of 10^{19} cm^{-3} and corresponding with different epi layer thickness and reverse diode bias. For the calculations $L_n = 100$ μm and $D_n = 30$ cm^2/s have been used.

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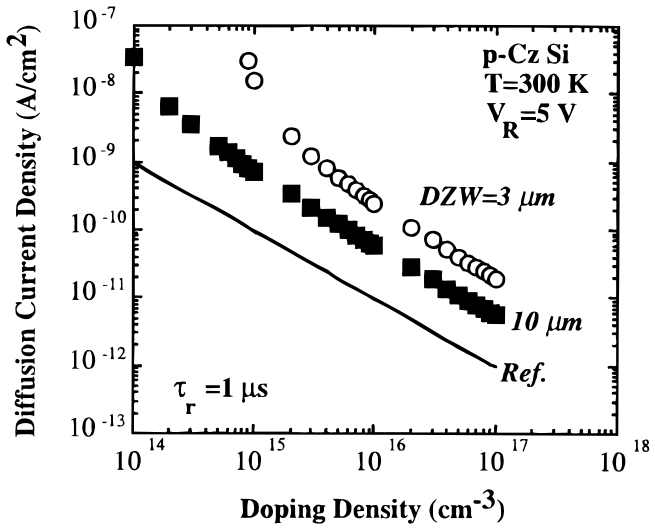

Figure 9. Diffusion current density vs. doping concentration for IG CZ diodes, having a DZW of 3 and 10 μm, respectively. The reverse bias is 5 V and the recombination lifetime 1 μs. The solid line is the limit for the homogeneous p-type substrate.

with L_n' and D_n' the value of the diffusion length and the electron diffusion coefficient in the defect-rich region where the gettering is taking place. For IG wafers, D is equal to the denuded zone width (DZW) minus $[d_j + W_A(V_R)]$. In the case that the defect region has a very low diffusion length (i.e., $L_n' << L_n$ or $\alpha \approx 0$) and that $D << L_n$, Eq. 11a further simplifies to

$$F = \coth\left(\frac{D}{L_n}\right) \approx \frac{L_n}{D} \qquad [12]$$

The J_{diff} values shown in Fig. 9 correspond to a τ_r of 1 μs and a V_R of 5 V. The increase of F with lower doping density occurs because D becomes much smaller than L_n. In other words, when the depletion width penetrates the defective bulk region. In that case, also the generation current increases.[14] Physically this means that, for small denuded zone and/or large depletion widths, the generated minority carriers in the defective bulk will be collected with high efficiency by the reverse biased diode. In the limit of higher doping densities, a ratio of about three between J_{diff} values for the 3 and the 10 μm DZW cases can be observed in Fig. 9, and the same ratio seen in Fig. 5 was found experimentally.[4] The same remark applies here, i.e., one should treat the calculated recombination lifetimes of Fig. 6 with some care, given this correction factor F. Generally, for IG CZ diodes a too low value will be found, while for epitaxial ones the opposite holds, if Eq. 7 is used to calculate τ_r. In the case of internally gettered substrates, it becomes rather difficult to use a graphical technique to determine the diffusion length and recombination lifetime. In that case the extracted diffusion current density yields information on the electrical denuded zone width.[28]

Conclusions

Optimizing the analysis of the diode *I-V* and *C-V* characteristics yields more information about the impact of the substrate on the generation/recombination properties, which can hardly be traced with the same accuracy by other "electrical" techniques. The proposed method is very consistent. However, a few problem areas remain, in particular for substrates with inhomogeneous recombination lifetime parameters, like epitaxial and IG wafers, which require a dedicated approach.

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