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Impact of threshold voltage extraction methods on semiconductor device variability

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ABSTRACT

This paper presents a study of the impact that several widely used threshold voltage (V_T) extraction methods have on semiconductor device variability studies. The second derivative (SD), linear extrapolation (LE) and third derivative (TD) extraction techniques have been compared to the standard method used in variability, the constant current criteria (CC). To estimate the influence of these methods on the results, an ensemble of 10.7 nm gate length Si FinFETs affected by RD variability have been simulated. We have shown that variability estimators like the σV_T, $\langle V_T \rangle$ and the V_T shift, are heavily affected by the selected extraction methodology, with up to 30% differences in the standard deviation. We have demonstrated that being aware of which V_T extraction technique has been used in a variability analysis is crucial to properly interpret the results as they may be heavily method-dependent.

1. Introduction

Threshold voltage is one of the key parameters of a transistor's operation [1]. Therefore, it is crucial to obtain a precise and accurate V_T value to correctly characterize a device performance.

Across previously published work many methodologies to obtain V_T appear, from the traditional band-bending condition [2] to other vastly used techniques like the second derivative method (SD) [1], constant current criteria (CC) [3], linear extrapolation (LE) [4] and third derivative (TD) [1], that have been applied to different devices, such as MOSFETs [1], non-crystalline TFETs [5] or junctionless transistors [6].

Multigate devices are the preferred architecture beyond the 32 nm technology node [7,8] because of their superior gate control in comparison with the conventional MOSFET [8]. However, non-planar FETs also suffer from fabrication defects [3] and operation degradation [9] due to variability issues, which become serious limiting factors as the devices are continued to be scaled down. Sources of statistical variability, such as random dopants (RD) [10], line-edge roughness (LER) [11] and metal grain granularity (MGG) [3] can play an immense role in device performance as they are one of the main factors constraining supply voltage, causing power dissipation [3]. Therefore, detailed investigation on these devices' operation and variability effects is crucial to aid both industry and academia to overcome these challenges.

Generally, when performing variability studies, the parameters that characterize the V_T statistical distribution (e.g. standard deviation, mean value) are used as the main criteria to assess the impact of a variability source on the device's performance in the sub-threshold region [3]. However, a question that may arise is how independent the statistical results are from the selected V_T extraction method. For this reason, in this work we present a complete comparison of four commonly used extraction techniques (SD, CC, LE and TD), with the aim of establishing the impact that V_T extraction methods have on statistical variability studies. These extraction techniques have been implemented in our simulation toolbox, compared in terms of computational cost and robustness and, tested, by applying them to a RD affected state-of-the-art 10.7 nm gate length Si FinFET that has been scaled down from an experimental device [12].

The paper is structured as follows: Section 2 contains a thorough scheme of the simulated device, dimensions and models used. Section 3 explains the different implemented V_T extraction methods.In Section 4 the gate voltage discretization step and its effect on the figure of merit (FoM) obtained values is studied. Next, a comparative study between the extraction methods and its effect on variability is discussed and finally, in Section 5 a complete overview of the results will be presented.

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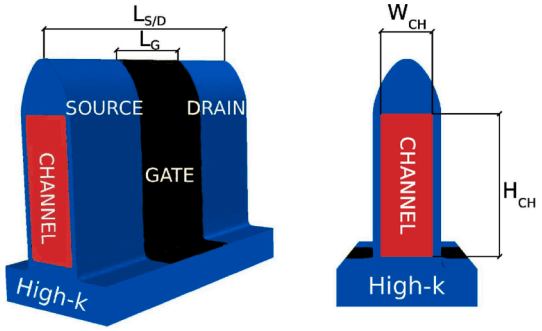

Fig. 1. Schematics of the 10.7 nm gate length Si FinFET with a rectangular shape channel [3].

2. Device characterization and simulator description

The device architecture studied in this work is a 10.7 nm gate length Si FinFET (see schematics in Fig. 1). This is a state-of-the-art device characterized from experimental data [13,14] and later scaled following the ITRS guidelines [15]. The device dimensions are, 10.7 nm gate length (L_G), 10.7 nm source and drain lengths ($L_{S/D}$), 5.8 nm channel width (W_{CH}), 15 nm channel height (H_{CH}) and 0.62 effective oxide thickness (EOT). Other important modeling parameters are the carrier concentrations in the different regions: a p-type uniformly doped to 1×10^{15} cm^{-3} channel and a n-type Gaussian doping in the source/drain, with a peak value of 1×10^{20} cm^{-3} and a lateral straggle $\sigma = 3.45$ nm. The effective perimeter of the channel is 35.8 nm.

This device has been studied using our 3D in–house built, finite element, quantum corrected (density gradient), drift diffusion (DD) simulator [16]. Several fitting parameters have been adjusted in order to obtain the DD curves used in the work, and this has been done through a meticulous calibration against simulation data from Non-Equilibrium Green's Function (NEGF) [17], in the subthreshold region, and quantum corrected Monte Carlo (MC) [18], in the on-region, as shown in Fig. 2. Some of the main fitting parameters are, the saturation velocity (v_{sat}), coming from the Caughney and Tomas model [19], and the perpendicular critical electric field (E_{CN}) [20] that mimic the behavior of the curve in the on-region. Also for the subthreshold region the DG electron mass in the transport (m_x) and perpendicular directions (m_y, m_z) are calibrated to emulate source-to-drain tunneling and quantum confinement effects as seen in [11] and a perfect match has been achieved for the subthreshold and threshold regions. Note that all IV curves shown in this work are normalized by the channel effective perimeter, resulting in current per unit of length and have been simulated at a low drain bias of 50 mV.

3. Threshold voltage extraction methodologies

In this section, we present four popular extraction methodologies found in the literature, a straightforward constant current, a geometrical linear extrapolation and two transconductance-based methods

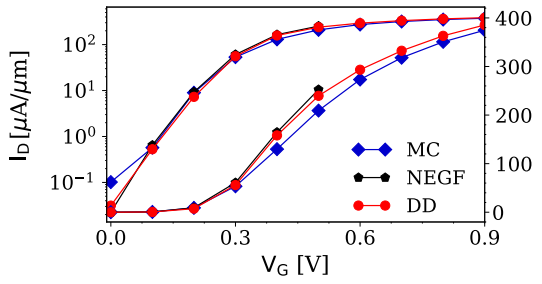

Fig. 2. DD simulated transfer characteristics for the 10.7 nm gate length Si FinFET calibrated against both MC and NEGF simulations at $V_{D,lin} = 0.05$ V.

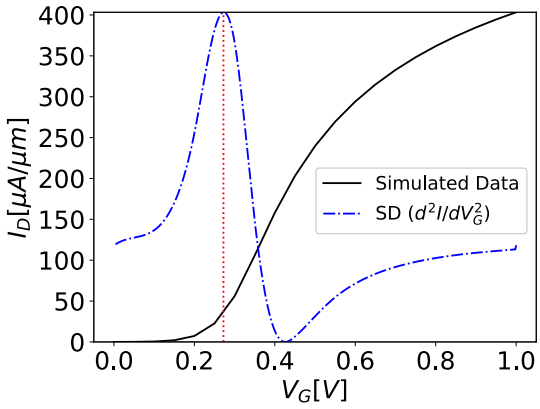

Fig. 3. Second derivative (SD) method implementation (blue dashed line) for the FinFET device. The red dotted line indicates the position of V_T. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

like the second and third derivatives.

3.1. Second derivative (SD)

The second derivative method, also called transconductance change method, is one of the most popular used methods [4]. It evaluates V_T at the V_G value where the derivative of the transconductance ($g_m = dI_D/dV_G$) is maximum. In Fig. 3, the IV curve for the device is plotted along with the V_T extracted value where the red dotted line crosses the x-axis and the second derivative curve with the blue dashed line. A drawback of this method is its sensitivity to noise and error, as it acts as a high pass filter on the measured data [1]. One way of solving it, is to apply smoothing techniques or numerical fitting [1].

3.2. Constant current (CC)

Traditionally the constant current method has been the preferred technique used to obtain the threshold voltage value in variability studies [1,3,21] due to its simplicity and speed. This method determines V_T at a critical user-defined value of the drain current (I_{Dcc}) where the transition point from linear to saturation regime happens [4]. A general criteria is to consider $I_{Dcc} = W_{eff}/L_G \times I_0$, being $W_{eff} = 2 \times H_{CH} + W_{CH}$ the effective perimeter of the Si channel [22], and I_0 a constant current level [23] defined by the user depending on the studied device. A graphical depiction of this method can be seen in Fig. 4.

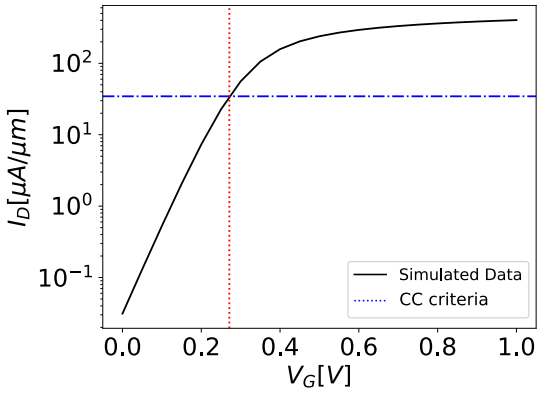

Fig. 4. Constant current (CC) criteria applied to the FinFET device with a value of $I_{Dcc} = 34.6$ μA/μm (blue dashed line). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

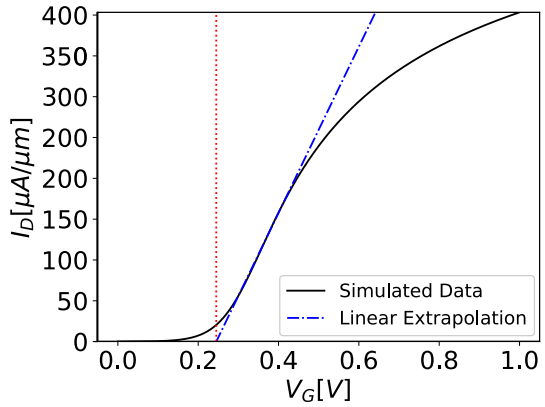

Fig. 5. Linear Extrapolation (LE) method showing the extrapolated line (blue dashed line) intersecting with the x-axis at V_T (red dotted line). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3.3. Linear extrapolation (LE)

The linear extrapolation method is another widely used technique based on the quadratic law [4]. Ortiz et al. state that, using this method V_T is obtained as the gate voltage axis intercept of the tangent of the IV characteristics at its maximum first derivative (slope) point [1] (see Fig. 5).

3.4. Third derivative (TD)

The third derivative method consists on choosing the V_T where the third derivative of the current (d^3I_D/dV_G^3) has a maximum (see Fig. 6). This extraction method disagrees with the SD method inherently as the values extracted from the maximums and minimums of the function always fall to the sides of the ones obtained with the SD method. Beside this, successive differentiation amplifies the noise, hence increasing the instability, making it less reliable. To reduce this induced error fitting and smoothing techniques can be applied.

4. Impact of the threshold voltage extraction method on variability studies

The previously described V_T extraction methods are dependent on the gate voltage step size used to obtain the IV curve. Initially, using a fine step of 1 mV as reference, we have compared the V_T values calculated for several coarser step sizes in order to assess the trade-off

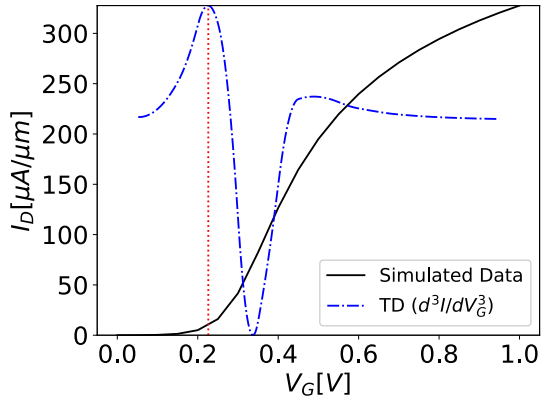

Fig. 6. Third derivative (TD) method (blue dashed line) plot showing the extracted V_T at the V_G point where the third derivative is maximum (red dotted line). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
Threshold voltage V_T[V] results for the simulated Si FinFET at V_D = 0.05 V for the different gate voltage step sizes [V]. These values have been extracted for the various implemented methods and the IV simulation time for each step size is indicated.

Step Size [V]	SD [V]	CC [V]	LE [V]	TD [V]	Time [hours]
0.001	0.273	0.272	0.244	0.219	48
0.005	0.273	0.272	0.244	0.222	13
0.01	0.273	0.272	0.244	0.222	6
0.05	0.273	0.272	0.244	0.218	2
0.07	0.281	0.271	0.248	0.216	1.3

between the computational expense and the threshold voltage accuracy. Table 1 shows the total simulation time and the yielded V_T values as a function of the gate bias step size and the extraction method. It is evident that the computational cost increases when the gate voltage step size decreases. As shown in this table, in the SD, CC and LE methods, when using a step size of up to 0.05 V there is no loss of accuracy in the V_T value, while allowing us to reduce the simulation time 24 times. When the step size is further increased to 0.07 V, only the CC method is able to maintain an acceptable extraction value. Note that, the TD method is clearly unstable as soon as the step size is increased from 1 mV (as previously explained in subSection 3.4).

Next, a complete study to estimate the influence that the V_T extraction method has on variability results is performed. A set of 300 devices affected by discrete RDs have been simulated for the 10.7 gate length FinFET. The n-type dopants were generated using a rejection technique from the continuous doping distribution and spread in the S/D regions via an atomistic grid defined by the positions of the atoms [24]. A graphical representation of a randomly chosen RD profile can be seen in Fig. 7, displaying the electron concentration in a cross sectional view of the channel in the transport direction.

Two figures of merit (FoM) that characterize the RD induced variability, V_T and I_{ON}, are analyzed to compare the influence of the extraction methods on the results. Note that I_{ON} is also extraction-dependent, as it has been defined as the current at $V_T + V_{D,sat}$, being $V_{D,sat}$ = 0.70 V. For each FoM the following parameters have been analyzed: the ideal case where the device has a continuous doping distribution in the S/D regions (FoM_{ideal}), and the distribution mean

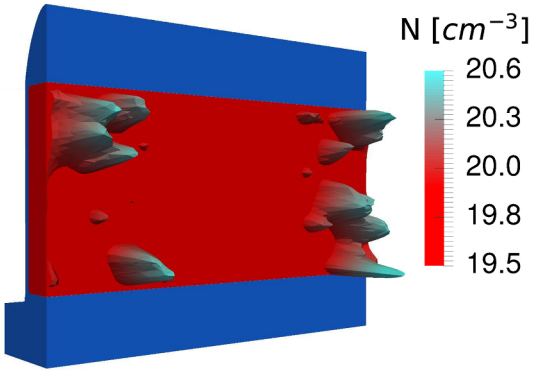

Fig. 7. 3D cross sectional view of the 10.7 nm gate length Si FinFET affected by random dopant fluctuations showing the electron concentration throughout the channel of the device.

Table 2
V_T and I_{ON} results extracted from the simulated IV curves affected by RD variability indicating: the ideal uniformly doped device (FoM_{ideal}), the distribution mean value ($\langle FoM \rangle$), standard deviation (σFoM), FoM shift (ΔFoM = FoMideal − $\langle FoM \rangle$), skewness (γ(FoM)) and kurtosis (κ(FoM)). These results have been extracted with the four implemented methods at a gate voltage step size of 0.01 V and V_D = 0.05 V.

Method	$V_{T,ideal}$ [V]	σV_T [mV]	$\langle V_T \rangle$ [V]	ΔV_T [V]	$\gamma(V_T)$	$\kappa(V_T)$	$I_{ON,ideal}$ [μA/μm]	σI_{ON} [μA/μm]	$\langle I_{ON} \rangle$ [μA/μm]	ΔI_{ON} [μA/μm]	$\gamma(I_{ON})$	$\kappa(I_{ON})$
SD	0.273	10.7	0.277	− 0.004	− 0.91	− 1.97	399	29.5	339	60	0.144	− 2.95
CC	0.272	13.6	0.285	− 0.013	− 0.36	− 2.54	398	28.7	340	58	0.143	− 2.96
LE	0.244	10.7	0.248	− 0.004	− 0.80	− 2.13	393	29.1	335	58	0.147	− 2.94
TD	0.218	10.9	0.226	− 0.008	− 1.01	− 1.76	388	28.9	331	57	0.144	− 2.94

value ($\langle FoM \rangle$), standard deviation (σFoM), skewness (γ(FoM)) and kurtosis (κ(FoM)).

Before analyzing the variability results, we want to test the robustness of the different methods when extracting an ensemble of V_T and I_{ON} values. For that, we have compared the standard deviations and mean values of the distributions obtained from several sets of simulations performed with different gate voltages step sizes (ranging from 0.01 V to 0.05 V). The gate voltage intervals do not affect either σI_{ON} or the mean values of V_T and I_{ON} for the 4 analyzed extracted methods. However, when the step size is increased from 0.01 V to 0.05 V there is a slight change (around 5%) in σV_T for the SD and TD methods, whereas the CC and LE methods remain unaffected.

For the above mentioned reason, in Table 2 we only present the different extracted parameters for a 0.01 V simulation step size. Results show that the difference in σV_T as a function of the extraction method can be up to 3.2 mV, which amounts to a dramatical 30% increase in the variability. The largest σV_T variability is observed for the CC method.

Another meaningful parameter that can be extracted from the statistical distribution is the RD induced threshold voltage shift, $\Delta V_T = V_{T,ideal} - \langle V_T \rangle [V]$, that is also dependent on the extraction method utilized (see values in Table 2). ΔV_T ranges between − 13 mV for the CC method (a value as large as σV_T) and − 4 mV for the LE. Note that, if instead of CC or TD, the selected method is LE or SD, the voltage shift would be unnoticed, changing the interpretation of the variability results. In case of σI_{ON}, the obtained values are very close, with differences lower than 1μA/μm (less than 3% of the total variability in the on-region) between the extraction methods. ΔI_{ON} values are also similar among the four extraction methods (around 58μA/μm). Note that for FinFET devices, ΔI_{ON} and ΔV_T have opposite signs. For I_{ON}, the extracted results are practically independent of the method and the same conclusions will be drawn in variability studies, unlike what we have previously shown for V_T.

Fig. 8 (top) shows the scatter plots of the threshold voltage extracted with the implemented techniques versus the values for the SD method (V_T SD). The correlation coefficient (R) is also included for comparison. The same study has been done for I_{ON} in Fig. 8 (bottom). Note that, the V_T values between SD, LE and TD extraction methods are highly correlated, whereas that is not the case for the CC technique. This is due to the fact that the CC method is based on a fixed current criterion, whereas the remaining techniques try to capture the change in the curvature of the IV characteristics. With regards to the I_{ON}, all extraction methods are highly correlated due to the behaviour of the IV curves in the on-region, reinforcing the sense of independence of this FoM with the applied extraction method. To better understand these different correlation values, Fig. 9 shows for the simulated IV curves the V_T and I_{ON} extracted values. It can be clearly seen in this figure how the different extraction techniques follow different distributions on the IV curves. V_T excursion is happening in a part of the curve where the behaviour is exponential (subthreshold region) whereas I_{ON} changes are quadratic (saturation).

Fig. 10 shows an example of three IV curves that have the same V_T value when using the CC criteria. Note that these curves have significantly different I_{ON}, I_{OFF} and sub-threshold slope values. This is a inherent property of a method based on a arbitrary criteria fixed by the user, which can be problematic when dealing with sources of variability with a greater excursion like MGG [3].

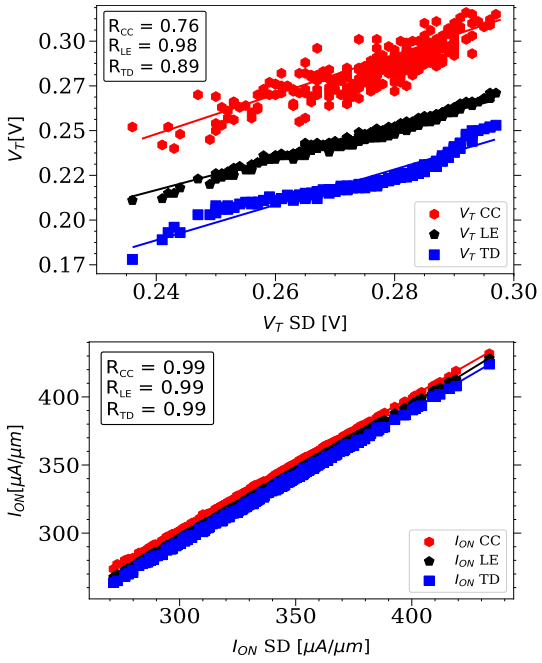

Fig. 8. (Top) Correlation between the different V_T extraction methods. This correlation is measured through the correlation coefficient (R) for each method against V_T SD. (Bottom) Correlation between the different obtained I_{ON} results with each extraction method. This correlation is measured through the correlation coefficient (R) for each method against I_{ON} SD.

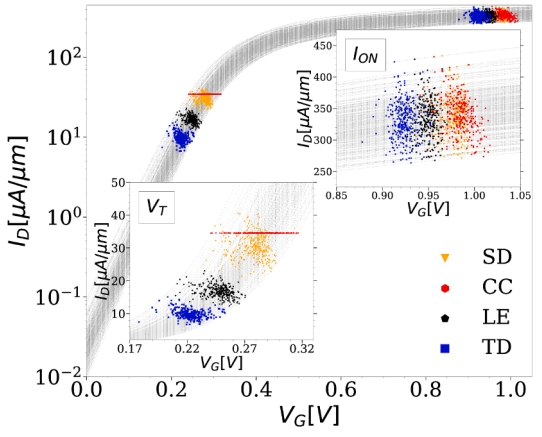

Fig. 9. Ensemble of 300 simulated IV curves affected by different RD fluctuations, and the extracted values for both V_T and I_{ON}. The four implemented extraction methodologies are applied to the curves resulting in the different displayed V_T values.

Another characteristic parameter that has been studied is the

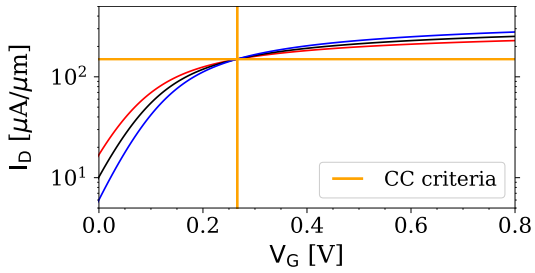

Fig. 10. Example of several simulated IV curves affected by RD variability with exactly the same V_T obtained using the CC method. The curves are represented in logarithmic scale and the blue lines represent the CC criteria.

skewness (γ) of the distribution which provides a measure of its symmetry. In our case, all the skewness values are negative for V_T (see Table 1), meaning that the left tails of these distributions are longer, showing a noticeable asymmetry, particularly in the distributions from the SD, LE and TD methods. On the other hand, the I_{ON} distributions are right-skewed and their γ values are very close for the four analyzed extraction methods.

We have also calculated the excess kurtosis (κ) that accounts for how heavy or light-tailed a distribution is when compared to a normal distribution ($\kappa = 0$). From Table 2, both in case of V_T and I_{ON} all κ values are negative, indicating that the distributions are heavily-tailed. For V_T, the κ values are dispersed for the different extraction methods, the TD method is the one whose tails resemble the most to those of a normal Gaussian distribution. In the I_{ON}, the κ values are close to -3 in all studied cases.

The results presented in this section have proved that the V_T extraction method may seriously impact, not only the obtained V_T values, but also the conclusions achieved in variability studies. For this reason, the V_T extraction method presents itself as an additional parameter that needs to be considered when comparing variability studies for semiconductor device simulation.

5. Conclusions

In this work we investigated the impact of the threshold voltage extraction methods on semiconductor device variability studies. In order to do so, four commonly used methods have been analyzed: second derivative (SD), constant current criteria (CC), linear extrapolation (LE) and third derivative (TD). Also these methods were compared in terms of computational cost and robustness.

As a proof of concept we have tested the influence of these V_T extraction methods on 10.7 nm gate length Si FinFETs affected by RD variability. We have shown that the TD method is more sensitive than its counterparts to the value of the voltage step size, leading to inconsistencies in the extracted V_T values.

Reliability estimators like σV_T, $\langle V_T \rangle$ and ΔV_T become affected by the selected extraction methodology, with up to a 30% difference in the standard deviation. The difference in ΔV_T among the methods can be quite dramatic, with a -13 mV shift for the CC method (a value as large as σV_T) and of only -4 mV for LE. For I_{ON} a completely different tendency has been observed as all the implemented methods yield almost the same results, with less than a 3% difference in σI_{ON} and a constant ΔI_{ON}.

While SD, LE and TD methods produce highly correlated V_T values, the CC method can produce inconsistent results as it may fail to capture changes in the slope introduced by variability effects. As a final study, a complete analysis on the FoM distributions has been performed, comparing their symmetry and tails for all the implemented extraction methods. It has been demonstrated that these distribution properties are also highly dependent on the extraction methods for V_T, while for I_{ON} the values are almost identical.

Finally, even though we cannot clearly establish which method is the most physically accurate, we have proved that to properly compare variability studies it is critical to employ the same extraction method as the calculated results are heavily influenced by the extraction methodology.

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