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IOP Publishing Journal Title
J. Phys. D: Appl. Phys https://doi.org/XXXX/XXXX

Silicon Acoustoelectronics with thin film Lithium Niobate

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Abstract

We report on acoustoelectric (AE) interaction in heterogeneously integrated thin-film Lithium Niobate on standard resistivity and high resistivity Silicon substrate (LNOS). The monolithic LNOS platform delivers acoustic waves with a large electromechanical coupling coefficient (K^2) and draws on standard MOSFET techniques to maximise AE interaction by impedance matching the acoustic wave with the semiconductor carriers. Preliminary results are obtained on AE attenuation (4 dB/cm) and AE gain (6 dB/cm). With further improvement of the LN/Si interface, the LNOS platform can be expected to give rise to an era of non-reciprocal silicon acoustoelectronics.

Keywords: Acoustoelectric, acoustic wave, piezoelectric/semiconductor

1. Introduction

The electric potential of an acoustic wave (AW) travelling at a piezoelectric/semiconductor interface induces a periodic modulation in the energy band levels of the semiconductor. Charge redistribution in response to these evanescent piezoelectric fields confines electrons to the minima, and holes to the maxima, of the AW potential [1]. This interaction, termed the acoustoelectric effect (AE) [2][3][4][5][6][7][8][9][10][11], results in an acoustically driven current [12] and attenuation of the AW. The direction of momentum transfer can also be reversed and amplification of the AW achieved by applying an electric field to make the carriers confined in the AW minima drift faster than the acoustic wave velocity. The result is non-reciprocal wave propagation or selective amplification/attenuation of acoustic waves depending on whether the waves propogate in/against the direction of the electric field. AE amplification is thus highly sought-after to recover propagation loss in acoustic transmission lines and to design fundamentally non reciprocal circuits. Furthermore, designing AE devices with silicon provides a route to integrating high-gain analog amplifiers and signal processing devices [13] with IC technology.

AE effect is at its strongest when a 2D semiconducting layer with high mobility and low carrier density is placed in close proximity with a high K^2 acoustic wave [14][15][16][17]. Fundamental investigations on AE have focused on Surface Acoustic Waves (SAW, or Rayleigh waves) in the GaAs/AlGaAs heterostructure due to the intrinsic piezoelectricity of GaAs and the high quality of the modulation doping induced 2DEG [18],[19]. Electrostatically constricting the GaAs/AlGaAs 2DEG along the acoustic beam width results in quantization of the number of electrons transported in each SAW minimum [20]. It has been shown that AWs can shuttle a continuous stream of single electrons, confined and isolated from each other as individual quantum dots [19]. These "dynamic quantum dots" have been routed for widespread applications as single photon sources, and more importantly as a quantum bus for manipulation of spin-qubits [21]. Recently, complentary metal oxide semiconductor (CMOS) based gate-defined quantum dots [22], isotropically purified Si lattices [23],[24], along with Si/SiGe heterostructures [25] have emerged as the leading contenders for quantum computing application with spin-qubits. The absence of intrinsic piezoelectricity in these heterostructures restricts the investigation of AE interactions. In this work, we report on the first demonstration of gate-tunable acoustoelectric (AE) interaction in heterogeneously integrated Lithium Niobate thin film on Silicon substrate (LNOS). The intrinsically large coupling coefficient (K^2) of LNOS provides a promising path toward CMOS compatible silicon acoustoelectronics, for high gain, non-reciprocal RF components, as well as qubit manipulation.

2. AE interactions in LNOS

AE interaction (α) is expressed as [2]:

$$\alpha = 0.5\, k\, K^2\, \frac{y}{(1+y^2(1+b)^2)} \qquad (1)$$

where $y = \frac{\sigma/k}{(\epsilon_p+\epsilon_s)(v_d-v_s)}$, $b = \frac{k^2(\epsilon_p+\epsilon_s)D}{\sigma}$, k is the AW wavenumber, ϵ_p is the piezoelectric permittivity, K^2 is the effective electromechanical coupling coefficient of the AW, D is the diffusion coefficient, v_s is the velocity of the AW, v_d is the drift velocity of free carriers, and σ and ϵ_s are the conductivity and permittivity of the semiconductor, respectively. The ratio y describes the Kramers–Kronig relationship [26] between the AE effect and the AW velocity. Renormalization of the AW velocity is induced, in response to varying the electrostatic boundary condition at the piezoelectric-semiconductor interface. The AW velocity continuously changes between its two extreme values corresponding to unscreened (v_s) and metallic screening of the piezoelectric fields at the interface ($\frac{v_s}{(1+0.5\,K^2)}$). In contrast, the AE effect is non-existent for both boundary values and is at its strongest when AW velocity is midway ($\frac{v_s}{(1+0.25\,K^2)}$). between its extreme values[12]. This critical conductivity of the semiconductor corresponds to a regime where the semiconductor carrier density is maximally modulated by the displacement charge density of the AW potential. Mathematically, maximum AE interaction happens for a semiconductor sheet conductance

$$\sigma_m = k * (\epsilon_p+\epsilon_s) * (v_d - v_s). \qquad (2)$$

Typical σ_m values lie between 1E-6 and 1E-4 mho sq^{-1} [12],[27].

In the LNOS heterostructure, the desired semiconductor conductance can, in principle, be attained by impurity doping the silicon lattice or by using standard field effect techniques. Controlling the carrier concentration by impurity doping becomes challenging in lowly-doped Si nanostructures [28], which are prone to the influence of surface states [29] at the LN/Si interface. Thus, in addition to controlling the Si dopant concentration, control over surface state density at the interface is necessary to optimize AE interaction. Alternatively, a gate electrode deposited on the top surface of the high permittivity LN film can be used to provide an electrostatically tunable 2D inversion or accumulation layer for AE interaction on a high resistivity (HR) substrate. The larger acoustic velocity of silicon, compared to LN, confines the AW energy and electrostatic potential to the LN/Si interface. Hence, the presence of a metallic gate on the top surface of the LN film does not significantly affect the AW electrostatic potential at the LN-Si interface.

The application of an electrostatic potential at the LN-Si interface allows one to tune the surface potential of Si [23],[30],[31] and hence, dynamically control the AE interaction. Fig. 1(a) shows the plot of AE gain, at a carrier drift velocity of 1E6 cm/s, as a function of the surface potential of an n-type, standard resistivity (~1E16 phosphorous dopants per cm^3) silicon wafer [13],[32]. For comparison, the surface potential of silicon is expressed in terms of a back-gate voltage. As alluded to earlier, maximum AE gain occurs when the semiconductor sheet conductance is comparable to σ_m. This happens close to flat band and weak inversion for majority and minority carriers in a standard doped n-type Si wafer. The maximum around flat-band can be understood from the fact that, around flat-band, AE interaction decreases for both accumulation (when the carrier density is increased, and screening length is decreased) and depletion (when the static space charge region also contributes to the screening of the AW). The expected AE attenuation for a high resistivity, n-type wafer is plotted as a function of the gate voltage in supplementary information Fig S1.

3. Experimental design and characterization

3.1. Passive AE devices for capacitance measurements on standard doped silicon substrates (LNOS-C)

128° Y-cut LN thin films were transferred onto standard doped (n-type 1E16 cm^{-3}) Silicon substrates. These substrates can be used to study AE attenuation by simply integrating a metal oxide semiconductor capacitor (MOSCAP) in the AW delay line (Fig 1b). In this case, the MOSCAP is a hybrid metal/LN/SiO_2/Si/metal capacitor. The thin silicon dioxide film (20 nm) acts as a buffer between the LN film and Silicon, reducing the interface charge density. The gate voltage is applied between the top electrode on the LN film and the bottom electrode at the back of the substrate.

3.2. Active AE devices on HR silicon substrates

In this case, the starting material is a n-type, high resistivity (>5000 Ω.cm) Si substrate (Fig. 1c). An implantation mask is lithographically defined to selectively dope regions (~300 nm deep, ~5E19 cm^{-3}), which would be used later for Ohmic contacts. After implantation and dopant activation, 128° Y-cut LN thin films were transferred onto the substrates using "ion-slicing" technology [33]. After bonding, Ti/Au electrodes are deposited and patterned by lift-off on the LN surface for the IDT and the gate electrode. Ohmic contacts are subsequently made to the heavily doped contact regions by opening vias in the LN by RIE and depositing Al. Thermal oxide on the back-side of the wafer is removed by BOE and Al is deposited for back-gating. A final post-metallization anneal is conducted at 430° C in forming gas ambient for 20 minutes. A detailed schematic of the process flow is provided in supplementary information Fig S2.

4. Results and discussion

4.1. Acoustic wave measurements

On standard doped silicon substrates (LNOS-C), electromagnetic feedthrough coupling between the two IDT ports dominates the transmission data. Hence, the frequency response of the AW delay lines is time-gated to isolate the acoustic mode. This procedure is not necessary to identify the acoustic mode in the case of HR silicon substrates (LNOS) but

is still used for consistency. The time-gated insertion loss of Rayleigh mode devices fabricated with IDT pitch corresponding to wavelengths between 4.5 and 10 μm deposited on LNOS-C is shown in Fig. 2(a). Insertion loss of Rayleigh devices fabricated on LNOS substrates is provided in supplementary information Fig S3. The frequency dispersion of the SAW velocity, K^2 on LNOS-C substrates and their comparison with COMSOL simulation is discussed in an earlier publication [34].

4.2. AE attenuation on LNOS-C

The integration of MOSCAPs in the middle of the AW delay line allows us to tune electrostatically the surface carrier concentration of the silicon substrate. Fig. 2(b) shows the optical image of a 680 MHz SAW delay line with a MOSCAP, as well as the measurement setup. An approximate K^2 of 0.9% is extracted from fitting the corresponding dip in the reflection (S11) spectra [35]. The measured AE attenuation, manifested through the change in the peak transmission of the mode as a function of the gate voltage, is plotted in Fig. 2(b). The normalized capacitance is also plotted for comparison to clearly identify the electronic regime of device operation. Maximum AE interaction is expected for a sheet conductance corresponding to the substrate dopant concentration (1E16 cm^{-3}). Hence, maximum AE attenuation can be expected to occur close to flat-band for LNOS-C substrates. Capacitance measurements reveal a shift in the flat-band voltage, indicating a negative charge density has been induced at the interface due to the bonding process. Hence, at zero gate bias, the Si surface is in depletion and the AE interaction is at a minimum. The maximum attenuation measured is about 4 dB/cm and occurs when the positive gate bias can compensate the shift in flat-band from trapped charges. The magnitude of AE interaction expected (Fig S4) by assuming a K^2 of 0.9% is 16 dB/cm, which is significantly larger than the measured value. The discrepancy is expected to be due to a large fraction of AW induced displacement charge being compensated by traps and localized interface charge sites, rather than semiconductor space charge [36], [37].

4.3. AE attenuation and gain on LNOS

It can be inferred from measurements on the LNOS-C substrates that ion doping the Si substrate does not guarantee the carrier concentration desired for AE interaction. Hence, standard field effect techniques are used to achieve carrier control for AE interactions in the LNOS substrates. The HR substrate used in the LNOS heterostructure eliminates electromagnetic feedthrough coupling between the IDT ports and provides an intrinsically higher mobility for free carriers than standard doped wafers. Regions with n+nn+ doping were defined at the surface of the substrate by heavily doping with Phosphorus ions (n+ regions are coloured blue in Fig. 3(a)). Standard metal oxide semiconductor field effect techniques (MOSFET) techniques were used for control of the carrier density and velocity in the channel region.

An SEM micrograph of the device used for LNOS measurements is shown in Fig. 3(a). The device is basically an AW delay line with 8 pairs of gated n+nn+ channel (GC) regions chained together in the middle of the delay line. The GC structure is a simple array of interdigitated 50 um channels whose edges are defined with heavily doped 10 um silicon regions. The alternating polarity of the interdigitated leads correspond to the source and drain terminals. A top gate (coloured red in Fig. 3(a)) deposited on alternating channel regions provides electrostatic control to create the desired carrier concentration in one half of the interdigitated pattern, while surface depletion eliminates drift of carriers in the other half of the pattern corresponding to the opposite electric field direction. The gated segmented regions are designed to provide two major benefits: 1) switchable AE interaction by control of impedance presented by the semiconductor to the acoustic wave; 2) small channel length (50 um) to reach the required drift velocities at small voltages and hence, operate within the linear regime of the transistor.

AE attenuation of the GC regions is demonstrated by plotting the change in the peak of the mode as a function of the gate voltage applied to VG in Figure 3(b). A clear peak in the AE attenuation is observed at around 4VG, corresponding to a sheet conductance of 5E-6 mho sq^{-1}. The magnitude of peak AE attenuation is about an order of magnitude smaller than analytical estimation (Fig S5). The difference in measured and estimated data is further evidence of weak coupling at the LN/Si interface. Indeed, a large interface state density can be expected to partially screen the piezoelectric fields and drastically reduce the AE interaction.

In contrast to AE attenuation, obtaining AE amplification in a gated structure is less straightforward. The addition of a large drift field significantly distorts the uniformity of carrier density under the gated region. To enable direct comparison with two terminal measurements, it is important to limit operation of the device in the linear or quadratic regime. It can be seen in Fig. 4(a) that by using sufficiently short channels (50 um) we are able to reach electric fields (up to ~0.5 kV/cm) required to demonstrate AE non-reciprocity in the linear regime. At larger applied fields, in addition to saturation effects, the measured current becomes dominated by parasitic contribution from conduction paths through the bulk n-type HR substrate. This happens because below threshold operation of the GC regions makes the HR substrate conductivity comparable with the surface conductivity. In future devices, the surface conductivity can be easily isolated from substrate conductivity by switching to inversion layer regime of operation. For these accumulation mode devices,

AE was studied at small fields close to the linear regime of device operation. Fig. 4(b) shows clear non-reciprocity observed between S12 and S21 for 7 V bias to the gate electrode and electric fields from 0 KV/cm to 0.5 KV/cm. For larger gate biases, and hence larger sheet conductance, an increased linearity is observed but with a decreased strength of AE interaction. This trend can be expected from theory [2]. However, the magnitude of the change is about an order of magnitude smaller which could be attributed to poor interface quality and any non-uniformity of carrier concentration in the GC regions. Observation of AE effects at larger electric field is limited by device design, Joule heating, and non-uniformity in surface potential due to channel pinch-off effects.

5. Conclusion

The large K^2, in combination with gated control of carrier density offered by the LNOS material platform promises to overcome past hurdles to AE technology, enabling a new era of gate-controlled, non-reciprocal RF devices. Additionally, the flexibility of LNOS heterostructure allows straightforward integration of AE devices with CMOS transistors as well as ambipolar quantum dots fabricated on HR Silicon wafers [38],[39]. However, further understanding of trap states at the LN/Si interface is required to realize the full potential of the LNOS heterostructure.

Figure captions

Figure 1(a) Theoretical estimation of AE gain at the LNOS heterostructure for a carrier drift velocity of 1E6 cm/s. Parameters are K^2 =5%, oxide thickness = 75 nm, dopant density = 1E16 cm^{-3}, and AW frequency= 680 MHz; (b) Cross section of the LNOS-C structure and the metal/LN/SiO_2/Si/metal MOSCAP; (c) Cross section of the LNOS device fabricated with Ohmic contacts realized by n+ implantation of HR Si.

Figure 2(a) Time-gated insertion loss of IDTs fabricated on LNOS-C substrates with wavelengths varying from 10 μm to 4.5 μm; (b) Optical image of AE delay line with MOSCAP and schematic of the measurement setup; (c) Experimental characterization of AE attenuation with respect to the applied gate voltage for a 680 MHz (λ = 6 μm) device. The measured capacitance is also shown to identify the electronic regime of operation.

Figure 3: (a) SEM micrograph of an interdigitated array of gated channel (GC) regions designed to obtain tunable gain. Implanted regions are colored in blue, while the GC regions are colored in red; (b) AE attenuation of the GC region studied as a function of the gate voltage. The measured sheet conductance of the device is also plotted for comparison.

Figure 4: (a) Output characteristics of a gated-segmented LNOS device; (b) The time-gated peak of S_{12} and S_{21} of a 680 MHz gated-segmented LNOS device is plotted as a function of bias, showing clear non-reciprocity. The dots correspond to experimental measurement and the line is a guide to the eye. The measured current is also plotted for comparison; (c) Measurement of non-reciprocal asymmetry is plotted as a function of drift field for different gate voltages.

Acknowledgements

The author acknowledges insightful discussions with Matthew Storey, and Siddhartha Ghosh. This work was funded through the DARPA MTO SPAR program (Grant 108712). LNOS substrates were prepared by Dr. Payam Rabiei at Partow Technologies, LLC. Fabrication was performed at the Pritzker Nanofabrication Facility of the Institute for Molecular Engineering at the University of Chicago, which receives support from Soft and Hybrid Nanotechnology Experimental (SHyNE) Resource (NSF ECCS-1542205).

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