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Carbon vacancy control in p^+-n silicon carbide diodes for high voltage bipolar applications

H M Ayedh[1,2,*], K-E Kvamsdal[1], V Bobal[1], A Hallén[3], F C C Ling[4] and A Yu Kuznetsov[1]

[1] University of Oslo, Department of Physics, P.O. Box 1048 Blindern, N-0316 Oslo, Norway
[2] Department of Electronics and Nanoengineering, Aalto University, Tietotie 3, FI-02150 Espoo, Finland
[3] Royal Institute of Technology KTH, School of Information and Communication Technology (ICT), SE-164 40 Kista-Stockholm, Sweden
[4] Department of Physics, The University of Hong Kong, Pokfulam, Hong Kong, People's Republic of China

E-mail: hussein.ayedh@aalto.fi

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Abstract

Controlling the carbon vacancy (V_C) in silicon carbide (SiC) is one of the major remaining bottleneck in manufacturing of high voltage SiC bipolar devices, because V_C provokes recombination levels in the bandgap, offensively reducing the charge carrier lifetime. In literature, prominent V_C evolutions have been measured by capacitance spectroscopy employing Schottky diodes, however the trade-offs occurring in the p^+-n diodes received much less attention. In the present work, applying similar methodology, we showed that V_C is re-generated to its unacceptably high equilibrium level at $\sim 2\times10^{13}$ V_C cm^{-3} by 1800 °C anneals required for the implanted acceptor activation in the p^+-n components. Nevertheless, we have also demonstrated that the V_C eliminating by thermodynamic equilibrium anneals at 1500 °C employing carbon-cap can be readily integrated into the p^+-n components fabrication resulting in $\leqslant 10^{11}$ V_C cm^{-3}, potentially paving the way towards the realization of the high voltage SiC bipolar devices.

Supplementary material for this article is available online

Keywords: silicon carbide (SiC), carbon vacancy, high voltage bipolar devices, thermodynamic equilibrium, DLTS

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon carbide (SiC) unipolar power devices, such as Schottky diodes and MOSFETs, are nowadays commercially available. These devices feature lower losses, less cooling needs and improved reliability as compared to the silicon (Si) power devices. Thus, SiC Schottky diodes and MOSFETs, in particular based on 4H-SiC polytype, are now viable alternatives to Si p-n diodes and IGBTs in the voltage range of 1–3 kV, but are also taking increasing market shares below 1 kV. For extreme higher voltage devices, 5–10 kV and beyond, used, e.g. for traction and high voltage direct current applications, Si bipolar devices are still dominating, because of two SiC limitations: the bipolar degradation issues and insufficiently long charge carrier lifetimes. The bipolar degradation issues, have gradually been resolved; both on behalf of the improved substrates quality and using more advanced device architectures,

* Author to whom any correspondence should be addressed.

e.g. by introducing buffer layers between the substrate and the low doped voltage supporting drift layer, preventing the basal plane dislocations to protrude into the drift layer. Thus, the remaining hurdle for manufacturing of high voltage SiC bipolar devices is the control of point defects that give rise to the recombination levels in the bandgap, reducing the charge carrier lifetimes. In this context, much of the research attention was attracted to the carbon vacancy (V_C), known as the prime carrier lifetime killer in SiC [1–3].

The dominant electrically active defects in n-type 4H-SiC are conventionally labelled as $Z_{1/2}$ and EH_7, representing two different charge states of the V_C [4]. $Z_{1/2}$ is located at ∼0.7 eV below the conduction band edge (E_C) and is attributed to a double acceptor state, i.e. $V_C(2-/0)$; notably, (2−/0) index means that V_C is neutral when the state is empty and negative doubly-charged when filled. EH_7 is a single donor state of V_C at $\sim E_C - 1.5$ eV, i.e. $V_C(0/+)$; it is neutral when the state is filled and positively charged when empty. Typically, the V_C concentration ($[V_C]$) in the state-of-the-art epitaxial 4H-SiC wafers remains in the order of $\sim 5\times10^{12}$ cm^{-3} hindering charge carrier lifetime in excess of ∼5 μs. Thus, dedicated efforts were undertaken to reduce the $[V_C]$ in 4H-SiC by post-growth processing of the epi-wafers, based on injecting highly mobile carbon interstitials (C_i's) from the surface or the near surface region, to recombine with V_C's in the 'bulk' of the epi-layer resulting in the V_C's annihilation, ($V_C + C_i \rightarrow \varnothing$). Three different approaches are commonly used: (1) near surface ion implantation followed by high temperature annealing [5–7], (2) thermal oxidation of the Si-terminated 4H-SiC surface [8–12] and (3) annealing the 4H-SiC wafers at moderate temperature ≤1500 °C under C-rich surface conditions (carbon cap) to establish a thermodynamic equilibrium of V_C [13–16]. The target was to keep the $[V_C] \leqslant 10^{11}$ cm^{-3} which could enable sufficiently long lifetimes. However, most of the literature data correlating the V_C with electrical performance were collected using Schottky diodes, while the trade-offs occurring in the p^+-n diodes received much less attention.

Indeed, anneals at ∼1800 °C are inevitable for sufficient electrical activation of the ion-implanted acceptors in order to realize low-resistivity p-type layers [17], even though one can try playing with such parameters like the implantation temperature and dose rate [18]. Previous studies on the evolution of $[V_C]$ in 4H-SiC epi-wafers showed that V_C's can be formed easily and sharply during high temperature device processing [19, 20]. Indeed, the formation enthalpy of ∼4.8 eV for V_C in its neutral charge state under the carbon-rich ambient was deduced theoretically and experimentally [20–22]. These aspects make the initial mastering of $[V_C] \leqslant 10^{11}$ cm^{-3} in the epi-wafers dedicated for the bipolar device manufacturing not practical. Thus, even though the $[V_C] \leqslant 10^{11}$ cm^{-3} criterion has been demonstrated in the epi-wafers employing one of the methods mentioned above, there is a serious remaining question related to the V_C re-generation during the p^+-n diode fabrication. Moreover, there is no data whether the Al doped p^+-layer may influence the transportation of C_i's from the surface into the bulk of the epi-layer.

In the present paper, we clearly demonstrate that the V_C indeed re-generates during the p^+-n diode manufacturing in spite of the initial V_C elimination in the epi-wafers applying thermodynamic equilibrium anneals at 1500 °C under C-rich ambient (C-cap). Nevertheless, we also show that this C-rich ambient anneals at moderate temperatures ∼1500 °C can be readily integrated as crucial steps of the p^+-n fabrication process. The instructive message of this paper is that, the processing recipes might be extended with a finishing carbon-cap annealing step at ∼1500 °C intended to remove the V_C's generated in 4H-SiC by high temperature.

2. Experimental

The starting material in this work was an n-type (nitrogen doped) 100 mm diameter 4H-SiC wafer purchased from Cree Inc. with ∼10 μm thick epi-layer. The epi-layer was grown by chemical vapour deposition (CVD) 4°-off the c-axis on top of the (0001) Si-terminated surface of a heavily doped n-type 4H-SiC substrate ($\geqslant 10^{18}$ cm^{-3}). The net carrier (electron) concentration of the epi-layer was $\sim 1\times10^{15}$ cm^{-3} as determined by capacitance-voltage (CV) measurements undertaken at room temperature with a 1 MHz probe frequency.

A set of p^+n diodes were prepared on four identical samples with a size of 6×6 mm^2 that were laser-cut from the epi-wafer. After the standard RCA cleaning, ∼220 nm thick SiO_2 films were deposited on all samples using plasma enhanced CVD. Further, conventional photolithography was then applied to make circular 500 μm in diameter openings for subsequent fabrication of the p^+ regions by 36 keV Al^+ ion implants using the dose of $\sim 1\times10^{15}$ cm^{-2} at 500 °C. Notably, before subsequent dopant-activation anneal, the remaining lithography pattern was etched away and the samples were protected by a pyrolized resist film (called carbon-cap in the rest of the paper), where the pyrolysis was performed in forming gas at 900 °C for ∼5 min. Then all four samples were annealed at 1800 °C for 30 min in a high-purity argon atmosphere employing an RF inductively heated furnace. The carbon-cap was then removed by dry thermal oxidation at 900 °C for 30 min (we clarify here that these oxidation conditions are insufficient to affect V_C engineering that needs much higher thermal budgets, see references [8–12]).

The Al concentration versus depth profiles in the fabricated p^+n diodes were measured by secondary ion mass spectrometry, confirming Al maximum concentration of $\sim 3\times10^{19}$ cm^{-3} at the depth of ∼100 nm. Ohmic contacts to the p^+ areas of the diodes were deposited by electron beam evaporation of Al into self-aligned 400 μm in diameter openings determined by the second lithography step. Ohmic contacts to the back side, i.e. n-area of the diodes were Al evaporated too. The contacts were then annealed in a tube furnace with nitrogen flow at 350 °C for 30 min. In term of electrical performance of the diodes at the conditions of our measurements—we envisage no negative effects of using Al as an Ohmic contact, however, for better and more practical Ohmic contacts one can use the recipe stated in Ref. [23]. The diodes were labelled as B, C, D and E so that the first 1800 °C acceptor activation anneal was common for all of the p^+n diodes used in this study. In addition, a similarly shaped

Table 1. Samples and corresponding annealing steps. Notably, annealing step (1) is inevitable thermal treatment to activate ion implanted acceptors in the p^+-n diodes; additional thermal treatments, i.e. annealing steps (2) and (3), were applied to monitor the evolution of the $[V_C]$.

Label (sample type)	Annealing step (1) T (°C)/time	Annealing step (2) T (°C)/time	Annealing step (3) T (°C)/time
A (Schottky diode)	—	—	—
B (p^+-n diode)	1800 °C/30 min.	—	—
C (p^+-n diode)	1800 °C/30 min.	1500 °C/3 h	—
D (p^+-n diode)	1800 °C/30 min.	1500 °C/3 h	1800 °C/30 min.
E (p^+-n diode)	1800 °C/30 min.	1600 °C/40 min.	—

Schottky diode was fabricated on a piece of the epi-wafer not subjected to thermal treatments; this sample was labelled 'A', benchmarking the $[V_C]$ in the as-grown epi-wafer.

The A–E diodes were characterized by current–voltage (IV), CV, and deep level transient spectroscopy (DLTS) to check the diodes quality and to monitor the $[V_C]$. In particular, for DLTS we used the setup and $[V_C]$ extraction methodology described elsewhere [7, 20, 24]. In short, the reverse bias voltage was kept at −10 V, pulsing it to 0 V using a filling pulse width of 50 ms. The DLTS signal ($\Delta C/C$), the capacitance change as carriers are emitted from defect states relative to the reverse bias capacitance, was extracted applying a lock-in weighting function having rate windows in the range of (20–640 ms)$^{-1}$. For clarity, the $[V_C]$ was monitored via the $V_C(2-/0)$ level (known as the $Z_{1/2}$ level) located at $\sim E_C - 0.7$ eV and having a peak position of ∼285 K in DLTS spectra with a rate window of (640 ms)$^{-1}$. Upon accomplishing the first round of the characterization, some of the samples were subjected to additional anneals in accordance with the data in table 1. Notably, prior to these additional anneals all metallic contacts were removed, samples were cleaned and carbon-caps were re-fabricated. After the additional anneals—referred as 'annealing step (2) and (3)' in table 1—the contacts were re-fabricated to enable the next steps of the IV, CV, and DLTS measurements. Notably, the 1500 °C–1600 °C anneals were performed in a high-purity Ar ambient employing a tube furnace, applying the C_i ambient (carbon-cap) thermodynamic equilibrium annealing method known to reduce the $[V_C]$ [13–16].

3. Results and discussion

Figure 1 displays a portion of DLTS spectra for samples A and C, highlighting the intensity of the $V_C(2-/0)$ signature having a peak position at ∼285 K for the rate window (640 ms)$^{-1}$. The activation energy of $V_C(2-/0)$ thermal ionization is deduced from the DLTS measurements and found to be 0.7 eV below the conduction band edge ($\sim E_C - 0.7$ eV), while the intensity of this peak is directly proportional to the V_C concentration. Thus, the peak in the A sample represents the initial $[V_C]$, which is relatively low and is characteristic of the state-of-the-art 4H-SiC epi-wafers. However, the p^+-n diode fabrication (see sample C after 1800 °C in figure 1) is associated with a dramatic increase of the $V_C(2-/0)$ signal. Apparently,

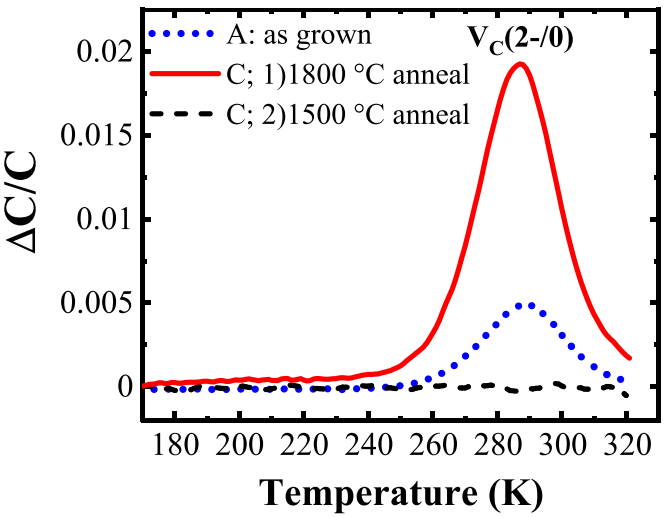

Figure 1. DLTS spectra of the $V_C(2-/0)$ ($Z_{1/2}$) level in sample A (as grown) and in sample C; first after post-implantation annealing at 1800 °C for 30 min and then after an extra heat treatment at 1500 °C for 3 h. Spectra are recorded with lock-in weighting function for the rate window (640 ms)$^{-1}$.

low V_C contents in the initial epi-wafers dedicated for high voltage bipolar device processing is insufficient, since the V_C regenerates during the acceptor activation anneals in p^+-n diodes, see figure 1. Nevertheless, the additional annealing step (see sample C after 1800 + 1500 °C in figure 1) results in the $V_C(2-/0)$ intensity falling below the DLTS detection limit. Thus, the data in figure 1 supports the validity of thermodynamic equilibrium anneals employing carbon-caps for controlling the $[V_C]$ in 4H-SiC p^+n diodes, consistently with the literature data measured using Schottky diodes in thermally treated epi-wafers [5–16]. Notably, the annealing step (2) applied for sample C in figure 1 was sufficient for eliminating the V_C's in the present ∼10 μm thick epi-layer, however customized anneals might be applied as a function of the layer thickness in accordance with the simulation results in Ref. [14] for thicker samples. Importantly, samples B–E behaved identically after the first annealing step.

At this point, C_i-ambient annealing methods known from the literature may be compared for the applicability of controlling the $[V_C]$ in p^+-n diodes. Systematically speaking, the three approaches (1–3) mentioned in the introduction part of this paper and examined in literature for eliminating the $[V_C]$

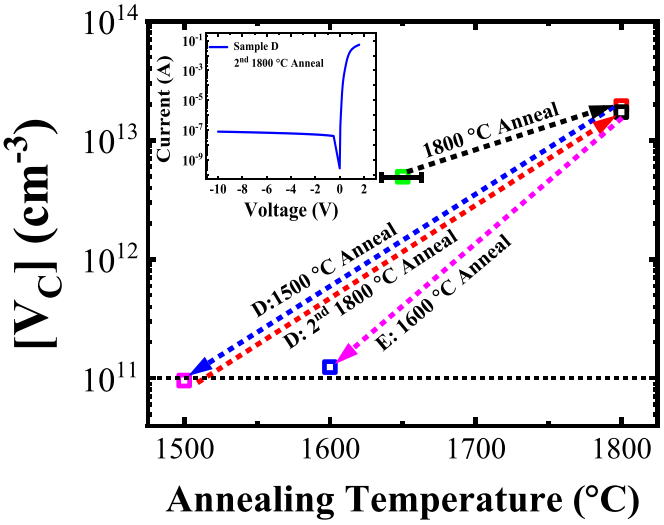

Figure 2. V_C concentration versus annealing temperature under C-rich ambient conditions for p^+n 4H-SiC diodes. The displayed data are for the samples D and E after different annealing stages; starting from as grown level before the fabrication processes of the p^+n 4H-SiC diodes, and then after the post-implantation anneal at 1800 °C for 30 min. The data include the [V_C] in sample D after 1500 °C anneal for 3 h and then after another round of re-annealing at 1800 °C for 30 min. It shows also V_C content in sample E after 1600 °C anneal for 40 min following the ion-activating anneal at 1800 °C. The as grown [V_C] level measured in sample A was assigned to correspond heat treatment at around 1650 °C with a margin of ±25 °C, according to the equilibrium line of V_C formation. The inset plots the IV data in sample D after several consequent anneals, illustrating the high quality of the p^+n diodes.

in SiC epi-layers have a common conceptual principle in terms of injecting the C_i's towards the bulk to recombine with the V_C's. However, the excess C_i originates from different locations, where C_i's in (1–2) are released from the carbon sublattice inside the sample—either by oxygen interaction with Si atoms or kicking-out of C atoms by energetic ions. In either case, if applying (1–2) to a p^+-n diode, it will consume or modify at least the p^+ region of the device. In contrast, while applying (3), C_i's are introduced from the carbon-cap via the surface, not disturbing the sample structure.

Importantly, approach (3) employing carbon-cap anneals at moderate temperatures can be readily applied several times and if needed at different steps of the device fabrication to remove the V_C's without a negative impact on the top layers of the device. Indeed, we demonstrated it by selecting several identical p^+-n diodes (see samples B–E in table 1) and monitoring the [V_C] upon different thermal treatment steps during the device fabrication, as shown in figure 2. It should be mentioned here that the dotted lines/arrows in figure 2 are to indicate the trends for the [V_C] change between two different annealing steps, and they do not represent linear relations between [V_C] and annealing temperatures. The data in figure 2 confirm that V_C in 4H-SiC is a refractory point defect and will not be eliminated permanently during the first run of V_C elimination by the C_i ambient annealing. Moreover the [V_C] is practically controlled by the last annealing run that plays a crucial role for determining the [V_C], and consequently the carrier lifetime. Indeed, the re-anneal of sample D at 1800 °C for the second time, returns the [V_C] back to its unacceptably high equilibrium level at $\sim 2\times10^{13}$ V_C cm^{-3}, see figure 2.

The inset in figure 2 provides an example of the IV characteristics for the diodes in table 1, specifically for sample D after the 3rd annealing step. In addition, the IV data for a separate batch of identical samples processed under conditions identical to that for samples B–E in table 1 are presented in the supplementary material (available online at stacks.iop.org/JPD/54/455106/mmedia). It could be deduced as a preliminary conclusion that the trend for the leakage current variations in these samples are consistent with the V_C evolutions, indicating good repeatability of the phenomena under investigation. Notably, the detailed analysis of the IV curves as a function of the [V_C] is beyond the direct scope of the present study. Overall, the IV data re-confirm the quality of the p^+-n diodes used in the present study, as an added value for the DLTS data credibility; since the applicability of the DLTS measurements relies on the high diode quality.

Notably, the major physical processes occurring during the thermodynamic equilibration of the V_C under C_i ambient anneals are [14, 15]: thermal generation of V_C's, injection of C_i's from the carbon-cap followed by recombination with V_C's in the bulk, and out-diffusion of V_C's towards the surface. Thermal generation of V_C competes with the injection of C_i's at each specific temperature. In practice, the V_C generation dominates at high temperatures and C_i injection prevails at moderate temperatures leading to the V_C annihilation.

Thus, the initial elimination of V_C's in 4H-SiC epi-wafers employing one of the C_i ambient methods [5–16] will not keep the epi-layer free of V_C permanently—as shown in figure 2—since it can be readily re-generated during any further annealing step at high temperature required for the fabrication of the bipolar devices. Therefore, in order to control the [V_C] and, consequently, the minority carrier lifetime, the processing recipes might be extended with an extra C_i ambient annealing step at ~1500 °C intended to remove the V_C's generated in 4H-SiC by high temperature. At this end, thermodynamics equilibrium anneals with C-cap at moderate temperatures demonstrated effective control of the V_C in 4H-SiC devices and can be readily integrated in the fabrication process customizing the specific annealing conditions in accordance with the thickness of the epi-layer to treat.

4. Conclusions

We have clearly demonstrated that extra high temperature processing during the fabrication steps of the p^+-n diodes will enhance the [V_C] to its thermodynamic equilibrium value at the applied temperature. Therefore, for effective control of the [V_C] and for corresponding minority carrier lifetime control, the p^+-n fabrication process recipe might involve a finishing C_i ambient annealing step, for eliminating the re-generated V_C's. At this end, all carbon ambient annealing methods known from literature—with exception of the carbon cap anneals—will consume and/or modify the near surface

part of the device, which is unacceptable for typical device architectures. In contrast, our data demonstrate that the carbon cap anneals at moderate temperature can be readily integrated into the p^+-n components fabrication, potentially paving the way towards the realization of the high voltage SiC bipolar devices.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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ORCID iDs

H M Ayedh https://orcid.org/0000-0002-1677-0160
A Hallén https://orcid.org/0000-0002-8760-1137
F C C Ling https://orcid.org/0000-0003-4757-1065
A Yu Kuznetsov https://orcid.org/0000-0003-1822-9850

References

[1] Klein P B, Shanabrook B V, Huh S W, Polyakov A Y, Skowronski M, Sumakeris J J and O'Loughlin M J 2006 Lifetime-limiting defects in n-4H-SiC epilayers *Appl. Phys. Lett.* **88** 052110
[2] Danno K, Nakamura D and Kimoto T 2007 Investigation of carrier lifetime in 4H-SiC epilayers and lifetime control by electron irradiation *Appl. Phys. Lett.* **90** 202109
[3] Klein P B 2008 Carrier lifetime measurement in n-4H-SiC epilayers *J. Appl. Phys.* **103** 033702
[4] Son N T *et al* 2012 Negative-U System of carbon vacancy in 4H-SiC *Phys. Rev. Lett.* **109** 187603
[5] Storasta L and Tsuchida H 2007 Reduction of traps and improvement of carrier lifetime in 4H-SiC epilayers by ion implantation *Appl. Phys. Lett.* **90** 062116
[6] Storasta L, Tsuchida H, Miyazawa T and Ohshima T 2008 Enhanced annealing of the Z1/2 defect in 4H-SiC epilayers *J. Appl. Phys.* **103** 013705
[7] Ayedh H M, Hallén A and Svensson B G 2015 Elimination of carbon vacancies in 4H-SiC epi-layers by near-surface ion implantation: influence of the ion species *J. Appl. Phys.* **118** 175701
[8] Hiyoshi T and Kimoto T 2009 Reduction of deep levels and improvement of carrier lifetime in n-type 4H-SiC by thermal oxidation *Appl. Phys. Express* **2** 041101
[9] Hiyoshi T and Kimoto T 2009 Elimination of the major deep levels in n- and p-type 4H-SiC by two-step thermal treatment *Appl. Phys. Express* **2** 091101
[10] Lovlie L S and Svensson B G 2011 Enhanced annealing of implantation-induced defects in 4H-SiC by thermal oxidation *Appl. Phys. Lett.* **98** 052108
[11] Lovlie L S and Svensson B G 2012 Oxidation-enhanced annealing of implantation-induced Z1/2 centers in 4H-SiC: reaction kinetics and modeling *Phys. Rev.* B **86** 075205
[12] Kawahara K, Suda J and Kimoto T 2012 Analytical model for reduction of deep levels in SiC by thermal oxidation *J. Appl. Phys.* **111** 053710
[13] Ayedh H M, Nipoti R, Hallén A and Svensson B G 2015 Elimination of carbon vacancies in 4H-SiC employing thermodynamic equilibrium conditions at moderate temperatures *Appl. Phys. Lett.* **107** 252102
[14] Ayedh H M, Nipoti R, Hallén A and Svensson B G 2017 Thermodynamic equilibration of the carbon vacancy in 4H-SiC: a lifetime limiting defect *J. Appl. Phys.* **122** 025701
[15] Ayedh H M, Nipoti R, Hallén A and Svensson B G 2018 Kinetics modeling of the carbon vacancy thermal equilibration in 4H-SiC *Mater. Sci. Forum* **924** 233–6
[16] Ayedh H M, Baathen M E, Galeckas A, Hassan J U, Bergman J P, Nipoti R, Hallen A and Svensson B G 2018 (Invited) controlling the carbon vacancy in 4H-SiC by thermal processing *ECS Trans.* **86** 91–7
[17] Nipoti R, Nath A, Rao M V, Hallén A, Carnera A and Tian Y-L 2011 Microwave annealing of very high dose aluminum-implanted 4H-SiC *Appl. Phys. Express* **4** 111301
[18] Kuznetsov A Y, Wong-Leung J, Hallén A, Jagadish C and Svensson B G 2003 Dynamic annealing in ion implanted SiC: flux versus temperature dependence *J. Appl. Phys.* **94** 7112–15
[19] Zippelius B, Suda J and Kimoto T 2012 High temperature annealing of n-type 4H-SiC: impact on intrinsic defects and carrier lifetime *J. Appl. Phys.* **111** 033515
[20] Ayedh H M, Bobal V, Nipoti R, Hallén A and Svensson B G 2014 Formation of carbon vacancy in 4H silicon carbide during high-temperature processing *J. Appl. Phys.* **115** 012005
[21] Hornos T, Gali A and Svensson B G 2011 Large-scale electronic structure calculations of vacancies in 4H-SiC using the Heyd-Scuseria-Ernzerhof screened hybrid density functional *Mater. Sci. Forum* **679-680** 261–4
[22] Trinh X T, Szász K, Hornos T, Kawahara K, Suda J, Kimoto T, Gali A, Janzén E and Son N T 2013 Negative-carbon vacancy in 4H-SiC: assessment of charge correction schemes and identification of the negative carbon vacancy at the quasicubic site *Phys. Rev.* B **88** 235209
[23] Nipoti R, Moscatelli F and De Nicola P 2013 Al^+ implanted 4H-SiC p^+-i-n diodes: forward current negative temperature coefficient *IEEE Electron Device Lett.* **34** 966–8
[24] Svensson B G, Rydén K-H and Lewerentz B M S 1989 Overlapping electron traps in n-type silicon studied by capacitance transient spectroscopy *J. Appl. Phys.* **66** 1699–704