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The analysis of the series resistance and interface states of MIS Schottky diodes at high temperatures using *I–V* characteristics

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ABSTRACT

The temperature dependence of the current–voltage (*I–V*) characteristics of Au/SiO_2/n-Si (MIS) Schottky diodes has been measured in the temperature range of 300–400 K. Based on the thermionic emission (TE) theory, the forward and reverse *I–V* characteristics are analyzed to calculate the MIS Schottky diode barrier parameters. The calculated zero-bias barrier height (Φ_{Bo}) and ideality factor (n) assuming TE theory show strong temperature dependence. A decrease in the value of n and an increase in Φ_{Bo} with increasing temperature is observed. The calculated values of Φ_{Bo} and n varied from 0.63 eV and 2.90 at 300 K to 0.80 eV and 1.79 at 400 K, respectively. Also, the temperature dependence of energy distribution of interface states (N_{ss}) was obtained from the forward bias *I–V* measurements by taking into account the bias dependence effective barrier height (Φ_e) and ideality factor (n). In addition, the values of series resistance (R_s) were determined using Cheung's method. These *I–V* characteristics confirmed that the distributions of N_{ss} and R_s are important parameters that influence the electrical characteristics of MIS Schottky diodes.

1. Introduction

It has been well known that there have been currently a vast number of experimental and theoretical studies on the *I–V* characteristics of metal–semiconductor (MS), metal–insulator–semiconductor (MIS) Schottky diodes and solar cells [1–15]. The analysis of *I–V* characteristics of the Schottky diodes only at room temperature does not give detailed information about their current transport mechanisms or the nature of barrier formation at the MS interface. However, the temperature dependence of the *I–V* characteristics allows us to understand different aspects of device characteristics. In general, the forward bias *I–V* characteristics of these devices deviate from the ideal thermionic emission (TE) theory [2–5,12,13]. It was often observed that the ideality factor (n) was found to decrease, while the zero-bias barrier height (Φ_{Bo}) increases with increasing temperature. Lately, the nature of the decrease in the barrier height and increase in ideality factor with a decrease in temperature in some studies [2,12,14–17] have been successfully explained on the basis of a TE mechanism with Gaussian distribution of the barrier height.

In general, the performance of a MIS Schottky diode depends on various factors such as the presence of the localized interface states existing at the semiconductor–insulator interface, interface preparation process, metal to semiconductor barrier height and series resistance. Therefore, these possible sources of error must be taken into account. The series resistance is an important parameter, which causes the electrical characteristics of MIS Schottky diodes to be non-ideal [18–21].

In this study, the forward and reverse bias *I–V* characteristics of Au/SiO_2/n-Si Schottky diodes were measured in the temperature range of 300–400 K. The temperature dependence of electrical parameters such as ideality factor, barrier height and series resistance were extracted from forward bias *I–V* measurements. Also, the density of interface state as a function of E_c–E_{ss} was obtained from *I–V* measurements. The experimental results show that these parameters were found to be strong function of temperature.

2. Experimental details

The Au/SiO_2/n-Si (MIS) Schottky diodes used in this study were fabricated using n-type (P-doped) single crystals silicon wafer with ⟨1 0 0⟩ surface orientation having thickness of 350 μm, 2 in. diameter and 2 Ω cm resistivity. For the fabrication process, Si wafer was degreased in organic solvent of $CHClCCl_2$, CH_3COCH and CH_3OH consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:35H_2O, 20% HF and finally quenched in de-ionized water for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ cm.

Immediately after surface cleaning, to form ohmic contacts on the back surface of the Si wafer, high purity gold (Au) metal (99.999%) with a thickness of ~2000 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer in the pressure of $\sim 2 \times 10^{-6}$ Torr in vacuum pump system and the evaporated Au was sintered. The oxidations are carried out in a resistance-heated furnace in dry oxygen with a flow rate of a 1.5 l/min and the oxide layer thickness

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is grown at the temperatures of 750 °C during 1.5 h. To form the Schottky contacts, the circular dots of ~2 mm diameter and ~2000 Å thick Au are deposited onto the oxidized surface of the wafer through a metal shadow mask in a liquid nitrogen trapped vacuum system in a vacuum of $\sim 2 \times 10^{-6}$ Torr. The interfacial oxide layer thickness was estimated to be about 50 Å from high frequency (1 MHz) measurement of the interface oxide capacitance in the strong accumulation region for MIS Schottky diodes.

The temperature dependence of current–voltage measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer in the temperature range of 300–400 K using a temperature-controlled Janes vpf-475 cryostat, which enables us to make measurements in the temperature range of 77–450 K. The sample temperature was always monitored by using a copper-constantan thermocouple close to the sample and measured with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers with sensitivity better than ±0.1 K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

According to the thermionic emission (TE) theory for a MIS Schottky diode with series resistance (R_s), the relation between an applied forward bias and current can be expressed as [22,23]

$$I = I_o \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \quad (1)$$

where the IR_s term is the voltage drop across the R_s of structure, I_o is the saturation current derived from the ln(I)–V plot as the straight line intercept of the ln(I) axis at zero bias, V is the applied voltage across to rectifier contact, n is the ideality factor, T is the absolute temperature in K, q is the electronic charge and k is the Boltzmann constant. Due to the existence of the R_s, significant voltage drop is observed at large forward currents. In this case, the ln(I)–V plot deviates from a straight line at high forward bias. The ideality factor n is introduced to calculate the deviation of the experimental I–V data from the ideal thermionic model, and the value of ideality factor should be unity for an ideal contact. The saturation current I_o is given by

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

where A is the diode area, A^* is the effective Richardson constant of 112 A cm^{-2} K^{-2} for n-type Si [23] and Φ_{Bo} ($kT/q \ln[AA^*T^2/I_o]$) is the zero-bias barrier height. The ideality factor is a measure of the conformity of the diode current to be pure thermionic emission, and it is calculated from the slope of the linear region of the forward bias ln(I)–V plot according to Eq. (1):

$$n = \frac{q}{kT}\frac{d(V - IR_s)}{d(\ln I)} \quad (3a)$$

where $d(V - IR_s)/d(\ln I)$ is the slope of linear region of ln(I)–V plots. In addition, voltage dependent ideality factor $n(V)$ can be written from Eq. (1) as

$$n(V) = \frac{q(V - IR_s)}{kT \ln(I/I_o)} \quad (3b)$$

Fig. 1 shows the forward and reverse bias semi-logarithmic current–voltage characteristics of the MIS Schottky diode, measured as a function of temperature. As seen in Fig. 1, the I–V plots shift towards the higher bias side with decreasing temperature. The I–V characteristic of the MIS Schottky diode shows a good rectifying behavior with relatively low leakage current of 7×10^{-4} A at reverse bias of $V_R = -2$ V at 300 K. The current curve in forward bias becomes quickly dominated by series resistance from contact wires or bulk resistance of the semiconductor, giving rise to the curvature at high current in the semi-logarithmic ln(I)–V plot.

The saturation current I_o was obtained by extrapolating the linear intermediate voltage region of the linear part of the curve to a zero applied bias voltage for each temperature. The experimental values of the barrier height (Φ_{Bo}) and the ideality factor (n) for the Schottky diode were determined from intercepts and slopes of the forward bias ln I vs. V plot at each temperature. The values of n and Φ_{Bo} were obtained from Eqs. (2) and (3a), and are presented in Fig. 2 and Table 1, respectively. Both parameters depend strongly on temperature. This feature can be connected either with the lateral inhomogeneity of barrier height or with the domination of the current with thermionic field emission [13]. The experimental values of Φ_{Bo} and n for the MIS Schottky diode are changed from 0.63 eV and 2.90 at 300 K to 0.80 eV and 1.79 at 400 K, respectively. The barrier height calculated from forward bias I–V characteristics shows an unusual behavior that increases with the increase of temperature. Such temperature dependence is an obvious disagreement

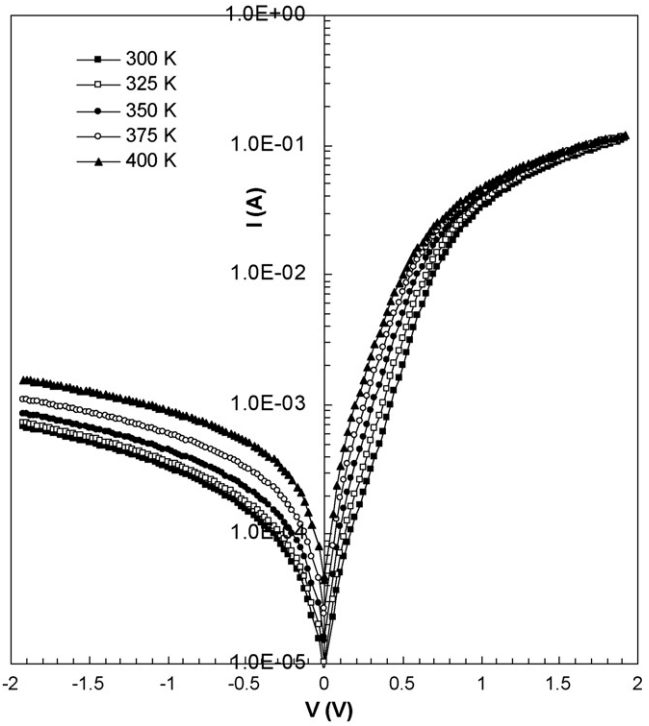

Fig. 1. Forward and reverse bias semi-logarithmic current–voltage characteristics of the MIS Schottky diode as a function of temperature.

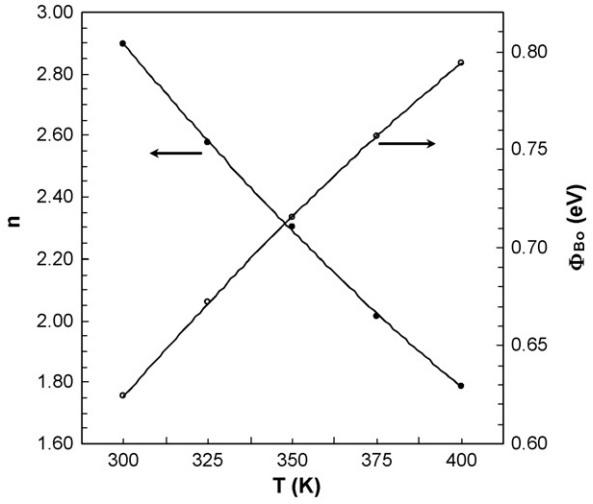

Fig. 2. Temperature dependence of ideality factor and barrier height for the MIS Schottky diode.

Table 1
Temperature dependence of various parameters determined from forward bias *I–V* characteristics of Au/SiO_2/n-Si (MIS) Schottky diode.

Temperature (K)	R_s ($dV/d\ln(I)$) (Ω)	R_s ($H(I)$) (Ω)	N_{ss} (eV^{-1} cm^{-2})
300	11.59	10.79	7.92×10^{12}
325	12.58	10.92	6.56×10^{12}
350	12.55	10.99	5.40×10^{12}
375	12.35	11.29	4.18×10^{12}
400	12.61	11.67	3.22×10^{12}

with the reported negative temperature coefficient of the barrier height obtained from reverse bias capacitance–voltage measurements. Also, the ideality factor is not constant with temperature and decreased with increasing temperature. Such behavior of an ideality factor has been attributed to particular distribution of interface states and insulator layer (SiO_2) between metal and semiconductor [1,24–27].

As explained in Refs. [2,5,16,17,24,26–28], since the current transport across the metal–semiconductor interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers. In other words, more and more electrons have sufficient energy to overcome the higher barrier build up with increasing temperature and bias voltage. Therefore, the current transport will be dominated by the current flowing through the patches of lower Schottky barrier height, leading to a larger ideality factor.

The interface states for electrons or holes must not necessarily introduce energy levels in the band gap; i.e., only the density of states in the valence and conduction bands may be affected. The non-linearity of *I–V* characteristics of the MIS structure at high bias indicates a continuum of interface states, which are in equilibrium with the semiconductor [1]. Nevertheless, the structures exhibit excellent rectification characteristics with a relatively low leakage current density. The effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and interface states located at the Si/SiO_2 interface. The applied voltage dependence of the barrier height can be written as

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n(V)} \tag{4}$$

where β is the voltage coefficient of the effective barrier height Φ_e and is given by [1,3,28,29]

$$\Phi_e = \Phi_{Bo} + \beta(V - IR_s) = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{5}$$

For MIS Schottky diodes having interface states N_{ss} in equilibrium with semiconductor, the ideality factor becomes greater than unity and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{6}$$

where W_D is the space charge region width, δ is the thickness of interfacial insulator layer, ε_i and ε_s are the permittivity of the insulator layer and the semiconductor, respectively. This expression of voltage dependent ideality factor is identical to Eq. (18) of Card and Rhoderick [1]. The expression for the interface state density as deduced by Card and Schroder [1,30] is reduced to [22,31]

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{7}$$

The values of δ and W_D are obtained from high frequency (1 MHz) *C–V* characteristics (not given here) using the equation for insulator layer capacitance ($C_{ox} = \varepsilon_i\varepsilon_o A/\delta$). Furthermore, in n-type semiconductors, the energy of interface states E_{ss} with respect to the bottom of the conduction band, E_c, at the surface of semiconductor, is given by [1,3,32]

$$E_c - E_{ss} = q(\Phi_e - V) \tag{8}$$

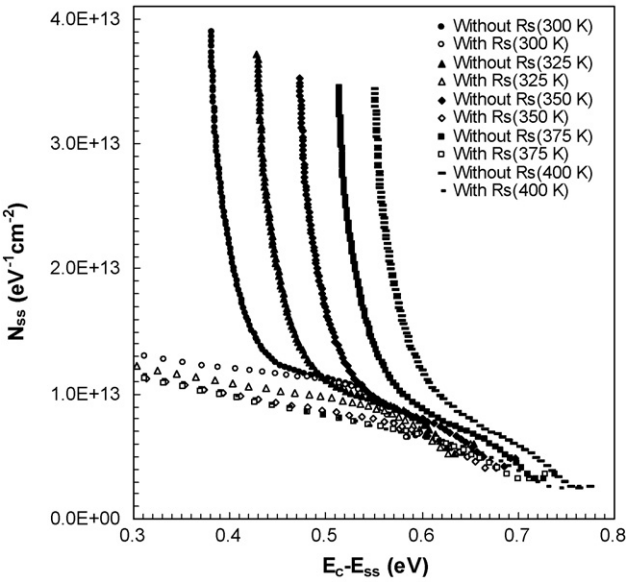

Fig. 3. The density of interface states (N_{ss}) as a function E_c–E_{ss} obtained from the forward bias *I–V* data at various temperatures for the MIS Schottky diode.

For each temperature, using the values of the voltage dependence of $n(V)$ obtained from the experimental forward bias *I–V* data in Fig. 1 and taking $\delta = 50$ Å, $\varepsilon_i = 3.8\varepsilon_o$, $\varepsilon_s = 11.8\varepsilon_o$ [23,33], the values of interface states N_{ss} were obtained from Eq. (7) as a function of (E_c–E_{ss}) and are plotted in Fig. 3.

Fig. 3 shows the density of interface states (N_{ss}) distribution profiles as a function E_c–E_{ss} for each temperature, extracted from the forward bias *I–V* characteristics taking into account both the bias dependence of the effective barrier height and with and without R_s obtained from the forward bias *I–V* characteristics of the MIS Schottky diode. We have observed that the values of N_{ss} increase with decreasing temperature. As can be seen in Fig. 3, the increase in the N_{ss} from the mid-gap towards the bottom of the conduction band is very apparent. Similar results have been reported in the literature [4,9,17,26,34].

As seen in Fig. 3, the magnitude of the N_{ss} with and without the R_s at E_c 0.41 (eV) has changed in the range from 2.42×10^{13} to 1.19×10^{13} eV^{-1} cm^{-2} (300 K), and at E_c 0.56 (eV) it has changed in the range from 2.84×10^{13} to 7.21×10^{12} eV^{-1} cm^{-2} (400 K). The values of N_{ss} obtained by taking the R_s values into account are lower than those of without the R_s, particularly near the conductance band. The above explanations clearly show that the R_s value should be taken into account in determining the interface state density distribution profiles. Similar results have been reported in the literature [17,35,36]. Aydın et al. [36] explained the importance of the fact that the neutral-region resistance value is considered in calculating the N_{ss} distribution from the non-ideal forward bias *I–V* characteristics. Also, Hudait and Krupanidhi [17] researched the effect of insulator layer on same electronic parameters such as ideality factor, reverse saturation current and interface states of MS and MIS structures. They found that the value of N_{ss} in MIS structure is lower than MS structure.

The series resistance is a very important parameter of MIS Schottky diode. The resistance of the Schottky diode is the sum total resistance value of the resistors in series and resistance in semiconductor device in the direction of current flow. Therefore, the series resistances were evaluated from the forward bias *I–V* data using methods developed by Cheung and Cheung [37]. The forward

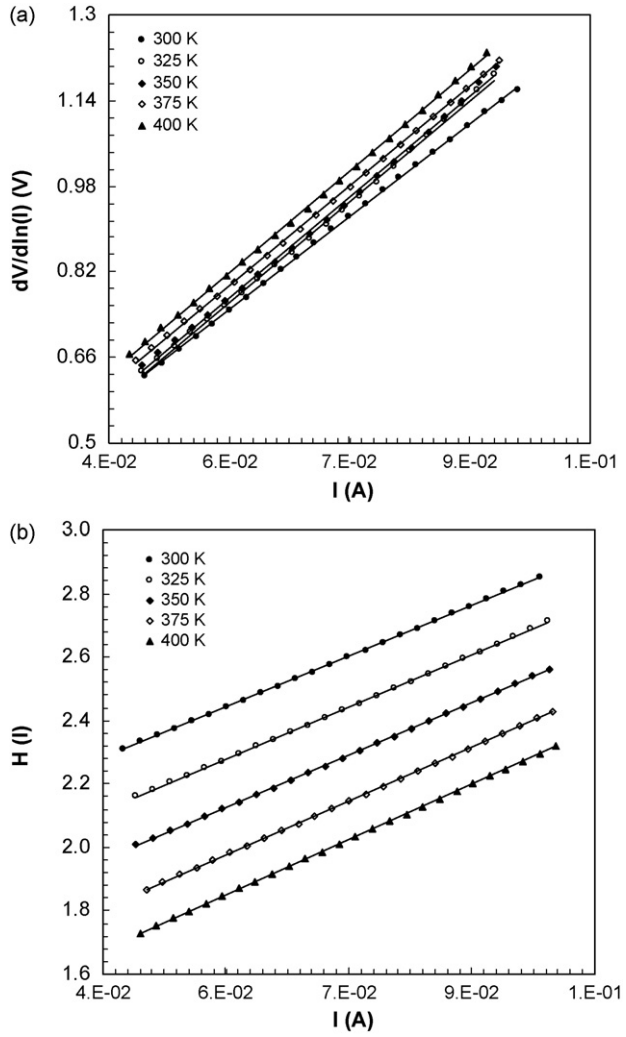

Fig. 4. The characteristics of the MIS Schottky diode obtained from the forward bias *I–V* data at various temperatures: (a) $dV/d\ln(I)$ vs. I and (b) $H(I)$ vs. I.

bias current–voltage characteristics due to thermionic emission of a Schottky contact with the series resistance can be expressed as [22,23] Cheung's functions:

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{9}$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ \ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_B + IR_s \tag{10}$$

These two equations should give a straight line for the data of downward curvature region in the forward bias *I–V* characteristics. In Fig. 4(a) and (b), experimental $H(I)$ vs. I and $dV/d\ln(I)$ vs. I plots are presented at different temperatures for MIS Schottky diode, respectively. Eq. (9) should give straight line for the data of downward curvature region in the forward bias *I–V* characteristics. Thus, a plot of $dV/d\ln(I)$ vs. I will give R_s as the slope and $n(kT/q)$ as the y-axis intercept. As a function of temperature, the values of n (obtained from plots $H(I)$ vs. I and $dV/d\ln(I)$) and R_s derived from Fig. 4(a) and (b) are given in Table 1. Using the n value determined from Eq. (10), a plot of $H(I)$ vs. I will also give a straight line (as shown in Fig. 4(a)) with y-axis intercept equal to $n\Phi_B$. The slope of these plots also provides a second determination of R_s, which can be used to check the consistency of Cheung's approach. As can be seen in Table 1, the values of R_s obtained from $dV/d\ln(I)$–I and $H(I)$–I plots are in good agreement with each other [9,26,38]. Also, the difference in the values of ideality factor obtained from Eqs. (3a) and (9) is an effect of existence of series resistance, thickness of interfacial layer and the presence of interface states [39]. The last two factors affect the Schottky barrier height, which also depends on the applied bias (throughout reloading processes of interface states).

4. Conclusion

In this study, we have investigated the temperature-dependent *I–V* characteristics of the MIS Schottky diode in the temperature range of 300–400 K. Based on the thermionic emission (TE) theory, the *I–V* characteristics of the Schottky diode have been explained. The barrier heights (Φ_{Bo}) and ideality factor (n) obtained from *I–V* are in the range of 0.63–0.80 eV and 2.90–1.79, respectively. The calculated ideality factor and barrier height shows strong dependence on temperature. The decrease in ideality factor and increase in barrier height with increase in temperature may be attributed to spatial variations of the barrier height at the interface. Also, the value of the series resistance (R_s) has been calculated from high voltage region of the structure by using Cheung functions. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. In summary, in the present study, we conclude that the prepared MIS Schottky diodes have been controlled by the interfacial layers, interface states and series resistance, which are responsible for the non-ideal behavior of *I–V* characteristics.

Acknowledgments

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