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Temperature-dependent barrier height in CdSe Schottky diode

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Abstract This article reports the measurements of temperature-dependent barrier height (BH) of CdSe Schottky diodes. These diodes have been made by thermal evaporation technique on ITO glass and glass substrates at room temperature. The XRD measurements have been made and the average particle size has been calculated which comes out to be ~20 nm. The Au dots have been made for non-ohmic contacts. *I–V* characteristics have been measured at different temperatures (280–330 K). These characteristics obey the thermionic emission theory. The BH decreases and ideality factor increases with the increase in temperature. Richardson's plot has been made and Richardson's constant has been calculated which is less than the expected value. Capacitance measurements have been done at different frequencies and the interface states have been calculated. The results have been explained on the basis of BH inhomogeneities.

Introduction

The synthesis of binary metal chalcogenides of groups II–VI semiconductors in a nanocrystalline form is a rapidly growing area of research due to their important nonlinear optical properties, luminescent properties, quantum-size effect, and other important physical and chemical properties [1, 2]. In this group, cadmium selenide is a widely used semiconductor whose band gap lies in the solar energy spectrum. CdSe has been studied intensively in recent years because of its potential use as a photoanode in photoelectrochemical cells, gas sensors, solar cells, etc. [3–6].

Schottky barrier diodes (SBD) are of the most simple of metal–semiconductor (MS) contact devices [7, 8]. Although Schottky interfaces have been well studied for over 50 years, it is only in the past decade that inhomogeneous contact has been considered as an explanation for voltage-dependent barrier height (BH) [9–11]. The BH is likely to be a function of the interface atomic structure, and the atomic inhomogeneities at an MS interface which are caused by grain boundaries, multiple phases, facets, defects, a mixture of different phases, etc. [9, 10]. The nonideal behavior in the SBD could be quantitatively explained by assuming specific distribution of nanometer-scale interfacial patches (small regions) with lower BH than the junction's main BH [12]. In such cases, the current across the MS contact may be greatly influenced by the presence of the BH inhomogeneity [11, 12]. Some authors have been able to account for much of the observed non-ideal behavior by assuming certain distributions of microscopic BHs for the different diodes [13–15].

Measurements of current–voltage (*I–V*) of Schottky barrier, only at room temperature, do not give satisfactory information about the conduction process and the nature of barrier formation at the MS interface. However, the temperature dependence of the *I–V* characteristics allows to understand different aspects of conduction mechanisms. The Schottky barriers with low BH have found applications in devices operating at cryogenic temperatures as infrared detectors and sensors in thermal imaging [13, 16–18]. Thermionic emission (TE) theory is widely used to extract the SBD parameters [16–18]. Some authors have also stressed [13, 16] the importance of BH inhomogeneities over the MS contact. The nature and origin of the temperature dependence of BH have been successfully

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explained on the basis of a TE mechanism with Gaussian distribution of BHs by some authors [16–18]. Simulation studies on *I–V* characteristics of inhomogeneous diodes with a Gaussian distribution have also yielded results similar to those observed in experimental data [19].

So, the homogeneity or uniformity of the Schottky BH is an issue with important implications on the theory of Schottky BH formation and important ramifications for the operation of SBD and contacts. The devices are produced to show the ability of employing CdSe as a candidate in semiconductor device production. In this study, the *I–V* characteristics of Au Schottky contacts on CdSe films on ITO substrate are measured over the temperature range 280–330 K. These characteristics will be discussed and analyzed to show the ability of obtaining the rectifying properties of these structures to be used as Schottky diodes. The capacitance measurements have also been made at different frequencies (1–400 kHz). The following section describes the experimental part. Results are presented and discussed in the "Results and discussion" section. Last section deals the conclusion of this study.

Experimental

The semiconducting $Cd_{30}Se_{70}$ alloy is prepared from its constituents (5 N pure) by melt-quenching technique as described earlier [20]. Thin films of this material are prepared in a conventional vacuum coating system on well-degassed ITO-coated glass substrates. These substrates have been heated at 380 K to remove any moisture or methanol present. The vacuum chamber is evacuated to 2×10^{-4} Pa. Thermal evaporation of the material is carried out from the Mo boat. The distance between the source and the substrate is about 7 cm. Crystallographic study is carried out using a Phillips PW-1610 X-ray diffractometer using Cu K_α radiation in the 2θ range from 10° to 70°. Thin film of gold (thickness $\sim$100 nm) is deposited for making the nonohmic contact onto the CdSe thin film. The area of the Schottky diode is $\sim 3.14 \times 10^{-3}$ cm^{-2}. *I–V* measurements are performed using a high impedance electrometer (Keithley 614) and a dc voltage source. The capacitance measurements at different frequencies are carried out with a digital LCR bridge. The temperature dependence of *I–V* measurements has been done in the temperature range 280–330 K.

Results and discussion

XRD pattern of CdSe film deposited on the glass substrates at room temperature has been made. The spectrum (figure not shown) shows a single diffraction peak at 2θ value of 25.3°. The comparison of observed '*d*' values with standard '*d*' values [111] confirms the sphalerite cubic (zinc blende type) nanocrystalline structure of CdSe thin films. The particle size has been calculated using Scherrer's relation:

$$\beta = k\lambda/D \cos\theta \quad (1)$$

where β is the full width at half maximum (FWHM) and D is the diameter of the particles. The average particle size is found to be $\sim$20 nm. Aneva et al. [2] have also deposited the thin films of CdSe of different thicknesses (50–100 nm) by thermal evaporation technique. They have studied the structure of these films by AFM technique.

According to the SBD theory, the relationship between current and voltage is given by [21]:

$$I = I_0 \exp(qV/nkT)\,[1 - \exp(-qV/kT)] \quad (2)$$

here

$$I_0 = AA^{**}T^2 \exp[-q\Phi_{B0}/kT] \quad (3)$$

where I_0 is the saturation current obtained from the straight line intercept of ln *I–V*, plot at $V = 0$, V is the forward-bias voltage, k is the Boltzmann constant, q is the electronic charge, A is the effective diode area, T is the absolute temperature, A^{**} is the effective Richardson constant, Φ_{B0} is the BH, and n is ideality factor. The ideality factor n is defined as the deviation of the experimental *I–V* data from the ideal TE diffusion model as given below

$$n = (q/kT)[dV/d(\ln I)] \quad (4)$$

Figure 1 shows the forward *I–V* plots of ITO/CdSe/Au SBD in the temperature range 280–330 K. In the case of best rectifying system, ITO/CdSe/Au, which I took into consideration for the rest of the analysis, the device is forward biased when the ITO side is made positive with

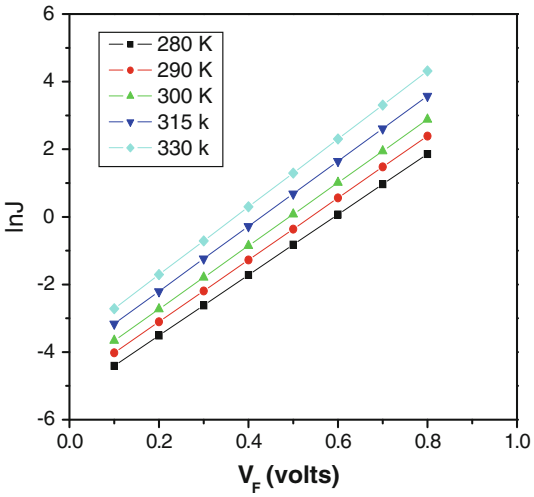

Fig. 1 The current density (J) versus forward bias voltage (V_F) at different temperatures

respect to the Au electrode. The barrier is a typical Schottky barrier, formed when electrons are transferred from the metal to the semiconductor. At the equilibrium, the current flows in both the directions, i.e., from metal-to-semiconductor and vice versa. For the Schottky diodes operated at moderate temperature (e.g., 300 K), the dominant transport mechanism is TE of majority carrier from semiconductor over the potential barrier into the metal. At the semiconductor surface, carriers may recombine with the recombination centers due to dangling bonds of the surface region. Thus, I may suggest a potential barrier at the interface. The experimental values of n and Φ_{B0} have been obtained from intercepts and slopes of the forward bias plots at each temperature, respectively.

Figure 2 shows the plots between the zero-bias BHs (Φ_{B0}) at different temperatures. It is clear from the figure that the value of Φ_{B0} increases with the increase in temperature. The value of n decreases as the temperature increases. These changes are indicative of deviations from the pure thermionic mechanism as explained by other workers [22, 23]. Such temperature dependence is in obvious disagreement with the reported negative temperature coefficient of the Schottky BH. Since the current transport across the metal–semiconductor interface is a temperature-activated process, electrons are able to surmount the lower barriers. Therefore, the current flow through the lower SBH and a larger ideality factor will dominate current transport. In other words, more electrons have sufficient energy to overcome the higher barrier when the BH builds up with increasing temperature and bias voltage.

Figure 3 shows the activation energy plot, $\ln(J_s/T^2)$ versus $1000/T$ of the forward bias ITO/CdSe/Au Schottky diode. It is clear from the figure that the plot is a straightline and the value of the Richardson constant, A^{**},

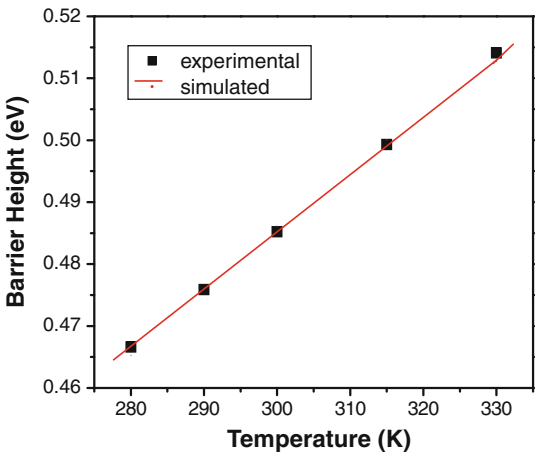

Fig. 2 The BH versus temperature; *solid lines* are obtained by simulating the data as discussed in the text

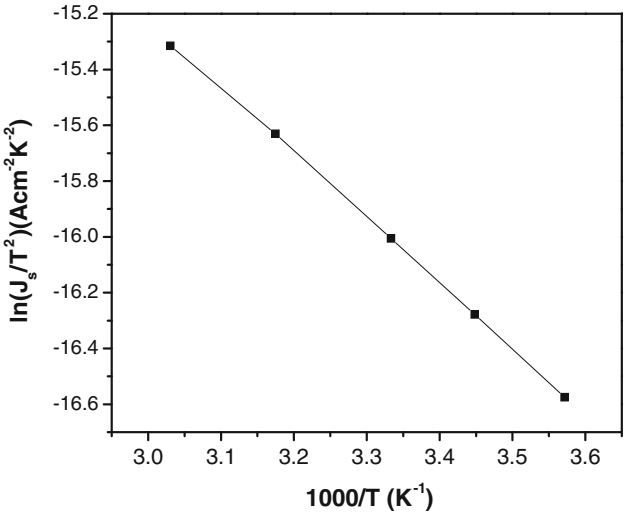

Fig. 3 The plot of $\ln(J/T^2)$ versus $1000/T$

is found to be $\sim 2.66 \times 10^{-4}$ A cm^{-2} K^{-2}. This value is lower by four times than the known value of 15.6 A cm^{-2} K^{-2} [24]. This variation on the value of Richardson's constant may be due to the spatial inhomogeneous BHs and potential fluctuations at the interface and consist of low and high barrier areas [25]. In other words, the current of the diode will flow preferentially through the lower barrier in the potential distribution. The A^{**} value obtained from the temperature dependence of the I–V characteristics may be affected by the lateral inhomogeneity of the barrier.

An alternative method has been suggested by the Tung [13]. He has shown that the lateral inhomogeneities are found in the Schottky barrier interfaces. The Schottky barriers consist of laterally inhomogeneous patches of different BHs. Larger ideality factor is obtained due to the patches of lower BHs and vice versa. Schmitsdorf et al. [16] using Tungs' [25] theoretical approach have found a linear correlation between the experimental zero-bias SBHs and ideality factors. So, a graph has been plotted between the BHs and the ideality factor (see Fig. 4) in the measured temperature range (280–330 K). It is clear from the figure that these two values are correlated linearly with each other and thus justify the lateral inhomogeneities in the Schottky barrier area. Φ_{B0} is calculated theoretically as suggested by Chand and Kumar [26] at different temperatures and shown in Fig. 2 with solid line which matches well with the experimental results.

Figure 5 shows the variation of capacitance with frequency at the zero bias. It is clear from the figure that the variation of capacitance with frequency at low frequency is stronger than at higher frequencies. The variation at low and high frequencies is due to the presence of interface states at the Schottky junction.

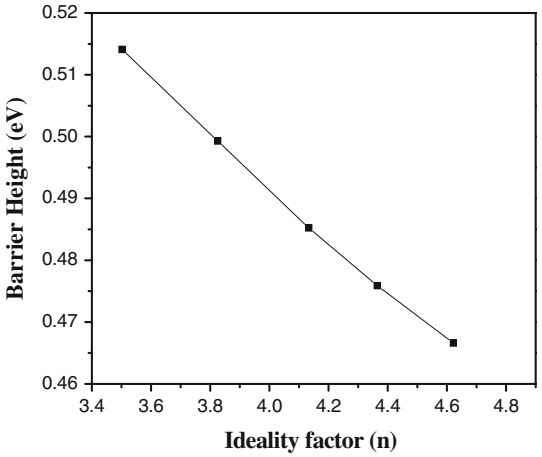

Fig. 4 Plot between the BH and the ideality factor

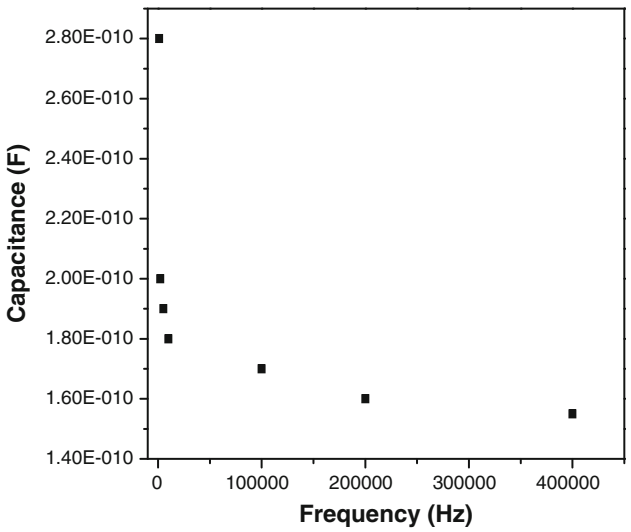

Fig. 5 Variation of capacitance with frequency at zero bias

The number of interface states (N) can be estimated by using the following relation:

$$N = \left(C_{\text{low}} - C_{\text{high}}\right)/q \tag{5}$$

where C_{low} and C_{high} denote the low and high frequency capacitance values, respectively. At the zero bias and room temperature, the number of interface states is calculated from the above equation and is found to be $\sim 7.8 \times 10^8$ cm^{-2} V^{-1}.

Conclusions

Thin films of nanocrystalline CdSe have been deposited on glass and ITO substrates. The average particle size has been calculated using XRD technique. The forward bias I–V characteristics of ITO/CdSe/Au Schottky barrier have been measured in the temperature range 280–330 K. The value of Φ_{B0} decreases and the value of n increases with the decrease in temperature. BH inhomogeneities at the interface cause the deviation in Φ_{B0} and n and produce an additional current such that the I–V characteristics continue to remain consistent with the TE process. The number of interface states (N) has been calculated using measured frequency dependence capacitance values. The value of the band gap has been calculated from the spectral response of the diode. The inhomogeneities can be described by the Gaussian distribution of the BHs.

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