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Low-voltage driven I–V hysteresis loop in Ag/$SrTiO_3$/Si heterostructure

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ABSTRACT

Hysteresis loop is a vital feature in the study of electronic devices, like ferroelectric hysteresis loop in ferroelectric devices, magnetic hysteresis loop in spin-electronic devices, and current–voltage (I–V) loop in memristors. Here, we report a type of I–V loop observed in the Ag/$SrTiO_3$/Si structure, which can be dynamically varied by purely electrical modulation. This phenomenon can be attributed to the capacitive effect based on the resistance–capacitance circuit model. Additionally, we further explore the carrier transport mechanism by establishing different modulation methods of I–V hysteresis loops. This work expands our understanding of the behavior of electronic devices.

In physics, hysteresis character refers to the phenomenon where, it cannot retrace the exact path after dual-direction scanning by an external field. Classical hysteresis loops can be traced back to the control of magnetization (M) and polarization (P) by magnetic field (H) and electric field (E),[1–5] known as M–H loops and P–E loops. M–H loops offer potential applications in spin-electronic devices like magnetic sensors and memories.[6,7] Meanwhile, P–E loops hold promise for ferroelectric memories, piezoelectric devices, and ferroelectric photovoltaics.[8–11] Recently, the current-voltage (I–V) hysteresis loop has emerged as a promising property that has attracted significant interest in information technology, particularly for data storage and brain-inspired computing applications.[12–14] However, I–V hysteresis loops are mostly discussed in memristors based on the coupling of ion-migration effects and redox processes.[15–18] In addition, other studies done on I–V loops, such as transistor-based memories,[19,20] are pseudo I–V loops since the applied gate-voltage and detected drain current directions are perpendicular. Thus, discovering and uncovering such I–V loops in more systems is of fundamental interest to physics research, providing a deeper understanding of the carrier transport mechanism of electronic devices.

Recently, researchers have developed an organic memory device based on the I–V loop that can be used for data storage and logic operations.[21] In their study, the I–V loop of the device relies on specific organic chemical reactions, and its mechanism is relatively complex and lacks universality. However, we observe an I–V loop phenomenon with a more well-defined mechanism. In this work, we investigate the I–V hysteresis loops observed in Ag/$SrTiO_3$ (STO)/Si structures, showing tunable windows based on capacitive effect. Interestingly, the resistance-capacitance (RC) circuit model is established to reveal the dynamic carrier transport process by employing various sweeping methods. Compared with similar works, we focus more on the physical process itself, hoping to provide a clearer and more reliable physical picture for the further study of the I–V loop.

The structure of Ag/STO (or MoS_2, HfO_2, TiO_2)/Si is synthesized by a bottom-up approach. The n-type single-crystal Si (111) wafers (approximately 0.3 mm thick, 50–70 cm Ω resistivity) are used as substrates. The STO, MoS_2, HfO_2, and TiO_2 films are fabricated by radio frequency (RF) magnetron sputtering under 50 W sputtering power. Ag electrodes are fabricated by direct current (DC) magnetron sputtering under 20 W sputtering power. An argon gas pressure of 0.7 Pa is maintained during deposition. The deposition rates, determined by a stylus profile meter on thick calibration samples, are 0.03 nm/s (STO), 0.02 nm/s (MoS_2), 0.01 nm/s (HfO_2), 0.01 nm/s (TiO_2), and 0.59 nm/s (Ag).

The cross-sectional image of Ag/STO/Si structure is measured by scanning electron microscope (SEM, ZEISS GeminiSEM 300). The surface morphology of the STO/Si structure is measured using an atomic force microscope (MFP-3D). Electrical measurements are carried out using a Keithley 4200-SCS Parameter Analyzer and a Lake Shore Cryotronics TTPX probe station at room temperature. The testing voltages are applied to the Ag electrodes, ensuring the Si substrates remain consistently grounded.

Figure 1(a) presents a schematic diagram of the Ag/STO/Si structure, in which the STO layer plays the pivotal role in the observed effect. Figure 1(b) is the surface topography of STO film characterized by atomic force microscope (AFM), exhibiting atomically flat surfaces with a root mean square roughness of approximately 0.349 nm over an area of $5 \times 5\ \mu m^2$. Additionally, the cross-sectional image of Ag/STO/Si structure is also produced by scanning electron microscope (SEM), as shown in the inset of Fig. 1(b). The thickness of the STO layer is found to be around 20 nm.

Initially, we discuss the I–V characteristics of the Ag/STO/Si structure. It displays a hysteresis window characteristic at low sweep voltage (−0.3–0.3 V, then back to −0.3 V), as illustrated in Fig. 2(a). Notably, From B to C, the device exhibits a positive current even when the applied voltage is negative. However, a typical rectification effect instead of the hysteresis window is observed when the sweep voltage is raised to 2.0 V, as shown in the inset of Fig. 2(a). This means that the rectification characteristics will gradually mask the hysteresis characteristics as the sweep voltage gradually rises. The 210 cycles of the device under low sweep voltage are shown in Fig. 2(b), demonstrating the repeatability of the device performance.

We first provide a qualitative understanding of the hysteresis loop based on this hypothesis, and the specific evidence and quantitative analysis of this capacitive effect will be discussed later. In Fig. 2(a), point A is the starting point of the sweep voltage. A certain amount of charge is instantly injected into the capacitor at point A. Then, during the process from A to B, as shown in Fig. 2(c), capacitor voltage U_C increases as the charging quantity increases, approaching the gradually decreasing sweep voltage U_S, resulting in a rapidly decreasing current. However, during this process, U_C is always smaller than U_S, so the current direction is consistent with the sweep voltage direction. When U_C is equal to U_S, as shown in Fig. 2(d), there is no current (point B). Subsequently, as the sweep voltage continues to decrease, the capacitor begins to discharge, resulting in a current direction that is opposite to the sweep voltage, as shown in Fig. 2(e) corresponding to the process of B to C. As the sweep voltage increases from C to D, the capacitor begins to recharge, resulting in a current that is aligned with the direction of the sweep voltage, as shown in Fig. 2(f). The analysis of the reverse process (D to A) is similar, thus forming a hysteresis loop that is symmetric about the origin of coordinates.

To verify the reliability of the above mechanism, several sets of control experiments are carried out, as shown in Fig. 3. By replacing the top electrode Ag with Pt, it is found that the hysteresis phenomenon still exists, as shown in Fig. 3(a). This indicates that the electrode has almost no influence on the hysteresis phenomenon, and the slight change of I–V curve comes from the difference in metal work function. Specifically, Pt has a slightly higher work function than Ag,[22,23] resulting in a larger interfacial barrier at the Pt/STO interface and a correspondingly smaller hysteresis loop. When the STO film is replaced with TiO_2 film, the hysteresis phenomenon of the device is weakened, as shown in Fig. 3(b). Furthermore, when HfO_2 and MoS_2 are used, the direct rectification characteristics without hysteresis window are displayed, as shown in Figs. 3(c) and 3(d). At room temperature, the permittivity (ε_r) of STO is usually in the hundreds or even thousands.[24–26] The permittivity of TiO_2 is around 100.[27–29] However, the permittivity of HfO_2 is usually in the tens[30–32] and that of MoS_2 usually does not exceed 10.[33–35] It is easy to observe that, as the permittivity of the material decreases, the I–V loop phenomenon gradually weakens and eventually vanishes. Therefore, we suppose that the permittivity of the dielectric material plays a key role in shaping the I–V hysteresis loops, according to the equation $C = \frac{\varepsilon_0 \varepsilon_r S}{d}$. More directly, the I–V loop depends on the non-steady-state charging and discharging process.

The voltage of the capacitor is always different from the sweep voltage, leading to hysteresis behavior. Because in addition to the capacitance effect, there are also loads such as barriers and the resistance of the material itself. Therefore, the overall electrical structure can be equivalent to a RC circuit as shown in Fig. 4(a). In the RC circuit, the change in capacitance voltage often lags the applied bias voltage. The hysteresis characteristics we measured are obtained by continuously varying the applied bias voltage, resulting in a non-steady-state current. Based on Kirchhoff's theorem, the relationship among the external bias U_S, the capacitor voltage U_C, and the equivalent resistance R of the device can be derived,

$$RC\frac{dU_C}{dt} + U_C = U_S. \tag{1}$$

Under the initial condition of $t = 0$, $U_C = 0$, we can obtain the following:

$$U_C = U_S(1 - e^{-\frac{t}{RC}}). \tag{2}$$

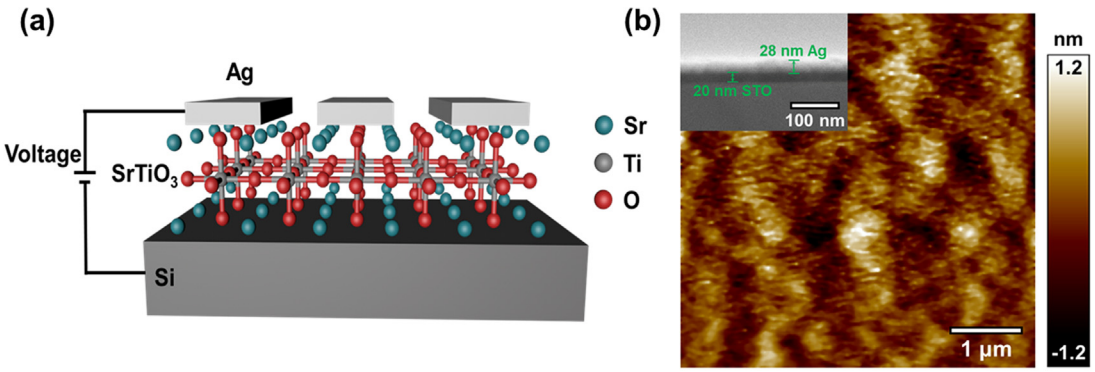

FIG. 1. (a) Schematic of the Ag/STO/Si structure. (b) AFM image of the surface morphology of STO thin film. The inset is the cross-sectional SEM image of Ag/STO/Si structure.

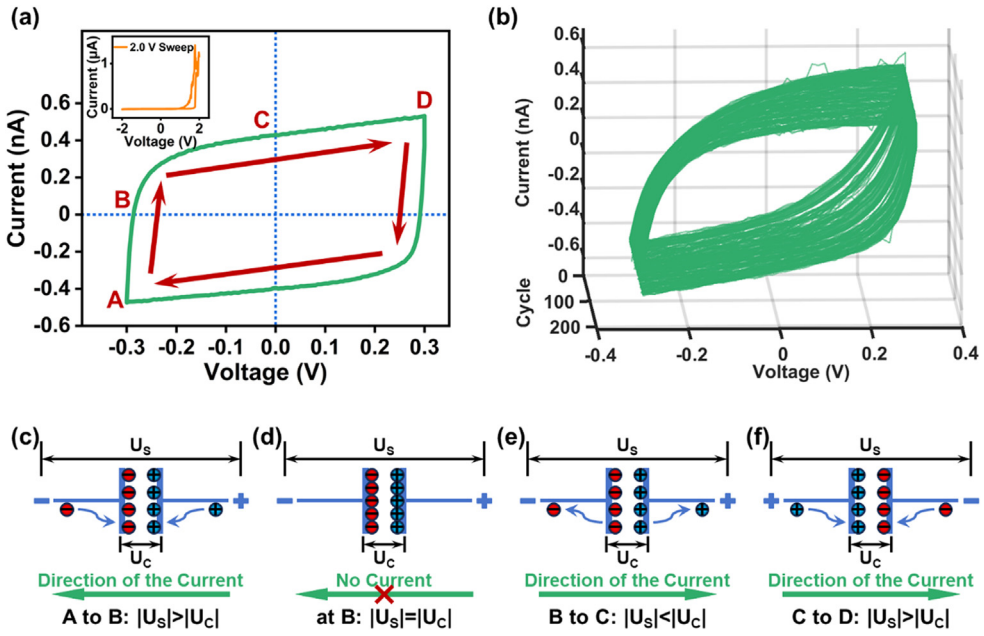

FIG. 2. (a) Current–Voltage (I–V) curves of Ag/STO/Si structure with the dual voltage sweeping from −0.3 to 0.3 V. The inset is the rectification effect with the voltage sweeping from −2.0 to 2.0 V. (b) The I–V curves of Ag/STO/Si structure for 210 cycles. (c)–(f) The mechanism diagrams of the hysteresis loop in (a). Panel (c) corresponds to the process of A to B. Panel (d) corresponds to point B. Panel (e) corresponds to the process of B to C. Panel (f) corresponds to the process of C to D.

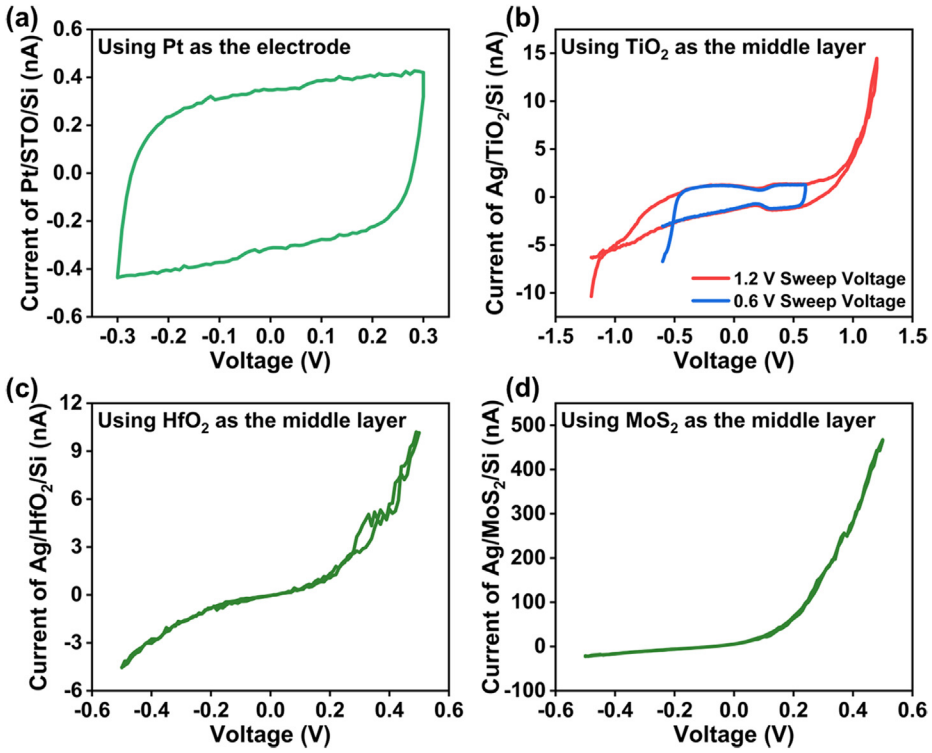

FIG. 3. (a) I–V curve of the Pt/STO/Si structure, verifying that the change of the electrode almost does not affect the effect. (b) I–V curves based on TiO_2, showing a slight hysteresis phenomenon. I–V curves based on (c) HfO_2 and (d) MoS_2, confirming no hysteresis phenomenon.

Here, $\tau = RC$ is defined as the time constant of this RC circuit. Equation (2) reflects the change in capacitor voltage during the charging process. Similarly, the situation during the discharging process is obtained as follows:

$$U_C = U_{C0}e^{-\frac{t}{RC}}. \tag{3}$$

If discharging begins at $t = 0$, U_{C0} represents the capacitor voltage at the exact start of discharging. Furthermore, the discharging current is derived as follows:

$$I = \frac{dQ}{dt} = \frac{CdU_C}{dt} = I_0 e^{-\frac{t}{RC}}. \tag{4}$$

Here, $I_0 = -\frac{CU_{C0}}{RC}$ is the discharging current at $t = 0$. Therefore, by monitoring the current changes during the discharging process of our device, we can calculate the corresponding time constant and further verify the correctness of the explanation of the hysteresis loop based on the RC model. Figure 4(b) illustrates the process of applying the sweep voltage to test the time constant of our device. Here, $t = 0$ means a transition from charging to discharging. Within 4 s, the sweep voltage is uniformly changed from 0 to 0.3 V to charge the capacitor. After that, the sweep voltage is removed, and a small voltage of 5 mV is used to monitor the current decay of the device. The corresponding current variations with the above-mentioned sweep voltage are shown in Fig. 4(c), where a clear exponential rise and a subsequent exponential decay in current can be observed, corresponding to the charging and discharging currents of the RC circuit respectively. In addition, based on the current variations during the discharging process, a fitting using Eq. (4) is performed, yielding a time constant of 46.9 ms for our device, as shown in the inset of Fig. 4(c).

By adjusting the thickness of the STO film, its capacitance and resistance can be changed, so that the influence of these two physical quantities on the hysteresis characteristics can be further investigated. The STO films with thicknesses of 5, 10, 20, and 40 nm are used to study the I–V hysteresis loops, as shown in Fig. 5(a). It shows that STO films with different thicknesses can exhibit a certain hysteresis phenomenon. However, as the thickness of the STO film increases, the current decreases to some extent, and the hysteresis loop relatively shrinks. The capacitance and resistance of these four devices with different STO thickness can be seen in Figs. 5(b) and 5(c). The capacitance of the devices is basically consistent when the STO thickness is 10, 20, or 40 nm. However, when the STO thickness is reduced to 5 nm, the capacitance of the device increases rapidly. It can be inferred that the capacitance of the structure mainly comes from the barrier capacitance generated between the STO film and the Si substrate. The resistance of the device gradually increases as the STO thickness increases, see Fig. 5. The corresponding time constants can be calculated from the capacitance and resistance of the devices, as shown in Fig. 5(d). The time constants of the four devices are basically at the same level, so all of them can show the hysteresis phenomenon in Fig. 5(a). Although the four devices exhibit comparable time constants, the thicker STO films possess higher resistance. Consequently, under an identical capacitor charging voltage, the current intensity during charging and discharging processes becomes inconsistent. Specifically, thicker films demonstrate a reduced overall current intensity.

To further reveal the carrier transport mechanism behind the I–V hysteresis loops based on the RC model, the various sweeping methods are employed to test the device, as shown in Fig. 6. A dual

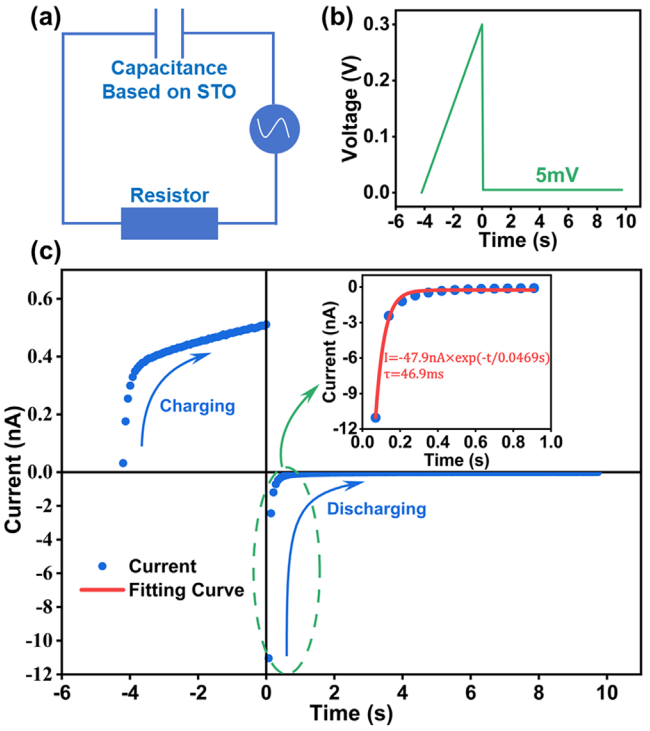

FIG. 4. (a) Equivalent Resistance–Capacitance (RC) circuit diagram of the Ag/STO/Si structure. (b) Diagram of the process of applying sweep voltage for testing the time constant of the device. (c) The current–time curves for the charging and discharging processes of the device, and the inset figure shows the fitting of the discharging process and the calculation of the time constant τ. The time is translated in (b) and (c) such that $t = 0$ corresponds to the instant of the transition from charging to discharging.

sweep test is conducted on the device within the voltage range of −0.3–0.3 V, and the sweep speed is gradually increased from 14.6 to 133.3 mV/s. The I–V response of the device is observed in Fig. 6(a). Under different sweep speeds, I–V hysteresis loops can be observed. As the sweep speed increases, the amplitude of the current also increases. A faster sweep speed means that the sweep voltage will change more rapidly in the same time interval. At this point, the capacitance of the device has not had enough time to reach a stable state in the recent short time interval, and the sweep voltage applied to it changes more drastically, resulting in a larger difference between the capacitor voltage and the sweep voltage. Consequently, more charging or discharging processes are carried out in the same time interval, leading to a higher current.

Figure 6(b) investigates the I–V hysteresis loop under the same sweep speed but with different voltage ranges. It can be observed that the initial current increases as the sweep range becomes larger. However, during the subsequent sweep process, the current quickly reaches a nearly consistent level. This is because the initially larger voltage triggers faster charging. When the subsequent sweep speed remains consistent, the difference between the capacitor voltage and the sweep voltage remains basically unchanged, resulting in the charging and discharging currents maintaining the same level.

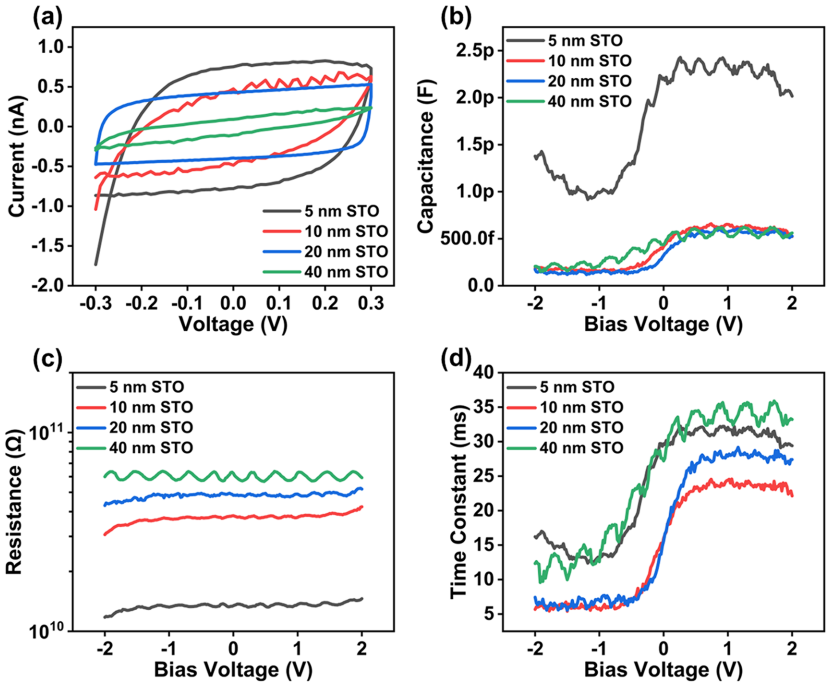

FIG. 5. (a) I–V loops, (b) C–V curves, and (c) R–V curves of Ag/STO/Si structures with different STO thickness. (d) The calculated time constant as a function of the bias voltage.

By investigating the relationship among the sweep speed, sweep range, and hysteresis loops, we can adjust the sweep speed at different sweep ranges to ensure that the starting and ending points of the sweep current coincide, thus forming a complete closed curve as shown in Fig. 6(c). This means that under the guidance of the RC model, the windows of the hysteresis loops can be freely adjusted. Additionally, we have also studied the I–V curves under the conditions of independently performing positive voltage sweeps and negative voltage sweeps, and compared with the dual sweep ranging from −0.3 to 0.3 V, as shown in Fig. 6(d). It can be observed that although

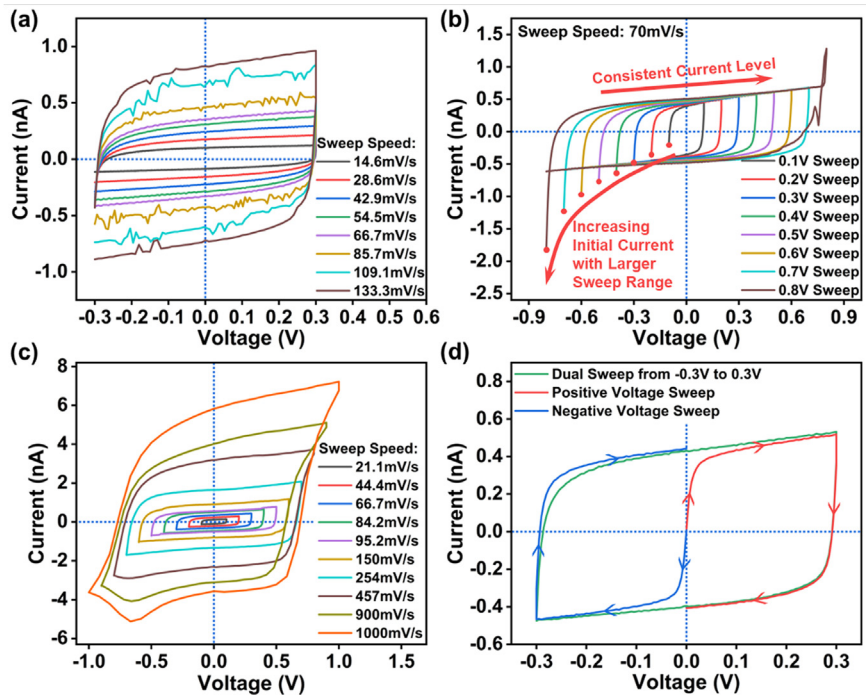

FIG. 6. (a) I–V loops under the same sweep range with different sweep speeds. (b) I–V loops under different sweep ranges with the same sweep speed. (c) I–V loops appear in the closed states by adjusting the sweep speed under different sweep ranges. (d) Comparison of I–V hysteresis loops between positive voltage sweep, negative voltage sweep, and dual sweep from −0.3 to 0.3 V.

the starting point of the sweep is different, the current quickly reaches a stable level consistent with the dual sweep from −0.3 to 0.3 V. This indicates that after experiencing a rapid charging process, the difference between the capacitor voltage and the sweep voltage reaches a relatively stable level, resulting in the same current level as that of dual sweep. The subsequent discharging process is also consistent with that under dual sweep, which is consistent with the proposed RC model. Therefore, as depicted in Fig. 6, we further understand the carrier transport mechanism behind the I–V hysteresis loops by various testing methods.

In conclusion, we have clearly demonstrated I–V hysteresis loops observed in Ag/STO/Si structure, which exhibits tunable windows under low-voltage driving. It can be attributed to the dynamic modulation of capacitive effect. Furthermore, the RC model is established to clarify this hysteresis effect, and the model is further confirmed by adjusting the sweep methods. This work provides a deeper understanding of the carrier transport mechanism of electronic devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors declare no conflicts of interest.

Author Contributions

Yuhong Cao and Kang'an Jiang contributed equally to this work.

Yuhong Cao: Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Kang'an Jiang:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Yuyang Zhang:** Investigation (equal); Validation (equal); Writing – review & editing (equal). **Dehui Huang:** Methodology (equal); Validation (equal); Visualization (equal). **Hui Wang:** Conceptualization (lead); Formal analysis (equal); Funding acquisition (lead); Project administration (lead); Supervision (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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