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Research

Improvement of Charge Minority-Carrier Lifetime in p*(Boron)-type Czochralski Silicon by Rapid Thermal Annealing*

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In* p*-type Czochralski-grown (Cz) silicon a light-induced degradation of the minority-carrier lifetime is well known in the literature. Reducing the extent of this degradation would significantly improve the stable effective lifetime and thus the related performance of solar cells. In this work, the reduction of the density of the metastable defect underlying the degradation is performed by rapid thermal annealing (RTA). For a proper analysis it is extremely important to avoid contamination by the RTA furnace. Both, SiN_x and SiO_2 were examined as a barrier layer. A 60 nm SiN_x layer was proven to act as the most effective barrier layer, allowing maintenance of a very high lifetime of 700 µs on 1·25 Ω cm* p*-type FZ material. A design-of-experiments (DOE) study was used to analyze the effect of five process parameters on the stable effective lifetime. Especially, the plateau temperature shows a strong correlation with τ_d, the stable effective lifetime after light-induced degradation. The effect of plateau temperature on τ_d of Cz- and FZ-Si wafers is examined in the temperature range of 700–1050°C for plateau time 120 s. It was found that the stable effective lifetime of all RTA-treated Cz-wafers is increased compared with the initial stable effective lifetime before processing. The highest increase of stable effective lifetime (by a factor of around 2) is obtained at 900°C with a process time of 120 s. This increase in lifetime is reflected in a reduced concentration of the metastable defect. Copyright © 2001 John Wiley & Sons, Ltd.

INTRODUCTION

Boron-doped *p*-type Cz-silicon, with its typical interstitial oxygen contamination, is used widely for the fabrication of electrical devices and solar cells because this type of material is more cost-effective than oxygen-free FZ-silicon. However, the lifetime of *p*(boron)-type Cz-silicon is significantly reduced, owing to illumination[1] or carrier injection.[2] The metastable defect underlying the degradation can be thermally

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deactivated by an annealing step at 200°C. From recent studies[3–5] it can be concluded that the metastable defect is correlated with boron and oxygen. In the case of conventional tube furnace processing it has been shown that the metastable defect concentration can be reduced, resulting in an increase of the stable effective lifetime. The stable effective lifetime is increased from initially 12·7 μs up to 54 μs by means of an optimized process at 1050°C, and is decreased to 0·8 μs if inappropriate process parameters are used.[6]

Rapid thermal processing has many advantages over conventional tube processing, such as low thermal budget due to very high heating and cooling rates, of the order of 100°C/s, and short process time. However, defects can be introduced during RTA by external contamination from the furnace, gas supply or sample surfaces, and by internal impurities such as the dopant, oxygen, carbon and other residual impurities, which can be activated during a high-temperature step and may stay active if high cooling rates are applied (i.e. quenching).[7,8] Eichhammer *et al.*[9] have shown that residual impurities play an important role in determining the final diffusion length. The purer the initial material the higher the final diffusion length. The most harmful impurities in Czochralski and polycrystalline silicon, such as Fe, V, Cr, Ti, form pairs with the primary dopant boron.[10–13] These defects attributed to metal–boron pairs (Fe_iB_s, Cr_iB_s, etc.), act as recombination centers and are responsible for the degradation of the minority-carrier diffusion length. In order to reduce the defect concentration gettering processes with phosphorus, aluminium or co-diffusion have been examined under RTP conditions.[14,15] Recently, it was shown that it is possible to reduce the concentration of the metastable defect of Cz-Si by a fast annealing process in a belt furnace.[16]

The purpose of this paper is to analyze how different RTA conditions affect the stable effective lifetime if the influence of external contamination and external gettering is essentially suppressed during the process. In order to optimize the RTA, a set of adjacent *p*-type Cz-Si wafers were processed with variable combinations of process parameters, using the design-of-experiments (DOE) approach. From the measured effective lifetime the parameters which are important with respect to the stable effective lifetime and minimal defect concentration are deduced.

EXPERIMENTAL PROCEDURES AND RESULTS

Selection of a barrier layer to avoid external contamination

It is well known that the ambient (furnace, gas) or the sample surfaces can act as sources of external contamination, which can lead to deep energy levels in the silicon bandgap during RTA. They could act as recombination centers and thus degrade the lifetime.[9–10] Therefore, a barrier layer is needed in order to protect the bulk sample against external contamination. This is especially important since in this study only the effect of high-temperature cycles on the carrier lifetime was analyzed.

High-lifetime, *p*-type FZ-wafers of resistivity 1·25 Ω cm were used. The wafers are 4 inches in diameter and 250 μm thick. For lifetime measurements the samples are passivated on both sides with a 60 nm thick SiN_x layer which has been optimized with respect to low surface recombination velocities, $S < 10$ cm/s (H. Mäckel *et al.*, to be published). With this excellent passivation layer, lifetimes are measured by microwave-detected photoconductance decay (MW-PCD) with an additional bias light of 0·5-sun.[17] Since this is a differential measurement method, the measured values are strictly speaking differential effective lifetimes.

After RCA-cleaning SiN_x is deposited by means of PECVD at low temperature (350°C) or SiO_2 is processed at 1050°C in a conventional tube furnace. Subsequently the SiN_x- or SiO_2-covered samples are processed at a plateau temperature of 950°C for 100 s. After the RTA process SiN_x and SiO_2 are removed by plasma etching, and the sample surfaces are passivated with SiN_x for lifetime measurement.

Figure 1 shows the effective lifetime of different layers: (1) before; (2) directly after RTA; and (3) after etching the barrier layer and depositing a new SiN_x passivation layer. The values given in Figure 1 are the average values and standard deviations of five points measured on each wafer. It is obvious that the passivation quality is severely decreased by the RTA step. If the barrier layer is replaced by a new SiN_x passivation layer, high effective lifetimes can be recovered. This shows that all barrier layers protect the wafers from contamination effectively. The best result is obtained for the SiN_x-covered wafer, where the lifetime level can be kept on a very high level. A second result is that a thick oxide can protect the wafer better than a thinner

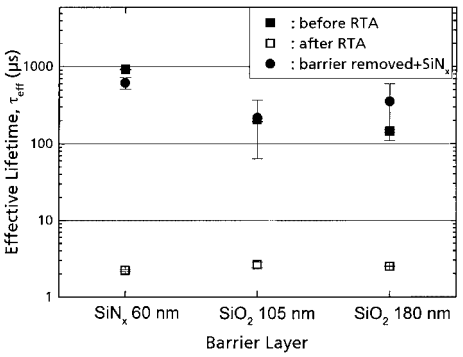

Figure 1. Comparison of the effective lifetime of FZ-Si wafer before and after RTA, covered by three different barrier layers: solid squares, before RTA with SiN_x or SiO_2 passivation as barrier layer; open squares, after RTA with SiN_x or SiO_2 passivation as barrier layer; solid circles, after removal of SiN_x or SiO_2, and new SiN_x passivation

layer. Especially, the spatial lifetime deviation is much greater if the wafer is protected with a thin oxide (i.e. τ_{eff} varies from 30 to 419 µs across the wafer).

In this work the STEAG-RTP system SHS 100 is used, in which the wafer is processed in a quartz chamber. In order to assess the influence of external contamination from the surrounding quartz chamber, lifetime measurements before and after intense cleaning of the chamber are carried out. The chamber is cleaned in 65% HNO_3 for 10 min and etched in 5% HF for 2–5 min at room temperature. Subsequently, the chamber is rinsed with deionized water and purged with nitrogen.

Table I shows the effective lifetime before and after chamber cleaning. After cleaning τ_{eff} of the oxidized wafer improves by 51·4% from 354·1 to 536 µs, whereas τ_{eff} of the SiN_x-coated wafer is not influenced by cleaning. This shows that the lifetime reduction of SiO_2-coated samples during the RTA process is likely to be caused mainly by external contamination. In contrast, the SiN_x wafers exhibit the same high lifetime before and after chamber cleaning. This underlines the excellent barrier quality of SiN_x, even though it is thinner than the SiO_2 layers and is deposited at low temperatures (350°C).

Optimzation of process parameters

A design-of-experiments (DOE) approach is used to analyze the influence of process parameters. DOE is widely used in research in order to determine effects of different factors and to optimize a process statistically and systematically. The major classes of designs that are typically used in scientific experiments are $2^{(k-p)}$ (two-level, multifactor), $3^{(k-p)}$ (three-level, multifactor) and screening designs for large numbers of factors. In this work $2^{(5-1)}$ experiments are used.[18] 'Two-level' means that we choose a maximum and minimum in the actual values of each parameter; '(5-1)' indicates that this design has in overall 5 parameters, but requires only 16 (2^4) runs instead of 32 (2^5) runs. In Table II, a17 and a18 are the center-point runs, where all factors are set at their midpoint. This is to test whether or not there is a nonlinear component in the relationship between the factors in the design and the dependent parameters. The 17 different parameter sets for the $2^{(5-1)}$ experiment

Table I. Comparison of effective lifetime of *p*-type FZ-silicon sample, before and after quartz chamber cleaning

Barrier layer	τ_{eff} (µs)		Deviation(%)
	Before cleaning	After cleaning	
SiN_x 60 nm	612·7	634	+3·5
SiO_2 180 nm	354·1	536	+51·4

Table II. Scheme of 17 different processes in RTA for $2^{(5-1)}$ design-of-experiments; − and + refer to the slow and fast ramping rates or low and high cooling-point temperatures, respectively; 0 represents the middle value between the low (−) and the high (+) value

Run	$T_{plateau}$ (°C)	$t_{plateau}$ (s)	R_{down} (°C/s)	R_{up} (°C/s)	$T_{cooling\ pt.}$ (°C)
a1	850	30	−	−	+
a2	850	30	−	+	−
a3	850	30	+	−	−
a4	850	30	+	+	+
a5	850	120	−	−	−
a6	850	120	−	+	+
a7	850	120	+	−	+
a8	850	120	+	+	−
a9	1050	30	−	−	−
a10	1050	30	−	+	+
a11	1050	30	+	−	+
a12	1050	30	+	+	−
a13	1050	120	−	−	+
a14	1050	120	−	+	−
a15	1050	120	+	−	−
a16	1050	120	+	+	+
a17	950	75	0	0	0
a18	950	75	0	0	0

design are represented in Table II. In this work the variable process parameters are: plateau temperature $T_{plateau}$; plateau time $t_{plateau}$; heating rate R_{up}; cooling rate R_{down}; and cooling-point temperature $T_{cooling\ pt}$.

Boron-doped Cz-Si wafers with resistivity 1·06 Ω cm, thickness 350 μm and size $5 \times 5\,cm^2$ are used for this experiment. The oxygen content $[O_i]$ of the Cz-wafer is $5 \times 10^{17}\,cm^{-3}$, and the initial stable effective lifetime is 15 μs as measured on SiN_x-passivated reference samples.

After RCA-cleaning SiN_x is deposited at low temperature by PECVD, since this gives better protection against contamination from the furnace than thermal SiO_2, as already shown. After the RTA process the SiN_x layer is etched off an optimized plasma etch step[19] and a new SiN_x layer is deposited. Subsequently, the effective lifetime before light-induced degradation τ_0 is measured directly after a forming gas anneal (FGA) step at 425°C. The wafer is then illuminated with white light of intensity $100\,mW/cm^2$ (1-sun) for at least 30 h. Finally, the stable effective lifetime τ_d is measured.

Figure 2 shows the stable effective lifetime τ_d after light degradation with respect to 17 different process parameters. The values given in Figure 2 are the average values and standard deviations of five points measured on each wafer. The average of the stable effective lifetime of a reference sample which has received the SiN_x barrier layer, the plasma etch step and deposition of the SiN_x passivation layer, but no RTA step is 15 μs after light degradation. In the case of RTA-treatment at 850°C for 120 s, plateau time τ_d is increased drastically by 60% from 15 to 24 μs (a5–a8) almost independent of the ramping conditions.

In order to exclude the possibility that the significant improvement of the Cz-material is caused by hydrogen diffusion from the SiN_x into the silicon bulk, we have repeated the experiment with a 200-nm-thick SiO_2 barrier layer. Since we achieve the same lifetime improvement, we can exclude any external gettering. To our knowledge this is the first time that an improvement of the stable effective lifetime of Cz-Si by an RTA-process without external gettering has been demonstrated.

The wafers (a9–a10, a13–a14) with a slow cooling rate at 1050°C in RTA have higher stable effective lifetimes than the wafers treated by fast cooling (a11–a12, a15–a16). If high cooling rates are applied, the stable effective lifetime is 50% lower compared with the non-RTA-treated reference sample.

These facts can also be seen in Figure 3, which shows the pareto chart of standardized effects through $2^{(5-1)}$ experimental design. The magnitude of each effect is represented by a column. The line $p = 0{\cdot}05$ indicates the limit beyond which an effect is statistically significant. Obviously, the plateau temperature has a strong

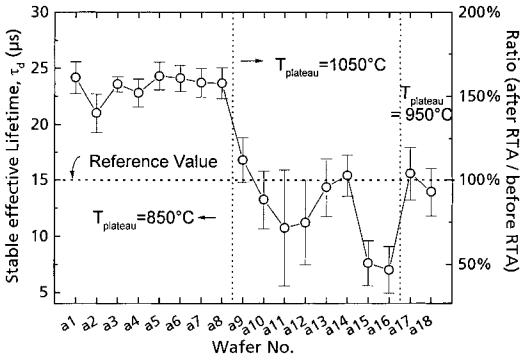

Figure 2. Stable effective lifetime of boron-doped Cz-silicon wafer after RTA-processing according to Table II. The stable effective lifetime of the unprocessed reference wafer is 15 µs

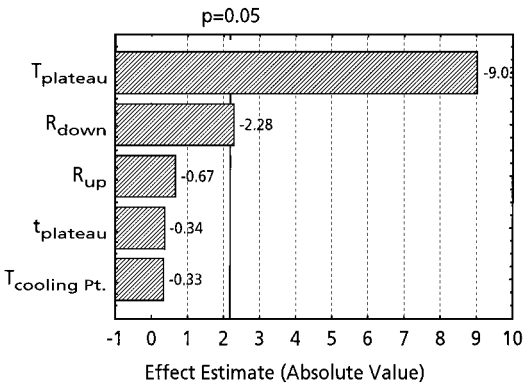

Figure 3. The pareto chart of standardized effects through $2^{(5-1)}$ design-of-experiments. For $p \geqslant 0{\cdot}05$ an effect is statistically significant. Here, the plateau temperature has a strong influence on the stable effective lifetime

correlation with the effective lifetime after light-induced degradation. Furthermore, the cooling rate R_{down} has some effect on the stable effective lifetime which is apparent from the wafers treated at 1050°C. The other parameters seem to be negligible.

In the literature, RTA-induced defects have been analyzed by deep level transient spectroscopy (DLTS).[12,20] We have investigated samples a5 and a16 by DLTS, but it was not possible to detect a signal.

Effect of plateau temperature on the stable effective lifetime

For a further optimization the parameters of the a5 run are chosen, which gave the best stable effective lifetime (see Figure 2). The plateau temperature is varied between 700 and 1050°C, keeping the other parameters fixed.

The normalized defect concentration N^*_{t} is determined from the minority-carrier lifetime before (τ_0) and after (τ_{d}) light-induced degradation.[6]

$$N_{\mathrm{t}}^{*} := \frac{1}{\tau_{\mathrm{d}}} - \frac{1}{\tau_0} = \sigma_{\mathrm{n}} \upsilon_{\mathrm{th}} N_{\mathrm{t}}$$

where N_{t} is the concentration of the metastable defect and σ_{n} and υ_{th} are the electron capture cross-section of the metastable defect and the thermal velocity, respectively. It is possible to calculate N^*_{t} under the assumption that

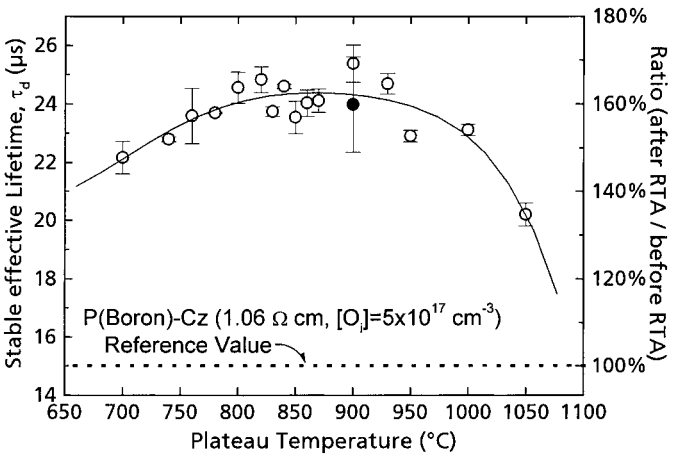

Figure 4. Evolution of stable effective lifetime after light-induced degradation as a function of the temperature for SiN_x-coated Cz-Si samples (open symbols). The solid circle indicates the stable effective lifetime of a sample with a 200-nm-thick SiO_2 barrier layer. The dashed line indicates the stable effective lifetime of the non-RTA-treated reference sample with SiN_x surface passivation

the metastable defect is completely deactivated after annealing at 200°C, and is completely activated after illumination for 30 h at 100 mW/cm^2 (1-sun).

Figure 4 shows the dependence of the stable effective lifetime in Cz-Si on the plateau temperature in the range 700–1050°C. The plateau time is set to 120 s. The non-RTA-treated reference wafer shows a stable effective lifetime of 15 μs. All RTA-processed wafers have a lifetime higher than the reference wafer. In Figure 4, 100% represents the stable effective lifetime of the non-RTA-treated reference sample. The highest improvement, of ~80% (from 15 to 25·5 μs) can be observed at 900°C. The solid circle denotes the stable effective lifetime of a sample covered with a 200-nm-thick SiO_2 barrier layer. Since we can obtain the same improvement, we can exclude any external gettering, i.e. by hydrogen diffusion from the SiN_x layer. On the other hand, after rapid thermal annealing at 1050°C, the stable effective lifetime is reduced to 82·3% of this optimum value, but for this high temperature a strong improvement on the initial value is also observed.

Figure 5 shows the normalized defect concentration after RTA. The normalized defect concentration of the non-RTA-treated reference sample is 0·06 μs^{-1}. N^*_t is strongly reduced from 0·06 to 0·037 μs^{-1}, due to

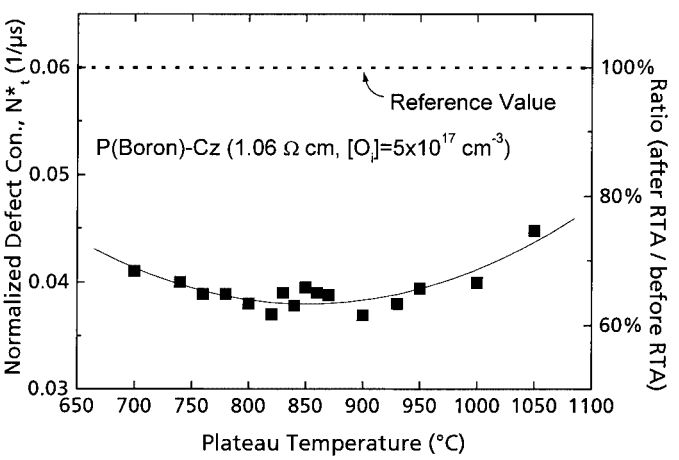

Figure 5. Normalized defect concentration of the RTA-processed CZ-Si samples (SiN_x-coated) for different plateau temperatures. The dashed line at 100% indicates the defect concentration of the unprocessed reference sample

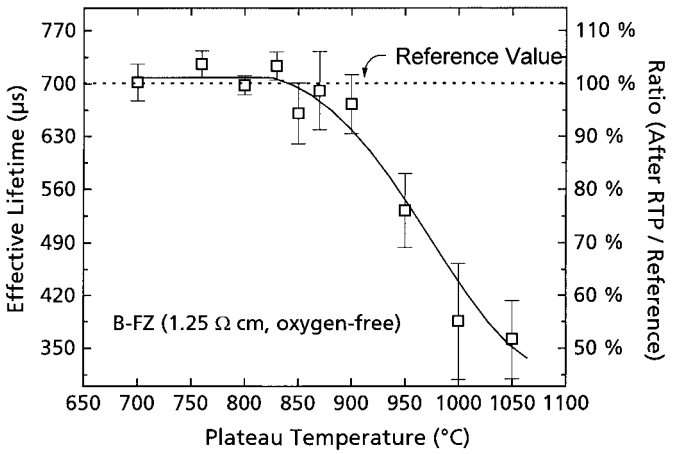

Figure 6. Effective lifetimes of SiN_x-coated FZ-Si samples for different plateau temperatures, with plateau time set to 120 s

RTA at 900°C. Thus, it is possible to improve the stable effective lifetime and reduce the normalized defect concentration by rapid thermal annealing. This reduction is somewhat smaller for temperatures higher than 950°C.

Figure 6 shows the dependence of the effective lifetime on processing temperature in the range 700–1050°C for 120 s for FZ-Si. The reference wafer which has received the SiN_x barrier deposition, the plasma etch step and deposition of the SiN_x passivation layer, but no RTA step, exhibits a lifetime of 700 µs. This reference value was reached for all RTP-treated FZ-wafers with plateau temperature between 700 and 900°C. However, a dramatic degradation occurs at temperatures higher than 900°C. Especially, the effective lifetime at 1050°C is reduced by 50% from 700 to 360 µs. Also, for higher temperatures, the standard deviation of the five measurement points on the wafer is higher than that for lower temperatures. A similar trend has been observed by Eichhammer *et al.*[9] We attribute this reduction of the lifetime, which reduces the improvement in Cz-Si, to disruption of the crystalline order at higher temperatures.

CONCLUSION

The potential of RTA to reduce the metastable defect density in Cz-Si was studied. To avoid external contamination during the RTA-process, SiN_x deposited with PECVD, and two different thermally processed SiO_2 layers on FZ-wafers were examined. The SiN_x layer was found to be very effective as a barrier layer, even without previous cleaning of the RTP furnace. By using the barrier layer, it was possible to keep FZ-Si reference samples at a high lifetime level of 700 µs.

The influence of process parameters on the stable effective lifetime of Cz-Si was investigated by DOE. The wafers were SiN_x-covered, and five process parameters were varied: plateau temperature; plateau time; heating rate; cooling rate; and cooling-point temperature. It was found that the plateau temperature is the most important parameter with respect to the stable effective lifetime. For all plateau temperatures, light-induced degradation could be strongly reduced.

The optimal plateau temperature was approximately 900°C with a plateau time of 120 s. This led to an improvement of the stable effective lifetime of 1 Ω cm Cz-Si by a factor of 2. The reduced improvement at higher temperatures around 1000°C seems to be correlated with an induced crystal defect, as the lifetime degradation also occurs in FZ-Si. To our knowledge this is the first time that an improvement of the stable effective lifetime of Cz-Si by a rapid thermal annealing process without external gettering has been demonstrated.

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