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ScienceDirect
Nuclear Instruments and Methods in Physics Research B 266 (2008) 2479–2482
NIM B Beam Interactions with Materials & Atoms
www.elsevier.com/locate/nimb

# Defect characterization in boron implanted silicon after flash annealing

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Available online 7 March 2008

**Abstract**

Flash-assisted rapid thermal processing (fRTP) has gained considerable interests for fabrication of ultra-shallow junction in silicon. fRTP can significantly reduce boron diffusion, while attaining boron activation at levels beyond the limits of traditional rapid thermal annealing. The efficiency of fRTP for defect annealing, however, needs to be systematically explored. In this study, a (1 0 0) silicon wafer was implanted with 500 eV boron ions to a fluence of $1 \times 10^{15}$ cm$^{-2}$. fRTP was performed with peak temperatures ranging from 1100 °C to 1300 °C for approximately one milli-second. High resolution transmission electron microscopy and secondary ion mass spectrometry were performed to characterize as-implanted and annealed samples. The study shows that fRTP at 1250 °C can effectively anneal defects without causing boron tail diffusion.


*PACS:* 61.72.Cc; 61.72.sh; 61.72.U

*Keywords:* Shallow junction; Doping; Boron; Annealing

## 1. Introduction

Ultra-shallow junction formation in silicon has been a technological bottleneck for scaling down the size of complementary metal oxide semiconductor (CMOS) devices in ultra large integrated circuits [1]. The primary challenges during the past decades have included the development of a high-current low-energy ion implanter for the doping process and the novel high temperature processor for dopant activation. The first issue comes from the well known space charge effect in which a significant current loss occurs during beam extraction and transport. The second issue is due to the transient enhanced diffusion of dopant in silicon [1,2]. For p-type doping, implanted boron (B) atoms interact with Si interstitials to create a diffusion path with almost zero diffusion barrier [1–3]. The penetration of B tail is determined by annealing temperature and time, as well as the population of free interstitials, which is further determined by the Ostwald ripening process of defect annealing [1–3]. In addition to the problem of enhanced diffusion at the tail region of B profile, junction formation also faces the challenge caused by limited solid solubility of B in Si. Basically, to scale down the size of CMOS devices, it requires a junction with a depth as shallow as possible and a resistivity as low as possible [4]. Thus it is obvious that a high temperature annealing process with a short annealing duration can achieve such requirements.

Today, rapid thermal annealing with a ramp up rate above ~100 °C has been widely used. Driven by the need to further optimize/minimize thermal budget, various alternative thermal annealing processes, such as flash annealing

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doi:10.1016/j.nimb.2008.03.036

[5], flame annealing [6], and laser annealing [7], have been seriously investigated. Considering factors such as repeatability, integrability and high throughput, flash annealing represents one of the most promising solutions for the semiconductor industry. Extensive efforts have been made to investigate the mechanisms and to optimize the process associated with ultra-fast thermal annealing of B implanted Si (a good review can be found, for example, in the proceeding of Symposium C "Sub-Second Rapid Thermal Processing for Device Fabrication" at the MRS Spring Meeting 2006, San Francisco).

Like all other techniques, the annealing parameters need to be optimized. In this study we have characterized defects and defect induced B diffusion in B implanted silicon after flash annealing at various temperatures, with the aim to understand and minimize irradiation damage and B diffusion in ultra-shallow junction formation.

## 2. Experimental procedure

In this study, a Si (100) wafer was implanted with 0.5 keV B to a dose of $1 \times 10^{15}$ cm$^{-2}$ at room temperature. The sample was then cut into pieces and annealed by using a milli-second flash anneal technique developed by Mattson Technologies. Samples were annealed in two steps. First, the annealing reached an intermediate temperature of 750 °C. Then it jumped to peak temperatures ranging from 1100 °C to 1300 °C. The gas ambient in the tool was maintained around 100 ppm $O_2$ for all the wafer samples. To reach the intermediate temperature, a heating rate of 150 K/s was programmed. After flash annealing, samples were characterized by using secondary ion mass spectrometry (SIMS) and transmission electron microscopy (TEM). High resolution SIMS analysis for B depth profiling was obtained by using 1 keV $O_2^+$ primary beam at 56° incident angle with oxygen flooding techniques. TEM analysis for defect characterization was obtained by using parallel illumination, with a Philips CM200 field-emission gun TEM operated at an accelerating voltage of 200 kV. A focused ion-beam lift-off method was used to prepare the TEM samples.

## 3. Results and discussion

Fig. 1(a)–(d) shows the B profiles after flash annealing at peak temperatures of (a) 1100, (b) 1175, (c) 1250 and (d) 1300 °C, respectively. An implanted B profile is plotted for comparison. A very small diffusion at the tail region of B profile occurs in the 1300 °C flash annealed sample. The tail shift, judged by B concentration of $3 \times 10^{18}$/cm$^3$, is around 1.6 nm. In annealing with peak temperatures below 1300 °C, there is no B diffusion observed.

In order to verify that the B diffusion results were not affected by the nonuniformity of annealing or the uncertainty in SIMS analysis, we repeated SIMS analyses three times on different spots of both the implanted sample and 1300 °C annealed sample. In all cases, SIMS results over-

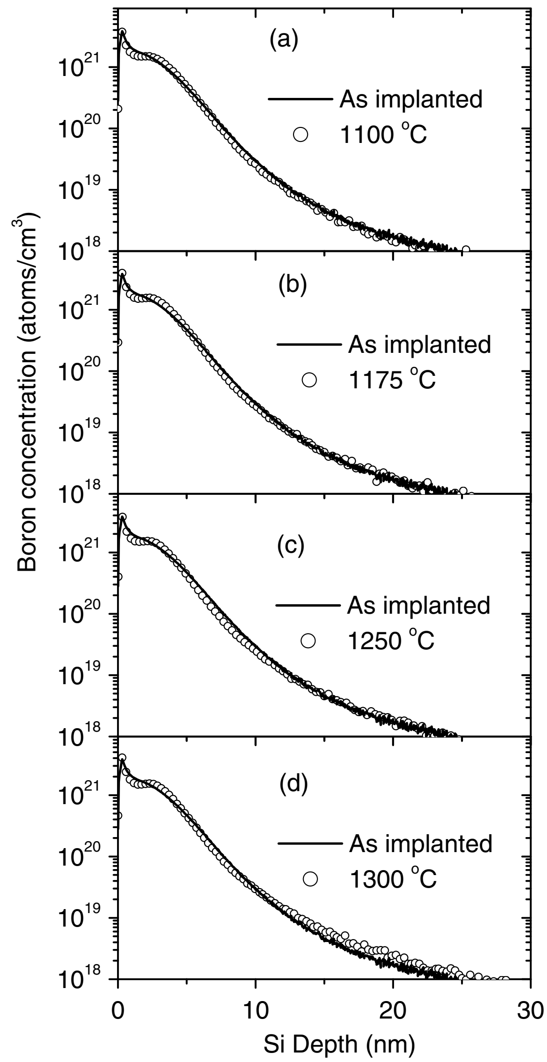


Fig. 1. (a)–(d) Boron SIMS profiles in $1 \times 10^{15}$ cm$^{-2}$, 0.5 keV B implanted Si after flash annealing with peak temperatures of (a) 1100 °C, (b) 1175 °C, (c) 1250 °C and (d) 1300 °C, respectively. B profile from the implanted sample is plotted for comparison.

lapped very well. Therefore, we believe that both annealing and B profiling are reliable and repeatable.

In all annealed samples, B profiles near the surface (<5 nm) show a sharp surface peak and a shoulder-like distribution (at a concentration of $\sim 1.5 \times 10^{21}$/cm$^3$). The sharp surface peak is almost a universal feature in all B profiles after annealing. The flat shoulders indicate that very high B activations were achieved by annealing. Similar features have been observed in laser annealed samples [7]. However, we made no attempt to characterize the electronic property of junction, primarily due to the reason that currently existing techniques such as spreading resistance analysis are not reliable for ultra-shallow junctions.

Fig. 2(a)–(d) present cross-section TEM micrographs of Si after the 0.5 keV B implantation (a) and after flash annealing at peak temperatures of (b) 1100 °C, (c) 1250 °C, and (d) 1300 °C. Some of the micrographs are intentionally slightly under-focused to increase edge

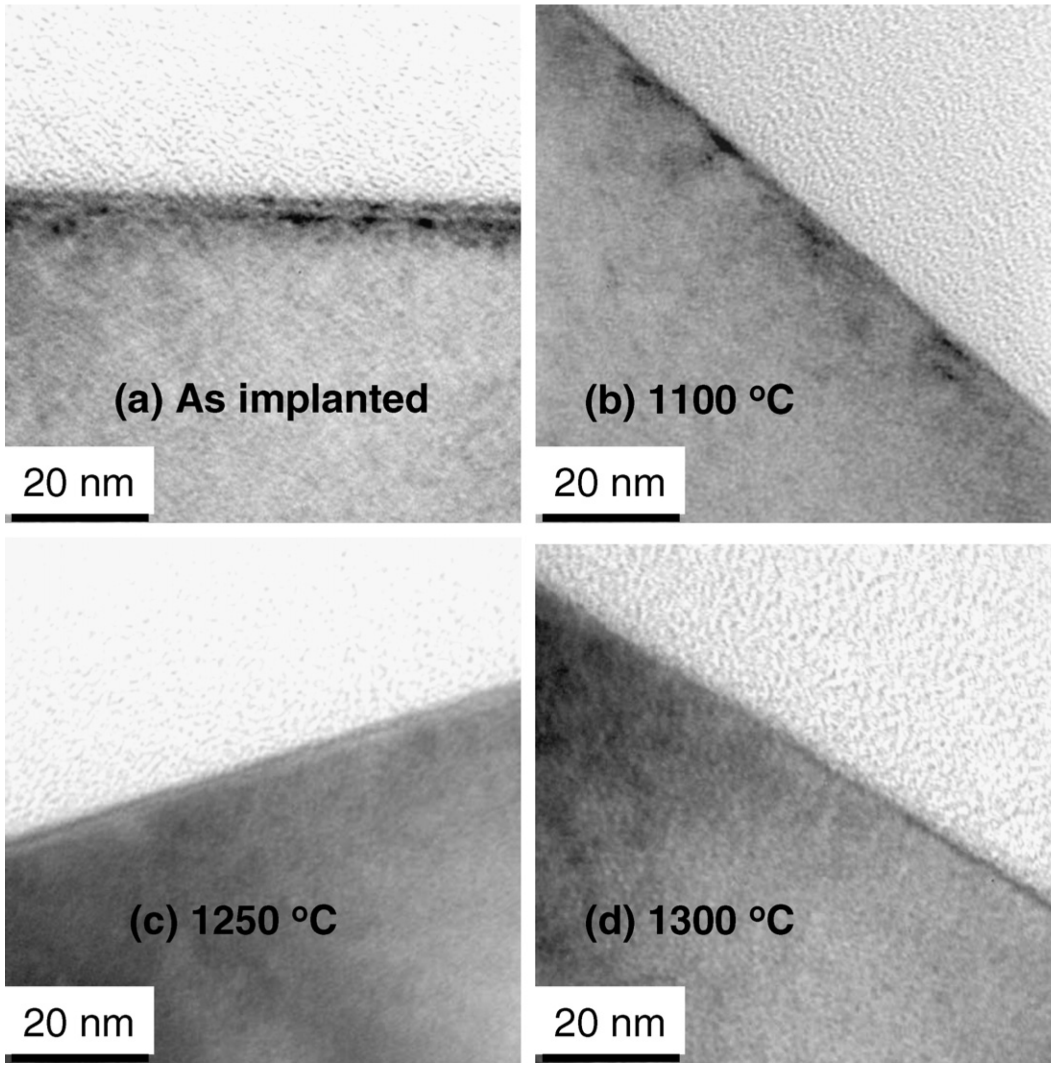


Fig. 2. (a)–(d) TEM micrographs obtained from (a) as-implanted Si, (b) after 1100 °C, (c) after 1250 °C, and (d) after 1300 °C flash annealing for a period of ~1 ms.

contrast. As shown in Fig. 2(a), a band of defect clusters are visible in the implanted Si at a depth of ~5 nm. After flash annealing at 1100 °C, Fig. 2(b) shows that defect clusters still exist near the surface. However, as shown in Fig. 2(c) and (d), Si is defect free at annealing temperatures of 1250 and 1300 °C.

Defects observed in Fig. 2(b) are small point defect clusters, rather than large extended defects such as {311} rod like defects or dislocation loops. This is determined by the detail of Ostwald ripening of defects. In a quasi steady state, when growth and decay of defect clusters reach equilibrium, the concentration of free interstitials around defect clusters is determined by the binding energy of interstitials trapped in clusters. Normally, the larger the cluster, the higher the binding energy [1]. Therefore, small clusters create a high concentration of free interstitials around them and large clusters create a relatively low concentration of free interstitials in their surrounding media. Concentration gradient thus drives Si interstitials' diffusion from small clusters toward larger defect clusters, thus causing the growth of cluster size. This Ostwald ripening process, however, is significantly altered if defects are in the vicinity of a free surface. A free Si surface is a strong sink for point defects [8], and interstitial removal at the surface will limit the chance to form larger defect clusters. In our study, end of range defects are located at a depth of ~5 nm, and quick defect removal at the surface ends the annealing process within a short time without forming large clusters.

The above study suggests that an effective defect removal can be achieved by flash annealing at a peak temperature at or above 1250 °C. On the other hand, in order to minimize boron diffusion, annealing temperature should be less than 1300 °C. Thus, a flash annealing at a temperature of 1250 °C would reach a good balance between diffusion and activation.

It is worthwhile to note that B diffusion in the 1300 °C annealed sample has a tail shift which is more like an exponential like spreading, rather than a Gaussian spreading (featured with a shoulder shape). Under a traditional rapid thermal annealing process, a Gaussian spreading would be observed after a relatively high temperature annealing, i.e. 1000 °C for 1 s. As a contrast, an exponential like spreading will be observed at low temperature annealing, i.e. 650 °C for 30 min. The underlying physics for the difference is that when the mean number of B diffusion events occurring during the whole annealing process is less than 1, profile spreading is featured with an exponential like spreading [1]. If averaged diffusion events occurring for a single B atom is significantly larger than 1, profile diffusion will follow a Gaussian spreading [2]. In this study, the exponential like spreading observed in 1300 °C annealed sample suggests that the annealing is done either with extremely low Si interstitial concentration (which reduces the frequency of B–Si interstitial interaction) or for an extremely short annealing period (which reduces diffusion events even with a high B–Si interaction frequency). Thus, tail diffusion observed in Fig. 1 agrees with our annealing condition, a milli-second annealing.

## 4. Summary

We have systematically studied the defects formed in B implanted Si after flash annealing at peak temperatures of 1100, 1175, 1250 and 1300 °C, respectively. High resolution SIMS analysis shows that only the 1300 °C annealed sample has noticeable B diffusion at the tail region. For the sample annealed at 1250 °C, neither tail diffusion nor defect clusters are observed. This suggests that flash annealing at a temperature of around 1250 °C can achieve desired junctions. The study is aimed to optimize the flash annealing technique to minimize the impact of implantation induced damage on boron diffusion. A good balance among diffusion, activation and defect removal can be reached under certain annealing conditions. Furthermore, fundamental understanding about the features observed in SIMS and TEM have been discussed.

## Acknowledgements

The study was supported in part by the Welch Foundation through Grant No. A-1671.

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