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Determination of interface states in metal(Ag,TiN,W) – Hf: Ta_2O_5/SiO_xN_y – Si structures by different compact methods

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ABSTRACT

In this work a compact set of analytical methods for determination of the interface state densities of metal-insulator-silicon structures containing ultrathin dielectrics is constructed (high-low method, conductance method using G_{ps}/ω–ω curves, conductance method using G_{ps}/ω–V curves and Terman's method). Specific structures metal(Ag,TiN, W) – Hf:Ta_2O_5/SiO_xN_y – Si are studied in details.

It has been found that the serial measurement mode is more suitable for use than the parallel one. Obtained capacitance values in serial mode can be used in majority of the cases without further corrections, if very high precision is not required. The proposed correction method for serial resistance gives substantial improvements for G_{ps} values.

At midgap all four considered methods give similar values. Terman's method appears to give substantially overestimated values of D_{it} for energies other than that of the midgap, owing to the charging of the internal interface between the higk-k layer and the interfacial SiO_xN_y layer.

1. Introduction

Interfacial energy states located in the forbidden energy gap of the semiconductor (interface states) are an important factor affecting the functioning of electron devices containing metal-dielectric-semiconductor (MIS) structures. Various methods of determination of the distribution of these states over the range of energies lying between the top of the valence band (E_v) and the bottom of the conduction band (E_c), have been developed during several decades; these methods are well described in several textbooks [1–3]. Simultaneously, with the progress of the technology and the downscaling of the devices towards nanoscale, limitations of the adopted methods emerge.

Results obtained by different methods are compared in several works. In [4], interface states of Au/Ta_2O_5/n-InP structures were determined by conductance method, Terman's method and deep-level transient spectroscopy. Recently, extraction of interface state densities with Terman's, conductance and high-low method was discussed for the case of metal–SiO_2/SiC structures [5]. The issue of the correct extraction of interface trap density of MOS devices with high mobility semiconductor substrates has been studied in [6], where it was stated that the conductance method can be adapted and made reliable for alternative semiconductors while maintaining its simplicity. Detailed comparison of methods to quantify interface trap densities at dielectric/III–V semiconductor interfaces is given in [7]. In [8] it has been shown that frequency-dependent conductance measurements give similar results to those obtained in [7] by C–V measurements. An attempt for reexamination of the extraction of MIS interface-state

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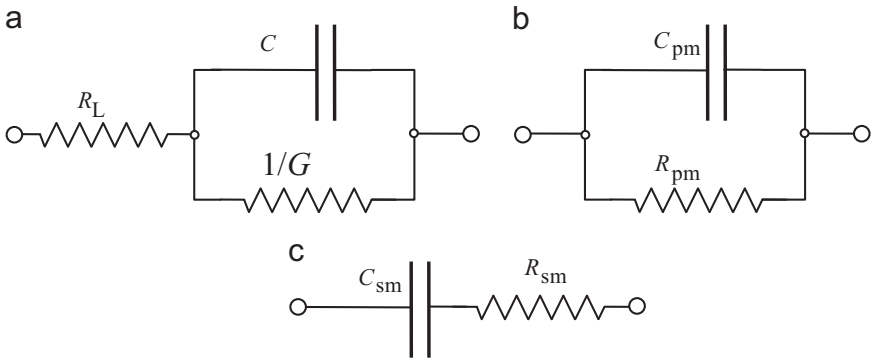

Fig. 1. Equivalent circuit with serial resistance (a) and corresponding circuit for parallel measurement mode (b) and serial measurement mode (c).

density by *C–V* stretchout and conductance methods has been recently done in [9]. Several limitations of the considered methods have been noted. In [10] an adaptation of Terman's high frequency capacitance–voltage method for interface trap density extraction for the heterojunction multi-layer capacitor has been proposed.

In this work we study a specific combination of gate materials (Ag, W and TiN) with high permittivity (high-κ) dielectric stack obtained by Hf doping of tantalum pentoxide deposited on a nitrided Si substrate ($Hf:Ta_2O_5/SiO_xN_y$). We demonstrated earlier that Hf doping improves substantially the dielectric and reliability properties of tantalum pentoxide [11], which is particularly noticeable in the case of nitrided substrates [12], since the nitridation improves the properties of the interfacial layer and limits its excessive growth [13]. We have shown in [14] that metal-oxide-silicon structures containing Ag-gate exhibit superior leakage properties compared to those with some other typical N-gate materials, while having comparable capacitance properties.

In this work we propose a compact method of correction of the measured *C–V* and *G–V* curves at various frequencies (*f*) for the effect of leakage currents and serial resistance. Thus corrected curves are thereafter used for extraction of interface state densities by three different methods: low-high frequency, admittance and Termann's method. Determination methods are presented in a practical form enabling easy computation and comparison of the results obtained by different methods, without compromising the accuracy of the obtained results usually obtained by the considered methods.

2. Theory

2.1. Choice of the measurement mode, correction method and correction for the serial resistance

It is a common practice to measure *C–V* characteristics of metal-insulator-semiconductor structures in parallel mode. The main reason for this choice is that in the ideal case the quantities required for the determination of interface states (C and $G=1/R_p$) are straightforward obtained. However, in the realistic case where serial resistances are present, C_p–V and G_p–V characteristics are substantially distorted. Some methods were proposed to account for the effect of the serial resistance. In the standard method, serial resistance is included in the equivalent circuit and then the expressions for actual capacitance and admittance derived for the case of measurement in parallel mode [3]. The main deficiency of this method originates from the strong distortion of the *C-V* and *G-V* curves at high frequencies compared to the actual curves. As a result, subsequent transformation from the measured to the actual curves is subject to substantial errors. In one other method [15], *C–V* curves are recorded for two substantially different frequencies and than a single frequency independent curve calculated based on an equivalent circuit model. The main deficiency of this method is that possible real frequency dependence of the capacitance is ignored.

In order to overcome the shortcomings of both methods, here we propose the use of C_s-V and G_s-V curves measured in serial mode and their subsequent transformation to corresponding actual curves. We consider only low applied voltages where leakage current is not too high to influence the measurements. In this case, realistic equivalent circuit shown in Fig. 1a) can be used.

Usual assumption is that the serial resistance is negligible and hence circuit (a) can be replaced with (b), thus allowing using parallel mode for determination of capacitance and admittance of the MOS structure, using simple expressions

$$C = C_{pm} \tag{1a}$$

and

$$G = \frac{1}{R_{pm}}. \tag{1b}$$

In the realistic case serial resistance strongly affects capacitance value at higher frequencies and the serial resistance has to be taken into account. Impedance of the circuit in this case is

$$Z = \frac{1/G}{1+(\omega C/G)^2} + R_L + \frac{1}{i\omega}\frac{1/C}{1+1/(\omega C/G)^2}, \tag{2}$$

where $\omega = 2\pi f$ is the cyclic frequency.

Capacitance and resistance measured in serial mode are hence

$$R_s = R_s(V;\omega) = \frac{1/G}{1+(\omega C/G)^2} + R_L \tag{3a}$$

and

$$C_s = C_s(V;\omega) = C\left(1+(G/\omega C)^2\right). \tag{3b}$$

Inversely, for the actual capacitance and admittance we obtain

$$C = C(V;\omega) = \frac{C_{sm}}{1+\omega^2 C_{sm}^2 (R_{sm}-R_L)^2} \tag{4a}$$

and

$$G = G(V;\omega) = \frac{\omega^2 C_{sm}^2}{1+\omega^2 C_{sm}^2 (R_{sm}-R_L)^2}(R_{sm}-R_L). \tag{4b}$$

2.2. Determination of the capacitance in accumulation

Standard methods of characterization by C–V measurements comprise measurement of capacitance in strong accumulation, at voltages of about 5 V, required to determine the capacitance of the insulating layer itself (C_{ox}). For extremely thin dielectrics it is impossible to approach such high values, due to enormous leakage currents, irreversible degradation and even breakdown of the MOS structures. Besides, quantum effects are present, modifying the characteristics in even more complicated manner. Quite often, complex computations are employed to determine the capacitance C_{ox} starting from the experimental data obtained and substantially lower voltages in accumulation, of about 2 V [16,17]. Another approach for determining C_{ox} is that using the extrapolation method proposed by Kar [18]. This method accounts for the quantum effects. In [19] it has been demonstrated that this extrapolation method can efficiently be incorporated in a parameter extraction technique for high-κ gate dielectrics that directly yields values of several parameters.

The extrapolation method is based on the validity of the expression

$$\sqrt{\frac{d}{dV_g}\frac{1}{C^2}} = \sqrt{2|\beta_{ac}|}\left(\frac{1}{C}-\frac{1}{C_{ox}}\right), \tag{5}$$

where β_{ac} is the accumulation layer surface potential quotient. Capacitance C_{ox} is determined from the intercept ($(1/C_{ox})$) of the fitting line for the part in strong accumulation obtained in a $\left(\sqrt{(d/dV_g)(1/C^2)}\right)$,$1/C$ plot with the $1/C$ axes.

From our extensive experience with high-κ dielectrics we find out that the above explained compact analytical method gives rather good results close to those obtained by using numerical quantum simulators. Therefore, here we propose in determination of interface state densities to use the given extrapolation method along with corrected values of the capacitance calculated as described in Section 2.1.

Thus obtained value of the capacitance in accumulation (C_{ox}) is used in determination of the equivalent oxide thickness (d_{eq}) of the dielectric with the expression

$$d_{eq} = \frac{\varepsilon_{so}}{C_{ox}} S, \tag{6}$$

where S is the surface area of the capacitor and ε_{so} is the dielectric permittivity of SiO_2.

2.3. Determination of the flatband voltage and the oxide charge

We consider the case of a p-type substrate. First the flatband voltage capacitance is determined as

$$C_{fb} = \frac{\frac{C_{ox}\varepsilon_{Si}S}{\lambda_D}}{C_{ox}+\frac{\varepsilon_{Si}S}{\lambda_D}}, \tag{7}$$

where λ_D is the Debye length calculated as

$$\lambda_D = \sqrt{\frac{\varepsilon_{Si}kT}{q^2 p_0}}. \tag{8}$$

In (8) ε_{Si} is the static dielectric permittivity of silicon, p_0 is the equilibrium hole concentration in the bulk of the semiconductor, q is the elementary charge, k is the Boltzmann constant and T is the temperature.

Flatband voltage, V_{fb}, was determined as the voltage value at which the capacitance equals the calculated value of flatband capacitance, C_{fb}, using a linear interpolation method for values between the measured points.

Once having determined the flatband voltage, the oxide charge Q_{ox} is calculated using the standard expression

$$Q_{ox} = \left(\frac{\Phi_{ms}}{q} - V_{fb}\right)C_{ox}, \tag{9}$$

where Φ_{ms} is the work function difference between the metal and the silicon substrate.

2.4. Determination of the surface potential

In the case of a p-type substrate, electric field in the oxide (high-κ dielectric) at the contact with the substrate is given with the expression [2].

$$E_{ox} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(\frac{2kT}{q}\frac{p_0}{\varepsilon_{Si}}q\right)^{1/2}\left(\exp\left(\frac{-qV_s}{kT}\right) + \frac{qV_s}{kT} - 1 + \left(\frac{n_i}{p_0}\right)^2\left(\exp\left(\frac{qV_s}{kT}\right) - \frac{qV_s}{kT} - 1\right)\right)^{1/2}, \tag{10}$$

where ε_{ox} is the effective dielectric permittivity of the dielectric, V_g is the voltage drop in silicon (surface potential) and n_i is the intrinsic carrier concentration is silicon.

Oxide voltage V_{ox} is

$$V_{ox} = E_{ox} d_{ox} \tag{11}$$

where d_{ox} is the physical thickness of the dielectric.

The equivalent oxide thickness (d_{eq}) of the high-κ dielectric, is connected to d_{ox} with the relation

$$d_{eq} = \frac{\varepsilon_{so}}{\varepsilon_{ox}} d_{ox}. \tag{12a}$$

Quite often dielectric layer is of variable composition, and hence the quantity in (12) corresponds to an effective permittivity of the dielectric layer. Approximately the high-κ dielectric can be regarded as stacked layer composed of a bulk high-κ layer with thickness d_{hk} and an interfacial layer with thickness d_{if}. In this case the equivalent oxide thickness is expressed as ([13])

$$d_{eq} = \frac{\varepsilon_{so}}{\varepsilon_{hk}} d_{hk} + \frac{\varepsilon_{so}}{\varepsilon_{if}} d_{if}, \tag{12b}$$

where ε_{hk} is the permittivity of bulk high-κ layer and ε_{if} is the permittivity of the interfacial layer.

On the other hand, oxide voltage is given by

$$V_{ox} = V_g - V_{fb} - V_s, \tag{13}$$

Combining (10)–(13) one obtains the following expression

$$V_s = V_g - V_{fb} - \frac{\varepsilon_{Si}}{\varepsilon_{so}} \left(\frac{2kT}{q} \frac{p_0}{\varepsilon_{Si}} q \right)^{1/2} d_{eq} \left(\exp\left(\frac{-qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left(\frac{n_i}{p_0} \right)^2 \left(\exp\left(\frac{qV_s}{kT} \right) - \frac{qV_s}{kT} - 1 \right) \right)^{1/2} \tag{14}$$

Using the value of the flatband voltage V_{fb} obtained as described, for each value of the gate voltage V_g the value of the voltage drop in silicon V_s is determined numerically solving the Eq. (14) by the direct iteration method. As a result, we obtain the $V_s - V_g$ curve corresponding to a given corrected $C-V$ curve, V_{fb} for which is used in (14). In this we use for each sample the sole value for V_{fb} obtained from the $C-V$ measurements at the highest frequency (1 MHz), as well as the corresponding value of d_{eq}.

The energy position in the forbidden gap of Si corresponding to a given value of V_g is

$$E = qV_s + kT \ln\left(\frac{p_0}{n_i} \right). \tag{15}$$

2.5. Determination of the theoretical low frequency capacitance

Low frequency capacitance of the depletion layer, C_{id}, in silicon is determined as [2]

$$C_d = \frac{\varepsilon_{Si}}{\sqrt{2}\lambda_D} S \frac{\left| 1 - \exp\left(\frac{-qV_s}{kT} \right) + \left(\frac{n_i}{p_0} \right)^2 \left(\exp\left(\frac{qV_s}{kT} \right) - 1 \right) \right|}{\left(\exp\left(\frac{-qV_s}{kT} \right) + \frac{qV_s}{kT} - 1 + \left(\frac{n_i}{p_0} \right)^2 \left(\exp\left(\frac{qV_s}{kT} \right) - \frac{qV_s}{kT} - 1 \right) \right)^{1/2}}, \tag{16}$$

Capacitance of the MIS structure is

$$C_{id} = C_{id}(V_s) = \left(\frac{1}{C_{ox}} + \frac{1}{C_d} \right)^{-1} = \frac{C_{ox} C_d}{C_{ox} + C_d}. \tag{17}$$

In (17) the value of the capacitance C_{ox} determined as explained in Section 2.2 is to be used and the value of the voltage drop in silicon V_s determined as explained in Section 2.4.

2.6. Terman's method

In Terman's method the distribution of the interface states is determined using a single high frequency $C-V$ curve [20]. In this work, first the capacitance of the dielectric layer itself, C_{ox}, is determined as described in Section 2.2. Then, the flatband voltage, V_{fb}, is determined as described in Section 2.3. Using thus obtained values for C_{ox} and V_{fb}, values of the voltage drop on silicon, V_s, and the ideal capacitance, C_{id}, are calculated.

Next, interface state densities for given value of V_s are determined from the stretch-out of the experimental curve relative to the ideal one,

$$D_{it} = D_{it}(V_s) = \frac{C_{ox}}{q^2 S} \frac{d(V_g - V_{g,id})}{dV_s}, \tag{18}$$

where $V_{g,id}$ is the gate voltage value of the point on the ideal $C-V$ curve having the same capacitance as the actual capacitance of the structure at a given value V_g, and hence of V_s.

2.7. Conductance method using $G_{ps}/\omega-\omega$ curves

In the standard conductance method using $G_{ps}/\omega-\omega$ curves, $G-\omega$ and $C-\omega$ curves are recorded for a given gate voltage, V_g. From thus obtained values of C and G the interface trap admittance G_{ps} is determined. This determination is based on the use of an equivalent circuit shown in Fig. 2a), where a resistor with resistance $R_{ps} = 1/G_{ps}$ is connected in parallel to the capacitor with capacitance C_{ps}.

Corresponding circuit for parallel measurement mode in the case where serial resistance is not present is shown in Fig. 2b). Interface trap admittance G_{ps} is then

$$G_{ps} = \frac{\omega^2 G^2 C_{ox}^2}{G^2 + \omega^2 (C_{ox} - C)^2}. \tag{19}$$

Afterwards, $G_{ps}/\omega-\omega$ curves are plotted and the maximum value of G_{ps}/ω obtained at certain value ω_{max} is used to determine the interface state density corresponding to

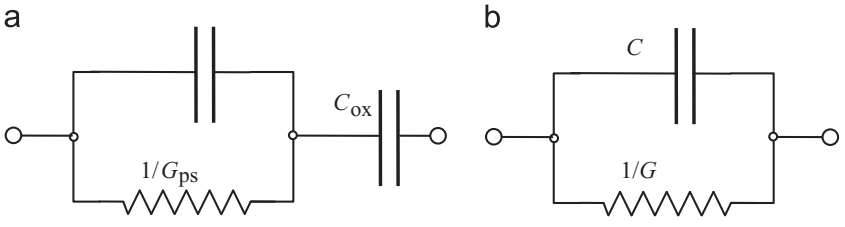

Fig. 2. Simplified equivalent circuit used in the conductance method (a) and corresponding circuit for parallel measurement mode in the case where serial resistance is not present (b).

the given V_g. Although the exact calculation is relatively complex, it has been demonstrated that a simplified expression can be used to calculate D_{it} [4]

$$D_{it} \approx \frac{2.5}{qS}\left(\frac{G_{ps}}{\omega}\right)_{max} = \frac{2.5}{qS}\left(\frac{\omega^2 G^2 C_{ox}^2}{G^2+\omega^2(C_{ox}-C)^2}\right)_{max}. \quad (20)$$

Nevertheless, straightforward application of this method to the measured G_m/ω–V curves in the case of ultrathin high-κ dielectrics leads to huge errors due to the presence of a serial resistance. Quite often, it is impossible to determine the required value, since no clear maximum is observed. In order to obtain corrected G–V curves, we propose to apply the following procedure. First, C_s–V and R_s–V curves are to be recorded for a set of fixed measurement frequencies, ω. Second, C–V and G–V curves are to be calculated from the measured curves, using the method for correction for the serial resistance described in Section 2.1. From the set of G–V curves for all measurement frequencies, the table of G_{ps}/ω values (corrected) is to be constructed. If the rows correspond to given frequencies, then the columns will give the sets of G_{ps}/ω values for given gate voltages corresponding to the sets of measurement frequencies, i.e. the corrected G_{ps}/ω–ω curves.

2.8. Conductance method using G_{ps}/ω–V curves

A method using single G_{ps}/ω–V curve measured at a given frequency ω has been proposed in [21]. Maximum of the quantity G_{ps}/ω in the considered voltage range at certain gate voltage value $V_{g,m}$ is used instead of the maximum in a frequency range. Interface state density is then calculated as

$$D_{it} = D_{it}(V_{g,m}) = \frac{2}{qS}\left(\frac{G_{ps}}{\omega}\right)_{max} = \frac{2}{qS}\left(\frac{\omega^2 G^2 C_{ox}^2}{G^2+\omega^2(C_{ox}-C)^2}\right)_{max}. \quad (21)$$

It has been demonstrated that the values obtained by this method are close to the values obtained by the method using G_{ps}/ω–ω curves [21].

In this work we use the values of the surface potential $V_{s,m}$ corresponding to voltage values $V_{g,m}$, determined as described in subsection Section 2.4.

2.9. High-low method

Another method that is rather efficient for oxides that are not extremely thin is the method using simultaneously obtained high-frequency (C_{hf}) and low-frequency (C_{lf}) C–V curves. Particularly useful is the variation of the method using quasistatic instead of low-frequency curves. For nanosized high-κ dielectrics (thinner than 10 nm), leakage currents are several orders of magnitude higher than the displacement currents and the correct measurement of the quasistatic C–V curves is impossible. This is similar to the case of silicon dioxide films thinner than 4 nm, where low-frequency measurements at about 1 kHz are to be used [22]. The expression for the interface state density for this method is [23]

$$D_{it} = D_{it}(V_g) = \frac{C_{ox}}{q^2 S}\left(\frac{C_{lf}(V_g)/C_{ox}}{1-C_{lf}(V_g)/C_{ox}} - \frac{C_{hf}(V_g)/C_{ox}}{1-C_{hf}(V_g)/C_{ox}}\right). \quad (22)$$

In this work we use high-frequency curves measured at 1 MHz and low-frequency curves measured at 10 kHz. Surface potential when using high-low method is usually determined by using the Berglund integral [24]

$$V_s = q\int_{V_{fb}}^{V_g}(1-C_{lf}(V)/C_{ox})dV. \quad (23)$$

Since the measurement in the cases considered here are done at 1 kHz, the use of the expression (19) is not advantageous as is the case for measurements at very low frequencies. Instead, we propose to use the values obtained using the high frequency C–V curve as described in Section 2.4. Simultaneously, values of the surface potential will be coherent for all the methods compared in this work.

3. Experimental

Metal–Hf:Ta_2O_5/SiO_xN_y–Si structures used in this study were obtained as follows. First chemically cleaned (100) p-type 3÷5 Ω cm silicon wafers were nitrided in ammonia by rapid thermal processing at 700 °C for 20 s. Tantalum oxide was then deposited by reactive sputtering of a Ta target in an Ar+10% O_2 atmosphere so as to obtain Ta_2O_5 layer approximately 7.5 nm thick; the working gas pressure was 3 Pa and rf power density was 4.9 W/cm^2. The Si substrate was heated at 200 °C during deposition. The Hf-doped Ta_2O_5 layers were obtained by deposition of a Hf layer ~0.7 nm thick, on the top of previously deposited Ta_2O_5 layer. Hf was deposited by sputtering of Hf target in an Ar atmosphere. The samples were subjected to a post-deposition annealing at 400 °C in N_2, for 30 min in order to mix the two layers and to ensure the diffusion of Hf into the matrix of Ta_2O_5, resulting in an 8-nm-thick final layer. Top electrodes of MOS structures were formed by sputtering of TiN, W and Ag in an Ar atmosphere. Fabrication sequence ended with post metallization annealing in forming gas at 450 °C for 1 h. Square gates for MIS capacitors with an active area of 2.5×10^{-3} cm^2 were defined by photolithography.

C_p–V and G–V characteristics (parallel mode) and C–V and R_s–V characteristics (serial mode) were measured in the voltage range from −1.5 V to +0.5 V at frequencies ranging from 1 kHz to 1 MHz with the use of a HP 4284A LCR meter.

4. Results and analysis

4.1. C–V and G–V characteristics

C–V and G-V characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures measured in parallel mode at signal frequencies ranging from 1 kHz to 1 MHz are shown in Fig. 3. It is seen

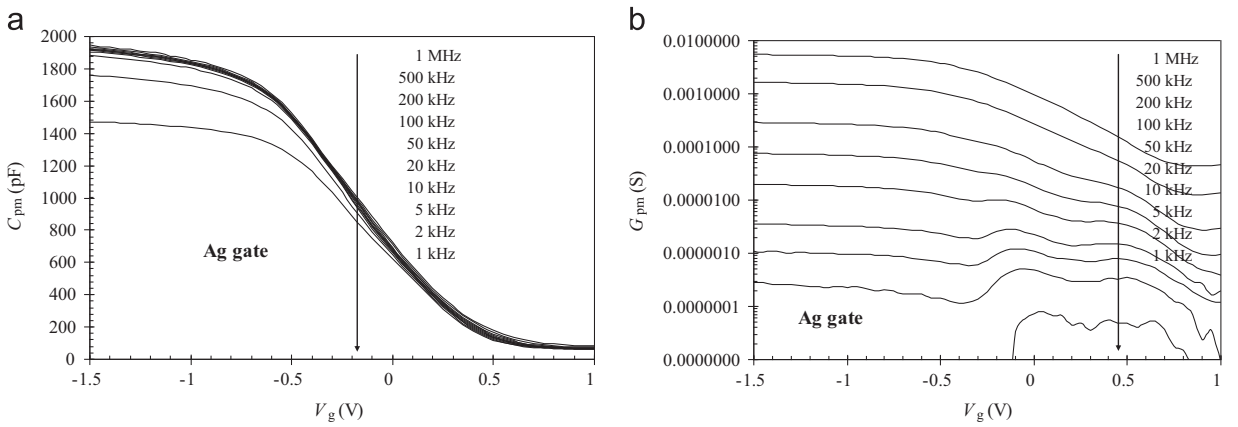

Fig. 3. *C–V* (a) and *G–V* (b) characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures measured in parallel mode at signal frequencies ranging from 1 kHz to 1 MHz.

that the frequency dispersion of the *C–V* characteristics (a) is significant, particularly at highest frequencies. In addition, it is seen that *G–V* characteristics (b) are critically distorted by the effect of leakage currents. Thus, it is practically impossible to use *G–V* characteristics for further calculations. Results for the cases of the other two gate metals (TiN, W) are similar and hence they are not shown here.

C–V and *G–V* characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures measured in serial mode at signal frequencies ranging from 1 kHz to 1 MHz are shown in Fig. 4. It is seen that the frequency dispersion of the *C–V* characteristics (a) is much smaller than in the case of parallel measurement mode. *G–V* characteristics (b) exhibit clear maxima for all signal frequencies in the range. However, these maxima are not enough sharp as in the case of thicker oxides, due to the effect of serial resistance. Thus, it is possible to use *G–V* characteristics for further calculations, but significant errors are expected to be present. Results for the cases of the other two gate metals (TiN, W) are similar and hence they are not shown here.

Next, correction for the serial resistance described in Section 2.1 was done. Corrected *C–V* characteristics are quite close to those obtained for the serial mode for all three gate metals and hence they are not shown here. The figure for corrected *C–V* characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures is practically the same as Fig. 4a. From this we conclude that the frequency dispersion observed in *C–V* characteristics for parallel mode (Fig. 3a) is mainly an artefact due to the presence of a series resistance in the circuit. Therefore, serial measurement mode is much more appropriate for analysis than the parallel mode.

Corrections are quite often not indispensable for obtaining only *C–V* characteristics if high precision is not required. However, for *G–V* characteristics, these corrections are rather important. As is shown in Fig. 5 for selected corrected *G–V* characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures, sharp maxima are obtained for gate voltages between 0 V and −1 V, while the values in strong accumulation and inversion are tending to zero. *G–V* characteristics for other frequencies exhibit the same patterns, but they are not shown in order to make the figure clear. Quite similar behavior was observed in the case of TiN and W gated structures.

4.2. Determination of interface state densities

As it was mentioned above, the main interest of this work is the determination of the interface state densities. In all the cases considered, the surface potential values were determined from the corrected *C–V* characteristics obtained at 0.1 MHz.

In the case of Terman's method, corrected *C–V* characteristics obtained at 0.1 MHz were used. While using any other frequency in the range 1 kHz to 1 MHz quite similar results are obtained. In the case of high-low method (Section 2.9), corrected *C–V* characteristics for 10 kHz (low frequency) and for 1 MHz (high frequency) were used.

In the conductance method using G_{ps}/ω–*V* curves, corrected *C–V* characteristics for 1 MHz were used. In the case of conductance method using G_{ps}/ω–ω curves, the entire set of corrected G_{ps}/ω–*V* characteristics for various frequencies was used. A matrix containing rows of G_{ps}/ω values for each frequency was constructed. Then, the G_{ps}/ω–ω table for each value of the gate voltage was constructed using the row corresponding to the given value of gate voltage as one with the set of frequency values. To illustrate the result of this procedure, in Fig. 6 the G_{ps}/ω–*f* curves for two given gate voltages are shown. As is seen in Fig. 6, these maxima are not well pronounced. In some cases the maxima are not clear and for some other cases maxima cannot be detected. This is the reason why in next figures many points for G_{ps}/ω–*f* curves are missing. In addition, for such a large frequency range (three orders of magnitude), the variations of the gate voltage are small (only about 0.3 V), and hence the corresponding surface potential variations are also narrow. Therefore, we conclude that this method even with good quality samples and attentively applied corrections is not enough robust to be exploited for determination of the distribution of interface state densities in the entire silicon bandgap.

In Fig. 7 the interface state densities determined by all four different methods described in Section 2 are shown for each of the three gate metals.

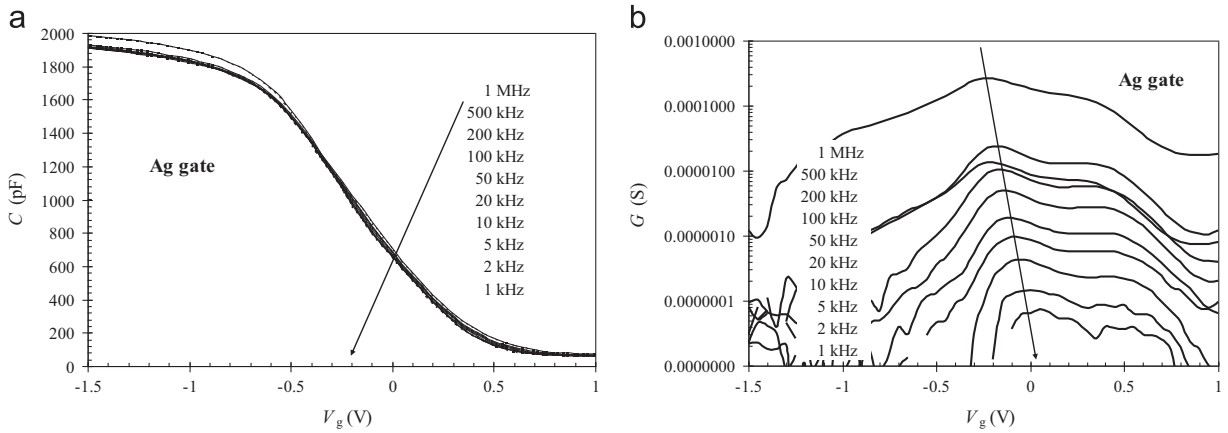

Fig. 4. *C–V* (a) and *G–V* (b) characteristics of Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures measured in serial mode at signal frequencies ranging from 1 kHz to 1 MHz.

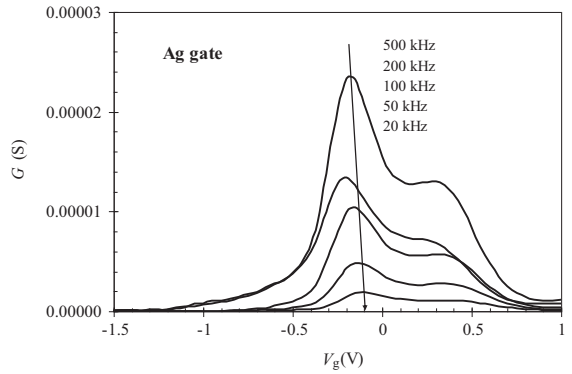

Fig. 5. Corrected admittances calculated from serial mode Ag (clear maxima are observed).

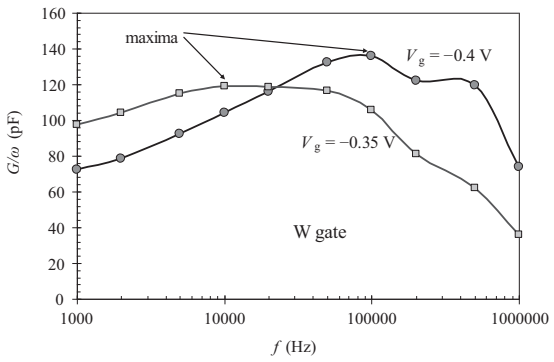

Fig. 6. $G_p(\omega)/\omega$ versus frequency f for Ag–Hf:Ta_2O_5–SiO_xN_y–Si structures at different two gate voltages: −0.35 V and −0.4 V.

Most important finding to be emphasized is that for each of the structures all four different methods give close values of the interface state density at midgap: from 2×10^{11} cm^{-2} eV^{-2} to 4×10^{11} cm^{-2} eV^{-2} in the case of an Ag gate, from 2×10^{11} cm^{-2} eV^{-2} to 6×10^{11} cm^{-2} eV^{-2} in the case of a TiN gate, and from 8×10^{11} cm^{-2} eV^{-2} to 1.5×10^{12} cm^{-2} eV^{-2} in the case of a W gate. Therefore, all the methods can be equally used in the determination of the dominantly used description of the interface states by their density at the silicon midgap.

It is seen that conductance method using G_{ps}/ω–ω curves gives results only for a restricted par of the bandgap about 0.3 eV large, close to the flatband. In order to obtain values for the entire bandgap, much larger range of signal frequencies has to be used. Since this will introduce additional sources of error, it appears to be not productive for a compact method of determination of interface states.

Other three methods give values covering large portion of the bandgap. Between them, the conductance method using G_{ps}/ω–V curves covers smallest part of the bandgap. Both this method and the high-low method give unrealistic decrease of D_{it} in the strong inversion region. Sharp increase of D_{it} values towards the conduction band edge appears in the results of all the methods.

It is to be noted that the conductance method using G_{ps}/ω–V curves, the conductance method using G_{ps}/ω–ω curves and the high-low method give similar D_{it} values for the parts of the bandgap where they appear. Therefore, they can be equally used in determination of the interface states density distribution over the bandgap. It appears that the high-low method gives results covering largest part of the bandgap. However, it is to be taken into account that the values obtained in strong inversion are not reliable and have not to be used in final presentations of the results.

It is particularly significant that in the central part of the energy gap, fairly distant from the band edges, all these three methods give similar values. Thus, for the Ag gate, the value $D_{it}\approx2\times10^{11}$ eV^{-1} cm^{-2} is obtained. In the case of TiN gate $D_{it}\approx5\times10^{11}$ eV^{-1} cm^{-2}, while for W gate the highest value $D_{it}\approx1\times10^{12}$ eV^{-1} cm^{-2} is obtained. Above values are in accordance with the results for leakage current characteristics of here studied structures. Namely, as it was reported in [14], lowest leakage currents are obtained for Ag-gated capacitors and highest for TiN-gated capacitors. Therefore, it can be affirmed that Ag-gated structures possess very low density of both bulk and interfacial defects. With the observed extremely low leakage currents (0.1 μA/cm^2 at −3 V), low oxide charge (3×10^{11} cm^{-2}), flatband voltage of −0.03 V for p-type substrate [14] and fairly low interface state densities (2×10^{11} eV^{-1} cm^{-2}),

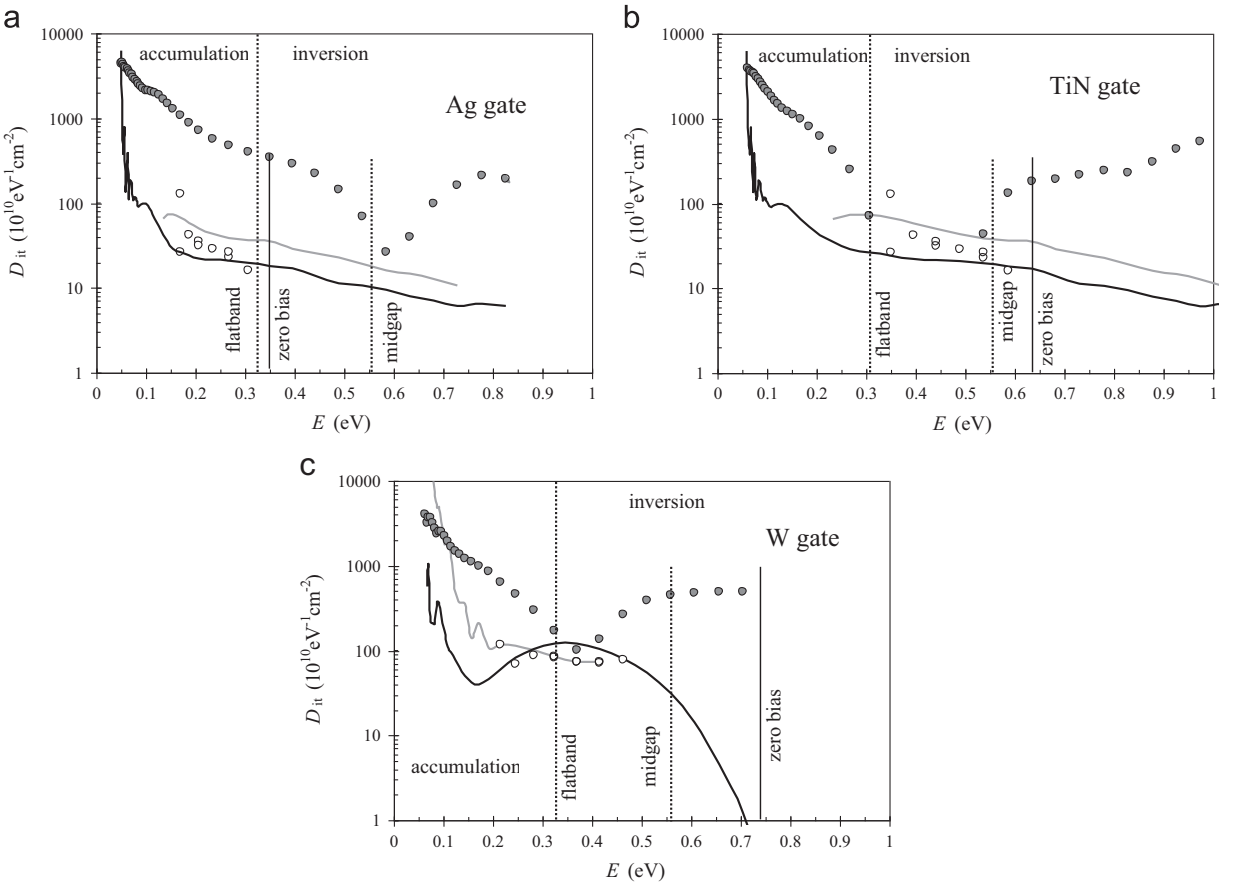

Fig. 7. Distribution of interface state densities (D_{it}) over the silicon bandgap energy values (E) for metal–Hf:Ta_2O_5–SiO_xN_y–Si structures, as obtained by four different methods: high-low method (black line), conductance method using G_{ps}/ω–ω curves (gray line), conductance method using G_{ps}/ω–V curves (empty circles) and Terman's method (gray filled circles). Gate metals are: Ag (a), TiN (b) and W (c).

$Ag-Hf:Ta_2O_5/SiO_xN_y-Si$ structures of equivalent oxide thickness of approximately 4 nm exhibit very good properties for microelectronics applications.

It is particularly interesting that the Terman's method gives D_{it} values over almost entire bandgap. Besides, the expected U-shaped distribution is observed in all cases studied here [25]. Nevertheless, the obtained D_{it} values are consistent with values obtained by other three methods only in the proximity of the midgap. Substantial difference of almost two orders of magnitude compared to other methods is observed in other parts of the bandgap.

The above finding can be explained as follows. At low voltages interfacial layer acts as a particularly good insulator, since the dominant conduction mechanism in it is the direct tunneling resulting in negligible current densities for films thicker than 2 nm. Dominant conduction mechanism in high-k Hf:Ta_2O_5 layer is Poole–Frenkel field enhanced emission from traps leading to small but perceptible currents in the case of nanosized (thinner then 10 nm) films. Equivalent circuit for such a structure is shown in Fig. 8a). For static voltages circuit reduces to the one shown in Fig. 8b) and for high frequencies to the circuit shown in Fig. 8c). When applying d.c. bias, interfacial capacitor (C_{if}) is charged through the serial resistance (R_{hk}) up to the voltage V_{ox}. Thus, at the same time with charging interface states at the interface of the dielectric with the substrate, the interface between the high-κ and the interfacial layer (internal interface) is also charged. While measuring high frequency C–V characteristics, the stacked dielectric capacitor behaves as a serial connection of capacitors (Fig. 8c).

As a result, surface potential in the silicon substrate is modified both by the charges on interface states in the dielectric close to the substrate and by the charges on the internal interface. Therefore, the Terman's method does not give interface states capacitance itself (C_{it}), but the sum $C_{it}+C_b$, where C_b is the capacitance corresponding to the charging of the internal interface. Capacitance C_b can be obtained by multiplying the capacitance C_{if} by the relative position of the charge centroide relative to the gate, $(d_{eq}-d_{if})/d_{eq}$, where d_{if} is the interfacial layer thickness ($\varepsilon_{if}\approx\varepsilon_{so}$). For our samples, $d_{eq}\approx 4$ nm, $d_{eq}\approx 2.5$ nm and $C_{if}/S\approx 4$ nF/$(2.5\times10^{-3}\ \mathrm{cm}^2)\approx 1.6\times10^{-6}$ F/cm^2. Finally, the estimated value of the additional capacitance is

$$C_b=\frac{d_{eq}-d_{it}}{d_{eq}}C_{if}\approx\frac{4-2.5}{4}\cdot 1.6\times10^{-6}\frac{\mathrm{F}}{\mathrm{cm}^2}\approx 6\times10^{-7}\frac{\mathrm{F}}{\mathrm{cm}^2}. \quad (24)$$

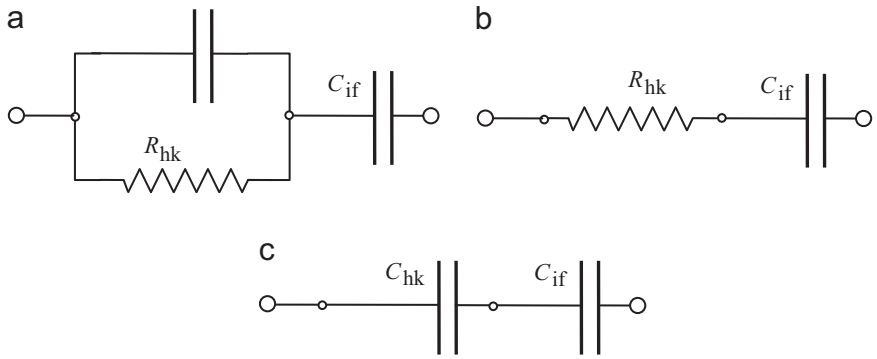

Fig. 8. Equivalent circuit of the stacked dielectric capacitor (a) and its static (b) and high frequency limit (c) cases.

Above corresponds to an extra fake value in the determined interface state density of about

$$\delta D_{it} = \frac{C_b}{q} \approx \frac{6 \times 10^{-7}}{1.6 \times 10^{-19}} \text{eV}^{-1}\ \text{cm}^2 \approx 4 \times 10^{12}\ \text{eV}^{-1}\ \text{cm}^2. \quad (25)$$

The above value is quite close to the values obtained here using Terman's method. Therefore, the above described charging mechanism accounts quantitatively very well for the observed discrepancy between the D_{it} values obtained by different methods.

At surface potentials close to the midgap such a charging of the internal interface is negligible and the obtained D_{it} values are similar to the values obtained by the other methods. Consequently, Terman's method is not appropriate for determining interface state densities of nanosized high-k stacked dielectrics, except for the midgap value.

5. Conclusions

Compact analytical methods for determination of the interface state densities of metal-insulator-silicon structures containing ultrathin dielectrics can be constructed. Four methods discussed in this work are: high-low method, conductance method using G_{ps}/ω–ω curves, conductance method using G_{ps}/ω–V curves and Terman's method. Detailed study of the metal(Ag,TiN,W) − Hf: Ta_2O_5/SiO_xN_y − Si structures has been done. Our results on other similar structures containing high-k dielectrics confirm the findings observed here for some specific structures.

First, it is found that the serial measurement mode (C_p–R_s) is more suitable for use than the parallel mode (C_p–R_p or C_p–G). Thus obtained capacitance values can be used in majority of the cases without further corrections. Using the correction method for serial resistance, as described in Section 2.1, substantial improvement of the results for G is obtained.

Determination of the capacitance in accumulation can be efficiently done using the Kar's method of extrapolation, as described in Section 2.2. This method gives results in particularly good agreement with the values obtained by using numerical quantum mechanical simulators.

It is found that at midgap all four considered methods give similar values. Therefore, they can be equally used for determination of the most frequently used midgap value of the interface state density.

Terman's method appears to give substantially erroneous values of D_{it} for energies other than that of the midgap, owing to the charging of the internal interface between the higk-κ layer and the interfacial SiO_xN_y layer. Nevertheless, thus obtained value gives a real integral measure of the variation of charges in the dielectric influencing the surface potential in the substrate, and hence is important for the description of the functioning of devices based on such metal-insulator-silicon structures.

Acknowledgments

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