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Determination of the interface state density of the In/p-Si Schottky diode by conductance and capacitance–frequency characteristics

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Abstract

The electrical characterization of the In/p-Si Schottky diode has been investigated by conductance and capacitance–frequency techniques. The characteristic parameters of the interface states have been determined from the capacitance–frequency and conductance–frequency measurements. The capacitance of the In/p-Si Schottky diode decreases with increasing frequency. The increase in capacitance at lower frequencies results from the presence of interface states. The peak observed in the conductance curve of the In/p-Si diode indicates the presence of an interfacial layer in the In/p-Si Schottky barrier. The interface-state parameters, interface-state density D_{it} and relaxation time τ of the In/p-Si diode were calculated. The interface-state density was found to vary from $7.82\times10^{12}\,eV^{-1}\,cm^{-2}$ in $(0.53-E_v)\,eV$ to $8.01\times10^{12}\,eV^{-1}\,cm^{-2}$ in $(0.28-E_v)\,eV$. Furthermore, the relaxation time was found to vary from $4.543\times10^{-8}\,s$ in $(0.53-E_v)\,eV$ to $4.435\times10^{-8}\,s$ in $(0.28-E_v)\,eV$.

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Keywords: Schottky diode; Interface state density; Conductance

1. Introduction

Schottky barrier diodes have been intensively investigated because of their technological applications [1–4]. Many Schottky barrier diodes are not intimate metal–semiconductor contacts but have, instead, a metal-interfacial layer-semiconductor (MIS) structure unless specially fabricated. A Schottky barrier diode possesses a thin interfacial native oxide layer between the metal and the semiconductor. The existence of such an insulating layer converts the device to an MIS diode, which may have a strong influence on the diode characteristics and may also change the interface-state charge with bias, which will give rise to an additional field in the interfacial layer [4]. Therefore, the non-ideal behavior observed in electrical characteristics of Schottky barrier diodes has been generally attributed to the effect of interface layer properties [5–7]. It causes the interface-state density D_{it} and the relaxation time obtained from admittance spectroscopy to become different from the values that would be expected [7–12]. In general, the C–f and G–f plots in the idealized case are frequency independent [9–14]. However, this idealized case is often disturbed due to the presence of interface states at the interfacial layer and semiconductor interface [9–14].

In our previous study [3], the temperature-dependent barrier characteristics of inhomogeneous In/p-Si Schottky barrier diode has been investigated. The value of the ideality factor, higher than unity for the diode studied, indicates the presence of interface states, which play an important role in the determination of the characteristic parameters of the diode. In such a case, the determination of the interface states cannot be ignored. Furthermore, the interface states affect the performance of the diode studied. Thus, the main aim of this study is to determine the interface state parameters of the In/p-Si having an MIS structure for its technological applications. In the present

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paper, we report the electrical characterization of a In/p-Si Schottky diode using capacitance–frequency (C–f) and conductance–frequency (G–f) measurements to obtain valuable information about the interface states.

2. Theoretical background

The interface-state conductance and capacitance of an MIS structure are expressed as [13]

$$C_{ss} = \frac{SqD_{it}}{\omega\tau} \operatorname{arc}\, tg(\omega\tau), \tag{1}$$

$$\frac{G_{ss}}{\omega} = \frac{SqD_{it}}{2\omega\tau} \ln(1+\omega^2\tau^2), \tag{2}$$

where D_{it} is the interface-state density, q is the electronic charge, S is the diode contact area, and τ is the time constant of interface states. The conductance measured and junction capacitance can be related to conductance and capacitance of interface states as [15]

$$G = \frac{qJ_{dc}}{kT} \frac{C_i(C_\Sigma + C_{ss})}{(C_\Sigma + C_{ss})^2 + (G_{ss}/\omega)^2}, \tag{3}$$

$$C = \frac{qJ_{dc}}{kT} \frac{C_i G_{ss}/\omega^2}{(C_\Sigma + C_{ss})^2 + (G_{ss}/\omega)^2} + C_{HF}, \tag{4}$$

where C_i is the interfacial-layer capacitance, C_{HF} is high frequency capacitance, and C_{SS} is the interface-state capacitance.

The conductance of interface states can be obtained from the exact solution of Eqs. (3) and (4) as

$$G_{ss} = \frac{qJ_{dc}}{kT} \frac{\omega^2 C_i(C - C_{HF})}{G^2 + \omega^2(C - C_{HF})^2}, \tag{5}$$

where J_{dc} is the forward-bias current density. The relation between capacitance and voltage for a Schottky diode is given by [6]

$$\frac{dC^{-2}}{dV} = \frac{2}{S^2\varepsilon_s q}\left[\frac{\varepsilon_i}{N_d(\varepsilon_i + qD_{it}\delta)}\right], \tag{6}$$

where ε_s and ε_i are the dielectric constants of semiconductor and interfacial layer, respectively and δ is the thickness of interfacial layer.

3. Experimental

The semiconductor substrate used in this study was p-type Si, with a (1 0 0) surface orientation, 280 μm thick and 0.8 Ω cm resistivity. The Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of H_2SO_4, an H_2O_2, 20%HF, a solution of $6HNO_3$:1HF: $35H_2O$, 20%HF. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of 18 MΩ cm resistivity. Immediately after surface cleaning, high-purity aluminum (Al) metal (99.999%), with a thickness of 2000 Å, was thermally evaporated onto the whole back surface of the wafer at about 1×10^{-7} Torr. Then, a low-resistivity ohmic contact was followed by a temperature treatment at 500 °C for 3 min in N_2 atmosphere. Schottky contact was formed by evaporation of indium (In, 99.999%) dots with diameter of about 1.0 mm (diode area = 1.76×10^{-2} cm^2). Metal layer thickness was monitored with the help of a digital quartz crystal thickness monitor. The thickness of In film was found to be about 1500 nm. The deposition rates were about 10–20 Å/s [3]. All evaporation processes were carried out in a liquid nitrogen trapped high-vacuum system at about 1×10^{-7} Torr. The C–V and G–f measurements were performed using an HP 4192A LF impedance analyzer at room temperature at dark conditions. We have also repeated the measurements such as sample preparation, measurement and data analysis, and relative accuracy of 5% was reached for the calculations. This implies that the parameters calculated were again found with an accuracy of 5%.

4. Results and discussion

Our previous results show that the In/p-Si Schottky diode exhibits a non-ideal current–voltage behavior with an ideality factor greater than unity (1.52) [3]. This suggests that the diode is an MIS-type diode. Fig. 1 shows the capacitance–frequency curves of the In/p-Si diode at different bias voltages. The capacitance decreases with increasing frequency. The increase in capacitance at lower frequencies results from the presence of interface states. The interface states at lower frequencies follow the alternating current signal, whereas, at higher frequencies, interface states are constant as they cannot follow the AC

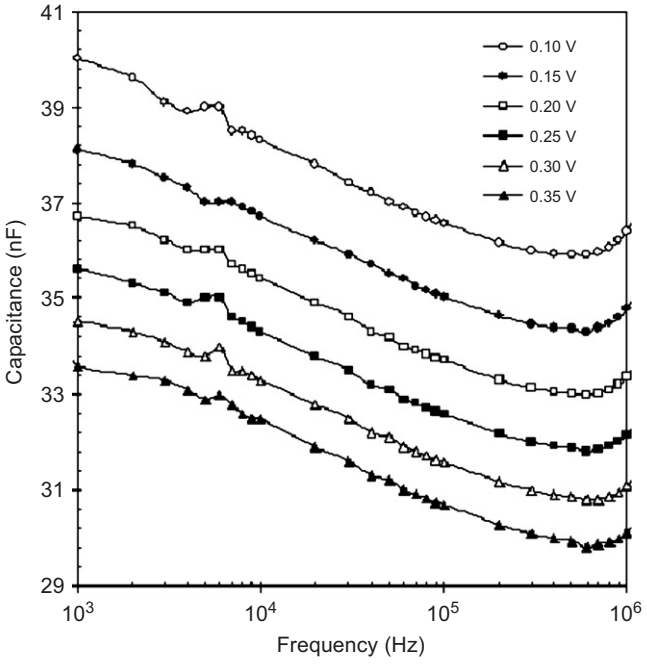

Fig. 1. Plots of capacitance vs. frequency of the In/p-Si Schottky diode at different biases.

signal. This suggests that the contribution of interface-state capacitance to total capacitance, which is small, may be ignored [14]. The capacitance increases with decreasing frequency as the traps start to respond to the signal. But at higher frequencies, traps can no longer respond. The C^{-2} vs. V curves at different frequencies were plotted (Fig. 2). A linearity in the curves was observed and this linearity in $C^{-2}(V)$ curves is due to uniform distribution of interfacial states density D_{it}. The capacitance of the In/p-Si diode at different frequencies is dependent on the voltage applied.

The density of interface state and interface state time constant can be obtained via conductance technique. The conductance G dependence of frequency at different biases is shown in Fig. 3. Fig. 3 shows two regions, which are low- and high-frequency regions. At lower frequencies, the conductance is almost constant and is similar to direct current (DC), conductivity whereas at higher frequencies, the conductance corresponds to alternating current conductance (AC), in which the conductance rapidly increases with increasing frequency. It is evaluated that the second region is characteristic of trapped carriers hopping between filled and empty states at the Fermi level. The incorporated atoms in the thin interlayer at metal–semiconductor interface act as additional impurities in the disordered layer. Thus, hoping conductance mechanism through this layer takes place and can be expressed as [16]

$$G(f) \propto f^{p}, \tag{7}$$

where p is a constant, which is a measure of number carriers that are free [17]. p value is determined from the slopes of curves shown in Fig. 3. In order to obtain p value, $\ln G$–$\ln f$ data is fitted by a polynomial form,

$$\ln G(f) = a + b\ln f + c(\ln f)^2. \tag{8}$$

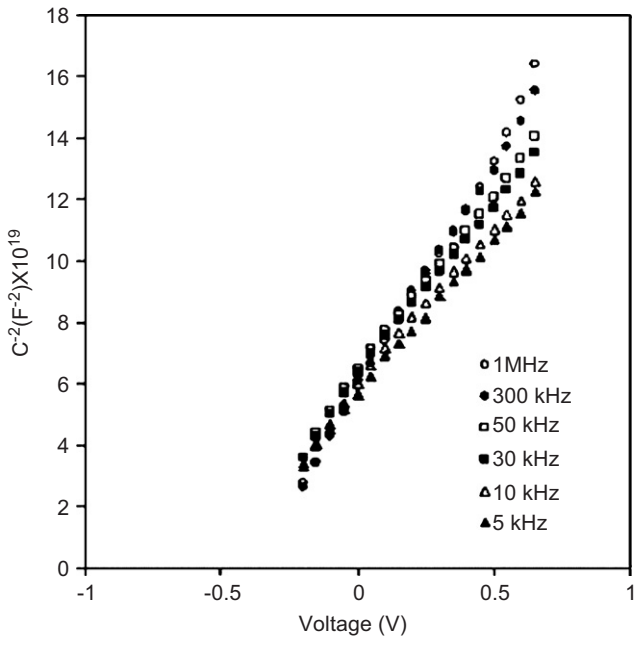

Fig. 2. C^{-2} vs. voltage plots of the In/p-Si Schottky diode at different frequencies.

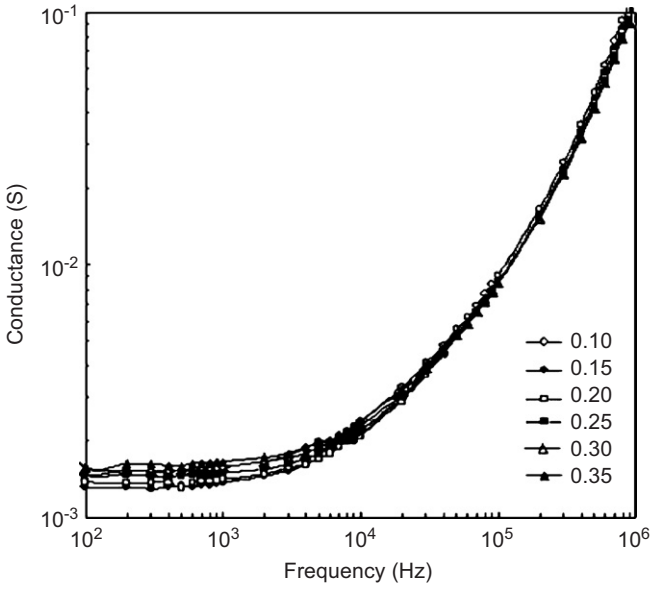

Fig. 3. The frequency dependence of conductance of the In/p-Si Schottky diode.

The slope at any f was determined by the following equation:

$$p = \frac{\mathrm{d}\ln G}{\mathrm{d}\ln f}. \tag{9}$$

By using Eqs. (8) and (9), p is determined as follows:

$$p = b + 2c\ln f. \tag{10}$$

The p value was determined from curves of conductance–-frequency shown in Fig. 3, and the conductance for the second region was expressed as

$$G(f) \propto f^{0.91}. \tag{11}$$

The p value suggests that 91% of traps are empty [17].

In order to determine interface-state parameters of the In/p-Si diode, curves of G_{ss}/ω vs. f in logarithmic scales at different biases were plotted (Fig. 4). The figures show the presence of distribution of interface state energy levels. A peak is observed in curves, and the existence of the peak verifies the presence of interface traps. The peak position and intensity change with applied voltage and the Fermi level fixes the occupancy of the interface trap levels. This indicates that traps are uniformly distributed inside the silicon gap. This method is useful in understanding of the electrical quality of interface states. The presence of interface charges affects device performance. These states will create a charge distribution at the interface, which will affect the value of capture cross sections of traps. The presence of interface charges results from different origins such as impurities, network vacancies and voids. The interface-state parameters such as interface-state density and interface trap time constant can be calculated from the results obtained [13]. At the peak observed in Fig. 4, $\mathrm{d}(G_{ss}/\omega)/\mathrm{d}(\omega\tau) = 0$ and maximum condition for Eq. (2)

gives $\omega\tau = 1.98$. D_{it} expression was obtained by substituting maximum condition value into Eq. (2) and, thus, interface-state density is expressed as follows:

$$D_{it} = \frac{(G_{ss}/\omega)_{max}}{0.402qS}. \quad (12)$$

This equation was applied to determine density of interface state and the D_{it} values are obtained given in Table 1. The interface state time for emission of electron exchange between interface states and valence band was calculated using $\tau = 1/\omega_p$ relation and, are given in Table 1. The obtained time constant for the majority of interface states is much smaller than 1 μs and thus, interface states follow 1 MHz signal and in turn, at 1 MHz, the increase of interface state density is not constant.

In a p-type semiconductor, the energy of interface states E_{it}, with respect to top of valence band at the surface of the semiconductor, is described as [14]

$$E_{it} - E_v = q\phi_b - qV, \quad (13)$$

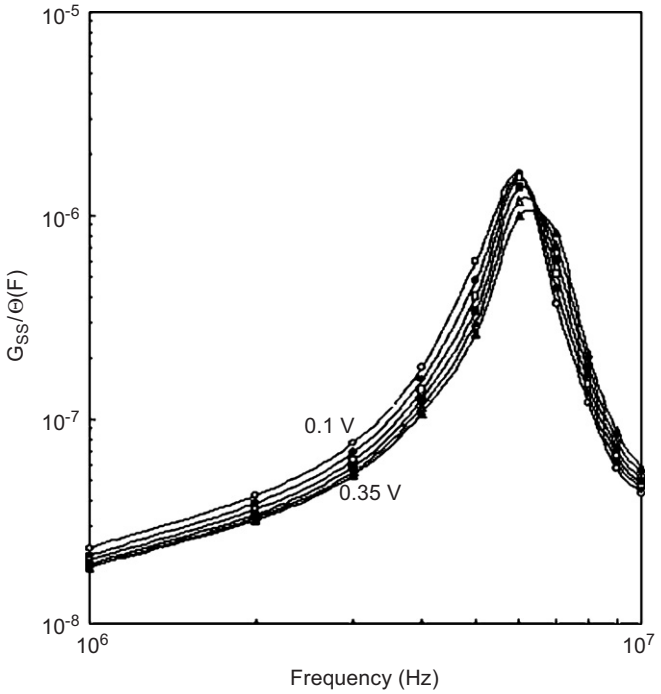

Fig. 4. G_{ss}/ω vs. frequency plots of the In/p-Si Schottky diode at different biases.

Table 1
The electronic parameters of interface-states of the In/p-Si Schottky diode

V_G (V)	$E_{it}-E_V$ (eV)	D_{it} ($eV^{-1}cm^{-2}$)	τ (s)
0.10	0.53	7.823×10^{12}	4.543×10^{-8}
0.15	0.48	7.752×10^{12}	4.420×10^{-8}
0.20	0.43	7.911×10^{12}	4.521×10^{-8}
0.25	0.38	7.856×10^{12}	4.313×10^{-8}
0.30	0.33	7.913×10^{12}	4.324×10^{-8}
0.35	0.28	8.012×10^{12}	4.435×10^{-8}

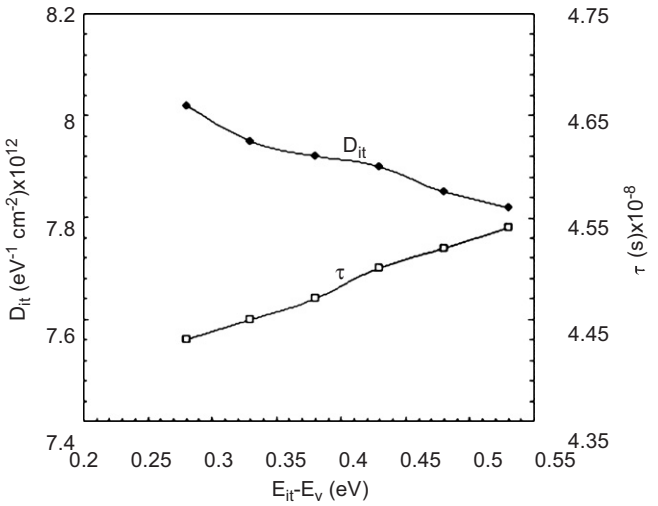

Fig. 5. Plots of D_{it} and t vs. $E_{it}-E_v$ of the In/p-Si Schottky diode.

where E_{it} is the energy of interface states, E_v is the valence band edge. $E_{it}-E_v$ values were determined using Eq. (13) and are given in Table 1. The dependence of D_{it} and τ values on E_{it}–E_v values is shown in Fig. 5 and Table 1. As seen in Fig. 5, the interface-state density was found to vary from $7.82\times10^{12}\,eV^{-1}\,cm^{-2}$ in $(0.53-E_v)$ eV to 8.01×10^{12} $eV^{-1}\,cm^{-2}$ in $(0.28-E_v)$ eV. The D_{it} values decrease with interface energy from top of valence band toward mid-gap. This verifies that the density of interface states changes with bias and each of the applied biases corresponds to a position inside the silicon gap. The obtained values D_{it} are of the same order as those reported by some authors for metal–semiconductor Schottky diodes [7–11]. It has been seen that interface-state density has an exponential rise with bias toward top of valence band. Furthermore, the interface trap time was found to vary from 4.54×10^{-8} s in $(0.53-E_v)$ eV to 4.43×10^{-8} s in $(0.28-E_v)$ eV. The interface trap time shows an exponential rise with bias toward mid-gap. This suggests that τ is bias dependent.

4. Conclusions

The interface state properties of the In/p-Si Schottky diode have been investigated by conductance and capacitance techniques. The energy distribution curves of interface states and their relaxation time have been determined from *C–f* characteristics as well as *G–f* characteristics. The ideality factor of the In/p-Si diode suggests that the diode is an MIS-type diode. The conductance and capacitance measurements verify the presence of interfacial layer between a metal and a semiconductor. The interface-state density was found to vary from $7.82\times10^{12}\,eV^{-1}\,cm^{-2}$ in $(0.53-E_v)$ eV to $8.01\times10^{12}\,eV^{-1}\,cm^{-2}$ in $(0.28-E_v)$ eV. Furthermore, the interface trap time changes from 4.54×10^{-8} s in $(0.53-E_v)$ eV to 4.43×10^{-8} s in $(0.28-E_v)$ eV.

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