

MOS Capacitance–Voltage Characteristics

III. Trapping Capacitance from 2-Charge-State Impurities*

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Abstract: Low-frequency and high-frequency capacitance–voltage curves of Metal–Oxide–Semiconductor Capacitors are presented to illustrate giant electron and hole trapping capacitances at many simultaneously present two-charge-state and one-trapped-carrier, or one-energy-level impurity species. Models described include a donor electron trap and an acceptor hole trap, both donors, both acceptors, both shallow energy levels, both deep, one shallow and one deep, and the identical donor and acceptor. Device and material parameters are selected to simulate chemically and physically realizable capacitors for fundamental trapping parameter characterizations and for electrical and optical signal processing applications.

Key words: MOS; silicon; trapping capacitance; dopant impurities; donors; acceptors

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1. Introduction

In an earlier investigation (Report I^[1]) and a current investigation (Report II^[2]) we described the presence of giant trapping capacitances in Metal–Oxide–Semiconductor Capacitors (MOSC's) due to electron or hole trapping at the donor or acceptor dopant impurity centers in the semiconductor. These trapping capacitances can significantly modify the capacitance–voltage (CV) curves of the MOS capacitor, showing up as structures (inflection points and Gaussian-like peaks) in the CV curves, because the trapping capacitance can be made very large, many times larger than the oxide capacitance, by simply increasing the trap concentration. The large trapping capacitance persists at all temperatures, with narrowing lineshape at lower temperatures. It can be easily measured routinely, in research laboratory and manufacturing setups, as experienced over half a century by the senior author.

The large magnitude of the trapping capacitance can provide unprecedented sensitivity for characterization of the fundamental electrical and optical properties of these electronic traps at the dopant and the residual or intentionally added chemical impurities, and at the residual, not annealed or intentionally created physical defects in semiconductors (point defects such as the vacancies and divacancies, and larger atomic defects, such as the dislocation lines and loops, the grain boundaries, and the planar boundaries including the SiO₂/Si and metal/semiconductor and semiconductor/semiconductor interfaces, and the clusters). The large trapping capacitance can also be utilized in integrated circuits for electrical and optical signal processing.

In the two initial reports, I and II^[1,2], we presented the computed CV curves of MOS capacitors containing only the one-electron or one-hole trap in semiconductors with only one dopant impurity species as the trapping center. At an electronic

trapping center, the electron in the conduction band or the hole in the valence band undergoes trapping, namely, sequentially and continually taking the two quantum mechanical transition steps, consisting of electron capture from, then trapped electron emitted or released back to, the conduction band of the semiconductor, or hole, the valence band of the semiconductor.

To search for and to demonstrate the conditions of large trapping capacitance, as revealed by the large structures in the capacitor-terminal-measured CV curves, hence high sensitivity for applications, in this report (III), as a computer-aided design (CAD) exercise and simulation, we followed the traditional approach used classrooms and factories, namely the Model Semiconductor, which we employed in I and II, by varying the electronic properties of the assumed impurity electronic traps, rather than using the experimentally determined electronic properties of specific impurities in a semiconductor, that is, by varying their energy levels in the semiconductor energy gap, or the binding energy of the trapped electron or the trapped hole. The numerical values of the energy levels are selected to simulate: (1) the shallow level dopant impurities in Si (See Fig. 1) at about 50 meV energy level or electron or hole binding energy (~ 10 THz, $30 \mu\text{m}^3$), such as P, As, Sb donors and B, Al, Ga acceptors, (2) the deeper level acceptor dopant impurities in Si, such as Indium (In) with a hole binding energy of ~ 150 meV (30 THz, $10 \mu\text{m}$) and Thallium (Tl) with a binding energy of ~ 250 meV (50 THz, $5 \mu\text{m}$), and (3) the still shallower dopant donor and acceptor impurities in Ge (See Fig. 2), at about 10 meV binding energy (2.5 THz, $120 \mu\text{m}$). Most of the experimentally observed impurity levels and the electronic thermal capture cross-section data in Si and Ge are shown in Figs. 1 and 2. They were collected and compiled by the senior author 50 years ago for classroom demonstrations^[4]. The precision of the experimental values of the energy levels and capture cross sections, indicated in the two figures,

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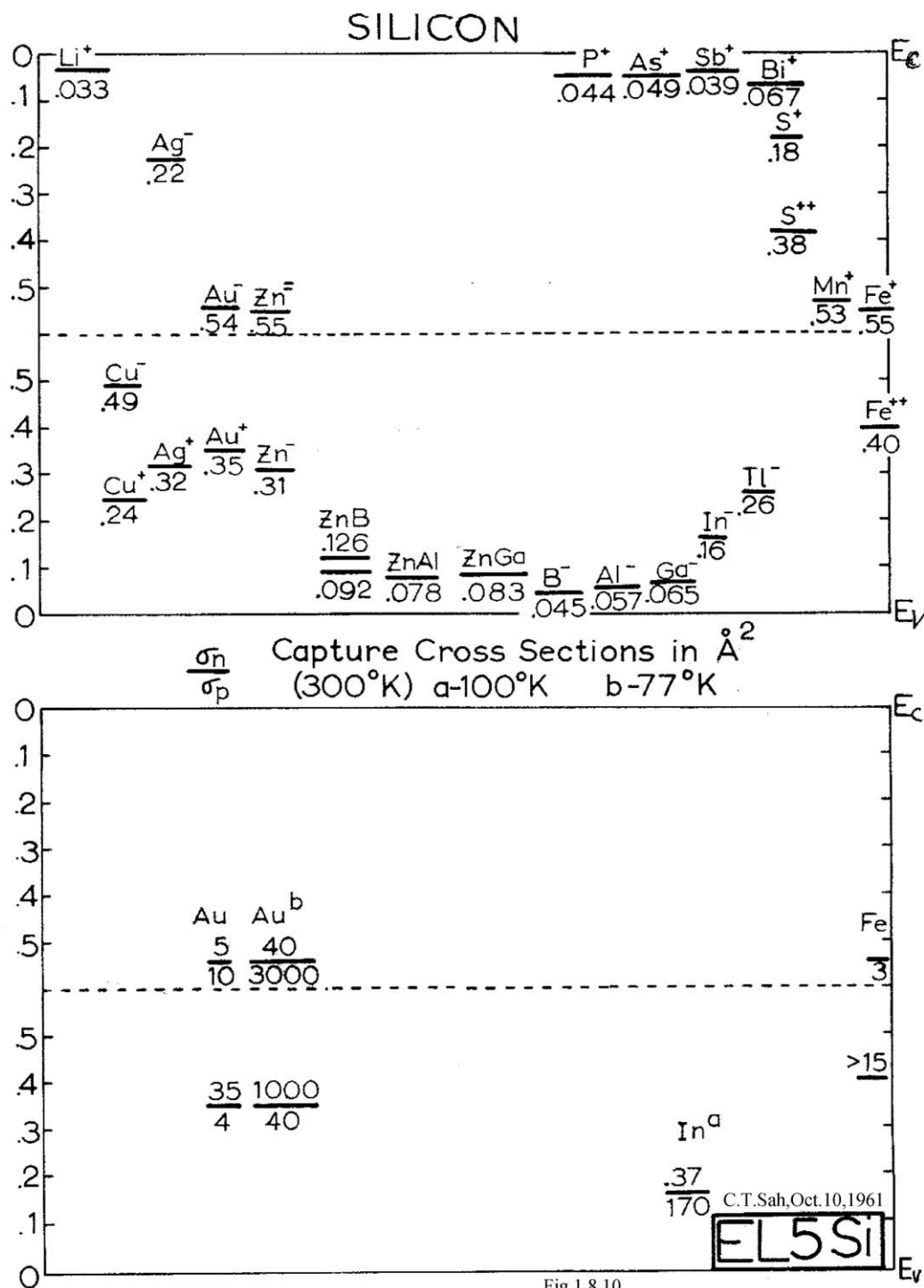


Fig.1.8.10

Fig. 1. Electronic energy levels and thermal capture cross sections (in sq. Angstrom or 10^{-16} cm^2) at impurity centers in silicon. From Chih-Tang Sah, Semiconductor Data Handbook, unpublished, October 10, 1961. Collected and composed at the Shockley and Fairchild Semiconductor Laboratories during his tenures there from 1956 to 1959 and 1959 to 1964.

have not been improved significantly due to the lack of continued experimental research, hampered and hindered by lack of grant and contract funding from the US federal agencies because the two semiconductors, Si and Ge, were classified as “well-developed” manufacturing materials, rather than those far-out exotic new materials that might have practical application potentials. Even the atomic configurations (substitutional or interstitial) of the metal impurities were uncertain, except a few non-metal impurities in Si (such as the double-donor or

two-electron trap Sulfur, and the double-acceptor or two-hole trap Zinc). These double electronic traps were used in textbook^[5-7] to illustrate the rich and fascinating electronic and quantum-mechanical phenomena of semiconductor imperfection physics, not unlike the Bohr electron model of the atoms of an earlier era.

One observation of the Gaussian-like shape of the CV curve of the electron and hole trapping capacitances, C_{nt} and C_{pt} in the previous two reports, I and II^[1,2], was their masking

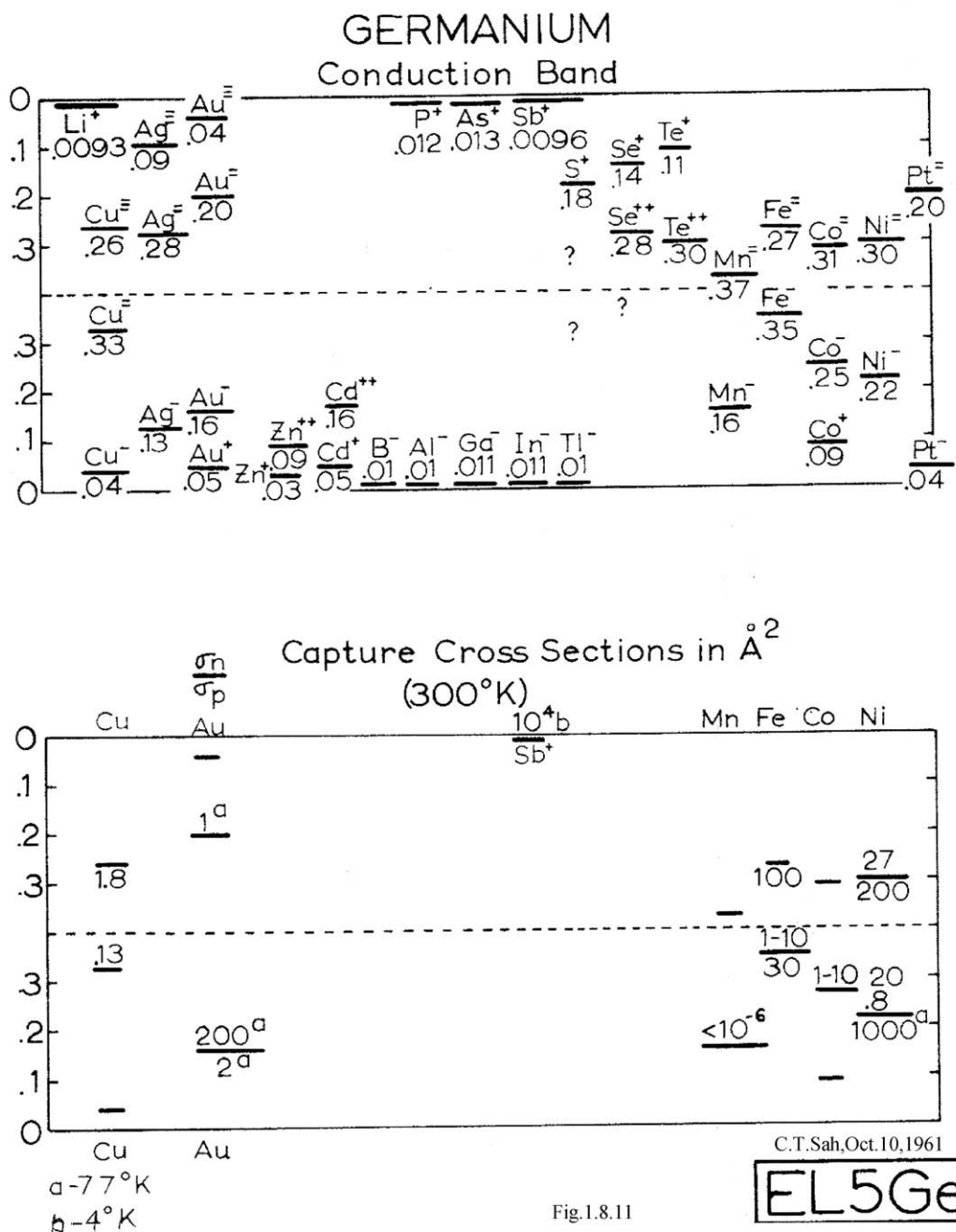


Fig.1.8.11

Fig. 2. Electronic energy levels and thermal capture cross sections (in sq. Angstrom or 10^{-16} cm^2) at impurity centers in germanium. From Chih-Tang Sah, Semiconductor Data Handbook, unpublished, October 10, 1961. Collected and composed at the Shockley and Fairchild Semiconductor Laboratories during his tenures there from 1956 to 1959 and 1959 to 1964.

in the terminal MOSCV curves by the large electron and hole charge-storage capacitances, C_n and C_p . Thus, a second purpose of this third report, III, is to discover and to illustrate the possible means to lessen this masking. In this report, we shall focus on the chemical means to lessen the masking, namely, using the simultaneous presence of a second impurity species in the MOSC, whose trapping capacitance peak lies in the majority carrier depletion and inversion gate-voltage range, which has lower majority carrier concentration while not yet much minority carrier accumulation in the silicon or semiconductor surface space-charge layer under the gate oxide, therefore, lesser masking of C_{nt} and C_{pt} by both the majority and minor-

ity carrier storage capacitances, C_n and C_p . In MOS transistor terminology, this is the subthreshold gate-voltage range. In terms of MOS physics, this is in the flatband to strong inversion surface potential range, respectively at the thermal voltage ($k_B T/q$) normalized surface potential of $U_S \equiv qV_S/k_B T = 0$ or Flatband and at $U_S = 2U_F$ which is the inversion threshold where the semiconductor surface under the gate oxide begins to become strongly inverted from the bulk conductivity type. This is twice the equilibrium (both thermal and electrical) value of the Fermi energy level (far from the interface), which is also when the minority carrier surface concentration is equal to the majority carrier bulk concentration. To illustrate, we follow the

graphic scheme employed in I^[1] and II^[2], by presenting a family of CV curves in a figure, from varying one parameter to give the family of CV curves. Three device physics points are labeled in every one of the CV curves. These are: flatband $U_S = 0$, intrinsic surface $U_S = U_F$ where $P_S = N_S$, and strong inversion, $U_S = 2U_F$ which is when $P_S = N_{DD}$ in n-Si MOSC or $N_S = P_{AA}$ in p-Si MOSC. Parameters kept constant for each CV curve include the concentration or the energy level of the second impurity species in the semiconductor body containing two impurity species.

2. Theory of Capacitance–Voltage Characteristics with Trapping Capacitance

The equations used to compute the CV curves are those given in I^[1] and II^[2], extended to MOSC's containing two impurity species, with uncorrelated and far-apart atomic locations, so their trapping capacitances are additive or in parallel. We ignore impurity bands at high impurity concentrations. In this paper, they both have just one energy-level or one trapped carrier, electron or hole, and hence two charge-states. These equations will be further detailed in a future report^[8,9 or 10] which will give the list of numerical values of the universal constants and of the characteristic electronic parameters of the traps. The computed CV curves are presented in the figures described in the following section. To provide some historical perspectives, selected CV figures similar to those given in this paper but computed 50 years ago by the senior author, such as the sample given in Ref. [2], using slide rules shown in Ref. [2], will also be presented later.

3. Computed Capacitance–Voltage Characteristics with Trapping Capacitance

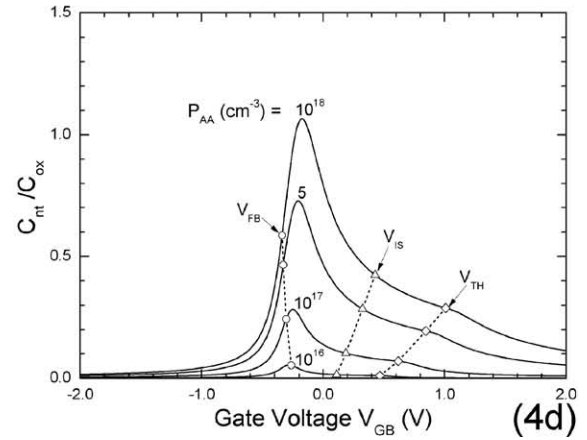
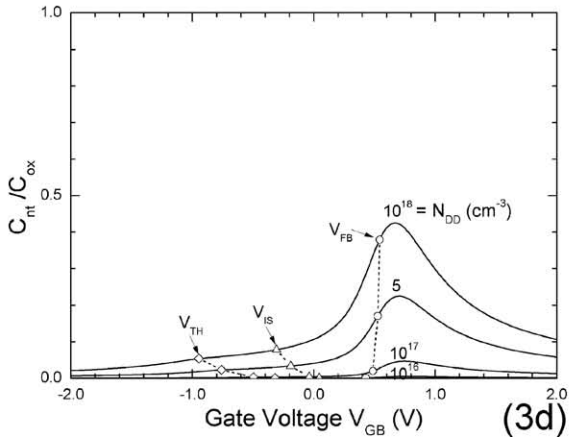
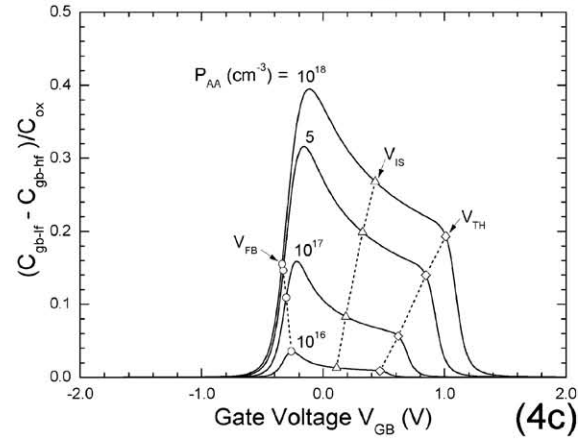
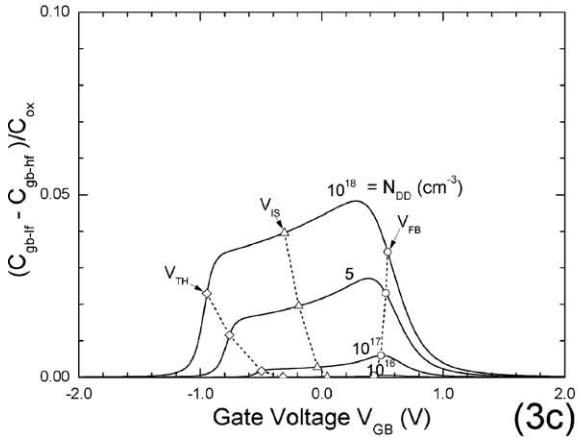
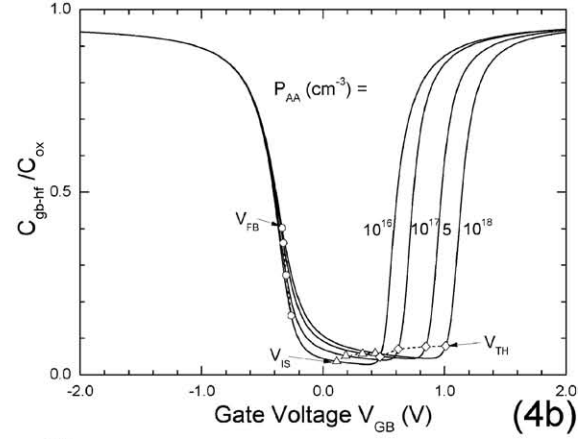
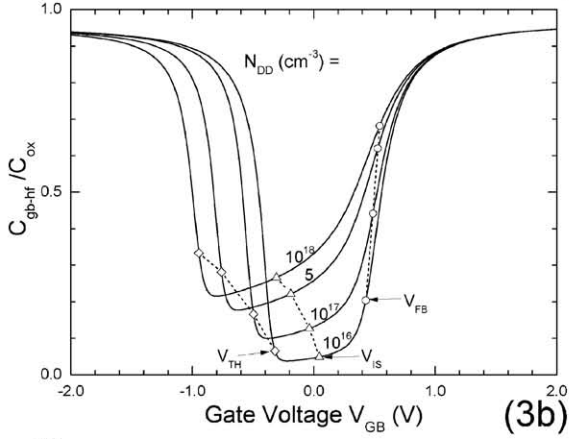
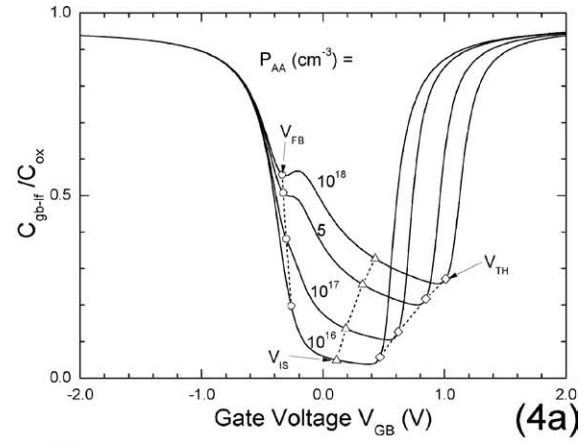
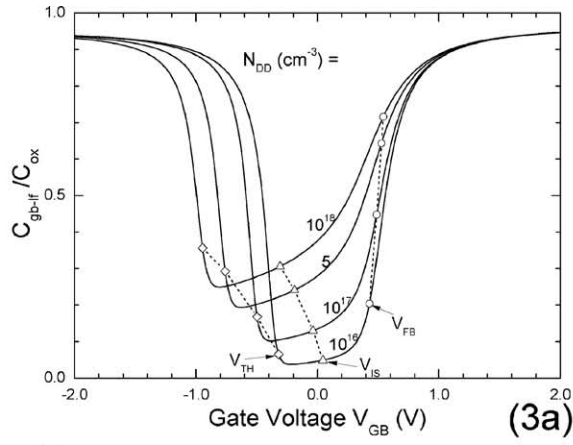
To illustrate the huge increase in the legibility or readability of the trapping capacitance in a terminal CV curve at the size of a journal page figure, via deepening the energy level or increasing the binding energy of the trapped electron or hole to place the peaks in the carrier exhaustion range from flatband to inversion, $U_S = 0$ to $2U_F$, in addition to increasing the concentration of the impurity trapping center, we first present two figures, each contains four parts or four sub-figures, with a family of CV curves in each sub-figure or part, placing the corresponding sub-figures side by side on one page, for ease of comparison. These are, in the left column, Figs. 3(a) to 3(d) of the 50 meV model for a shallow donor (P, As or Sb in Si), and in the right column, Figs. 4(a) to 4(d) of the 150 meV model for a deeper acceptor (Indium in Si, or even the deeper 260 meV Tl = Thallium in Si). It is evident^[11] from each of the four low-frequency CV curves in Fig. 3(a) that the trapping capacitance structures (inflection point or peak) from the shallow (50 meV) dopant donor (P, As or Sb in n-Si) is not legible. These feature points should appear near flatband, $V_{FB} = \sim +0.4$ V, labeled by the four hollow circles, one each on each of the four CV curves. However, in Fig. 4(a) of the MOSC's that contain the 150 meV Indium acceptor in p-Si, the trapping capacitance structure (inflection point or peak) is highly visible, near or below flatband, $V_{FB} = -0.3$ V. On the other hand, as indicated in Figs. 3(c) and 4(c), the trapping capacitance peaks do show up

clearly for both cases, in the plot of the MOS terminal capacitance difference, $C_{gb-lf} - C_{gb-hf}$, versus the terminal gate voltage, V_{GB} , of both the n-MOSC in Fig. 3(c) and the p-MOSC in Fig. 4(c). This was already illustrated in I^[1] and especially in II^[2]. These first two reports also showed that the true line-shape of the trapping capacitance itself can be obtained from the reciprocal terminal capacitance difference, defined by the identity Eq. (7) in II. These are plotted also here, in Figs. 3(d) and 4(d), showing not only the huge trapping capacitance peak but also the tiny structure at threshold, V_{TH} , and at intrinsic surface, V_{IS} , which would be amplified in the first and second voltage derivative plots, not presented here due to substantially exceeding the page limitation. One important feature to note of Fig. 3(d) is that the peaks of the 50 meV shallow donor CV curves are located beyond the flatband towards accumulation while those of the 150 meV deep acceptor in Fig. 4(d) are located between the flatband and intrinsic surface but moving beyond the flatband towards accumulation as the concentration of the 150 meV acceptor decreases below 10^{16} cm^{-3} . These markers could be used to locate the energy level of the trap by initial visual inspection of the experimental data, before theoretical least square fit or calculation using the approximate analytical formula expanded about flatband, $U_S = 0$.

Next, we use here the figure-presentation format of placing eight sub-figures or parts, (a) to (h), on one journal page for ease of observing and describing the details of the CV curves. This presentation scheme was previously used in II^[2]. In order to see the tiny inflection points and small labels of the curves, again, the figures can be greatly enlarged^[11].

Figures 5(a) to 5(h) give the first family of CV curves. These MOSC's have a high concentration of the 50 meV shallow-level phosphorus donor ($N_{DD} = 1.0 \times 10^{18} \text{ P/cm}^3$) and each MOSC is compensated by a deep-level (150 meV) indium acceptor at a concentration of $P_{AA} = (0, 2, 4, 7, 9, \text{ or } 9.9) \times 10^{17} \text{ In/cm}^3$. Figure 5(a) shows that the structure of the electron (majority carrier) trapping capacitance at the phosphorus donor electron trap, C_{nt} , is not legible, which is located around flatband, $V_{FB} \sim +0.4$ to $+0.5$ V, because it is masked by the high concentration of electrons and its high electron storage capacitance C_n . However, Figure 5(a) shows that the peak or the structure of the hole trapping capacitance, C_{pt} , at the 150 meV Indium acceptor level, is clearly evident in each of the six low-frequency CV curves. They are located slightly below or above the threshold, V_{TH} (-1.0 to -0.3 V) towards the inversion range (negative V_{GB} for these n-Si). This enhanced appearance the hole trapping capacitance, C_{pt} , is still rather small^[11] in this subthreshold gate voltage range, because this semiconductor surface space charge layer is not yet sufficiently inverted to exhaust surface layer of holes. Nevertheless, this double doping by a deeper level compensating impurity, does give an encouraging proof of leveraging the lowered majority carrier (electron) storage capacitance, C_n , in the majority-carrier (electron)-depletion gate-voltage range, where the minority carrier (hole) storage capacitance, C_p , in this hole inversion range has not yet risen to the large inversion value to mask off the hole trapping capacitance, C_{pt} .

Figure 5(b) contains the high-frequency CV curves measured at sufficiently high signal frequencies that the electrons and holes do not have enough time to be trapped, therefore, the gb or gate-body terminal high-frequency capacitance, C_{gb-hf}



Figs. 3 and 4. Comparing the 50 meV donor model in Si in parts (a) to (d) with those of the 150 meV acceptor model in Si. N_{DD} and P_{AA} are 10^{16} , 10^{17} , 5×10^{17} or 10^{18} cm^{-3} . Ground state only. Degeneracy $g_D = 2$ and $g_A = 4$. $X_{ox} = 3.5 \text{ nm}$. $T = 300 \text{ K}$.

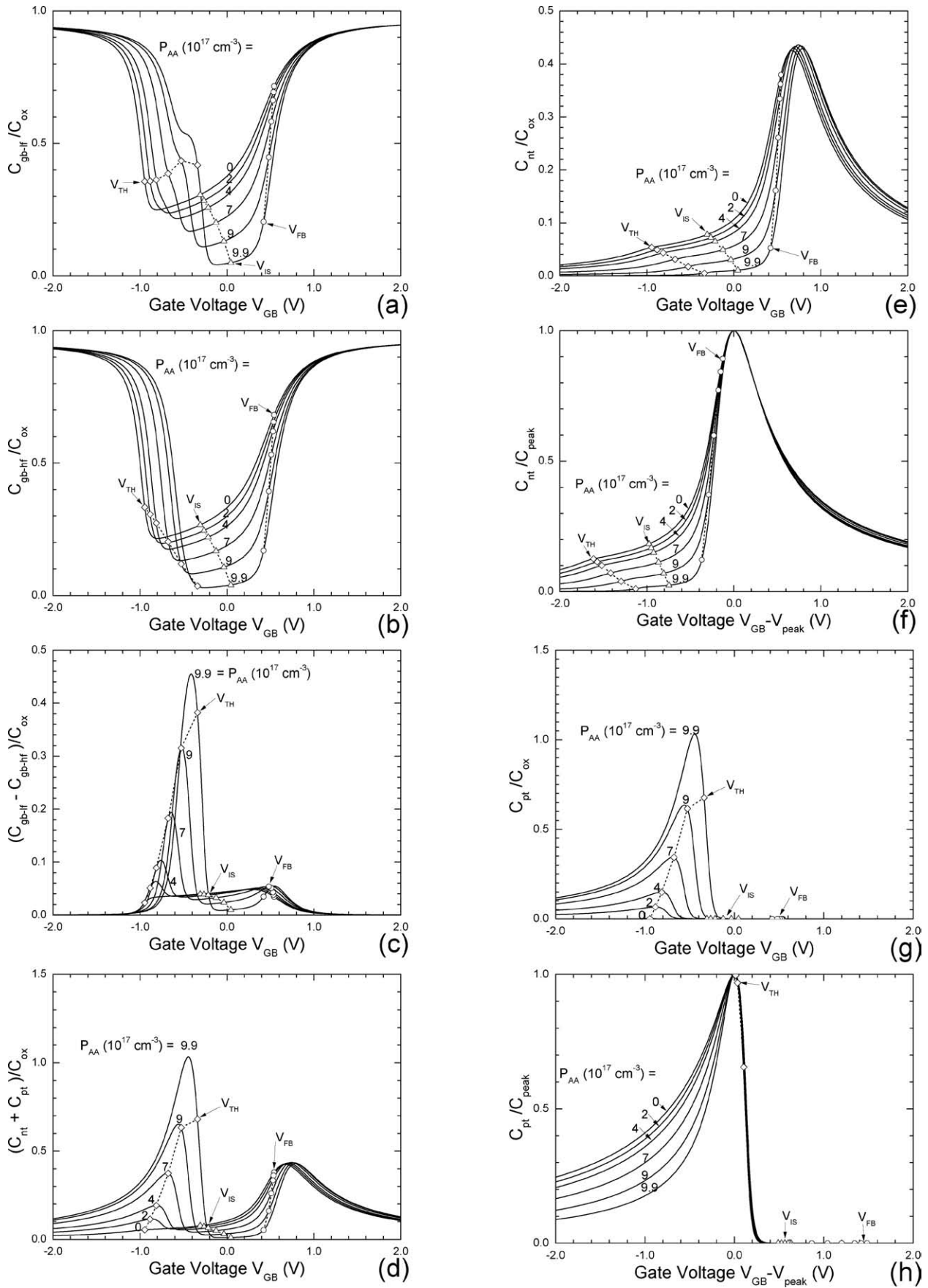


Fig. 5. Capacitance–Voltage curves of n-Si MOSCs containing a 50 meV donor and a compensating 150 meV acceptor. $T = 300$ K. $X_{ox} = 3.5$ nm. $N_{DD} = 10^{18}$ cm $^{-3}$. $g_D = 2$. $P_{AA} = (0, 2, 4, 7, 9 \text{ or } 9.9) \times 10^{17}$ cm $^{-3}$. $g_A = 4$. (a) C_{gb-lf} . (b) C_{gb-hf} . (c) $C_{gb-lf} - C_{gb-hf}$. (d) $C_{nt} + C_{pt}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

does not contain the trapping capacitances, that is, the semiconductor capacitance contains only the electron and hole storage capacitances in parallel, $C_s = C_n + C_p$. This makes the further assumption that the electrons and holes are supplied and removed instantaneously (in comparison with the measurement signal frequency) by one or more sources and drains.

The experimentally measureable difference of the low-frequency and high-frequency terminal-capacitances, $C_{gb-lf} - C_{gb-hf}$, in Fig. 5(c), and the reciprocal difference of the reciprocal high-frequency and low-frequency capacitances calculated from experimental data, which is also just the total trapping capacitances as proven in II^[2], Eq. (7) in II, in Fig. 5(d), both prominently show the presence of both the larger deeper-level minority carrier (holes) trapping capacitance, C_{pt} , near the threshold voltage V_{TH} (-1.0 to -0.3 V), and the smaller shallower-level majority carrier (electron) trapping capacitance, C_{nt} , above the flatband voltage V_{FB} ($\sim +0.5$ V). The main difference between Figs. 5(c) and 5(d) is that Figure 5(c) is reduced by the series oxide capacitance C_{ox} while Figure 5(d) is not. The individual trapping capacitances, C_{nt} and C_{pt} , are separately graphed in Figs. 5(e) and 5(g), and their magnitude normalized (to the peak) and voltage shifted (to coincide the normalized peak) CV curves are plotted in Figs. 5(f) and 5(h) for lineshape fits to experimental data. The nearly constant or compensation-independent majority carrier trapping capacitances, $\sim 0.05 C_{ox}$ near flatband $\sim +0.5$ V, of the capacitance difference in Fig. 5(c); and $\sim 0.44 C_{ox}$ above flatband $\sim +0.7$ V of both the reciprocal capacitance difference in Fig. 5(d) and individual trapping capacitance C_{nt} in Fig. 5(e); are due to the constant majority dopant donor impurity concentration used in the model, $N_{DD} = 10^{18} \text{ cm}^{-3}$, and also because the main dependence of the majority carrier surface concentration is on the surface potential, which is relatively independent of the compensation by the deeper-level (150 meV) minority dopant acceptor impurity from 0 to 99%, $P_{AA} = (0, 2, 4, 7, 9 \text{ and } 9.9) \times 10^{17} \text{ cm}^{-3}$, hence a nearly constant masking by the majority carrier storage capacitance of the majority carrier trapping capacitance. The peak difference between the terminal-capacitance-difference of $0.05 C_{ox}$ and the reciprocal-terminal-capacitance-difference of $0.44 C_{ox}$ is from the absence of reduction of the trapping capacitance by the series oxide capacitance C_{ox} in the two latter, especially in Fig. 5(e), which give the C_{nt} and its peak, without reduction from C_{ox} and without the minority carrier trapping capacitance C_{pt} .

The much larger peak from the minority carrier (holes) trapping at the deeper level (150 meV) acceptor impurity, which increases with increasing minority dopant impurity concentration over the range of $P_{AA} = (2, 4, 7, 9 \text{ and } 9.9) \times 10^{17} \text{ cm}^{-3}$, from $0.06 C_{ox}$ to $0.45 C_{ox}$ seen in the capacitance difference in Fig. 5(c) and from $0.06 C_{ox}$ to $1.06 C_{ox}$ seen in the reciprocal capacitance difference in Fig. 5(d) and in the C_{pt} itself in Fig. 5(g), is due to the smaller inversion hole concentration in the surface space charge layer that is strongly dependent on the compensation, hence lesser hole storage capacitance, C_p , that masks the hole trapping capacitance. The deeper minority trap energy level further reduces masking by the minority carrier charge storage. Figure 5(c) also shows that the rise of the difference-capacitance peak from minority carrier trapping is nonlinear, actually super-linear, with respect to the increasing compensating minority dopant acceptor impurity concen-

tration, P_{AA} . This is because the higher minority impurity doping also reduces the majority carrier concentration, further reducing the masking by the majority carrier charge storage capacitance, in addition to that by the minority carriers. This large minority carrier trapping capacitance is an important feature in applications.

We now provide a device and materials physics based estimate to reveal the origin of the differences discussed in the preceding paragraph, that of the majority and minority carrier trapping capacitance peaks, $0.44 C_{ox}$ at $N_{DD} = 1.0 \times 10^{18} \text{ cm}^{-3}$ shown in Fig. 5(e) and $P_{AA} = 7.8 \times 10^{17} \text{ cm}^{-3}$ interpolated between the $P_{AA} = 7 \times 10^{17} \text{ cm}^{-3}$ and $9 \times 10^{17} \text{ cm}^{-3}$ $C_{pt} V_{GB}$ curves in Fig. 5(g). As to be shown in the following analysis, this difference comes entirely from the different density of states used for both the electron and hole traps and the electron and hole bands, which is expected by device and materials physics. These last five of the eight sub-figures or parts, show the two trapping capacitances themselves, as a function of the applied DC gate voltage, V_{GB} , with the series C_{ox} reduction in Fig. 5(c), and no series C_{ox} reduction in Figs. 5(d), 5(e), 5(f), 5(g) and 5(h). Figures 5(e) and 5(g) are the trapping capacitance normalized to the oxide capacitance to show that the 150 meV deep acceptor in Fig. 5(g) gives a peak of $0.43 C_{ox}$ at a concentration of $P_{AA} = 7.8 \times 10^{17} \text{ cm}^{-3}$ while the 50 meV deep donor in Fig. 5(e) gives a similar peak of about $0.43 C_{ox}$ at a concentration of $N_{DD} = 1.0 \times 10^{18} \text{ cm}^{-3}$. The difference, 0.78 and 1.0, can be accounted for as follows. The trapping degeneracy factor, $g_A/g_D = 4/2 = 2$, which is a measure of the effective density of state of the trap state, and the effective density of state of the valence and conduction band, $N_V/N_C = 2.4277/5.1270 = 0.47351$ (See p.49 of Ref. [6]), combine to give a total of $(g_A/g_D) \times (N_V/N_C) = (4/2) \times (2.4277/5.1270) = 0.9470$, which accounts only for a part of this impurity concentration difference $P_{AA}/N_{DD} = 7.8 \times 10^{17}/1.0 \times 10^{18} = 0.78$. The other part comes from the closeness of the 50 meV donor level to the conduction band edge compared with the thermal energy, $k_B T = 25.85 \text{ meV}$, which lowers the trapped electron concentration because of thermal excitation to the conduction band, by the ratio of the Boltzmann factors (trap occupation factors should be used) of $\exp(-50/25.85) = 0.1445$, giving $0.9470 \times (1 - 0.1445) = 0.8102$ which is within 3% from the peak trapping capacitance ratio of 0.78 just read off the expanded CV curves of Figs. 5(d) and 5(g). Figures 5(f) and 5(h) are both peak-normalized and peak-voltage-shifted to show their line-shapes for visual evaluation of the experimental CV curves. The above physics-based (density of states) back-of-the-envelope estimate, of course, can be obtained exactly by analytical expansion to get the formulas of the peak capacitance, $\partial C_t / \partial V_{GB} = 0 = (\partial C_t / \partial U_S) / (\partial V_{GB} / \partial U_S)$ or $(\partial C_t / \partial U_S) = 0$, which then gives the analytical dependence of the factors we just used to make the estimate of the size of the trapping capacitance peak.

In view of the results of Figs. 5(a) to 5(h), and the thorough physics understanding of the fine structures in the CV curves, just described in the preceding paragraphs, we then ask the question to further enhance the application potentials: Does the compensation scheme also work when the compensating impurity is also a shallow level impurity? This is important because such compensation is a common occurrence in transistor

structures. In addition, the shallow levels would also cover the far infrared and sub-millimeter-wave ranges of applications, as Shockley's prophetic Nomogram of the Energy Conversion Chart of 60 years ago was anticipating^[3]. For examples, boron in the phosphorus doped (or diffused or implanted) n-type silicon (n-Si), or phosphorus in boron doped (or diffused or implanted) p-Si, could leverage the trapping capacitance as the transducer at the 50 meV energy or 25 μm wavelength and 12 THz frequency electromagnetic as well as optical electronics. The answers are given by the computed CV curves of n-Si compensated by p-impurity, displayed in Figs. 6(a) to 6(h), with $N_{\text{DD}} = 1.0 \times 10^{18} \text{ P/cm}^3$ and $N_{\text{AA}} = (0, 0.1, 0.2, 0.5, 0.7, 0.9, \text{ or } 0.99) \times 10^{18} \text{ B/cm}^3$. The results are self-explanatory based on the descriptions just given for the corresponding eight part Figs. 5(a) to 5(h) in the preceding two paragraphs. Yes, indeed it does work and the descriptions of the magnitude and the location (gate voltage) of the peaks due to the trapping capacitances do follow the descriptions given in the preceding paragraphs for the corresponding eight parts of Fig. 5, Figs. 5(a) to 5(g), including two factors: (i) the lower minority (hole) trapping capacitance peak due to the shallower hole trap here at 50 meV so some of the trapped holes are thermally excited to the valence band, which was a power of 3 (from 150 meV/50 meV = 3) smaller at the deeper 150 meV in Fig. 5 and (ii) the difference of density of state of both the band and trap electrons and holes.

To make the above complete, we also computed the CV curves with the donor and acceptor of Fig. 6 interchanged, namely, p-Si MOSC with an 50 meV acceptor, compensated by an 50 meV donor. These are shown in the eight-part Figs. 7(a) to 7(h). Their fine structures, the inflection points and peaks^[11], are nearly mirror image of those obtained for the n-Si MOSCs shown in Figs. 6(a) to 6(h) just described. The difference in detailed CV shape arises from the differences in density of state between the trapped and band electrons and the trapped and band holes. These two results, shown in the 8-part Figs. 6 and 7, could be especially important in applications employing the electron trapping capacitance at the shallow-dopant donor impurities in silicon containing P, As, and Sb donor dopant impurities, and its counterpart of hole trapping capacitance, which are used in npn and pnp bipolar transistors and n-channel and also p-channel MOS field-effect transistors.

Because the voltage location of the trapping capacitance peak is roughly scaled with the depth of the trap energy level, we then ask a second question. Can the doping with a second impurity species of the same conductivity type as that of the majority impurity species but deeper in energy level, bring out prominently the trapping capacitance of the second impurity species or the trapping capacitance of both of the two impurity species? This corresponds to the physical realizable case of p-Si doped, diffused, or/and ion-implanted with two acceptor species, the shallow-level boron (or Al or Ga) at 50 meV and the deep-level Thallium (Tl) at 260 meV (or the more common, and not toxic, but not as deep and not as large in atomic size Indium acceptor at 160 meV which has been used to strain the surface channel in sub-100-nm Si p-MOS transistors in order to increase the hole mobility in the surface channel). This also corresponds to the physical realizable case of n-Si doped, diffused or/and implanted with the shallow-level donor (P, As, Sb) at 50 meV and the deep-level donor Bi at 70 meV. The answers are given in Figs. 8(a) to 8(d) for the 2-acceptor doped

p-Si at 50 meV and 260 meV and in Figs. 9(a) to 9(d) for the 2-donor doped n-Si at 50 meV and 70 meV. Figure 8(d) prominently displays the peak of both acceptor impurity traps, $C_{\text{pt-50meV(Boron)}}$ and $C_{\text{pt-260 meV(Thallium)}}$ in the $C_{\text{pt}}-V_{\text{GB}}$ curves, but Figure 9(d) shows only a broad peak from the two donor impurity traps, $C_{\text{nt-50meV(Phosphorus)}}$ and $C_{\text{nt-70meV(Bismuth)}}$ in the $C_{\text{nt}}-V_{\text{GB}}$ curves. The difference came from the deeper level of the second impurity, the 260 meV Thallium, which locates its peak away from the peak of the first impurity, the 50 meV Boron, as indicated in Fig. 8(d), while for the two impurities of similar energy levels, 50 meV Phosphorus and 70 meV Bismuth, shown in Fig. 9(d), their trapping capacitance curves are nearly additive with their peaks merged into a broader peak, still near the flatband voltage of +0.8 V.

As a modeling exercise and device physics curiosity, we also computed the CV curves of MOSCs doped with a donor and an acceptor which are completely identical, in both the trap and band density of states and trap g-factors (equal to two). The parameters are the identical donor and acceptor concentration $N_{\text{DD}} \equiv P_{\text{AA}} = 10^{15}, 10^{16}, 10^{17}, 10^{18}, \text{ or } 10^{19} \text{ cm}^{-3}$, with $E_{\text{C}} - E_{\text{D}} \equiv E_{\text{A}} - E_{\text{V}} = 50 \text{ meV}$ in Figs. 10(a) to 10(h); 300 meV in Figs. 12(a) to 12(h); and 900 meV in Figs. 13(a) to 13(h); and the identical donor and acceptor energy levels of $E_{\text{C}} - E_{\text{D}} \equiv E_{\text{A}} - E_{\text{V}} = (10, 50, 300, 600, \text{ or } 900) \text{ meV}$, with $N_{\text{DD}} \equiv P_{\text{AA}} = 10^{18}$ in Figs. 11(a) to 11(h). The symmetry is expected from the completely identical electron and hole trap and band structure. We intentionally left in one asymmetry factor, namely, the true aluminum gate work function, to show a shift of the flatband voltage away from the zero applied gate-body voltage. The larger structure of the trapping capacitances with deeper energy levels is also anticipated from the results of the previous figures. The amplitude of the trapping capacitance does not scale linearly with the trap concentration, only super-logarithmically. In Fig. 11 with the energy level as the constant parameter for each CV curves, the "inverted" energy level traps with $E_{\text{C}} - E_{\text{D}} \equiv E_{\text{A}} - E_{\text{V}} = 900 \text{ meV}$ is not particularly distinguishable from the "not inverted" energy level traps with $E_{\text{C}} - E_{\text{D}} \equiv E_{\text{A}} - E_{\text{V}} = 300 \text{ meV}$, both with the trap levels at the approximately the two mid-half-gap locations (or exactly if the energy gap is taken to be 1200 meV instead of that of Si, which is 1120.85 at 300 K). The inverted case, of 900 meV, is possible in indirect energy gap materials such as silicon and germanium, with a large imperfection perturbation potential. Thus, the trapping capacity CV curves could not easily distinguish them, unless individual trapping capacitances are measured or decomposed out of the data, such as the C_{nt} and C_{pt} respectively in Figs. 11(e) and 11(g), which show that the peaks have moved from the majority carrier side to the minority carrier side of the gate voltage.

4. Summary

The main result from this survey calculation of the CV of MOS capacitors is the demonstration of making the trapping capacity large so that it is legible in the CV curve as an inflection point or better, a peak, which translates to larger signals in applications. In this report, III, the enhancement is accomplished chemically by addition (doping during crystal growth and epitaxial film growth, ion implantation, and diffusion) of a second trap species into the Si-base of the MOS capacitor. This

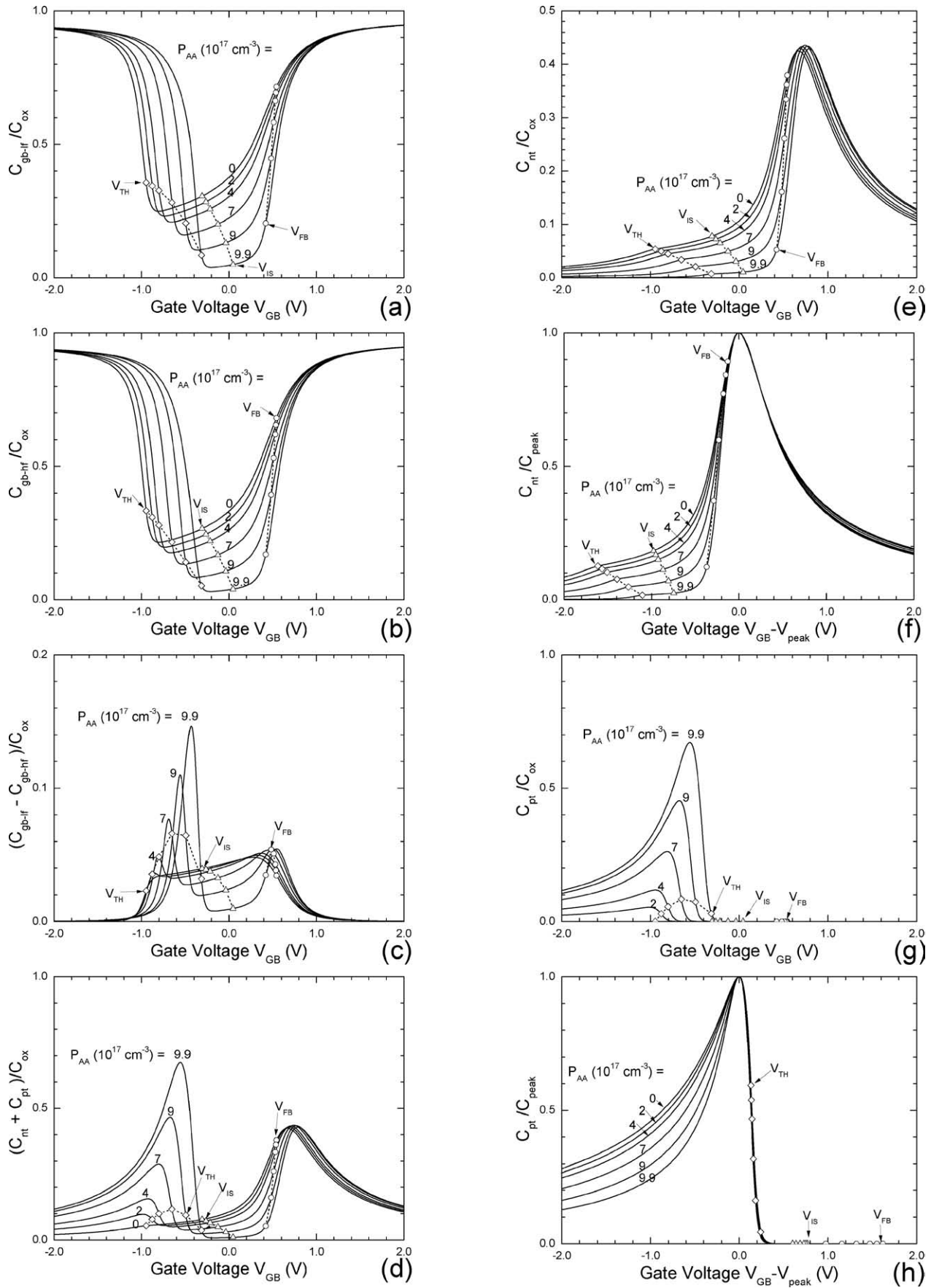


Fig. 6. Capacitance–Voltage curves of n-Si MOSCs containing a 50 meV donor and a compensating 50 meV acceptor. $X_{ox} = 3.5$ nm. $T = 300$ K. $N_{DD} = 10^{18} \text{ cm}^{-3}$. $g_D = 2$. $P_{AA} = (0, 2, 4, 7, 9 \text{ or } 9.9) \times 10^{17} \text{ cm}^{-3}$. $g_A = 4$. (a) C_{gb-lf} . (b) C_{gb-hf} . (c) $C_{gb-lf} - C_{gb-hf}$. (d) $C_{nt} + C_{pt}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

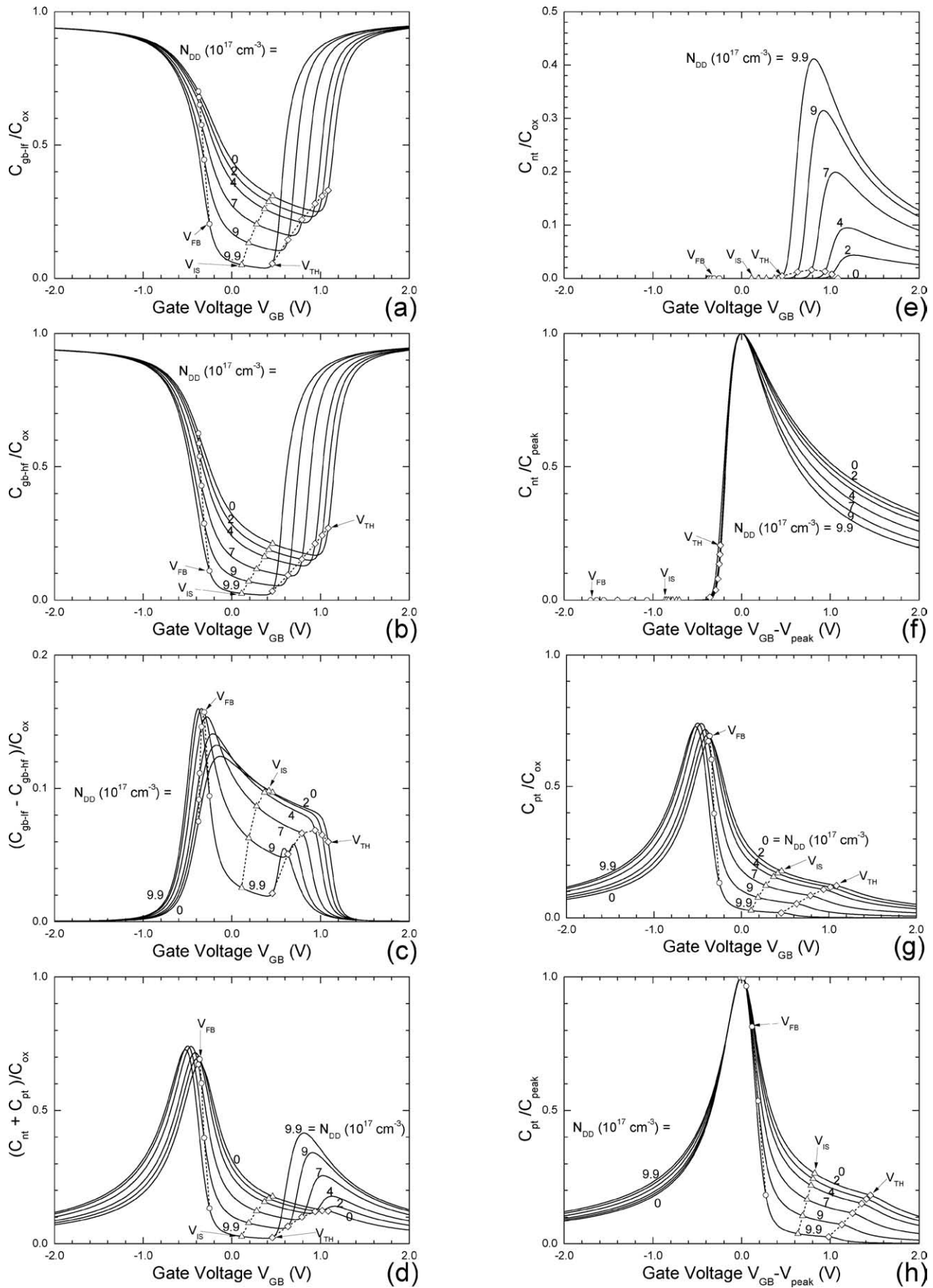
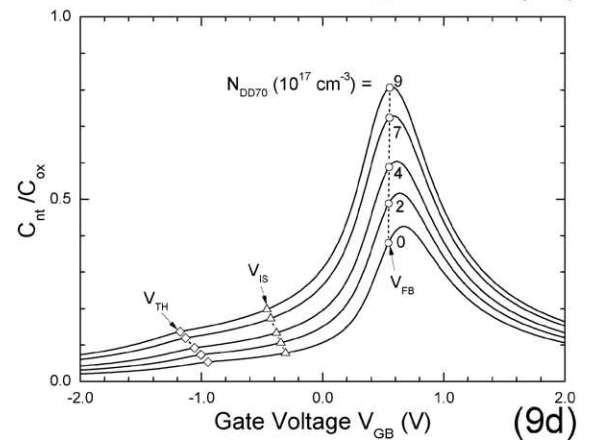
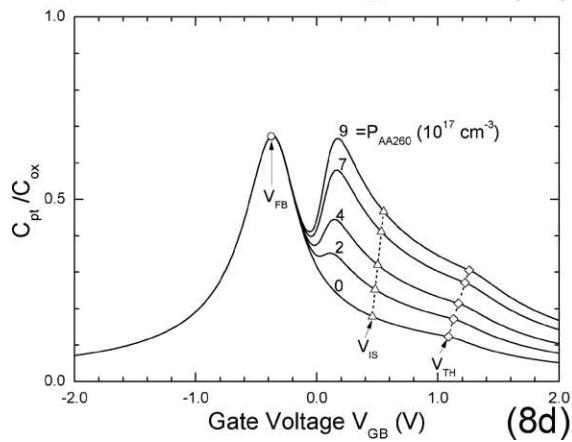
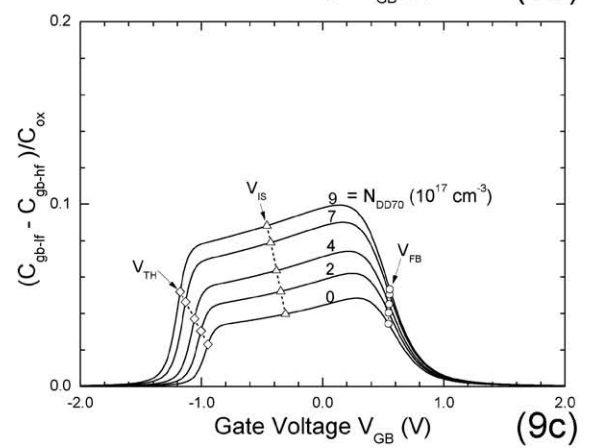
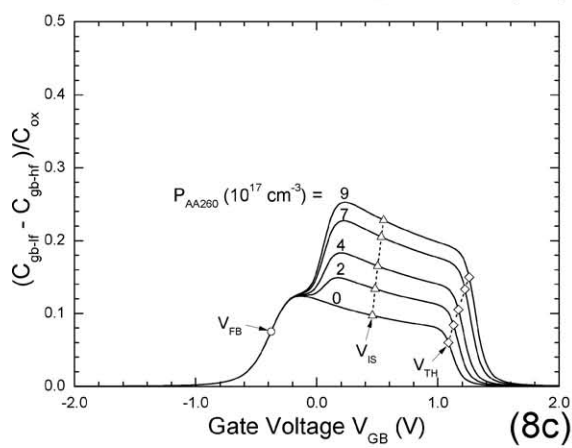
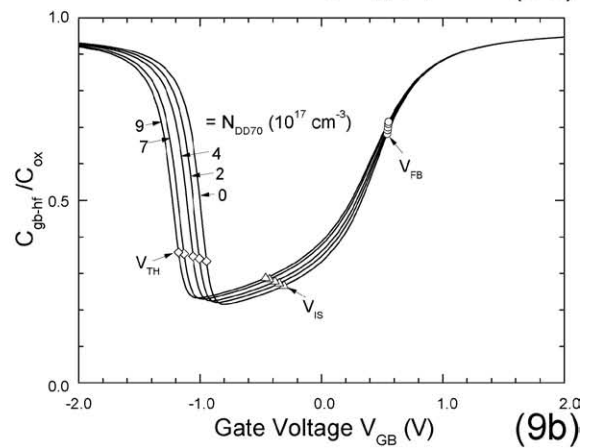
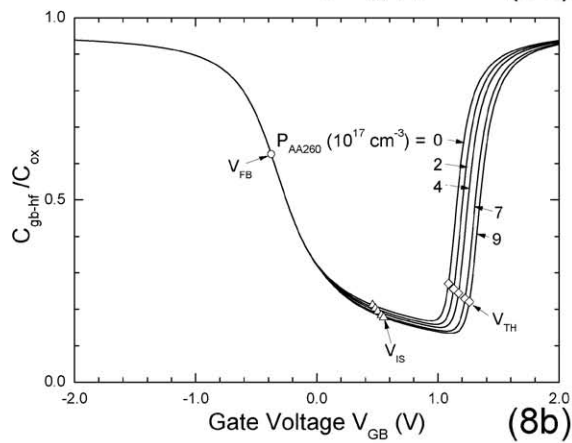
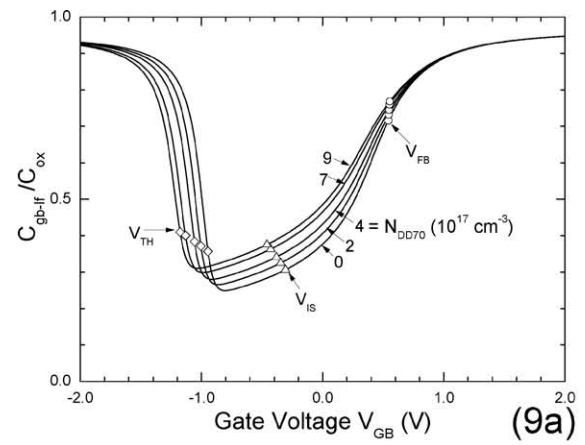
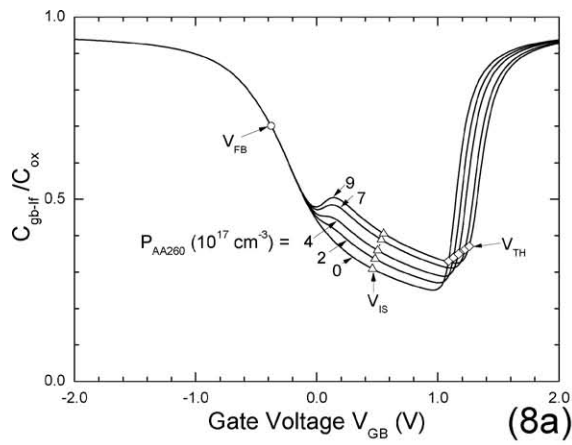


Fig. 7. Capacitance–Voltage curves of p-Si MOSCs containing a 50 meV acceptor and a 50 meV compensating donor. $X_{\text{ox}} = 3.5$ nm. $T = 300$ K. $P_{\text{AA}} = 10^{18} \text{ cm}^{-3}$. $g_{\text{A}} = 4$. $N_{\text{DD}} = (0, 2, 4, 7, 9 \text{ or } 9.9) \times 10^{17} \text{ cm}^{-3}$. $g_{\text{D}} = 2$. (a) $C_{\text{gb-lf}}$. (b) $C_{\text{gb-hf}}$. (c) $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) $C_{\text{nt}} + C_{\text{pt}}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .



Figs. 8 and 9. Comparing the 50 meV + 260 meV two-acceptor-species model with the 50 meV + 70 meV two-donor-species model. P_{AA} for the 50 meV acceptor = 10^{18} cm^{-3} . N_{DD} for the 50 meV donor = 10^{18} cm^{-3} .

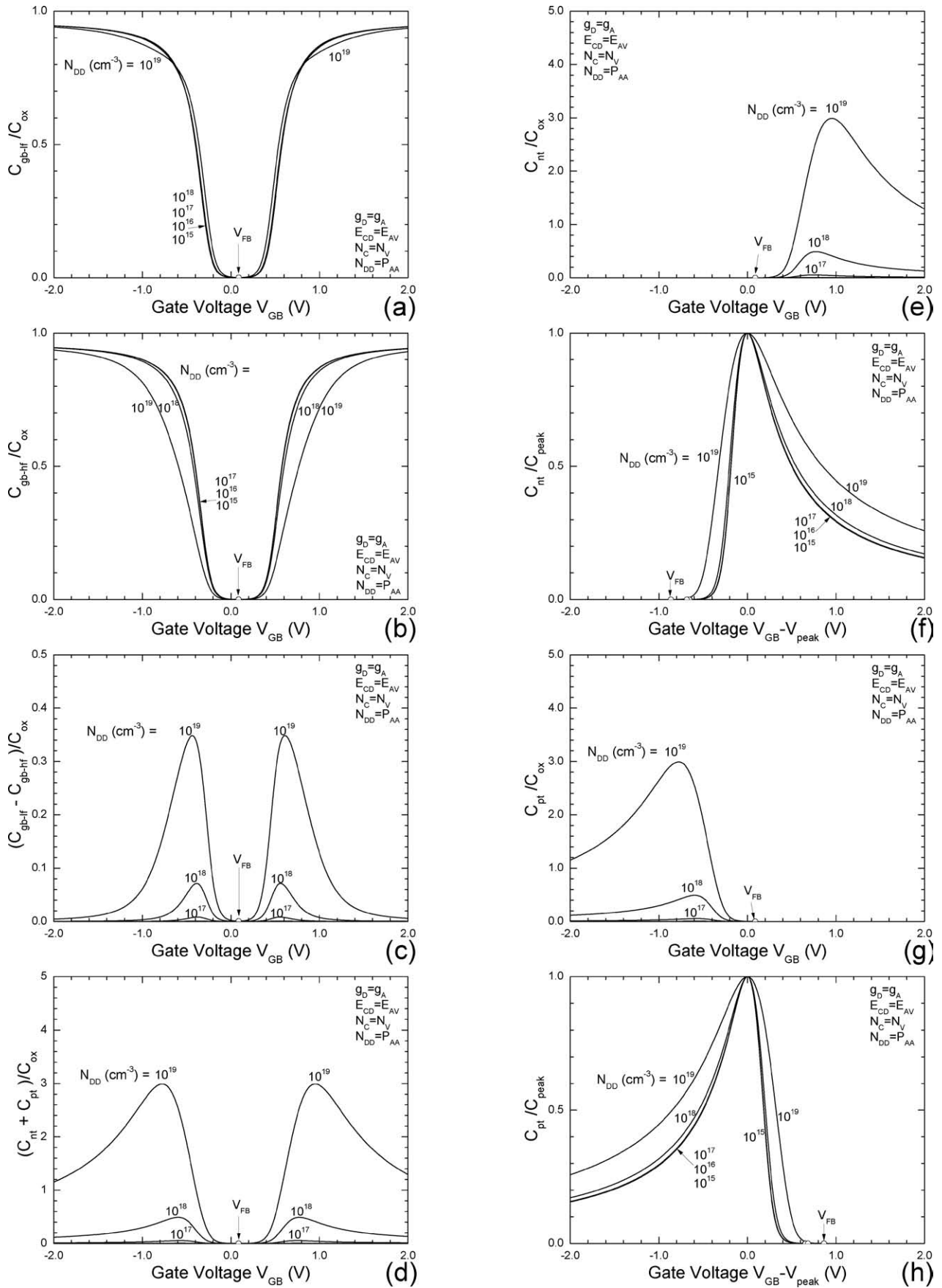


Fig. 10. Capacitance–Voltage curves of i-Si MOSCs containing an acceptor and a donor of identical properties. $X_{ox} = 3.5$ nm. $T = 300$ K. $N_{DD} = P_{AA} = 10^{15}, 10^{16}, 10^{17}, 10^{18}$ or 10^{19} cm $^{-3}$. $g_D = g_A = 2$. $E_C - E_D = E_A - E_V = 50$ meV. $N_C = N_V$. $E_{G-Si} = 1120.85$ meV. (a) C_{gb-lf} . (b) C_{gb-hf} . (c) $C_{gb-lf} - C_{gb-hf}$. (d) $C_{nt} + C_{pt}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

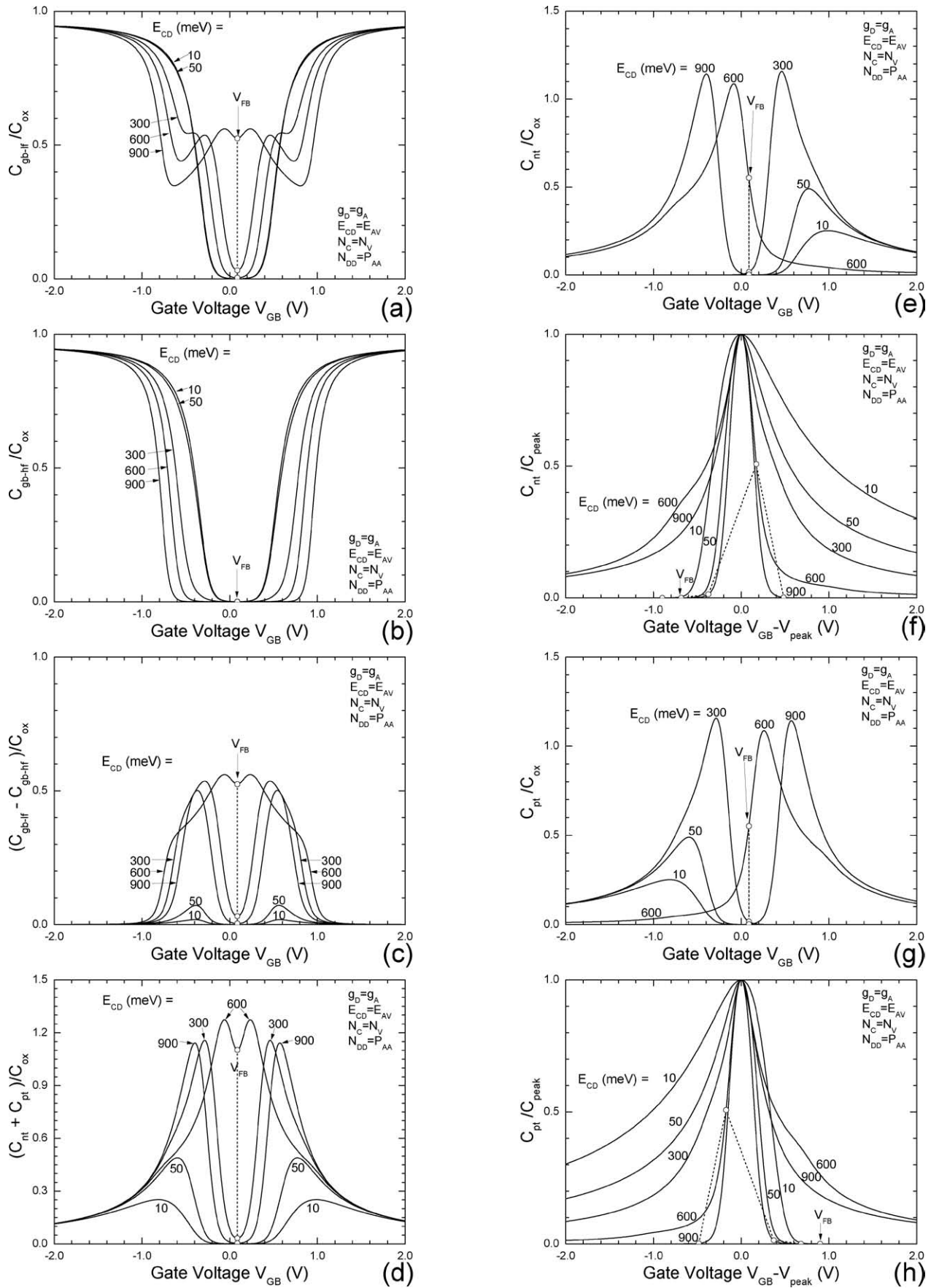


Fig. 11. Capacitance–Voltage curves of i-Si MOSCs containing an acceptor and a donor of identical properties. $X_{ox} = 3.5$ nm. $T = 300$ K. $N_{DD} = P_{AA} = 10^{18}$ cm $^{-3}$. $g_D = g_A = 2$. $E_C - E_D = E_A - E_V = 10, 50, 300, 600$ or 900 meV. $N_C = N_V$. $E_{G-Si} = 1120.85$ meV. (a) C_{gb-lf} . (b) C_{gb-hf} . (c) $C_{gb-lf} - C_{gb-hf}$. (d) $C_{nt} + C_{pt}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

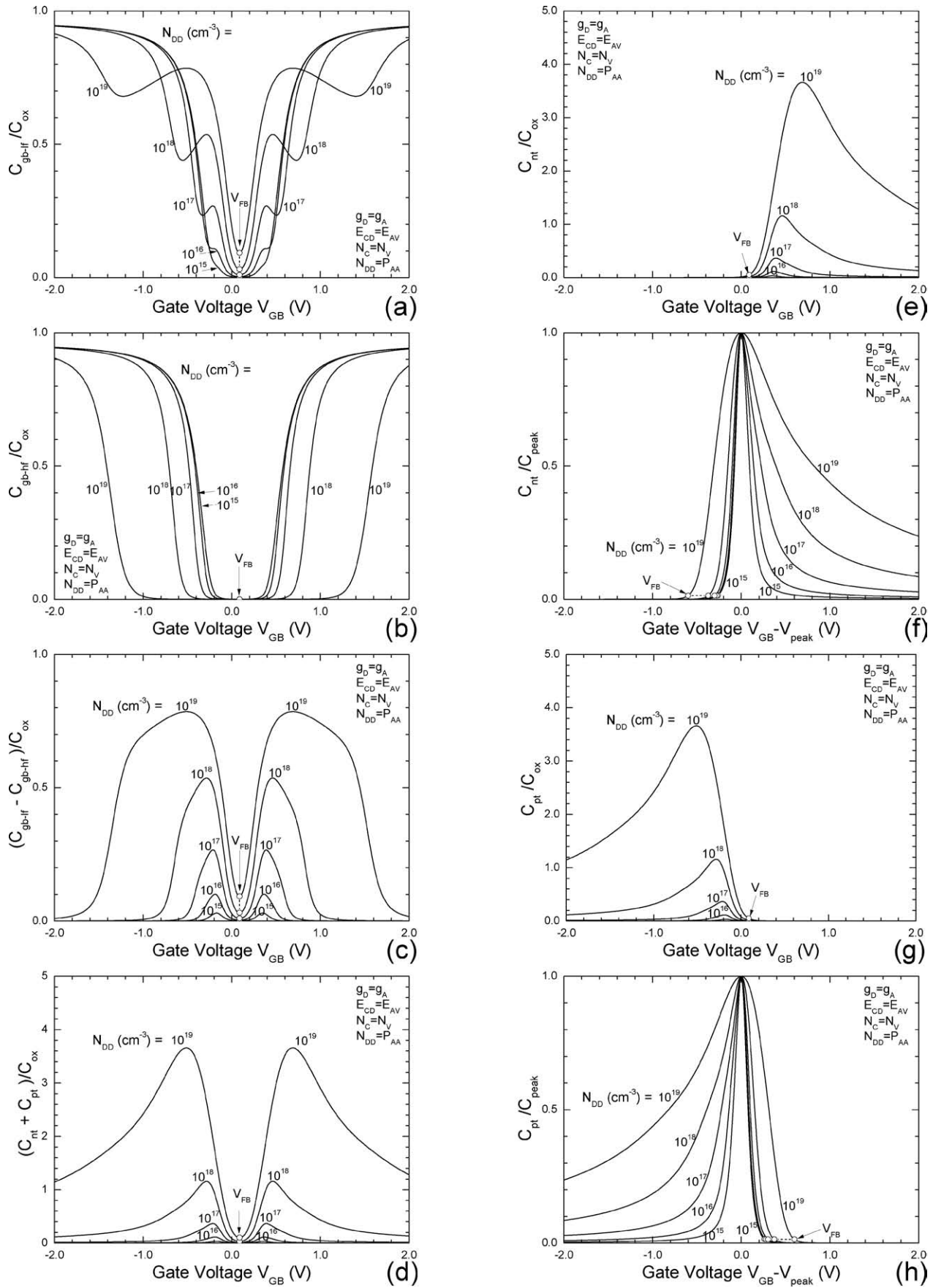


Fig. 12. Capacitance–Voltage curves of i-Si MOSCs containing an acceptor and a donor of identical properties. $X_{\text{ox}} = 3.5$ nm. $T = 300$ K. $N_{\text{DD}} = P_{\text{AA}} = 10^{15}, 10^{16}, 10^{17}, 10^{18}$ or 10^{19} cm^{-3} . $g_{\text{D}} = g_{\text{A}} = 2$. $E_{\text{C}} - E_{\text{D}} = E_{\text{A}} - E_{\text{V}} = 300$ meV. $N_{\text{C}} = N_{\text{V}}$. $E_{\text{G-Si}} = 1120.85$ meV. (a) $C_{\text{gb-lf}}$. (b) $C_{\text{gb-hf}}$. (c) $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) $C_{\text{nt}} + C_{\text{pt}}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

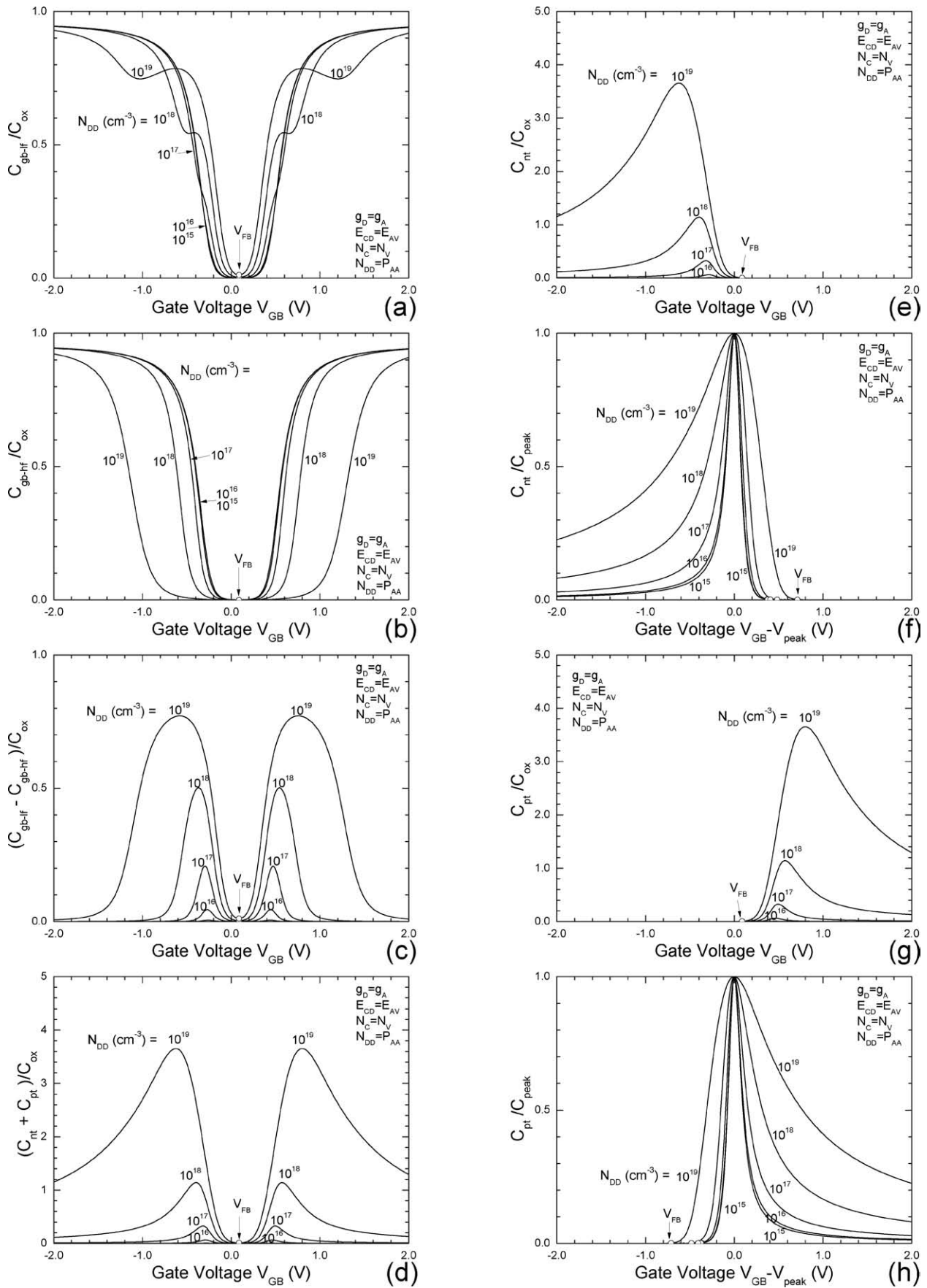


Fig. 13. Capacitance–Voltage curves of i-Si MOSCs containing an acceptor and a donor of identical properties. $X_{ox} = 3.5$ nm. $T = 300$ K. $N_{DD} = P_{AA} = 10^{15}, 10^{16}, 10^{17}, 10^{18}$ or 10^{19} cm $^{-3}$. $g_D = g_A = 2$. $E_C - E_D = E_A - E_V = 900$ meV. $N_C = N_V$. $E_{G-Si} = 1120.85$ meV. (a) C_{gb-lf} . (b) C_{gb-hf} . (c) $C_{gb-lf} - C_{gb-hf}$. (d) $C_{nt} + C_{pt}$. (e) C_{nt} . (f) Normalized-Shifted C_{nt} . (g) C_{pt} . (h) Normalized-Shifted C_{pt} .

second trap can be a deep majority carrier trap, or a shallow or deep minority carrier trap, so that its trapping capacitance peak appears in the subthreshold range in order to avoid or reduce masking of the trapping capacitance peaks by the majority and minority carrier storage capacitances. The illustration examples presented in this third report, III, have demonstrated this capability that would make the trapping capacitance legible in the experimental low-frequency CV curve, via data processing, by subtracting out the high-frequency CV. This sensitizing enables the high sensitivity detection and monitoring from the use of the trapping capacity in potential signal processing applications.

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