Detection of electron emission as DLTS signal in CdTe solar cells

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This work identifies an incongruity in the detection of the minority carrier signal in CdTe solar cells during the deep level transient spectroscopy (DLTS) measurement. Use of quasi-Fermi level instead of Fermi level of majority carriers to estimate the probability of emitting carriers seems to correct the ambiguity. During the experiment, signals from minority carrier traps (electron traps) were detected by using a long filling pulse time instead of an electron injection pulse. The DLTS measurements of CdTe solar cells observed a single electron trap with energy level $E_{E1} = 0.47$ eV, and two hole traps with energy levels, $E_{H1} = 0.17$ eV and $E_{H2} = 0.27$ eV. The possibility of any impact from the back contact was excluded, and the phenomenon was clarified by the simulation. It was further observed that when the condition of quasi-Fermi level is considered, the results of calculated probability were significantly different from that of the results that used only Fermi level of majority carriers. The simulations further aided the explanation of the defect behavior in DLTS measurements and the overlapping phenomenon of the capacitance spectrum of hole and electron traps. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4964438]

I. INTRODUCTION

Thin film CdS/CdTe solar cell module has been demonstrated to be one of the most promising alternative photovoltaic (PV) products. It has a low cost,[1] larger open-circuit voltage ($V_{OC} \sim 0.88$ V) as compared to that of polycrystalline Si (~ 0.67 V),[2] and higher theoretical conversion efficiency (perfect match to the spectrum of AM1.5).[3] In the last five years, the first solar has improved the efficiency from 17.3% to 22.1%,[2] which is about twice as much as that of improvements from 1993 to 2011.[4] As well reviewed and foreseen by Gloeckler *et al.*[4] in 2013, the enhancement of the efficiency was approached by increasing short-circuit current (J_{sc}) from ~ 28 mA/cm^2 to ~ 31 mA/cm^2 while V_{OC} has been stagnant around ~ 850 mV.[2,4] The increased J_{sc} was fulfilled by reducing the blue loss using a ZnMgO window layer,[5] and selenium was doped in the CdTe absorber layer to reduce the bandgap in order to convert a wide range of light waves.[6] Both Gloeckler[4] and Geisthardt[7] commented that improving V_{oc} to above 900 mV is necessary for the new record of efficiency. The metrics of V_{oc} is not as well understood as that of J_{sc}. During the last two decades, V_{oc} has shown no significant improvements. However, theoretically, researchers predicted that V_{oc} can be increased by increasing carrier lifetime, which is related to bulk recombination lifetime.[4] Deep level transient spectroscopy (DLTS) is a very powerful technique to understand defects in the bulk,[8] which is important for the future improvement of V_{oc}. In this paper, the quality of the devices under test (Table I) is not as sophisticated as devices at the state-of-the-art since a normal structure, material, and process were used. However, the results of DLTS measurement and the discussion of how minority carrier trap can be detected in this work can be critical as a metric of affecting the lifetime of carriers and therefore a demonstration of potential of increasing V_{oc}.

The DLTS has been used frequently to study the signatures of defects in p-type CdTe. Some studies reported only the majority carrier (hole) trap signal,[10,11] whereas some others have reported the detection of a minority carrier trap (electron) signal[12–17] if the injection pulse voltage (V_p) is set to be a positive value[13–15] or the injection pulse width is long enough (order of milliseconds).[16,17] In this work, it is found that the injection pulse width has a more significant impact on minority carrier capture rate compared with that on majority carrier capture rate. More importantly, after ruling out the possible effects of back contact, we confirmed that the minority trap DLTS signal can be detected even with a negative injection pulse voltage. To gain fundamental insights of this unexpected observation, we proposed to calculate the probability of emitting carriers using a quasi Fermi-level condition rather than using the conventional equation that only considers a single Fermi level. Our simulations based on the quasi-Fermi level condition resulted in a theoretical map of probability of emitting carriers. This map can be used to predict a detective region of the device as well as the reason why minority trap emission is possible in a diode system.

II. DEVICE INFORMATION AND MEASUREMENT INSTRUMENT

CdTe solar cells were fabricated using the commercial fluorinated tin oxide (FTO) glass substrates that were first cleaned by sonication in a solution of liquinox soap, followed by Deionized (DI) water, acetone, and isopropyl alcohol. An 80 nm thick CdS layer was deposited on the FTO glass using chemical bath deposition (CBD). A 5 μm thick CdTe layer was then deposited by close space sublimation (CSS) with $T_{source} = 650\,^\circ$C and $T_{superstrate} = 610\,^\circ$C. The CSS background gas pressure was maintained at 13 Torr under a He/O$_2$ flow

TABLE I. Electrical parameters of the device under test.

Efficiency	V_{oc}	J_{sc}	Fill factor	Carrier lifetime[a]	Carrier concentration[b]
13.5%	814.4 mV	22.62 mA/cm^2	73%	0.1 ns–1 ns	$\sim 10^{14}$ cm^{-3}

[a]The values are reported in Ref. 9.
[b]Measured by the capacitance-voltage method.

ratio of 14/1. A dry $CdCl_2$ thermal treatment was conducted at 400 °C for 40 min under a He/O_2 flow ratio of 2/1. The cell was then etched in phosphoric acid, nitric acid, and DI-water solution (NP etch) to provide a clean Te-rich surface. Immediately on removal from the acid, the samples were rinsed in DI water. A 10 nm thick Cu_2O film as the back contact was then prepared using reactive thermal evaporation. A graphite-based ELECTRODAG was then sprayed/brushed onto the surface of Cu_2O, and the sample was annealed at 170 °C in air for 20 min. Finally, the solar cell was finished with a layer of silver paste as high conductivity assistant back electrode. Similar cells were scribed to ~ 0.5 cm $\times$ 0.5 cm area. The electrical parameters of these gate stacks were listed in Table I.

DLTS system used in this work made use of a capacitance meter (either Boonton 7200 capacitance meter or commercial DLTS capacitance meter), and analog voltage output was acquired by the National Instrument DAQ board (PCIe-625) at different temperatures controlled by Lakeshore model 335. A Labview program was used for both control and post-experiment data processing.

III. EXPERIMENT AND DISCUSSION

Since the DLTS spectrum relies on the capacitance transient data, the corresponding data were plotted at four different temperatures (Fig. 1) to investigate how the capacitance transient behaves at different temperatures. Classically, the device under test was initially biased by a reverse bias voltage, V_r, that extends the depletion region in p-type CdTe since the doping level of CdTe (10^{14} cm^{-3}) is much lower than that of CdS (10^{18} cm^{-3}). During V_r period, carriers are depleted leaving the ionized acceptors (negative charged) in the depletion region. These traps emit either positive or negative charges because of the depletion voltage V_r. The capacitance measured during V_r shows an increased transient if traps emit holes (overall density of negative charge increase). On the contrary, it shows a decreased transient if traps emit electrons. The capacitance transient due to carrier emission is usually measured at V_r after an injection pulse voltage V_p is applied. Conventionally, V_p is set larger than V_r to inject majority carriers from the bulk (the depletion region is smaller than that under V_r) and minority carriers from the n-type material (the barrier height of pn junction is reduced). The capacitance transient during V_p can be accessed by the same explanation (considering additional charge density in the depletion region via traps capturing carriers). The capacitance increases if traps capture electrons or decreases if traps capture holes. The detection of emission of minority carriers (electrons) is possible by modifying V_p period to an appropriate level such that electrons capture is significant. As shown in Fig. 1(a), it was found that both the majority carrier (hole) capture and the minority (electron) carrier capture are possible during V_p period (first 100 ms) at 100 K. The capacitance decreases as holes are captured or increases as electrons are captured. However, the capture of electrons is slow, and it is not saturated even after 100 ms. Therefore, if the DLTS measurement is conducted with a filling pulse less than 5 ms, it is difficult to detect the minority trap spectrum since the electron traps were not significantly filled by electrons (it depends on the resolution of specific capacitance meter). The rates of capture and emission of a specific trap are not identical since the capture rate only depends on carrier concentration whereas the emission rate depends on the defect energy level. The rate window (emission rate or
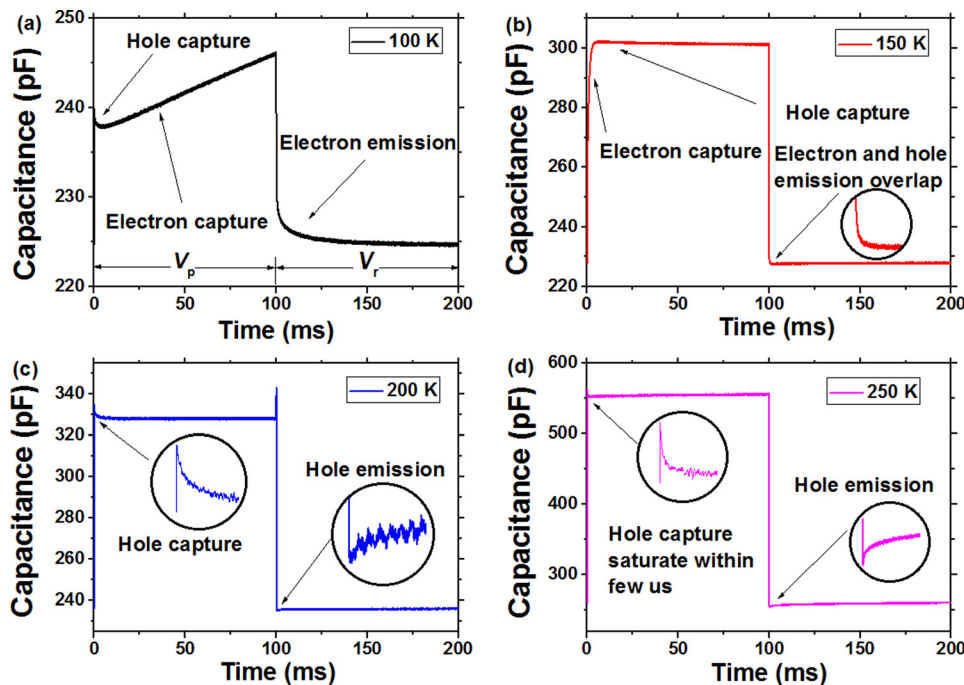

FIG. 1. The capacitance transient was measured as a function of time at four different temperatures (100 K, 150 K, 200 K, and 250 K). $V_p = 0.5$ V, $V_r = 0$ V. The data were averaged to reduce the Gaussian noise.
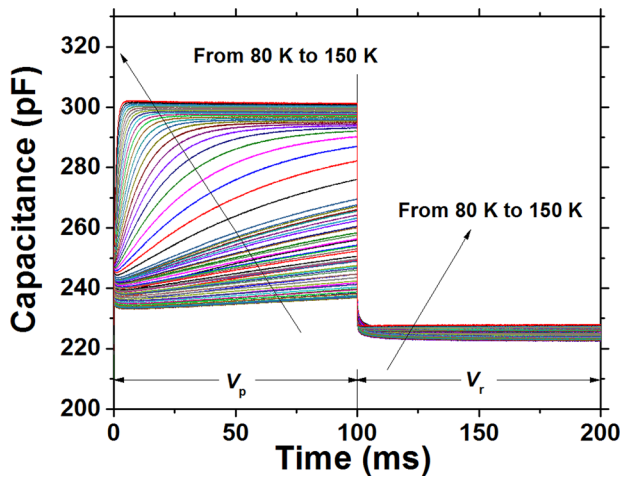
FIG. 2. The capacitance transient was measured as a function of time from 80 K to 150 K. $V_p = 0.5$ V, $V_r = 0$ V. The data were averaged to reduce the effect of Gaussian noise.

capture rate) of DLTS spectrum was set by choosing two sampling times in the boxcar t_1, t_2 ($t_1 < t_2$), that gives the value of rate window $\frac{\ln(t_2/t_1)}{t_2-t_1}$ as a function of t_1 and t_2.[8] For example, Fig. 1(a) shows that both the capture/emission processes of a specific electron trap occur at 100 K. As the temperature increases, the minority capture rate is also increased (Fig. 1(b)), which is confirmed by plotting this transient from 80 K to 150 K in Fig. 2. After the temperature reaches 200 K, a secondary hole carrier trap is active as shown in Figs. 1(c) and 1(d). There are observed transients in both emission/capture periods. In Fig. 1(c), the transients of both hole capture/emission can be observed as inset figure shows. However, the transient of hole capture saturates in a few microsecond as shown in Fig. 1(d). The capture/emission processes of electrons and holes can proceed simultaneously as Figs. 1(a) and 1(b) indicate. This leads the DLTS spectrum to be more complicated when more than one defect exists in the bulk. It is, therefore, necessary to summarize the first condition of detecting minority carrier spectrum in the DLTS measurement. The filling pulse must be set long enough depending on the specific device and capacitance meter resolution. On the contrary, filling process of majority carriers is much faster than that of minority carriers as shown in Figs. 1(c) and 1(d).

Figure 3(a) shows that the peak representing the electron trap is dependent on the pulse width (from 500 μs to 4000 μs) at a temperature around 140 K, and the peak of the

hole trap is not dependent on the filling pulse since 500 μs pulse width is long enough to fill the hole traps. A new set of pulse widths (from 5 μs to 40 μs) were used to investigate whether the reduction in the height of the peak for hole traps can be achieved by using a smaller pulse width. It was observed that a sufficient small filling pulse width could impede the minority trap peak but favor the majority trap since the detection of majority traps does not rely on filling pulses as much as minority traps do. In other words, the capture rate difference of minority and majority traps can be utilized to overcome the problem that peaks of electron/hole traps overlap in a DLTS measurement. As shown in Fig. 3(b), by applying a pulse width of a few μs, the peak of the hole trap appears at around 140 K instead of the peak of the electron trap since the process of capturing electrons is significantly limited, while the process of capturing holes is not. The pulse width dependent DLTS measurement was first discussed by Nakashima *et al.* in the study of accurate calculation of majority traps in p-type Si Schottky diodes.[18] In this study, it was observed that when the filling pulse is sufficiently long, the detection of the electron trap spectrum is possible. Therefore, the DLTS spectrum is skewed since the electron trap spectrum and the hole trap spectrum cancel each other as shown in Fig. 4.

However, it is necessary to rule out the possibility that the signal of DLTS is from the back contact barrier. The simulation by Thurzo and Dubecky[19] suggested that if the back contact resistance (R_b) is a function of activation energy over temperature, a similar plot like in Fig. 2 (Ref. 19) appears. As discussed extensively by Lauwaert *et al.*,[20] the difference between defects and the contact can be examined by the capture/emission spectra: significant difference of time constants indicates that it is a defect signal (the peak of spectra at different temperatures shown in Fig. 5), otherwise, it is a back contact signal. Since the emission rate will change several folds over a few Kelvin, around 10 K difference of signal peak is adequate to demonstrate the difference between the capture rate and the emission rate.

To study how the electron and hole spectra interact with each other over temperature, three different approaches of voltage pair (V_r, V_p) were used:

- Keep V_r at a constant negative value (emission dominates capture), and alternate V_p from negative to positive direction.
- Keep V_p at 0 V or above 0 V (capture dominates emission), and alternate V_r to different negative values.
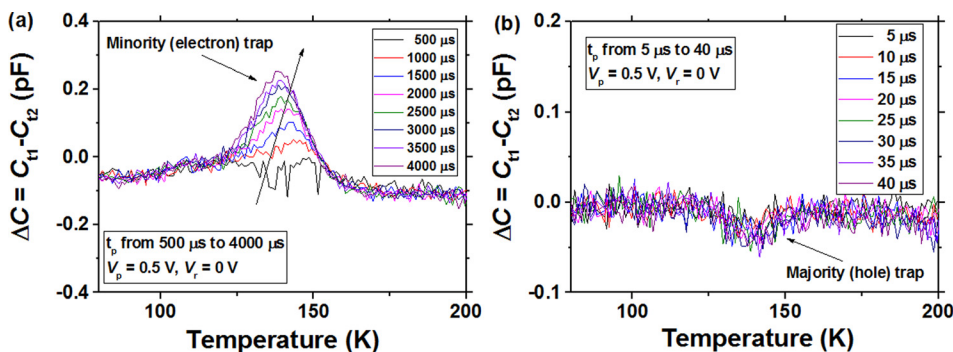

FIG. 3. The DLTS measurements were conducted at different pulse width parameters (a) from 500 μs to 4000 μs; (b) from 5 μs to 40 μs. $V_p = 0.5$ V, $V_r = 0$ V. The rate window is 866 s^{-1}.
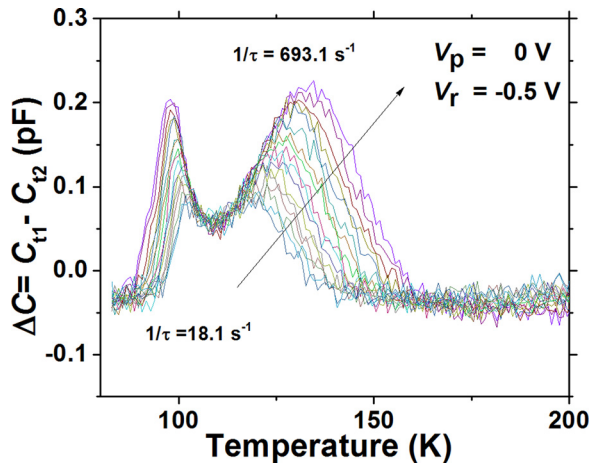
FIG. 4. The DLTS measurement was conducted at $V_p = 0$ V, $V_r = -0.5$ V with a pulse width 100 ms. Rate window is set from $18.1 \, \mathrm{s}^{-1}$ to $683.1 \, \mathrm{s}^{-1}$. The hole peak (negative peak) subtracts the electron peak (positive peak) around 110 K.

- Vary both V_r and V_p together in terms of depletion region width, W_r and W_p.

The DLTS spectra according to three approaches are shown in Figs. 6(a)–6(c), respectively. Figs. 6(a) and 6(b) show that the hole emission spectrum and the electron emission spectrum can be overlapped when they are compared to Fig. 6(c). Due to the existence of quasi-Fermi level in the depletion region, this phenomenon is expected (discussed later). Typically, for a device with only Fermi level of majority carriers, for example, a metal oxide semiconductor (MOS) structure, the amplitude of the peak of spectra is increased in one direction when the pulse height (V_p-V_r) is increased.[21,22] However, for a device with a quasi-Fermi level condition, for example, a pn junction diode, the overlap of the peaks of spectra of electron and hole traps could cancel each other (Figs. 4, 6(a), and 6(b)). It is observed that electron trap (E1) is more distinct when the pulse height is decreased to a certain level. (The electron emission overwhelms the hole emission.)

The above discussion raises a question whether hole and electron emissions can be separated by using a specific
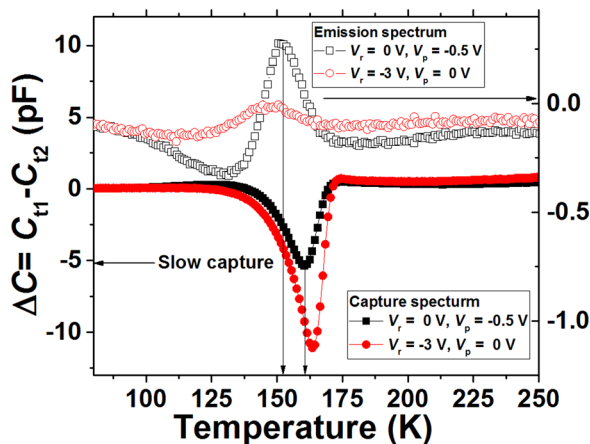

FIG. 5. The capture/emission spectra were measured at two different voltage pairs with $54.2 \, \mathrm{s}^{-1}$ rate window.

voltage pair to favor one type of emission over the other. The answer is, yes. But it also depends on the specific condition in the sample itself such as the concentration of traps, the distribution of traps, and the maximum depletion region width of the sample. As shown in Fig. 6(a), the direction of the arrow indicates that increased value of the injection pulse (keeping V_r constant) increases the ΔC in the negative direction. However, the overlap of peaks can still continue. On the other hand, minority carrier emission is much easier to be dominated by using a small pulse height as indicated in Fig. 6(c). The temperature of the peak of E1 is, therefore, constant at various voltage pair conditions. Therefore, we believe that the minority carrier emission without any minority carrier injection pulse[16,23] can be explained effectively by considering the probability of emitting carriers (discussed in Sec. IV).

Figure 6(c) further suggests that the use of a voltage pair with a relatively small pulse height is more robust for calculating the E1 energy level, while the hole trap levels were calculated based on Fig. 6(a) (using a relatively large pulse height to ensure that the hole emission overwhelms electron emission). Fig. 6(d) shows the Arrhenius plot of three different traps. The defects energy level (E_T) and signature value (K_T) are obtained from the slope and the intercept from the Arrhenius plot, respectively. The capture cross-section (σ) is then calculated by assuming $\gamma = 10^{20} \, \mathrm{cm}^{-2} \, \mathrm{s}^{-1} \, \mathrm{K}^{-2}$ since K_T is a product of $\sigma\gamma$. γ is a material dependent parameter. The defect concentration (N_T), can then be estimated by using Eq. (1), where $r = t_2/t_1$, N_A is the concentration of the acceptors in the depletion region, ΔC_{max} is the peak value of the DLTS spectra, and C_o is the capacitance measured at a specific temperature. Their signatures are $E_{E1} = 0.47$ eV, $K_{E1} = 5.3 \times 10^9 \, \mathrm{s}^{-1} \, \mathrm{K}^{-2}$) and two hole traps ($E_{H1} = 0.17$ eV, $K_{H1} = 3 \times 10^5 \, \mathrm{s}^{-1} \, \mathrm{K}^{-2}$; $E_{H2} = 0.27$ eV, $K_{H2} = 3 \times 10^5 \, \mathrm{s}^{-1} \, \mathrm{K}^{-2}$). The information of the defects is summarized in Table II. Since the samples were prepared by Tellurium-rich strategy, intrinsically, interstitial of Te (Te_i), substitutional of Cd by Te (Te_{Cd}), and Cd vacancy (V_{Cd}) are the most appropriate candidates for the observed defects. Extrinsically, due to diffusion of Cu from the back contact, Cd vacancies occupied by Cu (Cu_{Cd}) are also possible in this work. According to calculations of Wei and Zhang,[24] E1, H1, and H2 can be attributed to interstitial of Te (Te_i), Cd occupied by Cu (Cu_{Cd}), and Cd vacancy (V_{Cd}), respectively, since values are close to theoretical value. Versluys reported a similar energy level of one electron trap (0.441 eV) in their work by using an injection DLTS method.[15] Balcioglu believed that their hole trap ($E_v + 0.35$ eV) is due to the Cu substitutional.[16] We, therefore, believe, it is $E_v + 0.17$ eV in this work. The Cd vacancies (V_{cd}) are reported in literature, but their values range from 0.13 eV to 0.4 eV (Ref. 10)

$$N_T = \frac{\Delta C_{max}}{C_o} \frac{2 r^{r/(r-1)}}{1 - r} N_A. \tag{1}$$

IV. SIMULATION AND DISCUSSION

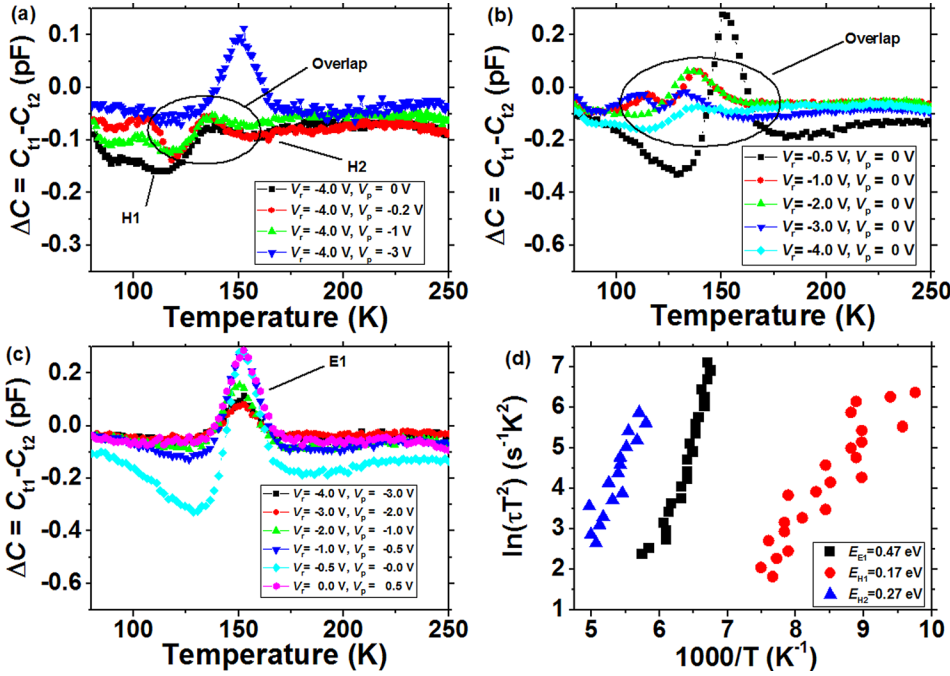The traditional study of behaviors of defects in the depletion region of pn junctions and metal-semiconductor

FIG. 6. The DLTS signals at different voltage pairs (V_r and V_p) calculated by the rate window 54.2 s^{-1}. (a) V_r is constant, V_p is alternating; (b) V_r is alternating, V_p is constant; (c) ΔV is small (d) Arrhenius plots of three different traps (E$_1$, H$_1$, and H$_2$), different rate windows range from 18.05 s^{-1} to 2777.8 s^{-1}.

diodes lacks analysis of the probability of occupation of the specific defect energy level. For example, it is known that both majority carrier emissions and minority carrier emissions can be observed in the pn junction and the metal-semiconductor junction devices. The explanation of the minority carrier emission is attributed to the injection of minority carriers by using a minority pulse voltage ($V_p > 0\,$V), while the majority carrier emission can be measured using a majority carrier pulse voltage ($V_p \leq 0\,$V).[8] In other words, if the pulse voltage is lower than the minority pulse voltage (no minority carriers are injected), the minority carrier emission should be significantly impeded. However, the detection of minority carriers is observed on Schoktty diodes without minority carrier injection.[23] Additionally, the minority trap signal was also observed in our solar cell devices and in Balcioglu's work without any minority carrier injection.[16] It is, therefore, necessary that the explanation should be based on the calculation of the probability of occupation. Equations (2)–(5) involving Fermi level and the carrier interactions at the defect sites are given by Shockley–Hall–Read (SHR) process.[25] The parameters are described in the subsequent discussions

$$f = \frac{1}{1 + \exp\left(\dfrac{E_T - E_F}{kT}\right)}, \tag{2}$$

TABLE II. Trap signature determined by the Arrhenius plot.

	E_T (eV)	K_T (s^{-1} K^{-2})	σ (cm^2)[a]	N_T (cm^{-3})[b]
E1	0.47	5.3×10^9	5.3×10^{-11}	3.2×10^{11}
H1	0.17	3×10^5	3×10^{-15}	3.1×10^{11}
H2	0.27	3×10^5	3×10^{-15}	1.5×10^{11}

[a]The capture cross-section is calculated by assuming $\gamma = 10^{20}\,$cm^{-2} s^{-1} K^{-2}.
[b]N_T is calculated by Eq. (1) for a quantitative information.

$$f = \frac{c_n + e_p}{c_n + e_p + c_p + e_n}, \tag{3}$$

$$c_n = \sigma_n v_n n_i \exp\left(\frac{E_{Fn} - E_i}{kT}\right), \tag{4a}$$

$$e_n = \sigma_n v_n n_i \exp\left(\frac{E_T - E_i}{kT}\right), \tag{4b}$$

$$c_p = \sigma_p v_p n_i \exp\left(\frac{E_i - E_{Fp}}{kT}\right), \tag{4c}$$

$$e_p = \sigma_p v_p n_i \exp\left(\frac{E_i - E_T}{kT}\right), \tag{4d}$$

$$E_{Fn} - E_{Fp} = \alpha q V. \tag{5}$$

Fermi level can be utilized to estimate the probability of electrons being trapped (defects being occupied by electrons) on a specific defect level as shown in Eq. (2), where E_T is the defects energy level, E_F is the Fermi level, k is the Boltzmann's constant, and T is the temperature. The change of probability can be calculated in the case of single Fermi-level for the large signal as Fermi level changes as a function of the carrier concentration. However, a pn junction or a metal-semiconductor junction device has the quasi-Fermi level in the depletion region. The calculation of the probability of occupation of electrons can be carried out by using Eq. (3), where c_n and e_n stand for the capture rate and the emission rate of electrons, respectively, and c_p and e_p stand for the capture rate and the emission rate of holes, respectively.

If a single Fermi level is considered, Eqs. (2) and (3) are interchangeable via Eq. (4) when $\sigma_n v_n = \sigma_p v_p$, $E_{Fn} = E_{Fp}$, where σ_n and σ_p are the capture cross-sections for electrons and holes, respectively, and v_n and v_p are the thermal velocities for electrons and holes, respectively. In case of

quasi-Fermi level, Eq. (2) is no longer valid. Fig. 7 shows the difference of trap behavior in band diagram between the single Fermi level system (Figs. 7(a) and 7(b)) and quasi-Fermi level systems (Figs. 7(c) and 7(d)) when the bias condition is changed from the equilibrium condition to the depletion condition (Figs. 7(a) to 7(b) and 7(c) to 7(d), respectively). When correlating probability of emitting carriers with injection pulse type (majority or minority), the simulation agrees with the single Fermi level system perfectly (no minor carrier injection). However, it cannot explain why there is a minority carrier emission in pn junction device if there is no minority injection (pulse voltage is lower than 0 V or 0 V) like Balcioglu's work[16] or this work. Fig. 7(d) shows how quasi Fermi level affects the probability of occupation in the bandgap. The trap energy level near the quasi Fermi level region is significantly different from systems with single Fermi level as the question mark shows (Fig. 7(d)). The probability of occupation of an electron is, therefore, necessary to be calculated correctly in Eq. (4) regarding quasi Fermi condition. When the pn junction is biased, Eq. (5) gives the relationship between bias voltage and quasi-Fermi level, where V is the voltage applied to the pn junction, q is the elementary charge, and α is the coefficient considering the difference between the applied voltage on diode (E_{Fn}-E_{Fp}) and the voltage consumed (V) in the depletion region, which is larger than one.

There are several assumptions made in the simulation: (i) the probability of occupation of carriers is valid under steady state; and (ii) no recombination and current flow take place in the depletion region (Fermi level is flat). This may be applicable when a pn junction is reversed biased and the concentration of defects is not significant. The band bending is calculated based on the Poisson equation. The doping concentration is set to be 10^{14} cm^{-2}. The capture cross-section is set to be 10^{-15} cm^{2}. Carrier concentration can affect the overall probability in two different ways. The detection

region is affected by carrier concentration in terms of depletion region range. Carrier concentration also affects the rate of majority carriers being captured, as predicted in Eq. (4c). The foundation of the quasi-Fermi level condition is based on the fact that we also consider minority capture rate. Therefore, a change in majority carrier concentration affects the map to some extent, but not significantly, since trapping carriers is the prerequisite of capture/emission events. In systems with quasi-Fermi level, the probability of occupation of electron depends on the capture rates of both majority and minority carriers, indicated in Eq. (3).

10^{-15} cm^{-2} is a typical value for the capture cross-section of the defect which corresponds to a defect radius of 10^{-7} cm approximately. Therefore, a value of 10^{-15} cm^{-2} was used for the capture cross-section. This cross-section value is not valid for all types of defects, especially when defects are the shallow traps or when the columbic interaction (charged state traps additional charges) is possible.[26,27] Compared to the carrier concentration, σ has an enhanced effect in simulation results since σ directly affects the capture rate. In this simulation, same values of σ were used for both holes and electrons. If holes and electrons are assigned by different cross-sectional values, the capture process is favored by the one with the larger cross-section (the difference of the magnitude can be several fold), and the overall map is shifted.[27] For example, if the capture cross-section for electrons is larger than that of holes, traps will tend to emit electrons for the same biased condition because more traps captured electrons during capture process. However, this is just a probability map. In the real device, it depends on what the specific trap is (hole or electron trap). For the hole trap, it can be assumed that the cross-section for electrons is of 0 cm^{-2}.

Figure 8 compares the change of the probability of trapping an electron when different Fermi level conditions are given where majority carriers are holes. The plot in Fig. 8(a)
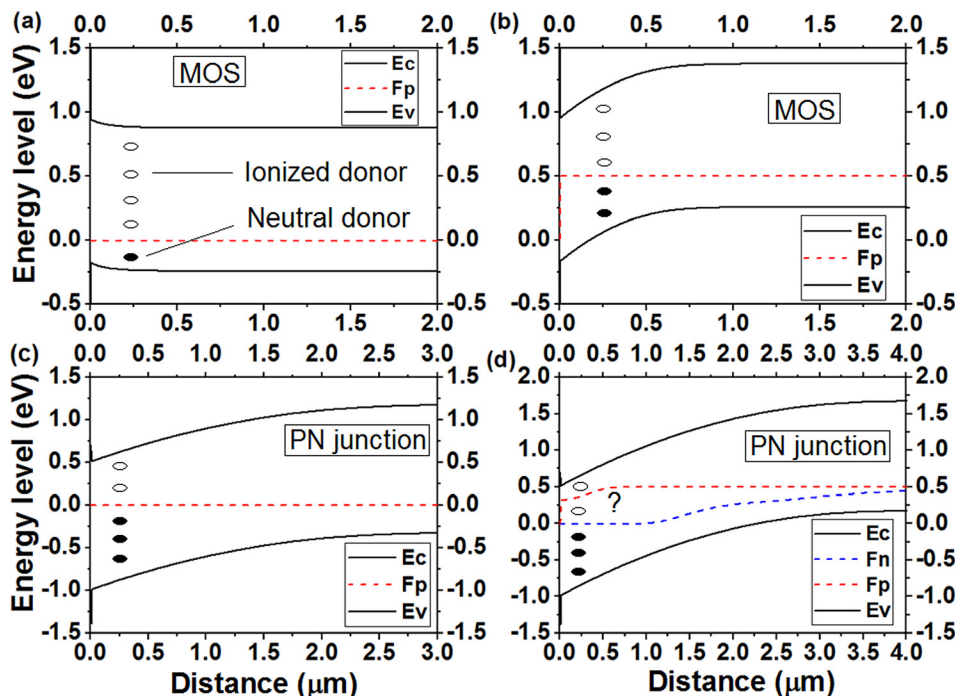

FIG. 7. The band diagram at two different bias conditions for p-type substrate is plotted for both the MOS structure (SiO$_2$/p type Si) and the pn junction (n-type CdS/p-type CdTe): (a) the MOS structure, bias voltage = 0 V, (b) the MOS structure, bias voltage = −0.5 V (the voltage difference between Si and SiO$_2$); (c) the pn junction, bias voltage = 0 V, and (d) the pn junction, bias voltage = −0.5 V (the voltage difference between CdTe and CdS). The state of defect is illustrated in the band gap. It is clear that the probability of occupation of electrons under quasi-Fermi level conditions (d) is necessary to be calculated from Eqs. (3) and (4).
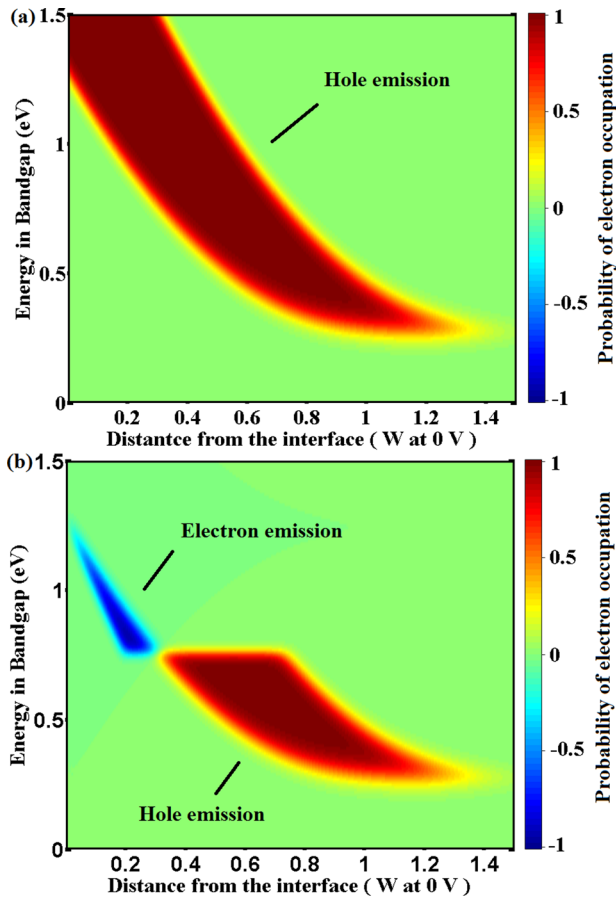
FIG. 8. The probability of emitting electrons as a function of space and energy level is plotted by Matlab when the bias voltage is alternated from 0 V to −1 V. (a) The case of one Fermi level, and (b) the case of quasi-Fermi level using Eqs. (3) and (4). Red part indicates the probability of occupation of electron changes from 0 to 1 (hole emission); blue part indicates the probability of occupation of electron changes from 1 to 0 (electron emission). W is the depletion layer width under 0 V.

considers only one Fermi level in the depletion region. It is observed that only hole emission is possible under the one Fermi level case, as observed in a single Fermi level case.[22,28] On the other hand, Fig. 8(b) shows that both the electron emission and the hole emission exist under the quasi-Fermi level case as in a pn junction device like the solar cell. The simulation results in Fig. 8(b) are consistent with the following description: the energy level close to the conduction band tends to emit electrons and the energy level close to the valence band tends to emit holes. Two states are defined here, and they are identical to that used in Sec. III. V_r is the reversed bias voltage and V_p is the pulse voltage, and then the capacitance transient is measured when V_p changes to V_r. When calculating the map of probability, it is not necessary to have V_r smaller than V_p. If the steady state is maintained long enough, the probability of occupation of electrons will finally follow Eq. (3). If V_r and V_p are interchanged, the change in probability has an opposite sign. But it is required that V_p is set to inject the carriers, and V_r is set to emit the carriers ($V_p > V_r$).

The simulation further suggests that the minority carrier emission can occur without a minority carrier injection condition in the earlier report by Versluys,[15] who used a value of

V_p as 0.5 V. Practically, the peak of the minority carrier emission can be obtained with the voltage pair ($V_r = -4$ V, $V_p = -3$ V) as shown in Fig. 6(c). Another important observation in the simulation is that the defects in the probability map that emit the minority carriers are rarely changed with the pulse height as long as the pulse height is large enough (for example, the V_p was kept at 0 V when V_r was decreased in Sec. III). Comparing Figs. 8(b) and 9, the probability maps under three different voltage pairs demonstrate that the space of the minority emission was not varied significantly at a specific energy level. It is shown in the signature part (blue) in Fig. 9. On the contrary, the probability map of hole emissions could be varied by using different bias voltage pairs as shown in the red part of Fig. 9. The probability of emitting carriers, calculated by quasi-Fermi level, is consistent with the experimental results and helps in the explanation of defect behavior of DLTS and the overlapping phenomenon of the capacitance spectrum of both hole and electron traps.

V. CONCLUSION

The conventional capacitance transient was carefully observed before the DLTS measurement using a long filling
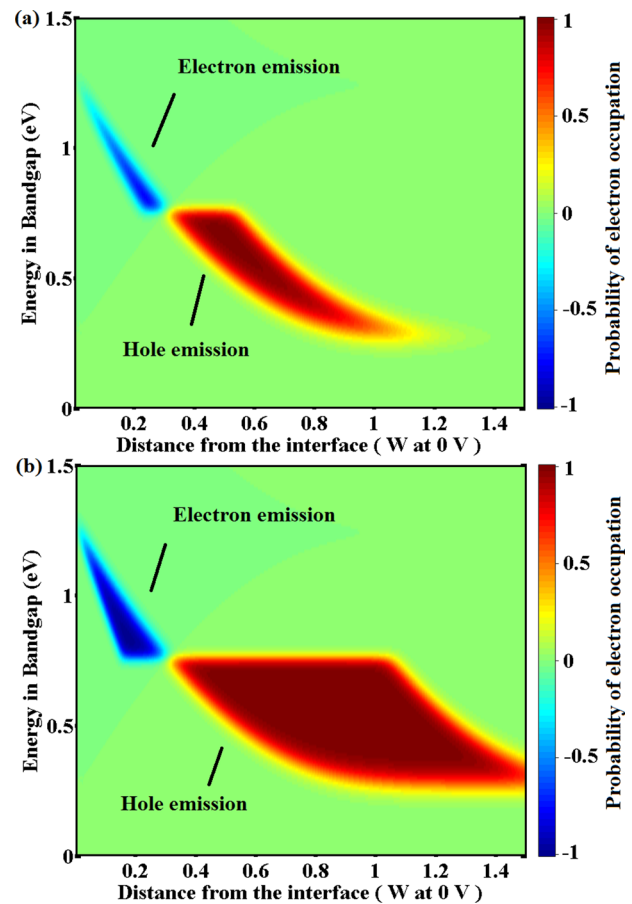

FIG. 9. The probability of emitting electrons as a function of space and energy level is plotted by Matlab when the bias voltage is alternated from (a) 0 V to −0.5 V, (b) 0 V to −2 V. $\sigma_n v_n = \sigma_p v_p$ was assumed. Red part indicates the probability of occupation of electron changes from 0 to 1 (hole emission); Blue part indicates the probability of occupation of electron changes from 1 to 0 (electron emission). W is the depletion layer width under 0 V.

pulse. After ruling out possibility of the back contact, the electron trap-like DLTS signal is attributed to the electron trap ($E_{E1} = 0.47$ eV). Besides the electron trap, two hole traps ($E_{H1} = 0.17$ eV, $E_{H2} = 0.27$ eV) were also discovered by setting different voltage pairs. To explain why the electron trap is detectable theoretically and why DLTS spectrum conducted under large ΔV showed an overlapped or averaged out phenomenon, the simulation based on quasi-Fermi level assumption was carried out. It theoretically demonstrates that minority traps can trap and emit electrons if the biased condition is alternated and subsequently interacts with the majority trap signal. More importantly, the idea of quasi-Fermi level simulation holds generally for devices with a quasi-Fermi level condition like pn junction diodes, metal-semiconductor diodes, and the idea of detection of minority carriers holds for both n and p-type substrates.

[1] J. D. Major, R. E. Treharne, L. J. Phillips, and K. Durose, Nature **511**, 334 (2014).

[2] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, Prog. Photovoltaics: Res. Appl. **24**(7), 905 (2016).

[3] A. Morales-Acevedo, Sol. Energy **80**, 675 (2006).

[4] M. Gloeckler, I. Sankin, and Z. Zhao, IEEE J. Photovoltaics **3**(4), 1389 (2013).

[5] R. Shao and M. Gloeckler, U.S. patent application US20120067421 A1 (2012).

[6] A. R. Duggal, J. J. Shiang, W. H. Huber, and A. F. Halverson, U.S. patent application US20140373908 A1 (2014).

[7] R. M. Geisthardt, M. Topi, and J. R. Sites, IEEE J. Photovoltaics **5**(4), 1217 (2015).

[8] D. V. Lang, J. Appl. Phys. **45**, 3023 (1974).

[9] Z. Cheng, A. E. Delahoy, Z. Su, and K. K. Chin, Thin Solid Films **558**, 391 (2014).

[10] A. Castaldini, A. Cavallini, B. Fraboni, P. Fernandez, and J. Piqueras, J. Appl. Phys. **83**, 2121 (1998).

[11] J. Szatkowski, E. Phzek-Popko, and A. Hajdusianek, J. Phys.: Condens. Matter **6**, 7935 (1994).

[12] V. Komin, B. Tetali, V. Viswanathan, S. Yu, D. L. Morel, and C. S. Ferekides, Thin Solid Films **431**, 143 (2003).

[13] W. Zhao, L. Bing, Z. Xu, X. Jing, H. Zheng, L. Cai, F. Liang-Huan, and Z. Jia-Gui, Chin. Phys. B **19**, 027303 (2010).

[14] M. A. Lourenco, Y. K. Yew, K. P. Homewood, K. Durose, H. Richter, and D. Bonnet, J. Appl. Phys. **82**, 1423 (1997).

[15] J. Versluys, Thin Solid Films **451–452**, 434 (2004).

[16] A. Balcioglu, J. Appl. Phys. **88**, 7175 (2000).

[17] K. Scholz, H. Stiens, and G. Muller-Vogt, J. Cryst. Growth **197**, 586 (1999).

[18] H. Nakashima, T. Miyagawa, S. Sugitani, and K. Hashimoto, Jpn. J. Appl. Phys., Part 1 **25**, 205 (1986).

[19] I. Thurzo and F. Dubecky, Phys. Status Solidi A **89**, 693 (1985).

[20] J. Lauwaert, S. Khelifi, K. Decock, M. Burgelman, and H. Vrielinck, J. Appl. Phys. **109**, 063721 (2011).

[21] A. V. P. Coelho, M. C. Adam, and H. Boudinov, J. Phys. D: Appl. Phys. **44**, 305303 (2011).

[22] K. Yamasaki, M. Yoshida, and T. Sugano, Jpn. J. Appl. Phys., Part 1 **18**, 113 (1979).

[23] S. W. Johnston, S. R. Kurtz, D. J. Friedman, A. J. Ptak, R. K. Ahrenkiel, and R. S. Crandall, Appl. Phys. Lett. **86**, 072109 (2005).

[24] S.-H. Wei and S. B. Zhang, Phys. Rev. B **66**, 155211 (2002).

[25] W. Shockley and W. T. Read, Phys. Rev. **87**, 835 (1952).

[26] K. K. Chin and Z. Cheng, J. Semicond. **37**, 092003 (2016).

[27] Z. Cheng and K. K. Chin, in *Photovoltaic Specialists Conference (PVSC)* (IEEE, Austin, TX, 2012), p. 25.

[28] M. Schulz and N. M. Johnson, Appl. Phys. Lett. **31**, 622 (1977).