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Current–voltage characteristics of p-Si/carbon junctions fabricated by pulsed laser deposition

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ABSTRACT

Amorphous carbon/p-Si junctions were fabricated at different temperatures using KrF excimer laser ($\lambda = 248$ nm, pulsed duration 20 ns). The current–voltage measurements of the devices showed diode characteristics. The value of various junction parameters such as ideality factor, barrier height, and series resistance were determined from forward bias *I–V* characteristics, Cheung method, and Norde's function. There was a good agreement between the diodes parameters obtained from these methods. The ideality factor of ~1.12 and barrier height of ~0.37 eV were estimated using current–voltage characteristics for films grown at room temperature.

1. Introduction

Amorphous carbon films have attracted considerable attention due to potential applications in microelectronic devices, field emission, gas sensors, and hard coatings [1–5]. The properties of these films largely depend on the presence of sp, sp^2, and sp^3 bonds [6]. The graphite-like structure having high sp^2 character is responsible for high electrical conductivity, while high sp^3 character produces films with high mechanical strength. Different methods have been used for deposition of various kinds of carbon films [4]. The electrical properties of these films are reported to improve by doping with boron and phosphorus [6].

Iron doped amorphous carbon–silicon p–n junctions, fabricated using direct current magnetron sputtering, show junction resistance undergoing a metal–insulator transition [7]. Literature survey reveals that there is no detailed study on diode parameter analysis using different methods such as Cheung and Norde's methods. In this paper, we report the fabrication and diode characterization of amorphous carbon/p-Si junctions grown at different temperatures by the pulsed laser deposition technique. Different diode parameters such as ideality factor, barrier height, and series resistance are determined using different methods.

2. Experimental details

Carbon and gold targets for pulsed laser deposition were purchased from Kart J. Leasker, USA. The device was prepared using p-type silicon wafer. The silicon substrate was cleaned using the RCA technique [8] before making contacts and depositing carbon. The oxide layer on silicon wafer was removed using HF:10H_2O solution followed by sonication in acetone and isopropanol. Carbon films were deposited on silicon at room temperature and 200 °C under vacuum of base pressure 1.2×10^{-6} mbar. Gold contacts were also deposited at room temperature at the same base pressure. KrF excimer laser (Lambda Physik COMPex, $\lambda = 248$ nm and pulsed duration of 20 ns) was used for film deposition at a pulse rate of 10 Hz and with an energy of 300 mJ/pulse. The carbon films thickness were measured to be ~72 nm by atomic force microscopy [9]. For this one has to scratch the film down to the substrate first and then scan the sample across the scratch to get a height profile. Micro-Raman scattering experiments were performed in the perfect backscattering geometry using a fiber-optically coupled confocal micro-Raman system (TRIAX 320) which is equipped with a liquid N_2 cooled charge coupled detector. The current–voltage (*I–V*) characteristics of Au/p-Si/carbon/Au device were measured using programmable electrometer (model 617, Keithley) and programmable voltage source (model 230, Keithley). All data was collected using an IBM-compatible PC via IEEE-488 interface.

3. Results and discussion

The Raman spectra of the carbon films deposited at different temperatures are shown in Fig. 1. It is observed that the peak positions are almost same for the films grown at different temperatures. The variation of the Raman *D* and *G* peaks and the ratio of their intensities provide information on sp^2/sp^3 and the sp^2 cluster size in the films. The Raman shift of the *D* band and *G* bands are

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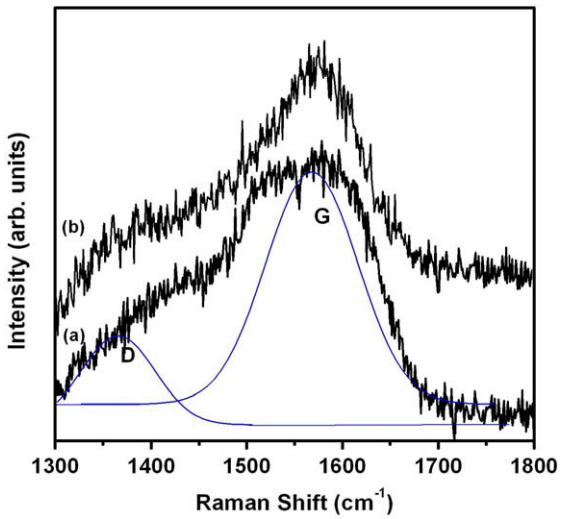

Fig. 1. Raman spectra of carbon film grown at (a) room temperature and (b) 200 °C.

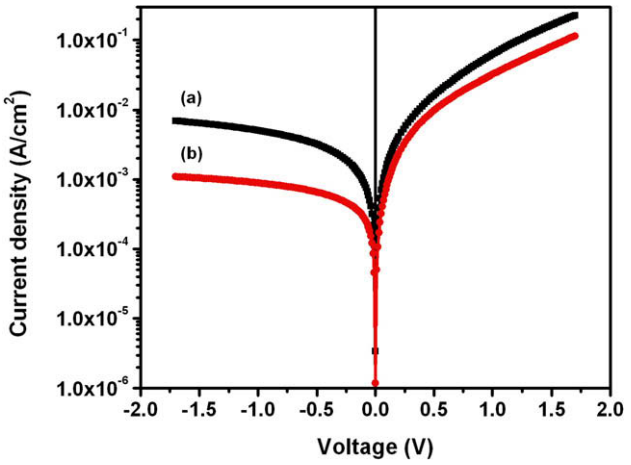

Fig. 2. *I–V* characteristic of Au/p-Si/carbon/Au structure grown at (a) room temperature and (b) 200 °C.

expected at 1350 and 1580 cm^{-1}, respectively for carbon-based materials [10]. The spectra show clear the *G* peak around 1580 cm^{-1} which suggests disordered diamond-like carbon characteristics of the amorphous carbon films [4].

The current–voltage characteristics of silicon–carbon junctions grown at two different temperatures are shown in Fig. 2. The non-linear *I–V* characteristics typical of diode behavior could be described by the thermionic emission model. According to thermionic emission theory, the current in such a device can be expressed as [11]

$$I = I_o[\exp(qV/nkT) - 1] \quad (1)$$

where I_o is the saturation current, k is the Boltzmann constant, T is the absolute temperature, q is the elementary electric charge, V is applied voltage, and n is the ideality factor. The saturation current (I_o) is expressed as

$$I_o = AA^*T^2 \exp(-q\phi_b/kT) \quad (2)$$

where A is the active device area, A^* is the effective Richardson constant equal to 32 $A/cm^2\,K^2$ for p-type silicon [12], and ϕ_b is the barrier height. The ideality factor is determined from the slope of the linear region of the forward bias In*I* versus *V* plot. The ideality factor is expressed as

$$n = [q/kT] \cdot [dV/d(\ln I)] \quad (3)$$

whereas the barrier height of the device is calculated using the equation

$$\phi_b = kT/q \ln(AA^*T^2/I_o) \quad (4)$$

The barrier height is estimated to be 0.37 and 0.41 eV for junctions fabricated at room temperature and 200 °C, respectively. The value of ideality factor at low and high voltage is estimated to be 1.12 and 2.32, respectively for junctions grown at room temperature. We observe a decrease in ideality factor (1.06 and 2.31, at low and high voltage, respectively) for junction grown at 200 °C. The ideality factor for ideal diode is reported as 1 at low voltage and 2 at high voltage [13]. In general, high value of ideality factor results from the presence of a native oxide layer, accelerated recombination of electrons and holes in depletion region, interfacial layer [14], and imperfections [15].

Fig. 3 exhibits the double logarithmic forward bias *I–V* characteristics of the p-Si/carbon junction. The log(*I*)–log(*V*) plot clearly shows the power law behavior of current and voltage. The power low behavior indicates that charge transport through the junction is influenced by space-charge-limited current (SCLC) process. From the double logarithmic plot of forward bias *I–V* characteristic, we can identify three linear regions. The slopes of region (I), (II), and (III) are 1.1, 1.4 and 2.2 for the junctions grown at room temperature, while slopes for films grown at 200 °C are 1.2, 1.5 and 2.2, respectively. The region (I) shows an ohmic behavior. The region (III) has a slope of 2.2 which is seen for junctions that exhibit SCLC with no traps. Such type of SCLC with no traps is given by Child's law [16].

$$I = (9/8)q\varepsilon_r\varepsilon_o\mu V^2/d^3$$

where $\varepsilon_r\varepsilon_o$ is dielectric permittivity, μ is the carrier mobility, and d is the thickness.

The nature of the non-linear *I–V* characteristics in forward bias depends on the series resistance (R_s) of the junction. If the series resistance is high, the non-linear forward bias *I–V* curve will show wide curvature, and if the effect of series resistance is less, then the non-linear region of the forward bias *I–V* curve will be small [17]. The series resistance of the carbon/p-silicon device can be estimated using Cheung and Norde methods. According to Cheung

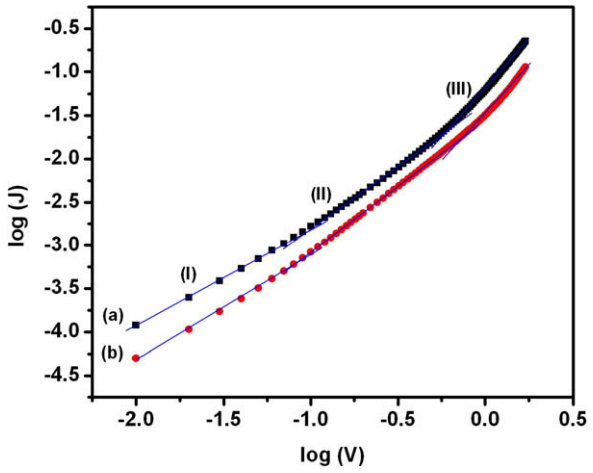

Fig. 3. The forward bias log(*I*)–log(*V*) plot of Au/p-Si/carbon/Au structure grown at (a) room temperature and (b) 200 °C.

and Cheung's method, the forward bias I–V characteristic of a device having series resistance is given as [18]

$$I = I_o \exp[q(V - IR_s)/nkT] \quad (5)$$

where the IR_s is the voltage drop across the device series resistance. The values of series resistance, ideality factor and barrier height are determined using the following equations.

$$dV/d(\ln I) = nkT/q + IR_s \quad (6)$$

$$H(I) = n\phi_b + IR_s \quad (7)$$

$$\text{where } H(I) = V - (nkT/q)\ln(I/AA^*T^2) \quad (8)$$

A plot of $dV/d(\ln I)$ versus I will be linear and the slope will give the value of series resistance and the intercept will give the device ideality factor. We have obtained n and R_s as 4.25 and 2.67 kΩ, respectively for junctions grown at room temperature and 4.59 and 3.12 kΩ, respectively for junctions grown at higher temperature. We observe that there is a difference between the values of ideality factor obtained from the $\ln I$–V and the $dV/d(\ln I)$–I plots. This difference is believed to be due to the presence of series resistance, interface states, and the voltage drop across the interfacial layer [19]. Series resistance and barrier height can also be calculated from Eq. (7) using the value of ideality factor obtained from Eq. (6). The slope of the $H(I)$ versus I plot gives series resistance and intercept gives the barrier height (Fig. 4). The obtained values of barrier height for device grown at room temperature and 200 °C are 0.34 and 0.39 eV, respectively, while the values of series resistance are 2.83 and 3.23 kΩ, respectively.

The second method used to determine the series resistance is due to Norde [20], which uses the following function to obtain the series resistance and barrier height.

$$F(V) = V/\gamma - (kT/q)\ln[I(V)/AA^*T^2] \quad (9)$$

where γ is the integer (dimensionless) greater than n. It is taken as 2 here. $I(V)$ is the current obtained from the I–V characteristic plot. The value of the barrier height is calculated after getting minimum of the F versus V plot. Fig. 5 shows the $F(V)$ versus V plot of the devices grown at different temperatures. The barrier height is given as

$$\phi_b = F(V_o) + V_o/\gamma - kT/q \quad (10)$$

where $F(V_o)$ is the minimum point of $F(V)$ and V_o is the corresponding voltage. The value of the series resistance is calculated using

$$R_s = kT(\gamma - n)/qI \quad (11)$$

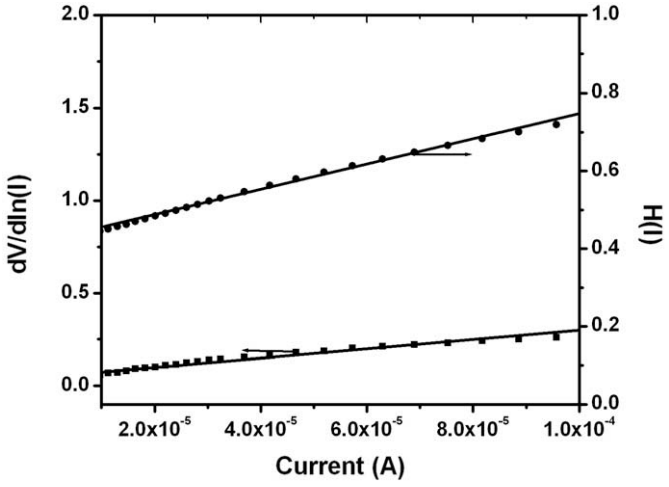

Fig. 4. The forward bias $dV/d(\ln I)$–I and $H(I)$–I plot for junction grown at room temperature.

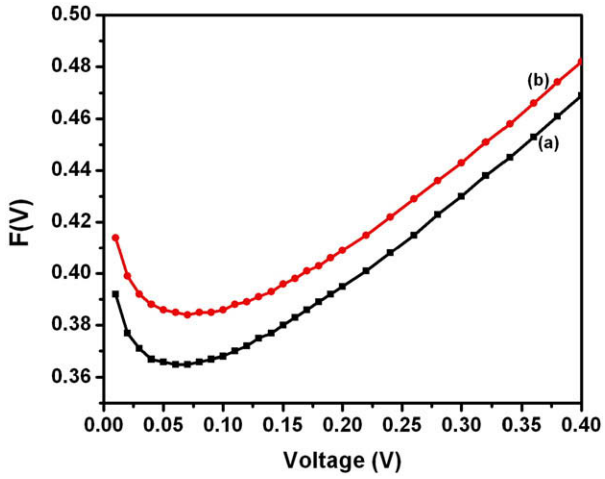

Fig. 5. $F(V)$–V plot of the Au/p-Si/carbon/Au junction grown at (a) room temperature and (b) 200 °C.

The values of barrier height and series resistance are obtained to be 0.37 eV and 2.98 kΩ, respectively for room temperature grown junctions. It is observed the barrier height increases (0.41 eV) for the device grown at high temperature. The increase in barrier height may be due to high series resistance (3.92 kΩ) of the junction. A small difference in R_s obtained from the Cheung and the Norde methods, is due to the fact that Cheung's model is applicable in high voltage region of the forward bias $\ln I$–V characteristics while Norde's model is applied to the full voltage range of forward bias $\ln I$–V characteristics of the junctions.

4. Conclusions

Carbon/p-Si junctions were fabricated at different temperatures using pulsed laser deposition technique. The current–voltage characteristics of the junctions showed typical diode behavior. Various diode parameters such as ideality factor, barrier height, and series resistance were calculated using different methods. There was a good agreement between the diodes parameters obtained from different methods.

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