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Moderately-doped Schottky barriers: a description using thermionic emission over a wide temperature range

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Abstract

We report on a low temperature study of Schottky barriers between Au, Cr or Al electrodes deposited directly onto moderately-doped Si or GaAs substrates with doping densities in the range 1×10^{15}–3×10^{16} cm^{-3} and find the unexpected result that for temperatures $5 < T \leqslant 150$ K both the zero-voltage Schottky barrier height, $\Phi^0_{SB}(T)$ and the reciprocal ideality factor, $\eta(T)^{-1}$, have linear temperature dependences that extrapolate to zero at $T = 0$. Accordingly, the thermionic emission equation with these modified temperature-dependent parameters gives a good description of the current–voltage (I–V) characteristics at temperatures where thermionic field emission and field emission (direct tunneling) in addition to thermionic emission *are known to be important*. Our analysis utilizes a barrier inhomogeneity model to show that the temperature-independent product $\Phi^0_{SB}(T)\eta(T)$ determined from forward bias characteristics defines a flat band voltage which is shown to be equivalent to the built-in voltage separately determined by extrapolation of capacitance versus voltage measurements made in the reverse bias region.

Keywords: Schottky barriers, thermionic emission, thermionic field emission, field emission, Schottky barrier tunneling

(Some figures may appear in colour only in the online journal)

1. Introduction

When a metal or semimetal is placed into intimate contact with a doped semiconductor the equilibration of the chemical potential of the semiconductor with the Fermi energy of the metal gives rise to Schottky barriers [1, 2] with corresponding current–voltage (I–V) diode characteristics that are well described by thermionic emission (TE), a theory that incorporates the voltage and temperature dependent forward and reverse bias flow of carriers that are thermally excited over the intervening barrier [3, 4]. Despite the relative simplicity of the TE model, there are no simple comprehensive models that satisfactorily explain the characteristics of individual metal–semiconductor interfaces, a problem especially complicated by the presence of both physical and chemical constraints at the interface [5]. A further complication in the interpretation of the I–V characteristics is associated with temperature and voltage dependence where it is known that thermal field emission and direct tunneling through the barrier become increasingly more important as the temperature is lowered and that the TE equation, which in principle describes only charge transported over the barrier, should therefore become increasingly less relevant at these low temperatures. In contrast to this expected complication, we demonstrate here that the TE equation can be modified in a straightforward way to give a full and relatively accurate description of Schottky behavior characteristics to temperatures as low as 5.0 K where tunneling and thermal field emission become increasingly important.

2. Experimental methods

Commercially available (MTI Corp) n-type GaAs ((1 0 0) Si doped, 500 μm thick, doping density $N_d \sim 3-6 \times 10^{16}$ cm^{-3},

Table 1. Metal/semiconductor Schottky barrier parameters.

	Φ^0_{SB}(eV)/η @ 300K	V^{sat}_{bi}(eV) @ 10 kHz	ϕ_{fb}(eV)	$\bar{\Phi}^0_{SB}$(eV)/ρ_2	$s_1(\times 10^{-3}$eV K$^{-1})$	E_{00t}(meV)	E_{00exp}(meV)
Au/n-GaAs	0.928(44)/1.19(9)	1.04(15)	1.08(10)	1.04(13)/0.039(26)	6.31(9)	4.62(17)	17.1(4)
Cr/n-GaAs	0.684(61)/1.34(21)	1.07(9)	1.07(3)	0.912(57)/0.148(29)	3.23(11)	4.56(6)	29.5(2.4)
Al/n-GaAs	0.974(17)/1.29(1)	1.16(6)	1.24(10)	0.971(116)/0.217(28)	5.07(8)	4.79(9)	19.8(1.2)
Au/n-Si	0.792(35)/1.23(6)	1.07(10)	1.19(13)	0.796(105)/0.331(14)	2.73(9)	0.24(2)	49.7(5)
Cr/n-Si	0.682(20)/1.36(19)	1.05(5)	1.02(10)	0.852(109)/0.165(23)	1.93(6)	0.22(1)	54.1(8)
Au/p-Si	0.294(20)/1.03(7)	0.339(56)	0.312(28)	0.310(28)/0.006(1)	1.94(2)	0.73(1)	19.6(9)
Cr/p-Si	0.431(25)/1.14(3)	1.17(5)	0.486(45)	0.432(63)/0.112(38)	2.23(28)	0.75(3)	23.1 (3.7)
Al/p-Si	0.465(104)/1.05(4)	1.01(6)	0.580(84)	0.527(104)/0.092(19)	1.96(36)	0.77(7)	28.0(7.0)

resistivity $\rho \sim 2$–$5 \times 10^{-2}\ \Omega \cdot$ cm), n-type Si ((1 0 0) P doped, 500 μm thick, $N_d \sim 1$–3×10^{15} cm^{-3}, $\rho \sim 1$–$10\ \Omega \cdot$ cm), and p-type Si ((1 0 0) B doped, 500 μm thick, $N_a \sim 1$–3×10^{16} cm^{-3}, $\rho \sim 1$–$10\ \Omega \cdot$ cm) were used. Low resistance back Ohmic contacts were made using multi-metal deposition followed by rapid thermal anneals (RTA) on RCA-I method [6] cleaned wafers. For n-type GaAs, 50 Å Ni/450 Å Au/450 Å Ge/1000 Å Au were sequentially deposited on the non-polished side via thermal evaporation in vacuum space ($<2 \times 10^{-6}$ Torr). The multilayer was then RTA processed at 450 °C for 1 min in dry N_2 flow. Low resistance back Ohmic contact for the GaAs substrates could be achieved for temperatures as low as 5 K. For both n- and p-type Si, 2000 Å Al/500 Å Au were deposited and RTA was applied at 450 °C for 5 min in dry N_2 flow. In contrast to the GaAs, low resistance back Ohmic contact for the Si wafers could only be achieved for temperatures as low as 40 K, below which carrier freeze out occurred.

Prior to the fabrication of our Schottky barriers, the semiconductor wafers were first cleaned via RCA-I method for removing any native organics and soaked into 3:1:50 HNO_3–HF–H_2O for 2 min in order to remove any native oxides. Then, 80 nm Au, 50 nm Al and 50 nm Cr were deposited, via thermal evaporation in vacuum space ($<2 \times 10^{-6}$ Torr), on the polished side of n-type GaAs, n- and p-type Si wafers. Eight different Schottky barriers, which are listed in the first column of table 1, were measured.

All measurements were performed over a wide range of temperature using a quantum design physical properties measurement system (PPMS). Samples were mounted on a commercial PPMS puck and inserted into a homemade low-noise shielded chamber. The current–voltage (I–V) characteristics of the Schottky barriers were processed using a Keithley 2400 sourcemeter. I–V measurements were taken at room temperature and used to determine the zero-bias Schottky barrier height Φ^0_{SB} and corresponding idealities η. These values are listed in the second column of table 1 and will be discussed in detail below. Importantly, they are in good agreement with previous works [7–9]. From capacitance–voltage (C–V) characteristics measured by a HP4284A precision LCR meter, information about the Schottky barrier profile including built-in potential, depletion region width and carrier concentration was obtained. We report here only on those diodes having sufficiently low ohmic contact resistance to the semiconductors under investigation to assure negligible difference between the capacitances measured in series-mode and parallel-mode. Under these conditions the measured complex impedance can be reliably modeled as a depletion resistor in parallel with the depletion capacitor [10]. Consequently, the parallel-mode measured capacitance accurately represents the capacitance C_{dep} of the depletion region of our Schottky barriers.

3. Thermionic emission

Our analysis begins with the thermionic emission equation [3–5]

$$I(T,V) = I_S(T)[e^{(V-I\cdot R_S)/\eta(T)k_BT} - 1] = AA^*T^2e^{-e\Phi^0_{SB}(T)/k_BT}[e^{(V-I\cdot R_S)/\eta(T)k_BT} - 1], \quad (1)$$

where the saturation current, $I_S(T) = AA^*T^2e^{-e\Phi^0_{SB}(T)/k_BT}$, is written as a prefactor to a term that is exponentially sensitive to voltage. The critical parameters of the theory which can be extracted experimentally from the I–V characteristics are the zero-voltage Schottky barrier height $\Phi^0_{SB}(T)$, the voltage-independent ideality factor $\eta(T)$ and the series resistance $R_s(T)$ which includes the contact resistances, the semiconductor resistance and the resistance associated with the Schottky barrier. The remaining constants are the area A, the Richardson constant A^* and the Boltzmann constant k_B. In forward bias for $V > k_BT$ the exponential term in the square brackets dominates over unity and there is a strong forward bias current whereas for reverse bias the exponential term is less than unity and the significantly smaller saturation current $I_S(T)$ dominates the reverse bias characteristics.

3.1. Reverse bias

In the reverse bias region the depletion region is thicker than it is in forward bias and capacitance measurements can be used to measure the built-in potential V_{bi} depicted schematically in figure 1. To interpret these capacitance measurements, the abrupt junction approximation is made in which it is assumed that ionized donor (acceptor) impurities are uniformly distributed for n-type (p-type) semiconductors. Under these conditions, it is straightforward to use Poisson's equation to solve for the potential distribution and show that the reciprocal square areal capacitance $1/C^2 = 2(V_{bi} - V)/(q\epsilon_0\varepsilon_s N_D)$ can be fit to straight lines with slopes proportional to the reciprocal of the density of donor impurity ions N_D with an intercept

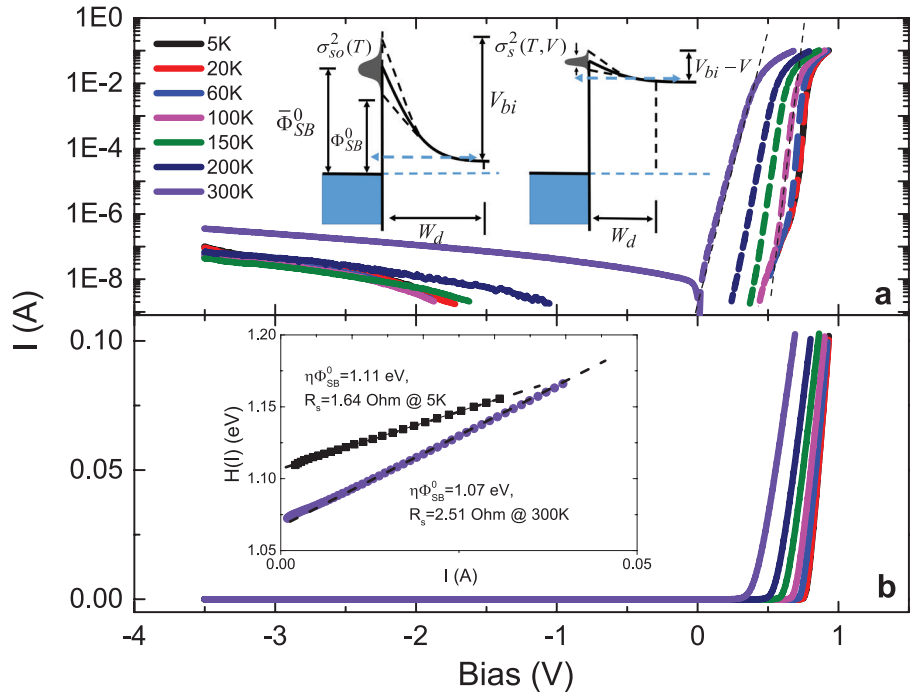

Figure 1. Current–voltage plots at the indicated temperatures for a Au/n-GaAs Schottky diode on log-linear (panel (a)) and linear–linear (panel (b)) scales. The inset of panel (a) depicts respectively schematics of barrier heights, the built-in potential $V_{\rm bi}$ and current distributions under the indicated bias conditions and in panel (b) linear Cheung plots for data at 300 (lower) plot and 5 K (upper) plot.

$V = V_{\rm bi}$ determined by the built-in potential [4]. Here q is the electric charge, ϵ_0 the vacuum permittivity and ε_s the relative permittivity of the semiconductor. Examples of such plots are shown in the inset of panel (b) of figure 3. At the lowest temperatures where $V_{\rm bi}$ is saturated at a maximum we write $V_{\rm bi} = V_{\rm bi}^{\rm sat}$. The good agreement of our C–V measured experimental carrier concentration (derived from the slopes of the voltage-dependent $1/C^2$ measurements, for all the Schottky barriers discussed in table 1), with the factory information also verifies the accuracy of the capacitance–voltage measurements applied to our Schottky barriers.

3.2. Forward bias

An ideal Schottky barrier with no second order effects has an ideality $\eta = 1$, i.e. the barrier heights are uniformly flat and homogeneous, there are no interface states at the metal-semiconductor boundary, there is no reduction of the barrier height by image forces, and there are no tunneling or generation/recombination currents within the depletion region. For the purposes of this work we incorporate these second order effects into equation (1) using a barrier inhomogeneity model described below. We justify this approach for two reasons: firstly the room temperature idealities are already reasonably close to unity, thereby implying that second-order effects are present but not dominant and secondly, as we will see below, with decreasing temperature $\eta(T)$ increases significantly above unity due to the importance of thermal field emission and field emission (tunneling).

Early workers [11–14] have recognized that the barrier height of a Schottky barrier is electric field dependent and that the fundamental barrier height should be independent of electric field and therefore defined under flat band conditions where there is no band bending at the interface. Accordingly an ideality greater than unity must be incorporated in equation (1) to unmask the differences between the experimentally accessible zero-voltage Schottky barrier height $\Phi_{\rm SB}^0(T)$ and the voltage-dependent quantity $\Phi_{\rm SB}(T, V)$, which at flatband $V = \phi_{\rm fb}$ defines the intrinsic Schottky barrier in the absence of electric fields at the metal/semiconductor interface. We will show below that there is a strong correlation between $\Phi_{\rm SB}^0(T)$ and $\eta(T)$ enforced by a potential fluctuation model arising from inhomogeneous Schottky barrier heights [12–16]. This condition becomes particularly pronounced at low temperatures where thermal field emission and tunneling dominate.

Although $\Phi_{\rm SB}(T, V = \phi_{\rm fb})$ and not $\Phi_{\rm SB}^0(T)$ is the fundamental barrier height, the quantities in equation (1) which can be accessed experimentally are the zero-voltage Schottky barrier $\Phi_{\rm SB}^0(T)$ and the voltage-independent ideality $\eta(T)$. We illustrate the implications of these considerations in our analysis by referring to the temperature dependent I–V data of a Au/n-GaAs diode depicted in figure 1. In forward bias the log-linear dependence of equation (1) is obeyed (panel a, dashed lines) for more than four decades in current. Since the data are analyzed only over the region where the voltage drop $IR_{\rm S}$ is negligible, we can extract from plots of $\log(I)$ versus $V/(\eta(T)k_{\rm B}T)$ rather accurate estimates of the *voltage-independent* values of $\eta(T)$. These values are listed in column 2 of table 1 for the 300 K data on the Au/n-GaAs diode shown in figure 1. Similar data have been acquired and listed in table 1 for the eight different diodes made with different combinations of metals and semiconductors identified in column 1.

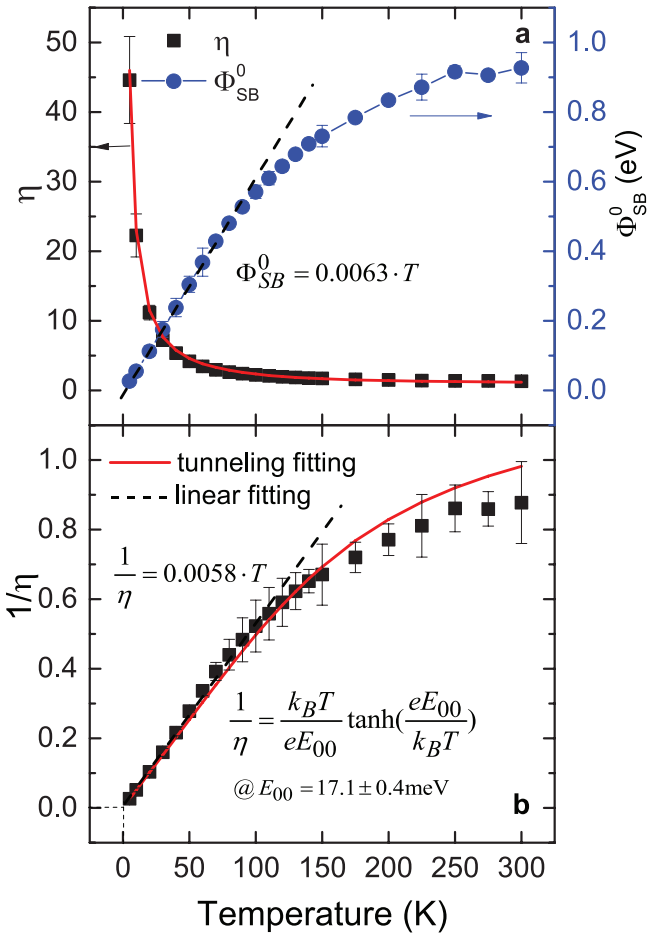

Figure 2. Temperature dependence of η (black squares) and Φ^0_{SB} (blue circles) in panel (a) and η^{-1} in panel (b) shows that η diverges to large values (>40) at low temperatures and that for $T < 100$ K both η^{-1} and Φ^0_{SB} are linear in temperature (dashed lines) with extrapolations to zero at $T = 0$.

Once $\eta(T)$ is known, it is straightforward to transform equation (1) to the form

$$H(I) = V - \frac{\eta(T)k_BT}{e} \ln \frac{I}{AA^*T^2} = IR_s + \eta(T)\Phi^0_{SB}(T) \qquad (2)$$

where Cheung's function [17] $H(I)$ plotted against I as done in the panel (b) inset of figure 1 takes on a linear dependence with slope R_s and intercept $\eta(T)\Phi^0_{SB}(T)$. The good linearity for the two temperatures (300 and 5 K) shown confirms agreement with thermionic emission (equation (1)) and reveals that the series resistance R_s which includes contact resistance and is responsible for the current-limiting flattening of the curves at high forward bias is sufficiently low to avoid carrier freeze out problems to temperatures as low as 5 K. The avoidance of carrier freeze out by using shallow Si donor impurities with small effective masses [18] as we do in this paper, is essential for meaningful low-temperature measurements. Using these techniques we have found as shown in figure 2 that both η^{-1} and Φ^0_{SB} have linear temperature dependencies that extrapolate to zero at zero temperature. Accordingly, the ratio $\Phi^0_{SB}(T)/\eta(T)^{-1}$ appears to be independent of temperature with the product $\eta(T)\Phi^0_{SB}(T)$ having the values 1.07 and 1.11 eV at 300 and 5 K respectively as shown in the inset of figure 1(b).

We will show below that $\eta(T)\Phi^0_{SB}(T)$ is the flat band voltage which establishes the condition necesssary to obtain zero electric field at the metal semiconductor interface. To make this connection, we follow earlier authors [12–14] and write

$$\eta(T)^{-1} - 1 = -[\Phi_{SB}(T, V) - \Phi^0_{SB}(T)]/V \qquad (3)$$

which when substituting into equation (1) *without dropping* the −1 term gives the result

$$I(T, V) = AA^*T^2 e^{-e\Phi_{SB}(T,V)/k_BT}[e^{eV/k_BT} - e^{\Delta\Phi_{SB}(T,V)/k_BT}] \qquad (4)$$

where $\Delta\Phi_{SB}(T, V) = \Phi_{SB}(T, V) - \Phi^0_{SB}(T)$. Equation (4) reduces to a particularly simple form when $\Delta\Phi_{SB}(T, V) = 0$ (or equivalently when $\Phi_{SB}(T, V) = \Phi^0_{SB}(T)$) describing thermal emission (equation (1)) for a diode with ideality of unity [12]. Said in another way, $\eta(T) > 1$ is the consequence of the 'deformation of the spatial barrier distribution when a bias voltage is applied' [13].

4. Barrier inhomogeneity and voltage dependence

We now make the assumption that the Schottky barrier height $\Phi_{SB}(T, V)$ is a Gaussian distributed variable with probability distribution [11, 13–15], $P(\Phi_{SB}(T, V)) = (1/\sigma_S\sqrt{2\pi}) \cdot e^{-(\bar{\Phi}_{SB}(T,V) - \Phi_{SB}(T,V))^2/2\sigma_s(T,V)^2}$ having a mean value $\bar{\Phi}_{SB}(T, V)$ and standard deviation $\sigma_s(T, V)$. A similar expression holds for the zero-voltage probability $P(\Phi^0_{SB}(T))$ with voltage-independent standard deviation $\sigma_{s0}(T) = \sigma_s(T, V)|_{V=0}$. Using these Gaussian distributions to average over the exponential terms of equation (4), i.e. $\langle e^{-e\Phi_{SB}(T,V)/k_BT}\rangle = e^{-e(\bar{\Phi}_{SB}(T,V) - e\sigma_S^2(T,V)/2k_BT)/k_BT}$ with a similar expression for $\langle e^{-e\Phi^0_{SB}(T)/k_BT}\rangle$, we find that equation (4) ensues providing that the following two conditions are met:

$$\Delta\Phi_{SB}(T, V) = \bar{\Phi}_{SB}(T, V) - \Phi^0_{SB}(T) - e\sigma_s^2(T, V)/2k_BT$$
$$\Phi_{SB}(T, V) = \bar{\Phi}_{SB}(T, V) - e\sigma_s^2(T, V)/2k_BT \qquad (5)$$

For the case of zero bias ($V = 0$) equation (5) becomes

$$\Phi^0_{SB}(T) = \bar{\Phi}^0_{SB}(T) - e\sigma^2_{so}(T)/2k_BT. \qquad (6)$$

Using equations (3) and (5) we find the relation

$$\eta(T)^{-1} - 1 = -[(\bar{\Phi}_{SB}(T, V) - e\sigma_s^2(T, V)/2k_BT) - \Phi^0_{SB}(T)]/V = -\rho_1(T), \qquad (7)$$

where $\rho_1(T)$ is a temperature-dependent function independent of voltage. At $V = V^{sat}_{bi}$, equation (7) becomes

$$\Phi^0_{SB}(T) - V^{sat}_{bi} + e\sigma_s^2(T, V^{sat}_{bi})/2k_BT = -\rho_1(T)V^{sat}_{bi}, \qquad (8)$$

where we have made the association $V_{bi}(T) = \bar{\Phi}_{SB}(T, V^{sat}_{bi})$.

When V_{bi} is saturated as $T \to 0$ (as observed in T-dependent capacitance measurements) the bands are flat and there is no dispersion in the SBHs. In this limit it is reasonable to make the assumption that for any thermal emission theory, the following limit applies.

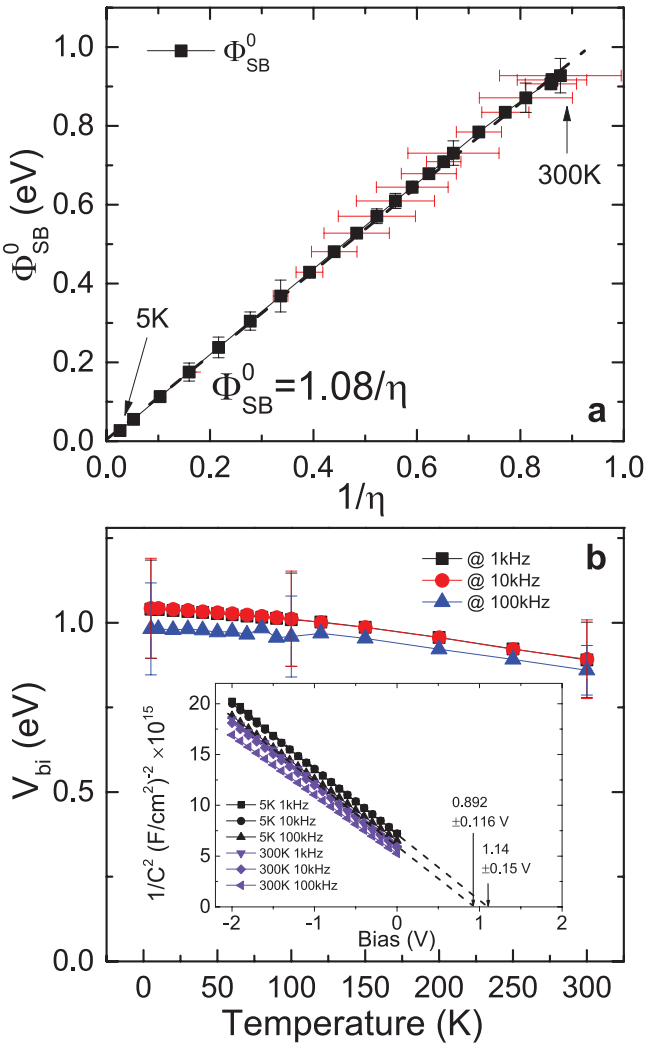

Figure 3. Panel (a): the linear dependence of $\Phi^0_{SB}(T)$ on $\eta^{-1}(T)$ discussed in the text validates the extraction of a flat band voltage, 1.08 eV, from forward bias measurements. Panel (b): the temperature dependence of the built-in potential V_{bi} at the indicated temperatures and frequencies show a small increase towards saturated values V^{sat}_{bi} with decreasing temperatures.

$$\lim_{V\to V^{sat}_{bi}} \frac{\sigma_s^2(T,V)}{T} = 0. \tag{9}$$

This is especially true at $T = 0$, since there are no thermally activated processes and thus variations in barrier heights would be irrelevant. Equations (7)–(9) combined then give

$$V^{sat}_{bi} = \bar{\Phi}_{SB}(0, V_{bi}(0)) = \eta(T)\Phi^0_{SB}(T) \tag{10}$$

which is a central result of this paper in agreement with the experimentally determined linear dependence of $\Phi^0_{SB}(T)$ on η^{-1} shown in figure 3(a). For the sake of clarity we use the symbol V_{bi} when discussing capacitance measurements made in reverse bias, the symbol $\bar{\Phi}_{SB}(T, V)$ for the average Schottky barrier height and the symbol ϕ_{fb} for the flatband voltage equal to the slope extracted from the linear dependence of $\Phi^0_{SB}(T)$ on $1/\eta(T)$ shown in panel (a) of figure 3. The data which include the origin reveal a best-fit value $\phi_{fb} = 1.08 \pm 0.10$ eV.

Before commenting further on the result of equation (10), it is instructive to tease out the temperature and voltage dependencies of the barrier height averages and the corresponding standard deviations. Firstly, we emulate the notation of Werner and Guttler [14] and combine equations (3), (5) and (6) to obtain

$$\eta(T)^{-1} - 1 = -[\bar{\Phi}_{SB}(T, V) - \bar{\Phi}^0_{SB}(T)]/V + (e/2k_BTV) \times [\sigma_s^2(T, V) - \sigma_{so}^2(T)] = -\rho_2(T) + (e/2k_BT)\rho_3(T) \tag{11}$$

where, like $\rho_1(T)$ in equation (7), both $\rho_2(T)$ and $\rho_3(T)$ are dimensionless temperature-dependent functions independent of voltage. With some algebraic manipulation using equations (5), (6), (9) and (10), it is straightforward to arrive at the expression $\rho_2(T) = 1 - \bar{\Phi}^0_{SB}(T)/V^{sat}_{bi}$ which is only weakly temperature dependent since $\bar{\Phi}^0_{SB}(T)$ is roughly constant over the whole temperature range as will be seen below. Using the result for V^{sat}_{bi} in equation (10) and solving for $\sigma^2_{so}(T)$ evaluated at $V = V^{sat}_{bi}$ in equation (11) we arrive at an expression involving linear and quadratic temperature corrections,

$$\sigma^2_{so}(T) = (2k_B/e)[\bar{\Phi}^0_{SB}(0)T - s_1T^2] \tag{12}$$

where we have again used $V_{bi}(T) = \bar{\Phi}_{SB}(T, V^{sat}_{bi})$ and s_1 is the experimentally determined slope of the linear dependence $\Phi^0_{SB}(T) = s_1T$ seen for example in figure 2(a).

5. Results and discussion

5.1. Tabulation of barrier parameters

Key parameters for our eight different diodes are summarized in table 1 and now discussed in reference to the above figures and accompanying equations. The room temperature zero-voltage Schottky barrier heights $\Phi^0_{SB}(T)$ and corresponding idealities in column 2 having values close to unity indicate that the diodes are of high quality and well described by thermionic emission in which the majority of carriers are excited over the barrier. The saturated built-in potentials V^{sat}_{bi} extracted from low-temperature capacitance measurements (panel (b) of figure 3) shown in column 3 correlate well with the flat band barrier heights ϕ_{fb} (column 4) extracted from the slopes of $\Phi^0_{SB}(T)$ plotted against $\eta(T)^{-1}$ as done in figure 3(a). The theoretical basis for this linear dependence is embodied in the development of equation (10).

Figure 4 is a plot of $\Phi^0_{SB}(T)$ versus $\eta(T)^{-1}$ for the eight diodes shown in table 1. We note that the linearity for the three diodes fabricated on *n*-type GaAs is excellent with the data extrapolating closely to the $T = 0$ origin. The data for the *n* and *p*-type Si substrates is likewise linear but do not reveal the same accuracy in extrapolating to the origin. We attribute these differences to the fact that for GaAs we can obtain data to temperatures as low as 5 K where R_s remains at a low value whereas for Si the lowest measuring temperature is ~40–50 K because of carrier freeze-out, i.e. a large current limiting R_s.

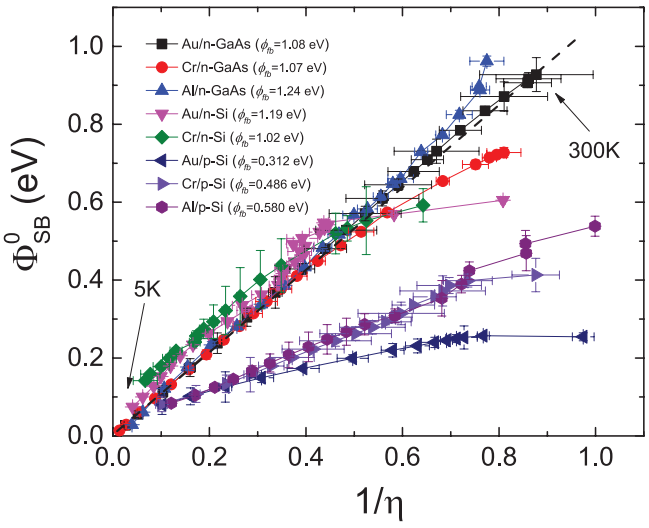

Figure 4. The linear dependence of $\Phi^0_{SB}(T)$ on $\eta^{-1}(T)$ discussed in the text validates the extraction of a flat band voltage, for all Schottky barriers in table 1, from forward bias measurements.

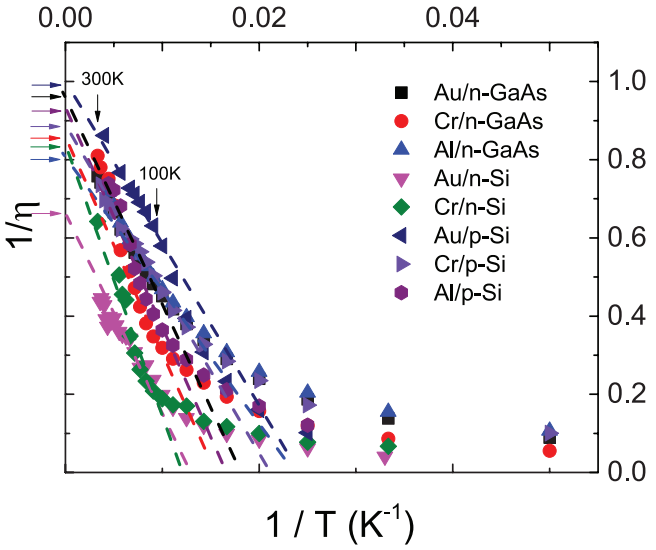

Figure 5. At high temperatures the linear dependence of $\eta^{-1}(T)$ versus T^{-1} discussed in the text validates the extraction of the parameter $\rho_2(T)$ for all Schottky barriers in table 1. The colored dashed lines act as indication of the linear fit, horizontal arrows indicate the intercepts.

As shown in the figure 5 plot of $\eta(T)^{-1}$ versus $1/T$ for all of our diodes, the linear dependencies indicated by the dashed lines for temperatures greater than ~100 K are in accord with equation (11). The color-coded intercepts to these high temperature data are marked by horizontal arrows which identify the intercept values of $1-\rho_2$ from which the entries for ρ_2 in column 5 of table 1 are computed. This high-temperature dependence has been seen in previous investigations of a variety of diodes [13, 19–21]. Using our experimentally determined values of ρ_2 and the relation $\bar{\Phi}^0_{SB}(T) = V^{sat}_{bi}(1-\rho_2(T))$ derived from our above definition of $\rho_2(T)$, we find that our high temperature estimate of $\bar{\Phi}^0_{SB}(T)$ shown in column 5 of table 1 is relatively unchanged from the low temperature estimates V^{sat}_{bi} (column 3) and ϕ_{fb} (column 4). Importantly, V^{sat}_{bi}, ϕ_{fb} and $\bar{\Phi}^0_{SB}(T)$ are roughly equivalent over the whole temperature range while the experimentally measured zero-voltage barrier height $\Phi^0_{SB}(T)$ decreases dramatically as temperature is lowered. The inequality $\Phi^0_{SB}(T) < \bar{\Phi}^0_{SB}(T)$ has also been noted and ascribed to inhomogeneous barriers in higher temperature studies of PtSi/Si diodes [14].

The column 6 entries of table 1 list the experimentally determined values of s_1, the experimentally determined slope of the linear dependence $\Phi^0_{SB}(T) = s_1 T$ shown for example in the plot of figure 1(a) for the Au/n-GaAs row 1 entry of the table. Since the zero bias standard deviation is temperature dependent as shown in equation (12), we calculate the maximum value σ^0_{SB}, to be approximately 0.10 eV. For all the diodes listed in table 1, we find the typical sizes of σ^0_{SB} to be within 8–15% of the value of $\bar{\Phi}^0_{SB}$.

5.2. Tunneling

It has long been recognized that field emission (tunneling) and thermionic field emission (thermally assisted tunneling) are responsible for excess forward and reverse bias currents of Schottky diodes [11, 22]. Accordingly, the excess currents associated with field emission and thermal field emission, which both increase with decreasing temperature, are associated with concomitantly decreasing barrier heights. At first sight it seems mysterious, if not unphysical, that $\Phi^0_{SB}(T)$ should vanish at $T = 0$ simultaneously with $\eta(T)$ becoming very large. For direct tunneling using a thermionic emission model this is an expected result since thermal activation plays no role for electrons transferred at constant energy from the Fermi energy of the semiconductor to the metal. Such processes have been discussed for low resistance ohmic contacts [23] and directly observed for example in Au/Nb:$SrTiO_3$ Schottky junctions [24].

For small currents ($I \ll V/R_s$) and low temperatures, it is straightforward to see from the thermionic emission equation, equation (1), that since $\Phi^0_{SB}(T)$ and $\eta(T)^{-1}$ are linear in temperature, then the temperature dependence in both exponentials cancels. The only temperature dependence remaining is the T^2 term in the prefactor, which has its physical origin in the Fermi factors used in the calculation of thermionic emission. Accordingly the thermionic equation does not permit flow of current over the barrier at $T = 0$ since there are no thermally excited carriers. The bands however retain their curvature thereby determining the height and shape of the tunnel barrier.

Clearly when $T = 0$ quantum tunneling is present (i.e. the flow of charge at constant energy through the barrier) the T^2 prefactor of the thermionic emission (equation (1)) precludes the flow of thermally excited carriers over the barrier. To include thermal field emission, which is a combination of thermal excitation and tunneling, a more appropriate theory describing the I–V characteristics reflects a hybrid combination of the quantum mechanical WKB approximation and thermal excitation [3, 11, 22]. The resulting transport equation, $J = J_s e^{V/E_{00}\coth(eE_{00}/k_BT)}$, includes a characteristic

parameter, $E_{00} = \hbar\sqrt{N_d/4m^*\varepsilon}$ for tunneling which separates the region for pure thermionic emission ($k_BT \gg E_{00}$) and pure field emission ($k_BT \ll E_{00}$). As with pure thermionic emission (equation (1)) there is an exponential sensitivity to voltage.

By analogy with the ideality parameter of equation (1) [3, 25] we find the reciprocal ideality parameter for the tunneling model to be

$$1/\eta(T) = (k_BT/eE_{00})\tanh(eE_{00}/k_BT). \quad (13)$$

At low temperatures this expression has the linear in T dependence extracted from our thermionic emission analysis as denoted by the dashed line of figure 2(a) but over a larger temperature range allows a best fit estimate $E_{00} = 17.1$ meV for the Au/*n*-GaAs diode of table 1. As can be seen from the column 7 and 8 entries of table 1 E_{00} extracted from $1/\eta(T)$ versus T fits (column 7) are systematically larger than theoretical predictions (column 8). Qualitatively this difference can be attributed to the fact that the voltage corrections necessary to achieve flatband conditions are larger and hence $\eta(T) \propto eE_{00}/k_BT$ is necessarily greater when tunneling is present.

As a parenthetical remark we note that numerous previous authors [11, 13, 16, 22, 26] have chosen to rewrite the diode (equation (1)) by setting $\eta = 1$ and replacing T by $T + T_0$ where T_0, an additive constant, replaces η, a multiplicative correction, to parameterize excursions from ideal thermionic behavior. The two models are made equivalent by setting $\eta(T) = 1 + T_0/T$. Written in this manner, T_0 serves to mark a crossover temperature where for high temperatures $T \gg T_0$, $\eta(T) = 1 + T_0/T$ is slightly larger than unity as is observed for most diodes measured at room temperature [13, 19–21, 10] including ours (see column 2 of table 1, but for low temperatures $T \ll T_0$, $\eta(T) \propto 1/T$ as has been experimentally determined in this manuscript. In combination with the tunneling interpretation presented in the previous paragraph we see that $T_0 = eE_{00}/k_B$ and that T_0 is thus directly related to the dominance of tunneling in Schottky diodes. For Au/ *n*-GaAs diode, the theoretical and experimental T_0 are calculated as E_{00t} and E_{00exp} in table 1 as 53.6 K and 200.1 K respectively.

6. Conclusion

The arguments in this manuscript do not detract from the necessity of formulating a more detailed theory that includes thermal excitation, field emission and thermal field emission for a comprehensive understanding of charge transport through moderately-doped Schottky barriers. In this paper we have focused primarily on the well known thermionic emission equation and found that with a few straightforward modifications inspired by our investigation of low temperature behavior, a rather complete description of charge transport through 'moderately-doped' Schottky barriers can be obtained. Moderate doping restricts our discussion to semiconductors with doping densities in the approximate range 1×10^{15}–3×10^{16} cm^{-3}, a range where we have found that at low temperatures both tunneling (I–V characteristics) and capacitance (static electric potentials) can be simultaneously measured. Moderate doping thus leads to a 'sweet spot'; lower doping would give an R_s that is too high thereby limiting the current that can flow through the diode and higher doping would place the diode firmly in the tunneling regime where different theory applies [22, 24, 25, 27, 28]. We expect that our results will still apply for more highly doped samples where tunneling plays an important role with a behavior at higher temperatures similar to the case of low temperature tunneling in moderately-doped Schottky barriers as described in this manuscript.

Our description is accurate down to low temperatures where thermal field emission and field emission are known to be important. We have made a critical distinction between experimental observables such as the zero-voltage Schottky barrier height $\Phi^0_{SB}(T)$ and the voltage-independent ideality factor $\eta(T)$ and shown how these parameters can be connected to the electric field independent average barrier height $\bar{\Phi}^0_{SB}(T)$ and its variance $\sigma^2_{so}(T)$. Interestingly, as equation (10) shows, capacitance measurements made in reverse bias are a direct measure of $\bar{\Phi}^0_{SB}(T)$ which is found to be equivalent to the product $\eta(T)\Phi^0_{SB}(T)$ of quantities measured in forward bias at currents significantly lower than the saturation currents limited by the value of R_s.

Knowledge of these barrier parameters not only is an essential starting point for a full quantum mechanical treatment of transport by tunneling but importantly provides immediately useful information about interface charge redistribution associated with the choice of metal (or semimetal) in contact with the semiconductor. Contributions to the charge distribution at the interface come from both the metallic and semiconductor sides of the interface. One can imagine for example using a metallic electrode which undergoes a structural transition driven by a charge density wave which terminates with a surface charge density at the interface, giving rise to a sudden change in the Schottky barrier height. We anticipate that our understanding of Schottky barriers as presented here will facilitate understanding of the novel physics expected when exotic metals harboring unusual electronic structure such as charge density waves or superconductivity are directly connected to semiconductors.

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