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Scrutinization of non−saturation behaviour of reverse current−voltage characteristics in Ni/SiO2/p-Si/Al diodes

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ABSTRACT

The present work is an endeavour to investigate non−saturation behaviour of reverse current in Ni/SiO_2/*p*-Si/Al over a wide low temperature range of 70–300 K at step of 10 K using well accepted models i.e., Poole-Frenkel emission, Schottky emission and Fowler−Nordheim tunneling mechanisms. The results of the study revealed that Schottky emission has the dominance over Poole-Frenkel emission in the temperature range of 200–300 K with the trap state activation energy of 0.17 eV. In the remaining temperature range trap assisted tunnelling and involvement of other mechanisms were suggested. Further, the Fowler−Nordheim tunneling mechanism was found to be effective above reverse bias of 0.5 V over the entire temperature range of 70–300 K. Thus, variation of barrier height with temperature was examined using Fowler−Nordheim tunneling model and it was found to increase from 0.17 eV to 0.28 eV as temperature varied from 300 to 70 K. The increase in barrier height with decrease in temperature corroborates the decrease in reverse current with temperature.

1. Introduction

Since, metal−semiconductor (M−S) and metal−insulator−semiconductor (MIS) or metal−oxide−semiconductor (MOS) junctions are the most basic and widely used components in the electronic circuits [1–11], thus detailed understanding of these structures from every perspective possible is vital to improve the performance, reliability and stability of the electronic devices. One of the major factors that effects the utility of these components in circuits is the high leakage current issues [12,13]. To date, SiO_2 based MOS diodes are the most basic and practical MOS structures. However, rigorous scaling of the electronic devices has decreased the utility of SiO_2 as gate dielectric due to high leakage current issues when SiO_2 thickness scaled down below 2 nm [1,5,14]. One of the possible causes for the high leakage current is related to the defect's generation during the growth process or the contacts metallization [10,15,16].

There are several models for analyzing the charge transport in MOS type structures of devices. Among these models, the Poole−Frenkel emission (PFE), Schottky emission (SE), Fowler−Nordheim tunneling (FNT) and space charge limited conduction (SCLC) mechanisms are well−known and widely used to interpret the experimental results as these model permits the estimation of various important parameters such as dielectric constant value, effective mass of electron and activation energy related to trap states [17–22].

Tomar et al. investigated current transport in reverse−biased Gr/SiC, Gr/GaAS, and Gr/Si Schottky junctions over temperature range of 250–340 K using PFE and SE mechanisms [23]. Jabbari et al. studied leakage current in (Pd/Au)/$Al_{0.22}Ga_{0.78}N$/GaN heterostructures [24]. They found evidences of PFE in the temperature range 200–300 K and FNT transport mechanisms in the

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temperature range 60–300 K for the fabricated structures. Kumar et al. fabricated Al/ZrO_2/*p*-Si/Al using solution processed synthesis technique and studied transport properties using various models at room temperature [25]. Guclu et al. studied reverse bias current–voltage–temperature characteristics of the Au/Ti/Al_2O_3/*n*-GaAS structures over temperature range of 80–300 K. They reported that the trap–assisted tunneling and Ohmic conduction mechanisms were the dominant mechanisms in these structures [26].

Most of the reviewed studies have focused on the analysis of forward bias current–voltage–temperature characteristics of MOS type structures, whereas investigation of non–saturation behaviour of reverse current in these structures have been relatively lesser reported. Therefore, present work is an endeavour to investigate non–saturation behaviour of reverse current in Ni/SiO_2/*p*-Si/Al structures over a low temperature range of 70–300 K at step of 10 K using well popular models i.e., PFE, SE and FNT of current transport mechanisms.

2. Experimental details

Fabrication of Ni/SiO_2/*p*-Si/Al Schottky diodes were done using *p*–type silicon wafers (Boron doped (100) orientation) having resistivity 1 Ω–cm. The wafers were first cleaned with organic solvents viz. trichloroethylene, acetone and methanol in sequence then rinsed in deionized water of resistivity 18 MΩ–cm followed by etching in a 40% hydrogen fluoride (HF) solution for 1 min. After cleaning process, the *p*–type Si wafer was loaded in 12 vacuum coating unit model–12A4D for the deposition of metal contacts. Aluminum having purity level 99.999% was deposited with thickness of ~200 nm on back side of the silicon wafer to form the Ohmic contact at a pressure of 3×10^{-6} mbar. After that, the thermal oxidation was carried out to grow SiO_2 layer on Si substrate by sintering the wafers in oxygen environment in a furnace. The process involves annealing of wafers at 700° C for 1 h in a flowing dry oxygen ambient at a rate of 1 lt min^{-1}. This process served both to sinter the Al and to form the interfacial oxide layer (SiO_2) on the top surface of the p-Si wafer. The SiO_2 film thickness was estimated to be 58 Å. Then nickel (Ni) film of thickness ~ 200 nm was deposited by thermal evaporation process using high purity nickel metal wire to form a Schottky contact [27]. In this way the Ni/SiO_2/*p*-Si/Al diode was fabricated and the schematic of the structure is shown in Fig. 1.

The temperature–dependent current–voltage measurements were performed using programmable Keithley–2400 source meter, a Lake shore model–331 temperature controller with close cycle helium refrigerator Sumitomo cryogenics HC–2.

3. Results and discussion

Fig. 2 shows the semi–logarithmic plot of reverse bias current-voltage characteristics of Ni/SiO_2/*p*-Si/Al MIS diode over a wide temperature range of 70–300 K in bias range of −2.0 to 0.0 V. From these characteristics it can be clearly visualized that the reverse current increases with increase in the reverse bias, as also evident from the actual plot of I–V shown in inset of Fig. 2. The non–saturation behaviour of reverse bias current in the diode is inconsistent with well–known thermionic emission (TE) theory, where for V < - 3 kT/q the reverse bias current should saturate which mathematically can be written as [1,23],

$$I_R(T) = AA^* T^2 \exp\left(\frac{-q\varphi_{b0}}{kT}\right) \tag{1}$$

where $I_R(T)$ is the reverse saturation current at zero–bias, φ_{b0}represents the zero–bias barrier height, A is the diode area, A* is for effective Richardson constant. The rise in current with reverse bias at fixed temperature probably indicates more migration of charges through or over insulating barrier in Ni/SiO_2/*p*-Si/Al which gives rise to non-saturating behaviour.

As can be seen in Fig. 3 (a) the barrier height derived from reverse current at different bias decreases sharply as reverse bias increases which implies that more charge carriers cross the barrier through or over the junction suggesting involvement of various conduction mechanisms. Further, the I–V characteristics shows that reverse bias current increases gradually with rise in temperature from 70 to 300 K. The increase in current is consistent with Eq. (1) which shows that as temperature increases the reverse current increases. It is the thermionic emission nature of charge carriers over the barrier at the interface [28]. The temperature dependence of the barrier height derived using Eq. (1) for reverse bias of 1 V is shown in Fig. 3 (b) which was found to decrease with decrease in

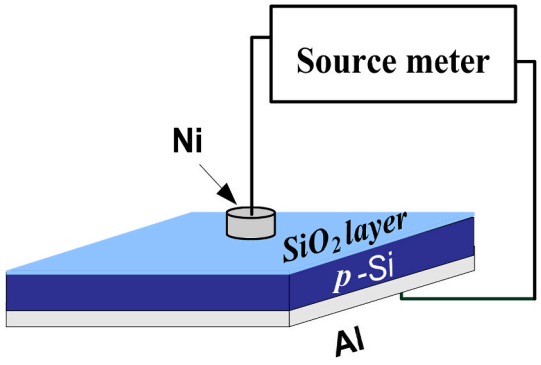

Fig. 1. Schematic of the Ni/SiO_2/*p*-Si/Al diode.

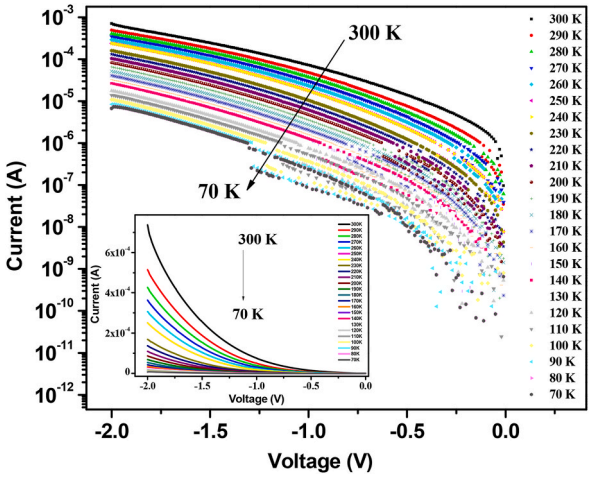

Fig. 2. Semi−logarithmic reverse current−voltage characteristics of Ni/SiO_2/*p*-Si/Al diode over a temperature range of 300–70 K.

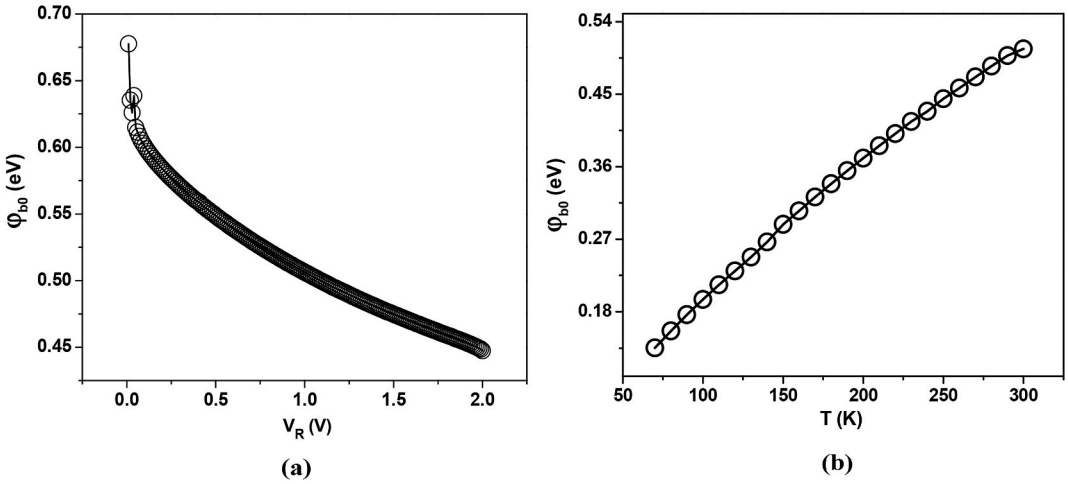

Fig. 3. Variation of Schottky barrier height as a function of (a) reverse bias measured at room temperature, (b) temperature at fixed bias voltage of −1 V.

temperature.

3.1. Analysis of reverse current using various models

To account for the non−saturation behaviour of reverse current in the diode, we have employed various current conduction mechanisms namely PFE, SE, and FNT.

To begin with, the Poole−Frenkel emission or hopping mechanism is considered for analysing the leakage current in the diode. This effect is believed to occur from low-field assisted thermionic emission of trap states from the bulk of dielectric material, most preferably hopping of electrons or holes from trap to trap and has prevalence when the conductivity of gate oxide has dependence on the external applied field. The trap state energy associated with the hopping of charges can be estimated using the following mathematical relation [29–31],

$$J_{PF} = CE\ exp\left(-\frac{q\varphi_t}{kT} + \frac{\sqrt{\frac{q^3E}{\pi\varepsilon_r}}}{kT} \right) \tag{2}$$

where C, φ_t, E, T, k represents a constant, emission barrier height of electron from its trap level, electric field, temperature and Boltzmann constant. Whereas, SE is a field assisted thermionic emission of charge carriers over the barrier and is given by Refs. [26,

32],

$$J_{SE} = A^{*} T^{2}\, exp\left(-\frac{q\varphi_t}{kT} + \frac{\sqrt{\frac{q^3 E}{\pi \varepsilon_r}}}{2kT} \right) \tag{3}$$

with. $A^{*} = \left(\frac{4\pi q m^{*} k^2}{h^3} \right)$

where A* is the Richardson constant and ε_r is the relative dielectric constant of the SiO_2 oxide layer. As Eq. (2) and Eq. (3) can be expressed as straight-line relations by taking $\log_e$ of both sides and plotting ln (J/E) versus $E^{1/2}$ and ln (J/T^2) versus $E^{1/2}$ for PFE and SE models, respectively. Fig. 4 (a) and (b) shows these plots for Ni/SiO_2/*p*-Si/Al over a wide temperature range of 70–300 K. The appearance of the straight region in these plots indicates the presence of both PFE and SE mechanism in the fabricated diode.

In order to identify the dominance of any of these two mechanisms, we can evaluate the emission coefficient (s) as [23],

$$s = \frac{1}{nkT}\sqrt{\frac{q^3}{\pi \varepsilon}} \tag{4}$$

where the value of n = 1 for PFE and n = 2 for the SE. The temperature dependence of *s* parameter for both are shown in Fig. 5 (a) and (b). The evaluated values of *s* are then compared with calculated values using Eq. (4) and we note that the values obtained for SE fit are nearly close to the theoretically obtained values than for PFE in the temperature range of 200–300 K as can be seen in Fig. 5 (a) and (b). The experimental and calculated values of *s* for PFE and SE are also listed in Table 1. Based on these observations, it can be concluded that none of the above implied CCMs exactly follow the actual mechanism happening in the diode. However, SE has superiority over PFE in the temperature range of 200–300 K.

Thus, the values of *s* obtained in the temperature range of 200–300 K for SE were used to estimate the trap state activation energy from the intercept [I (T)] of Eq. (3) as,

$$Intercept = I\,(T) = \frac{-q\varphi_t}{kT} + \log(A^{*}) \tag{5}$$

The I (T) versus 1/T plot is shown in Fig. 6. The value of barrier height estimated from the slope of Eq. (5) was 0.17 eV which is quite lower than the value estimated using Eq. (1). The obtained lower value of barrier height can be ascribed to trap state activation energy, which may be the possible cause for non-saturation behaviour of reverse current in the diode as the charge carriers can easily cross through the barrier. However, for the temperature range below 200 K, there may be possibility of involvement of more than one type of conduction mechanism.

Further, we analyzed the experimental data to distinguish the bias range for which current conduction is governed by FNT, in which the charge carriers' tunnel through the dielectric layer to the conduction band of dielectric material and generates leakage current density which is given as [33],

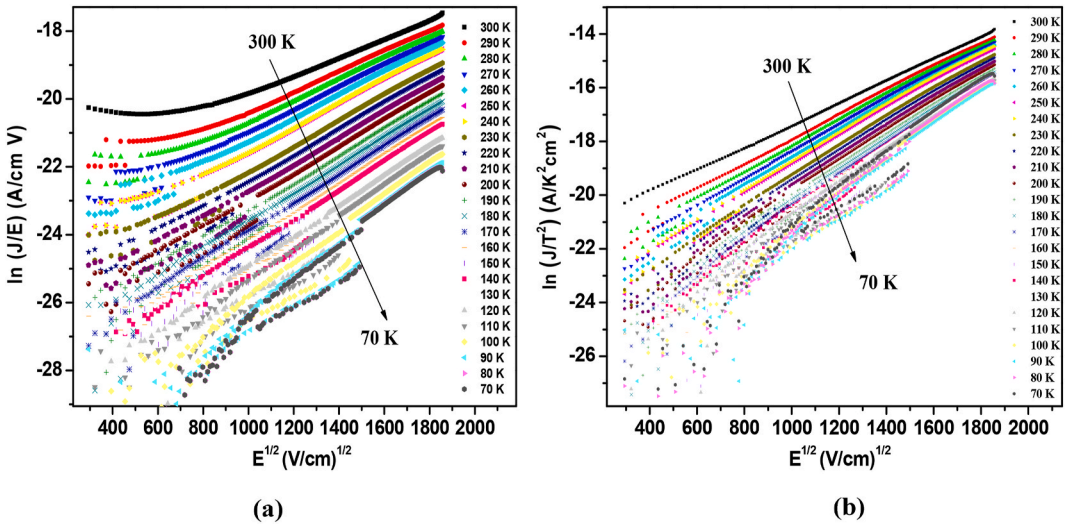

Fig. 4. (a) Poole–Frenkel, (b) Schottky emission temperature–dependent plots for Ni/SiO_2/*p*-Si/Al diode.

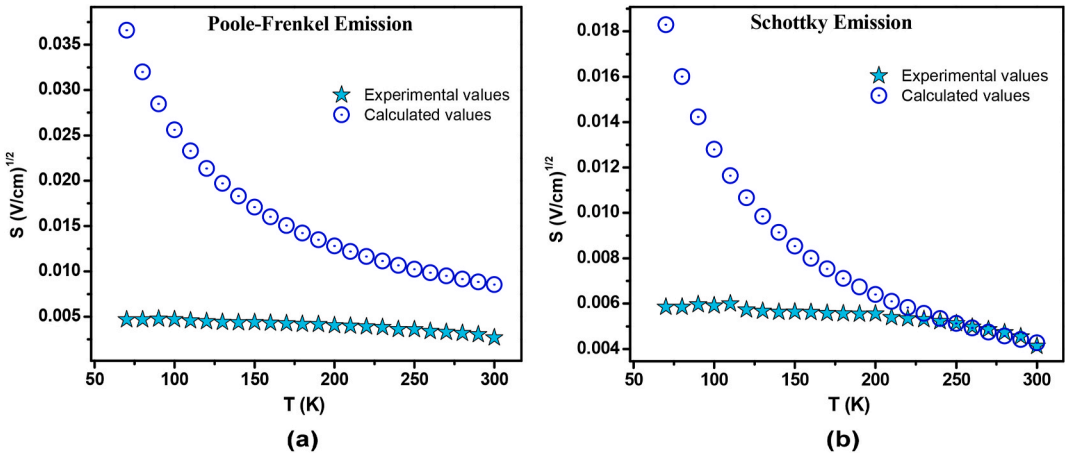

Fig. 5. Variation of experimental and calculated values of emission coefficient with temperature for (a) Poole–Frenkel, (b) Schottky emission.

Table 1
Comparison of slope values obtained by fitting and calculation for Poole–Frenkel and Schottky emission coefficients between 300 and 70 K for the Ni/SiO_2/*p*-Si/Al diode.

Temperature (K)	Poole-Frenkel emission $(V/cm)^{1/2}$		Schottky emission $(V/cm)^{1/2}$	
	From fitting	Calculated values	From fitting	Calculated values
300	0.00270	0.00854	0.00422	0.00427
290	0.00304	0.00883	0.00454	0.00442
280	0.00318	0.00915	0.00472	0.00457
270	0.00329	0.00949	0.00486	0.00474
260	0.00340	0.00985	0.00497	0.00493
250	0.00359	0.01024	0.00512	0.00512
240	0.00361	0.01067	0.00522	0.00534
230	0.00382	0.01114	0.00530	0.00557
220	0.00391	0.01164	0.00534	0.00582
210	0.00398	0.01220	0.00539	0.00610
200	0.00404	0.01281	0.00555	0.00640
190	0.00417	0.01348	0.00554	0.00674
180	0.00418	0.01423	0.00576	0.00711
170	0.00426	0.01507	0.00558	0.00753
160	0.00431	0.01601	0.00562	0.00800
150	0.00437	0.01707	0.00564	0.00854
140	0.00435	0.01829	0.00563	0.00915
130	0.00440	0.01970	0.00567	0.00985
120	0.00448	0.02134	0.00573	0.01067
110	0.00458	0.02328	0.00599	0.01164
100	0.00470	0.02561	0.00591	0.01281
90	0.00476	0.02846	0.00596	0.01423
80	0.00467	0.03201	0.00585	0.01601
70	0.00467	0.03659	0.00585	0.01829

$$J_{FN} = \frac{q^2}{8\pi h \varphi_b} E^2 exp\left(-\frac{8\pi\sqrt{2qm^*}}{3hE}\varphi_b^{3/2} \right) \quad (6)$$

where E, m^*, φ_b and h represents the applied electric field, electron effective mass, effective Schottky barrier height and h implies the Planck's constant respectively.

Using Eq. (6), the plot of ln (J/E^2) versus 1/E should yield a straight line, from the slope $\left(= \frac{8\pi\sqrt{2qm^*}}{3hE}\varphi_b^{3/2} \right)$ of which barrier height can be estimated. The ln (J/E^2) versus 1/E plot for Ni/SiO_2/*p*-Si/Al diode in the temperature range of 70–300 K is shown in Fig. 7 (a). As can be seen that the linear behaviour of curves at each temperature starts appearing above −0.5 V which means that FNT tunneling in Ni/SiO_2/*p*-Si/Al diode is effective above 0.5 V. Thus, the linear region observed in the bias range between −0.5 and −2.0 V was best fitted to estimate the temperature dependence of the barrier height using the slope of Eq. (6). It was observed that the BH increases from 0.16 eV to 0.28 eV as temperature changes from 300 to 70 K as shown in Fig. 7 (b). The increase in barrier height with decrease in temperature from 300 to 70 K can be understood in terms of decrease in

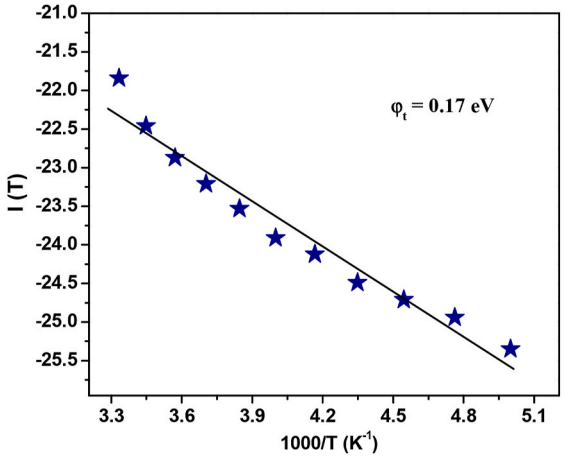

Fig. 6. Variation of I (T) as function of inverse temperature.

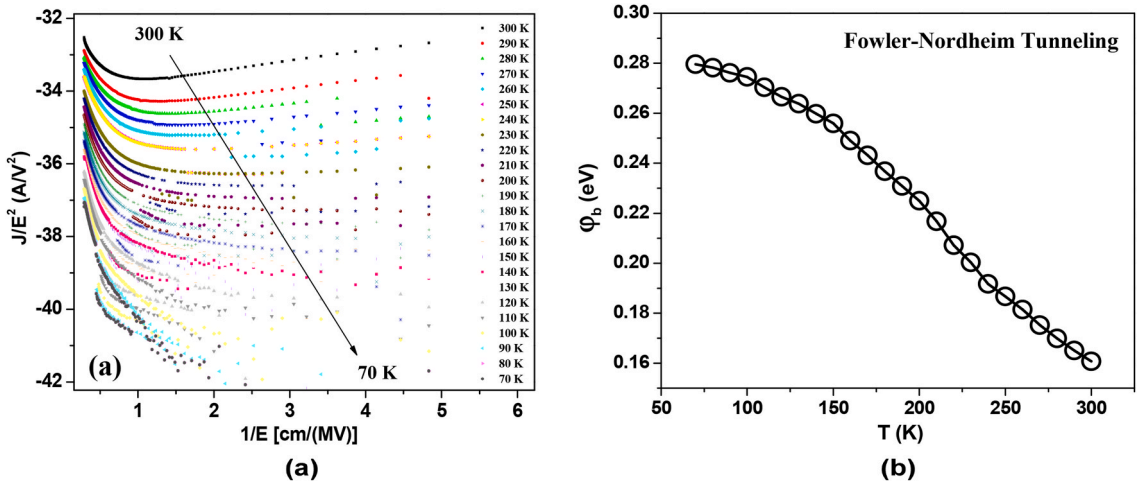

Fig. 7. (a) Temperature dependent Fowler–Nordheim plot, (b) barrier height variation with temperature obtained using FNT model.

reverse current with temperature. Further, such a low values of barrier height obtained using FNT mechanism may be due to the fact that the in the bias range between −0.5 and – 2 V the conduction mechanism is not only governed by FNT but there can be an involvement of other mechanisms such as SE.

4. Conclusion

We analyzed the non–saturation behaviour of reverse current–voltage characteristics over a wide temperature range of 300–70 K with $\Delta T = 10$ K for Ni/SiO_2/*p*-Si/Al diode. The results of the study revealed that none of the employed well–known CCMs i.e., Poole–Frenkel emission and Schottky emission exactly follow the actual conduction mechanism occur in the diode over the measured bias and temperature range. However, from the analysis of emission coefficient we note that the SE has dominance over other mechanisms in the temperature range of 200–300 K and bias range of −0.5 – 0 V. In this temperature range the trap activation energy was estimated to be 0.17 eV. Further, from the FNT model analysis we noticed that Fowler–Nordheim tunneling is effective above the −0.5 V up to −2.0 V along with SE mechanism which may be the possible cause of low values of barrier height obtained using FNT mechanism. These observed low values of barrier height can be attributed to trap state activation energy.

Credit statement

Naveen Kumar: Experimental work, Methodology, Writing. Subhash Chand: Supervision, Conceptualization, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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