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Analysis of device parameters of Al/In_2O_3/*p*-Si Schottky diode

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ABSTRACT

Thin film of indium oxide (In_2O_3) is deposited on *p*-silicon substrate using sol–gel spin technique. The sol–gel spin deposited film is very smooth with grain size and root mean square surface roughness of ~40 nm and ~7.9 nm, respectively. The device parameters of Al/In_2O_3/*p*-Si Schottky diode were investigated using direct current current–voltage (*I–V*) and impedance spectroscopy. The ideality factor and barrier height of the diode were determined to be 1.07 ± 0.03 and 0.72 ± 0.02 eV, respectively. At higher voltages, the charge transport mechanism of the diode is controlled by a trap-charge limited conduction mechanism (TCLC). The series resistance profile of the diode was extracted to show the presence of the interface states changing with frequency.

1. Introduction

Transparent conducting oxides have attracted considerable interest because of their wide applications in electronics and optoelectronics [1,2]. Among the transparent conducting oxides, indium oxide (In_2O_3) is extensively used for flat panel display, light emitting diodes and photovoltaic cells [3,4]. The wide range of applicability of In_2O_3 is due to its low electrical resistivity and high transparency in the visible range of solar spectrum [5]. Different techniques such as DC magnetron sputtering [6], radio-frequency sputtering [7], electron beam evaporation [8], high density plasma evaporation [9], thermal reactive evaporation [10], spray pyrolysis [11], sol–gel [12], chemical vapor deposition [13], and pulsed laser deposition [14] have been used for deposition of thin films. Among them, sol–gel offers many important advantages in materials processing. The nanostructure of the gels permits low temperature processing, low cost and easy technology [15]. The product can be influenced by careful control of several reaction variations. Another advantage of the sol–gel method is the wide range of accessible shapes such as nano particles, fibers, thin films etc. [16].

Savarimuthu et al. have synthesized the In_2O_3 films using sol–gel spin coating technique [17]. Cheng et al. have prepared In_2O_3 nanorods with length of ~120 nm and diameter of ~20 nm by sol–gel technique [18]. The influence of annealing temperature on the properties of In_2O_3 films obtained by sol–gel method is reported [19]. Schottky barrier diode using indium tin oxide (ITO) as Schottky electrode is reported [20,21]. It is observed that annealing the ITO/*n*-GaN Schottky junction at 500 °C in nitrogen ambient increases the barrier height. In_2O_3 is an extensively used semiconductor for device fabrication. The most common substrate for these device fabrications is silicon. It would be very interesting to study the junction properties of In_2O_3 and silicon. The literature survey indicates that there is no report on the Schottky junctions of Al/In_2O_3/*p*-Si using sol–gel spin coating technique.

In present paper, we report detail electrical characterizations of the Al/In_2O_3/*p*-Si Schottky device fabricated using sol–gel spin coating technique. The device parameters are calculated using different methods.

2. Experimental details

Thin film of In_2O_3 was synthesized using indium chloride, 2-methoxyethanol and monoethanolamine as precursors. In typical synthesis, 0.3 M of indium chloride was dissolved in 2-methoxyethanol followed by addition of monoethanolamine in the resulting solution. The molar ratio of monoethanolamine to indium chloride was taken as 1.0. Finally, the solution was stirred at 60 °C for 2 h at room temperature. The Schottky barrier diode of In_2O_3 was fabricated on *p*-Si wafer by sol–gel spin coating followed by drying at 150 °C for 10 min and finally at 500 °C for 1 h. The thickness of the Si wafer was 600 μm with resistivity of 5–10 Ω cm. Before fabrication of the Schottky diodes the silicon substrate was cleaned. In order to remove the native oxide layer on surface of silicon, the wafer was etched by HF and then rinsed in deionised water using an ultrasonic bath for 10–15 min. Finally silicon wafer was chemically cleaned according to method based

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on successive baths of methanol and acetone. The ohmic contact was deposited by evaporating Al metal on the back of Si wafers followed by annealing at 570 °C for 3 min in N_2 atmosphere. The top Ag contacts were deposited by evaporating Ag metal onto In_2O_3 film. The contact area of the diodes was calculated to be 3.14×10^{-2} cm^2. Surface morphology of the films was investigated using a PARK system XE 100E atomic force microscopy (AFM). The electrical characterizations of the device were performed using semiconductor characterization system (Keithley 4200).

3. Results and discussion

The AFM image of the In_2O_3 deposited onto a *p*-Si substrate by sol–gel spin coating method is shown in Fig. 1. As seen in Fig. 1, the In_2O_3 film is formed from nanoparticles. The grain size of the film was determined to be ~40 nm using Park system XEI software. This suggests that the In_2O_3 film is a nanomaterial. The film is very smooth with the root mean square (rms) surface roughness of 7.9 ± 0.3 nm. The current–voltage (*I–V*) characteristics of the device are studied in ± 2.0 V. Fig. 2 shows the *I–V* characteristics of the fabricated junction. It is clear from the figure that the device shows rectifying behavior. It is evaluated that at lower voltages, the diode behaves like Schottky diode and thus, *I–V* characteristics of the diode could be described by thermionic emission model. According to this model, the current in such device could be expressed as [22]

$$I = I_O \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{nkT}\right)\right] \quad (1)$$

where I_O is the saturation current, k is the Boltzmann constant, T is the absolute temperature, q is the elementary electric charge, V is the applied voltage and n is the ideality factor. The saturation current I_O is expressed as

$$I_O = AA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \quad (2)$$

where A is the active device area, A^* is the effective Richardson constant (equal to 32 A/cm^2K^2 for *p*-type silicon) and ϕ_b is the barrier height [23]. The ideality factor is determined from the slope of the linear region of forward bias ln *I–V* plot. The barrier height of the device is calculated using the Eq. (2); on the other hand, the ideality factor is calculated using the expression

$$n = \left(\frac{q}{kT}\right) \cdot \left(\frac{dV}{d(\ln I)}\right) \quad (3)$$

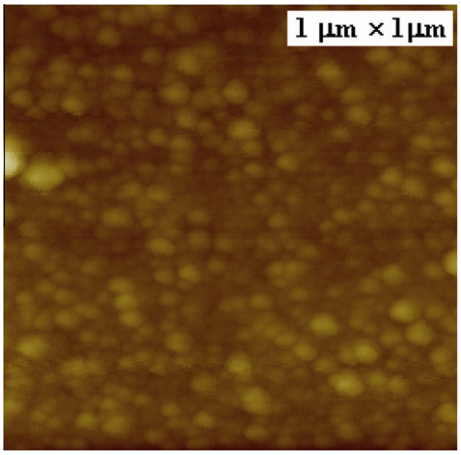

Fig. 1. AFM image of In_2O_3 film on *p*-Si substrate.

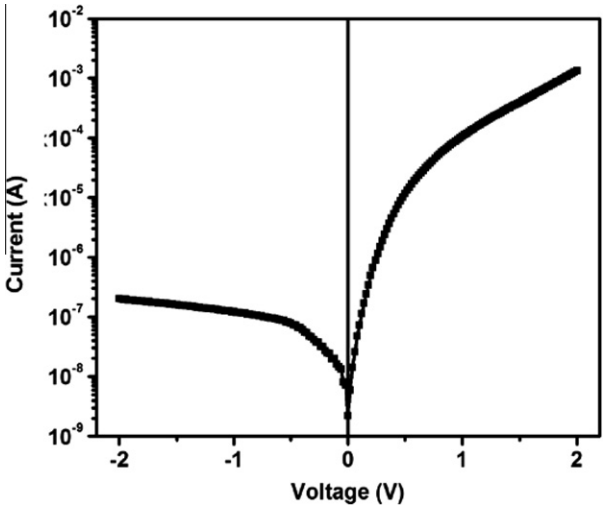

Fig. 2. Semi-log *I–V* characteristics of the Ag/In_2O_3/*p*-Si/Al Schottky diode.

The ideality factor was found to be 1.07 ± 0.3, which is very close to the ideal value of 1.02 [24]. The higher value of the ideality factor may be due to the presence of interface states, oxide layer on silicon and series resistance [25].

In order to better understand the charge transport mechanism that controls the device characteristics, we present double-log *I–V* characteristics of the fabricated junction in Fig. 3. It is clear from the figure that the forward bias log*I*–log*V* characteristics show two distinct linear regions separated by transition segment. The first region is ohmic with slope of 1.2. The ohmic behavior of the device at low voltage is due to existing background doping (oxygen vacancies) or thermally generated carriers [26]. The slope of the second region was found to be 3.3, indicating that a trap-charge-limited conduction (TCLC) mechanism is controlled by the presence of traps within the bandgap of the indium oxide film. It is evaluated that the diode indicates a non-linear behavior due to the series resistance and interface states. Thus, we cannot ignore the series resistance effect on the *I–V* characteristics of the diode and the device parameters of the Schottky junction could be also determined using Cheung–Cheung method [27]. According to Cheung–Cheung method, the forward bias *I–V* characteristics due to the thermionic emission having the series resistance can be expressed as

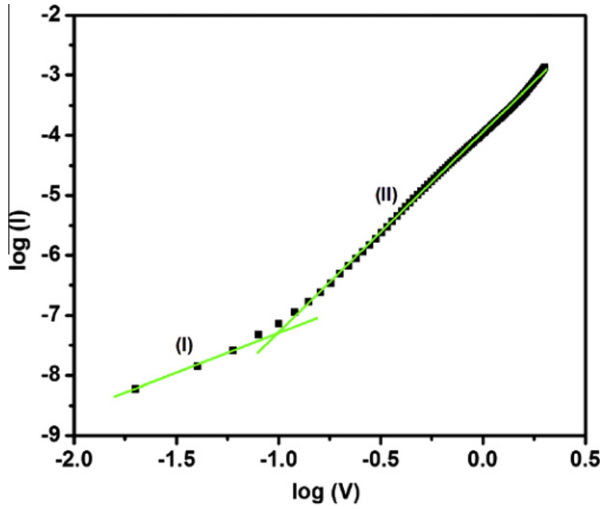

Fig. 3. Double log *I–V* plot of the Ag/In_2O_3/*p*-Si/Al Schottky diode.

$$I = I_O \exp\left[\frac{q(V - IR_S)}{nkT}\right] \quad (4)$$

where IR_S is the voltage drop across the series resistance. According to this method, the series resistance, ideality factor, and barrier height can be calculated from the following equations

$$\frac{dV}{d(\ln I)} = n\left(\frac{kT}{q}\right) + IR_S \quad (5)$$

and $$H(I) = IR_S - n\phi_b \quad (6)$$

where, $$H(I) = V - n\left(\frac{kt}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (7)$$

The series resistance and ideality factor of the device can be calculated from the slope and y-axis intercept of the $dV/d(\ln I)$ *vs. I* plot (Fig. 4). The value of ideality factor and series resistance is calculated to be 1.7 ± 0.1 and 3.5 (±0.3) × 10^4 Ω, respectively. It is observed that there is a difference between the ideality factor obtained from the forward bias semi-log *I–V* plot and $dV/d(\ln I)$ *vs. I* plot. This difference could be due to the presence of series resistance, interface states, and the voltage drop across the interfacial layer [28]. Series resistance and barrier height can be also calculated using Eq. (6). A plot of $H(I)$ *vs. I* will be linear and slope of this plot gives series resistance and intercept gives the barrier height (Fig. 4). From the $H(I)$ *vs. I* plot, the barrier height and series resistance of the device is calculated to be 0.72 ± 0.2 eV and 1.1 (± 0.2) × 10^5 Ω, respectively.

Capacitance–voltage (*C–V*) study is one of the most popular electrical measurement techniques used to characterize a Schottky device. Fig. 5 shows the forward and reverse bias *C–V* characteristics of the Ag/In_2O_3/*p*-Si/Al Schottky diode at different frequencies. It is observed that the capacitance increases with decrease in frequency. The increase of the capacitance at low frequencies depends on the ability of the electron concentrations to follow the applied alternating current (*AC*) signal. If the *C–V* measurement carries out at sufficiently high frequencies, the charge at the interface cannot follow an *AC* signal [29]. It is observed that the *C–V* characteristics have an anomalous peak at higher frequencies. And the peak position shifts towards negative high voltage. This may be because the capacitance of the thin films is very sensitive to the interface properties [25]. This occurs because of the interface states that respond differently to low and high frequencies. Similar results have been observed by other researches also [8,30,31]. It is reported that

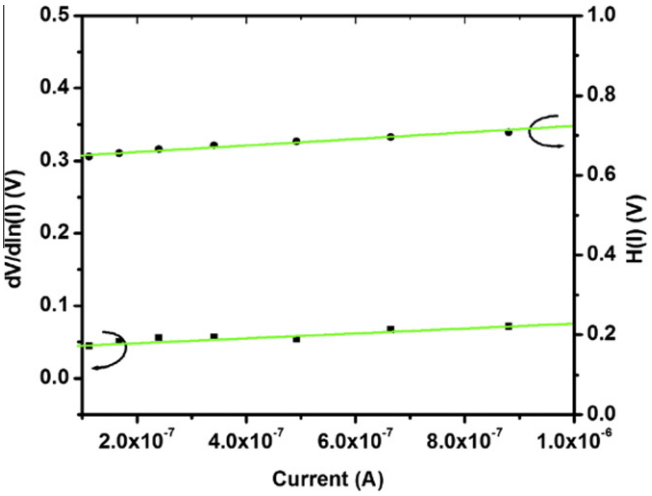

Fig. 4. $dV/d(\ln I)$ *vs. I* and $H(I)$ *vs. I* plots of the Ag/In_2O_3/*p*-Si/Al Schottky diode.

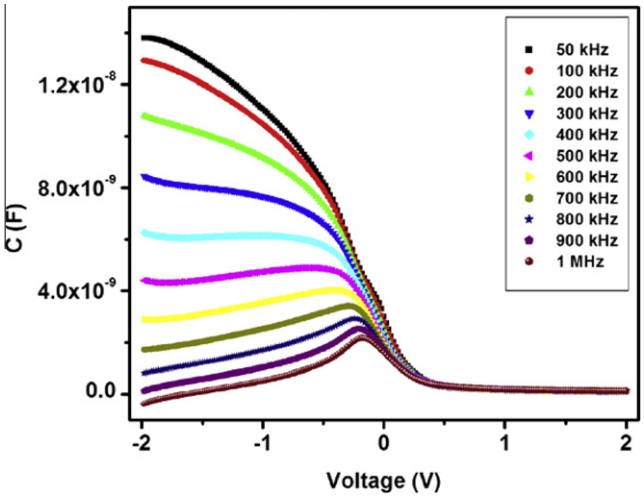

Fig. 5. *C–V* plots of the Ag/In_2O_3/*p*-Si/Al Schottky diode.

the peak value of the capacitance varies with the series resistance and interface state density [32].

The variations of conductance with voltage at different frequencies are shown in Fig. 6. It can be seen that the conductance of the film is independent of the frequency in the forward bias voltage; on the other hand the conductance is highly dependence on the frequency in the reverse bias voltage. The conductance of the Schottky diode increases with increase in the frequency in the reverse bias voltage. Similar observation is reported for the Schottky diode based on ZnO/*n*-Si [15]. In order to investigate the effect of series resistance on the capacitance and conductance, the corrected capacitance (C_{ADJ}) and corrected conductance (G_{ADJ}) were calculated using the expressions [33,34].

$$C_{ADJ} = \frac{[G_m^2 + (\omega C_m)^2]C_m}{a^2 + (\omega C_m)^2} \quad (8)$$

$$G_{ADJ} = \frac{[G_m^2 + (\omega C_m)^2]a}{a^2 + (\omega C_m)^2} \quad (9)$$

where $$a = G_m - G_m^2 + (\omega C_m)^2 R_S \quad (10)$$

where C_{ADJ} and G_{ADJ} are series resistance compensated capacitance and conductance respectively. C_{ADJ}–*V* and G_{ADJ}–*V* plots as a function

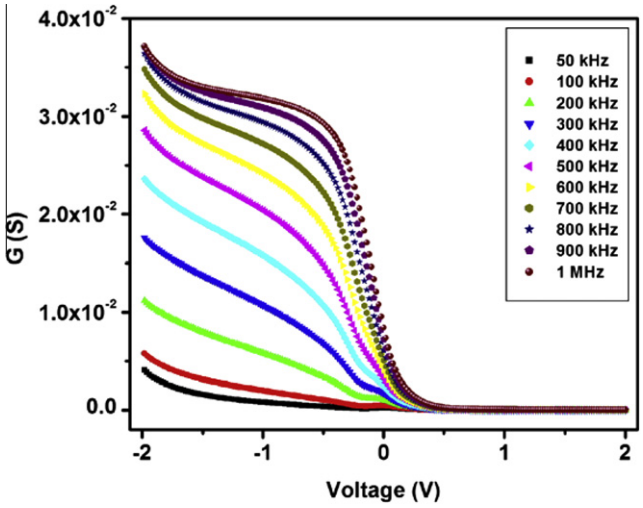

Fig. 6. *G–V* plots of the Ag/In_2O_3/*p*-Si/Al Schottky diode.

of frequencies are shown in Figs. 7 and 8, respectively. We observe a peak in C_{ADJ}–V and G_{ADJ}–V plots which may be due to the presence of interface [15]. It is seen that the peak position moves towards lower negative voltage with increase in frequency. The peak intensity of C_{ADJ} plots found to decrease with increase in frequency, which is due to the dielectric dispersion of the device. On the other hand, it is observed in G_{ADJ}–V plots that the peak intensity increases with increase in frequency, which indicates that the interface states can follow the AC signal. The observation of the peak in the C_{ADJ}–V and G_{ADJ}–V plots is explained with the interface states and series resistance. The density of interface states can be obtained by means of Fig. 8. As seen in Fig. 8, the plot shows a peak, which confirms the presence of interface states. The D_{it} value can be calculated by the following relation [35],

$$D_{it} = \left(\frac{2}{qA}\right)\left[\frac{(G_{\max}/\omega)}{\left[(G_{\max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2\right]}\right] \quad (11)$$

where C_m is the measured capacitance, $(G_{\max}/\omega)$ is the measured conductance, C_{ox} is the capacitance of the insulating layer, A is the area of the diode and ω is the angular frequency.

The D_{it} value obtained from G_{ADJ} *vs.* V plot under 1 MHz is 7.03×10^{12} eV^{-1} cm^{-2}. The obtained D_{it} is considerably high and it affects the I–V characteristics of the diode. The series resistance of the device is calculated using the equation

$$R_S = \frac{(G_m/\omega C_m)^2}{1 + (G_m/\omega C_m)^2} G_m \quad (12)$$

The variations of R_S with applied bias voltage at different frequencies are shown in Fig. 9. As seen in the Fig. 9, the R_S–V plots have a peak and the peak position shifts towards lower positive bias voltage with increase in frequency. It is also noted that the peaks intensity decreases with increasing frequency. This behavior indicates that the interface states changes with frequency. The high value of series resistance at low frequencies is because the interface states can follow the AC signal and yield an excess capacitance at low frequency. Whereas at higher frequencies, the low series resistance is explained as the interface states cannot follow the AC signal and do not make a contribution to interface states [36].

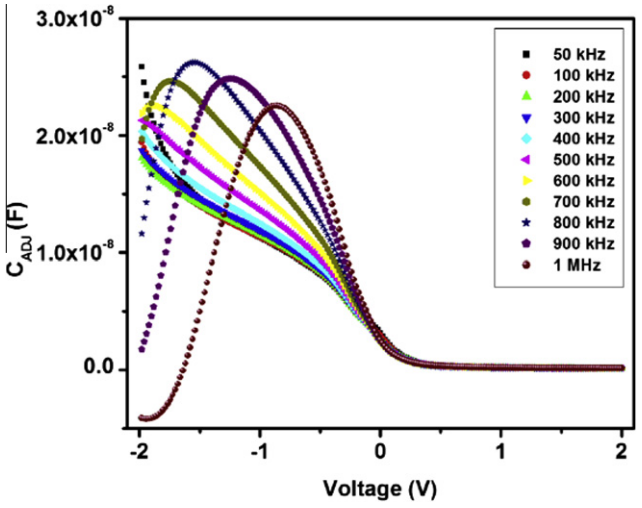

Fig. 7. Corrected C–V plots of the Ag/In_2O_3/p-Si/Al Schottky diode.

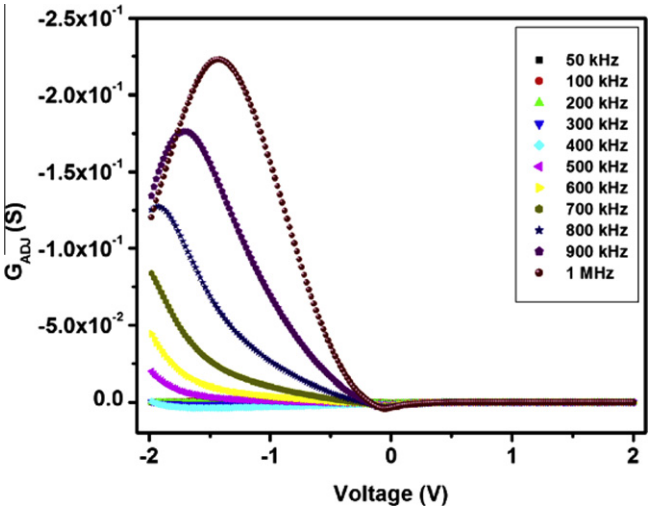

Fig. 8. Corrected G–V plots of the Ag/In_2O_3/p-Si/Al Schottky diode.

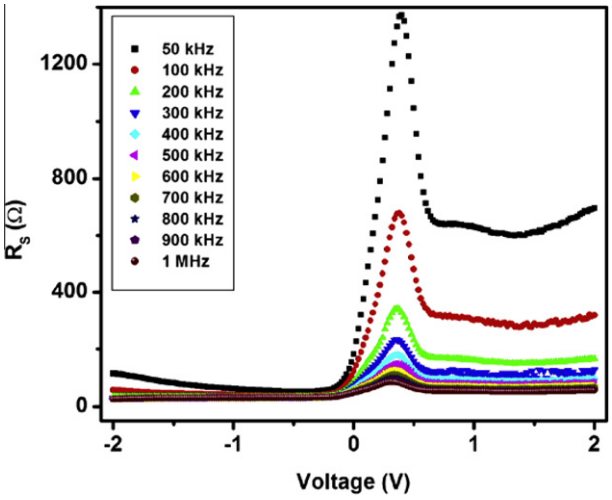

Fig. 9. R_S–V plots of the Ag/In_2O_3/p-Si/Al Schottky diode.

4. Conclusions

We have fabricated an Ag/In_2O_3/p-Si/Al Schottky diode using sol–gel spin coating method. The device parameters such as ideality factor, barrier height, and series resistance were calculated. The deviation from the ideal behavior is explained on the basis of series resistance. The forward bias semi-log I–V characteristics show ohmic behavior at low bias voltage and follows TCLC mechanism at higher bias voltage. The C–V measurements indicate that the capacitance is independent of the voltage and frequency at higher positive voltage. The high value of capacitance at low frequency in reverse bias region is attributed to the excess capacitance resulting from the interface states that could follow the AC signal.

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