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The interface state energy distribution from capacitance–frequency characteristics of gold/n-type Gallium arsenide Schottky barrier diodes exposed to air

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Abstract

A study on gold/n-type Gallium arsenide (Au/n-GaAs) Schottky barrier diode (SBD) parameters with and without thin native oxide layer fabricated on n-type GaAs was made. The native oxide layer for metal/oxide/semiconductor (MIS) SBD was obtained by exposing the chemically cleaned GaAs surface to clean room air for 30 days, before metal evaporation. The values of 1.089 and 0.730 eV for the ideality factor and barrier height of the reference Au/n-GaAs SBD were obtained, respectively, and the values of 1.427 and 0.671 eV for the MIS and SBD, respectively. We calculated the density distribution and time constant of the interface states from the capacitance–frequency measurements using the Schottky capacitance spectroscopy method. The interface state density N_{ss} of the diodes has an exponential rise with bias from the midgap towards the top of the conduction band; for example, from 1.20×10^{10} cm^{-2} eV^{-1} in $(E_c-0.730)$ eV to 3.41×10^{12} cm^{-2} eV^{-1} in $(E_c-0.470)$ eV for reference diode, and from 1.47×10^{10} cm^{-2} eV^{-1} in $(E_c-0.671)$ eV to 1.68×10^{13} cm^{-2} eV^{-1} in $(E_c-0.411)$ eV for the MIS diode.

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Keywords: Gallium arsenide; Interfaces; Metal/oxide/semiconductor structure; Metallization; Schottky barrier

1. Introduction

There are currently a vast number of experimental study reports on characteristic parameters such as barrier height and ideality factor in a great variety of metal–semiconductor (MS) contacts [1–16]. The popularity of such studies, rooted in their importance to the semiconductor industry, does not assure uniformity of the results or of the interpretation. The semiconductor crystal surfaces are usually covered with layers of native oxides and organic contaminants in the laboratory environment. In many cases, the barrier heights obtained on cleaved and chemically prepared semiconductor surfaces indicate the presence of an interfacial layer [6–16]. The layer-by-layer growth of the native oxide layer that is inevitably present on chemically prepared semiconductor surfaces thus occurs even when it is exposed to clean room air [6–13]. Furthermore, the interfacial native oxide layer thickness between metal and semiconductor is dependent on exposure time of the semiconductor surface to residual gases in the case of chemically cleaned substrates [6–13]. Turner and Rhoderick [10] observed no difference in Schottky barrier heights (SBH) on cleaved and etched surfaces for gold and nickel but a significant decrease on the etched surfaces for copper, silver and aluminum, and they also studied the effect of ageing in Au/n-Si diodes. Vanalme et al. [11] determined the distribution of SBH over the contact area in Au/III–V semiconductor diodes using ballistic electron emission microscopy. Their samples with chemical pretreatment in aqueous HF or HCl solutions showed changes in the barrier height distribution.

As mentioned above, the understanding of the detailed mechanisms of the oxidation, reduction and etching processes involved in wafer cleaning is essential for

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high device yield. Moreover, after the device fabrication, its performance and stability depending on time are important matters in the device manufacturing. Therefore, the purpose of this paper is to characterize the density distribution and relaxation time of the interface states from the capacitance–frequency–voltage (C–f–V) characteristics of the reference and metal–insulating–semiconductor (MIS) gold/n-type Gallium arsenide (Au/n-GaAs) Schottky barrier diodes (SBDs) prepared by exposing to clean room air for 30 days.

2. Experimental procedure

The samples (SBDs) were prepared using cleaned and polished n-GaAs (as received from the manufacturer) with (1 0 0) orientation and $2–5\times10^{17}$ cm^{-3} carrier concentrations. Before making contacts, the n-GaAs wafer was dipped in $5H_2SO_4+H_2O_2+H_2O$ solution for 1.0 min to remove any surface damaged layer and undesirable impurities and then in H_2O+HCl solution. Following a rinse in de-ionized water of 18 MΩ, the wafer was dried with high-purity nitrogen and inserted into the deposition chamber immediately after the etching process. For ohmic contacts, Au–Ge (88%, 12%) was evaporated on the back of the wafer in a vacuum-coating unit of 10^{-5} Torr. After that, low resistance ohmic contacts were formed by thermal annealing at 450 °C for 3 min in flowing N_2 in a quartz tube furnace. The native oxide layer for metal/oxide/semiconductor (MIS) diode was obtained by exposing the chemically cleaned GaAs surface to clean room air for 30 days, before Schottky contact formation. The Schottky contacts were made by evaporation of Au as dots with a diameter of approximately 1.35 mm onto all of the n-GaAs surfaces. The current–voltage (I–V) and C–V and impedance characteristics were measured using a HP 4140B picoampermeter and a HP model 4192A LF impedance analyzer, respectively, at the room temperature and in the dark.

3. Results and discussion

When the SBDs with a thin interfacial layer (MIS) are considered, it is assumed that the forward bias current of the device is due to thermionic emission current and it can be expressed as [2]

$$I=I_0\exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right], \quad (1)$$

where

$$I_0=AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right), \quad (2)$$

is the saturation current density, Φ_b is the barrier height

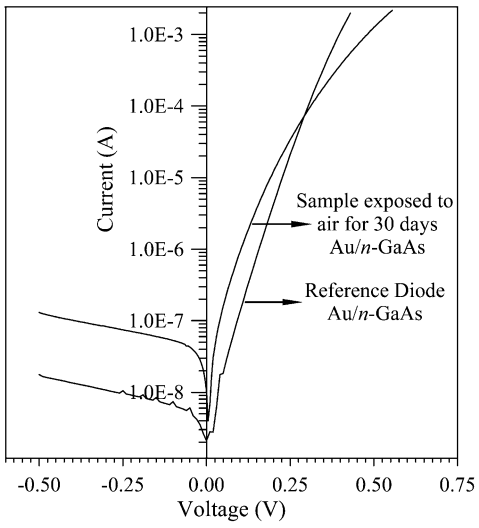

Fig. 1. The forward and reverse bias current vs. voltage characteristics of the reference and MIS (metal/oxide/semiconductor—the sample exposed to clean room air for 30 days) Au/n-GaAs Schottky diodes, at room temperature. The values of 1.089 and 0.730 eV, and 1.427 and 0.671 eV for the ideality factor and barrier height of the reference and MIS diodes, respectively, these values were calculated from the y-axis intercept and slope of the linear region of the semilog-forward bias plot.

at zero bias, A^* is the effective Richardson constant and equals to 8.16 $A/cm^2\,K^2$ for n-type GaAs; A is the diode area; n is an ideality factor that is a measure of conformity of the diode to pure thermionic emission and is calculated from the slope of the straight line region of the forward bias ln I–V characteristics through the relation

$$n=\frac{q}{kT}\frac{dV}{d(\ln I)}. \quad (3)$$

If n is equal to one, pure thermionic emission occurs. However, n has usually a value greater than unity.

The curves in Fig. 1 show the experimental semilog-forward and reverse bias I–V characteristics of the reference and MIS samples Au/n-GaAs SBDs. The MIS SBD was obtained by exposing the chemically cleaned GaAs surface to clean room air for 30 days, before formation of Schottky contact. The barrier height value of Au/n-GaAs SBDs was calculated with the help of Eq. (2) from the y-axis intercepts of the semilog-forward bias I–V plots, and the value of the ideality factor n was obtained using Eq. (3) from the linear region of these plots. The values of 1.089 and 0.730 eV for the ideality factor and barrier height of the reference sample were obtained, respectively, and the values of 1.427 and 0.671 eV for the MIS diode, respectively. The value of 1.427 of n for MIS Schottky contact indicates the presence of an insulator layer on the n-GaAs surface [6–13]. For a sufficiently thick interface layer, the

interface states are in equilibrium with the semiconductor (the n-GaAs substrate) and they cannot interact with the metal [2–4,7–9,15,16]. For MS contacts it is known that the contact characteristics are controlled by Fermi level pinning due to the interface states. That is, it can be concluded that the barrier height determined from the I–V characteristics is controlled by the interface states in equilibrium with the semiconductor.

If measurements are carried out at sufficiently high frequencies, ω, (such that lifetime, τ, is much larger than ω^{-1}) the charge at the interface states cannot follow an a.c. signal. This will occur when the time constant is too long to permit the charge to move in and out of the states in response to an applied signal [2,8,15,16]. Thus, in an ideal Schottky diode, the depletion layer capacitance can be expressed as [2,8]

$$C^{-2}=2(V_{\mathrm{do}}+V)/q\varepsilon_s A^2 N_{\mathrm{d}} \tag{4}$$

and

$$\frac{\mathrm{d}(C^{-2})}{\mathrm{d}V}=\frac{2}{q\varepsilon_s A^2 N_{\mathrm{d}}} \tag{5}$$

where A is the area of the diode, V_{do} is the diffusion potential at zero bias and is determined from the extrapolation of the linear C^{-2}–V plot to the V axis.

Furthermore, the capacitance for a MIS Schottky diode with the interfacial layer is represented by [8]

$$\frac{1}{C^2}=\frac{2(\Phi_{\mathrm{b}}-C_2V-V_{\mathrm{n}})}{qC_2^2\varepsilon_s A^2 N_{\mathrm{d}}} \tag{6}$$

Furthermore, as can be seen from this expression, the C^{-2} vs. V plot is a straight line whose intercept with V axis gives the value of V_0 and the slope gives the value of C_2. The C_2 is a parameter inverse of the ideality factor n. V_{n} is the potential difference between the Fermi level and the bottom of the conduction band in the neutral region of n-GaAs and can be calculated knowing the carrier concentration of the ideal diode N_{d}. Thus, C_2, respectively, can be given as follows:

$$C_2=\frac{1}{n}=\frac{2}{q\varepsilon_s A^2 N_{\mathrm{d}}\left[\mathrm{d}(C^{-2})/\mathrm{d}V\right]}. \tag{7}$$

Since we know values of the Fermi energy and C_2, the barrier height for a Schottky diode with the interfacial layer can be calculated from [8]

$$\Phi_{\mathrm{b}}=C_2V-V_{\mathrm{n}}, \tag{8}$$

where Fig. 2 shows the reverse bias C^{-2}–V (1.0 MHz) characteristics of the ideal (the reference diode) and

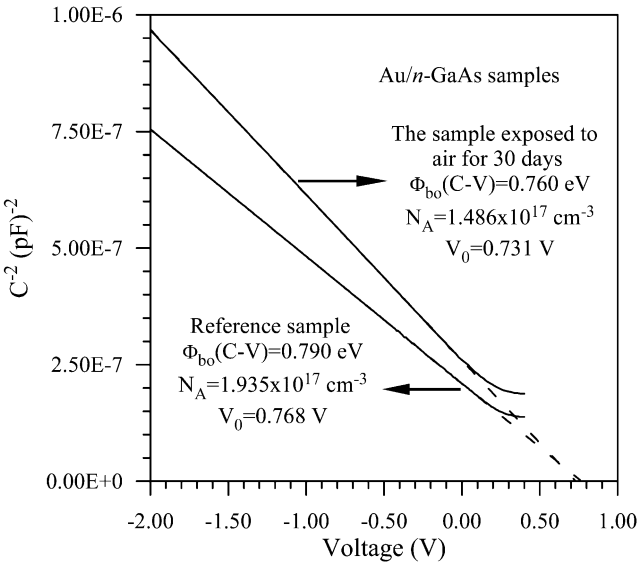

Fig. 2. The reverse bias C^{-2}–V curves of the reference and metal/oxide/semiconductor (MIS—the sample exposed to clean room air for 30 days) Au/n-GaAs Schottky diodes, at 1.0 MHz and room temperature.

MIS Au/n-GaAs Schottky diodes made by us. Using Eq. (7), the values of $1/C_2=n=1.30$ and $N_{\mathrm{d}}=1.486\times10^{17}$ cm^{-3} for the reference Schottky contact were obtained from its experimental reverse bias C^{-2}–V. The value of $N_{\mathrm{d}}=1.935\times10^{17}$ cm^{-3} of the reference diode (Fig. 2) was used in Eq. (7) for calculating C_2 value of the MIS diode. An intercept voltage value (V_0) of 0.731 V for the MIS Schottky diode was determined, and thus a barrier height value of 0.760 eV from Eq. (8), where $V_{\mathrm{n}}=0.029$ V was determined approximately using the experimental doping concentration above. An intercept voltage value (V_0) of 0.768 V for the reference Schottky diode was determined, and thus a barrier height value of 0.790 eV, where $V_{\mathrm{n}}=0.022$ V.

As can be seen, the C–V curves gave Φ_{b} values higher than those derived from I–V measurements as expected. Although this discrepancy could be explained by the existence of an interfacial layer or trap states in the semiconductor, the existence of the barrier inhomogeneity offers another explanation [2,8,16–18]. The capacitance C is insensitive to potential fluctuations on a length scale of less than the space-charge width and the C–V method averages over the whole area and measures to describe SBD. The d.c. current I across the interface depends exponentially on Φ_{b}. Any spatial variation in the barriers causes the current I to flow preferentially through the barrier minima. Consequently, for an inhomogeneous interface, the spatial variations of band bending V_{n} and barrier height Φ_{b} result in different SBH for the current and capacitance [4,17,18].

Now, let us calculate the density distribution of the interface states from the capacitance–frequency meas-

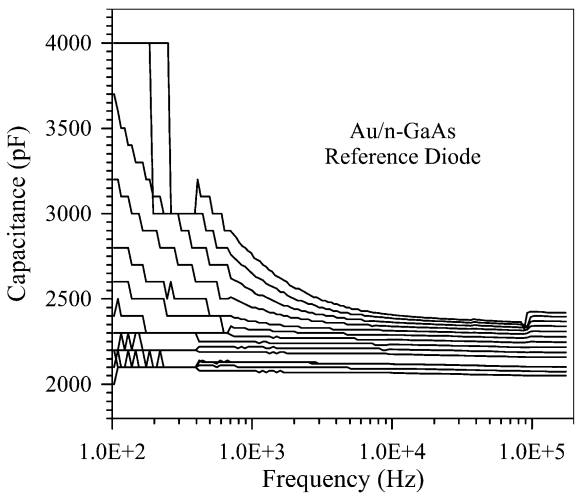

Fig. 3. The experimental forward bias capacitance plot as a function of the frequency with bias voltage as a parameter of the reference Au/n-GaAs Schottky diode, at room temperature (0.00–0.24 V with steps of 0.02 V).

urements of the diodes using the Schottky capacitance spectroscopy (SCS) method. The capacitance measurement is one of the most important methods for obtaining information on the interface of the Schottky contacts. The SCS is a measurement technique that can provide the required accuracy in determining the variation of the interface state capacitance as a function of the forward bias at low frequency [15–29]. In general, the interface states in equilibrium with the semiconductor do not contribute to the capacitance at sufficiently high frequencies because the charge at the interface states cannot follow the a.c. signal. In this case, the SBD has the space-charge capacitance only. At low frequencies, the contribution of the interface states to diode capacitance decreases toward high frequencies. Experimental capacitance corresponding to low frequency in the data obtained from the $C–f$ measurements approximately equals to the sum of the space-charge capacitance (C_{sc}) and the interface capacitance (C_{ss}) [17,19–29]. Thus, the capacitance of the devices depending on frequency is given as follows [15,19–28]:

$$C = C_{sc} + C_{ss} \quad \text{(at low frequency)} \tag{9}$$

$$C \cong C_{sc} \quad \text{(at high frequency)} \tag{10}$$

According to Nicollian and Goetzberger [19], the interface state capacitance can be described as:

$$C_{ss} = AqN_{ss}\frac{\arctan(\omega\tau)}{\omega\tau} \tag{11}$$

where τ is time constant and can be written as

$$\tau = \frac{1}{v_{th}\sigma N_d}\exp\left(\frac{qV_d}{kT}\right) \tag{12}$$

where σ is the cross-section of interface states, v_{th} the thermal velocity of carrier and N_d the doping concentration. The interface state density for small values of $\omega\tau$ equals to [15,19–29]

$$N_{ss} = \frac{C_{ss}}{qA} \tag{13}$$

where A is the diode area. The interface state capacitance C_{ss} is determined from the vertical axis intercept of $C_{ss}–f$ plots.

In n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given by [15,20]

$$E_c - E_{ss} = q\Phi_b - qV. \tag{14}$$

Figs. 3 and 4 show the measured capacitance–frequency ($C–f$) for the reference and MIS diodes with steps of 0.02 V, respectively. As have been seen from the figures, the higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states that can follow the a.c. signal. As the frequency was increased further, the diode capacitance first decreased and then became almost constant. A near constant value of the capacitance resulting in the intermediate frequency region means the case where a much small part of the interface states can only follow the signal.

At a given forward bias, the value of the space-charge capacitance in high frequency region of the experimen-

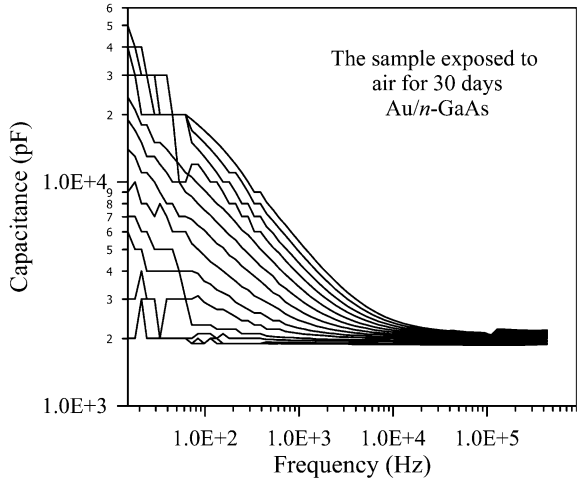

Fig. 4. The experimental forward bias capacitance plot as a function of the frequency with bias voltage as a parameter of the MIS Au/n-GaAs Schottky diode, at room temperature (0.00–0.24 V with steps of 0.02 V).

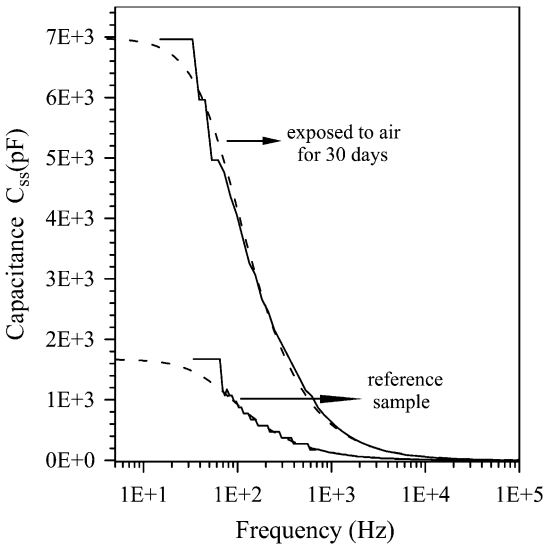

Fig. 5. The forward bias interface state capacitance plot as a function of the frequency at bias voltages of 0.14 and 0.20 V for the reference and MIS Au/n-GaAs Schottky diodes, respectively, at room temperature. The dashed lines represent best fits of Eq. (14) to the experimental values C_{ss}–f to obtain the relaxation time of the interface state density τ.

tally obtained forward bias C–f plots are subtracted from the experimental junction capacitance C, thus the interface states capacitance C_{ss} is obtained, then C_{ss}–f plots for the diodes (Fig. 5). In the plateau region, Eq. (13) is applicable and the value of the interface state density N_{ss} for each applied bias voltage can be deduced directly from the ordinate of the plateau. Then, we fitted Eq. (11) to the experimental values C_{ss}–f to obtain relaxation time of the interface state density τ (the dashed lines in Fig. 5) [20–29]. Based on our results, there is a good agreement between experimental and theory. To obtain the dependence of N_{ss} and τ on the bias, the fitting procedure was repeated for various values of the bias voltage as in Fig. 5. The dependence of N_{ss} and τ on the bias was converted to a function of E_{ss} using Eq. (14) and these plots are shown in Figs. 6 and 7, respectively.

As can be seen from Fig. 6, the interface state density N_{ss} has an exponential rise with bias from the midgap towards the top of the conduction band for each diodes; for example, from 1.20×10^{10} $cm^{-2}\,eV^{-1}$ in $(E_c-0.730)$ eV to 3.41×10^{12} $cm^{-2}\,eV^{-1}$ in $(E_c-0.470)$ eV for the reference diode, and from 1.47×10^{10} $cm^{-2}\,eV^{-1}$ in $(E_c-0.671)$ eV to 1.68×10^{13} $cm^{-2}\,eV^{-1}$ in $(E_c-0.411)$ eV for MIS diode. The values obtained for N_{ss} are of the same order as those reported by some authors for metal/Schottky diodes [15,16,21–28,30–35]. Furthermore, as can be seen from Fig. 7, the relaxation time of the interface state density for the reference has an exponential rise with bias from the midgap towards the top of the conduction band, that

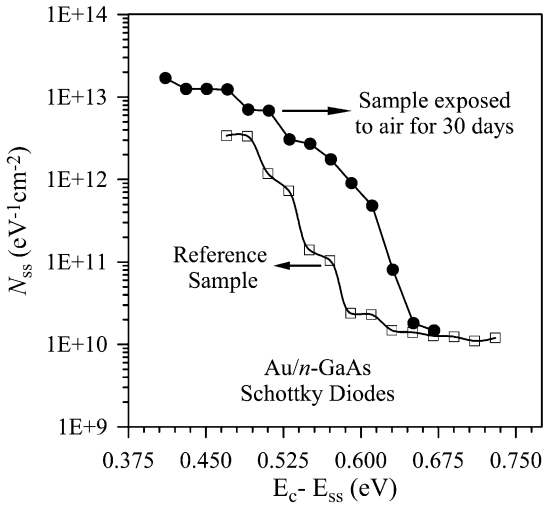

Fig. 6. The energy distribution curves of the interface states obtained from the low C_{ss}–f characteristics for the reference and MIS Au/n-GaAs Schottky diodes.

is, it ranges from 2.80×10^{-5} s in $(E_c-0.730)$ eV to 6.35×10^{-3} s in $(E_c-0.470)$ eV for reference diode. For the MIS diode, the relaxation time has an exponential rise with bias from 3.50×10^{-5} s in $(E_c-0.671)$ eV to 4.51×10^{-3} s in $(E_c-0.570)$ eV, and it remains about unchanged in the range 3.52×10^{-3}–4.23×10^{-3} s from $(E_c-0.570)$ eV to $(E_c-0.411)$ eV, that is, we can state that the relaxation time about saturates from $(E_c-0.570)$ eV to $(E_c-0.411)$ eV for the MIS diode.

4. Conclusion

In conclusion, the ideality factor values of 1.089 and 1.427 for the reference and MIS diodes were obtained

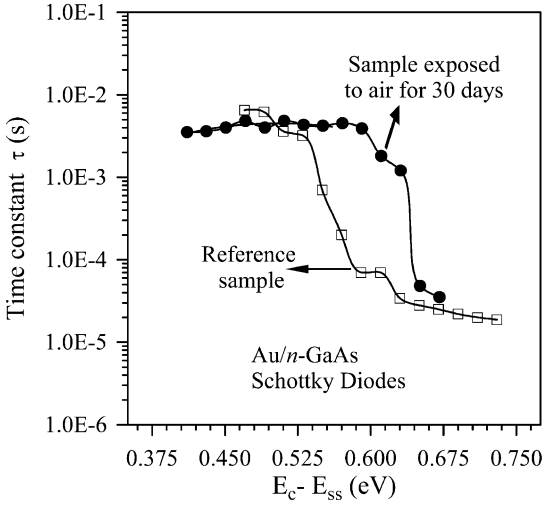

Fig. 7. The energy distribution curves of time constant of the interface states obtained from the low C_{ss}–f characteristics for the reference and MIS Au/n-GaAs Schottky diodes.

from the forward bias I–V characteristics. The value of 1.427 of n for MIS Schottky contact was attributed to the presence of a native oxide layer on the n-GaAs surface. Furthermore, the energy distribution curves of the interface states and their relaxation time were determined from the experimental low C–f characteristics. The interface state density for each two diodes has an exponential rise with bias from the midgap towards the bottom of the conduction band. Moreover, the relaxation time for the MIS showed an exponential rise with bias from $(E_c-0.671)$ eV to $(E_c-0.570)$ eV while it remains about unchanged from $(E_c-0.570)$ eV to $(E_c-0.411)$ eV. But, the relaxation time for the reference has an exponential rise with bias from the midgap towards the top of the conduction band.

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