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Large barrier, highly uniform and reproducible Ni-Si/4H-SiC forward Schottky diode characteristics: testing the limits of Tung's model

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Abstract

We report highly ideal ($n < 1.1$), uniform nickel silicide (Ni–Si)/SiC Schottky barrier (1.60–1.67 eV with a standard deviation <2.8%) diodes, fabricated on 4H-SiC epitaxial layers grown by chemical vapour deposition. The barrier height was constant over a wide epilayer doping range of 10^{14}–10^{16} cm^{-3}, apart from a slight decrease consistent with image force lowering. This remarkable uniformity was achieved by careful optimization of the annealing of the Schottky interface to minimize non-idealities that could lead to inhomogeneity. Tung's barrier inhomogeneity model was used to quantify the level of inhomogeneity in the optimized annealed diodes. The estimated 'bulk' barrier height (1.75 eV) was consistent with the Shockley–Mott limit for the Ni–Si/4H-SiC interface, implying an unpinned Fermi level. But the model was not useful to explain the poor ideality in unoptimized, as-deposited Schottky contacts ($n = 1.6 - 2.5$). We show analytically and numerically that only idealities $n < 1.21$ can be explained using Tung's model, irrespective of material system, indicating that the barrier height inhomogeneity is not the only cause of poor ideality in Schottky diodes. For explaining this highly non-ideal behaviour, other factors (e.g. interface traps, morphological defects, extrinsic impurities, etc) need to be considered.

Keywords: silicon carbide, Ni/SiC Schottky, Schottky barrier inhomogeneity, Schottky barrier diode, Tung's model

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon carbide Schottky barrier diode (SBD) is considered an attractive alternative to Si p–i–n junction diode for high-power, high-frequency applications such as photovoltaic (PV) inverters, power factor correction and motor control circuits [1]. To extend the application space of SiC SBDs to higher power systems, such as solid-state transformers, it is necessary to develop reproducible, high barrier, thermally stable rectifying contacts.

Nickel is an attractive Schottky contact to 4H-SiC due to the large Schottky barrier it forms. The large barrier height offers very low reverse leakage, which is important for applications such as high-frequency power switching [2] and solid-state sensors used in emission monitoring and nuclear radiation detection [3]. As-deposited Ni was reported to form rectifying contact with 4H-SiC with barrier heights in the range of 1.3–1.6 eV [4–8], while the diode characteristics were found to be highly sensitive to the surface preparation prior to contact deposition [8–10]. Several groups reported formation of double barriers [9] and strong deviation from ideal thermionic emission behaviour [10–13] in the as-deposited contacts. Annealing the Schottky interface in the temperature range of 600–800 °C was reported to flatten out double barriers

and improve the ideality factor of the diodes. These annealed diodes also showed larger barrier heights than those for the as-deposited contacts [9–13]. However, the statistical distribution of barrier heights over the entire substrate was not reported in most of these studies, and those reported showed significant 'inter-sample' variation [10].

The improvement in ideality with annealing is often attributed to the formation of nickel silicide at the Ni/SiC interface [11, 12]. As shown by Roccaforte *et al* [10], the Schottky characteristics obtained for the as-deposited contacts (Ni/SiC) were strongly dependent on the surface treatment prior to device fabrication, while the annealed (nickel silicide/SiC) contact characteristics were process-independent. This result infers that the surface defects and/or impurities introduced during the fabrication process may lead to the non-ideal behaviour of the as-deposited contact. When the contact is annealed, Ni diffuses into the epilayer and reacts with the Si atoms, moving the metal/semiconductor interface beneath the epilayer surface, reducing the influence of surface impurities. Although this qualitative picture is widely accepted, a quantitative understanding of the non-ideal behaviour is important for gaining insight into the nature of the change the Schottky interface undergoes upon annealing.

Non-ideal Schottky behaviour is often described in terms of Schottky barrier inhomogeneity in the diode active area [14]. The total diode current is considered an aggregate of the current flowing through different regions in the interface with different barrier heights. The non-ideality in the diode characteristics arises from the low barrier regions turning on at a lower bias than the high barrier region. However, Tung *et al* [15, 16] and Gutler *et al* [14] pointed out that the small barrier regions can be in the form of patches with dimensions comparable to or less than the depletion width. In that case, these regions can be 'pinched off' by the surrounding high barrier regions at low bias, rendering a bias-dependent barrier height. This additional bias dependence manifests as an additional voltage drop across the diode, leading to poorer ideality.

The Tung model, however, does not make any assumption on the nature or origin of inhomogeneity at the Schottky interface. Rather, it defines an inhomogeneity parameter γ that encapsulates every form of non-ideality at the interface, e.g. surface roughness, grain boundaries, interface phases (i.e. silicides), etc [15]. The conduction through each of the patches of the various barrier heights is, however, assumed to follow ideal thermionic emission behaviour. Tung argues that almost all types of non-idealities in the I–V characteristics of 'real' Schottky diodes, including poor ideality and temperature effects, can be modelled by his analytical theory. However, Im *et al* experimentally showed that Tung's model works well only for diodes with near-ideal characteristics ($n \sim 1.06$), while it fails to model the I–V characteristics that widely deviate from the ideal thermionic emission behaviour (double barrier, $n \sim 1.5$) [17]. Other groups have also attempted to fit the I–V characteristics and/or quantify the level of barrier inhomogeneity at various metal/SiC Schottky interfaces using Tung's model [11, 12, 18–20]. However, the bias-dependent local barrier height parameters in Tung's model are often misunderstood for the overall diode barrier height, leading to an incorrect estimation of the γ parameter. We discuss these issues in this paper and determine the limit of applicability of Tung's model.

In this paper, we report the fabrication of high barrier ($\Phi_b > 1.6$ eV), near-ideal ($n < 1.1$) Ni silicide/4H-SiC Schottky diodes by post-deposition annealing of Ni/4H-SiC contact. We show that the annealed Schottky diodes on the same epilayer demonstrate near-ideal characteristics and a tight distribution of barrier heights ($\sigma = 8 - 46$ meV) over a wide epilayer doping level of 10^{14}–10^{16} cm^{-3}. The effect of epilayer doping on the estimated barrier heights is discussed in terms of various doping dependent Schottky parameters. Tung's model is applied to estimate the extent of barrier inhomogeneity within individual diodes and the range of applicability for the model is determined. We conclude that Tung's model produces physically meaningful parameters only for near-ideal diodes, but fails to model I–V characteristics with ideality factors, $n > 1.21$.

1.1. Experimental details

The 4H-SiC epilayers used for the fabrication of the diodes were grown by chemical vapour deposition (CVD) in a hot-wall CVD reactor. Instead of the conventional silane precursor, tetrafluorosilane (SiF_4, TFS), a halogenated silicon precursor gas was used for the epitaxial growth. The use of TFS produces smooth, low defect density epitaxial layers as discussed in detail elsewhere [21]. The epigrowth was performed on 2 cm × 2 cm pieces cut out of commercial 4° offcut Si-face 4H-SiC wafers. The surfaces of the grown epilayers were observed by Nomarski optical imaging and atomic force microscopy (AFM). The typical thicknesses of the epilayers used were 20–30 μm. The epilayer doping levels were determined from C–V data obtained from a mercury probe setup. All of the epilayers were n-doped with doping concentrations in the range of 10^{14}–10^{16} cm^{-3}. Doping was achieved by varying the C/Si ratio in the precursor flow during epigrowth.

Prior to fabrication of Schottky diodes, the backsides of the wafers were lapped by diamond paste to remove residual deposition. Before diode fabrication, the episurfaces were dry-oxidized at 1100 °C for 4 h. Upon removal of the thermal oxide by dilute (1 : 10) HF solution, the epilayer surface was cleaned by standard RCA cleaning procedure, followed by another round of dilute HF etch. The ohmic contact on the backside was formed by the deposition of 120 nm Ni by e-beam evaporation at $\sim 2 \times 10^{-6}$ Torr, followed by rapid thermal annealing at 1000 °C in Ar flow. Schottky 'dot' areas with diameters of 100, 150 and 250 μm were defined by standard photolithography and 100 nm thick Schottky contacts were formed by e-beam evaporation of Ni. Prior to the metal deposition, the wafer was dipped in buffered HF solution to remove any thermal oxide present on the surface. A post-deposition rapid thermal annealing was carried out at 450 and 650 °C in Ar environment to study the effect of annealing on the Schottky barrier properties. No edge termination was used to limit electric field crowding during reverse bias operation. Figure 1 shows the schematic structure of the fabricated 'unterminated' Schottky diodes. The lack of the

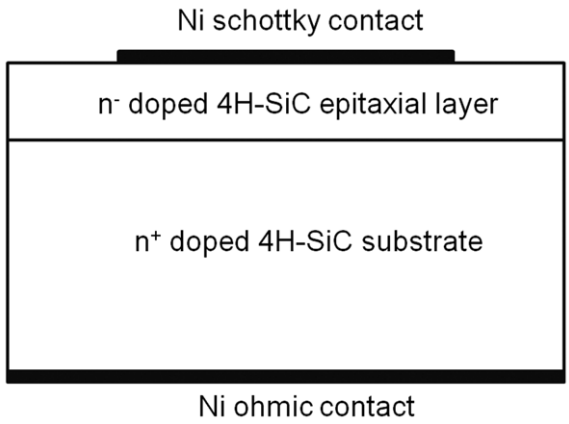

Figure 1. The Schottky diode structure fabricated on epitaxial SiC. The Schottky contact was formed by depositing Ni on the episurface. The ohmic contact was formed by deposition of Ni on the backside, followed by rapid thermal annealing. No edge termination was done.

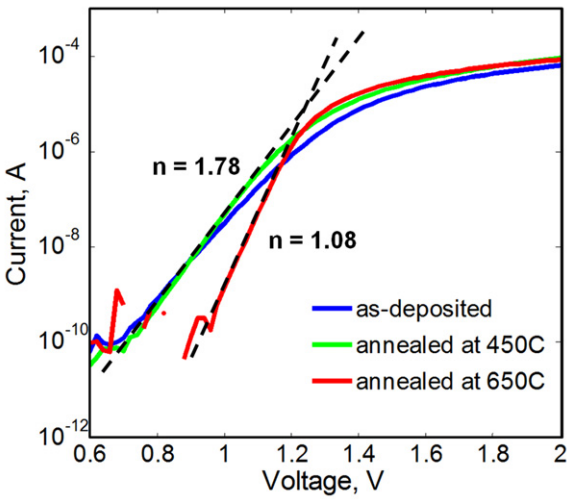

Figure 2. Effect of post-deposition annealing on forward I–V characteristics of a Schottky diode. The diode was fabricated on a 20 μm thick epilayer with n-doping density of 1×10^{15} cm^{-3}. The I–V slopes are shown for D450 (450 °C annealed) and D650 (650 °C annealed).

edge termination resulted in high, area-dependent reverse leakage current (perimeter leakage) and lower than expected, unpredictable breakdown voltages. Nevertheless, breakdown voltages exceeding 1200 V (measurement capability) were occasionally observed.

2. Results and discussion

2.1. Diode characterization: as-deposited and annealed

To study the effect of annealing on the diode I–V characteristics Ni Schottky contacts were formed by Ni deposition on a 20 μm thick epitaxial layer with doping density of 10^{15} cm^{-3}. The as-deposited contacts were subject to 60 s rapid thermal annealing at 450 and 650 °C consecutively. Figure 2 shows the effect of annealing on the forward I–V characteristics of a Schottky 'dot' of 150 μm diameter. From this point, the as-deposited characteristics will be referred to as D0, and the characteristics obtained after annealing at 450 °C and 650 °C will be referred to as D450 and D650, respectively. However, it should be noted that all three characteristics were obtained from the same contact after annealing at different temperatures. As can be seen in the figure, annealing at 450 °C had no significant impact on the I–V characteristics, whereas a 650 °C anneal dramatically improved the slope of the I–V curve. The ideality factor n and barrier height Φ_b obtained by fitting the linear part of the forward I–V characteristics are shown in table 1. The 450 °C anneal improved the ideality factor only slightly (from 2.14 for as-deposited to 1.78 after the 450 °C anneal), whereas the 650 °C anneal resulted a dramatic improvement in the diode characteristics and rendered near-ideal ($n = 1.08$), high barrier ($\Phi_b = 1.65$ eV) Schottky contact. The extracted Φ_b value is close to the Schottky–Mott limit (~1.76 eV), which can be estimated from the difference between the work function of Ni (~5 eV) and the electron affinity of 4H-SiC (~3.24 eV [22]), as shown in the band diagram in figure 3. This result implies that the annealed contact interface is possibly free from Fermi level pinning by the interface-related electronic states. It is to be noted that, for the Ni-rich Ni–Si phases, the work function values quoted in literature are typically >4.8 eV [23, 24]. The values are very close to the Ni work function ~5.0 eV, which allows us to use the same band diagram to approximately describe the ideal barrier height for the annealed contacts too.

Table 1. Effect of annealing: ideality factor and barrier height values obtained from linear fit of forward I–V curves.

Annealing temperature (°C)	Ideality factor (n)	Apparent barrier height Φ_b (eV)
As-deposited (D0)	2.14	1.12
450 (D450)	1.78	1.20
650 (D650)	1.08	1.65

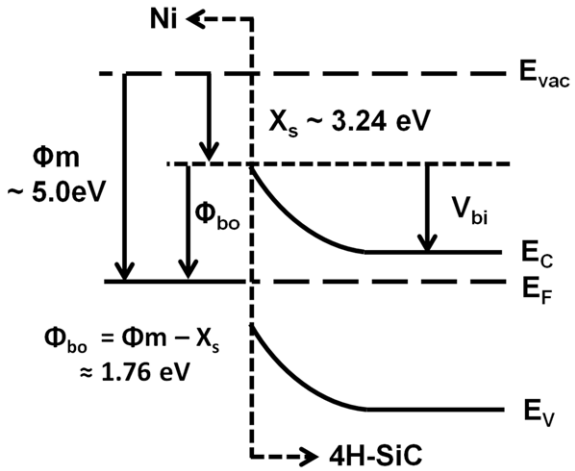

Figure 3. The zero-bias energy band diagram for the Ni/SiC Schottky interface. The electron affinity value reported in [22] was used for calculating the ideal barrier height value.

The annealing results (650 °C) were reproduced on epitaxial layers of a wide doping range (10^{14}–10^{16} cm^{-3}). Figure 4 shows a boxplot of the barrier heights obtained from

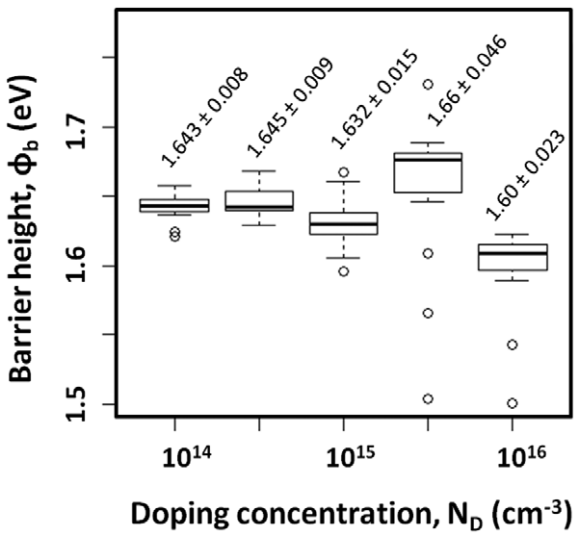

Figure 4. A boxplot of the Schottky barrier height versus epilayer doping concentration generated by *R* (v2.15.3), a statistical programming environment. Each box represents 1st, 2nd and 3rd quartiles (Q_1, Q_2/median and Q_3) of the barrier heights obtained from 30 diodes at the corresponding doping level. The whiskers denote the maximum values within 1.5× interquartile range (Q_3–Q_1). Outliers are shown as circles. The mean and standard deviation values are shown next to each box as $\mu \pm \sigma$.

Table 2. Spatial variation of Schottky barrier height, Φ_b, and ideality factor, n, at various doping levels.

Growth precursor	Doping N_D (cm^{-3})	Barrier height, $\Phi_b + \sigma_\Phi$ (eV)	Ideality factor, $n \pm \sigma_n$
TFS	1×10^{14}	1.643 ± 0.008	1.07 ± 0.007
	5×10^{14}	1.645 ± 0.009	1.095 ± 0.011
	1×10^{15}	1.632 ± 0.015	1.069 ± 0.006
DCS	1×10^{15}	1.667 ± 0.036	1.056 ± 0.034
	5×10^{15}	1.66 ± 0.046	1.059 ± 0.033
	1×10^{16}	1.60 ± 0.023	1.077 ± 0.037

the Schottky diodes fabricated on epilayers of different doping levels. Each box represents the distribution of barrier height values extracted from the J–V characteristics of 30 diodes of the same doping level. The mean (μ_Φ) and standard deviation (σ_Φ) values are also shown next to each box (listed in table 2). The spatial variation (σ_Φ) of the barrier heights fell within the range of 8–46 mV (0.1–3% of the mean value), indicating a very 'uniform' barrier height distribution across the substrate. These data, to the best of the authors' knowledge, show the tightest distribution of Schottky parameters ever reported for Ni/SiC Schottky system. It is to be noted that the low doped epilayers (10^{14}–10^{15} cm^{-3}) were produced by a CVD process that used the novel, tetrafluorosilane (TFS) gas, while the higher doped layers were grown by dichlorosilane (DCS), a more conventional Si precursor gas [25, 26]. The low barrier outliers on the high doped Schottky data in figure 4 are possibly a consequence of the poorer doping uniformity and/or higher morphological defect density rendered by the DCS-based CVD growth process [27].

At any given doping level, the spatial variation in both of the parameters are given in terms of the corresponding standard deviation, calculated over 21–42 Schottky 'dots' distributed across the entire substrate. The typical I–V characteristics obtained from the as-deposited Ni/4H-SiC contacts on an n-doped epilayer are shown in figure 5(*a*). The figure shows I–V curves obtained from 21 Schottky 'dots' of three different sizes deposited on a 20 μm epitaxial layer with an n-doping density of 5×10^{14} cm^{-3}. All of these contacts showed highly non-ideal behaviour with ideality factor $n > 2$, while few showed double barrier characteristics. However, apart from the double barrier diodes, the as-deposited contacts showed a tight distribution of diode parameters—ideality factor, $n = 2.01 \pm 0.04$ and barrier height, $\Phi_b = 1.22 \pm 0.09$ eV. Annealing the contacts at 650 °C for 120 s improved the ideality factor (n) to 1.095 ± 0.01 and the barrier height (Φ_b) was increased to 1.645 ± 0.09 eV. Figure 5(*b*) shows the I–V characteristics obtained from the same diodes after annealing. The double barriers flattened out (became a single barrier) and the ideality and barrier heights improved significantly. An important thing to note here is that, although the characteristics improved after annealing, the standard deviations of the diode parameters (n and Φ_b) were similar for both the as-deposited and annealed diodes. It can be inferred from the narrow distribution of the Φ_b values in the as-deposited contacts that the non-ideality in these diodes should be attributed to interface anomaly that is evenly distributed across the substrate (e.g. interface layer/traps, etc), and not to microscopic defects or surface impurities, which are likely to show a large scatter in their distribution. The double barrier characteristics, on the other hand, are more sporadic, and can be attributed to surface defects or impurities.

2.2. Applying Tung's model

We applied Tung's model of inhomogeneous Schottky barrier to the measured I–V characteristics. According to this model, the non-ideal behaviour of the as-deposited contact arises from the spatial inhomogeneity of Schottky barrier height across the metal–semiconductor interface. The Schottky interface is described as a uniform 'high barrier' region with patches of lower barrier height embedded in it. The regions with different barrier heights turn on at different bias voltages, leading to a deviation from ideal ($n \sim 1$) thermionic emission behaviour. The total diode current is an aggregate of the current flow through the different, non-interacting regions with different barrier heights. Tung [15, 16] and Werner *et al* [14] pointed out that the length-scale associated with barrier inhomogeneity can be comparable to the Schottky depletion width. In that case, low barrier regions surrounded by higher barrier regions can undergo current pinch-off at low bias voltages (figure 6). A thorough numerical detail of the model can be found in [15]. The effective barrier height of these pinched-off patches becomes a function of the applied voltage, which leads to a high ideality factor. Im *et al* [17] performed ballistic electron emission microscopy (BEEM) to determine the barrier height variation across the Pd/6H-SiC interface at the nm scale and found excellent agreement with Tung's model for diodes with good ideality factors ($n < 1.1$). However, for diodes with significant degrees of non-ideality, application of Tung's model obtained unphysical fitting parameters, which indicated that

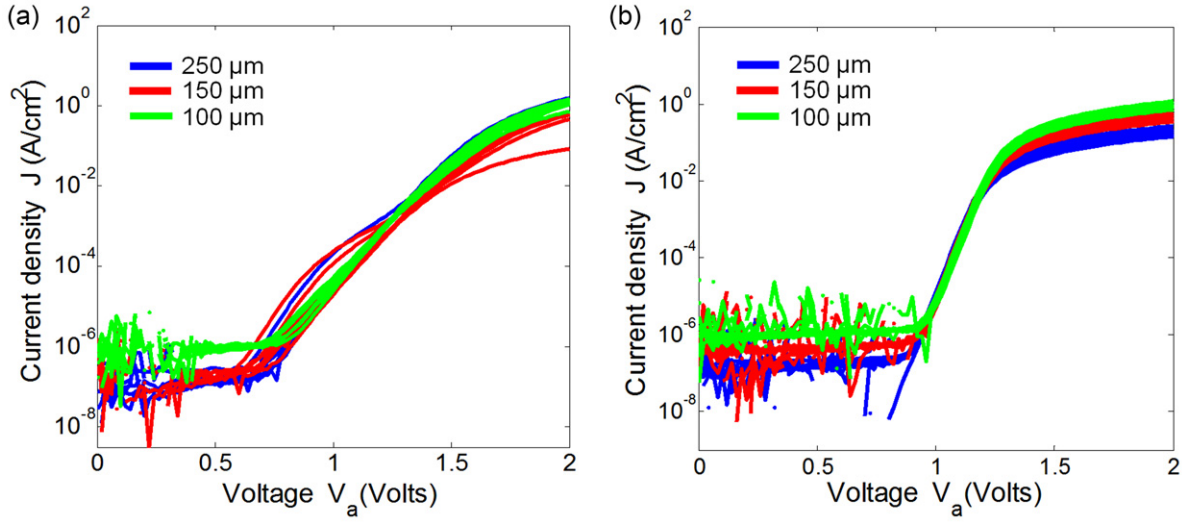

Figure 5. Forward J–V characteristics for (a) the as-deposited Schottky diodes (seven contacts of each size are shown, diameters shown in the legend) and (b) Schottky diodes annealed at 650 °C for 120 s (14 contacts of each size shown).

the possible source of inhomogeneity in those diodes was possibly extrinsic in nature, e.g. crystallographic defects and/or impurities introduced during surface preparation. We will revisit this point in the section below on the limits of Tung's model.

Tung's model describes the inhomogeneous barrier height distribution over the diode area in terms of a bias and temperature independent, inhomogeneity parameter, γ, which is intrinsic to the Schottky interface. In the microscopic level, γ is defined as

$$\gamma = 3\left(\frac{\Delta R_o^2}{4}\right)^{1/3}. \tag{1}$$

Equation (1) assumes low barrier patches embedded in an otherwise high barrier $\left(\Phi_b^o\right)$ Schottky interface. The shape of the patch is circular with a radius of R_o and the barrier height of the patch is given as $\left(\Phi_b^o - \Delta\right)$. As can be inferred from the equation, a high γ value indicates a 'deeper' (in terms of energy) and/or larger low barrier patch, leading to a higher degree of inhomogeneity.

The current through a single low barrier patch is given as

$$I_{patch}(\gamma) = A^* A_{patch} \exp(-\beta\Phi_{eff}) \exp(\beta V_a - 1). \tag{2a}$$

Here, A_{patch} is the effective area of current conduction for the patches and is given by $A_{patch} = 4\pi\gamma\eta^{2/3}/9\beta V_{bb}^{2/3}$ and the effective barrier height of the patch is expressed as

$$\Phi_{eff} = \Phi_b^o - \frac{\gamma V_{bb}^{1/3}}{\eta^{1/3}}. \tag{2b}$$

Assuming a sharp distribution of γ (i.e. a single value of γ for all patches, rather than a distribution), for a patch density of c_1, the aggregate of the current flowing through individual patches is given by

$$\Sigma I_{patch} = c_1 A I_{patch}. \tag{2c}$$

In the equations above, A is the total diode area, V_{bb} is the band bending under bias V_a, η is a constant equal to $2\varepsilon_s/qN_d$.

It is to be noted that the effective barrier height for the low barrier patches, Φ_{eff} given by (2*b*) is often inappropriately attributed to the diode as a whole and/or assumed equal to experimentally determined Φ_b values, whereas in reality, this parameter applies exclusively to the low barrier regions in the interface, and is a function of applied bias. The bias-dependent barrier lowering term in (2*b*), $\gamma V_{bb}^{1/3}/\eta^{1/3}$, will be referred to as δ in the subsequent analysis.

Assuming c_1 to be the low barrier patch concentration (with respect to total area A), the current through the 'high barrier' bulk region of the diode area (I_{bulk})is given by the thermionic emission equation

$$I_{bulk} = A(1 - c_1 A_{patch}) A^* T^2 \exp(-\beta\Phi_b^o) \exp(\beta V_a - 1). \tag{3}$$

The total current through the diode is estimated as an aggregate of the low barrier patch current $\left(I_{patch}\right)$ and the current through the uniform 'bulk' region (I_{bulk}) with barrier height Φ_b^o,

$$I_{tot} = \Sigma I_{patch} + I_{bulk}. \tag{4a}$$

The full expression is given by

$$I_{tot} = AA^* T^2 \exp(-\beta\Phi_b^o) \exp(\beta V_a - 1) \times \left[1 + \frac{4c_1\pi\eta^{2/3}\gamma}{9\beta V_{bb}^{2/3}} \exp\left(\frac{\beta\gamma V_{bb}^{1/3}}{\eta^{1/3}}\right)\right]. \tag{4b}$$

Figure 7 shows the theoretical fits to the experimental I–V curves D450 and D650 previously shown in figure 2, using (4*b*). The fitting parameters are given in table 3. For the D650 characteristics, a bulk barrier height of 1.75 eV and a homogeneity parameter $\gamma = 7 \times 10^{-4}\,\mathrm{cm}^{1/3}\,\mathrm{V}^{2/3}$ provided the best fit. It can be noticed from the figure that the current through the low barrier patches dominate the conduction at low bias (up to about $V_a = 1$ V), whereas the bulk current gradually catches up and dominates the conduction at high bias. Because of this general trend, in the literature, while modelling the I–V characteristics of near-ideal diodes, the bulk current term (I_{bulk}) is often ignored. Rather, the low barrier patches are assumed to carry the major portion of the total diode current

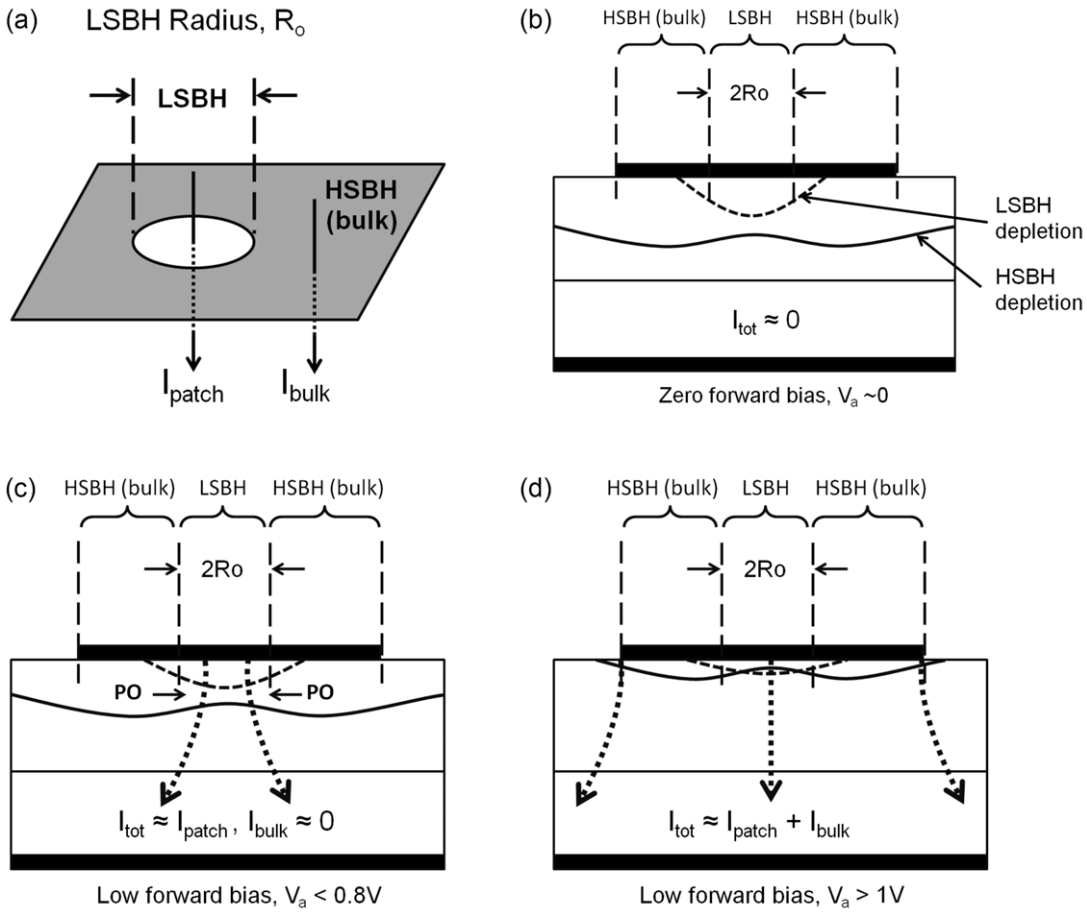

Figure 6. A qualitative illustration of Tung's model: non-ideal diode behaviour caused by the Schottky barrier inhomogeneity. (*a*) The inhomogeneity is perceived as a low barrier 'patch' (LSBH) surrounded by the high barrier bulk of the interface. (*b*) A cross sectional view of the interface showing the depletion regions corresponding to the low and high barrier regions. (*c*) At low bias, the LSBH patch starts conducting, while the bulk of the interface remains depleted. As the depletion width is comparable to the patch dimension, the field under the HSBH bulk laterally pinches off (PO) the current through the LSBH patch, the amount of pinch-off being a function of applied voltage. (*d*) At sufficiently high bias, the bulk turns on and both the LSBH and HSBH regions start conducting, and the pinch-off effect disappears.

$I_{total} \approx \sum I_{patch}$, and the patch barrier height is used as the overall barrier height ($\Phi_{eff} \approx \Phi_b$) for calculating the ideality factor and/or the inhomogeneity parameter, γ. However, as shown, in figure 7(*b*), a complete fit of the I–V characteristics (accounting for both I_{patch} and I_{bulk}) reveals that I_{bulk} cannot be ignored in these calculations, especially at high bias levels. Another interesting thing to note is that the bulk barrier height Φ_b^o extracted from the fit is close to the theoretical Schottky–Mott limit of 1.76 eV (figure 3), further providing evidence of the absence of Fermi level pinning.

The D0 (as-deposited) and D450 (450 °C annealed) I–V curves were also fitted using (4*b*). In these fits, however, the patch current was the dominant component of the total diode current up to bias levels as high as ~1.2 V. Only the fit to D450 is shown in figure 7(*a*) as the representative non-ideal characteristics. However, the fitting parameters obtained for both D0 and D450 are listed in table 3. It was assumed that the bulk barrier heights $\left(\Phi_b^o\right)$ were comparable at all stages of annealing, so we can still use $\Phi_b^o \approx 1.75$ eV. However, the best fits to D0 and D450 using $\Phi_b^o \approx 1.75$ eV were obtained using c_1 values that were unphysically small (table 3), as the minimum possible value of c_1 is 2.01×10^3 cm^{-2} (one patch per diode area). On the other hand, if we fix the c_1 value at its minimum, the closest (but not the best) fits required unphysically large Φ_b^o values (~2.8 eV). These results indicate that the Tung's model is not adequate for modelling the highly non-ideal characteristics D0 and D450. For these diodes, Tung's model overestimates the current through the individual patches, which leads to unphysically small (less than one per diode) patch density. The overestimation of patch current density follows from the very high level of barrier inhomogeneity required to fit the experimental data. As will be discussed in the subsequent section, this high level of inhomogeneity goes beyond the scope of Tung's model which works with small perturbation to the bulk barrier potential. The question that follows is, 'What is the highest degree of non-ideality that can be modelled using Tung's model?'

2.3. Testing the limits of Tung's model—the 'bad' diodes

As seen in table 3, the 'good' close-to-ideal diodes are very well described using Tung's model, as has been established by Im *et al* [17]. However, diodes with a large degree of non-ideality i.e. 'bad' diodes are not effectively described

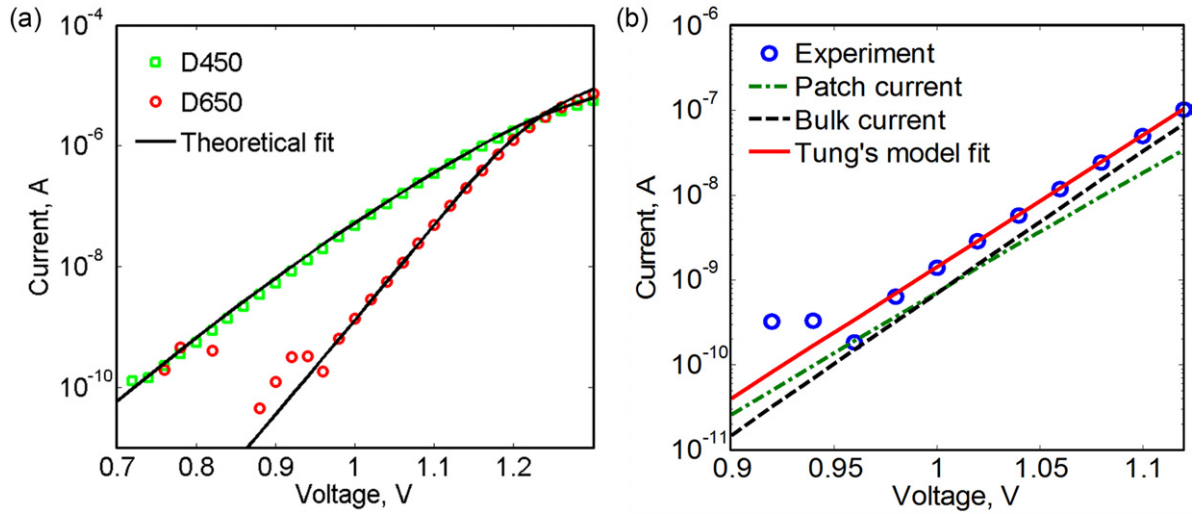

Figure 7. (*a*) Theoretical fits (black solid lines) to the I–V characteristics D450 and D650 from figure 3 using Tung's model (equation (4*a*)). The fitting parameters are shown in table 2. (*b*) A blown up view of the fit to the 650 °C annealed diode I–V characteristics and the corresponding theoretical fit. The patch current (dashed–dotted green) and bulk current (dashed black) contributions are also shown.

Table 3. Schottky barrier characteristics extracted using Tung's model.

Annealing temperature (°C)	Bulk barrier height Φ_b^o (eV)	Inhomogeneity parameter γ ($V^{1/3}$ $cm^{2/3}$)	Low barrier patch density, c_1 (cm^{-2})
As-deposited (D0)	1.75	2.55×10^{-3}	3.48×10^{-5} (unphysical)
450 (D450)	1.75	2.15×10^{-3}	1.5×10^{-3} (unphysical)
650 (D650)	1.75	7×10^{-4}	2.49×10^{5}

by this model, as was demonstrated in the previous section. While good fits can be obtained if the variables in the model are unconstrained, the values of these parameters can be highly unphysical. Therefore, we will show below that using Tung's model, idealities $n > 1.21$ cannot be described with physically meaningful parameters, setting a critical bound for the description of non-ideal Schottky diodes in any material system.

As the patch current dominates in high γ, non-ideal diode I–V, the ideality of the patch current will give an approximate value for the overall ideality factor, which is given from (2*a*) as

$$n \approx \beta \left[\frac{\delta I_{\text{patch}}}{\delta V_a}\right]^{-1} = 1 + \frac{\gamma}{3\eta^{1/3} V_{bb}^{2/3}}. \qquad (5)$$

Here, the ideality is dependent on voltage, as V_{bb}, the amount of band bending, is a voltage dependent term. Therefore, if we want to ascribe a single ideality value to a diode over a large voltage range, as is done experimentally (e.g. figure 2), then the value of γ must be small, giving a second term in the rhs of (5) that is also small compared to unity so that a single ideality value is a reasonable approximation over the entire range of measurement. Otherwise, the model fails to describe the experimental ideality which is a single value extracted from the linear region of the I–V curve, which typically spans a measurement range of a few hundred mVs. The barrier lowering within a patch with respect to the surrounding high barrier Φ_b^o at a given bias is given by $\delta = \gamma V_{bb}^{1/3}/\eta^{1/3}$, i.e. $\Phi_{\text{eff}=}\Phi_b^o - \delta$ from (2*b*). If γ is small, then in (2*b*), δ must be small compared to Φ_b^o in order for a single ideality factor to describe the entire voltage range of measurement. It is to be noted that δ is a bias-dependent parameter and is maximum at zero bias. In the discussion that follows, we will denote the zero-bias δ as δ_o.

Now, if we define a generously conservative limit of $\delta_o = 0.5\Phi_b^o$, the corresponding γ (the critical value, γ_{crit}) that can be described by Tung's model turns out to be $\sim 2.1 \times 10^{-3}$ $V^{1/3}$ $cm^{2/3}$ for a bulk barrier height $\Phi_b^o = 1.75$ eV. Using this value, from (5), we can determine the maximum possible patch ideality to be 1.42. In other words, Tung's model can be used to model only I–V characteristics with patch ideality $n \leqslant 1.42$ (at $V_a \sim 1$ V). The overall ideality of the entire current (equation (4*b*)) will be only slightly smaller, as I_{bulk} has ideality 1 by definition. The method to determine these limits more rigorously will be demonstrated in the numerical exercise below, where we see that in fact, the real limit on ideality in Tung's model is even less than $n = 1.42$. It is, however, interesting to note that this upper limit of $n = 1.42$ is applicable to inhomogeneous Schottky interfaces irrespective of the material system. The barrier lowering δ is a function of Φ_b^o, as $\delta = \gamma V_{bb}^{1/3}/\eta^{1/3}$ and V_{bb} is $\Phi_b^o - V_n$ (refer to the band diagram in figure 3). The only material sensitive parameter in this dependence is η, a function of material dielectric constant ε, the value of which is of the same order of magnitude for the most common semiconductor materials.

As shown in figure 6, at sufficiently high forward bias voltage V_a, both low barrier patches and high barrier bulk regions of the diode are turned on. At this point the diode should conduct similar current levels irrespective of the degree

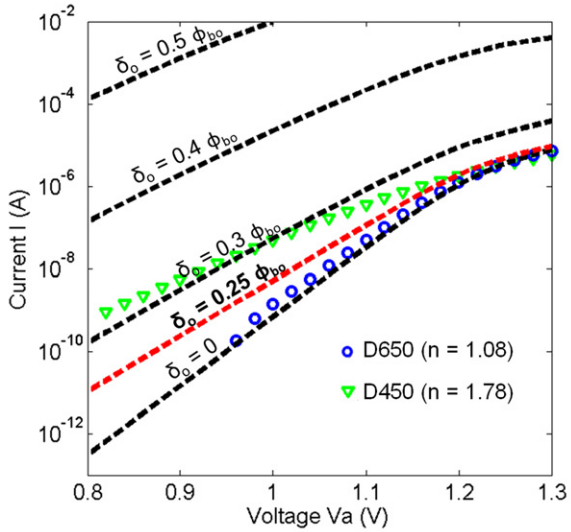

Figure 8. Diode current at various δ_o/Φ_b^o ratios. D450 and D650 are placed alongside for reference. The curve denoted by $\delta_o = 0$ curve shows the ideal thermionic emission characteristics ($n = 1$).

of Schottky barrier inhomogeneity. Therefore, we can use this bias level as a reference point, where the total diode current for all degrees of inhomogeneity (i.e. irrespective of the γ value) become comparable to each other. As can be seen from figure 2, the current in the non-ideal D0 and D450 approach D650 at approximately $V_a \sim 1.2$ V. Therefore, based on the experimental data, the γ_{crit} (maximum level of inhomogeneity that can be modelled by Tung's model) can be estimated as the γ value for which I_{total} calculated from (4*b*), is comparable to the measured current at $V_a \approx 1.2$ V with a single low barrier patch (e.g. the lower limit of patch density c_1) in the diode area. Figure 8 shows a family of I–V curves plotted using various $\delta_o < 0.5\Phi_b^o$, $\Phi_b^o = 1.75$ eV and $c_1 = 2.01\times10^3$ cm^{-2}, corresponding to a single patch in each diode. The closest match was obtained for $\delta_o = 0.25\Phi_b^o$, from which we can estimate $\gamma_{crit} = 1.1\times10^{-3}$ V$^{1/3}$ cm$^{2/3}$ and the corresponding ideality factor $n_{max} = 1.21$ (from equation (5), at $V_a \sim 1$ V). In the present study, only the D650 characteristics shows an ideality smaller than 1.21. The other two I–V curves show much higher n values (table 1), and thereby cannot be modelled meaningfully within Tung's theoretical framework. These results show that the microscopic barrier inhomogeneity at the Schottky interface can produce a worst case ideality factor of no more than 1.21. Therefore, if experimentally, values of $n > 1.21$ are obtained, as in the case of D0 and D450, we can conclude that the Schottky barrier inhomogeneity is not alone responsible for the poor ideality. For explaining this type of highly non-ideal behaviour ($n > 1.21$), other extrinsic reasons (such as interface traps, morphological defects, extrinsic impurities, etc) need to be considered, as also pointed out by Im *et al* [17].

The SiC surface is subject to various chemical and thermal treatments through the diode fabrication procedure. These treatments alter the reactivity of the surface through reconstruction and can render the surface prone to contamination. Although the standard wet chemical etching using dilute/buffered HF is supposed to produce an atomically flat surface, it has been shown to provide incomplete hydrogen termination, and a number of study have shown the presence of monolayer-thick oxygen coverage of the surface, as summarized by Seyller *et al* [28]. Surface contamination by fluorine and excess carbon (in the form of hydrocarbons) has also been reported. Another processing step that can cause surface reconstruction and/or alter the stoichiometry of the surface is the back contact annealing. Hara *et al* reported that the top (Schottky) surface became insensitive to further surface treatment following back contact annealing [29]. Although the specific form of reconstruction caused by annealing in Ar environment is unknown, UHV annealing of SiC surface has been reported to cause surface reconstruction at temperatures as low as 800 °C [28, 30]. Therefore, further study of surface structure and stoichiometry through the fabrication process is needed to gain insight into the nature of Schottky interface inhomogeneity in the highly non-ideal ($n > 1.21$) diodes.

3. Conclusion

To summarize, we report highly uniform and reproducible nickel silicide/4H-SiC Schottky barrier diodes with large barrier heights of 1.6–1.7 eV, which are among the largest values reported to this date. The diodes were fabricated on 4H-SiC homoepitaxial layers grown using the novel tetrafluorosilane (TFS) gas. The as-deposited diodes showed poor ideality ($n > 2$) and low barrier heights ($\Phi_b < 1.1$ eV). Near-ideal ($n \leqslant 1.1$), high barrier ($\Phi_b > 1.6$ eV) Schottky behaviour was obtained by post-deposition rapid thermal annealing of the contacts at 650 °C in Ar environment. For diodes fabricated on the same wafer, the measured Φ_b showed very small variation (0.1–1.5% of mean values). The results were reproduced on wafers with doping levels varying from 10^{14}–10^{16} cm^{-3}, demonstrating the robustness and consistency of the process. Using Tung's model, the barrier inhomogeneity parameters were extracted for the diode I–V characteristics measured after annealing at different temperatures. A study on the applicability limit of Tung's model indicated that the lower measured barrier height and poor ideality factor ($n > 1.21$) in the as-deposited contact cannot be modelled by Tung's model for Schottky barrier inhomogeneity alone. Rather, extrinsic sources of non-ideality, such as interface layers and/or trap levels need to be considered.

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