

Review

A practical guide to electrical characterization of interface states: Case studies on SiC and GaN

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A B S T R A C T

SiC and GaN have garnered significant attention from both academia and industry due to their promising applications. However, interface states in these devices have become a critical performance-limiting factor. Furthermore, as novel device architectures continue to evolve, the characterization of interface states presents increasingly complex challenges. Among available techniques, electrical defect characterization methods have emerged as indispensable tools for investigating interface states due to their non-destructive nature, rapid measurement capabilities, cost-effectiveness, and ability to provide comprehensive parameters—including energy distribution, energy levels, and capture cross-sections. This tutorial highlights three widely used electrical characterization techniques for interface state analysis: capacitance-voltage (CV) profiling, the conductance method, and constant-capacitance deep-level transient spectroscopy (CC-DLTS). Each technique has demonstrated value within specific measurement ranges, and practical experience suggests that combining multiple approaches often yields the most reliable results. The discussion includes fundamental principles, implementation considerations, and case studies from actual device measurements, aiming to provide experimental researchers with practical guidance. With a focus on SiC and GaN, this guide seeks to offer actionable starting points for characterizing interface states, particularly for those new to these measurement techniques.

1. Introduction

Represented by SiC and GaN, wide-bandgap semiconductor (WBS) devices, include several notable examples: SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) [1], GaN-based high electron mobility transistors (HEMTs) [2], and emerging optoelectronic devices such as GaN-based LEDs [3] and lasers [4]. These devices exhibit immense application potential across various fields [5]. However, the unavoidable presence of interface states bring in localized electronic energy states at semiconductor-oxide or semiconductor-metal interfaces, act as carrier capture or emission center. The trapped charge density is typically denoted as interface state density (D_{it}), which commonly ranges from 10^{10} to 10^{14} cm^{-2} . And different from Si, SiC and GaN lack native oxides and are prone to defect formation during growth, leading to significantly higher D_{it} values [6]. When D_{it} is sufficiently high, the Fermi level may fail to respond to interface state variations, even resulting in Fermi-level pinning, further impeding effective carrier control [7]. The detrimental effects of interface traps include mobility degradation [8], threshold voltage instability [9], and increased turn-on voltage requirements in MOSFETs [10]. When investigating interface states in WBS, conventional approaches developed for Si-based

materials cannot be directly applied lower conduction band density of states (DOS) and larger bandgaps, leading to distinct minority carrier response times and fundamentally different interface state distributions [11].

Due to these material-specific characteristics, accurately assessing D_{it} , energy distribution, and related properties in WBS becomes crucial. Existing interface state characterization techniques reveal interface properties from different perspectives. Surface-sensitive methods such as X-ray photoelectron spectroscopy [12] and atomic force microscopy primarily analyze chemical composition [13] and surface morphology. While optical techniques like Raman spectroscopy and photoluminescence detect optically active traps and recombination centers [14]. However, due to their limited resolution, these techniques encounter challenges in decoupling interface states from bulk characteristics—particularly in submicron-scale devices. Under these circumstances, electrical characterization methods exhibit numerous advantages, including non-destructiveness, compatibility with encapsulated components, and suitable for operando monitoring (e.g., during degradation or health assessment). Additionally, these methods require minimal consumables, low maintenance costs, and simple operation. Most importantly, electrical techniques provide rapid and precise

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measurements of key parameters of interface states, including D_{it} , energy distribution, capture cross-sections, mobility and so on.

Table 1 summarizes three commonly used interface state characterization techniques. Firstly, the CV method refers to an analytical technique that infers interface state effects by examining changes in CV curve characteristics (voltage shifts, stretch-out, or distortion) under varying measurement conditions, which can be subdivided into several variants such as the Terman method, high-low frequency CV(HLCV), multi-frequency CV and photo-assisted CV. It is operationally simple, cost-effective, and suitable for both laboratory research and production-line testing. Secondly, the conductance method is based on analyzing the loss that is caused by the change in the interface charge state. The conductance response is measured under AC excitation as a function of frequency, temperature, or bias. This approach offers two major advantages: *a*. it allows direct determination of D_{it} from experimental data, and *b*. it enables real-time observation of band bending and Fermi-level movement in response to gate bias variations, which are reflected in the characteristic frequency shift of the normalized conductance peak. The third method is Constant-Capacitance deep level transient spectroscopy (CC-DLTS), which overcomes the limitations of conventional DLTS in measuring high-concentration traps and inaccuracies caused by depletion region width variations. Unlike the first two steady-state methods, CC-DLTS can characterize the transient emission of interface traps, presenting interface state properties from multiple perspectives with high sensitivity. This tutorial provides a detailed introduction to three interface state characterization methods specifically tailored for early-career researchers, with illustrative applications in SiC- and GaN-based WBS and devices. These methods are systematically compared according to trap emission rates, their respective applicable conditions and advantages. The analysis enables researchers to quickly grasp the fundamental characterization approaches and gain deeper insights into interface state mechanisms.

2. Principles and application examples of three characterization methods

2.1. Capacitance-voltage method

1. High-Low CV and its improvement methods

The HLCV method was first proposed by Castagné and Vapaille [24], enabling more detailed characterization of interface state distributions within the bandgap. The fundamental concept it follows is that interface states cannot respond to the AC signal with high frequencies (e.g., 1 MHz), but fully respond at low frequencies (e.g., below 1 kHz). Consequently, the equivalent circuits differ between high and low frequencies, as illustrated in Fig. 1.

At high frequencies, the measured capacitance (C_{HF}) is governed by the series combination of the oxide capacitance (C_{ox}) and the semiconductor charge-induced capacitance (C_s). In contrast, the low-frequency capacitance (C_{LF}) comprises the parallel combination of C_s and the interface state-induced capacitance (C_{it}), subsequently connected in series with C_{ox} [30]. By comparing the voltage-dependent characteristics of C_{HF} and C_{LF} , interface state information can be derived from the equivalent circuit relationships of low-frequency CV

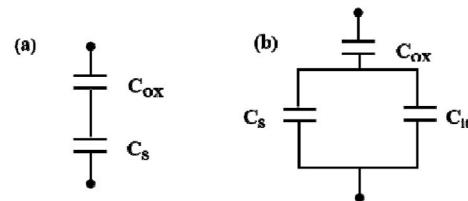


Fig. 1. Equivalent circuit diagrams of CV measurements at high (a) and low (b) frequencies.

TABLE I
Comparison of interface state characterization methods.

Method	CV Method			Conductance Method	CC-DLTS
Typical Modes	High-low CV	Multiple frequency CV	Photo-assisted CV	Frequency sweep; Temperature sweep; Bias sweep	CC-DLTS with temperature/rate-window scans
Materials	SiO ₂ /SiC	Al ₂ O ₃ /GaN, Al ₂ O ₃ /AlGaN	Al ₂ O ₃ /GaN, Al ₂ O ₃ /AlGaN	SiO ₂ /SiC	SiO ₂ /SiC, Al ₂ O ₃ /GaN
Energy Range (eV)	0.1–0.5 [15], 0.2–0.5 [16]	0.2–0.7 [17], 0.3–5.1 [18]	1.2–3.2 [19], 2.5–3.1 [20]	0.05–0.8 [21]	0.05–0.8 [22], 0.1–0.8 [23]
Core Characteristics & Principle	Measures CV at high and low frequencies; low frequencies includes interface state response, high frequencies do not; difference yields D_{it} [24].	Acquires CV at multiple frequencies; frequency response reveals trap time constants and energy distribution; often modeled with equivalent circuits [25].	Combines CV with optical excitation; light releases carriers from deep traps, revealing otherwise thermally inactive states [26].	Measures AC loss (G/ω) caused by interface state transitions vs frequency/temperature/bias; peak frequency tracks trap time constant [27].	Keeps capacitance constant to suppress depletion-width variations; measures transient emission/capture to extract activation energies and kinetics of interface states [28].
Advantages	Direct D_{it} extraction, quick measurement.	Resolves traps with different response times; covers wide energy range.	Detects deep states; effective for WBG materials; distinguishes optically active from thermally active states.	More direct D_{it} extraction near surface Fermi level; captures time constants; real-time view of band bending & Fermi-level movement.	High sensitivity; tolerates higher trap concentrations; provides activation energy, capture cross-section, time constants.
Limitations	Insensitive to slow/deep states; low frequencies data affected by leakage; accuracy depends on frequency selection.	Requires stable, precise measurement over wide frequency range; results model-dependent; complex data fitting.	Requires optical setup; interpretation complicated by photo-generated carriers.	Requires stable, low-noise setup; parasitics at high frequency; very slow or very fast traps may be missed; small-signal amplitude tuning needed [29].	Instrumentation complexity; strict temperature control; slower throughput; parameter extraction assumes capture cross-section models.
Selection Considerations	Use when shallow states are of interest; ensure low leakage for low frequency measurement.	Use for full D_{it} spectrum analysis; suitable for research-level characterization.	Use for deep-level trap analysis in WBG devices; choose illumination wavelength to match trap levels.	Choose when quantitative D_{it} around the operating bias is required; plan a broad frequency sweep; calibrate/open-short de-embedding; add temperature sweeps to widen time-constant coverage.	Use when energy-resolved trap parameters are needed; design rate windows; extend temperature range; optimize pulse width/height.

measurements, where C_{it} per unit area.

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - C_S \quad (1)$$

C_S is determined by:

$$C_S = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \quad (2)$$

$$D_{it} = \frac{C_{it}}{q} \quad (3)$$

Therefore, D_{it} can be obtained from

$$D_{it} = \left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right] / q \quad (4)$$

Based on the above theoretical framework, the measured high-frequency and low-frequency CV curves are first obtained as shown in Fig. 2(a). The Dit values extracted at different bias voltages correspond to interface states located at various energy depths within the bandgap, taking the p-type MOS capacitor as an example.

$$E_T - E_V = E_g / 2 - \left(k_b T / q \ln \left(\frac{N_d}{n_i} \right) - \varphi_s \right) \quad (5)$$

E_g stands for the bandgap width, N_d indicates the doping concentration, and n_i signifies the intrinsic carrier concentration. φ_s represents the surface potential, which can be determined from the relationship introduced by Berglund [31].

$$\varphi_s(V_1) = \int_{V_1}^{V_2} \left[1 - \frac{C(V_1)}{C_{ox}} \right] dV_1 + \varphi_s(V_2) \quad (6)$$

The voltages V_1 and V_2 in the equation can be arbitrarily selected. V_1

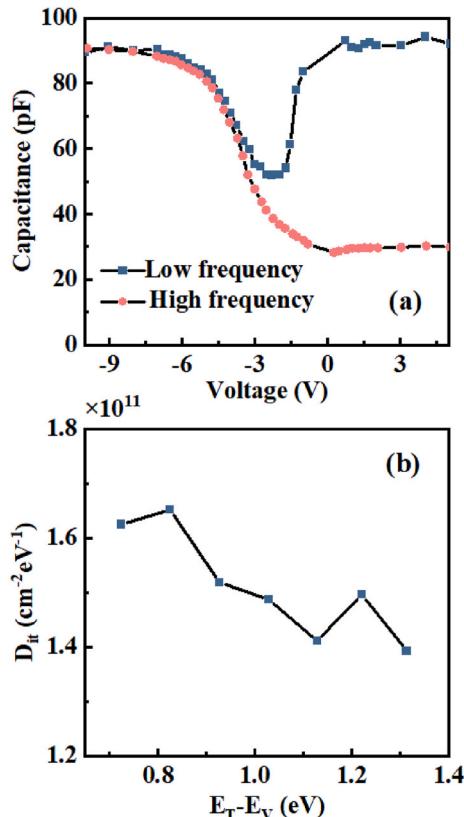


Fig. 2. (a) CV curves measured at high and low frequencies. (b) The D_{it} as a function of energy depth of interface states [37].

is typically set as an arbitrary voltage value, while V_2 is designated as a specific voltage value that makes $\varphi_s(V_2)$ equal to a constant A. The relationship between the surface potential and any applied voltage can thus be obtained. The value of A can be determined through multiple calculation methods. First, when $V_2 = V_{FB}$, the band bending is considered to be zero and $\varphi_s(V_2) = 0$, which means A = 0.

Secondly, when considering the contribution of interface states, the capacitance in this equation should employ either the low-frequency measured capacitance $C_{LF}(V_1)$ or quasi-static capacitance $C_{QS}(V_1)$. Hironoroshi Yoshioka et al. [32] proposed a method for determining parameter A in 2012. The approach is based on the linear relationship between depletion region capacitance and surface potential $\left(\frac{1}{C_{dep}} \right)^2 = - \frac{2\varphi_s}{S^2 \varepsilon_{SiC} q N_D}$.

The left-hand side of the equation can be approximated by $\left(\frac{1}{C_u + C_D} \right)^2$ obtained through equivalent circuit analysis. By plotting this linear relationship against φ_s , parameter A was determined such that the extrapolated straight line intersects the origin of the plot.

An alternative method for determining parameter A involves measuring the interface potential in both accumulation and strong inversion regions of n-type MOS devices [33–35]. This approach assumes the interface potential coincides with the conduction band edge during accumulation and the valence band edge during strong inversion, with the mid-gap position defined as their midpoint for calibration. The calibration procedure measures symmetric potential values in both regions, calculates their average to establish the mid-gap reference, then shifts the original data by this offset to align the mid-gap with zero. Notably, this method depends solely on oxide capacitance and effective reference capacitance, remaining independent of doping distribution. And then, the energy depth ($E_T - E_V$) of interface states under various applied bias can be obtained, as illustrated in Fig. 2(b).

However, in practical experiments, it is challenging to achieve sufficiently high-frequency conditions (e.g., up to 100 MHz) where defects show no response. Consequently, conventional measurements typically fail to characterize interface states with ultrafast emission rates. Moreover, high-frequency operation is susceptible to interference from series resistance and inductance, which can compromise the accuracy of capacitance measurements. These limitations are particularly critical in applications involving high-mobility samples. Furthermore, certain materials and device structures are incompatible with high-frequency measurements, as the high-frequency operation may cause irreversible damage.

Taking SiC MOSFET devices as an example, their switching characteristics are constrained by velocity-saturation capacitance and drain capacitance [36]. High-frequency measurements can lead to excessive heat accumulation, potentially damaging the device. Consequently, operation beyond specific frequency thresholds not only degrades device performance but may also impair the insulating layer and sensing capabilities, rendering ultra-high frequency measurements impractical [37]. Thus, when the experimental frequency is insufficiently high, the conventional high-low frequency CV method yields underestimated results, failing to effectively characterize rapidly emitting interface states.

2. Multi-frequency CV and Photo-Assisted CV method

In the analysis of interface state energy-depth distributions, the multi-frequency CV method is typically employed to characterize shallow energy levels, while the photo-assisted CV technique is utilized to probe deep-level states located near mid-gap. The multi-frequency CV approach measures CV curves at various frequencies, where each frequency corresponds to a specific emission time constant, enabling determination of interface state energy depths [25]. The voltage shifts between these curves represent the interface charge variation ΔQ_{it} , from which the D_{it} can be calculated, ultimately yielding comprehensive interface state distribution characteristics [38]. Fig. 3 illustrates the

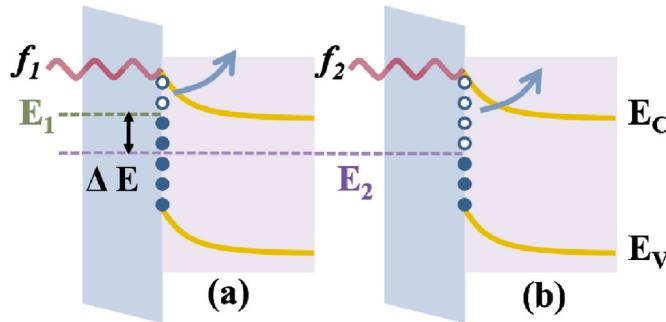


Fig. 3. Schematic diagram of the electrons emission in the interface state under different AC frequencies f_1 and f_2 . E_1 and E_2 are the energy level corresponding to f_1 and f_2 , $f_1 > f_2$.

response characteristics at the oxide-semiconductor interface using two AC signal with frequencies (f_1 and f_2 , $f_1 > f_2$).

When an AC signal with frequency f_1 is applied, the corresponding demarcation energy level depth E_1 can be determined by the following equation [38].

$$E = k_B T \ln \left(\frac{\sigma N_C v_{th}}{2\pi f} \right) \quad (9)$$

Among them, the average thermal velocity $v_{th} = \sqrt{3k_B T/m^*}$, and the effective density of states $N_C = 2 * \frac{(2\pi m^* k_B T)^{3/2}}{h^3}$, k_B is the Boltzmann constant and σ is the capture cross section. Interface states located above this demarcation energy level exhibit sufficiently short response time constants ($\tau < 1/2\pi f_1$) to follow the AC excitation, while those below this level remain inactive due to their longer response times ($\tau > 1/2\pi f_1$). When a lower-frequency AC signal ($f_1 > f_2$) is applied, the responsive region extends to deeper energy levels (E_2), creating an accessible energy window of $\Delta E = E_2 - E_1$.

The CV curves measured at different frequencies exhibit horizontal shifts along the voltage axis, from which the interface charge quantity (ΔQ_{it}) can be determined through the threshold voltage difference (ΔV_{th}). Moreover, the average D_{it} between these two energy levels can be quantitatively determined through Eq. (10) [39]:

$$D_{it}(E=E_{AVG}) = \frac{C_{ox}}{q} \frac{|V_1 - V_2|}{|E_1 - E_2|} = \frac{C_{ox}}{q} \frac{\Delta V_{th}}{\Delta E} \quad (10)$$

Among them, the average energy level E_{AVG} between E_1 and E_2 is determined by the following expression:

$$E_{AVG} = \frac{E_2 - E_1}{2} = E_1 + \frac{\Delta E}{2} \quad (11)$$

Fig. 4 presents two capacitance-voltage (CV) curves measured at distinct frequencies, 5 kHz and 50 kHz. The difference between the intersection points of the tangent extensions of the two curves at the depletion region with the x-axis is ΔV_{th} . However, in conventional multi-frequency CV measurements, interface trap states located at mid-gap exhibit extremely large time constants (τ) and remain nearly unchanged during CV sweeping. This means that the interface states do not affect on the slope of the measured CV curve but act as fixed charges [40], suggesting the difficulty for detecting the interface states using the standard CV measurement.

To characterize deeper-level interface states, the photo-assisted CV method utilizes sub-bandgap monochromatic illumination to effectively excite these slow traps. When illuminated with photon energy $h\nu_1$, all interface states located at $h\nu_1$ below the conduction band edge become activated. As the photon energy increases to $h\nu_2$, the probed energy depth extends further by $\Delta h\nu = h\nu_2 - h\nu_1$, as illustrated in **Fig. 5**. By selecting progressively higher photon energies, the defect characterization range can comprehensively cover the mid-gap region.

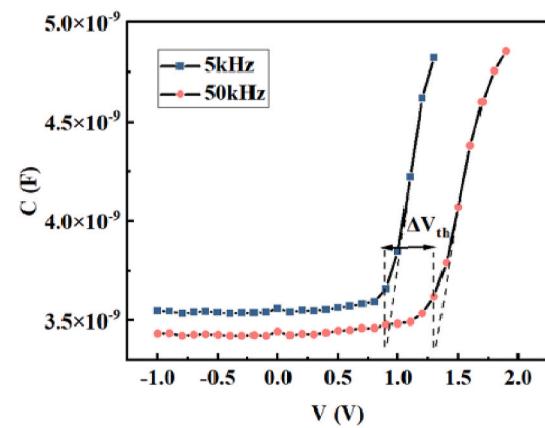


Fig. 4. This figure presents the multi-frequency CV measurement results along with the corresponding threshold voltage differences (ΔV_{th}) between the curves [25].

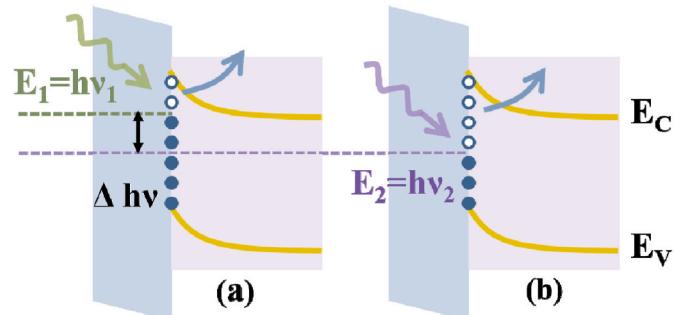


Fig. 5. The photo-assisted CV presents a schematic diagram of carrier excitation using different photon energies ($h\nu_1$ and $h\nu_2$, where $h\nu_2 > h\nu_1$), corresponding to distinct energy level depths.

Meanwhile, photo-assisted CV excitation enables direct access to deeper-level defects through band-to-band transitions and trap-assisted emission processes [35]. Mizue et al. [41] first quantitative characterization of midgap interface states in $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ structures.

Fig. 6 presents a set of results obtained through photo-assisted CV measurements. The measurement procedure consists of the following three steps:

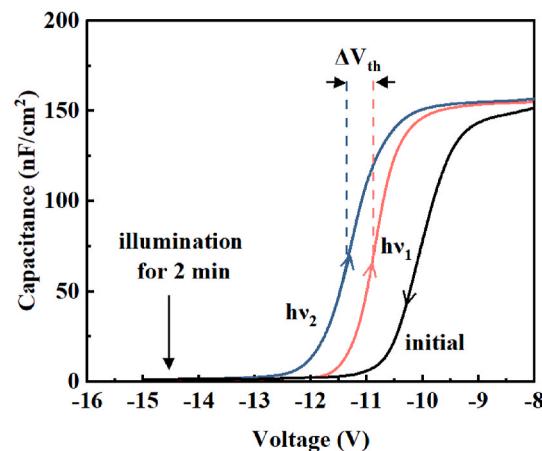


Fig. 6. The photo-assisted CV measurement results under illumination with photon energies $h\nu_1$ and $h\nu_2$ reveal distinct threshold voltage shifts (ΔV_{th}), as evidenced by the parallel displacement of the CV curves [41].

- The measurement begins with a dark CV scan from accumulation to inversion bias (black curve) to ensure complete carrier filling in interface states.
- Under fixed inversion bias, the sample is exposed to monochromatic light (photon energy below the bandgap) for 2 min, inducing photo-assisted electron emission from deep-level interface states.
- After terminating illumination, a final CV scan returns to accumulation bias, capturing the modified curve due to trap emptying. The threshold voltage is extracted from the CV curves. Similar to the multi-frequency CV method, the D_{it} in the photo-assisted CV method is determined by the following equation:

$$D_{it}(E=E_{AVG}) = \frac{C_{ox}}{q} \frac{|V_1 - V_2|}{|\hbar\nu_1 - \hbar\nu_2|} = \frac{C_{ox}}{q} \frac{\Delta V}{\Delta h\nu} \quad (12)$$

Finally, by repeating the above procedure with multiple photon energies to cover as much of the mid-gap region as possible, a more accurate determination of the interface state energy distribution can be achieved.

As demonstrated in Fig. 7, the D_{it} distribution results obtained from photo-assisted CV are compared with those from variable-frequency CV measurements. The comparison clearly reveals that the photo-assisted method provides significantly broader characterization of interface state distributions across the bandgap compared to purely electrical techniques. These two techniques are often employed to achieve comprehensive characterization of interface states across the entire bandgap.

2.2. Conductance method

Although capacitance-based methods can characterize interface states, they face a fundamental challenge: the interface-state capacitance must be extracted from the total measured capacitance, which includes contributions from the C_{ox} , C_S , and C_{it} . As previously noted, while both capacitance and conductance variations (with voltage/frequency) contain equivalent interface-state information, deriving this information from capacitance data introduces significant measurement errors. In contrast, conductance measurements avoid this limitation, as the measured conductance directly reflects interface-state properties.

Nicollian and Goetzberger [27] introduced a conductance-based technique for interface state characterization, which offers superior sensitivity and reliability compared to alternative methods. This approach enables the detection of D_{it} as low as $10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ [35]. This

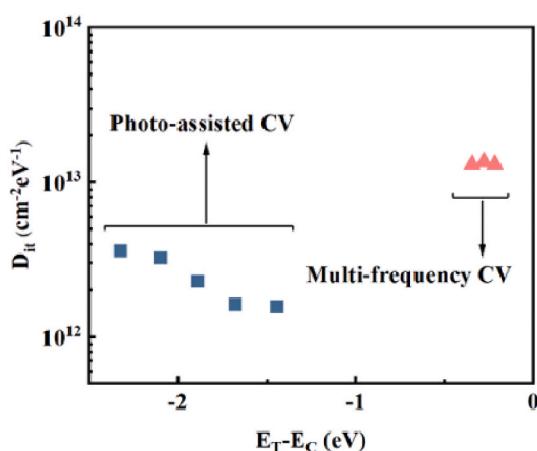


Fig. 7. Distribution of D_{it} with respect to the energy level. The red data points are the results obtained by measuring GaN MOS devices using the multi-frequency CV method. The blue data points are the results obtained by using the photo-assisted CV method [25]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

technique enables the most comprehensive characterization among commonly used methods, as it simultaneously extracts key parameters such as the D_{it} across the depletion and weak inversion regions, majority carrier capture cross-sections, and fluctuations in surface potential.

1. The theory of conductance method

Fig. 8 shows the theoretical schematic of the conductance method. Under the modulation of a small AC signal (red curve at frequency f), the band bending exhibits periodic oscillations with the amplitude of small signal voltage amplitude (V_{AC}). This causes interface states at the Fermi level depth (yellow region) to alternate between charging and discharging states [42]. When experimental parameters (temperature, frequency, bias voltage) satisfy the response conditions of interface states, carriers will emit into the conduction band as shown by the blue arrows. The emission conditions depend on both D_{it} and the DOS of the conduction band. To obtain the D_{it} distribution at different energy depths within the bandgap, various DC bias voltages can be applied to modulate the degree of band bending, thereby probing interface states at different energy levels.

In the equivalent circuit of the conductance method (Fig. 9(a)), interface states contribute an additional C_{it} that appears in parallel with C_S , forming a composite element that subsequently connects in series with C_{ox} [43]. While experimental measurements yield parallel capacitance (C_m) and conductance (G_m) values (Fig. 9(c)). Consequently, G_p of the MOS structure cannot be directly obtained and must be extracted using the following transformation:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (13)$$

In cases where the series resistance (R_s) cannot be neglected, as depicted in Fig. 9(b), the measured conductance values must be properly corrected according to Eq. (14).

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)[G_m^2 - (G_m^2 + \omega^2 C_m^2)R_s]}{[G_m - (G_m^2 + \omega^2 C_m^2)R_s]^2 + \omega^2 C_m^2} \quad (14)$$

After obtaining G_p/ω , D_{it} can be quantitatively determined under the assumption of a continuous, uniform distribution of interface states across the bandgap using Eq. (15) [27].

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau} \ln(1 + \omega^2\tau^2) \quad (15)$$

When $\left(\frac{G_p}{\omega}\right)_{max}, \frac{\partial \omega\tau}{\partial G_p} = 0$, and it is calculated that $\omega\tau = 1.98$. So D_{it} can be calculated by Ref. [25]:

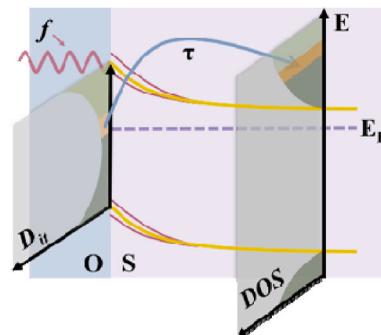


Fig. 8. Schematic of the conductance method at the oxide (O)/semiconductor (S) interface. Dark green: occupied states; light green: unoccupied states; yellow: AC-modulated states with time constant τ . (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

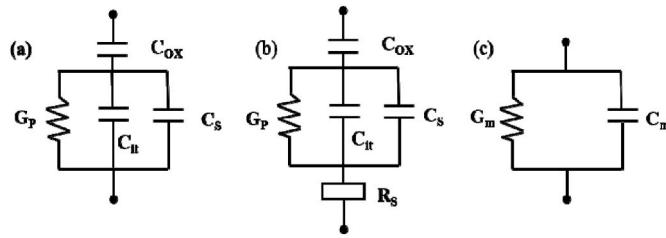


Fig. 9. (a) Equivalent circuit incorporating interface states, (b) accounting for series resistance and (c) according to experimental measurement.

$$D_{it} \approx \frac{2.5}{Sq} \frac{G_p}{\omega} \quad (16)$$

From this equation, D_{it} can be directly determined from the conductance spectrum's G_p . It is important to note that this calculation assumes uniformly distributed interface states. For more complex distributions, Section 3.3 provides a detailed discussion of advanced analysis methods.

2. Examples of the conductance method

Hironori Yoshioka et al. [44] conducted systematic investigations on the distinctive near-interface traps (NITs) introduced by nitric oxide (NO) annealing at SiO_2/SiC interfaces through the low-temperature conductance method. The conductance method provides a powerful

approach for characterizing interface states at dielectric/semiconductor interfaces.

The conductance method data analysis involves three distinct steps.

- The D_{it} is determined by extracting the peak values of normalized conductance from both temperature- and frequency-dependent measurements (Fig. 10a and b).
- The capture cross-section (σ) and trap energy level ($E_C - E_T$) can be extracted from the Arrhenius fitting using Eq. (17).

$$\tau_{peak} = \frac{1}{\sigma \nu_{th} N_C} \exp \left[\frac{E_C - E_T}{k_B T_{peak}} \right] \quad (17)$$

where τ_{peak} is given by Eq. (18).

$$\tau_{peak} = \frac{\xi(\sigma)}{\omega} \quad (18)$$

The τ_{peak} exhibits a linear relationship with frequency, the value of $\xi(\sigma)$ depends on the distribution of interface state and band bending degree. An appropriate value must be selected according to the specific interface defect characteristics, which will be explained in detail later.

- By correlating D_{it} with the energy level ($E_C - E_T$), the energy-dependent interface state distribution is obtained, with results presented in Fig. 10(d).

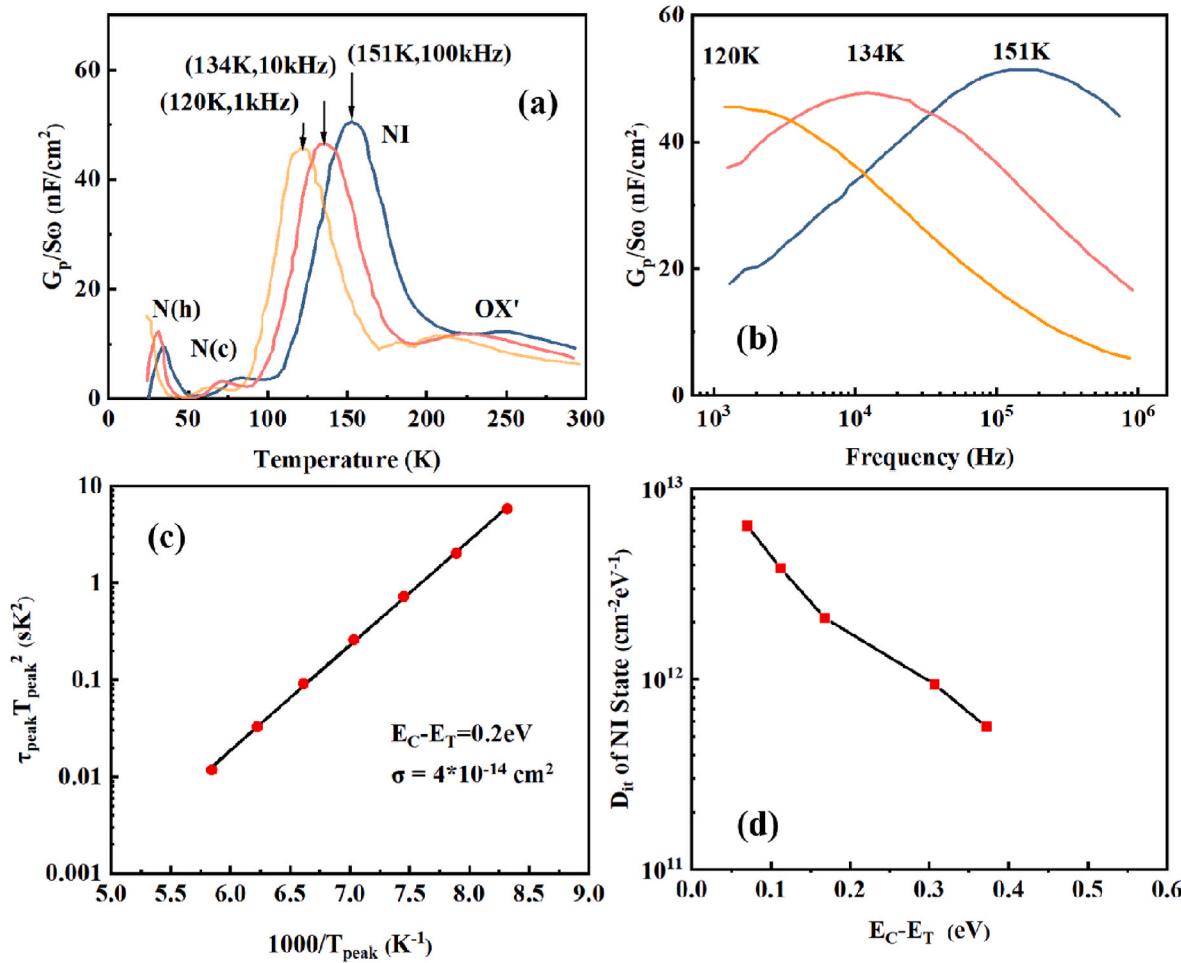


Fig. 10. The G-f-T curves (a) and G-T-f curves (b) under the same voltage; (c) The relationship between $\tau_{peak} T_{peak}^2$ and $1/T_{peak}$; (d) The distribution of the D_{it} with respect to the energy level [44].

2.3. CC-DLTS

The CC-DLTS method, originally proposed by Johnson et al. [28,45], is an advanced characterization technique derived from traditional DLTS. The approach of monitoring capacitance transients corresponding to carrier emission is replaced by a constant-capacitance method, wherein the transient voltage signal is recorded while maintaining a fixed capacitance. This modification enables accurate measurement of interface state properties.

In the traditional DLTS method, a bias voltage is applied to the traps and remains constant, then the capacitance transient is [46]:

$$C(t) = S \left[\frac{\epsilon q}{2(V_R + V_{bi})} (N_D + N_{TT}(1 - \exp(-e_n t))) \right]^{\frac{1}{2}} \quad (19)$$

where S is the sample area, ϵ is the dielectric constant, V_R is the bias voltage, V_{bi} is the built-in voltage, N_D is the doping concentration of the sample, N_{TT} is the total trap concentration, and e_n is the electron emission rate ($e_n = \frac{1}{\tau}$). Rearranging the above Eq. (19), a calculation formula for the capacitance transient that is approximately exponentially changing is obtained as

$$C(t) = S \left(\frac{\epsilon q N_D}{2(V_R + V_{bi})} \right)^{\frac{1}{2}} \left(1 - \frac{1}{2} \frac{N_{TT}}{N_D} \exp(-e_n t) \right) \quad (20)$$

In Eq. (20), it consists of two terms. According to $W = \left[\frac{2\epsilon_s(V_R + V_{bi})}{qN_D} \right]^{\frac{1}{2}}$, the first term is related to the width of the depletion region. In the second item, N_D is the doping concentration of the sample, N_{TT} is the total trap concentration, and e_n is the electron emission rate. N_D, N_{TT}, e_n are constant values under the same device, temperature, and frequency. This item changes exponentially over time. When $\frac{N_{TT}}{N_D} < 10\%$, the change in the width of the space charge region (W) has a relatively small impact on the capacitance. So at this point, the capacitance value decays exponentially with time. However, when this ratio exceeds 10%, the trapped carriers will cause a significant change in the capacitance, indicating that W has changed significantly over time. The W -dependent prefactor in Eq. (20) causes non-exponential capacitance transients, making traditional DLTS ineffective for high-concentration defects.

Consequently, maintaining a constant depletion region during emission is critical for operational stability. This is achieved through dynamic voltage adjustments that compensate for emitted charge quantities, as governed by the fundamental C-V relationship ($C = \frac{dQ}{dV}$). Experimentally, this can be achieved using a feedback circuit that stabilizes the capacitance (the CC-DLTS method), which outputs a voltage transient signal

$$V(t) = \left\{ \frac{\epsilon q S^2}{2C^2} (N_D + N_{TT}(1 - \exp(-e_n t))) \right\} - V_{bi} \quad (21)$$

In Eq. (21), the voltage transient exhibits ideal exponential characteristics, enabling precise determination of trap emission parameters through the emission rate. This method is not only applicable to high-concentration traps but also eliminates signal distortion while providing dynamic signatures. It offers enhanced sensitivity to interface states with superior energy resolution [45].

1. The theory of CC-DLTS

Fig. 11 illustrates the CC-DLTS measurement procedure [45] for a SiC-based MOS structure. The measurement begins with acquisition of the high-frequency CV characteristics (solid blue line, **Fig. 11(a)**), which establishes the operational voltage ranges for accumulation and depletion regions while simultaneously determining optimal experimental parameters. Here, pulse voltage (V_{pulse}) is applied to populate interface

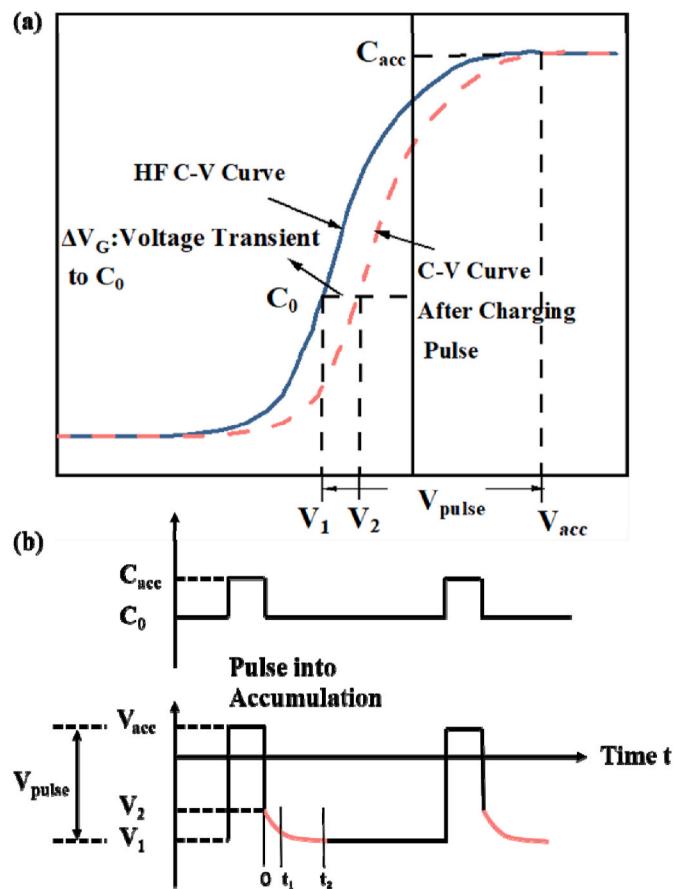


Fig. 11. (a) Capacitance-voltage characteristics during CC-DLTS measurement before (solid line) and after (dashed line) pulse voltage application. (b) Schematic representation of the capacitance (C) and applied varying voltage signal as functions of time [45].

traps, transitioning the device from depletion region ($V = V_{acc}, C = C_{acc}$) to accumulation region. The capacitance before filling (C_0), corresponding to voltage $V_1 = V_{acc} - V_{pulse}$, must remain constant during CC-DLTS measurements. After the interface state is fully filled, the CV curve exhibits a parallel shift (red dashed line), where the voltage corresponding to C_0 increases to V_2 . After complete trap emission, the system dynamically returns to V_1 through an exponential decay process mediated by a feedback system to maintain constant capacitance. The CC-DLTS signal, derived from the recorded voltage transient (solid red trace in **Fig. 11(b)**), provides direct correlation with interface trap emission characteristics.

The analysis method for voltage transients follows a strategy similar to the rate window approach in conventional DLTS. By selecting two specific time points (t_1 and t_2), the CC-DLTS signal is [45].

$$\Delta V_G = V_G(t_1) - V_G(t_2) \quad (22)$$

Thereby quantitative characterization of interface state properties are implemented.

2. Examples of CC-DLTS

Unlike traditional DLTS that shows obvious emission peaks, CC-DLTS often lacks distinct peaks owing to the continuous distribution of interface state energy levels. However, CC-DLTS can be employed to calculate D_{it} through parameters such as temperature and ΔV_G , thereby establishing the relationship between D_{it} and energy levels [46,47].

Fig. 12 presents the interface trap characterization of thermally oxidized and NO-annealed SiO₂/4H-SiC MOS structures investigated by

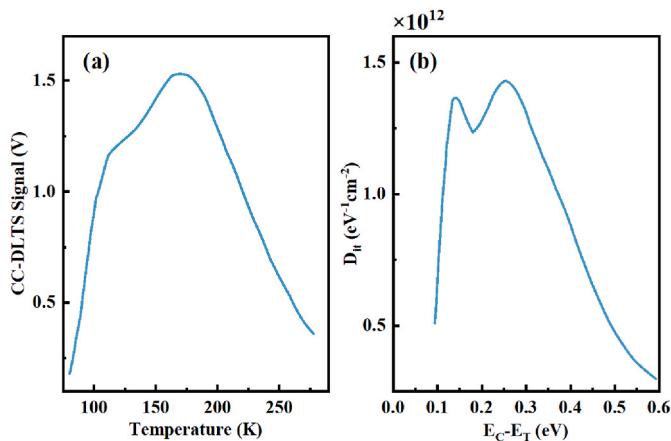


Fig. 12. (a) Temperature-dependent CC-DLTS signal (ΔV_G) for $\text{SiO}_2/4\text{H-SiC}$ MOS structures. (b) Corresponding interface trap density (D_{it}) extracted from the CC-DLTS signal in (a) [48].

X. D. Chen et al. [48] using CC-DLTS. Similar to traditional DLTS measurements, the CC-DLTS signal is then plotted as a function of temperature, as shown in Fig. 12(a).

With the capture cross sections of the different trap species established, D_{it} can be calculated from the CC-DLTS signal(ΔV_G). For electron emission from a continuous distribution of interface states, Eq. (23) is proportional to the $D_{it}(E)$, with E_C-E_T given by Eq. (24) [47,49]. Using the temperature and rate window parameters corresponding to the calculated D_{it} , the energy level E can be derived.

$$D_{it}(E) = \frac{\Delta V_G}{qk_b T \ln\left(\frac{t_1}{t_2}\right)} \frac{\epsilon_{ox}}{t_{ox}} \quad (23)$$

$$E_C - E_T = -k_B T \ln\left(\frac{\ln(t_2/t_1)}{(t_2 - t_1)\sigma_n v_{th} N_c}\right) \quad (24)$$

where ΔV_G is the voltage change between the measurement times t_1 and t_2 , ϵ_{ox} is the dielectric constant of the oxide, t_{ox} is the thickness of the oxide, σ_n is the average electron capture cross - section, v_{th} is the electron thermal velocity, N_c is the effective density of states in the conduction band, and the interface state distribution is the surface density D_{it} with the unit of $\text{cm}^{-2} \text{ eV}^{-1}$.

To accurately obtain the density of interface state defects, the CC-DLTS signals of an MOS structured sample are usually compared with those of a diode structure made of the same material and by the same process. The diode structure contains only discrete energy levels, while for the MOS, in addition to the discrete - level signals, it also contains interface - state information [47]. Therefore, a more accurate result of the concentration distribution of interface trap energy levels can be obtained by subtracting the influence of discrete energy levels.

3. Important considerations in interface state characterization

Note for beginners: This section provides foundational insights to help new researchers recognize and avoid common pitfalls in experimental measurements and data interpretation.

3.1. Measurement of slow interface states

The slow interface states have very long time constants, leading to time-dependent electrical characteristics, and the defect measurement process does not reach thermal equilibrium. The presence of slow interface states leads to hysteresis effects in the CV characteristics. As

shown in Fig. 13, a typical hysteresis loop is formed between the forward sweep (from inversion to accumulation) and the reverse sweep (from accumulation to inversion). By integrating the absolute area of the CV hysteresis curve, the relevant characteristic parameters of the slow interface states can be quantitatively evaluated. It is important to note that the magnitude of the hysteresis is significantly influenced by experimental parameters such as the voltage range and scan rate during the measurement process [51].

V. V. Afanas'ev et al. [50] observed that the flat-band voltage shift in the CV characteristics shows a pronounced increasing trend with higher accumulation region bias voltage (V_{acc}) in SiC, as demonstrated in Fig. 14. Curves (1) through (7) represent CV reverse sweeps with initial voltages ranging from 10 V to 40 V in 5 V increments. The hysteresis magnitude exhibits gradual saturation when V_{acc} surpasses a critical threshold voltage. Notably, the selection of an insufficiently low accumulation voltage may result in an underestimation of the measured D_{it} .

Katsuhisa Tanaka et al. [52], measured the capacitance-time characteristic to study the interface of Ge MOS devices. Initially, the MOS capacitor was biased under strong accumulation conditions to fully fill the slow interface states with carriers. Subsequently, the voltage was switched to depletion and this voltage was maintained during the measurement. A transient response in the capacitance was observed, requiring a relatively long period to return to a steady state. As shown in Fig. 15, the measured capacitance-time (C-t) reveals a clear relaxation characteristic, where the capacitance value increases with measurement time. The capacitance rises rapidly with time, then the rate of change gradually slows down, eventually stabilizing after a prolonged period. It is noteworthy that the relaxation time shown in the figure is quite long, exceeding 100 s without reaching full thermal equilibrium. When the measurement time for slow interface states is shorter, there can be a significant discrepancy between the measured capacitance value and the steady-state value.

John R. Hauser et al. [53] discovered the influence of scan rate on the CV characteristics of MOS capacitors. As shown in Fig. 16, the degree of shift in the CV curves exhibits a significant correlation with the scan rate. As the scan rate increases, the CV curves systematically shift toward the negative bias direction; conversely, when the scan rate decreases, the CV curves gradually approach the quasi-static theoretical curve. This scan rate-dependent shift phenomenon can lead to an underestimation of the D_{it} at specific energy levels when calculating their values.

Therefore, when conducting measurements for slow interface states, the recommended experimental strategies include: (1) Maintain the same initial accumulation voltage when performing measurements under different frequencies or temperature conditions; (2) Select a sufficiently large accumulation region bias voltage to ensure that the interface state carriers reach a fully filled; and (3) Use a slower scan rate

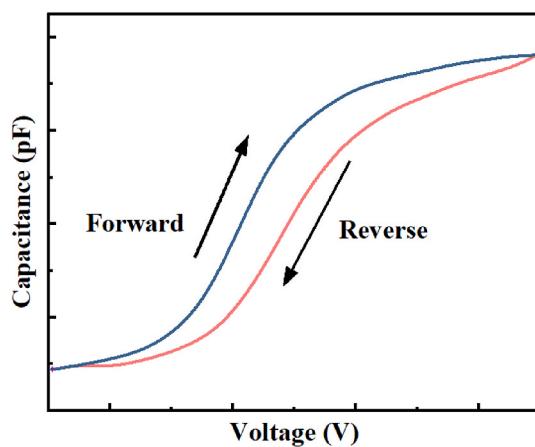


Fig. 13. Schematic representation of the CV hysteresis curve.

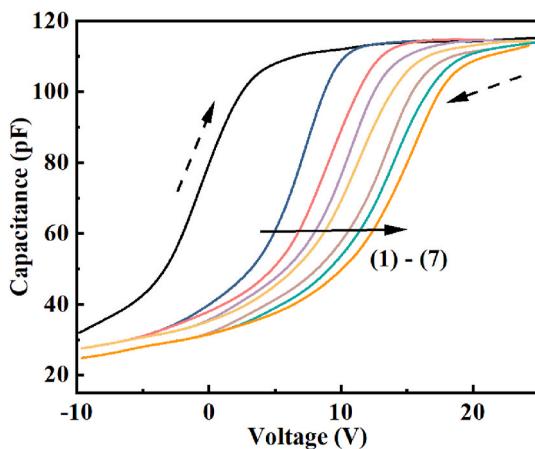


Fig. 14. CV characteristics of a SiC MOS capacitor under varying bias conditions. Curves 1–7 correspond to reverse sweeps with progressively increasing maximum V_{acc} from 10 V to 40 V in 5 V increments. Arrows indicate the voltage sweep direction (forward and reverse) [50].

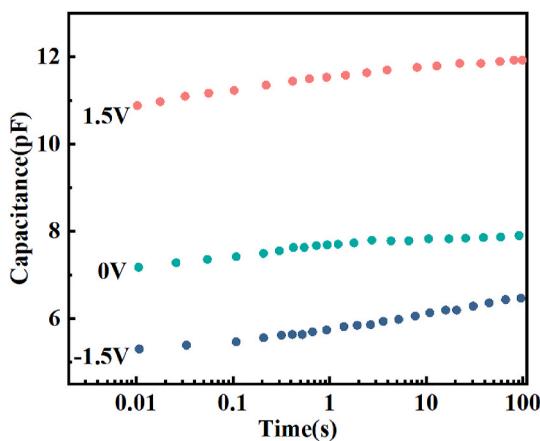


Fig. 15. Capacitance as a function of time. The voltage values in the figure represent the bias voltage applied during measurement [52].

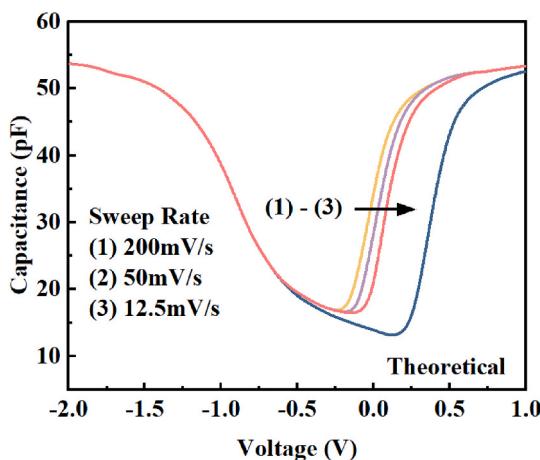


Fig. 16. Sweep-rate dependence of CV characteristics in MOS. The purple curves is calculated from theory [53]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

for measurements. These optimized parameters can effectively reduce measurement errors, thereby improving the accuracy of extracting key parameters such as D_{it} .

3.2. Measurement of fast interface states

Fast interface states are characterized by emitted carriers exhibiting extremely small time constants, which present significant measurement challenges in capacitance spectroscopy systems. [30]. In n-type semiconductors, the relationship between the time constant and the energy level depth (E_T) follows Eq. (25).

$$\tau = \frac{1}{\sigma \nu_{th} N_C} \exp \left[\frac{E_C - E_T}{k_b T} \right] \quad (25)$$

σ denotes the capture cross-section, ν_{th} is the thermal velocity of electrons, N_C is the effective density of states in the conduction band, $E_C - E_T$ is the energy difference between the interface trap level and the conduction band edge, k_b is the Boltzmann constant, and T is the temperature. Therefore, small time constants correspond to interface trap states in close proximity to the conduction band (or valence band for p-type devices)

Furthermore, measurement of fast interface states requires careful consideration of operational frequency and temperature parameters. Taking SiC as a representative material, the schematic diagram in Fig. 17 illustrates the relationship between response time constants of interface states with varying energy level depths versus measurement frequency and temperature requirements. The horizontal axis represents the depth of the interface state energy levels, while the left vertical axis denotes the time constant, and the corresponding right vertical axis indicates the measurement frequency [42]. Here, typical parameters of SiC MOS capacitors are adopted, such as capture cross-section of the interface states remains constant across the bandgap, with $\sigma = 1 \times 10^{-16} \text{ cm}^2$, $\nu_{th} = 1.87 \times 10^7 \text{ cm/s}$, and $N_C = 1.83 \times 10^{19} \text{ cm}^{-3}$. For 300 K (room temperature), the responsive energy levels are predominantly distributed within 0.1–0.4 eV below the conduction band [44]. As operational temperature decreases, the same measurement system enables access to energy levels closer to the conduction band edge, facilitating detection of ultrafast interface states.

Consequently, the strategy of lowering the measurement temperature is often adopted by researchers to study fast interface states [54]. Yoshioka et al. [44] observed no distinct interface state signals in the $G_p/\omega-\omega$ characteristic curves under room temperature conditions. However, this result does not entirely rule out the existence of fast interface states, as even when the MOS capacitor is biased into the strong

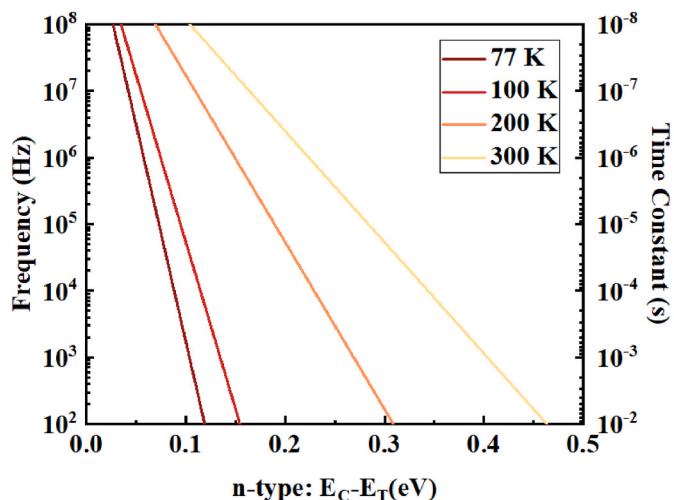


Fig. 17. Time constants for hole emission from an interface state to the majority carrier band in a n-type semiconductor.

accumulation region, fast interface states may still remain undetectable. Fig. 18 (a) shows the $G_p/\omega\omega$ characteristic curves measured at 220 K, where only two peaks (signal of interface state) under each were detected. As the temperature decreases, the response time of the interface state slows down, enabling the effective extraction of interface state signals under more bias voltages, as illustrated in Fig. 18(b)-(d) [55]. Different bias voltages correspond to shifts in the Fermi level position, which can be used to study the impact of interface states on band bending.

3.3. Extracting time constants from the spectrum of dispersion characteristics

Unlike Si materials, WBS often exhibit a strong asymmetry in the conductance peak as a function of frequency [30]. This phenomenon is attributed to the dispersion of the interface trap time constant, which is caused by fluctuations in the surface potential due to non-uniformities in oxide charge, interface states, and doping density [35]. This situation implies that the previous theoretical calculation methods can no longer be applied to determine D_{it} and capture cross-sections.

According to Nicollian's theory [27], the dependence curve of G_p/ω on frequency can reveal distinct characteristics of interface state distributions, as illustrated in Fig. 19. When the interface states are of a single level, the peak signal occurs at $\omega\tau = 1$, satisfying the $\frac{G_p}{\omega} = \frac{q\sigma D_{it}}{1+(\omega\tau)^2}$, as shown by the blue line in Fig. 19 (1). In cases where the interface states are continuous distributed across the measured range, the condition $\omega\tau = 1.98$ is met, adhering to the $\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau} \ln(1 + \omega^2\tau^2)$, as shown by the red line in Fig. 19 (2).

However, when the interface state distribution is significantly influenced by dispersion, the value of $\omega\tau$ must be determined through fitting. As shown in Fig. 19, the interface state signal affected by dispersion exhibits a broader peak. Assuming the interface states follow a Gaussian distribution, they satisfy Eq. (26) [35].

$$\frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{U_s - \bar{U}_s}{2\sigma^2}\right) dU_s \quad (26)$$

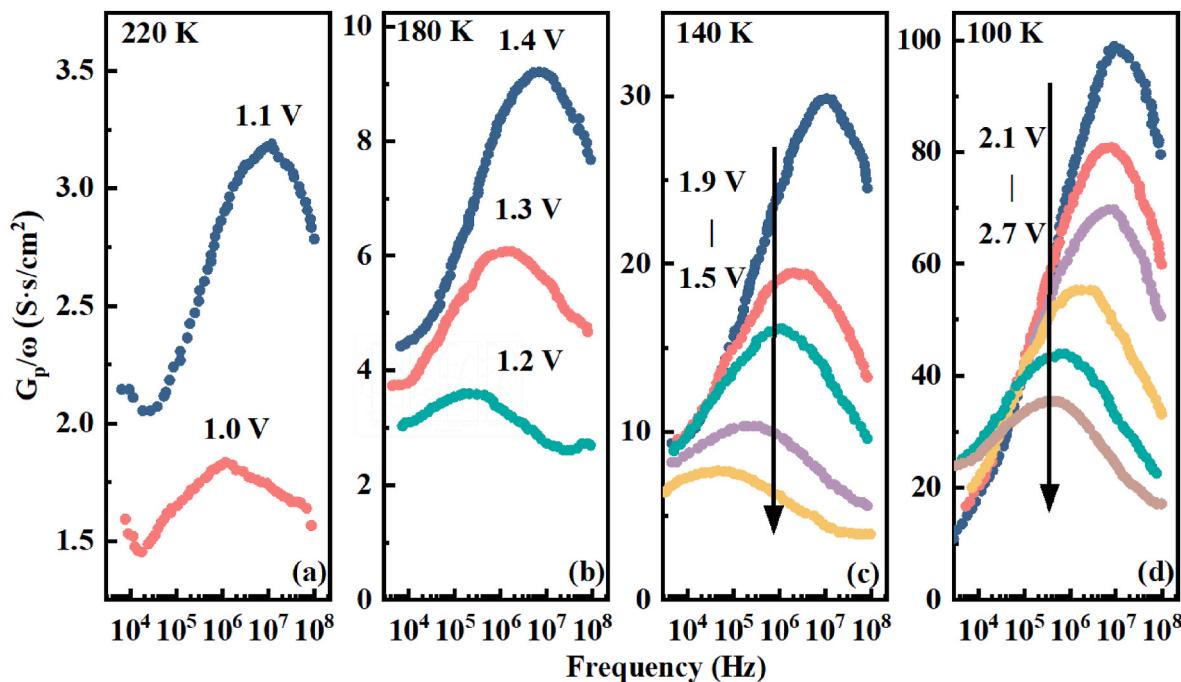


Fig. 18. It illustrates the conductance G_p/ω as a function of ω at temperatures of 220 K, 180 K, 140 K, and 100 K. Each curve represents the measurement results under different bias voltages. As the temperature decreases, the range of measurable bias voltages expands [55].

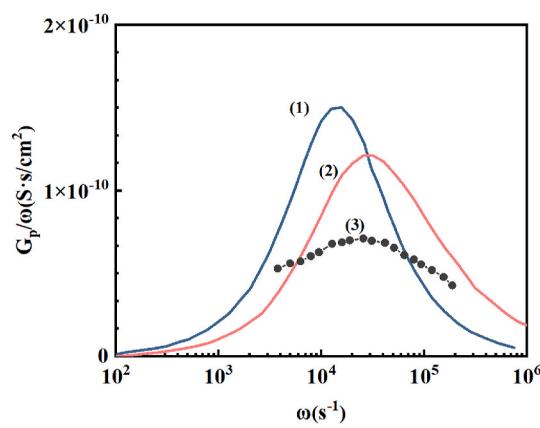


Fig. 19. It illustrates how the G_p/ω versus frequency curves reflect three distinct distributions of interface states. (1) corresponds to the case where the interface states are at a single level, exhibiting no time constant dispersion. (2) represents a continuous distribution of interface states with constant density and capture probability, typically assumed to be uniformly distributed across the measured range. (3) depicts the measured data that exhibits time constant dispersion [35].

Here, \bar{U}_s and σ represent the normalized mean surface potential and standard deviation, respectively, ω denotes the frequency corresponding to the peak of the measured curve, and τ_{it} is the emission rate associated with the interface states. By fitting the experimentally measured G_p/ω versus frequency characteristic curve, key parameters such as the D_{it} and the interface state time constant (τ_{it}) can be accurately extracted.

3.4. Key distinctions and caveats versus conventional Si-based device methods

WBS such as SiC and GaN have less mature epitaxial growth and processing technologies compared to Si, leading to generally higher interface trap densities and interface states whose nature and energy distribution are not yet well understood. Unlike the relatively smooth

distribution of interface traps at Si/SiO₂ interfaces, WBS exhibit more non-uniform distributions. For instance, SiC/SiO₂ interfaces often show a high density of traps near the conduction band [56]. In Si, the capture cross section is usually assumed to be energy-independent; in contrast, WBS frequently display asymmetric conductance peaks, which further indicates non-uniform D_{it} distributions and dynamics. Moreover, owing to their larger bandgaps, some traps in WBS exhibit slow response times, which prevents conventional low-frequency CV measurements from fully capturing the entire trap response. At the same time, the conventional Terman method based on high-frequency CV is not suitable for WBS and may even cause device damage [57], while calculating ideal CV curves accurately is also difficult due to the lack of reliable model [43]. As a result, characterization of interface traps in WBS often relies on more sophisticated techniques, such as the conductance method and CC-DLTS, along with more complex data processing and interpretation. Furthermore, accurate determination of the C_{ox} is critical for reliable device characterization. Unlike conventional Si-based MOS structures where C_{ox} can be approximated from accumulation capacitance, WBS require independent measurements due to their significantly lower conduction band DOS [42].

4. Conclusion

This tutorial provides a comparative analysis of the three most widely-used electrical methods for interface state characterization: CV analysis, the conductance method, and CC-DLTS. While presenting these fundamental techniques in an accessible format for beginners, we emphasize that interface state characterization remains a nuanced field requiring deeper exploration. For each method, we systematically examine the operating principles, practical implementation considerations, and specific advantages/limitations, enabling researchers to select appropriate approaches for quantitative D_{it} measurement with improved accuracy and reliability.

At present, the study of interface states necessitates a comprehensive

evaluation that integrates multiple characterization techniques, combined with in-depth analysis supported by precise computational methods and detailed physical models. As no single technique can capture the full complexity of interface phenomena, a hybrid and cross-validated approach is increasingly required.

To overcome the limitations imposed by interface states on device performance, future research should focus on the development of more accurate, robust, and scalable measurement techniques, as well as effective defect passivation strategies. In particular, the characterization and modeling of interface states in nanoscale devices and emerging semiconductor materials remain areas where significant theoretical challenges must be addressed. Furthermore, the systematic accumulation of high-quality empirical data will be essential to refine existing models and advance the understanding of defect dynamics, ultimately driving technological innovation in next-generation electronic devices.

CRediT authorship contribution statement

Zilan Wang: Writing – original draft. **Hongling Wu:** Writing – original draft. **Haoyang Li:** Data curation. **Jiaxuan Yang:** Data curation. **Francis C.C. Ling:** Writing – review & editing. **Lai Wang:** Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix

Table 2 lists the commonly used parameters in the measurement of interface states for two WBS. The average thermal velocity $v_{th} = \sqrt{3k_B T/m^*}$, and the effective density of states $N_C = 2 * \frac{(2\pi m^* k_B T)^{\frac{3}{2}}}{h^3}$. Here, k_B is the Boltzmann constant and h is the Planck constant [52].

Table 2
Commonly Used Parameters for the Characterization of Interface States in SiC and GaN

Temperature (K)	SiC			p-type		
	n-type			v_{th} (cm/s)	N_V (cm ⁻³)	$m^*(1m_0)$ (kg)
	v_{th} (cm/s)	N_C (cm ⁻³)	$m^*(0.29m_0)$ (kg)			
77	1.10×10^5	3.92×10^{15}	2.64×10^{-31}	5.92×10^4	3.27×10^{15}	9.11×10^{-31}
100	1.25×10^5	2.14×10^{15}		6.74×10^4	4.84×10^{15}	
200	1.77×10^5	7.55×10^{15}		9.53×10^4	1.37×10^{16}	
300	2.17×10^5	5.10×10^{15}		1.17×10^5	2.51×10^{16}	
Temperature (K)	GaN					
	n-type			v_{th} (cm/s)	N_V (cm ⁻³)	$m^*(0.9m_0)$ (kg)
	v_{th} (cm/s)	N_C (cm ⁻³)	$m^*(0.22m_0)$ (kg)			
77	1.26×10^5	3.37×10^{14}	2×10^{-31}	6.24×10^4	2.79×10^{15}	8.2×10^{-31}
100	1.44×10^5	4.99×10^{14}		7.11×10^4	4.13×10^{15}	
200	2.03×10^5	1.41×10^{15}		1.00×10^5	1.17×10^{16}	
300	2.49×10^5	2.59×10^{15}		1.23×10^5	2.15×10^{16}	

Data availability

The data that has been used is confidential.

References

- [1] M. Cabello, V. Soler, G. Rius, Cal. Advanced processing for mobility improvement in 4H-SiC MOSFETs: a review, *Mater. Sci. Semicond. Process.* 78 (2018) 22–31.
- [2] U.K. Mishra, P. Parikh, Yi-Feng Wu, AlGaN/GaN HEMTs—an overview of device operation and applications, *Proc. IEEE* 90 (6) (June 2002) 1022–1031, <https://doi.org/10.1109/JPROC.2002.1021567>.
- [3] H.S. Wasito, J.D. Prades, J. Güllink, et al., Beyond solid-state lighting: miniaturization, hybrid integration, and applications of GaN nano-and micro-LEDs, *Appl. Phys. Rev.* 6 (4) (2019).
- [4] K. Jiang, P. Zhang, S. Song, et al., A review of ultra-short pulse laser micromachining of wide bandgap semiconductor materials: SiC and GaN, *Mater. Sci. Semicond. Process.* 180 (2024) 108559.
- [5] H. Morkoc, S. Strite, G.B. Gao, et al., Large-band-gap SiC, III-V nitride, and II-VI zinc-based semiconductor device technologies, *J. Appl. Phys.* 76 (3) (1994) 1363–1398.
- [6] S. Wirths, G. Alfieri, A. Prasmusinto, et al., Improved SiO₂/4H-SiC Interface Defect Density Using Forming Gas Annealing[C]//Materials Science Forum, 963, Trans Tech Publications Ltd, 2019, pp. 465–468.
- [7] K. Martens, W. Wang, K. De Keersmaecker, et al., Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS CV and GV characteristics, *Microelectron. Eng.* 84 (9–10) (2007) 2146–2149.
- [8] A. Pérez-Tomás, P. Godignon, N. Mestres, et al., A field-effect electron mobility model for SiC MOSFETs including high density of traps at the interface, *Microelectron. Eng.* 83 (3) (2006) 440–445.
- [9] S. Yu, M. Kang, T. Liu, et al., Bias-induced threshold voltage instability and interface trap density extraction of 4H-SiC MOSFETs [C]. IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2019, pp. 420–424, 2019.
- [10] D. Peters, T. Aichinger, T. Basler, et al., Investigation of threshold voltage stability of SiC MOSFETs [C]. 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2018.
- [11] R. Yeluri, X. Liu, B.L. Swenson, et al., Capacitance-voltage characterization of interfaces between positive valence band offset dielectrics and wide bandgap semiconductors, *J. Appl. Phys.* 114 (8) (2013).
- [12] Hinkle C L, Vogel E M, Ye P D, et al. Interfacial Chemistry of Oxides on Inxga (1–x) As and implications for MOSFET applications, *Curr. Opin. Solid State Mater. Sci.* 15 (5) (2011) 188–207.
- [13] S.R. Kodigala, S. Chattopadhyay, C. Overton, et al., Growth and surface analysis of SiO₂ on 4H-SiC for MOS devices, *Appl. Surf. Sci.* 330 (2015) 465–475.
- [14] M. Yoshikawa, K. Kosaka, H. Seki, et al., Stress characterization of 4H-SiC metal–oxide–semiconductor field-effect transistor (MOSFET) using raman spectroscopy and the finite element method, *Appl. Spectrosc.* 70 (7) (2016) 1209–1213.
- [15] H. Yoshioka, T. Nakamura, T. Kimoto, Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance, *J. Appl. Phys.* 111 (1) (2012).
- [16] T. Kobayashi, J. Suda, T. Kimoto, Reduction of interface state density in SiC (0001) MOS structures by post-oxidation Ar annealing at high temperature, *AIP Adv.* 7 (4) (2017).
- [17] W. Yang, J.S. Yuan, B. Krishnan, et al., Characterization of deep and shallow traps in GaN HEMT using multi-frequency CV measurement and pulse-mode voltage stress, *IEEE Trans. Device Mater. Reliab.* 19 (2) (2019) 350–357.
- [18] X.H. Ma, W.W. Chen, L. Yang, et al., Method of evaluating interface traps in Al₂O₃/AlGaN/GaN high electron mobility transistors, *Chin. Phys. B* 28 (6) (2019) 067304.
- [19] Y. Irokawa, T. Nabatame, K. Yuge, et al., Investigation of Al₂O₃/GaN interface properties by sub-bandgap photo-assisted capacitance-voltage technique, *AIP Adv.* 9 (8) (2019).
- [20] J.R. Nicholls, A.M. Vidarsson, D. Haasemann, et al., A method for characterizing near-interface traps in SiC metal–oxide–semiconductor capacitors from conductance–temperature spectroscopy measurements, *J. Appl. Phys.* 129 (5) (2021).
- [21] K.K. Lee, G. Pensl, M. Soueidan, et al., Very low interface state density from thermally oxidized single-domain 3C-SiC/6H-SiC grown by vapour–liquid–solid mechanism, *Jpn. J. Appl. Phys.* 45 (9R) (2006) 6823.
- [22] A. Jayawardena, X. Shen, P.M. Mooney, et al., Mechanism of phosphorus passivation of near-interface oxide traps in 4H-SiC MOS devices investigated by CCDLTS and DFT calculation, *Semicond. Sci. Technol.* 33 (6) (2018) 065005.
- [23] R.D. Long, C.M. Jackson, J. Yang, et al., Interface trap evaluation of Pd/Al₂O₃/GaN metal oxide semiconductor capacitors and the influence of near-interface hydrogen, *Appl. Phys. Lett.* 103 (20) (2013).
- [24] R. Castagne, A. Vapaille, Description of the SiO₂–Si interface properties by means of very low frequency MOS capacitance measurements, *Surf. Sci.* 28 (1) (1971) 157–193.
- [25] S. Yang, Z. Tang, K.Y. Wong, et al., Mapping of interface traps in high-performance Al₂O₃/AlGaN/GaN MIS-heterostructures using frequency-and temperature-dependent CV techniques. 2013 IEEE International Electron Devices Meeting, IEEE, 2013, 6.3. 1-6.3. 4.
- [26] Y. Hori, Z. Yatabe, T. Hashizume, Characterization of interface states in Al₂O₃/AlGaN/GaN structures for improved performance of high-electron-mobility transistors, *J. Appl. Phys.* 114 (24) (2013).
- [27] E.H. Nicollian, A. Goetzberger, The si-sio, interface–electrical properties as determined by the metal-insulator-silicon conductance technique, *Bell Sys. Tech. J.* 46 (6) (1967) 1055, 1033.
- [28] N.M. Johnson, D.J. Bartelink, R.B. Gold, et al., Constant-capacitance DLTS measurement of defect-density profiles in semiconductors, *J. Appl. Phys.* 50 (7) (1979) 4828–4833.
- [29] Y. Karamoto, X. Zhang, D. Okamoto, M. Sometani, T. Hatakeyama, S. Harada, N. Iwamuro, H. Yano, Analysis of fast and slow responses in AC conductance curves for p-type SiC MOS capacitors, *Jpn. J. Appl. Phys.* 57 (6S3) (2018) 06KA06.
- [30] Jr J.A. Cooper, Advances in SiC MOS technology, *Phys. Status Solidi* 162 (1) (1997) 305–320.
- [31] C.N. Berglund, Surface states at steam-grown silicon-silicon dioxide interfaces, *IEEE Trans. Electron. Dev.* (10) (2005) 701–705.
- [32] Hironori Yoshioka, Takashi Nakamura, Tsunenobu Kimoto, Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance, *J. Appl. Phys.* 111 (1) (2012) 014502.
- [33] S. Nishimatsu, M. Ashikawa, A simple method for measuring the interface state density, *Rev. Sci. Instrum.* 45 (Sept. 1984) 1109–1112.
- [34] T.C. Lin, D.R. Young, New methods for using the Q-V technique to evaluate Si–SiO₂ interface states, *J. Appl. Phys.* 71 (April 1992) 3889–3893.
- [35] D.K. Schroder, *Semiconductor Material and Device Characterization*[M], John Wiley & Sons, 2015.
- [36] P. Fiorenza, F. Giannazzo, F. Roccaforte, Characterization of SiO₂/4H-SiC interfaces in 4H-SiC MOSFETs: a review, *Energies* 12 (12) (2019) 2310.
- [37] J.N. Shenoy, G.L. Chindalore, M.R. Melloch, et al., Characterization and optimization of the SiO₂/SiC metal-oxide semiconductor interface, *J. Electron. Mater.* 24 (1995) 303–309.
- [38] Y. Hori, C. Mizue, T. Hashizume, Interface state characterization of ALD-Al₂O₃/GaN and ALD-Al₂O₃/AlGaN/GaN structures, *Phys. Status Solidi C* 9 (6) (2012) 1356–1360.
- [39] M. Fagerlin, F. Allerstam, E.Ö. Sveinbjörnsson, et al., Investigation of the interface between silicon nitride passivations and AlGaN/AlN/GaN heterostructures by C(V) characterization of metal-insulator-semiconductor-heterostructure capacitors, *J. Appl. Phys.* 108 (1) (2010).
- [40] S. Yang, Z. Tang, K.Y. Wong, et al., Mapping of interface traps in high-performance Al₂O₃/AlGaN/GaN MIS-heterostructures using frequency-and temperature-dependent CV techniques. 2013 IEEE International Electron Devices Meeting, IEEE, 2013, 6.3. 1-6.3. 4.
- [41] Y. Hori, C. Mizue, T. Hashizume, Interface state characterization of ALD-Al₂O₃/GaN and ALD-Al₂O₃/AlGaN/GaN structures, *Phys. Status Solidi C* 9 (6) (2012) 1356–1360.
- [42] R. Engel-Herbert, Y. Hwang, S. Stemmer, Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces, *J. Appl. Phys.* 108 (12) (2010).
- [43] E.H. Nicollian, J.R. Brews, *Mos (Metal Oxide Semiconductor) Physics and Technology*[M], John Wiley & Sons, 2002.
- [44] H. Yoshioka, T. Nakamura, T. Kimoto, Characterization of very fast states in the vicinity of the conduction band edge at the SiO₂/SiC interface by low temperature conductance measurements, *J. Appl. Phys.* 115 (1) (2014).
- [45] N.M. Johnson, Measurement of semiconductor–insulator interface states by constant-capacitance deep-level transient spectroscopy, *J. Vac. Sci. Technol.* 21 (2) (1982) 303–314.
- [46] R.Y. Dejule, M.A. Haase, D.S. Ruby, et al., Constant capacitance DLTS circuit for measuring high purity semiconductors, *Solid State Electron.* 28 (6) (1985) 639–641.
- [47] C.M. Jackson, A.R. Arehart, E. Cinkilic, et al., Interface trap characterization of atomic layer deposition Al₂O₃/GaN metal-insulator-semiconductor capacitors using optically and thermally based deep level spectroscopies, *J. Appl. Phys.* 113 (20) (2013).
- [48] X.D. Chen, S. Dhar, T. Isaacs-Smith, et al., Electron capture and emission properties of interface states in thermally oxidized and NO-annealed SiO₂/4H-SiC, *J. Appl. Phys.* 103 (3) (2008).
- [49] N.M. Johnson, D.J. Bartelink, R.B. Gold, J.F. Gibbons, Constant-capacitance DLTS measurement of defect-density profiles in semiconductors, *J. Appl. Phys.* 50 (7) (1979) 4828–4833.
- [50] V.V. Afanas' ev, A. Stesmans, M. Bassler, et al., Shallow electron traps at the 4H-SiC/SiO₂ interface, *Appl. Phys. Lett.* 76 (3) (2000) 336–338.
- [51] A.R. Peaker, V.P. Markevich, J. Coutinho, Tutorial: junction spectroscopy techniques and deep-level defects in semiconductors, *J. Appl. Phys.* 123 (16) (2018).
- [52] K. Tanaka, R. Zhang, M. Takenaka, et al., Quantitative evaluation of slow traps near Ge MOS interfaces by using time response of MOS capacitance, *Jpn. J. Appl. Phys.* 54 (4S) (2015), 04DA02.
- [53] J.R. Hauser, Bias sweep rate effects on quasi-static capacitance of MOS capacitors, *IEEE Trans. Electron. Dev.* 44 (6) (1997) 1009–1012.
- [54] M. Weger, J. Kuegler, M. Nelhiebel, et al., Photon-assisted electron depopulation of 4H-SiC/SiO₂ interface states in n-channel 4H-SiC metal-oxide-semiconductor field effect transistors, *J. Appl. Phys.* 136 (3) (2024).

- [55] W.C. Kao, M. Goryll, M. Marinella, et al., Characterization of fast interface states in nitrogen-and phosphorus-treated 4H-SiC MOS capacitors, *Semicond. Sci. Technol.* 30 (7) (2015) 075011.
- [56] H.L. Rao Maddi, S. Nayak, V. Talesara, Y. Xu, W. Lu, A.K. Agarwal, Characterization of near conduction band SiC/SiO₂ interface traps in commercial 4H-SiC power MOSFETs. 2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (Wipda), 2022, pp. 22–25.
- [57] C. Yuan, R. Hanus, S. Graham, A review of thermoreflectance techniques for characterizing wide bandgap semiconductors' thermal properties and devices' temperatures, *J. Appl. Phys.* 132 (22) (2022).