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Application of Phosphorus-Doped Polysilicon-Based Full-Area Passivating Contact on the Front Textured Surface of *p*-Type Silicon

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A *p*-type crystalline silicon (c-Si) passivated emitter and rear contact (PERC) nowadays have become mainstream in the highly competitive photovoltaic market. Herein, the recently popular passivating contact concept on the front textured surface of *p*-type c-Si PERC solar cells is applied. The full-area textured passivating contact consists of an ultrathin SiO_2 film of ≈1.5 nm thickness grown with thermal oxidation and phosphorus-doped polysilicon (poly-Si) contact layer by low-pressure chemical vapor deposition. A detailed investigation of poly-Si with different crystalline structures, doping conditions, and thicknesses on the passivation effect and parasitic absorption loss is carried out. Preliminary achievement of 21.3% efficiency is realized in large-area (244.3 cm^2) *p*-PERC c-Si solar cells without the need for additional laser selective redoping. Theoretical calculation expects that the cell efficiency can be enhanced to 23.4% by decreasing the recombination current to a reasonable level. It is demonstrated that further improvement of low-cost *p*-PERC c-Si solar cells is feasible using the full-area textured passivating contact processes which are fully compatible with existing production lines.

Crystalline silicon (c-Si) solar cells nowadays dominate the global photovoltaic (PV) market due to their high conversion efficiency and mature industrial technology, and experience the transition from the conventional c-Si aluminum-back surface field (Al-BSF) design into passivated emitter and rear contact (PERC) solar cells. Traditional Al-BSF solar cells suffer from severe carrier recombination because of the direct contact between metal and semiconductor on the back side, and meanwhile lack the light reflection of a dielectric film for long wavelength. PERC solar cells greatly reduce these photoelectric losses by implementing a rear dielectric passivation layer, leading to an improvement by 1–2% for the absolute conversion efficiency. The concept of PERC was first proposed by Blakers et al.,[1] in 1989. The advantages of this solar cell are mainly profiting from the development and utilization of a series of technologies, e.g., double-sided silicon nitride (SiN_x:H),[2,3] stack layer passivation films,[4,5] back contact optimization,[6,7] and selective emitter (SE).[8] Especially, Hoex et al.,[9] used atomic layer deposition to prepare the back film of aluminum oxide (Al_2O_3) with superior passivation, which significantly promotes the industrialization of PERC solar cells. By the end of 2019, the PERC production capacity had exceeded 100 GW per year (GWp) in China.[10] The average efficiency of mass production for Czochralski (Cz) c-Si PERC solar cells has been increased from 20% in 2014 to over 22% in 2019.[11] LONGi Solar has recently declared the realization of world-record efficiency of 24.1% for industrial-grade PERC solar cells, providing a boost to the PV industry.[12] However, it should be noted that as the PERC cell efficiency increases, especially beyond 22.5%, the front surface passivation that was not a major impact becomes increasingly important. A detailed electrical and optical loss analysis of PERC with cell efficiency of 22%[13,14] had demonstrated that the loss mainly occurred in the homogenous and selective-diffused regions of the emitter. This implies that the advantages of further improvement for PERC cell efficiency cannot be fully harvested if only SE technique is used on the front surface of c-Si solar cells.

One promising solution is to introduce the recently popular tunnel oxide passivated contact (TOPCon) technology. TOPCon structure consists of ultrathin silicon oxide (SiO_2) and doped polysilicon (poly-Si), which has the superiority of full-area passivation contact and compatibility with high-temperature sintering process of PERC cell production lines. At present,

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssr.202000455.

DOI: 10.1002/pssr.202000455

a lot of encouraging research results have been made on TOPCon solar cells, e.g., the laboratory efficiency of 25.7% at Fraunhofer ISE (TOPCon alone)[15] and 26.1% at ISFH (a POLO structure similar to TOPCon combining with interdigitated back contact),[16] as well as the industrialization efficiency of 24.6% at Trina Solar (called i-TOPCon).[17] We have also done some meaningful work on adopting TOPCon to passivated emitter and rear totally diffused (PERT) bifacial c-Si solar cells for high passivation.[18] Nevertheless, most of the achievements related to TOPCon are made from *n*-type c-Si substrate with the stack structure usually used for BSF. The present PV industry reality is that the production capacity of *n*-type c-Si solar cells is less than 5 GWp,[19] far lower than that of PERC solar cells (>100 GWp) based on *p*-type c-Si substrate. Several scientific research institutions have began to explore the application of TOPCon on *p*-type substrate, demonstrating the potential for high cell efficiency of combining TOPCon with *p*-type c-Si solar cells, e.g., improved blue response with a semicrystalline emitter,[20] dependence of surface passivation on carrier transport of front surface field,[21] and excellent passivation based on physical vapor deposition of TOPCon.[22] However, the TOPCon structure in these solar cells was either still at back side or on a planar c-Si substrate. As we know, the passivation property of TOPCon is very sensitive to textured surface,[23] and parasitic absorption inside poly-Si also seriously affects the extensive application of TOPCon at the front side of solar cells.[23,24] Preparation of high-performance TOPCon on the front textured surface of *p*-type substrate has significant academic and industrial value for further development of high-efficient c-Si PERC solar cells, since so far, conversion efficiency for such solar cells are still less than 20%.[20,25,26]

In this work, we studied in detail about the photoelectric characteristic of front textured TOPCon and related structures on solar-grade *p*-type c-Si wafers, where the front surface was immersed in alkaline solution to form the compact, small-size, randomly arranged pyramids (see Figure S1, Supporting Information). The textured ultrathin SiO_2 was grown with thermal oxidation and intrinsic poly-Si contact layer was then deposited through thermal decomposition of silane based on the same low-pressure chemical vapor deposition (LPCVD) tube furnace with short intervals to avoid the natural oxidation of cell precursor. We focused on the influence of drive-in temperature and drive-in time on passivation of poly-Si, as they determine the crystalline structures i.e., co-existence for poly-Si and hydrogenated amorphous silicon (a-Si:H) as well as doping conditions of poly-Si materials. We achieved a champion efficiency of 21.3% on large-area (244.3 cm^2) *p*-Si PERC solar cells with a full-area passivation contact of front poly-Si. The proposed cell technology is fully compatible with existing PERC production lines without the need for additional laser selective redoping step. We finally expected an effective improvement through theoretical calculation with the PERC cell efficiency reaching up to 23.4%.

As starting materials, we employed solar-grade (100)-oriented *p*-type Cz c-Si wafers (244.3 cm^2) with a thickness of 180 μm and a resistivity of 1 Ω cm. **Figure 1**a,b shows the schematic structure and main production process, respectively, used to manufacture 5-busbar PERC solar cells combining with front poly-Si-based passivating contacts.

Fabrication of PERC Solar Cells with Front Poly-Si-Based Passivating Contacts: The c-Si wafers were first immersed in alkaline solution (KOH of 3% by volume for 420 s) to create the random pyramids after saw damage removal of ≈5 μm $side^{-1}$ (KOH of 4% by volume for 150 s). Hydrochloric acid (HCl) and hydrofluoric acid (HF) immersion were necessary to strip the metal ion and oxide layer, respectively. Front poly-Si-based passivating contacts structure was prepared by tubular LPCVD. The front textured insulating SiO_2 was first grown in 580 °C for 10 min based on thermal oxidation, and then the intrinsic poly-Si was deposited in 610 °C for 3, 5, and 15 min through thermal decomposition of silane. A liquid phosphorus oxychloride ($POCl_3$) diffusion was carried out to dope the intrinsic poly-Si into n^{++} emitter (for comparison of PERC solar cell, front homogeneous n^+ emitter was just formed in a $POCl_3$ diffusion tube with a sheet resistance of 130 Ω $\square^{-1}$ without SiO_2/poly-Si structure). Rear polishing and edge isolation treatment were implemented to resolve the diffraction coating issue caused by tube LPCVD together with the phosphorosilicate glass (PSG) removal. For the back side, solar cells with a full-area Al layer atop Al_2O_3 and SiN_x:H stack films were deposited with plasma-enhanced chemical vapor deposition (PECVD) of MAiA tools. Al_2O_3 film

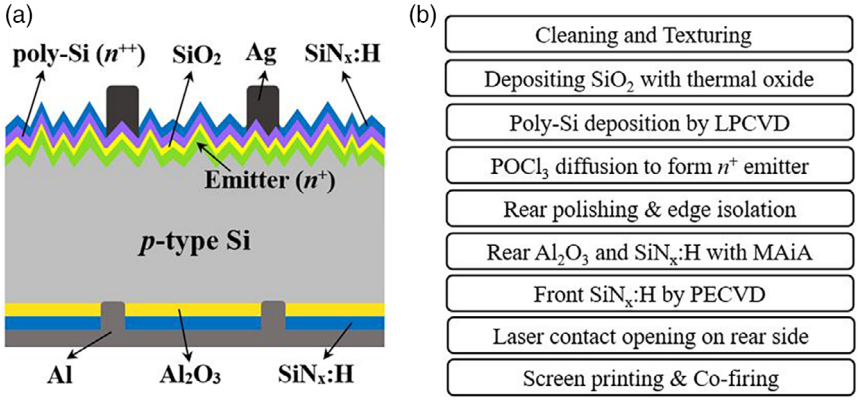


Figure 1. a) Schematic diagram and b) main fabrication process of *p*-type c-Si PERC solar cells with front poly-Si-based passivating contacts. The solar cells featuring a front phosphorus diffused emitter passivated by SiO_2/poly-Si stack and SiN_x:H antireflective coating using LPCVD and PECVD, respectively, together with a rear Al_2O_3/SiN_x:H passivating layers deposited with PECVD of MAiA tools.

possesses the fixed thickness of ≈10 nm, covered by thicker SiN_x:H of ≈150 nm for better passivation and rear surface reflection. The front emitter was passivated with 75 nm SiN_x:H antireflective coating. Finally, laser opening step was guaranteed for metal–semiconductor contact. Front Ag with single printing of 5-busbar and rear Al electrode were used by screen-printed metallization, together with a cofiring in an infrared belt-furnace.

Simulation by Wafer Ray Tracer and AFORS-HET v2.5: To further understand the influence of front texturing structure and covering films on the reflection and absorption characteristics of incident photons, we used the silicon solar cell numerical software Wafer Ray Tracer (Version 1.64)[27] to perform the detailed reflection loss due to random or regular small size-textured surface based on the recombination models of radiative, Shockley–Read–Hall, Auger, and surface recombination through combining Monte Carlo ray tracing with thin-film optics. Another numerical simulation tool of AFORS-HET v2.5[18,28] developed by Helmholtz-Zentrum Berlin is suited to deal with ultrathin dielectric layers of, e.g., SiO_2 and a-Si:H featuring two carrier transportation mechanisms of the thermionic-emission and thermionic field model and the heterointerface quantum tunneling model. The SiN_x:H/poly-Si(n^{++}) stacks were modeled as MS-Schottky contacts, together with flat band of metal work function being set in the back contact boundary. We emphasized further that the input parameters were from the experimental data, including 1 Ω cm *p*-type bulk resistivity, an industrially feasible wafer thickness of 170 μm, the aspect ratio of a pyramid of 0.7 with average height of 1.4 μm, the peak substitutional dopant concentration of 6.4×10^{19}cm^3 and front SiN_x:H thickness of 75 nm with "PECVD 2.13 [Vog15]" model. **Table 1** shows the main input parameter values in the Wafer Ray Tracer and AFORS-HET v2.5 simulations.

Characterization Methods of Solar Cells and Cell Precursors: The thickness of poly-Si, Al_2O_3, and SiN_x:H layers were extracted from spectroscopic ellipsometry. The sheet resistance was determined by four-point probes. The external quantum efficiency (EQE) and total reflectance (*R*) were received on the platform of quantum efficiency measurement. The electrical properties (open-circuit voltage V_{OC}, short-circuit current I_{SC}, fill factor *FF*, and conversion efficiency *Eff*) of c-Si solar cells were measured under standard test condition with a steady-state solar cell *I*–*V* tester equipped with a class AAA solar simulator. The effective minority carrier lifetime (τ_{eff}) and implied-V_{OC} of the cell precursors were obtained by quasi-steady-state photoconductance (QSSPC) method in the transient or generalized mode. Thickness of SiO_2 and poly-Si layer could be obtained by spectroscopic ellipsometry from the samples deposited on polished c-Si wafers or by transmission electron microscopy. The Raman spectral intensity was measured by a Raman spectrometer with excitation at 325 nm by an argon-ion laser.

It is one of the challenges to prepare high-quality textured ultrathin SiO_2 layer on an industrial large-area silicon wafer. We therefore need to conduct a clear observation to the integrity and uniformity of silicon oxide grown between c-Si substrate and poly-Si. Since Fraunhofer ISE applied wet-chemical method to TOPCon fabrication,[29] a wide range of techniques were gradually generated to prepare tunneling oxides, such as thermal oxidation, plasma-assisted oxidation, wet-chemical hydrochloric acid oxidation, wet-chemical nitric acid oxidation, and ultraviolet/ozone anodization.[17,30] The most commercially promising thermal oxidation method was selected herein based on our LPCVD tools because it is not easy to control the oxide layer thickness using wet-chemistry technique, due to the formation of native oxide that could increase the thickness to >2 nm before the wafer is subjected to poly-Si deposition.[31,32] **Figure 2**a,b shows the relatively low and high resolution of transmission electron microscopy (TEM) cross-section images for SiO_2 grown by LPCVD at 580 °C for 10 min with thermal oxidation, and poly-Si deposited at 610 °C with thermal decomposition of silane together with a treatment of high temperature annealing at 780 °C (without silane). It is clear that the SiO_2/poly-Si stack deposition were compact and uniform for the SiO_2 thickness of ≈1.5 nm. The sheet resistance uniformity of full-area poly-Si after doping is controlled within 5%.

Table 1. The main input parameter values for the wafer ray tracer and AFORS-HET v2.5 simulations.

Wafer ray tracer	Unit	Value	AFORS-HET v2.5	Unit	Value
Spectrum of incidence		AM1.5 g [Gue95]	Wafer thickness	μm	170
Front side morphology		Upright pyramids	Background dopant		Boron
Periodicity		Random/Regular	Resistivity ρ	Ω cm	1
Height/weight	μm	1.41/2.00	Bulk density of state N_{tr}	cm^{-3} eV^{-1}	8×10^9
Rear side morphology		Planar	Front contact boundary		Standard Si <111> pyramids
Front SiN_x:H thickness	nm	75; PECVD 2.13 [Vog15]	Schottky front interface S_{eff}	cm s^{-1}	10
Front poly-Si thickness	nm	25 (0–160); Crystalline, 300 K [Gre08]	Poly-Si density of state N_{tr}	cm^{-3} eV^{-1}	2×10^{11}
Front a-Si:H thickness	nm	5 (0–20); Amorphous [Pal85d]	Insulator SiO_2		Thermionic emission
Front SiO_2 thickness	nm	1.5 (0.4–2.2); Thermal [Pal85e]	Electron affinity *chi*	eV	1
Rear Al_2O_3 thickness	nm	10; ALD on Si [Kim97]	Energy band	eV	8.9
Rear SiN_x:H thickness	nm	150; PECVD [Bak11]	Pinhole density D_{ph}	[0...1]	1×10^{-8}
Number of rays per run		5000	Density of interfacial states D_{it}	cm^{-2} eV^{-1}	2×10^{10}
			Schottky rear interface S_{eff}	cm s^{-1}	1×10^5

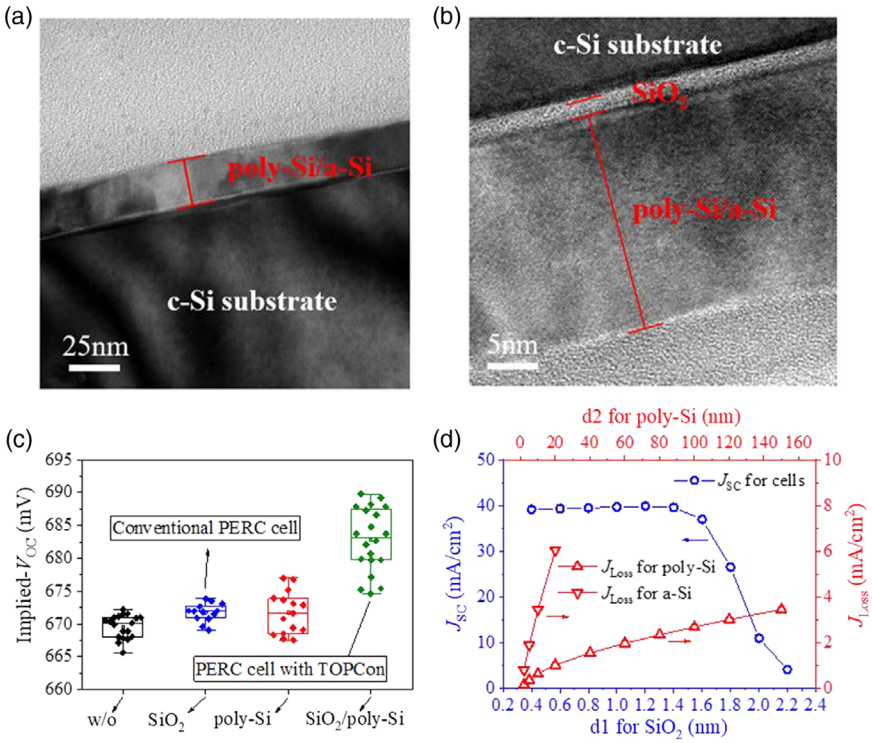


Figure 2. a,b) Relatively low-resolution (a) and high-resolution (b) TEM cross-section images for ultrathin SiO_2 layer grown by LPCVD at 580 °C with thermal oxidation, and poly-Si layer deposited at 610 °C with thermal decomposition of silane, together with appropriate annealing treatment. c) Statistical diagram of implied-V_{OC} of cell precursors with three different passivating structures. Note that all test samples are covered with SiN_x:H film. SiO_2/SiN_x:H stack can subsequently prepare the traditional PERC solar cell, while TOPCon/SiN_x:H stack for the new PERC. d) Calculated electrical parameters of J_{SC} (blue curve) versus the tunneling SiO_2 thickness d1, and current density loss J_{Loss} (red curves) absorbed inside impure poly-Si thickness d2, with the lower triangle curve for only a-Si:H absorption and the upper triangle one only poly-Si absorption.

To test the passivation effect of SiO_2/poly-Si stack, we show in Figure 2c, the statistical diagram of implied-V_{OC} of cell precursors with three different passivating structures. Just SiO_2 or poly-Si passivated c-Si wafers (the process here is the same as that of the corresponding TOPCon structure) yielded the mean implied-V_{OC} of 672 mV, whereas c-Si wafers covered with SiO_2/poly-Si stack improved the implied-V_{OC} to 683 mV. Noted that the reference group had only SiN_x:H covering film. The main reason is that the absence of SiO_2 or poly-Si leads to an increase for the saturation current density, and the SiO_2 layer needed for passivation does not restrain majority charge carrier transport across its barrier.[33] Passivation of only SiO_2 or poly-Si is similar to that of the reference group. Perhaps thickness of the materials may not be enough to fully demonstrate the advantages and disadvantages of passivation. We had further simulated in Figure 2d that the dependence of SiO_2 and poly-Si thickness on the electrical performance of solar cells using AFORS-HET v2.5 and Wafer Ray Tracer software, respectively. Note that LPCVD tools deposit imperfectly crystallized poly-Si, including a-Si:H. Here we separate the impure poly-Si into two separate materials to determine film absorption loss in simulation. Ultrathin SiO_2 has a threshold thickness, e.g., 1.4–1.6 nm beyond which the J_{SC} rapidly decreases because of the weakened carrier tunneling effect.[34] Our realization of ≈1.5 nm SiO_2 layer establishes the successful base for the front poly-Si-based passivating contact *p*-type Si solar cells. Front poly-Si layer thickness was fixed at ≈25 nm for SiO_2 simulation. SiO_2 thickness was fixed at 1.5 nm for poly-Si simulation. Moreover, the current density loss (J_{Loss}) inside a-Si:H and poly-Si both increases versus the silicon layer thickness due to the photon parasitic absorption in films. The J_{Loss} from 60 nm poly-Si was ≈2 mA cm^{-2}, which was the same as the loss from just 5 nm thick of a-Si:H layer.

Formation of a good passivated contact requires not only the tunneling SiO_2 layer but also a properly doped poly-Si. Although the impurity can be blocked by SiO_2 when P diffusing in poly-Si, it is not complete, so the doping distribution optimized from e.g., drive-in temperature and drive-in time plays an important role in improving interfacial passivation as well as carrier collection. **Figure 3**a,b shows the statistical diagram of passivation effect of poly-Si/SiO_2/c-Si stack with double-sided symmetric structure for the poly-Si deposition time of 5 min versus the drive-in temperature after pre-deposition of phosphorus-dopant. Pre-deposition results in a thin but highly concentrated impurity layer that establishes a concentration gradient for the entire diffusion and is therefore a constant surface source diffusion process. This poly-Si thickness measured by spectroscopic ellipsometry from the sample deposited on polished c-Si wafers covered with SiN_x:H film was about 25 nm. It can be seen that the mean implied-V_{OC} after sintering was 15–25 mV higher than that before sintering because of the activation of hydrogen passivation. Moreover, the decrease in drive-in temperature would increase the effective minority lifetime τ_{eff} and implied-V_{OC} in

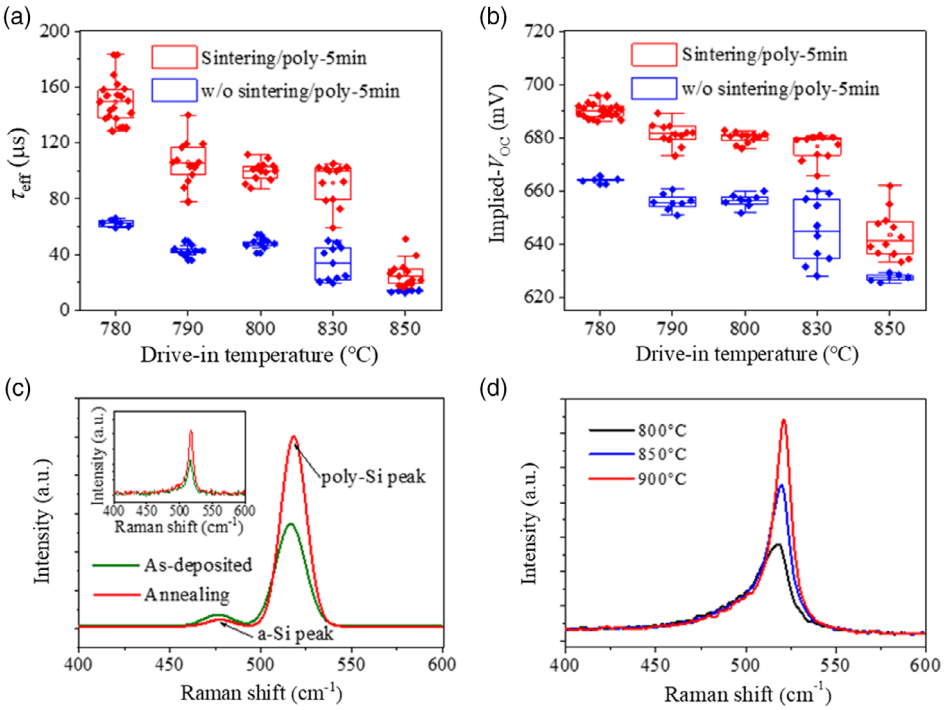


Figure 3. a,b) Statistical diagrams of effective minority lifetime τ_{eff} (a) and implied-V_{OC} (b) of poly-Si/SiO_2/c-Si stack structures with 5 min for poly-Si deposition time as a function of drive-in temperature from 780 to 850 °C. c) Raman spectra of as-deposited a-Si:H layer on quartz glass substrate measured using ultraviolet lasers with the wavelength of 325 nm before and after annealing. Annealing temperature was set to 780 °C. The original Raman spectrum tested, containing both a-Si:H and poly-Si information, is shown in the inset. d) Effect of three different annealing temperatures on Raman spectra of a-Si:H layer on quartz glass substrate.

the range of 780–850 °C. As the temperature rises, more phosphorus diffuses across the SiO_2 layer into the silicon substrate, resulting in a higher recombination current J_0 due to the decreasing field effect passivation. Average implied-V_{OC} after sintering increased from 643 mV at 850 °C to 690 mV at 780 °C.

Figure 3c shows the Raman spectra of as-deposited a-Si:H using 325 nm laser before and after annealing with the fixed annealing temperature of 780 °C. Note that the drive-in temperature and annealing temperature are related in the diffusion process. The ultraviolet laser with 325 nm wavelength has a detection depth of only 10 nm in the a-Si:H, while it can reach deeper in c-Si and poly-Si films. Based on this, we prepared thicker a-Si:H layers with the deposition time of 20 min on quartz glass to avoid other interference signals. The results in Figure 3c clearly shows the Raman shift of ≈480 cm^{-1} for a-Si:H and 520 cm^{-1} for poly-Si after peaks separation, together with the crystallization of amorphous Si increased after annealing. Shown in the inset is the original Raman spectrum tested containing both a-Si:H and poly-Si information. The crystallization was also subjected to different annealing temperatures, as shown in Figure 3d. This observation also revealed that the drive-in temperature should not be too low. As we know, the absorption coefficient of a-Si:H is much higher than that of poly-Si at the wavelength of 400–700 nm. Reiter et al.,[35] have demonstrated that the J_{SC} loss caused by 20 nm doped a-Si:H is ≈2.5 mA cm^{-2} higher than that of doped poly-Si with the same thickness through ray tracing method. Parasitic absorption loss of poly-Si-based passivating contact materials was severe at low temperatures due to the presence of a large proportion of a-Si:H. Our experiment proved that the optimized drive-in temperature was 780 °C as it can not only fully activate the advantage of interfacial hydrogen passivation but also avoid serious absorption loss.

Figure 4a shows the statistical diagram of implied-V_{OC} of poly-Si/SiO_2/c-Si stack with double-sided symmetric structure for 3, 5, and 15 min poly-Si deposition time after conventional phosphorus diffusion from $POCl_3$ for the fixed drive-in temperature of 780 °C. The poly-Si of deposition time 5 min has the thickness of 25 nm, and the thickness is linear with the deposition time. The 15 min poly-Si layer is thicker than that of 5 min poly-Si, so the drive-in time is correspondingly lengthened. We could find that the appropriate drive-in time was also important, and implied-V_{OC} of over 690 mV was obtained for the drive-in time of 900 s in poly-Si of 5 min deposition time. For the less drive-in time, phosphorus atom diffusion in poly-Si is not sufficient. For longer drive-in time, more phosphorus atoms penetrate silicon oxide into c-Si substrate, reducing the insulating passivation effect caused by silicon oxide. Moreover, it is clear to see that the thinner 3 min poly-Si layer not only had inferior passivation than that of poly-Si with 5 min deposition but also is more sensitive to drive-in time. The solar cells with poly-Si deposition time of 15 min showed similar passivation compared with other groups, which could also be reflected in the comparison of V_{OC} between poly-Si 5 and 15 min in Figure 4b.

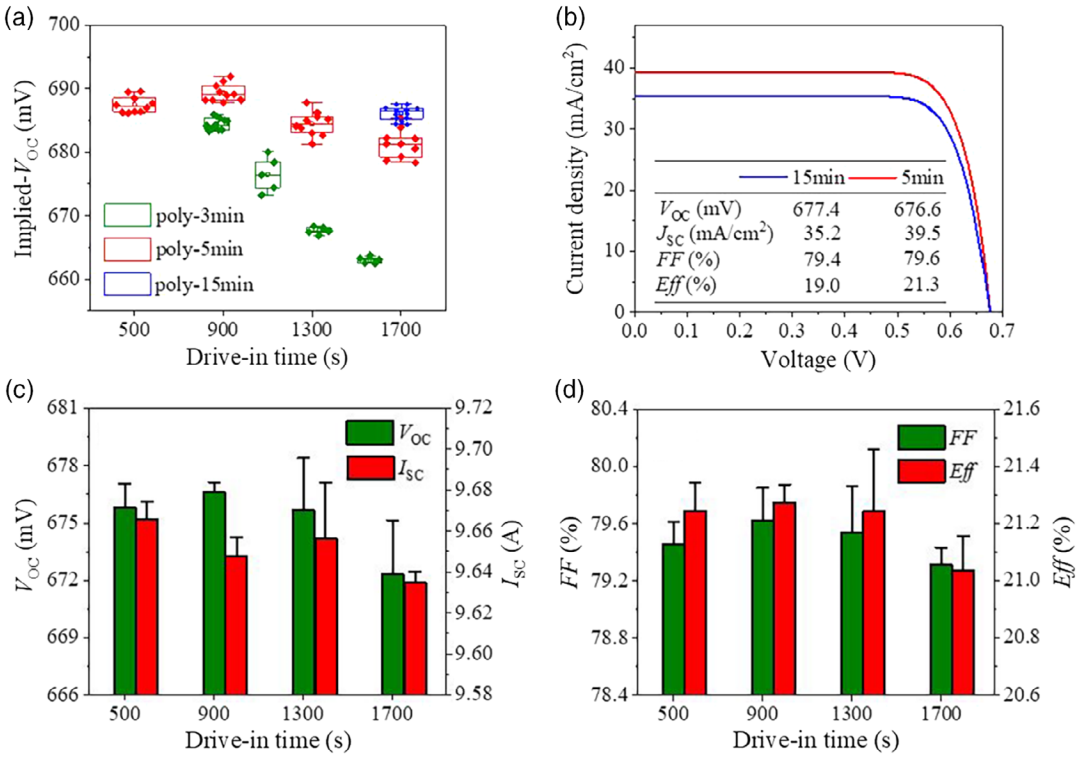
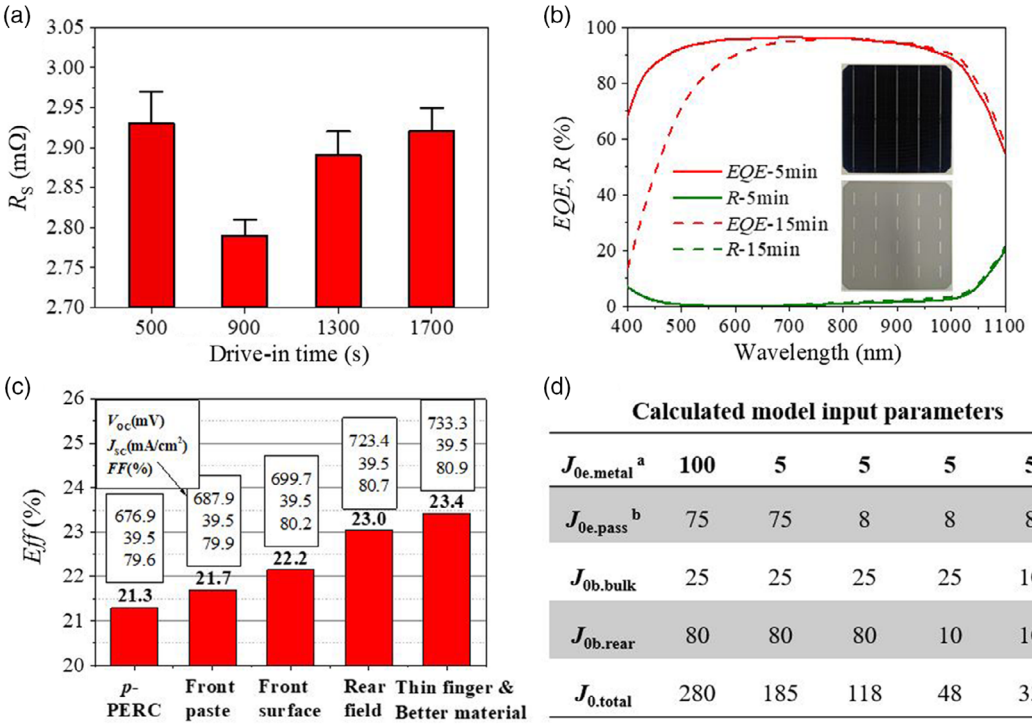


Figure 4. a) Implied-V_{OC} of poly-Si/SiO_2/c-Si stack structures with 3, 5, and 15 min for poly-Si deposition time as a function of drive-in time from 500 to 1700 s. The 15 min poly-Si layer is thicker than that of 5 min poly-Si, so the drive-in time is correspondingly lengthened. b) Comparison for the current–voltage curves between poly-Si of 5 min and 15 min deposition time. c,d) The electrical properties of V_{OC} and J_{SC} (c) and *FF* and *Eff* (d) for front poly-Si-based passivating contact solar cells with 5 min poly-Si deposition time for the same drive-in time. Note that the drive-in temperature was fixed to 780 °C. The pillars and top error bars in the bar graphs represent the mean and maximum values of those electrical parameters, respectively.

We had further investigated the influence of drive-in time of phosphorus diffusion in poly-Si on the electrical properties of solar cells. Double-sided symmetrically passivated samples and poly-Si-based passivating contact solar cells were prepared in the same process conditions using the same diffusion and deposition tube. Figure 4c,d shows the electrical properties (V_{OC}, I_{SC}, *FF*, and *Eff*) of poly-Si based passivating contact solar cells with 5 min poly-Si deposition time. The same variation trend for the conversion efficiency, *Eff*, in Figure 4d and implied-V_{OC} in Figure 4a could be clearly found featuring the optimal value of drive-in time of 900 s, which is also reflected in the test results of the series resistance R_s shown in **Figure 5**a. For the drive-in time of 900 s, R_s had the minimum value of 2.8 mΩ, resulting in the realization of average V_{OC} of 676.6 mV, I_{SC} of 9.6 A, *FF* of 79.6%, and *Eff* of 21.3% (traditional PERC with front TOPCon solar cells were compared in Table S1, Supporting Information). Figure 5b presented the comparison of external quantum efficiency EQE and reflectance *R* for the finished c-Si PERC solar cells with poly-Si deposition time of 5 and 15 min using the same condition in Figure 4b. Obviously, in the range of medium-short wavelength (<700 nm), the EQE of 15 min poly-Si was lower than that of 5 min poly-Si. Since thicker poly-Si does not cause a reduction in passivation performance as shown in Figure 4b, the lower EQE was mainly attributed to the parasitic absorption loss in impure poly-Si layer, resulting in the lower cell efficiency of equal to 19.0% as well as the J_{SC} of just 35.2 mA cm^{-2}. For poly-Si of 5 min, gratifying news lie in that the high EQE (over 90%) in the range of the medium-long wavelength (500–950 nm), which demonstrated the good carrier collection throughout the solar cells, including the electrical shading areas.[36]

Recombination current J_0 measured from double-sided symmetrically passivated sample with textured surfaces in our experiments only reflects the passivation properties of front surface emitter. The J_0 had the optimal value of ≈30 fA cm^{-2} for the drive-in time of 900 s (see Figure S2, Supporting Information), which still greatly exceeded that of symmetrical samples on *p*-type c-Si with rear TOPCon emitter of 3.1 fA cm^{-2} conducted by Fraunhofer ISE.[21] Also, during high temperature sintering, firing-through silver paste is easy to penetrate poly-Si layer and contact with c-Si substrate, increasing the J_0 value in the passivating contact area.[37,38] The investigation of front textured poly-Si based passivating contact *p*-type c-Si solar cells is at early stage. It is, therefore, necessary to analyze the carrier recombination loss in each part of the solar cell, so as to find an effective way to improve the cell efficiency. We employed the numerical simulation tool named Equivalent Circuit from PV Lighthouse.[39] Based on the initial experimental parameters of the front emitter recombination current caused by surface passivation $J_{0e,pass}$, light-collected current J_L, series



(d)

Calculated model input parameters

$J_{0e.metal}$ [a]	100	5	5	5	5
$J_{0e.pass}$ [b]	75	75	8	8	8
$J_{0b.bulk}$	25	25	25	25	10
$J_{0b.rear}$	80	80	80	10	10
$J_{0.total}$	280	185	118	48	33

Figure 5. a) Series resistance R_s versus drive-in time. The pillars and top error bars in the bar graphs represent the mean and maximum values. b) Comparison of EQE and R for the solar cells with poly-Si deposition time of 5 and 15 min. Photographs of the front and rear side of the c-Si PERC solar cell with 5-busbar for the cell efficiency of 21.3% conducted by screen printing, combining half-chip technology, are shown in the inset. c) Calculated cell efficiency improvements from 21.3% to 23.4% for p-PERC silicon solar cells with front poly-Si based passivating contacts versus the decreased J_0 values on both sides, together with d) the important model input parameters listed for comparison. $J_{0.total} = J_{0e} + J_{0b}$, where $J_{0e} = J_{0e.metal} + J_{0e.pass}$ and $J_{0b} = J_{0b.bulk} + J_{0b.rear}$. In the table, the footnotes (a) and (b) are indicated as follows: [a]All the J_0 values are in units of fA cm^{-2}; $J_{0e.metal}$ means the J_0 value for front emitter caused by metal electrodes; [b]The word "pass" is short for passivation; J_{0b} means the J_0 value for base region of solar cells.

resistance R_s, and shunt resistance R_{sh}, we show in Figure 5c that the simulated electrical properties of the p-type c-Si PERC solar cells, together with all the important model input parameters listed for comparison in Figure 5d.

We started from the solar cell efficiency of 21.3% ($V_{OC} = 676.9$ mV, $J_{SC} = 39.5$ mA cm^{-2}, $FF = 79.6\%$), closing to the average experimental result of 21.3% for the best drive-in time of 900 s (see Figure 4d). As shown in Figure 5d, the total J_0 of solar cells, named $J_{0.total}$, was divided into four parts including $J_{0e.pass}$, front emitter recombination current caused by metal electrode $J_{0e.metal}$, J_0 value caused by bulk recombination in base region $J_{0b.bulk}$, and the back recombination current caused by passivation and metallization $J_{0b.rear}$. This classification standard has been demonstrated by modeling a reference cell with TOPCon stack from Fraunhofer Institute, which was then extended to assess the efficiency potential of large area TOPCon cells on commercial grade Cz Si material with screen-printed contacts.[40] Taking advantage of the technology available including the increase in surface concentration and junction depth of emitter doping, constriction of front finger width, and improvement of paste composition as well as sintering has the capacity to keep the electrode forming good ohmic contact.[41] The $J_{0e.metal}$ value was expected to decrease from 100 to 5 fA cm^{-2}, resulting in an absolute increase in cell efficiency of 0.4% to 21.7%. SiO_2 layer can be further optimized such as reducing the density of interface state, adjusting oxygen content to increase the energy gap, and optimizing the film thickness and compactness to enhance the field effect and chemical passivation.[18,40] Improvement of cell efficiency to 22.2% is calculated due to the decrease of $J_{0e.pass}$ from 75 to 8 fA cm^{-2}. Furthermore, using local boron doping, better back electrode paste, less front electrode shading, and better substrate material such as increase in resistivity and bulk lifetime,[40] the optimized solar cell can be realized with the efficiency increased to 23.4% based on the decrease of $J_{0.total}$ from 118 to 33 fA cm^{-2}. From the listed solar cell electrical parameters in Figure 5c, the enhancement in cell efficiency is mainly profited from the improved V_{OC}.

In summary, we have investigated both experimentally and theoretically the application of full-area poly-Si based passivating contacts on front textured p-type c-Si PERC solar cells. The random textured surface prepared by alkali solution exhibited an excellent anti-reflectance of less than 2%. The passivation quality of SiO_2/poly-Si stack grown with low-cost thermal oxidation and LPCVD technology in the same tube furnace has been evaluated from the implied-V_{OC} and minority carrier lifetime τ_{eff} of solar cell precursors. The relatively higher passivation of implied-V_{OC} of over 690 mV could be obtained by optimizing drive-in temperature and drive-in time of phosphorus dopants inside poly-Si. Poly-Si with a

deposition time of 5 min (≈25 nm thick) is a better choice since greater thickness can lead to severe photonic parasitic absorption. The large-area (244.3 cm^2) *p*-PERC c-Si solar cells yielding top efficiency of 21.3% was successfully achieved without the need for additional laser selective redoping. Theoretical analysis was finally conducted to further understand the recombination current loss in each part of the c-Si PERC solar cells. The optimized cell efficiency could be expected to increase to 23.4% with the total J_0 decreased from 280 to 33 fA cm^{-2} through optimizing the surface passivation, metal paste and substrate material. This work has demonstrated that front textured SiO_2/poly-Si stack has a good full-area passivation effect for further improvement of *p*-type c-Si PERC solar cells. More important is that the passivating contact technology is compatible with the current PERC production lines, which has a good commercial prospect.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Major State Basic Research Development Program of China (2018YFB1500501 and 2018YFB1500302), National Natural Science Foundation of China (11974242, 11834011, and 11674225).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

cell efficiency, *p*-PERC, solar cells, textured passivating contacts

Received: September 19, 2020
Revised: November 8, 2020
Published online:

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