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Schottky Barrier Height reduction using strained silicon-on-insulator and dopant segregation

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ABSTRACT

Schottky Barrier Height (SBH) lowering at the source/drain contacts appears as an inescapable requirement for CMOS downscaling in the sub-20 nm regime that legitimates metallic source/drain technology as a relevant solution. For that sake, we have developed a test structure which enables the extraction of the effective SBH by the combination of experimental data to a transport model taking into account thermionic and tunnel emission. In this study, we demonstrate the compatibility and the cumulative effects of two SBH lowering techniques: dopant segregation integration and wafer-based biaxial tensile strain.

1. Introduction

Schottky Barrier contacts have been identified as a potential candidate in replacement to the conventional ohmic source/drain (S/D) module. The evolutionary purpose is the replacement of the conventional resistance components by a metallic layer, which decreases the series resistance needed for increased speed and current drive capabilities. Many substantial advantages are associated to this technology: (i) less critical interplay between S/D doping and silicidation, (ii) low sheet resistance of metal alloy and (iii) relatively abrupt junction profile due to the absence of dopant spreading [1]. However, this technology is also subject to some weaknesses as the strong dependence of the specific contact resistance with the SBH and the need for two different silicides for contacting regions with both polarity types. In brief, the viability of this technology is strongly correlated to the SBH which is difficult to lower because of the Fermi level pinning. Several approaches for mitigating the pinning effect have been explored but band structure engineering appears to be the most promising. This method consists in modifying the energy difference between one of the silicon band-edge and the silicide Fermi level. The energy shift can be induced locally by dopant segregation (DS) at the silicon/silicide interface and more judiciously by the introduction of strain in silicon which is known to break degeneracy at the conduction and valence band minima. In that context, the objective of the present study is to assess the impact of the two aforementioned SBH lowering methods. For that sake, a test structure composed of two back-to-back diodes is proposed to characterize platinum silicide SBH on strained and unstrained substrates. As platinum silicide is known to have a high work function, leading to a low Schottky barrier to hole, its integration is convenient for the study of valence sub-bands evolution. Moreover, the compatibility of tensile strain application with boron dopant segregation (B-DS) is analyzed to determine whether the two advantageous contributions are cumulative. However, p-type B-DS does not give access to conduction sub-bands evolution with respect to tensile strain application. For that reason, arsenic dopant segregation (As-DS) is also used to tune the SBH in order to convert platinum silicide into n-type contacts and give access to the desired information.

2. Schottky Barrier lowering techniques

Strain is commonly known to enhance carrier mobility because of its impact on the effective mass and on scattering mechanisms. Another effect associated to strain application is to break degeneracy between the light and heavy hold sub-bands and at conduction band minimum, as well. Sub-bands degeneracy can be explained by the alteration of the semiconductor crystal symmetry [2] that, in turn, induces band splitting. As the SBH is related to the position of the metal Fermi level with respect to the closest silicon band edge, its value is also expected to be altered by strain application. However, strain-induced sub-bands variation is dependent on strain type, i.e. compressive or tensile, direction and intensity. The two main approaches that induce strain in the transistor channel, i.e. process induced strain and wafer-based global strain, can be distinguished by their integration complexity, costs and type. Wafer-based biaxial tensile strain is obtained by silicon epitaxial growth onto a relaxed SiGe buffer layer previously grown on a silicon substrate. The main effect of strain is to shift the Δ_2 and Δ_4 bands differently (downward and upward respectively) and thus change the energy splitting between them. The valence sub-band

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set, i.e. heavy hole (HH), light hole (LH) and Split off (SO) valence sub-bands, follows a similar behavior with respect to biaxial tensile strain increase. Degenerated HH and LH valence sub-bands splits up under tensile strain whereas SO sub-band and the average valence position decrease (Fig. 1). As a conclusion, strained-induced silicon sub-band splitting is a relevant technique for SBH lowering. In order to further reduce contact resistivity at the silicide/silicon interface, the DS approach provides an additional leverage to modulate the SBH. This concept consists in introducing acceptor (or donor) type species near the valence band (or conduction band) [3]. The introduction of a highly localized dopant sheet at the vicinity of the silicide/silicon interface results in the formation of an interface dipole that modifies the shape of the band structure. For instance, boron dopant segregation (B-DS) results in the substitution of Si atoms by B atoms at the vicinity of the PtSi/silicon interface (Fig. 2a). As B atoms are expected to be ionized and negatively charged, a charge transfer takes place, leading to the rise of a positively charged layer on the metallic side and the creation of a dipole directed from the silicon to the silicide [4]. The induced band bending only slightly lowers the SBH but mainly reduces the barrier width. The mechanism behind contact resistance reduction is therefore associated to enhanced carrier tunneling. From the modeling standpoint, enhanced injection can also be viewed as a reduction of the effective SBH. The impact of arsenic dopant segregation (As-DS) is similar except that substitutional As atoms are positively charged. The dipole direction and the band bending are therefore inverted (Fig. 2b). Although a silicide like PtSi that presents a large SBH to electrons is theoretically not attractive for n-type contacts, its association to As segregation proves to be very efficient to render PtSi compatible with 0.1–0.2 eV effective SBH to electrons.

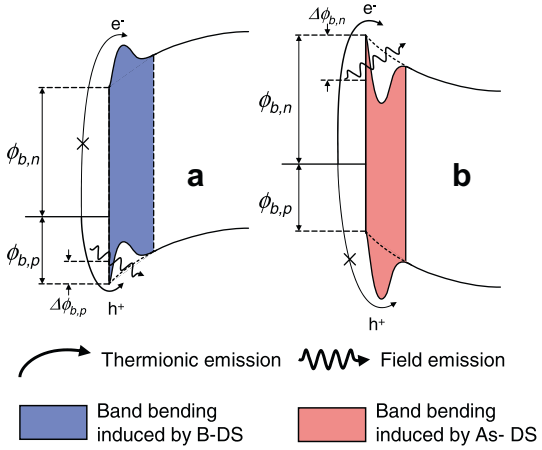

Fig. 2. Schematic representation of silicon bands at the vicinity of a PtSi/Si interface on a lightly p-doped substrate with: B-DS (a) and As-DS (b).

3. Experimental procedures

The objective of this section is to quantify the SBH reduction under well controlled conditions to unambiguously identify contributions associated to each technique, namely, DS or strain application. For that sake, back-to-back test structures especially well suited to SBH measurements [5] on ultra-thin film have been implemented on tensile strained SOI (sSOI). Dopant segregation was introduced in the so-called ITS (Implant-to-Silicide) flavor making use of p-type (B) and n-type (As) impurities [6]. An additional unstrained SOI was also processed and measured for a comparison purpose. In our experiments, we used unstrained (100) SOI wafer with a 18 nm thick p-type Si layer and (100) sSOI wafers with two stress levels. The strained Si layer seats directly on the buried oxide and the strain level corresponds to $Si_{1-x}Ge_x$ buffer layers with a Ge fraction of $x = 0.2$ and 0.4 and a 13 and 9 nm thick silicon on insulator layer respectively. The dedicated test structures consisted in $1000 \times 1000\ \mu m^2$ square-shaped silicided contacts separated by a 500 nm gap of silicon to produce back-to-back junctions. The active zone of the back-to-back diodes was structured by e-beam lithography using PMMA positive resist and SF_6/N_2 RIE etching step, creating a trench down to the buried oxide. A protecting layer of 300 nm was defined with a negative tone resist HSQ, densified by rapid thermal annealing. The $0.5 \times 1000\ \mu m^2$ silicon channel region is therefore protected from the silicidation process. Prior to the deposition of a 6 nm thick Pt overlayer, substrates were dipped into HF 1% and subjected to a slight Ar^+ plasma etch at 150 eV to remove residual oxide. The wafers were subsequently transferred to a RTA system and the formation of PtSi was thermally activated in forming gas (N_2:H_2 – 95:5) for 2 min at 500 °C. Unreacted Pt was selectively removed using a sacrificial germanidation technique [7]. B-DS and As-DS were implemented on each of the three substrate types. Boron and Arsenic atoms were implanted without tilt at 17 and 15 keV, respectively, and a common dose of 10^{15} atoms/cm^2. The post-silicidation thermal anneal was conducted at 600 °C for 5 min in forming gas. These doping steps were performed directly into PtSi after the selective etch of Pt over PtSi (ITS scheme [6]). In summary,

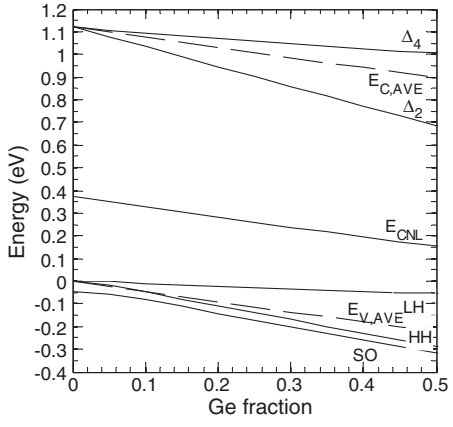

Fig. 1. Variation of silicon sub-band energies and E_{CNL} of a $Si/Si_{1-x}Ge_x$ heterostructure as a function of Ge fraction x. $E_{C,ave}$ is the average level of the conduction band. $E_{V,ave}$ is average level of the valence band.

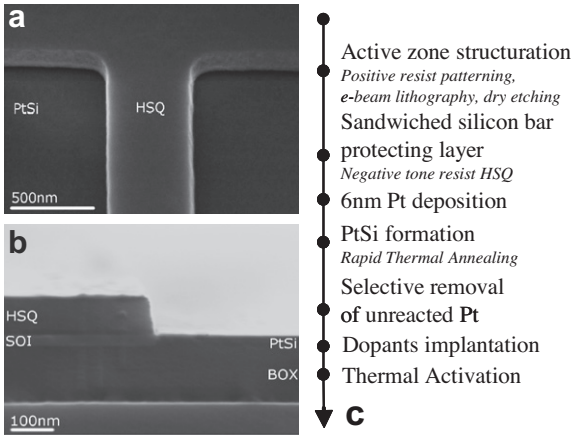

Fig. 3. Aerial (a) and cross section (b) SEM view of back-to-back diodes on SOI substrate. Schematic process flow (c) of its integration.

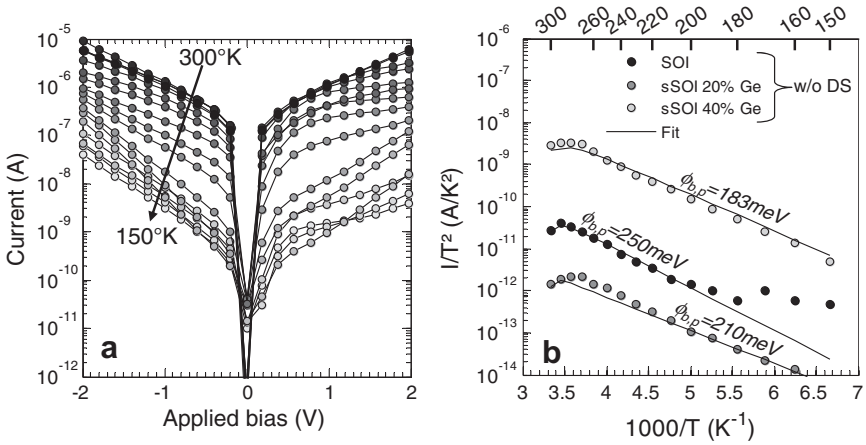

Fig. 4. (a) Experimental I–V–T @ V_{BG} = 0 V of back-to-back Schottky diode using PtSi silicide on an unstrained SOI substrate. (b) Experimental and calculated Arrhenius plot of unstrained SOI, sSOI 20% Ge and sSOI 40% Ge w/o DS @ V_{BG} = 0 V and V = 1 V.

Table 1
Summary of SBH extracted from experimental data (meV).

	No DS $\varphi_{b,p}$	B ITS DS $\varphi_{b,p}$	As ITS DS $\varphi_{b,n}$
Unstrained SOI	250	125	270
sSOI 20% Ge	210	115	220
sSOI 40% Ge	183	105	160

back-to-back diodes were processed on unstrained and strained SOI (20% and 40% Ge fractions) with dopant segregation of p- and n-type (Fig. 3). The Schottky Barrier Heights were determined using a methodology combining experimental data and transport modeling [8]. Measured data consist in I–V curves measured at different temperatures from 300 to 150 K by step of 10 K. For each measurement, the backside substrate contact is used as a gate structure, which is biased from 0 to ±50 V by step of 5 V. Arrhenius plots (I/T^2 vs. 1000/T) are then extracted from these measurements (Fig. 4).

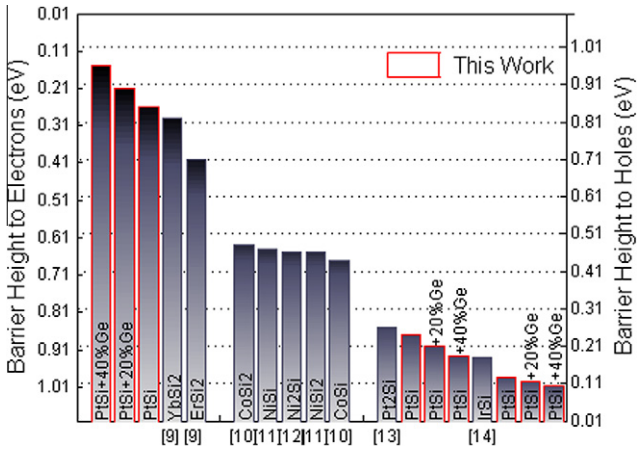

Fig. 5. Summary of SBHs extracted from this work and for other silicides [9–14].

4. Results and discussion

Table 1 presents SBH results extracted from devices previously described. These results show an obvious increase/decrease of the valence/conduction band which is in correlation with simulated band structures for $Si/Si_{1-X}Ge_X$ heterostructures. The reduction of the Schottky barrier to holes associated to strained silicon is 40 and 67 meV for strain introduced by SiGe buffer layers with 20% and 40% Ge content, respectively. This effect can be explained by the degeneracy break of the LH and HH valence sub-bands induced by the application of a gradual strain in the substrate plane. The impact of B-DS is different whether strain is introduced or not. Considering the unstrained case, SBH lowering induced by B-DS is equal to 125 meV. This result obviously shows that the thin p-dopant layer increases hole injection by activating tunneling through the junction. In the case of strained SOI, an additional SBH reduction associated to DS superimposes to the initial barrier lowering introduced by strain. This additional decrease amounts to 95 meV and 78 meV for sSOI with 20% Ge and 40% Ge content, respectively. This results in a cumulative reduction of the SBH to holes of 135 and 145 meV, respectively, with respect to the unstrained case. As previously discussed, DS of n-type dopants makes the extraction of effective $\varphi_{b,n}$ possible on unstrained and strained SOI. Therefore, SBHs extraction of As-DS samples represents the evolution of the conduction band minima as a function of strain. The stress related to the degeneracy break of the Δ_2 conduction valleys results in a barrier reduction of 50 and 110 meV for the 20% and 40% Ge content cases, respectively. However, the efficiency of As-DS as a function of strain increase is not assessable because $\varphi_{b,n}$ extraction on devices without DS cannot be measured as far as platinum silicide is used. Table I summarizes results extracted from experimental data and Fig. 5 compare them to other silicides.

5. Conclusion

This study was designed to determine whether the SBH is effectively further reduced when strain application is coupled to a DS technique. The results extracted from experiments suggest that these two techniques are efficient to lower the SBH on sSOI. In other words, the present work confirms that DS and strain applied from the substrate have cumulative effects. It is here confirmed that ITS-based arsenic and boron DS enables both p- and n-type as far as PtSi is concerned. Both $\varphi_{b,n}$ and $\varphi_{b,p}$ reduction are clearly related to the degeneracy break of the valence and conduction bands. This trend is in agreement with modeling results shown in Fig. 1. Nonetheless, even if the benefit is minor for boron-based DS, no degradation of current injection is observed.

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