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Detection of traps induced and activated by high field stress in an N-channel VDMOSFET transistor using current deep level transient spectroscopy (CDLTS)

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ABSTRACT

Commercial VDMOSFETs transistors were subjected to positive and negative high field stress. A new model of current deep level transient spectroscopy (CDLTS) characterization is adopted in a research of defects induced and activated by electrical stress. This model is based on pulse width scan instead of classical temperature scan. The band gap is scanned by varying the pulse base level. Positive and negative high field stresses were applied for different periods ranging from 30 to 120 min. After each stress period, activation energies and capture cross sections of detected traps were estimated. Different defects were detected and we have distinguished the doping levels and interface states from deep levels located in the forbidden band gap.

1. Introduction

Semiconductor crystals are of highest purity and quality, but they are not perfect. They contain some crystal defects such as interstitials (excess semiconductor atoms in the crystal lattice), vacancies (missing semiconductor atoms in the crystal lattice) and dislocations (imperfections in the crystal structure), as well as traces of impurity elements such as metallic atoms or oxygen. These defects and impurities give rise to permitted levels within the energy band gap. These levels exchange electrons with conduction and valence bands and are called "generation-recombination centers" or in short "recombination centers". The recombination of carriers takes place not only within the bulk of a semiconductor crystal, but at its surface as well. The surface is indeed a place where the periodicity of the crystal lattice is interrupted and where contact with another substance (SiO_2 in our studied devices) is made. The existence of deep levels has detrimental effects on the performance of the devices based on these semiconductors. Therefore, the investigation of their origin and properties plays a crucial role in improving the devices performance and quality [1,2].

Metal-oxide-semiconductor field effect transistor (MOSFET) structures play an important role in semiconductor technology. Measurement of deep level defects in these devices provides essential information for optimizing production processes and to predict device performance [3]. Capacitance deep level transient spectroscopy (DLTS) [4] on metal-oxide-semiconductor (MOS) capacitors and schottky diodes or pn junctions has received much attention in recent years and many papers have improved the original model or technique. Otherwise, very few works have focused on the development of models for the characterization of transistors by current DLTS even though this technique is known to be much more sensitive than the capacitance DLTS and allows measurements on small area and/or resistive samples [5–7]. The deep level transient spectroscopy (DLTS) has turned out to be a powerful method to analyze transient signals and to characterize deep level defects by determining their concentrations, their thermal energies and their capture section [8,9].

The DLTS method uses the difference between two points of the capacitance transient signal as a function of temperature. This difference is called a DLTS signal. The conventional current deep level transient spectroscopy (CDLTS) method is based on the difference between two points of the current transient signal at two different times (t_1, t_2) as a function of temperature. But in our work, the CDLTS signal is the difference between two points of the current transient as a function of the pulse width which eliminates temperature scanning or variation and enables faster measurements [10].

2. Experimental set-up

Studied devices were IRF540 N commercial N-channel VDMOSFET structures, manufactured by standard commercial processes and capsulated in a low cost TO220 plastic package. The drain–source breakdown voltage is 100 V and the maximum gate–source voltage is 20 V, the approximate oxide thickness is 100 nm. Electrical stressing was performed by applying a positive bias of

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44 V and a negative bias of −44 V to the gate electrode, with drain and source terminals grounded. This stress was assured by a step of 1 V/s until the maximum value is reached in order to prevent a sudden breakdown of the oxide. Different stress periods were applied going from 30 to 120 min with a step of 30 min. Stressing was stopped at various times and CDLTS characterization was performed. The measuring procedure will not induce any changes in the created defects since the measurement is completed at room temperature without any annealing.

In this work, we are going to adopt a different approach for the determination of the trap energy E_T. This method is based on a pulse width scan in order to determine the value (T_{max}) which gives the max CDLTS signal S_{max}. Then the pulse width is fixed at T_{max} and the pulse base level is varied to scan a large part of the energy gap searching for the location of the trap level. It is worth noting that the variation of the pulse base level is frequently used in charge pumping [11] and was also applied for the DLTS profiling of the interface traps in MIS diodes in a limited part of the band gap [12]. In our case the pulse base level allows us to scan a large part of the energy gap as minority carrier generation problems are absent in enhancement MOSFETs. Just like in classical CDLTS, deep levels are filled during the pulse and their emission characteristics are extracted from the transient analysis [13].

The measurements were performed by applying a drain to source voltage of 0.7 V to keep the drain in the linear regime, in order to have a more or less symmetric depleted region under the gate. The filling pulse voltage applied to the gate is of 4 V (in the strong inversion regime), with a frequency of 1 kHz while the pulse width has been varied from 40 to 3000 μs. Fig. 1 resumes the applied technique and shows the different experimental parameters.

A polarization of 4 V on the gate contact is a transition state between the weak inversion and the strong inversion regimes. For this polarization, bulk traps are no longer separable from interface traps which exhibit comparatively long time constant. As a result, the time variation of drain current is governed by the transient behaviors of interface states, which density greatly exceeds that of bulk traps.

3. Results and discussion

We have made use of the current dependent mobility model. The CDLTS signal is defined in unit of current by:

$$S = \mu_0 (Z/L) V_{ds} Q_{d0} \left(\frac{N_{tt}}{N_a}\right) [\exp(-t_1/\tau) - \exp(-t_2/\tau)] \quad (1)$$

Where μ_0 is the low field mobility, V_{ds} is the drain voltage, Z is the channel width, L is the channel length, Q_{d0} is the depletion charges when all defects are neutral, V_{ds} is the drain voltage, N_{tt} and N_a are respectively the traps and dopants concentrations and τ is the emission time constant at fixed temperature [10].

The trap energy level E_T was identified by carrying out a pulse–width scan at room temperature and at a fixed value of the pulse base level V_2. As a result, the value of the pulse width T_{max} which gives the maximum CDLTS signal is determined. The pulse width is then fixed at this value and the CDLTS signal is measured as a function of V_2, while the pulse top level V_1 is kept fixed at a specific value in strong inversion. As the base level in increased, the CDLTS signal S remains constant at the beginning, then starts to decay and approaches zero. This decay happens when the Fermi level position corresponding to V_2 starts to be close to E_T. The CDLTS signal continues to decrease and eventually reaches zero when the Fermi level at the semiconductor surface goes just above E_T.

Fig. 2 represents the variation of CDLTS signal S with respect to the inverse of the pulse width $1/T$ for different stress periods in the case of positive bias stress.

It is clear that the CDLTS signal S is altered by the applied stress. T_{max} is equal to 420 μs for the virgin device and the devices stressed for 30, 60 and 90 min while T_{max} is about 400 μs in the case of the device stressed for 120 min. CDLTS signal S shows larger values after stress and we noticed that for stress periods above 60 min S has smaller values than those detected at 60 min [14].

Fig. 3 shows the variation of CDLTS signal S vs. pulse base level V_2. We found that the signal's annulations do not take place at the same V_2.

Fig. 4 represents the variation of the CDLTS signal S vs. the inverse of the pulse width $1/T$ for different stress periods in the case of negative bias stress. CDLTS signal S shows an ascending variation with stress time in the case of negative bias stress.

Fig. 5 represents a plot of the CDLTS signal S vs. V_2 for different stress periods and in the case of negative bias stress. As positive bias stress, the annulations in the case of negative bias stress show different values of V_2 with respect of stress time.

As shown in Figs. 3 and 5 the signal CDLTS reaches zero at a certain value of V_2, which corresponds to $E_T - E_V$. Tables 1 and 2

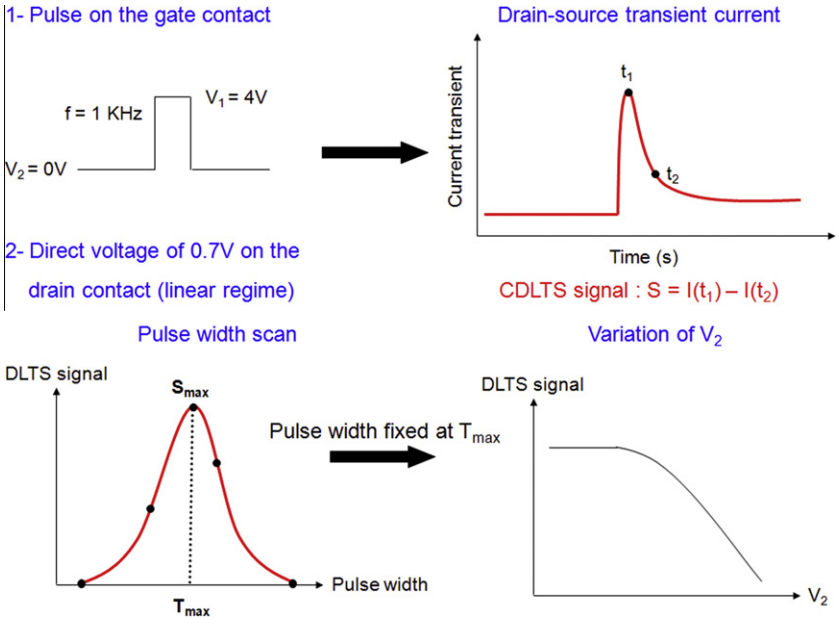

Fig. 1. Illustrated figure of the CDLTS technique and different experimental parameters.

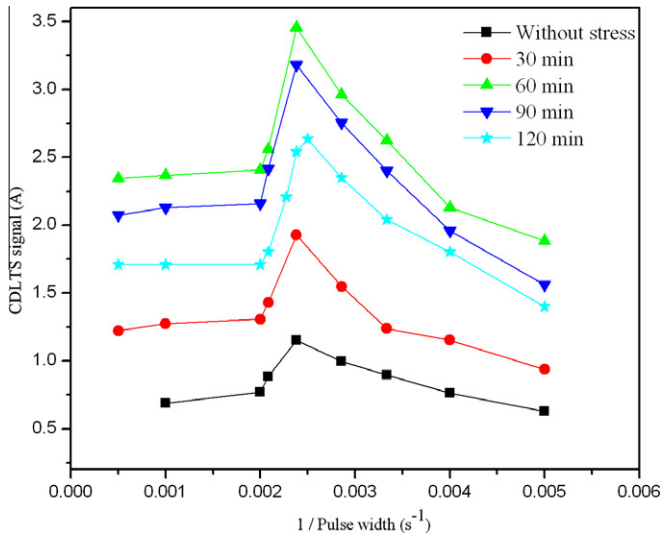

Fig. 2. Measured CDLTS signal vs. the inverse of the pulse width $1/T$ for different stress periods in the case of positive bias stress.

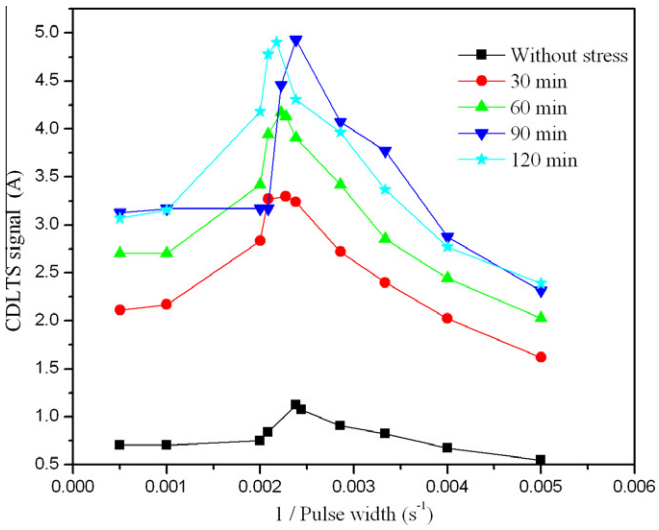

Fig. 4. Measured CDLTS signal vs. the inverse of the pulse width T for different stress periods in the case of negative bias stress.

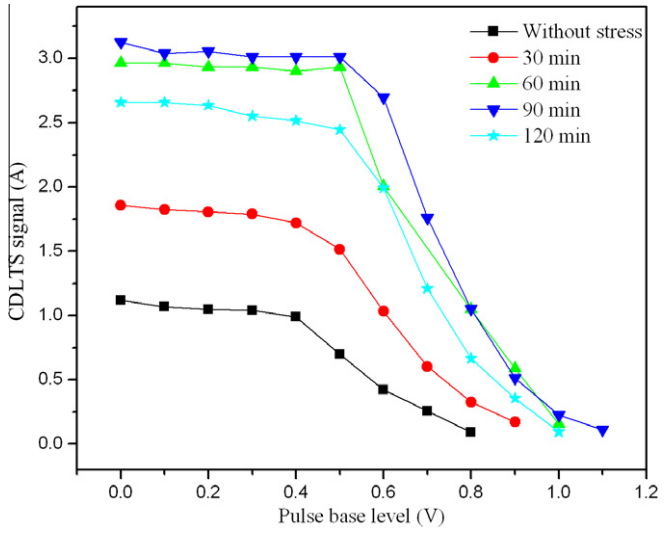

Fig. 3. Measured CDLTS signal vs. pulse base level V_2 in the case of positive bias stress.

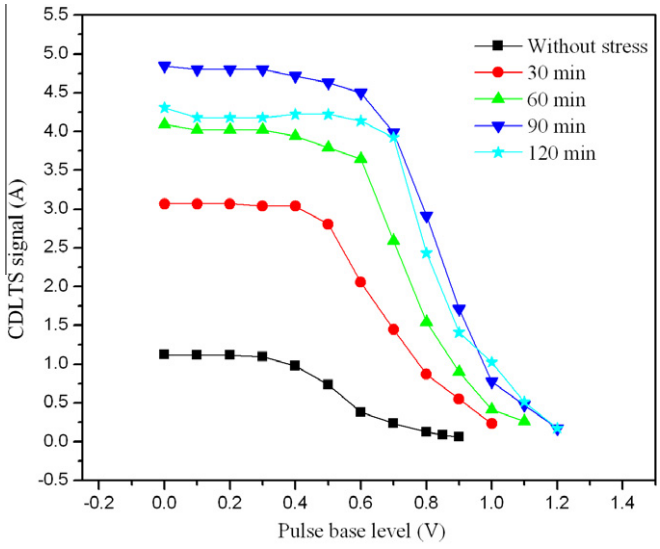

Fig. 5. Measured CDLTS signal vs. pulse base level V_2 in the case of negative bias stress.

represent the value of V_2 given annulations, the corresponding energies in the band gap $E_T - E_V$ and the nature of detected defects and the capture cross section in the case of positive and negative bias stress respectively.

Fig. 6 represents the energy bands diagram under polarization. The surface potential can be expressed as a function of the gate voltage V_2 and the flat band voltage V_{FB} by:

$$\psi_S = V_2 + |V_{FB}| \tag{2}$$

Knowing Ψ_S, the traps activation energy is calculated basing on the following relation [11]:

$$E_T - E_V = \frac{E_g + V_2 - |V_{FB}|}{2} \tag{3}$$

Fig. 7 shows the positions of different trap levels presented into the band gap of the semiconductor. Donor and acceptor impurities are commonly introduced into semiconductors to increase electron or hole concentrations, which modifies the electrical properties of the material. The energy levels created in the band gap by the presence of such impurities are situated close to the top of the valence band or the bottom of the conduction band. Other elements, such as gold, silver, iron, copper and zinc introduce one or several energy level in the band gap of silicon. These levels are located closer to the center of the band gap and are called "deep levels".

The growth of the semiconductor, the processing of the device and operating conditions can be considered as the main source for defects [15]. Also the applied high field stress leads to the creation of oxide trapped charges (into the gate oxide) and interface states (at the Si/SiO_2 interface) [16,17].

Knowing the trap activation energy, the capture cross section can be estimated via the following relation:

$$\mathrm{Ln}\left(\frac{e_p}{T^2}\right) = \mathrm{Ln}(\gamma\sigma_p) - \frac{E_a}{KT} \tag{4}$$

Where e_p is the emission rate $\left(e_p = \frac{\mathrm{Ln}(t_2/t_1)}{(t_2-t_1)}\right)$, T is the room temperature, γ is a pre-exponential factor ($\gamma = 1.78 \times 10^{21}\ s^{-1}cm^{-2}$ for

Table 1
Deep levels detected in the case of positive bias stress.

Stress time (min)	V_2 (V)	$E_T - E_V$ (eV)	Defect nature	Capture cross section (cm^{-2})
0	0.84	0.24	Cu	3.136×10^{-19}
30	1	0.34	Ag	1.824×10^{-17}
60	1.05	0.41	Fe	2.665×10^{-16}
90	1.27	0.40	Fe	1.852×10^{-16}
120	1.12	0.48	Complex Fe contamination	5.206×10^{-15}

Table 2
Deep levels detected in the case of negative bias stress.

Stress time (min)	V_2 (V)	$E_T - E_V$ (eV)	Defect nature	Capture cross section (cm^{-2})
0	1.06	0.11	Fe–B	1.893×10^{-21}
30	1.06	0.21	Shallow trap	9.562×10^{-20}
60	1.38	0.15	Shallow trap	9.378×10^{-21}
90	1.40	0.14	Shallow trap	6.682×10^{-21}
120	1.35	0.26	Interface state	7.20×10^{-19}

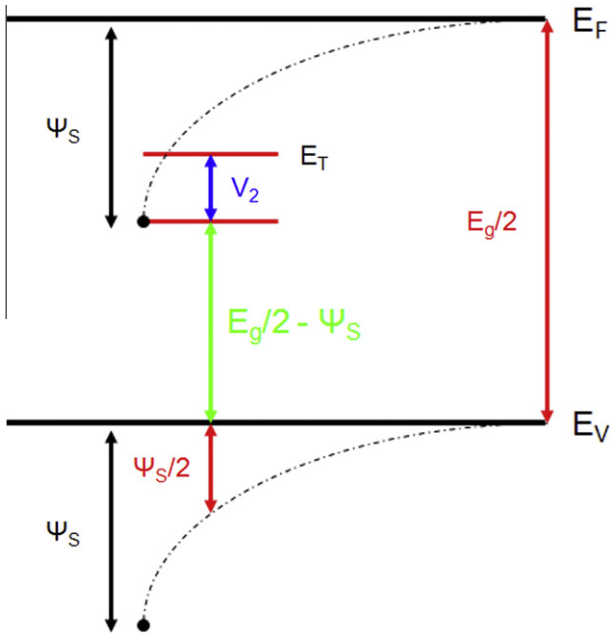

Fig. 6. Energy-band diagram of the semiconductor surface with a deep trap under polarization.

p-type Si), K is the Boltzmann constant and E_a is the activation energy ($E_a = E_T - E_V$).

In the case of positive bias stress, initially we could detect the copper atom Cu [18]. This atom may be the result of a contamination during fabrication process.For other stress periods, two assumptions can be made:

1. Metallic atoms present in the channel as residue of manufacturing process are activated by the applied stress such as silver Ag at 30 min [19], iron Fe for 60, 90 min [20,21] and complex Fe contamination for 120 min [22–25].
2. These defects are created by the electrical stress and their activation energies are equal to those of Ag and Fe.

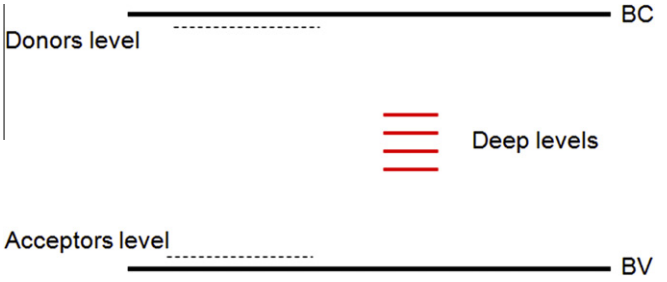

Fig. 7. Illustrated figure of different levels presented within the band gap of the semiconductor.

The disappearance of traps associated to copper Cu and silver Ag for larger stress periods can be due to their healing after 30 min of positive bias stress.

In the case of negative bias stress, defect detected before stress corresponds to acceptors level due to the formation of the Fe–B complex [26]. Since the material is p type doped, pairing of the interstitial iron with boron is probably occurring. However, this case has been investigated by several authors [27–29] and they found an activation energy for FeB of nearly 100 meV. For 30, 60, 90 min of stress, defects detected are shallow traps emerged associated to fast trapping/detrapping mechanisms of both type of carriers, due to the alternative charging of gate oxide with holes and electrons [30]. Trap detected at 120 min of negative bias stress is associated to an interface state at the Si/SiO_2 interface [30].

Considering the capture cross section, we notice that defects detected in the case of positive bias stress have larger capture cross section than those detected for negative bias stress.

All these defects are located in the lower half of the forbidden band gap scanned by applying a positive voltage V_2 on the gate contact (inversion regime) and where energy levels are inclined downwards.

4. Conclusion

In this paper, a novel approach for current DLTS has been adopted by using a pulse width scan. This measurement procedure does not involve any temperature variation and is therefore simpler and faster than the conventional measurement scheme. The originality of our work consists on studying commercial VDMOSFETs structures subjected to a high field stress. Trapping energies and capture cross sections have been determined for different stress periods. In the case of positive bias stress metallic atoms have been activated and displaced into the channel. Fe–B complex level, shallow traps and interface state have been detected in the case of negative bias stress.

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