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Fabrication and electrical characterization of Au/Pyronine-G/p-Si diode

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ABSTRACT

Au/Pyronine-G/p-Si diode was fabricated via solution-processing method. The current–voltage and the capacitance–voltage characteristics of the diode were measured at room temperature. It was seen that a rectifying behavior from the current–voltage characteristics and the current in the reverse direction was increased by white light-illumination. The characteristic parameters of the device such as barrier height, ideality factor and interface states density were determined from the current–voltage measurements. Also, Norde method was used to evaluate the current–voltage characteristics. From the dark current–voltage characteristics, the values of ideality factor and barrier height of the device were calculated as 1.36 and 0.78 eV, respectively. It was seen that this barrier height value calculated for the Au/Pyronine-G/p-Si diode was significantly larger than the value of conventional Au/p-Si Schottky diodes at room temperature. The energy distribution of the interface state density determined from the current–voltage characteristics increased exponentially with bias from $1.05\times10^{10}\,eV^{-1}\,cm^{-2}$ at $(0.74\ E_V)$ eV to 1.19×10^{12} at $(0.49\ E_V)\,eV^{-1}\,cm^{-2}$. The barrier height and acceptor carrier concentration values for the Au/Pyronine-G/p-Si diode was extracted as 0.92 eV and $9.35\times10^{14}\,cm^{-3}$ from linear region of its the capacitance–voltage characteristics at 1 MHz, respectively.

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1. Introduction

Organic materials can be the “core” of a wide range of new opto-electronic and electronic devices. Organic electronic devices demonstrate unique advantages compared with the inorganic semiconductor devices [1,2]. These include low fabrication cost, excellent processability, high mechanical flexibility, and versatility of the material chemical structure [3]. Because of interesting physical properties, the applications of organic semiconductors are extensive, such as for organic thin film transistors, organic light-emitting diodes, and organic solar cells [4,5].

The organic pigments were used to fabricate organic photoreceptor as a charge photogenerating materials for electro-photography and organic photovoltaic devices [6]. The modification and control of the interfacial potential barrier for metal/semiconductor diodes has been achieved using thin interlayers of the organic semiconductor [7–14].

Water-soluble xanthene dye families such as pyronins, acridines, and rhodamines have a remarkable position among organic dyes. These dyes are used for various purposes due to their unique and tuning optical properties [6,15–18].

Pyronin B and Pyronin G are cationic xanthene dye compound and sensitive to the molecular environment.

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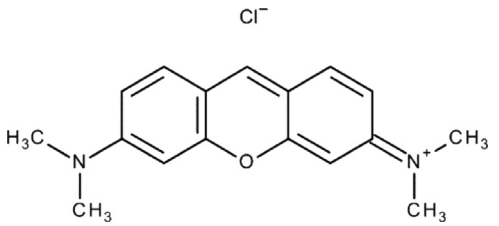

Fig. 1. Molecular structure of Pyronine-G organic compound.

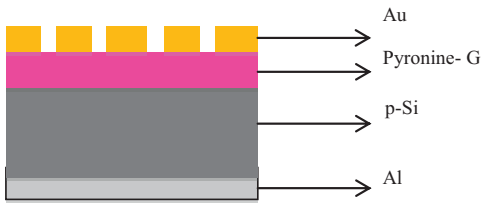

Fig. 2. The schematic diagram of the Au/Pyronine-G/p-Si diode.

Pyronin-G was studied due to their high molar absorptivity, high quantum yields of fluorescence [19]. Pyronin-G solutions are red in transmitted light displaying a yellow fluorescence in reflected light [20]. The molecular structure ($C_{17}H_{19}ClN_2O$) is of Pyronine-G [20] is shown in Fig. 1. Pyronine-G absorbs the light in the visible region from 440 nm to 660 nm with a maximum at 540 nm. It is also a well known material as an electron acceptor in photochemistry and the electronic transition in the molecular system is π–π^* [21].

In the present work, Au/Pyronine-G/p-Si diode was fabricated and the current–voltage (I–V) and capacitance–voltage (C–V) characteristics of device was investigated at room temperature and in dark. The purpose of this work is to investigate the electrical characterizations of the Au/Pyronine-G/p-Si device and to compare the electrical parameters of this device with those of conventional Au/other organic compounds/p-Si diodes.

2. Experimental procedures

In this study, p-type Si semiconductor wafer with (1 0 0) orientation and 400 μm thickness and 1–10 Ω cm resistivity was used. The p-Si wafer was chemically cleaned using the RCA cleaning procedure (i.e. 10 min boiling in $NH_3+H_2O_2+6H_2O$ followed by 10 min $HCl+H_2O_2+6H_2O$ at 60 °C) before making contacts. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of resistivity of 18 MΩ cm with ultrasonic vibration for 5 min and finally dried by high purity nitrogen (N_2) atmosphere. The ohmic contact was made by evaporating the Al metal on the back of the p-Si substrate, and then was annealed at 580 °C for 3 min in N_2. The native oxide on the front surface of the substrate was removed in a $HF+10H_2O$ solution and then, the wafer was rinsed in de-ionized water for 30 s before forming the Pyronine-G organic thin layer on the front surfaces of the substrate. After the cleaning procedures and ohmic metallization, the pyronine-G film on the front surface of the p-Si wafer was directly formed by using the solution processing method and dried for 20 min. Then, for the other ohmic contact the 99.99% purity gold (Au) metal were deposited on this organic film with a diameter of 1 mm using a metal shadow mask. All evaporation processes were carried out in a vacuum coating unit at about in 10^{-6} Torr. I–V and C–V measurements were measured using a Keithley 487 Picoammeter/Voltage source and a HP 4192A LF Impedance Analyzer, respectively. Fig. 2 shows a schematic diagram of the Au/Pyronine-G/p-Si device.

3. Results and discussion

According to the thermionic emission theory, the current in Schottky barrier diodes (SBDs) for $qV > 3kT$ can be expressed as [22]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right) \tag{1}$$

where I_0 is the saturation current defined by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \tag{2}$$

where the quantities V, A, A^*, T, k, q, Φ_b and n are the forward-bias voltage, the effective diode area, effective Richardson constant for p-type Si, temperature in Kelvin, Boltzmann constant, electronic charge and the zero bias apparent barrier height (BH) and ideality factor, respectively. From Eq. (1), n can be written as

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln\ I)}\right) \tag{3}$$

n is introduced to take the deviation of the experimental I–V results from the ideal thermionic model into account or to include the contributions of other current transport mechanisms. It should be $n=1$ for an ideal contact. However, n may be a value greater than unity. The high values in the ideality factor are caused possibly by various effects such as inhomogeneities of film thickness, interface states, series resistance, tunneling process and non-uniformity distribution of the interfacial charges, the image-force effect and recombination–generation mechanisms [23–28].

Φ_b is the zero bias barrier height (BH), which can be obtained from the following equation:

$$\Phi_b = \frac{kT}{q\ln(AA^*/I_0)} \tag{4}$$

Fig. 3 shows the experimental semi-log forward- and reverse-bias ln I–V characteristics of the Au/Pyronine-G/p-Si under dark and illumination conditions. As can be seen in Fig. 3, the Au/Pyronine-G/p-Si diode exhibits rectifying behavior. The weak voltage dependence of the reverse-bias current and the exponential increase of the forward-bias current are characteristic properties of rectifying interfaces. The reverse current of the diode has increased by white light illumination (Fig. 3). The charge carriers generate as a result of the light absorption and the current increase.

Using the thermionic emission theory [22,29], the experimental values of the BH and the n were determined from the current axis intercept and the slope of the linear

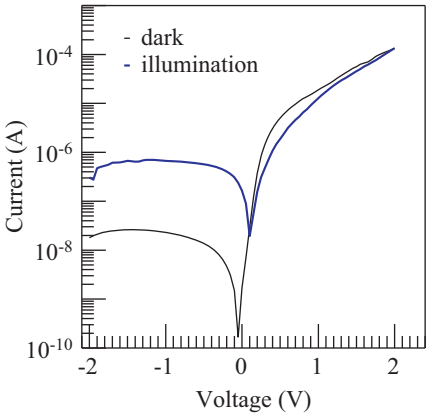

Fig. 3. The current–voltage characteristics of the Au/Pyronine-G/p-Si diode.

region (indicating that the effect of series resistance in this region was not important) [30] of the forward bias ln *I–V* characteristics of Au/Pyronine-G/p-Si diode, respectively. The values of the *n* and the Φ_b for the Au/Pyronine-G/p-Si diode were calculated as 1.36 and 0.78 eV in dark and 3.77 and 0.71 eV for white light illumination using Eqs. (3) and (4), respectively. It was seen that the BH value of 0.78 eV calculated for the Au/Pyronine-G/p-Si structure was significantly larger than the values of 0.34 eV [29] and 0.29 eV [31] of conventional Au/p-Si Schottky diodes at room temperature.

Two electronic structures are possible in which the conjugation is totally different, one where the oxygen assumes positive charge and in the other possible structure the nitrogen assumes positive charge. However, because the nitrogen is less electronegative than oxygen, the former can support a positive charge more easily than the latter, and therefore the structure with positive nitrogen is the more likely one [7,14,32,33]. These findings indicate that the Pyronine-G organic thin film formed on inorganic substrate change the barrier height of Au/p-Si Schottky diode. Thus, the change in barrier height can qualitatively be explained by an interface dipole induced by the organic layer passivation [7,10,34]. It should be noted that barrier height is the contact potential barrier that exists at the interface between the organic Pyronine-G and inorganic p-Si. The barrier height controls the injection of charge from the metal/organic contact into the inorganic semiconductor substrate [7]. Ideality factor and barrier height values of Au/Pyronine-G/p-Si were compared with Au/other organic compound/p-Si diodes in Table 1. As can be seen Table 1, these ideality factor values are larger than the value of 1.36 obtained by us.

The rectification ratio of Au/Pyronine-G/p-Si diode was calculated from the ratio of forward and reverse current at certain bias. The voltage dependence of the calculated rectification ratio at room temperature is shown in Fig. 4.

As can be seen Fig. 3, the current curve in forward bias quickly becomes dominated by series resistance giving rise to the curvature at high current in the semilog *I–V* plot. The series resistance (R_s) of device plays an important role on electrical characteristics. Especially it can arise from

Table 1
Ideality factor and barrier height values of Au/Pyronine-G/p-Si compared with Au/other organic compound/p-Si diodes.

Diodes	*n*	Φ_b (eV)	Reference
Au/Pyronine-G/p-Si	1.36	0.78	Present work
Au/Polypyrrole/p-Si/Al	1.88	0.78	[35]
Au/p-Si/Strontium titanate/Au	5.1	0.41	[36]
Au/Poly(4-vinyl phenol)/p-Si	2.76	0.70	[37]
Au/Aniline blue/p-Si	2.17	0.75	[38]
Au/PDI Perylene-diimide /p-Si	1.77	0.58	[4]
Au/Pyronine G(Y)/p-Si/Al	2.7	0.83	[17]

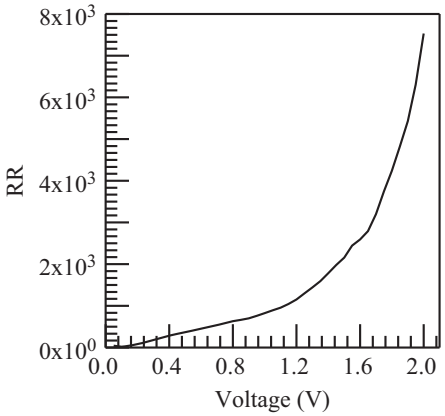

Fig. 4. The voltage dependence of rectification ratio of the Au/Pyronine-G/p-Si diode.

five different sources: (1) the contact wires, (2) the back contact of semiconductor; (3) impurities in semiconductor; (4) bulk resistance of the organic material and inorganic semiconductor and (5) non-uniform doping distribution in the semiconductor [39].

Norde's functions [40] *F*(*V*) are used to obtain the values of BH and the R_s. The *F*(*V*) function is defined as

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \quad (5)$$

where *I*(*V*) is current obtained from the *I–V* curve and γ is an integer (dimensionless) greater than *n*. A plot of *F*(*V*) versus *V* for the diode at room temperature is shown in Fig. 5.

The value of the BH of a diode can be determined as follows (by using Norde's functions):

$$\Phi_b = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{kT}{q} \quad (6)$$

where $F(V_{min})$ is the minimum value of *F*(*V*) and V_{min} is the corresponding voltage [40].

It has been observed that voltage drop caused non-ideal behavior at all temperatures at high voltage region (series resistance region). For real contacts ($n > 1$), the series resistance can be determined as

$$R_s = \frac{(\gamma - n)kT}{qI_{min}} \quad (7)$$

where I_{min} is the value of the forward current at the voltage V_{min} where the function *F*(*V*) exhibits a minimum.

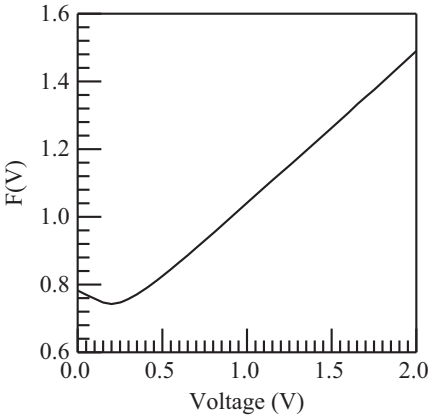

Fig. 5. $F(V)$ versus V plot of the Au/Pyronine-G/p-Si diode at room temperature.

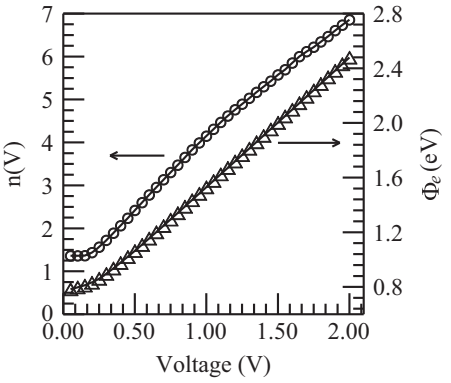

Fig. 6. The voltage dependence of the ideality factor ($n(V)$) and the effective barrier height (Φ_e) of Au/Pyronine-G/p-Si diode.

From the F–V plot by using $F(V_0)=0.74$ and $V_0=0.2$ V values, the values of BH and R_s of the Au/Pyronine-G/p-Si diode were determined as 0.82 eV and 44 kΩ at room temperature, respectively. Furthermore, the value of series resistance indicates that the series resistance is a current-limiting factor for this structure. There is a good agreement among the values of BH obtained from the forward bias ln I–V and Norde functions.

It is more important to know how the barrier height varies with the applied voltage. The potential across the interface varies with bias because of the change in the interface states charge as a result of the applied voltage, which modifies the barrier height. The effective barier height Φ_e is given by [41,42]

$$\Phi_e = \Phi_b + \beta V = \Phi_b + \left(1 - \frac{1}{n(V)}\right)V \tag{8}$$

where β is the voltage coefficient of the Φ_e and is a parameter that combines the effects of both the interface states and interfacial layer thickness for the cases in which interface states are in equilibrium with the semiconductor.

Fig. 6 shows the voltage dependence of the n and the effective barrier height Φ_e. A strong bias dependence for both n and Φ_e is observed. This bias dependence is presumed to be due to the presence of an organic interfacial layer and interface states located between interfacial layer and semiconductor interface [4,28]. In the forward bias case, the increase in the effective barrier height, Φ_e of the diode with bias can be understood as follows: when the diode is forward biased, the quasi Fermi level for the majority carriers rises on the semiconductor side. Thus, most of the electrons will be injected directly into the metal forming a thermionic emission current, while some of them are trapped by the interface states. This charge capture process results in an increase in the effective barrier height, thereby reducing the diode current [43].

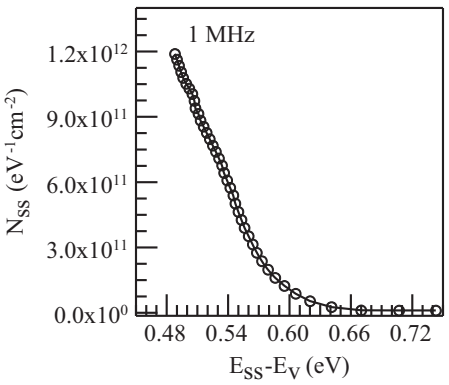

Fig. 7. Interface state density distribution curve of the Au/Pyronine-G/p-Si diode.

For sufficiently thick interfacial layer, then the interface state density N_{ss} [42,44,45] is given by

$$N_{ss} = \frac{1}{q}\left(\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right) \tag{9}$$

where δ is the thickness of the organic interfacial layer (δ=93 nm) (calculated from C–V measurement at 1 MHz frequency using the formula ($C_{org}=\varepsilon_i\varepsilon_0 A/\delta$) where C_{org} is the capacitance of the interfacial layer in strong accumulation region (C_{org}=269.5 pF at 1 MHz), ε_i is the permittivity of pyronine-G taken as 3.616 [21] and W_D is the width of the space charge region (W_D=974 nm) calculated from C^{-2}–V characteristic at 1 MHz using the formula ($W_D=\sqrt{2\varepsilon_S/qN_AV_d}$)[22], respectively.

For a p-type semiconductor, the energy of the interface states E_{ss} with respect to the top of the valance band is given by

$$E_{SS} - E_V = q\Phi_e - qV \tag{10}$$

The N_{ss} versus E_{ss}–E_v was obtained substituting values of the $n(V)$ and other parameters in Eq. (9). The energy distribution curve of the interface state density (N_{ss}) ranges from 1.05×10^{10} eV^{-1} cm^2 at (0.74 E_V) eV to 1.19×10^{12} at (0.49 E_V) eV^{-1} cm^{-2} for Au/Pyronine-G/p-Si diode as given in Fig. 7. It has been seen that the interface state densities have exponential rise with bias towards the top of the valence band. The order of interface states is lower than other metal/organic compound/p-Si semiconductor devices [4,42,46].

Fig. 8 shows the forward and reverse bias C–V characteristics of the Au/Pyronine-G/p-Si device measured at 1 MHz and room temperature. As observed, the C–V curve

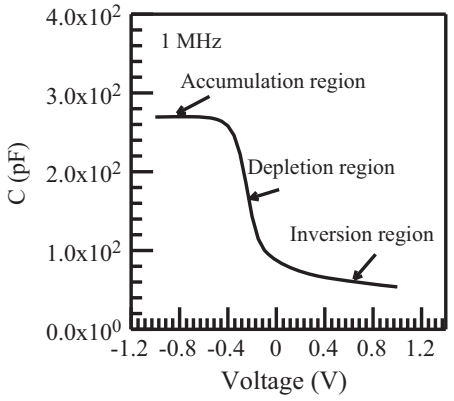

Fig. 8. The forward and reverse bias *C–V* characteristics of the Au/Pyronine-G/p-Si diode.

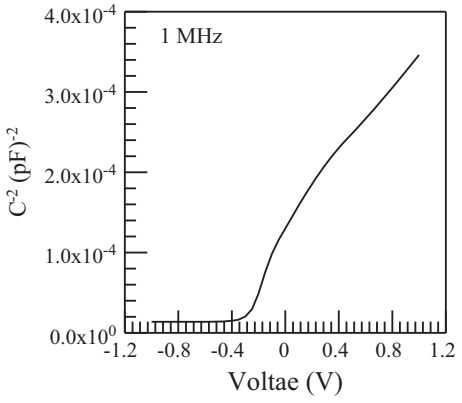

Fig. 9. The forward and reverse bias C^{-2}–*V* characteristics of the Au/Pyronine-G/p-Si diode.

has three regimes of accumulation–depletion–inversion region. The capacitance is dependent on the applied bias voltage and increases with increasing positive voltage until accumulation steady state [4,47].

The relation between capacitance and applied bias voltage for diodes is given by [18,48]

$$C^{-2} = \frac{2(V_d + V)}{q\varepsilon_s\varepsilon_o A^2 N_A} \tag{11}$$

where V_d is the diffusion potential at zero bias, which is determined from the extrapolation of the linear C^{-2}–*V* plot to the *V*-axis (Fig. 9). V_d is the barrier seen by holes in the valance band of p-type semiconductor trying to move into the metal, ε_s the dielectric constant of Si, and N_A is the concentration of ionized acceptors, which is given as

$$N_A = N_V \, exp(qV_p/kT) \tag{12}$$

where N_V is the state density in the valance band for Si and V_p the potential difference between the Fermi energy level (E_f) and the top of the valance band in the neutral region of p-Si, which is directly equal to E_f and can be calculated once the carrier concentration N_A is obtained through Eq. (12). The value of V_p was obtained from the following relation:

$$qV_p = kT \ln\left(\frac{N_V}{N_A}\right) \tag{13}$$

The value of the Φ_b can be obtained by the relation

$$\Phi_b = V_d + V_p \tag{14}$$

From the *C–V* measurements, Φ_b was calculated using the voltage intercept V_d of the C^{-2}–*V* plot from Eq. (14). By using the relationship between capacitance and voltage [22], the barrier height and acceptor carrier concentration values for the Au/Pyronine-G/p-Si devices were extracted as 0.92 eV and 9.35×10^{14} cm^{-3} from linear region of its C^{-2}–*V* characteristic for 1 MHz, respectively. Also, it is seen that this BH value is in good agreement with the obtained value by Ref. [17].

It can also be seen that the barrier height obtained from *I–V* measurements is lower than that obtained from *C–V* measurements. The difference between Φ_b (*I–V*) and Φ_b (*C–V*) for Au/Pyronine-G/p-Si diode was attributed the different nature of the *I–V* and *C–V* measurements. This difference is caused by three factors, i.e. image force lowering, tunneling and an inhomogeneous distribution of the barrier height over the surface [33]. The capacitance *C* is insensitive to potential fluctuations on a length scale of less than the space charge region and *C–V* method averages over the whole area and measures to describe BH [22,48,49].

4. Conclusions

The Au/Pyronine-G/p-Si diode was obtained forming a thin Pyronine-G layer by solution-processing method. The *I–V* and *C–V* characteristics of diode were investigated at room temperature and the characterization of Pyronine-G/p-Si interface was reported. The forward *I–V* characteristic of the diode was analyzed on the basis of the Standard thermionic emission theory. It was seen that the Au/Pyronine-G/p-Si diode indicated a good rectifying behavior. The main electrical parameters of this device, such as ideality factor (n) and barrier height values were found as 1.36 and 0.78 eV. The higher barrier height value of the diode was attributed to the physical barrier between the organic pyronine-G and inorganic P-Si. Thus, the modification of the barrier height for Au/p-Si diode was achieved by using the Pyronine-G organic layer. The ideality factor value of 1.36 obtained for the Au/Pyronine-G/p-Si diode was significantly lower than ideality factor value of the Au/other organic compound/p-Si diodes. In addition, the energy distribution of the interface state density determined from the current–voltage characteristics increased exponentially with bias from 1.05×10^{10} eV^{-1} cm^{-2} at (0.74 E_V) eV to 1.19×10^{12} at (0.49 E_V) eV^{-1}cm^{-2}. It was seen that the order of the interface state density of Au/Pyronine-G/p-Si is lower than most of metal/organic compound/inorganic semiconductor devices. It can be said that the organic pyronine-*G* is used to increase the quality of devices and to minimize the surface states, surface damage and contamination on the p-type Si substrate surface.

Acknowledgments

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