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Electrical characteristics of $CoSi_2$/n-Si(1 0 0) Schottky barrier contacts formed by solid state reaction

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Abstract

The Schottky barrier height (SBH) of $CoSi_2$ contacts formed by solid state reaction of Co, Co/Ti, Ti/Co and Ti/Co/SiO_2 on n-Si(1 0 0) substrates has been measured in the temperature range from 80 to 300 K with the use of current– and capacitance–voltage techniques. The forward *I–V* characteristics are analyzed on the basis of the standard thermionic emission model and the assumption of a Gaussian distribution of the barrier heights. The difference in SBHs determined from the *I–V* and *C–V* data is temperature dependent. From this difference, the standard deviation and its temperature coefficient are derived and are in the range of 58–78 meV and -0.07 to -0.14 meV K^{-1}, respectively. The Richardson plots, modified according to the Gaussian distribution model, have a good linearity over the whole temperature range for all samples. The corresponding activation energy is in good agreement with the barrier height determined from the *C–V* data. The SBH of the $CoSi_2$ contacts grown from Co and Ti bimetallic layers is lower than that grown from a Co layer only. The temperature coefficient of the SBH varies from approximately -0.16 meV K^{-1} for polycrystalline $CoSi_2$ to ~ 0 meV K^{-1} for epitaxial $CoSi_2$ contacts, thus suggesting different interfacial Fermi level pinning at the $CoSi_2$/Si contacts grown from different multilayer structures.

Keywords: Schottky-barrier; Silicide; Solid state reaction; Inhomogeneities

1. Introduction

The formation and characterization of $CoSi_2$ layers on Si has been the subject of a vast number of fundamental studies due to its importance as a contact material in sub-0.25 μm VLSI technology [1]. Both polycrystalline and epitaxial $CoSi_2$ layers can be grown by solid state reaction. Polycrystalline $CoSi_2$ is formed by direct reaction of a deposited Co layer with the Si substrate and epitaxial $CoSi_2$ is obtained when there exists a deposited Ti interlayer (TIME: Ti-interlayer Mediated Epitaxy [2]) or a very thin oxide layer (OME: Oxide Mediated Epitaxy [3]). Recently, it was also reported that a thick epitaxial $CoSi_2$ layer can be obtained by ex situ anneal of a Ti/Co/SiO_2/Si system [4–6]. The Schottky barrier characteristics of $CoSi_2$/Si contacts have been studied by *I–V*, *C–V*, photo-emission and ballistic electron emission microscopy (BEEM) techniques. It has been shown that $CoSi_2$/Si contacts grown by different conditions have different Schottky barrier characteristics due to the different structural properties at the $CoSi_2$/Si interface. For example, Lauwers et al. [7] reported a difference in barrier height between polycrystalline and epitaxial $CoSi_2$ contacts at low temperatures. Hatzikonstantinidou et al. [8] reported a dependence of the room temperature Schottky barrier height (SBH) of $CoSi_2$/Si contacts grown by solid state reaction of a Co/Ti/Si system on their annealing process.

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We have found that the $CoSi_2$ layers grown from the Co/Ti/Si reaction have slightly lower SBH than those grown from the Co/Si reaction [9].

However, the *I–V* characteristics of real MS contacts usually deviate from the standard thermionic emission (TE) model. Various models have been used to describe the deviations [10]. Recently, it was pointed out that the inhomogeneity of a real MS contact may cause anomalous *I–V* behavior [11–13]. One simple way to describe the inhomogeneity is to assume a Gaussian distribution of the barrier heights over the contact area [12–16]. This has been used to explain the difference in barrier heights determined by different measurement techniques: the non-linearity of the Richardson plot, the strong temperature dependence of the apparent SBH and ideality factor deduced from *I–V* data at low temperatures. The assumption of a Gaussian distribution has been confirmed by our previous BEEM measurements [9,16], where several hundreds of local SBHs measured over the whole contact area display an approximate Gaussian distribution. But BEEM measurements on $CoSi_2$/Si contacts have to be done at low temperature and only very thin $CoSi_2$ layers (<10 nm) can be measured. In this paper, various $CoSi_2$/Si contacts formed by solid state reaction of different multilayer structures have been measured using conventional *I–V*/*C–V* techniques in the temperature range of 80–300 K. Their detailed SBH properties are compared using the same analysis model, i.e., the assumption of a Gaussian distribution with a temperature dependence of both the mean barrier height and the standard deviation.

2. Experimental

Two different deposition systems (e-beam evaporation and ion sputtering) were used to fabricate $CoSi_2$ films on two types of n-Si(1 0 0) substrates. The first type of substrates were n/n^+ epitaxial wafers with a surface epitaxial layer of ~7 μm thickness and a $\sim 1 \times 10^{16}$ cm^{-3} doping concentration. The heavily doped substrates had a resistance of ~0.01 Ω·cm. A ~200 nm thick thermal oxide was grown, then rectangular windows were opened on the front side of the wafers to define active areas of Schottky diodes by using standard lithography and wet etching. The areas of the diodes ranged between 0.01 and 4 mm^2. Immediately after standard RCA cleaning and dipping in a diluted HF solution, the wafers were loaded in a multifunction sputtering system (OXFORD) with a base pressure of $\sim 1 \times 10^{-4}$ Pa. Metal layers (Co, Ti) were deposited sequentially by ion beam sputtering without breaking the vacuum. Four different structures, Co(10 nm)/Si, Co(20 nm)/Si, Co(5 nm)/Ti(3 nm)/Si and Ti(5 nm)/Co(5 nm)/Si were deposited. The silicide was achieved by a two-step ex situ rapid thermal anneal (RTA) process in an N_2 ambient: a first step annealing at 600°C for 60 s, followed by a two-step selective etch; in a boiling solution of H_2SO_4:H_2O_2 = 3:1 for 5 min and in a boiling solution of NH_4OH:H_2O_2:H_2O = 1:2:5 for 2 min, and finally a second step annealing for 60 s at various temperatures (700°C, 800°C or 900°C) (two-step annealing procedure). An In–Ga alloy (liquid) was used as backside ohmic contact. The second type of substrates were n-Si wafers with a doping level of $\sim 1 \times 10^{15}$ cm^{-3}. After standard RCA cleaning and a diluted HF dip, a thin layer of SiO_2 was grown by immersing the samples into a boiling solution of HCl:H_2O_2:H_2O = 3:1:1 for 5 min (Shiraki cleaning) [17]. Then the wafers were loaded immediately into an e-beam evaporation system with a base pressure of $\sim 2 \times 10^{-4}$ Pa. Two multilayer structures, Ti(5 nm)/Co(5 nm) and Ti(10 nm)/Co(10 nm) were deposited sequentially without breaking the vacuum. For comparison, wafers without the Shiraki oxide were also fabricated: Co(10 nm) and Co(10 nm)/Ti(7 nm). The deposited wafers were ex situ annealed in a RTA system for 30 s at 800°C or 1000°C (one-step annealing procedure). The backside ohmic contact was achieved by evaporating a 100 nm thick Ti layer. The diodes for the *I–V*/*C–V* measurements were made by cutting the wafers into small pieces (~2 mm^2).

I–V/*C–V* measurements were carried out from 80 K to room temperature using a computer controlled multifrequency LCR meter (HP 4274 A) and a Keithley 619 electrometer. The capacitance was measured at a frequency of 100 and 500 KHz. The temperature stability during the measurements was better than ±3 K.

3. Results

3.1. Polycrystalline $CoSi_2$/Si diodes grown from the Co/Si reaction

The $CoSi_2$/Si contacts, which were grown by solid state reaction of 20 nm thick Co on the patterned Si substrates with a final annealing at 800°C for 60 s, are studied first. From the literature [18] and our previous studies, it is known that the deposited Co has been completely transformed into polycrystalline $CoSi_2$. Fig. 1 shows the forward *I–V* characteristics at room temperature of four diodes with areas of 0.36, 0.61, 1.0 and 4.0 mm^2, respectively. The symbols represent the actual data obtained at 292 K and the solid curves are theoretical fittings based on the well-known thermionic emission equation [10]. At a forward bias V ($V > 3\,kT/q$), the current is given by

$$I = I_0 \exp\left(q(V - IR_s)/nkT\right), \tag{1a}$$

$$\text{and } I_0 = AA^*T^2 \exp\left(-q\Phi^{I-V}/kT\right), \tag{1b}$$

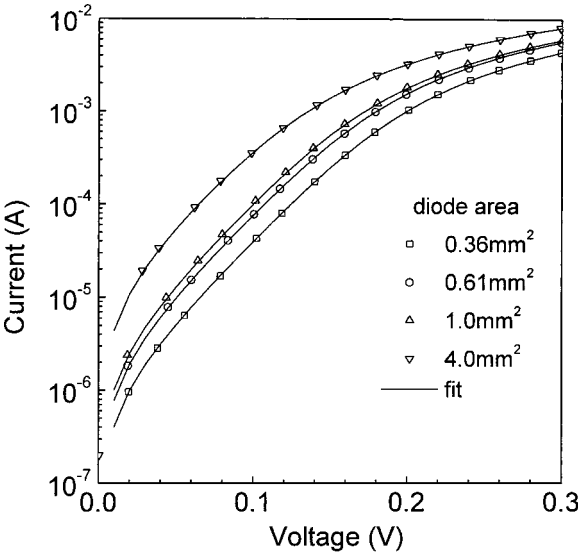

Fig. 1. Forward I–V characteristics at 292 K of four polycrystalline $CoSi_2$/Si diodes with different areas.

where I_0, A, A^*, T, q, Φ^{I-V}, R_s and n are the saturation current at zero bias, the diode area, the effective Richardson constant (the theoretical value is 112 A cm^{-2} K^{-2} for n-Si), the temperature in Kelvin, the electronic charge, the barrier height at zero bias determined from the I–V data, the diode series resistance and the ideality factor, respectively. A computer program is used for the least square fitting of the experimental data using Φ^{I-V}, n and R_s as adjustable parameters. Fig. 1 shows clearly that the fitting curves can match the experimental data quite well with almost the same fitting parameters: $\Phi^{I-V} = 0.615$ eV, $n = 1.01$–1.02 and $R_s = 16$–18 Ω for the four diodes. Other $CoSi_2$/Si contacts have similar behavior. This illustrates the quite good reproducibility of the fabrication process. The ideality factor slightly larger than unity can be attributed to the effect of image force lowering. In the above diodes, it causes a ~0.013 increase of the ideality factor and a ~20 meV lowering of the barrier height. The barrier heights determined from the C–V data are between 0.618–0.630 eV. Taking the image force lowering into account they are in agreement with the values of Φ^{I-V}.

Fig. 2(a) presents the forward I–V characteristics of one of the above diodes with an area of 0.61 mm^2 in the temperature range from 100 to 293 K. Eqs. (1a) and (1b) was used to fit the experimental data. The results are shown as the solid curves. At high temperatures or in the high bias region at low temperatures, the fitting curves match the experimental data quite well, while at low temperatures ($\lesssim$~200 K) a "double threshold" phenomenon is observed below about 10^{-6} A. The current in excess to that expected by the TE model in the low bias region has been attributed to recombination in the

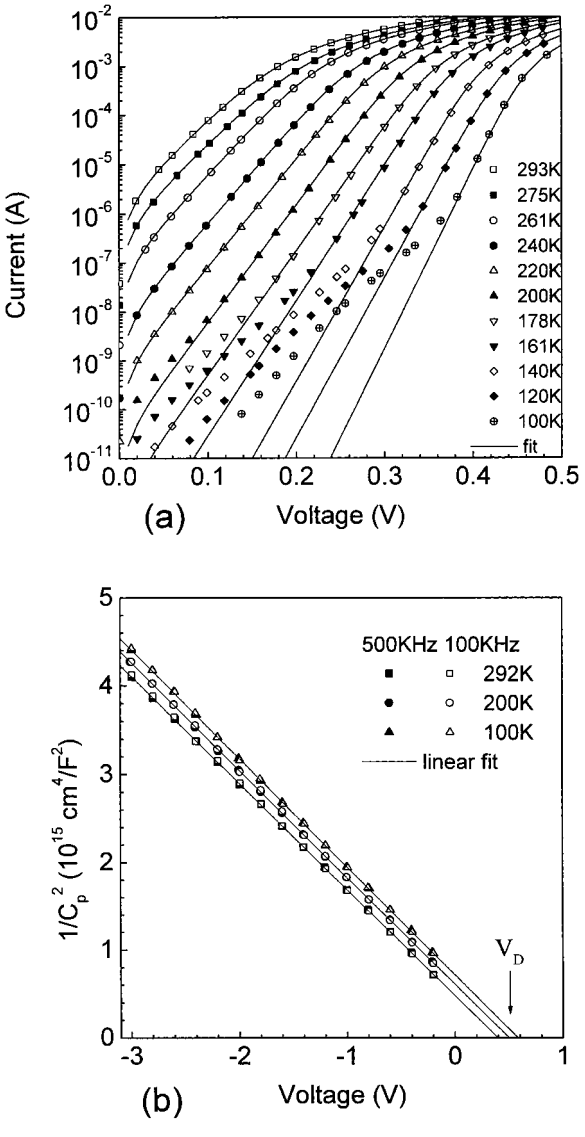

Fig. 2. (a) Forward I–V characteristics, (b) reverse $1/C^2$ versus V_r plots of a polycrystalline $CoSi_2$/Si diode with an area of 0.61 mm^2 in the temperature range of 100 to 293 K, the capacitance is measured at 100 and 500 KHz.

depletion region [8] or to a few patches of reduced barrier height embedded in the MS contact (SBH inhomogeneity) [11,16,19]. We find that the latter explanation is more reasonable in the present case. First, one can expect that improving the $CoSi_2$/Si interfacial quality can reduce the amount of patches, thus reduce the excess current. We observe that there is no such excess current in some epitaxial $CoSi_2$/Si diodes (Figs. 4 and 7). Second, carrier recombination is expected to occur in the depletion region at the periphery of the diodes [20], so diodes with a small area to periphery

ratio are expected to exhibit a larger carrier recombination current. However, no significant difference is found between the diodes with different areas in our experiments. Third, the absence of a frequency dependent capacitance at all temperatures indicates that the diode does not contain a measurable amount of deep levels within the depletion region. The excess current has been analyzed in detail using the pinch-off model in our previous paper [16], and will not be discussed in detail in this paper.

The values of Φ^{I-V} and n determined from the fitting are shown in Fig. 3(a) as a function of temperature. The series resistance R_s varies between 13 and 16 Ω, and is almost independent of the temperature. At low temperatures ($\leqslant \sim 220$ K) both Φ^{I-V} and n are strongly dependent on temperature, which will be explained by the following model of a Gaussian distribution of barrier heights [12–14].

Fig. 3(a) also displays the barrier heights deduced from the C–V data which are shown in Fig. 2(b). The plots of $1/C^2$ versus the reverse bias V_r give straight lines at all temperatures. The flatband voltages (V_D) are obtained from the intercepts of the extrapolated lines with the V_r axis. Then, the values of Φ^{C-V} are calculated by [10]

$$\Phi^{C-V} = V_D + kT/q + (kT/q)\ln(N_C/N_d), \tag{2}$$

where N_C is the effective density of states in the conduction band and N_d is the doping level which can be deduced from the slope of the Mott–Schottky line. The values obtained at different temperatures and at different frequencies are between 9.6 and 9.8×10^{15} cm^{-3}, which is in good agreement with the manufacturer's value (1×10^{16} cm^{-3}). Fig. 2(b) shows that the capacitance measured at 500 KHz is almost the same as that measured at 100 KHz. Due to the square dependence of Φ^{C-V} on $1/C$, compared to the logarithmic dependence of Φ^{I-V} on the current, Φ^{C-V} is more sensitive to the experimental error of the measured data than Φ^{I-V}. The same diode has been measured at the same frequency for several times at room temperature, and the variation of the determined Φ^{C-V} is similar to that determined at different frequencies. However, the trend of increasing Φ^{C-V} with decreasing temperature is clear in Fig. 3(a), which can be understood by the temperature dependence of the Si band gap [21]. We can assume a linear dependence of Φ^{C-V} on T in the above temperature range approximately:

$$\Phi^{C-V}(T) = \Phi_0^{C-V} + \alpha_\Phi^{C-V} T, \tag{3}$$

where α_Φ^{C-V} is the temperature coefficient of Φ^{C-V} and Φ_0^{C-V} is the SBH extrapolated towards zero temperature. The values of $\Phi_0^{C-V} = 667$ meV and $\alpha_\Phi^{C-V} = -0.14$ meV K^{-1} are obtained by linear least square fitting of the averaged values of Φ^{C-V} measured at 100 and 500 KHz.

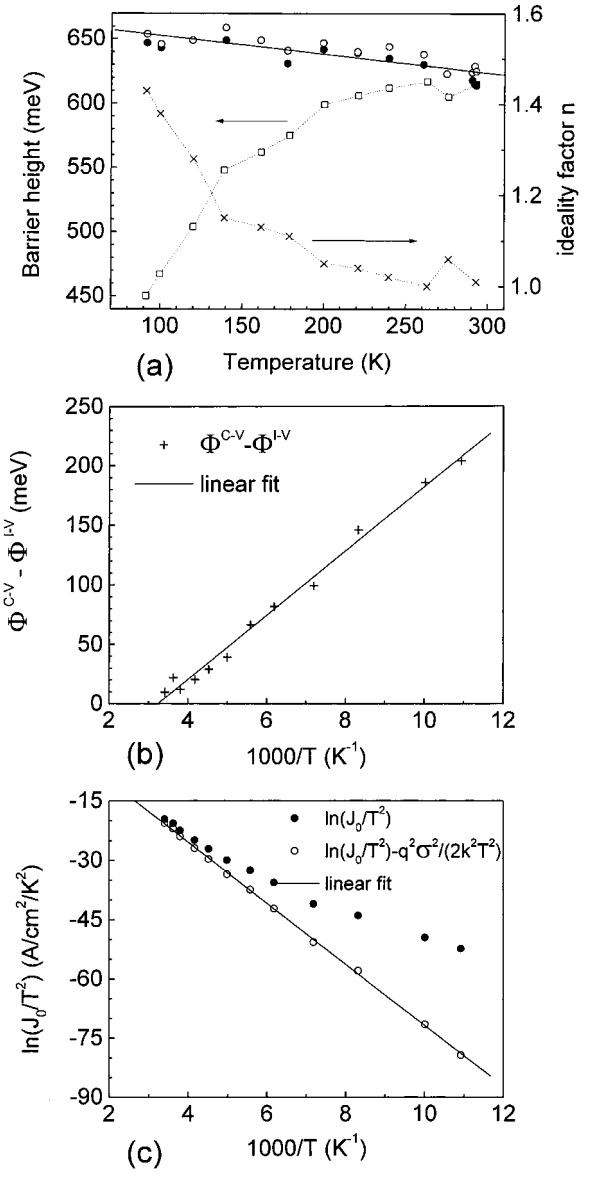

Fig. 3. (a) Φ^{I-V} and the ideality factor n from I–V data, and the capacitance barrier Φ^{C-V} from C–V data as a function of temperature: (○) Φ^{C-V}, 100 KHz, (●) Φ^{C-V}, 500 KHz, (□) Φ^{I-V}, (×) n; (b) the difference in barrier heights obtained between I–V and C–V data as a function of $1/T$; (c) the standard and modified Richardson plots for above polycrystalline $CoSi_2$/Si diode.

The difference between Φ^{I-V} and Φ^{C-V}, as well as the strong temperature dependence of Φ^{I-V} and n at low temperatures, has been explained by assuming a Gaussian distribution of barrier heights with a mean value $\overline{\Phi}_B$ and a standard deviation σ [12–16]. Both $\overline{\Phi}_B$ and σ may be temperature dependent [12]. For simplicity, a linear dependence of both $\overline{\Phi}_B$ and σ is assumed as a first approximation:

$$\overline{\Phi}_{B}(T) = \overline{\Phi}_{B0} + \alpha_{\Phi} T, \tag{4}$$

$$\text{and } \sigma(T) = \sigma_0 + \alpha_{\sigma} T, \tag{5}$$

wherein $\overline{\Phi}_{B0}$ and σ_0 are the mean barrier height and the standard deviation extrapolated towards zero temperature and α_{Φ} and α_{σ} are their temperature coefficients, respectively. The total current can be calculated by integrating the current determined by the ideal TE model for a single barrier height and weighted by the distribution function (parallel conductance model) [12,13,16,22]. The current expression has a similar form as Eqs. (1a) and (1b) but with the modified barrier height [13]:

$$\Phi^{I-V} = \overline{\Phi}_{B}(T) - q\sigma(T)^2/(2kT). \tag{6}$$

It reveals that the I–V data at low temperatures can still be described by Eqs. (1a) and (1b) apparently, but the apparent barrier height decreases with decreasing temperature. Moreover, it has been demonstrated that the capacitance C depends only on the mean barrier height and the capacitance Φ^{C-V} is equal to the mean barrier height $\overline{\Phi}_{B}$ [12,13]:

$$\Phi^{C-V}(T) = \overline{\Phi}_{B}(T). \tag{7}$$

Comparing Eqs. (6) and (7), one gets

$$\Phi^{C-V}(T) - \Phi^{I-V}(T) = q\sigma(T)^2/(2kT) \approx q\sigma_0^2/(2kT) + q\sigma_0\alpha_{\sigma}/k. \tag{8}$$

According to Eq. (8), the plot of $\Phi^{C-V} - \Phi^{I-V}$ versus reciprocal temperature is a straight line. Such a plot is shown in Fig. 3(b). By linear least square fitting the experimental data, the values of σ_0 and α_{σ} can be deduced from the slope and the intercept of the fitting line, respectively. From Fig. 3(b) $\sigma_0 = 68$ meV and $\alpha_{\sigma} = -0.14$ meV K are obtained.

The conventional Richardson plot is now modified as [12,13,16,22]

$$\ln(J_0/T^2) - q^2\sigma(T)^2/(2k^2T^2) = \ln(A^* e^{-q\alpha_{\Phi}/k}) - q\overline{\Phi}_{B0}/kT, \tag{9}$$

where J_0 is the saturation current density at zero bias, which can be obtained from the fitting curves in Fig. 2(a). The factor $\ln(J_0/T^2) - q^2\sigma(T)^2/(2k^2T^2)$ is calculated using the $\sigma(T)$ value derived from Fig. 3(b) and is plotted as a function of $1/T$ in Fig. 3(c). The plot of $\ln(J_0/T^2)$ versus $1/T$ is also shown for comparison. It can be seen that the modified Richardson plot has a quite good linearity over the whole temperature range corresponding to a single activation energy around $\overline{\Phi}_{B0}$. By least square linear fitting the data, $\overline{\Phi}_{B0} = 666$ meV is obtained from the slope of the fitting line, which is in good agreement with Φ_0^{C-V} (667 meV). Moreover, the effective Richardson constant A^* itself can be obtained from the intercept of the line on the ordinate. Using the α_{Φ} value obtained from the linear fitting of $\Phi^{C-V}(T)$ versus T, $A^* = 47$ A cm^{-2} K^{-2} is calculated, which is in good agreement with the theoretical value (112 A cm^{-2} K^{-2}).

The contacts fabricated from Co layers with different thickness have similar I–V and C–V characteristics. For example, a diode grown from 10 nm thick Co on the patterned Si substrate has values of Φ_0^{C-V}, α_{Φ}^{C-V}, σ_0, α_{σ}, $\overline{\Phi}_{B0}$ and A^* as indicated in Table 1. Increasing the annealing temperature to 900°C does not influence the I–V and C–V characteristics of the $CoSi_2$/Si contact and the results are given in Table 1. However, the $CoSi_2$/Si contacts fabricated by the one-step annealing process show normal I–V and C–V characteristics at high temperatures ($\Phi^{I-V} \approx 0.62$ eV, $\Phi^{C-V} \approx 0.64$ eV), but have bad rectifying properties at low temperatures ($<\sim$180 K) due to the large 'leakage current', which may be

Table 1
Summary of the values of Φ_0^{C-V}, $\overline{\Phi}_{B0}$, α_{Φ}^{C-V}, σ_0, α_{σ} and A^* for various $CoSi_2$/Si diodes

Samples		Φ_0^{C-V}	$\overline{\Phi}_{B0}$	α_{Φ}^{C-V}	σ_0	α_{σ}	A^*
As-deposit	Annealing	(meV)	(meV)	(meV K^{-1})	(meV)	(meV K^{-1})	(A cm^{-2} K^{-2})
Co(20 nm)/Si	800°C, 60 s,[a]	667	666	−0.15	68	−0.11	47
Co(10 nm)/Si	800°C, 60 s,[a]	652	653	−0.17	62	−0.07	88
Co(20 nm)/Si	900°C, 60 s,[a]	662	662	−0.15	78	−0.13	36
Co(5)/Ti(3)/Si	700°C, 60 s,[a]	549	542	−0.02	58	−0.14	20
Co(5)/Ti(3)/Si	800°C, 60 s,[a]	582	582	−0.04	63	−0.12	45
Co(5)/Ti(3)/Si	900°C, 60 s,[a]	581	589	−0.09	69	−0.13	67
Co(10)/Ti(7)/Si	1000°C, 30 s,[b]	614	619	−0.11	72	−0.12	68
Ti(5)/Co(5)/Si	800°C, 60 s,[a]	565	571	−0.11	66	−0.14	33
Ti(5)/Co(5)/SiO_2/Si	800°C, 30 s,[b]	593	590	0.00	64	−0.11	40
Ti(10)/Co(10)/SiO_2/Si	800°C, 30 s,[b]	588	596	−0.01	75	−0.13	74
Ti(10)/Co(10)/SiO_2/Si	1000°C, 30 s,[b]	594	599	0.00	73	−0.12	63

[a] Two-step anneal procedure.
[b] One-step anneal procedure.

contributed to the large amount of patches with low barrier height. It is known [18] that the $CoSi_2$ layers fabricated by a two-step RTA process with an intermediate selective etch have better interfacial quality than those fabricated by an one-step anneal process. The latter contains more patches than the former. Moreover, the *I–V* and *C–V* characteristics of the $CoSi_2$/Si contacts annealed at 1000°C show a strong deviation from the ideal TE model even at room temperature. No meaningful barrier height could be obtained. Atomic force microscopy (AFM) has shown that the surface roughness increases significantly after annealing at that temperature [23], indicating that the $CoSi_2$ layer has been partly destroyed due to agglomeration.

3.2. Epitaxial $CoSi_2$/Si diodes grown from Co/Ti/Si systems

The reaction mechanism of the Co/Ti/Si systems has been studied by many researchers [2,7,8,24]. It has been known that an inversion of the Ti and Co layer occurs upon annealing and an epitaxial $CoSi_2$ layer is formed at the M–S interface. It is believed that the ability of Ti to clean the Si surface and the fact that Co diffusion is slowed down by the Ti interlayer promote the epitaxial growth. X-ray diffraction (XRD) and Rutherford backscattering spectroscopy/channeling (RBS/C) studies show that the $CoSi_2$ layer grown by utilizing the two-step annealing procedure has better epitaxial quality than by using the one-step annealing procedure. The *I–V* and *C–V* characteristics of the $CoSi_2$/Si contacts grown by solid state reaction of Co/Ti/Si with different annealing procedures are compared in this part of our paper.

The forward *I–V* characteristics of the diode grown by using the two-step annealing procedure with a final annealing at 700°C for 60 s are depicted in Fig. 4. The fitting curves calculated based on Eqs. (1a) and (1b) are also shown. In this case, the experimental data can be fitted by Eqs. (1a) and (1b) quite well at the whole temperature range. No excess current is observed in the low bias region at low temperatures. It reveals that the epitaxial $CoSi_2$/Si contacts have more homogeneous interfacial properties than the polycrystalline ones. This is in agreement with cross sectional transmission electron microscopy (XTEM) observations on $CoSi_2$/Si films formed from Co/Si and Co/Ti/Si reactions [2,7,8,18]. Generally, the direct reaction of Co–Si leads to a polycrystalline $CoSi_2$ with a rough and undulated $CoSi_2$/Si interface due to an inhomogeneous nucleation caused by the native oxide. In the case of the Co/Ti/Si reaction, the thin Ti interlayer can react with SiO_2, so that the following Co/Si reaction occurs on an atomically clean Si surface.

Fig. 5(a) shows the barrier heights and the ideality factors, which are obtained from the fitting as a function

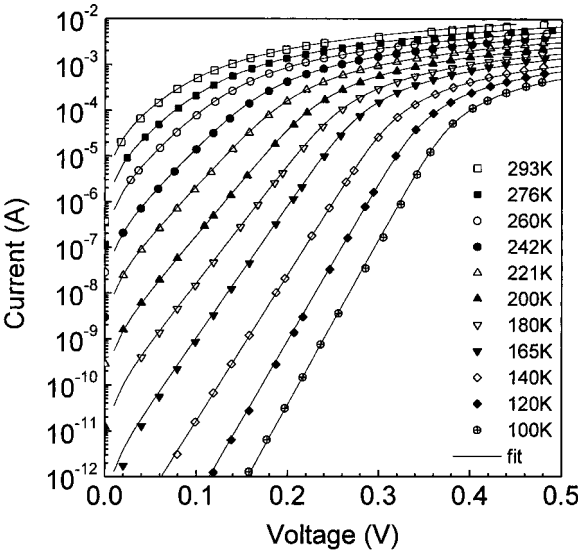

Fig. 4. Forward *I–V* characteristics of an epitaxial $CoSi_2$/Si diode with an area of 0.61 mm^2 in the temperature range of 100 to 293 K. The $CoSi_2$ layer was made by reaction of Co(5 nm)/Ti(3 nm)/Si with a final annealing at 700°C for 60 s.

of temperature. At high temperatures (above 220 K), the *I–V* barrier heights are 0.56 eV and the ideality factor is near unity. Below that temperature, the barrier height decreases and the ideality factor increases with decreasing temperature, which is again explained by the model of a Gaussian distribution of the SBHs. Fig. 5(a) also shows the SBHs obtained from the *C–V* data, which have similar characteristics as those shown in Fig. 2(b). The value of Φ^{C-V} has a very weak temperature dependence: $\Phi_0^{C-V} = 549$ meV and $\alpha_\Phi^{C-V} = -0.02$ meV K^{-1} are determined by linear least square fitting of the Φ^{C-V} data. The difference in Φ^{C-V} and Φ^{I-V} is shown in Fig. 5(b) as a function of $1/T$. By linear least square fitting the experimental data, the standard deviation of the Gaussian distribution and its temperature coefficient are obtained as $\sigma_0 = 58$ meV and $\alpha_\sigma = -0.14$ meV K^{-1}, which are in the same order of magnitude as those of the polycrystalline $CoSi_2$/Si diodes. From the modified Richardson plot, which is shown in Fig. 5(c), one obtains $\overline{\Phi}_{B0} = 542$ meV, in agreement with the value of Φ_0^{C-V}, and $A^* = 20$ A cm^{-2} K^{-2}, of the same order of magnitude as the theoretical value.

The other two diodes, which were grown by a similar procedure as the above diode but with a final annealing at 800°C and 900°C, have similar *I–V* and *C–V* characteristics as displayed in Figs. 4 and 2(b), respectively. The values of Φ^{C-V}, Φ^{I-V} and n are shown in Fig. 6 as a function of temperature. The values of Φ_0^{C-V} are 582 and 581 meV for those two diodes, in close agreement with the reported value (0.59–0.61 eV) for epitaxial $CoSi_2$/Si contacts [7,9,16]. The temperature coefficients of the

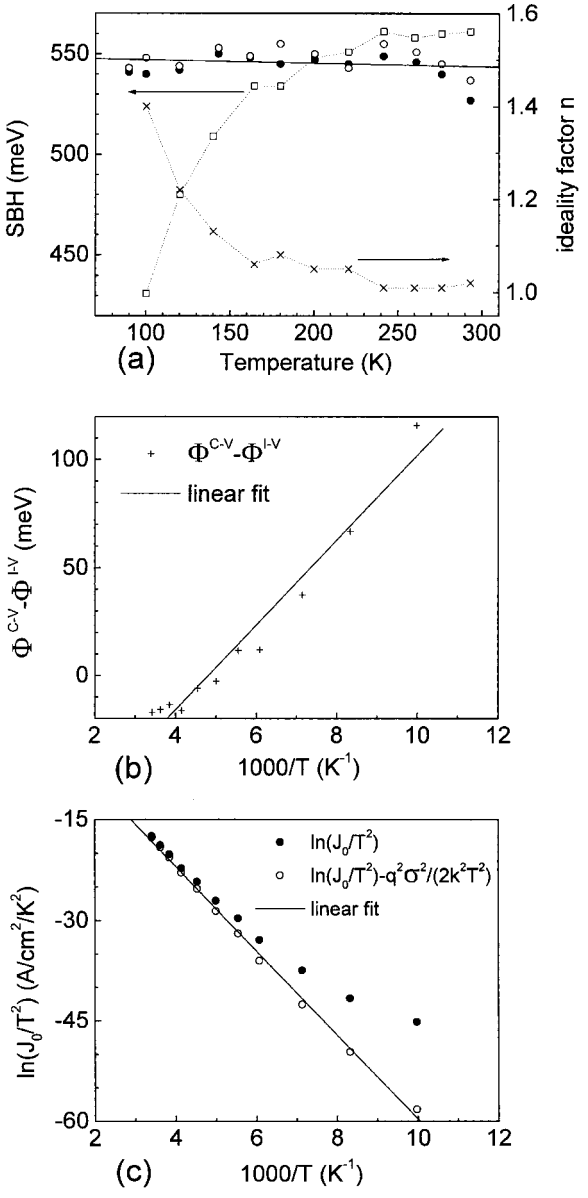

Fig. 5. The results of an epitaxial $CoSi_2$/Si diode which was made by reaction of Co(5 nm)/Ti(3 nm)/Si with a final annealing at 700°C for 60 s. (a) Φ^{I-V}, Φ^{C-V} and n versus T, (○) Φ^{C-V}, 100 KHz, (●) Φ^{C-V}, 500 KHz, (□) Φ^{I-V}, (×) n; (b) $\Phi^{C-V} - \Phi^{I-V}$ versus $1/T$; (c) $\ln(J_0/T^2)$ versus $1/T$.

SBH are -0.04 and -0.09 meV K^{-1}. The values of σ_0, α_σ, $\overline{\Phi}_{B0}$ and A^* are again given in Table 1.

The forward I–V characteristics of the $CoSi_2$/Si contact grown by the one-step annealing procedure at 1000°C for 30 s show excess currents in the low bias region at low temperatures as observed in the polycrystalline $CoSi_2$/Si contacts (Fig. 2(a)). It is consistent with the fact that the M–S interface of the $CoSi_2$/Si

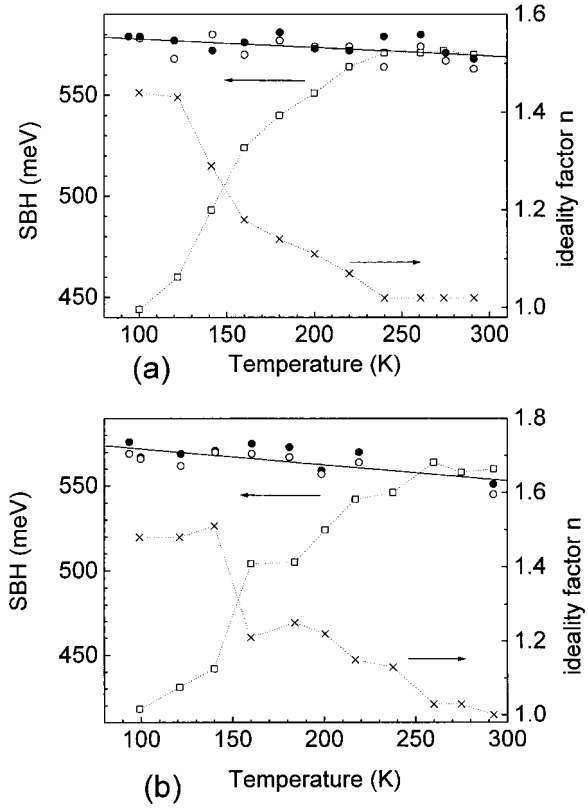

Fig. 6. Values of Φ^{I-V}, Φ^{C-V} and n as a function of temperature for two epitaxial $CoSi_2$/Si diodes which were made by reaction of Co(5 nm)/Ti(3 nm)/Si with a final annealing at (a) 800°C, (b) 900°C for 60 s, (○) Φ^{C-V}, 100 KHz, (●) Φ^{C-V}, 500 KHz, (□) Φ^{I-V}, (×) n.

contact grown by the one-step annealing procedure is not as smooth as that grown by the two-step annealing procedure as observed by XTEM [8,18]. In Table 1, the fitting data for these contacts are listed.

3.3. Polycrystalline $CoSi_2$/Si diodes grown from Ti/Co/Si systems

The above results show that the SBH of epitaxial $CoSi_2$/Si contacts grown by the Co/Ti/Si reaction is significantly lower than that of polycrystalline ones grown by Co/Si reaction. To distinguish if this is due to the nature of the $CoSi_2$ film (polycrystalline or epitaxial) or due to the influence of the Ti atoms, a $CoSi_2$/Si contact was fabricated by reaction of a Ti/Co/Si system with a final annealing at 800°C for 60 s. The resulting $CoSi_2$ film is polycrystalline with a preferred (2 2 0) orientation and contains Ti atoms as those grown from the Co/Ti/Si reaction [25]. The values of Φ_0^{C-V} and $\overline{\Phi}_{B0}$ are 565 and 571 meV, respectively. This is close to the SBHs

of the epitaxial $CoSi_2$/Si contacts grown from the Co/Ti/Si reaction. It reveals that it is the Ti incorporation that reduces the barrier height of the $CoSi_2$/Si contacts. Secondary ion mass microscopy (SIMS) also showed that there are Ti atoms in the $CoSi_2$ films formed from Co/Ti/Si reactions [26].

3.4. Epitaxial $CoSi_2$/Si diodes grown from Ti/Co/SiO_2/Si systems

It has been reported recently that an epitaxial $CoSi_2$ film can also be obtained by ex situ annealing of the Ti/Co/SiO_2/Si system due to the fact that Ti from the capping layer can diffuse through the unreacted Co and transform the interfacial SiO_2 diffusion barrier into a $Co_xTi_yO_z$ diffusion membrane [4–6]. Fig. 7 shows the forward I–V characteristics of a diode grown from Ti(5 nm)/Co(5 nm)/SiO_2/Si with annealing at 800°C for 30 s. The measured data can be fitted by Eqs. (1a) and (1b) quite well in the whole temperature range. This reveals that the $CoSi_2$/Si interface is quite homogeneous. The C–V characteristics are similar to those shown in Fig. 2 (b). The values of Φ^{C-V}, Φ^{I-V} and n, which are obtained from the C–V and I–V data, are displayed in Fig. 8(a) as a function of temperature. The value of Φ^{C-V} is about 593 meV and is almost independent on temperature, i.e., $\alpha_{\Phi}^{C-V} \approx 0$ meV K^{-1}. From the plot of $\Phi^{C-V} - \Phi^{I-V}$ versus $1/T$ and the modified Richardson plot shown in Fig. 8(b) and (c), the values of σ_0, α_σ, $\overline{\Phi}_{B0}$ and A^* are 64 meV, -0.11 meV K^{-1}, 590 meV and 40 A cm^{-2} K^{-2}, respectively.

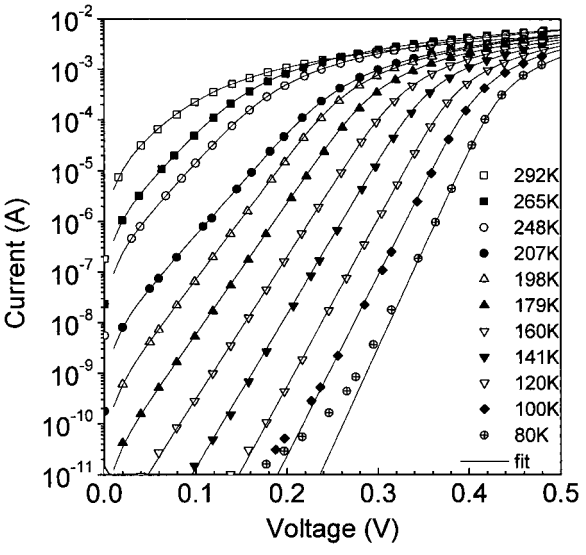

Fig. 7. Forward I–V characteristics of an epitaxial $CoSi_2$/Si diode with an area of 0.61 mm^2 in the temperature range of 80 to 292 K. The $CoSi_2$ layer was made by reaction of Ti(5 nm)/Co(5 nm)/SiO_2/Si with annealing at 800°C for 30 s.

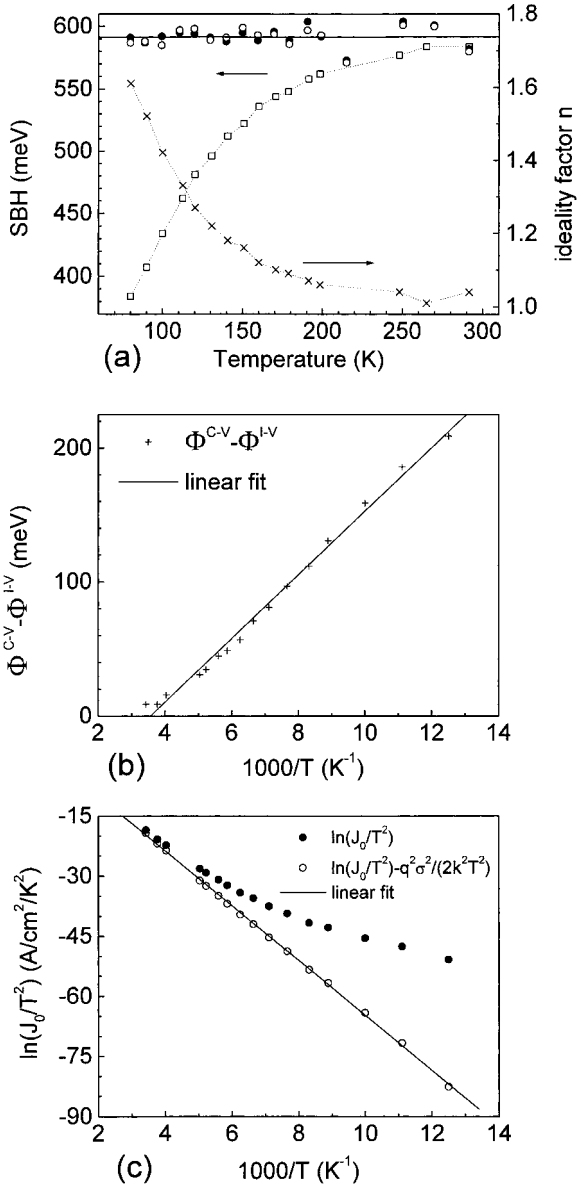

Fig. 8. The results of an epitaxial $CoSi_2$/Si diode formed by reaction of Ti(5 nm)/Co(5 nm)/SiO_2/Si with annealing at 800°C for 30 s. (a) Φ^{I-V}, Φ^{C-V} and n versus T, (○) Φ^{C-V}, 100 KHz, (●) Φ^{C-V}, 500 KHz, (□) Φ^{I-V}, (×) n; (b) $\Phi^{C-V} - \Phi^{I-V}$ versus $1/T$; (c) $\ln(J_0/T^2)$ versus $1/T$.

The $CoSi_2$/Si contact fabricated from a Ti(10 nm)/Co(10 nm)/SiO_2/Si system with annealing at 800°C has similar ideal I–V characteristics. But increasing the annealing temperature to 1000°C influences significantly the I–V characteristics. A double threshold phenomenon at low temperatures is observed. The excess current in

the low bias region and at low temperatures indicates that there exist large patches with low SBH at the M–S interface. The diode made from the Ti(5 nm)/Co(5 nm)/SiO_2/Si system by annealing at 1000°C also has such double threshold phenomenon. It is consistent with the phenomenon reported by Kim et al. [27] that the leakage current density for the silicidation temperature of 900°C was much higher than for silicidation at 800°C, which may be attributed to the reaction between the upper layer consisting of Co/Ti/Si and the $CoSi_2$ layer at the higher annealing temperature. The values of the electrical measurements are given in Table 1.

4. Discussion

The $CoSi_2$/Si contacts grown from different multilayer structures show significantly different SBH properties. The main results for various contacts are summarized in Table 1 for comparison. For all samples, the barrier heights determined from the C–V data are in good agreement with those derived from the modified Richardson plots, which are almost linear at the whole temperature range. Moreover, the effective Richardson constant derived from the intercept of the plot with the ordinate is close to its theoretical value. The above results reveal that the assumption of a Gaussian distribution of barrier heights [13] can explain the experimental data quite well in the whole temperature region except the double threshold phenomenon in the I–V characteristics at low temperatures observed in some $CoSi_2$/Si diodes. Our previous BEEM measurements have directly shown the presence of an approximate Gaussian distribution made up by several hundred local SBHs, randomly spread over an ultrathin $CoSi_2$/Si contact area [9,16]. A similar distribution was also reported by Palm et al. [28] and Detavernier et al. [29] on Au/Si contacts using the BEEM technique. In the literature, a Gaussian distribution of SBHs has been used to analyze the anomalous behavior of the I–V and C–V characteristics for various MS contacts, such as Al/p-InP [13], PtSi/n-Si [12], PtSi/p-Si [15] and Pd_2Si/Si [14] etc. The barrier height inhomogeneity may be attributed to the variation in thickness and composition of the silicide layer, non-uniformity of the interfacial charges and local defects. It is known that the TIME or OME grown epitaxial $CoSi_2$/Si interface contains various terraces connected by steep steps, which can cause the barrier height inhomogeneity. Crystalline defects in $CoSi_2$ films also lead to SBH inhomogeneity. Sirringhaus et al. reported that the barrier height near a dislocation of a molecular beam epitaxy (MBE) grown $CoSi_2$ film on n-Si(1 0 0) is lower than that on the surrounding dislocation-free region [30]. It shows that fluctuations in barrier heights are unavoidable as they exist even in the most carefully fabricated MS contacts.

However, the above model of the Gaussian distribution of SBHs cannot explain the double threshold behavior which has been observed in some $CoSi_2$/Si contacts at low temperatures. Such phenomenon has been explained by the pinch-off model quantitatively [16,19]. Moreover, the above model is not satisfactory in the whole temperature range if the standard deviation of the Gaussian distribution is temperature independent [31]. In this paper, the temperature dependence of σ is introduced (Eq. (5)). Its temperature coefficient (α_σ), which is determined based on Eq. (8) in this work, is between -0.07 to -0.14 meV K^{-1} (Table 1). The physical meaning of the negative values of α_σ can also be understood by the pinch-off model [11]. For a small patch of the interface that has a lower barrier height than the surrounding region by an amount Δ, the effective barrier height measured at the center of the patch will display much less drop than Δ if the patch size is smaller than the width of the depletion region. The effective reduction (Δ_{eff}) for a circular patch can be calculated by [11]

$$\Delta_{\mathrm{eff}} = 3[qN_{\mathrm{d}}R_0^2\Delta(\Phi_{\mathrm{B0}} - V_{\mathrm{n}} - V)/(4\varepsilon_{\mathrm{s}})]^{1/3}, \tag{10}$$

where R_0 is the patch radius and ε_{s} is the permittivity of Si. $V_{\mathrm{n}} = (kT/q)\ln(N_{\mathrm{C}}/N_{\mathrm{d}})$ is the semiconductor Fermi level in the neutral region, which increases with increasing temperature, so that the value of Δ_{eff} decreases. For example, a circular patch with $R_0 = 10$ nm and $\Delta = 400$ meV displays a drop of $\Delta_{\mathrm{eff}} \approx 112$ meV at 100 K and approximately 100 meV at 300 K in our cases ($\Phi_{\mathrm{B0}} = 0.60$ eV and $N_{\mathrm{d}} = 1 \times 10^{16}$ cm^{-3}). A real MS contact may contain many patches with various Δ and R_0. One can expect that the amount of large patches (both Δ and R_0) is significantly smaller than that of small patches [16,19]. At low temperatures and in the low bias region, the I–V characteristics may be dominated by a few large patches with low barriers, thus a double threshold phenomenon is obvious since the current through the patches saturates at relatively low bias due to the large spreading resistance. At high temperatures or in the large bias region at low temperatures, the total current is dominated by a large number of small patches, which can be approximately described as a Gaussian distribution of the barrier heights [16]. Due to the pinch-off model, the barrier heights appear more homogeneous than they actually are, which leads to similar values of σ_0 for all $CoSi_2$/Si contacts (between 58–78 meV, see Table 1). According to Eq. (10), Δ_{eff} decreases with increasing temperature, thus the barrier heights appear more uniform at higher temperatures. Furthermore, Aniltürk et al. suggested that the current through the patches may be dominated by tunneling [31]. The effect of the patches also gradually decreases as

the temperature increases. Both of them lead to $\alpha_\sigma < 0$. At high temperatures (above about 220 K), the tunneling effect is negligible and the value of σ is small, thus the I–V characteristics are nearly ideal.

The temperature dependence of the apparent ideality factor can be explained by the bias dependence of both the mean barrier height and the standard deviation [12,16,22]:

$$1/n = 1 - \rho_1 + q\sigma_s(T)\rho_2/(kT) \approx 1 - \rho_1 + q\rho_2\alpha_\sigma/k + q\sigma_{s0}\rho_2/(kT), \quad (11)$$

where ρ_1 and ρ_2 are the coefficients of the voltage dependence of Φ_B and σ_s, respectively. A plot of $(1/n) - 1$ versus $1/T$ should yield a straight line with an y-axis intercept and a slope which depend on ρ_1 and ρ_2. Fig. 9 shows such a plot for four $CoSi_2$/Si diodes which were grown from the different multilayer structures. Other diodes also have such nearly linear behavior. By linear least square fitting the data, the voltage coefficients ρ_1 and ρ_2 can be derived as $\rho_1 \approx -0.02$ to -0.07 and $\rho_2 \approx -0.05$ to -0.07 for all diodes listed in Table 1. (The values of σ_{s0} and α_σ which are listed in Table 1 are used to calculate ρ_1 and ρ_2.) There is no single dependence between the $CoSi_2$ properties and the values of ρ_1 and ρ_2. The physical meaning of the negative bias coefficient of the standard deviation ($\rho_2 < 0$) can be understood by the pinch-off model. According to Eq. (10), Δ_{eff} decreases with increasing the bias voltage, thus the barrier heights appear more uniform.

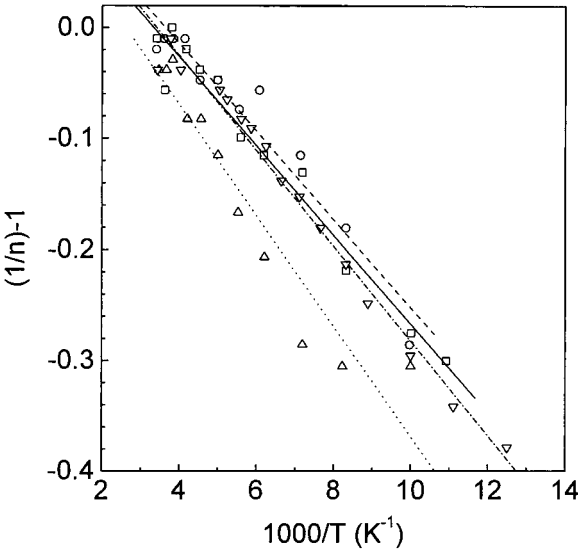

Fig. 9. $(1/n)-1$ versus $1000/T$ plots of four $CoSi_2$/Si diodes, (□) polycrystalline $CoSi_2$ grown by Co(20 nm)/Si with a final annealing at 800°C for 60 s, (○) epitaxial $CoSi_2$ grown by Co(5 nm)/Ti(3 nm)/Si with a final annealing at 700°C for 60 s, (Δ) polycrystalline $CoSi_2$ grown by Ti(5 nm)/Co(5 nm)/Si with a final annealing at 800°C for 60 s, (▽) epitaxial $CoSi_2$ grown by Ti(5 nm)/Co(5 nm)/SiO_2/Si with annealing at 800°C for 30 s.

The epitaxial $CoSi_2$/Si contacts grown from the bilayer metals (Co, Ti) and Si have significantly lower SBH than the polycrystalline $CoSi_2$/Si contacts grown from the Co/Si direct reaction (Table 1). Such behavior is also observed from the BEEM measurements [16]. In this paper, we find that the barrier height of a polycrystalline $CoSi_2$/Si contact which was grown from the Ti/Co/Si reaction is closer to that of the epitaxial $CoSi_2$/Si contacts than that of the polycrystalline $CoSi_2$/Si contacts. Also noticing that the barrier height of Ti/Si contacts is lower than that of $CoSi_2$/Si contacts [32], one may attribute the lowering of the barrier height to Ti incorporation into the $CoSi_2$ film. Using SIMS, Lauwers found that the Ti is homogeneously distributed in the $CoSi_2$ film and its concentration is about 0.1%, depending on the relative thickness of the Ti film for a Co/Ti/Si system after silicidation and selective etch [26]. In our experiments, we find that the barrier height of a $CoSi_2$/Si contact grown from a Ti–Co bilayer with thicker Ti layer is slightly lower than that grown with a thinner Ti layer. Furthermore, in the case of the Co(5 nm)/Ti(3 nm)/Si reaction, the barrier height increases from 0.54 to 0.58 eV by increasing the annealing temperature from 700°C to 800°C, while further increases of the annealing temperature have no influence on the barrier height. This phenomenon can be understood by the reaction mechanism of a Co/Ti/Si system. Co diffuses through the Ti interlayer to react with the substrate Si upon annealing. After annealing at 700°C for 60 s, the M–S interface may be still dominated by the Ti, thus the barrier height is closer to that of the Ti/Si contact (≈0.50 eV). Increasing the annealing temperature speeds up the reaction. When the inversion of Ti and Co layer is totally completed, the M–S interface is just $CoSi_2$/Si and the SBH remains constant for higher annealing temperatures.

Table 1 also shows the significant difference in the temperature coefficients of the barrier height for various $CoSi_2$/Si contacts. The temperature dependence of the SBH is normally explained within the frame of the Fermi level pinning concept [21]. According to the band to which the Fermi level is pinned, the temperature coefficient varies from 0 to dE_g^i/dT, where E_g^i is the energy gap of Si. In the temperature range between 90–300 K, the value of dE_g^i/dT is about -0.2 meV K^{-1} [33]. Our results show that the temperature coefficient of polycrystalline $CoSi_2$ grown by Co/Si reaction is between $1/2\ dE_g^i/dT$ and dE_g^i/dT, suggesting that the Fermi level is partially pinned to the valence band edge of Si. On the other hand, the near zero temperature coefficient of $CoSi_2$ grown by OME (Table 1) suggests pinning to the conduction band edge for these contacts. For the case of the Co/Ti/Si reaction, we find the tendency of an increasing temperature coefficient from ≈0 to

$\approx 1/2\ dE_g^i/dT$ with increasing the annealing temperature. The temperature coefficients of SBH on Si have been correlated to the chemical nature of the contact metal [21] or the metal electronegativity [34]. Our results reveal that the $CoSi_2$ films grown from different multilayer structures have different interfacial properties.

5. Conclusion

The model of a Gaussian distribution of SBHs was used to analyze the *I–V*/*C–V* data measured in the temperature range 90–300 K for various $CoSi_2$/Si contacts which were fabricated by solid state reaction of Co/Si, Co/Ti/Si, Ti/Co/Si and Ti/Co/SiO_2/Si systems. After introducing a temperature dependence of the standard deviation, the model can describe the experimental data satisfactorily in the whole temperature range. In all cases, the barrier heights obtained from the *C–V* data are in good agreement with those derived from the modified Richardson plots, and the effective Richardson constant deduced from the intercepts of these plots with the ordinate is in close agreement with its theoretical value. The $CoSi_2$/Si contacts fabricated from different multilayer structures have significantly different values of both the mean barrier height itself and its temperature coefficient. The lowering of the barrier height for TIME or OME (with a Ti capping layer) grown epitaxial $CoSi_2$/Si contacts is attributed to the Ti incorporation into the $CoSi_2$ films. The temperature coefficient of the mean SBH varies from approximately $-0.16\ meV\,K^{-1}$ for polycrystalline $CoSi_2$ to $\sim 0\ meV\,K^{-1}$ for the OME grown epitaxial $CoSi_2$/Si contacts. This shows that the band to which the Fermi level is pinned is different for various $CoSi_2$/Si contacts grown from different multilayer structures. On the other hand, the standard deviation of the Gaussian distributions and their temperature coefficients are of the same order of magnitude for all samples. The decrease of the standard deviation with increasing temperature, as well as the double threshold behavior in the *I–V* characteristics at low temperatures, could be explained by the pinch-off model.

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References

[1] Maex K, Lauwers A, Besser P, Kondoh E, dePotter M, Steegen A. IEEE Trans Electron Dev 1999;46(7):1545–50.
[2] Liu P, Li BZ, Shen Z, Gu ZG, Wang WN, Zhou ZY, Ni RS, Lin CL, Zou SC, Hong F, Rozgonyi GA. J Appl Phys 1993;74(3):1700–6.
[3] Tung RT. Appl Phys Lett 1996;68(24):3461–3.
[4] Detavernier C, Van Meirhaeghe RL, Cardon F, Donaton RA, Maex K. Appl Phys Lett 1999;74(20):2930–2.
[5] Kim GB, Kwak JS, Baik HK, Lee SM. J Appl Phys 1999;85(3):1503–7.
[6] Kim GB, Kwak JS, Baik HK, Lee SM. J Vac Sci Techn B 1999;17(1):162–5.
[7] Lauwers A, Larsen KK, van Hove M, Verbeeck R, Maex K, Vercaemst A, Van Meirhaeghe RL, Cardon F. J Appl Phys 1995;77(6):2525–36.
[8] Hatzikonstantinidou S, Wikman P, Zhang SL, Petersson CS. J Appl Phys 1996;80(2):952–61.
[9] Zhu SY, Detavernier C, Van Meirhaeghe RL, Qu XP, Cardon F, Ru GP, Li BZ. Semicond Sci Technol 2000; 15:349–56.
[10] Rhoderick EH, Williams RH. Metal-Semiconductor Contacts. 2nd ed. Oxford: Clarendon Press; 1988 [chapter 3].
[11] Tung RT. Phys Rev B 1992;45(23):13509–23.
[12] Werner JH, Güttler HH. J Appl Phys 1991;69(3):1522–33.
[13] Song YP, Van Meirhaeghe RL, Laflere WH, Cardon F. Solid-State Electron 1986;29(6):633–8.
[14] Chand S, Kumar J. J Appl Phys 1996;80(1):288–94.
[15] Mccafferty PG, Sellai A, Dawson P, Elabd H. Solid-State Electron 1996;39(4):583–92.
[16] Zhu SY, Van Meirhaeghe RL, Detavernier C, Cardon F, Ru GP, Qu XP, Li BZ. Solid-State Electron 2000;44(4): 663–71.
[17] Ishizaka A, Shiraki Y. J Electrochem Soc 1986;133(4):666–71.
[18] Schreutelkamp RJ, Coppye W, De Bosscher W, Van Meirhaeghe RL, Van Meirhaeghe L, Vanhellemont J, Deweerdt B, Lauwers A, Maex K. J Mater Res 1993; 8(12):3111–21.
[19] Lahnor P, Seiter K, Schulz M, Dorsch W, Scholz R. Appl Phys A 1995;61(4):369–75.
[20] Wittmer M. Phys Rev B 1991;43(5):4385–95.
[21] Werner JH, Güttler HH. J Appl Phys 1993;73(3):1315–9.
[22] Chand S, Kumar J. J Appl Phys 1997;82(10):5005–10.
[23] Ru GP, Liu J, Qu XP, Li BZ, Detavernier C, Van Meirhaeghe RL, Cardon F. International Conference on solid state and integrated circuit technology proceedings. Beijing, China, 1998. p. 271.
[24] Vantomme A, Nicolet MA, Theodore ND. J Appl Phys 1994;75(8):3882–91.
[25] Detavernier C, Van Meirhaeghe RL, Cardon F, Donaton RA, Maex K. Microelectron Engng 2000;50:125–32.
[26] Lauwers A, PhD Thesis. IMEC, Leuven, Belgium, 1995.
[27] Kim GB, Kwak JS, Baik HK, Lee SM. J Appl Phys 1997;82(5):2323–8.

[28] Palm H, Arbes M, Schulz M. Phys Rev Lett 1993; 71(14):2224–7.
[29] Detavernier C, Van Meirhaeghe RL, Donaton R, Maex K, Cardon F. J Appl Phys 1998;84(6):3226–31.
[30] Sirringhaus H, Meyer T, Lee EY, von Känel H. Phys Rev B 1996;53(23):15944–50.
[31] Aniltürk ÖS, Turan R. Solid-State Electron 2000;44:41–8.
[32] Aboelfotoh MO. J App Phys 1988;64(8):4046–55.
[33] Bludau W, Onton A, Heinke W. J Appl Phys 1974; 45(4):1846–8.
[34] Aboelfotoh MO. Solid-State Electron 1991;34(1): 51–5.