Analysis of GaAs Schottky/tunnel metal–insulator–semiconductor diode characteristics based on an interfacial layer model

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Current-voltage (I-V) characteristics of GaAs Schottky and tunnel metal–insulator–semiconductor diodes were measured at various temperatures between 100 and 400 K and analyzed on a basis of an interfacial layer model recently proposed by Maeda, Umezu, Ikoma, and Yoshimura [J. Appl. Phys. **68**, 2858 (1990)]. The ideality factor n obtained from the forward I-V characteristics increased from about 1.05–1.1 to 2–3 as the temperature was decreased from 400 to 100 K. This could be interpreted as an increase in the electron occupation ratio of the interface states with decreasing temperatures. Precise measurement of the n value of the I-V curve revealed anomalous behavior as a function of the forward current, which was not observed in either amorphous or crystalline Si Schottky diodes. This seems to be related to the presence of a density peak in the interface state distribution like those proposed by Spicer, Newman, Spinat, Liliental-Weber, and Weber, [J. Vac. Sci. Technol. A **8**, 2084 (1990)]. The interfacial Fermi level was demonstrated to move from the metal Fermi level as applied voltage is increased, but it hardly moved relative to the conduction band bottom. This is considered to be the first direct evidence of Fermi level pinning in I-V characteristics.

I. INTRODUCTION

There have been many investigations[1–5] on metal–semiconductor Schottky barrier diode characteristics. Experimental current-voltage (I-V) characteristics of Schottky diodes always deviate from ideal ones calculated from the thermoionic and diffusion theories. For explanations of these deviations, the effects of interfacial film and/or interface states between this film and the semiconductor, have so far been discussed. Such an interfacial insulative film is unavoidably formed between the metal and the semiconductor during usual diode fabrication and the localized electronic states ordinarily exist at the interface between this film and the semiconductor. Recent understanding of these subjects was reviewed in Ref. 1.

Some models have been presented[6–11] in which Schottky barrier height was modified by an applied voltage due to the presence of interface states. In these models, the electron population of the interface states was assumed to have been changed by applied bias voltage. Due to this electron population in the interface states, the space charge within the semiconductor and the potential drop across the interfacial layer changed. Accordingly, the Schottky barrier height was varied. Deviations from the ideal I-V characteristics were attributed to this change of Schottky barrier height with applied voltage.

Cowley and Sze[6] and Crowell *et al.*[7,8] discussed the effects of the interfacial states on I-V characteristics of Schottky diodes on a basis of one of such models. They assumed that all the interface states were nearly in thermal equilibrium only with the metal.

Card and Rhoderick[9] calculated I-V characteristics of a Schottky diode based on their model in which the interface states were subdivided into two groups. One of these groups readily communicates and is in thermal equilibrium only with the metal and the other group only with the semiconductor. Only electrons occupying the former group of interface states tunnel through the thin interfacial film to the metal. However, it might be more reasonable to assume that all of the interface states exchange electrons with both the conduction band of semiconductor and metal Fermi level, that is, they communicate with both metal and semiconductor.

Very recently, Maeda *et al.*[12] proposed a model in which all the interface states communicate both with metal and semiconductor and the interface Fermi level is determined by occupation of the interface states by electrons. The position of the interface Fermi level is determined by a balance between a capture and release of electrons in the interface states from and to the conduction band and the metal. This model was based on a nearly constant density of the interface states over an energy range of interest. It was reported that the interface Fermi level thus moves between the metal Fermi level and the bulk Fermi level of the semiconductor as the electron population of the interface states is changed with applied voltage. They analytically derived the I-V characteristics based on this model. This model could well interpret nonideal I-V characteristics of a-Si:H Schottky diodes[12] and also single crystalline Si Schottky diodes.[13]

As for the compound semiconductor like GaAs, it is known that a very high density of interface or surface states exists. The Fermi level pinning is known to be caused by such a high interface state density.[14–20] The origin of the Fermi level pinning has long been a subject of many investigations.[14,15,17–20] Concerning the Fermi level pinning, an energy distribution of the interface states in the semicon-

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ductor band gap is also of fundamental importance. A U-shaped interface state distribution has widely been believed for both Si and compound semiconductors.[15] However, many papers reported existence of a density peak or peaks at an intermediate energy position or positions in the interface state distribution in GaAs. For example, Spicer *et al.*[14] observed density peaks at energy positions of 0.75 and 0.9 eV from the valence band maximum in GaAs surface states from their measurements of photoemission on (110) cleaved-surface samples. They then proposed the defect-induced gap state (DIGS) model as the origin of the Fermi level pinning.[14]

There have been no reports on a relation between the Fermi level pinning and the I-V characteristics of GaAs Schottky diode.

It is therefore interesting to apply our model[12] to an analysis of I-V characteristics of GaAs Schottky diodes at various temperatures. Anomalous behaviors of the electron occupation ratio of the interface states deduced from the I-V characteristics would indicate large variation in the distribution of the interface states.

In the present study, I-V characteristics of GaAs Schottky diodes were measured at various temperatures between 100 and 400 K. The employed samples include those made on intentionally oxidized substrates. The experimental results were analyzed on the basis of our model.

Experimental procedures are presented in Sec. II. The model and method of analysis used here are briefly presented in Sec. III. Experimental results are analyzed and discussed in Sec. IV. Finally a summary and conclusions are given in Sec. V.

II. EXPERIMENTAL PROCEDURES

A. Sample preparations

Horizontal Bridgeman (HB)-grown n-type GaAs (100) substrates with a room-temperature carrier concentration of around 1×10^{17} cm^{-3} were employed throughout the experiments. Free carrier concentration was estimated from the capacitance-voltage (C-V) characteristics at a frequency of 1 MHz. GaAs substrates were sequentially cleaned by ultrasonic washing in trichloroethylene, acetone, and deionized water in this order. Substrates were then soaked in an HCl solution to remove the native oxide and rinsed in deionized water. Ohmic contact was formed by evaporating Au-Ge alloy on a back side surface of substrate and annealing at 350 °C in a nitrogen atmosphere. After that, the same surface treatments were again performed to eliminate contaminations and native oxide on the front surface of the substrate. A Schottky barrier contact was then quickly formed by evaporating Au, Al, Ag, and Ni through a metal mask in a vacuum of about $1\sim2\times10^{-6}$ Torr. The Schottky contact used in the present study was rectangular in shape with each side equal to 1 mm. Thin native oxide films were inevitably formed during preparations. However, these samples are hereafter referred to as "nonoxidized" samples.

Adding to the above standard samples, several kinds of Schottky [tunnel metal–insulator–semiconductor device (MIS)] diode samples were prepared using substrates on which very thin oxide films were intentionally grown using various oxidation techniques. Included were samples of native oxide, chemical oxide, and thermal oxide. In making the native oxide samples, GaAs substrates were exposed to ambient air in the laboratory for about one day after the above stated surface treatment. Chemical oxides were grown by immersing the GaAs substrates in room-temperature de-ionized water for one day or in boiling deionized water for 60 min. The thermal oxide samples were fabricated by thermal oxidation of the GaAs substrates in a dry oxygen (100%) atmosphere at 500 °C for 5 or 10 min. In any case, Schottky metal was evaporated on the grown oxide. A check of preparation and environment has been made by fabricating Si metal–oxide–semiconductor (MOS) diodes and measuring their flat band voltage from C-V characteristics.[13]

B. Measurements

The detailed measurements of the current-voltage (I-V) characteristics were automatically and continuously conducted at various temperatures between 100 and 400 K with a digital electrometer controlled by a personal computer. Measurements were made for the Schottky diodes of different sizes on a same sample chip. The measured current was nearly proportional to the contact area at a constant applied voltage so that the leakage current at the diode periphery was negligible. From the forward I-V characteristics, an ideality factor n was computed as a function of the applied voltage using a personal computer.

III. THEORETICAL MODEL AND METHOD OF ANALYSIS

In this section, the model of a nonideal Schottky barrier proposed by us[12] is first described as a basis of the method of analysis of experimental results. In this model, it is first assumed that the deviation from the ideal I-V characteristics can be attributed to the change of the barrier height due to the change of space charge in the interface states under the applied voltage. The electron concentration at the top of the barrier is considered to be in thermal equilibrium with the bulk semiconductor.

In Ref. 12, effects of the space charge in the depletion region and voltage across the interface layer were not apparently taken into consideration. However, a contribution of the depletion layer to the nonideality in the presence of interfacial layer can be proven to be very small and is neglected hereafter.

In the present model, metal and semiconductor are separated by an insulative layer of thickness δ and dielectric constant ϵ_i. Localized electronic states of density D_s are present at the insulator–semiconductor interface. Here, D_s is considered not to depend strongly on its energy level in the interface.

An energy band diagram of a Schottky barrier under the forward applied voltage is shown in Fig. 1.

Schottky barrier height ϕ_B^0 at zero bias voltage is well known to be represented by[6]

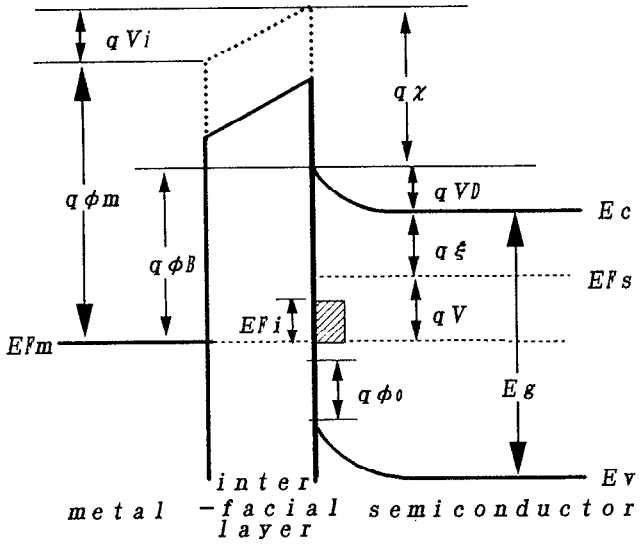

FIG. 1. Energy band diagram of Schottky barrier with interfacial layer under forward bias voltage. Various quantities are defined. Shaded area indicates the electron population in the interface states constituting space charge. Broken line in the interfacial layer represents the vacuum level.

$$\phi_B^0=\gamma(\phi_m-\chi)+(1-\gamma)\left(\frac{E_g}{q}-\phi_0\right) \tag{1}$$

where

$$\gamma=\frac{1}{1+(qD_s\delta/\epsilon_i)}. \tag{2}$$

Here, ϕ_m is a metal work function, χ is an electron affinity of the semiconductor, E_g is a band gap energy of semiconductor, q is an electronic charge, ϕ_0 is a neutral level of the interface states, and D_s is the interface state density in $\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$. The barrier height changes with the space charge in the interface states; i.e., $\phi_B^0=\phi_m-\chi$ when $D_s=0$ and $\gamma=1$, and $\phi_B^0=(E_g/q)-\phi_0$ when $D_s=\infty$ and $\gamma=0$. When the bias voltage is applied, a difference in the Fermi level occurs between the bulk semiconductor and the metal. Then the interface states between the two Fermi levels are populated with electrons. This space charge induces changes in the voltage V_i across the interfacial layer and the conduction band bending. Therefore, this change of space charge induces the variation of Schottky barrier height $\Delta\phi_B$ with applied voltage V. A change of Schottky barrier height $\Delta\phi_B$ due to applied voltage V is given by[12,13]

$$\Delta\phi_B=\phi_B-\phi_B^0=(1-\gamma)\frac{D_{Sb}}{D_s}V, \tag{3}$$

where D_{Sb} is an average density of occupied interface states between E_{Fi} and E_{Fm} due to the applied voltage in $\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$. Here, E_{Fi} and E_{Fm} are Fermi levels of the interface states and the metal, respectively.

The change of population in the interface states depends on the communication probability of the interface states with two Fermi levels, i.e., those of metal E_{Fm} and bulk semiconductor E_{Fs}. If the interface states more readily communicate with the metal and are nearly in thermal equilibrium with the metal, the interface Fermi level E_{Fi} defined below always coincides with that of the metal E_{Fm} under an arbitrary applied voltage. On the contrary, provided that the interface states more readily communicate with and are in thermal equilibrium with the semiconductor, E_{Fi} coincides with the bulk Fermi level E_{Fs} of the semiconductor as the bias voltage is varied.

Actually, all of the interface states are considered to communicate with both metal and semiconductor. Thus, the interface Fermi level E_{Fi} is always between those of metal E_{Fm} and semiconductor E_{Fs}. E_{Fi} can be defined by the electron occupation ratio of the interface states between E_{Fm} and E_{Fs} and is represented by[12]

$$E_{\mathrm{Fi}}-E_{\mathrm{Fm}}=q\frac{D_{Sb}}{D_s}V. \tag{4}$$

The interfacial Fermi level $(q\phi_B-E_{\mathrm{Fi}})$ relative to the conduction band edge at the interface can be written as

$$q\phi_B-E_{\mathrm{Fi}}=q\phi_B-q\frac{D_{Sb}}{D_s}V=q\phi_B^0-q\gamma\frac{D_{Sb}}{D_s}V, \tag{5}$$

by taking into account the change in Schottky barrier height due to the applied voltage from Eqs. (3) and (4).

The occupation ratio D_{Sb}/D_s can be represented as a function of the electron concentration n_s (cm^{-2}) at the top of the Schottky barrier by

$$\frac{D_{Sb}}{D_s}=\frac{Cn_s}{B^*+\nu\exp(-U/kT)+Cn_s}, \tag{6}$$

where B^* is a tunneling probability (s^{-1}) of electrons from the interface states to the metal, ν is an attempt-to-escape frequency (s^{-1}) of the thermal release of electrons from the interface states to the conduction band, U is an activation energy of the thermal release, and C is a capture coefficient $(\mathrm{cm}^2\,\mathrm{s}^{-1})$ of electrons by the interface states from the conduction band. Current I of a Schottky diode is proportional to n_s. Thus D_{Sb}/D_s is a function of the current I and changes with applied voltage V.

By comparing the calculated forward I-V characteristics with the conventional I-V equation involving the well-known ideality factor n, the following relation between n and D_{Sb}/D_s was obtained:[12]

$$\frac{D_{Sb}}{D_s}=\frac{1}{1-\gamma}\frac{n-1}{n}. \tag{7}$$

Equation (7) is one of the most important relations in the present model. The occupation ratio D_{Sb}/D_s was calculated from this equation using the experimental value of γ and n. γ is estimated by a slope in a plot of the Schottky barrier height ϕ_B^0 at zero bias voltage versus the metal work function ϕ_m according to Eq. (1). The ideality factor n was obtained as a function of the applied voltage by computer calculation of slopes of the experimental forward I-V characteristics at each applied voltage. Analyses were only performed for the data at low voltages where the effect of the series resistance was negligible. The interface Fermi level E_{Fi} was obtained from D_{Sb}/D_s and γ from Eqs. (4) and (5) as a function of the applied voltage.

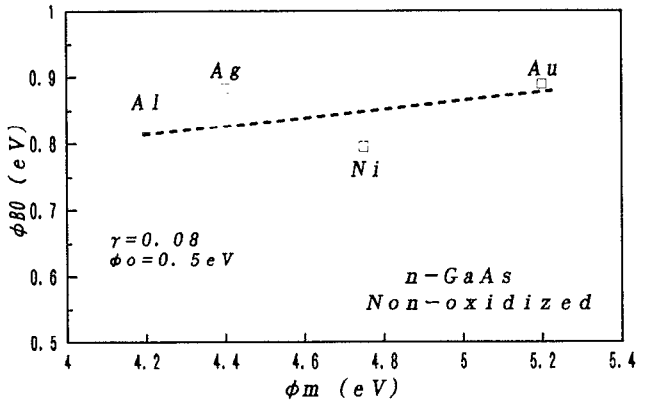

FIG. 2. Relation between Schottky barrier height ϕ_B^0 at zero bias voltage and metal work function ϕ_m for nonoxidized GaAs Schottky samples. γ was derived from this relation using Eq. (1).

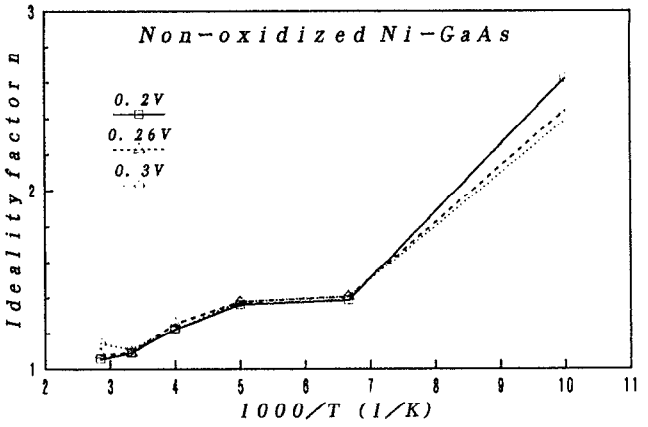

FIG. 3. Temperature dependence of the ideality factor n of the forward I-V characteristics for nonoxidized Ni-GaAs Schottky diode samples at various applied voltages between 0.2 and 0.3 V.

IV. ANALYSIS AND DISCUSSION OF EXPERIMENTAL RESULTS

A. Schottky barrier parameters at zero bias voltage

Schottky barrier height ϕ_B^0 at zero bias voltage was obtained as usual from the forward I-V characteristics of nonoxidized samples. The Richardson constant A^* was taken to be 8.16×10^4 (A m^{-2} K^{-2}). In Fig. 2, ϕ_B^0 is plotted as a function of the metal work function $\phi_m$for nonoxidized Schottky diode samples. Although the data are somewhat scattered, the value of γ was obtained by a least squares fitting to Eq. (1) to be about 0.08. In other sample groups stated in Sec. II, γ values were calculated in the same manner to be 0.07–0.13. These values are much smaller than those of other Schottky barriers such as a-Si and c-Si, suggesting that the Fermi level pinning takes place at or near the neutral level ϕ_0 of the interface states at zero bias voltage.

The neutral level ϕ_0 of the interface states was determined using Eq. (1) to be about 0.5 eV from the valence band maximum. This is about one-third of the GaAs bandgap (1.42 eV at room temperature).

In order to obtain the interface state density D_s from Eq. (2), the interfacial layer thickness δ and dielectric constant ϵ_i should be known. Though these values are not exactly known, it is assumed hereafter for the case of Si[3,13] that δ and ϵ_i are about 20 Å and ϵ_0, respectively, where ϵ_0 is the dielectric constant of vacuum. The interface state density D_s was then roughly estimated from Eq. (2) to be about $(6\pm4)\times10^{13}$ eV^{-1} cm^{-2}. These values seem to be reasonable considering the above uncertainty.

B. Analysis of the forward *I-V* characteristics

1. Nonoxidized samples

In nonoxidized samples, the ideality factor n only slightly changes with the increase of the applied voltage V. However, it always increases with a decrease in temperature T from 400 to 100 K. An example of the n versus reciprocal temperature $1/T$ relation is exhibited in Fig. 3 for various applied voltages between 0.2 and 0.3 V for the nonoxidized Ni-GaAs Schottky sample.

The increase in the ideality factor n at lower temperatures can be understood as follows. From Eq. (7), n is written as[12]

$$n=\left(1-(1-\gamma)\frac{D_{Sb}}{D_s}\right). \tag{8}$$

Equation (6) indicates that D_{Sb}/D_s increases as the temperature T is lowered because the probability of the thermal release of electrons from the interface states to the conduction band is substantially decreased. Therefore, n is increased from 1.1 to 3.0 (see Fig. 3) as D_{Sb}/D_s is varied from 0.1 to 0.7 with a decrease in temperature. It is reasonable from Eq. (6) that D_{Sb}/D_s changes by such an amount as the temperature is lowered.

The electron population ratio D_{Sb}/D_s in the interface states was calculated as a function of current I from Eq. (7) using experimentally obtained n and γ. D_{Sb}/D_s monotonically increases with an increase in current similar to the cases of both amorphous and crystalline Si and can be interpreted by Eq. (6). However, in GaAs, the increase in D_{Sb}/D_s is more gradual and smaller than those in Si.

It is very interesting to investigate the behavior of the interface Fermi level E_{Fi} with the applied voltage because the interface Fermi level is considered to be strongly pinned at the metal Fermi level. In Fig. 4, the interface Fermi level $E_{Fi}-E_{Fm}$ relative to the metal Fermi level is calculated from Eq. (4) and plotted as a function of the applied voltage V for the nonoxidized Au-GaAs sample at room temperature. It can be seen that E_{Fi} increases from the metal Fermi level E_{Fm} by about 0.1 eV as the applied voltage is increased from 0.1 to 0.4 V.

On the other hand, the interface Fermi level $q\phi_B-E_{Fi}$ relative to the conduction band edge at the interface is calculated using Eq. (5) and shown as a function of the applied voltage V in Fig. 5 for the same sample. In this case, the change of Schottky barrier height $\Delta\phi_B$ and therefore the conduction band bending is taken into consider-

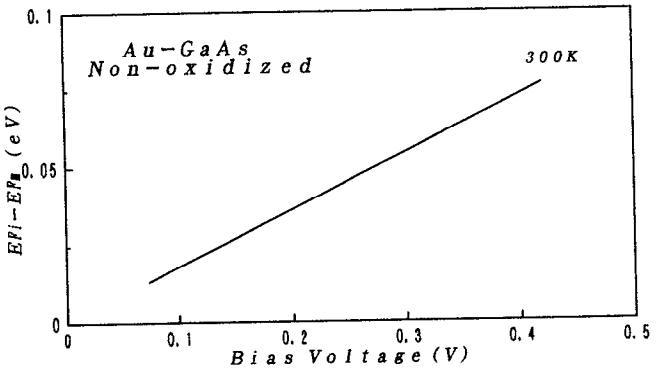

FIG. 4. The interface Fermi level $E_{Fi}-E_{Fm}$ relative to the metal Fermi level E_{Fm} vs the applied voltage V. $E_{Fi}-E_{Fm}$ increases by about 0.1 eV as the applied voltage is increased from about 0.1 to 0.4 V.

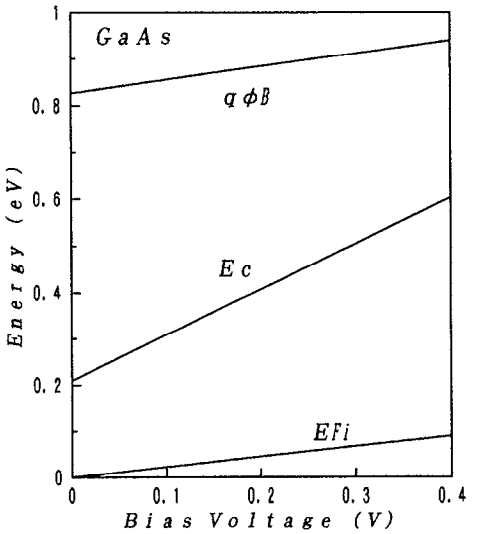

FIG. 6. Variations of the interface Fermi level E_{Fi}, the conduction band minimum E_c in bulk semiconductor, and the top of Schottky barrier $q\phi_B$, i.e., the conduction band minimum at the interface with the applied voltage. The metal Fermi energy is taken to be a zero of energy. $q\phi_B$ and E_{Fi} increase nearly the same order of magnitude with increasing applied voltage so that the interface Fermi level hardly approaches the conduction band edge at the interface. This seems to represent the Fermi level pinning effect.

ation as was indicated in Sec. III. In this figure, the interface Fermi level only approaches the conduction band edge by less than 0.01 eV as the applied voltage is increased from 0.1 to 0.4 V. From these, it is clearly demonstrated that while E_{Fi} moves relative to the metal Fermi level E_{Fm} with applied voltage, it hardly moves relative to the conduction band edge at the interface. This is due to the decreasing conduction band bending in the upward direction with increasing applied voltage and $\Delta\phi_B$. In Fig. 6, the changes of the Schottky barrier height energy $q\phi_B$, the conduction band edge E_c in the bulk semiconductor, and the interface Fermi level E_{Fi} with the applied voltage are schematically shown, where the metal Fermi energy is taken as a zero of energy. The increase of $q\phi_B$ is nearly the same order of magnitude as that in E_{Fi}, and E_{Fi} hardly moves relative to the conduction band edge at the interface. This is considered to be the first direct observation of the Fermi level pinning behavior under applied voltage.

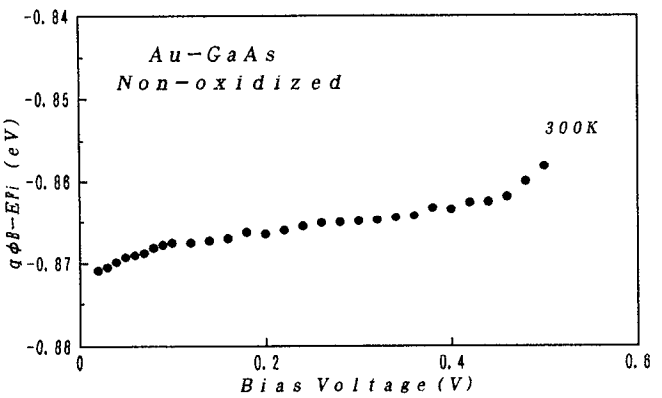

FIG. 5. The interface Fermi level $q\phi_B-E_{Fi}$ relative to the conduction band minimum at the interface vs the applied voltage V. $q\phi_B-E_{Fi}$ only increases by less than 0.01 eV as the applied voltage is increased from 0.1 to 0.4 V.

2. Oxidized samples

In both chemical and thermal oxide samples, the ideality factor n shows a considerable variation with the change in the applied voltage. The electron population ratio D_{Sb}/D_s in the interface states is calculated and plotted as a function of the current I in the same way as the case of nonoxidized samples. An example is shown in Fig. 7 for the chemical oxide Au-GaAs tunnel MIS diode sample for various temperatures between 100 and 400 K. In this figure, D_{Sb}/D_s shows an anomalous behavior. It first increases with an increase in current I and then decreases with further increase in I after passing a maximum at a certain value of I. In the highest current range observed, D_{Sb}/D_s again increases with an increase in I. This behavior was not observed in either amorphous or single crystalline Si nor in most of the nonoxidized GaAs samples.

This anomalous behavior of D_{Sb}/D_s can be explained when it is assumed that the interface state density D_s begins to decrease at an energy of about 0.05 eV above the metal Fermi level E_{Fm} where D_{Sb}/D_s shows the maximum. Here, 0.05 eV was roughly estimated from Fig. 7 and the I-V characteristics for the same sample as a difference between voltages corresponding to A and B points in Fig. 7. This is because the value of D_s in Eqs. (2), (3), and (5) is that between the metal Fermi level E_{Fm} at zero bias and $q\phi_0$ (see Fig. 8). On the other hand, D_{Sb} is the density of the interface states which are actually occupied by electrons between E_{Fi} and E_{Fm}. Therefore, if the interface state density D_s decreases at this energy as is shown in Fig. 8 and the communication probabilities remain the same, D_{Sb}/D_s should be decreased. The fact that D_s decreases at this energy shows a presence of a density peak in the interface

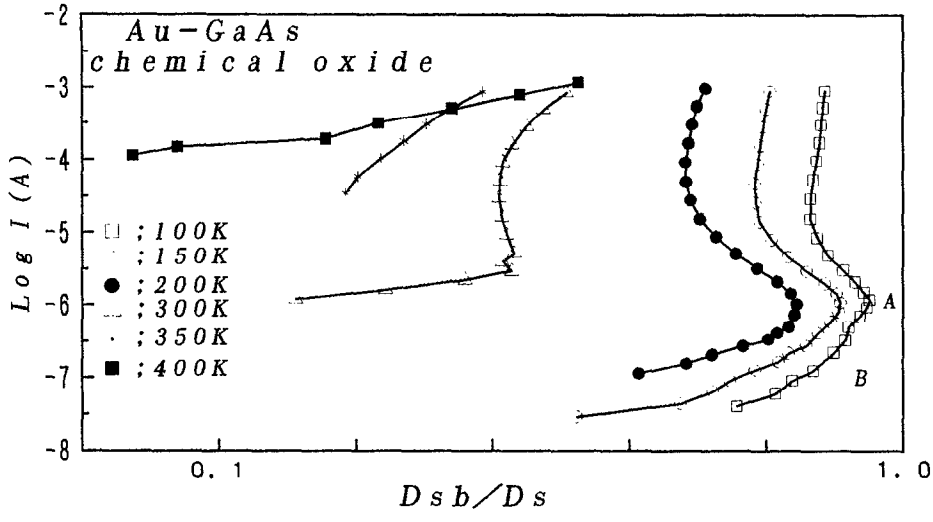

FIG. 7. The electron population ratio D_{Sb}/D_s of the interface states plotted as a function of log I under the forward bias for the chemically oxidized Ni-GaAs tunnel MIS diode sample at various temperatures between 100 and 400 K.

state distribution as is exhibited in Fig. 8. The Schottky barrier height $q\phi_B^0$ at zero bias is always 0.8~0.9 eV. The neutral level ϕ_0 of the interface states is about 0.5 eV from the valence band maximum. Then the interface state distribution has a peak at 0.8–0.9 eV from the conduction band edge. This model of the interface state distribution is consistent with the well-known defect model (DIGS) proposed by Spicer *et al.*[14]

V. SUMMARY AND CONCLUSIONS

I-V characteristics of metal-GaAs Schottky barrier diodes were measured at various temperatures between 100 and 400 K. In some samples, very thin oxides were intentionally grown on GaAs substrates using various oxidation techniques (tunnel MIS diodes). Both chemical and thermal oxidations were utilized to grow thin oxide films. The observed results were analyzed based on a recently proposed interfacial layer model for Schottky barriers. Values of γ deduced from the relation between the Schottky barrier height and the metal work function were very small compared to unity, indicating the Fermi level pinning at or near the neutral level ϕ_0 of the interface states. ϕ_0 and the interface state density D_s were approximately derived to be 0.5 eV from the valence band top and $(6\pm4)\times10^{13}$ $eV^{-1}\,cm^{-2}$, respectively.

The ideality factor n obtained from the forward *I-V* characteristics typically increased with decreases in temperature. This temperature dependence of n could be qualitatively explained in the present model.

In nonoxidized samples, it was clearly demonstrated that the interfacial Fermi level moved to some extent relative to the metal Fermi level with the applied voltage, while it hardly moved relative to the conduction band edge at the interface. This is due to the decreasing upward conduction band bending with increasing applied voltage. Thus this observation seems to represent the Fermi level pinning effect. This is considered to be the first direct observation of the Fermi level pinning behavior under applied voltage.

In oxidized samples, the electron population ratio D_{Sb}/D_s showed anomalous behaviors as a function of the forward current I. This could be explained by assuming that a density peak in the interface state distribution is about 0.8–0.9 eV from the conduction band bottom. This is consistent with the defect-induced gap states (DIGS) model proposed by Spicer *et al.*[14]

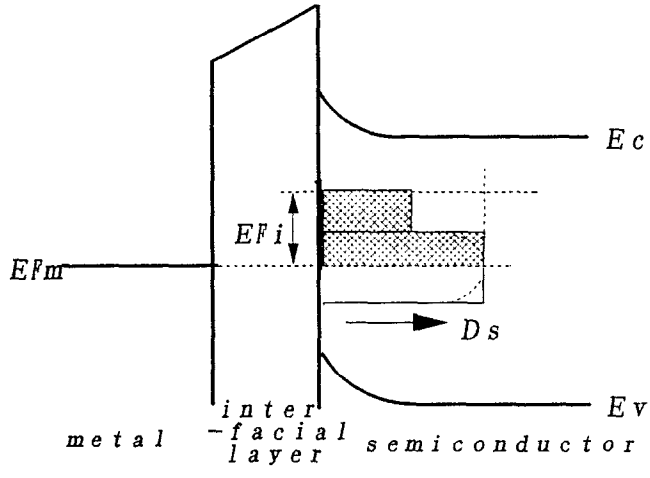

FIG. 8. The possible energy distribution of the interface states near the metal Fermi level E_{Fm}. The interface state density D_s decreases at a slightly higher energy position than the metal Fermi level E_{Fm} Electron population in the interface states due to applied voltage is shown by shaded area.

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