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FORMATION OF NiSi AND CURRENT TRANSPORT ACROSS THE NiSi–Si INTERFACE

J. M. ANDREWS
Bell Laboratories, Allentown, Pennsylvania 18103, U.S.A.

and

F. B. KOCH
Bell Laboratories, Murray Hill, New Jersey 07974, U.S.A.

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Abstract—The metallic compound NiSi has been produced by solid–solid metallurgical reaction in both *n*- and *p*-type silicon by sputtering Ni onto freshly back-sputtered silicon wafers and sintering for 5 min at 550°C. Identification of the orthorhombic (B31) monosilicide phase was made by X-ray diffraction, utilizing a glancing-angle Debye–Scherrer photograph of the 1300 Å thin-film phase on the silicon substrate.

NiSi Schottky barrier diodes, formed by this technique through holes in a silica mask and containing diffused guard rings around the periphery of the metallization, yield nearly ideal reverse I–V characteristics. The data have been fitted to a thermionic emission model for current transport, with barrier heights of 0.66 and 0.45 (eV) to *n*- and *p*-type silicon, respectively. The nature of the current transport characteristics strongly indicates the presence of a dipolar charge layer at the metal-semiconductor interface caused by quantum mechanical penetration of metallic electrons into the forbidden gap of the semiconductor.

Résumé—Le compound métallique NiSi a été produit par réaction métallurgique solide—solide dans du silicium de type *n* et aussi de type *p* en projetant du Ni sur des tranches de silicium contre-projetées et en frittant pendant 5 min à 550°C. L'identification de la phase orthorhombique (B31) du monosilicure a été faite par diffraction de rayons-X en utilisant une photographie Debye–Scherrer de l'angle critique de la phase de pellicule mince de 1300 Å sur la base en silicium.

Les diodes de barrière Schottky NiSi formées par cette technique par des trous dans un masque de silice et contenant des anneaux de protection diffusés autour de la périphérie de la métallisation, fournissent des caractéristiques inversées I–V presque idéales. Les données ont été adaptées à un modèle d'émission thermoionique pour transport de courant, avec des hauteurs de barrière de 0,66 et 0,45 (eV) au silicium du type *n* et du type *p* respectivement. La nature des caractéristiques du transport de courant indiquent fortement la présence d'une couche de charge dipolaire à l'interface métal-semi-conducteur causée par une pénétration mécanique quantique des électrons métalliques dans l'espace interdit du semi-conducteur.

Zusammenfassung—Die metallische Verbindung NiSi wurde durch eine metallurgische Festkörperreaktion in *n*- und *p*-leitendem Silizium hergestellt. Hierzu wurde Ni auf frisch durch Oberflächensputtern vorbehandelte Siliziumscheiben aufgesputtert und anschließend bei 550°C für 5 min zusammengesintert. Durch Röntgenbeugung wurde eine orthorombische Monosilizidphase (B31) identifiziert. Hierzu wurde von der 1300 Å dicken Dünnfilmphase auf dem Siliziumsubstrat ein Glanzwinkelphoto nach Debye–Scherrer aufgenommen.

Ni–Si-Schottky-Dioden, die nach der beschriebenen Technik durch Löcher in einer Quarzmaske mit diffundiertem Schutzring hergestellt waren, wiesen nahezu ideale Sperrcharakteristiken auf. Die Ergebnisse wurden mit einem Modell in Übereinstimmung gebracht, das für den Stromtransport die thermische Emission ansetzt mit einer Barriere von 0,66 und 0,45 eV für *n*-bzw. *p*-leitendes Silizium. Die Art der Stromcharakteristik deutet auf eine Dipolschicht an der Grenzfläche zwischen Metall und Halbleiter hin, die sich durch das quantenmechanische Eindringen der Metallelektronen in das verbotene Band des Halbleiters aufbaut.

NOTATION

A^{**} effective Richardson constant for metal-semiconductor interface (A cm^{-2} $°K^{-2}$)
$\mathscr{E}_m$ maximum electrostatic field at metal-semiconductor interface (V cm^{-1})
J_R reverse current density (A cm^{-2})
J_S' quasi-saturation current density (A cm^{-2}) (practical case, with barrier lowering)
k Boltzmann's constant (J $°K^{-1}$)
N_A acceptor density in silicon (cm^{-3})
N_D donor density in silicon (cm^{-3})
q electronic charge (coul)
R_C specific contact resistance for Schottky barrier at low reverse bias ($V_R < kT/q$) (Ω cm^2)
T absolute temperature (°K)
V_R reverse bias (V)
α rate of change of electrostatic barrier height with respect to electric field (cm)
ϵ_S electrical permittivity of silicon (F cm^{-1})
φ_B effective potential barrier at metal-semiconductor interface (eV)
φ_{B0} effective potential barrier at metal-semiconductor interface for vanishing electric field, or flat-band case (eV)

1. INTRODUCTION

THE FORMATION of metallic silicides by solid–solid metallurgical reaction between certain transition metals and silicon has resulted in a viable technology that is applicable to silicon integrated circuit manufacture[1]. Control of metallization material and substrate doping yields devices with electrical characteristics that span the entire range from ohmic behavior to strongly rectifying contacts, electrically similar to p–n junctions. Continuing research into the formation of metallic silicides will provide a variety of metallizations with different metal–semiconductor barrier heights from which a circuit designer can select the one best suited for his particular application.

The compound NiSi has been formed by thermal solid-state reaction between the elemental constituents at temperatures below the lowest nickel–silicon eutectic, occurring at 964°C. The barrier heights to n- (0.66 eV) and p-type silicon (0.45 eV) are close enough in magnitude so that unequal reverse leakage current densities can be compensated by a 25-fold ratio in contact diameter. This factor could be useful in complementary circuit applications where reverse diode leakage currents need to be approximately matched.

The following two sections describe the method of sample preparation and the identification of the NiSi phase by X-ray diffraction. Some effort has been spent to determine whether NiSi in contact with silicon is stable or is subject to transformation into $NiSi_2$. Annealing at 650°C for 28 hr in vacuum yields no evidence of a phase transformation, and it is therefore concluded that this metal–semiconductor system is quite stable. The fourth section presents preliminary results of experimental measurements of the room temperature reverse I–V characteristics of Schottky diodes consisting of NiSi formed in both n- and p-type silicon.

2. SAMPLE PREPARATION

Before deposition of the nickel, the silicon substrate wafer was subjected to a standard chemical cleaning procedure. This consisted of the seven following steps: (1) 5 min in boiling trichloroethylene; (2) Rinse in acetone and methanol; (3) 5 min in boiling Superoxol; (4) Rinse in deionized water; (5) Soak 5 min in 100:1 HF; (6) Rinse in methanol; (7) 2 min in boiling methanol.

The next step is a critical one in the formation of a metallic silicide, because, even after the most sophisticated chemical cleaning, traces of chemical contamination, such as photoresist, and a layer of nascent SiO_2 remain in the contact windows. These were removed by back-sputtering in an argon plasma at a pressure of 20 μ. Furthermore it is likely that the residual damage layer on the silicon surface, caused by exposure to the high energy argon ions, facilitated the initiation of the solid-solid metallurgical reaction required in the formation of NiSi. The back-sputtering step was carried out in the vacuum chamber illustrated in Fig. 1. The silicon wafers were placed on the graphite electrode and exposed to 1 min of r.f. back-sputtering with 4,000 V (peak-to-peak at 800 KHz). A nickel film was then deposited with a diode sputtering process (5,000 V at 15 mA applied to the Ni cathode shown in Fig. 1) at a deposition rate of 65 Å/min.

The NiSi contacts on silicon substrates were then formed by sintering the Ni metal film in a vacuum so that a thin film of NiSi was formed by solid-state metallurgical reaction. The nickel deposition and sintering processes were all carried out in the sputtering chamber during a single vacuum pumpdown. The sputtering deposition was done in an atmosphere of high-purity argon at a pressure of 25 μ. The subsequent sintering operation was completed at a pressure of less than 5×10^{-6} Torr.

NiSi Schottky barrier diodes with diameters of 1,

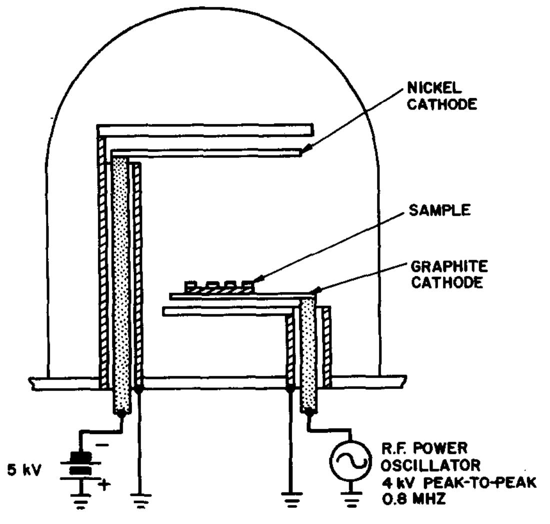

Fig. 1. Nickel sputtering system.

3, 8 and 20 mils were formed in this way in wafers of n- and p-type silicon through holes in a SiO_2 mask, 6000 Å thick. The edges of the diodes were protected by diffused guard rings extending to a depth of 2 μ into the silicon substrate and formed by a diffusion drive-in at 1130°C for 1 hr. The NiSi was formed on the two sample slices in the sputtering station together with a monitor slice used both for measuring the NiSi thickness and determining the metallurgical phase. Deposition for 10 min produced a film of nickel 600 Å thick which was then sintered at 550°C for 5 min to form the compound NiSi. The thickness of the NiSi film was calculated to be 1330 Å from the ratio of molar volumes of Ni and NiSi. The unreacted residual nickel on the oxide was subsequently removed by etching in a solution of 40 per cent (w/v) ferric chloride. The device slices were then given the usual Ti–Pt–Au overlays[1], the gold back contact, and an overnight bakeout at 300°C.

3. X-RAY ANALYSIS

The phase diagram of the nickel-silicon system is shown in Fig. 2. This diagram is reproduced from the work of Hansen[2], but it also shows the temperature values where the nickel–silicon

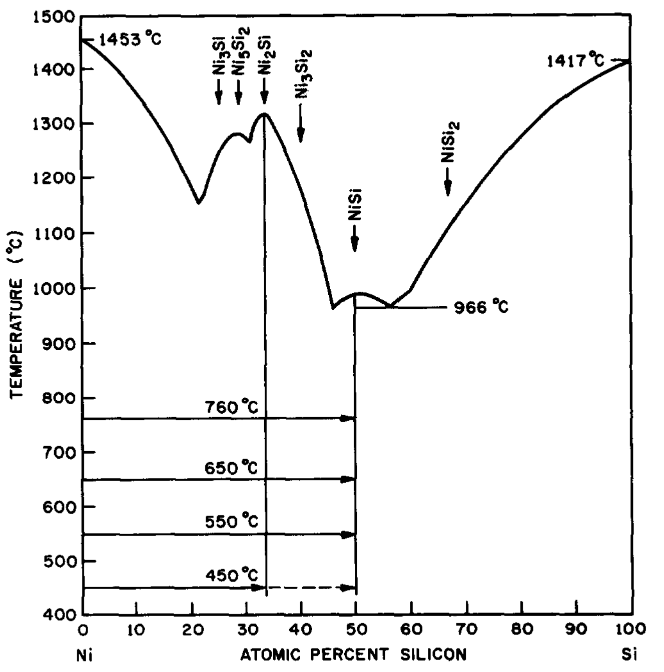

Fig. 2. Phase diagram of the nickel–silicon system.

compounds reported here have been produced by solid-solid metallurgical reaction.

A single-phase, thin film of NiSi was formed by vacuum sintering for 5 min at 550°C. This is indicated by the horizontal line in Fig. 2 drawn at the appropriate ordinate intercept. Figure 3 shows an X-ray diffraction photograph obtained from a NiSi film on a control slice. A similar control slice of bare (111) silicon was used to check the phase of the NiSi films formed in the contact windows of the device slices used for the electrical measurements reported in Section 4. The diffraction lines from the nickel silicide are superimposed upon a pattern of Laue spots from the (111) silicon substrate. All observed lines were found to correspond to the orthorhombic (B31) crystal structure of NiSi; the Miller indices are shown in Fig. 3 for $d > 1$ Å. Identification of the lines for which $d < 1$ Å is uncertain because of the large number of allowed reflections. The sample was oriented at a grazing angle of 16° with respect to the beam, and the shadow of the sample gives rise to the dark portion on the bottom of the photograph.

Table 1 lists the observed diffraction lines together with the d-spacings calculated for the B31 structure with $a_0 = 5.657$, $b_0 = 5.238$, $c_0 = 3.240$. Good agreement is obtained with the peak positions measured by a diffractometer, whereas there were small but significant discrepancies when the d-spacings were calculated using Toman's previously published lattice parameters: $a_0 = 5.62$ Å, $b_0 = 5.18$ Å, $c_0 = 3.34$ Å [3]. The discrepancy may be due to the formation of NiSi at relatively low temperatures (650–750°C), whereas in Toman's work the samples were prepared by cooling from the melt above 992°C. There is strong preferential orientation evident in some of the NiSi patterns studied in which the (020) plane of the NiSi film is parallel to the silicon (111) substrate plane, as evidenced by the arcing of some of the diffraction rings.

For sintering temperatures at 450°C or below, additional diffraction lines were observed which could be indexed as orthorhombic Ni_2Si [2]. The

Table 1. Diffraction lines from NiSi

Approx. d-Spacing (photos)	d-Spacing Diffractometer	Int. (Photo)	hkl	Nom. B31 (Calc.)	Refined B31 (Calc.)
3.82	N.D.	W	110	3.808	3.843
2.82	N.D.	W	200	2.810	2.828
2.62	2.619	S	020	2.590	2.619
2.48	2.482	M	210	2.470	2.489
2.04	2.033	W	021	2.046	2.037
1.98	1.973	W	211	1.986	1.973
1.92	1.916	S	121	1.923	1.916
1.92	N.D.	S	220	1.904	1.921
1.77	N.D.	W	310	1.762	1.774
1.63	N.D.	W	002	1.670	1.620
1.68	N.D.	M	130	1.650	1.688
1.63	1.630	W	301	1.633	1.629
N.D.		–	112	1.529	1.493
N.D.		–	202	1.436	1.405
N.D.		–	022	1.403	1.378
N.D.		–	321	1.381	1.384
N.D.		–	231	1.346	1.350
N.D.		–	040	1.295	1.309
1.28		W	330	1.269	1.281
N.D.		–	140	1.261	1.276
N.D.		–	411	1.256	1.258
N.D.		–	222	1.255	1.239
1.185	1.195	M	312	1.211	1.196
			141	1.180	1.187
			240	1.176	1.188
1.16			132	1.174	1.162

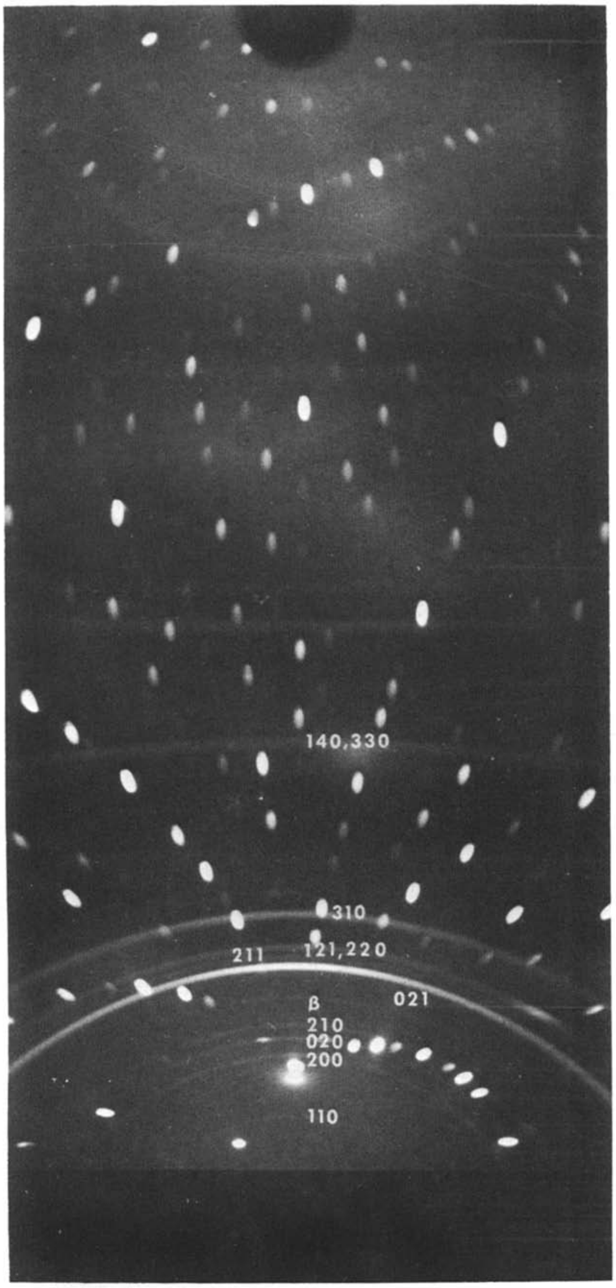

Fig. 3. X-ray diffraction photograph of the B31 structure of NiSi, shown by arcs. The spots are due to the Laue pattern from the (111) silicon substrate.

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nickel–silicon system is thus similar to the platinum–silicon system[4] in the sense that the phase that is normally formed at temperatures high enough to avoid a kinetic limitation on the film growth is a monosilicide with an orthorhombic (B31) crystal structure. In both systems a nonequilibrium $(Metal)_2Si$ phase is always formed when the reaction temperature is too low. In the case of platinum, Pt_2Si results for sintering temperatures up to about 300°C, whereas Ni_2Si is evident in films sintered at temperatures up to 450°C.

Also indicated in Fig. 2 is the phase $NiSi_2$, which would be in equilibrium with excess silicon[2]. To test the possibility that the compound NiSi is unstable and might transform into $NiSi_2$, a series of samples were formed both at higher temperatures and with longer sintering times. Samples sintered for 5 min at 650°C and 760°C showed no diffraction lines other than those expected from the B31 structure of NiSi. Further sintering at 650°C for 1 hr and for 28 hr produced some change in the amount of preferential orientation, but no evidence of any new phase was observed. It is therefore concluded that the NiSi phase is either in true equilibrium with silicon at these temperatures or transforms with extreme difficulty into $NiSi_2$. Preparation at 550–760°C is thus expected to yield pure NiSi, and this is the phase observed by X-ray diffraction.

4. REVERSE *I-V* CHARACTERISTICS

Schottky barrier diodes have been fabricated with NiSi contacts formed by solid–solid chemical reaction in both *n*- and *p*-type silicon. The reverse current–voltage characteristics of these devices have been measured at room temperature and compared with a theoretical model based upon thermionic emission of carriers over the potential barrier existing at the NiSi–Si interface. According to this model, the reverse current density is given by

$$J_R = A^{**}T^2 \exp(-q\varphi_B/kT)[1-\exp(-qV_R/kT)] \quad (\mathrm{A\,cm^{-2}}) \qquad (1)$$

Appropriate values for the effective Richardson constant A^{**} have been discussed by Andrews and Lepselter[5]. These values are slightly field-dependent, but, in silicon, can be taken to be nearly constant over a wide range of reverse bias.

$$A^{**} \simeq 112\,(\mathrm{A\,cm^{-2}\,°K^{-2}})\ \text{electrons} \qquad (2)$$

$$A^{**} \simeq 32\,(\mathrm{A\,cm^{-2}\,°K^{-2}})\ \text{holes} \qquad (3)$$

The value of the effective barrier height φ_B is also dependent upon the maximum value of the electric field $\mathscr{E}_m$ in the depletion region of the silicon at the NiSi–Si interface.

$$\varphi_B(\mathscr{E}_m) = \varphi_{B0} - (q\mathscr{E}_m/4\pi\epsilon_s)^{1/2} - \alpha\mathscr{E}_m\ (\mathrm{eV}) \qquad (4)$$

The quantity φ_{B0} is an empirical value for the barrier height in the limit of vanishing electrical field at the interface (flatband), a situation that cannot be fully realized physically. The empirical parameter α represents approximately the barrier-lowering associated with an electric dipole layer, postulated on the basis of the quantum mechanical penetration of free electronic charge from the metal into the forbidden gap of the semiconductor [6]. In the experiments reported here the values of φ_{B0} and α are treated as adjustable parameters that are varied to minimize the RMS deviation between the experimental data and the theory.

The diodes were fabricated with diffused guard rings surrounding the edge of the NiSi metallization to prevent the high electric field, associated with the discontinuation of the metal, from causing premature breakdown and general softening of the reverse characteristics. A cross-sectional view of the diode structure is shown in Fig. 4 for one of the diodes formed in *n*-type silicon. Data on the reverse characteristics of a NiSi Schottky diode formed in *n*-type silicon are shown in Fig. 5 for two diode diameters. The effective diode diameter is controlled by the inside diameter of the guard ring structure. Allowing for lateral diffusion under the oxide during drive-in, the effective diode diameters are 2.7 mils (6.8×10^{-3} cm) and 7.7 mils (1.96×10^{-2} cm). The substrate material is 1 Ωcm with $N_D = 6 \times 10^{15}$ cm^{-3}. Measurements, made at room temperature (~297°K), are shown by the open circles; the theoretical predictions of equations

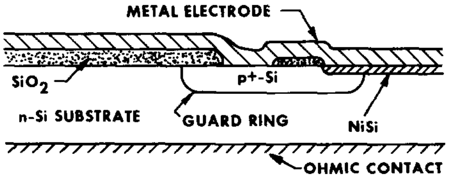

Fig. 4. Guard-ring structure of a NiSi Schottky diode formed in *n*-type silicon.

(1)–(4) are shown by the solid lines with $q\varphi_{B0} = 0.656, 0.657$ (eV); $\alpha = 11.0, 9.0$ Å; RMS deviation between theory and experiment is 2.9, 3.6 per cent for the 2.7 mil and the 7.7 mil diodes, respectively. The relatively low values of the barrier lowering parameter α are consistent with theoretical expectation for metal-semiconductor systems with the Fermi level close to the center of the forbidden gap[6].

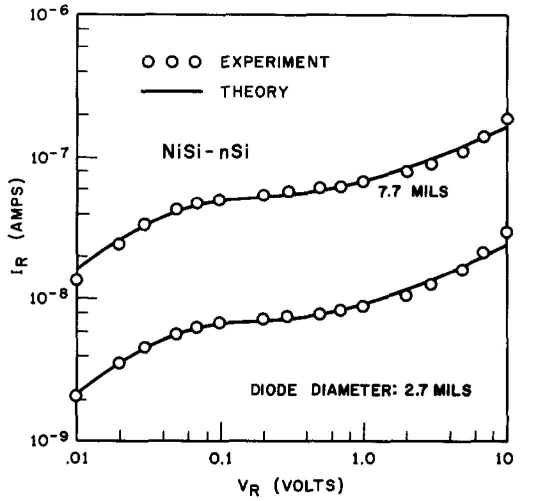

Fig. 5. Reverse current–voltage characteristics of NiSi Schottky diodes formed in n-type silicon. $N_D = 6 \times 10^{15}$ cm^{-3}, $\phi_{B0} = 0.66$ eV.

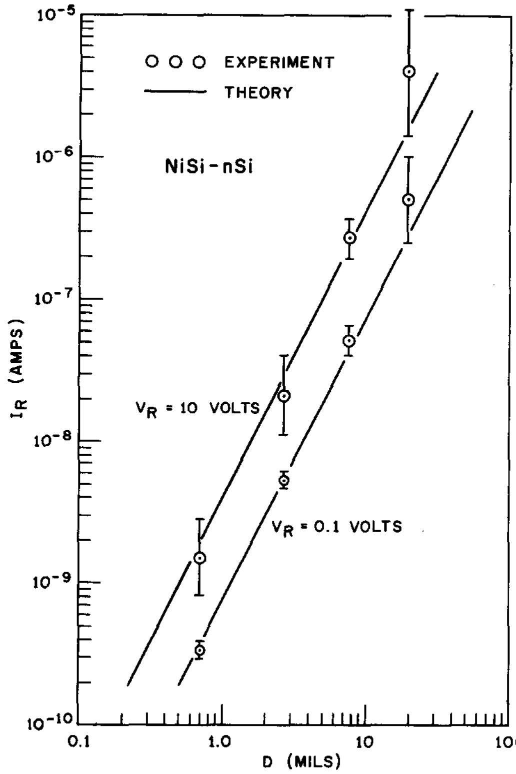

Fig. 6. Summary of reverse leakage current data, shown as a function of diode diameter. Measurements were made on 40 NiSi devices, formed in n-type silicon with $N_D = 6 \times 10^{15}$ cm^{-3}.

The efficacy of the guard ring structures in preventing premature breakdown and surface leakage can be ascertained by studying reverse leakage current as a function of diode diameter at constant reverse bias. For this purpose, arrays of Schottky diodes with diameters equal to 0.7, 2.7, 7.7 and 19.7 mils were formed in n-type silicon. Reverse leakage currents were measured for 10 devices of each diameter at reverse biases equal to 0.1 and 10 V. The resulting measurements were plotted on log-normal probability paper in order to select the data points that fall close to a normal distribution probability curve. From these plots the mean values and the standard deviation of the data population were determined. The results are summarized in Fig. 6, in which a circle designates each median value, and the length of each bar shows twice the standard deviation of the corresponding data. The solid lines drawn through the experimental data have slopes equal to 2, showing that the leakage currents are proportional to the squares of the diameters of the diodes. If, on the other hand, the leakage currents were dominated by edge effects, the data would be expected to lie along straight lines with slopes equal to unity. The large area diodes show some tendency toward excess leakage with sharply increasing standard deviation in the measured data. These characteristics are attributed to leakage associated with defect centers at the silicon–silicide interface. The probability of the occurrence of such defects increases 800 times over the range of diode diameters investigated.

Data on the reverse characteristics of a NiSi Schottky diode formed in p-type silicon are shown in Fig. 7 for a diode with an effective diameter of 0.7 mils (1.78×10^{-3} cm). The substrate material is 1 Ωcm with $N_A = 1.7 \times 10^{16}$ cm^{-3}. Measurements

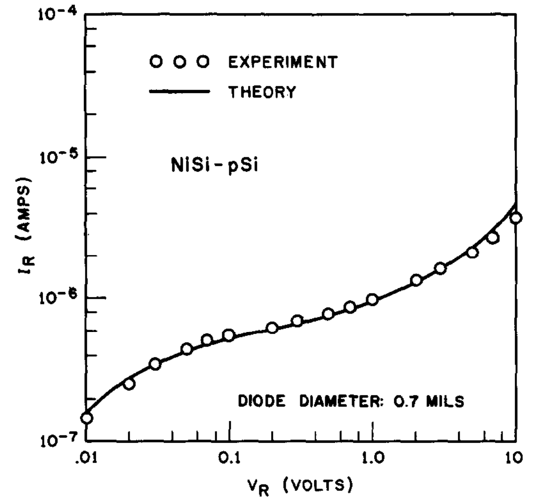

Fig. 7. Reverse current-voltage characteristics of a NiSi Schottky diode formed in p-type silicon. $N_A = 1.7\times 10^{16}$ cm^{-3}, $\phi_{B0} = 0.45$ eV.

made at room temperature (~ 297°K) are shown by the open circles; the theoretical prediction of equations (1)–(4) is shown by the solid line with $q\varphi_{B0} = 0.448$ eV, $\alpha = 14$ Å. RMS deviation between theory and experiment is 5.2 per cent.

Although the concept of saturation current density does not precisely characterize a device exhibiting soft or non-saturating behavior, it nevertheless provides the designer with a useful quantitative parameter. We therefore define a quasi-saturation current density J_S' in the usual manner.

$$J_S' = \frac{kT}{q}\left.\frac{\mathrm{d}J_R}{\mathrm{d}V_R}\right|_{V_R\to 0} = A^{**}T^2 \exp(-q\varphi_B/kT) \quad (\mathrm{A\ cm^{-2}}) \qquad (5)$$

Equation (5) can also be expressed in terms of a specific contact resistance.

$$R_C \equiv \left.\frac{\mathrm{d}V_R}{\mathrm{d}J_R}\right|_{V_R\to 0} = (k/qA^{**}T)\exp(q\varphi_B/kT) \quad (\Omega\ \mathrm{cm^2}) \qquad (6)$$

A summary of the measured electrical data for the NiSi Schottky diodes reported here is contained in Table 2.

5. CONCLUSIONS

Films of nickel, sputtered onto freshly back-sputtered wafers of silicon, produce metallic compounds by solid-state metallurgical reaction when sintered in vacuum at elevated temperatures below the melting point of the NiSi–Si eutectic. The reaction products have been identified by X-ray diffraction, utilizing glancing-angle Debye–Scherrer photography. At sintering temperatures below 450°C, a non-equilibrium mixture of the compounds Ni_2Si and NiSi was observed. At sintering temperatures above 550°C, a single-phase thin film of orthorhombic (B31) NiSi was formed. Subsequent annealing at temperatures up to 760°C did not reveal any tendency for the system to progress toward a more silicon-rich phase, such as $NiSi_2$. Evidently NiSi is either in true equilibrium with silicon throughout the temperature range covered in this investigation (450–760°C) or kinetic limitations prevent the reaction from proceeding toward the more silicon-rich phase, $NiSi_2$.

The reverse I–V characteristics of Schottky barrier diodes, produced by forming NiSi in both n- and p-type silicon, have been measured at room temperature. Reverse current transport has been successfully fitted to a thermionic emission model with barrier heights 0.66 eV and 0.45 eV to n- and p-type silicon, respectively. These experimental devices contained diffused guard rings around the periphery of the metallization to suppress excess reverse leakage current due to electric field en-

Table 2. Summary of data on nickel silicide Schottky barrier diodes

						Room temperature	
Silicon type	Device diameter D (cm)	Barrier height φ_{B0}(eV)	Barrier lowering parameter α (Å)	RMS deviation S(%)	Doping density $N_{D,A}$(cm^{-3})	Quasi-saturation current density J_s' (A cm^{-2})	Specific contact resistance R_c (Ω cm^2)
n	6.8×10^{-3}	0.656	11	2.9	6.0×10^{15}	1.9×10^{-4}	136.000
n	19.6×10^{-3}	0.657	9	3.6	6.0×10^{15}	1.8×10^{-4}	141.000
p	1.78×10^{-3}	0.448	14	5.2	1.7×10^{16}	0.21	0.123

hancement near the discontinuation of the contacts. The observed reverse currents scale correctly with the squares of the diameters of the active areas of the diodes, but the electric field dependence of the effective barrier height is slightly greater than that expected from the image-force mechanism alone. The additional barrier lowering indicates the presence of a dipolar charge layer at the metal–semiconductor interface, previously interpreted[6] in terms of quantum mechanical penetration of metallic electrons into the forbidden gap of the semiconductor. Empirical values of the dipolar barrier lowering parameter α, determined in this investigation by minimizing the RMS deviation between theory and experiment, have been found to range between 9 and 14 Å (Table 2). These values are the lowest that have been observed for metallic silicide Schottky diodes[1, 5], which is consistent with theoretical expectation[6] for metal-semiconductor (M–S) systems with the Fermi level occurring close to the center of the semiconductor energy gap at the M–S interface.

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