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Fast low bias pulsed DC transport measurements for the investigation of low temperature transport effects in semiconductor devices

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ABSTRACT

We present a setup for fast, low-bias (≤ 1 mV) DC transport measurements with μs time resolution for high ohmic resistance (≈ 20 kΩ) semiconducting samples. We discuss the circuitry and instrumentation for the measurement approach that can be applied to any kind of semiconductor device or (gated) two-dimensional material and demonstrate the main measurement artifacts in typical measurements by means of circuit simulation. Based on the latter, we present a simple two-step protocol for eliminating the measurement artifacts reliably. We demonstrate the technique by measuring the transitions between quantum Hall plateaus in the HgTe quantum wells and resolve plateaus as short-lived as 100 μs.

I. INTRODUCTION

Electronic transport measurements determine the electronic response of a device against externally controlled parameters like gate voltage, magnetic field, or temperature. Sensitive low-frequency lock-in techniques have been the essential core of electronic (quantum) transport research for decades. A good overview of the lock-in technique can be found in Ref. 1. While the technique has many advantages, all centered around the locked phase relation between bias and measured signal, the (long) integration time can be a limiting factor of this approach, when parameters change on time scales comparable to or shorter than the integration time. One prominent example are semiconductor transport experiments at low temperatures in pulsed magnetic fields. Pulsed magnetic fields can provide up to ~ 100 T (significantly larger than currently available with static magnetic fields), but typically only last for around 100 ms,[2] which is difficult to measure using lock-in amplifiers at low bias without using special circuit layouts and cryostat wiring.[3,4] Hence, DC measurement techniques are often employed in pulsed fields.[4,5] Other examples for transport measurements where parameters change on short time scales are, e.g., heat transport studies[6–8] or experiments interested in resolving the time evolution of charge transport inside a device.[9,10] Lastly, fast transport measurements can also be beneficial when one is interested in the transport response of a device across a wide range in parameter space. *Pulsing* the external parameter(s) while measuring the transport response can allow for significant time savings compared to the steady-state approach.[11]

Conducting fast transport experiments always requires a good understanding of the measurement setup. In cryostats with ordinary twisted-pair wiring, especially low-pass filtering and charging effects need to be taken into account when interpreting the results. In this work, we perform a careful circuit analysis of a typical measurement setup and derive methods to eliminate the spurious effects originating from the setup rather than the physical properties of the device under test when performing fast transport measurements. We employ pulsed DC measurements rather than high-frequency AC techniques in the pulsed measurement scheme

as the device along with the cryostat wiring inevitably forms a low-pass filter that limits the bandwidth to $\ll 1$ kHz (discussed later in this work), resulting in insufficient time resolution. The technique is primarily targeted at conducting transport experiments on semiconductor samples with resistances on the order of 10 Ω–100 kΩ at cryogenic temperatures. In order to ensure that the device stays within the linear transport regime and is not heated excessively, we impose a limit of 1 mV bias over the semiconductor sample. The whole measurement circuit is highly modular and fully located outside the cryostat at room temperature. A gate electrode (which allows varying the carrier density) is supported but not necessary for the measurement scheme.

We start with a discussion of the measurement circuitry as well as the required instruments in Sec. II A, followed by a detailed circuit analysis based on LTspice circuit simulations in Sec. II B. The real-world applicability of the fast technique is then demonstrated in Sec. II C by resolving quantum Hall plateaus that are only observed for around 100 μs while quickly ramping the gate voltage. Pulsing the gate voltage at constant magnetic fields mimics measurements in pulsed magnetic fields, which are the main motivation for our investigation. Even though the pulsed gate measurements were originally only conducted for development purposes, we show that they are also already useful in and of itself for recording two-dimensional conductance maps as a function of external parameters, as we demonstrate in our first application (Sec. III A). The second application are then measurements in pulsed magnetic fields that allow significantly extending the range of maximum magnetic field available, as compared to static magnetic fields (Sec. III B).

II. FAST PULSED DC TRANSPORT MEASUREMENTS

A. Circuit design and measurement instruments

The general circuit for a low voltage bias measurement is shown in Fig. 1. We consider a sample in a standard six-terminal Hall bar design with a top gate, which is grounded at the current drain. A small DC bias (on the order of 1 mV) is applied across the Hall bar and a serial reference resistor. The reference resistor is used for measuring the current flow into the Hall bar. The longitudinal and transverse voltages are first amplified by 60 dB differential voltage pre-amplifiers and then recorded by an analog-digital converter. For experiments at cryogenic temperatures, the sample is placed inside a cryostat and is typically wired with twisted pairs or cryogenic coaxial cables, which are then connected to the measurement devices at room temperature. A magnet is optionally fitted in the cryostat for conducting field-dependent studies. The presented sample also features a gate electrode for varying the carrier density.

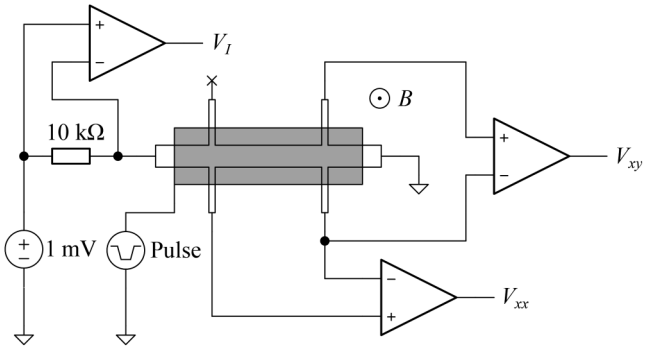

FIG. 1. Measurement setup for time resolved transport measurements in dependence of a fast swept (*pulsed*) gate voltage. The longitudinal (R_{xx}) and transverse (R_{xy}) resistance of the Hall bar device can be calculated from the corresponding voltages V. The voltages are measured using high-input-impedance differential voltage pre-amplifiers. A magnetic field B in out-of-plane direction is indicated. Further details are discussed in the main text.

In this work, we use *Femto* model *DLPVA-100-F-D* as differential voltage pre-amplifiers. They feature differential voltage inputs, a low-noise voltage amplification between 20 and 80 dB and a very large input impedance of 1 TΩ. They also include a selectable low-pass filter (1 or 100 kHz) at the output stage to suppress radio frequency noise. The main goal is to perform measurements on time scales below 1 ms, which requires a sufficiently fast voltage recorder (analog–digital converter), featuring at least 100 kS s^{-1} for sufficient time resolution. The voltage resolution of the converter ideally surpasses 12 bit to avoid digitization steps. The number of required input channels is obviously specified by the intended measurement. For the Hall bar device, four input channels are required to simultaneously record V_I, V_{xx}, V_{xy}, and the gate voltage V_G. Suitable devices include a digital storage oscilloscope, a computer measurement card, or a transient recorder. We employ all three device types for the presented demonstration measurements, according to their distinct advantages and disadvantages (discussed later). For the circuit tests shown in Sec. II, we use a *Rhode & Schwartz HMO3004* four-channel oscilloscope. For the applications shown in Secs. III A and III B, we use an *NI 6212* computer card and a *Yokogawa DS850E* transient recorder with *No. 701251* inserts, respectively. The analog-to-digital conversion rate of these devices (and comparable) can easily surpass the discussed necessary rate for measurements on the ms time scale, as sampling rates of GS s^{-1}are readily available. However, as will be shown in the following, the pulsing speed of the discussed technique is not limited by the conversion rate, but rather by circuit and device-based time-domain effects on the timescale of order 100 μs. Therefore, exceeding the recommended minimum of 100 kS s^{-1} might provide larger data sets with a higher resolution, but the time scale of a single parameter sweep cannot be reduced arbitrarily. To enable measurements on the ms time scale in the first place, the systematic errors and time-domain effects in the circuit need to be evaluated and eliminated, which is done in detail in the upcoming Sec. II B.

Before continuing with a detailed analysis of the time-domain response of the measurement circuit, a few practical remarks and best practices regarding the setup of the circuit should be noted. The high impedance of the sample (the impedance of a semiconductor device in a large magnetic field is of the order of tens of kΩ) and the low voltage bias results in small currents (on the order of 10 nA). The measurement is, therefore, prone to parasitic currents caused by ground loops. To avoid these, careful grounding in a star configuration to a single user-defined drain terminal is advisable. When possible, two separated mains-electricity circuits should be used, one for noisy equipment like pumps, magnet power

supply, and computers, and the other for measurement equipment like multimeters, lock-in amplifiers, and power supplies. Care must be taken to always keep the two different grounds galvanically isolated (or at least separated through a high-impedance path), as this is often a significant source of noise when done incorrectly. Furthermore, high-quality shielded cables (*Belden 9223 Low Noise Coax*), connectors (*Amphenol BNC Straight Crimp Plug RG-58*, *Amphenol UG-274/U BNC T-Shape Adapter*) and metal enclosures should be used for shielding the measurement circuit. Small signals should always run on inner conductors, i.e., a pair of BNC cables should be used for differential measurements instead of using the inner conductor plus the shield of a single one. The pair of BNC cables can be twisted (like a twisted pair) to further reduce the coupling loop area and to increase mechanical stability (against piezoelectrics). The wiring inside the cryostat should consist of twisted pairs or coaxial cables. Topics like noise pickup, coupling between wires, induced voltages in a magnetic field, and heat load should be considered.[1,12] Another useful reference for general techniques and best practices for performing low-level measurements is Ref. 13.

B. Circuit analysis

The interplay of resistance, capacitance, and inductance (*RCL* effects) induces systematic errors in the measurements upon changing from steady-state DC to pulsed operation. Like every other circuit, the circuit in Fig. 1 also includes (parasitic) capacities and inductances. Both are predominantly introduced by the wiring of the cryostat, as twisted pair wires (just like coaxial cables) have a significant inter-wire capacitance. Characterization measurements performed with an LCR-meter yield an effective capacitance of around 600 pF between a single wire and ground, as well as around 60 pF inter-wiring capacitance. These values coincide well with those established in a cryostat wired with twisted pairs.[14] Our analysis further reveals that inductive effects are negligible compared to the capacitances in the circuit at the target frequencies. We, therefore, neglect inductances for the remainder of the work. Finally, we have to take into account the well-defined low-pass output-filter characteristics of the pre-amplifiers.

In order to assess and correct the measurement artifacts introduced by the presence of the parasitic capacitances and low-pass filters, we devise a simple two-probe model of our measurement using LTspice. To accurately model the device response to a fast gate voltage sweep (which we term *gate-pulsing*), we input the steady-state two-probe response obtained from slow lock-in measurements into the simulation by fitting a sixth-order polynomial to the observed response [see Fig. 2(a)]. The test material system is a quantum well in a HgCdTe/HgTe/HgCdTe heterostructure with a type III inverted band structure, effectively resulting in a low electron density two-dimensional electron gas. The grounded carrier density is $1.5 \times 10^{11}\,\mathrm{cm}^{-2}$ and can be tuned between n and p-conducting state by a gate voltage of $\sim \pm 1$V. Further details on the material system and on the Hall bar device fabrication can be found in Refs. 15–19.

Figure 2(b) shows the LTspice model for a gate-pulsing measurement. It includes the previously discussed 600 pF wire-to-ground capacitance and the 60 pF wire-to-wire capacitance in the form of two capacitors. The gate voltage pulse is modeled by a trapeze-shaped signal applied directly to the gate electrode, as is later used during the experiments, in order to record the bidirectional response. The single pre-amplifier in the two-probe measurement is modeled as an ideal differential amplifier with a 1 kHz low-pass filter at its output. The LTspice simulation is a transient simulation over the time period of the gate voltage pulse. The result of the simulated 20-30-20 (numbers indicate the rise times and plateau time in ms) voltage pulse, along with a selection of even faster rise times, is shown in Fig. 2(c).

Inspecting the right panel, the pulsed gate measurements clearly show a systematic deviation from the steady-state signal by forming a hysteresis loop that encloses the steady-state response. With smaller rise times, a stronger hysteresis develops. The left panel shows the time transients, in which the influence of the capacitance in the circuit becomes clear (regions marked by boxes). In the left blow-up, an exponential decay toward the steady-state value is observed. Analyzing the time constant of the decay indicates a cutoff frequency of 1 kHz, clearly identifying the output low-pass filter of the pre-amplifier as the source of the discharging effect. The right blow-up reveals an undershoot compared to the steady-state value as soon as the gate voltage ramping starts. As this is a non-monotonic effect, it cannot be explained by a low-pass effect. Instead, this undershoot occurs due to the charging of the inter-wiring capacitance, C3. The required charge flows from the voltage source V2 through the reference resistor, which creates an additional voltage drop. This results in the observed undershoot in V_I.

With the available quantitative understanding of the model, we next perform a pulsed gate measurement on a real sample using the circuit described in Sec. II A. We use one of the analog outputs of the *NI 6212* computer card to generate the excitation pulses. A trigger signal is sent by the card to start the recording of data by the oscilloscope at the start of the gate voltage pulse. Figure 2(d) shows the measurement results. The agreement between the simulation and experimental results is very good. The simulation exhibits the observed (dis-)charging effects both qualitatively and quantitatively. This confirms that the discussed effects are indeed the dominant time-domain artifacts when the gate voltage is changed quickly. Because similar charging effects also occur when the gate voltage is fixed and the sample impedance is changed rapidly, for example, by applying a pulsed magnetic field, this circuit analysis forms the basis for all further analysis steps discussed in the following.

Based on the analysis of the circuit response above, we can correct for the (dis-)charging as well as the low-pass effect in the measured signal and reconstruct the steady-state response from the pulsed gate measurements. We follow the two-step recipe presented in Fig. 3. Step I is based on the observation that the charging effects are essentially independent of the applied voltage bias (due to the low-bias voltage compared to the gate voltage change). As shown in Fig. 3(a), even when zero bias is applied, a significant charging current is observed, as the combined gate- and wiring-capacitance is charged during the gate voltage sweep. We eliminate this charging effect by subtracting the zero-bias response from the measurement with 1 mV bias, which is shown in Fig. 3(b). The hysteresis is reduced significantly and particularly eliminates the large

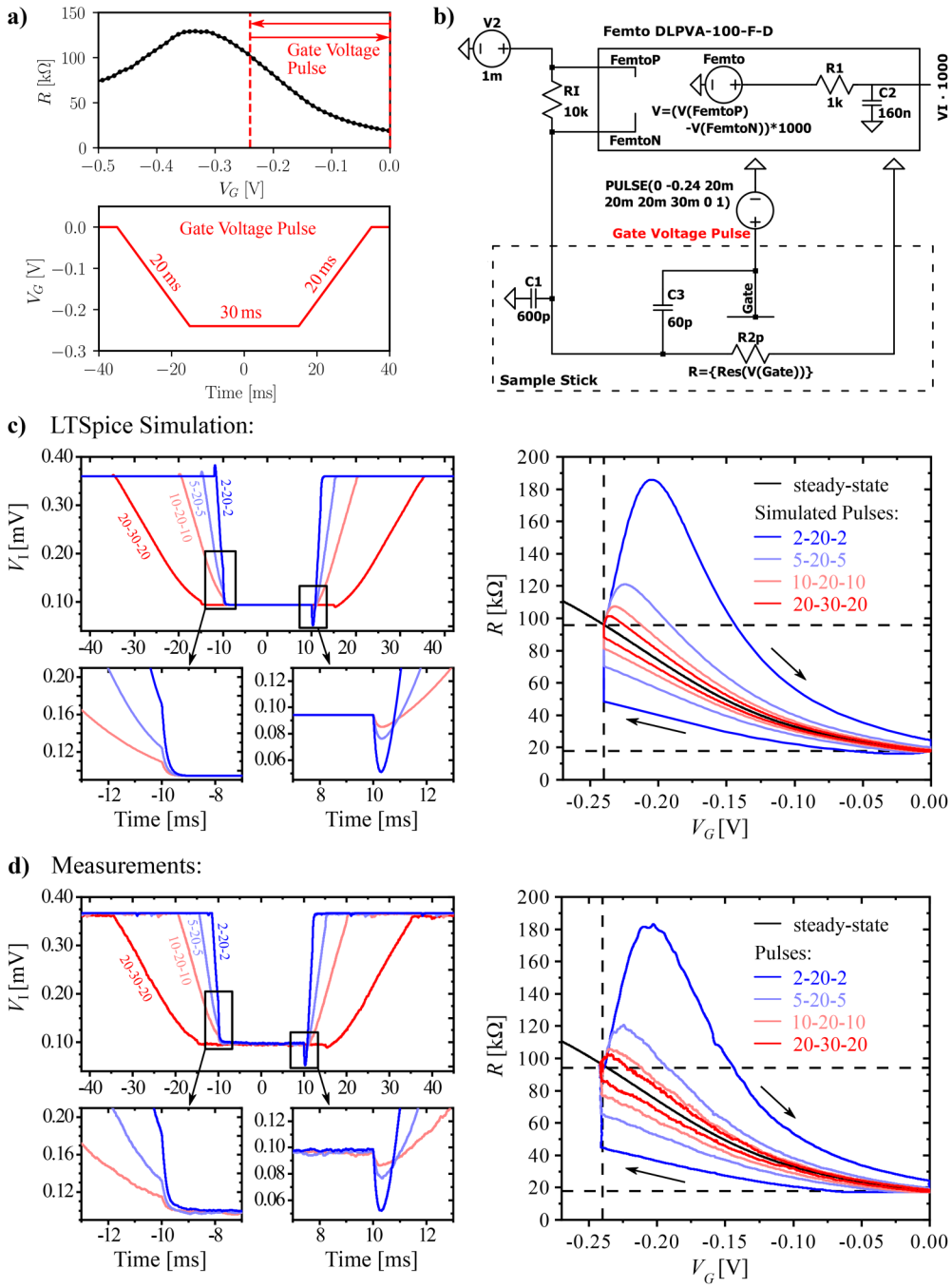

FIG. 2. Comparison of experimental pulsed gate two-probe resistance measurements with simulation results using a simple RC-model. (a) Steady-state two-probe resistance R of a test device as a function of applied gate-voltage V_G at 4.2 K. The red dashed line indicates the range of the gate pulses used in this figure. The lower plot shows an exemplary trapeze-like 20 ms-30 ms-20 ms (20-30-20) gate pulse. (b) LTspice circuit model of the experiment. The *Femto* DLPVA-100-F-D differential preamplifier is modeled as an ideal differential amplifier with a 1 kHz bandwidth first-order low-pass filter at its output. The wiring capacitance is modeled by a 600 pF capacitor, and the gate capacitance (including the wire that leads to the gate) by a 60 pF capacitor. (c) Left: LTspice simulation of the voltage V_I across the pre-resistor for gate pulses with different slew rates. The two plots at the bottom show the region around the pulse edges in more detail. Right: Apparent two-probe resistance R against gate voltage, the arrows indicate time. A strong hysteresis develops for smaller slew rates. (d) Same as in (c), but showing the gate-pulsing measurement of the test device at 4.2 K.

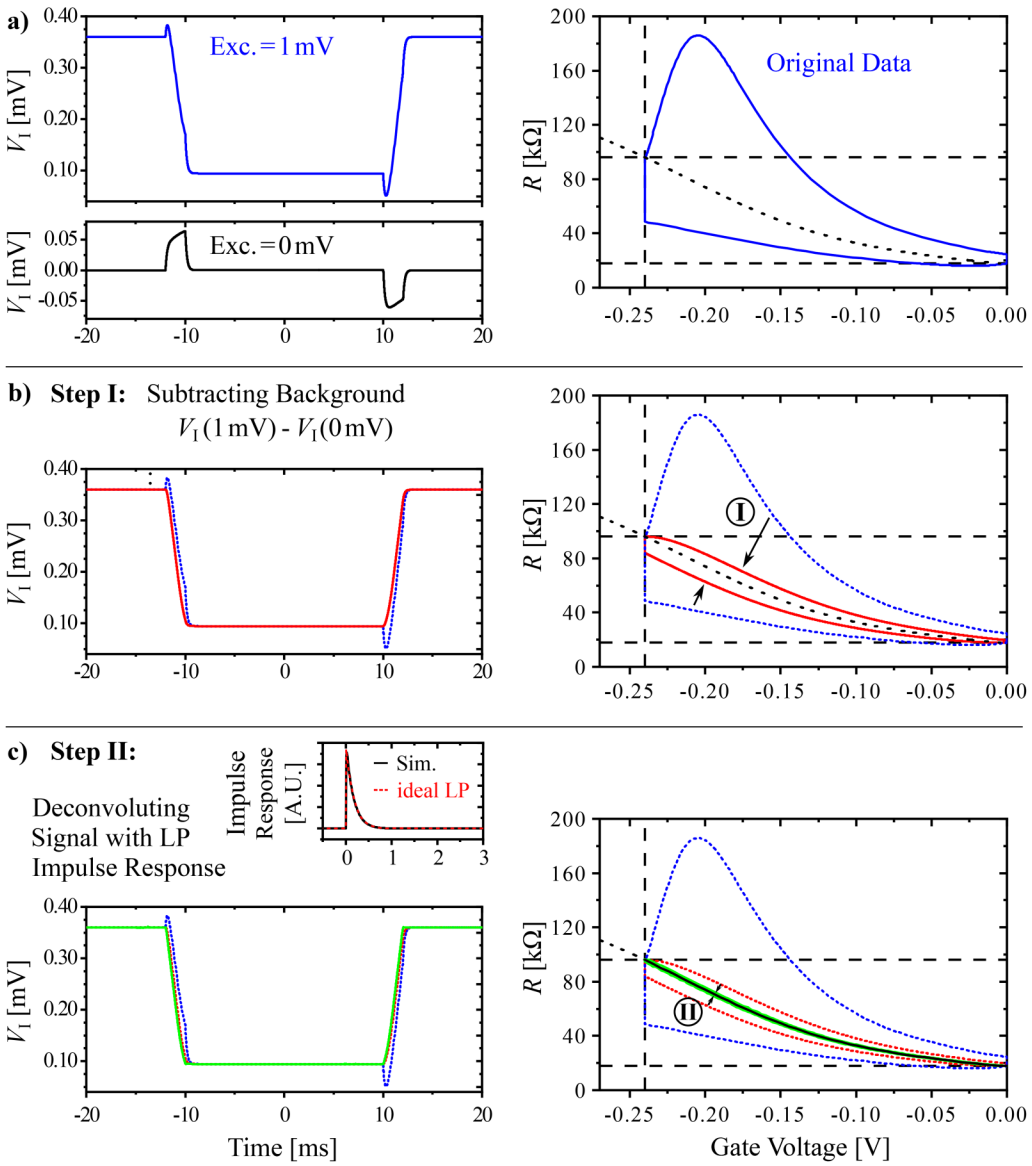

FIG. 3. Two-step recipe for extracting the steady-state equivalent gate sweeps from pulsed gate measurements. The procedure is illustrated for the simulated 2-20-2 pulse [cf. Fig. 2(c)], as short pulses naturally require the most post-processing. (a) The original data (1 mV DC excitation) are shown in blue as a function of time and gate voltage. The black dashed line represents the steady-state response of the circuit which is to be reconstructed. The response of the circuit to a gate pulse with zero DC excitation is also shown. (b) Step I: Subtracting the zero-excitation pulse from the original data leads to the red curve. This step eliminates the charging effects caused by charging the gate wiring capacitance during the pulse [C3 in the LTspice simulation, cf. Fig. 2(b)]. (c) Step II: Deconvoluting the signal with the circuit's impulse response (see the inset) results in the green curve. This step removes the low-pass-induced delay for monotonous signals (see the main text). The inset shows both the simulated circuit impulse response and that of an ideal first-order 1 kHz low-pass filter. The two-step procedure reproduces the steady-state lock-in equivalent to within 1%.

overshoot when plotted as a function of gate voltage (see the right panel). The remaining loop is monotonic and the remaining deviations can, therefore, be attributed to the low-pass effect, which is eliminated in step II. To reconstruct the steady-state signal from the low-pass-filtered one, filter response theory implies that the low-pass-filtered signal needs to be deconvoluted with the impulse response[20] of the circuit. The impulse response $g(t)$ of an arbitrary circuit can be simulated by the response to a step function (applied to the gate voltage) in LTspice, which is then differentiated and normalized. The result of our test circuit is shown in the inset of Fig. 3(c). As the circuit's low-pass response is dominated by the first-order low-pass output filter with a cutoff frequency of

$\nu_{-3dB} = 1$ kHz, the impulse response can also be calculated analytically: $g(t) = 2\pi\nu_{-3dB}\exp(-2\pi\nu_{-3dB} \cdot t)$.[21] The simulation and the textbook formula agree to high precision, confirming that the output filter dominates in this limit.

The deconvoluted signal is shown in green in Fig. 3(c). The hysteresis is now completely removed, and only minor deviations between the gate pulsing signal and steady-state response remain, which we attribute to the finite numerical precision during the deconvolution step. Hence, we have shown that this simple two-step recipe can be used to reconstruct the steady-state signal from a strongly distorted pulse transient.

Regarding step II, an additional remark is important: The reproduction of all original features of a signal upon deconvolution only works when the signal changes monotonically on the timescale of the filter impulse response. This requires a separate treatment of the two signal flanks of the pulse. Furthermore, this will not generally work for more complex signal shapes, e.g., in Sec. II C. Therefore, it is advisable to reduce low-pass effects in the circuit as much as possible, in our case, for example, by using the 100 kHz low-pass stage of the Femto amplifier. The recorded signal would then be more susceptible to radio frequency noise, but this can readily be removed by digital filters during the data analysis.

Trying to replicate the fast pulsed DC measurements with lock-in techniques would be very difficult. The lock-in amplifier would need to operate at a modulation frequency larger than the cutoff of the low-pass filter formed by wiring capacitance and sample resistance, which is on the order of 1 kHz, to provide a useful time resolution. Hence, even when considering the circuit presented in Fig. 2(b) at a fixed gate voltage, the excitation signal is attenuated and phase shifted in a complex manner that is highly dependent on the applied gate voltage (device resistance) and, thus, makes it *a priori* much more difficult to reconstruct the true device resistance.

C. Pulsed measurements of the quantum Hall effect

In this section, we apply the pulsed gate technique to measure a gate sweep of the Hall bar sample at a magnetic field of 5 T. We measure the longitudinal resistance R_{xx} and the transverse resistance R_{xy} as depicted in Fig. 1. For our sample and at that field, we expect to see quantum Hall effect plateaus with values $R_{xy} = R_K/\nu$, where ν is an integer and R_K is the von Klitzing constant. Along with this quantization in R_{xy} comes a non-monotonic R_{xx}, which approaches zero when R_{xy} is on a plateau value and peaks at transitions between them.[22]

To demonstrate that the gate-pulsing technique is robust in measuring this quantum transport effect, we pick out the fastest pulse type from Sec. II B, the 2-20-2 pulse. In this measurement, the trapeze-like pulse ranges from +0.24 to −0.1 V. This measurement also uses the 1 kHz low-pass filter in all three pre-amplifiers that are set to a gain of +60 dB. First, a gate pulse measurement with a bias of 1 mV is recorded. A zero-bias measurement is recorded shortly after and subtracted from the measurement, as discussed previously. The resulting corrected time transients of the three recorded voltages are shown in Fig. 4 (left). The pale curves show the raw data after background subtraction, while the full-colored curves include digital filtering with a

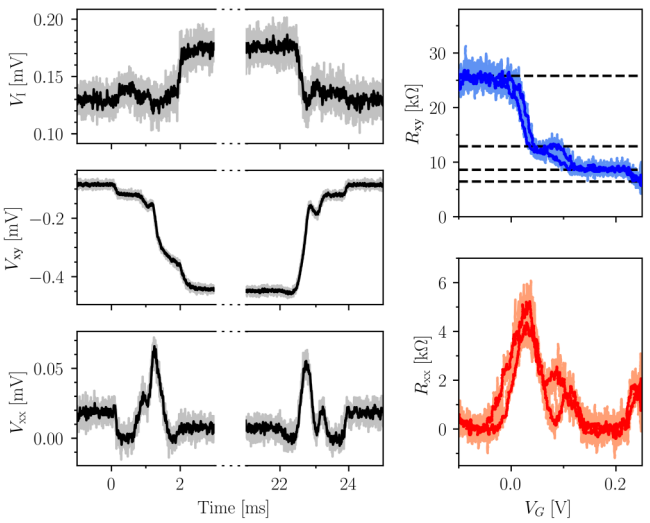

FIG. 4. Measurement of the quantum Hall effect by using a 2-20-2 pulse at 4.2 K. The left side shows the individual voltages (current V_I, transverse V_{xy}, and longitudinal V_{xx}) as a function of time. The plots on the right show the transverse (R_{xy}) and longitudinal (R_{xx}) resistance mapped to the gate voltage. The dashed lines indicate the quantum Hall plateaus $R_\nu = R_K/\nu$ with the von Klitzing constant R_K. The $\nu = 2$ plateau is resolved in about 200 μs. The subtraction of the zero-bias pulse was applied to the presented data, but no deconvolution step was performed. The dark curves are the result of light digital filtering (using a 100 μs wide Hanning window), while the pale curves show the raw data.

bidirectional 1 kHz low-pass filter. On the right, we show R_{xy} and R_{xx} against gate voltage. R_{xy} clearly shows quantized plateaus with the dashed lines corresponding to the $\nu = 1$, 2, 3, and 4 plateaus. States as short-lived as the $\nu = 2$ plateau, which is only observed for around 200 μs, are resolved. R_{xx} shows the expected drop toward zero resistance whenever the Hall resistance shows a quantized plateau.

The deconvolution from Sec. II B is skipped here, as the individual voltages are strongly non-monotonic (see V_I, which factors into both R_{xx} and R_{xy}) and are therefore deformed by low-pass effects in a way impossible to reconstruct unambiguously. The low-pass effect is why R_{xx} and R_{xy} show a slight hysteresis in general, and in particular around the short-lived $\nu = 2$ plateau.

The qualitatively and quantitatively correct observation of the quantum Hall effect proves that our time-dependent gate pulsing technique is capable of resolving complex quantum transport effects at a small bias of only 1 mV and within 2 ms. Slower pulses would work even better and changing the low-pass filter setting from 1 to 100 kHz would reduce the remaining distortion/hysteresis effects (if the noise level allows for it). The first application presented in Sec. III uses 1000 ms flanks.

The data presented in Fig. 4 are relatively noisy compared to conventional lock-in measurements of the quantum Hall effect in similar samples.[17–19] We attribute the noise floor (order ∼20 μV, which is around 2% of the applied bias) to pickup by the circuit outside the cryostat, which is not averaged out on the time scale of

our measurement. An obvious solution might be to place the amplifiers inside the cryostat where they are shielded. In conventional lock-in measurements, this noise is eliminated due to strict phase and frequency locking between bias and measured signal. Another difference to the lock-in measurements is the much larger input impedance of the differential pre-amplifiers (1 TΩ compared to 10 MΩ). This generally also increases noise due to worse impedance matching between source and amplifier.[1]

III. APPLICATIONS

A. Fast acquisition of two-dimensional maps

For purposes of material or device characterization, it is often necessary to study transport properties as a function of several parameters. A common way of displaying data to provide a quick overview over large parameter spaces is two-dimensional (often false-color) maps, in which a certain key property such as the conductance is shown in dependence of two input parameters. In semiconductor devices, the first parameter is commonly either the gate voltage or the voltage bias. Prominent choices for the second parameter include magnetic field B or device temperature T.

The pulsed gate technique introduced above allows for a fast and thus efficient way of recording such maps: First, a slow continuous sweep of the secondary parameter (e.g., magnetic field or temperature) is initiated. While the second parameter continuously changes, we perform pulse measurements that are fast compared to the sweep rate of the second parameter. This ensures that every pulse occurs at a quasi-fixed value of the second parameter.

Contrary to the conventional approach, this method results in significant time savings and often even higher resolution maps. The conventional approach is to record the maps by stepwise increasing the secondary parameter and recording a steady-state gate sweep. As a sweep using steady-state techniques takes on the order of minutes to finish, a map with hundreds of steps in the second parameter can take tens of hours or even days to record, depending strongly on the resolution in both dimensions. Compared to this, the gate-pulsing approach essentially reduces the time to the duration of a single one-dimensional sweep of the second parameter, which can easily reduce the measurement time by more than a factor of ten.

We apply the gate-pulsing technique to the two-dimensional map of the quantum Hall effect (R_{xx} and R_{xy}) against gate voltage and magnetic field (also known as a "Landau level fanchart," as the plateau transitions occur when the Fermi energy crosses with the Landau levels). The gate voltage is thereby the first parameter, while the magnetic field is the second parameter. The goal is to construct the two-dimensional map of the derivative of the transverse conductance σ_{xy} as a function of magnetic field and carrier density—essentially mapping out where the transitions between quantum Hall plateaus occur. The carrier density is linear in gate voltage and is extracted from the low-field Hall response.

A steady-state map as well as a gate-pulsing map are recorded to compare the two approaches (see Fig. 5). The steady-state map consists of 400 individual gate sweeps done in 20 mT steps, using an AC bias of ∼1 mV. It took around 18 h to record. The gate-pulsing map is performed using a sweep rate of the magnetic field of 0.1 T min^{-1} and rise times of 1 s for the gate pulses, resulting in a change in magnetic field during a single pulse of 1.6 mT—a significant improvement over the 20 mT step size of the steady-state approach. The fast approach only took 80 min to complete—more than 10 times faster compared to the steady-state approach and simultaneously at a higher resolution in magnetic field.

Comparing the two techniques reveals that the gate-pulsing technique and steady-state technique precisely reproduce the same two-dimensional map (see Fig. 5). The gate-pulsing technique even outperforms the lock-in technique when it comes to the sharpness of transitions, especially in small magnetic fields. Furthermore, the transition between $\nu = 1$ and $\nu = 0$, which is a transition between the $\approx 25.8\,\mathrm{k\Omega}$ plateau and the insulating regime $\gg \mathrm{M\Omega}$, is smoother when measured by the fast DC technique. We attribute the latter to the integration time constant of the lock-in amplifiers, which causes smearing when large impedance changes are covered in a sweep.

It should be noted that the reduced measurement time not only allows for time savings in the home lab, but is essential when relying on large user facilities as the National High Magnetic Field Laboratory (MagLab)[23] or the European Magnetic Field Laboratories (EMFL)[24] to measure high magnetic field fan charts in the limited measurement times.

To conclude this section, we would like to briefly comment on the measurement equipment and post-processing. We use a *NI 6212* computer card to record the output of the amplifiers and to apply the gate pulses simultaneously. During the measurement, the data are streamed to a measurement PC, which allows us to handle and save the data immediately. Additionally, the synchronization between the gate pulse and the recorded signal becomes trivial. Compared to the oscilloscope employed in Sec. II, the computer card features a much smaller sample rate with 50 kS s^{-1} per channel. This sampling rate is still more than sufficient for the long flank rise times of 1 s. The total amount of raw data for the shown map exceeds 2 GB. For economical plotting and data storage, we apply a running-average resampling scheme to 500 data points in gate voltage direction, resulting in < 50 MB per map without significant loss of measurement features. The zero-excitation pulse subtraction discussed in Sec. II B is skipped here, as the long rise time significantly surpasses the timescale of any (dis-)charging effects in the circuit, simplifying the process even more.

B. Pulsed magnetic field quantum Hall effect

We now use the fast DC measurement technique to probe transport features that are intrinsically inaccessible when using steady-state lock-in techniques:[25] We measure the quantum Hall effect in a pulsed magnetic field all the way up to 65 T in less than 100 ms. The measurement shown in this section is performed at the Hochfeldlabor Dresden (HZDR, EMFL).[2] We discuss a measurement up to ∼20 T and up to ∼65 T to highlight the applicability of the fast low-bias DC technique and its limitations. The magnetic field transients applied are shown in the insets of Fig. 6. The electronic circuit is the same as discussed before but without a gate electrode. When the magnetic field pulse is initiated, a *Yokogawa DS850* transient recorder is triggered accordingly, which saves the voltage transients along with the magnetic field response (by using a pickup coil in close proximity to the sample).

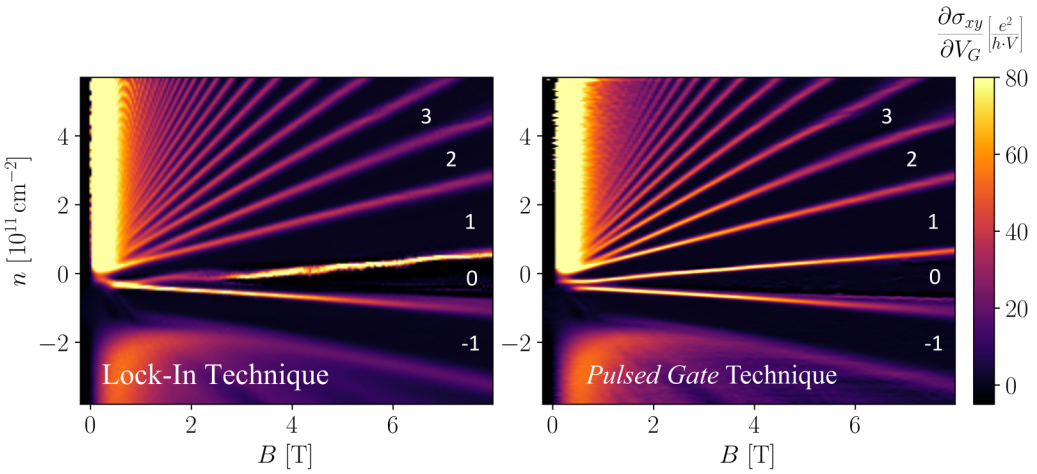

FIG. 5. Application I: Comparison of two two-dimensional false-color maps using conventional steady-state lock-in techniques (left) and using the pulsed gate technique introduced here (right). The two-dimensional maps show the derivative of the transverse conductance σ_{xy} as a function of magnetic field B and carrier density n (see the main text for details and physical background). White numbers indicate the quantum Hall plateaus and 0 represents the band insulator phase. It is important to note that the conventional lock-in technique took 18 h to complete, while the pulsed gate map was completed in 80 min. The temperature is 1.4 K.

When performing measurements in pulsed magnetic fields using a small voltage bias, subtracting the zero-excitation response of the circuit is essential. Not only charging effects of the wires due to impedance changes, as extensively discussed in Sec. II B, can be eliminated, but also the (reproducible) induced pickup voltage that is proportional to $\mathrm{d}B/\mathrm{d}t$.[26] Therefore, two consecutive magnetic field pulses are necessary for each measurement. The result of a pulsed magnetic field sweep until ∼20 T is shown in Fig. 6(a). The pale curves show the uncorrected raw measurement, while the saturated colors show the result after subtracting the zero-excitation pulse. The dark curves represent the latter after 500 Hz FFT filtering. Especially in R_{xy}, non-reproducible oscillations on top of the quantum Hall ladder are observed, which is most obvious around the nominally flat quantum Hall plateaus. In steady-state measurements on similar devices (similar material stack and lithographic processing), such non-reproducible features are not observed.[19,27] The non-reproducible oscillations are attributed to pickup induced by chaotic vibration of the sample in the large magnetic field due to the strong forces created by the magnetic field pulse, which are not precisely reproduced between pulses and therefore not eliminated by subtracting the zero-excitation measurement. To counteract this, we had to increase the bias to 5 mV in the measurement up to ∼20 T to increase the signal-to-noise ratio (and hence also reduce the amplifier gain to 40 dB). Irrespective of the vibrations, the typical harmonic quantum Hall effect ladder is well resolved, proving the viability of the fast low-bias DC technique when the magnetic field is the quickly swept parameter.

A magnetic field pulse until 65 T, which is higher than any magnetic field accessible in a DC magnet system, for the same device is shown in Fig. 6(b). The quantum Hall effect is observed in the whole magnetic field range in R_{xx} and R_{xy}. As the vibration-based non-reproductive pickup scales significantly more-than-linear with the magnetic field,[28] a reasonable signal-to-noise ratio [see Fig. 6(b)] has been achieved by an increase in the voltage bias to 50 mV. At this voltage bias, charging effects and reproducible pickup are negligible compared to the vibrations. Therefore, the zero-bias subtraction is skipped, as it only increases the noise floor further. Instead, digital FFT filtering is used to remove the dominant frequencies of the non-reproducible pickup at large magnetic fields.

To measure transport at the largest magnetic field (≫ 20 T) with a small voltage bias (order 1 mV), the non-reproducible pickup needs to be reduced significantly. To reduce the vibration-based pickup in future experiments, the use of twisted pair wiring all the way to the device contacts (skipping wire-bonding in a chip carrier that inevitably results in loops formed by the bonding wires) as well as a sample design with limited area is strongly recommended. In the latter, the correction of the remaining pickup as well as charging effects via the zero-bias subtraction will be indispensable.

As shown by van der Burgt *et al.*,[14] the influence of (wiring) capacitances parallel to the current path of the Hall bar can also lead to distorted quantum Hall plateaus. Especially for highly resistive current paths and large parallel (to the current path) capacitances, they observe an initial overshoot followed by undershooting the end of the plateau, while no distortions are observed in the middle of the plateau, where $R_{xx} = 0$. van der Burgt *et al.* also derive a model, which allows reconstructing of the original flat plateaus from the distorted measurements. This situation, however, does not seem to apply in our case, as the distorted shape does not really match and also the resistance of the current path in our device is fairly low (due to the large channel width of 200 μm). Furthermore, subtracting the zero-excitation pulse also already largely accounts for this effect as well. For other sample and wiring geometries, the effect identified by van der Burgt *et al.* might become (more) significant and is hence mentioned for the sake of completeness.

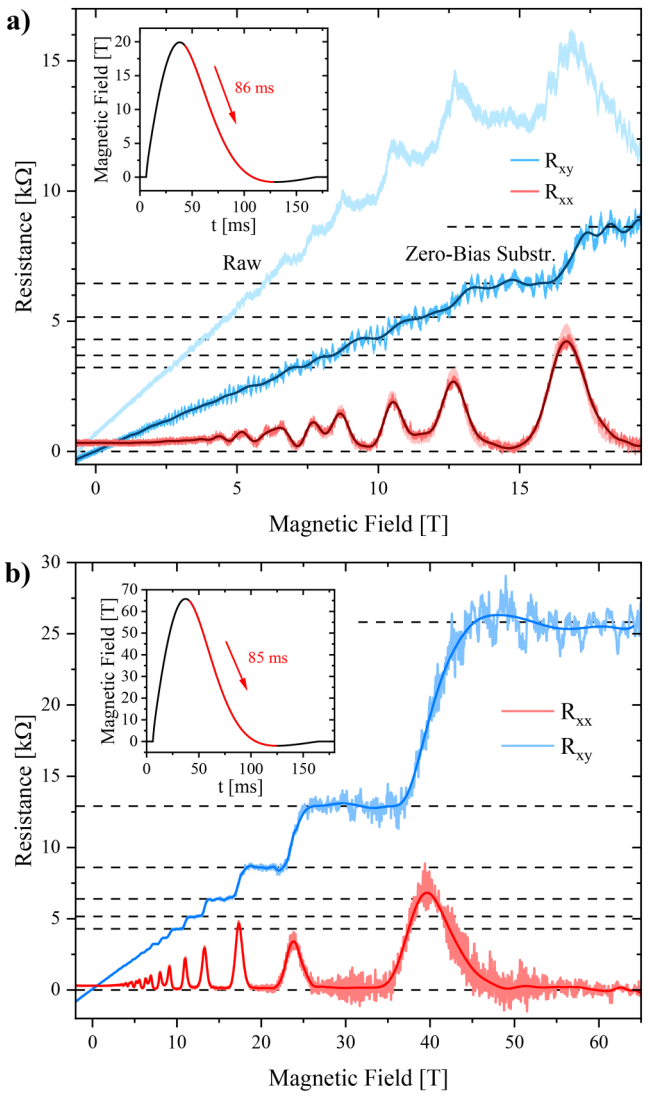

FIG. 6. Application II: Quantum Hall effect measured in a pulsed magnetic field. Shown are the longitudinal resistance R_{xx} (red) and transverse resistance R_{xy} (blue) as a function of magnetic field B at 4.2 K. The insets show the magnetic field pulses as a function of time t. The measurement is conducted during the approximately 85 ms long falling edge of the pulses. (a) A magnetic field pulse up to ca. 20 T using a voltage bias of 5 mV. The pale curves are the raw data, while the medium tone indicates the results after subtraction of the zero-excitation reference. The dark curve is the corrected data after a digital 500 Hz FFT filter. (b) A magnetic field pulse up to ca. 65 T using a voltage bias of 50 mV. The pale curve is the raw data, while the dark tone indicates the resistance after digital filtering.

This technique is especially interesting for investigating highest-field phenomena, as pulsed magnetic fields up to 100 T are readily available at user facilities.[23,24] For example, the $\nu = 1$ to 0 insulator transition that is already observed in Fig. 5 can be studied at larger carrier densities. Additionally, a competing Mott-like insulator transition that is expected to occur for low-density two-dimensional electronic systems at very large magnetic fields can be probed. Furthermore, materials with high intrinsic density, narrow Landau level spacing, or studies at elevated temperatures can benefit from the very large magnetic fields (for example, the discovery of the room temperature quantum Hall effect in graphene[29]).

IV. FINAL REMARKS

In this paper, we present an overview of low-bias ($\lesssim 1$ mV) DC transport measurements in dependence of an externally controlled parameter like the gate voltage on timescales as fast as a few milliseconds. The electric circuit is discussed and modeled with an LTspice simulation, including a discussion of the most prominent measurement artifacts that arise at these fast time scales. A comparison to an actual measurement confirms all predictions of the simulation. The result of the successful circuit analysis is a simple protocol for eliminating the measurement artifacts of such measurements reliably. This is applied to a quantum transport measurement to quickly ($\ll 1$ ms) resolve transitions between quantum Hall plateaus.

We introduce two practical applications where the fast DC approach clearly outperforms traditional steady-state transport measurement such as low-frequency lock-in techniques. The first application is a ten times faster way to record two-dimensional (false-color) maps in dependence of gate voltage and magnetic field compared to traditional techniques. The second application covers transport measurements in pulsed magnetic fields, which is inaccessible using steady-state techniques for semiconductor samples.

We show that traditional steady-state techniques, such as lock-in measurements or DC measurements with long integration time, can often be replaced by fast DC transport measurements. Specially in the field of material and device characterization, the latter allows for a very significant increase in sample throughput and thereby savings in operating costs. The transport measurement technique is rather simple to operate, does only require affordable and non-specialized test equipment, and can be modeled with widely available software such as LTspice. As we include a versatile scheme to analyze and correct for measurement artifacts, it can be adapted to a wide range of test applications. Therefore, the fast low-bias DC transport technique presented in this review turns out to be a valuable tool for semiconductor characterization purposes in addition to the traditional steady-state techniques.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

C. Fuchs: Formal analysis (lead); Investigation (lead); Software (equal); Writing – original draft (equal). **M. Hofer:** Formal analysis (supporting); Investigation (supporting); Software (equal); Writing – original draft (equal). **L. Fürst:** Resources (lead). **S. Shamim:** Formal analysis (supporting); Investigation (supporting). **T. Kießling:** Conceptualization (equal); Formal analysis (supporting); Investigation (supporting); Writing – review & editing (equal). **H. Buhmann:** Conceptualization (equal); Supervision (equal); Writing – review & editing (equal). **L. W. Molenkamp:** Conceptualization (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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