



Electrical characterization of a single-crystalline Si quantum well formed by thermal oxidation of ultrathin silicon-on-insulator film (Al/SiO₂:c-Si QW/n-Si) for optoelectronic applications

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Abstract

The incorporation of nanostructures such as silicon nanocrystals into the oxide of an MOS structure has attracted significant interest in improving the performance of MOS-based devices. However, integrating crystalline silicon quantum wells into this structure remains a challenge due to the difficulties associated with growing a crystalline Si film on an amorphous oxide. This study presents the fabrication and electrical characterization of a quantum well formed by the thermal oxidation of an ultrathin silicon-on-insulator (UT-SOI) film. Structural analysis by electronic transmission reveals the formation of a monocrystalline quantum well with a homogeneous thickness and a perfectly flat surface, free from any crystalline defect. The electrical characterizations, carried out using capacitance–voltage (C–V) and current–voltage (I–V) measurements, confirm the success of the integration of the quantum well into the MOS structure. In addition, a systematic study of the dielectric properties details the evolution in bias voltage and in frequency of the main dielectric parameters of the structure such as the dielectric constant (ϵ^*), the electrical loss ($\tan \delta$), and the electrical modulus (M^*). The results obtained demonstrate normal operation of the new structure, paving the way for efficient integration of this type of nanostructures in MOS-based photodetectors and solar cells.

Keywords Silicon quantum well · SOI · MIS structures · Electrical and dielectric properties of MIS structures · Thermal oxydation of SOI

1 Introduction

The significance of silicon in modern technology has been exemplified through its multifaceted properties and widespread applications across diverse industries. Its abundance, coupled with exceptional electrical properties, has established silicon as a cornerstone material in materials science and technology. Previous studies have extensively explored various silicon nanostructures, including porous silicon, silicon nanocrystals, and silicon nanowires, showing

their unique characteristics and potential applications. For instance, the work of Canham demonstrated the remarkable optical properties of porous silicon, paving the way for its utilization in sensors, optoelectronics, and biomedical applications [1].

In the realm of industry and technology, silicon nanostructures have played an instrumental role, particularly in CMOS technology. The integration of silicon nanostructures into CMOS technology has been highlighted by several research [2–5], showing their potential to enhance device performance and energy efficiency in microelectronics. Silicon nanostructures find applications in microelectronics by providing innovative solutions for miniaturization, increased performance, and reduced power consumption. For example, silicon nanowires have shown promise in field-effect transistors (FETs) with enhanced electrical properties due to their one-dimensional nature [6].

Within the vast diversity of silicon nanostructures, this article focuses specifically on a still unexplored avenue: the creation of silicon quantum wells on insulators. By taking

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advantage of pre-existing work on the integration of quantum structures such as silicon nanocrystals and nanowires, which have proven their great relevance in improving the performance of MOS devices for photodetection and energy harvesting applications [7, 8]. This study aims to fabricate silicon quantum wells on insulators using partial thermal oxidation of Silicon-on-Insulator (SOI) substrates. Notably, the advantages and characteristics of Silicon-On-Insulator (SOI) structures play a pivotal role in enabling this novel fabrication method [9–11].

SOI technology involves the use of a thin layer of silicon (the active layer) on an insulating substrate, typically made of silicon dioxide. The key advantage of SOI lies in its ability to eliminate parasitic capacitance and improve device performance. These results in enhanced speed, reduced power consumption, and increased radiation tolerance, making SOI an ideal platform for advanced semiconductor devices [9, 12, 13]. Furthermore, SOI structures are known for better isolation between devices, reducing crosstalk, and improving overall device reliability.

The incorporation of quantum wells or quantum dots within the oxide layer opens up a myriad of possibilities for advanced MOS-type photodetectors, light-emitting diodes (LEDs), sensors, and more. Silicon quantum wells integrated into the oxide layer offer enhanced light absorption capabilities, making them ideal candidates for high-performance photodetectors. By leveraging the quantum confinement effect, these devices can achieve superior sensitivity and response characteristics, catering to various applications in optical communication, imaging, and sensing. The utilization of silicon quantum wells in the oxide matrix presents an intriguing avenue for the development of efficient silicon-based LEDs. Quantum confinement effects enable precise control over the emission wavelength, facilitating the realization of tunable and high-brightness light sources. This innovation holds promise for diverse applications ranging from display technologies to optoelectronic integrated circuits. MOS structures incorporating quantum wells or dots offer unique advantages in sensor applications. The confinement-induced modulation of electronic properties enables sensitive detection of environmental changes, such as light intensity, temperature, and gas composition. By exploiting these quantum phenomena, MOS sensors can achieve enhanced performance metrics, including sensitivity, selectivity, and response time, thus addressing critical needs in fields such as environmental monitoring, biomedical sensing, and industrial process control.

Understanding the electrical transport properties of silicon quantum wells becomes imperative, as highlighted in previous studies on quantum well devices [14, 15].

Hence, this paper underscores the significance of employing impedance spectroscopy to assess dielectric properties, interface states, performance, and equivalent circuits.

Several research demonstrates the efficacy of impedance spectroscopy in analyzing and optimizing the performance of semiconductor devices, emphasizing its importance in evaluating the novel electrical behavior of silicon quantum wells [15–22].

By delving into this uncharted territory, this study not only aims to uncover the untapped potential of silicon quantum wells (Si QWs) but also emphasizes the critical need to comprehend their electrical properties for future technological advancements and innovations.

2 Experimental

In this experiment, a novel approach was undertaken to fabricate high-quality crystalline silicon quantum wells (c-Si QW) embedded in a SiO₂ matrix utilizing a distinctive method: partial oxidation of an ultrathin silicon-on-insulator (SOI) via thermal oxidation process in a Jet First 200-type Rapid Thermal Processor (RTP). The SOI substrate consisted of a monocrystalline silicon film isolated from the silicon substrate by a buried oxide (BOX) with a thickness of 25 nm, while the top silicon film had a thickness of 10 nm and was n-type doped (10^{15} cm^{-3}). The oxidation process, conducted at 1000 °C in an O₂ flow of 200 SCCM, was meticulously controlled using the Jet First 200-type furnace, enabling precise regulation of temperature, gas flow, and oxidation time. This meticulous control facilitated the creation of ultra-thin SiO₂ layers with a homogeneous thickness and high-quality Si/SiO₂ interfaces, validated through electrical assessments. Structural evaluations were performed using transmission electron microscopy to analyze the fabricated structures.

To assess electrical and dielectric properties, the c-Si QW was metallized by depositing a transparent aluminum layer via magnetron sputtering deposition. Subsequent electrical transport studies were conducted utilizing an HP 4140B PA Meter DC Voltage Source-type instrument with a measurement resolution of 10^{-15} A . Current–voltage (I–V) measurements were performed at room temperature using a gold-tipped contact on the sample's front face, while the rear face was securely affixed to a mechanical support using silver lacquer to establish good ohmic contact (Fig. 1). Voltage ramps ranging from -30 V to 30 V with steps of 100 mV were applied to the sample during the measurements.

Moreover, a HP/Agilent 4192A LF-type impedance analyzer equipped with an HP/Agilent 16034E test fixture, incorporating gold-plated tips and interfaced to a PC via LabView software, was employed to conduct precise impedance measurements. The analyses encompassed capacitance, conductance, and impedance characteristics as functions of frequency (C-F, G-F, and Z-F) and voltage (C-V, G-V, and Z-F) across a wide frequency range (5 Hz to 13 MHz) under

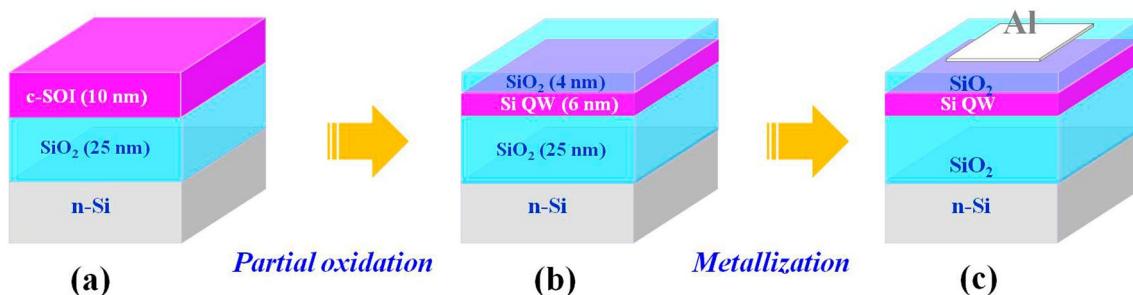


Fig. 1 A schematic illustration delineates the specific steps in the fabrication process of a crystalline quantum well, embedded within the oxide layer of an MOS structure: (a) chemical cleaning of an ultra-

thin SOI substrate; (b) rapid thermal oxidation; and (c) metallization and the formation of the MOS structure

various bias voltage values. These meticulous experimental setups allowed for comprehensive evaluations of the electrical and dielectric properties of the fabricated silicon quantum well structures.

3 Results

Within the realm of creating silicon quantum wells on SiO_2 , we introduce a novel approach for fabricating a crystalline silicon quantum well seamlessly integrated into the core of a MOS (metal–oxide–semiconductor) architecture. This significant milestone is realized through an innovative technique based on the precise partial oxidation of the SOI substrate.

The TEM image shown in Fig. 2 provides an intricately detailed perspective, accentuating both the exquisite crystallinity of the silicon quantum well and the meticulous uniformity of the film thicknesses embedded in the oxide of the MOS structure. Notably, the illustration unveils a 6 nm thickness for the silicon quantum well, flanked by oxide layers measuring 3 nm on top and 25 nm beneath the Si quantum well. The conspicuous absence of any

discernible structural defects serves as a testament to the exceptional quality of the quantum well produced through this method of partial oxidation of the SOI substrate.

This particular configuration of the obtained MOS structure enabled the exploration of the vertical transport through the quantum well, embedded in the oxide, between the substrate and the aluminum gate through the measurements of the capacitance–voltage (C–V) and current–voltage (I–V) characteristics. Figure 3a displays the evolution of the capacitance–voltage characteristic, measured on this MOS structure integrating the silicon quantum well, at a high frequency of 1 MHz. This curve reveals the three characteristic regimes of MOS-type capacitance: inversion, depletion, and accumulation, demonstrating that the electrical transport in the structure remains mainly dictated by the oxide, even in the presence of the quantum well. Figure 3b reveals the I–V characteristic obtained. The detailed analysis of this I–V curve reveals the typical rectification behavior of a PMOS-type Schottky diode, characterized by a rectification ratio of 100. Indeed, the insertion of the silicon quantum well within the oxide plays a crucial role in facilitating the transfer of charges through the upper and lower layers of the substrate oxide

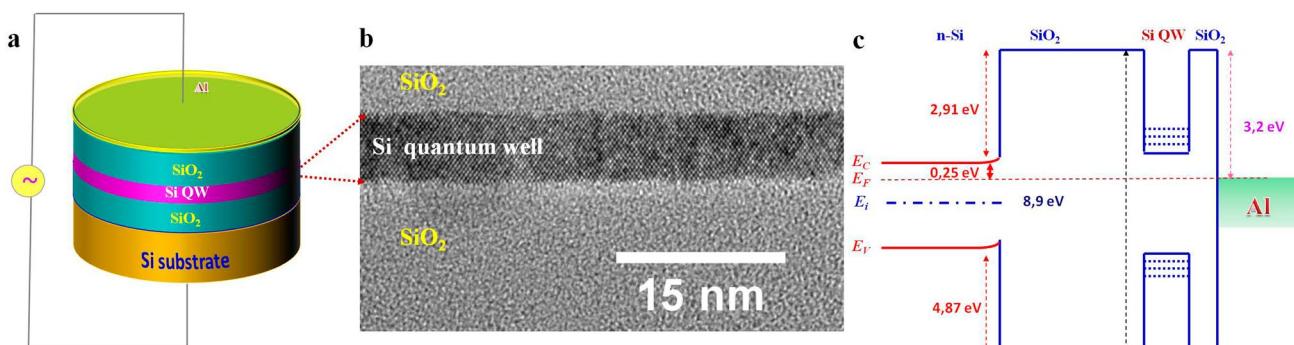


Fig. 2 **a** Depict the structure diagram of the MOS structure with Si QW; **b** Show TEM image, emphasizing a crystalline silicon quantum well buried within the oxide layer of a metal–oxide–semiconductor

(MOS) capacitor, measuring 6 nm in thickness; **c** shows the energy diagram of the structure

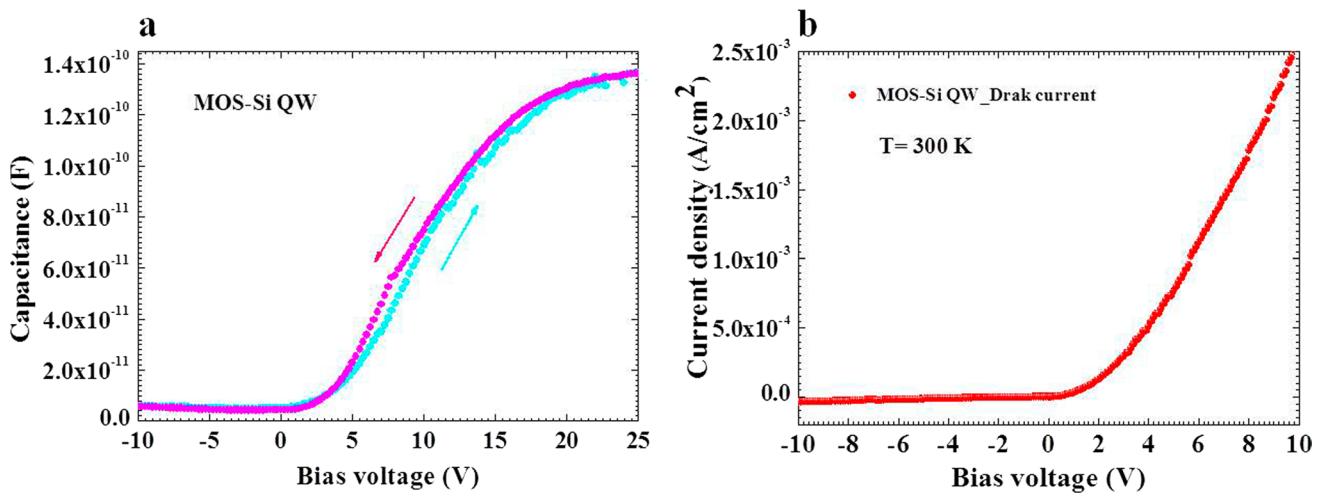


Fig. 3 **a, b** Display the characteristic C–V and I–V curves, respectively, for the MOS with an embedded Si quantum well (MOS_Si QW)

to the aluminum gate, thanks to the Fowler–Nordheim effect.

Figure 4a, b illustrate the representative curves of capacitance–voltage (C–V) and conductance–voltage (G–V) at various frequencies. A remarkable observation is the decrease in capacitance as frequency increases. This significant trend was corroborated by the analysis of capacitance and conductance measurements as a function of frequency, detailed respectively in Fig. 8a, b. The dispersion of the capacitance in frequency can be attributed to the presence of the interface states [23–27]. These states, unable to effectively follow the electrical excitation signal at high frequencies, encounter difficulty in sensing and emitting electrical charges, thus inducing a reduction in capacitance and an increase in conductance at these higher frequencies. Additionally, it is

possible that the interfaces associated with the quantum well inserted in the oxide of the MOS capacitance contribute to this dispersion of capacitance and conductance as a function of frequency.

In order to evaluate the influence of the quantum well and the interface states on the charge capture and emission rates in MOS structures integrating a quantum well in crystalline silicon, we used a High–low frequency capacitance method, as developed by Kar and Dahlke [28]. This approach allows us to quantify the evolution of the density of the traps present in the MOS structure as a function of the applied bias voltage (Fig. 5). The Kar and Dahlke method is widely recognized as a benchmark in the field, providing a reliable assessment of charge trap density in MOS structures [25, 29–33]. It is based on a specific

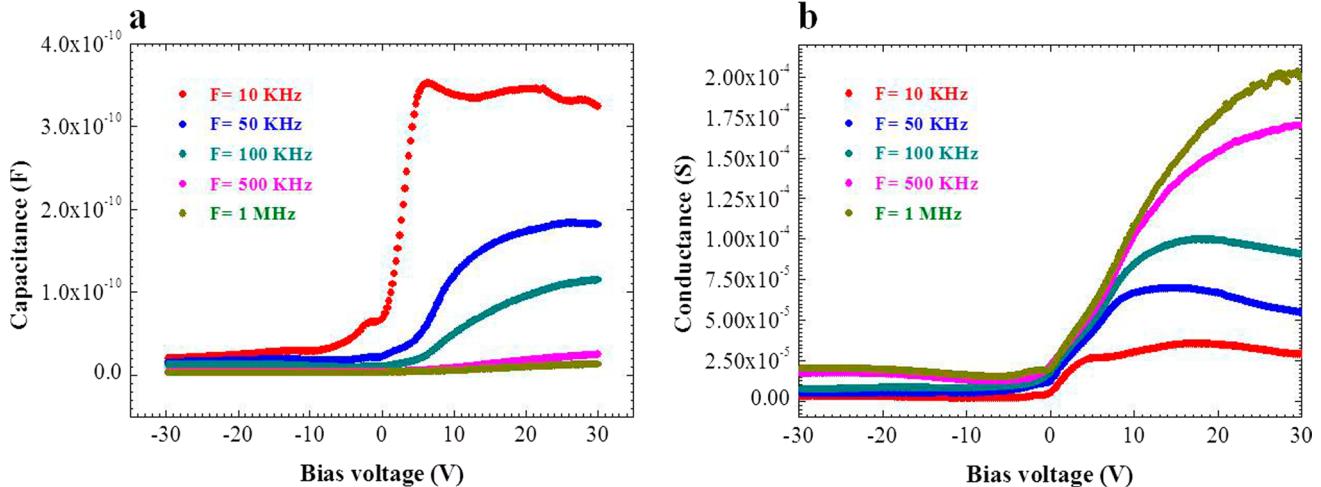


Fig. 4 **a, b** Respectively, present the capacitance–voltage (C–V) and conductance–voltage (G–V) characteristic curves of the MOS_Si QW structure at different frequencies

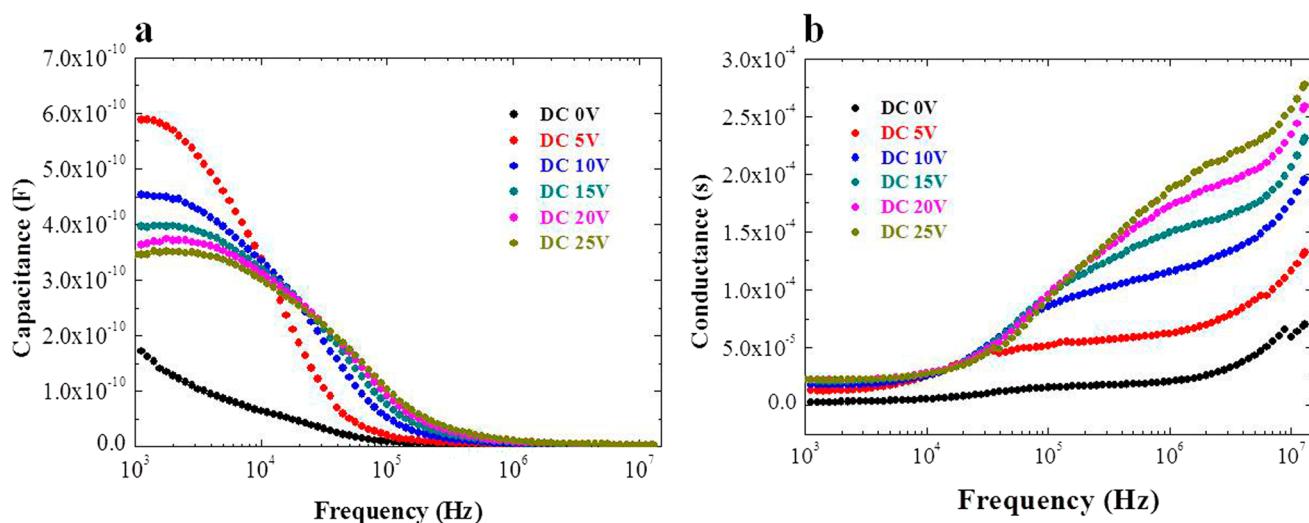


Fig. 5 **a, b** Show, respectively, the capacitance-frequency (C–F) and conductance-frequency (G–F) characteristics of the MOS_Si QW structure under different bias voltages

function commonly used for this type of calculation, thus providing an in-depth understanding of the charge capture and emission phenomena associated with MOS structures comprising crystalline silicon quantum wells.

$$N_{ss} = \frac{C_{OX}}{q} \left(\frac{C_{LF}/C_{OX}}{1 - C_{LF}/C_{OX}} - \frac{C_{HF}/C_{OX}}{1 - C_{HF}/C_{OX}} \right)$$

(C_{LF}) and (C_{HF}) correspond to the capacitances measured at low and high frequencies, respectively. Cox represents the capacitance of the oxide containing the silicon quantum well. The value of this capacity (C_{OX}) is calculated using the following equation:

$$C = \frac{A}{\frac{t_{Ox1} + t_{Ox2}}{\epsilon_{SiO_2}} + \frac{t_{SiQW}}{\epsilon_{Si}}}$$

In this equation, "A" symbolizes the surface area of the aluminum contact, while ϵ_{Si} and ϵ_{SiO_2} represent the dielectric constants of silicon and oxide, respectively. t_{Ox1} and t_{Ox2} denote the thicknesses of the oxide below and above the quantum well.

Figure 6 reveal the evolution of the charge trap density within the MOS_Si QW structures, calculated using the high-low method. This curve highlights a notable peak, reaching a height of $D_t = 6 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, observed at a bias voltage of $V_B = 1 \text{ V}$. This peak is attributed to the coexistence of interface states and the silicon quantum well. However, it is essential to emphasize that the density of the charge traps remains below the maximum tolerated limit for microelectronics applications. This finding confirms the viability of this structure for applications in

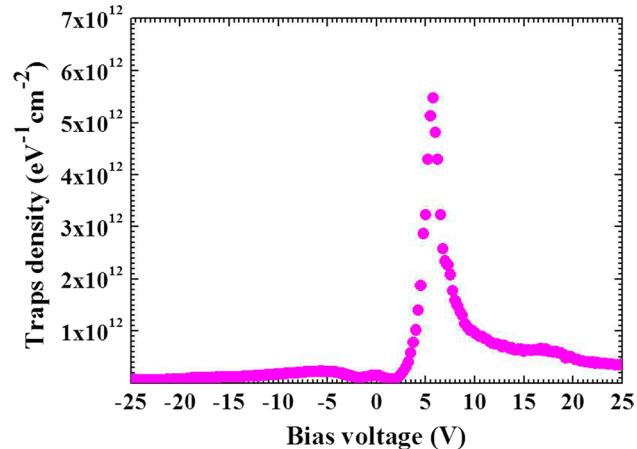


Fig. 6 This curve illustrates the variation of trap densities (D_t) as a function of bias voltage for MOS_Si QW

microelectronics highlighting electrical performances conforming to the required standards.

All these results undoubtedly show that the insertion of quantum wells in a MOS structure can modify the transport and trapping of charges in the MOS structure, which can modify the dielectric properties of the MOS structure.

The study of the dielectric properties of MOS structures is of fundamental importance in various fields of modern electronics. MOS (metal–oxide–semiconductor) are key components used in many microelectronic devices, such as field-effect transistors (FETs), MOS photo detector and integrated circuits. Understanding the dielectric properties of these structures is crucial to optimizing their electrical performance, reliability, and long-term integrity. Impedance spectroscopy is emerging as a precise and non-destructive

method for studying the dielectric characteristics of these structures.

This method is based on the principle of measuring variations in electrical impedance as a function of the frequency of the applied signal. It provides detailed information on the electrical and dielectric properties of materials, including interfaces, oxide layers, and semiconductor structures present in MOS. Impedance spectroscopy allows the assessment of key parameters such as conductivity, permittivity, density of interface states, and interface quality.

Its use has several significant advantages, including its high sensitivity to subtle changes in dielectric properties, its ability to probe very thin layers accurately, and its non-invasiveness, which allows measurements on functional devices. Additionally, it offers extended frequency resolution, allowing material behavior to be analyzed over a wide frequency range, which is crucial for high-frequency applications.

Previous research has shown the effectiveness of impedance spectroscopy in characterizing the dielectric properties of MOS [18, 26, 34–36]. This technique is well used to evaluate the dielectric properties of gate oxide layers of MOS-FET transistors. The results helped understand the effect of fabrication processes on electrical performance and helped optimize device quality [37–39].

In sum, impedance spectroscopy offers a powerful method to study the dielectric properties of MOS structures, thus paving the way for significant advances in the development of more efficient, reliable microelectronic devices suitable for various industrial applications.

Impedance measurements provide a powerful tool for determining the electrical permittivity of MOS capacitances [26, 35, 40]. The complex permittivity ϵ^* can be expressed by the following relation:

$$\epsilon^* = \frac{Y^*}{J\omega C_0} = \epsilon' - i\epsilon''$$

The real (ϵ') and imaginary (ϵ'') parts of the complex permittivity can be determined using the following expressions:

$$\epsilon' = \frac{C}{C_0} = \frac{Cd_{ox}}{\epsilon_0 A}$$

$$\epsilon'' = \frac{G}{\omega C_0} = \frac{Gd_{ox}}{\epsilon_0 \omega A}$$

In these equations, C and G represent the measured capacitance and conductance, respectively; C_0 is the capacitance of a vacuum capacitor; and ϵ_0 is the dielectric permittivity of the vacuum ($8.85 \cdot 10^{-14}$ F/cm). The parameters A and dox correspond respectively to the area of the contact deposited on the structure ($A = 3.14 \cdot 10^{-2}$ cm 2) and to the thickness of the interfacial insulating layer.

The loss tangent is defined by the relation: $\tan\delta = \frac{\epsilon''}{\epsilon'}$

The variations of the dielectric constant (ϵ') and the imaginary part of the permittivity (ϵ'') of the MOS_Si QW structure as a function of the bias voltage for different frequencies are shown, respectively, in Fig. 7a, b. These graphical representations provide a detailed perspective of the dielectric changes induced by the bias voltage, thereby providing a better understanding of the electrical behavior of the MOS_Si QW structure under varied conditions. This precise electrical permittivity information is essential to optimizing the design and performance of electronic devices associated with this particular structure.

At a bias voltage below -1 V for a MOS structure, the ϵ' and ϵ'' components demonstrate low values and maintain

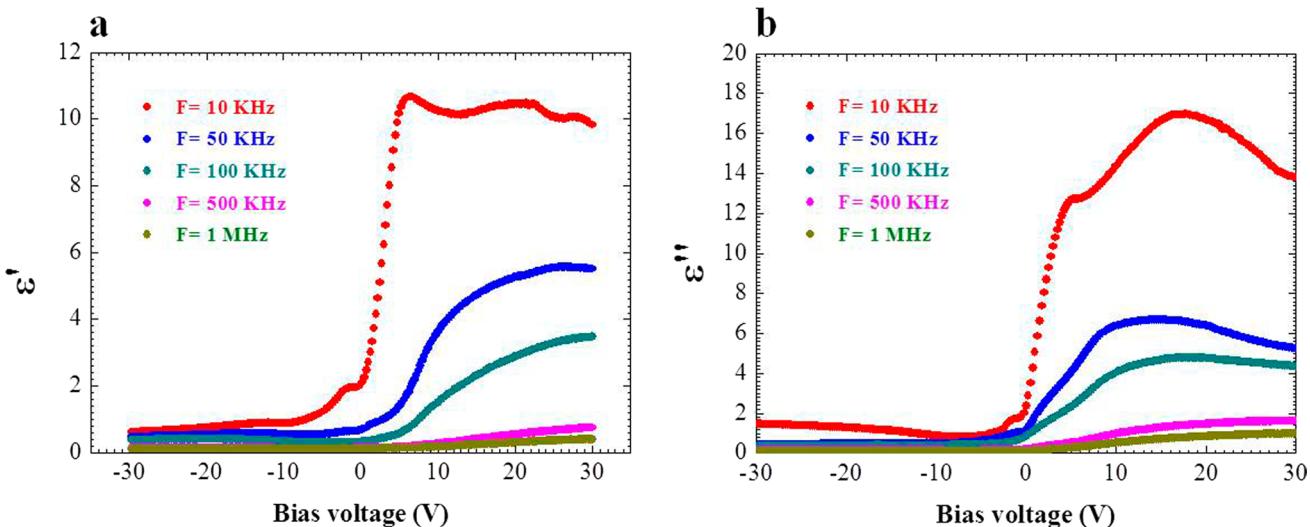


Fig. 7 **a, b** Illustrate, in a distinct manner, the evolution of the real component (ϵ') and the imaginary component (ϵ'') of the permittivity of the MOS_Si QW structure versus voltage polarization at different frequencies

their independence with respect to the frequency of the excitation signal. A striking example of this stability is observed in the work of Smith et al. (2018), where a voltage of -1 V applied to a similar structure generated constant values of ϵ' and ϵ'' independent of frequency.

In contrast, for a bias voltage greater than -1 V , these components exhibit relative bias voltage stability at high frequencies, but show significant variability at low frequencies. This feature was identified in Yang and colleagues' (2020) study of MOS at voltages above -1 V , where ϵ' and ϵ'' remained constant at high frequency but showed substantial variation at low frequency.

A common observation in several studies, such as that conducted by TATAROĞLU et al., is the frequency dispersion of these two components, ϵ' and ϵ'' [25–27]. They noted a progressive decrease in these components as the frequency increased. This reduction is often associated with the decrease in polarization with increasing frequency.

This progressive decrease can be attributed to the limitation of the electrons ability to follow the alternating signal beyond a certain frequency of the external field. This phenomenon is clearly evoked in the work of Tataroglu et al. on MOS structures, where frequency played a crucial role in the modulation of ϵ' and ϵ'' due to the constraints imposed by the type of interfacial polarization Maxwell–Wagner [25–27].

The results shown in Fig. 8a) depict the influence of frequency on the real part (ϵ') of the MOS_Si QW structure for various bias voltages. This observation is consistent with previous studies, such as that conducted by Tataroglu et al., who also observed a notable decrease in the ϵ' and ϵ'' components as a function of frequency for similar structures. These variations are often attributed to Maxwell–Wagner

effects, a phenomenon amplified by the specific structure of the interfaces.

Moreover, the values of these two components ϵ' and ϵ'' also demonstrated a decreasing tendency for the negative bias voltages studied in the MOS structure. This finding is consistent with literatures on similar polarization structures, where a gradual decay of ϵ' and ϵ'' was recorded with negative voltages, thus corroborating the current results.

Figure 8b presents the variation of the imaginary part of the permittivity (ϵ'') as a function of frequency for the MOS_QW structure. A clear decrease in (ϵ'') is observed as the frequency increases. This phenomenon can be explained by the intense interactions between dipoles at low frequencies, which weaken as the frequency increases, thus leading to a significant reduction in dielectric losses [25–27]. At high frequencies, electronic and ionic polarization mechanisms predominate, while at low frequencies, interface polarization takes center stage. Interfacial polarization, mainly induced by defects present at the Si/SiO₂ interface, contributes to the increase in the values of ϵ' and ϵ'' . The nanometric dimensions and the homogeneous and perfectly defined thickness of the silicon quantum well integrated into the MOS structure result in minimal dielectric losses. Previous work has also highlighted that this structural perfection contributes significantly to the reduction of dielectric losses, which is consistent with our observations [26, 27, 41].

The variations of tangential losses ($\tan \delta$) as a function of bias voltage and as function of frequency for the MOS_Si QW under are shown respectively in Fig. 8a, b. The evolution of $\tan \delta$ reveals a correlation between the movement of the charge carriers and both the frequency and the applied polarization. For a positive bias $V_B > 5\text{ V}$, the quantum well

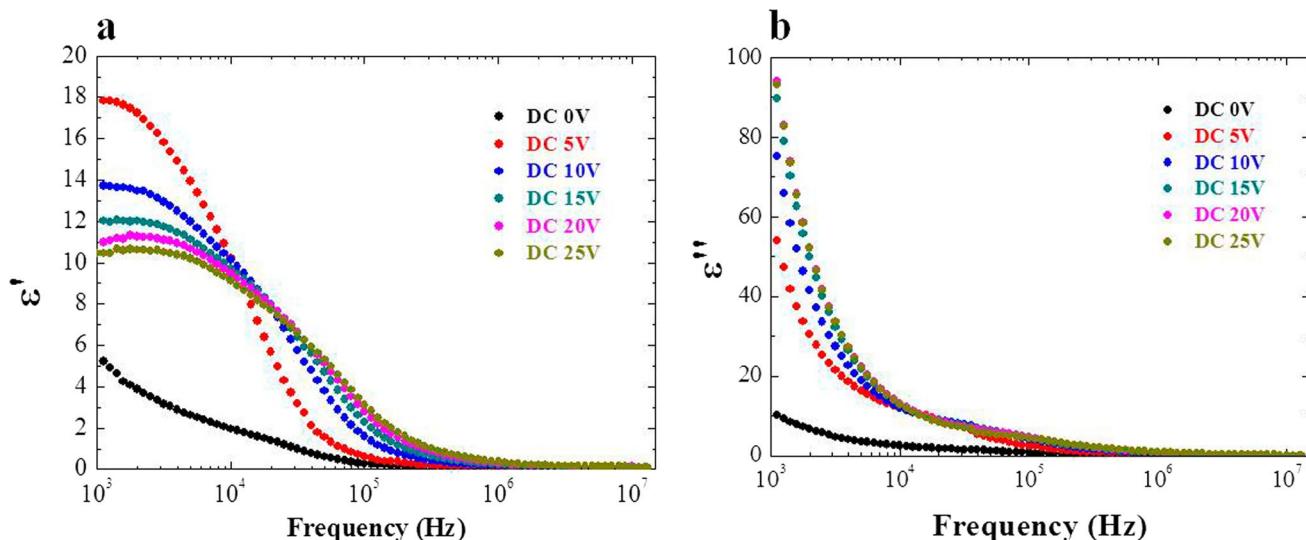


Fig. 8 a, b Illustrate the variation of the real component (ϵ') and the imaginary component (ϵ'') of the permittivity of the MOS_Si QW structure versus frequency at various bias voltage

acquires a charge. When the frequency increases, the electrons inside the silicon quantum well change their trajectory, thereby reducing their interactions with the $\text{SiO}_2\text{-Si}$ QW interfaces. This modification reduces the polarization and, therefore, decreases the $\tan \delta$, a phenomenon that can be explained by the Maxwell–Wagner model. Our structure shares a certain similarity with this model because it incorporates a semiconductor quantum well (Si QW) within a dielectric (silicon oxide).

The high barriers formed by the Si oxide with the silicon quantum well oblige the electrons to reach the latter by the Fowler–Nordheim effect, leading to their accumulation in the quantum well and thus generating polarization. The increase in $\tan \delta$ with the polarization voltage corroborates this phenomenon. As this voltage increases, the number of charge carriers reaching the quantum well also increases, forming new electric dipoles.

Previous studies have also highlighted this charge accumulation in energized quantum wells, highlighting its impact on dielectric properties, which is consistent with our observations. These results highlight the crucial importance of bias voltage in modulating the behavior of charge carriers and polarization within the MOS_Si QW, which directly influences its dielectric characteristics at different frequencies (Fig. 9).

The electrical modulus is expressed by:

$$M^* = \frac{1}{\epsilon^*} = M' + iM''$$

with

$$M' = \frac{\epsilon'}{\epsilon'^2 + \epsilon''^2}$$

$$M'' = \frac{\epsilon''}{\epsilon'^2 + \epsilon''^2}$$

This electrical modulus has been widely studied in various contexts for dielectric materials and complex structures. For example, research by Jones et al. examined variations in electrical modulus in polymer nanocomposites, highlighting how charges trapped at interfaces impact dielectric properties. Likewise, in the field of microelectronic devices, the work of Smith et al. explored the electrical modulus behaviors in field-effect transistor structures, providing insights into the optimization of dielectric materials to improve device performance.

In the specific context of MOS_Si QW structures, the research of Chen et al. analyzed the variations of the electrical modulus as a function of frequency to understand the polarization mechanisms and dielectric losses in these systems. These studies highlighted the importance of the imaginary component of the electric modulus (M'') to evaluate the dielectric losses specific to these structures, thus providing valuable insights into the interactions between space charges and oscillating electric fields.

To sum up, studying the electrical modulus, which includes both real and imaginary parts, is one of the most important approaches to understanding the relaxation phenomena of space charges in various dielectric materials and complex structures, thus offering perspectives rich in applications in the field.

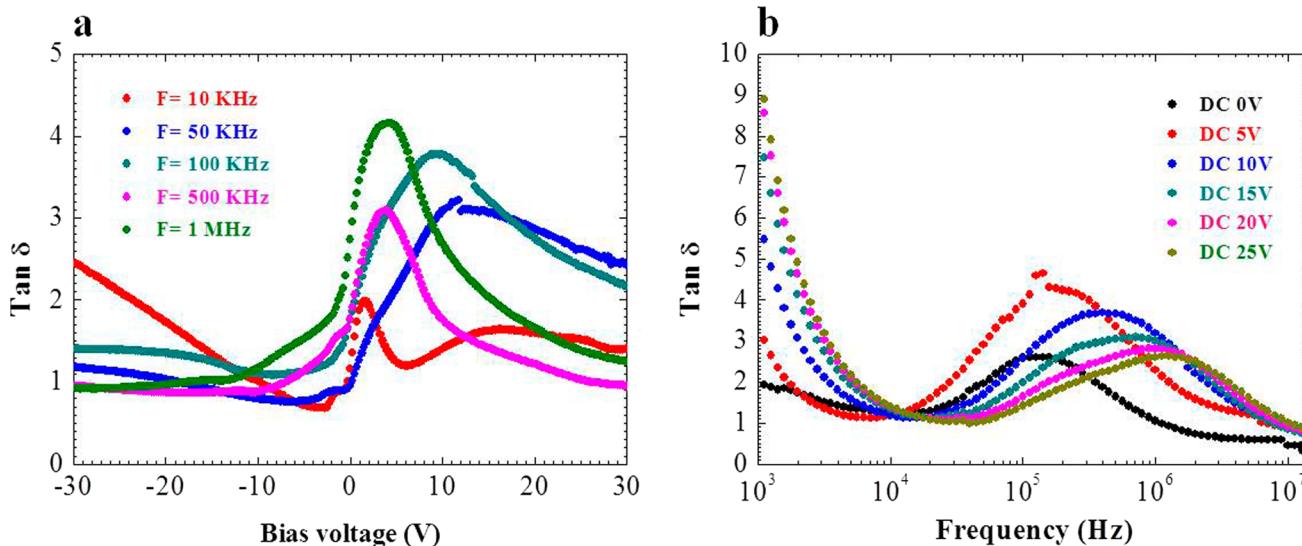


Fig. 9 **a, b** Present the variation of dielectric losses ($\tan \delta$) as a function of bias voltage and as a function of frequency for different bias voltages applied to the MOS_Si QW structure

Figure 10a) remarkably illustrates the variation of the real part (M') of the electrical module as a function of frequency for the MOS_Si QW structure under different positive bias voltages. This representation highlights abrupt increases in the value of M' at two distinct frequencies while showing a decrease with increasing applied voltage. This exciting evolution of M' suggests specific charge relaxation behaviors in the silicon quantum well in response to frequency and polarization.

When analyzing the permittivity components (ϵ' and ϵ''), a trend emerges: the decrease in ϵ with increasing frequency results in a corresponding increase in M . This correlation suggests that when the constant dielectric tends towards infinity, the electrical modulus M tends towards zero, especially at low frequencies. However, at high frequencies where the signal period is much shorter than the lifetime of the interface states (τ), these states fail to follow the excitation signal. Thus, the electrical module M reaches a maximum value, $M_{\infty} = 1/\epsilon_{\infty}$, linked to the Maxwell–Wagner relaxation process.

By observing the imaginary part of this electrical module, M'' , represented in Fig. 10b, we see a tendency to approach zero at the lowest frequencies, confirming the removal of electrical polarization. Compared to classical MOS structures without quantum wells, this underlines the significant impact of the 6 nm-thick silicon quantum well on the dielectric properties of the MIS structures. In particular, this quantum well occupies 25% of the volume of the insulating layer, which is crucial data that underlines the importance of its influence on electrical and dielectric properties. This observation is of particular importance in optoelectronic applications such as photodetectors and MOS-LED diodes.

We observe an impact of the polarization voltage on both components of the electric modulus, M' and M'' . This influence is corroborated by the measurements of these two components, presented in Fig. 11a, b, depicting their variations with respect to the polarization voltage.

Comparative studies with references from the literature on similar structures thus confirm the capital importance of this quantum well in the modulation of frequency responses and electrical and dielectric properties of MOS structures, thus highlighting the need to take into account its impact in the design and optimization of optoelectronic devices.

4 Conclusion

Through a novel approach based on the partial thermal oxidation of an ultra-thin silicon-on-insulator (UT-SOI) film, we have successfully fabricated and integrated a crystalline silicon quantum well within an MOS capacitor. Rigorous structural analysis using HR-TEM has verified the high crystalline quality of the formed quantum well, characterized by a uniform thickness and a flawlessly flat surface devoid of any crystalline defects.

Electrical measurements, employing capacitance–voltage and current–voltage analyses, demonstrate the normal operational behavior akin to a classic MOS capacitance, exhibiting distinct regimes of inversion, depletion, and accumulation. A comprehensive study of dielectric properties reveals insights into the structure's behavior, showing the evolution of key parameters such as dielectric constant (ϵ^*), electrical loss ($\tan \delta$), and electrical modulus (M^*) with varying bias voltage and frequency.

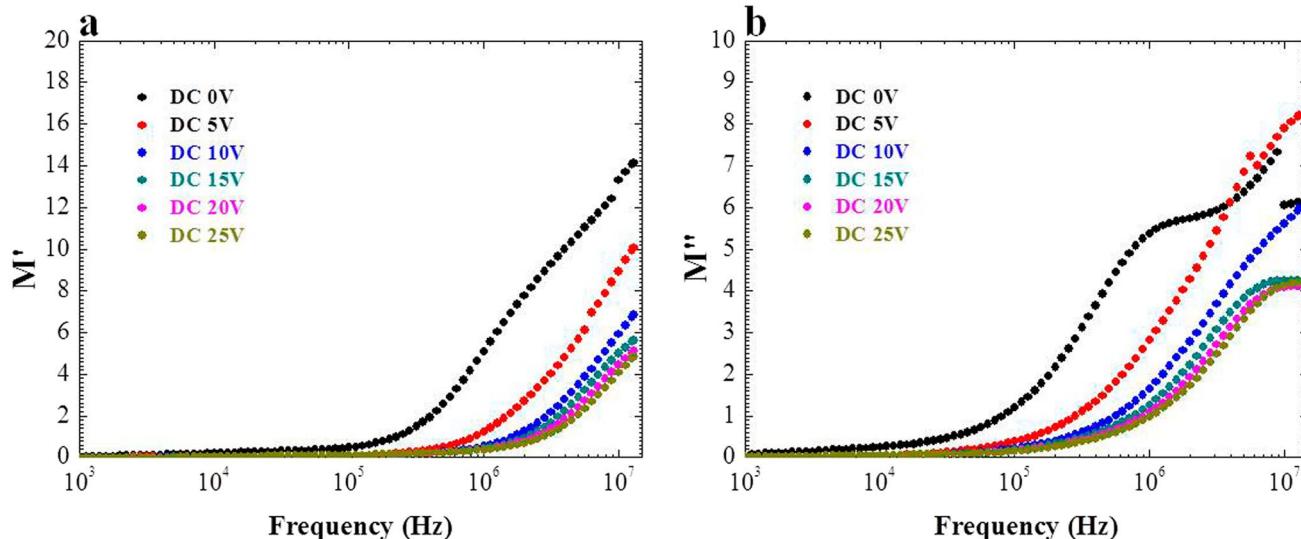


Fig. 10 a, b Respectively, show the variation of the real part and the imaginary part of the complex electrical module (M) as a function of the bias voltage for different frequencies

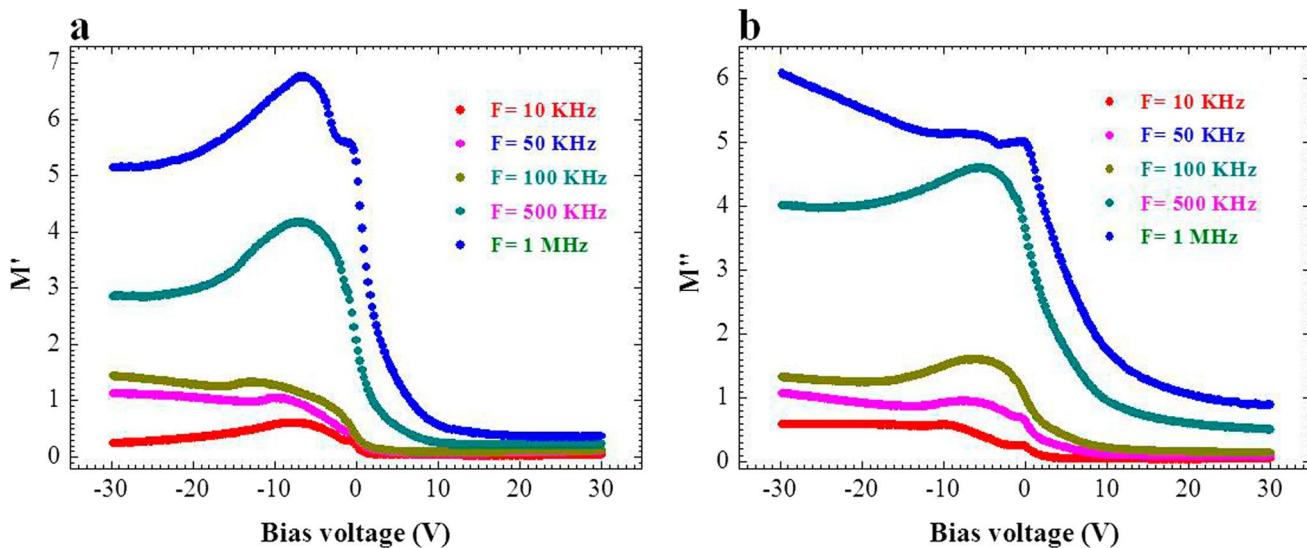


Fig. 11 **a, b** Respectively, show the variation of the real part and the imaginary part of the complex electrical module (M) as a function of the frequency for various bias voltages of the MOS_Si QW structure

The analysis of the obtained measurements reveals the structure's low density of states (Dit) and the presence of a Maxwell–Wagner-type dielectric relaxation. These compelling results underscore the efficacy of the proposed approach in the fabrication of silicon quantum wells, paving the way for the efficient integration of such nanostructures in applications like photodetection and energy harvesting, leveraging the unique properties of MOS structures. This research marks a significant advancement in the pursuit of high-performance electronic devices incorporating silicon nanostructures.

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Author contributions The authors confirm contribution to the paper as follows: study conception and design: M. A. Data collection: M. A.; I. G.; M. B. Analysis and interpretation of results: M. A.; Draft manuscript preparation: M. A. All authors reviewed the results and approved the final version of the manuscript.

Data availability Data can be obtained upon request from Prof. Dr. Mansour Aouassa.

Data availability All data that support the findings of this study are included within the article (and any supplementary files).

Declarations

Conflict of interest The authors declare that they have no competing interests.

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