Received: 22 March 2018 | Revised: 18 May 2018 | Accepted: 13 June 2018

DOI: 10.1002/pip.3062

BROADER PERSPECTIVES

WILEY PROGRESS IN PHOTOVOLTAICS

Challenges facing copper-plated metallisation for silicon photovoltaics: Insights from integrated circuit technology development

Alison Lennon[1] | Jack Colwell[1] | Kenneth P. Rodbell[2]

[1] School of Photovoltaic and Renewable Energy Engineering, UNSW, Sydney, NSW 2052, Australia

[2] IBM Thomas J. Watson Research Centre, Yorktown Heights, New York, USA

Correspondence
Alison Lennon, School of Photovoltaic and Renewable Energy Engineering, UNSW, Sydney, NSW 2052, Australia.
Email: a.lennon@unsw.edu.au

Funding information
Australian Renewable Energy Agency, Grant/Award Number: RND 2014/RND002; Australian Research Council, Grant/Award Numbers: FT170100447 and LP100100712

Abstract

Copper-plated interconnects were widely adopted for volume manufacture of integrated circuits after more than a decade of intensive research to demonstrate that use of Cu would not impact device reliability. However, although Cu-plated metallisation promises significantly reduced costs for Si photovoltaics, its adoption in manufacturing has not gained the same traction. This review identifies some key challenges facing the introduction of Cu-plated metallisation for Si photovoltaics. These include the following: (1) increased carrier recombination due to the use of Cu for metal contact formation; (2) reduced module reliability due to adhesion or contact integrity failures; and (3) limited availability of cost-effective processes and equipment for metal plating. For integrated circuits, Cu's low electrical resistance and high resistance to electromigration provided an impetus for the large investment in process development that was required to realise Cu-plated interconnects. However, the technical advantages of using Cu for Si solar cell contacts are not as compelling, as solar cells can tolerate larger feature sizes thus reducing the criticality of the contact metal's conductivity and electromigration properties. Additionally, for Si photovoltaics, low cost is paramount, and new challenges arise from the need for modules to absorb light and operate in the field for 25+ years in diverse outdoor climates. However, with the scale of Si photovoltaic manufacturing expected to increase dramatically in the next decade, the use of large quantities of silver for cell metallisation will provide an incentive to address reliability concerns regarding the use of Cu for Si photovoltaic metallisation.

1 | INTRODUCTION

Today, at least 90% of all Si solar cells that are produced commercially have electrodes formed using screen-printed Ag.[1] As photovoltaic (PV) module costs decrease, the use of Ag is increasingly under scrutiny as a way in which further cost reductions can be achieved. Silver remains the costliest non-Si component in the crystalline Si PV value chain, with Ag pastes contributing 1 US$ cent/Wp per 20.0% efficient 156-mm cell,* or 13% of the non-Si cell price in early 2018.[1] Currently, Ag is ~ 80 times the cost of Cu on a per weight basis, and so for a PV manufacturer producing 5 to 10 GW annually, the potential financial advantage of using Cu rather than Ag for cell metallisation based on materials alone is substantial. However, the actual advantage depends on: (1) the cost of equipment and processes required for Cu-plated metallisation; (2) achievement of similar or increased module efficiencies compared with what can be achieved with screen-printed Ag cell metallisation; and (3) the comparative durability of Cu-plated modules. Many reports have highlighted the potential cost benefits of transitioning to Cu-plated metallisation for industrial p-type Si solar cells,[2-7] with cost reductions ranging from 0.0125 to 0.18 US$/Wp having being quoted for one-sided Cu metallisation,[7,8] and costs as

*Note this value does not include the cost of screen replacement and other costs associated with screen printing (eg, depreciation, labour).

low as US$0.28/Wp being suggested for Ni/Cu/Ag plated bifacial modules.[9] Potential efficiency and yield gains for Cu-plated cells over screen-printed cells have also been frequently suggested. These gains include reduced front surface shading and the electrical contacting of more lightly doped emitters.[2-6,10,11] Self-alignment of Cu-plated contacts may also be advantageous for more complex cell structures.[9,12] However, so far, moves to replace Ag cell metallisation with plated Cu have failed to find traction, with several attempts to introduce plated Cu into PV manufacturing stalling due to concerns about either reliability or the plating process not being as cost-effective as the incumbent screen-printed Ag cell metallisation process, despite the significantly cheaper raw material costs.

This situation may be considered surprising because electroplated Cu has been used extensively in the fabrication of interconnects for integrated circuits (ICs). Initial reports of the use of electroplated Cu conductors for electronic circuits date back to early patents filed by Hanson (1903)[13] and Ducas (1925).[14] Then, in 1997, IBM introduced the use of Cu for interconnects in their very large scale integrated (VLSI) technology.[15-21] Many in the IC industry did not believe in Cu's promise due to the challenges in how it was deposited and patterned and the difficulty of finding a suitable barrier material to prevent the Cu from diffusing into the Si where it could contaminate and 'poison' the device.[19] However, a dedicated cross-disciplinary team of researchers working in partnership with Motorola were able to realise the promise of Cu interconnects which can conduct electricity with approximately 40% less resistance than Al wires, leading to a 15% increase in processor speed.[15,18,20] A further advantage of using Cu for interconnects was its higher resistance than Al to electromigration. Electroplated Cu interconnections using the dual damascene Cu plating process[22-25] entered high-volume manufacturing in 1998 at IBM, with the initial chip technology combining up to six levels of electroplated Cu circuitry.[19] Relatively quickly, Cu-plated interconnects proceeded to become the default standard technology used worldwide for ICs and are now in their tenth generation of manufacturing.[26]

Figure 1A shows a cross section of a 2015 state-of-the-art microprocessor unit fabricated using the Cu dual damascene process to form interconnects between the different metal layers of the device, and Figure 1B shows a cross section through a 14-nm technology Intel IC with 13 layers of metal. Tungsten has been routinely used in the lower levels of Cu interconnects due to its greater resistance to electromigration than Cu (it also acts to place an additional barrier between the Cu and Si); however, in recent years, as the dimensions of the lower levels of interconnects reduce with 7 and 10-nm IC technology, parasitic capacitances increase and IC manufacturers are investigating the replacement of W with Co due to both its less granular structure and hence lower resistance and RC effects.[27]

The dual damascene Cu plating technology has evolved to also meet the challenges of through-Si-vias (TSVs) to enable the fabrication of 3D ICs.[28-34] Unlike VLSI circuits where the electroplated Cu was used to connect metal layers on different planes of the device, in 3D ICs the Cu TSVs extend through Si wafers and provide a conductive path between layers of the ICs. This allows stacking of chips in 3D structures that are more compact and have a reduced footprint on a circuit board. Greater levels of integration require that the diameters of the TSVs are reduced to minimise stress and Cu protrusion from the surface of vias (also called 'pumping').[35,36] Resistance to electromigration can also be improved by moving to narrower TSVs as smaller stress gradients result.[37] These drivers have resulted in the development of technology to achieve Cu-plated TSVs with diameters of <1 μm and aspect ratios exceeding 15,[38] although typical TSV diameters for global interconnects are more likely to be in the range of 2 to 4 μm between 2015 and 2018 with aspect ratios of 12 to 15.[26]

From the technology pathway traced for Cu-plated metallisation for Si PV,[39] we see quite a different story. Although the first Si solar cells were plated and several attempts have been made to

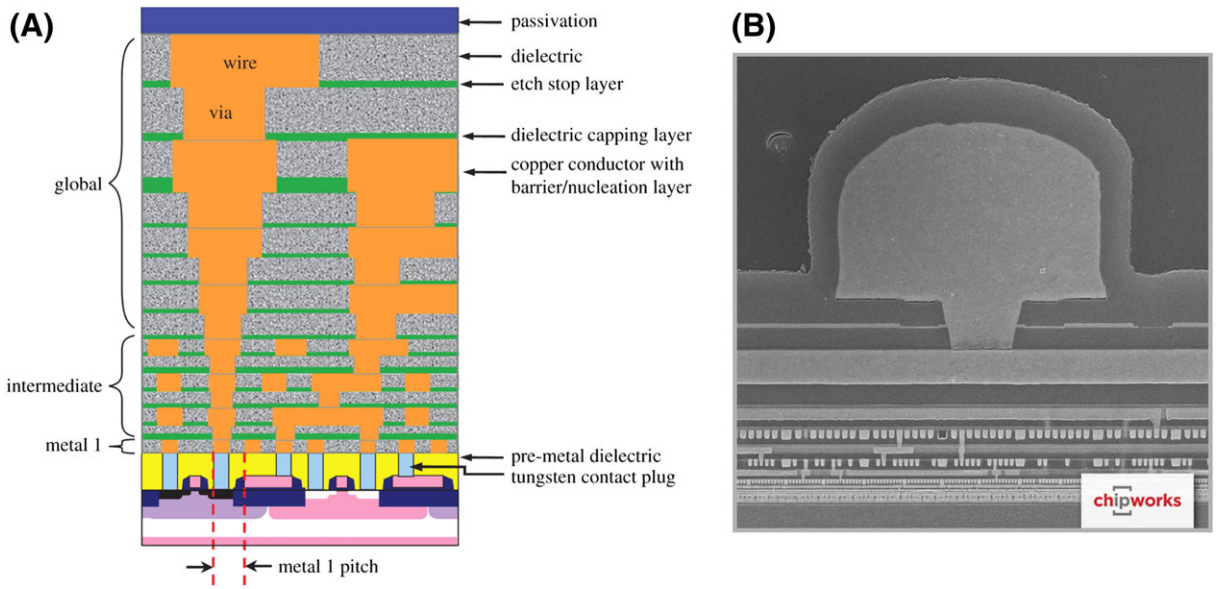

FIGURE 1 A, Diagram of a cross section of a VLSI circuit for a microprocessor fabricated using the double damascene Cu plating process, showing interconnections from individual transistors to form global circuit wiring (adapted from the 2015 International Technology Roadmap for Semiconductors 2.0: Interconnects[26]). B, Cross section through an IC fabricated using Intel's 14-nm technology with 14 layers of metal (image provided courtesy of TechInsights, www.techinsights.com) [Colour figure can be viewed at wileyonlinelibrary.com]

re-introduce plating in manufacturing,[40-47] Cu plating has failed to gain the same market share and momentum that it achieved in ICs. One exception to this observation is the successful use of Cu plating in the metallisation of back contact cells by SunPower[47]; however, the market share of back-contacted cell technology remained limited to less than 5% in 2017[1] due to the higher cost of manufacturing back contacted cells. The question is: why have the PV and IC technology pathways for Cu plating been so different?

The technical challenges of integrating Cu-plated metallisation in Si PV modules can be perceived in some ways as being less demanding than its integration into high performance ICs. Firstly, Si PV modules do not require the high aspect ratio metallisation and narrow vias for high performance. Providing that current can be extracted from the solar cell with sufficiently low series resistance, there may be limited benefit in metal fingers on cells being much narrower than 20 μm, which is much wider than the via diameters of <5 μm required for IC metal interconnects. This means that metal conductors on solar cells are less susceptible to electromigration failures. Secondly, because Ni can be electrochemically deposited directly on Si,[40,48,49] it is not necessary to deposit surface seed layers for electroplating using higher-cost vacuum processes. Finally, because solar cells can provide a source of current when illuminated, they can provide their own source of electrons for electrodeposition.[39,50-52] This additional functionality, which is specific to solar cells, can reduce the complexity of the electrochemical deposition process for the Si PV application.

However, set against these potential advantages is the need for PV modules to have a long field life. Unlike most IC devices, PV modules are expected to last 25+ years in the field, with even longer field lifetimes being proposed as a means of reducing the levelised cost of electricity (LCOE) provided by PV.[53] Most Si PV manufacturers make no assumptions of where a module is installed and so stability to both high (up to 85°C) and low (−40°C) temperatures and very wet/dry conditions is required. Process uniformity across wide areas is also necessary to ensure that, when cells are connected in series in a module, the current is not limited by cells or cell regions of lower performance. These additional requirements can introduce new challenges for Cu-plated Si solar cells.

This review aims to identify some key challenges for Cu plating for PV and to explore how these challenges could be addressed using insights from the IC industry. In particular, it attempts to address the issues of: (1) increased carrier recombination due to either the penetration of plated Cu into the Si device and/or from metal being directly in contact with the Si; (2) reduced module reliability due to adhesion or contact integrity failures; and (3) limited availability of cost-effective processes and equipment. Although a focus is placed on the current mainstream industrial p-type Si PV technology where metal contacts are formed directly on P-diffused Si regions of solar cells, many discussion points also remain relevant to cell designs where metal contacts are formed on n-type cells, passivated contact surfaces, and/or on the rear surfaces of back contact cells.

2 | CHALLENGES FOR COPPER-PLATED SILICON SOLAR CELLS

BP Solar successfully manufactured their Cu-plated Si laser buried grid (LBG) Saturn modules (see Figure 2) until 2009.[41,42,44,45] These modules have achieved performance ratios (PR) exceeding 70% after 20 years in the field in Spain, values which are consistently higher than that of comparative screen-printed modules that were manufactured at the same time and installed at the same location.[54] Although this result suggests that the use of Cu metallisation does not seriously impact device performance, the Saturn modules in the Toledo study had an efficiency of ~14% and so would not have been highly sensitive to the presence of metal impurities in the Si wafer.

Since the Toledo modules were manufactured, Si PV module efficiencies have increased considerably through the use of a rear passivation layer with localised contacts. This passivated emitter and rear cell (PERC) design, which was first reported by Blakers et al,[55] is now being manufactured in increasing volumes in China.[56,57] The reduced recombination current density in these cells makes them more sensitive to impurities in the Si such as B-O defects and metal impurities. For this reason, any metal that is introduced into the Si during the metallisation process would be expected to have a greater relative impact on module efficiency than it would on a less efficient module. Additionally, the achievement of higher energy conversion efficiencies in PERC cells has required the carrier collecting regions of the cells to be more lightly-doped. This may have implications for the ability of the P-doped emitters of cells to getter metal impurities that are either present in the wafer or enter the wafer during cell processing. Consequently, it may be prudent to re-visit the possibility that Cu (from plated metallisation) may diffuse into the Si in modules in the field and cause additional recombination in the event that diffusion barrier layers are insufficient. It may also be wise to reconsider the

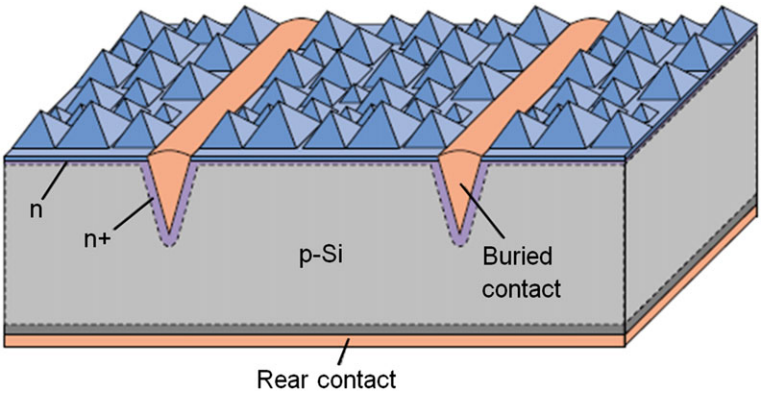

FIGURE 2 Cross-sectional schematic of BP Solar's LBG solar cell showing the Cu-plated fingers contained within heavily doped laser trenches (from Bruton et al[41]) [Colour figure can be viewed at wileyonlinelibrary.com]

contribution of contact recombination to device performance, as this is expected to increase with the reduced emitter dopant concentrations that are now being used to achieve higher energy conversion efficiencies. Section 2.1 discusses in more depth these metallisation-induced recombination losses.

Although BP Solar's LBG cells were able to be interconnected by soldering, this achievement was not possible with Suntech's laser-doped Pluto cells, for which light-induced plating (LIP) was used to form the front metal grid instead of electroless plating.[58-60] This meant that alternative interconnection methods were required which resulted in a more complex and expensive manufacturing process. The observed poor adhesion of plated metal contacts to laser-doped surfaces introduced a new challenge for the adoption of Cu plating. Not only did the poor adhesion limit options for cell interconnection, it raised concerns about reduced durability due to insufficient finger adhesion, something which had not previously been considered a problem due to the smaller wafer sizes used earlier in the history of Si PV and BP Solar's use of grooves to contain the metal. Reduced durability directly impacts the LCOE, a direction that is clearly undesirable. Module lifetime may also be impacted by metal contact degradation or corrosion. In the past, module manufacturers have relied on certification to provide justification for reliability; however, as discussed in Section 2.2, the International Electrotechnical Commission (IEC) standard tests are highly accelerated tests that have been designed to identify design flaws that have led to early failures (primarily for screen-printed modules) and do not necessarily provide a measure or indicator of reliability. Reliability requires an understanding of how materials age in a module. Due to the difficulty of identifying the underlying physical reasons for module failure, Si PV module aging has not been comprehensively investigated. Section 2.2 discusses reliability issues relating to plated contact adhesion and metal contact degradation and, in doing so, raises the further challenge of providing appropriate metrology tools and type tests for module qualification to ensure that a plated metallisation process can be reliably monitored in large-scale commercial production.

Then, in Section 2.3, we provide a discussion on whether the required plating processes and equipment for reliable plated PV metallisation are available and can be cost-effective. As with the introduction of Cu plated interconnects to the VLSI industry, additional processes are required to provide adequate diffusion barriers and to integrate the patterning of the metal conductors. For the IC industry, the technological advantages of using Cu for interconnects in place of Al clearly outweighed the cost required for the additional processes, and so the transition from Al to Cu interconnects proceeded relatively quickly. For Si PV, in spite of many reports highlighting the potential cost benefits of Cu-plated metallisation,[2-6,9,61] the economic advantages appear to be less convincing for Si PV manufacturing companies, most likely due to insufficient knowledge of the actual costs involved. For PV manufacturers to transition from screen-printed Ag to plated Cu, they will need equipment that can pattern the cells' antireflection coating (ARC) and plate cells (with diffusion barriers and capping layers) at a sufficient throughput to be competitive with a screen-printed metallisation process. If the cost of providing these additional processes and equipment is high, then the cost benefits of using the cheaper Cu metal in manufacturing may be eroded.

2.1 | Metallisation-induced recombination

For a Cu-plated metallisation process to be commercially viable, plated cells will need to achieve similar or superior efficiencies to comparative screen-printed cells. Many reports have highlighted the potential of Cu-plated cells to out-perform screen-printed cells,[2-6,10,11] due to their narrower fingers resulting in reduced shading and the ability of Ni to form ohmic contact to Si surfaces with P concentrations as low as 4×10^{19} cm^{-3} [10] and potentially even lower.[62,63] However, these attributes only provide an advantage if other sources of loss are not introduced during the metallisation process. This section therefore considers the possibility of recombination that may be introduced in the wafer, or at the surface, by a Cu-plated metallisation process.

Copper-plated metallisation processes can introduce additional recombination through either: (1) plated metal (Ni and/or Cu) penetrating into the Si wafer where it forms recombination-active sites in the emitter or base of the solar cell (bulk recombination); and/or (2) contacting Si surfaces having low dopant concentrations (ie, contact recombination). Quantifying the impact of the first source of recombination requires an understanding of the ability of diffusion barriers to prevent ingress of the Ni and/or Cu into the cell and how the introduced metal causes additional recombination in the absorber and emitter regions of cells. Quantification of the second source requires accurate measurements of metal-Si contact recombination.

Section 2.1.1 reviews the implications of Cu penetrating into Si devices where it can introduce additional recombination in p-type Si, n-type Si, and in devices containing p-n junctions. It then considers the possible pathways by which plated Cu may enter the Si device and the effectiveness of barriers that have been used by both the IC and Si PV industry to prevent Cu ingress. Finally, in Section 2.1.2, the impact of the metal/Si interface on device performance is examined. Although this source of efficiency loss can be quantified using first principles by assuming a metal contact fraction area-normalised surface recombination velocity (SRV),[64-66] the possibility that some metallisation schemes may actually effectively increase the physical metal-Si contact area from its projected area, due to the way the contact is formed, will be considered.

2.1.1 | Bulk recombination

One of the concerns raised about using Cu to form the metal electrodes to Si solar cells is that the Cu may penetrate into the Si where it can form deep-level traps that are detrimental to cell performance.[67-70] The introduction of Cu interconnects into ICs also faced that concern.[19] Copper is a fast-diffusing element in Si,[67] where it has an intrinsic diffusion length on the order of 1 mm after 3 hours at room temperature.[68] It tends to diffuse towards extended defects (eg, dislocations) and surfaces where it precipitates.[71] However, especially for n-type Si, if the Cu concentration is sufficiently high and cooling is rapid, then it can also precipitate in the bulk forming platelet-like defects presumably comprising Cu silicide (Cu_3Si), mainly on {111} crystal planes. These defects are believed to introduce a band-like state in the upper half of the Si bandgap.[71,72]

Copper-induced defects in Si and Si solar cells

Copper contamination can reduce the minority carrier lifetime in p-type Si[67,68,73,74] and n-type Si[73,75] with the impact on carrier lifetime being more significant in n-type.[70,73,76] The effect of Cu impurities on the carrier lifetime in Si and attribution of the associated recombination to energy levels within the Si bandgap has been widely reported over the years. Copper can exist in interstitial (Cu_i) forms, substitutional (Cu_s) forms, in complexes with Si (eg, Cu_3Si), other Cu atoms (Cu_sCu_{3i}) and other Cu impurities including hydrogen (eg, Cu_s-H_i) (see Figure 3).[70,77] The Cu_i state does not induce any defect levels in the gap and is stable only in the singly positive charge state (Cu_i^+) for all Fermi-level positions in the Si band gap.

The Cu complexes with Si, Cu_3Si, are commonly referred to as precipitates and cause severe recombination because they form a deep defect band in Si (see Figure 3).[72,77-82] At room temperature, Cu_3Si precipitates will only form and grow when the Fermi level exceeds the Cu_3Si neutrality level of E_C – 0.2 eV, at which point Cu_3S changes its charge state from being positive to neutral or negative and therefore attracts Cu_i^+ for further precipitate growth. Below E_C – 0.2 eV, the Cu_3Si defects are positively-charged and hence repel the Cu_i^+.[77,83] In n-type Si, the Fermi level exceeds E_C − 0.2 eV at P dopant concentrations > 1.7×10^{16} cm^{-3}, and at these doping levels, Cu precipitation occurs at 300 K regardless of the Cu concentration in the Si. In p-type Si, Cu_3Si has been shown to reach the neutrality level, only when the Cu concentration exceeds the acceptor density by 1×10^{16} cm^{-3}.[71] Consequently, n-type Si is more sensitive to Cu contamination than p-type Si due to the ease at which Cu precipitates can grow[76] and, in p-type Si, the more benign Cu_s-Cu_{3i} complex predominantly forms (see Figure 3).[70,77]

Fast quenching from high temperatures leads to high supersaturation and the consequent formation of homogeneously distributed small Cu precipitates. If the Cu concentration is >10^{17} cm^{-3}, then larger platelet-like precipitates (in the order of 30-500 nm) can form mostly in the {111} crystal plane.[71,72,77] The large lattice mismatch between Cu_3Si and Si results in the precipitates being decorated by an extensive extrinsic dislocation network.[77,82,84] Slower cooling typically leads to the formation of precipitate colonies, referred to as a "haze", which are distributed near the surface of defect-free Si.[72,77,80]

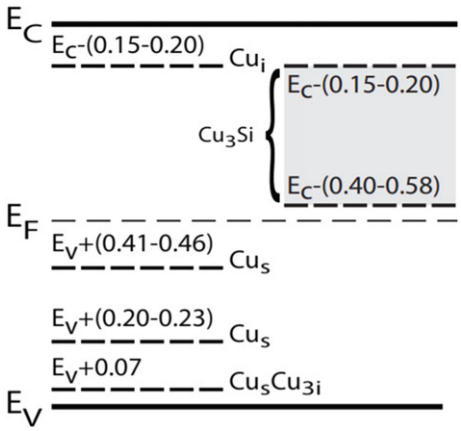

FIGURE 3 Defect energy levels in the Si bandgap associated with Cui, Cus, the Cu complexes CusCu3i, and Cu3Si (from Lindroos[77]). Note the trap states are listed as E_C – from the conduction band and E_V+ from the valence band (in eV)

Copper contamination in Si devices with a p-n junction has been shown to lead to an increase in leakage current.[85-90] Istratov et al suggested that the leakage current at p-n junctions increases through the formation of Cu precipitates in the junction area, most likely starting from the n-type side of the junction, where Cu complex formation is favoured.[90] Miyazaki et al confirmed this theory using secondary-ion mass spectrometry (SIMS) and transmission electron microscope (TEM) imaging, by showing that Cu precipitates that formed in the n^+ region of p-n junctions, can cause large dislocations in the n+ region as the precipitates extend into that region from the junction. Interestingly, they also observed Ni precipitates in the n^+ region, but these appeared to form without concomitant dislocation formation and did not result in an increase in the leakage current.[91]

Early studies suggested that Cu concentrations of up to 10^{16} cm^{-3} in the original wafer did not significantly impact efficiency for p-type or n-type solar cells.[88,89] However, with higher Cu concentrations, solar cell efficiency was observed to reduce due to increased junction recombination.[85,88,89] A high tolerance to Cu may have been observed in these early experiments due to the gettering of Cu (initially in the wafer) by the diffusion glasses.[92] It is also expected that the cell efficiency in these earlier reports was limited by the surfaces and therefore not highly sensitive to bulk recombination. However, a more recent cell study by Coletti et al using Cu-contaminated ingots found that Cu could increase recombination in both the emitter and bulk when its concentration exceeded 1.75×10^{17} cm^{-3} (8 ppmw), which is lower than for Fe (11 ppm) but higher than that required for other impurities such as Cr and Ti (0.11 ppm).[82]

The early studies also appear not to have considered the impact of illumination on increased recombination due to metal impurities. Reports of light-induced degradation (LID) due to the B-O defects[93,94] raised the importance of this problem with numerous subsequent reports seeking to elucidate the mechanisms of the B-O complex formation[95-100] and deactivation through thermal treatments under carrier injection conditions.[101-107] The ability to mitigate the effects of the light-induced (also referred to as carrier-induced) B-O defect became more critical with the projected greater market share of commercially-produced PERC cells,[55-57,108] as these more efficient cells are more sensitive to bulk recombination. Light-induced degradation due to B-O complexes also raised questions about the role of carrier concentration in altering the recombination properties of other impurity-related complexes and, in doing so, has re-energised investigations into the contribution of metal impurities to recombination in Si solar cells.

Under illumination, the effective minority carrier lifetime in p-type wafers that have been intentionally-doped with Cu has been shown to degrade due to the formation of Cu precipitates in the p-type Si.[109-116] Enhanced precipitation can occur due to the repulsion between the positively-charged Cu_i^+ and existing Cu precipitates decreasing with increased electrical carrier concentration.[117,118] Inglese et al identified that the light-induced Cu defect in float-zone p-type Si (with minimal oxygen precipitates) occurred within a range of mid-gap energies E_c - E_t = 0.48 to 0.62 eV with donor-like capture cross-section asymmetry (k = 1.7 – 2.6).[114] The relatively large range of energy levels identified was most likely due to the different sized precipitates in the sample. The proposed precipitation process was

modelled by Vahlman et al using classical nucleation theory with precipitates growing or dissolving one atom at a time.[116] Light-induced degradation of p-type wafers due to Cu was shown to be more extensive in Czochralski (Cz) than float-zone Si, and so Lindroos et al suggested that oxygen and its related defects may provide nucleation sites for Cu precipitates.[113] Additionally the presence of B, rather than the p-type dopant Ga, appeared also to promote LID.[113]

Light-induced degradation due to Cu impurities has been reported in p-type PERC cells,[119,120] with the extent of the performance loss being greater for cells fabricated using multi-crystalline Si wafers.[121] Copper precipitates have been detected in multi-crystalline PERC cells for which up to 15% relative efficiency loss was observed after illumination.[120,121] The kinetics of the observed efficiency loss were not consistent with models reported for B-O and Fe-B lifetime degradation, adding further credence to the theory that carrier injection could enhance recombination at metal-containing complexes as well as B-O complexes. It is possible that Cu, either present in the ingot feedstock or introduced through the wire sawing process,[122,123] may not be completely gettered to the surface during P diffusion processes, and when cells are exposed to high concentrations of carriers, any Cu remaining in the cell can form precipitates at grain boundaries or crystal defects which can decrease carrier lifetimes.[120] Luka et al also demonstrated, through microstructural imaging, that Cu can be gettered to defects in amorphous rear dielectric passivation layers.[120] This highlights the possibility that any Cu remaining in the fabricated cells may continue to precipitate at grain boundaries, dislocations, and defects in dielectric layers in the presence of high concentrations of carriers. They also raised the possibility that the full-area Al BSF may have provided an important role in gettering any remaining Cu to the rear electrode in earlier Si solar cells.

These wafer-based and cell-based reports suggest that if Cu remains in fabricated p-type solar cells, operation in the field can result in the Cu precipitating at a range of defects both within the bulk and at the surface of encapsulated cells. Although this risk is expected to be greater for multi-crystalline cells due to their higher concentrations of impurities, it remains finite also for cells fabricated from mono-crystalline wafers where Cu may be introduced through either the wire sawing process or metallisation.[122,123] If Cu is introduced through ingot contamination or wire-sawing, there is an opportunity for the Cu to be gettered by the P diffusion step. However, if Cu is introduced during the metallisation process, it does not experience a high temperature diffusion process and consequently is unlikely to be gettered. Furthermore, the plating process is most commonly performed after the firing of the rear surface Al in Al BSF and PERC cells, the latter process having been reported to introduce O-containing precipitates,[124-126] which may provide a site for heterogeneous nucleation. This suggests that, in the absence of any effective gettering steps post-plating, minimising the potential of Cu ingress from Cu contacts is critical especially for PERC cells due to their increased sensitivity to bulk recombination.

One key advantage that IC devices with Cu interconnects have over Cu-plated Si solar cells is that they are not typically exposed to illumination and so LID is not expected to be a problem. Additionally, because CMOS elements are formed on Si surfaces, any Cu introduced from either the Si feedstock or wafer sawing can be removed from the active areas of the device by gettering steps using intentionally-formed O precipitates in the centre of the wafer prior to device fabrication.[33,127-129] The higher $ value per unit area of device also means that ICs have typically not used the lower-cost multi-crystalline Si wafers and so the Si material of the device contains less crystal defects, grain boundaries, and intrinsic metal impurities where Cu precipitation can be nucleated. All in all, this suggests that Cu contamination of Si may represent a more significant problem for solar cells than ICs due to the solar cell utilising the entire Si wafer and the requirement for Si PV modules to operate in a wide range of environments under illumination. These operating requirements can increase the potential for Cu-related complexes to form and introduce recombination during a module's operating lifetime.

However, balanced against these concerns of bulk wafer contamination, contamination of Si surfaces may be more critical for IC devices. For Si solar cells with reasonably heavily-doped emitters, the impact of any Cu gettered to the Si surface may be relatively minor; however, the surfaces are critical for CMOS components. This may explain why the IC industry focussed so much attention on the development of: (1) highly effective diffusion barriers; and (2) alternative metals (eg, W and Co) for the lower level interconnects, to prevent the Cu from penetrating into both the adjacent dielectric and the Si of the device.

Copper ingress into silicon through diffusion barriers

The general strategy that both the IC and Si PV industries have adopted to protect devices from the impact (s) of Cu ingress from metallisation is to use diffusion barriers. It is well understood that placement of chemically different atoms in close proximity leads to atomic migration to lower overall free energy. This migration can be driven by the presence of concentration differences, existence of a negative free energy of reaction, application of an electric field, availability of thermal energy, generation of a strain gradient, or a combination of some or all of these factors.[130] An ideal barrier for a metal contact to a semiconductor is electronically transparent and atomically opaque.[131] Electronic transparency requires a low bulk resistivity and a low contact resistance. In addition, a passive (non-reacting) barrier must be thermodynamically stable with its adjacent materials.[131]

Diffusion barrier failure may occur as a result of: (1) diffusion of the metal or the substrate through defects in the barrier materials; (2) diffusion of metal along grain boundaries in the barrier material; and (3) loss of integrity of the barrier materials due to a metallurgical or chemical reaction with the metal and/or substrate.[130] These barrier failure mechanisms suggest that microstructure plays a critical role in the diffusion barrier performance of a material. Most thin films contain many defects, and so it can be very difficult to fabricate highly effective passive (non-reacting) barrier layers. Consequently, other approaches, such as stuffed or sacrificial layers, have also been investigated as practical diffusion layers.[132] In the discussion below, the requirements for passive or non-reacting barriers are first considered as this is the approach that has typically been adopted for Cu diffusion barriers in IC device fabrication. However, the possibility that the Ni/Cu metallisation scheme used by Si PV devices could act as an effective sacrificial barrier after sintering to form a Ni silicide is also considered later in the discussion.

Thin film microstructures (see Figure 4) can be categorized as single crystal, polycrystalline, nanocrystalline (ie, polycrystalline with grain size below < 5 nm) and amorphous (no long-range ionic periodicity). The arrangement and number of grain boundary pathways in these different microstructures can play a large role in the rate of Cu penetration. In addition to providing an effective barrier to Cu, the layer should ideally also adhere strongly to the surface so that an additional adhesion layer is not required.

The Cu diffusion barrier materials employed for ICs typically include metallic refractory alloys due to their high melting points, chemical inertness, high thermal stability and high conductivity.[133-135] This ensures minimal inter-diffusion during thermal processes involved in device fabrication. Of this class of materials W-, Ta-, and Ti-based binary and ternary compounds (eg, TiN, WN, ZrN, TaN, and TiZrN) have been most studied owing to their desirable physical, chemical, and electrical properties, although the performance of Ti-based alloys can be impacted by Ti's metallurgical reactivity with Cu at temperatures of ~350°C. In general, elemental materials are poor diffusion barriers unless they are single crystalline.[136]

The microstructure of films can depend on how films are deposited.[137] Many binary alloy films deposited by physical vapour deposition (PVD) have a columnar polycrystalline structure which is generally undesirable for a barrier layer due to Cu's propensity to diffuse rapidly along grain boundaries.[138,139] For these types of films, there are two generally accepted ways of reducing the diffusion paths for Cu: (1) increasing the grain size; or (2) 'stuffing' the grain boundaries with light elements like O, N, and C.[140-142] The former can be achieved through annealing after deposition and the latter can be achieved by changing the temperature and/or gas mixture during deposition. These two approaches can be further developed to achieve crystalline barriers (for (1)) and nano-crystalline or amorphous films (for (2)), each of which typically has more effective barrier properties than the original columnar polycrystalline films.[143] In general, barrier performance improves with the microstructure trend shown in Figure 5.[130,140]

Amorphous ternary alloys, consisting of one or two non-metal components, have been extensively used as barrier materials for Cu in the IC industry due to their high crystallisation temperatures and stability.[137,144] The addition of non-metal elements (eg, Si or N) to a binary metal alloy can result in a grain-free amorphous barrier material which does not crystallise until subjected to very high temperatures (eg, in excess of 800°C). Although placing Cu in contact with the deposited barrier materials can reduce the crystallisation temperature, in general, sufficiently high crystallisation temperatures can be achieved with ternary alloys of Ta, Si, and N (eg, $Ta_{36}Si_{14}N_{50}$[137]).

Another requirement of diffusion barriers for ICs is to provide a seed surface that can allow for uniform nucleation of plated Cu. Most

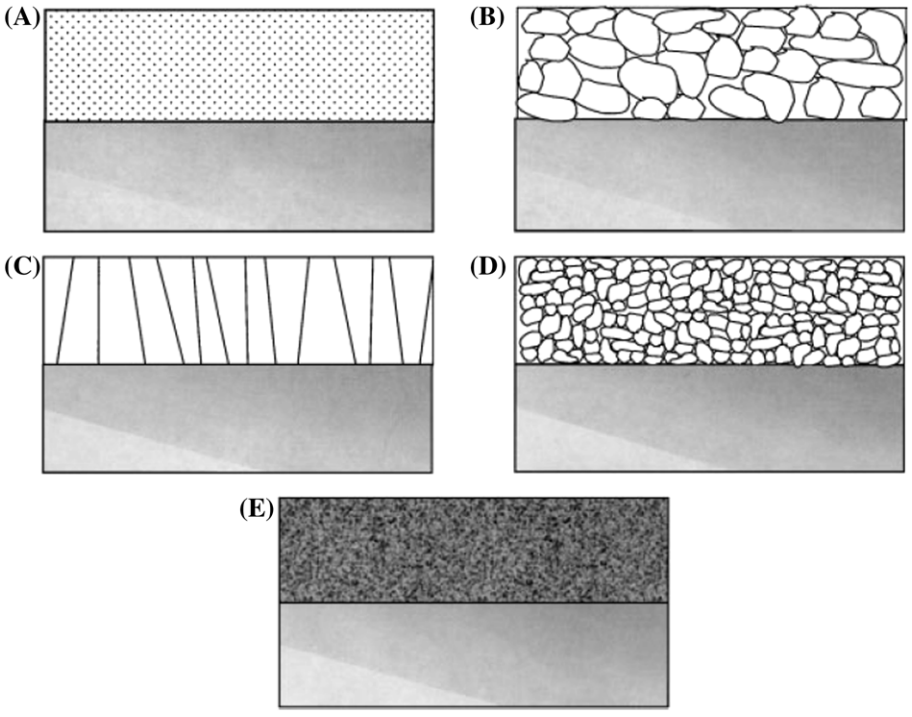

FIGURE 4 Diffusion barrier microstructure can be classified as: A, crystalline; B, polycrystalline; C, polycrystalline columnar; D, nano-crystalline; and E, amorphous (reproduced from Kaloyeros and Eisenbraun[130])

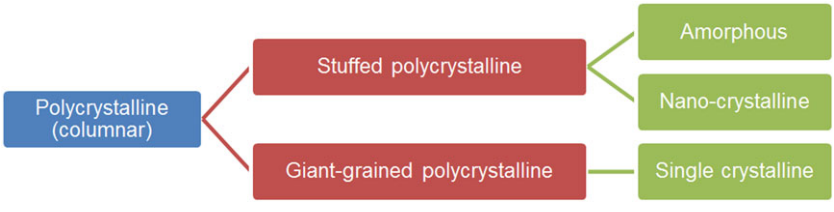

FIGURE 5 Evolution of diffusion barrier quality in terms of crystallinity from left to right [Colour figure can be viewed at wileyonlinelibrary.com]

binary and ternary alloys are not effective seed layers for electroplated Cu due to their high resistivities.[145] A diffusion barrier process, developed by Colgan and Fryer, that has been extensively used in the fabrication of IC interconnects, involves the sputtering of a very thin layer of N-doped Ta (32 Å) followed by a subsequent low resistivity alpha-Ta seed layer deposited without breaking vacuum.[133,146] This process results in an amorphous N-doped Ta diffusion barrier with the desirable formation of alpha (bcc) Ta which has lower resistivity than the beta phase and hence is a more suitable seed layer for Cu electroplating.

Although a large number of studies that document barrier layer properties for Cu interconnects have been published, when we trace the comparative investigations into diffusion barrier layers for Si PV we see significantly fewer reports. SunPower reported the use of a sputtered Ti/W diffusion barrier with a Cu seed layer for their Cu-plated IBC cells,[47] but the plated metallisation processes developed for p-type cells have focused on using plated Ni diffusion barriers for Cu and few reports address the adequacy of these layers compared with diffusion barriers deposited by PVD methods.[147] The electroless Ni/Cu plating process that BP Solar used in their Saturn LBG technology was developed by Motorola in 1970s.[40,148] The underlying thin Ni layer was sintered to form a Ni silicide, and residual Ni was then stripped followed by flash plating of Ni and Cu and immersion capping with Ag. It was understood at the time that the electrolessly-plated Ni layer provided a diffusion barrier for the subsequently plated Cu, and Motorola claimed that the metallisation system was expected to be stable for 20 years assuming an exposure of 6 hours per day at ~60°C.[49] However, in discussions following a research forum on Photovoltaic Metallization Systems in 1983, Nicolet cautioned care with regard to assuming that plated Ni layers were stable diffusion barriers for Cu.[49,132]

Electroplated metal deposits are typically polycrystalline, with smaller grains expected for metals having high melting points.[143] Nickel has a high melting temperature of 1455°C and cross-sectional images of Ni/Cu stacks formed using bias-assisted LIP[39] show that the Ni layer is clearly polycrystalline with many small grains thus confirming expectations from theory (see Figure 6). Copper is an extremely effective grain boundary diffuser, especially in the presence of sink reactions.[138,139,143,149,150] Consequently, LIP Ni is not expected to present an effective barrier to Cu, especially in the situation where defects (eg, such as introduced by laser ablation as shown in Figure 7) exist at the Si surface to provide a sink for Cu diffusion.

If impurities are present in significant concentrations in electrochemically deposited films, then the resulting films can be amorphous.[141] This may be beneficial for diffusion barriers as amorphous materials can provide a more effective barrier due to the lack of grain boundaries that can provide paths for diffusion.[137] In the hypophosphite-based Ni-P process[151] used by Motorola, P is co-deposited with Ni at concentrations of 3% to 15%.[40,152] Bredael et al reported that when the percentage of incorporated P exceeds 11.6%, the resulting films are expected to be amorphous rather than polycrystalline.[153] However, review of the properties of a commonly-used alkaline electroless Ni-P formulation that was used in the early development of the LBG cells (Transene's Nickelex) solution reveals that only ~1% P was expected to be deposited with the 90°C to 98°C plating process proposed in the technical data sheet.[154] Consequently, it is assumed that the Ni barrier layers of BP Solar's cells were polycrystalline and therefore would not necessarily have provided an effective passive barrier to Cu diffusion. However, as mentioned above, 20-year-old BP Solar Saturn modules are continuing to achieve PRs that exceed those of comparative screen-printed modules of the same age installed at the same location.[54]

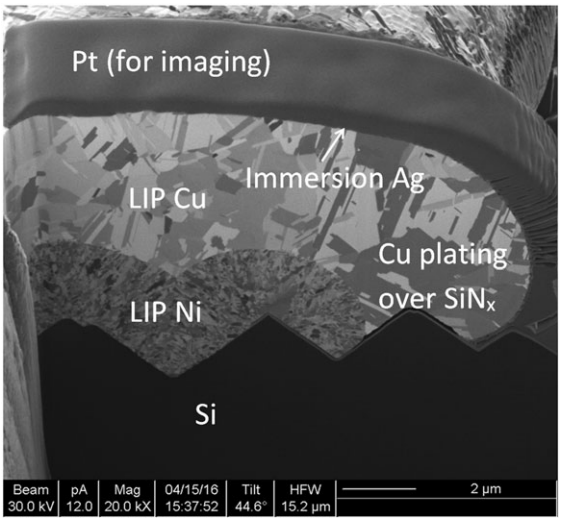

FIGURE 6 Cross-sectional SEM image of a Ni/Cu finger, deposited using bias-assisted LIP onto Si exposed through a UV ps laser-ablated opening in a PECVD SiNx ARC dielectric layer of thickness of ~75 nm. The right side of the image shows the plated Cu growing directly over the SiN_x ARC of the solar cell (image by W. Zhang, UNSW Sydney)

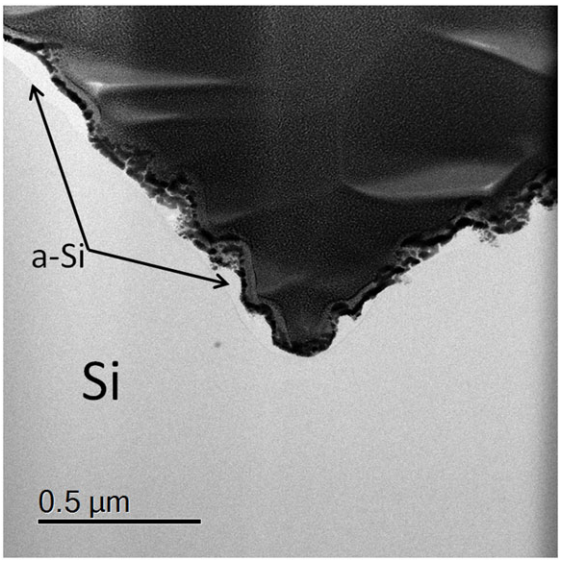

FIGURE 7 Cross-sectional TEM image showing laser damage and amorphous Si (a-Si) formation resulting from 266-nm ps laser ablation of the SiN_x ARC on a monocrystalline Si solar cell (image by N. Song, UNSW Sydney)

Following the initial success of BP Solar with their use of Cu-plated metallisation, Suntech also adopted Cu plating for their laser-doped selective emitter (LDSE) cells.[59,155] They addressed the problem of a slow Cu plating rate by pioneering the use of LIP[50-52] for depositing Ni and Cu in the production of their Pluto cells. This

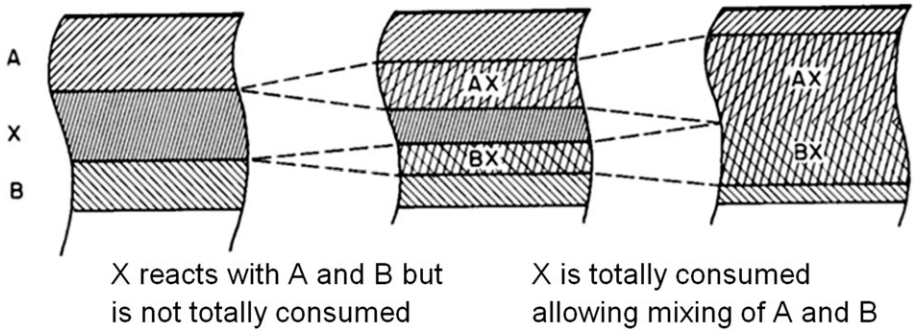

FIGURE 8 Schematic depicting a sacrificial barrier (adapted from Nicolet and Bartur[132]). The Si/Ni/Cu system can be represented by B/X/A. if the rates of formation of AX and BX are known, then the time at which AX and BX come in contact with each other can be predicted

not only allowed the Cu plating time to be reduced from 3 hours to ~10 minutes[46] but also ensured the long life of the electrolyte in their inline plating tool. However, an implication of using LIP Ni was that the barrier layer was clearly now polycrystalline and therefore provided many paths for Cu diffusion to the Si interface. At the time Pluto modules were released into the market, Suntech claimed to be performing advanced levels of environmental testing on its products,[60] and so given these reports it would appear that even if the Cu could penetrate through LIP Ni diffusion barriers in Pluto modules, the electrical performance of modules was not significantly degraded. This conclusion is also supported by a number of other studies which have reported that Ni/Cu plated modules, where the contact regions in the cells had been formed by short pulse laser ablation, have also passed the thermal cycling and damp heat test sequences required by the IEC 61215 standard.[2,4,6,10,156]

One possible reason for this apparent durability of Cu-plated Si PV modules may be that the Si/Ni/Cu system forms a sacrificial diffusion barrier for Cu, with the Ni both reacting with the Si to form a silicide and alloying with the Cu. When elements of a metal stack intermix then a sacrificial barrier[132,143] can form (see Figure 8) and, provided that the Ni is not totally consumed, an effective diffusion barrier can result. If the reaction rates of the two intermixing reactions (ie, that form AX and BX, respectively) are known as a function of temperature, then it can be predicted when A and B come into contact with each other. This fact was recognised in the early reports on Ni/Cu plating for Si solar cells[148] and would also suggest that a sufficiently thick Ni layer should be plated to ensure that if alloying with Cu, and possibly also Si, continues into a module's life that all the Ni is not consumed.

Although the BP Solar plating process was complex and costly to achieve in production due to having to dry wafers in between the initial Ni and subsequent Ni/Cu/Ag plating processes, it could potentially address both the requirements of forming a uniform Ni silicide and ensuring that sufficient Ni remained in the metal stack to form an effective sacrificial barrier. Consequently, the plating process may have contributed to the stability of the BP Solar Saturn modules. However for Suntech's Pluto modules, it is questionable whether a sufficient Ni silicide formed in the laser-doped openings due to the significantly shorter sintering time (1-2 minutes at 350°C compared with 30 minutes at 220°C[40]) and the presence of an oxide at the surface of the continuous wave (CW) laser-doped regions which is known to inhibit silicide formation.[157] This would suggest that, at least for the case of the Pluto modules, the Si/Ni/Cu may not have acted as an effective sacrificial barrier to Cu diffusion and some other factor (s) must have contributed to the stability of these plated modules.

Further evidence to support the assumed stability of Cu-plated modules in the field has been provided by studies that have evaluated the effectiveness of various Ni barrier layers on maintaining the pseudo fill factor (*pFF*) of heat-treated and cooled Cu-plated Si solar cells at close to their initial values.[156,158-160] The rationale for this analysis is that, if Cu penetrates through the barrier, then the performance of a solar cell will be most likely impacted first by junction recombination due to Cu's likely precipitation at the junction as discussed in Section 2.1.1. Figure 9 shows how the *pFF* of Cu-plated cells degraded with increased hotplate heating duration. The degradation occurred at a faster rate when annealing at higher temperatures and for cells with a lower Ni barrier layer mass. From an Arrhenius analysis using the time taken for the *pFF* to decay to 95% of the pre-heat treated *pFF* value[†] for different temperatures, it was concluded that for 20-mg Ni (estimated to correspond to 200 nm of Ni barrier layer thickness), the cell lifetime would not be limited due to Cu diffusion at 80°C for 100 years.[160]

The activation energy, E_A, predicted from Kraft's analysis was 1.01 eV for 20-mg Ni,[160] which is ~ half the E_A of Cu diffusing through pure Ni. Given that the *pFF* degradation involves multiple steps (Cu diffusion through Ni, Cu diffusion in Si, and presumably also Cu precipitation close to the junction), the estimated E_A is representative of the rate limiting step associated with the degradation which in fact may well be the precipitation reaction rather than the diffusion of Cu through Ni. Consequently, it can be concluded that the E_A estimated by Kraft for Cu transport through the Ni barrier is at most half of that expected for diffusion through pure Ni and could actually be much lower. This suggests that the microstructural properties of the plated Ni barrier layer can contribute to enhanced Cu diffusion into the cell.

Although monitoring of cell *pFF* may be a useful metric by which to predict solar cell tolerance to Cu as a function of barrier layer properties, Kraft identified the sensitivity of this analysis to the time interval between measurements. If cells were measured less frequently, then a greater *pFF* degradation resulted (see Figure 10). He attributed this to the fact that Cu, which penetrates into the cell, has a greater chance of diffusing to the junction where it can impact the *pFF* when the high temperature treatment was longer. Figure 10 appears to suggest that

[†]This limit of 95% loss in *pFF* relates to the requirement for module power degradation following IEC 61215 environmental testing to be <5%.

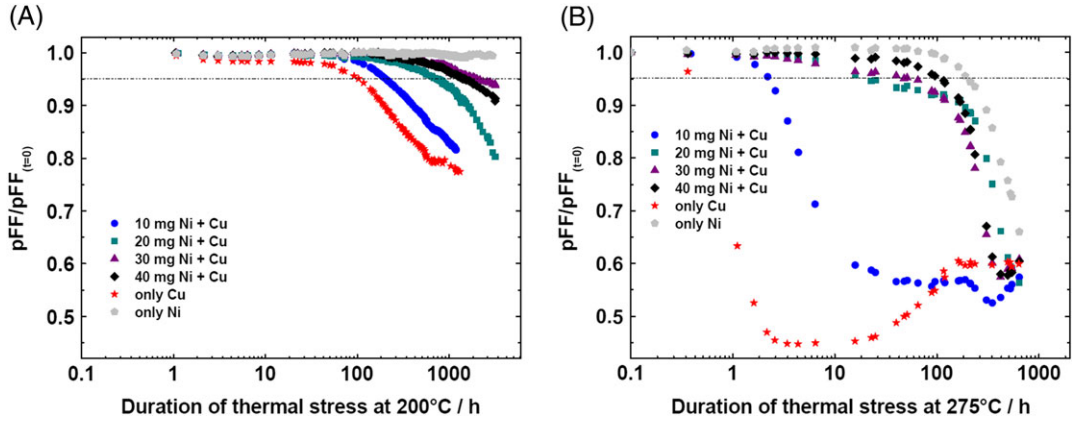

FIGURE 9 Value of $pFF/pFF_{t=0}$ as a function of time exposed to thermal stress (hotplate heating) at (A) 200°C and (B) 275°C for Si solar cells plated with different Ni masses (with Cu), only Ni and only Cu. The cells were allowed to cool for 2 min in ambient before measurement of the *pFF* using a Suns-V_{OC} measurement (reproduced with permission from Kraft[160]) [Colour figure can be viewed at wileyonlinelibrary.com]

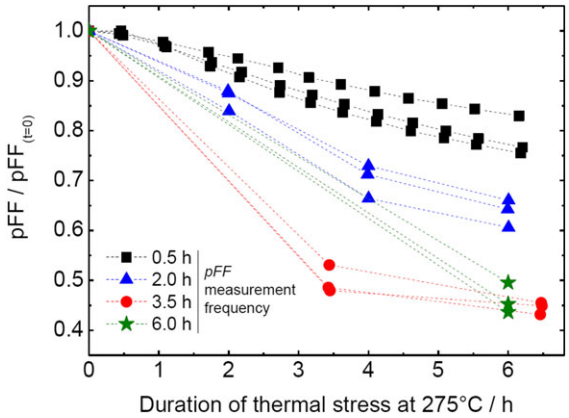

FIGURE 10 Values of $pFF/pFF_{t=0}$ measured for cells (with a screen-printed Ag barrier layer) heated on a hotplate at 275°C and remeasured using Suns-V_{OC} at different time intervals (reproduced with permission from Kraft[160]) [Colour figure can be viewed at wileyonlinelibrary.com]

once the intervals between measurements are at least 3.5 hours, then the sensitivity to the frequency of measurement is removed and the true impact of the Cu diffusion into the cell can be observed. Although these measurements were obtained from cells which had a screen-printed Ag seed layer under the plated Cu, they demonstrate that if Cu does penetrate through the barrier then the impact on the electrical properties of the cell depends also on the durations of the heat treatments.

In addition to the complexity introduced by the dependence of the degradation rate on the measurement interval, Colwell et al raised a further complication for this Arrhenius analysis.[139] They showed that Cu could also diffuse through plated Ag capping layers during heat treatments to result in voids under the Ag capping layer and an additional partially oxidised Cu layer over the surface of the contact. This outward diffusion of Cu can reduce the accuracy of *pFF* measurements by significantly increasing the contact resistance between the plated contact and measurement probe and suggests that it may be more appropriate to perform Arrhenius analyses on encapsulated modules rather than cells.

In order to resolve the conundrum between the observed electrical stability of Ni/Cu plated Si PV modules, the expected deficiency of plated Ni layers in providing a barrier to Cu diffusion and the heating duration sensitivity of the Arrhenius analyses, it is necessary to perform material studies. Using cross-sectional TEM/EDX of heat-treated Ni/Cu plated LDSE cells, Flynn and Lennon observed Cu precipitates in the Si under Ni/Cu plated fingers of cells after heat treatment and quenching in ethylene glycol (see Figure 11). However, if the heated cells were slow-cooled, then no precipitates were observed in any of the TEM cross sections imaged. Furthermore, precipitates were observed in all the TEM images recorded for quenched samples, irrespective of whether the Ni had been plated using an alkaline electroless hypophosphite process or by bias-assisted LIP. Flynn and Lennon

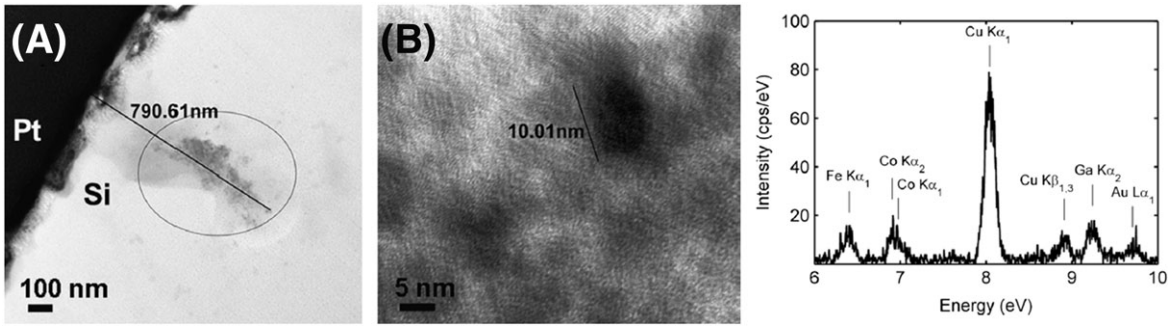

FIGURE 11 Cross-sectional TEM images showing Cu precipitates in the region under a metal finger in a p-type LDSE cell which was heated at 400°C for 5 h and then quenched in ethylene glycol. In A, closely-packed Cu precipitates located ~ 790 nm from the cell surface were identified using EDX; B, shows a close-up view of individual Cu precipitates; and C, shows an EDX point analysis of a precipitate identified from a TEM image (reproduced from Flynn and Lennon[69])

also confirmed that thermal treatments only resulted in an electrical impact when cells were rapidly cooled after heating. This was presumably because the Cu had insufficient time to out-diffuse to the surface during quenching and instead precipitated in the n-type Si causing increased recombination in the emitter of the cells. The observed Cu precipitate formation with high cooling rates in n-type Si is consistent with the findings of Istratov et al[72] and Flink et al.[71]

This proposed theory may explain the observed stability of Ni/Cu plated Si PV modules. Because modules are not rapidly cooled in thermal cycling and damp heat environmental tests and are not expected to experience temperature changes in the order of 100 K/s[69,72,160] in the field, any Cu that enters the cell during higher temperature exposure would be expected to out-diffuse to the surface. Significantly increased recombination due to Cu precipitating at the Si surface would not be expected if the precipitates formed at the site of metal contacts or if the charge properties of the overlaying dielectric (SiN_x in the case of the LDSE cells) minimised the concentration of minority carriers at the surface. The use of a selective-emitter (SE) in cells (as in the case of the LBG and Pluto cells) would be expected to further 'constrain' any out-diffused Cu to the n+ regions where its potential impact on the electrical properties of the cell is reduced even further. Furthermore, in the case of the Pluto LDSE cells, crystal defects in the n^+ Si region under the contact[59,161] may have also provided effective gettering sites for any entrant Cu. Although this apparent out-diffusion/gettering of Cu to heavily-doped n-type surfaces may be fortuitous for SE p-type solar cells, the case may be different for n-type Cu-plated PERT cells where Cu precipitates may form in the base of the cell.[162-165]

From the previous discussion on diffusion barriers, it must be concluded that most (if not all) Cu-plating processes that have been developed for Si solar cells since the 1980s have perhaps incorrectly assumed that plated Ni layers provide an effective diffusion barrier for Cu. The observed durability of Cu-plated modules may explain why Si PV engineers have persisted with plated Ni diffusion barriers whilst reports of more effective diffusion barriers were available from the IC research. Another reason for this persistent use of plated Ni in Si PV is that the task of forming a cost-effective diffusion barrier for Si solar cells is perhaps more challenging than for the IC application. The surfaces of commercially-produced p-type Si solar cells are textured (eg, with random pyramids in the case of monocrystalline p-type cells) for anti-reflection and light trapping, and this rough surface makes it difficult to form uniformly thick barrier layers. For example, the TaN/Ta process developed by IBM in the late 1990s used sputtered N-doped Ta layers as thin as 32 Å as the diffusion barrier. Such uniformity would be difficult to achieve on alkaline-textured Si surfaces without some regions being thicker, and hence more resistive, and other regions potentially not being covered sufficiently. This situation is exacerbated when the Si surface is required to be rough for strong adhesion as discussed in Section 2.2.2 (see also Figure 7). Additionally, PVD processes such as sputtering have been considered too costly for use in solar cell mass manufacturing due to their slow deposition rate and the need to use a vacuum.

Whilst some ingress of Cu into Si solar cells in the past may not have impacted electrical performance of modules significantly, as manufacturers strive to achieve higher efficiencies through the use of more lightly-doped emitters in p-type cells and more stringent accounting of device recombination, the impact of additional recombination due to Cu, which has diffused from cell-level metallisation, may ultimately limit device efficiency. Consequently, it may be prudent to develop more robust diffusion barrier processes/materials that can prevent the ingress of Cu into the cells in the first place. Given Cu's rapid diffusion once it is in the Si, it is reasonable to assume that any weaknesses in a barrier layer across the solar cell (eg, defects in the Ni plating) may impact the performance of higher efficiency cells and modules.

Electrochemical deposition is well-suited to covering rough surfaces uniformly, and so it may be an appropriate low-cost method for diffusion barrier formation on textured Si surfaces. However, it can be challenging to 'plate' metals to Si,[166] and the use of LIP to form the barrier layer can complicate the matter even further as the surface overpotential needs to be carefully controlled to minimise the H_2(g) evolution. Nickel plating processes previously optimised for the lower voltage full-area Al BSF cells need to be tuned for the plating of PERC cells as an increase in the surface potential can result in an increased evolution of H_2, and gas 'bubbles' can block Ni nucleation sites at the Si surface and impact the interfacial adhesion. Additionally, evolved H_2 can result in the formation of colloidal Ni $(OH)_2$ on the Si surface which further catalyses the H_2 evolution reaction.[167] Consequently, approaches which seek to add impurities to the plated Ni (eg, as described by Younes et al[141] and Cai et al[168]) to reduce the crystallinity of the barrier layer for improved diffusion barrier performance need to consider carefully whether the added impurities may also enhance the rate of H_2 evolution (eg, additives such as Co, P, and W are known to catalyse H_2 evolution[169]). Interestingly, approaches which increase the roughness of the Si for improved adhesion (see Section 2.2.2) may also contribute to increased H_2 evolution through the increased surface area.

Copper ingress into devices through dielectrics

Copper may also penetrate into IC devices and solar cells through its contact with a dielectric. For VLSI devices, the full encapsulation of the Cu connectors with an effective diffusion barrier can be difficult to achieve (eg, on the sidewalls of vias as shown in Figure 1A). This can leave Cu in direct contact with the dielectric. Copper has been shown to penetrate through SiO_2 layers by diffusion[137,170] and drift processes.[137,171] This transport can be retarded by the use of CVD SiN_x,[137,172] although these barriers are not well suited to interlayer devices due to SiN_x being non-conductive. Processes whereby the SiN_x completely covers only the sidewalls of vias and not the bottom device surface would be required. For this reason, alternative barriers are typically used in VLSI devices which involve either: (1) the deposition of thin metal layers (eg, Ti or Al) which form more stable oxides with SiO_2 in preference to Cu; or (2) the deposition of refractory nitrides (eg, TiN[173]) as discussed in Section 2.1.1.[137]

It is also possible for plated Cu to diffuse into Si solar cells through the dielectric adjacent to the plated conductors.[160,174] When openings are formed in a dielectric ARC mask, and Ni and Cu are plated to the Si exposed in the openings, the Cu deposit can extend over the underlying dielectric layer placing it in direct contact with the cell's ARC (see Figure 6). Kraft evaluated (using photoconductance lifetime measurements) the ability of SiN_x ARCs deposited using inline PECVD, sputtering and batch PECVD on Si wafers to prevent ingress of Cu that

was evaporated onto the dielectric surface after being held at 300°C for 500 hours. The effective minority carrier lifetime was only decreased for wafers where the SiN_x had been deposited by inline PECVD, and the observed decrease was ≤10%. It was concluded that Cu ingress through the adjacent dielectric was not a significant problem for Si solar cells.[159]

However, a concern introduced by the use of lasers to form the openings in the ARC for plated contacts is that the ARC can be damaged by the laser, leaving additional paths for Cu to enter the cell through the dielectric.[175,176] For example, CW laser-doping processes can result in molten Si being ejected onto the surface in the regions adjacent to the fully-opened area (see Figure 12). This damage can result in lightly-doped Si being in contact with plated metal which, in addition to increasing contact recombination (see Section 2.1.2), can provide a further path by which Cu may enter the solar cell.

Although SiN_x appears to provide a more effective barrier than SiO_2,[177] Miyazaki et al have highlighted the importance of measuring material properties rather than just electrical properties as charge transport can be masked by the positive Cu ions being compensated by trapped electrons in SiN_x films deposited by PECVD.[172] Gupta et al also reported that Cu could diffuse through amorphous hydrogenated SiN_x films that had been deposited by PECVD at temperatures <400°C and accumulate at interfaces.[178] Because the SiN_x films being used as ARCs for Si solar cells are similar to the films investigated by both Miyazaki et al and Gupta et al, it is suggested that, as for diffusion through Ni barrier films, more material studies need to be performed for Cu-plated Si solar cells with SiN_x ARCs, with Cu penetration being investigated under both thermal and voltage stress. Although carrier lifetime studies can be used to identify barrier failures, these studies need to be performed using cells with low recombination emitters and be supported by material (elemental) studies to provide the necessary confidence that Cu-plated modules can achieve the required durability in the field.

2.1.2 | Contact recombination

Metallisation of solar cells introduces contact recombination if the metal is in direct contact with the Si of the cell. The doping density of the Si at the surface directly affects the recombination current density under the metal, so whilst it may seem beneficial for Ni/Cu plated contacts to be able to form ohmic contacts to Si surfaces with P concentrations as low as 4×10^{19} cm^{-3},[10,63] the reduced emitter recombination current density, that results from adoption of more lightly doped emitters, may be achieved at the cost of a larger contact recombination current density due to the higher concentration of minority carriers at the metal-Si surface.[57,63]

In a two-diode model of a solar cell, the recombination current density J_{0n} (n = 1 and n = 2) for the cell can be expressed as the sum of the recombination current densities occurring in the different parts of a solar cell, with the dominant n = 1 recombination current density, J_{01} being represented as:

$$J_{01} = J_{01,\text{emitter}} + J_{01,\text{base}} + J_{01,\text{rear}}, \quad (1)$$

where $J_{01,\text{emitter}}$, $J_{01,\text{base}}$, and $J_{01,\text{rear}}$ represent the recombination current densities arising from the emitter, base and rear surface components of the solar cell, respectively. The recombination that occurs in the emitter can be further broken down into recombination current densities that occurs under metal contacts, $J_{01,\text{cont}}$, and in the regions coated with the ARC, $J_{01,\text{pas}}$, according to:[62]

$$J_{01,\text{emitter}} = \frac{1}{A_{\text{cell}}}\left((A_{\text{cell}} - A_{\text{cont}})J_{01,\text{pas}} + A_{\text{cont}}J_{01,\text{cont}}\right), \quad (2)$$

where A_{cell} and A_{cont} represent the areas of the cell and metal-contacted region, respectively.

Technology roadmaps predict continually decreasing $J_{01,\text{emitter}}$ values, with values < 50 fA/cm^2 expected in production by 2024.[1] Although Min et al suggest that very low $J_{01,\text{emitter}}$ values for P-doped emitters (~10 fA/cm^2) can be achieved by either: (1) reducing the electrically active P concentration to $<2 \times 10^{19}$ cm^{-3} whilst also reducing the SRV of holes to <1000 cm s^{-1}; or (2) increasing electrically active P concentration up to 1×10^{21} cm^{-3},[179] to-date most focus appears to be placed on the former approach due to the difficulty in achieving very high P concentrations at the surface without P precipitates using standard tube diffusions. Unlike screen-printed Ag, plated Ni can make

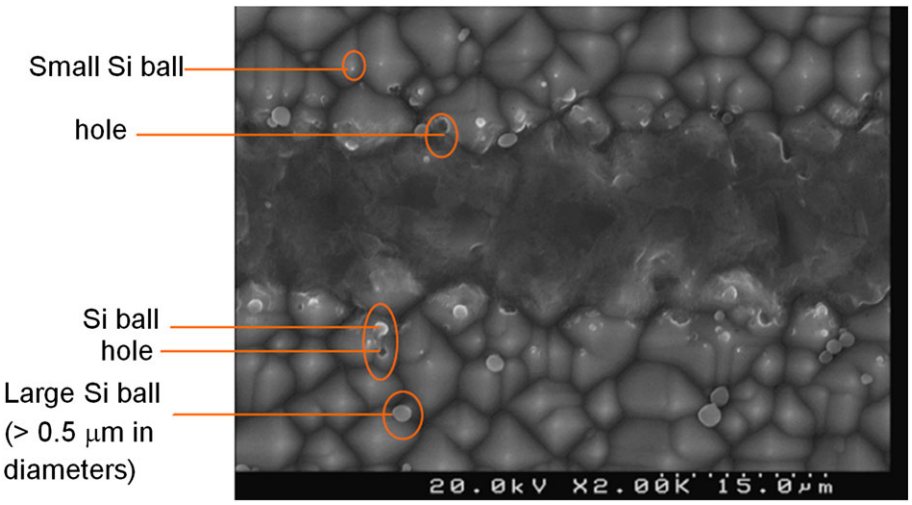

FIGURE 12 Scanning electron microscope image of a laser-doped opening in a SiN_x ARC formed using a 532-nm CW laser. During the laser melting, defects comprising openings where "balls" of Si were forced out of holes are evident adjacent to the line opening (from Sugianto[175]) [Colour figure can be viewed at wileyonlinelibrary.com]

ohmic contact to Si with P concentrations <2 × 10^{19} cm^{-3} (see the contact resistivity comparison reported by Kluska[62]); however, Figure 13 suggests that the junction depth will need to approach 1.5 μm for $J_{01,cont}$, to reach values of ≤600 fA/cm^2, given this low P surface concentration.[62,180,181]

Contact recombination can be minimised by reducing the contact area, and hence finger width. However, further reductions in contact widths are to a large extent limited for Si PV by the requirement to use lower-cost patterning methods. So, unlike the IC industry, which can use photolithography to form very small area contacts, there is a limit to how small contact areas can become for Si solar cells without increasing processing cost. Furthermore, the smaller contact areas achieved by lasers for plated contacts require higher aspect ratio conductors with a smaller interface area for adhesion, which can present potential additional challenges with respect to module reliability (see Section 2.2.2). One approach to reducing contact recombination is to use a SE, where the surface under the metal contact is more heavily-doped.[57,182] Copper-plated metallisation has been demonstrated with solderable p-type SE PERC cells;[183,184] however, achievement of the SE required additional patterning steps to either form the SE[184] or form anchor points in laser-doped regions to provide sufficient adhesion for soldered interconnection.[183]

The specifics of the metallisation process may also impact the magnitude and properties (ie, ideal or non-ideal) of the surface recombination by providing additional recombination sites some distance from the metal surface. For example, Ni silicides and Ag crystallites may extend non-uniformly into the Si from the metal surface for plated and screen-printed cells, respectively. For plated cells, depending on the thermal conditions used for silicide formation, Ni can penetrate some distance from the surface and may impact the *pFF* of the device through increased non-ideal recombination.[11,184,185] Figure 14 shows a TEM image of a silicide formed after sintering a Ni layer (which had been deposited using LIP) for 10 minutes at 450°C. The silicide extends into the Si wafer as much as 100 nm and introduces a non-uniform interface with the Si due to the difficulty of removing all the oxide from the surface.[186] This non-uniform growth can increase non-ideal (n = 2) recombination and present an effective metal-Si area that is larger than the projected area of the contact on the surface. To some extent, this problem can be addressed by engineering a deeper junction[10,184]; however, the longer diffusion times required to form deeper junctions may not always be justified in a manufacturing environment.

The different physical processes involved in forming metal contacts to cells are expected to impact the accuracy of simulation models used to estimate the $J_{01,cont}$ (such as depicted in Figure 13) and suggest that it will be important in the future to accurately measure contact recombination for Ni/Cu plated cells in order to also take into account non-ideal recombination which may be incurred through the metal contact, and to draw comparisons with screen-printed Ag contacts.[187-193]

2.2 | Module reliability

Most Si PV module manufacturers provide a 25-year warrantee which covers safe operation (no electrical, thermal, mechanical, and fire hazards) and a performance of at least 80% of nameplate power after 25 years.[194] If this 80% power loss occurs linearly with time,[195] then it correlates to an annual degradation rate of 0.5% per year. A 2016 study by Jordan et al identified a mean annual degradation rate of 0.8% to 0.9% for crystalline Si PV modules from ~ 200 studies involving 40 different countries.[194] This suggests that many of the currently installed Si PV modules will not meet the expected performance after 25 years. Although a large number of warrantee returns might be expected, this may not occur as it can be time-consuming to directly measure power generation from individual modules in an array.[196] However, with the requirement to more accurately predict the power generated from large PV arrays, it is expected that there will be increased monitoring of power generation at a module level and therefore unacceptable power degradation may be more actively policed in the future. Another reason for more pro-actively striving to reduce annual degradation rates is that increased module lifetime is an effective way in which the LCOE of PV-generated electricity can be reduced.[53]

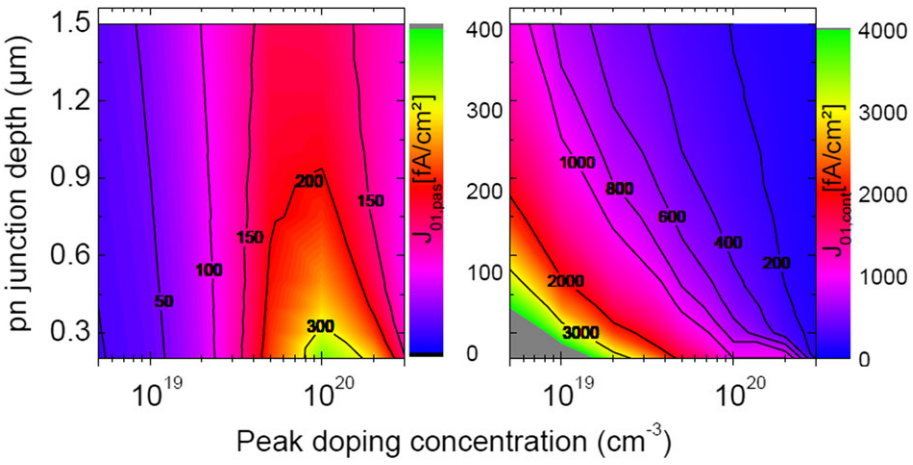

FIGURE 13 Calculated recombination current densities for passivated, $J_{01,pas}$ (left) and metallised, $J_{01,cont}$ (right) Si surfaces resulting from Gaussian P doping profiles with a range of metallurgical p-n junction depths and peak doping concentrations. The calculations were performed using the EDNA software[180] and assuming the parameterised SRV provided by Altermatt et al[181] for calculation of $J_{01,pas}$ and a SRV of 10^7cm/s for $J_{01,cont}$ (reproduced with author permission from Kluska[62]) [Colour figure can be viewed at wileyonlinelibrary.com]

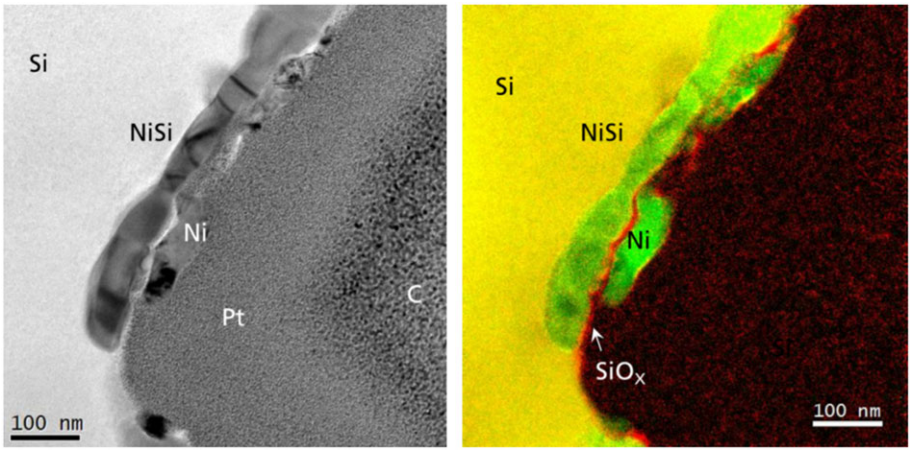

FIGURE 14 (Left) Transmission electron microscope images of a Ni silicide region formed at an alkaline-textured Si surface under a Ni/Cu finger plated using LIP; and (Right) energy-filtered TEM elemental mapping (Si = yellow, Ni = green, O = red) of the image shown on the left (from Mondon et al[186]). The $NiSi_x$ was assumed to grow through pinholes in an interfacial SiO_x layer on the Si surface [Colour figure can be viewed at wileyonlinelibrary.com]

Almost all reports to-date which investigated failure modes of field-aged Si PV modules have been based on modules which have screen-printed cell-level metallisation. Typical metallisation failures include finger or busbar discolouration,[197] solder joint failure,[198,199] finger breaks (often caused by cell cracking), and interconnect failure.[197-199] Use of Cu-plated metallisation may introduce failure modes in addition to those observed with screen-printed cells due to the larger number of metal interfaces and the possibility of Cu ingress into the Si. Additionally, unlike screen-printed Ag fingers which are fired to induce the penetration of Ag crystallites into the Si,[200] plated metal adheres to a Ni silicide surface. This different contact formation method also introduces the possibility of finger (and busbar) dislodgement in modules. However, set against these concerns is the possibility that the stronger cohesion or strength of plated fingers may make them less likely to break in the event of cell cracking. This can potentially reduce the electrical impact of cell cracking in modules.

Consequently, any introduction of Cu plating for cell-level metallisation must also consider reliability. This section first presents a discussion on reliability testing in Section 2.2.1 then, in the following sections, potential reliability issues that may be introduced with Cu-plated modules will be reviewed. In particular, contact adhesion and metal contact integrity are discussed in Sections 2.2.2 and 2.2.3, respectively.

2.2.1 | Reliability testing

Reliability is a facet of quality, but it is neither defined, nor covered by the existing IEC standards.[201,202] So whilst the IEC standard can identify design, materials, and process flows that could lead to premature field failures, measures of reliability require field data which can be collected from PV installations and accelerated field testing. Some testing laboratories provide comparative accelerated tests, which involve IEC qualification tests but using longer durations or combinations of the tests in different sequences.[203,204]

The objective of reliability testing is to estimate the expected lifetime of a device for a specific use, environment, and power generation. The testing can identify key issues with durability (eg, degradation or corrosion of metal contacts) which manufacturers can then address through changes in process and/or materials. Results of reliability testing can also allow manufacturers to differentiate their products through their longer predicted lifetimes and to secure investment for new construction projects.[203]

Due to the complexity of ICs and their large number of components, reliability testing for these devices is well established and quantitative in terms of metrics such as mean time between failure (MTBF) and mean time to failure (MTTF).[205] The metric MTTF is a measure of reliability that is reserved for non-repairable items, whereas MTBF is commonly used to indicate the reliable lifetime of a device or component which can be repaired. Failure-in-time (FIT) is another way of reporting MTBF and is defined as the number of failures per million hours for a repairable product, with 1 FIT being equivalent to having an MTBF of 10^9 hours. The terms MTBF and FIT are commonly used by the semiconductor industry and component manufacturers, whereas many quantitative reliability studies involving Cu-plated interconnects have used MTTF as typically the failure mechanisms are non-repairable (eg, voiding due to electromigration[206,207]).

However, reliability testing for PV modules is made more difficult due to a number of reasons. First, modules in the field may fail due to many different mechanisms, and therefore an accurate estimate of lifetime requires study of all these mechanisms. Second, the environments in which PV modules are installed vary much more than for most electronics, making it difficult to reduce the anticipated failure mechanisms to a more manageable list. This also makes it more complicated to simulate failures because many failures have been identified to occur as a result of multiple stresses applied in a sequence that may depend on the environment. Additionally, the rapid product-development cycle times that are common in the rapidly-growing PV industry, are at odds with the long expected lifetimes of products. As module prices drop rapidly, PV manufacturing companies are repeatably modifying their products and each small change can result in new failure modes that have not been previously studied.[208] All the previously mentioned challenges are made additionally more complex as degradation is typically gradual for PV modules rather than

catastrophic, and the degradation can be difficult to measure due to the difficulty in monitoring the generated power of individual modules in large PV arrays.[196]

The IC industry uses simulation methods to predict failure metrics. These simulations generally use failure statistics to derive constant failure rates for components which are then used by experiential rules to predict MTTF or MTBF. However, more recent approaches which include physics of failure (PoF) indicators in addition to statistical failure rate data have been proposed to provide more accurate reliability estimates.[209-211] In addition to developing more formal and standardised ways of assessing reliability, the physics underlying failure modes has generally been well researched within the IC industry in order to improve products in terms of reliability and/or performance. For example, IBM's introduction of Cu interconnects motivated studies that investigated durability concerns (due to electromigration) arising from using Cu instead of Al, and using electrodeposited Cu rather than CVD Cu.[212] As the dimensions of interconnects decreased, more sophisticated methods for reliability testing have been suggested[213,214] with simulations increasingly being used to predict FIT values for electronic devices.

There are currently limited simulation tools available to predict failure metrics for Si PV, especially models that take into account annual degradation rates.[196] There is also limited PoF analysis currently being performed with most manufacturers relying on electrical measurements and pass/fail statistics. In order to address the large fraction of metallisation and interconnection failures, a greater emphasis may need to be placed on analysing the PoF in Si PV modules, especially to address failures due to metallisation and interconnection. Sharma et al also concluded that new outdoor characterization methods are required to completely understand the degradation/failure mechanism of PV modules due to physical and chemical changes taking places at different interfaces.[195]

2.2.2 | Contact adhesion of plated metal

The early Jet Propulsion Lab reports raised concerns about the reliability, and more specifically, contact adherence of plated contacts to Si. In Motorola's final 1978 report for their Jet Propulsion Lab project they stated the following with respect to using electroless Ni for Si solar cell contacts:[40]

> "The first major problem area is uniformity control and repeatability of the plating process itself; the second problem area is ensuring good contact adherence, especially to shallow junction devices. Both of these problems contribute to questionable reliability."

BP Solar's application of Motorola's electroless Ni/Cu process to deep grooves did not appear to raise any issues with regard to contact adhesion. The process uniformity may have been assisted by the heavily-doped n^+ surface to which the Ni was plated. This permitted a long sintering duration that would be expected to effectively reduce any surface oxides which may have formed at the Si interface during the electroless Ni plating process.[40,215,216] Consequently, a uniform Ni silicide most likely formed across the entire contact surface and increased contact adhesion.[186,217,218]

However, weak plated metal adhesion did emerge as a problem when the plated Ni/Cu/Ag grid was formed flush to the solar cell surface as with Suntech's Pluto cells. With the Pluto (or LDSE) cell structure, the area available for contact adhesion was significantly reduced with the elimination of the grooves. Additionally, the CW laser-doping process results in smooth melted regions (see Figure 15) with contact adhesion being largely due to Cu adhesion to the peripheral rougher regions rather than the laser-doped surface itself.[219] Mondon et al proposed that Ni silicide does not form after sintering Ni-plated CW laser-doped surfaces due to the laser-doping process leaving the surface covered with an oxide that is difficult to remove without also etching the SiN_x ARC and causing overplating.[157] The necessity to form a Ni silicide under the contact for strong interfacial adhesion is discussed further below.

The weak plated metal adhesion to the CW laser-doped openings of LDSE cells meant that alternatives to soldering were required for cell interconnection. Wenham et al sought to address the poor adhesion to laser-doped regions by using lasers to form anchor points in the n^+ regions.[220,221] Although this process resulted in 90° busbar pull tests on PERC cells that were comparable to those measured on screen-printed cells, the cells with anchor points were limited by *FF*s

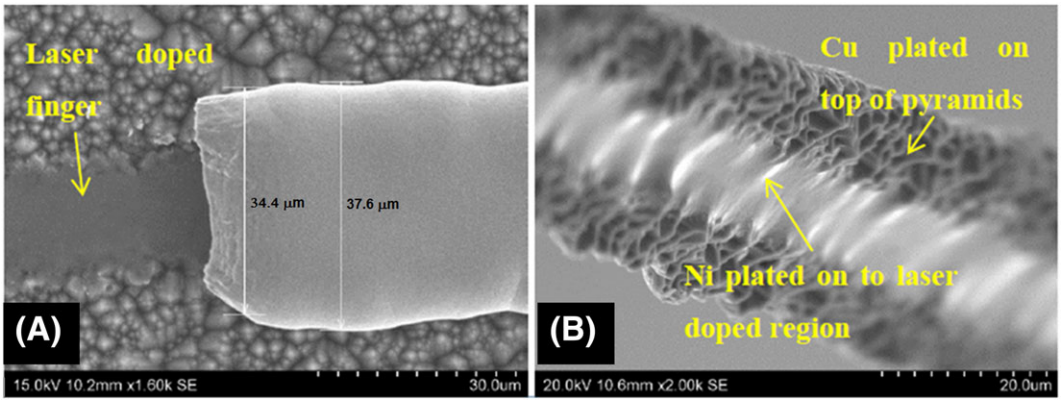

FIGURE 15 Scanning electron microscope images of: A, a Ni/Cu finger deposited using bias-assisted LIP on a laser-doped contact region with part of the finger removed to expose a smooth laser-doped Si region; and B, the underside of the removed finger showing the smooth Ni surface and the Cu morphology following the alkaline-textured wafer surface (from Yao[219]) [Colour figure can be viewed at wileyonlinelibrary.com]

that were <73%, presumably due to either increased non-ideal recombination or localised shunting.[183]

Another approach which has been successfully used to increase interfacial adhesion is the use of a ps UV laser to ablate the ARC from the Si surface.[2-4,10,222,223] The short pulse laser results in increased direct ablation of the SiN_x with only a small surface region of the Si being thermally-melted by the laser process.[224-228] Importantly from the perspective of increased adhesion, the short pulses cause the formation of laser-induced periodic surface structures (LIPSS)[229-234] on the exposed Si surface after SiN_x ablation (see Figure 16) which can act to increase the adhesion of plated metal.

The use of a UV ps laser has enabled busbar adhesion strengths and *FF*s that are comparable with, and in some cases superior to, screen-printed cells.[2-6,63,223,235-237] This was an important achievement for Ni/Cu plated cells because it has enabled the cells to be interconnected by soldering which is an established and cost-effective production process. However, the need to plate fingers and busbars at the same time using LIP can result in different plating rates across a cell due to the different opened areas.[223,236,238] Because the fingers also collect the light-induced current from the adjacent passivated regions, their plating rate can be faster than at the busbars.[239] Wang et al showed that if fingers were allowed to plate too quickly then, even though strong busbar pull forces could be achieved, finger adhesion could be sufficiently weak such that the fingers can dislodge from the Si surface and peel (see Figure 17).[223,236] This finding highlighted the need to monitor finger adhesion as well as busbar adhesion in a production process in order to identify any drift in the plating process.

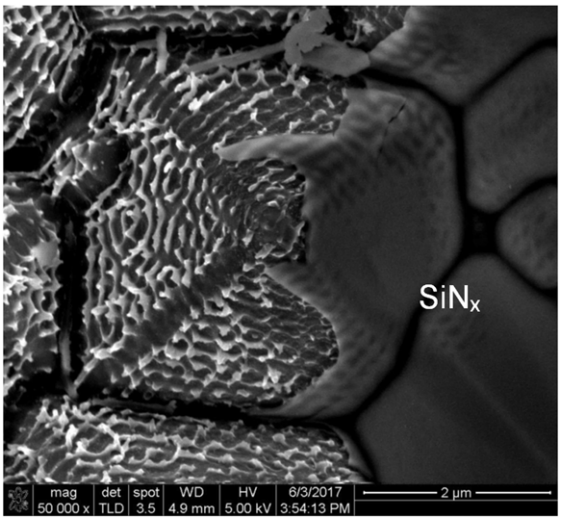

FIGURE 16 An exposed alkaline-textured Si surface showing formation of LIPSS by ablation of a SiN_x ARC using a 266-nm ps laser (image recorded by X. Shen, UNSW Sydney)

To address this need, Young et al designed a stylus-based finger adhesion tester (see Figure 18) that could measure the adhesive force of metal fingers by measuring the force required to dislodge or cut-through fingers from the Si surface.[240,241] This tool enabled cell adhesion to be mapped across a wafer to identify regions of lower adhesion and allowed correlations between plating rate and chemistry to be directly observed in finger adhesion measurements[236] (see Figure 19). This finger adhesion measurement technique also enabled finger adhesion to be spatially mapped across a wafer to detect variations in plating processes (see Figure 20).

Although the use of a UV ps laser has provided a method for forming adherent Cu-plated grids on Si solar cells, some concerns remain regarding variability in the process. Hsiao et al reported that the 180° busbar pull force measured for some p-type PERC cells could be as high as that measured for comparative screen-printed cells, but measurements on similarly-processed cells could be very low and insufficient for soldering.[184] They identified that Ni silicides (Ni_2Si and NiSi) could be detected in cells for which a strong pull force was measured but was absent in cells with a very low pull force. This result appears to confirm the requirement for Ni silicide formation for strong contact adhesion[242]; however, the reason for why the silicide formed sometimes and not at other times with post-plating annealing was unclear.

Silicide formation has been extensively studied for IC contact formation since the 1970s. Of the different silicides investigated, NiSi is attractive due to its low resistivity, low consumption of Si, ability to be formed in a single thermal treatment with a lower thermal budget (compared with Co and Ti silicide), minimal dependence on line width and relatively planar interface with the Si substrate.[243-245] Nickel silicides are also advantageous compared with other metal silicides due to the fact that silicide formation is driven by Ni diffusion (rather than Si diffusion), which reduces the likelihood of void formation in the

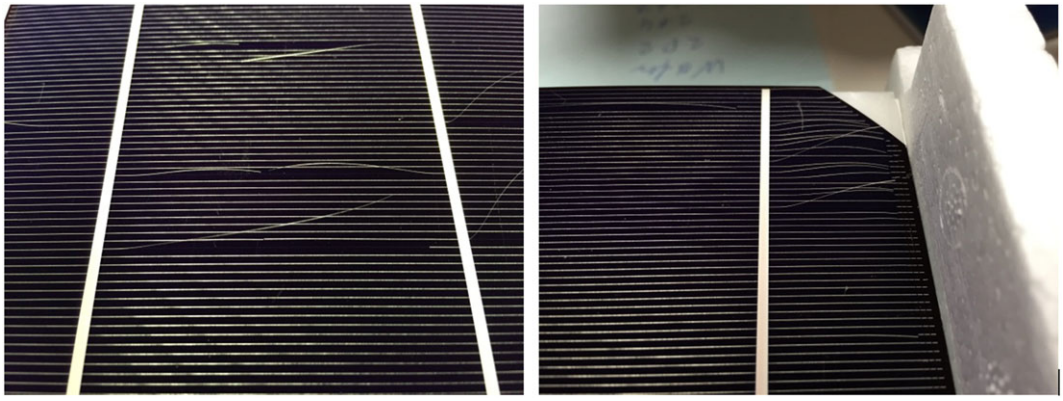

FIGURE 17 Examples of poor plated finger adhesion whilst busbar adhesion remained sufficient for cell interconnection [Colour figure can be viewed at wileyonlinelibrary.com]

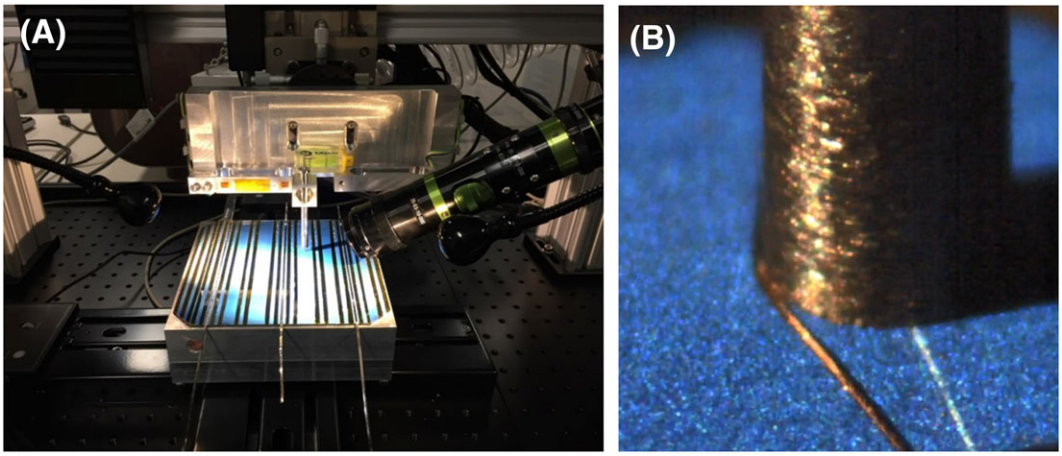

FIGURE 18 A, Finger adhesion testing tool guided by the design of Young et al[240] and enhanced by the incorporation of a camera to record video of all the finger impacts; and B, close-up image of a stylus dislodging a Ni/Cu plated finger from a laser-ablated contact region on a Si solar cell [Colour figure can be viewed at wileyonlinelibrary.com]

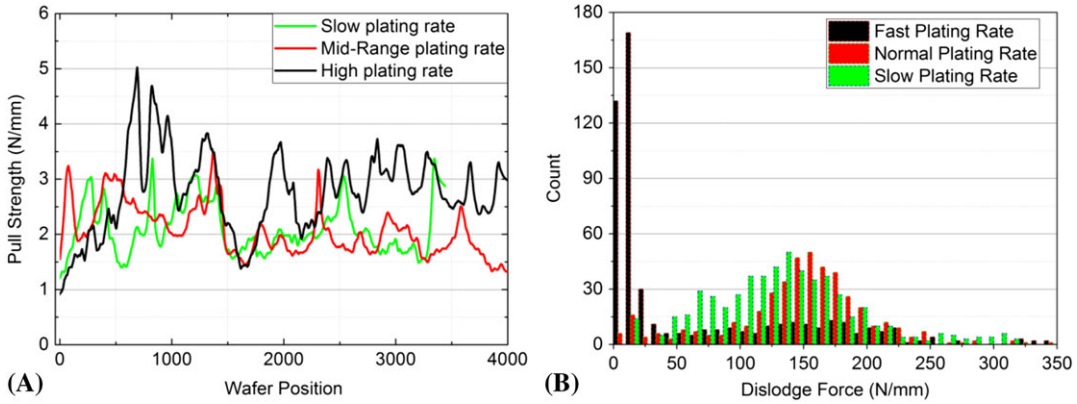

FIGURE 19 A, Busbar pull forces measured for industrial cells Cu-plated at different rates; and B, finger dislodgement forces measured for the same cells. All plating rates were within the recommended range of the proprietary plating electrolyte used (reproduced with permission from Wang[238]) [Colour figure can be viewed at wileyonlinelibrary.com]

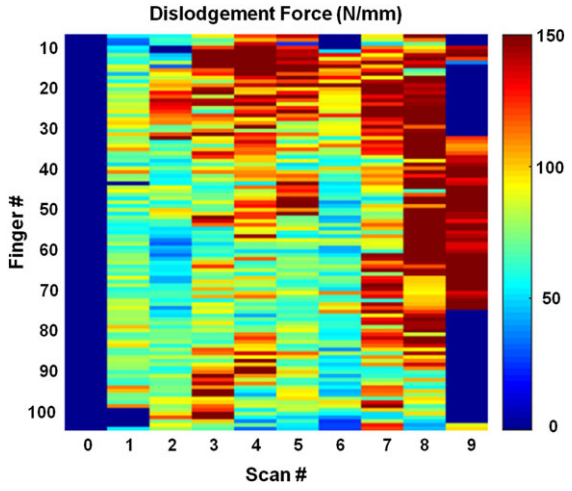

FIGURE 20 A map of finger dislodgement force over a 5 busbar 156 mm Ni/Cu/Ag plated p-type PERC solar cell showing large variations in finger adhesion that may arise due to variability in the cell precursors (eg, SiN_x ARC) thickness, laser ablation, plating and post-plating annealing processes [Colour figure can be viewed at wileyonlinelibrary.com]

contact regions. However, countered with these advantages is the complexity introduced by the different Ni silicide phases and the poorer thermal stability of the desirable NiSi phase in post silicide thermal steps. The properties of the silicides depend on the surface preparation,[246,247] and so given the rough and heterogeneous nature of ps-laser ablated Si surfaces, it is reasonable to assume that Ni silicide formation may not be uniform across the Si surface exposed by laser ablation. Although the number of processing steps can be reduced by annealing after all plating steps have been performed (see Figure 22), the simpler process allows for less control over the silicide formation than possible with the process used by BP Solar (see Figure 21). However, very little analysis and optimisation have been performed with regard to the formation of Ni silicides in the presence of an overlying Cu/Ag stack and the results of Hsiao et al[184,248] would suggest that it may be timely to investigate how the Ni silicide phases form for different surface pre-treatments and annealing conditions, and correlate these findings with contact adhesion for both busbars and fingers.

Another way to achieve a more reliable Cu plating process is to remove the complication of having busbars on the cells by using a

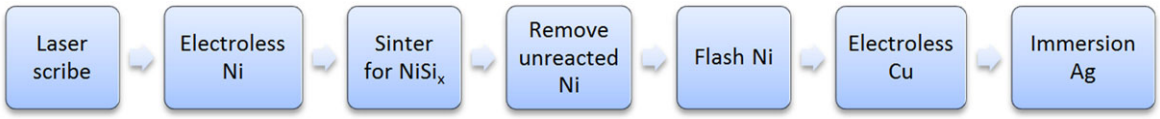

FIGURE 21 Electroless plating process flow that was used by BP Solar (based on that developed by Motorola) [Colour figure can be viewed at wileyonlinelibrary.com]

wire-based cell interconnection method.[249-253] As mentioned earlier in this section, the presence of busbars as well as fingers in the grid pattern can result in a non-uniform plating rate across the cell that can be difficult to control.[223,236] Use of a wire-based interconnection scheme can also reduce the required cross-sectional area and hence height of the plated fingers. This can result in improved finger adherence to the Si. Although costs for these wire-based schemes may currently be greater than soldered interconnection, the balance of costs may shift with Cu-plated cell metallisation, especially once more field studies have confirmed the reliability of wire-based schemes.

2.2.3 | Metal contact integrity

As early as 1983, possible problems associated with the Ni/Cu metallisation system were documented in the proceedings of a meeting discussing metallisation systems for flat plate arrays.[49] Concern was raised that the Ni/Cu system was unstable because Ni and Cu form a solid solution. The ease at which Ni and Cu intermix (or form a solid substitutional solution) arises from the fact that both metals crystallise in a face-centred cubic structure have similar ionic radii, electronegativities, and valences.[254] However, there was uncertainty regarding the impact of this fundamental instability as Motorola had previously reported that their electroless Ni/Cu metallisation was stable for a period of 20 years (assuming 6 hours at 60°C).

As discussed in Section 2.1.1, Colwell et al have shown that Cu can penetrate through Ag capping layers in unencapsulated cells.[139] This result appears to support the earlier concerns about Cu interdiffusion and raises concern about what may occur in a module. If Cu does penetrate through Ag capping layers in modules (which has not been observed to-date to the authors' knowledge), then it would be expected that it may react with acetic acid arising from EVA degradation and impact module lifetime. However, further research is required to understand the conditions under which Cu/Ag interdiffusion may occur. This research may also inform as to whether the Ag can be safely replaced by Sn in capping layers to further reduce costs.

In early studies at IBM, it was shown that the microstructure of electroplated Cu can change dramatically in the hours following deposition at room temperature.[255] The changes can result in increases in grain size, changes in preferred crystallographic texture and reductions in resistivity, hardness, and compressive stress. Song et al have reported similar changes with Cu deposited on solar cells using LIP.[256,257] Although the changes in resistivity that can occur during self-annealing[255,256] are not expected to impact the performance of Cu-plated Si solar cells as much as they could impact ICs, the evolution in grain size may have implications for metal inter-diffusion and module aging. The Cu plating processes used by BP Solar and Suntech did not employ a post-annealing step, and so it is possible that the cell metallisation may not have completely self-annealed by the time the cells were interconnected and encapsulated into modules. Consequently, the Cu microstructure evolution with time may have depended on the thermal cycling history of modules in the field. Song et al showed that by performing short anneals at ~350°C after Cu LIP, large Cu grains result and variations in microstructure due to different self-annealing processes can be effectively eliminated.[256,257]This suggests that annealing after plating may reduce variability in module aging in the field.

When IEC tests are performed on modules, the design (quality) criterion is that the module power reduction must be <5%. However, this test result does not inform on how the module components may be aging. Phua et al showed using cross-sectional imaging that in Cu-plated n-type PERT modules subjected to 200 thermal cycles, Cu could penetrate the Ni barrier layer to be found at the Si-Ni interface under some conditions.[258] Although it was hypothesised that the driving force for the observed diffusion of Cu may have been poor adhesion of the plated fingers resulting in a surface that permitted Cu precipitation, further investigations are required to confirm this. This report highlights the importance of investigating the underlying physical and chemical reasons for failures that occur during environmental testing in order to understand and address limitations of metallisation solutions. Not only can these analyses lead to increased module lifetime (and hence reduce the LCOE), increased confidence in module durability can increase the bankability of a Cu-plated metallisation technology.[259,260]

It should also be noted in this discussion that screen-printed Ag metallisation can also corrode/or degrade with time in PV modules. Discolouration of cell surfaces due Ag grid corrosion, commonly referred to as 'snail trails' or 'snail tracks',[261,262] can occur due to a number of different degradation mechanisms depending on the additives used in pastes and the way the modules have been encapsulated.[263] Additionally, loss of adhesion of screen-printed Ag contacts due to reactions with acetic acid (from EVA) has been observed after damp heat testing of modules.[264] Copper plating results in effectively a pure polycrystalline metal, and consequently reactions that occur due to the presence of other elements arising from additives in pastes are not of concern. Additionally, although the tensile strength of plated Cu fingers can contribute to finger peeling if plating is not well controlled (as discussed in Section 2.2.2), finger breakage is not expected for Cu-plated fingers with finger widths <20 μm. This increased strength may result in increased resilience to wafer cracking, a very common problem being experienced with current PV modules.[265-269] Although reducing wafer thickness has helped to reduce costs,[270] it has resulted in wafers being more prone to cracking in modules.[265] The cracks may not be immediately evident or deleterious to module performance, but with thermal cycling, fingers overlying the cracks can break and reduce current collection in the module. Consequently, with future increases in efficiency assuming further

FIGURE 22 Process flow when using a UV ps laser to ablate the ARC for contact openings. This process allows for the sintering step to be performed after all plating (wet) steps [Colour figure can be viewed at wileyonlinelibrary.com]

reductions in metal finger width to reduce shading, polycrystalline Cu plated conductors may present some advantages over the more heterogeneous screen-printed Ag conductors.

The above differences in metallurgy between Ag screen-printed and Cu-plated modules also suggest that different (or additional) qualification tests may be needed for Cu-plated modules. The current IEC 61215 tests for crystalline Si modules have been developed largely assuming Ag screen-printed metallisation, where concerns of grain boundary interdiffusion and self-annealing are not relevant. New qualification tests could be designed to test for plated contact adhesion, contact integrity, LID, and potential-induced degradation.

2.3 | Availability of cost-effective processes and equipment

An economically viable Cu plating process for Si PV requires that cost-effective processes and equipment are available for manufacturers. Section 2.3.1 reviews the availability and complexity of the required plating processes, and then in Section 2.3.2 we consider the important problem of plating (metal) waste treatment. Finally, Section 2.3.3 reviews the requirements and availability of plating equipment for the PV application and considers their functionality compared with equipment that is available to the IC industry.

2.3.1 | Plating processes

Figure 21 summarises the process that was developed by Motorola and used by BP Solar in the production of their LBG Si solar cells. An undesirable feature of this process was that it required wafers to be dried after the Ni plating step in order to be sintered for silicide formation. Additionally, the large number of wet chemical steps necessitated large volumes of rinse water that was expensive to be treated. BP Solar ceased their production of Saturn modules due to the cell production cost no longer being competitive compared with screen-printed cells despite using Cu rather than Ag. Essentially the same process flow was used by Suntech in the manufacture of their Pluto cells, with the exception that a CW laser was used to both open the dielectric and selectively dope the underlying Si and LIP was used in place of electroless plating.[46,59] Although the use of laser-doping instead of the two-step diffusion process of the LBG cells reduced process complexity, it was still necessary to sinter the Ni after plating to improve contact adhesion, thereby retaining the wet-dry-wet processing sequence.[186]

The use of UV ps lasers to open the dielectric has enabled more adhesive contacts to be formed by plating (see Section 2.2.2). This has made it possible to perform the sintering step after all the wet chemical steps (see Figure 22). Although this process has reduced the complexity significantly, a key limitation is that additional processing steps are necessary if a SE is required. Hsiao et al reported the successful alignment of ps laser-ablated openings (and subsequent Ni/Cu/Ag plating) in heavily-doped emitter regions[‡], but the resulting SE PERC cells required additional pre-processing to form the pattern of heavy and light diffusions.[248] Ideally, what is required is a way in which a SE can be fabricated with the adhesive properties introduced through the use of a ps laser for contact openings.

As the industry moves to introduce new cell structures such as bifacial cells and cells employing doped passivated contacts, new plating processes will be required. Bifacial module technology is expected to comprise ~40% of the market by 2028.[1] However, one-step plating of bifacial cells requires the formation of a seed layer on the exposed device contact regions on both wafer surfaces before the plating of Cu on both wafer surfaces. This seed layer followed by Cu plating process has resulted in industrial-sized bifacial Si heterojunction cells with efficiencies exceeding 23%.[271,272] Although PVD methods can be used to form this seed layer, they are typically expensive, and so direct plating of a seed metal is desirable. Cornagliotti et al have reported the use of electroless plating of a Ni seed layer to both n- and p-type (diffused) Si after a proprietary sensitisation process[12] to achieve bifacially-plated Ni/Ag busbar-less n-PERT cells[§] with an efficiency of 22.8%.[9]

An alternative bifacial cell plating process, which used a combination of LIP and forward-bias plating,[273,274] was demonstrated by Wang et al.[275] They used a 'soft' carbon electrode to electrically contact Si exposed through the laser openings, thereby allowing direct plating of Ni to both n-type and p-type Si on bifacially-passivated solar cells.[275,276] This combination of LIP and forward-bias plating can eliminate the requirement to use electroless plating processes (which are typically more complex to control) and has been used to plated bifacial Si heterojunction cells without the requirement to form a PVD seed metal layer.[277]

Cell designs employing doped polySi passivated contacts[278-283] also present challenges with regard to metallisation. Silver pastes that have been developed for fire-through contacts can damage the passivation provided by the doped polySi layers.[284] Consequently, metallisation of this newer cell technology will require the development of new processes and/or pastes. However, the use of doped polySi passivated contacts may present a new opportunity for plated Cu contacts as Cu plating can be performed at room temperature and therefore is not expected to impact the polySi passivation. Another interesting opportunity may be to utilise the polySi as a sacrificial diffusion barrier for plated Cu. Metal gettering by doped polySi layers was reported in the 1990s,[285,286] and it has been more recently recognised by Si PV engineers that gettering by the doped polySi could contribute to the record high efficiencies being achieved by Si

[‡]Busbar openings of width 0.8 mm were aligned within heavily-doped regions of width 0.9 mm and 13-μm-wide finger openings were aligned within heavily-doped regions of width 200 μm.

[§]The efficiency of the busbar-less cells was measured using Grid^{TOUCH} and a back chuck with low reflectance. The cell *FF* was corrected for the voltage drop between the Grid^{TOUCH} *V* and *I* wires.

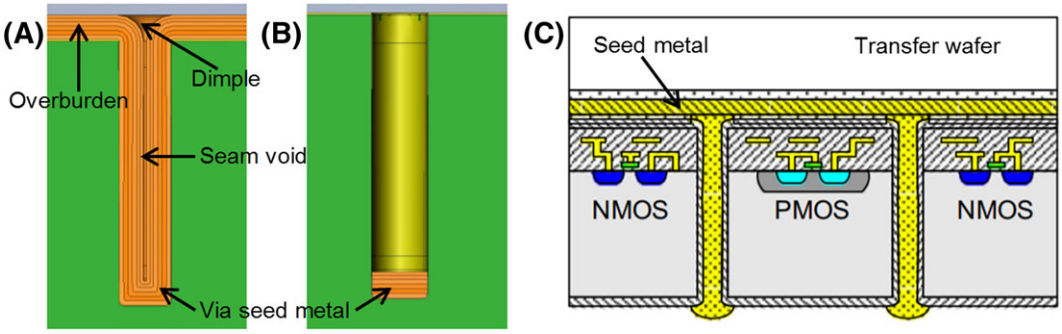

FIGURE 23 Schematics showing: A, conformal plating; and B, bottom-up plating, of a blind via. C, Shows an example of bottom-up through-wafer plating where a transfer wafer is used to deliver the current to the surfaces to be plated and the electrolyte penetrates from the other wafer surface (adapted from Song et al[304]) [Colour figure can be viewed at wileyonlinelibrary.com]

solar cells employing these passivated contact layers.[282] New cell designs which rely on doped polySi layers resisting Cu diffusion by grain boundary saturation may be possible. In other words, using the language of diffusion barriers, the polySi layer may act both as a carrier-selective contact and a 'stuffed' diffusion barrier for Cu. Therefore, Cu plating directly to polySi may address the concern of Cu penetration through plated Ni seed layers as well as presenting a viable option for metallising cells with passivated contacts.

2.3.2 | Plating waste treatment

Rinsing/spraying steps, employed to reduce drag-out as wafers move from one plating electrolyte to another, create metal-contaminated waste water. Although Cu is an abundant metal that is naturally found in all bodies of water and is an essential nutrient for plant and animal life, concentrations as low as 5 to 10 ppb can cause toxic effects such as reduced growth, photosynthesis in algae or teratogenic effects in sensitive species of fish or amphibians.[287] For this reason, levels of Cu in effluent waste water from manufacturing must be monitored and the effluent treated if allowed levels are exceeded. In the US, manufacturing facilities can either directly discharge their treated waste into a water body or discharge to a treatment facility (indirect discharge). In the former case, the discharged Cu limit is periodically updated by the National Pollutant Discharge Elimination System, the allowable limit being revised to ensure that the pollutant load remains below the total maximum daily load in water body (typically ~1 ppb). In the case of indirect discharge, local limits for manufacturers discharging to a treatment plant vary depending on the treatment plant, but are typically in the order of 1 ppm.[288,289] In China, whilst Cu concentrations of 1 ppm were tolerated in existing electroplating fabrication plants before 2010, emissions are now limited to 500 ppb, or 300 ppb in environmentally sensitive regions.[290] The move towards the proposed 'Plating Industrial Parks' in China, where Cu-contaminated waste water can be treated and monitored more closely, resembles the 'indirect discharge' arrangement already well-established in the US. It may, however, present some problems for PV manufacturing if partly-processed wafers have to be transported to these parks for metallisation, as wafer scratching can result in overplating.

However, irrespective of whether local or centralised monitoring is performed, metal contaminants need to be removed from the waste water. Various physical-chemical techniques can be used to remove metals from waste water, including precipitation, evaporation, coagulation-flocculation, ion-exchange, absorbents, biological processes, and electrowinning.[291-295] Many of these processes result in a solid 'sludge', the chemical content of which depends on the processes involved. Historically, Cu electroplating waste from IC manufacturing in the US has been classified as an F-006 hazardous waste according to the US 40 CFR 261.31 regulation,[296] meaning that any sludge resulting from treated waste water must be recycled rather than disposed of in landfill. However, cases have recently been put to the EPA, that the F-006 classification is based on older plating processes which used toxic elements (eg, cyanides) and therefore should not apply to current Cu interconnect electroplating processes where these chemicals are no longer used.[297,298] Furthermore, sludge resulting from electroplating waste water contains far lower Cu concentrations than that arising from the chemical mechanical polishing (CMP) process used for Cu removal at every IC level.[289,297]

Like the current electroplating processes used for IC manufacturing, the PV plating waste water would not contain toxic and hazardous

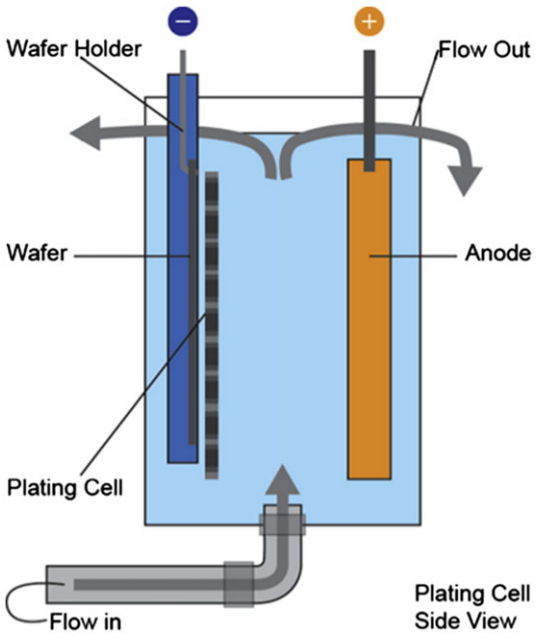

FIGURE 24 Wafer holder showing the use of shear plates to provide diffusion boundary control (from Gambino et al[33]) [Colour figure can be viewed at wileyonlinelibrary.com]

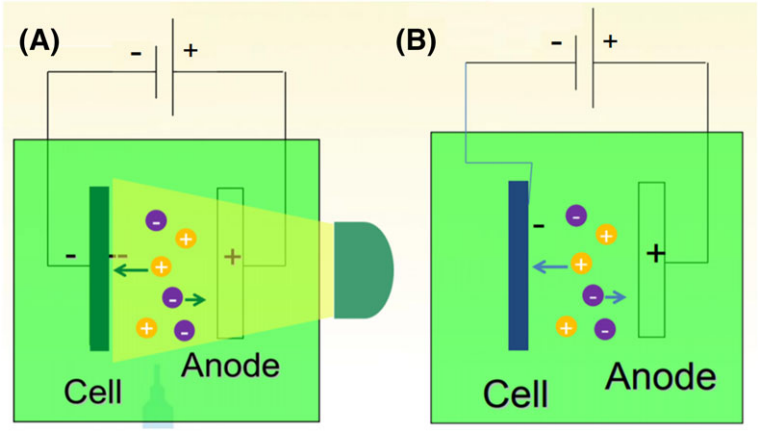

FIGURE 25 Solar cell plating line configured to achieve: A, LIP; and B, electroplating. In A, electrode contact is made to the rear of the wafer to apply a bias current to offset the resistances in the electrochemical circuit. In B, the electrode contacts a seed layer on the wafer surface (reproduced with permission from Meco Equipment Engineers BV) [Colour figure can be viewed at wileyonlinelibrary.com]

chemicals such as cyanide, as no plating companies to our knowledge are proposing the use of cyanide-based chemistry for PV. Rinse water would typically contain low concentrations of Ni and/or Cu and very low concentrations of other elements (eg, C, S, and B) due to plating additives. Furthermore, the Ni and Cu rinse waters can be readily separated on site allowing for effective recycling. This allows for low-cost methods such as evaporation to be used for PV waste treatment, with the resulting metal solid content being recycled. Electrolytic recovery or electrowinning (after initial metal concentration processes) may present an attractive option for PV plating waste as high quality Cu anodes can be obtained from Cu plating waste.[291]

Consequently, although the cost of treating and disposing of PV plating waste has been frequently muted as a barrier to the update of plating technology, it is likely that metal treatment facilities such as have been established already in the US will need to be established in China to support not only a growing PV industry but also a growing electronics industry. Opportunities may indeed exist for companies establishing new metal treatment facilities to use 'cleaner' metal reclamation processes that utilise the low-cost electricity that PV can provide. A balanced discussion about waste management probably also should consider the comparative challenges of disposing of waste Ag pastes with additives such as Pb in the light of Terawatt production levels.

2.3.3 | Equipment availability and functionality

Interconnect and TSV electroplating of wafers for IC applications have generally been achieved using single wafer plating tools. The requirements for the plating process are as follows: (1) void-free interconnects/vias; (2) small overburden (Cu that must be removed using the CMP process[24,25]); and (3) fast plating times.[299] Additives are typically used to achieve (1) and (2) and will not be discussed here because of the many other reports on additives for interconnect and TSV electroplating.[300,301] Additionally, many additives are the proprietary knowledge of providers of electroplating services.

Whereas Cu electroplating of interconnects for earlier IC devices involved trench (blind via) conformal plating using damascene chemistry,[18] bottom-up plating approaches are being developed for the high aspect ratio TSVs required for 3D-IC applications[302-306] (see Figure 23). Bottom-up plating makes it easier to achieve void-free[184] interconnectors and allows higher aspect ratio structures to be formed.[305] It can also reduce the overburden, hence Cu wastage and CMP time[307] and allow the use of through-wafer (one-side) plating.[302]

Dual damascene plating is typically performed by placing the wafer in a vertical fluid flow ('fountain') and the hydrodynamic boundary layer thickness on the wafer surface[308] (typically ~50 μm) is determined by the rotation speed of the wafer relative to the fluid.[33] A similar plating tool has been used for LIP of solar cells (Suncup® solar cell plating tool developed by NB Technologies[¶]). Copper electroplating of TSVs requires reduced boundary layer thickness, and so wafers are usually plated using single or dual wafer handling fixtures (or holders) that are moved from tank to tank in a vertical direction using high levels of automation.[309] The holders typically include shear-plates (or similar technology) that can prevent thick hydrodynamic boundary layers from forming on the surface of the wafer (s) by directing the flow of electrolyte through a series of flow shaping elements (see Figure 24).[33,308-310]

The vertically transported arrangement used by the IC industry has also been adapted for Si solar cell plating,[311] though to reduce cost, wafers are suspended in the baths using a number of clips rather than being loaded into individual holders. Solar cell plating lines can be configured to perform LIP or electroplating as illustrated in Figure 25, the latter requiring a seed layer to which the electrode can be contacted. In the plating line supplied by Meco,[7] the rear side of the wafer (screen-printed Al for most p-type industrially-produced cells) is also exposed to the plating electrolyte. The cathodic potential applied to the rear surface acts to minimise Al corrosion. However, it can be challenging to totally eliminate Al oxidation and dissolution and so some contamination of the plating electrolyte with Al is expected. An important consideration for this solar cell plating approach is that the wafer is fully dried before encapsulation as any residual moisture may impact the durability of modules. High processing throughput can be achieved by duplicating lines, as is routinely done for screen-printing production lines for Si PV.

Another approach which has been developed for the plating of Si solar cells is to adapt the belt-based multi-lane transport systems used by the Si PV industry to perform chemical etching and texturing to perform multi-lane plating.[4,6,312] This multi-lane approach can enable wafer plating rates of up to 3200 wafers per hour and low costs.[6] It

[¶]http://www.nb-technologies.de/en/products/labtools/suncupR-smart-plating.html

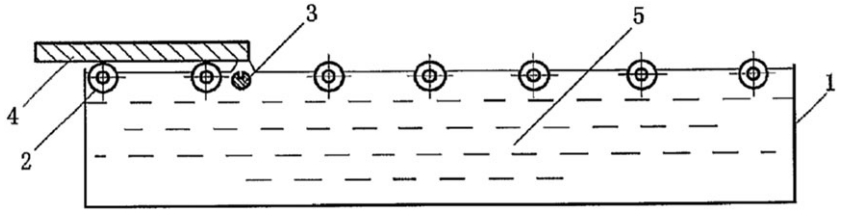

FIGURE 26 Method for wetting the surface of the wafer to be plated whilst minimising wetting of the rear Si wafer surface. 1 = plating bath, 2 = transport roller, 3 = jet for wetting wafer surface, 4 = Si solar cell, and 5 = electrolyte (from Ji et al[313])

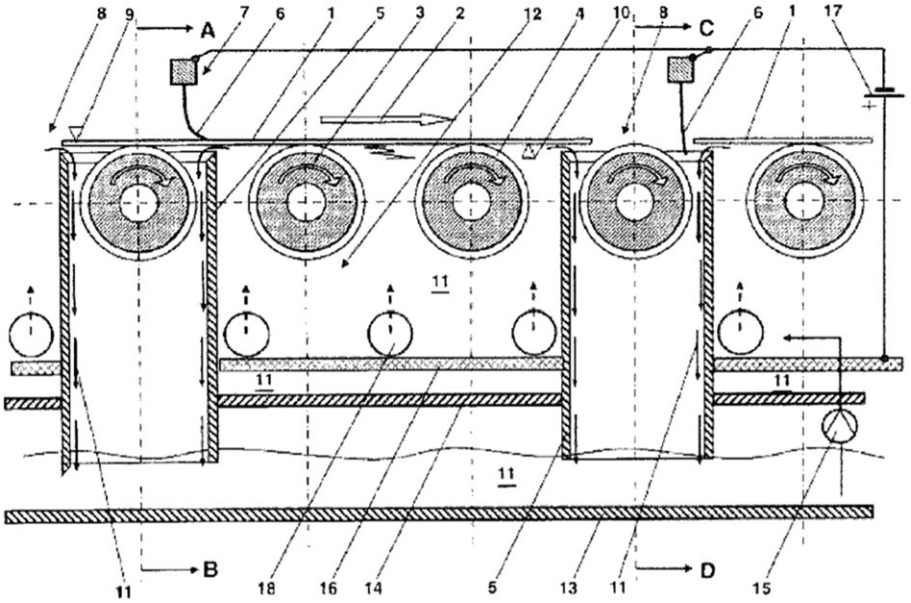

FIGURE 27 Schematic showing horizontal transport of Si wafer solar cells through a plating bath showing electrolyte flow arrangements that minimise rear surface wetting (numbering is detailed in Gutekunst[314])

also allows for the rear surface to be kept largely dry and thereby eliminates concerns about moisture carried over into modules. However, with the solar cell conveyor belt design, it is difficult to provide the same level of boundary layer control as provided by IC plating equipment. It is also challenging to completely prevent electrolyte from wetting the rear surfaces of wafers. Although engineering strategies have been employed to minimise rear surface wetting (eg, see Figure 26),[313] this can be difficult to achieve without incurring the cost of carrying a thick boundary layer on the surface of the wafer and hence limiting precise control of the electrodeposition process. Another approach to address the problem of keeping the rear solar cell surface dry whilst providing a uniform electrochemical environment at the front-surface of the solar cell has been proposed by Rena GmbH (see Figure 27).[314] In this arrangement, electrolyte is constrained to regions which are covered by wafers and so the risk of overlapping on the rear is reduced. This arrangement is also expected to provide benefits in terms of a more uniform boundary layer over the solar cell surface, although probably not to the extent required for TSV electroplating.

In summary, although the requirements for fast processing throughput and low cost have inspired new equipment designs for the plating of Si wafer-based solar cells and equipment now exists for manufacturers to purchase equipment for large-scale production, the resulting tools typically provide reduced control of the hydrodynamics. Consequently, the electrodeposition process on Si solar cells in a production environment is generally not as precisely controlled at the wafer surface as it is with plating equipment developed for IC Cu plating. This limited process control may contribute to variable solar cell plating. If cell metallisation designs continue to require the typical H-bar cell pattern comprising busbars and fingers, then solar cell plating equipment may benefit from providing a more controlled electrochemical environment at the Si surfaces to be plated.

3 | CONCLUSIONS

Copper-plated interconnects were widely adopted for volume manufacture of Si IC interconnects after more than a decade of intensive research to demonstrate that the use of Cu would not decrease the reliability of devices. This adoption was driven by the significant technological advantages that Cu interconnects provided over the previously-used Al in terms of increased conductivity and improved resistance to electromigration. However, although Cu-plated cell-level metallisation promises significantly reduced metallisation costs for Si PV compared with the existing screen-printed Ag, its adoption in large-scale manufacture has been limited. This review explored some of the key challenges facing Cu-plated metallisation for Si PV, drawing insights from the technology pathway that paved the way for the introduction of Cu-plated interconnects for VLSI circuits.

It is proposed that the different technology pathways for Cu-plated interconnects for IC and Cu plating for Si PV arise essentially from differences in scale and field operation conditions. The larger width of the Cu-plated fingers on solar cells compared with the diameter of the lower-level Cu-plated interconnects, and the fact that Cu would be replacing Ag in Si PV (Ag being both conductive and highly resistant to corrosion) reduces to a large extent the technological advantages of using Cu in the place of Ag. Additionally, Si PV metallisation presents some new challenges. The rough, textured surfaces of Si solar cells and the tight price constraints of Si PV have made it difficult to use IC processes for Cu diffusion barriers for solar cells. This has led to the use of plated Ni barrier layers rather than PVD-deposited metal alloys, despite concerns that Cu may penetrate through these layers. Although not studied as extensively for Si PV, Cu contamination may be a more significant problem for the PV application than for IC devices, due to the need to reduce Cu concentrations below threshold levels through the entire thickness of the Si wafer. In addition, light absorption may introduce new recombination-active defects and/or increase Cu precipitation causing LID of modules in the field. Given the increased understanding of the requirement of low levels of deleterious impurities, such as Cu, for industrial cells to approach the efficiencies that have been reported in laboratories, it may be time to reconsider the approaches that have been used to date to prevent Cu ingress into the Si wafer from plated cells. New barrier layers will need to be of uniform thickness across the contact area, with amorphous barrier materials presenting potentially more reliable Cu diffusion barrier properties than the polycrystalline barrier materials currently being used.

As the power generation from large PV installations will need to be accurately predicted to address new grid integration challenges, the reliability of Si PV modules is expected to come under greater scrutiny. Device reliability has been critical for ICs with devices required to have very low failure rates. This has resulted in high levels of investment which has not been paralleled for Si PV, where reliability has not been as extensively studied. Two aspects of reliability were considered in this review. First, the arrangement of unsupported high aspect ratio conductors across a Si solar cell surface presents a challenge for plated contact adhesion, which can be made even more challenging if LIP rates are not well controlled across the surface of a solar cell. Adoption of a plated-Cu metallisation process will require metrology tools to measure both finger and busbar adhesion to ensure reliable metallisation. However, perhaps a superior solution for Cu-plated solar cell metallisation may be to transition to busbar-less interconnection methods thereby eliminating the difficulties introduced by non-uniform plating rates at busbars and fingers and allowing for less complex plating equipment. A second reliability concern is the need to increase our understanding of the PoF of metallisation systems for PV modules. For plated contacts which involve metal stacks, metal interdiffusion under field conditions and its impact on contact integrity need to be better understood. The previously-mentioned challenges become even more difficult to address due to the requirement for PV modules to operate in the field in a wide range of environments for 25+ years.

With the scale of Si PV manufacturing expected to increase dramatically over the next decades to provide the world with a sustainable source of electricity, the financial advantages of using a metal other than Ag for solar cell contacts will become even more important. Currently, Ag is ~80 times the cost of Cu on a per weight basis. Consequently, a transition from Ag to Cu metallisation with this material cost differential, extrapolated to 5 to 10-GW production levels for PV manufacturers, represents a potentially large financial saving and a reduced drain on the world's Ag resources. In 2018, it is estimated that the Si PV industry will consume ~ 146 MOz, or > 4000 tonne of Ag,[315] and will continue to consume a larger proportion of this precious metal with the forecasted Terawatt manufacturing capacity.[316]

Although the real cost advantage of transitioning to Cu metallisation will depend on the costs of processes and equipment required, this was also true for the IC industry as they transitioned from Al to Cu interconnects. However, the IC industry invested billions of dollars in the research and development of manufacturing equipment and the patterning, polishing, and plating processes that were required to enable Cu-plated interconnects. This is in contrast to the relatively modest investment in processes and equipment for Cu-plating of Si solar cells. Investment is required in manufacturing equipment, and further research is needed to more effectively test for Cu ingress in solar cells under different conditions, form effective diffusion barriers and/or gettering strategies to prevent Cu-induced device degradation, characterise metal-related reliability issues, and to develop more quantitative reliability metrics. Further confidence in Cu metallisation would also be assisted by research aimed at realising the often-suggested efficiency potential and advantages of Cu-plated cells and demonstrating the potential reliability advantages (eg, reduced finger breaks, greater resistance to damp heat) of Cu-plated modules.

ACKNOWLEDGEMENTS

This work has been supported by the Australian Research Council (ARC) through grants LP100100712 and FT170100447 and by the Australian Renewable Energy Agency (ARENA) through the RND 2014/RND002 grant. Alison Lennon and Jack Colwell acknowledge the support of the Australian Government through their Future Fellowship and Research Training Program Scholarship, respectively. Ning Song, Pei-Chieh Hsiao, and Xiaowei Shen are thanked for provision of TEM and SEM images used in the manuscript. Pierre Verlinden is thanked for his advice and assistance with proof-reading the manuscript. The authors would like to acknowledge the suggestions and advice of Sarah Kurtz, especially with regard to the sections on PV module reliability, Robert Dumbrell for his review of the sections on contact recombination, and Damian Pysch, Martijn Zweigers, Yuan Shengzhao, and Chen Yifeng for their advice on plating waste management.

The Australian Government, through ARENA, is supporting Australian research and development in solar PV and solar thermal technologies to help solar power become cost competitive with other energy sources. The views expressed herein are not necessarily the views of the Australian Government, and the Australian Government does not accept responsibility for any information or advice contained herein.

ORCID

Alison Lennon http://orcid.org/0000-0002-9166-7171

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How to cite this article: Lennon A, Colwell J, Rodbell KP. Challenges facing copper-plated metallisation for silicon photovoltaics: Insights from integrated circuit technology development. *Prog Photovolt Res Appl*. 2019;27:67–97. https://doi.org/10.1002/pip.3062