A study of process-related electrical defects in SOI lateral bipolar transistors fabricated by ion implantation

J.-B. Yau, J. Cai, P. Hashemi, K. Balakrishnan, C. D'Emic, and T. H. Ning
IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York 10598, USA

(Received 22 August 2017; accepted 22 October 2017; published online 6 November 2017)

We report a systematic study of process-related electrical defects in symmetric lateral NPN transistors on silicon-on-insulator (SOI) fabricated using ion implantation for all the doped regions. A primary objective of this study is to see if pipe defects (emitter-collector shorts caused by locally enhanced dopant diffusion) are a show stopper for such bipolar technology. Measurements of I_C-V_{CE} and Gummel currents in parallel-connected transistor chains as a function of post-fabrication rapid thermal anneal cycles allow several process-related electrical defects to be identified. They include defective emitter-base and collector-base diodes, pipe defects, and defects associated with a dopant-deficient region in an extrinsic base adjacent its intrinsic base. There is no evidence of pipe defects being a major concern in SOI lateral bipolar transistors. *Published by AIP Publishing*. https://doi.org/10.1063/1.5001203

I. INTRODUCTION

While CMOS completely dominates applications in the digital domain, bipolar transistors are certainly superior to CMOS for many non-digital applications. For example, for RF applications, state-of-the-art SiGe-base bipolar transistors can reach $f_{max} > 350$ GHz.[1] For sensor applications, bipolar transistors are superior to field-effect transistors due to low noise and their collector currents having a 60 mV/decade behavior.[2,3] In the development of a bipolar technology, it is critically important to reduce "pipes" or emitter-collector shorts caused by locally enhanced diffusion of emitter dopants into the base region.[4,5]

Commercially available advanced bipolar transistors, such as those in Refs. 1–3, are vertical transistors, with current flowing from the emitter vertically down through the base to the collector. These transistors typically employ a polysilicon-emitter process which, after emitter polysilicon deposition, involves relatively low thermal cycles and hence are not prone to have problems with pipe defects.

In recent years, there were several reported studies of Silicon-on-Insulator (SOI) symmetric lateral bipolar junction transistors (LBJTs) (Fig. 1) where the current flows from the emitter laterally parallel to the silicon-oxide interface through the base to the collector.[6,7] Unlike a vertical transistor, a lateral transistor does not suffer from the base-push-out effect (Kirk effect) because its collector doping concentration is larger than its base doping concentration. It has inherently small collector capacitance because its base-collector junction area is the same as its base-emitter junction. Model calculations suggest that f_T and f_{max} of a lateral transistor can be much higher than those of state-of-the-art vertical transistors.[8] Furthermore, lateral bipolar transistors are CMOS compatible in the fabrication process and layout densely just like CMOS, suggesting them to be much lower cost than vertical bipolar transistors.

The simplest process, and hence the method of the lowest cost, for fabricating SOI LBJT is to use ion implantation to form all the doped regions. Post-implant thermal annealing temperatures are typically around 1000 °C. With emitter-collector separation of less than 100 nm, needed to achieve $f_{max} > 500$ GHz,[8] there is a concern of pipe defects in LBJT fabricated by ion implantation, caused by a combination of residual implant damage and localized enhanced diffusion of dopants into the base from both the emitter and the collector regions.

In this paper, we report a systematic study of possible concerns of pipe defects in SOI lateral NPN bipolar transistors fabricated using high-dose boron implantation to form the extrinsic base and high-dose arsenic implantation to form the emitter and collector regions. The goal was to determine if pipe defects are a show stopper for such a technology. The methodology of the study is described, and some subtle but interesting device physics associated with the device fabrication process is discussed.

II. TEST-SITE DESIGN FOR THE PIPE DEFECT STUDY

To obtain meaningful statistics in the characterization of pipe defects, a special device test-site was designed which enables detection of pipe defects in SOI lateral bipolar transistors through testing arrays of parallel chains of devices. The array sizes are 1-device, 10-device, 100-device, 1000-device, and 10 000-device. At the mask level, the nominal emitter-collector spacings (L_{DES}) are 60 nm, 70 nm, 80 nm, and 90 nm. For each L_{DES}, there are two device widths (W_{DES}), one at 0.5 μm and one at 1.0 μm. Examples of the layout of a 100-device array and the corresponding individual transistor therein are shown in Figs. 2(a) and 2(b), respectively. Each location where the meandering (green) base region crosses the mesh-like emitter-collector arrays corresponds to one single transistor. On a 200 mm SOI wafer, there are 25 chips, where each chip contains 2 identical copies of the above five groups of parallel connected transistor arrays for each combination of L_{DES} and W_{DES}. Thus, for each combination of L_{DES} and W_{DES}, there are a

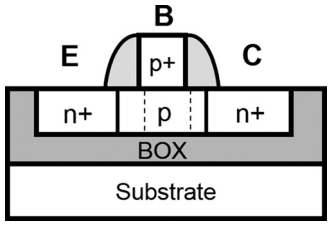

FIG. 1. Schematic illustrating the structure of an SOI lateral NPN bipolar transistor with symmetric emitter and collector regions. The quasi-neutral base (marked between the dashed lines) is narrower than the physical E-C separation by the depletion layers from both E and C sides (After Ref. 6).

total of 55 550 transistors per wafer available for testing. Figure 2(c) shows a schematic that depicts an emitter-to-collector short due to locally enhanced dopant diffusion (pipe defect). The circuit diagram for parallel chains of m transistors is illustrated in Fig. 2(d), where r_{bn} is the base resistance of the nth transistor. The voltages that govern the operation of the nth transistor in a parallel chain of m transistors are listed below in Eqs. (1)–(3) and will be reviewed in detail later in the analysis of the measurement technique and the observed excess currents due to process-related defects. In Eqs. (1) to (3), V_E, V_B, and V_C are the voltages, relative to the ground, applied to the emitter, base, and collector terminals, respectively, of the transistor chain. V'_{Bn}, V'_{BEn}, and V'_{BCn} are the internal base voltage relative to the ground, base-emitter junction voltage, and base-collector junction voltage, respectively, of the nth transistor in the parallel chain. I_{Bn} is the base current of the nth transistor. The base and collector currents of the nth transistors are determined by its internal voltages V'_{BEn} and V'_{BCn}.

$$V'_{Bn} = V_B - r_{b1}\sum_{i=1}^{m} I_{Bi} - \cdots - r_{bn}\sum_{i=n}^{m} I_{Bi} - \cdots - r_{bm} I_{Bm}, \quad (1)$$

$$V'_{BEn} = V'_{Bn} - V_E, \quad (2)$$

$$V'_{BCn} = V'_{Bn} - V_C. \quad (3)$$

III. NPN DEVICE FABRICATION

The fabrication process of the NPN LBJT is essentially the same as reported previously in Refs. 6 and 7 using the test-site

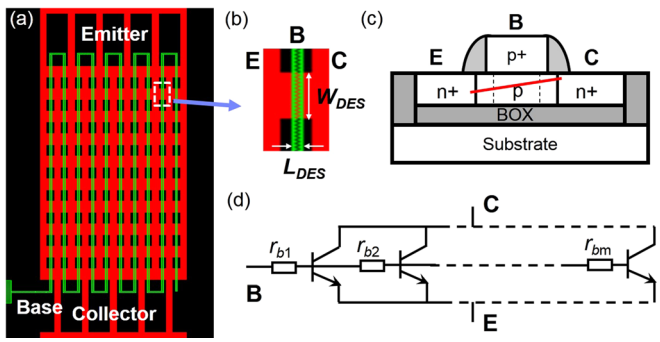

FIG. 2. (a) Example layout for a 100-transistor parallel chain used for defect detection in this study. (b) Layout of an individual device within the chain. The device width (W_{DES}) parallel to E-B and C-B junctions is 0.5 μm. (c) Schematic of the emitter-to-collector short caused by pipe defects (red line). (d) Circuit diagram of a parallel chain.

described in Sec. II. The process flow is outlined in Fig. 3. The starting SOI wafers have a silicon thickness of about 60 nm. The base/well doping concentration is about 5×10^{18} cm^{-3}, formed by boron implantation followed by rapid thermal anneal (RTA) at 1000 °C for 10 s. The extrinsic-base polysilicon has a nominal thickness of 100 nm, doped by 2×10^{15} cm^{-2} boron implantation at 5 keV, resulting in an average doping concentration of about 2×10^{20} cm^{-3}. The emitter/collector regions were doped to an average concentration of 4×10^{20} cm^{-3} by arsenic implantation. The devices were then given a standard RTA (RTA 1) at 1000 °C for 5 s. This standard RTA step is meant to activate the implanted arsenic in the emitter and collector regions and to distribute the implanted boron uniformly within the extrinsic-base polysilicon layer. (Diffusion along polysilicon grain boundaries is much more rapid than diffusion in crystalline silicon.[9]) The devices were first measured after RTA 1. Subsequently, additional cycles of RTA (RTA 2 to 4), each being 10 s at 1000 °C, followed by measurements were carried out to study the changes in device characteristics and to look for signs of pipe defects.

IV. DETECTION OF PIPE DEFECTS

A. Measurement technique

When a voltage V_{CE} is applied across an NPN transistor, a pipe defect provides a current path for electrons to flow from the emitter to the collector, leading to a positive collector current. If the emitter-base diode is forward biased at the same time, the measured collector current would be the sum of the pipe current and the normal collector current due to electrons injected from the emitter into the base. Therefore, for detection of a pipe defect, a transistor should be operated at small V_{BE} so that the normal collector current is small compared to the expected pipe current. In this paper, we focus on the device characteristics measured at $V_{BE} = 0$ V and $V_{BE} = 0.3$ V in pipe defect detection. Also, since the measured characteristics from the $W_{DES} = 0.5$ μm and $W_{DES} = 1.0$ μm arrays were essentially the same, we use the data from the 0.5-μm arrays to illustrate the device physics and learning.

1. Typical output characteristics at low V_{BE}

Typical measured output characteristics, i.e., I_C-V_{CE}, at $V_{BE} = 0.3$ V for the $L_{DES} = 60$ nm 100-device arrays are

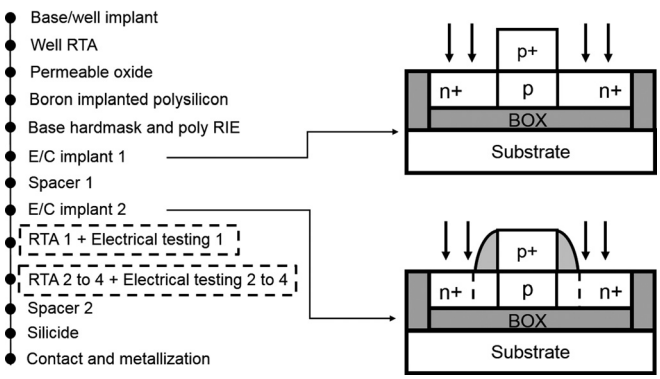

FIG. 3. CMOS-compatible process flow for fabricating lateral SOI bipolar transistors.

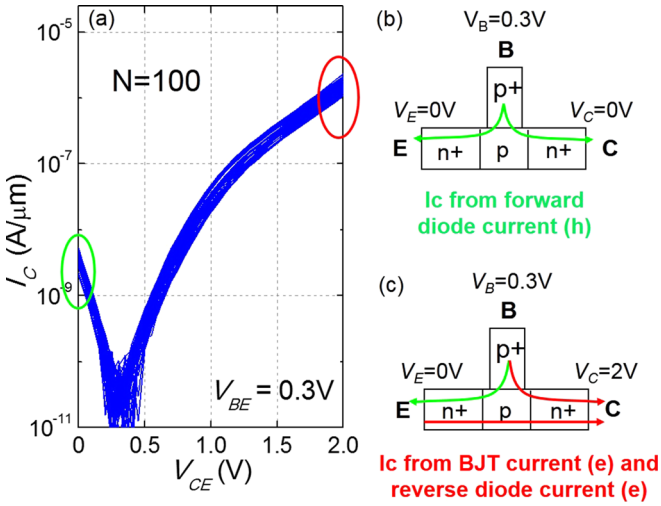

FIG. 4. I_C-V_{CE} behavior at $V_{BE} = 0.3$ V. (a) I_C-V_{CE} for a chain of 100 devices. 50 traces are shown, two from each of the 25 chips on the wafer. (b) and (c) The flow of electrons and holes at $V_{CE} = 0$ and $V_{CE} = 2$ V, respectively, as explained in the text.

shown in Fig. 4(a) on a semi-log scale. It shows I_C starting as a negative current at $V_{CE} = 0$ V. As V_{CE} is increased from zero, the magnitude of (the negative) I_C decreases and eventually reaches zero at $V_{CE} \approx V_{BE}$. As V_{CE} is increased beyond this point, I_C changes the sign, becoming positive, and increases with V_{CE}. This behavior of the transistor can be understood from Figs. 4(b) and 4(c) with the help of Eqs. (1)–(3) as follows:

When $V_{BE} > 0$ and $V_{CE} = 0$, see Fig. 4(b), both the emitter-base and the collector-base diodes are forward biased by the same magnitude of voltage, and the measured collector current is due to holes injected from the base into the collector and is hence negative. There is no electron component in the collector current because the electron injection from the emitter is cancelled by the electron injection from the collector. As V_{CE} is increased from zero, the collector-base diode becomes less forward biased than the emitter-base diode, and the collector current is a combination of the reduced hole injection from the base and the net electron injection from the emitter, causing the negative collector current to decrease in magnitude. As V_{CE} approaches V_{BE}, the collector current becomes completely dominated by electron

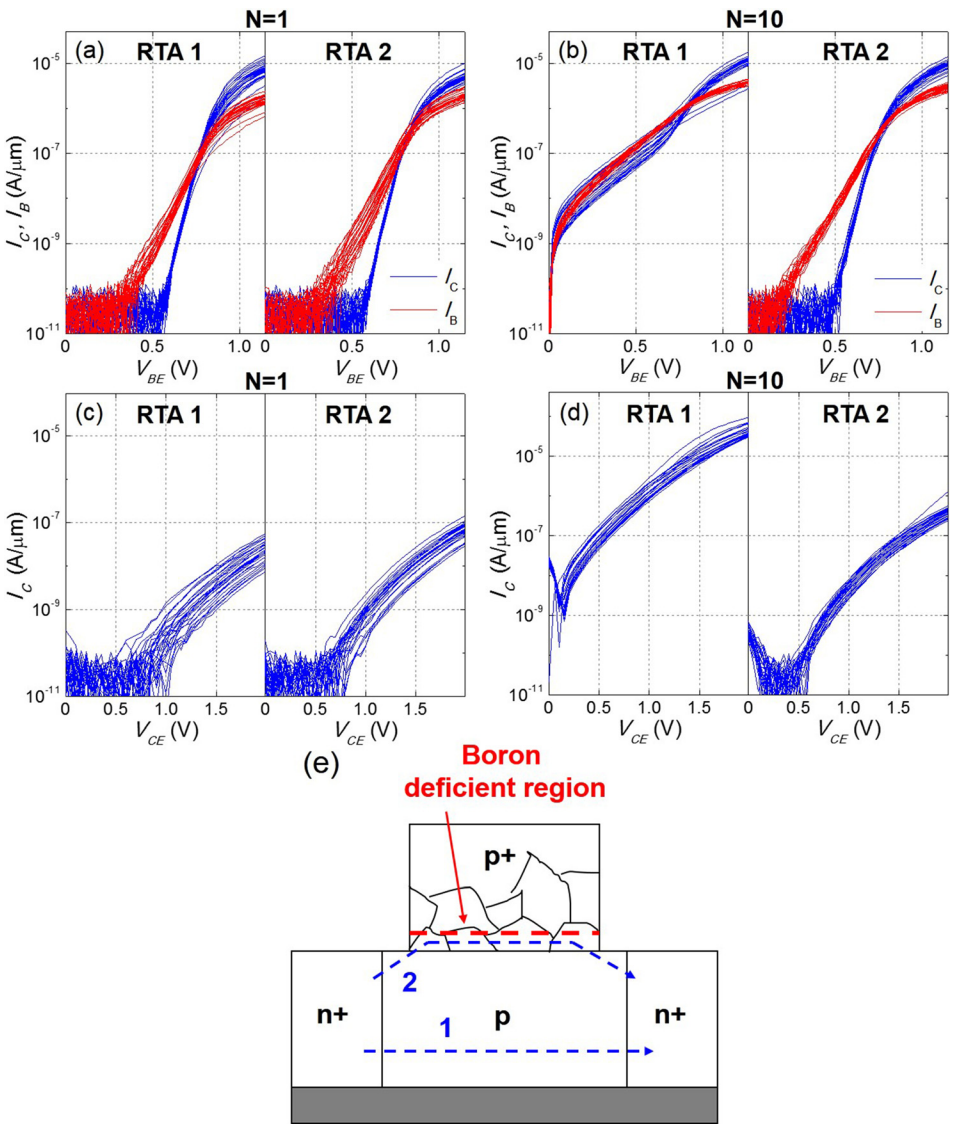

FIG. 5. (a) Sample Gummel plots for the 1-device structure after RTA 1 and RTA 2 and (b) for the corresponding 10-device arrays. (c) and (d) The output characteristic at $V_{BE} = 0.3$ V of the same devices in (a) and (b), respectively. (e) Schematic illustrating that a boron-deficient region could form at the bottom of the extrinsic base polysilicon due to insufficient annealing, providing a parasitic path (path 2) for electron flow besides the normal path (path 1). 25 traces are shown in plots (a)–(d).

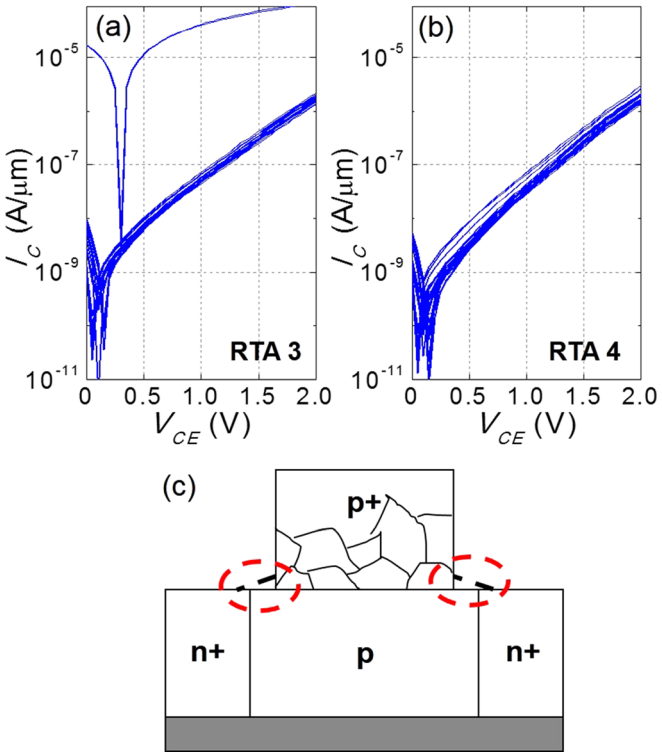

FIG. 6. Sample measured output characteristics of 10 000-device arrays at $V_{BE} = 0.3$ V, showing a defect detected after RTA 3 (a) but not after RTA 4 (b). (c) A schematic illustrating possible defective emitter-base and collector-base diodes due to polysilicon residue (circled by red dashed lines) after RIE. 25 traces are shown in (a) and (b).

injection from the emitter and becomes positive. At V_{CE} larger than V_{BE}, see Fig. 4(c), the collector current is a combination of electron injection current from the emitter and diode leakage current from the reverse-biased collector-base diode.

2. Effect of base resistors in a parallel transistor chain

The above picture becomes more complex for a parallel transistor chain due to the $I{\cdot}R$ drops in the base resistors [see Eqs. (1)–(3)]. The base current due to a forward-biased emitter-base (or collector-base) diode is positive. However, the base current due to leakage current from a reverse-biased collector-base diode is negative. For the nth transistor in a chain, Eq. (1) suggests that $V'_{Bn} < V_B$ if the net $I{\cdot}R$ drop is positive and $V'_{Bn} > V_B$ if the net $I{\cdot}R$ drop is negative. The collector current I_{Cn} from the nth transistor is governed by its internal voltages V'_{BEn} and V'_{BCn}, given by Eqs. (2) and (3). As V'_{Bn} changes due to the net $I{\cdot}R$ drop, I_{Cn} changes accordingly. The change in I_{Cn} induced by $I{\cdot}R$ drop could be fairly pronounced at large V_{CE} where reverse-biased collector-base diode leakage could be large. Collector-base diode leakage gives rise to a negative base current, leading to an increase in V'_{BEn} according to Eq. (2), which in turn causes I_{Cn} to increase exponentially. This explains the very rapid rise of the measured I_C in Fig. 4(a) at $V_{CE} > V_{BE}$.

According to Eqs. (1) and (2), if only one transistor in a parallel chain has a defect that changes its base current appreciably, say transistor n has a defect and I_{Bn} is changed appreciably, the V'_{BE} of every transistor along the chain between transistor n and the base electrode will be affected, causing their collector currents to change accordingly. Therefore, the measured I_C of a transistor chain could reveal a defect in just one of its component transistors. This will be discussed further in Sec. IV B.

B. Effect of post-implantation thermal annealing

Since pipe defects are due to locally enhanced dopant diffusion from the emitter and collector, manifesting as excessive I_C at low V_{BE}, it is important to understand how device behavior changes with post-implantation annealing to unambiguously distinguish between excess currents due to pipe defects from other defects caused by fabrication process issues. Excessive currents not related to pipe defects were indeed observed in our experiments. They are described and discussed below.

1. Parasitic I_C and I_B due to the inadequately doped extrinsic base

Figure 5(a) compares the Gummel plots after RTA 1 and RTA 2, respectively, for 1-device structures. The currents after RTA 1 and after RTA 2 are about the same and are as expected from properly fabricated individual NPN

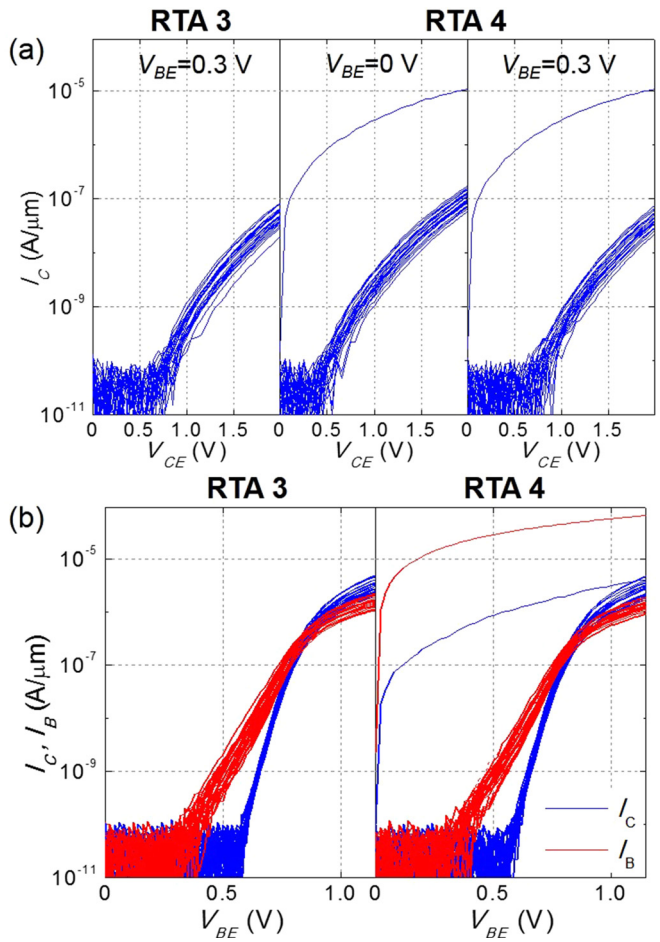

FIG. 7. Sample plots showing the evolution of (a) output currents and (b) Gummel currents from RTA 3 to RTA 4. No pipe defect was detected after RTA 3, but one pipe defect appeared after RTA 4. 25 traces are shown in each plot.

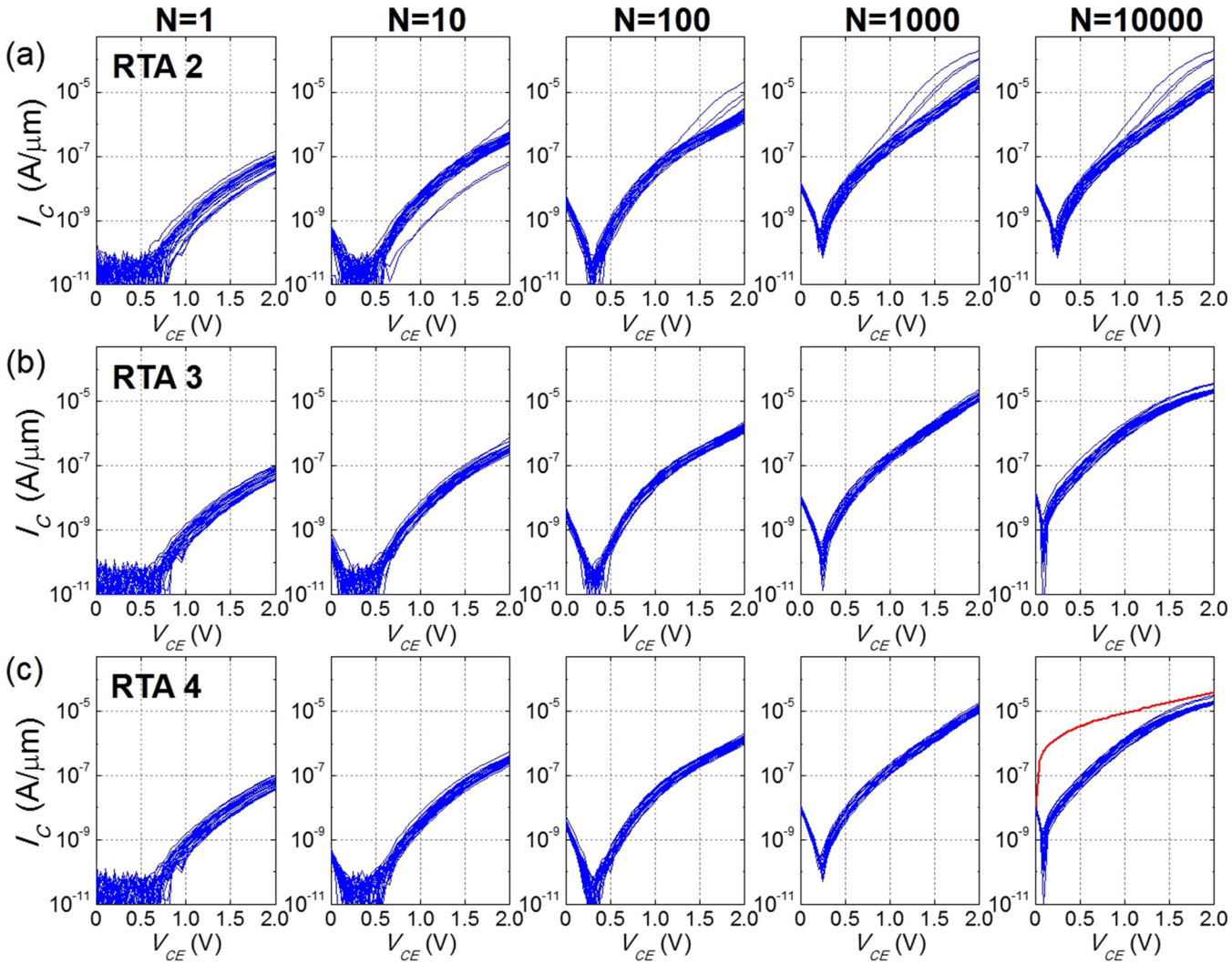

FIG. 8. Sample output characteristics after RTA 2 (a), RTA 3 (b), and RTA 4 (c). In each case, the characteristics for $W_{DES} = 0.5\ \mu$m single-device, 10-device, 100-device, 1000-device, and 10 000-device arrays are shown. One pipe defect was detected from the 10 000-device arrays after RTA 4. 25 traces are shown in each plot.

transistors measured prior to silicide formation. The base currents show a 120 mV/decade behavior, indicating domination by recombination in the emitter-base diode space-charge region.[10] Figure 5(c) shows the corresponding plots of I_C-V_{CE} at $V_{BE} = 0.3$ V. Figures 5(a) and 5(c) do not suggest any process induced parasitic currents.

Figures 5(b) and 5(d) show the Gummel plots and plots of I_C-V_{CE} at $V_{BE} = 0.3$ V, respectively, after RTA 1 and RTA 2 for the corresponding 10-device chains. Figure 5(b) clearly shows a large unexpected base and collector currents in the Gummel plot after RTA 1. However, the unexpected currents are absent after RTA 2. The fact that the unexpected collector current in Fig. 5(b) was gone after RTA 2 suggests that the unexpected collector current is not caused by pipe defects. We expect pipe-induced collector current to increase, instead of decrease, with additional RTA steps.

Comparison of the I_C-V_{CE} plots in Figs. 5(c) and 5(d) shows a large reduction of I_C in the 10-device chains after RTA 2. This is consistent with the discussion earlier that changes in the base currents in a transistor chain could cause large changes in collector current.

The origin of the parasitic base and collector currents in the Gummel plot in Fig. 5(b) can be explained by a "boron deficient region" in the extrinsic base, as illustrated in Fig. 5(e). The extrinsic-base was doped by boron implantation. Even though boron diffusion is much faster in polysilicon than in crystalline silicon, RTA 1 (1000 °C 5 s) may not be sufficient for boron to reach the intended doping level of 2×10^{15} cm^{-2} at the polysilicon/silicon interface. As a result, a device may have a boron deficient region in the extrinsic-base polysilicon adjacent the intrinsic base. When the emitter-base diode is forward biased, electrons from the emitter may be injected into the intrinsic base (crystalline p-type region) and into the boron deficient region of the extrinsic base, as illustrated in Fig. 5(e). It is known that minority carriers have a fairly long diffusion length in doped polysilicon, which is the physical basis for the so-called polysilicon-emitter technology.[11] Therefore, electrons injected into the boron deficient extrinsic-base polysilicon can lead to a parasitic collector current, and recombination of electrons within the polysilicon gives rise to a parasitic base current. Additional RTA steps could

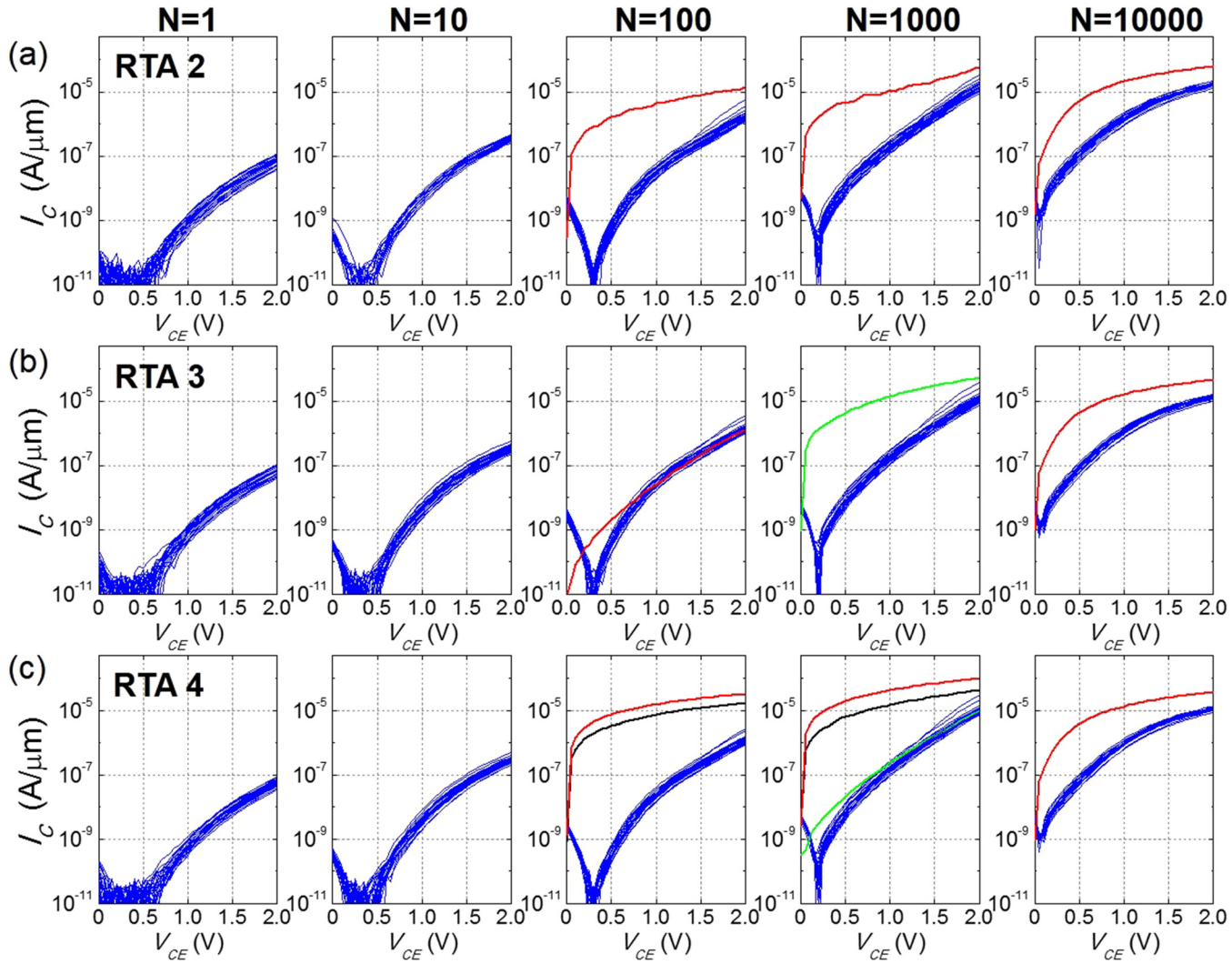

FIG. 9. Sample output characteristics, similar to Fig. 8, for arrays with $W_{DES} = 1.0\,\mu$m. Several pipe defects were detected from the 100-device, 1000-device, and 10 000-device arrays after RTA 2. Different colors correspond to different chip sites. 25 traces are shown in each plot.

eliminate a boron deficient region and hence eliminate the associated parasitic base and collector currents. In a chain of multiple transistors, the measured excessive currents could be due to just one transistor in the chain having parasitic currents. This explains why the Gummel plot in Fig. 5(a) for single-device structures does not show excessive base and collector currents, while the Gummel plot in Fig. 5(b) for 10-device chains shows excessive base and collector currents. The probability of having a boron-deficient region in a 10-transistor chain is higher than in a 1-device structure. The 100-, 1000-, and 10 000-transistor chains all show excessive base and collector currents consistent with boron deficiency in the extrinsic-base region adjacent the intrinsic base.

2. Defective emitter-base and collector-base diodes

The measured I_C-V_{CE} characteristics for the $L_{DES} = 60$ nm 10 000-device arrays at $V_{BE} = 0.3$ V are shown in Fig. 6(a) after RTA 3 and in Fig. 6(b) after RTA 4. After RTA 3, one of the 10 000-device arrays exhibited a collector current almost 100× higher than the rest of the arrays. However, after RTA 4, this defective array became normal just like the rest, suggesting that the observed excessive collector current after RTA 3 was not caused by a pipe defect.

In Fig. 6(a), the current from the defective array has the same behavior as the rest of arrays and as those in Fig. 4(a), except that its magnitude is much larger. As discussed earlier in Sec. IV A, the currents in Fig. 4(a) at $V_{CE} < V_{BE}$ is due to a combination of electron injection from the emitter and recombination in the base-collector diode space-charge region and at $V_{CE} > V_{BE}$ by a combination of electron injection from the emitter and leakage current from the reverse-biased base-collector diode. Therefore, the array showing extra-large current in Fig. 6(a) is likely due to the defective base-collector diode in one or more devices in the array. The defective diode (or diodes), which caused larger recombination current in forward bias at $V_{CE} < V_{BE}$ and larger leakage current in reverse bias at $V_{CE} > V_{BE}$, became normal after RTA 4. One possible origin of a diode defect could be a diode having a component with the junction inside the extrinsic-base polysilicon. This could be due to the polysilicon residue from Reactive-Ion-Etch (RIE), as illustrated in Fig. 6(c). A polysilicon p-n diode is more "defective"

compared to a regular crystalline silicon p-n diode. During subsequent RTA steps, fast boron diffusion in polysilicon may compensate the arsenic dopant, thus pushing the junction from inside the polysilicon to outside the polysilicon and hence "repairing" the defective diode.

C. Effect of post-implantation thermal annealing

A pipe defect is not expected to be repairable with additional RTA steps. One example of a pipe defect is shown in Fig. 7(a), which shows the measured I_C-V_{CE} data for $L_{DES} =$ 60 nm 1-device structures. After RTA 3, no defective device was detected. However, after RTA 4, one of the devices shows excess collector current. This excess current is positive for all V_{CE} values, independent of V_{BE}, consistent with a pipe defect (instead of a diode defect). The corresponding Gummel plots (measured at $V_{CB} = 0$ V) are shown in Fig. 6(b) where the defective device exhibits excessively large I_C and I_B. The large I_C at relatively small V_{BE} is certainly a sign of pipe defects. The excessively large I_B suggests that the pipe defect is accompanied by a highly defective emitter-base diode.

As discussed in Sec. IV B (see Fig. 5 and associated discussion), excess I_C and I_B caused by a boron deficient region in the extrinsic-base polysilicon layer could occur after RTA 1. Such excess currents are not related to pipe defects and can be eliminated with additional post-implant annealing (e.g., RTA 2). Thus, we will focus on the I_C-V_{CE} data taken after RTA 2, where excess currents due to boron deficiency in extrinsic base are minimized, to study pipe defects in our SOI LBJT.

The I_C-V_{CE} data for $L_{DES} =$ 80 nm devices in the $W_{DES} = 0.5\ \mu$m arrays of various sizes after several sequential annealing steps (RTA 2, RTA 3, and RTA 4) are plotted in Figs. 8(a), 8(b), and 8(c). Regardless of the array size, all devices show less variation after each successive RTA step, suggesting that additional thermal treatments reduced process variations, probably due to better dopant activation and reduction of implant-related defects. As discussed in Sec. IV A 2, reduction of implant-related defects should reduce base-collector diode leakage, which in turn should reduce collector current at large V_{CE}. This is clearly seen by comparing Figs. 8(a) and 8(b). Figure 9 shows plots, similar to those in Fig. 8, for the $W_{DES} = 1.0\ \mu$m arrays. In Fig. 8, only one pipe defect was detected in the N = 10 000 array after RTA 4. (See Fig. 7 and the accompanying discussion for the expected electrical properties of pipe defects.) Figure 9 shows more pipe defects compared to Fig. 8, consistent with the fact that the devices in Fig. 8 have a W_{DES} of 0.5 μm, while those in Fig. 9 have a W_{DES} of 1.0 μm.

V. DISCUSSION AND CONCLUSIONS

Several process-related electrical defects in SOI LBJT fabricated by ion implantation of extrinsic base and emitter/collector regions have been revealed by testing arrays of parallel-connected transistor chains. Emitter-base and collector-base diode defects, which exhibit large recombination currents when the diodes are forward biased and large leakage current when the diodes are reverse biased, can be readily distinguished from pipe defects which manifest as emitter-to-collector shorts.

Dopant deficiency in the extrinsic base region adjacent the intrinsic base could produce a parasitic bipolar transistor with its intrinsic base being the dopant-deficient extrinsic-base region, operating in parallel with the normal transistor. Therefore, it is important to have the entire extrinsic-base region much more heavily doped than the intrinsic base. In this respect, *in-situ* doping of the extrinsic base may be preferred over doping the extrinsic base by ion implantation.

A few pipe defects were detected. In most cases, a pipe defect was formed only after more than 30 s of RTA at 1000 °C. When pipe defects were detected, the pipe defect density appeared quite low. For example, only 1 pipe defect was detected in testing 55 550 transistors in the arrays with $W_{DES} = 0.5\ \mu$m after 35 s of RTA at 1000 °C. Thus, pipe defects do not appear to be a show stopper for SOI LBJT fabricated by ion implantation. One direction of future development of SOI LBJT is to use *in-situ* doping, instead of ion implantation, to form emitter/collector regions.[12] *In-situ* doping requires much lower temperature for post-emitter RTA and hence should be much less likely to create pipe defects.

ACKNOWLEDGMENTS

The authors thank Dr. G. G. Shahidi for insightful discussions and management support. The device fabrication was done at the Microelectronics Research Laboratory at the IBM T. J. Watson Research Center.

[1]J. J. Pekarik, J. Adkisson, P. Gray, Q. Liu, R. Camillo-Castillo, M. Khater, V. Jain, B. Zetterlund, A. DiVergilio, X. Tian, A. Vallett, J. Ellis-Monaghan, B. J. Gross, P. Cheng, V. Kaushal, Z. He, J. Lukaitis, K. Newton, M. Kerbaugh, N. Cahoon, L. Vera, Y. Zhao, J. R. Long, A. Valdes-Garcia, S. Reynolds, W. Lee, B. Sadhu, and D. Harame, in *Proceedings of the 2014 Bipolar/BiCMOS Circuits and Technology Meeting* (2014), pp. 92–95.
[2]S. Zafar, M. Khater, V. Jain, and T. Ning, Appl. Phys. Lett. **106**, 063701 (2015).
[3]S. Zafar and T. Ning, in *2016 European Solid-State Device Research Conference (ESSDERC)* (2016), pp. 389–392.
[4]F. Barson, IEEE J. Solid-State Circuits **11**, 505–510 (1976).
[5]E. M. Juleff, Solid-State Electron. **16**(10), 1173–1180 (1973).
[6]J. Cai, T. H. Ning, C. D'Emic, K. K. Chan, W. E. Haensch, J.-B. Yau, and D.-G. Park, in 2011 Int. Electron Devices Meet. (IEDM), Washington, DC, 5–7 December 2011 (IEEE, 2011).
[7]J. Cai, T. H. Ning, C. D'Emic, J.-B. Yau, K. K. Chan, J. Yoon, K. A. Jenkins, R. Muralidhar, and D.-G. Park, in IEEE S3S Conference (2013).
[8]T. H. Ning and J. Cai, IEEE J. Electron Devices Soc. **1**(1), 21–27 (2013).
[9]B. Swaminathan, K. C. Saraswat, R. W. Dutton, and T. I. Kamins, Appl. Phys. Lett. **40**, 795–798 (1982).
[10]J.-B. Yau, J. Cai, and T. H. Ning, IEEE J. Electron Devices Soc. **4**, 116–123 (2016).
[11]T. H. Ning and R. D. Isaac, IEEE Trans. Electron Devices. **27**, 2051–2055 (1980).
[12]P. Hashemi, J.-B. Yau, K. K. Chan, T. H. Ning, and G. G. Shahidi, in IEEE S3S Conference (2017).