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Development of CdSe thin films for application in electronic devices

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Abstract Thin films of cadmium selenide (CdSe) have been deposited on fluorine-doped tin oxide (FTO)-coated glass using potentiostatic electrodeposition method. The suitable range of deposition potentials for the formation of stoichiometric layer of CdSe was established using cyclic voltammograms. The films have been characterised using X-ray diffraction (XRD), Raman spectroscopy, optical absorption, scanning electron microscopy, atomic force microscopy and photo-electrochemical (PEC) cell techniques. XRD results show that the deposited films are polycrystalline in nature having hexagonal structure with preferred orientation along (002) plane. PEC study reveals that the films have n-type electrical conductivity. The optical bandgap of the film have been estimated to be 2.00 and 1.80 eV for as-deposited and heat-treated layers respectively when grown at a cathodic potential of 1,972 mV. The electronic quality of the electrodeposited CdSe layers was also tested using the device structure glass/FTO/n-CdSe/Au which produced Schottky diodes with rectification factor of $10^{2.9}$, reverse saturation current of $\sim$372 nA and threshold voltage of $\sim$0.15 V. The potential barrier observed for Au/n-CdSe interface is >1.10 eV.

1 Introduction

CdSe is a well-known II–VI semiconductor that can crystallize in either wurtzite (hexagonal) or the zinc blende (cubic) structure. It is a direct bandgap semiconductor material which is used in opto-electronic devices, light-emitting diodes (LEDs), field-effect transistors (FETs), biosensors, biomedical imaging and solar cells fabrication [1]. CdSe can be used as an n-type buffer, window or absorber layer in thin film solar cells by selecting its thickness appropriately. It is suitable as a buffer layer because of its unique wetting properties on glass/fluorine-doped tin oxide (FTO) surfaces. CdSe has a bandgap of $\sim$1.80 eV in the wurtzite crystal phase and $\sim$1.71 eV in the zinc blende phase [1]. According to Zhao et al. [1], this wide bandgap favours absorption over a wide range of the visible spectrum. The deposition of CdSe thin film has been achieved using different growth methods such as pulsed laser deposition [2], thermal evaporation [3], chemical bath deposition (CBD) [2, 4, 5], spray pyrolysis [6, 7] and electrodeposition [8–12]. Among the above mentioned deposition techniques, the electrodeposition method is suitable because of its low temperature growth, its low capital cost and the ability to control the film thickness by varying the deposition time and potential.

Electrodeposition method also provides the platform for controlling the material properties (optical, structural, morphological and electrical) by adjusting the preparative parameters such as growth temperature of the electrolyte, pH, concentration of the electrolyte, stirring, deposition time and post-deposition annealing temperature. One key requirement in electrodeposition technique is that the substrate must be conductive. Golan et al. [9] produced epitaxially oriented arrays of CdSe nanocrystals electrodeposited (ED) onto gold substrates. Thanikaikarasan et al. [13] have prepared CdSe thin films on indium-doped tin oxide (ITO)-coated glass substrates from an aqueous electrolyte using a 3-electrode electrodeposition method. Pawar et al. [14] used 3-electrode electrodeposition method

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to electrosynthesize thin films of CdSe on stainless-steel and FTO-coated glass substrates from aqueous acidic bath using cadmium acetate as a Cd ion source. Athanassopoulou et al. [15] ED CdSe films on nickel substrates using a thermostat-controlled three-electrode cell. CdSe thin films were also ED by Lokhande et al. [11] on titanium substrates from aqueous and weakly alkaline bath using a three-electrode cell.

Several works have been carried out to-date on electrodeposition of CdSe thin films using three-electrode cell from aqueous and non-aqueous solution in either acidic or basic medium. Substrates such as ITO-coated glass, FTO-coated glass, nickel, stainless steel, titanium and so on have also been used as conductive substrates to carry out electroplating work. This work focuses on cathodic electrodeposition of CdSe thin films on FTO-coated glass substrates using two-electrode system and aqueous acidic electrolyte. Electronic qualities of the ED-CdSe layers were also tested using the device structure glass/FTO/n-CdSe/Au metal contact.

2 Experimental details

2.1 Electrodeposition of CdSe layers

The precursors used for the growth of CdSe thin films were 0.3 M $CdCl_2$ as Cd^{2+} source and 0.003 M SeO_2 as Se^{2-} source in 400 ml of deionised water. All chemicals used for electrodepositon were analytical reagent grade of purity 5 N (99.999 %) from Sigma Aldrich. The growth temperature and pH of the bath used for the optimisation of the growth voltage were approximately 80 °C and 2.20 ± 0.02 respectively. The pH of the bath was adjusted accordingly by adding ammonia or HCl solution. The glass/FTO used in this work was TEC-15 with a sheet resistance of 13 Ω/square. Since substrate cleaning is a very important step in thin films deposition, the glass substrates were thoroughly cleaned using soap solution and organic solvents (methanol and acetone). Samples were also rinsed with de-ionised water in between solvents; finally, the substrates were dried with nitrogen gas. The electroplating of CdSe was carried out in potentiostatic mode using a 2-electrode system which is known for its low-cost and impurities reduction in the electrolytic bath [16, 17]. Figure 1 shows the typical electrodeposition set-up for the simplified 2-electrode system.

2.2 Experimental techniques

The films were characterised for their structural properties by using Philips PW 3710 X'pert Pro diffractometer (Philips Analytical, Almelo, The Netherlands) with Cu-K_α monochromator of wavelength, $\lambda = 1.5416$ Å in the range of $2\theta = (10–70)°$. The X-ray generator tension and current were 40 kV and 40 mA respectively. The surface morphology of the deposited films was studied with scanning electron microscopy (SEM) by using FEI NOVA 200 NanoSEM equipment. Atomic force microscopy (AFM) was carried out by the collaborator in Kazakhstan. A Carry 50 scan UV–Visible spectrophotometer (Varian Australia Pty. Ltd.) was used for studying the optical properties of the deposited films and for bandgap estimation, while thickness measurement on the deposited layers was carried out using UBM Microfocus optical measuring system (UBM, Messetechnik GmbH, Ettlingen, Germany).

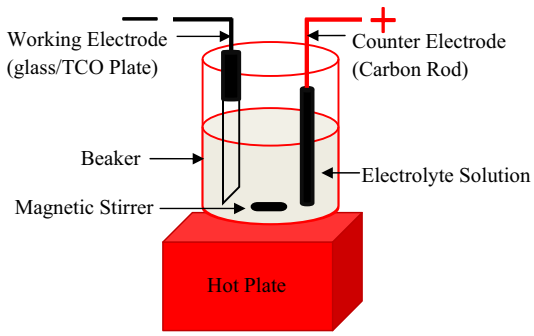

Fig. 1 Electrodeposition set-up used for a simplified 2-electrode system

A computerised GillAC potentiostat was used to carry out the cyclic voltammetry and electrodeposition while photoelectrochemical (PEC) cell measurements were carried out to determine the electrical conductivity type of the ED-CdSe. The PEC cell consists of a graphite electrode which acts as the counter electrode, the semiconducting electrode (FTO/CdSe) to form the active junction and electrolyte made from aqueous solution of 0.10 M $Na_2S_2O_3$. By immersing the semiconducting electrode inside the electrolyte, a solid/liquid junction is formed. The difference between the voltages when the semiconductor is illuminated (V_L) and when the semiconductor is in dark condition (V_D) represents the PEC signal or open circuit voltage that is produced by the solid/liquid junction. The light source is a DC 12 V, 5 W tungsten filament bulb. The sign of the PEC signal determines the electrical conductivity type while the magnitude of the PEC signal indicates the quality of the depletion layer formed at the interface [17].

3 Results and discussion

3.1 Cyclic voltammetry

Cyclic voltammetry is a very useful tool in electrochemistry to determine the suitable voltage range for growing

thin film materials [18]. In this process, a range of cathodic potentials from 0 to 2,500 mV was applied across the electrolyte through the electrodes, using a computerised potentiostat at a sweep rate of 180 mV min^{-1}. The current through the electrolyte was monitored as the voltages between electrodes are changed. Cyclic voltammetry was used to monitor the electrochemical reactions in solutions of 0.3 M $CdCl_2$, 0.003 M SeO_2 and 0.3 M $CdCl_2$ + 0.003 M SeO_2 each in 400 ml of de-ionised water to determine the approximate deposition voltages for Cd, Se and CdSe respectively.

3.1.1 Cyclic voltammogram of 0.3 M $CdCl_2$

0.3 M $CdCl_2$ was prepared using 400 ml of de-ionised water and the pH of the first solution was measured to be 3.79 ± 0.02 at room temperature; this pH was adjusted to 2.20 ± 0.02 by the addition of HCl solution. The first voltammogram of the $CdCl_2$ solution as shown in Fig. 2 was taken to help in determining the potential at which the Cd deposition and dissolution take place. From Fig. 2, the first hump appears at a cathodic potential ~910 mV; this shows that Cd begins to deposit at this potential. In the reverse direction of the curve, the transition point from the positive current density axis to the negative is ~1,440 mV; this voltage is an indication of the potential at which Cd dissolution begins to dominate. In fact, at ~1,440 mV, equal amounts of Cd deposition and dissolution take place and hence the resultant current becomes zero. The reduction of Cd^{2+} to Cd on the surface of FTO electrode takes place according to Eq. (1), and the current flow is in the forward direction. However, the dissolution of Cd takes place according to Eq. (2) and the current produced is in the opposite direction.

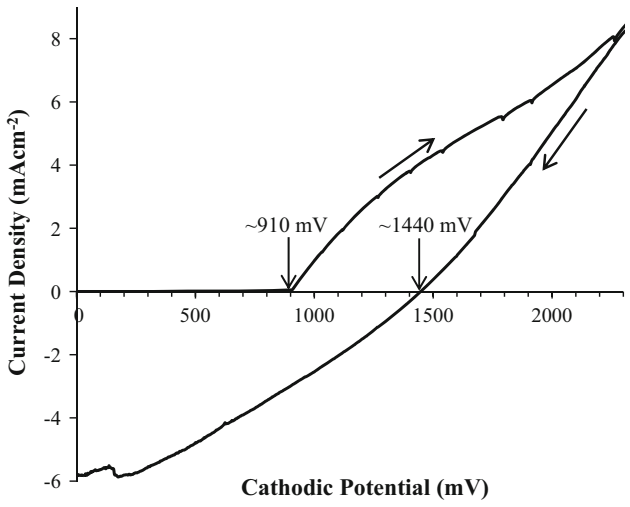

Fig. 2 A typical cyclic voltammogram of electrolyte containing 0.3 M of $CdCl_2$ aqueous solution (pH = 2.20 ± 0.02, T = 80 °C)

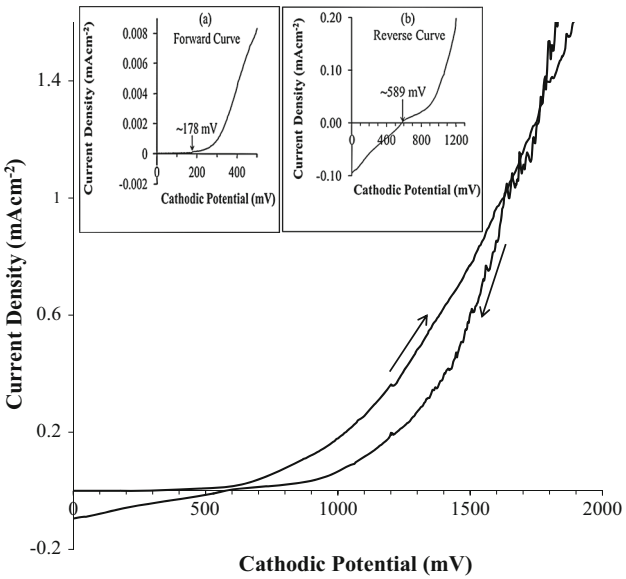

Fig. 3 A typical cyclic voltammogram of electrolyte containing 0.003 M of SeO_2 aqueous solution (pH = 2.20 ± 0.02, T = 80 °C)

$$Cd^{2+} + 2e^- \rightarrow Cd \quad (1)$$

$$Cd \rightarrow Cd^{2+} + 2e^- \quad (2)$$

3.1.2 Cyclic voltammogram of 0.003 M SeO_2

A cyclic voltammogram of 0.003 M SeO_2 solution is shown in Fig. 3. In the forward curve (Fig. 3a), the first hump appears at a cathodic potential ~178 mV; this voltage is an indication of the potential at which Se deposition begins. According to Pawar et al. [14], this reduction peak is due to the irreversible reaction shown in Eq. (3b). Se dissolution begins to dominate at approximately 589 mV as shown in Fig. 3b.

$$SeO_2 + H_2O \rightarrow H_2SeO_3 \quad (3a)$$

$$H_2SeO_3 + 4H^+ + 4e^- \rightarrow Se + 3H_2O \quad (3b)$$

3.1.3 Cyclic voltammogram of 0.3 M $CdCl_2$ + 0.003 M SeO_2

Figure 4 shows the cyclic voltammogram measured for glass/FTO electrode in an aqueous solution containing a mixture of 0.3 M $CdCl_2$ and 0.003 M SeO_2. It is also worth noting that the minimum standard reduction potential for electrolysis of water molecules is about 1,230 mV [19]. The discharging of most active H atoms at the cathode while CdSe is forming is an excellent built-in method to passivate defects in the CdSe layer. However, if H_2 bubbles are formed at the cathode, it could have a detrimental effect of delamination of the semiconducting layer.

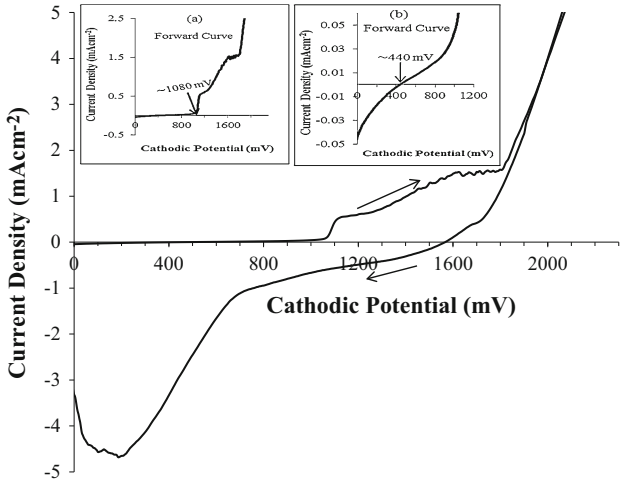

Fig. 4 Cyclic voltammogram of electrolyte containing 0.3 M of $CdCl_2$ + 0.003 M of SeO_2 aqueous solution (pH = 2.20 ± 0.02, T = 80 °C). (*Insets* show the transition voltages)

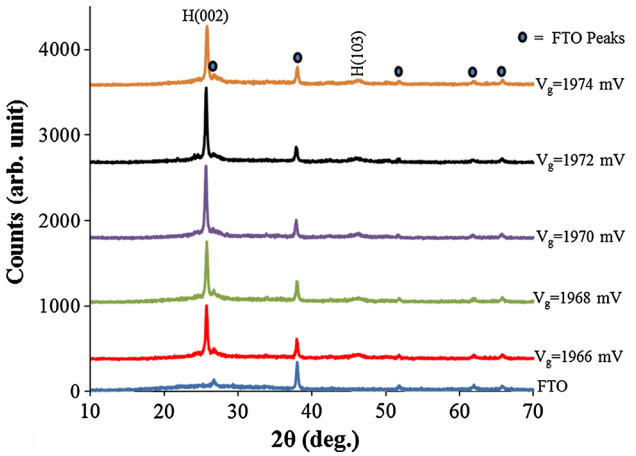

Fig. 5 XRD patterns for as-deposited CdSe layers as a function of growth voltage, V_g

The forward curve illustrated in Fig. 4a shows that Cd begins to deposit at ~1,080 mV while Fig. 4b shows that Se begins to deposit at ~440 mV. The sudden rise in deposition current at 1,080–1,800 mV shows the beginning of reaction between Cd and Se to form CdSe. In this region, the layer formed is a mixture of CdSe and elemental Se thus giving rise to a Se-rich CdSe layer. Beyond 1,800 mV, a sharp rise is noticed in the deposition current. This leads to a gradual decrease in the amount of elemental Se because more Cd is incorporated into the CdSe layer. As the growth voltage further increases, the amount of elemental Se in the CdSe layer gradually reduces thus giving rise to stoichiometric formation of CdSe layer in the voltage range between 1,900 and 2,000 mV. Beyond 2,000 mV, formation of Cd dendrites was observed. The Cd dendrites formation shows that at voltages ≥2,000 mV, the CdSe layer formed is a Cd-rich material.

The formation of CdSe thin film is according to the following overall reactions:

$$CdCl_2 \cdot H_2O \rightarrow Cd^{2+} + 2Cl^- + H_2O \quad (4a)$$

$$SeO_2 + H_2O \rightarrow H_2SeO_3 \quad (4b)$$

$$H_2SeO_3 + 4H^+ + 6e^- \rightarrow Se^{2-} + 3H_2O \quad (4c)$$

Reaction for the formation of CdSe on FTO substrate may be due to Eq. (5).

$$Cd^{2+} + Se^{2-} \rightarrow CdSe \quad (5)$$

As seen from Figs. 2 and 3, Cd begins to deposit at around 910 mV while Se begins to deposit at around 178 mV under the experimental conditions used in this work. The shift in the reduction potential of both Cd and Se from ~910 and 178 (Figs. 2, 3) to ~1,080 and 440 mV (Fig. 4a, b) respectively may be due to the chemical reaction that takes place to form CdSe. Comparing the potential at which both Cd and Se begin to deposit, it can be seen that Se deposits first before Cd as seen from the cyclic voltammogram. The redox potential (E_o) of Se and Cd are ~+0.74 and −0.40 respectively [20]. From the redox potential values, Se shows a more positive redox potential than Cd and therefore deposits first. The theoretical redox potential value can be used to determine which of the elements deposit first; however, its shortcoming is that it cannot be used to determine the approximate potential at which the compound is formed. This is why cyclic voltammetry was used to determine which of the elements deposit first and the suitable potential range to grow CdSe compound.

3.2 Material characterisation

The three techniques; XRD, optical absorption and PEC cell measurements were used in the preliminary characterisation and optimisation of growth voltage of the CdSe layers. To obtain a suitable deposition potential for the CdSe layer, other preparative parameters such as the growth temperature, pH and growth time (t_g) were kept constant at 80 °C, 2.20 ± 0.02 and 5 min respectively.

3.2.1 X-ray diffraction (XRD) studies

Samples of CdSe layers were grown in the voltage range between 1,900 and 2,000 mV in order to examine their structural properties and to identify material phases. This allows preliminary optimisation of growth voltage, V_g to produce near stoichiometric CdSe. Typical XRD patterns for as-deposited (AD) CdSe as a function of V_g are shown in Fig. 5 while Fig. 6 shows the XRD patterns of

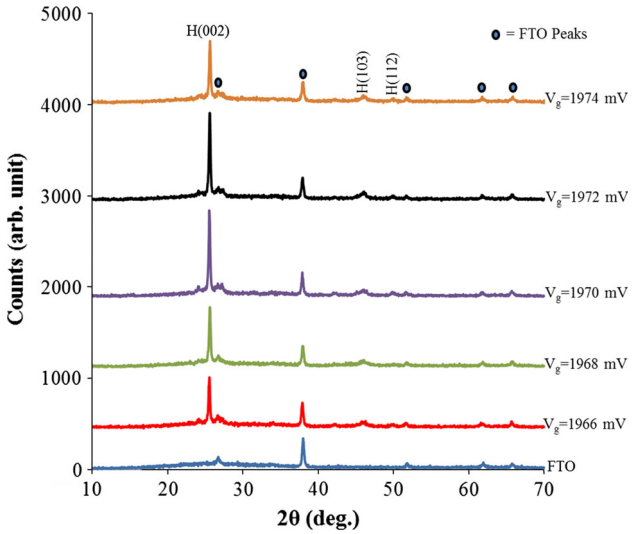

Fig. 6 XRD patterns for heat-treated CdSe layers at 350 °C for 15 min in air, as a function of growth voltage, V_g

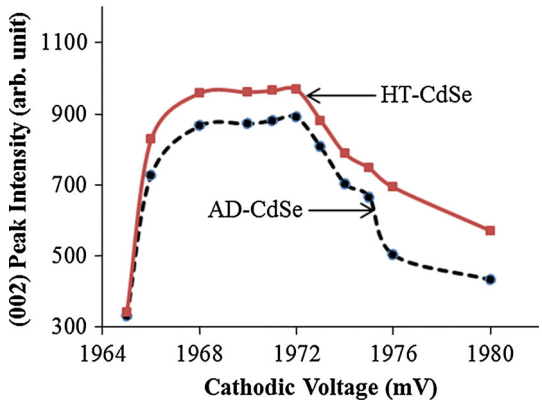

Fig. 7 Variation of (002) peak intensity as a function of growth voltage for AD- and HT-CdSe layers

heat-treated (HT) CdSe in air at 350 °C for 15 min. The XRD results thus show that CdSe layer grows best in the cathodic voltage range between 1,966 and 1,974 mV. A continuous increase in peak intensity was observed as the cathodic deposition voltage increases from 1,960 to 1,972 mV. A further increase in the voltage led to a decrease in the peak intensity indicating decrease in crystallinity in this V_g region. The XRD results also show that the highest intensity of the (002) peak occurs at a cathodic potential of 1,972 mV for both AD- and HT-CdSe samples (see Fig. 7). Therefore, in this work, V_g of 1,972 mV was selected as the optimum potential for electrodeposition of CdSe thin films. The XRD peaks also show that the as-grown and annealed CdSe films are polycrystalline in nature having hexagonal structure with the preferred orientation along (002) plane. Other peaks that correspond to (103) and (112) planes are also observed with lower peak intensities.

Figure 7 shows how the intensity of the (002) peak varies with the cathodic potential for both AD- and HT-CdSe. This result also explains how the crystallinity of the CdSe layers is improved when subjected to heat treatment. The peak intensities of the HT-CdSe are generally higher than those of the AD-CdSe. This is because increase in temperature also increases the grain size of the CdSe layers thereby leading to a corresponding improvement in crystallinity.

The observed d-spacing values (Table 1) from XRD results are compared with the standard values reported in JCPDS data, reference code '01-077-2307' and both are found to be in good agreement. The crystallite sizes of the AD- and HT-CdSe grown at 1,972 mV for 20 min are determined using Scherrer's equation given in Eq. (6). This

Table 1 Summary of XRD measurement results for AD- and HT-CdSe layers

Sample	Peak intensity	2θ (°)	d-Spacing (Å)	β°	β (rad.)	D (nm)
AD-CdSe	1,626	~26.00	3.4352	0.2598	0.0045	33.3
HT-CdSe	2,944	~26.00	3.4652	0.1299	0.0023	63.0

relationship is useful in calculating the crystallite size of a thin film material by using the results obtained from XRD analysis [13].

$$D = \frac{0.9\lambda}{\beta \cos\theta} \tag{6}$$

where D is the crystallite size in nm, λ is the X-ray wavelength (1.5416 Å), θ is the Bragg's angle in degree and β is the full width at half maximum (FWHM) of the peak with highest intensity, measured in radian. However, the Scherrer's equation has limitation since it cannot be used to estimate crystallite sizes more than (100–200) nm [21].

The calculated crystallite sizes for AD- and HT-CdSe thin films using (002) peak were ~33 and 63 nm respectively. Table 1 shows the comparison between the peak intensity and FWHM of AD- and HT-CdSe layers obtained from XRD measurements. After annealing, the intensity increases and the FWHM decreases indicating the improvement of crystallinity of the material. According to the Scherrer's Eq. (6), a reduction in FWHM (β) leads to an increase in the crystallite size and hence, a corresponding increase in grain size. Thus, the higher the crystallite sizes of a thin film material, the better its crystallinity.

3.2.2 Raman spectroscopy measurements

Raman spectroscopy is another technique that can be used in determining the crystallinity of semiconductor material.

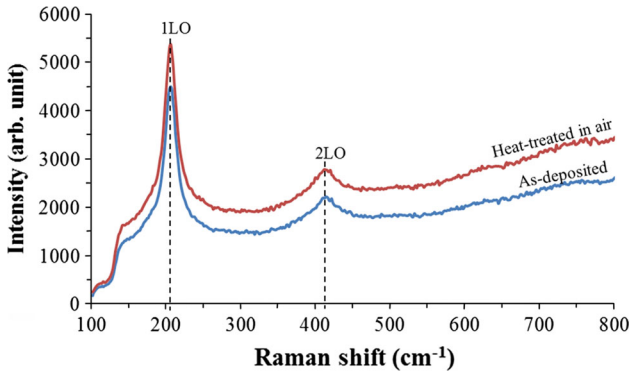

Fig. 8 Raman spectra of as-deposited and heat-treated CdSe thin films at 200 °C for 10 min in air

The Raman spectra were obtained using a Renishaw Raman microscope with 514 nm argon ion laser source and a charge-coupled device (CCD) detector. An extended spectrum for the AD- and HT-CdSe layers was collected at room temperature using a 50 % laser power (~15 mW) and 100× objective in the Raman microscope for 10 s. Initially, a 100 % laser power (~30 mW) was used in the experiment but after switching to white light, it was observed that a section of the sample exposed to the beam was already damaged. For this reason, the laser power was reduced to 50 %. Thus, the 50 % laser power was able to reduce the heating effect of the laser beam thereby preventing any change on the layer which could lead to loss or reduction of crystallinity. Curve fitting was also performed on the spectra using a combination of Lorentzian/Gaussain mathematical function to obtain parameters such as peak position, peak intensity and peak width also known as full width at half maximum (FWHM).

Figure 8 shows two visible Raman peaks for AD- and HT-CdSe layers at 200 °C for 10 min in air. These peaks are Raman longitudinal optical (LO) vibration mode at wave numbers 206 and 414 cm^{-1} for 1LO and 2LO peaks respectively. The wave numbers obtained in this experiment is almost similar to that obtained by Brioude et al. after using an excitation wavelength of 514.5 nm from an argon–krypton laser power [22]. Both AD- and HT-CdSe thin films reveal clear peaks at 1LO and 2LO with no shift in the peak positions. Table 2 shows the parameters obtained after performing curve fitting on the spectra. The result shows that HT-CdSe layer possesses a better crystallinity than the AD-CdSe layer due to reduced FWHM and higher peak intensity as observed in both 1LO and 2LO Raman peaks.

Table 2 Raman parameters obtained by curve fitting of the CdSe spectra

	As-deposited		Heat-treated	
	1LO	2LO	1LO	2LO
Raman peak position (cm^{-1})	206	414	206	414
Peak intensity (arb. unit)	3,002	428	3,171	450
FWHM (cm^{-1})	18.66	30.59	17.67	30.53

3.2.3 *Optical absorption studies*

The optical absorption measurements of the ED-CdSe layers were carried out in order to estimate the optical bandgap energy (E_g). Typical optical absorption graphs for estimation of bandgap energy of both AD- and HT-CdSe are shown in Fig. 9a; the graph was obtained by plotting the square of absorbance (A^2) as a function of the photon energy (hν). The bandgaps were estimated by extrapolating the straight line portion to the photon energy axis (at absorbance^2 = 0). Figure 9b shows the variation of the bandgap energy with the cathodic potential for both AD- and HT-CdSe layers. The results further show that the bandgap energy of the annealed CdSe at a cathodic voltage of 1,972 mV tends to be closer to the bandgap of bulk CdSe in the wurtzite crystal phase. This value has been reported by Zhao et al. [1] to be ~1.80 eV.

3.2.4 *Photoelectrochemical (PEC) cell measurements*

Figure 10 illustrates the PEC signal for both AD- and HT-CdSe layers grown at different growth voltages (V_g). The PEC

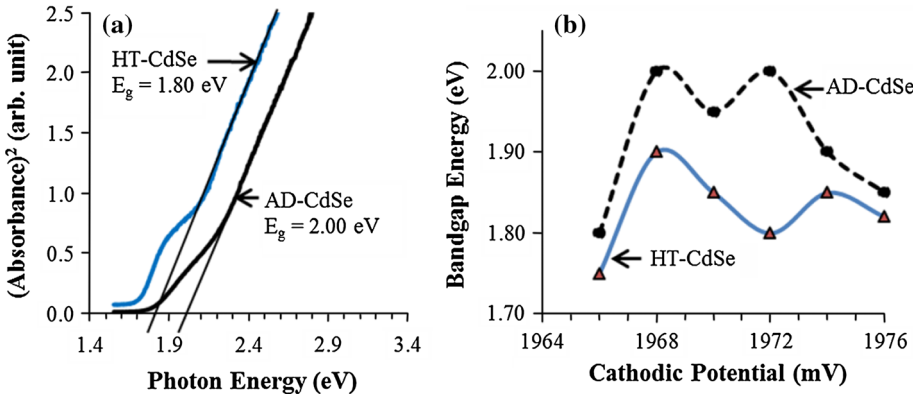

Fig. 9 **a** Typical optical absorption graphs for CdSe layers grown at 1,972 mV and **b** variation of the bandgap energy as a function of cathodic deposition potential

signal shows that both AD and HT samples of CdSe layers grown in the voltage range of 1,966–1,976 mV are n-type in electrical conduction. The result also shows a crossing/overlapping of the PEC signals for both AD- and HT-CdSe layers at a cathodic potential of 1,972 mV. This may be an indication of V_g for growing stoichiometric CdSe layers.

3.2.5 Scanning electron microscopy (SEM)

Scanning electron microscopy was used to investigate the surface morphology, the range of the grain sizes and the average thickness of CdSe layer grown on FTO substrates. SEM is a useful tool to study microstructure of thin films [14]. Figure 11a shows that the surface of AD-CdSe film is uniformly covered by large numbers of spherical grains without pinholes. The obtained micrographs of AD-CdSe layers reveal compact films of regular morphology. Figure 11b shows the presence of pinholes on the surface of the HT film; these pinholes are due to sublimation of excess Se element in the CdSe layer that arises as a result of the high annealing temperature of 380 °C for longer duration of 30 min.

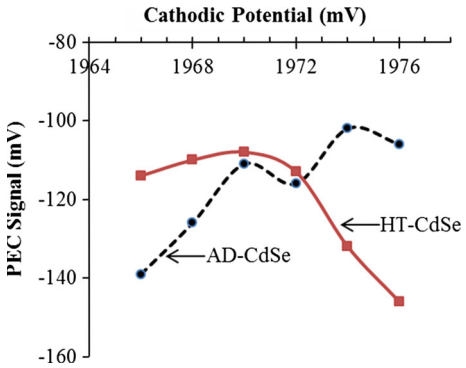

Fig. 10 Variation of PEC signals for CdSe/electrolytic junctions as a function of growth voltage, indicating n-type electrical conduction

Figure 12a, b show the SEM images of AD- and HT-CdSe grown at a shorter duration of 5 min. In Fig. 12a, the grain size of the AD-CdSe layer ranges from 27 to 320 nm while in Fig. 12b, the grain size of HT-CdSe layer ranges from 72 to 360 nm. The minimum and maximum grain sizes of HT-CdSe are greater than those of the AD-CdSe. This increase in grain size may be attributed to the annealing parameters (temperature and time) used. Both images show that the whole surface of the substrate is more compact together with absence of pinholes. The SEM cross-section illustrated in Fig. 13 gives the average film thickness of CdSe layer as 156 nm comparable with the theoretical value of 154 nm which was calculated using Faraday's laws of electrolysis. The thickness of SiO_2 and FTO from Fig. 13 are 18 and 196 nm respectively.

3.2.6 Atomic force microscopy (AFM)

Figure 14 shows AFM pictures of annealed CdSe deposited at 1,972 mV on glass/FTO substrates. The AFM images reveal the presence of large and dense agglomeration of small grains with good cementing effect. The layers produce pinholes free material suitable for buffer, window and absorber materials in thin film solar cells.

3.2.7 Thickness of ED-CdSe layers

A fore knowledge of thickness of thin film materials is important before device fabrication. This is essential because thickness affects device performance most especially in thin film solar cells. CdSe can be used as an n-type

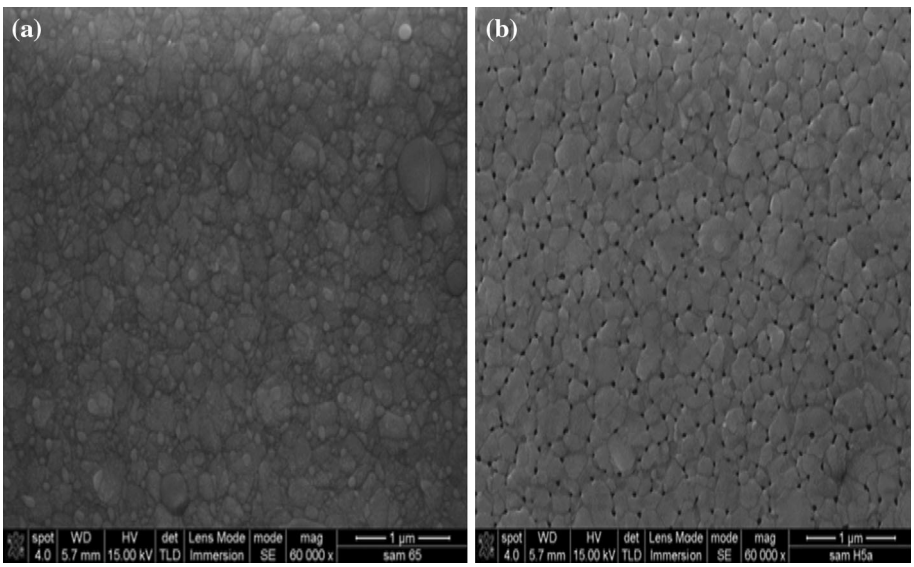

Fig. 11 SEM images of CdSe thin films on FTO substrates grown at $V_g = 1{,}972$ mV and $t_g = 30$ min. Surface morphology of **a** AD-CdSe and **b** CdSe heat-treated at 380 °C for 30 min in air

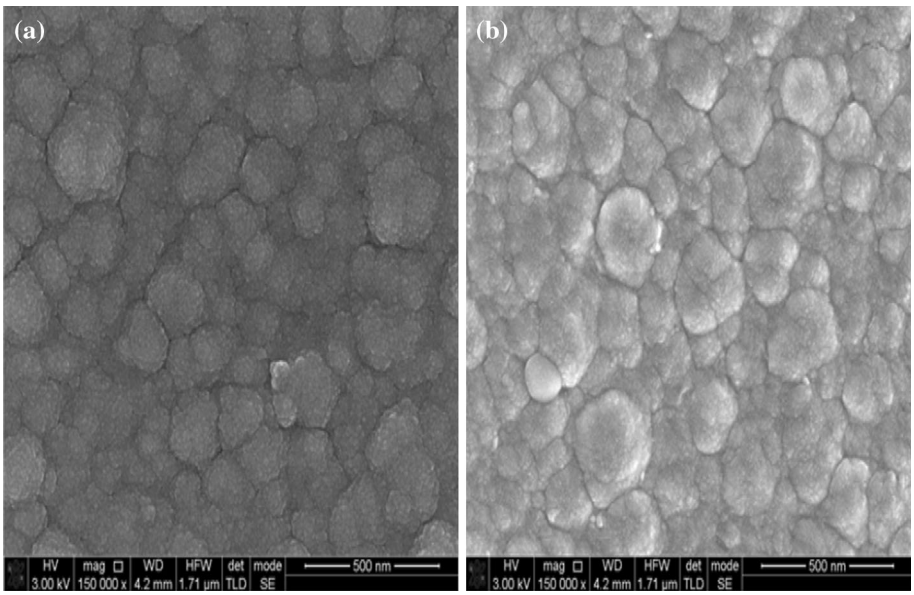

Fig. 12 SEM images of CdSe thin film on FTO substrate grown at $V_g = 1{,}972$ mV for $t_g = 5$ min. **a** Surface morphology of AD-CdSe with grain size ranging from 27 to 320 nm and **b** surface morphology of HT-CdSe at 250 °C for 10 min in air with grain size ranging from 72 to 360 nm

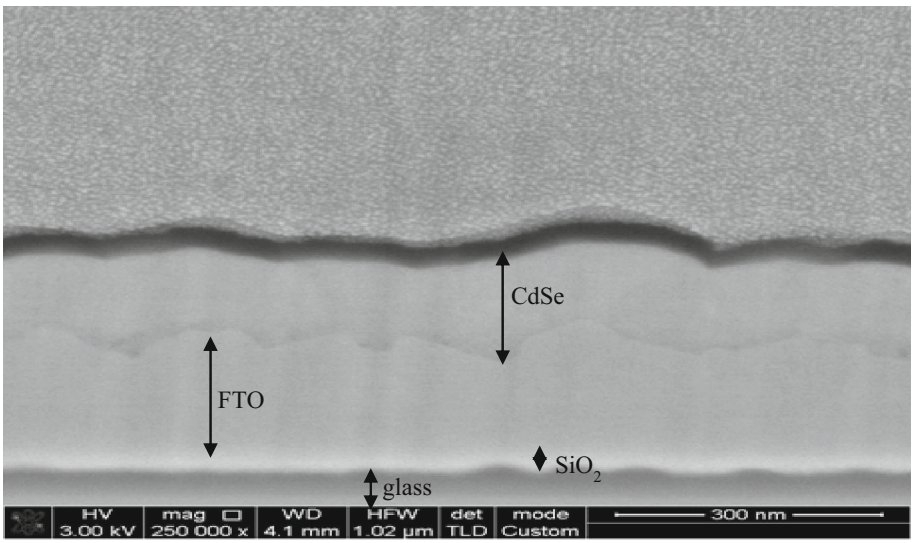

Fig. 13 Cross-section of CdSe thin film grown on FTO substrate and heat-treated at 250 °C for 10 min in air ($V_g = 1{,}972$ mV and $t_g = 5$ min.) (Courtesy: G.J. Russel microscopy center at University of Durham, UK)

buffer, window or absorber layer in thin film solar cells by selecting its thickness appropriately. In this study, different thicknesses of cadmium selenide were obtained by using deposition times in the range (5–30) min at a constant deposition potential of 1,972 mV. The thicknesses obtained by using Microfocus Optical Thickness Profilometer measurement system was compared with the theoretical estimate obtained using Faraday's laws of electrolysis as illustrated in Fig. 15. Faraday's law used in the theoretical thickness estimation is given by Eq. (7) [23].

$$T = \frac{JtM}{nF\rho} \tag{7}$$

where T is the thickness of the CdSe film, J is average deposition current density, F is Faraday's constant, t is the deposition time, M is the molecular weight of CdSe, n is the number of electrons transferred in the reaction for the formation of 1 mol of CdSe ($n = 6$ as given by Eqs. 4a, 4b, 4c, 5) and ρ is the density of CdSe.

Figure 15 shows that the thickness of AD-CdSe increases as the deposition time increases. The result shows an approximate linear variation of thickness with deposition time for the experimental curve while in the theoretical curve, a non-linear response is observed. This non-linear behaviour may be due to variation of current density with deposition time during growth period. As shown in Fig. 15, the thickness of ED-CdSe layer grown for 15 min shows a value of approximately 0.80 µm (800 nm) when measured using the thickness profilometer while the theoretical estimate using Faraday's equation gave an approximate value

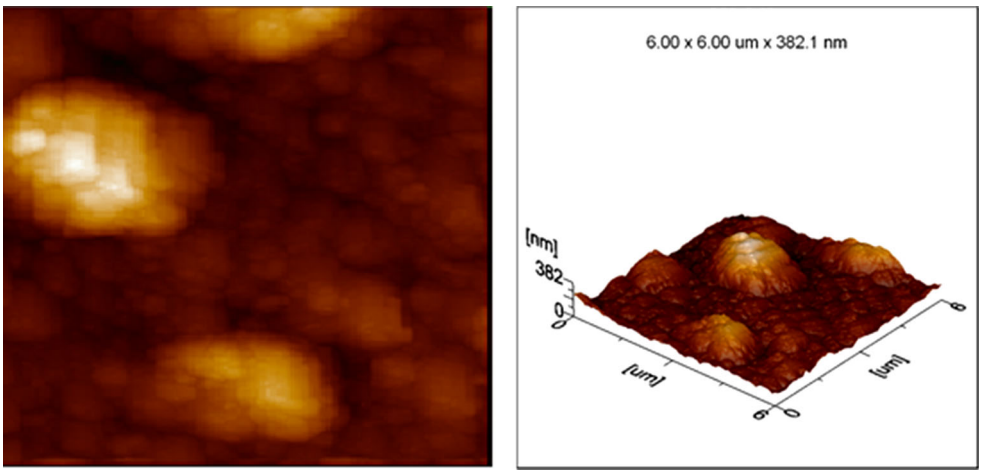

Fig. 14 Typical AFM images of annealed ED-CdSe grown at 1,972 mV on glass/FTO substrate (Courtesy: Institute of Organic Catalysis and Electrochemistry, Almaty, Kazakhstan)

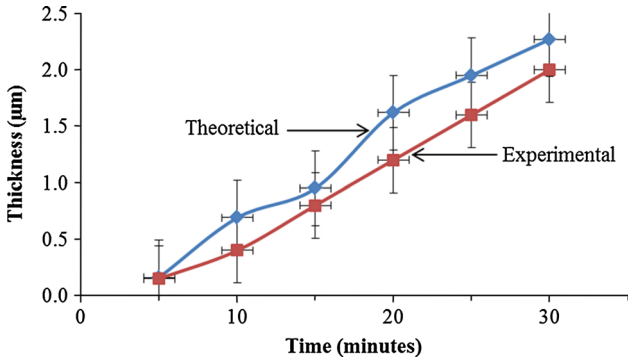

Fig. 15 Estimated experimental and theoretical values of thickness for CdSe layers as a function of growth period

of 0.95 μm (950 nm). The discrepancy between the theoretical estimate and measured value may be due to the fact that not all the electronic charges used in the theoretical estimate are actually involved in the deposition of CdSe. Part of these electronic charges flow through the electrolyte to take part in the electrolysis of water; hence, the observed thicknesses from experimental results are lower than the theoretical values [23]. One of the main advantages of CdSe is the growth of 2.0 μm layer in a short period of ~30 min. This is a very important factor for lowering the manufacturing cost of solar cells.

3.3 Testing of electronic quality of ED-CdSe layers

In order to test the electronic quality of ED-CdSe layers, Schottky barrier diodes of the structure glass/FTO/n-CdSe/Au (Fig. 16a) were fabricated and tested using current–voltage (I–V) technique. Figure 16b shows the energy band diagram for the metal semiconductor (MS) structure formed at n-CdSe/Au interface. The potential barrier height formed at the junction between the CdSe semiconductor and Au metal contact is also illustrated. CdSe layers grown for durations less than or equal to 5 min were very transparent thus allowing them to be used as buffer and window layers. However, no diode behaviour was observed when the CdSe layers were grown for this short duration. For this reason, the growth duration was further optimised to find a suitable time to grow CdSe layers that produce diodes with good rectification property. A good Schottky diode behaviour with high rectification factor was observed at 20 min growth time. For this growth time, film thickness is ~1.6 μm. The log-linear and the linear–linear I–V graphs under dark condition for the Schottky diodes are illustrated in Fig. 17a, b respectively.

The rectifying properties were produced by n-CdSe layers grown for 20 min, and heat treated at 200 °C for 10 min in air. Under these growth conditions, the Schottky barriers produced showed rectification factor (R.F.) ~$10^{2.9}$, ideality factor (n) in the range 1.44–2.57, potential barrier height (Φ_b) greater than 1.10 eV, series resistance (R_s) ~625 Ω, shunt resistance, (R_{sh}) → ∞, reverse saturation current (I_o) ~372 nA and threshold voltage ~0.15 V. The I–V results observed under AM1.5 (Air-Mass 1.5) illumination for glass/FTO/n-CdSe/Au structure reveal the photovoltaic activity of the Schottky barrier interface. The initial solar cell parameters observed are: $V_{oc} = 0.28$ V, $J_{sc} = 1.68$ mA/cm^2 and FF = 0.40. These properties indicate that electroplated CdSe layers possess electronic device qualities and our future research is directed towards development of thin film devices incorporating these layers.

4 Conclusion

The experimental results presented in this paper show that CdSe can be successfully grown using a 2-electrode system. XRD results have shown that the layers are hexagonal and polycrystalline with preferential orientation along the

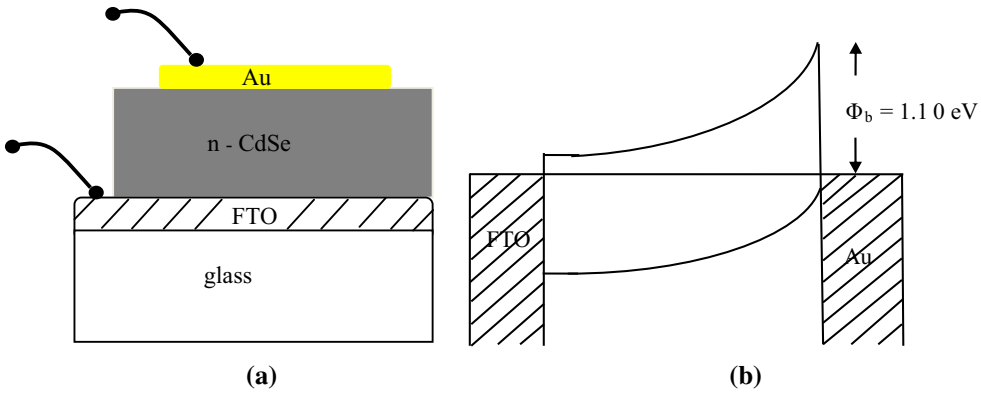

Fig. 16 **a** Schematic diagram of the n-CdSe/Au Schottky diodes and **b** energy band diagram of n-CdSe/Au Schottky diodes

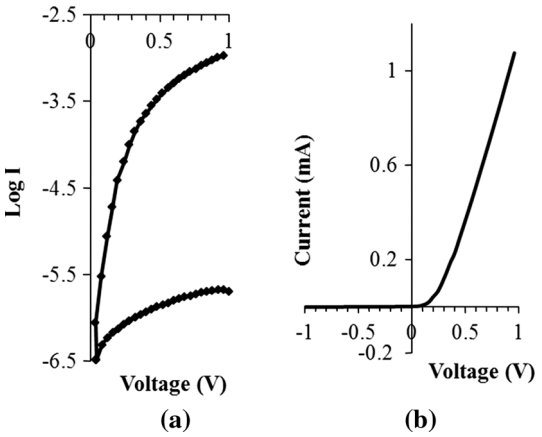

Fig. 17 I–V Characteristics of n-CdSe/Au Schottky diodes under dark conditions **a** the log-linear I–V and **b** the linear–linear I–V

(002) plane. Depending on the thickness of the layer, CdSe can be useful in thin film PV development for use as a window, buffer or absorber material. PEC study reveals that the films have n-type electrical conductivity. The results obtained from the optical absorption measurement show that ED-CdSe layers have direct band gaps in the range (1.80–2.00) eV for AD and (1.75–1.90) eV for HT thin films. n-CdSe/Au Schottky barriers show the electronic device quality of ED-CdSe layers. The wetting property of compounds containing Se and the ability of the CdSe layer to grow within a very short period of time with good electronic quality thus make it very attractive in thin film solar cell development. Work is continuing to develop multi-layer graded bandgap solar cells incorporating electroplated CdSe layers.

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References

1. L.J. Zhao, L.F. Hu, X.S. Fang, J. Adv. Funct. Mater. **22**, 1551–1566 (2012)
2. M.A. Hernandez-Perez, J. Aguilar-Hernandez, G. Contreras-Puente, J.R. Vargas-Garcıa, E. Rangel-Salinas, Phys. E **40**, 2535–2539 (2008)
3. K. Sharma, A.S. Al-Kabbi, G.S.S. Saini, S.K. Tripathi, Mater. Res. Bull. **47**, 1400–1406 (2012)
4. S.S. Kale, C.D. Lokhande, Mater. Chem. Phys. **62**, 103 (2000)
5. P.P. Hankare, V.M. Bhuse, K.M. Garadkar, S.D. Delekar, I.S. Mulla, Semicond. Sci. Technol. **19**, 70 (2004)
6. T. Elango, V. Subramanian, K.R. Murali, Surf. Coat. Technol. **123**, 8–11 (2000)
7. A.A. Yadav, M.A. Barote, E.U. Masumdar, Mater. Chem. Phys. **121**, 53–57 (2010)
8. S.J. Lade, M.D. Uplane, C.D. Lokhande, Mater. Chem. Phys. **68**, 36 (2001)
9. Y. Golan, L. Margulis, I. Rubinstein, G. Hodes, Langmuir **8**(3), 749–752 (1992)
10. E. Benamar, M. Rami, M. Fahoume, F. Chiraibi, A. Ennaoui, Ann. Chim. Sci. Mater. **23**, 369 (1998)
11. C.D. Lokhande, E.-H. Lee, K.-D. Jung, O.-S. Joo, Mater. Chem. Phys. **91**, 399 (2005)
12. S. Thanikaikarasan, T. Mahalingam, M. Raja, T. Kim, Y.D. Kim, J. Mater. Sci. Mater. Electron. **20**, 727–734 (2009)
13. S. Thanikaikarasan, K. Sundaram, T. Mahalingam, S. Velumani, J.-K. Rhee, J. Mater. Sci. Eng. B **174**, 242–248 (2010)
14. S.M. Pawar, A.V. Moholkar, K.Y. Rajpure, C.H. Bhosale, J. Phys. Chem. Solids **67**, 2386–2391 (2006)
15. M.D. Athanassopoulou, J.A. Mergos, M.D. Palaiologopoulou, T.G. Argyropoulos, C.T. Dervos, Thin Solid Films **520**, 6515–6520 (2012)
16. I.M. Dharmadasa, J. Haigh, J. Electrochem. Soc. **153**(1), G47–G52 (2006)
17. I.M. Dharmadasa, R.P. Burton, M. Simmonds, Sol. Energy Mater. Sol. Cells **90**, 2191–2200 (2006)
18. Y.G. Gudage, N.G. Deshpande, R. Sharma, J. Phys. Chem. Solids **70**, 907–915 (2009)
19. J. Sun, D.K. Zhong, D.R. Gamelin, Energy Environ. Sci. **3**, 1252–1261 (2010)
20. S.G. Bratsch, J. Phys. Chem. Ref. Data **18**(1), 1–21 (1989)

21. H. Uwe, G. Neil, Nat. Nanotechnol. **6**, 534 (2011)
22. A. Brioude, J. Bellessa, S. Rabaste, B. Champagnon, L. Sphanel, J. Mugnier, J.C. Plenet, J. Appl. Phys. **95**(5), 2744–2748 (2004)
23. F. Fauzi, D.G. Diso, O.K. Echendu, V. Patel, Y. Purandare, R. Burton, I.M. Dharmadasa, Semicond. Sci. Technol. **28**, 045005 (2013). doi:10.1088/0268-1242/28/4/045005