

SMART Cast-Monocrystalline p-Type Silicon Passivated Emitter and Rear Cells: Efficiency Benchmark and Bulk Lifetime Analysis

Stephan Maus,* Felix Maischner, Stephan Riepe, Johannes Greulich, Elmar Lohmüller, Florian Schindler, Pierre Saint-Cast, Patricia Krenckel, Adam Hess, Sabrina Lohmüller, Andreas Wolf, and Ralf Preu

Herein, boron-doped cast-monocrystalline silicon wafers that have been fabricated using the Seed Manipulation for ARTificially controlled defect Technique (SMART mono-Si) are examined. Their suitability for passivated emitter and rear cell (PERC) fabrication is investigated. Applying a zero busbar layout energy conversion efficiencies of $\eta = 21.9\%$ for SMART mono-Si, $\eta = 22.2\%$ for gallium-doped Cz-Si (Cz-Si:Ga), and $\eta = 22.3\%$ for boron-doped Cz-Si (Cz-Si:B) are achieved at similar doping levels between $0.7 \Omega \text{ cm} \leq \rho_B \leq 1.0 \Omega \text{ cm}$. Therefore, SMART mono-Si PERCs show almost the same performance as Cz-Si PERCs. Apart from the performance of SMART mono-Si PERCs, the minority charge carrier bulk lifetime τ_B of the SMART mono-Si wafers after different high-temperature process steps in the PERC process flow is investigated. After emitter formation, this analysis confirms the high material quality of SMART mono-Si yielding $\tau_B \approx 1.3 \text{ ms}$ at an injection level of $\Delta n = 10^{15} \text{ cm}^{-3}$. The bulk lifetime after firing is similar to the level determined for mCz-Si:B and Cz-Si:Ga reference wafers of similar doping level.

1. Introduction


In recent years, a clear market trend toward using Czochralski-grown silicon (Cz-Si) in manufacturing of passivated emitter and rear cells (PERC) has taken place.^[1] In addition to a higher material quality of Cz-Si and thus higher cell efficiencies compared with multicrystalline silicon (mc-Si), the reason for

this trend is a decrease in the price of Cz-Si material. Nevertheless, it is assumed that between both materials a gap in power consumption for the crystallization of silicon material of more than 15 kWh kg^{-1} will remain for the next years.^[1] To reach a sustainable PERC cell production with low electricity consumption, and therefore lower CO_2 emission^[2] as well as lower costs, there is a demand for material, which includes both advantages of mc-Si and Cz-Si: low power consumption for its fabrication and high material quality, which will lead to lowering production costs while still obtaining high cell efficiencies.

Cast-monocrystalline silicon material has been suggested to serve that demand and has been intensively investigated in the past.^[3–10] However, despite the excellent material quality achieved, this material suffers from unwanted ingrowth of parasitic grains from the crucible into the ingot volume,^[11] which reduce the material quality significantly. This leads to yield losses and therefore to higher fabrication costs, which cannot be compensated by higher solar cell efficiencies. To suppress the ingrowth of parasitic grains, a highly convex growth interface can be used.^[12,13] However, a highly convex growth interface can lead to high thermal stress and thus the occurrence of detrimental dislocation clusters in the ingot volume.^[13]

A new technique to reduce the unwanted ingrowth of parasitic grains as well as the formation of significant dislocation clusters in cast-monocrystalline silicon material is the Seed Manipulation for ARTificially controlled defect Technique (SMART), which was first published by Takahashi et al. in 2015^[14] and with substantial progress reported by Riepe et al. in 2019.^[11] The SMART technique uses functional defects for blocking parasitic grains, which enables the usage of a slightly convex growth interface. Thereby, the functional defects are introduced by a silicon plate system, which is placed between a Cz-Si spacer plate to the crucible wall and the Cz-Si seed plates. That results in a complete blocking of parasitic grains as well as low thermal stress in the brick volume.^[11] Just recently, a certified peak energy conversion efficiency of 23.3% for n-type SMART cast-monocrystalline silicon (SMART mono-Si) TOPCon cells has been reported,^[2] which demonstrates the high quality of this material. Consequently,

S. Maus, F. Maischner, Dr. S. Riepe, Dr. J. Greulich, Dr. E. Lohmüller, Dr. F. Schindler, Dr. P. Saint-Cast, Dr. P. Krenckel, A. Hess, S. Lohmüller, Dr. A. Wolf, Dr. R. Preu
Photovoltaic Production Technology
Fraunhofer Institute for Solar Energy Systems (ISE)
Heidenhofstrasse 2, Freiburg 79110, Germany
E-mail: stephan.maus@ise.fraunhofer.de

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/solr.202000752>.

© 2021 The Authors. Solar RRL published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution-NonCommercial-NoDerivs License, which permits use and distribution in any medium, provided the original work is properly cited, the use is non-commercial and no modifications or adaptations are made.

DOI: 10.1002/solr.202000752

SMART mono-Si might be a more sustainable and inexpensive alternative to Cz-Si in PERC production.

In this work, we investigate the suitability of boron-doped SMART mono-Si for p-type PERC fabrication with respect to p-type Cz-Si reference wafers. Moreover, we investigate the minority charge carrier bulk lifetime of the different material types after different high-temperature process steps in the PERC process flow, such as emitter formation and contact firing.

2. Sample Preparation

As reported by Riepe et al.,^[11] we manufacture two boron-doped SMART mono-Si ingots in a G2 crucible with a base resistivity $0.7 \Omega\text{cm} \leq \rho_B \leq 0.9 \Omega\text{cm}$ for ingot 1 and $1.2 \Omega\text{cm} \leq \rho_B \leq 1.5 \Omega\text{cm}$ for ingot 2. For each ingot, 30 mm-thick Cz-Si seed plates with rotated crystallographic orientation (seed A and seed B) are placed in the crucible, as shown in **Figure 1a**. Between the seed

plates and the crucible wall, a 40 mm-wide spacer Cz-Si plate as well as the SMART silicon plate system is placed. The crystallization is performed using a laboratory vertical gradient freeze furnace, leading to a 210 mm high ingot. For more information about the manufacturing and characterization of these SMART mono-Si ingots, see Riepe et al.^[11] After crystallization, a brick from the center part of each G2 ingot is cut (brick 1 and brick 2) and sawn into full-square wafers with 156.6 mm edge length and a thickness of 190 μm , which contain parts of all four seed plates (see **Figure 1b**). It is important to mention that in an industrial approach, larger Cz-Si seed plates would be used, which ensure that the bricks can be cut along the grain boundaries, resulting in complete monocrystalline bricks. Furthermore, an “inner grain” appears and slightly grows with increasing brick height. All wafers of both bricks manufactured in this experiment are affected by this unwanted effect. For this experiment, we investigate SMART mono-Si wafers from three heights of each brick, i.e., 100, 140, and 175 mm, in the following denoted as bottom, center, and top, respectively.

Using the SMART mono-Si of both bricks and all three heights, we manufacture PERCs using a process flow similar to the Fraunhofer ISE PVTEC baseline,^[15] which includes an alkaline texture, an Al_2O_3 rear passivation, a local contact opening (LCO) via laser ablation, and a full aluminum metallization (no silver pads) on the rear side, as well as a five busbar (5BB) layout for the front side metallization. In a parallel processed batch, we also manufacture 5BB PERCs using boron-doped magnetically cast Cz-Si (mCz-Si:B) wafers, which are taken as a reference for the SMART mono-Si PERCs.

In a second batch, we manufacture PERCs using a zero busbar (0BB) layout for the front side metallization as well as adapted processes for front and rear side passivation. In this second batch, SMART mono-Si wafers of brick 1 with $0.7 \Omega\text{cm} \leq \rho_B \leq 0.8 \Omega\text{cm}$ are used, as well as boron-doped Cz-Si (Cz-Si:B with $\rho_B = 0.8 \Omega\text{cm}$) and gallium-doped Cz-Si (Cz-Si:Ga with $\rho_B = 1.0 \Omega\text{cm}$) wafers as reference. Thus, this batch does not contain a mCz-Si:B reference group due to limited experimental resources.

To investigate the minority charge carrier bulk lifetime τ_B (in the following denoted as bulk lifetime) of the SMART mono-Si after two high-temperature process steps in the PERC process flow, we manufacture bulk lifetime samples. These high-temperature process steps are emitter formation via phosphorus diffusion using POCl_3 as dopant precursor and contact firing. For this investigation, mCz-Si:B material ($\rho_B = 1.3 \Omega\text{cm}$) and Cz-Si:Ga ($\rho_B = 1.2 \Omega\text{cm}$) are used as reference to the SMART mono-Si material. All base resistivities mentioned in this article are measured after thermal donor annihilation.^[16] For the determination of τ_B after the phosphorus diffusion process ($\tau_{B,\text{diff}}$), samples after diffusion are etched in hydrofluoric acid (HF) and caustic potash (KOH) to remove the phosphosilicate glass and the diffused emitter, respectively, on both sides. For determining τ_B after firing ($\tau_{B,\text{fire}}$), we manufacture nonmetallized cell test structures, which are processed analogously to the PERCs until surface passivation without local contact opening and without metallization. These samples are fired, characterized using quasi-steady-state photoconductance (QSSPC) measurements to determine the implied open-circuit voltage (iV_{OC}), and afterward etched in HF and KOH to remove

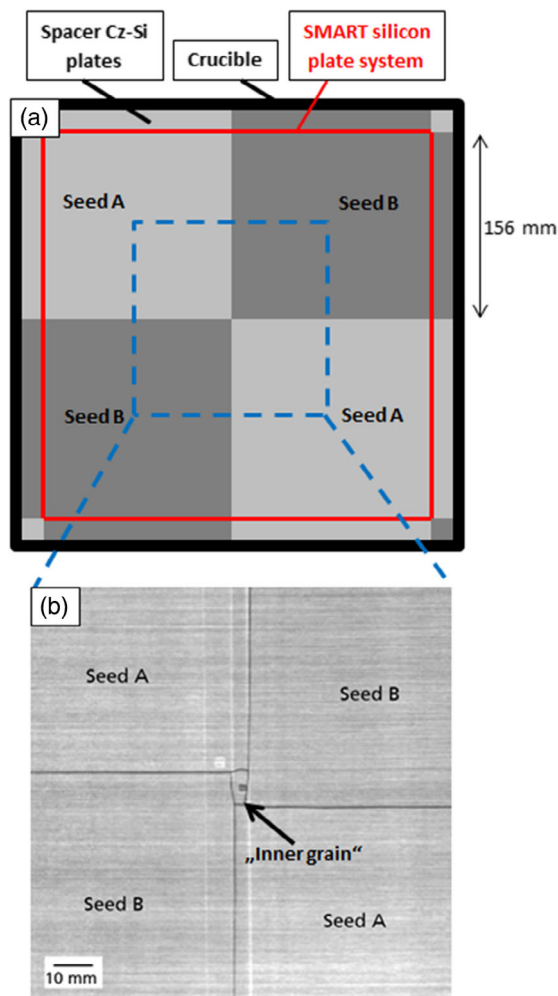


Figure 1. a) Sketch of the G2 crucible with depicted positioning of the seed plates A and B, the spacer Cz-Si plates, SMART silicon plate system (red solid square), and brick cutting position (blue dashed square). b) A photoluminescence image of an exemplary wafer in as-cut state showing the vertical and horizontal grain boundaries, an “inner grain” and two data-matrix codes at the sample center.

the passivation layers, the front texture, and the emitter. Both groups of bulk lifetime samples ($\tau_{B,diff}$ and $\tau_{B,fire}$) are then passivated using a 20 nm-thick layer of Al_2O_3 , which is activated in a forming gas anneal at a temperature of 400 °C for 10 min. A QSSPC analysis yields the implied open-circuit voltage of the τ_B samples $iV_{OC}(\tau_B)$ as well as the bulk lifetimes $\tau_{B,diff}$ and $\tau_{B,fire}$, neglecting residual surface recombination. This analysis is performed after storage of the samples in the dark right after the forming gas anneal to avoid a formation of boron oxygen defects.^[17] Hence, the interstitial iron, which might be present in the samples, is in associated state (FeB and FeGa) during these measurements. To measure the concentration of interstitial iron $[Fe_i]$, a method based on microwave detected photoconductance (MDP)^[18] is used. This tool uses the defect model by Rein and Glunz^[19] for the calculation of $[Fe_i]$ in boron-doped material. All investigated materials are measured using this setup. However, for Cz-Si:Ga the measurements are afterward corrected using the parameterization reported by Schmidt and Macdonald.^[20] Furthermore, an efficiency limiting bulk recombination analysis (ELBA)^[21,22] is performed to determine the bulk-related efficiency loss. This analysis is based on a Quokka3^[23] simulation, using injection-dependent lifetime images from PLI measurements of the bulk lifetime samples as input data.

3. Results and Discussion

In Figure 2a, the results of $\tau_{B,diff}$ and $\tau_{B,fire}$ are shown for all investigated materials at an injection level of $\Delta n = 10^{15} \text{ cm}^{-3}$. As the doping concentration influences τ_B , only materials with roughly the same ρ_B should be regarded for comparison. This holds for the SMART mono-Si material from the top of brick 2, the mCz-Si:B as well as the Cz-Si:Ga reference material with $1.2 \Omega\text{cm} \leq \rho_B \leq 1.3 \Omega\text{cm}$. After emitter formation the SMART mono-Si ($\tau_{B,diff} \approx 1.1 \text{ ms}$) outperforms the mCz-Si:B material ($\tau_{B,diff} \approx 0.5 \text{ ms}$). Nevertheless, the Cz-Si:Ga with $\tau_{B,diff} = 1.9 \text{ ms}$ exceeds both. The SMART mono-Si of brick 1 shows a lower $\tau_{B,diff} \approx 0.5 \text{ ms}$, which can be attributed to the lower base resistivity of $0.7 \Omega\text{cm} \leq \rho_B \leq 0.8 \Omega\text{cm}$. To compare the electrical properties of all materials independent of base resistivity, the implied open-circuit voltage of the τ_B samples $iV_{OC}(\tau_B)$ is shown in Figure 2b. After emitter formation $iV_{OC}(\tau_{B,diff}) \approx 730 \text{ mV}$ for SMART mono-Si of both bricks and all heights is similar to mCz-Si:B, while Cz-Si:Ga outperforms both materials ($iV_{OC}(\tau_{B,diff}) \approx 740 \text{ mV}$). The passivation and firing sequence during PERC processing decreases τ_B and $iV_{OC}(\tau_B)$ for SMART mono-Si and Cz-Si:Ga ($\tau_{B,fire} < \tau_{B,diff}$), whereas both increase for the mCz-Si:B material, which is discussed later. Thus, after the passivation and firing sequence we find a similar level of $\tau_{B,fire} \approx 0.8 \text{ ms}$ at similar ρ_B for the top of SMART brick 2, mCz-Si:B, and Cz-Si:Ga. In that state, all materials show $720 \text{ mV} \leq iV_{OC}(\tau_{B,fire}) \leq 730 \text{ mV}$, whereas a slight advantage is visible for the Cz-Si materials.

We perform a contamination analysis to investigate the observed decrease in τ_B along the PERC process flow. This analysis is performed after storage of the samples in the dark for 48 h and at an injection level of $\Delta n \approx 10^{15} \text{ cm}^{-3}$. Figure 3 shows the interstitial iron concentration $[Fe_i]$ for the top of SMART brick 1, the center of SMART brick 2, mCz-Si:B, and Cz-Si:Ga.

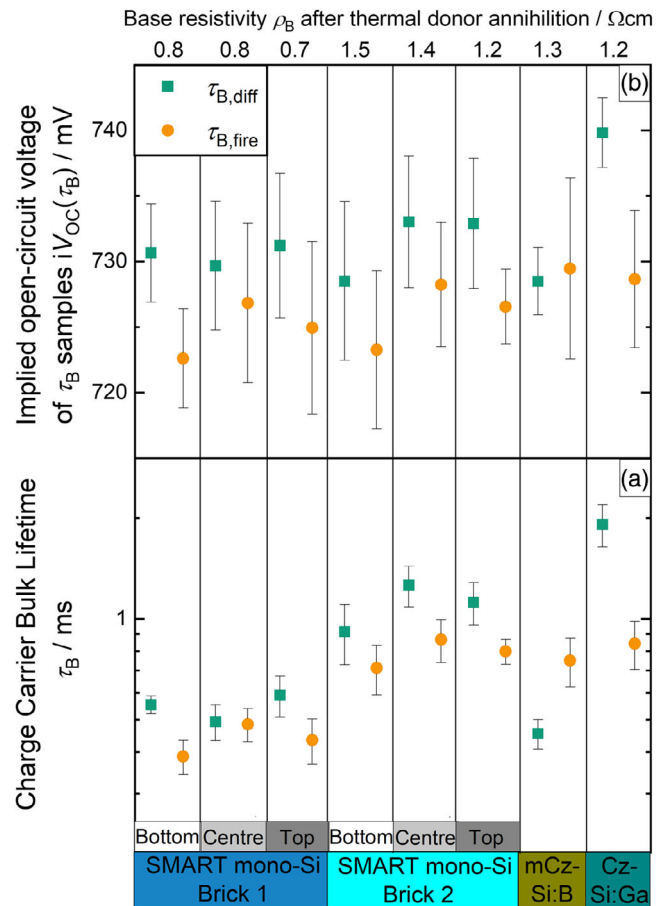


Figure 2. a) Bulk lifetime at an injection level of $\Delta n = 10^{15} \text{ cm}^{-3}$ and b) implied open-circuit voltage (both in FeB and FeGa state). Both for τ_B samples after diffusion ($\tau_{B,diff}$) and firing ($\tau_{B,fire}$) measured with QSSPC on five positions of three samples per group. The base resistivities ρ_B for all investigated material types are given above the graph.

Note that a direct comparison of the absolute $[Fe_i]$ between the boron- and gallium-doped material is not admissible because two different defect models are considered. For all materials $[Fe_i]$ increases due to the passivation and firing sequence ($\tau_{B,fire}$). As all materials are affected, an external iron contamination, originating from one of the performed processes after emitter formation, is assumed as the root cause. To investigate the correlation between the decrease in τ_B and the iron contamination, the Shockley–Read–Hall (SRH) recombination rate ΔR_{Fe} is calculated based on the measured $[Fe_i]$, using the defect model by Rein and Glunz.^[19] Note that also for Cz-Si:Ga the measured (not the corrected) $[Fe_i]$ is used to ensure the consistency of the calculation. In addition, the change in bulk recombination between diffusion and firing

$$\Delta R_{meas} = \tau_{B,fire}^{-1} - \tau_{B,diff}^{-1} \quad (1)$$

is derived for the QSSPC-measured τ_B values. Figure 4 compares the recombination rate ΔR_{Fe} expected from the iron content and the measured rate ΔR_{meas} . For the top of SMART brick 1, the center of SMART brick 2, and the Cz-Si:Ga material, the ΔR_{Fe} is lower than ΔR_{meas} . Hence, the iron contamination

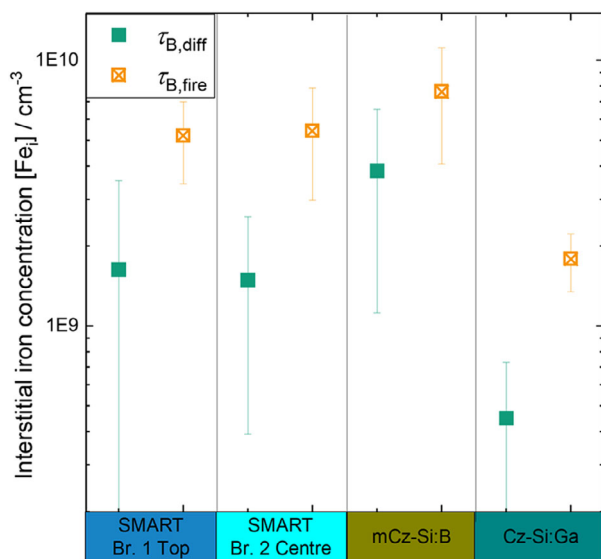


Figure 3. Average value and standard deviation (error bars) of the interstitial iron concentration $[Fe_i]$ measured by a MDP map for one sample per group for SMART mono-Si (top of brick 1 and center of brick 2), mCz-Si:B, and Cz-Si:Ga. For Cz-Si:Ga, the values are corrected using a defect model for FeGa.^[20]

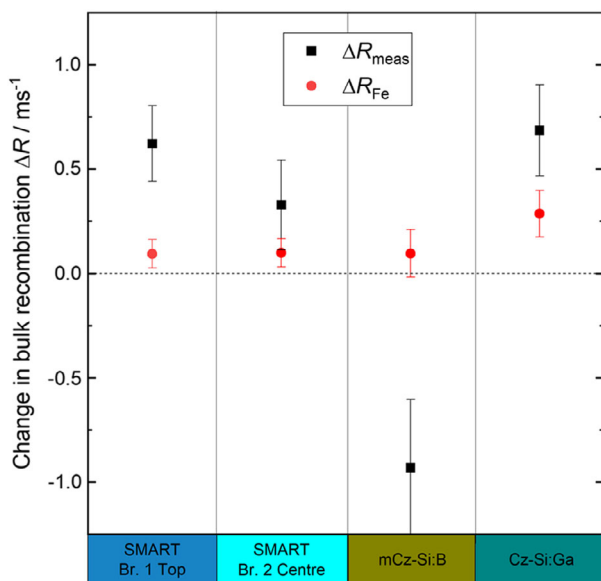


Figure 4. Change in bulk recombination between diffusion and firing (both in FeB and FeGa state) for one sample per group for SMART mono-Si (top of brick 1 and center of brick 2), mCz-Si:B, and Cz-Si:Ga, derived by Equation (1) from QSSPC measured bulk lifetimes (ΔR_{meas}) and calculated from the determined Fe_i concentrations using literature data from Rein and Glunz^[19] (ΔR_{Fe}).

can only partially explain the decrease in τ_B due to the passivation and firing sequence. One explanation for the difference between the ΔR values could be the presence of other impurities or the occurrence of light- and elevated temperature-induced degradation (LeTID) during firing.^[24] However, for mCz-Si:B a

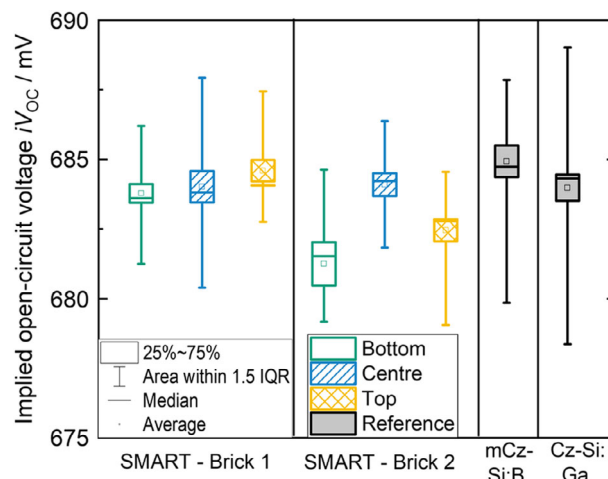


Figure 5. Implied open-circuit voltage (iV_{OC}) for all investigated material types, measured on a nonmetallized cell test structure by QSSPC on five positions of three samples per group.

negative ΔR_{meas} can be found, leading to the assumption that another (positive) effect on τ_B is overlaying the influence of $[Fe_i]$. The origin of this effect is not yet understood.

The cell test structures exhibit implied open-circuit values in the range $681 \text{ mV} \leq iV_{OC} \leq 685 \text{ mV}$ for all materials, as shown in **Figure 5**. This is consistent with the $iV_{OC}(\tau_{B,\text{fire}})$ data (see Figure 2b), which also showed similar iV_{OC} levels. The Cz-Si materials show a larger area within the 1.5 interquartile range (IQR) (see Figure 5) compared with the SMART mono-Si, which can be explained by handling defects and is not attributed to the material itself. The decrease in iV_{OC} compared with $iV_{OC}(\tau_{B,\text{fire}})$ is attributed to recombination losses at the phosphorus emitter (dark saturation current density $j_{0e} \approx 70 \text{ fA cm}^{-2}$; emitter sheet resistance $R_{\text{sheet}} \approx 93 \Omega \text{ sq}^{-1}$) and the rear side passivation. The SMART mono-Si wafers from the top of brick 1 as well as the mCz-Si:B material show the highest $iV_{OC} \approx 685 \text{ mV}$. Using these both materials, we achieve peak energy conversion efficiencies of $\eta = 21.5\%$ for 5BB SMART mono-Si and $\eta = 21.6\%$ for 5BB mCz-Si:B PERCs (see **Table 1**). The lower doping concentration of the mCz-Si:B cell compared with the SMART mono-Si cell and the usage of the same LCO pitch of $450 \mu\text{m}$ for both lead to a higher series resistance R_s for the mCz-Si:B cell. Due to the almost similar pseudo fill factor (pFF), this difference in R_s results in a lower FF for the mCz-Si:B cell. The efficiency standard deviation over all cells manufactured using wafers of SMART brick 1 (bottom, center, and top) is $\Delta\eta_{SD} = 0.08\%_{\text{abs}}$. This shows the constant high quality of the SMART mono-Si material along the brick height and gives a first impression of the possible yield.

However, avoiding the decrease in τ_B due to the passivation and firing sequence might enable an even higher efficiency for the SMART mono-Si PERC cells. To determine the potential gain in efficiency by avoiding the observed decrease in τ_B , an ELBA is performed using PLI measurements of one bulk lifetime sample after emitter formation ($\tau_{B,\text{diff}}$) as well as after the passivation and firing sequence ($\tau_{B,\text{fire}}$). The difference between both yields a potential efficiency gain of $0.25\%_{\text{abs}} \leq \Delta\eta \leq 0.35\%_{\text{abs}}$ for SMART mono-Si, if the used 5BB cell architecture is assumed.

Table 1. Current–voltage data of the most efficient SMART mono-Si as well as the most efficient Cz-Si PERC cell with 5BB and 0BB front side metallization layout.

Material	Front side layout	ρ_B [Ω cm]	$J_{sc}^{a)}$ [mA cm^{-2}]	$V_{oc}^{a)}$ [mV]	pFF ^{b)} [%]	$R_s^{b)}$ [Ω cm ²]	FF ^{a)} [%]	$\eta^{a)}$ [%]
SMART	5BB	0.7	39.7	669	83.2	0.42	81.1	21.5
mCz-Si:B	5BB	1.3	39.7	673	83.1	0.47	80.8	21.6
SMART	0BB	0.7	40.3	673	82.9	0.43	80.8	21.9
Cz-Si:Ga	0BB	1.0	40.3	676	83.2	0.44	81.3	22.2
Cz-Si:B	0BB	0.8	40.3	674	83.1	0.39	81.9	22.3

^{a)}Measured by Fraunhofer ISE CalLab PV Cells; ^{b)}Measured using in-house IV tester.

In the second batch, where a 0BB layout for the front side metallization as well as adapted processes for front and rear side passivation is used, we achieve peak energy conversion efficiencies of $\eta = 21.9\%$ for SMART mono-Si, $\eta = 22.2\%$ for Cz-Si:Ga, and $\eta = 22.3\%$ for Cz-Si:B (see Table 1). This increase in efficiency mainly results from lower metallization fraction of 1.85% (screen opening) for the used 0BB cell architecture compared with 3.16% (screen opening) of the 5BB cell architecture, which leads to less shadowing and less recombination at the metal contacts. Therefore, the short-circuit current density (J_{sc}) as well as the V_{oc} increase. For the SMART mono-Si, the adapted front side passivation was found to decrease the bulk lifetime up to 30% compared with the not adapted passivation of the previous batch (5BB layout). This leads to a lower pFF for the SMART mono-Si compared with the Cz-Si materials (see Table 1), whereas the loss in V_{oc} is compensated through the aforementioned lower recombination at the metal contacts. Due to almost similar R_s , the lower pFF of the SMART mono-Si results in a lower FF and, therefore, to a lower η compared with the Cz-Si reference groups. This passivation-induced loss in bulk lifetime is not yet understood and will be analyzed in further research.

4. Summary

In a first batch, we show that SMART mono-Si exhibits electrical properties in terms of bulk lifetime τ_B and iV_{oc} similar to boron-doped magnetically cast Cz-Si (mCz-Si:B) and gallium-doped Cz-Si (Cz-Si:Ga). This results in a conversion efficiency $\eta = 21.5\%$ for SMART mono-Si 5BB PERCs and therefore shows almost the same performance compared with the reference group that uses mCz-Si:B wafers yielding a peak efficiency $\eta = 21.6\%$.

All material types exhibit an external iron contamination originating from a process subsequent to emitter formation. Furthermore, a decrease in τ_B due to the passivation and firing sequence is found for SMART mono-Si and Cz-Si:Ga. In addition to the iron contamination, a further bulk defect leading to this decrease is assumed, which might be the presence of other impurities or the occurrence of LeTID during firing. For the 5BB cell architecture, ELBA modeling shows a potential efficiency gain for SMART mono-Si of $0.25\%_{abs} \leq \Delta\eta \leq 0.35\%_{abs}$ if this decrease in τ_B can be avoided. This shows that the full potential of SMART mono-Si is not yet utilized.

In a second batch, where a 0BB layout for the front side metallization is used, we achieve a peak energy conversion efficiency of $\eta = 21.9\%$ for SMART mono-Si, $\eta = 22.2\%$ for Cz-Si:Ga, and $\eta = 22.3\%$ for Cz-Si:B at similar doping level ($0.7 \Omega \text{ cm} \leq \rho_B \leq 1.0 \Omega \text{ cm}$).

In conclusion, SMART mono-Si offers the opportunity to significantly reduce the power consumption for wafer production and delivers almost the same energy conversion efficiency of PERCs compared with Cz-Si. For that reason, SMART mono-Si is a promising alternative to Cz-Si and offers the potential to a more cost-effective and sustainable PERC production.

Acknowledgements

This work was funded by the German Federal Ministry for Economic Affairs and Energy BMWi in project “CUT-A PLUS” (contract number 0324282). The authors would like to thank the research teams at Fraunhofer ISE PV-TEC, especially J. Haunschild, J. Dalke, R. Post, S. Al-Hajjawi, and M. Pengerla for assistance with interstitial iron measurements.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

bulk, cast-monocrystalline silicon wafers, iron contamination, passivated emitter and rear cell, Seed Manipulation for Artificially controlled defect Technique, solar cells

Received: November 26, 2020

Revised: February 10, 2021

Published online: March 1, 2021

- [1] ITRPV Consortium, International Technology Roadman for Photovoltaic (ITRPV), 2020.
- [2] M. C. Schubert, F. Schindler, J. Benick, S. Riepe, P. Krenckel, A. Richter, R. Müller, B. Hammann, S. Nold, *Sol. Energy Mater. Sol. Cells* **2021**, 219, 110789.

- [3] N. Stoddard, B. Wu, I. Witting, M. C. Wagener, Y. Park, G. A. Rozgonyi, R. Clark, *SSP* **2007**, 131–133, 1.
- [4] M. Kivambe, B. Aissa, N. Tabet, *Energy Procedia* **2017**, 130, 7.
- [5] C. Y. Lan, Y. C. Wu, A. Lan, C. F. Yang, C. Hsu, C. M. Lu, A. Yang, C. W. Lan, *J. Cryst. Growth* **2017**, 475, 136.
- [6] Z. Liu, V. Vähänissi, H. S. Laine, M. Lindeberg, M. Yli-Koski, H. Savin, *Adv. Electron. Mater.* **2017**, 3, 1600435.
- [7] S. Nakano, B. Gao, K. Jiptner, H. Harada, Y. Miyamura, T. Sekiguchi, M. Fukuzawa, K. Kakimoto, *J. Cryst. Growth* **2017**, 474, 130.
- [8] E. Olsen, S. Bergan, T. Mehl, I. Burud, K. E. Ekstrøm, M. Di Sabatino, *Phys. Status Solidi A* **2017**, 214, 1700124.
- [9] P. Wang, C. Cui, D. Yang, X. Yu, *Sol. RRL* **2020**, 4, 1900486.
- [10] Y. Lv, Y. F. Zhuang, W. J. Wang, W. W. Wei, J. Sheng, S. Zhang, W. Z. Shen, *Sol. Energy Mater. Sol. Cells* **2020**, 204, 110202.
- [11] S. Riepe, P. Krenckel, Y. Hayama, A. Hess, T. Trötschler, K. Kutsukake, S. Maus, F. Schindler, N. Usami, in *36th EU PVSEC*, WIP GmbH & Co Planungs-KG, Munich, Germany **2019**, pp. 120–125.
- [12] B. Gao, S. Nakano, H. Harada, Y. Miyamura, T. Sekiguchi, K. Kakimoto, *J. Cryst. Growth* **2012**, 352, 47.
- [13] Y. Miyamura, H. Harada, K. Jiptner, J. Chen, R. R. Prakash, S. Nakano, B. Gao, K. Kakimoto, T. Sekiguchi, *J. Cryst. Growth* **2014**, 401, 133.
- [14] I. Takahashi, S. Joonwichien, T. Iwata, N. Usami, *Appl. Phys. Express* **2015**, 8, 105501.
- [15] S. Werner, E. Lohmüller, P. Saint-Cast, J. M. Greulich, J. Weber, S. Schmidt, A. Moldovan, A. A. Brand, T. Dannenberg, S. Mack, S. Wasmer, M. Demant, M. Linse, R. Ackermann, A. Wolf, R. Preu, in *33rd EU PVSEC*, WIP GmbH & Co Planungs-KG, Munich, Germany **2017**, pp. 406–412.
- [16] A. Borghesi, B. Pivac, A. Sassella, A. Stella, *J. Appl. Phys.* **1995**, 77, 4169.
- [17] T. Niewelt, M. Selinger, N. E. Grant, W. Kwapil, J. D. Murphy, C. Schubert, *J. Appl. Phys.* **2017**, 121, 185702.
- [18] M. Pengerla, S. Al-Hajjawi, V. Kuruganti, J. Haunschild, K. Schüler, S. Rein, in *37th EU PVSEC*, WIP GmbH & Co Planungs-KG, Munich, Germany **2020**.
- [19] S. Rein, S. W. Glunz, *J. Appl. Phys.* **2005**, 98, 113711.
- [20] J. Schmidt, D. Macdonald, *J. Appl. Phys.* **2005**, 97, 113712.
- [21] B. Michl, M. Rüdiger, J. A. Giesecke, M. Hermle, W. Warta, M. C. Schubert, *Sol. Energy Mater. Sol. Cells* **2012**, 98, 441.
- [22] B. Michl, M. Kasemann, W. Warta, M. C. Schubert, *Phys. Status Solidi RRL* **2013**, 7, 955.
- [23] A. Fell, J. Schön, M. C. Schubert, S. W. Glunz, *Sol. Energy Mater. Sol. Cells* **2017**, 173, 128.
- [24] W. Kwapil, L. Dalke, T. Niewelt, M. C. Schubert, in *37th EU PVSEC*, WIP GmbH & Co Planungs-KG, Munich, Germany **2020**.