Because the n^--regions are so short, carrier spillover occurs, so that the carrier density $n(x)$ depends on x in those regions. Using computer calculation the total number of carriers may be evaulated [4] in each of the n^--layers. Furthermore, Fig. 5 clearly indicates that $S_I(f)/I^2$ is independent of bias. Thus (1) can be used to calculate α.

The Hooge's constant is equal 1.95×10^{-6} at room temperature and 0.959×10^{-6} at liquid nitrogen temperature. This is about three orders of magnitude smaller than Hooge's original value of 2×10^{-3} but it is of the order of magnitude found for other materials [5], [6].

In a truly ballistic case (no collisions) there should be no scattering and hence no mobility fluctuation $1/f$ noise, so that α would be zero. The twofold decrease of α from 300 to 77 K may be due to this mechanism.

The $1/f^{0.5}$ behavior of noise spectrum at higher frequency can be explained by one-dimensional diffusion which increases with decrease of temperature. However, it is not known at present what is diffusing there.

Our data roughly agree with those obtained at the University of Florida [7].

References

[1] M. A. Hollis, N. Dandekar, L. F. Eastman, M. Shur, D. Woodard, R. Stall, and C. Wood, in *IEDM Tech. Dig.*, pp. 622-625, 1980.
[2] A. van der Ziel and G. Bosman, to be published.
[3] F. N. Hooge, *Physica (Utrecht)*, vol. 60, p. 130, 1972.
[4] A. van der Ziel *et al.*, to be published.
[5] H. I. Hanafi and A. van der Ziel, *Physica (Utrecht)*, vol. 94B, p. 351, 1978.
[6] G. Bosman, "Charge transport noise in monocrystalline silicon," Ph.D. thesis, University of Utrecht, The Netherlands, 1981.
[7] R. R. Schmidt, G. Bosman, K. M. van Vliet, and M. A. Hollis, to be published.

On the Mechanism of Carrier Transport in Metal-Thin-Oxide Semiconductor Diodes on Polycrystalline Silicon

SAMARES KAR, MEMBER, IEEE, K. M. PANCHAL, SUDIP BHATTACHARYA, AND SUDHANSHU VARMA

Abstract—**A systematic experimental investigation was carried out to determine the dominant mechanism of carrier transport in MOS tunnel diodes and solar cells fabricated on Wacker cast polycrystalline silicon. A large number of diodes were fabricated and direct current-voltage and 100-kHz small signal capacitance-voltage characteristics were measured at various values of device temperature ranging between circa 300 and 420 K. Only those polysilicon diodes were chosen for analysis which exhibited exponential *I-V* characteristics. This excluded diodes located on large angle grain boundaries and on very small grains. For the sake of comparison, a few diodes and cells were fabricated, on single-crystal silicon also, by identical processing, and were measured and analysed. The measurements and their analysis reveal the following. The density and nature of defects present in the surface barrier region of the Wacker polysilicon material seem to have a significant influence on the mechanism of carrier transport across the barrier. With increasing number of such defects as dislocations, incoherent twin boundaries and precipitates, the dominant transport mechanism became multistep tunneling, while in MOS tunnel diodes on single-crystal silicon it was an activated process such as thermionic emission or minority-carrier injection. Stacking faults and coherent twin boundaries seemed to have a milder influence.**

Manuscript received April 15, 1982; revised July 12, 1982.

The authors are with the Department of Electrical Engineering and Materials Science Program, Indian Institute of Technology, Kanpur, 208016, India.

I. Introduction

SURFACE barrier devices, such as metal-semiconductor (MS), metal-thin oxide-semiconductor (MOS), and degenerate semiconductor-thin oxide-semiconductor (SOS) diodes are assuming increasing importance as these find a wide variety of especially optoelectronic and high-frequency applications. If tunneling through the interfacial layer is easy, then the

0018-9383/82/1200-1839$00.75

potential barrier, that will *mainly* influence carrier transport across any of the above surface barrier diodes, is located at the surface of the substrate semiconductor. Consequently, the various mechanisms of carrier transport that are known to be possible across these devices, are basically the same [1]. These are, namely, thermionic emission, thermionic field emission, tunneling, minority-carrier injection, bulk recombination-generation, recombination tunneling via interface states, and multi-step tunneling [1]-[5]. Since the dependence on device temperature, device voltage, surface barrier height, doping density, and bulk and interface trap densities varies from mechanism to mechanism, for a given diode at a certain temperature and in a certain voltage regime, one particular transport mechanism may dominate over the others, however, simultaneous contributions from two or more mechanisms could also occur in certain diodes.

A procedure, for identification of the dominant transport process, can be formulated, as follows, on the basis of currently available diagnostic tools. Since most of the above transport processes, except recombination tunneling via interface states, lead to exponential current-voltage (I_D-V) characteristics, the linear region of the measured ln I_D versus V plot can be extrapolated to obtain the zero voltage-current density intercept J_D^0. Plots of ln J_D^0 versus T^{-1}, ln J_D^0 versus $(n \cdot T)^{-1}$, ln J_D^0 versus T, and the diode quality factor n versus the temperature T can then be analyzed to identify the most prevalent carrier transport process across the surface barrier [1], [6]. Further, values of semiconductor band bending and doping density, obtained from the measured high-frequency reciprocal squared capacitance-voltage (C^{-2}-V) characteristics, can be utilized to distinguish thermionic emission from minority-carrier injection [1]. In case of diodes, where a particular mechanism of carrier transport prevails over large enough voltage and temperature regimes, the procedure, outlined above, can, generally, succeed in achieving its aim, at least, can be expected to narrow down the number of most probable mechanisms to a few.

Recent years have witnessed an ever increasing application of various kinds of semicrystalline/polycrystalline silicon in low-cost solar cells and in integrated circuits. In the context of the promise that beam processing holds out for crystallization, one can expect to see, in the future, widespread use of polysilicon also in thin film photovoltaic devices and in thin film VLSI/VHSIC. In the last few years, surface barrier solar cells have been fabricated on Wacker cast polysilicon, exceeding 10.0-percent efficiency [7]. The Wacker material has larger grains in the central region, of the dimensions of 4-6 mm, surrounded by smaller ones at the periphery. Several investigations have been carried out to evolve suitable procedures for delineation of various types of defects in this material, which include large angle and small angle grain boundaries, coherent and incoherent twin boundaries, stacking faults, dislocations, and individual and cluster of precipitates. A few attempts have been made to determine the influence of different types of defects on the electrical characteristics of surface barrier cells fabricated on this material [8], [9]. For example, experimental evidence indicates large angle grain boundaries to deform the electrical characteristics much more seriously than the small angle ones [8], [9].

The present investigation was undertaken to identify the predominant carrier transport mechanisms in MOS solar cells and tunnel diodes, fabricated on the central region of 5 cm × 5 cm Wacker cast polysilicon wafers. For the purpose of this investigation, both MOS cells and tunnel diodes were co-fabricated with aluminum barrier metal on p-type and with gold barrier metal on n-type polysilicon. The MOS tunnel diodes had small areas to facilitate measurements of diode current-voltage and 100-kHz small signal capacitance-voltage characteristics at various values of temperature ranging between approximately 300 and 420 K. Solar cells are expected to operate within the above temperature range. It is quite likely that, at low temperatures, a different mechanism will dominate than the one at elevated temperatures. Hence, the results of this study will be relevant at elevated temperatures only. Only those samples were chosen for analysis, on which the cells had conversion efficiencies ranging between 7.0 and 11.0 percent under equivalent AM I illumination, and on which the devices exhibited exponential diode current-voltage characteristics. The motivation behind the present study was to examine how a large density of defects, present in Wacker polysilicon, as dislocations, twin boundaries, and small angle grain boundaries, which still permit cell efficiencies to be reasonable, affect the dominant transport process. For the sake of comparing the transport process, MOS cells and diodes were fabricated also on single-crystal wafers with aluminum barrier metal on p-type silicon.

II. Experimental

The starting material was either "SILSO" polysilicon wafers from Wacker Chemitronic, both sides lapped, or Monsanto single-crystal wafers of (111) orientation, one side polished and the other side lapped. All the wafers had a resistivity of the order of 1.0 Ω/cm. All the fabrication processes, i.e., wafer surface cleaning, oxidation, and metallization, were done in class 100 clean environment using electronic grade chemicals and oil-free ultra-high vacuum systems.

Chemical etching was a critical step for the removal of the damaged layer from the surface of the polysilicon wafers as well as to delineate the defects on the surface. After initial degreasing in trichloroethylene, acetone, and methanol, 15 to 20 μm of the surface layer was removed in a mixture of CP4A and HNO_3. This left a surface which was not too uneven, but permitted defects to be recognized under an optical microscope. The surface roughness, present after etching, may influence the carrier transport mechanisms, however, our experience with different etchants [9] did not indicate this to significantly affect the nature of electrical characteristics. The monocrystalline wafers were, after initial degreasing, treated in HF, then in HNO_3, followed by HF again. Preceding each cleaning step, as well as finally, the wafers were rinsed thoroughly in deionized water of resistivity in the range of 14-16 MΩ/cm. Immediately after surface cleaning, a thin layer of silicon oxide was grown thermally in dry oxygen at 700°C, at atmospheric pressure, for 60 s. The oxide thickness was estimated to be about 20 Å from measurement of the oxide capacitance in accumulation. Immediately after oxidation, metallization was carried out in an oil-free ultra-high vacuum system in the pres-

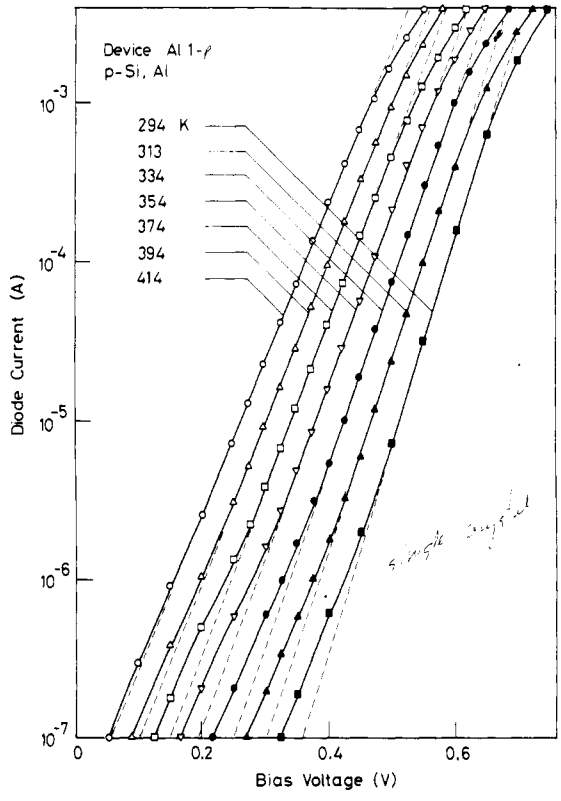

Fig. 1. Diode current-voltage (I_D-V) characteristics of MOS tunnel diode Al 1, with Al barrier metal on p-type single-crystal silicon, measured at 294, 313, 334, 354, 374, 394, and 414 K.

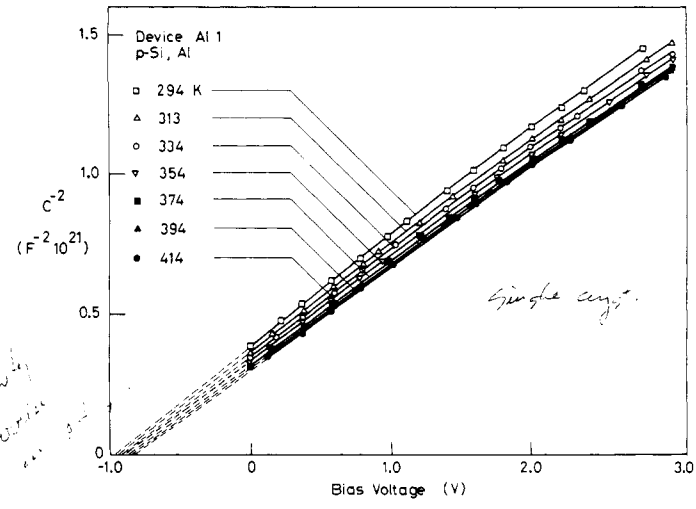

Fig. 2. Squared reciprocal capacitance-voltage (C^{-2}-V) characteristics of MOS tunnel diode Al 1, measured at 294, 313, 334, 354, 374, 394, and 414 K.

TABLE I
EXPERIMENTALLY OBTAINED VALUES OF VARIOUS PARAMETERS OF MOS TUNNEL DIODE Al 1

T (K)	φ_i^0 (V)	N_{doping} (10^{16}/cm^3)	$\varphi_i^0 + \varphi_F$ (V)	n
294	0.96	2.2	1.12	1.33
313	0.94	2.2	1.11	1.34
334	0.92	2.2	1.10	1.33
354	0.90	2.3	1.09	1.33
374	0.88	2.3	1.08	1.32
394	0.86	2.3	1.07	1.31
414	0.84	2.3	1.06	1.28

sure range of 2 to 4 X 10^{-6} torr. 5N purity metals were thermally evaporated from tungsten filaments. On n-type silicon, Au was used as the barrier metal, and Al on p-type silicon. The back contact metal was Al on n-type silicon and Au on p-type silicon. The front contacts were deposited through molybdenum shadow masks with circular holes of 4.0- and 0.5-mm diameter for cells and diode array, respectively. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The metal layer thickness for front contacts was in the range of 60-100 Å and the deposition rate was about 1-3 Å/s. A thick metal pad of 0.50-mm diameter was used on cells.

For each MOS tunnel diode chosen for examination, diode current-voltage, I_D-V and 100-kHz capacitance-voltage C-V, characteristics were measured at 6 or 7 values of device temperature, approximately between 300 and 420 K. The device temperature was controlled within ±0.5°C. From the C^{-2} versus V plot, doping density N_{doping} as well as the zero-bias silicon band-bending φ_i^0, were obtained at each temperature. The corresponding value of the bulk Fermi level φ_F was obtained from N_{doping}. From the linear region of the ln J_D versus V plot, the diode quality factor n and the zero-bias current intercept J_D^0 were obtained.

III. Results and Discussion

For each MOS tunnel diode measured, the following experimental plots were made: (i) ln I_D versus V at various values of the temperature, (ii) C^{-2} versus V at various values of the temperature, (iii) ln J_D^0 versus T^{-1}, (iv) ln J_D^0 versus $(n \cdot T)^{-1}$, and (v) ln J_D^0 versus T. Among a large number of diodes investigated, data obtained from 4 representative devices have been presented in the following.

Fig. 1 contains the ln I_D versus V characteristics of device Al 1, with Al barrier metal on p-type single crystal silicon, measured at 294, 313, 334, 354, 394, and 414 K. The broken lines are extrapolations of the linear regions, observed for intermediate values of the voltage. The deviation of I_D from an exponential form is due to the series resistance at high values of V, and may be due to recombination current at low values of V. Fig. 2 presents the high-frequency C^{-2} versus V characteristics of device Al 1 measured at the same values of temperature as in Fig. 1. The important experimental data derived from the measured characteristics of Figs. 1 and 2 have been displayed in Table I. For the device Al 1 as well as other diodes, Figs. 3, 4, and 5 depict the behavior of the logarithm of the current-density intercept, ln J_D^0, with T^{-1}, $(n \cdot T)^{-1}$, and T, respectively.

As can be observed in Table I in case of diode Al 1, diode quality factor n more or less remains unchanged in the tem-

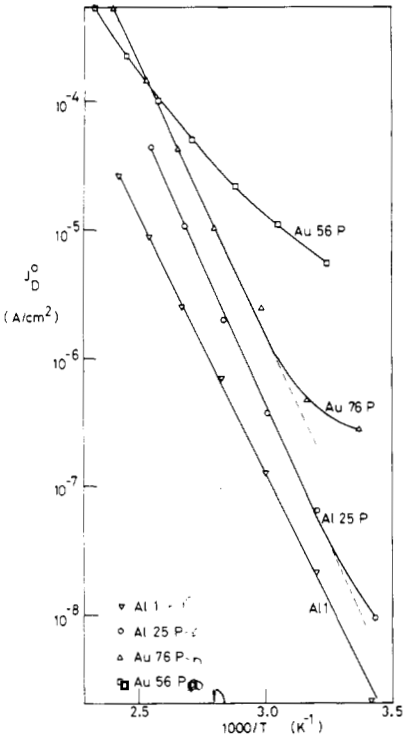

Fig. 3. The experimental current density intercept J_D^0 as a function of the reciprocal temperature T^{-1} for the following MOS tunnel diodes: (i) Al 1 with Al barrier metal on p-type single-crystal silicon: (ii) Al 25 P with Al barrier metal on p-type polysilicon: (iii) Au 76 P with Au barrier metal on n-type polysilicon; and (iv) Au 56 P with Au barrier metal on n-type polysilicon.

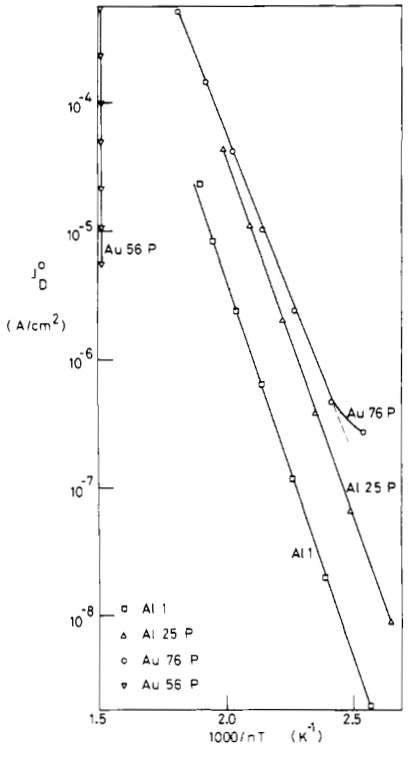

Fig. 4. The experimental current density intercept J_D^0 as a function of $(n \cdot T)^{-1}$ for MOS tunnel diodes: Al 1, Al 25 P, Au 76 P, and Au 56 P.

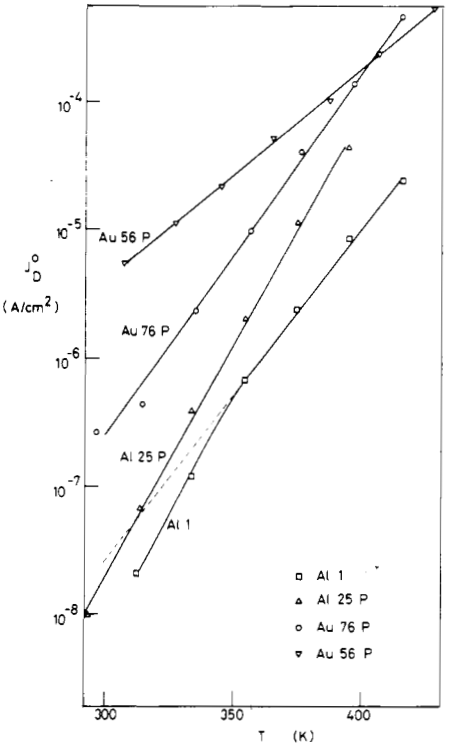

Fig. 5. The experimental current density intercept J_D^0 as a function of the device temperature T for MOS tunnel diodes, Al 1, Al 25 P, Au 76 P, and Au 56 P.

perature range of 294-414 K. The plots in Figs. 3-5 indicate that the logarithm of the current density intercept, $\ln J_D^0$, is a linear function of T^{-1}. The activation energy obtained from $\ln J_D^0(T^{-1})$ was 1.08 eV, which compares well with the value of $(\varphi_i^0 + \varphi_F)$ obtained from $C^{-2}(V)$ data, as well as with the value of the silicon bandgap. These features lead to the conclusion that the dominant carrier transport mechanism in device Al 1 is either thermionic emission or minority-carrier injection. Recently, Tarr and Pulfrey [10] have investigated MOS solar cells with Al barrier metal on single-crystal p-type silicon and they found the diode current to be dominated by minority-carrier injection, while Wu *et al.* [8] concluded thermionic emission to dominate the carrier transport in Schottky-barrier solar cells with Al barrier metal on Wacker p-type polysilicon. In case of sample Al 1, the experimental data do not quite allow us to choose between these two processes. Table I shows $(\varphi_i^0 + \varphi_F)$, which is equivalent to the uncorrected barrier height, to change with T by - 0.06 V. The experimentally recorded change in E_G between 294 and 414 K is - 0.04 eV which can more or less account for the observed $\delta(\varphi_i^0 + \varphi_F)$.

A set of characteristics, very different from those of sample Al 1, were obtained from device Au 56 P with Au as barrier metal on n-type polysilicon. The diode current-voltage and the high-frequency capacitance-voltage characteristics of device Au 56 P measured at device temperatures of 307, 327, 345, 365, 385, 405, and 425 K have been displayed in Figs. 6 and 7, respectively. The experimental data obtained from the mea-

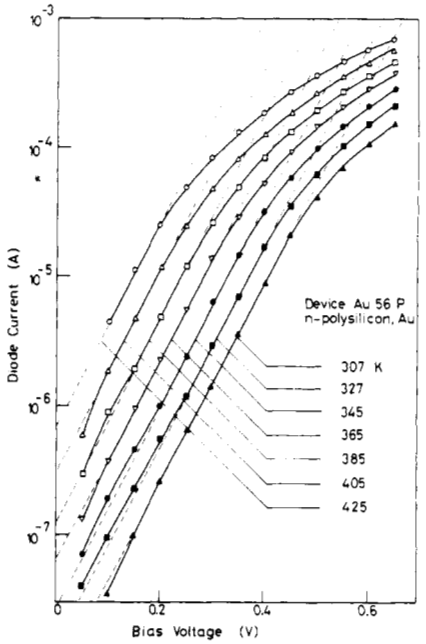

Fig. 6. Diode current-voltage (I_D-V) characteristics of MOS tunnel diode Au 56 P, with Au as barrier metal on n-type polysilicon, measured at 307, 327, 345, 365, 385, 405, and 425 K.

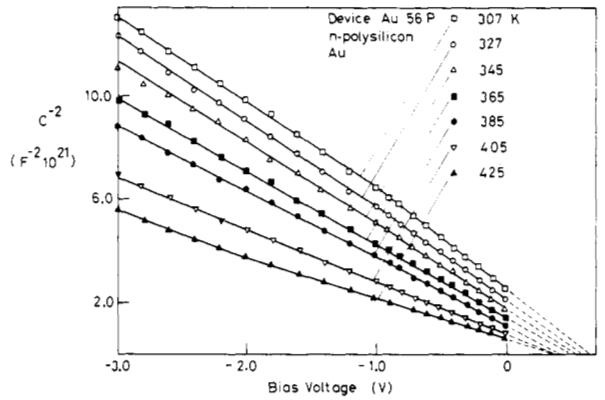

Fig. 7. Squared reciprocal capacitance-voltage (C^{-2}-V) characteristics of MOS tunnel diode Au 56 P, measured at 307, 327, 345, 365, 385, 405, and 425 K.

sured characteristics of device Au 56 P have been arranged in Table II and plotted in Figs. 3-5.

Tables I and II and Figs. 3-5 amply illustrate how the features of MOS tunnel diode Au 56 P differ from those of Al 1. Firstly, the diode quality factor n is much larger and varies as T^{-1}, so that $n \cdot T$ is invariant of T. Secondly, J_D^0 is a close linear function of T rather than of T^{-1} or $(n \cdot T)^{-1}$ (cf. Figs. 3-5). Thirdly, the zero-bias band bending φ_i^0 undergoes a much larger change with T than in the case of diode Al 1, i.e., -0.28 V in case of Au 56 P compared to -0.12 V in case of Al 1 (cf. Tables I and II). Fourthly, the doping density is seen to increase with T while it remained constant in case of Al (cf. Tables I and II).

The above characteristics and features of device Au 56 P lead one to conclude that the dominant mechanism of carrier transport across the surface barrier in this device is multistep tunneling [1], [5]. It is worth noting at this point that the voltage displacement between the ln I_D-V characteristics at 425 and 307 K, respectively, is exactly equal to the corresponding decrease in φ_i^0. This has the following implication. Normally, the multistep tunneling current is expressed in the form: $I_{MST} = C \cdot \exp(AT) \cdot \exp(B \cdot V)$. However, in view of the above observation, it may as well be expressed as $I_{MST} = C \cdot \exp[-B(\varphi_i^0 - V)]$, which amounts to saying that the temperature variance of I_{MST} is a direct consequence of the change in φ_i^0 with T. The values of A and B come out to be, for device Au 56 P, 0.040 K^{-1} and 18 V^{-1}, respectively. These values compare well with those reported in the literature in connection with multistep tunneling in MOS tunnel diodes on p-type polysilicon (0.052 K^{-1} and 22 V^{-1}, respectively) [1], in SOS diodes fabricated by spray hydrolysis on n-type silicon (0.050 K^{-1} and 23 V^{-1}, respectively) [1], and in SOS diodes fabricated by ion-beam sputtering on p-type silicon (0.064 K^{-1} and 24 V^{-1}, respectively) [5].

TABLE II
EXPERIMENTALLY OBTAINED VALUES OF VARIOUS PARAMETERS OF MOS TUNNEL DIODE Au 56 P

T (K)	φ_i^0 (V)	N_{doping} ($10^{15}/cm^3$)	$\varphi_i^0 + \varphi_F$ (V)	n	nT (K)
307	0.66	2.0	0.91	2.14	657
327	0.60	2.1	0.87	2.01	657
345	0.54	2.3	0.83	1.90	656
365	0.50	2.6	0.80	1.80	657
385	0.45	2.8	0.76	1.71	658
405	0.41	3.8	0.73	1.62	656
425	0.38	4.8	0.72	1.54	655

Experimental data obtained from the measured characteristics of device Al 25 P with Al as barrier metal on p-type and of device Au 76 P with Au as barrier metal on n-type polysilicon have been partly summarized in Tables III and IV, respectively, and partly displayed in Figs. 3-5. Figs. 3-5 and Tables III and IV indicate features of diodes Al 25 P and Au 76 P to lie somewhere between those of device Al 1 and of device Au 56 P. The features of device Al 25 P resemble those of thermionic emission in terms of a temperature-independent n, however, the degree of linearity of ln J_D^0 with respect to T is not any worse than the same with respect to T^{-1} or $(n \cdot T)^{-1}$. The value of the activation energy obtained from the plot of ln J_D^0 versus $(n \cdot T)^{-1}$ came out to be 1.04 eV which is somewhat higher than the value of $(\varphi_i^0 + \varphi_F)$ obtained, (cf., Table III). The change in $(\varphi_i^0 + \varphi_F)$ between 294 and 394 K for device Al 25 P is -0.17 V which is much larger than what can be accounted for by the corresponding change in E_G. The features of device Au 76 P illustrated in Figs. 3-5, and in Table IV are probably closer to those of device Au 56 P than to those of

TABLE III
EXPERIMENTALLY OBTAINED VALUES OF VARIOUS PARAMETERS OF MOS TUNNEL DIODE Al 25 P

T (K)	φ_i^0 (V)	N_{doping} (10^{15}/cm^3)	$\varphi_i^0 + \varphi_F$ (V)	n
294	0.80	6.3	0.99	1.29
314	0.76	6.4	0.96	1.29
334	0.72	6.4	0.93	1.29
354	0.66	6.4	0.88	1.29
374	0.62	6.5	0.86	1.28
394	0.57	6.5	0.82	1.28

TABLE IV
EXPERIMENTALLY OBTAINED VALUES OF VARIOUS PARAMETERS OF MOS TUNNEL DIODE Au 76 P

T (K)	φ_i^0 (V)	N_{doping} (10^{15}/cm^2)	$\varphi_i^0 + \varphi_F$ (V)	n
298	0.60	2.9	0.83	1.32
316	0.57	3.5	0.82	1.31
336	0.54	3.6	0.80	1.31
357	0.51	3.7	0.79	1.31
376	0.48	4.0	0.78	1.31
396	0.46	4.4	0.77	1.31
415	0.44	5.1	0.76	1.32

device Al 1. Although the diode quality factor n is invariant of the device temperature T, $\ln J_D^0$ versus $(n \cdot T)^{-1}$ or versus T is more linear than versus T^{-1}. In addition, the doping density, N_{doping} seems to change considerably with T. For diode Au Au 76 P, the observed change in $(\varphi_i^0 + \varphi_F)$ between 298 and 415 K is not significantly larger than what can be accounted for by δE_G. For devices Al 25 P and Au 76 P, when all the experimental data are considered, it appears that the mechanisms of multistep tunneling as well as thermionic emission are simultaneously operating to transport carriers across the surface barrier.

To obtain an account of the defects underlying each MOS tunnel diode, the polysilicon surface was examined under a high resolution optical microscope. As the barrier in MOS tunnel diodes is located within one micrometer of the surface, the defects visible on the surface should portray a reliable account of the mechanical imperfections that are likely to affect carrier transport across the surface barrier. Since it was necessary that diode current-voltage characteristics be exponential to permit diagnosis of the transport mechanism by the current procedure, diodes overlying regions that contained large angle grain boundaries and small grains were not chosen for analysis.

The region underlying device Al 25 P was found to contain a low density of etch pits, stacking faults, and one low angle grain boundary. Diode Au 76 P was located in a region characterized by several coherent twin boundaries and a low density of etch pits. The region underlying device Au 56 P contained some incoherent twin boundaries and a large density of etch pits.

The large number of MOS tunnel diodes, that were chosen for analysis, were located in regions that contained various combinations of defects, however, the latter did not include large angle grain boundaries and small grains, for reasons already explained. In terms of the electrical characteristics, all of these devices are more or less represented by the three polysilicon diodes whose experimental data have been presented already.

IV. CONCLUSIONS

Summarizing the experimental evidence, the following trend seems to emerge. With the density of such defects going up, as dislocations, incoherent twins, and precipitates, the mechanism of carrier transport across surface barriers, located in regions containing these, tend to be increasingly dominated by multistep tunneling. In other words, as defect density goes up, $\ln J_D^0$ becomes more linear with T rather than with $(n \cdot T)^{-1}$ or T^{-1}, the diode quality factor n ceases to be temperature invariant, instead $n \cdot T$ becomes constant, and $(\varphi_i^0 + \varphi_F)$ goes down significantly with T, while the effective doping density increases. This trend is most likely related to the generation of traps in the surface barrier region by the grown-in defects present in the polysilicon material. When the trap density is high enough, as in diode Au 25 P, multistep tunneling is the predominant carrier transport process. In case of lower defect densities, as in devices Al 25 P and Au 56 P, carriers may be transported simultaneously by multistep tunneling as well as by an activated process such as thermionic emission. Characteristics very similar to those displayed by device Au 56 P have been evidenced in case of surface barrier diodes fabricated on p-type single-crystal silicon by ion-beam sputtering of indium-tin-oxide [5], including the strong decrease of $(\varphi_i^0 + \varphi_F)$ with increasing temperature. There is increasing evidence now that ion-beam etching, prior to sputtering, damages the surface and introduces defects into the surface region [13]. If the surface barrier region contains a high density of traps, with increasing temperature, one may except a higher percentage of these to be ionized leading to an increase in the oxide potential and a subsequent decrease in $(\varphi_i^0 + \varphi_F)$.

REFERENCES

[1] S. Kar, S. Ashok, and S. J. Fonash, *J. Appl. Phys.*, vol. 51, p. 3417, 1980.
[2] E. H. Rhoderick, *Metal-Semiconductor Contacts.* Oxford, England: Clarendon Press, 1978.
[3] L. B. Freeman and W. E. Dahlke, *Solid-State Electron.*, vol. 13, p. 1483, 1970.
[4] S. Kar and W. E. Dahlke, *Solid-State Electron.*, vol. 15, p. 869, 1972.
[5] N. S. Chang and J. R. Sites, *J. Appl. Phys.*, vol. 49, p. 4833, 1978.
[6] A. N. Saxena, *Surface Sci.*, vol. 13, p. 151, 1969.

[7] K. K. Ng and H. C. Card, *IEEE Trans. Electron Devices*, vol. ED-27, p. 716, 1980.
[8] C-M. M. Wu, E. S. Yang, W. Hwang, and H. C. Card, *IEEE Trans. Electron Devices*, vol. ED-27, p. 687, 1980.
[9] C. Anandan and S. Kar, "On the delineation of defects in polysilicon," to be published.
[10] N. G. Tarr and D. L. Pulfrey, *Appl. Phys. Lett.*, vol. 34, p. 295, 1979.
[11] S. Ashok, S. J. Fonash, R. Singh, and P. Wiley, *IEEE Electron Device Lett.*, vol. EDL-2, p. 184, 1981.

Theory of Traveling-Wave Transistors

ANDREW S. PODGORSKI AND LING Y. WEI

Abstract—A distributed FET is treated as a problem of coupled active transmission lines over which the traveling waves grow by interaction. Models and equivalent circuits are proposed for evaluation of line parameters and propagation constants. Our calculations show that: 1) the gain increases with transistor width (or length of transmission line) up to about 2 cm, 2) at 15 GHz, a gain of 9 dB is achievable, and 3) the 3-dB bandwidth could be as large as 15 GHz. Possible applications of both types of traveling-wave transistors, unipolar and bipolar are discussed.

INTRODUCTION

IN electron devices, there are two important factors that limit frequency of operation: 1) electron transit time and 2) parasitic capacitances. It is obvious that these effects can be reduced by shrinking the size of the device. On the other hand, one could stretch device dimensions to take advantage of the electron transit time effect. This principle has been well demonstrated in klystrons, in traveling-wave tubes [1], [2] and in double stream amplifiers [3]. Dimension stretching can also convert lumped parameters into distributed ones, thus boosting the frequency of operation and increasing the bandwidth [4], [5]. Another advantage of having a large dimension is the isolation between the input and the output, resulting in a good stability in amplification.

It is natural to develop analogs to traveling-wave tubes and distributed amplifiers in solid-state devices. Work along these two lines took shape in 1965 when Thim and Barber [6] demonstrated a transferred-electron reflection amplifier made from GaAs while McIver [7] proposed a distributed MOSFET in which the calculated power gain could increase indefinitely with the width of the device. Following Thim and Barber's work, several devices using the same or similar principle appeared [8]-[12]. A good example is the GaAs traveling-wave transistor reported by Dean *et al.* [12]. The device could provide a gain of 12 dB in the 8-12-GHz range but the gain fluctuated widely (over 5 dB) in that range and the width of the structure was only 0.5 mm. The traveling-wave transistor as proposed by McIver can be viewed as coupled transmission lines. Though the theory appears simple and has been slightly refined by others [13]-[16], a truly distributed structure of MESFET's is yet to be made. In fact, the theory was too incomplete to predict what could be achievable.

This paper analyzes a distributed Schottky-barrier FET. Unlike previous work, we shall treat the lossy case in great detail. Circuit parameters are evaluated and then used to calculate the propagation constants of the transmission lines. Finally, the frequency response of a traveling-wave transistor is presented. The theory shows what can be achieved in a traveling-wave transistor. Potential applications are also indicated.

GENERAL FORMULATION

We consider a wide Schottky-barrier field-effect transistor (SBFET) (Fig. 1). In this model, a regular three-dimensional problem can be reduced to a one-dimensional problem with TEM waves in the x-direction by keeping dimensions in the

Manuscript received September 28, 1981; revised July 12, 1982. Support for this work was provided by the National Sciences and Engineering Council of Canada.

A. S. Podgorski was with the Electrical Engineering Department, University of Waterloo, Waterloo, Ont., Canada N2L 3G1. He is now with the National Research Council of Canada, Ottawa, Ont., Canada.

L. Y. Wei is with the Electrical Engineering Department, University of Waterloo, Waterloo, Ont., Canada N2L 3G1.

0018-9383/82/1200-1845$00.75