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Effect of thermal annealing on the defects and electrical properties of semi-insulating 6H-SiC

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ABSTRACT

Vanadium-doped 6H-SiC wafers were annealed at 950 °C, 1350 °C and 1650 °C in argon atmosphere for 1 h in order to investigate the thermal annealing effect on the defects and electrical properties. It was experimentally observed that the electrical and crystalline property of vanadium-doped 6H-SiC didn't obviously change after annealing at 950 °C and 1350 °C. However, the resistivity of vanadium-doped 6H-SiC dropped by 5–6 orders of magnitude after annealing at 1650 °C. The glow discharge mass spectrometry (GDMS), electron paramagnetic resonance (EPR), high resolution x-ray diffraction (HRXRD) and resistivity mapping measurements implied that both vanadium dopants and intrinsic defects were responsible for the semi-insulating property of the as-grown single crystal SiC. After annealing at high temperature (≥1650 °C), the doped vanadium in single crystal SiC would partially evaporate and the left vanadium dopants might be not enough to compensate the unintentional donors/acceptors with the disappearance of silicon vacancy defects.

1. Introduction

Silicon carbide (SiC) has superior physical and material properties. It is regarded as an excellent wide band-gap semiconductor material for fabricating high temperature, high frequency and high power electronic devices [1–3]. In the fabrication of high frequency devices, semi-insulting property of SiC substrate is required to minimize the parasitic capacitances between the terminals, including the ground. Therefore, it's necessary to keep a high level of resistivity all the time for the substrate material [4]. For semi-insulating SiC substrate, vanadium is often used to compensate the donors/acceptors dopants in order to pin the fermi level near the trap level. This is also commercially used since it is hard to reduce the background dopant density to a quite low level [5,6]. As an amphoteric impurity, the solubility limit of vanadium in single crystal SiC is in the level of 10^{17} cm^{-3} and thermally stable. The thermal activation energy of vanadium is 1.2–1.4 eV with acceptor levels of E_C-(0.65–0.72 eV) in p-type 6H-SiC and donor levels of E_V-(1.3–1.5 eV) in n-type 6H-SiC [1,4,7–9]. Besides the intentionally doping method, there are extensively investigations on the deep level native defects which are responsible for the semi-insulting property of single crystal SiC [10–13]. The silicon vacancy (V_{Si}), carbon vacancy (V_C), divacancy (V_C-V_{Si}), and carbon vacancy antisite pairs (V_C-C_{Si}) are common defects in single crystal SiC. These native defects can create deep levels which are responsible for the semi-insulting property. Different types of defect have different thermal activation energy ranging from 0.8 eV to 1.5 eV [14,15].

Son et al. [16] revealed that the high purity semi-insulating (HPSI) SiC had different thermal active energy. For the HPSI sample with Ea = 0.8–0.9 eV, the negatively charged V_{Si} exhibited the highest density and the resistivity significantly decreased after annealing at 1600 °C. For the HPSI sample with Ea = 1.1–1.3 eV, the positively charged V_C or the negatively charged C_{Si}-V_C were dominant. For the HPSI sample with Ea = 1.5 eV, the positively charged V_C and V_C-V_{Si} were dominant and the resistivity was stable after annealing at 1600 °C[17]. But the performance of vanadium-doped SiC after high temperature annealing is still unclear since it's hard to detect deep levels and types of point defects in vanadium-doped semi-insulating SiC. Both vanadium and native defects are responsible for semi-insulting property, but it is still unknown for the cooperation between vanadium dopants and the native defects in vanadium-doped semi-insulting SiC and their behavior which may affect the electrical properties after high temperature environment. It is well-known that high temperature process is indispensable for the fabrication of SiC-based electronic devices. It is quite necessary to know the change in structural and electrical properties after high temperature fabrication process. In order to get the knowledge of temperature-dependent structural and electrical

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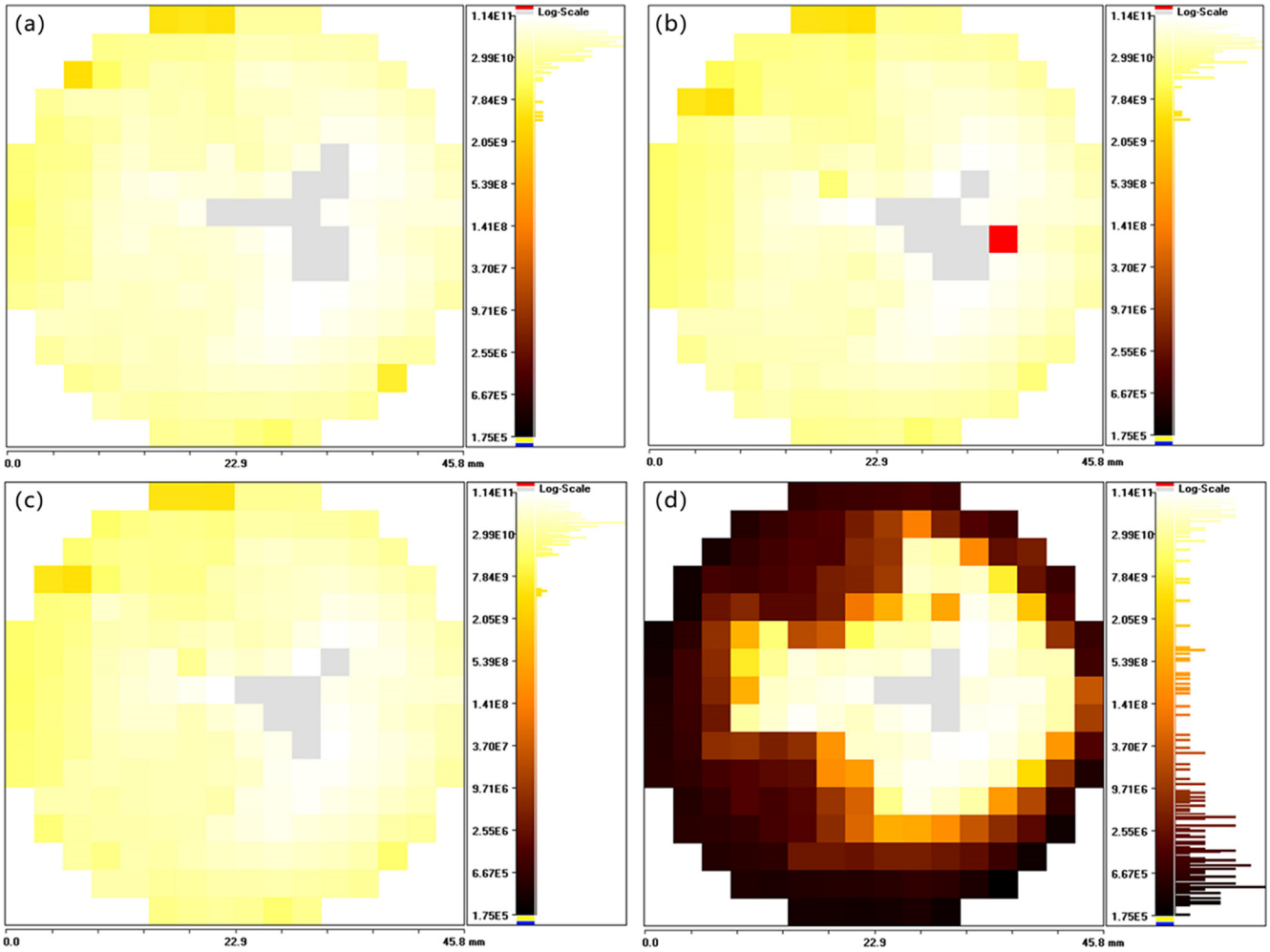

Fig. 1. Contactless resistivity mapping of a semi-insulating 6H-SiC wafer: (a) before thermal annealing; (b) annealed at 950 °C; (c) annealed at 1350 °C; (d) annealed at 1650 °C.

property of semi-insulting SiC, we investigated the typical temperature environment of annealing temperature of forming ohmic contact, surface morphological etching, and homo-epitaxial temperature by thermal annealing. An in-depth characterization was performed to analyze the change in defect, dopant and electrical properties.

2. Experiments

2-inch vanadium-doped semi-insulating 6H-SiC wafers were sliced from a single crystal SiC ingot which was grown by sublimation method. The resistivity was detected by a contactless resistivity mapping system (COREMA-WT). High resolution x-ray diffraction (HRXRD) mapping was used to characterize the crystalline quality. The thermal annealing process was carried out in argon atmosphere, and was performed sequentially at 950 °C, 1350 °C and 1650 °C corresponding to the typical temperature range of fabricating electronic devices [1,4,18]. The temperature ramping rate was 15 °C/min and was kept at the target temperature for 1 h, and then cooled down to room temperature. The wafer was polished after high temperature annealing and was washed with hydrofluoric acid in order to avoid graphene or carbon layer impurities occurring on the surface of SiC. The crystalline quality and resistivity properties were characterized before and after each thermal annealing processing. Glow discharge mass spectrometry (GDMS) and electron paramagnetic resonance (EPR) were used to characterize the change in vanadium concentration and defects in different wafer region.

3. Results and discussion

3.1. The electrical properties of vanadium-doped 6H-SiC

Fig. 1 shows the contactless resistivity mapping results of a vanadium-doped 6H-SiC wafer before and after thermal annealing at 950 °C, 1350 °C and 1650 °C. The data points recorded from the COREMA instrument have a resolution of 16 × 16 grids for a 2 in. wafer. Fig. 1(a) shows the wafer resistivity distribution mapping before annealing treatment. Fig. 1(b)–(d) show the wafer resistivity distribution mapping after annealing at 950 °C, 1350 °C and 1650 °C, respectively. The resistivity of a typical semi-insulating SiC wafer is $> 10^5$ Ω·cm. From the contactless resistivity mapping results of Fig. 1(a), it can be seen that the resistivity for the whole wafer is $> 4.3 \times 10^8$ Ω·cm. However, the distribution of resistivity is not uniform for the whole wafer. The maximum value of resistivity is 1.5×10^{11} Ω·cm. The resistivity of right central region is about one order of magnitude higher than that of the other areas. No obvious change in the resistivity is observed after annealing at 950 °C and 1350 °C, as shown figure (b) and figure (c). However, noticeable change is clearly observed after annealing at 1650 °C as shown in Fig. 1(d). The resistivity of peripheral region decreases from ~1010 Ω·cm to ~105 Ω·cm. The resistivity of central region remains 10^{10}–10^{11} Ω·cm. The change in resistivity means a corresponding change in the vanadium content or point defects [19].

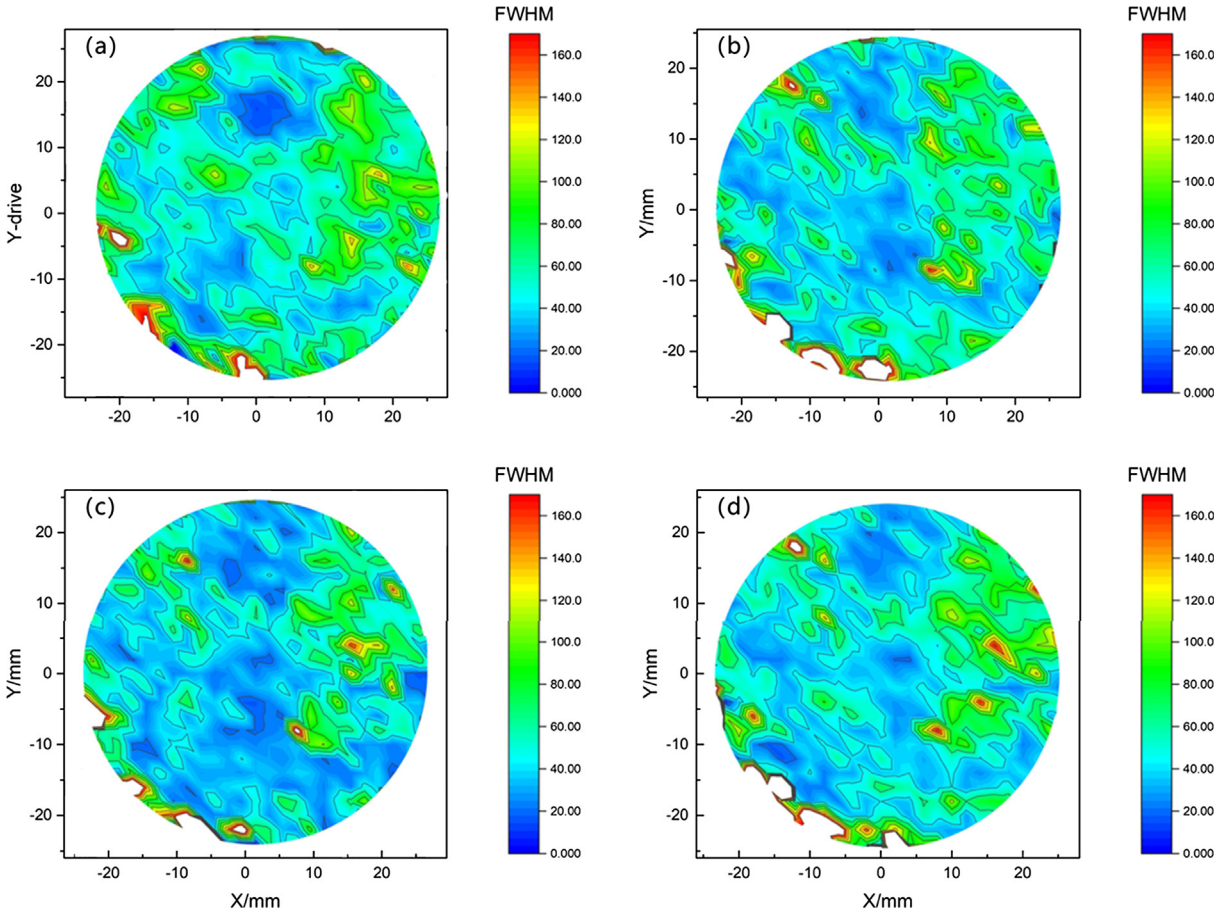

Fig. 2. The distribution mapping of FWHM value of HRXRD rocking curve plane scanning: (a) without thermal annealing; (b) annealed at 950 °C; (c) annealed at 1350 °C; (d) annealed at 1650 °C.

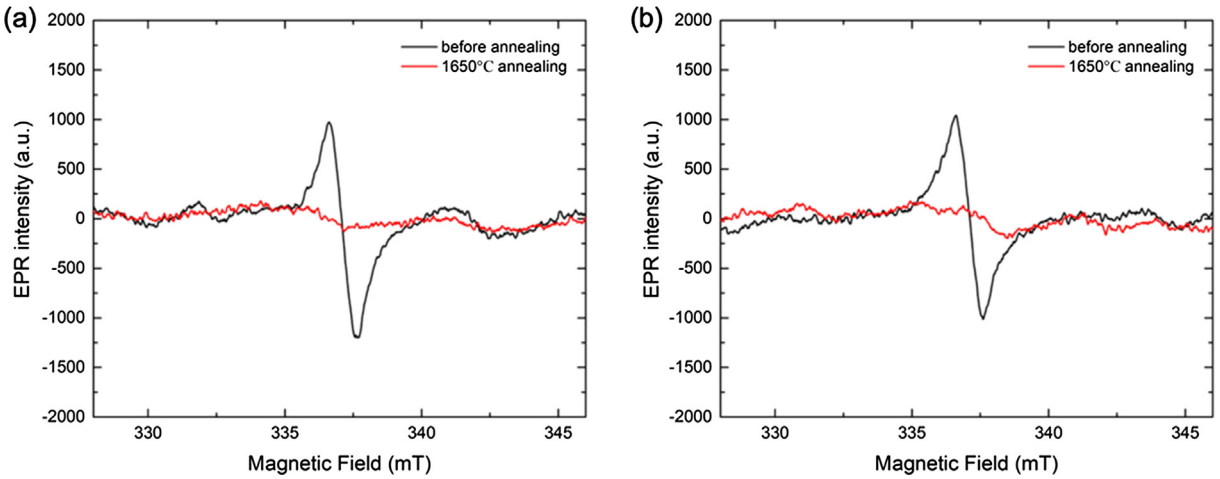

Fig. 3. EPR spectra of the central region and the peripheral region before and after the 1650 °C annealing: (a) central region; (b) peripheral region.

3.2. The structural properties of vanadium-doped 6H-SiC

Fig. 2 shows the distribution of full width at half maximum (FWHM) values analyzed from the HRXRD results. We adopted the method of surface scanning by changing the position of the incident X-ray light. The coordinate axis was set up by taking the center of the wafer as the coordinate origin and taking the Si-face of the wafer as the reference plane. An interval of 2 mm was used to collect the X-ray rocking curve signal, and then we obtained the X-ray rocking curve mapping for the whole wafer. The FWHM values of all the measured points were changed into distribution mapping within the axes. The distribution charts were filled with different colors corresponding to different FWHM values. Fig. 2(a) shows the distribution mapping of the 6H-SiC wafer without annealing treatment. Fig. 2(b)–(d) show the distribution mapping of the 6H-SiC wafer after annealing at 950 °C, 1350 °C and 1650 °C, respectively.

As can be seen from Fig. 2(a), the FWHM values of 60% regions of SiC wafer is < 60 arcsec. The FWHM values of ~30% regions is 60–100 arcsec. The FWHM values of some marginal regions (about 10%) is > 100 arcsec. The HRXRD results show that the crystalline quality of

the selected wafer is good, while the uniformity of crystalline quality is not good. It can be seen from Fig. 2(b)–(c) that after annealing at 950 ˚C and 1650 ˚C, the area of FWHM values < 60 arcsec slightly increased, and correspondingly the area of FWHM values of 60–100 arcsec slightly decreased. This indicates that thermal annealing can slightly improve the crystalline quality. However, after annealing at 1650 ˚C, as shown in Fig. 2(d), the FWHM values of the 6H-SiC all slightly increases, indicating that the crystalline quality of the 6H-SiC wafer slightly decreases. This is not responsible for the noticeable change in the resistivity.

3.3. The changes in vanadium concentration and defects after annealing at 1650 ˚C

In order to elucidate the change in the resistivity after annealing, we used the GDMS to detect the content of vanadium in the central areas and peripheral areas of the 6H-SiC wafer. The content of vanadium decreased from 1.3 ug/g to 0.56 ug/g for the central areas. The resistivity of peripheral region decreased by 5–6 orders of magnitude with the decreased in vanadium content from 0.93 ug/g to 0.45 ug/g. Besides the GDMS measurement, we investigated the defect in the 6H-SiC by using EPR. Fig. 3 shows the characterization of EPR at 300 K. Before annealing, there were signals both in the central areas and in the peripheral areas with g = 2.00210 and g = 2.00193 for central region and peripheral region. After annealing at 1650 ˚C for 1 h, these two signals all vanished as shown in Fig. 3(a) and (b). The strong signals of EPR are often attributed to the collective effect of various defects in single crystal SiC and it reflects the decrease in defect content. From the point of thermal activation energy, the silicon vacancy (V_{Si}) is prior to vanish after high temperature annealing up to 1650 ˚C due to its small thermal activation energy of 0.8–0.9 eV. The carbon vacancy (V_C) and divacancy (V_CV_{Si}) are more stable for its large thermal activation energy of 1.5 eV. Thus it can be deduced that defects are selectively compensated during high temperature annealing process which agrees well with Zvanut's research [11]. Son et al. [16] considered that only in heavily vanadium-doped semi-insulating SiC, the semi-insulating properties were determined by vanadium dopants. Whereas in moderate vanadium-doped SiC, the semi-insulting properties were determined by intrinsic defects. In this experiment, the EPR results indicate that vacancies with low thermal activation energy (such as V_{Si}) can keep stable when the annealing temperature lower than 1350 ˚C. Even if these defects were compensated by annealing, the vanadium still can compensate the acceptors and donors. Higher annealing temperature (≥1650 ˚C) can result in defect compensation. Both vanadium dopants and intrinsic defect are responsible for the semi-insulating property of the as-grown single crystal SiC. After annealing at high temperature (≥1650 ˚C), the vanadium dopants will partially evaporate and the left vanadium dopants may be not enough to compensate the unintentional donors/acceptors and thus leads to noticeable change in the electrical properties.

4. Conclusion

The thermal annealing effect on the defects and electrical properties of semi-insulating SiC was studied. Vanadium-doped 6H-SiC wafers were annealed at different temperatures from 950 ˚C to 1650 ˚C. The electrical and crystalline property of vanadium-doped 6H-SiC didn't change after annealing at 950 ˚C and 1350 ˚C. High annealing temperature of 1650 ˚C resulted in an obvious drop in the resistivity by 5–6 orders of magnitude. The GDMS, EPR, HRXRD and resistivity measurements revealed that both vanadium dopant and intrinsic defect were responsible for the electrical property of semi-insulating single crystal SiC. After annealing at high temperature (≥1650 ˚C), the doped vanadium would evaporate and the left vanadium might be not enough to compensate the unintentional donors/acceptors.

CRediT authorship contribution statement

Tingxiang Xu: Investigation, Data curation, Writing - original draft. **Xuechao Liu:** Conceptualization, Methodology, Supervision, Writing - review & editing. **Shiyi Zhuo:** Validation. **Wei Huang:** Formal analysis. **Pan Gao:** Resources. **Jun Xin:** Resources. **Erwei Shi:** Project administration, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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