Physica B 406 (2011) 4355–4360

Contents lists available at SciVerse ScienceDirect

Physica B

journal homepage: www.elsevier.com/locate/physb

The influence of substrate temperature on electrical properties of Cu/CdS/SnO_2 Schottky diode

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ARTICLE INFO

Article history:
Received 9 June 2011
Received in revised form
22 August 2011
Accepted 23 August 2011
Available online 26 August 2011

Keywords:
CdS
Thin film
Vacuum evaporation
Schottky diode

ABSTRACT

Polycrystalline CdS samples on the SnO_2 coated glass substrate were obtained by vacuum evaporation method at low substrate temperatures (T_S=200 and 300 K) instead of the commonly used vacuum evaporation at high substrate temperatures (T_S > 300 K). X-ray diffraction studies showed that the textures of the films are hexagonal with a strong (0 0 2) preferred direction. Circular Cu contacts were deposited on the upper surface of the CdS thin films at 200 K by vacuum evaporation. The effects of low substrate temperature on the current–voltage (*I–V*) characteristics of the Cu/CdS/SnO_2 structure were investigated in the temperature range 100–300 K. The Cu/CdS (at 300 K)/SnO_2 structure shows exponential current–voltage variations. However, *I–V* characteristics of the Cu/CdS (at 200 K)/SnO_2 structure deviate from exponential behavior due to high series resistance. The diodes show non-ideal *I–V* behavior with an ideality factor greater than unity. The results indicate that the current transport mechanism in the Cu/CdS (at 300 K)/SnO_2 structure in the whole temperature range is performed by tunneling with E_{00}=143 meV. However, the current transport mechanism in the Cu/CdS (at 200 K)/SnO_2 structure is tunneling in the range 200–300 K with E_{00}=82 meV.

1. Introduction

The polycrystalline CdS is a II–VI group semiconductor with a band gap value of 2.42 eV at 300 K. CdS has been studied extensively for various applications such as solar cells, optical detectors and optoelectronic devices [1–3]. There are currently a vast number of reports of experimental studies on metal/semiconductor Schottky diodes [4–9]. The electrical performance of metal/semiconductor Schottky diodes depends mainly on the surface and interface properties [10]. The crystal surfaces are usually covered with thin oxide layer during sample preparation or metal evaporation. This interface oxide layer may have a strong influence on the diode characteristics and leads to increased series resistance of the diode [11]. Oktik et al. [12] determined that the values of saturation current and ideality factor of Au/CdS (single crystal) diode for the surface of CdS characterized by randomly sized etch hillocks are higher than that of Au/CdS diode with the surface of CdS characterized by a regular array of smoothly faceted etch hillocks. Patel et al. [13] investigated *I–V* characteristics of Au/nano-CdS and Au/bulk-CdS junctions. They obtained the higher current flow in the case of Au/nano-CdS compared to Au/bulk-CdS junction due to the presence of a high density of surface/interface traps at the Au/nano-CdS interface. It was determined by Mandal et al. [14] that *I–V* plot of Au/nano-CdS/CdS/SnO_2 device becomes steeper than that of Au/CdS/SnO_2 device due to the presence of a higher defect concentration in the nano-CdS layer, which resulted in higher stress. It has been proved by Kislyuk et al. [15] that the CdS surface plays a major role in the photovoltaic activity of the heterojunction, whereas the polymer serves as the conducting component of the heterojunction, and thus, the mechanism of photovoltaic response in this heterojunction is very similar to that observed in classical Schottky diodes.

The metals of group I (Ag, Cu) are the fast diffusing impurities in CdS and the penetration by diffusion into CdS can cause changes in physical properties of the interface region between the metal and CdS and so in characteristics of the structure [16,17]. The thin film devices are made on glass coated by transparent conductive oxides such as tin oxide, SnO_2. The electron affinity and band gap of SnO_2 are 4.0 eV and 3.6 eV, respectively [6]. SnO_2 increased the amount of the surface roughness of CdS thin films [18] and also $CdS_{1-x}Sn_x$ solid solution can be formed between CdS and SnO_2 layers [19]. The device performance can be changed by these effects.

The CdS deposition process is important in determining the quality of Schottky diodes. Various techniques have been used to prepare CdS thin films such as vacuum evaporation [20], chemical bath deposition [21], close spaced sublimation [22], spray pyrolysis [23] and pulsed laser deposition [24]. Vacuum evaporation technique

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doi:10.1016/j.physb.2011.08.067

is a well established technique for the preparation of uniform films with good crystallinity [25–27]. Our research group investigated CdS thin films prepared by vacuum evaporation method that is vacuum deposition at low substrate temperatures (<300 K) instead of the commonly used vacuum deposition at high substrate temperatures [28]. It was determined that, as the substrate temperature decreases from 300 K to 100 K, the surface morphology of the CdS becomes more homogeneous and the surface roughness of the CdS decreases. In addition, the surface of the sample deposited at room temperature has more porous character than that of the sample deposited on the cooler substrate. Also, the sample deposited at room temperature has randomly sized grains. Similar results were obtained by our group for the CdSe thin films prepared with vacuum deposition at low substrate temperatures [29].

In this paper we report the effects of low substrate temperatures (T_S=200 and 300 K) used for the production of CdS thin film prepared by vacuum evaporation technique on electrical properties of Cu/CdS/SnO_2 structure. *I–V* characteristics of these devices were measured to establish a correlation between the process parameters and the electrical properties of Cu/CdS/SnO_2 structure.

2. Experimental details

The CdS thin films were deposited by vacuum evaporation in a quasi-closed volume on SnO_2 coated glass substrates using high purity CdS polycrystalline powder (99.995%, from Aldrich Chemical Company, USA) as the source material. The cross-sectional view of the evaporation apparatus is given in Fig. 1. The source–substrate distance was fixed at 9 cm. Source and substrate temperatures were monitored and controlled separately using thermocouples. When a base pressure of 6.0×10^{-6} Torr was reached, the substrate was cooled by pumping liquid nitrogen through the substrate cooler made of copper pipe. A resistive heater was placed between the substrate and cooling block to adjust its temperature in the range 200–300 K during deposition. To prevent the splattering of the source, the source powder was pressed into disks of 13 mm diameter. The source temperature was kept at around 923 K. The CdS thin films were grown at substrate temperatures of 300 and 200 K (±3.0 K). The shutter is continuously kept open during deposition.

The crystal structure of CdS thin films was studied by X-ray diffraction (XRD) using RigakuD/Max-IIIC diffractometer with CuK_α radiation (λ=1.5418 Å) over the range 2θ=3–70° at room temperature. The hot probe method and Hall effect measurements (in dark) were used to find carrier type and carrier density of the CdS thin films at room temperature. Resistivity of CdS thin films was measured by four probe method in the dark at room temperature. Transmission measurements were performed to determine the optical properties of the films using a Shimadzu UV-1601 spectrophotometer in the range 400–1000 nm.

Circular Cu contacts with 1 mm diameter were deposited on the upper surface of the CdS thin films using a vacuum evaporation method. The CdS/SnO_2/glass structure was cooled by pumping liquid nitrogen in order to decrease the possible diffusion of Cu into the structure. The temperature of CdS/SnO_2/glass structure was fixed at 200 K during Cu evaporation. The *I–V* characteristics of the Cu/CdS/SnO_2 structures were obtained in the temperature range of 100–300 K using Leybold–Heraeus HR1 cryostat.

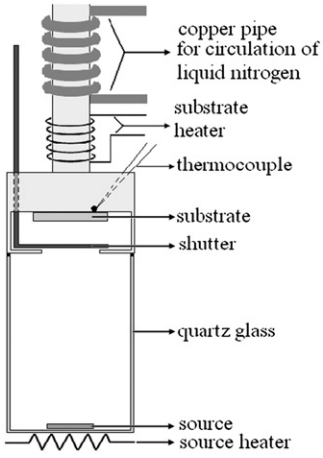

Fig. 1. A cross-sectional view of the thermal evaporation apparatus.

3. Results and discussion

The XRD results of the CdS films on SnO_2/glass substrates at temperatures of 300 and 200 K are shown in Fig. 2. The textures of the films are hexagonal with a strong (0 0 2) (2θ=26.6°) preferred direction perpendicular to the substrate. The intensity of (0 0 2) reflection increases as the substrate temperature decreases from 300 K to 200 K. The low intensity peaks located at $2\theta=\sim24.0°$, $\sim29.1°$, $\sim48.1°$ and $\sim54.7°$ are attributed to (1 0 0), (1 0 1), (1 0 3) and (0 0 4) planes of hexagonal CdS, respectively. In the XRD patterns was observed a peak at $2\theta=\sim37.9°$. This peak is attributed to the SnO_2 with tetragonal structure [JCPDS 41-1445]. The SnO_2 exhibits *T*(2 0 0) peak at 2θ=38° [30]. There is a small shift in the position of the (2 0 0) peak of SnO_2. The shift of the *T*(2 0 0) peak is most probably an indication of the formation of $CdS_{1-x}Sn_x$ solid solution that is formed due to the interdiffusion in the junction region [19]. As can be seen, the intensity of *T*(2 0 0) reflection decreases as the substrate temperature decreases from 300 K to 200 K. The amount of decrease is attributed to the reducing of interdiffusion in the junction region due to the low temperature deposition [31]. Scherrer's formula was used for the calculation of the crystallite sizes, which is given by the following formula:

$$D=\frac{0.94\lambda}{\beta\cos\theta} \tag{1}$$

where *D* is the grain size, β is the FWHM, θ is the Bragg angle and λ is the wavelength of X-rays. The grain size of samples was calculated from the (0 0 2) peak. The grain sizes of the CdS thin films prepared at 300 K and 200 K are 39.2 nm and 38.1 nm (±0.1 nm),

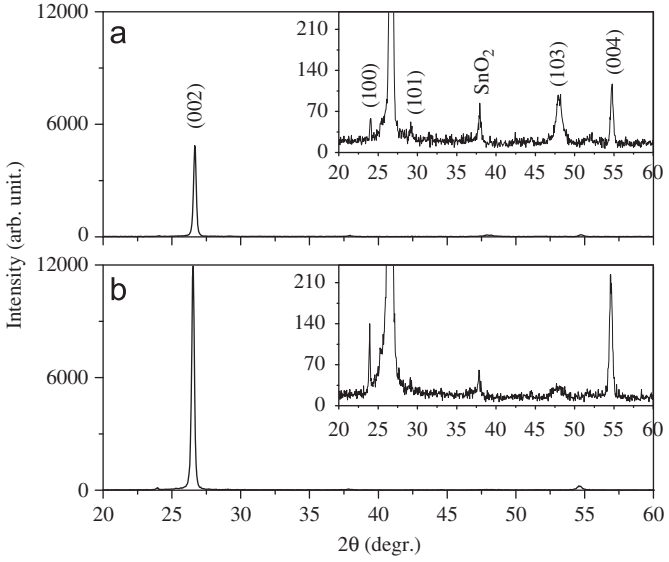

Fig. 2. XRD patterns of CdS thin films prepared at (a) 300 K and (b) 200 K.

respectively. The lattice parameter c of the unit cell was calculated according to the following relation:

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2+hk+k^2}{a^2}\right) + \frac{l^2}{c^2} \quad (2)$$

where d is the interplanar spacing of the atomic planes. The c lattice constants for the samples prepared at 300 K and 200 K are 6.683 Å and 6.711 Å ($\pm$0.005 Å), respectively. The sample prepared at 300 K has smaller c lattice constant than the corresponding value of the powder CdS (6.72 Å) indicating that the film is subjected to a tensile stress in the plane parallel to the substrate surface [32].

The optical transmittance spectra of the CdS films as a function of wavelength are shown in Fig. 3. The maximum transmission of the CdS thin films was above 75%. The thickness of the films was calculated from the transmission interference using the following equation [33]:

$$t = \frac{\lambda_1\lambda_2}{2(\lambda_1 n_2 - \lambda_2 n_1)} \quad (3)$$

where t is the film thickness, n_1 and n_2 are the refractive indices at the two adjacent maxima (or minima) at λ_1 and λ_2. The thicknesses of the CdS thin films prepared at 300 K and 200 K are 4.8 μm and 4.6 μm, respectively. The band gap energy E_g of the CdS thin films was determined using the dependence of the absorption coefficient (α) on the photon energy

$$\alpha = A(h\nu - E_g)^{1/2} \quad (4)$$

where E_g is the optical band gap and A is a constant. The band gap energy is obtained by extrapolating the linear part of the $(\alpha h\nu)^2$ versus $(h\nu)$. The variation of $(\alpha h\nu)^2$ as a function of $h\nu$ is shown in the inset of Fig. 2. The band gaps of the samples are 2.38 eV (at 300 K) and 2.39 eV (at 200 K). E_g value of our samples is found to be in good agreement with those reported by Pal et al. [34]. Pal et al. found 2.38 eV for CdS sample prepared at 300 K substrate temperature with vacuum evaporation method.

Fig. 4 shows I–V characteristics of the Cu/CdS/SnO_2 structure measured in the temperature range of 100–300 K. As can be seen in Fig. 4, the I–V characteristics of the Cu/CdS/SnO_2 structure are significantly affected from the sample preparation temperature of CdS thin film. It was observed that the I–V characteristic of the samples shows approximately symmetrical rectifying behavior with the polarity of the applied voltage. In Fig. 4a, the Cu/CdS (at 300 K)/SnO_2 structure illustrates more or less exponential current–voltage variations. However, the I–V characteristic of the Cu/CdS (at 200 K)/SnO_2 structure (Fig. 4b) deviates from the exponential behavior. In our samples the appearance of ohmic behavior can be attributed to Cu contacts deposited at 200 K. The low temperature deposition decreases the copper diffusion in CdS. Lepley et al. [16] determined that the Cu/CdS contact is ohmic just after the copper deposition for the formation of a typical Cu/CdS sample at room temperature; however after 2 days the Schottky barrier is set up due to the Cu diffusion into CdS. In our work, a higher current flow was observed in the Cu/CdS (at 300 K)/SnO_2 structure compared to the Cu/CdS (at 200 K)/SnO_2 structure. The rectifying behavior and the higher current of Cu/CdS (at 300 K)/SnO_2 structure can be attributed to the increasing contact between Cu and CdS due to porous surface of CdS (at 300 K) [28] and thus increasing the density of surface/interface traps at the Cu/CdS (at 300 K)/SnO_2 structure [13,35].

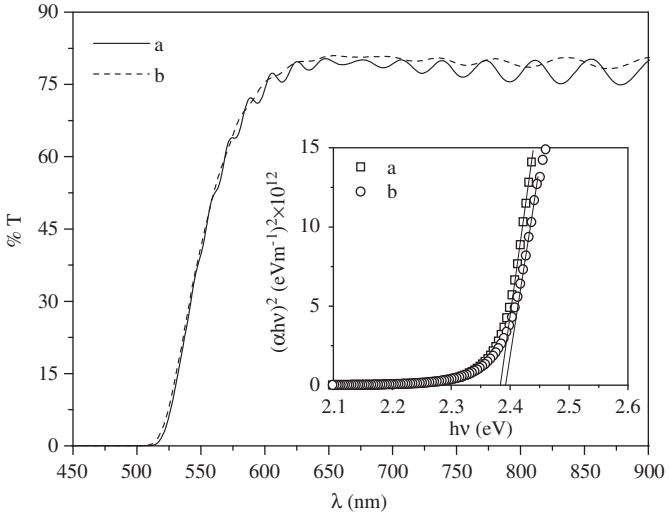

Fig. 3. Optical transmittance spectra of CdS thin films prepared at (a) 300 K and (b) 200 K.

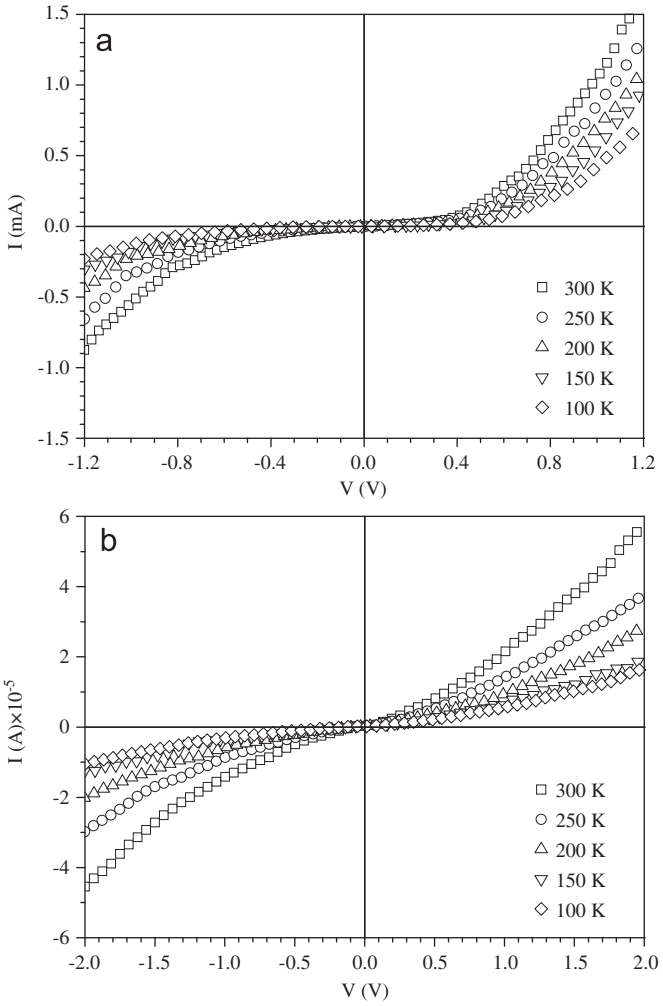

Fig. 4. I–V characteristics of the Cu/CdS/SnO_2 structure with (a) CdS prepared at 300 K and (b) CdS prepared at 200 K.

The thermionic emission current–voltage relation of a Schottky diode is given by [36]

$$I = I_0(e^{qV/nkT} - 1) \quad (5)$$

where I_0 is the saturation current, q is the electronic charge, V is the applied voltage, n is the ideality factor, k is Boltzmann's constant and T is the temperature in K. The saturation current I_0 is defined by

$$I_0 = AA^*T^2 e^{q\phi_{b0}/kT} \quad (6)$$

where A^* is the theoretical Richardson constant (24 A/cm^2 K^2 for CdS), A is the diode area and ϕ_{b0} is the zero bias barrier height.

For V values greater than $3\,kT/q$, the ideality factor n can be calculated from the slope of the straight line region of the forward bias ln(I)–V plot for each temperature and can be written as

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)}. \tag{7}$$

I_0 can be determined by an extrapolation of the forward bias ln(I)–V curve to $V=0$ for each temperature. The zero bias barrier height (ϕ_{b0}) is calculated by the following formula:

$$\phi_{b0} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \tag{8}$$

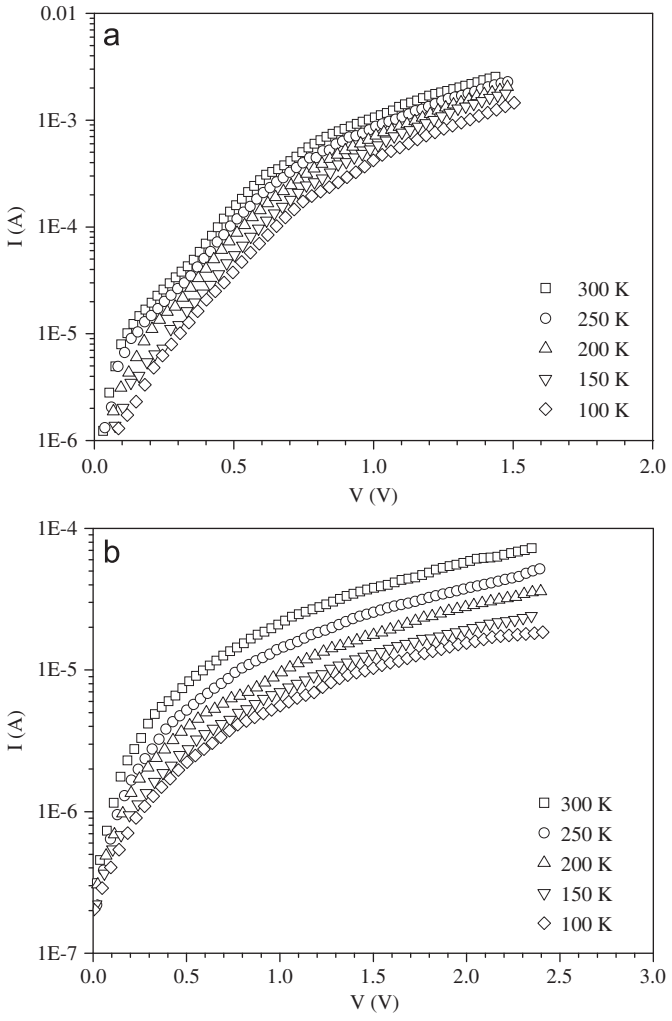

Fig. 5. The semi-logarithmic forward bias I–V characteristics of a Cu/CdS/SnO_2 structure with (a) CdS prepared at 300 K and (b) CdS prepared at 200 K.

Fig. 5 shows a set of the semi-logarithmic forward bias I–V characteristics of Cu/CdS/SnO_2 structures measured at different temperatures ranging from 100 K to 300 K. The ln(I)–V curves of Cu/CdS (at 300 K)/SnO_2 structure depict linear behavior in the range of $0.1\ V < V < 0.7$ V bias voltages (Fig. 5a). The I–V characteristics of the Cu/CdS (at 200 K)/SnO_2 structure are linear on a semi-logarithmic scale at low forward-bias voltage ($0\ V < V < 0.3$ V) and deviate significantly from linearity at high bias voltage because of the effect of serial resistance (Fig. 5b). The experimental values of n, I_0 and ϕ_{b0} were given in Table 1. As can be seen in Table 1 the ideality factor n increases while the zero bias barrier height ϕ_{b0} decreases with decreasing temperature. Such behavior may be due to the Schottky barrier height potential inhomogeneity between the metal and semiconductor layer [37,38]. The Schottky barrier has formed parallel inhomogeneous patches of different barrier heights [39,40]. The larger ideality factor is due to patches with a lower barrier, and vice versa [41]. Also it can be seen from Table 1 that the values of saturation current and ideality factor of Cu/CdS (at 300 K)/SnO_2 structure are higher than that of Cu/CdS (at 200 K)/SnO_2. The higher saturation current and ideality factor of Cu/CdS (at 300 K)/SnO_2 structure can be attributed the porous surface and randomly sized grains of CdS deposited at room temperature [12,13,15]. Ideality factors of all samples are greater than unity, which indicates that thermionic emission is not the only conduction mechanism for current flow. The high value of n may be due to potential drop in the interfacial layer between the metal and semiconductor layers [40]. High n values have been reported for several nano-structured devices [13,14].

The thermionic emission current–voltage relation of a Schottky diode with series resistance is given by [36]

$$I = I_0[e^{q(V-IR_S)/nkT} - 1] \tag{9}$$

where R_s is serial resistance. Eq. (9) can be differentiated as follows:

$$\frac{dV}{d(\ln I)} = IR_S + \frac{nkT}{q} \tag{10}$$

The series resistances are evaluated by using the slopes of $dV/d(\ln I)$ versus I curves. Fig. 6 shows $dV/d(\ln I)$ versus I plots for the Cu/CdS (at 200 K)/SnO_2 structure. The series resistances in the range of the investigated temperature values are listed in Table 1. The high series resistance of the Cu/CdS (at 200 K)/SnO_2 structure may be attributed to the high resistivity of the CdS film prepared at 200 K [42]. Resistivity values of the CdS samples prepared at 300 K and 200 K are 28.6 Ω cm and 73.7 Ω cm, respectively. The series resistance of the ideal Schottky diode is in the order of the bulk resistivity. The non-ideality induces an increase for the series resistance [11,42].

The I–V characteristics in a double logarithmic plot of Cu/CdS (at 300 K)/SnO_2 and Cu/CdS (at 200 K)/SnO_2 structures were investigated at all temperatures. Fig. 7 shows the double logarithmic forward bias I–V plots at only 300 K. As can be seen from Fig. 7, the forward bias characteristic of the Cu/CdS(at 300 K)/SnO_2 structure has three distinct linear regions with different slopes. The device shows the

Table 1
Experimental values of n, I_0, ϕ_{b0} and R_s.

T (K)	T_s=300 K				T_s=200 K			
	I_0 (A)	n	ϕ_{b0} (eV)	R_s (Ω)	I_0 (A)	n	ϕ_{b0} (eV)	R_s (kΩ)
300	4.16×10^{-6}	5.44	0.57	89.7	2.89×10^{-7}	3.14	0.64	3.14
250	3.37×10^{-6}	6.72	0.47	97.8	1.88×10^{-7}	3.54	0.54	4.22
200	2.60×10^{-6}	8.51	0.38	104.2	2.22×10^{-7}	5.02	0.42	5.89
150	1.53×10^{-6}	10.89	0.28	107.8	1.95×10^{-7}	7.48	0.31	7.09
100	1.20×10^{-6}	16.73	0.18	118.4	1.91×10^{-7}	13.25	0.20	8.94

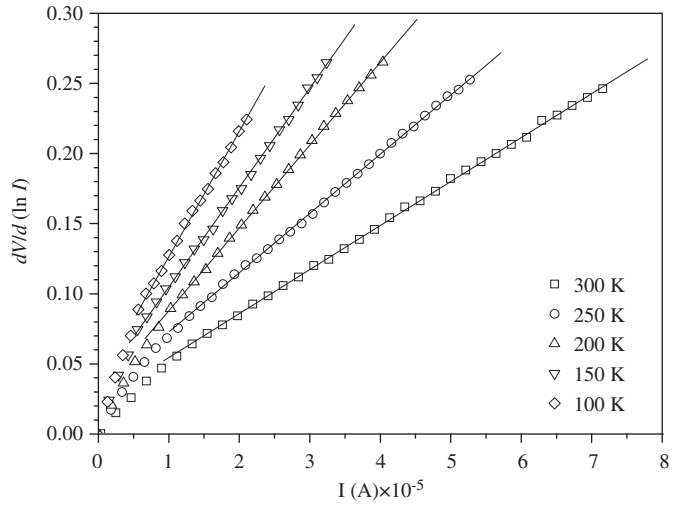

Fig. 6. Experimental $dV/d(\ln I)$ versus I plots for the Cu/CdS (at 200 K)/SnO_2 structure.

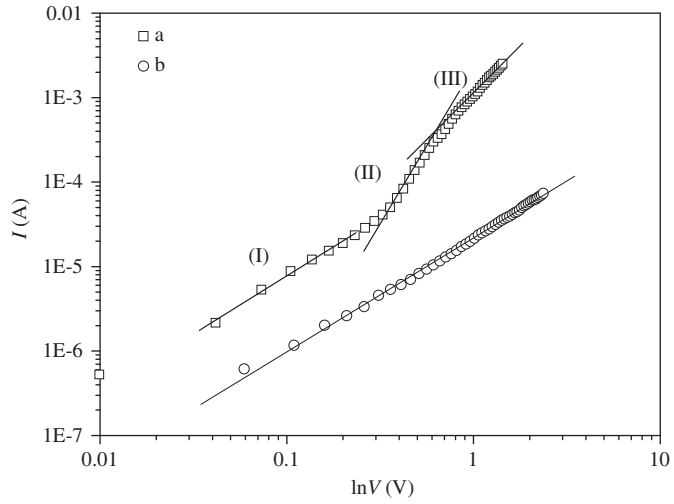

Fig. 7. Double logarithmic forward bias I–V plots of a Cu/CdS/SnO_2 structure at 300 K with (a) CdS prepared at 300 K and (b) CdS prepared at 200 K.

same behavior at all temperatures. This result indicated that there are different conduction mechanisms for the Cu/CdS (at 300 K)/SnO_2 structure. The region I shows an Ohmic behavior with slopes about unity (~1.4). Furthermore, at relatively small bias voltage the I–V dependency is close to $V^{3/2}$. Such I–V dependencies are indicative of the contribution of the tunneling process [35]. The double logarithmic I–V plot with a slope larger than two (~3.5) at region II suggests the possibility of the space charge limited current mechanism (SCLC) [43,44]. The slope of the region III in the double logarithmic forward bias characteristic is found to be about 2.4. At higher voltages the slope tends to decrease because the device approaches the 'trap-filled' limit, when the injection level is high, whose dependence is the same as in the trap-free space-charge-limited current [35,45]. The double logarithmic I–V plot of the Cu/CdS (at 200 K)/SnO_2 structure has one linear region. Similar behavior for the double logarithmic I–V characteristic was reported by Patel et al. [13] for the Au/nano-CdS Schottky junction.

In practice, tunneling mechanism is very significant for semiconductors with $E_{00}=10$ meV or a doping level higher than $\sim 1\times 10^{17}\,cm^{-3}$ [41]. The carrier concentration of CdS prepared at 300 K is determined to be $1.91\times 10^{17}\,cm^{-3}$. Therefore, the tunneling mechanism was investigated for Cu/CdS (at 300 K)/SnO_2 structure. Tunneling mechanism can occur as two mechanisms: (i) field emission (FE) (ii) thermionic field emission (TFE). TFE theory is the dominant mechanism in the intermediate temperature and doping concentration, but FE theory is dominant only at quite low temperatures for the material having high doping concentrations [36]. The low, moderate or intermediate and high doping levels are about 10^{13}–$10^{14}\,cm^{-3}$, 10^{15}–$10^{16}\,cm^{-3}$ and 10^{17}–$10^{19}\,cm^{-3}$, respectively. Current–voltage relation for tunneling mechanism is given by [46,47]

$$I_t = I_{t0}(e^{(qV_a/E_0)}) \tag{11}$$

where

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right). \tag{12}$$

E_{00} is the characteristic energy; it is expressed as

$$E_{00} = \frac{h}{4\pi}\sqrt{\frac{N_d}{m_e^*\varepsilon_S}} \tag{13}$$

According to the theory, FE is the dominant mechanism if $E_{00} \gg kT$, TFE is the dominant mechanism if $E_{00} \sim kT$ and the dominant mechanism is the thermionic emission–diffusion for $E_{00} \ll kT$. The slope of $\ln(I)$–V plot does not change with temperature for FE and it is equal to q/nkT for the TFE. So the ideality factor n can be written as

$$n = \frac{E_{00}}{kT}\coth\left(\frac{E_{00}}{kT}\right) \tag{14}$$

Fig. 8 shows a plot of n versus T for all samples. The solid line shows values of n calculated from Eq. (14) for $E_{00}=143$ meV. It can be seen from Fig. 8 that the calculated values of n depict a good fitting with experimental values of the Cu/CdS (at 300 K)/SnO_2 structure. This value of E_{00} is greater than kT, so it can be said that the FE mechanism is the dominant current transport mechanism for the Cu/CdS (at 300 K)/SnO_2 structure. Also, the tunneling mechanism was investigated for the Cu/CdS (at 200 K)/SnO_2 structure. The dashed line shows values of n calculated from Eq. (12) for $E_{00}=82$ meV. It was determined from Fig. 8 that the calculated values of n depict a good fitting with experimental values of the Cu/CdS (at 200 K)/SnO_2 structure in the range of 200–300 K. According to this result it can be said that the dominant conduction mechanism of this diode changes at ~200 K [48]. Recombination mechanism becomes dominant only for large barrier

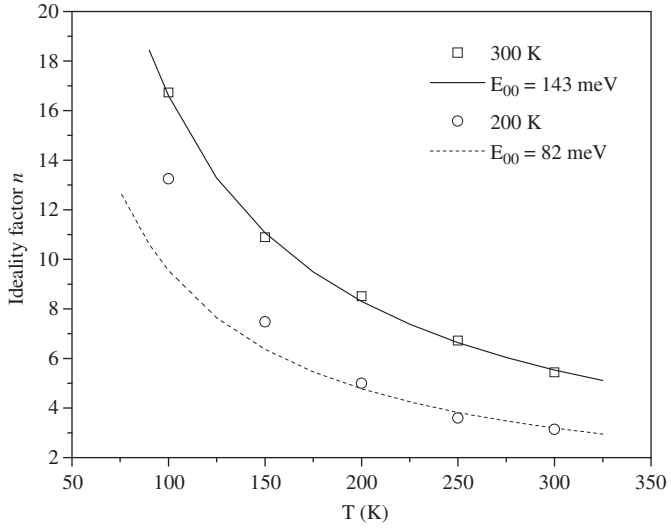

Fig. 8. The plot of n versus T for Cu/CdS/SnO_2 structure with (a) CdS prepared at 300 K and (b) CdS prepared at 200 K.

height, low temperature and lightly doped semiconductor of low carrier lifetime. The CdS sample prepared at 200 K has lower carrier concentration ($1.97\times10^{16}\,cm^{-3}$) than that of the sample prepared at 300 K and the barrier height of the Cu/CdS (at 200 K)/SnO_2 structure is higher than that of the Cu/CdS (at 300 K)/SnO_2 structure (Table 1). Therefore, this behavior at low temperatures can be explained by increase of the recombination contribution on the conduction mechanism.

4. Conclusion

In this study, CdS thin films on SnO_2 coated glass substrate were deposited at low substrate temperature by vacuum evaporation method. X-ray diffraction studies showed that the textures of the CdS/SnO_2 structure are hexagonal with a strong (0 0 2) preferred direction. In addition, a peak at $2\theta=\sim37.9^\circ$ in the XRD patterns was observed that is attributed to the existence of SnO_2 with tetragonal structure. The *c* lattice constants for the samples prepared at 300 K and 200 K are 6.683 Å and 6.711 Å, respectively. The band gaps of the samples are 2.38 eV (at 300 K) and 2.39 eV (at 200 K). The experimental *I–V* characteristics of the Cu/CdS/SnO_2 structure are significantly affected by the sample preparation temperature. The *I–V* characteristic of the Cu/CdS (at 200 K)/SnO_2 structure deviates from exponential behavior due to the high series resistance. The Schottky barrier of two devices has formed parallel inhomogeneous patches of different barrier heights. Ideality factors of all samples are greater than unity, which indicates that thermionic emission is not the only conduction mechanism for the current flow. The results indicate that the current transport in the Cu/CdS (at 300 K)/SnO_2 structure in the whole temperature range can be controlled by the tunneling at low bias voltages and SCLC at high bias voltages. However, the current transport mechanism in the Cu/CdS (at 200 K)/SnO_2 structure is the tunneling in the range of 200–300 K. It was determined that the surface morphology of CdS samples is important in determining the quality of the Schottky diode.

References

[1] M.A. Contreras, B. Egaas, K. Ramanathan, J. Hiltner, A. Swartzlander, F. Hasoon, R. Noufi, Prog. Photovoltaics: Res. Appl. 7 (1999) 311.
[2] A.I. Oliva, R. Castro-Rodriguez, O. Solis-Canto, V. Sosa, P. Quintana, J.L. Pena, Appl. Surf. Sci. 205 (2003) 56.
[3] J.P. Enriquez, X. Mathew, Sol. Energy Mater. Sol. Cells 76 (2003) 313.
[4] S. Guduru, V.P. Singh, S. Rajaputra, S. Mishra, R. Mangu, I. Omer St., Thin Solid Films 518 (2010) 1809.
[5] A.A.M. Farag, I.S. Yahia, M. Fadel, Int. J. Hydrogen Energy 34 (2009) 4906.
[6] H. Uslu, Ş. Altındal, İ. Polat, H. Bayrak, E. Bacaksız, J. Alloys Compd. 509 (2011) 5555.
[7] H. Uslu, A. Bengi, S.Ş. Çetin, U. Aydemir, Ş. Altındal, S.T. Aghaliyeva, S. Özçelik, J. Alloys Compd. 507 (2010) 190.
[8] E. Arslan, Ş. Altındal, S. Özçelik, E. Ozbay, Semicond. Sci. Technol. 24 (2009) 075003.
[9] E. Arslan, Ş. Altındal, S. Özçelik, E. Ozbay, J. Appl. Phys. 105 (2009) 023705.
[10] A. Tataroğlu, Ş. Altındal, Microelectron. Eng. 85 (2008) 233.
[11] A. Keffous, M. Siad, S. Mamma, Y. Belkacem, C.L. Chaouch, H. Menari, A. Dahmani, W. Chergui, Appl. Surf. Sci. 218 (2003) 336.
[12] S. Oktik, G.J. Russell, J. Woods, Semicond. Sci. Technol. 2l (1987) 661.
[13] K. Patel, K.K. Nanda, S.N. Sahu, J. Appl. Phys. 85 (1999) 3666.
[14] S.K. Mandal, A.B. Maity, J. Dutta, R. Pal, S. Chaudhuri, A.K. Pal, Phys. Status Solidi A 163 (1997) 433.
[15] V.V. Kislyuk, M.I. Fedorchenko, P.S. Smertenko, O.P. Dimitriev, A.A. Pud, J. Phys. D: Appl. Phys. 43 (2010) 185301.
[16] B. Lepley, P.H. Nguyen, C. Boutrit, S. Ravelet, J. Phys. D: Appl. Phys. 12 (1979) 1917.
[17] T.D. Dzhafarov, M. Serin, D. Ören, B. Süngü, M.S. Sadıgov, J. Phys. D: Appl. Phys. 32 (1999) L5.
[18] M.A. Martinez, C. Guillen, J. Herrero, Appl. Surf. Sci. 140 (1999) 182.
[19] S.J. Ikhmayies, R.N. Ahmad-Bitar, Sol. Energy Mater. Sol. Cells 94 (2010) 878.
[20] S.Y. Kim, D.S. Kim, B.T. Ahn, H.B. Im, J. Mater. Sci.: Mater. Electron. 4 (1993) 178.
[21] H. El-Maliki, J.C. Bernede, S. Marsillac, J. Pinel, X. Castel, J. Pouzet, Appl. Surf. Sci. 205 (2003) 65.
[22] A.I. Oliva, O. Solís-Canto, R. Castro-Rodríguez, P. Quintana, Thin Solid Films 391 (2001) 28.
[23] K.S. Ramaiah, V.S. Raja, M. Sharon, J. Mater. Sci.: Mater. Electron. 9 (1998) 261.
[24] B. Ullrich, J. Mater. Sci.: Mater. Electron. 18 (2007) 1105.
[25] S.A. Al Kuhaimi, Vacuum 51 (1998) 349.
[26] K. Senthil, D. Mangalaraj, Sa.K. Narayandass, R. Kesavamoorthy, G.L.N. Reddy, Nucl. Instrum. Methods B 173 (2001) 475.
[27] J.H. Lee, Appl. Surf. Sci. 252 (2005) 1398.
[28] M. Tomakin, M. Altunbaş, E. Bacaksız, İ. Polat, Mater. Sci. Semicond. Process. 14 (2011) 120.
[29] E. Bacaksiz, B.M. Basol, M. Altunbaş, S. Yılmaz, M. Tomakin, B. Abay, Phys. Status Solidi B 244 (2007) 497.
[30] Z.C. Feng, C.C. Wei, A.T.S. Wee, A. Rohatgi, W. Lu, Thin Solid Films 518 (2010) 7199.
[31] V.D. Novruzov, N.M. Fathi, O. Gorur, M. Tomakin, A.I. Bayramov, S. Schorr, N. Mamedov, Phys. Status Solidi A 207 (2010) 730.
[32] R. Sathyamoorthy, S. Chandramohan, P. Sudhagar, D. Kanjilal, D. Kabiraj, K. Asokan, Sol. Energy Mater. Sol. Cells 90 (2006) 2297.
[33] R. Swanepoel, J. Phys. E: Sci. Instrum. 16 (1983) 1214.
[34] U. Pal, R.S. Gonzalez, G.M. Montes, M.G. Jimenez, M.A. Vidal, S. Torres, Thin Solid Films 305 (1997) 345.
[35] T.B. Jomaa, L. Beji, A. Ltaeif, A. Bouazizi, Mater. Sci. Eng. C 26 (2006) 530.
[36] D.K. Schroder, Semiconductor Materials and Device Characterization, Wiley, New York, 1990.
[37] R.T. Tung, Phys. Rev. B 45 (1992) 13509.
[38] J.H. Werner, H.H. Guttler, J. Appl. Phys. 69 (1991) 1522.
[39] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. 70 (1991) 7403.
[40] R.T. Tung, Mater. Sci. Eng. R: Rep. 35 (2001) 1.
[41] A.M. Rodrigues, Appl. Surf. Sci. 253 (2007) 5992.
[42] J.H. Lee, J.S. Yi, K.J. Yang, J.H. Park, R.D. Oh, Thin Solid Films 431–432 (2003) 344.
[43] S. Aydogan, M. Saglam, A. Türüt, J. Phys.: Condens. Matter 18 (2006) 2665.
[44] Z. Ahmad, M.H. Sayyad, Physica E 41 (2009) 631.
[45] Ö. Güllü, S. Aydoğan, A. Türüt, Microelectron. Eng. 85 (2008) 1647.
[46] F.A. Padovani, R. Stratton, Solid-State Electron. 9 (1966) 695.
[47] C.R. Crowell, V.L. Rideout, Solid-State Electron. 12 (1969) 89.
[48] A.L. Fahrenbruch, R.H. Bube, Fundamentals of Solar Cells and Photovoltaic Solar Energy Conversion., Academic Press, California, 1983.