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Effects of silicon surface defects on the graphene/silicon Schottky characteristics

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ABSTRACT

Distinct characteristics and yet adverse in some cases have been widely reported in the graphene/silicon Schottky junction under DC biasing, for biological and chemical sensing, or as a photodetector. The explanations to these observations are often attributed to the nature of the graphene layer but are still far from satisfactorily for many cases. In this work, we conducted a detailed analysis on both the forward and reverse current-voltage characteristics under different temperatures and we proposed that the silicon surface defects, which had been well-known as P_{b0} centers or ≡Si, should play an important role in the adverse characteristics observed in the Gr/Si junction. Compared with the metal/Si and oxide/Si interface, the graphene-isolated P_{b0} centers at the Gr/Si interface are chemically inactive but are still electrically active and that modify the carrier transportation over the junction barrier. Without efficient chemical passivation, the graphene-covered Si surface should maintain the most native Si surface such that it preserves a much higher amount of P_{b0} centers as compared with other Si junctions or interfaces. This should be the main origin for the reported adverse current-voltage characteristics.

Introduction

The emerging of two-dimensional materials such as graphene, MoS_2, WSe_2, and phosphorene has shed new light on the material and electronic device applications with numerous excellent properties such as high electron mobility, high electrical and thermal conductivity, and low optical absorption coefficient which have never been found in the conventional semiconductor materials [1–3]. Graphene/silicon Schottky junction, as the most elemental and important structure, has attracted significant attention in the aspect of device research and sensing applications [4,7–9]. However, several fundamental issues of the graphene/silicon interface are still not well understood. Several puzzling issues, such as the wide distribution of Schottky barrier height, and large variation of the ideality factor (~1 to 30) were found from this simple structure [4,8–12]. The large range of the parameter values indicates that some different physics in addition to the Schottky emission should be involved. For chemical or biosensing properties, the measured characteristics were usually attributed to the nature of graphene itself [4–7]. For light sensing applications, most studies attributed the characteristics to the carrier generation from the depletion layer of junction in the silicon side [5–6,10]. Seldom reports discuss the role of the silicon surface defects which has been well-known for decades and has been extensively studied in (metal–oxidesemiconductor (MOS) community [13–17]. As compared with an un-passivated silicon surface, the 2D graphene surface should have a much lower surface defect density. We are inclined to believe that the Gr/Si interface and hence some of the device properties, to a certain extent, should be affected by the silicon surface [18]. This work intends to explore some possible correlations of the adverse characteristics of the Gr/Si junction to the silicon surface defects.

In this work, we propose the possible interactions of silicon surface defects in the charge transport characteristics. We shall conduct a detailed investigation on both the forward and the reverse current–voltage-temperature (I-V-T) characteristics in the elemental graphene/silicon junction. From the measurements, we reveal several adverse characteristics such as a larger non-ideality factor, a smaller value of potential barrier. By extending reverse bias up to 90 V, the adverse temperature dependence of the low-bias reverse current was found in comparison with the large reverse bias ones. We further proposed models and mechanisms for explaining these characteristics based on the framework of charge trapping-detrapping and trap-assisted conduction involving the silicon surface defects. The experimental details

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are given in the next section. The third section highlights the formula to be used for the parameter extraction and it also provides the definitions for the key parameters we are going to discuss. In the forth section, we shall report the experimental results. To explain the experimental observations, we first highlight the properties of silicon surface defects, P_{b0} centers, and then new models on the charge trapping-detrapping and current conduction involving P_{b0} centers for Gr/Si Schottky junction will be proposed the fifth section. Finally, we summarize the major outcomes and their implications in the last section.

Materials and methods

The starting substrate was a lightly-doped n-type Si wafer with resistivity in the range of 2 to 4 Ω-cm. After standard cleaning, a 285 nm thick oxide layer was first thermally grown. Top metal electrode forming by 5 nm thick Cr and 70 nm thick Au layer was deposited by vacuum evaporation. Then a 500 × 500 μm^2 window which is the active region of the Schottky diode was defined by photolithography patterning. The graphene layer was grown separately by chemical vapor deposition (CVD) on a copper foil. The 2D structure of the graphene layer is confirmed by Renishshaw RM2000 Raman spectroscopy with a wavelength of 532 nm. The graphene layer showed a weak D (1350 cm^{-1}) feature, a sharp G (1580 cm^{-1}) peak, and a strong 2D (2690 cm^{-1}) peak. To remove the backing copper foil, we coated the top surface of the as-deposited graphene layer with Allresist AR-26 polymethylmethacrylate (PMMA), then the copper layer was etched away by using copper sulfate hydrochloric acid solution (formula $CuSO_4$:HCl:H_2O = 10 g:50 ml:50 ml). The PMMA-supported graphene layer was repeatedly cleaned with DI water four times to minimize the potential contamination of copper residues in the final devices. The PMMA coated graphene layer was then transported and placed onto the patterned Si substrate. Immediately prior to the graphene transfer, the defined region was further etched by using a buffered oxide etchant in order to remove the native oxide and to have better Schottky contacts. The top PMMA layer was removed by dipping the wafer in dichloromethane (DCM) solution with a temperature of 45 °C for 4 min. and the wafer then was washed in acetone and isopropyl solutions each for 5 min. The graphene layer outside the electrode and active windows are removed by oxygen plasma etching. The current–voltage (I-V) characteristics were measured using an Agilent B1500 Semiconductor Analyzer with a probe station with a temperature-control hot stage.

Current-voltage characteristics and parameter extraction

The current–voltage characteristic of a Schottky junction derived from the thermionic emission theory is [19,20]:

$$I = AA^*T^2 exp\left(-\frac{\Phi_B}{kT}\right)\left(exp\left(\frac{qV}{nkT}\right)-1\right) \quad (1)$$

where A is the junction area, Φ_B is the Schottky barrier height, q is the elementary charge, k is the Boltzmann's constant, T is the absolute temperature, and n is the ideality factor.

The effective Richardson constant, A^*, in (1) is given by

$$A^* = \frac{4\pi q m^* k^2}{h^3} \quad (2)$$

where m^* is the carrier effective mass and h the Planck constant. For electron current in silicon Schottky junction, the Richardson constant is about 112 $A{\cdot}cm^{-2}{\cdot}K^{-2}$ [19–20]. Minor adjustments may be made by using a slightly different value of effective mass.

For the case of non-negligible series resistance, R, due to the contact and the silicon substrate, (1) is revised to [21]:

$$I = AA^*T^2\exp\left(-\frac{\Phi_B}{kT}\right)\left(\exp\frac{q(V-IR)}{nkT}-1\right) \quad (3)$$

The parameters, R, and n in (3) can be extracted by plotting $\frac{dV}{d(\ln I)}$ versus I based on the following equation:

$$\frac{dV}{d(\ln I)} = IR - \frac{kT}{q}n \quad (4)$$

The barrier height, Φ_B, can be further deduced from (3) with the given value of R and n as [21]

$$H = V - \frac{nkT}{q}\ln\frac{I}{AA^*T^2} = IR + n\Phi_B \quad (5)$$

Considering the nature of massless fermions behavior of electron transport in the graphene plane, it was suggested that the Richardson constant defined in (2) is no longer appropriate for the Gr/Si Schottky barrier. Liang *et al.* proposed that the Schottky current should be revised to [22]:

$$J = A^*T^3\exp\left(-\frac{\Phi_B - E_F}{kT}\right)\left(\exp\frac{q(V-IR)}{nkT}-1\right) \quad (6)$$

where E_F is the Fermi level of graphene and the Richardson constant is expressed in terms of the fermion velocity, v_f, as:

$$A^* = \frac{qk^3}{\pi\hbar^3 v_f^2} \quad (7)$$

Note that the approach for ideality factor and series resistance extraction given in (4) is still valid for (6).

Experimental results

Forward characteristics

Fig. 1(a) depicts the forward I-V characteristics of the fabricated graphene/Si Schottky junction at different temperatures. The current level increases with temperature. A slope change is noted for a voltage greater than 0.6 V and it is more obvious for higher temperatures. The smaller increase of current level at larger voltage can be attributed to the large series resistance which in effect reduces the voltage across the junction when the forward current is large. It looks like that the curves measured at different temperatures tend to merge together at a large forward bias. It indicates that some non-thermally activated processes should contribute more significantly to the current conduction in this region. To make the analysis and parameter extraction simpler, we focus on the low voltage region only. We performed the parameter extraction with the equations (4) and (5). Fig. 1(b) plots $dV/d(\ln I)$ as a function of I at different temperatures. The plot shows quite a linear relationship for the low current or small forward bias region. Although it was suggested that the vanishing of the density of states at Dirac point could result in a tunable Fermi level of the graphene and give rise to a voltage controllable Schottky barrier height [23]. The present $d\ln I/dV$-I plot does not imply the need for including a voltage controllable Schottky barrier height in the current range we picked. The ideality factor and the series resistance for each curve can be extracted, respectively, from the intercept and slope based on (4). Fig. 1(c) plots the ideality factor (*i.e.* the n value in (3)) as a function of temperature. The ideality factor decreases monotonically from 3.7 at room temperature to 3.08 at 450 K. Similar trend and with a similar range of n value was observed in [24]. The ideality factor is larger than several other reports which have a value in the range of 1.1–2 [25,26]. Much larger values over 30 [9] were also reported but it is rare. Formulated from Landauer transport with the low density state of graphene, Sinha and Lee found that the ideal I-V curve of Graphene/Si Schottky should have an ideality factor near unity [12]. The silicon surface defects were not considered in the study. Several causes, such as the presence of thin oxide layer [27–28], image force lowering of the Schottky barrier due to the presence of interface charges, graphene Fermi level modification due to bias, Schottky barrier inhomogeneities, for the large ideality factor have been proposed

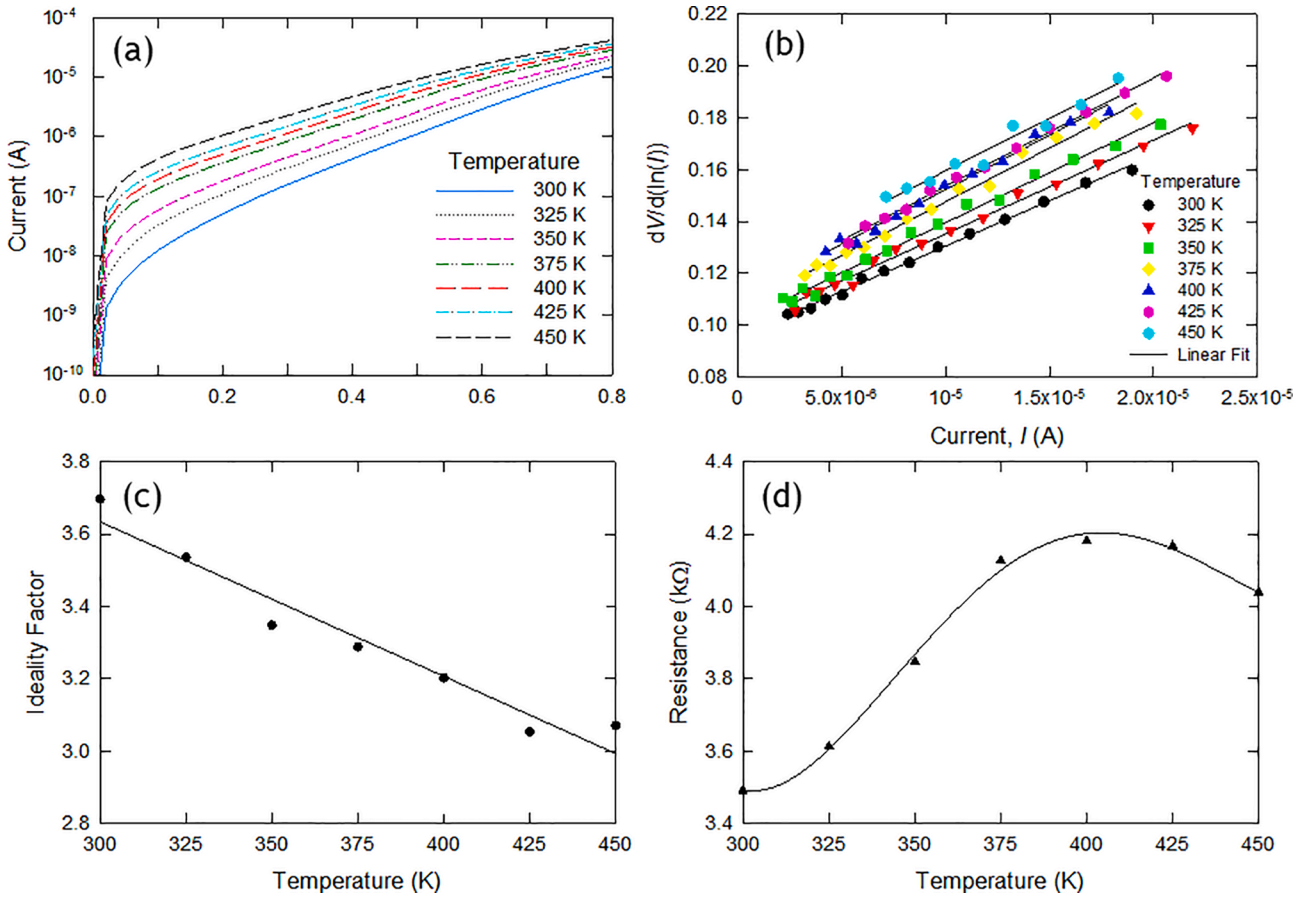

Fig.1. (a) Current-voltage characteristics of graphene/Si Schottky junction for temperature ranging from 300 K to 450 K. (b) $dV/d(\ln I) - I$ plot at different temperatures for parameter extraction; (c) plot of extracted ideality factor as a function of temperature; (d) plot of the extracted parasitic series resistance as a function of temperature.

[22,25–29]. Since our device's size is quite large, the potential barrier fluctuation should have been averaged out with the long correlation length of parameter fluctuation and the large cross-section area, junction inhomogeneity seems not to be the main cause. The presence of oxide or some interface defect states should be the main cause for the very large ideality factor [27–28]. Charge transport processes other than thermionic emission such as thermionic field emission or tunneling may enhance the junction current, especially at large biasing voltage. We shall further elaborate on this issue in next section.

Fig. 1(d) shows the extracted series resistance as a function of temperature. The resistance is in the range of several kilo-ohms which is much smaller than that reported by Luongo *et al.*[24]. In addition, instead of monotonically decrease with temperature reported in Ref. [24], our result shows a turn-around behavior which should be due to the use of lightly-doped substrate in this work. As the temperature rising from 300 to 450 K, the resistance first increases, peaks at around 400 K, and then decreases. This trend agrees with the temperature dependence of silicon resistivity. The resistance increases due to impurity scattering which is proportional to $T^{3/2}$. At higher temperatures, lattice scattering which is proportional to $T^{-3/2}$ will dominate the charge transport [20]. Despite of the large device size, the series resistance is still in the range of several kΩ which is the thousandth of that reported by Luongo *et al.* [24]. This result shows that the series resistance does affect the parameter extraction and needs to take the temperature effect into account in some cases. Because of the large series resistance and as well as the involvement of the other conduction mechanism, extracting the barrier height using (5) could be quite inaccurate and unreliable. Large temperature dependence of the barrier height was reported with this method [18,24]. Considering all these issues and the different temperature dependences given in (3) and (6) as well, we extracted the Schottky barrier from different temperatures instead of different voltages or currents.

Fig. 2 plots the current–temperature dependences based on the conventional Schottky equation given in (2) and Fermion-based model given in equation (6) for current taken at small reverse bias such that the effect of the bias dependence terms including series resistance and ideality factor had been reduced to a minimum. Both curves show quite a linear relation with $1/T$, the negative slopes representing the Schottky

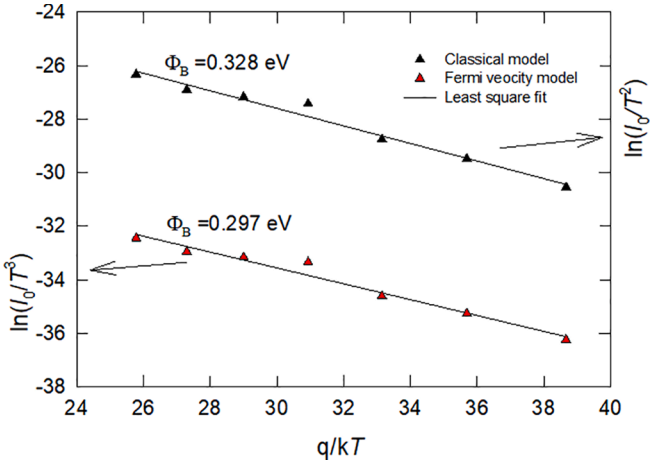

Fig. 2. Extraction of barrier height from reverse current- reciprocal temperature plot for Fermion model (left) and classical Schottky emission model (right).

barrier height, Φ_B. The rather linear curves in Fig. 2 show that there is no need to introduce additional temperature dependency for the barrier height under this situation. Other than about 0.031 eV smaller in the potential barrier for the Fermion-based model, from the mathematical point of view, both models are able to describe the temperature-dependent I-V characteristics satisfactorily. The barrier height value extracted from this present work is on the low side as compared with the reported values in the range of 0.11 to 0.86 eV [4]. The differences in the ideality factor and the barrier height should be due to the contribution of other current conduction mechanisms or may be due to the ways of parameter extraction in some cases. Since the major current in the forward conduction should come from the Schottky emission, it is difficult to have a clearer picture of the contribution of other kinds of conduction. In the next part of this section, we try to explore the possible conduction mechanisms under reverse biasing where the Schottky current should be much smaller.

Reverse characteristics

Fig. 3(a) plots the reverse current–voltage characteristics for the reverse bias up to −90 V. No junction avalanche breakdown was observed up to −90 V. The lightly doped substrate should make the surface depletion region of the junction too wide to have a breakdown voltage smaller than 90 V. The plot in Fig. 3 can be divided into two regions. For the low-voltage region ($|V| <\sim 60$ V), the current–voltage characteristics and its temperature dependencies look like don't have any order. They have different widths of quasi-saturation regions at different temperatures. In addition, the current levels and the slopes are quite random and do not follow the temperature trend at all. For example, at $|V| = 20$ V, the temperature order of the current magnitudes is 350 K < 300 K < 425 K < 375 K < 425 K. No conduction model can be applied to explain this "random" distribution. For the high-voltage region, the current increases almost exponentially (the near-linear curve for the semi-log plot of current versus voltage). The temperature dependence of the current level was restored to a monotonically increasing manner. The ordered characteristics at high voltages imply that the device and the measurements we made should be reliable and the measurements were repeatable. Considering the characteristics of the high-voltage portion, all the curves can be plotted with Fowler-Nordheim (FN) relationship as shown in Fig. 3(b) or Poole-Frenkel (PF) plot in 3(c) [20,30]. Considering the temperature dependence, the thermionic nature of Poole-Frenkel conduction looks more reasonable. We can also extract the barrier height in the same way as has been done in Fig. 2 by taking the current at $|V| = 60$ V at different temperatures. Again, the temperature dependence of the current follows quite well with $I \exp(-q\Phi_B/kT)$. The barrier height is 0.197 eV and 0.166 eV, respectively, for the classical model and the Fermion model (see Fig. 3 (d)). The value is about 0.1 eV smaller as compared with those extracted for the forward characteristics. Such a small value of barrier, even smaller than the forward ones is unexpected. In general, a reversely biased junction should have a larger barrier resulting from the band alignment. The smaller reverse barrier was also obtained and was

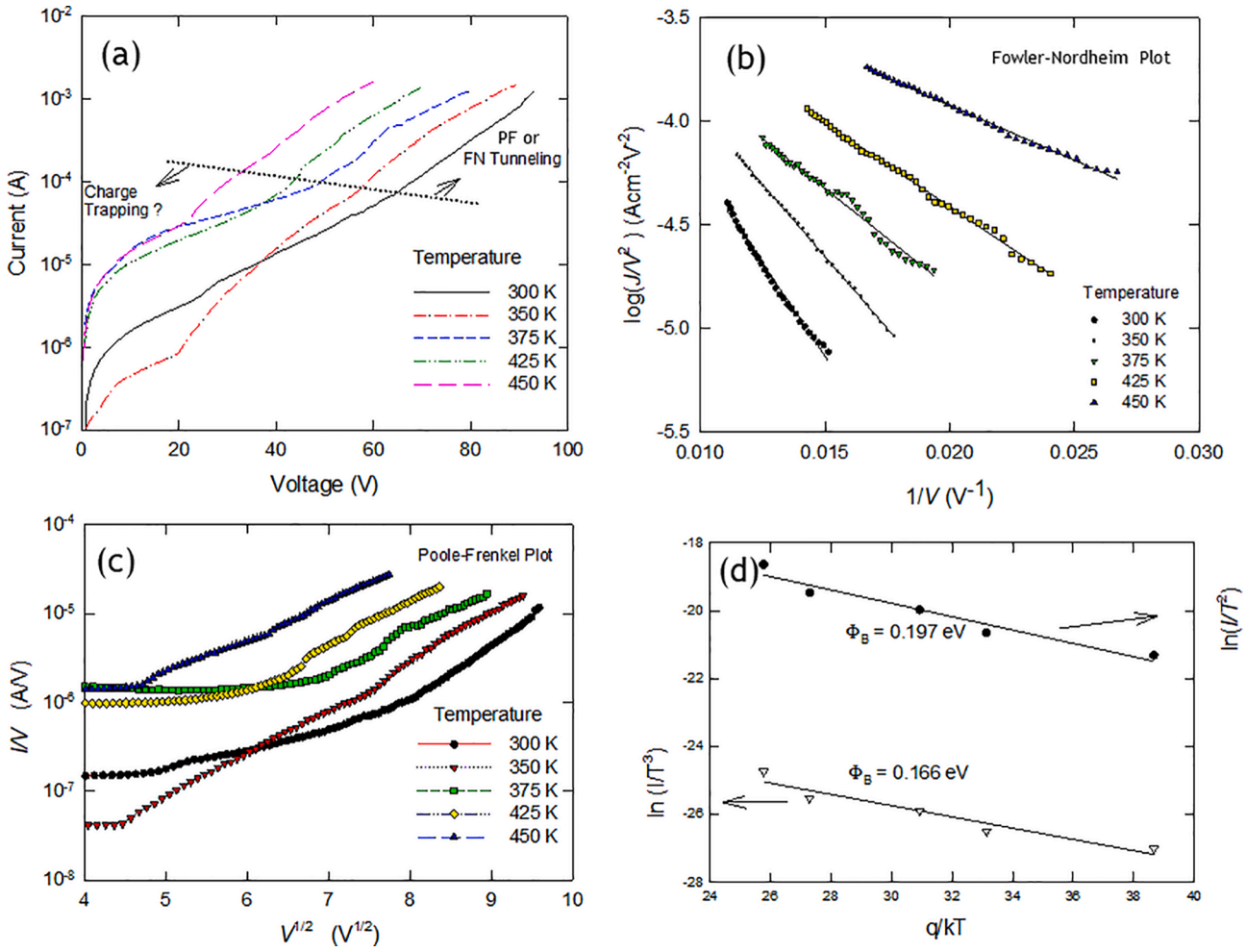

Fig.3. (a) Reverse current–voltage characteristics of Gr/Si Schottky diode showing two regions; (b) Fowler-Nordheim plot of the high-voltage region; (c) Poole-Frenkel plot of the high-voltage region; (d) extraction of barrier height from Arrhenius plot by using Fermion model (left) and classical Schottky emission model (right).

explained with the image force and electrostatic doping effects. Different from the metal/Si junction which has a constant Fermi level, the image charge induced by the depletion charge in silicon results in a higher Fermi level of graphene and lower the barrier height [31]. It was reported that the reverse Gr/Si junction current increase exponentially with the temperature at low temperature and tend to be saturated at high temperature [4,24]. The electrostatic doping or the shift of graphene Fermi level [31,32] can explain the increase of the reverse current but it failed to explain the saturation effect [24]. It is hard to attribute to the silicon substrate or the depletion layer on the silicon side as it should be more or less the same for the metal/Si Schottky junction but no similar phenomena were observed. Yet the change of the slope is just wrongfully attributed to the current solely by that thermionic emission. The difference in the two barrier height values, from the thermionic model and Ferimion model, is again 0.031 eV. Because of that, we tentatively ascribe the reverse current conduction at high-voltage to PF conduction. For small reverse bias, we are inclined to believe that the random characteristics should be related to surface defects at the graphene/silicon interface. Detail explanation is given in the next section.

Silicon surface defects and their effects

Before explaining the possible consequences of the silicon surface defects on the current conduction of Gr/Si junction, we first highlight the nature of the major silicon surface defect and its effect when interfacing with different materials. The 2D structure makes the graphene surface has a much lower surface defect density than most of the conventional semiconductor materials and is usually considered as an almost defect-free material. However, there are lots of dangling bonds on the silicon surface that have been well-known and have been investigated extensively, especially in the MOS community [13–17]. The conventional MOS transistor is basically a surface device and the current conduction and other device characteristics are governed by the surface or interface states to a great extent. A freshly-etched silicon surface is full of silicon dangling bonds which have been well-known as P_{b0} centers, $Si_3{\equiv}Si\cdot$, or $\equiv Si^{\cdot}$ for short [13–14]. Its density depends on the crystalline orientation; ⟨111⟩ surface has the highest amount of P_{b0} centers and ⟨100⟩ the lowest. Fig. 4 illustrates the ⟨100⟩ silicon surface interfacing with different materials with the presence of silicon dangling bonds,

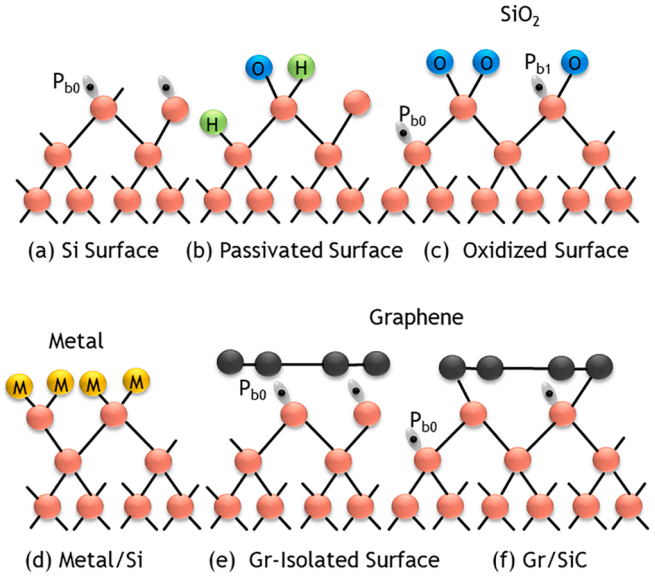

Fig.4. Illustration of Si surface interfacing to different materials: (a) bare silicon surface and surface dangling bonds or P_{b0} centers; (b) P_{b0} centers passivated with hydrogen and hydroxyl; (c) oxidized silicon surface; (d) metal/Si interface; (e) graphene/Si interface; (f) interface with Si/carbon covalent or Si/carbide bonding.

$\equiv Si\cdot$ (See Fig. 4(a)). A P_{b0} center is an amphoteric defect. It can capture both electrons and holes. The defects can be passivated with hydrogen or water-related hydroxyl group (see Fig. 4(b)). The number of surface defects can be reduced to the greatest extent by thermal oxidation (see Fig. 4(c)). SiO_2/Si interface was considered as one of the best interfaces with almost the lowest interface-state density in the order of 10^{10} to $10^{11}cm^{-2}\ eV^{-1}$. However, this low amount of interface state density is still the key factor in governing the threshold voltage value and results in several instability issues of MOS transistors. MOS devices were found to be more sensitive to light illumination which was also partially attributed to this kind of interface defect. Thermal annealing in hydrogen-containing forming gas is the general practice for passivating the SiO_2/Si interface states in the CMOS processes. For metal-silicon contact (see Fig. 4(d)), the metallic or silicide bonds may still affect the potential barrier of the metal-silicon junction but it attracted far less attention as the conductive layer make the defect effects to be fairly negligible in most cases. However, if there exists an oxide layer, charge trapping and detrapping associated with the P_{b0} centers would still occur. For graphene/Si interface, graphene may be able to form covalent bonding such as in the Gr/SiC structure (See Fig. 4(f)). However, it is not the case we have here as the graphene layer in this investigation is brought to the silicon surface by transportation and without a further high-temperature process for activating the chemical reaction. There should have no strong physical bonding (covalent or ionic) between the silicon and the 2D graphene layer. The graphene layer is attached to the silicon surface by van der Waal force or maybe more precisely the "charged defect"-dipole van der Waal force to account for the presence of P_{b0} centers. Since the hexagon opening the graphene crystal is so small (radius ~ 0.71 Å) that most of the atoms or molecules are too large to pass through the windows. Then we have a "new" nature of P_{b0} centers which are not chemically passivated but are physically isolated (see Fig. 4(e)). We can expect a very high amount of un-passivated dangling bonds which are chemically inactive but it is electronically active in the graphene/Si interface. Yoon *et al* observed a strong Fermi level pinning at the graphene/Si interface [33]. This observation can be attributed to the high amount of silicon surface defects as proposed. This kind of defect nature was not found in previous materials or electronic devices. The amphoteric P_{b0} centers behave as both donor level and acceptor level, namely, they can capture both electrons and holes.

It was confirmed both from experiments and *ab initio* calculations that the P_{b0} center appears as both acceptor-like and donor-like defects [13,14]. A P_{b0} center can capture both electron and hole (denoted as and e^- and h^+, respectively, in the following equations). For the acceptor-like feature, the P_{b0} center was found to have an energy level of about 0.27 eV under the silicon conduction band. It is electrically neutral (paramagnetic) when empty. It can be negatively charged (diamagnetic) when occupied by an electron

$$P_{b0} + e^- \rightarrow P_{b0}^- \tag{8}$$

The donor-like nature of the P_{b0} center has a level of about 0.25 eV above the top of the valance band. In this case, the defect is positively charged when empty, *i.e.*

$$P_{b0} + h^+ \rightarrow P_{b0}^+ \tag{9}$$

And is electrically neutral when occupied by an electron, *i.e.*

$$P_{b0}^+ + e^- \rightarrow P_{b0} \tag{10}$$

It is reasonable to assume that the aforementioned trapping and detrapping properties of the P_{b0} centers should remain at the graphene/silicon interface. The associated energy levels may be slightly different for van der Waal-P_{b0} bonding. It is worth further detailed investigation with quantum calculation [15–16] or to probe it with some electron spin resonance (ESR) experiments [14].

Fig. 5(a) shows some possible involvements of the P_{b0} centers in the current conduction under both forward and reverse biases. For the sake

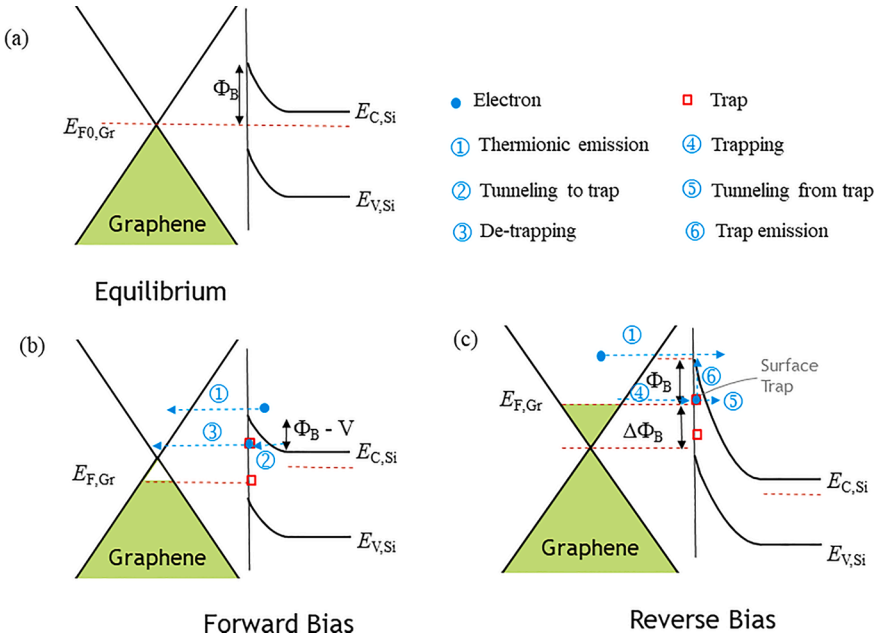

Fig. 5. Band alignment of Gr/n-type Si contact under: (a) equilibrium, (b) forward bias, and (c) reverse bias. (b) and (c) also show the involvement of silicon P_{b0} centers in the current conduction.

of simplicity, we do not discuss the hole trapping in this work. Hole trapping and detrapping should play a similar role, especially for a p-type silicon substrate. The mechanisms given in Fig. 5 can be readily modified to take hole trapping via (9) into account. Under forward bias and the n-substrate used in this work, the majority current should be thermionic emission of electrons from the silicon conduction band to the graphene conduction over the lowered barrier (see arrow labeled as ① in Fig. 5(b)). Some of the P_{b0} centers may capture electrons from the silicon conduction band (mechanism ②). The electron capturing may slightly modify the barrier and lower the current level. Some of the trapped electrons may be depopulated and transported into the graphene conduction band (via mechanism ③) under certain field strength and thermal energy. These effects may result in a different effective barrier and thus the ideality factor. Since the P_{b0} centers can capture both electrodes and holes. The actual current conduction model should be more complicated when taking the hole capture and emission into consideration. With the charge conduction model proposed above. For the forward current, the trap-assisted tunneling via mechanisms ② and ③ should contribute to the forward current but the thermionic current via ① should dominate the current flow in general. The trap-assisted tunneling may still enhance the total current and results in a different value of ideality factor in some cases. Considering the energy levels (E_C − 0. 27 eV and E_V + 0.25 eV) of P_{b0} centers found in the SiO_2/Si structure, it is reasonable to ascribe the ~ 0.2 eV barrier height at the Gr/Si interface derived from the forward current to the P_{b0}. Similar to many other reports, this conjecture needs further experimental and theoretical validation, however.

Many theories were proposed to explain the abnormally large values of the ideality factor. Some attribute the non-idealities to the Cu remnants which can serve as carrier recombination centers [34]. The copper defect in Si is close to the midgap (E_v + 0.52 eV) [35] and was not considered as a serious issue with the modern copper-based on metallization process. If Cu contamination was the root cause for the large non-ideality of Gr/Si junction, then similar results should also be often reported in other metal/Si Schottky diodes. Copper has now been widely used in IC manufacturing and had never been reported to have such a large ideality factor as reported in the Gr/Si diodes. In addition, the density of donor-like or acceptor-like P_{b0} centers on the silicon surface should be much higher than that of the copper midgap defects. And so far there is no similar characteristics or charge trapping-detrapping involving the defect level near the midgap was reported. On the contrary, the values of barrier height extracted from the forward and reverse I-V characteristics are closer to the energy levels of P_{b0} centers. Nevertheless, if the copper defect does play a role, its effect should be much smaller than that of the P_{b0} centers. Several researchers attributed the larger ideality factor to the barrier inhomogeneous [22,29]. Theoretically, including spatial distribution of the Schottky barrier should provide an additional degree for a better fitting of the current–voltage characteristics [36,37]. In this work, as our device sizes were quite large, we believe that the spatially inhomogeneous of the Schottky barrier should have been minimized. Liang attributed the origin of the inhomogeneous Schottky barrier to the random distributed “charged impurities” on the surface of the semiconductor [22]. Yet a more precise description of the “charged impurities” is the P_{b0} centers on the silicon surface. In this work, we report an ideality factor of about 4. This can be explained by the coupled defect level recombination involving the high amount of P_{b0} centers with two energy levels in the silicon bandgap. The ideality factor close to 2 is due to carrier recombination. Schenk and Krumbein found that the ideality factor can increase up to 4 if the recombination involves multiple defect levels [38]. The near “4” ideality factor together with other evidence or phenomena as shown, P_{b0} centers should be one of the main causes for producing large value of ideality factor of this work. For the cases of an even larger value of ideality factor, we believe this should be due to the existence of an oxide layer at the Gr/Si interface. Under this situation, the current conduction should be mainly due to tunneling and the ideality factor is not an appropriate way to characterize the current–voltage characteristics [18].

The model given in Fig. 5(c) can explain the adverse temperature dependence of the reverse current given in Fig. 3. Under reversed bias, the thermionic emission from graphene to silicon should be very small because of the large barrier (See Fig. 5(c)). As shown in Fig. 3, we observed “random” current–voltage characteristics for small reverse bias ($|V| < 60$ V). Charge trapping should occur due to the capture of electrons from the graphene layer (mechanism ④ in Fig. 5(c)) and that results in a lower current level and showing the first quasi-saturated region in the I-V curves. The different widths and levels of the quasi-saturation region are tentatively ascribed to the different energy levels and densities related to the defects [39]. In general, the charge trapping

is smaller at a higher temperature because of the detrapping or thermionic emission of the trapped charges (mechanism ⑥ in Fig. 5(c)). For a larger reverse bias, charge tunneling over the triangular edge or by tunneling from traps or field-assisted emission (mechanism ⑤) should dominate the current conduction. The "normal or ordered" I-V-T relationship for the magnitude of the reverse bias $|V| > 60$ V in Fig. 3 indicates that the charge trapping by the P_{b0} centers should have been reduced to a minimum due to the tunneling or field-assisted emission. In Fig. 3(d), the energy level derived from the reverse I-V characteristics is smaller than 0.2 eV which is even smaller than the forward barrier height. This energy level or barrier cannot be the contact potential as a result of band alignment between graphene and silicon which should be much larger according to Fig. 5(c). Because of that, direct tunneling or FN tunneling of electrons from the graphene conduction band to silicon conduction band cannot be the dominating current conduction path as they should be governed by the barrier height between the graphene and silicon also. The energy levels of P_{b0} are about 0.25 and 0.27 eV. Considering the electrostatic doping effect of graphene, the barrier may be lowered, the barrier heights obtained in Fig. 3 (d) look reasonable if we ascribe the reverse current to the P_{b0} center-assisted tunneling. We note the reverse characteristics we reported are not very common. The sample condition and biasing can lead to different shapes of the reverse I-V-T curves. If the samples were undergone with forming gas annealing, if the silicon surface is not freshly etched before the graphene transfer, or if the samples were stored in ambient with high humidity, the density of P_{b0} centers will be significantly reduced and the anomalous may not be very obvious. However, extending the measurement to a larger reverse bias, one should be able to observe similar behavior.

Conclusions

By conducting a detailed investigation on both the forward and the reverse current–voltage-temperature (I-V-T) characteristics, several findings, such as a large non-ideality factor, a small value of potential barrier, and adverse temperature dependence of the low-bias reverse current, smaller reverse bias barrier together implied that they should have arisen from the charge trapping-detrapping and trap-assisted conduction. It has been well-known that the silicon surface dangling bonds or P_{b0} centers can govern the electrical properties and device reliability of CMOS devices. However, this issue has hardly been addressed for the graphene/Si junction or graphene/Si interface studies. We have clearly manifested in this work that the weak van der Waal interaction between the Gr/Si should have preserved the native high density of P_{b0} centers on the silicon surface to the greatest extent. From an electrical point of view, the P_{b0} center should behave similar to other structures such as at the SiO_2/Si interface, it serves as both electron and hole trap. The carrier generation and recombination via the two trap energy levels led to an ideality factor close to 4 in the forward characteristics. That is, the defect centers can assist in the current conduction, and it should be more obvious in the reverse region because of the smaller thermionic current. It can be further inferred that the graphene isolated P_{b0} centers should be able to capture some kinds of gas molecules via charge-dipole interaction and that could be the key mechanism leading to the excellent chemical and biological sensing properties of the Gr/Si junction widely reported in the literature. This also implies that the electronic properties of the graphene/Si Schottky junctions could be improved by optimizing the processing and fabrication conditions.

Author contributions

H.W. conceived the experiment, analyzed the data, develop the theories, and wrote the article. M.A.A. performed the experiment, S.D. conceived the experiment, provided funding and facility supports, discussed the results.

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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