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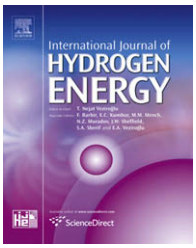

Electrical and photovoltaic characteristics of Al/n-CdS Schottky diode

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ABSTRACT

In this work, we have investigated the structure of the thermally evaporated CdS thin films. The electrical characteristics, such as capacitance–voltage *CV* and current–voltage *IV* measurements, of identically prepared Al/n-CdS structure were studied. The values of barrier height and ionized trap like-donors concentration were obtained from the reverse bias capacitance–voltage *CV* measurements at 1 MHz under different temperatures in the range 303–403 K. The effect of different illumination intensities were also investigated. Current–voltage *IV* measurement indicates two conduction mechanisms: a conduction limited by thermionic emission *TE* at lower forward voltages and space charge limited conduction *SCLC* regime at higher forward voltages. A qualitative description of *IV* characteristics under different illumination intensities was done. The reverse biased *IV* measurement under illumination exhibited a high photosensitivity as compared to the forward one. The former was explained in terms of minority carrier injection phenomenon. The photovoltaic parameters, such as open circuit voltage and short circuit current, were obtained.

1. Introduction

Semiconductor compounds of the II–VI group have drawn considerable interest due to their potential applications in photovoltaic devices, photo-resistors, heterojunction diodes, electroluminescent layers and surface acoustic wave devices. Chalcogenides, especially of cadmium, lead and zinc, have proved their potential as efficient absorbers of electromagnetic radiation [1–3]. Cadmium chalcogenides form a technically important class of materials owing to their widespread utility in a variety of electronic and optoelectronic devices [4]. CdS thin films are well known for their extensive applications as an optoelectronic material in solar cells [5] and photodetectors [4,6]. They are also used in the fabrication of optical filters, multilayer LEDs, photodiodes, phototransistors, etc. [6]. Heterojunction solar cells with a wide bandgap window and a narrow bandgap absorber are currently becoming the focus of intensive research in order to develop efficient, stable and low-cost cells. Cadmium sulfide, with a band gap of 2.43 eV, is an ideal material for use as the window layer of heterojunction solar cells [7,8]. A wide variety of techniques have been employed for the deposition of CdS thin films [9–11]. In this work, CdS films were deposited by the conventional thermal evaporation technique.

It well known that metal/semiconductor (MS) contacts are frequently used in integrated circuits, in light detectors and as solar cells. Schottky barrier diodes (SBDs) such as Al/CdS, which has a rectifying nature, are among the

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simplest MS contact devices [12–17]. The most important feature characterizing an SBD is its barrier height (BH). The existence of native oxide layer between metal and semiconductor influence the interface states and can modify the electrical properties of metal–semiconductor structures [18]. This layer plays an important role in the determination of Schottky barrier height and interface states. Since reliability and stability of all semiconductor devices are intimately related to their interface conditions, understanding of the interface physics with the help of metal–insulator–semiconductor diodes has great importance to the device operations [13,14].

The current–voltage IV characteristics of SBDs usually deviate from the ideal thermionic emission current model [1–3]. There are currently a vast number of reports of experimental studies of characteristic parameters such as the barrier height BH and ideality factor in a great variety of metal–semiconductor MS contacts [11,19–21]. Although analysis of the temperature-dependent current–voltage IV and capacitance–voltage CV characteristics of the SBDs gives detailed information about their conduction process or the nature of barrier formation at the MS interface, a complete description of the charge carrier transport through a MS contact is still a challenging problem. In spite of the numerous applications of Schottky barriers, the factors controlling the BH are not completely understood [22,23]. Apart from our work, and to the best of our knowledge, little information on the essential parameters and optoelectronic properties of Al/n-CdS devices semiconductor has been reported in the literature.

This work is relevant with the research activities on electrical properties of CdS-based devices for production of photovoltaic electricity. The photovoltaic electricity can be used for hydrogen generation which is a clean renewable fuel through water electrolysis [24,25].

In the present work, vacuum evaporated Al/n-CdS Schottky devices were prepared and investigated to identify the dominant current transport conduction mechanisms. The temperature dependence of the current–voltage and capacitance–voltage characteristics were analyzed in order to understand the effects of interface states and traps on the Al/n-CdS Schottky devices' behavior. Moreover, the sensitivity of Al/n-CdS Schottky devices using photovoltaic measurements was also discussed.

2. Experimental details

CdS thin films were prepared using the thermal evaporation technique with average thickness of 850 nm, deposited onto a pre-cleaned glass substrates separated 21 cm from the source of evaporation, which keeps substrate at room temperature during the deposition. A high vacuum coating unit (Edwards, E-306 A) was used. Thin films were deposited by using a molybdenum boat under vacuum of 2×10^{-5} Torr. The rate of deposition was 10 nm s^{-1} and the film thickness was controlled using a quartz crystal thickness monitor (FTM4, Edwards).

The structural characterization of CdS thin film was investigated using X-ray diffraction pattern. A Philips X-ray diffractometer (model X'-Pert) was used for the measurement of utilized monochromatic CuKα radiation operated at 40 kV and 25 mA. The diffraction patterns were recorded automatically with a scanning speed of 2°/min.

The ohmic and non-ohmic electrodes were evaporated on the CdS films as a coplanar configuration. Capacitance–voltage measurements were performed on Al/n-CdS devices using a computerized controlled 410 CV meter with an operating frequency at 1 MHz. The measurements were performed under a sweep of voltage from −10 to +10 V in the temperature range 303–403 K. The temperature of the device was recorded using chromel–alumel thermocouple (Type-K) connected to the temperature controller. Schematic diagram of the CV system is shown in Fig. 1. The measurements of the IV characteristics in dark were taken using a high internal impedance electrometer (Keithely 617A).

The source of light was a halogen lamp containing iodine vapor and tungsten filament. The intensity of light was measured with a solar power meter (TM-206, Taiwan). The intensity of light was varied by changing the distance between the device and the halogen lamp.

3. Results and discussion

3.1. Structure properties of CdS thin film

X-ray diffraction (XRD) pattern was recorded for the thermally evaporated CdS thin film as shown in Fig. 2. As observed, no phases other than CdS were present. According to the standard JCDPS card No. (77-2306), the structure is hexagonal with lattice parameters $a = 4.13$ Å and $c = 6.71$ Å [26–28] and the sharp diffraction peak at $2\theta = 26.59°$ corresponds to the (002) plane as the preferred orientation, compared to the other planes at $2\theta = 48.02°$ for (103) plane and $2\theta = 54.56°$ for (004) plane.

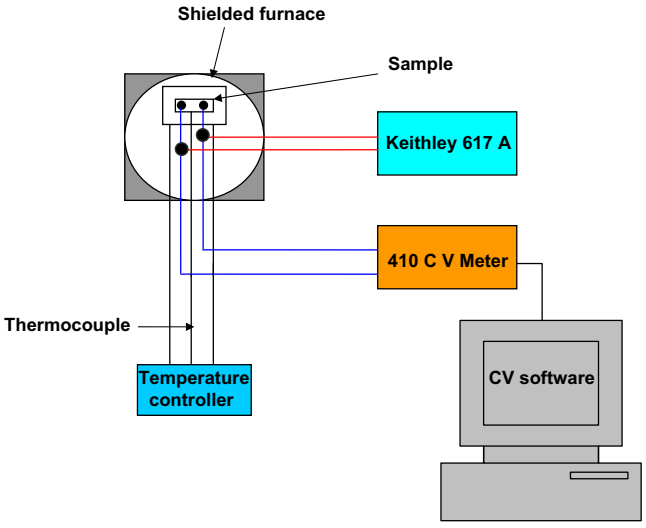

Fig. 1 – Schematic diagram of the computer controlled 410 CV meter and IV measurements.

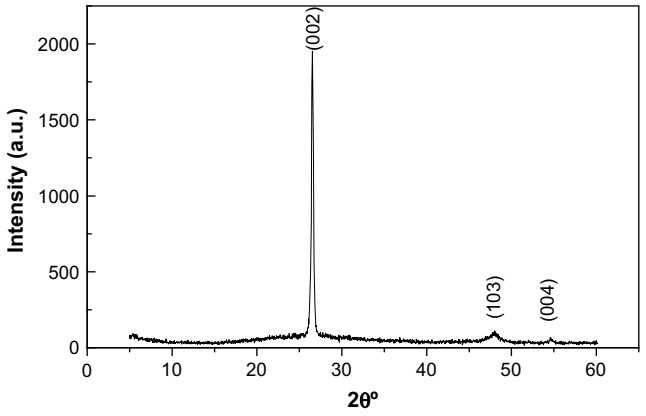

Fig. 2 – XRD pattern of the as-deposited CdS thin film.

3.2. *Capacitance–voltage measurements*

3.2.1. *Dark condition*

The dark capacitance–voltage CV dependence in both reverse and forward biasing voltages at different temperatures in the range 303–403 K at 1 MHz was studied. It is clear from Fig. 3 that at strong reverse bias ($V \leq -5$ V), the capacitance is bias independent which indicates that the sample is fully depleted. As the bias increases, a locally linear behavior is obtained in all temperatures and can be compared with the Mott–Schottky plot ($1/C^2$ versus V). This linear dependence occurs between −5 and 0 V. This dependence is assigned to the presence of traps acting as donors in the Al/n-CdS device, and allows estimation of their trap density. The depletion layer capacitance is defined as [18]:

$$C = \frac{dQ_c}{dV}, \tag{1}$$

where dQ_c is the incremental increase in charge upon an incremental change of the applied voltage dV. For one-sided abrupt junctions, the capacitance per unit area at equilibrium is given by [18]:

$$C = \frac{dQ_c}{dV} = \frac{d(qN_dW)}{d\left[q(N_d/2\varepsilon\varepsilon_o)W^2\right]} = \frac{\varepsilon\varepsilon_o}{W}, \tag{2}$$

where

$$W = \sqrt{\frac{2\varepsilon\,\varepsilon_o V_b}{qN_d}}, \tag{2a}$$

where N_d is the ionized traps like-donor, V_b is the built-in potential, q is the electronic charge, ε_o is the permittivity of free space, W is the width of the depletion region and ε is the relative permittivity of the CdS thin films. When a voltage is applied to the junction, the total electrostatic potential variation across the junction is given by $(V_b + V)$ for the reverse biasing, and by $(V_b - V)$ for the forward biasing. So, in the reverse case;

$$W = \left(\frac{2\varepsilon\,\varepsilon_o(V_b + V)}{q\,N_d}\right)^{1/2}. \tag{3}$$

If the measurements are carried out at sufficiently high frequencies, the charge at the interface states cannot follow an AC signal. This will occur when the time constant is too long to permit the charge carriers to move in and out of the states in response to an applied signal [18,29]. Thus the depletion layer capacitance can be expressed as:

$$C^{-2} = \frac{2\,(V_b + V)}{q\varepsilon\,\varepsilon_o A^2 N_d}, \tag{4}$$

where A is the area of the device. The slope of $1/C^2$ versus V relationship of the obtained lines, where we supposed that the traps are uniformly distributed in space in the range $(-5 \geq V \geq 0)$ at different temperatures gives the ionized traps like-donor N_d and V_b obtained from the extrapolation intercept of $1/C^2$ with the abscissa. The obtained values of N_d and V_b at different temperatures is tabulated in Table 1.

The built-in potential, V_b in a semiconductor devices equals the potential across the depletion region in thermal equilibrium. The obtained value of V_b is considered high as compared to the published data by Chen et al. [30], Bayhan [31], Montaha and Choudhury [32], and Habibe and Kavasoglu [33] for Ti/Au/CdS, Ag/CdS, CdTe/Cd and CdS/Cu(In,Ga)Se_2 devices, respectively.

The high values of V_b may be attributed to the dependence of built-in potential on the device fabrication processes and the measurement frequency. This suggests that either the traps are not uniformly distributed in space in contrary to our

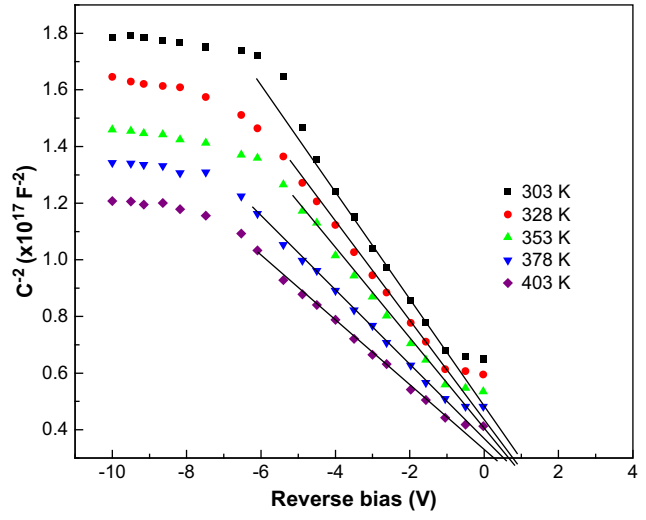

Fig. 3 – The dark capacitance–voltage dependence in both reverse and forward biasing at different temperatures for Al/n-CdS thin film.

Table 1 – Parameters calculated from the CV measurements.

T (K)	V_b (V)	$N_d/10^{14}$ (cm^{-3})	ϕ_b (eV)
303	0.95	7	1.27
328	0.74	8.2	1.9
353	0.56	8.7	0.92
378	0.42	10	0.81
403	0.31	12	0.72

supposition above. Therefore, our analyses remain as an estimation and the values obtained should be used as indicative rather than absolute. The value of the barrier height ϕ_b can be calculated using CV measurements by the following well-known equation:

$$\phi_b = V_b + V_P, \tag{5}$$

where V_P is the potential difference between the Fermi level and the top of the valence band in CdS and can be calculated knowing the carrier concentration N_d, and it is obtained from the following relation:

$$V_P = kT \ln\left(\frac{N_c}{N_d}\right), \tag{6}$$

where $N_c = 1.5 \times 10^{20}\ cm^{-3}$ is density of states in the conduction band for CdS [34]. Thus, the barrier height values for the Al/n-CdS device at different temperatures is calculated and given in Table 1. Fig. 4 shows the variation of the capacitance in the forward biasing. It is clear that the capacitance is nearly constant between 0 and 2 V followed by an increase between 2 and 6 V and finally a decrease above 7 V. The obtained results for the capacitance in the Al/n-CdS device suggest that the majority of the sample thickness is still depleted at the low voltage region 0 V. In this range of bias, the capacitance should increase but this is not observed, and indicates that the capacitance may be result of the contribution of both bulk and depletion parts [35]. Above 2 V, charge trapping by impurity states or intrinsic states of the bulk occurs, and then the capacitance increases. These traps are neutralized at higher voltages with significant carrier injection, and may be acted as recombination sites [35], which reduce the capacitance.

3.2.2. *Illumination condition*

Fig. 5 displays the capacitance of Al/n-CdS device under different light intensities without any bias voltage dependence and the corresponding depletion widths W were calculated. Results showed that the capacitance increases with increasing light power intensity. This behavior may be attributed to the shrinking of the depletion region width under illumination [36]. This suggests that even at zero bias and low optical bias, the depletion region quenches to its minimum value and the current collection becomes diffusion controlled.

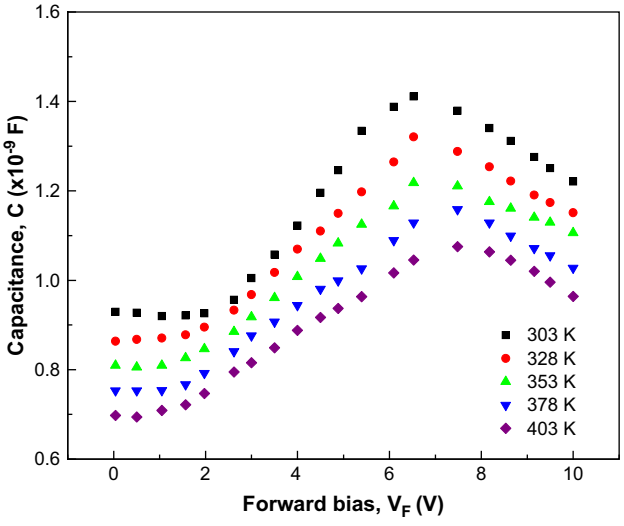

Fig. 4 – The variation of the capacitance in the forward biasing at different studied temperatures for Al/n-CdS thin film.

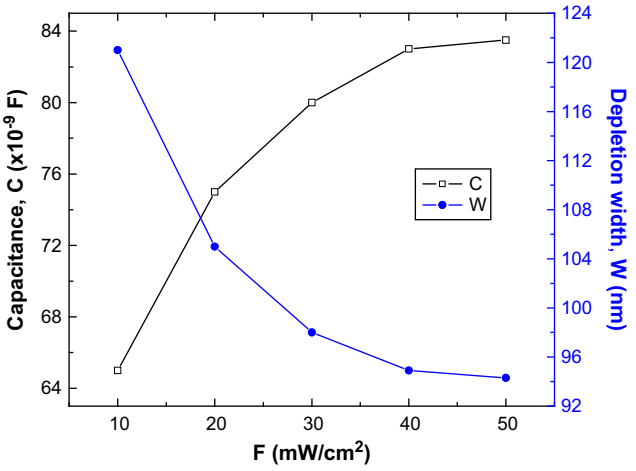

Fig. 5 – The capacitance and the depletion width of Al/n-CdS device under different illumination intensities without any bias voltage.

3.3. *Current–voltage characteristics*

3.3.1. *Dark condition*

Fig. 6 shows the *IV* behavior of the Al/n-CdS device under forward and reverse biasing conditions at different temperatures in the range 303–403 K. The curves are similar to that of a metal/semiconductor (MS) Schottky barrier. Asymmetrical *IV* characteristic under the forward and reverse biasing voltages is observed. This indicates a wide depletion layer width in the structure as obtained above using CV measurements, which favors the thermionic emission of charge carriers through the wide barrier.

The forward current–voltage characteristics as shown in Fig. 7 can be classified into two regions according to the applied voltages. In region II, above ~0.6 V, the forward current deviates from linearity due to the effect of a series resistance and interfacial layer on the Al/n-CdS structure. In region I, below ~0.6 V, the temperature dependence of the forward currents was tentatively analyzed by using a simple Schottky model. In this model, the carrier transport occurs across the barrier by thermionic emission, the drift and diffusion of carriers within the depletion region are less important. Then, the current as a function of applied biasing voltages is given by [37]:

$$I = I_s\left(e^{qV/nkT} - 1\right), \tag{7}$$

where n is the ideality factor, k is the Boltzmann constant, T is the absolute temperature in Kelvin. Value of the saturation current I_s is given by [18]:

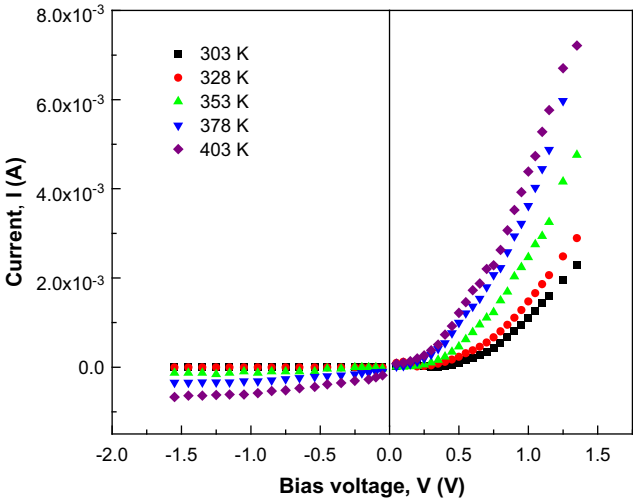

Fig. 6 – The *IV* characteristics of the Al/n-CdS device in forward and reverse biasing condition at different temperatures.

$$I_s = AA^*T^2\, e^{-\Phi_b/kT}, \tag{8}$$

where $A^* = 4\,\pi\, qm^*k^2/h^3$ is the Richardson constant and m^* is the effective mass of the carriers.

In addition, it is clear that the value of n calculated in the downward curvature region is smaller than those obtained from the linear region of the same characteristics as shown in Table 2. This downward curvature region may be attributed to the series resistance and the interface effects. As a result, the barrier height showed a voltage biasing dependence due to the potential change across the interfacial layer thickness as a result of the applied voltage. The series resistance R_s here includes the contact resistance and the thermionic emission is assumed to be the most predominant mechanism [38]. The effect of R_s is significant in the non-linear region of the forward voltage biasing and results in reducing the linear range of the forward *IV* curves [39]. Indeed, the determination

Table 2 – Parameters calculated from the *IV* measurements.

T (K)	First straight line portion (0<V < 0.6 V)			Curvature portion (0.6<V < 1.4 V)	
	$I_o/10^{-7}$ (A)	n	ϕ_b (eV)	R_s (Ω)	n
303	3.25	3.4	0.76	840	2.1
328	15.6	3.3	0.79	513	2.3
353	41.0	3.2	0.82	267	2.1
378	200	3.5	0.84	200	1.2
403	400	4.3	0.86	147.5	1.3

of ϕ_b and n becomes inaccurate. Taking into account the series resistance, Eq. (7) can be written as [40,41]:

$$I = I_s\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right], \tag{9}$$

To overcome the series resistance problems, Eq. (9) can be differentiated as follows:

$$\frac{dV}{d(\ln I)} = IR_s + \frac{nkT}{q}, \tag{10}$$

For the result shown in Fig. 7, the ideality factor n and the series resistance R_s are evaluated by using the slope of $dV/d(\ln I)$ characteristic according to Eq. (10). The plot associated with Eq. (10) is given in Fig. 8, where the linear fit represents the least-square fit of the experimental data. The slope of the line fit gives R_s, while n is determined from Eq. (10) and the y-axis intercept of the line fit. The ideality factor and the series resistance in the range of the investigated temperatures are listed in Table 2. The obtained high series resistance of the Al/n-CdS device may be attributed to the high resistance of the starting CdS and some defects through the preparation or to the interfacial layer created between the metal and CdS [42,43].

We attempted to fit the experimental *IV* curves to Eq. (10) by assuming that the first forward voltage biasing region

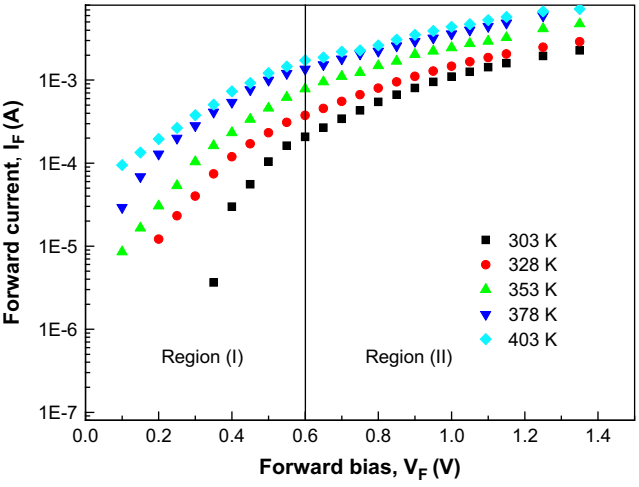

Fig. 7 – The forward current–voltage characteristics at different elevated temperatures for Al/n-CdS thin film.

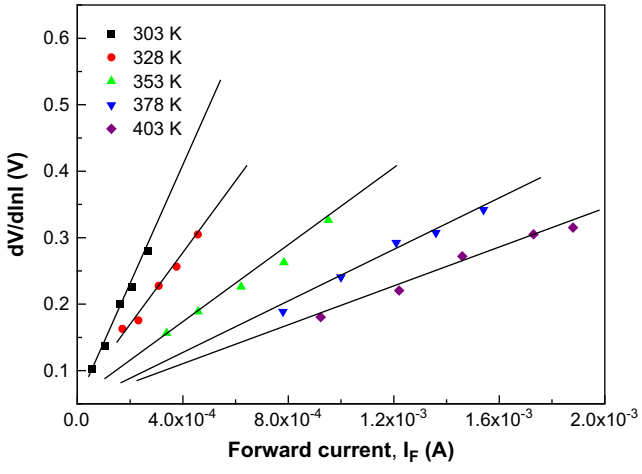

Fig. 8 – $dV/d(\ln I)$ versus I at different temperatures for Al/n-CdS thin film.

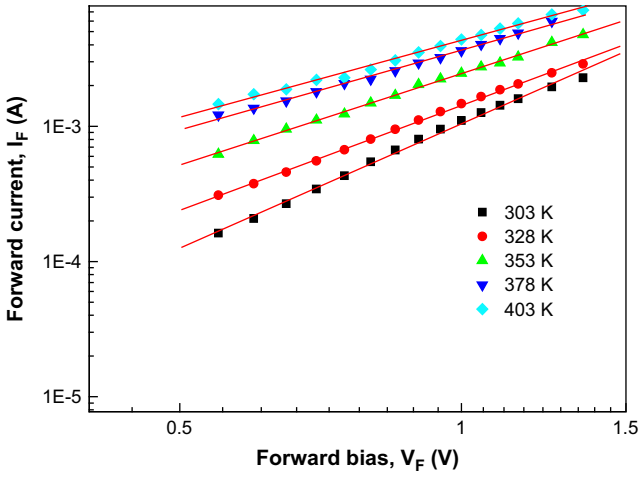

Fig. 9 – The *IV* characteristics of the Al/n-CdS device in log–log scale.

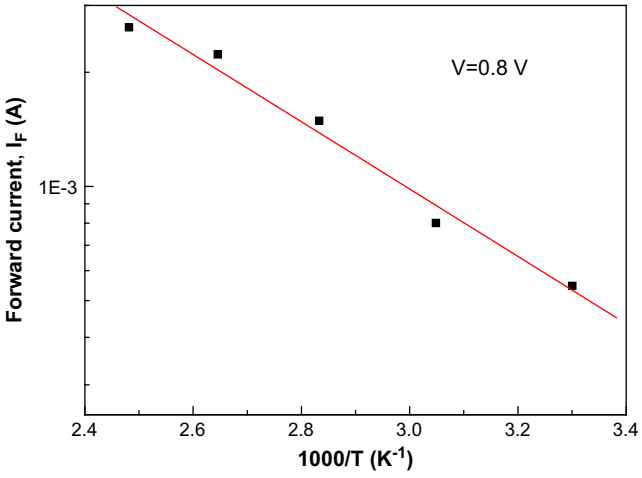

Fig. 10 – The plot of log *I* versus 1/*T* at a certain voltage (0.8 V) in the SCLC region for Al/n-CdS thin film.

consisted of thermionic emission current. The I_s was obtained by extrapolating the linear region of the curve to zero applied voltage and the value of zero-bias barrier height ϕ_b was calculated from the well-known relationship:

$$\phi_b(I-V) = \frac{kT}{q}\ln\frac{AA^*T^2}{I_s}, \tag{11}$$

The value of n was obtained from the slope of the linear region of the *IV* plot at different temperatures. Thus, it is clear from Table 2 that the high value of n may be probably due to potential drop in the interfacial layer and presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers [44].

It can also be seen that the barrier height obtained from *IV* measurements is smaller than those obtained from *CV* measurements. According to Werner and Guttler [45], spatial inhomogeneities at the metal–semiconductor interface of abrupt Schottky contact can also cause such differences in the barrier height determined from *IV* and *CV* measurements. Another possibility may be the transport mechanism in these diodes which is not purely due to thermionic emission. For this structure, the barrier height obtained from *IV* measurement is voltage or electric field sensitive, whereas the barrier height obtained from *CV* is not.

The forward current at the higher voltages, above ~0.6 V, cannot be explained by the theory of the metal/semiconductor interfaces. However, Fowler–Nordheim tunneling emission [46] cannot be evoked by the higher applied bias voltage and the nonlinear dependence of ln *I* vs. $V^{1/2}$ eliminate the possibility of Poole–Frenkel emission [47].

Indeed, space charge limited conduction (SCLC) may be the possible phenomenon that explains the deviation from the ideality of the Al/CdS device. In this case, the *IV* characteristics of the Al/n-CdS device is presented in log–log scale as shown in Fig. 9. At large biasing voltage, the dependencies become close to V^2. The observed transition from thermionic to super-linear dependence of the current with the increase of the biasing voltage usually indicates the onset of a SCLC regime. In the case of existence of a single discrete set of shallow traps in solids, the current is controlled by the space charge. Because of the existence of traps, the current is proportional to V^2. The current in the case of SCLC controlled by a single dominant trap level is given by [48]:

$$I = \frac{9}{8}\varepsilon\mu\left(\frac{N_c}{N_t}\right)\left(\frac{V^2}{d^3}\right)\exp\left(\frac{E_t}{kT}\right), \tag{12}$$

where N_t is the concentration of traps at energy level E_t, below the conduction band edge, μ is the electron mobility and d is the film thickness. Fig. 10 shows the plot of log *I* versus 1/*T* at a certain voltage (0.8 V) in the SCLC region. In this region, the trap energy and the trap concentration can be obtained from the slope and the intercept as 0.17 eV and 1.5×10^{18} cm^{-3}, respectively.

3.3.2. *Illumination condition*

Fig. 11 shows the current–voltage *IV* characteristics Al/n-CdS Schottky junction measured in dark and under different light illuminations. As clearly seen, the device has a photosensitive behavior. Therefore, the photovoltaic parameters of the

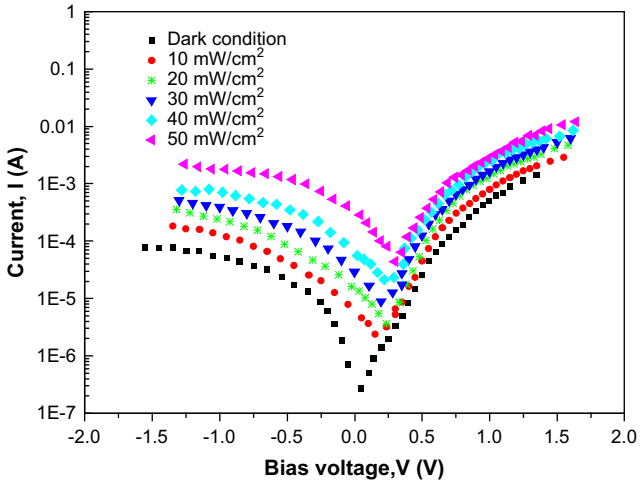

Fig. 11 – *IV* characteristics of Al/CdS device under different illuminations.

Table 3 – Parameters of illuminated IV characteristics.

Illumination (mW/cm^2)	V_{oc} (mV)	I_{sc} (μA)	Photosensitivity (I_{light}/I_{dark})
10	150	3.38	8.7
20	240	3.60	13.2
30	280	6.70	24.5
40	290	12.0	43.95
50	300	44.0	161.1

device (V_{oc} = the open circuit voltage, I_{sc} = short circuit current) are obtained and tabulated in Table 3 as well as the photosensitivity of Al/n-CdS device under different intensity of light illumination. Hence, because of the presence of photovoltaic properties, Al/n-CdS Schottky diodes could be used as a photodiode. If the photovoltaic parameters could be made even better, the diode could be a good candidate for solar cell technology.

Generally, Al/n-CdS Schottky contacts are considered as majority carrier devices and minority carrier injection is disregarded. Though injection of minority carriers (holes for n-type CdS) is usually ignored, one should have to consider the phenomenon especially at high forward bias condition where minority carrier injection and charge storage become significant. In other words, both electrons and holes transportation takes place simultaneously. To do so, barrier height for minority carriers should be low compared to that of majority carriers. Indeed, the barrier height for minorities will decrease as the barrier height for majority carriers increases. Consequently, minority carrier injection occurs inevitably and produces an inversion layer at the interface where the minority carrier amount exceeds the majority carrier amount. Those charges would not contribute to the survey techniques unless certain conditions were fulfilled. One of these occurs in the dark condition: those stored minorities (holes) will diffuse into the neutral region of n-CdS semiconductor under forward bias. In the meantime, additional electrons should enter the neutral region of Schottky diode to preserve the charge neutrality, leading to an increase in bulk conductivity [49,50]. This phenomenon is known as conductivity modulation. On the other hand, once *IV* measurement is performed under light, additional electrons would be supplied over the one created due to illumination. Thus, the reverse bias current exceeds the forward bias current values under light condition.

4. Conclusion

The thermally evaporated CdS films exhibit a stable texture structure along the (002) preferred orientation plane. The capacitance–voltage *CV* and current–voltage *IV* characteristics of the Al/n-CdS device were measured in the temperature range of 303–403 K. The forward current transport can be controlled by the thermionic-field emission and SCLC at low and high voltage biasing, respectively. A discrepancy was found between the values of the barrier height obtained using *CV* measurements and that obtained from the *IV* measurements. The high value of the ideality factor *n* is probably due to the potential drop in the interfacial layer and recombination through the interface states between the Al/n-CdS interfaces. Both *CV* and *IV* measurements showed a good response under the effect of illumination in the range 10–50 mW/cm^2. Photovoltaic measurement indicated that Al/n-CdS Schottky diodes had sensitivity to light, proposing them as a good candidate as a photodiode. Speculation was attempted to resolve this issue.

REFERENCES

[1] Murugan AV, Sonawane RS, Kale BB, Apte SK, Kulkarni AV. Microwave-solvothermal synthesis of nanocrystalline cadmium sulfide. Mater Chem Phys 2001;71:98.

[2] Qingqing W, Gang X, Gaorong H. Solvothermal synthesis andcharacterization of uniform CdS nanowires in high yield. J Solid State Chem 2005;178:2680.

[3] Lee JH. Influence of substrates on the structural and optical properties of chemically deposited CdS films. Thin solid films 2007;515:6089.

[4] Sharupich L, Tugov N. Optoelectonics. Moscow: MIR Publisher; 1987. p. 99.

[5] Nishitani M, Ikeda M, Negami T, Kohoki S, Kohara N, Terauchi M, et al. Fabrication of substrate-type $CuInSe_2$ thin film solar cells. Sol Energy Mater Sol Cells 1994;35:203.

[6] Keitoku S, Ezumi H. Preparation of CdS/CdTe solar cell by laser ablasion. Sol Energy Mater Sol Cells 1994;35:299.

[7] Basol BM. Electrodeposited CdTe and HgCdTe solar cells. Sol Cells 1988;23:69.

[8] Das SK, Morris GC. Preparation and properties of electrodeposited indium tin oxide/SnO2/CdTe and indium tin oxide/SnO_2/CdS/CdTe solar cells. J Appl Phys 1993;73:782.

[9] Zhao Q, Hou L, Huang R, Li S. Surfactant-assisted growth and characterization of CdS nanorods. Inorg Chem Commun 2003;6:1459.

[10] Yang H, Huang C, Li X, Shi R, Zhang K. Luminescent and photocatalytic properties of cadmium sulfide nanoparticles synthesized via microwave irradiation. Mater Chem Phys 2005;90:155.

[11] Lokhande CD. Chemical deposition of CdS thin films from an acidic bath. Mater Chem Phys 1990;26:405.

[12] Rhoderick EH, Williams RH. Metal–semiconductor contacts. Oxford, Buckingham: Clarendon Press, Oxford University Press; 1988. p. 20, 48.

[13] Dimitruk NL, Borkovskaya OYu, Dimitruk IN, Mamykin SV, Horvath ZsJ, Mamontova IB. Morphology and interfacial properties of microrelief metal–semiconductor interface. Appl Surf Sci 2002;190:455.

[14] Saha AR, Chattopadhyay S, Das R, Bose C, Maiti CK. Determination of the interface properties of Ni-silicided strained-Si/SiGe heterostructure Schottky diodes using capacitance–voltage technique. Solid State Electron 2006;50:1269.

[15] Osvald J, Horvath ZsJ. Theoretical study of the temperature dependence of electrical characteristics of Schottky diodes with an inverse near-surface layer. Appl Surf Sci 2004;234:349.

[16] Chand S, Kumar J. Effects of barrier height distribution on the behaviour of a Schottky diode. J Appl Phys 1997;82:5005.

[17] Aydin ME, Yıldırım N, Türüt A. Temperature-dependent behaviour of Ni/4H–nSiC Schottky contacts. J Appl Phys 2007;102:043701.

[18] Sze SM. Physics of semiconductor devices. 2nd ed. New York: John Wiley & Sons; 1981.

[19] Hamida AF, Ouennoughi Z, Sellai A, Weiss R, Ryssel H. Barrier inhomogeneities of tungsten Schottky diodes on 4H–SiC. Semicond Sci Technol 2008;23:045005.
[20] Boyarbay B, Cetin H, Kaya M, Ayyildiz E. Correlation between barrier heights and ideality factors of H-terminated Sn/p-Si(100) Schottky barrier diodes. Microelectron Eng 2008;85:721.
[21] Kiziroglou ME, Zhukov AA, Lia X, Gonzalez DC, De Groot PAJ, Bartlett PN, et al. Analysis of thermionic emission from electrodeposited Ni–Si Schottky barriers. Solid State Commun 2006;140:508.
[22] Forment S, Van Meirhaeghe RL, De Vrieze A, Strubbe K, Gomes WP. A comparative study of electrochemically formed and vacuum-deposited n-GaAs/Au Schottky barriers using ballistic electron emission microscopy (BEEM). Semicond Sci Technol 2001;16:975.
[23] Bao ZL, Kavanagha KL. Epitaxial Bi/GaAs diodes via electrodeposition. J Vac Sci Technol B 2006;24:2138.
[24] Tributsch H. Photovoltaic hydrogen generation. Int J Hydrogen Energy 2008;33:5911.
[25] Yamaguchi K, Udono H. Novel photosensitive materials for hydrogen generation through photovoltaic electricity. Int J Hydrogen Energy 2007;32:2726.
[26] International Centre for Diffraction Data. N 2002 JCDPS PCPDFWIN, v. 2.3; 2002.
[27] Raji P, Sanjeeviraja C, Ramachandran K. Thermal and structural properties of spray pyrolysed CdS thin film. Bull Mater Sci 2005;28:233.
[28] El Deeb AF. Structural and optical characteristics of CdS thin films deposited by infrared pulsed-laser technique. Eur Phys J Appl Phys 2007;38:252.
[29] Gupta RK, Singh RA. Electrical properties of junction between aluminium and poly(aniline)–poly(vinyl chloride) composite. Mater Chem Phys 2004;86:279.
[30] Chen J, Xue K, An J, Tsang SW, Ke N, Xu JB, et al. Photoelectric effect and transport properties of a single CdS nanoribbon. Ultramicroscopy 2005;105:275–80.
[31] Habibe B. Investigation of the effect of CdCl2 processing on vacuum deposited CdS/CdTe thin film solar cells by DLTS. J Phys Chem Solids 2004;65:1817–22.
[32] Montana D, Choudhury A. Frequency dependent electrical properties of nano-CdS/Ag junctions. Eur Phys J B 2005;45:63–8.
[33] Bayhan H, Sertap Kavasoglu A. Study of CdS/Cu(In, Ga)Se_2 heterojunction interface using admittance and impedance spectroscopy. Solar Energy 2006;80:1160–4.
[34] Madelung O. Semiconductors: data handbook. Springer; 2004.
[35] Burrows PE, Shen Z, Bulovic V, McCarty OM, Forrest SR, Cronin JA, Thompson ME. Relationship between electroluminescence and current transport in organic heterojunction light-emitting devices. J Appl Phys 1996;79:7991.
[36] Louro P, Vieira M, Vygrranenko Yu, Fernandes M, Schwarz R, Schubert M. Bias-dependent photocurrent collection in p–i–n a-Si:H/SiC. H heterojunction Sensors Actuators A 2002;97-98:221.
[37] Halliday DP, Gray JW, Adams PN, Monkman AP. Electrical and optical properties of a polymer semiconductor interface. Synthetic Metals 1999;102:877.
[38] Olbrich A, Vancea J, Kreupl F, Hoffmann H. The origin of the integral barrier height in inhomogeneous Au/Co/$GaAs_{67}P_{33}$-Schottky contacts: A ballistic electron emission microscopy study. J Appl Phys 1998;83:358.
[39] Turut A, Saglam M, Efeoglu H, Yalcin N, Yildirim M, Abay B. Interpreting the nonideal reverse bias C-V characteristics and importance of the dependence of Schottky barrier height on applied voltage. Physica B 1995;205:41.
[40] Rhoderick EH, Williams RH. Metal–semiconductor contacts. London: Oxford University Press; 1988.
[41] Quan DT, Hbib H. Temperature dependence of barrier heights of Au/n-type GaAs Schottky diodes. Solid-State Electron 1993;36:339.
[42] Lee JH, Yi JS, Yang KJ, Park JH, Oh RD. Electrical and optical properties of boron doped CdS thin films prepared by chemical bath deposition. Thin Solid Films 2003;431-432:344.
[43] Zhu Y, Ishimaru Y, Takahashi Y, Shimizu M. Correlation between current–voltage and capacitance–voltage characteristics of Schottky barrier diodes. IEEE Trans Electron Devices 1998;9:2032.
[44] Tung RT. Recent advances in Schottky barrier concepts. Mater Sci Eng R Reports 2001;35:1.
[45] Werner JH, Guttler HH. Barrier inhomogeneities at Schottky contacts. J Appl Phys 1991;69:1522.
[46] Aarik J, Bichevin V, Jõgi I, Käämbre H, Laan M, Sammelselg V, et al. Tunnelling in Au–TiO_2–Ag film structures. Central Eur J Phys 2004;2:147.
[47] Zhenyu WU, Yintang Y, Jiayou W. Electrical properties of plasma deposited low-dielectric-constant fluorinated amorphous carbon films. Plasma Sci Technol 2006;8:724.
[48] De Blasi C, Micocci G, Rizzo AR, Tepore A. Electrical properties of indium selenide single crystals. Phys Rev B 1983;27:2429.
[49] Sze SM, Kwok KN. Physics of semiconductor devices. Hoboken, NJ: John Wiley & Sons Inc; 2007.
[50] Kanicki J. Amorphous and microcrystal semiconductor devices II. London: Artech House; 1992.