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GaAsP/InGaP HBTs grown epitaxially on Si substrates: Effect of dislocation density on DC current gain

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Heterojunction bipolar transistors (HBTs) with $GaAs_{0.825}P_{0.175}$ bases and collectors and $In_{0.40}Ga_{0.60}P$ emitters were integrated monolithically onto Si substrates. The HBT structures were grown epitaxially on Si via metalorganic chemical vapor deposition, using SiGe compositionally graded buffers to accommodate the lattice mismatch while maintaining threading dislocation density at an acceptable level ($\sim 3 \times 10^6\,cm^{-2}$). $GaAs_{0.825}P_{0.175}$ is used as an active material instead of GaAs because of its higher bandgap (increased breakdown voltage) and closer lattice constant to Si. Misfit dislocation density in the active device layers, measured by electron-beam-induced current, was reduced by making iterative changes to the epitaxial structure. This optimized process culminated in a $GaAs_{0.825}P_{0.175}/In_{0.40}Ga_{0.60}P$ HBT grown on Si with a DC current gain of 156. By considering the various GaAsP/InGaP HBTs grown on Si substrates alongside several control devices grown on GaAs substrates, a wide range of threading dislocation densities and misfit dislocation densities in the active layers could be correlated with HBT current gain. The effect of threading dislocations on current gain was moderated by the reduction in minority carrier lifetime in the base region, in agreement with existing models for GaAs light-emitting diodes and photovoltaic cells. Current gain was shown to be extremely sensitive to misfit dislocations in the active layers of the HBT—much more sensitive than to threading dislocations. We develop a model for this relationship where increased base current is mediated by Fermi level pinning near misfit dislocations. *Published by AIP Publishing*. https://doi.org/10.1063/1.5001038

I. INTRODUCTION

Monolithic integration of III-V microelectronic devices onto Si substrates—and in particular, Si CMOS circuitry—has many benefits: a broadening of the capabilities of traditional Si CMOS, shorter interconnects and reduced power losses between Si and III-V transistors, reduced chip footprint, and increased flexibility for circuit architecture.[1–4] All of these are obtained while retaining the low cost, large diameters, and good mechanical strength of Si substrates. Direct epitaxial growth of III-Vs such as GaAs on Si substrates is a desirable route for hybrid integration. Through the use of appropriate strain relief schemes such as compositionally graded buffers, GaAs can be grown on Si with defect densities low enough for fabrication of heterojunction bipolar transistors (HBTs), despite the 4% lattice mismatch and break in crystal symmetry.[5]

In this work, we explore the growth and fabrication of $GaAs_{0.825}P_{0.175}$ HBTs on Si substrates. At this composition, GaAsP does not exhibit a significant decrease in electron mobility from GaAs.[6] The substitution of GaAsP for GaAs as an active material offers several advantages. Because GaAsP is closer in the lattice constant to Si, it does not require as thick of a compositionally graded buffer for integration. In addition, the higher bandgap of GaAsP allows for higher breakdown voltage. Lastly, the coefficient of thermal expansion (CTE) of GaAsP is lower than that of GaAs and closer to that of Si, reducing the likelihood of the III-V epi-layer cracking due to CTE mismatch between the films and the substrate.[7]

$GaAs_{0.825}P_{0.175}$ and GaAs HBTs are grown on both GaAs and Si substrates using varying strain relief schemes (including SiGe graded buffers) and other structural parameters, yielding a wide range of defect densities. $In_yGa_{1-y}P$ is used as the emitter material, with y chosen such that the emitter is lattice-matched to the base and collector material. The density of threading dislocations, as well as misfit dislocations (MDs) in the active layers, is measured using electron-beam-induced current (EBIC). We demonstrate a $GaAs_{0.825}P_{0.175}/In_{0.40}Ga_{0.60}P$ HBT on Si with a high current gain. In addition, we model the effect of threading dislocations and misfit dislocations in the active layers on HBT current gain.

II. EXPERIMENTAL

A. Epitaxial growth

$GaAs_xP_{1-x}/In_yGa_{1-y}P$ HBT structures were grown via metalorganic chemical vapor deposition (MOCVD) on both GaAs and Si substrates with several different methods of strain relief. Table I shows a generalized target epitaxial structure for the HBTs. x was either 1 or 0.825, while y was set to 0.49 or 0.40, respectively, such that the GaAsP and InGaP were lattice-matched to each other. Specific structural details of each epitaxial sample are listed in black in Table II. This includes the base dopant type (C or Zn), substrate material (GaAs or Si), strain relaxation scheme, and other

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TABLE I. Target epitaxial structure for the GaAs(P)/InGaP HBTs.

Layer	Material	Thickness (nm)	Growth Temperature (°C)	Polarity	Doping (cm^{-3})
Contact	$GaAs_xP_{1-x}$	100	650	*n*	2×10^{19} Si
Emitter Cap	$In_yGa_{1-y}P$	25	650	*n*	1×10^{18} Si
Emitter	$In_yGa_{1-y}P$	50	650	*n*	6×10^{17} Si
Spacer	$GaAs_xP_{1-x}$	3	650	…	UID
Base	$GaAs_xP_{1-x}$	90	600 or 650	*p*	7×10^{17} C or 5×10^{18} Zn
Collector	$GaAs_xP_{1-x}$	500	650	*n*	1×10^{17} Si
Sub-collector	$GaAs_xP_{1-x}$	100 or 1100	650	*n*	5×10^{18} Si
Buffer Layers	ΔGaAsP, ΔSiGe, or Ge	various	various	*n*	…
Substrate	GaAs or Si	…	…	*n*	…

miscellaneous notes. The measured results from those samples are listed in bold and will be discussed later.

Samples S1–S4 were grown on GaAs substrates. The etch pit density specification of these substrates is $500\,cm^{-2}$. S1 is a fully lattice-matched GaAs/InGaP HBT control sample on a GaAs substrate. S2 is $GaAs_{0.825}P_{0.175}/In_{0.40}Ga_{0.60}P$ HBT grown on a GaAs substrate via a slow tensile GaAsP graded buffer (0.2% strain/μm grade rate). Samples S1 and S2 are characterized more thoroughly in a previous study.[8] Sample S3 is the same as S2, except with a faster grade rate (0.8% strain/μm) in the GaAsP graded buffer. This was done to intentionally increase the defect density for the purpose of understanding the impact of dislocations on device performance. Sample S4 also has an intentionally raised defect density for the same reason. Here, we graded from GaAs to $GaAs_{0.88}P_{0.12}$ with a 0.2% strain/μm grade rate, immediately jumped back to GaAs, and then grew a GaAs HBT structure, well-exceeding the critical thickness. This abrupt introduction of lattice mismatch and growth above the critical thickness introduced nucleation of a high number of dislocations, again to understand their effect on current gain.

Samples S5 through S9 were all grown on Si substrates. S5–S8 are all $GaAs_{0.825}P_{0.175}$ HBTs with SiGe graded buffers accommodating the lattice mismatch between the GaAsP device layers and the Si substrate. These graded buffers were grown using the process described by Sharma *et al.*;[9] however, the final $Si_{1-z}Ge_z$ graded buffer extended to $z = 0.82$, upon which the $GaAs_{0.825}P_{0.175}$ was initiated. With this SiGe graded buffer technique, threading dislocation densities of around $3 \times 10^6\,cm^{-2}$ have been reported, with a buffer thickness of $\sim 10\,\mu m$.[9,10] Sample S5 uses C base doping just like S1–S4. C base doping requires a reduced growth temperature (600 °C instead of 650 °C) to increase C incorporation into the GaAsP.[11] This means that for C-doped GaAsP HBTs where the emitter and collector layers are grown at 650 °C, the emitter, base, and collector layers all have independent compositional calibrations for the MOCVD growth. In addition, growth pauses are required at the base-collector and emitter-base interfaces for temperature ramping and stabilization. For these reasons, S6 uses Zn base doping instead of C. S7 is the same as S6 but with an intentionally mismatched $In_{0.42}Ga_{0.58}P$ emitter layer (compositional shift of 2% In, corresponding to 0.15% strain). Sample S8 is also similar to S6 but includes a thicker subcollector layer (1100 nm increased from 100 nm). This allows for more complete relaxation of the $GaAs_{0.825}P_{0.175}$ subcollector before growth of the active device layers.

Sample S9 is a GaAs/InGaP HBT grown on a Si substrate via a Ge buffer grown using a two-step approach. First, a thin conformal layer of Ge is deposited at low growth temperature. Then, a thicker Ge layer ($\sim 1\,\mu m$) is grown at a higher temperature. Finally, the sample is cyclically annealed to reduce threading dislocation density via dislocation-dislocation annihilation.[12,13] Further details of the Ge buffer growth can be found in the study by Lee *et al.*[14] The two-step Ge growth technique requires a

TABLE II. List of samples for studying the effect of various structural parameters on defect density and HBT performance. Measured threading dislocation density (ρ_{TD}), misfit dislocation density (ρ_{MD}), and current gain (β) for 60 μm diameter HBTs are shown in bold.

Sample #	$GaAs_xP_{1-x}$ Comp. (*x*)	Base dopant	Substrate	Strain relaxation scheme	Notes	ρ_{TD} (cm^{-2})	ρ_{MD} (cm^{-1})	β at $I_C = 2 \times 10^{-4}$ A	β at $I_C = 1 \times 10^{-1}$ A
S1	1	C	GaAs	n/a		**<6000**	**<1**	**70**	**263**
S2	0.825	C	GaAs	GaAsP GB		**1.5×10^5**	**52**	**50**	…
S3	0.825	C	GaAs	GaAsP GB, fast grade rate	Defect density purposefully increased from S2	**9.7×10^5**	**119**	**41**	…
S4	1	C	GaAs	GaAsP GB then jump back to GaAs	Defect density purposefully increased from S1	**1.7×10^6**	**335**	**23**	…
S5	0.825	C	Si	SiGe GB		**2.7×10^6**	**1880**	**1.6**	…
S6	0.825	Zn	Si	SiGe GB		**1.6×10^6**	**594**	**16**	…
S7	0.825	Zn	Si	SiGe GB	Intentionally mismatched InGaP emitter	**3.4×10^6**	**897**	**9.2**	…
S8	0.825	Zn	Si	SiGe GB	Thick subcollector layer (1100 nm)	**3.7×10^6**	**<1**	…	**158**
S9	1	C	Si	two-step Ge		**2.2×10^7**	**<1**	…	**60**

substantially thinner buffer layer than the SiGe graded buffer technique (~1 μm); however, it yields a higher dislocation density (~1–2 $\times 10^7$ cm^{-2}).

The HBT structures were all grown in a Thomas Swan/Aixtron cold-walled $6 \times 2''$ metalorganic chemical vapor deposition (MOCVD) reactor with a close-coupled showerhead configuration. Trimethylgallium (TMGa), trimethylindium (TMIn), dimethylzinc (DMZn), AsH_3, PH_3, Si_2H_6, and $CBrCl_3$ were used as precursors. The total reactor pressure for all samples was 100 Torr, and N_2 was used as a carrier gas. The susceptor rotation speed was 100 rpm. Growth rates were approximately 0.55 nm/s for GaAs and GaAsP and 0.35 nm/s for InGaP. A 5 s purge step, holding group V precursor flow rates constant from the previous layer, was implemented while switching from GaAs(P) to InGaP and from InGaP to GaAs(P). Device layers were then grown at 650 °C, except for the C-doped GaAsP base layers, which were grown at 600 °C. All temperature ramps were executed with a group V overpressure (mixed AsH_3 and PH_3) but with no group III precursor flow.

B. Film characterization and HBT fabrication

Lattice constant of the films—and by Vegard's law, their composition—were confirmed using high-resolution x-ray diffraction (XRD) using a procedure described previously.[11] Film thicknesses and morphologies were verified using cross-sectional transmission electron microscopy (TEM) with an accelerating voltage of 200 kV. Electron-beam-induced current (EBIC) images were taken for all the samples. For the EBIC measurements, large mesa structures (160×120 μm) were patterned and ohmic contacts deposited. An accelerating voltage of 20 kV and a beam current of 0.34 nA were used. This permitted the measurement of threading and misfit dislocations in a wide range of densities. The dopant concentration of a representative sample was verified using dynamic secondary ion mass spectrometry (SIMS), performed by the Evans Analytical Group.

HBTs were fabricated in an annular geometry from the epitaxial structures using standard lithography and wet-etching techniques, as described in a previous report.[8] DC measurements were taken at 300 K from 60 μm diameter devices using a Keysight B1500 semiconductor parameter analyzer.

III. RESULTS

A. Epitaxial film characterization

EBIC was used to measure the threading dislocation density (ρ_{TD}) and misfit dislocation density in the active region (ρ_{MD}) for each sample. Representative EBIC images from S1, S6, and S9 are shown in Figs. 1(a), 1(b), and 1(c), respectively. In S1, there are no defects visible. In S6, there are both threading dislocations (black dots) and misfit dislocations (black lines) visible. While all of the lattice-mismatched samples have misfit dislocations in the buffer layers in order to accommodate their relaxation, the misfit dislocations detected by EBIC are in the active regions and therefore have a negative impact on device performance. The grey vertical features in S6 are due to surface roughness known as "cross-hatch."

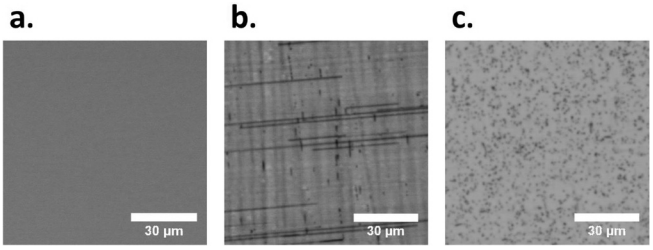

FIG. 1. EBIC images of GaAs(P) HBTs grown on (a, S1) lattice-matched GaAs substrate, (b, S6) Si substrate via unoptimized SiGe graded buffer, and (c, S9) Si substrate via 2-step Ge buffer. Threading dislocations are visible in (b) and (c) and misfit dislocations are visible in (b).

This is caused by growth-rate variations induced by strain fields surrounding underlying misfit dislocations.[15] In S9, the black dots are threading dislocations. To calculate ρ_{TD}, the total number of threading dislocations in an image is divided by the area. To calculate ρ_{MD}, the total misfit dislocation length is divided by the image area. ρ_{TD} and ρ_{MD} are listed for all of the samples in Table II. The 95% confidence window of ρ_{TD} is estimated by Poisson statistics to be approximately ±20%.

XTEM of Sample S5 was used to measure film morphology, observe any dislocations in the film, and verify layer thickness (see Fig. 2). While the thicknesses are on target, there is a misfit dislocation visible at the emitter-base interface. This is consistent with the high ρ_{MD} measured with EBIC for this sample.

B. DC characterization

Gummel characteristics were measured for all nine samples on devices with an emitter mesa diameter of 60 μm. Gummel plots for Samples S1, S8, and S9 are plotted in Fig. 3. Sample S1, a GaAs HBT on a GaAs substrate, serves as a control device with no measured dislocations. Sample S8 is the GaAsP sample on Si with the lowest misfit dislocation density. Sample S9 is the GaAs sample on Si with the lowest defect density and was also grown without the use of graded buffers.

The series resistance for Sample S9 is much higher than for S1 and S8. This is why when compared to S1, V_{BE} must be higher to yield the same I_C for $I_C \gtrsim 10^{-7}$ A. The series resistance for S9 is higher because the Ge buffer is undoped, so the collector current is forced to travel laterally tens of microns through the relatively thin GaAs subcollector. The

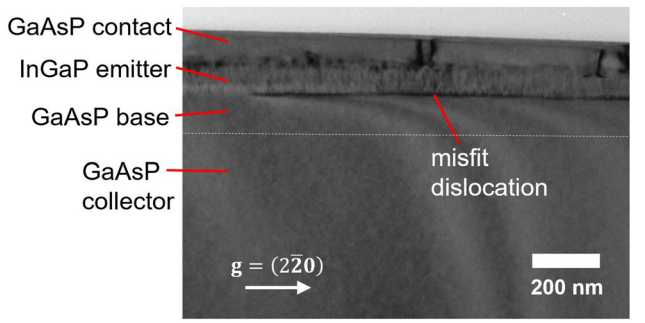

FIG. 2. XTEM image of Sample S5 [(110) orientation, bright field], showing a misfit dislocation at the emitter-base interface.

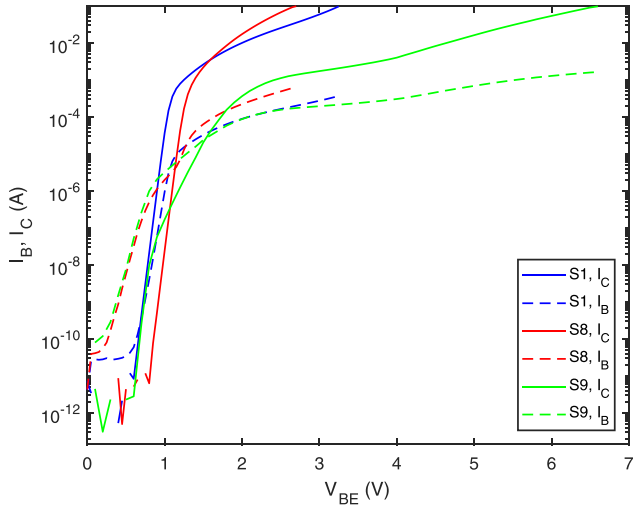

FIG. 3. Gummel plots (I_C and I_B vs. V_{BE} at $V_{BC} = 0$ V) for Samples S1, S8, and S9. S9 exhibits a high series resistance.

GaAs subcollector could not be made thicker because if the III-V layers are too thick, the film cracks due to CTE mismatch between the films and the substrate. The high series resistance exhibited in this case is not expected to impact performance in real applications because the contacts would be made much nearer to the device.

At low V_{BE} of less than 1–1.5 V, a significant leakage component is observed in I_B for the samples on Si substrates. This reduces the DC current gain ($\beta = I_C/I_B$) in this voltage range. It is unlikely that this leakage is from generation currents from trap states associated with threading dislocations near the emitter-base interface, as these currents have been shown to be many orders of magnitude lower than what is observed here.[16] It is therefore unclear what the mechanism of this leakage current is. However, because it is only present at lower V_{BE}, β can still be compared between devices at high V_{BE} without its effect.

The differences in series resistance between samples make direct comparison of device performance (i.e., β) difficult from Fig. 3. To make this comparison easier, we plot β as a function of I_C in Fig. 4. In this figure, we have a better sense of the relative performance of S1, S8, and S9. The

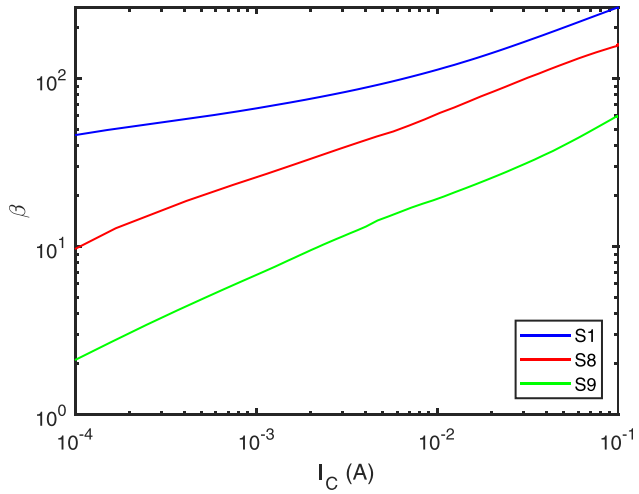

FIG. 4. Current gain vs. collector current for Samples S1, S8, and S9.

maximum β for S8 is 158, which is the highest current gain that we achieved for a GaAs(P) HBT grown on Si. The maximum β for S9 is 60, which is the highest that we achieved for a III-V device grown on a Si substrate without the use of a graded buffer.

In order to quantitatively compare current gain for S1–S9, we list β at singular values of I_C in Table II. These values will be used in Sec. IV for modelling the current gain as a function of defect density.

IV. DISCUSSION

A. Effect of threading dislocations on current gain

Threading dislocations are necessarily generated when lattice-mismatched layers are allowed to plastically relax, because dislocations must terminate at a free surface. Therefore, it is important to understand the effect of threading dislocations on device performance. Here, we will focus on how threading dislocation density (ρ_{TD}) affects the DC current gain (β), as this is a critical device parameter that is highly sensitive to enhanced minority carrier recombination.

The effect of misfit dislocations in the active device layers will be discussed later in Sec. IV B. However, it is important for now to note that misfit dislocations cause a comparatively larger reduction in β than threading dislocations. Therefore, in order to isolate the effect of ρ_{TD} on β, in this section we will consider only devices without any misfit dislocations detected in the active region. Of the samples listed in Table II, only samples S1, S8, and S9 will be considered here because they have negligible misfit dislocation densities (ρ_{MD}) as determined by EBIC measurements.

The effect of threading dislocations on GaAs- or GaAsP-based HBT performance can be estimated by a model for minority carrier lifetime vs. threading dislocation density developed by Roedel *et al.* for describing the efficiency of GaAs/AlGaAs LEDs grown on lattice-mismatched substrates.[17] This model was further developed by Yamaguchi *et al.* for describing the efficiency and open-circuit voltage of GaAs photovoltaic cells in the presence of threading dislocations.[18,19] In Fig. 5, Yamaguchi's model is plotted alongside efficiency data for Roedel's LEDs as well as for GaAs photovoltaic (PV) cells over a wide range of ρ_{TD}. The model and data are in reasonably good agreement, varying by a factor of 2–3 in ρ_{TD}. We can use this model as a basis for describing the effect of threading dislocations on HBT current gain.

The model starts by calculating the average distance (L_{TD}) that a given electron must diffuse in the p-type base to reach a threading dislocation at a given ρ_{TD}

$$L_{TD} = \frac{2}{\pi^{1.5}\rho_{TD}^{0.5}}. \quad (1)$$

The details of the derivation of this equation can be found in Sec. II A of Yamaguchi's paper.[18] From this, we can calculate the overall electron diffusion length in the base region (L)

$$L = \left(\frac{1}{L_0^2} + \frac{1}{L_{TD}^2}\right)^{-0.5}, \quad (2)$$

where L_0 is the diffusion length due to all other recombination mechanisms. Major contributors to L_0 in our HBTs

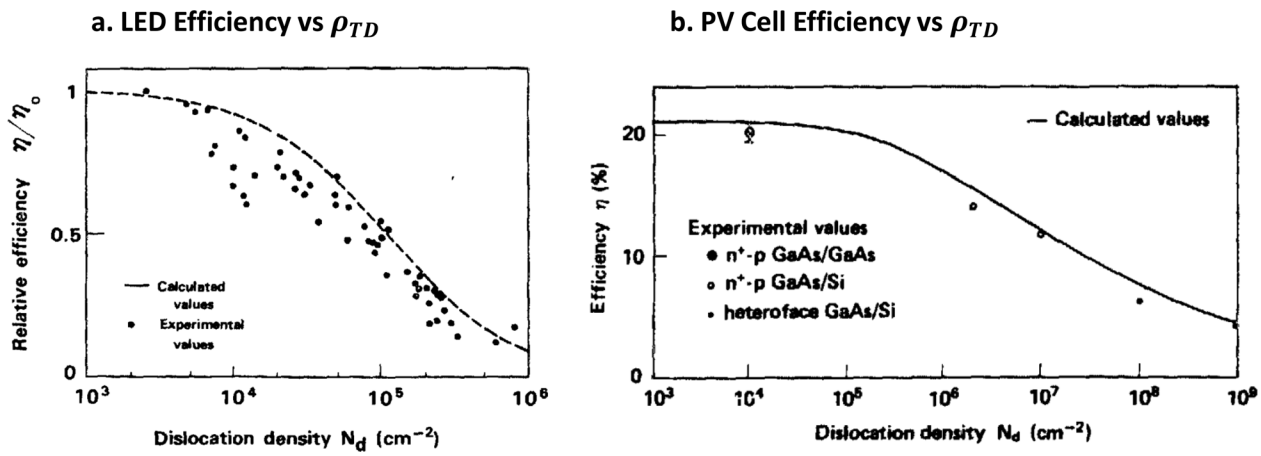

FIG. 5. Models for the effect of threading dislocation density on (a) GaAs/AlGaAs LED efficiency and (b) GaAs PV cell efficiency. Reproduced with permission from J. Appl. Phys. **59**, 1751 (1986).[19] Copyright 1986 AIP Publishing LLC.

include recombination in the quasi-neutral base region due to the heavy p-type doping, recombination at the emitter-base junction, and recombination at the device sidewalls.[8] From here, we calculate the minority carrier lifetime in the base in the presence of threading dislocations ($\tau_{n,TD}$)

$$\tau_{n,TD} = \frac{L^2}{D_{nB}} = \frac{1}{D_{nB}}\left(\frac{1}{L_0^2} + \frac{\pi^3 \rho_{TD}}{4}\right)^{-1}, \tag{3}$$

where D_{nB} is the diffusivity of electrons in the base region.

Now, to calculate the current gain in the presence of threading dislocations (β_{TD}), we find the ratio of electrons which diffuse all the way across the base to those which recombine in the base. This is simply equal to $\tau_{n,TD}$ divided by the base transit time (τ_B)[20]

$$\beta_{TD} = \frac{\tau_{n,TD}}{\tau_B}, \tag{4}$$

τ_B is the average time for an electron to transit the base region, and is a function of the quasi-neutral base width (x_B) and of $D_{n,B}$[20]

$$\tau_B = \frac{x_B^2}{2D_{nB}}. \tag{5}$$

By combining Eqs. (3)–(5), we can now find β_{TD} as a function of ρ_{TD} with only one unknown parameter (L_0). For our purposes, we will set L_0 such that the current gain in the case of no threading dislocations is predicted correctly. It should be noted that β_{TD} has no dependence on $D_{n,B}$.

β vs. ρ_{TD} data for Samples S1, S8, and S9 are plotted in Fig. 6, along with the model discussed above. The model slightly overpredicts β—the ρ_{TD} for a given value β is shifted by about a factor of two. This error is similar in direction and magnitude to the errors exhibited in the model from Yamaguchi and Amano.[18] Error in the measurement of ρ_{TD}, which is estimated to be around $\pm 20\%$, is not enough to explain this shift. One source of error could be the estimation of the base thickness x_B (in this case assumed to be 100 nm). A larger base thickness (caused by diffusion of the base dopant into the emitter or collector) would cause a higher τ_B and therefore a lower β. Another source of error is our approximation that recombination only occurs at the dislocation core and not at any distance away from the dislocation. A final source of error is the estimation of the average distance between dislocations, which, following Yamaguchi *et al.*, we set as $2/(\pi\rho_{TD})^{0.5}$.[19] However, Roedel *et al.* simply use $1/\rho_{TD}^{0.5}$ for this distance,[17] which yields a β vs. ρ_{TD} model in closer alignment to our data.

B. Effect of misfit dislocations on current gain

Misfit dislocations in the active region of an HBT have a particularly detrimental effect on performance. While a threading dislocation pierces through the active layers near-perpendicularly on its way to the upper surface, a misfit dislocation can run along the active region for considerable distances. Therefore, for the same overall dislocation density (total dislocation length divided by volume), misfit dislocations have the potential to cause much greater carrier recombination in the base region. In any relaxed lattice-mismatched epitaxial structure, misfit dislocations are necessary to accommodate the plastic deformation of the mismatched layers. However, in general, it is desirable to ensure that these misfits are located sufficiently below (or above) the active layers such that they do not interfere with device performance.

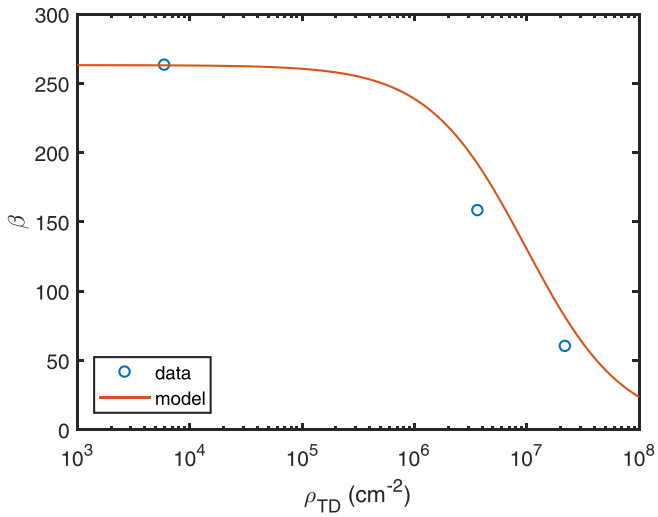

FIG. 6. Effect of threading dislocation density on GaAs(P)/InGaP HBT current gain ($I_C = 8 \times 10^{-1}$ A).

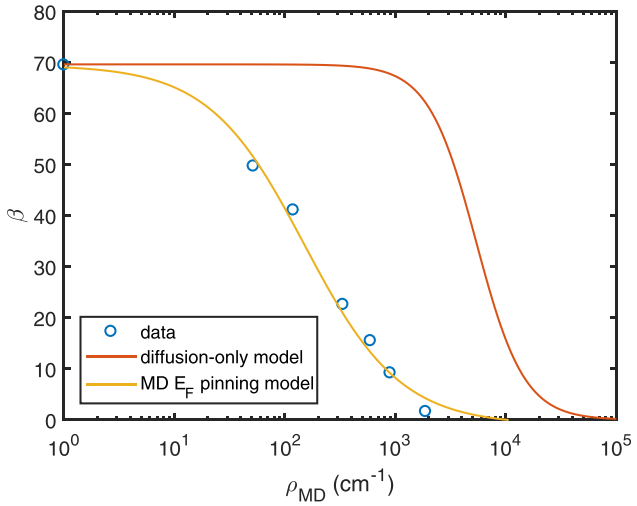

FIG. 7. Effect of misfit dislocation density on GaAs(P)/InGaP HBT current gain ($I_C = 2 \times 10^{-4}$ A).

In all but one of the GaAsP HBTs grown on Si substrates for this work, misfit dislocations were observed at one or both of the base-collector and emitter-base interfaces [(e.g., Fig. 1(b)]. Misfit dislocation density (ρ_{MD}) for these samples is listed in Table II. We can see that the changes made in S6 and S8 (Zn base doping and a thick subcollector layer, respectively) caused improvements in ρ_{MD}, while the intentionally mismatched emitter layer of S7 caused a worsening of ρ_{MD}.

By considering samples S1–S7, we have a wide range of ρ_{MD} measured by EBIC. In addition, for these samples, the ρ_{TD} is low enough that it should not significantly affect β according to the model developed in Sec. IV A. In other words, threading dislocations do not make a considerable contribution to minority carrier recombination in the base compared with recombination caused by misfit dislocations in samples S1-S7. In order to compare β from HBTs with different GaAsP compositions without seeing the effects of differing bandgaps, β is taken with constant I_C rather than constant V_{BE}.[8] In Fig. 7, β is plotted at $I_C = 2 \times 10^{-4}$ A as a function of ρ_{MD}. We pick this current because it is in a regime where both I_C and I_B vary exponentially with V_{BE} for all of the devices. The first data point, with $\beta = 70$, was from Sample S1, which had no observable misfit dislocations. This was assigned an upper bound ρ_{MD} of 1 cm^{-1} based on the area of the sample measured by EBIC. As expected, β decreases monotonically with increasing ρ_{MD}.

The model for the effect of threading dislocations on minority carrier lifetime described in Sec. IV A can be extended to apply to misfit dislocations as well. We will refer to this model as the diffusion-only model, because the additional component of I_B due to the presence of misfit dislocations is controlled by diffusion of electrons in the quasi-neutral base region. A schematic of this process is shown in Fig. 8(a). Electrons are injected from the emitter into the quasi-neutral base uniformly across the emitter-base junction, unaffected by the presence of dislocations. Similar to the model for β_{TD}, these electrons can then diffuse either to the collector, where they are captured and contribute to I_C, or to a misfit dislocation, where they recombine and contribute to I_B. The ratio of electrons which make it across the base to those which recombine is therefore equal to the minority carrier lifetime in the presence of misfit dislocations ($\tau_{n,MD}$) divided by the base transit time (τ_B). This ratio can be defined as the current gain in the presence of misfit dislocations (β_{MD})

$$\beta_{MD} = \frac{\tau_{n,MD}}{\tau_B}, \tag{6}$$

where τ_B is the same as in the model for β_{TD} and is defined in Eq. (5).

We can estimate $\tau_{n,MD}$ based on Eq. (3) for $\tau_{n,TD}$. In the case of threading dislocations, the average distance between two dislocations is $2/(\pi\rho_{TD})^{0.5}$.[18] However, for the case of misfit dislocations, the average distance between two misfits

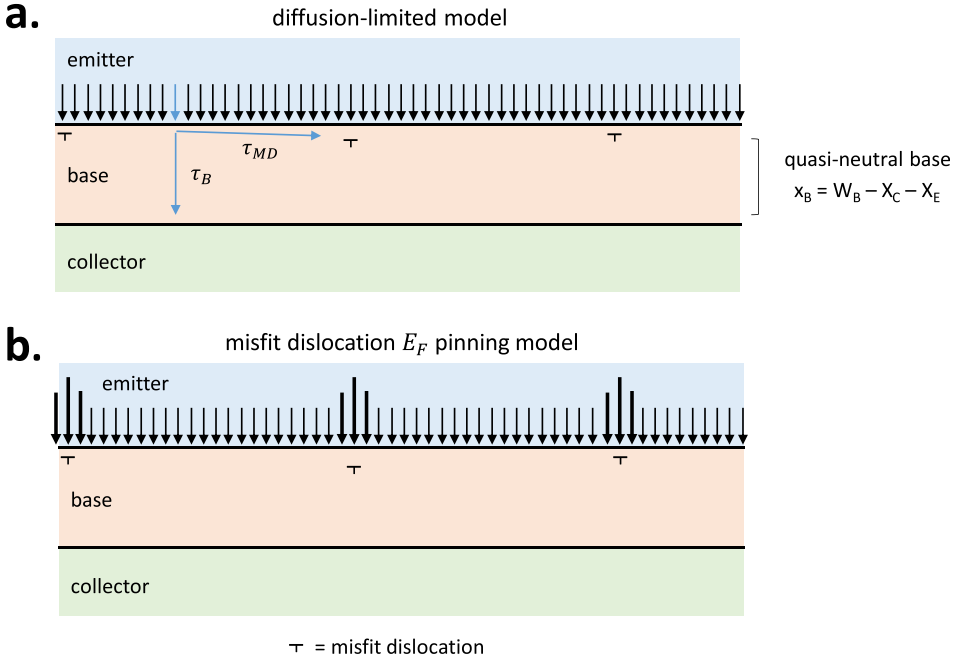

FIG. 8. Schematics of two models for describing the effect of misfit dislocations on current gain: (a) diffusion-limited model and (b) misfit dislocation E_F pinning model.

is simply $1/\rho_{MD}$. Therefore, by substitution into Eq. (3), we derive an equation for $\tau_{n,MD}$ of

$$\tau_{n,MD} = \frac{1}{D_{nB}}\left(\frac{1}{L_0^2} + \pi^2\rho_{MD}^2\right)^{-1}. \quad (7)$$

Just as in Sec. IV A, we will set L_0 such that β for the HBT with no misfit dislocations is predicted correctly.

β_{MD} as predicted by the diffusion-only model is plotted in orange in Fig. 7. This model fails in multiple respects. First, it overestimates the misfit dislocation density at which the current gain begins to fall by two orders of magnitude. Some of this error may be attributed to an error in the average distance an electron must travel to encounter a misfit dislocation and recombine. However, this distance should be on the order of $1/\rho_{MD}$, so the model should not be off by more than one order of magnitude.

A second failure of the diffusion-only model is that it predicts the wrong slope for β vs. ρ_{MD} in the section where β is rapidly falling. This stems from the fact that in this model, for higher values of ρ_{MD}, β is proportional to ρ_{MD}^{-2}. However, the data follow more closely with ρ_{MD}^{-1}. This suggests that the diffusion-only mechanism that governs the effect of threading dislocations on β does not also apply to misfit dislocations in the active region of the HBT.

In place of the diffusion-only model, we hypothesize another model, which we call the misfit dislocation (MD) E_F pinning model. Instead of being injected uniformly across the emitter-base interface, electrons are injected preferentially near the locations of misfit dislocations. Dislocations have mid-gap energy states that cause local pinning of the Fermi level (E_F).[21] This causes band bending surrounding the dislocations, which in turn causes turn-on of the emitter-base junction at lower V_{BE} in these areas compared to areas far from dislocations. This effect is illustrated qualitatively in Fig. 9. The band bending surrounding the dislocation in Fig. 9(b) causes a reduction in the energy barrier for electrons moving from the emitter to the base (blue arrows). It also causes the quasi-neutral base thickness to decrease (orange arrows). Both of these effects can increase the rate of electron injection from the emitter into the base.[8] The extra electron current caused by this effect is injected in close proximity to the misfit dislocations, which act as recombination centers, and therefore largely recombines with majority holes in the base. This process is illustrated in Fig. 8(b).

In order to describe this phenomenon, we define $I_{B,MD}$ as the extra base current that is caused by E_F pinning near misfit dislocations. $I_{B,MD}$ is proportional to the total length of misfit dislocations in the area of the emitter-base junction and to the collector current

$$I_{B,MD} = CI_{C,0}\rho_{MD}. \quad (8)$$

The arbitrary proportionality constant C accounts for the area of the emitter-base junction and the amount of extra current per unit length of misfit dislocation. $I_{C,0}$ is the collector current in the absence of misfit dislocations. From this, we can calculate the overall β with misfit dislocations

$$\beta_{MD} = \frac{I_C}{I_B} = \frac{I_{C,0} - I_{B,MD}}{I_{B,0} + I_{B,MD}}, \quad (9)$$

where $I_{B,0}$ is the base current in the absence of misfit dislocations. By dividing all terms in the numerator and denominator of Eq. (9) by $I_{C,0}$, it can be written as a function of β_0 (current gain without misfit dislocations)

$$\beta_{MD} = (1 - C\rho_{MD})\left(\frac{1}{\beta_0} + C\rho_{MD}\right)^{-1}. \quad (10)$$

In Fig. 7, β_{MD} according to this model is plotted in yellow. β_0 is 70, taken from sample S1 which has no observable misfit dislocations. Adjusting C simply translates the curve horizontally without any other distortion. It is set such that the curve overlays the data. The model is approximately proportional to ρ_{MD}^{-1} for higher values of ρ_{MD} and therefore fits the data well. We therefore believe that the MD E_F pinning mechanism is the main factor determining the reduction in β due to misfit dislocations into the active layers.

It is interesting that the E_F pinning model applies to misfit dislocations while the diffusion-only model applies to threads. The increase in I_B associated with increased dislocation density in the diffusion-only model is inversely proportional to the spacing between dislocations, whether they are misfits or threads. However, the increase in I_B associated with the E_F pinning model is proportional to the total area of the emitter-base interface that is intersected by dislocations.

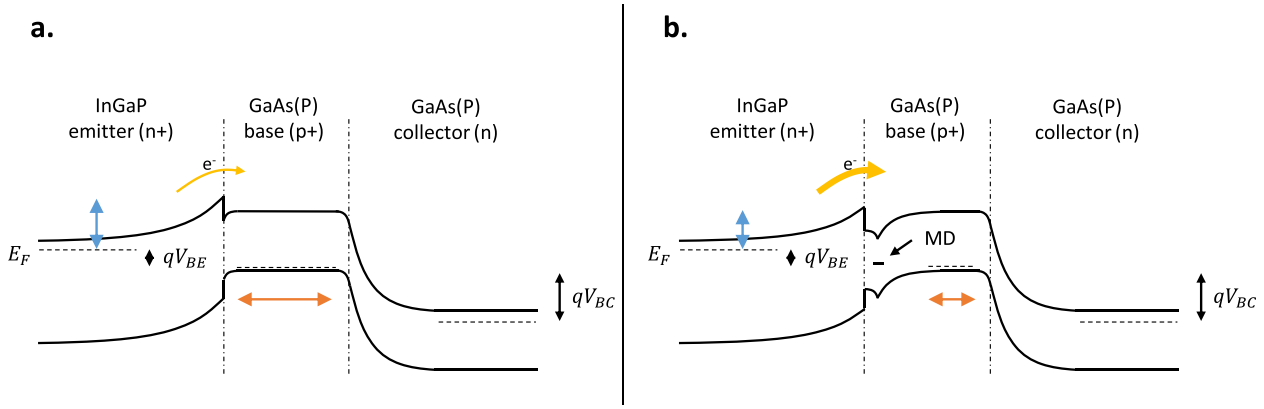

FIG. 9. Qualitative schematic of an HBT band diagram (a) from a normal area and (b) near a misfit dislocation. The band bending near the misfit dislocation in (b) causes a reduced energy barrier for electrons flowing from the emitter to the base (blue) and a thinner quasi-neutral base region (orange), resulting in an increase in injected electrons.

Because the intersection of misfit dislocations with this interface is one-dimensional while the intersection of threading dislocations with this interface is zero-dimensional, misfit dislocations have a much larger contribution given the same average spacing. This is illustrated in Fig. 10. This causes the E_F pinning mechanism to be significantly weaker for threading dislocations than for misfit dislocations.

By combining the applicable models for the effects of threading and misfit dislocations on current gain and normalizing by β_0, we can create a contour map showing the relative effects of threads and misfits in a sample containing both (Fig. 11). It is important to note that this map is only valid for HBTs of this design, with the same base width and material parameters governing carrier recombination by other mechanisms.

Clearly, misfit dislocations in the active region have a pronounced effect on current gain. Even with an average lateral spacing as large as 1 mm, misfit dislocations would result in a 20% drop in β. This spacing of misfit dislocation is far too large to be observed via TEM. EBIC measurements, which have a very large sampling area, are required for observing misfit dislocations at this density.

The following equation describes the average spacing between misfit dislocations (S) below a relaxed lattice-mismatched film:

$$S = \frac{b_{eff}}{\delta}, \tag{11}$$

where b_{eff} is the effective Burger's vector (in-plane component of $\boldsymbol{b}$ in the direction of spacing S) and δ is the plastic strain.[22] A 1 mm average misfit spacing corresponds to an extremely small plastic strain ($\delta = 1.4 \times 10^{-7}$). This amount of mismatch is not measureable using XRD. Therefore, the base and emitter films must not be allowed to relax via plastic deformation at all during growth if β is to be maintained.

V. CONCLUSIONS

This paper demonstrates good DC performance of $GaAs_{0.825}P_{0.175}/In_{0.40}Ga_{0.60}P$ HBTs grown on Si substrates. Current gain as high as 158 was measured for devices using a SiGe compositionally graded buffer to relieve the strain between the film and the substrate. The GaAsP/ΔSiGe/Si platform offers a threading dislocation density of $\sim 3 \times 10^6\,cm^{-2}$, which is shown to be suitable for HBT fabrication. The use of GaAsP offers benefits over GaAs, including higher bandgap (for increased breakdown voltage) and reduced lattice mismatch with Si, which allows for a thinner SiGe graded buffer. Misfit dislocations in the active region (i.e., at the emitter-base or base-collector interfaces) presented an issue for some of the GaAsP devices on Si substrates. However, they were eliminated by moving from C to Zn base doping, ensuring good lattice-matching between the InGaP emitter and underlying GaAsP layers, and using a thick ($>1\,\mu m$) GaAsP subcollector layer grown using the same growth conditions as the GaAsP collector and base.

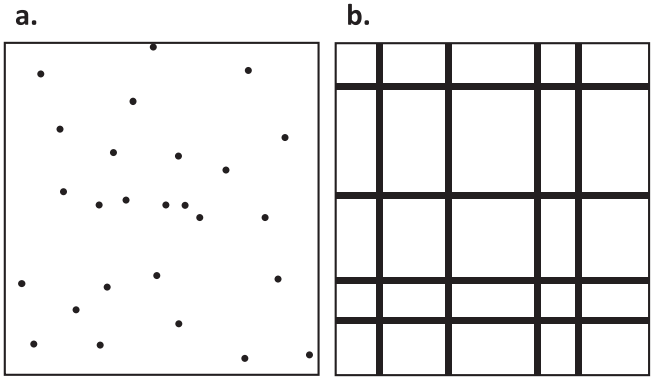

FIG. 10. Intersection of (a) threading dislocations and (b) misfit dislocations with the emitter-base interface. For densities with a similar average spacing, misfit dislocations intersect a much larger effective area.

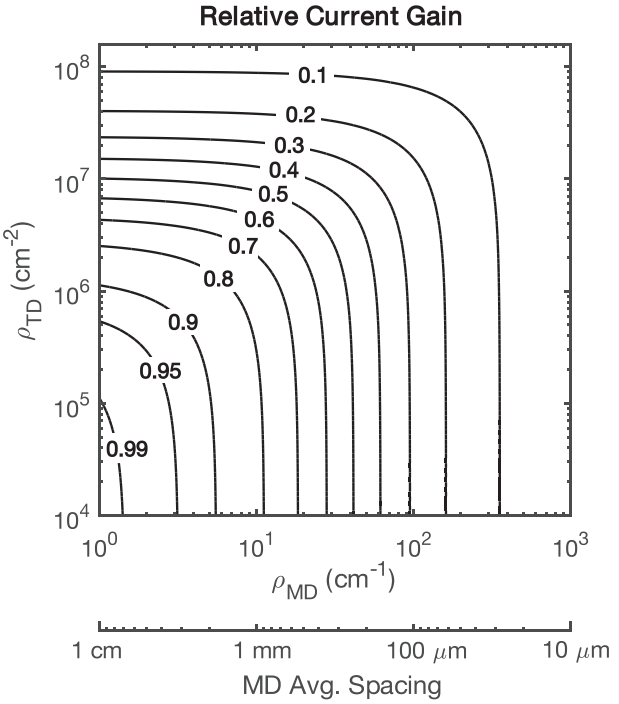

FIG. 11. Map of relative current gain (β/β_0) as a function of misfit dislocation density and threading dislocation density.

Understanding the exact nature of defects in III-V HBTs on Si substrates and their effect on device performance is necessary to engineer successful devices. GaAs(P)/InGaP HBTs were measured with a wide range of threading dislocation densities and misfit dislocation densities in the active region. The effect of these defect densities on current gain was modeled after appropriate physical mechanisms. At high threading dislocation densities, current gain was limited by reduced minority carrier lifetime as compared with the base transit time for electrons. The reduction in lifetime due to threading dislocations was consistent with previous studies of GaAs LEDs and photovoltaic cells.[17,19] However, at high misfit dislocation densities, we propose that current gain reduction is caused by an increase in injected electrons in close vicinity to the misfit dislocations due to Fermi level pinning. This causes current gain to be highly sensitive to misfit dislocations in the active region, even at high average lateral spacing in excess of 1 mm. Therefore, the importance of precise control of lattice mismatch at or near the active device layers, and of microscopy techniques such as EBIC that are sensitive to low defect densities, is underscored.

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