Coulomb blockade in a Si channel gated by an Al single-electron transistor

L. Sun,[a)] K. R. Brown,[b)] and B. E. Kane
Laboratory for Physical Sciences, 8050 Greenmead Drive, College Park, Maryland 20740, USA

We incorporate an Al–AlO$_x$–Al single-electron transistor as the gate of a narrow ($\sim$100 nm) metal-oxide-semiconductor field-effect transistor (MOSFET). Near the MOSFET channel conductance threshold, we observe oscillations in the conductance associated with Coulomb blockade in the channel, revealing the formation of a Si single-electron transistor. Abrupt steps present in sweeps of the Al transistor conductance versus gate voltage are correlated with single-electron charging events in the Si transistor, and vice versa. Analysis of these correlations using a simple electrostatic model demonstrates that the two single-electron transistor islands are closely aligned, with an interisland capacitance approximately equal to $1/3$ of the total capacitance of the Si transistor island, indicating that the Si transistor is strongly coupled to the Al transistor. © 2007 American Institute of Physics. [DOI: 10.1063/1.2793712]

Single-electron transistors (SETs) are sensitive electrometers, able to detect a small fraction of an electron charge, with a sensitivity around 10^{-6} $e/\sqrt{\text{Hz}}$.[1] They have been extensively utilized for metrology[2] and may have applications in quantum information processing.[3,4] While metal SETs are more common, Si SETs are desirable because of their better stability[5] and their ease of incorporation into Si quantum computation architectures.[6]

In this letter, we present results from a Si SET self-aligned and vertically coupled to a metal SET. An Al–AlO$_x$–Al SET is incorporated as the gate of a narrow ($\sim$100 nm) n-channel metal-oxide-semiconductor field-effect transistor (MOSFET). Near the channel conductance threshold, we observe Coulomb blockade oscillations in the conductance, revealing the unintentional formation of tunnel barriers in the channel and the creation of a Si SET. We simultaneously monitor the conductance of each SET and observe a clear correlation between single-electron charging events in the two SETs, indicating that the SET islands are closely situated. The large charge ($\sim$0.33–0.35 e) induced onto the Al SET island by the addition of another electron onto the Si SET island indicates that the Si SET is strongly coupled to the Al SET, in the sense that the interisland capacitance is comparable to the total Si SET capacitance. Consequently, this device structure could be used to study individual tunneling events in the Si SET,[7] and it represents a single-electron current switch.[8] It could also be used to probe defect charge motion in MOS structures under large electric field at low temperature,[9] a potential source of decoherence for Si quantum computation.[10]

Figure 1(a) shows a scanning electron micrograph of a typical sample. Fabrication starts with the oxidation of a Si(100) wafer (resistivity $\rho > 8000$ Ω cm) at 1000 °C, yielding a SiO$_2$ thickness of about 20 nm. The wafer is selectively ion implanted with P at an energy of 50 keV and an areal density of 5×10^{14}/cm^2 to create n+ contacts. To limit the extent of the channel, p+ regions outside of the n+ contacts are created by another ion implantation of B at 18 keV with an areal density of 5×10^{14}/cm^2 [Fig. 1(b)]. The peak densities of both dopants are high enough to conduct at 20 mK and reside close to the Si/SiO$_2$ interface. If the two implantations are interchanged, a p-channel device can be made instead, so that both polarities can be fabricated on a single chip. After both implantations, the wafer is annealed at 950 °C for 60 s to activate the dopants and to repair implantation damage. Electron-beam lithography and self-aligned double angle evaporation are used to fabricate the leads and island of the Al SET,[11] as well as an Al side gate, used to modulate the conductance of both the Al SET and the MOSFET channel [Fig. 1(a)]. Finally, the sample is annealed at 425 °C in forming gas for 30 min to passivate dangling bonds at the Si/SiO$_2$ interface.

All of the measurements that we present here were made on a single device at a temperature of about 20 mK. A 1 T magnetic field was applied to keep the Al SET in the normal state. The device survived multiple thermal cycles to room temperature and displayed only small background charge offset variations between cycles. To avoid confusion, we present data from a single cooldown.

Figure 1(b) shows a schematic of the measurement circuit. Both n+ contacts are dc biased at V_{n+}, while the Al SET is grounded except for a small dc bias $V_{ds} \sim 100$ μV. An ac excitation $V_{ac} = 10$ μV rms at 46 Hz is applied between the two n+ contacts to measure the channel differential conductance. The two p+ regions are dc biased at potential $V_{p+} = -0.800$ V to confine the channel to a small region between them. Figure 1(c) presents typical data for the channel differential conductance ($G_{ch} = I_{ch}^{ac}/V_{ac}$) as a function of V_{n+} at constant side gate voltage $V_g = -0.604$ V. The appearance of Coulomb blockade oscillations is surprising, because no tunnel barriers are deliberately engineered in the channel.

In order to determine the coupling strength between the two SETs and to infer the proximity of the islands, systematic sweeps of V_g and V_{n+} are performed while the conductances of both SETs are measured. Figure 2(b) shows the Al SET conductance ($G_{Al} = I_{ds}/V_{ds}$), and Fig. 2(d) shows the channel SET differential conductance versus V_g and V_{n+}. If each SET were electrostatically isolated from the other, its conductance maxima would trace out straight lines in these graphs. Discontinuities from this straight-line behavior evi-

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a)Electronic mail: sunlyday@lps.umd.edu
b)Present address: Time and Frequency Division, National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80305.
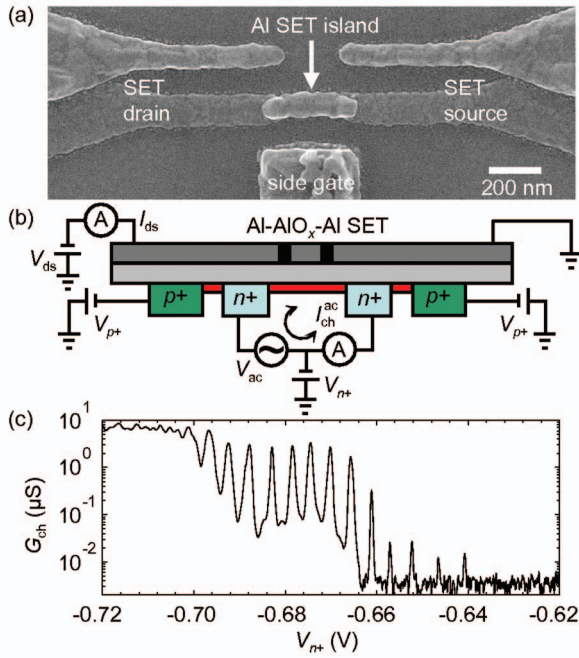
FIG. 1. (Color) (a) SEM image of a typical device. The Al SET island forms during the second of two evaporations at different angles. (b) Schematic of the measurement circuit. The conductance of each SET is measured using independent circuits. The red region represents the MOSFET conducting channel confined between the two $p+$ regions. The circles containing the letter "A" represent current-sensitive amplifiers. (c) Coulomb blockade oscillations of the Si SET differential conductance as a function of the relative bias V_{n+} between the Al SET and the Si SET at $V_g = -0.604$ V.

dent in Figs. 2(b) and 2(d) are a signature of discrete charging events close to the SET islands, events we would expect to observe if the two islands were in close proximity.[8,12,13] To confirm this hypothesis, the maxima in Figs. 2(b) and 2(d) are fitted with Gaussians, and the resulting peak centroids are
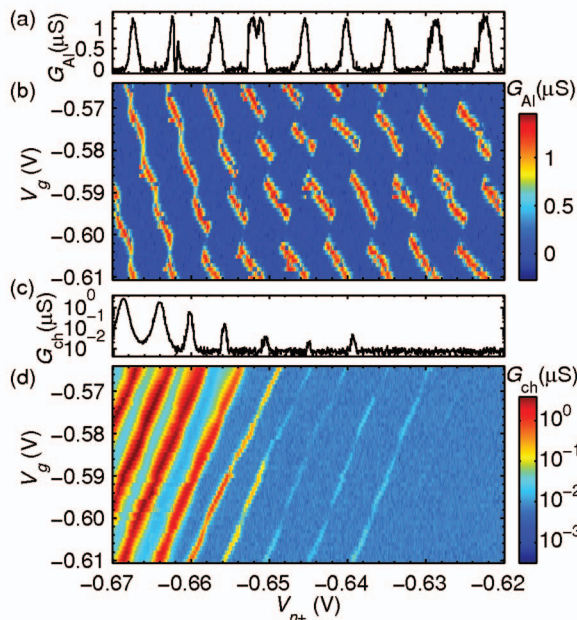

FIG. 2. (Color) Simultaneously measured conductances of both SETs. [(a) and (c)] Coulomb blockade oscillations of the Al and Si SET conductances, respectively, at $V_g = -0.610$ V. [(b) and (d)] Conductance of the Al and the Si SET, respectively, vs V_g and V_{n+}.
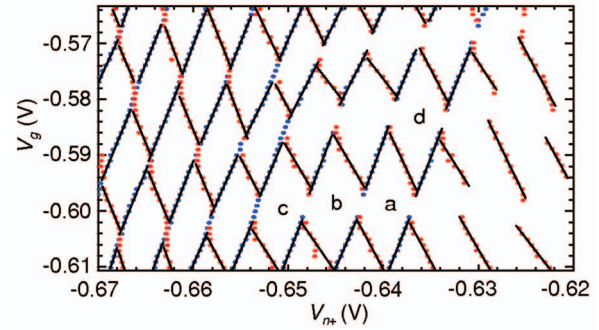

FIG. 3. (Color) Conductance maxima of both SETs vs V_{n+} and V_g. Red dots and blue dots are Gaussian fits to the data in Figs. 2(b) and 2(d), respectively. Black lines are a linear fit to the points on each edge. The regions labeled a, b, c, and d are the four hexagons whose parameters are presented in Table I.

plotted in Fig. 3. The two SETs display a clear correlation: whenever an Al SET conductance peak trace meets one from the Si SET, it makes an abrupt step, and vice versa. Because each peak trace corresponds to a unit change in the number of electrons on the corresponding SET island, this correlation proves that single-electron charging events in one SET are coupled to the other.

To more quantitatively explain the above results, we have modeled the device using the circuit depicted in Fig. 4(a). Under the assumption that the system can minimize its electrostatic energy automatically by independently adjusting the number of electrons N_{Si} and N_{Al} on the two SET islands, the total electrostatic energy of this circuit is given in matrix form by[14]

$$E(N_{Al}, N_{Si}, V_g, V_{n+}) = \frac{1}{2} Q^T \begin{pmatrix} C_{\Sigma\_Al} & -C_c \\ -C_c & C_{\Sigma\_Si} \end{pmatrix}^{-1} Q. \quad (1)$$

Here, $C_{\Sigma\_Al} = C_1 + C_3 + C_c + C_{g\_Al}$ and $C_{\Sigma\_Si} = C_2 + C_4 + C_c + C_{g\_Si}$ are the total capacitance of the Al SET and of the Si SET island, respectively, and $Q = (-eN_{Al} + C_{g\_Al}V_g + C_3V_{n+}, -eN_{Si} + C_{g\_Si}V_g + C_2V_{n+})^T$ includes the virtual and actual charges on the SET islands.[14] Under energy degenerate conditions, Coulomb blockade is lifted, resulting in the maximal SET conductances. There are in total six such degeneracy conditions associated with adding or subtracting one electron
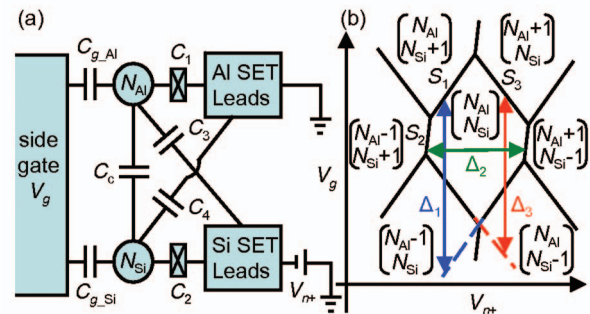

FIG. 4. (Color) (a) Circuit model for the coupled SET system. N_{Al} and N_{Si} are the number of electrons on the Al and the Si SET island, respectively. Due to the very small drain-source bias of each SET, we can simplify the two tunnel barrier capacitances for each SET to a single capacitance (C_1 and C_2) as shown. (b) Hexagonal phase diagram based on the model in (a). Each hexagon represents a configuration with a different number of charges on the SET islands. S_1, S_2, and S_3 are the slopes of the hexagon edges. Δ_1, Δ_2, and Δ_3 are the separations between opposite parallel edges of the hexagon.

TABLE I. Capacitances of the four hexagons labeled in Fig. 3 for the circuit model in Fig. 4.

Hexagon	C_2(aF)	C_c(aF)	C_3(aF)	C_4(aF)	C_{g_Al}(aF)	C_{g_Si}(aF)
a	20±6	16±1	14±1	7±1	4.1±0.2	6.0±0.2
b	32±6	21±1	7±1	1±1	4.6±0.3	6.0±0.3
c	32±4	22±1	7±1	2±1	4.1±0.3	6.7±0.2
d	31±5	21±1	10±1	2±1	3.9±0.2	5.9±0.2

from a SET island, determined by $E(N_{Al},N_{Si},V_g,V_{n+})$ $=E(N_{Al}+\delta N_{Al},N_{Si}+\delta N_{Si},V_g,V_{n+})+(\delta N_{Si})eV_{n+}$. Here, $\delta N_{Al}=0,\pm 1$; $\delta N_{Si}=0,\pm 1$; and $|\delta N_{Al}+\delta N_{Si}|<2$, and $(\delta N_{Si})eV_{n+}$ is the extra work done by voltage source V_{n+} when one electron tunnels through junction C_2.[15] These equations establish the hexagonal phase diagram depicted in Fig. 4(b), and there is a correspondence evident between this diagram and the data in Fig. 3. However, the capacitances associated with the Si SET appear to be bias voltage dependent, resulting in the non-identical hexagons in the data.

There are in total seven capacitance parameters in our circuit model. $C_1=282\pm 6$ aF is extracted from diamond chart measurements (not shown) with the MOSFET in the off state ($V_{n+}=0$ V). C_1 is dominated by overlap between the Al SET leads and its island and should be insensitive to the presence or absence of an underlying MOSFET channel. The remaining six parameters can be extracted from the slopes S_1, S_2, S_3 and the separations Δ_1, Δ_2, Δ_3 of each hexagon in Fig. 3, as defined in Fig. 4(b). We extract these parameters from the data as follows. First, the boundaries given by $\delta N_{Al}+\delta N_{Si}=\pm 1$ (the nominally straight lines traced out by the data in Fig. 3) are each fitted to a line. Boundaries corresponding to $\delta N_{Al}+\delta N_{Si}=0$ (an effective transfer of an electron from one island to the other) are not clearly visible, so they are determined by neighboring intersections of the visible boundaries. To compensate for gradual changes in the capacitances with bias voltage, averages are made for the slopes and separations from opposite boundaries within each hexagon. Then, the six unknown capacitances can be extracted by solving six analytical equations relating S_1, S_2, S_3, Δ_1, Δ_2, and Δ_3.

Discrete background charge motion near the SET islands, which changes the electrostatics of the system, makes systematic study of all the hexagons in Fig. 3 difficult. The capacitances for the four typical hexagons labeled in Fig. 3 are presented in Table I. For hexagon a, $C_{\Sigma\_Si}=49\pm 6$ aF. A diamond chart measurement of the Si SET near this bias point (not shown) gives $C_{\Sigma\_Si}=49\pm 3$ aF, in good agreement and confirming the validity of the circuit model. Significantly, for all the hexagons in Table I, $C_c/C_{\Sigma\_Si}\sim 33\%-35\%$ indicates that the Si SET is strongly coupled to the Al SET, while $C_c/C_{\Sigma\_Al}\sim 5\%-7\%$ explains why the discontinuities in Fig. 2(d) are less obvious than those in Fig. 2(b).

If the overlap between the two SET islands were perfect, the value of C_c as calculated from the Al SET island dimensions and the SiO_2 thickness would be about 30 aF. This is close to the values in Table I for hexagons b–d. The small values for C_4 in these hexagons mean that there is almost no overlap between the Si SET island and the Al SET leads. This strongly suggests that the induced Si SET island is located directly beneath the Al SET island.

We hypothesize the following reasons for the formation of an aligned SET in the channel. Although the width of the SET island and that of the leads in the evaporation shadow mask are the same, the SET island is formed during the second evaporation. A slow pinch off of features in the mask during the first evaporation therefore makes the island slightly narrower than the leads. If the angle between the evaporations is incorrect, there may also be a lateral offset between the island and leads. This island/leads width asymmetry and lateral offset may lead to lateral constrictions in the MOSFET channel below, creating tunnel barriers and therefore a SET in the channel aligned with the Al SET above.

This SET sandwich architecture could be used to characterize the MOS structure at low temperature via a cross-correlation measurement between the two SETs.[4] For example, measurements of the Al SET show that about 10 electrons have already accumulated on the Si SET island when the first measurable Si SET conductance peak appears. This architecture could help identify sources of unwanted charge motion that may also be sources of decoherence for Si quantum computation. Because the SiO_2 layer could be made much thinner, future experiments could more fully explore the strongly coupled two SET regime.

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