Phys. Status Solidi C **8**, No. 3, 816–818 (2011) / **DOI** 10.1002/pssc.201000076

physica status solidi c
www.pss-c.com
current topics in solid state physics

Electrical characterisation of Si-SiO_2 structures

Ivana Capan*, Branko Pivac, and Robert Slunjski

Rudjer Boskovic Institute, Bijenicka 54, 10 000 Zagreb, Croatia

Received 1 April 2010, revised 4 May 2010, accepted 10 May 2010
Published online 15 November 2010

Keywords silicon, oxide, interface, DLTS

* Corresponding author: e-mail capan@irb.hr, Phone: +00 385 1 456 1111, Fax: +00 385 1 468 0114

The possibility of studying the Si-SiO_2 structures by means of deep level transient spectroscopy (DLTS) has been presented. Contrary to the standard application of this technique, the temperature interval has to be reduced. In order to minimize the influence, and possible errors due to the capacitance base line shift and the Fermi level pinning, C-V characterization at different temperatures is crucial prior the DLTS measurement. The interface traps related to the P_b centers, distributed around 0.35 eV below the conduction band, have been observed.

1 Introduction

Over the past several years one of the most expanding research field in the area of nanoelectronics deals with three-dimensionally confined semiconductor nanocrystals in the oxide matrix. The reason is their promising application in nonvolatile memories [1], third generation solar cells [2] and single-electron devices [3]. These structures have predominantly been studied by structural and optical characterization techniques, such as transmission electron microscopy (TEM), infrared absorption spectroscopy (IR) and photoluminescence (PL). However, the electrical properties of semiconductor nanocrystals are crucial for the future device applications. The number of studies dealing with electrical properties is increasing in the past few years. The capacitance-voltage measurements (C-V) of metal-oxide-semiconductor (MOS) structures with a silicon dioxide layer (SiO_2) containing Si or Ge nanocrystals have attracted considerable attention. However, when studying such MOS structures with electrical characterization techniques, several problems arise. The most important one is the influence of the oxide-semiconductor interface, which contains interface traps, on the electrical properties of the nanocrystals distributed very close to the interface. Moreover, the question how does those traps (i.e. fast traps), as well as the fixed charges in the oxide in vicinity of the interface (i.e. slow traps) affect the charge storage in the nanocrystals, is still unanswered. The fast traps are linked with P_{b_0} centers while the slow traps are mostly correlated with E' centers. Both centers have been established by electron-paramagnetic-resonance (EPR) measurements to be trivalent silicon atoms with an unpaired valence electron arising from an unsatisfied silicon-oxygen bond [4]. As mentioned before, information regarding the energy distribution, the density of traps and capture kinetics of the interface and oxide traps are crucial for the future device applications. To obtain those information deep level transient spectroscopy (DLTS) could be used. The DLTS is a well established technique which is commonly used in studying the trap states in the semiconductors [5], and recently it has been applied in studying the semiconductors quantum dots (QD) [6]. It can provide information regarding the activation energy, trap concentration, capture cross section and spatial distribution.

In order to apply DLTS for studying MOS structures containing the nanocrystals it is necessary to obtain and analyze DLTS results on clean MOS structures (i.e. without nanocrystals in the oxide). This will enable us to separate DLTS signals coming from Si-SiO_2 interface and Si nanocrystals. In this work, we present a study of the Si-SiO_2 structure by means of DLTS.

2 Experimental details

The single crystal Si (100) substrate used in this study was prepared by Cemat Silicon S.A. (Warsaw, Poland). The substrate was phosphorous-doped with initial resistivity in the range 10 to 20 Ωcm. SiO_2 film was thermally grown at an oxidation temperature of 1000 °C in a [H_2 + O_2] atmosphere (wet oxide). The obtained oxide thickness

was 49 nm. For the ohmic and gate metallization pure Al and Au were used, respectively. High-frequency (1MHz) C-V characterization was performed at different temperatures. All DLTS spectra were taken with a SULA Technologies spectrometer.

3 Results and discussion

Figure 1 shows C-V measurements observed for the Si-SiO_2 MOS structure at different temperatures. This step-like form or "S-shape" is typical for the MOS structures on n-type Si substrate in case of high frequency measurements [7]. For the positive voltage the capacitance reaches its maximum value (accumulation region), while for the negative voltage the capacitance is reducing to the minimal value (inversion region). However, as the sample temperature decreases from 300 K to 150 K, the accumulation region shifts to higher voltages. This effect is well known and has been described as being due to discrete energy levels related to the interface states [8].

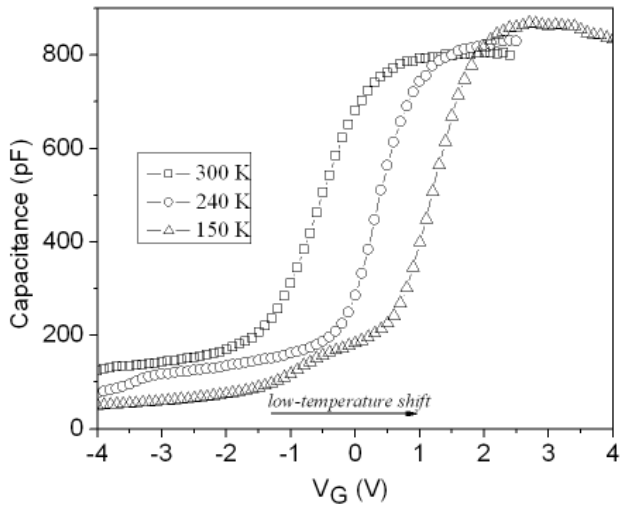

Figure 1 The 1 MHz C-V curves observed for the (100) Si-SiO_2 structure at different temperatures.

Although the conventional DLTS has been used in numerous studies of MOS structures, the reported results and proposed analysis differ from study to study. By use of large-pulse DLTS [9, 10] and small-pulse DLTS [11, 12] several interface-related traps have been observed. However, there are several reasons why conventional DLTS measurements are very difficult to interpret. The conventional DLTS signal is measured as a function of temperature (usually in a range from liquid nitrogen temperature to room temperature). The scanning of the temperature causes a change in the capacitance signal due to the thermal dependence of the electron emission rate. The important assumption is $\Delta C << C$ i.e. the measured traps make only a small contribution to the sample total capacitance. This is not the case for the interface traps. Moreover, the knowledge of the Fermi level position during the measurements is important. It is given by the length λ, the depth for which the energy level of defect E_t crosses the Fermi level E_F for the selected polarization. However, the behaviour of the Fermi level at the interface is strongly affected by the temperature. The shift of the accumulation region to higher voltages (as seen in Fig. 1) has been explained by the Fermi level pinning effect [8]. The magnitude of the Fermi level pinning depends on temperature.

In the recent paper by Dobaczewski et al. [8], the authors have addressed those issues. As they pointed out, the main disadvantage of conventional DLTS measurements on MOS structures is the capacitance base line shift and the Fermi level pinning effect [8]. Those arguments are very conclusive. If, e.g. we chose +1 V for the bias and make a DLTS scan (77–300 K) on a MOS structure (shown at Fig. 1) at 150 K we probe the depletion region, while at 300 K we have reached the accumulation region.

Taking into account all the facts, we offer the scenario of how and when the conventional DLTS could be used for studying the interface traps. As shown in Fig. 1, for the low temperature (150 K) the accumulation region is reached at higher voltages. We have used biases between 2 and 2.8 V for the DLTS measurements in a selected temperature interval (140-200 K). With those measurement settings we have assured that as the temperature increase we scan the same region i.e. accumulation. Moreover, as we have reduced the temperature range, the Fermi level pinning effect is reduced as much as possible. Figure 2 shows DLTS spectra observed after measurements of the Si-SiO_2 structure for different rate windows with bias settings correlated with accumulation region. The origin of the DLTS signal, for a positive gate voltage electrons are captured at the interface, is illustrated in the inset.

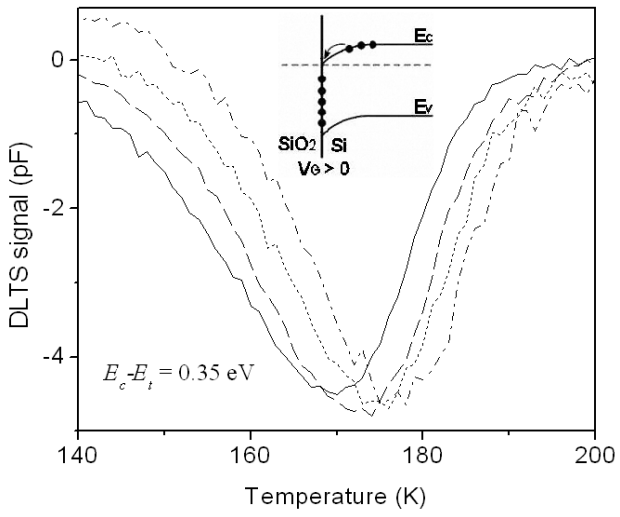

Figure 2 The DLTS spectra of the Si-SiO_2 structure for different rate windows with bias settings correlated with accumulation region, V_G>0. In the inset: the origin of the DLTS signal, for a positive gate voltage electrons are captured at the interface traps.

The activation energy for the electron emission is determined from Arrhenius plot of $\ln(e_n/T^2)$ versus $1/kT$. In the selected temperature interval (140 -200K) five different rate windows were used. The obtained value of 0.35 eV is shifted toward higher energies by 0.05 eV comparing to the value of 0.3 eV which is quoted in a large number of papers where DLTS measurements on the P_b centers are reported [8, 13]. However, this value is shifted toward lower energies comparing to the value of 0.43 eV which has been reported for the (100) Si-SiO_2 interface studied by isothermal Laplace DLTS [8]. We have ascribed our 0.35 eV trap to the P_b centres-related trap which exist in the upper half of the silicon band gap.

The interface state densities D_{it} have been estimated according to [12]:

$$D_{it} = \frac{\varepsilon_r \varepsilon_0 A N_D C_{ox}}{C_q^3 kT} \Delta C \qquad (1)$$

where C_q is the quiescent capacitance, ΔC is the amplitude, A the capacitor area, N_D the semiconductor doping concentration, C_{ox} the capacitance in accumulation, and T the temperature of the peak maxima. We have estimated the value of D_{it} as $5 \cdot 10^{11}$ eV^{-1} cm^{-2}, which is very low.

4 Conclusions

In this work, we have demonstrated that, despite many difficulties, the conventional DLTS could be used for studying the interface traps. Prior the measurements, C-V characterization at different temperatures is crucial, for defining the measurement parameters such as bias conditions and temperature range. We have shown that in the case of (100) Si-SiO_2 structure the interface-related trap is detected. The 0.35 eV is ascribed to the P_b centres-related trap.

Acknowledgements This work has been supported by Unity Through Knowledge Fund (UKF Grant Agreement no. 48).

References

[1] J.-M. Shieh, J. Y. Huang, W.-C. Yu, J.-D. Huang, Y.-C. Wang, C.-W. Chen, C.-K. Wang, W.-H. Huang, A.-T. Cho, H.-C. Kuo, B.-T. Dai, F.-L. Yang, and C.-L. Pan, Appl. Phys. Lett. **95**, 143501 (2009).
[2] B. Pivac, P. Dubcek, I. Capan, I. Zulim, T. Betti, H. Zorc, and S. Bernstroff, J. Nanosci. Nanotechnol. **9**, 3853 (2009).
[3] F. Yun, B. J. Hinds, S. Hatatani, and S. Oda, Jpn. J. Appl. Phys. **39**, L792 (2000).
[4] S. N.Volkos, E. S. Efthymiou, S. Berbardini, I. D. Hawkins, A. R. Peaker, and G. Petkos, J. Appl. Phys. **100**, 124103 (2006).
[5] L. Dobaczewski, A. R. Peaker, and K. B. Nielsen, J. Appl. Phys. **96**, 4689 (2004).
[6] S. W. Lin, C. Balocco, M. Missous, A. R. Peaker, and A. M. Song, Phys. Rev. B **72**, 165302 (2005).
[7] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology (Wiley, New York, 1982).
[8] L. Dobaczewski, S. Bernardini, P. Kruszewski, P. K. Hurley, V. P. Markevich, I. D. Hawkins, and A. R. Peaker, Appl. Phys. Lett. **92**, 241104 (2008).
[9] D. Vuillaume, J. C. Bourgoin, and M. Lannoo, Phys. Rev. B **34**, 1171 (1986).
[10] H. Lakhdari, D. Vuillaume, and J. C. Bourgoin, Phys. Rev. B **38**, 13124 (1988).
[11] S. Ozder, I. Atilgan, and B. Katircioglu, Semicond. Sci. Technol. **10** 1510 (1995).
[12] R. Beyer, H. Burghardt, I. Thurzo, D. R. T. Zahn, and T. Geβner, Solid-State Electron. **44**, 1463 (2000).
[13] P. K. Hurley, B. J. O'Sulivan, F. N. Cubaynes, P. A. Stolk, F. P. Widdershoven, and J. H. Das, J. Electr. **149**, G194 (2002).

