Internal and external gettering of iron contamination in power technologies

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Substrate gettering and the contribution to contamination reduction of backside layers are evaluated after high temperature annealing following intentional iron contamination at backside in silicon epitaxial wafers typical of Bipolar-CMOS-DMOS (BCD) power technologies. Iron is detected at frontside by Deep Level Transient Spectroscopy within a depth corresponding to the actual devices. This work allows to simulate a contamination occurring at the beginning of the semiconductor process flow and to isolate the role of the different gettering mechanisms. Substrate boron in epitaxial p over p+ wafers is effective in more than halving iron contamination at front compared to a p-only substrate, especially at high contamination dose. In the absence of a specific thermal cycle for oxygen precipitation and growth in the bulk, long thermal treatment at 1200°C could induce a significant precipitates growth even at the beginning of the process flow, greatly contributing to iron gettering in the bulk. However, this effect is found to strongly depend on the silicon condition after crystal growth. No significant contribution to iron gettering from a backside polycrystalline silicon layer is found after high temperature annealing, while a back oxide acts as diffusion barrier effectively screening the substrate from contamination only for short thermal treatments or annealing temperature below 1000°C.

1. Introduction

Iron is a common and often unavoidable contaminant found in the integrated circuits (IC) production line that can affect device properties such as oxide integrity,[1,2] carrier lifetime[3], and

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junction leakage current.[4] To reduce iron contamination at the device level, several strategies are put in place in modern technologies. Internal gettering relies on iron relaxation in the heavily boron doped region of the substrate or gettering at oxygen precipitation sites and related defects in the bulk.[5,6] On the other hand, external gettering is often added to further reduce contamination by applying a certain finishing to the backside of the wafer, such as a backside layer, backside damaging or implantation. For example, polycrystalline silicon was found to provide effective gettering especially for fast diffusing elements such as Ni and Cu.[7] A third methodology to reduce contamination in the device, which is used especially for slow diffusing contaminants, is proximity gettering by on purposely implanted areas close to the devices.[8]

Silicon power technologies have specific characteristics and requests in terms of contamination control. Considering the high voltages involved, contamination could hamper the oxide quality and reduce the junction breakdown voltage. Furthermore, long high temperature thermal treatments at 1100°C and above are present in the initial steps of the process flow. This exposes the wafers to a high risk of contamination since at this stage oxide precipitates contributing to internal gettering are not yet fully formed.

We envisioned an experiment aimed to test substrates gettering efficacy to prevent a possible contamination coming from the backside at the beginning of the process. Substrates with different backside layers, boron concentration and coming from different suppliers were implanted on the backside with Fe atoms producing a shallow implant with controlled dose. Thermal treatments spanning from rapid thermal processing (RTP) to long furnace annealing at temperature up to 1200°C were performed to test several process conditions. After intentional contamination and diffusion, deep level transient spectroscopy (DLTS) technique was applied at frontside to quantify the contamination level reaching the device region.

The comparison among contaminated substrates and processing conditions allows to isolate the several contributions to gettering efficacy.

2. Experimental Section

Sample preparation: the experiment comprises Czochralski boron doped substrates (resistivity 10 Ω·cm and as grown oxygen content less than 12 ppma, ASTM F121-83 standard) and p/p+ epitaxial wafers (20 mΩ·cm substrate resistivity, interstitial oxygen in the 11-14 ppma range, ASTM F121-83 standard, and 10 Ω·cm resistivity of the epitaxial layer). The backside of the epitaxial wafers is either double side polished or has different backside layers, according to **Table 1**. Polycrystalline silicon and low temperature oxide (LTO) layers are deposited by the silicon supplier, while thermal oxide is grown by furnace annealing at 1100°C. In a few samples, densification of the LTO is performed by furnace annealing at 1150°C.

Table 1. Backside layers and resistivity of the specimens.

Sample type, backside	Backside poly.silicon (nm)	Backside oxide (nm)	Substrate	Epitaxy
p/p+, poly.silicon and LTO	800	800	P+, 20 mΩ·cm	P, 10 Ω·cm
p/p+, LTO		300 800	P+, 20 mΩ·cm	P, 10 Ω·cm
p/p+, thermal or densified back oxide		300	P+, 20 mΩ·cm	P, 10 Ω·cm
p/p+, poly.silicon	800		P+, 20 mΩ·cm	P, 10 Ω·cm
p/p+ substrate			P+, 20 mΩ·cm	P, 10 Ω·cm
p substrate			P, 10 Ω·cm	

To introduce Fe contamination, substrates are implanted on the backside at 60 keV, tilt 7° to produce a shallow Fe implant (ion range 55 nm in Si and 51 nm in SiO_2). Ion implantation is chosen to best control the contamination level, while different implant doses (10^{11}, 10^{12} and 10^{13} at cm^{-2}) allow to reproduce different contamination conditions. Wafers with diameter of 20 cm are implanted only in a central circle of 10 cm in diameter to preserve an in-wafer reference monitor for

background contamination. The detected background level is about one decade lower or less than the intentional iron contamination.

After Fe implantation, the wafers are annealed with different alternative thermal budgets to diffuse Fe atoms in the silicon substrate and simulate contamination events. Rapid thermal processing (RTP) is performed in N_2 ambient at 1100°C for 180 s with cooling ramp of 5°C s^{-1}. Furnace thermal treatments are performed in N_2 ambient with 5% O_2 during ramp-up to avoid surface nitridation. Four different thermal treatments are performed: 30 min 1000°C, 90 min 1100°C, 120 min 1100°C, 180 min 1150°C or 180 min 1200°C. Furnace treatments are followed by RTP to enhance Fe detection in solution thanks to its fast cooling ramp.

Schottky junctions are prepared on sample frontside by optical lithography followed by surface cleaning in diluted HF and Ti/Pt sputter deposition and lift-off. Ohmic contact on wafer backside is ensured by backside lapping followed by Al deposition. All metal depositions are performed at room temperature to reduce Fe diffusion.

Experimental technique: Fe concentration is determined by DLTS using a DLS-1000 spectrometer from Semilab. Spectra are acquired between 40 K and 300 K with a reverse bias of +5 V, a filling pulse of +0.5 V and a secondary pulse of +4.5 V to avoid edge effects (corresponding to an inspection depth of 1 – 2.5 µm from surface). The duration of the filling pulse is fixed at 20 µs, while the lock-in frequency is set at 23 Hz for temperature scan.

Analysis of the oxygen precipitation in the silicon bulk is performed by sample cleave and etch for 120 s with Secco d'Aragona solution[9] followed by SEM inspection in cross section.

3. Experimental results

Several samples with p or p/p+ substrates and different backside layers were implanted with Fe atoms on the backside to induce Fe contamination. Iron implantation was chosen to carefully control the contamination dose, which was varied between 10^{11} cm^{-2} and 10^{13} cm^{-2}. An annealing

treatment drove diffusing Fe atoms towards the frontside, where DLTS measurements were carried out to detect active traps in the lower half of the silicon bandgap.

DLTS spectra of the samples implanted with Fe atoms after annealing show two main distinct peaks attributable to interstitial iron (Fe_i) and FeB donor-acceptor pairs **(Figure 1)**: a linear fit of the inverse temperature dependence of thermal emission rates for the two peaks allows to extract activation energies of (0.439 ± 0.014) eV and (0.090 ± 0.011) eV, in good agreement with previous data for Fe_i and FeB traps, respectively.[10] On the other hand, FeB peak is always much higher than Fe_i peak since measurements were taken several days after sample preparation with samples stored at room temperature and in p-type samples at equilibrium most of the iron is present in the paired form.[11] Considering that FeB constitutes almost 98% of the total Fe components and that other contaminant peaks could overlap in the spectral region of Fe_i, we considered only the FeB peak for the quantification of Fe concentration.

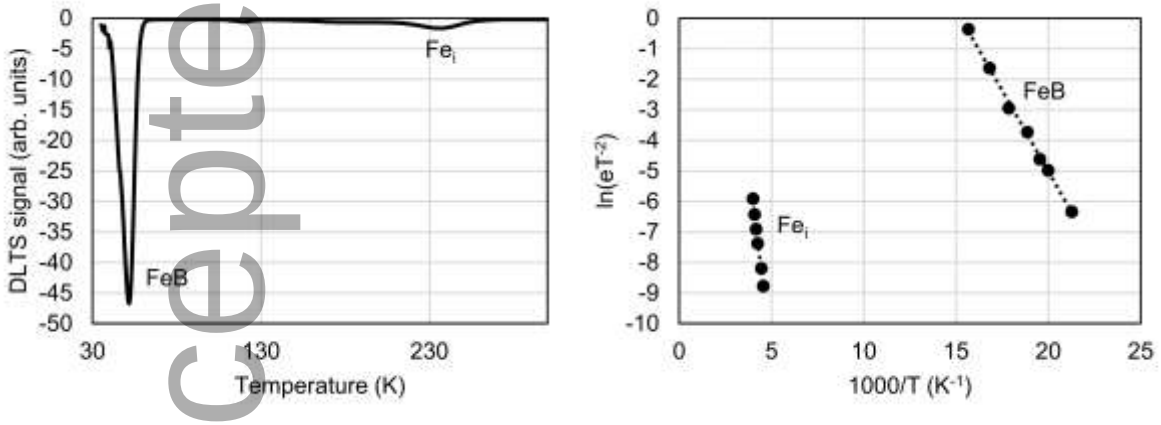

Figure 1. DLTS temperature spectrum of a p substrate implanted with a Fe dose of 10^{13} at cm^{-2} at backside and RTP annealed at 1100°C for 3 min. Two main peaks can be identified, which can be associated with Fe_i and FeB traps based on thermal emission rates.

Iron is a medium-fast diffuser in silicon and already at room temperature its diffusion is not negligible.[11] Therefore an RTP treatment at 1100°C for 180 s is sufficient to make a significant portion of the implanted iron at backside reach the front surface. Moreover, performing only this short treatment, no oxygen precipitation occurs in silicon and no other gettering centers are present

in the bulk. This allows to estimate the gettering efficacy produced only by boron doping. **Figure 2** reports the iron concentration revealed at frontside by DLTS in p and p/p+ substrates implanted at backside with iron doses of 1×10^{11} cm^{-2} and 1×10^{13} cm^{-2} after RTP treatment. Considering first bare substrates without any backside layer, in the p-only substrate with uniform resistivity Fe is expected to distribute evenly across the thickness. However, already in this sample Fe content shows an 82-90% loss compared to what can be expected assuming that all the implanted dose has been uniformly spread across the 725 μm wafer thickness. This could be explained by surface segregation during cooling. Indeed, ToF-SIMS profiling confirms a Fe signal increase close to the surface **(Figure S1)**.

Comparing p and p/p+ samples, in the p/p+ the contamination detected at frontside in the bulk silicon shows a reduction of about 66% for the 10^{13} cm^{-2} dose. This effect can be ascribed to preferential segregation of Fe atoms in the heavily boron doped bulk.[6,12,13] This contamination reduction produced by the difference in boron content between substrate bulk and epitaxy is of particular importance since it reflects the initial stages of the IC manufacturing process, when no other gettering centers exist in the wafer and high temperature treatments are involved. With the low contamination dose of 10^{11} cm^{-2} the reduction in p/p+ compared to the p substrate decreases to 46%, albeit with greater error in these measurements due to implant variability and detection sensitivity at this low concentration. A concentration dependent gettering efficiency was already observed for other transition metals such as copper.[14]

When backside layers are added to the p/p+ substrate, no significant improvement is observed with 800 nm polycrystalline silicon. This result can be surprising, taking into account recent literature on gettering effect of grain boundaries in multicrystalline silicon[12,15] and in polycrystalline silicon layers.[7,16] However, it should be noted that several characteristics of the deposited polycrystalline silicon layer, such as deposition temperature and thermal history, grain size and doping can greatly influence the impurity gettering efficiency. Iron gettering in polysilicon was found to happen

significantly after slow cooling below 900°C or by isothermal annealing at 700°C.[17] Moreover, it was reported that after high temperature annealing the gettering efficiency of backside polycrystalline silicon layers are greatly reduced.[16] Unfortunately, these treatments are commonly present in power device processing and our result greatly reconsiders the importance of a polycrystalline silicon layer for gettering of iron contamination.

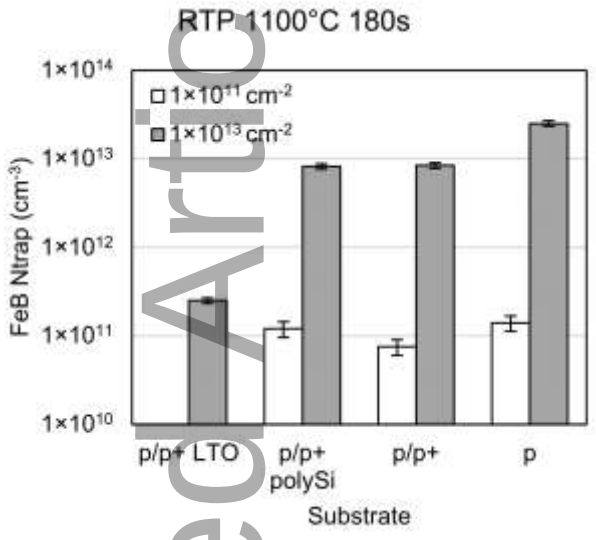

Figure 2. Fe concentration detected by DLTS at frontside in different substrates Fe implanted at backside after 3min RTP annealing at 1100°C.

A different role is played by the backside LTO. No gettering occurs in this layer, but iron diffusion in oxide is significantly reduced compared to silicon: diffusivity ratio is about 10^{-7} at the temperatures tested[18] and a sufficiently thick oxide layer can prevent iron from entering the substrate. This shielding role is significant for short annealing such as the one in Figure 2, but it decreases for increasing thermal budget. **Figure 3** shows the iron concentration at frontside in a p/p+ substrate with 800 nm of backside LTO for different thermal treatments. After long furnace annealing at 1200°C, iron concentration reaches a similar level to the one found in Figure 2 for the bare p/p+ substrate, meaning that most of the iron has crossed the oxide. Further annealing steps only mildly increase the iron concentration.

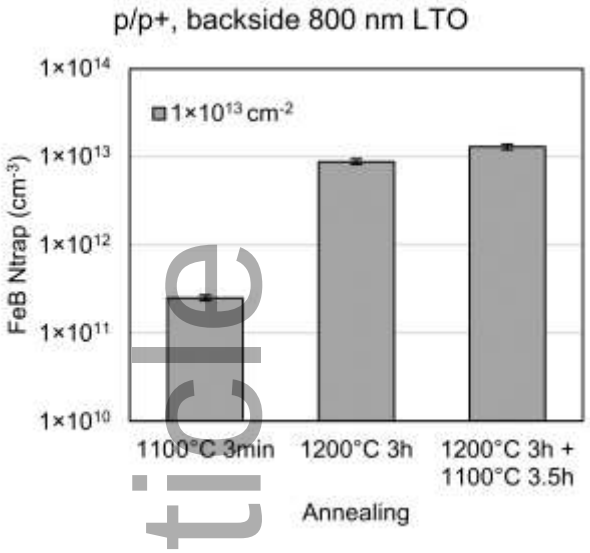

Figure 3. Fe concentration reaching frontside for different thermal budgets. Substrates with 800 nm backside LTO were implanted at backside with Fe dose 10^{13} at/cm^2.

The above experiment with 800 nm of backside LTO and annealing at 1200°C was repeated with implant doses of 10^{11} at cm^{-2} and 10^{12} at cm^{-2} to simulate several contamination scenarios. A lower gettering efficacy at low contamination dose is verified in **Figure 4** as for the lowest dose of 10^{11} cm^{-2} the iron concentration no longer follows a linear decline as a function of the contamination dose. This is a further indication of a concentration dependent gettering efficiency of the internal gettering in the substrate. This phenomenon is plausibly related to segregation gettering, since for relaxation in the highly boron doped region a concentration dependence is not expected.

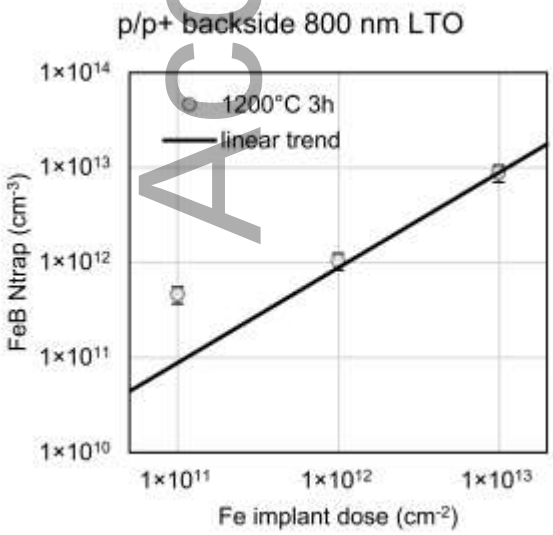

Figure 4. Fe concentration detected at frontside for different Fe backside implant doses. Substrates with a backside LTO layer of 800 nm were thermal threated for 3h at 1200°C.

A similar experiment was carried out in **Figure 5** after Fe implantation with the lowest dose of 10^{11} cm^{-2} and several furnace treatments in substrates with 300 nm of thermal oxide instead of a deposited LTO. Similarly, iron concentration increases for increasing thermal budget and, within variability, it reaches a plateau at 1150°C. These results well collimate with the estimated diffusion of iron in SiO_2[18,19]: considering annealing ramps, diffusion lengths of 90-150 nm, 400 nm, 600-800 and 800-1200 nm are expected after annealing at 1000°C, 1100°C, 1150°C and 1200°C, respectively. The ranges depend on the literature considered. It should be considered that even if the LTO is initially more permeable to iron than the thermal oxide, during high temperature annealing it is densified and iron diffusion does not differ much from the thermal oxide. This is further confirmed in **Figure 6** comparing Fe contamination after high temperature annealing when implantation is carried out in standard LTO or in a pre-densified LTO, finding only a minor difference. Moreover, when additional thermal budget is added, Fe contamination does not increase much, meaning that most of the iron has already been gettered or diffused to frontside.

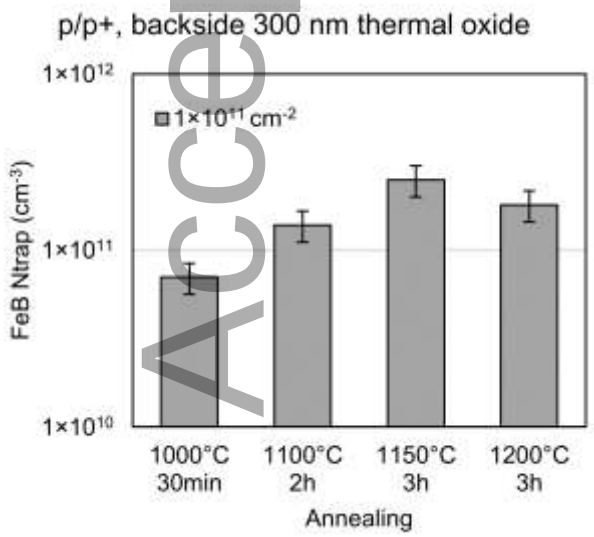

Figure 5. Fe concentration reaching frontside for different thermal budgets. Substrates with 300 nm thermal backoxide were implanted at backside with Fe dose 10^{11} at/cm^2.

These results point out that a back oxide could be effective in stopping iron contamination coming from the backside (e.g. from wafer handling) only for short RTP treatments or for furnace annealing not exceeding 1000°C.

All the aforementioned experiments were carried out on substrates coming from the same ingot (from here on called ingot 1) in order to reduce variability. The amount of gettering sites depends on the interstitial oxygen content and on the concentration and dimension of oxygen precipitation centers in the wafer produced during the pulling process. Therefore, wafers from different suppliers subjected to the same thermal budget could have different amount of gettering sites despite having similar oxygen content. This condition occurs in **Figure 6**. By cleave and etch method in ingot 1 we estimate a BMD density of 3×10^{8} cm^{-3}, while in ingot 2 almost no BMDs are visible (density < 6×10^{6} cm^{-3}). This translates in a 3 times difference of gettering efficiency after annealing at 1200°C. It should be considered that no specific annealing for BMD precipitation and growth was carried out, but are the thermal treatments at 1200˚C and 1100˚C, which perform that function. This result suggests that even at the beginning of the IC process, when high temperature annealing are involved, the role of internal gettering from oxygen precipitates and related defects plays a considerable role.

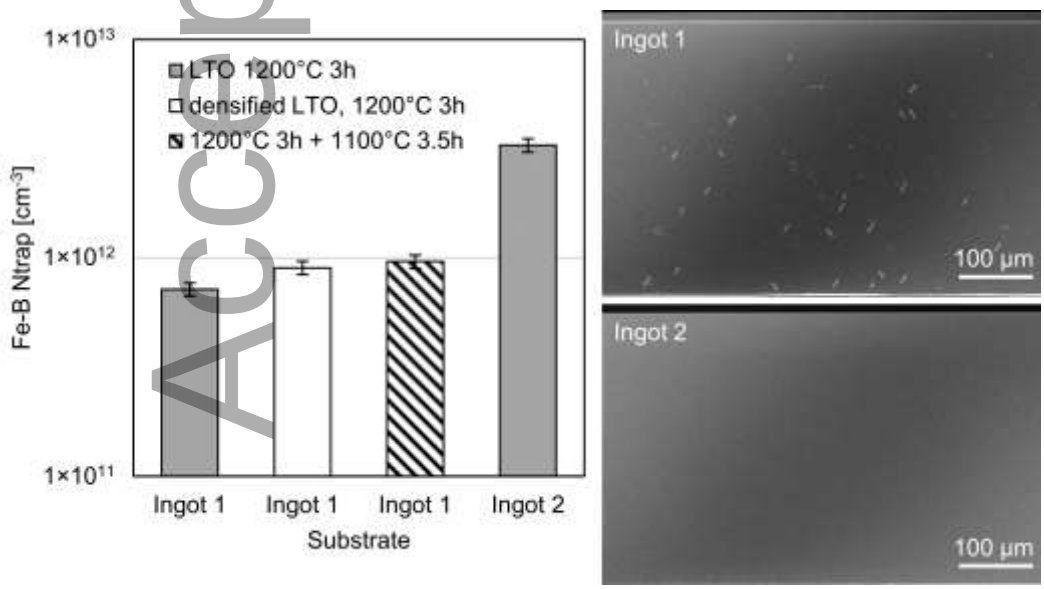

Figure 6. Bar chart: Fe concentration reaching frontside in wafers from two different suppliers but similar specifications (ingot 1 and ingot 2). Substrates with 300 nm LTO backoxide were implanted at backside with Fe dose 10^{12} at/cm^{2}. On the right, cross section SEM images after cleave and etch to reveal defects in the bulk in the two ingots after annealing at 1200°C for 3h.

4. Conclusion

In power technologies, iron contamination at the beginning of the process flow is especially critical following high temperature annealing. Several strategies are put in place to contain contamination by substrate gettering and shielding. In this work, different contributions to Fe gettering are evaluated after short RTP annealing or long thermal treatments up to 1200°C in substrates typical of BCD technologies. Gettering in the heavily boron doped region of p/p+ epitaxial wafers is effective in reducing contamination at frontside by more than a factor of two when compared to p wafers, especially for the highest contamination dose tested.

When long thermal treatments are carried out, gettering by oxygen precipitates formed in the bulk starts to contribute to substrate gettering. A Fe contamination reduction of a factor of three is achieved with a BMD density of 3×10^{8} cm^{-3} compared to a substrate without any visible bulk defect. In the absence of an on-purpose oxygen nucleation treatment, oxygen precipitation occurs at nuclei already present after ingot pulling and, since the amount of oxygen precipitates strongly depends on the ingot pulling specifics, different silicon suppliers report different gettering effectiveness. Considering external gettering, a polycrystalline silicon of 800 nm layer deposited on the backside of the wafer was not found to provide any significant reduction of Fe contamination after high temperature treatment. On the other hand, back oxide layers, either deposited at low temperature or grown thermal oxide, could screen contamination coming from the backside only for short annealing treatment or for furnace annealing below 1000°C.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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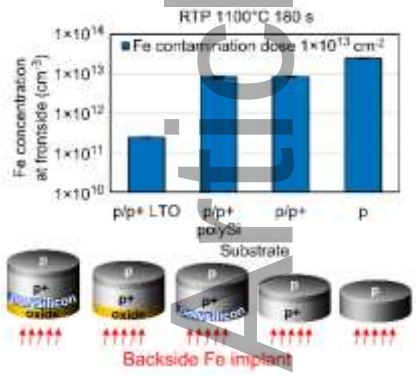

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