Resistive switching device with highly-asymmetric current-voltage characteristics: its error analysis and new design parameter

To cite this article before publication: Jinho Bae *et al* 2018 *Semicond. Sci. Technol.* in press https://doi.org/10.1088/1361-6641/aaf7d3

Resistive switching device with highly-asymmetric current-voltage characteristics: its error analysis and new design parameter

Jinho Bae[1]* and Nobuhiko P. Kobayashi[2]

[1]Department of Ocean System Engineering, Jeju National University, 102 Jejudaehakro, Jeju 63243, Korea

[2]Baskin School of Engineering, University of California Santa Cruz, 1156 High Street, Santa Cruz, CA 95064, USA

***E-mail: baejh@jejunu.ac.kr**

Abstract

As a solution to future non-volatile random access memories (NV-RAMs) with large scale integration, many researchers are studying a crossbar array built with many resistive switching cells because of its simple architecture and scalability. However, a sneak current in the crossbar array that energizes memory cells not explicitly selected, rises various issues that need to be addressed for commercialization. Hence, we clearly describe what are the dominant cause and consideration in a passive crossbar array based on memrstors. We discover that such resistive switches under reverse bias along the sneak current paths can play an important role to minimize overall sneak current by blocking their reverse current. To develop a commercializable passive crossbar resistive switching arrays, we demonstrate a read error bound and propose a new design parameter (R_{RL}/R_{FL} as ratio of reverse low resistance state and forward low resistance state) using the switching resistances on the forward and reverse current paths.

Keywords: Crossbar array, resistive switch, sneak current, error bound, design parameter.

1. Introduction

The complementary metal oxide semiconductor (CMOS) technologies are approaching to their physical limits due to quantum uncertainties, heat problems, and economic issues of new fab costs [2, 3]. To replace dynamic random access memory (DRAM) memories, in 2008,

Hewlett-Packard Laboratories reported the resistive switching device (or memristor) [4] as the fourth fundamental passive circuit element that was postulated by Leon O. Chua in 1971 [5]. As an alternative memory device, the resistive switch has attracted worldwide attention as a promising next generation nonvolatile memory (NVM) due to its high density fabrication [6, 7]. Utilizing unique resistance switching behaviors, many single bit memristor-based NVMs have been proposed, which can store two distinctive resistance states, high resistance state (HRS) and low resistance state (LRS) [8, 9]. For the high density integrations of NVMs, crossbar arrays with single bit resistive switch cells are demonstrated [3-6]. However, those crossbar designs incur severe sneak current problems, which result in the serious read errors and unnecessary power consumption when the intended memory cells are accessed [1]. Especially, the sneak current issue becomes more pronounced as the size of a crossbar array increases. To overcome the sneak current issue, the various approaches have been proposed, including a rectifying element connected to a resistive switch in series at each cross-point [10, 11] and anti-serial memristors complementary resistive switches [12]. Although these attempts have addressed the sneak current issue to some extent, further investigations are required through various viewpoints for this issue [1].

In a passive crossbar array, a specific row-column pair is connected by a memory cell that is either in the HRS or the LRS depending on the logic value stored in it. The sneak path problem occurs when a memory cell in the HRS surrounded by other memory cells in the LRS is read [1], causing an erroneous reading as illustrated in Fig. 1(a). The sneak current (I_{Sneak}) causes not only reading errors but also unnecessary power consumption, as the current flow through the neighboring memristors, it is added to the element current ($I_{Element}$). Especially, in large size arrays, the sneak current problem becomes more pronounced. Here, the sneak current (I_{Sneak}) should be suppressed as much as possible so that $I_{Element}$ dominates a read current ($I_{Read} = I_{Eelement} + I_{Sneak}$). In a crossbar array, there is at least one memristor, along

a sneak path, through which I_{Sneak} flows enters the bottom electrode (i.e. a memristors under reverse bias: for instance, $M_{i+1,j}$ in Fig. 1(a)). Such resistive switching cells under reverse bias along the sneak current paths can play an important role to minimize overall sneak current by minimizing their reverse current [1, 9-12]; thus, we clearly ananlyze a passive crossbar array to understand resistive switching behaviour that allow current to flow in the forward direction (i.e. direction from the top electrode to the bottom electrode) in LRS and that maintain the resistance in the reverse direction (i.e. direction from the bottom to the top electrode) at the level comparable to that of HRS [1]. When we assume that the array size is N as shown in Fig. 1(b), a miss read error occurs for $N = 3$ in a conventional memristor array because $R_{FL} = R_{RL}$. However, we show that a miss read error is decreased if R_{RL}/R_{FL} ratio, where, it is ratio of reverse low resistance state and forward low resistance state. is larger than 1 in Fig. 1(c) as the published literature in [1].

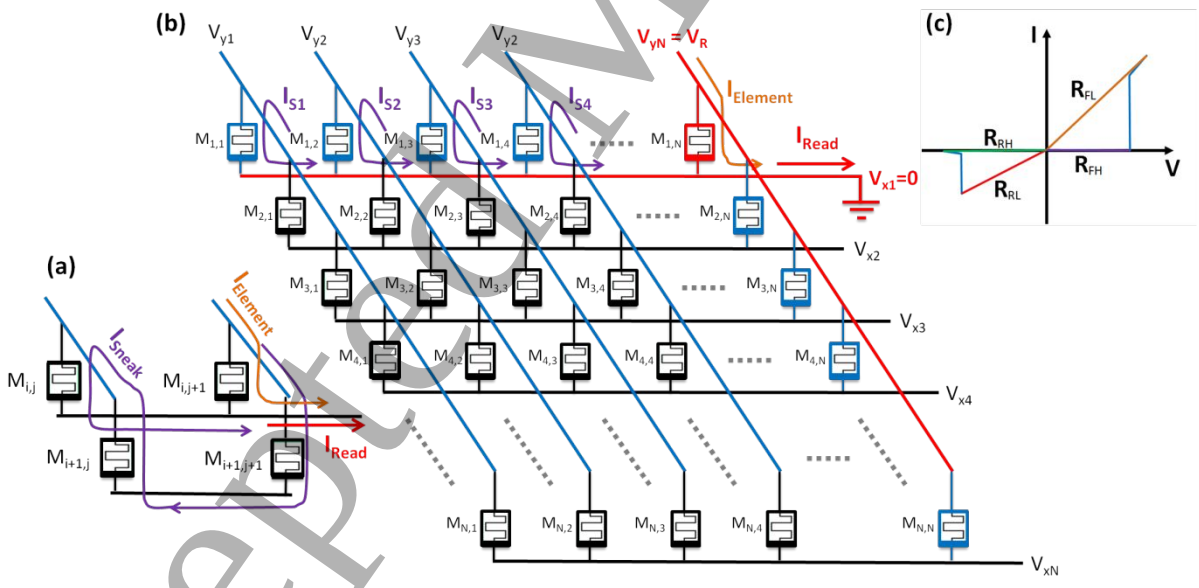

Fig. 1: (a) Sneak currents problem in a passive crossbar array. To begin with, only 2×2 array is shown with one possible sneak path and one desired element. Desired memristor $M_{i,j+1}$ is in the HRS, and all surrounding elements are in the LRS (worst case). A reading voltage is applied across $M_{i,j+1}$, current flows through the addressed element ($I_{Element}$), but the same

voltage is applied the series combination of $M_{i+1,j+1}$, $M_{i+1,j}$, and $M_{i,j}$, because of their LRS state a significant sneak current (I_{Sneak}) flow through them. The sneak current is not distinguishable hence it makes the read current erroneous [1]. (b) Conventional passive crossbar array N×N. (c) I-V curve of a single resistive cell.

2. Read error bound and new design parameter

In general, the published passive crossbar array based on memristors is composed of the structure of memristors sandwiched in between row and column electrode bar as shown in Fig. 1(b). Here, V_{xi} and V_{yi} are node voltages of the row and column bars, respectively, and $M_{i,j}$, (i = 1, 2, ···, N and j = 1, 2, ···, N) are memristors. To analyze the current detection error of one memristor element, the nodal analysis is more convenient, where $M_{1,N}$ is selected for the detection memristor cell. To calculate the read current at $M_{1,N}$, we insert $V_{yN} = V_R$ and $V_{x1} = 0$ (assume connecting ground). From Fig. 1(b), the read current with sneak currents can be calculated as

$$I_{Read} = I_{Element} + I_{Sneak} = I_{Element} + \sum_{i=1}^{N-1} I_{Si} = \frac{V_R}{M_{1,N}} + \sum_{j=1}^{N-1} \frac{V_{yj}}{M_{1,j}} \quad (1)$$

Here, voltage drops $\{V_{yj}\}_{j=1}^{N-1}$ of each column bar can be obtained from the N×N linear equation given by (2). In a summation parts of the sneak currents in (1), $(\sum_{i=1}^{N-1} I_{Si})$, $\{V_{yj}\}_{j=1}^{N-1}$ must be reduced as a sufficient small values due to memritances $\{M_{1,j}\}_{j=1}^{N-1}$ are fixed. Especially, since the red colored terms in (2) are occurred by the sneak currents, the values of the red colored terms must be reduced to avoid the sneak currents coupling, and also the memristance $M_{i,j}$ (i = 2, ···, N and j = 1, 2, ···, N-1) in the red colored terms are always obtained on reverse current flows.

$$\begin{bmatrix} \frac{1}{M_{2,N}}+\sum_{j=1}^{N-1}\frac{1}{M_{2,j}} & 0 & \cdots & 0 & -\frac{1}{M_{2,1}} & -\frac{1}{M_{2,2}} & \cdots & -\frac{1}{M_{2,N-1}} \\ 0 & \frac{1}{M_{3,N}}+\sum_{j=1}^{N-1}\frac{1}{M_{3,j}} & \ddots & \vdots & -\frac{1}{M_{3,1}} & -\frac{1}{M_{3,2}} & \cdots & -\frac{1}{M_{3,N-1}} \\ \vdots & \ddots & \ddots & 0 & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{1}{M_{N,N}}+\sum_{j=1}^{N-1}\frac{1}{M_{N,j}} & -\frac{1}{M_{N,1}} & -\frac{1}{M_{N,2}} & \cdots & -\frac{1}{M_{N,N-1}} \\ -\frac{1}{M_{2,1}} & -\frac{1}{M_{3,1}} & \cdots & -\frac{1}{M_{N,1}} & \frac{1}{M_{1,1}}+\sum_{i=2}^{N-1}\frac{1}{M_{i,1}} & 0 & \cdots & 0 \\ -\frac{1}{M_{2,2}} & -\frac{1}{M_{3,2}} & \cdots & -\frac{1}{M_{N,2}} & 0 & \frac{1}{M_{1,2}}+\sum_{i=2}^{N-1}\frac{1}{M_{i,2}} & \ddots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & 0 \\ -\frac{1}{M_{2,N-1}} & -\frac{1}{M_{3,N-1}} & \cdots & -\frac{1}{M_{N,N-1}} & 0 & \cdots & 0 & \frac{1}{M_{1,N-1}}+\sum_{i=2}^{N-1}\frac{1}{M_{i,N-1}} \end{bmatrix} \begin{bmatrix} V_{x2} \\ V_{x3} \\ \vdots \\ V_{xN} \\ V_{y1} \\ V_{y2} \\ \vdots \\ V_{yN-1} \end{bmatrix}$$

$$= \begin{bmatrix} V_R \\ \frac{M_{2,N}}{V_R} \\ \frac{M_{3,N}}{\vdots} \\ \frac{V_R}{M_{N,N}} \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (2)$$

As current-voltage (I-V) curev shown in Fig. 1(c), we set R_{FH} is the resistances of FHRS (forward high resistance state), R_{FL} is FLRS (forward low resistance state), R_{RH} is RHRS (reverse high resistance state), and R_{RL} is RLRS (reverse low resistance state). Here, V_R is a read voltage. From these variables, we can define the read currents with the sneak currents.

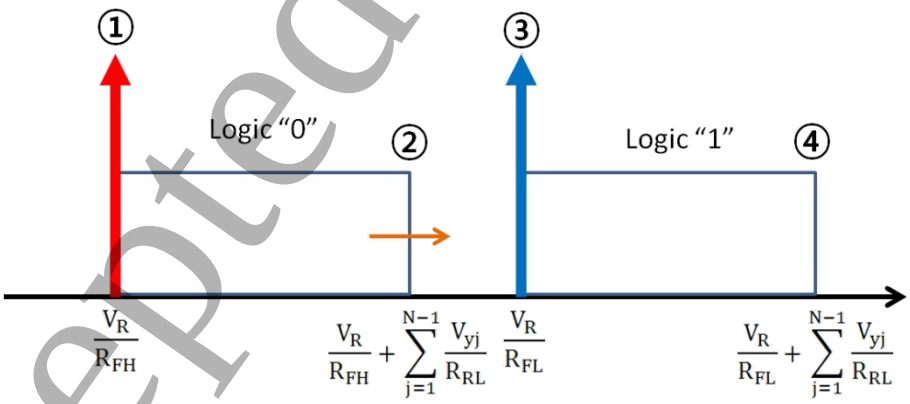

Fig. 2: Read currents for logic "0" and "1".

In Fig. 2, off/on resistance ratio (R_{FH}/R_{FL}) is composed of V_R/R_{FH} for a logic "0" (①) and V_R/R_{FL} for a logic "1" (③), which is important parameter to classify the logic "0" or "1".

Here, as a range between ① and ③ is wider, it is better to detect a logic state. However, the sneak currents are increased by increasing the crossbar array size, and the current values ① and ③ are increased as ② and ④, respectively as shown in Fig. 2. For the reason, a minimum current value for logic "1" is greater than a maximum current value for logic "0". Since all memristors have the same states in the worst case, each current flows on $M_{i,N}$ (i = 2, 3, .., N) are also the same, and each column of $M_{i,j}$ (i = 1, 2, ···, N and j = 1, 2, ···, N) operate a parallel connect per each column. In this case, we assume that $M_{1,N} = R_{FH}$, $M_{1,j}$ (j = 1, 2, .., N-1) and $M_{i,N}$ (i = 2, 3, .., N) are the same that R_{FL} at FLRS, and $M_{i,j}$ (i = 2, ···, N and j = 1, 2, ···, N-1) are R_{RL} at RLRS. Hence, $\{V_{xj}\}_{j=2}^{N}$ are the same value and $\{V_{yj}\}_{j=1}^{N-1}$ are also the same vale. On the conditions in Fig. 2, (1) can be changed as

$$\frac{V_R}{R_{FH}} + \sum_{j=1}^{N-1} \frac{V_R}{R_{FL} + \frac{1}{\sum_{i=1}^{N-1} \frac{1}{R_{RL}}} + R_{FL}} < \frac{V_R}{R_{FL}} \tag{3}$$

$$\frac{1}{R_{FH}} + \frac{N-1}{2R_{FL} + \frac{R_{RL}}{N-1}} < \frac{1}{R_{FL}} \tag{4}$$

In above equation (4), due to $R_{FH} \gg R_{FL}$ and $1/R_{FL} - 1/R_{FH} \approx 1/R_{FL}$, the read error bound can define as

$$N - 1 \leq 2 + \frac{R_{RL}}{(N-1)R_{FL}} \tag{5}$$

Here, sneak current problem is occured if (5) is not satified. Ratio R_{RL}/R_{FL} is a parameter to close at ③ by moving a right way of ②, and we cannot classify a logic state if ② meets at ③ even though off/on resistance ratio has very high value.

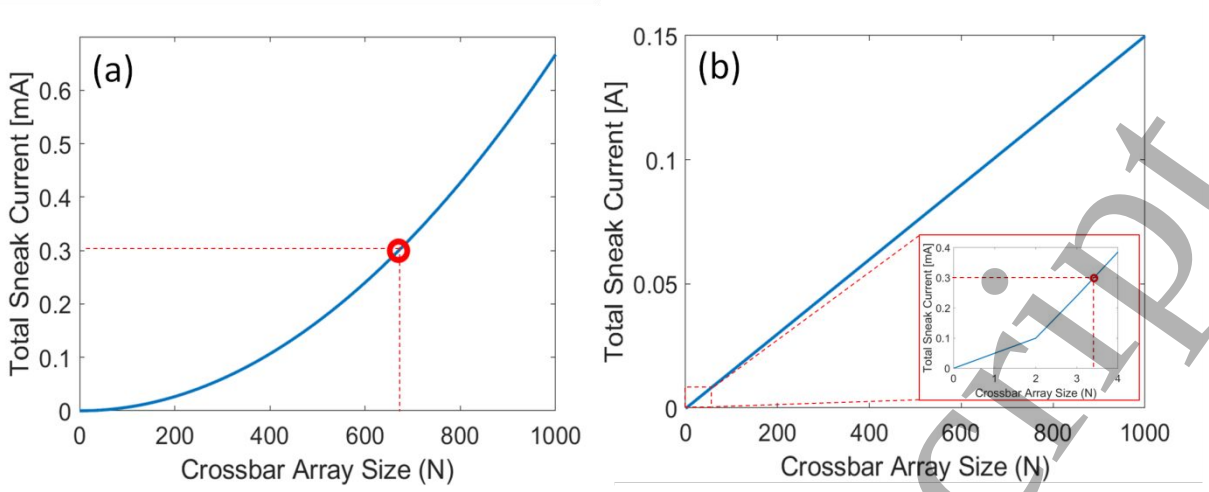

Fig. 3: Variation of the total sneak current ($\sum_{i=1}^{N-1} I_{Si}$) in the cases of the worst situation along memory sizes for (a) the asymmeric memristor proposed in [1] and (b) the conventional memristor. These simultions can get through the supporting Mathlab code (sneak_current_crossbar_array.m).

For example, when it is satified as a conventional memristor, $R_{FL} = R_{RL}$, a read error is occurred over N = 3 due to the condition of (5) is not satisfied. To increase a crossbar array of size (N) without a sneak problem, R_{RL}/R_{FL} ratio should be more increase than 1, and a read error is decreased. To verify the proposed statements, we take a comparison of the device proposed in the literature [1] and a conventional memristor. In the worst case, all memristors except $M_{1,N}$ have only LRS. Hence, we assume that resistances of HRS and LRS for a conventional memristor are 3 GΩ and 10 kΩ, respectively, and R_{FH}, R_{FL}, R_{RH}, and R_{RL} for the asymmeric memristor proposed in [1] are 3 GΩ, 10 kΩ, 5.3 GΩ, and 4.47 GΩ, respectively, that is, $V_R = 3$, $M_{1,N} = R_H = 3$ GΩ, $M_{1,j}$ (j = 1, 2, .., N-1) and $M_{i,N}$ (i = 2, 3, .., N) are the same that R_{FL} = 10 kΩ at FLRS, and $M_{i,j}$ (i = 2, ⋯, N and j = 1, 2, ⋯, N-1) are R_{RL} = 4.47 GΩ at RLRS. As shown in Fig. 3(a), the simulation result shows the variation of the total sneak currents in the cases of worst situation along memory sizes, which describes that the proposed memristor function in [1] protects up to N = 670 size, whereas the conventional memristor function is occurred the severe read error over N = 3 size as shown in Fig. 3(a), due to the sneak current problem is ocuured if the total sneak current ($(\sum_{i=1}^{N-1} I_{Si})$) is over the V_R/R_{FL} = 0.3 mA. Here, we can see that it is over 3 mA in between 3×3 and 4×4 array sizes as inset shown in Fig. 3(b). However, if the memristors ($M_{i,j}$, where, i = 2, 3, .., N and j = 1, 2, .., N-1) have different states of LRS or HRS, the sneak current is lower than the one on the worst case,

and we can easily take a simuation using the supporting Mathlab code (sneak_current_crossbar_array_random_case.m).

In the case of a writing cycle, it is not a problem because of a small voltage drop on a sneak current path even though it operates the asymetric memristor function if all memristors are uniformly fabricated. In non-uniform fabrication, due to a small voltage drop on a sneak current path cannot make down to switch voltage for a HRS it has a little bit miss writing problem in the case of small size. However, the case of the memory size to avoid a miss writing error is also not occurred due to voltage drops is sufficiently distributed. From the paper, we can define that overall sneak current is minimized when R_{RL}/R_{FL} in (5) is maximaized. Therefore, the resistance ratio, HRS/LRS (R_{FH}/R_{FL}), used in all literature is very important for the performance of the memristor, but the sneak current dominantly depends on the proposed ratio, R_{RL}/R_{FL}. The paper recommends that the researchers have to consider this ratio in passive crossbar resistive switching arrays.

3. Conclusion

From analytical ananlysis results, we have clearly discribed that such resistive switches under reverse bias along the sneak current paths can play an important role to minimize overall sneak current by blocking their reverse current by using the asymmeric memristor. We have defined the read error bound in (5) to find significantly reduced cause the problematic sneak current of a passive crossbar resistive memory array, and also demonstrated that the sneak current can be minimized when the new ratio (R_{RL}/R_{FL}) is maximaized. In the sumulation results as shown in Fig. 3, the asymmeric memristor protected without the sneak currents up to N = 670 size, whereas the severe read error was occurred over N = 3 size in the conventional memristor function. Although the researchers have considered design parameters such as off/on resistance ratio, retension time, and switching voltage for a resistive switching, but we are sure that the proposed R_{RL}/R_{FL} ratio is also considered for a design specification of the sneak current problem.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (NRF-2016R1A2B4015627).

References

[1] Ali S, Bae J, Lee C H, Kobayashi N P, Shin S and Ali A 2018 Resistive switching device with highly asymmetric current–voltage characteristics: a solution to backward sneak current in passive crossbar arrays Nanotechnol. **29** 455201

[2] Waldrop M M 2016 The chips are down for Moore's Law Nature **530** 144-7

[3] Moore G E 1988 Cramming more components onto integrated circuits Proc. IEEE **86** 82-5

[4] Strukov D B, Snider G S, Stewart D R and Williams R S 2008 The missing memristor found Nature **453** 80-3

[5] Chua L 1971 Memristor-the missing circuit element IEEE Trans. Circuit Theory **18** 507-19

[6] Heath J R, Kuekes P J, Snider G S and Williams R S 1998 A defect-tolerant computer architecture: opportunities for nanotechnology Science **280** 1716-21

[7] Kuekes P J, Stewart D R and Williams R S 2005 The crossbar latch: logic value storage, restoration, and inversion in crossbar circuits J. Appl. Phys. **97** 034301

[8] Duygu K, Shimeng Y and Wong H S P 2013 Synaptic electronics: materials, devices and applications Nanotechnol. **24** 382001

[9] Chang T C, Chang K C, Tsai T M, Chu T J and Sze S M 2016 Resistance random access memory, Mater. Today **19** 254-64

[10] Cho B, Kim T W, Song S, Ji Y, Jo M, Hwang H, Jung G Y and Lee T 2010 Rewritable Switching of one diode–one resistor nonvolatile organic memory devices Adv. Mater. **22** 1228-32

[11] Ventra M D and Pershin Y V 2011 Memory materials: a unifying description Mater. Today **14** 584-91

[12] Linn E, Rosezin R, Kugeler C and Waser R 2010 Complementary resistive switches for passive nanocrossbar memories Nat. Mater. **9** 403-6