Device design-enabled Schottky barrier height extraction for nanoFETs based on the 1D Landauer-Büttiker equation

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A Schottky barrier height extraction method for one dimensional nanoFETs based on the Landauer-Büttiker equation and a transistor architecture with a displaced gate is presented. In contrast to the conventional activation energy method developed for 3D material interfaces, the proposed extraction method eases the identification of the flat-band voltage and thus the Schottky barrier height. The methodology is applied to simulation data of single-tube carbon nanotube field-effect transistors feasible for manufacturing and to experimental data of nanoFETs. In both cases, the results with the proposed methodology turn out to be closer to the reference values than the ones obtained with the conventional method. *Published by AIP Publishing*. https://doi.org/10.1063/1.4998807

The Schottky barrier height (Φ_{SB}) is a typical parameter to quantify the quality of a semiconductor-metal interface, especially for material combinations that are weakly affected by Fermi level pinning such as specific metal-carbon nanotube (CNT) interfaces in CNT-based field-effect transistors (CNTFETs),[1] certain metal-InP/InGaAs interfaces,[2,3] and special metal-2D material interfaces.[4] Typically, based on the extracted value for the barrier height, decisions for further technology development and improvement are made. Furthermore, the characterization of this key parameter is critical since it could aid to validate sophisticated physics-based models of nanoFETs. A reliable extraction method of Φ_{SB} is therefore essential.

A widely known Φ_{SB} extraction method related to current-voltage characteristics at different temperatures is the activation energy method (AEM)[5] which assumes the thermionic emission of carriers over a potential barrier in a Schottky diode. In AEM, the parameter Φ_{SB} is extracted at a flat-band voltage V_{FB}. The latter is quite often challenging to identify especially for materials with a low effective mass, such as CNTs and various III/V compounds.

AEM has been applied to nanoscale electronic devices such as CNTFETs.[6–10] However, the conventional AEM assumes a metal interface with a 3D material channel. For interfaces involving 1D channels, such as a CNT or a CNT array, alternative rigorous methodologies are required to extract Φ_{SB}. While AEM has been adapted to 1D by modifying the Schottky diode equation,[11] no further comparison with 3D AEM has been provided. A more straightforward expression for 1D channels such as the 1D Landauer-Büttiker equation has not been used so far for Φ_{SB} extraction in nanoFETs.

In this work, Φ_{SB} is extracted following a methodology based on the 1D Landauer-Büttiker equation. The results are then compared to data obtained with 3D AEM. Additionally, the identification of V_{FB} is eased by a non-symmetric gate test structure. The proposed method is applied to data of quasi-ballistic devices with different 1D transport channels such as single-tube (ST) CNTFETs and single-nanowire (NW) FETs.

The electron current in quasi-ballistic devices can be related to the electron transmission probability by the Landauer-Büttiker equation,[12] which can be simplified in various ways according to bias regions and transport regimes. A simplified Landauer-Büttiker equation describing the quasi-ballistic transport considering only the first subband for pure thermionic electron current in the subthreshold regime can be expressed as[13]

$$I_{th}^{sub} = \frac{4q^2}{h} V_t \mathcal{T}_{th,eff} \left[\ln\left(1+\zeta_{cc}(E_{F,S})\right) - \ln\left(1+\zeta_{cc}(E_{F,D})\right)\right], \tag{1}$$

where $V_t = k_B T q^{-1}$ is the thermal voltage, k_B the Boltzmann constant, q the electronic charge, T the temperature, $\mathcal{T}_{th,eff}$ an effective thermionic transmission probability, and $E_{F,S(D)}$ the source (drain) Fermi energy level, and the function ζ_{cc} is given by $\zeta_{cc}(E) = \exp\left[-(E_{cc}-E)(k_B T)^{-1}\right]$, where $E_{cc} = q\left[\Phi_{BH} - n_{q,g}(V_{GS}-V_{FB}) - n_{q,d}V_{DS}\right]$ is the current control energy defined as the minimum energy for which the transmission through the device is not zero. Typically, the current control energy point is associated with the minimum of the conduction band. If $E_{cc} - E \gtrsim 3k_B T$, a Taylor series expansion leads to $\ln(1+\zeta_{cc}) \approx \zeta_{cc}$. Thus, by replacing terms, Eq. (1) can be written as

$$I_{th}^{sub} \approx \frac{4q^2}{h} V_t \mathcal{T}_{th,eff} \exp\left[\frac{n_{q,g}}{V_t}(V_{GS}-V_{FB}) - \frac{\Phi_{BH}}{V_t} - \frac{n_{q,d}}{V_t}V_{DS}\right], \tag{2}$$

where $n_{q,g}$ and $n_{q,d}$ are the gate and drain coupling coefficients, V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltage, respectively, and Φ_{BH} is the potential barrier height. A similar expression can be derived for the hole current.

In the following analysis, $\mathcal{T}_{th,eff}$ is considered approximately equal to 1, a true condition for quasi-ballistic devices.

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Additionally, a weak dependence on temperature and bias of $n_{q,g}$ is expected due to the negligible charge carrier density along the channel in the subthreshold region. While $n_{q,g}$ can be calculated from the subthreshold slope with Eq. (2), its actual value does not affect the extraction technique. An electrostatic coupling between the drain contact and the channel might leads to drain-induced barrier lowering (DIBL), which shifts the transfer curve along the V_{GS} axis while changing V_{DS}. This phenomenon is captured by $n_{q,d}$.

From Eq. (2), an Arrhenius plot of $\ln(I_{th}^{sub}T^{-1})$ over T^{-1} is obtained for different V_{GS} in the subthreshold region at each V_{DS} [see Fig. 2(b)]. The slope of these curves is then calculated and plotted over V_{DS} at the corresponding V_{GS} [see inset in Fig. 2(b)] from which $n_{q,d}$ can be determined, in contrast to AEM where this calculation is not possible. The potential barrier height at each V_{GS} is obtained from the point at which the linear extrapolation of these curves crosses the y-axis. (The last step could be skipped for $n_{q,d} = 0$.) A plot showing the V_{GS}-dependence of Φ_{BH} is obtained from these data [see Fig. 2(c)]. As long as the current is purely thermionic, Φ_{BH} depends linearly on V_{GS}. The onset of tunneling current for increasing V_{GS} leads to a deviation from this linear dependence.[6,14] The voltage that marks this onset is called flat-band voltage V_{FB}, and the Schottky barrier height Φ_{SB} is identified with Φ_{BH} at this bias point.

Notice that while the methodology resembles AEM, the 1D Landauer-Büttiker-equation-based method (1D LBM) presented here, which uses Eq. (2) for extracting the parameters, better fits the transport physics in 1D nanoFETs than the conventional[5] or modified[11] Schottky diode equation employed in AEM. The extraction method is also valid for p-type devices by considering the hole current equation equivalent to Eq. (2).

In general, the identification of V_{FB} could be challenging due to multiple apparent linear regions and noisy experimental data. Therefore, a test structure for an accurate identification of the flat-band voltage and related Schottky barrier height is proposed.

However, it should be emphasized that both AEM and 1D LBM fail in extracting accurate barrier heights for $\Phi_{SB} \lesssim 3k_BT/q$ in nanoFETs due to the involved Boltzmann approximation for the energetic carrier distribution. Alternatively, contact resistance extraction methods[15] could be employed for the characterization of the contact quality.

Numerical device simulations (NDSs) of an n-type ST buried-gate (BG) CNTFET with a (23,0) CNT have been performed using a simulator discussed elsewhere.[16] In comparison to other feasible device architectures, BG CNTFETs have a higher performance associated with a better gate control over the channel.[17–19] Although more complex fabrication steps are involved, promising experimental data for BG CNTFETs have already been reported.[19–21] A cross section of the simulated device is shown in Fig. 1. The channel L_{ch} and gate length L_g of the device are 200 nm and 180 nm, respectively. The spacer lengths at the source $L_{sp,s}$ and drain $L_{sp,d}$ sides are identical and equal to 10 nm, i.e., a symmetric gate is considered. The high-κ oxide has a thickness t_{ox} of 15 nm and a permittivity of 16. The length $L_{s/d}$ and height $h_{s/d}$ of the source and drain contacts are 50 nm and 100 nm, respectively, while the gate height h_g is 200 nm. The CNT

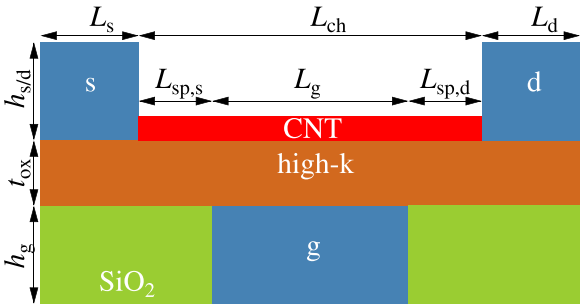

FIG. 1. Cross section of the simulated symmetric ST BG CNTFET.

with a diameter of 1.8 nm is located exactly at the middle of the device width of 20 nm.

The device is simulated with a reference Schottky barrier height $\Phi_{SB,ref}$ equal to 0.2 eV at T varying from 200 K to 500 K in steps of 50 K. The bias voltages have been set as V_{GS} varying from −0.1 V to 1 V and eight V_{DS} from 0.1 V to 2 V. Tunneling mechanisms are enabled unless stated otherwise. The transfer characteristics at 300 K and 500 K are shown in Fig. 2(a), while the Arrhenius plot and the calculated slopes for this data are shown in Fig. 2(b). The weak V_{DS}-dependence of these slopes gives an $n_{q,d}$ close to zero. The conduction band profile of this device is shown in Fig. 2(e) at three representative V_{GS}, while Fig. 2(f) shows the weak temperature and bias dependences of $n_{q,g}$.

The $\Phi_{BH}(V_{GS})$ plot obtained from the simulations of the same device with and without tunneling enabled is shown in Fig. 2(c). As a guide for the following analysis, the plot is split into two regions by the reference flat-band voltage $V_{FB,ref}$. Region (i) corresponds to the subthreshold region and region (ii) to the linear region.

In region (i), only thermionic emission from the source contact is possible, so the Φ_{BH} curves [in Fig. 2(c)] with and without tunneling enabled in the simulation have a similar linear V_{GS} dependence. At $V_{GS} \approx V_{FB,ref}$, the conduction band close to the source is almost flat and at the same energy as $\Phi_{SB,ref}$ [Fig. 2(e)].

For $V_{GS} > V_{FB,ref}$, i.e., in region (ii), the conduction band forms a tunneling barrier near the source contact. With disabled tunneling in the simulations, the Φ_{BH} dependence abruptly changes its quasi-linear behaviour in region (ii), leading to an extracted $\Phi_{SB,tun.off}$ close to the reference value as shown in Fig. 2(c). If tunneling is enabled in the simulations, a second apparent linear region, in the V_{GS} dependence of Φ_{BH}, can mislead the extraction as shown by the square marker in Fig. 2(c). Therefore, the identification of V_{FB} and the corresponding Φ_{SB} are expected to be less challenging when the tunneling mechanisms are suppressed or at least diminished. The extracted flat-band voltages, obtained with linear extrapolation [steepest dotted line in Fig. 2(c)], indicate approximated values for the validity limit of Eq. (2).

Additionally, the Φ_{BH} dependence obtained with 3D AEM is shown in Fig. 2(d). Due to the quadratic dependence on the temperature, which is still under discussion for 1D nanoFETs, 3D AEM underestimates the potential barrier height, and therefore, false Φ_{SB} and V_{FB} are obtained in contrast to the extracted values using 1D LBM, which are closer to the reference values. This is confirmed by comparing Φ_{SB}

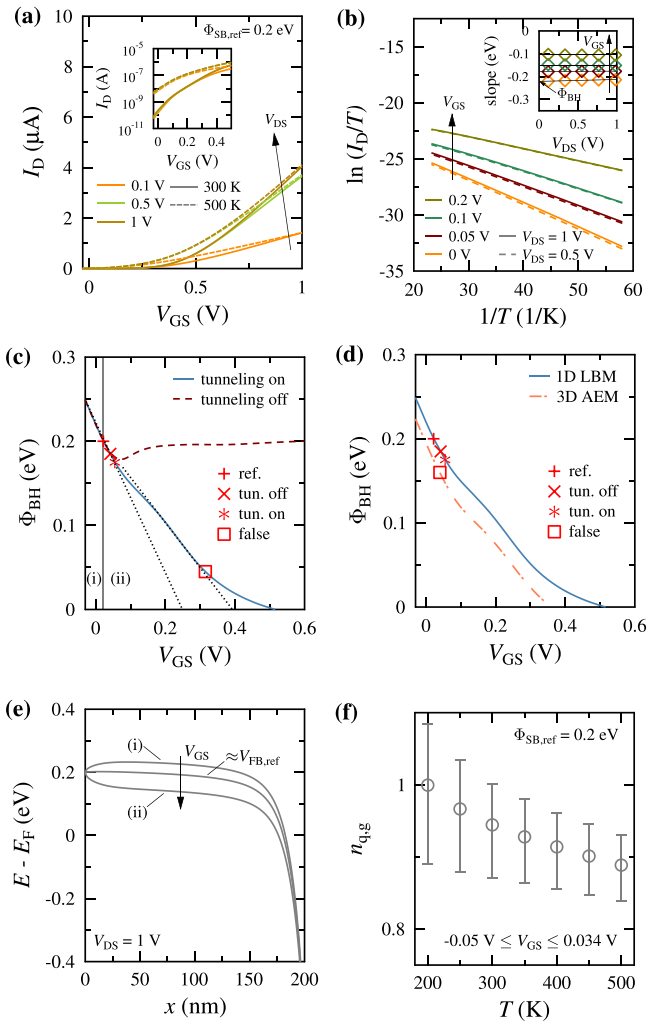

FIG. 2. Simulation data for a symmetric ST BG CNTFET. (a) Transfer characteristics for different V_{DS} at two temperatures. (b) Arrhenius plot and its calculated slope (inset) in the subthreshold bias region. (c) Potential barrier height over V_{GS} obtained from simulations with tunneling enabled (solid line) and disabled (dashed line). Markers represent the points at which (V_{FB}, Φ_{SB}) is extracted for the different simulation data. (d) Comparison of the V_{GS}-dependence of Φ_{BH} obtained with 3D AEM and 1D LBM. (e) Conduction band profile and (f) temperature and bias dependences of $n_{q,g}$.

extracted with 1D AEM and 3D AEM in Fig. 3(a) from similar NDS setups as described above but different $\Phi_{SB,ref}$. Notice that both methods fail for $\Phi_{SB,ref} \lesssim 3k_BT/q$.

1D LBM has been applied to experimental data of fabricated n- and p-type global-back-gate (GBG) ST CNTFETs[6–8] and of an n-type top-gate (TG) Ge NWFET[22] with different contact materials. A weak dependence on temperature and bias of $n_{q,g}$ for all the devices has been verified. Figure 3(b) compares the extracted $\Phi_{SB,1DLBM}$ with the values reported in the literature for these devices which are obtained with 3D AEM. The latter explains the underestimation of $\Phi_{SB,3DAEM}$ compared to the values extracted with 1D LBM.

Figure 3(a) also shows extracted barrier heights from synthetic data obtained by NDSs.[25,26] The input parameters including the barrier height had been calibrated to experimental data of a p-type BG ST CNTFET[23] ($\Phi_{SB,ref}$ = 0.150 eV) and of a Si NWFET[24] ($\Phi_{SB,ref}$ = 0.580 eV). The same barrier height has been used in a physics-based compact model reproducing the BG CNTFET characteristics.[27] While the extracted values

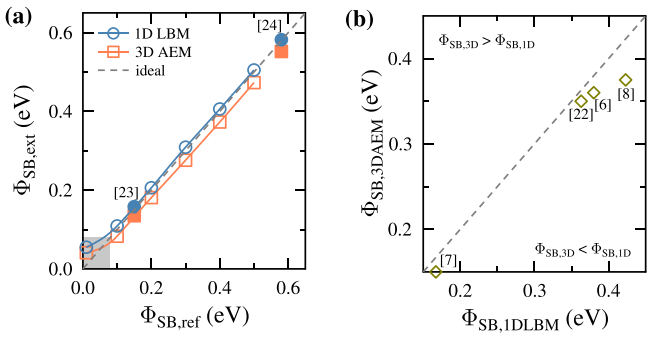

FIG. 3. Comparison of Φ_{SB} extracted with 1D LBM and 3D AEM from (a) synthetic and (b) experimental data.[6–8,22] The dashed line shows the ideal values. The shaded region indicates $\Phi_{SB} \lesssim 3k_BT/q$. Filled markers correspond to extracted values from experimental-based[23,24] synthetic data.[25,26]

based on 1D LBM are very close to the values used in the calibrated NDSs, the 3D AEM is with 0.135 eV for the CNTFET and 0.552 eV for the NWFET far away.

In order to ease the extraction of Schottky barrier heights, a test structure is proposed, which diminishes the impact of tunneling on the extraction of the barrier height by changing the device electrostatics[17–21,25,28,29] close to the injecting contact. A non-symmetric gate architecture, shown in Fig. 4, is proposed. The buried-gate contact is moved as far away from the source contact as possible in order to reduce the electrostatic control of the gate on the Schottky barrier.[29] This will enlarge the barrier width, thus preventing electrons to tunnel through the barrier. The same effect can be exploited in top-gate architectures which are less challenging to fabricate.

Simulations of symmetric and non-symmetric ST BG CNTFETs with an L_{ch} of 260 nm have been performed at the same temperature and bias conditions described in the previous simulation study. The gate contact in the symmetric structure is centered, so $L_{sp,s} = 0.5L_{sp} = 40$ nm, while in the non-symmetric gate structure, the gate contact is moved away from the source contact such as $L_{sp,s} = L_{sp} = 80$ nm. Other parameters are the same as in the initial device structure (Fig. 1). $\Phi_{SB,ref}$ is set to 0.2 eV in the simulations, while flat-band conditions are approximately obtained at $V_{GS} = 0.034$ V.

The transfer characteristics of the simulated devices are shown in Fig. 5(a) at 300 K where it can be noticed that as the distance between the source and gate contacts increases, the current decreases due to a diminished tunneling current. Figures 5(c) and 5(d) show the conduction band profiles at three representative V_{GS} and the weak temperature and bias dependences of $n_{q,g}$ for the BG devices. At $V_{GS} \leq V_{FB} = 0.034$ V,

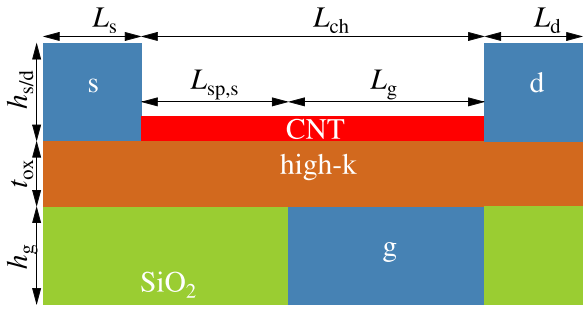

FIG. 4. Cross section of the simulated non-symmetric ST BG CNTFET.

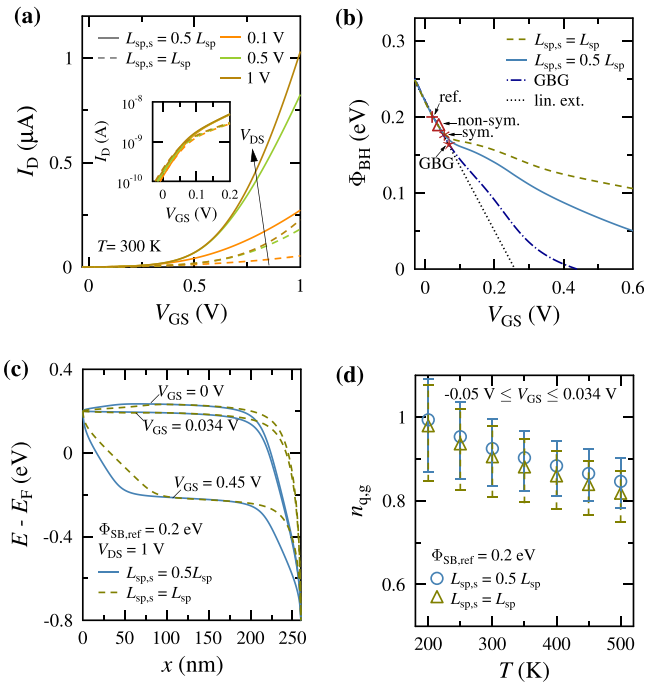

FIG. 5. Simulation data for symmetric and non-symmetric ST BG CNTFETs with $L_{ch} = 260$ nm and $L_g = 180$ nm. (a) Transfer characteristics for different V_{DS}. (b) Potential barrier height over V_{GS} obtained for each of these devices and a GBG structure. The linear extrapolation for extraction is represented by the dotted line. The markers represent the point (V_{FB}, Φ_{SB}) at which these values are extracted for each simulated device. (c) Conduction band profiles and (d) temperature and bias dependences of $n_{q,g}$ of the BG devices.

both devices operate with pure thermionic current. At voltages larger than V_{FB}, e.g., at $V_{GS} = 0.45$ V, thermionic-assisted-by-tunneling current flows through the channel of both devices; however, the thicker potential barrier at the source side [see Fig. 5(c)] induced by the non-symmetric gate decreases the tunneling current in this device. The device allowing less tunneling current, i.e., the non-symmetric structure, is also the device with the more pronounced turning point in the $\Phi_{BH}(V_{GS})$ plot as shown in Fig. 5(b). Results from a simulated GBG device with similar physical characteristics as the BG devices but with a gate length equal to the channel length are also included for comparison purposes. The different extracted V_{FB} are identified in this plot as the voltage at which the corresponding curve deviates from a linear extrapolation [dotted line in Fig. 5(b)] with a relative error ≈0.5%.

In contrast to the other extracted values, the Φ_{SB} values of 0.188 eV and V_{FB} of 0.038 V extracted from the curve of the non-symmetric structure are the closest to both reference values. This is due to the lower tunneling current translated into a larger deviation from the linear extrapolation of the curve obtained with this device.

By exchanging the source and drain contacts in the architecture shown here, the same test structure can be used for high RF performance[18] without the need to fabricate special test structures for the Schottky barrier height extraction.

The Landauer-Büttiker equation for quasi-ballistic devices has been considered for the extraction of Schottky barrier heights. The reliability of the extraction method, named here 1D LBM, has been shown for synthetic and experimental data of nanoFETs with different gate architectures and channel materials. Moreover, a FET test structure with a displaced gate has been suggested, which significantly improves the accuracy of the barrier height extraction in conjunction with the 1D LBM in contrast to the conventional 3D AEM. In addition, the expected affordability of the fabrication of buried- or top-gate test structures makes this extraction method plausible to be applied. The accuracy improvement obtained with this extraction method is crucial for the technology development of nanoFETs and for the verification of more sophisticated models.

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