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Microcrystalline silicon solar cells with passivated interfaces for high open-circuit voltage

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We introduce passivating hetero-interfaces in single-junction microcrystalline silicon (μc-Si:H) solar cells. We investigate the effect of different i–n layer stacks in thin μc-Si:H devices, in which recombination is significant at the interfaces as well as in the bulk material. By applying amorphous silicon passivating layers at the μc-Si:H i–n interface, we show a device with a high open-circuit voltage (V_{oc}) of 608 mV, for a standard Raman crystalline fraction of the i-layer (>50%). This V_{oc} is the highest reported value for a state-of-the-art μc-Si:H device made by plasma-enhanced chemical vapor deposition. We also report an efficiency of 9.45% for a solar cell with an absorber layer as thin as 650 nm on an area greater than 1 cm^2, and show with a simple crystalline silicon model that for such thin μc-Si:H devices or μc-Si:H devices with a very high bulk-material quality, well-mastered interfaces and doped layers are of paramount importance for high efficiency.

1 Introduction State-of-the-art single-junction microcrystalline silicon (μc-Si:H) solar cells deposited by plasma-enhanced chemical vapor deposition (PECVD) generally exhibit open-circuit voltages (V_{oc}) values in the 500–560 mV range. These numbers are far below the theoretical upper limit of above 800 mV that can be expected from the μc-Si:H bandgap (1.1 eV) [1]. To improve V_{oc}, attention has lately been focused on developing both high-quality μc-Si:H material and a suitable cell design [2–8]. One way to increase the V_{oc} of μc-Si:H solar cells is to increase the amorphous fraction of the absorber layer, but the subsequent gain is generally accompanied by an increased light-induced degradation and a loss in fill factor (FF) due to less efficient carrier collection [9–13]. Recently, promising results have also been obtained with alternative precursors and deposition conditions, yielding high V_{oc} values even with a large crystalline fraction in the absorber layer [14, 15]. V_{oc} is sensitive to absorber layer material and quality, but also to interfaces [16]. For example, the use of silicon suboxide (SiO_x) for the buffer and doped layers has been shown to boost the efficiency of thin-film silicon solar cells [17–19]; a higher resilience of the efficiency on challenging superstrates and improved transparency in the short-wavelength range of the solar spectrum were demonstrated [20, 21]. A high V_{oc} value of 603 mV was also reported by introducing buffer layers grown by hot-wire chemical vapor deposition at the p–i interface. The absence of ion bombardment on the p–i interface was suggested as the cause of this high value [22].

In this paper, we investigate the interplay between the thickness of the μc-Si:H absorber layer and the thickness of an amorphous silicon (a-Si:H) buffer layer applied at the μc-Si:H i–n interface. We use this buffer layer as a tool to probe the influence of the interfaces and the bulk on the V_{oc} of thin single-junction μc-Si:H solar cells. In particular, we show that applying thin intrinsic and n-doped a-Si:H layers at the μc-Si:H i–n interface in thin devices improves V_{oc} to a value above 600 mV, reaching a value close to that of

standard multicrystalline silicon solar cells. The followed approach is similar to the amorphous/crystalline silicon heterojunction concept, where passivation of the crystalline surface drastically enhances V_{oc}, compared to traditional diffused-junction cells [23].

2 Experimental The solar cell design we used was based on the one of our independently-verified record device [24], incorporating high-quality bulk material and an SiO_x buffer layer at the p–i interface [19]. The p-doped layer (SiO_x) was identical in all cases [21]. A 5-μm-thick boron-doped zinc oxide (Z5) layer deposited by low-pressure chemical vapor deposition (LPCVD-ZnO) was used as the front electrode. To obtain smooth surfaces favorable to the growth of high-quality μc-Si:H, an argon-based plasma treatment was applied to the LPCVD-ZnO before the deposition of the silicon layers. Short treatment times (typically below 20 min) correspond to a rough surface of the front electrode and low-quality μc-Si:H, whereas longer treatment times increase the bulk quality of the μc-Si:H absorber layer by reducing the zones of defective and porous material [17]. As illustrated in Fig. 1, μc-Si:H absorber layers with thicknesses ranging from 0.4 to 2.5 μm were deposited by PECVD using silane diluted in hydrogen in a dual-chamber small-area research system, at an excitation frequency of 70 MHz, a pressure of 0.7 mbar and a temperature of 200 °C [7].

A constant and low power was used to obtain a deposition rate of around 1.5 Å/s. The silane-to-hydrogen ratio was varied (by adjusting the silane flow) during the early stages of the growth of the absorber layer (from about 4 to 5% with three steps), to ensure a fast microcrystalline nucleation and a high crystalline fraction. The Raman crystalline fraction (R_c) of the absorber layer was thus kept high, above 50% in all cases, as measured through the p-doped side of the cell. An R_c profile of a cell fabricated with similar deposition conditions can be found in Ref. [25].

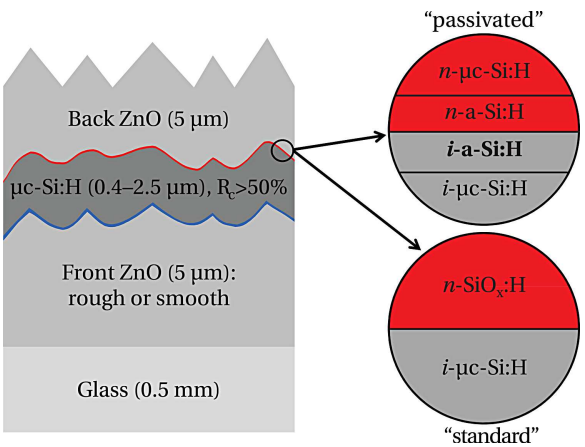

Figure 1 Cross-sectional schematic of our device. Two front-electrode roughnesses and two cell designs with various i–n interfaces are investigated: a standard SiO_x n-doped layer ("standard") and a passivated design with a-Si:H layers ("passivated").

First, two designs for the i–n interface were compared, as shown in Fig. 1, for solar cells with a 650-nm-thick absorber layer. One design utilizes a single SiO_x n-doped layer ("standard"); in the other a passivated interface was introduced, which consisted of a stack comprising a 20-nm-thick intrinsic a-Si:H buffer layer and an a-Si:H n-doped layer ("passivated"). The intrinsic a-Si:H buffer layer was deposited with silane and hydrogen in the same chamber than the absorber layer, with a silane content of 50% of the total gas mixture, at the same temperature (200 °C). In the passivated design, a thin μc-Si:H n-doped layer was used to ensure good contact with the back electrode. We also investigated the configuration using an n-doped SiO_x layer instead of an n-doped μc-Si:H layer in the passivated design, but poor FF was obtained, probably due to the non-optimized n-a-Si:H –n-SiO_x interface. We therefore stuck to the comparison of our standard i–n interface design for single-junction μc-Si:H solar cells (namely using SiO_x), and the passivated design. As a second step, the interplay of the thicknesses of the intrinsic μc-Si:H absorber layer and the a-Si:H buffer layer was evaluated.

Unless otherwise stated, a 5-μm-thick LPCVD-ZnO back electrode was used and cells with a nominal area of 0.25 cm^2 (default area) or 1.2 cm^2 were patterned by lift-off of the back electrode between the cells. Access to the front electrode was provided via dry etching of the silicon between the cells. A dual-lamp sun simulator was used for the measurements of the *J–V* curves of solar cells, operating under standard conditions (AM1.5 g, 1000 W/m^2, 25 °C). From these measurements, V_{oc} and FF were deduced. For variable illuminations measurements, grey filter were used during the *J–V* measurement [26]. For the small cells (0.25 cm^2), the short-circuit density (J_{sc}) was calculated from external quantum efficiency (EQE) measurement, performed with a white dielectric back reflector. This calculated J_{sc} was used for determining the conversion efficiency (η). For the larger cells (1.2 cm^2), J_{sc} and η were deduced from the *J–V* measurements, performed with a white dielectric back reflector and a dark mask which defined the area of the device (1.06 cm^2). The area of the mask was made slightly smaller than the cell nominal area to avoid lateral collection of light which could artificially increase light collection. Unless otherwise stated, no anti-reflective coating (ARC) was used at the air–glass interface.

3 Results and discussion Table 1 shows the performance of solar cells with a 650-nm-thick absorber layer for the two cell designs of Fig. 1 as a function of superstrate roughness. For such thin devices, the impact of the bulk defect density in the intrinsic absorber layer is reduced so that recombination at the interfaces plays a major role in V_{oc}.

State-of-the-art efficiencies are obtained on all superstrates with both the standard and passivated designs. In both cases, V_{oc} and FF on very smooth (Z5 150') and smooth (Z5 45') superstrates are similar, indicating that the absorber layer contains almost no zones of porous and

Table 1 Performance of thin p–i–n μc-Si:H solar cells with a 650-nm-thick absorber layer and two i–n-interface designs, as a function of the argon plasma treatment of the front electrode (from very smooth for the Z5 150' to rough for the Z5 20').

design	Z5 treatment time	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm^2]	η [%]	n [−]
"standard"	150' (very smooth)	589	78.0	16.3	7.5	1.1
	45' (smooth)	582	77.4	20.0	9.0	1.1
	20' (rough)	576	75.4	20.4	8.9	1.2
"passivated"	150' (very smooth)	606	76.6	16.1	7.5	1.1
	45' (smooth)	608	77.1	19.7	9.2	1.2
	20' (rough)	571	72.5	20.2	8.4	1.5

defective material ("cracks") when grown on such superstrates. Still, although both cell designs yield similar efficiencies, a notably larger V_{oc} value is obtained for the passivated design. A V_{oc} gain of 26 mV with minor FF loss is reached on the smooth superstrates. However, on the rough superstrate, even though V_{oc} remains rather stable, FF is reduced compared to the standard design, due to less efficient shunt quenching in the passivated design.

Figure 2(a) presents the V_{oc} values of four of the cells in Table 1 measured under variable illumination. From these measurements, the diode ideality factor (n) can be extracted by fitting the V_{oc} vs. illumination data with a one-diode model [26, 7].

For the smooth superstrate, the slope of V_{oc} as a function of illumination, and hence the diode ideality factor, is independent of the i–n interface design. On the contrary, for the rough superstrate, shunt quenching is more efficient with the standard design (with a SiO_x n-doped layer), for a similar initial V_{oc}. This result shows that a high-quality absorber layer with no or few zones of defective and porous material is mandatory to obtain, and maintain at lower illumination, a gain with the passivated design. This is relevant for multi-junction solar cells in the p–i–n configuration, since in that case the μc-Si:H sub-cell is usually grown on a highly textured superstrate and it gets only half or less (for more than two junctions) of the illumination as compared to the single-junction configuration. J–V and EQE curves of the best device of Table 1, which was obtained with the passivated design on Z5 45', are shown in Fig. 2(b).

Table 2 shows the electrical properties of a solar cell with a 650-nm-thick absorber layer and a passivated design, which was co-deposited with the solar cells presented in Table 1, on a smooth Z5 45' superstrate, with and without a textured ARC applied at the air-glass interface of the same cell. This ARC consists of random pyramids which provide very effective geometrical light-trapping [27].

Whereas V_{oc} and FF remain almost unchanged when applying a textured ARC (both around 600 mV and 73%). A boost in J_{sc} of 1.2 mA/cm^2 is obtained with the textured ARC, increasing η from 8.89 to 9.45%.

Figure 3 shows V_{oc} and FF as a function of the thickness of both the intrinsic μc-Si:H absorber layer and the intrinsic a-Si:H buffer layer for two superstrate roughnesses, in the passivated design. For these cells, a 2.5-μm-thick LPCVD-

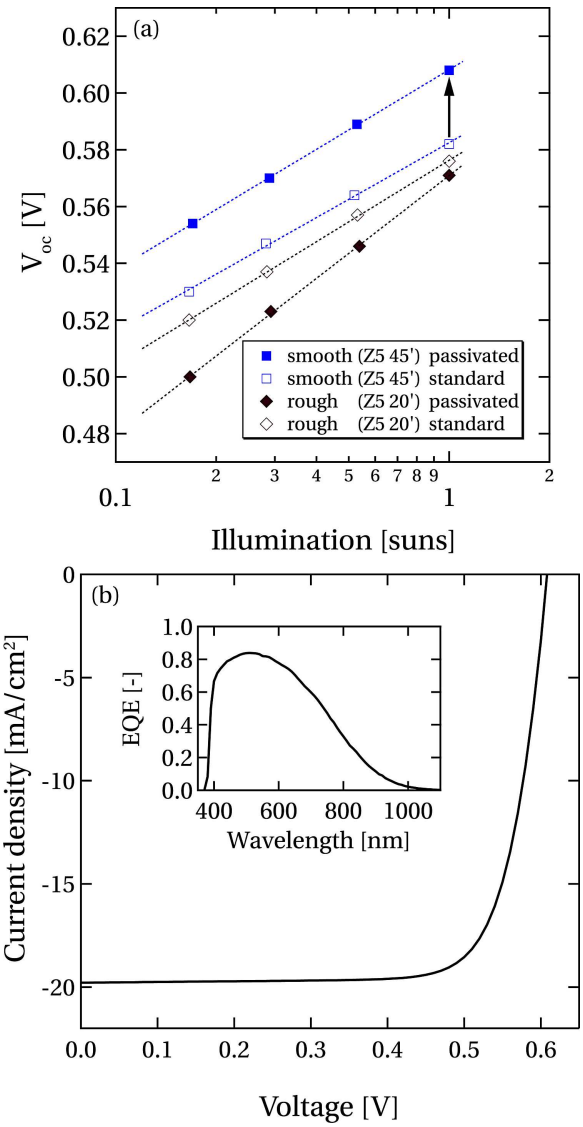

Figure 2 (a) V_{oc} values as a function of illumination level for single-junction μc-Si:H solar cells with a 650-nm-thick absorber layer, deposited on smooth and rough superstrates. The dotted lines represent fits with a one-diode model. The diode ideality factor was calculated from the slope of the fit. (b) J–V and EQE (inset) curves of the best cell reported in Table 1, yielding a V_{oc} value of 608 mV.

Table 2 Performance of a thin p–i–n μc-Si:H solar cell deposited on a smooth Z5 45' superstrate, with a 650-nm-thick absorber layer, a passivated design at the i–n interface and a designed area of 1.06 cm^2, with and without a textured ARC at the air-glass interface of the cell.

ARC ?	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm^2]	η [%]
no	600	72.8	20.35	8.89
yes	599	73.2	21.55	9.45

ZnO back electrode is used and for the cells without an a-Si:H buffer layer (0 nm), the n-doped layer is unchanged (n-a-Si:H /n-μc-Si:H).

A generalized V_{oc} drop is observed for increasing absorber layer thickness [7] for all buffer layer thicknesses, except for the case of the thickest cell on rough superstrate

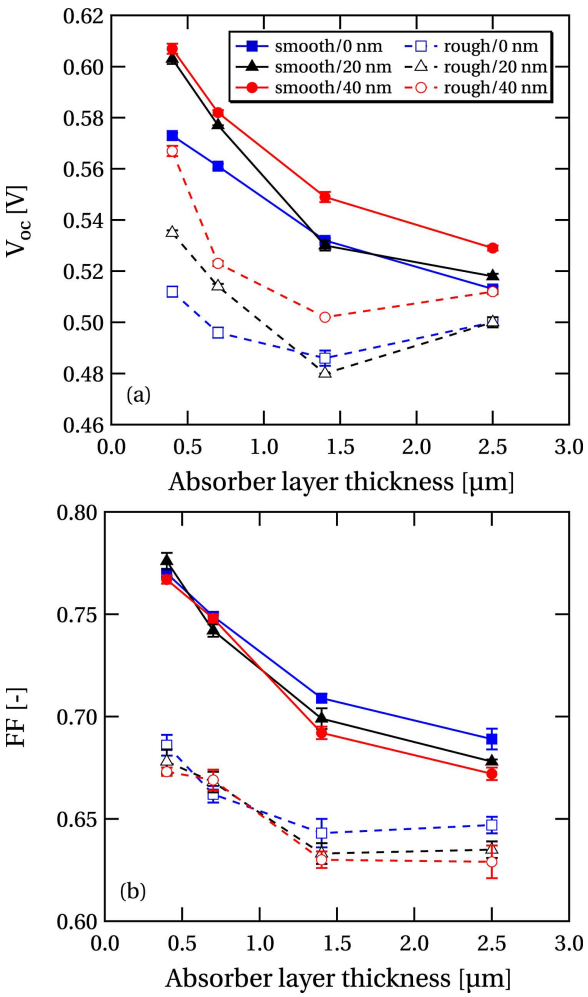

Figure 3 Evolution of V_{oc} (a) and FF (b) as a function of the thickness of both the intrinsic μc-Si:H absorber layer and the intrinsic a-Si:H buffer layer for solar cells deposited on smooth Z5 45' (solid symbols) and rough Z5 15' (empty symbols) superstrates (average and standard deviations (error bars) of the five best cells).

where V_{oc} is slightly increased as compared to the 1.4-μm-thick cells. We attribute this slight increase in V_{oc} to the formation of nanoporous zones on rough superstrate: the increased absorber layer thickness may allow these regions to close, reducing V_{oc} losses induced by connecting such defective regions directly with the ZnO back electrode. An increase in V_{oc} is observed on smooth and rough superstrates with increasing buffer layer thickness for all absorber layer thicknesses (from 0.4 to 2.5 μm), except for the solar cells with a 1.4-μm-thick absorber layer and 20-nm-thick buffer layer. In that case, a very small decrease is observed (of up to 5 mV). We attribute this deviation to a slightly higher crystalline fraction. The effect of the buffer layer is particularly visible on very thin devices, with a large increase in V_{oc} of up to 55 mV for the thickest buffer layer (40 nm).

As can be seen in Fig. 3(b), FF values decrease with increasing absorber layer thickness, suggesting limited transport properties in the absorber layer [28]. For thin cells (0.4 and 0.7 μm), there is no significant effect of the buffer layer on the FF . However, for the thicker cells, a drop in FF is systematically observed with increasing buffer layer thickness, due to further hindering of the transport properties [23, 29].

Thus, for a very thin absorber layer, a large increase in FF is obtained on the smooth superstrate (Z5 45') as the buffer layer is thickened. Conversely, for thicker absorber layers or on rough superstrates such as a Z5 15' (slightly rougher than the Z5 20' of Table 1), only a slight gain is reached for increased buffer layer thickness, as the V_{oc} gain is canceled by a FF loss, linked to a too high defect density in the bulk, limiting the cell performance.

Since very high V_{oc} values above 600 mV could be achieved experimentally for thin absorber layers, we wondered if the observed gain in V_{oc} could be reproduced qualitatively, by simulating low-quality crystalline silicon, sandwiched between two "electronically dead" doped layers, and adding a passivation. Simulations were thus performed with the solar cell modeling program PC1D [30], assuming absorber layer thicknesses of 0.5 and 3 μm. We modeled a low-quality crystalline silicon intrinsic layer with low electron (μ_e) and hole (μ_h) mobilities (μ_e = 10 cm^2/Vs, μ_h = 1 cm^2/Vs), sandwiched between two "electronically dead" doped layers with low bulk lifetimes (τ_{bulk}) and carrier mobilities (μ) ($\tau_{bulk,p=}\tau_{bulk,n}$ = 0.01 s, μ_e = 0.1 cm^2/Vs, μ_h = 0.02 cm^2/Vs). The thickness of these doped layers was fixed at 20 nm. Furthermore, the bandgap of the n-doped layer was set at 1.75 eV, and the conduction-band offset at the heterojunction was set at 0.15 eV by using electron affinities of 4.05 eV for the crystalline layers and 3.9 eV for the n-doped layer [31]. The surface recombination velocity at the p-doped side was fixed at 10^4 cm/s. Passivation at the i–n interface was subsequently introduced by varying the surface recombination velocity at this interface, for various τ_{bulk} of the absorber layer, linked to the quality of the absorber layer. To assess what would happen for very high μc-Si:H bulk quality, the chosen parameters cover a wide range of surface recombination velocities, from that

of a non-passivated silicon surface to that of a very well passivated surface, and τ_{bulk} values from below those reported for μc-Si:H (on the order of 100 ns [32, 33]) up to those for low-quality crystalline silicon.

Figure 4(a) shows the results of the simulation for a 0.5-μm-thick absorber layer.

For poor passivation (high surface recombination velocities at the i–n interface), V_{oc} is limited by this interface and stays low, even for higher τ_{bulk} values. Passivation of the interface becomes increasingly relevant for higher bulk quality (*i.e.* higher τ_{bulk}), the device is dominated by the interfaces and a gain in V_{oc} is observed in very thin devices, as also marked by an arrow in Fig. 2(a).

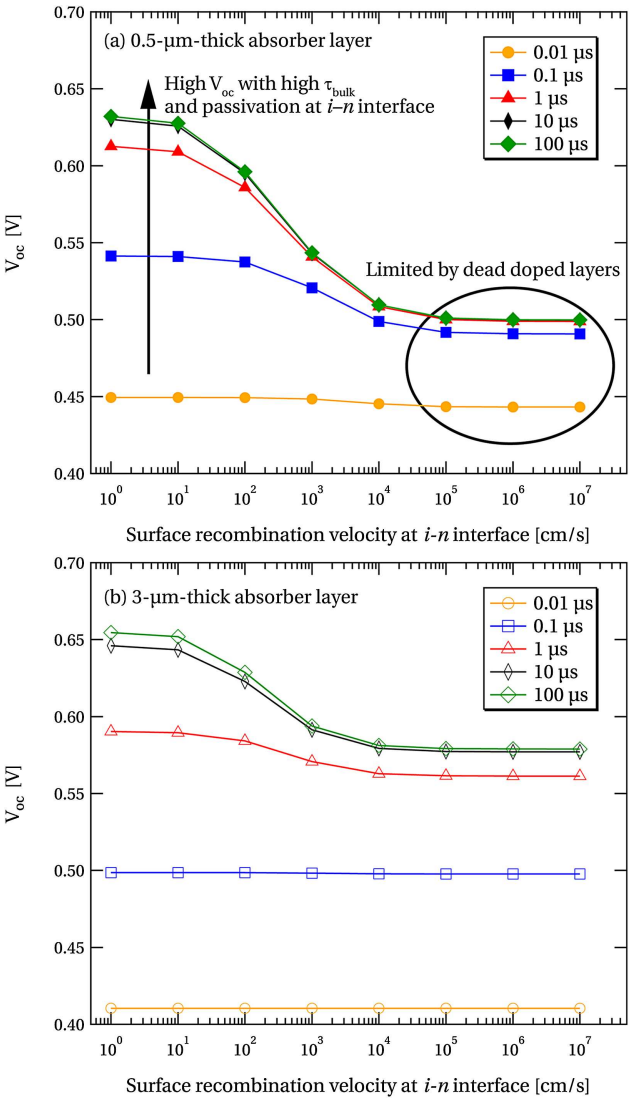

Figure 4 PC1D simulations for the V_{oc} of μc-Si:H solar cells with a 0.5 (a) and 3-μm-thick (b) absorber layer for different τ_{bulk} in the absorber layer and low-lifetime doped layers. Passivation at the i–n interface is simulated by reducing the surface recombination velocity at this interface.

For the case of a 3-μm-thick absorber layer, as shown in Fig. 4(b), a similar behavior is observed. Here, the thickness of the absorber layer reduces the effect of passivation, as a higher τ_{bulk} value is needed to obtain a gain in V_{oc}. However, note that whereas for low bulk lifetimes, the V_{oc} of the thicker device is lower than the V_{oc} of the thinner device, the situation is opposite for high bulk lifetimes. This lower V_{oc} for thin devices, counterintuitive for thin-film silicon but usual for crystalline silicon cells, is due to a lower surface lifetime (τ_{surf}) which scales with the thickness squared for high surface recombination velocity values, the overall effective lifetime (τ_{eff}) being calculated [34] by

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}}.$$

Although further investigation of the exact passivation mechanism is required, the conduction-band offset at the i–n interface is by nature not sufficient to fully passivate μc-Si:H. To obtain such a high V_{oc} value, we believe that surface defect passivation must be present as well, in the same way that an amorphous phase is likely required to passivate grain- and column boundaries in the μc-Si:H bulk.

4 Conclusion In conclusion, we have shown that a very high V_{oc} can be reached with thin μc-Si:H devices, provided a high-quality bulk material is used. The remarkable V_{oc} of 608 mV which was obtained, together with a high FF, demonstrates the potential of μc-Si:H, when compared to the best values currently obtained with crystalline silicon on glass [35, 36]. Furthermore, it was confirmed by simulation that "electronically dead" doped layers can limit the performance of solar cells. Passivation of these recombinative interfaces is therefore of high importance to further improve thin-film silicon devices. This result also paves the road towards single-junction μc-Si:H solar cells with efficiencies above 11% [37] and multiple-junctions containing middle or bottom cells with high V_{oc}, and allows the use of less silicon for similarly high efficiencies.

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