

Research progress of Si-based germanium materials and devices*

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Abstract: Si-based germanium is considered to be a promising platform for the integration of electronic and photonic devices due to its high carrier mobility, good optical properties, and compatibility with Si CMOS technology. However, some great challenges have to be confronted, such as: (1) the nature of indirect band gap of Ge; (2) the epitaxy of dislocation-free Ge layers on Si substrate; and (3) the immature technology for Ge devices. The aim of this paper is to give a review of the recent progress made in the field of epitaxy and optical properties of Ge heterostructures on Si substrate, as well as some key technologies on Ge devices. High crystal quality Ge epilayers, as well as Ge/SiGe multiple quantum wells with high Ge content, were successfully grown on Si substrate with a low-temperature Ge buffer layer. A local Ge condensation technique was proposed to prepare germanium-on-insulator (GOI) materials with high tensile strain for enhanced Ge direct band photoluminescence. The advances in formation of Ge n⁺p shallow junctions and the modulation of Schottky barrier height of metal/Ge contacts were a significant progress in Ge technology. Finally, the progress of Si-based Ge light emitters, photodetectors, and MOSFETs was briefly introduced. These results show that Si-based Ge heterostructure materials are promising for use in the next-generation of integrated circuits and optoelectronic circuits.

Key words: Ge; Ge-on-insulator; Si-based; epitaxy; light emitting diode; photodetector; MOSFET

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1. Introduction

As the downscaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) is approaching its fundamental physical limit, re-novel materials, such as GaAs, Ge etc, with higher carrier mobility and good optical properties are gaining considerable research interests in integrated photonic circuits. Future circuits may not only be composed of high speed microelectronic devices but may also use photonic devices for on-chip optical interconnection.

Among those materials, Si-based germanium has attracted increasing attention because of its ability to serve as a promising channel material to boost the MOSFET performance due to its higher carrier mobility, and two times and four times higher electron and hole mobilities than Si^[1]. On the other hand, it is also a good platform for the fabrication of photonic devices, compared to Si. Although Ge is an indirect band gap material, the energy difference between its direct bandgap and indirect bandgap is only 140 meV, which is much smaller than that of Si. It has been theoretically and experimentally demonstrated that the energy band structure can be tailored to the pseudo-direct bandgap by the introduction of a tensile strain in Ge. Thus, Ge efficient light emitters, modulators, photodetectors etc. based on direct band gap transitions in Ge were anticipated and experimentally demonstrated at wavelengths near 1.55 μm.

Over recent decades, various photonic devices based on

Ge materials have also been performed. The absorption coefficient of Si-based Ge layers at around 1.55 μm was significantly enhanced by strain-induced direct bandgap narrowing in Ge, which made the Si-based Ge photodetectors show high responsivity at 1.55 μm and 3 dB bandwidth over 40 GHz^[2–4]. Based on the quantum confined Stark effect at the direct bandgap of Ge in the strain-compensated Ge/SiGe multiple quantum wells, a modulator made on Si substrate operating at 10 GHz was demonstrated^[5, 6]. Si-based Ge light emitters have also very recently been reported based on the strain tailored band structure of Ge^[7, 8]. In microelectronics, the applications of high-k dielectric such as HfO₂, Al₂O₃ etc. overcame the barrier of the inherent instability of Ge oxides, high mobility Ge p-MOSFETs have been successfully demonstrated^[9]. However, the performance of Ge n-MOSFET degraded seriously due to the high interface state density^[10].

To realize the high performance of Ge photonic and microelectronic devices, we have to confront some big challenges, such as: (i) epitaxial growth of Ge films and its heterostructures on Si substrate; (ii) enhancement of Si-based Ge luminescence, and (iii) advance in Ge technologies, etc. Further investigation in these fields is necessary.

In this paper, the epitaxial techniques of strained germanium layer on Si substrate and their properties are reviewed, and then the tensile-strained Ge/SiGe heterostructures are designed and fabricated for photonic applications. Finally, some progress in the fundamental technology for Ge devices is described.

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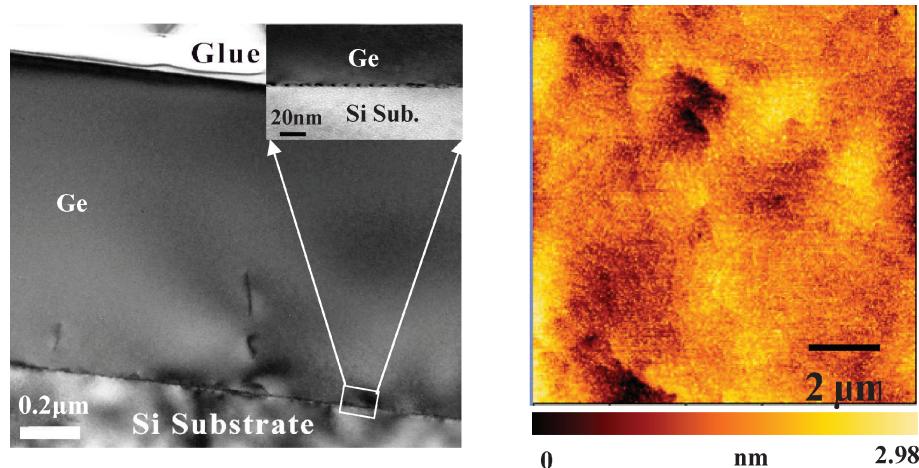


Figure 1. (Color online) Typical HRTEM and AFM images of Ge on Si grown by two-step growth techniques^[13].

2. Growth of Ge and its heterostructures on Si substrate

2.1. Epitaxy of Ge and Ge/SiGe MQWs on Si substrate with UHV/CVD

Si-based Ge material is considered to be a good platform for integrated photonic devices. However, it is difficult to directly grow Ge on Si substrate because of the large lattice mismatch (4.2%) between Si and Ge, which usually causes: (i) a high density of misfit dislocations at the Ge/Si interface and a high threading dislocation density (TDD) in the Ge layers, and (ii) high surface roughness due to island growth. Several methods have been proposed to overcome these negative effects, and two of them are widely employed. One uses thick component graded SiGe buffer layers to reduce the TDD in the final Ge top layer^[11]. In this method, about 10 μm thick SiGe layers are needed to obtain pure Ge films with low dislocation density of less than 10^6 cm^{-2} , this is too thick to be grown by UHV/CVD with low growth rate and used for device integration. The other is so called “two-step growth technique”^[12], in which a thin Ge layer is deposited directly on Si at a low temperature of 300–400 °C, followed by a higher-temperature growth (typically 600 °C) with a larger growth rate. Most of the misfit dislocations are confined near the low-temperature Ge layer and the interface between Si and Ge. Figure 1 shows typical high resolution transmission electron microscopy (HRTEM) and atomic force microscopy (AFM) images of Ge on Si grown by two-step growth techniques^[13]. The sample consists of 90 nm fully relaxed low temperature Ge layer and 870 nm high temperature Ge layer grown at 330 °C and 600 °C, respectively. It is indicated that there are period dislocations at the Ge/Si interface and the threading dislocations are mainly confined in or near the low-temperature Ge buffer layer. The surface is very smooth and the root mean square of surface roughness is only about 0.5 nm.

Considering the high crystal quality Ge epilayer on Si substrate as ‘virtue substrate’, we prepared Ge/SiGe multiple quantum wells (MQW) with Ge-rich barriers, which attracted more attention because of its possible application with the quantum confinement effect^[14–16]. Figure 2 shows typical HRTEM images of Ge/SiGe MQW on virtue substrate.

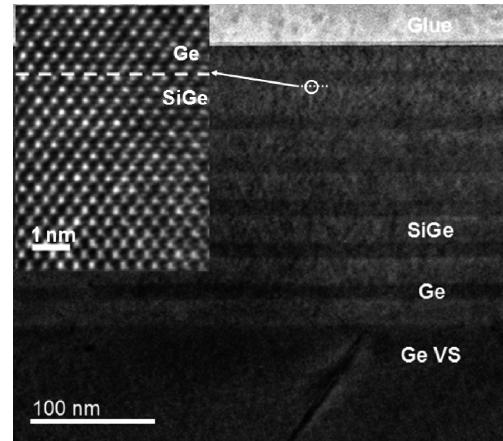


Figure 2. HRTEM images of Ge/SiGe on Si substrate^[15].

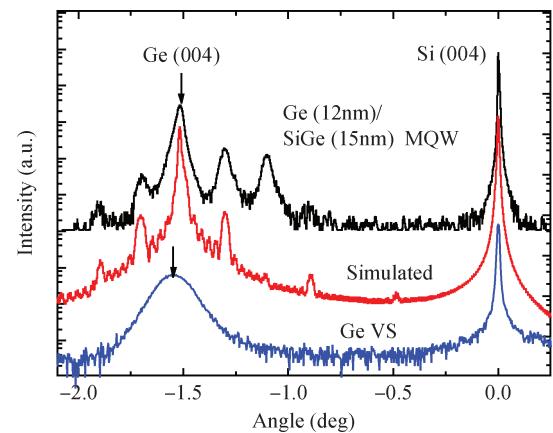


Figure 3. (Color online) Measured and simulated XRD rocking curves of Ge/SiGe MQW and Ge-on-Si virtue substrate^[15].

There are a few of dislocations in the Ge/SiGe MQW and the perfect lattice match at the Ge/SiGe interface suggests that the alternating growth of SiGe and Ge layers is pseudomorphic. Figure 3 shows DCXRD curves of the sample with Ge (12 nm)/ $\text{Si}_{0.13}\text{Ge}_{0.87}$ (15 nm) MQW on Ge virtue substrate. For comparison, the XRD rocking curve of Ge-on-Si virtue sub-

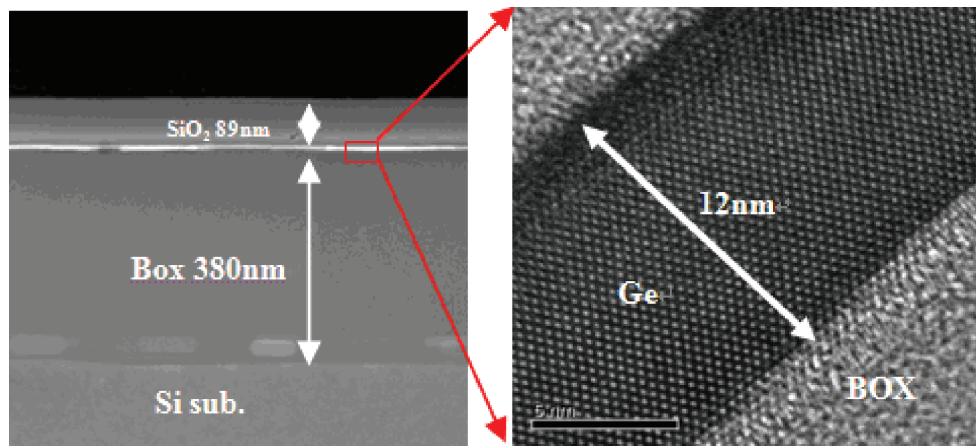


Figure 4. HRTEM images of GOI fabricated by Ge condensation techniques^[19].

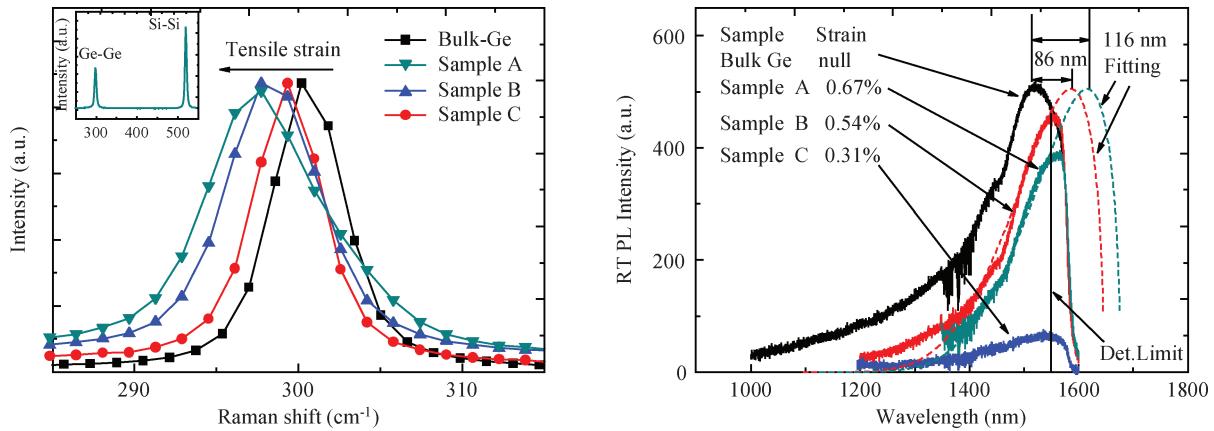


Figure 5. (Color online) Raman spectra and PL of ultra-thin GOI with sidewall protected by SiO₂ (sample A) and Si₃N₄ (sample B) and sample C without defining patterns for comparison^[19].

strate is also shown in this figure. The peaks from Ge virtue substrate are symmetric. Tensile strain of 0.17% in the Ge layer is evaluated from the peak position. For the Ge/SiGe MQW samples, five to six orders of superlattice satellite peaks are observed, indicating that these samples have high crystal quality and a sharp interface between Ge and SiGe layers. The structure parameters of the samples, such as thickness, Ge fraction, strain etc. can be determined by simulating the XRD curves based on the dynamical XRD theory. With the high quality Ge/SiGe MQW samples, quantum-confined direct band transitions in the tensile strained Ge quantum wells were directly demonstrated by room temperature photoluminescence. The photoluminescence peak energy of the tensile strained Ge/SiGe quantum wells shift to higher energy with the reduction of thickness of Ge well layers, which can be well explained by the direct band transitions that are due to the quantum confinement effect at the Γ point of the conduction band.

2.2. Preparation of Ge-on-insulator by Ge condensation techniques

Ge-on-insulator (GOI) is the other important kind of Si-based Ge material, which can be made by wafer bonding or so

called ‘Ge condensation’ techniques^[17]. When SiGe alloy on SOI substrate is oxidized, Ge is rejected from the oxide and piles up at the oxidizing interface, and then diffuses towards substrate, which is blocked by buried oxide layer to form a GOI substrate. In this way, SiGe thickness decreases linearly since the Si is selectively oxidized to form SiO₂, while Ge is ejected from the SiO₂ and accumulates in the region just beneath the oxide until to form pure Ge. The strain status of GOI can be modified by local Ge condensation processes, which is interested in improving performance of Ge MOSFET and photonic devices. Figure 4 shows the TEM images of GOI fabricated by cycling oxidation and annealing of SiGe on SOI substrate. The thin GOI is uniform and has high crystal quality. In order to modify strain in GOI during condensation process, we proposed a method of local oxidation of circular patterned SiGe mesa on SOI with the sidewall protected by SiO₂ or Si₃N₄^[18,19]. The high tensile strain of 0.67% is achieved for GOI mesa surrounded by SiO₂ estimated by Raman spectra, as shown in Figure 5(a). The relatively large tensile strain in GOI reduces the direct band gap energy of Ge, enhancing direct band transition PL intensity, as shown in Figure 5(b). These results suggest that the Ge condensation method is a promising approach for fabrication of high crystal quality ultrathin GOI materials for high performance devices.

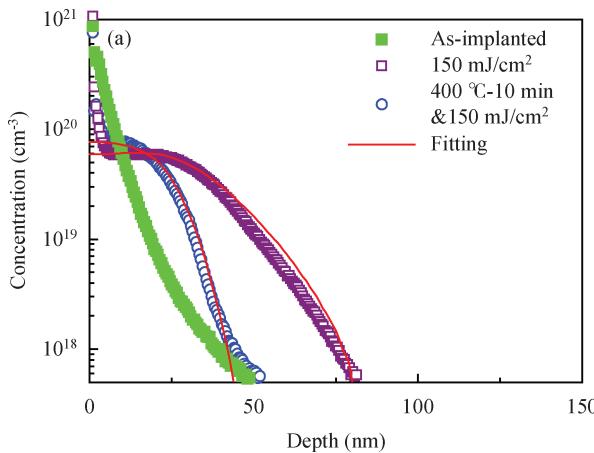


Figure 6. (Color online) SIMS profile of phosphorous in Ge before and after excimer laser annealing.

3. Advance in Ge device technology

3.1. Ge n⁺p shallow junctions fabricated with excimer laser annealing

Although the first transistor was made on Ge in 1947, the achievements in integrated circuits have been based on Si rather than Ge because of its many advantages, such as low interface state density and stable oxide. Ge has been excluded from the mainstream in microelectronics for several decades. However, recently the scaling limitation of integrated circuits has re-excited interest in the development of Ge devices. Even now, Ge device technology, unlike Si, is still far from mature. For example, reducing the naturally high surface state density on Ge and obtaining a high activation rate of n-type doping are still big challenges that make it hard to realize scaled Ge n-MOSFETs with higher channel conductance. Most n-type dopants such as P, As etc. have been demonstrated to diffuse quickly in Ge via vacancy-mediated mechanisms and the transient enhanced diffusion effect during thermal treatments. This makes it more difficult to get high n-type doping concentrations and shallow n⁺p junctions in Ge.

In order to suppress n-type dopants diffusion in Ge to make n-type shallow junction, the thermal treatment time should be short and the energy should be high enough to activate dopants. Compared with conventional thermal annealing, rapid thermal annealing (RTA), millisecond flashing etc., excimer laser annealing (ELA) is considered to be an effective method to obtain high n⁺ dopant activation in Ge^[20]. The pulse time can be adjusted to ns, which is also proven to be very efficient for recrystallization of ion-implanted Ge substrates.

Based on the properties of n-type dopant diffusion in Ge^[21], we proposed a novel approach to make Ge n⁺/p shallow junctions with high electrical activation of n-type dopant by using a combination of low temperature pre-annealing (LTPA) and ELA for phosphorus-implanted p-type Ge substrate^[22]. After implanting n-type dopant ions into Ge, the top Ge layer is severely damaged and even changes to an amorphous phase. The ion-implant induced defects in Ge were partially recovered by low temperature annealing, which could effectively suppress the TED effect and achieve shallow junctions during the following laser annealing. Figure 6 shows the phos-

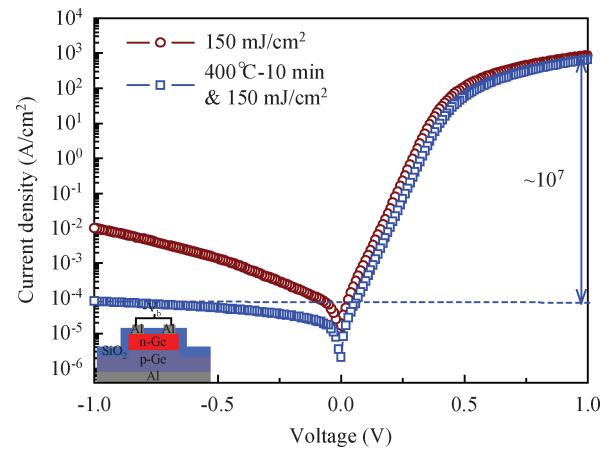


Figure 7. (Color online) I - V characteristics of Ge n⁺p shallow junctions^[22].

phorous profile of phosphorous ion implanted Ge before and after laser irradiation w/o pre-annealing process. It is shown that pre-annealing at 400 °C for 10 min. can significantly suppress phosphorous dopant diffusion in Ge during the following pulse laser annealing at 150 mJ/cm², which is more helpful to make n-Ge shallow junctions.

As a result, a Ge n⁺/p shallow junction diode was fabricated. Figure 7 shows the I - V characteristics of the n⁺p shallow junctions annealed by pulse laser annealing at 150 mJ/cm² w/o pre-annealing process. It is indicated that pre-annealing at 400 °C plays a significant role in reducing reverse leakage current via improving the crystal quality of Ge and sharp pn junction. The largest-ever-reported rectification ratio (I_{on}/I_{off}) of about 10⁷ and a high forward current density (658 A/cm² at 1 V) was obtained for the Ge n⁺p diode.

3.2. Modulation of the Schottky barrier height (SBH) of the metal/n-Ge contacts

Another challenge in making Ge devices is the formation of the metal/n-Ge Ohmic contact. Metal/n-Ge contacts always show a high Schottky barrier height of about 0.6 eV due to the strong Fermi level pinning effect (pinning energy is at about 0.1 eV above valence band), which is nearly independent on the metal's work function. The high SBH in metal/n-Ge contact could lead to large series resistance and degrade the performance of Ge devices.

To make good Ohmic contact for n-Ge, it is necessary to improve doping concentration and reduce SBH. In order to reduce the SBH of the metal/n-Ge contact, several techniques have been proposed to alleviate the FLP effect to form Ohmic contacts on n-type Ge. Ge surface passivation by nitridation or by (NH₄)₂S solution treatment before metal deposition were found to be effective to reduce the FLP, probably due to the elimination of the dangling bonds at Ge surfaces. Inserting an ultra-thin insulating layer (Al₂O₃^[23], SiN^[24], GeO_x, or AlO_x^[25]) between the metal and Ge was also effective to modify the SBH.

We proposed an approach of inserting an ultra-thin TaN layer between metal and n-Ge to modify the SBH. TaN is chosen because it is well compatible with standard Si CMOS technology^[26]. Figure 8 shows the I - V characteristics of Al, Fe,

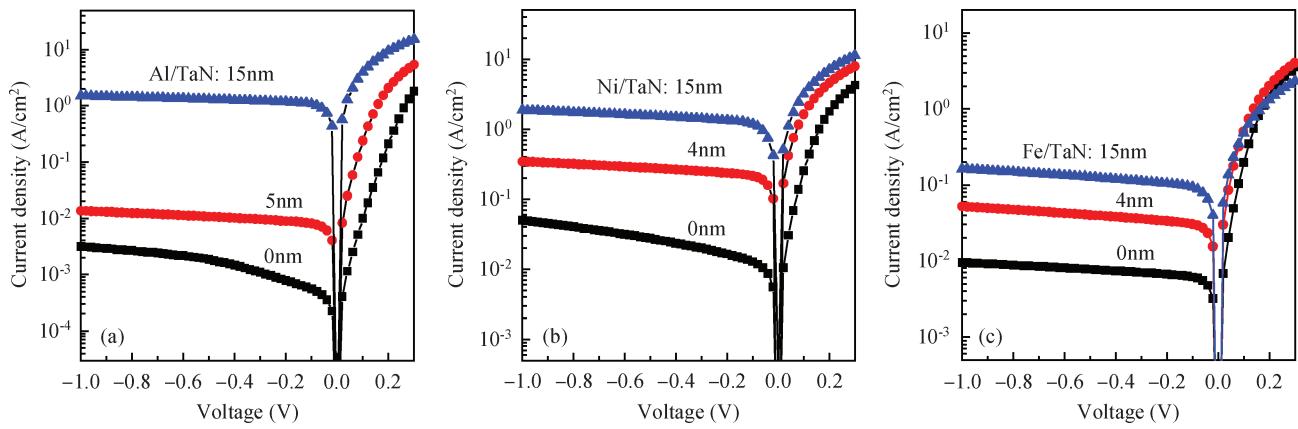


Figure 8. (Color online) Current–voltage characteristics of the (a) Al/TaN/n-Ge, (b) Ni/TaN/n-Ge, and (c) Fe/TaN/n-Ge contacts with various TaN interlayer thicknesses of 0, 4, 5, and 15 nm^[26].

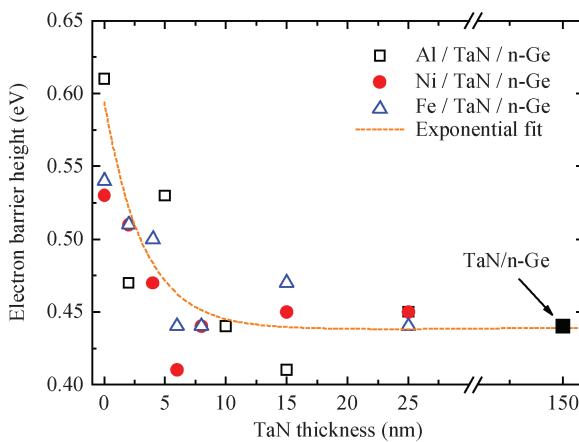


Figure 9. (Color online) Extracted SBHs as a function of the TaN interlayer thickness in the Al/TaN/n-Ge, Ni/TaN/n-Ge, and Fe/TaN/n-Ge contacts. The dotted curve is the exponential fitting line^[26].

or Ni/TaN/n-Ge with various thicknesses of TaN interlayer. In this experiment, Al, Ni, and Fe were chosen by considering their different work functions (4.28 eV for Al, 4.5 eV for Fe, and 5.15 eV for Ni). TaN interlayer thickness varies from 2 to 25 nm. It can be seen that the reverse current increases with an increase of TaN thickness, regardless of the kind of cap metals. This result implies that the SBH decreases with an increase of TaN thickness. By fitting the current–voltage curves based on a modified thermionic emission model^[27], the SBHs were extracted and comparatively plotted in Figure 9.

The SBHs of metal/TaN/n-Ge decreases from about 0.6 to 0.44 eV for the TaN/n-Ge contact with the increase of TaN thickness. It is clearly shown that the metallic TaN compound is different from the element metals for a n-Ge contact.

In order to clarify the role of N in metallic nitrides, TiN_x, WN_x with various N components were deposited on n-Ge for extraction of SBH for TiN_x, WN_x/n-Ge contacts^[28, 29]. Figure 10 shows the typical *I*–*V* characteristics of WN_x/n-Ge contacts. In this figure, N components are evaluated by XPS measurements to be 0, 0.06, 0.09, 0.15, and 0.19 corresponding to the flow ratio of Ar/N₂, respectively. It is indicated that the reverse current increases with the increase of N component in WN_x. For TiN_x on Ge, the similar *I*–*V* characteristics are ob-

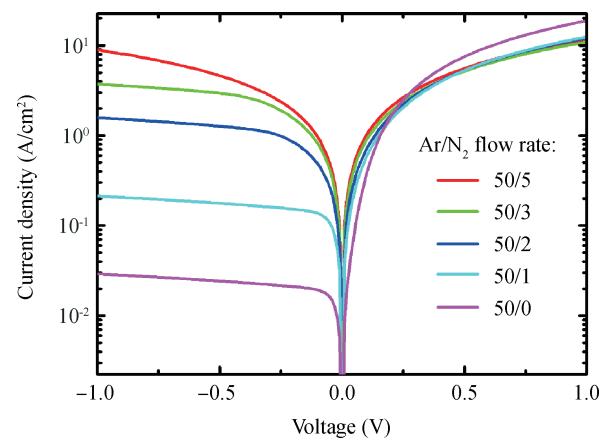


Figure 10. (Color online) Current–voltage characteristics of the WN_x films formed with various Ar/N₂ flow rate ratios, corresponding to x: 0, 0.06, 0.09, 0.15 and 0.19^[29].

tained with N component. The SBH, extracted with emission model, decreases from 0.52 eV for Ti/n-Ge to Ohmic contact (< 0.3 eV) for TiN_{0.19}/n-Ge. When metallic nitrides are deposited on Ge, N–Ge bonds may be formed at the interface between TiN and Ge. Because there is a large difference in electron negativities of N (3.04 eV) and Ge (2.01 eV), a dipole layer with an electrical potential drop at the contact interface is formed. This potential drop was added to the energy band bending and reduced the WN_x/n-Ge SBH. The SBH modulation mechanism is schematically depicted in Figure 11.

4. Si-based Ge devices

Along with the breakthrough of Ge epitaxy on Si and Ge device technology, various devices based on Ge-on-Si platform have been developed for possible application in microelectronics and optoelectronics. Here, the advances of Si-based Ge light emitters, photodetectors, and MOSFETs will be briefly introduced.

4.1. Si-based Ge light emitter

Ge light emitters have been fabricated by several groups

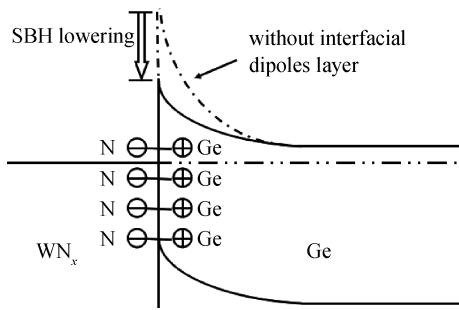


Figure 11. Schematics of band diagram of the pinning-alleviated $\text{WN}_x/\text{n-Ge}$ contact by the interfacial dipoles layer^[29].

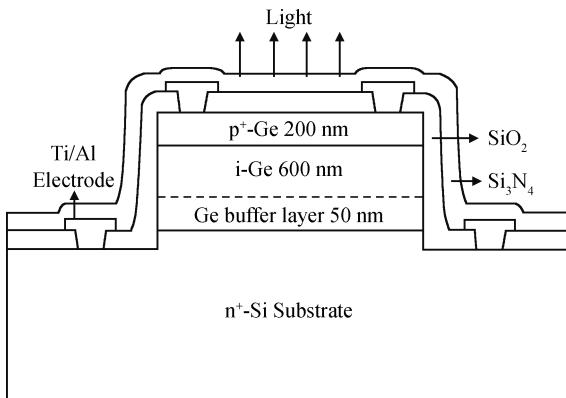


Figure 12. The cross-sectional view of the light emitting diode. The dash line is the border of the Ge buffer layer. The emission was measured from the top by detecting the light escaping from the surface of the device^[31].

since 2009. In 2009, almost at the same time, MIT^[30] and our group^[31] realized Ge LED on Si substrate. Our device has a $\text{p}^+ \text{-Ge}/\text{i-Ge}/\text{n}^+ \text{-Si}$ structure, while MIT's device has a $\text{p}^+ \text{-Si}/\text{i-Ge}/\text{n}^+ \text{-poly Si}$ structure. Electroluminescence is observed at room temperature. The cross-sectional view of our device is shown in Figure 12. The device was formed using the UHVCVD technology on $\text{n}^+ \text{-Si}(100)$ substrate with a carrier concentration about $5 \times 10^{18} \text{ cm}^{-3}$. A 50 nm thick Ge buffer layer was grown at 290 °C. Then the substrate temperature was elevated to 600 °C and an 800 nm thick Ge layer was grown on the buffer layer. The 200 nm p-type top Ge layer was boron-doped by implantation with a carrier concentration of about 10^{19} cm^{-3} . Circular mesa with diameters of 70 μm was then fabricated by dry etching patterned films down to the Si substrate using an inductively coupled plasma etcher. After a 640 nm thick SiO_2 film was deposited, metal contacts on Si and Ge were formed with a 50 nm titanium adhesion layer and a 1 μm thick aluminum layer. Electroluminescence measurements were performed on the LabRam HR 800 Raman Instrumentation with an InGaAs photodetector within 1350–1600 nm range at room temperature. When the bias was below 1.0 V, no emission was observed. Emission peaks around 1565 nm were detected under forward bias ranging from 1.1 to 2.5 V as shown in Figure 13.

Stanford University also reported a $\text{n}^+ \text{-Ge}/\text{p-Ge}$ light emitting diode on Si in 2009^[32]. It is demonstrated that n-type doping and higher temperature can enhance the luminescence

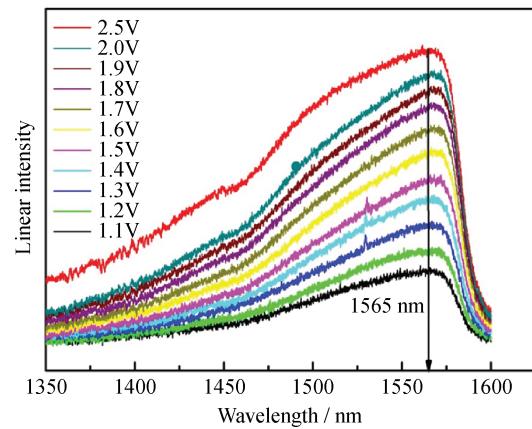


Figure 13. (Color online) The EL measurement of the device, the bias was ranging from 1.1 to 2.5 V.

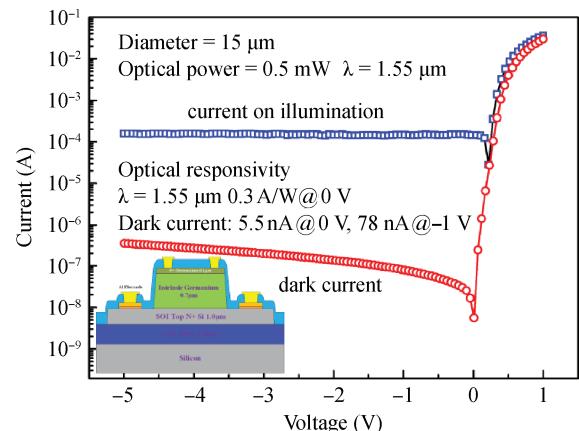


Figure 14. (Color online) The I – V characteristics of the device in dark and in light illumination. A schematic of the structure of the device is also shown.

efficiency of Ge. In 2010, a light-pumping Ge laser on Si was realized by the MIT group^[33]. They grew a Ge strip on Si by selected-area growth technology. The Ge strip was n-type doped to improve the luminescence. Pumped by pulsed 1064 nm laser with 50 μJ , the device showed lasing phenomena. In 2012 and 2015, Ge laser on Si was demonstrated by MIT^[34] and Kasper's group in Stuttgart University^[35], respectively. Although the threshold current is higher than 280 kA/cm^2 , which is too high for practical application, it is an important step for a laser on Si that is compatible with the CMOS process.

4.2. Si-based Ge photodetector

A Si-based Ge photodetector is one of the key photonic devices for Si optoelectronics. Thanks to the breakthrough of the growth of high crystal quality Ge on Si substrate, Ge photodetectors have had a very rapid progress. In 2009, we fabricated our first Ge photodetector on Si substrate with a 3 dB bandwidth of 4.72 GHz in 0 V bias^[36]. Due to the parasitic effect of the high doped Si substrate, the speed of the device is not so high. In order to improve the high speed performance, SOI substrate was used to fabricate a Ge photodetector^[37]. Figure 14 shows the structure and the I – V characteristics of the device in dark and in light illumination. The dark current is 78 nA

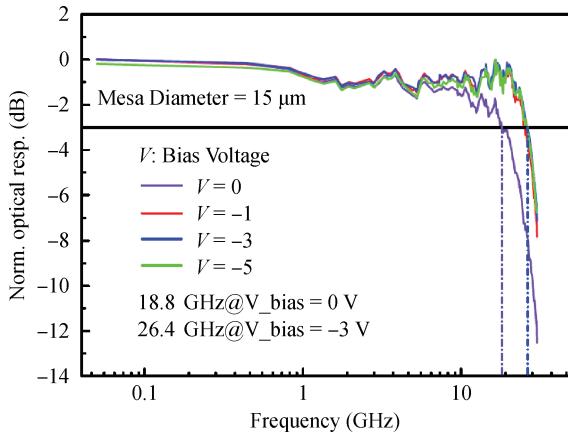


Figure 15. (Color online) Normalized frequency responses of the $15\text{ }\mu\text{m}$ diameter detector under different bias at 1550 nm.

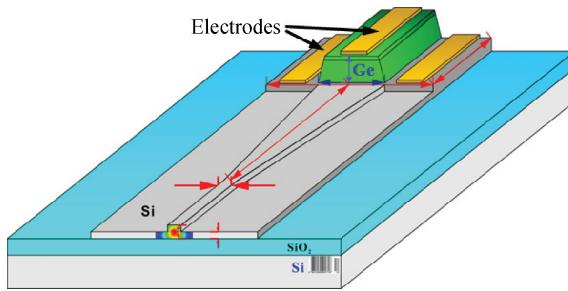


Figure 16. (Color online) Schematic diagram of waveguide structure Ge on SOI.

at -1 V bias for the device with $15\text{ }\mu\text{m}$ diameter. The responsivity is about 0.3 A/W at 1550 nm wavelength. Figure 15 illustrates the normalized frequency responses of the detectors under different bias at 1550 nm. A 3 dB bandwidth as high as 26.4 GHz is obtained for the $15\text{-}\mu\text{m}$ -diameter device under a bias of -3 V .

At normal illumination a Ge photodetector on Si suffers from a trade-off issue between quantum efficiency and bandwidth. In order to obtain high responsivity, the Ge absorption layer must be thick enough, but this will decrease the bandwidth. In contrast, if we decrease the thickness of the Ge absorption layer to improve the bandwidth of the photodetector, then the responsivity will decrease. This problem can be overcome by using a device with a waveguide structure since this design can decouple the photon absorption path and the carrier collection path. Figure 16 is a schematic diagram of waveguide structure Ge on SOI. The light from the Si waveguide will be coupled into the Ge layer and it can then be absorbed into it due to the higher refractive index of Ge than that of Si. For a device with $4\text{ }\mu\text{m}$ width and $10\text{ }\mu\text{m}$ length, the responsivity is about 0.842 A/W at the 1550 nm wavelength. The normalized frequency responses of the detector with an active area of $4 \times 10\text{ }\mu\text{m}^2$ at different bias voltages are shown in Figure 17. The 3 dB bandwidths at bias of 0, 1, 3, and 5 V are 0.28, 4.58, 16.64, and 19.00 GHz, respectively^[38].

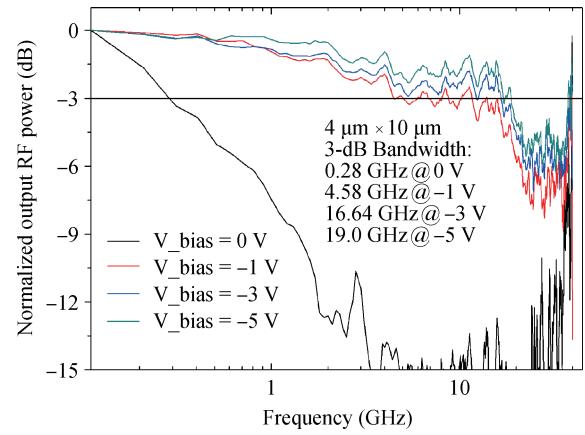


Figure 17. (Color online) Normalized frequency responses at the wavelength of 1550 nm for the detector with a size of $4 \times 10\text{ }\mu\text{m}^2$ ^[38].

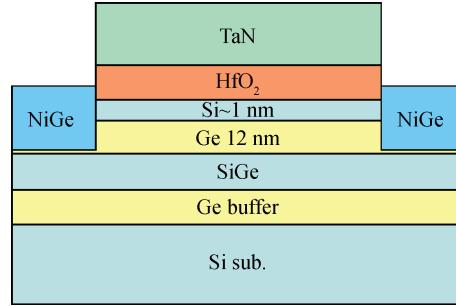


Figure 18. (Color online) A schematic of a Si-based Ge heterostructure SB-MOSFET.

4.3. Si-based Ge MOSFET

We proposed and fabricated a Si-based Ge/SiGe heterostructure Schottky barrier S/D metal oxide semiconductor field effect transistor (SB-MOSFET) with high- k /metal gate stack. The schematic of the device structure is shown in Figure 18. Firstly, a Ge layer was grown on Si substrate by a so called “two-step” approach, which serves as a Ge virtue substrate. A thin SiGe layer with/without *in-situ* doping was then grown on the Ge virtual substrate which acts as a potential barrier to confine the holes in the Ge channel due to the large valence band shift between Ge and SiGe layer. A 12 nm Ge channel layer and a 1 nm Si cap layer, as passivation layer, were grown. After that, a thin gate dielectric HfO₂ was deposited and NiGe/Ge Schottky junctions serving as source and drain was made to form MOSFET structure. Figure 19 shows the transfer and output characteristics of Si-based Ge heterostructure MOSFET. With the $I-V$ characteristics, the effective hole mobility of the devices was extracted, and the results are shown in Figure 20. The effective hole mobility of the device shows $\sim 80\%$ enhancement over the Si universal hole mobility. The off-state current caused by the lower Schottky barrier height of NiGe/Ge contacts can be effectively suppressed with a phosphorus doped SiGe layer. These results suggest that Ge/SiGe heterostructure is promising for a p-channel MOSFET.

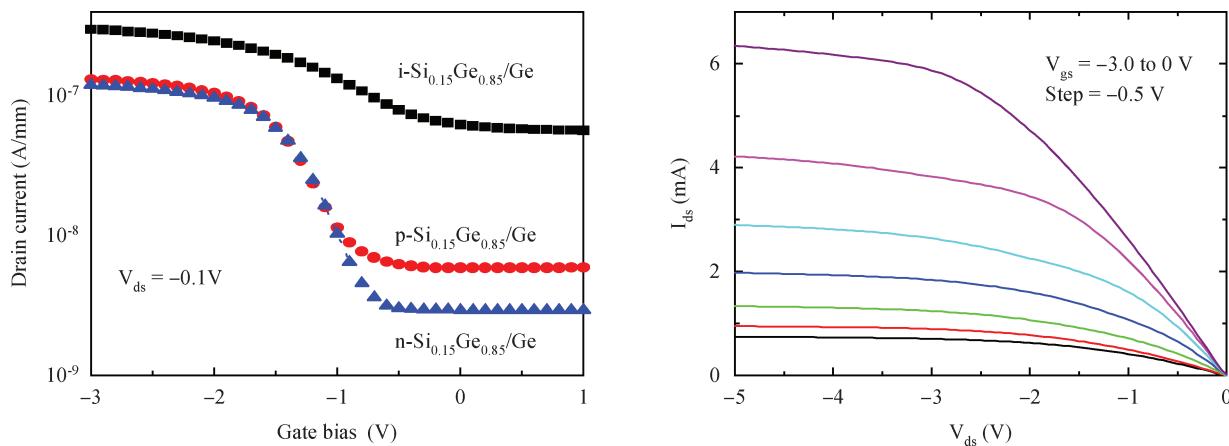


Figure 19. (Color online) Transfer and output characteristics of Si-based Ge p-MOSFET.

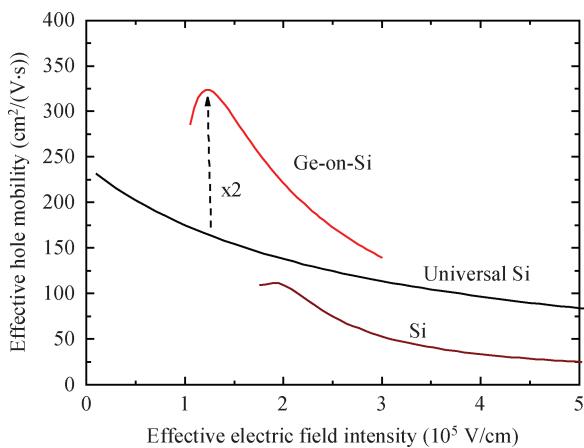


Figure 20. (Color online) Extracted effective hole mobility of Si-based Ge MOSFET versus electric field.

5. Summary and outlook

This paper has reviewed our development of Si-based Ge materials and devices, which was the result of a project that was financially supported by the National Nature Science Foundation of China. A high crystal quality Ge epilayer and GOI materials were fabricated on a Si substrate by a two-step epitaxy method and Ge condensation techniques. Based on these materials, high performance Si-based Ge light emitters, photodetectors, and MOSFETs were successfully developed.

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