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Review article

Ion implantation of advanced silicon devices: Past, present and future

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ABSTRACT

Ion implantation has been a key enabler, along with improvements in lithography, for the 40+ year evolution of MOS and then CMOS devices. Alterations in the channel doping levels followed the template developed by Dennard in the mid-70's from feature sizes of mm to tens of nm. When increasing channel doping in bulk planar CMOS created unacceptably high leakage current problems, ion implantation process developed past the "End of the Roadmap" to the "geometry-controlled" channels of fully-depleted finFETs and FDSOI of the present day. Future applications for nm-scale devices call for new understanding of ion damage accumulation in fin and nano-wire materials, consideration of effects of quantum confinement on channel conductivity, development of new implantation tools for efficient operation in the 100 eV range with ion and neutral species and soon after, for single-ion doping for quantum entangled, "atomic" electronics.

The structure of this paper frames the discussion in three time periods; (1) the 4 decades since the mid-1970's with the introduction and growth of Si-based ICs, first as bipolar and then MOS and CMOS devices, (2) the present day applications of ion implantation, focused on the process conditions related to the doping of finFETs and other 3D structures, and (3) the near-future (next 5–10 years) applications for ion (and energetic neutral) beams for processing of nm-scale semiconductor structures.

1. The past: ion implantation as enabler of CMOS scaling: 1970–2020

By the early 1970's it was recognized, at IBM, Intel and elsewhere, that, even though the ICs of the day were almost all based on bipolar transistors, the manufacturing "simplicity" and low-power operation of metal-oxide-semiconductor (MOS) transistors will greatly facilitate the development of increasingly complex IC circuits. This trend, recognized by Gordon Moore at Intel in 1965, that the number of transistors and memory bits in IC devices will double in approximately 2-year intervals, became a driving goal for the IC industry for half a century. By 1974, Robert Dennard at IBM systematized the changes in MOS transistor structure and operating characteristics that would follow from improvements in patterning technology. "Dennard scaling" for MOS transistors, built on the use of ion implantation to provide steadily shifting junction depths and dopant concentrations as lateral device dimensions were reduced, or "scaled", provided a template for design of next-generation transistors and fabrication process conditions. With the wide-spread introduction of CMOS transistors in the mid-1980's, replacing higher operating power bipolar, the combination of the planned regular scaling of lateral transistor dimensions by 0.7 (leading to a device area shrink of 0.49) for each new "node" and the corresponding shifts in junction depths and doping densities, guided by Dennard scaling, resulted in a global IC industry "roadmap" based on planar CMOS designs on "bulk" Si wafers. The exponential shrinkage of gate lengths, oxide thickness and junction depths (Fig. 1) for bulk CMOS continued until 2011.

Although technologically demanding, involving the use of vacuum processing, high voltages and requiring high temperature (> 1000 C) annealing for recovery of lattice damage and dopant diffusion, ion implantation brought key process and economic advantages to both bipolar and MOS transistor fabrication. For bipolar transistors, precise control of base implant energies and doses enabled much tighter controls on transistor gain with corresponding increases in device yield. For MOS devices, ion implantation was essential for setting channel doping levels for threshold voltage control and, when combined with self-aligned designs using poly-Si gates, reduced the source/drain-gate dopant overlap, resulting in faster and more controlled switching speeds. The ability of implant doping to use photoresist films as patterning masks, replacing the dielectric "hard masks" used for diffusion-doping, was a fundamental process simplification and positive economic driver. By the end of the 70's, ion implantation tools were well established as direct enablers of continued device scaling, especially for MOS and then CMOS chips.

1.1. Dennard scaling to the "End of the Roadmap"

Dennard's analysis of the doping requirements for increasing

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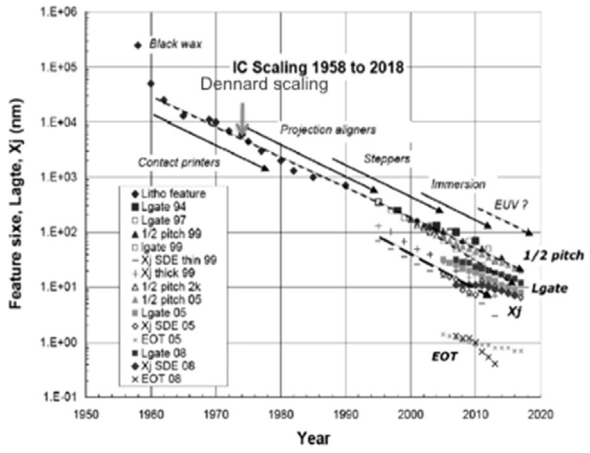


Fig. 1. IC transistor feature sizes (gate lengths, gate oxide thickness and source/drain junction depths) versus time as tracked by a succession of "roadmaps" for planar bulk CMOS.

"scaled" MOS transistors highlighted the use of ion implantation for doping of the channel and source/drain regions as a key enabler of systematic shrinkage of transistor size [1]. The key doping step was the use of implant to set the channel doping level for a controlled depletion width, w_d, and corresponding threshold voltage. The channel doping levels, initially in the mid-e16 dopants/cm^3, were far below the controlled capability of diffusion doping. Dennard then developed a description of the coordinated changes in doping and device dimensions (L_{gate}, t_{ox}, w_d, etc.), in both lateral and vertical directions, and the corresponding shifts in drive voltages that maintained a *constant local electric field* as the transistor size is shrunk. This progression of "well-tempered" MOS (CMOS) transistors resulted in systematic improvements in switching speed and power requirements (Fig. 2).

However, one crucial feature of the "well-tempered" CMOS scaling plan was universally ignored from the start. To maintain constant local electric fields within the transistor, the drive voltage should also be reduced by the scale factor 1/k, where k≈1.4. The general design goal for operating circuits at the highest available switching speeds led to the delay in reducing the supply voltage from its 1974 value of 5 V to the present day value of ≈1 V. If Dennard scaling were followed in detail, circuit drive voltages would all be in the vicinity of 0.2 V (Fig. 3) [2]. Scaling physical dimensions of MOS transistors while holding the drive voltage constant has the desired effect of decreasing the switching delay by 1/k^2 instead of the constant field (Dennard) case of 1/k. However a consequence of "constant voltage" scaling is the increase in channel doping by k^2 rather the linear, k, scaling with constant field designs. This will accelerate the conditions that eventually led to the breakdown of continual scaling for bulk planar CMOS transistors.

Other than the pace of reduction of supply voltages, "Dennard scaling" provided a detailed template for CMOS transistor designs for the decades of dimensional scaling shown in Fig. 1. For ion implantation process, the decades of 1970's until 2010 saw a steady, highly predictable, shrinkage of source/drain junction depths, leading to the use of lower ion energies, pre-amorphization implants to suppress channeling effects for light ion (Boron) doping and increasingly constrained thermal budgets to minimize dopant diffusion during damage annealing and activation.

1.2. Red Brick Walls

The evolution of CMOS transistor designs along the seemingly peaceful path shown in Fig. 1 was punctuated by a number of difficult challenges, referred to at the time as "Red Brick Walls". The early challenges for formation of "ultra-shallow" source/drain extension junctions was addressed in the late 1990's by the introduction of sub-keV ion implanters and a continued evolution of "rapid" annealers. Throughout the 2000's, the introduction of strained channels to increase carrier mobility using SiGe epi and other methods, then use of Cu metal lines and low-k inter-metal dielectrics to reduce RC signal delays and then introduction, for 45 nm CMOS, of high-k dielectrics and metal electrodes in the gate stack continually increased transistor drive currents with minimal dependence on scaling other than aggressive shrinkage of S/D contact pitch.

However one "Brick Wall" remained for continued scaling of bulk planar CMOS transistors, the consequences of increased channel doping levels to scale the channel depletion depth, w_d, and suppress lateral leakage currents. By 1998 it was recognized that the increased doping levels in the channel and "halo" regions would lead to unacceptably high leakage currents due to band-to-band tunneling (BTBT) for scaled MOS gate lengths of ≈25 nm (Fig. 4) [3]. Throughout the late 1990's and 2000's numerous process designs, such as "super-steep retrograde wells", were used as "workarounds" to BTBT leakage current effects. But by 2010, as gate lengths approached 25–30 nm, the "End of the Roadmap" for bulk, planar CMOS as described by Dennard in 1974 was reached.

1.3. Transition from dopant-controlled to geometry-controlled depletion widths

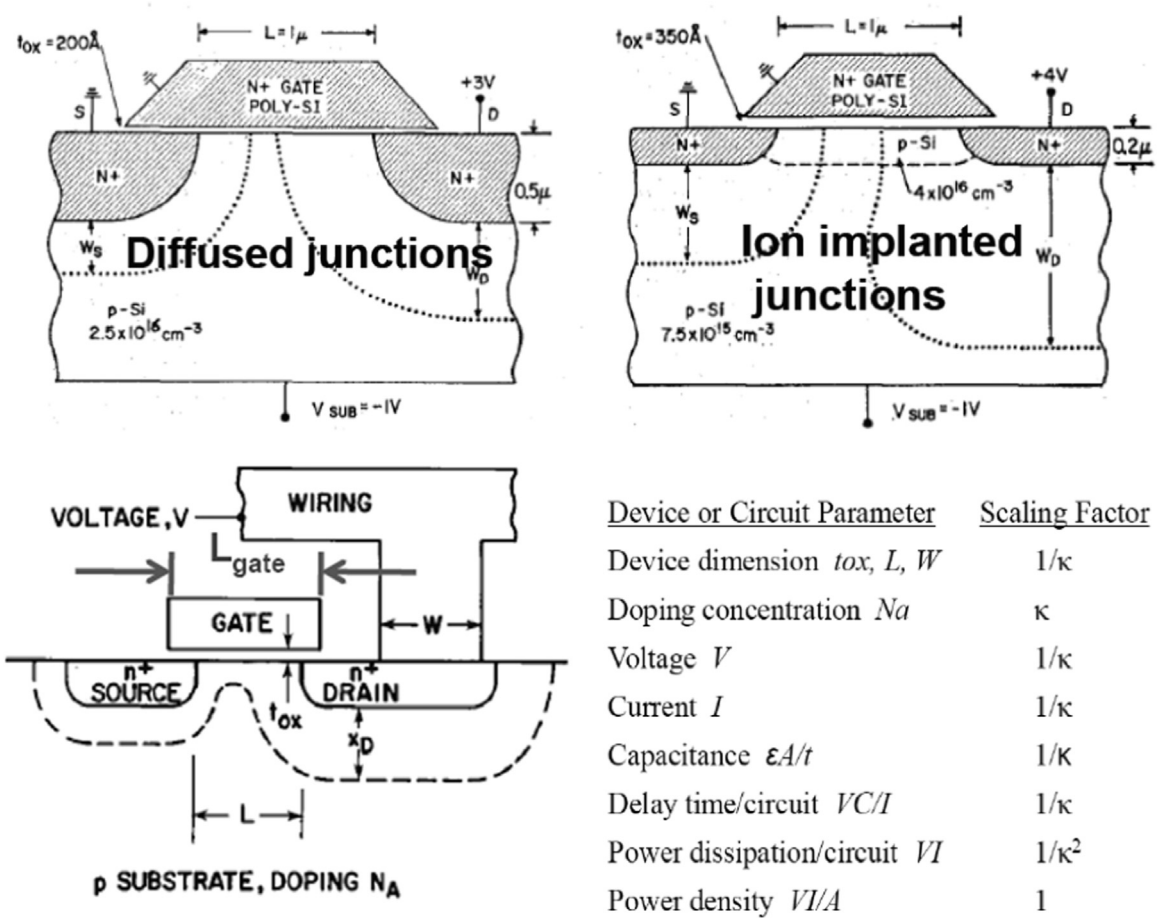
The industry response, again led by Intel in 2012, to the limitations of "dopant-controlled" channel depletion widths was to shift CMOS evolution to "geometry-controlled" channel lengths. Two design options were developed, both with channel widths considerably less than the ≈10 nm limit for bulk planar CMOS; (1) finFETs, where conduction in an ≈8 nm wide vertical channel is controlled by a "high-k/metal gate" electrode wrapped over the fin channel and (2) the use of planar "fully-depleted SOI" (FDSOI) where conduction in a ≈6 nm thick channel is controlled by bias on a top gate electrode and "back gate" bias on n and p-type doped wells below a relatively thin (≈25 nm) buried oxide (BOX). In both of these "fully-depleted" architectures, the ideal case is an un-doped channel. Gate lengths for both finFET and FDSOI transistors are expected to approach ≈10–15 nm in "7 nm" node devices. Further development of CMOS channels into nm-scale "gate-all-around" nano-wire arrays provides pathways for CMOS evolution well beyond the "End of the Roadmap".

2. The present: doping challenges for finFETs

The first commercial utilization of finFET devices was introduced by Intel in their “22 nm” products. Each CMOS transistor was formed from single or multiple fin-channels etched in bulk Si. The challenges for doping CMOS junctions in these vertical arrays are significantly different than planar devices. These include: (1) the need for conformal (uniform in depth) doping in the SD contact and extension regions so that the carrier conduction is uniform in the body of the fin-channel bounded by the gate electrodes, (2) the use of little or no doping in the channel region to take obtain high carrier mobility and avoid threshold voltage variations, (3) the tight pitch (≈42 nm for the Intel "14 nm" designs) of the fins limits the beam incidence angles that can be used and still avoid shadowing from neighboring fins to ≈10° off-vertical or less, (4) the combination of the increased surface area of a multi-fin array over the equivalent planar area and the ion reflection, recoils and sputtering for grazing angle ion incidence increases the effective dose and desired beam currents for doping finFET devices, and (5) damage accumulation and annealing in high-aspect ratio vertical fins are significantly different from the well-known challenges for planar junctions and need to be re-learned in this new context.

2.1. Creation of “ultra-slim” doping by grazing angle ion incidence

The doping of vertical structures with energetic ions, with either beam line or plasma immersion systems, always involves the incidence



Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/κ
Doping concentration *Na*	κ
Voltage *V*	1/κ
Current *I*	1/κ
Capacitance *εA/t*	1/κ
Delay time/circuit *VC/I*	1/κ
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1

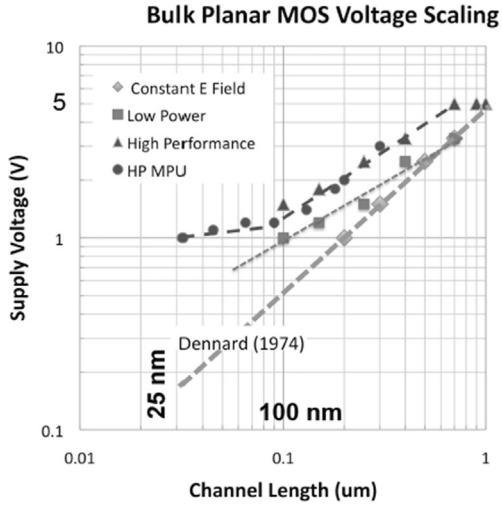
Fig. 2. MOS junctions and depletion regions for a 1 μm gate length nMOS transistor with diffusion and ion implanted doping (upper) and device scaling and electrical performance for dimension shrinking of a factor of 1/k (lower) [1].

of ions at some degree of glancing incidence to the surface. These conditions increase the rate of ion reflection and surface sputtering as well as reducing the ion penetration depth, all of which decreases the retained dose in the surface region to below the levels one gets with normal incidence ions. Lighter ion masses, with wider straggling ranges, tend to lose a higher fraction of the implanted dose through back reflection although the retained dose for highly glancing angle incidence falls rapidly for all ion types (Fig. 5) [4].

The effect of beam incidence angle on isolated fin structures is shown in Fig. 6, where increasing the grazing angle to 45° results in much higher sidewall doping levels and improved uniformity ("conformality").

2.2. Damage engineering in finFETs

For high-dose implants in source/drain regions of finFETs, the formation of amorphous regions is to be avoided, in direct contrast to the situation for planar junctions. When the a-Si region after high-dose



Parameters	Const Field	Const Volt
Dimensions	1/λ	1/λ
Potentials	1/λ	1
Doping Concentration	λ	λ^2
Electric Field	1	λ
Current	1/λ	λ
Gate Delay	1/λ	$1/\lambda^2$

Fig. 3. Supply voltage history from 1974 to ≈2010 (left) and scaling parameters for constant field ("Dennard") and constant voltage conditions (right) (data taken from [2]).

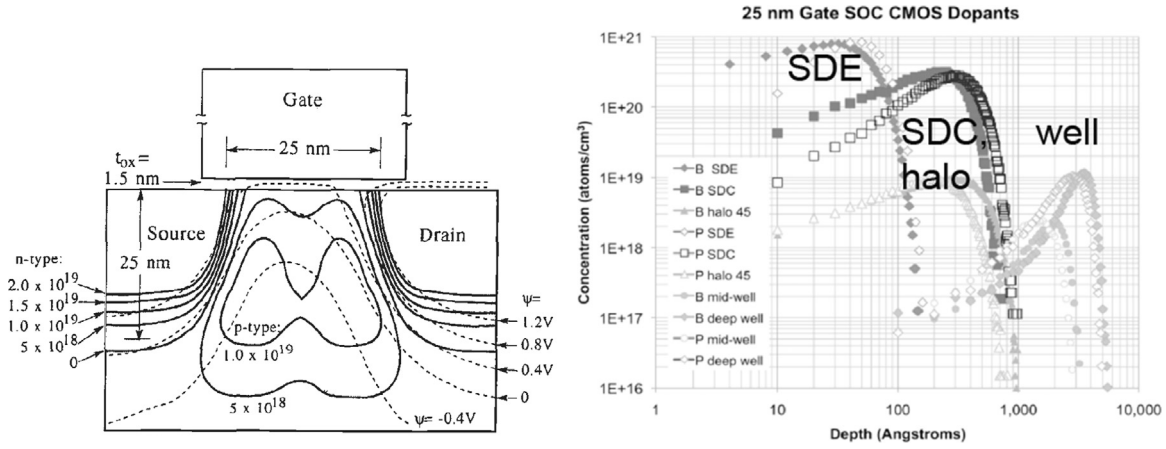


Fig. 4. Channel and source/drain doping profiles for an nMOS transistor with an effective channel length of 25 nm (left) [3] and doping profiles (right) for ≈25 nm gate length CMOS following the "well-tempered" rules of thumb; S/D extension (SDE) depth ≈L_{gate}/3≈10 nm, S/D contact (SDC) (and halo) depth ≈L_{gate}≈30–50 nm and well depth ≈ shallow trench isolation (STI) depth ≈400 nm.

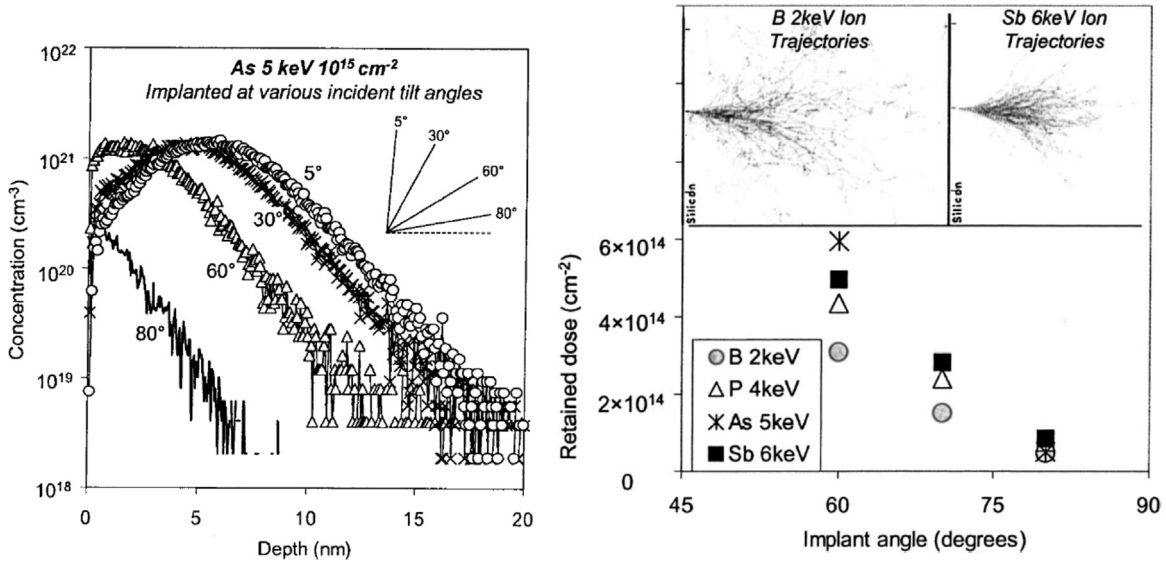


Fig. 5. SIMS profiles for 5 keV As at various incidence angles (left) and SRIM calculations of projectiles and retained doses for a variety of ions with a normal incidence mean range of ≈10 nm in Si (right) [4].

implants extends across the entire width of the fin, the crystal re-growth occurs from the c-Si seed in the base of the fin (for bulk finFETs). However the crystalline re-growth front is slowed near the fin sidewalls leading to formation of twinned regions and nucleation of poly-Si regions deeper in the a-Si segments (Fig. 7) [6]. Highly defective fin structures can be expected to show low carrier mobility and poor dopant activation from carrier scattering and dopant segregation to grain and twin boundaries.

Following on the earlier example of the use of high wafer temperature (≈600 C) for Oxygen implants for direct formation of buried SiO_2 layers for SOI wafers, implant temperatures of ≈450 C have been reported to be effective in preventing the formation of amorphous layers in finFET source/drain regions during high-dose As implants (Fig. 8) [7].

3. The future: implants for quantum confined and entangled systems

The direct extension of the exponential decrease in device feature size shown in Fig. 1 is the near-term exploration of semiconductor structures on the scale of nm's and then atoms. One finds that devices in this dimension range are not just smaller but are *fundamentally different*. In this quantum-dominated regime, the behavior of isotopic populations, effects of quantum confinement and long-range entanglement are added to the changes in basic mechanisms, such as ion damage accumulation, to create a very changed process environment from the accumulated experience with larger "bulk" devices.

Quantum confinement effects occur when the physical dimensions of a material are small enough to alter of basic quantum entities, such as phonon and electrical band structures. Among the changes with the onset of quantum confinement of a 3D solid to a 2D plane, to a 1D wire and then to a 0D quantum dot (QD) are: (1) increases in the band gap for semiconductor materials (familiar from the use of QDs for pure color sources for high-definition displays) and (2) strong reduction in the density of conduction and valance states and phonon bands (with corresponding reductions in electrical and thermal conductivity).

A figure of merit for the scale where the onset of 2D confinement becomes effective is the radius of an exciton, electron-hole pair, in the semiconductor material. Since an electron-hole pair is reminiscent of a hydrogen atom (with the hole acting as the nucleus) in the dielectric background of the semiconductor bulk, this radius is referred to as the Bohr radius, a_{Bohr}, 4.9 nm for Si.

From a kinematic point of view, for ions implanted into solids at energies approaching the onset of deposition conditions, at ≈100 eV, not only is the ion mean penetration depth reduced to a few nm but also the

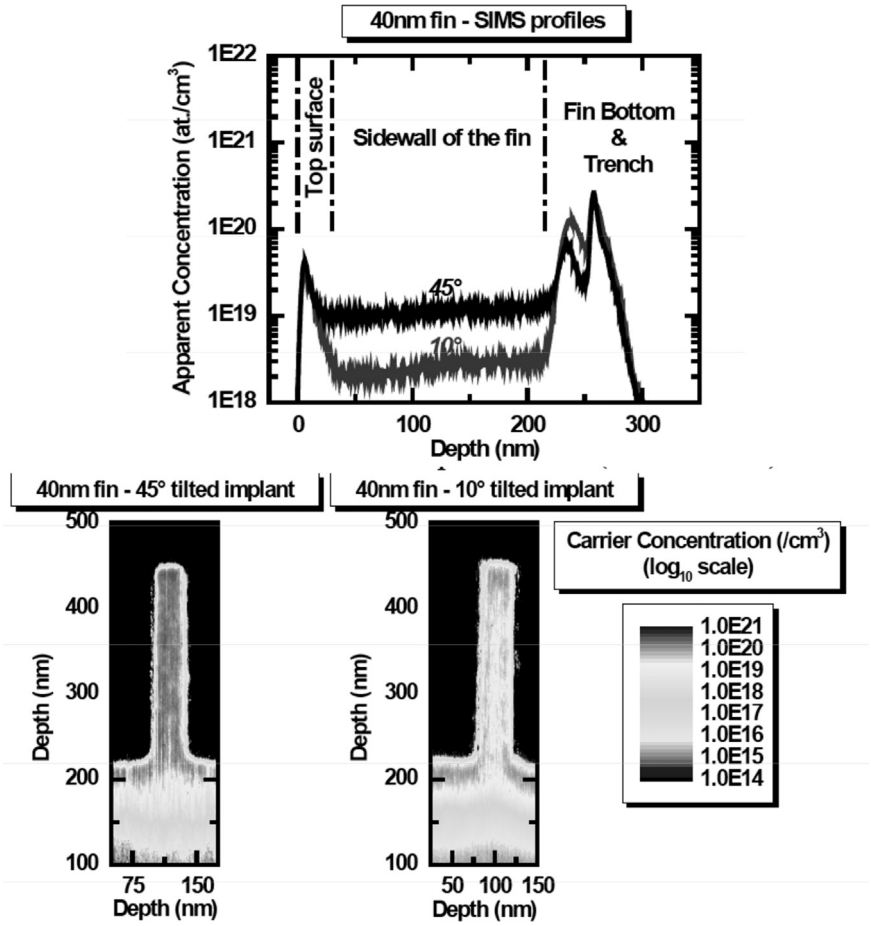


Fig. 6. Poly-fill-SIMS (upper) and Scanning Spreading Resistance Mapping (SSRM) images (lower) for B implants into "fat" (40 nm) fins at incidence angles of 10 and 45° (grazing incidence angle) [5].

number of created vacancy-interstitial ("Kinchen") pairs, backscattered ions and sputtered target atoms are all strongly reduced (Fig. 9).

3.1. Implant damage in nm-scale Si structures

Accumulated damage distributions in small dimension targets are markedly different than those for irradiated surfaces of 3D materials. Molecular dynamic calculations of damage superposition from multiple Ar ion impacts on a 4 nm wide Si hexagonal wire show very low levels of accumulated damage in the volume of the Si wire, even when the main ion profile is centered within the wire (see the 300 eV Ar^+ case in Fig. 10) [8]. The effects of the energy deposition from the ion impacts

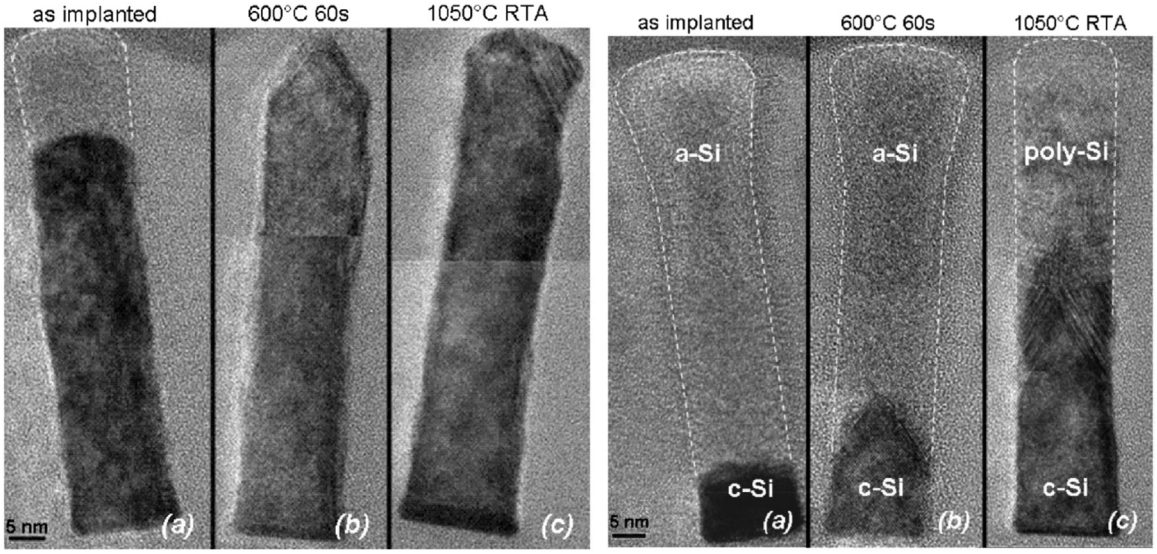


Fig. 7. TEM images of As and P implanted ≈15 nm wide Si fins and after anneals at 600 and 1050 °C for a shallow implant (left) (45° quad implants with 5 keV As at 1e15 As/cm^2) and a deep implant (right) (normal incidence 25 keV As at 3e15 As/cm^2 and 8 keV P at 2e15 P/cm^2). Note the effect of pinning of the re-growth front by the fin sides and formation of twin defects [6].

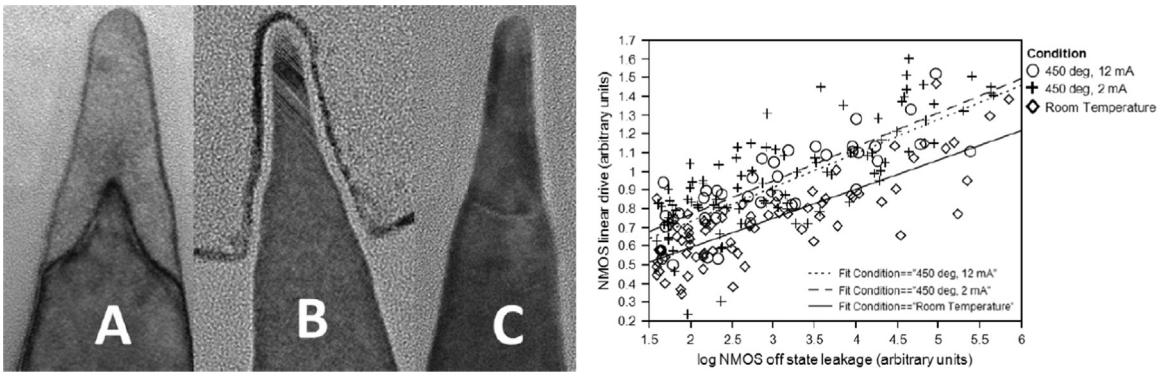


Fig. 8. TEM cross-sections (left) of (A) As implanted fins at room temperature (showing an amorphous region), (B) room temperature implant after spike anneal (≈1000 C/1 s) (showing {111} twin defects) and (C) after As implant at 450 C (showing no amorphous layer formation) and drive currents vs. leakage (right) for As implants at ≈25 and 450 C [7].

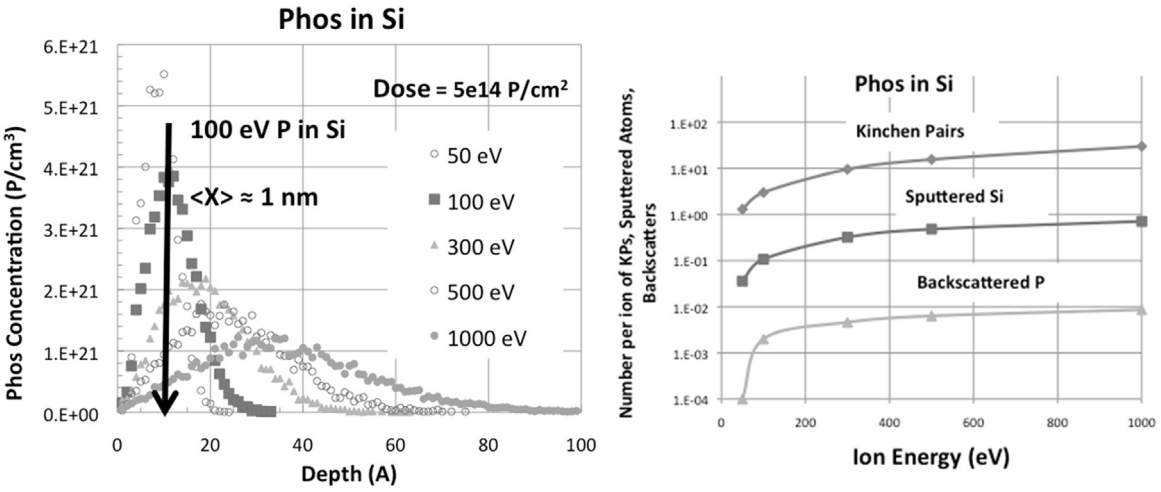


Fig. 9. SRIM (Monte Carlo) calculations of P in Si profiles (left) and number of Kinchen-Pease vacancy-interstitial pairs, sputtered Si atoms and backscattered P (right). Note the strong drop off in the sputtered and backscattered atoms for P energies below ≈100 eV.

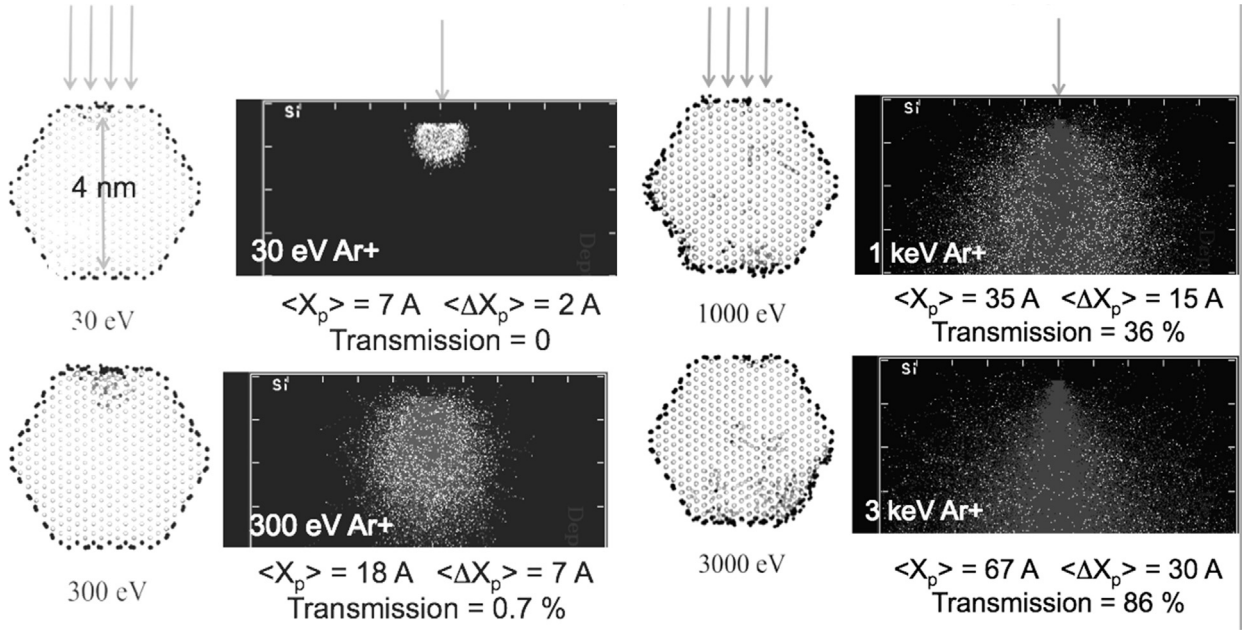


Fig. 10. Damage (indicated by darker dots) distributions along the surfaces and volume of 4 nm wide hexagonal Si wires after the impact of 200 Ar^+ ions at energies from 30 to 3000 eV [8]. Shown are the molecular dynamic calculations (on left) and SRIM (Monte Carlo) trajectories into planar Si (right). Also listed are the profile parameters (mean range and straggling) and the ion transmission percentage for a 4 nm thick Si plane. Note the buildup of damage along the target surfaces rather than in the bulk of the Si nano-wire.

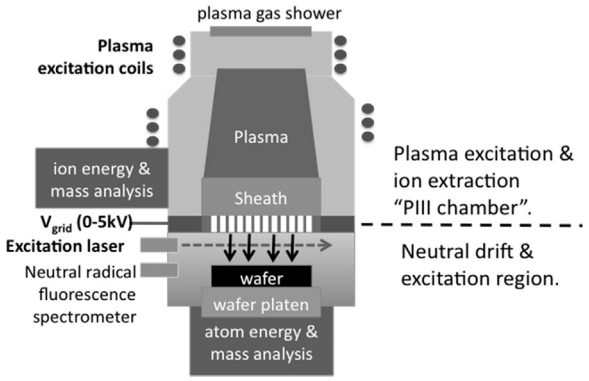


Fig. 11. Sketch of a "neutral beam processing" (NBP) chamber for ≈100 ev deposition, etching and implantation.

are mainly felt along the surface atoms of the wire.

3.2. Neutral beam processing

Ion processing, for implantation, etching and plasma-enhanced deposition, leads to damage effects resulting from build up of charge on isolated semiconductor and insulator structures. These types of problems become harder to deal with for smaller feature sizes. An efficient way to avoid space charge and charge accumulation effects is to convert an ion beam into a beam of energetic neutrals by electron transfer during ion-wall collisions while passing through a grid array (Fig. 11). This approach has been developed for neutral beam etching (NBE) and applied to fabrication of finFETs [9] and quantum dot (QD) arrays [10]. In the system sketched in Fig. 11, applications for energetic neutral atoms for deposition and implantation are added to the etching functions by choice of the plasma chemistry and pulsed extraction/neutralization grid bias voltage and duty cycle. This "Neutral Beam Processing" (NBP) chamber could have additional capability for measurements of ion and neutral atom mass and energy, neutral atom excitation with a scanned laser beam below the grid array and atom fluorescence spectroscopy. The upper plasma chamber, similar to designs for "plasma immersion ion implanters" (PIII), can be operated efficiently with extraction grid bias of ≈100 eV and below for nano-scale processing.

3.3. Template engineering for growth of 2D "monolayer" structures

The controlled formation of single and bi-layer graphene is a requirement for industrial exploitation of the electrical properties of these molecular materials for FETs, laser diodes, etc. Ion implantation, when combined with selected metal bi-layers, can be used to deliver a precise dose of C to the metal layer surface for formation of nearly perfect single and multi-layer graphene [11]. When C is implanted at a selected dose into a C-soluble metal (Ni in the case shown in Fig. 12) deposited on a C-insoluble metal (Cu in this case) and the implanted metals are annealed, the inter-diffusion of Cu into the Ni layer drives the C dose to the metal surface allowing the formation of near-perfect graphene layers; a single layer for an implanted dose of 4×10^{15} C/cm^2 and a bi-layer for a dose of 8×10^{15} C/cm^2. The use of implantation to deliver a precisely required dose of C provides a potentially large-area method for multi-layer graphene film fabrication with a higher degree of control than thermal CVD methods.

3.4. Atomic electronics for quantum computing

The implantation of controlled arrays of "single and few" atoms with nm-scale precision has been actively pursued now for nearly 2 decades. The value of such precision arrays of dopants was shown by the increased control of the threshold voltage distribution with regular arrays (ΔVth=0.1 V) compared to a random distribution (ΔVth=0.3 V) of dopants (Fig. 13) [12].

The single ion arrays shown in Fig. 13 were implanted by passage of ions through a small aperture with the ion impact on target monitored by a burst of secondary electrons. After the impact signal was detected, the beam was blanked off and the target stage moved to the new location for another single ion shot. Such single-ion implant designs did not offer a clear path towards higher throughput systems or reliable use for precision implantation of multiple ions in a single location without significant statistical variations. Modern single-ion "determi-

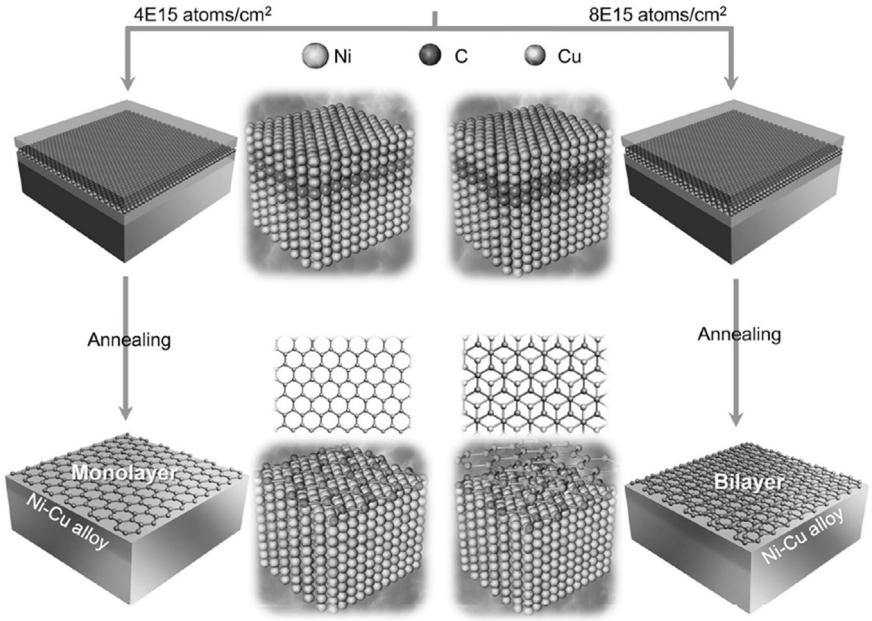


Fig. 12. Growth of monolayer (left) and bi-layer (right) graphene after implantation of C at a dose of 4×10^{15} C/cm^2 (left) and 8×10^{15} C/cm^2 (right) into a 300 nm thick Ni layer on Cu. Thermal annealing at 950 C for 10 min results in inter-diffusion of the Ni-Cu layers and expulsion of the implanted C dose onto the Ni-Cu metal surface, forming controlled layers of graphene depending on the C implant dose [11].

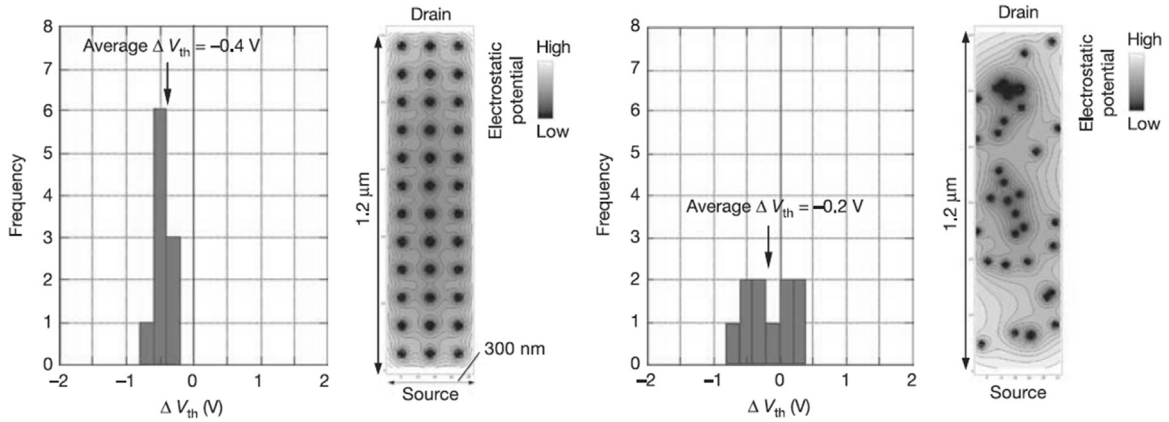


Fig. 13. Threshold voltage distributions for an ordered array of dopants implanted with a single-ion technique (left) compared to a random array (right). Shown are the Vth values and a contour plot of the implanted dopant Coulomb potentials. The threshold voltages for the 1.2 µm long channels were Vth=0.4 ± 0.1 V for the ordered array and Vth=0.2 ± 0.3 V for the random array [12].

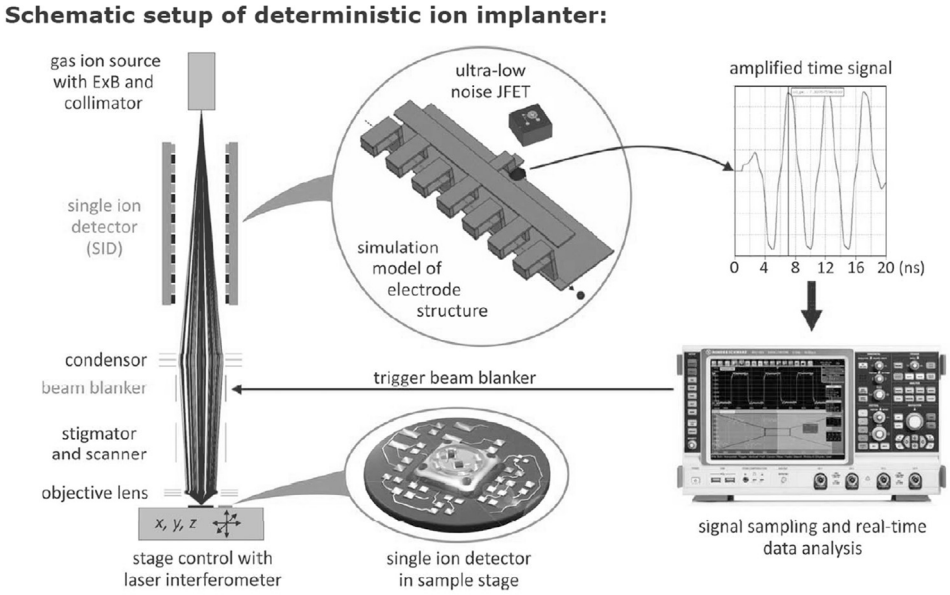


Fig. 14. Components of a "deterministic" ion implanter for controlled implantation of single ions by tracking passage of single ions along a detector grid array coupled with precision beam location on a target by focus-ion beam optics and laser monitored target stage positioning [13].

nistic" ion implanters include designs such as on-demand release from single-ion field "traps" and detection "on the fly" of the passage of single ions at the entrance to a focused ion beam optical scanner (Fig. 14) [13].

Modern deterministic doping work includes many studies of the electrical properties of single-atom channel transistors, monolayer dopant lines and properties of quantum entangled atoms as "qubits" in 3D arrays for quantum computing applications [14,15].

In the "single atom" transistor channel shown in Fig. 15, a single P dopant atom was centered between source/drain and gate electrodes using an AFM tip to disrupt a H-passivation layer on the Si channel surface at the central position, allowing for precision doping (within one lattice site) of a single P atom by exposure to PH_3 gas [16]. The measured transistor characteristics, after capping with a 180 nm Si layer, showed quantized behavior in full agreement with expectations, pointing to the use of deterministic methods for more complex atomistic electronics. The implementation of deterministic doping into commercial devices will require the development of single-ion implanters and other methods from the present day "table top" apparatus into fully foundry compatible, high throughput precision doping tools.

4. Summary

Ion implantation, in its many forms, continues to play an enabling role by providing a direct, controllable and cost effective method for delivery of dopants in specific device locations and in appropriate concentrations. The ongoing evolution of CMOS continues beyond the "End of the Roadmap" for bulk planar transistors, with dopant-controlled channel thicknesses, onward to geometry-controlled channels in fully-depleted finFETs and FDSOI transistors. Shrinks in channel thickness below ≈5 nm in Si or use of higher mobility materials (Ge, SiGe, InGaAs, etc.) will introduce band gap and density of states variations that will complicate and generally reduce carrier conductivity from bulk levels. The next steps will bring in transistors and other devices formed with single or a "countable few" atoms in quantum entangled systems.

A "quantum-based time line" for the near future is shown in Fig. 16, where recent ITRS roadmap values for bulk planar gate length and source/drain extension junction depth are plotted vs time. After the "End of the Roadmap" for bulk, planar CMOS with the transition to fully-depleted channels in advanced commercial devices (in 2011–12),

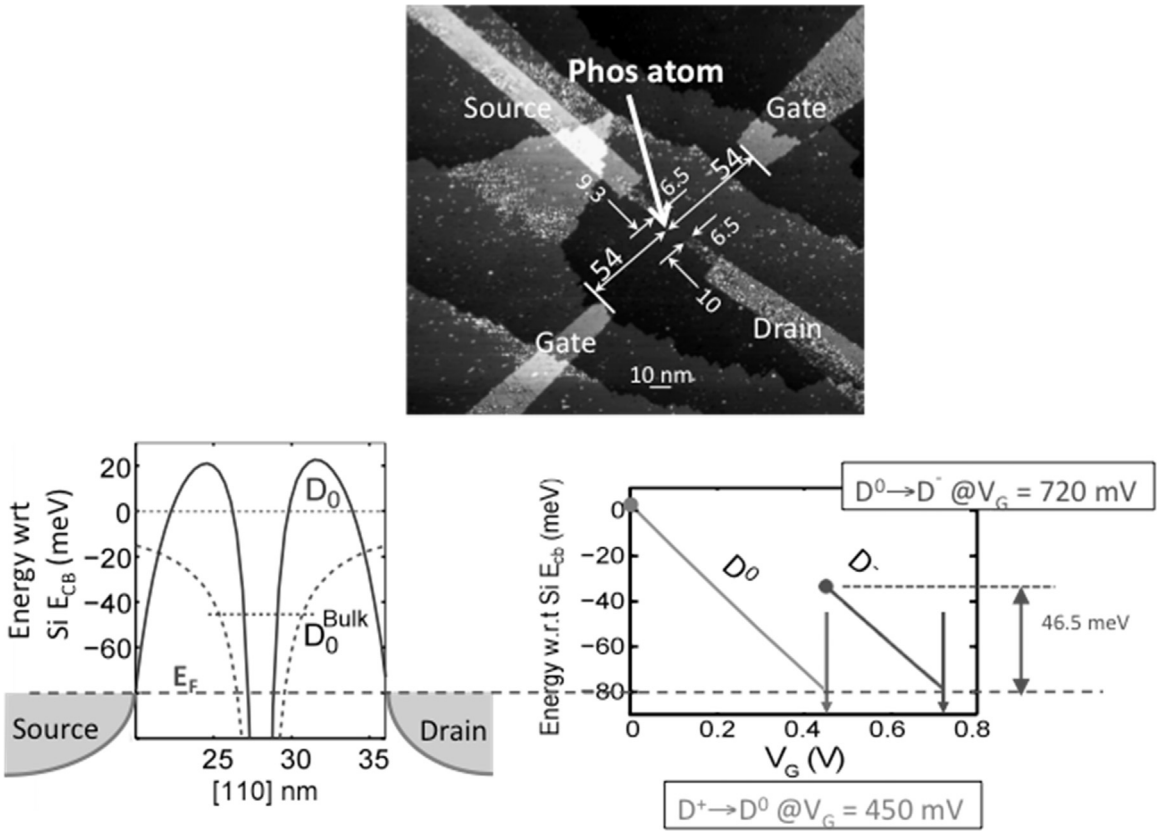


Fig. 15. STM images (upper) and quantum diagrams (lower) for a Si-based MOS transistor containing a single P atom centered in the S/D channel. The precision location of the single P channel dopant was accomplished by use of a H-passivation layer disrupted in the central location by an STM tip and doped by exposure to PH_3 [16].

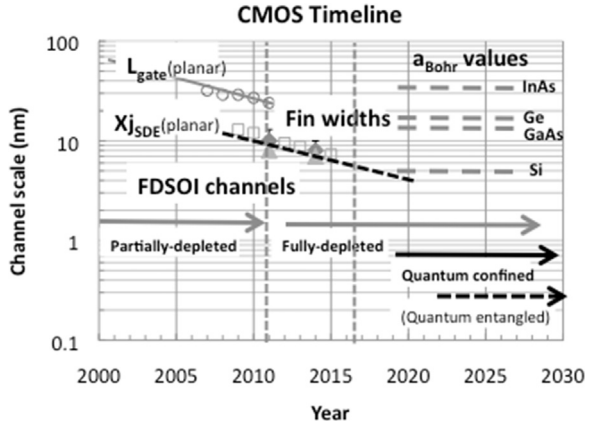


Fig. 16. Source/drain extension depth, channel thickness (for finFETs and FDSOI) and gate electrode size from recent roadmap reports, looking forward to 2030. Note that the channel thickness for finFETS adn FDSOI follow the same dimensional trends as the earlier planar S/D extension junctions depths, but now into the sub-10 nm range. Shown as vertical dotted lines are the transition from partially-depleted to fully-depleted CMOS (in 2011) and the present time (nid-2016). Also shown, as horizontal dotted lines, are the size of the exciton (electron-hole pair) radius in Si and a selection of candidates for high-carrier mobility channel materials, anticipating a transition to quantum confined behavior by ≈2020 and the advent of quantum entangled commercial devices in the early 2020's.

the channel widths for finFETs and FDSOI continue the timeline trends for source/drain extension thickness into < 10 nm values. If these "post-roadmap" trends continue, Si channels will shrink to less than 5 nm (by about 2020) and begin to enter the quantum confined regime (which takes strong effect in Si for channel dimensions of 3 nm and less). If Si channels are replaced by higher carrier mobility materials, such as Ge or InGaAs, strong quantum confinement effects will be experienced even with no shift in the channel thickness from the present day value of ≈7 nm.

Throughout this transition to nm-scale and quantum-controlled IC devices, ion implantation will continue to play key roles in many areas. Certainly the use of implantation for doping and materials modification of films and surfaces in "routine" ICs will continue. The use of high-dose H implants will continue for splitting of Si, Ge and other semiconductors for fabrication of SOI wafers and other forms of heterogeneous materials as well as a playing a role in advanced forms of 3D stacking of IC devices into high-bandwidth heterogeneous systems.

Ion implantation will also play a role in the industrial-scale fabrication of 2D films for advanced devices, such as the controlled formation of graphene bi-layers discussed earlier. Also as the commercial applications for quantum entangled devices for advanced computing grow, one fully anticipates the development of new ion (and perhaps neutral) beam implantation tools to enable these new forms of intelligent electronics.

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