An ultralow noise preamplifier for low frequency noise measurements

Gianluca Cannatà, Graziella Scandurra, and Carmine Ciofi
Dipartimento di Fisica della Materia e Ingegneria Elettronica, Salita Sperone 31, 98166 Messina, Italy

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Low frequency noise measurements are among the most sensitive tools for the investigation of the quality and of the reliability of semiconductor devices. The sensitivity that can be obtained depends on the background noise of the low noise preamplifier coupled to the device under test (DUT) that, at very low frequencies, is dominated by flicker noise. The low frequency noise produced by the DUT, on the other end, is very often the most interesting signal to be detected and analyzed. In this work we propose a very simple topology for the realization of a general purpose low noise preamplifier whose noise performances, at very low frequencies (below 10 Hz), are significantly better than those that can be obtained by the most popular commercial instrumentation. Indeed, a gain of 80 dB with a pass band extending from a few tens of mHz up to a few kHz with an equivalent input voltage noise as low as 14 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (100 mHz), 1.4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (1 Hz), 1.0 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (10 Hz), and 0.8 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (1 kHz) are consistently obtained by using quite standard electronic components and with no need for trimming and/or calibration steps. Moreover, the junction field-effect transistor input stage of the amplifier is characterized by an equivalent input current noise below 4 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ in the entire bandwidth, resulting in negligible background noise degradation for DUT impedances in excess of 100 $\mathrm{k}\Omega$. © *2009 American Institute of Physics.*
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I. INTRODUCTION

Noise measurements are among the most sensitive tools that are available for the study of the conduction mechanisms in electron devices.[1] Low frequency noise measurements (LFNM), in particular, have proven to be effective as a very sensitive probe for the investigation of the quality and of the reliability of microelectronic devices and processes.[2–4] Performing sensible noise measurements, especially at very low frequencies ($f<10$ Hz), is never an easy task because of the extremely low level of the voltage or current fluctuations that must be detected. In any low frequency noise measurement system there are several sources of noise and disturbances that contribute to set the lowest detectable noise level. Besides external disturbances that can be, at least in principle, completely eliminated by proper shielding, both the device under test (DUT) biasing system and the voltage or transresistance preamplifiers needed to rise the noise signal level to the proper amplitude for data acquisition and spectral elaboration, contribute to set the background noise of the system.[5] Bias system noise contribution can be made negligible by resorting to high capacity batteries as the source of power supply and, therefore, the equivalent input voltage and current noise of the preamplifiers do set the ultimate sensitivity that can be obtained. In the case of low frequency voltage noise measurements, the best performances in terms of equivalent input voltage noise (EIVN) are obtained by resorting to bipolar input stages. Unfortunately, bipolar input stages are also characterized by a relatively high level of current noise that, at best, is in the order of a few $\mathrm{pA}/\sqrt{\mathrm{Hz}}$, thus limiting the usefulness of such instrumentation to the case of DUT impedances in the order of 100 Ω or less. As an example, the FEMTO DLPVA-100-BLN-S bipolar input stage low noise voltage amplifier is characterized by an EIVN of about 0.7 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ with a $1/f$ frequency corner of 80 Hz, resulting in an estimated equivalent input voltage noise of about 20, 6.3, and 2.1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $f=100$ mHz, $f=1$ Hz, and $f=10$ Hz, respectively. However, the amplifier is characterized by an equivalent input noise of about 3 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ whose effect, depending on the frequency range, becomes significant with respect to the equivalent input noise for source impedances above a few hundred ohms. Much better voltage noise performances in the very low frequency range can be obtained with dedicated designs at the cost, however, of a higher level of equivalent input current noise.[6]

Input ac coupling down to very low frequencies ($f \ll 1$ Hz) is often required in the case of LFNM in order to reject the possibly large dc voltages resulting from the biasing of the DUT that would otherwise saturate the high gain input stages. Because of the large input biasing current, ac input coupling down to very low frequencies is not easily obtained in the case of bipolar input stages. For these reasons, junction field-effect transistor (JFET) input stage voltage preamplifiers are often preferred in the field of LFNM because, when compared to bipolar input stages, they are characterized by very low bias current and equivalent input current noise (in the order of a few $\mathrm{fA}/\sqrt{\mathrm{Hz}}$): because of the very low bias current (usually below 100 pA) ac input coupling down to a few mHz is possible by means of a simple RC high pass network with R in the range of few MΩ and reasonable capacitance values (a few μF); because of the low equivalent input current noise, no degradation of the

background noise is expected even in the case of DUTs with impedances in the range of a few hundreds kΩ.

If we search for commercially available voltage preamplifiers with the above mentioned characteristics, we realize that no significant advances have been made during the last several years. Indeed, researchers involved in the field of LFNM either resort to home made instrumentation or to quite old devices such as SR560 by Stanford Research or EG&G PAR113.[7–9] While remaining excellent and reliable pieces of instrumentation, such two amplifiers are characterized, at very low frequencies, by a high level of EIVN. Typical values of the EIVN at $f=100$ mHz, 1 Hz, and 10 Hz are 300, 40, and 13 nV/$\sqrt{}$Hz, respectively, for the SR560 and 130, 40, and 18 nV/$\sqrt{}$Hz, respectively, for the PAR113. When performing noise measurements on electron devices it is often possible to increase the noise level at low frequencies by increasing the bias or the operating temperature. In this way, one can overcome the limitation imposed by the background noise of the measurement system by increasing the noise level to be detected. However, increasing the bias and the operating temperature of a DUT may result in overstressing the device, which is not desirable, especially in the case of reliability studies. As an example, in the case of LFNM applied to the investigation of electromigration in metal lines, the wide dispersion in the results obtained by several researchers about the frequency and the temperature dependence of the electromigration noise is likely to be due to the fact that, because of the different sensitivity of the measurement system employed by each research group, significantly different stress conditions had to be applied to the samples during experiments, possibly resulting in the fact that different electromigration regimes and failure mechanisms were being investigated.[10] It is therefore apparent that the availability of JFET input preamplifiers with better noise performances with respect to those available on the market would be very useful in the field of LFNM. Indeed, general purpose JFET input ultralow noise preamplifiers with excellent performances at very low frequencies have been proposed in the past few years[5,11] and recently[12] in the literature. With these designs, noise performances better than 20, 2, and 1 nV/$\sqrt{}$Hz at $f=100$ mHz, 1 Hz, and 10 Hz, respectively, can be obtained.

Notwithstanding the possible advantages that could be expected in terms of gain in sensitivity, the design and realization of a custom low noise preamplifier may represent too large an investment in terms of time and effort for a researcher interested in noise measurements. Indeed, the degree of complexity of the designs proposed so far in the literature may be discouraging: besides the complexity in the circuit configuration, in almost any proposed design there must be a phase in which a device selection is made in order to get the best matching among discrete components and another phase in which calibration and/or trimming must be performed. It is for these reasons that we decided that it was worth investigating on the possibility of defining a very simple topology for a general purpose very low noise preamplifier whose actual realization should not require anything more that a very basic skill in the prototyping of board level electronic circuits. In this investigation we have regarded the low cost, the absence of any adjustment or trimming step, and the easy availability on the market of the components as mandatory requirements. As it will be demonstrated in the following, we believe that we have reached this goal since we have been able to devise a very simple circuit topology that, while characterized by excellent noise performances, requires a very small number of components and does not require any trimming or calibration step. In the proposed approach, gain accuracy as well as robustness with respect to device parameter dispersions are guaranteed by design.

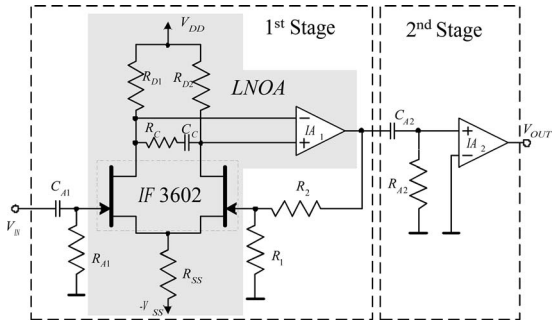

FIG. 1. Complete schematic of the proposed low noise voltage amplifier. Component type an values are reported in Table I. V_{DD} and V_{SS} are 12 V lead acid batteries.

II. NEW LOW NOISE AMPLIFIER

The design we propose in this paper is based on the very low noise JFET differential pair produced by Interfet. The schematic of the proposed low noise amplifier is shown in Fig. 1. A list of the required components, together with their relevant characteristics, is reported in Table I. The amplifier

TABLE I. Component list for the circuit in Fig. 1.

Component	Component type	Component value
J_1	Low noise JFET differential pair	Interfet IF3602
IA_1, IA_2	Instrumentation amplifier	INA131 (Gain=100)
R_1, R_2	0.1%, $\frac{1}{4}$ W, wirewound	10 Ω, 1 kΩ
R_{D1}, R_{D2}	5×10 kΩ, 0.1%, 1/8 W, in parallel, metallic film	2 kΩ
R_{SS}	2×3,3 kΩ in parallel, metallic film	1,65 kΩ
R_{A1}, R_{A2}	----	3.3 MΩ, 1 MΩ
C_{A1}, C_{A2}	Polyester	22 μF, 10 μF
R_C, C_C	----	68 Ω, 33 nF

consists of two cascaded gain stages each of which is characterized by a voltage gain of 100, thus resulting in an overall gain of 80 dB. The second stage is quite simple as it consists of an ac coupling stage (C_{A2},R_{A2}) and of a low input bias current instrumentation amplifier with a fixed gain of 100 (INA 131 by Texas Instruments). The role of the second stage is that of rising the level of the signal prior to digitization for spectral analysis. The high pass filter (C_{A2},R_{A2}) is characterized by a low corner frequency of about 16 mHz and provides for removing the large dc offset at the output of the first stage that, as we shall discuss in the following, is the result of the large input offset introduced by the discrete JFET differential amplifier. Because of the low input bias current of I_{A2}, it is possible to select a large value for R_{A2} in order to keep the size of the capacitor C_{A2} to a minimum. With $R_{A2}=1$ MΩ we have $C_{A2}=10$ μF. Even with such a value, since electrolytic capacitors cannot be used in low noise design because of the presence of microdischarges that would affect the noise level at very low frequencies, the polyester capacitors C_{A1}, together with C_{A2}, represent the largest size components employed in the design. The second stage, because of the large gain of the first stage (40 dB), does not introduce a significant contribution to the overall equivalent input noise of the amplifier. Indeed, at frequencies above 100 mHz, the most important contribution of the second stage to the equivalent input noise of the entire amplifier comes from the EIVN of I_{A2} that, in the case of the INA 131, is about 30 nV/$\sqrt{\text{Hz}}$ ($f=1$ Hz) and 12 nV/$\sqrt{\text{Hz}}$ ($f>30$ Hz). The contribution to the EIVN of the entire amplifier is, therefore, in the order of 300 and 120 pV/$\sqrt{\text{Hz}}$ at $f=1$ Hz and for $f>30$ Hz, respectively.

For obtaining a very low EIVN for the first stage, we resort to the very large area JFET transistors pair IF3602 by Interfet as the first stage of a low noise operational amplifier (LNOA, gray area in Fig. 1) that is used, in turn, for realizing an ac input coupled voltage amplifier with a gain approximately equal to $1+R_2/R_1$. The JFETs IF3602 are characterized by a very low EIVN (0.4 nV/$\sqrt{\text{Hz}}$ and below 0.3 nV/$\sqrt{\text{Hz}}$ at $f=10$ Hz and for $f>100$ Hz, according to the manufacturer datasheet) and a high transconductance gain ($g_m=70$ mA/V for a drain current $I_D=4$ mA). Typical pinch off voltages for the IF3602 fall in the range between −1.5 and −0.5 V and the reverse gate current in the active region of operation at room temperature is below 10 pA, provided that the drain to source voltage is maintained below 4 V. The amplifier is supplied with $V_{DD}=V_{SS}=12$ V by means of lead acid batteries. With $R_{SS}=1.65$ kΩ obtained as the parallel of two 3.3 kΩ $\frac{1}{4}$ W metallic film resistor in order to reduce the power dissipated by each one of them, the bias current for each JFET is about 4 mA regardless of the actual value of the pinch off voltage of the particular device that is being employed. The noise introduced by the resistance R_{SS} (both thermal noise and flicker noise) is rejected by the differential configuration of the input stage. The resistors R_{D1} and R_{D2} have a resistance value of 2 kΩ, thus providing for a drain to source voltage drop below 4 V. Each resistor R_D is obtained as the parallel of five 10 kΩ, 1/8 W metallic film resistors in order to reduce to a negligible level their flicker noise contribution at very low frequencies. The instrumentation amplifier INA131 (I_{A1}) acts as a gain stage providing for a factor 100 in the open loop gain of the LNOA. The INA131 is characterized by a dominant pole at $f_{\text{INA}}=70$ kHz and, therefore, by neglecting for the time being the presence of the series of R_C and C_C, the open loop gain of the LNOA can be approximated as follows:

$$A_{\text{VLN}}=\frac{A_{\text{VLN0}}}{1+s\tau_{\text{INA}}};\quad A_{\text{VLN0}}=g_mR_DA_{\text{DINA}};$$
$$\tau_{\text{INA}}=1/(2\pi f_{\text{INA}});\quad R_D=R_{D1}=R_{D2}, \tag{1}$$

where $A_{\text{DINA}}=100$ is the low frequency gain of I_{A1}.

In the operating conditions detailed above, the value of A_{VLNO} is about 14×10^3, resulting in a gain product bandwidth of 1 GHz. With such a high value, the parasitic capacitances introduced by the JFETs and by the other devices in the circuit can easily result in instability. The series connection R_C and C_C is used for implementing a pole-zero compensation. With $R_C=68$ Ω and $C_C=33$ nF, a zero at $f_0=1/(2\pi R_CC_C)=70$ kHz and a pole at $f_C=1/(2R_DC_C)=1.2$ kHz are introduced: the zero removes the effect of the pole introduced by I_{A1}, while the pole at f_C becomes the dominant pole, thus setting the gain bandwidth product at about 17 MHz. With such a compensation, stability of the first stage is obtained with a flat response that extends up to a few kHz. As far as the gain of the first stage is concerned, if we were to assume the virtual short circuit approximation at the input of the LNOA, a gain equal to $(1+R_2/R_1)=101$ would be expected. However, this is not the case with the amplifier we are designing. Indeed, the loop gain G_L of the first stage, that can be calculated form the input of I_{A1} to the output of the JFET differential stage, is not very large although it can be considered to be constant up to about 1 kHz. We have

$$G_L=A_{\text{DINA}}\left(\frac{R_1}{R_1+R_2}\right)g_mR_D\approx g_mR_D\approx 140. \tag{2}$$

Hence, in the pass band of the first stage, the actual voltage gain A_{V1} is

$$A_{V1}=\left(1+\frac{R_2}{R_1}\right)\frac{G_L}{1+G_L}\approx 101\times 0.993=100.3. \tag{3}$$

Therefore, from now on, we will assume the voltage gain of the first stage to be equal to 100. Note that errors as large as 20% in the actual value of the product g_mR_D would result in the gain of the first stage to remain within the range from 100.1 to 100.4.

Before discussing the noise performances of the first stage, we need to take into account the effect of the relatively large offset voltage introduced by the differential JFET stage. It is indeed the need for compensating such an offset that sets a maximum to the voltage gain of the first stage. The offset voltage of a few IF3602 belonging to the same lot is reported in Fig. 2 as a function of the bias current. As it is apparent, offset voltages as large as 50 mV are obtained and, according to the datasheet, a maximum of 100 mV can be expected. Because of the dc connection between the output of I_{A1} to the rightmost gate of the IF3602 in Fig. 1, the maximum offset that can be tolerated depends on the ratio R_1/R_2 and on the

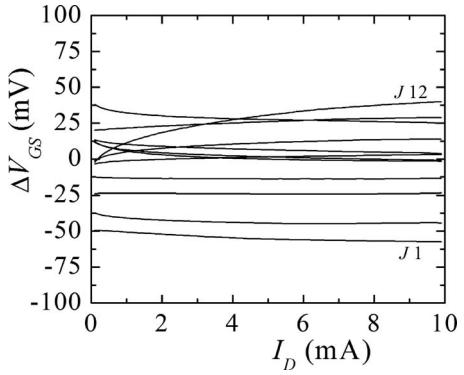

FIG. 2. Offset voltage of a few IF3602 belonging to the same lot as a function of the bias current.

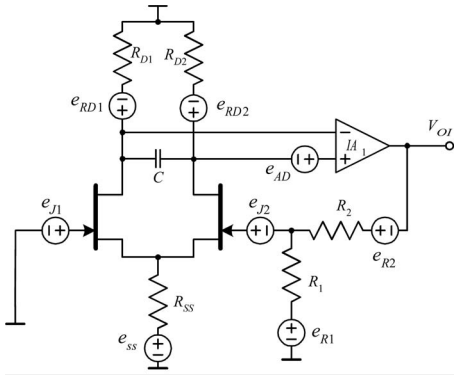

FIG. 3. Equivalent circuit of the first stage of the amplifier in Fig. 1 for EIVN estimation.

maximum voltage V_M at the output of the instrumentation amplifier. With a power supply of ± 12 V, the maximum voltage at the output of I_{A1} is in the order of 10 V, thus setting to about 1/100 the minimum value of R_1/R_2 and this, in turn, results in a maximum gain of 100 for the first stage. In the case in which the offset voltage of the JFET input pair approaches its maximum value, a relatively large current flows across the series of R_1 and R_2 (R_1 is set to 10 Ω for reasons that will become clear in the following). For this reason, R_1 and R_2 are high quality wire wound resistors, in such a way as to contribute a negligible level of excess low frequency noise.

An input high pass (HP) filter (C_{A1},R_{A1}) is employed in order to filter out the dc component across the DUT that would otherwise cause the saturation of the first stage. The corner frequency of this filter is much lower than that of the HP filter employed between the first and the second stage. Indeed, the voltage noise generated by the resistance R_{A1} does directly contribute to the EIVN of the amplifier. It can easily be calculated that, at frequencies much higher than the corner frequency and assuming a DUT impedance much lower than R_{A1}, the contribution to the EIVN is

$$S_{\mathrm{VRA1}} = 4KTR_{A1}\frac{f_C^2}{f^2}, \tag{4}$$

where K is the Boltzmann constant, T the absolute temperature, f is the frequency, and $f_C = 1/(2\pi R_{A1}C_{A1})$ is the corner frequency of the HP filter. Since, as we have noted before, a polyester capacitor has to be used for C_{A1}, its capacitance value is limited to a few tens of μF for its physical size to be reasonable. With $C_{A1}=22$ μF, that is the largest easily available commercial value for this type of capacitors, it is apparent, from Eq. (4) and from the definition of the corner frequency f_C, that the larger the resistance R_{A1}, the lower the noise at any given frequency. At the lowest design frequency (100 mHz) we obtain that with $R_{A1}=3.3$ MΩ the noise contribution of the input HP filter is less than 3×10^{-18} V^2/Hz (1.7 nV/$\sqrt{}$Hz), that is much lower than the contribution of the EIVN of the JFETs at the same frequency (in the order of 100×10^{-18} V^2/Hz or 10 nV/$\sqrt{}$Hz). Because of the frequency dependence of the noise spectrum in Eq. (4), at frequencies higher than 100 mHz, the noise contribution of the HP filter becomes negligible. Note that a similar problem exists, in principle, in the case of the HP filter separating the first and the second stage. In this case, however, its noise contribution to the EIVN of the entire amplifier is attenuated by 40 dB (the gain of the first stage). It must be noted that, with the selected values of C_{A1} and R_{A1}, a time constant of 220 s is obtained, and this implies a settling time for the system in the order of a few min, depending on the size of the voltage step at the input of the amplifier that occurs when a DUT is connected. Such a long settling time is fully acceptable as a much longer averaging time is required in order to obtain a reliable estimation of the DUT noise spectrum down to 100 mHz. Should one not be interested into such a low frequency limit, the HP corner frequencies of the two HP filters could be risen in order to reduce the settling time.

The estimation of the EIVN of the first stage can be obtained with reference to the equivalent circuit in Fig. 3. In order to simplify the discussion, we have assumed a simple dominant pole compensation ($R_C=0$). As we have noted before, the EIVN of the first stage essentially coincides with that of the entire amplifier. In the equivalent circuit of Fig. 3 the following assumptions have been made:

- No significant noise contribution comes from the input HP filter. This assumption is justified at frequencies above 100 mHz, as we have noted above.
- No significant excess noise contribution comes from the resistances R_{D1} and R_{D2}. This assumption is justified by the fact that each R_D is obtained as the parallel of five low excess noise metallic film resistors.
- No significant excess noise comes from the resistances R_1 and R_2. This assumption is justified by the fact that high quality wire wound resistors have been used for R_1 and R_2.
- The noise contribution by the resistance R_{SS} (e_{ss} in Fig. 3) can be neglected. This assumption is justified by the differential configuration of the LNOA that rejects common mode noise signals.
- The noise contribution of the equivalent input current noise (EICN) sources of I_{A1} can be neglected. Indeed, we observe that in the circuit configuration in Fig. 3 their effect is equivalent to an additional voltage noise source in series with the EIVN source of I_{A1} with an equivalent voltage noise power that, at frequencies below the pole compensation frequency, is about $S_{VI}=S_I R_D^2$ (S_I is the power spectrum of the EICN sources). It can easily be shown, either by direct measurements or by resorting to the speci-

fications of the INA131, that S_{VI} is always much lower than the power spectrum of the EIVN source of the amplifier. As an example, at $f=10$ Hz, S_I is about 1.6×10^{-25} A^2/Hz, resulting in an $S_{VI}=6.4\times10^{-19}$ V^2/Hz: this value is negligible with respect to the EIVN of the INA131 that, at the same frequency, is about 2.5×10^{-16} V^2/Hz.

- All noise sources in Fig. 3 are uncorrelated.

With the above assumptions, the power spectrum S_{BN} of the EIVN source of the amplifier can be readily calculated. Let S_{J1} and S_{J2} be the power spectral densities of the EIVN sources e_{J1} and e_{J2} of the JFET; let S_{Rx} be the power spectral density of the noise source e_{Rx} due to the resistance R_x; finally, let S_{AD} be the power spectrum of the EIVN source e_{AD}. Because of the symmetry of the circuit we have

$$S_{J1}=S_{J2}=S_J; \quad S_{RD1}=S_{RD2}=S_{RD}. \tag{5}$$

S_{BN} can be calculated as

$$S_{BN}=2S_J+\frac{1}{(g_mR_D)^2}\left[2S_{RD}+S_{AD}\left(1+\frac{f^2}{f_C^2}\right)\right]+S_{R1}\left(\frac{R_2}{R_1+R_2}\right)^2+S_{R2}\left(\frac{R_1}{R_1+R_2}\right)^2. \tag{6}$$

Since

$$S_{R1}=4KTR_1; \quad S_{R2}=4KTR_2; \quad R_2\gg R_1 \tag{7}$$

we have

$$S_{R1}\left(\frac{R_2}{R_1+R_2}\right)^2+S_{R2}\left(\frac{R_1}{R_1+R_2}\right)^2=4KT(R_1\parallel R_2)\approx4KTR_1. \tag{8}$$

Moreover

$$\frac{2S_{RD}}{(g_mR_D)^2}=\frac{2\times4KTR_D}{(g_mR_D)^2}=4KTR_{\mathrm{eq}}; \quad R_{\mathrm{eq}}=\frac{2}{g_m^2R_D} \tag{9}$$

and since $R_{\mathrm{eq}}\ll R_1$ ($\mathrm{Req}\approx0.2$ Ω), the noise contribution coming from the resistances R_D can be neglected with respect to that due to R_1. Therefore, we have that the spectrum of the EIVN of the amplifier can be approximated as follows:

$$S_{BN}=2S_J+\frac{S_{AD}}{(g_mR_D)^2}\left(1+\frac{f^2}{f_C^2}\right)+4KTR_1. \tag{10}$$

A plot of the three terms contributing to S_{BN}, as can be directly estimated from the typical noise performances reported in the data sheets (INA131) and from direct measurements on the JFET devices, are reported in Fig. 4. The way in which it has been possible to perform a direct measurement of the EIVN of a typical JFET will be discussed in the section devoted to the experimental results. From Fig. 4, where the resulting expected S_{BN} of the new amplifier is also reported, the following conclusions can be drawn:

- At very low frequencies ($f\ll1$ Hz) S_{BN} is expected to coincide with that introduced by the JFET pair, since the other contributions are negligible.
- In the frequency range between 1 Hz up to 1 kHz, S_{BN} is mainly due to the noise introduced by the JFETs and by the feedback resistor R_1. In principle, it could be possible to reduce S_{BN} by employing an even lower value for R_1. However, values of R_1 below 10 Ω would make to accurately set the gain of the first stage quite difficult because of the influence of parasitic resistances. Besides, since R_2 should be decreased accordingly, there would be the risk of exceeding the maximum current that can be delivered by the output of I_{A1} in the case of large input offsets. With $R_1=10$ Ω we can expect an equivalent input noise level in the order or below 1 $nV/\sqrt{Hz}$ which has to be regarded as an excellent result.
- At frequencies higher than 1 kHz, the noise introduced by the EIVN of I_{A1} becomes dominant. This is due to the fact that, because of compensation, the voltage gain of the JFET input stage is being reduced at high frequencies. This noise increase at frequencies above 1 kHz is not important in an amplifier that has been designed with the target of obtaining very good noise performances at very low frequencies. It should be noted, however, that at 10 kHz the expected equivalent input noise is still in the order of 1 $nV/\sqrt{Hz}$.

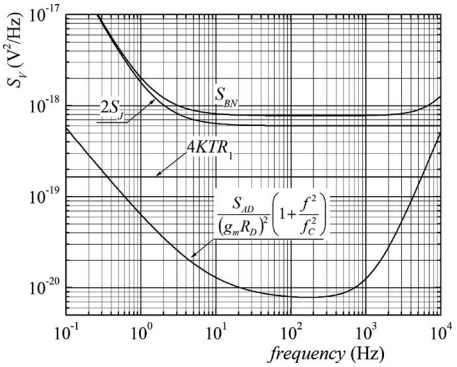

FIG. 4. Contributions and total EIVN spectrum (S_{BN}) of the amplifier.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Four amplifiers have been built according to the schematic in Fig. 1 and to the design guidelines discussed above. In all the cases almost identical noise performances have been obtained with the targeted gain of 80 dB without any adjustment or calibration. This is in itself a remarkable result since it proves that the design, as it was expected, is robust with respect to the quite widespread JFET characteristics. For signal acquisition and spectra estimation, we used a spectrum analyzer that employs a National Instruments PCI-4451 two channels DSA board.

A typical EIVN spectrum is reported in Fig. 5. As it can be observed, the experimental results are in quite good agreement with what was expected form the design. In the same figure, the equivalent input noise when 1 and 10 kΩ 0.1% resistors are connected at the input of the amplifier is reported. In all cases, the EIVN was calculated by subtracting exactly 80 dB from the measured output voltage noise. Figure 5 demonstrates that the gain is indeed the expected one and that it is flat in the explored frequency range. The very same measurements results are reported in Fig. 6 in the

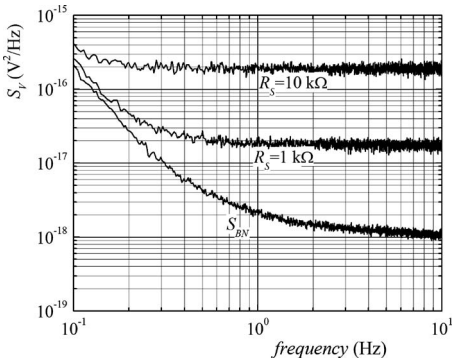

FIG. 5. A typical EIVN spectrum of the amplifier. The equivalent input noise when a 1 and 10 kΩ 0.1% resistors are connected at the input of the amplifier is also reported (S_{BN} is not subtracted).

frequency range between 100 Hz and 40 kHz. As it can be observed, the EIVN of the amplifier increases at frequencies above a few kHz, as it was expected. However, the usable flat bandwidth of the amplifier, as it can be deduced from the noise measurements on the 1 kΩ and the 10 kΩ resistors, extends above 10 kHz. The slight increase of the spectrum at high frequencies for the case of the 1 kΩ input termination results form the combination of the increase of S_{BN} and the proximity of the bandwidth limit of the amplifier. The fact that the bandwidth limit is being reached is apparent from the spectrum relative to the 10 kΩ resistance. From the measured spectra it is also apparent that no detectable contribution to the noise comes from the equivalent input current noise source of the amplifier. When increasing the source impedance up to a value that is no longer negligible with respect to R_{A1}, a partition of the source noise due to the very presence of R_{A1} is to be expected. Moreover, the noise contribution coming from R_{A1} may not be negligible any longer. When dealing with very high source impedances it is possible, in principle, to increase the value of R_{A1} for reducing the input voltage partition and its noise contribution. However, for increasing source resistances, it is expected that the EICN at the input of the JFET will eventually become detectable and will contribute to the background noise of the measurement system in which the preamplifier is employed. In the attempt of estimating the current noise at the input of the amplifier we removed the capacitor C_{A1} and performed noise measurements by replacing R_{A1} with larger and larger

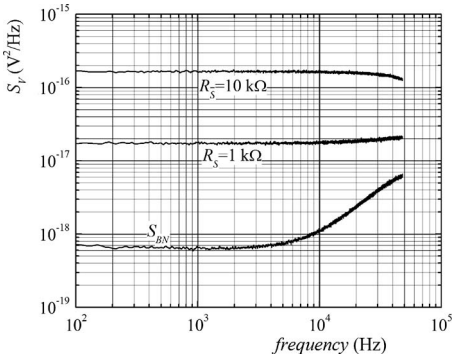

FIG. 6. Results of the very same measurements reported in Fig. 5 in the frequency range between 100 Hz and 40 kHz. As in Fig. 5, S_{BN} has not been subtracted.

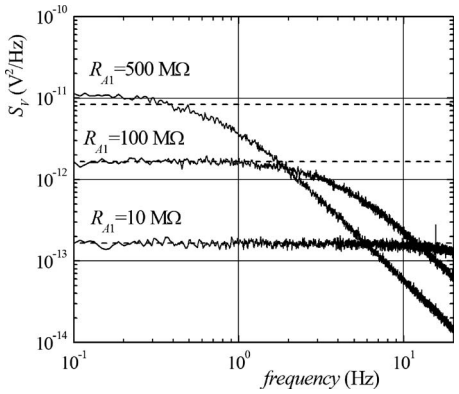

FIG. 7. Input referred voltage noise with 10, 100, and 500 MΩ source resistances. The dashed lines represent the thermal noise contribution for each resistance value. Only in the case of the 500 MΩ resistance, excess noise due to the contribution of the equivalent input current noise source of the input JFET can be clearly detected.

precision (1%) resistors. The effect of the EICN at the gate of the JFET is expected to appear as excess noise superimposed to the thermal noise of the resistors, the level of the EIVN of the amplifier being negligible in the case of such large resistances. We expect the input referred voltage noise S_{VEQ} to be given, in these conditions, by

$$S_{VEQ} = 4KTR_{A1} + S_{IJ}R_{A1}^2, \tag{11}$$

where S_{JI} is the power spectral density of the EICN source at the gate of the JFET. The results of the measurements of S_{VEQ} for R_{A1}=10 MΩ, R_{A1}=100 MΩ, and R_{A1}=500 MΩ are reported in Fig. 7. As a first observation, we notice that for large source resistances the bandwidth of the amplifier appears to be considerably reduced. Indeed, this is not the case as the apparent reduction in the bandwidth is the result of the noise attenuation due to the amplifier input capacitance. This capacitance, from the very noise measurements in Fig. 7, can be estimated to be of about 400 pF. As a second observation, we notice that up to 100 MΩ the contribution of the EICN is negligible with respect to the thermal noise of the resistors. Only in the case of R_{A1}=500 MΩ some excess noise is detected before the noise is attenuated because of the presence of the amplifier input capacitance. From the measured spectrum in the case of R_{A1}=500 MΩ and from Eq. (11) we can estimate S_I to be in the order of 4 fA/$\sqrt{\text{Hz}}$. Because of the limited input bandwidth, we cannot draw definite conclusion on the value of S_{IJ} for larger frequencies, but it is expected that it either decreases (below 1 Hz we may be exploring the $1/f$ region of the current spectrum) or it remains constant. Even assuming that S_{IJ} remains constant in the entire bandwidth of the amplifier, its contribution to the input referred voltage noise would remain below 1 nV/$\sqrt{\text{Hz}}$ for DUT impedances as large as 250 kΩ.

As an application example of the new amplifier, we report the results that were obtained in the noise characterization of the very JEFTs that are used in the first stage of the amplifier. One way of obtaining a direct measurement of the EIVN of a JFET in the very same bias conditions in which it operates in the new amplifier is to resort to the circuit in Fig. 8. The voltage noise at the source terminal essentially coincides with the EIVN of the JFET. The noise generated by R_D

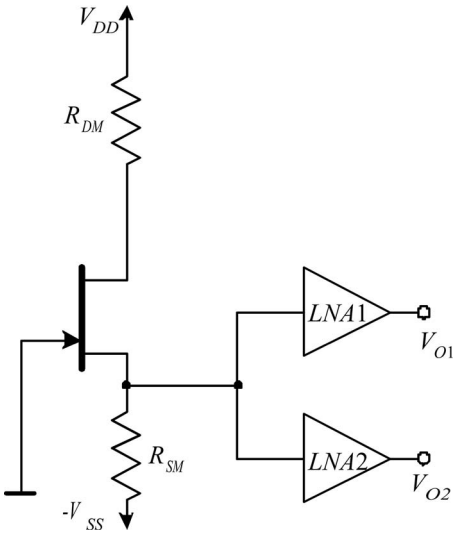

FIG. 8. Circuit topology employed to obtain an estimation of the EIVN of a JFET in the very same bias conditions in which it operates in the new amplifier by means of cross correlation.

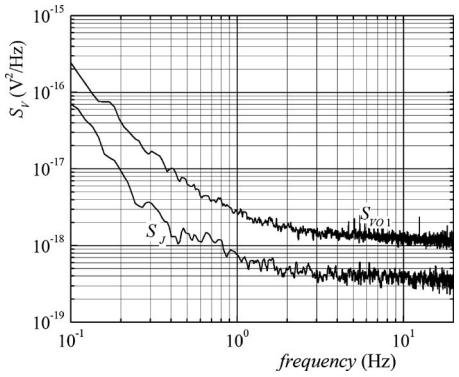

FIG. 9. Equivalent input voltage power spectrum at the input of one of the two preamplifiers employed to perform cross correlation measurements in Fig. 8 and estimated input cross spectrum. The cross spectrum provides a direct estimate of the power spectrum of the EIVN of one single JFET in the IF3602 differential pair.

is rejected by the very high drain output impedance, while the noise generated by R_{SM} is "shorted" by the very low source output impedance (in the bias conditions we are interested in, the source output impedance is in the order of $1/g_m$, that is about 14 Ω). The drain and source resistances are selected in such a way as to have the JFET operating in the same conditions as in the circuit in Fig. 1 ($R_{DM}=R_D$; $R_{SM}=2R_{SS}$). As the noise to be measured is below the equivalent input noise of the new amplifier, we resorted to a double channel measurement chain in order to make it possible to estimate the source noise by means of cross correlation. The cross correlation method is a very well established approach for the estimation of noise levels below that of the background noise of the voltage preamplifiers that are available.[13] By resorting to cross correlation it is possible, in principle and provided that the effect of the equivalent input current noise of the employed preamplifiers can be neglected, to perform accurate noise measurements of very low noise levels regardless of the magnitude of the EIVN of the preamplifiers. However, the measurement time that is required in order to extract the correlated component (S_C) from the uncorrelated ones (S_{UC}) is a strongly increasing function of the ratio S_{UC}/S_C.[13] Therefore, also in the case of cross correlation measurements, in order to take full advantage from the technique, it is mandatory to resort to preamplifiers with the lowest possible level of background noise. For this reason we employed two of the prototypes of the new preamplifier discussed in this paper. The equivalent voltage power spectrum at the input of one of the two preamplifiers is reported in Fig. 9 together with the estimated cross spectrum obtained by analyzing a time record of about 1 h. It can be noted that, according to the results of the measurements, of the EIVN of the JFET, a slightly lower background noise level should be obtained for the preamplifiers in the frequency range above 1 Hz. This difference, however, can be considered to be compatible with the dispersion of the noise characteristics among JFETs belonging to the same lot, as was also observed by other researchers.[14]

IV. CONCLUSIONS

In this paper we have addressed the problem of the design of a very low noise voltage preamplifier that, thanks to a very simple circuit configuration, to a very low component count and to its intrinsic robustness with respect to the parametric deviations of the discrete devices that are employed, can be easily reproduced by any researcher involved in the field of low frequency noise measurements. We believe that we have succeeded in the task, as the circuit we propose employs just three active components (a JFET differential pair and two identical instrumentation amplifiers) and a few passive components. All the circuit components, possibly with the exception of the JFETs, can be easily obtained from any general distributor of electronic components at a very low cost. Once the circuit is built, no adjustment or calibration is needed as the voltage gain is guaranteed by design to be 10 000 (80 dB) with an error less that 0.5% and the background noise in the low frequency range essentially coincides with that introduced by the JFETs. Notwithstanding the very simple topology and the very low cost, the noise performances of the proposed JFET input preamplifier are among the best ever reported in the literature and are much better than those that can be obtained by employing commercial instrumentation. Indeed, noise levels as low as 14 nV/$\sqrt{\text{Hz}}$ (100 mHz), 1.4 nV$\sqrt{\text{Hz}}$ (1 Hz), 1.0 nV$\sqrt{\text{Hz}}$ (10 Hz), and 0.8 nV$\sqrt{\text{Hz}}$ (1 kHz) were consistently obtained in all the prototypes that were build, tested, and employed for actual measurements in our laboratories. Proper measurements for estimating the contribution of the equivalent input current noise source of the input JFET have allowed to conclude that no significant contribution to the background noise is to be expected for source impedances in excess of 100 kΩ.

[1] R. Landauer, Nature (London) **392**, 658 (1998).
[2] L. K. J. Vandamme, IEEE Trans. Electron Devices **41**, 2176 (1994).
[3] C. Ciofi and B. Neri, J. Phys. D: Appl. Phys. **33**, R199 (2000).
[4] N. Labat, N. Malbert, C. Maneux, and A. Touboul, Microelectron. Reliab. **44**, 1361 (2004).
[5] C. Ciofi, G. Giusi, G. Scandurra, and B. Neri, Fluct. Noise Lett. **4**, L385 (2004).

[6] C. Ciofi, M. De Marinis, and B. Neri, IEEE Trans. Instrum. Meas. **46**, 789 (1997).
[7] Vas. P. Kunets, T. Al. Morgan, Yu. I. Mazur, V. G. Dorogan, P. M. Lytvyn, M. E. Ware, D. Guzun, J. L. Shultz, and G. J. Salamo, J. Appl. Phys. **104**, 103709 (2008).
[8] W. Kruppa, J. B. Boos, B. R. Bennett, N. A. Papanicolaou, D. Park, and R. Bass, IEEE Trans. Electron Devices **54**, 1193 (2007).
[9] Z. Çelik-Butler, S. P. Devireddy, H. Tseng, P. Tobin, and A. Zlotnicka, Microelectron. Reliab. **49**, 103 (2009).
[10] B. Neri, C. Ciofi, and V. Dattilo, IEEE Trans. Electron Devices **44**, 1454 (1997).
[11] B. Neri, B. Pellegrini, and R. Saletti, IEEE Trans. Instrum. Meas. **40**, 2 (1991).
[12] F. A. Levinzon, IEEE Trans. Circuits Syst., I: Regul. Pap. **55**, 1815 (2008).
[13] M. Sampietro, G. Accomando, and G. Ferrari, Rev. Sci. Instrum. **70**, 2520 (1999).
[14] F. A. Levinzon, IEEE Trans. Instrum. Meas. **54**, 2427 (2005).