

Influence of local surface defects on the minority-carrier lifetime of passivating-contact solar cells

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ABSTRACT

Unlocking the full potential of passivating contacts, increasingly popular in the silicon solar cell industry, requires determining the minority carrier lifetime. Minor passivation drops limit the functioning of solar cells; however, they are not detected in devices with open-circuit voltages below 700 mV. In this work, simulations and experiments were used to show the effect of localized surface defects on the overall device performance. Although the defects did not significantly affect lifetime measurements prior to electrode deposition or open-circuit voltage measurements at standard-test conditions, they had a significant impact on the point of operation and, in turn, device efficiency (up to several percent efficiency drop). Furthermore, this study demonstrates that localized defects can have a detrimental effect on well-passivated areas located several centimeters away through electrical connection by the electrode. This leads to a low-injection lifetime drop after electrode deposition. Thus, commonly measured lifetime curves before metallization (and therefore internal voltage) are usually not representative of their respective values after metallization. The low-injection lifetime drop often observed after electrode deposition can be derived from such local surface defects and not from a homogeneous passivation drop.

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Good surface passivation is essential in monocrystalline silicon solar cell technologies as it enables taking full advantage of high-purity wafers.^{1,2} Lifetime spatial non-uniformity is common in multicrystalline silicon (due to bulk variations)^{3,4} and for monocrystalline devices with local contacts between the wafer and metallization.⁵ Parasitic effects, such as shunts, localized recombination centers, or edge recombinations, are known to specifically affect the low-injection (typically below a minority carrier density of 10^{15} cm^{-3}) lifetime of silicon-based devices^{3–7} as well as undiffused monocrystalline silicon wafers passivated with charged dielectrics.⁸ The interconnection of such defects with the remaining (well-passivated) device area can furthermore strengthen their detrimental influence.^{5,9} The lifetime of solar-cell devices with passivating contacts (consisting of a continuous stack separating the metal electrode from the wafer) is usually characterized in terms of the homogeneous lifetime, using a unique recombination parameter (J_0) value.¹⁰ Surface passivation is typically followed by monitoring the effective lifetime via photoconductance decay measurements,¹¹ assuming that passivation occurs homogeneously.

In silicon solar cells, passivation is typically achieved by applying intrinsic amorphous silicon or silicon oxide thin films,^{10,12,13} whereas carrier selectivity usually relies on the work function of a layer of

doped silicon¹⁴ or other material.¹⁰ In such thin films, spatial passivation non-uniformities are likely to occur (e.g., a speck of dust, scratch, or inhomogeneous wet-chemistry). This can be relevant as recombination in high-efficiency devices is limited by the surface (besides inherent Auger recombination).

This study shows that small defects in passivating contact stacks can cause performance drops of up to a few percent; therefore, it may prevent future data misinterpretation and incorrect optimization procedures. Additionally, the influence of defects interconnecting through the electrode is discussed. Although this work focuses on silicon heterojunction solar cells (and uses the corresponding terminology), these observations also apply to other passivating-contact technologies, including tunnel-oxide-based and dopant-free approaches.

A schematic of the used device can be seen in Fig. 1(a), and Fig. 1(b) shows its modelization as an array of parallel elements connected through a sheet resistance R_{ITO} , similar to models of multi-crystalline devices or homojunction cells with localized contacts.^{15–19} Each element includes a current generator, three diodes to account for bulk, surface and Auger recombination, and a series resistance R_s accounting for the contact resistance between the conductive sheet and the absorber. A one-dimensional array (parallel to the solar cell plane) is

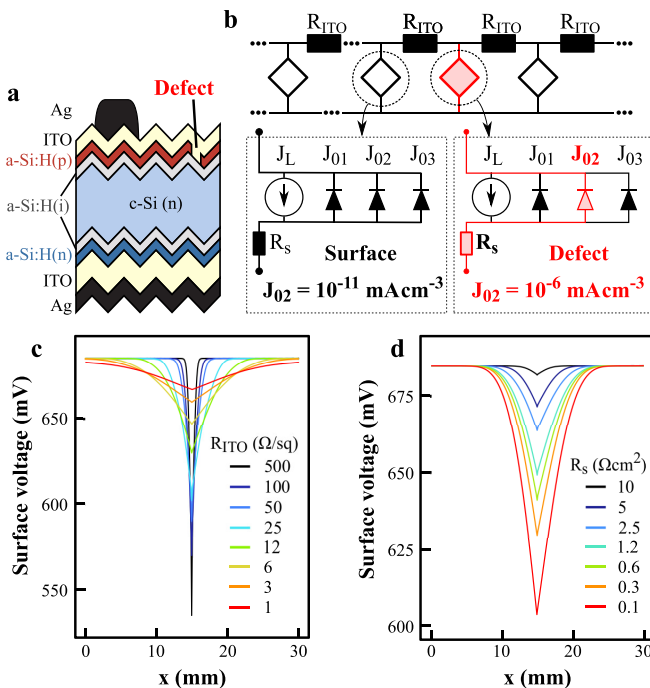


FIG. 1. (a) Schematic of the devices studied here consisting of a crystalline silicon absorber, intrinsic, p-type and n-type amorphous silicon for the contacts, and indium tin oxide and silver for the electrode. (b) Equivalent circuit for the simulations of localized defects; only J_{02} is changed between good areas and defects. (c) and (d) Simulated effect on the surface voltage at 0.05 sun of a single local defect as a function of the (c) surface sheet resistance (R_{ITO}) (d) series resistance (R_s). $R_s = 0.3 \Omega \text{ cm}^2$ in (c) and $R_{ITO} = 10 \Omega$ in (d).

assumed for simplicity. This one-dimensional nature describes an infinite linear defect and would not accurately describe a point defect with a radial current spreading symmetry, which would require a two-dimensional finite-element treatment.^{18,19} However, similar trends and conclusions are expected. Furthermore, as the solar cell thickness is aggregated in the diode model, diffusion within the c-Si bulk is not accounted for, making this approach inaccurate for sub-millimeter-scale analysis.

Most elements in the array have “good” properties, which were obtained by fitting the current–voltage (JV) characteristics of an experimental solar cell with an open-circuit voltage, V_{oc} , of $\sim 730 \text{ mV}$. One or a few elements in the array have “defect” properties, which were obtained by fitting the JV curve of a poor device showing $\sim 540 \text{ mV}$ of V_{oc} . This is considered as the representative of a zone with very poor passivation, possibly resulting from the presence of dust on the surface during deposition, scratches or inhomogeneous film-deposition during processing, broken pyramid, etc.

Figures 1(c) and 1(d) show the impact of sheet resistance (R_{ITO}) and contact resistance (R_s) on the local surface voltage around a localized defect. A photocurrent (J_L) corresponding to an illumination of 5 mW/cm^2 (0.05 sun) was chosen to be representative of the injection level at the maximum power point (MPP) in standard test conditions.²⁰ Decreasing R_{ITO} distributes the detrimental influence of the defect over a larger area and reduces the local voltage drop.

Decreasing R_s enlarges the range of influences of the defect, as well as the local surface voltage drop, as more charges can flow through the defect.²¹ Although the device is in the open circuit, in both cases, the current flows from the good area through the conductive sheet toward the defect. The diodes’ properties of the defect dictate the local potential. The local absence of the p-aSi:H layer could be such a defect, which is well represented by a diode (since the i-aSi:H/ITO stack acts as a Schottky contact) with a very high dark saturation current, J_{02} .

Figure 2 presents the impact of homogeneous distribution of localized defects with a small coverage fraction of 0.3%. Figure 2(a) shows a simulation of the lifetime curve that would be measured for such a device. The data were extracted from surface voltage simulations considering variable-illuminations (hence variable photocurrents), in the open circuit, as is done in “Suns-Voc” measurements.²² The average voltage over the entire array was determined (as commonly done) to obtain a unique value, despite spatial variations.^{23,24} Figures 2(b) and 2(c) show the spatial voltage variation for 0.05-sun ($\sim \text{MPP}$) and 1-sun illumination, respectively. Three values are compared for R_{ITO} , which are representative of a device without any electrodes (then the inversion layer at the p–n interface still leads to a conducting sheet of $\sim 10\,000 \Omega/\text{sq}$,^{25,26} with only a transparent conducting layer (for which $100 \Omega/\text{sq}$ is a usual value²⁷), and after metallization ($5 \Omega/\text{sq}$).²⁸

Figure 2(a) shows that the introduction of defects has a negligible effect on the lifetime curve when assuming a high R_{ITO} value (i.e., prior to any electrode deposition), implied V_{oc} (iVoc), and implied fill-factor (iFF) values equivalent to the no-defect case (728 mV and 87.3%, respectively). However, there is a severe lifetime drop, specifically at low injection, when decreasing the sheet resistance of the electrode. Hence, iFF drops to 86.8% (respectively, 84.6%) for R_{ITO} of $100 \Omega/\text{sq}$ (respectively, $5 \Omega/\text{sq}$). Nonetheless, iVoc is almost unaffected (727 mV and 725 mV, respectively). This phenomenon will more strongly affect the device performance at low-injection (FF under low irradiation) and, in turn, the energy yield.²⁹ In these simulations, only R_{ITO} was changed, with the lifetime drop deriving solely from the lateral spreading of the influence of the defects, as discussed in Fig. 2 and shown in Figs. 3(b) and 3(c).

Experimental observations of such curves during operation could be misinterpreted, e.g., as passivation deterioration introduced by ITO

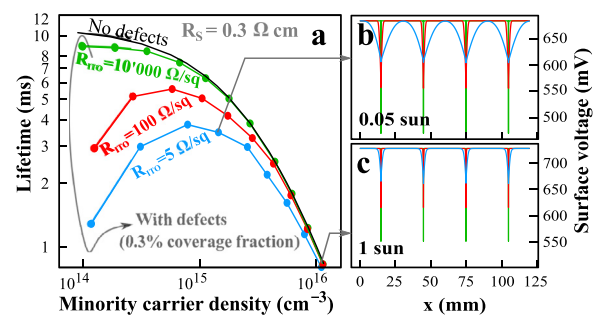


FIG. 2. (a) Lifetime curves simulated from the 1D array with various sheet resistances for the interconnection, representative of the state prior to any electrode deposition ($10\,000 \Omega/\text{sq}$, corresponding to R_{sheet} of the inversion layer), after ITO ($100 \Omega/\text{sq}$), and after metal grid ($5 \Omega/\text{sq}$, reasonable estimate since the grid is not a homogeneous sheet). (b) and (c) Surface voltage at two illumination levels for the three different R_{ITO} values.

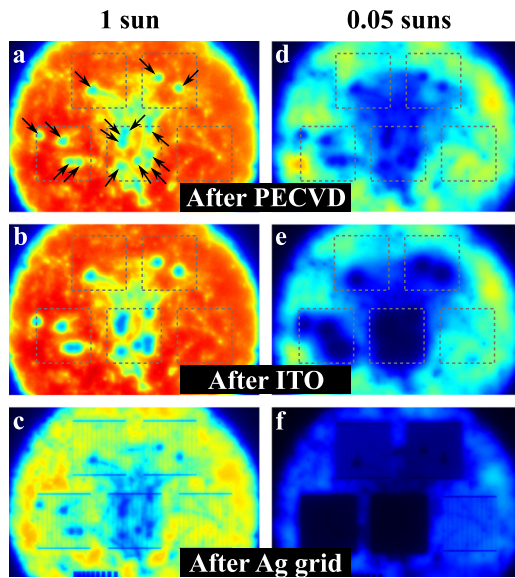


FIG. 3. Photoluminescence images at 1 sun (a)–(c) and 0.05 sun (d)–(f) of $2 \times 2 \text{ cm}^2$ solar cells' wafer prior to any electrode deposition (a) and (d), after ITO (b) and (e), and after the metal grid (c) and (f). Especially engineered localized defects are indicated by arrows in a, and dashed gray squares illustrate the position of the solar cells.

deposition (sputter damage^{30,31}) or metallization when, in this case, these steps actually only reveal some pre-existing passivation issues. Moreover, as increasing R_{ITO} or R_{S} mitigates the spreading of local passivation non-uniformity [Figs. 1(c) and 1(d)], applying an electrode with a high sheet resistance or yielding a high contact resistance would limit the lifetime drop shown in Fig. 2(a). This could be misinterpreted as improved electrode processing, only requiring fine tuning to decrease series resistance. However, such fine tuning would annihilate the advantage of this electrode as the poor electrical connection is the exact cause of the reduced lifetime drop. Finally, fitting the lifetime curves of Fig. 2(a) before and after ITO deposition (implicitly assuming a homogeneous passivation) would suggest variations in surface defect density and/or fixed charge.³² The phenomenon described here can provide alternative explanations to the experimental observations of a lifetime drop at low injection upon deposition of the transparent electrode.^{32–34} This also highlights the importance of ensuring good sample homogeneity and accounting for changes in minority-carrier sheet conductance when fitting lifetime curves.

To validate these simulation findings, $2 \times 2 \text{ cm}^2$ silicon heterojunction solar cells were fabricated using float-zone, $180\text{-}\mu\text{m}$ -thick, n-type ($2 \text{ }\Omega\text{cm}$) silicon wafers, textured by alkaline etching, as depicted in Fig. 1(a). Prior to plasma-enhanced chemical vapor deposition of the a-Si layers, an HF solution was used to remove the native oxide from the surfaces. The front indium tin oxide (ITO) and rear ITO/Ag layers were deposited by means of reactive sputtering and the front Ag grid using screen-printing. 0, 1, 2, 4, or 8 defective spots were achieved by introducing 1-mm^2 masks during the a-Si(p) layer deposition. Figure 3 shows photoluminescence images illustrating the impact of illumination and electrode sheet resistance on the range of influence of the local defects. At 1-sun illumination (Voc) [Figs. 3(a)–3(c)],

the defects can be seen individually on PL images. The addition of a $90 \text{ }\Omega/\text{sq}$ ITO layer [Fig. 3(b)], followed by the screen-printed metallization [Fig. 3(c)] enlarges slightly the area of influence of each local defect although this effect is negligible as can be expected from Fig. 1. At 0.05-sun illumination ($\sim\text{MPP}$), individual defects can also be observed prior to the deposition of electrodes [Fig. 3(d)]. However, when introducing a conducting electrode [Figs. 3(e) and 3(f)], the area of influence of each defect is enlarged, finally spreading to the entire cell area after metallization [Fig. 3(f)]. Notably, the no-defect cell (low-right) does not show any strong sputter-damage as the area within and outside the cell is similar in color. Furthermore, although the 4-defect-cell (low-left) is only locally impacted at 1-sun illumination, the whole cell area is impacted at MPP as seen in [Figs. 3(c) and 3(f)]. Table I confirms these findings with open-circuit voltage and fill factor (FF) values for each device.

Next, the influence of local surface defects was analyzed for defects located outside the probed area (and much further than the diffusion length). Tests showed that they also can affect lifetime measurements due to defect interconnection through the electrode. Figure 4(a) depicts the sample designed to probe such a scenario through the use of an annular mask during the deposition of the a-Si:H(p) layer. The lifetime was measured in the center of this wafer as well as in the center of a reference un-masked wafer, prior to and after deposition of a $480 \text{ }\Omega/\text{sq}$ ITO layer [Fig. 4(b)]. Almost no lifetime modification was observed upon ITO deposition for the unmasked sample; however, a severe drop at low injection was seen for the masked sample. This is similar to the observations of Tomasi *et al.*³³ although in our experiment this phenomenon only occurred when the annular mask was used. We, thus, attribute this effect to the interconnection of the probed area (still well passivated) with the remote low-passivation annular area.

This phenomenon can be reproduced with an equivalent circuit [overlaid on Fig. 4(a)] including a resistance-limited high-recombination diode. Such a kind of model was previously used to explain discrepancies in current-voltage behaviors of solar cells.⁹ Varying the resistance value enables reproducing the low-injection lifetime drop as shown in Fig. 4(c). In this graph, lifetime curves shown in Fig. 4(b) are overlaid, along with the measured lifetime of a third wafer, without any mask, before and after deposition of a $40\text{-}\Omega/\text{sq}$ ITO. In that case, a noticeable lifetime drop is still observed despite the absence of a mask. The ITO work function was expected to be fully screened as the a-Si(p) layer was four times the standard thickness. Although this phenomenon could stem from the presence of localized defects within the probed area, it could also originate from the connection of undesired poorly passivated areas on the wafer's periphery, be it the sample edge or tweezer marks from handling.^{8,35} This effect is similar to the one previously observed for homojunction devices with a highly conductive minority-carrier collector.^{9,36} Our study shows that it also applies to passivating contacts and should be considered when analyzing lifetime curves.

TABLE I. Voc and FF measured on the solar cells shown in Fig. 3.

#Defects	0	1	2	4	8
Voc (mV)	723	719	716	714	697
FF (%)	76.7	75.2	74.5	73.8	72.8

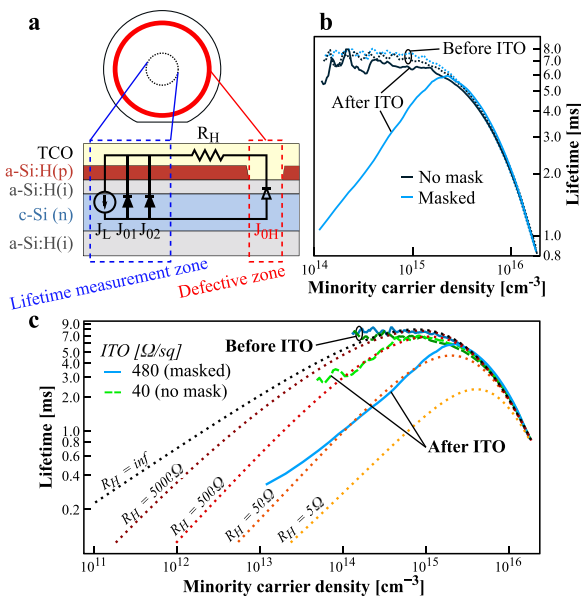


FIG. 4. (a) Top- and side-view sketch of a wafer prepared with a tailored, annular defective area. An equivalent circuit is overlaid on the side view. (b) Lifetime measured on such sample and an unmasked reference sample before and after deposition of a 480 Ω/sq ITO film. (c) The same data as b overlaid with lifetime curves simulated with the 3-diode model shown in (a), for various values of R_H . Green lines additionally show experimental data before/after ITO for an unmasked sample for an ITO sheet of 40 Ω/sq .

In conclusion, in this work, we showed the impact of local surface defects on the lifetime of silicon solar cells at various processing stages. It was observed that local surface defects have an insignificant effect on the lifetime prior to electrode deposition or on the Voc of a finished device. Simultaneously, the defects can affect the performance of high-efficiency devices through a reduction in internal voltage at the maximum power point. The interconnection of well-passivated and defective areas through the electrode leads to a lifetime drop at low injection, even for defects outside the probed area. This effect is reduced through increasing the contact resistance between the electrode and the wafer or the sheet resistance of the electrode. Although this work focused on silicon heterojunction technology, the studied phenomena also apply to devices using high-temperature passivated contacts, for which lower contact resistance values are reported.

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