On the electronic properties of a single dislocation

Manfred Reiche,[1,a)] Martin Kittler,[2,3] Wilfried Erfurth,[1] Eckhard Pippel,[1] Kornelia Sklarek,[1] Horst Blumtritt,[1] Angelika Haehnel,[1] and Hartmut Uebensee[4]
[1]*Max Planck Institute of Microstructure Physics, Weinberg 2, 06120 Halle (Saale), Germany*
[2]*IHP microelectronics, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*
[3]*IHP/BTU JointLab, K.-Wachsmann-Allee 1, 03046 Cottbus, Germany*
[4]*CIS Research Institute of Microsensorics and Photovoltaics, K.-Zuse-Str. 14, 99099 Erfurt, Germany*

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A detailed knowledge of the electronic properties of individual dislocations is necessary for next generation nanodevices. Dislocations are fundamental crystal defects controlling the growth of different nanostructures (nanowires) or appear during device processing. We present a method to record electric properties of single dislocations in thin silicon layers. Results of measurements on single screw dislocations are shown for the first time. Assuming a cross-section area of the dislocation core of about $1\,nm^2$, the current density through a single dislocation is $J = 3.8 \times 10^{12}\,A/cm^2$ corresponding to a resistivity of $\rho \cong 1 \times 10^{-8}\,\Omega$ cm. This is about eight orders of magnitude lower than the surrounding silicon matrix. The reason of the supermetallic behavior is the high strain in the cores of the dissociated dislocations modifying the local band structure resulting in high conductive carrier channels along defect cores. [http://dx.doi.org/10.1063/1.4876265]

I. INTRODUCTION

Dislocations are one-dimensional crystal defects. They influence many of the physical and mechanical properties of crystalline solids.[1,2] While some of them, for instance, mechanical properties (work hardening, etc.), are related to the generation and interaction of large numbers of dislocations, others, as electrical properties, are affected by only a few of the defects. This causes that individual dislocations might have detrimental impacts on electrical parameters of semiconductor devices, in particular, if scaling reduces device dimensions below 20 nm. Here, especially the integration of dissimilar materials into specific device regions is a main reason for defect generation. For instance, high mobility channel materials, as Ge, SiGe, or III–V compounds, are integrated[3,4] having different lattice constants to the substrate, which results in high local strains and may induce the generation of dislocations. Therefore, the knowledge about the electronic structure of individual dislocations is an important issue for next generation nanodevices.

Electronic properties of dislocations were intensively studied for a long time using numerous analytical techniques[5–9] requiring, however, high densities of dislocations to attain the detection limits of the methods. The dominantly applied method for dislocation generation was plastic deformation introducing also large numbers of other defects and defect reactions making it sometimes difficult to interpret experimental data.[7] In order to avoid interactions between dislocations or between dislocations and other defects, methods are required allowing the formation and analyses of only a few dislocations or, in the ideal case, of a single dislocation. There are some early investigations which showed only the diode character of an individual edge dislocation running through a whole wafer.[10–12] Recent studies have drawn a more detailed picture indicating that dislocations possess some exceptional electronic and optical properties induced by their small dimensions.[13–15] Possible applications of dislocations as active components of semiconductor devices have been discussed.[16] Note that the cross-section area of a dislocation core is about $1\,nm^2$ characterizing the defects itself as native nanowires embedded in a perfect matrix.

Here, we present a method allowing us to generate defined numbers and types of dislocations in two-dimensional arrangements, their separation by nanolithography, and, for the first time, results of detailed measurements of electrical properties of individual dislocations in combination with structural analyses by electron microscopy. Metal-oxide-semiconductor field-effect transistors (MOSFETs) and diodes have been used for measurements.

II. SAMPLE PREPARATION AND EXPERIMENTAL TECHNIQUES

Semiconductor wafer direct bonding under hydrophobic surface conditions was applied to realize two-dimensional dislocation networks.[17,18] Varying the angles of rotational and azimuthal misfit, respectively, different dislocation distances result. The type of the dislocations forming the network is controlled by the crystal symmetry of the bonded wafers. Using {100}-oriented silicon wafers, a screw dislocation network with square-like meshes results from the rotational misfit.

Silicon-on-insulator (SOI) wafers were applied to avoid the effect of bulk material and possible defects therein. Commercially available wafers were utilized having the following specification: Czochralski-grown silicon, diameter

a)Author to whom correspondence should be addressed. Electronic mail: reiche@mpi-halle.de.

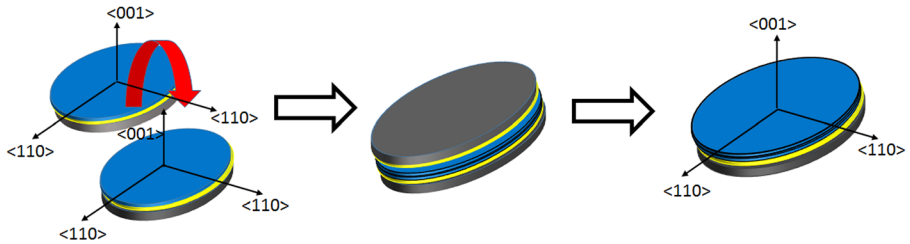

FIG. 1. Schema of the wafer bonding process. Two ⟨100⟩-oriented SOI wafers are used (left), where the blue color characterizes the thin device layer (30 nm thick), yellow the buried oxide, and grey the substrate wafer. Both wafers are sticked (bonded) together, so that the surfaces of both device layers are in contact (middle). A new SOI wafer results after removing one of the original substrate wafers (right). The thickness of the device layer is now 60 nm.

150 mm, p-type, resistivity $\rho = 1$–$10\ \Omega$ cm, ⟨100⟩-orientation, buried oxide thickness (BOX) 60 nm. The initial device layer thickness of 260 nm or 600 nm was reduced to 30 nm by thermal oxidation. The bonding process was performed under hydrophobic conditions in an atmospheric environment. Various twist angles between $0.01° < \vartheta_{twist} < 0.4°$ were realized. Fig. 1 shows a schema of the process. After bonding, a subsequent annealing at 1050 °C for 4 h in nitrogen result in the formation of the two-dimensional dislocation network in the interface. Finally, one of the handle wafers was removed by a combination of mechanical grinding and chemical etching (spin etching) followed by chemical etching of the oxide layer. This results in new SOI wafers having two-dimensional dislocation networks in their 60 nm thick device layers (Figs. 2(a) and 2(b)).

SOI MOSFETs and arrays of n^+pn^+-diode structures were prepared on such substrates using lithographic techniques and reactive ion etching (RIE). The channel region was defined first.

The channel direction is chosen ⟨110⟩-crystal directions which coincides with the dislocations direction in Si (Fig. 2(c)). In order to study the effect of the dislocation density, the channel width was varied between 1 μm and 10 μm. The channel length, however, was constant ($L = 1\ \mu$m). Source and drain contacts were formed by As^+ implantation (5 keV, $1 \times 10^{15} cm^{-2}$) combined with a rapid thermal annealing (RTA) step (950 °C, 60 s).

For MOSFETs, a thin gate oxide of about 6 nm was formed by thermal oxidation. The device gates were prepared by low-pressure chemical vapor deposition (LP-CVD) of polycrystalline silicon (100 nm thick) followed by As^+ implantation (30 keV, $1 \times 10^{15} cm^{-2}$) and a RTA step (950 °C, 60 s). Finally, contacts were formed by Al deposition and annealing at 420 °C for 30 min in hydrogen.

Electron beam lithography (EBL) was utilized to realize n^+pn^+-structures with channel widths down to 30 nm. Arrays of primary structures with $W = 250\ \mu$m and $L = 1\ \mu$m were prepared first by photolithography. After that EBL was

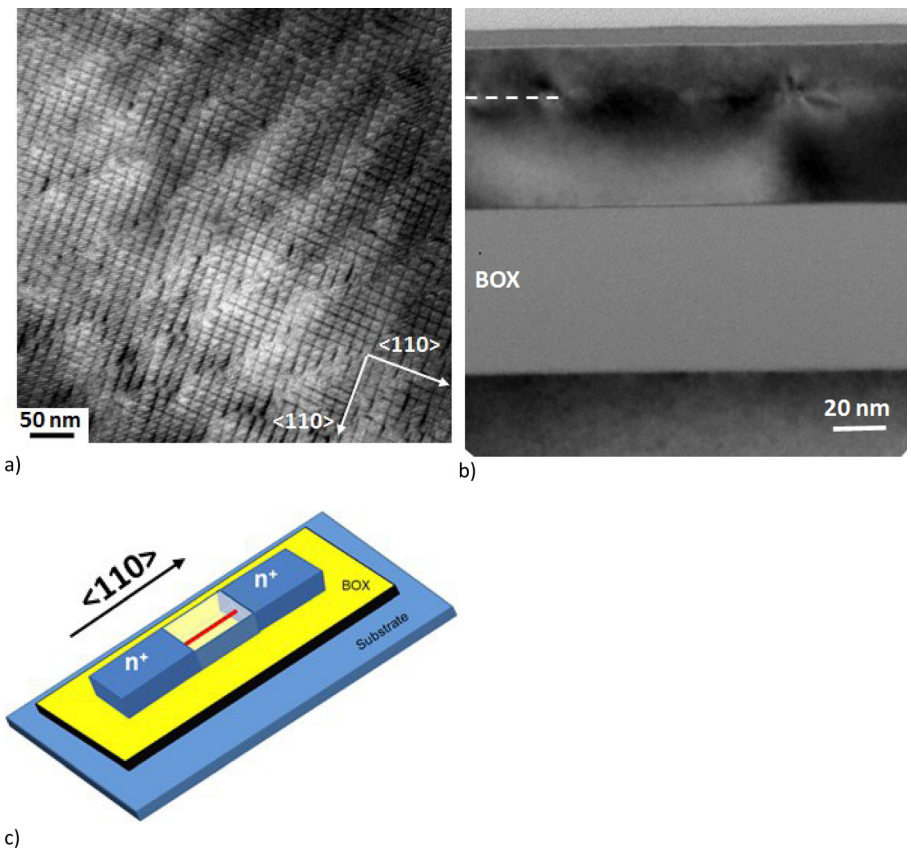

FIG. 2. TEM plan-view image of the screw dislocation network in the bonded interface (a) and the corresponding cross-section image ({110}-plane) through the SOI stack with the dislocation network (dotted line) in the 60 nm thick device layer (b). Parts of the device layer are consumed by device processing (for instance oxidation) causing that the dislocation network is not precisely in the center of the layer. Schema of an n^+pn^+ diode structure with a dislocation (red line) in the channel (c). Devices are fabricated parallel to ⟨110⟩ directions, i.e., parallel to the dislocation line direction.

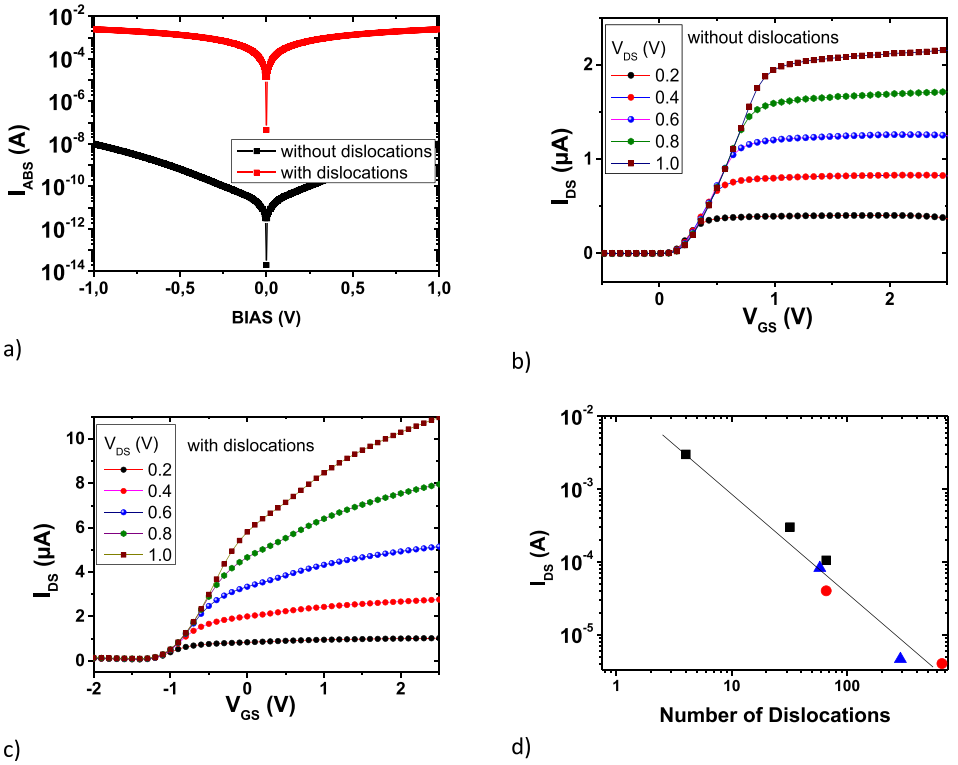

FIG. 3. Current-voltage (I–V) characteristics of n^+pn^+ diode structures with (red) and without dislocations (black) in the channel (a). Transfer characteristics (I_{DS}-V_{GS}) of nMOSFETs without (b) and with dislocations in the channel (c). Source-drain current I_{DS} as a function of the number of dislocations in the channel (d). Measurements at $V_{DS} = 2\,V$ and $V_{GS} = 0\,V$. Different symbols characterize measurements on various wafers having different dislocation densities.

used to reduce the channel width. Within an array, n^+pn^+-structures with $30\,nm \leq W \leq 1\,\mu m$ were realized. A high-resolution positive electron beam resist (ZEP 520A, ZEON Corp.) was used. All exposures were carried out in a JBX 6300 FS electron beam lithography system (JEOL). The real channel width of all structures was measured in a scanning electron microscope after dry etching (cryoprocess at $-60\,°C$, SF_6/O_2 chemistry) and resist removing.

All device measurements were carried out at room temperature using an Agilent B1500A Semiconductor Device Analyzer in combination with a PM5 probe station (Suss).

The defect structure was analyzed by applying a probe C_S corrected scanning transmission electron microscope (FEI Titan 80–300).

III. RESULTS AND DISCUSSION

Fig. 3(a) shows the conductance of the dislocation layer by measuring current-voltage (I–V) curves of a n^+pn^+-structure. An increase of the current I by more than five orders of magnitude is obtained even at low bias-conditions for devices containing dislocations compared to a reference sample prepared on a SOI wafer with the same device layer thickness (60 nm) but without dislocations. The carriers transported through dislocations are electrons. Between the two n^+-contacts, an n^+-n-n^+ transport path through dislocations is formed resulting in a higher conductance. The current increase depends on the dislocation density and on the type of the dislocations. Electron microscope analyses revealed a dislocation network formed dominantly by screw dislocations, where the dislocation distance is about 17 nm (Fig. 2(a)). An increase of the drain current I_{DS} is also proved for nMOSFETs containing dislocations. The increase of the drain current depends on the existing dislocation type and may exceed a factor of 50 if mixed dislocations are present in the channel. For devices containing screw dislocations, an increase of I_{DS} by a factor of five results for MOSFETs with channel lengths L and widths W of 1 μm, respectively (Figs. 3(b) and 3(c)). Assuming a dislocation distance of 17 nm, this implies that there are about 60 screw dislocations in the MOSFET channel. Furthermore, an unexpected

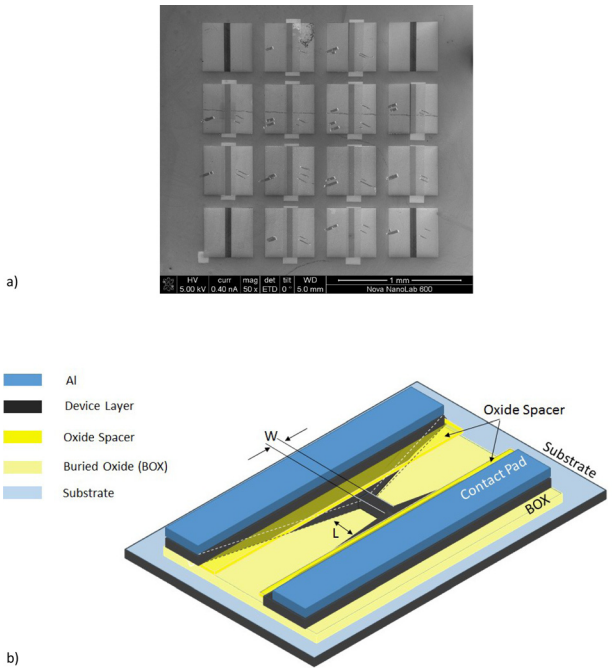

FIG. 4. Scanning electron microscope (SEM) image of the diode array (a) and schema of a diode (b). The length L was fixed to 1 μm, while widths of $W = 1000\,nm$, 500 nm, 400 nm, 300 nm, 200 nm, 100 nm, 80 nm, 60 nm, 50 nm, and 30 nm were used.

dependence of I_{DS} on the number of dislocations in the MOSFET channel was proved,[13,19] where the drain current increases as the number of dislocations decreases (Fig. 3(d)). The measurements suggest that the highest drain current exists if only one dislocation is present in the transistor channel. One explanation could be the appearance of interactions between neighboring defects with decreasing dislocation spacing (or increasing number of dislocations).

In order to study the effect of individual dislocations, arrays of n^+pn^+-diodes were fabricated on the wafer containing the same screw dislocation network used for MOSFET analyses described above. Arrays of 16 diodes with $W = 250\ \mu m$ and $L = 1\ \mu m$ were fabricated first by photolithography (Fig. 4(a)). The diodes are closely spaced in order to avoid any inconsistency of the dislocation network. The width of the diodes was subsequently reduced by electron beam lithography in combination with a dry etching step down to $W = 30$ nm (Fig. 4(b)). The channel length was constant in all cases ($L = 1\ \mu m$). Results of measurements of the current density J as a function of the applied bias are shown in Fig. 5(a) for diodes having channel widths ranging from $W = 1\ \mu m$ down to $W = 30$ nm. The data clearly proved an increase of J with decreasing channel width, or, in other words, with decreasing number of dislocations. Fig. 5(b) shows the corresponding plot of the resistivity ρ demonstrating that ρ decreases by more than one order of magnitude as W decreases from 1 μm to 30 nm. The dependence of ρ on W is shown in Fig. 5(c) and compared with data of a reference sample without dislocations. There is no effect of W on the resistivity of the reference sample which is $\rho \cong 2\ \Omega$cm corresponding to the data of the initial SOI material. If

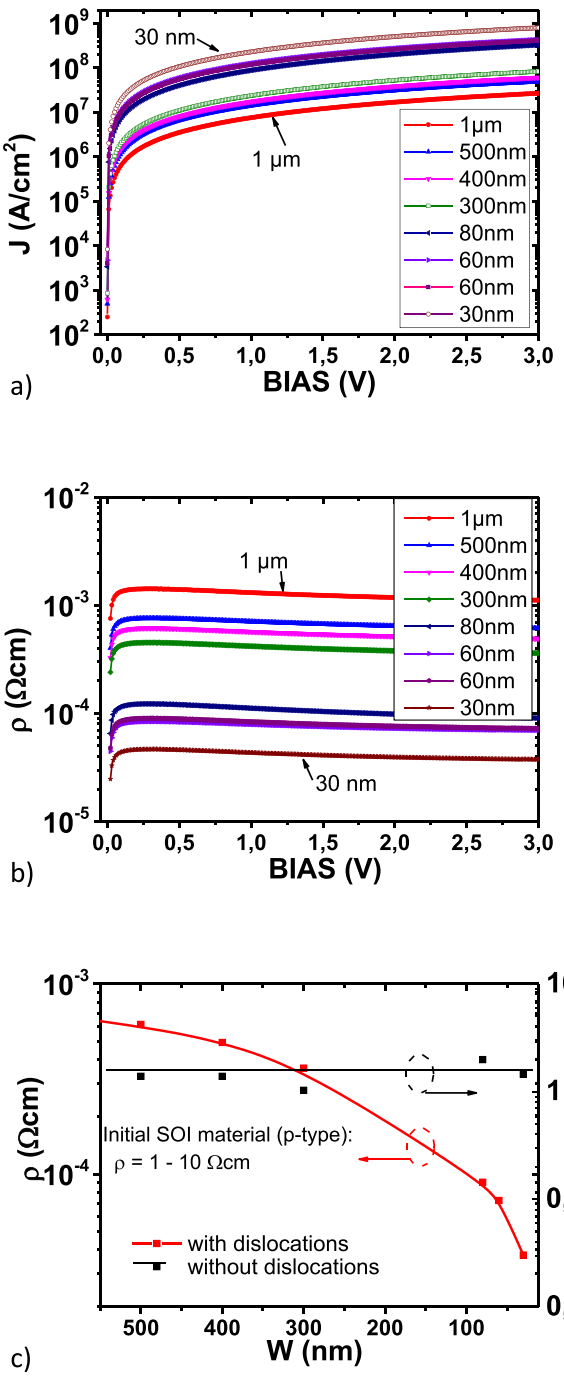

FIG. 5. Current density J (a) and corresponding resistivity (b) measured for diodes having widths from $W = 1\ \mu m$ down to $W = 30$ nm. Resistivity as a function of the channel width for diodes with (red) and without dislocations (black) (c). Note the different scale. All measurements were carried out on the same screw dislocation network.

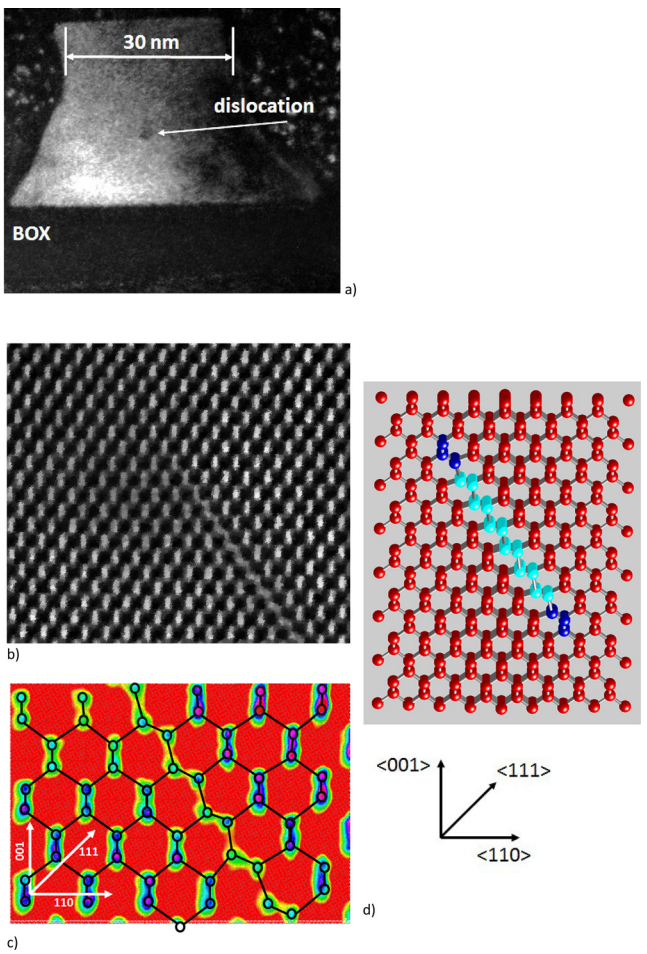

FIG. 6. Dark field image of a 30 nm structure with a single dislocation (a). FIB technique was used for target preparation of the cross section through the device channel. HAADF image of a part of a dissociated screw dislocation (b). Adopted atom positions (c) around one partial dislocation shown in (b), and stick-and ball model of the whole defect in a projection parallel to {110} (d). Atoms in the core of the 30° partial dislocations marked dark blue, while atoms in the stacking fault are plotted in light blue. Atoms of the undisturbed Si matrix are shown in red color.

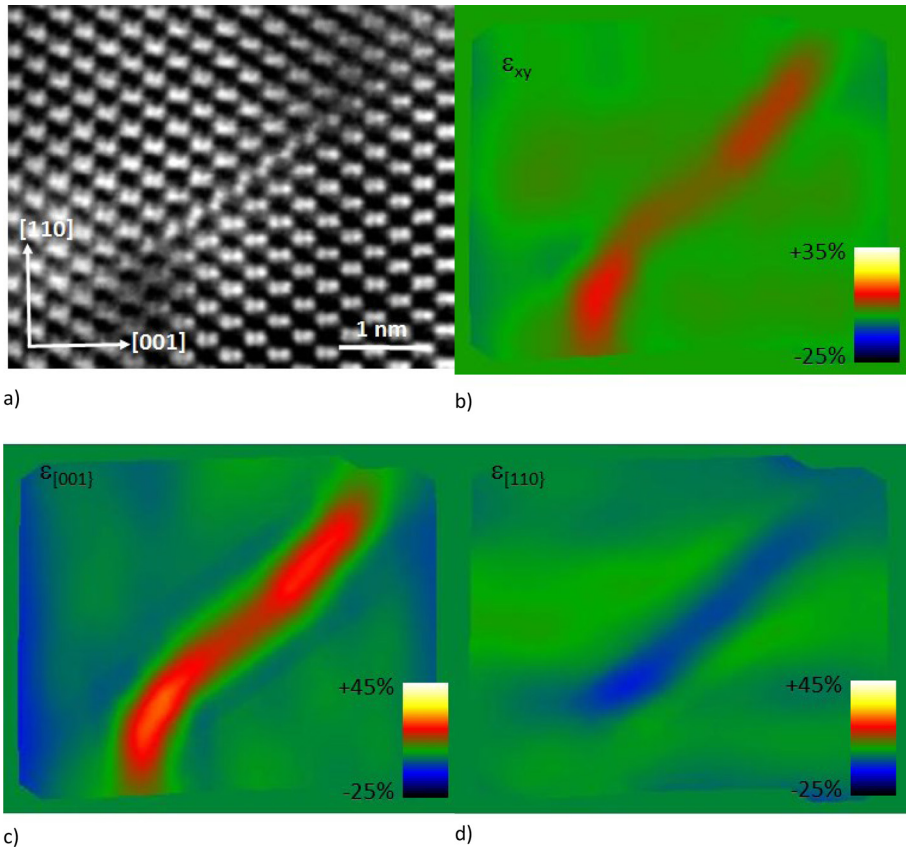

FIG. 7. HAADF image of a dissociated screw dislocation (a). A {110} cross-section sample was used for imaging. The resulting in-plane strain (ε_{xy}) in {110} is tensile ($\varepsilon_{xy} \cong 10\%$) and concentrated on the partial dislocations (b). Strain components in the main directions ($\varepsilon_{[001]}$ and $\varepsilon_{[110]}$) are shown in (c) and (d), respectively. Lighter colors characterize increasing tensile strain, while dark colors are related to increasing compressive strain. Strain analyses were performed using PPA.

dislocations are present in the channel, a linear decrease of ρ with decreasing W is obtained which correlates to

$$\rho(\Omega\,\mathrm{cm}) = 1.228 \cdot 10^{-6} W - 3.117 \cdot 10^{-6}, \qquad (1)$$

where W is measured in nanometers.

The number and type of dislocations in the channel of individual diodes were analyzed by transmission electron microscopy (TEM). Cross sections of individual channels were fabricated by applying focused ion beam (FIB) target preparation. Fig. 6(a) shows the TEM dark-field image of the smallest structure with $W = 30$ nm where the diffraction contrast refers to the presence of an individual dislocation. More details about the structure of the dislocation are obtained by applying high-resolution electron microscopy and by analyzing the whole dislocation network on unpatterned areas of the wafer. Weak-beam images show that most of the screw dislocations forming the network dissociate into Shockley partial dislocations. The dissociation according to the reaction

$$\frac{1}{2}[110] \rightarrow \frac{1}{6}[12\bar{1}] + \frac{1}{6}[211], \qquad (2)$$

is generally known and represents a minimization of the energy of the dislocation.[20] The dissociation causes also the generation of a stacking fault between both partial dislocations. The size of the stacking fault is 6.8 nm. High-angle annular dark field (HAADF) microscopy confirms the results (Fig. 6(b)). The high resolution of this scanning transmission electron microscope method allows comparing the image with the crystal structure (Figs. 6(c) and 6(d)). It can be shown that the distortion of atoms inside the defect correlates to models of dissociated screw dislocations obtained by molecular dynamic simulations.[21] Both partial dislocations are oriented parallel to ⟨110⟩-directions in the {111}-glide plane. Their Burgers vectors are therefore inclined at an angle of 30° to the line direction of the dislocations resulting in surrounding strain fields (Fig. 7(a)). The strain fields are quantified by peak-pairs analysis (PPA) of high-resolution electron microscope images.[22] This method extracts the strain ε in the defects and the surrounding area by measurement of the lattice distortion. Analyses of ε in different directions clearly proved the strain fields on the partial dislocations but show also that most of the strain is concentrated on the dislocation cores (Fig. 7). Inside the defects, tensile strain of about 10% exists, which is in accordance with theoretical predictions[23,24] and measurements on other dislocations.[25]

IV. CONCLUSIONS

The described measurements demonstrate that dislocations form channels of higher conductance in thin silicon layers. The increase of the conductance is primarily related to the number of dislocations but depends also on the dislocation type. An increase of the drain current of MOSFETs with decreasing number of dislocations was already stated.[13,19] An increase of the current density is also observed if screw dislocations are present in diode structures analyzed here. The results show an increase of the current density if the number

of dislocations decreases. The highest current density is obtained if only one dislocation is present in the channel. The experimental data shown in Fig. 5(a) are scaled to the device dimensions. Because only the dislocation forms the conductive channel scaling to their dimensions is required. Assuming the cross section of the defect core of 1 nm^2, the current density would be $J = 3.8 \times 10^{12}$ A/cm^2 for a single screw dislocation. This results in a resistivity of $\rho \cong 1 \times 10^{-8}$ Ω cm, which is eight orders of magnitude below that of the surrounding silicon. The resistivity of the dislocation is also significantly smaller than for most metals[1] and implies a supermetallic behavior of dislocations in silicon. The reason for the exceptional conductivity is the very high strain in the dislocation core induced by atomic displacements therein. PPA analyses revealed tensile strain of $\varepsilon \cong 10\%$ close to the cores of the 30° partial dislocations. It is generally known that strain modifies the band structure of silicon and carrier mobility by (i) the reduction of the carrier effective mass and (ii) by reduction of the intervalley phonon scattering rates.[26–28] For p-type material analyzed here, the potential barrier induced by the tensile strain generates the confinement of electrons along the dislocation line.[29] This is combined with changes of the electron effective masses and a reduction of the electron scattering due to conduction valley splitting, which lowers the rate of intervalley phonon scattering.[26,30,31] The electron channel is screened by holes in the surrounding silicon.

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