Low-voltage transistor array with dynamic synaptic plasticity for neuromorphic computing

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ABSTRACT

This study demonstrates the integrated junctionless indium-tin-oxide transistor arrays for neuromorphic computing, exhibiting remarkable stability and consistency. Stable and dynamic synaptic plasticity is demonstrated by these devices, with both paired pulse facilitation (PPF) and paired pulse depression (PPD) being achieved within a single device. Through the modulation of synaptic weights, the dynamic conversion from PPD to PPF can be realized, thereby enabling multimodal learning and reducing the complexity of the neuromorphic system. The unique ion migration mechanism of chitosan electrolytes enables short-term plasticity and pulse-number-dependent weight modulation. Utilizing these properties, a feedback-enhanced learning model was constructed to emulate spatiotemporal integration of neural signals. The array exhibits excellent scalability, offering a cost-effective solution for large-scale neuromorphic systems. Notably, the controllable switch between inhibition and potentiation modes represents a demonstrated capability in artificial synapse design, holding promise for bioelectronic devices and adaptive sensing applications.

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Recently, neuromorphic devices that mimic the information-processing functions of the human brain have received increasing attention because neuromorphic computing, by simulating the efficient parallel-processing characteristics of biological neural networks, can overcome the performance limitations brought about by the separation of memory and processing units in the traditional von Neumann architecture.[1–4] The brain enables efficient parallel computing via synaptic plasticity. Artificial synapses require tunable conductivity to advance neuromorphic computing.[5] Currently, synaptic devices include two-terminal devices represented by memristors and phase-change memories, as well as three-terminal devices represented by ferroelectric transistors and floating-gate transistors.[6–8] Among various synaptic devices, electrolyte-gated transistors (EGTs), which simulate the neurotransmitter release process of biological synapses by regulating ion migration within the gate dielectric, have shown unique advantages in the field of brain-inspired computing.[9,10] Chitosan, as the gate dielectric of EGTs, can not only form a functional electric-double-layer (EDL) but also mimic the ion dynamics of synapses, providing an ideal platform for the development of high-performance neuromorphic devices.[11,12] EDL synaptic transistors have been used to simulate

various synaptic functions, including short-term plasticity (STP) and long-term plasticity (LTP).[13,14] Previous studies have reported EDL electrolyte-gated synaptic transistors that can achieve STP, such as paired pulse facilitation (PPF), paired pulse depression (PPD), and spike-timing-dependent plasticity (STDP).[15] However, these devices faced challenges in dynamically switching between depression and facilitation modes. The feedback mechanism of the human brain is crucial for the formation of learning and memory and is also very important for bionic intelligence. Therefore, it is necessary to introduce a feedback mechanism in synaptic transistors for simulating the human brain.

For the fabrication of solid-state devices, photolithography is the main traditional method. Most electronic components in modern production processes are almost manufactured using photolithography technology. However, the photolithography process is usually complex and has strict requirements on the environment. Moreover, some impurities may be introduced during the photolithography process, which can affect the performance of the thin film to a certain extent. Therefore, the integrated junctionless transistor array, in which the channel layer, source/drain electrodes, and interconnected channels

are prepared through a single magnetron sputtering process, can simplify the fabrication procedure, reduce the introduction of impurities, and simultaneously improve the fabrication efficiency and quality.

In this study, a photolithography-free mask-assisted magnetron sputtering technique is implemented for fabricating chitosan-gated integrated junctionless ITO transistor arrays. This technique avoids photoresist contamination and enables scalable production. By merely adjusting the pulse parameters to regulate the synaptic weight, dynamic switching between depression and facilitation modes can be achieved within a single device. In addition, the feedback-enhanced learning model constructed using this array effectively simulates the spatiotemporal integration function of biological axons. The device exhibits good stability and can effectively simulate synaptic plasticity, including excitatory postsynaptic current (EPSC), PPF, and PPD. Through the coordinated modulation of pulse intensity and width, gradient modulation of EPSC can be achieved. Compared with the no-feedback condition, the application of adaptive filtering and sensory signal processing significantly improves the learning efficiency of the feedback model, demonstrating the application potential of neuromorphic systems. This study provides a practical method for low-cost, large-scale artificial neural networks and bioelectronic interfaces.

Chitosan precursor solution preparation: Chitosan powder was mixed with acetic acid in a 1:1 mass ratio at room temperature to form a solution. This solution was then combined with de-ionized water in a 1:25 mass ratio. The mixture was stirred on a magnetic stirrer for 1 hour and then placed in an ultrasonic bath for 15 min. The beaker was left to stand until all bubbles disappeared.

TFT array fabrication: The chitosan solution was spin-coated onto FTO (fluorine-doped tin oxide)-coated glass substrates to create 2×2 cm^2 samples. The samples were dried in an oven and then fitted with specifically shaped masks. Subsequently, the samples were placed in a magnetron sputtering device for deposition at 0.8 Pa pressure and 100 W power for 50 s, forming a junctionless 2×2 ITO thin-film transistor array. In this array, each individual transistor had a channel width of 1500 μm and a channel length of 100 μm.

X-ray photoelectron spectroscopy (XPS) (ESCALAB250Xi) was employed for the characterization of the structure and composition of the ITO thin film. Scanning electron microscope (SEM) (FEI SEM450) was utilized to observe the surface morphology of both the chitosan and ITO thin films. The electrical properties of the transistor array were measured using a semiconductor parameter analyzer (Keithley 4200 SCS).

Figure 1(a) illustrates the transistor array structure fabricated in this study, which adopts a glass/FTO/chitosan/ITO stacked structure. The mask-assisted magnetron sputtering technique is used to achieve a photolithography-free process, which not only simplifies the manufacturing process but also potentially avoids interface contamination caused by residual photoresist. XPS analysis, as shown in Fig. 1(b), confirms that the dominant components in the ITO layer are In^{3+} (In 3d: 444/452 eV; 3p: 665/704 eV) and Sn^{4+} (Sn 3d: 486/495 eV), with a low content of oxygen vacancies, suggesting that the material might possess a high stoichiometric ratio. The O 1s (531 eV) and C 1s (285 eV) peaks correspond to lattice oxygen and surface carbon adsorption, respectively.[16] SEM images, as shown in Figs. 1(c) and 1(e), reveal a uniform chitosan and ITO film, which is likely to ensure favorable dielectric properties and carrier transport. Observations under an optical microscope show that the device surface pattern is

consistent with the mask pattern, which may indicate the effectiveness of the magnetron sputtering method. This photolithography-free approach could potentially provide a scalable fabrication route for low-cost transparent electronic devices.

The transfer and output characteristics of four distinct devices on the same substrate are shown in Fig. 2, demonstrating the stability and uniformity of the transistor array fabricated by the magnetron sputtering process.[17,18] In Figs. 2(a)–2(d), when V$_{ds}$ is fixed at 2 V, a distinct counterclockwise hysteresis window can be observed during the V$_{gs}$ sweep from -2.5 to 3 V. The counterclockwise hysteresis induced by ion relaxation phenomena exhibits fundamental differences from conventional clockwise hysteresis.[19] When a small gate voltage (<2 V) is applied, the high capacitance of the EDL induces a large number of charge carriers in the channel layer. This high capacitance is due to the very short distance between the two layers of charges in the EDL, which creates a strong electric field even at low voltages. Consequently, compared to traditional dielectric materials, the transistor can switch on and off at much lower gate voltages, thereby enhancing the device's performance in low-power applications.[20] Furthermore, after five consecutive measurements, the variations in transfer characteristics seem negligible. As illustrated in Figs. 2(e)–2(h), the differences in output characteristics lie within a reasonable and acceptable range, suggesting that the process exhibits excellent uniformity, thereby meeting the integration requirements for arrayed devices. These results suggest that the devices integrated through the magnetron sputtering process could exhibit a high degree of uniformity and stability, which may provide a reliable foundation for applications in biological synapse simulation and artificial neural networks.[21]

The synaptic structure of the biological nervous system is shown in Fig. 3(a). In this structure, the presynaptic terminal releases neurotransmitters, which diffuse across the synaptic cleft and bind to receptors on the postsynaptic terminal, completing the information transmission process. To simulate this, we use ITO transistors with a chitosan-based gate dielectric in a zero-bias structure. Specifically, the gate is considered the presynaptic terminal, providing the stimulating input; the chitosan dielectric serves as the neurotransmitter layer for ion transfer, and the ITO channel simulates the postsynaptic terminal.[22]

Synaptic plasticity, a fundamental mechanism for biological learning and memory, plays a critical role in neural signal transmission in the brain.[23] In Fig. 3(b), when a gate pulse (1 V, 20 ms) is applied, a conductive channel is established between the source and the drain. However, when the gate pulse is removed, the drain current gradually decays back to its initial resting state. This indicates that under the action of the applied voltage pulse, the migration of cations at the gate dielectric/channel interface leads to the formation of the EDL. This results in the accumulation of a large number of cations at the gate dielectric/channel interface. Due to the electrostatic coupling effect, a significant number of electrons are induced in the channel, thereby increasing the channel current. As the pulse is removed, the cations at the gate dielectric/channel interface gradually diffuse back to their equilibrium positions, and the channel current gradually decays and returns to its initial resting state. The current response behavior in this channel is highly similar to the EPSC process in biological synapses. The attenuation of the resting current can be observed when the material is subjected to repeated pulsed voltages. This phenomenon may be attributed to the fact that during the pulse intervals, some ions are
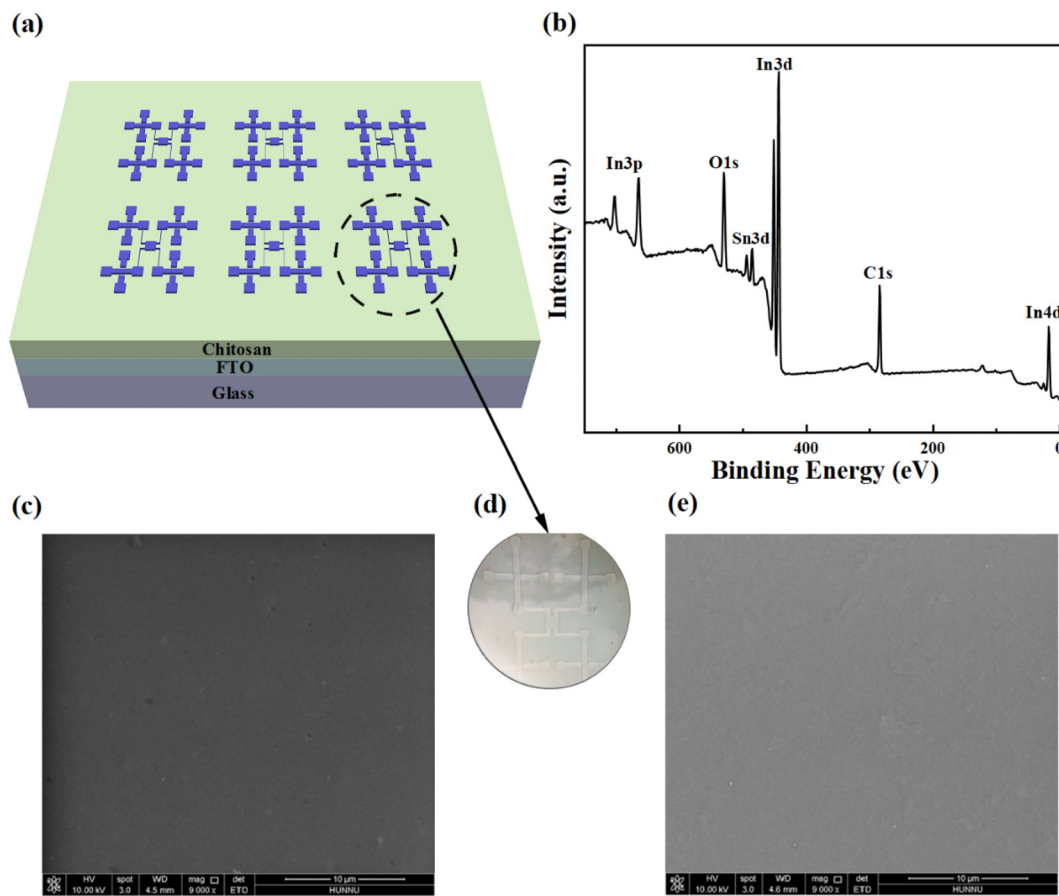
FIG. 1. (a) Schematic of transistor array structure. (b) XPS of the survey scan of the ITO film. (c) SEM image of the chitosan film. (d) Optical microscopy image of the device surface. (e) SEM image of the ITO film.
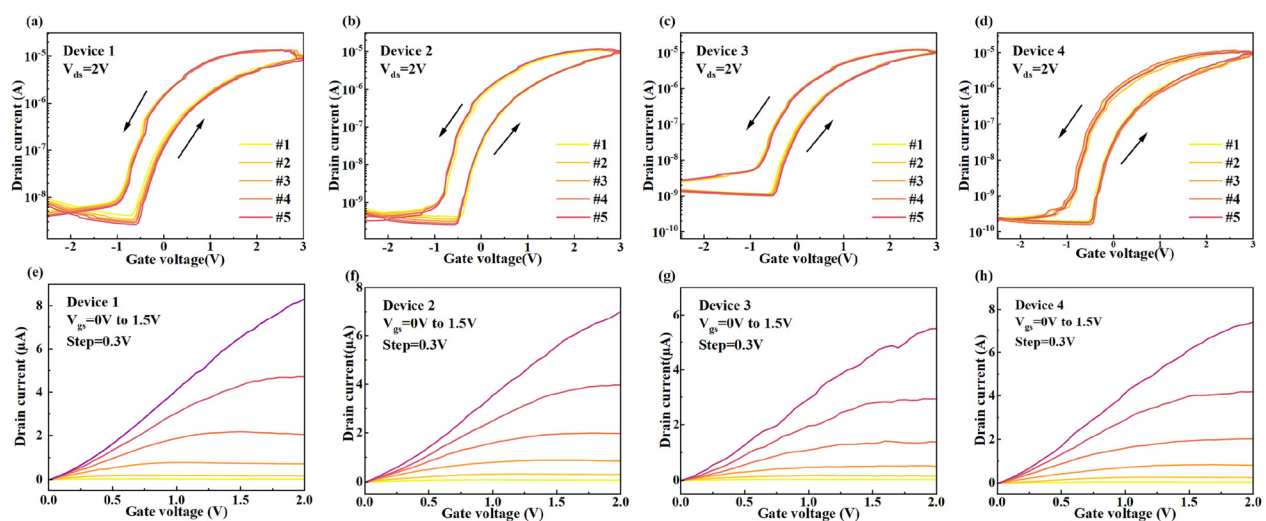
FIG. 2. (a)–(d) Transfer and (e)–(h) output curves of four different junctionless ITO transistor on the same FTO glass.
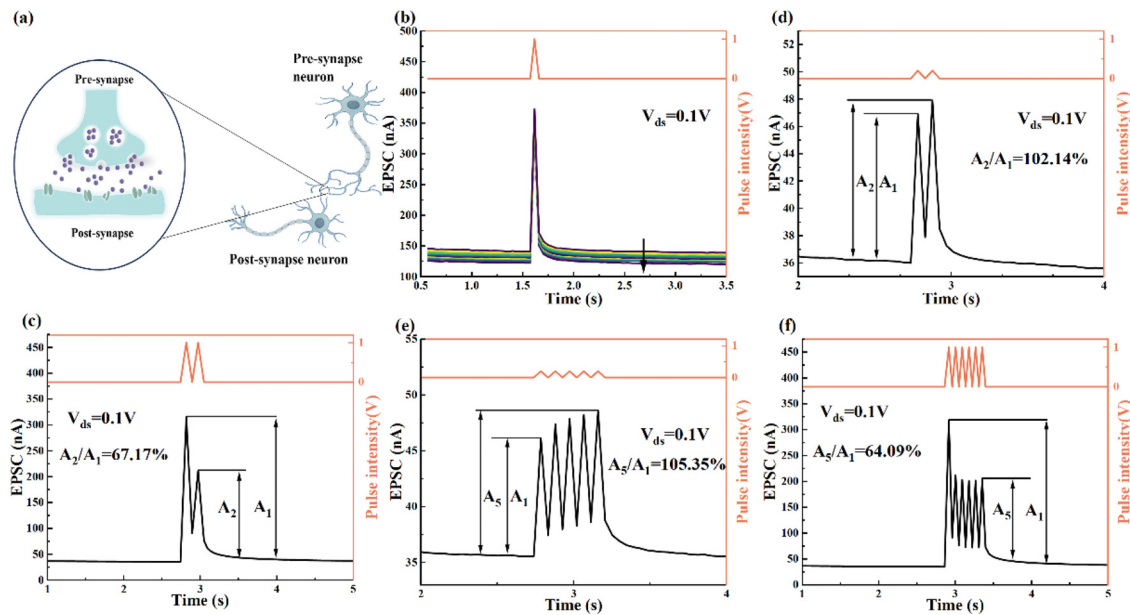
FIG. 3. (a) Schematic diagram of the synapse structure. (b) EPSC and habitual learning. (c) Paired pulse facilitation. (d) Paired pulse depression. (e) Spike number-dependent synaptic facilitation. (f) Spike number-dependent synaptic depression.

trapped by the oxygen vacancies on the ITO surface while returning to their initial positions. Such trapping reduces the driving force of subsequent pulses, consequently leading to a decrease in the resting current.[24,25] This phenomenon resembles the diminished response of biological neural systems to repeated non-threatening stimuli, enabling the emulation of synaptic habituation. By utilizing the resting current decay to simulate synaptic weight reduction, we can construct adaptive filtering circuits for sensor signal preprocessing, such as removing redundant environmental noise. This approach may also contribute to building more efficient spiking neural networks for improved image processing.[26]

Furthermore, PPF and PPD are basic short-term synaptic plasticity behaviors crucial for biological synapses in visual and auditory information processing. PPF occurs when the second of two consecutive spike stimuli produces a stronger response than the first, while PPD occurs when the second response is weaker.[27] As shown in Figs. 3(c) and 3(d), these behaviors can be simulated by applying two identical voltage pulses to the device. When the pulse voltage is 0.2 V with a 20 ms interval, the device shows PPF behavior; when the pulse voltage is increased to 1 V with the same interval, PPD behavior is observed. This phenomenon is likely due to the charge storage capability of chitosan. Under 0.2 V pulses, charge storage and release are stable, and the charge from the first pulse enhances the current response to the second pulse, resulting in PPF. However, at 1 V, excessive charge storage may lead to charge trapping or insufficient release during the second pulse, inhibiting current increase and causing PPD. In the figure, A_1 and A_2 represent EPSC triggered by the first and second pulses.

To investigate the PPF/PPD characteristics further, we define the PPF/PPD index as PPF/PPD index = $A_2/A_1 \times 100\%$.[28] Figure 3(e) shows EPSC generated by five 0.2 V pulses, each 20 ms in width with a 20 ms interval, where each pulse produces a larger EPSC than the

previous one. The PPF/PPD index is extended to A_5/A_1, yielding 105.35%, greater than the PPF index (102.14%), indicating spike number-dependent synaptic facilitation. Similarly, Fig. 3(f) demonstrates spike number-dependent synaptic depression.

In synaptic transistors, pulse intensity and pulse width represent two different weights,[29–31] and focusing on different weights corresponds to two distinct regulation modes, indicating its potential in multimodal learning, such as simultaneously handling tasks related to temporal correlation and frequency dependence, which can reduce the complexity of the neuromorphic system. Figures 4(a)–4(c) demonstrate the variation of EPSC under the cooperative regulation of pulse intensity as the leading variable and pulse width as the minor variable. The collaborative regulation of pulse intensity and width mimics biological synapses' multimodal integration: Long widths prolong ion migration to simulate postsynaptic potential summation like sustained glutamate release, while high voltages drive nonlinear EPSC enhancement analogous to Ca^{2+}-dependent neurotransmitter bursts. This mechanism enables single-device frequency-intensity decoding for multimodal reservoir computing. In Fig. 4(a), with a fixed pulse width, EPSC increases monotonically with increase in pulse intensity. However, the difference in the rate of EPSC increase at different pulse widths causes the curves to intersect. At a pulse width of 60 ms, when the pulse intensity increases from 0.2 to 1.2 V, the EPSC increases by 483%, while at a pulse width of 10 ms, the increase is only 163%. This phenomenon may arise because the increased pulse width allows more time for ions in chitosan to migrate to the ITO interface and form a stable double electric layer, thereby significantly enhancing the EPSC amplitude as pulse intensity increases. Figure 4(b) further illustrates the trend of EPSC variation under a fixed pulse intensity. When the pulse intensity is low (0.2 V), EPSC decreases as pulse width increases. However, as the pulse intensity increases, EPSC exhibits a three-stage
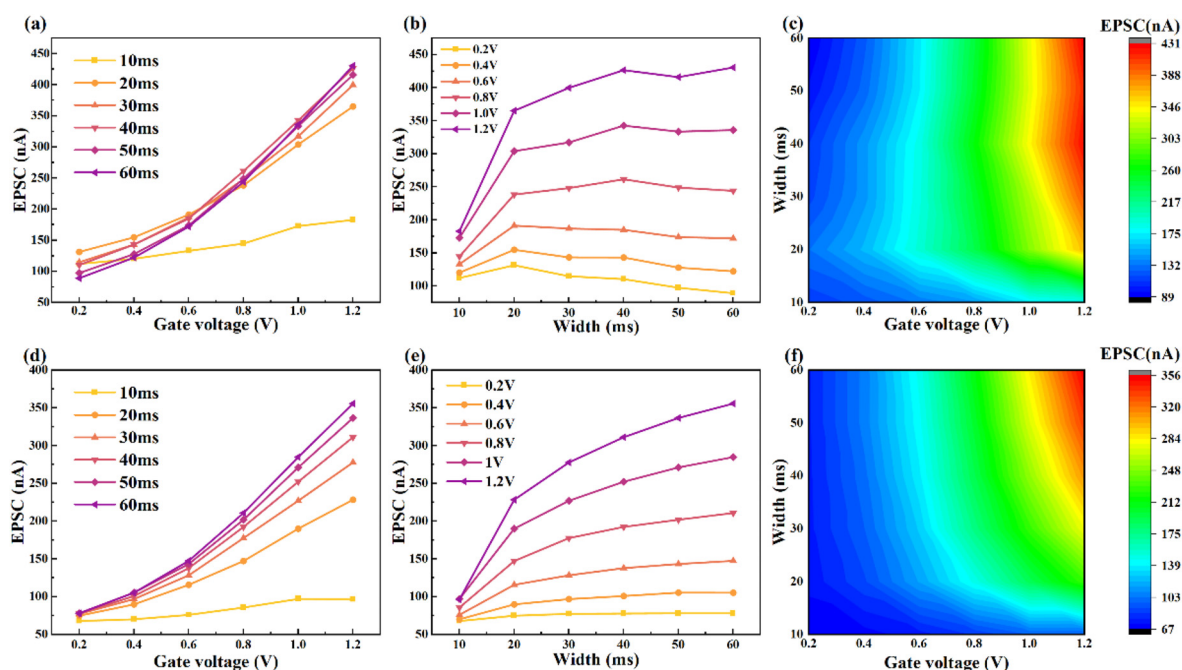
FIG. 4. Pulse intensity (leading) and pulse width (minor) cooperative regulation: EPSC variation under fixed (a) pulse width (b) pulse intensity, (c) global EPSC variation trend. Pulse width (leading) and pulse intensity (minor) cooperative regulation: (d) pulse width (e) pulse intensity, and (f) global EPSC variation trend.

change: suppression, maintenance, and enhancement. This may be related to the different stages of ion movement at the chitosan/ITO interface, providing a potential approach for the regulation of suppressive and enhancing devices. Figure 4(c) provides a more intuitive display of the global trend of EPSC, where the uneven distribution near a 20 ms pulse width suggests that 20 ms may be the threshold at which the device transitions from suppression to enhancement. Figures 4(d)–4(f) show the effects of cooperative regulation of EPSC with pulse width as the leading variable and pulse lentisty as the minor variable. Under a fixed pulse intensity or pulse width, EPSC monotonically increases with increase in the other variable, and the changes are more significant at higher pulse intensities or longer pulse widths. This indicates that the spatiotemporal superposition effect of pulse intensity and pulse width is likely the result of ion migration and accumulation. High pulse intensity accelerates H^+ migration, while long pulse width provides more accumulation time. Figure 4(f) presents a contour map that further reveals the uniform distribution characteristics of EPSC, with high-intensity EPSC concentrated in the upper-right region (high pulse intensity – long pulse width). This predictable response pattern provides a stable foundation for the simulation of synaptic functions, particularly in the simulation of visual signal processing at high pulse intensity and long pulse width, while low pulse intensity and long pulse width aid in simulating memory formation.[32,33]

Figure 5(a) presents a feedback-enhanced brain-like learning model, which consists of input nodes, output nodes, and a feedback loop. In this model, output node responses modulate gate inputs via reverse biasing, emulating how backpropagating action potentials regulate synaptic plasticity in biological neural systems. During enhanced feedback, weight potentiation occurs through prolonged ion retention or increased ion release, analogous to PPF. This aligns with feedback

spike-timing-dependent plasticity (STDP), where postsynaptic firing timing controls presynaptic H^+ migration—the functional equivalent of neurotransmitter release in biological synapses. The improvement in learning efficiency under the feedback loop arises from dynamic regulation of pulse parameters: feedback signals adjust the intensity and width of input pulses. Figure 5(b) quantifies the impact of the feedback mechanism on learning efficiency, with the results indicating that learning efficiency under the feedback condition is significantly higher than under the no-feedback condition with the same stimulus.[34] Additionally, Fig. 5(b) shows that learning efficiency varies across different regions, and the sensitivity of different regions to different stimuli may differ.[35] Figure 5(c) illustrates the learning process under both feedback and no-feedback modes, and also simulates the spatiotemporal integration function of the axons. Through the simulation presented in the figure, it can be more clearly observed that the introduction of feedback results in differences in the device responses. The region most sensitive to the stimulus is defined as the dominant region, and its activation may drive the axonal response. The graded response of synapses corresponding to different devices to the input may reflect the spatial integration of the axons, while the cumulative activation of the dominant region may simulate the temporal integration of the axon. The spatiotemporal integration function of axons can enhance robots' perception and decision-making capabilities in dynamic environments, demonstrating significant potential.[36,37]

In summary, this study developed a chitosan-based transparent thin-film transistor array fabricated via a photolithography-free mask-assisted magnetron sputtering technique, simplifying the manufacturing process and avoiding interface contamination. XPS and SEM characterization confirmed the high stoichiometric ratio and uniformity of the ITO film, ensuring excellent dielectric properties and charge carrier
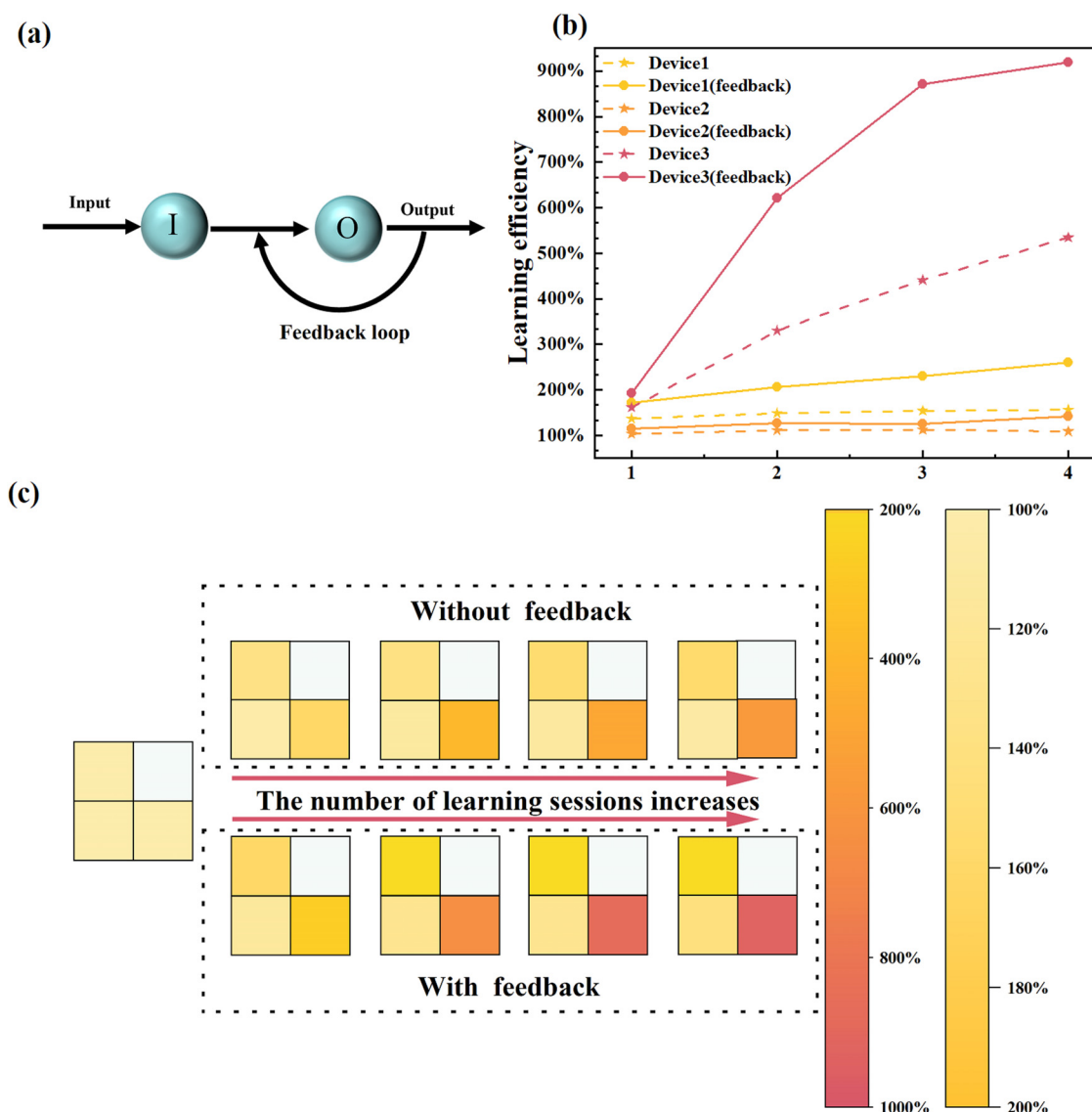
FIG. 5. (a) Feedback-enhanced learning model. (b) Feedback impact on learning efficiency. (c) Spatiotemporal integration of axonal responses.

transport. Electrical measurements demonstrated the stability and consistency of the array, laying the foundation for simulating stable synaptic plasticity, including EPSC, PPF, and PPD. The EDL effect of chitosan renders the realization of dynamic synaptic plasticity possible, enabling the transition from PPD to PPF through weight adjustment. Furthermore, a feedback-enhanced brain-like learning model was constructed, offering a practical method for neuromorphic computing and adaptive sensing systems. This study provides ideas for optimizing device integration, constructing more complex neural networks, and expanding their application in the field of wearable flexible electronic devices.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Pengfei Chen: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (lead); Writing – review & editing (equal). **Wei Dou:** Conceptualization (lead); Data curation

(lead); Formal analysis (lead); Funding acquisition (lead); Investigation (lead); Methodology (lead); Project administration (lead); Resources (lead); Supervision (lead); Visualization (lead); Writing – original draft (equal); Writing – review & editing (lead). **Xiaodong Xu:** Investigation (equal); Methodology (equal). **Yuling Peng:** Investigation (equal); Methodology (equal). **Jiangyun Lei:** Formal analysis (equal). **Guanggang Jiang:** Formal analysis (equal). **Guangxiu Zeng:** Formal analysis (equal). **Dongsheng Tang:** Resources (equal); Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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