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Low-temperature conductance measurements of surface states in HfO_2–Si structures with different gate materials

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Abstract

Metal-oxide-semiconductor capacitors based on HfO_2 gate stack with different metal and metal compound gates (Al, TiN, NiSi and NiAlN) are compared to study the effect of the gate electrode material on the trap density at the insulator–semiconductor interface.

C–V and *G–ω* measurements were made in the frequency range from 1 kHz to 1 MHz in the temperature range 180–300 K. From the maximum of the plot G/ω vs. $\ln(\omega)$ the density of interface states was calculated, and from its position on the frequency axis the trap cross-section was found. Reducing temperature makes it possible to decrease leakage current through the dielectric and to investigate the states located closer to the band edge.

The structures under study were shown to contain significant interface trap densities located near the valence band edge (around $2\times10^{11}\,cm^{-2}eV^{-1}$ for Al and up to $(3.5–5.5)\times10^{12}\,cm^{-2}\,eV^{-1}$ for other gate materials). The peak in the surface state distribution is situated at 0.18 eV above the valence band edge for Al electrode. The capture cross-section is $5.8\times10^{-17}\,cm^2$ at 200 K for Al–HfO_2–Si structure.

Keywords: High-*k* dielectrics; Gate stack; Interface state density; G/ω measurements

1. Introduction

The scaling of SiO_2 below 1.5 nm is associated with several critical drawbacks, such as increased leakage current, dopant penetration from the gate electrode and the effect of polysilicon depletion. To reduce gate leakage while maintaining the gate capacitance, dielectrics with higher permittivity than SiO_2, the so-called high-*k* dielectrics are being pursued. Among the high-*k* dielectrics HfO_2 is the most promising candidate because of its relatively high dielectric constant, large band gap and thermal stability. Although polysilicon has been the gate electrode of the transistor technology for several decades, the gate depletion problem becomes a major drawback for its further application. In addition, reaction between the polysilicon gate and high-*k* dielectric can produce silicides, which affects the dielectric integrity of the gate stack. Also polysilicon gates suffer from Fermi-level pinning

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on HfO_2-based dielectrics, which limits their usefulness on high-k gate stacks [1]. These reasons justify the investigation of metal and metallic compounds as gate electrodes for CMOS devices.

In this work, we have investigated HfO_2-based metal-oxide-semiconductor (MOS) capacitors with various metal and metallic compounds, including NiAlN, TiN, NiSi and Al.

2. Experimental

The HfO_2 films were deposited on fresh un-etched p-type Si(1 0 0) substrate with resistivity of $1 \div 10\,\Omega$cm. Films were deposited at 500 °C by liquid injection MOCVD, using the Aixtron AIX 200FE atomic vapor deposition (AVD) reactor fitted with the "Trijet"™ injector system. The hafnium precursor was $Hf(mmp)_4$. The wafers were HF cleaned before the deposition. The metal gate electrodes were deposited by sputtering to fabricate MIS capacitors. The nitride gates were reactively sputtered in Ar/N flow, the silicidation process of the NiSi gate was performed in argon at 500 °C for 10 s. Thickness of the metal and metal compound layers was 50 nm. Standard lift-off process has been used to pattern the conducting films to define the circular dots with areas of 1.28×10^{-3} or $7.3 \times 10^{-4}\,cm^2$. Then the samples were annealed in forming gas at 400 °C for 30 min. Five samples with four different gate materials were investigated: CS1 (NiAlN), CS4 (TiN), CS5 (NiSi), s440 (TiN) and s443 (Al).

The physical thickness of the dielectric layers was determined using single-angle spectroscopic ellipsometry (240–1000 nm spectral range) and was in the range 9–12 nm. Relatively large thickness was chosen to minimize the leakage currents through the dielectric and to make the electrical measurements more reliable. C–V and conductance–frequency (G–ω) dependences were measured using Agilent 4192 impedance analyzer, and special attention was paid to avoid the contribution of the leakage current in the accumulation region and to eliminate the parasitic series resistance. Conductance measurements were performed in the frequency range from 10^3 to 10^6 Hz.

3. Results and discussion

One of the general problems in C–V characterization of ultra-thin SiO_2 and alternative dielectric layers is large leakage current, leading to the appearance of parasitic resistance of back contact and semiconductor bulk. These effects lead to underestimation of the true capacitance in accumulation region, if the C–V curve is measured in parallel mode [2,3]. The correct C–V dependence can be extracted from C–V data measured at two different frequencies using an approach described in Ref. [4]. In this case the resistance is given by

$$R_p = \frac{1}{\sqrt{\omega^2 C' C(1 + D'^2) - \omega^2 C^2}}, \quad (1)$$

where $D' = 1/\omega R' C'$, R' and C' are measured resistance and capacitance, respectively, and the corrected capacitance equals

$$C = \frac{f_1^2 C_1'(1 + D_1'^2) - f_2^2 C_2'(1 + D_2'^2)}{f_1^2 - f_2^2}. \quad (2)$$

For the case of measurements at two frequencies in the series mode respective equations can be modified as follows:

$$C = \frac{f_1^2 C_{s1}' - f_2^2 C_{s2}'}{f_1^2 - f_2^2}. \quad (3)$$

Fig. 1 shows the current density vs. voltage characteristics for sample s440 measured at temperatures 300 and 260 K. One can see that the level of parasitic currents is rather high, but it decreases with reducing the measuring temperature.

Fig. 2(a) shows the measured C–V curves in the parallel mode at two frequencies at room temperature and the calculated corrected C–V dependence. Fig. 2(b) shows the similar dependences at 220 K. At 300 K, a pronounced kink is observed in C–V curves

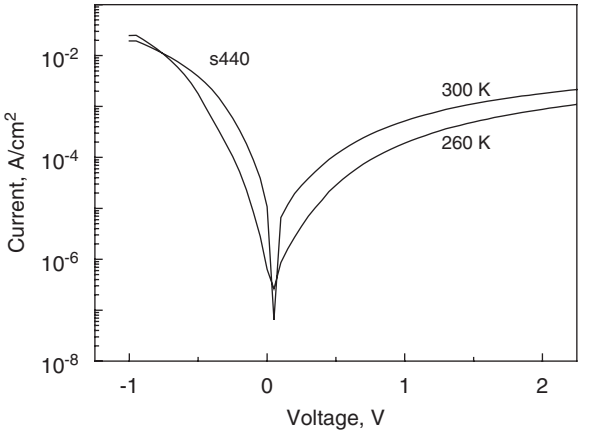

Fig. 1. I–V characteristics for TiN–HfO_2–Si MOS at 300 and 260 K.

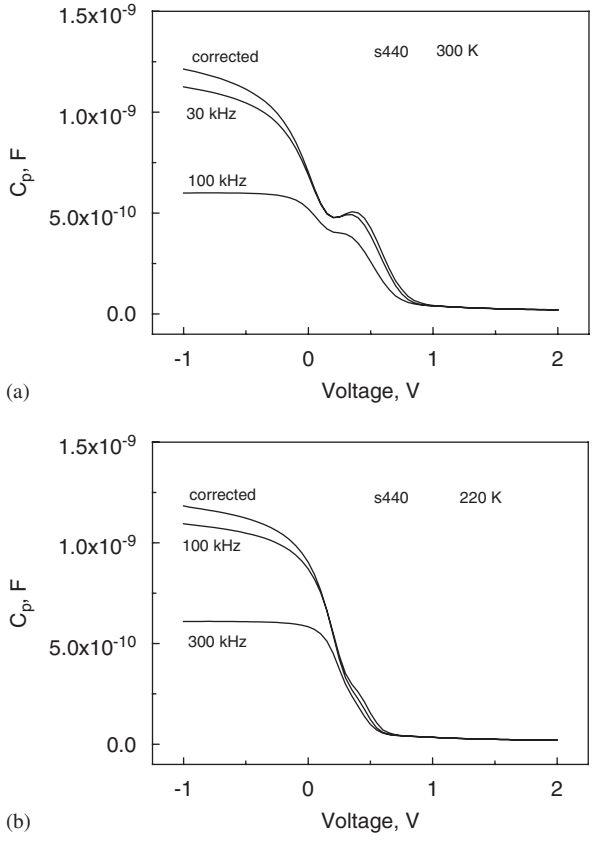

Fig. 2. *C–V* characteristics for TiN–HfO_2–Si MOS structure measured at two frequencies and the calculated corrected curves at 300 K (a) and 220 K (b).

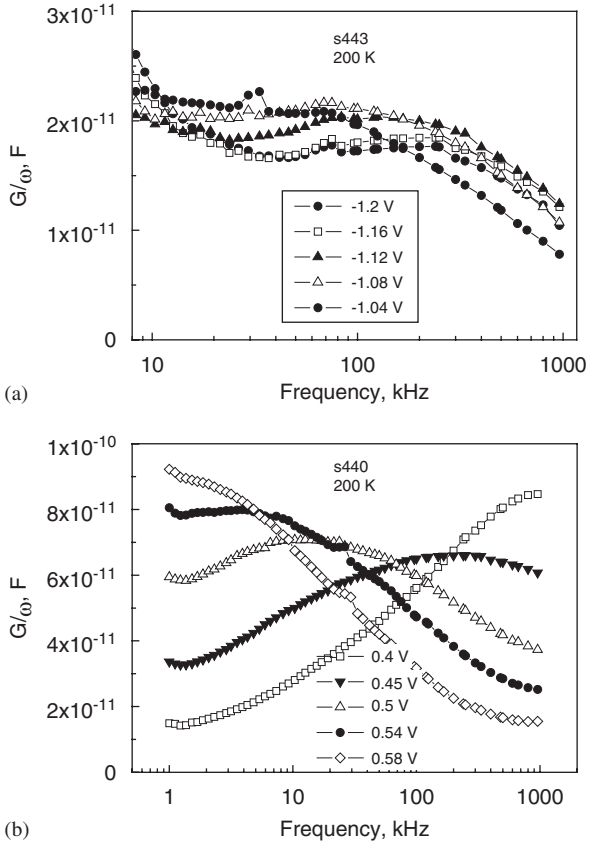

Fig. 3. G/ω vs. frequency dependences for Al–HfO_2–p–Si (a) and TiN–HfO_2–p–Si (b) structures at different gate voltages.

at the gate voltage around 0.4 V. This feature is frequency dependent, becoming stronger at lower frequencies. Similar behavior was reported for SiO_2/HfO_2 interface in Refs. [5,6], and the respective peak in density-of-states distribution was located at about 0.3 V above the valence band edge. Reduction of temperature down to 220 K leads to almost complete disappearance of the kink (Fig. 2(b)). This may reflect the fact that at lower temperatures deep centers no longer contribute to the charge exchange due to relatively high time constant. At the same time low-temperature measurements allow us to study the distribution of surface states closer to the bandgap edge, and only at low-temperatures conductance-frequency measurements give reasonable results for the samples with high leakage.

Fig. 3(a, b) shows the G–ω dependences for samples s443 and s440, respectively, measured at 200 K. The increase of the curves in the low-frequency range for the gate voltages corresponding to accumulation mode is attributed to the parasitic contribution of the leakage current through the dielectric. This effect is more pronounced for sample s443, because the measuring voltage range is shifted to more negative values, as compared to sample s440. The reduction of the measurement temperature well-below room temperature is necessary to reduce the leakage current.

From the value of G/ω at the maximum of the G/ω vs. $\ln(\omega)$ curve the density of interface states D_{it} can be found [7]. From the respective position of the maximum at the frequency axis the trap cross-section was derived. To plot the interface state density as a function of semiconductor interface Fermi level, the surface potential vs. gate voltage characteristic is required. For each value of the gate voltage, at which conductance–frequency dependences were measured, the band bending at the surface was calculated with a standard procedure,

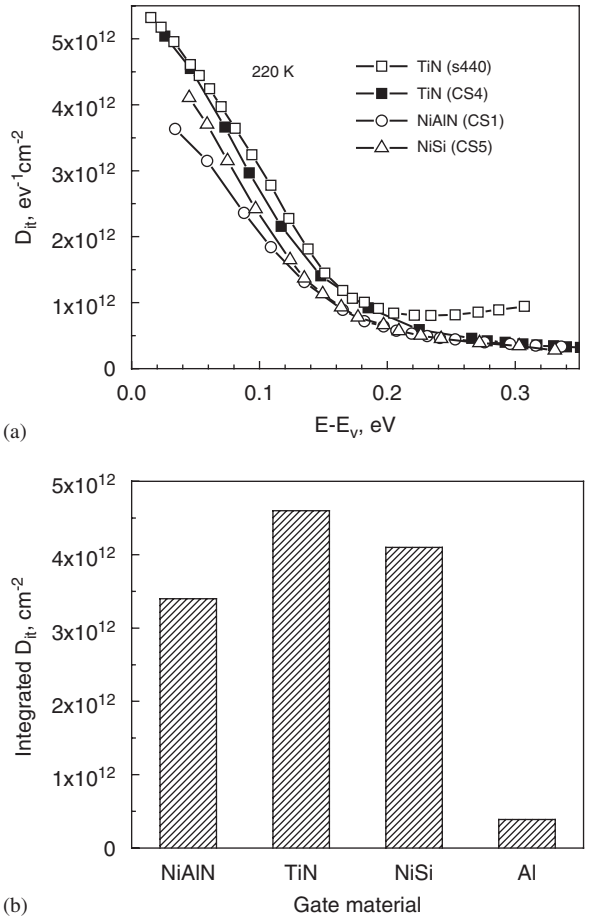

Fig. 4. Interface state spectrum for four samples measured at 220 K (a), and integrated density of surface states for structures with different gate materials (b).

using the corrected C–V curve. Then each value of D_{it} can be linked to its position in the band gap.

The distribution of interface traps for four samples is shown in Fig. 4(a). The interface states spectrum is similar for these samples increasing from $3 \times 10^{11}\,cm^{-2}eV^{-1}$ in the depth of the band gap up to $(3.5 \div 5.5) \times 10^{12}\,cm^{-2}eV^{-1}$ closer to the valence band edge. The difference of the gate materials affects mainly the part of the distribution near the band-gap edge. The lowest D_{it} values were observed for NiAlN gate, and the highest—for the TiN gate. For comparison, the density of interface states was integrated in the range from $E_v + 0.05$ to $E_v + 0.30$ eV and plotted in Fig. 3(b). It should be noted, that an order of magnitude lower interface state densities can be obtained in Si–HfO_2 system for ALD technique of dielectric layer deposition [8].

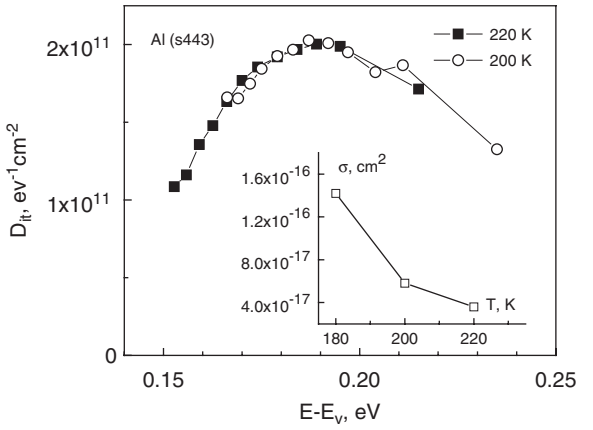

Fig. 5. Interface state spectrum for Al–HfO_2–Si structure measured at 200 and 220 K. The inset shows the temperature dependence of the trap capture cross-section.

Completely different behavior of the distribution of interface states was found for Al–HfO_2–Si structure, as shown in Fig. 5. In this case the peak of the D_{it} distribution is observed with a maximum at $E_V + 0.19$ eV and with much lower value of the interface trap density, than for other samples at the same energy position. Such a distribution can be attributed to the presence of a local state within the band gap. The temperature dependence of the capture cross-section for the respective trap is plotted in the inset of Fig. 5.

4. Conclusions

In this work the interface state distribution was studied in MOS structures with HfO_2-based dielectric stack and various metal and metallic compound gates. It was shown that C–V and G–ω techniques can be successfully applied for determination of interface states parameters even for the dielectric layers with high leakage currents. In this case the parasitic series resistance of back contact and semiconductor bulk should be taken into account. Measurements at reduced temperatures are favorable because of lower leakage currents.

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