



## Stencil-masked phosphorus-implanted silicon for solar cell applications

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### ABSTRACT

Stencil-masked phosphorus implantation on silicon wafers is demonstrated for solar cell applications. Line-shaped window patterns with areas of 156 mm × 156 mm and 125 mm × 125 mm are laid out in the silicon stencil mask with diameters of 200 and 300 mm, respectively. According to laser optical microscopy and scanning electron microscopy observation, the phosphorus-implanted line is 100 μm wide with an edge roughness of a few micrometers. Based on the silicon-stencil-masked phosphorus implantation, the fabrication process of alternative phosphorus-implanted and boron-diffused patterns on silicon wafers is proposed. During the post-implantation wet oxidation process, a thick oxide layer is grown on the phosphorus-implanted silicon, acting as a protective layer for the subsequent diffusion of boron. Scanning capacitance microscopy observation reveals the p-type polarity in boron-diffused silicon and the n-type in phosphorus-implanted silicon with homogeneous contrast along the textured surface. Silicon-stencil-masked ion implantation has potential as a selective doping method on silicon wafers for solar cells.

### 1. Introduction

Ion implantation technology is widely used in the doping processes of semiconductor devices such as ultra-large-scale integrated circuits. The conventional doping process by ion implantation requires many steps: photolithography patterning, ion implantation, photoresist ashing, cleaning, and thermal treatment. Stencil-masked ion implantation technology was proposed to reduce the number of process steps [1,2]. In this technology, an ion beam is irradiated onto the wafer through a stencil mask window, and the photolithography patterning and photoresist ashing steps are not required. Shibata et al. reported stencil-masked implantation for channel doping of p-type metal-oxide-semiconductor field effect transistors [1]. Nishihashi et al. developed a stencil mask lithographic ion implanter, which implants ions in one chip through a silicon stencil mask window without a photoresist mask [2]. Stencil-masked ion implantation has also been studied for application to nonvolatile flash memory. Dumas et al. fabricated localized implanted areas of silicon nanoparticles in SiO<sub>2</sub> layers through a SiN stencil mask with a periodic array of opened windows, which is a rectangular micrometric pattern 5 μm long and 1.5 μm wide [3]. Thus, stencil-masked ion implantation is an effective method for fabricating fine structures in semiconductor devices.

Recently, ion implantation doping has been developed as an

alternative to the furnace diffusion process in the fabrication of crystalline silicon solar cells such as selective emitter cells [4], interdigitated back contact (IBC) cells [5–7], and other types [8,9]. The p-type silicon selective emitter solar cell has a selective phosphorus-doped area under the front electrode line to improve the metallization contact and surface passivation of the field area. The n-type silicon IBC solar cell consists of a boron-doped emitter and phosphorus-doped back surface field (BSF) on the rear side of the substrate. Thus, selective emitter and IBC solar cells have a specific doping line pattern on one side of the substrate. For this reason, stencil-masked ion implantation technologies are used as the fabrication processes for these solar cells. Low et al. reported the formation of phosphorus-implanted selective emitters with widths of 300 and 500 μm by using an in situ proximity mask [10]. Here, the finger line is approximately 100 μm in width or less. A stencil mask window with a narrow slit line is required in a selective emitter solar cell. Therefore, high machining accuracy for the window opening is required in the fabrication of the stencil mask, i.e., small variation in the window. In addition, the position accuracy of the window in the mask is extremely important for aligning the electrode line. The length of the slit line in a previous paper is not known [6,7,10], but it is assumed to approximately correspond to the length of the side of the wafer, i.e., 156 mm in length. Thus, the stencil masks for selective emitter and IBC silicon solar cells consist of window patterns with a high aperture ratio. For this reason,

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the material of the stencil mask must have high mechanical strength.

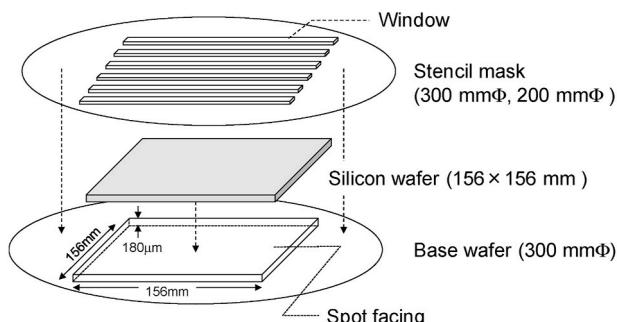
Previous papers regarding silicon solar cells do not mention the material of the stencil mask [6,7,10]. In the present study, we fabricated a stencil mask for solar cells by using silicon wafers for semiconductors for the first time. Silicon material has a high elastic modulus with small temperature dependence, resulting in high mechanical strength. The stencil mask window of the silicon wafer has high position accuracy and mechanical accuracy because it is fabricated by using photolithography and a dry etching process. Thus, the silicon wafer satisfies the requirements as a stencil mask for ion implantation for solar cells. We demonstrate the implantation of phosphorus through a silicon stencil mask with a narrow slit pattern. Additionally, we propose a fabrication process with an alternative phosphorus-implanted and boron-doped area by using only one stencil mask. As the applications of these implantation technologies, the former is for selective emitter silicon solar cells and the latter is for IBC silicon solar cells. Stencil-masked phosphorus-implanted silicon is characterized by optical laser microscopy and scanning electron microscopy (SEM). We discuss the two-dimensional carrier distribution of phosphorus-implanted and boron-diffused silicon, respectively, by using scanning capacitance microscopy (SCM).

## 2. Experimental

A silicon stencil mask was fabricated by using commercially available silicon wafers for semiconductor devices with a diameter and thickness of 200 mm and 725  $\mu\text{m}$ , and 300 mm and 775  $\mu\text{m}$ , respectively. Following oxidation of the wafer, the window layout was patterned on the front surface of the wafer via photolithography. The resist layer on the window pattern was removed, after which the oxide layer and silicon substrate were removed via reactive ion etching, resulting in the window as a stencil mask.

The ion implanter used in the present study is the SHX-III model designed and manufactured by Sumitomo Heavy Industries Ion Technology for silicon semiconductor device processes. This implanter is equipped with a mass analyzer. The applicable wafer size is limited to 300 mm in diameter, whereas the standard silicon wafer for solar cells used in this study is 156 mm  $\times$  156 mm in size. It is necessary to set the stencil mask on the silicon wafer of the solar cell. Fig. 1 shows the special setup for the stencil mask, silicon wafer for solar cells, and base wafer. The spot facing is fabricated on the front side of the base wafer to place in the silicon wafer for solar cells with a size of 156 mm  $\times$  156 mm and a depth of 180  $\mu\text{m}$ . Next, the stencil mask is placed on the base wafer. After the setup is completed, an ion beam is scanned over the entire wafer.

Following the wafer texturing, SC-1 and SC-2 cleaning was performed. Then, the oxide was removed by dipping in HF solution. The surface morphology of the silicon wafer is textured to prevent the



**Fig. 1.** Setup of the silicon stencil mask, silicon wafer for solar cell, and base wafer. The size of the base wafer is 300 mm in diameter, which is limited by the ion implanter used in the present work. The spot facing is fabricated on the front side of the base wafer to place in the silicon wafer for solar cells with a size of 156 mm  $\times$  156 mm and a depth of 180  $\mu\text{m}$ . Stencil masks with 200 and 300 mm in diameter are placed on the base wafer.

reflection of incident light; the composition is upright tetrahedral pyramids with four (111) planes. The depth and in-plane distributions of the as-implanted phosphorus atoms in the sub-surface region of the texture depend on the acceleration voltage, tilt angle, and twist angle [11]. In the present study, elemental phosphorus was implanted in the silicon wafer through the stencil mask window at an acceleration voltage of 10 keV, dose of  $4 \times 10^{15}$  atoms/cm $^2$ , tilt angle of 35°, and twist angle of 15°. An amorphous layer was formed in the as-implanted textured surface under the above conditions. The phosphorus-implanted silicon was characterized by using laser optical microscopy (VK-X 1000, KEYENCE) and SEM (JCM-6000 Plus, JEOL).

An alternative phosphorus-implanted and boron-doped area was formed by using one stencil mask. Elemental phosphorus was also implanted in the silicon wafer through the stencil mask window. Previously, we found an improvement in the electrical characteristics of a phosphorus-implanted emitter silicon solar cell with aluminum BSF due to the post-implantation oxidation [11]. Implantation of the phosphorus enhanced the oxidation of the silicon wafer [11]. A thick oxide layer was grown on the phosphorus-implanted line pattern, acting as a protective layer for the subsequent diffusion of boron. The details are discussed in Section 3.2.

## 3. Results and discussion

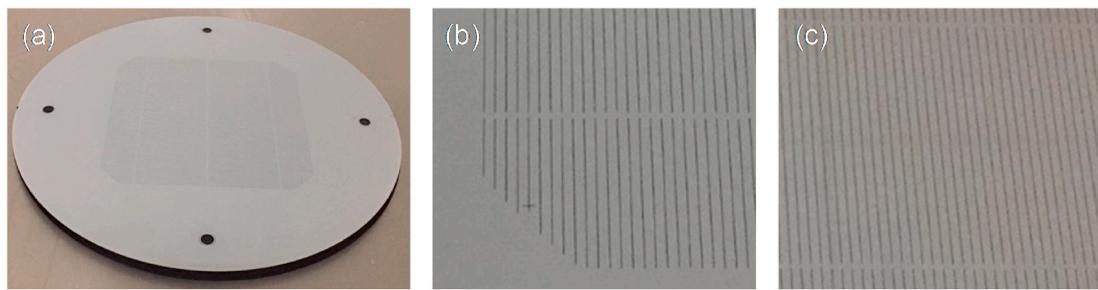
### 3.1. Characterization of the phosphorus-implanted area through silicon stencil mask opening

Fig. 2 shows a photograph of the silicon stencil mask with a diameter of 300 mm. The line-shaped contrasts are the mask window with a length of 9.8–51 mm, width of 100  $\mu\text{m}$ , and pitch of 1.73 mm. Fig. 2(b) and (c) are enlarged photos of the corner and center of the window area, respectively. The window pattern is laid out with an area of 156 mm  $\times$  156 mm, corresponding to the size of the silicon wafer for solar cells.

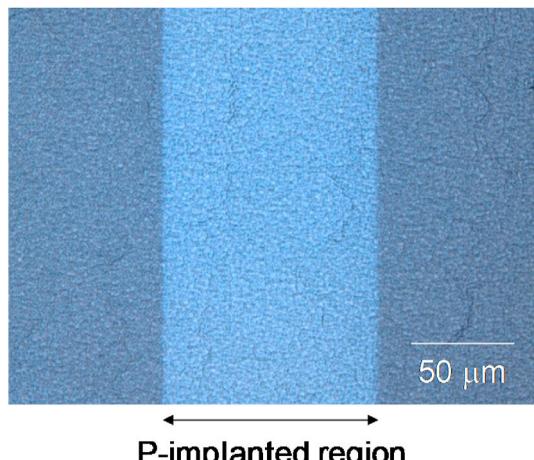
We placed a silicon wafer for solar cells in the spot facing shown in Fig. 1. Following the setup of the stencil mask, phosphorus was implanted under the conditions described in Section 2. Fig. 3 shows a laser optical microscopy image of the phosphorus-implanted silicon surface through the stencil mask window. The bright contrast indicated by the arrow corresponds to the phosphorus-implanted silicon. Under the implantation conditions employed in this study, the phosphorus-implanted silicon becomes an amorphous layer, which is clearly visible due to the difference in reflection between the amorphous layer and the crystalline silicon. The phosphorus-implanted line with a width of 100  $\mu\text{m}$  is a third of that previously reported [10]. We also observed a phosphorus-implanted pattern at an arbitrary 19 points in the wafer by using laser optical microscopy, and measured the width of the phosphorus-implanted line. Fig. 4 shows the width distribution of individual phosphorus-implanted lines. The phosphorus-implanted line width ranges from 103.1 to 105.0  $\mu\text{m}$ .

Fig. 5 shows backscattered electron images of phosphorus-implanted (left half) and non-implanted (right half) silicon observed by SEM. The left-half contrast in the image is slightly dark compared to that in the right half. The intensity of the backscattered electrons depends on the mass of the element, which makes it possible to observe the distribution of the constituent element in the matrix. Thus, we can observe the phosphorus-implanted and non-implanted silicon, although it is not sufficiently clear due to the small mass difference between the silicon and the phosphorus. The broken line is the boundary between the phosphorus-implanted and non-implanted silicon, which is determined by the contrast in the image. According to the SEM observation, the phosphorus-implanted area shows a line edge roughness of a few micrometers.

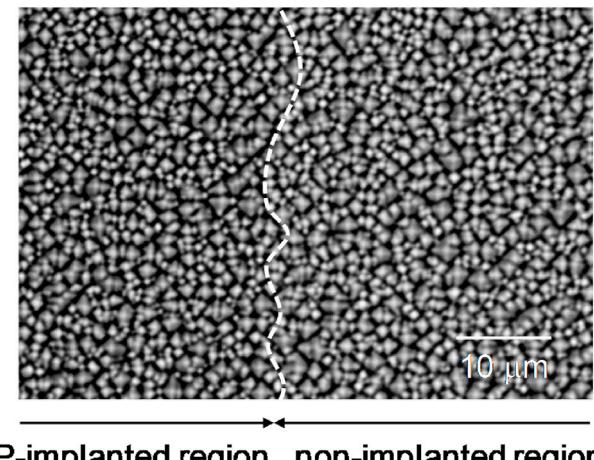
Thus, the implantation of phosphorus was implemented for the first time through a silicon stencil mask of 300 mm in diameter. Despite the large size of the mask, the phosphorus-implanted line is narrow compared to that previously reported [10]. One of the applications of



**Fig. 2.** Photos of the silicon stencil mask with a diameter of 300 mm. (a) Whole mask, and enlargement of (b) corner and (c) center of the window pattern are displayed. Line-shaped contrasts are the mask window, which is laid out with an area of 156 mm × 156 mm, corresponding to the size of the silicon wafer for solar cell.

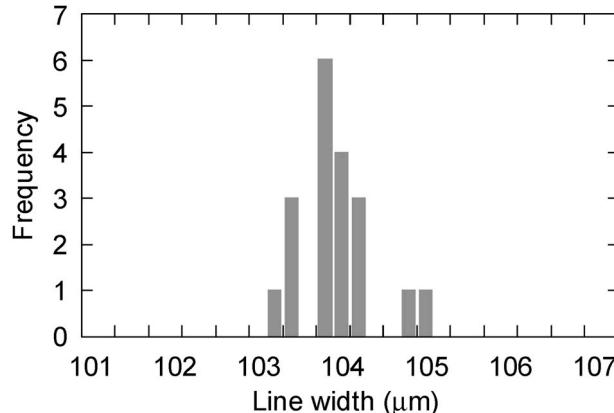


**Fig. 3.** Optical laser microscopy image of phosphorus-implanted silicon surface through the stencil mask window. Bright contrast indicated by the arrow corresponds to the phosphorus-implanted silicon.



**P-implanted region non-implanted region**

**Fig. 5.** Backscattered electron images of phosphorus-implanted (left half) and non-implanted (right half) silicon observed by SEM. The broken line is the boundary between the phosphorus-implanted and non-implanted silicon, which is determined by the contrast in the image.



**Fig. 4.** Distribution of the line width of individual phosphorus-implanted silicon through the stencil mask shown in Fig. 3. Arbitrary 19 points were observed in the wafer, and the line width was determined by the optical laser microscopy images.

stencil-masked phosphorus implantation with a narrow slit pattern is the selective emitter solar cell. This method is effective for selective emitter solar cells with fine electrode lines.

### 3.2. Fabrication process for alternative phosphorus-implanted and boron-diffused pattern via stencil mask implantation

Müller et al. previously reported the *n*-type IBC silicon solar cell with phosphorus-implanted BSF thorough a stencil mask window and subsequently a boron-diffused emitter [6,7]. Boron diffusion on BSF is blocked by a locally implanted phosphorus, resulting in the phosphorus-implanted BSF and boron-diffused emitter. The retardation of boron diffusion on phosphorus-implanted silicon is due to a Fermi level shift and the pairing of boron and phosphorus ions depending on the phosphorus doping level [12,13]. As reported previously, the phosphorus distribution in individual textures depends on several factors including the doping level, acceleration voltage, tilt angle, and twist angle. Moreover, it also depends on the process sequence for boron diffusion: diffusion of phosphorus atoms during load-in of the boat, ramp-up of temperature, and deposition of boron silicate glass (BSG). The approach reported by Müller et al. is a simplified process, but does not match our phosphorus implantation and boron diffusion process. Therefore, we propose another approach for fabricating alternative phosphorus-implanted and boron-diffused patterns on *n*-type silicon wafers based on stencil-masked phosphorus implantation as described below.

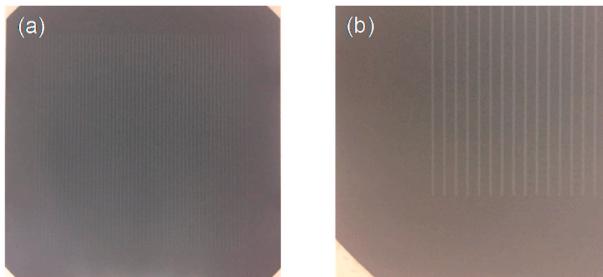
Fig. 6 shows (a) a photo of the silicon stencil mask with a diameter of 200 mm and (b) an enlarged photo of the slit pattern. An individual slit has an area 123 mm long, 0.42 mm wide, and a 1.8 mm pitch. The window pattern is laid out with an area of 125 mm × 125 mm. Following the wafer texturing on the front and rear sides with a size of 156 mm ×



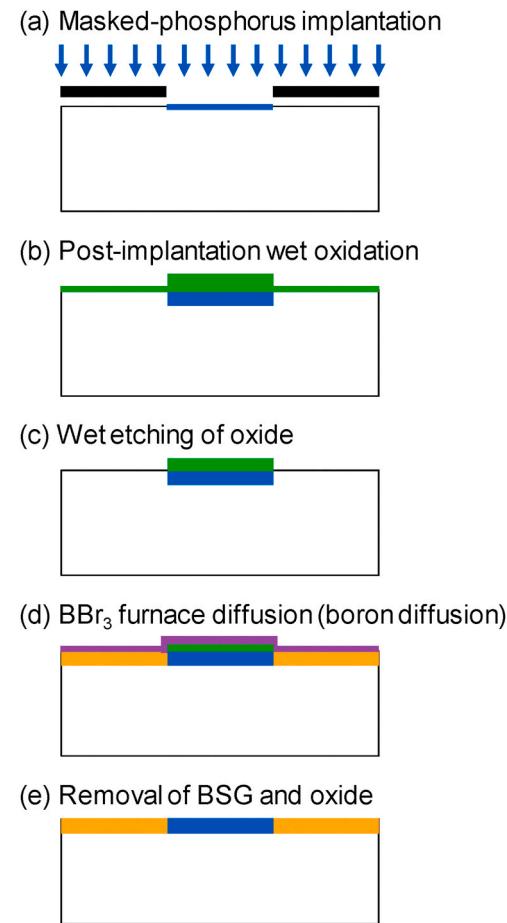
**Fig. 6.** Photos of the silicon stencil mask with a diameter of 200 mm. (a) Whole mask and (b) enlargement of the window pattern are displayed. The line-shaped window is laid out with an area of 125 mm × 125 mm.

156 mm and a thickness of 180  $\mu\text{m}$ , a wafer is placed on the base wafer shown in Fig. 1. Elemental phosphorus is implanted in the silicon wafer through the stencil mask window shown in Fig. 6. The phosphorus implantation conditions are described in Section 2. Fig. 7 shows a photograph of the phosphorus-implanted silicon wafer. The phosphorus-implanted silicon is characterized by the contrast due to the amorphous layer, as described in Section 3.1. White contrast lines are regularly arranged on the entire wafer.

Fig. 8 shows the processing steps undertaken during the fabrication of the phosphorus-implanted and boron-diffused patterns on the *n*-type silicon wafer. Following the implantation of phosphorus, wet oxidation is performed as post-implantation annealing. Enhanced oxidation on ion-implanted silicon surface was reported [14]. Here, we discuss the enhanced oxidation due to the implantation of phosphorus. Elemental phosphorus was implanted in the mirror-polished silicon wafer at an acceleration voltage of 10 keV, dose of  $4 \times 10^{15}$  atoms/cm<sup>2</sup>, tilt angle of 7°, and twist angle of 90°. Next, phosphorus-implanted and non-implanted silicon wafers were subjected to wet oxidation. The resulting oxide thickness of the phosphorus-implanted and non-implanted silicon wafer was 2050 and 410 Å, respectively. Thus, the implantation of phosphorus has quite a large effect on oxidation enhancement [11]. Fig. 9 shows the decrease in the oxide thickness after dipping in 1% HF solution at room temperature. According to the slope of the linear relationship in Fig. 9, the etching rates of oxide on the phosphorus-implanted and non-implanted silicon by 1% HF solution are 0.8 and 1.4 Å/s, respectively. Next, we discuss the blocking effect of the oxide layer on boron diffusion. Boron was thermally diffused on the oxidized silicon wafers with an oxide thickness of 0, 270, 650, and 1400 Å, which was performed in a tube furnace using liquid BBr<sub>3</sub> as a diffusion source at 975 °C for 10 min. The silicon wafer used in this experiment was a phosphorus-doped *n*-type with a sheet resistivity of 28 Ω/sq. Following the removal of BSG and oxide by dipping in HF solution, we measured the sheet resistance. Table 1 shows the average sheet resistance over the silicon wafer processed for the boron diffusion on the oxidized silicon wafer. The sheet resistances of the processed wafers with an oxide thickness of 0, 270, and 650 Å are higher than that of the initial wafer, whereas the wafer with an oxide thickness of 1400 Å is comparable in sheet resistivity to the initial wafer. This means that an



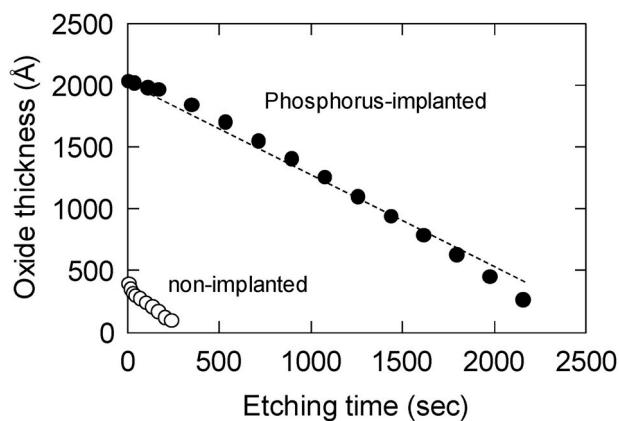
**Fig. 7.** Photos of (a) phosphorus-implanted silicon wafer through the stencil mask shown in Fig. 6 and (b) enlarged image of the phosphorus-implanted line. The phosphorus-implanted silicon is characterized as white contrast due to the amorphous layer.



**Fig. 8.** Processing steps undertaken during the fabrication of the phosphorus-implanted and boron-diffused area on the *n*-type silicon wafer based on the implantation of phosphorus through the silicon stencil mask shown in Fig. 6.

oxide layer with a thickness of at least 1400 Å can block the in-diffusion of boron.

Thus, the diffusion of boron into the silicon depends on the thickness of the oxide on the silicon. Here, we propose selective boron doping based on the combination of enhanced oxidation and etch-back of the oxide. Post-implantation annealing involves wet oxidation at 900 °C for 45 min to recover from the implantation damage and activate the phosphorus atoms. At this time, enhanced oxidation due to the phosphorus-implanted silicon was observed, as shown in Fig. 8(b). We checked the oxide thickness using an ellipsometer on the monitoring mirror wafer, which was subjected to the same process as in Fig. 8(a) and (b). The resulting oxide thickness of the phosphorus-implanted and non-implanted silicon was 3800 and 1000 Å, respectively, which thinned to 3450 and 350 Å, respectively, by dipping in 1% HF solution for 460 s, as shown in Fig. 8(c). Subsequently, boron diffusion was performed at



**Fig. 9.** Oxide thickness of phosphorus-implanted and non-implanted silicon wafer after dipping in 1% HF solution at room temperature. Elemental phosphorus was implanted in the mirror-polished silicon wafer at an acceleration voltage of 10 keV, dose of  $4 \times 10^{15}$  atoms/cm<sup>2</sup>, tilt angle of 7°, and twist angle of 90°. Next, the phosphorus-implanted and non-implanted mirror-polished silicon wafers were subjected to wet oxidation. Oxide thickness was measured using an ellipsometer.

**Table 1**

Average sheet resistance over silicon wafer subjected to boron diffusion on oxidized silicon wafer.

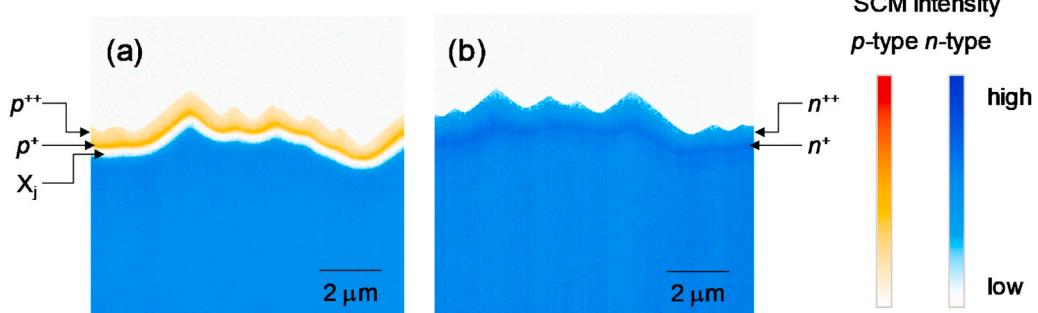
Oxide thickness (Å)	0	270	650	1400
Sheet resistance ( $\Omega/\text{sq}$ )	67.5	68.2	72.1	32.1

975 °C for 10 min, as shown in Fig. 8(d). The oxide layer on the phosphorus-implanted silicon with a thickness of 3450 Å was sufficiently thick to block the in-diffusion of boron. Finally, the BSG and oxide layer were removed by dipping in HF solution.

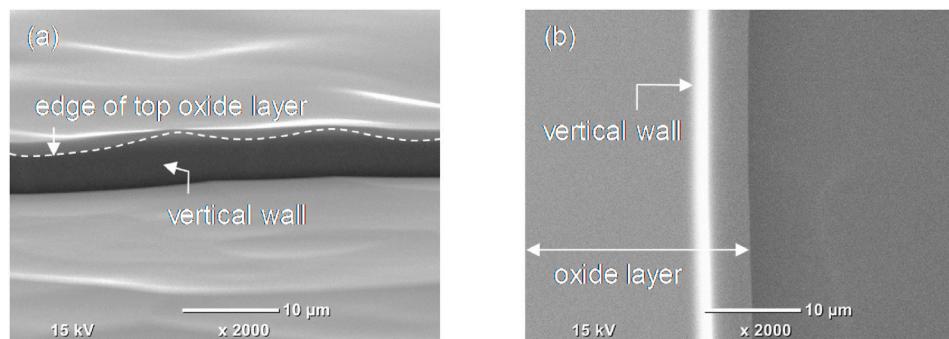
Fig. 10 shows the cross-section SCM images of the (a) boron-diffused and (b) phosphorus-implanted silicon. SCM samples were cleaved at the center of the phosphorus-implanted and boron-diffused slits. The cleavage plane was mirror polished with colloidal silica followed by SCM observation. A detailed explanation of the SCM image is given in Refs. [11]. The polarization of the observation point is determined by noting whether the SCM signal is positive or negative. In this observation, positive and negative signals correspond to the n-type and p-type region, respectively, which are colored in blue and orange, respectively. In Fig. 10(a), the sub-surface orange contrast is p-polarity due to the boron diffusion, and the blue contrast is n-polarity due to the silicon substrate. The orange contrast underneath the surface is weak, whereas it becomes strong and subsequently weak with the increase in depth from the surface. The intensity of SCM signal depends on the carrier

concentration and bias voltage applied to the sample. Smoliner et al. reported a nonmonotonic dependence of the SCM signal on the carrier concentration under the condition of an adequate bias voltage to observe the p-n junction [15]. It is known that the intensity of the SCM signals becomes weak at high and low carrier concentrations [15]. The orange contrast variation in the depth direction is due to the depth profile of the boron. Boron atoms diffuse into the bulk during  $\text{BBr}_3$  furnace diffusion process as shown in Fig. 8(d). The weak orange contrast underneath the surface is due to the high concentration of boron. Boron concentration decreases with the increase in the depth from the surface. Consequently, the SCM signal in the depth direction increases, exhibits a maximum, and then decreases, depending on the boron concentration. The white line is the p-n junction where the SCM signal equals zero. The concentration of the boron is qualitatively shown in Fig. 10(a): a high concentration region  $p^{++}$ , a medium concentration region  $p^+$  and the p-n junction depth  $X_j$ . The p-n junction is formed at a uniform depth along the texture. In Fig. 10(b), the entire image shows the blue contrast because of the n-polarity due to the implantation and substrate. The blue contrast underneath the surface is weak, whereas it becomes strong and reaches that of the substrate. The intensity of the SCM signal also becomes weak at high and low carrier concentrations, regardless of the boron or phosphorus. Phosphorus atoms diffused into the bulk during the post-implantation wet oxidation at 900 °C for 45 min and the subsequent boron diffusion process. At the same time, phosphorus atoms piled up at the interface between the silicon and oxide, resulting in the white contrast underneath the surface. The concentration of the phosphorus decreases and becomes constant at the concentration of the substrate with an increase in the depth from the surface. The concentration of the phosphorus is also qualitatively shown in Fig. 10(b): a high concentration region  $n^{++}$  and a medium concentration region  $n^+$ . The SCM signal is the result of the net carrier concentration, even if the opposite polarity carrier is included in the observation. However, an oxide layer sufficiently thick to protect the boron diffusion was grown on the phosphorus-implanted area. Moreover, the SCM image in Fig. 10(b) shows the homogeneous contrast along the texture surface. We believe that the boron diffusion is suppressed by the oxide layer on the phosphorus-implanted silicon. Thus, we fabricated alternative phosphorus-implanted and boron-diffused patterns via only one stencil mask implantation process step.

There is an issue regarding the fabrication process shown in Fig. 7: formation of gap between the phosphorus-implanted and boron-diffused silicon; further process tuning is now under way to address this issue. Previously, we proposed a fully implanted IBC silicon solar cell with a gap structure between the boron-implanted emitter and phosphorus-implanted BSF via a self-aligned process [16]. In this process, wet chemical silicon etching with alkali solution such as KOH is performed following the partial etching of the oxide layer on the silicon. The sub-surface silicon is etched off laterally and in the depth direction, resulting in a hollow structure with an overhang of the oxide layer.



**Fig. 10.** Cross-section SCM images of (a) boron-diffused and (b) phosphorus-implanted silicon. SCM samples were cleaved at the center of the phosphorus-implanted and boron-diffused line. p-type polarity and n-type polarity are displayed in orange and blue, respectively.  $p^{++}$  is a high concentration region of boron,  $p^+$  is medium concentration region of boron, and  $X_j$  is the p-n junction depth.  $n^{++}$  and  $n^+$  are high and medium concentration regions of phosphorus, respectively. . (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)



**Fig. 11.** SEM (a) bird's-eye view and (b) top-view image of typical hollow structure with overhanging oxide layer. Following the partial etching of oxide layer on silicon, wet chemical silicon etching with alkali solution such as KOH was performed. Sub-surface silicon was etched off laterally and in the depth direction, resulting in this structure.

**Fig. 11** shows an example. The stencil mask implantation process makes it possible to form the gap between the *p*- and *n*-region by using the above process. Following the etching of oxide on the non-implanted silicon shown in **Fig. 7(c)**, wet etching with alkali solution is performed to make a hollow structure with an overhang of oxide layer. Then, boron implantation is performed instead of boron diffusion. The ion beam is not irradiated on the silicon under the overhanging oxide layer as a protection layer. The distance of gap depends on the lateral etching amount of silicon under the oxide layer. This enables us to optimize a gap structure in the near future.

#### 4. Conclusions

In this study, we demonstrated ion implantation on silicon wafers by using silicon stencil masks with diameters of 200 and 300 mm. Phosphorus was implanted in silicon wafers for solar cells through a silicon stencil mask with a diameter of 300 mm. The window pattern was laid out with an area of 156 mm × 156 mm. The mask has a line-shaped window with a length of 9.8–51 mm, width of 100 μm, and pitch of 1.73 mm. The phosphorus-implanted silicon was characterized by using optical laser microscopy and SEM. The phosphorus-implanted line is 100 μm wide with an edge roughness of a few micrometers. We also performed phosphorus implantation through a silicon stencil mask with a diameter of 200 mm. This mask has a line-shaped window 123 mm long, 0.42 mm wide, and a 1.8 mm pitch. The window pattern was laid out with an area of 125 mm × 125 mm. The aperture ratio of the mask was quite high. Based on the implantation of phosphorus by using the stencil mask with a diameter of 200 mm, we proposed the fabrication process of alternative phosphorus-implanted and boron-diffused patterns on silicon wafers by using only one stencil mask. A thick oxide layer was formed on the phosphorus-implanted silicon with a slit pattern during post-implantation wet oxidation, acting as a protective layer for the subsequent diffusion of boron. SCM observation revealed *p*-type polarity in the boron-diffused silicon and *n*-type in the phosphorus-implanted silicon with homogeneous contrast along the textured surface. Further process tuning is under investigation to attain *p-n* isolation between the phosphorus- and boron-doped silicon based on the silicon stencil mask implantation. Thus, silicon stencil-masked ion implantation has potential as a selective doping method in silicon wafers for solar cells.

#### CRediT authorship contribution statement

**Katsuto Tanahashi:** Conceptualization, Data curation, Investigation, Writing - original draft. **Masaaki Moriya:** Investigation.

**Katsuhiko Shirasawa:** Conceptualization, Writing - review & editing. **Hidetaka Takato:** Supervision, Writing - review & editing.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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