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Impacts of silicon carbide defects on electrical characteristics of SiC devices

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ABSTRACT

With more than thirty years of research and development until commercialization, performance, reliability, and robustness of silicon carbide (SiC) based devices have been improved significantly due to drastic reduction in crystal defects from the well-controlled processes of crystal growth and device fabrication. It is crucial to investigate the effects of SiC crystal defects on the electrical characteristics of devices. Here, an up-to-date development of the correlation between crystal defects of SiC with electrical performance of the devices has been reviewed. The effect of defects on the electrical parameters of the device and the failure mechanism are discussed, and the development of SiC in recent years is prospected.

I. INTRODUCTION

With the rapid development of power electronic technology to address the stringent performance and complicated requirements of semiconductor power devices to serve both commercial and specialized applications, selection of an appropriate semiconductor to fabricate the devices would be extremely critical to ensure the performance, reliability, robustness, and safety aspects of the devices that can be achieved.[1–3] Table I shows the physical properties of SiC compared with Si, GaAs, and other wide bandgap materials such as GaN, diamond, and Ga_2O_3. Due to limitation of material properties in the commonly used Si and narrower bandgap of GaAs, silicon carbide (SiC) as the third generation of semiconductors has been identified and widely accepted as one of the wide-bandgap semiconductors that offers superior material properties for this application.[4,5] SiC is a mechanically rugged, electrically excellent, chemically and thermally stable semiconductor with bandgap, saturated electron velocity, thermal conductivity, and breakdown field higher than those of Si.[6] Some physical properties of GaN and 4H–SiC are similar, but due to the limited growth size of the GaN single crystal substrate, epitaxial sheets are usually grown on heterogeneous substrates (sapphire, SiC, and Si).[7,8] Still, there are lattice mismatch and thermal mismatch problems between epitaxial layer GaN and a heterogeneous substrate, and the efficiency is reduced. Researchers are striving to break through the preparation technology of the GaN single crystal substrate. In addition, GaN contains a large number of defects in the small size range, and the high-density defects make the application efficiency of GaN low. The most promising semiconductor material should be ultra-wide bandgap (UWBG) semiconductors. One such UWBG semiconductor is diamond,[9,10] which exhibits the largest thermal conductivity and bandgap of all the materials listed in Table I. Additionally, diamond displays the highest electron mobility and a bandgap that is significantly larger than that of other semiconductor materials. However, the manufacturing technology of materials and devices is far less mature and developed than silicon carbide. Diamond is still in the basic research stage to be broken through, there are a lot of scientific problems in materials, devices, and other aspects to be overcome, such as the high cost of diamond materials, and small size is the main obstacle restricting the development of diamond power electronics, among which, large size splicing single crystals, heteroepitaxy, doping, device reliability, thin

TABLE I. Physical properties (room temperature values) of silicon, GaAs, GaN, diamond, Ga_2O_3, and silicon carbide (4H).[17–21]

Property	Silicon	GaAs	GaN	Diamond	Ga_2O_3	4H–SiC
Bandgap (eV)	1.1	1.43	3.45	5.45	4.5	3.26
Saturated electron velocity (10^7 cm s^{-1})	1.0	1.0	2.2	2.7	~2	2.0
Thermal conductivity (W cm^{-1} K^{-1})	1.5	0.46	1.3	22	0.11–0.27	4.9
Breakdown field (10^6 V cm^{-1})	0.3	0.4	3.0	5.7	>7	3.2
Electron mobility (cm^2 V^{-1} s^{-1})	1430	8500	900	1900	300	900
Melting point (°C)	1420	1240	2500	4000	1740	2830

polishing, and so on are the existing problems at this stage. Another ultra-wide bandgap semiconductor material is Ga_2O_3,[11,12] whose exceptional physical properties are largely attributed to its remarkably large bandgap energy of 4.5 eV. It is also noteworthy that substantial bulk single crystals can be produced through melt growth. The former results in enhanced device performance for high-breakdown-voltage and high-power applications, whereas the latter facilitates reduced device manufacturing costs. The thermal conductivity of Ga_2O_3 is markedly diminished in comparison to that of other power semiconductors, as outlined in Table I. This deficiency in thermal conductivity not only impedes the performance of high-power devices but also constrains their long-term reliability. Consequently, thermal management arises as a pivotal technical challenge for the forthcoming practical applications and commercialization of Ga_2O_3 RF and power devices. With these excellent properties, it enables SiC to be used as a substrate to fabricate high-efficiency power electronic devices with high voltage, high temperatures, and high frequencies.[13–16]

At present, SiC-based diodes and MOSFETs have been widely used in electric vehicles, charging piles, new energy power generation (solar, wind power), UPS, industrial power, rail transit, and other fields.[22–24] Figure 1 shows on-state characteristics of several power devices with a breakdown voltage of 1200 V, besides PiN with a rated voltage at 6.5 kV, and $V_{GS} = 20$ V for MOSFETs. Different types of devices have different specific on-resistance, and SiC power MOSFETs deliver a high current density of 250 A/cm^2 at a considerably lower drain voltage of about 1.1 V than other devices, resulting in a much smaller conduction loss compared to other devices. However, to go for a high power rating with higher voltage for applications in smart grids, high voltage transmission and distribution, a higher quality of SiC epitaxial with lower defect density is required for the development of super junction MOSFET, IGBT (Insulated Gate Bipolar Transistor), etc. Common defects in SiC epitaxial layers include nano-scale pits, basal plane dislocations, stacking faults, triangular defects, micropipes, comet defects, and carrot defects.[25–27] These defects adversely affect the characteristics, and reduce the reliability and production yield of the devices.[28–30] Therefore, it is essential to correlate the types of defects in the epitaxial layer to the performance, reliability, and robustness of the devices.[31] Some review articles introduce the defects in 4H–SiC and the impact of defects on SiC devices.[32–35]

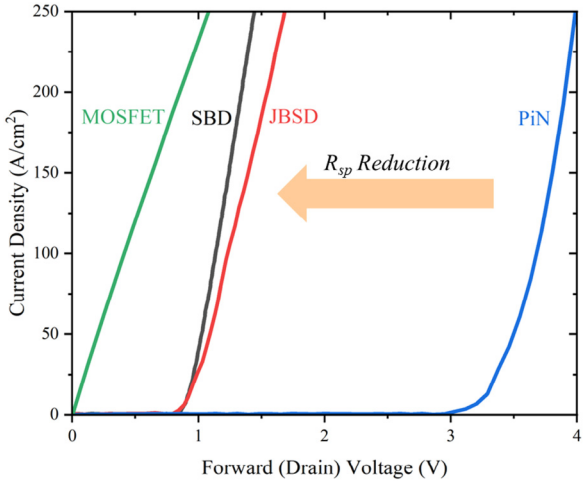

FIG. 1. On-state characteristics of SiC power devices, where the blocking voltage of the devices is 1200 V besides 6.5 kV PiN, and $V_{GS} = 20$ V for MOSFETs.

This paper introduces the defects of SiC epi and their impact on the device, including nano-scale pits, basal plane dislocation (BPD), stacking fault (SF), and so on. In particular, it elucidates the mechanism of device degradation or failure caused by different defects and introduces several defects and their effects on the long-term reliability of the device, as well as defects induced by the implantation process. These topics are rarely addressed in other articles, with the exception of the effects of defects on the device in CP (chip probing) tests. This review connects epilayer defects and devices, which provides references to research workers to improve the epitaxial growth technique and cull the "bad" dies.

II. DEFECTS OF SiC EPITAXIAL LAYERS

A. Nano-scale pits (or epi-layer growth pits)

Nano-scale pits or epitaxial layer growth pits located on the surface of an epitaxial layer originate from the propagation of threading dislocation penetrating through the SiC epitaxial layer such as in the drift region (Fig. 2). The typically reported dimensions [inset of Fig. 2(b)] of nano-scale pits are width, depth, and angle of 160–300 nm, approximately 45 nm, and 100°–175°,[36] respectively. In general, these nano-scale pits are usually found in

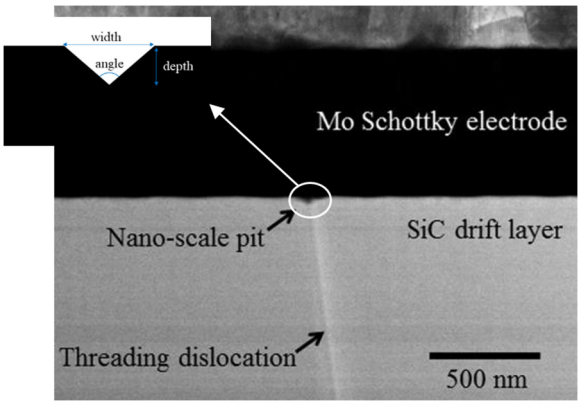

FIG. 2. Cross-sectional morphology of micrographs from a scanning transmission electron microscope of a nano-scale pit extended from a threading dislocation. Reproduced with permission from Fujiwara *et al.*, Appl. Phys. Lett. **100**(24), 242102 (2012). Copyright 2012 AIP Publishing LLC.

AFM detection, and their cross-sectional analysis shows that there are dislocation lines below the pits.[37]

B. Basal plane dislocation (BPD)

Basal plane dislocations (BPDs) in the SiC substrate can convert and transfer into the SiC epilayer as either BPD with Burgers vector of 1/3 [11$\bar{2}$0] or threading edge dislocation (TED) and stacking fault (SF).[39–41] When inclusion occurs in the epitaxial growth process, it will distort the surrounding lattice and release stress through the formation of BPD, which leads to the formation of a large number of BPD dislocations (as indicated by bright lines in the UVPL image) as seen in Fig. 3(a). The darker regions in Fig. 3(b), located at the top and bottom of the inclusion, indicate the strain fields corresponding to the BPD area. Figures 3(c) and 3(d) display the micro-Raman result of the inclusion, which is typical of the 3C–SiC polytype. BPD is not visible under a normal light microscope and is usually detected by a photoluminescence (PL) spectrometer, with images showing a linear pattern. In addition, BPD will form a shell-shaped corrosion pit after corrosion by molten KOH.

C. Stacking fault (SF)

Principally, the formation of stacking faults (SFs) is caused by the dissociation of BPDs to Shockley partial dislocations,[43] and SFs could nucleate at threading dislocations, low angle grain boundaries, and SFs in substrates.[44–46] Generally, SFs show triangular shapes in the PL mode,[47] and are typically classified into two categories according to whether they are transformed by defects: In-grown stacking faults (IGSFs) and stacking faults extended from substrates. Various types of stacking faults can be formed in SiC epitaxy, such as Shockley type and Frank type, because a small amount of stacking energy disorder between crystal planes can lead to considerable irregularity in the stacking order. Figure 4(a) depicts the PL spectra of 380–480 nm, wherein the peak value of region A is 395 nm, suggesting the presence of 4H–SiC, and the peak value of region B is 425 nm, denoting the existence of defects. The μ-PL intensity map in Fig. 4(b) reveals the characteristic Shockley SFs of triangular shapes located in region B.

D. Triangular defect

In the process of SiC epitaxial growth, particles, stacking faults, or 3C–SiC affect the flow of atomic steps, which leads to the formation of defects in triangular shapes on the surface of SiC epitaxial layers, also known as triangular defects.[49,50] Figure 5 illustrates a triangular defect with a particle at the head of the defect, situated on the cutting path, and two corners extending into the terminal area of the MOSFET dies. The triangular region is the mixed crystalline region of 3C–SiC and 4H–SiC.[51,52] Also, the triangular defects originate from the interface of the epitaxial layer/substrate, extending to the epitaxial layer. The length of triangular defects along the step flow direction can be obtained as follows:

$$L = d/\sin\theta, \tag{1}$$

where d is the thickness of the 4H–SiC epitaxial layer and θ is the deflection angle of the substrates. As the lattice constants of 3C–SiC and 4H–SiC are different, there is a strain field around the triangular defects.

E. Micropipes

Micropipes in epilayers are usually extended from micropipes in the substrate along the c axis in 4H–SiC, whose Burgers vector is several times higher than TSD's Burgers vector 1c⟨0001⟩.[53] The butterfly-shaped bright spot of the micropipe can be observed by polarized transmitted light in Fig. 6(a), and the micropipe is exhibited as a black hole in the PL luminescence image of Fig. 6(b). Micropipes are believed to be hollow super threading screw dislocations, whose diameter can be up to one-tenth of a micrometer. Under certain growth conditions, micropipes in the substrate can be partially or completely transformed into threading screw dislocations during epitaxial growth, which is defined as micropipes closure. Current processes have been able to reduce the number of micropipes to very low or even none.[54]

F. Comet defects

Comet defects are comet-like defects on the surface of the SiC epilayer, consisting of a core and a tail, as shown in Figure 7(a). Arrows are used to denote 3C triangular inclusions, which are buried within a 4H epitaxial film. The direction of comet defects is parallel with the [11$\bar{2}$0] direction. The length of comet defects meets formula (1). Figure 7(b) illustrates that comet defects usually start from falling particles with the tail portion formed during the step-flow growth process, and the core and tail are observed to contain 3C–SiC inclusions,[55] with great roughness on comet defects' surface.

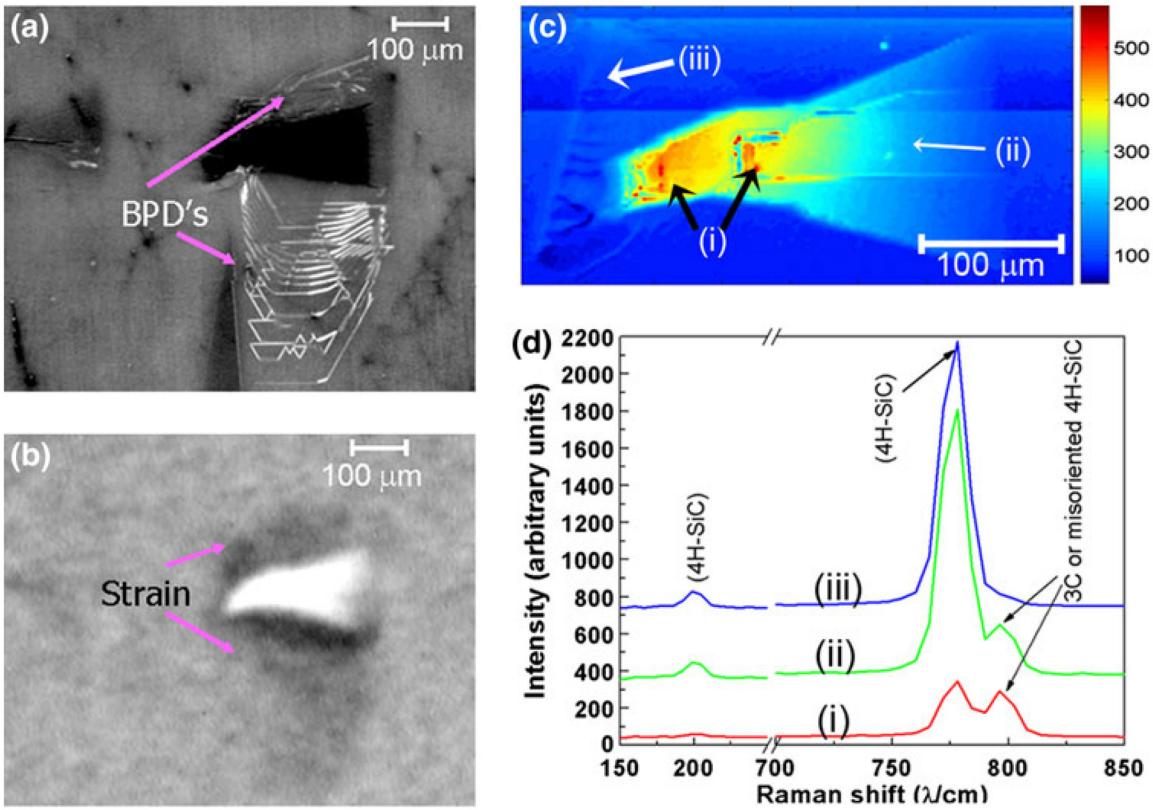

FIG. 3. (a) UVPL image of an inclusion formed during epi growth and the cluster of BPDs and the inclusion induces around it due to local stress. (b) High-resolution x-ray topography (HRXT) image of the same position. (c) Micro-Raman intensity map of 796 cm^{-1} (3C) peak at the same position. (d) Raman spectra of inclusions inside [(i) and (ii)] and outside (iii). Reproduced with permission from Mahadik *et al.*, J. Electron. Mater. **40**(4), 413–418 (2011). Copyright 2011 Springer Nature.

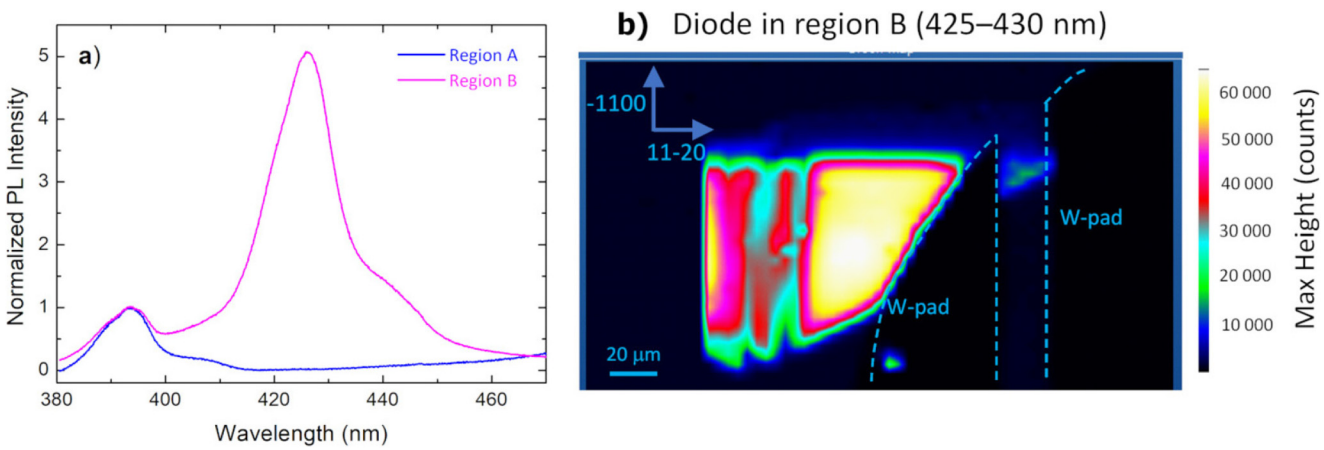

FIG. 4. (a) PL spectra in the 380–480 nm range acquired in the (region A) reference region and the SF defect region (region B) and (b) μ-PL intensity maps in the 425–430 nm range obtained in the SF defect region. Reproduced with permission from Vivona *et al.*, Appl. Phys. Lett. **123**(7), 072101 (2023). Copyright 2023 AIP Publishing LLC.

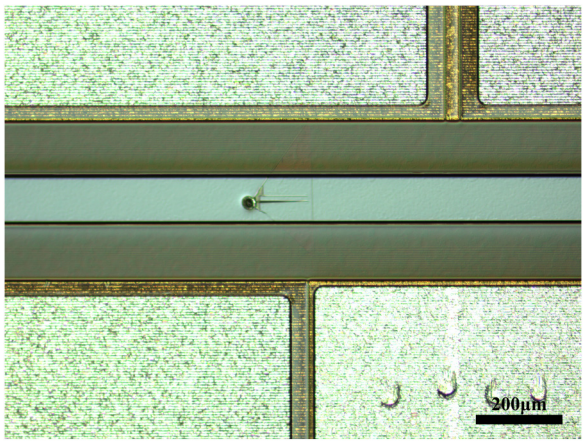

FIG. 5. Images of triangular defects.

G. Carrot defects

Carrot defects are carrot-like defects on the surface of the SiC epilayer, without core structures, as shown in Fig. 8(a). The carrot defect exhibited a groove that was almost parallel to the [11$\bar{2}$0] direction. This groove was attributed to surface roughness, which was induced by the prismatic SF. The pit, which was formed due to a threading dislocation, was discernible at the leading side of the carrot defect in the mirror projection electron microscopy (MPJ) image. Figure 8(b) is a schematic diagram of Fig. 8(a). The length of carrot defects conforms to formula (1), and the carrot defects usually originate from threading screw dislocations in the substrate.[55]

A summary of the aforementioned defects can be found in Table II, which outlines the nature of the defect, the method of detection, and the density within the wafer. Figure 9 illustrates the schematic diagram of various defects that may be presented on a silicon carbide wafer. Generally, killer defects in the epitaxial layers are recognized as micropipes, carrots, triangular defects, and large topographic defects.[58,59]

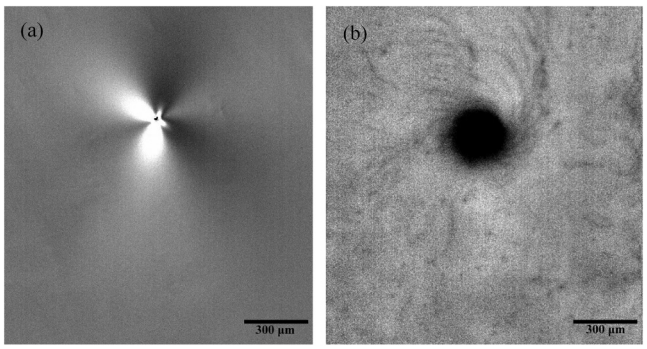

FIG. 6. (a) Differential interference image of a micropipe and (b) PL luminescence image of a micropipe.

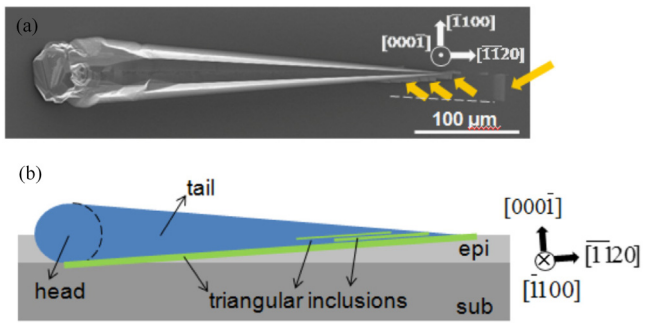

FIG. 7. (a) A surface-view scanning electron microscopy (SEM) image of a comet defect and (b) a cross-sectional schematic of a comet defect. Reproduced with permission from Yamashita *et al.*, J. Cryst. Growth. **416**, 142–147 (2015). Copyright 2015 Elsevier.

III. THE EFFECT OF DEFECTS ON ELECTRICAL CHARACTERISTICS

A. The effect of nano-scale pits on SiC devices

Studies have shown that the leakage current density in the Schottky barrier diodes (SBDs) and junction barrier Schottky diodes (JBSDs) with nano-scale pits become larger than those without nano-scale pits, but nano-scale pits have little effect on the leakage current density in p-n junction diodes (PNDs),[38,60] as shown in Fig. 10(a). However, Kudou *et al.* found that epi-layer growth pit density does not affect the leakage current of SBDs and lifetime of constant current time-dependent dielectric breakdown.[61] This is because different growth pit shapes are formed by different growth conditions on the epitaxial layers. In addition, the growth pits have wider and shallower shapes that do not affect the leakage current of SBDs and lifetime of constant current time-dependent dielectric breakdown.[60,62,63] When reverse voltage is applied to the SiC device, the maximum electric field strength is found at the interface between metal and SiC surfaces. If there is a nano-scale pit, the electric field will be concentrated at the nano-scale pit, as shown in Fig. 10(b), so the leakage current will be generated from the nano-scale pit. The deeper and narrower the nano-scale pits, the higher the leakage current because of the concentration of the electric field. Nevertheless, the leakage current of PN diodes is not affected by nano-scale pits, due to the fact that the maximum electric field is formed at the PN junction when applied with reverse voltage, rather than the interface of metal and SiC surfaces. The magnitude of increase in the leakage current of nano-scale pits is typically below 1 mA. The blocking voltage of SiC SBDs or MOSFET devices is typically within the range of 650–1700 V, while the forward voltage drop is only 1.2–1.6 V, which is considerably smaller than the blocking voltage. Consequently, the defect has a negligible impact on the forward characteristics.

B. The effect of BPDs on SiC devices

The reliability of metal-oxide-semiconductor (MOS) could degrade because of BPD below the thermal oxide forming area.[64]

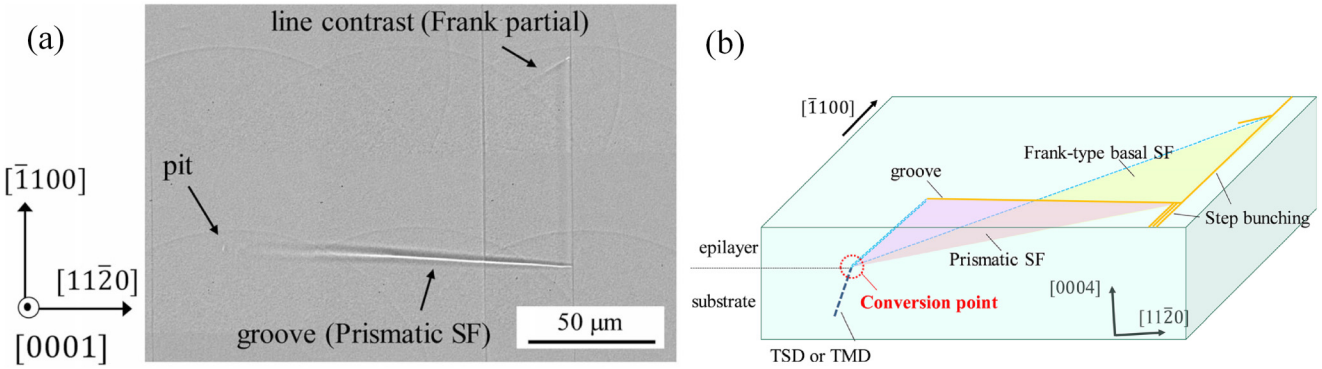

FIG. 8. (a) Mirror projection electron microscopy (MPJ) image of a carrot defect, and (b) schematic diagram of the carrot defect. Reproduced with permission from Sako *et al.*, J. Electron. Mater. **49**(9), 5213–5218 (2020). Copyright 2020 Springer Nature.

BPDs affect metal oxide semiconductor field effect transistors (MOSFETs) by increasing the leakage current and on-resistance (Ron) [see Fig. 11(a)], Vsd shift, making MOSFETs degradation and limiting SiC devices' applications.[41] BPDs could cause PiN diode leakage current rise, distinct breakdown voltage reduction,[65] and forward voltage increase. This paper[66] proposed the diffusion process that epitaxial wafer was annealed for 2 h at 1800 °C under high vacuum, restraining the forward voltage drift of 4H–SiC PiN diodes. When the p-n junction is forward-biased, the electron–hole recombination provides energy to motivate the nucleation and expansion of Shockley-type stacking faults (SSFs).[67] The SSFs serve as quantum wells to capture electrons, as shown in Figs. 11(b)–11(d), where electrons and holes recombine lessening the minority carrier lifetime and decreasing the carrier flow.[68] Also, when the p-n junction is reverse-biased, the SSFs act as a serious leakage current path.[69] These phenomena are also known as "bipolar degradation," which could have a devastating impact on the reliability of SiC bipolar devices.[15]

C. The effect of SFs on SiC devices

The stacking faults (SFs) can be grossly divided into two groups: in-grown stacking faults and expanded stacking faults. When occurring in the process of epitaxial growth, the SFs are described as in-grown stacking faults with 3C–SiC or 8H–SiC structures,[71,72] and the vast majority of these faults are Shockley SFs, which occur through slippage in the base plane. When occurring after a stress test, for example, electric stress,[73–75] the SFs are described as expanded stacking faults, which were introduced in the previous section. In this section, in-grown stacking faults are described more. In-grown stacking faults could cause the leakage current to increase and the breakdown voltage to decrease for SBDs, the reason of which is that a low Schottky barrier height enhances the tunneling current when the devices are applied at high electric fields.[76–78] Also, the same is true for JBSDs, as shown in Fig. 12. In addition, it is found that the increase of specific on-resistance and degradation of forward I–V characteristic of SBDs with in-grown stacking faults can be attributed to carrier traps formed by in-grown stacking faults.[79] These in-grown stacking faults could also cause the forward voltage to drop and on-resistance to increase for PiNs, which would be due to the current transport decrease because in-grown stacking faults capture electrons and reduce the carrier lifetime.[79,80] Some MOSFETs fail with increased leakage current because of the existence of SFs.[81] In order to reduce in-grown stacking faults, someone found that the introduction of source gases at a relatively high temperature in the initial epilayer-grown stage could remove damage of the substrate surfaces, inhibiting the formation of SFs.[82]

TABLE II. Characteristics of different defects in silicon carbide epitaxy.

Defects	Burgers vector	Major direction	Inspection method	Typical density (cm^{-2})
TEDs	⟨11$\bar{2}$0⟩/3	⟨0001⟩	KOH, XRT	≤5000
TSDs	n⟨0001⟩ (n = 1,2)	⟨0001⟩	KOH, XRT	≤5000
BPDs	⟨11$\bar{2}$0⟩/3	⟨11$\bar{2}$0⟩	KOH, PL	≤0.5
SFs	Shockley:⟨1$\bar{1}$00⟩/3 Frank:⟨0001⟩/n	In {0001} plane	PL, TEM	≤1
Micropipes	n⟨0001⟩ (n>2)	⟨0001⟩	KOH, SEM	0–0.1
Triangular defects	…	In {0001} plane	OM, SEM	≤0.2
Comet defects	…	In {0001} plane	OM, SEM	≤0.1
Carrot defects	…	In {0001} plane	OM, SEM	≤0.1

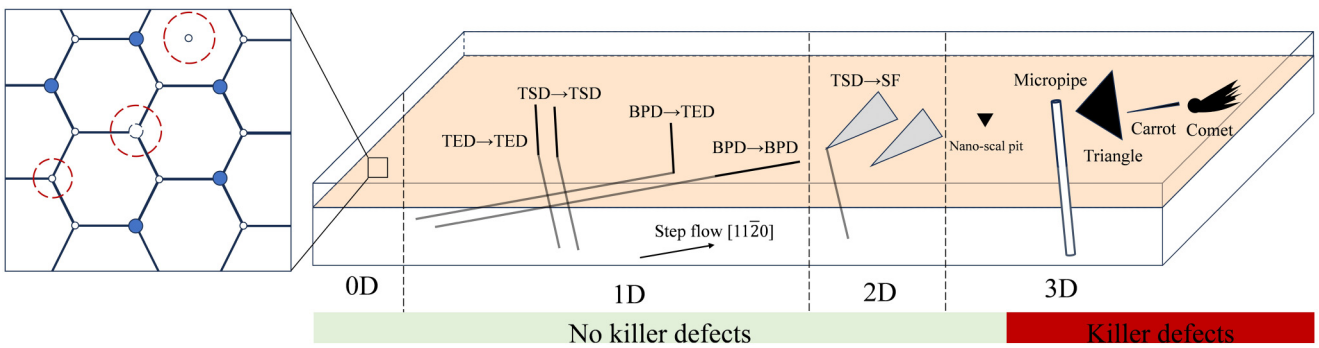

FIG. 9. Various defects in silicon carbide wafers.

D. The effect of triangular defects and other defects on SiC devices

Triangular defects are the "killer" defects.[83,84] The triangular defects have a great influence on the leakage current of SiC devices.[85] During epitaxial growth, the C/Si ratio increases, the epitaxial quality becomes worse, the triangular defect density becomes higher, the reverse leakage current of SBDs increases gradually, and the spectral noise density increases.[49] In addition, triangular defects can cause a sudden increase in the reverse leakage current and abnormal forward characteristics of the JBS diodes.[50,86] Similarly, triangular defects can lead to increased reverse leakage current and abnormal forward characteristics of the PiN diodes, as well as longer reverse recovery times.[87] It has been reported that triangular defects containing cubic 3C–SiC inclusions are formed during epitaxial growth, so the device barrier is reduced, affecting the reverse characteristics of SiC devices and reducing the blocking voltage.[58,88] Normally, diodes with triangular defects exhibit high leakage and can withstand voltages as low as a few volts (when the leakage is 100 μA or 1 mA). In forward characteristics measurement, diodes (e.g., PiNs and JBSDs) with triangular defects have a small current path at a low bias voltage, whereas normal diodes are not turned on.[87,89,90] However, this phenomenon has not been fully analyzed in past articles. In this paper,[91] it is proposed that the density of SiC epitaxial surface defects decreases sharply from 1.01 to 0.14 cm^{-2} after the optimization of CMP treatment and *in situ* etching time, especially for triangular defects, so that the forward and reverse *I–V* characteristics of JBS diodes become better.

Micropipes will lead to a surge of leakage current in SiC devices, especially for SBDs and MOSFETs.[59,85,92,93] The reverse blocking performance is significantly reduced.[94–97] The micropipes are considered to be the direct leakage path through the power device.[85,98–100]

Carrot defects have an obvious effect on SiC devices, which will increase the leakage current of SBDs.[55,85] Similarly,

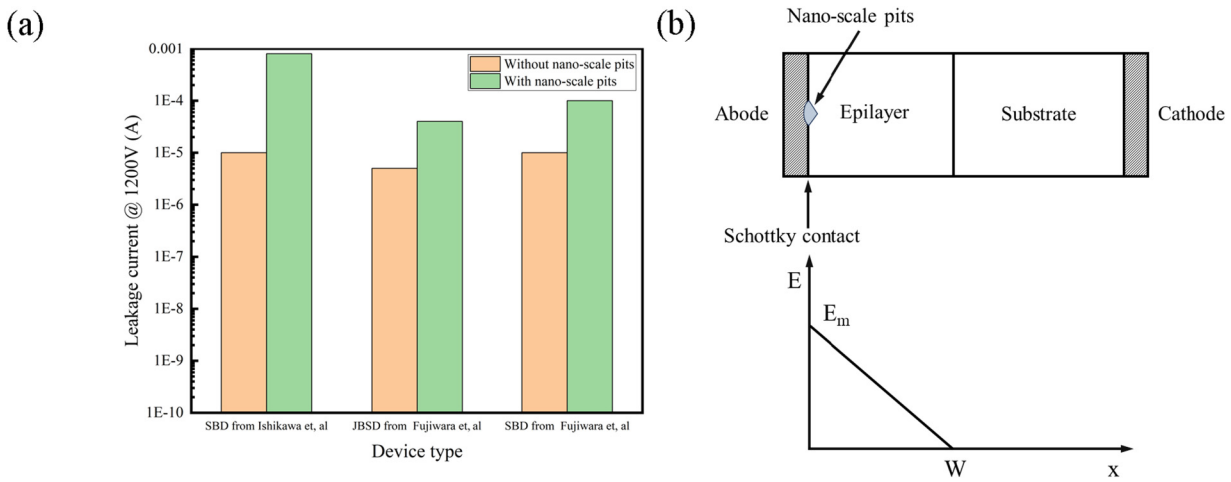

FIG. 10. (a) The leakage current of devices from different articles;[38,60,63] (b) Schottky structure with nano-scale pits and electric field distribution when reverse voltage is applied.

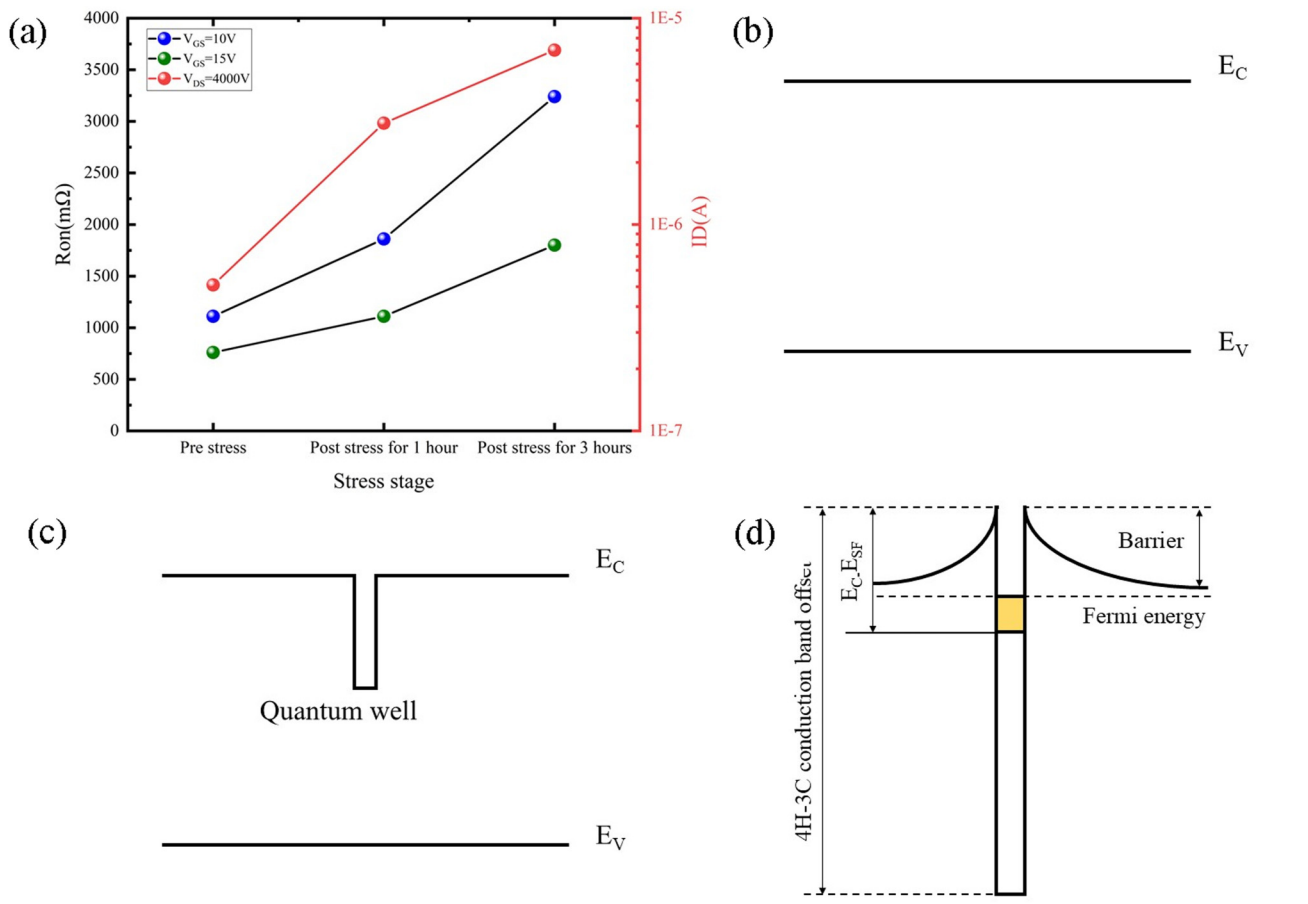

FIG. 11. The effect of expanded SF by BPDs on devices: (a) the on-resistance and leakage current under different electrical stress stages for MOSFETs;[67] (b) normal 4H–SiC band structures; (c) after SF expands, the local conduction band decreases; (d) after trapping electrons, the conduction band raises and a conduction barrier forms.[70]

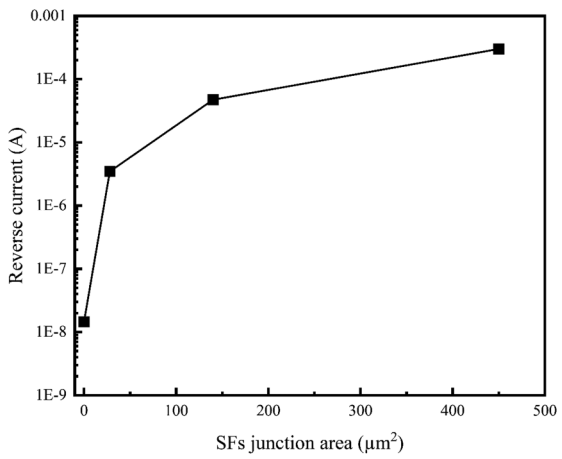

FIG. 12. The relationship between SF's junction area and reverse current at reverse voltage = 500 V for JBSDs.[71]

PiN diodes containing carrot defects exhibit higher leakage current and lower breakdown voltage.[101] The barrier height of devices containing carrot defects is lower than the barrier height of no-defect devices, and the tunneling current at high electric fields is enhanced.[58]

Comet defects on the electrical performance of the device are less relevant in literature, so it is not mentioned here, but the comet belongs to the morphological defects, and the same will affect the device breakdown and leakage.

The leakage current growth for different defects is plotted as shown in Fig. 13, and the leakage current growth is as follows:

$$G = (Ir_{\text{defect}} - Ir_{\text{ref}})/\text{Ir}_{\text{ref}}\,, \tag{2}$$

where Ir_{defect} is leakage current values of the device with defect, Ir_{ref} is leakage current values of the reference device, and the leakage current growth of killer defects is much larger than that of no-killer defects.

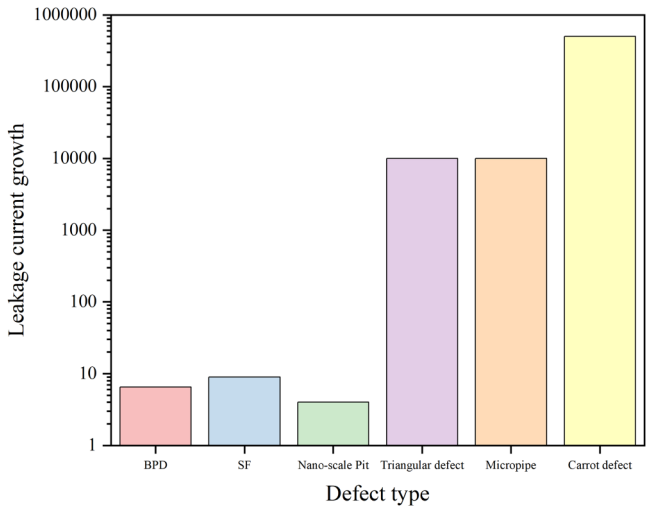

FIG. 13. The leakage current growth for different defects.[55,60,67,85,86,102]

E. The effect of threading dislocations on SiC devices in long-term reliability

There is another situation to note here: some devices fail in long-term applications due to defects.

Research studies[103] show that 4H–SiC MOSFETs experienced dielectric breakdown after three months of reverse bias stress at high temperatures, and examination of the failed device revealed a threading dislocation (TD) at the failure location. In the JEFT region of simulated MOSFETs, the oxide electric field of the structure comprising threading dislocation is 0.3% larger than that of the ideal structure's, at the same condition. The bandgap of threading dislocation is 2.3 eV, E_V of which is 1 eV higher than the ideal 4H–SiC, and E_C is the same. High E_V position for threading dislocation results in a quantum well and strengthens the hole injection into the oxide layer, so the hole current through the oxide layer could rise, which accelerates the dielectric breakdown and does harm to MOSFET gate oxide reliability.

In this paper,[104] MOS capacitors with arch-shaped pits failed in TDDB experimental. They think that the dislocations do not contribute to failures directly, but the surface morphology formed by threading dislocations produces extrinsic failure for gate oxide.

After the HTRB test was typically applied to the device at high temperatures (140 °C), reverse bias was 520 V and performed for 30 h. A small depression was found by Em.Mi emission in failed MOSFET with high leakage current, which results from perturbation in step flow growth at a threading dislocation.[105] Hence, electric field crowding is formed when 520 V is applied, and the device with depression performance deteriorates gradually until it fails.

F. The effect of defects induced by the implantation process

After the implantation process, there is degradation in the quality of the diode, which is caused by the emergence of defects in the material being studied.[106] Consequently, this leads to changes in both slope and intercept in the I–V curve, resulting in a reduction of barrier height and enlargement of ideality factor of the device.

Carrier lifetime and defect distributions were analyzed in 4H–SiC SJ-MOSFETs produced through ion implantation.[107] It was found that the carrier lifetimes of the sample within the SJ structure by Al ion implantation were shorter compared to those in the sample without the SJ structure. Deep levels were observed in the p-type regions of the SJ structures using DLTS (deep level transient spectroscopy), indicating that the defects introduced by Al ion implantation led to decreased carrier lifetimes.

There is research that BPDs are formed after Al implantation and anneal process.[108] When a forward current stress test is performed, electron–hole pairs are injected and recombined at BPDs, promoting the conversion of BPDs to Shockley stacking faults and, thereby, contributing to the increase of resistance and leakage current for MOSFETs.

As we have seen, defects can deteriorate devices' characteristics and reliability. Devices with triangular defects, carrot defects,

TABLE III. Effects of silicon carbide defects on the electrical characteristics of devices. BV, blocking/breakdown voltage; Vf, forward voltage; IR, leakage current; ID, zero gate voltage drain current; ron, on-resistance; Vsd, diode forward voltage; trr, reverse recover time; IF, a small leakage current path at a low forward bias voltage, whereas normal diodes are not turned on.

Device type \ Defect type	1	2	3	4	5	6
	Nano-scale pits	BPDs	SFs	Triangular defects	Micropipes	Carrot defects
SBD	IR↑[36,38,60–63,109]		IR↑, BV↓[76–78], Ron↑, Vf↑[79]	BV↓[49]	IR↑[59,85]	IR↑[55,85]
JBSD	IR↑[38,60]		IR↑[71,102]	IF↑, IR↑, BV↓[50,84,86,90]		
PiN		Vf↑[65,66,110]	Ron↑, Vf↑[79,80]	IF↑, IR↑, trr↑[87,89]		IR↑, BV↓[101]
MOSFET	Reliability↓[37]	ID↑, Ron↑, Vsd shift[41,47,67,74,102,108,111]	ID↑, Ron↑[81,102]	ID↑, BV↓[50]	ID↑[59,85]	

BPDs, and micropipes are more affected, but devices with carrot defects, SFs, and nano-scale pits are less affected. Moreover, the effect of silicon carbide defects on the electrical characteristics of devices is summarized in Table III.

IV. CONCLUSION

In this review article, we describe the defects in the epitaxial layer of silicon carbide and review the influence on silicon carbide devices, providing a reference for improving the yield of silicon carbide devices. Defects will inevitably be inherited or introduced in the process of epitaxial growth. These defects will affect the performance of the device to varying degrees, reduce the yield of the device, and hinder the promotion and application of 4H–SiC materials in the field of power electronic devices, so the research and suppression of epitaxy surface defects become the focus of 4H–SiC epitaxy growth. High-quality seed crystal is the key to growing high-quality SiC crystals. The seed crystal without obvious defects is selected, and surface polishing of the seed crystal is carried out to reduce the roughness, so as to reduce the inheritance of defects, and the generation of new defects in the crystal growth process. In addition, when growing SiC crystals, it is crucial to accurately control the growth temperature, pressure, raw material gas flow, and other parameters, through the combination of thermal field simulation and experiment, optimize the process parameters or equipment structure optimization, and inhibit the production of defects.

Furthermore, no-killer defects in SiC epitaxy, although they do not lead to complete device failure, may cause problems in the application. Therefore, the long-term reliability and stability of SiC devices in extreme environments such as high temperatures, high voltage, and high current still need to be tested for a long time and in multiple scenarios. Future efforts include improving the SiC substrate and epitaxial quality, optimizing the gate oxygen process, improving device reliability, developing high-voltage and high-current SiC devices, and developing new structures such as super junctions. With the advancement of technology and cost reduction, SiC materials have broad application prospects and are expected to play an important role in many fields.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Lingling Lai: Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Yingxin Cui:** Conceptualization (equal); Funding acquisition (equal); Resources (equal); Supervision (equal). **Yu Zhong:** Investigation (equal); Methodology (equal); Supervision (equal). **Kuan Yew Cheong:** Supervision (equal); Visualization (equal); Writing – review & editing (equal). **Handoko Linewih:** Investigation (equal); Methodology (equal); Supervision (equal). **Xiangang Xu:** Funding acquisition (equal); Resources (equal); Supervision (equal). **Jisheng Han:** Funding acquisition (equal); Resources (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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