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PHYSICS OF SEMICONDUCTOR DEVICES

I–V Characteristics of High-Voltage 4*H*–SiC Diodes with a 1.1-eV Schottky Barrier

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Abstract—The *I–V* characteristics of high-voltage 4*H*–SiC diodes with a Schottky barrier ~1.1 eV in height are measured and analyzed. The forward *I–V* characteristics proved to be close to "ideal" in the temperature range of 295–470 K. The reverse *I–V* characteristics are adequately described by the model of thermionic emission at the voltages to 2 kV in the temperature range of 361–470 K if, additionally, a barrier lowering with an increase in the band bending in the semiconductor is taken into account.

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1. INTRODUCTION

The classical diode theory (the theory of thermionic emission) predicts for the Schottky diodes (SDs) the following dependence of the current I on the voltage V [1]:

$$I = SA^*T^2\exp\left(-\frac{\Phi_{B0}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right], \quad (1)$$

where q is the elementary charge, A^* is the Richardson constant, S is the Schottky-contact area, Φ_{B0} is the barrier height (in the classical theory, it is considered constant), V is the applied voltage (positive for the forward direction and negative for the reverse direction), T is the absolute temperature, and k is the Boltzmann constant. The *I–V* characteristics of real Schottky diodes usually differ from the *I–V* characteristics of the idealized diodes. In the forward direction, these differences, as a rule, are not so significant; thus, the forward *I–V* characteristics $I_f(V_f)$ can be described by the empirical formula

$$I_f = I_0\left[\exp\left(\frac{qV_f}{nkT}\right) - 1\right], \quad (2)$$

which differs from expression (1) in that it involves empirical quantities—the "saturation" current I_0 and the ideality coefficient n. From the value of the coefficient n, it is used to estimate the Schottky-diode quality. It is considered that the ideality coefficient should be less than 1.1 for good SDs.

Classical formula (1) predicts that the reverse current in the Schottky diodes should be saturated at voltages amounting to several units of kT/q at the level of

$$I_0 = SA^*T^2\exp\left(-\frac{\Phi_{B0}}{kT}\right). \quad (3)$$

However, it never happens in practice, while gradual and substantial increase in the current always takes place with the reverse bias. The leakages can be caused by defects in semiconductors, the nonuniformities in the barrier-height distributions over the contact area, the design features of diodes resulting in the premature boundary breakdown, etc. Even in homogeneous contacts with a perfect structure, the reverse current can increase due to several physical causes: (i) due to the dependence of the barrier height on the bias voltage, (ii) due to the electron field and thermal–field emissions from metal to semiconductor, (iii) due to the thermal generation of electron–hole pairs in the space-charge region (SCR), etc.

Previously, we fabricated high-voltage 4*H*–SiC diodes with a Schottky barrier of 1.5 eV in height [2]. In the temperature range of 298–522 K, the forward *I–V* characteristics of these diodes are adequately described by formula (2) with an ideality coefficient close to unity. However, in the reverse direction, the current proved to be excessive with respect to overbarrier emission. In [2] we proposed a model of flow of the excess reverse current due to the local electron injection of from metal to semiconductor at the dislocation-emergence spots to the semiconductor surface. It is possible to expect that the thermionic-emission current in the 4*H*–SiC Schottky diodes for reasonably low barriers and elevated temperatures exceeds the current caused by defects. In this study we present the results of investigations of high-voltage 4*H*–SiC diodes with an ~1.1-eV Schottky barrier. It is shown that the *I–V* characteristics, both in the forward and reverse (to 2 kV), directions are well described in the thermionic-emission model if in addition to take into account a barrier-height lowering with an increase in the band bending in the semiconductor.

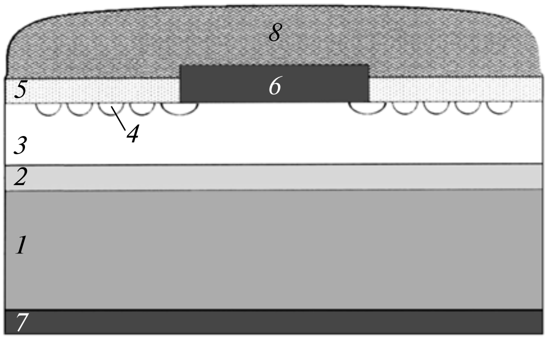

Fig. 1. Schematic image of the cross section of the 4*H*–SiC Schottky diode: (*1*) the *n*-type substrate (the resistivity is 0.02 Ω cm, the thickness is 370 μm), (*2*) the buffer epitaxial *n*-type layer (the donor concentration is 1×10^{18} cm^{-3}, the thickness is 8 μm), (*3*) the base epitaxial *n*-type layer (the donor concentration is 9×10^{14} cm^{-3}, the thickness is 34 μm), (*4*) the protective *p*-type rings, (*5*) the passivating oxide, (*6*) the Schottky metal contact (anode), (*7*) the metal ohmic contact (cathode), and (*8*) the hermetic (silicone gel).

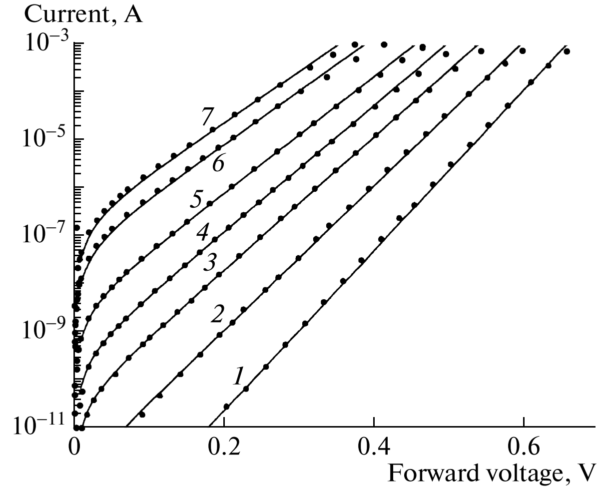

Fig. 2. Forward *I*–*V* characteristics of the 4*H*–SiC Schottky diodes. The points are experimental, and the solid lines are the approximations by formula (2). The temperature T = (*1*) 295, (*2*) 334, (*3*) 361, (*4*) 380, (*5*) 411, (*6*) 449, and (*7*) 470 K.

2. EXPERIMENTAL

The diodes were fabricated on the basis of a commercial epitaxial material (Cree Inc.): the donor concentration in the base *n*-type layer is $N = 9 \times 10^{14}$ cm^{-3}, and the *n*-type layer thickness is d = 34 μm. A schematic image of the diode-chip cross section is shown in Fig. 1. On the surface of the basic epitaxial *n*-type layer, a deposited-nickel Schottky contact of 1.2 × 1.2 mm in size was formed. On top of nickel, we deposited an aluminum layer. On the rear side of the structure, an ohmic contact from deposited and thermally fired-in nickel layer was formed. On top of the contact metal, a silver layer was deposited. For suppressing the premature edge breakdown in the SD structure, we used the protective system of floating *p*-type rings formed by nonequilibrium boron diffusion from the implanted source. The surface of the basic epitaxial *n* layer is passivated by thermal oxide SiO_2. The chip is filled with silicone gel.

For measuring the *I*–*V* characteristics, we used a special small table supplied with a clamping needle and the system of the quartz-lamp heating to the temperature of 500 K (the accuracy of maintaining temperature is ±2 K). The measurements were carried out at low residual pressure. The forward *I*–*V* characteristics were measured in the range of currents of 10^{-11}–10^{-3} A and the reverse ones in the range of 10^{-11}–10^{-4} A. For the measurements, we selected several diode chips, which had a leakage no larger than 10 nA at a voltage of 1000 V at room temperature.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1. Forward I–V Characteristics

In Fig. 2 the points show the typical forward *I*–*V* characteristics measured at different temperatures in the range of 295–470 K for fabricated 4*H*–SiC Schottky diodes. At the portion preceding the current restriction by a series resistance of the diode blocking base, the measured *I*–*V* characteristics were approximated by Eq. (2) (in this case I_0 and n were the fitting parameters). At all temperatures the ideality parameter differed only slightly from unity: $n \approx 1.02$. In Fig. 3 the points show the dependence of $\ln(I_0/T^2)$ on $1/(nkT)$ (the Richardson plot) from the slope of which

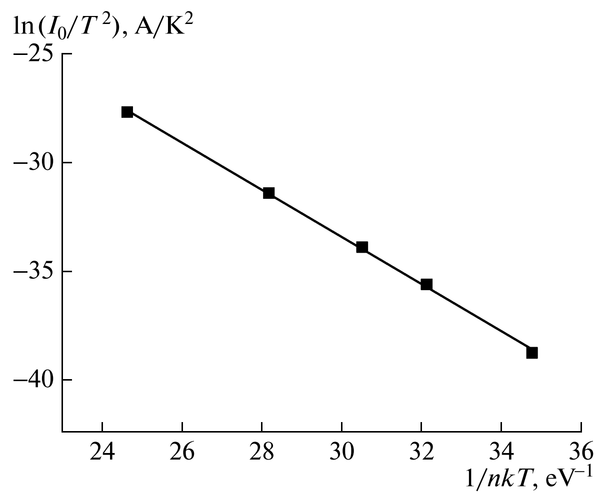

Fig. 3. Richardson plot.

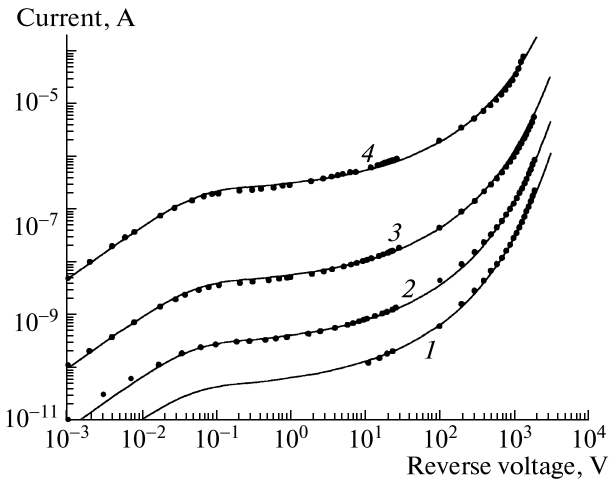

Fig. 4. Reverse *I*–*V* characteristics of the 4*H*–SiC Schottky diodes. The points are experimental, and the solid lines are the approximation by formula (9). The temperature T = (*1*) 361, (*2*) 380, (*3*) 411, and (*4*) 470 K.

it is possible to determine the effective barrier height: $\Phi_{B\,eff} = 1.12$ eV. Thus, the forward *I*–*V* characteristics in the entire temperature range proved to be reasonably close to the ideal ones.

3.2 Reverse I–V Characteristics

In Fig. 4 the points show the typical reverse *I*–*V* characteristics $I_r(V_r)$ measured in the fabricated diodes at the voltages to 2 kV in the temperature range of 361–470 K. It should be noted that the appreciable reverse current appeared at the voltage $V_r = 3kT/q$ and the temperature $T \approx 380$ K. In the double logarithmic scale, the measured *I*–*V* characteristics have the form of "softly" increasing dependences of the current on the voltage: with increasing voltage from 0.1 to 1000 V, the reverse current increases at least by three orders of magnitude. Thus, the reverse *I*–*V* characteristics, in contrast to the forward ones, very strongly differ from the "ideal," which is the subject of the following discussion.

As was mentioned above, the possible mechanisms responsible for the observed increase in the reverse current are nonuniform barrier-height distribution over the contact areas [3], the tunneling, the thermal generation of carriers in the SCR, and the barrier-height dependence on the bias voltage.

The proximity of the ideality coefficient n to unity indicates that the barrier-height distribution over the area is most likely very uniform. Therefore, this factor can be excluded at once.

3.2.1.Tunneling. With increasing reverse voltage, the energy barrier narrows so that the probability of electron-tunnel transmission from metal to semiconductor increases. In the Padovani–Stratton tunnel-transmission theory [4], the parameter qE_{00} with the dimension of energy and representing the barrier height at which the tunnel-transmission probability is e^{-1} was introduced. The potential E_{00} depends on the effective electron mass m^* in semiconductor and the donor concentration N:

$$E_{00} = \frac{h}{4\pi}\sqrt{\frac{N}{m^*\varepsilon_s}}. \quad (4)$$

Here, h is the Planck constant and ε_s is the semiconductor's permittivity. In the roughest approximation, it is possible to assume that the thermionic emission dominates over tunneling if the thermal energy $kT \gg qE_{00}$. In the case of n-4*H*–SiC with the donor concentration $N = 9 \times 10^{14}$ cm^{-3}, calculation by formula (4) yields $qE_{00} = 0.33$ meV. Even at $T = 300$ K, the thermal energy $kT = 26$ meV, which is 80 times higher than qE_{00}. From this it is possible to draw the conclusion that the tunneling should play no substantial role in the case considered by us.

3.2.2. Thermal generation of carriers. With increasing reverse voltage, the SCR in semiconductor extends so that the generation component of the reverse current can increase (the same as in diodes with *p*–*n* junction):

$$I_g = \frac{qn_iW}{2\tau}S, \quad (5)$$

where n_i is the concentration of intrinsic carriers in semiconductor, τ is the effective lifetime of carriers in the SCR, and W is the SCR width. In *p*–*n* diodes based on such a wide-gap semiconductor as 4*H*–SiC, the appreciable generation current usually appears only at temperatures above 700 K [5] (indeed, at $T = 700$ K, the intrinsic-carrier concentration $n_i \sim 10^7$ cm^{-3}; assuming that $\tau \sim 10^{-8}$ s, $W = 34$ μm, and $S = 10^{-2}$ cm^2, we obtain $I_g \sim 1$ nA). From here it is possible to draw a conclusion that the thermal generation of carriers also should play no substantial role in the case considered by us.

3.2.3. Field dependence of barrier height. In the classical diode theory, the barrier height is considered constant; however, there are at least two causes of the barrier-height lowering with increasing reverse voltage. The first cause is the effect of image forces on the shape and height of the potential barrier (the Schottky effect [1]). The second cause is the presence of a thin intermediate insulator layer between metal and semiconductor, across which there is a low voltage drop decreasing the barrier height [6].

(i) The barrier lowering caused by the Schottky effect amounts to

$$\Delta\Phi_1/q = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}}, \quad (6)$$

where E_m is the electric-field strength on the semiconductor surface. It is necessary to note at once that the electric field E_m in the 4H–SiC-based SD can be as high as ~10^6 V/cm (an order of magnitude higher in comparison with that in silicon-based and gallium–arsenide-based diodes). For such fields the barrier-height lowering attains $\Delta\Phi_1 = 0.12$ eV. The corresponding increase in the reverse current I_r at $T = 470$ K amounts to

$$\frac{I_r}{I_0} = \exp\left(\frac{\Delta\Phi_1}{kT}\right) \approx 20. \qquad (7)$$

(ii) The barrier lowering caused by the presence of the intermediate layer amounts to

$$\Delta\Phi_2/q = \frac{\varepsilon_s\delta}{\varepsilon_\delta + q\delta D_s}E_m, \qquad (8)$$

where δ and ε_δ are the thickness and the permittivity of the intermediate layer, respectively; D_s [V^{-1} cm^{-2}] is the energy density of surface states at the Fermi level in metal. In the case of 4H–SiC, it is a thin natural oxide SiO_x on the surface that can be the intermediate layer. We set $\delta = 5$ Å and $\varepsilon_\delta = 2$; then, we obtain $\Delta\Phi_2 = 0.25$ eV at $E_m = 10^6$ V/cm in the Mott limit ($D_s \longrightarrow 0$). The corresponding increase in the reverse current at $T = 470$ K amounts to

$$\frac{I_r}{I_0} = \exp\left(\frac{\Delta\Phi_2}{kT}\right) \approx 500.$$

Thus, the total barrier-height lowering in the 4H–SiC Schottky diodes can attain 0.37 eV at high fields, which means an increase in the reverse current to 10 thousand times in comparison with the saturation current I_0.

Taking into account the field dependence of the barrier height, the approximating formula for the reverse current can be written in the following form:

$$I_r = I_0\exp\left[\frac{\Delta\Phi_B(V_r)}{kT}\right]\left[1 - \exp\left(-\frac{qV_r}{kT}\right)\right], \qquad (9)$$

where

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} + \alpha E_m, \qquad (10)$$

$$\alpha = \frac{\varepsilon_s\delta}{\varepsilon_\delta + q\delta D_s}. \qquad (11)$$

At a reverse voltage substantially exceeding the band bending in the semiconductor at the zero bias, the electric field E_m is expressed in terms of the reverse voltage V_r in the following form:

$$E_m = \sqrt{\frac{2qNV_r}{\varepsilon_s}}. \qquad (12)$$

The approximation of the experimental reverse I–V characteristics according to formula (9) requires only one fitting parameter α. The result of this approximation is shown in Fig. 4 (solid lines). As can be seen, the experimental results are very well described by formula (9) for $\alpha = 1.2 \times 10^{-7}$ cm (identical at all temperatures). If we assume that $\varepsilon_\delta = 2$ for the SiO_x layer, we obtain $D_s = 2 \times 10^{13}$ V^{-1} cm^{-2} for $\delta = 5$ Å (one monatomic layer). Such natural-oxide thicknesses and the values of density of states seem to be quite reasonable for the 4H–SiC real surface.

It is of importance to note that the presence of thin natural oxide has almost no or little effect on the ideality coefficient n. Indeed, it is shown in [6] that, at the presence of the intermediate layer, the value of n can be estimated from

$$n = 1 + \frac{\delta\varepsilon_s}{W_0(q\delta D_s + \varepsilon_\delta)}, \qquad (13)$$

where W_0 is the SCR width at the zero bias. Even in the Mott limit ($D_s \longrightarrow 0$) and a relatively thick oxide ($\delta = 20$ Å, $\varepsilon_\delta = 2$), the ideality parameter calculated by formula (13) remains close to unity: $n = 1.01$.

4. CONCLUSIONS

From the analysis carried out of the reverse I–V characteristics, it can be seen that the basic mechanism responsible for increasing reverse current in the investigated 4H–SiC diodes at high reverse voltages is most likely the barrier-height lowering caused by the presence of the intermediate layer in the form of natural oxide on the 4H–SiC surface. This implies that the manufacturing of diodes under the conditions favoring the formation of a thick intermediate layer can have a negative effect on the leakage currents (even in [7], it was shown that the reverse current of the diode with relatively thick intermediate layer can exceed the current of the diode with a thin layer due to decreasing barrier height).

REFERENCES

1. S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1969; Energiya, Moscow, 1984), vol. 1.
2. P. A. Ivanov, I. V. Grekhov, A. S. Potapov, T. P. Samsonova, N. D. Il'inskaya, O. I. Kon'kov, and O. Yu. Serebrennikova, Semiconductors **44**, 653 (2010).
3. R. T. Tung, Phys. Rev. B **45**, 13509 (1992).
4. F. A. Padovani and R. Stratton, Solid State Electron. **9**, 695 (1966).
5. P. A. Ivanov, M. E. Levinshtein, T. T. Mnatsakanov, J. W. Palmour, and A. K. Agarwal, Semiconductors **39**, 861 (2005).
6. E. H. Rhoderick and R. H. Williams, *Metal–Semiconductor Contacts* (Clarendon, Oxford, 1988; Radio i svyaz', Moscow, 1982).
7. N. S. Card and E. H. Rhoderick, Solid State Electron. **16**, 365 (1973).

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