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Fabrication and electrical characteristics of the Pt/SiNWs/*n*-Si/Al Schottky diode structure

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ABSTRACT

Array-ordered silicon nanowires (SiNWs) were fabricated directly on *n*-Si substrate by wet chemical etching. The electroless plating method was used to modify SiNWs with platinum (Pt) nanoparticles as the top electrodes, forming the novel tridimensional Pt/SiNWs/*n*-Si/Al Schottky diode structure. The structural and electrical characteristics were investigated to obtain the optimal experimental conditions for forming the Pt/SiNWs/*n*-Si/Al Schottky barrier diode structures. Three key electrical parameters (ideality factors, barrier heights and series resistance) are 11.58 eV, 0.93 eV and 1.99 kΩ, respectively. The study reveals that the Pt/SiNWs/*n*-Si/Al Schottky diode structure would have a great potential application in nanoscale optoelectronic devices by controlling the experimental parameters properly.

1. Introduction

Metal–semiconductor (MS) Schottky barrier diodes play an important role in the modern semiconductor industry due to their extensive applications in various electronic and optoelectronic devices. The traditional Schottky barrier diodes are based on planar structure. So far lots of investigations on the structure have been carried out [1–4].

Silicon nanowires are considered to the promising building block for the next generation's nanodevices due to their interesting shape-dependent and unique electrical properties [5–8]. Now, the devices based on silicon nanowire employe both the single silicon nanowire and the silicon nanowire arrays [9,10]. For example, the single silicon nanowire has been used as the building block to construct the FET sensors [11]. The silicon nanowire arrays have been employed to develop the sensors [12–14]. However, to the best of our knowledge, works related to the novel tridimensional Schottky barrier diodes based on silicon nanowire arrays are seldom reported.

In the present work, a simple, low cost wet chemical etching method was used to fabricate the large-scaled SiNWs. While, the platinum (Pt) nanoparticles were deposited by the electroless plating process to prepare Pt/SiNWs/*n*-Si/Al structure. The structural characterizations of Pt/SiNWs were examined by scanning electron microscope (SEM), X-ray diffraction (XRD) and transmission electron microscopy (TEM). The electrical characteristics were investigated by current–voltage (*I*–*V*) technique for the Pt/SiNWs/*n*-Si/Al structure formed in different experimental conditions. The diode parameters (ideality factor *n*, barrier height Φ_b, series resistance R_s) were extracted by Cheung's model [15].

2. Experiment

2.1. Silicon nanowires fabrication

Single-side polished *n*-type silicon-wafers (with (100) orientation and ~0.1–10 Ω cm resistivity) were used as the substrates for the preparation of SiNWs. Before etching, the silicon wafers were cleaned carefully via standard RCA process. Then the cleaned silicon wafers were placed into a Teflon etching container which contained a mixture of 35 mM $AgNO_3$ and 15 mM HF. The silicon wafers were etched for 60 min at room temperature under 1 atm. After etching, the samples were taken out and washed with concentrated HNO_3 to remove surface byproduct, Ag nanodendrites. Then the samples were rinsed with DI water and dried with nitrogen carefully. The in-detailed process for SiNWs fabrication can be found in our previous paper [8,16].

2.2. Pt/SiNWs Schottky contact

Prior to the electroless process, the SiNWs samples were treated by dipping into 5% aqueous hydrofluoric acid solution (HF) for 10 s to remove the surface silicon oxide layer. After HF immersion, the SiNWs surface is passivated by hydrogen to form the hydrogen (H)-terminated Si surface, which is particularly resistant to air

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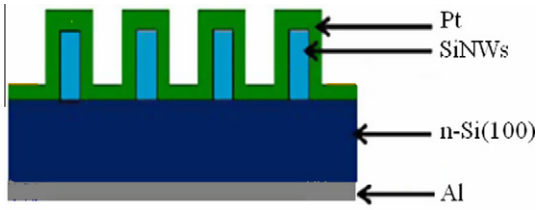

Fig. 1. Schematic of Pt/SiNWs/*n*-Si/Al structures.

oxidation. Then, the samples were immerged into K_2PtCl_6 solutions to form directly the Pt/SiNWs Schottky contact. In the experiment, the K_2PtCl_6 concentration and the deposition time varied, respectively, to investigate their influence on current–voltage characteristics of the Pt/SiNWs/*n*-Si/Al structure.

2.3. Al/n-Si ohmic contact

For current–voltage measurements, an Al layer was thermally evaporated on the backside of the *n*-Si substrate, and then annealed at 450 °C for 3 min in N_2 atmosphere to establish a large area ohmic contact. So the Pt/SiNWs/*n*-Si/Al structures were formed. The schematic of the corresponding SBD structure is shown in Fig. 1.

3. Results and discussion

3.1. Structural characteristics of Pt/SiNWs

Fig. 2 is the SEM image of the Pt/SiNWs nanocomposite structure formed in 10 mM K_2PtCl_6 solutions for 10 min electroless plating time. As can be seen from Fig. 2, the SiNWs are encapsulated by a relatively homogeneous and smooth layer. The result of the X-ray diffraction analysis further illustrates that the outside layer is Pt nanoparticles, just as shown in Fig. 3. Therefore, it implies the Pt/SiNWs structure is fabricated successfully through modifying SiNWs with platinum (Pt) nanoparticles by the electroless plating method.

3.2. The influence of the electroless plating parameters

For electroless plating method, the key parameters are the K_2PtCl_6 concentration and plating time (t). It is found that the two factors can determine the Pt layer thickness and the electrical properties of Pt/SiNWs/*n*-Si/Al structure. So the effect on current–voltage (I–V) characteristics for Pt/SiNWs/*n*-Si/Al structure was investigated. Meanwhile, the corresponding electrical parameters

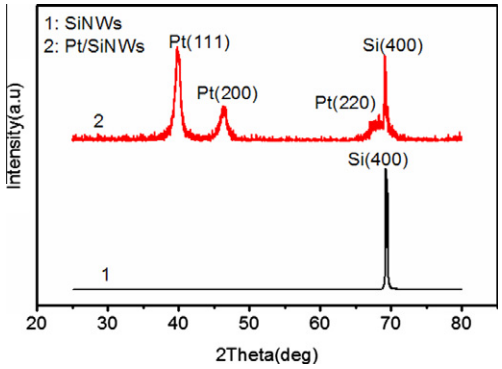

Fig. 3. X-ray diffraction (XRD) image of SiNWs and Pt/SiNWs.

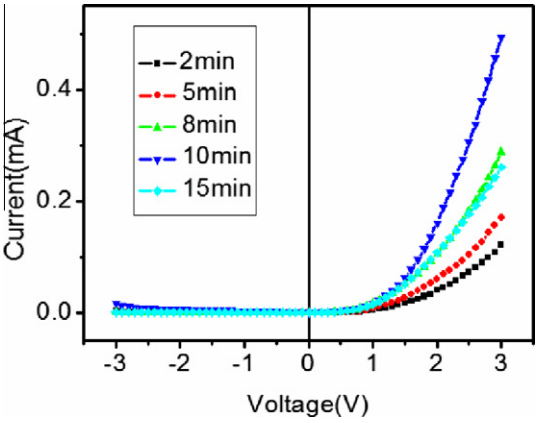

Fig. 4. Current–voltage (I–V) curves measured for Pt/SiNWs/*n*-Si/Al structures which Pt layers formed in 5 mM K_2PtCl_6 solutions for 2, 5, 8, 10 and 15 min, respectively.

Table 1
Experimental I–V characteristics parameters for Pt/SiNWs/*n*-Si/Al structures at different electroless plating time of Platinum (Pt) nanoparticles.

	2 min	5 min	8 min	10 min	15 min
R_s (kΩ)	17.91	15.47	8.24	3.80	6.95

(ideality factor n, barrier height ϕ_b and series resistance R_s) were extracted by Cheung mode to evaluate the influences. Cheung's functions [15] can be written as

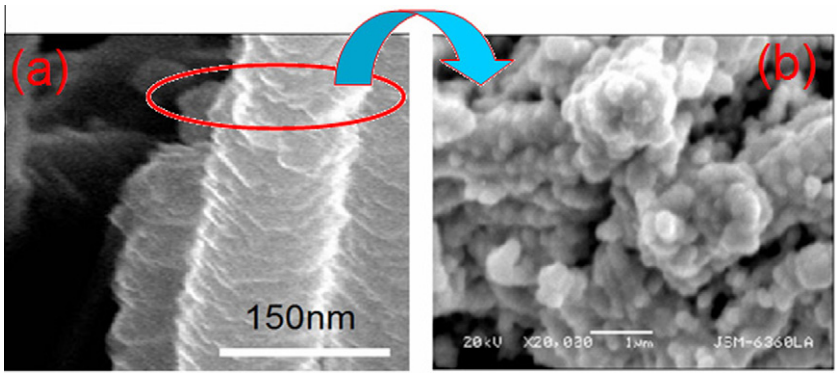

Fig. 2. Scanning electron microscope (SEM) image of (a) Pt/SiNWs nanocomposite structure formed in 10 mM K_2PtCl_6 solutions for 10 min electroless plating time and (b) partial enlarged detail.

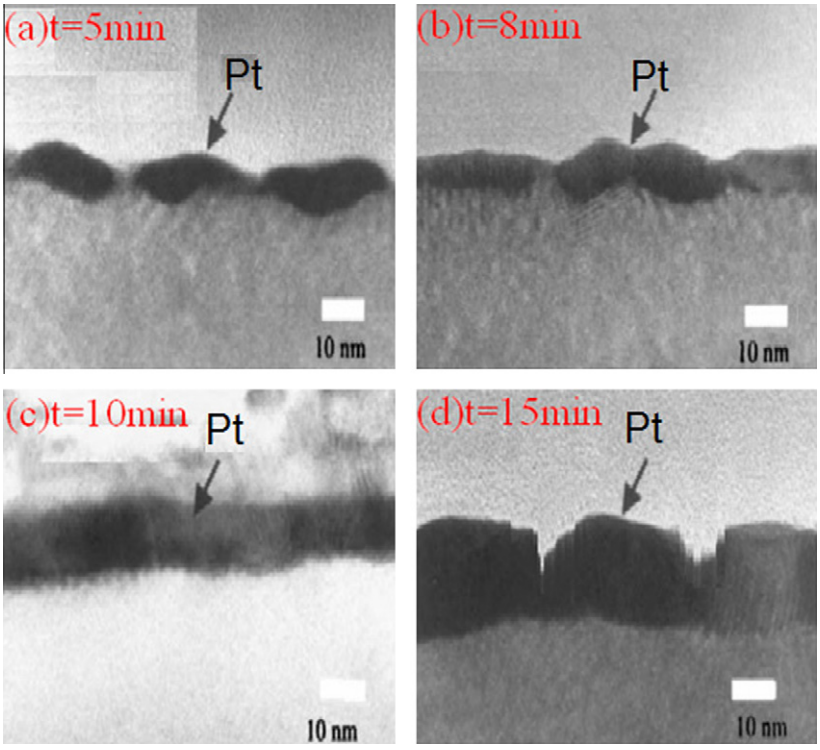

Fig. 5. Transmission electron microscopy (TEM) of Pt/SiNWs structures which Pt layers formed in 5 mM K_2PtCl_6 solutions for 5, 8, 10 and 15 min, respectively.

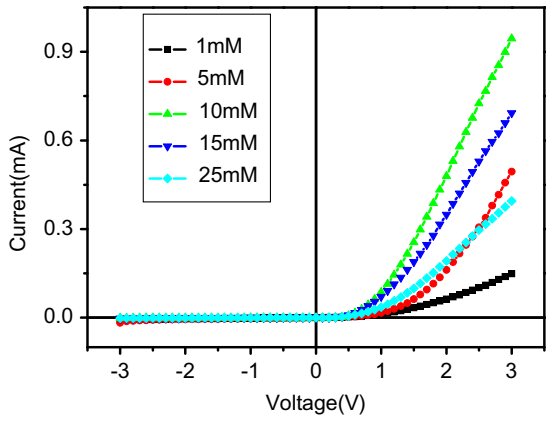

Fig. 6. Current–voltage curves measured for Pt/SiNWs/*n*-Si/Al structures at different K_2PtCl_6 concentration with 10 min plating time.

$$\frac{dV}{d(\ln I)} = IR_s + n\frac{kT}{q} \tag{1}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{2}$$

$$H(I) = IR_s + n\Phi_b \tag{3}$$

where n is ideality factor, R_s is the series resistance, Φ_b is the barrier height, A is the Schottky barrier diode area (0.01 cm^2), A^* the effective Richardson constant is equal to 112 $A/cm^2\ K^2$ for n-type Si, V is the applied voltage. For voltage larger than $3kT/q$, The Eq. (1) shows that a plot of $dV/d\ln I$ versus I should give a straight line whose slope and y-axis intercept can be used to determine the value of R_s and n, respectively. In the same way, given the obtained value of n, the values of Φ_b can then been calculated from Eq. (3) by drawing a plot of $H(I)$ versus I.

Fig. 4 shows the current variation as a function of applied bias voltage for the Pt/SiNWs/*n*-Si/Al structure which Pt layers formed in 5 mM K_2PtCl_6 solutions for 2, 5, 8, 10 and 15 min, respectively. The rectifying properties can be observed and differ from each other, as shown in Fig. 4. The corresponding series resistance (R_s) is extracted and listed in Table 1. It is found that R_s decreases with the increase of the electroless plating time (t). When t is set as 10 min, R_s reaches a minimum 3.8 kΩ. With the further increasing of t, R_s increases significantly. This behaviour can be explained that the series resistance R_s is dominated by the morphological characteristics of Pt layer on the surface of SiNWs. As shown in Fig. 5, Pt layer is not continuous when t is less than 10 min. The continuous and homogeneous Pt layer is formed on the SiNWs when t is equal to 10 min. The corresponding thickness of Pt layer is ~10 nm. With the further increasing of t, for example, when t is fixed to 15 min, the Pt layer is rupture due to film growth kinetics.

The current–voltage (I–V) characteristics were further examined for the Pt/SiNWs/*n*-Si/Al structures which Pt layers formed at different K_2PtCl_6 solutions concentrations ($C_{K_2PtCl_6}$) for 10 min plating time. Fig. 6 shows the corresponding I–V curves. The series resistance R_s is also extracted from the I–V curve by Cheung model, shown in Table 2. The series resistance R_s decreases from 14.49 to 3.8 kΩ as $C_{K_2PtCl_6}$ increases from 1 to 5 mM, then reaches a minimum, 1.99 kΩ when $C_{K_2PtCl_6}$ is fixed at 10 mM. With the further

Table 2
Experimental I–V characteristics parameters for Pt/SiNWs/*n*-Si/Al structures at different K_2PtCl_6 concentration with 10 min plating time.

	1 mM	5 mM	10 mM	15 mM	25 mM
ϕ_b (eV)	0.97	0.97	0.93	0.92	0.93
R_s (kΩ)	14.49	3.80	1.99	3.04	4.83
n	14.56	12.07	11.58	13.11	13.93

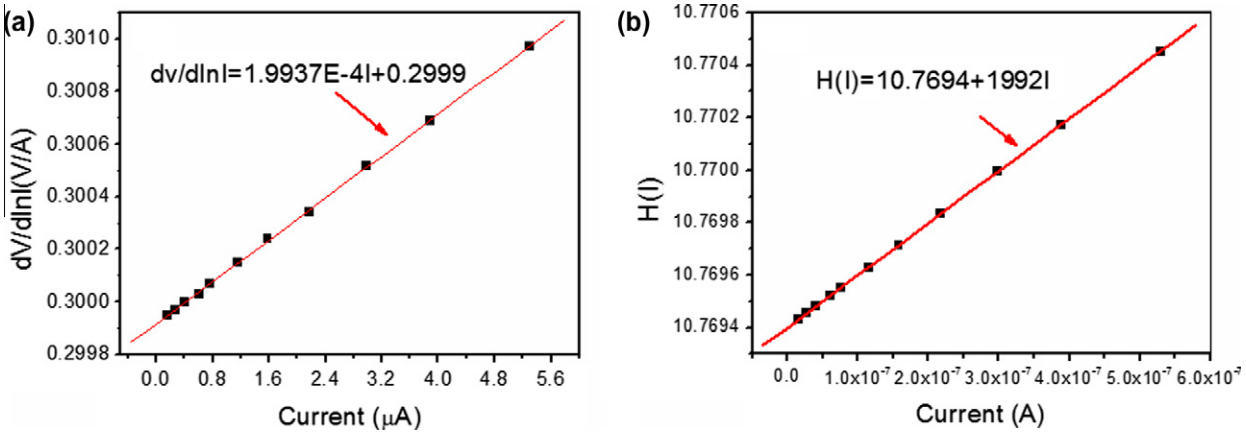

Fig. 7. Extraction procedure of three key parameters (ideality factor n, barrier height ϕ_b and series resistance R_s) by Cheung's model.

increasing of $C_{K_2PtCl_6}$, the R_s increases significantly. The behavior can also be attributed to the morphological characteristic of Pt layer. So the optimal parameters conditions for forming the Pt/SiNWs/n-Si/Al Schottky diode structures are obtained: 10 mM K_2PtCl_6 solutions and 10 min electroless plating time. Fig. 7 shows the corresponding extraction procedure. The experimental results give the ideal straight line when the applied voltage ranges from 0.08 to 0.28 V. In this case, the barrier height (Φ_b) and ideality factor (n) are 0.93 and 11.58 eV, respectively. It is obvious that the ideality factor (n) is greater than 3 for Pt/SiNWs/n-Si/Al structures. It means that the mechanism governing the current transportation through the structures cannot be described by the thermionic emission theory [17]. The underlying cause for $n > 1$ can be attributed to either the existence of an interfacial layer, the barrier inhomogeneity, or the barrier height lowering due to the image-force which is voltage dependent [1,2]. Meanwhile, the barrier height (~0.93 eV) reported here is larger than the values of ~0.9, 0.73, 0.68 and 0.83 eV for Pt/n-Si structure SBD reported in Refs. [18–21]. The possible reasons may be attributed to the introduction of SiNWs and the different methods for the formation of thin Pt layer.

For a real metal/semiconductor Schottky barrier diode, the barrier height is to a certain degree dependent on the metal work function but, due to the presence of interface states, it is partly pinned to a fixed level in the bandgap. According to the Schottky–Mott model and the Bardeen model, the metal/semiconductor barrier height is given by $\Phi_b = r(\Phi_M - \chi_S) + (1 - r)(E_g - \Phi_0)$ [22]. As is known, when the bulk silicon is etched to form the SiNWs, the smaller size induces the increment of the band gap E_g directly. So, given the metal work function Φ_M, the Schottky barrier becomes larger while the electron affinity χ_S decreases. Meanwhile, the redox reaction during the electroless plating process leads to the increment of interfacial intensity. Therefore, the barrier height also become larger due to the presence of large interfacial intensity.

4. Conclusion

The Pt/SiNWs/n-Si/Al Schottky diode structures were first fabricated through modifying SiNWs with platinum (Pt) nanoparticles by the electroless plating method. The electrical characteristics were investigated and three key electrical parameters were extracted for Pt/SiNWs/n-Si/Al Schottky diode structures formed in different experimental conditions. The results indicates that the factor determining the electrical characteristics is the microstructure of the Pt/SiNWs. The optimal parameters conditions for forming the Pt/SiNWs/n-Si/Al Schottky diode structures by electroless plating are obtained: 10 mM K_2PtCl_6 solutions and 10 min electroless plating time. The Pt film formed in the optimal experiment conditions is relatively homogeneous and smooth. The corresponding thickness of Pt is ~10 nm.

Acknowledgements

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