Vertical leakage induced current degradation and relevant traps with large lattice relaxation in AlGaN/GaN heterostructures on Si

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We present a mechanism for the vertical leakage induced current degradation with identification of the properties of the relevant traps in AlGaN/GaN heterostructures on Si. The extent of the current degradation is determined by back-gating sweep measurements in double directions at different sweep rates and temperatures. It is found that the current degradation is only observed at relatively slow sweep rates and high temperatures. Time dependent back-gating measurements further suggest that the current degradation process is related to traps with long time constants. By comparing with the measurement results of samples on sapphire substrates, we confirm that the current degradation is caused by vertical leakage in heterostructures on Si. On the basis of the vertical leakage induced current degradation mechanism and in conjunction with the long-time degradation process, we measure both the trapping and detrapping processes of the relevant trap states to identify their properties. We find that there is a 0.6 eV capture barrier and a 0.67 eV emission barrier for the trap states, indicating that the trap states are of large lattice relaxation. *Published by AIP Publishing.*
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Gallium nitride (GaN) based high electron mobility transistors (HEMTs) on Si have attracted great attention for high-power applications in recent years.[1,2] However, the performance of HEMTs is limited by reliability issues like output current degradation or threshold voltage instability.[3–5] Those problems could be due to bulk traps in the GaN buffer layer.[6,7] During off-state of HEMT devices, the vertical voltage between the drain and the substrate is high, which may cause buffer trap ionization or trapping effects and finally lead to current degradation when turning the devices to on-state. To eliminate the impact of buffer traps on device performance, the trap ionization/trapping mechanism should be clarified. Several literatures have tried to address the issue, but the results are still controversial. There are mainly two explanations of the current degradation under the vertical voltage bias condition: One assumes that the current degradation is due to acceptors' ionization in the buffer layer induced by the vertical electric field. The ionized acceptors are negatively charged and will deplete the 2DEG to cause current degradation.[8,9] The other declaims that the current degradation is caused by vertical leakage current. The excess electrons injected from the Si substrate are trapped by buffer traps and result in current degradation.[10] In this work, we present the current degradation mechanism under vertical voltage bias in AlGaN/GaN heterostructures on Si and identify the relevant trap parameters by simultaneously measuring the trapping and detrapping processes of the traps. We observe the current degradation phenomenon by back-gating measurements. By comparing with the measurement results conducted on samples on sapphire substrates, we confirm that the degradation in heterostructures on Si is indeed caused by vertical leakage. On the basis of that, we measure the trapping and detrapping processes of the traps simultaneously to identify their properties. As there are obvious energy barriers for both the trapping and detrapping processes, we assume that the traps are of large lattice relaxation.

The study was carried out on AlGaN/GaN heterostructures grown on *p*-type Si (111) substrates by metal organic chemical vapor deposition (MOCVD). The structure consists of 600 nm AlN/AlGaN transition layers, a 3.0 μm GaN buffer layer, and a 25 nm AlGaN barrier layer. More details can be found in our previous work.[11] The test structure features three Ohmic terminals with two on the front and one on the Si substrate. The front Ohmic terminals are denoted as D and S, respectively, and the substrate terminal is denoted as B.

To investigate the impact of the buffer traps on the output current under the vertical bias condition, we conduct back-gating sweep measurements at different sweep rates and temperatures. In the back-gating sweep measurements, the lateral voltage between terminal D and terminal S is fixed at 1 V and the current between them is recorded as a function of the substrate voltage. The substrate is swept in bi-directions from 0 V to −200 V (down sweep) and immediately back to 0 V (up sweep). Figure 1(a) shows the result of the back-gating sweep measurements at a slow sweep rate of 10 V/s at 300 K.

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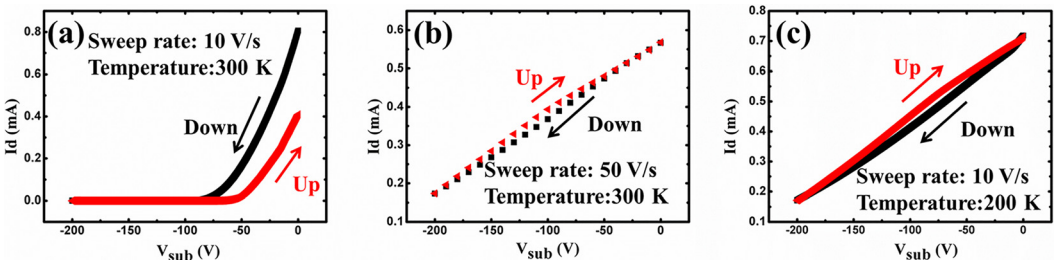

FIG. 1. Back-gating sweep measurement results at (a) 10 V/s and 300 K, (b) 50 V/s and 300 K, and (c) 10 V/s and 200 K.

The lateral current in the up sweep direction is much smaller than that in the down sweep direction indicating the current degradation. However, when the sweep rate is raised to be faster as 50 V/s at 300 K, the current degradation disappears. The lateral current in the up sweep direction is larger than that in the down sweep direction, as shown in Fig. 1(b). The current increase is due to donor ionization under the vertical electric field which leaves positive charges in the buffer layer, and hence, the 2DEG density is increased. The current degradation can only be observed at slow sweep rates, indicating that it is related to traps with long time constants. Then, we investigate the impact of temperature on current degradation by reducing the temperature to 200 K while keeping the sweep rate the same as that in Fig. 1(a) at 10 V/s. The result is shown in Fig. 1(c). There is no current degradation at such low temperature, i.e., the current degradation only happens at relatively high temperatures.

To observe the current degradation process more clearly, we conduct time dependent back-gating measurements. In the measurements, the lateral voltage is also fixed as 1 V and the substrate is constantly biased at −50 V. The time evolution of the lateral current is observed at different temperatures of 200 K, 220 K, and 300 K, respectively. Because the absolute current values differ a lot at different temperatures, if put together, the current trend at low temperatures will be blurred. Therefore, an arbitrary unit is used as shown in Fig. 2(a). At 200 K, the lateral current presents a sudden increase and then saturates, indicating that only donors are ionized. At 220 K, the current increases with time at first and then shows a decreasing trend, which means that the current degradation starts to dominate after the donor ionization. However, at 300 K, the current only shows a decreasing trend. We assume that the degradation process is faster at this temperature and covers up the signal of the donor ionization.

The real mechanisms for the current degradation under vertical bias are still controversial. The degradation could be induced by the vertical electric field or leakage current.[10] We think that the acceptor ionization mechanisms discussed in Refs. 8 and 9 may be vertical field induced although they are not clarified in the literature. As illustrated in Fig. 3, in the electric field induced model, when a positive voltage is applied between the front terminal and the substrate, the holes near the 2DEG in the GaN buffer layer are drifted towards the hole potential well at the interface between buffer and transition layers or flow away through the substrate. To achieve a new balance, the electrons in the valence band will transit to the acceptors in the buffer near the 2DEG, causing an acceptor ionization. It is an electron exchange process between the valence band and acceptor states. The ionized acceptors are negatively charged and so that will deplete the 2DEG, leading to the current degradation. In the leakage current induced model, considering the injection of electrons from the substrate (through thermal injection or along dislocations), the excess injected electrons will be captured by traps. If the trapped electrons are not released in time, they will also act as negative charges to deplete the 2DEG and cause current degradation. Different from the electric field induced model, it is an electron exchange process between the conduction band and trap states.

To discriminate the real current degradation mechanism under the vertical bias condition, we conduct similar time dependent back-gating measurements on devices fabricated on sapphire substrates. Except for the different substrates and transition layers, the growth conditions of GaN buffer and AlGaN barrier layers are the same for devices on Si and sapphire substrates. We suppose that the defect status in GaN buffer is similar for both samples from the view point of growth conditions (similar point defects) and X-ray diffraction results. [The FWHM values of the GaN (002) and (102) rocking curves are 389 and 527 arc sec for samples on Si and 297 and 558 arc sec for samples on sapphire, indicating

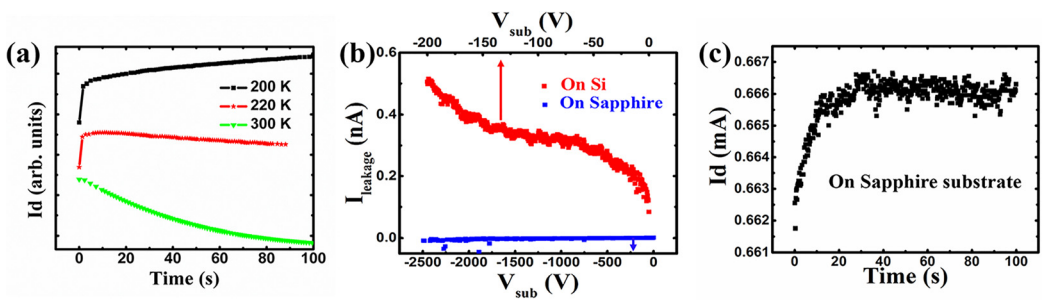

FIG. 2. (a) Time dependent back-gating measurement results in devices on Si. (b) Vertical leakage in devices on Si and on Sapphire. (c) Time dependent back-gating measurement results in devices on Sapphire.

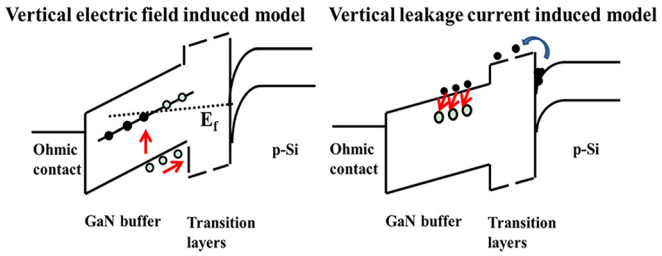

FIG. 3. Two different models for current degradation.

similar dislocation density.] Because of a very low vertical leakage current in devices on sapphire substrates compared to that on Si [as shown in Fig. 2(b)], the vertical leakage induced model is excluded. Thus, if there is still the current degradation phenomenon, the degradation should be due to the vertical electric field, while the degradation in devices on Si should be due to vertical leakage if no degradation occurs under the same field in the sapphire based devices. Considering the semi-insulating property of the sapphire substrate and its thickness (430 μm) higher than that of the GaN buffer layer (3 μm), it is possible that most of the potential drop will be across the sapphire substrate instead of the GaN buffer. Thus, the electrical field across the buffer on sapphire may be much smaller than that on Si. To solve this problem, we apply much higher voltage on the sapphire substrate to make the electric field in the GaN buffer on sapphire comparable with that on Si. Taking into account the fact that the resistivity of the semi-insulating GaN buffer can reach that of sapphire in the order of $10^{11}\,\Omega\,\mathrm{cm}$,[12] the potential drop across the GaN buffer and the sapphire substrate is determined by their thickness. In order to make the electric field in GaN buffer on sapphire in the same order as that on Si, about -2500 V voltage is applied on the sapphire substrate. However, as shown in Fig. 2(c), the current only presents an increasing trend, which indicates that there is only donor ionization but no current degradation. As such, we can deduce that the current degradation in samples on Si is caused by vertical leakage and the process is actually a process of electron trapping.

On the basis of the vertical leakage induced current degradation mechanism, the electrons transit from the high energy conduction band to the low energy trap states and release energy. Therefore, the trapping time should be very short (in the order of several ms)[13] for regular trap states. However, as shown in Fig. 2(a), the current degradation time (the trapping time) constant can be up to 100 s at 300 K. According to that result, the trap states in the buffer may be of special properties with a trapping energy barrier. As many literatures only concentrate on the detrapping process of the traps in GaN,[14,15] it is also important to monitor the trapping process to identify the traps more comprehensively.

To identify the degradation relevant traps, both the trapping and detrapping processes are examined. The measurement configuration is the same as that in time dependent back-gating measurements. The trapping process is detected by measuring the lateral current transient with the substrate bias on (-50 V), while the detrapping process is monitored by measuring the recovery transient of the lateral current immediately after removing the substrate bias. The same

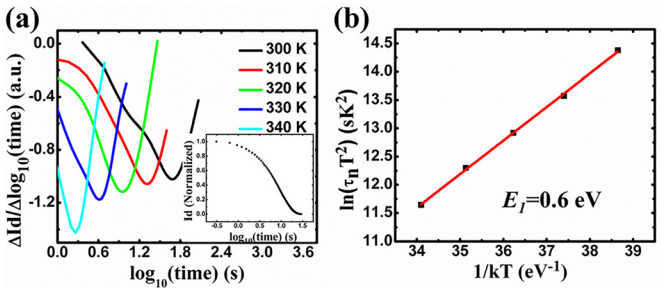

FIG. 4. (a) The trapping time-constant spectra. The inset shows lateral current's evolution with time at 300 K. (b) The Arrhenius plot.

experiments are conducted at different temperatures. The lateral current transient of the trapping process is shown in Fig. 4. First, as seen in the inset of Fig. 4(a), the lateral current decreases with time, indicating a trapping process. The current is normalized to the value obtained before applying the substrate bias. By performing a differential calculation according to the current transient spectra, Fig. 4(a) exhibits the time-constant spectra evaluated at different temperatures. Interestingly, the time constants fulfill the Arrhenius plot according to the equation[16]

$$\ln\left(\tau_n \times T^2\right) = \frac{E_1}{kT} - \ln(\sigma_n \times \gamma_n), \tag{1}$$

where τ_n indicates the trapping time constant, k is the Boltzmann constant, γ_n is a constant, σ_n is the capture cross section, and E_1 is the energy barrier for the trapping process. The calculated trapping barrier is about 0.6 eV as shown in Fig. 4(b). Besides, we simultaneously monitor the detrapping process. The results in Fig. 5 show that the detrapping energy barrier E_2 is about 0.67 eV.

The existence of the trapping and detrapping barriers can be explained by an assumption that the trapping center is with large lattice relaxation. It can be depicted by a configuration coordinate diagram[17,18] as illustrated in Fig. 6. The diagram is generally used to represent the coupling relationship between the electron transition process and the lattice vibration around the defect centers. Since the electron transition from one energy level to another is accompanied by a change in its orbit, this change alters the force between the defect center and the surrounding atoms by electrostatic interaction, thereby changing their equilibrium position. Therefore, in considering the transition process of electrons, we should also consider the change of the relative position between the defect center and the surrounding atoms. In the

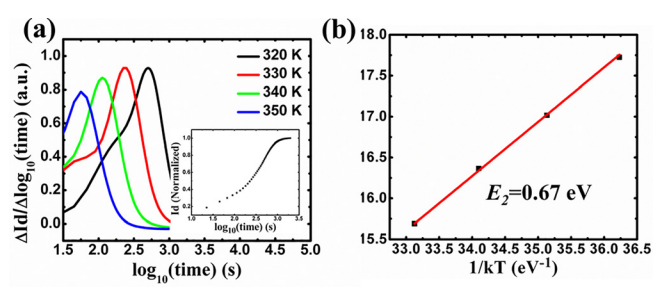

FIG. 5. (a) The detrapping time-constant spectra. The inset shows lateral current's evolution with time at 320 K. (b) The Arrhenius plot.

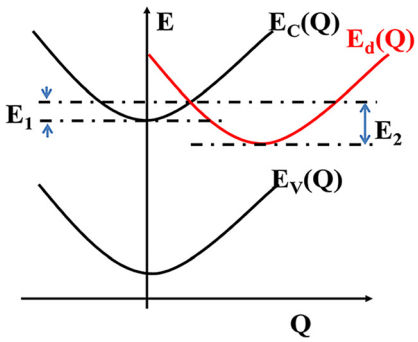

FIG. 6. Configuration coordinate diagram.

diagram, the horizontal axis represents the relative position, namely, the configurational coordinate, which is denoted by Q. The vertical axis represents the total energy of the electron-atom system, which is denoted by E, including the electron energy, atomic potential energy, and electron-atomic interaction energy. E_C (Q), E_V (Q), and E_d (Q) are the system energies corresponding to the conduction band, the valence band, and the trap state, respectively. There is a large deviation between the minimum point of the conduction band and the minimum point of the trap level in terms of the configurational coordinate Q, which is called a large lattice relaxation at the trap state. In the trapping process, electrons in the conduction band should overcome an energy barrier of E_1 to be trapped. On the contrary, electrons in the traps have to overcome an energy barrier E_2 to be released to the conduction band in the detrapping process. Thus, we can conclude that the current degradation relevant trap is a state with large lattice relaxation which has a trapping barrier of 0.6 eV and a detrapping barrier of 0.67 eV.

In summary, we report the vertical leakage induced current degradation mechanism under vertical voltage bias in AlGaN/GaN heterostructures on Si and further identify the relevant trap information. By performing back-gating sweep and time dependent back-gating measurements, we find that the current degradation is with long time constants at room temperature. By comparing with the measurement results on devices on sapphire substrates, we conclude that the current degradation in devices on Si is caused by vertical leakage current. On the basis of that, we measure the trapping and detrapping processes of the relevant traps, respectively. The traps have a trapping barrier of 0.6 eV and a detrapping barrier of 0.67 eV. Analyzed by the configuration coordinate diagram, the trap states are suggested to be with large lattice relaxation.

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