

The Principles and Applications of Electrical Characterization Techniques for Electrically Active Defects in 4H-SiC Devices

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Silicon carbide (SiC) has become one of the most promising materials in the field of power semiconductors in the last 20 years. Among the SiC polytypes, 4H-SiC is considered the suitable polytype for power electronic applications due to its large bandgap, high thermal conductivity, and high electron-saturated drift velocity. Currently, the electrically active defects in the 4H-SiC epitaxial layer and at the interface of 4H-SiC/SiO₂ are still the primary impediments to SiC-based power electronics from reaching their true potential limit. These defects are responsible for the degradation of device performance over time. Therefore, analysis of these defects is critical for the control and development of SiC devices. In this review, the point defects in the 4H-SiC epitaxial layer and 4H-SiC/SiO₂ interface states are emphasized, and the important electrical characterization techniques for these electrically active defects are compared. The key summary of electrical characterization techniques helps to better understand electrically active defects in SiC materials, providing a precise basis for further research and material applications.

1. Introduction

Silicon carbide (SiC)-based solid state-devices are being used in a wide range of applications, including electric vehicles, aerospace, and power conversion.^[1–6] If compared with silicon (Si) or gallium arsenide (GaAs), SiC exhibits a larger bandgap, a higher breakdown field strength, a faster electron saturation drift velocity, and excellent thermal conductivity. Intrinsically, SiC material comes with different polytypes, such as 3C-SiC, 4H-SiC, 6H-SiC,

and so on. Of these, 4H-SiC is considered the most suitable polytype for power electronic applications due to its wider bandgap, higher bulk mobility, and smaller anisotropy.^[7–10]

One limitation of adopting 4H-SiC as the material for power devices is the electrically active defects in the bulk crystal, in the epitaxial layer, and at the interface between the epitaxial layer and gate oxide layer. These defects are generated during crystal growth and device fabrication, especially under harsh conditions.^[11] The usual thermal oxidation method produces a high density of interface states (D_{it}) at 4H-SiC/SiO₂ with a complex energy distribution.^[12,13] Typically, the density of the 4H-SiC/SiO₂ interface states (this value is about $\approx 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in the middle of the bandgap and $\approx 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ or even higher at the edge of bandgap) is two or


three orders of magnitude higher than that of the Si/SiO₂ system ($< 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$).^[14–18] The decrease in channel mobility, instability of threshold voltage, and rise in leakage current are the negative effects of these electrically active defects.^[14,19–21] Thus, the performance of the commercially available SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) is still far below the theoretical limit.

Electrically active defects in SiC materials need to be further minimized to improve the performance and reliability of SiC-based devices. Therefore, reliable techniques to identify defects in SiC materials, particularly the behavior of the defects in harsh operating environments for commercialization purposes, are essential. Although there are many academic researchers devoted to the characterization of defects in SiC, the electrical properties of point defects and interface states are still not fully understood.^[14,22–36] This is due to the complexity of these defects, which makes it difficult to directly observe and analyze them with conventional characterization techniques. Currently, most of the existing literature focuses on the types and formation mechanisms of epitaxial layer point defects or interface defects, respectively.^[14,35–37] The review that combines these two types of defects and studies their limitations in practical applications is still lacking. So, a comprehensive overview of point defects in the 4H-SiC epitaxial layer and interface states of 4H-SiC/SiO₂ based on existing studies is presented in this review. Furthermore, it elaborates on extensive consideration of the

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characterization methods under different application conditions. By comparing traditional characterization methods with emerging techniques, the review reveals the potential of electrical characterization in understanding and predicting the performance and reliability of SiC devices.^[24,34,38–44]

2. Electrically Active Defects in 4H-SiC Devices

2.1. Point Defects in SiC Epitaxial Layer

There are extensive defects present in the 4H-SiC epitaxial layer, including triangle defects, pits, carrot defects, stacking faults, micropipe defects, surface steps, and so on.^[36,45,46] These extended defects reduce the production yield of devices, affect device reliability, and impede the application of 4H-SiC devices.^[47] Large extended defects have been greatly ameliorated during crystal growth over the last decade.^[48] Still, the production of SiC wafers with very low defect density remains a challenge.

Besides a variety of extended defects in the SiC epitaxial layer, point defects are important types of defects that originated from deep energy levels in the bandgap.^[30,49] They are generally generated during the production of SiC material. SiC point defects consist of silicon and carbon vacancies (V_{Si} and V_C), silicon and carbon interstitials (Si_i and C_i), and silicon and carbon antisites (C_{Si} and Si_C) as well as the combinations of these, such as the divacancy ($V_{Si}V_C$) and the carbon antisite–vacancy pair ($C_{Si}V_C$).^[42,50–54] Figure 1 shows the energy levels of various point defects in 4H-SiC obtained by theoretical calculations.^[55–57] On the one hand, point defects in 4H-SiC can act as carrier traps.^[58] On the other hand, there exist site effects from the inequivalent site in 4H-SiC unit cell on the ionization energy of doping impurities.^[59] Thus, point defects within the 4H-SiC can significantly affect the electrical conductivity.^[58,60] The presence of varying degrees of point defects in 4H-SiC results in the reduction of breakdown voltages, an increment of junction leakage currents, and a decrease of minority carrier lifetime.^[61–65]

Figure 2 illustrates the energy levels of major deep-level defects detected in n- and p-type 4H-SiC epilayers. Studies using deep-level transient spectroscopy (DLTS) indicate that although $Z_{1/2}$ and $EH_{6/7}$ centers have distinguished charge states, they originate from the same defect centers.^[66] $Z_{1/2}$ center is

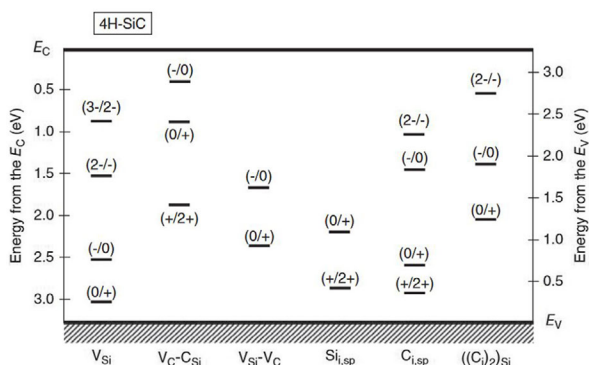


Figure 1. The theoretical energy positions of different intrinsic defects that are expected in 4H-SiC. Reproduced with permission.^[123] Copyright 2014, Wiley.

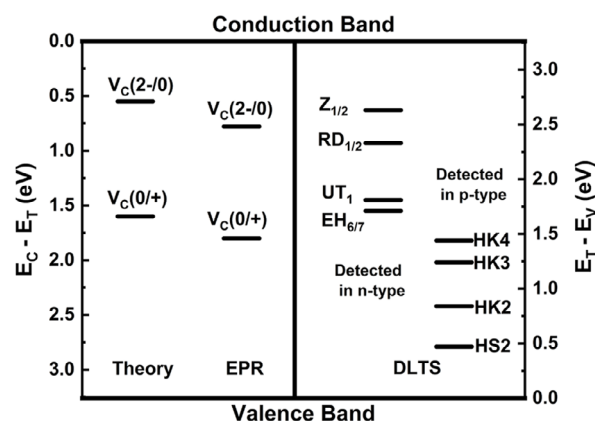


Figure 2. A comparison of energy levels of major deep-level defects in 4H-SiC epilayers measured by DLTS and theoretical calculations. Adapted with permission.^[67,74,123,186] Copyright 2014, Wiley.

identified as the acceptor level of the V_C , and the $EH_{6/7}$ center is the donor level of the V_C .^[67] The Z_1 centers and Z_2 centers are derived from the h -sites and k -sites of V_C , respectively.^[68,69] Among these levels, the deep-level defects $Z_{1/2}$ ($E_c = -0.65$ eV) and $EH_{6/7}$ ($E_c = -1.65$ eV) centers are the two common high-concentration and thermally stable defects observed within n-type 4H-SiC epilayers.^[70] A high concentration of these deep-level defects is always introduced by ion implantation,^[71] dry etching,^[72] and low-energy electron irradiation.^[73] HK_2 ($E_v + 0.84$ eV), HK_3 ($E_v + 1.24$ eV), and HK_4 ($E_v + 1.44$ eV) centers detected in p-type 4H-SiC almost disappear after annealing at 1450–1550 °C,^[74] while $Z_{1/2}$ centers and $EH_{6/7}$ centers are stable even at high-temperature annealing condition. Previous studies showed that $Z_{1/2}$ center is an important type of defect because it is a minority carrier-lifetime killer when its concentration exceeds 10^{13} cm^{-3} .^[64,65] By increasing C/Si ratio and appropriately decreasing the temperature during the epitaxial growth, densities of $Z_{1/2}$ and $EH_{6/7}$ centers can be reduced.^[64,75] Another method to eliminate $Z_{1/2}$ and $EH_{6/7}$ centers is by thermal oxidation of SiC under optimum conditions.^[76]

The characterization of defects in SiC epilayers is a crucial step in the development of SiC devices. The nature of several point defects in SiC must be thoroughly investigated because they can impact the performance and reliability of devices. Deep levels of point defects or impurities are generally tracked by DLTS. Experimental results show that DLTS can detect most of the deep-level defects in both n- and p-type SiC epilayers, as shown in Figure 2. Moreover, DLTS can also detect the interface states of SiC/SiO₂ which will be elaborated in the next section.

2.2. 4H-SiC/SiO₂ Interface States

In contrast to bulk traps, which possess discrete energy levels, the interface states of 4H-SiC/SiO₂ are continuously distributed across the energy bandgap.^[14] It is generally believed that the donor-like interface states occupy the lower half of the SiC bandgap and the acceptor-like interface states are located in the upper half.^[77] The high density of interface states at the SiC/SiO₂ interface significantly affects the channel mobility,

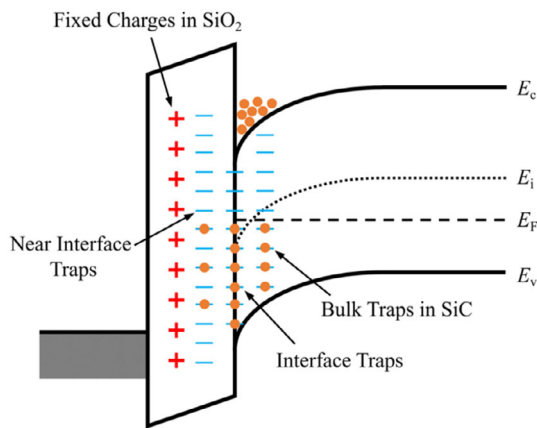


Figure 3. Sketch of 4H-SiC/SiO₂ interface states locations. Reproduced with permission.^[187] Copyright 2023, Springer Nature.

threshold voltage, and reliability of SiC MOS devices, primarily due to charge trapping and Coulomb scattering.^[78–80] For the improvement of device performance, particularly MOSbased devices, it is necessary to accurately identify the properties of interface traps (ITs) and reduce the impact of Coulomb scattering on the charged IT.

Defects at the SiC/SiO₂ interface can be classified based on physical location, properties, and energy levels.^[14,44] **Figure 3** illustrates the various types of electrically active defects and their corresponding locations within the SiC MOS structure and energy band diagram. Based on the location distribution of defects, interface states of the 4H-SiC/SiO₂ MOS system are categorized into two types: ITs at the interface region of 4H-SiC/SiO₂ and near-ITs (NITs), located inside the SiO₂ layer, a few nm away from the SiO₂/SiC interface.^[81–83]

2.2.1. ITs

Despite extensive experimental and theoretical research over the past decades, all the root causes and formation of ITs at SiC/SiO₂ remain unclear. Since the structural properties of the SiC/SiO₂ interface are very similar to those of the Si/SiO₂ interface, it is speculated that the dangling bond caused by lattice mismatch is also indicated to be the main origin of the ITs of SiC/SiO₂. However, some experimental results show that dangling bond plays a minor role in the traps at the 4H-SiC/SiO₂ interface if compared with the Si/SiO₂ interface.^[14,84,85] Early studies have shown that electrically active defects consisting of *sp*²-bonded or graphitic carbon clusters in SiO₂ are proposed to dominate SiC devices due to the existence of high concentrations of excess carbon.^[86–88] Still, some subsequent studies have questioned the existence of carbon clusters, suggesting that excess carbon at the SiC/SiO₂ interface may be in the form of carbon-related defects, such as threefold-coordinated carbon atoms and carbon di-interstitial defects.^[89–92] Besides this, the *V*_C and *V*_{Si} on the SiC surface, oxygen vacancies in the oxide, and high strain in the interfacial atomic layer at the interface have also been reported to be the cause of the ITs in the 4H-SiC/SiO₂.^[34,90] Taking into account the results of previous studies, a more widely

recognized view is that most ITs are related to dangling bonds and carbon-related traps.

ITs can capture carriers within the bandgap and release them from the bandgap via thermal emission and electric field. The density of SiC/SiO₂ ITs is strongly dependent on the crystal face of SiC.^[93] Most studies investigated 4H-SiC/SiO₂ structures with different IT densities for different crystal faces of 4H-SiC.^[14,24,34,93] Among the results, the 4° off-axis cut (0001) silicon face is commonly used for the manufacturing of high-voltage devices. Moreover, one effective method to reduce these traps is by direct nitridation or by post-oxidation annealing in N₂O or NO at high temperatures that can reduce the density of interface states near the conduction band of SiC MOS to 10¹¹–10¹² cm^{−2} eV^{−1}.^[18,34,94,95]

2.2.2. NITs

The origins of NITs remain controversial in the literature. Using photon-stimulated electron tunneling, Afanas'ev et al. discovered the high density of NITs in the oxide layer, suggesting that it could be from oxygen vacancies generated during the SiC oxidation, which resulted in a significant decrease in channel mobility.^[14,96,97] Later, through systematic studies, Knaup et al. found that silicon interstitial and carbon dimers were responsible for the origin of NITs as they caused an increase of NITs gap levels in the experimentally inferred energy range.^[37] However, Pippel et al. indicated that NITs near the 4H-SiC conduction band are independent of the carbon structure in the SiO₂/SiC interlayer.^[12] The NITs contribute to the high concentration of neutral defects closer to the SiC conduction band.^[96]

NITs are able to electrically communicate with the electrons located at or very near the SiC conduction band via direct tunneling.^[98,99] However, the electron de-trapping response time from the NITs is widely distributed due to the different tunneling distances between the NITs and SiO₂/4H-SiC interface.^[100] Thus, NITs can be distinguished from the acceptor states near the conduction band of SiC by using specific techniques.^[96,101,102]

In order to minimize the negative effect of these defects on device performance and reliability, the density of deep-level defects and interface defects can be reduced by optimizing processes. Suitable treatment methods can be used to reduce the formation of interface states and deep-level defects. Furthermore, the influence of defects on device performance can be decreased by optimizing device structure, and thus the performance and reliability of the device can be improved. Hence, understanding the origin and impact of these different types of defects, proper defect characterization techniques are crucial.

3. Electrical Characterization

A comprehensive understanding of the properties of defects in SiC can be gained by fully exploiting its electrical characteristics. However, each electrical characterization technique has its inherent limitations that must be recognized to ensure the accuracy of data and the reliability of interpretations. For example, the deep-level trap concentration of SiC epilayer is closely related to the charge carrier lifetime, which can be precisely characterized

by DLTS, despite its potential insensitivity to shallow-level defects. Thus, the subsequent sections of this article will delve into the principles, advantages, limitations, and practical applications of each electrical characterization technique in SiC's study. Especially, the limitations of current technologies, including measurement scope, sensitivity, and applicable conditions, are clarified and can stimulate new research ideas to promote technological advancement. The combination of different methods to interpret SiC defects deepens the understanding of material defect characteristics that are vital for optimizing device performance.

3.1. DLTS

DLTS is a fast, sensitive, and powerful defect spectroscopy technique developed by Lang.^[103] It is used to characterize impurities and point defects with concentrations 10^4 times lower than the background doping concentrations. A simplified illustration of the experimental setup for DLTS measurement is shown in **Figure 4a**. The principle of DLTS is based on the measurements of capacitance, current, charge, or conductance transient of a device as a pulsed reverse bias voltage is applied. The transient thermal sweeping signals are measured and processed using boxcar or lock-in techniques to determine the defect densities, energy level, and capture cross sections of the deep-level traps.^[103]

Figure 4b shows the variation of the energy band diagram under the filling pulse and after the filling pulse voltages. When the bias voltage across the device is altered, the width of the space charge region will change accordingly. It causes the variation of free charges on both sides of the junction and further affects the transient capacitance. The transient capacitance $C(t)$ is written as follows:

$$C(t) = C_0 \left[1 - \left(\frac{N_T}{2N_D} \right) \exp\left(-\frac{t}{\tau_e}\right) \right] \quad (1)$$

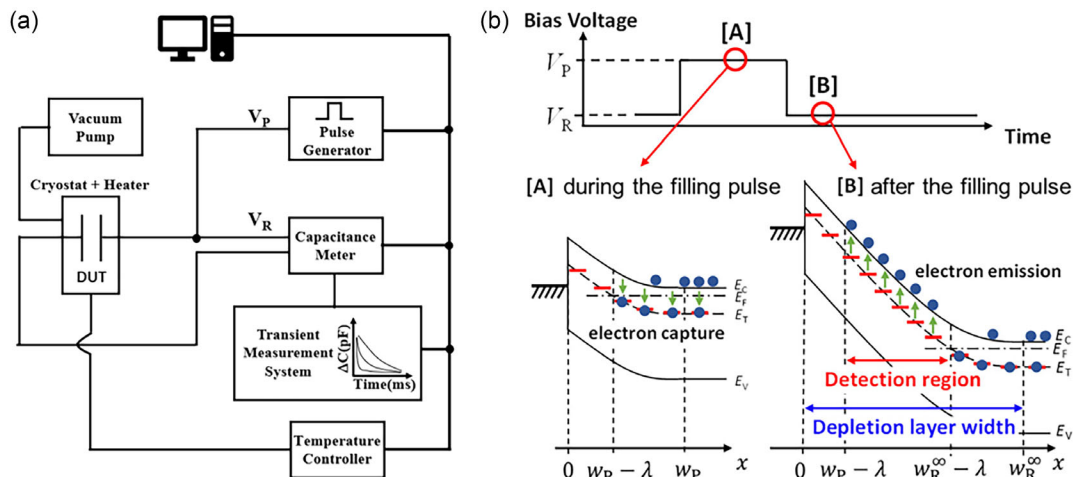


Figure 4. a) A simplified diagram of the experimental setup for DLTS measurement. b) Typical bias voltage sequence that is applied during DLTS measurements of an n-type semiconductor along with the energy band diagrams [A] under the filling pulse, and [B] after the filling pulse. w_P is the depletion layer widths at the filling pulse voltages and w_R^∞ is the depletion layer widths after the filling pulse voltages, and λ is the lambda length. Reproduced under the terms of the CC BY 4.0 license.^[13] Copyright 2024, Haruki Fujii. Published by IOP Publishing.

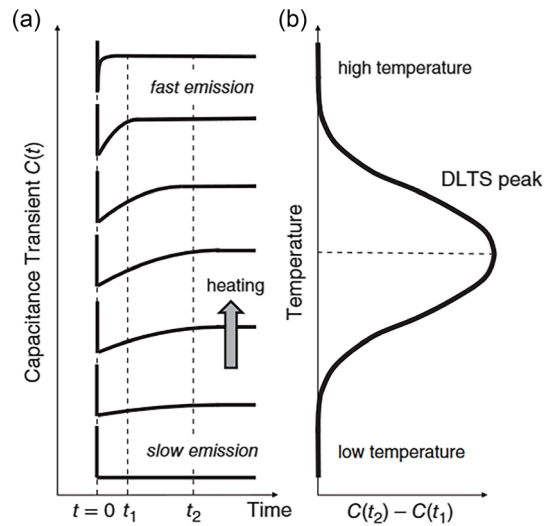


Figure 5. a) The capacitance transient changes as the temperature increases. b) The output signal is the difference between the capacitance at sampling times t_1 and t_2 . Reproduced with permission.^[123] Copyright 2014, Wiley.

where C_0 is the capacitance at reverse bias, N_T is the density of traps occupied by electrons, N_D is the donor concentration, and τ_e is the time constant with temperature dependence.

The peak in trap spectroscopy of DLTS is usually achieved by adjusting the device temperature as the position of the Fermi level changes. As presented in **Figure 5a**, the transient capacitance changes along with the temperature rise or fall at a constant rate. The DLTS signal is the difference between the capacitance at two time points t_1 and t_2 in the process of the deep-level trap-emitting charge carriers in Figure 5b. The signal is weak at extremely low temperatures because almost no electrons are released. Since most captured electrons have been emitted at

time t_1 , the DLTS signal is also low at sufficiently high temperatures. Therefore, the DLTS signal has a maximum value as a function of temperature when the time constant is the same order of magnitude as the time interval $t_2 - t_1$.

$$\tau_{e,\max} = \frac{t_2 - t_1}{\ln(t_2/t_1)} \quad (2)$$

The concept of rate window is introduced into the conventional DLTS. For another rate window, the maxima are located at other temperatures. Thus, the concentration of defects is determined from the height of the maximum.^[103,104] Then, an Arrhenius plot can be obtained, and the DLTS signature of a deep-level defect is detectable using the transient capacitance from thermal sweeping at different rate windows. The activation energy on the trap center can be derived through the slope of the Arrhenius plot of the DLTS maxima as a function of temperature, and the capture cross section can be obtained through its intercept.

DLTS has been applied in the study of SiC-related defects, including ITs, NITs, and point defects in the SiC epilayer near the interface.^[105] Whether majority or minority carriers are detectable depends on the carrier injection conditions. Typically, Schottky barrier diodes are used for detecting majority carrier traps and pn junction diodes are used for detecting

minority carrier traps. **Figure 6a** is an example of a typical DLTS spectrum showing dominant deep levels of $Z_{1/2}$ and $EH_{6/7}$ of n-type 4H-SiC diodes. Meanwhile, the remaining positive DLTS signals also indicate that all peaks are associated with the thermal emission of the majority of deep-level carriers. To further precisely study DLTS spectra of SiC-related defects, refinements of the conventional DLTS have been proposed.

3.1.1. Deep-Level Transient Fourier Spectroscopy

In complex emission processes, it is often difficult to conclude from single transient curves by conventional DLTS. To avoid the drawbacks, a new analytical technique deep-level transient Fourier spectroscopy (DLTFS) was developed.^[106,107] The DLTFS technique can directly extract trap parameters from the transient signals without the need to indirectly determine the time constants from temperature-dependent curves. Consequently, the behavior of the transient can be analyzed and assessed during the temperature scanning measurement. DLTFS is widely used to understand electrically active defects in SiC due to its ability to effectively handle overlapping emissions, its good signal-to-noise ratio, and the improved sensitivity in characterizing traps. Alfieri et al. used DLTFS to perform the electrical characterization of n-type SiC epilayers and found four

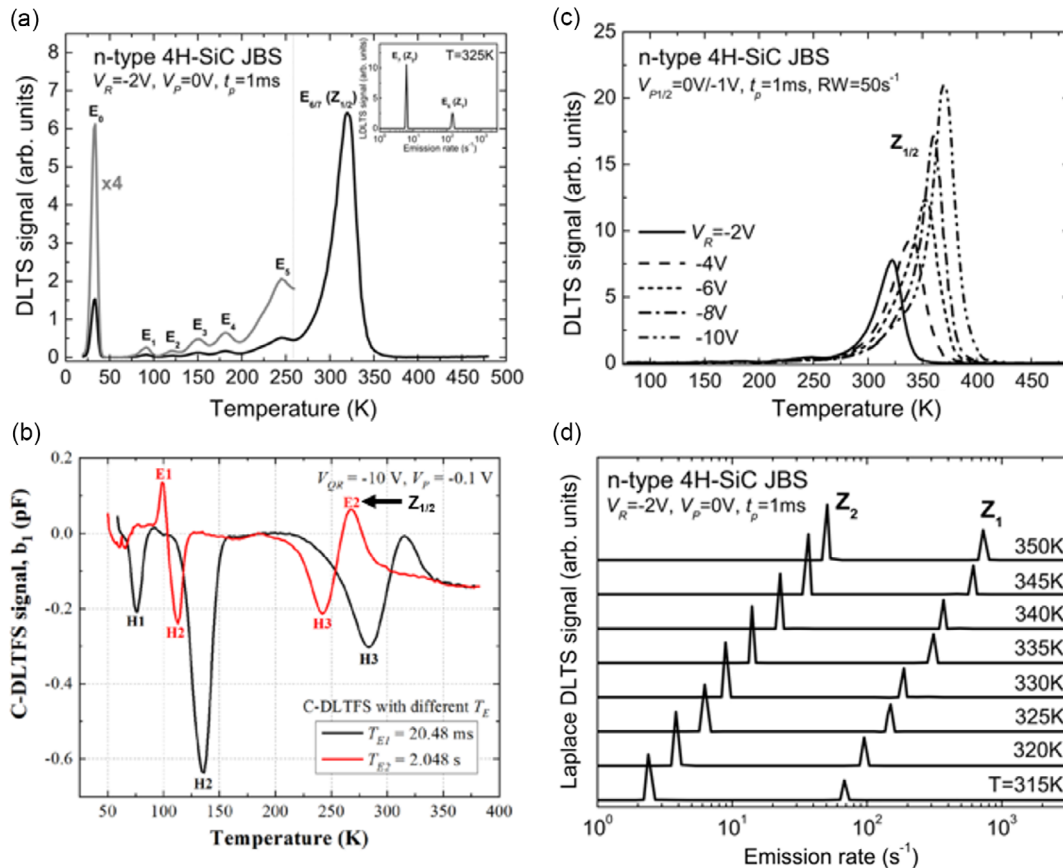


Figure 6. DLTS spectra of the $Z_{1/2}$ centers in n-type 4H-SiC epilayers. a) Conventional DLTS. Reproduced with permission.^[112] Copyright 2020, AIP Publishing. b) DLTFS. Reproduced with permission.^[109] Copyright 2023, Springer Nature. c) D-DLTS. d) L-DLTS. Reproduced with permission.^[112] Copyright 2020, AIP Publishing.

deep energy levels in the range of 0.2–0.73 eV lower than the conduction band.^[108] Figure 6b illustrates the DLTS peaks of majority carrier and minority carrier emission in the 4H-SiC PiN diode under different emission transient conditions and their corresponding trap energy levels.^[109]

3.1.2. Double-Correlation DLTS

The double-correlation DLTS (D-DLTS) technique, as proposed by Lefevre and Schulz, represents an innovative modification to the conventional method.^[110] This method employs two pulses of different amplitudes to define a narrow interval in the depletion layer for trap detection instead of the traditional single amplitude pulse. The D-DLTS approach eliminates the detrimental effects typically observed in the contact region through double correlation, thus reducing the measurement noise and enabling a more accurate determination of the deep level defect profile. Moreover, it can analyze the dependence of the emission time constant on the electrical field.^[110,111] By D-DLTS spectra of n-type 4H-SiC junction barrier Schottky (JBS) diodes as a function of reverse bias, Gelczuk et al. found that the peak of D-DLTS spectrum is affected by the applied reverse bias voltage, as presented in Figure 6c.^[112] Also, Evwaraye investigated the dependence of the emission rate on the electric field and the effect of electron irradiation on the $Z_{1/2}$ centers in 4H-SiC devices by using D-DLTS.^[113] Shota Kozakai et al. analyzed the depth profiles of the deep energy levels induced by reactive ion etching in the whole bandgap of 4H-SiC by D-DLTS.^[114]

3.1.3. Laplace DLTS

Laplace DLTS (L-DLTS) has a higher resolution than the conventional DLTS and can separate traps with similar emission rates.^[115–118] The standard DLTS gives featureless peaks, while the L-DLTS reveals that each defect in the thermal emission process has its characteristic signal. Capan et al. discovered that $Z_{1/2}$ centers consist of two different components by combining L-DLTS and theoretical calculations.^[68] Figure 6d is an example of this and it shows two components of $Z_{1/2}$ centers in

4H-SiC JBS sample.^[112] In the study of Alfieri and Kimoto, the overlapping emission rates of EH₆ and EH₇ trap levels in n-type 4H-SiC were distinguished by L-DLTS, confirming that the nature of the EH_{6/7} trap levels is related to V_C defects.^[118]

3.1.4. Constant-Capacitance DLTS

Constant-capacitance DLTS (CC-DLTS) is commonly used for interface measurement due to its high-energy resolution. During the measurement, capacitance is kept constant while the applied voltage is dynamically changing through a feedback loop.^[119,120] The trap information from interface states, oxide traps, and bulk traps in CC-DLTS can be extracted from the time-varying voltage. Trap density depth profiling is also suitable for CC-DLTS. Thus, Hatakeyama et al. employed CC-DLTS to investigate the impact of the oxidation atmosphere and crystal faces on the density of IT.^[120] Okada proposed a quantitative analysis method for extracting NITs at 4H-SiC interface using CC-DLTS.^[121] As presented in Figure 7a, using CC-DLTS method, the DLTS signal shows the signals of two types of NITs in SiO₂/SiC interface as a function of pulse voltage. Jayawardhena et al. demonstrated that both traps are inherent to thermal SiO₂ interface.^[122] In addition, it is possible to observe different ITs by using samples with different SiC wafer orientations, as compared in Figure 7b.

These modified DLTS techniques offer a higher accuracy compared to conventional DLTS. DLTS utilizes transients to directly determine the emission time constant, facilitating automated control of the measurement. D-DLTS reduces the measurement noise and accurately determines deep-level defect profiles. L-DLTS yields a higher resolution to distinguish the traps with very close energy levels. CC-DLTS is suitable for detecting interface states at SiC/SiO₂. The basic principle used in these DLTS methods is junction capacitance transient and the commonly applied sample structure includes pn junction, Schottky junction, and MOS structure. The various signal processing features allow the majority carrier trap to be distinguished from the minority carrier trap. In SiC, to use DLTS measurement, the device leakage current of the sample is required to

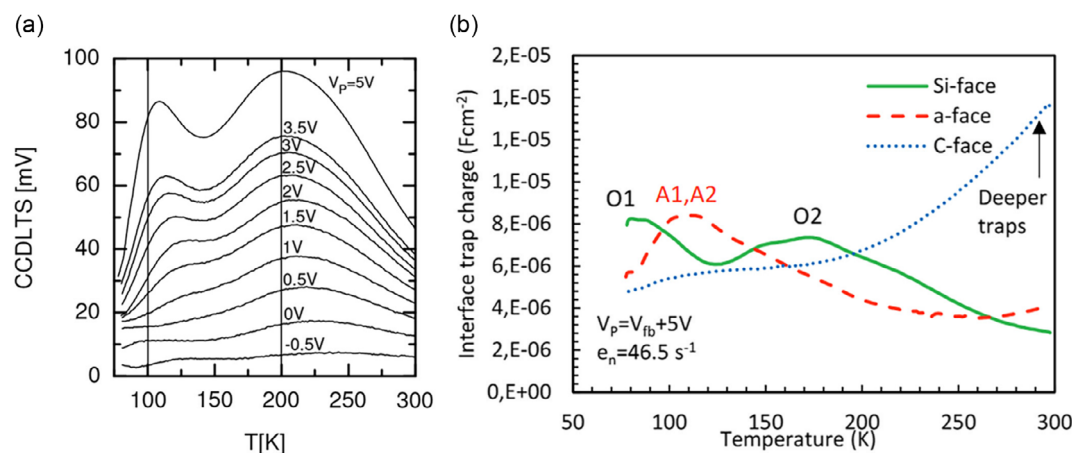


Figure 7. CC-DLTS spectra for 4H-SiC MOS capacitors a) at different pulse voltages Reproduced with permission.^[188] Copyright 2010, Springer Nature and b) at different wafer orientations. (Reproduced with permission.^[122] Copyright 2019, Trans Tech Publications).

be minimal in order to obtain an accurate DLTS signal, and the measurement must be conducted in a wide temperature range in order to detect the shallow and deep energy levels.^[123] It was discovered that using small Schottky barrier heights for DLTS could produce inaccurate results for the concentration of energy depth defects.^[124]

3.2. Capacitance–Voltage Method

Capacitance-voltage (CV) measurement is a widely applied way of characterizing defects in SiC MOS-based devices due to its efficiency, feasibility, and sensitivity. A DC voltage and a small amplitude AC voltage are applied simultaneously to the electrode of the device as shown in **Figure 8**. Carriers move within the semiconductor under the voltage bias, and defects capture or emit carriers. Each interface defect causes a deviation between the actual CV curve and the ideal CV curve. Therefore, the interface states can be detected by changing the voltage sweep rate and sweep direction.^[125,126] This measurement method can quantify the concentration and distribution of defects by capturing or emitting the charges within the bandgap. There are several techniques that have been developed to extract interface states density at the SiC/SiO₂, namely, low-frequency (quasi-static) CV methods,^[127] conductance,^[24,128–133] high-frequency (Terman) CV methods,^[24,134] high-low-frequency CV methods,^[135,136] $C-\psi_s$ method,^[129,131] and so on. These techniques have been used in many reports to achieve separation of ITs and NITs.^[44,99,102,137–139]

3.2.1. High–Low-Frequency CV

The high–low-frequency technique is one of the most common methods for measuring the density of interface states of SiC MOS structure. This method assumes that the interface states respond completely and the low-frequency capacitance contains the contributions from all the interface states at low frequencies. At high frequencies, the interface states do not fully respond, and thus the high-frequency capacitance may not contain these interface states' information. D_{it} is extracted from the differential capacitance by comparing the low-frequency CV curve with the high-frequency CV curve and is calculated using^[77,135,136,140]

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (3)$$

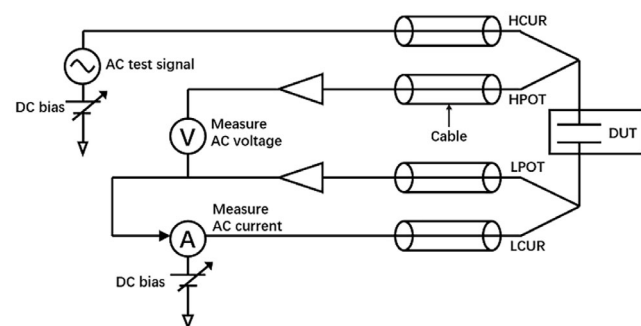


Figure 8. A simplified diagram of the experimental setup for CV measurements.

where q is the value of electron charge, C_{ox} is the oxide capacitance, C_{lf} is the capacitance at low frequency, and C_{hf} is the capacitance at high frequency. In order to minimize the flat band voltage shift in the CV curve caused by carrier captured in the accumulation region, the low-frequency and high-frequency capacitances are measured simultaneously. As shown in **Figure 9**, in the accumulation region of a 4H-SiC MOS capacitor, there exists a variation in the CV curves at various frequencies, and the value of the quasi-static capacitance is larger than that of the high-frequency capacitance, which is caused by the interface states. The electrical response of NITs is separated from that of ITs. The appearance of inflections in the CV curve is common and usually attributed to NITs.^[43,102,141]

The typical high–low CV method has some limitations. Firstly, it is usually performed at 1 MHz for high-frequency capacitance, which includes the interface states with fast emission rates when the D_{it} is high.^[77] Therefore, the interface states located at the shallow levels (energy levels shallower than $E_c - 0.2$ eV or $E_v + 0.2$ eV) are underestimated.^[24] However, if higher frequencies are used, the effect of series resistance must be considered. As demonstrated in Figure 9, the effect of parasitic impedance at the extremely high frequency (100 MHz) is calibrated. Yoshioka et al. detected very fast states at SiC/SiO₂ interface with the response frequency of 100 MHz or higher at room temperature.^[131] Second, the low-frequency capacitance is measured in the quasi-static mode and usually does not contain interface states with slow emission rates at room temperature,^[129] thereby grossly underestimating the interface states located at deep levels (energy levels deeper than $E_c - 0.5$ eV or $E_v + 0.5$ eV). Therefore, D_{it} can be reasonably detected in a narrow range of energy by the conventional high–low-frequency at room temperature. To improve the energy range and the accuracy of D_{it} , it is necessary to measure high-frequency capacitance at higher frequencies and in a wider temperature range.

3.2.2. Conductance Methods

The conductance method is generally used as a sensitive and accurate technique to extract D_{it} , proposed firstly by Nicollian and Goetzberger.^[130,132,142] It is worth mentioning that if

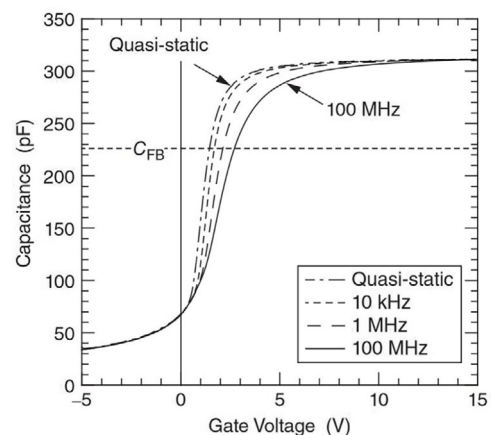


Figure 9. CV curves of an n-type 4H-SiC MOS capacitor at various frequencies. Reproduced with permission.^[129] Copyright 2012, AIP Publishing.

compared with other CV methods, it is more sensitive to detect D_{it} in the weak inversion and depletion portion of the bandgap. It also allows the calculation of the time constant, the capture cross sections of traps, and surface potential fluctuations.^[132] The equivalent parallel conductance of the SiC MOS capacitor is measured as a function of frequency and bias voltage within depletion as demonstrated in **Figure 10**. Its maximum measurement frequency can increase up to 100 MHz.^[129] The conductance–frequency characteristics should yield a peak which originates from the interface states at a specific frequency. All the interface states have their definite peaks in G/ω – f curves and can be monitored. The extraction of interface state conductance from measured conductance makes use of small-signal AC equivalent circuits. The parallel conductance can be extracted by^[133,136]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (4)$$

where C_m is the measured capacitance, G_m is the measured conductance, ω is the angular frequency, and ω is the angular frequency. G_p/ω can be related to the D_{it} by the following equation:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{\sqrt{2\pi}\sigma_s^2} \int_{-\infty}^{+\infty} \frac{\ln[1 + (\omega\tau e^{-\Delta U_s})^2]}{2\omega\tau e^{-\Delta U_s}} e^{-\frac{\Delta U_s^2}{2\sigma_s^2}} \cdot d\Delta U_s \quad (5)$$

where U_s is the normalized surface potential and σ_s is the standard deviation of the surface potential. Compared with the conductance curves of conventional ITs, the conductance curves with obvious abnormal characteristics are referred to as NITs, which have a larger cross section than conventional ITs.^[77,102]

In contrast to capacitance, conductance is less affected by semiconductor capacitance and easier to interpret, i.e., all observed peaks are valid data, though it is time consuming. One restriction of the conductance technique is the limited range of energy that can be measured even at high temperatures.^[24] It is insensitive to detect the fast traps and slow traps in the commonly used frequency range. Fast traps with a very short response time can only be detected by high-frequency or low-temperature conductance.^[131] Due to frequency limitations, the conductance measurements should be performed over a wide range of temperatures. For example, Zhai et al. measured the thermally oxidized 4H-SiC/SiO₂ MOS sample from 75 K to

270 K and distinguished interface states from unusual parameters extracted from the conductance method, i.e., detecting the ITs and NITs.^[102]

3.2.3. Surface Potential Methods

The energy position of interface states is usually determined by the surface potential ψ_s , so it is crucial to determine ψ_s of SiC accurately. Berglund proposed that ψ_s can be calculated from low-frequency capacitance and oxide capacitance using^[77,136]

$$\psi_s(V_G) = \int \left(1 - \frac{C_{if}}{C_{ox}}\right) dV_G + A \quad (6)$$

where A is an integration constant and is determined based on the flat band capacitance in high-frequency measurements. As some fast interface states still respond at 1 MHz in traditional high-frequency CV measurements, the flat-band capacitance is affected. As a result, the corresponding energy level shifts and the value of D_{it} underestimates the density of these fast interface states at a specific energy level.^[143] To address the possibility that ψ_s may be affected by these fast interface states, Yoshioka et al. proposed one C – ψ_s method that ψ_s can be accurately determined based on depletion capacitance. This C – ψ_s method evaluates D_{it} at SiC/SiO₂ based on the difference between quasi-static and theoretical capacitances almost without frequency limits.^[129,131,144]

$$D_{it}(C - \psi_s) = \frac{C_{QS} - C_{theory}(\psi_s)}{Aq^2} \quad (7)$$

The theoretical capacitances can be calculated by the obtained ψ_s using

$$C_{theory}(\psi_s) = \frac{qAN_D \left| \exp\left(\frac{q\psi_s}{kT}\right) - 1 \right|}{\sqrt{\frac{2kTN_D}{\epsilon_{SiC}} \left\{ \exp\left(\frac{q\psi_s}{kT}\right) - \frac{q\psi_s}{kT} - 1 \right\}}} \quad (8)$$

where C_{QS} is the capacitance at quasi-static mode, A is the active area, N_D is the donor concentration of the SiC epilayer, k is the Boltzmann constant, T is the absolute temperature, and ϵ_{SiC} is the dielectric constant of SiC. **Figure 11** manifests the variation of capacitance of a n-type SiC MOS capacitor with the surface potential at various frequencies. With the increase of measurement frequency, the measured capacitance approaches the

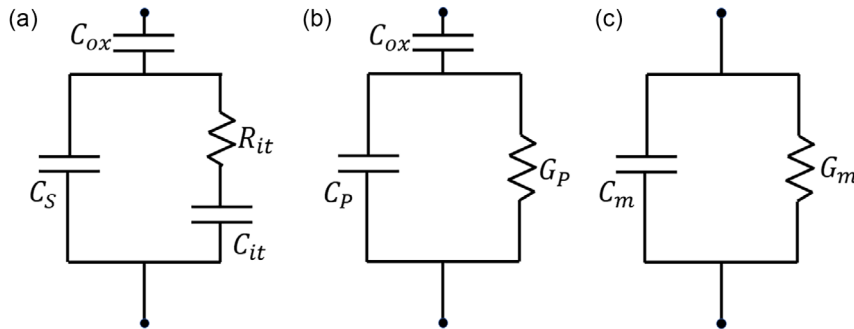


Figure 10. Equivalent circuits of a MOS capacitor for conductance measurements: a) equivalent circuit with IT, b) simplified circuit, and c) measurement circuit.

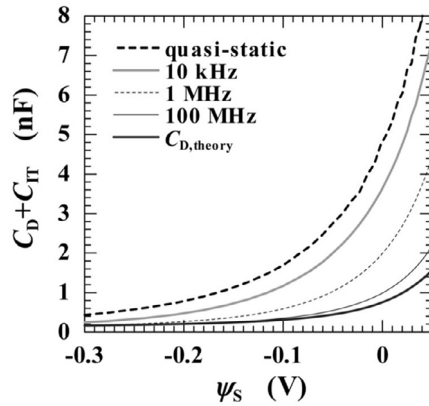


Figure 11. Variation of capacitance with surface potential at various frequencies for a n-type SiC MOS. Reproduced with permission.^[129] Copyright 2012, AIP Publishing.

theoretical value, because the traps at the interface state hardly respond to the higher frequency.

By employing the $C-\psi_s$ method, Nakazawa et al. found that D_{it} could be determined and a correlation between D_{it} and the field-effect mobility μ_{FE} could be established.^[145] Rummel et al. concluded that the D_{it} distribution obtained by $C-\psi_s$ method is not only accurate near the conduction band edges or valence band edges, but also sensitive to the measurement noise and the underestimated gate oxide capacitance.^[146] However, as it can only measure the interface state with response time within the measurement frequency range, it is difficult to detect extremely slow states that do not respond to voltage sweep. Using $C-\psi_s$ method, it is required that the doping concentration is uniform from the SiC/SiO₂ surface to the epitaxial layer. Yoshioka et al. utilized the $C-\psi_s$ based on depletion capacitance to estimate the density of the interface state in SiC MOS structures, which is in good agreement with the conductance method.^[129,131]

3.2.4. Other Methods

The quasistatic method is effective for detecting the fast interface states and is one of the most commonly used methods. D_{it} extracted by quasi-static methods is strongly dependent on the calculation of theoretical capacitance and surface potential.^[143] This can possibly lead to inaccuracy of the final result.

In the high-frequency (Terman) method, due to the IT occupancy varying with the gate bias, the high-frequency CV curves stretch along the gate voltage axis. Therefore, the interface state density can be extracted using the Terman method. However, D_{it} of SiC/SiO₂ interface at room temperature is subject to serious underestimation because small deviations in the surface potential and doping concentration can have a large effect on the extracted interface states. As a result, this technique is only useful in high interface state density.^[123]

Figure 12 compares results obtained from different CV methods. Figure 12a,b exhibit the D_{it} extracted by four methods that have a good agreement in the energy range of $E_c - 0.05 - E_c - 0.18$ eV at 150 K and in the energy range of $E_c - 0.18 - E_c - 0.3$ eV at 300 K.^[147] The results clarify that within

a certain temperature range, a reliable defect density measurement can only be carried out over a limited energy range. The interface states respond consistently to the measurement signals of all four measurement methods in these energy ranges. Figure 12c,d demonstrate that annealing in NO can reduce the interfacial state density. The D_{it} distributions obtained by the $C-\psi_s$ method, the conductance method, and the high-low frequency methods (high frequency is 100 MHz) are also consistent as presented in Figure 12c. However, the interface state density obtained by the conventional (1 MHz) high-low frequency methods is lower than the other methods. The reason is that the fast interface states do not correspond under frequencies lower than 1 MHz. The interface state density evaluated by $C-\psi_s$ is higher than the density measured by other methods, especially in the range of $E_c - E_T < 0.4$ eV, as shown in Figure 12d. It presents that $C-\psi_s$ method is more sensitive for the interface states near the conduction band.

The results of D_{it} measurements by different methods under different conditions partially vary, because they are influenced by the parameters of measurement conditions and samples. For example, Vidarsson et al. observed two categories of fast and slow NITs at 4H-SiC/SiO₂ interface by high-low CV and conductance methods at low temperatures.^[43] Nakazawa et al. characterized the interface properties of 4H-SiC MOS structures using conductance, high-low, and $C-\psi_s$ methods. It was observed that if compared with the Si-face of 4H-SiC, the density of fast interface states is much lower in the a-face and (1 $\bar{1}$ 00) face.^[145]

3.3. Charge Pumping

Charge pumping (CP) is a well-established measurement method, known for its high sensitivity to individual IT detectability^[148] and its detectability of most traps across the bandgap, particularly at the semiconductor dielectric interface in MOSFET devices, especially in planar MOSFETs. The basic method of CP was initially discovered by Burgler and Jespers,^[149] and it could profile the trap density throughout the entire energy gap.^[44] Important information about the trap-level parameters, such as the density of ITs and the average capture cross section can be extracted from the CP current (I_{CP}).

The setup for the CP experiment is shown in **Figure 13**. As a pulse bias is applied to the gate electrode of MOSFET, the channel region alternates between accumulation and inversion under the continuous function of gate pulse voltage. The drain and source terminals are connected and grounded or given a small reverse bias. I_{CP} is measured at the substrate by connecting a sensitive ammeter due to carrier recombination at the SiC/SiO₂ interface, and it is proportional to the mean trap density and frequency.

The applied pulse bias causes the I_{CP} to flow through the channel region. As a portion of the I_{CP} is trapped by the IT in the channel region, the interface state density can be calculated from the I_{CP} by^[149]

$$\bar{D}_{it} = \frac{I_{CP}}{\Delta E * A_G * q * f} \quad (9)$$

where A_G is the gate area of the MOSFET, \bar{D}_{it} is the mean interface state density, and ΔE is the energy interval. From this

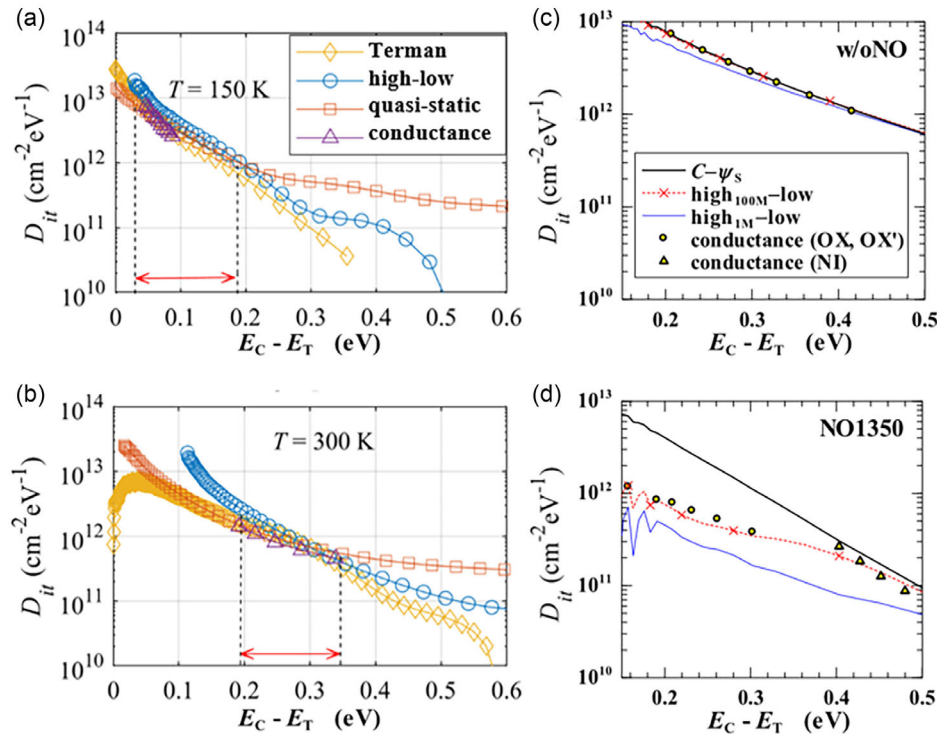


Figure 12. Comparison of D_{it} distributions calculated by different methods for a 4H-SiC MOS structure at a) 150 K and b) 300 K; dashed lines and arrows mark the range with high consistency. Reproduced with permission.^[147] Copyright 2019, AIP Publishing. c) w/o NO and d) annealed in NO at 1350 °C. Reproduced with permission.^[131] Copyright 2012, AIP Publishing.

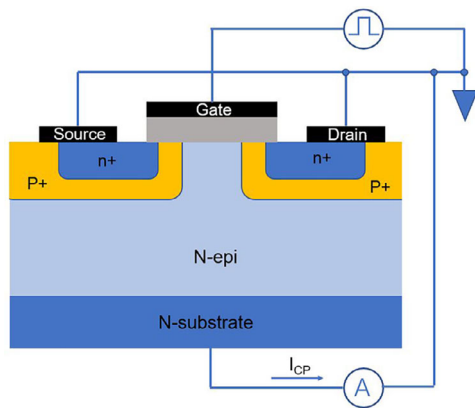


Figure 13. Measurement circuit of the n-channel MOSFET for basic CP.

formula, the energy distribution of the ITs cannot be directly extracted. Then, great efforts have been put to obtaining an energy-dependent distribution of ITs,^[150,151] and a few CP methods have been developed. There are various shapes of the gate pulse bias trains being applied, such as square, triangular, trapezoidal, sinusoidal, and trilevel waveforms.^[152] **Figure 14a** shows the variable amplitude and constant-base sweep method that the base voltage is kept constant, while the variable voltage amplitude is pulsed from accumulation into inversion. With the increase of pulse voltage amplitude, the I_{CP} tends to be saturated. **Figure 14b**

shows the constant-amplitude and voltage-base sweep mode, in which maintains a constant amplitude while increasing the base voltage from accumulation into inversion.

In addition to the above two methods, other CP techniques are used. In some cases, the rise time and fall time of the gate pulse can be changed which determines the time window available for capture and emission of trapped charges,^[151] or the I_{CP} can be measured as a function of frequency. As illustrated in **Figure 15**, variable-amplitude sweep and constant-amplitude sweep measurements were performed using trapezoidal pulse trains with different pulse fall times t_f . The I_{CP} introduces an extra current component known as the geometric component during actual testing. Switching from the inversion to accumulation transition, the geometric component emerges because certain electrons are unable to reach the source or drain region.^[149,151] As shown in **Figure 15b,c**, when the gate voltage increases, the current does not saturate and it increases with decreasing fall time because of the geometrical components included in the current. Due to the interface state and geometric component of 4H-SiC MOSFETs, the SiC CP curve of the constant-amplitude sweep method is asymmetrical and there is a long current tail on the curve as highlighted in **Figure 15e,f**. It is also observed that the length of the current tail decreases with the increase of pulsed fall time. The reasonable way to determine whether a geometric component is present is to examine the shape of the CP curve.^[153] Due to the lower density of interface states near the conduction band edges in NO-annealed 4H-SiC MOSFETs, the effect of the geometric

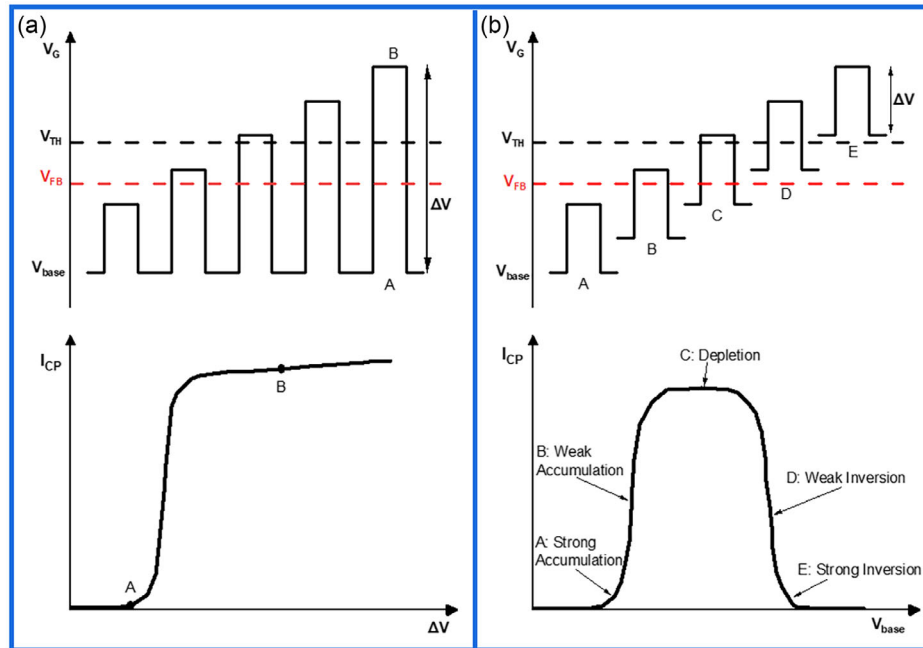


Figure 14. Pulse waveform for a) constant-base/variable-amplitude sweep method and b) constant-amplitude/voltage-base sweep method.

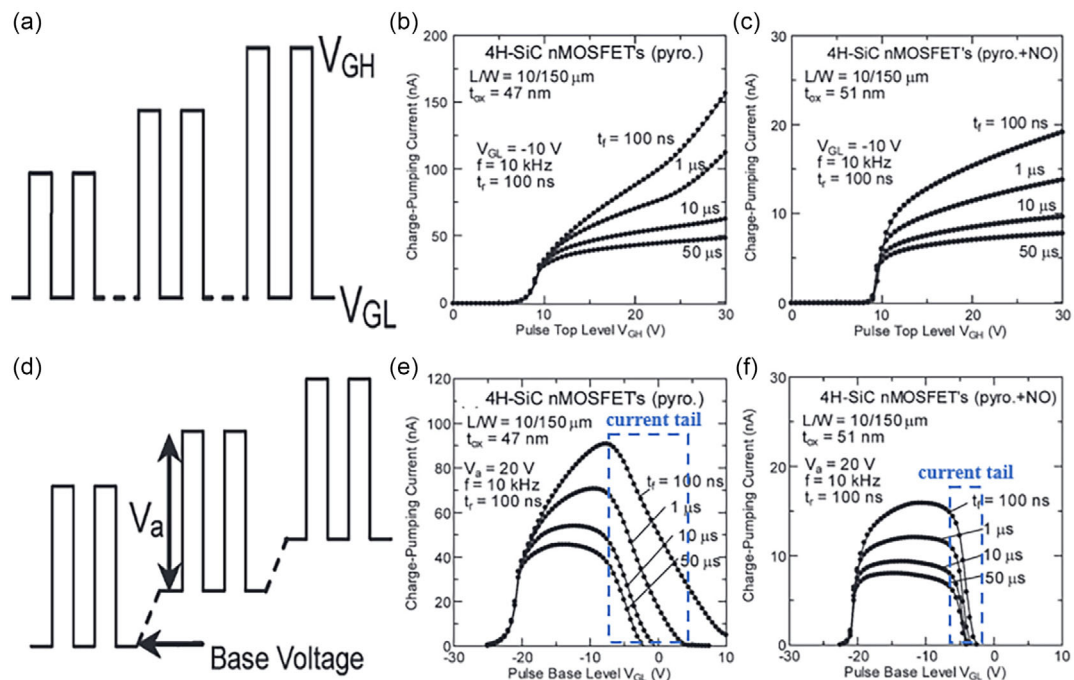


Figure 15. a) Pulse trains waveform, b) measurement current of unannealed 4H-SiC MOSFETs, and c) NO-annealed 4H-SiC MOSFETs for constant-base/variable-amplitude sweep method; d) pulse trains waveform, e) measurement current of unannealed 4H-SiC MOSFETs, and f) NO-annealed 4H-SiC MOSFETs for constant-amplitude/voltage-base sweep method. Adapted with permission.^[154] Copyright 2008, IEEE.

components is smaller. The influence of the geometric component is primary in SiC MOSFETs with the low channel mobility, and the measurement accuracy can be improved by reducing the geometric component.^[151]

In some other cases, the influence of geometric components does not need to be considered. Okamoto et al. studied the effects of pulse rise times and fall times and concluded that the geometric component can be avoided when the fall time is long

enough.^[153,154] Salinaro et al. proposed that by optimizing SiC MOSFETs with the proper geometry and the measurement parameters carefully, the geometric component can be neglected.^[155]

As discussed above, conventional CP was originally developed for 4-terminal lateral MOSFETs with separated source and body contacts. However, many commercial power MOSFETs have only three terminals. Then, Passmore et al. developed a three-terminal CP (3T-CP) technique for vertical MOSFET with P-body substrate connected to the source.^[156] In the 3T-CP method, IT density can be extracted from the drain current I_{CP} by grounding the source and applying the measuring pulse to the gate. Zhou et al. used modified 3T-CP to reveal possible failure mechanisms of 4H-SiC MOSFETs during aging experiments and short-circuit tests.^[157,158] As demonstrated in **Figure 16a**, it can be observed from the curves that I_{CP} shifts toward the negative direction until the end of the unclamped-inductive-switching (UIS) stress cycles. It indicates the major cause of the failure phenomena is the hole injecting and trapping in the gate oxide. In **Figure 16b**, the CP curves of SiC MOSFET shift toward the negative direction with the increase in the number of short-circuit tests. It represents that there are positive charges formed in the oxide due to the hole trapping during the short-circuit tests.

CP is sensitive to detecting and distinguishing ITs and NITs by adjusting the CP parameters properly.^[159] Altering the voltage applied to the gate enables the extraction of traps with different activation energies.^[160] The characterization of 4H-SiC MOSFETs requires large pulse amplitudes due to the obvious difference between their thresholds and flat-band voltages.^[154] Okamoto et al. investigated the anomalous CP characteristics of 4H-SiC MOSFETs and illustrated the effect of interface states on the flat band voltage and the threshold voltage from the line shape of the CP curve.^[154] Yu et al. used frequency-dependent CP at different gate voltages and found that a significant fraction of the total traps are located in the near interface oxides.^[161] The fast ITs also contribute to the I_{CP} so that IT charge dominates when the frequency is in the order of MHz. The conventional CP technique requires a measurement time in the range of tens of seconds. As a result, there is a delay time between the removal of the applied stress and the measurement, where the trap recovers

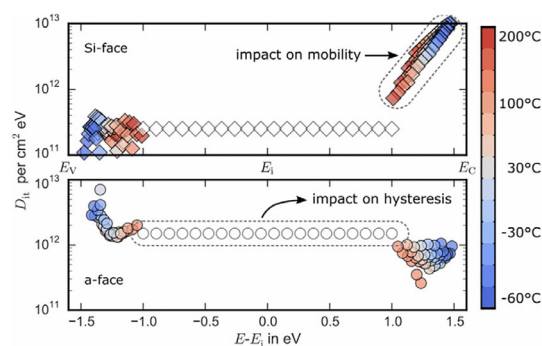


Figure 17. Interface states energy distribution of 4H-SiC/SiO₂ for Si-face and a-face were extracted using CP. Reproduced with permission.^[168] Copyright 2016, IEEE.

quickly, and the extracted interface state density is underestimated. To avoid this situation, the on-the-fly CP (OTF-CP) method has been developed to reduce the recovery effect after stress removal.^[162] The OTF-CP method has been used to study the generated interface states during bias temperature instability stress and the threshold voltage shift of 4H-SiC MOSFETs.^[163–166] As shown in **Figure 17**, Si-face devices exhibit an exponentially increasing interface state density at the edge of the 4H-SiC conduction band and the IT density on a-face devices originates from deep states around the bandgap.^[167,168] Therefore, charge pump measurements can be a useful and reliable tool by setting reasonable test parameters for interface state characterization of SiC MOSFETs.

These electrical characterization techniques have different capabilities of defecting the electrically active defects. The combination of these techniques can provide multilevel and multian-gle defect information and also fully and accurately reveal the defect characteristics in materials and devices. **Table 1** summarizes the widely used characterization methods and discusses their advantages and limitations. Understanding the advantages and limitations of different technologies helps to acquire reliable defect information on SiC materials and devices. This can further provide important feedback for the research and

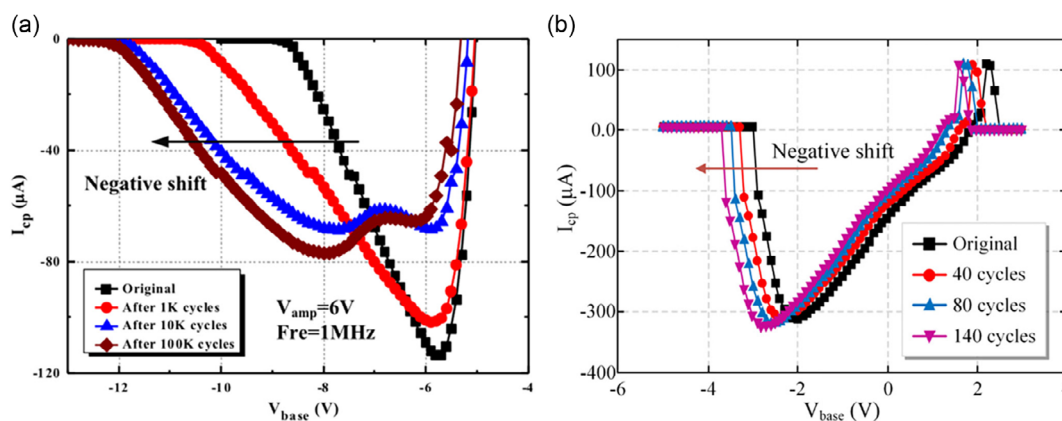


Figure 16. 3T-CP measurements for 3-terminal SiC MOSFET a) after different UIS stress cycles. Reproduced with permission.^[189] Copyright 2018, Elsevier Ltd. b) Every specified cycle of short-circuit tests. Reproduced under the terms of the CC-BY license.^[190] Copyright 2021, The Author. Published by IEEE.

Table 1. An overview of the widely used characterization methods for evaluating the density of active traps.

| Characterization methods | Device typology | Advantages | Limitations | References |
|--------------------------|--|--|--|-----------------------|
| DLTS | MOS capacitor, SBD, pn junction diodes | Ability to detect defects at very low concentrations and to distinguish them between energy-level positions and concentrations at deep-level defects, and to study the temperature dependence of electroactive defects | A wide temperature range requirements and samples require small leakage and large Schottky barrier heights | [103,122,124,188,191] |
| High–Low CV | MOS capacitor | Test equipment and methods are convenient | Only part of the ITs can be detected, accuracy is affected by surface potential | [24,129,136,192] |
| Conductance | MOS capacitor | It is more sensitive to detect D_{it} in the weak inversion and depletion portion of the band gap | Wide temperature range and time-consuming | [136,193] |
| $C-\psi_s$ | MOS capacitor | It can monitor the very fast interface states and without a limitation of the measurement frequency | Difficult to detect extremely slow states that do not respond to voltage sweep | [77,129,131] |
| CP | MOSFET | Profile the trap density throughout the entire energy gap | Specific measurement conditions and difficult to determine the energy-level distribution accurately | [153,154,194] |

development of SiC devices. Furthermore, these methods lack lateral resolution. During last 20 years, scanning probe microscopy based approaches, such as scanning capacitance microscopy,^[169–176] scanning extended resistance microscopy,^[177–182] and scanning microwave impedance microscopy,^[183–185] have demonstrated their respective advantages in electrical characterization at the nanoscale. These techniques are capable of providing high spatial resolution resistance, capacitance, and impedance measurements and are particularly suitable for local electrical characterization of 4H-SiC materials and 4H-SiC/SiO₂ interfaces. They have been widely used to assess the electrical activation of implanted dopants in 4H-SiC epitaxial layers during postimplantation annealing processes, 2D carrier profiling and the effect of annealing of the oxide layer after deposition on the electrical properties of the 4H-SiC/SiO₂ interfaces. However, despite these advances, these methods still face some challenges in practical applications, such as how to further improve the spatial resolution, to enhance the measurement accuracy, and to minimize the impact of probe-sample interactions on data reliability. It will become a trend to multidimensionally characterize the 4H-SiC and the interfaces by combining these microscale electrical techniques with macro-scale electrical characterization (such as CV, DLTS, and CP).

4. Summary

SiC is a more complex material compared to silicon but has more advantages in the field of high-power electronic device applications. However, there are various active defects in SiC materials, such as point defects and interface states, which significantly impact the performance and reliability of devices. Therefore, it is essential to understand and characterize electrically active defects in SiC materials. This review analyzes in detail the electrical properties of SiC active defects, revealing the effects of different defect types on the performance of SiC devices. It also discusses the application of various electrical characterization

techniques, such as DLTS, CV, and CP characterization techniques. This comprehensive analytical approach not only deepens the understanding of the intrinsic properties of SiC materials but also provides a scientific basis for device design and optimization. The research on SiC materials will continue to advance, especially in the areas of defect engineering and device performance optimization. With the development of novel characterization techniques and innovations in data analysis methods, combining nanoscale with macroscopic electrical characterization techniques, the defect properties of SiC materials will be revealed more comprehensively so that defects in SiC can be more precisely controlled and exploited to achieve higher-performance electronic devices. In addition, a deeper understanding of the dynamic behavior of defects in SiC will help to develop new device structures and fabrication processes, further promoting the use of SiC in high-power, high-frequency, and high-temperature applications.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

4H-SiC, defects, electrical characterizations

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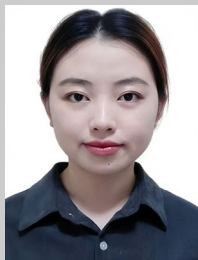
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