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Deep levels in silicon–oxygen superlattices

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Abstract

This work reports on the deep levels observed in Pt/Al_2O_3/p-type Si metal-oxide-semiconductor capacitors containing a silicon–oxygen superlattice (SL) by deep-level transient spectroscopy. It is shown that the presence of the SL gives rise to a broad band of hole traps occurring around the silicon mid gap, which is absent in reference samples with a silicon epitaxial layer. In addition, the density of states of the deep layers roughly scales with the number of SL periods for the as-deposited samples. Annealing in a forming gas atmosphere reduces the maximum concentration significantly, while the peak energy position shifts from close-to mid-gap towards the valence band edge. Based on the flat-band voltage shift of the Capacitance–Voltage characteristics it is inferred that positive charge is introduced by the oxygen atomic layers in the SL, indicating the donor nature of the underlying hole traps. In some cases, a minor peak associated with P_b dangling bond centers at the Si/SiO_2 interface has been observed as well.

Keywords: deep-level transient spectroscopy, silicon–oxygen superlattices, oxygen–silicon bonds, dangling bonds, MOS capacitor

(Some figures may appear in colour only in the online journal)

1. Introduction

It is well-known that even a minor oxygen contamination, either present on the silicon surface or in the reactor atmosphere is a source of extended defects in a growing epitaxial layer [1–3]. In spite of this, it has been shown that for a controlled deposition of less than a monolayer of oxygen, epitaxial silicon can be subsequently grown, opening the door for the formation of oxygen/silicon superlattices (SLs). Proof of concept has first been demonstrated by Molecular Beam Epitaxial growth [4–6]. More recently, the feasibility of the more industry-compatible chemical vapor deposition (CVD) of Si-O SLs has been demonstrated [7–10]. The interest in such SLs is for their potential application in so-called high-mobility transistors [7–9]. The insertion of an oxygen (sub) atomic layer (AL) in the silicon lattice causes anisotropy in the band structure, yielding a reduction of the effective mass in the transport direction and an increase in the transverse direction. This leads in turn to a higher low-field mobility and on-current, while the second effect gives rise to a lower gate tunneling current, relaxing the requirements on the thickness of the gate dielectric. The use of Si-based SL structures avoids the problems associated with hetero-epitaxy of other semiconductor materials (Ge, InGaAs,…) and offers a silicon surface for the deposition of the gate stack. Finally, there could be potential applications of Si:O alloys for Photovoltaics, based on the higher optical band gap [11].

A key issue in the growth optimization of the Si–O SLs is the control of extended defects and, hence, the preservation of the lattice order beyond the oxygen layer. It has been shown that stacking faults and other extended defects or disorder are easily introduced [7, 9, 10, 12, 13]. Careful investigations have shown that there exists a narrow window of around 0.7 to 0.9 oxygen ALs, for which the epitaxial deposition of silicon can be achieved, using CVD in combination with chemisorption of O_3 at 50 °C [13]. The question remains, however, whether the presence of a (sub)AL of oxygen does or does not introduce electrically active point defects. The latter can compromise the expected mobility enhancement by introducing charged scattering centers or traps.

In order to tackle this question in this paper, Deep-Level Transient Spectroscopy (DLTS) [14, 15] will be applied on

Metal-Oxide-Semiconductor (MOS) capacitors containing Si–O SL with a different number of periods (0, 2 or 5). It will be shown that the presence of the atomic oxygen layers in p-type Si gives rise to a broad band of deep donors around mid-gap. The corresponding density of states (DOS) increases with the number of SL periods and is reduced significantly after a 500 °C forming gas anneal (FGA). As such, the results show a strong similarity with the deep levels found frequently at the Si/SiO_2 interface [16–22].

2. Experimental details

2.1. Process: growth of Si–O SL and MOSCAP fabrication

Boron doped p-Si (100) wafers are used for the fabrication of Si–O SL structures. Silicon layers are deposited in a CVD reactor using silane (SiH_4) as precursor at a temperature of 500 °C with a partial pressure of 20 mTorr using N_2 as carrier gas. The reactor pressure during the deposition is 40 Torr. The O ALs are deposited in an AL Deposition (ALD) reactor using Ozone (O_3) as precursor at 50 °C with the partial pressure of 0.01 Torr generated from O_2 in a TMEIC OP-250H O_3 generator. The CVD and the ALD reactors are connected through the transport chamber in a single platform called the polygon cluster [12]. The transport chamber is maintained in N_2 ambient to minimize the transport contaminations. Low temperature depositions of Si and O AL are performed to limit the diffusion of the oxygen atoms in Si.

First, the wafers undergo a standard clean [10] followed by 2% HF/H_2O clean for 30 s to remove the native oxide, metal contaminations and protect the surface with H-termination. Then the wafers are loaded into the load ports of the polygon cluster. Second, before the depositions a pre-epi clean [3] is performed in the CVD reactor at 850 °C for 2 min at 40 torr in H_2 ambient. The residual O contaminations on the surface and the surface hydrides are desorbed during the high temperature pre epi-clean [3, 10, 12]. The wafers are cooled down to 350 °C in H_2, where the surface reconstructs to form a 2×1 morphology with H termination [12, 13]. Later, the H-terminated 2×1 Si (100) wafers are *in situ* transferred to the ALD reactor for the deposition of oxygen AL. Wafers are transferred back to the CVD reactor for the epitaxial deposition of Si on the oxygen AL. Thus the wafers are moved between the CVD and ALD reactors, until the desired number of Si and the O depositions of the SL are achieved. The O contamination recorded during the transfer is 2.97×10^{13} O atoms cm^{-2}, an order of magnitude lower than the desired O-content (1 oxygen AL = 6.78×10^{14} atoms cm^{-2}). Therefore, the *in situ* depositions are suitable for the growth of epitaxial Si–O SL with well controlled O-content, Si thickness and crystalline quality.

Si–O SL based MOS capacitors are fabricated by depositing 1 nm SiO_2 and 4 nm of Al_2O_3 at 300 °C on the Si–O SL structures. The Al_2O_3 is deposited by ALD using trimethyl aluminum (TMA) and H_2O chemistry. The Pt top metal contacts are evaporated through a shadow mask with a diameter varying between 50 and 500 μm. The bottom electrode consists of blanket Pt deposition (figure 1).

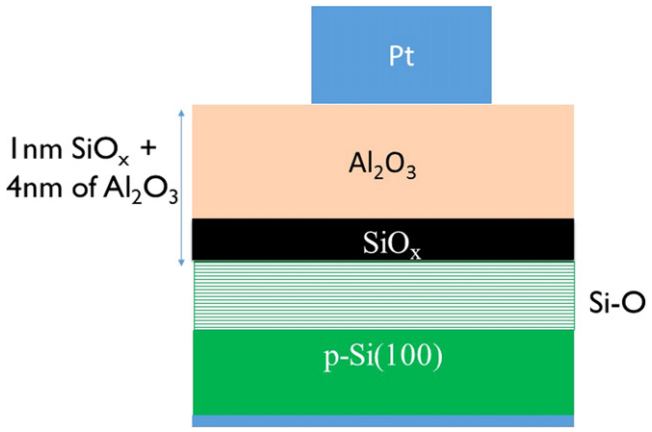

Figure 1. Schematic structure of a MOS capacitor on a Si–O superlattice sample.

2.2. Measurements conditions

Fourier-transform DLTS (FT-DLTS) [23] has been performed, with a fixed measurement frequency of 1 MHz of the Boonton capacitance bridge. Spectra have been recorded either isothermally, by sweeping the sampling period t_w (~pulse period) or by scanning the temperature from 75 K to room temperature (RT). Before cooling the sample in the flow cryostat, capacitance–voltage (C–V) and current–voltage (I–V) characteristics are recorded at RT on MOS capacitors with a diameter $\Phi = 500\ \mu$m. Typical results are shown in figure 2(a) for the as-deposited samples and in figure 2(b) for the 2 period SL capacitors before and after FGA. First of all, one can conclude from the accumulation found at negative gate voltage that the epitaxial layers, while nominally undoped, behave as p-type layers. In addition, from the negative flat-band voltage shift in figure 2(a), it is observed that the silicon–oxygen SL introduces positive charges in the silicon depletion region, compared with the silicon epi references (0 SL). FGA removes or passivates a major fraction of these positive charges, as can be discerned from figure 2(b). As indicated in figure 2(a), a bias pulse from deep depletion to accumulation is typically applied to fill the traps with holes during the DLTS measurements. The more negative the pulse voltage V_P, the stronger the accumulation and the higher the contribution of interface states at the Si/SiO_2 interface to the DLT-spectra [24], while the contribution of the SL states will be more prominent for a lower value of V_P. The bias pulse is applied for a time t_p, which is normally sufficiently long to saturate all the deep level centers in the probed region, unless otherwise specified. The doping density N_A of the p-type substrates is $1 \times 10^{15}\ cm^{-3}$.

3. Results

From the RT isothermal spectra of figure 3(a) for the reference silicon epi samples once can discern the presence of a

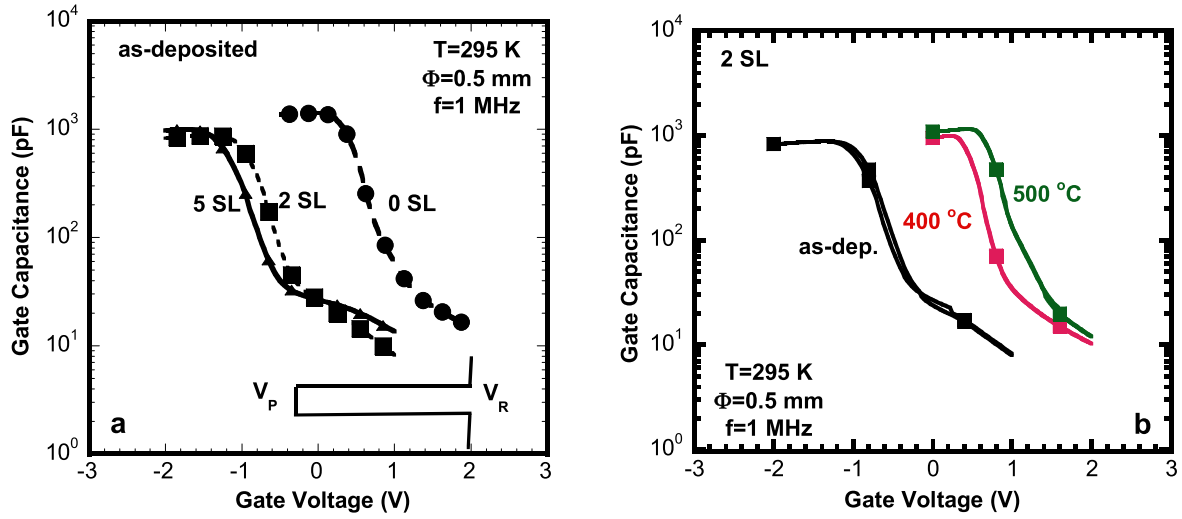

Figure 2. *C–V* characteristic at 1 MHz and room temperature for (a) the as-deposited samples with 0 (silicon epi reference), two and five SL periods and (b) for two-period SL capacitors as-deposited and after 5 min annealing in forming gas at 400 °C or 500 °C.

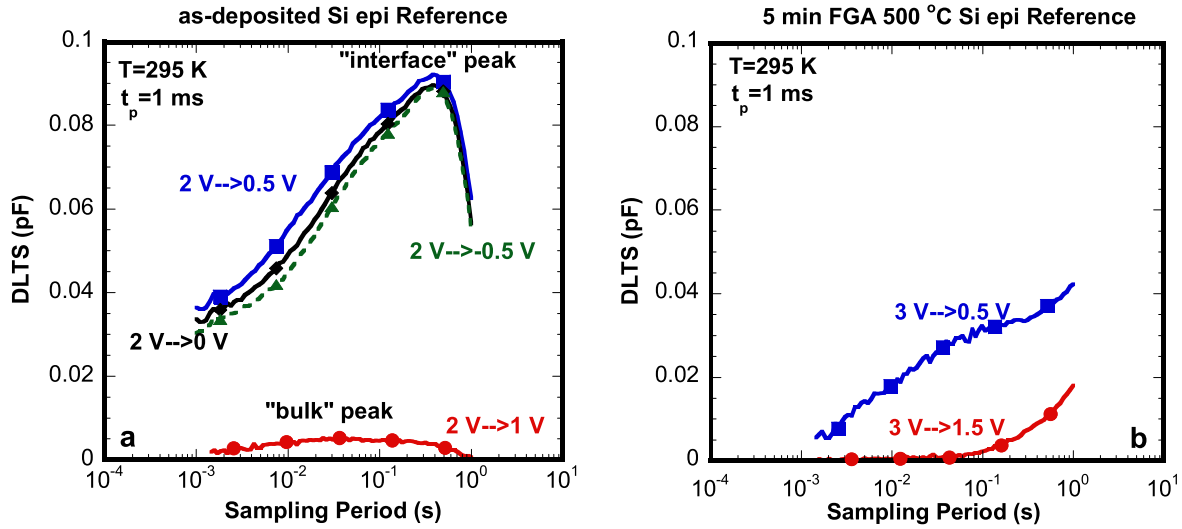

Figure 3. Frequency scan DLTS at room temperature and for different bias pulses, corresponding with (a) a silicon epi reference capacitor as-deposited and (b) a silicon reference after 5 min FGA at 500 °C. A filling pulse duration t_p of 1 ms was used.

rather broad peak, with increasing amplitude for more negative V_P. This indicates that when pulsing more into accumulation, more traps are filled, which are mainly associated with states at the Si/SiO_2 interface. On the other hand, only a small 'bulk' or depletion layer peak is observable for the 2 V–>1 V pulse, indicating a low defect density in the silicon epi layer, deposited at 500 °C. After a FGA at 500 °C for 5 min, a pronounced reduction of the DLTS peak height is observed, indicating a significant reduction of the trap density, both in the silicon epi layer and at its interface with the gate stack (figure 3(b)). This indicates a passivation of the respective deep levels by reaction with atomic hydrogen or annealing under the applied thermal budget.

According to figure 4(a), as-deposited five period SL capacitors exhibit rather similar behavior compared with the reference samples, albeit with a roughly six times higher amplitude, i.e., trap concentration. Again, a lower trap density is found in the depletion region for a small bias pulse (+1 V–> +0.5 V), while a much higher trap density is found near the interface, comprising both the defects associated with the Si–O SL and with the Si/SiO_2 interface. It explains the slight shift in peak position, i.e., in activation energy of the underlying deep-level band of states. Assuming that the Si/SiO_2 quality is similar for the reference and the SL capacitors, the increase in deep-level density can be ascribed to the presence of the 5 ALs of oxygen. However, as will be shown below, an increase of the dangling bond density at the Si/SiO_2 interface has been observed as well, possibly owing to a lower quality of the final silicon layer on top of the SL. Again, FGA at 500 °C yields about a factor two reduction of the peak height in figure 4(b). Similar results have been found for the 2 period SL capacitors at room temperature.

Temperature scan (T-scan) DLTS for the reference samples confirms largely the picture of the frequency-scan data: the reference samples give rise to a low trap density in the 75–300 K range (figure 5(a)), especially in the epi layer

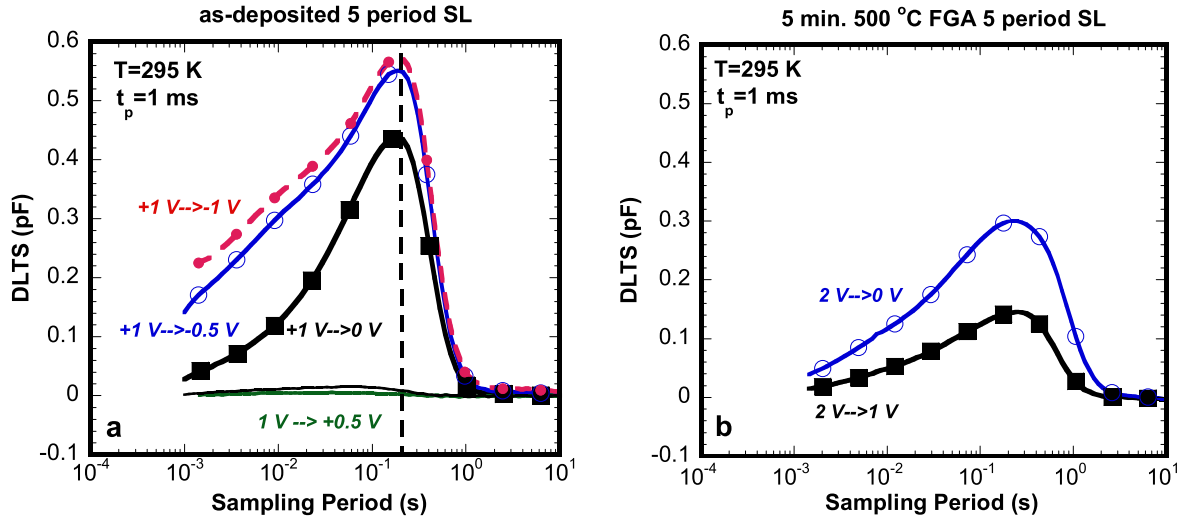

Figure 4. Frequency scan DLTS at room temperature and for different bias pulses, corresponding with (a) a 5 period SL capacitor as-deposited and (b) a 5 period SL sample after 5 min FGA at 500 °C. A filling pulse duration t_p of 1 ms was used.

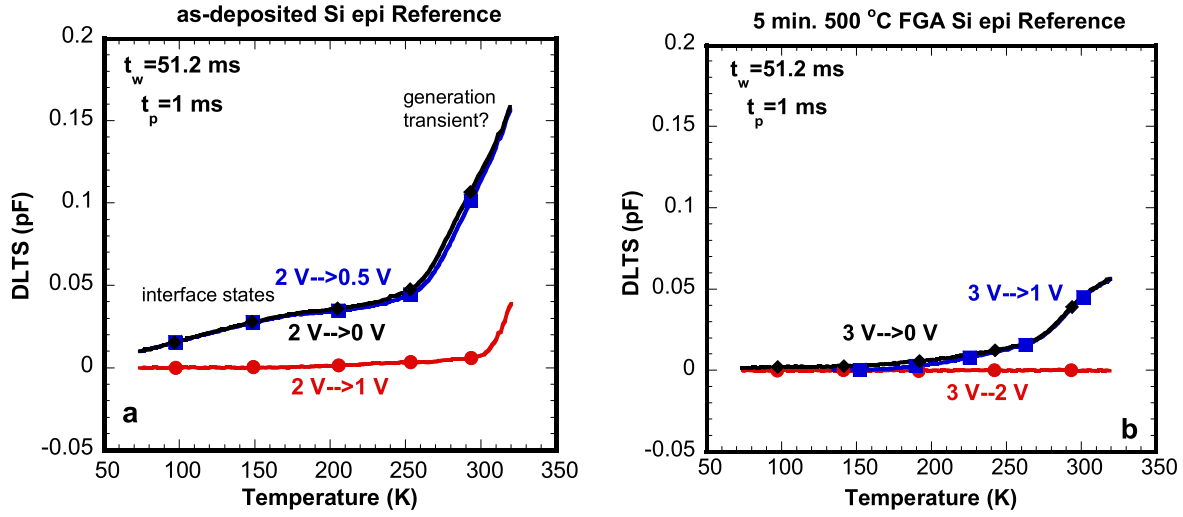

Figure 5. Temperature scan DLTS at $t_w = 51.2$ ms and for different bias pulses, corresponding with (a) a reference silicon epi capacitor as-deposited and (b) a reference silicon epi sample after 5 min FGA at 500 °C. A filling pulse duration t_p of 1 ms was used.

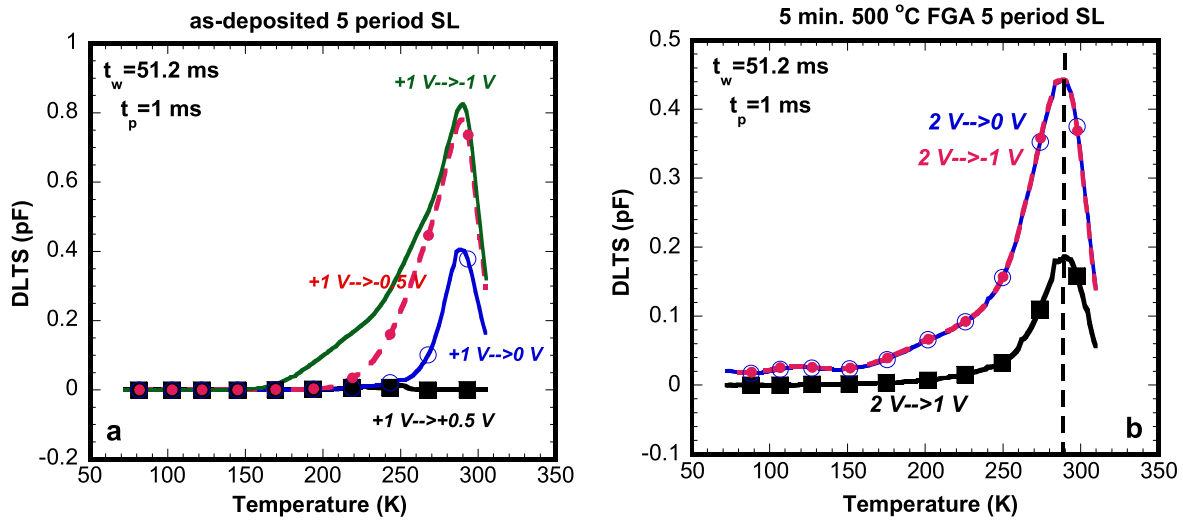

Figure 6. Temperature scan DLTS at $t_w = 51.2$ ms and for different bias pulses, corresponding with (a) a 5 period SL capacitor as-deposited and (b) a 5 period SL sample after 5 min FGA at 500 °C. A filling pulse duration t_p of 1 ms was used.

(2 V to V pulse). The signals become even smaller after a 500 °C FGA in figure 5(b). In the case of the 5 period SL, a pronounced broad peak is found in figure 6(a) close to room temperature and for a pulse towards accumulation. Its position is unaffected by the pulse bias V_P but the amplitude at the low-temperature flank of the peak increases, indicating the contribution of shallower states, probably at the Si/SiO_2 interface [24]. FGA yields a reduction of the DLTS peak amplitude roughly by a factor two (figure 6(b)). In addition, for the 2 V to 0 V or 2 V to −1 V spectra, a small peak around 125 K is noted in figure 6(b). At the same time, both before and after FGA, a low-temperature shoulder is present in the spectra, which occurs at the position of the silicon dangling bond or P_b donor centers, usually observed at the p-Si/SiO_2 interface [16–22]. It is rather unexpected that the P_b centers still show up after a FGA treatment at 500 °C, as it is known that such a treatment can reduce the P_b density below the detection limit of standard interface-state characterization methods.

An Arrhenius analysis of the T-scan peaks yields the activation energy (E_T) and hole capture cross section (σ_p) of table 1. One can observe that the average E_T reduces after FGA in the 5 SL case, while at the same time, also the σ_p reduces. This indicates that the deeper states can be more easily passivated or annealed, suggesting either a position closer to the interface or a different defect structure, e.g., associated with a different Si–O bonding configuration. The rather small values for the hole capture cross section indicate a neutral or even repulsive state for the empty deep levels, i.e., they correspond with deep donors near the middle of the silicon band gap.

4. Discussion

Summarizing the main observations, it has been shown that the presence of a Si–O SL introduces an additional band of hole-trap states in p-type silicon, with a peak position close to RT in the spectra and an activation energy around mid-gap, which reduces after FGA. In order to quantify the DOS of the underlying deep levels, the sampling period (which is proportional with the hole emission time constant τ_0) or the temperature T is converted into an activation energy based on [22]:

$$E_T = E_{V,Si} + kTln\left(\sigma_p \times 3.33 \times 10^{21} T^2 \tau_0\right) \ (p\text{–Si}) \quad (1)$$

with k Boltzmann's constant and $E_{V,Si}$ the top of the silicon valence band. Note that in equation (1), the DOS in the silicon valence band N_V is used, based on the standard DOS effective mass. It is known that the presence of the oxygen SL layers changes the effective mass [8, 25], which yields a change in N_V, that, for the time being, is neglected. The correction is expected to be rather limited, given that N_V occurs in the logarithmic term of equation (1).

It is well-known that the Arrhenius plot results of table 1 yield an order-of-magnitude estimate of σ_p. In order to assess the hole capture cross section more directly, trap filling

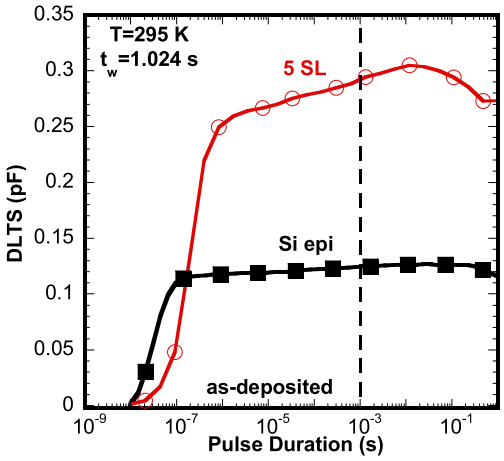

Figure 7. DLTS amplitude versus filling pulse duration for an as-deposited silicon epi and 5 period SL MOS capacitor at room temperature. The sampling period $t_w = 1.024$ s.

Table 1. Average activation energy and hole capture cross section derived from T-scan DLTS.

Sample	E_T (eV)	σ_p (cm^2)
as-grown 5 SL	0.589	2.9×10^{-16}
FGA 5SL	0.450	2.1×10^{-18}
FGA 2 SL	0.485	5.9×10^{-18}

measurements have been performed as a function of the bias pulse duration t_p. A typical result is shown in figure 7, where one can also discern that the standard t_p of 1 ms is indeed saturating the DLTS peak amplitude for the as-deposited Si epi and 5 period SL sample. From an exponential fit to the initial part of the curves in figure 7, a capture time constant of 4.1×10^{-8} s and 2.9×10^{-7} s has been derived for the reference and the 5 SL capacitor, respectively. Assuming a thermal velocity of 1×10^7 cm s^{-1} and a doping density of 1×10^{15} cm^{-3} would yield a σ_p of 2×10^{-15} cm^2 and 3.4×10^{-16} cm^2, respectively. However, as we are pulsing a MOS capacitor in accumulation, the relevant free hole density is the one at the interface, which can be orders of magnitude higher than the doping density. This means that the above values can be considered as an upper limit of the true σ_p. It appears that the Arrhenius plot value for the as-deposited 5 SL sample of table 1 is in fact close to the σ_p derived from the direct measurement in figure 7. Therefore, the data of table 1 have been substituted in equation (1) to convert the T- into an activation energy axis. The same has been applied for the frequency-scan spectra at room temperature.

Next, the equivalent surface DOS in a MOS capacitor can be derived from [22]:

$$D_T = \frac{\varepsilon_{Si} A C_{ins} N_{dop} \Delta C}{\beta k T C_R^3} \quad \left(\text{in } eV^{-1}\,cm^{-2}\right). \quad (2)$$

In equation (2), ε_{Si} is the permittivity of silicon $\sim 10^{-12}$ F cm^{-1}, A the area of the capacitor (1.9×10^{-3} cm^2), C_{ins} the oxide capacitance (2 nF). Finally, β is a semi-empirical peak width factor, estimated 2.5. C_R is

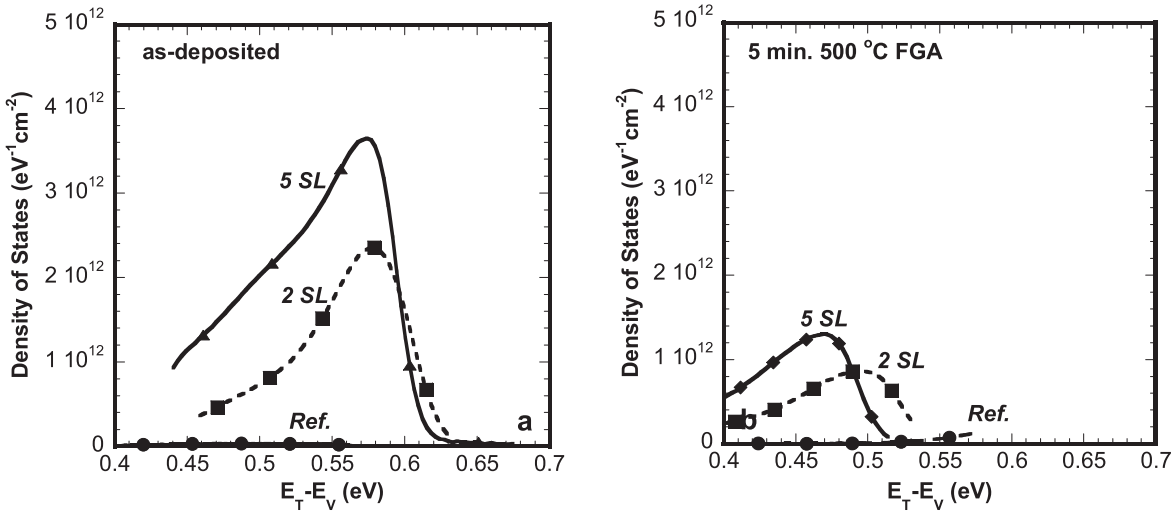

Figure 8. Density of states derived from the frequency-scan data at room temperature for the as-deposited (a) and FG-annealed samples (b).

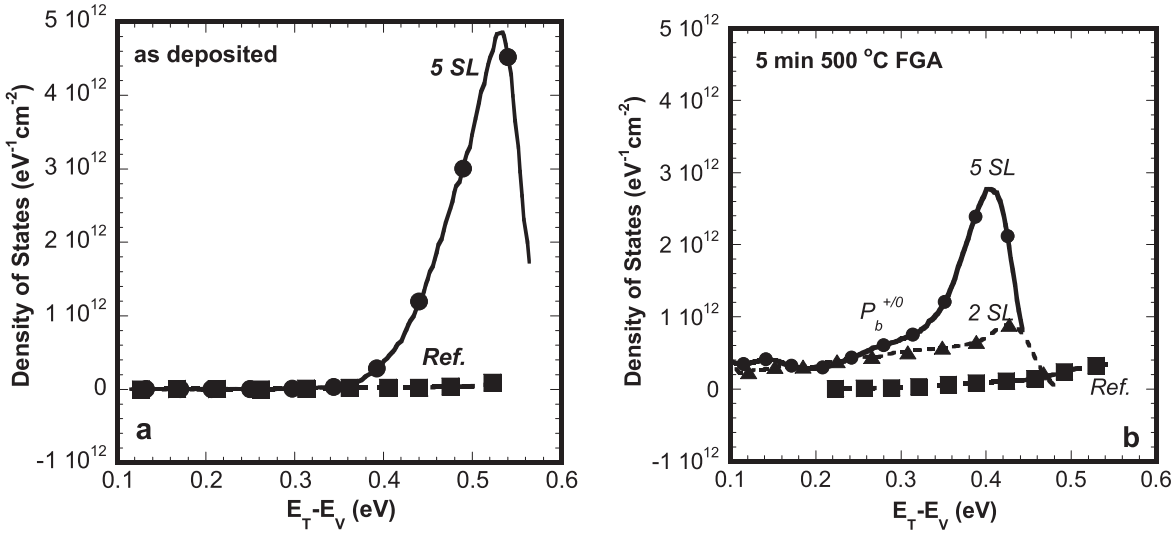

Figure 9. Density of states derived from the temperature scan data for the as-deposited (a) and FG-annealed samples (b).

Table 2. Maximum DOS and peak E_T derived from figures 8 and 9.

Sample	FGA	DOS_{max} (f-scan) (eV^{-1} cm^{-2})	E_T (f-scan) (eV)	DOS_{max} (T-scan) (eV^{-1} cm^{-2})	E_T (T-scan) (eV)
Si epi	no	3.4×10^{10}	0.485	n.a.	n.a.
2 SL	no	2.4×10^{12}	0.58	not meas.	not meas.
5 SL	no	3.7×10^{12}	0.57	4.9×10^{12}	0.53
Si epi	yes	n.a.	n.a.	n.a.	n.a.
2 SL	yes	8.7×10^{11}	0.49	8.9×10^{11}	0.43
5 SL	yes	1.3×10^{12}	0.47	2.8×10^{12}	0.40

the quiescent capacitance at V_R and ΔC is the capacitance transient amplitude, which is proportional with the vertical axis in figures 3–6. It is furthermore tacitly assumed that for the mid-gap states electron emission towards the conduction band can be neglected with respect to the hole emission. In other words, e_p should be much higher than e_n. In case $e_n \sim e_p$, the calculated DOS will be smaller than the true value by a factor $e_p/(e_n + e_p)$, which will be the more likely the closer E_T is to mid gap. Measurements on n-type silicon capacitors should clarify whether this is justified or not.

The outcome of this analysis is represented in figures 8 and 9, respectively based on the isothermal spectra or T-scan spectra. From figure 8, one can derive that the DOS in the first instance scales with the number of SL periods, i.e., a roughly 2.5 times higher value is obtained (see also table 2), while FGA reduces the maximum DOS by a factor 2 to 3. At the

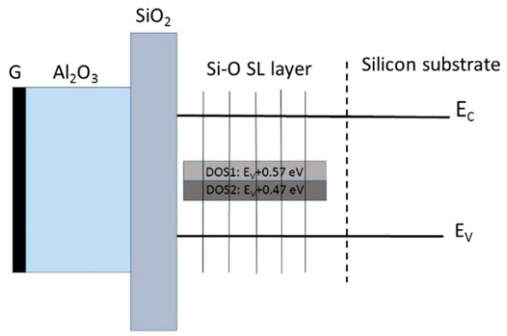

Figure 10. Schematic representation of a silicon MOS capacitor containing a 5 period Si—O SL at flat band voltage. Also indicated is the DOS of the two bands of deep levels derived from DLTS and centered at about $E_V + 0.57$ eV for the as-deposited sample and $E_V + 0.47$ eV after FGA. At the position of the oxygen atomic layers, indicated by the five vertical lines, a potential barrier is present according to the model of Xu *et al* [8].

same time, the peak energy position shifts slightly to lower values, in agreement with the Arrhenius data of table 1. The T-scan data of figure 9 consistently show a slightly higher DOS and a lower peak energy position (table 2). The latter fact could point to some T-dependence of the hole capture cross section, as the σ_p values in table 1 correspond with the peak maximum temperatures in figure 6 and not with room temperature. In fact, when comparing the as-deposited DOS with the one after FGA in figures 8(a) and (b), it is tempting to concluded that the spectra are composed of two peaks, with one contribution at higher activation energy being completely removed by the FGA and the less deep peak around 0.45–0.5 eV (figure 8(b)) surviving largely the annealing treatment. This could point to two different defect centers associated with the Si–O SLs. Finally, figure 10 represents schematically a band diagram at flat band for a MOS capacitor containing a SL layer. Also indicated is the estimated position of the two deep-level bands with corresponding DOS1 and DOS2, derived from DLTS.

The next question to answer is about the possible nature of the Si-O related defects. It is well-known that oxygen clustering occurs during heat treatments in the range of 450 °C typically employed here, giving rise to the so-called double thermal oxygen donors in n-type silicon [26–29]. While we cannot exclude their formation, these centers are not responsible for the observed Si–O SL peaks. As it can be expected that similar types of bonding configuration may exist at the Si/SiO_2 interface, it seems straightforward to compare with the corresponding DLT-spectra on p-type Si MOS capacitors. In fact, there exists a large similarity between the spectra of figures 3–6 and what has been reported in the literature for the Si/SiO_2 interface, where frequently a broad near mid-gap peak has been reported [20, 22]. This holds in fact also for the Si/Al_2O_3 interface, where the formation of a thin SiO_x interfacial layer can hardly be avoided [30]. The microscopic origin of this band of states remains obscure, however. In the past, several possible atomic configurations, based on possible Si–O bonds have been speculated on in the literature [4, 13], whereby recent Density Functional Theory calculations strongly support the presence of Si–O–Si bridges connecting reconstructed Si{100} surfaces [25].

Besides the dominant mid-gap peak, other deep levels are found as well: as shown in figure 6(a), clear evidence of the presence of P_b centers at the interface has been found. They give rise to the low-temperature shoulder of the main DLTS peak and are also present in the reference silicon epi spectra of figure 5, between 150 and 200 K. The corresponding concentration is roughly a factor 4 lower, indicating that additional P_b centers might be introduced by the Si–O ALs. The presence of P_b centers has been confirmed by Electron Paramagnetic Resonance on similar samples [32]. Comparing the FGA spectra with the ones for the as-deposited capacitors demonstrates that the P_b centers become passivated by atomic hydrogen, yielding a reduction of their DLTS signal.

The deep levels observed in the depletion region of the silicon epi references should be distinguished from those in the Si–O SL samples. Most DLTS studies in the past on silicon epi layers are concerned with as-deposited n-type silicon [32–34], while for p–Si, a band of states in the upper half of the bandgap at E_C-0.3 eV has been reported, corresponding with the Si–Si interface [35]. Here, a negligible density of traps is found for a pulse in depletion (e.g., the +2 V to +1 V spectrum in figure 5(a)), indicating the good quality of the pre-epi cleaning and the CVD processes. On the other hand, the up going trace around 300 K and above in for example figure 5 could be related to the inversion (or Zerbst) response of the MOS capacitor by minority carrier generation in the depletion region, which can also give rise to a kind of DLTS peak at temperatures typically above 300 K [36, 37].

5. Conclusions

The deep levels introduced by Si–O ALs in p-type silicon epitaxial layers have been studied by DLTS. It is shown that at least two types of defects have been created: first, a broad distribution of donor-like hole traps, with a DOS which roughly scales with the number of SL periods and an activation energy around mid-gap. Second, dangling bonds are created at the Si/SiO_2 interface, as evidenced by the $E_V + 0.3$ eV donor states. FGA at 500 °C reduces these defects significantly, whereby the nominal activation energy and hole capture cross section for the dominant band of states become smaller. The presence of such a high density of electrically active states is expected to negatively affect the electrical properties (carrier lifetime; mobility;…) of devices fabricated in these SL layers. While post-deposition FGA improves the 'electrical' layer quality, further process optimization is required to arrive at a similar high quality as the silicon epi reference layers.

Acknowledgments

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