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# Photodiode with Low Dark Current Built in Silicon-on-Insulator Using Electrostatic Doping

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**Abstract** – In this paper, we demonstrate experimentally a novel SOI-based photodiode using electrostatic doping and fabricated in a simple, low-cost process. Unlike a conventional ion-implanted *pn* junction diode, the electrostatically doped devices feature extremely low reverse-bias current. When used for photodetection, our devices exhibit a dark current three decades lower than a conventional photodiode and provide excellent detectivity even under low optical power density. Our electrostatically-doped diodes also feature enhanced response in the near-UV and 1/*f* low-frequency noise.

*Keywords:* silicon on insulator; photodiode; electrostatic doping; ultraviolet detection

**Introduction**

Compared with traditional bulk silicon, silicon-on-insulator (SOI) substrates confer a number of advantages, including low leakage currents, reduced capacitance, low power consumption, better immunity against short channel effects (SCEs), and superior scaling capability [1-4]. This makes SOI substrates not only suitable for conventional MOSFETs, but also attractive for novel semiconductor devices, such as TFETs and $Z^2$-FETs due to natural substrate isolation [5-8] and simpler multi-gate designs. Furthermore, photodetectors (PDs) built on the SOI platform also show excellent optoelectronic performance. The advantages of high working speed, high radiation resistance and low parasitic capacitance make the SOI-based PDs very competitive in many applications, such as the electronic and photonic integrated circuits (EPICs), optical communication systems and aerospace [9-16].

In order to form a *pn* photodiode in the SOI film, conventional ion implantation is typically used to dope the Si channel [17]. However, the ion implantation can cause damage and degrade the quality of the Si, a problem that is especially severe in ultra-thin SOI films that lack seed layer to facilitate recrystallization. Further, the high- temperature annealing used to activate the dopants may cause stress and damage, and further degrade the performance of the device. To overcome these disadvantages, electrostatic doping [18, 19] induced by electric field can be used to form the *pn* junction and avoid ion implantation entirely. Previously, we have shown that the field-induced diode formed in the SOI substrate has similar band-diagram and photodetection properties as standard *pn* junction diodes [20]. Also, reconfigurable field-induced *pn* junctions controlled by top- and bottom-gate have been formed in the top Si channel of a $Z^2$-FET device (the Hocus-Pocus diode [21]) and used for carrier lifetime extraction.

In this work, we demonstrate a novel photodiode formed in the top Si film of SOI by electrostatic doping. To retain high quality top Si film, the device uses Schottky source/drain contacts and is free of any implantation and high-temperature annealing steps. With appropriate bias on the top and bottom gates, the device behaves as a standard *pn* diode with a high rectification ratio. Thanks to its extremely low dark current, 3 decades lower than a conventionally doped Si *pn* diode, our electrostatically doped PD shows excellent

photodetection performance under low-intensity illumination in the visible and UV spectral ranges. The response spectrum, response speed, and interesting low-frequency noise properties of our device are also presented.

**Device structure and fabrication**

Figure 1(a) schematically shows a simplified fabrication process flow of our device based on a SOI substrate with undoped 100 nm thick top silicon ($T_{Si}$) and 145 nm thick buried oxide (BOX). Mesa isolation of devices is achieved by photolithography and wet etching in diluted tetramethylammonium hydroxide (TMAH). Then, thermal evaporation is employed to deposit the 10/80 nm Cr/Au metal stack in source and drain regions, forming Schottky S/D contacts. After that, an $Al_2O_3$ layer of 30 nm thickness is deposited as the gate dielectric via atomic layer deposition (ALD). This is followed by the gate electrode formation using lithography, metal deposition and lift-off. No ion implantation is used throughout the process, and only a low-temperature anneal (300 °C) serves to improve the Schottky contacts.

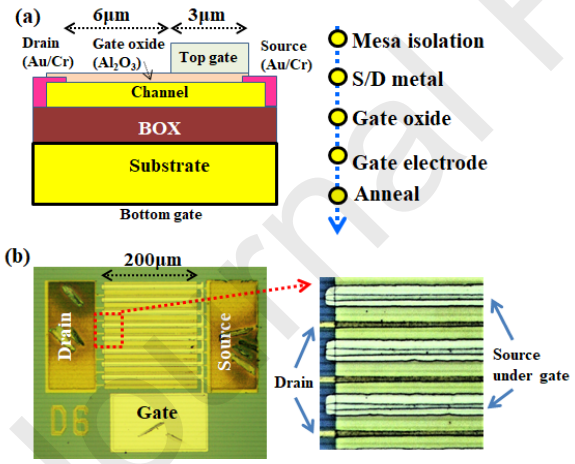


Fig. 1. (a) Schematic view and simplified fabrication process flow of the device. (b) Top-down optical view of the fabricated device.

Figure 1(b) shows the top-down structure of the fabricated device, in which the top gate is 3 μm long and overlaps the source, but leaves a 6 μm long gap between the gate and drain. In order to increase the diode current, the fabricated device has interdigitated source/drain

electrodes with 16 gate fingers, increasing the effective gate width while maintaining a compact 200×200 μm active area.

**Electrical characterization**

Figure 2(a) shows the $I_D$-$V_D$ characteristics of the fabricated device under a fixed back-gate voltage ($V_{BG}$ = –2 V) as a function of top gate bias $V_G$. When $V_G$ = –4 V, the channel becomes fully *p*-type because of the negative top and bottom gate voltages, as shown in Fig. 2(b), leading to nearly symmetrical resistor-like $I_D$-$V_D$ curves. On the other hand, when $V_G$ = 4 V, the device works like a standard *pn* diode with a ~$10^8$ rectification between forward and reverse current. Essentially, there is an electrostatically doped *pn* junction in the channel formed by the two gates, as illustrated in Fig. 2(c). The *n*-type region is created under the front gate because of the large positive $V_G$, whereas the uncovered part of channel remains *p*-type due to the negative $V_{BG}$. It should be highlighted that the reverse current of the device is dramatically reduced from 1 mA to 1 pA as $V_G$ increases from –4 V to 4 V, under a fixed $V_D$ = –1 V. This corresponds to a dark current density of 2.5 nA/cm$^2$, which is 3 decades lower than that reported in ion-implanted SOI photodiodes [22]. We attribute this low dark current to the undamaged Si layer that does not see any ion implantation or high-temperature anneals in our process.

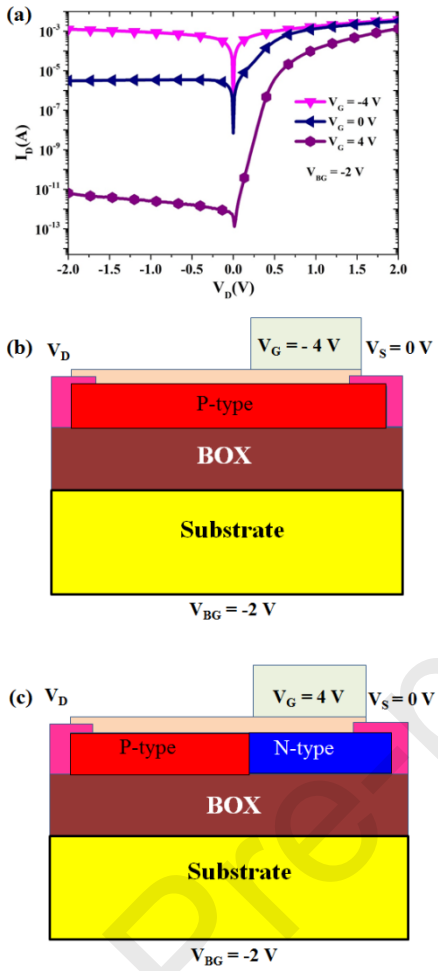


Fig. 2. (a) $I_D$-$V_D$ characteristics of the fabricated device operated with constant $V_{BG}$ = –2 V for $V_G$ = –4, 0, and 4 V. Schematic views of device operated as a resistor (b) when $V_G$ = –4 V and as a *pn* junction diode (c) when $V_G$ = 4 V.

In addition, the $I_D$-$V_D$ characteristics as a function of $V_{BG}$ were measured at a fixed top gate bias of $V_G$ = 4 V. The results shown in Fig. 3(a) correspond to backgate $V_{BG}$ = –20, –2, and 20 V. Again, for $V_{BG}$ = –20 V, the device behaves like a resistor with symmetrical output characteristics, as the large negative $V_{BG}$ overcomes the smaller positive $V_G$ and makes the entire channel *p*-type, as illustrated in Fig. 3(b). Similarly, for large positive $V_{BG}$ = 20 V the channel becomes completely *n*-type, as shown schematically in Fig. 3(c), leading to symmetrical resistor-like $I_D$-$V_D$ curves without rectification.

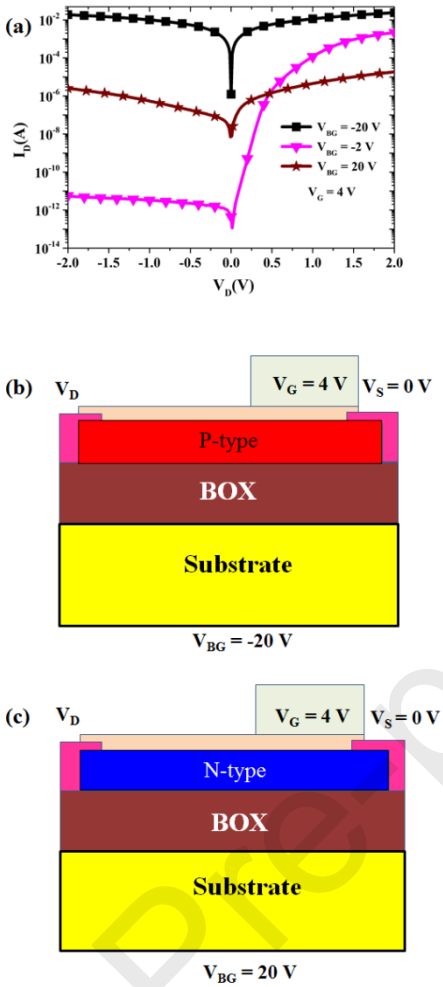


Fig. 3. (a) $I_D$-$V_D$ characteristics of the fabricated device *vs.* backgate bias $V_{BG}$ at fixed $V_G$ = 4 V. Schematic views of device when (b) $V_{BG}$ = –20 V and (c) $V_{BG}$ = 20 V.

It is worth noting that the current of the *n*-type resistor is much lower than that of the *p*-type resistor because the workfunction of Cr/Au is close to the valence band of silicon, leading to better contacts to *p*-type material [13]. But for an intermediate $V_{BG}$ = –2 V bias, a high-rectification *pn* diode curve is recovered, demonstrating that diode-like characteristics can be controllably obtained using appropriate $V_{BG}$ and $V_G$ biasing.

In a photodetector, a low dark current is helpful to improve the signal/noise ratio, so the extremely low dark current in our device is attractive for PD applications. In the experiment, we assume that the light beams shooting on the surface of the device are completely uniform, due to the diameter of the light spot is much larger than the device scale. Figure 4(a) shows the output characteristics of the fabricated device under illumination with $\lambda$ = 520 nm light as a function of optical power density ranging from 10 to 1000 $\mu W/cm^2$ . The reverse current rises

significantly with optical power density. As in a conventional photodiode, the open-circuit voltage ($V_D$ when $I_D = 0$) shifts towards positive $V_D$ values in proportion to the optical power density. Thanks to the low dark current, even low-intensity illumation of 10 μW/cm$^2$ can produce a measurable photocurrent that is almost an order of magnitude higher than the dark current.

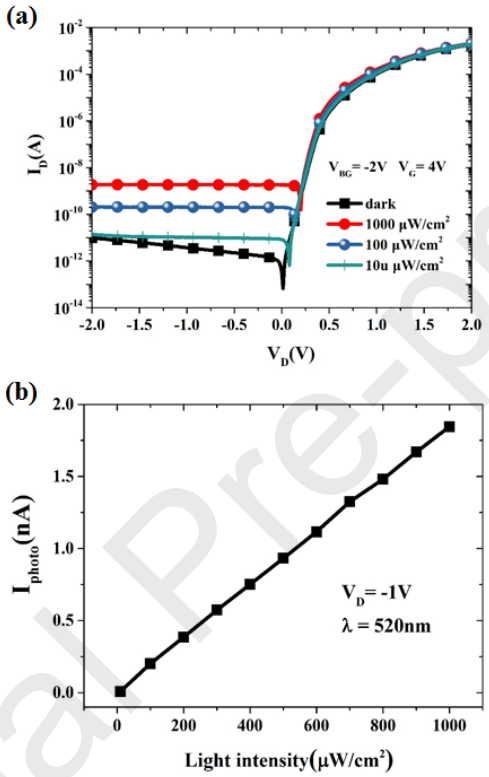


Fig. 4. (a) $I_D$-$V_D$ characteristics of the device under λ = 520 nm illumination as a function of intensity in the 10–1000 μW/cm$^2$ range. (b) Photocurrent *vs.* illumination intensity at $V_D$ = –1 V (λ = 520 nm).

The relationship between photocurrent and optical power density is presented in Fig. 4(b) at a constant $V_D$ = –1 V. As the optical power density increases from 0 to 1000 μW/cm$^2$ with a step of 100 μW/cm$^2$, the photocurrent at $V_D$ = –1 V increases to 1.8 nA with very good linearity. The responsivity of the device extracted from the slope in Fig. 4(b) reaches 8.5 mA/W, equivalent to a quantum efficiency of 2.1%. This low value of quantum efficiency is due to the relatively weak absorption by the thin Si channel layer ($T_{Si}$ = 100 nm) of λ = 520 nm light.

The dependence of the diode responsivity on the wavelength of the light is shown in the output characteristics in Fig. 5(a). As the wavelength decreases from 900 nm to 300 nm under a fixed intensity of 100 μW/cm$^2$, the photocurrent increases dramatically. The spectral responsivity *R* (*i.e.* the ratio of photocurrent and optical power) of the device as a function of wavelength in the 300–1000 nm range at a constant intensity of 100 μW/cm$^2$ and a fixed $V_D$ = –1 V is summarized in Fig. 5(b). Different from the results shown in previous work, the electrode areas including source, drain and gate which are not transparent are taken into account at this work, thus the same photocurrent corresponds to the smaller optical area, that's why the calculated responsivity R becomes higher than before. Unlike a conventional Si photodiode built in a bulk Si substrate, our device shows an enhanced responsivity in the near UV, increasing by a factor of ~3 as λ is decreased from 500 to 400 nm. This enhanced UV response is explained by the higher absorption of shorter wavelengths in the thin Si channel and might find many applications [12, 23]. Note that the little bump at λ = 700 nm in Fig. 5(b) is probably due to the light interference in the SOI film stack, which was also observed in our previous study [20].

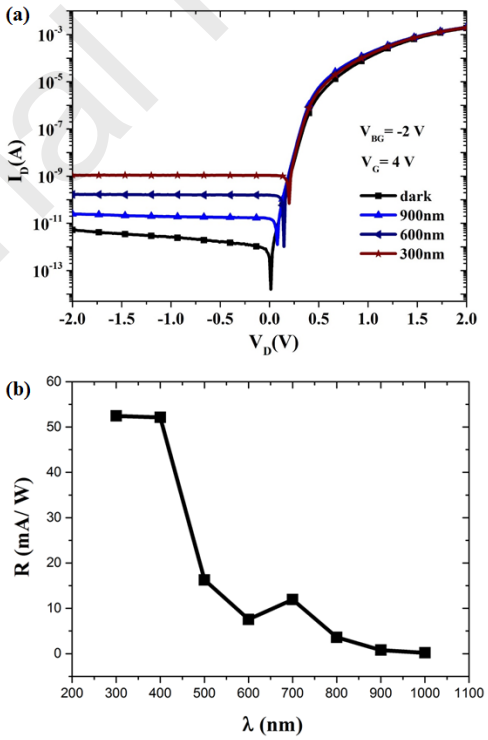

Fig. 5. (a) $I_D$-$V_D$ characteristics of the device under fixed illumination intensity of 100 μW/cm$^2$ at wavelengths λ = 300, 600, and 900 nm. (b) Responsivity *vs.* wavelength in the λ = 300–1000 nm range, at a fixed reverse bias of $V_D$ = –1 V and optical power density of 100 μW/cm$^2$.

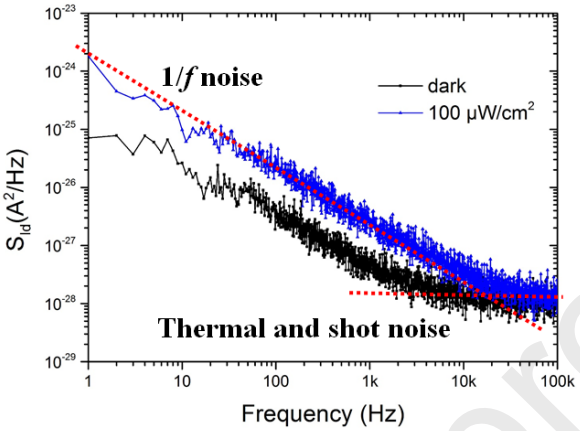


Figure 6. The low-frequency noise power spectrum in the dark and under constant 100 μW/cm$^2$ illumination (measured at $V_G$ = 4 V, $V_{BG}$ = –2 V and $V_D$ = –1 V).

The low-frequency noise properties of our device are also characterized and shown in Figure 6. Above 10 kHz, a white noise spectrum is observed, which we attribute to the usual combination of thermal and shot noise as in conventional pn photodiodes [24-27]. However, below ~10 kHz, we observe a 1/*f* noise spectrum with a nearly fixed slope, which is different from the flat white noise spectrum observed in conventional photodiodes at all frequencies. Under λ = 520 nm illumination at 100 μW/cm$^2$ the noise increases slightly compared to the dark, but retains the same 1/*f* slope. Since the junction is induced by the top and bottom gates through the gate oxide, the trapping and detrapping events in the interfaces between Si channel and the front gate oxide/BOX cause fluctuations in $I_D$ and thereby induce 1/*f* noise, as in a conventional MOSFET [28].

## Conclusions

We have demonstrated a novel SOI- based photodiode where the *pn* junction is created using electric fields produced by the top and bottom gates. Free of any implantation damage,

the electrostatically- induced diode has extremely low dark current, down to 2.5 nA/cm$^2$, some three orders of magnitude lower than conventional implanted diodes in SOI substrates. The device shows similar optical response to a conventional doped photodiode, with excellent photodetection of low-intensity illumination in the visible and near-UV. The relation between optical power density and output photocurrent shows good linearity. The device also has enhanced response in the near-UV, which might find applications in UV-selective detection. The low-frequency noise measurement on the device reveals a 1/*f* noise spectrum, which we attribute to interface trapping as in a MOSFET. Finally, our device can be switched between photodiode mode and resistor mode by applying appropriate top and bottom gate biasing. This unique feature can be potentially used for selective access in a photodetector array.

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