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The role of interface states and series resistance on the I–V and C–V characteristics in Al/SnO_2/p-Si Schottky diodes

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Abstract

In order to good interpret the experimentally observed non-ideal Al/SnO_2/p-Si (MIS) Schottky diode parameters such as the barrier height Φ_B, series resistance R_s and density of interface states N_{ss}, a calculation method has been reported by taking into account interfacial oxide layer and ideality factor n in the current transport mechanism. The current–voltage (I–V) and capacitance–voltage (C–V) characteristics of MIS diodes are studied over a wide temperature range of 80–350 K. The effects of R_s, interfacial layer and N_{ss} on I–V and C–V characteristics are investigated. The values of n were strongly temperature dependent and decreased with increasing temperature. The energy distribution of N_{ss} was determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height. The mean N_{ss} estimated from I–V and C–V measurements decreased with increasing temperature. The R_s estimated from Cheung's functions was strongly temperature dependent and decreased with increasing temperature. The I–V characteristics confirmed that the distribution of N_{ss}, R_s and interfacial layer are important parameters that influence the electrical characteristics of MIS devices.

Keywords: MIS structure; Insulating layer; Series resistance; Density of interface states

1. Introduction

Metal–insulator–semiconductor (MIS) type Schottky diodes have attracted much interested in the last few years. They are important research tools in the characterization of new semiconductor materials and at the same time the fabrication of these structures play a crucial role in constructing some useful devices in technology. The performance and reliability of a Schottky diode is drastically influenced by the interface quality between the deposited material and the semiconductor surface. Due to the technical importance of MIS Schottky barrier diodes, these devices have been studied extensively but satisfactory understanding in all details has still not been achieved. Especially the formation and characterization of SnO_2 insulator layers on Si still remains a basic problem. Until now, the literature has contained several reports on the current transport mechanism of tunnel MIS diodes and solar cells [1–18].

In practical, there are several possible sources of error, which cause deviations of the ideal behavior and must be taken into account. These include the effects of insulating layer between metal and semiconductor, density of interface states N_{ss} and series resistance R_s. The series resistance is an important parameter, which causes the electrical characteristics of MIS diodes to be non-ideal [1,11,19–21]. Usually, the forward bias current voltage (I–V) characteristics are linear in the semilogarithmic scale at low voltages but deviate considerably from linearity due to the effect of parameters such as the R_s and the N_{ss} when the applied voltage is sufficiently large [1,11,19–23]. The parameter R_s is only effective in the curvature downward region of the forward I–V

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characteristics, but the other parameter is effective in both the linear and non-linear regions of these characteristics, accompanying a change of the Schottky barrier height [20,21]. Especially the series resistance and interfacial oxide layer (SnO_2) have strong influences on the forward I–V and C–V characteristics. An efficient technique to determine R_s, n and Φ_B has been proposed by Cheung and Cheung [24]. This technique has been applied to Al/SnO_2/p-Si diodes and the values of R_s, Φ_B and ideality factor n calculated as a function of temperature from 80 to 350 K.

In this study, we have reported a modification which is includes the ideality factor n and tunneling parameter $a\chi^{1/2}\delta$ in the expression of reverse saturation current I_0. In order to extract the values of the real R_s, Φ_B and n of Al/SnO_2/p-Si (MIS) diodes, Cheung's method [24] has been applied in the temperature range of 80–350 K. The other purpose of this paper is to present the results of a systematic investigation of the role of N_{ss} and R_s on the I–V and C–V characteristics of Al/SnO_2/p-Si (MIS) Schottky diodes over the temperature range 80–350 K. Furthermore, it is also to characterize the interface states in Al/SnO_2/p-Si (MIS) Schottky diodes and determine the energy density distribution of the interface states.

2. Experimental

The semiconductor substrates used were p-type B-doped Si single crystals, with a (1 0 0) surface orientation, 300 μm thick and 8 Ω cm resistivity. The Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of resistivity of 18 MΩ cm. Immediately after surface cleaning, high purity aluminum (Al) metal (99.999%) with a thickness of 2500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of 1×10^{-6} Torr. Sintering the evaporated Al back contact was formed the ohmic contact under vacuum. Immediately after ohmic contact, a thin layer of SnO_2 was grown on the p-Si substrate by spraying a solution consisting of 32.21 wt.% of ethyl alcohol (C_2H_5OH), 40.35 wt.% of deionized water (H_2O) and 27.44 wt.% of stannic chloride ($SnCl_4\cdot5H_2O$) on the substrate, which was maintained at a constant temperature of 400 °C. The temperature of the substrates was monitored by chromel–alumel thermocouple fixed on top surface of the substrate. The variation of the substrate temperature during spray was maintained within ±2 °C with the help of a temperature controller. The rate of spraying was kept at about 30 cc/min by controlling the carrier gas flowmeter. N_2 was used as the carrier gas. SnO_2 dots were 4 mm in diameter. After spraying process, circular dots of 2 mm in diameter and 2500 Å thick aluminum rectifying contacts were deposited onto the SnO_2 surface of the wafer through a metal shadow mask in liquid nitrogen trapped oil-free ultra-high vacuum system in the pressure of 1×10^{-6} Torr. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The deposition rates were about 1–3 Å/s. The interfacial oxide layer thickness was estimated to be about 28 Å from measurement of the oxide capacitance in the accumulation.

The I–V measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. The C–V and G–V measurements were performed at 500 kHz by using HP 4192A LF impedance analyzer (5 Hz–13 MHz). The I–V and C–V characteristics of the Al/SnO_2/p-Si Schottky diode were studied in the temperature range of 80–350 K by using temperature controlled Janes 475 cryostat.

3. Results and discussion

3.1. Effects of series resistance and interface states on I–V/T characteristics

For a Schottky diode with a uniform thin oxide layer, it is assumed that the relation between the applied forward bias and current of the device is due to thermionic emission current and it can be written as [11]

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{1}$$

where n is the ideality factor, I_0 is the saturation current and defined by

$$I_0 = AA^*T^2\exp\left[-\frac{q\Phi_{B0}}{kT}\right] \tag{2}$$

where the quantities A, A^*, T, q, k and Φ_{B0} are the diode area, the effective Richardson constant, temperature in Kelvin, the electronic charge, Boltzmann's constant and the apparent barrier height. The semilog-forward bias I–V plots of the Al/SnO_2/p-Si Schottky diodes in the temperature range of 80–350 K are shown in Fig. 1. The I_0 was obtained by extrapolating the linear region of the curve to zero applied voltage and the Φ_{B0} values were calculated from Eq. (2). The values of ideality factor n were obtained from the slope of linear region of I–V plots. The change in n and Φ_{B0} with temperature is seen in Table 1. As shown in Table 1, the Φ_{B0} and n determined from semilog-forward I–V plots were found to be a strong function of temperature. The ideality factor n was found to increase, while the Φ_{B0} decrease (Fig. 4) with decreasing temperature ($n = 7$ and $\Phi_{B0} = 0.208$ eV at 80 K, $n = 2.6$ and $\Phi_{B0} = 0.640$ eV at 350 K). The

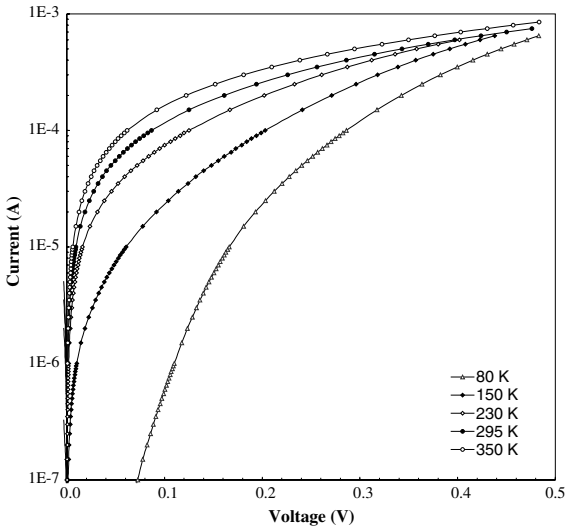

Fig. 1. Forward I–V characteristics of Al/SnO_2/p-Si at various temperatures.

values of the diode ideality factor n as obtained here indicate that the current transport mechanism consists of both the trap-assisted tunneling and the thermionic emission. Nagatomo et al. reported that the variation of the diode ideality factor corresponds to the performance of a SnO_2/Si heterojunction solar cell [25]. It is worth nothing that the product of n and temperature seems to remain constant in the temperature range investigated. On the basis of information available in the literature [25], the constant product means that the diode carrier transport should be dominated by trap-assisted tunneling at temperatures well below 300 K. Above 300 K, the thermionic emission of carriers at the heterojunction barrier should dominate the diode carrier transport and cause the diode ideality factor to approach unity. When a metal is evaporated on the semiconductor surface coated with an insulator layer, the metal and semiconductor do not make intimate contact because of interfacial layer. Electron tunneling traps localized in the interfacial layer close to the p-Si surface can cause Φ_{B0} to increase. The ideality factor n is not constant with temperature. Similar results have been reported in the literature [2,5,9,13,14,16]. The high values of the ideality factor at low temperatures are probably due to the potential drop in the interfacial layer, presence of excess current at low temperature region and the recombination current through the interfacial states of the junction [26].

The increase in ideality factor with decreasing temperature is known as T_0 effect [27]. Explanations of the possible origin of such case have been proposed taking into account the interface state density distribution [28,29], quantum mechanical tunneling [29,30] and image force lowering [30]. n was found to be inversely proportional with temperature (as shown in Fig. 2) as

$$n(T) = n_0 + \frac{T_0}{T} \tag{3}$$

where the n_0 and T_0 are constants which were found to be 1.44 and 450 K, respectively.

For the evaluation of the barrier height, one may also make use of the Richardson plot of the saturation current. Eq. (2) can be rewritten as

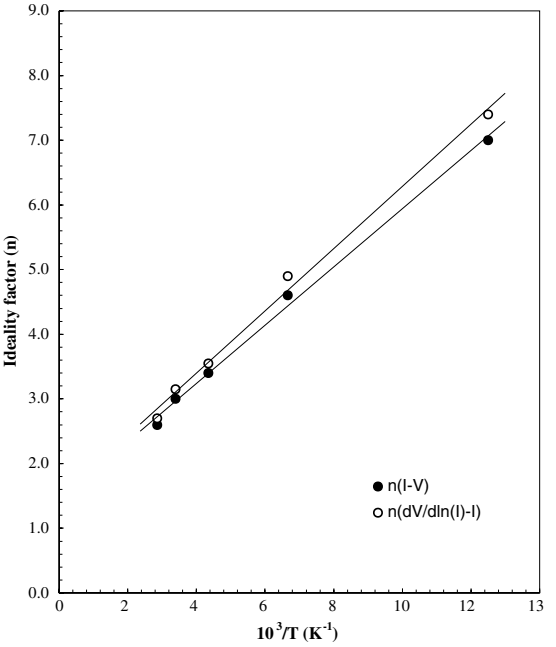

Fig. 2. Plots of n vs. $10^3/T$ of Al/SnO_2/p-Si (MIS) diode obtained from I–V and $\mathrm{d}(V)/\mathrm{d}\ln(I)$–$I$.

Table 1
Temperature dependent values of various parameters determined from I–V characteristics of Al/SnO_2/p-Si Schottky diode

T (K)	$n(I$–$V)$	$\Phi_{B0}(I$–$V)$ (eV)	$\Phi_B(H(I))$ (eV)	$\Phi_{Bf}(I$–$V)$ (eV)	$N_{ss}(I$–$V)$ ($\times 10^{13}$ eV^{-1} cm^{-2})	$n(\mathrm{d}V/\mathrm{d}\ln I)$	$R_s(\mathrm{d}V/\mathrm{d}\ln I)$ (Ω)	$R_s(H(I))$ (Ω)
80	7.0	0.208	0.192	0.804	8.29	7.40	460.64	462.95
150	4.6	0.303	0.293	0.792	4.97	4.90	401.64	415.98
230	3.4	0.439	0.415	0.738	3.31	3.55	277.50	290.33
295	3.0	0.558	0.512	0.719	2.76	3.15	160.36	166.89
350	2.6	0.640	0.622	0.681	2.20	2.70	50.19	77.94

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{q\Phi_{B0}}{kT} \quad (4)$$

The dependence of $\ln(I_0/T^2)$ vs. $1000/T$ is found to be non-linear in the temperature range measured; however, the dependence of $\ln(I_0/T^2)$ vs. $1000/nT$ gives a straight line (Fig. 3). The non-linearity of the conventional $\ln(I_0/T^2)$ vs. $1000/T$ is caused by the temperature dependence of the barrier height and ideality factor. Similar results have also been found by several authors [12,13,31]. This shows that the reverse saturation current I_0 can be described by

$$I_0 = AA^*T^2 \exp\left(-a\chi^{1/2}\delta\right) \exp\left(\frac{-q\Phi_{Bf}}{nkT}\right) \quad (5)$$

where A is the diode area, A^* is the effective Richardson constant, Φ_{Bf} is the flat-band barrier height, $a = (4\pi/h)(2m^*)^{1/2}$ is a constant that depends on the tunneling effective mass m^* and Planck's constant h, χ is the mean tunneling barrier presented by the interfacial layer. $a\chi^{1/2}\delta$ is the hole tunneling factor. Eq. (5) is valid only for forward biases $V > 3kT/q$ since the reverse current contribution (due to holes tunneling from the metal into the semiconductor) has been neglected. δ is the thickness of the interfacial layer in which holes move through tunnel. The interfacial layer thickness δ can be obtained for the MIS diode from high frequency C–V characteristics using the equation $C_i = \varepsilon_i\varepsilon_0 A/\delta$, where C_i is the capacitance of the interfacial oxide layer, $\varepsilon_i = 7\varepsilon_0$ [32] and ε_0 are the permittivities of the interfacial layer and free space. Thus, the interfacial layer thickness was calculated as 28 Å.

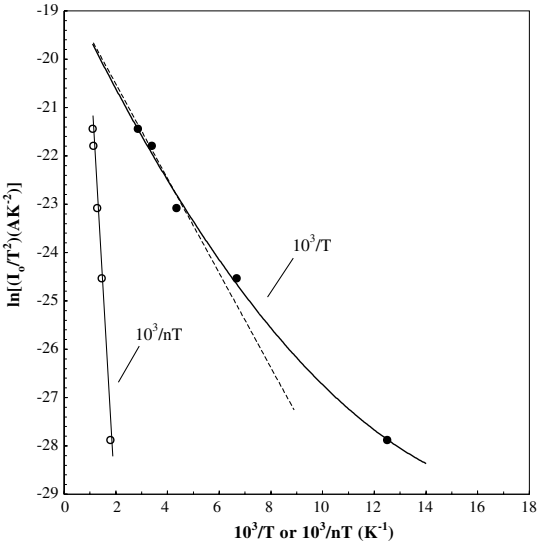

Fig. 3. Richardson plots of $\ln(I_0/T^2)$ vs. $10^3/T$ and $10^3/nT$ for Al/SnO_2/p-Si Schottky diodes.

The Richardson plot of $\ln(I_0/T^2)$ versus $1/nT$ giving a straight line is found as expected from

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - a\chi^{1/2}\delta - \frac{q\Phi_{Bf}}{nkT} \quad (6)$$

The tunneling factor can be obtained as 11.22 from the straight line extrapolated intercept on the $\ln(I_0/T^2)$ axis (Fig. 3). The mean tunneling barrier height is calculated as 0.580 eV taking the value of $a = 0.526$ eV$^{-1/2}$ Å^{-1} ($m^* = 1.51 \times 10^{-12}$ eV s^2 m^{-2} and $h = 4.135 \times 10^{-15}$ eV s). The value of χ is high and transmission for through the interfacial layer can be due to solely to simple tunneling.

Using the tunneling factor of 11.22 the temperature dependent barrier height Φ_{Bf} is obtained from Eq. (5) for each temperature and presented in Table 1. Φ_{Bf} is considered to be real fundamental quantity. The flat-band Φ_{Bf} is also shown in Fig. 4 as a function of the temperature. Φ_{Bf} is always larger than zero-bias barrier height Φ_{B0}. However, the flat-band barrier height Φ_{Bf} is obtained to increase with decreasing temperature in a manner similar to those reported by the others [31,33,34]. Furthermore, the temperature dependence of the flat-band barrier height can be described as

$$\Phi_{Bf}(T) = \Phi_{Bf}(T=0) + \alpha T \quad (7)$$

where $\Phi_{Bf}(T=0)$ is the flat-band barrier height extrapolated to zero temperature and α is the temperature coefficient of $\Phi_{Bf}(T)$. In Fig. 4, the fitting of the $\Phi_{Bf}(T)$ yields $\Phi_{Bf}(T=0) = 0.849$ eV and $\alpha = -4.64 \times 10^{-4}$ eV/K. We also found that the barrier height $\Phi_B(C$–$V)$ from C–V characteristics decreases linearly with the temperature (Fig. 4). In Fig. 4, the fitting of the $\Phi_B(C$–$V)$

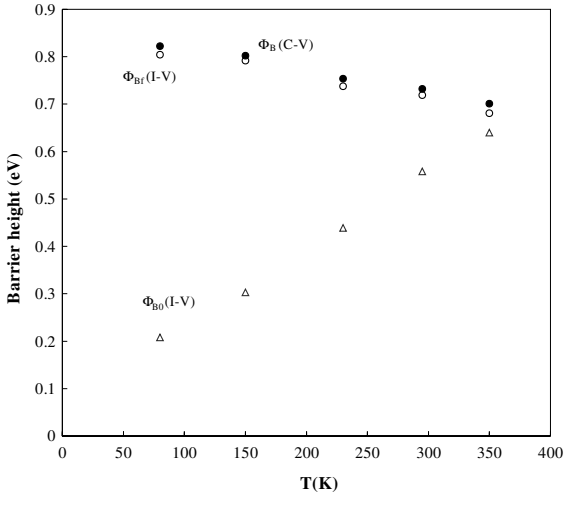

Fig. 4. Zero-bias barrier height $\Phi_B(I$–$V)$ (open triangles) and the effective barrier height $\Phi_{B0}(I$–$V)$ (open circles) from I–V data and the $\Phi_B(C$–$V)$ (filled circles) from C–V data as a function of the temperature.

yields $\Phi_B(C\text{–}V, T = 0) = 0.862$ eV and $\alpha = -4.55 \times 10^{-4}$ eV/K. These values of temperature coefficient of the barrier height were in very close agreement with the temperature coefficient of Si band-gap (-4.73×10^{-4} eV/K). At low temperatures, there should be minority carrier accumulation near the interface but at the Si side (i.e. electrons for p-type Si substrate). However, the phenomenon of the minority carrier accumulation is gradually forbidden if temperature is higher. So, the height of the Schottky barrier decreases with increasing temperature (Table 1).

Usually, the forward bias $I\text{–}V$ characteristics are linear on a semilogarithmic scale at low forward bias voltages but deviate considerably from linearity due to the effect of series resistance R_s, the interfacial layer, and the interface states when the applied voltage is sufficiently large. The series resistance is significant in the downward curvature (non-linear region) of the forward bias $I\text{–}V$ characteristics, but the other two parameters are significant in both the linear and non-linear regions of the $I\text{–}V$ characteristics. The lower the interface states density and the series resistance, the greater the range over which the $I\text{–}V$ curve yields at straight line [23]. As the linear range of the forward $I\text{–}V$ plots is reduced, the accuracy of the determination of Φ_{Bf} and n becomes poorer. Here, the ideality factor, the barrier height and the series resistance were evaluated using a method developed by Cheung and Cheung [24] in the high current range where the $I\text{–}V$ characteristic is not linear. The forward bias current–voltage characteristics due to thermionic emission of a Schottky diode with the series resistance can be expressed as [1,23,30,35]

$$I = I_0 \exp\left[\frac{q(V - IR_s)}{nkT}\right] \tag{8}$$

where I_0 is the saturation current. The term IR_s is the voltage drop across series resistance of diode. The voltage $V_d = V - IR_s$ across the diode can be expressed in terms of the total voltage drop V across the series combination of the diode and the series resistance. The value of n calculated from the slope of the linear portion of the $I\text{–}V$ characteristics especially includes the effect of the interfacial parameters rather than that of the series resistance [14,21,36]. Now, to determine diode parameters such n, Φ_B and R_s, let us obtain the functions of Cheung and Cheung [24]. From Eq. (8), the following functions can be written as

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \tag{9}$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) \tag{10}$$

and $H(I)$ is given as follows:

$$H(I) = n\Phi_B + IR_s \tag{11}$$

where Φ_B is the barrier height obtained from data of downward curvature region in the forward bias $I\text{–}V$ characteristics.

In Fig. 5a and b, experimental $dV/d(\ln I)$ vs. I and $H(I)$ vs. I plots are presented at different temperatures for Al/SnO_2/p-Si MIS Schottky diode, respectively. Eq. (9) should give straight line for the data of downward curvature region in the forward bias $I\text{–}V$ characteristics. Thus, a plot of $dV/d(\ln I)$ versus I will give R_s as the slope and nkT/q as the y-axis intercept. As a function of temperature, the values of n and R_s derived from Fig. 5a and are presented in Table 1. Using the n value determined from Eq. (9), and the data of downward curvature region in the forward bias $I\text{–}V$ characteristics in Eq. (10) a plot of $H(I)$ vs. I will also lead a straight line (as shown in Fig. 5b) with y-axis intercept equal to $n\Phi_B$. The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of this approach. Thus, for each temperature and by performing different plots (Eqs. (9) and (11)) of the $I\text{–}V$ data,

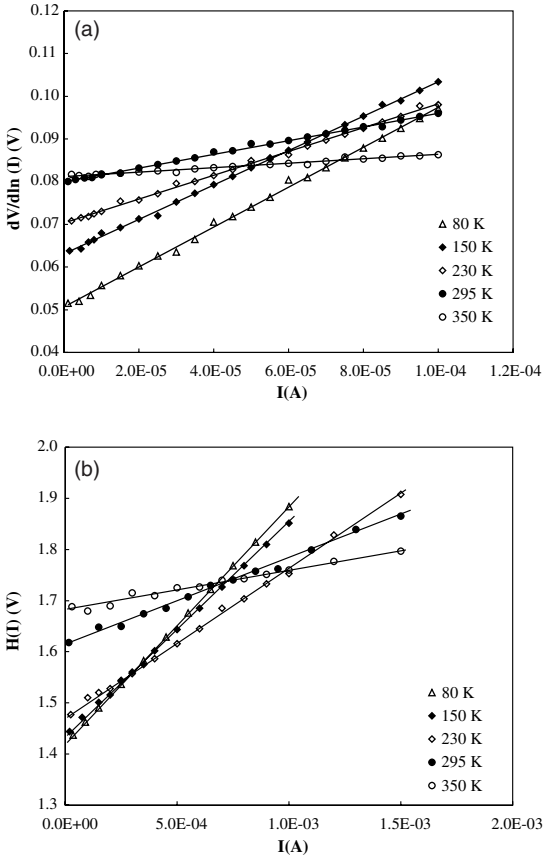

Fig. 5. The characteristics of Al/SnO_2/p-Si at different temperatures: (a) $dV/d\ln(I)$ vs. I and (b) $H(I)$ vs. I.

three main diode parameters (n, Φ_B and R_s) are obtained and presented in Table 1. As shown in Table 1, the obtained n and R_s values by different techniques are in good agreement with each other and decrease strongly with increasing temperature ($R_s \cong 460.64\ \Omega$ and $n = 7.40$ at 80 K; $R_s \cong 50.19\ \Omega$ and $n = 2.70$ at 350 K).

For MIS diode having interface states N_{ss} in equilibrium with the semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [11], and is given by

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W_D} + qN_{ss}\right) \tag{12}$$

where W_D is the space charge width, ε_s and ε_i are the permittivity of semiconductor and interfacial layer, respectively. N_{ss} is the density of interface states in equilibrium with the semiconductor. For each temperature, substituting in Eq. (12) the values of n related to forward bias V obtained from experimental data of the I–V in Fig. 1 and the variation of W_D calculated from $1/C^2$–V characteristics (Fig. 6), the values of N_{ss} as a function of V were obtained and are given in Table 1. In p-type semiconductors, the energy of the interface states E_{ss} with respect to the top of the valance band at the surface of the semiconductor is given by

$$E_{ss} - E_v = q(\Phi_e - V) \tag{13}$$

where

$$\Phi_e = \Phi_{Bf} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{14}$$

The energy distribution or density distribution curves of the interface states can be thus obtained from experimental data of this region of the forward bias I–V in Fig. 1. Fig. 7 shows the resulting dependence of N_{ss} converted to a function of E_{ss} using Eq. (13) at various temperatures. We have observed then that the mean N_{ss} decreases when the temperature increases ($N_{ss} = 8.29 \times 10^{13}$ $eV^{-1}\,cm^{-2}$ at 80 K; $N_{ss} = 2.20 \times 10^{13}$ $eV^{-1}\,cm^{-2}$ at 350 K (Table 1)). This case is a result of molecular restructuring and reordering of the metal–semiconductor (Al/SnO_2/p-Si) interface under the temperature effect [37]. As can be seen Fig. 7, exponential growth of the interface state density towards the top of the valance band is very apparent. There is a drift effect with temperature. In the range $0.62 - E_v$ to $0.70 - E_v$ eV the values of the interface state density are 7.47×10^{13} and 2.37×10^{13} $eV^{-1}\,cm^{-2}$, respectively, at room temperature (295 K). Here, E_v is the valance band edge. Furthermore, the interface state density distribution curves have a minimum. It was seen to appear shifting towards the valance band in the N_{ss} curves, which are due to the interfacial layer at different temperature.

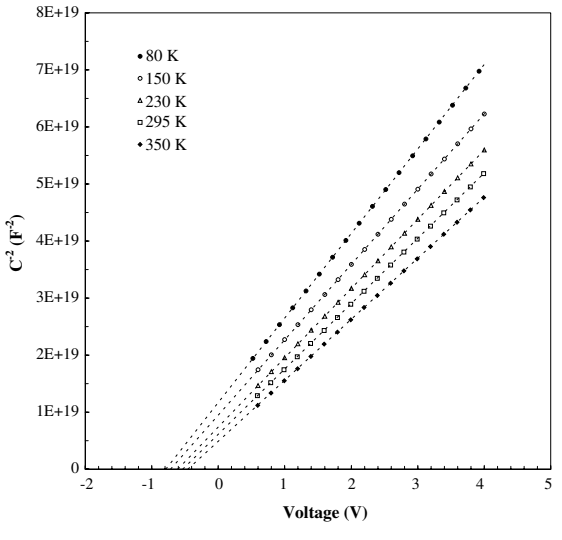

Fig. 6. The $1/C^2$ vs. V plot of Al/SnO_2/p-Si for different temperatures at frequency of 500 kHz.

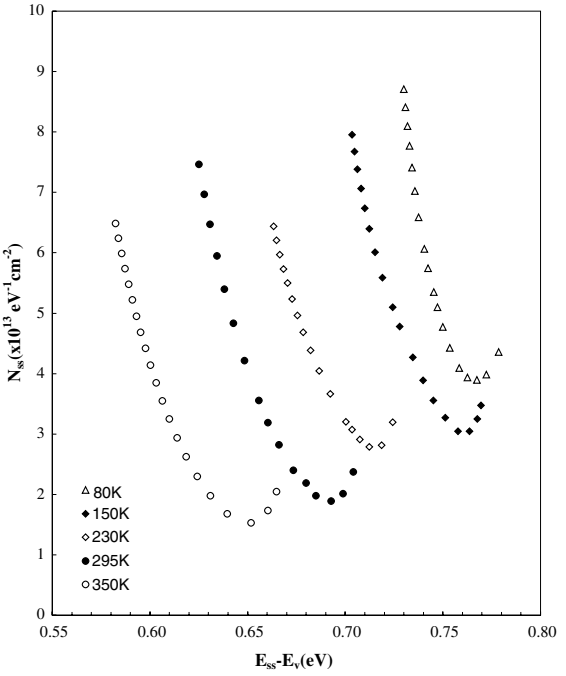

Fig. 7. Density of interface states N_{ss} as a function of $E_{ss} - E_v$ deduced from the I–V data at various temperatures.

3.2. Effects of series resistance and interface states on C–V/T characteristics

The capacitance–voltage (C–V) measurements were performed at high frequency (500 kHz) by using HP 4192A LF Impedance Analyzer, so that the interface states are unable to respond to the AC signal. The C–V

Table 2
Temperature dependent values of various parameters determined from C–V characteristics of Al/SnO_2/p-Si Schottky diode

T (K)	N_A (cm^{-3})	E_F (eV)	V_D (eV)	W_D (cm)	$\Delta\Phi_B$ (meV)	$\Phi_B(C$–$V)$ (eV)	$N_{ss}(C$–$V)$ ($\times 10^{13}$ eV^{-1} m^{-2})
80	8.19×10^{14}	0.038	0.795	1.14×10^{-4}	13.3	0.822	1.53
150	9.19×10^{14}	0.083	0.732	1.02×10^{-4}	13.2	0.802	1.22
230	9.99×10^{14}	0.138	0.629	9.05×10^{-5}	13.0	0.754	1.01
295	1.06×10^{15}	0.185	0.558	8.24×10^{-5}	12.7	0.732	0.87
350	1.13×10^{15}	0.225	0.487	7.46×10^{-5}	12.5	0.701	0.73

measurements under reverse bias were performed over the range of 80–350 K. The C^{-2}–V characteristics illustrated in Fig. 6 are linear for each temperature. From the C–V measurements, the barrier height $\Phi_B(C$–$V)$ were calculated at temperatures 80, 150, 230, 295 and 350 K using the voltage intercept V_0 of the C^{-2}–V plot from the relation

$$V_0 = \frac{(E_g - \Phi_m + \chi_s)}{q - E_F - V_i} \tag{15}$$

and

$$V_0 = V_D - \frac{kT}{q} \tag{16}$$

where E_g, E_F, Φ_m, V_i, χ_s and V_D are the band gap of Si, the energy difference between the bulk Fermi level and valance band edge, the metal work function, the potential drop on the oxide layer, the electron affinity, and diffusion potential, respectively. The barrier height from the inset to Fig. 6 is

$$\Phi_B(C-V) = V_0 + \frac{kT}{q} + E_F - \Delta\Phi_B \tag{17}$$

where $\Delta\Phi_B$ is the image force barrier lowering and given by [1]

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}} \tag{18}$$

where $E_m = \sqrt{2qN_AV_D/\varepsilon_s\varepsilon_0}$ is the maximum electric field. The values of carrier doping density N_A used in the calculations were determined from the slope of C^{-2}–V plots at different temperatures. The temperature dependent E_F values were obtained from

$$E_F = \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \tag{19}$$

with

$$N_V = 4.82\times10^{15}T^{3/2}\left(\frac{m_h^*}{m_0}\right)^{3/2} \tag{20}$$

where N_V is the effective density of states in Si valance band, $m_h^* = 0.16m_0$ the effective mass of holes [38] and m_0 the rest mass of the electron.

In general, at sufficiently high frequencies ($f \geqslant 500$ kHz) the interface states do not contribute to the capacitance [15,16,37,39] since they are in equilibrium with the semiconductor. The relationship of the theoretical carrier doping density $N_A' = 1.73\times10^{15}$ cm^{-3} and the experimental the theoretical carrier doping density N_A is known $c_2 \cong N_A'/N_A$ [17]. The density of interface states N_{ss} were calculated at different temperatures by using

$$c_2 = \frac{1}{1+\beta} \tag{21}$$

where $\beta = q\delta N_{ss}/\varepsilon_i$ [35,40]. The mean density of interface states N_{ss} were calculated at different temperatures from Eq. (21), by taking the δ value as 28 Å. The obtained values of N_A, E_F, V_D, W_D, $\Delta\Phi_B$, $\Phi_B(C$–$V)$ and N_{ss} at different temperatures are presented in Table 2. As shown in Table 2, the obtained $\Phi_B(C$–$V)$ and $N_{ss}(C$–$V)$ values decrease with increasing temperature and they are in a close agreement with $\Phi_{Bf}(I$–$V)$ and $N_{ss}(I$–$V)$ calculated from I–V characteristics (Table 1).

4. Conclusions

The studied Al/SnO_2/p-Si Schottky diode is an MIS structure with interface states in thermal equilibrium with the semiconductor. The current conduction mechanism across Al/SnO_2/p-Si Schottky diode was carried out using I–V and C–V measurements in the temperature range of 80–350 K. The non-ideal forward bias I–V behavior observed in the Al/SnO_2/p-Si Schottky diode was attributed to a change in the metal–semiconductor barrier height due to the interfacial layer, interface states and the series resistance.

We have reported a modification, by the inclusion both of n and $a\chi^{1/2}\delta$ in the expression of I_0 to explain the experimental I–V characteristics of Al/SnO_2/p-Si Schottky diode. The validity of including n and $a\chi^{1/2}\delta$ in the expression of I_0 are demonstrated by comparing the corrected values of the barrier height Φ_{Bf} with the values obtained from the C–V measurements and by checking the temperature dependence of barrier height against that of energy band-gap E_g. The flat-band barrier height Φ_{Bf} obtained from I–V data using this modification

agrees with that obtained from C–V data, confirming the validity of the present approach.

The values of the ideality factor n controlled by the interface state density were found to be strongly temperature dependent and increased with the decreasing of temperature. Hence, the values of the ideality factor n indicated that the current transport mechanism consists of both the trap-assisted tunneling and the thermionic emission. It is shown that the series resistance values decreased as the temperature is increased. This case proves the validity and applicability of Cheung's method to calculate R_s and the other parameters of Schottky diodes. Such behaviors of n and R_s have been attributed to distribution of interface states, inhomogeneity interfacial layer and surface preparation.

Interface state density N_{ss} obtained from the I–V and C–V measurements at different temperatures agrees with each other and decreased with increasing temperature. At the same time, the density of interface states distribution profile as a function of $E_{ss} - E_v$ (from the I–V at various temperature) decreased with increasing temperature. The improvement obtained by the temperature effect is probably due to the thermal restructuring and reordering of the interface.

In summary, it is clear that ignoring the interfacial layer, series resistance and interface states can lead to significant errors in the forward bias I–V and C–V characteristics. The saturation current is high and the interface state density is large in our sample (Al/SnO_2/p-Si). Hence, it is of technological importance to study the interface state density distribution, especially for the SnO_2/Si solar cells and SnO_2-based gas sensors.

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