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MIS-TSC: A combination of the thermally stimulated current method and a metal-insulator-semiconductor device for unipolar trap spectroscopy

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ABSTRACT

To determine the density of states distribution of traps within a semiconductor, the thermally stimulated current (TSC) method is often applied. However, the bipolar nature of the typical device structure does not allow for strict unipolar operation, and therefore the method does not allow for the separate evaluation of electron and hole traps. The recombination between electrons and holes makes the interpretation of the data difficult, which becomes an essential drawback of this method. To address these issues, we propose the use of a metal insulator semiconductor (MIS) device structure for TSC measurements, which can be operated strictly unipolar by the sign of the applied voltage during the charging process. Thus, the problem of recombination and bipolar contribution to the measurement signal is avoided. As an additional benefit, the MIS device structure typically results in very low leakage currents, and thus a low noise level for the measurement. This permits precise measurements even below 1 pA, and consequently increases the resolution of the method. This aspect is especially important for fractional TSC, as the measurement time is long and the current low when compared to the envelope measurement. Here, we demonstrate the basic principle of this TSC approach, which we name MIS-TSC, using the well-studied organic semiconductor P3HT as a benchmark.

A detailed understanding of the density of trap states of semiconductors is crucial for their use in various electronic applications like, e.g., photo- and light-emitting diodes or transistors. A well-known method for the determination of the density of trap states is thermally stimulated current (TSC) measurements.[1–3] This method is used for the characterization of semiconductors, both inorganic[4,5] and organic[6,7] as well as hybrid materials like, e.g., perovskites.[8] While the method has the advantage of direct access to the activation energy of trapped charge carriers, which is assigned to the energetic trap depth, it also has significant disadvantages, hindering its widespread application. Classical TSC measurements on bipolar diodes do not avoid recombination of complementary charge carriers, falsifying the trap depth and distribution information.[3,9] Consequently, the evaluation of separate electron and hole trap depth information is not possible without further analysis. Furthermore, classical TSC approaches utilize the device built-in field for charge extraction, which leads to special requirements for the contact materials.

Here, we propose a modification of the TSC method by using a metal insulator semiconductor (MIS) device structure, which allows for unipolar trap occupation by choosing the direction of the electric field during the electrical charging process. Consequently, this modification avoids recombination and bipolar contributions. Instead of being dependent on the built-in field for the charge extraction, the charge extraction is driven by the electric field introduced into the device by the trapped charges.

For the MIS-TSC measurement, the device under test (DUT) is charged by a DC voltage V_{ch}. The timing of the charging process is schematically shown in the supplementary material (Fig. S1). V_{ch} is applied at Δt_1 prior to, during, and at Δt_2 after cooling down. For complete charging of the DUT, Δt_1 must exceed the RC time constant τ_p of parasitic capacitances (10 ns in our case), e.g., coaxial cables or contact metallization directly on top of the insulator, and the temperature dependent RC time constant τ_i for the injection of charges into the DUT (1 s at 300 K in our case). For the MIS structure, this

parameter is primarily defined by the injection barrier, the resistance of the semiconductor and the capacitance of the insulator.

The occupation of traps will occur during the application of V_{ch}. After Δt_2, V_{ch} is switched off and the sample is short circuited with an electrometer (Keithley 6517B) connected in series just as with classical TSC measurements.[1–3] After short-circuiting, free excess charge will be discharged with a temperature dependent RC time constant τ_e, which differs from τ_i by the ejection barrier compared to the injection barrier. Simultaneously, the parasitic capacitances will discharge with τ_p. The generated discharging current by both effects needs to drop down close to the noise floor prior to the actual MIS-TSC measurement. Furthermore, it needs consideration that the electric field, introduced by the trapped charge carriers, may lead to the injection of complementary charge carriers while the sample is in short circuit condition, resulting in unintentional recombination. To avoid this, the ejection resistance must be much smaller than the injection resistance, meaning $\tau_e \ll \tau_i$. Thus, a contact metallization with a work function in the middle of the semiconductor bandgap leading to a high injection but no ejection barrier is preferred.

For the MIS-TSC (i_{TSC}) measurement, the sample is heated at a constant rate β, and trapped charge carriers are thermally released as TSC. On dependents of β, there are two effects observed on the occurring TSC peaks. As there is a time delay dependence on τ_e before the ejection of charge carriers, a peak will shift to higher temperatures at a higher β. Simultaneously, for the second effect, the peak will increase as the same amount of charge carriers is extracted over a shorter time period. This might result in a worse resolution in the case of multiple and overlapping peaks. At the same time, the signal to noise ratio is improved.

During heating, the injection of complementary charge carriers is still possible. The total amount of these charge carriers during the measurement must be small compared to the total amount of extracted charge carriers. Thus, τ_i must be large compared to τ_e and to the remaining measurement time at all temperatures. Assuming neglectable re-trapping and a single trap state, i_{TSC} is related to the activation energy E_a, as defined by the following equation:[1,2,10]

$$i_{TSC} \propto e^{\frac{-E_a}{k_B T}}. \tag{1}$$

Here, k_B is the Boltzmann constant and T the temperature. From the slope of $ln(i_{TSC})$ over $1/T$, a linear regression can extract E_a. The integration of i_{TSC} over time gives the total amount of excited charge carriers. The measured density of trapped charge carriers is strongly dependent on the trap filling probability during charging. A distribution of occupied trap states can be determined using fractional measurements by sequentially discharging the DUT.[1] Every sequence consists of a temperature increase, with a subsequent cool down. For each maximum temperature and sufficiently small temperature steps, the associated E_a can be approximated using Eq. (1) by assuming a single trap level.

For benchmarking the MIS-TSC experiment, classical TSC measurements are performed on poly(3-hexylthiophene-2,5-diyl) (P3HT, Sepiolid P200 from BASF) diodes, with the following structure on glass: indium tin oxide (ITO), poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS, 40 nm), P3HT (80 nm), calcium (Ca, 30 nm) and aluminum (Al, 200 nm). The substrate is commercially available from Naranjo BV with a pre-structured ITO layer and is UV light- and ozone-treated at 110 °C for 15 min prior to further processing. The PEDOT:PSS solution (Clevios HIL-E100 from Heraeus) was diluted with twice distilled water in the ratio 1:1. For spin coating PEDOT:PSS, the parameters 5 s/500 rpm followed by 40 s/5000 rpm were used, forming the hole injection layer with a work function of 5 eV to 5.2 eV.[11] For P3HT deposition, a solution with a concentration of 20 mg/ml in chlorobenzene was heated for 2 h at 60 °C and then dissolved further using a Vortex Genie 2 for 3 days. For deposition, the solution was again heated to 60 °C and spin coated with 5 s/200 rpm, 30 s/1000 rpm and 10 s/3000 rpm. Ca was evaporated with a rate below 1 Å/s at a maximum pressure of 6×10^{-6} mbar. The deposition of the first 30 nm Al was done using the same parameters. For further Al film thickness, the rate was increased up to 50 Å/s at 10^{-5} mbar. The effective diode area of 7.5 mm^2 is defined by the electrode overlap.

For the MIS-TSC sample (Fig. 1), a 10^{15} cm^{-3} n-doped crystalline silicon (n-Si) substrate with one-sided 200 nm thermally grown SiO_2 ($\epsilon_r = 3.9$) and an Al bottom contact was used. The layer stack on SiO_2 is subsequently made up of Ca (0.5 nm, passivation purposes), P3HT (80 nm), silver (Ag, 100 nm) and Al (200 nm). Hereby, the parameters employed for Ca evaporation were 0.1 Å/s and 4×10^{-6} mbar and for Ag were 2 Å/s and 6×10^{-6} mbar. P3HT and Al were deposited using the same process as for the diode structure. The effective sample area of 16.25 mm^2 was defined by wiping the material away with a cloth soaked in chlorobenzene. As discussed in the theory part, a contact metal with a work function in the middle of the HOMO (between 4.65 eV and 5.2 eV) and the LUMO (between 2.13 eV and 3.2 eV) of P3HT[12–15] is necessary. Ag is a suitable choice as the work function is 4.3 eV.[16]

For contacting either sample in the cryostat, wires were glued onto the contacts using the silver epoxy EPO-TEK H21D from Epoxy Technology. In this step, the samples are tempered at 130 °C for 12 min. All processing steps apart from the deposition of PEDOT:PSS were performed in an inert nitrogen atmosphere.

For charging the MIS samples, $V_{ch} = 50$ V (e-) and $V_{ch} = -50$ V (h+) are applied. The cooling is done with $\beta = 0.05$ K/s and $\Delta t_1 = \Delta t_2 = 600$ s. Hereby, the amount of accumulated charge Q is related to the capacitance C of the insulator by $Q = C \cdot V_{ch}$, which can be distributed over the available trap states in the semiconductor. If the total amount of trap states is smaller than the required amount of states to store Q, all trap states will be filled up under the assumption that Q is sufficiently distributed over the volume. The remaining non-trapped charge will be released as soon as the device is short-circuited. If the total amount of trap states is larger, then the trap states are not completely filled and the charges will most probably not be homogeneously distributed over the volume of the semiconducting layer. For the DUT discussed in this contribution, a $|V_{ch}| = 50$ V will result in the charge carrier accumulation of 5×10^{12} cm^{-2}. Assuming a

FIG. 1. Schematic MIS device structure. The P3HT layer is completely covert by the metal top contact.

homogeneous trap distribution in an 80 nm thick semiconductor layer, a trap density of $1.25 \times 10^{17}\,cm^{-3}$ would be required to completely trap this charge. As for the conventional TSC method, only the integral charge can be measured, and therefore no conclusions can be made about the spatial trap distribution. Consequently, trap states at the P3HT/SiO_2 interface could have a significant influence on the measurement, making the passivation of the interface necessary. For an organic semiconductor on SiO_2, e.g., a thin calcium oxide (CaO) passivation layer is an option,[17] which reduces hydroxyl groups on the surface,[17,18] or different polymer caps are an option. Likewise, the top contact (semiconductor/metal interface) may introduce interface defect states, which will influence the MIS-TSC results. These aspects will be considered in further more detailed studies.

After an additional waiting time of 1800 s for discharging excess charges, the heating of the DUT with $\beta = 0.015$ K/s for an enveloping measurement is started. Such a low β value is possible due to the low noise level of the MIS measurement. For the case of fractional MIS-TSC measurements, effective 20 K (+50 K, −30 K) temperature steps are used. Between each temperature step, the waiting time is 20 min. For every temperature ramp, $\beta = 0.02$ K/s is used, which is higher than that of the enveloping measurement, as the extracted TSC might fall below the noise level for lower β. The procedure for the classical TSC measurement differs from the MIS TSC measurement by $V_{ch} = -3$ V and $\beta = 0.02$ K/s.

Preliminary experiments are conducted to exclude influences, like potential charge carrier trapping, of the Si-substrate and the Si/SiO_2 interface on the MIS-TSC measurement. For this purpose, a reference sample was built using a Si/SiO_2 substrate and the described contact metallization only. Figure 2 shows the TSC signal of this sample with and without charging. Both signals are identical in the 0.2 pA range, substantiating a neglectable influence of charge trapping in the substrate and its interfaces (n-Si/SiO_2 and n-Si/Al) during the MIS-TSC measurement. The measurement also substantiates low leakage currents, which are caused by the burden voltage of the electrometer (up to 100 μV), due to the high serial resistance of the MIS substrate. This makes precise measurements in the subpicoampere range possible.

Second, as the unipolar measurement of traps requires either $V_{ch} > 0$ V (e-) or $V_{ch} < 0$ V (h+) applied to the MIS structure, the influence of the space charge in the n-Si on the capacitance, as well as on the accumulated charge needs consideration. For the MIS sample in our case, the capacitance reduction results in a reduced electron accumulation by 10% in the P3HT when compared to the hole accumulation as shown in the supplementary material with further details. Consequently, this may influence the maximum measurable density of electron trap states.

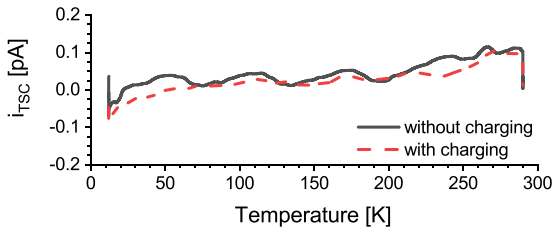

FIG. 2. MIS-TSC of the reference sample without P3HT and Ca with ($V_{ch} = 50$ V) and without charging ($V_{ch} = 0$ V).

Furthermore, using a MIS structure for the TSC evaluation may result in polarization currents, as observed for the temperature stimulated depolarization current (TSDC) method.[19] However, for the case at hand, consideration of TSDC is not necessary, as polarization effects are only relevant for P3HT at temperatures far above 300 K.[20] In general, the influence of this effect should be identifiable when using an amorphous isotropic semiconductor, as TSDC would be independent of the field direction.

Figure 3(a) shows a classical TSC signal of the P3HT diode, built as described above, for benchmarking the MIS-TSC measurements as discussed below. For all figures, the TSC signal is normalized to the active area, in order to account for different electrode areas. The temperature dependent current without sample charging $I_{TSC,without}$ (red dashed/dotted line) is the consequence of the burden voltage and the temperature dependent low serial resistance of the device.[21] The current with charging $I_{TSC,with}$ (black dotted line) is the superposition of $I_{TSC,without}$ and the actual TSC signal, which is consequently falsified. To correct this measurement, the difference between the $I_{TSC,with}$ and $I_{TSC,without}$ currents is formed, resulting in the actual TSC (solid blue line). Hereby, the measurement artifacts of $I_{TSC,without}$ cause false peaks in the determined TSC, as indicated by the gray arrows. However, the corrected measurement is well in line with literature data, as can be determined from the trap peaks at 145 K and near 300 K, as well as the

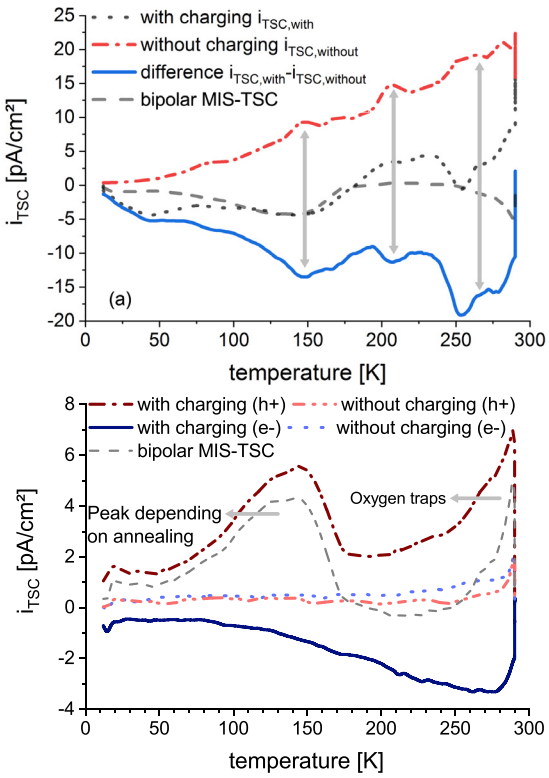

FIG. 3. (a) Enveloping TSC of a P3HT diode: The gray arrows mark the measurement artifacts within the $i_{TSC,without}$, resulting in false peaks in the calculated difference curve. (b) Enveloping TSC of a MIS sample for electrons and holes with $|V_{ch}| = 50$ V. Additionally, the sum of both currents is shown as a bipolar MIS-TSC curve in (b) and as a negative curve in (a).

elevated current level between 170 K and 270 K, which originates from the use of PEDOT:PSS.[7,20] The peak at 250 K is not described in the literature, but may as well be a measurement artifact in $I_{TSC,with}$ similar to those in $I_{TSC,without}$.

The result of the MIS-TSC measurement is illustrated in Fig. 3(b), highlighting a separate electron and hole measurement using one and the same MIS sample. The burden voltage current of the measurement without charging is neglectable, and thus does not require correction as discussed for the classical TSC measurement. Essentially, the high serial resistance of the MIS sample is responsible for this effect. The hole-only TSC (dark-red dashed/dotted line) demonstrates pronounced peaks at 140 K and 300 K, which is in line with the classical TSC signal and confirms the interpretation of Yu *et al.* as hole related traps.[20] The electron-only TSC (dark-blue solid line) demonstrates a wide peak at 270 K. Here, we suggest this peak to be the consequence of interface states such as hydroxyl groups on the SiO_2 surface.[18] By assuming a recombination probability of 1, the electron and hole currents can be added to form the bipolar MIS-TSC signal (gray dashed line, Fig. 3), which is comparable to the classical TSC. Hereby, a good match of peak positions is evident. The lower bipolar MIS-TSC signal compared to the classical TSC signal is a result of the burden voltage. This equipment-dependent bias voltage increases the TSC signal of a diode due to a higher conductivity, originating from a higher charge carrier concentration and possibly a higher charge carrier mobility.[3,5,21] The slight difference in peak positions can be explained by the higher β chosen for the classical TSC. The absence of the PEDOT:PSS influence in the current signature of the bipolar MIS-TSC signal is to be expected, as this material was not used in the MIS device.

For the investigation of the energetic electron and hole trap distribution, a fractional MIS-TSC experiment was conducted (Fig. 4).

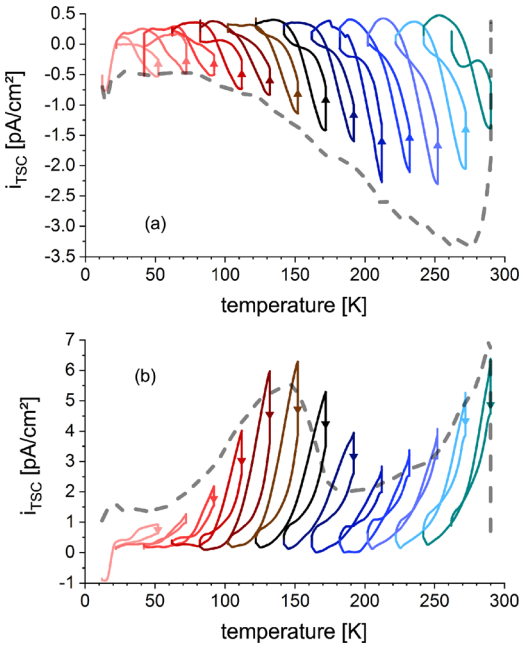

FIG. 4. Fractional MIS-TSC measurement with a 20 K step width of electrons (a) and holes (b). The gray, dashed line is in both cases the enveloping measurement shown in Fig. 3.

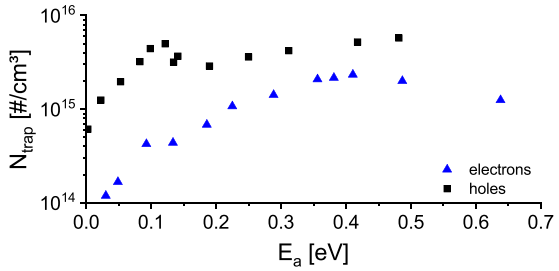

FIG. 5. Activation energies and the number of trapped charge carriers (N_{trap}) calculated from the MIS-TSC (Fig. 4).

Hereby, the same MIS-TSC peaks as within the enveloping results (dashed gray line) are visible. Slightly higher currents may be the consequence of the higher β. The occasionally higher current during cool down, when compared to the heating sequence, is the result of re-trapping. However, the return to zero current at the beginning of each temperature step suggests a full charge extraction for the previous E_a level, and therefore no negative impact on the measurement.

The densities of trapped charge carriers determined from the MIS-TSC are summarized in Fig. 5. The hole trap density distribution demonstrates a maximum at 100 meV as well as a trap shoulder starting at 200 meV up to 500 meV, which is correlated with a temperature of 300 K. These are in line with the trap distribution discussed by Yu *et al.*[20] and Schafferhans *et al.*[22] The electron trap distribution shows a small peak at 100 meV as well, which is typically not visible using the classical TSC approach, due to recombination. Furthermore, a second electron peak can be determined at an activation energy of $E_a = 400$ meV. This level is in line with a trap state discussed by Nicolai *et al.*,[23] as the consequence of oxygen defects. The energetic difference to the Nicolai-level at 600 meV is possibly the consequence of the LUMO uncertainty for P3HT, which was the basis for their calculation. However, from this measurement, it is not possible to determine if those defects are located in the bulk or on the P3HT/SiO_2 interface. The total amount of trapped charge carriers of 2.5×10^{15} cm^{-3} (holes) and 1.3×10^{15} cm^{-3} (electrons) is significantly lower than the maximum density of introduced charges (1.25×10^{17} cm^{-3}) during the charging process. Thus, a complete filling of all traps states is possible.

We have introduced an improvement to the TSC method used for the energetic trap state evaluation in semiconductors. By using a MIS structure instead of the classical diode, both electron and hole trap state distributions can be determined individually in a single test sample. Beyond the unipolar trap evaluation, the MIS-TSC approach reduces the recombination effects, which are one of the major challenges for classical TSC. Furthermore, due to the high serial resistance of MIS structures, a noise level in the subpicoampere range was obtained, making a precise evaluation of the TSC below 1 pA possible.

See supplementary material for a schematic timing diagram of the MIS-TSC measurement sequence. Additionally, a capacitance-voltage measurement of the MIS device is shown, which indicates the effect of Ca passivation and voltage dependent capacitance change.

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