Modified Charge Amplifier for Stray Immune Capacitance Measurements

Robert Oven, *Member, IEEE*

***Abstract*— It is shown theoretically and by experimentation that the ac stray immune capacitance meter based on the charge amplifier circuit can be modified to reduce the effects of the parasitic capacitance across the feedback capacitor. This is achieved by simply introducing a unity gain buffer amplifier within the circuit loop.**

***Index Terms*— Capacitance measurement, capacitive sensor, charge amplifier, operational amplifier, parasitic capacitance.**

I. Introduction

THE measurement of small capacitances has been an area of active research for many years both for scientific and industrial applications [1]. Many circuit designs have been proposed offering the ability to measure small capacitances with varying degrees of accuracy, linearity, speed of measurement, immunity to stray capacitance, circuit complexity, and ease of use [1]–[7]. The basic charge amplifier with ac excitation and some variants has been used by a number of authors to measure small capacitances [8]–[15]. The circuit, shown in Fig. 1, is popular since it is immune to a number of stray capacitances. It and some variants have been used in capacitive sensor circuits [8], [9], capacitance tomography [10], in the laboratory for measurement of physical quantities [11], [12] in human proximity sensor applications [13] and in 3-D capacitive probing [14], [15]. Fig. 1 shows the basic circuit including various parasitic capacitances. Capacitor C_X is usually the unknown capacitance that is to be determined, C_f is a fixed feedback capacitor and resistor R is for dc stability. Provided $R \gg 1/\omega C_f$ then the gain is given by

$$\frac{V_O}{V_i} = -\frac{C_X}{C_f} \tag{1}$$

over a wide range of the operating frequency ω. As argued in [8], parasitic capacitance C_{p1} has little effect on the circuit since it is being charged and discharged by the low impedance source V_s. This argument can also be applied to C_{p4} due to the low impedance output of the operational amplifier. Parasitic capacitor C_{p2} is across the virtual earth of the operational amplifier and so the potential across it is very small. Hence, its presence will not significantly affect the measurement of the capacitance C_x [8]. It has, however, been shown to reduce the bandwidth of the circuit [10]. For capacitive tomography applications CMOS switches are introduced into the circuit. Their finite resistance combined with parasitic capacitances also affect the circuit bandwidth [10].

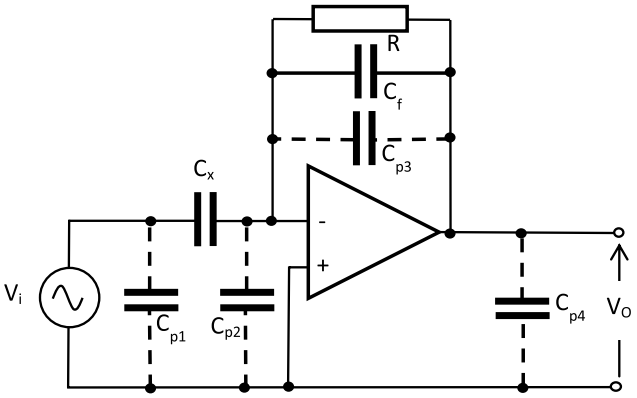

Fig. 1. Basic stray immune capacitance meter with parasitic capacitances.

Clearly, parasitic capacitor C_{p3} is in parallel with C_f and is associated with the packaging of the chip and board layout. In [8], C_f was large, ~300 pF, and so the effect of C_{p3} was negligible although its potential effect was recognized. With the measurement of smaller capacitances, C_x, with this circuit the values of C_f used have reduced, with values in the order of a few pFs [11], [14] down to 0.5 pF being found in [11] and [12]. Hence, the sensitivity of the circuit's performance and accuracy to board layout and component packaging can be expected to increase. Recently, the above circuit has been used in the development of a 3-D capacitive probing system where now C_f is the unknown capacitance associated with the probe and is in the order of 0.4 pF [15]. Here, the parasitic capacitance in parallel with C_f is of prime importance.

In this paper, we demonstrate theoretically and by measurement that it is possible to reduce the sensitivity of the circuit to C_{p3} by simply introducing a unity gain buffer amplifier at the input of the operational amplifier but within the loop, as shown in Fig. 2. This can immediately be observed qualitatively. Applying the above reasoning to the circuit in Fig. 2, we can ignore the parasitic capacitances C_{p1}, C_{p4}, C_{p5} and C_{p6} since they are again being charged and discharged by low impedance sources, i.e., either by the source V_i or by the outputs of the operational amplifiers. The voltage across either end of C_{p3} will be almost identical since it is now across a

Manuscript received June 27, 2013; revised September 4, 2013; accepted October 25, 2013. Date of publication January 23, 2014; date of current version June 5, 2014. The Associate Editor coordinating the review process was Dr. Theodore Laopoulos.

The author is with the School of Engineering and Digital Arts, The University of Kent Canterbury, Kent CT2 7NT, U.K. (e-mail: r.oven@kent.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2014.2298673

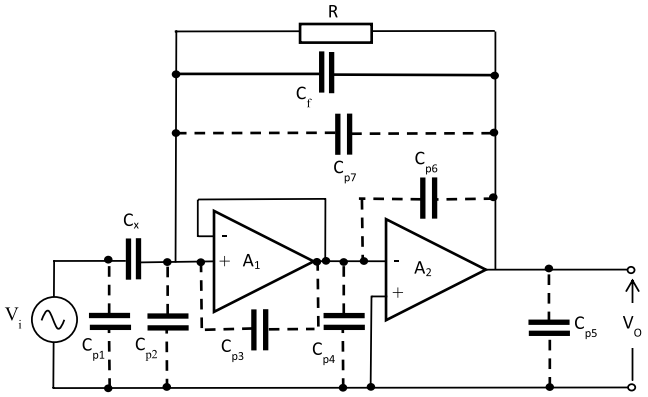

Fig. 2. Modified stray immune capacitance meter with parasitic capacitances.

noninverting amplifier with unity gain. Hence, provided the operating frequency is well below the unity gain bandwidth of that particular amplifier C_{p3} can now also be ignored.

The value of the new parasitic capacitance denoted by C_{p7} in Fig. 2 should be much less than C_{p3} since its two end points can now be physically separated by a larger distance than those of C_{p3} and can be reduced even further if necessary, since an electrostatic screen can be introduced between the two amplifiers, as will be demonstrated.

In Section II, the transfer function of the modified charge amplifier in Fig. 2 is derived and its performance discussed. It is formally shown that C_{p3} has little effect on the circuit's operation. In Section III, the performance of the modified charge amplifier is experimentally confirmed by measuring values of C_f, the feedback capacitor in the femtoFarad range for a fixed value of C_x. This necessitates the use of a feedback network rather than a simple feedback resistance R due to the smallness of C_f. Finally, the circuit is used to measure the capacitance of an adjustable parallel plate capacitor with guard ring, which replaces C_f.

II. Analysis

To formally analyze the circuit shown in Fig. 2, we assume that the two operational amplifiers can be modeled by single dominant pole transfer functions. We hence have

$$A_1(s) \cong \frac{\omega_1}{s}, \quad A_2(s) \cong \frac{\omega_2}{s} \tag{2}$$

where ω_1 and ω_2 are the unity gain bandwidths of op-amps 1 and 2, respectively, and $s = j\omega$. A_1 is the buffer amplifier. In the analysis, we include the parasitic components C_{p3} and C_{p2}. Assuming negligible output impedances for the amplifiers the other parasitic capacitances can be ignored. For the circuit in Fig. 2, we have (3), which is shown at the bottom of the page.

Parasitic C_{p7} can be included by replacing C_f by $C_f + C_{p7}$. If $\omega \gg 1/\mathrm{RC}_f$ and $\omega_2 \gg 1/\mathrm{RC}_f$ such that the first two terms in the denominator can be ignored then the remaining transfer function has poles at

$$\omega_{U,V} = \frac{\omega_1\left(C_f + C_x + C_{p2}\right)}{2(C_f + C_x + C_{p2} + C_{p3})} \times \left[1 \pm \sqrt{1 - \frac{4(C_f + C_x + C_{p2} + C_{p3})C_f\omega_2}{(C_f + C_x + C_{p2})^2\omega_1}}\right]. \tag{4}$$

If $\omega_1 > \omega_2 C_f/(C_f + C_x + C_{p2})$ then since $\sqrt{1+x} \cong 1 + \frac{1}{2}x$ for small x these can be approximated by

$$\omega_U = \frac{\omega_2 C_f}{(C_f + C_x + C_{p2})} \tag{5}$$

and

$$\omega_V = \frac{\omega_1\left(C_f + C_x + C_{p2}\right)}{(C_f + C_x + C_{p2} + C_{p3})} - \omega_U \cong \omega_1 - \omega_U. \tag{6}$$

Hence, provided $\omega < \omega_U$ then V_o/V_i reduces to that given by (1). The expression for ω_U in (5) is identical to the conventional charge amplifier circuit [10]. It can be observed from (6) that C_{p3} has no significant effect on the transfer function for $\omega < \omega_U$ and only has a small influence on the frequency of the pole $\omega_V > \omega_U$.

In the above analysis, it has been assumed that the amplifiers have negligible output resistance. However, it should be borne in mind that the output resistance of the second amplifier will combine with the capacitance of the output cable to form another pole and if this capacitance is particularly large it will reduce the circuit bandwidth. This is also applicable to the unmodified charge amplifier of Fig. (1).

III. Experiment

To confirm the design, the circuit was experimentally investigated with a fixed value of $C_x = 1.1$ pF and with decreasing values of $C_f < C_x$. A CA3140 was used for the unity gain buffer amplifier ($\omega_1/2\pi = 4.5$ MHz) and an OPA637 was used for the second amplifier ($\omega_2/2\pi = 80$ MHz). It was necessary, due to the smallness of C_f, to change R in Fig. 2 to a Tee-network comprising of R_1, R_2, R_3, C_2 and C_3, shown in Fig. 3. This has an effective dc resistance $R_1 + R_2 + R_1R_2/R_3 \sim 1$ GΩ. The purpose of $C_3 = 1$ μF is to make the impedance of this Tee-network large as the frequency increases so that the feedback impedance is determined by C_f rather than the Tee-network. Without C_2, the impedance of this network increases linearly with ω above a break frequency given by $1/R_3C_3$. Unfortunately without C_2 a large resonant peak in the gain occurs at a frequency ω_o given by

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_3C_f}} \tag{7}$$

$$\frac{V_O}{V_i} = \frac{-\frac{C_X}{C_f}}{\frac{1}{s\mathrm{RC}_f} + \frac{1}{\omega_2\mathrm{RC}_f} + 1 + \frac{s}{\omega_2}\left(\frac{C_X + C_f + C_{p2}}{C_f}\right) + \frac{s^2}{\omega_1\omega_2}\left(\frac{C_X + C_f + C_{p2} + C_{p3}}{C_f}\right)} \tag{3}$$

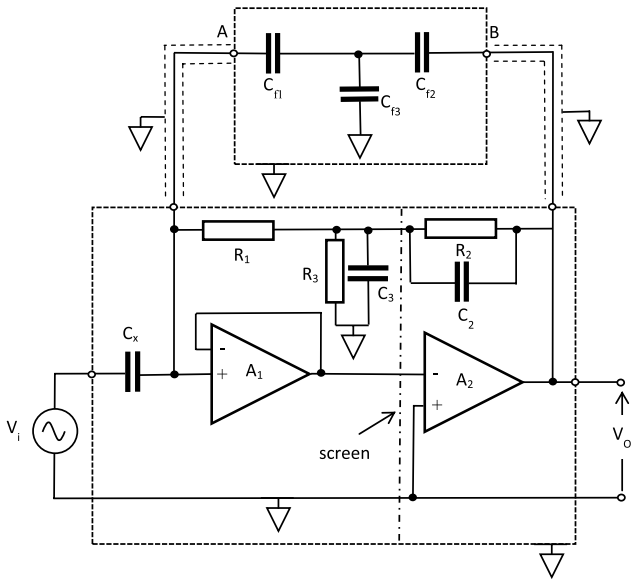

Fig. 3. Test circuit used to verify the modified stray immune capacitance meter. C_x = 1.1 pF. $R_1 = R_2 = 10$ MΩ. $R_3 = 100$ kΩ. $C_3 = 1$ μF. $C_2 = 100$ pF. $C_{f1} = C_{f2} = 2.2$ pF. C_{f3} see text.

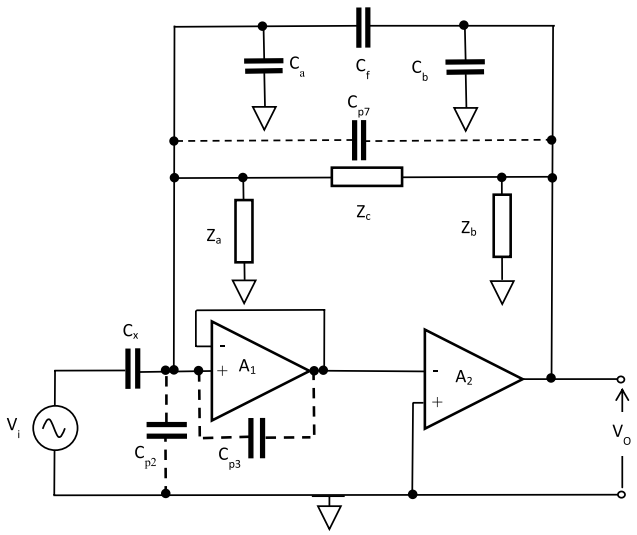

Fig. 4. Test circuit with Tee networks transformed to Pi networks. Parasitic capacitances C_{p2}, C_{p3} and C_{p7} also shown.

and the circuit becomes only marginally stable. A compensating capacitor C_2 was therefore introduced to reduce this effect. To produce small values for C_f a Tee-network of capacitors was formed by C_{f1}, C_{f2} and C_{f3} in a small screened box, as shown in Fig. 3. C_{f1} and C_{f2} were fixed at 2.2 pF and C_{f3} was increased to reduce the effective feedback capacitance C_f. Transforming the two Tee networks to Pi networks gives the equivalent circuit shown in Fig. 4 with the following formulas of the transformed components:

$$C_f = \frac{C_{f1}C_{f2}}{C_{f1}+C_{f2}+C_{f3}} \tag{8}$$

$$C_a = \frac{C_{f1}C_{f3}}{C_{f1}+C_{f2}+C_{f3}} \tag{9}$$

$$C_b = \frac{C_{f2}C_{f3}}{C_{f1}+C_{f2}+C_{f3}} \tag{10}$$

$$Z_a = \frac{R_1R_2\,(1+s\tau_3)+R_1R_3\,(1+s\tau_2)+R_2R_3}{R_2(1+s\tau_3)} \tag{11}$$

$$Z_b = \frac{R_1R_2\,(1+s\tau_3)+R_1R_3\,(1+s\tau_2)+R_2R_3}{R_1(1+s\tau_3)\,(1+s\tau_2)} \tag{12}$$

$$Z_c = \frac{R_1R_2\,(1+s\tau_3)+R_1R_3\,(1+s\tau_2)+R_2R_3}{R_3(1+s\tau_2)} \tag{13}$$

where $\tau_2 = R_2C_2$ and $\tau_3 = R_3C_3$. Impedance Z_b and capacitor C_b are across the output of the second op-amp and have no effect on the circuit's performance as they are again driven by the low impedance output of the second op-amp. Z_a and C_a are in parallel with C_{p2}. The transfer function is now given by (14), which is shown at the bottom of the page.

The conditions for (14) reducing to (1) are slightly more involved. For $\omega > 1/\tau_2 = 10^3$ rads. s^{-1} and $\omega > 1/\tau_3 = 10$ rads. s^{-1}, then $Z_a \sim R_1 \sim 10^7$ Ω and $Z_c \sim R_1C_3/C_2 \sim 10^{11}$ Ω. We require $\omega \gg 1/C_fZ_c$, $\omega \ll \omega_U$ where now $\omega_U = \omega_2 \cdot C_f/(C_x + C_f + C_{p2} + C_a)$ and $1 \gg 1/\omega_2C_f\ (1/Z_c + 1/Z_a)$. Since $Z_C \gg Z_a$ this last condition is approx. $1 \gg 1/\omega_2Z_aC_f$, which sets a lower limit on $C_f \gg 1/\omega_2Z_a \sim 0.2$ fF for the op-amp and resistive feedback network used. The condition $\omega \gg 1/C_fZ_c$ sets a lower limit on $C_f \gg 1/\omega Z_c \sim 0.16$ fF for measurements at 10 kHz with the resistive feedback network used. The condition $\omega \ll \omega_U$ is the most demanding, which implies $C_f \gg \omega(C_x + C_{p2} + C_a)/\omega_2 \sim 1$ fF for measurements at 10 kHz.

Parasitic C_{p7} can be included in (14) by replacing C_f by $C_f + C_{p7}$. Parasitic C_{p7} will include the small parasitic capacitance between the terminals A and B within the screened box shown in Fig. 3 containing C_{f1}, C_{f2} and C_{f3}.

Three circuits were constructed and tested. Circuit A consisted of the circuit shown in Fig. 3 including the electrostatic screen shown by the dash-dot line between the two operational amplifiers, which were on separate circuit boards. Circuit B consisted of the circuit shown in Fig. 3 without the electrostatic screen and with both operational amplifiers on the same circuit board, and finally circuit C consisted of the circuit of Fig. 3 without the screen and without the unity gain buffer amplifier. Basic wire ended components were used in the construction and the amplifiers were eight pin DIL versions. The same components were used for C_{f1}, C_{f2} and C_{f3} for each of the three circuits to aid the comparison.

$$\frac{V_O}{V_i} = \frac{-\frac{C_X}{C_f}}{\frac{1}{sC_fZ_c} + 1 + \frac{1}{\omega_2C_f}\left(\frac{1}{Z_c}+\frac{1}{Z_a}\right) + \frac{s}{\omega_2}\left(\frac{C_X+C_f+C_{p2}+C_a}{C_f}\right) + \frac{s}{\omega_1\omega_2}\frac{1}{C_f}\left(\frac{1}{Z_c}+\frac{1}{Z_a}\right) + \frac{s^2}{\omega_1\omega_2}\left(\frac{C_X+C_f+C_{p2}+C_a+C_{p3}}{C_f}\right)}. \tag{14}$$

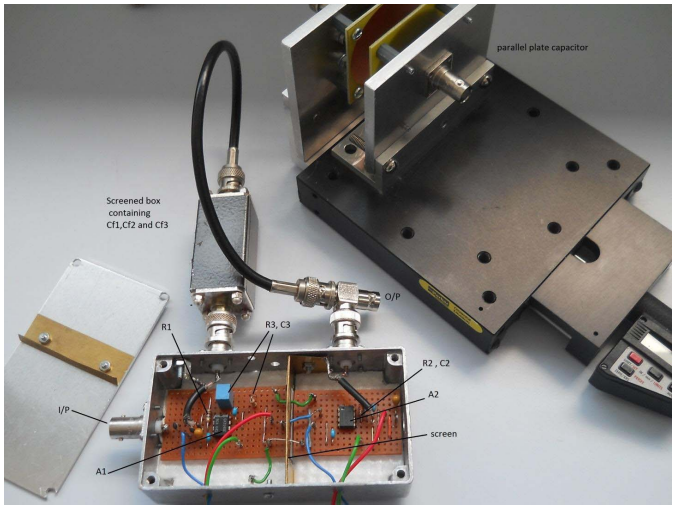

Fig. 5. Photograph showing circuit A together with screened box containing C_{f1}, C_{f2} and C_{f3}. The parallel plate capacitor is also shown.

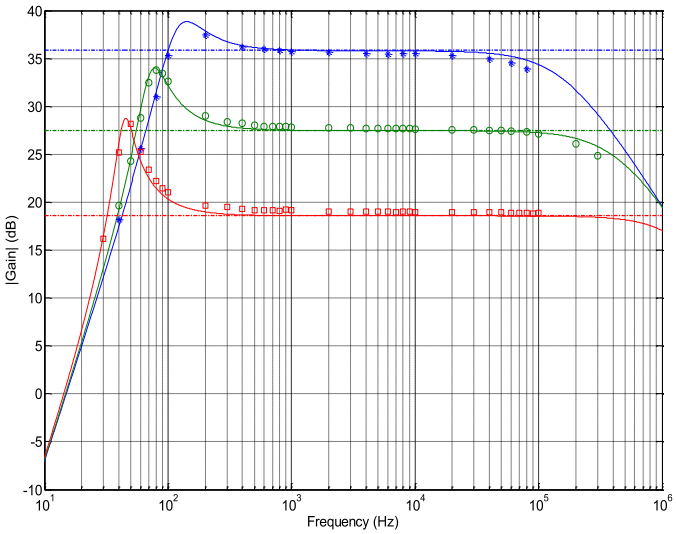

Fig. 6. Measured modulus of gain *vs* frequency for circuit in Fig. 3. (circuit A) for three values of C_f (□ $C_f = 129.4$ fF, ◯ $C_f = 46.4$ fF, * $C_f = 17.6$ fF) Solid lines are generated using (14) with $C_{p2} = 6$ pF and $C_{p3} = 0$ pF Dash horizontal lines are the ratio (C_x/C_f) with $C_x = 1.1$ pF.

Hence, differences in the performance of the three circuits cannot be ascribed to the tolerances of these particular components. Fig. 5 shows the experimental arrangement for circuit A. The capacitive Tee-network C_{f1}, C_{f2} and C_{f3} is contained within the external screened box.

Fig. 6 compares the measured and theoretical modulus of the frequency response, using (14), for circuit A for three values of C_f. Parasitic capacitance C_{p2} is unknown but only affects the location of the high frequency cut-off and was adjusted to give the curves shown in Fig. 5. Its value was 6 pF, which is a few pFs higher than the quoted input capacitance of the CA3140. The dashed horizontal line on each curve is the ratio C_x/C_f in dB. It can hence be observed that the mid frequency gain of the amplifier is determined simply by this ratio as predicted.

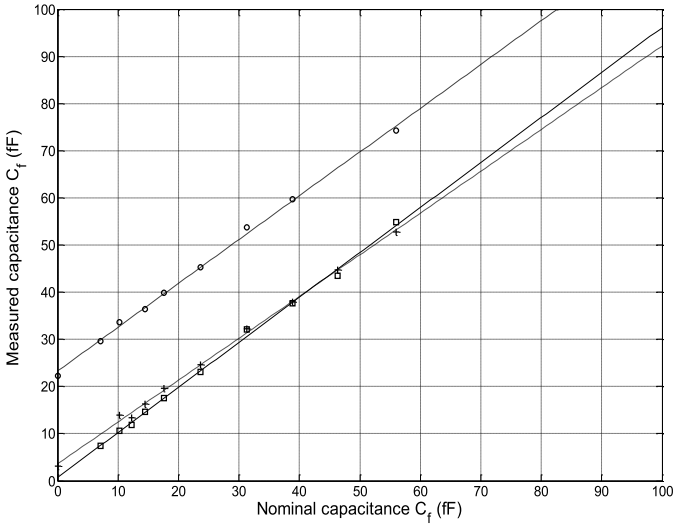

Fig. 7. Measured capacitance versus nominal feedback capacitance (C_f) for the three circuits. □ circuit A, + circuit B, and ◯ circuit C.

Fig. 7 shows a plot of the measured C_f, as determined from the modulus of the gain at 10 kHz, plotted as a function of the nominal value of C_f, as calculated from (8), for all thee circuits. Ideally, the slope of these lines should be unity. Any differences in the slope can be attributed to the tolerance of C_x and the parasitic capacitance across it. Any vertical offset can be attributed to the parasitic capacitance in parallel with C_f, i.e., C_{p7} in Fig. 3 for circuits A and B and C_{p3} in Fig. 1 for circuit C. For circuit A, the linear relationship between the nominal and measured C_f has a gradient of 0.953 and more importantly, when extrapolated, passes almost though the origin with an off-set of only 0.75 fF. For circuit B, the line has a gradient of 0.886 and has a small off-set ~3.6 fF. Finally, for the single op-amp circuit, circuit C, the line has a gradient of 0.928 and has an off-set of ~24 fF, which we ascribe to C_{p3}. It can hence be observed that the biggest reduction in the off-set is between the circuits B and C, the difference between these two circuits being the introduction of the unity gain buffer amplifier. A very small further decrease can be achieved by the introduction of the electrostatic screen. One likely cause of the final small off-set of circuit A is the internal stray capacitance associated between the terminals A–B in the box containing C_{f1}, C_{f2} and C_{f3}. It should be borne in mind that using different components packages for the op-amps and construction methods will result in different off-set values.

As a further demonstration of the performance of the improved circuit, the capacitive Tee-network in circuit A is replaced by a parallel plate capacitor with a guard ring [8]. This is shown in Fig. 5. The plate separation distance d is controlled by a translation stage and measured with a Vernier. The plate connected to the input of the unity gain buffer A_1 has a radius $r_1 = 2.5$ mm. The guard ring surrounding it, which is connected to ground, has an inner radius is $r_2 = 2.75$ mm and an outer radius of 24 mm. The other plate, which also has a radius of 24 mm, is connected to the second op-amp output. Hence, we have a feedback capacitance given

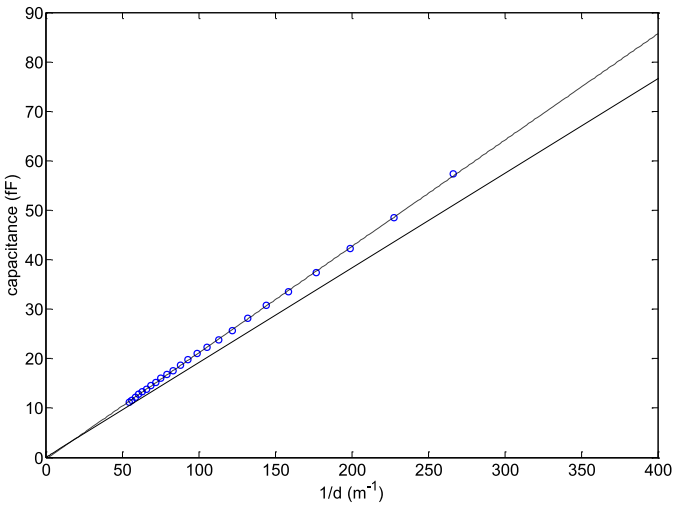

Fig. 8. Capacitance for parallel plate capacitor with guard ring. Solid line: (15). Dashed line: linear fit to data.

approximately by

$$C_f \cong \frac{\varepsilon_0 \pi \ (r_1 + r_2)^2}{4d}. \tag{15}$$

Fig. 8 shows the measured C_f for circuit A as a function of $1/d$. The solid line is the theoretical value deduced from (15) with a slope of 0.192 fFm. The measured capacitance follows nearly a straight line with $1/d$ and has a slope of 0.215 fFm. The difference in slope between the data and theoretical curve are likely to be caused by the tolerance in C_x and the approximate construction of the parallel plate capacitor. However, the important point is that extrapolation of the experimental data toward the origin indicates that the parasitic capacitance in parallel with C_f is very small <1 fF.

IV. Conclusion

It has been shown both theoretically and experimentally that the stray immune ac capacitance circuit can be modified by the introduction of a unity gain buffer amplifier within the loop. This reduces errors caused by the parasitic capacitance across the feedback capacitance C_f. It has utility when either C_x is the unknown capacitance and C_f is small or when C_x is fixed and C_f is a small unknown capacitance.

References

[1] S. M. Huang, A. L. Scott, R. G. Green, and M. S. Beck, "Electronic transducers for industrial measurement of low value capacitances," *J. Phys. E, Sci. Instrum.*, vol. 21, no. 3, pp. 242–250, 1988.

[2] R. F. Wolffenbuttel and P. P. L. Regtien, "Capacitance-to-phase angle conversion for the detection of extremely small capacities," *IEEE Trans. Instrum. Meas.*, vol. 36, no. 4, pp. 868–872, Dec. 1987.

[3] M. Bramanti, "A high sensitivity measuring technique for capacitive sensor transducers," *IEEE Trans. Ind. Electron.*, vol. 37, no. 6, pp. 584–586, Dec. 1990.

[4] D. Marioli, E. Sardini, and A. Taroni, "Measurement of small capacitance variations," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 2, pp. 426–428, Apr. 1991.

[5] A. Ashrafi and H. Golnabi, "A high precision method for measuring very small capacitive changes," *Rev. Sci. Instrum.*, vol. 70, pp. 3483–3487, May 1999.

[6] F. Q. Shao and Q. G. Mong, "A method of measuring low capacitances for tomography," *Rev. Sci. Instrum.*, vol. 70, no. 7, pp. 3177–3179, 1999.

[7] A. Abu-Al-Aish and M. Rehman, "Development of a capacitive mass measuring system," *Sens. Actuators, A*, vol. 151, no. 2, pp. 113–117, 2009.

[8] S. Kuroda, "A simple stray free capacitance meter by using an operational amplifier," *IEEE Trans. Instrum. Meas.*, vol. 32, no. 4, pp. 512–513, Dec. 1983.

[9] T. Eberharter and G. Brasseur, "Improvements of the charge amplifier used in a capacitive angular-position sensor," in *Proc. 2IEEE Instrum. Meas. Technol. Conf.*, Ottawa, Canada, May 1997, pp. 1273–1277.

[10] J. C. Gamio, W. Q. Yang, and A. L. Stott, "Analysis of non-ideal characteristics of an AC-based transducer for tomography," *Meas. Sci. Technol.*, vol. 12, no. 8, pp. 1076–1082, 2001.

[11] L. Malkinski and W. Malkinski, "Electronic system for the measurement of elasticity moduli and internal friction of thin metallic ribbons," *Meas. Sci. Technol.*, vol. 1, no. 3, pp. 277–281. 1990.

[12] J. Wei, C. Yue, M. van der Velden, Z. L. Chen, Z. W. Liu, K. A. A. Makinwa, *et al.*, "Design, fabrication and characterisation of a femto-farad capacitive sensor for pico-liter liquid monitoring," *Sens. Actuators A, Phys.*, vol. 162, no. 2, pp. 406–417, 2010.

[13] F. N. Toth and G. C. M. Meijer, "A low-cost smart capacitive position sensor," *IEEE Trans. Instrum. Meas.*, vol. 41, no. 6, pp. 1041–1044, Dec. 1992.

[14] J. Graham, M. Kryzeminski, and Z. Popovic, "Capacitance based scanner for thickness mapping of thin dielectric films," *Rev. Sci. Instrum.*, vol. 71, no. 5, pp. 2219–2223, 2000.

[15] J. B. Tan and J. N. Cui, "Ultraprecision 3D probing system based on spherical capacitive plate," *Sens. Actuators A, Phys.*, vol. 159, no. 1, pp. 1–6, 2010.

Robert Oven (M'10) has been a Lecturer of electronics with the University of Kent, Canterbury, U.K., since 1986. He has published over 40 refereed papers on ion implantation and more recently on integrated optics and interferometry.