Solid-State Electronics 54 (2010) 243–251

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Quantitative prediction of junction leakage in bulk-technology CMOS devices

R. Duffy [a], A. Heringa [a,*], V.C. Venezia [b,1], J. Loo [c], M.A. Verheijen [d], M.J.P. Hopstaken [d,2], K. van der Tak [d], M. de Potter [c], J.C. Hooker [a], P. Meunier-Beillard [a], R. Delhougne [a]

[a] NXP-TSMC Research Center, Kapeldreef 75, 3001 Leuven, Belgium
[b] Philips Research Leuven, Kapeldreef 75, 3001 Leuven, Belgium
[c] IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[d] Philips Research Laboratories Eindhoven, High Tech Campus 11, 5656 AE Eindhoven, The Netherlands

ARTICLE INFO

Article history:
Received 13 March 2009
Received in revised form 20 August 2009
Accepted 8 September 2009
Available online 17 October 2009

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Diode
Leakage
CMOS
Tunneling

ABSTRACT

Junction leakage becomes more significant as metal-oxide-semiconductor (MOS) technologies scale down in bulk-silicon. In this work we quantify the four key elements to junction leakage generation through a combination of experiment and device simulation. These elements are: (i) ultra-shallow junction steepness, (ii) channel and pocket concentrations, (iii) junction curvature, and (iv) the presence of residual defects. We first characterize n^+/p and p^+/n diodes to quantify how changes in doping profiles affect reverse bias leakage. Diodes with end-of-range (EOR) silicon defects intentionally located in the junction depletion region are also characterized to quantify their contribution. This feeds into a device simulation study to gain insight in the experimental results and in the capabilities of available physical models. Thereafter simulation is used to predict leakage in future generation bulk-silicon MOS devices. In summary, band-to-band tunneling (BBT) due to aggressively scaled doping profiles and trap-assisted tunneling (TAT) due to the increased presence of defects make off-state low-standby-power leakage targets difficult to meet. With the increase of junction leakage from aggressively scaled ultra-shallow junctions, the assumption that the subthreshold leakage component dominates off-state current is no longer valid.

1. Motivation

Leakage currents in MOS devices are undesirable as they drain power supply resources in integrated circuits and systems. The International Technology Roadmap for Semiconductors [1] (ITRS) specifies leakage targets for current and future generation MOS technologies. Literature on diode leakage has been available for many decades now. However there are a number of aspects of modern MOS device processing and design that necessitate an updated study on junction leakage. For example previous work is almost exclusively devoted to investigations in one dimension. If the device is primarily one-dimensional (1D), such as in a large area diode, that is sufficient. This approach is not always reliable if you consider a two-dimensional (2D) problem, namely the junction in a MOS transistor, where the curvature of the junction significantly affects the electric field (E_{FIELD}): sharper curvature leads to higher E_{FIELD}. In this paper, extended 1D experimental analysis is presented, and the 2D problem is explored through predictive device simulation.

Furthermore we have entered an era where bulk-silicon MOS devices require relatively high channel doping concentrations. With increased background concentrations, additional leakage effects potentially exist that did not require consideration before. Recently Solomon et al. [2] provided an extensive study of BBT, through a diode experiment that had background doping concentration as one of the variables. The relationship between tunneling current and effective tunneling distance was examined. In that work the emphasis was on establishing tunneling parameters rather than on the study of field-effect-transistors.

There has been growth in popularity of advanced annealing techniques such as flash, laser, and solid-phase-epitaxial-regrowth (SPER), which can place impurity atoms on substitutional sites in the silicon lattice to extremely high concentrations [3–5]. The drawback is that they can leave residual damage in the silicon substrate [6–8]. These disturbances create localized energy levels in the silicon band gap, and if located in or close to the space charge depletion region they may act as centers for carrier generation or recombination events. In fact carrier lifetimes and non-ideal leakage currents can be considered as an effective monitor for process induced defects and for the processing history of the junction [9,10].

* Corresponding author. Tel.: +32 16 28 1028; fax: +32 16 28 7588.
E-mail address: anco.heringa@nxp.com (A. Heringa).
[1] Present address: OmniVision Technologies Inc., 1341 Orleans Drive, Sunnyvale, CA 94089, United States.
[2] Present address: IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, United States.

0038-1101/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2009.09.007

The variables in our experimental work were junction type (n^+/p and p^+/n), doping species (boron, arsenic, and phosphorus), and the presence and position of intentional residual defects. Electrical characterization involved the extraction of current–voltage relationships and temperature dependence of the diodes. Thereafter the fabricated diodes were subjected to a deprocessing step where the contact metallization was removed. For material characterization we used secondary ion mass spectrometry (SIMS) analysis to extract doping profiles, and Transmission Electron Microscopy (TEM) to image crystal defects. The SIMS profiles were input into a well-established simulation tool (MEDICI [11]) to enable a closer evaluation of the measurements and to validate the accuracy of device simulation models.

2. Experimental

A simple process was defined to fabricate the diodes with relatively deep junctions. Due to the metallization removal inaccuracies in the SIMS analysis close to the surface were expected. To ensure accurate SIMS profiling at the metallurgical junction, a junction depth of >150 nm was targeted. For most diodes the high-concentration profile was implanted shallow (projected range ~20 nm) and diffused into position by a high-temperature drive-in anneal. Thus the damage from this implant is located near the surface, where it is likely to be annihilated. The low-concentration profile was implanted thereafter. A high temperature spike anneal was performed to remove the damage from the low-concentration profile implant. The activation of this profile should be high because: (i) the low concentrations are well within the solid solubility limits [12] after the high temperature anneal, (ii) the low dopant concentration reduces the risk of deactivation driven by dopant clustering, (iii) the implant damage from the low dose implant is small.

The process flow consisted of standard processing to define the active area and poly-buffered LOCOS isolation on ⟨100⟩ oriented 200 mm Czochralski silicon wafers. The starting resistivity was 12 and 20 Ω cm for n-type and p-type wafers respectively. These high quality wafers contained oxygen concentrations of $\sim 5 \times 10^{17}\,cm^{-3}$, carbon concentrations of $\sim 5 \times 10^{16}\,cm^{-3}$, and $<10^{11}\,cm^{-3}$ for other contaminants such as iron, zinc, copper, and nickel. A 5 nm screen oxide was deposited before the implants and anneals. Details of the implants and anneals are available in Table 1.

For the n^+/p diodes, high-concentration arsenic was implanted shallow and driven-in by a 1100 °C 5 min anneal. Thereafter the low-concentration profile was formed by a boron implant. A spike anneal at 1100 °C was used to activate the boron. For the n^+/p diodes with EOR defects intentionally located in the depletion region, the high-concentration profile was implanted deep into a preamorphized layer formed by high dose silicon implants. In this case the arsenic profile was implanted into position instead of being driven-in, because we wanted to avoid annihilating the EOR defects completely. An additional low-energy arsenic implant was included to ensure a high concentration at the surface for a good electrical contact. For the p^+/n diodes one anneal was sufficient for both drive-in of the p^+ profile and activation of the n profile, due to the relatively high diffusivity of boron. The activation/drive-in anneal was 1050 °C 10 s. The rest of the flow consisted a clean step to remove the screen oxide, and the deposition of a Ti/TiN contact layer. Finally a 650 nm layer of AlCu metal was deposited and patterned.

Current–voltage characteristics were measured using a HP4155 parameter analyzer. A thermochuck was used to investigate temperature dependency. For each structure and split, several die were measured. The within-wafer reproducibility of the measurements was good, as there was little spread from die to die. Most of the measurements were done on large area square diodes. Perimeter current was extracted from meander structures. In all square diodes the perimeter component was several orders of magnitude lower than the area contribution.

After electrical characterization of the diodes, the contact metallization was removed by using a standard Al etch followed by a standard Ti etch. Impurity profiles were then determined by SIMS analysis using 3 keV O_2^+ primary ions. TEM cross-section and plan-view samples were prepared by mechanical polishing down to electron transparency. The TEM studies were performed on a Tecnai F30ST TEM operated at 300 kV. Off-axis diffraction contrast imaging was performed with a tilt of 1.5°. The local thickness of the TEM sample was determined using energy filtered TEM.

3. Electrical results

3.1. Definitions

Generation mechanisms that lead to leakage currents are temperature and/or E_{FIELD} dependent. To extract the dominant mechanisms we need to analyze: (a) the voltage dependence and (b) the temperature dependence of the leakage current [13,14]. The relevant mechanisms are diffusion current, Shockley Read Hall (SRH) generation, TAT, and BBT. Obviously the total leakage current is the sum of all component parts

$$I_{leak} = I_{diffusion} + I_{SRH} + I_{TAT} + I_{BBT} \quad (1)$$

and the leakage current activation energy (E_A) is function of the component parts and their E_A values

$$E_{A\_leak} = f((I,E_A)_{diffusion},(I,E_A)_{SRH},(I,E_A)_{TAT},(I,E_A)_{BBT}). \quad (2)$$

Ideal diffusion current is proportional to n_i^2, where n_i the intrinsic carrier concentration. The temperature dependence behavior is related to the temperature dependence of n_i which is proportional to $\exp(-\frac{E_G}{2kT})$, where E_G is the band gap of silicon. Thus $I_{diffusion}$ is proportional to $\exp(-\frac{E_G}{kT})$, and E_A expected to be 1.12 eV.

SRH generation is temperature dependent and relies on the presence of deep levels in the depletion region. It occurs when

Table 1
Implant and anneal details for the diodes discussed in this work.

	n^+/p Diodes	n^+/p Diodes with intentional defects	p^+/n Diodes
High conc. profile	As $6 \times 10^{15}\,cm^{-2}$ 10 keV	As $1 \times 10^{15}\,cm^{-2}$ 10 keV As $4 \times 10^{15}\,cm^{-2}$ 180 keV	B $5 \times 10^{15}\,cm^{-2}$ 5 keV
Drive in anneal	1100 °C 5 min	–	–
Low conc. profile	*AB1*: B $2.0 \times 10^{14}\,cm^{-2}$ 100 keV *AB2*: B $9.3 \times 10^{13}\,cm^{-2}$ 100 keV *AB3*: B $4.3 \times 10^{13}\,cm^{-2}$ 100 keV *AB4*: B $2.0 \times 10^{13}\,cm^{-2}$ 100 keV *AB1-5*: B $1.2 \times 10^{13}\,cm^{-2}$ 180 keV	B $2.0 \times 10^{13}\,cm^{-2}$ 100 keV	*BA1*: As $9.3 \times 10^{13}\,cm^{-2}$ 250 keV *BA2*: As $4.3 \times 10^{13}\,cm^{-2}$ 250 keV *BA3*: As $2.0 \times 10^{13}\,cm^{-2}$ 250 keV *BA4*: As $1.0 \times 10^{13}\,cm^{-2}$ 250 keV *BA1-4*: P $2.0 \times 10^{13}\,cm^{-2}$ 230 keV
Activation anneal	1100 °C spike RTA	1100 °C spike RTA	1050 °C 10 s

an electron that is trapped in a deep level, gains energy, and climbs out of the Coulombic well. Assuming the trap level population is dominated by mid-gap states, SRH generation is proportional to n_i. The temperature dependence behavior is thus related to the temperature dependence of n_i, so I_{SRH} is proportional to $\exp(-\frac{E_G}{2kT})$, and E_A is expected to be 0.56 eV. SRH dominated current is proportional to the width of the depletion region and thus proportional to $V^{0.5}$, assuming a one-sided step junction.

TAT can be considered as SRH in the presence of an E_{FIELD}, or as a combination of electron capture and tunneling through the barrier. In this case the tunneling electron uses a deep level trap in the depletion region as a stepping stone to make the transition. TAT is also temperature dependent and E_A will indicate a trap level within the band gap. Like SRH this value is usually mid-gap, however TAT voltage dependence is V^X, where X is greater than 0.5.

BBT occurs when the E_{FIELD} across the junction is strong enough to propel an electron from the valence band on the p-side through the forbidden band gap, into the conduction band on the n-side. BBT in a diode is described as being proportional to $\exp\left(-\frac{E_G^{1.5}}{E_{FIELD}^{max}}\right)$, where E_{FIELD}^{max} is the maximum electric field [15]. The probability of BBT increases if the E_{FIELD} increases or if the tunneling distance decreases. Hurkx et al. reported that BBT becomes important above a local electrical field strength of 7×10^5 V/cm [16]. The temperature dependence of BBT is related to the temperature dependence of E_G. As a rule of thumb, BBT increases approximately 2× for a 100 °C increase above room temperature [15], so E_A is close to 0 eV.

At low forward biases the ideality of the junction can be determined from the slope of the current–voltage characteristics. In the ideal case the slope is $\frac{q}{kT}$, but in the non-ideal case in the presence of recombination centers in the depletion region, the slope is $\frac{q}{nkT}$, with $n > 1$. This parameter n is known as the ideality factor.

Note, the concept "background concentration" discussed in our diode experiments, is analogous to the channel and pocket concentrations in a CMOS device.

3.2. n^+/p Diodes

Arsenic/Boron (AB) diodes are presented in this section. These are labeled AB1, AB2, AB3, AB4, and AB5, according to the variation in boron concentration. Diode AB1 has the highest boron concentration, diode AB5 has the lowest. Shown in Fig. 1 are SIMS depth profiles for the five diodes. The arsenic profile is the same for all cases. The shape of the boron profile near the junction is affected by the high-concentration arsenic. Boron is known to migrate to the n^+ region due to the associated electric field. Due to the chemistry of the metal strip the near-surface boron SIMS were noisy and untrustworthy. As this was a function of the deprocessing rather than being present in the actual devices electrically characterized, this portion of the SIMS is omitted to avoid confusion. Finally, the boron concentrations at the junction are 6.1×10^{18}, 3.9×10^{18}, 1.9×10^{18}, 7×10^{17}, and 1×10^{17} cm^{-3} for diodes AB1–AB5 respectively.

Fig. 2 shows the corresponding forward and reverse bias current density as a function of applied bias voltage. Measurements were performed with the thermochuck temperature set to 25 °C. Current density increases with reverse bias as expected, due to the increase in the depletion layer width and the increase of the local E_{FIELD}. Clearly as the background boron concentration increases, the reverse bias leakage also increases. For <2 orders of magnitude increase in boron concentration, the current density at 1 V increases by ~8 orders of magnitude.

Analyzing the forward characteristics in Fig. 2 the n values for AB1–AB5 are 2.77, 2.55, 1.07, 1.03, and 1.01 respectively. With n close to 1, diodes AB3–AB5 exhibit close to ideal behavior. Note that the reverse current density for these diodes spans several orders of magnitude (seven orders at 5 V) despite only a small change in ideality factor. The highly non-ideal behavior for diodes AB1 and AB2 is a surprising result as these diodes were fabricated in such a way so as to avoid the presence of non-idealities, like residual crystal damage, after the final anneal step. The arsenic profile was implanted shallow and driven-in using a high thermal budget anneal. Thus the source of non-ideality can only stem from the boron profile. Boron is a light ion and is not expected to generate high levels of damage, thus the likelihood of residual EOR defects is low. If present after the high temperature anneal they should have evolved into easily visible dislocation loops. At these boron concentrations, 1100 °C is expected to remove other known defects such as boron-interstitial clusters. Cross sectional TEM

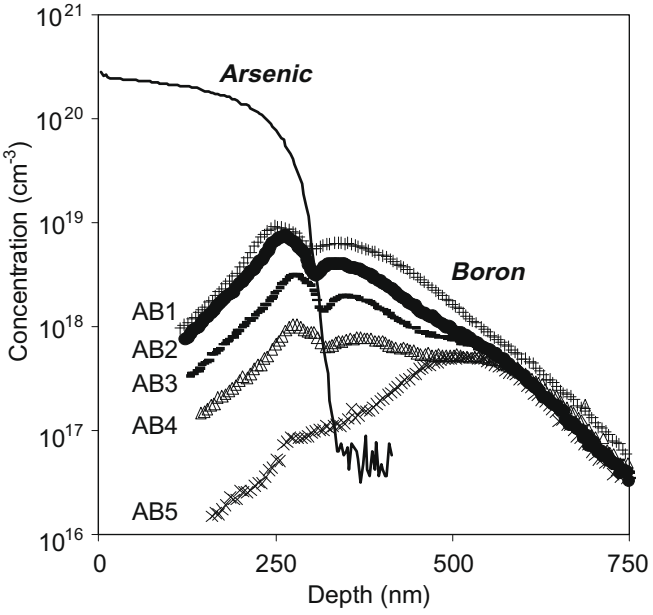

Fig. 1. SIMS depth profiles of arsenic and boron for the diodes AB1–AB5.

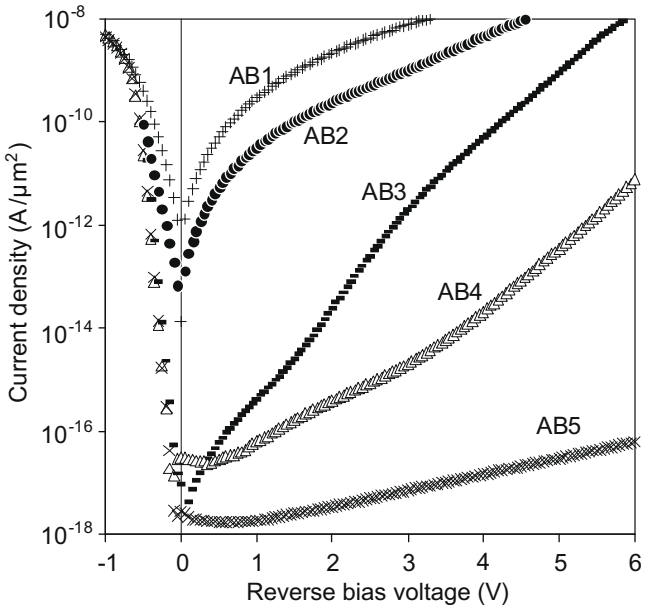

Fig. 2. Forward and reverse current density versus bias, for the diodes AB1–AB5, corresponding to the SIMS depth profiles in Fig. 1.

(XTEM) analysis was performed on the diodes AB1 and AB2, to search for EOR defects and precipitates, but none were found. Note increased ideality factor with increased background concentrations has been previously reported for n^+/p (phosphorus/gallium) diodes [17] and for p^+/n (boron/phosphorus) diodes [18].

The thermochuck temperature was then ramped between 25 °C and 105 °C, in 10 °C steps. To avoid a busy looking graph, a selection of results is shown in Fig. 3. At higher temperatures the reverse leakage is greater. Diode AB1 exhibits very little temperature dependency. This indicates an E_{FIELD} dominated leakage mechanism. Diode AB5 on the other hand shows a strong temperature dependency. Diode AB3 is somewhere in-between as there is temperature dependence at low biases and temperature independence at high biases. Hurkx et al. reported a similar temperature dependence for p^{++}/n^+ Zener diodes with 3 different background concentrations [19].

Using the temperature dependency measurements of Fig. 3 for each diode, the leakage current was plotted as a function of $\frac{1}{kT}$ for biases between 0.5 and 6 V, and E_A was extracted. For diodes AB1–AB4 only one E_A was extracted per bias value as the current versus $\frac{1}{kT}$ plot produced a straight-line, but for diode AB5 there were different E_A values at high and at low temperatures. E_A versus reverse bias voltage is plotted in Fig. 4. For diodes AB1 and AB2 $E_A \sim 0$ eV for all biases which is an indication that the leakage currents are dominated by E_{FIELD} mechanisms (BBT). For diode AB3, $E_A = 0.4$ eV at 0.5 V and drops to 0 eV as the reverse bias increases. This indicates that the E_{FIELD} mechanisms do not fully dominate at low biases, but BBT becomes more significant as the voltage is increased. It is a similar story for diode AB4. For AB5 at high measurement temperatures (65–105 °C) diffusion current is evident as $E_A = 1.2$ eV. This is consistent with the reported results of Tamai et al. [20]. At low measurement temperatures (25–55 °C) $E_A \approx E_G/2$, but the SRH signature is not evident, as $I \propto V^{2.7}$ at 25 °C, so we conclude that TAT is dominant with a mid-gap trap level. The inset of Fig. 4 shows E_A of reverse leakage at 1 V as a function of background concentration for all the diodes in this work. The legend of the inset refers the doping species (high concentration/low concentration). E_A falls as concentration increases, from ~0.8 eV at 7×10^{17} cm^{-3}, to ~0 eV at 6×10^{18} cm^{-3}. This confirms that BBT will increase and start to dominate as background doping levels are increased, for a fixed bias.

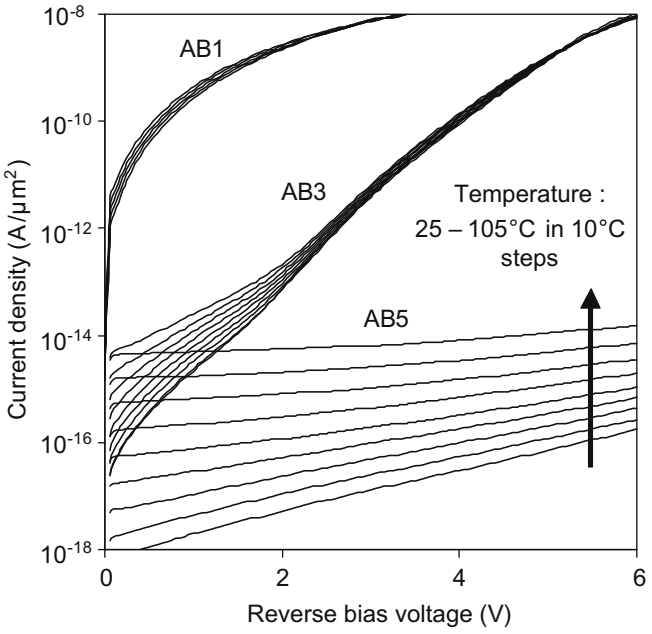

Fig. 3. Reverse current density versus reverse bias, with temperature varied between 25 °C and 105 °C. For clarity only diodes AB1, AB3, and AB5, are shown.

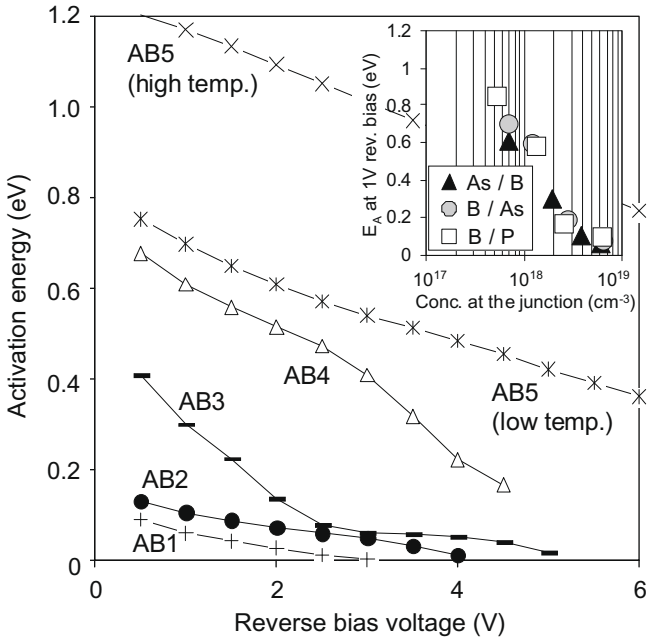

Fig. 4. Activation energy of the current density characteristics versus reverse bias for the diodes AB1–AB5. For AB5 low temperatures are 25–55 °C, and high temperatures are 65–105 °C. The inset shows activation energy of the current density at 1 V reverse bias versus background concentration at the junction for both n^+/p and p^+/n diodes.

3.3. p^+/n Diodes

Boron/Arsenic and Boron/Phosphorus p^+/n diodes were characterized in the same way as the Arsenic/Boron n^+/p diodes. Since the analysis and conclusions are similar, a shorter version will be presented here.

The Boron/Arsenic (BA) diodes are labeled BA1, BA2, BA3, and BA4, according to the variation in arsenic concentration. Shown in Fig. 5 are SIMS depth profiles for the four diodes. The boron profile is the same for all cases. The arsenic concentrations at the junction are 6.4×10^{18}, 2.8×10^{18}, 1.2×10^{18}, and 6.8×10^{17} cm^{-3} for diodes BA1–BA4 respectively. The inset of Fig. 5 shows the corresponding forward and reverse bias current density as a function of applied bias voltage. From the forward characteristics, the n values for BA1–BA4 are 2.39, 1.96, 1.04, and 1.01 respectively. With n close to 1, diodes BA3 and BA4 exhibit close to ideal behavior. With $n > 2$ in diode BA1, severe non-ideal behavior is evident. Like the n^+/p case these diodes were fabricated in such a way to avoid the presence of residual non-idealities. For ~1 order of magnitude increase in arsenic concentration, the reverse current density at 1 V increases by ~7 orders of magnitude. For diodes BA1 and BA2, $E_A \sim 0$ eV for all biases which is an indication that the leakage currents are dominated by E_{FIELD} mechanisms such as BBT. For diode BA3, $E_A = 0.75$ eV at 0.5 V and drops toward 0 eV as the reverse bias increases. For diode BA4 at high temperatures (65–105 °C) diffusion current is evident as $E_A = 1.2$ eV. At low temperatures (25–55 °C) $E_A \approx E_G/2$ is observed, but the SRH signature is not evident, as $I \propto V^{1.9}$ at 25 °C, so we conclude that TAT is dominant with a mid-gap trap level.

Similar results were obtained for p^+/n diodes with phosphorus as the background dopant species. The phosphorus concentrations at the junction were 6.3×10^{18}, 2.6×10^{18}, 1.3×10^{18}, 5×10^{17}, and 5×10^{16} cm^{-3}, resulting in n values of 2.41, 1.89, 1.04, 1.00,

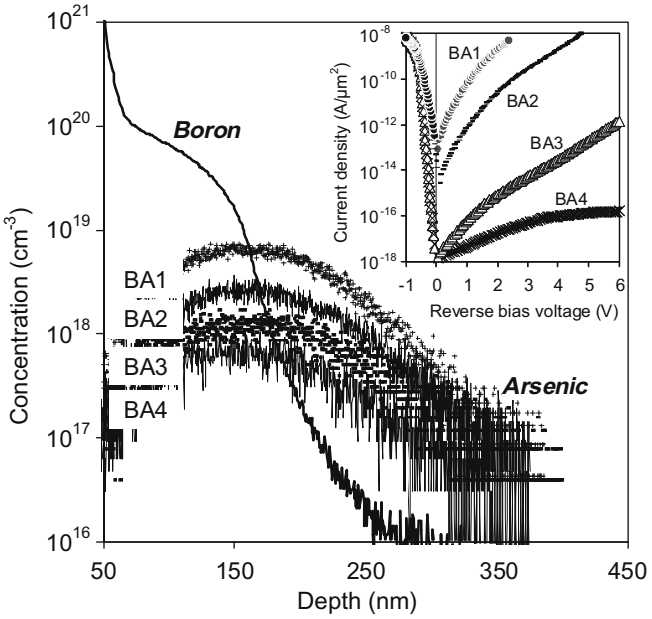

Fig. 5. SIMS depth profiles of boron and arsenic for the diodes BA1–BA4. The inset shows the corresponding forward and reverse current density versus bias characteristics.

1.03. For the sake of brevity the details are reported elsewhere [21].

3.4. Diodes with intentional EOR defects

Arsenic/Boron diodes with defects (ABD) show the dependency of leakage on residual process induced defects. Junction leakage has been studied in the presence of intentional EOR defects previously, for example in p^+/n diodes with a silicon preamorphization implant (PAI) [22–24], with a germanium PAI [25–27], or with a tin PAI [28,29], and in n^+/p diodes with a self-amorphizing implant [30], or with a germanium PAI [27]. Recently junction leakage variations in the presence of EOR defects have been presented in flash anneal [7] and laser anneal [31] studies.

Studying the defect contribution is complicated if the doping profile of the junction is not extracted. Changing the type or position of an EOR defect band will inevitably change the shape and/or slope of the doping profile at the junction also. By extracting the profile, the doping contribution to leakage can be filtered out to more accurately quantify the defect contribution. The experimental variable here is the location of the EOR defect band. The arsenic and boron doping implants were kept constant in this investigation. The diodes in this section are labeled ABD1, ABD2, and ABD3, according to the variation in position of the EOR defect band. Details of the defect density as well as depth and width of the defect band can be found in Table 2. Fig. 6a shows the SIMS profiles for these diodes.

Representative XTEM images of the diodes can be seen in Fig. 6b–d. Threading dislocations (hairpin defects) are visible in the regrown layer. A rough amorphous/crystalline interface after preamorphization can lead to hairpins [32,33]. Chen et al. [34] showed some clear XTEM images of such defects, for silicon samples preamorphized to a depth of 440 nm. For diode ABD3 the defect density in the EOR band could not be determined due to overlap of the two different defect types in the projected image.

Table 2 also shows a summary of the electrical analysis of diodes ABD1–3, along with the corresponding case without defects, diode AB4, which has the same boron concentration at the junction. The addition of defects has increased the leakage current density, which agrees with previous studies on leakage in p^+/n diodes [35–37]. The increase is greater at low E_{FIELD} (1 V) compared to at high E_{FIELD} (5 V). For diodes ABD2 and ABD3 the defect band is located deeper than the junction and at 1 V reverse bias the increase in leakage is more than three orders of magnitude. E_A is close to mid-gap, thus TAT is the dominant mechanism. The same E_A for ABD1–3 indicates that the defect band depth has little qualitative impact on the generation mechanism. At 5 V the defect band contribution is ~2 orders of magnitude. The thermal emission from traps may be field dependent [38] so the TAT contribution to the leakage current may change with bias. Also at higher biases BBT becomes more significant, the relative contribution of TAT to the total current drops. For diode ABD1 the defects are shallower than the junction and as a result are not all located in the depletion region. Thus the defect contribution to leakage is less.

The forward bias ideality factors are >1 as expected, due to the presence of large silicon-interstitial defects. Here we observe n values of 1.57, 1.79 and 1.75 respectively. Walker et al. [35] reported n values in the 1.67–1.81 range for p^+/n diodes with EOR defects located deeper than the junction. Note that diodes ABD1–3 are more ideal than diodes AB1 and AB2 where no defects were visible in XTEM but where the boron concentration was relatively high.

4. Simulation

4.1. Calibration

The extracted doping profiles were then used to define donor and acceptor profiles in the device simulator MEDICI to enable a closer evaluation of the electrical measurements and to validate the accuracy of the physical models available. Established models [11,19] were used for doping concentration dependent SRH, Band Gap Narrowing (BGN), TAT, BBT, self-consistent impact ionization, and Auger recombination. Here we focus our calibration effort on the diodes without residual EOR defects.

In Fig. 7 are the simulated and experimental forward and reverse biased current density characteristics for diodes AB1–AB5. Similar results were generated for the p^+/n diodes. With only a minor calibration (~1 order of magnitude change) to BBT and carrier lifetime prefactors the fit between simulated and experimental current density is excellent for AB3, AB4, and AB5. These diodes had an ideality factor ~1. However the simulation of diodes AB1 and AB2 proved to be more problematic. The dashed lines in

Table 2
Defect density and depth, forward ideality factor, reverse current density at 1 and 5 V, and activation energy at 1 and 5 V, for the diodes with similar background doping concentrations, namely diodes AB4 (no defects) ABD1–ABD3 (with EOR defects).

Split	Depth/width of defect band (nm)	Defect density EOR/hairpins (μm^{-2})/(μm^{-1})	n	J at 1 V Expt./simul. (A/μm^2)	E_A at 1 V (eV)	J at 5 V Expt./simul. (A/μm^2)	E_A at 5 V (eV)
AB4	–/–	–/–	1.03	$6.5 \times 10^{-17}/3.9 \times 10^{-17}$	0.61	$3.6 \times 10^{-13}/1.0 \times 10^{-13}$	0.17
ABD1	236/50	$2.5 \times 10^2/0$	1.57	$1.5 \times 10^{-14}/5.1 \times 10^{-17}$	0.38	$6.2 \times 10^{-12}/7.7 \times 10^{-14}$	0.15
ABD2	373/80	$3 \times 10^2/3$	1.79	$1.3 \times 10^{-13}/7.4 \times 10^{-17}$	0.38	$7.6 \times 10^{-11}/3.8 \times 10^{-12}$	0.16
ABD3	452/90	NA/6	1.75	$1.5 \times 10^{-13}/8.2 \times 10^{-17}$	0.39	$2.1 \times 10^{-10}/8.2 \times 10^{-12}$	0.15

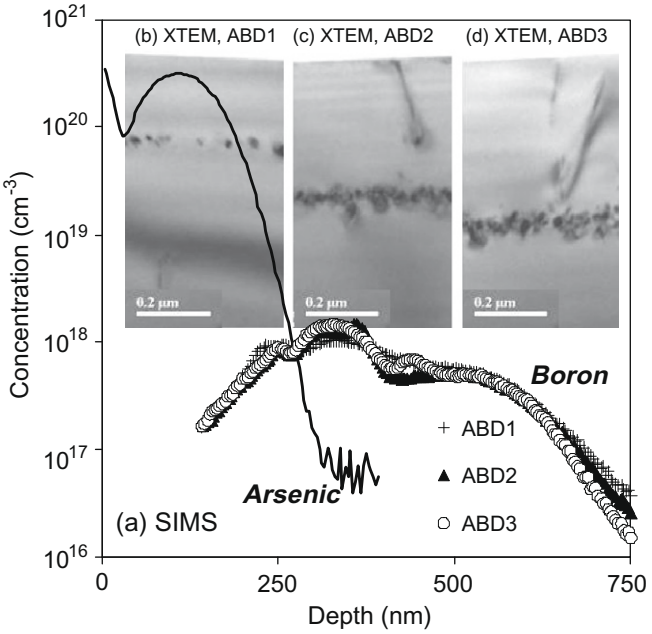

Fig. 6. (a) SIMS depth profiles of arsenic and boron for the diodes ABD1–ABD3, i.e. the diodes with intentional residual damage, (b) an XTEM image of diode ABD1, (c) an XTEM image of diode ABD2, and (d) an XTEM image of diode ABD3. Details of the defect density and location can be found in Table 2.

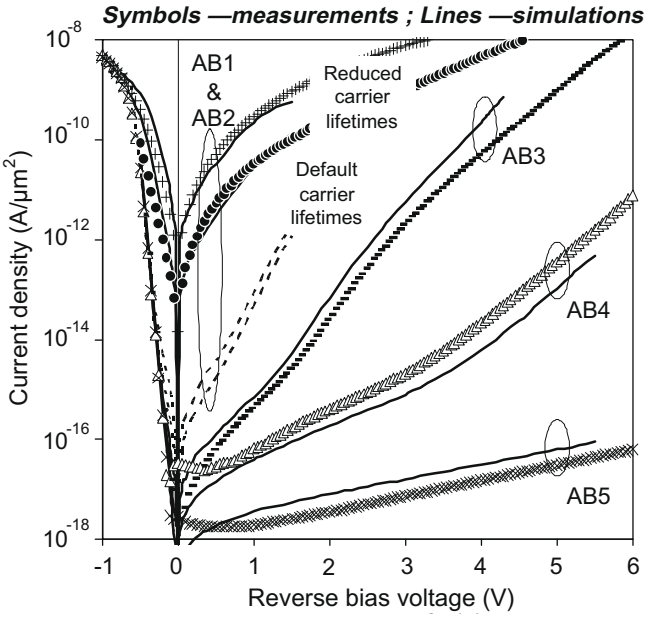

Fig. 7. Experimental and simulated forward and reverse current density versus bias, for the diodes AB1–AB5. For AB1 and AB2 the dashed lines show the simulations with default carrier lifetimes, the solid lines are those with reduced carrier lifetimes.

Fig. 7 show simulation results using default carrier lifetimes, and they underestimate the experimental results by 3–4 orders of magnitude at 1 V reverse bias. A similar simulation trend was observed for the p^+/n diodes. Measurements and simulations diverge at background concentrations above 2×10^{18} cm^{-3}, independent of background dopant species.

To gain further insight, carrier lifetimes were used as a fitting parameter and the solid lines in Fig. 7 for AB1 and AB2 are the result of this. In Fig. 8 is the comparison between experimental and

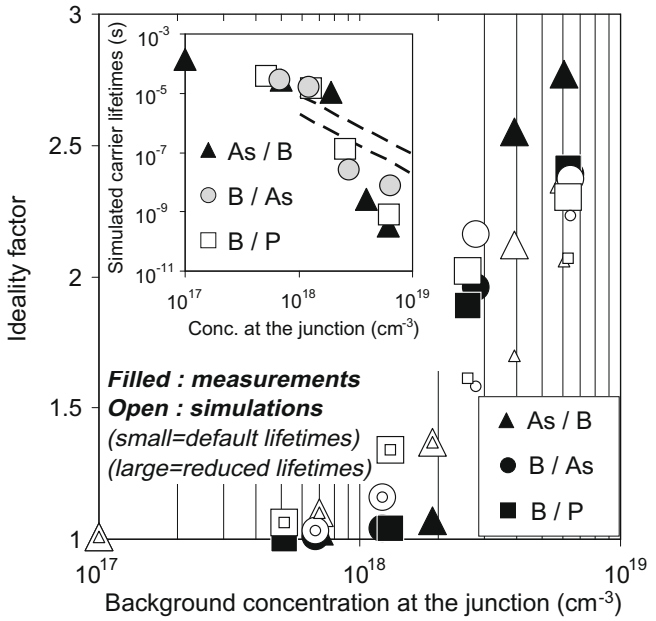

Fig. 8. Experimental and simulated forward bias ideality factor versus background concentration at the junction n^+/p and p^+/n diodes in this work. Inset: Carrier lifetimes versus background concentration, where the symbols represent the lifetimes required to fit the simulations to the measured electrical characteristics for the n^+/p and p^+/n diodes. The dashed lines represent experimental data from Dziewior and Schmid [39].

simulated ideality factor as a function of background concentration. With default carrier lifetimes n is predicted well up to 2×10^{18} cm^{-3}, above that point they are underestimated. With carrier lifetime reduction the fit is improved. Simulated values of the carrier lifetimes are shown in the inset of Fig. 8 as a function of background doping concentration. Experimental data from Dziewior and Schmid showed doping concentration dependent carrier lifetimes associated with Auger recombination [39], and fit lines to their data are included in the inset. For the diodes with background concentrations $>2 \times 10^{18}$ cm^{-3} the simulated lifetimes must be reduced significantly. Although the SRH and Auger recombination models include the effect of doping concentration on carrier lifetimes, we need to reduce them even further to get an acceptable simulation fit. While this calibration approach is sufficient for the current density characteristics at 25 °C, it is not satisfactory as the temperature dependence in AB1 and AB2 ($E_A \sim 0$ eV) is not well reproduced. This indicates that a severe local E_{FIELD} enhancement is present in those diodes that is not captured in the simulations.

Shown in Fig. 9, for ideally behaved diodes ($n \sim 1$) AB3, AB4 and AB5, the E_A dependence on reverse bias is quantified very well by the simulations. In conclusion, MEDICI can accurately quantify leakage in ideal junctions and predict the dominant physical mechanisms responsible.

4.2. High background concentrations

Based on the observations in Fig. 7 it is clear that enhanced leakage generation is present at high background doping concentrations. Furthermore it appears to be independent of dopant type and species. This discrepancy is not considered to be a miscalibration of the BBT model as fitting the current density characteristics would require a large, unphysical, change in the BBT model parameter set. Likewise it is not thought to be a miscalibration with the BGN model. BGN has a significant effect on tunneling generation because if the band gap is smaller it is easier for

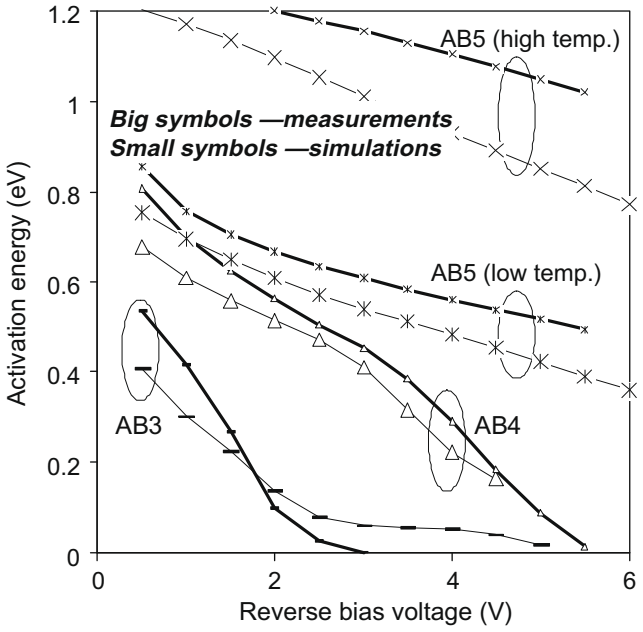

Fig. 9. Experimental and simulated activation energy of the current density characteristics versus reverse bias for the diodes AB3, AB4, and AB5. For AB5 low temperatures are 25–55 °C, and high temperatures are 65–105 °C.

carriers to tunnel through. There are many experimental and theoretical papers on this subject [40–45]. The highest BGN for our doping concentrations predicted by theory is ~60 meV. If a forced calibration is applied in our simulations, BGN of >400 meV is required for the high background concentration diodes, which clearly is not physical.

Carrier lifetimes are known to decrease with increasing impurity concentrations [10]. Generation/recombination centers that reduce carrier lifetimes can be induced by the presence of clusters or precipitates in the silicon. In their work on silicon emitters, Andersson and Engström reported that generation centers were formed due to a clustering process linked to high phosphorus concentrations [46]. Fourier Transform Infra-Red analysis of De Gryse et al. [47] show oxygen related precipitation at high boron concentrations. Bothe and Schmidt reported that carrier lifetime limiting centers form in boron-doped oxygen-contaminated crystalline silicon [48]. Their concentrations are linearly dependent on substitutional boron concentration and quadratically dependent on interstitial oxygen concentration [49]. Furthermore oxygen content in the starting wafer in the 10^{17} cm^{-3} range has been shown to increase leakage by Slotboom et al. [50], while Claeys et al. correlated diode leakage and carrier lifetimes with initial oxygen concentration [51].

While the exact source of enhanced leakage in our diodes is not certain at this point in time, it is clear that the starting wafer quality and the processing history of the diodes is important to reduce junction leakage. Our work shows that this is even more critical as the doping level at the junction increases $>2 \times 10^{18}$ cm^{-3}, independent of dopant species and type. Future experiments are required on this point, and should include an investigation on wafer oxygen content for doping concentrations similar to those here.

Finally, Hurkx and Agarwal [52] recently reported that quantum-mechanical effects not only influence the generation–recombination rates but also the carrier concentrations in the depletion layer. At doping concentrations much higher than 10^{18} cm^{-3} the carrier concentrations in the depletion layer (pn product) are several orders of magnitude greater than in the semiclassical case. This indicates that for such high doping levels the classical drift–diffusion theory, which is the basis of our comparison, starts losing its validity for predicting diode currents. For this reason our simulations may be inaccurate at very high doping levels.

4.3. EOR defect contribution

As there is no calibration attempted for the EOR defect leakage contribution, in the simulations we predict the leakage generated by the doping profile (i.e. E_{FIELD}). In the experiment we have the combination of the doping profile and EOR defect contributions. Thus by comparison we can quantify the EOR defect contribution. Returning to Table 2 the measured and simulated characteristics can be compared for n^+/p diodes with EOR defects. As stated previously the defect contribution is dependent on applied bias, and thus on E_{FIELD}.

4.4. Predictions for extended planar bulk CMOS

In this analysis we consider specifications from the International Technology Roadmap for Semiconductors [1] (ITRS) for "Extended Planar Bulk" silicon MOS devices with sub-40 nm gate lengths. The ITRS roadmap lists specs for supply voltage (V_{dd}), off-state current (I_{OFF}), physical gate length, extension steepness, and junction depth (X_J). The extension steepness and X_J values are functions of the physical gate length. The extension steepness = 0.11 × the physical gate length. In the following simulations, for high doping concentrations, we do not include quantum-mechanical effects, extra carrier lifetime reduction, or defect induced leakage current. Thus this should be considered a "best-case" analysis. In other words the devices are assumed to be processed without defects or non-idealities.

Shown in Fig. 10 is a plot of diode leakage current density at 1.1 V reverse bias from 1D simulations. There are two variables, namely the steepness of the extension profile, and the background concentration which represents the pocket profile. The peak activation of the extension is assumed to be 2×10^{20} cm^{-3}. As both extension steepness and background concentration increase, the current density increases. Included in the legend is a guideline for where BBT dominates the leakage current. Typically for junc-

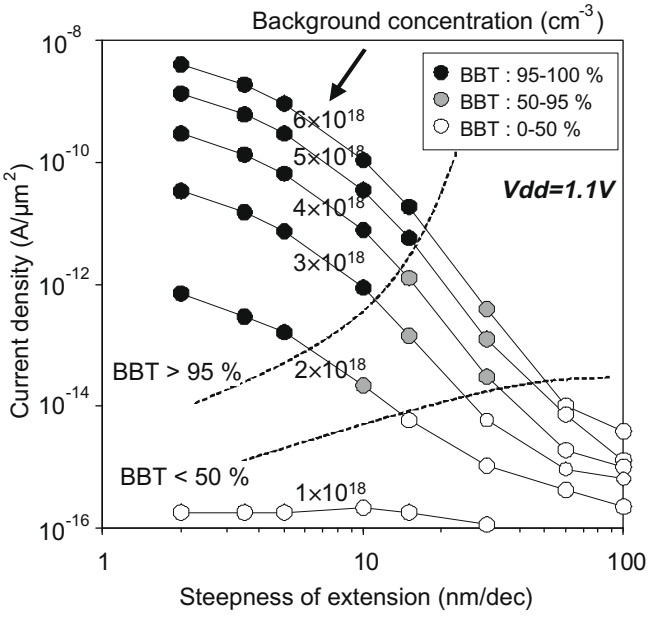

Fig. 10. 1D simulations of current density at 1.1 V reverse bias versus extension profile steepness and background concentration. The regime were BBT dominates is specified.

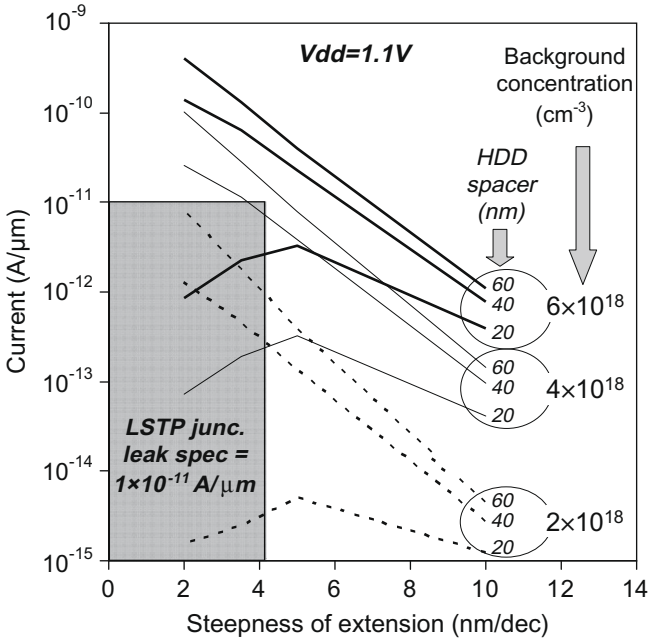

Fig. 11. 2D simulations (i.e. curvature effects included) of junction leakage current at 1.1 V reverse bias versus extension profile steepness, background concentration, and HDD spacer length. The shaded area indicates junction leakage and steepness targets for a 37 nm physical gate length LSTP device, according to the ITRS Roadmap.

tions that produce low local E_{FIELD} BBT is not significant, while for junctions that generate high E_{FIELD} BBT dominates. Modern bulk MOS devices have extension junctions steeper than 5 nm/dec and pocket concentrations in the 2–5 $\times$ 10^{18} cm^{-3} concentration range, thus junction leakage is BBT dominated.

In Fig. 11 is a plot of transistor leakage current at 1.1 V reverse drain bias from 2D simulations (i.e. MOS device in off-state). The 2D nature of a junction in an advanced CMOS technology can be seen in the work of Eyben et al. [53,54]. In our simulations the variables are extension steepness, HDD spacer thickness, and background concentration. While we have focused on the HDD spacer here, note that other process variables such as extension implant angle, multiple extension implants, and combinations of those, could also be used to affect the junction leakage in a CMOS device. The HDD profiles are assumed to have a steepness of 10 nm/dec. These 2D simulations inherently include the influence of junction curvature. For a Low Standby Power (LSTP) device with a 37 nm physical gate length, the junction steepness target is 4.1 nm/dec. With V_{dd} = 1.1 V, the junction leakage is targeted at 10 pA/μm in the 2007 edition of the ITRS Roadmap. These specs for extension steepness and leakage define a target region, as shown in Fig. 11. As before leakage increases with increased background concentration and extension steepness. However leakage is reduced with a smaller HDD spacer, as the HDD profile covers more of the aggressive extension profile. For the 20 nm spacer the leakage falls with extension steepness <5 nm/dec, as the extension is being pulled more and more inside the HDD profile. The drawback of the scaled spacer is a potential loss in short channel effect control.

The 4 $\times$ 10^{18} cm^{-3} background concentration with the 40 nm spacer can just penetrate the target box. With EOR defects remaining after junction formation, assuming a two orders of magnitude leakage increase, the LSTP leakage target becomes very difficult to meet. In the 2D system of a CMOS device, EOR defects will not encompass the junction completely. Due to annihilation close to the surface, few defects should remain close to the channel. This aspect may partially reduce the EOR defect contribution to junction leakage in the CMOS device application. The maximum allowed subthreshold leakage ($I_{sd,\ leak}$) spec in the ITRS Roadmap for an LSTP device with a 37 nm physical gate length is 3.03 $\times$ 10^{-11} A/μm. From Fig. 11 it is clear the junction leakage is in the order of the ITRS Roadmap subthreshold leakage for realistic doping profiles, invalidating the assumption that off-state current is dominated by subthreshold leakage.

5. Conclusions

We quantified the influence of doping levels and implant related damage on reverse biased leakage currents in n^+/p and p^+/n diodes. There was a vast increase of current density as function of background concentration at the junction. In the n^+/p diodes, the current density at 1 V increased by ~8 orders of magnitude for a <2 orders of magnitude increase in boron concentration. The EOR defect contribution to leakage is E_{FIELD} dependent. In the diodes where the defect band was located entirely in the depletion region the increase in leakage was three orders of magnitude at 1 V reverse bias, but was 1–2 orders of magnitude at 5 V reverse bias. Clearly reverse leakage is more sensitive to doping changes than to the existence of residual EOR defects.

Furthermore, for background doping concentrations >2 $\times$ 10^{18} cm^{-3} the ideality and leakage levels of the diodes degraded rapidly despite standard processing. This is a serious concern for modern and future bulk-silicon MOS devices as pocket doping concentrations have entered this regime. This degradation in performance was independent of dopant type as boron, arsenic, and phosphorus all produced this phenomenon. The temperature independence of the high leakage levels points to an E_{FIELD} dependent tunneling related mechanism.

With respect to device modeling, established models can accurately predict the dominant leakage mechanism and quantify experimental current densities in diodes with ideality factors <2, with only a slight alteration of model parameters. However in diodes with ideality factors ~2 and higher, the simulations underestimate the very high leakage levels, indicating that there is a source of leakage that current simulation code does not yet account for.

Finally, the ITRS Roadmap specs for LSTP leakage contain assumptions that need to be reconsidered. With the emergence of junction leakage from aggressively ultra-shallow junctions, the assumption that the subthreshold leakage component dominates off-state current is no longer valid.

References

[1] The international technology roadmap for semiconductors. <http://www.itrs.net>.
[2] Solomon PM, Jopling J, Frank DJ, D'Emic C, Dokumaci O, Ronsheim P, et al. Universal tunneling behavior in technologically relevant P/N junction diodes. J Appl Phys 2004;95:5800–12.
[3] Duffy R, Dao T, Tamminga Y, Van der Tak K, Roozeboom F, Augendre E, et al. Group III and V impurity solubilities in silicon, due to laser, flash, and solid-phase-epitaxial-regrowth anneals. Appl Phys Lett 2006;89:071915.
[4] Tsai MY, Streetman BG. Recrystallization of implanted amorphous silicon layers. I. Electrical properties of silicon implanted with BF_2^+ or Si^+ + B^+. J Appl Phys 1979;50:183–7.
[5] White CW, Wilson SR, Appleton BR, Young Jr FW. Supersaturated substitutional alloys formed by ion implantation and pulsed laser annealing of group-III and group-V dopants in silicon. J Appl Phys 1980;51:738–49.
[6] Duffy R, Aboy M, Venezia VC, Pelaz L, Severi S, Pawlak BJ, et al. Boron pocket and channel deactivation in NMOS transistors with SPER junctions. IEEE Trans Electron Dev 2006;53:71–7.
[7] Jain SH, Griffin PB, Plummer JD, McCoy S, Gelpey J, Selinger T, et al. Low resistance, low-leakage ultrashallow p^+ junction formation using millisecond anneals. IEEE Trans Electron Dev 2005;52:1610–5.
[8] Earles S, Law M, Brindos R, Jones K, Talwar S, Corcoran S. Nonmelt laser annealing of 5-keV and 1-keV boron-implanted silicon. IEEE Trans Electron Dev 2002;49:1118–23.
[9] Claeys C, Simoen E, Poyai A, Czerwinski A. Electrical quality of epitaxial wafers based on p–n junction diagnostics. J Electrochem Soc 1999;146:3429–34.

[10] Schroder D. Carrier lifetimes in silicon. IEEE Trans Electron Dev 1997;44:160–70.
[11] MEDICI Users Manual, Synopsys.
[12] Trumbore FA. Solid solubilities of impurity elements in germanium and silicon. Bell Syst Tech J 1960;39:205–33.
[13] Loukianova NV, Folkerts HV, Maas JPV, Verbugt DWE, Mierop AJ, Hoekstra W, et al. Leakage current modeling of test structures for characterization of dark current in CMOS image sensors. IEEE Trans Electron Dev 2003;50:77–83.
[14] Poyai A, Simoen E, Claeys C, Czerwinski A, Gaubas E. Improved extraction of the activation energy of the leakage current in silicon p–n junction diodes. Appl Phys Lett 2001;78:1997–9.
[15] Hurkx GAM. On the modelling of tunnelling currents in reverse-biased P–N junctions. Solid State Electron 1989;32:665–8.
[16] Hurkx GAM, Klaassen DBM, Knuvers MPG. A new recombination model for device simulation including tunneling. IEEE Trans Electron Dev 1992;39:331–8.
[17] Andersson GI, Engström O. Forward-bias tunneling at defect clusters in silicon emitter junctions. J Appl Phys 1991;69:4418–25.
[18] Del Alamo J, Swanson RM. Forward-bias tunneling: a limitation to bipolar device scaling. IEEE Electron Dev Lett 1986;7:629–31.
[19] Hurkx GAM, De Graaff HC, Kloosterman WJ, Knuvers MPG. A new analytical diode model including tunneling and avalanche breakdown. IEEE Trans Electron Dev 1992;39:2090–8.
[20] Tamai Y, Oka MM, Nakada A, Ohmi T. Influence of substrate dopant concentration on electrical properties and residual defects in pn junction formed by low-temperature post-implantation annealing. J Appl Phys 2000;87:3488–96.
[21] Duffy R, Heringa A, Loo J, Augendre E, Severi S, Curatola G. Low-leakage ultra-scaled junctions in MOS devices; from fundamentals to improved device performance. In: Proceedings of the 210th meeting of the electrochemical society, vol. 3-2; 2006. p. 19–33.
[22] Solmi S, Landi E, Negrini P. Effect of annealing conditions on the electrical characteristics of p+/n shallow junctions. IEEE Electron Dev Lett 1984;5:359–61.
[23] Tsaur BY, Anderson Jr CH. Dual ion implantation technique for formation of shallow p+/n junctions in silicon. J Appl Phys 1983;54:6336–9.
[24] Felch S, Borland J, Fang Z, Koo BW, Gossmann H, Jones K, et al. Optimized BF_3 P^2LAD implantation with Si-PAI for shallow, abrupt and high quality p^+/n junctions formed using low temperature SPE annealing. In: Proceedings of the 14th international conference on ion implantation technology; 2002. p. 52–5.
[25] Alquier D, Van Haaren B, Bergaud C, Plana R, Graffeuil J, Martinez A. Influence of depth position of end-of-range defects on current–voltage and noise characteristics of shallow (p+/n) junctions. Jpn J Appl Phys 1997;36:1999–2003.
[26] Graoui H, Al-Bayati A, Duane M, Tichy R. Optimization of p+/n formation using solid phase epitaxy for the 100 nm technology node and beyond. In: Proceedings of the 14th international conference on ion implantation technology; 2002. p. 694–7.
[27] Ozturk MC, Wortman JJ, Osburn CM, Ajmera A, Rozgonyi GA, Frey E, et al. Optimization of germanium preamorphization conditions for shallow-junction formation. IEEE Trans Electron Dev 1998;35:659–68.
[28] Ayres JR, Brotherton SD, Clegg JB, Gill A, Gowers JP. Defects in tin pre-amorphized p+n junctions in silicon. Semicond Sci Technol 1989;4:399–407.
[29] Delfino M, Sadana DK, Morgan AE. Shallow junction formation by preamorphization with tin implantation. Appl Phys Lett 1986;49:575–7.
[30] Kamgar A, Fichtner W, Sheng TT, Jacobson DC. Junction leakage studies in rapid thermal annealed diodes. Appl Phys Lett 1984;45:754–6.
[31] Ong KK, Pey KL, Lee PS, Wee ATS, Wang XC, Tung CH, et al. Role of low temperature rapid thermal annealing in post-laser-annealed p-channel metal-oxide-semiconductor field effect transistor. Appl Phys Lett 2006;89:122113.
[32] Myers E, Rozgonyi GA, Sadana DK, Maszara W, Wortman JJ, Narayan J. Ge+ preamorphization of Si: effects of dose and very low temperature thermal treatment on extended defect formation during subsequent SPE. Mater Res Symp Proc 1986;32:107–13.
[33] Sadana DK, Maszara W, Wortman JJ, Rozgonyi GA, Chu WK. Germanium implantation into silicon. J Electrochem Soc 1984;131:943–5.
[34] Chen PS, Hsieh TE, Chu CH. Removal of end-of-range defects in Ge^+ pre-amorphized Si by carbon ion implantation. J Appl Phys 1999;85:3114–9.
[35] Walker AJ, Woerlee PH, Pomp HG, Cowern NEB. Shallow boron junctions and preamorphization for deep submicron silicon technology. J Appl Phys 1993;73:4048–53.
[36] Landi E, Solmi S. Electrical characterization of p^+/n shallow junctions obtained by boron implantation into preamorphized silicon. Solid State Electron 1986;29:1181–7.
[37] Brotherton SD, Ayres JR, Clegg JB, Gowers JP. Electrically active defects in shallow pre-amorphised p^+n junctions in silicon. J Electron Mater 1989;18:173–84.
[38] Vincent G, Chantre A, Bois D. Electric field effect on the thermal emission of traps in semiconductor junctions. J Appl Phys 1979;50:5484–7.
[39] Dziewior J, Schmid W. Auger coefficients for highly doped and highly excited silicon. Appl Phys Lett 1977;31:346–8.
[40] Dumke WP. Comparison of band-gap shrinkage observed in luminescence from n^+ Si with that from transport and optical absorption measurements. Appl Phys Lett 1983;42:196–8.
[41] Wagner J, Del Alamo JA. Band-gap narrowing in heavily doped silicon: a comparison of optical and electrical data. J Appl Phys 1988;63:425–9.
[42] Slotboom JW. The pn-product in silicon. Solid State Electron 1977;20:279–83.
[43] Lanyon HPD, Tuft RA. Bandgap narrowing in moderately to heavily doped silicon. IEEE Trans Electron Dev 1979;26:1014–8.
[44] Klaassen DBM, Slotboom JW, De Graaff HC. Unified apparent bandgap narrowing in n- and p-type silicon. Solid State Electron 1992;35:125–9.
[45] Jain SC, Roulston DJ. A simple expression for band gap narrowing (BGN) in heavily doped Si, Ge, GaAs and Ge_xSi_{1-x} strained layers. Solid State Electron 1991;34:453–65.
[46] Andersson GI, Engström O. Defect clustering in silicon emitter junctions. J Appl Phys 1990;68:6434–41.
[47] De Gryse O, Clauws P, Vanhellemont J, Lebedev OI, Van Landuyt J, Simoen E, et al. Characterization of oxide precipitates in heavily doped B-doped silicon by infrared spectroscopy. J Electrochem Soc 2004;151:G598–605.
[48] Bothe K, Schmidt J. Fast-forming boron–oxygen-related recombination center in crystalline silicon. Appl Phys Lett 2005;87:262108.
[49] Bothe K, Schmidt J. Electronically activated boron–oxygen-related recombination centers in crystalline silicon. J Appl Phys 2006;99:013701.
[50] Slotboom JW, Theunissen MJJ, De Kock AJR. Impact of silicon substrates on leakage currents. IEEE Electron Dev Lett 1983;4:403–6.
[51] Claeys C, Simoen E, Poyai A, Czerwinski A, Katcki J. P–n junction diagnostics to determine surface and bulk generation/recombination properties of silicon substrates. J Electrochem Soc 1999;146:1151–7.
[52] Hurkx GAM, Agarwal P. Quantum-mechanical effects on the carrier distribution around a semiconductor p–n junction. Phys Rev B 2006;73:233309.
[53] Eyben P, Vemula S-C, Noda T, Vandervorst W. Two-dimensional carrier profiling with sub-nm resolution using SSRM: from basic concept to TCAD calibration and device tuning. In: Proceedings international workshop on junction technology; 2009. p. 74–8.
[54] Eyben P, Vandervorst W, Alvarez D, Xu M, Fouchier M. Probing semiconductor technology and devices with scanning spreading resistance microscopy. In: Kalinin S, Gruverman A, editors. Scanning probe microscopy. New York: Springer; 2007. p. 31–87.