Materials Science in Semiconductor Processing 30 (2015) 451–455

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

The impact of thermal treatment on gettering efficiency in silicon solar cell

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ARTICLE INFO

Keywords:
Extrinsic getterings
Al gettering
LBIC
WTC-120 lifetime tester

ABSTRACT

This paper describes a study to understand the impact of heat treatment on the crystal Silicon (c-Si) with developed surface by Aluminum /Porous silicon (Al/PS) and evaluating their influence on the solar cell performance. In fact, the heat treatment of silicon surfaces with PS/Al is an effective means of structural and electrical adjustment and performance improvement of c-Si solar cells. The new process could be accomplished by a two-step annealing in order to benefit from both the high and low temperature processes. The advantages of such a new getter in comparison with traditional getter were demonstrated in various devices. We can estimate that the resistivity using the standard Van Der Pauw, and LBIC measurements have been performed to determine the diffusion length. The resistivity of crystalline silicon decreased when the porous layer was removed at about a depth around 70 μm. As a result, we found amelioration in the *I–V* characteristics and an enhancement of minority carrier lifetime. It has been shown that this simple method leads to improve the charge carrier collection and the electrical properties of c-Si based solar cells.

1. Introduction

In monocrystalline silicon for modern technology application, active areas of microelectronic devices are located in a thin region below the wafer surface. Unlike such a case, the solar cell depended strongly on the bulk of the wafer as being the active device region. Unfortunately, the c-Si solar cells can be generally affected by the unwanted impurities at deep levels in the band gap; which may drastically decrease the minority carrier lifetime, and deteriorate the bulk of length diffusion. Therefore, it is desirable to use the extrinsic gettering techniques at the solar cell fabrication process because solar cells are volume devices. [1–4]. Nevertheless, Al/PS gettering appear to be an efficient and cost effective technique to improve silicon wafers. The Al compound can getters impurities from the silicon substrate by chemical segregation, it has a relatively low diffusivity in Si compared to most other metals. However, a greater solubility for metal impurities than silicon can be provided in the AL/PS layer. [5–11]. It is well admitted that gettering efficiency depends strongly on the type of crystalline silicon and on its history; this suggests that the appropriate gettering can be affected over a wide temperature range [12,13]. However, the gettering effect with heat treatment has been widely discussed in the previous studies due to its benefit for the photovoltaic conversion. Nevertheless, studies about temperature optimization have seldom been reported. In light of these circumstances, efforts have been focused on the development of defect engineering tools in a precise temperature range, such as extended gettering, for further metal impurity concentration reduction that could allow an enhanced gettering effect [14,15]. However, it is necessary to consider two steps annealing in order to take into account the effect of each step on the metal impurity concentrations within the Si material for these purposes. The crucial first step at high temperature included the solar

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http://dx.doi.org/10.1016/j.mssp.2014.10.042
1369-8001/

cell fabrication process, thereby; precipitate dissolution impurities can be expected. Then, the impurities cooled down at low-temperature where they received a new gettering. This technique of two-step annealing has been used to facilitate an excellent control profile without precipitation and surface segregation effects.

In this study, we demonstrated that it is possible to enhance silicon wafer purification by two-step annealing. Further, we reported electrical results in order to evaluate the effect of two-step annealing in the same silicon.

2. Experimental procedure

The used substrates are Czochralski (Cz) low-cost, oriented (100), and p-type boron doped silicon, with a resistivity ranging from 1 to 2 Ω cm and a thickness of about 200 μm. The wafers were dipped in an acid mixture solution (HF: 16%, HNO_3: 64%, CH_3COOH: 20%) for a few seconds, then they were rinsed in deionized water. A thin porous layer was formed on both sides of the sample by stain-etching of the wafers in an $HF/HNO_3/H_2O$ solution with 1:3:5 volume compositions. Then, a thick aluminum layer was evaporated onto both sides of samples.

In order to optimize the range temperature and improve the electrical quality, the Cz wafers were individually annealed in either one or two steps. This experimental is organized as follows:

First treatment: samples (C1) were thermally treated at 750 °C for 30 min in N_2 ambient.

Second treatment: samples (C2) were thermally treated at1050 °C for 30 min in N_2 ambient.

Third treatment: samples (C3) were thermally treated at 1050 °C for 25 min and cooled down to 750°C where the wafers received a gettering anneal in N_2 ambient for 30 min.

C0 is an untreated sample taken as a reference for comparison.

After the heat treatment and in order to remove the PS/Al layer, we immersed these samples successively in an HF and NaOH (1 N) solutions. Then, the wafers to be studied were separated into three sets. The first set was used for developing an $Al/SiO_2/Si–SiO_2/Si$ structure. The MIS ($Al/SiO_2/Si$) structure was deployed for the LBIC method that proved to be much more sensitive to fine detail than channeling measurements. At the second step, we carried out resistivity measurements using the standard Van der Pauw. The third set to be used with the c-Si solar cells was achieved by performing phosphorus diffusion in a rapid thermal infrared tubular furnace at 925 °C for 30 min. The back aluminum (Ag/Al) and the front contact (Ag) were made by screen printed and fired at 850 and 620 °C respectively. The minority carrier lifetime was measured by a Sinton WTC-120 set-up with the intention. The electrical characterization (*I–V*) was measured by a source meter keithley 2400. The data were analyzed by software origin.

3. Results and discussion

3.1. Minority carrier lifetime

Table 1 illustrates the variation of the effective minority carrier lifetime τ_{eff} for each treatment after being immersed in 0.1 M concentrated I–E solution [16,17]. The effective lifetime τ_{eff} is the net result of summing up all the recombination losses that occur within the different regions constitutive of a given silicon sample.

Table 1
Variation of minority carrier lifetime values from top surface of solar cells with the treatment conditions.

Samples	C0	C1	C2	C3
τ_{eff} (μs)	4.88 ± 0.9	21.68 ± 1.15	14.7 ± 1.07	24.87 ± 1.26

All lifetime measurements were taken through the photoconductance lifetime tester (WTC 120 Sinton) technique. The latter is based on the measurement of the relative change of Δn with time. A simple flash lamp is used to produce a slowly varying illumination and a resulting time dependence of the excess photoconductance of the sample. The analysis of data determined the effective minority carrier lifetime. All reported lifetimes were measured at an injection level of $1 \times 10^{15}\,cm^{-3}$. According to this formula (1)

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{\omega} \quad (1)$$

where τ_{bulk}: the bulk lifetimes; S_{eff}: the surface recombination velocities and ω is the thickness of the c-Si substrate.

The measured effective lifetime is equivalent to the actual lifetime bulk when the surfaces are well passivated. Nevertheless, the demands on surface passivation can be relaxed when determining the relatively bulk lifetimes. This suggests that the differences between surface recombination rates and samples are not substantial. In this case $(1/\tau_{eff}) \cong (1/\tau_{bulk})$.

The effective lifetime of bare c-Si wafer untreated was measured as 1.2 μs, which increased to 4.88 μs after passivation although some native dangling bonds near the surface are saturated.

The effective lifetime is significantly different for the samples and more significative depending on the process history of the sample.

As mentioned above, a significant change of the τ_{eff} after annealing at 750 °C was observed, which determined a decrease of impurities diffused into the gettering zone. The corresponding increase in lifetime is further enhanced with the 1050–750 °C combination. We observed lifetime degradation in the wafer treated at extremely high temperature annealed at 1050 °C

Nonetheless, we can make several tentative conclusions from the lifetime results which are briefly discussed below.

3.2. Diffusion length

To investigate whether an effect to the sample interior could be observed. A second, equally important aspect of the lifetime is that it is directly related to the diffusion length. The lifetime is primarily used in integrated circuit engineering whereas the diffusion length measurement is more commonly specified for photovoltaic.

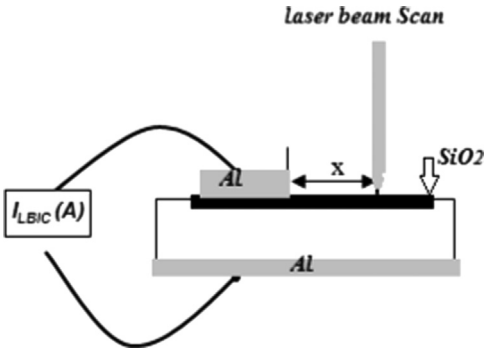

Fig. 1. MIS-structure realized for LBIC measurements.

Table 2
Variation of the diffusion length with the treatment conditions.

Samples	C0	C1	C2	C3
LD (μm)	74	156	116	186

The LBIC method makes possible to most types of defect detection under the surface of silicon wafer. A He–Ne laser focused beam, with 0.6328 μm wavelength, is used for excitation [18]. Indeed, there exist various defects which decrease the diffusion length. However, we have provided an empirical correlation between the densities for defect and measured the diffusion length.

In this method, wafers gettered require Al on entire back surface and a part on the front surface leaving the rest part as a bare for illumination. A photocurrent I is generated when an area of a part of the bare front surface in the vicinity of the $Al/SiO_2/Si$ interface is illuminated with a laser beam. (Fig. 1).

We used a theoretical model [19,20] that foresees a decay of the LBIC intensity with the distance x of the laser beam from the interface between the SiO_2/Si structure and the $Al/SiO_2/Si$ diode.

Table 2 illustrates the variation of diffusion length (L_D) for each treatment. Hence, for wafer C1, after annealing at temperature 750 °C, the L_D quantity has increased. Then, we noticed that the wafer treated at 1050 °C (C2) gave a low result associated with low diffusion length.

For wafer C3, here, we showed that with a combination of high and low temperatures, the diffusion length has performed well, it seems that the impurity atoms diffuse easily to the gettering zone after pre-anneal step at 1050 °C but at low temperature.

A comparison between various samples revealed an enhancement factor for the impurities density. Thus, we can mention that the heat treatment with the Al/PS layer ensures a very important improvement of the photocurrent generated in the bulk. Such an improvement in diffusion length and minority carrier lifetime are probably due to the reduction in defects bulk at applied temperature but it seems that there will exist a more effective treatment which will result in large minority carrier lifetime and large diffusion length.

From Tables 1 and 2, in the first case (wafers C1), this process has shown a significant increase in τ_{eff} and L_D values, but are still low and the recombination activity remains important. Since, the metal precipitates remain insoluble, and the result may be associated at the low release of metal impurities. In general, the low temperature enhances the diffusion gettering of dissolved metals but has only a minor effect on the precipitated metals. Thereby, the amount of getterable metals depends on the dissociation temperature. The issue was studied further by deep level in Ref. [21].

After a thermal treatment at 1050 °C, the resulting improvement of minority carrier lifetime and diffusion length remains low. It has been suggested that impurity precipitates dissociate at high temperatures, allowing the impurities to diffuse throughout the bulk. Once the impurities are released, one of the two processes, diffusion or capture, is a limiting step, as a result more impurities facilitate the defect reactions involving supersaturated metals [21]. Thus, obtained low values of τ_{eff} and L_D after annealing at 1050 °C could be the outcome of an initial increase in the number of dissolved impurity atoms which are not gettered at the surface or there may a substantial fraction of impurity atoms which may have promptly re-precipitated probably while quenching to the temperature. Previous work has suggested a relatively high diffusivity of most of the transition metals which facilitate the defect reactions involving supersaturated metals. [22]

After a thermal treatment at 1050 °C and a subsequent annealing at 750 °C, changes in τ_{eff} and L_D were observed in this process as illustrated in Tables 1 and 2, respectively, due to the decrease of the recombination centers. Particularly, this enhancement was due to the decrease in the number of dissolved impurity atoms as a result of a precipitate dissolution at 1050 °C, the impurities may remain interstitially dissolved at this temperature, and capture of impurities in the gettering layer at a subsequent treatment (750 °C) that can provide the mobility necessary to reach the sinks, when it may form complexes with Al and so causes reduction in impurity instead of precipitating. However, such an interaction between dissolved impurity atoms is unlikely [21]. However, it seems reasonable to suppose that the effective gettering would exhibit some dependence on the temperature, considering the segregation coefficient and diffusion coefficient. Thus, the choice of the gettering temperature is a compromise between diffusion coefficient (precipitate dissolution) on the one hand, and segregation coefficient on the other hand. [23,24].

3.3. Resistivity measurement

In the present study the nature and the concentration of contaminants in the bulk are unknown; the atoms impurities may pair with dopant atoms to form complexes which can cause a strong concentration of scattering centers in the bulk. This means that while the higher impurity concentration reduces the carrier mobility, it tends to increase the resistivity.

The resistivity is measured by means of the Van Der Pauw method investigations. The measured values of electrical resistivity seemed to be directly affected by the total concentration of scattering centers. We clearly assume a decrease in values of R with diminishing in concentration of

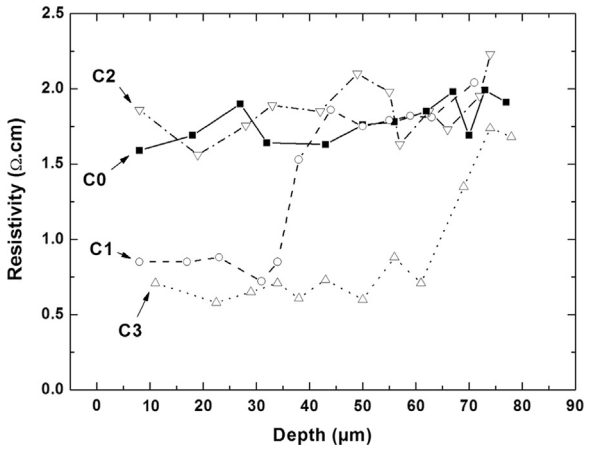

Fig. 2. Resistivity profile of ungettered wafer C0 and gettered Si wafers; C1 at 750 °C, C2 at 1050 °C and C3 at 1050 °C with a subsequent annealing at 750 °C.

scattering centers bulk which will result itself in a minimum of impurity contamination.

The resistivity profile was achieved through the successive eliminations of thick Si layers by etching in an acid solution (HNO_3: 64%, HF: 16%, CH_3COOH: 20%). This procedure shows to which extent the interior of the sample was influenced by the heat treatment. The two steps annealing process was chosen as the optimal gettering step for the Cz wafers.

Fig. 2 illustrates the variation of the resistivity of various samples after gettering process at different temperatures and at several depths.

The resistivity decreases after annealing at 750 °C for the wafer C1. This behavior is more sensitive with the combination of two step annealing (wafer C3).

In this case, the resistivity with respect to depth has been taken into account in our work.

After a thermal treatment at 750 °C (wafer C1), the resistivity of crystalline silicon decreased when the porous layer was removed and abruptly increased from depth 40 μm. This behavior is as expected from previous publications [22–24]. Thus it seems that during the process, the dissolution of precipitates proceeds in a layer by layer manner, starting at the Al/PS–Si interface depending of the applied temperature.

We obtain a significant reduction in *R* values that is only visible near the sample surface, a region in the range of less than 40 μm from the surface that seems to be affected. No true bulk recovery is observed; the effect is attributed to chemical segregation, PS/Al layer to the surface. In this applied temperature, we believe that the rate of impurities removal is severely restricted by the limited dissolution of precipitates although more impurities in the area of less than 40 μm take the form of precipitates.

After a thermal treatment at 1050 °C (wafer C2), there is no significant change in the resistivity, Fig. 2, comparing with the reference wafer. This result could be the outcome of an initial increase in the number of impurity dissolved that cannot reach the surfaces to form precipitates in the bulk and the reason might be related to the higher solubility of metals at this temperature.

We can conclude that in this temperature range from 1000 to 1100 °C, the rate of precipitate dissolution exceeds the rate of impurity out diffusion to the Al/PS layer [20,25,26].

After a thermal treatment at 1050 °C and a subsequent annealing at 750 °C (wafer C3); the resistivity of the gettered wafer C2 decreases; as the order of magnitude is higher than that of the wafer C1 at a depth of about 70 μm. This optimum could be the result of the competition between the release of impurities from the bulk (at first step) and a capture of impurities in the gettering layer (on second step).

Although the problem of precipitates in principle has been eliminated, the purity effectiveness depends on the establishment of gettering sites for absorbing impurities, the diffusion coefficients of the impurities in bulk Si, and the segregation coefficient of the impurities at the gettering sites [27–30].

4. The *I–V* characteristics: *I–V* under illumination

After presenting a general methodology used in this work, a new experimental data was added where the focus was specially on photovoltaic. The *I–V* measurement is the most important characterization tool for photovoltaic devices. Even though quite simple, it is the one that gives the most information on the device quality.

The current–voltage characterization under illumination (100 mW/cm^2) is demonstrated in Fig. 3. The experimental results on the photovoltaic parameters for four solar cells before and after high temperature annealing such as short circuit current (I_{SC}), open circuit voltage (V_{OC}), fill factor (*FF*) and efficiency (η) were extracted from the *I–V* curves and are shown in Table 3. Nonetheless, we can make several observations from the *I–V* results.

The measured V_{oc} values seem to be directly affected by the final impurity density level in the bulk leading to a strong correlation between V_{oc} and impurity density. We clearly notice a substantial increase in V_{oc} with diminishing bulk impurity density similarly as in the case of measurement of minority carrier lifetime and bulk length diffusion. Notice that with the most efficient gettering treatment used here, with two steps annealed.

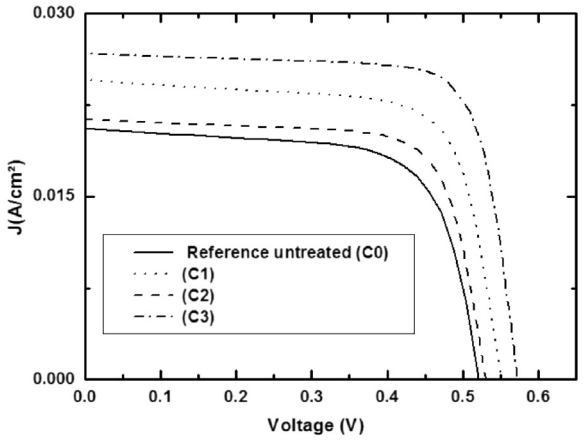

Fig. 3. Current density characteristics versus applied voltage under illumination with the treatment conditions.

Table 3
Photovoltaic parameters of processes c-silicon solar cells.

Solar cell parameters	Untreated c-Si C0	Sample C1	Sample C2	Sample C3
I_{sc} (A)	21.4×10^{-3}	25.7×10^{-3}	22.4×10^{-3}	28×10^{-3}
V_{oc} (V)	0.520	0.556	0.528	0.573
FF	0.69	0.74	0.72	0.77
η (%)	7.8	10.6	8.5	12.3

The obtained short-circuit current density values (J) are also interesting (Table 3). We obtain a correlation between the J_{sc} and the various parameters, but J_{sc} is also clearly dependent on the used treatment. This can be seen by comparing the cells treated at 750 °C and that treated at 1050 °C, where the J_{sc} value decreases with high temperature leading to negatively affect the wafer quality.

The fill factor (*FF*) values of the cells vary between 0.69 and 0.77, thus, we obtain an individual correlation between the (*FF*) and treatments are observed. We obtain a significant improvement in the (*FF*) value after each gettering process.

The behavior of the conversion efficiency of the cells with different treatments is a result of the combined effects of the V_{oc}, J_{sc} and *FF* described previously. As can be seen from Table 3, the efficiency values are indeed in correlation with the applied treatment. Similarly as in the case of L_D, the efficiency of the cells significantly improves as the bulk diffusion length increases. This is a key electrical property that needs to be improved in order to achieve high conversion efficiency [31].

5. Conclusion

In this work, we have shown that furnace annealing at 1050 °C, in combination with low-temperature annealing, a much better quality of silicon is obtained with minimum defects. These processes are intended to guard them against any more contamination during further thermal processing. Al/PS improves the crystalline quality which confirmed by clear improvement in the minority carrier lifetime. The increase of the diffusion length is attributed to the clear reduction of the deep-level impurities density [18]. In the resistivity measurements of these samples show that a big deep-level seems to be affected. We conclude that this treatment could be very beneficial to the final cell performance.

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