Solid State Electronics 159 (2019) 171–176

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Experimental analysis and improvement of the DC method for self-heating estimation

C.A.B. Mori[a,*], P.G.D. Agopian[a,b], J.A. Martino[a]

[a] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[b] Sao Paulo State University (UNESP), Sao Joao da Boa Vista, Brazil

ARTICLE INFO

Keywords:
Self-heating effect
Silicon-on-insulator
UTBB

ABSTRACT

This paper reports an improved method for estimating the thermal resistance of a MOSFET device using the inverse of the transistor efficiency as a function of the power applied to the transistor's channel. This method was deduced considering that the main effect of the self-heating is on the carriers' mobility, where the temperature dependency, vertical/lateral field degradation and saturation velocity were taken into account. After performing the analytical considerations, the method was validated through numerical simulations to verify if its results were compatible with other traditional pulsed-like method for the thermal resistance extraction. This improved method was applied experimentally to attest its robustness. The advantages of this method are the use of DC measurements only and differences smaller than 10 K in the estimation of the absolute channel temperature due to the self-heating effect compared to a traditional pulsed-like method for the UTBB SOI studied in this work.

1. Introduction

Although the continuing scaling of transistors has brought many improvements to their electrical characteristics, since the VLSI MOSFETs, the self-heating effect (SHE) has become significant, affecting their performance even at room temperature [1,2]. This occurs because the area available for heat dissipation is reduced, while the use of Silicon-On-Insulator (SOI) technology adds a thermal barrier below the channel, resulting in an overall higher thermal resistance (R_{th}), which means that it is harder to eliminate the heat generated in the channel due to the electric current, leading to ever-increasing temperatures. Currently, both Ultra-thin Body and Buried oxide (UTBB) and FinFET technologies suffer significantly with the effect, affecting not only their electrical performance [3,4], but also their reliability [5].

Traditionally, the main parameter related to the SHE is the thermal resistance, which can be obtained through several methods, ranging from infrared imaging techniques to small-signal RF [6]. This parameter has such a great importance in this context because it allows the direct conversion from electric power to temperature rise due to the SHE. Nevertheless, given the difficulty to implement those methods, which require dedicated structures or measurement equipment (e.g. the gate resistance requires a four-terminal gate, while the pulsed I-V needs ultra-short pulses for scaled nodes, and the small signal RF relies on specialized RF test setups), it becomes hard to assess the intensity of the SHE in a specific device.

Until very recently, there were no entirely DC electrical techniques that allowed the extraction of R_{th}; however, in [7] we first introduced a method capable of performing such a task. Thus, in this work we demonstrate and further improve this method, taking into consideration the mobility lateral field degradation and velocity saturation on the extraction of R_{th} and the subsequent estimation of the operation temperature of a given device. Then, we apply for the first time this method to experimental devices to verify whether the results obtained in such a condition present coherent results with what is expected from current technologies.

2. Proposed method

The first assumption for this method is that the drain current (I_D) in saturation can be described by

$$I_D = \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} \cdot \frac{(V_{GS} - V_t)^2}{2n} \cdot (1 + \lambda \cdot V_{DS}) \quad (1)$$

where μ_{eff} is the effective mobility, C_{ox} the gate oxide capacitance, W the channel width, L the channel length, V_{GS} the gate voltage, V_t the threshold voltage, λ the channel length modulation parameter, V_{DS} the drain voltage, and n the body factor. For the effective mobility, the expressions from the Level 3 model were considered, that is, its dependence with vertical and lateral electric fields, as well as the

* Corresponding author.
E-mail address: carlos.mori@usp.br (C.A.B. Mori).

https://doi.org/10.1016/j.sse.2019.03.056

Available online 19 March 2019

temperature dependence, resulting in

$$\mu_{eff} = \frac{\mu_0 \cdot v_{sat} \cdot L}{v_{sat} \cdot L \cdot (1 + \theta \cdot V_{GT}) + \mu_0 \cdot V_{Dsat}} \cdot \left(\frac{T_0}{T}\right)^c \tag{2}$$

where μ_0 is the low field mobility at reference temperature T_0, T is the temperature of operation, c is the coefficient of the mobility degradation with temperature, θ is the mobility reduction factor due to the vertical electric field, v_{sat} is the carriers saturation velocity, V_{Dsat} is the saturation drain voltage, and $V_{GT} = V_{GS} - V_t$ is the overdrive voltage. For this model, considering the operation in the saturation region, it is assumed simply that $V_{Dsat} = V_{GT}$. Defining the transconductance (g_m) as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3}$$

it is possible to write the transistor efficiency (g_m/I_D) as

$$\frac{g_m}{I_D} = \frac{1}{I_D} \cdot \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial \log(I_D)}{\partial V_{GS}} \tag{4}$$

Then, considering operation in the saturation region allows the application of (1) in (4), resulting in

$$\frac{g_m}{I_D} = \frac{\partial \log(\mu_{eff})}{\partial V_{GS}} + \frac{\partial \log(V_{GT}^2)}{\partial V_{GS}} + \frac{\partial \log\left[\frac{C_{ox}}{2n} \cdot \frac{W}{L} \cdot (1 + \lambda \cdot V_{DS})\right]}{\partial V_{GS}} \tag{5}$$

Using (2) for the term related to the mobility in (5) allows its expansion as

$$\begin{aligned} \frac{\partial \log(\mu_{eff})}{\partial V_{GS}} &= \frac{\partial}{\partial V_{GS}} \log\left[\frac{\mu_0 \cdot v_{sat} \cdot L \cdot T_0^c}{v_{sat} \cdot L \cdot (1 + \theta \cdot V_{GT}) + \mu_0 \cdot V_{GT}} \cdot \frac{1}{T^c}\right] \\ &= -\frac{v_{sat} \cdot L \cdot \theta + \mu_0}{v_{sat} \cdot L_{eff} \cdot (1 + \theta \cdot V_{GT}) + \mu_0 \cdot V_{GT}} - c \cdot \frac{\partial \log(T)}{\partial V_{GS}} \end{aligned} \tag{6}$$

Considering that C_{ox}, W, L, V_t, λ and n present a weak or no dependence on V_{GS}, (5) becomes

$$\frac{g_m}{I_D} = -\frac{v_{sat} \cdot L \cdot \theta + \mu_0}{v_{sat} \cdot L \cdot (1 + \theta \cdot V_{GT}) + \mu_0 \cdot V_{GT}} - c \cdot \frac{\partial \log(T)}{\partial V_{GS}} + \frac{2}{V_{GT}} \tag{7}$$

In a device suffering from SHE, the mean temperature of the channel can be written as

$$T = R_{th} \cdot P + T_{ext} \tag{8}$$

where $P = V_{DS} \cdot I_D$ is the power applied to the device's channel and T_{ext} is the external temperature. Thus, expanding the partial derivative in (7) as

$$\begin{aligned} \frac{\partial \log(T)}{\partial V_{GS}} &= \frac{1}{R_{th} \cdot P + T_{ext}} \cdot R_{th} \frac{\partial P}{\partial V_{GS}} = \frac{R_{th} \cdot V_{DS} \cdot g_m}{R_{th} \cdot P + T_{ext}} = \frac{R_{th} \cdot V_{DS} \cdot I_D}{R_{th} \cdot P + T_{ext}} \cdot \frac{g_m}{I_D} \\ &= \frac{R_{th} \cdot P}{R_{th} \cdot P + T_{ext}} \cdot \frac{g_m}{I_D} \end{aligned} \tag{9}$$

and defining M as an auxiliary function on V_{GT}

$$M = \left[-\frac{v_{sat} \cdot L \cdot \theta + \mu_0}{v_{sat} \cdot L \cdot (1 + \theta \cdot V_{GT}) + \mu_0 \cdot V_{GT}} + \frac{2}{V_{GT}}\right]^{-1} \tag{10}$$

allows the reformulation of (7) as

$$\begin{aligned} &\frac{g_m}{I_D} = \frac{1}{M} - c \cdot \frac{R_{th} \cdot P}{R_{th} \cdot P + T_{ext}} \cdot \frac{g_m}{I_D} \Leftrightarrow \frac{g_m}{I_D} \cdot \left(1 + c \cdot \frac{R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right) = \frac{1}{M} \Leftrightarrow \frac{I_D}{g_m} \\ &= M \cdot \left(1 + \frac{c \cdot R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right) \end{aligned} \tag{11}$$

In (11), we chose to present an expression for the inverse of the transistor efficiency, since it allows a simpler approach on the estimation of M. Considering V_{GT} as a constant, M becomes a constant as well; as a result, it is possible to write an approximation of (11) in P using a first degree Taylor polynomial centered at $P = P_0$, that is:

$$\begin{aligned} \frac{I_D}{g_m}(P) &\cong \frac{I_D}{g_m}(P_0) + \frac{d\left(\frac{I_D}{g_m}\right)}{dP}(P_0) \cdot (P - P_0) \\ &= M \cdot \left[\left(1 + \frac{c \cdot R_{th} \cdot P_0}{R_{th} \cdot P_0 + T_{ext}}\right) + \frac{c \cdot T_{ext} \cdot R_{th}}{(R_{th} \cdot P_0 + T_{ext})^2} \cdot (P - P_0)\right] \\ &= M \cdot \left[1 + \frac{c \cdot R_{th} \cdot P_0}{R_{th} \cdot P_0 + T_{ext}} \cdot \frac{R_{th} \cdot P_0 + T_{ext} - T_{ext}}{R_{th} \cdot P_0 + T_{ext}} + \frac{c \cdot T_{ext} \cdot R_{th} \cdot P}{(R_{th} \cdot P_0 + T_{ext})^2}\right] \\ &= M \cdot \left[1 + c \cdot \left(\frac{R_{th} \cdot P_0}{R_{th} \cdot P_0 + T_{ext}}\right)^2 + \frac{c \cdot T_{ext} \cdot R_{th}}{(R_{th} \cdot P_0 + T_{ext})^2} \cdot P\right] \end{aligned} \tag{12}$$

Considering that $c.[R_{th}P_0/(R_{th}P_0 + T_{ext})]^2 \ll 1$ results in

$$\frac{I_D}{g_m}(P) \cong M \cdot \left[1 + \frac{c \cdot T_{ext} \cdot R_{th}}{(R_{th} \cdot P_0 + T_{ext})^2} \cdot P\right] \tag{13}$$

The main use of (13) is to obtain an estimation of M through a linear approximation of the I_D/g_m in saturation. Then, if the c-factor is known, R_{th} can be extracted by adjusting the experimental points to the original model in (11). To ensure the validity of these approximations within the range of temperature rise expected due to the SHE (around 100 K for modern technologies [6–8]), (11) and (13) are used to calculate the relative error (ε_{rel}):

$$\begin{aligned} \varepsilon_{rel} &= \frac{M \cdot \left[1 + \frac{c \cdot T_{ext} \cdot R_{th}}{(R_{th} \cdot P_0 + T_{ext})^2} \cdot P\right] - M \cdot \left(1 + \frac{c \cdot R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right)}{M \cdot \left(1 + \frac{c \cdot R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right)} \\ &= \left[\frac{c \cdot T_{ext} \cdot R_{th} \cdot P}{(R_{th} \cdot P_0 + T_{ext})^2} - \frac{c \cdot R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right] \Big/ \left(1 + \frac{c \cdot R_{th} \cdot P}{R_{th} \cdot P + T_{ext}}\right) \\ &= \frac{c \cdot T_0 \cdot R_{th}^2 \cdot P^2 + c \cdot T_0^2 \cdot R_{th} \cdot P - (R_{th} \cdot P_0 + T_{ext})^2 \cdot c \cdot R_{th} \cdot P}{(R_{th} \cdot P_0 + T_{ext})^2 \cdot [(1 + c) \cdot R_{th} \cdot P + T_{ext}]} \\ &= c \cdot \frac{[T_{ext} \cdot R_{th} \cdot P - (R_{th} \cdot P_0 + 2 \cdot T_{ext}) \cdot R_{th} \cdot P_0] \cdot R_{th} \cdot P}{(R_{th} \cdot P_0 + T_{ext})^2 \cdot [(1 + c) \cdot R_{th} \cdot P + T_{ext}]} \end{aligned} \tag{14}$$

Instead of presenting ε_{rel} values for multiple P and R_{th}, an analysis of this error as a function of the temperature rise due to the SHE (given by $R_{th}.P$) is more relevant, which allows its study as a function of the intensity of the SHE rather than an electrical analysis. Through this approach, only two factors influence ε_{rel}: the P_0 adopted point, which can be seen as a temperature rise when multiplied by R_{th}, and the temperature mobility degradation factor (c). To evaluate the influence of those parameters, Figs. 1 and 2 show $|\varepsilon_{rel}|$ using (14) and considering the room temperature $T_{ext} = 300$ K.

From Fig. 1, it becomes clear that the proper choice of the P_0 point is necessary to achieve smaller values of $|\varepsilon_{rel}|$ within the range of temperature rise expected for the device. One consequence of using the approximation from (12) to (13) is that the point where $|\varepsilon_{rel}| = 0$ does not happen when $R_{th}.P = R_{th}.P_0$ as expected from the Taylor polynomial. Instead, as can be seen from (14), it moves to 0 and ($R_{th}.P_0$/

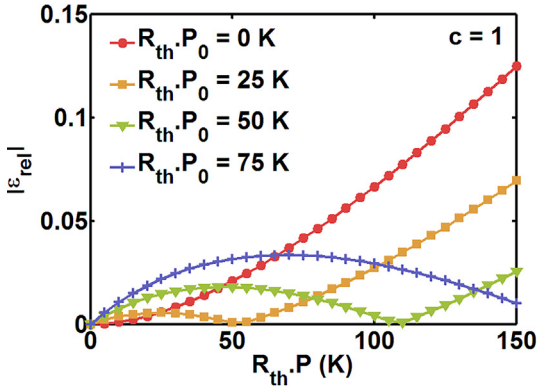

Fig. 1. Absolute value of the relative error as a function of the temperature rise due to the SHE for different P_0 points.

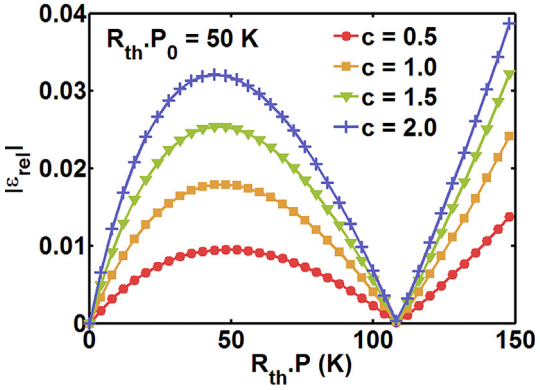

Fig. 2. Absolute value of the relative error as a function of the temperature rise due to the SHE for different c-factors.

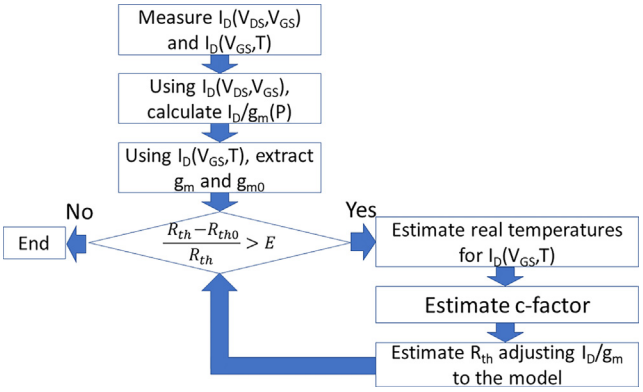

Fig. 3. Flowchart for the estimation of the thermal resistance using the proposed method.

T_0 + 2).$R_{th}.P_0$, which, for low values of $R_{th}.P_0$ can simply be approximated to 2.$R_{th}.P_0$, as observed in Fig. 1. For instance, a device that would heat 50 K above the room temperature could be well approximated with $R_{th}.P_0$ = 25 K, resulting in relative errors smaller than 0.01 (1%). On the other hand, this approximation would be less appropriate for a device that could reach up to 100 K above room temperature, resulting in a maximum relative error of approximately 4%.

Fig. 2 shows that the c-factor has a direct relation with $|\varepsilon_{rel}|$, as expected from (14). However, given the range of temperatures expected to be reached due to the SHE, combined with the relatively low values of the c-factor (ranging from 0.8 to 1.7 [9,10]), the relative error obtained is considered acceptable within the precision of the method being developed. Therefore, the first order Taylor polynomial approximation and considering that $c.[R_{th}P_0/(R_{th}P_0 + T_{ext})]^2 \ll 1$ do not interfere considerably using the I_D/g_m model for extracting M.

Thus, to estimate R_{th}, M can be calculated directly as the independent term of the linear regression from I_D/g_m (P), as observed in (13), while the c-factor can be extracted in the saturation regime using (2) and assuming that $g_m \propto \mu_{eff}$, that is:

$$\frac{g_m}{g_{m0}} = \frac{\mu_{eff}}{\mu_{eff0}} = \left(\frac{T_0}{T}\right)^c \Leftrightarrow c = \frac{\log\left(\frac{g_m}{g_{m0}}\right)}{\log\left(\frac{T_0}{T}\right)} \quad (15)$$

where g_{m0} and g_m are the transconductances at temperatures T_0 and T, respectively, measured for the same V_{GT}, at high V_{DS}, and μ_{eff0} is the effective mobility at T_0. However, T_0 and T are also affected by the SHE when such polarizations are employed, which makes an unreliable estimate of the c-factor when only the application of an external temperature is considered. To solve this problem, we suggest an iterative approach to estimate properly both c and R_{th} simultaneously.

To summarize the application of this method, the following steps are proposed: (I) Measurement of the I_D versus V_{DS} for some values of V_{GT} with a small step for both voltages (~10 mV) and the I_D versus V_{GS} at high V_{DS} to ensure that the device operates in the saturation region and at multiple temperatures. (II) Calculation of the I_D/g_m in saturation using the I_D versus V_{DS} curve for a fixed V_{GT} and varying V_{DS}, then execution of a linear regression to obtain M. (III) Extraction of g_m and g_{m0} from the I_D versus V_{GS} curves at constant V_{GT}. With all the required extractions performed, it is possible to start the iterative process, repeating steps IV through VI until the variation on the estimated R_{th} from the current step to the previous one (here referred to as R_{th0}) is as small as desired. (IV) Correction of the temperatures T and T_0 for the I_D versus V_{GS} curves using (8), P at V_{GT} and V_{DS} used for extracting g_m and g_{m0}, and R_{th0} (from the previous iteration, for the first execution of the loop it may be considered R_{th0} = 0 K/W). (V) From T and T_0 estimated in IV, calculate the c-factor using (15). (VI) Estimation of a new R_{th} that best fits the analytical model in (13) to the experimental data of I_D/g_m. This whole process is synthetized through a flowchart presented in Fig. 3.

3. Devices characteristics

In order to validate the proposed improved method with a traditional one, an UTBB structure was employed, with equivalent oxide thickness of 1.2 nm, source and drain doping of 10^{20} cm^{-3}, lightly doped drain extension of 10 nm length and concentration of 10^{17} cm^{-3}, buried oxide thickness (t_{BOX}) of 30 nm, silicon film thickness of 10 nm, channel width of 140 nm and lengths of 150 nm, 300 nm, and 500 nm. The devices were simulated using Sentaurus Device from Synopsys and are presented in Fig. 4. Experimental measurements were performed on UTBB transistors fabricated at imec, with t_{BOX} = 10 nm, t_{Si} = 10 nm, gate oxide of SiO_2 and 5 nm thick, W = 1 μm and L from 130 nm to 1 μm.

4. Simulation results

First, simulations to obtain the R_{th} of the devices according to a traditional pulsed method were conducted. Since it is possible to simply perform simulations considering or not the effect, an approach similar to the pulsed method described in [11] is developed, henceforth referred to as the traditional method. Using the intersections of the I_D versus V_{DS} of the SHE-free device at multiple temperatures with the I_D curve of the device with SHE at room temperature, it is possible to estimate the channel temperature increase due to the SHE at a given power level. The intersection between I_D with SHE and I_D without SHE at a higher temperature gives the power required by the self-heated device to reach such a temperature. Fig. 5 shows the I_D versus V_{DS} for each of the three different L simulated with and without SHE, allowing the extraction of the power and temperature points required to obtain Fig. 6, from which the thermal resistance for each L is obtained as being the slope of the lines.

Once the reference values were determined through the traditional method, the extraction through the method proposed was performed. Following the process described in Fig. 3, both I_D versus V_{DS} at multiple V_{GS} and I_D versus V_{GS} at multiple temperatures were simulated. From the latter, V_t is extracted through the square root of I_D for each of the temperatures simulated, resulting on the data presented in Fig. 7.

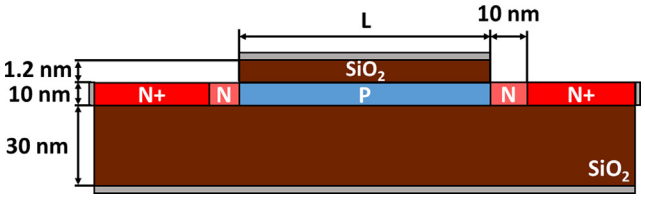

Fig. 4. Schematic view of the UTBB SOI MOSFET.

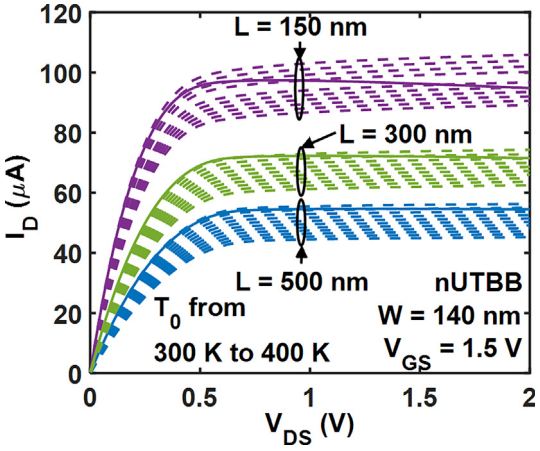

Fig. 5. Estimation of the channel temperature through simulated currents with SHE at room temperature (solid lines) and without SHE at multiple temperatures (dashed lines) for different channel lengths.

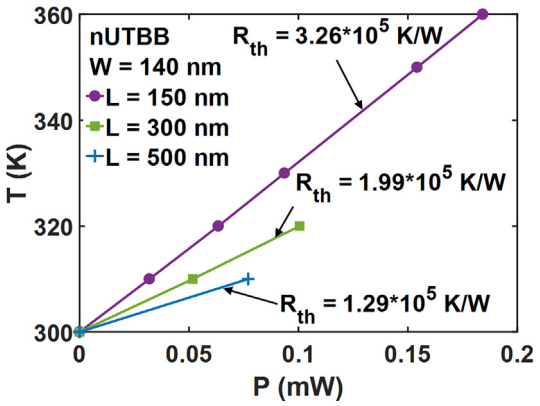

Fig. 6. Estimated channel temperature versus applied power.

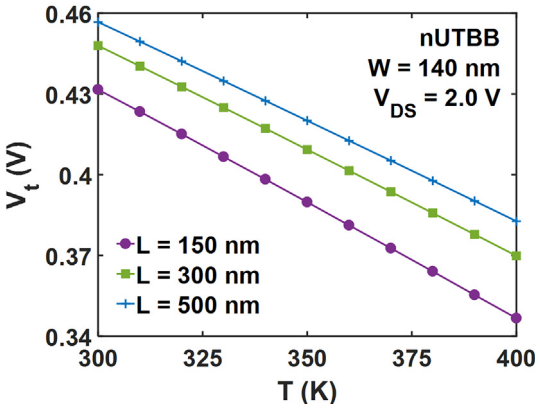

Fig. 7. Simulated threshold voltage versus external temperature.

Then, the I_D/g_m (P) is calculated using the I_D (V_{DS}) data with SHE, first obtaining g_m for each V_{DS}, using V_{GS} in the range between 0.5 V and 2.0 V, then fixing the value of V_{GT} = 0.9 V to obtain the dashed lines in Fig. 8. The criterion $V_{DS} > V_{GT}$ is used to define the points of I_D/g_m where the device is saturated, which are used to perform linear regressions for each device, represented by the solid lines in Fig. 8. From those regressions, the M-factor is obtained.

From the simulated I_D (V_{GS}), the g_m versus V_{GS} for temperatures between 300 K and 400 K is obtained as presented in Fig. 9. Establishing V_{GT} = 0.9 V as the reference for g_m and g_{m0}, it becomes possible to obtain the first estimate of the c-factor.

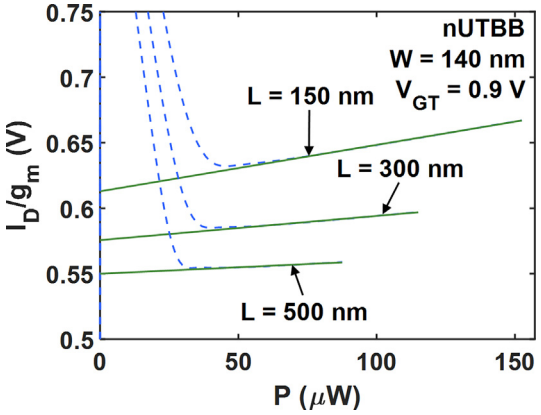

Fig. 8. Simulated inverse of the transistor efficiency versus applied power (dashed lines) and linear regression on the saturation region (solid lines).

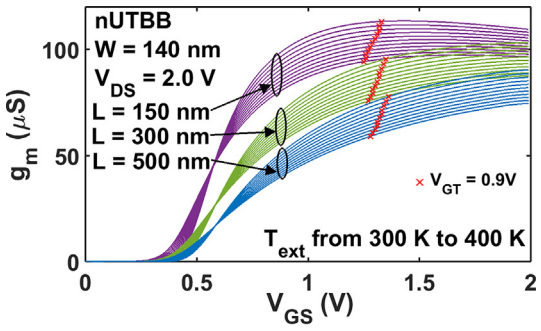

Fig. 9. Simulated transconductance versus gate voltage at multiple temperatures for each channel length, with the marks indicating the points where V_{GT} = 0.9 V.

With all the necessary parameters extracted, the iterative part of the process may be conducted until convergence is obtained. So far, a V_{GT} of 0.9 V was adopted to obtain the results presented, however, theoretically, the method should be independent of the overdrive voltage employed. To verify that, the extraction of R_{th} was performed for multiple V_{GT} values, resulting on the curves in Fig. 10.

Although the model proposed did not predict the oscillations and peak observed for low V_{GT}, they might be attributed to the fact that the SHE is not significant at lower power levels, compromising the extraction. Thus, the use of higher values of V_{GT} ensures that the approximations made are valid, which is confirmed by the stability observed of the extracted R_{th} at those values. Setting again V_{GT} = 0.9 V, the R_{th} for each one of the three devices is obtained, and then compared

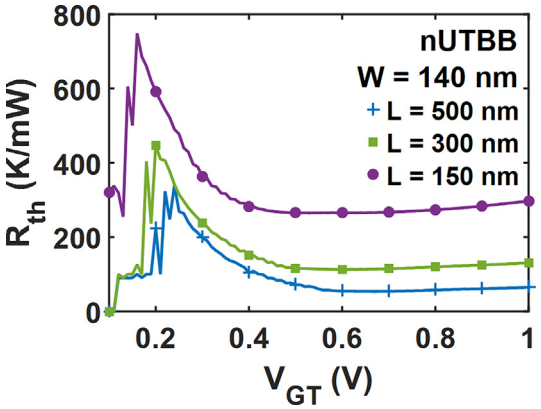

Fig. 10. Simulated thermal resistance for different overdrive voltages and for multiple channel lengths.

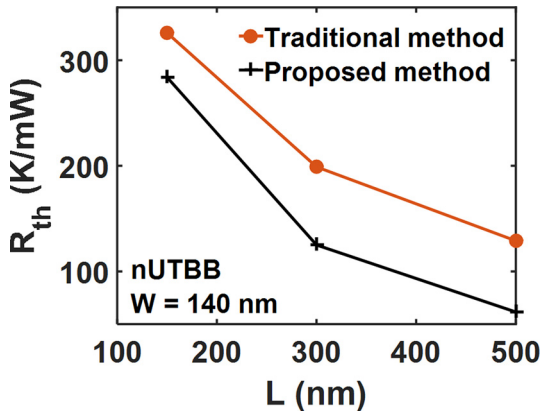

Fig. 11. Thermal resistances obtained through the traditional and proposed methods versus channel length.

to the values previously extracted through the traditional method in Fig. 11.

When the R_{th} is extracted, the c-factor has to be evaluated to verify if it remains within a reasonable value for the Taylor polynomial approximation. To perform this verification, the c-factor as a function of the external temperature is presented in Fig. 12.

As shown on Fig. 12, the c-factor remains relatively close to 1, thus, the error due to the approximation employed can be considered negligible.

Finally, one important metric to be considered when studying the SHE is the device effective temperature, since it will affect directly its output current. Comparing the estimated temperatures in Fig. 13 obtained for each L through (8) (considering external temperature of 300 K and a worst-case scenario with both high V_{GS} and V_{DS}), with the extracted values of R_{th} through both methods, it becomes clear that the proposed method provides a good approximation even at the worst case, resulting in a difference between absolute temperatures lower than 10 K.

Considering that this value represents less than 3% of the device's absolute temperature, such a difference would result in an almost negligible difference on the mobility degradation. Given that it requires only DC measurements while the pulsed method requires ultra-short pulses for scaled nodes (< 5 ns), the new method shows promise to be a more applicable option.

5. Experimental results

To verify the applicability of this method to experimental devices, measurements were performed on UTBB devices following the method

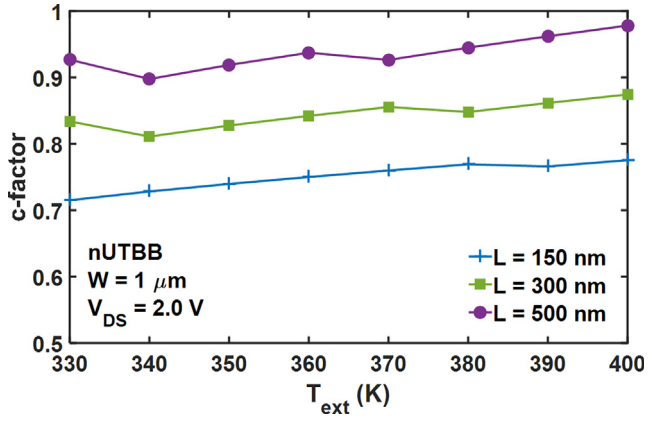

Fig. 12. Values obtained for the c-factor as a function of the external temperature.

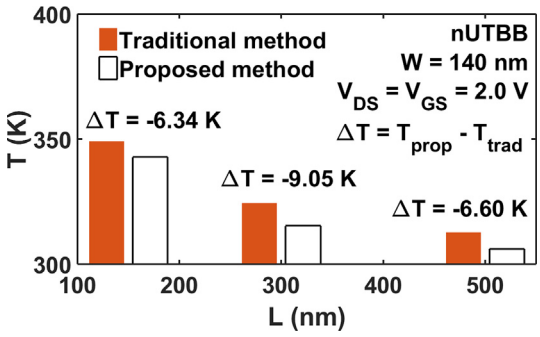

Fig. 13. Comparison of the traditional and proposed methods to estimate channel temperature.

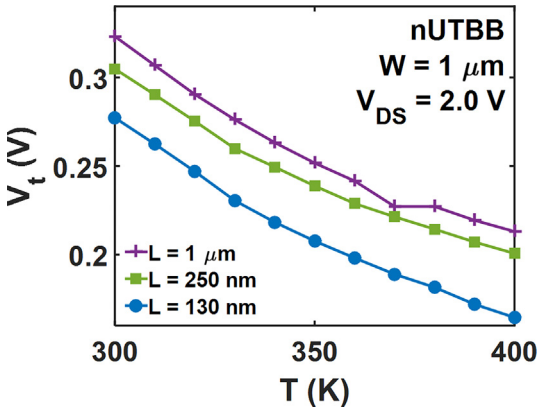

Fig. 14. Extracted threshold voltage versus external temperature.

proposed. Before applying the method, once again the threshold voltage is extracted for each device in the temperature range to be studied, as presented in Fig. 14.

Since the first noticeable change on the V_t values happened for the device with L = 250 nm, the curve for L = 500 nm was suppressed in this figure. Although the behavior of V_t with the temperature in this case is not as linear as the one observed for the simulated devices in Fig. 7, this should not affect significantly the estimation process. Then, the I_D/g_m was calculated at a high, fixed V_{GT}, as shown in Fig. 15.

A reasonable linear fit was possible for the saturation region of the I_D/g_m, suggesting that the model proposed in (13) is adequate for experimental devices. Next, values for g_m and g_{m0} were extracted at multiple temperatures, as presented in Fig. 16.

Despite the difficulty for obtaining smooth g_m curves, a general decreasing trend for g_m at the same V_{GT} for increasing temperatures was

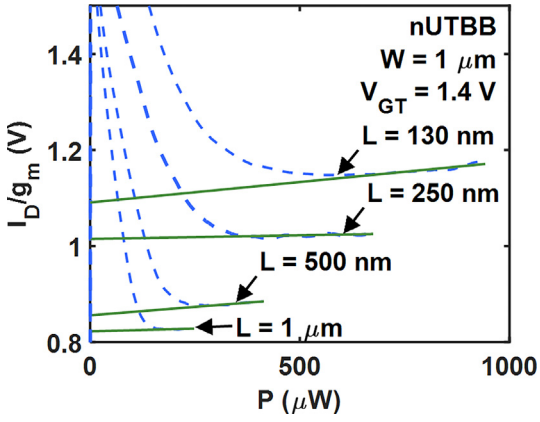

Fig. 15. Measured inverse of the transistor efficiency versus applied power (dashed lines) and linear regression on the saturation region (solid lines).

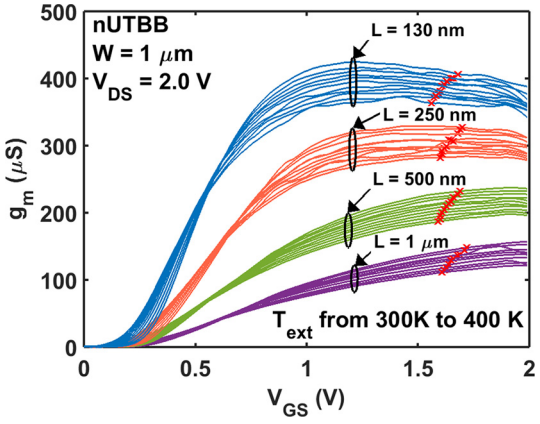

Fig. 16. Measured transconductance versus gate voltage at multiple temperatures for each channel length, with the marks indicating the points where V_{GT} = 1.4 V.

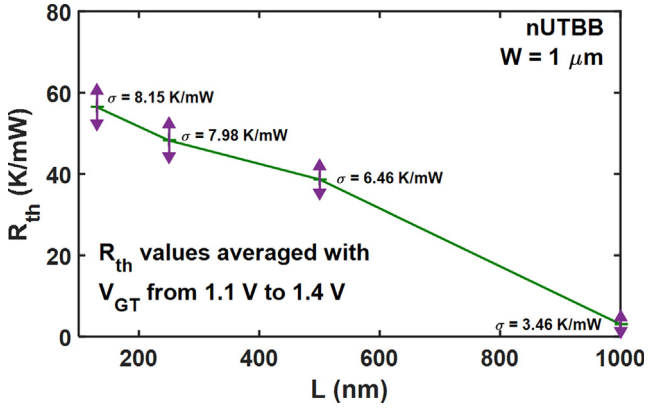

Fig. 17. Averaged thermal resistance versus channel length.

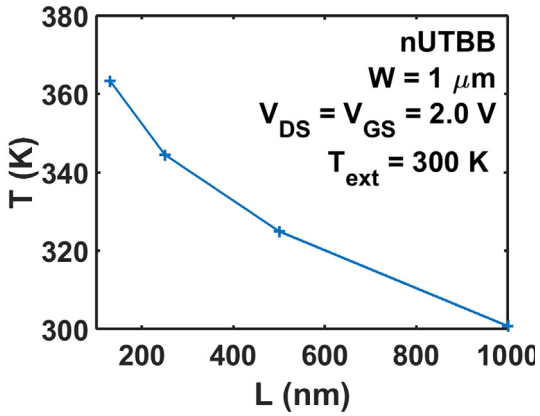

Fig. 18. Experimental temperatures estimated at high power condition as a function of channel length.

observed, which is an expected behavior for the extraction of the c-factor.

As observed in Fig. 10, the extraction of R_{th} should be performed at higher values of V_{GT}, however, since the precise value cannot be determined a priori, the extraction was performed on a range from 1.1 V to 1.4 V of V_{GT}. The obtained results were not perfectly constant, thus, to address this, it was considered that each R_{th} obtained at different V_{GT} was an independent experiment. Consequently, the variations on R_{th} observed are most likely result of noise problems during the measurements, which means that an average R_{th} value in the V_{GT} interval between 1.1 V and 1.4 V could approximate the expected R_{th} value for that device. The results when such a technique is applied are presented in Fig. 17.

To demonstrate how the values varied in the process of experimental extraction, the standard deviation (σ) was presented for each R_{th}. One important remark is that the experimental results cannot be directly compared to those obtained in the simulations, given that these devices are different. However, a similar trend of higher R_{th} for shorter devices is observed, suggesting that the method results in coherent values for experimental devices as well. It was observed that, for all the extractions performed for different V_{GT}, the values of the c-factor remained within a range from 0.5 to 1.1, in a trend similar to that presented in Fig. 12, ensuring the validity of the approximation used. Finally, the worst-case temperature estimated for each one of the devices at high V_{DS} and V_{GS} is presented in Fig. 18.

Once again, the results obtained seem to be coherent with the simulations and with what was expected from theory, as well as with results from other works. Shorter devices present higher currents at the same bias conditions, resulting in more significant SHE, even if the R_{th} of those devices present similar magnitude. The increase of approximately 63 K for the shortest device seems reasonable, considering that in [12], for a UTBB transistor with similar dimensions, an average temperature rise of 37 K was obtained through other extraction methods when half the power used in this work (similar current but at V_{DS} = 1 V) was applied.

6. Conclusions

A new improved method for obtaining R_{th} using I_D/g_m at room temperature and I_D (V_{GS}) at multiple temperatures was proposed. Using this method, it is possible to obtain an estimative of the channel temperature increase due to the SHE very similar to that obtained by the traditional pulsed-like method but using only DC measurements. When applied to the UTBB SOI through simulations, an increase of the channel temperature when L decreases is observed as expected and, comparing to the traditional method, a difference lower than 10 K between the absolute temperatures of the pulsed-like method and our approach was obtained in the worst case for the studied range. When the same procedures were applied to experimental devices, noise in the measurements required the use of an average on R_{th} for different V_{GT}, but nonetheless the results presented trends very similar to those observed in simulations and temperature elevations coherent to other works. Therefore, the use of this method when special equipment and structures are not available to characterize the SHE suffered by a device is well justified.

Acknowledgment

The authors acknowledge CNPq and FAPESP for financial support.

References

[1] Takacs D, Trager J. ESSDERC '87 1987:729–32.
[2] Mcdaid LJ, Hall S, Mellor PH, Eccleston W, Alderman JC. ESSDERC '89 1989:885–8.
[3] Makovejev S, et al. ESSDERC 2014;2014:222–5.
[4] Monga U, et al. IEEE EDL March 2011;32(3):249–51.
[5] Jiang H, Shin S, Liu X, Zhang X, Alam MA. IEEE EDL. 2017. p. 430–3. 4.
[6] Prasad C, Ramey S, Jiang L. IRPS 2017 2017:6A-4.1–7.
[7] Mori CAB, Agopian PGD, Martino JA. EUROSOI -ULIS 2018:1–4.
[8] Wang R, Zhuge J, Huang R, Kim DW, Park D, Wang Y. IEEE EDL May 2009;30(5):559–61.
[9] Rodriguez N, Andrieu F, Navarro C, Faynot O, Gamiz F, Cristoloveanu S. IEEE 2011 International SOI Conference. 2011. p. 1–2.
[10] Tenbroek BM, Lee MSL, Redman-White W, Bunyan RJT, Uren MJ. IEEE TED 1996;43(12):2240–8.
[11] Jenkins KA, Sun JY-C, Gautier J. IEEE TED 1997;44(11):1923–30.
[12] Makovejev S, Olsen S, Andrieu F, Poiroux T, Faynot O, Flandre D, et al. ULIS 2012:109–12.