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Threshold Voltage Extraction Using Conductance–Voltage Method for Nano-Organic/Oxide Thin-Film Transistors: Comparative Study of P- and N-Type Devices

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Threshold voltage is an essential component for a transistor to operate properly. In this work, an alternate technique for obtaining the threshold voltage, which is referred to as the conductance–voltage method, is suggested. In this technique, the threshold voltage is estimated by measuring the change in drain current with an applied gate voltage when the device transits from the weak accumulation to the strong accumulation mode of operation. The 2D simulations are then used to apply this strategy to pentacene-based and amorphous indium-gallium-zinc-oxide-based thin-film transistors (TFTs) in their linear region of operation. These seem promising, and the technique offers a useful tool for enhancing the functionality of complementary organic/oxide TFTs in the future.

1. Introduction

Organic thin-film transistors (OTFTs) have garnered significant attention in the last few decades owing to their numerous advantages, such as flexibility, lightweight, and low-cost fabrication, making them ideal for various applications, including flexible displays, radio frequency identification (RFID) tags,[1] and wearable electronics, allowing for newer unexplored form factors. The first OTFTs were fabricated and analyzed in 1986,[2] leading to extensive research in the field of organic electronics.[3,4] In contrast to traditional inorganic transistors that use silicon, OTFTs employ organic materials such as organic molecules,[5] polymers, or oligomers that can be deposited onto a substrate to create a thin film as the active semiconducting layer. To optimize the performance of OTFTs, it is important to accurately determine key parameters, such as the threshold voltage, which is essential for proper device operation. The linear extrapolation method, which is conventionally employed to extract the threshold voltage in metal oxide semiconductor field effect transistor (MOSFETs), can be extended to OTFTs. This technique entails identifying the x-axis intercept of the linearly extrapolated line from the transfer characteristic curve.[6] Several other methods, such as the constant current (CC) method, second derivative (SD) method, and third derivative method, have also been widely used to extract the threshold voltage from the transfer characteristic curve.[7–10] This study presents a novel approach, known as the conductance–voltage method, for extracting the threshold voltage. This method is simple, straightforward and nondestructive; it preserves the integrity of delicate organic devices during characterization. Its suitability for organic materials enables accurate threshold voltage determination in OTFTs, and its low-frequency operation is ideal for analyzing slow electronic processes. The applicability of the method over a wide temperature range allows for a comprehensive investigation of temperature-dependent behavior. In addition, it provides detailed insights into various device parameters, making it a versatile tool for comprehensive OTFT characterization. Notably, it can be effectively applied to both p-type and n-type devices, making it suitable for studying complementary OTFT architectures and mixed-device configurations.

Both p-type pentacene-based OTFT and n-type amorphous indium-gallium-zinc-oxide (a-IGZO)-based thin-film transistor (TFT) (inorganic) were subjected to this method using the SILVACO TCAD simulation tool from ATLAS TCAD.[11] The investigation delves into the influence of key parameters, such as trap concentration, doping concentration, characteristic temperature, bandgap, and work function, on the threshold voltage. Additionally, the findings were validated by comparing the observed threshold voltage shift with the expected shift. In addition to the factors considered in the present study, the threshold voltage is also influenced by the gate-bias-dependent mobility,[12] mobility enhancement factor,[9] degradation of transconductance caused by parasitic source and drain resistances,[13] and charges trapped at the interface.[14] However, these factors have not been addressed in the current work and are left as potential areas for future research.

2. Basic Concept

In comparison with conventional MOSFETs, the threshold voltage definition in OTFTs is unique because of their operation within the accumulation region. Ideally, OTFTs should exhibit a zero-threshold voltage;[15] therefore, when the gate voltage is applied, the majority of charge carriers are injected from the source to the substrate and accumulate at the insulator–semiconductor

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interface, forming the conduction channel. However, in practice, in the presence of work function differences between the source and gate electrodes, traps, and interfacial dipoles, a minimum voltage (called the zero voltage[10]) is required to form a conduction channel. Zero voltage is equivalent to the threshold voltage of conventional MOSFETs. The value of zero voltage is given by

$$V_{\mathrm{TH}}\,(\mathrm{or})\,V_0 = \pm\frac{q \times n_0 \times W}{C_i} + V_{\mathrm{fb}} \tag{1}$$

where q is the absolute charge of an electron, n_0 is the free carrier density, W is the thickness of the channel, C_i is the capacitance per unit area of the gate insulator, and V_{fb} is the flat-band voltage. The flat-band voltage arises owing to the work function difference between the semiconductor and the gate electrode. The sign on the right-hand side of Equation (1) is defined by the majority of charge carriers in the semiconductor. The value of n_0 varied with traps and doping concentrations. The drain current in a field-effect transistor varies linearly with the gate voltage once the threshold voltage is reached. The drain current for FET devices in the linear region is given by Equation (2):

$$I_{\mathrm{DS}} = C_i \times \mu \times \frac{W}{L}\left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) \times V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2}\right] \tag{2}$$

The region after the flat-band voltage and before the linear region is called the subthreshold region. In this region, the current varies nonlinearly (usually exponentially) with the gate voltage. The proposed method (called the conductance–voltage method) for threshold voltage extraction in OTFTs employs the linear and nonlinear behavior of the drain current. This differential technique method has already been used for accurate calculation of power–law exponents and enables precise inference of trap-filling voltage and trap concentration in two-terminal devices.[16] The same technique can also be used to estimate the V_{TH} in TFTs. The proposed technique given by Equation (3) resembles the function given in CC ratio method (RM).[17] The estimation of the threshold voltage is based on the transition of the drain current from the subthreshold region to the linear region as the gate voltage was varied. The transfer characteristic curve is transformed by taking the logarithm of both the absolute value of the drain current and the absolute value of the gate voltage, which transforms the transfer characteristic curve to an approximate step function. The voltage-dependent function, G (transconductance), is then determined by differentiating this approximated step function curve, resulting in an impulse function, with its peak corresponding to the gate voltage being equal to the threshold voltage or zero voltage.

$$G = \frac{d(\log_{10}(I_{\mathrm{DS}}))}{d(\log_{10}(V_{\mathrm{GS}}))} \tag{3}$$

It is evident that G equals the exponent m when current exhibits a power–law dependency on voltage. As the transistor transits from the subthreshold to the threshold region, function G would therefore show a peak. As a signature of V_{TH}, this unique peak in the G versus V plot makes it easier to visualize than when V_{TH} is extracted from the current–voltage (I–V) curve. Among the different methods for identifying V_{TH}, the use of steady-state I–V characteristics is particularly attractive because it is the simplest measurement technique that is routinely performed. However, the presence of a large number of traps distorts the I–V characteristics, and extraction becomes difficult. The $G(V)$-based V_{TH} extraction method offers several advantages. Differential approaches are known to be more effective at enhancing transitions; as a result, they should be helpful in marking subthreshold to threshold regions. When a current changes from rapidly increasing in the exponential regime (subthreshold zone) to a relatively slower power–law dependence (above the threshold region), the $G(V)$ function produces a strong peak to indicate the transition. This makes it simple to identify a V_{TH}-related transition region. The $G(V)$ method can be effectively employed in various materials and transistor types, making it a valuable tool for the broader electronics community. This comprehensive understanding makes it a powerful tool for understanding the device behavior, optimizing TFT performance, and designing future electronic devices.[18]

Using algebraic manipulations, Equation (3) can be rewritten as

$$G' = \frac{dI_{\mathrm{DS}}/dV_{\mathrm{GS}}}{I_{\mathrm{DS}}/V_{\mathrm{GS}}} \tag{4}$$

Equation (4) represents the ratio of the incremental change in drain current to the incremental change in gate voltage divided by the ratio of drain current to gate voltage. The numerator corresponds to the transconductance, a key parameter characterizing the relationship between changes in the gate voltage and resulting variations in the drain current. A plot of G' (a dimensionless quantity) when plotted with gate voltage gives a peak that can also be used to extract the V_{TH}. In the present work, V_{TH} is extracted using Equation (3) and the analysis of Equation (4) is left as a future work.

3. Results and Discussion

In this section, we aim to extract the threshold voltages of pentacene, and a-IGZO-based OTFTs using the conductance–voltage method in the linear region of operation. The key parameters were systematically varied and the shift in the threshold voltage was analyzed. A bottom-gate top-contact structure was used for the simulation of the TFT, as shown in **Figure 1**. The simulation parameters employed in this study were drawn from previously published experimental investigations that depict realistic behavior.[19,20] The dimensions of the channel and the contacts were

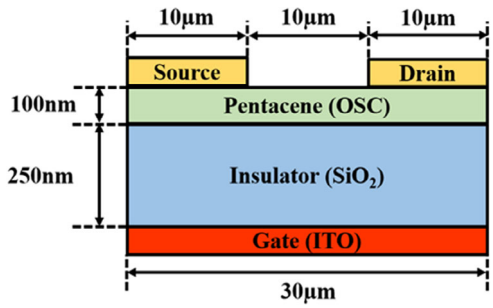

Figure 1. Basic structure used for simulation of pentacene-based organic thin-film transistor.

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chosen based on the desired accuracy of the simulation results, and available computational resources. In simulation studies, dimensions are often kept relatively small to allow convergence of the simulation process and reduce computational complexity.

To validate the simulated outcomes, the simulation results were compared and calibrated against existing experimental data found in the literature. There was a noticeable deviation in the threshold voltage which is attributed to the absence of specific device parameters, such as trap density (bulk, interface, or both) and series resistance in the available experimental results. This absence makes it challenging to precisely adjust the simulated device characteristics to align them with those of the fabricated device. However, it is noteworthy that the device slope and ON current at −40 V closely resembled those observed in the fabricated device. Consequently, it can be inferred that the simulation setup is accurate, supporting its continued utilization.[21]

3.1. Pentacene OTFT (P Type)

In organic semiconductors, conduction occurs because of the presence of conjugated bonds in the organic material. The charge flow is determined by the work function of the source and drain electrodes. In this section, the effect of key parameters, such as the work function, on the threshold voltage is studied and analyzed. In this study, a set of electrical parameters listed in **Table 1** are used to simulate a pentacene-based OTFT.

3.1.1. Traps

The introduction of traps in the OTFT channel resulted in an increase in the free electron concentration. When a negative gate voltage is applied, holes begin to accumulate at the metal–semiconductor interface and become trapped by the electrons present, leading to a decrease in the free hole concentration. As the negative gate voltage increases, all traps are gradually depleted until the gate voltage equals the turn-on voltage (V_{ON}), at which point all traps are depleted, and free holes begin to accumulate. Once the free holes begin to accumulate, a conduction channel is formed when the gate voltage reaches the threshold voltage. By introducing discrete traps at an energy level of 0.69 eV below the conduction band (lowest unoccupied molecular orbital (LUMO)) and increasing their concentration, the threshold voltage shifts toward a negative gate voltage, as shown in **Figure 2**.

Table 1. Physical and electrical parameters used for simulating p-type OTFT.

Symbol	Description/reference	Values
L	Device length	30 μm
W	Device width	1 μm
L_{ch}	Channel length	10 μm
E_g	Bandgap	2.2 eV
ε	Relative permittivity/[19]	3.8
χ_s	Affinity	2.9 eV
N_C	LUMO effective DOS/[19]	1×10^{21} cm^{-3} eV^{-1}
N_V	HOMO effective DOS/[19]	1×10^{21} cm^{-3} eV^{-1}
μ_p	Hole mobility	0.1 cm^2 Vs^{-1}
μ_n	Electron mobility	10^{-5} cm^2 Vs^{-1}
Φ_m	Source and drain work function/[19]	5.1 eV
Φ_m	Gate work function	5.1 eV

3.1.2. Doping

In ideal p-type devices, the operation occurs at negative gate voltages. The introduction of acceptor dopants in organic semiconductors increases the concentration of free holes, which leads to the formation of a conduction channel without requiring gate voltage. The presence of these dopant atoms shifts the V_{ON} toward positive gate voltages. When a positive gate voltage greater than the V_{ON} is applied to a doped semiconductor, the electrons from the source deplete all acceptor dopants, resulting in no current flow. At a gate voltage equal to the V_{ON}, the number of accumulated electrons becomes equal to the acceptor concentration and completely depletes the acceptor dopant.

Further decreasing the gate voltage from the V_{ON} led to an accumulated electron concentration lower than that of the acceptor dopants, resulting in a decrease in the width of the depletion layer and an increase in the concentration of free holes from the acceptor dopants. Therefore, a conduction channel was formed, which contributed to the drain current. As the doping concentration increased, the V_{ON} shifted toward a positive gate voltage. As shown in **Figure 3**, when the doping concentration is increased, the threshold voltage shifts toward a positive gate voltage.[22] It should be noted that in the case of doping, the V_{ON} is considered as the threshold voltage as the device operates in the depletion region at a positive gate voltage.

3.1.3. Bandgap

Ideal organic semiconductors are intrinsic in nature and can conduct both electrons and holes.[5] However, as OTFTs operate in

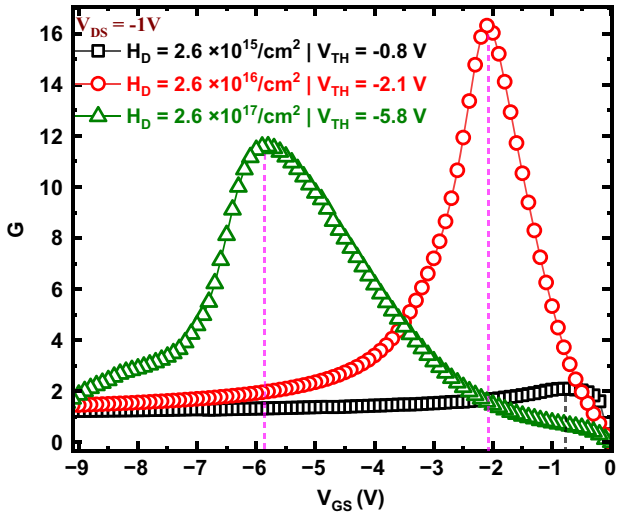

Figure 2. Threshold voltage extracted using the $G(V)$ method for different trap concentrations.

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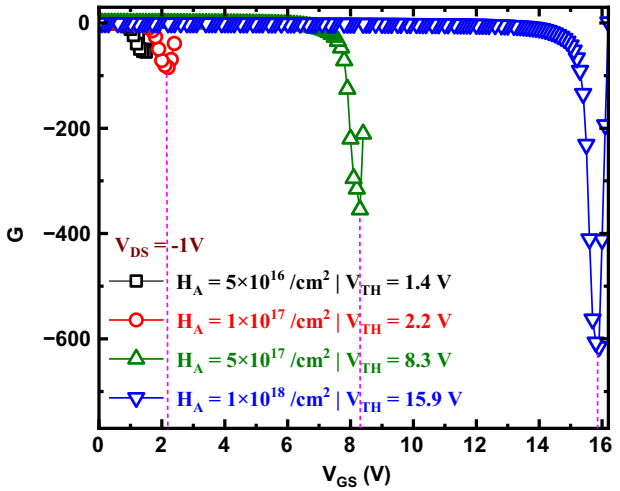

Figure 3. Threshold voltage extracted using the $G(V)$ method for different doping concentrations.

the accumulation region, the polarity of the charge injected through the source electrode is determined by the type of metal–semiconductor contact (Ohmic or Schottky, as shown in **Figure 4**a). For an OTFT to operate as p type, the metal should form an Ohmic contact with the semiconductor, allowing charge carriers to be injected easily into the valence band (highest occupied molecular orbital (HOMO)). Such a contact can be formed when the metal's work function Φ_m is greater than that of the semiconductor Φ_s. The work function of the semiconductor can be calculated using Equation (5):

$$\phi_s = \chi_s + (E_C - E_f) \tag{5}$$

where χ_s is the affinity of the semiconductor, E_C is the conduction band energy level, and E_f is the Fermi energy level. The position of the Fermi level in a semiconductor is primarily determined by its bandgap. In Ohmic contacts, the contact resistance between the metal and semiconductor depends on the difference in the work function ($\Phi_m - \Phi_s$).[23] Increasing the bandgap can lead to an increase in the Fermi energy E_f, which, in turn, can increase the contact resistance at the metal–semiconductor interface and reduce the rate of charge injection into the semiconductor when a gate voltage is applied. Therefore, as the bandgap increased, the threshold voltage also increased. During the simulation, it was difficult to observe changes in the threshold voltage with an increase in the bandgap. To address this issue, uniform traps with a concentration of $H_D = 5 \times 10^{16}\,\mathrm{cm}^{-2}$ are introduced to the organic semiconductor. As shown in **Figure 5**, increasing the bandgap resulted in a shift of the threshold voltage toward the negative gate voltage.

3.1.4. Work Function

As mentioned earlier, in OTFTs, the work function of the metal electrodes must be carefully tuned to ensure that the correct charge carriers are injected into the organic semiconductor layer. As shown in **Figure 6**, when the work function of the metal electrodes is decreased from 5.1 eV, the threshold voltage of the device shifts toward the negative gate voltage. This is due to an increase in contact resistance at the metal–semiconductor interface, which allows fewer charge carriers to be injected into the semiconductor. The increase in the contact resistance can be attributed to the increase in the barrier height (Φ_B) (as shown in Figure 5a) relative to the Fermi level and the valence band (HOMO) of the semiconductor at the metal–semiconductor interface. The barrier height determines the injection of charge carriers (the majority of holes) into the valence band (HOMO) of the semiconductor.[24] It should be noted that the choice of metal for the electrodes can also affect device performance. Different metals have different work functions, which can affect the charge injection and transport properties of devices. Therefore, the selection of appropriate metals for the electrodes is an important consideration in the design and optimization of OTFTs.

3.1.5. Characteristic Temperature

Traps are typically introduced during the fabrication process owing to impurities or defects in the material. In organic semiconductors, traps can arise from a variety of sources such as residual solvents, chemical impurities, or structural defects. These traps can have a significant impact on the performance of organic electronic devices, as they can act as barriers to charge transport, reduce the mobility of charge carriers, and increase the contact resistance at the metal–semiconductor interface

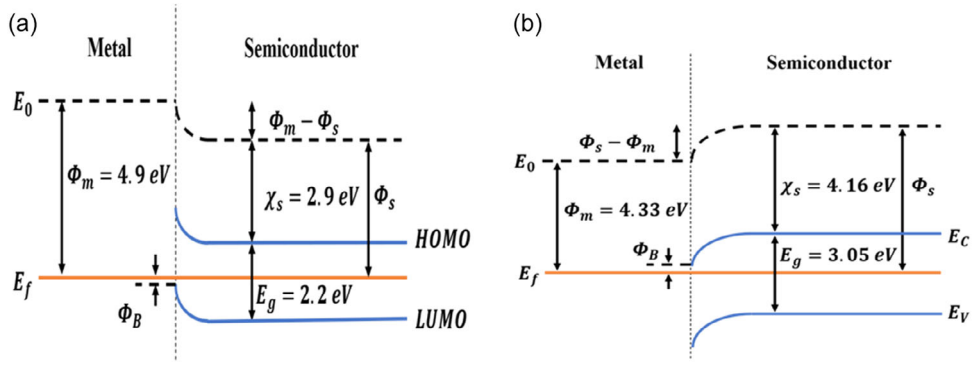

Figure 4. a) Energy band diagram at metal/semiconductor interface with the metal work function of 4.9 eV and semiconductor as pentacene; b) the energy band diagram at metal/semiconductor interface with the metal work function of 4.33 eV and semiconductor as a-IGZO.

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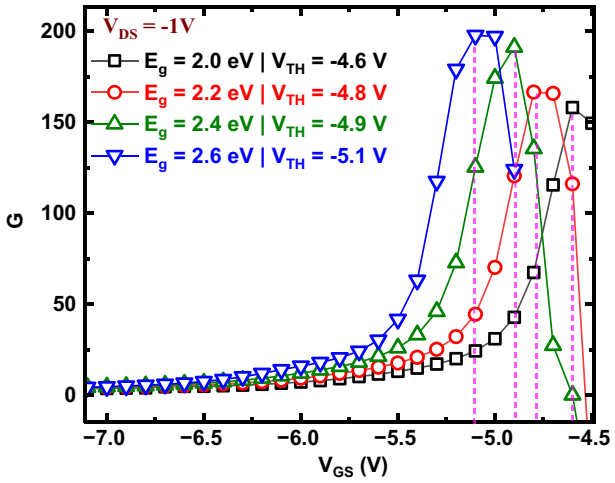

Figure 5. Threshold voltage extracted using the $G(V)$ method for different energy bandgaps.

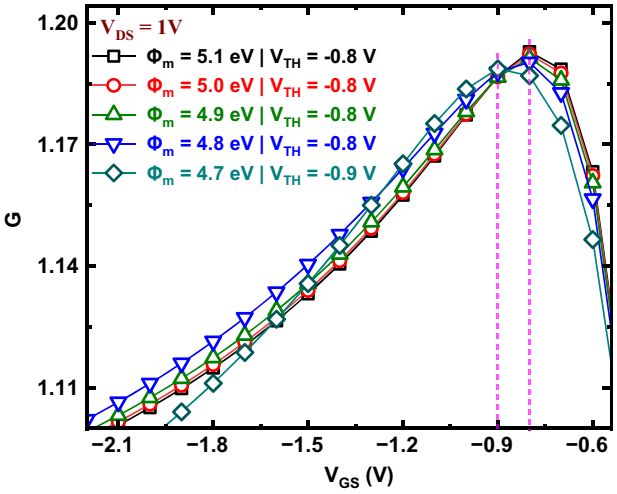

Figure 6. Threshold voltage extracted using the $G(V)$ method for various metal work functions.

(interfacial traps). The exponential distribution of traps[25] across the energy bandgap can be considered a reasonable approximation for the density of trap states ($h(E)$), as traps can be present at any energy level within the bandgap, as described by Equation (6).

$$h(E) = \frac{H_D}{k \times T_C} \times \exp\left(\frac{E_V - E}{k \times T_C}\right) \tag{6}$$

where H_D is the total density of the donor trap states, k is the Boltzmann constant, E_V is the energy level of the valence band, and T_C is the characteristic temperature. The characteristic temperature (T_C) is an important parameter that characterizes the distribution of trap states and can vary from device to device. It should be noted that the characteristic temperature is not a physical temperature but rather an empirical parameter used to represent the trap distribution across the bandgap. An increase in the characteristic temperature can lead to an increase in the distribution of trap

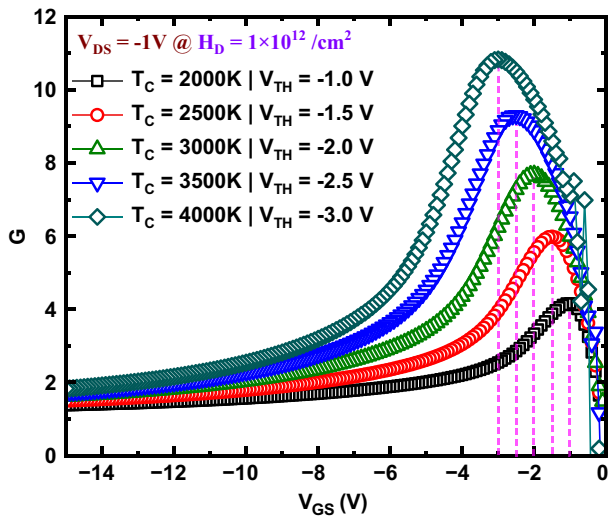

Figure 7. Threshold voltage extracted using the $G(V)$ method for different TCD values.

states over the bandgap, which can increase the threshold voltage. For simulations of different characteristic temperatures, a shift of the threshold voltage toward the negative gate voltage is observed, indicating an increase in the threshold voltage, as shown in **Figure 7**.

3.2. a-IGZO TFT (N-type)

Amorphous TFTs (a-TFTs) are important electronic devices widely used in liquid-crystal displays (LCDs).[26] In amorphous semiconductors, atoms or molecules are randomly arranged to form highly distorted covalent bonds.[27] This random arrangement increases the energy of the localized states, which pushes these states into bandgap forming tail states. The electrical behavior of a-TFTs is primarily determined by the localized tail states and deep states present within the bandgap, as illustrated in **Figure 8**.

This section focuses on the analysis of several key parameters of a-TFTs and their effects on threshold voltage. For this study, a-IGZO was selected as the semiconductor layer for the thin film, as shown in **Figure 9**. **Table 2** lists the relevant electrical and dimensional parameters used in this study.

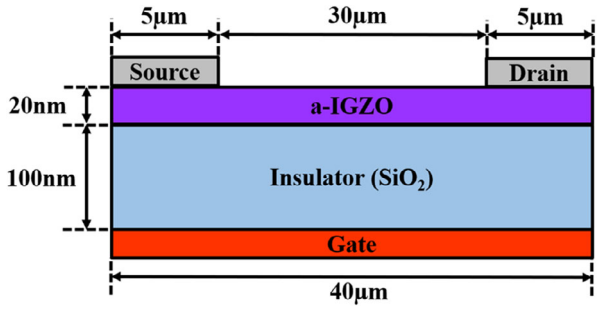

Figure 8. Basic structure used for simulation of amorphous indium-gallium-zinc-oxide-based thin-film transistor.[17]

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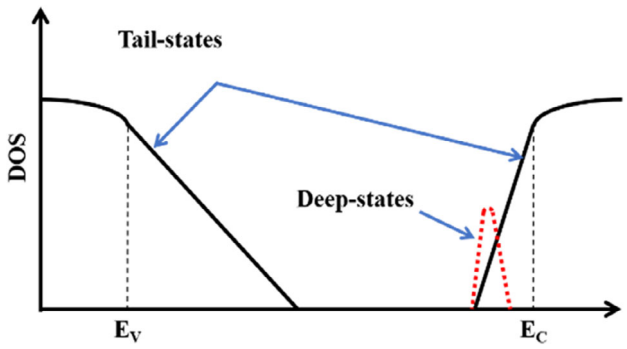

Figure 9. Density of states distribution (in log scale) of tail states and deep states over energy bandgap for a-IGZO.

3.2.1. Gaussian Traps

In amorphous semiconductors, the majority of deep states are thought to be formed by dangling bonds, which are nonbonded atomic states with unpaired electrons that are not fully bonded to neighboring atoms and are located primarily on the surface and cavities of the semiconductor. These dangling bonds are highly reactive and can trap electrons, which can affect the threshold voltage of a device. Because of the large number of dangling bonds present in amorphous semiconductors, they can become pinned to the Fermi level of the semiconductor.[27] This shift in the Fermi level of the semiconductor from its ideal position (without any traps being present in the bandgap) can ultimately affect device performance. These deep states were approximated using a Gaussian distribution, as shown in Equation (7).[28]

Table 2. Physical and electrical parameters used for simulating n-type TFT.

Symbol	Description/reference	Values
L	Device length/[33]	40 μm
W	Device width/[33]	180 μm
L_{ch}	Channel length/[33]	30 μm
E_g	Bandgap/[33]	3.05 eV
ε	Relative permittivity/[33]	10
χ_s	Affinity/[33]	4.16 eV
N_C	Effective DOS of conduction band/[33]	5×10^{18} cm^{-3}
N_V	Effective DOS of valence band/[33]	5×10^{18} cm^{-3}
g_{ta}	Density of conduction band edge states/[33]	1.55×10^{20} cm^{-3} eV^{-1}
g_{td}	Density of valence band edge states/[33]	1.55×10^{20} cm^{-3} eV^{-1}
E_{ta}	Conduction band tail slope/[33]	13 meV
E_{td}	Valence band tail slope/[33]	120 meV
μ_p	Hole mobility/[33]	0.1 cm^2 Vs^{-1}
μ_n	Electron mobility/[33]	15 cm^2 Vs^{-1}
N_{gd}	Peak of donor Gaussian states/[33]	6.5×10^{16} cm^{-3} eV^{-1}
λ_d	Mean level of donor-like Gaussian states/[33]	2.9 eV
σ_d	Standard deviation of donor-like Gaussian states/[33]	0.1 eV
Φ_m	Source and drain work function/[33]	4.33 eV
Φ_m	Gate work function/[33]	5.1 eV

$$g_{ga}(E) = N_{ga} \times \exp\left(\frac{-(E-\lambda_a)^2}{\sigma_a{}^2}\right) \tag{7}$$

where g_{ga} is the density of states (DOS), N_{ga} is the maximum value of the DOS, λ_a is the value of the energy level where the peak of the DOS is located (generally near the Fermi level), and σ_a is the standard deviation. This Gaussian distribution varies from device to device, owing to variations in the fabrication process. Electron conduction cannot occur until all deep traps are filled; therefore, the gate voltage at which all deep-state traps are filled is defined as the threshold voltage. As shown in **Figure 10**, increasing the peak of acceptor Gaussian states from $N_{ga} = 1 \times 10^{17}$ cm^{-3} shifts the threshold voltage toward a positive gate voltage, where $\lambda_a = 1.5$ eV and $\sigma_a = 0.1$ eV. Additionally, it was observed that an increase in N_{ga} by a factor leads to an increase in the threshold voltage by the same factor, indicating a clear dependence on the DOS of deep states.

3.2.2. Doping

In a-IGZO, donor dopants are added to increase the concentration of electrons in the semiconductor and improve current conduction. When V_{GS} is greater than zero, the majority of the electrons accumulate, and the donor dopants in the channel contribute to the source–drain current. However, when V_{GS} is negative, holes accumulate and deplete the donor dopants, leading to a reduction in current conduction. The gate voltage at which all the dopant atoms are depleted, and no further conduction occurs is known as the V_{ON}. When the doping concentration is increased, the V_{ON} is expected to shift toward a negative gate voltage. As anticipated, **Figure 11** shows that the V_{ON} shifts toward a negative gate voltage when the peak doping concentration (N_{gd}, as shown in Equation (8)) of the Gaussian distribution described in Table 2 is increased.

$$g_{gd}(E) = N_{gd} \times \exp\left(\frac{-(E-\lambda_d)^2}{\sigma_d{}^2}\right) \tag{8}$$

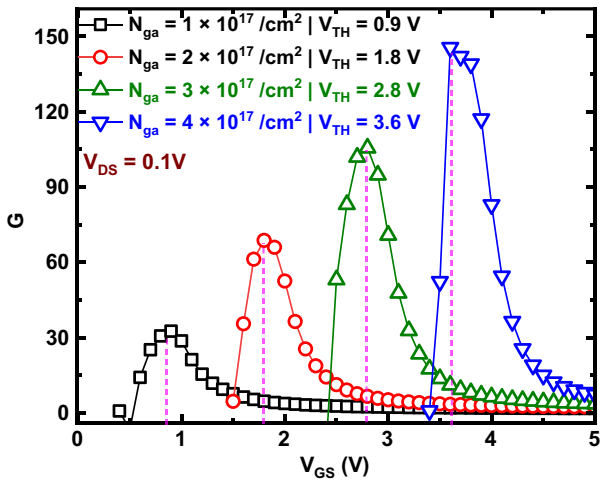

Figure 10. Threshold voltage extracted using the $G(V)$ method for Gaussian traps in a-IGZO.

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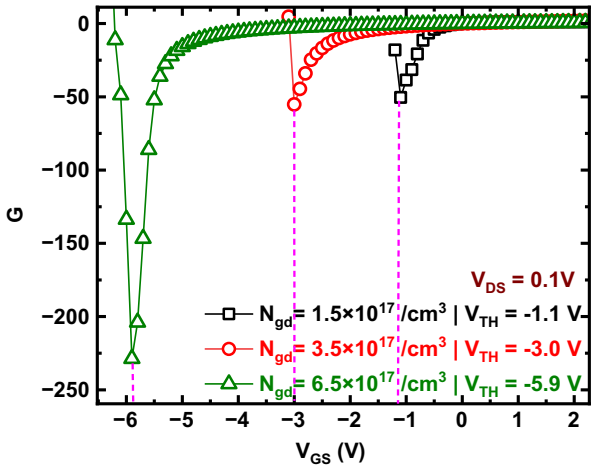

Figure 11. Threshold voltage extracted using the $G(V)$ method for different Gaussian doping concentrations.

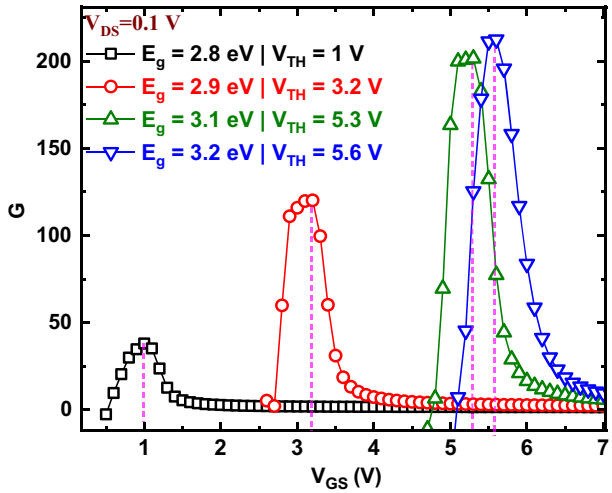

Figure 12. Threshold voltage extracted using the $G(V)$ method for different energy bandgaps in a-IGZO.

Here, the V_{ON} is considered the threshold voltage because the device operates in the depletion region.

3.2.3. Bandgap

The rate of electron injection in an n-type a-TFT depends largely on the energy difference ($\Delta\Phi$) between the work function of the semiconductor and the work function of the source electrode as shown in Figure 4b, which determines the type of contact (Ohmic or Schottky) at the metal–semiconductor interface, which controls the injection rate of carriers from the source to the semiconductor.

To form an Ohmic contact in an n-type semiconductor, the work function of the semiconductor should always be higher than that of metal. The work function of the source electrode (Φ_m) is fixed at 4.33 eV, and the work function of the semiconductor is given by Equation (4). In the case of a-IGZO, which has an electron affinity of 4.16 eV, the value of E_C–E_f can be approximately equal to half of the bandgap ($E_g = 3.08$ eV), resulting in $\Delta\Phi \approx 1.37$, which forms an Ohmic contact ($\Delta\Phi > 0$) at the metal–semiconductor junction. The Fermi level is approximately located in the middle of the bandgap (with no trap states present inside the bandgap and no potential). As the bandgap increases, the position of the Fermi level shifts toward the valence band and increases the semiconductor work function; however, this increase in bandgap has less impact on the threshold voltage. So, to observe a shift in threshold voltage, Gaussian acceptor traps were added 2.9 eV below the conduction band with a peak concentration of $N_{ga} = 6 \times 10^{17}\,\mathrm{cm}^{-3}$ and characteristic decay energy $\sigma_a = 0.1$ eV. As the bandgap increases, the Fermi level moves toward the valence band, resulting in more unoccupied Gaussian trap states. A more positive gate voltage is required to compensate for the increase in unoccupied Gaussian trap states, which raises the threshold voltage. After modeling, it was found that when the bandgap was raised from 2.8 to 3.2 eV, as illustrated in **Figure 12**, the threshold voltage shifted toward positive gate voltage as anticipated.

3.2.4. Work Function

Increasing the work function of the source and drain electrodes in a semiconductor device can reduce band bending at the metal–semiconductor interface, which can lead to an increase in the contact resistance and reduce the number of carriers injected into the semiconductor when the gate voltage is applied. These effects can result in an increase in the threshold voltage required to form a conductive channel in the semiconductor and drive current through the device, upon simulating a-IGZO devices with different metal work functions ranging from 4.3 to 4.6 eV. As seen in **Figure 13**, a hump-like behavior[29] was observed in the transfer characteristics of the device when the metal work function equals 4.6 eV. Two distinct peaks were observed at different gate voltages when the $G(V)$ method was applied. The first peak at a positive gate voltage equal to V_H is

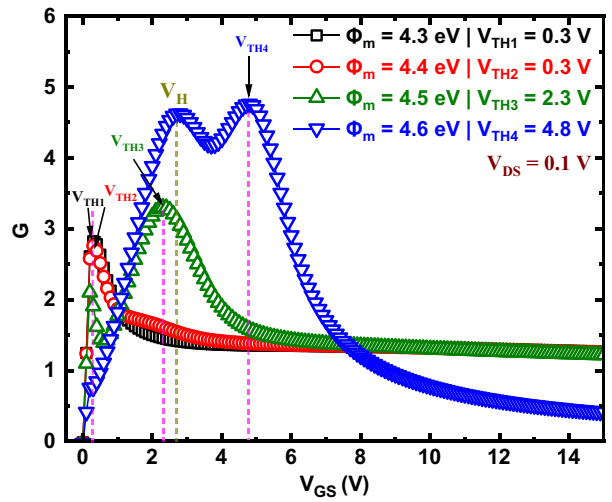

Figure 13. Threshold voltage extraction using the $G(V)$ method for different values of metal work function (Φ_m) of a-IGZO (n-type) device.

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attributed to the formation of parasitic edge channels, which are caused by positive charges accumulating from the electrodes and becoming trapped in shallow states away from the gate–insulator/active layer interface.[30] This resulted in the formation of a conduction channel. The second peak at a positive gate voltage equal to V_{TH} was due to the formation of a second conduction channel from the accumulated electrons at the gate–insulator/active layer interface. The second peak was considered the final threshold voltage. This hump-like behavior observed at work functions 4.6 eV is likely because of an increase in the Schottky barrier potential, which impedes electron flow and allows more flow of holes at higher metal work functions. As expected, the final threshold voltage increased with an increase in the work function of the source and drain electrodes.

3.2.5. Characteristic Decay Energy (σ)

The threshold voltage in amorphous semiconductors can be described as the gate voltage at which all deep trap states are filled with charges, resulting in an increased Fermi level near the conduction band and contributing to measurable current flow in the device.[30,31] The characteristic decay energy is the standard deviation of the Gaussian distribution of the density of the deep trap states (from Equation (7)) near the Fermi level. It characterizes the deep trap state dispersion over the bandgap. The value of the characteristic decay energy can vary depending on the specific properties of the amorphous semiconductor material and the nature of the defects or trap states present. As the characteristic decay energy increased, the traps in the deep states increased, thereby increasing the threshold voltage. As shown in **Figure 14**, by introducing Gaussian distribution trap states at $\lambda_a = 2.9$ eV and $N_{ga} = 8 \times 10^{17}$ cm^{-3} and varying characteristic decay energy (σ_a) from 0.01 to 0.02 eV, it is observed that threshold voltage had shifted toward positive gate voltage.

It is crucial to analyze the I–V properties of a transistor before conducting further investigations of the device. The I–V characteristics provided initial insights into the transistor type (n/p), operation mode (linear/saturation), and contact resistance

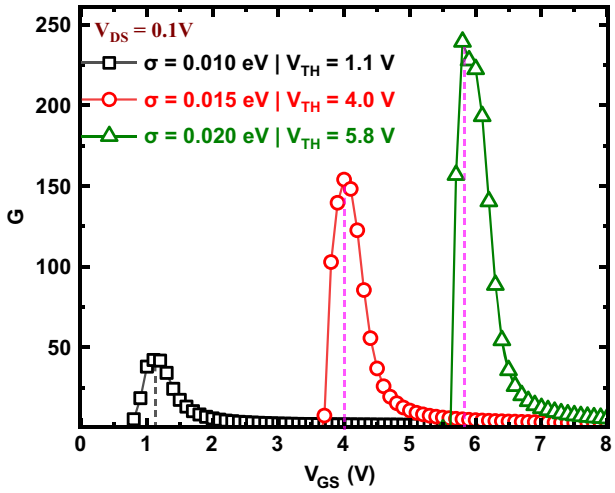

Figure 14. Threshold voltage extracted using the $G(V)$ method for different characteristic decay energies.

(s-shaped characteristics). These features provide quick and direct information about the transistor without requiring a complex model. Furthermore, these characteristics play a crucial role in extracting vital parameters from an OTFT, such as mobility, threshold voltage, ON/OFF ratio, and subthreshold slope. This process aids in gaining a firsthand understanding of a device. **Figure 15** displays the I–V characteristics of both the n- and p-type transistors showing bandgap, Gaussian trap, and characteristic decay energy for n-type transistor and trap, work function, and characteristic temperature for p-type transistor.

A comparison of V_{TH} extracted from different methods for both n-type and p-type using steady-state and the proposed method is presented in **Table 3**. The conventional methods used to compare are the linear extrapolation method (ELR), CC method, transconductance linear extrapolation method (GMLE), SD method, RM, inverse ratio method (VX), and transition method (TM).[7] The comparison is made for one value of trap and work function for both n- and p-type transistors. As is evident from Table 3, for an n-type transistor and for a trap value of 4.0×10^{17} cm^{-2}, the threshold voltage ranges from 3.6 to 4.1 V showing that the V_{TH} value extracted from all other alternative methods falls very close to the proposed method.

The percentage error is calculated by taking the reference value of 3.6 V for n-type material for a trap density of 4.0×10^{17} cm^{-2} extracted from the $G(V)$ method as shown in Table 3. For alternative methods such as CC, GMLE, SD, RM, and VX, the margin of error falls within an acceptable range of 10%. In contrast, the ELR, TM, and CC methods exhibit a slightly higher error rate, ranging between 12% and 16%. It is noteworthy that each of the alternative methods carries certain limitations and is often dependent upon factors such as trap density and temperature. These methods also depend on the range of the gate voltage chosen to extract the V_{TH} and thus fail to produce a unique value of V_{TH} as different range of V_{GS} gives different values of V_{TH}.

To verify the correctness and the accuracy of the proposed method, additional simulations were conducted in the maple environment using a simple, continuous and analytical polylogarithmic model for TFTs[32] in which the V_{TH} is already known and is equal to 4.5 V. This model is based on only three parameters and can be expressed as

$$I_{DS}(V_{GS}) = -I_0 L_{im}\left[-\exp\left(\frac{V_{GS} - V_{TH}}{n \times V_{TH}}\right)\right] \tag{9}$$

where L_{im} is the polylogarithm of order m, I_0 is a parameter that depends on the device's geometry and physical properties, and n is the quality factor parameter. The values of these parameters are $m = 1.5$, $V_{TH} = 4.5$ V, $n = 15$, and $I_0 = 1e^{-6}$ A.[32] The threshold voltage is extracted for the proposed and the SD method for comparison. The values obtained from the proposed method resemble very close to the value of 4.5 V used in the simulation as shown in **Figure 16**.

4. Conclusion

The new method of extracting the threshold voltage in OTFTs uses transfer characteristics to determine V_{TH}, which is essential for their successful implementation in modern electronics. The

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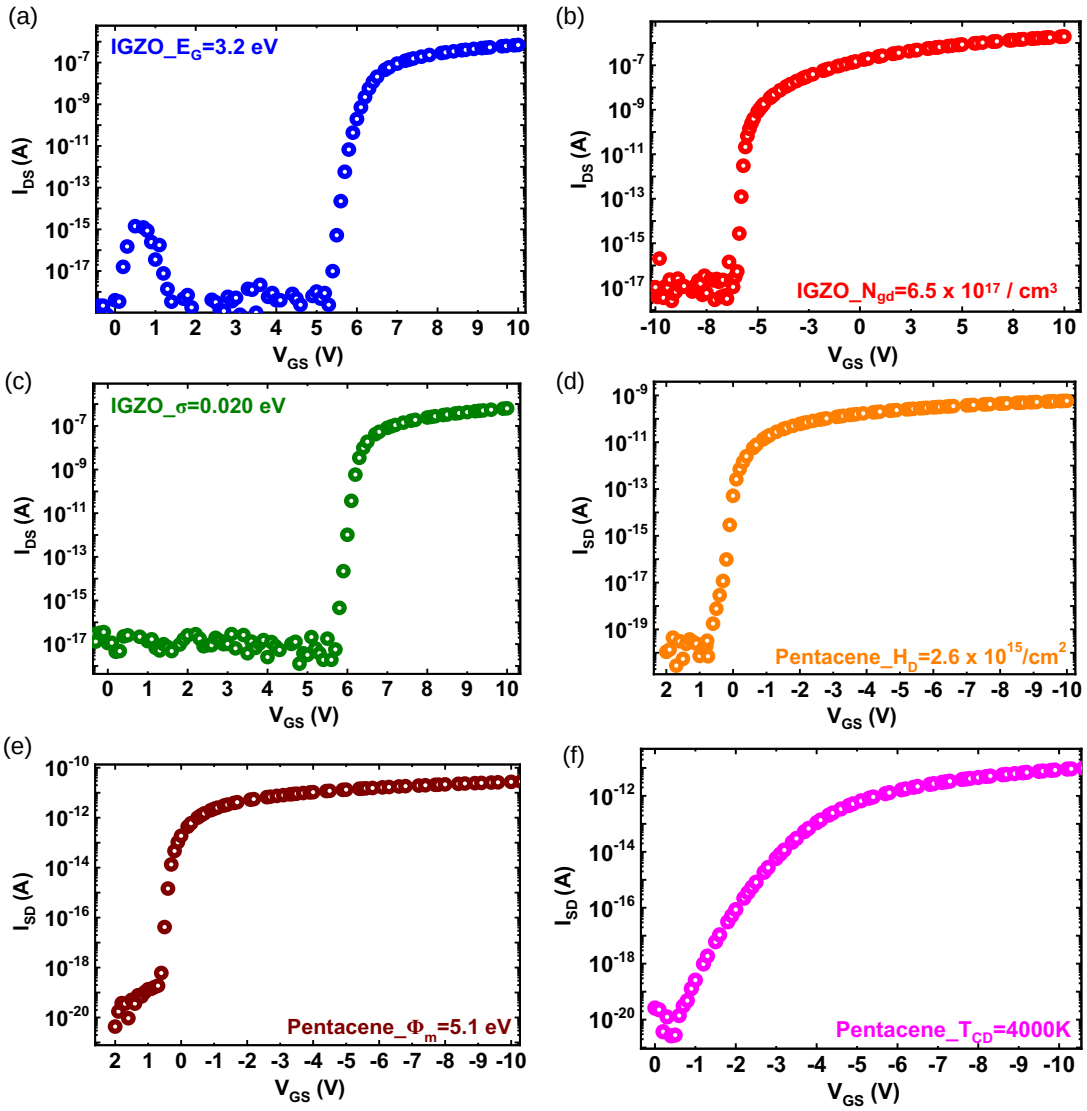

Figure 15. *I–V* characteristics of IGZO for a) a bandgap of 3.2 eV, b) Gaussian trap of 6.5×10^{17} cm^{-3}, and c) characteristic decay energy of 0.020 eV. *I–V* characteristics of pentacene for d) a trap of 2.6×10^{15} cm^{-2}, e) work function of 5.1 eV, and f) characteristic temperature of 4000 K.

Table 3. Comparison of V_{TH} extracted using G(V) and conventional methods for both p- and n-type material focusing on work function and trap.

Extraction methods	p type		n type		
	$\phi_m = 5.1$ eV	$H_D = 2.6 \times 10^{17}$ cm^{-2}	$\phi_m = 4.3$ eV	$N_{ga} = 4.0 \times 10^{17}$ cm^{-2}	% Error
G(V)	−0.8 V	−5.8 V	0.3 V	3.6 V ←	Reference value
ELR	−0.2 V	−5.5 V	0.5 V	4.1 V	12.2%
CC	−0.9 V	−9.5 V	0.4 V	4.3 V	16.0%
GMLE	−0.4 V	−5.3 V	−0.1 V	4.0 V	10.0%
SD	−0.1 V	−5.4 V	0.4 V	3.9 V	7.7%
RM	−0.5 V	−5.3 V	0.5 V	4.0 V	10.0%
VX	−0.3 V	−6.5 V	0.3 V	3.8 V	5.3%
TM	−0.15	−5.5 V	0.4 V	4.1 V	12.2%

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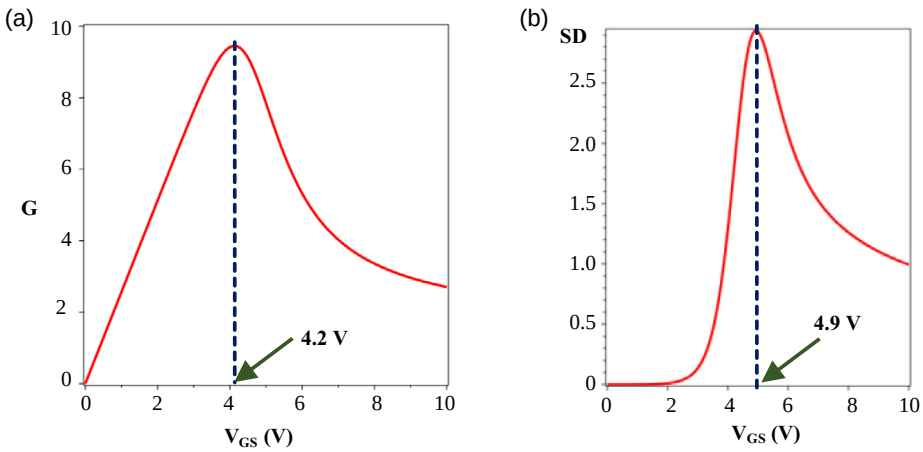

Figure 16. Comparison of V_{TH} obtained from the a) $G(V)$ method and b) SD method using Equation (9).

$G(V)$ method was applied to OTFTs made with two different materials, pentacene and a-IGZO, and 2D simulations were used to analyze the shift in V_{TH} with changes in the key parameters. This new approach is a valuable tool for optimizing the OTFT performance in future applications.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

a-indium gallium zinc oxides, organic thin-film transistors (OTFTs), pentacenes, threshold voltage extractions

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[1] V. Fiore, P. Battiato, S. Abdinia, S. Jacobs, I. Chartier, R. Coppard, G. Klink, E. Cantatore, E. Ragonese, G. Palmisano, *IEEE Trans. Circuits Syst. I: Regul. Pap.* **2015**, *62*, 1668.
[2] A. Tsumura, H. Koezuka, T. Ando, *Appl. Phys. Lett.* **1986**, *49*, 1210.
[3] C. D. Dimitrakopoulos, P. R. L. Malenfant, *Adv. Mater.* **2002**, *14*, 99.
[4] G. Horowitz, *J. Mater. Res.* **2004**, *19*, 1946.
[5] Z. A. Lamport, H. F. Haneef, S. Anand, M. Waldrip, O. D. Jurchescu, *J. Appl. Phys.* **2018**, *124*, 071101.
[6] K. Terada, K. Nishiyama, K. I. Hatanaka, *Solid-State Electron.* **2001**, *45*, 35.
[7] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. T. Barrios, J. J. Liou, C. S. Ho, *Microelectron. Reliab.* **2013**, *53*, 90.
[8] N. Makris, M. Bucher, L. Chevas, F. Jazaeri, J. M. Sallese, *IEEE Trans. Electron Devices* **2020**, *67*, 4658.
[9] R. Rodriguez-Davila, A. Ortiz-Conde, C. Avila-Avendano, M. A. Quevedo-Lopez, *IEEE Trans. Electron Devices* **2019**, *66*, 2979.
[10] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, M. Hajlaoui, *Adv. Mater.* **1998**, *10*, 923.
[11] S. ATLAS User's Manual, Inc. ATLAS User's Manual, SILVACO, Inc, **2016**.
[12] D. Guo, T. Miyadera, S. Ikeda, T. Shimada, K. Saiki, *J. Appl. Phys.* **2007**, *102*, 023706.
[13] S. Jun, H. Bae, H. Kim, J. Lee, S.-J. Choi, D. H. Kim, D. M. Kim, *IEEE Electron Device Lett.* **2015**, *36*, 144.
[14] A. Bolognesi, M. Berliocchi, M. Manenti, A. DiCarlo, P. Lugli, K. Lmimouni, C. Dufour, *IEEE Trans. Electron Devices* **2004**, *51*, 1997.
[15] K. Fukuda, Y. Takeda, M. Mizukami, D. Kumaki, S. Tokito, *Sci. Rep.* **2014**, *4*, 3947.
[16] S. M. H. Rizvi, B. Mazhari, *IEEE Trans. Electron Devices* **2018**, *65*, 3430.
[17] A. Ortiz-Conde, A. Sucre Gonzalez, R. Torres-Torres, J. Molina, R. S. Murphy-Arteaga, F. J. García Sánchez, *IEEE Trans. Electron Devices* **2016**, *63*, 3844.
[18] P. Kumari, A. D. D. Dwivedi, *Glob. J. Res. Eng.* **2019**, *19*, 7.
[19] R. Agarwal, *Silicon* **2022**, *14*, 1315.
[20] R. Nirosha, R. Agarwal, *J. Mater. Sci.: Mater. Electron* **2023**, *34*, 2120.
[21] B. Lüssem, M. L. Tietze, H. Kleemann, C. Hoßbach, J. W. Bartha, A. Zakhidov, K. Leo, *Nat. Commun.* **2013**, *4*, 2775.
[22] C. Liu, Y. Xu, *Mater. Today* **2014**, *18*, https://doi.org/10.1016/j.mattod.2014.08.037.
[23] J. C. Scott, G. G. Malliaras, *Chem. Phys. Lett.* **1999**, *299*, 115.
[24] P. Mark, W. Helfrich, *J. Appl. Phys.* **1962**, *33*, 205.
[25] T. Kamiya, K. Nomura, H. Hosono, *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305.
[26] A. Rockett, *The Materials Science of Semiconductors*, Springer, New York, NY **2007**.
[27] E. K. H. Yu, S. Jun, D. H. Kim, J. Kanicki, *J. Appl. Phys.* **2014**, *116*, 154505.
[28] T.-C. Fung, Amorphous In-Ga-Zn-O Thin Film Transistor for Future Optoelectronics, **2010**.
[29] M. Mativenga, M. Seok, J. Jang, *Appl. Phys. Lett.* **2011**, *99*, 122107.

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[30] S. Sambandan, *Semiconductors*, CRC Press, Boca Raton **2012**, https://doi.org/10.1201/b12683.
[31] M. J. Powell, *IEEE Trans. Electron Devices* **1989**, *36*, 2753.
[32] A. Ortiz-Conde, C. Ávila-Avendaño, J. A. Caraveo-Frescas, M. A. Quevedo-López, F. J. García-Sánchez, *Solid-State Electron.* **2022**, *188*, 108218.
[33] J. Martins, P. Barquinha, J. Goes, *Technological Innovation for Cyber-Physical Systems. DoCEIS 2016. IFIP Advances in Information and Communication Technology* (Eds: L. M. Camarinha-Matos, A. J. Falcão, N. Vafaei, S. Najdi), Vol. *470*, Springer, Cham **2016**, https://doi.org/10.1007/978-3-319-31165-4_52.

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