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Interface trap density in ITO/Si Schottky junction photodetectors

Yaming Li [b,1], Dianbo Liu [a,1], Ruixi Liu [a], Yunxiao Cui [a], Yunfei Liu [a], Ziyi Ma [a], Yuewen Liu [a], Jiaxuan Wang [a], Ziqian Li [a], Yusen Dong [a], Jiaxin Li [a], Chenxi Du [a], Guihua Liao [a], Chong Li [a,*]

[a] Key Laboratory of Optoelectronics Technology, School of Information Science and Technology, Beijing University of Technology, Beijing, 100124, China
[b] Beijing Research and Development Center, The 54th Research Institute of China Electronics Technology Group Corporation (CETC54), Beijing, 100070, China

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ABSTRACT

Interface trapping is a notorious effect that is known to limit the performance of Schottky junction photodetectors. In this paper, the interface traps and mobility mechanism of silicon Schottky junction photodetectors were studied with two different electrode structures, namely, field and Schottky structures. The dark current of the devices mainly originated from the junction area-dependent dark current. The characteristic tunneling energies of the devices with field and Schottky structures were 0.095 and 0.102eV, respectively, and their activation energies were 0.193 and 0.294eV, respectively, which are less than half the band gap of silicon. These values are consistent with the devices displaying a trap-assisted tunneling (TAT) mechanism. An equivalent circuit model of metal–insulator–semiconductor interface traps was constructed. The interface trap densities of the devices with field and Schottky structures were calculated to be 1.37×10^{10} and 3.96×10^{11}/(cm^2•eV), respectively. Thus, the field structure can effectively suppress the current arising from trap-assisted tunneling.

1. Introduction

Schottky junction photodetectors (SJPDs) have attracted much attention because of their unique internal photoemission mechanism, which is dominated by the majority carrier [1–3]. The electric field of Schottky devices extends from the device surface, resulting in high-speed drifting of photocarriers without low-speed diffusion [4]. SJPDs have the advantage of high-frequency performance, fast response speed, and short charge storage time [5,6]. However, traditional silicon (Si) SJPDs suffer from low responsivity because of the light shielding by metal electrodes and their thin depletion region [7]. Therefore, transparent conductive materials such as graphene and indium tin oxide (ITO) are used to improve the conductivity and transparency of SJPDs. The traps, state, and quality of the interface between the transparent electrode and semiconductor determine SJPD performance, including dark current, spectral responsivity, and bandwidth [8–10].

The most common transparent conductive material is ITO, which has a mature production process and is widely used in Si solar cells [11]. However, the limitations of the ITO/Si interfaces of SJPDs result in high leakage current, high series resistance, and low responsivity at short wavelength [12,13]. Several solutions have been proposed to suppress the formation of interface traps and states and improve the performance of SJPDs. A common solution is to insert an ultrathin metal film between the Si and ITO layers to increase the barrier height and lower the leakage current without introducing additional resistance. For example, inserting a silver (Ag) film decreased the dark current by a factor of 2300; an ITO/Ag/n-Si SJPD displayed a rectification ratio of 4×10^5 at ±1 V and dark current density of 2.4×10^{-3} mA/cm^2 at −1 V [14]. Gold (Au) is also a suitable interfacial film for ITO/Si devices. ITO/Au/n-Si SJPDs exhibited a low dark current density of 3.7×10^{-4} mA/cm^2 at −1 V and high rectification ratio of 1.5×10^8 [15]. Moreover, spherical Au nanoparticles (NPs) have been used to extend the absorption spectrum of devices to the near-infrared region. An ITO/Au/Au NPs/n-Si SJPD showed a high responsivity of 22.82 mA/W at 1310 nm, which is longer than the intrinsic absorption edge of Si (~1100 nm). Another solution to improve interfaces in SJPDs is including an oxide insulating layer to lower the density of lattice mismatches and trapping sites. The photoresponse ratios of an ITO/copper(II) oxide/Si photodetector were one order of magnitude higher than those of the corresponding ITO/Si photodetector over a broad wavelength range [16].

In this paper, SJPDs with field and Schottky structures are designed, fabricated, and analyzed. The main sources of dark current in the two kinds of SJPDs are discussed according to the dark currents measured in the temperature range of 80–300K. Based on the interface-trap

* Corresponding author.
E-mail address: lichong@bjut.edu.cn (C. Li).
[1] Equal contribution to the work.

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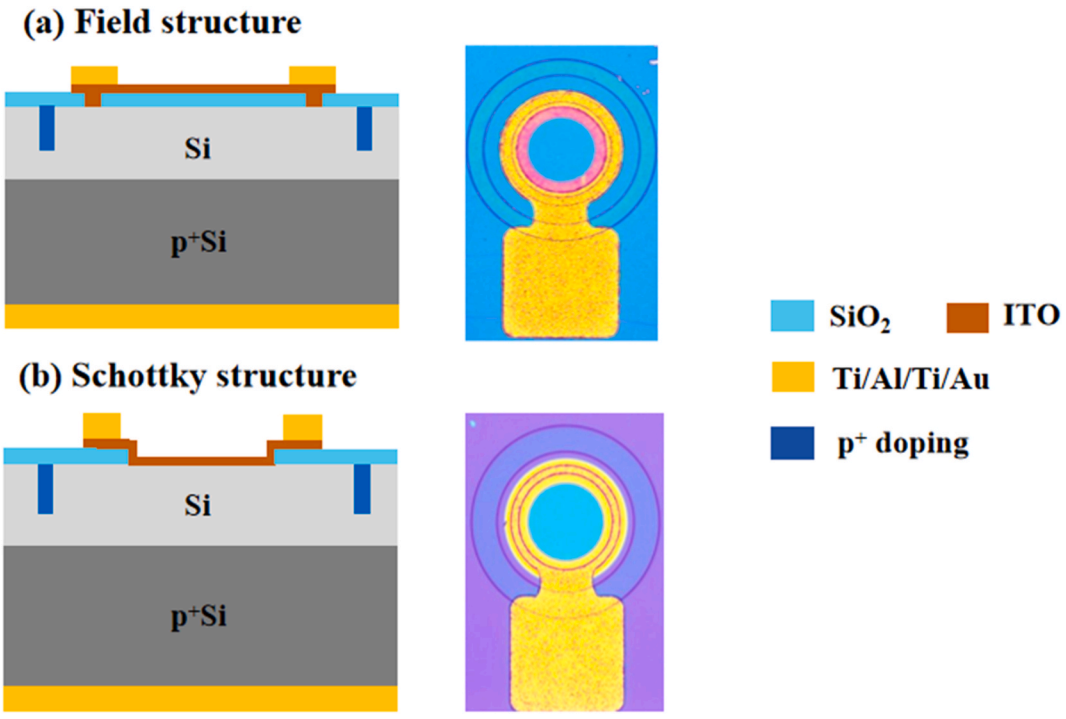

Fig. 1. Schematic diagrams (left) and photomicrographs (right) of photodetectors with (a) field and (b) Schottky structures.

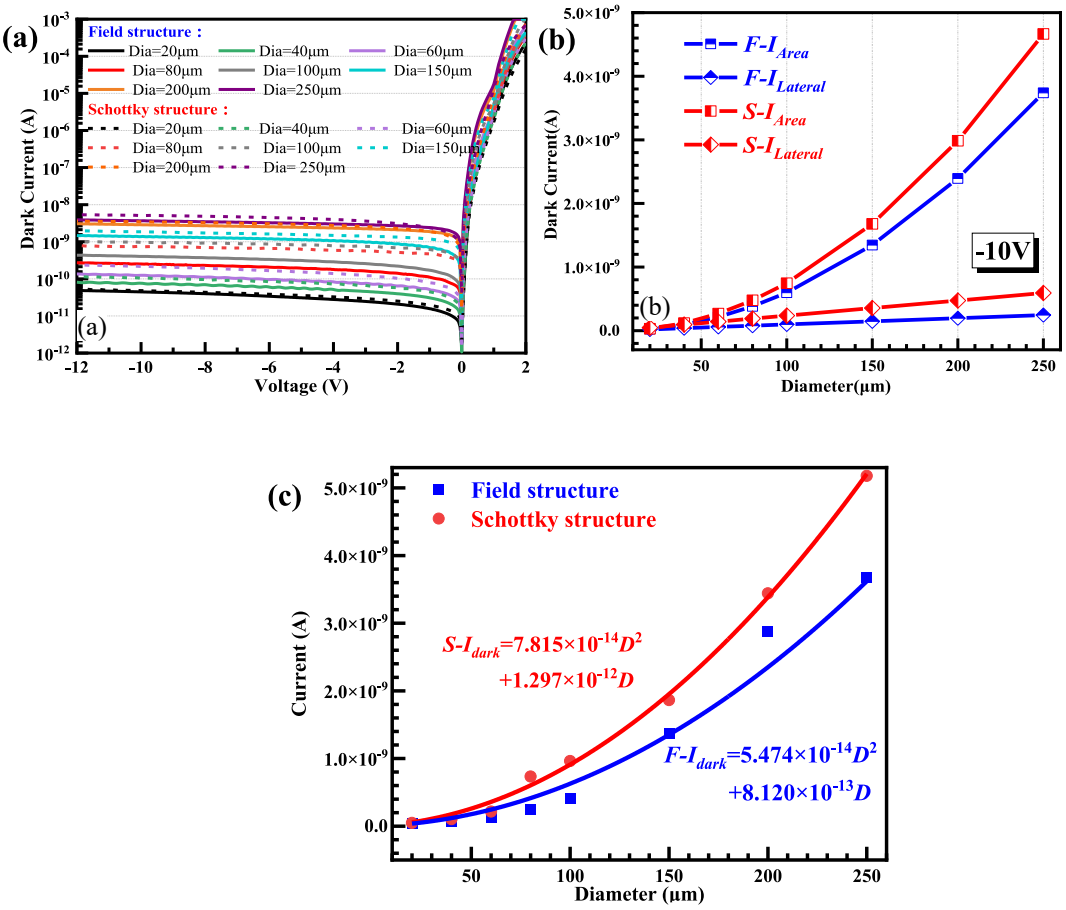

Fig. 2. (a) Dark *I-V* characteristics and (b) leakage current components of SJPDs with different diameters. (c) Relationship between dark current and mesa diameter.

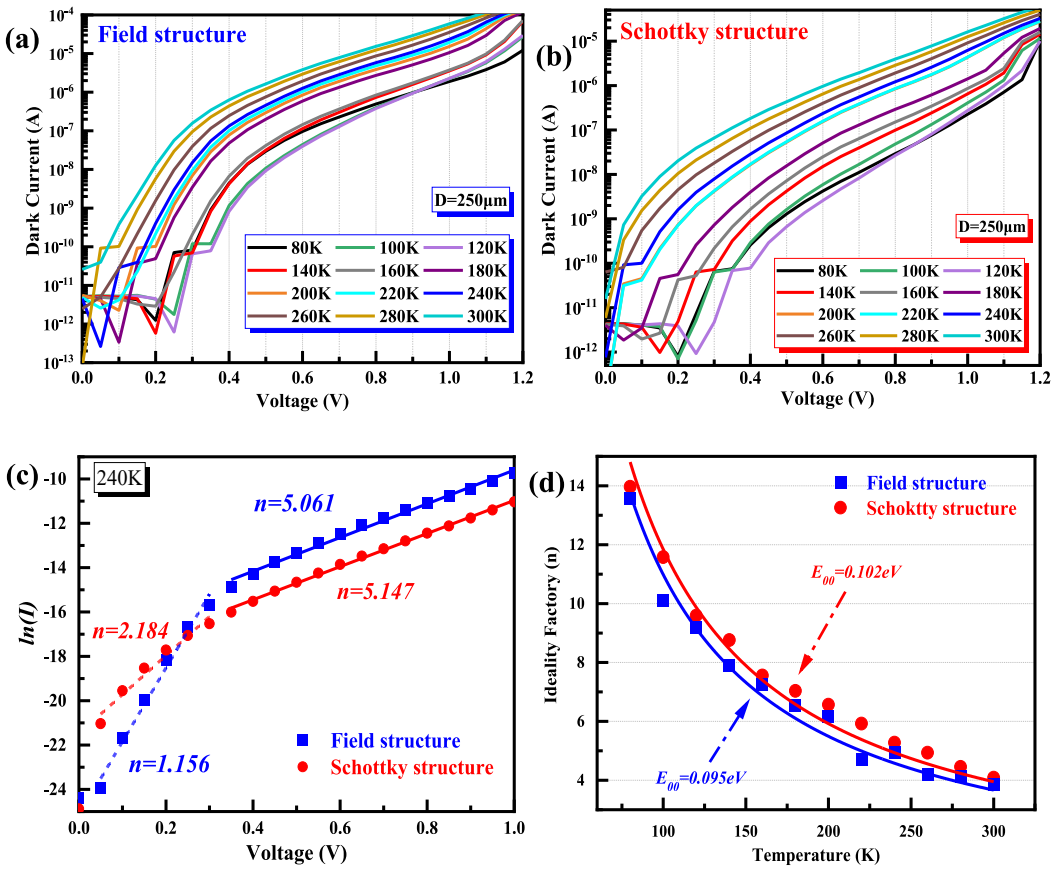

Fig. 3. Forward *I–V* characteristics of devices with (a) field and (b) Schottky structures and a diameter of 250 μm at different temperatures. (c) Ideality factors of devices under different bias voltages. (d) Tunneling characteristic energies E_{00} of devices fitted by their ideality factors at different temperatures.

equivalent circuit model, the interface trap densities of the field and Schottky devices are calculated.

2. Device structure

Fig. 1 shows schematic diagrams and photomicrographs of the Si SJPDs, including the field structure with a ring electrode and Schottky structure with a full-surface electrode. A 20-μm-thick layer of Si (resistivity >1000 Ω cm,$N_s = 10^{13}$~10^{14}/cm^3) was epitaxially grown on a p-type Si substrate (substrate concentration $N_s = 10^{18}$~10^{19}/cm^3). The isolation guard ring was formed by p-type ion implantation. The devices were annealed at 1000 °C in a nitrogen atmosphere for 30s to repair implantation defects and activate and redistribute impurity ions. In Schottky contact preparation, the field electrode region is defined by two-sided alignment photolithography, and after being degumped by O_2 plasma (100W, 30 s), ITO layers are deposited in an Ar:O_2 = 20:1 atm by magnetron sputtering. Then, three layers of photoresist (LOR 3B/AZ 5214/PMMA) were used to optimize the step coverage, and Ti/Al/Ti/Au (15/400/10/100 nm) multilayer metal was deposited successively by magnetron sputtering. Finally, the electrode pattern was completed by ultrasonic peeling in 60 °C acetone for 10 min. The process ensures low resistance ohmic contact and structural reliability through interface cleaning and metal layer stacking.

3. Results and discussion

3.1. Location of leakage current

The dark current–voltage (*I–V*) characteristics of SJPDs with different diameters were characterized by a Keithley 4200 semiconductor analyzer with two-point probe mode (sweep range: 12V–2V, step 0.1V, delay 100 ms) at room temperature (25 °C) without light. The results for the two types of devices with diameters of 20–250 μm are shown in Fig. 2(a). The leakage current of the Schottky device with a diameter of 100 μm was 0.962 nA at −10V, and the corresponding leakage current density was 0.012 mA/cm^2. The leakage current of the field device of the same size was 0.403 nA and its leakage current density was 0.005 mA/cm^2.

The reverse dark current (I_{Dark}) can be decomposed into a length-dependent current ($I_{Lateral}$) generated from the lateral transport of carriers, area-dependent current (I_{Area}) generated in or close to the depletion region, and a compensation current ($I_{M\text{-}S}$), which is independent of area and circumference [17,18]. Thus, I_{Dark} can be expressed as:

$$I_{Dark} = J_{Area} \times D^2 + J_{Lateral} \times D + I_{M-S} \quad (1)$$

Generally, $I_{M\text{-}S}$, which is independent of device size, is small enough to be negligible. Therefore, a plot of I_{Dark} versus the device diameter (D) could be fitted with a quadratic function without a constant term. I_{Dark} of the two structures at −10 V is presented in Fig. 2(c). The area-dependent dark current coefficient (J_{Area}) of the devices with a field structure was 5.474×10^{-6}A/cm^2 and their length-dependent coefficient ($J_{Lateral}$) was 8.12×10^{-9}A/cm. J_{Area} of the Schottky devices was 7.815×10^{-6}A/cm^2 and their $J_{Lateral}$ was 1.297×10^{-8}A/cm. Obviously, the leakage current of the devices with a field structure was lower than that of the devices with a Schottky structure. The area-dependent leakage current is the main source of leakage current for both structures, as shown in Fig. 2(b). Because of the highly mature complementary metal–oxide–semiconductor process, high-quality Si crystal, and high electric field near the ITO/Si interface, the leakage current of the SJPDs is mainly generated at this interface.

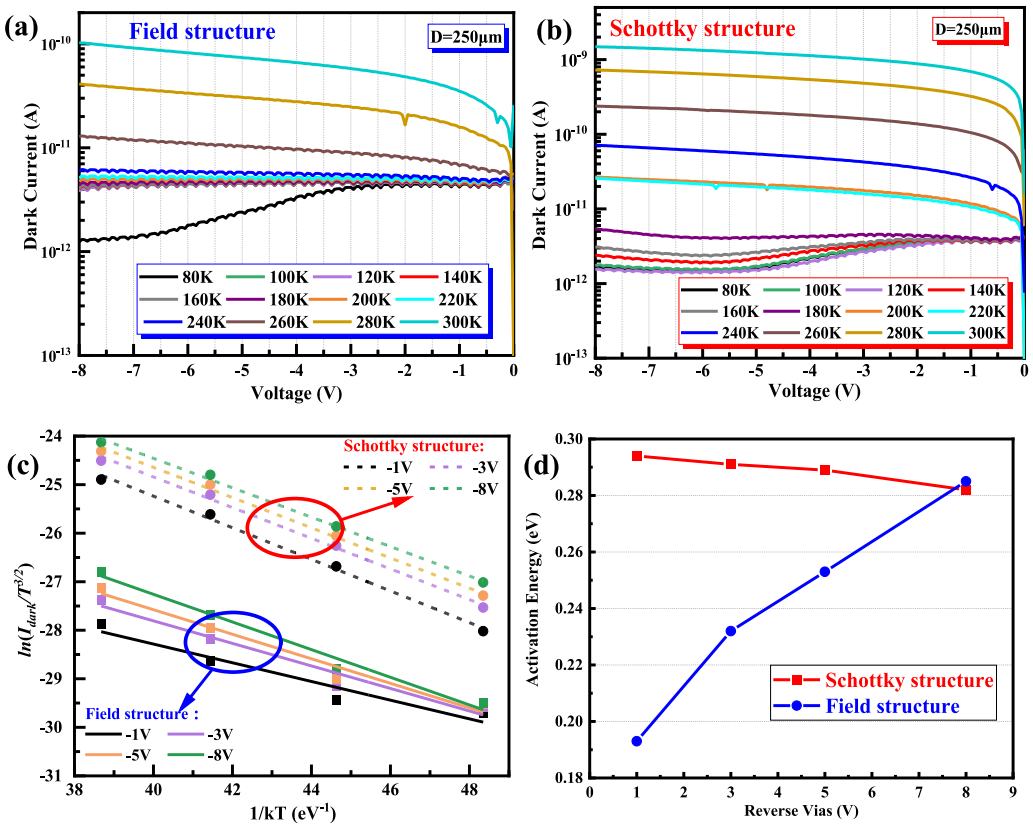

Fig. 4. Reverse *I–V* characteristics of devices with (a) field and (b) Schottky structures and a diameter of 250 μm at different temperatures. (c) The natural logarithm of ($I_{Dark}/T^{3/2}$) as a function of (1/kT), where the slope corresponds to the activation energy. (d) Activation energy as a function of the reverse bias voltage.

3.2. Origins of leakage current

The main causes of leakage current in SJPDs include the thermionic emission (TE) current over the potential barrier, the generation recombination current, and tunneling (primely the inter-band or trap-assisted tunneling) current [19,20]. Generally, the tunneling current components can be categorized into three types: (1) tunneling near the Fermi level around the interface of metal and silicon, known as field emission (FE) current, (2) tunneling at an energy between TE and FE around the interface, i.e., thermionic-field emission (TFE) current and (3) tunneling in the silicon depletion region. Generally, the origin of leakage current in SJPDs can be ascertained by measurement and analysis of ideality factor and activation energy (E_a) [21,22].

The forward dark *I–V* characteristics of SJPDs with field and Schottky structures and a diameter of 250 μm were characterized using a cryogenic probe station and Keithley 6517B electrometer at different operating temperatures (80–300K), as shown in Fig. 3(a) and (b). The measurement current below 10^{-11} A shows slight fluctuations because of the minimum perturbation error of the probe station. The ideality factor (n) was determined using the formula $n = \frac{q}{k_0 T}\frac{dV}{d(\ln I)}$ under forward bias [23],where q represents the elementary charge (1.602×10^{-19}C) and k_0 is the Boltzmann constant (1.381×10^{-23}J/K). The natural logarithm of dark current as a function of bias voltage is shown in Fig. 3 (c). The ideality factors of the field and Schottky structures in the bias range of 0<V < 0.3 V were 1.156 and 2.184, respectively. This means that at low bias voltage, the recombination current around the ITO/Si interface dominates in the Schottky structure, whereas the diffusion current outside the depletion region dominates in the field structure [24]. In the bias voltage range of 0.4<V < 1 V, the ideality factors of the field and Schottky structures increased to 5.061 and 5.147, respectively. The high value of n was attributed to several effects such as interface states, tunneling currents in regions with high dislocation density [25–27], image force lowering of the Schottky barrier in the high electric field at the metal–semiconductor interface, and generation currents within the space–charge region [28]. Because of the high-quality Si crystal and high electric field near the ITO/Si interface, it can be speculated that there are various interface and defect states present in this region [29]. Then, the measurement results of the ideal factors (n) in 0.4<V < 1V at different temperatures were marked by point in Fig. 3(d), and the temperature dependence of n could be indicated by the data points. Based on the TAT model, the ideality factor could be expressed as [30]:

$$n = E_{00} / kT \coth(E_{00} / kT) \quad (2)$$

where k is the Boltzmann constant, T is the temperature, and E_{00} is the characteristic tunneling energy that is related to the tunneling probability. The fitting of the ideality factors with temperature by the TAT model is shown in Fig. 3(d). The theoretical curve perfectly matched the measured values. E_{00} of the SJPDs with field and Schottky structures were 0.095 and 0.102eV, respectively. This indicates that the main contributor to the leakage current of the SJPDs is the TAT current around the ITO/Si interface, and the probability of TAT is higher in the Schottky structure than in the field structure.

3.3. Activation energy

To obtain further insight into the leakage mechanism in the devices, their reverse dark *I–V* characteristics were measured, as shown in Fig. 4 (a) and (b). The conventional Richardson diagram is appropriate for describing the thermal emission mechanism in ideal Schottky junctions. However, the field structure in this study exhibits nonlinearity due to localized strong electric fields and high-density shallow energy traps,

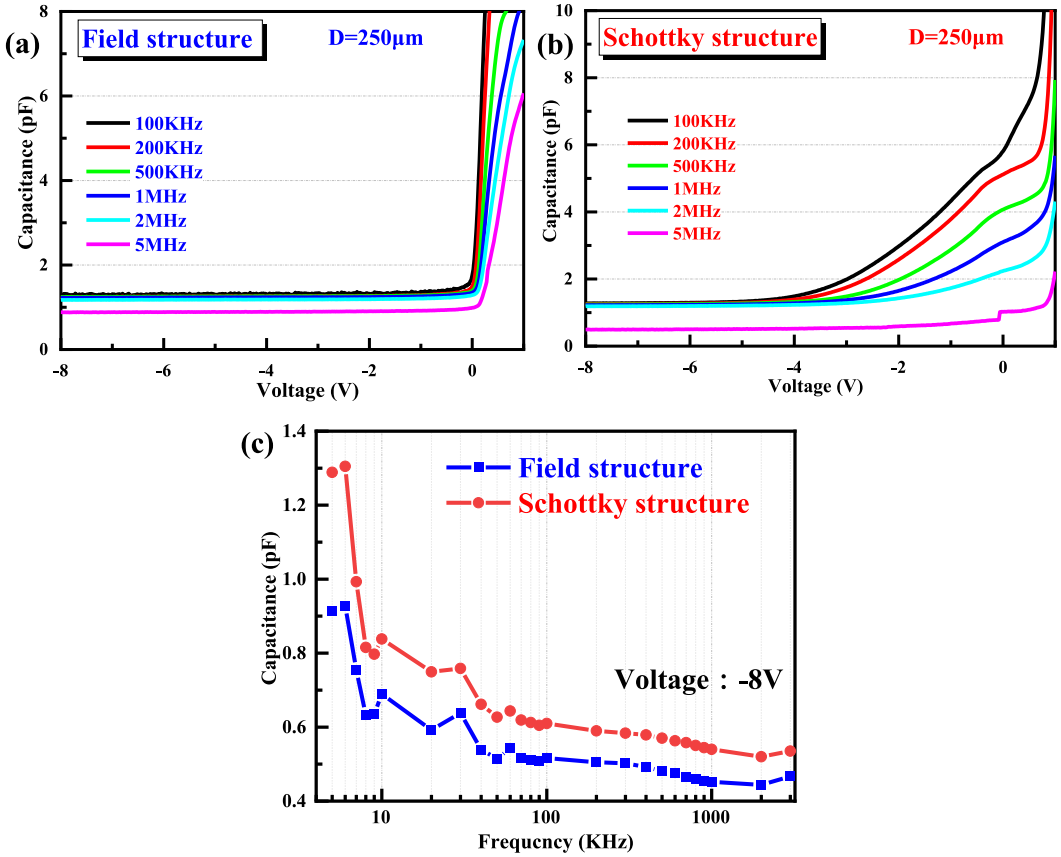

Fig. 5. *C–V* characteristics of SJPDs with (a) field and (b) Schottky structures at frequencies from 100 KHz to 5 MHz. (c) Capacitance of SJPDs as a function of frequency at −8 V.

which results in the forward current being influenced by both tunneling and recombination processes. Consequently, the activation energy derived from the reverse bias curve more accurately represents the dominant influence of interface traps on leakage current, aligning with the TAT model and energy band analysis. An analysis of the activation energy of the dark current of the devices was performed. In this analysis, I_{Dark} can be modeled using the following functional form [31]:

$$I_{\mathrm{Dark}} = BT^{3/2} e^{-E_a/kT}\left(e^{qV_a/2kT} - 1\right) \tag{3}$$

where T is the temperature, V_a is the external bias voltage, and E_a is the activation energy that causes device leakage current. The natural logarithm of $(I_{Dark}/T^{3/2})$ as a function of 1/kT at various reverse bias voltages is shown in Fig. 4(c). The slope of the linear fitting of this plot yields the activation energy. As shown in Fig. 4(d), E_a of the field and Schottky devices was 0.193 and 0.294 eV, respectively, at −1 V, and 0.285 and 0.282 eV, respectively, at −8 V, which are less than half of the band gap of Si (~0.56 eV). Therefore, the main origin of the leakage current is TAT and E_a represents the minimum energy required for the TAT process [32,33]. Fig. 4(d) shows E_a of the two types of devices as a function of the external reverse bias voltage. E_a of the SJPDs with a Schottky structure changed slightly with the bias voltage. This observation could be explained by the pinning of the surface Fermi level, which results from the high peak density of surface states or defects near the ITO/Si interface.

3.4. Measurement of interface traps

Capacitance measurements can be used to evaluate interface trap density because information about interface traps is contained in the input capacitance of the equivalent circuit. Fig. 5(a) and (b) show capacitance–voltage (*C–V*) characteristics of the devices with field and Schottky structures, respectively, and a diameter of 250 μm at frequencies from 100 KHz to 5 MHz, which was measured with sweeping-voltage mode of the Keithley 4200 semiconductor analyzer. There is obvious stretching of the curves in the voltage direction. Because of the interface traps, it takes more charge or applied voltage to reach the same

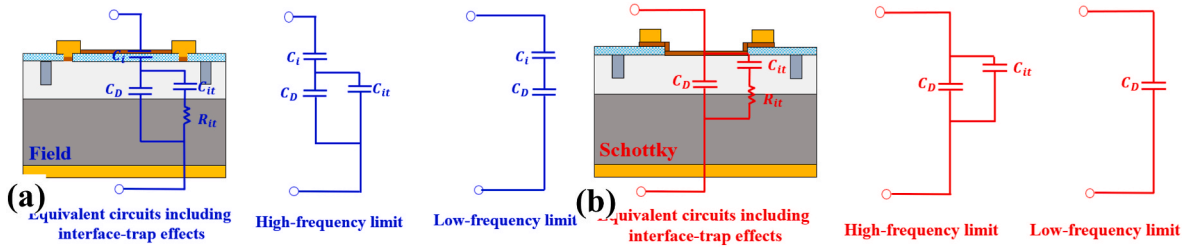

Fig. 6. Equivalent circuits including interface trap effects and corresponding high- and low-frequency equivalent circuits for SJPDS with (a) field and (b) Schottky structures.

surface potential (or band bending) as in the theoretical case without traps. When the voltage is over -5V, the capacitance no longer changes with the bias voltage, indicating a fully depleted in the 20 μm epitaxial silicon layer and same junction capacitance for both field and Schottky devices. Therefore, the relationships between capacitance and frequency were measured at -8V with the sweeping-frequency mode of the analyzer, as shown in Fig. 5(c). The capacitance of the Schottky structure is higher than that of the field structure up to 9 MHz. At high frequency, the interface traps are not fast enough to respond to the rapid signal, which results in the two types of structures showing similar capacitance [34,35].

The high–low frequency capacitance (HLFC) method was used to calculate the interface-trap density distribution D_{it} (number of traps/(cm^2•eV)) of the SJPDs [24]. The equivalent circuits at the low- and high-frequency limits of the two types of structures are shown in Fig. 6 (a). In this figure, C_{it} is the capacitance associated with interface traps and C_D is the semiconductor depletion-layer capacitance. According to the capacitance expression of the equivalent circuit model in the low-frequency and high-frequency limits and the relationship $D_{it} = C_{it}/q$, the trap density can be calculated as follows:

$$\text{Schottky structure}: D_{it} = (C_{LF} - C_{HF}) / q, \tag{4}$$

$$\text{field structure}: D_{it} = \left[(1/C_{LF} - 1/C_i)^{-1} - (1/C_{HF} - 1/C_i)^{-1} \right] \Big/ q. \tag{5}$$

As shown in Fig. 5(c), below 6 KHz and above 2 MHz, the capacitance tends to be stable with frequency, inferring that the contribution of the interface trap to the capacitance tends to be saturated in this frequency range [36]. Meanwhile, referring to previous publics about HLFC mode [37,38], the capacitance of the devices at high frequency (3 MHz) and low frequency (5 KHz) was extracted. C_{it} and D_{it} of devices with Schottky and field structures and a diameter of 250 μm were calculated using Equations (4) and (5), respectively. D_{it} of the devices with field and Schottky structures was 1.37×10^{10} and 3.96×10^{11}/(cm^2•eV), respectively.

4. Conclusion

ITO/Si SJPDs with different electrode structures were fabricated and their leakage current generation mechanism was analyzed based on *I–V* characteristics measured at 80–300 K. The ideality factor fitting results extracted from the forward *I–V* curves showed that the TAT current is the dominant component of I_{Dark} in the two device structures. As the reverse bias voltage increases, the band bending increases, and the hole tunneling of the deep energy-level defect state in the middle of the band gap is enhanced. The interface trap density of the field and Schottky structures was calculated to be 1.37×10^{10} and 3.96×10^{11}/(cm^2•eV), respectively, based on capacitance measurements. Thus, the field structure can suppress I_{Dark} caused by interfacial defects. Optimizing the fabrication process and interfaces of Si SJPDs can improve their electrical properties.

CRediT authorship contribution statement

Yaming Li: Funding acquisition, Formal analysis, Data curation. **Dianbo Liu:** Writing – original draft, Visualization, Validation. **Ruixi Liu:** Methodology, Investigation. **Yunxiao Cui:** Validation. **Yunfei Liu:** Project administration. **Ziyi Ma:** Formal analysis. **Yuewen Liu:** Formal analysis. **Jiaxuan Wang:** Resources. **Ziqian Li:** Project administration. **Yusen Dong:** Visualization. **Jiaxin Li:** Formal analysis. **Chenxi Du:** Investigation. **Guihua Liao:** Methodology. **Chong Li:** Writing – review & editing, Supervision, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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