Temperature-dependent capacitance–voltage and current–voltage characteristics of Pt/Ga_2O_3 (001) Schottky barrier diodes fabricated on n^-–Ga_2O_3 drift layers grown by halide vapor phase epitaxy

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We investigated the temperature-dependent electrical properties of Pt/Ga_2O_3 Schottky barrier diodes (SBDs) fabricated on n^--Ga_2O_3 drift layers grown on single-crystal n^+-Ga_2O_3 (001) substrates by halide vapor phase epitaxy. In an operating temperature range from 21 °C to 200 °C, the Pt/Ga_2O_3 (001) Schottky contact exhibited a zero-bias barrier height of 1.09–1.15 eV with a constant near-unity ideality factor. The current–voltage characteristics of the SBDs were well-modeled by thermionic emission in the forward regime and thermionic field emission in the reverse regime over the entire temperature range. © *2016 AIP Publishing LLC*.
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Technologies for high-power and high-voltage electronics based on wide bandgap semiconductors such as SiC and GaN have attracted much interest and development effort in light of the superior Baliga's figures of merit of these materials to that of Si by several hundred times.[1] As a result, SiC and GaN transistors and diodes have already been commercialized with increasing market share in certain applications. Driven by these social circumstances, we have recently proposed another wide bandgap semiconductor —gallium oxide (Ga_2O_3)— as a candidate for power electronics. Due to an extremely large bandgap of 4.5–4.9 eV,[2–5] Ga_2O_3 is expected to sustain a breakdown electric field about three times higher and hence present a Baliga's figure of merit substantially larger than those of SiC and GaN. Moreover, large-size and high-quality native Ga_2O_3 wafers manufactured from melt-grown Ga_2O_3 bulk single crystals will enable low-cost mass production of Ga_2O_3 power devices in the future. These two merits of Ga_2O_3 will accelerate the development of Ga_2O_3 transistors and diodes to bridge the present gap in technology maturity between Ga_2O_3 and Si as well as other mainstream wide bandgap materials.

The first demonstration of single-crystal Ga_2O_3 transistors was marked by our successful fabrication of Ga_2O_3 metal-semiconductor field-effect transistors.[6] Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) with good characteristics were achieved soon after, with devices showing an off-state breakdown voltage (V_{br}) of over 400 V and an on/off drain current ratio of ten orders of magnitude.[7,8] Fairly recently, field-plated Ga_2O_3 MOSFETs with an enhanced V_{br} of 750 V were also demonstrated.[9] While lateral FETs have made tremendous and rapid progress, the research and development of vertical Ga_2O_3 power devices have been hampered by the lack of an epitaxial growth technology suitable for thick Ga_2O_3 layers with a low electron density typical of drift layer designs of about $1 \times 10^{16}\,cm^{-3}$ or less.[10–12]

Recently, halide vapor phase epitaxy (HVPE), which is an epitaxial growth technique proven valuable to many other compound semiconductors, provided a viable pathway for the epitaxy of Ga_2O_3 drift layers.[13,14] Vertical Ga_2O_3 Schottky barrier diodes (SBDs) incorporating an HVPE-grown drift layer with a net donor concentration (N_d–N_a) of $1.4 \times 10^{16}\,cm^{-3}$ exhibited good device characteristics such as a specific on-resistance of $3.0\,m\Omega\,cm^2$ and a high reverse V_{br} of around −500 V at room temperature (RT).[15] In this letter, we report on the temperature-dependent device characteristics of Pt/Ga_2O_3 SBDs with n^--Ga_2O_3 drift layers grown by HVPE.

Highly Sn-doped n-type β-Ga_2O_3 (001) substrates produced by the edge-defined film-fed growth method with an N_d–N_a of $2.5 \times 10^{18}\,cm^{-3}$ were used for the HVPE growth of 10-μm-thick n^--Ga_2O_3 drift layers at 1000 °C. GaCl and O_2 source gases were separately introduced into the growth zone by an N_2 carrier gas. $SiCl_4$ was simultaneously supplied during the growth as an n-type dopant gas. Note that unintentionally doped Ga_2O_3 films grown under the same conditions were highly resistive with a background N_d–N_a of less than $1 \times 10^{13}\,cm^{-3}$.[14]

Figure 1 shows a schematic cross section of the Ga_2O_3 SBD structure fabricated in this work. Although devices with N_d–N_a in the drift layer ranging from $2 \times 10^{15}\,cm^{-3}$ to $6 \times 10^{17}\,cm^{-3}$ were fabricated and characterized, this letter focuses on those with Si doping concentrations of around $1 \times 10^{16}\,cm^{-3}$. The fabrication of SBDs began with chemical

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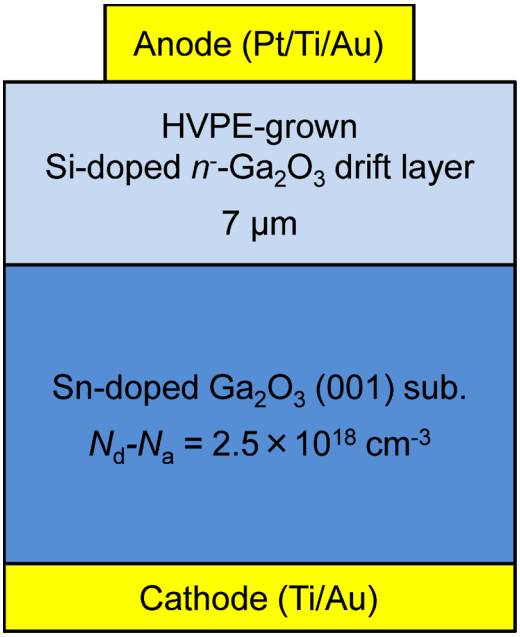

FIG. 1. Schematic cross section of Ga_2O_3 SBD structure.

mechanical polishing (CMP) of the front epitaxial surface to remove pits formed during HVPE growth. The flattened post-CMP drift layer thickness was about 7 μm. To ensure good ohmic contact formation for the cathode electrode, the back face of the substrate was also ground and polished to remove the layer damaged from wafer slicing. After solvent and acid cleaning of the samples followed by BCl_3 reactive ion etching of the polished back face, a Ti(20 nm)/Au(230 nm) ohmic metal stack was blanket evaporated to form the backside cathode electrode. Finally, circular Schottky anode electrodes with diameters of 200 μm for current density–voltage (J–V) measurements and 400 μm for capacitance–voltage (C–V) measurements were fabricated on the Ga_2O_3 drift layer by standard photolithographic patterning, evaporation of a Pt(15 nm)/Ti(5 nm)/Au(250 nm) stack, and liftoff. No dielectric passivation was applied to the surface of the epitaxial layer. On-chip electrical measurements were carried out in air by using a Keithley 4200 Parameter Analyzer and a probe station with a thermal chuck.

Before undertaking systematic temperature-dependent studies, we calibrated the effect of inadvertent thermal annealing during measurements on the properties of Ga_2O_3 SBDs. After annealing up to 200 °C, the zero-bias built-in potential ($qV_{bi,0}$) at RT as extracted from C–V data by using a method to be discussed in the following paragraphs shifted from about 1.1 eV to about 1.0 eV, and the reverse leakage current decreased significantly by five orders of magnitude. Other parameters such as ideality factor (η) and N_d–N_a depth profile remained unchanged. The physical mechanisms behind these phenomena are still under investigation. We should also point out that the $qV_{bi,0}$ of 1.0–1.1 eV for Pt/Ga_2O_3 (001) obtained in this work was 0.3–0.4 eV smaller than the value previously reported for Pt/Ga_2O_3 (010).[12] This discrepancy in $qV_{bi,0}$ could be attributed to the difference in the Ga_2O_3 surface orientation.

The performance of the Ga_2O_3 SBDs at elevated temperatures was investigated to extract fundamental diode parameters and gain insight into the properties of the Pt/Ga_2O_3 (001) Schottky contact, which was modeled by the energy band diagram in Fig. 2. Device characteristics discussed in the remainder of this paper were obtained for Ga_2O_3 SBDs having an annealing history up to 200 °C prior to the temperature-dependent measurements. First, 1-MHz C–V measurements were performed on the SBDs over a temperature range of 21–200 °C. Figure 3(a) plots the inverse square capacitance ($1/C^2$) against anode voltage (V) for a typical device at 21, 100, and 200 °C. The value of $V_{bi,0}$–kT/q at each temperature was determined by linear extrapolation of the $1/C^2$–V data to the V–axis using

$$\frac{1}{C^2} = \frac{2\left(V_{bi,0} - kT/q - V\right)}{q\epsilon_s\epsilon_0 S^2 (N_d - N_a)}, \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, ϵ_s is the relative dielectric constant of Ga_2O_3, ϵ_0 is the vacuum permittivity, and S is the area of the anode electrode. An effective Schottky barrier height at zero bias ($q\phi_{b,0}$) is given by

$$q\phi_{b,0} = qV_{bi,0} + (E_c - E_f) - q\Delta\phi_{ifbl,0}, \tag{2}$$

where E_c is the conduction band minimum of Ga_2O_3, and E_f is the Fermi level. The last term, $q\Delta\phi_{ifbl,0}$, represents the potential barrier lowering due to the image charge induced in the Schottky metal under the zero-bias condition as shown in Fig. 2 and is expressed by

$$q\Delta\phi_{ifbl,0} = \sqrt{\frac{q\mathcal{E}_0}{4\pi\epsilon_s\epsilon_0}}, \tag{3}$$

where $\mathcal{E}_0$ is the electric field at the Pt/Ga_2O_3 interface at $V = 0$ V calculated by

$$\mathcal{E}_0 = \sqrt{\frac{2q(N_d - N_a)V_{bi,0}}{\epsilon_s\epsilon_0}}. \tag{4}$$

Using the Boltzmann approximation for E_f, we calculated the value of $E_c - E_f$ by using the following equations:

$$E_c - E_f = -kT\ln\left(\frac{N_d - N_a}{N_c}\right), \tag{5}$$

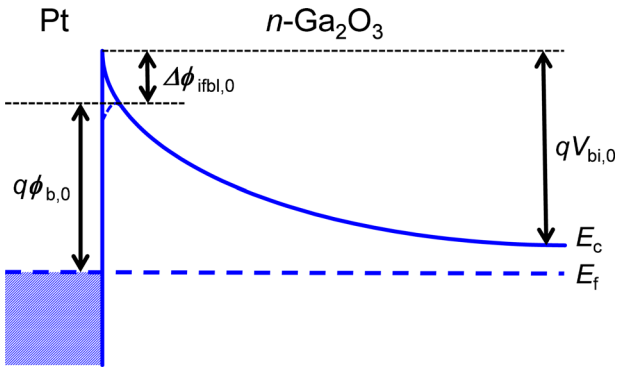

FIG. 2. Energy band diagram of Pt/n-Ga_2O_3 Schottky interface at thermal equilibrium.

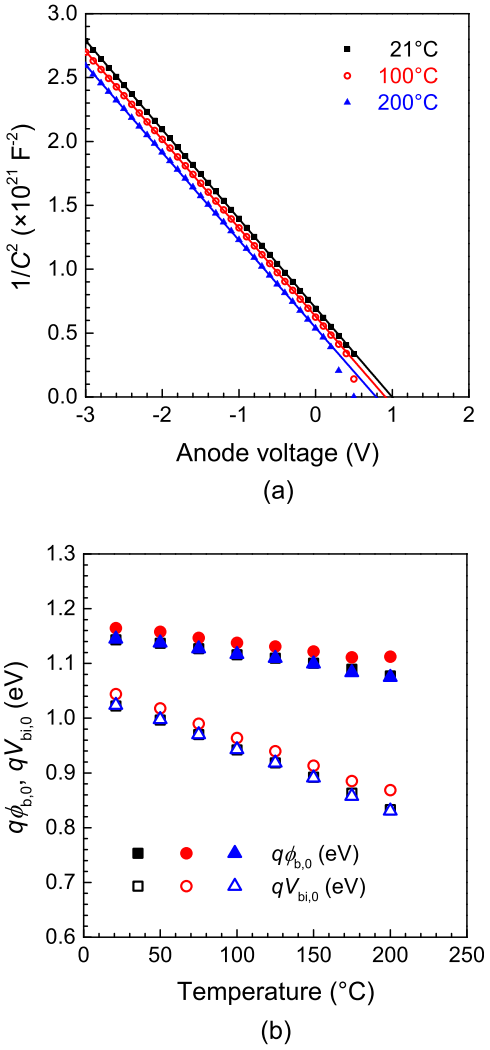

FIG. 3. (a) $1/C^2$–V characteristics at 21, 100, and 200 °C and (b) temperature dependences of $qV_{bi,0}$ and $q\phi_{b,0}$ for Ga_2O_3 SBDs.

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2}, \tag{6}$$

where N_c is the effective density of states in the conduction band of Ga_2O_3, m^* is the electron effective mass in Ga_2O_3, and h is the Planck's constant. We have experimentally determined that the activation energy of Si doped in Ga_2O_3 films is 30–50 meV for a doping concentration range of 10^{15}–10^{17} cm^{-3} by temperature-dependent Hall measurement. The Si donor level is sufficiently shallow for full dopant activation above RT; therefore, we assumed that N_d–N_a as expressed in Eq. (5) was equal to the electron density in the neutral region of Ga_2O_3. It was also confirmed from the C–V characteristics that the depth profile of N_d–N_a was constant at 1.2×10^{16} cm^{-3} regardless of the operating temperature. In the calculations of $q\phi_{b,0}$, a theoretical value of $0.34m_0$ (m_0: free electron mass) predicted by first-principles calculations and an experimental value of 10 were used for m^* and ϵ_s of Ga_2O_3, respectively.[4,16] Figure 3(b) plots the extracted $qV_{bi,0}$ and $q\phi_{b,0}$ for three different devices fabricated on the same epitaxial wafer as a function of operating temperature. The $qV_{bi,0}$ monotonically decreased from 1.03 eV to 0.84 eV with increasing temperature from 21 °C to 200 °C. On the other hand, the $q\phi_{b,0}$ slightly decreased with temperature but was almost constant at 1.12 ± 0.03 eV over the same temperature range. The experimental $q\phi_{b,0}$ value is consistent with the theoretically calculated one for Pt/Ga_2O_3 Schottky contacts.[17] The weak temperature dependence of $q\phi_{b,0}$ was justified, because $E_c - E_f$ increased with temperature due to an increase in N_c as derived from Eqs. (5) and (6), compensating the effect of decreasing $qV_{bi,0}$ on $q\phi_{b,0}$. Note that the $q\phi_{b,0}$ of an ideal n-type Schottky contact decreases with increasing temperature due to the shrinkage of the semiconductor bandgap.[18,19] However, the variation should be up to tens of meV in the measurement temperature range.

Figure 4(a) shows the forward temperature-dependent J–V (J–V–T) characteristics of an illustrative Ga_2O_3 SBD in semi-logarithmic scale. These characteristics, which were typical of the SBDs investigated in this work, evolved smoothly with increasing operating temperature from 21 °C to 200 °C. The forward J–V data were well fitted by the thermionic emission (TE) model[20,21]

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right], \tag{7}$$

and

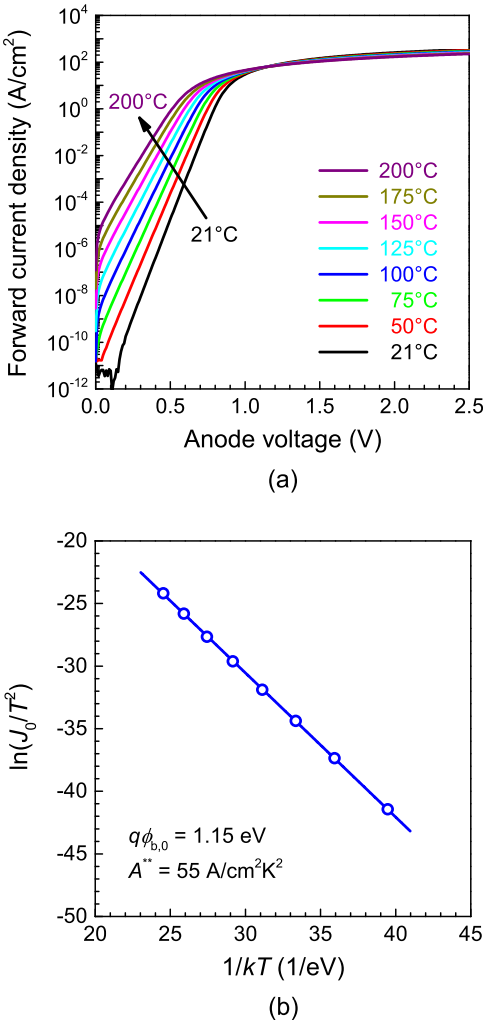

FIG. 4. (a) Forward J–V–T characteristics and (b) Richardson's plot [$\ln(J_0/T^2)$ vs $1/kT$] of Ga_2O_3 SBD in a temperature range of 21–200 °C.

$$J_0 = A^{**}T^2 \exp\left(-\frac{q\phi_{b,0}}{kT}\right), \tag{8}$$

where A^{**} is the reduced effective Richardson's constant, $q\phi_b$ is the V-dependent Schottky barrier height including the effect of image force barrier lowering, and J_0 is the saturation current density. In general, $q\phi_b$ depends linearly on V in the range of small V values, i.e., $\phi_b = \phi_{b,0} + \beta V$, where β is the positive coefficient. Thus, Eq. (7) can be written as

$$\begin{aligned} J &= A^{**}T^2 \exp\left(-\frac{q(\phi_{b,0}+\beta V)}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \\ &= J_0 \exp\left(\frac{qV}{\eta kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \end{aligned} \tag{9}$$

where $1/\eta = 1-\beta$. It should be noted that rigorous TE analysis should take into account optical phonon scattering between the top of the barrier and the Schottky metal as well as quantum mechanical reflection of electrons. As a result, the effective Richardson's constant $A^* = 4\pi q m^* k^2/h^3$ was replaced with A^{**} in Eqs. (7), (8), and (9).[20] Using Eq. (9), η values of 1.03 ± 0.01 were extracted from the slopes of linear fits to the forward J–V curves for $V > 3kT/q$ over the temperature range of 21–200 °C.

The forward J–V–T characteristics were further analyzed by the Richardson's plot. As discussed in the preceding paragraphs, the values of $q\phi_{b,0}$ and η estimated from the C–V–T and J–V–T characteristics, respectively, were almost constant with temperature. Therefore, the Richardson's plot expressed an approximate linear relationship between $\ln(J_0/T^2)$ and $1/kT$. Using Eq. (8)

$$\ln(J_0/T^2) = \ln(A^{**}) - q\phi_{b,0}/kT. \tag{10}$$

Figure 4(b) plots $\ln(J_0/T^2)$ as a function of $1/kT$ where the J_0 values for each temperature were extracted from the ordinate intercepts of linear fits to the respective J–V curves in Fig. 4(a). The $q\phi_{b,0}$ and A^{**} were determined from the slope and ordinate intercept, respectively, of a linear fit to the plotted data in Fig. 4(b) to be 1.15 eV and 55 A/cm^2 K^2. In general, spatial inhomogeneity of Schottky barrier height due to defects and traps across an anode contact results in a smaller $q\phi_{b,0}$ extracted from J–V data than from C–V data since the defects and traps act as intermediate states that assist in leakage current conduction.[22,23] However, the $q\phi_{b,0}$ value of the Ga_2O_3 SBDs extracted from the Richardson's plot was nearly equal to that determined from C–V–T characteristics, indicating negligible spatial fluctuations of $qV_{bi,0}$ and $q\phi_{b,0}$. Moreover, the extracted A^{**} values for several SBDs fabricated on the same substrate were tightly distributed between 20–55 A/cm^2 K^2, in close agreement with other experimental reports[24,25] as well as theoretical A^* values of 28–41 A/cm^2 K^2 obtained using $m^* = 0.23$–$0.34 m_0$ from first-principles calculations.[4,26,27]

Figure 5 shows the reverse J–V–T characteristics measured on the same device as for the forward J–V–T characteristics at the same temperatures between 21 and 200 °C, together with the theoretical curves calculated based on the thermionic field emission (TFE) model that took into account tunneling current across a reverse-biased Schottky junction.[20,28] While the TE model with image force barrier lowering can adequately reproduce the reverse leakage current in Si SBDs,[29] similar analyses often underestimate the leakage in wide bandgap semiconductor SBDs such as SiC, GaN, and diamond since these devices present higher thermionic barriers and stronger electric fields at the metal/semiconductor interface with resultant tunneling leakage being dominant over the TE current.[30–32] The TFE reverse leakage current density (J_{TFE}) was theoretically calculated by the following simplified equation proposed by Hatakeyama and Shinohe:[30]

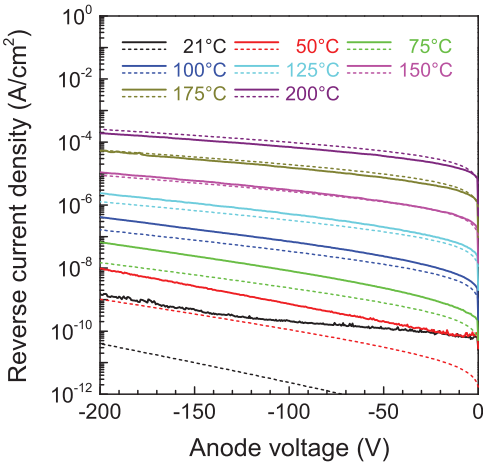

FIG. 5. Reverse J–V–T characteristics of Ga_2O_3 SBD at 21–200 °C. Solid and dotted lines correspond to experimental and calculated values, respectively.

$$\begin{aligned} J_{TFE} = &\frac{A^* T q\hbar\mathcal{E}}{k}\sqrt{\frac{\pi}{2m^* kT}} \\ &\times \exp\left[-\frac{1}{kT}\left(\phi_{b,0} + \Delta\phi_{ifbl,0} - \frac{(q\hbar\mathcal{E})^2}{24m^*(kT)^2}\right)\right], \end{aligned} \tag{11}$$

where $\hbar$ is the reduced Planck's constant ($=h/2\pi$), and $\mathcal{E}$ is the electric field at the Schottky interface expressed as

$$\mathcal{E} = \sqrt{\frac{2q(N_d - N_a)(V_{bi,0} - V)}{\epsilon_s \epsilon_0}}. \tag{12}$$

In the calculations of J_{TFE}, we used $q\phi_{b,0}$ and $qV_{bi,0}$ values averaged from the data plotted in Fig. 3(b) for each temperature, an N_d–N_a value of 1.2×10^{16} cm^{-3} extracted from C–V characteristics, and the theoretical value of A^* calculated using $m^* = 0.34 m_0$.[4] Note that the uncertainty in A^* would introduce small errors. As shown in Fig. 5, the calculated J_{TFE} were in good agreement with the experimental data especially for temperatures above 100 °C. The small discrepancies between calculation and experiment at temperatures below 100 °C could be attributed to leakage through the unpassivated Ga_2O_3 surface.[33] Thus, an additional process such as surface treatment prior to metal deposition and/or dielectric surface passivation could be important to further reduce the leakage current to the theoretical TFE limit.

In summary, Ga_2O_3 SBDs with HVPE-grown drift layers on single-crystal β-Ga_2O_3 (001) substrates were fabricated and characterized at operating temperatures of 21–200 °C. The $q\phi_{b,0}$ at a Pt/Ga_2O_3 interface were determined to be

1.15 eV at RT and 1.09 eV at 200 °C, and there was little discrepancy between *C–V–T* and *J–V–T* extractions. Forward current conduction in the SBDs was governed by TE with a near-unity η of 1.03 ± 0.01, whereas the reverse leakage current agreed well with the TFE model as would be expected of wide bandgap semiconductor SBDs. These results indicated that the Pt/Ga_2O_3 (001) interface formed a nearly ideal Schottky contact with excellent spatial homogeneity, and that Ga_2O_3 SBDs can be expected to deliver promising performance as next-generation power devices.

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