Self-assembled patches in PtSi/n-Si (111) diodes

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Abstract: Using the effect of the temperature on the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of PtSi/n-Si (111) Schottky diodes the profile of apparent doping concentration (N_{Dapp}), the potential difference between the Fermi energy level and the bottom of the conduction band (V_n), apparent barrier height (Φ_{Bapp}), series resistance (R_s) and the interface state density N_{ss} have been investigated. From the temperature dependence of (C–V) it was found that these parameters are non-uniformly changed with increasing temperature in a wide temperature range of 79–360 K. The voltage and temperature dependences of apparent carrier distribution we attributed to the existence of self-assembled patches similar the quantum wells, which formed due to the process of PtSi formation on semiconductor and the presence of hexagonal voids of Si (111).

Key words: Schottky barrier diode (SBD); temperature dependence; self-assembled patches; temperature dependence; PtSi/n-Si (111); C–V characteristics; quantum wells

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1. Introduction

Schottky diodes on the base of silicide/silicon contact most widely used both in electronic and optoelectronic applications, due to the advantageous properties of metal silicides such as thermal stability, low resistance, and reduced silicide/silicon specific contact resistance[1–3]. On the other hand, the performance and reliability of these contacts are dependent on the choice of silicides, crystal structure of contacting materials and on the quality of the contact interface[4, 5]. Due to formation of silicide film on surface of semiconductor, the interface shifted deeper into the semiconductor. In addition, the crystal lattice of Si (111) contains deformed hexagonal voids[6]. As a result, formation of silicides/silicon contact structures creates the possibility of the process of self-organization defects or quantum wells in the semiconductor.

Silicide film on silicon has received a lot of attention in the past, because the formation of self-assembled quantum wells is very specific for nanoelectronics[7–14]. However, there is practically no experimental information in the literature about quantum wells of PtSi in silicon[15–18]. With this purpose, we tried to investigate the possibility of the forming of the self-assembled quantum wells of PtSi in Si (111) and their influences on C–V characteristics.

The reason for this investigation of contact structure PtSi/n-Si (111) on the base of Schottky barrier is threefold: first, we wish to investigate the influence of formation of silicide on electrical characteristics of PtSi/n-Si (111) diode structure, because the crystal lattice of Si (111) contains deformed hexagonal voids. Besides, nearly all the islands, clusters and dislocations formed on the surface (111) of silicon[12, 19, 20]. However, the reason for the difference in the characteristics of Si (111) from the characteristics of Si (100) was not explained. Second, admittance–voltage measurement (C–V and G/ω–V) is one of the most popular non-destructive methods for getting information on Schottky rectifying interfaces[21, 22]. In addition, the method makes it possible to obtain the information on the amount of charge in quantum wells[23]. Third, the investigation of C–V and G/ω–V characteristics of small diodes, areas of about 10^{-6} cm^2, is interesting, because detailed study of the characteristics reveals the possibility of creating new multifunctional devices[3, 4, 24].

The values of C and G depend on various parameters, such as density of interface states (N_{ss}), series resistance (R_s), doping concentration (N_D), formation of barrier height (BH) and device fabrication technology. Therefore, due to the influence of the temperature on characteristics, can be revealed the profile of doping concentration, the dependences of potential barrier height and series resistance on it[25].

2. Materials and methods

For the fabrication of PtSi/n-Si (111) structures the method of planar technology and standard photolithography was used, traditionally used for the fabricating of the diodes with small geometrical sizes. Silicide film was deposited by the magnetron-sputtering method on single crystal n-type silicon (P-doped) wafer Si (111), with 3 inch diameter, 0, 7 Ω·cm resistivity and 3, 5 μm thickness[26]. The condition of deposition process of Pt film with the thickness about 0, 6 μm is: the vacuum about 10^{-4} Torr, as working gas was used Argon plasma, the temperature of preliminary heating of the substrate plates in chamber was 523 K during 250 s.

At first, the silicon n-Si (111) wafer was cleaned in a mix of a peroxide-ammoniac solution for 10 min using two stages of chemical process and subsequently quenched in de-

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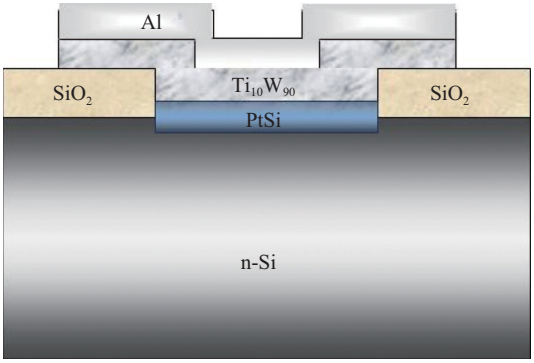

Fig. 1. (Color online) Cross section of PtSi/n-Si (111) with diffusion barrier.

ionized water with resistivity of 18 MΩ·cm. Then, for fabrication of a homogeneous PtSi film the wafers (Pt/n-Si) were annealed at 6×10^{-5} Torr at 773 K for 10 min and annealed outside of the chamber in a special ampoule with the furnace at 783 K for 30 min in atmosphere of the gases N_2 and H_2. All processes were carried out in a room with 100 percent cleanness.

It is known that Al has a great diffusion ability and is traditionally used as ohmic contact. In this case, to prevent the disadvantage of Al diffusion to PtSi, the amorphous TiW alloy was deposited (Fig. 1) between Al and PtSi as diffusion barrier[27–29].

The *C–V* and *G/ω–V* measurements of PtSi/n-Si (111) structure were performed in the temperature range from 79 to 360 K by using a HP 4192A LF impedance analyzer. Small sinusoidal test signal of 20 mV_{p-p} (500 kHz) from the external pulse generator is applied to the sample in order to meet the requirement. The temperature dependence measurements were performed in a Janes VPF-475 cryostat with a Lake Shore model 321 auto-tuning temperature controllers in a vacuum of 5×10^{-5} Torr. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card. In this paper are presented the results measurements of diode with the area of 8×10^{-5} cm^2.

It is known, that at high frequency ($f > 1$ MHz), the surface states cannot follow the AC signal and consequently do not contribute appreciably to the PtSi/n-Si structure capacitance, because the carrier lifetime τ is much larger than $1/(2\pi f)$. In our investigations the frequency of 500 kHz was used as the frequency of small AC signal (20 mV_{p-p}). In such case, it is possible a detection of a small contribution from surface states[3, 4, 24, 26].

3. Results and discussion

Figs. 2 and 3 show a set of capacitance–voltage (*C–V*) and conductance–voltage (*G/ω–V*) characteristics of PtSi/n-Si (111) Schottky barrier diodes (SBDs) which were measured in the temperature region 79–360 K at 500 kHz with a small AC signal of 20 mV peak to peak amplitude from −2 to 2 V. As can be seen from these figures, the values of the capacitance and conductance exhibit a saturation or broad peak in the forward bias region. However, dependences of *C–V* and *G/ω–V* characteristics of PtSi/n-Si diodes on temperature are

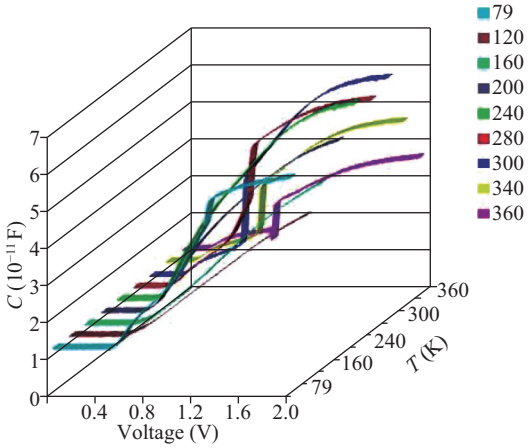

Fig. 2. (Color online) The *C–V* characteristics of PtSi/n-Si diode as a function of temperature.

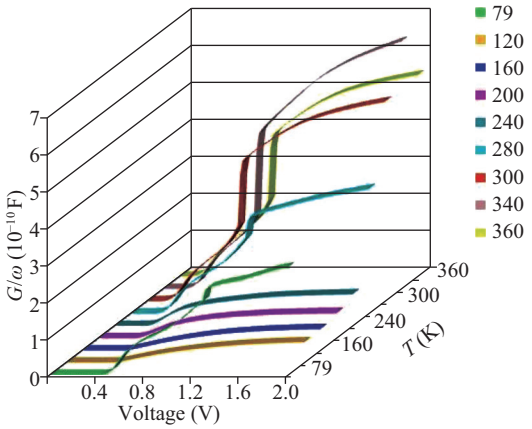

Fig. 3. (Color online) The *G/ω–V* characteristics of PtSi/n-Si diode as a function of temperature.

different for different regions of voltage. In the region 0–0.2 V capacitance and conductance are independent of the voltage at all temperatures. This indicates the existence of fixed negative charge at the interface[3, 4, 24].

Sharp jump of *C* was observed for temperature range from 280 to 360 K at the different voltage values of 0.92–0.74 V, respectively. At low temperatures (below 280 K), the capacitance value is weakly dependent on the temperature. This behavior can be explained by the fact that below 280 K the interface states do not contribute to the capacitance, practically.

In addition, at the temperature 360 K and forward bias 0.72–0.78 V is observed the effect of the negative differential capacitance caused by the distortion of the equilibrium distribution function of the charges in the semiconductor layer of the quasi-neutral region on the border with the depletion layer due to the intense emission of hot electrons in the semiconductor at a forward bias. On the other hand, this behavior of negative capacitance has been ascribed to the loss of interface charges of the occupied states below Fermi level due to impact ionization processes[4, 24]. The position of jump of increasing of capacitance shifts to small voltage with increase of temperature, which is caused by the changes of charges of the interface. Moreover, this result revealed that temperature lowering and test frequency increase lead to the similar changes of

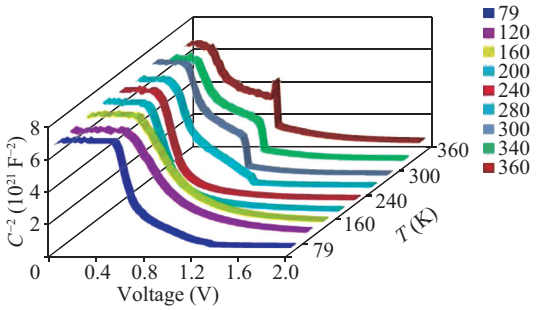

Fig. 4. (Color online) The C^{-2}–V characteristics of PtSi/n-Si diode as a function of temperature.

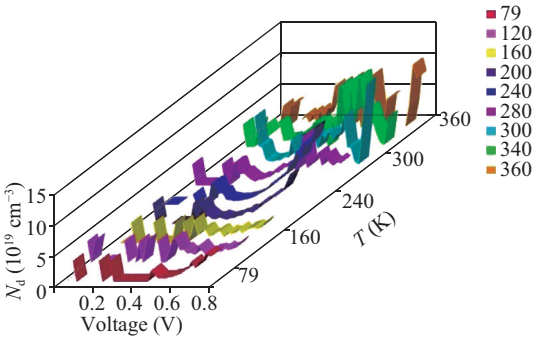

Fig. 5. (Color online) The profile of apparent charge distribution of PtSi/n-Si Schottky diode at different temperatures.

capacitance. Fig. 2 shows the experimental measured conductance (G/ω) of PtSi/n-Si. The maximum of characteristics shifts due to inductance process.

Formed potential distribution in the depletion layer and its dependence on the voltage determine the features of the electronic processes and $C-V$ characteristics[4, 24]. Nonuniform changing of C^{-2}–V characteristics may not accurately determine the doping concentration, although, the primary doping concentration of n-Si (111) substrate is 6.12×10^{15} cm^{-3} (Fig. 4). In reality, we can fit two or three linear parts of characteristics as in our previous paper[30].

In the present paper, taking into account that the slope of experimental C^{-2}–V characteristic of PtSi/n-Si (111) diodes is changed, the values of apparent doping concentration N_{Dapp} have been determined from the slope of the plot with the help of Eq. (1)[4].

$$\frac{d\left(1/C^2\right)}{dV} = \frac{2}{\varepsilon_s \varepsilon_0 q N_{Dapp} A^2}, \tag{1}$$

where ε_s is the permittivity of the semiconductor (11.8 for Si), ε_0 is the permittivity of free space charge ($\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, N_{Dapp} is the apparent doping concentration of n-type semiconductor Si, and A is the Schottky contact area.

As is shown from Fig. 5, in all temperature regions the apparent doping concentration of real contact locally differs from primary doping concentration of n-Si (111) ($N_{Dapp} > N_D$) and it has a value of about 10^{18}–10^{19} cm^{-3}. This result indicated that semiconductor is locally degenerated[3, 4, 24], and the revealing of apparent charge concentration increased with the increasing of temperature. The obtained results are in a good agreement with the result of investigation of the capacitance–voltage characteristics of tunneling diodes prepared by erbium and oxygen ion co-implantation into single crystal Si (111)[31].The similar results have been obtained by the investigations of heterostructures with quantum well while the temperature has been changed from 77 to 300 K[23]. The displacement of the peaks with increasing voltage is due to a change in the width of the space charge region and a change in capacitance, respectively. The change in the height of the peaks indicates an increase in the contribution to the capacitance of deep levels with increasing temperature.

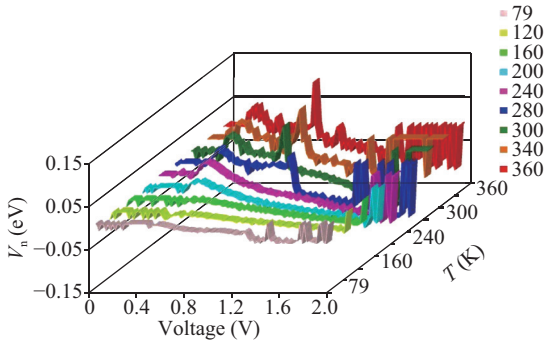

Fig. 6. (Color online) The distribution of the potential difference (V_n) between the Fermi energy level E_F and the bottom of the conduction band of PtSi/n-Si diodes.

It is known that nonlinear dependence of C^{-2}–V on voltage is caused by ionization of deep and shallow levels[23, 32]. A sharp jump of characteristics revealed that the diffusion potential V_0 for the temperature 300, 340 and 360 K is about 0.8 V[32]. As is shown by Buzaneva[24] similar C^{-2}–V characteristics are observed when the contact is metal-p^+-n-semiconductor with deep centers in the semiconductor.

The value of the barrier height Φ_{B0} has been calculated by the following equation using the C–V measurements[3, 4]:

$$\Phi_B = q(V_0 + V_n), \tag{2}$$

where V_n is the potential difference between the Fermi energy level E_F and the bottom of the conduction band in the neutral region of n-Si.

The values of V_n can be obtained as

$$V_n = \frac{kT}{q} \ln\left(\frac{N_c}{N_D}\right), \tag{3}$$

with

$$N_c = 4.82 \times 10^{15} T^{3/2} \left(\frac{m_e^*}{m_0}\right)^{3/2}, \tag{4}$$

where N_c is the effective density of states in nondegenerated Si conductance band, $m_e^*/m_0 = 1.09$ is the effective mass of the density of states of silicon (Fig. 6). Diffusion potential V_0 for different temperatures has been determined from the intersection of the linear part of C^{-2}–V characteristics with V axis.

As is shown from Figs. 5 and 6 some regions of the semiconductor in the contact zone are degenerated and deep and shallow centers have a different contribution to the capacitance. On the basis of calculations it was obtained that difference between the Fermi energy level E_F and the bottom of the

Table 1. The parameters for PtSi/n-Si (111) SBD at temperature from 79 to 360 K.

N	T (K)	$E_F - E_c$ ($5kT/q$ eV)	$E_c - E_F = V_{n\,max}$ (10^{-2} eV)	$\Phi_{B\,app}$ (eV)	$R_{s\,max}$ (Ω)
1	79	0.039	−0.016	0.65	8.04
2	120	0.05	−0.017	0.91	7.28
3	160	0.064	−0.015	0.91	7.34
4	200	0.086	−0.014	0.52	7.4
5	240	0.1	−0.029	0.68	7.48
6	280	0.12	−0.033	0.53	7.9
7	300	0.129	0.056	0.53	8.19
8	340	0.148	0.066	0.55	6.3
9	360	0.155	0.101	0.84	7.98

conduction band (V_n) has negative or positive values (Table 1). Due to the fact, that some regions of the semiconductor are degenerated, the conduction band crosses the Fermi level at the increases of bias. The bottom of the conduction band is located below or above the Fermi level for PtSi/n-Si diodes.

On the basis of obtained results, apparent potential barrier height Φ_{B0} has been calculated with the help of Eq. (2) and tabulated (Table 1). Apparent potential barrier height also changes (nonuniform) with increase of temperature, a trend that disagrees with the negative temperature coefficient for the semiconductor material. In reality, the barrier height decreases with increase of temperature, because expansion of the lattice leads to a change in the work function and other parameters, that determine the height of the barrier[4]. On the other hand, potential barrier height of PtSi/nSi is about 0.81–0.85 eV[2, 5, 16–18]. In the result of our investigations, obtained values can be taken as the apparent values of the barrier height ($\Phi_{B0\,app}$) of PtSi/n-Si (111) diodes. As is shown, the apparent potential barrier height differs from known barrier height of PtSi/n-Si contact. A similar result is observed in Ref. [30]. The apparent height of the barrier depends on potential difference of contact between the metal and the semiconductor, the surface states charge at the metal-semiconductor interface and physical parameters of semiconductor in the depletion layer, which in turn depend on the process and conditions of formation of the barrier.

Changing the distribution profile of the charge leads to a change in the potential in the depletion layer and the apparent height of the barrier. It is known that condition of full degeneration is $5kT/q$[4]. From the calculation it was found that for PtSi/nSi diodes $V_n < 5kT/q$. Accordingly, a weak degeneration of n-Si (Table 1) is observed in the temperature range from 79 to 280 K. It is understood that Fermi level is above the conductance band. Accordingly, in the temperature range from 300 to 360 K Fermi level is below the bottom of the conductance band. It is also known that when the difference between the Fermi energy level E_F and the bottom of the conduction band E_c reaches values greater than kT/q, the semiconductor is non-degenerated. For the PtSi/nSi structure at 300, 340, and 360 K, V_n equas to 0.056, 0.066, and 0.101 eV, whereas kT/q take values of 0.025, 0.029 and 0.03 eV, respectively. This result shows that at the temperature 300–360 K semiconductors are nondegenerated.

The value of series resistance R_s and its dependence on temperature have been calculated by the method of Nicollian and Brews[34] from the measured capacitance C_m and conductance G_m in strong accumulation region. Then, the admittance is given by

$$Y_{ma} = G_{ma} + j\omega C_{ma}, \tag{5}$$

and then

$$R_s = G_{ma}\left(G_{ma}^2 + (\omega C_{ma})^2\right)^{-1}. \tag{6}$$

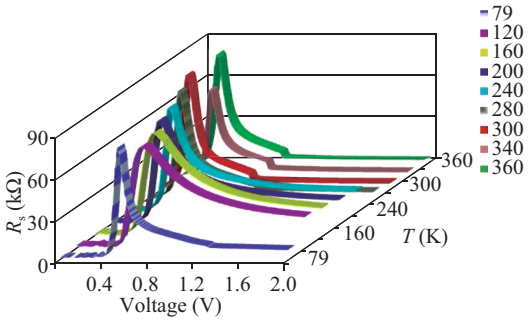

Fig. 7. (Color online) The variation of the R_s–V plots of PtSi/n-Si structures obtained at 500 kHz under various temperature levels.

In this study, using Eq. (6), R_s of PtSi/n-Si structures was calculated as a function of bias at various temperature levels as shown in Fig. 7. As seen in Fig. 7, the series resistance gives a peak between about 0–0.5 V, the value of which weakly depended on temperature. However, the position of peaks shifts towards low voltages with increasing of temperature. This behavior implies that the trap charges have enough energy to escape from the traps located in the Si band gap. It is also evident from Fig. 6, that the R_s is independent of voltage and temperature at sufficiently high voltages 0.6–2 V. It is known that the series resistance R_s is dependent on recharging of deep levels.

In our previous papers we interpreted the abnormal I–V and C–V characteristics on the basis of additional sources of the carriers. The received results have been explained by assuming small patches in the Schottky area with different potential barrier height[35, 36]. The results of investigation show that the formation mechanism of the Schottky barrier is locally nonuniform and this result very well correlated with the general theory of Tung[37].

The distribution of interface states distribution profile dependent of PtSi-n-Si (111) SBD on the temperature was obtained for capacitance from 79 to 360 K similar to the low-high frequency capacitance method, as shown in the following[34, 35]:

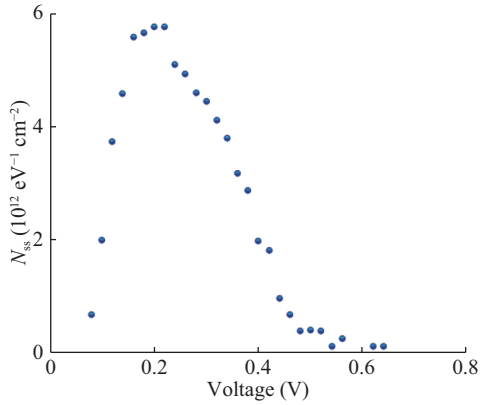

Fig. 8. (Color online) The energy distribution profile of the N_{ss} obtained from high-low temperature technique for PtSi/n-Si structure.

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{HT}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{LT}} - \frac{1}{C_{ox}}\right)^{-1}\right], \quad (7)$$

where C_{HT} and C_{LT} are the measurement C at high and low temperature, respectively. In this method, the N_{ss} is extracted from its capacitance contribution to the measured experimental C–V curve. In the generalized model of the metal–semiconductor contact a thin dielectric interface layer is taken into account[27]. In this case, C_{ox} is oxide capacitance, which in series with the parallel combination of the interface trap or surface state capacitance (C_{it}) and the space charge capacitance (C_{sc}). The density distribution of N_{ss} profile as function of the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given in Fig. 8. The energy of the interface states E_{ss}, according to Ref. [4], obtained as

$$E_c - E_{ss} = q(\Phi_{av} - V), \quad (8)$$

where Φ_{av} is average value of apparent barrier height.

As shown in Fig. 8, the values of N_{ss} give a wide peak when $E_c - E_{ss} = 0.22$ eV. The values of N_{ss} are of order about 10^{12} eV^{-1}·cm^{-2}. It is known that at sufficiently high frequencies, the surface states do not contribute to the capacitance as the charge at the surface states cannot follow the AC signal. At low frequencies, the contribution of surface states to diode capacitance decreases towards high frequencies. In the present paper the result of increase of temperature is similar to that at decrease of frequency[6]. The small value of N_{ss} caused with of a small contribution from interface states at frequency 500 kHz.

As was shown above, due to the formation of silicide film the metal/semiconductor interface displaced deep into the semiconductor. As a result, the pressure leads to the displacement of atoms from the equilibrium positions. This results in the lattice deformation of contacting materials and in a change in the band structure of materials[38]. Besides, it is known from a lot of investigation, where was noted, that characteristics of contact structures on the basis of Si (111) differs from characteristics of structures on Si (100)[31, 39, 40].

In addition, the crystal lattice of Si (111) contains deformed hexagonal voids, areas of which are about 14.6 × 10^{-2} nm^2[6]. On the other hand, the formation of a film on the surface of the semiconductor depends on the ratio of crystallographic parameters of the contacting materials[4, 5]. Silicide of Pt (PtSi) is the chemical phase and it may have a different structure and a thickness due to the condition of the experiment, and thereby affects the height of the potential barrier[38]. Moreover, the ratio of parameters of the contacting materials plays an important role in the formation of a film on the surface of the semiconductor. Traditionally, this fact has been used to create quantum wells structures for example on the basis of Ge–Si. It is known that if the mismatch is greater than 4% at the initial stage of growth of the epitaxial film so films are formed as three-dimensional islands[38]. The mismatch of the lattice parameters of PtSi and Si is about 9%. The radius of Pt atom is 1.39 Å, radius of the Si atom is 1.17 Å, whereas the radius of the voids, assuming that it is a circular, is approximately 2.15 Å[6]. In this case, these voids can be irregularly filled with atoms of platinum. Accordingly, there are formed patches with a high degree of doping, which contribute to local narrowing of the space charge region of PtSi/n-Si diodes. Heavily doped silicon patches lead to a change in the spatial position of the quasi-Fermi[37].

On the basis of these results, we can conclude that in the semiconductor Si (111), as a result of technology formation of platinum silicide, one can produce self-assembled local patches with a high doping concentration. In this case, the interface of these patches in the space charge region represent the transition n–n$^+$, the resistance of which is essential to identify and predicting the further range of applicability of the instrument. In this way, in the space charge region of PtSi/n-Si (111) SBDs there are patches with high doping concentration (10^{18}, 10^{19} cm^{-3}), whereas initially doping degree of Si (111) was about ~10^{15} cm^{-3}. In this case, the reduced resistance of n$^+$–n boundary is interesting[41]

$$R_{n-n+} = \frac{L_D N_C}{q\mu_n K n n^+}, \quad (9)$$

where L_D is Debye length in n region, N_c is the effective density of states in nondegenerated Si conductance band, μ_n is the mobility of electrons in the n-region, and n, n^+ is electron concentration in n and n$^+$-regions, K is coefficient indicating amount of the electron concentration n$^+$-region exceeds n, q-electron charge.

In this case, taking L_D as the width of the space charge region (3.8 × 10^{-5} cm), N_C = 2.85 × 10^{19} cm^{-3}, μ_n = 1.4 × 10^3 cm^{2}V^{-1}s^{-1}, n and n^+ as 6.12 × 10^{15} and 2 × 10^{18} or 2 × 10^{19} cm^{-3}. Have been obtained, the values of resistance of the interface n–n$^+$ (patches in space charge Φ region) are R_{n-n+} = 9.87 × 10^{-7} Ω·cm^2 and R_{n-n+} = 9.87 × 10^{-8} Ω·cm^2, respectively. The results for PtSi/n-Si diodes well correlate with values of the reduced resistance for n$^+$–n jump resistive transition with tunnel jump[41].

Taking into account the presence of patches in space charge region the radius of these patches have been calculated as[4]

$$r_{patch} = \left[\frac{4\varepsilon_s\varepsilon_0\Delta_{eff}^3}{27qN_D\Delta\Phi_B(\Phi_{B0} - V_n - V)}\right]^{1/2}, \quad (10)$$

where ε_s is the dielectrical permittivity of silicon, ε_0 is the permittivity of free space charge (ε_0 = 8.85 × 10^{-14} F/cm),

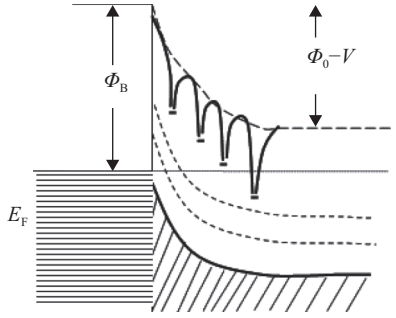

Fig. 9. Potential barrier for discrete charge distribution.

$\Delta_{eff} = \Phi_{Bo} - \Phi_{eff}$, N_D is the doping concentration, $\Delta\Phi_B$ is image forces lowering of the barrier height[4]

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}}, \quad (11)$$

where $E_m = \sqrt{2qN_DV_0/\varepsilon_s\varepsilon_0}$ is the maximum electric field, and V_0 is the diffusion potential.

As a result, calculated radius of patches is about $R = 7.8 \times 10^{-7}$ cm. The obtained value correlates well with the theory of electron transport at metal–semiconductor interfaces[37, 41].

On the basis of the obtained result we presented potential barrier for discrete charge distribution for PtSi/n-Si (111) diode (Fig. 9). Areas with a high doping concentration contribute to the local degeneration of the semiconductor. The field application shifts the quasi Fermi level, the position of the levels and their charge state.

On the other hand, due to PtSi being the semiconductor with a narrow band gap, a series of self-assembled heterojunctions such as Si (111)–PtSi–Si (111) can be formed into Si (111). The presence of hexagonal voids of Si (111) increases the probability of irregular formation of a lot of self -assembled quantum wells[23, 42]. The change in temperature leads to a change in the rate of charge relaxation in quantum wells. At low temperature, the charge in quantum wells does not have time to follow the test signal. It was revealed that the capacitance increase at increasing of the temperature is similar to the case of decreasing of the frequency. This is caused by contribution of recharged carriers at high temperature and low frequency. As is shown from Fig. 4 the temperature dependence of apparent carrier distribution revealed the gaps between the peaks meet the quantum wells[23, 33]. Increasing of the temperature leads to the shifting of the positions of peaks relative to the interface, due to the change in charge relaxation rate.

4. Conclusion

The forward and reverse bias (C–V) and (G/ω–V) characteristics of PtSi/n-Si SBDs were investigated for different temperatures in the region 79–360 K versus applied voltage from −2 to 2 V at a frequency of 500 kHz (20 mV). Capacitance and conductance of diodes in a temperature region from 79 to 360 K change nonuniformly from region to region, which is caused by contribution of recharged carriers. On the basis of the obtained nonlinear C^{-2}–V characteristics have been calculated the temperature dependence of the apparent doping concentration (N_{Dapp}), apparent potential barrier height (Φ_{Bapp}), series resistance (R_s), distribution of interface states (N_{ss}). Due to calculated N_{Dapp} (about 10^{18}–10^{19} cm^{-3}) differing from primary doping level, difference between the Fermi energy level E_F and the bottom of the conduction band (V_n) has negative or positive values, it was concluded that the some regions of the space charge region are degenerate. Taking into account, that the crystal lattice of Si (111) contains deformed hexagonal voids, geometrical size of Pt atom less than the size of the voids and possibility of local penetration of Pt atoms into Si (111) we attributed obtained result to formation of self-assembled local patches. The presence of hexagonal voids of Si (111) increases the probability of irregular formation of a lot of self-assembled quantum wells. The change in temperature leads to a change in the rate of charge relaxation in quantum wells. The obtained result can be used for fabricating multifunctional devices.

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