Summary of HgCdTe 2D Array Technology in the U.K.

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HgCdTe 2D arrays are needed in both medium (MW) and long (LW) wavebands for imaging, search, and track and guidance applications. Often the detector is the performance-limiting component in the system, and it is necessary to use detectors with very low excess noise and few defective pixels. Normally the detector is cooled sufficiently to freeze-out thermally generated leakage currents, so the main interest is to understand the mechanisms that determine the general detector performance and the cause of defective pixels. This paper describes the detector technology and the ion beam junction-forming process. The fundamental performance limits of homojunction HgCdTe technology and the doping levels needed to produce a detector with impact-ionization limited performance are discussed. Extensive studies have been made on defective pixels in long wavelength arrays and some technologies for reducing them are described here. Defective pixels have been found to be associated with material dislocations crossing the p-n junction and a model has been proposed for the noise-generating mechanism.

Key words: HgCdTe, infrared detectors, 2D arrays

INTRODUCTION

Two-dimensional (2D) infrared arrays using HgCdTe are manufactured in both the long waveband (LW) and the medium waveband (MW) for applications requiring near background limited performance and very low defect levels. LW applications in the area of very high performance imaging and search-and-track (IRST) are typified by the STAIRS'C' system which uses a 768×8 close-packed array on 30 μm pitch. MW arrays are produced in a variety of sizes including the OSPREY detector which has a 384×288 matrix on 20 μm pitch. The process that has provided the best radiometric performance and lowest defect levels so far is a via-hole technology, which we call loophole technology. This was originally developed for long linear arrays where the challenge was to produce a mechanically robust hybrid array for cryogenic operation. Originally experience was taken from the SPRITE class of detectors, which owe their durability to the thinness of the HgCdTe monoliths. Thin monoliths have been shown to yield elastically to the thermal mismatch forces without introducing dislocations or changing electrically. The development of the process has been oriented to reducing excess noise in the general population of diodes and minimizing defective elements. Both of these are key to achieving useful performance in 2D arrays and they have driven the development activity towards lower and lower dislocation levels in the array material. By the nature of the process the technology is very different from that used in indium bumped arrays, and the development path to produce low 1/f noise and few defects in 2D arrays has led to some fresh approaches. This paper summarizes the results of some of the development and industrialization programs performed on LW arrays aimed at optimizing the technology and finding the origins of defects and the causes of 1/f noise.

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DESCRIPTION OF HYBRID TECHNOLOGY

LPE Growth Technology

Liquid phase epitaxy (LPE) of HgCdTe at present provides the lowest crystal defect levels, and very good short and long range uniformity. The Te-rich LPE process has been developed specifically for the loophole device technology. As the substrate is removed, the infrared (IR) transmission of the growth substrate, and the crystallography of the near-interface region of the layer are of no importance. This is

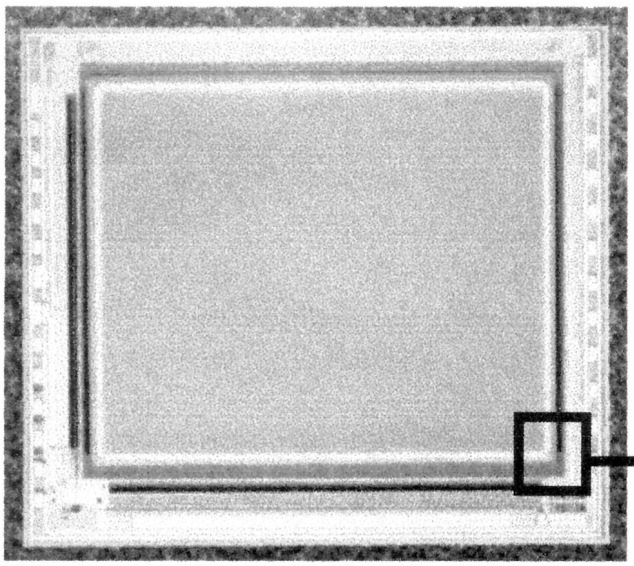

Fig. 1. OSPREY 348×228 HgCdTe on CMOS hybrid with 20 μm pixels.

exploited to concentrate the growth process on creating a very high quality zone in the middle of the wafer from which the monoliths are extracted. As will be seen later, the junction control and uniformity of 2D arrays depends on very good uniformity of the as-grown vacancy doping. Also, for satisfactory reverse-bias characteristics in the final devices, there is a need for low and uniform n-type residual doping, which calls for careful control of the purity of start elements, cleaning solvents, and hardware.

Lattice matched CdZnTe substrates are carefully polished in very clean conditions to minimize nucleation defects. Substrates are oriented on <111>b to better than 0.1° accuracy to avoid short-range terracing. The Zn content for lattice matching is accurately specified for the particular growth conditions and wavelength. There is no direct evidence that these steps are important for producing low defect levels but a macroscopically clean layer is necessary for monolith processing and this can reflect in lower process-induced strain in the final device.

More details of the process, resulting doping levels, and compositional profiles are described elsewhere.[1–4]

Device Technology

The basic loophole technology is described in detail elsewhere[5] and illustrated in Figs. 1 to 3. It differs from most other hybrid technologies in that the growth substrate for the HgCdTe is removed to allow front surface illumination, and the photodiode and interconnect are made in an essentially planar process. The thermal expansion mismatch problem encountered in all hybrid structures is solved in this technology by using a thin monolith of HgCdTe, typically 9 μm thick, bonded rigidly to the silicon multiplexer so that strain is taken up elastically. The aim is to make the devices mechanically and electrically very robust. Figure 2 is a scanning electron microscope view of one corner of the hybrid and this illustrates graphically the membrane-like nature of the HgCdTe monolith on the multiplexer.

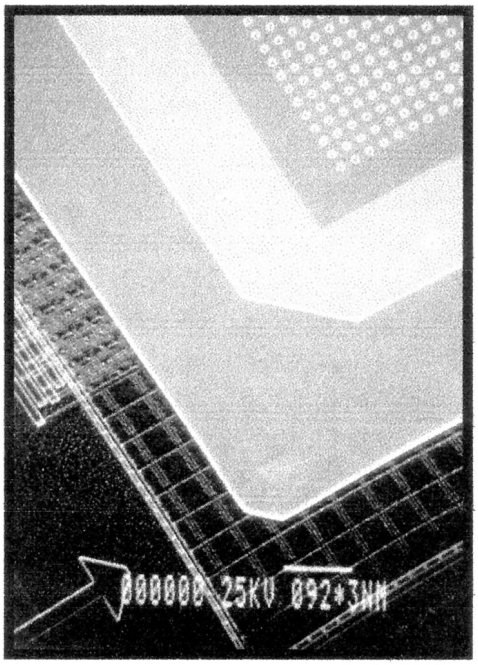

Fig. 2. SEM detail of one corner of HgCdTe monolith.

The monoliths are processed from the low defect zone of the p-type LPE layers and passivated. The earth plane contact to the p-type material is applied around the active area at this stage (visible in Fig. 2). The monoliths are then bonded onto silicon multiplexers. Only one photolithographic stage is used, and this defines a photoresist film with a matrix of small holes. Using ion beam milling, the HgCdTe is eroded through the holes exposing the underlying aluminum contact pads on the multiplexer. The device is then coated with a metal. On removal of the photoresist, the metal remains in the hole to form the bridge between the HgCdTe and the multiplexer pad. Typically the via-hole top diameter is 7.0 μm and the bottom diameter is 3.5 μm with a typical accuracy of ±0.1 μm. The junction is formed around the via-hole during the ion beam milling process, as described in detail in the following section. The via-hole is made part of the sensitive area by only coating one side of the hole with metal and this gives a device with 100% fill-factor.

The photosensitivity is by absorption in both the n- and p-type regions of the pixel, and diffusion of the minority carriers to the junction. The diffusion length in the central n-region is long compared with the n-region width and this provides high quantum efficiencies and low optical crosstalk. The diffusion length in the p-region is controlled by the p-type carrier concentration, and this is tailored by annealing to give the best sensitive area to match the modulation transfer function (MTF) requirement of the system. The total photoelectric conversion efficiency, including obscuration, lateral collection efficiency, absorption, and reflection losses, typically exceeds 65% when referred to the square pixel. Modulation transfer function calculations have shown that for a 30×30 μm pitch a junction

diameter of 23 μm is optimum resulting in a sensitive area plateau of 23 μm diameter sur-rounded by flanks with a diffusion length of 6–7 μm.

The critical part of the process is the creation of an n-type region around the via hole during the ion beam milling process.[6]

Junction Creation Using Ion Beam Milling

Homojunction technologies based on LPE material require a type-conversion technique to produce a photodiode structure. Conventional semiconductor doping techniques cannot be easily applied to HgCdTe. The diffusion of indium for 'n' junctions has been used[7] but high temperature mercury diffusion processes can be unreliable. The conventional semiconductor technique of ion implantation followed by a damage removal anneal is not so easy in HgCdTe because of competing interdiffusion and activation mechanisms during the anneal. The literature has only a few reports of true electrically active ion implantation.[8–10] The unusual characteristic of HgCdTe is that it is fairly easy to type convert p-type material using a variety of processes, including ion beam milling, reactive ion etching, and ion implantation, without the need to anneal. We believe that in each case the junction-forming mechanism is the same and this section describes some of our observations on ion beam formed junctions.

For n-on-p devices, manufacturers obtain the desired p-type level by controlling the density of acceptor-like mercury vacancies within a carrier concentration range of, say, 10^{16} to 10^{17} cm^{-3}. It is relatively straightforward, then, to achieve local type-conversion of the material by neutralizing the vacancies by the in-diffusion of mercury. The low binding energies and ionic bond nature of HgCdTe give rise to two important effects, which are influential in most junction forming processes. The first is the role of mercury, which is liberated readily by processes, such as: ion beam milling[6] and ion implantation.[11–16] This creates a much deeper junction than would be expected from the implantation range. A second effect is the role of dislocations, which may play a part in annihilating vacancies. A further effect is the anomalous diffusion of impurities under the influence of an ion beam, which is a common observation in secondary ion-mass spectroscopy (SIMS) analysis, and can result in an impurity sweep-out effect in the converted volume. The role of mercury interstitials, dislocations, and ion bombardment in the junction forming process is complex and not well understood in detail.

Figure 4 shows schematically the junction growth. The electron beam induced current technique (EBIC) is a very convenient technique to reveal the junction position and sensitivity profile.[16] Our observations are that ion beam milling results in a disordered, n^+, surface layer of approximately 0.5–1 μm in thickness, an n-type doping profile which decreases exponentially away from the surface for 2–3 μm, and a weakly doped n-region of controllable width. The n^+ grade conveniently provides a minority carrier barrier and drift field, leading to a highly sensitive n-region. Control of the width of the weakly doped region is vital for 2D array manufacture. A deeper junction results from a higher beam current, longer milling time (linear), lower beam voltages, and higher ion mass. The advantage of forming junctions with ion beam milling is that the whole process is at low temperature, preserving the original material and passivation quality.

Research on the mechanism for conversion has shown that simplistically the ion beam injects a small proportion of the Hg atoms (approximately 0.02%) into the lattice. These then neutralize acceptor-like Hg vacancies, and leave the lattice weakly n-type by background donor atoms. This model is supported by evidence that the converted volume is approximately proportional to the volume of CdHgTe removed by the ion beam. Additional observations have revealed that the actual mechanism is more complex than this.

1. When the junction depth is plotted against time, it does not go through zero indicating that there is strong initial junction growth in the first few seconds of milling.
2. The ratio of surface damage to junction depth decreases as the gas species becomes larger, i.e., hydrogen produces a pure damaged layer, whereas xenon produces a deep, low-doped junction with little damage.
3. We find that the junction depth is a weak function of temperature and varies little whether the milling is performed on a cryogenically cooled stage or on a heated stage.

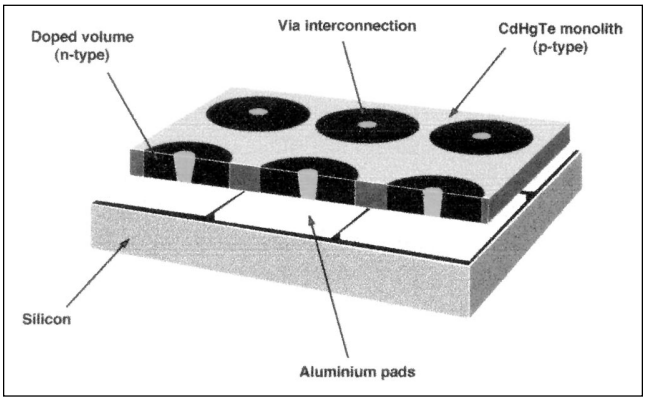

Fig. 3. Schematic of hybrid structure.,

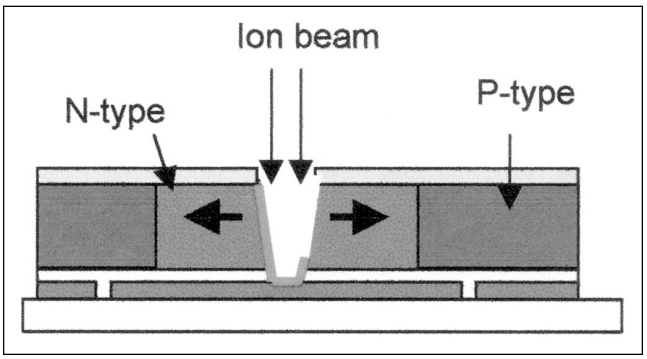

Fig. 4. Junction formation using an ion beam.

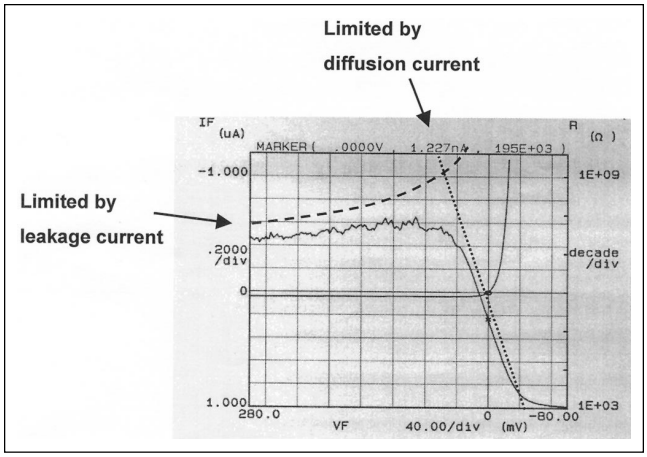

Fig. 5. Typical I-V characteristic for 10 μm cut-off element at 80 K.

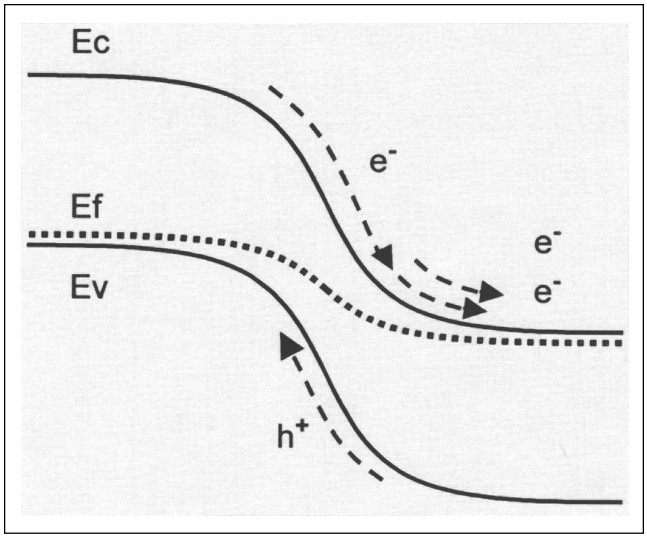

Fig. 6. Principle of excess minority carrier generation by impact ionization.

4. The growth of the junction does not appear to be diffusion-like, but has a tendency to approach a sphere, independent of the shape of the diffusion window.
5. The junction depth is not significantly different in silver-, sodium-, and copper-doped material i.e., when the vacancies are partially occupied by extrinsic dopants. This is also confirmed for gold by Kinch.[17]
6. In very weakly doped material it has been observed that the junction propagation can cover several hundred microns for very short ion beam times.

Our tentative explanation is that ion beam erosion results in three effects: disruption of the lattice at the erosion surface, recoil implantation of surface mercury atoms, and plasma enhanced diffusion. The apparent role of lattice disruption is to inhibit the efficient inwards propagation of mercury, so slowing the junction growth. The propagation mechanism for mercury atoms is almost certainly not conventional thermally activated diffusion. The long-range effect and the athermal nature of the process suggests that the lattice is excited by the ion beam, creating either a knock-on effect for the mercury sub-lattice or anomalous mercury mobility. Another consideration is that the lattice constant for the n-type region will be slightly smaller than that of the p-region and the strain field may encourage a tendency towards spherical geometry.

In the loophole technique the milling time is usually over 1 h and the damage layer is well developed. Our work suggests that the highly damaged surface layer appears to act as a buffer between the low-doped n-type region and the metal contact, and is critical for ensuring long-term stability of the junction.

We do not have experimental data for ion implantation into HgCdTe, but the literature references quoted above report very similar results, and almost certainly the physical mechanisms are the same. Kinch[17] also reports similar behavior for plasma-enhanced milling in the high density, via-hole interconnected diode process (HDVIP).

SOME COMMENTS ON GENERAL PERFORMANCE LIMITATIONS

In LW arrays it is usually necessary to operate HgCdTe diodes in reverse-bias to take advantage of a higher dynamic resistance. A high dynamic resistance ensures a good injection efficiency into the silicon multiplexer and also provides immunity to long-range electrical crosstalk. In reverse-bias there are leakage currents that limit the maximum dynamic resistance that can be obtained in practice. Various models have been proposed for leakage mechanisms in LW HgCdTe—for instance, trap-assisted tunnelling[18,19]—and these models may give good fits for particular technologies. In our technology, which aims to use low doping levels and few dislocations, we have not been able to fit our observations to existing models.

The reverse-bias characteristics of our arrays have two main features. First, the product of p-side diffusion currents (including photocurrent) and reverse bias resistance is fairly insensitive to temperature and cut-off wavelength over a wide range (at least 4–11 μms); and second, the current increases much more slowly with reverse-bias than tunneling models would predict. Figure 5 shows a typical characteristic.

A model based upon an impact ionization effect within the depletion layer gives a good fit to the practical observations.[20] The model proposes that leakage current arises because of the creation of extra electron-hole pairs within the depletion region due to impact ionization by minority carrier electrons from the p-side. Figure 6 illustrates the principle using a band diagram of the junction. The leakage mechanism has a linear relationship with optically injected minority carriers over a wide temperature range and this has been confirmed, as is shown in Fig. 7.

Calculations have been performed on the effect of impact ionization on homojunction performance as a function of the doping levels[21] and this is shown in

Fig. 8. These predict that at 10 μm cut-off and 77 K a carrier concentration on the n-side of the junction of 4×10^{14} cm^{-3} results in a photocurrent, reverse-bias resistance product of approximately 8.5 V. This is equivalent to a satisfactory signal injection efficiency of 0.999. Note that in this model the injection efficiency is predicted to be independent of photocurrent. We have confirmed this in medium waveband devices over two orders of magnitude of flux. The carrier concentration in the p-region has a second order effect compared with that of the n-region, for the range of concentrations normally used. A weakly doped and uniform n-side is essential for good junction characteristics in homojunction structures and we believe that ion beam milling and ion implantation produce this automatically.

TECHNOLOGY FOR MINIMIZING DEFECTS IN 2D ARRAYS

Multiplexed 2D arrays are effectively d.c. coupled to the infrared scene, especially in staring applications, and low frequency noise (1/f noise) can be a controlling factor in the general performance of the sensor. Most manufacturers have developed processes that minimize 1/f noise with an appropriate choice of passivation technology and junction processes. The quality of the sensor then becomes limited by defects in the array. Defective diodes, when they arise, are usually characterized by low reverse-bias resistance and high 1/f noise. We have tried to identify the main causes of defective diodes and develop technologies to minimize them.

Existing Knowledge for 1/f Noise Sources in HgCdTe

Excess noise in HgCdTe photodiodes normally takes the form of conventional 1/f noise. The scatter within databases is usually large and the noise depends strongly on the technology used. However, several workers report noise roughly proportional to leakage current or effectively inversely related to shunt resistance.[22,23] The noise has been associated with surface leakage currents,[24] trap-assisted tunneling across a pinched-off surface depletion region,[25,26] and g-r currents originating from junction defects, such as dislocations.[27]

Many workers[23,28–31] have found that the reverse-bias characteristics of HgCdTe diodes depend strongly on the density of dislocations in the material. This is an important observation for HgCdTe device technology, because of the ease with which dislocations can be introduced, due to materials growth and strain in the device fabrication process. The electrically active nature of dislocations is well reported[32,33] and is understood in terms of an increase in both states within the bandgap and recombination centers.

One of the problems of analyzing the literature is that the actual device structure is critical to establish the importance of various leakage mechanisms. However, we have difficulty reconciling existing models with our observed data, particularly the reverse-bias characteristic and the current dependencies of the 1/f noise in our structures.

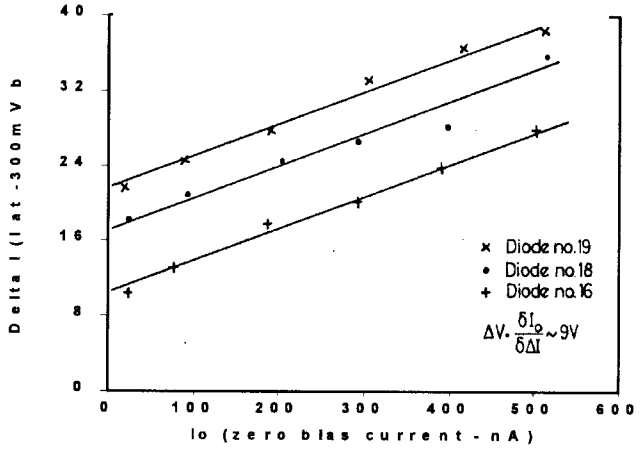

Fig. 7. Leakage current as a function of photocurrent.

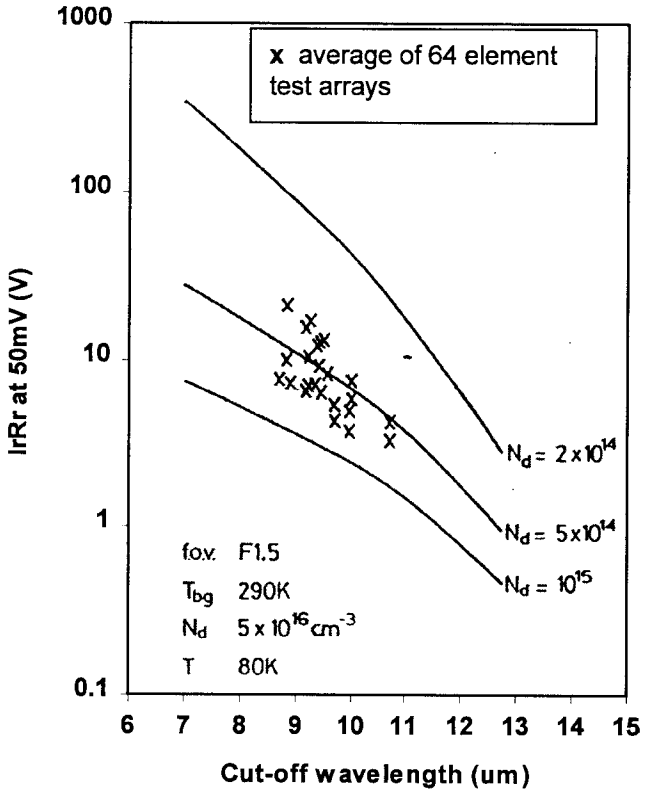

Fig. 8. $R_r \cdot I_r$ versus cut-off wavelength with n-type doping as parameter.

Results of Defect Tracing in the LPE Layer

Defect etches suggested by Nakagawa[34] for <111>a surfaces of CdZnTe substrates and Hanert & Schenk (H&S)[35] for <111>b surfaces are routinely used to assess the etch pit density (EPD) of the material. For revealing structure in arrays, strain revealing etches provide disclosure of p-n junctions, dislocations, and strain fields. One of the advantages of the loophole process is that measured arrays can be easily etched to correlate device performance with defect structure and the exact position of defects can be determined with reference to the p-n junction.

Mapping has been performed on CdZnTe substrates, HgCdTe LPE layers through to final arrays. This has

shown an almost 1:1 correspondence of strong etch pits in the substrate with similar strong etch pits in the grown material. The etch pits are associated with threading dislocations which appear to run normal or near normal to the <111>b surface.

Chemically etched bevels on LPE layers have been used with the H&S etch to give plan view information of how the defect density varies throughout the depth of the LPE layer. This has shown that with careful control of the HgCdTe growth rate the EPD can be contained to a range from 3 to 7×10^4 cm^{-2}, which is dictated by the substrate. Typically, close to the interface (just under 2 μm) a few small pits are observed, but above this a band of high EPD is found. Directly above this, individual defect pits start to agglomerate into lines, having 3-fold symmetry parallel with the <111> planes. At between 3 to 4.5 μm the EPD decreases to a low level and stays constant throughout the rest of the layer. If the growth rate is not correct, the EPD will tend to remain at levels above 10^5 cm^{-2} through the layer.

Observations on Excess Noise in Photodiodes

An important general observation is that dislocations have no effect on the diode performance unless they physically intercept the p-n junction. Glancing incidence has no apparent effect, indicating that dislocations do not act as significant centers for higher thermal generation or alter impurity distributions in the nearby region by gettering.

In arrays, interception of threading dislocations with the junction can cause strong leakage in reverse-bias, but this is a variable effect, possibly because these dislocations can become randomly decorated during growth. Consequently, the threading dislocation density in the substrate is very important for controlling defect levels in the array. Threading dislocations can occasionally result in very low reverse-bias resistance, nearly pure resistors, and this is difficult to explain. One speculative possibility is that the decorated dislocation is associated with a tensile stress field, which can locally narrow the bandgap and promote interband tunneling within the depletion region.

Defect etching of hybrid arrays sometimes shows a weaker EPD pattern associated with process-induced defects (PIDs). These also appear to rise vertically through the layer, but they have a very much weaker effect on the leakage current.

LW arrays have been measured for noise spectra and I-V characteristics, and then surveyed pixel-by-pixel for PIDs through the junction. A key observation is that diodes with etch pits on the junction have enhanced 1/f noise and degraded reverse-bias characteristics. The database is highly scattered but dislocations appear to behave as almost pure shunt resistors.

The characteristics of degraded diodes can offer clues to the mechanism involved in the increase of noise and decrease of shunt resistance (R_{sh}) due to dislocations. The principle observations are as follows:

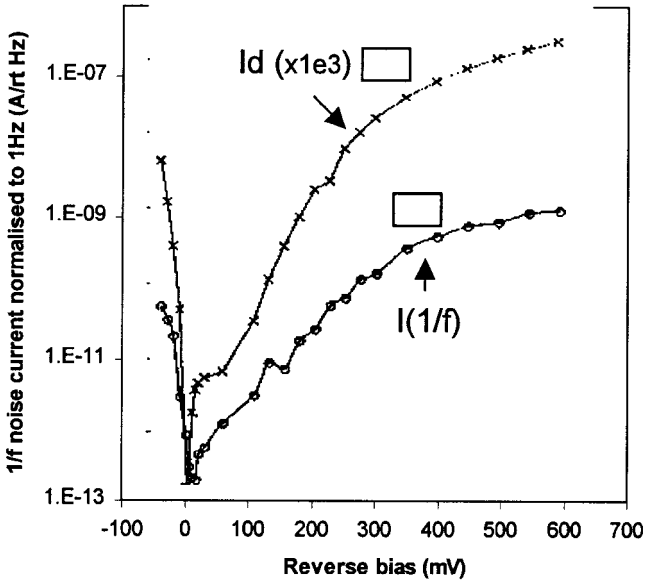

Fig. 9. 1/f noise and diode current versus bias.

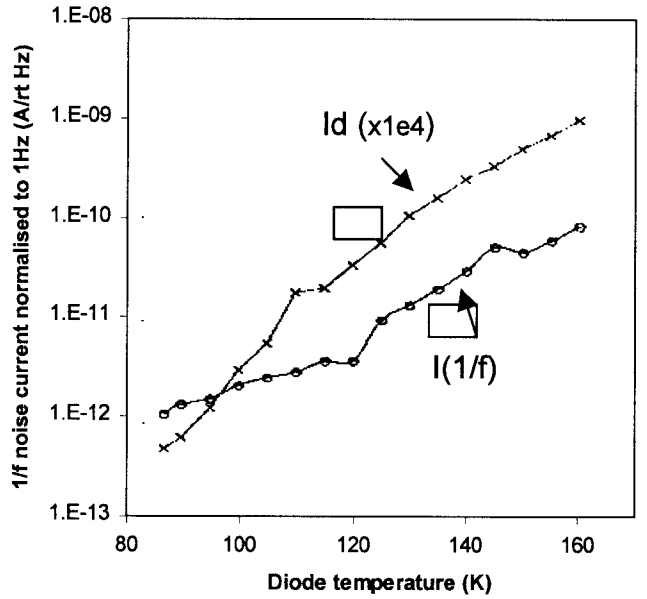

Fig. 10. 1/f noise and diode current versus temperature.

1. The 1/f noise is roughly dependent on R_{sh}^{-n} where n is typically around 1.
2. The 1/f noise is dependent on both the thermal diffusion current and the photocurrent from the p-type side of the junction. (The dependence on photocurrent supports the work of Williams).[27] Figures 9 and 10 illustrate this graphically for a defective diode.
3. The I/V characteristics of noisy diodes show a flat or slightly decreasing dynamic resistance with increasing reverse bias. Figure 11 shows a typical characteristic with one PID on the junction.
4. The ratio of noise current normalized to 1 Hz against detector current is about 10^{-5} for an impact ionization limited diode with no etch

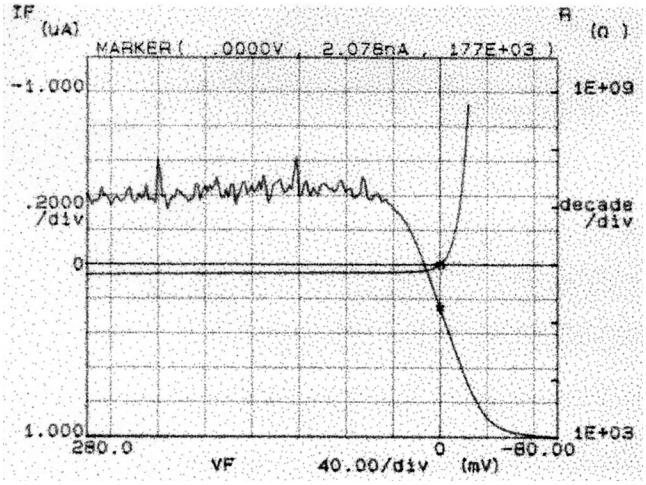

Fig. 11. I-C charcteristic of diode with dislocation through junction.

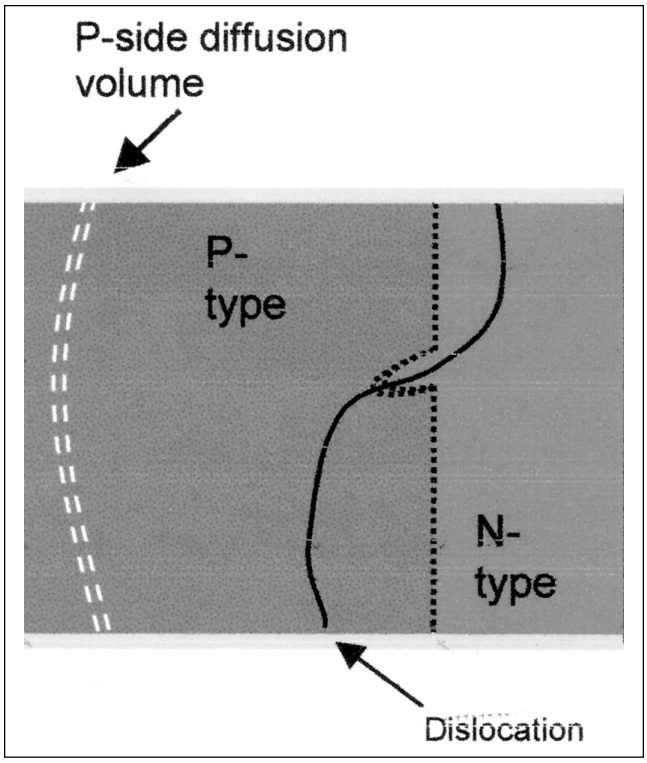

Fig. 12. Proposed mechanism for 1/f noise in homojunction HgCdTe due to dislocations.

pits in the junction. With one etch pit the ratio is about 10^{-4}, but can be variable. In both cases this refers to 77 K operating temperature, 10 μm cut-off, and 50 mV reverse-bias voltage.

5. Defects tend to have a weak temperature coefficient and tend to heal at lower temperatures.

Proposed Model for Origin of Noise and Shunt Resistance

The model that we propose is based on a now-accepted view[33] that dislocations in HgCdTe are associated with n-type pipes. This has been reinforced by a number of observations, including a direct one in our work where dislocated material was observed to connect adjacent diodes electrically at low bias but not at higher bias, where the dislocation pipes were presumably depleted. Figure 12 shows a schematic of the junction. If dislocations cause a microscopic extension of the n-region into the p-region then the collecting volume for photocurrent and thermal current on the p-side is controlled by the extension. Any fluctuation in trap occupancy along the dislocation could cause the depletion region extension to fluctuate and apply a noise modulation to the current from the p-side. The detailed physics of the trapping and detrapping mechanism and the generation of a 1/f noise spectra is not fully understood, however the link of dislocations and 1/f spectra is well established.[23,28–31] To account for the observed noise, the fluctuation length is only 50–100 nm. The model explains the dependence of noise on diffusion and photocurrent from the p-side. The variability in the database would result from the range of possible interception angles of the dislocation and the junction.

The model predicts the observed dynamic resistance versus bias characteristic as follows: The depletion layer associated with the dislocation has a roughly square root dependence on the applied bias. The increased current will have a square or cube dependence on the depletion layer extension depending on the geometry of the lateral collection area. As a consequence, the current will increase linearly or slightly superlinearly with bias, which, in fact, is the observed behavior.

Technology for the Reduction of Point Defects

Threading dislocations are probably the biggest concern in LPE material for LW arrays. Substrates can be specified at levels down to 3 to $7\times10^4\,cm^{-2}$. The substrate defect level can be as low as mid-$10^3\,cm^{-2}$ in some horizontal Bridgman CdZnTe, but this is not easy to reproduce. Similar defect densities are found in CdTeSe material, but the impurity levels have proved difficult to control in the past. It seems that device processing, therefore, must expect to cope with threading dislocation levels in the mid $10^4\,cm^{-2}$ range for routine HgCdTe epilayers. For via-hole technologies the junction lies normal to the 111 plane and should miss most of the threading dislocations. Nevertheless, around 1% of diodes should be affected by dislocations and experience some increase in 1/f noise. For long linear arrays with time delay and integration (TDI) a defective element disabling function is highly effective in neutralizing point defects at this level and is used routinely. In 2D arrays this cannot be employed and various pixel replacement strategies are used.

The main cause of process-induced defects in the loophole process was found very early in the development to be the glue mounting process of the HgCdTe monolith onto the silicon multiplexer. The process-induced defects were found to correlate with steps on the silicon surface, and in the worst case, when the crystal orientation is aligned to the silicon topology the etch pits agglomerated into slip lines. It was found to be essential to use panelized silicon, a thin, uniform

glue layer without particulates, and low shrinkage glue. This process routinely produces a very weak etch pit pattern and no spatially correlated high noise pixels.

It is difficult to make cross-comparisons with indium-bumped, planar junction technologies because the retention of the substrate may give extra rigidity and prevent PID formation. Also, the planar geometry of the junction will alter the interception probability of dislocations and their noise contribution.

In MW arrays threading dislocations appear to be the main cause of defects but the proportion of diodes is very much less. At 77 K almost all of the defects are frozen out. At 100 K the percentage of diodes outside of the normal population averages about 0.1% for 5.0 μm cut-off material. This increases by a factor of about 3 for each 10 K increase in temperature. At around 150 K weak PIDs start to become active as thermally-generated diffusion currents increase and become modulated by dislocation extensions.

CONCLUSIONS

For 2D arrays, where there is a particular interest in low defect levels and a generally low level of excess-noise, it is essential to control crystallographic defect levels in the vicinity of the p-n junction. LPE material and via-hole technology can provide low levels of threading dislocations and few process-induced dislocations, as well as providing a low intersection probability for the junction. The limit to the number of defects in 2D arrays is set by the quality of the original CdZnTe growth substrate. The low and uniform n-type doping level that results from ion beam-generated junctions is important for minimizing leakage currents and improving the general radiometric uniformity. A new model for the generation of noise from dislocations crossing the p-n junction has been proposed and this has proven to fit quite well with our observations on the properties of excess noise in defective pixels.

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