In situ electron holographic analysis of biased Si n^+ -p junctions

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The two-dimensional electrostatic potential distribution across Si n^+ -p junctions over a range of positive and negative biasing conditions has been studied *in situ* using off-axis electron holography. A sample holder with a movable probe as the electrode was used to bias focused-ion-beam-milled membranes during hologram acquisition. Reverse biasing of the junction resulted in an increase in potential across the junction, whereas the junction potential decreased with forward bias and eventually completely disappeared. The trends of the experimental results matched reasonably well with computer simulations. © 2008 American Institute of Physics. [DOI: 10.1063/1.2908045]

Off-axis electron holography has been used to measure two-dimensional (2D) electrostatic potential profiles associated with dopant distributions in semiconductor devices. 1-6 Analysis of biased devices under actual operating conditions would make this technique even more useful. However, preparation of suitable samples has been a major difficulty for these types of applications. ^{2,7–11} Initial biasing attempts involved samples prepared by chemical thinning, and electrostatic fringing fields were observed outside the sample edge. 12 Quantitative results were later obtained from reverse biased samples prepared by cleavage and focused-ion-beam (FIB) milling. 13,14 However, the sample preparation approach used in these latter biasing studies cannot be used for specimens consisting of real device structures. In this current study, a different biasing geometry has been developed that should be suitable for the analysis of 2D device structures, and results obtained under a range of biasing conditions have been compared with simulations.

The electron holography studies were performed using a FEI CM200 FEG transmission electron microscope (TEM) equipped with a Lorentz lens and an electrostatic biprism.³ A special TEM holder developed specifically for biasing samples was used. 15 This sample holder has two fixed electrodes, and one movable probe with a tip diameter of about 5 μ m which can serve as a third electrode. The sample consisted of a heavily doped n-type (n^+) region formed by rapid thermal diffusion of phosphorus at 850 °C from a spin-ondopant (SOD) source into a p-type substrate (boron concentration of $\sim 10^{18}/\text{cm}^3$). The sample was patterned by photolithography with a 200-nm-thick oxide mask grown by lowpressure chemical vapor deposition before applying SOD to the substrate. 16 After junction fabrication, the SOD was selectively removed by HF etching. Conventional mechanical polishing was used to thin the sample to $\sim 30 \mu m$ after sputter deposition of a Cr layer for protection of the top surface. The sample was then attached to a half-cut copper washer, and a 1- μ m-thick Pt pad and a 0.5- μ m-thick Pt line were deposited using a Ga⁺ ion beam, as illustrated in Fig. 1(a). Finally, a region containing the edge of the oxide mask and the unmasked region was FIB milled to a thickness of less than 300 nm in preparation for electron holography. Figure 1(b) shows a tilted scanning-electron-microscope image of a prepared sample. The Pt pad is located on the oxide layer, while the Pt line runs across the opening area (n^+ region) and is also connected to the Pt pad. The Pt pad and line were used as the electrode for the n^+ region by physical contact with the movable electrode in the sample holder, while the p-type Si substrate was grounded by silver paste and fixed electrodes.

Figure 2(a) shows the bright-field TEM image of the sample, with contact made between the movable electrode and Pt pad. Since the contact was somewhat sensitive to mechanical vibration, a current-voltage (I-V) curve was usually obtained to check for electrical continuity before hologram acquisition. A typical I-V curve obtained as a result of biasing the sample is shown in Fig. 2(b). The polarity of the applied voltage is shown inverted for convenience. The threshold voltage is around 0.6 V and the reverse breakdown voltage occurs at around -2 V. Since there is an oxide mask under the Pt pad, there is no direct electrical connection between the probe and the p-type Si substrate. However, it is likely that damage layers induced by FIB milling on both

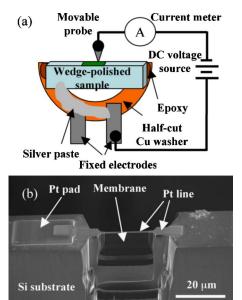


FIG. 1. (Color online) (a) Schematic showing geometry used for *in situ* sample biasing during electron holography observation. (b) Scanning electron micrograph showing thin membrane as prepared by FIB milling, as well as Pt pad and Pt line to be used for biasing sample.

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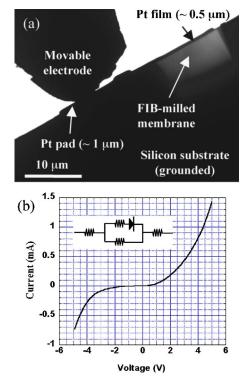


FIG. 2. (Color online) (a) Bright-field TEM image showing sample with movable electrode contact. (b) Current-voltage (I-V) curve from the sample. The inset shows circuit schematic.

sides of the membrane provide additional current paths. These leakage paths can be represented as an extra resistance in parallel with the n^+ -p junction, which is indicated by the diode symbol in the schematic circuit shown in Fig. 2(b). This current leakage path will also serve as a current-limiting device for the n^+ -p junction by dividing the total current in the circuit and limiting current flow through the junction itself. The additional series resistance sketched schematically in Fig. 2(b) represents all components of resistance present in the circuit, including any contact resistance between the Pt line and the n^+ region, resistance of the FIB-milled membrane, resistance of the Pt pad and line, and resistance of the Si substrate.

Off-axis electron holograms were recorded over a range of forward, zero, and reverse bias conditions, and reconstructed images showing the electrostatic potential across the junction are given in Figs. 3(a)-3(c), respectively. Negative 10 V was needed to reach a flatband condition, when the n^+ -p potential contrast completely disappeared, as shown in Fig. 3(a). This high flatband voltage implies high series resistances elsewhere in the effective circuit, where significant voltage drops must occur. Positive 10 V applied to the Pt pad brought the n^+ -p junction to a strongly reverse biased condition, corresponding to an increase of the potential barrier across the junction, which is visible as enhanced contrast of the n^+ region in the p-type substrate in Fig. 3(c). It is also clear that the p-type substrate is not entirely covered by the oxide mask layer. As indicated in Fig. 3(b), a small part of the p-type substrate seems to be in contact with the top electrode. This unmasked p-type region is likely to have resulted from overetching of the oxide mask layer during HF etching, which was intended to selectively remove the SOD layer. The unmasked p-type region is likely to provide an additional current path through the sample.

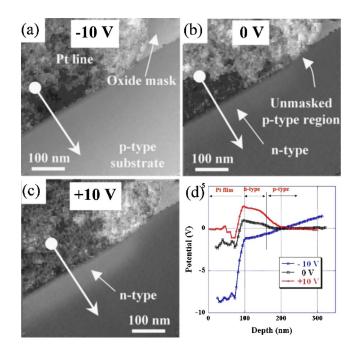


FIG. 3. (Color online) Electrostatic potential images of oxide mask sample: (a) forward bias; (b) zero bias; and (c) reverse bias. Junction contrast is enhanced with reverse bias: *n*-type region is brighter in (c) than in (b). (d) Electrostatic potential profiles from the regions indicated in (a)–(c).

Potential profiles across the junction, as shown in Fig. 3(d), were obtained along the arrows indicated in the reconstructed potential images of Figs. 3(a)-3(c). For convenience, the position of zero potential is assumed to be located at the point where the p-type substrate region begins. It is clear that the junction contrast disappears by applying -10 V to the n^+ region (forward bias), whereas it is enhanced by applying 10 V (reverse bias), while the unbiased junction displays a potential difference of $\sim 1.0 \pm 0.1 \,\mathrm{V}$, which agrees with the result previously obtained from a wedgepolished sample of the same junction that was unbiased. 11 This agreement implies that the effect of the electrically inactive surface depletion layer normally caused by FIB milling^{8,9} has been offset by cycling the junction through the range of biasing conditions, which most likely heats up and anneals the sample. Forward bias generates a positive slope in the potential profile toward the substrate direction while reverse bias generates a small but negative slope. The smaller slope under reverse bias conditions implies that the voltage drop across the junction is smaller than under forward bias, i.e., a larger proportion of the voltage drop occurs across the junction itself under reverse bias. The change in potential across the junction on going from the reverse bias condition to the unbiased condition is measured in Fig. 3(d) to be around ~1.6 V, which is considerably smaller than the applied bias of 10 V. Thus, the remainder of the applied bias must be accounted for the various series resistance components elsewhere in the sample. From the positive slope in the forward-biased potential profile, and considering the built-in potential of 1 V from the unbiased potential profile, the potential drop from the n^+ region to the p region is around -2.2 V. It should be noted that the position of the junction, as defined by half of the total potential difference, does not appear to be shifted under either biasing condition. These results also suggest that reverse sample biasing could be used as a means to enhance the visibility of junctions with small

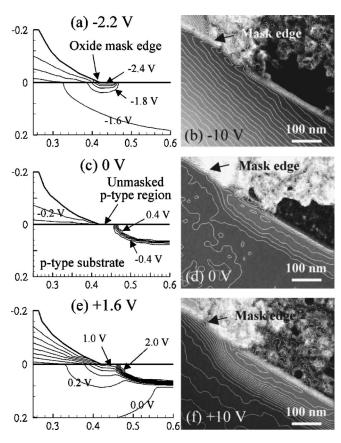


FIG. 4. Simulated potential distributions: (a) -2.2 V bias, (c) zero bias, and (e) +1.6 V bias, respectively. Separation between contour lines is 0.2 V for all images. The unit of x and y coordinates in (a), (c), and (e) is microns. Contoured potential images with bias applied to n^+ region; (b) -10 V bias, (d) zero bias, and (f) +10 V bias.

potential differences that might otherwise be difficult to observe using electron holography.

The potential distributions within the biased sample examined here have been simulated using DIOSTM, MDRAWTM, DESSISTM, and ISE-TCAD. More detailed information about these simulations for biased devices can be found elsewhere.¹⁷ The top electrode for biasing of the simulated n^+ -p junction structure was defined so that the entire top surface had a metallic layer running across the n^+ -doped Si region and the oxide mask layer. After defining the substrate as the second electrode, biasing simulations were performed. The unmasked *p*-type region, connected to the top electrode [i.e., the Pt line in Fig. 1(b)], and the overetched oxide mask shape were also considered. The p-type substrate potential was set to -0.38 V as the reference default setting of the simulation software. The simulated electrostatic potential distributions under forward, zero, and reverse bias conditions are shown in Figs. 4(a), 4(c), and 4(e), respectively. The external biases across the junction of -2.2 V for forward bias, and +1.6 V for reverse bias, as experimentally determined in Fig. 3(d), were used for the simulation. For comparison, the potential distributions experimentally obtained in Figs. 3(a)–3(c), are also shown with contour lines in Figs. 4(b), 4(d), and 4(f). The separation between contour lines is 0.2 V.

The forward bias removes the potential barrier across the junction and creates a linear potential slope in the Si substrate, as shown in Figs. 4(a) and 4(b). The simulated potential slope in the Si substrate is smaller than experimentally observed. This difference is due to different biasing conditions between the experiments and the simulations. It should also be noted that the FIB-milled membrane (\sim 230 nm) is thinner than the simulated structure (1000 nm), thus, resulting in the higher resistance of the FIB-milled membrane. The unmasked p-type region is visible as a potential dip close to the surface, as shown in Fig. 4(a). This feature is absent in the potential image of Fig. 4(b) experimentally obtained. Thus, it is possible that the electrical contact between the Pt line and the small unmasked p-type region is not stable. For the reverse biased simulation, the potential increase across the junction and the small negative slope in Si substrate can be observed in Fig. 4(e).

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