Solar Energy Materials & Solar Cells 144 (2016) 472–480

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

CdTe solar cell performance under low-intensity light irradiance

Kai Shen [a], Qiang Li [a], Dezhao Wang [a], Ruilong Yang [a], Yi Deng [c], Ming-Jer Jeng [d], Deliang Wang [a,b,*]

[a] Hefei National Laboratory for Physical Sciences at the Microscale, University of Science and Technology of China, Hefei, Anhui 230026, PR China
[b] Key Laboratory of Materials for Energy Conversion, Chinese Academy of Sciences, University of Science and Technology of China, Hefei, Anhui 230026, PR China
[c] College of Electronical and Information Engineering, Hankou University, Wuhan, Hubei 430212, PR China
[d] Department of Electronic Engineering and the Green Technology Research Center, Chang Gung University, Taoyuan 333, Taiwan

ARTICLE INFO

Article history:
Received 16 March 2015
Received in revised form
17 August 2015
Accepted 26 September 2015

Keywords:
CdTe
Weak light
Shunt path
Solar cell

ABSTRACT

Study of the device characteristics of a CdTe solar cell under weak light irradiance (E_{irra}) is important both for the understanding of the fundamental device physics and for the commercial application, where E_{irra} with intensity much less than one sun is often encountered for an outdoor solar cell module. In this study, CdTe solar cell performance under E_{irra} as low as 0.015 sun was studied. Both the fill factor (FF) and the open-circuit voltage (V_{oc}) were found to be critically affected by the shunt resistance at low E_{irra}. The current shunting depends critically on the physical location of the shunting paths in the CdTe absorber layer. Space-charge limited current (SCLC) was identified to be an important contribution to the shunting current in thin film CdTe solar cell. At an E_{irra} as low as 0.015 Sun, CdTe solar cell with a high shunt resistance maintained an efficiency of ~70 to 80% of the value tested at the standard AM1.5 E_{irra}. The experimental results showed that polycrystalline CdTe thin film solar cell is a good photovoltaic device for electric power generation at low E_{irra}. This study provides constructive guidelines for the future design and fabrication of CdTe solar cells.

1. Introduction

CdTe has a nearly ideal direct band gap of 1.45 eV and an absorption coefficient as high as 10^5 cm^{-1} for the photons with energy higher than the band gap. It is an efficient semiconductor material for the fabrication of low-cost thin film solar cell. At the standard test condition (STC) of the AM1.5 Sun spectrum with an intensity of 1000 W/m^2, the highest efficiency for CdS/CdTe heterostructure solar cell is 21.5% [1]. CdTe solar cell is one of the thin-film solar cells which have been commercialized. On the commercial photovoltaic market it has been successfully maintaining a competitive challenge to the dominant Si-based solar cell products. However, due to the relatively small scientific community devoting to the basic research study on the CdTe material and the CdTe solar cell, much of the technological procedures for CdTe solar cell fabrication are based on the empirical experience. The fundamental studies related to the CdTe material and devices are relatively scarce. Currently almost all the CdTe solar cell efficiency has been tested and analyzed under the STC. Consequently the fabrication processes of a solar cell have been optimized with respect to the cell performance under the STC. In fact, the standard AM1.5 illumination irradiance is not the representative E_{irra} received by an outdoor-employed module. Rather the outdoor sun light irradiance usually has an intensity range of 100–1000 W/m^2, and even lower at the Sun set and down time. Indoor photovoltaic products designed for low-power microelectronics, weak E_{irra} with low light intensity in the order of 1–10 W/m^2 is the energy source of a solar cell [2]. Efficiency of a solar cell tested at the STC, therefore, is not a reliable guide to a cell performance over the light intensity range from 1 Sun down to 0.1% Sun [2,3].

From the above discussions it can be seen that study of a solar cell under low-intensity E_{irra} is realistically more important than that under the STC. This is especially true for a thin film solar cell module, which is made of monolithically connected unit cells [4]. It will be shown in this study that the weak light performance of a CdTe thin film solar cell depends critically both on the specific micro structure and on the specific micro-electrical shunting paths. If the individual unit cells have almost the same device performance at the STC but behave much differently at weak E_{irra}, the module would have much low efficiency than the nominally claimed efficiency. The device performance mismatch between the unit cells under weak E_{irra} would induce hot spot effect, which is the main concern for commercial solar cell modules [5]. For

* Corresponding author at: Hefei National Laboratory for Physical Sciences at the Microscale, University of Science and Technology of China, Hefei, Anhui 230026, PR China.
E-mail address: eedewang@ustc.edu.cn (D. Wang).

http://dx.doi.org/10.1016/j.solmat.2015.09.043
0927-0248/

polycrystalline thin film solar cells, such as CdTe and $CuIn_xGa_{1-x}Se_2$, from this study it can be seen that the material and device uniformity is highly demanded for the fabrication of high efficient cells worked under weak E_{irra}.

Solar cell performance under low E_{irra} depends critically on the cell fabrication technology, cell suppliers, and cell types such as single-, polycrystalline-, or amorphous-based semiconductor material [2,3,6–8]. Under low E_{irra} condition, the photocurrent is very low, the influence of series resistance is relatively small due to the small electrical voltage drop on the series resistance. On the other hand, the influence of the shunt resistance plays an important role if the E_{irra} becomes very weak, and the shunting current may be comparable to the photocurrent. Studies on thin film $CuIn_xGa_{1-x}Se_2$ solar cell have shown that the shunt resistance has a strong influence on the low-intensity E_{irra} efficiency [9]. Our previous study on CdTe thin film solar cells under high-intensity light irradiance showed that the electrical resistance of the cell front electrode is the limiting factor for the efficiency of a solar cell working under concentrated light irradiance [10]. Tiwari et al. has studied CdTe/CdS solar cell device performance under low light irradiance, and the cell performances were compared to the conventional crystalline Si and GaAs solar cells [11]. Their experimental results showed that CdTe thin film solar cell demonstrated superior relative efficiency and voltage at low intensities compared to the c-Si and GaAs cells. At an E_{irra} as low as 1 W/m^2, the open-circuit V_{oc} of a CdTe solar cell still had a value as high as 600 mV. The reported results indicated that the CdTe solar cell is a promising photovoltaic device for indoor and low-E_{irra} environment application [11]. The authors employed the conventional 1-diode model to analyzed the data obtained. In this study, the device performance of CdTe solar cells under weak E_{irra} was studied. The current–voltage curves were fitted by employing a more realistic compact electric circuit model, in which the contributions from different possible current shunting mechanisms were considered. The influences of different shunting paths/mechanisms, including the space-charge limited transport, the effect of weak diode, ohmic and non-ohmic shuntings, on the cell performance were analyzed. The experimental results and analyses provide constructive guidelines for the future design and fabrication of CdTe thin film solar cells.

2. Experimental

The CdTe solar cells fabricated in this study had a structure of glass/SnO_2:F(FTO)/n-CdS/p-CdTe/back contact electrode [12,13]. CdS window layers with a thickness of ~80 nm were prepared on glass/FTO substrates by chemical bath deposition (CBD) technique from a solution composed of de-ionized water, cadmium acetate, ammonium acetate and thiourea. An intrinsic tin oxide interlayer was not introduced between the FTO and the CdS layers. After heat treated in a $CdCl_2$ atmosphere, high crystalline CdS thin films with a mono-grain layer were fabricated, as shown in Fig. 1(a). The detailed CdS fabrication process can be found in our previous work [14]. The CdTe absorber films, which had a thickness of ~4 μm, were deposited by the close-spaced sublimation (CSS) technique in a home-made film-deposition system [13]. Fig. 1(b) shows the SEM cross-sectional microstructure of a high-crystalline quality CdTe film fabricated in our laboratory. It can be seen that the CdTe films had an excellent crystallinity with large vertically grown grains. Most of the CdTe grains were preferentially grown along the normal direction of the film, leading to the formation of through-thickness grains. This is desirable for the fabrication of a high efficient CdTe solar cell. The carrier scattering at the grain boundaries were minimized in such a structured polycrystalline CdTe thin film. Such a microstructure is also favorable for carrier transport governed by the space-charge limited current. The cell structure glass/SnO_2:F (FTO)/n-CdS/p-CdTe was then heat treated with the presence of a $CdCl_2$ thin layer on the CdTe surface in the air atmosphere and then etched in a nitric–phosphoric (NP) solution. The back contact in this study was a Cu/Au bi-metal layer, which was prepared by successive thermal evaporation of Cu and Au in a vacuum chamber. The Cu thickness in this study was 5 nm. This is the optimal thickness for the fabrication of high efficiency CdTe solar cells [13–15].

The morphological microstructures of the films were characterized by using a field emission scanning electron microanalyser (SEM, Sirion 200). The cell current–voltage J–V curves were measured using a solar simulator (Oriel Sol 3A, USA), which has a standard AM1.5 (1 kW/m^2, 25 °C) illumination intensity. The weak light intensity less than the standard AM1.5 irradiance was obtained by using neutral-density filters (Thorlabs NDK01, USA). The illumination intensities were calibrated by a mono-crystalline silicon reference solar cell.

3. Results and discussions

3.1. Device performance of a well-fabricated CdTe solar cell under weak light irradiance

The current voltage J–V curves of a CdTe solar cell measured under STC and weaker light intensity are shown in Fig. 2. Under 1-Sun light irradiance, the CdTe solar cell has a V_{oc} of 786.2 mV, J_{sc} of 24.7 mA/cm^2, fill factor of 67.5%, and an energy conversion efficiency of 13.1%, indicating that the cell has been well fabricated regarding both the film crystalline and junction quality of the solar cell.

The output current of a solar cell can be described as the following equation [10,16],

$$J = J_0\left[\exp\left\{\frac{q(V-JR_S)}{Ak_BT}\right\}-1\right]+\frac{V-JR_S}{R_P}-J_L \quad (1)$$

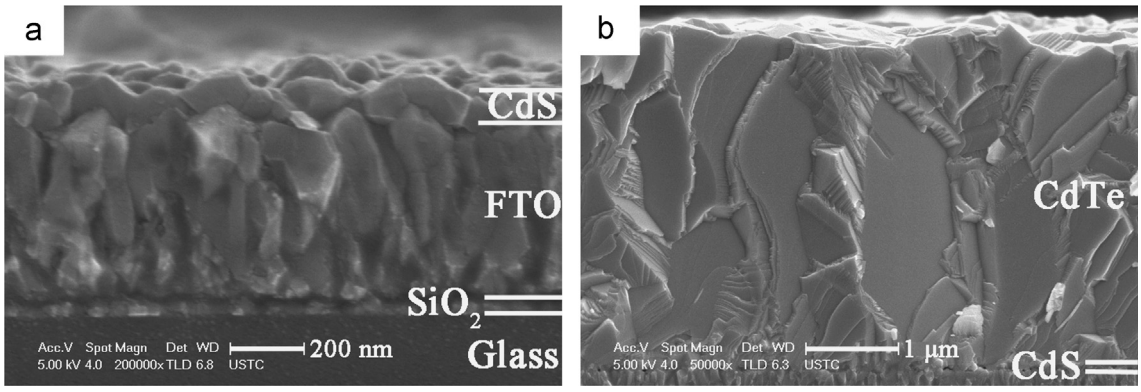

Fig. 1. SEM cross-sectional microstructures of (a) a mono-grained CdS film on Glass/SiO_2/FTO; and (b) of a 4-μm-thick CdTe film.

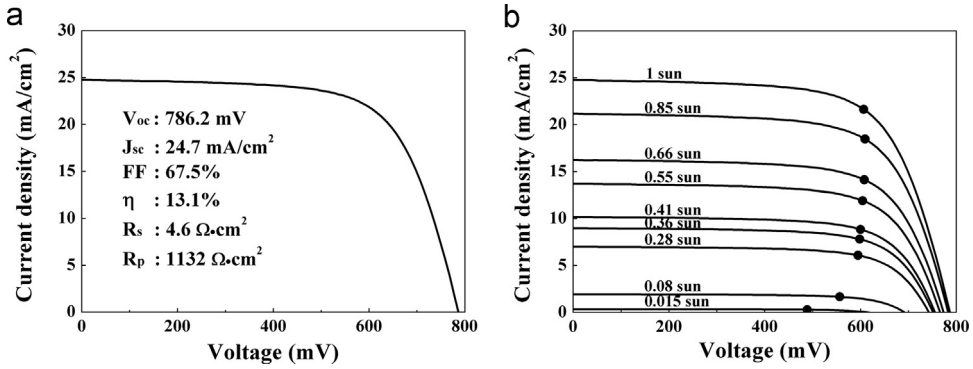

Fig. 2. (a) Current–voltage curve of a CdTe solar cell measured under one-Sun, and (b) under different light irradiance intensities. The black dots on the $J-V$ curves indicate the maximum-power point.

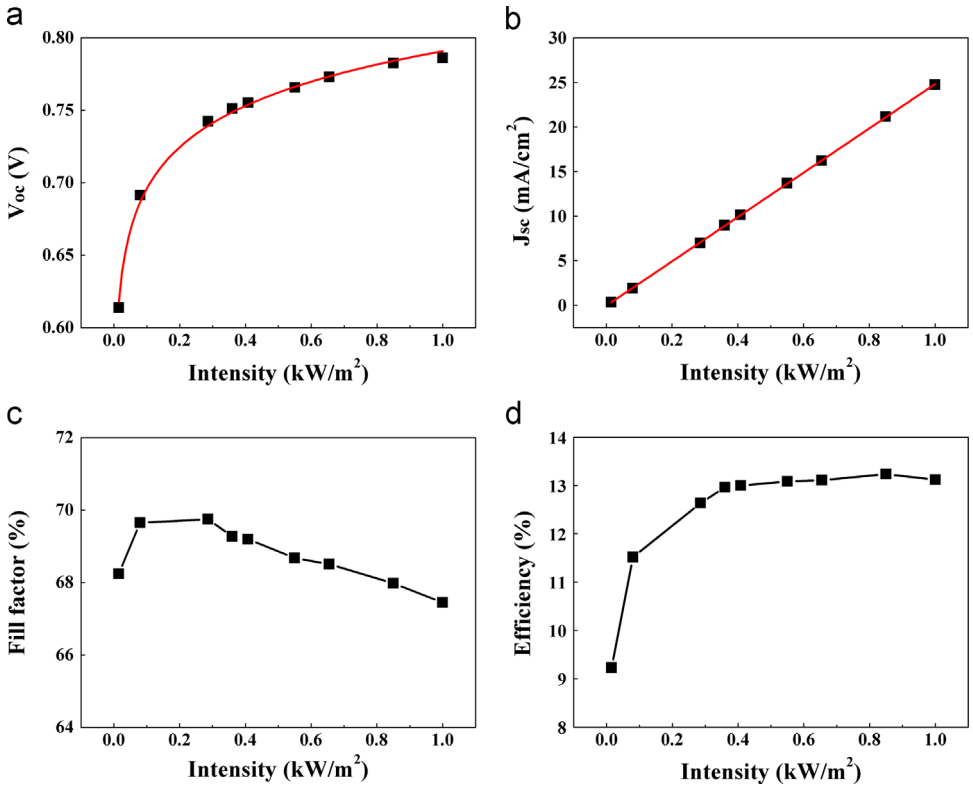

Fig. 3. CdTe solar cell performance measured under different light irradiance intensities. (a) Open-circuit voltage, (b) short-circuit current, (c) fill factor, and (d) cell efficiency versus the light intensity.

where J_0 is the reverse saturation current density of the solar cell diode, J_L and J are the photocurrent and the output current density, V is the output voltage, A is the ideality factor of the CdS/CdTe junction diode, q is the electron charge, k_B is Boltzmann's constant and T is the temperature. The series resistance R_s and shunt resistance R_p are lumped circuit model representations of the losses that occur in series and parallel with the primary diode, respectively. If R_s is negligibly small and R_p is very large, the short-circuit current density $J_{sc} \approx J_L$. The photocurrent density J_L is linearly proportional to the light intensity. Therefore, the short circuit current density J_{sc} under different light intensity can be described as the followings [17],

$$J_{SC} = J_{SC,STC}\frac{E_{irra}}{E_{irra,STC}} \tag{2}$$

where $J_{SC,STC}$ is the short circuit current density under STC, E_{irra} is the experimental light intensity, and $E_{irra,STC}$ is the light intensity under STC. At the open-circuit, $J=0$, when R_s is negligibly smaller than R_p, the open circuit voltage V_{oc}, obtained from Eq. (1) is [10],

$$V_{OC} = \frac{Ak_BT}{q}\ln\left(\frac{J_{SC}}{J_0}\right) \tag{3}$$

For a good quality junction diode, if A and J_0 are taken as constants or they don't vary much with the light irradiance intensity, the V_{oc} is then proportional to $\ln(J_{sc})$. Because the photocurrent $J_L \approx J_{sc}$ is proportional to the light intensity, the V_{oc} under different light intensity can be written as [17],

$$V_{OC} = V_{OC,STC} + \left(\frac{Ak_BT}{q}\right)\cdot \ln\left[\frac{E_{irra}}{E_{irra,STC}}\right] \tag{4}$$

where $V_{OC,STC}$ is the open circuit voltage under STC.

The short circuit current density J_{sc} was decreased linearly with the reduced light intensity, as shown in Fig. 3(b). The relationship between J_{sc} and light E_{irra} can be well fitted with a linear line with $J_{sc}=24.86\times[E_{irra}/E_{irra,STC}]-0.042$, which is in good agreement with

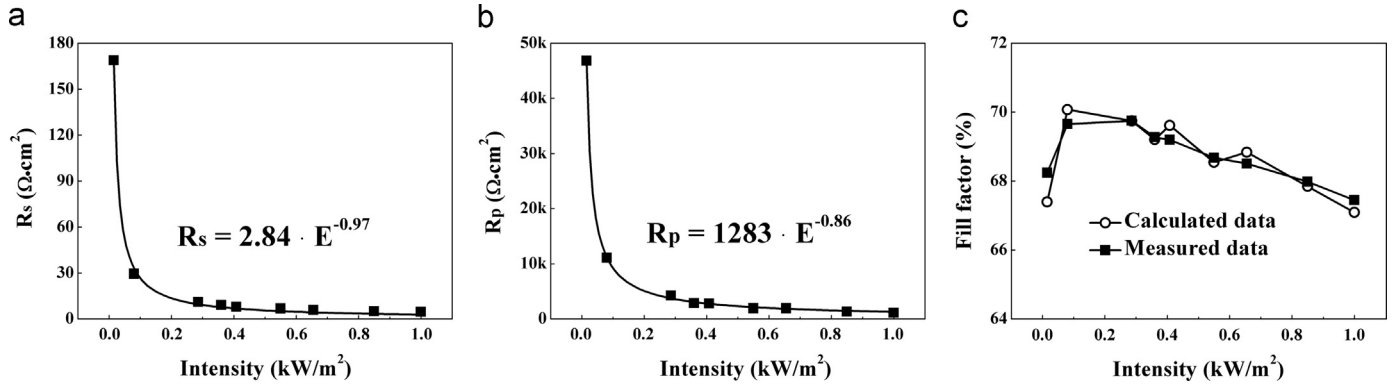

Fig. 4. (a) The series resistance R_s and (b) the shunt resistance R_p measured under different light intensities. The variations of the R_s and the R_p with the light intensity were fitted by power functions indicated in the figures, respectively. (c) The measured and the calculated fill factors versus the light intensity.

Eq. (2). The linear proportional relationship between J_{sc} and light intensity shows that the efficiency variation at low E_{irra} was not influenced by the J_{sc} as can be seen in the following. The V_{oc} variation upon decreasing E_{irra} was shown in Fig. 3(a). It was logarithmically decreased with light intensity and can be fitted to a relation, $V_{oc}=790.8+0.0414\times\ln[E_{irra}/E_{irra,STC}]$, also in good agreement with the relation, $V_{oc}=786.2+(Ak_BT/q)\times\ln[E_{irra}/E_{irra,STC}]$, according to Eq. (4). The ideality factor A deduced from the V_{oc} fitting is 1.6, the reverse saturation current density J_0 is 1.4×10^{-7} mA/cm^2. These values demonstrate that the CdTe solar cell has a high quality CdS/CdTe hetero junction and the junction current was dominated by the Shockley–Read–Hall recombination [14].

An important finding for the CdTe cell performance under weak light E_{irra} is that the fill factor was increased slightly from 67.5% to 69.8% with the irradiance E_{irra} from 1 down to 0.28 kW/m^2, as shown in Fig. 3(c). Because the J_{sc} was linearly changed with the light intensity, the variation of efficiency with E_{irra} mainly came from the changes of the V_{oc} and the fill factor (FF). The cell efficiency under different E_{irra} is shown in Fig. 3(d). It can be seen that even though the V_{oc} decreased logarithmically with E_{irra}, the efficiency of the solar cell remained almost unchanged from 1 down to 0.4 kW/m^2 and a slightly higher efficiency was achieved at 0.8 kW/m^2 compared to the efficiency at STC. Below the light intensity of 0.4 kW/m^2, the cell showed a significant efficiency decrease with the decreased E_{irra}.

The cell's efficiency was kept almost unchanged from 1 to 0.4 kW/m^2. This was mainly contributed from the increased fill factor, as shown in Fig. 3(c). The decreased V_{oc} upon decreasing E_{irra} was almost completely counteracted by the increased fill factor in the light intensity range of 1 down to 0.4 kW/m^2. To understand the device performance of a CdTe solar cell under weak light E_{irra}, the key is to study the factors which induced the change of FF. The fill factor depends on the series resistance R_s and shunt resistance R_p. The two resistances are actually the lumped parameters of the equivalent electric circuit model for a solar cell. Therefore they represent the "apparent" resistances. The impacts of R_s and R_p on the fill factor can be separately expressed by the following empirical expressions [6],

$$FF_0=\frac{v_{OC}-\ln(v_{OC}+0.72)}{v_{OC}+1} \tag{5}$$

$$FF_s=FF_0(1-r_s) \tag{6}$$

$$FF_p=FF_0\left[1-\frac{(v_{OC}+0.7)}{v_{OC}}\frac{FF_0}{r_p}\right] \tag{7}$$

$$FF=FF_0(1-r_s)\left(1-\frac{(v_{OC}+0.7)}{v_{OC}}\frac{FF_0(1-r_s)}{r_p}\right) \tag{8}$$

where $v_{OC}=V_{oc}/(Ak_BT/q)$, $r_s=R_s/(V_{oc}/I_{sc})$, $r_p=R_p/(V_{oc}/I_{sc})$. The R_s and R_p in this study were calculated from the line slope of the $J-V$ curves at the open-circuit voltage and short-circuit current points, respectively. The values of the R_s and the R_p obtained under different light intensities are shown in Fig. 4. Both the R_s and the R_p were increased almost in the same trend with the decreased E_{irra}. According to Eqs. (6) and (7), FF_s and FF_p decrease linearly and increase inversely with the increase of R_s and R_p, respectively. The variation of FF with E_{irra} results from the combined effect both from the R_s and the R_p, as can be seen in Eq. (8). When the light intensity was down from 1 to 0.2 kW/m^2, the increase of FF, shown in Fig. 3(c), mainly came from the increased value of the R_p. When the light intensity was lower than 0.2 kW/m^2, the decrease of FF mainly came from the increased R_s. Using Eq.(8) the FFs were calculated based on the values of R_s and R_p measured under different E_{irra}. The calculated FFs, shown in Fig. 4(c), agreed well with the measured data, confirming that the variation of FF mainly came from the increase of the R_s and the R_p with decreased E_{irra}.

p-type CdTe thin film prepared by the close-spaced sublimation technique is a high-resistivity semiconductor material [18]. In our lab the carrier concentration of thin CdTe films measured by CV profiling is 8.6×10^{13} cm^{-3}. Under light illumination the resistance of a semiconductor material decreases sharply due to the photon-generated carriers. The change of electrical resistance with the irradiance light intensity can be described by the following equation [19],

$$R=\gamma\cdot E_{irra}^{-\chi} \tag{9}$$

where γ is a constant, and χ is a parameter whose value depends on the specific material. The line in Fig. 4(a) shows the fitting of the R_s with the light intensity by a power function, $R_s=\gamma\times E_{irra}^{-0.97}$ with $\gamma=2.84$, which is in excellent agreement with Eq. (9). The carrier concentration of the CdTe thin film in this study is $\sim10^{14}$ cm^{-3}, while for the CdS window layer the n-type carrier concentration is 10^{16}–10^{17} cm^{-3}[20,21]. The CdS thickness employed in our cell fabrication was ~80 nm. It is far thinner than that of CdTe (~4 μm). Therefore the resistance of the CdS layer was neglected in the analysis in this study, and we suggest that under weak light irradiance the R_s was mainly contributed by the resistance of the CdTe absorber layer [10]. The R_p can also be well fitted by a power function, and $R_p=\gamma\times E_{irra}^{-0.86}$, with $\gamma=1283$, as shown in Fig. 4(b). With decreased E_{irra} both the R_s and the R_p were increased in the same way with light intensity. The changes of these two resistances were closely correlated with each other, indicating that the solar cell was well fabricated and the current shunting was closely related to the bulk resistivity of the CdTe layer for the cell worked under low E_{irra} if a CdTe solar cell was well fabricated. This can be made more clear in the following analysis by employing a comparative study of two CdTe solar cells with a high and a low shunt resistance.

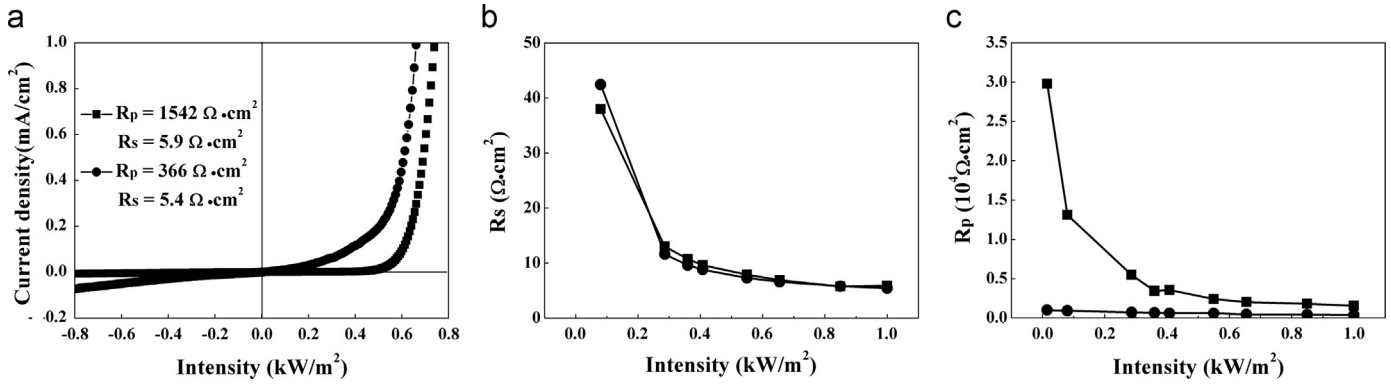

Fig. 5. (a) Dark $J-V$ curves of two CdTe solar cells with a high and a low shunt resistance. (b) The series resistance R_s and (c) the shunt resistance R_p of the two solar cells versus the light intensity.

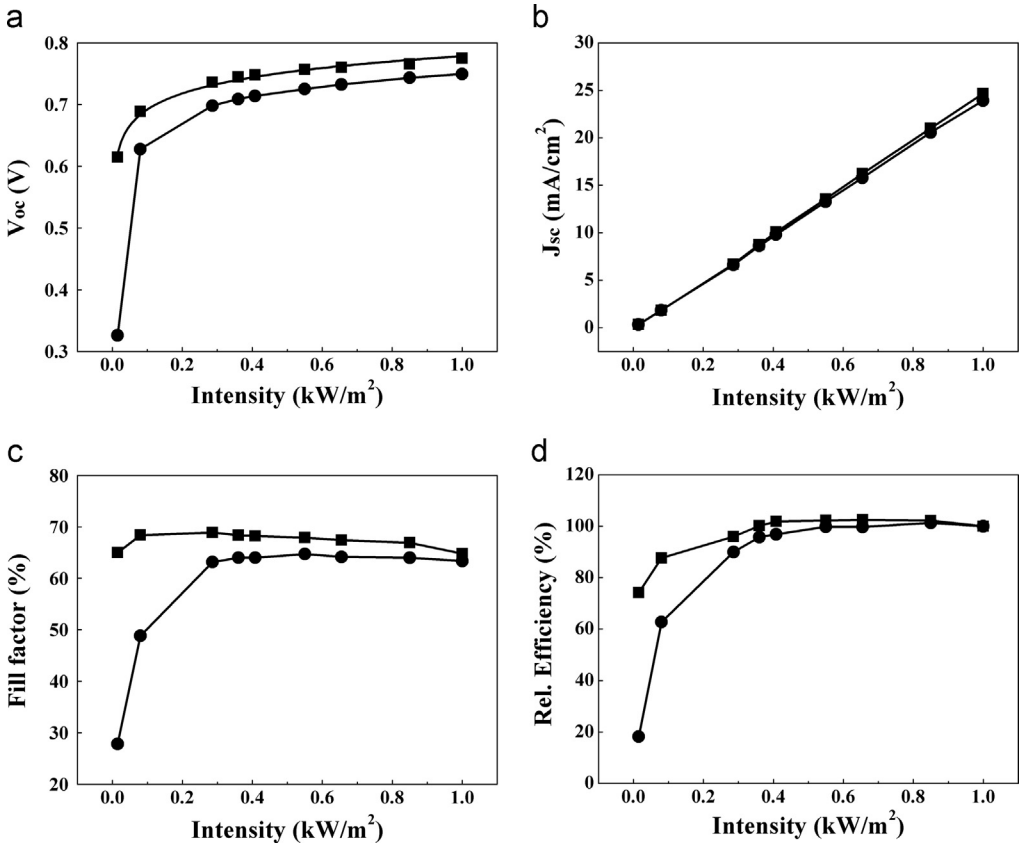

Fig. 6. Solar cell performances of two CdTe solar cells with a high and a low shunt resistance measured under different light irradiance intensities. (a) Open-circuit voltage, (b) short-circuit current, (c) fill factor, and (d) cell efficiency versus the light intensity.

3.2. Comparative study of device performances of two CdTe solar cells under weak light intensity

In order to have a comprehensive understanding of the influence of R_p on the weak light performance of a CdTe solar cell, we selected two solar cells with almost the same device performance tested at the STC. The efficiencies are 12.4% and 11.3%, the open-circuit voltages are 774.9 and 749.5 mV, the fill factors are 64.8% and 63.4%, the series resistance are 5.9 and 5.4 Ω cm^2, and the short circuit current densities are 24.7 and 23.9 mA/cm^2, respectively, for the two cells measured under STC. The only notable difference for these two cells is that they had much different values of R_p. We call these two cells the high-R_p and the low-R_p cells. The two cells had a high- and a low-R_p values of 1542 and 366 Ω cm^2, respectively. The dark $J-V$ curves for the two solar cells are shown in Fig. 5(a). Compared to the high-R_p solar cell, the low-R_p cell showed a much increased leakage current. The series resistances of the two cells increased almost in the same way with the decreased light intensity, as shown in Fig. 5(b). This provided an ideal case that the cell performances under low E_{irra} for these two cells can be analyzed without considering the influence of the series resistance R_s [8]. In the following we concentrate on the effect of the R_p on the device performance worked at low E_{irra}.

The increase of the two R_s shown in Fig. 5(b) was induced by the increased bulk resistance of the CdTe layers due to the decreased concentration of the photo-generated carrier. The change of R_p of the two cells with decreased E_{irra} showed a dramatic difference, as shown in Fig. 5(c). For the high-R_p cell, the device was well fabricated and the value of R_p measured at STC was relatively large. The R_p demonstrated a power-law increase with the decreased light

intensity as discussed above. For the low-R_p cell, the R_p measured at STC was relatively small, and the value demonstrated only slightly increased values even at very low light intensities. This is totally different from that of the high-R_p cell. The physical basis for these observations will be discussed in the following.

It has been reported that the solar cell performance under weak light performance depends critically on the shunt resistance R_p [6–9]. Fig. 6 shows the comparative device performance of the two cells with a high and a low R_p resistance. The short-circuit currents of the two cells were almost the same and decreased linearly with the decreased light intensity, see Fig. 6(b). The values of the V_{oc} and the FF of both cells changed with decreased light intensity with almost the same way from 1 down to 0.4 kW/m^2 irradiance intensity, see Fig. 6(a) and (c). Below a light intensity of 0.4 kW/m^2, both the V_{oc} and the FF of the low-R_p cell decreased sharply with the decreased E_{irra}, leading to much decreased cell efficiencies, see Fig. 6 (d). For the high-R_p cell at an E_{irra} of 0.015 sun, its efficiency still kept at a value of 9.2%, namely, ~74% of the efficiency was remained at the level of that measured under STC. But for the low-R_p cell, the V_{oc} and the efficiency were decreased to values of only 326.1 mV and 2.1%. The FF was also dramatically decreased from 63.4% to 27.8%. The much worsened device performance under low E_{irra} was caused by the electric current shunting in the low-R_p cell, which will be analyzed in details in the following paragraphs.

3.3. Compact electric circuit models and electric shunting path fittings to the experimental data

Shunt current depends sensitively on the solar cell fabrication technologies, cell types and the microstructure of cell devices [2,7]. Variations of the shunt resistance under weak E_{irra} would critically depend on the physical location and the electrical conductivity of the shunting paths. The *J–V* characteristics of a solar cell can be analyzed by an equivalent compact electric circuit model based on the superposition of a photocurrent source on the characteristics of the cell dark diode. The dark diode in the one-exponential electric circuit model for a solar cell consists of a diode shunting, the series and parallel shunt resistances. For a non-ideal solar cell, especially for thin film solar cells, in addition to these shunting components, other shunting paths/mechanisms must be considered to fit/explain the experimental data [22,23]. In order to make clear how and where the shunting paths influenced the device performance under weak light intensity, in this study, different compact electric circuit models were developed to analyze the dark *J–V* characteristics of the two cell devices. Fig. 7(a) schematically shows the electric transport paths presented in a polycrystalline thin film CdTe solar cell. The compact electric circuit for a standard solar cell is composed of a photocurrent I_L, a p–n junction diode, lumped shunt and series resistances. For a thin film CdTe solar cell, which is made of polycrystalline p-type CdTe and n-type CdS thin films, micro-scale weak diodes could be easily formed through inhomogeneous interdiffusion or reaction at the CdTe/CdS interface [12,24]. Our study showed that micro-scale weak diodes played an important role as an efficient shunting path in low-R_p cells, as can be seen from the following discussions. Another possible shunting path considered in this study is the space-charge limited current (SCLC). In a solar cell, SCLC can be induced by the unbalanced charge transport between photo-generated holes and electrons [25,26]. SCLC has been reported in some kinds of solar cells, such as inorganic Si and $CuIn_xGa_{1-x}Se_2$, and organic solar cells [22,27]. CdTe is a high-resistivity semiconductor material with a resistivity of ~10^4 Ω cm. The hole mobility in CdTe is ~40 cm^2 V^{-1} s^{-1} and the electron mobility is much higher ~320 cm^2 V^{-1} s^{-1} at 300 K [28]. The charge transport in CdTe is supposed to be strongly unbalanced. SCLC effect should be taken into consideration in analyzing the

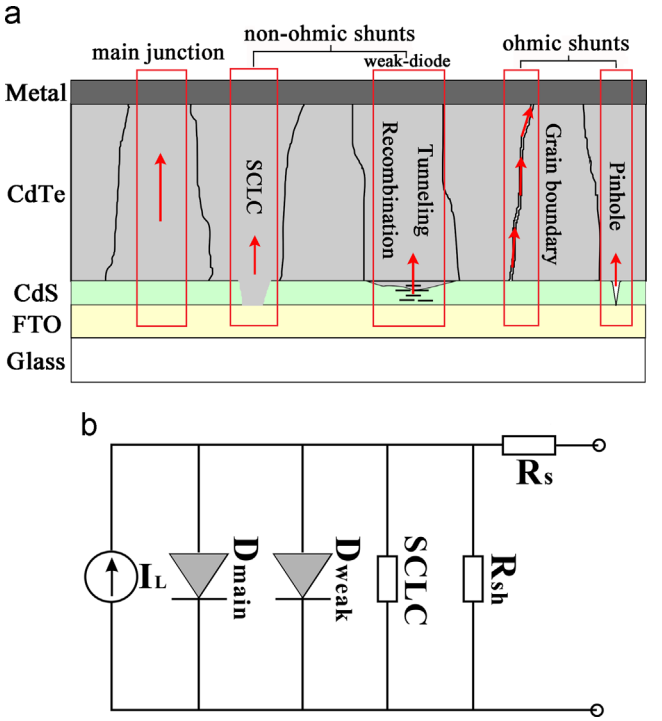

Fig. 7. (a) Schematic diagram of the electric shunting paths presented in a polycrystalline thin film CdTe solar cell; (b) equivalent compact electric circuit model for a CdTe thin film solar cell.

shunting paths in CdTe solar cells [29,30]. Our model and the data fittings in this study strongly support this suggestion.

According to the discussions above, the equivalent compact electric circuit for a thin film CdTe solar cell can be modeled by including an ideal diode (the main diode) and 3 shunting contributions, two non-ohmic shunting paths represented by a weak diode and a SCLC, and one ohmic shunting path represented by R_{sh}, as shown in Fig. 7(b). The weak diode represents an exponential contribution to the shunting current and is described by a similar mathematical term as that of the main diode, but with much different diode parameters. According to the equivalent circuit model, the total dark current density J_D of a cell device can be expressed as in the following [23],

$$J_D = J_{01}(e^{q(V-J_DR_S)/A_1k_BT}-1)+J_{02}(e^{q(V-J_DR_S)/A_2k_BT}-1) + K(V-J_DR_S)^m+(V-J_DR_S)/R_{sh} \quad (10)$$

The first term $J_{01}(e^{q(V-J_DR_S)/A_1k_BT}-1)$ represents the main diode junction. The term $J_{02}(e^{q(V-J_DR_S)/A_2k_BT}-1)$ represents the weak-diode which is responsible for the electronic current contributed from shorting current, recombination and tunneling processes. J_{01} and J_{02} are the reverse saturation current densities, V is the output voltage, A_1 and A_2 are the idealilty factors for the two diodes, R_s is the lumped ohmic series resistance. The term $K(V-J_DR_S)^m$ represents the space-charge limited current, where K is related to the film thickness, trap distribution, and conductivity of the transport path. m is related to the density of states of the transport path, $m=2$ for a SCLC without traps and $m>2$ with traps [26]. The $(V-J_DR_S)/R_{sh}$ represents the ohmic shunting current, which is mainly caused by pinholes at the CdS/CdTe interface and by the conductivity at the grain boundaries in a polycrystalline CdTe thin film. In this study, in order to reduce the light absorption in a CdS window layer, the CdS thickness was controlled to be ~80 nm. When the thickness of a window CdS layer is several tens of nanometers, the so called pinhole can be almost unavoidably formed at the CdS/CdTe interface [31,32]. Because of the small thickness part of the CdS layer could be totally reacted with CdTe

during the deposition of a CdTe absorber layer and/or during the $CdCl_2$ thermal activation process, leading to direct contact of CdTe with the front FTO electrode.

Fig. 8 shows the experimental dark *J–V* data and the curve fittings, which accounted for the different contributions induced by the shunting paths discussed above. For the high-R_p cell, the main shunting paths are the ohmic shunting and the SCLC. The shunting contribution from the SCLC increased to the same level as that induced by the ohmic shunting at voltages of $\sim \pm 0.8$ V. It can be clearly seen from the fittings that the current above the voltage of $\sim$0.5 V was mainly contributed by the main diode due to the forward bias carrier injection at the CdS/CdTe junction. The level off of the experimental $J-V$ curves in Fig. 8(a) and (b) at voltage higher than $\sim$0.7 V was induced by the voltage drop on the series resistance R_s. In the reverse and forward voltage with an absolute voltage value smaller than $\sim$0.7 V, the dark current was relatively low and so was the value of $J_D \times R_s$. The series resistance R_s had little effect on the curve fitting and the data analysis. At high forward voltage with a value larger than $\sim$0.7 V, the R_s is not a constant value because of the Schottky barrier at the back contact, and the voltage drop on the R_s could not be ignored anymore. In the data fittings we ignored the effect of R_s and it can be seen that the fitting and the experimental data are perfectly matched when voltage is smaller than $\sim$0.7 V. The mismatch at forward voltage larger than $\sim$0.7 V was induced by the voltage drop on the R_s. For the high-R_p cell, the shunting current caused by a weak-diode can be ignored. Including the effect of a weak-diode, the experimental data would be overestimated at the voltage range of $0-0.5$ V, as shown in Fig. 9(e). This is not the case for the low-R_p cell, as can be seen in the Figs. 8(b) and 9(f). For the low-R_p cell the main shunting paths came from three mechanisms, namely, the ohmic shunt resistance R_{sh}, the SCLC, and the weak diode. It should be noted that at the forward bias, the shunting current was dominated by the weak diode at the voltage range of $0-0.5$ V. From the fittings of the dark *J–V* curves we can recognize four different voltage regions in which the current shunting was dominated by different physical processes. The first region is for $V<-0.5$ V, the dark current was mainly contributed by the SCLC and the ohmic shunt resistance R_{sh}. The second region is from -0.5 to 0.4 V, for the high-R_p cell, the dark current was mainly determined by the ohmic shunt resistance R_{sh}; for the low-R_p cell, the dark current was controlled by the combined effect of both the ohmic shunt resistance R_{sh} and the weak diode. The third region is from 0.4 to 0.7 V, for the high-R_p cell, the dark current was dominated by the main junction; and for the low-R_p cell, in addition to the main junction, the dark current was significantly contributed by the weak diode. For the fourth region of $V>0.7$ V, for the high-R_p cell the dark current was mainly limited by the series resistance, and for the low-R_p cell, the current was also affected by the weak diode. From the above discussions, it can be clearly seen that compared with the high-R_p cell, the main difference for the shunting paths in the low-R_p cell was the existence of the weak diode, which had significant effect in nearly all the voltage regions in the *J–V* curve.

The parameters of the equivalent electric circuit models can be extracted from the fittings discussed above, and they are listed in Table 1. For the high-R_p cell, the ohmic shunt resistance R_{sh} obtained by the fitting is $2.2\times10^5\ \Omega\ cm^2$, which is high enough to guarantee good device performance for a CdTe solar cell worked under low light intensity irradiance. Studies have shown that a shunt resistance higher than $\sim10^4\ \Omega\ cm^2$ is required for a $CuIn_xGa_{1-x}Se_2$ solar cell to perform well under low light intensity irradiance, especially for light intensity lower than 10 W/m^2 [9]. The reverse saturation current density $J_{01}=9.5\times10^{-7}$ mA/cm^2 for the high-R_p cell is relatively low, indicating that the main junction had an excellent diode characteristics. The diode ideality factor A_1 is 1.7, indicating that the junction current was dominated by the Shockley–Read–Hall recombination. The ideality factor A_1 value of 1.7 obtained by the fitting in Fig. 8 is in excellent agreement with that of a value of 1.6 obtained by the light $J-V$ curves discussed above. The SCLC parameters $K=1.1\times10^{-6}$ and $m=2.8$ are related to the characteristics of the charge-transport path. $m>2$ indicates that the trap states are distributed in energy below the conduction band [26]. For the low-R_p cell, the value of $J_{02}=1.1\times10^{-3}$ mA/cm^2 is about 3 orders of magnitude larger than that of the main diode, indicating that the weak diode played an essential role in the electric shunting of the device.

One of the important findings of this study is that space-charge limited current played an important role in the electric current shunting in a CdTe thin film solar cell. In order to identify the contributions from different shunting paths, we employed different equivalent compact electric circuit models to fit the dark $J-V$ curves, as shown in Fig. 9. The different electric circuit models and the corresponding fittings to the dark $J-V$ curves are shown in the same figures. The fitting curves for the high-R_p and low-R_p cells using the standard model, namely, a main diode with ohmic shunt resistance R_{sh} and series resistance R_s, didn't fit the experimental data, as shown in Fig. 9(a) and (b). For the high-R_p cell, a modified model by considering the effect of SCLC fitted the experimental data very well, confirming that the SCLC played an important role in the current shunting, especially in the reverse voltage region. For the low-R_p cell, the modified model by including the SCLC was not enough, as shown in Fig. 9(d). There was a big mismatch between the experimental and the fitting data in the voltage region from 0 to 0.7 V for the model shown as the inset in Fig. 9(d). The shunting current induced by a weak diode needed to be included for the low-R_p cell, as shown in Fig. 9(f). The inclusion of a weak diode for the high-R_p cell was not necessary. The fitting

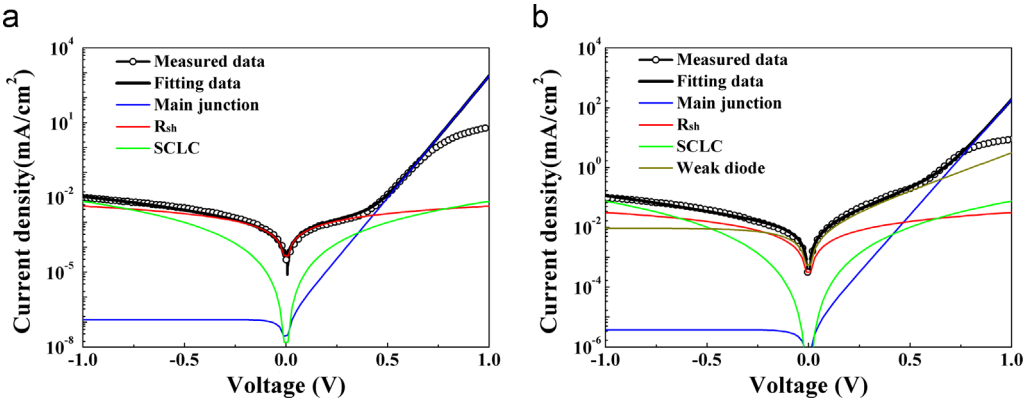

Fig. 8. Experimental dark current–voltage data and the fitting curves from the contributions of different shunting paths for (a) the high-R_p and (b) the low-R_p CdTe solar cells.

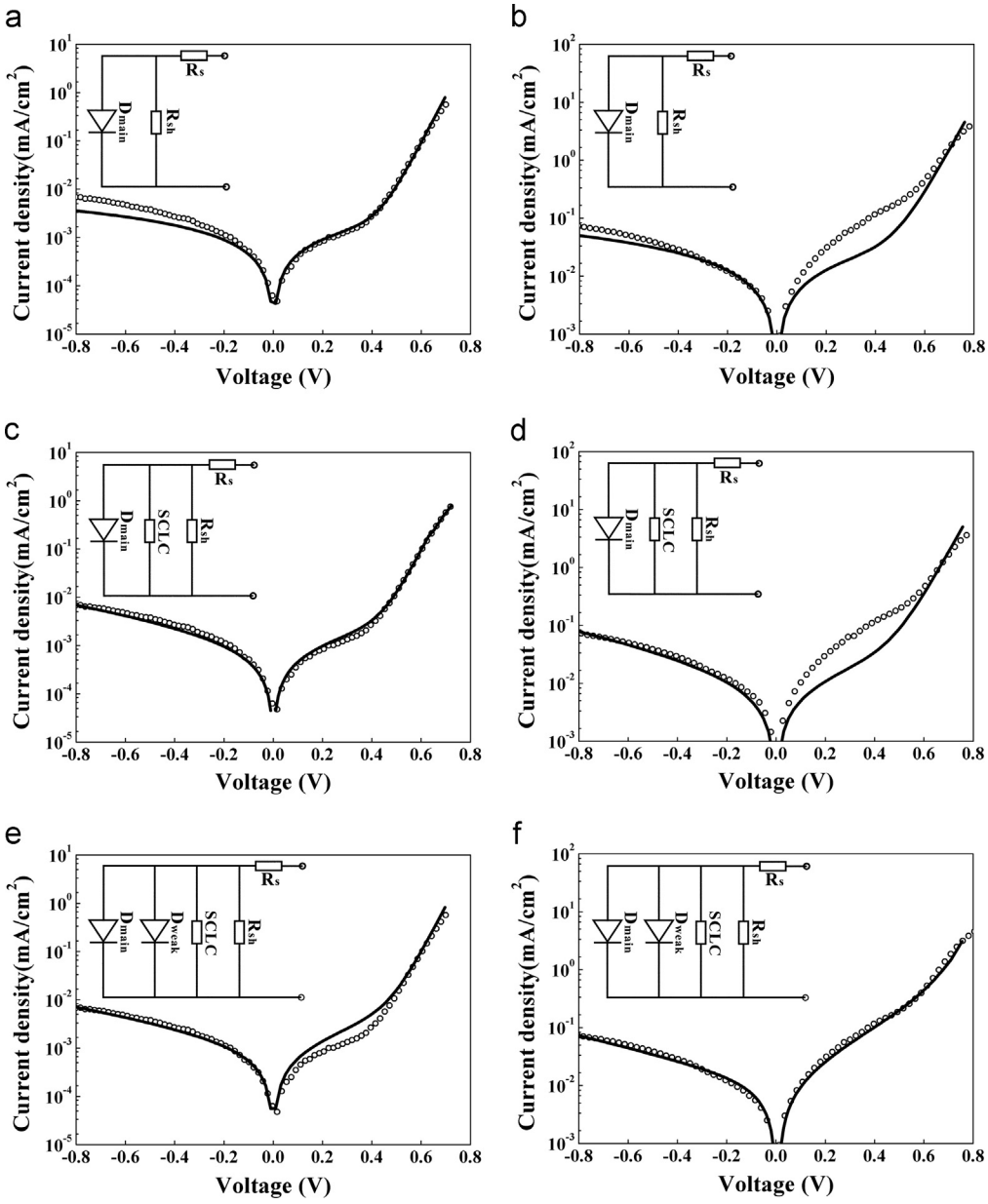

Fig. 9. The experimental dark current-voltage data (symbols) and fitting curves of (a), (c), and (e) for the high-R_p solar cell, and (b), (d), and (f) for the low-R_p solar cell. The equivalent electric circuit models are shown as the insets in the corresponding figures.

Table 1
Parameters of the equivalent electric compact models for the high-R_p and the low-R_p CdTe solar cells extracted from the experimental data fittings.

Device	J_{01} (mA/cm^2)	A_1	J_{02} (mA/cm^2)	A_2	K	m	R_{sh} (Ω cm^2)
High-R_p cell	9.5×10^{-7}	1.7	0	0	1.1×10^{-6}	2.8	2.2×10^{5}
Low-R_p cell	3.8×10^{-6}	2.2	1.1×10^{-3}	6.6	1.2×10^{-5}	2.9	3.2×10^{4}

data were overestimated by including the effect of a weak diode in the voltage range of 0 – 0.5 V for the high-R_p cell, as shown in Fig. 9(e). The series fittings of the different models clearly demonstrate that the SCLC is an important shunting mechanism for a thin CdTe solar cell. For a low-R_p cell, weak diode played a significant role in the current shunting.

The ohmic shunting path was mainly induced by the presence of pinholes found at the CdS/CdTe interface and by the conducting grain boundaries in the CdTe absorber layer. The ohmic shunt resistance is therefore highly dependent on the bulk resistivity of the CdTe layer. The increased R_p for the high-R_p cell, which was well described by Eq. (9), indicates that the current shunting induced by weak diode is not necessary to be considered in the model fitting. Different from the ohmic shunting path, the shunt effect related to the weak diode and the SCLC were less dependent on the bulk resistivity of CdTe. This resulted in the almost unchanged values of the R_p for the low-R_p cell with decreased light intensity, as shown in Fig. 5(c). The increased shunt resistance with decreased light irradiance intensity is essential for a solar cell to maintain good device performance at low light irradiance intensity. Under low-intensity light irradiation, the photocurrent becomes very low, and its value is comparable to the shunting current. The relatively high loss of current will greatly reduce the values of the output voltage and the fill factor of a low-R_p cell device.

4. Conclusions

In summary, CdTe thin film solar cell performance under weak light intensities was studied. The experimental results presented in this study demonstrated that polycrystalline CdTe thin film solar cell is intrinsically suitable for electric power generation at weak light-intensity irradiance. For a well fabricated CdTe solar cell with a high shunt resistance, the cell efficiency at an E_{irra} as low as 0.015 Sun maintained a value of ~70 to 80% of that tested at the STC condition. The open-circuit voltage and the fill factor of a CdTe solar cell were critically depended on the shunting paths/mechanisms. Different types of shunting paths are suggested to be responsible for the deteriorated cell performance at low E_{irra}. Space-charge limited current was identified to be an important contribution to the shunting current due to the thin film stacking structure. For CdTe solar cells with relatively low shunt resistances, the cell performance deteriorated dramatically with decreased light intensity. This was attributed to the presence of weak diode in the cell structure. This study provides constructive guidelines for the future design and fabrication of CdTe solar cells.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (Nos. 51272247, 61474103) and Natural Science Foundation of Anhui Province (No. 1408085MF119).

References

[1] M. Green, K. Emery, Y. Hishikawa, W. Warta, E. Dunlop, Solar cell efficiency tables (Version 46), Prog. Photovolt.: Res. Appl. 23 (2015) 805–812.
[2] J. Randall, J. Jacot, Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra, Renew. Energy 28 (2003) 1851–1864.
[3] J. Randall, C. Droz, M. Goetz, A. Shah, J. Jacot, Comparison of 6 photovoltaic materials across 4 orders of magnitude of intensity, in: the proceedings of 17th European Photovoltaic Solar Energy Conference, Munich, vol.3, 2001, pp. 603–606.
[4] A. Shah, H. Schade, M. Vanecek, J. Meier, E. Vallat-Sauvain, N. Wyrsch, U. Kroll1, C. Droz, J. Bailat, Thin-film silicon solar cell technology, Prog. Photovolt.: Res. Appl. 12 (2004) 113–142.
[5] M. Simon, E. Meyer, Detection and analysis of hot-spot formation in solar cells, Sol. Energy Mater. Sol. Cells 94 (2010) 106–113.
[6] N. Reich, W. Sark, E. Alsema, R. Lof, R. Schropp, W. Sinke, W. Turkenburg, Crystalline silicon cell performance at low light intensities, Sol. Energy Mater. Sol. Cells 93 (2009) 1471–1481.
[7] N. Reich, W. Sark, E. Alsema, S. Kan, S. Silvester, A. van der Heide, R. Lof, R. Schropp, Weak light performance and spectral response of different solar cell types, in: the proceedings of 20th European Solar Energy Conference and Exhibition, Barcelona, 2005.
[8] P. Grunow, S. Lust, D. Sauter, V. Hoffmann, C. Beneking, B. Litzenburger, L. Podlowski, Weak light performance and annual yields of pv modules and systems as a result of the basic parameter set of industrial solar cells, in: the proceedings of 19th European Photovoltaic Solar Energy Conference, Paris, 2004, pp. 2190–2193.
[9] A. Virtuani, E. Lotter, M. Powalla, U. Rau, J. Werner, Highly resistive Cu(In,Ga)Se_2 absorbers for improved low-irradiance performance of thin-film solar cells, Thin Solid Films 451–452 (2004) 160–165.
[10] W. Li, R. Yang, D. Wang, CdTe solar cell performance under high-intensity light irradiance, Sol. Energy Mater. Sol. Cells 123 (2014) 249–254.
[11] D. Bätzner, A. Romeo, H. Zogg, A. Tiwari, CdTe/CdS solar cell performance under low irradiance, in: 17th European Photovoltaic Solar Energy Conference, Munich, 2001, VB 1.40.
[12] D. Wang, Z. Hou, Z. Bai, Study of interdiffusion reaction at the CdS/CdTe interface, J. Mater. Res. **26** (2011) 697–705.
[13] Z. Bai, J. Yang, D. Wang, Thin film CdTe solar cell with an absorber layer thickness in micro- and sub-micrometer scale, Appl. Phys. Lett. 99 (2011) 143502.
[14] R. Yang, D. Wang, L. Wan, D. Wang, High-efficiency CdTe thin-film solar cell with a mono-grained CdS window layer, RSC Adv. 4 (2014) 22162–22171.
[15] S. Demtsu, J. Sites, D. Albin, Role of copper in the performance of CdS/CdTe solar cells, in: the proceedings of IEEE 4th World Conference on Photovolatic Energy Conversion, Hawaii, 2006, NREL/CP-520-39923.
[16] S. Hegedus, W. Shafarman, Thin-film solar cells: device measurements and analysis, Prog. Photovolt.: Res. Appl. 12 (2004) 155–176.
[17] H. Yu, Q. Yue, J. Zhou, W. Wang, A hybrid indoor ambient light and vibration energy harvester for wireless sensor nodes, Sensors 14 (2014) 8740–8755.
[18] K. Biswas, M. Du, What causes high resistivity in CdTe, New J. Phys. 14 (2012) 063020.
[19] M. Satyam, K. Ramkumar, Foundations of Electronic Devices, New Age International (P) Ltd., New Delhi, 1990.
[20] J. Britt, C. Ferekides, Thin-film CdS/CdTe solar cell with 15.8% efficiency, Appl. Phys. Lett. 62 (1993) 2851–2852.
[21] J. Lee, J. Yi, K. Yang, J. Park, R. Oh, Electrical and optical properties of boron doped CdS thin films prepared by chemical bath deposition, Thin Solid Films 431–432 (2003) 344–348.
[22] J. Pallarès, R. Cabré, L. Marsal, A compact equivalent circuit for the dark current–voltage characteristics of nonideal solar cells, J. Appl. Phys. 100 (2006) 084513.
[23] B. Williams, S. Smit, B. Kniknie, N. Bakker, W. Kessels, R. Schropp, M. Creatore, Identifying parasitic current pathways in CIGS solar cells by modelling dark JV response, in: 40th IEEE Photovoltaic Specialist Conference, Denver, 2014, pp. 1729–1734.
[24] V.G. Karpov, A.D. Compaan, Diana Shvydka, Effects of nonuniformity in thin-film photovoltaics, Appl. Phys. Lett. 80 (2002) 4256.
[25] V. Mihailetchi, J. Wildeman, P. Blom, Space-charge limited photocurrent, Phys. Rev. Lett. 94 (2005) 126602.
[26] A. Rose, Space-charge-limited currents in solids, Phys. Rev. 97 (1954) 1538–1544.
[27] S. Dongaonkar, J.D. Servaites, G.M. Ford, S. Loser, J. Moore, R.M. Gelfand, H. Mohseni, H.W. Hillhouse, R. Agrawal, M.A. Ratner, T.J. Marks, M. S. Lundstrom, M.A. Alam, Universality of non-Ohmic shunt leakage in thin-film solar cells, J. Appl. Phys. 108 (2010) 124509.
[28] M. Gloeckler, A.L. Fahrenbruch, J.R. Sites, Numerical modeling of CIGS and CdTe solar cells setting the baseline, in: 3rd World Conference on Photovolraic Energy Conversion, Osaka, 2003, pp. 491–494.
[29] R.D. Gould, B.B. Ismail, Space-charge-limited conductivity and mobility measurements in cadmium telluride thin films, Int. J. Electron. 69 (1990) 19–24.
[30] X. Mathew, J.P. Enriquez, P.J. Sebastian, M. Pattabi, A. Sanchez-Juarez, J. Campos, J.C. McClure, V.P. Singh, Charge transport mechanism in a typical Au/CdTe Schottky diode, Sol. Energy Mater. Sol. Cells 63 (2000) 355–365.
[31] B. McCandless, K. Dobson, Processing options for CdTe thin film solar cells, Sol. Energy 77 (2004) 839–856.
[32] A. Bosio, N. Romeo, S. Mazzamuto, V. Canevari, Polycrystalline CdTe thin films for photovoltaic applications, Prog. Cryst. Growth Charact. Mater. 52 (2006) 247–279.