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Effect of quantum confinement on the defect-induced localized levels in 4H-SiC(0001)/SiO_2 systems

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ABSTRACT

In the present study, we characterize the nature of interface states in silicon carbide (SiC) metal–oxide–semiconductor (MOS) systems by analyzing the electrical characteristics of MOS field effect transistors (MOSFETs) based on the results of numerical calculations. In the calculation, the potential distributions and energy sub-bands were calculated by solving Poisson and Schrödinger equations, respectively. As a result, we demonstrate that the defect-induced localized levels in the bandgap are subjected to quantum confinement at the inversion layer, leading to the increase in their energy levels. The result implies that the conventional interface defects (e.g., near-interface oxide traps), which create defect states at certain energy levels measured from the vacuum level, are unlikely to be the major origin of the interface states in SiC MOS systems. The interface state density is almost uniquely determined by the oxide formation process (as oxidation or interface nitridation) and independent of the acceptor concentration (3×10^{15}–1×10^{18} cm^{-3}). It is also suggested that the drain current decrease observed in heavily doped MOSFETs is mainly due to the decrease in the drift mobility rather than that in the free carrier density.

I. INTRODUCTION

The interface between a semiconductor and its oxide plays an important role in nanoscience and technology. An example that has been studied intensively is the interface of silicon carbide (SiC) and silicon dioxide (SiO_2). SiC is a compound semiconductor having unique physical properties for power device applications, such as a wide bandgap and a high breakdown electric field.[1,2] Thus, SiC metal–oxide–semiconductor field effect transistors (MOSFETs) have been attracting increasing attention as low-loss and high-frequency power switching devices. SiC MOSFETs have, however, suffered from low channel mobility due to the high interface state density (D_{it}) in SiO_2/SiC structures ($\sim 10^{13}$ cm^{-2} eV^{-1}).[3–14] Although it was found that interface nitridation [annealing in nitric oxide (NO)[15–18] or nitrous oxide (N_2O)[15,19,20]] or phosphorus treatment [annealing in a gas mixture of phosphoryl chloride ($POCl_3$), oxygen (O_2), and nitrogen (N_2)][21,22] can reduce the D_{it} and improve the channel mobility to some extent, the physical origin of the abnormally high interface state density is still not understood.

In previous studies, it was indicated that the D_{it} values rapidly increase with approaching the conduction band edge (E_C).[9,23] Thus, determination of the D_{it} in the shallow energy range near E_C ($E_C - E_T < 0.2$ eV) is particularly important in understanding the nature of the interface states. However, few reports have focused on the D_{it} distributions in the vicinity of E_C ($E_C - E_T < 0.2$ eV) so far, since they cannot be simply estimated from capacitance–voltage (C–V) characteristics of MOS capacitors;[24] a study using MOS-Hall effect and split C–V measurements indicated that the D_{it} values near E_C are reduced with interface nitridation.[9] A more recent study has suggested the possibility that the interface states originate from the *tail* of two-dimensional density of states (2D-DOS) of SiC by characterizing wet-oxidized MOSFETs at cryogenic temperatures.[25] In order to understand the nature of interface states, however, a more systematic study involving MOS structures with various acceptor densities and oxide formation conditions is demanded.

In this study, we determined the D_{it} distributions for SiC MOS structures in the vicinity of E_C by reproducing the experimental gate characteristics of MOSFETs with numerical calculations. In the calculations, potential distributions and energy sub-bands in the inversion layer were calculated by solving Poisson and

Schrödinger equations, respectively. We prepared MOSFETs with various acceptor densities and oxidation formation conditions to discuss their impacts on the interface properties. The limiting factors of drain current in SiC MOSFETs are also discussed based on the results.

II. SAMPLE PREPARATION

MOSFETs were fabricated on 8° off-axis p-type (acceptor density: $N_A = 3 \times 10^{15}$–1×10^{18} cm^{-3}) 4H-SiC (0001) epilayers. The p-type body regions of MOSFETs were formed either by epitaxial growth ($N_A = 3 \times 10^{15}$ cm^{-3}) or by aluminum (Al) implantation ($N_A = 3 \times 10^{16}$–1×10^{18} cm^{-3}). The Al implantation was performed at room temperature (RT) to form a 0.6 μm-deep box profile (implant energy: 25–300 keV, total dose: 1×10^{12}–1×10^{14} cm^{-2}). The source/drain regions were formed by high-dose phosphorus (P) implantation ($N_D = 1 \times 10^{20}$ cm^{-3}) to obtain good ohmic contacts. The P implantation was performed at 300 °C (implant energy: 10–180 keV, total dose: 2×10^{15} cm^{-2}). After ion implantations, the surface was covered with a carbon cap, and dopant activation annealing was performed at 1650 °C for 20 min in an argon (Ar) atmosphere. The gate oxides were formed by dry oxidation at 1300 °C for 30 min (As-Ox.) or by dry oxidation with subsequent annealing in NO [10% diluted in nitrogen (N_2)] at 1250 °C for 70 min (Ox. + NO), resulting in an oxide thickness of about 42 nm. Note that we also prepared n-type 4H-SiC (0001)/SiO_2 structures as reference samples to determine the resulting oxide thickness for each oxidation and annealing condition (i.e., As-Ox. and Ox. + NO). The oxide thickness was then measured by using spectroscopic ellipsometry. The channel length and width of the MOSFETs were 50 or 100 μm and 200 μm, respectively. All of the measurements were conducted at room temperature (RT).

III. CALCULATION MODEL

Figure 1 shows a schematic illustration describing the concept of the model to extract the D_{it} distribution from the gate characteristics of MOSFETs.[26] In this model, it is assumed that the electrons in the inversion layer contribute to the conduction with constant drift mobility and that the electrons trapped at the interface states are completely immobile. In general, the drain current (I_D) and the gate voltage (V_G) are expressed as a function of the surface potential (ψ_S) by[27]

$$I_D(\psi_S) = \frac{W}{L} e n_{free}(\psi_S) \mu_{drift}(\psi_S) V_D, \tag{1}$$

$$V_G(\psi_S) = V_{FB} + \psi_S + \frac{-Q_{fix} + eN_A z_{dep} + en_{free}(\psi_S) + en_{trap}(\psi_S)}{C_{ox}}. \tag{2}$$

Here, W is the channel width, L is the channel length, e is the elementary charge, μ_{drift} is the drift mobility, n_{free} is the density of free electrons in the channel, n_{trap} is that of trapped electrons, V_D is the drain voltage, V_{FB} is the flatband voltage, Q_{fix} is the fixed charge, z_{dep} is the depletion width, and C_{ox} is the oxide capacitance.

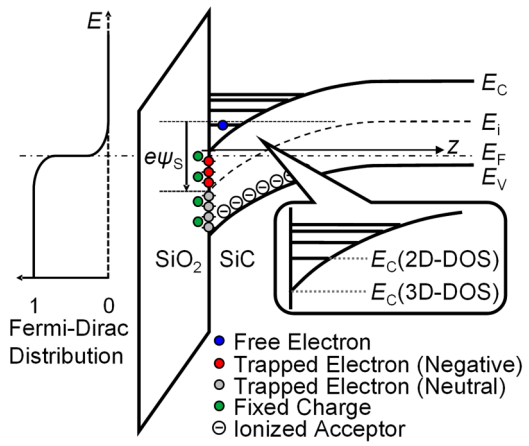

FIG. 1. Concept of a calculation model for extracting interface state density (D_{it}) distributions from gate characteristics of SiC MOSFETs. E_C, E_i, E_F, E_V, and ψ_S indicate the conduction band edge, the intrinsic level, the Fermi level, the valence band edge, and the surface potential of SiC, respectively.

In using the model above, we assumed constant μ_{drift} of 100, 35, 25, 15, and 5 cm^2 V^{-1} s^{-1} for MOSFETs with N_A of 3×10^{15}, 3×10^{16}, 1×10^{17}, 3×10^{17}, and 1×10^{18} cm^{-3}, respectively, regardless of the oxide formation conditions (As-Ox. or Ox. + NO), based on the reported values of Hall mobility for NO-annealed MOSFETs.[28] Indeed, Ref. 9 indicated that the difference in the Hall mobility between as-oxidized and NO-annealed MOSFETs is considerably small (e.g., about 160 and 140–180 cm^2 V^{-1} s^{-1} at $n_{free} = 10^{11}$ cm^{-2} for as-oxidized and NO-annealed MOSFETs, respectively), making such assumption reasonable.

To take account of the quantum effects (e.g., energy quantization) in the inversion layer[29,30] accurately, it is necessary to solve the Schrödinger and Poisson equations self consistently. By numerically solving the Schrödinger and Poisson equations with setting n_{free} and N_A as initial values such as 1×10^{12} cm^{-2} and 3×10^{15} cm^{-3}, respectively, E_F, ψ_S, and the energy level of the first sub-band of 2D-DOS were determined.[29,31] Then, by assuming a triangle-shaped potential [$\varphi(z)$] at the MOS interface, we obtained the initial values of $\varphi(z)$. As the next step, we solved the Schrödinger equation with the effective mass approximation, that is,[29]

$$\left[-\frac{\hbar^2}{2m^*_{c\parallel}} \frac{d^2}{dz^2} - e\varphi(z) \right] \xi_i(z) = \epsilon_i \xi_i(z), \tag{3}$$

where $\hbar$ is the Dirac constant, $m^*_{c\parallel}$ is the effective mass parallel to the c axis, i is the number of the sub-band of energy eigenvalues, $\xi_i(z)$ is the wave function, and ϵ_i is the energy eigenvalues. As a result of this calculation, $\xi_i(z)$ and ϵ_i were obtained. We then determined E_F and the electron density at each sub-band in the inversion layer (n_i) so as to satisfy the following equations:[29,32]

$$D_{2D} = M_C \frac{m^*_{c\perp}}{\pi \hbar^2}, \tag{4}$$

TABLE I. Effective masses for the lowest and the second lowest energy bands in 4H-SiC.[33] Here, m_e is the electron rest mass. In calculating the effective masses, we applied $m^*_{c\perp} = \sqrt{m_{M\Gamma} m_{MK}}$ and $m^*_{c\parallel} = m_{ML}$.

	Lowest band	Second lowest band
m_{ML}	$0.31m_e$	$0.71m_e$
$m_{M\Gamma}$	$0.57m_e$	$0.78m_e$
m_{MK}	$0.28m_e$	$0.16m_e$
$m^*_{c\perp} = \sqrt{m_{M\Gamma} m_{MK}}$	$0.40m_e$	$0.35m_e$
$m^*_{c\parallel} = m_{ML}$	$0.31m_e$	$0.71m_e$

$$n_i = D_{2D} k_B T \ln\left[1 + \exp\left(\frac{E_F - \epsilon_i}{k_B T}\right)\right], \tag{5}$$

$$n_{free} = \sum_i n_i, \tag{6}$$

where M_C (=3)[2] is the number of equivalent valleys, $m^*_{c\perp}$ is the effective mass perpendicular to the c axis, k_B is the Boltzmann constant, and T is the absolute temperature. A sufficient number of the subbands were taken into consideration up to the energy level at which the occupied electron density was negligible. The lowest and second lowest energy bands with different effective masses are considered; Table I summarizes the effective masses of those bands.[33] The band edge of the second lowest energy band is located at ~0.12 eV higher than that of the lowest band.

The Poisson equation was solved based on the obtained n_i and ξ_i above to determine $\varphi(z)$ for the next step,[29]

$$\frac{d^2\varphi(z)}{dz^2} = -\frac{\rho_{dep}(z) - e\sum_i n_i |\xi_i(z)|^2}{\varepsilon_s}, \tag{7}$$

where $\rho_{dep}(z)$ (= $-eN_A$) is the charge density inside the depletion layer and ε_s is the dielectric constant of the semiconductor. The above calculation procedure was repeated until the difference of E_F between N and $(N-1)$ steps (N is a natural number) was less than 10^{-6} eV.

Finally, n_{trap} was calculated by[34]

$$n_{trap}(\psi_S) = \int_{E_i}^{\infty} \frac{D_{it}(\psi_S)}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} dE. \tag{8}$$

Here, D_{it} distribution was assumed to be expressed as[6,35]

$$D_{it} = D_0 + D_1 \exp\left(\frac{E - E_C(\text{3D-DOS})}{E_1}\right) + D_2 \exp\left(\frac{E - E_C(\text{3D-DOS})}{E_2}\right), \tag{9}$$

where D_0, D_1, D_2, E_1, E_2, and Q_{fix} were used as fitting parameters to reproduce the experimental gate characteristics and E_C (3D-DOS) is the bottom edge of three-dimensional density of states of SiC. These six parameters were needed to reproduce the experimental gate characteristic in the whole measured voltage range.

IV. EXTRACTION OF INTERFACE STATE DENSITY

Figure 2(a) shows the typical experimental and calculated gate characteristics for lightly doped ($N_A = 3 \times 10^{15}$ cm^{-3}, peak mobility: 31 cm^2 V^{-1} s^{-1}) and heavily doped ($N_A = 1 \times 10^{18}$ cm^{-3}, peak mobility: ~6 cm^2 V^{-1} s^{-1}) NO-annealed MOSFETs. Figure 2(b) shows those for lightly doped ($N_A = 3 \times 10^{15}$ cm^{-3}, peak mobility: ~3 cm^2 V^{-1} s^{-1}) and heavily doped ($N_A = 1 \times 10^{18}$ cm^{-3}, peak mobility: ~0.01 cm^2 V^{-1} s^{-1}) as-oxidized MOSFETs. In either Figs. 2(a) or 2(b), the calculated results reproduce the experimental characteristics in the range of $V_G = 0$–15 V (corresponding to the energy range of $E_C - E_T = -0.18$–0.38 eV) very well.

Figure 3(a) shows the D_{it} distributions plotted with respect to the bottom edge of 3D-DOS obtained from the I_D–V_G fitting. The obtained D_{it} distributions strongly depend on the acceptor concentration of the p-body: The D_{it} values obtained from the lightly

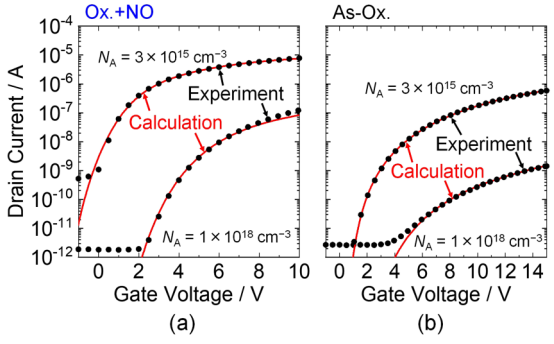

FIG. 2. Typical experimental and calculated gate characteristics for (a) lightly doped ($N_A = 3 \times 10^{15}$ cm^{-3}, peak mobility: 31 cm^2 V^{-1} s^{-1}) and heavily doped ($N_A = 1 \times 10^{18}$ cm^{-3}, peak mobility: ~6 cm^2 V^{-1} s^{-1}) NO-annealed MOSFETs and for (b) lightly doped ($N_A = 3 \times 10^{15}$ cm^{-3}, peak mobility: ~3 cm^2 V^{-1} s^{-1}) and heavily doped ($N_A = 1 \times 10^{18}$ cm^{-3}, peak mobility: ~0.01 cm^2 V^{-1} s^{-1}) as-oxidized MOSFETs.

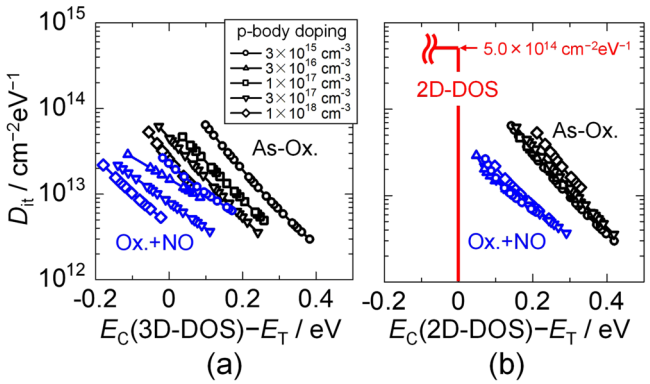

FIG. 3. Energy distributions of the interface state density with respect to the bottom edge of (a) three-dimensional and (b) two-dimensional density of states obtained from the gate characteristics of MOSFETs.

doped MOSFET are about five times higher than those for the heavily doped MOSFET, which is hardly understandable. On the other hand, Fig. 3(b) shows the D_{it} distributions plotted with respect to the bottom edge of 2D-DOS. In contrast to the results based on the bottom edge of 3D-DOS [Fig. 3(a)], the D_{it} distributions are almost uniquely determined by the oxide formation condition (As-Ox. or Ox. + NO) and independent of acceptor concentration. In general, the formation energy of a defect should depend on the position of the Fermi level. As the oxidation/annealing of SiC is carried out at a high temperature (1250–1300 °C), however, the Fermi level approaches the intrinsic level and only slightly depends on the acceptor density. This is due to the carrier excitation from the valence to conduction band, which occurs at a sufficient high temperature. In such a sense, the picture presented in Fig. 3(b) is more reasonable than in Fig. 3(a), where the D_{it} distributions are uniquely determined by the oxide formation process and hardly depend on the acceptor density. Note that the difference between Figs. 3(a) and 3(b) is only the difference in the energy basis (how to plot the data with respect to the energy), and in either case, the free electron density was calculated using the two-dimensional density of states. The results presented in Fig. 3(b) clearly indicates that the defect levels are subjected to quantum confinement and thus pushed up to higher energy levels in samples with higher acceptor density due to stronger surface electric field. One of the possible origins of the observed interface states is the *tail states*, originating from the energy fluctuation of conduction band edge.[25,36] As the tail states originate from perturbation/fluctuation of the conduction band, it is natural that their energy levels are shifted together with the 2D-DOS due to the quantum confinement. Indeed, a recent study based on first-principles calculations revealed that the atomic-level interface roughness could severely affect the energy level of E_C in the case of SiC (0001)/SiO_2 systems.[37] Since the energy levels of conventional defects (e.g., near-interface traps[38]) should be fixed with respect to the vacuum level, these are unlikely to be the origin of the observed defect states.

Here, we discuss the impact of the assumed mobility values on the D_{it} distributions. Figure 4 shows the free electron density dependence of Hall mobility for the lightly doped NO-annealed MOSFET ($N_A = 3 \times 10^{15}$ cm^{-3}). It can be seen that the actual Hall mobility weakly depends on the free electron density (or the surface potential) and takes values of 80–120 cm^2 V^{-1} s^{-1} for the lightly doped NO-annealed MOSFET ($N_A = 3 \times 10^{15}$ cm^{-3}). It is also reported that the Hall mobility for a heavily doped MOSFET ($N_A = 4 \times 10^{17}$ cm^{-3}) is in the range of about 10–20 cm^2 V^{-1} s^{-1}.[28] Thus, we intentionally changed the value of assumed mobility to see if the obtained D_{it} distributions are affected, as shown in Figs. 5(a) and 5(b). In Figs. 5(a) and 5(b), similar D_{it} distributions are obtained even when changing the value of assumed mobility within 80–120 cm^2 V^{-1} s^{-1} for lightly doped MOSFETs ($N_A = 3 \times 10^{15}$ cm^{-3}) and within 10–20 cm^2 V^{-1} s^{-1} for heavily doped MOSFETs ($N_A = 3 \times 10^{17}$ cm^{-3}). Therefore, we may conclude that the error resulting from the assumed constant mobility is negligibly small. In addition, although the highest energy level of occupied sub-bands depends on free electron density, the measured Hall mobility weakly depends on the free electron density. This fact suggests that the difference in the mobility for electrons in different sub-bands is rather small.

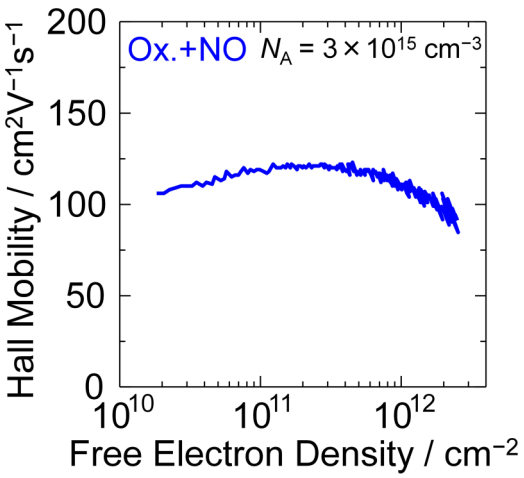

FIG. 4. Free electron density dependence of the measured Hall mobility for the lightly doped NO-annealed MOSFET ($N_A = 3 \times 10^{15}$ cm^{-3}).

Based on the obtained results, we briefly discuss the dominant limiting factors of the drain current in the SiC MOSFETs. Figure 6 shows the ratio of free electron density (n_{free}) to the total electron density ($n_{free} + n_{trap}$) for the fabricated MOSFETs as a function of the free electron density dependence. In Fig. 6, we see that the $n_{free}/(n_{free} + n_{trap})$ ratio is about two to four times higher in the NO-annealed samples than in the as-oxidized samples at a given n_{free}, indicating that the drain current increase by the NO annealing is attributable to the increase in the free electron density. The $n_{free}/(n_{free} + n_{trap})$ ratio is almost identical among samples with different acceptor densities. On the other hand, it is known that the drain current remarkably decreases in heavily doped MOSFETs.[14,39] Thus, the drain current decrease in heavily doped MOSFETs is mainly due to the decrease in the drift mobility,

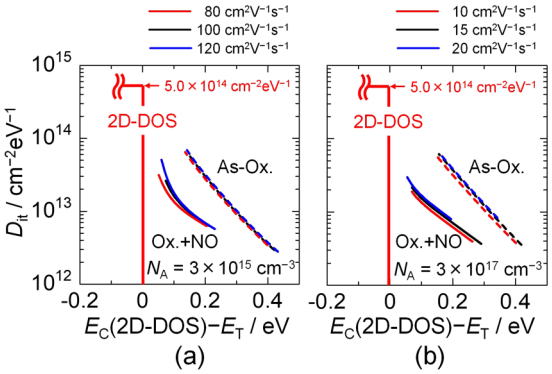

FIG. 5. Energy distributions of the interface state density obtained by changing the value of assumed mobility (a) within 80–120 cm^2 V^{-1} s^{-1} for lightly doped MOSFETs ($N_A = 3 \times 10^{15}$ cm^{-3}) and (b) within 10–20 cm^2 V^{-1} s^{-1} for heavily doped MOSFETs ($N_A = 3 \times 10^{17}$ cm^{-3}).

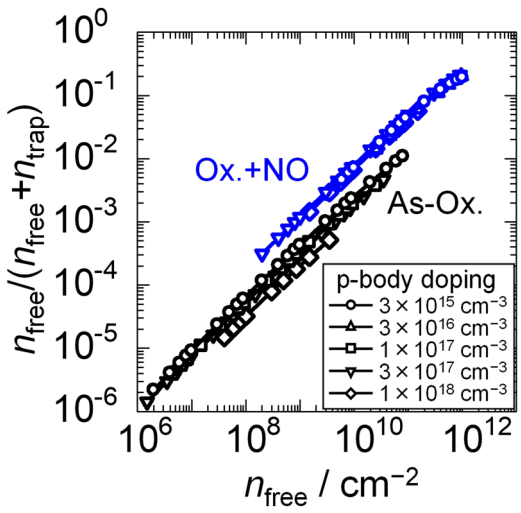

FIG. 6. Proportion of free electrons to the total electrons [$=n_{free}/(n_{free}+n_{trap})$] as a function of the free electron density for SiC MOSFETs with various acceptor concentrations of p-bodies.

rather than the decrease in the free electron density. The Hall mobility likely degrades in heavily doped MOSFETs due to the Coulomb scattering.[28]

V. CONCLUSION

In conclusion, we determined the D_{it} distributions near the conduction band edge in 4H-SiC (0001) MOS structures by reproducing the experimental I_D–V_G characteristics of MOSFETs with numerical calculations. In the calculation, potential distributions and energy sub-bands in the inversion layer were calculated by solving Poisson and Schrödinger equations, respectively. The obtained D_{it} distributions are almost uniquely determined by the oxide formation process (as oxidation or interface nitridation) and independent of the acceptor concentration (3×10^{15}–1×10^{18} cm^{-3}). We confirmed that the ratio of the free electron density with respect to the total electron density increases by the NO annealing, suggesting that the drain current increase in the NO-annealed MOSFETs is attributable to the increase in the free carrier density. In contrast, the $n_{free}/(n_{free}+n_{trap})$ is almost identical among MOSFETs with different acceptor concentrations (3×10^{15}–1×10^{18} cm^{-3}), indicating that the drain current decrease observed in heavily doped MOSFETs is mainly ascribed to the decrease in the drift mobility rather than the decrease in the free carrier density.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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