Electrical properties of Si-Si interfaces obtained by room temperature covalent wafer bonding

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(Received 20 December 2017; accepted 6 February 2018; published online 23 February 2018)

We study covalent bonds between p-doped Si wafers (resistivity ∼10 Ω cm) fabricated on a recently developed 200 mm high-vacuum system. Oxide- and void free interfaces were obtained by argon (Ar) or neon (Ne) sputtering prior to wafer bonding at room temperature. The influence of the sputter induced amorphous Si layer at the bonding interface on the electrical behavior is accessed with temperature-dependent current-voltage measurements. In as-bonded structures, charge transport is impeded by a potential barrier of 0.7 V at the interface with thermionic emission being the dominant charge transport mechanism. Current-voltage characteristics are found to be asymmetric which can tentatively be attributed to electric dipole formation at the interface as a result of the time delay between the surface preparation of the two bonding partners. Electron beam induced current measurements confirm the corresponding asymmetric double Schottky barrier like band-alignment. Moreover, we demonstrate that defect annihilation at a low temperature of 400 °C increases the electrical conductivity by up to three orders of magnitude despite the lack of recrystallization of the amorphous layer. This effect is found to be more pronounced for Ne sputtered surfaces which is attributed to the lighter atomic mass compared to Ar, inducing weaker lattice distortions during the sputtering. *Published by AIP Publishing*. https://doi.org/10.1063/1.5020139

I. INTRODUCTION

Low temperature (LT) covalent bonding of semiconductors has attracted significant attention in the past years as it is expected to facilitate the integration of various semiconductor materials with silicon (Si) without the limitations of epitaxy.[1,2] The most important of these limitations is dislocations induced by the lattice mismatch and layer cracking and wafer bowing due to different thermal expansion coefficients. Furthermore, LT covalent bonding could provide novel possibilities for designing future semiconductor based devices, with an expected boost in performance and manufacturing efficiency. LT wafer bonding offers the unique possibility to combine the existing large-scale and low-cost complementary metal-oxide-semiconductor (CMOS) platform with advanced optoelectronic functionalities of other semiconductors, like GaAs, Ge, or CdTe with high mobilities and/or bandgaps.[1]

For devices that require a conductive bonding interface but do not allow for high-temperature treatments—as for CMOS based ones—conventional bonding techniques such as hydrophobic bonding[3] and hydrophilic bonding[4] are inapplicable. Hydrophobic bonding requires high temperature treatments to remove the hydrogen passivation prior to bonding, while hydrophilic bonds are non-conducting due to the oxide layer at their interface. The room temperature bonding method with ion beam sputtering was proposed as a viable alternative to these conventional direct wafer bonding techniques.[5] With this method, the native oxide on the Si wafer surface is removed by a noble gas plasma creating reactive dangling bonds ("surface activation"). At the same time, this sputtering process amorphizes the Si surface to a depth of typically 1–2 nm. Immediately after their respective activation, the two wafers are brought into contact and the self-propagating bonding process is initiated by a small load applied to the top wafer resulting in strong covalent Si-Si bonds.[5]

Previous research on wafer bonding with ion beam sputtering was mainly focused on structural aspects of the interface.[6,7] Only little interest was devoted to the electrical behavior of bonding interfaces especially between low-doped semiconductors for which the amorphous layer is likely to exert the biggest influence. Here, we study bonds between low p-doped Si wafers with a resistivity around 10 Ω cm. The wafer bonds were fabricated by the latest large-scale 200 mm industrial equipment to elucidate the impact of the amorphous bonding interface on the electrical conductivity.

II. EXPERIMENTAL

Wafer bonds from identical prime Si wafers with a 200 mm diameter were fabricated at room temperature using EVG's recently presented EVG580 ComBond machine—a high vacuum wafer bonding system.[8] The ComBond features a central handling cluster with attached modules for plasma surface activation, wafer flipping, and wafer bonding. Wafer transfer between the respective modules is fully automated with typical transfer times in the range of a minute. The handling cluster and the attached modules are under high-vacuum (∼10^{-8} mbar). Low-doped p-Si (100) with ∼10 Ω cm was chosen for this work as the electrical transport across the interface is especially sensitive to the presence of defects

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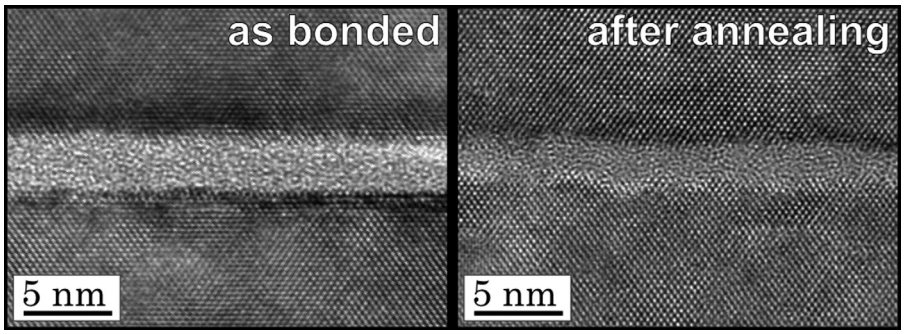

FIG. 1. Cross sectional HR-TEM images of the Ne-sputtered Si-Si bonding interface. Left: As bonded state. Right: After annealing for 14 days at 400 °C.

in this case. The oxide layers on the wafer surfaces were removed by ion beam sputtering prior to bonding with typical ion energies of ∼200 eV yielding bulk-like bond strengths. The sputtering was carried out with either Ne or Ar plasmas to investigate a potential dependence on the ion mass. Varying sputter times and energies as well as incidence angles within 10 to 180 s, 100 to 800 eV, and 15° to 45°, respectively, did not show any noticeable influence on the electrical behavior and will thus not explicitly be discussed here. Electrical characterization was done on quadratic samples with a surface area of ∼1 cm^2. Ohmic Al-contacts 8 × 8 mm^2 in size were deposited by electron beam evaporation and annealing for 5 min at 300 °C. Current-voltage (IV) measurements up to ±100 V were carried out between 300 and 420 K with a standard probe station on a heatable and temperature controlled stage. Post-bonding annealing was done in a tube furnace at 400 °C for annealing times up to 14 days. Electron beam induced current (EBIC) measurements were done on a Tescan FERA3 Plasma-FIB/scanning electron microscopy (SEM) in cross section for various beam currents at a fixed acceleration voltage of 10 kV. For the EBIC characterization, the sample surfaces were field effect passivated with atomic layer deposited Al_2O_3 to effectively prevent minority carrier electrons from recombining at the surface.[9] The EBIC samples were contacted in the scanning electron microscopy (SEM) chamber with a micromanipulator on their top contact and the stage connected to their back contact. High resolution transmission electron microscopy (HR-TEM) was carried out using a JEOL 2200FS TEM microscope operated at 200 kV. TEM samples were prepared by mechanical polishing and ion milling to achieve electron transparency using a Fischione ion mill model 1050 with 3 and 2 kV Ar ions.

III. RESULTS AND DISCUSSION

A. Structural

Figure 1 shows cross sectional HR-TEM images of the Ne-sputtered Si-Si interface taken along the [110] direction before (left) and after annealing at 400 °C for 14 days (right). As usual after ion beam sputtering, an amorphous layer of ∼3 nm exists at the as-bonded Si-Si interface, irrespective of the sputtering gas. In addition to removing the SiO_2, the ion beam also amorphizes the Si surface and creates reactive bonding partners. Despite the long annealing time of 14 days, the temperature treatment did not lead to full recrystallization of the layer but to an irregular reduction of its thickness. When annealing at high temperatures (e.g., for 1 h at 800 °C), the amorphous layer completely recrystallizes and forms a dislocation network due to the small twist and tilt of the two wafers with respect to each other (not shown). The latter is well known from conventional direct bonding and reported elsewhere.[10] Scanning acoustic microscopy measurements have proven the absence of voids at the interface. The obtained bond strengths, as accessed with the Maszara method,[11] took values up to the one of bulk silicon.

B. Electrical

Typical current-voltage characteristics of bonding interfaces before ("as-bonded," dashed lines) and after annealing (straight lines) are presented in Fig. 2. Regardless of the actual sputtering process, the as-bonded interface is strongly blocking and reveals a non-linear IV-behavior. In addition, the IV-curves commonly exhibit a pronounced asymmetry, which can be observed, for instance, for the Ar sputtered sample (red dashed line). The magnitude of this asymmetry was observed to vary between different wafer bonds and between individual samples of the same bond. This phenomenon, which indicates that the microscopic structure of the interface favors charge transport in one direction, will be explained in Sec. III C. Figure 2 also shows that after annealing for 48 h at 400 °C the conductivity across the interface is significantly higher. The improvement of the interface conductivity with annealing is discussed in detail in Sec. III D.

Figure 3 (left) represents current-voltage characteristics of a Ne-sputtered sample for temperatures between 300 K

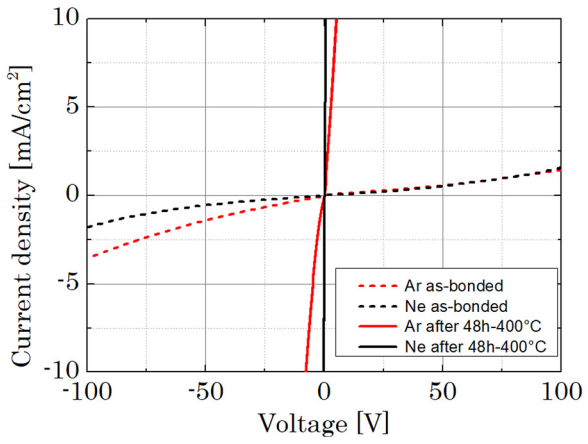

FIG. 2. Typical current-voltage characteristics of bonding interfaces fabricated by Ne or Ar sputtering. The dashed lines present the as-bonded state, while the straight lines show the behaviour after annealing for 48 h at 400 °C.

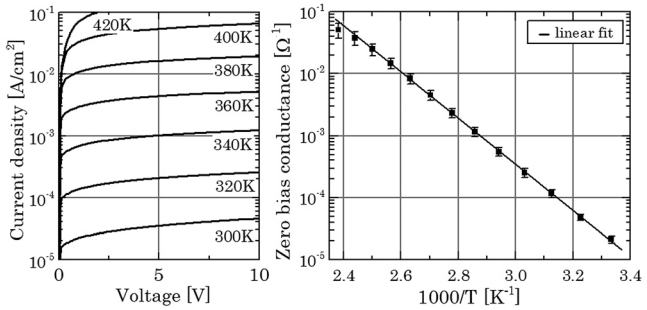

FIG. 3. Left: Temperature dependent current-voltage characteristic of the Ne-sputtered bonding interface. Right: Corresponding Arrhenius plot and linear fit of the data indicating an exponential thermal activation (data points are averaged over five samples and error bars show the standard deviation).

and 420 K. At 300 K, the interface is strongly blocking with a zero bias conductance of the order of $10^{-5}\ \Omega^{-1}$. With increasing temperature, the conductance continuously grows and reaches values $>10^{-2}\ \Omega^{-1}$ at 400 K. The right hand side of Fig. 3 shows the corresponding Arrhenius plot of the conductance for the temperature range between 300 K and 420 K, averaged for five identical samples. The straight Arrhenius plot over more than three decades implies an exponential increase $\sim\exp(-E_A/k_BT)$ of the current density with temperature and thus thermal activation of the charge transport across the interface. From the slope of the Arrhenius plot, one finds $E_A = 0.7\,eV$ for the activation energy of the conductance, independent of the plasma type. It should be noted that the comparison with Al_2O_3 passivated samples revealed no measureable contribution from surface leakage currents across the bonded interface at the cleaved sample edges.

The strongly blocking nature of the interface and the temperature dependence can be explained with a potential barrier induced by the amorphous layer. The sputter induced α-Si layer contains a high density of unsaturated bonds giving rise to a large number of localized electronic states at the bonding interface. Those states get occupied and thus charged such that the Fermi level is pinned resulting in a potential barrier of height Φ_b and a depletion region in the vicinity of the interface.[12] Figure 4 illustrates the resulting band alignment for a p-Si/p-Si interface: Holes get trapped at the interface and fill up the electronic states giving rise to a positively charged layer. The depletion of holes in the valence band leads to a negative space charge region on both sides of the interface. Macroscopically, this resembles a double Schottky barrier-like band alignment as initially suggested for grain boundaries in semiconductors[13] and later applied to bonding interfaces.[12] Therefore, charge transport across the bonding interface is dominated by thermionic emission across the barrier and is analogous to the saturation current of a Schottky diode under reverse bias which is $\sim\exp(e\Phi_b/k_BT)$. We thus ascribe the measured activation energy to a potential barrier of $\Phi_b = 0.7$ V at the interface.

For materials with a low charge carrier density as used for this work, the depletion region is particularly wide (in the μm-range). An external voltage drops across the full depletion region on both sides of the interface, such that the electric field strength in the amorphous region is too small to induce breakdown (the intrinsic breakdown field of crystalline Si is of the order of 3×10^5 V/cm). This explains our finding that the interface blocks charge transport even at voltages up to ±100 V at room temperature.

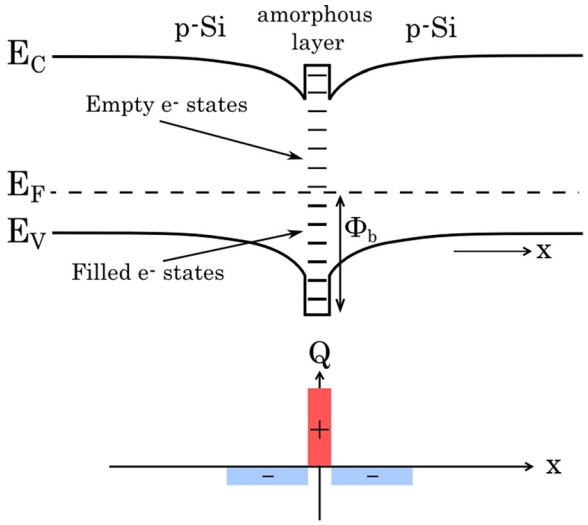

FIG. 4. Schematic band structure at the bonding interface and the corresponding charge distribution in equilibrium for p-doped Si. The Fermi level is pinned in the bandgap, and a depletion layer exists in the vicinity of the interface.

C. Asymmetry of the IV characteristic

In Fig. 5, EBIC line scans across the bonding interface are presented for a sample with pronounced asymmetric IV-characteristics as shown in the inset. The EBIC curves are presented for three different electron beam currents (2.5, 10, and 50 pA). The scan direction is perpendicular to the bonding interface which is located at zero position. Minority carrier electrons excited by the electron beam diffuse in the Si until they recombine in the bulk, at the surface, or at the bonding interface which acts as a sink for electrons in p-Si. If and only if excited electrons effectively recombine with a hole located on the opposite side of the interface, an EBIC current is measured. Recombination in the wafer excited by

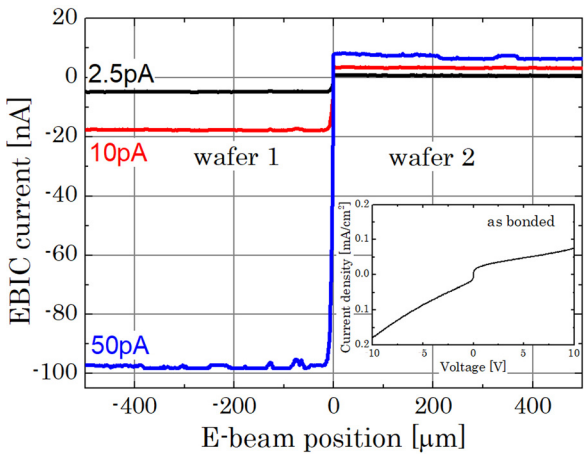

FIG. 5. EBIC line scans across the bonding interface from wafer 1 to wafer 2 for beam currents of 2.5, 10, and 50 pA. The inset shows the corresponding IV-measurement of the same sample.

the electron beam does not induce any EBIC current as there is no net charge flow through the interface. The figure shows that measured EBIC currents are approximately constant over the scan range of $\pm 500\,\mu$m from the bonding interface. This indicates negligible surface and bulk recombination, thus proving the effectiveness of the Al_2O_3 surface passivation—and it is consistent with the high diffusion length of electrons in weakly doped p-Si. The fact that the measured EBIC current scales approximately linearly with the beam current implies the absence of charging or saturation effects. The EBIC current generated by illuminating wafer 1 is, however, significantly higher compared to the one generated on wafer 2 for all beam currents. This observation can be explained by the existence of a small electric dipole at the bonding interface originating from different electronic density of states on the two sides, as proposed for EBIC results obtained on grain boundaries.[14,15]

A schematic drawing of the suggested asymmetric band alignment is presented in Fig. 6. The difference in state density pins the Fermi level at different positions on both sides of the interface, leading to tilted bands in the amorphous layer and an electric dipole field across the junction, as shown in the drawing. Thus, for electrons excited on wafer 1 [left side, Fig. 6(a)], the asymmetric band alignment favors recombination on the other side of the bonding interface. In contrast, when exciting on wafer 2 [right side, Fig. 6(b)], recombination on the same side of the interface is favored. While the first process does generate an EBIC current, the second does not, which explains the shape of the curves in Fig. 5. For a perfectly symmetric state distribution and horizontal bands, one would expect the generation of the same EBIC current on both sides. The asymmetric potential barrier is also the origin of the observed asymmetrical IV-behavior (inset). Indeed, the comparison of different samples has shown a consistent correlation of the favored charge flow direction for both IV and EBIC measurements.

For a bonding interface between two identical Si wafers, we suggest that the asymmetric electronic state density distribution is due to the successive (one after the other) sputter-treatment of the wafer surfaces prior to bonding. The highly reactive unsaturated bonds of the first sputtered wafer locally interact with residual gas in the bonding chamber before being brought into contact with the second sputtered wafer.

D. Annealing behavior

Figure 7 represents the impact of annealing at 400 °C on the interface conductivity. 400 °C was selected as annealing temperature as it poses a limit for possible CMOS applications. The zero bias conductance—with values averaged over five samples—strongly improves upon annealing. For Ne sputtered surfaces, the zero bias conductance increases by approximately three orders of magnitude within 48 h. In contrast, for Ar sputtered surfaces, the improvement is less pronounced and also takes longer with an increase by around two orders of magnitude within 120 h. The conduction of as-bonded structures is on the other hand nearly the same for both kinds of recipes. Longer annealing times did not have a significant additional impact on the conductivity for both plasma types. Despite the improvement, the conductance of annealed bonds remains more than one order of magnitude below the theoretical conductance of $\sim 1\Omega^{-1}$, given by the bulk resistivity and the sample geometry.

The improvement of the electrical performance through annealing can be explained by partial recrystallization along with a shrinking width of the α-Si and an effective reduction of states at the interface through defect annihilation.[16] In consequence, the position of the Fermi level in the α-Si layer shifts towards the valence band edge such that there is no potential barrier and no hole depletion anymore. Tunneling—also assisted by localized states in the α-Si—is then likely to be the dominant charge transport mechanisms across the amorphous layer. Apparently, the interface conductivity

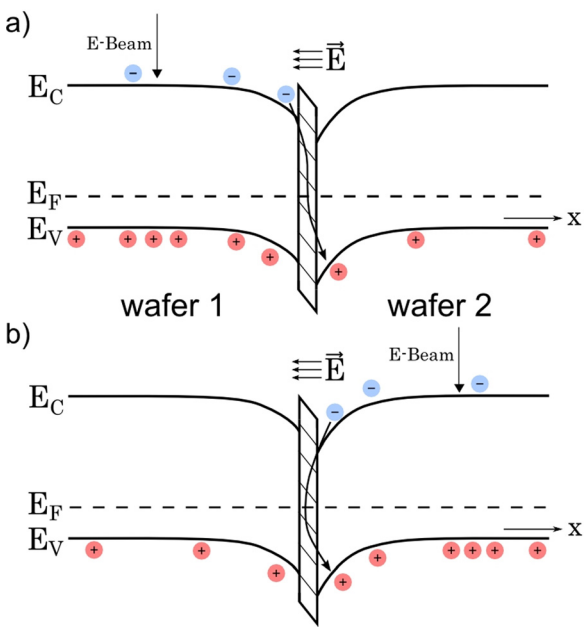

FIG. 6. Scheme of the band alignment for an asymmetric double potential barrier at the interface and the recombination processes involved. Recombination on the opposite side of the excitation (a) generates EBIC current, while recombination on the same side as the excitation (b) does not.

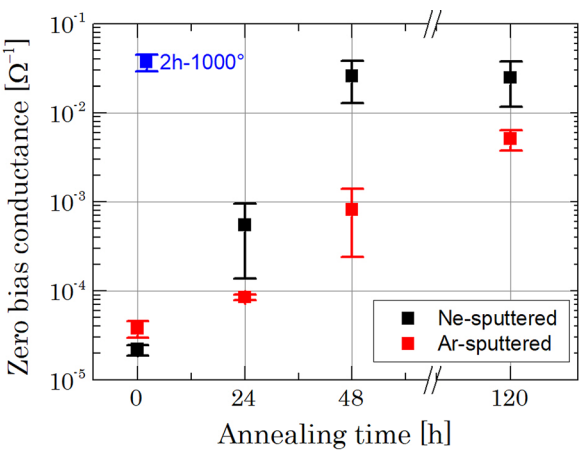

FIG. 7. Evolution of the zero bias conductance as a function of annealing time for both Ne and Ar sputtered surfaces, averaged over five samples, respectively.

improvement for Ne sputtered wafer surfaces is both faster and more effective compared to Ar sputtering. We assume that the Ne sputtering induces a weaker lattice distortion compared to the Ar sputtering which is thus easier to be relaxed upon annealing.

For the sake of comparison, the conductivity of entirely recrystallized bonded interfaces with dislocation networks obtained after annealing for 2 h at 1000 °C is shown (blue dot). The conductivity of the recrystallized interface is only slightly better compared to the amorphous one after annealing which we attribute to the electrical activity of the dislocation network. Indeed, it was shown before that dislocation networks of wafer bonded interfaces have a detrimental impact on the overall electrical performance as dislocations can serve as "scattering centers" for charge carriers.[17] It can thus be concluded that long term defect annihilation at low temperature presents a viable alternative to lattice recrystallization at high temperature which is an important result for devices that do not allow for high-temperature treatments.

E. Conclusion

Covalent p-Si/p-Si wafer bonds (10 Ω cm) fabricated at room temperature with ion beam sputtering prior to bonding were studied. The resulting amorphous layer at the interface impedes charge transport at room temperature. This was attributed to thermionic emission across the potential barrier formed by the amorphous interfacial layer through temperature-dependent IV measurements. IV-characteristics in combination with EBIC analyses suggest that the time lapse between the surface activation of the bonding partners can result in local interface state asymmetries. The interface conductivity significantly improves with defect annihilation at 400 °C after which its performance is almost as good as fully recrystallized bonding interfaces obtained through high-temperature annealing. This result is relevant for applications that require a conducting bonding interface but do not allow for high-temperature treatments such as CMOS based devices.

ACKNOWLEDGMENTS

We thank C. Floetgen from EVG for having fabricated the wafer bonds. In addition, we acknowledge I. Prieto, M. Doebeli, B. Bissig, and G.-L. Bona for valuable scientific discussions. G-ray Medical Sàrl, the FIRST Center for Micro- and Nano-Science and ScopeM Scientific Center for Optical and Electron Microscopy is gratefully acknowledged for making available their infrastructure. Finally, we cordially acknowledge the financial support by the CTI Project PIXISENS (No. 17703.1 PFNM-NM) and by the SNF Sinergia Project NOVIPIX (No. CRSII2_147639).

[1]U. Gösele and Q.-Y. Tong, Annu. Rev. Mater. Sci. **28**, 215 (1998).
[2]Z. H. Zhu, F. E. Ejeckam, Y. Qian, J. Zhang, Z. Zhang, G. L. Christenson, and Y. H. Lo, IEEE J. Sel. Top. Quantum Electron. **3**, 927 (1997).
[3]Q. Y. Tong, E. Schmidt, U. Gösele, and M. Reiche, Appl. Phys. Lett. **64**, 625 (1994).
[4]O. Engstrom, S. Bengtsson, G. I. Andersson, M. O. Andersson, and A. Jauhiainen, J. Electrochem. Soc. **139**, 3638 (1992).
[5]H. Takagi, K. Kikuchi, R. Maeda, T. R. Chung, and T. Suga, Appl. Phys. Lett. **68**, 2222 (1996).
[6]M. Morimoto, J. Liang, S. Nishida, and N. Shigekawa, Jpn. J. Appl. Phys., Part 1 **54**, 030212 (2015).
[7]J. Liang, T. Miyazaki, M. Morimoto, S. Nishida, and N. Shigekawa, J. Appl. Phys. **114**, 183703 (2013).
[8]C. Flötgen, N. Razek, V. Dragoi, and M. Wimplinger, ECS Trans. **64**, 103 (2014).
[9]B. Hoex, J. Schmidt, P. Pohl, M. C. M. van de Sanden, and W. M. M. Kessels, J. Appl. Phys. **104**, 44903 (2008).
[10]M. Reiche, Mater. Sci. Forum **590**, 57 (2008).
[11]W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, J. Appl. Phys. **64**, 4943 (1988).
[12]S. Bengtsson and O. Engström, J. Appl. Phys. **66**, 1231 (1989).
[13]N. C.-C. Lu, C. Y. Lu, L. Gerzberg, and J. D. Meindl, IEEE Trans. Electron Devices **30**, 137 (1983).
[14]E. Ziegler, W. Siegel, E. Blumtritt, and O. Breitenstein, Phys. Status Solidi A **72**, 593 (1982).
[15]D. B. Holt, B. Raza, and A. Wojcik, Mater. Sci. Eng. B **42**, 14 (1996).
[16]S. Roorda, W. C. Sinke, J. M. Poate, D. C. Jacobson, S. Dierker, B. S. Dennis, D. J. Eaglesham, F. Spaepen, and P. Fuoss, Phys. Rev. B **44**, 3702 (1991).
[17]M. Reiche, M. Kittler, R. Scholz, A. Hähnel, and T. Arguirov, J. Phys.: Conf. Ser. **281**, 12017 (2011).