Space-charge limited current in CdTe thin film solar cell

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In this study, we demonstrate that space-charge limited current (SCLC) is an intrinsic current shunting leakage in CdTe thin film solar cells. The SCLC leakage channel, which is formed by contact between the front electrode, CdTe, and the back electrode, acts as a metal-semiconductor-metal (MSM) like transport path. The presence of SCLC leaking microchannels in CdTe leads to a band bending at the MSM structure, which enhances minority carrier recombination and thus decreases the minority carrier lifetime in CdTe thin film solar cells. SCLC was found to be a limiting factor both for the fill factor and the open-circuit voltage of CdTe thin film solar cells. *Published by AIP Publishing.* https://doi.org/10.1063/1.5023106

Thin film solar cells, whether they are made of organic or inorganic materials, are composed of different kinds of thin films with several junction/contact interfaces. The interface electronic and micro-structure properties are the key factors to fabricate high efficient thin film solar cells. The interface is the location where the internal electric field is formed to separate light-generated carriers, and it is also the location where carrier recombination and current shunting/leaking occur.[1,2] The thickness decrease in the active layer in a thin film solar cell would induce electric shunting micropaths due to non- uniform structures at an interface. Space-charge limited current (SCLC), induced by formation of a metal-semiconductor-metal (MSM) electrical symmetric structure, has been detected to be formed in both organic and inorganic solar cells, such as amorphous silicon, germanium, and copper indium gallium diselenide solar cells.[3–6] SCLC is the dominant current transport mechanism in a semiconductor with a symmetric MSM structure where the carrier density in the semiconductor is negligibly low compared to the carriers injected from the metal contact.[7] SCLC in a thin film solar cell can be expressed as $I = k \times V^m$, where $m = \frac{T_c}{T} + 1$, k is related to the material dielectric permittivity and carrier drift mobility, and T_c is defined as a characteristic temperature which reflects trap energy distribution in bandgap.[5–8]

In a CdTe thin film solar cell, the CdS window layer thickness is usually thin and controlled to be ~80 nm to reduce light absorption in CdS. It is unavoidable that the symmetric contact MSM structure, namely, fluorine doped tin oxide (FTO)/p-CdTe/ohmic metal, can be formed in microscale through the inter-diffusion or reaction between CdTe and CdS, as shown in Fig. 1(a).[9] Here, FTO can be considered as a metal contact whose carrier concentration is $\sim 10^{21}\,cm^{-3}$. The polycrystalline CdTe absorber film in a CdTe solar cell has a carrier concentration of $\sim 10^{13}$–$10^{14}\,cm^{-3}$, which is quite low compared to that in FTO and in a metal contact. Figure 2 shows the schematic electronic energy band diagrams of a FTO/CdTe/Cu/Au MSM structure and a CdTe solar cell. When a low voltage is applied on a FTO/p-CdTe/ohmic metal contact structure, the current is mainly dominated by the transport of carriers generated in the p-CdTe layer through thermal activation. This transport can be described by the ohmic law. When the applied voltage on a MSM structure is increased to a voltage called as "transition voltage", the electric conduction begins to be dominated by SCLC, which is induced by accumulation of carriers injected into the CdTe layer from the metal electrode [see Fig. 2(a)].[7] The injected hole carrier density in a MSM microchannel is orders of magnitude larger than that in the depleted CdTe region in a CdTe thin film solar cell. This would lead to band bending around the MSM channel, as schematically shown in Fig. 1(b). The band bending collects minority electrons from the neighboring CdTe, resulting in much enhanced recombination in the MSM structure.

A key issue to fabricate a high efficiency CdTe solar cell is the low minority carrier lifetime in CdTe, which is usually of the order of nanosecond or tens of nanosecond.[10,11] The open-circuit voltage V_{oc} of the champion efficiency CdTe solar cell is 876 mV, much lower than the ideal value of 1156 mV.[12] Low minority carrier lifetime is one of the key limiting factors to increase the V_{oc}. In this work, SCLC has been experimentally demonstrated to be an intrinsic current shunting leakage in the thin film CdTe solar cell and one of the factors leading to enhanced carrier recombination and reduced minority carrier lifetime.

The CdTe solar cells fabricated in this study had a structure of glass/FTO/CdS/CdTe/Cu/Au. The CdS window layer was ~80 nm thick. The polycrystalline CdTe absorber films with a thickness of ~4 μm were prepared using a close-spaced sublimation apparatus. The bimetal Cu/Au layer was served as ohmic back contact. All-area MSM-like device structures were fabricated with a structure of glass/FTO/p-CdTe/Cu/Au, in which the window layer CdS was absent

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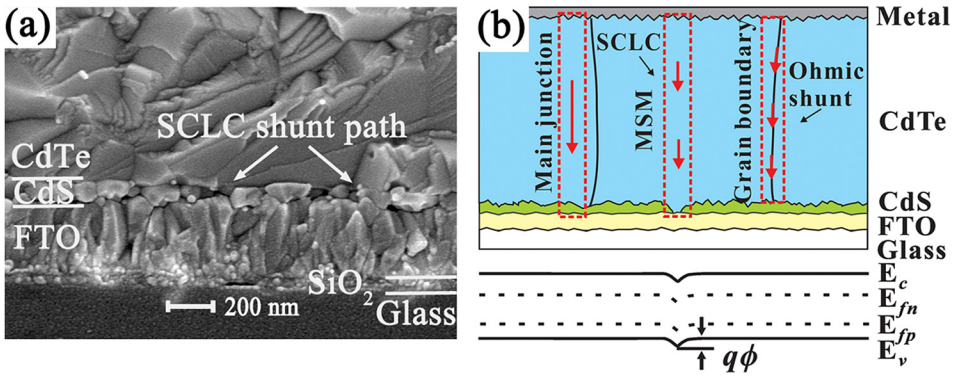

FIG. 1. (a) SEM cross-sectional microstructure of a CdS/CdTe solar cell and (b) schematic diagram of ohmic and SCLC shunting channels presented in a thin film CdTe solar cell and band bending near a SCLC leakage channel.

to let CdTe directly be contacted with the FTO electrode. The device size of both the solar cells and the MSM structures was $0.5 \times 0.5\,\mathrm{cm}^2$.

In a CdTe thin film solar cell, electric shunting paths, whether they are of macroscopic or microscopic scale, significantly reduce the V_{oc} and fill factor. The shunting paths can be classified as an ohmic or non-ohmic shunting type. Ohmic shunting path can be induced by the electric conduction along grain boundaries or by material bulk conductivity, as shown in Fig. 1(b).[13] Non-ohmic shunting can be induced by a microscopic weak diode due to electron tunneling caused by heavily doped regions at the interface of CdTe/CdS or SCLC along the MSM-like FTO/p-CdTe/Cu/Au structure channel.[6] The equivalent electric model of a CdTe solar cell in dark can be expressed as follows:[14]

$$J_D = J_{01}(e^{q(V-J_DR_S)/n_1k_BT} - 1) + J_{02}(e^{q(V-J_DR_S)/n_2k_BT} - 1) + k(V-J_DR_S)^m + (V-J_DR_S)/R_{sh}, \quad (1)$$

where the first term is the current corresponding to the main p-n junction. The second term represents the weak diode current. SCLC leaking through the MSM structure is represented by the third term $k(V-J_DR_S)^m$. The last term describes the ohmic shunting current. J_{01} and J_{02} are the reverse saturation current densities, V is the output voltage, n_1 and n_2 are the ideality factors, and R_s and R_{sh} are the lumped series and shunt ohmic resistance. k is related to the film thickness and the conductivity of the transport path. m is related to the density of states of the transport path. The currents contributed by the main and weak junctions can be easily identified in J-V curves, which demonstrate exponential curve shape. Both the SCLC and the ohmic shunting are symmetric with regard to applied reverse and forward voltage. These two shuntings can be readily identified by the fittings to a J-V curve due to the ohmic and non-ohmic dependence of the currents on the applied voltage. Figure 3 shows the curve fittings to the J-V curve of a CdTe solar cell with an efficiency of 11.2%. The fittings were carried out by using the equivalent electric model with and without SCLC contribution to the current. The fitting J-V curve shown in Fig. 3(a), which was fitted without considering the SCLC, demonstrates a much lower current than that of the measured data in the high reverse voltage region (<-0.25 V). When the SCLC contribution was included in the fitting, the fitting J-V curve perfectly matches the experimental data, as shown in Fig. 3(b). Figure 3(c) shows the current contributions to the experimental J-V data according to the equivalent circuit model described by Eq. (1). In the reverse voltage region, the currents were mainly contributed by the SCLC and the ohmic shunting leakage current. In the forward voltage region above 0.4 V, the main diode current dominated the current. Figure 3(d) shows the ratio of the SCLC to the total dark current. It can be seen that in the reverse voltage region, SCLC contributed a significant part to the dark current. In the low forward voltage region, SCLC had the same values as that in the reverse voltage due to the symmetric nature. However, the J_{sclc}/J_D ratio was decreased quickly with increased voltage due to the current turn-on of the main junction diode.

The current value of SCLC would be proportional to the MSM channel area presented in a CdTe solar cell. In this study, we fabricated an all-area MSM-like structure, namely, a structure of FTO/p-CdTe/Cu/Au, in which the CdS window

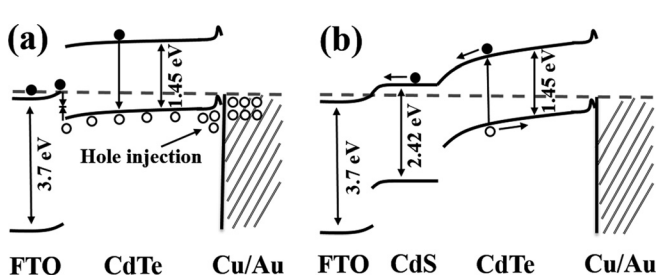

FIG. 2. Schematic electronic energy band diagrams, carrier transport, and carrier recombination in (a) a FTO/CdTe/Cu/Au structure and (b) a CdTe solar cell structure.

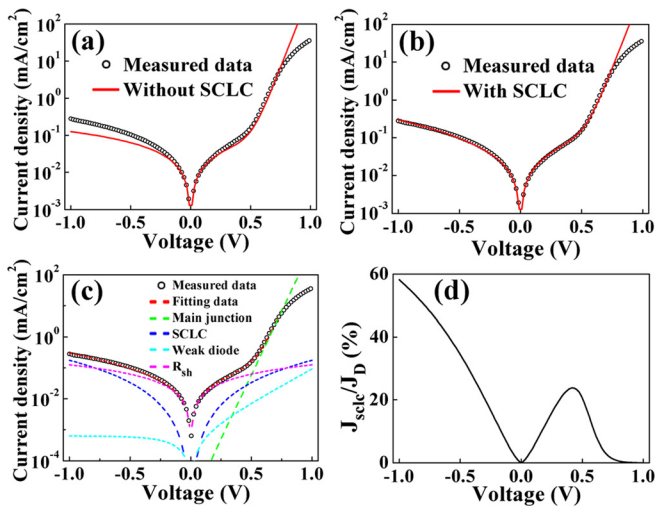

FIG. 3. Dark *J-V* curves fitted by an equivalent electric circuit model: (a) fitting without SCLC, (b) fitting with SCLC, (c) fitting details with all the different shunting paths, and (d) J_{sclc}/J_D versus the voltage.

layer was absent, and therefore, the CdTe semiconductor was in direct contact with the FTO. As a comparison, we also fabricated an FTO/p-CdTe/Au structure, which has a Schottky junction between the CdTe and the Au metal electrode.[15] Figs. 4(a) and 4(b) show the dark J-V curves of the two devices. The FTO/p-CdTe/Au structure exhibits a typical Schottky junction J-V curve. However, the J-V curve of the FTO/p-CdTe/Cu/Au structure was quite symmetric in both the forward and the reverse voltage region, which is consistent with the assumption that the current is mainly composed of SCLC and ohmic current, although the current at high forward voltage was little higher than that at reverse voltage. For the FTO/p-CdTe/Cu/Au structure, Cu/Au formed an almost ohmic contact with CdTe, and therefore, FTO/p-CdTe/Cu/Au acts as an MSM device for SCLC transport.

The SCLC conduction characteristics can be further studied by temperature dependent current transport. The temperature-dependent log J-log V curves of the FTO/p-CdTe/Cu/Au MSM structure are shown in Fig. 4(c). It can be seen that the current was dominated by ohmic current and SCLC at low and high voltages, respectively. The transition voltage, where ohmic transport was changed to SCLC, was increased with the increased device temperature as indicated by the dashed line. This was induced by the higher thermally generated carrier density in CdTe at high temperature.[8] The increased transition voltage with the increased temperature is a strong evidence that SCLC is the dominant transport current at high voltage, namely, at a high carrier injection level. The dark J-V curves of both an FTO/p-CdTe/Cu/Au MSM structure and a CdTe solar cell with an efficiency of 13.5% were measured and fitted from room temperature to 360 K. Figures 5(a) and 5(b) show the parameter k versus 1000/T curves of both the devices. It can be seen that both the k values show a similar changing behavior with decreased temperature. This is consistent with the previous study.[6] Due to the different coverage of the MSM channel area in these two devices, the k value of the FTO/p-CdTe/Cu/Au MSM structure is almost two orders of magnitude larger than that of the CdTe solar cell at room temperature. The parameter m values of both the devices were linearly increased with 1/T, as shown in Figs. 5(c) and 5(d). Since the value of m is influenced by trap energy distribution in the CdTe bandgap, the higher m value for the CdTe solar cell compared to the MSM structure is suggested to be induced by the diffusion of S into the CdTe layer which acted as an interstitial or substitute impurity in CdTe.[16]

The MSM microchannel structure formed in a CdTe solar cell can reduce minority carrier lifetime through two recombination processes. One is carrier recombination at the FTO/CdTe interface. The other is carrier recombination in CdTe enhanced by SCLC transport [see Fig. 2(a)]. Figure 6(a) shows the measured dark J-V and the fitting curves of three CdTe solar cells with efficiencies of 11.4%, 13.1%, and 14.4%. The light and dark J-V curves and the main parameters of the three cells are shown in Fig. 6(c). In Fig. 6(a), only the current contributions from the SCLC and the main junctions are shown for clarity. It is noted that the SCLC and the reverse saturation current J_0 demonstrate the same variation trend with increased/decreased cell efficiency. Figure 6(b) shows the variation of the J_0 and V_{oc} values of the four CdTe solar cells with the SCLC value J_{sclc}. It can be seen that there are strong correlations between J_0/V_{oc} and J_{sclc}.

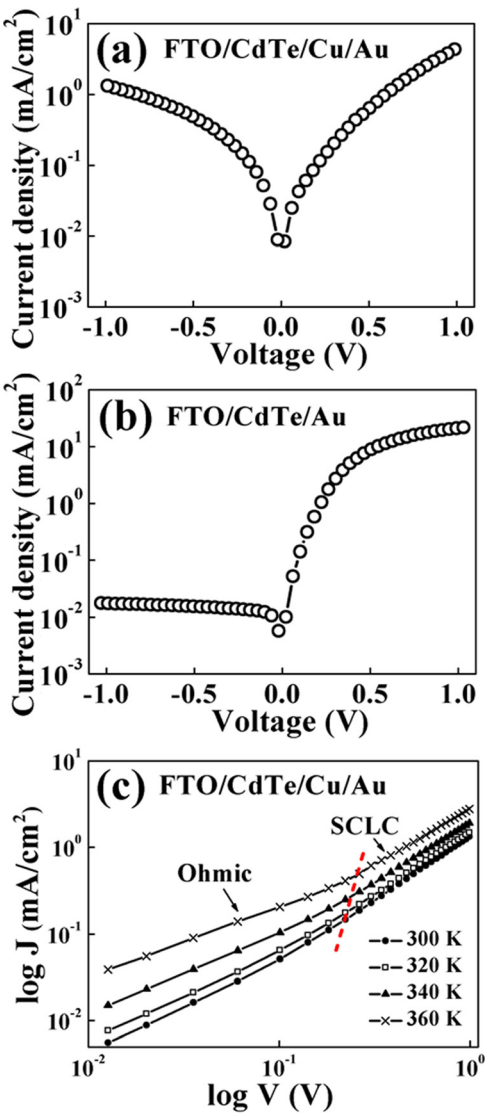

FIG. 4. Dark J-V curves of (a) the FTO/CdTe/Cu/Au structure, (b) the FTO/CdTe/Au structure, and (c) log J-log V curves of the FTO/CdTe/Cu/Au structure measured at different temperatures.

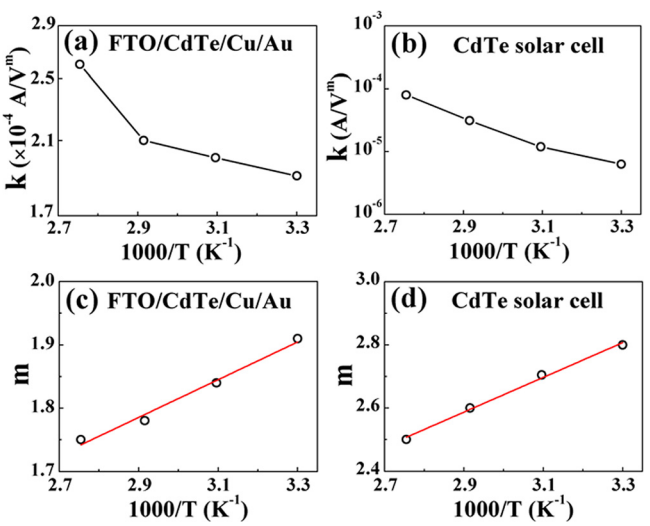

FIG. 5. Temperature dependence of the fitting parameters for the SCLC of the two devices: (a) and (b) k versus 1000/T and (c) and (d) m versus1000/T.

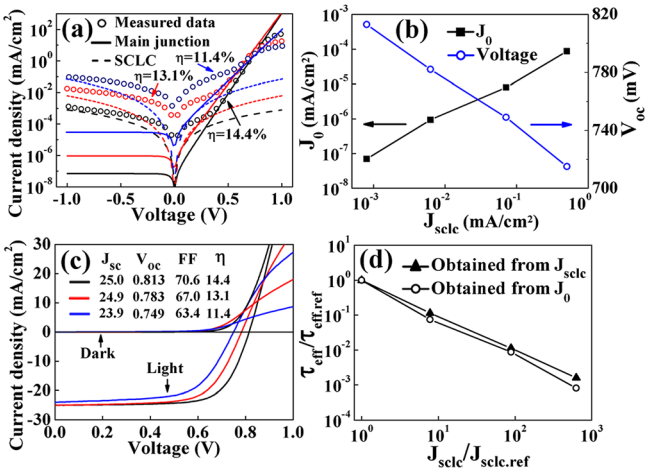

FIG. 6. (a) Dark *J-V* curves of three CdTe solar cells with different efficiencies and the corresponding fittings contributed by the main junction and the SCLC; (b) variation of the reverse saturation current density J_0 and the open-circuit voltage V_{oc} with SCLC current J_{sclc}; (c) light and dark J-V curves of the three solar cells; and (d) variation of the effective minority carrier lifetime with J_{sclc}.

The minority carrier lifetime in a p-type semiconductor can be written as $\tau_0 = \frac{p_1}{N_t r_n p_0}$, where N_t is the trap density in the semiconductor, r_n is the recombination rate of minority carrier electrons, p_0 is the thermal-equilibrium hole concentration, and $p_1 = N_v \exp[-(E_t - E_v)/kT]$, which is the hole concentration activated from traps with an effective energy level E_t.[17] The hole concentration in a MSM channel structure can be described by $p = p_0 \cdot \exp\frac{q\phi(V_b)}{kT}$.[8] The minority carrier lifetime in a MSM channel structure τ_{msm} can then be expressed as

$$\tau_{msm} = \frac{p_1}{N_t r_n p} = \tau_0 \cdot e^{-\frac{q\phi(V_b)}{kT}}. \tag{2}$$

The effective minority carrier lifetime in a CdTe solar cell can be expressed as $1/\tau_{eff} = 1/\tau_0 + 1/\tau_{msm}$, and thus, τ_{eff} can be written as

$$\tau_{eff} = \tau_0 \cdot \frac{1}{\exp\left(\frac{q\phi(V_b)}{kT}\right) + 1}. \tag{3}$$

From Eq. (3), it can be seen that, since kT has a value of 0.026 eV at room temperature, a very small band bending of $q\phi(V_b)$ would dramatically decrease the minority carrier lifetime in a CdTe solar cell. SCLC depends exponentially on $q\phi(V_b)$ by the following equation:[18]

$$J_{sclc} = qvp_0 \exp\left(\frac{q\phi(V_b)}{kT}\right), \tag{4}$$

where v is hole drift velocity. Then, τ_{eff} can be rewritten as

$$\tau_{eff} = \tau_0 \cdot \frac{1}{J_{sclc}/qvp_0 + 1}. \tag{5}$$

Choosing the CdTe solar cell with an efficiency of 14.4% as the reference device, we can estimate the relative minority carrier lifetime by using Eq. (5). For comparison, the practical minority carrier lifetime has been estimated by the saturation current values J_0 of the solar cells shown in Fig. 6(b). The minority carrier lifetime is related to J_0 by $J_0 = \frac{qw_d n_i}{2\tau_{eff}}$, where w_d is the junction depletion region width and n_i is the intrinsic carrier concentration of a semiconductor.[19] Assuming that w_d and n_i in all the four solar cells are the same, the practical relative effective minority carrier lifetime can be obtained using the J_0 values. From Fig. 6(d), we can see that the effective minority lifetimes obtained using the two methods have a strong correlation with the SCLC shunting in the CdTe solar cells. In a CdTe solar cell, recombination at interfaces and grain boundaries can also reduce the minority carrier lifetime. Therefore, the practical minority carrier lifetime is lower than that which only considers the lifetime decrease induced by SCLC. The results presented in this study demonstrate that SCLC is a key limiting factor of the minority carrier lifetime.

In summary, MSM-like FTO/p-CdTe/Cu/Au microscale leaking channel structure was found to be formed in the CdTe thin film solar cell. Space-charge limited current was the dominant current transport in the MSM microchannels and has been demonstrated to be an intrinsic shunting leakage current in the CdTe solar cell. The presence of SCLC transport channels enhanced carrier recombination and thus led to decreased minority carrier lifetime in the CdTe thin film solar cell.

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