



Interface traps contribution on transport mechanisms under illumination in metal–oxide–semiconductor structures based on silicon nanocrystals

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Abstract

The transport phenomena in metal–oxide–semiconductor (MOS) structures having silicon nanocrystals (Si-NCs) inside the dielectric layer have been investigated, in dark condition and under visible illumination. At first, using deep-level transient spectroscopy (DLTS), we find the presence of series electron traps having very close energy levels (comprised between 0.28 and 0.45 eV) for our devices (with/without Si-NCs). And a single peak appears at low temperature only for MOS with Si-NCs related to Si-NCs DLTS response. In dark condition, the conduction mechanism is dominated by the thermionic fast emission/capture of charge carriers from the highly doped polysilicon layer to Si-substrate through interface trap states for MOS without Si-NCs. The tunneling of charge carriers from highly poly-Si to Si substrate through the trapping/detrapping mechanism in the Si-NCs, at low temperature, contributed to the conduction mechanism for MOS with Si-NCs. The light effect on transport mechanisms has been investigated using current–voltage (I – V), and high frequency capacitance–voltage (C – V) methods. We have been marked the photoactive trap effect in inversion zone at room temperature in I – V characteristics, which confirm the contribution of photo-generated charge on the transport mechanisms from highly poly-Si to Si substrate through the photo-trapping/detrapping mechanism in the Si-NCs and interfaces traps levels. These results have been confirmed by an increasing about 10 pF in capacity's values for the C – V characteristics of MOS with Si-NCs, in the inversion region for inverse high voltage applied under photoexcitation at low temperature. These results are helpful to understand the principle of charge transport in dark condition and under illumination, of MOS structures having Si-NCs in the $\text{SiO}_{x=1.5}$ oxide matrix.

1 Introduction

The metal–oxide–semiconductor (MOS) structures having nanocrystals (NCs) embedded in their oxide layer (smart non-volatile memory devices [1–6], third generation solar cells [7] and single-electron devices [8]) have received much attention as promising candidates to replace conventional polycrystalline silicon or silicon nitride non-volatile memories for future high capacity and low power consuming memory devices. In this structure, we see that there are

likely traps present at the NC–matrix interface, at the Si/SiO₂ interface. The NCs (Si, Ge,...), presence in tunneling layer contributes to either directly to the memory effect or affects the charge trapping dynamics of the NC's. The NC's charging and discharging are widely supposed to take place by direct tunneling of charge carriers from/to the free carrier reservoir in the semiconductor substrate. So, the charge emission from NCs cannot be characterized by direct tunneling but rather by a trap-assisted tunneling mechanism, with the Si/SiO₂ interface states playing a key role as transfer nodes [9–11]. The energy distribution, the density of traps and capture kinetics of the interface and oxide traps are crucial for the future device applications. To obtain those information, deep-level transient spectroscopy (DLTS) could be used. Then, the DLTS technique is used to analysis the trap states in the semiconductors [12], and recently it has been applied in studying the semiconductor quantum dots (QD) [13]. To apply DLTS for studying MOS structures containing the nanocrystals it is necessary to obtain and analyze DLTS results on clean MOS structures (i.e., without

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nanocrystals). This will be enabling to separate DLTS signals coming from Si/SiO₂ interface and Si nanocrystals.

In this work, we confirmed the contribution of interface traps in the DLTS response of a MOS with and without Si-NCs. This contribution is marked on series of electron traps with too tight activation energies. This quantum of electron traps, assured the thermionic transition from conduction band of poly-Si to conduction band of Si substrate in dark condition. Under illumination, we confirm the contribution of photoactive traps to better dots photo-charging, and consequently, the contribution of photo-generated charge carriers on the transport mechanisms.

2 Experimental details

The MOS structures were developed in the Sherbrooke University combining nanolithography and reactive ion etching (RIE) process. The schematic cross-sectional structure of our device discussed in this paper is shown in Fig. 1a. Over a silicon (N-type) substrate, a non-stoichiometric oxide layer SiO_{x=1.5} is deposited by low pressure chemical vapor deposition (LPCVD) with two thicknesses: 5 and 10 nm (the fabrication and insulation of the oxide layer rich in silicon (SRO) is performed at CEA-LETI Grenoble). Then the layer is annealed of demixing for 3 min 30 s at 1000 °C to form silicon nanocrystals. A second annealing in oxygen at 1000 °C will be affected with a period of 5, 10 or 30 min. This annealing oxidizer allows the passivation of the nanocrystal surface. Finally, a high doped layer of polysilicon (with a doping density $N_{\text{polySi}} = 2 \times 10^{20} \text{ cm}^{-3}$) is deposited by LPCVD on SiO_x layer. The nanocrystals are formed by annealing the SRO in nitrogen environment. After the annealing, Si dots appear in thick and thin layers. The oxide is composed of silicon nanocrystals (Si-NCs) embedded in SiO_{x=1.5} layer. The thick SiO_{x=1.5} layer presents spherical silicon crystallites with an average size around 5 nm extracted from transmission electron microscopy

(TEM) measurements (Fig. 1b). The Si-NC density is about $\sim 1.6 \times 10^{-11} \text{ cm}^{-2}$. A second annealing step in oxygen was also performed. We used e-beam lithography and dry etching to obtain the vertical structures. $200 \times 200 \mu\text{m}^2$ active area detectors are finally obtained. The electrical insulation is provided by planar photosensitive resist: it was spun and then etched back by O₂ plasma. Then semi-transparent contacts Cr/Au (10 nm/10 nm) were formed on the polysilicon through photolithography and lifting of a bi-layer LOR 5A/S1813. They were then used as etching masks RIE to isolate the capacitors. The substrate is used for electrical continuity. Table 1 shows the layer structures of MOS of two samples (A) and (B). Sample (A) has a 5-nm thick SiO_{x=1.5} layer without Si-NCs (Reference), whereas sample (B) has a 10-nm thick SiO_{x=1.5} and indicate the presence of Si-NCs within the oxide layer.

The C–V and DLTS measurements were performed by a capacitance meter at a frequency of 1 MHz (model 410 C–V Plotter) with high resolution mode. To vary the filling pulse width, a pulse generator (Philips PM 5771) was used. The temperature measurement was varied in the range of 20–325 K using a closed-cycle liquid helium cryostat with a Lakeshore 330 auto-tuning temperature controller. For this system, the DLTS spectra will be made at a temperature where the locking frequency, f , was related to the emission rate by $e_n = 2.13 f$. [14]. The current–voltage (I – V) measurements were registered using a Keithley 238. To vary the wavelength and optical power, the illumination technique

Table 1 MOS structures

Sample (A)	Sample (B)
SiO _{x=1.5} (5 nm)	SiO _{x=1.5} (10 nm)
1000 °C/3 min 30 s/N ₂	1000 °C/3 min 30 s/N ₂
1000 °C/5 min/O ₂	1000 °C/5 min/O ₂
Poly-Si N ⁺ 50 nm	Poly-Si N ⁺ 50 nm
Substrat Si type N	Substrat Si type N

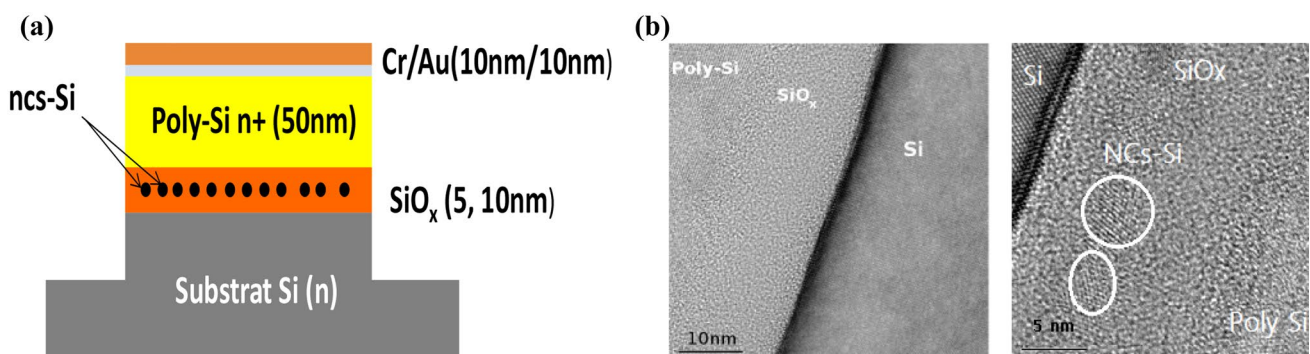


Fig. 1 **a** The schematic cross-sectional of MOS silicon nanocrystal structure, **b** TEM micrograph of MOS structures with and without silicon nanocrystals

used consist of passing a light beam through a monochromator from a tungsten lamp through an input slit, which will allow us to vary the excitation light wavelength. Then, the beam obtained at the exit of monochromatic will be focused on the sample using a lens. The device allows illuminating the sample on the side of the active layer and the side of the transparent substrate. The emitted radiation is relatively monochromatic; its optical power is of the order of a μW .

3 Results and discussion

3.1 DLTS analysis

Figure 2a and c shows the C – V measurements observed in MOS structure; a: reference sample: without Si-NCs, b: with Si-NCs: MOS-NCs. First, we can see the total absence of hysteresis in the reference sample which means that there

is no accumulated charge, so there is no Si-NCs at all the 5 nm $\text{SiO}_{2=1.5}$ layers. A clockwise hysteresis was observed for MOS-NCs, this hysteresis should be attributed to electron trapping into the Si-NCs or /and the interface of the nanocrystal dots, and not to defect in the oxide matrix or at the Si substrate/tunnel oxide interface [15].

The density of traps and the information regarding the energy distribution are crucial for the future device MOS applications. To obtain this information, deep-level transient spectroscopy (DLTS) could be used [12, 13].

A DLTS measurements have been carried out in temperature range from 50 to 320 K by varying the applied gate voltage from -2 to 0.5 V for windows ($e_n = 426 \text{ s}^{-1}$) and a filling pulse time of 0.5 ms (Fig. 2b: reference sample, and d: the MOS-NCs).

The DLTS is a well-established technique which is commonly used in studying the trap states in the semiconductors [16], recently it has been applied in studying

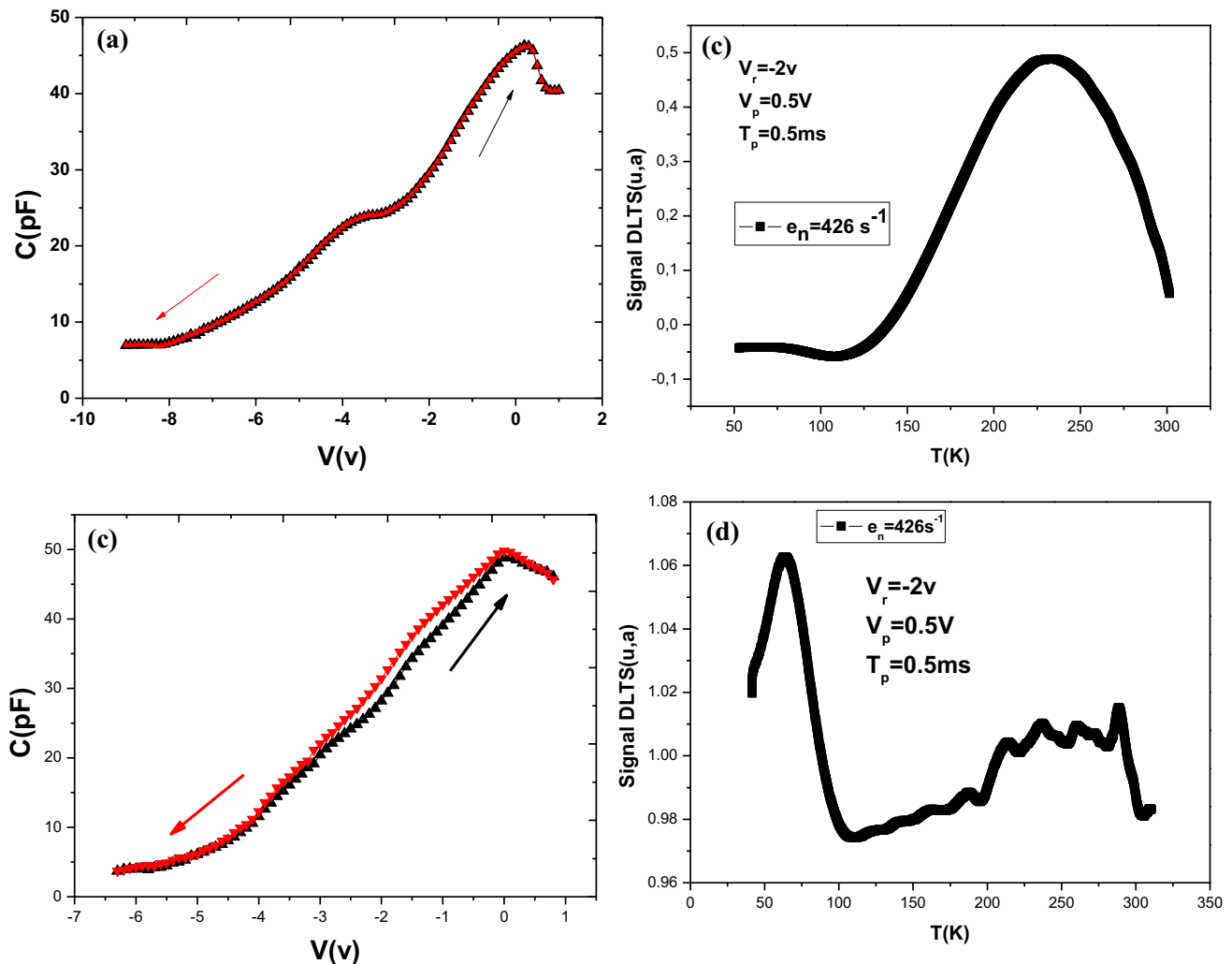


Fig. 2 Double sweep C – V curves and DLTS characteristics of the MOS; **a** and **b** structure without NCs, **c** and **d** devices containing NCs

the semiconductor-based nanocrystals [17]. In Fig. 2b, we have observed one positive signal for a large range temperature (120–300 K) in the DLTS spectrum for the MOS structure without Si-NCs. This signal is probably a DLTS response of a series electron traps with energy levels too close. This hypothesis can be enhanced by the DLTS response for a Si-NCs-MOS (Fig. 2d), where we can see clearly the separation on a series of multi-electron trap. Moreover, one positive signal corresponding to an electron trap has appeared for low temperature (70 K).

The principle of the DLTS technique consists in the analysis of the emission and capture assessed traps to variations in capacitance of a p–n junction or a Schottky diode. This is achieved by charging and discharging the traps repetitively, with a positive and /or negative polarization voltage applied to the sample. The curvature of the energy bands of semiconductor varied with the applied voltage, so a trap charge state will be dependent of the polarization and the capacity of the space charge region will be affected. During the pulse charging, the space charge zone decreases and the traps that lie below the Fermi level can be filled. To explain the origin physical of these signals, we need information on space zone depleted by the voltage bias, so the first step is the calculation of space charge zone extension ‘ w ’. In our case, we assume that the deep defect concentration is uniform with the space charge zone extension ‘ w ’ as the following Eq. (1) demonstrates [18]:

$$w = \sqrt{\frac{2\epsilon}{q(N_d + N_T^+)} \left(V_{bi} - V_r - \frac{kT}{q} \right)}, \quad (1)$$

where N_d is the doping concentration, N_T^+ is the deep defects concentration, V_{bi} is the intrinsic potential, and V_r is the applied potential.

Our structures are doped N^+ following densities ($N_{Si} = 6 \times 10^{17} \text{ cm}^{-3}$ and $N_{Poly-Si} = 2 \times 10^{20} \text{ cm}^{-3}$), which give a value of ‘ w ’ about 238 μm , so we can assume that the totality of the structure is scanned by the potential.

At low temperature (about 70 K), we can see that the electron trap appears only for the MOS with Si-NCs, so it is likely that a silicon nanocrystal DLTS response (Si-NCs DLTS response) has a high size dispersion of quantum dots which are considered as storage nodes. The thermally stimulated process is involved in the electron capture (hole emission) in the Si-NCs. In this case, the interface state may play a key role as transfer nodes [11]. The intrinsic levels of quantum dot are present on the energy band [11, 17] which is a series of discrete energy levels [17]. Applying low electrical pulse duration induces filling of the deeper levels and DLTS peak will be near of a discrete level. Increasing this time does not affect the deep levels of response, but the response of other shallower

levels is added to the DLTS signal. These levels have lower activation energies, therefore, faster emission (14 meV in our case; see Table 1; Fig. 6). This elementary reasoning explains the usefulness of a lower temperature to ensure detrapping carriers [19].

To explain the origin of the electron traps marked in Fig. 2b (The DLTS response of MOS structure without NCs), we varied the pulse duration from 0.2 to 0.5 ms, where we observed the variation of the amplitude of the DLTS peak for the same emission window (Fig. 4a).

The broad peak is a little decomposed for the low pulse duration [especially for the low time duration (0.3ms: Fig. 4a)]. As the saturation of these defects is fairly broad, this can be attributed to an extended series of electron traps behavior, having energy levels overly confined [20]. So basically, these levels are inherited in the oxide growth. Moreover, we note that the maximum of DLTS peak shifts to lower temperatures corresponding to increasing the window of issuance (Fig. 4b). A theoretical analysis and a measurement of the bulk traps and interface states in Si-MOS diodes demonstrated the distinction between interface charge and bulk traps [21]. This study confirmed that the emission rate of bulk traps at a temperature is constant regardless of the pulse bias for any pulse duration.

The peak temperature and shape of variation of transient capacitance should not change with pulse bias as time function (pulse duration), and consequently, their variation are not change. We keep the same rate window (462 s^{-1}), and constant reverse bias -2v but variable pulse duration (between 0.2, and 0.5 ms) on the MOS without Si-NCs. The obtained spectra are presented in Fig. 4a. In these DLTS spectra, we can see that the amplitude increasing with the pulse duration. At first, we can connect this result with the distorted in C – V curves (Fig. 3a, b). This results confirm the response of interfaces traps in DLTS analysis [15, 21]. This response is likely the emission/capture of charge carriers by an interface states and near-interface border traps [22].

The density of interface traps will be calculated using a Coleman–Hill method according to the following equation [23]:

$$D_{it} = \frac{(2/qs)(G_{\max}/w)}{\left[(G_{\max}/wC_{ox})^2 + \left(1 - \frac{C_m}{C_{ox}} \right)^2 \right]}. \quad (2)$$

With q the charge of the electron, S the surface in contact between the substrate and the gate oxide and between the gate oxide and the gate, G_{\max} the maximum value of the conductance at the excitation frequency (see Fig. 3), and C_{\max} the capacitance measured on the C – V curve at the same voltage as G_{\max} (see Fig. 3).

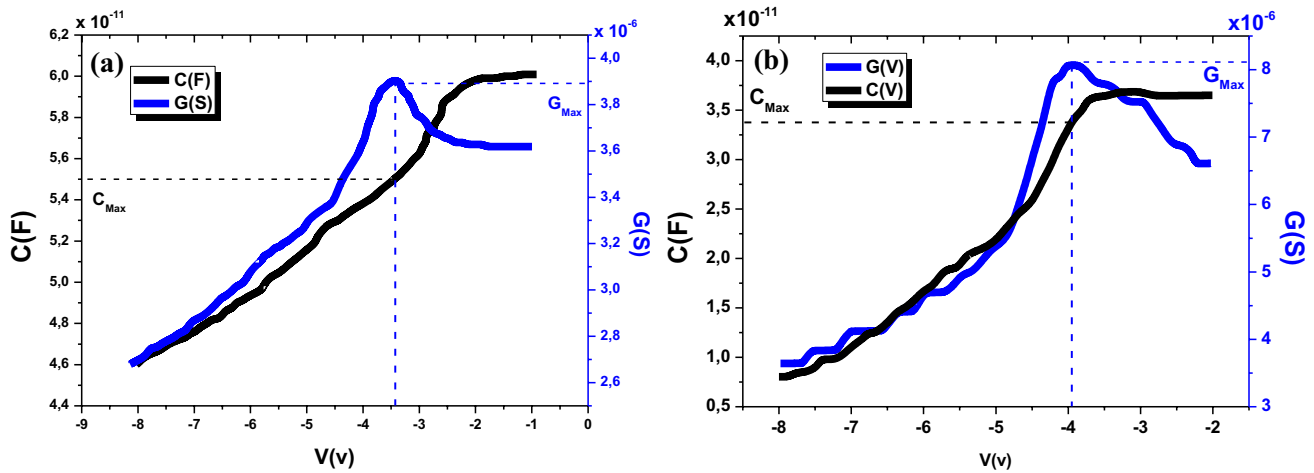


Fig. 3 Extraction of parameters (G_{\max} and C_m) from the Hill-Coleman method: **a** for MOS without Si-NCs ($G_{\max}=3.9 \times 10^{-6}$ S, $C_m=5.5 \times 10^{-11}$ F), and **b** for MOS with Si-NCs ($G_{\max}=8.3 \times 10^{-6}$ S, $C_m=3.45 \times 10^{-11}$ F)

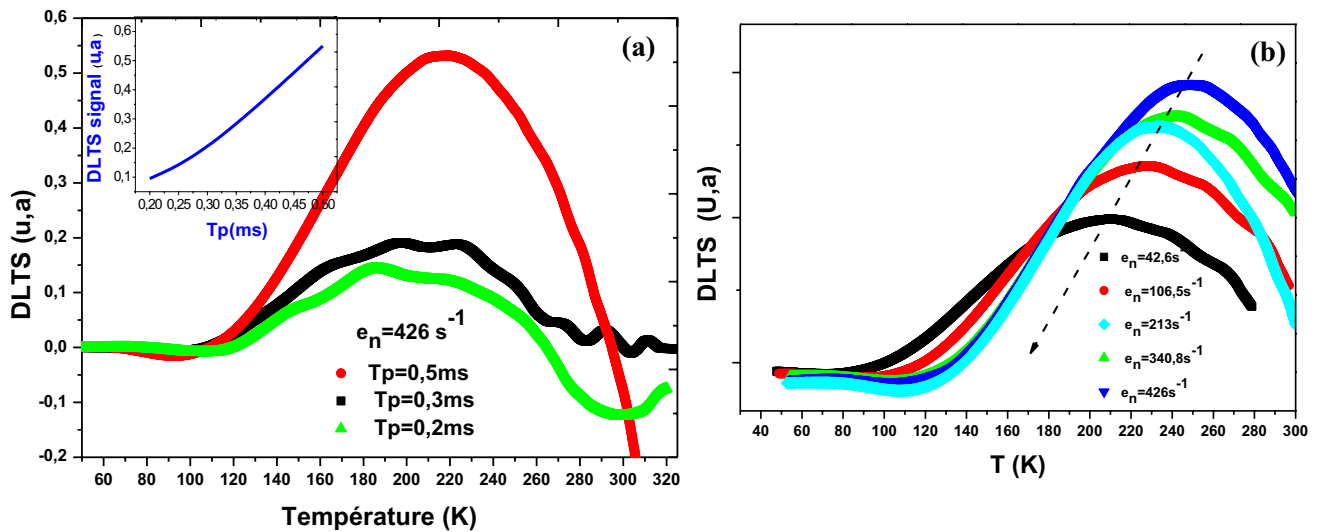


Fig. 4 The DLTS characteristics of the MOS structure without NCs: **a** the DLTS amplitude depending on pulse duration time, **b** DLTS characteristics depending on emission window

This method was well detailed in the following reference [24]. In our study, we used the conductance technique to determine the surface parameters with more accuracy than capacitance technique [25], because the conductance comes only from the interface states [26]. The conductance losses are the base of conductance technique, resulting from the exchange of majority carriers between the interface states, when a small AC signal is applied to the devices [27]. To calculate the approximate maximum density of surface states for our samples, we need only to determine the maximum value of conductance (G_{\max}) on the $G-V$ plot from Fig. 3a and b which involves capturing single $C-V$ and $G-V$ curves of the device. Once, we find the values of peak conductance

on the $G-V$ curve and the corresponding capacitance to that peak on the $C-V$ curve, this values will be used to calculate the interface trap density of the device by Eq. (2).

The value of this last density is about $2.49 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for a MOS structure without Si-NCs, and $D_{it}=6.1 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for a MOS-Si-NCs.

To test our hypothesis, we present the fitting of the DLTS response of NCs-MOS (Fig. 5). We assume that it is a series of multi-electron traps (five electron traps for MOS without Si-NCs, and six for a MOS having Si-NCs).

We can see also that it is the same activation energies order for the series of electron traps (with and without Si-NCs), so this is a DLTS response for same traps centers for

our MOS structures. The activation energies for this series of electron traps are too close (between 0.28 and 0.45 eV for a temperature range between 120 and 300 K (Tables 2, 3; Fig. 6). These traps have strong influence on the charge transport behavior, in which the traps and defects at the internal/surface of Si-NCs and the interface states at the SiO₂/Si substrate play different roles, respectively. It is suggested that the injected charges are mainly stored in the deep

traps of Si-NCs instead of the conduction band in long-term retention mode [28]. The long-term charge-loss process is primarily determined by the direct tunneling of the trapped charges to the interface states in the present experiment. The deep trapping centers are assured by quantum confinement and Coulomb charge effect [28]. In our case, the transport charge process is dominantly by the thermionic fast emission/capture of the charge carriers from the highly doped

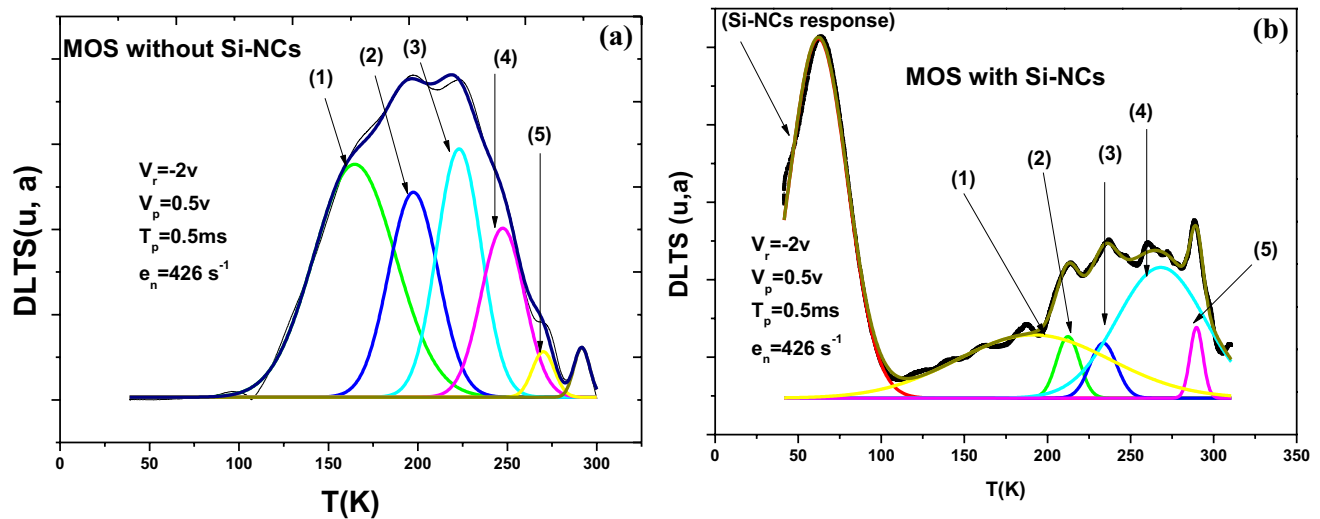


Fig. 5 DLTS deconvolution: **a** MOS without Si-NCs, **b** with Si-NCs

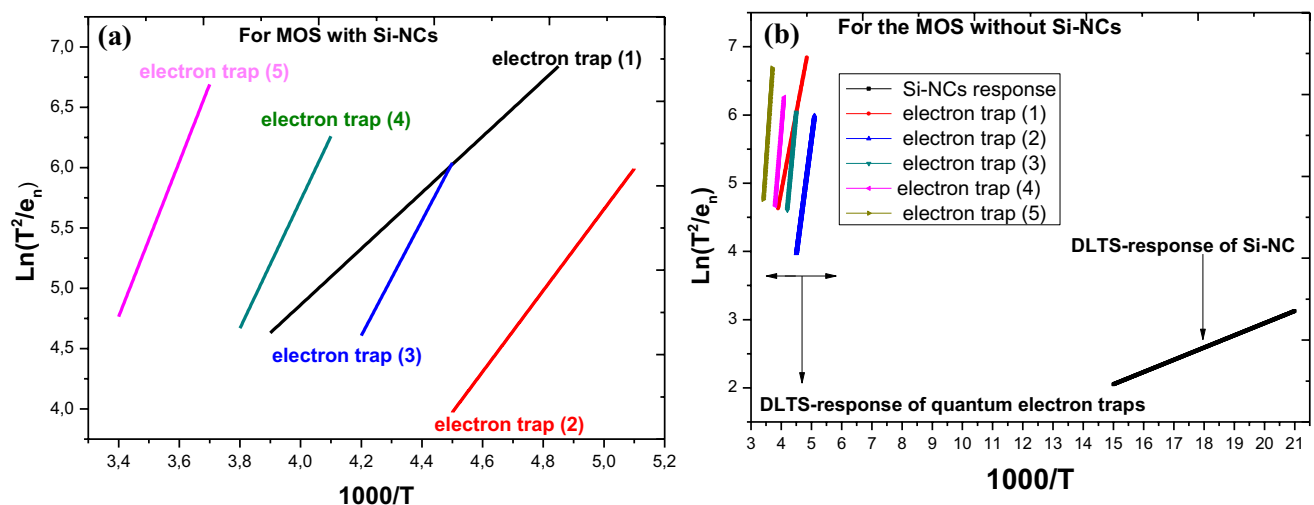


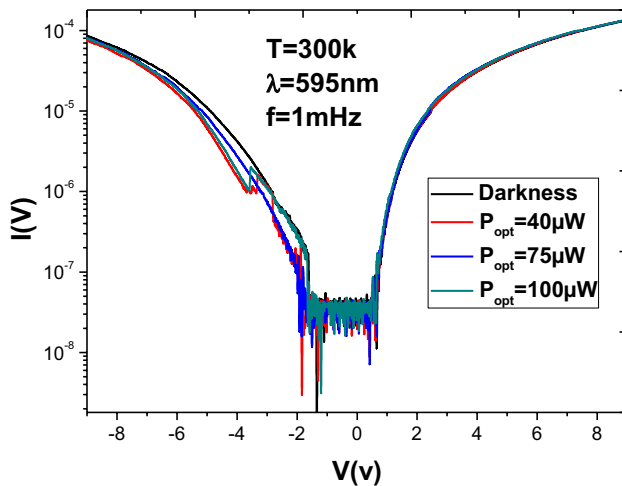
Fig. 6 Arrhenius diagram: **a** for MOS without Si-NCs, **b** for MOS with Si-NCs

Table 2 The activation energy (E_a) and capture section for MOS without a Si-NCs

	Without Si-NCs				
Electron traps no	1	2	3	4	5
E_a (eV)	0.29	0.34	0.41	0.45	0.45
σ_n (cm ²)	1.32×10^{-17}	1.56×10^{-17}	1.72×10^{-17}	2.12×10^{-17}	2.22×10^{-17}

Table 3 The activation energy (E_a) and capture section for MOS with a Si-NCs

With Si-NCs		1	2	3	4	5
Electron traps no	Si-NCs DLTS response					
E_a (eV)	0.014	0.28	0.33	0.41	0.45	0.45
σ_n (cm ²)	0.82×10^{-17}	1.34×10^{-17}	1.58×10^{-17}	1.42×10^{-17}	2.12×10^{-17}	2.22×10^{-17}

**Fig. 7** I – V measurements of MOS with Si-NCs at room temperature

poly-Si layer to the conduction band of substrate through interface traps states for a MOS structure without Si-NCs [29]. But for a Si-MOS structure, the transport process is dominated by the tunneling dot to dot of the charge carriers from the traps centers to the conduction band. The Coulomb interaction between electron and dots has sufficient time to transfer to tunnel oxide and to be captured in the NC-Si. The long-term localized charge detection characteristics in the oxidized nanocrystals can be directly attributed to their better encapsulation with $\text{SiO}_{x=1.5}$ and increased spatial isolation. This long duration time is marked in the DLTS response (a clear series of electron traps).

Generally, an optimum way to improve the retention time would introduce a certain number of deep trapping centers in Si-NCs and decrease the interface states at SiO_2 /Si substrate [28].

3.2 Light contribution on transport mechanisms

To analyze the light effect on the transport mechanisms, we used the I – V and C – V analyses in dark condition and under illumination.

3.2.1 I – V analysis

Figure 7 shows the current–voltage measurements of MOS having Si-NCs in dark condition and under illumination

(Photo- I – V), at room temperature (Fig. 7). This last figure proved that the light effect limited only in the inversion zone.

At first, we make think that is a photoactive traps effect for the voltage range comprised between (– 6 and 0 V).

Fundamentally, we recall the relationship between the Si-NCs absorbance and photon energy; this relationship is proportional to $(E_{\text{photon}} - E_g)^2$ where E_{photon} is the exciting photon energy and E_g is the band gap energy [30]. This relationship confirms the Si-NCs absorbance increasing is directly related to increase the emitted energy photon increase. Moreover, we see that Si-NCs have a fast optical transition [31], so facilitate their photo-charging. In addition, the capture of photo-generated charges carriers by the Si-NCs will be better by their quantum confinement effects [32]. Based on this last arguments and on our previous works [15, 33], we can confirm, that this light effect in the inversion region is related to Si-NCs photo-charging/discharging mechanism [15] or a photoactive trap effect. This photoactive trap serves to relate the transport phenomena of photo-generated charge carriers from poly-Si layer to SiO_2 through the Si-NCs.

3.3 C – V analysis

Figure 8 show the capacitance–voltage measurements in dark condition and under illumination (Photo- C – V) for our MOS having Si-NCs, at low temperature (Fig. 8a), and room temperature (Fig. 8b).

Figure 8 gives the evolution hysteresis phenomena with time duration of incident illumination. We can see the quasi-stable evolution of hysteresis width with the time duration. When we increase the time duration of light excitation, the hysteresis width increased also. We continue to increase the duration of light excitation, until we have saturation on the width of hysteresis after the 0.05 V/s ramp. These results can be attributed to full photo-charging of Si-NCs. The capacitance peak (~ 10 pF) appears in the inversion zone for low temperatures under photoexcitation attracts our attention. This result is directly related to the photo-generated traps effect. We can mention that this effect appeared only for low temperature. At first we recall that we have studied the traps contribution on the detection time for our devices in dark condition in our previous work [33]. The traps contribution in this last work is due to the dominance of tunneling of electrons from traps level thermally active at temperature range

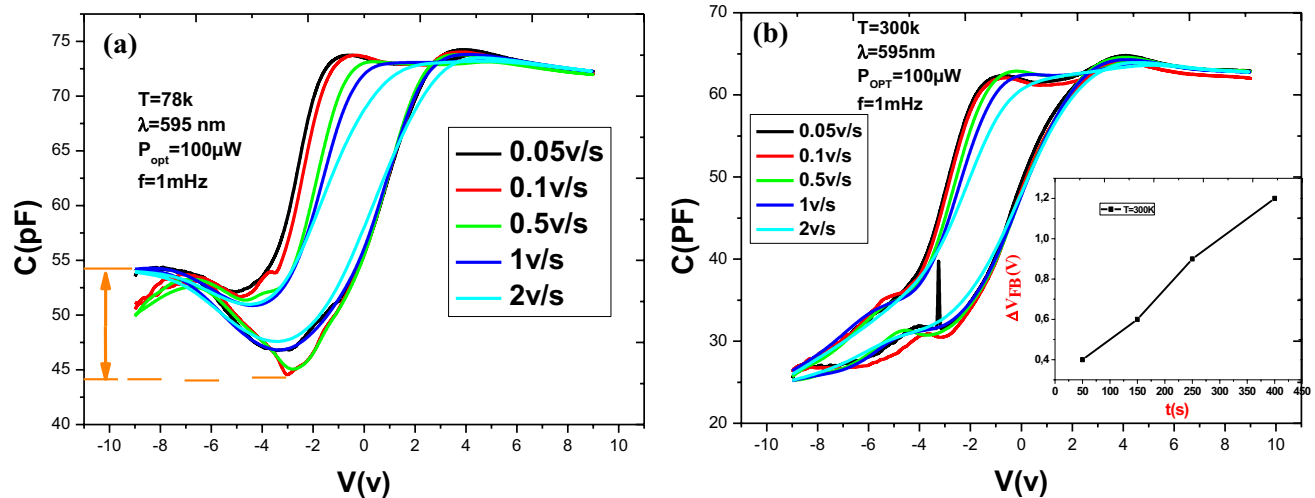


Fig. 8 C–V measurements of MOS having Si-NCs; **a** at low temperature, **b** at room temperature with the flat band evolution in time

comprised between 240 and 280 K to the Si/SiO₂ interface via the NCs-Si.

Our study confirms that is photoactive traps assured the direct exchange of photogenerated charge between Si-NCs and interface traps states [15]. Moreover, the contribution of these photoactive traps appears in the photo-detection time esteemed from the flat band evolution in time by values about 400 s (Fig. 8b). So we can conclude that Si-NCs will be better photo-charged at low temperatures through photoactive oxide traps. Consequently, the SiO₂ will not behave as a dielectric, but as a metal for a high illumination [34]. This makes us think that the total capacity of the structure no more corresponds to the capacity related to the oxide [34].

4 Conclusion

The DLTS measurements demonstrate their ability to study a Si-NCs and the interface traps density contribution on the charge transport for MOS structures with a small area. We identify the trapping mechanism in the Si-NCs quantum levels through a fine potential barrier by a tunnel emission from dot to dot for low temperatures. Moreover, we have identified the response of interface traps resulting by a series of slow electron traps, especially for the low pulse duration. Moreover, the effect of photoexcitation on silicon nanocrystals photo-charging-discharging phenomena was investigated. The photo-response of MOS photo detector was related to the absorption onset shift of Si-NCs, which was affected by the photo-active oxide tunnel traps. **In conclusion, our results indicate the important influence of silicon nanocrystals and the interface traps density of the charge transport for a MOS structure, and the photoactive traps contribution of transport mechanisms.**

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