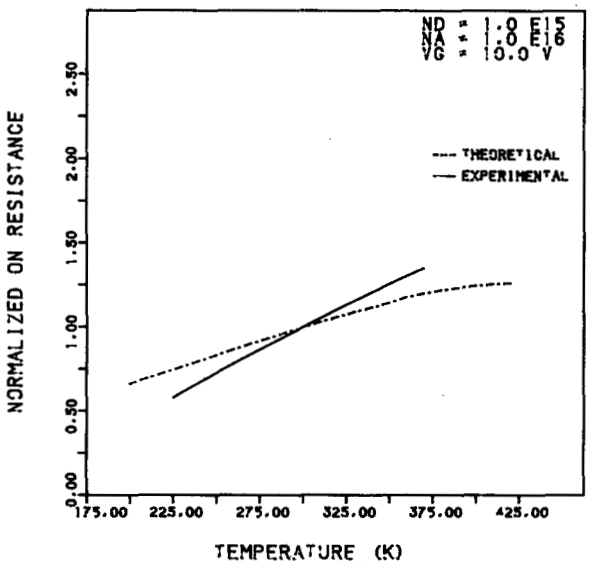

Fig. 6. Comparison of normalized R_{ON} with experimental results, for T = 175–425 K.

general behavior of R_{ON} and BV with temperature in the range 300–450 K, as derived from this model, has shown a good agreement with the experimental results given in [10]. Comparison of normalized R_{ON} with experimental results is shown in Fig. 6.

IV. Conclusions

The analysis shows that the LDMOS performance, in general, is degraded with the increase of temperature. The breakdown voltage rises slightly with temperature and such a rise is higher at higher donor doping levels. The device on-resistance also increases with temperature in the range 250 to 400 K before it falls back at higher temperatures. The analysis also shows that the ratio R_{ON}/BV, a measure of the device capability, is sensitive to temperature. However, it can become fairly insensitive to temperature at doping levels $N_D > 5 \times 10^{15}$ cm^{-3}.

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Interpretation of Forward Bias Behavior of Schottky Barriers

R. J. BENNETT

Abstract—**Forward bias current flow behavior of Schottky barriers provides important information about the contact through the saturation current and ideality factor. These parameters are usually determined by graphically determining the linear region of a plot of log I against V. This method is subject to the difficulty of determining a linear region if the contact exhibits any series resistance. However, a method is developed that unambiguously determines the three parameters, saturation current, ideality factor, and series resistance using a method suitable for a microcomputer.**

I. Introduction

It is well known [1] that the forward bias current flow of a Schottky barrier should yield a dependence, provided that $V > 3V_T$, of the form

$$I = I_s \exp(V/nV_T) \tag{1}$$

where I is the observed current for a bias V, $V_T = kT/q$ is the thermal voltage, and I_s and n are saturation current and ideality factor, respectively. Thus, it is usual to plot the (I, V) data on log-linear axes from which the intercept at $V = 0$ yields the constant I_s while the ideality factor can be determined from the slope [2], [3].

This method is difficult to apply at large forward bias where the voltage drop across any possible series resistance may become a significant proportion of the applied voltage. Such a condition has been discussed by Rhoderick [4] who indicated the consequence of erroneous determination of I_s and n. However, it is relatively simple to develop a method, based on a least squares method of fitting, that unambiguously yields optimal values of I_s, n, and R_s, where R_s is the series resistance that best fits the data.

II. Least Squares Interpretation

Let I_E be the current observed when an applied voltage V_A is provided across the device terminals. If the device has a series resistance R_S, then the actual barrier voltage V is given by

$$V = V_A - I_E R_s. \tag{2}$$

This is the voltage that should be used in (1). Thus, using (1)

$$V = nV_T \ln(I_E/I_s) \tag{3}$$

which can be written, using (2), as

$$V_A = I_E R_s + a \ln I_E + b \tag{4}$$

where

$$a = nV_T \quad \text{and} \quad b = -a \ln I_s. \tag{5}$$

Thus, if R_s, a, and b can be determined, then n and I_s can also be deduced.

Equation (4) predicts the applied voltage V_A required to yield a current I_E; thus, R_s, a, and b can be optimized by the method of least squares. For this purpose define

$$S = \sum_{i=1}^{m} \{I_{E_i} R_s + a \ln I_{E_i} + b - V_{E_i}\}^2 \tag{6}$$

Manuscript received June 18, 1986; revised September 30, 1986.
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IEEE Log Number 8612397.

where the summation is over m data pairs of experimentally determined I_E and V_E. The optimal combination of R_s and b would result in a minimum value of S, i.e.

$$\frac{\partial S}{\partial R_s} = \frac{\partial S}{\partial a} = \frac{\partial S}{\partial b} = 0. \tag{7}$$

This set of equations can be written as

$$(A)(X) = (R) \tag{8}$$

where

$$(A) = \begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{pmatrix} \tag{9}$$

$$(X) = \begin{pmatrix} R_s \\ a \\ b \end{pmatrix} \tag{10}$$

and

$$(R) = \begin{pmatrix} R_1 \\ R_2 \\ R_3 \end{pmatrix}. \tag{11}$$

It can be shown that the result of performing the differentiation required in (7) gives

$$a_{11} = \sum_{i=1}^{m} I_{Ei}^2; \quad a_{12} = \sum_{i=1}^{m} I_{Ei} \ln (I_{Ei}); \quad a_{13} = \sum_{i=1}^{m} I_{Ei}$$

$$a_{21} = \sum_{i=1}^{m} I_{Ei} \ln (I_{Ei}); \quad a_{22} = \sum_{i=1}^{m} \{\ln (I_{Ei})\}^2; \quad a_{23} = \sum_{i=1}^{m} \ln (I_{Ei})$$

$$a_{31} = \sum_{i=1}^{m} I_{Ei}; \quad a_{32} = \sum_{i=1}^{m} \ln (I_{Ei}); \quad a_{33} = m$$

while the right-hand cofactors in (11) become

$$R_1 = \sum_{i=1}^{m} I_{Ei} V_{Ei}; \quad R_2 = \sum_{i=1}^{m} V_{Ei} \ln (I_{Ei}); \quad R_3 = \sum_{i=1}^{m} V_{Ei}.$$

It is a relatively simple task to program a microcomputer to evaluate the summations and solve (8) for (X).

III. Application to Data from Cr-nSi Contacts

The effectiveness of the computer based fit can be seen from data [5] taken from forward bias behavior of chromium contacts, deposited by evaporation, onto ⟨111⟩ n-type silicon substrates. Measurements were taken, in isothermal sets, in the temperature range 180–380 K. The experimental data is plotted, on log-lin scales, in Fig. 1. It is apparent that the lower the temperature at which the data is measured, the less it is affected by the voltage drop across the series resistance. However, the high-temperature data is of importance since the greater the temperature range, the more accurate is the interpretation of temperature dependence.

Table I shows the best fit parameters for all of the temperatures at which measurements were taken, and these have been used to compute the curves shown in Fig. 1 in order that comparison with the experimental data can be easily seen. The agreement between the experimentally determined voltage V_E and the computed bias V_A is very good, and such agreement was found at all temperatures, including those high temperatures for which it would be impossible to choose an appropriate linear fit.

IV. Conclusion

A convenient and useful method for the interpretation of forward bias data from Schottky barriers has been given. The method is generally applicable and useful in resolving barrier parameters where the interpretation may be masked by effects of parasitic series resistance.

The method has been applied to chromium contacts to silicon over a wide temperature range. It has allowed the best fit values of saturation current and ideality factor to be determined for each isothermal set and show that the resulting fit had an rms error of less than 0.1 percent. The procedure would be a useful source of parameter values in the case of a fitting procedure that uses a multidimensional method such as simplex [6] as outlined by Boutrit *et al.* [7] since such methods depend upon provision of initial values.

Furthermore, the method of interpretation is probably simpler to implement than the graphical method of Norde [8], which either requires the implicit assumption that $n = 1$ or that the barrier height is temperature independent [9]. The benefit of the method outlined here is that best fit parameters can be obtained without such *a priori* assumptions.

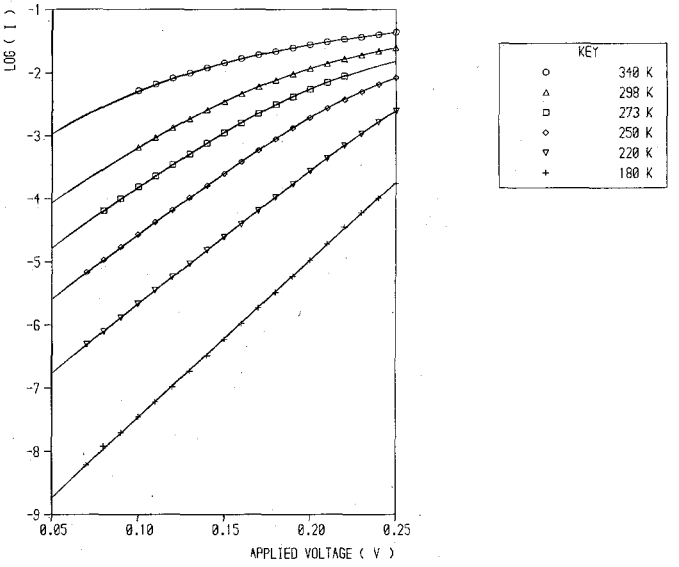

Fig. 1. Temperature dependence of forward bias current flow in Cr-nSi contacts.

TABLE I
BEST FIT PARAMETERS I_s, n, AND R_s FOR THE FULL TEMPERATURE RANGE

T	I_S(A)	n(T)	R_S (Ohms)
340	2.82×10^{-4}	1.023	2.32
298	1.49×10^{-5}	1.014	2.27
273	2.29×10^{-6}	1.01	2.74
250	2.96×10^{-7}	1.03	2.75
220	1.61×10^{-8}	1.079	2.35
180	1.09×10^{-10}	1.122	5.8

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A New Technology for Epitaxial II-VI Compound Semiconductor Devices

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***Abstract*—ZnS and ZnSe are grown by metalorganic chemical-vapor deposition over GaAs and GaAlAs chemi-stop layers on a GaAs substrate. The III-V layers allow selective chemical removal of the substrate in order to expose the ZnS. The device allows investigation of the electrical and optical properties of epitaxial wide-gap II-VI compounds in the absence of any influence from the substrate material.**

The metalorganic chemical-vapor deposition (MOCVD) technique is a potential route for producing epitaxial layers of wide-gap II-VI compounds for optoelectronic applications. Unfortunately, suitable substrates for homoepitaxy of these compounds have not been available, and for the epitaxial growth of ZnSe the most suitable substrate has been GaAs. However, this material limits the potential application of epitaxial wide-gap II-VI compounds in optoelectronic devices, due to its narrow bandgap and the difficulty in making direct electrical contact to both sides of the epitaxial layers.

Recently, light-emitting MIS devices with an MOCVD ZnS/ZnSe structure have been produced in which the ZnS i-layer also acted as a chemi-stop and allowed for the removal of the GaAs substrate in an H_2O_2/NH_3 solution [1], [2]. However, two important limitations arose from the fabrication process. Firstly, the ZnS remained exposed to the H_2O_2/NH_3 solution for several minutes during substrate removal, and the i-layer thickness could not be reduced below the 200–300 nm required for an efficient chemi-stop. This was greater than the optimum thickness for efficient minority-carrier injection [3]. Secondly, the need to make electrical contacts to both sides of the epitaxial II-VI layers resulted in a structure that was difficult to fabricate and required the use of very highly conducting ZnSe. In this correspondence a procedure that overcame both of these disadvantages is described.

The devices were prepared by MOCVD growth onto {100} orientated n-type Si-doped GaAs substrates. Prior to growth the substrates were etched in a 5:1:1 solution of $H_2SO_4:H_2O_2:H_2O$ for 20 min at 40°C. The first stage of the device production was the growth by MOCVD of the III-V epitaxial layers to enable the GaAs substrate to be selectively removed at a later stage. The substrates were baked out at 850°C for 20 min under an AsH_3 atmosphere, and the layers were then grown at 700°C. The first layer grown was a 2-μm-thick layer of $Ga_{1-x}Al_xAs$ with x greater than 0.6. This was followed by a capping layer of GaAs approximately 1 μm thick. The substrates were then transferred to a second MOCVD reactor for the deposition of the II-VI layers. Following a bake out at 500°C the ZnS i-layer and a 4-μm-thick ZnSe layer were deposited at 275°C. Several such structures were grown under identical conditions, while the thickness of the ZnS i-layer was varied in the range 50–200 nm. Although the GaAs/ZnS/ZnSe configuration involved considerable lattice mismatch (lattice constants 0.56535, 0.54093, and 0.56686 nm, respectively), reflection high-energy electron diffraction demonstrated that both the ZnS and ZnSe layers remained in good epitaxial register with the substrate.

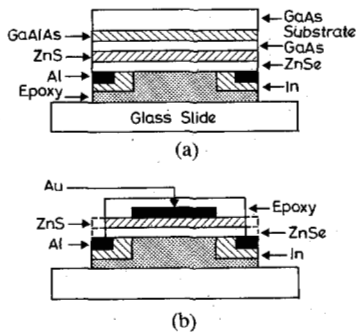

Fig. 1. Fabrication sequence for ZnS/ZnSe MIS device: (a) as-grown structure, (b) final device geometry (dotted region indicates structure prior to final etch to expose ohmic contacts).

Ohmic contacts were deposited onto the as-grown ZnSe by sequential thermal evaporations of aluminum and indium films with thicknesses of 100 and 200 nm, respectively. The structure was mounted on a glass slide with transparent epoxy resin in order to protect the contacts and to provide support for the epitaxial layers after substrate removal. This configuration is shown in Fig. 1(a). A solution of 95-percent H_2O_2 (100 volumes) and 5-percent NH_3 (35-percent solution) removed the GaAs substrate in 1–2 h, but was stopped at the GaAlAs layer due to the formation of a protective film of aluminum oxide [4]. This oxide film and the GaAlAs layer were subsequently etched in a 15-percent solution of HF. The GaAs layer exposed during this process dissolved more slowly and developed a very smooth chemically polished surface. The different wetting characteristics of the two surfaces provided a clear indication of the complete removal of the GaAlAs layer. The remaining GaAs was dissolved by a solution with the same composition as that used for substrate removal. Since the GaAs layer was extremely thin and dissolved uniformly, the first areas of ZnS to be revealed were only exposed to the solution for a few seconds. The control afforded by the use of chemi-stop layers allowed the thickness of the ZnS i-layer to be reduced to 50 nm. The exposed ZnS surface was extremely smooth, with no visible evidence of cracks or other defects.

A gold contact of diameter 1.5 mm was evaporated on to the ZnS and protected with epoxy resin as shown in Fig. 1(b). The ZnS remaining exposed was removed by a chemical polish composed of 35-percent phosphoric acid saturated with CrO_3, and 65-percent HCL [5]. This polish removed the ZnS within a few seconds and allowed subsequent uniform removal of the ZnSe in concentrated HNO_3, which dissolved the ZnSe, but passivated and hence did not attack the aluminum. The exposed aluminum allowed electrical connection to be made to the indium contacts on the underside of the device.

Electrical investigation of the structure confirmed that the characteristics were typical of an MIS device, and that effects attrib-

Manuscript received August 18, 1986; revised October 7, 1986. A. P. C. Jones was supported under a studentship by the Science and Engineering Research Council and the Royal Signals and Radar Establishment, Malvern.

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IEEE Log Number 8612479.