REVIEWS

Journal of Semiconductors
(2020) 41, 111404
doi: 10.1088/1674-4926/41/11/111404

A survey of high-speed high-resolution current steering DACs

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Abstract: Digital to analog converters (DAC) play an important role as a bridge connecting the analog world and the digital world. With the rapid development of wireless communication, wideband digital radar, and other emerging technologies, better performing high-speed high-resolution DACs are required. In those applications, signal bandwidth and high-frequency linearity often limited by data converters are the bottleneck of the system. This article reviews the state-of-the-art technologies of high-speed and high-resolution DACs reported in recent years. Comparisons are made between different architectures, circuit implementations and calibration techniques along with the figure of merit (FoM) results.

Key words: digital to analog converters; high-speed high-resolution; current steering

Citation: X Li and L Zhou, A survey of high-speed high-resolution current steering DACs[J]. *J. Semicond.*, 2020, 41(11), 111404. http://doi.org/10.1088/1674-4926/41/11/111404

1. Introduction

Digital to analog converters (DAC) are circuits that converse signals with information in bits to signals with information in their amplitude and time domain characteristics[1]. With the rapid development of high bandwidth applications, better performing high-speed high-resolution DACs are required[2, 3].

Due to the increasing demand for higher data rates, transmitters[4, 5], 5G base-station[6], software defined radio (SDR)[7], and other wireless communication systems have become the most significant application scenario for DACs with the sampling rate may exceed GS/s. For optical communication[8, 9], arbitrary wave generators (AWG)[10, 11] and some special applications, >10 GHz bandwidth is required. High resolution of DACs is also necessary for high quality of transmission signal or generated signal. Other important applications are in medical[12], instrument[13], military[14, 15], aerospace[16], and other fields. DACs have often become the bottleneck of the high frequency performance for these broadband systems. In this paper, we pay special attention on high-speed and high-resolution DACs according to the emerging application requirements. Nyquist DACs[17–19] combine voltage, charge, or current in a weighted combination to synthesize the final output. The core circuit of current steering DAC is usually composed of a group of weighted current sources and corresponding current switches[18]. And the output current can directly drive the load with no need for high-speed buffers[20], so higher output bandwidth and linearity than other types can be achieved. For this reason, the current steering architecture becomes the most qualified candidate for high-speed high-resolution DACs.

In the design of current steering DACs, the main challenge is to reduce the impact of static and dynamic errors. The static errors mainly come from the amplitude mismatch of current sources[21], which are caused by random errors and systematic errors[22]. In a given process technology, increasing the device size appropriately is an effective method for reducing random errors. However, systematic errors might be generated due to the large area[23]. To compensate the gradient errors, switching sequence optimization is a commonly used scheme[22, 23]. As the static performance of a segmented DAC is strongly dependent on the most significant bits (MSB) which are thermometer encoded, a suitable segmentation is also essential. In addition, the calibration techniques[24–28] of current sources can be introduced for higher linearity.

As the sampling rate and signal frequency increases, the dynamic errors begin to dominate. The dynamic errors include finite output impedance[21], timing mismatch[29], transient-induced nonlinearity[30], feed-through effect[31], clock jitter[21], etc. The finite output impedance is one of the important error sources. Unlike an ideal current source, the actual current source has finite output impedance, which makes the output impedance of the DAC vary with the input digital codes. To solve the problem, a multi-stage cascode structure and small bleeding current sources can be introduced[21]. Another major limitation of dynamic performance is the timing mismatch. The clock skews and the delay variation along the signal path can cause the unequal toggling time instants. A few techniques, such as timing calibration[32], dynamic element matching (DEM)[17], and pulsed-error pre-distortion (PEPD) scheme[33] have been proposed to resolve the timing errors. In addition, the signal-dependent switching operations cause the transient-induced nonlinearity. To reduce this effect, a quad-switch structure[34] and various return-to-zero (RZ) methods[30] can be adopted.

With the continuous development of IC design and process technology, a series of high-speed high-resolution DACs have been reported with a higher sampling rate, higher resolution, better performance, and lower power consumption. In Fig. 1, a comparison is made with the spurious free dynamic range (SFDR) performance versus sampling rate of high-

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Received 29 JUNE 2020; Revised 8 OCTOBER 2020.

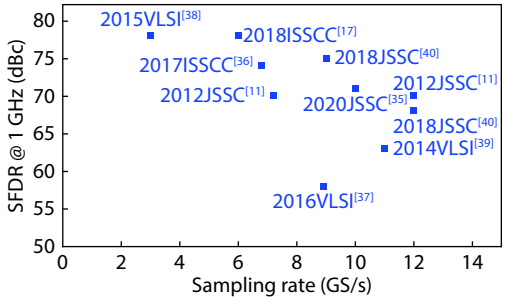

Fig. 1. (Color online) Performance comparison of state-of-the-art DACs: SFDR@1GHz vs. sampling rate.

speed high-resolution DACs published in the top conferences and journals in recent years.

Table 1 shows a more detailed performance summary and comparison with these state-of-the-art high-speed high-resolution current steering DACs. Figs. 2(a)–2(c) show the comparison of three common figures of merit (FoM) versus sampling rate with detailed definitions of the FoMs are given in Table 2.

This paper aims to provide a survey of cutting-edge high-speed high-resolution DACs with the mainstream technologies in circuit implementations. The rest of this paper is organized as follows. Section 2 presents a roughly description about the architecture of the current steering DACs. Section 3 outlines the dominating techniques in the subcircuit design, including the encoding segmentation, switching current source and the switch driver. Section 4 introduces the calibration and error reducing techniques for static and dynamic errors. The summary is given in Section 5.

2. Architecture of high-speed high-resolution DACs

The block diagram of a traditional high-speed high-resolution current steering DAC is shown in Fig. 3. In such an architecture, the input digital signal (binary bits) can be covert into unary bits by the thermometer encoder, or go through a delay equalizer to align the data stream for the segmented encoding. If a higher sampling rate is needed, multiplexers (MUX) can be introduced before or after the encoder[43, 44] to combine parallel data into double high-speed serial data. The on-off state of differential switches is controlled by the digital codes from the switch driver, and the weighted current sources are switched either to the positive or negative output node, forming the corresponding currents. Usually the DAC outputs a differential voltage on the resistive load. Some DAC products also integrate broadband balun within the chip. The clock generation circuit distributes clock signals to the digital cells or multiplexers, and the bias voltages of the entire current cell array are provided by a bias generation circuit[36, 37].

3. Subcircuit design

3.1. Encoding and segmentation

Encoder is one of the critical subcircuits. As mentioned before, a suitable encoding method is important for higher linearity design. According to the different current weights of current-steering cells, there are three encoding architectures of current steering DAC: binary-weighted architecture[20], thermometer-weighted architecture[45, 46], and segmented architecture[47].

Since the digital input of DAC is binary codes, the binary-weighted architecture is the most intuitive way. Refs. [18, 20] reveal that the advantages of this architecture are its simplicity. However, with the increase of N (resolution), the MSB-controlled current source differs greatly from the current source controlled by the least significant bits (LSB). To be precise, the maximum current is 2^{N-1} times that of the minimum current[18], resulting in a poor differential nonlinearity (DNL). To reduce the effects of static current source mismatch, a data-weighted averaging (DWA) algorithm[48] can be introduced, at the sacrifice of increasing the glitch energy in some cases.

The thermometer-weighted (unary-weighted) architecture is another option, which means that all switching currents have the same weight. This architecture can bring less disturbances on the output signal[46] at the cost of circuit complexity and power consumption[18]. Large layout dimensions increase routing complexity and lead to larger timing errors due to the presence of more parasitic components.

Generally speaking, the segmented architecture is the preferred one to combine the advantages of above architectures: the coarse bits use thermometer-type coding to reduce the requirements on matching and improve the linearity, while the fine bits using binary coding to reduce the complexity of current cells. As a result, the most important trade-off is the segment ratio[43].

Large coarse bits will introduce more parasitic capacitance, while large fine bits bringing the mismatch of current cells at the border. In Ref. [47], a design procedure of segmentation is outlined. The matching accuracy of the current source can be estimated based on the size of the transistors. After that, the maximum number of LSB section is determined according to the estimation and the yield requirements. Ref. [49] builds a model with the bandwidth and SFDR represented as a function of segmentation ratio for its hybrid DAC. Ref. [17] chooses a 6–10 segmentation in combination with the bounded INL calibration for a 16-bit DAC. In Ref. [35], the incoming data is decoded to the 3–3–3–5 (unary–unary–unary–binary) segmentation for a compact layout. In short, the segmentation design is not constant for a specific resolution, a compromise between good static and dynamic specifications versus power and area should be found[18].

3.2. Switching current source cell design

In current steering DACs, the performance of switching current source determines the performance of the DAC. A typical structure of the switching current source cell is shown in Fig. 4, which contains a cascoded current source, differential current switches, thick-oxide output cascodes and bleeding currents[21].

As discussed earlier, the finite output impedance of the current source is one of the important factors that affect the dynamic performance. For this reason, the thick-oxide cascode devices (M4/M5) are added between the switch (M2/M3) and the output node to reduce the effect at low frequencies[21], which also serve as the protecting devices for the switching pairs. The cascode device (M1) plays a role of isolating the current source (M0) from the switches[43, 44], so as to avoid the influence of the parasitic capacitance of the current source on the fast switching differential pairs. At high fre-

Table 1. Performance summary and comparison with state-of-the-art high-speed high-resolution DACs.

Parameter	Ref. [4]	Ref. [11]	Ref. [17]	Ref. [30]	Ref. [35]	Ref. [36]	Ref. [37]	Ref. [38]	Ref. [39]	Ref. [40]
Process (nm)	28	130	16	40	28	16	40	65	28	65
Resolution (bit)	13	14/12	16	12	14	14	14	16	9	16
Sampling rate (GS/s)	9	7.2/12	6	1.6	10	6.8	8.9	10	11	9/12
SFDR@Nyquist frequency (dBc)	N/A	67/55	67	70	65	62	50	69 @3GS/s	51	56/52
IM3@DC-Nyquist frequency (dBc)	<–45	N/A	<–82	<–70	<–70	<–71	<–65	<–73 @3GS/s	<–51	<–67/<–67
NSD (dBm/Hz)	N/A	–161/–159	–162 @2.6GHz	–150 @800MHz	–158 @5GHz	–160	N/A	N/A	N/A	–130 @6GHz
Power (mW)	360	N/A	350	40	162	330	1200	800	110	758/1065
Area (mm^2)	1.16	N/A	0.52	0.016	0.07	0.855	N/A	N/A	0.04	0.97
FoM1 (GHz/mW)	N/A	N/A	6.5×10^5	4.4×10^5	4.5×10^5	2.7×10^5	5.6×10^3	2.5×10^5	3.8×10^4	6.3×10^4/ 1.9×10^4
FoM2 (GHz/mW)	N/A	N/A	18.7	102.4	10.1	12.4	1.4	16.4	27.9	8.6/6.2
FoM3(GHz/(mW·mm^2))	N/A	N/A	2.4×10^6	2.6×10^7	2.4×10^6	2.4×10^5	N/A	N/A	3.6×10^5	5.8×10^5/ 4.2×10^5

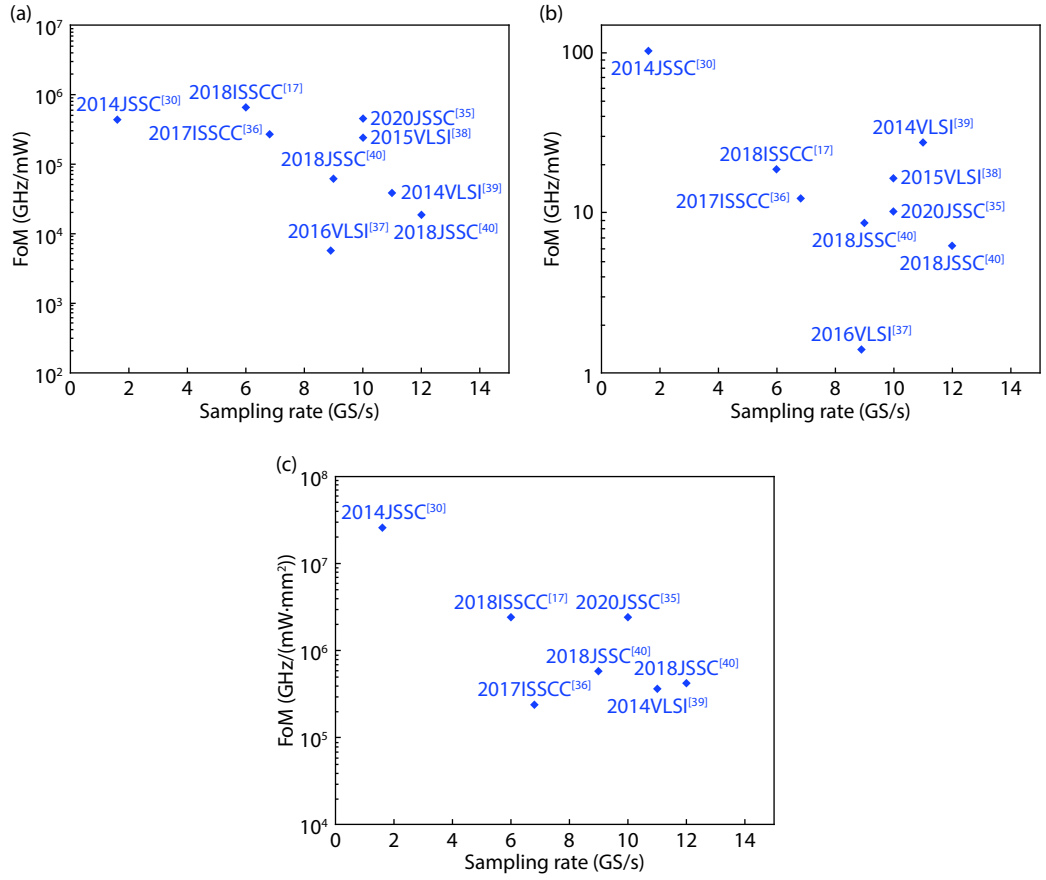

Fig. 2. (Color online) Performance comparison of state-of-the-art DACs: (a) FoM1, (b) FoM2, (c) FoM3 versus sampling rate.

Table 2. Detailed definitions of DAC FoMs.

	FoM1	FoM2	FoM3
Definition	$\frac{2^{\frac{SFDR_{Best}-1.76}{6.02}}\times 2^{\frac{SFDR_{Worst}-1.76}{6.02}}\times f_{clk}}{P_{total}-P_{load}}$	$\frac{2^N\times f_s@6(N-1)}{P_{total}}$	$\frac{2^{2N}\times f_s@6(N-1)}{P_{total}\times Area}$
Reference	[30]	[41]	[42]
Explanation	$SFDR_{Best}$/$SFDR_{worst}$: Best/Worst measured SFDR in whole Nyquist bandwidth; f_{clk}: Sampling rate; P_{total}/P_{load}: Power consumption of the whole DAC/load; N: Resolution; f_s@6(N–1): Output signal frequency where the SFDR has dropped with 6 dB (= 1 bit) in comparison with the expected result (≈ 6N) (Note: If the measured SFDR cannot reach 6(N–1), 0.1 GHz is selected here for calculation); Area: The core area of the DAC.		

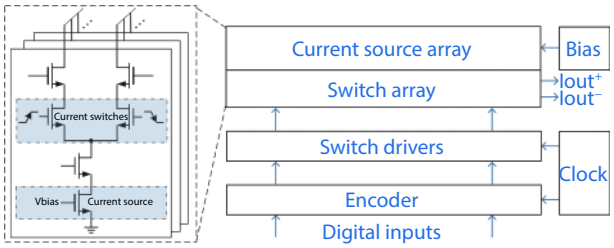

Fig. 3. (Color online) Block diagram of a high-speed high-resolution current steering DAC with a typical switching current cell.

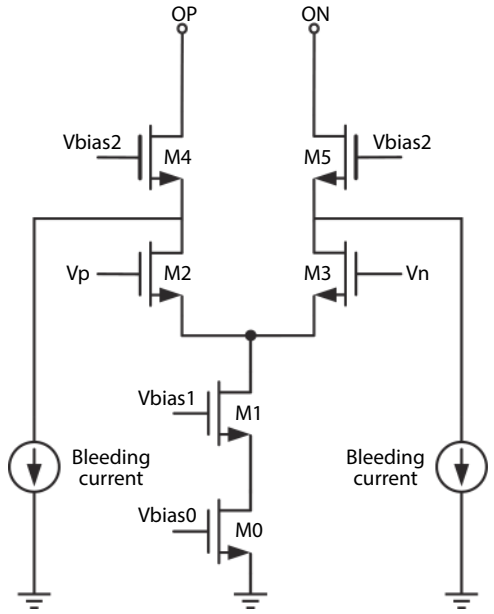

Fig. 4. A typical switching current cell proposed in Ref. [21].

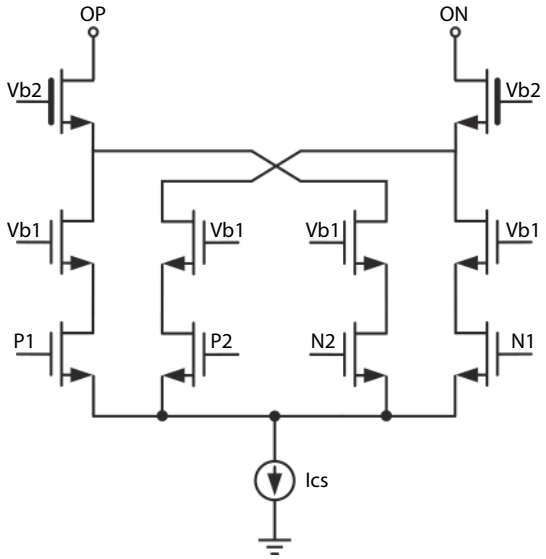

Fig. 5. Quad-switching current cell with switch cascodes reported in Ref. [38].

quencies, the signal dependence of the output impedance will be more severe as the impendence shows a first-order roll-off with frequency[21]. Ref. [21] also proposed a structure with bleeding current sources to overcome the finite output impedance which are now widely used[4, 17, 38]. Even in the off state, a small current pass through the cascode transistor to make it in a weak conduction state, so as to balance the output impedance. In addition, Ref. [38] incorporates core device cascodes in between the switches and the thick-oxide output cascode devices as depicted in Fig. 5, which serves to isolate the data-dependent distortion of the output cascode devices from the switches, reducing the effect of internal coupling.

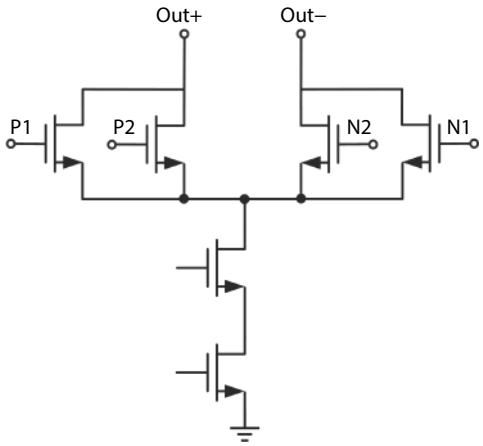

Fig. 6. A simplified quad-switch cell proposed in Ref. [34].

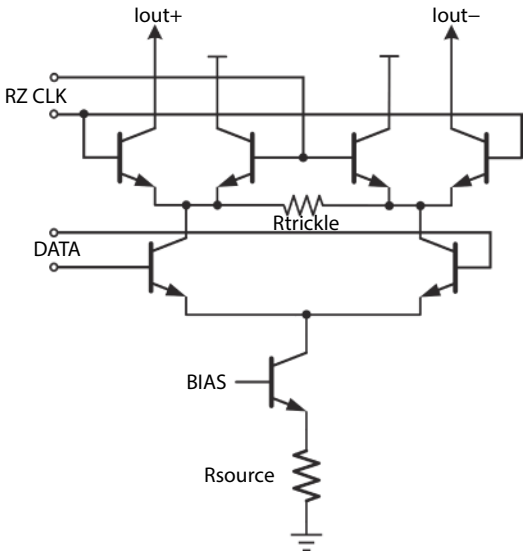

Fig. 7. RZ current cell with resampling switches proposed in Ref. [11].

In the design of switching current source cell, it is crucial to reduce the signal-dependence of switch behavior[37]. A few techniques are proposed including the quad-switch structure[34, 50] and the RZ current switches[51, 52].

Ref. [34] proposed a quad-switch as presented in Fig. 6, using two pairs of differential switches, which are activated alternately in every clock cycle. Even if there is no data change, the switching event will occur. The code-independent switching event improves the distortion performance at high frequency. Engel *et al.*[38] of ADI adopted the quad-switch in a 16-bit 10GS/s DAC as shown before in Fig. 5. Ref. [40] combines the quad-switch and the interleaved DAC structure in a 9-bit 11GS/s DAC to suppress the main dynamic error of the current-steering DAC. A major drawback of the quad-switch is the increased power consumption due to the increased switching frequency and twice as many switching transistors as ordinary differential switches.

RZ switch is also an effective method to reduce the signal-dependent nonlinearity, as it can insert a zero output

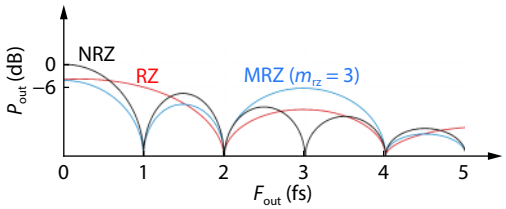

Fig. 8. (Color online) Magnitude of the frequency response for NRZ, RZ, and MRZ waveforms reported in Ref. [53].

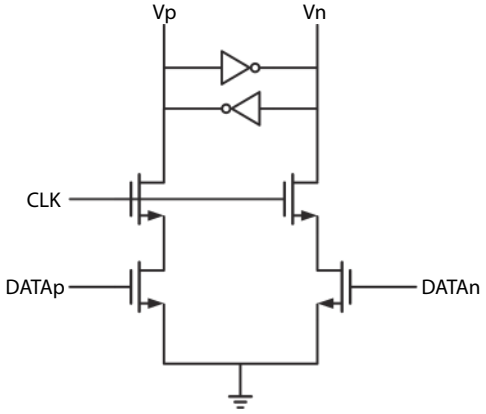

Fig. 9. A typical fast latch proposed in Ref. [21]

state between two consecutive signals[30]. This method allows the output transition to be independent and eliminates the distortion caused by uneven pulse duration. Ref. [51] proposed to adopt track and reset switches controlled by means of a two-phase clock generator, achieving a waveform composed of the signal value during the track and zero during the reset. Ref. [11] also utilized the RZ action. Two sub-DACs, with resampling switches illustrated in Fig. 7, produce two complementary return-to-zero waveforms, and synthesis a non-return-to-zero (NRZ) final waveform for better linearity at high frequencies. The output frequency can be synthesized in the second Nyquist zone for RZ DAC, and a multiple-return-to-zero (MRZ) architecture combining RZ and mixing DAC was proposed in Ref. [53], which can get a higher output with similar implementation, as the essence of this approach is to increase the RZ frequency. The frequency response for NRZ, RZ, and MRZ (m_{rz} = f_{mrz}/f_{rz}) waveforms are plotted in Fig. 8. One drawback of RZ switch is the data-dependent noise could still exist as the pulse may not switch to full level. Moreover, the jitter tolerance, the high switching frequency, and the low power efficiency limit the dynamic performance[34].

3.3. Switch driver circuit design

The switch driver is the transition cell from the digital domain to the analog domain[2], and is important for maintaining linearity, especially at high output frequencies[37]. The switch driver is always composed of latches or flip-flops, which can provide positive feedback and maintain latching status. In addition, the switch driver should be designed to reduce the clock feed-through effect and adjust the cross-point of the complementary control signals[54, 55].

Ref. [21] proposed a typical switch gate driving, which creates a steep transition and has a short clock-to-output delay. This structure, as shown in Fig. 9, is also applied in Refs. [2, 56]. This pseudo-differential CMOS latch has advantages on driving the analog current source cell directly, and providing the final timing for the data input of the current source cells. To accelerate the signal transition further, PMOS transistors are added in Ref. [57], getting the capability of both pull-up and pull-down. The simplified schematic of the high-speed latch is demonstrated in Fig. 10, while the similar structure demonstrated in Fig. 11 may produce faster rise/fall times owing to the devices M1–M4[37].

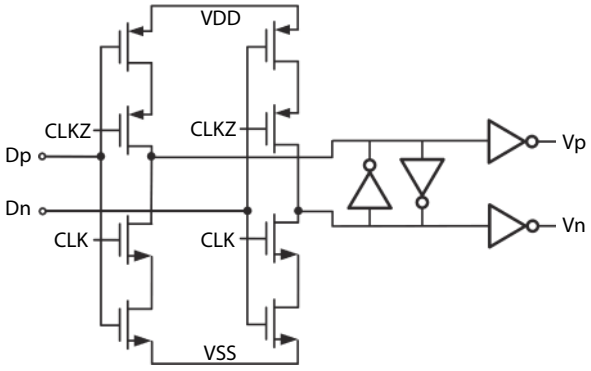

Fig. 10. High-speed latch presented in Ref. [57].

For the switch driver design, a critical problem is the mismatch of the signal-dependent switching timing. The latches driving the current source cells are intrinsically nonstatic, and the signal generated by the final latches will produce supply ripples[56], resulting in timing mismatch. For this reason, Spiridon *et al.*[56] of Broadcom proposed an effective method: establishing a dummy path, as illustrated in Fig. 12. When the main latch is not triggered, the dummy latch is triggered with dummy data. Since they share the same supply, and at each clock cycle the state changes in interface cell, the signal-dependent supply induced pattern is broken.

Erdmann *et al.*[36] of Xilinx adopted this method to obtain the current of switch independent of data. The data and dummy-data drive the main and dummy bit-slices made of 3 differential latches. In addition, in order to achieve a dual-mode DAC, the final latch needs to accomplish both the retiming of data in the normal mode and the XOR operation of data and clock in the mixing mode.

Ravinuthula *et al.*[37] of TI used differential clock CMOS inverter pairs to form their switch driver. The characteristic of the proposed circuit is that it takes advantage of the above-mentioned technique, using dummy data to switch the replica driver. The diagram of DAC output stack with the novel latch shown in Fig. 11. As a result, the effective path and the dummy path are complementary, and the influence of supply ripple on current is greatly reduced.

In addition, the CML latch configuration is commonly used for low-swing differential operation at high frequencies and small disturbance on the power supply. A master–slave CML latch was applied in Ref. [58]. The digital output of the encoder will be latched first by master latches, then by slave latches, as shown in Fig. 13. The usage of two latch stages enables precise timing and steep edges to minimize the timing errors. The double-edge switch driver can be introduced to reduce the input clock frequency, and one of its major drawbacks is the memory effect, or the inter-symbol interference (ISI). Since the last operation may affect the next working state, Ref. [59] adds reset transistors to the common source node of the CML switch driver to form an enhanced reset cir-

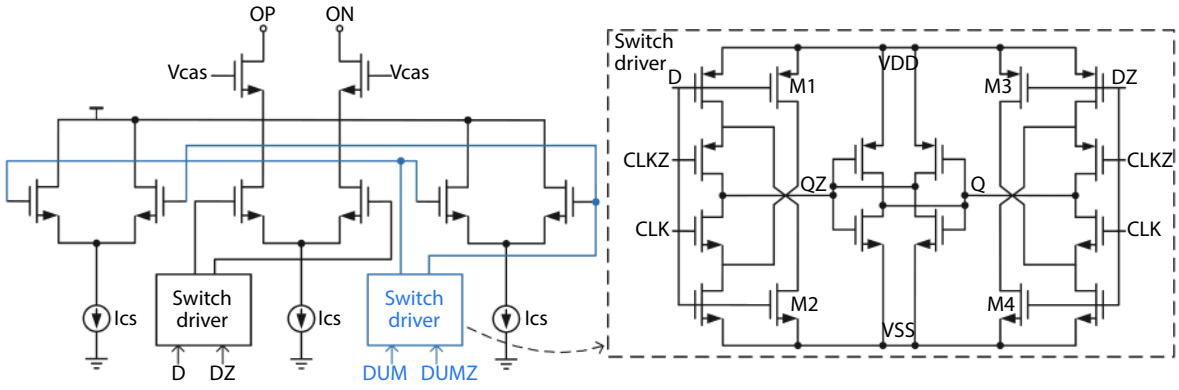

Fig. 11. DAC output stack, with the switch driver proposed in Ref. [37].

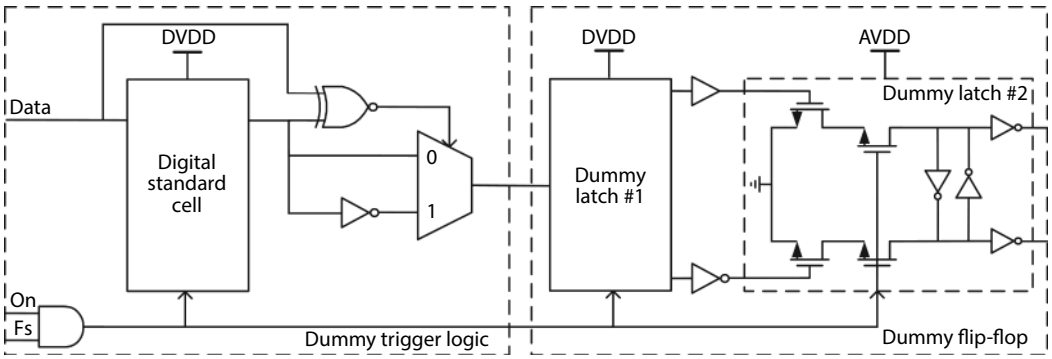

Fig. 12. Block diagram of dummy trigger proposed in Ref. [56].

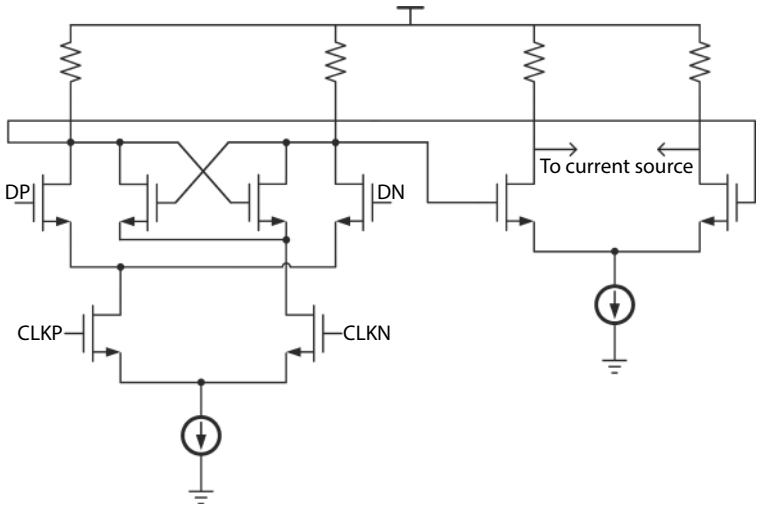

Fig. 13. Master-slave latch presented in Ref. [58].

cuit in a 14-bit 8GS/s DAC. As depicted in Fig. 14, when one branch is in off state, the associated reset transistor charges the common node to a fixed voltage.

4. Calibration and error reducing techniques

4.1. Static error calibration techniques

In current steering DACs, the main goal of static error calibration is reducing the amplitude mismatch between current sources.

Calibration techniques can be divided into foreground calibration[24] and background calibration[25, 26]. The foreground calibration technique usually needs to interrupt the operation process, and the background calibration can achieve continuous calibration at the cost of additional power consuming and extra spurious[27].

While the foreground calibration is performed only once, the background retriggers the current cell periodically. It not only eliminates the static mismatch, but also tracks the error slow varying with time, which is related to the bias conditions and chip temperature fluctuations[26, 60]. In Ref. [25], a digital background self-calibration technique is proposed. The calibration loop is achieved with an 8-bit auxiliary calibration DAC (CAL_DAC) current source in parallel with a main current source. The digital trimming memory is directly connected to its corresponding CAL_DAC, so it can be compensated

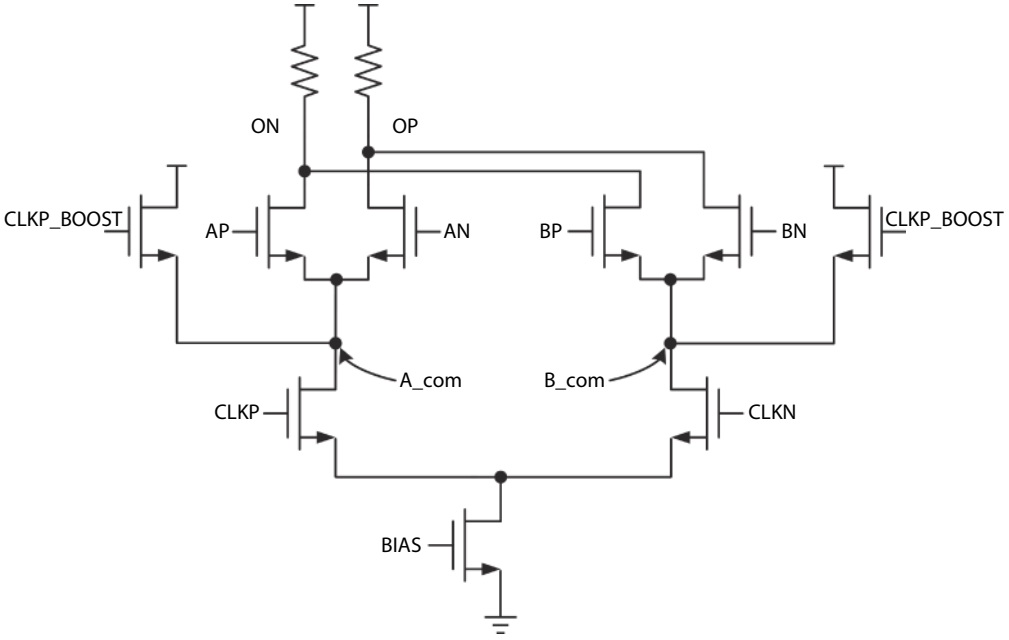

Fig. 14. Double-edge current switch driver with enhanced reset circuit reported in Ref. [59].

without converting digital calibration value into analog form, obtaining simple implementation and low power dissipation. To reduce the noise generated by the periodic calibration process, Ref. [60] introduced floating current cells without switching-in and out of DAC elements into calibration mode periodically. In Ref. [26], a method of time-domain randomization, which can convert the discrete calibration spurs into wideband noise, was proposed to eliminate spurious tones and reducing power consumption compared with Ref. [60].

Another attractive option for static error calibration is the foreground calibration technique. A successive approximation register (SAR) logic and a CAL_DAC can be introduced[17, 24]. In Ref. [24], the current source to be calibrated is measured against a master reference current I_{ref}. The CAL_DAC in parallel with the master current source is used to inject a small correction current to make the difference as close to zero as possible. The additional circuit for calibration is static during normal operation, neither consuming power nor injecting noise into the main signal path.

The main constraints of the foreground calibration techniques are their sensitivity to the temperature and supply voltage variations. To track the current source mismatch change with temperature, Zhu *et al.*[27] of ADI analyzed the two factors that caused the current source mismatch: threshold voltage mismatch and current factor mismatch, and the expression of the current source mismatch was given by

$$\Delta I = \frac{\Delta\beta}{\beta} I + g_{\mathrm{m}} \left(-\Delta V_{\mathrm{TH}}\right), \tag{1}$$

where I is the nominal bias current and $g_{\mathrm{m}} = \sqrt{2\mu C_{\mathrm{ox}} (W/L) I}$ is the nominal transconductance. According to the formula obtained, the calibration only focused on the dominant component of the mismatch current: $g_{\mathrm{m}}(-\Delta V_{\mathrm{TH}})$. The specific method is generating current which is proportional to $g_{\mathrm{m}} V_{\mathrm{ref}}$, where V_{ref} is a constant voltage derived from the bandgap voltage, ensuring that the output current of the CAL_DAC is equal to $g_{\mathrm{m}}(T)\,\Delta V_{\mathrm{TH}}$, so that the calibration current has the same temperature dependence with the assumed mismatch, hence improving matching to temperature variations.

However, the scheme explained above only considers the main component of the mismatch current. For greater accuracy, Zhu *et al.*[28] proposed a two-parameter calibration technique using two CAL_DACs, as shown in Fig. 15. In this technique, the calibration method of the inherent current in Ref. [24] is regarded as the calibration for I component only; at the same time, the scheme in Ref. [27] is used to calibrate the g_{m} component. This two-parameter calibration technique was applied to a 16-bit 10GS/s DAC[38], and the measurement results show a good matching across the temperature range from –40 to 85 °C. Table 3 summarized the INL/DNL at the calibration temperature (40 °C) and the standard deviations of the temperature drift[27, 28] of above foreground calibration techniques.

4.2. Dynamic error reducing techniques

With the improvement of the sampling rate and output bandwidth, the dynamic errors become more dominant on the high frequency performance. The DEM technique[61–63], RZ technique[51–53], the layout arrangement technique[35, 64], and some new proposed techniques are presented as follows.

DEM technique is an effective technique which can suppress both static and dynamic errors. Its principle is to select the circuit cell by randomization, which refers to the random permutation of switches[61]. This technique enables the amplitude and timing errors to be averaged over the entire time domain[17], and the harmonic components of the errors are converted into noises. The disadvantage of this technique is that the complexity of circuit increases significantly, and the complex digital logic may become a limitation for the improvement of DAC. Consequently, a good DEM technique requires less circuit overhead and complexity. In Ref. [17], a 2D thermometer-coded DEM technique was used to combine column and row thermometer-coded logic with local DEM to minimize glitch energy and greatly increase the randomness at an ap-

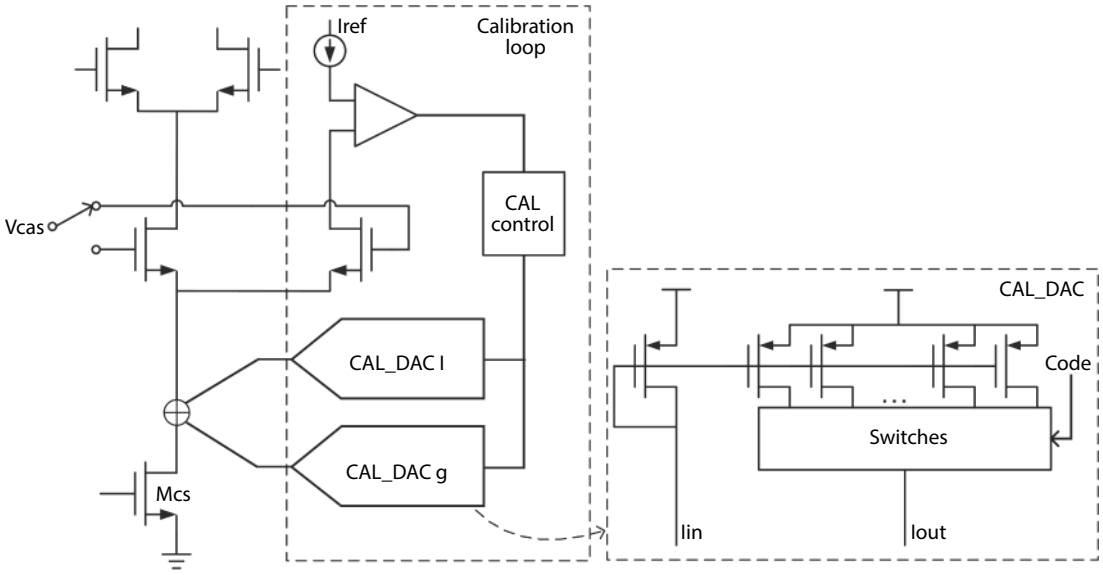

Fig. 15. Two-parameter calibration loop configuration and CAL_DACs proposed in Ref. [28].

Table 3. INL, DNL and temperature drift summary of proposed foreground calibration techniques.

Parameter	INL at 40 °C (14-bit level LSB)	DNL at 40 °C (14-bit level LSB)	Temperature drift 1σ (LSB)
No CAL	6.02	3.33	1.6
Ref. [24]	0.20	0.16	1.6
Ref. [27]	0.23	0.16	0.8
Ref. [28]	N/A	N/A	0.6

propriate hardware cost. Moreover, Ref. [63] reveals the DEM techniques increase the element switching activity, and the extra transitions introduce more ISI errors that result in harmonic distortions. The authors proposed new DEM algorithms with higher randomness and minimum element transition rate, while solving the problems of static mismatch and dynamic ISI errors.

RZ technique has been mentioned in Section 3.2, which means that the output tracks the signal once it has settled and then returns to zero. A typical RZ switching current cell was presented in Fig. 7 and the ideal RZ output is a square waveform composed of the signal value and zero in a clock cycle[51]. RZ technique can be divided into analog return-to-zero (ARZ) and digital return-to-zero (DRZ). ARZ[51] can be realized with reset transistors added at the output terminals, which can shield the effect of the transient-induced nonlinearity of the switches. The defect of this method is the excessive parasitic capacitance and area, and the DRZ technique[30, 65] gets more attention. It realizes equivalent return-to-zero by changing the control codes of the differential switches. Ref. [65] proposed a digital random return-to-zero (DRRZ) technique based on DRZ, to mitigate the impact of switching transients on the DAC dynamic performance. The DRRZ technique is adopted in a 12-bit 1.25 GS/s DAC[66].

DEM and DRZ can be used in combination[30, 67]. In Ref. [67], a time-relaxed interleaving return-to-zero DEM (TRI-DEMRZ) technique was proposed to implement a DEM decoder with enough randomization and less code-dependent switching glitches in a 14-bit 1GS/s DAC. Ref. [30] also proposed a dynamic-element-matching and digital return-to-zero (DEMDRZ) technique, which randomizes the code-dependent distortion by random numbers, so as to further suppress the current-source mismatch and transient-induced nonlinearity. Ref. [35] uses DEM and DRZ techniques to design a 14-bit 10 GS/s DAC, achieving > 64 dB SFDR over the entire Nyquist bandwidth.

The layout arrangement technique is also a significant option to mitigate the systematic matching errors. To reduce the timing skew induced between current cells, Ref. [35] applied the Q^2 random walk arrangement with a common centroid proposed in Ref. [64], and then described a novel method named concentric parallelogram routing (CPR). The routing lengths used to connect the sub-cells can be equal, achieving a lower gradient mismatch error. In Ref. [53], a vertically stacked tree (VST) structure forms an H-tree for each cell was proposed to provide identical path lengths to the output summing node, thereby minimizing variations in amplitude and phase.

A number of excellent dynamic error reducing techniques are proposed in recent years. To break the linearity limitation of Nyquist DAC, a hybrid DAC architecture with a Nyquist path and an oversampling path was proposed by Su *et al.*[49]. Fig. 16 illustrates the basic concept of the dual-rate hybrid DAC architecture. The MSB path operates at the Nyquist rate, while the LSB path operates at some oversampling rate via a delta–sigma modulator (DSM). This architecture leads to a better dynamic performance owing to the minimal analog complexity and the DSM dithering in the LSB path. Another delta–sigma assisted pre-distortion scheme is proposed to compensate for current mismatches in the MSB path through the delta–sigma modulated LSB path without using any other current cell, thereby achieving small simulation complexity and extremely high linearity[31]. Moreover, this technique can be used in combination with a DWA algorithm to further

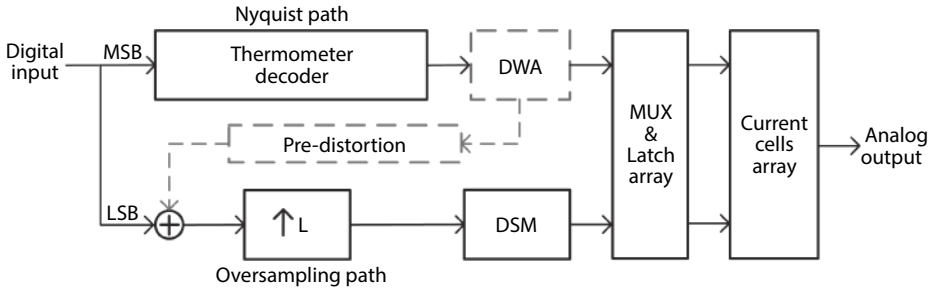

Fig. 16. Conceptual block diagram of a dual-rate hybrid DAC architecture proposed in Ref. [49].

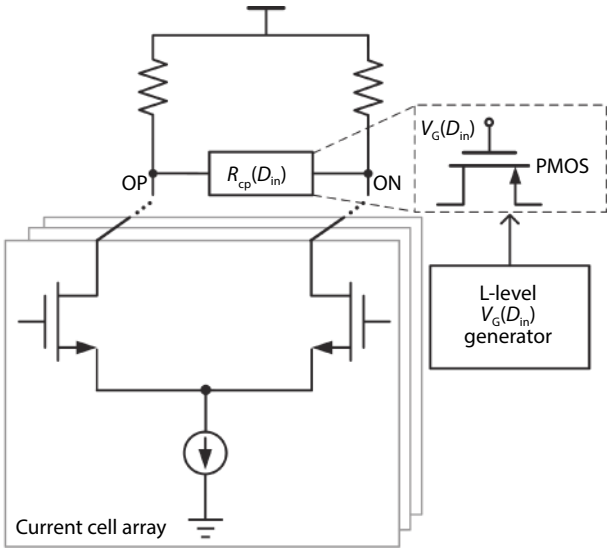

Fig. 17. OIC technique with compensation resistor proposed in Ref. [35].

randomize other dynamic errors, such as time skews. In order to further widen the DAC bandwidth, Su *et al.* proposed an in-band noise-cancellation scheme and a pulsed-error predistortion (PEPD) scheme, to tackle both amplitude and timing errors together without penalty on noise performance[33]. Nevertheless, this only synthesizes the baseband signal and is difficult when covering wide RF spectra. Ref. [40] proposed a hybrid DAC with a tunable bandpass DSM, to addresses the constraints for high-linearity and low-noise waveform synthesis over wide frequency spans. The implemented DAC achieves IM3 of –85 to –67 dBc over the Nyquist band, and the SFDR remains > 60 dBc up to a 4.2 GHz signal frequency at 12 GS/s.

To mitigate the data-dependent switching distortions, a random pairwise swapping (RPS) technique was proposed in Ref. [68], which reduces the intermodulation distortions between the element transition rate and the output-dependent unit switching. RPS randomly swaps the switching control signals of paired switching units in the random DEM decoding, resulting a 5–12 dB SFDR improvement at 1.0 GS/s.

To remedy the finite output impedance effect at high frequencies, an output impedance compensation (OIC) technique was proposed in Ref. [35], which introduces a data-dependent compensation resistor, $R_{cp}(D_{in})$. The current induced by the R_{cp} changes the current through the load resistors for compensating the distortion. The R_{cp} can be approximated by a PMOS biased with a data-dependent gate voltage $V_G(D_{in})$, as shown in Fig. 17. Notably, the OIC technique enables the use of non-cascoded current cells. A 14-bit 10 GS/s DAC with > 65 dBc SFDR over the entire Nyquist bandwidth was achieved by using the simple PMOS-based $R_{cp}(D_{in})$ with two-level $V_G(D_{in})$.

5. Conclusion

Nowadays high-speed high-resolution DACs have been widely applied. In 5G communication, optical communication, and more broadband applications, the DAC becomes a bottleneck that limits the performance of the system. The state-of-the-art high-speed high-resolution current steering DACs are reviewed in this paper, with focus on the subcircuit design and error reducing techniques. Comparisons are made between different architectures, circuit implementations and calibration techniques along with three common FoM results.

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