Available online at www.sciencedirect.com
SCIENCE DIRECT®
Thin Solid Films 510 (2006) 320–324
thin solid films
www.elsevier.com/locate/tsf

Effect of back-contact barrier on thin-film CdTe solar cells

S.H. Demtsu *, J.R. Sites

Department of Physics, Colorado State University, Fort Collins, CO 80523, USA

Received 12 October 2005; received in revised form 9 December 2005; accepted 6 January 2006
Available online 20 February 2006

Abstract

The presence of a back-contact barrier affects the current–voltage characteristics of thin-film CdS/CdTe/metal solar cells primarily by impeding hole transport, a current-limiting effect commonly referred to as "rollover." In this work, the CdS/CdTe solar cell with a CdTe/metal back-contact barrier is modeled by two opposite polarity diodes in series. Analytic simulations are fitted to the measured current–voltage curve, the voltage distribution between the two diodes is shown under different conditions, and the back-contact barrier height is extracted. Room-temperature barrier heights exceeding 0.5 eV will generally result in significant fill-factor reduction.

Keywords: Cadmium telluride; Schottky barrier; Solar cells; Contacts; Electrical properties; Measurements

1. Introduction

A stable back contact that is not significantly rectifying and has a low resistance is essential for good performance and long-term stability of CdS/CdTe solar cells. Since CdTe is a p-type semiconductor with a high electron affinity ($\chi = 4.5$ eV) and high band gap (1.5 eV), a high work-function metal is required to make good ohmic contact to CdTe. Most metals, however, do not have sufficiently high work-functions and therefore form Schottky-barrier contacts to CdTe absorber layers. When the Fermi level at the metal/CdTe interface is pinned by surface states, a metal with a reasonably high work-function might not make an ohmic contact. The presence of a back-contact barrier can significantly affect the current–voltage characteristics of a CdTe cell, primarily by impeding hole transport. This mechanism is one of the causes of the current-limiting effect referred to as "rollover." Prior to deposition of a back contact material, the CdTe surface can be chemically etched to create a Te-rich surface, and doping the surface with Cu has been found to improve the contact properties [1–5]. However, the diffusion of Cu^+ ions from the back-contact region towards the main junction during long-term stability studies may result in a Cu-depleted rectifying back contact.

In earlier work, Stollwerck and Sites showed that CdTe cell with a back contact barrier could be modeled by a series connection of two diodes with opposite polarities [6]: the CdS/CdTe main junction diode, and the CdTe/metal-contact back diode. Based on a similar two-diode model, Niemegeers and Burgelman developed a simple analytical theory that explains the observed rollover in thin-film CdTe solar cells [7]. Other groups have also studied the current limiting effect of the back contact on the performance of CdTe solar cells [8–10]. However, the effects of series resistance, and the leakage conductance at the main and back diodes were not included in the simplified model nor has been there a straightforward method to extract the barrier height from measured current–voltage curves. McCandless et al. have used a two-diode model to study the effect of back contact, and the barrier height was determined from the temperature dependence of the series resistance [11].

The current work investigates the details of the CdTe/metal contact using a similar two-diode model (Fig. 1a), and a straightforward technique that extracts the barrier height from room temperature current–voltage characteristics is presented. To simulate the behavior of a real CdS/CdTe/metal device, the effect of a lumped series resistance of the device, and the shunt resistances of the main and the back diodes are included. In the simulation, parameters are systematically changed to yield current–voltage characteristics that match the measured curves. With this approach, the corresponding back barrier height is

* Corresponding author.
E-mail address: samdem@lamar.colostate.edu (S.H. Demtsu).

0040-6090/$ - see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2006.01.004

extracted. Moreover, the voltage distribution between the two diodes as a function of the applied bias for different conditions is calculated.

2. CdTe/metal contact

The contact barrier height, Φ_b, for holes at the metal/semiconductor interface when the Fermi level is not pinned by interface states is given by the difference between the valence band edge and the Fermi energy in the metal.

$$\Phi_b = E_g/q + \chi - \varphi_m \tag{1}$$

where E_g is the band gap, χ is electron affinity of p-type CdTe, and φ_m is work function of the back contact metal.

Assuming that thermionic emission current is the dominant mechanism at the CdTe/metal interface, the hole current can be written as

$$J_b = -J_{bo}(e^{qV_b/kT} - 1) \tag{2}$$

(It should be noted that the polarity of the CdTe/metal junction is opposite that of the main junction, and hence the negative sign convention for its current). In Eq. (2), q is electronic charge, k is Boltzmann constant, T is temperature, V_b is the voltage across back contact, and the saturation current J_{bo} can be expressed as [12]

$$J_{bo} = A^* T^2 e^{-q\Phi_b/kT} \tag{3}$$

where T is temperature, Φ_b is the barrier height and $A*$ is the effective Richardson constant:

$$A^* = 4\pi q m^* k^2/h^3 = qN_v(k/2\pi m^* T^3)^{1/2} \tag{4}$$

Here, h is Planck's constant, N_v is the effective density of states in the valence band, and $m*$ is effective mass. Eqs. (3) and (4) yield

$$J_{bo} = qv_R N_v e^{-q\Phi_b/kT} \tag{5}$$

The Richardson velocity V_R is the thermal velocity given by

$$V_R = \frac{\int_0^\infty v\, e^{-m^* v^2/2kT} dv}{\int_{-\infty}^\infty e^{-m^* v^2/2kT} dv} = \frac{1}{\sqrt{2\pi}}\sqrt{\frac{kT}{m^*}} \tag{6}$$

and is proportional to $T^{1/2}$. For CdTe, the effective mass of holes is approximately 0.8 m_e [13], and hence the Richardson velocity is approximately 3×10^7 cm/s at room temperature.

The hole concentration in the quasi-neutral region of a p-type semiconductor is given by

$$p = N_v e^{-(E_F - E_v)/kT} \tag{7}$$

where E_F and E_v are the Fermi and valence band energy, respectively. The back contact saturation current J_{bo} given in Eq. (5) can be expressed in terms of the hole carrier density by solving for N_v from Eq. (7) and substituting it into Eq. (5).

$$J_{bo} = qv_R p e^{-[q\Phi_b - (E_F - E_v)]/kT} = qv_R p e^{-q\Phi_d/kT} \tag{8}$$

where $\Phi_b = \Phi_d + (E_F - E_v)$ is the energy difference between the Fermi level and the valence band edge at the metal interface, whereas Φ_d is the energy difference between the valence band in the bulk and valence band edge of the semiconductor.

The current-limiting effect, rollover, is attributed to the back contact barrier height (Φ_b) given by Eq. (1), and occurs because the total current saturates at a current equal to J_{bo} [7], given by Eq. (5).

3. Simulation and discussion

It is assumed that the main and the back diodes (Fig. 1a) can be treated as independent circuit elements with no interaction between the two diodes. This implies that the CdTe thickness is larger than the sum of the depletion regions of the two diodes as shown in Fig. 1b. For a reasonably thick CdTe layer (>3 μm) with a typical carrier density (2×10^{14} cm^{-3}), the conduction and valence bands are flat over about half of the CdTe thickness, and the two diodes can be treated as non-interacting elements. It is also assumed that thermionic emission is the dominant mechanism and the electron current is negligibly small at the semiconductor metal interface. Temperature is set to 300 K unless stated otherwise.

When a forward bias V is applied to the two-diode equivalent circuit in Fig. 1a, the voltage is divided between, V_m across the main junction, V_b across the back contact junction, and JR_s over any resistive components:

$$V = V_m + V_b + JR_s, \tag{9}$$

where J is the current density and R_s is the series resistance.

Under illumination, the voltage drop across the back contact (V_b) is less than zero when the applied voltage (V) is less than the open-circuit voltage (V_{oc}), zero at $V = V_{oc}$, and greater than zero for $V > V_{oc}$.

Under illumination the current across the main junction can be expressed as

$$J_m = J_{mo}(e^{qV_m/AkT} - 1) - J_L + V_m/R_{sh} \tag{10}$$

The current that flows through the back contact is

$$J_b = -J_{bo}(e^{qV_b/kT} - 1) + V_b/R_{sh}^b \tag{11}$$

Equating Eq. (10) to Eq. (11) yields

$$\begin{aligned} &J_{mo}(e^{qV_m/AkT} - 1) - J_L + V_m/R_{sh} \\ &\quad + J_{bo}(e^{qV_b/kT} - 1) - V_b/R_{sh}^b = 0 \end{aligned} \tag{12}$$

Using the technique described by Sites and Mauk [14] the parameters J_{mo}, A, and R_{sh} of the main diode are extracted

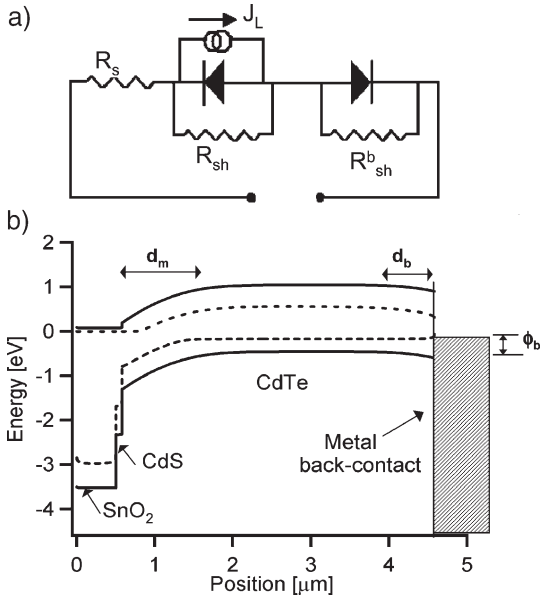

Fig. 1. (a) Two-diode equivalent circuit model, and (b) band diagram of two non-interacting diodes in the light at zero bias (the two depletion regions, d_m and d_b, do not overlap).

from experimental data in the region where the saturation of J_b is not significant. The value of J_{bo} is the current where the JV curve starts to show rollover. Thus, Eq. (12) can be solved analytically to generate the current–voltage characteristics, and the corresponding barrier height can be calculated from Eq. (3). A very similar result to the analytic solution is also obtained using discrete circuit element modeling with Pspice.

For illustration purposes, we show experimental current–voltage (JV) data of a typical CdS/CdTe cell with rollover (Fig. 2a). The CdTe layer is ~10 μm thick, and the device has a carrier density of 1.4×10^{14} cm^{-3} estimated from the capacitance–voltage (CV) measurement, hence, the main and back diodes can be treated as independent elements. The parameters extracted from the experimental data are $J_{mo}=7\times10^{-4}$ mA/cm^2, $J_L=24$ mA/cm^2, $A=2.9$, $R_s=1.4$ Ω cm^2, $R_{sh}=1500$ Ω cm^2. For this cell, rollover occurred when its total current saturated at 4 mA/cm^2, and from Eq. (5) this corresponds to a barrier height of 0.55 eV. Using these parameters and a back diode shunt resistance of $R^b_{sh}=75$ Ω cm^2 (or $G_b=13$ mS/cm^2), the current–voltage characteristic is simulated analytically.

Fig. 2a, shows the simulated curve overlaid on the measured data, and Fig. 2b shows the voltage drops across the main diode and across the back diode as a function of the applied bias. Under illumination and at low forward applied bias, the back diode is under forward bias, and the main diode is at slightly higher voltage than the applied bias. At open circuit voltage the current is zero. Zero current through the back diode, which receives no illumination, means no voltage across it, and hence the applied bias is entirely across the main diode. As the applied bias is further increased, the primary voltage increase is across the back diode, and the current reaches the reverse saturation value defined by the barrier height. Consequently, rollover occurs.

The voltage across the main diode saturates at a voltage, V_s, given by

$$V_s = \frac{AkT}{q}\ln\left[\frac{1}{J_{mo}}\left(J_{bo}+J_L+\frac{V_s}{R_{sh}}\right)\right] \quad (13)$$

If J_{bo} is very large ($J_{bo}\gg J_L$), then V_s becomes large. This implies no rollover ($\Phi_b=0$), and If J_{bo} becomes very small (large Φ_b from Eq. (5)) then the voltage saturates at,

$$V_s = \frac{AkT}{q}\ln\left[\frac{1}{J_{mo}}\left(J_L+\frac{V_s}{R_{sh}}\right)\right] = V_{oc} \quad (14)$$

The voltage across the main diode saturates at V_{oc}, hence any applied bias increment above V_{oc} will be entirely across the back diode.

The effect of shunt resistance at the back diode, R^b_{sh}, on rollover was also studied. The simulated result, Fig. 2a, showed that R^b_{sh} affects only the rollover part of the JV curve, and the slope of the roll over curve is the leakage conductance G_b at the back contact ($G_b=1/R^b_{sh}$). For room-temperature barrier heights in the range 0.5–0.6 eV, significant rollover appears only in the first quadrant, and hence FF is not affected by the magnitude of the shunt resistance at the back diode. For a very

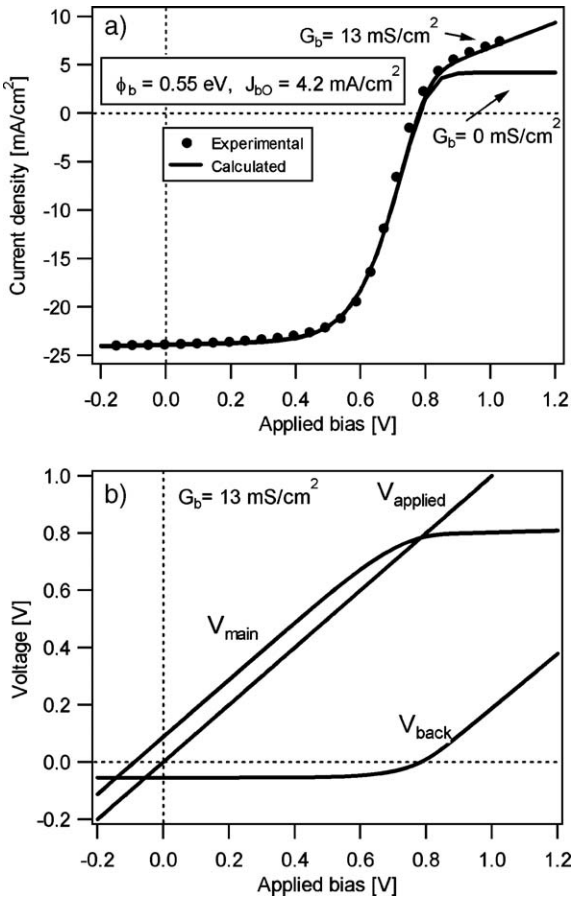

Fig. 2. (a) Experimental and simulated current–voltage characteristics of a CdTe cell with rollover, and (b) the voltage drops across the main and the back diode as a function of the applied bias.

large shunt, $R_{sh}^{b} \rightarrow \infty$, the rollover curve is very flat, but its slope increases with decreasing R_{sh}^{b}. When the shunt resistance at the back contact equals the lumped series resistance of the device, the slope of the rollover matches the *JV* curve slope, and hence rollover disappears despite a significant barrier height. In general, the magnitude of the barrier height determines the point where the current–voltage curve becomes current-limited, and the slope of the rollover curve is determined by the value of the shunt conductance of the back diode. Thus, a fixed barrier height could result in rollover curves that may appear different depending on the values of the shunt conductance; however, the curves will start to show rollover trend concurrently.

When the back-barrier height is varied in the calculation, keeping other parameters unchanged, the result is the series of curves shown in Fig. 3a. As the barrier height is increased, the current saturates at a lower value and hence rollover occurs at lower bias voltage. Note that the rollover changes dramatically over a relatively narrow range of barrier heights. With increasing barrier height, performance is affected by a reduction in fill factor. In general, the open-circuit voltage at room temperature is not significantly affected by barrier heights in the range 0.5–0.6 eV. Fig. 3b shows the effect of barrier height on fill

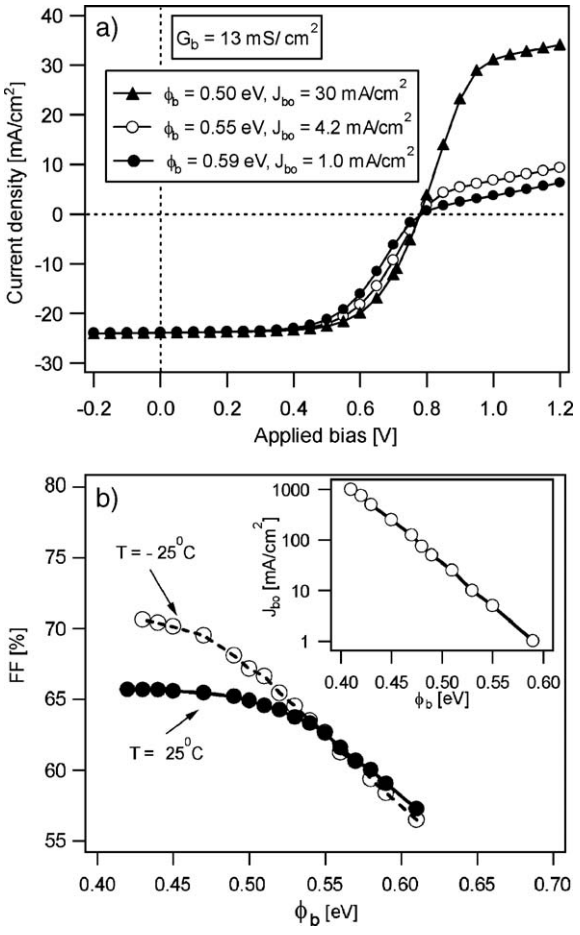

Fig. 3. (a) The effect of barrier height on the current–voltage characteristics (simulated), and (b) reduction of fill-factor with increase in barrier height and the insert shows the saturation current J_{bo} as a function of the barrier height.

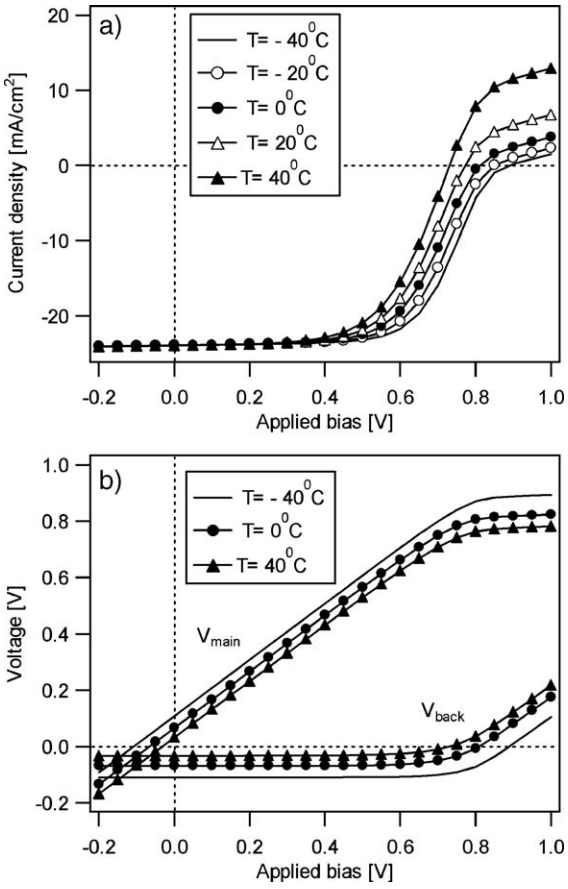

Fig. 4. (a) The effect of temperature variation on rollover, and (b) the corresponding voltage drops across the main and the back diode as a function of the applied bias.

factor for two temperatures. The fill factor difference for high and low temperature is smaller at higher barriers. The insert in Fig. 3b shows the saturation current J_{bo} as a function of the barrier height.

The effect of temperature on rollover was investigated by keeping the barrier height unchanged and varying the temperature from −40 to +40 °C. The simulated current–voltage curves are shown in Fig. 4a, and the voltage drops across each diode for three temperatures are shown in Fig. 4b. Fig. 4a, shows that the contact barrier has a larger impact as the temperature is lowered. Lower temperature has a similar effect to increased barrier height. As the temperature is lowered, rollover appears at a lower voltage, although the open-circuit voltage still increases.

4. Conclusions

The two-diode model simulation result helps to explain the non-ideal behavior of thin-film CdTe solar cells due to the back-contact barrier height. A reasonable estimate of the barrier height is obtained by fitting the simulated curve to the measured current–voltage characteristic curve. Simulated data indicates that barrier heights above 0.5 eV will significantly reduce fill-factor, but the open-circuit voltage will not be affected by barriers in the 0.5 to 0.6 eV range. This work illustrates that the

degree of rollover is determined by the barrier height, temperature, quality of main diode, and shunt resistance at the back diode.

Acknowledgment

This work was supported by US National Renewable Energy Laboratory. “AMPS-1D” software developed at Pennsylvania State University by S. Fonash et al. was used to calculate the energy band diagram.

References

[1] D.H. Rose, F.S. Hasoon, R.G. Dhere, D.S. Albin, R.M. Ribelin, X.S. Li, Y. Mahathongdy, T.A. Gessert, P. Sheldon, Prog. Photovolt. 7 (1999) 331.
[2] C.R. Corwine, A.O. Pudov, M. Gloeckler, S.H. Demtsu, J.R. Sites, Sol. Energy Mater. Sol. Cells 82 (2004) 481.
[3] A.O. Pudov, J.R. Sites, S.H. Demtsu, M. Gloeckler, K.L. Barth, R.A. Enzenroth, W.S. Sampath, Proc. of the 29th IEEE PVSC, New Orleans, LA, USA, May 17–24 2002, p. 760.
[4] C.S. Ferekides, V. Viswanathan, D.L. Morel, Proc. of the 26th IEEE PVSC, Anaheim, CA, USA, September 29–October 3 1997, p. 423.
[5] B.E. McCandless, Y. Qu, R.W. Bikmire, 1st world conference PVSEC, Waikoloa, HI, December 5–9 1994, p. 107.
[6] G. Stollwerck, J.R. Sites, Proc. of 13th European PVSEC, Nice, France, October 1995, p. 2020.
[7] A. Niemegeers, M. Burgelman, J. Appl. Phys. 81 (1997) 2881.
[8] T. McMahon, A. Fahrenbruch, Proc. of the 28th IEEE PVSC, Anchorage, AK, USA, September 15–22 2000, p. 539.
[9] P. Nollet, M. Burgelman, S. Degrave, Thin Solid Films 361–362 (2000) 293.
[10] M. Burgelman, J. Versharagean, S. Degrave, P. Nollet, Thin Solid Films 480–481 (2005) 392.
[11] B.E. McCandless, J. Phillips, J. Titus, Proc. 2nd world conference PVSEC, Vienna, Austria, July 6–19 1998, p. 448.
[12] S.M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981, p. 279.
[13] M. Gloeckler, A.L. Fahrenbruch, J.R. Sites, Proc. 3rd world conference PVSEC, Osaka, Japan, , May 11–18 2003, p. 491.
[14] J.R. Sites, P.H. Mauk, Sol. Cells 27 (1989) 411.