Carrier-selective contacts for Si solar cells

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Carrier-selective contacts (i.e., minority carrier mirrors) are one of the last remaining obstacles to approaching the theoretical efficiency limit of silicon solar cells. In the 1980s, it was already demonstrated that *n*-type polysilicon and semi-insulating polycrystalline silicon emitters form carrier-selective emitters which enabled *open-circuit voltages* (V_{oc}) of up to 720 mV. Albeit promising, to date a polysilicon emitter solar cell having a high *fill factor* (*FF*) has not been demonstrated yet. In this work, we report a polysilicon emitter related solar cell achieving both a high $V_{oc} = 694$ mV and $FF = 81\%$. The passivation mechanism of these so-called tunnel oxide passivated contacts will be outlined and the impact of TCO (transparent conductive oxide) deposition on the injection-dependent lifetime characteristic of the emitter as well as its implications on *FF* will be discussed. Finally, possible transport paths across the tunnel oxide barrier will be discussed and it will be shown that the passivating oxide layer does not lead to a relevant resistive loss and thus does not limit the solar cell's carrier transport. Contrary to amorphous silicon-based heterojunction solar cells, this structure also shows a good thermal stability and, thus, could be a very appealing option for next generation high-efficiency silicon solar cells. © *2014 AIP Publishing LLC*.
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For the realization of silicon solar cells approaching the theoretical efficiency limit of 29.4%,[1] carrier-selective contacts with low minority carrier recombination and efficient majority carrier transport are mandatory. One example of a solar cell with carrier-selective contacts is heterojunction solar cells with intrinsic thin-film (HIT), where record efficiencies of 24.7%[2] are already achieved. The outstanding open-circuit voltage (V_{oc}) of 750 mV can be ascribed to the excellent surface passivation provided by the intrinsic amorphous silicon layers (a-Si:H). However, this surface passivation scheme can withstand only low process temperatures (~250 °C) and therefore requires a dedicated back-end processing (low-temperature TCO deposition and metallization). Another approach of carrier-selective contacts are the polysilicon emitter (PE)[3] or the related semi-insulating polycrystalline silicon (SIPOS) technologies.[4] These technologies offer a higher tolerance to high-temperature back-end processes and thus facilitate the deposition of crystalline TCOs as well as sintering processes for metal contacts. In the 1980s, these contacts, which were invented for bipolar junction transistors (BJTs), were applied to solar cells with the aim to significantly reduce the surface recombination. An excellent V_{oc} of 720 mV was achieved using the SIPOS emitter.[5] However, the authors reported no values for the fill factor (*FF*) and therefore it is not clear if the majority carrier transport was efficient. At the same time, Tarr demonstrated a polysilicon emitter solar cell with Al back surface field (BSF) achieving 652 mV.[6] Unfortunately, a *FF* of only 60.5% was obtained. Moreover, the solar cell's blue response was significantly degraded by substantial parasitic absorption in the 50 nm thick polysilicon emitter. Although PE-based approaches promise excellent surface passivation, higher doping efficiency in comparison to amorphous silicon layers, and a significantly reduced parasitic absorption, neither a high *FF* nor a high J_{sc} has been demonstrated so far. In this work, we will demonstrate a solar cell with minority (emitter) and majority (BSF) carrier contacts realized by a thin tunnel oxide and doped silicon thin film, enabling a high V_{oc} and *FF* at the same time. The interface passivation achieved by the so-called tunnel oxide passivated contacts is investigated and the impact of TCO deposition is illustrated. It will be shown that these carrier-selective contacts do not only provide a high quasi-Fermi level (QFL) splitting but also yield a high external voltage and that the two tunnel oxides do not restrict the carrier transport.

The interface passivation of both carrier-selective contacts was studied by means of injection-dependent lifetime measurement utilizing the QSSPC (quasi-steady state photoconductance) setup.[7] Symmetrical lifetime samples were realized on 250 μm thick, (100)-oriented 1 Ω cm *p*-type FZ silicon. After an RCA clean, a ~14 Å thin tunnel oxide layer was wet-chemically grown in nitric acid (68 wt. %, 110 °C for 10 min).[8] Subsequently, 15 nm thick Si based layers (phosphorus or boron-doped) were deposited with an amorphous structure by chemical vapour deposition on both sides leading to symmetrical Si(n)/SiO_x/c-Si(p)/SiO_x/Si(n) (*n*-contact) and Si(p)/SiO_x/c-Si(p)/SiO_x/Si(p) (*p*-contact) structures. Thereafter, the samples were exposed to a furnace anneal with plateau temperatures in the range of 700 °C–900 °C which lead to a partial crystallization of the Si layers. The samples were finalized by a hydrogen passivation process at 400 °C.[9] The interface passivation of these structures is characterized by the implied voltage at 1 sun (iV_{oc}) which is calculated according to

$$iV_{oc} = \frac{kT}{q} ln\left(\frac{1}{n_i^2}\left(\Delta n + \frac{n_i^2}{N_D}\right)(\Delta n + N_D)\right).$$

Fig. 1 plots the iV_{oc} over T_{Anneal} for both P- and B-doped structures. For the *n*-contact, the optimum

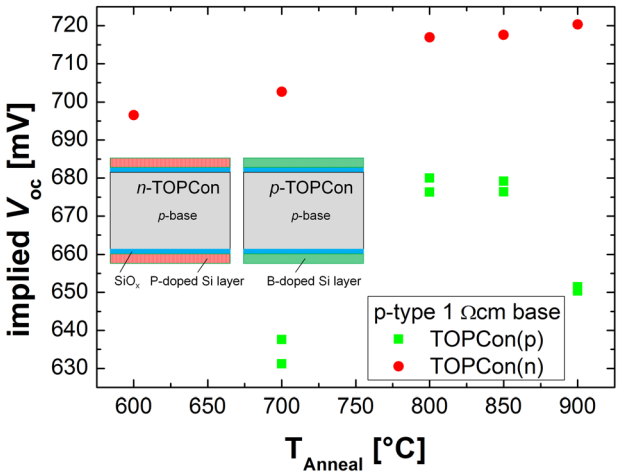

FIG. 1. Implied V_{oc} as a measure of the passivation quality of both the *n*- and *p*-contact after hydrogen passivation as a function of the furnace annealing temperature.

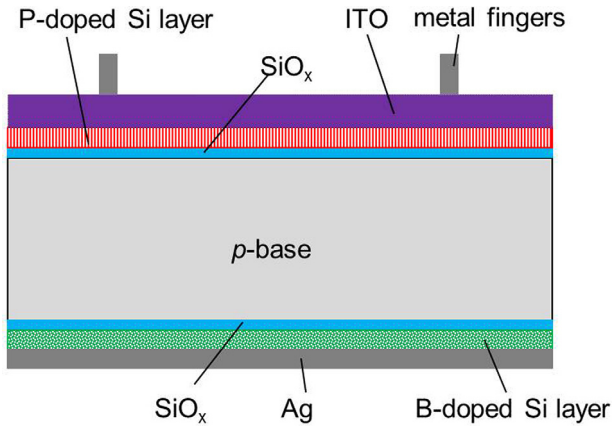

FIG. 2. Schematic of solar cell with tunnel oxide passivated emitter and BSF.

annealing temperature is in the range of 800 °C–900 °C and a maximum $iV_{oc} = 720$ mV was obtained. On the other hand, the optimum temperature range for the *p*-contact is narrower (800–850 °C) and the maximum $iV_{oc} = 680$ mV is significantly lower. The corresponding minimum J_0 values are about 10 and 50 fA/cm^2 for *n*- and *p*-contacts, respectively. This distinctive behavior was also observed for PE BJTs, where J_{0e} values as low as 20 fA/cm^2 (Ref. 10) and 100 fA/cm^2 (Ref. 11) for the P- and B-doped polysilicon emitter were reported, respectively. These fundamental differences between P- and B-doped layers can be attributed to the following reasons: (i) asymmetry of the oxide barrier height,[12] (ii) B-doped silicon thin films have a higher defect density,[13] and (iii) the penetration of the tunnel oxide by diffusing boron atoms leads to a higher defect creation.[14]

In Ref. 15, it was reported that the *n*-contact's passivation degraded strongly at $T_{Anneal} > 900$ °C. This effect is independent of doping but can be explained by the balling-up of the tunnel oxide layer which was observed for the related PE BJTs first.[16] This balling-up of oxide is accompanied by a strong reduction of R_s. Thus, for BJTs a fundamental trade-off between a high gain (low J_{0e}) and low series resistance had to be addressed. While this posed a big problem for the scaling of high-speed BJTs,[17] it does not affect our solar cell structure because the carrier-selective contacts cover the entire surface of the solar cell. This was already demonstrated for a majority carrier contact on an *n*-type solar cell achieving $FF > 82\%$.[15]

The contacts' selectivity can be characterized by their self-induced c-Si dark band bending. The dark band bending φ_0 was obtained by the surface photovoltage technique.[18] To this end, one-sided Si(n)/SiO$_x$/c-Si(p) and Si(p)/SiO$_x$/c-Si(n) structures were realized on *p*-type and *n*-type 1 Ω cm Si wafers ($N_A = 1.5 \times 10^{16}$ cm^{-3}, $N_D = 5 \times 10^{15}$ cm^{-3}), respectively. The theoretical upper limit for φ_0 is the difference between Fermi-level and conduction and valence band of the c-Si absorber and takes a value of 932 mV and 902 mV, respectively. The measured dark band bending of the Si(n)/SiO$_x$/c-Si(p) structure was $\varphi_0 = 928$ mV and $\varphi_0 = 900$ mV for the Si(p)/SiO$_x$/c-Si(n) structure. That both values agree well with the upper limit underlines the high selectivity of the contacts.

To study the charge carrier transport across the tunnel junction, planar solar cells on *p*-type silicon were fabricated (see sketch in Fig. 2). The *n*-contact formed the front emitter and the *p*-contact the BSF. After the deposition of the doped silicon layers, the wafer received a thermal treatment for 60 min at a plateau temperature of 800 °C. Since the sheet resistance of the 15 nm thin Si(n) layer is in the kΩ range, 70 nm ITO was sputtered on the front side to provide for the lateral transport of charge carriers to the metal fingers. The sputter damage was then cured by annealing at 250 °C for 10 min on a hotplate. Although the passivated contacts are tolerant to high-temperature processes, a higher annealing temperature would significantly alter the properties of the used ITO. Finally, Ag was thermally evaporated on the rear side and 60 μm wide fingers were realized by thermal evaporation of a Ti/Pd/Ag stack and the lift-off technique.

Fig. 3 illustrates the influence of ITO sputtering on the initial injection-dependent lifetime characteristic. An excellent passivation quality is achieved directly after the thermal treatment ($iV_{oc} = 706$ mV). At low-level injection, a constant lifetime characteristic is obtained and yields a very high implied *FF* (*iFF*) of 85%. After ITO deposition, the picture

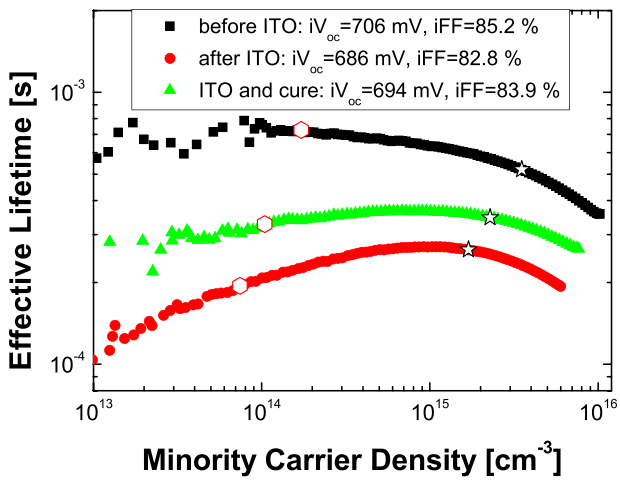

FIG. 3. Lifetime characteristic of non-metallized solar cell after specific processing steps. Stars and pentagons denote iV_{oc} and iV_{MPP}, respectively.

changes completely: not only iV_{oc} is significantly diminished but also the lifetime is strongly decreased at low-level injection. As a result, the *iFF* is reduced to 82.8%. This can be ascribed to substantial sputter damage which creates defects at the Si/SiO_x interface and in the bulk of the Si layer.[19,20] By means of hotplate annealing, the initial passivation quality could be partially recovered. However, the non-passivated defects still adversely affect the lifetime characteristic at open-circuit and maximum power point (MPP) conditions. Nevertheless, *iFF* takes a fairly high value of 83.9%. In combination with the 1D junction design of both the electron and hole contact, the solar cell has a high *FF* potential.

The finished cells yield a maximum V_{oc} of 694 mV and demonstrate that the QFL splitting, i.e., the implied voltage provided by both tunnel oxide passivated contacts is maintained in the finished device. Furthermore, the high *iFF* almost completely translates into a high pseudo *FF* (*pFF*) of 83.6% obtained by SunsV_{oc} measurement. Additionally, a SunsVoc characteristic was taken at high illumination intensities to probe the doping efficiency of the Si(n) emitter and its contact properties to the ITO contact.[21] In contrast to insufficiently doped a-Si:H layers, no pronounced counter-diode can be observed, which means that the doping efficiency of the emitter is sufficient and the Si(n)/TCO contact does not limit the *FF* of the cell.

Therefore, the remaining hurdles are the tunnel oxide layers which principally act as a barrier for the carrier transport. However, depending on the thickness and the existence of small pinholes, charge carriers can overcome this barrier without a relevant resistance loss. It was already shown that the used thin oxide layer can be integrated into a passivated electron rear contact for *n*-type Si solar cells without hampering the cell's fill factor.[15] Charge carriers can overcome this oxide barrier by means of tunneling (direct or trap-assisted)[22] or via pinholes in the oxide.[23] A partial oxide break up occurs at $T_{Anneal} > 900\,^{\circ}C$ (Ref. 16) and can be used to reduce the structure's contact resistance. However, after annealing at lower temperatures, a large proportion of the oxide layer remains intact (observed by TEM) and therefore tunneling has to be a relevant transport path for the realized solar cells. Regarding tunneling transport, the thin SiO_x layer exhibits a higher barrier for holes than for electrons due to the oxide's larger valence band offset to Si ($\Delta E_V = 4.5$ eV, $\Delta E_C = 3.1$ eV).[24] As a result, the direct tunneling process would be less likely for holes than for electrons and would lead to a higher resistance contribution of the boron-doped hole contact.

The results from the light *I-V* measurements of the solar cell are given in Table I. Besides a high V_{oc} of 694 mV, the best cell yields a *FF* of 81.1%. The solar cell's series resistance is calculated from the difference between *pFF* and *FF*[25] and takes a low of value of 0.5 Ω cm^2. This value includes all contact resistance contributions (metal/TCO, metal/Si, TCO/Si, and tunnel junctions) as well as series resistances contribution from the lateral transport in the TCO and the metal grid as well as transport in the silicon base. This shows that the oxide barrier in the boron doped hole contact does not lead to a serious contact resistance contribution which would limit the fill factor of the device. This means that either the barrier height for holes is still small enough for an appropriate direct tunneling process or other transport mechanisms like trap-assisted tunneling play a role in the transport of carriers.

TABLE I. Planar solar cell parameters measured by light *I-V* and SunsV_{oc}.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	*PFF* (%)	η (%)
Average (14 cells)	692.4 ± 1.6	31.6 ± 0.2	79.4 ± 1.7	83.1 ± 0.7	17.3 ± 0.4
Best	693.5	31.8	81.1	83.6	17.9

The low J_{sc} can be attributed mainly to the nature of the planar test structure. First, a poor light trapping at the non-textured front combined with a shading loss of ~10% due to the 60 μm wide metal grid fingers reduces the J_{sc} by about 8.9 mA/cm^2. Second, the escape of IR light at the rear side amounts to a J_{sc} loss of 3.0 mA/cm^2. Thus, the maximum absorbed current (calculated via 1-R) is 34 mA/cm^2. The difference between the measured J_{sc} and the absorbed photocurrent can be explained by parasitic absorption in the ITO and Si(n) emitter ($\lambda < 700$ nm) and by free-carrier absorption in the ITO and absorption in the Si(p) contact ($\lambda > 900$ nm).

A solar cell with a tunnel oxide passivated emitter and BSF was presented. The surface passivation mechanism of these carrier-selective contacts as well as the inferior performance of the *p*-contact were discussed. The selectivity of the contacts was substantiated by a high V_{oc} of 694 mV. While related PE solar cells suffered from low *FF*s, the tunnel oxide layers needed for passivation did not significantly increase the cell's series resistance and allowed for a high *FF* of 81%. Thus, these first results indicate that this passivated contact technology might be a promising alternative to amorphous silicon based heterojunctions.

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