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Silicon substrate effects on the current–voltage characteristics of advanced p–n junction diodes

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Abstract

An in-depth analysis of the forward and reverse current–voltage characteristics allows determination of the different geometrical (area, perimeter and corner) and physical (diffusion and generation) current components. This is a powerful technique to assess the silicon substrate quality. In this paper it is shown that the diffusion current of a good quality silicon p–n junction is significantly lower for an epitaxial (Epi) wafer compared to a Czochralski (Cz) wafer. This can be explained by a correction factor, F, which depends on the parameters of the highly doped substrate. The impact of the substrate is less pronounced when the leakage current is dominated by the peripheral component. Furthermore, for low reverse bias, current transients occur for large area diodes in Cz substrates. These are related to the presence of generation centres, which are absent in epitaxial wafers.

Keywords: Czochralski silicon; Epitaxial wafers; Leakage current; Current transient

1. Introduction

The economical down-scaling of a submicron CMOS technology necessitates the use of larger diameter silicon wafers. This goes along with an increased interest in epitaxial (Epi) wafers for volume production. One of the reasons is that due to the high electrical and structural quality of the thin epitaxial layer, high-yield processing can be achieved. In this work it will be shown that the area/bulk diffusion current is strongly reduced using Epi wafers, due to the presence of the highly doped substrate. On the other hand, reducing the p–n junction dimensions puts more and more emphasis on perimeter and corner effects, so that one can wonder whether there is still an impact of the substrate on the diode leakage. Several reports have pointed out that in state-of-the-art shallow junctions, the reverse bulk leakage component is dominated by the fundamental diffusion current [1,2]. It will be shown here that the dominant current component depends on the diode geometry and also on the wafer type, i.e. Cz or Epi. In the large area Cz diodes for which the leakage current is dominated by the area component, the possible occurrence of transient currents has to be accounted for. In such cases, measures have to be taken in order to eliminate the transients and to use the steady-state reverse current for diagnostic purposes.

2. Experimental

Diodes compatible with a 0.35 μm CMOS technology are processed on 150 mm p-type Cz and p/p^+ substrates. All wafers received a high-low-high internal gettering (IG) treatment. The substrate doping density is in the 10^{15} cm^{-3} range, as derived from capacitance–voltage (C–V) measurements on reverse biased junctions. The n^+ regions have been fabricated by a 70 keV, 3×10^{15} cm^{-2} As implantation followed by an 1100°C, 10 s rapid thermal anneal. This results in a junction depth in the range of 0.17–0.2 μm. Lateral isolation of the diodes is achieved by a classical LOCal Oxidation of Silicon (LOCOS) scheme.

Current–voltage (I–V) measurements have been performed on diodes with different geometry, as shown in Table 1 (A is the area, P the perimeter and N_C the

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number of corners). The variable forward or reverse bias is applied to the back contact, while the current is measured at the top junction contact. The bias voltage is varied from −5 to 1 V in 10-mV steps. The measurements are performed in the temperature-controlled dark chamber of a low noise wafer probe station. To avoid any effect from the ambient light, when opening the chamber between measurements, a hold time of 120 s is used. The current is also measured as a function of temperature at 25, 30, 40, 50, 60, 80, 100 and 120°C, respectively. The time dependence of the current is measured during 240 s, with a 1-s time step. The current measurements in the dark are performed at −1 and 0.4 V, respectively, while only −1 V is used for the measurements under light conditions. More details about the experiments are described in Ref. [3].

Table 1
Comparison of the minimum ideality factor m_0 and the diffusion current I_d which is obtained from the forward I–V characteristics of different geometry diodes in Cz and Epi wafers

Diode	A (cm^2)	P (cm)	N_C (no.)	I_d (A)-Cz	I_d (A)-Epi	m_0-Cz	m_0-Epi
SQ1	0.1	1.3	4	9.26×10^{-13}	9.4×10^{-14}	1.02	1.04
SQ2	0.001	0.13	4	1.4×10^{-14}	1.4×10^{-15}	1.00	1.04
SQ3	0.000064	0.032	4	3×10^{-15}	2×10^{-16}	1.01	1.05
ME1	0.001	8.04	320	8.3×10^{-14}	7.2×10^{-14}	1.09	1.22
ME2	0.001	2.04	80	4.2×10^{-14}	1.3×10^{-14}	1.05	1.15
ME3	0.001	1.04	40	3.3×10^{-14}	5×10^{-15}	1.04	1.08
ME4	0.001	0.54	20	3.0×10^{-14}	3×10^{-15}	1.03	1.07

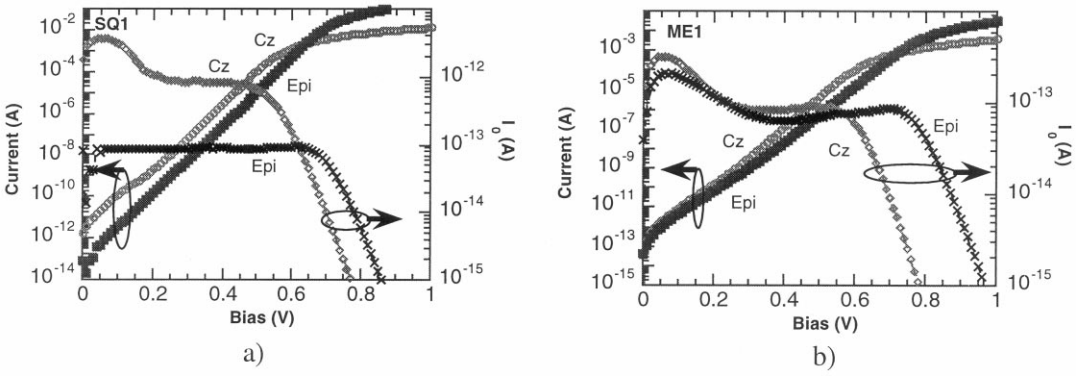

Fig. 1. The forward I–V characteristics and I_0 value defined by Eq. (1) for a fixed minimum ideality factor m_0 (Table 1) of (a) a large area diode (SQ1) and (b) a large perimeter diode (ME1) in Epi and Cz wafers.

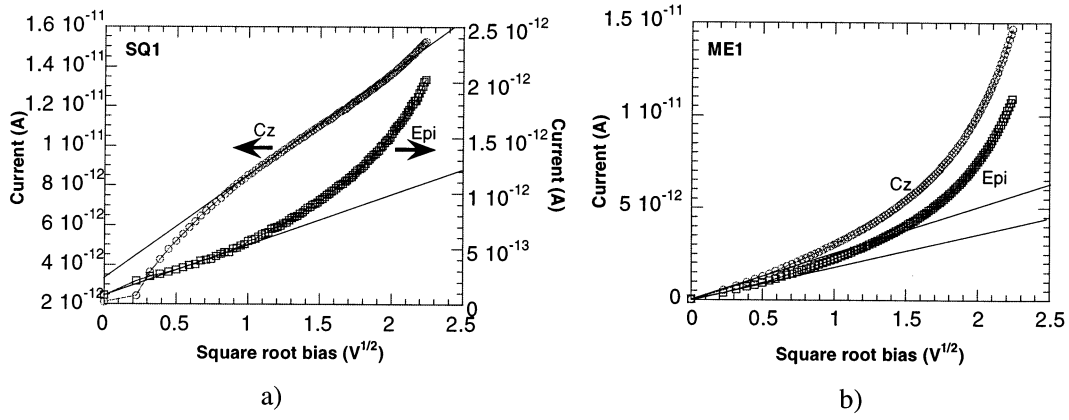

Fig. 2. The leakage current of (a) a large area (SQ1) diode and (b) a large perimeter (ME1) diode in Cz and Epi wafers.

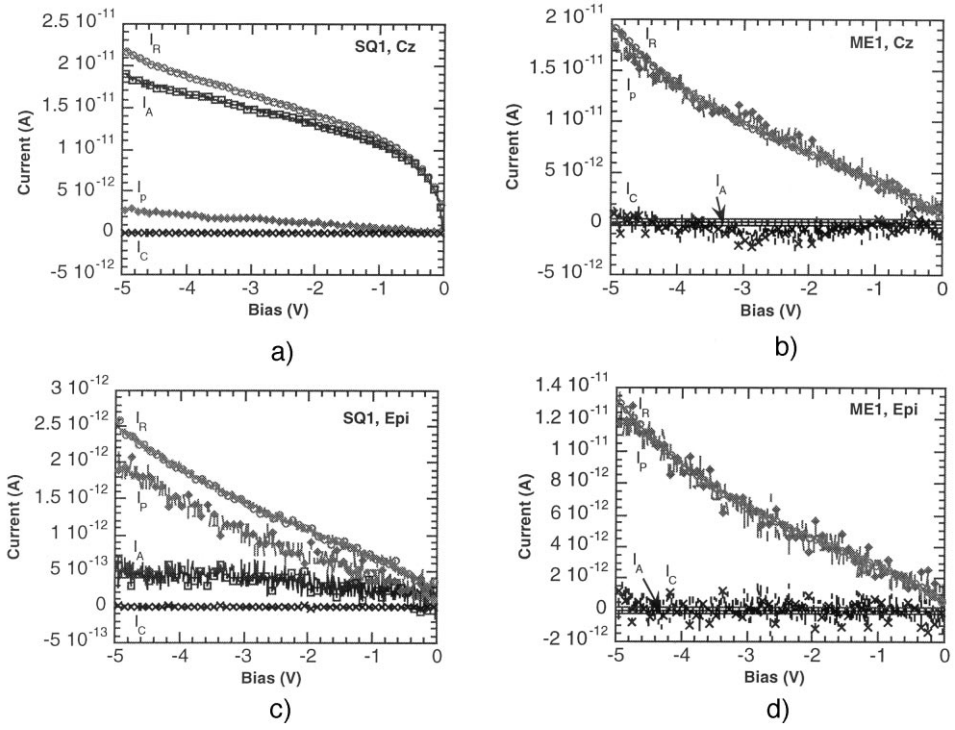

Fig. 3. The total leakage current (I_R), the area leakage current (I_A), the peripheral leakage current (I_P) and corner leakage current (I_C) in (a) a large area (SQ1) and (b) a large perimeter (ME1) diode in a Cz wafer, and (c) a large area (SQ1) and (d) a large perimeter (ME1) diode in an Epi wafer.

3. Results and discussion

3.1. Forward characteristics

For the case of $V_F \gg kT/q$, the experimental forward current can in general be approximated by the empirical formula

$$I = I_0 \exp(qV_F/mkT) \quad (1)$$

where q is the elementary charge, V_F is the forward bias voltage, k is the Boltzmann constant and T the absolute temperature. The ideality factor m equals 2 when the recombination current dominates and 1 when the diffusion current dominates. In the case that both currents are comparable, m has a value between 1 and 2 [4]. The I_0 pre-factor is determined in forward operation as shown in Fig. 1, and corresponds with the minimum ideality factor m_0 (Table 1).

Fig. 1(a) points out that below $V_F = 0.6$ V, the diffusion current dominates in the large area Epi diodes, while in Cz diodes the diffusion current governs for intermediate forward bias and the recombination current at low forward bias ($V_F < 0.2$ V). This demonstrates that the use of an Epi wafer can reduce both the diffusion and the recombination current in the large area diode. For a large perimeter diode, as shown in Fig. 1(b), the impact of the substrate type is rather limited. The diffusion current can accurately be determined from the ideal forward current by taking the minimum ideality factor m_0 into account [5]. This factor m_0 and the diffusion current for different geometry diodes in Cz and Epi wafers are summarised in Table 1.

The minimum ideality factor m_0 in Table 1 shows that the recombination process is more pronounced in the perimeter diodes than in the area diodes. By using Epi wafers, the diffusion current in area diodes can be reduced by more than one order of magnitude, while there is only a marginal impact on the perimeter diodes. This points out that the dominant leakage component is different in large area and perimeter diodes. The dominance of the different current components can be verified by considering the reverse current characteristics.

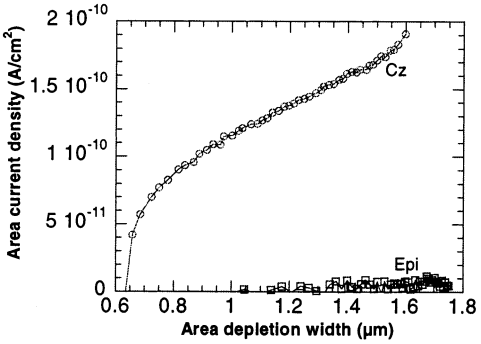

Fig. 4. The area leakage current versus area depletion width for Cz and Epi wafers.

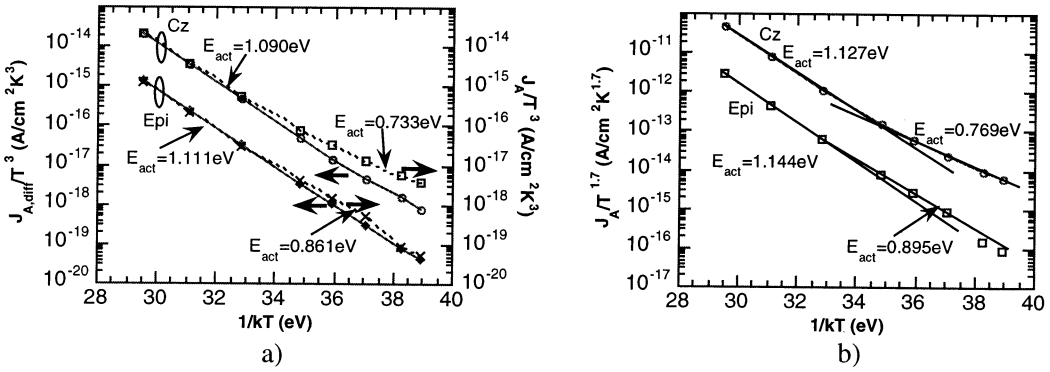

Fig. 5. Arrhenius plot of (a) the T^3 normalised area diffusion current density in an Epi and Cz wafer, derived from the forward I–V intercept (diamonds and circles) and from the reverse area current at -1 V (crosses and squares) and (b) the $T^{1.7}$ normalised area reverse current at -1 V.

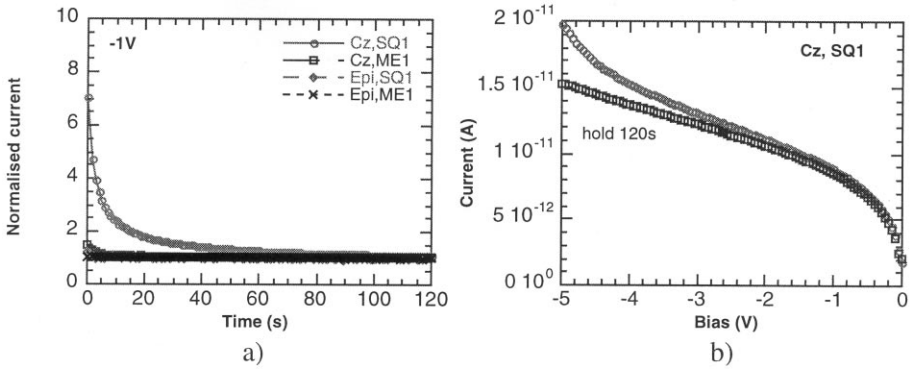

Fig. 6. (a) The current transient in a large area diode (SQ1) and a large perimeter diode (ME1) in Epi and Cz wafers at -1 V, and (b) the effect of current transients on the reverse I–V characteristics.

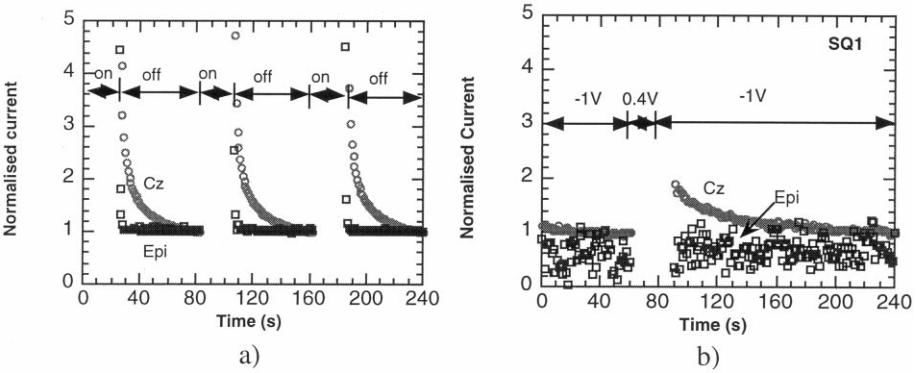

Fig. 7. Current transients due to (a) light and (b) forward bias carrier injection.

3.2. Reverse characteristics

Theoretically, the reverse current I_R of a p–n junction consists of different geometrical components, namely, the area (or volume) leakage current I_A and the perimeter leakage current I_P. For smaller device sizes a possible corner contribution, I_C, proportional to the number of corners N_C of the test structure, might become important. As a result, one can write for I_R [6]:

$$I_R = I_A + I_P + I_C + I_{par} = AJ_A + PJ_P + N_C J_C + I_{par} \quad (2)$$

with I_{par} a parasitic current, related to the device and measurement system parasitics and J_A, J_P and J_C the current densities corresponding to the different components mentioned above.

The area current normally consists of an area diffusion (I_{dA}) and an area bulk generation current, while the peripheral current consists of a peripheral diffusion,

a peripheral bulk generation and a surface recombination current at the Si–SiO_2 interface [1]. The area current can be represented by the equation

$$I_A = I_{dA} + qn_i WA/\tau_g \quad (3)$$

n_i is the intrinsic carrier concentration, τ_g the generation lifetime and W the depletion width in an abrupt junction [4], which is given by

$$W = [2\varepsilon_s(V_{bi} + V_R)/qN_A]^{0.5} \quad (4)$$

where ε_s is the semiconductor permittivity, V_{bi} the built-in voltage, V_R the reverse bias voltage and N_A the acceptor concentration.

From Eqs. (3) and (4), a linear relation between the area leakage current and the square root of the voltage is expected, in case that τ_g is constant. Fig. 2 gives the leakage current of SQ1 and ME1 diodes versus the square root of the voltage for Epi and Cz wafers. From the linear relationship in Fig. 2(a) it can be concluded that the area component dominates in the large area diode for the Cz wafer, while this is not the case for the Epi wafer. From Fig. 2(b) it can clearly be seen that the area component does not dominate in the large perimeter diode neither in the Epi nor in the Cz wafer. The analysis of both the forward and the reverse current allows us to conclude that using Epi wafers can reduce the area leakage current, especially the diffusion current.

In order to separate the different geometrical components by using Eq. (2), one has to combine the reverse I–V characteristics of at least four diodes with different area/perimeter ratios and number of corners, as explained elsewhere [6]. The results of the separation are shown in Fig. 3. The area component governs the leakage current in the large area Cz diode (SQ1), as shown in Fig. 3(a), while the peripheral component dominates in the large area Epi diode (SQ1) and in the large perimeter diode (ME1) in both Cz and Epi wafers as shown in Fig. 3(b,c,d), respectively.

The area bulk generation lifetime in Eq. (3) can be obtained from the linear slope of the area leakage current versus area depletion width curve. The latter can be obtained from the capacitance–voltage (C–V) characteristics. More details about the separation method are given in Refs. [3,6]. The results for Cz and Epi wafers are given in Fig. 4. It can be seen that the area leakage current in both wafers is dominated by the generation current. From the linear slope a generation lifetime of 1.2 ms (Cz) and 13 ms (Epi) is obtained, respectively. This allows us to conclude that the use of Epi wafers also has a beneficial impact on the area generation current (increased generation lifetime).

The experimental results show that the generation current in the Epi wafer is a decade lower than in the Cz wafer. A possible explanation is either a 10 times smaller concentration of the same type of defects or more likely the presence of different generation–recombination (G–R) levels in the depletion region of the two considered substrates.

3.3. Activation energy

The reverse area leakage current is due to both the diffusion and the generation current components. It is possible to separate these two components by studying the temperature dependence of the leakage current. If the area leakage current is dominated by the diffusion current, the temperature dependence should be given by [4]

$$J_A \propto T^{3+\gamma} \exp(-E_g/kT) \quad (5)$$

where E_g is the band gap of Si (~ 1.12 eV at 300 K) and γ is a small number (<1) related to the temperature dependence of the minority carrier mobility and the diffusion length. The temperature variation of the generation current holds

$$J_A \propto T^{1.7} \exp(-E_T/kT) \quad (6)$$

where E_T is the energy level of the G–R center.

Fig. 5 shows the Arrhenius plots of the area diffusion and area leakage current density at -1 V. The activation energy at high temperature in Fig. 5(a) is close to the band gap of Si, indicating that the diffusion current dominates. The activation energy at low temperature in Fig. 5(b) shows that the area leakage current is governed by the generation current. The activation energy for the generation current is 0.769 and 0.895 eV for the Cz and Epi wafer, respectively. The activation energy at low temperature is different for Cz and Epi wafers, which leads to the interpretation that the generation current is controlled by a different type of G–R centre.

The area diffusion current can be reduced by using an Epi wafer at high temperature as shown in Fig. 5(a). The reduction of the diffusion current in the Epi wafer can be explained by the correction factor F (subscript Epi and IG in the case of Epi and internally gettered Cz wafer, respectively) [7,8]. F is given by:

$$F_{Epi} = \tan h(\beta) \quad (7a)$$

$$F_{IG} = \coth(\beta) \quad (7b)$$

where $\beta = D/L_n$, D is the distance from the edge of the depletion region to the p/p^+ interface (Epi wafer) or to the end of the denuded zone (Cz wafer), and L_n is the diffusion length of the minority carriers in the top layer.

Fig. 5(a) shows that the area diffusion current density in a Cz wafer is on the average 18 times higher than in an Epi wafer, so that $F_{IG}/F_{Epi} = 18$. If one assumes that F_{IG} in a Cz wafer is approximately 1, then F_{Epi} is approximately 0.055. According to Eq. (7a), the factor F_{Epi} depends on the Epi layer thickness. The situation is

similar as in a narrow-base diode, in case that the n- or p-region is thinner than the minority carrier diffusion length [9]. Therefore, based on Eq. (7a), it can be predicted that the area diffusion current will reduce when the Epi layer thickness reduces.

In case that for Cz wafers the leakage current is dominated by the area component, other effects such as current transients have been reported [10]. In order to use the diodes as a diagnostic tool, these effects have to be accounted for.

3.4. Current transient

Current transients are observed only in large area diodes (SQ1) in Cz wafers. This is illustrated in Fig. 6(a), while the effect on the reverse characteristics is shown in Fig. 6(b). Taking into account that for SQ1 in a Cz wafer (Fig. 3) the leakage current is dominated by the area component (bulk generation current), this indicates that current transients are an area current effect. The current transient may be due to excess carriers, generated by different mechanisms, e.g. such as light or a carrier injection process. The carriers have to be trapped first and after removal of the excitation source they are released slowly with time (recombination process). Current transients from light and a forward bias injection are shown in Fig. 7(a and b), respectively. This clearly demonstrates that the effect triggered by light is more pronounced than for carrier injection. The origin of the observed current transients has been investigated by using a hold time of 120 s before starting the current measurements. The result is shown in Fig. 6(b) (lower line), and can lead to the conclusion that the current transient in this experiment is due to the light. To avoid this effect, a sufficiently long hold time has to be used after the diodes have been exposed to the microscope light.

4. Conclusion

It has been shown that the area diffusion current is significantly lower for an Epi wafer than for a Cz wafer, due to the Epi layer thickness and the presence of a highly doped substrate. The leakage current may be dominated by the peripheral component as demonstrated in the large perimeter diode in Cz and Epi wafers. The peripheral component dominates in large area diodes in an Epi wafer due to the reduction of the area component. In the case where the leakage current is dominated by the area component, current transients may occur due to light or carrier injection for Cz substrates.

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