The Role of Grown-In Defects in Silicon Minority Carrier Lifetime Degradation During Thermal Treatment in Epitaxial Growth Chambers

Chuqi Yi, Ned J. Western, Fa-Jun Ma, Anita Ho-Baillie, and Stephen P. Bremner

***Abstract*—Severe silicon lifetime degradation was found after its high-temperature treatment in III–V material growth chambers for the fabrication of III–V/Si multijunction solar cells. Further improvement of the cell efficiency requires insights into the root cause of such lifetime degradation and how to protect the silicon lifetime accordingly. While the exact origins of such degradation remain largely unknown, most published work concluded that extrinsic impurities that diffuse into the silicon bulk during the thermal treatment are the sole reason. In this article, we show that while not necessarily present in every float-zone silicon wafer, grown-in defects that can be thermally activated is also a key mechanism behind the observed silicon lifetime degradation during anneal in our molecular beam epitaxy chamber. As such, annealing of the silicon wafer in the furnace at 1000 °C to annihilate the grown-in defects, together with the deposition of a SiN_X diffusion barrier to prevent the extrinsic impurities from diffusing into the silicon bulk, are both required to preserve the silicon lifetime throughout the III–V material growth steps.**

***Index Terms*—III–V/Si, diffusion barrier, grown-in defects, silicon bulk lifetime degradation.**

I. Introduction

III–V/Si multijunction solar cells (MJSC), combining the advantages of ultra-high attainable efficiencies of MJSCs and the low-cost silicon substrates, are one of the promising techniques to be adopted by the photovoltaic (PV) industry after the efficiency of current single-junction silicon solar cell saturates at its fundamental limit [1], [2]. Among many integration techniques, III–V epitaxial growth on silicon substrates is believed to be one of the most mature and stable approaches. However, to achieve the high epitaxial crystalline quality of polar III–V materials on nonpolar silicon substrates, careful preparation of the silicon surface prior to the growth is required [3]–[5]. This includes extensive *ex-situ* wet chemical clean steps as well as *in-situ* silicon surface cleaning with the aid of high-temperature annealing, which essentially burns off any carbon or oxygen-based residuals left on the silicon wafer surface. The *in-situ* high-temperature treatment, often at above 700 °C, not only helps to refresh the silicon surface [6] but can also be used to promote the formation of double-steps which is essential in preventing the formation of anti-phase domains [7].

Nevertheless, the *in-situ* high-temperature annealing steps, regardless of being performed in either metal–organic chemical vapor deposition or molecular beam epitaxy (MBE) chambers, were found to cause severe lifetime degradation in silicon [8]–[16], lowering its bulk lifetime by as much as three orders of magnitude. While the exact origin of such degradation may vary because of different silicon wafers used and different annealing conditions presented across the III–V growth chambers, most of the published work to date concluded that extrinsic impurities, most likely transition metals that diffuse into the silicon during the thermal treatment from the III–V growth chambers, led to such degradation. Consequently, the deposition of a diffusion barrier such as silicon nitride layers at the rear of the silicon wafer was shown to preserve its lifetime [11], [13], [14], [17].

However, it was reported that float-zone (FZ) silicon wafers, which were used in most of the lifetime degradation experiments in the literature, should not be treated as intrinsically defect lean [18]. It was shown that grown-in defects may exist in the FZ wafers and can be thermal-activated when the wafers were heated to above 400 °C in clean oxidation furnaces. Such grown-in defects can then be permanently annihilated when the FZ wafers are annealed at above 800 °C [19]. It was argued in [14] and [20] that the impurities responsible for the silicon lifetime degradation after anneal in III–V growth chambers were not related to the activation of such intrinsic defects since the authors did not observe lifetime recovery after the FZ silicon wafers were heated up to 800 °C in the MBE system. However, mechanisms of formation and activation, plus the annihilation, of such grown-in defects are still largely unknown and thus it is not clear whether such defects present (or can be activated and deactivated during annealing in III–V growth chambers) in every FZ silicon wafer. Furthermore, it is possible that the observed silicon lifetime degradation so far is a combination of the effects of both intrinsic and extrinsic defects. To exclude every possible cause, it is necessary to investigate the intrinsic defects in silicon wafers that can potentially incur the observed lifetime degradation.

In this article, we report our observations for the silicon lifetime degradation after annealing in our MBE system.

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Possible intrinsic causes such as the grown-in defects that can be thermally activated are investigated with the aid from photoluminescence (PL) and photoconductance lifetime measurement techniques. It was found that, though not necessarily present in all FZ wafers, activation of the grown-in defects, together with the diffusion of extrinsic impurities from the growth chambers are both the reasons for the observed silicon lifetime degradation during anneal in our MBE system. Procedures to protect silicon lifetime from both origins are proposed as well.

II. Experimental Methods

A Veeco GEN930 solid source MBE system, consisting of a load-lock, buffer, and main growth chamber, was used to anneal the silicon wafers. All silicon wafers were cleaned with the standard Radio Corporation of America (RCA) clean procedure before being loaded into the load-lock of the MBE system. Indium-free molybdenum sample holders consisting of a ring-shaped base and a horseshoe-shaped retaining ring were used to sandwich the silicon wafers, as shown in the inset in Fig. 1(a). The entire wafer loading procedure was done in a very short period of time, thus minimizing the wafer exposure time to the ambient environment.

After being loaded into the load-lock, the silicon wafers were first heated to 150 °C for 12 h to desorb the surface moisture from exposure to the atmospheric environment during loading. Further outgassing was carried out by heating the silicon wafers in the buffer chamber to 400 °C for at least 2 h, before being transferred into the growth chamber for a full annealing cycle. A mechanical continuous azimuthal rotation assembly held and continuously rotated the silicon wafer during the annealing cycle. A pyrolytic boron nitride (PBN) heater design, featuring densely wound tungsten wire filament, was located at the back of the substrate holder to heat the substrate uniformly via radiation. It should be noted that the PBN heater used in our MBE system is designed for standard III–V applications, containing only tantalum, tungsten, and PBN in the hot zone of the heater, thus minimizing outgassing during annealing. The real-time substrate temperature was monitored via infrared thermal radiation by an external BASF Pyrometer mounted directly facing the substrate surface. Calibration of the Pyrometer was done in the following manner using an offcut silicon wafer from the same batch, not used in this study. The wafer was heated until deoxidation was observed by reflection high-energy electron diffraction (RHEED). The wafer was kept at this temperature for 30 min to ensure complete deoxidation. This deoxidation temperature was taken as 900 °C and the reading of the BASF pyrometer facing the sample was set to this value. The wafer temperature was then lowered to 650 °C (as indicated by the pyrometer) and a homo-epitaxial layer of around 10 nm of silicon was grown. Following this, the temperature was raised to observe the formation of a double atomic step surface through the RHEED pattern [3]. This was transition confirmed and so the temperature was taken to be 800 °C at this point. The settings for the pyrometer were kept for all of the thermal treatments in this study. Unless otherwise specified, the entire temperature ramp up and down rates were 12 and 16 °C/min, respectively. During the annealing,

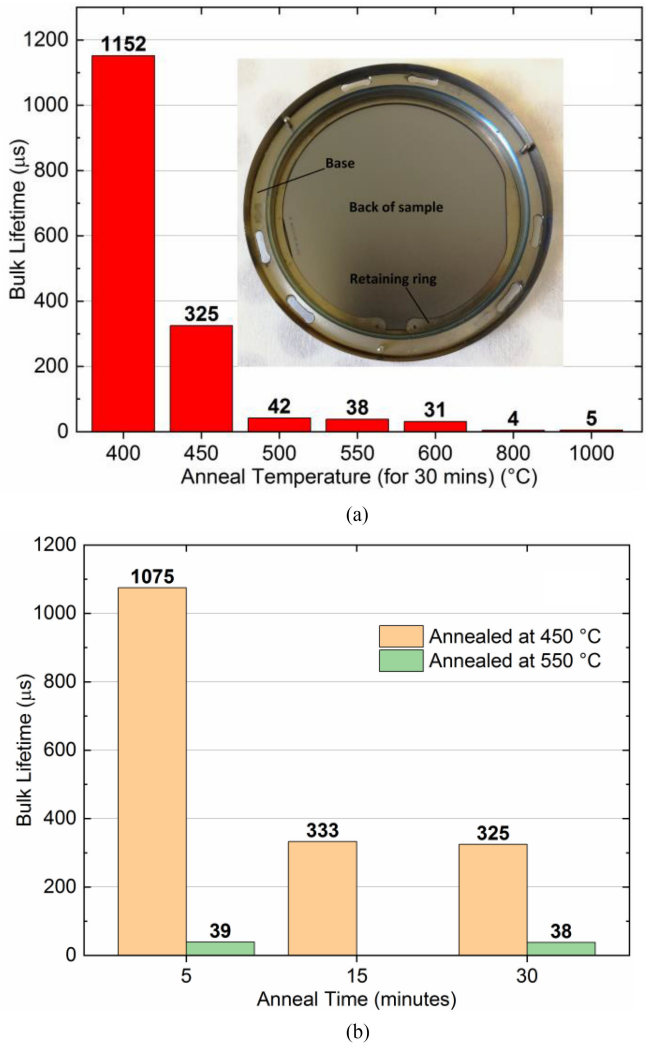


Fig. 1. Evolution of p-type FZ silicon bulk lifetime. (a) Wafers annealed in the MBE chamber at different temperature for 30 min. (b) Wafers annealed in the MBE chamber at 450 °C for 5, 15, and 30 min (yellow) and at 550 °C for 5 and 30 min (green). All lifetime values were measured at a 1×10^{15} cm^{-3} injection level in Sinton tool with iodine ethanol solution passivation. Inset in (a) is a photograph of the base and the retaining ring of the wafer holder that were used to hold the silicon wafer during MBE thermal cycles.

only the silicon substrate was heated, while all the effusion cells were kept at their idle temperature (i.e., no real material growth occurred during the annealing). The base pressure before beginning the anneal cycle was around 1×10^{-10} Torr for each sample, with the chamber pressure peaking at around 1×10^{-8} Torr during the highest temperatures of the anneal cycle. The pressure rise was determined to be primarily due to hydrogen evolution, presumably from the silicon nitride layers, by means of an in-situ Stanford Research Systems residual gas analyzer.

After every MBE anneal, around 10 μm of silicon on both sides of the wafers was removed by etching the silicon wafers in acidic HNA solution (prepared by mixing 49% hydrofluoric acid (HF) with 70% nitric acid and 30% acetic acid in a proportion of 16:1:3) for 5 min. For the wafers heated in the MBE with silicon oxide or silicon nitride layers on the surface, these layers were first removed in HF before an extra 10 μm of silicon on

both sides of the wafers was removed. This was to eliminate any possible contaminants accumulating near the surface that might affect the effective lifetime measurement of the silicon wafers. In this way, only the silicon bulk lifetime was probed.

A Sinton WCT-120 silicon lifetime metrology tool was used for measuring the effective lifetime of the silicon wafers with the quasi-steady-state photoconductance (QSSPC) lifetime measurement method [21]. Before all the lifetime measurements, silicon surfaces were passivated with iodine ethanol solution (more details later). The recombination parameter, J_0, was fitted by the conventional slope method proposed by Kane and Swanson [22]. Note that the inbuilt Eddy current sensor coil for this lifetime metrology tool has a diameter of 40 mm. For all the lifetime measurements, the sensor coil was at the center of the wafer. Thus, the measured lifetime was an average value over the center area of the wafer, omitting the effect of the wafer periphery if spatially nonuniform lifetime present across the wafer.

Spatially resolved PL images of the silicon wafers at different processing stages during the experiment were taken by the BT Imaging LIS-R1 PL imaging system, which is equipped with an 805 nm short excitation wavelength laser. For silicon wafers with severe lifetime degradation, only uncalibrated PL images with a long exposure time of up to 5 s were measured to maximize the PL counts. For these uncalibrated PL images, the units are in PL counts. For the wafers with relatively high lifetime, calibrated PL-based lifetime images were taken with the aid of an inbuilt inductively coupled eddy current sensor coil. The inbuilt current sensor coil allowed the QSSPC lifetime measurement in the PL tool, which is similar to the measurement done by the Sinton lifetime tool. Measured lifetime data was then used to calibrate the captured spatially resolved PL counts, thereby allowing the generation of spatially resolved lifetime images for the wafers [23]. Note that for some PL images a small white ring can be observed. This is caused by the reflection from the metal ring, which is part of the inbuilt eddy current sensor coil, on the QSSPC lifetime stage of the PL tool.

In this experiment, 350 μm p-type (boron-doped) and 380 μm n-type (phosphorus-doped), 3-in, $1-5\ \Omega\cdot$cm doped, $<100>$ off 6° towards the $<110>$ flat FZ silicon wafers from Virginia Semiconductor Inc. were used. Nitrogen content can be detected by secondary-ion mass spectrometry on the p-type wafer and thus the p-type wafers can be treated as [N]-rich [24]. To avoid any extra thermal treatment in addition to the main annealing steps, room-temperature chemical surface passivation using a 0.08 molar iodine ethanol solution [25] was employed. The wafers were first RCA cleaned and then dipped in 4.9% HF until hydrophobic to remove any chemical oxides formed during the RCA clean. The silicon wafers were then etched in a piranha solution, which was prepared by mixing 3 parts 98% sulfuric acid with 1 part 30% hydrogen peroxide (H_2O_2), for 5 min to remove any residual organic contaminants as well as 1–3 nm of the surface silicon. The 0.08 molar iodine ethanol solutions were freshly prepared before each lifetime measurement by dissolving 1 g of resublimed iodine crystals in 100 ml pure ethanol solution. The piranha-etched silicon wafers were then HF dipped again and then loaded into transparent zip-lock bags and 10 ml of the iodine ethanol solution was immediately poured into the bag, minimizing the exposure time of the silicon wafers in air. Since the passivation quality of iodine ethanol solution deteriorates with time, all measurements were performed within half an hour after the solution was prepared. The effect of the zip-lock bags and the iodine ethanol solution during the lifetime measurement was corrected by the optical constant setting, which was adjusted until the measured lifetime in transient mode equals that in the generalized mode in the Sinton tool.

Iodine ethanol solutions are difficult to remove from silicon surfaces with the standard acidic etching and RCA clean steps and were observed in this experiment to affect silicon lifetime after the subsequent annealing steps. To avoid any potential contamination from the iodine ethanol solution, the silicon wafers that were in contact with the iodine ethanol solution were discarded and sister wafers from the same ingot were used for the subsequent anneals and lifetime characterizations.

Repeated lifetime measurements of four similar Virginia Semiconductor silicon wafers with different polarities passivated by the iodine ethanol solution were first carried out to check its passivation quality and repeatability. Between measurements, the silicon wafers were RCA cleaned, HNA solution and piranha etched to remove residual iodine on the surface. Relatively consistent fitted surface J_0 values with an average at 38.3 fA/cm^2 and a standard deviation of 15.85 fA/cm^2 between measurements were achieved for both n- and p-type silicon wafers. In addition, to test lifetime variation of the as-received p-type silicon wafers, four wafers randomly picked from the 25-wafer cassette were passivated with the same iodine ethanol solution and their lifetimes were measured. Compared to the greater than two orders of magnitude variation in lifetime observed for the wafers between the various experimental conditions in this study, the lifetime variation of these four as-received wafers was small, ranging from 992 to 1260 μs.

III. Results and Discussions

A. Observation of Silicon Lifetime Degradation

To verify the lifetime degradation reported in the literature, 3-in, p-type FZ silicon wafers from the same ingot were annealed in our MBE chamber. For the first batch of wafers, the anneal time in the MBE chamber was fixed at 30 min, whilst the anneal temperature was increased from 400 to 1000 °C. For the second batch, the annealing temperature was fixed at 450 °C while the annealing time implemented were 5 and 15 min. For comparison, one more p-type wafer was annealed at 550 °C for 5 min. All wafers received the standard RCA clean before being loaded in the MBE chambers. After the annealing, an acidic etch was performed to remove 10 μm silicon from both sides of the wafers. The effective lifetime of the wafers with iodine ethanol solution passivation was measured and the results are shown in Fig. 1.

Fig. 1(a) shows that the bulk lifetime of the p-type silicon wafer annealed at 400 °C for 30 min is comparable with the as-received p-type wafers. However, for the wafer annealed at 450 °C, its lifetime dropped to almost a quarter of the wafer annealed at 400 °C. Increasing the annealing temperature further deteriorated the silicon lifetime, from 42 μs at 500 °C to below 10 μs at above 800 °C. Comparing the wafers annealed at 400 °C and above 800 °C, a drop in the lifetime by two orders of magnitude was observed.

To test the impact of annealing duration on the silicon lifetime, two more p-type silicon wafers were annealed in the MBE system with the temperature fixed at 450 °C, while the anneal time was varied from 5 to 15 min. It should be noted that for the wafers annealed in shorter periods, ramping rates during anneal might also affect the bulk lifetime. For all annealing in the MBE chamber, 12 and 16 °C/min ramping up and down rates, respectively, were used. Fig. 1(b) shows that when annealed at 450 °C for 5 min, lifetime of the p-type silicon wafer remained at above 1 ms. However, when the annealing time was slightly increased from 5 to 15 min, the silicon bulk lifetime plunged to 333 μs. Further increase of the annealing time to 30 min only slightly decreased the silicon bulk lifetime to 325 μs [results taken from Fig. 1(a)], indicating 450 °C annealing temperature is not high enough to fully degrade the silicon bulk lifetime. Therefore, one more sister p-type wafer was annealed at 550 °C for 5 min and its lifetime is shown in Fig. 1(b) (lifetime of the wafer annealed at 550 °C for 30 min shown in Fig. 1(a) is also plotted in Fig. 1(b) for comparison). It shows that it only took as little as 5 min for severe silicon bulk lifetime degradation to occur if the annealing temperature is high enough. This indicates that considering the ramping time during the MBE anneals, if extrinsic impurities that diffuse into the silicon bulk during the annealing were the reason for the observed lifetime degradation, they were most likely to be fast diffusers. If extrinsic contaminants were not involved, another possibility was that the annealing environment of the MBE growth chamber was very effective at catalyzing the conversion of the state of intrinsic crystal defects into effective recombination centers in the silicon bulk.

Uncalibrated PL images of the wafers with lifetime results shown in Fig. 1(a) and (b) are included in Appendix A as Fig. 8 and in Appendix B as Fig. 9, respectively. It can be seen in Figs. 8 and 9 that spatially nonuniform lifetime distributions occur on the lifetime degraded silicon wafers. As a result, the QSSPC measured lifetimes (with the results shown in Fig. 1) on these degraded samples were only the average lifetime in the center area of the wafers, omitting the relatively higher lifetime regions at the part of wafer periphery. The PL images also give a clue on how the silicon bulk lifetime was degraded after different annealing conditions in MBE. Fig. 8 shows that when annealed at 450 °C, lifetime across the whole 3-in wafer was degraded comparing with the wafer heated at 400 °C. However, a crescent-shaped area at the edge of the wafer retained a relatively higher lifetime compared with the rest area of the wafer. This pattern became prominent when the wafers were annealed at 500, 550, and 600 °C, with the lifetime at the crescent area increased whereas that at the rest area slightly decreased with increasing annealing temperature. While a similar PL pattern was observed for the wafer annealed at 800 °C, its overall PL counts were much lower compared with the wafers annealed between 500 and 600 °C. Interestingly, the crescent-shaped higher lifetime region disappeared for the wafer annealed at 1000 °C. This was possibly due to the overall PL counts were too low for the crescent-shape to be distinguished.

Following the procedures recommended in the literature [13], [17], [20], a 400 nm SiN_X layer was deposited on the full area of the rear of an n-type FZ silicon wafer by plasma-enhanced chemical vapor deposition. This wafer was then heated in our MBE system at 800 °C for 30 min with the nitride side facing the PBN heater in the chamber. Contrary to the results reported in the literature, the lifetime of this wafer with the protection from the SiN_X layer was degraded to below 100 μs. Normalized uncalibrated PL image of this wafer after MBE thermal treatment, as shown in Fig. 2, shows an annular pattern instead of the crescent-shapes seen for the p-type degraded wafers, with lower lifetimes occurring in the center and higher lifetimes around the periphery.

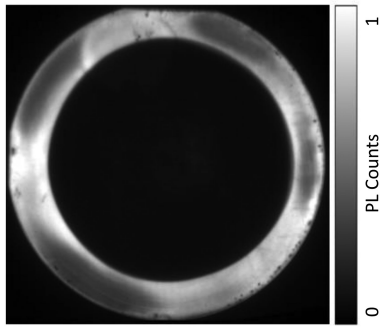


Fig. 2. Normalized uncalibrated PL image of an n-type FZ silicon wafer coated with the SiN_X diffusion barrier layer after heated in the MBE chamber at 800 °C for 30 min.

B. Grown-In Defects

The fact that a 400 nm SiN_X diffusion barrier cannot preserve the silicon lifetime suggests intrinsic defects might also involve in the lifetime degradation. Coincidentally, the PL image of the n-type silicon wafer after thermal cycling in our MBE chamber with the SiN_X diffusion barrier, as shown in Fig. 2 as an example, are very similar to the ones published in the work done by Grant *et al*. on thermally activated grown-in defects of FZ silicon wafers [18], [19]. It was shown in their work that PL images of the FZ wafers after annealing in clean oxidation furnace at 500 °C showed annular patterns, with a higher lifetime at the edge and lower lifetime at the center of the wafer. They showed that such spatially nonuniform distribution of the lifetime is correlated to the radial distribution of vacancies across the wafer. When the ingots are pulled in high rates, vacancies tend to form in the center region, whereas for the periphery a defect or silicon interstitials neutral region is formed [18], [19], [24], [26]–[28]. Note that the PL pattern in Fig. 2 is not as symmetric as the one shown in Grant's work [19]. One possible reason is our silicon wafers are 6° offcut from (100) plane, and so, the high lifetime region is not symmetric around the wafer as shown in Fig. 2. This is because the offcut wafering process gave elliptical defect-rich regions as a result of the projection of the concentric shape of the (100) plane onto the 6° offcut planes. When activated, such defect-rich regions became asymmetric ellipses. These results strongly indicate that grown-in defects that can be thermally activated were also at play in degrading silicon lifetime during the MBE chamber annealing.

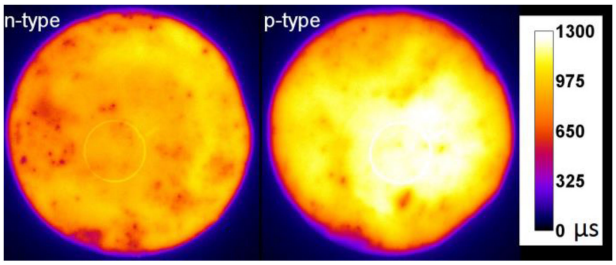


Fig. 3. Calibrated PL-based lifetime images of the as-received (a) n-type and (b) p-type FZ silicon wafers.

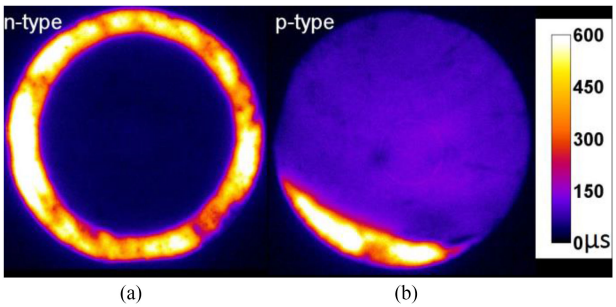


Fig. 4. Calibrated PL-based lifetime images of (a) an n-type and (b) a p-type FZ silicon wafers after annealed at 550 °C for 30 min in oxidation furnace.

To investigate the possible influence of grown-in defects, calibrated PL images of the two as-received FZ wafers, one p-type and one n-type were first captured with iodine ethanol passivation and are shown in Fig. 3. Two more wafers with both polarities were then annealed in a clean oxidation furnace at 550 °C under oxygen flow, which activated the grown-in defects in FZ wafers as indicated in [19]. Lifetimes and PL images of these furnace annealed wafers, as shown in Fig. 4, were measured with iodine ethanol surface passivation after etching off 10 μm of silicon on both sides. Compared with the PL images of as-received FZ wafers in Fig. 3, which exhibit uniform PL patterns and lifetimes of around 1 ms for both n- and p-type wafers, PL image of the n-type wafer after 550 °C furnace anneal shows the typical annular pattern with higher lifetimes around the periphery. The p-type wafer after annealing at 550 °C also shows a spatially nonuniform lifetime distribution, with only a portion of the wafer periphery, shows a higher lifetime as shown in Fig. 4(b), similar to the PL images of the p-type wafers annealed in MBE with degraded lifetimes in Figs. 8 and 9. It is likely that such distinct inhomogeneity in lifetime distribution for p-type wafers after the grown-in defects were activated was due to the way the ingot was sawn for the p-type offcut wafers. Presumably, the p-type ingot was larger than the 3-inch p-type wafers. As a result, only part of the ingot periphery, which is more defect neutral, remained in the 3-in p-type wafer. This is also evidenced by the PL images for the degraded p-type wafers as shown in Figs. 8(b) and 9(b). Portions of narrow, concentric dark rings can be seen on these PL images. These concentric dark rings were often observed on PL images for silicon wafers with concentric dopant density variations [29], thermal donors [30], or oxygen-precipitates [31]. The radius of these rings in Figs. 8(b) and 9(b) decreases from the side where brighter crescent-shape present (which is the edge of the ingot that is more defect neutral) to the other side across the p-type wafers. Therefore, it is likely that the p-type ingot is much bigger than the 3-in p-type wafer and the center of the ingot is located at the point where the radius of these concentric dark rings is the smallest.

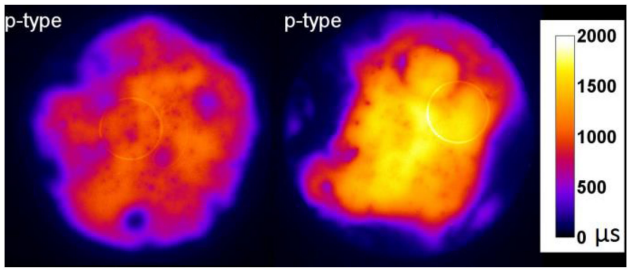


Fig. 5. Calibrated PL-based lifetime images of p-type FZ wafers after been (a) annealed in oxidation furnace at 1000 °C, (b) annealed at 1000 °C and then annealed at 550 °C again in oxidation furnace.

Figs. 3 and 4 clearly show that grown-in defects are present in these wafers. According to Grant *et al*. [19], a further anneal of such wafers at temperatures above 800 °C can permanently annihilate the thermally activated grown-in defects and thus the silicon lifetime can be recovered. As such, four p-type FZ wafers from the same ingot were RCA cleaned and then annealed in an oxidation furnace for 30 min at 1000 °C under oxygen flow. After the annealing, one of the four wafers were taken out and the thermally grown oxide was etched off in HF solution. PL images of this wafer were taken with iodine ethanol solution passivation. Fig. 5(a) shows the calibrated PL lifetime image of this wafer after a 1000 °C furnace annealing. It shows that after annealing of this wafer at 1000 °C in furnace, the ring pattern disappeared, and its lifetime was recovered back to around 1 ms. For comparison, an extra annealing of a p-type wafer in MBE at 1000 °C was performed. This p-type wafer was coated with a 400 nm SiN_X diffusion barrier to protect it from possible extrinsic impurities during MBE annealing. The lifetime of this wafer after the MBE annealing and removal of the nitride and 10 μm surface silicon, with iodine ethanol surface passivation, was 74 μs. PL image of this wafer (not shown) shows that the ring pattern disappeared. However, it also reveals that the nitride layer cracked due to the enormous thermal stress when heated in the MBE chamber at 1000 °C. As a result, possible extrinsic impurities diffused into the silicon bulk via the cracks and deteriorated the silicon bulk lifetime. This indicates that though it is more convenient to anneal the silicon wafer in the MBE chamber at high temperature to annihilate the grown-in defects, the required diffusion barrier layers for extrinsic impurities in the MBE chamber is unlikely to survive the enormous thermal stress, making this method impractical.

Grant *et al*. also reported that an important characteristic of the grown-in defects is that they can be permanently annihilated once the FZ wafers are annealed in the furnace at above 800 °C with oxygen flow. To confirm this, one p-type silicon wafer was heated in the furnace at 550 °C again after its previous 1000 °C

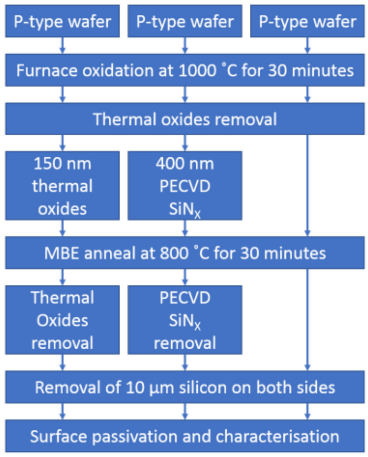


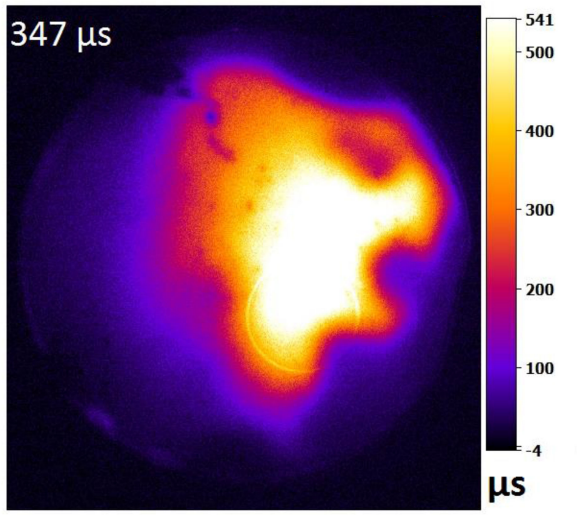
Fig. 6. Flowchart of the wafer processing steps for the silicon lifetime protection experiment.

furnace annealing. The calibrated luminescence-based lifetime image of this wafer shown in Fig. 5(b) indicates no fingerprint of the grown-in defects can be observed. The typical ring-shaped PL pattern is not seen after the wafer is reheated to 550 °C, which is in line with the results reported by Grant *et al.* [19].

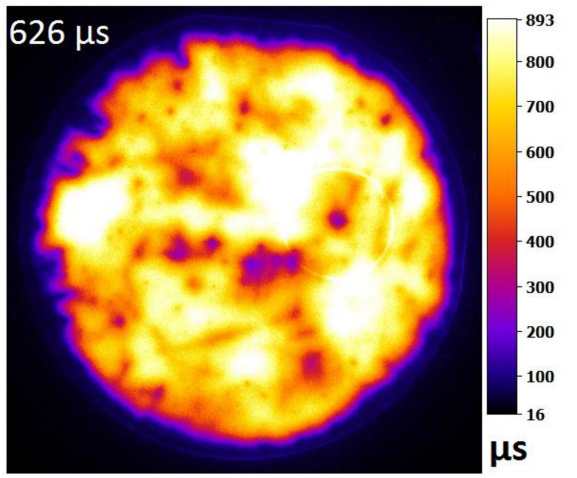
C. Silicon Lifetime Protection

Results shown in Fig. 5 indicate that intrinsic grown-in defects can be annihilated after annealing the FZ wafers in a clean oxidation furnace at 1000 °C. However, results shown in the literature [11], [13], [14], and [17] indicate that the silicon lifetime degradation is also related to extrinsic impurities that diffuse into the silicon during the annealing in epitaxial growth chambers. To test whether this is the case in our MBE chamber and to develop a corresponding method to prevent this to happen, another set of experiments was performed. A flow chart in Fig. 6 shows the general processes of this set of experiments. Briefly, the thermally grown oxides for the remaining three 1000 °C furnace-annealed p-type wafers were etched-off in HF solution. One wafer was then deposited with 400 nm single-side SiN_X layer on the side facing the heater in the MBE chamber, while another wafer was loaded into the oxidation furnace again and a 150-nm oxide was grown on both sides at 1000 °C for 5.5 h. These two wafers, together with the third bare wafer (annealed in a furnace at 1000 °C, thermal oxide etched off, and no subsequent deposition), were then loaded into our MBE chamber and annealed at 800 °C for 30 min. After being cooled down and removed from the MBE chamber, the oxide and nitride layers were etched off in HF and an acidic etch was performed on each of the three wafers to remove 10 μm of silicon on both sides. PL images of these three wafers with iodine ethanol passivation were then measured and shown in Fig. 7.

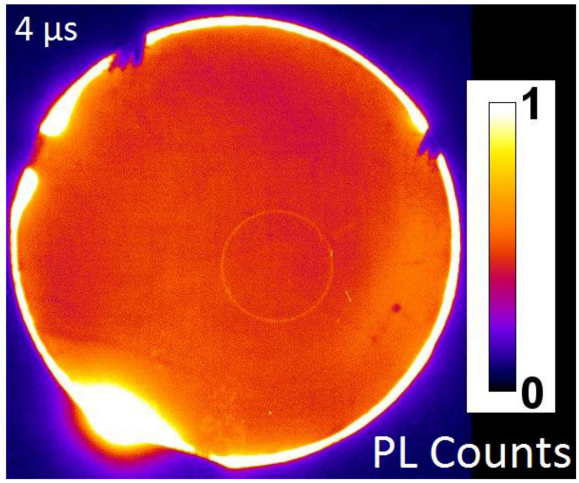
Fig. 7(a) shows only part of the lifetime was preserved for the wafer covered with a 150-nm oxide layer during the MBE annealing, whereas the wafer protected by silicon nitride had its lifetime largely preserved. A thicker thermal oxide layer (around 350 nm) was still not enough to protect the silicon lifetime (results not shown), indicating either the SiN_X layer was better



(a)



(b)



(c)

Fig. 7. Calibrated PL-based lifetime images of the p-type FZ wafers annealed in our MBE system at 800 °C for 30 min with (a) 150-nm thermal oxide layers on both sides or (b) 400-nm single-side SiN_X as the diffusion barrier layer. (c) Uncalibrated PL image of the bare FZ wafer after annealing in the MBE chamber, where the maximum count rate in the image has been normalized to one. Note that prior to the MBE annealing, all the wafers were annealed in oxidation furnace at 1000 °C for 30 min to annihilate grown-in defects. Inserted numbers are QSSPC lifetimes measured on Sinton tool.

as a diffusion barrier, or possible hydrogenation effect from the nitride layer helped recover the silicon lifetime [32], [33]. Note that the wafer coated with a single-side SiN_X layer was annealed in the MBE chamber with nitride side facing the heater, while the oxides protected wafer had oxide layers on both sides during MBE annealing. This confirms that the extrinsic contaminants were introduced from the side facing the PBN heater. Otherwise, lifetime of the single-side nitride coated wafer should be much lower than that of the sample with both sides protected by oxide layers. Fig. 7(a) and (c), however, indicates that in addition to the grown-in defects of the FZ wafers, extrinsic impurities diffusing from the MBE chamber indeed affect the silicon lifetime, since the PL images show uniformly low PL counts across part or whole wafer (instead of an annular pattern), with their bulk lifetime degraded to around 347 and 4 μs, respectively, as measured on Sinton tool. PL image in Fig. 7(c) also shows that there exists a bright area with higher lifetimes at the edge of this wafer, which replicates the shape of the horseshoe-shaped retaining ring of the molybdenum wafer holder as shown in the inset in Fig. 1(a). This means that the molybdenum holder can be ruled out as a possible cause of silicon lifetime degradation as reported by Ding *et al*. [11]; rather, it helped protecting the silicon lifetime by blocking the diffusion of extrinsic impurities into its bulk, thus leaving the part of the silicon underneath it with a relatively higher lifetime. This protective effect of the molybdenum wafer holder can only be observed in wafers with grown-in defects annihilated and without any protective diffusion barrier layers coated during the MBE annealing. This is because grown-in defects result in annular PL patterns with higher lifetimes at the wafer edge that covers the area in contact with the wafer holder. In addition, the protective coatings act as barriers to the in-diffusion of extrinsic impurities, blocking the effect of the retaining ring as a diffusion barrier as well.

Comparing the results shown in Figs. 2 and 7(b), it is clear that only a layer of 400 nm SiN_X layer as a diffusion barrier on silicon is not enough to protect its lifetime during III–V material growth, since grown-in defects might also present in the FZ wafer and can be activated during the thermal treatment in the III–V growth chamber. Therefore, it is recommended that a clean furnace anneal at 1000 °C for 30 min under oxygen flow needs to be performed as a precaution to annihilate these intrinsic defects for all the FZ wafers prior to the III–V material growth. This together with the deposition of a diffusion barrier at the back of the silicon are both required to protect the silicon lifetime.

IV. Conclusion

In summary, our experimental results indicate that apart from extrinsic impurities diffusing into the silicon bulk, grown-in defects that can be thermally activated in FZ wafers, though not necessarily exist in every FZ silicon wafer, are also a key mechanism that can lead to silicon bulk lifetime degradation during III–V material growth. In addition, a diffusion barrier at the rear of the silicon is clearly needed to prevent the diffusion of impurities from the growth chamber into the silicon. A silicon nitride layer of 400 nm was shown to be effective, in line with results reported elsewhere. The use of thermally grown silicon dioxide layers did provide some protection, but proved less effective than the nitride layers. To ensure high silicon bulk lifetime can be thoroughly preserved, annealing of the silicon wafer at 1000 °C to annihilate grown-in defects and the deposition of a SiN_X layer at the back of the silicon wafer as the diffusion barrier for extrinsic impurities are both required.

Appendix A

PL Images of the Wafers Annealed in MBE at different temperatures for 30 min.

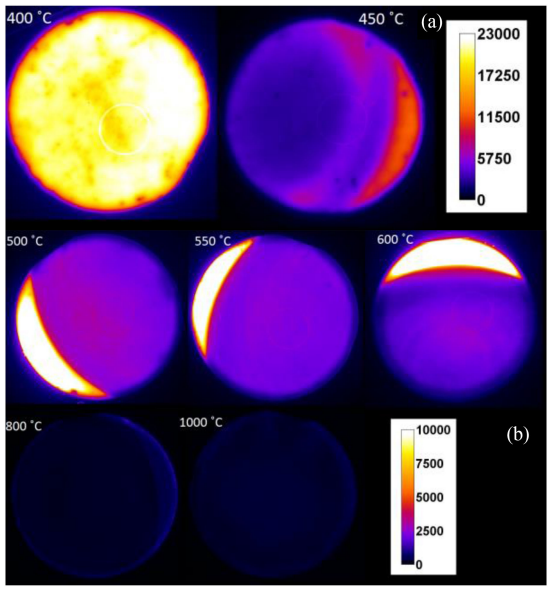


Fig. 8. Uncalibrated PL images of the p-type wafers that were annealed in MBE chamber for 30 min at (a) 400 and 450 °C, and (b) 500, 550, 600, 800, and 1000 °C.

Appendix B

PL Images of the Wafers Annealed in MBE at 450 and 550 °C for different durations.

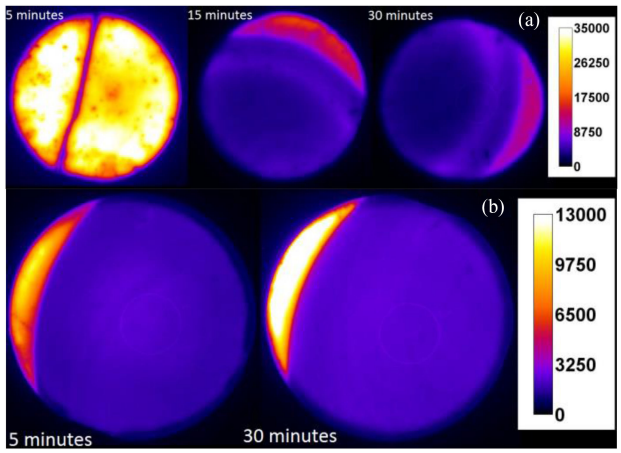


Fig. 9. Uncalibrated PL images of the p-type wafers that were annealed in MBE chamber at (a) 450 °C for 5, 15, and 30 min (note the wafer annealed for 5 min was accidentally broken into two pieces during clean process before the passivation and PL imaging steps) and (b) 550 °C for 5 and 30 min.

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