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Investigation of oxide precipitates in high resistivity silicon using light scattering tomography, low temperature photoluminescence, and deep level transient spectroscopy

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ABSTRACT

The formation and electrical activity of oxide precipitates were evaluated in p-type high-resistivity (HR) Czochralski (Cz) silicon (Si) wafers with varying interstitial oxygen concentrations [(O_i)] after high-temperature annealing. Using a combination of Light Scattering Tomography, Low Temperature Photoluminescence (LTPL) spectroscopy, and Deep Level Transient Spectroscopy (DLTS), we highlight the electrical signatures of oxide precipitates when they form in sufficient quantities to be detected. Meanwhile, the difficulty of growing oxide precipitates is confirmed in HR substrates with low oxygen content, which are safer for component integration. LTPL spectra confirm the activity of oxygen precipitates through D-band emissions across different [O_i] ranges. DLTS analysis of annealed samples with medium [O_i] enables the identification of deep level traps, notably at $E_V + 0.24$ eV and $E_V + 0.42$ eV, likely associated with oxygen precipitates and secondary defects. These findings will contribute to future strategies for the characterization of defects in industrial HR silicon substrates.

I. INTRODUCTION

High-resistivity (HR) Czochralski (Cz) silicon (Si) wafers have gained renewed interest in the semiconductor industry for advanced radio frequency (RF) and photonic applications.[1] These materials are characterized by their low intrinsic dopant densities ($<1 \times 10^{14}$ cm^{-3}) and minimal impurity content, specifically interstitial oxygen [(O_i)].[2]

During device fabrication, interstitial oxygen aggregates in the Si crystal to form electrically active species, known as thermal donors (TDs), and then can compensate for the intrinsic substrate doping.[3–5] This results in the increased noise of RF-CMOS components, for example. To mitigate the negative effects of TDs, reducing [O_i] levels in Cz Si below 6 ppma ($<3 \times 10^{17}$ atoms cm^{-3}) has proven to be an effective approach.[2,6–8]

However, oxygen precipitation phenomena occurring in Si bulk after high-temperature annealing become limited at low [O_i] levels. From this perspective, reducing the [O_i] content in Cz Si poses significant challenges for device thermal integration, as it adversely affects substrate properties such as mechanical robustness, related to slip line locking, and internal gettering (IG) efficiency, ultimately degrading the device yield and performance.[2,9–16]

In this industrial context, it is crucial to develop new methods to monitor oxygen precipitation formation through device integration in low-oxygen Cz Si wafers. To this end, we have developed, for the first time on 300 mm industrial HR Cz Si substrates, a

characterization protocol combining Light Scattering Tomography (LST), Low Temperature Photoluminescence (LTPL), and Deep Level Transient Spectroscopy (DLTS) to study oxygen-related defects.

In heat-treated p-type Cz Si with high [O_i] levels (>13 ppma), LTPL studies focus on the detection of D-band emissions within the 0.7–0.9 eV range, related to oxygen precipitation-induced defects.[17–20] Regarding DLTS, previous studies identified several deep level defects formed in the silicon bandgap.[18,21–23] Hwang and Schroder[24] identified a deep level at $E_V + 0.42$ eV, associated with interface states between oxygen precipitates and the silicon matrix, as the primary source of electrical activity. In contrast, Schmalz *et al.*[25] demonstrated that a deep level located at $E_V + 0.24$ eV, associated with dislocation loops formed during oxygen precipitation, is the dominant contributor. Thus, the origin of electrical activity whether arising from oxygen precipitates themselves or secondary defects such as dislocations remains unclear.

This paper establishes a relationship between oxide precipitates detected by LST and their optical and electrical signatures using LTPL and DLTS in heat-treated HR Si with significantly lower [O_i] levels than previous studies. The experimental conditions to ensure DLTS measurements accuracy are discussed, taking into account the limitations in the case of HR materials, which are due to high diode quality factors (Q) and irregular doping profile. These findings advance the understanding of oxygen-related defect properties in HR silicon and provide critical insights for the future integration of components on HR Si substrates.

II. METHODS

{100} Czochralski Si wafers, 300 mm in diameter, 775 μm thick, and p-type with high resistivity and different [O_i] ranges, were used. Oxygen and carbon concentrations were measured by Fourier transform infrared (FTIR) spectroscopy (Nanometrics QS-3300-ME).

Initial oxygen concentrations at the wafer center were determined close to 2.0×10^{17} atoms cm^{-3} for the low [O_i] samples and 4.5×10^{17} atoms cm^{-3} for medium [O_i] samples. The carbon impurity concentration [C] was around 5×10^{15} atoms cm^{-3} in the set of samples. The oxygen concentration and electrical resistivity of the samples are summarized in Table I.

The oxide precipitate (OP) density was estimated by light scattering tomography (LST; LST-2500HD). The sensitivity threshold for oxide precipitate detection is evaluated to be down to 20 nm. Both low [O_i] and medium [O_i] samples underwent the same thermal budget including Rapid Thermal Annealing (RTA) at 1150 °C under nitrogen (N_2), followed by a two-step annealing process—800 °C for 4 h under N_2, and then at 1050 °C for 16 h in a $N_2 + O_2$ ambient. This conventional precipitation thermal treatment is known to trigger oxygen precipitation in silicon substrates with standard [O_i] levels (>5×10^{17} atoms cm^{-3}) and resistivity between 10 and 15 Ω cm.

TABLE I. Parameters of the HR Si samples used.

Sample	(HR) Low [O_i]	(HR) Medium [O_i]
[O_i] level (ppma)	4	9
[O_i] level (×10^{17} at cm^{-3})	2	4.5
Resistivity range (Ω cm)	2000	1000
Intrinsic doping density (cm^{-3})	≈7×10^{12}	≈1×10^{13}

Two wafers from each sample set were heat treated; one wafer per set was (SiN)-passivated via plasma-enhanced CVD for LTPL analysis to reduce non-radiative surface recombination. The short SiN deposition process (few minutes at T = 780 °C) is expected to have a minimal impact on oxygen precipitation and thermal donors. The photoluminescence spectroscopy setup includes a closed helium-cooled cryostat with a minimum temperature of 7 K, a 532 nm continuous-wave laser for excitation, and a nitrogen-cooled GaInAs detector paired with a high-resolution monochromator.

For DLTS, Schottky diodes were fabricated by Au evaporation after oxide removal (HF and solvent cleaning), with InGa ohmic back contacts. Preliminary I–V and C–V characterizations were performed before DLTS. The DLTS alternative voltage frequency is fixed to 1 MHz.

III. RESULTS AND DISCUSSION

A. LST analysis on annealed HR low and medium [O_i] silicon substrates

Annealed low and medium [O_i] Si substrates were first characterized using LST, as shown in Fig. 1. In the low [O_i] sample [Fig. 1(a)], an oxide precipitate (OP) density of approximately 2×10^7 cm^{-3} is quantified. This defect density is comparable to that of as-grown substrates prior to any thermal wafer processing, which confirms the difficulty of growing oxide precipitates in low [O_i] ranges, as reported in the literature.[10–12] On the medium [O_i] sample [Fig. 1(b)], we quantified a much higher oxide precipitate density up to 5×10^9 cm^{-3}, confirming the role of the [O_i] parameter on the oxygen precipitation mechanism.

We extracted in this sample the OP size distribution, which follows a Gaussian profile centered at approximately 70 nm. This suggests that most of the precipitates formed may be strained due to their size and could be surrounded by extended defects such as punched-out dislocations (PODs) and stacking faults.[9,20,21,26] The extracted OP depth profile indicates that the first defects are located approximately 19 μm beneath the wafer surface, with most defects distributed between 19 and 150 μm. This distribution of defects is coherent with a nucleation mechanism assisted by vacancy diffusion due to the pre-treatment rapid thermal process. According to the literature, the in-diffusion of vacancies into the Si bulk enhances precipitate nucleation, while the out-diffusion of vacancies toward the substrate surface results in the formation of a well-defined denuded zone [see in Fig. 1(b)].[27]

B. LTPL spectra of annealed HR low and medium [O_i] silicon samples

LST analysis revealed poor oxygen precipitation properties in the annealed HR low [O_i] sample, whereas clear precipitation was

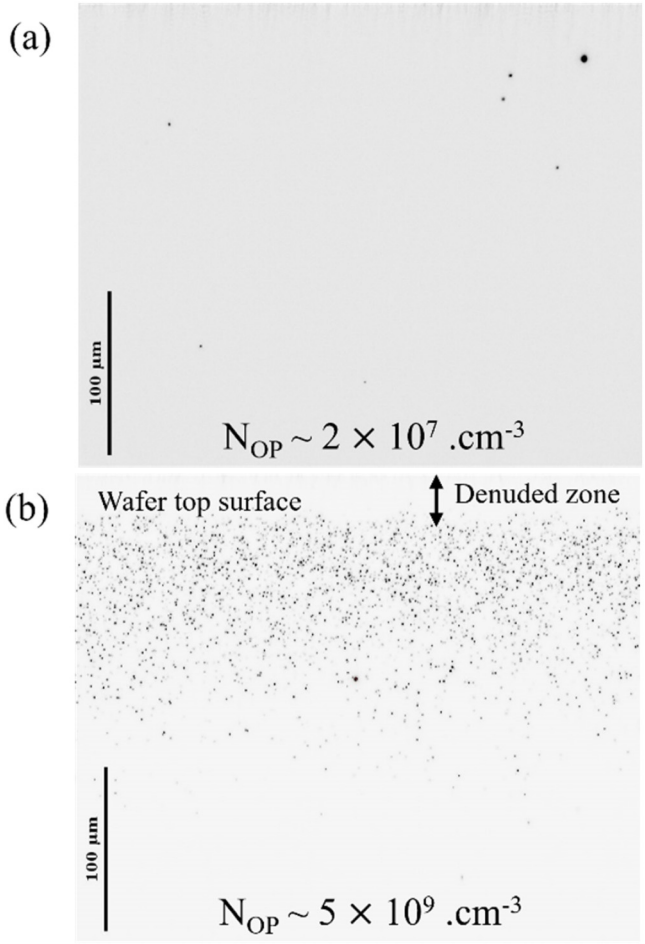

FIG. 1. Light scattering tomography cross section from annealed low (a) and (b) medium [O_i] Si substrates. The black dots appearing on images are oxide precipitates. Oxide precipitates density (N_{OP}) deduced from LST micrographs are annotated on the images. The denuded zone formed beneath the wafer surface is shown with an arrow in (b).

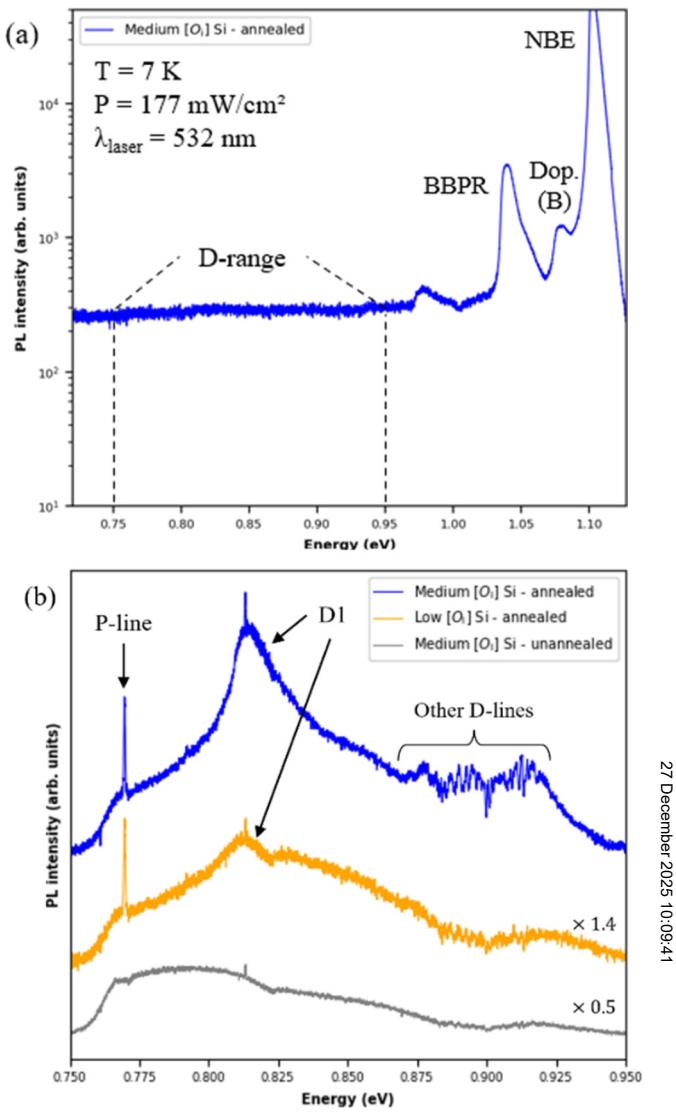

FIG. 2. (a) LTPL spectrum of the annealed/passivated HR Si medium [O_i] sample on a broad energy range, with the annotation of the main recombination, the measurement conditions are annotated on the plot. (b) Overlaid LTPL spectra of unannealed and annealed/passivated Si samples within the 0.75–0.95 eV range. P-line and D-lines are indicated on the plot. The recurrent sharp line at 0.813 eV is an artifact from the measurement setup, serving as a calibration reference.

evidenced in the medium [O_i] sample. Based on these observations, we correlated the oxide precipitate formation properties (density, size) with their optical signatures by LTPL spectroscopy. All samples were first measured over a broad energy range (0.7–1.15 eV) to simultaneously monitor both defect-related photoluminescence (PL) and near band edge (NBE) PL. The NBE PL spectrum, shown in Fig. 2(a) on a logarithmic scale, exhibits sharp and intense peaks corresponding to boron-bound exciton emission and its phonon replicas (BBPR).

Subsequently, the samples were compared in the defect-related PL region, located within the 0.7–0.9 eV range (referred to as the D-range), where a less intense and noisier PL signal is observed compared to the NBE region. To obtain meaningful data from the D-range, measurement conditions were set with longer acquisition times. Figure 2(b) compares the D-range PL spectra (0.75–0.95 eV) of annealed HR low and medium [O_i] samples with an unannealed HR medium [O_i] sample used as a reference.

From the spectra shown in Fig. 2(b), the following interpretation can be made: both HR low and medium [O_i] samples exhibit the broad D1 line centered at 0.81 eV. Although traditionally attributed to the presence of dislocations in Si, this peak is also known as a signature of oxygen precipitation, resulting from self-interstitial

silicon emission during oxide precipitate growth.[17–20] In the low [O_i] sample, where oxygen precipitation is limited, this optical signature can be observed under long acquisition measurement conditions. Notably, the D1 line is more intense and sharper in the medium [O_i] spectrum, suggesting a higher density of associated defects with less configurational variability (i.e., lower OP size heterogeneity), which is consistent with LST observations. We conclude that a precipitate population with a narrow size distribution tends to produce a correspondingly narrower D1 peak in the PL spectra.

Additional D-lines (in the 0.87–0.93 eV range), specifically the D2 line at 0.877 eV, is exclusively evidenced in the medium [O_i] spectrum. The detection of these lines is correlated with secondary defects induced by oxygen precipitation, which is consistent with previous literature.[18,19]

The sharp line at 0.767 eV, present in both annealed low and medium [O_i] spectra, suggests the presence of a well-coordinated complex rather than extended defects in Si. This line corresponds to the P-line emission, attributed to the thermal donor C_i–O_2 complex,[19,28] likely induced by the annealing. Given the thermal budget, these complexes could be related to new thermal donors (NTDs) formed at elevated temperatures via bonding with carbon impurities. The higher relative intensity of the P-line in the low [O_i] spectrum compared to the medium one suggests that complex formation is more dependent on the impurity level (C) than on the [O_i] concentration. Through LTPL analysis, we revealed the presence of emission lines that are likely related to thermally formed oxygen-related defects. To further correlate these optical signatures with their electronic energy levels and capture characteristics, we employed DLTS.

C. HR silicon diodes' characteristics for DLTS measurements

We performed DLTS on our set of HR annealed samples by preparing Schottky diodes. As preliminary tests, the following I–V, C–V, and C^{-2}–V curves at room temperature are presented in Fig. 3. From the I–V measurements, we estimated the Schottky barrier heights to be around 0.77 and 0.75 eV, respectively, in the low and medium [O_i] diodes.

From Fig. 3(a), in the diodes forward bias region, both samples exhibit high series resistance (R_S) in the kΩ range, with the medium [O_i] sample showing an order of magnitude higher R_S than the low [O_i] sample. Such high series resistance is linked to the high-resistivity nature of the samples and leads to elevated diode quality factors ($Q = R_S C_R \omega$, where C_R is the reverse capacitance, and $w = 2\pi f$ is the low-level alternative voltage frequency applied for C measurement). An increase in Q (>0.3) reduces the DLTS signal-to-noise ratio and shifts the maximum peak appearance in the temperature scan, resulting in erroneous extraction of trap parameters, as reported in the literature.[29–31] The Q factor evolves as a function of temperature because it is linked to free carrier density affecting both R_S (exponential increase in resistivity) and C_R (reduction with a 0.5 power law due to depleted region extension) and free carrier mobility affecting only R_S. As the frequency is fixed to 1 MHz, the Q factor can be minimized only by selecting appropriate voltage measurement windows (i.e., by

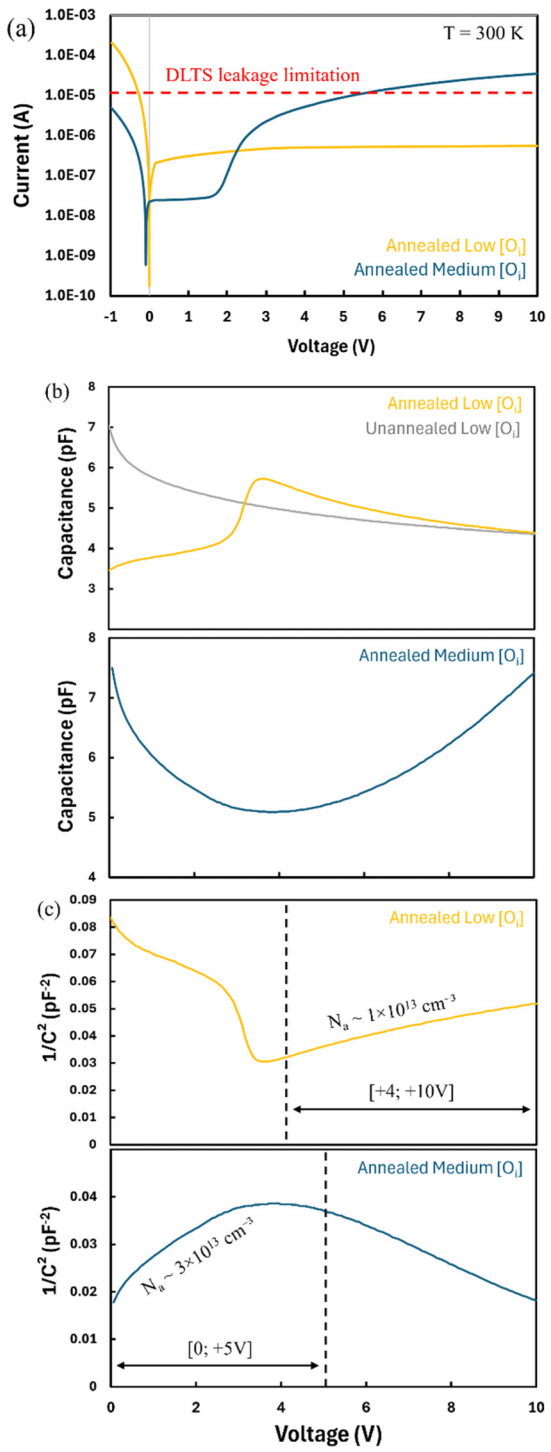

FIG. 3. (a) Room temperature I–V, (b) C–V [including the unannealed low (O_i) diode] and (c) C^{-2}–V curves measured on annealed HR low and medium [O_i] Schottky diodes. (c) The selected voltage windows for DLTS measurements and the corresponding doping densities.

choosing a lower C_R). Alternatively, analytic models can be applied (when $Q > 1$) to correctly determine the trap parameters, particularly trap densities (N_T).[29]

Regarding the diodes' reverse bias region, the leakage current is low even at high applied voltages for the low [O_i] sample. In contrast, an important increase in the leakage current beyond 3 V is observed for the medium [O_i] sample. This leakage current is likely due to the presence of extended defects in the Si bulk,[32–34] as expected from LST and LTPL analysis, which act as current generation centers. According to Schroder,[35] high leakage current characteristics can alter trap emission rates ($e_{n,app}$) according to the following equation:

$$e_{n,app} = e_n + \frac{J_{leak}\sigma_n}{q}, \quad (1)$$

where e_n is the standard trap emission rate (s^{-1}), σ_n is the trap capture cross section (CCS) (cm^2), and q is the elementary charge of the electron.

For a diode surface area of 7.85×10^{-3} cm^2, we maintained a diode leakage current below 10 μA at room temperature to minimize the $J_{leak}\sigma_n/q$ term in Eq. (1), by setting the voltage range between 0 and +5 V for DLTS measurements. This allowed us to benefit from lower C_R values and consequently reduced Q factors.

Additionally, to ensure the validity of the DLTS analysis of the medium [O_i] diode, exhibiting a high leakage current and expected high Q factors, we conducted I–V–T measurements to monitor the evolution of these parameters as a function of temperature, as presented in Fig. 4.

We observe from Fig. 4 that the leakage current of the medium [O_i] diode is below the 10 μA limit throughout the temperature scan of 80–300 K. Considering the Q factor, the value is below 0.25 from room temperature down to 130 K, which ensures appropriate conditions for the DLTS measurements in this temperature range.

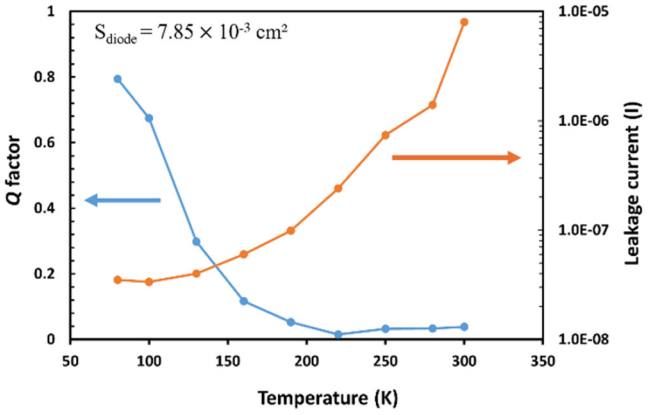

FIG. 4. Q factor and leakage current value at 5 V plotted as a function of temperature (80–300 K) for the medium [O_i] diode. The diode surface area is annotated on the plot.

From the C–V curves shown in Fig. 3(b), the HR low [O_i] diode exhibits an abnormal behavior characterized by C increasing between 0 and +4 V and a typical Schottky behavior beyond, at higher voltages. Such a deviation can be attributed to the presence of doping defects in the depleted region (W), likely induced by the annealing process, as evidenced by the comparison with the C–V curve of the unannealed sample. These doping defects are likely thermal donors as further supported by LTPL characterization. For the medium [O_i], an increase in the measured capacitance is observed above 4 V due to erroneous measurement caused by high leakage current.

Doping profiles were analyzed from the C^{-2}–V plots [Fig. 3(c)]. For a low [O_i] sample in the +4 to +10 V range, an almost constant N_a value of 1×10^{13} cm^{-3} is found. Therefore, for the low [O_i] diode, DLTS measurements were set within this voltage range of +4 to +10 V. For the medium [O_i] diode, the doping profile is constant in a limited voltage range (1–3 V). A mean N_a value of 3×10^{13} cm^{-3} was extracted in this range, and DLTS measurements were conducted next within 0 and +5 V range.

From the extracted doping densities, we can note that the samples are partially compensated relative to their intrinsic doping, due to the thermal donor formation. Consequently, trap densities are comparable to the semiconductor doping densities ($N_T \approx N_a$). As reported in the literature,[35] conventional DLTS (C-DLTS) under such compensated conditions leads to inaccuracies in extracted trap parameters, especially trap densities.

In our DLTS study, the analysis was conducted under the simplifying assumption of a uniform doping profile, as expected from the near-linearity of the C^{-2}–V curves within the selected voltage ranges for each diode. While compensation can influence the depletion region and carrier dynamics, its impact on the extracted emission rates and capture cross sections is considered moderate within the doping and trap density ranges investigated. Future work will focus on incorporating compensation-aware models to refine the DLTS analysis, as proposed in the literature.[36–38]

Furthermore, we chose not to report the N_T values for the analyzed samples, as these are likely to be further compromised by high Q factor effects discussed previously.

From these electrical tests, we highlighted the non-ideality of the annealed HR Si materials for C-DLTS measurements, due to high series resistance, leakage current characteristics, and compensated doping conditions where $N_T \approx N_a$. By adapting the voltage and temperature scan ranges, we aimed to ensure reliable information on deep level defects from DLTS analysis, although some deviations are expected in the extracted parameters.

D. DLTS characterization of annealed HR low and medium [O_i] silicon diodes

For the DLTS analysis, equilibrium depletion depths of approximately 30 and 17 μm are calculated, respectively, for the low and medium [O_i] samples. Consequently, the DLTS measurements will probe the silicon bulk, far from the surface and eventually the boundaries with the first OPs that can be detected in the

case of the medium [O_i] sample, at the limit with the denuded zone estimated in the LST micrograph.

For the low [O_i] sample, the DLTS signal remained low, with no detectable peaks across the entire temperature scan. Given the poor precipitation properties observed by LST in this sample (OP $\approx 10^7$ cm^{-3}), we expect that the trap concentration related to these precipitation features is below the DLTS detection limit ($N_T/N_a = 10^{-5}$), which corresponds to 10^8 cm^{-3} according to the extracted doping density. Therefore, the DLTS spectra of this sample were not plotted.

For the medium [O_i] diode, the DLTS spectra of are presented in Fig. 5. The DLTS analysis was conducted over the temperature range of 80–300 K due to the excessive leakage current at high temperatures.

The DLTS spectrum reveals three main traps, labeled T_1M, T_2M, and T_3M, within the temperature range of 100–220 K, at $T_w = 5$ ms. A subsequent trap emission at higher temperatures (T ≈ 250 K) is observed as T_w increases up to 200 ms. This peak is associated with a close midgap level, as indicated by its temperature emission characteristics. It can only be observed at long T_w because, at shorter T_w, the corresponding peak shifts to higher temperatures where measurements are affected by the increased leakage current. Given the near midgap position of this level, it likely facilitates electron capture and, consequently, carrier recombination, providing a parallel pathway for the removal of trapped holes from the level. In the high temperature range (250–300 K), the negative drop in the DLTS signal following the T_3M peak emission is attributed to the influence of the leakage current and is, thus, not related to minority carrier trap emission, such as traps potentially associated with thermal donors (around $E_c - 0.2$ eV).[39–41]

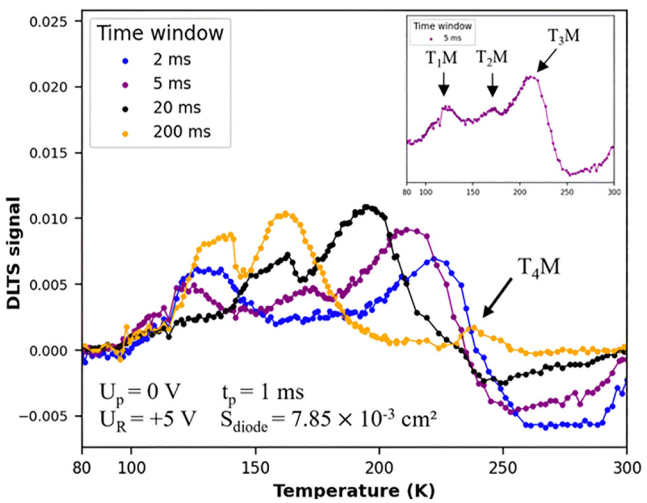

FIG. 5. DLTS spectra obtained from transient analysis for different time windows (T_w) for the sine Fourier coefficient b_1 of the annealed HR medium [O_i] sample. The inset in the figure highlights the presence of three peaks for $T_w = 5$ ms. The DLTS measurement conditions are indicated on the plots.

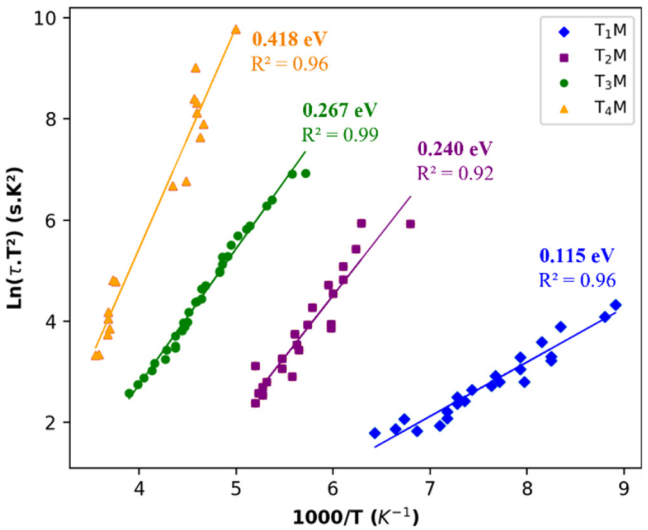

FIG. 6. Extracted Arrhenius plot from the DLTS spectrum of the annealed medium [O_i] sample.

The Arrhenius analysis from the b_1 sine Fourier coefficients at different T_w values is presented in Fig. 6, for the four detected levels in the medium [O_i] DLTS spectrum.

At low temperature, a deviation in the DLTS peak, due to the high Q factor, may cause substantial uncertainties in the extracted trap parameters for the T_1M level and in a lesser extent for T_2M ($Q < 0.3$). Additionally, the lack of many data points in the T_4M fingerprint is noted, due to the high-temperature peak occurrence where the leakage current increases. The extracted trap signatures are presented in Table II.

With a low activation energy of approximately 0.115 eV and a capture cross section (CCS) of about 10^{-19} cm^2, the T_1M trap is likely related to a charged level caused by metallic contaminants introduced during sample preparation. However, no low-temperature peak is detected in the HR low [O_i] diode subjected to the same fabrication process. Considering the high Q value in the temperature range of T_1M apparition, the interpretation for this level remains uncertain.

The T_2M and T_3M traps exhibit close activation energies but significantly different CCS values (four orders of magnitude),

TABLE II. Trap signatures extracted from the Arrhenius analysis of the DLTS spectrum of the annealed HR medium [O_i] sample.

Level	Trap energy, $E_a = E_T + E_V$ (eV)	Capture cross section, σ (cm^2)
T_1M	0.115 ± 0.011	3×10^{-19}
T_2M	0.240 ± 0.025	1×10^{-16}
T_3M	0.267 ± 0.006	1×10^{-20}
T_4M	0.418 ± 0.049	1×10^{-13}

suggesting that they may correspond to different charge states, so defects of different nature.

Relying on the literature for the T_2M trap, its signatures are in good agreement with trap P1,[21,22,26] identified in p-type oxygen-precipitated substrates with high [O_i] levels. Notably, this trap is observed only when secondary defects (such as PODs and stacking faults) are associated with oxide precipitates, consistent with the OP size distribution extracted from LST analysis. LTPL analysis has revealed additional D-line emissions (between 0.87 and 0.93 eV) in this sample, likely related to oxygen precipitation secondary defects. Furthermore, previous studies have attributed this trap to device leakage currents.[32–34] To confirm this hypothesis, we have analyzed the medium [O_i] diode leakage current activation with temperature according to the following equation:[35]

$$I_{leak} = SA^* T^2 \exp\left(-\frac{E_a}{kT}\right), \quad (2)$$

where S is the diode surface area (cm^2), A^* is the effective Richardson constant (equal to 120 A cm^{-2} K^{-2} for p-type Si), T is the absolute temperature (K), E_a is the trap activation energy (eV), and k is the Boltzmann constant.

As shown in Fig. 7, focusing on the temperature range where the leakage current is significant (between 220 and 300 K), we extracted from the slope of the linear regression and activation energy between 0.13 and 0.24 eV, which is compatible with the activation energy of the T_2M trap.

The extracted properties of the T_4M trap show an activation energy close to midgap, accompanied by an important CCS of $\approx 10^{-13}$ cm^2. Such a large CCS may indicate an extended defect nature. Thus, it is possibly related to precipitates in the silicon crystal.

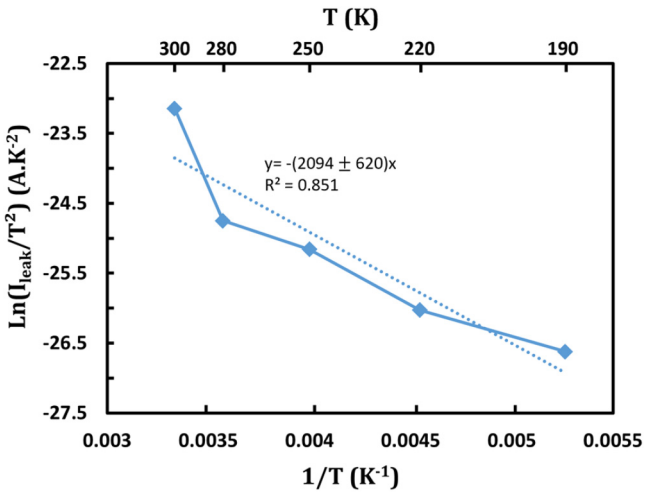

FIG. 7. Arrhenius plot related to the thermionic current emission of the medium [O_i] diode.

The midgap characteristics of the T_4M level suggest an association with oxide precipitates, as previously reported for interface states at the OP/Si matrix interface[24,25] in p-type standard silicon. Given the properties of the T_4M trap, this crystal defect may be detrimental to the performance of HR Si based devices, acting as a carrier generation–recombination center.[35]

Additionally, a recent study identified two levels associated with oxide precipitates and induced dislocations, respectively, at $E_V + 0.43$ eV with a $CCS \approx 4.0 \times 10^{-15}$ cm^2 and $E_V + 0.26$ eV with a $CCS \approx 7.0 \times 10^{-16}$ cm^2, in annealed p-type silicon (resistivity ≈ 1 Ω cm) with high [O_i] content ($\approx 1 \times 10^{18}$ cm^{-3}).[42] These trap properties are close to those observed in our analysis of the annealed HR Si sample with lower [O_i] content ($< 5 \times 10^{17}$ cm^{-3}).

IV. CONCLUSIONS

In this study, we have, for the first time on high-resistivity (HR) industrial silicon (Si) wafers with low oxygen content [(O_i) < 10 ppma], correlated the physical characteristics of oxide precipitates (OP) formed by conventional precipitation annealing with the optical and electrical signatures of these precipitates using LTPL and DLTS techniques.

We highlighted the sensitivity of the LTPL technique by detecting the early stages of oxide precipitate formation in low [O_i] samples (<5 ppma), attributed to the D1 line at 0.81 eV. Furthermore, we confirmed the relationship between the D2 line (at 0.877 eV) and precipitation-induced secondary defects in medium [O_i] silicon.

Electrical measurements on diodes revealed non-ideal characteristics for conventional DLTS measurements with elevated Q factors and doping profile inhomogeneity. Hence, we adapted our experimental measurement conditions to overcome these limitations.

No detectable traps by DLTS could be associated with the HR low [O_i] sample, highlighting the limitation of this technique in HR silicon for detecting defect densities below 10^7 cm^{-3}. In contrast, the DLTS spectrum of the medium [O_i] sample revealed several traps, including T_2M and T_4M, with trapping properties of $E_V + 0.240$ eV, $\sigma \approx 1.0 \times 10^{-16}$ cm^2 and $E_V + 0.418$ eV, $\sigma \approx 1.0 \times 10^{-13}$ cm^2, respectively. We correlate these peaks to the presence of traps related to oxide precipitates and their associated secondary defects, which could be responsible for leakage currents in the fabricated devices. These findings will contribute to future strategies for the characterization of defects in industrial HR silicon substrates.

ACKNOWLEDGMENTS

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

J. Crozelon: Data curation (equal); Formal analysis (lead); Funding acquisition (equal); Investigation (lead); Methodology (lead); Writing – original draft (lead). **A. Abbadie:** Conceptualization (equal); Project administration (lead); Supervision (lead); Validation (lead); Visualization (equal); Writing – review & editing (equal). **G. Bremond:** Conceptualization (equal); Methodology (equal); Resources (equal); Software (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **T. Szarvas:** Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Resources (equal); Writing – review & editing (supporting). **J. M. Bluet:** Conceptualization (equal); Resources (equal); Software (equal); Supervision (lead); Validation (lead); Visualization (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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