Solid-State Electronics 207 (2023) 108722

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Investigating the correlation between interface and dielectric trap densities in aged p-MOSFETs using current-voltage, charge pumping, and 1/f noise characterization techniques ☆

Ruben Asanovski [a,*], Jacopo Franco [b], Pierpaolo Palestri [c], Ben Kaczer [b], Luca Selmi [a]

[a] DIEF, Università degli Studi di Modena e Reggio Emilia, Via P. Vivarelli 10, Modena, 41125, Italy
[b] imec, Kapeldreef 75, Leuven, 3001, Belgium
[c] DPIA, Università degli Studi di Udine, via delle Scienze 206, Udine, 33100, Italy

ARTICLE INFO

Keywords:
Traps
Dielectric characterization
MOSFETs
1/f noise

ABSTRACT

Dielectric defects play a crucial role in the reliability of MOSFETs. In this study, we aim to gain a deeper understanding of dielectrics' degradation by correlating the effective interface (N_{2D}) and bulk (N_{BT}) trap densities extracted by different characterization techniques (I-V, charge pumping, and 1/f noise) under different electrical stress conditions. Additionally, we establish an empirical relation between the increase of N_{BT} (estimated via 1/f noise measurements) and $N_{2D,eff}$ (estimated through the monitoring of threshold voltage shift) after stress. This relation is useful to calculate the expected increase in 1/f noise from the V_T degradation models typically made available by the foundries to circuit designers.

1. Introduction

Dielectric defects are the main cause of reliability issues in MOSFETs [1]. They can affect the mobility, subthreshold swing, and threshold voltage of the device. Moreover, newly generated defects during the operational lifetime can cause Bias Temperature Instability (BTI) [2] and Random Telegraph Noise (RTN) [3], which can jeopardize the device reliability. Furthermore, dielectric defects are also the main cause of 1/f noise [4], which significantly affects the performance of many electronic circuits and must be precisely estimated at design time.

Various characterization techniques are employed to estimate trap densities and monitor the degradation. However, different techniques may yield varying results and different sensitivities to particular types of dielectric defects. Therefore, a comprehensive evaluation of these techniques under various electrical stress conditions is required to gain a better understanding of the underlying mechanisms of dielectric degradation.

In this study, we aim to evaluate different characterization techniques to estimate the effective interface (N_{2D}) and bulk (N_{BT}) trap densities and their correlation to electrical stress conditions. We also establish an empirical relationship between the post-stress increase in N_{BT}, as estimated through 1/f noise, and the effective trap density $N_{2D,eff}$, as estimated through the monitoring of the threshold voltage shift. This relationship is useful for predicting the expected increase in 1/f noise after stress when the effect of stress on V_T is known.

2. Characterization techniques

The characterization techniques used in this work and their sensitivity to dielectric defects at different energies and spatial depths are summarized in Fig. 1. For the N_{2D} estimation, we utilized the charge pumping (CP) technique using a base-level sweep implementation [5], through the relation

$$N_{2D,it} = \frac{I_{CP}}{qWLf} \quad , \tag{1}$$

where I_{CP} is the maximum charge pumping current measured at the substrate, q is the elementary charge, A is the area of the device, f is the frequency, W and L are the device width and length, respectively. To estimate the variation of N_{2D} with stress we considered the threshold voltage shift (ΔV_T) as [6]

$$\Delta N_{2D,eff} = \frac{C_{ox}}{q}\Delta V_T \quad , \tag{2}$$

and subthreshold swing degradation (ΔSS) [7] as

$$\Delta N_{2D,it} = \frac{C_{ox}}{\ln(10)kT}\Delta SS \quad , \tag{3}$$

where C_{ox} is the effective gate dielectric capacitance per unit area, k is the Boltzmann constant, and T is the temperature. The determination

☆ The review of this paper was arranged by Sorin Cristoloveanu.

* Corresponding author.
E-mail address: ruben.asanovski@unimore.it (R. Asanovski).

https://doi.org/10.1016/j.sse.2023.108722

Available online 26 July 2023

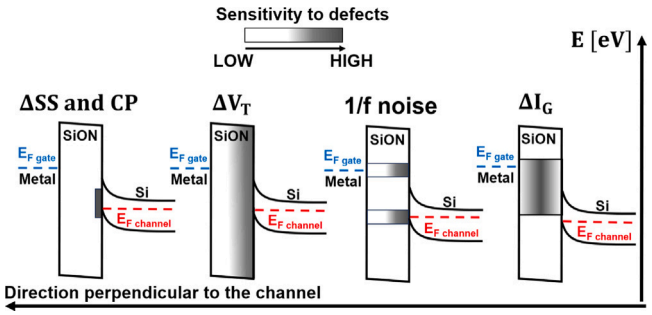

Fig. 1. Band diagrams of pMOSFETs in inversion highlighting the sensitivity to dielectric defects of the characterization techniques employed in this work.

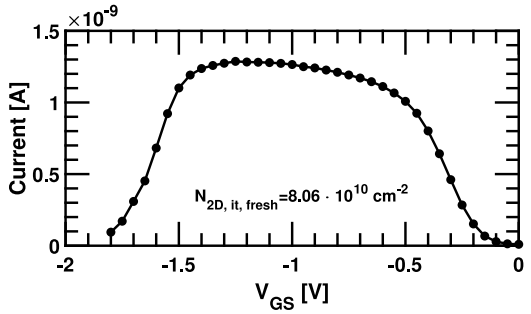

Fig. 2. Plot of the charge pumping current versus V_{GS} before stress. The charge pumping current is obtained by subtracting the charge pumping current measured at 1 kHz from the one measured at 1 MHz to eliminate bulk current components not related to traps. The pulse amplitude for the charge pumping measurement is 1.6 V. The value of fresh $N_{2D,it}$ is extracted from the peak current using Eq. (1).

of ΔN_{2D} via the change in threshold voltage, ΔV_T (Eq. (2)), includes also contributions from trapping in pre-existing and newly generated SiON bulk traps; therefore, it has been denominated $\Delta N_{2D,eff}$. The impact of trapped charge within the dielectric on the threshold voltage is weighted by the factor $(1 - z/T_{ox})$ [8], where z denotes the trap position perpendicular to the channel direction and T_{ox} corresponds to the dielectric thickness. Notably, Eq. (2) does not account neither for the spatial dependence of the trap concentration in the z direction nor for the factor $(1 - z/T_{ox})$. Hence, the parameter $\Delta N_{2D,eff}$ serves as an effective interface trap density, capturing the influence of the overall charge variation in the gate stack. The extraction of ΔN_{2D} using charge pumping techniques (Eq. (1)) might be influenced by bulk traps near the interface that can charge/discharge with times compatible with the pulsed measurement but to a lower extent. In this study, charge pumping measurements were conducted using pulses at a frequency of 1 MHz, which implies that only defects with capture/emission times within ≈0.5 microseconds would respond to the measurement [5]. Considering the exponential increase in capture and emission times due to electron tunneling towards bulk traps, charge pumping measurements primarily monitor the variation of interface traps. Similarly, the analysis of ΔSS (Eq. (3)) is anticipated to predominantly reflect the impact of interface defects capable of capturing and emitting charges within times compatible with the sweep time of the $I_D - V_{GS}$ measurement. For this reason, the N_{2D} extracted with Eqs. (1) and (3) has been denominated $N_{2D,it}$. It is expected that the values of $\Delta N_{2D,eff}$ extracted with ΔV_T (Eq. (2)) will be higher than the $\Delta N_{2D,it}$ values extracted with ΔSS (Eq. (3)) due to the contribution of bulk trap defects.

To estimate an effective value for N_{BT} we considered 1/f noise [4]

$$N_{BT} = S_{vg}\frac{WLC_{ox}^2 f\alpha}{qkT} \quad , \tag{4}$$

Table 1
Stress conditions applied to the pMOSFETs.

Condition	Temperature [°C]	Stress time [s]	V_{GS} during stress, V_{stress} [V]
(a)	25	1100	−2.4, −2.6 and −2.8
(b)	125	100	−3.1, −3.2, −3.3 and −3.4
(c)	125	7200	−3.1 and −3.2

where S_{vg} is the input-referred drain current noise and α is a tunneling coefficient routinely estimated through the WKB approximation and gate leakage current (I_G) increase with stress [9]

$$\Delta N_{BT}(\%) = \frac{\Delta I_G}{I_{G,fresh}} \quad . \tag{5}$$

The 1/f noise measurements on the drain current of MOSFETs provide insights into the behavior of traps whose occupancy fluctuates during the measurement. Consequently, the energy sensitivity of 1/f noise measurements is confined to traps located within a range of a few thermal energies (kT) from the Fermi level [10] of the reservoirs exchanging charge with the traps. Moreover, the extraction of N_{BT} from 1/f noise (Eq. (4)) is expected to display greater sensitivity to defects located near the interface (with a $(1 - z/T_{ox})^2$ weight [11]), owing to their higher electrostatic impact on the channel charge (thus the drain current). In contrast, the determination of N_{BT} using gate leakage current is more sensitive towards traps located at positions and energies favoring an increase in trap-assisted tunneling (TAT) current. When TAT predominantly occurs via a single defect acting as a "stepping stone", the N_{BT} determined through Eq. (5) will exhibit greater sensitivity to variations in the number of traps situated in the middle of the dielectric.

Regarding 1/f noise, Eq. (4) is derived from the general expression for the input-referred drain current noise [4]

$$S_{vg} = \frac{S_{id}}{g_m^2} = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha}\cdot\frac{1}{f}\cdot\left(1+\Omega\frac{I_D}{g_m}\right)^2 \quad , \tag{6}$$

where Ω is a parameter related to mobility fluctuations (MF), I_D is the drain current, and g_m is the transconductance. Note that Eq. (4) is valid only in the carrier number fluctuation (CNF) regime when $(\Omega I_D/g_m \ll 1)$. Therefore, all the trap extraction analysis is performed at low currents and above threshold ($V_{ov} = V_{GS} - V_T \approx -0.1$ V). The techniques introduced in this section are used to investigate the change in dielectric properties of p-MOSFETs after applying temperature and negative gate voltage stress V_{stress} (i.e., Negative Bias Temperature Instabilities conditions) as detailed in Table 1.

3. Measurements and discussion

We measured Silicon p-MOSFETs with SiON dielectric, T_{inv} = 2.5 nm, width (W) and length (L) equal to 10 μm and 1 μm, respectively.

We performed CP and 1/f noise measurements on fresh devices to estimate the values of $N_{2D,it}$ and N_{BT} before stress. The noise measurements are made with a Keysight A-LFNA low-frequency noise analyzer with V_{DS} equal to −100 mV.

The fresh $N_{2D,it}$ (Fig. 2) is extracted by subtracting from the peak CP current at 1 MHz the current at 1 kHz to eliminate current components related to gate leakage (and thus not related to traps), and then using Eq. (1). The fresh N_{BT}, instead, is extracted (Fig. 3) by measuring S_{vg} at $V_{ov} = -0.1$ V and then using Eq. (4).

After the characterization of the fresh devices, we apply the characterization methods of Section 2 to the stressed devices to evaluate the N_{2D} and N_{BT} increase with stress. The V_T is extrapolated from the linear $I_D - V_{GS}$ curve at the point of maximum transconductance [12], while the SS is extracted by taking the median value of SS in the 0.1 nA–100 nA drain current range. It is worth noting that this range was selected as the SS values remain roughly constant in this interval.

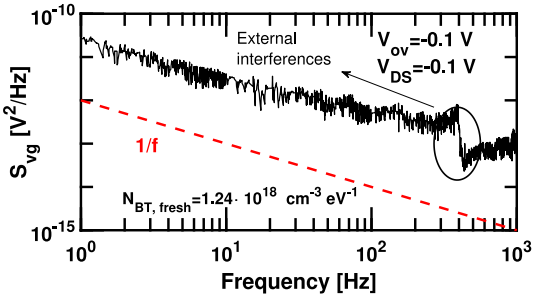

Fig. 3. Plot of S_{vg} versus frequency. Notice that S_{vg} goes as 1/f from 1 Hz to approximately 200 Hz. After 200 Hz, there is an external interference not related to the device. The value of fresh N_{BT} is extracted from S_{vg} using Eq. (4) with α = 1.4 ·10^{10} m^{-1}.

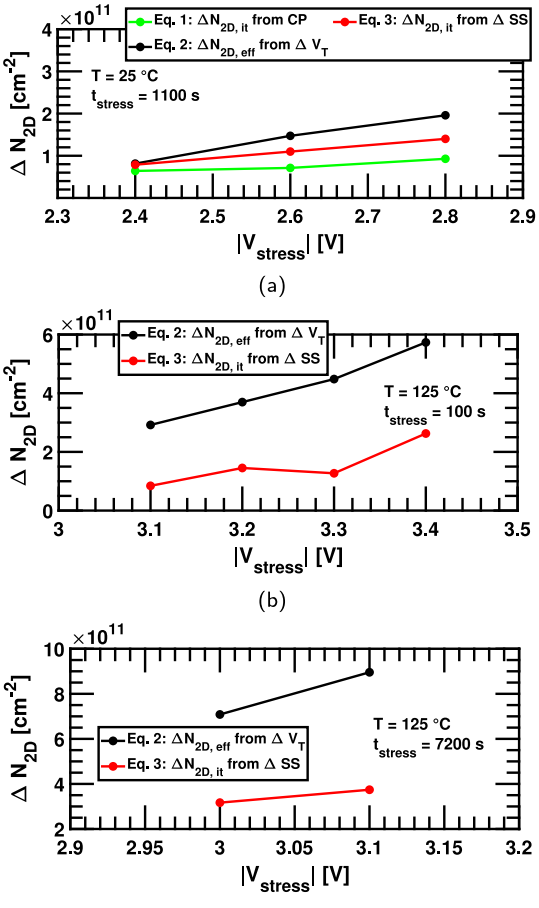

Fig. 4. ΔN_{2D} extracted through Eqs. (1)–(3) versus $|V_{stress}|$. Plots **(a)**, **(b)**, and **(c)** represent the data for stress conditions (a), (b), and (c) from Table 1, respectively. Eq. (2) yields a higher value of N_{2D} compared to Eq. (3), especially at elevated stress temperatures (b) and for long stress durations (c).

Fig. 4 compares the increase of trap density per unit area N_{2D} extracted with the different techniques. It is noteworthy that Eq. (2) yields higher values of N_{2D} than Eq. (3). This outcome is unsurprising since ΔV_T is more sensitive to the traps in the bulk of SiON compared to ΔSS (as detailed in Section 2). This is evident for high temperature and high voltage stress conditions (Figs. 4(b) and 4(c)). However, this difference becomes smaller at low-stress conditions (Fig. 4(a)), likely due to the small amount of degradation yielding larger extraction errors (especially Eq. (3) in the presence of small SS change). It is worth noting that the ΔN_{2D} values for the ΔV_T and ΔSS presented in Fig. 4 exhibit

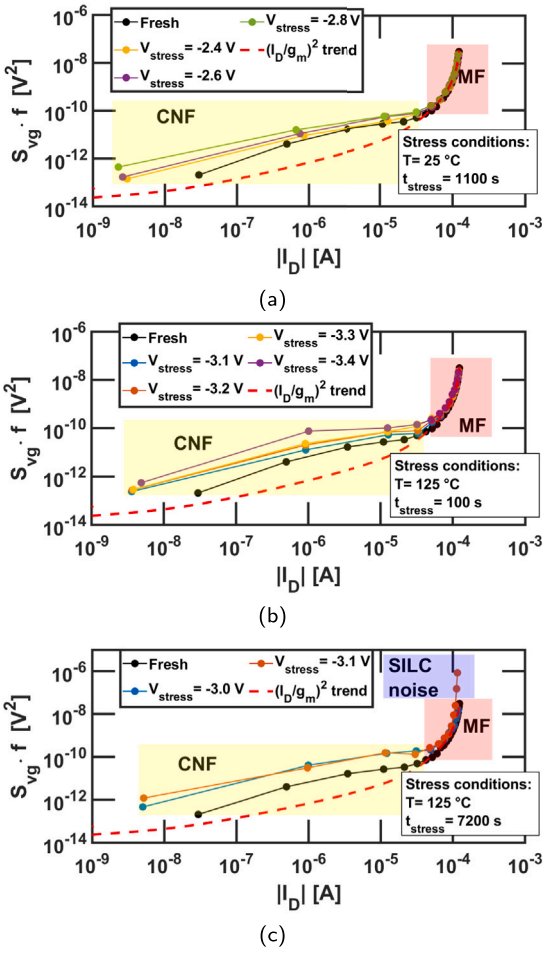

Fig. 5. Plot of $S_{vg} \cdot f$ (that is essentially flat over frequency between 1 Hz and 200 Hz for 1/f noise) versus the drain current. Plots **(a)**, **(b)**, and **(c)** represent the data for stress conditions (a), (b), and (c) from Table 1, respectively. The red dashed line is the $(g_m/I_D)^2$ scaled for a direct comparison with $S_{vg} \cdot f$ in order to identify the carrier number fluctuations (CNF) and mobility fluctuations (MF) regions.

consistent trends for increasing amount of stress. This implies that the defects generated during stress are detectable by all the techniques utilized in this study (see Fig. 1).

Fig. 5 plots the $S_{vg} \cdot f$ product (that is essentially independent on frequency) versus the drain current at V_{DS} = −100 mV, for the fresh device and the stressed devices of Table 1. No increase of S_{vg} is observed in the mobility fluctuations regime, suggesting that dielectric degradation does not affect noise at high currents. This contradicts the widely accepted view that mobility fluctuation is due to remote Coulomb scattering since this would increase with the dielectric degradation [4,13]. On the other hand, the electrical stress enhances the 1/f noise within the carrier number fluctuations regime. Moreover, Fig. 5(c) shows that the devices with high gate leakage current induced by stress exhibit a higher noise at very high I_D due to the stress-induced leakage current (SILC) flowing into the channel and increasing the overall 1/f noise.

Fig. 6 shows that ΔN_{BT} (estimated with 1/f noise via Eq. (4) at V_{ov} = −0.1 V) increases with increasing stress conditions, although it is difficult to establish the exact relation to $|V_{stress}|$ since uncertainties in the noise measurements generate significant error bars and make small changes in the N_{BT} difficult to assess. This increase is consistent with what was observed in other works [14].

Fig. 7 shows the percentage increase of N_{BT} estimated with ΔI_G via Eq. (5) at V_{ov} = −0.1 V vs. stress. This methodology can only

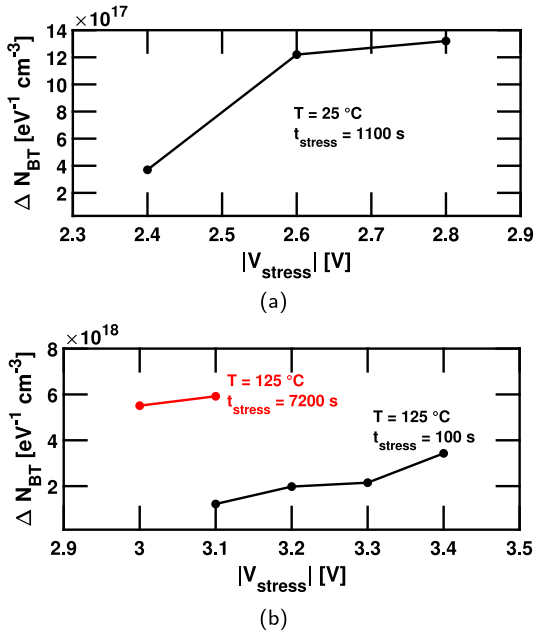

Fig. 6. Plot of ΔN_{BT} extracted through 1/f noise (Eq. (4)) versus $|V_{stress}|$. Plot **(a)** shows the data for stress condition (a) from Table 1, while plot **(b)** combines the data for stress conditions (b) and (c) from Table 1.

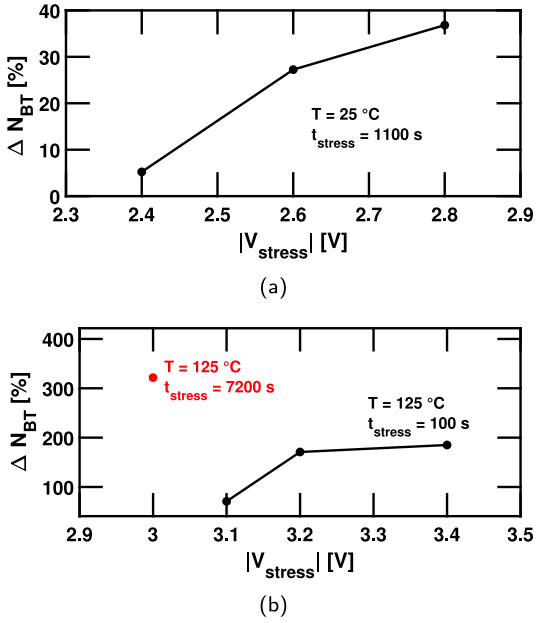

Fig. 7. Plot of the percentage increase of N_{BT} extracted through the increase of gate leakage current (Eq. (5)) versus $|V_{stress}|$. Plot **(a)** shows the data for stress condition (a) from Table 1, while plot **(b)** combines the data for stress conditions (b) and (c) from Table 1.

be applied under the condition that the variation of gate leakage is sufficiently small, such that it is reasonable to assume that the leakage still arises from TAT and scales linearly with the number of bulk traps N_{BT}; therefore, only a few data points can be used for the analysis.

The percentage changes of $N_{2D,it}$, $N_{2D,eff}$ and N_{BT} vs stress are compared in Fig. 8. Notice that $\Delta N_{2D,it}$ and ΔN_{BT} follow the same trends (especially at high temperature and voltage stress conditions), showing that the noise increase correlates with interface state degradation as assessed with the ΔSS. On the other hand, $\Delta N_{2D,eff}$ estimated through ΔV_T shows the largest changes as a function of stress, and it is

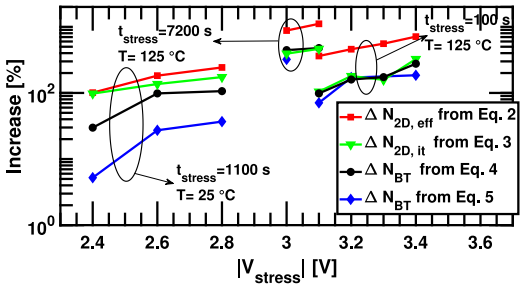

Fig. 8. Comparison between the overall increases of $N_{2D,it}$, $N_{2D,eff}$, N_{BT} with the methods of Section 2 and the stress conditions of Table 1.

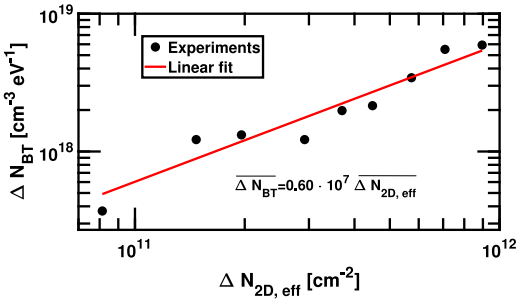

Fig. 9. Plot of ΔN_{BT} (extracted from 1/f noise with Eq. (4)) versus $\Delta N_{2D,eff}$ (extracted from ΔV_T measurements with Eq. (2)) for the measurements of Figs. 4 and 6. The increase in bulk dielectric trap density can be empirically related to the effective increase in interfacial trap density.

thus most effective in monitoring the overall dielectric degradation. As anticipated, the threshold voltage shift emerges as the most sensitive technique to detect variations in trapped charge within the dielectric (see Fig. 1). Moreover, the ΔN_{BT} extracted with 1/f noise and gate leakage match very well for high-stress conditions (i.e., entries (b) and (c) in Table 1). Notice that low-voltage SILC has been attributed to an increase of interfacial traps [15]; therefore, it is reasonable that it correlates well with the $N_{2D,it}$ trends. In general, it is observed that the traps generated under the bias and temperature stress conditions outlined in Table 1 are detectable through all the characterization techniques, as evident from the consistent trends depicted in Fig. 8.

Finally, Fig. 9 shows the increase of ΔN_{BT} as a function of $\Delta N_{2D,eff}$ for all the stress conditions explored in our work. Notice that there is a clear linear relationship

$$\Delta N_{BT}\ [\mathrm{cm^{-3}\ eV^{-1}}] = \beta\ [\mathrm{cm^{-1}\ eV^{-1}}]\Delta N_{2D,eff}\ [\mathrm{cm^{-2}}] \tag{7}$$

that can be fitted by one parameter $\beta = 0.60 \cdot 10^7\ \mathrm{cm^{-1}\ eV^{-1}}$. This empirical relationship suggests that the bias/temperature V_T shift models typically provided by foundries to designers can be also used to estimate the expected increase of 1/f noise in stressed devices.

4. Conclusions

We evaluated various characterization methods to monitor the degradation of the gate dielectric of pMOSFETs under bias/temperature stress conditions. Our results indicate that the ΔV_T method yields higher values of N_{2D} compared to the ΔSS method, especially at high-stress conditions due to the large contribution of charge trapping in pre-existing and newly generated bulk dielectric defects to ΔV_T. Similarly, we found that the ΔN_{BT} obtained from 1/f noise and gate leakage current is similar under high-stress conditions. Additionally, we noticed that the 1/f noise increases with stress only in the carrier number fluctuations regime, suggesting that the mobility fluctuations regime is not affected by the degradation of the dielectric. Finally, we established

an empirical relationship between ΔN_{BT} and $\Delta N_{2D,eff}$, which may be useful in calculating the expected increase in 1/f noise from an expected V_T shift (either measured or calculated from device aging models provided by foundries to designers).

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential

References

[1] Kaczer B, Franco J, Weckx P, Roussel P, Putcha V, Bury E, Simicic M, Chasin A, Linten D, Parvais B, Catthoor F, Rzepa G, Waltl M, Grasser T. A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability. Microelectron Reliab 2018;81:186–94. http://dx.doi.org/10.1016/j.microrel.2017.11.022.

[2] Grasser T. Bias temperature instability for devices and circuits. Springer Science & Business Media; 2013.

[3] Hung K, Ko P, Hu C, Cheng Y. Random telegraph noise of deep-submicrometer MOSFETs. IEEE Electron Device Lett 1990;11(2):90–2. http://dx.doi.org/10.1109/55.46938.

[4] Ghibaudo G, Roux O, Nguyen-Duc C, Balestra F, Brini J. Improved analysis of low frequency noise in field-effect MOS transistors. Phys Status Solidi (A) 1991;124(2):571–81. http://dx.doi.org/10.1002/pssa.2211240225.

[5] Groeseneken G, Maes H, Beltran N, De Keersmaecker R. A reliable approach to charge-pumping measurements in MOS transistors. IEEE Trans Electron Devices 1984;31(1):42–53. http://dx.doi.org/10.1109/T-ED.1984.21472.

[6] Liang M-S, Chang C, Yeow YT, Hu C, Brodersen R. MOSFET degradation due to stressing of thin oxide. IEEE Trans Electron Devices 1984;31(9):1238–44. http://dx.doi.org/10.1109/T-ED.1984.21694.

[7] Witczak SC, Suehle JS, Gaitan M. An experimental comparison of measurement techniques to extract Si-SiO2 interface trap density. Solid-State Electron 1992;35(3):345–55. http://dx.doi.org/10.1016/0038-1101(92)90238-8.

[8] Grasser T. Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities. Microelectron Reliab 2012;52(1):39–70. http://dx.doi.org/10.1016/j.microrel.2011.09.002, 2011 Reliability of Compound Semiconductors (ROCS) Workshop.

[9] Houssa M, Tuominen M, Naili M, Afanas'ev V, Stesmans A, Haukka S, Heyns MM. Trap-assisted tunneling in high permittivity gate dielectric stacks. J Appl Phys 2000;87(12):8615–20. http://dx.doi.org/10.1063/1.373587.

[10] Simoen E, Claeys C. On the flicker noise in submicron silicon MOSFETs. Solid-State Electron 1999;43(5):865–82. http://dx.doi.org/10.1016/S0038-1101(98)00322-0.

[11] Asanovski R, Palestri P, Caruso E, Selmi L. A comprehensive gate and drain trapping/detrapping noise model and its implications for thin-dielectric MOSFETs. IEEE Trans Electron Devices 2021;68(10):4826–33. http://dx.doi.org/10.1109/TED.2021.3104790.

[12] Ortiz-Conde A, Garcıa Sánchez F, Liou J, Cerdeira A, Estrada M, Yue Y. A review of recent MOSFET threshold voltage extraction methods. Microelectron Reliab 2002;42(4):583–96. http://dx.doi.org/10.1016/S0026-2714(02)00027-6.

[13] Barraud S, Thevenod L, Cassé M, Bonno O, Mouis M. Modeling of remote Coulomb scattering limited mobility in MOSFET with HfO2/SiO2 gate stacks. Microelectron Eng 2007;84(9):2404–7. http://dx.doi.org/10.1016/j.mee.2007.04.032, INFOS 2007.

[14] Samnakay R, Balandin AA, Srinivasan P. Reliability characterization of SiON and MGHK MOSFETs using flicker noise and its correlation with the bias temperature instability. Solid-State Electron 2017;135:37–42. http://dx.doi.org/10.1016/j.sse.2017.06.003.

[15] Nicollian P, Rodder M, Grider D, Chen P, Wallace R, Hattangady S. Low voltage stress-induced-leakage-current in ultrathin gate oxides. In: 1999 IEEE international reliability physics symposium proceedings. 37th annual (Cat. No.99CH36296). 1999, p. 400–4. http://dx.doi.org/10.1109/RELPHY.1999.761646.