

Early Detection of Potential Induced Degradation by Measurement of the Forward DC Resistance in Crystalline PV Cells

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Abstract—Potential induced degradation (PID) is still a serious threat for the photovoltaic (PV) industry and it is expected to aggravate due to the tendency to increase the operating voltage of PV systems. Therefore, a method which can detect PID at an infant stage is necessary in order to increase the reliability of PV systems and preserve their lifetime. This paper provides a pathway (proof of concept) for the early and reliable detection of PID, by using the forward dc resistance (FDCR) of a PV cell since it is a parameter, which is affected by the cell's shunt resistance (R_{sh}), which in turn is heavily affected by PID before any significant power loss occurs, and could act as a PID detection mechanism. The paper presents simulation results, which examine at which forward bias conditions the FDCR has to be measured for the purpose of using it as a PID detection means at an early stage (<1% power loss). The simulation examined the FDCR variation with shunt resistance, reverse dark saturation current (I_0), and ideality factor (n). Furthermore, an experiment was performed to verify the simulation results, demonstrating detection before 2% power loss occurs.

Index Terms—Early PID detection, forward dc resistance (FDCR), photovoltaic (PV), potential induced degradation (PID), shunt resistance.

I. INTRODUCTION

POTENTIAL induced degradation (PID) has been considered an important degradation mechanism in the last decade, especially for high-voltage photovoltaic (PV) systems (up to 1000 V dc). Laboratory tests on various PV modules have revealed that more than 67% of them are prone to PID and the trend to increase the operating voltage of PV systems to 1500 V dc will make the PID effect more severe and might even affect performance warranties [1]. Several methods to prevent it or slow its progression have been proposed, however, their practical implementation is subject to cost, performance, and long-term reliability [2], [3]. This paper deals with PID of the shunting type (PID-s) since it is the degradation mechanism that

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affects p-type crystalline PV cells, which dominate the market today.

The performance of a PV cell degrades fast when tested in the laboratory for PID under accelerated conditions. On the other hand, when the PV cells (PV modules) operate in the field (outdoor) and are subject to PID, their performance can degrade slowly and over a long time (more than a year). As a result, this failure mechanism can stay undetected for a long time by conventional power loss detection methods due to the combined measurement uncertainties which are higher than 5% [4]. Artificial neural network power loss estimation algorithms [5] can reduce the estimation error down to 1%, however, they require long-term training which defeats the early PID detection concept. Other researchers tried to employ the leakage current of a PV module as a detection means since it is directly related to the high voltage driving the PID, however, it was demonstrated that the leakage current is not directly related to PID progression [6].

Even though the cause of PID-s is known [7], there is still no widely accepted detection mechanism, which can be used in the field to sense the PID development in the PV modules under operation. The most common method for detecting PID is electroluminescence imaging, but this is time-consuming and costly as the modules have to be dismantled for indoor testing. Outdoor methods reported for the detection of PID are the use of a drone copter with a thermal camera to identify PID affected modules [8], impedance spectroscopy [9], and outdoor electroluminescence and photoluminescence imaging [10]–[13]. The outdoor methods avoid module dismantling but they still require relatively expensive equipment, frequent scans, and the labor cost for the test preparation is high. Therefore, a new detection technique is required [14]. We propose the use of electrical quantities which can be measured with cheap equipment continuously and without any human intervention.

Spataru [15], Hacke [16] and Luo [17] have presented a power loss estimation technique due to PID based on dark current-voltage (IV) curves. Their estimation technique achieves 3% accuracy, while our target is to detect PID before 1% power is lost. Our work [18]–[21] is in the same direction by examining the shunt resistance (R_{sh}) of the PV cell. The shunt resistance is a parameter that changes steeply with PID [22]–[25] and it could be used for the early PID detection in the field before any significant power loss occurs. The shunt resistance will not be

measured directly but instead the forward dc resistance (FDCR) will be measured since its value depends on the shunt resistance (see Section II).

Outdoor testing has so far positively asserted that the shunt resistance (R_{sh}) of a PV cell is affected by PID progression to a higher degree if it is measured at low forward/reverse bias conditions. The outdoor experimental results have demonstrated this for forward and reverse dark IVs [18], [19]. Lausch [24] has also indirectly demonstrated this under indoor conditions in an effort to calculate cell parameters with dark IV curves. The FDCR is expected to be affected in a similar way but this needs to be studied.

The FDCR also depends on the reverse dark saturation current (I_0) and the ideality factor (n) as described in Section II. Taubitz [26] demonstrated that the power loss due to PID is not only due to the reduction of the shunt resistance (R_{sh}), but also due to an increase of the ideality factor. A similar observation was made by Lausch [24], Spataru [27], and Hacke [28]. An increase in the low-voltage region (0–0.4 V) loss (J_{02}) was observed for PV modules with different PID sensitivity [24], [27]. On the other hand, the high-voltage region (0.4–0.6 V) loss (J_{01}) was more pronounced in PV modules with high PID sensitivity [27]. The aforementioned recombination losses are expected to contribute to the reduction of the FDCR in addition to the shunt resistance, increasing the sensitivity of the proposed method to PID even more. Nevertheless, a study is needed to determine the extent at which the FDCR is affected by the increased recombination losses.

The higher sensitivity of the shunt resistance (R_{sh}) to PID at low bias conditions and the increase of the recombination losses with PID makes it necessary to study how they affect the FDCR in more depth as presented in the subsequent sections. The target is to find the forward bias currents at which the FDCR has to be measured depending on the required PID detection accuracy.

In this paper, a novel simulation and experimental study was conducted in order to assess the FDCR appropriateness as a tool for PID detection. The simulation study, for the first time, examined at which forward bias conditions the measurement of the FDCR is more sensitive for PID detection. The simulations carried out demonstrated that the lower the bias conditions the earlier the PID can be detected, i.e., the lower the power loss due to PID at the time of detection. This approach was then experimentally validated by monitoring the FDCR at different forward bias conditions. Our target is not to calculate the power loss by measuring the FDCR value but to provide a simplified method to monitor PID progression. Our method will not rely on IV curves but on the measurement of the FDCR at a single forward bias condition which is derived in this paper. This is a pathway for the development of a low-cost method for PID detection on multi-cell PV modules.

II. SIMULATION MODEL

In an effort to identify the best forward bias conditions for the assessment of the occurrence of PID, a model was developed based on the one-diode model [29], [30] for crystalline silicon

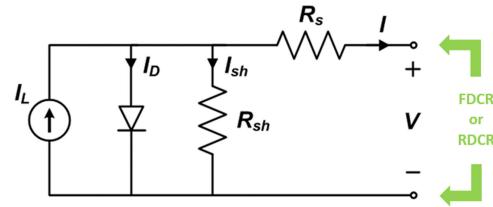


Fig. 1. One-diode model of a c-Si PV cell, showing how the FDCR and/or the RDCR are calculated.

(c-Si) PV cells (see Fig. 1). The model was used to calculate the FDCR of the PV cell under dark conditions with PID progression.

If a voltage is applied on the electrical terminals of a PV cell, its dc resistance can be measured. Depending on the polarity of the voltage, either the FDCR or the reverse dc resistance (RDCR) can be calculated based on the measured current as shown in Fig. 1. The FDCR was chosen instead of the RDCR mainly due to practical reasons since the bypass diodes used in PV modules will not allow the correct measurement of the RDCR. What is more, the FDCR is more predictable than the RDCR due to the many electrical non-linear parallel paths available for conduction in reverse bias which can vary among several manufacturers [31], [32].

Under dark conditions ($I_L = 0$ A), the resulting current consists of two components, the current through the shunt resistance (I_{sh}) and the current through the diode (I_D). Since the shunt resistance (R_{sh}) varies with PID progression, the FDCR varies as well. The proportion of the FDCR variation depends on the forward bias current it is measured; hence, a simulation was performed in order to identify the best bias conditions for PID detection. The FDCR variation with the diode current was studied as well since PID affects the recombination losses and hence the diode current.

In the simulation, the FDCR was calculated based on (1)–(4). A forward current (I) was applied at the terminals of the PV cell and the diode voltage (V_D) was calculated iteratively (1, 2). The voltage (V) at the terminals was then calculated (3) by considering the series resistance (R_s). Finally, the FDCR was calculated (4) based on the terminal voltage and current. The terminal current (I) was set to various values and at each value the shunt resistance (R_{sh}), the reverse dark saturation current (I_0) and the ideality factor (n) were varied independently to study their effect on the FDCR due to PID. The series resistance (R_s) and the thermal voltage (V_T) were kept constant. The actual values are defined in the methodology

$$I_D = I - \frac{V_D}{R_{sh}} \quad (1)$$

$$V_D = n * V_T * \ln \left(\frac{I_D}{I_0} + 1 \right) \quad (2)$$

$$V = V_D + I * R_s \quad (3)$$

$$\text{FDCR} = \frac{V}{I} \quad (4)$$

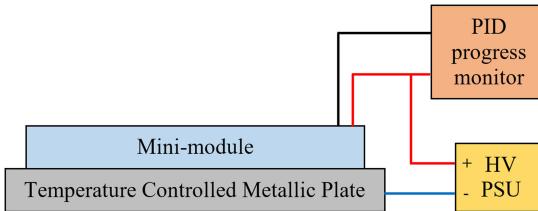


Fig. 2. Indoor PID test setup for inducing and monitoring PID progression of a single cell PV mini-module.

III. EXPERIMENTAL SETUP

For the experimental part, single cell p-type multi-crystalline silicon (mc-Si) PV mini-modules were used. The mini-modules were PID prone with a cell area of 243.4 cm^2 , 3 mm thick glass, x-23-105 EVA and TPT Akasol PV1000V back-sheet. The total surface area of the mini-module was approximately 400 cm^2 .

To induce PID in the PV cell, an indoor test setup (see Fig. 2) has been built which allows the temperature of the mini-module under test to be controlled while a high-voltage bias is applied at the same time to cause PID under dark conditions. A high-voltage power supply (HV PSU) was used for this purpose.

The glass facing side of the mini-module was placed on the metallic temperature controlled plate which was connected to the negative (−ve) terminal of the HV PSU. The power terminals of the mini-module were connected to the positive (+ve) terminal of the HV PSU through a dc resistance monitoring device (PID progress monitor). The resistance monitoring device (four-wire measurement) could be controlled to measure the resistance of the PV cell at various forward/reverse bias conditions while the high-voltage bias was being applied.

The setup was placed in a dark room and a Keithley source-meter device was used to acquire dark IV curves. The dark IV curves were used to analyse the FDCR at more forward bias conditions and were acquired with the four-wire measurement technique to eliminate the voltage drop across the wires in order to minimize the errors.

Finally, a solar simulator (flasher) was used to acquire the output power of the PV mini-modules at standard test conditions (STC) as PID was progressing. The measurement error of the equipment used is shown in Table I.

IV. METHODOLOGY

The methodology described next was followed to obtain the results, any deviation will be noted in the results section.

A. Forward Bias Conditions Simulation

With the objective of identifying the best forward bias conditions for the assessment of the occurrence of PID, a simulation was performed based on the one-diode model presented in Section II. The model was used to calculate the FDCR of the PV cell under dark conditions as its shunt resistance (R_{sh}), reverse dark saturation current (I_0), and the ideality factor (n) vary with PID progression. The three aforementioned parameters were varied independently, one at a time while keeping the other two

TABLE I
EQUIPMENT AND MEASUREMENT ERROR

Equipment	Measurement Error
HV PSU	< 1.0%
Source Meter (Keithley 2430)	< 0.1%
Solar simulator – Flasher (Pasan A+A+A+)	< 0.5%*
Cell temperature sensor (RTD)	< 0.5%
PID progress (DC resistance) monitoring device	< 1.0%

*The combined error is <1% (temporal instability <0.15%, irradiance uniformity <0.51%, and maximum power measurement <0.23%), however, the cell was always placed at the same location and hence the irradiance uniformity error was insignificant. Thus, the combined error was <0.5%.

TABLE II
SIMULATION VALUES TO TEST THE FDCR VARIATION WITH SHUNT
RESISTANCE (R_{sh}), REVERSE DARK SATURATION CURRENT (I_0), AND
IDEALITY FACTOR (n)

Case	R_{sh}	I_0	n
FDCR against R_{sh}	10 k Ω to 0.1 m Ω	5.82 nA*	1.15*
FDCR against I_0	50 Ω **	5 nA to 1 mA	1.15*
FDCR against n	50 Ω **	5.82 nA*	1 to 10

*Typical values for mc-Si cells [33]; **Simulated $P_{loss} < 0.01\%$ at STC.

constant (see Table II). The shunt resistance decreases with PID progression, whereas the reverse dark saturation current and the ideality factor increase. Since the temperature behavior of the tested parameters when they vary with PID progression is unknown, the cell temperature (T_{cell}) was set to 25 °C in order to demonstrate the concept. At 25 °C, the thermal voltage (V_T) was calculated to be 25.69 mV. The series resistance (R_s) of the cell was set to 15 m Ω (close to the 17 m Ω measured by the flash test at STC) for all cases.

In addition, the PV cell power loss (P_{loss}) was estimated based on the ratio of the output power change in each test case to the initial output power. The output power was calculated by finding the maximum power operating point of the cell at STC (short-circuit current set to 8 A). This was undertaken to assess whether it is possible to detect PID before any significant power loss occurs by using the FDCR method. The cell temperature (T_{cell}) was set constant at 25 °C in order to be able to directly compare the calculated power loss with the measured one from the flash test (solar simulator) which is also performed at 25 °C.

B. Experimental PID Progression

PID was induced by applying a voltage of −1000 V dc. During the HV bias, the cell temperature (T_{cell}) was kept constant at 60 °C (+/−1 °C) to accelerate the test time. The PID progression was monitored by measuring the FDCR. The measurements were performed at a forward bias voltage of 150 and 500 mV. The voltage was applied to the electrical terminals of the PV mini-module and the FDCR was calculated based on the measured current. The forward bias voltage levels were chosen

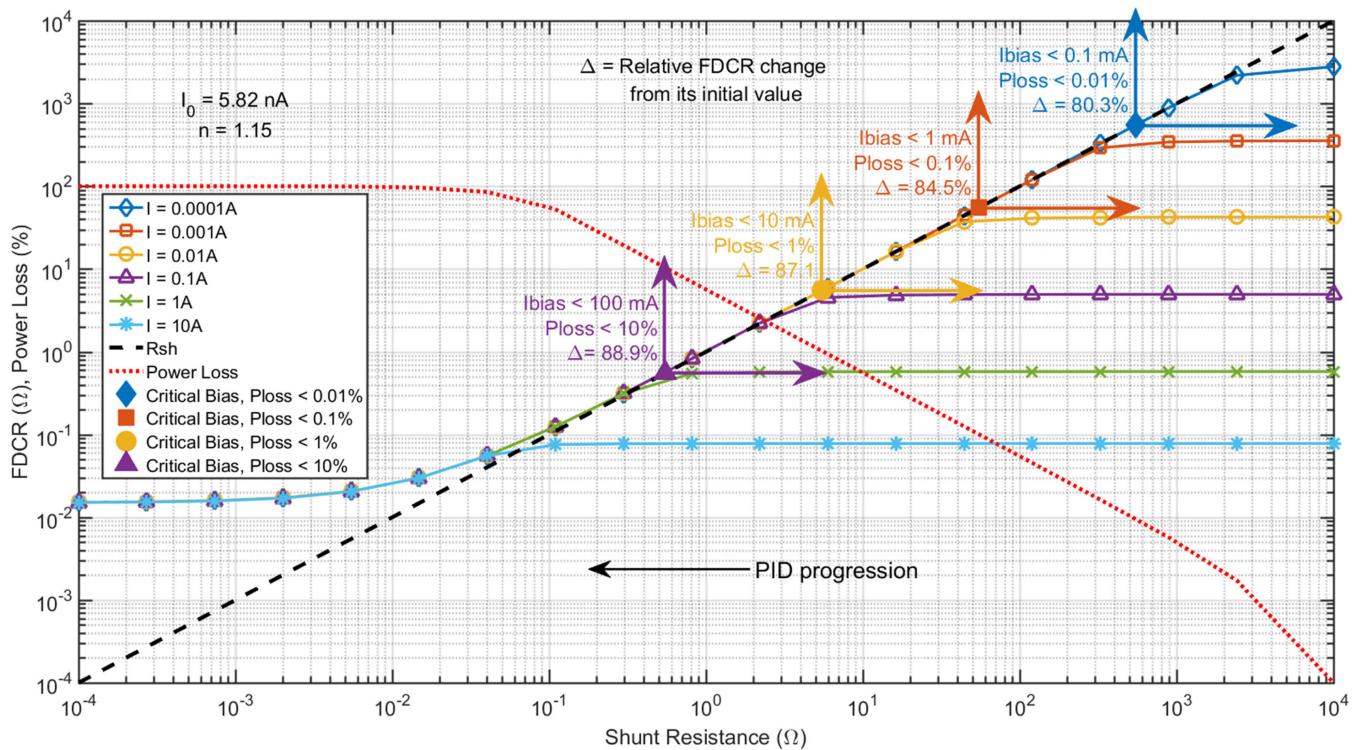


Fig. 3. Forward dc resistance (FDCR) and percentage cell power loss (P_{loss}) at STC against shunt resistance (R_{sh}) for various values of forward bias current. The initial cell output power at STC is 3.2 W. The more the PID progresses the lower the shunt resistance is. R_{sh} is shown as well in order to see at which point the measured FDCR matches the shunt resistance. Critical bias current values to detect PID before various power loss values are denoted by the arrows.

based on the simulation results (see Section V) to achieve a distinguishable comparison between the low and high forward bias conditions.

Since the shunt resistance is a good indicator for PID progression [26], it was approximated by measuring the RDCR of the PV mini-module at -0.5 V. Although the RDCR does not vary linearly with voltage, it gives a quite good approximation of the shunt resistance when measured at low reverse bias conditions [18]. The shunt resistance can be measured at forward bias as well but it requires very low bias conditions (<100 mV) [17] in order for the cell to be in a linear region and hence this was not studied due to the limitations of the monitoring device (PID progress monitor).

The FDCR and the RDCR were measured with a sampling rate of 10 s for a short period of time, i.e., every 10 s each of the three measurements (150 mV, 500 mV, -0.5 V) was performed for a duration of 75 ms. This was done in order not to bias the cell continuously and possibly affect its PID progression. The circuit was able to measure the dc resistance while the HV bias was applied in order to avoid any capacitive currents, which could affect PID progression, if the HV was switched ON/OFF every 10 s.

Dark FDCR curves (calculated from dark IV curves) were acquired as well to analyze the FDCR behavior with PID progression under a wide range of forward bias conditions for comparison with the simulation and also to estimate the shunt resistance with higher accuracy. Dark FDCR curves were recorded before starting the PID test (i.e., before applying the high

voltage) and then every time the RDCR was reaching a value of 10, 5, 2.5, 1, 0.5, and 0.25 Ω . The dark FDCR curves were recorded at a cell temperature (T_{cell}) of 60 °C ($+/- 0.25$ °C) within 5 s to keep the temperature change of the cell lower than 0.25 °C (verified by a thermal simulation).

The initial power of the cell (P_{cell}) was measured at STC prior to the PID test. In addition, every time and within 15 min (to reduce PID recovery) after the RDCR of the cell reached 10, 5, 2.5, 1, 0.5, and 0.25 Ω , the power of the cell was measured through flash tests at STC.

V. RESULTS

A. Forward Bias Conditions Simulation

Targeting to assess the best bias conditions for the measurement of the FDCR to detect PID occurrence, the FDCR variation with PID progression was calculated at different forward bias currents through a simulation based on the single-diode model (see Section II). The FDCR variation with PID was studied by varying the shunt resistance (R_{sh}), the reverse dark saturation current (I_0), and the ideality factor (n) as described in the methodology.

Fig. 3 shows the FDCR and cell power loss (P_{loss}) variation with shunt resistance (R_{sh}) for various values of forward bias current. From the results in Fig. 3, it can be seen that, initially, as PID progresses the calculated FDCR is constant (right-hand side of the R_{sh} curve) and does not change with the varying shunt resistance (R_{sh}) until the shunt resistance decreases below

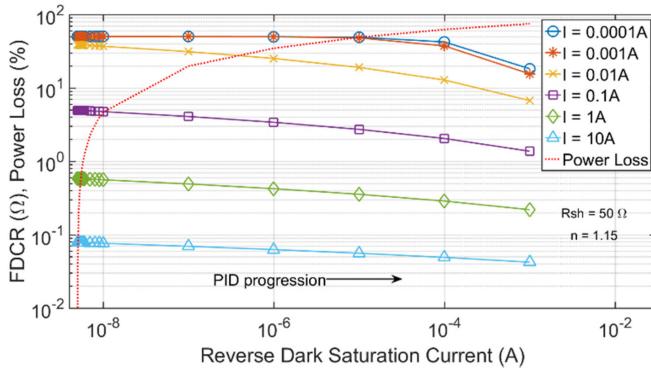


Fig. 4. Forward dc resistance (FDCR) and percentage cell power loss (P_{loss}) against the reverse dark saturation current (I_0) for various values of forward bias current. The initial cell output power at STC is 3.2 W.

a value which depends on the forward bias current. In addition, the constant FDCR region is wider with increased bias current, i.e., as the forward bias current increases the shunt resistance has to reduce more (i.e., PID has to progress more) in order to observe a change in the calculated FDCR. Our target is to detect PID at an early stage; before significant power loss occurs. For example, for 1% loss detection, it is possible to see that the forward bias current has to be less than 0.01 A (solid line with “o” marks) in order for PID to be detected before the output power decreases by 1%. This is deduced by finding the forward bias conditions (current values) at which the FDCR converges to the shunt resistance line (dashed line) before the power loss (dotted line) increases to 1%. With the visual aid of the critical bias area (arrows), the maximum current at which the FDCR converges to the shunt resistance before 1% power is lost is 10 mA. If earlier detection is required, before 0.1% or 0.01% power is lost, the forward bias current at which the FDCR has to be measured has to be lower than 1 and 0.1 mA, respectively. The bias current values were selected such that the relative FDCR change (Δ) is higher than 80% from its initial value for each power loss limit. Therefore, for the early detection of PID, the FDCR has to be measured at low forward bias conditions. Although not relevant to the PID detection, it is worth mentioning that the estimated FDCR converges to the series resistance of the cell (15 m Ω in this case) for high levels of PID degradation (i.e., very low shunt resistance).

As mentioned in the introduction, the reverse dark saturation current (I_0) and the ideality factor (n) change with PID progression and are expected to affect the FDCR. Figs. 4 and 5 present the results of the FDCR variation with the reverse dark saturation current and the ideality factor, respectively. From Fig. 4, it can be observed that as the dark saturation current (I_0) increases with PID progression the FDCR decreases. However, the FDCR variation before the power loss reaches 1% is insignificant and therefore the contribution of the reverse dark saturation current to PID detection (FDCR variation) at an early stage is negligible. Another useful result is that at low bias conditions ($I < 0.01$ A), the FDCR value is closer to the shunt resistance (R_{sh}) value. As a consequence and based on the result that the shunt resistance at low bias conditions changes steeply with PID progression

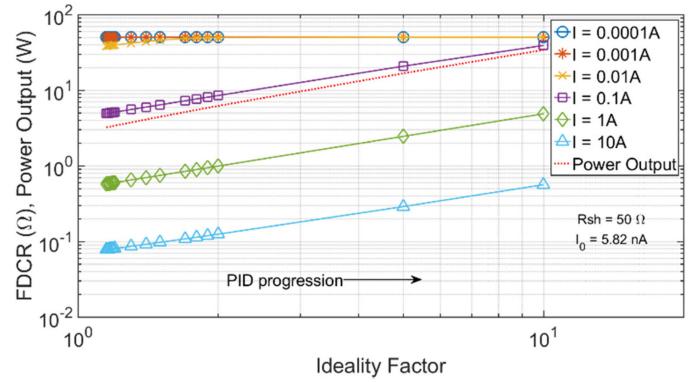


Fig. 5. Forward dc resistance (FDCR) and cell output power loss (P_{out}) against the ideality factor (n) for various values of forward bias current. The initial cell output power at STC is 3.2 W.

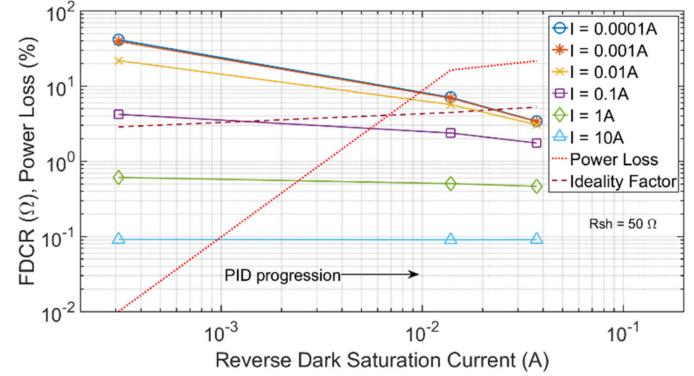


Fig. 6. Forward dc resistance (FDCR) and percentage cell power loss (P_{loss}) against the reverse dark saturation current (I_0) and ideality factor (n) for various values of forward bias current. The initial cell output power at STC is 4.1 W.

before 1% power is lost (see Fig. 3), measuring the FDCR at low bias conditions favours early PID detection. On the other hand, an increasing ideality factor (n) causes the FDCR and cell output power to increase (see Fig. 5). Again, while varying the ideality factor, the FDCR measurement at low bias conditions ($I < 0.01$ A) favours the early detection of PID since the FDCR value is closer to the shunt resistance value.

In reality, the reverse dark saturation current (I_0) and the ideality factor (n) change at the same time. The combined effect is a slower degradation rate that the one presented in Fig. 4. Since the exact proportion of change of the aforementioned parameters is not known to simulate the effect, real values calculated by Hacke [28] were used to demonstrate the effect on the FDCR (see Fig. 6). At high bias conditions (>0.5 A), the change on the FDCR is insignificant. At low bias conditions (<0.01 A), the FDCR change is more significant and adds positively to the reduction caused by the shunt resistance (see Fig. 3) aiding PID detection.

The simulation results demonstrated that for the early detection of PID (<1% power loss) with the proposed method, the FDCR has to be measured at low bias conditions (<10 mA). This is due to the exponential behavior of the cell p-n junction. The main parameter that affects the FDCR is the cell shunt

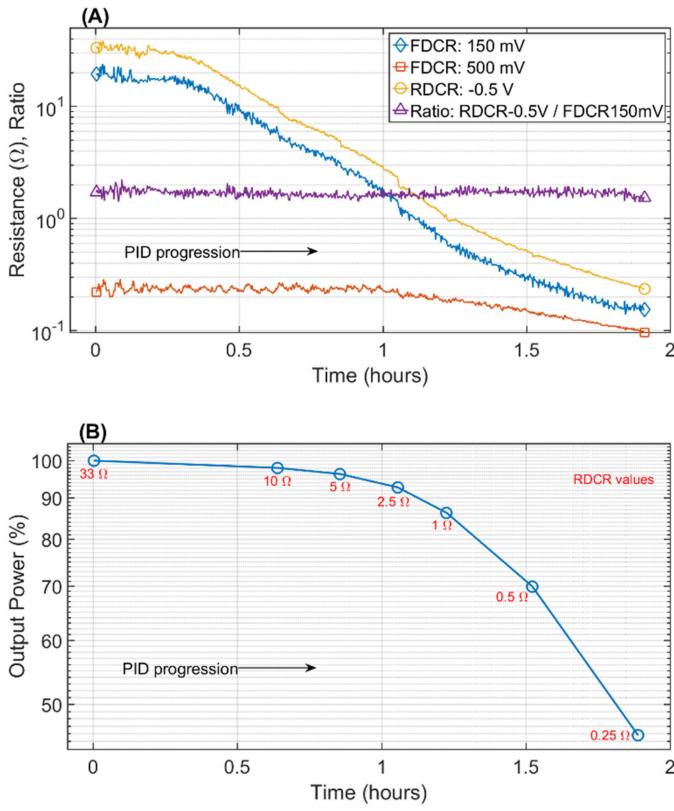


Fig. 7. (A) Forward dc resistance (FDCR) and reverse dc resistance (RDCR) at different bias conditions and (B) cell output power (P_{out}) against PID progression. FDCR and RDCR were measured at a cell temperature (T_{cell}) of 60 °C and the initial cell power at STC was 3.2 W. The ratio of the RDCR at -0.5 V to the FDCR at 150 mV is shown as well.

resistance. The reverse dark saturation current and the ideality factor partially counter-balance their effect with less change on the FDCR.

B. Experimental PID Progression

An experiment was performed to verify the results predicted by the simulation. The PID progression was monitored by measuring the FDCR and the RDCR as described in the methodology. The FDCR and the RDCR measurement data and the power measurements at STC are shown in Fig. 7. It can be observed that the RDCR of the cell decreases fast at the beginning as PID progresses while the output power of the cell (P_{out}) does not change significantly. A similar observation can be done for the FDCR at 150 mV, whereas the FDCR at 500 mV does not change until a significant amount of power is lost. The actual data are presented in Table III.

From the data, the relative change from the initial RDCR of 33.2 to 10 and 5 Ω is 70% and 85%, respectively. At the same time, the PV cell power loss (P_{loss}) at the RDCR values of 10 and 5 Ω is 2% and 3.7%, respectively. A similar observation can be done for the FDCR at 150 mV which decreases from 19.4 to 6.3 Ω (68% reduction) and to 3.1 Ω (84% reduction) for the same power loss of 2% and 3.7%, respectively. On the other hand, the FDCR at 500 mV started to change significantly

TABLE III
CELL POWER OUTPUT (P_{out}) AND LOSS (P_{loss}) AGAINST THE MEASURED REVERSE DC RESISTANCE (RDCR) AND FORWARD DC RESISTANCE (FDCR)

RDCR	FDCR _{150mV}	FDCR _{500mV}	P_{out}	P_{loss}		
Ω	Ω	%*	Ω	%*	%**	%*
33.2	19.4	0	0.22	0	100	0
10	6.3	67.5	0.22	0	97.97	2.03
5	3.1	84	0.22	0	96.28	3.72
2.5	1.5	92.3	0.22	0	92.69	7.31
1	0.63	96.8	0.18	18.2	86.22	13.78
0.5	0.29	98.5	0.15	31.8	69.92	30.08
0.25	0.16	99.2	0.1	54.4	45.77	54.23

*Relative change (%) compared to the initial value; ** $P_{out}-100\% = 3.2$ W.

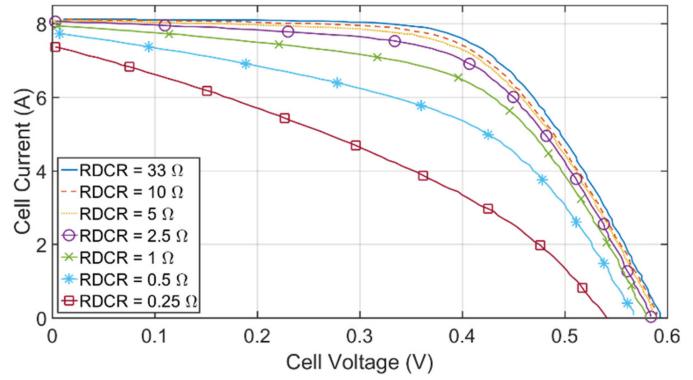


Fig. 8. Light IV curves at STC for various reverse dc resistance (RDCR) values (i.e., PID degradation levels).

($>10\%$ change) when the cell output power loss was higher than 7% (i.e., RDCR < 2.5 Ω). In this way, the concept of measuring the FDCR at low bias conditions for the early detection of PID is verified. Although the simulation predicted a power loss of 0.5% and 1% for shunt resistance (R_{sh}) values of 10 and 5 Ω, respectively, the experimental results demonstrated higher power loss, 2% and 3.7%, respectively (assuming the RDCR value is the cell shunt resistance). This can be attributed to the solar simulator uncertainty (up to 0.5%) and also due to the fact that the power loss in a PV cell due to PID is a combination of the reduction in the shunt resistance and increase of recombination losses [24], [26]–[28]. Nevertheless, this does not disprove the concept of detection before 1% power loss occurs. If the FDCR threshold for detection is set higher than 6.3 Ω, then the PID will be detected before 1% power is lost. The actual FDCR threshold will be studied later. Degradation testing at higher RDCR values (>10 Ω) and, hence, higher shunt resistance and FDCR values was not studied due to limitations in the testing procedure (the higher the shunt resistance the PID degradation is studied, the faster the PID recovery is).

The light IV curves (STC) used to obtain the maximum output power of the cell (P_{out}) at each RDCR with PID progression are shown in Fig. 8. The first parameter that changes with PID progression is the fill factor (FF) and then the open-circuit voltage (V_{oc}) confirming once again this well-known behavior.

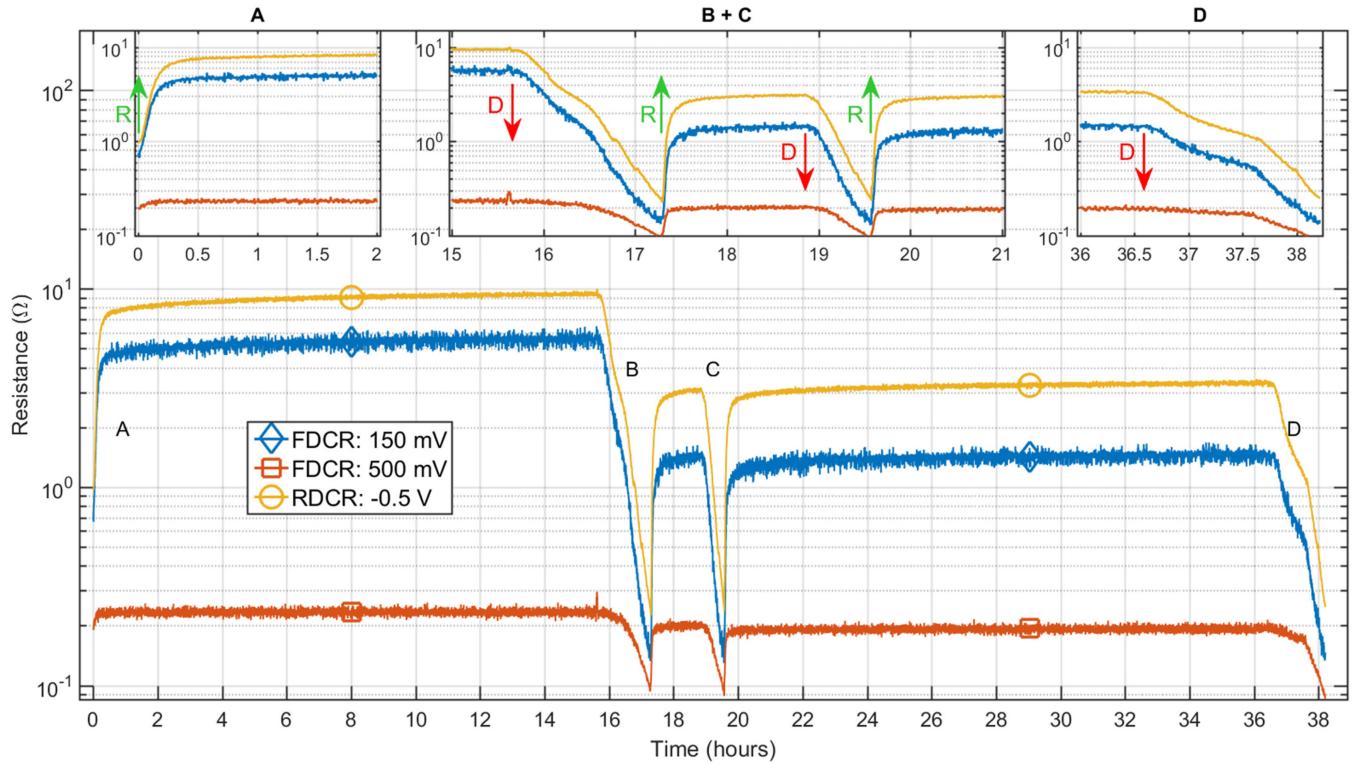


Fig. 9. Forward dc resistance (FDCR) and reverse dc resistance (RDCR) at different bias conditions against PID progression. The PID progression was a combination of recovery (R arrow, increasing R_{sh}) and degradation (D arrow, decreasing R_{sh}) at $+1000$ V and -1000 V dc respectively at 60 °C. Subplots A, B + C and D show a close view of the A, B + C and D areas of the main plot respectively. The recovery/degradation was started at the points denoted by R/D and continued until the next R/D event. The FDCR and RDCR were measured at a cell temperature (T_{cell}) of 60 °C and the initial cell power at STC was 3.2 W.

The short-circuit current (I_{sc}) seems to change similarly to the open-circuit voltage but this is not expected and can be attributed to the input resistance of the IV tracer. For a 60-cell PV module the IV tracer input resistance is not that important, however, for a single cell PV mini-module it makes a significant difference as its shunt resistance reduces with PID.

To demonstrate the robustness of the proposed method, the cell was subjected to a series of PID recovery/degradation cycles as shown in Fig. 9. For the results in Fig. 9, the test was performed 21 days after the initial test to obtain the results in Fig. 7 (day 1), i.e., the first degradation test was done 21 days before this series of recovery/degradation cycles was started. From day 1 to day 21, the cell was left at room temperature (15 – 18 °C) to recover slowly. This was done in order to show how the proposed detection method performs after different degradation stages. The recovery of the cell after day 21 was performed with a voltage of $+1000$ V dc at 60 °C.

From Fig. 9, the recovery of the cell occurs in less than 15 min and its shunt resistance was not stable for adequate time to allow flash testing. Therefore, the cell power variation with PID was only measured during the degradation phases. The measured output power at STC is presented in Table IV.

It can be observed that the RDCR and the FDCR at 150 mV increase (recovery) and decrease (degradation) with the same rate of change (i.e., they have a similar trend). In contrast, the FDCR at 500 mV is pretty much constant until the output power of the cell is well below its initial value. From the test, it is

TABLE IV
CELL POWER OUTPUT (P_{out}) AND LOSS (P_{loss}) AGAINST THE MEASURED REVERSE DC RESISTANCE (RDCR) AND FORWARD DC RESISTANCE (FDCR) AFTER A SERIES OF PID RECOVERY/DEGRADATION CYCLES

RDCR (Ω)	FDCR _{150mV} (Ω)	FDCR _{500mV} (Ω)	P_{out} (%)	P_{loss} (%)
Degradation Stage B				
33.2	19.4	0.22	100	0
9.8	5.5	0.22	96.84	3.16
5	2.6	0.22	95.19	4.81
2.5	1.19	0.2	91.6	8.4
1	0.48	0.17	79.04	20.96
0.5	0.24	0.13	64.17	35.83
0.25	0.15	0.1	44.45	55.55
Degradation Stage C				
2.5	1.1	0.19	87.82	12.18
1	0.4	0.14	77.07	22.93
0.5	0.22	0.12	58.29	41.71
0.25	0.13	0.088	40.92	59.08
Degradation Stage D				
2.5	1.1	0.19	88.07	11.93
1	0.43	0.16	79.26	20.74
0.5	0.22	0.11	61.04	38.96
0.25	0.15	0.085	43.3	56.7

$P_{out-100\%} = 3.2$ W.

shown that the proposed detection method at low bias conditions is able to capture both the degradation and recovery processes independently of the PID history of the cell, i.e., not affected whether the cell was subjected to slow (0 V dc HV bias) or fast

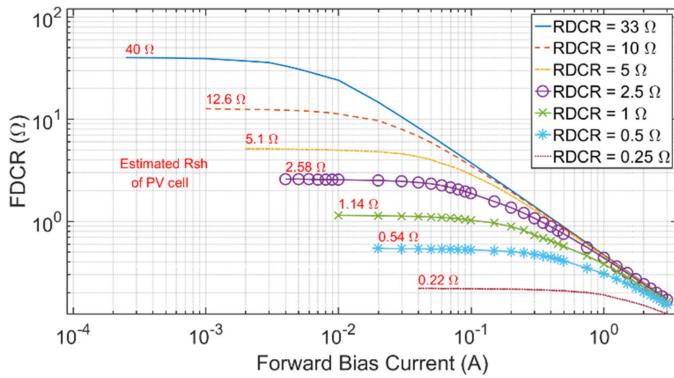


Fig. 10. Dark FDCR curves at different reverse DC resistance (RDCR) values (i.e., PID degradation levels). $T_{cell} = 60^\circ\text{C}$ and $P_{cell-100\%} = 3.2\text{ W}$ at STC. The shunt resistance (R_{sh}) was estimated from the FDCR curves.

(+1000 V dc HV bias) recovery or the duration (several days or a few hours) of the recovery process.

Another useful result that can be deduced is the progression rate of the FDCR at 150 mV and the RDCR with PID. If their ratio is calculated, the result is a constant value (see Fig. 7). This indicates that the same mechanism (cell shunt resistance) drives the observed changes in both the forward (FDCR) and reverse (RDCR) bias measurements. This is true for measurements at low bias conditions. At high bias conditions, other conduction mechanisms dominate (forward: diode current; reverse: non-linear paths and junction breakdown) which conceal the effect.

The experimental PID progression results indicate that the FDCR is a good parameter to be measured for the early PID detection (<2% power loss) at low forward bias conditions (<10 mA). The simulation predicted that it is possible to detect PID before 1% power loss but it was not possible to test it due to practical issues. It is also observed that for significant power loss (>2%), the FDCR at 150 mV has to be lower than $6.3\ \Omega$. This value corresponds to an RDCR value of $10\ \Omega$ (assuming that the RDCR value equals the cell shunt resistance). The results presented are for a cell with an initial (before PID) shunt resistance of $33\ \Omega$. In this study, other cells with higher initial resistances were encountered ($56, 122, 253\ \Omega$). A higher cell initial shunt resistance aids the detection due to the higher FDCR relative change before it reaches the critical value of $6.3\ \Omega$ (power loss < 2%). In this paper, the worst case is presented to test the proposed detection method. A shunt resistance threshold which will enable the PID detection before 1% power is lost will be studied later.

C. Dark IV Curves Analysis

It has been demonstrated that the FDCR is a good parameter to be used for early PID detection. This is enhanced from the results in Fig. 10 which presents dark FDCR curves at a cell temperature of 60°C . It is shown that the FDCR changes steeply with PID progression and especially at low forward bias conditions. It can be observed that the relative change in the FDCR reduces as the forward bias current increases. The FDCR at high bias current

TABLE V
RELATIVE FORWARD DC RESISTANCE (FDCR) CHANGE WHEN MEASURED AT DIFFERENT BIAS CONDITIONS

Forward bias current	Relative FDCR change (%)	Note
1 mA	79.7	The relative FDCR change was calculated from the initial reverse resistance (RDCR) to the $10\ \Omega$ value.
10 mA	55.0	According to the experimental results, at $10\ \Omega$ the power loss is lower than 2%.
100 mA	6.45	
1000 mA	0.85	

values tends to the same value except at severe PID conditions ($R_{sh} < 0.5\ \Omega$).

To further interpret the results of Fig. 10, Table V presents the calculated relative change of the FDCR at 1, 10, 100, and 1000 mA. From the data, the relative change of the FDCR from the initial RDCR to the $10\ \Omega$ value was calculated. The $10\ \Omega$ was selected because, according to the experimental measurements, it is the value at which the power loss is lower than 2%. The results show that the FDCR, when measured at 1 mA, has a relative change of 80% which is significantly higher (factor of 12) than the relative change (6.5%) when measured at 100 mA. A similar observation can be made for the 10 mA condition which experiences a relative change of 55%, 8.5 times higher than at 100 mA. On the other hand, the FDCR relative change is even smaller (<1%) when it is measured at 1000 mA. The analysis verifies the previous results (simulation in Section A and experimental in Section B) that the FDCR, when measured at low forward bias conditions, experiences a high relative change as PID progresses (i.e., as the shunt resistance of the cell changes due to PID) and can be used to monitor and detect PID at a very early stage. The high relative change in the FDCR and the low bias current means that a low cost PID monitoring device/sensor can be used.

Lastly, from Fig. 10, it can be observed that the FDCR value levels off at low bias currents. From this, the shunt resistance (R_{sh}) of the PV cell at the various PID stages can be estimated. The estimated value is close to the RDCR value.

VI. CONCLUSION

A proposed method for the early detection of PID is the measurement of the FDCR of the PV cell. This paper demonstrated that monitoring the FDCR at low forward bias conditions (forward bias current) can be a promising method for PID detection before any significant power loss occurs (<1%). The results presented are for single-cell PV mini-modules and it is the pathway for detection in multi-cell PV modules. A simulation demonstrated that to detect PID in a PV cell before 1% power is lost, the FDCR has to be measured at a forward bias current of less than 10 mA. It was also shown that earlier detection is possible with lower forward bias currents. The simulation examined the effect of the PV cell shunt resistance (R_{sh}), reverse dark saturation current (I_0), and ideality factor (n) on the FDCR since they are parameters which are affected by PID. The main contributor to the FDCR variation with PID was found to be the shunt resistance. Experimental results have verified that the lower the bias

current when measuring the FDCR the more sensitive the PID monitoring is (i.e., PID can be detected at an earlier stage). Due to practical limitations, it was only possible to demonstrate that PID can be detected before 2% power is lost. The presented PID monitoring method does not require full dark *IV* curves but measurement at a single forward bias current; this means a low-cost sensor can be used.

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