IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. **36** (2020) 024002 (8pp) https://doi.org/10.1088/1361-6641/abcb19

Characterization of defect states in Mg-doped GaN-on-Si p^+n diodes using deep-level transient Fourier spectroscopy

Y Lechaux[1], A Minj[2], L Méchin[1], H Liang[2], K Geens[2], M Zhao[2], E Simoen[2] and B Guillet[1]

[1] Normandie Univ, UNICAEN, ENSICAEN, CNRS, GREYC, 14000 Caen, France
[2] IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

E-mail: yoann.lechaux@ensicaen.fr and bruno.guillet@unicaen.fr

Received 15 July 2020, revised 4 November 2020
Accepted for publication 17 November 2020
Published 8 December 2020

Abstract

Mg-doped GaN-on-Si p^+n diodes have been fabricated and characterized by static electrical and deep-level transient Fourier spectroscopy (DLTFS) measurements. From static capacitance-voltage (C–V) and current–voltage (I–V) characteristics, we estimated the diffusion barrier of the p^+n diode close to the GaN band gap at room temperature. The temperature dependence of the capacitance showed freeze-out effect of the Mg-dopants at 200 K. From DLTFS measurements for various reverse bias and pulse voltages, two peaks were found and are composed of different defect states. The first peak with two components was related to diffusion of Mg p-type dopants in the n-GaN and V_N-related defects. The two components have activation energies close to 0.25 eV, from valence band and conduction band with a capture cross-section of $\sim 10^{-16}$ cm^2. The second peak with two components showed temperature shifts with the pulse height indicating a band-like behavior. This peak was commonly attributed to deep acceptor C_N-related defects with an activation energy of E_V +0.88 eV and a capture cross-section of 10^{-13} cm^2. A second acceptor level was found, with an activation energy of 0.70 eV and a capture cross-section of 10^{-15} cm^2. This second component was previously attributed to native point defects in GaN.

Keywords: GaN-on-Si, *pn* diodes, deep-level transient Fourier spectroscopy, defect states

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN is a promising material for numerous applications, from photonic devices such as blue light emitting diodes (LEDs) [1] to high power and high frequency devices such as high electron mobility transistors (HEMTs) or metal-oxide-semiconductor field effect transistors (MOSFETs). The quality of GaN epitaxy required for these devices is achievable in heterostructures grown by metal-organic-chemical vapor deposition (MOCVD) [2], molecular beam epitaxy (MBE) [3, 4] or hybrid vapor phase epitaxy [5, 6]. Due to the lack of cost efficient bulk GaN substrates [3], GaN based devices are realized on silicon carbide (SiC) [7, 8], sapphire (Al_2O_3) [9, 10] or silicon (Si) [11] substrates. It has been shown that devices fabricated on SiC substrates can deliver higher performance in terms of power density [7] due to the high thermal conductivity of SiC. Nevertheless, GaN-on-Si devices allow the exploration of new technologies and potentially facilitates wider integration of GaN [12]. However, GaN based devices suffer from a high density of defects. These defects commonly occur in GaN in the form of native point defects (nitrogen anti-sites, nitrogen or gallium vacancies), impurities

(oxygen and carbon substituted at nitrogen sites) or extended defects, with stress-induced threading dislocations as the most important ones [13]. Formation of dislocation allows for relaxation of highly mismatched GaN/substrate interface owing to strong difference in lattice constants and coefficient of thermal expansion. For example, GaN films grown on Al_2O_3, Si or SiC substrates suffer from compressive and tensile strains [14–16]. All these defects can degrade the device performance and reliability [17, 18].

The defect states in GaN based HEMT have been studied with different techniques such as low frequency noise [19–21], drain current transient spectroscopy [22–25] and deep-level transient spectroscopy (DLTS) [22, 25, 26]. In the same time, with the development of GaN MOSFET, *p*-type and *n*-type doped GaN Schottky diodes grown on Al_2O_3 [27–30] or on SiC [31, 32] substrates have also been studied. A few defect states were found but their origin is not completely understood and were attributed to nitrogen vacancies, Mg dopant or C impurities [13]. Besides, Mg-doped *p*-type GaN found a growth of interest because of the research on the development of blue LED [33]. Moreover, the use of Mg doping also turned out to play a crucial role in bringing HEMTs in the normally off/enhancement mode with a shift of the threshold voltage to positive values [34–36]. Also, many works about GaN *pn* diodes on Al_2O_3 [37], on GaN [38–41] and on Si [42, 43] substrates reported interesting electrical performance for power applications. Although the use of a Si substrate is promising for power applications with reduced cost of fabrication, there is a strong dependence of the electrical characteristics, breakdown voltage or OFF-current, on defects in GaN-on-Si *pn* diodes [44, 45]. So the understanding of GaN-on-Si *pn* diode defect properties is crucial for the development of GaN-on-Si based power devices [12].

In this work we investigated the defect characteristics of Mg-doped GaN p^+n diodes on Si substrates using a powerful technique, the deep-level transient Fourier spectroscopy (DLTFS) in order to extract the defects parameters.

2. Experimental details

2.1. Epitaxial layer

In this work, GaN p^+n diodes were fabricated at IMEC. The diodes were grown by MOCVD on Si substrates. The p^+n structure was composed of a 400 nm thick Mg-doped p^+-GaN layer at a doping concentration of 6×10^{19} cm^{-3} and of a 750 nm thick Si-doped *n*-GaN layer at 3×10^{16} cm^{-3}. We can note that Mg dopants have a rather deep acceptor level and exhibit freeze-out behavior [34] due to the Fermi level shift towards the valence band for lower temperature. This phenomenon is seen as a drop reduction of in the steady-state capacitance with decreasing the temperature at a fixed reverse bias U_R. This phenomenon is weakened due to high Mg doping concentration. Here, the Mg activation percentage is about 60% evaluated with secondary-ion mass spectroscopy by measuring Mg/H ratio.

A schematic representation of the diodes under study is depicted in cross-sectional view in figure 1(a) and in top view

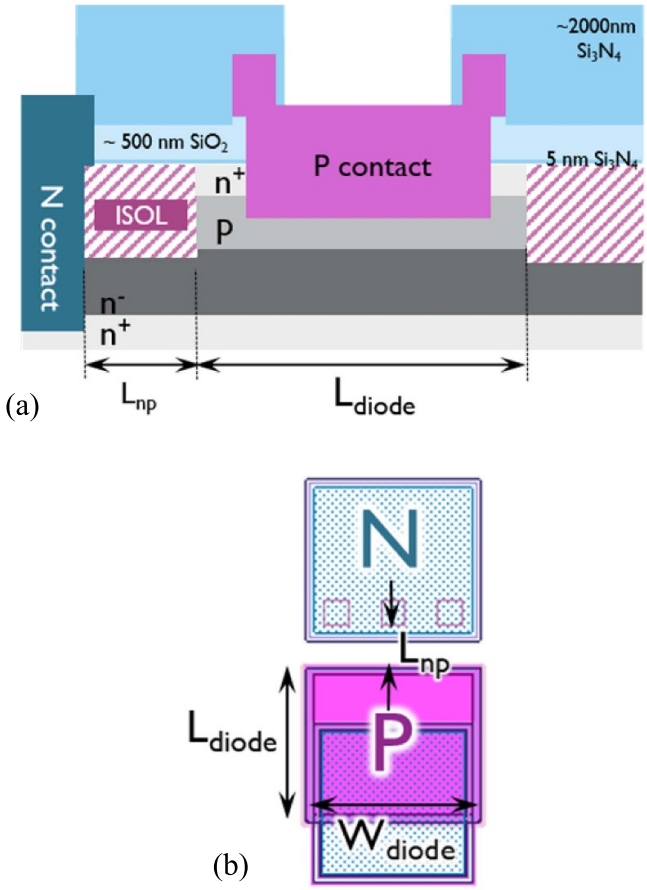

Figure 1. Schematic representation of the GaN-on-Si p^+n-diode under study, showing the diode in a cross-sectional view (a) and in top view (b). The diodes under study have an area of 100×112 μm^2 ($L_{diode} \times W_{diode}$) and there is a 14 μm distance between the top N and P contact area (L_{np}).

in figure 1(b). In the fabricated diode, a top n^+-GaN layer is present because trench gate transistors are integrated in the same wafer. It is etched out prior to *p* metal contact, hence, the role of the top n^+-GaN layer in the diode electrical characteristic is neglected. For the diode fabrication, a Si_3N_4/SiO_2 layer is used as surface passivation. Ti/Al/TiN containing metal stacks are used to contact the *p*-GaN layer and the bottom n^+-GaN layer from the top. These metal contacts are annealed at 565 °C. The top n^+-GaN and *p*-GaN layers are isolated towards the drain contact by using a N-implantation (see ISOL area in figure 1(a)). A 4 μm thick Al is put on top of the *n* and *p* contacts and a 2 μm thick Si_3N_4 layer is used as final surface passivation. The diodes under study have an active area of 100×112 μm^2 ($L_{diode} \times W_{diode}$). Both the *n* and *p* metal contacts are made at the frontside of the wafers with an L_{np} of 14 µm. The threading disclocation density was estimated using the in-plan transmission electron microscopy at about $1–3 \times 10^9$ cm^{-3} while x-ray diffraction gave similar readout.

2.2. The DLTFS

In order to characterize the defect states of the Mg-doped GaN p^+n diodes, DLTFS measurements were carried out.

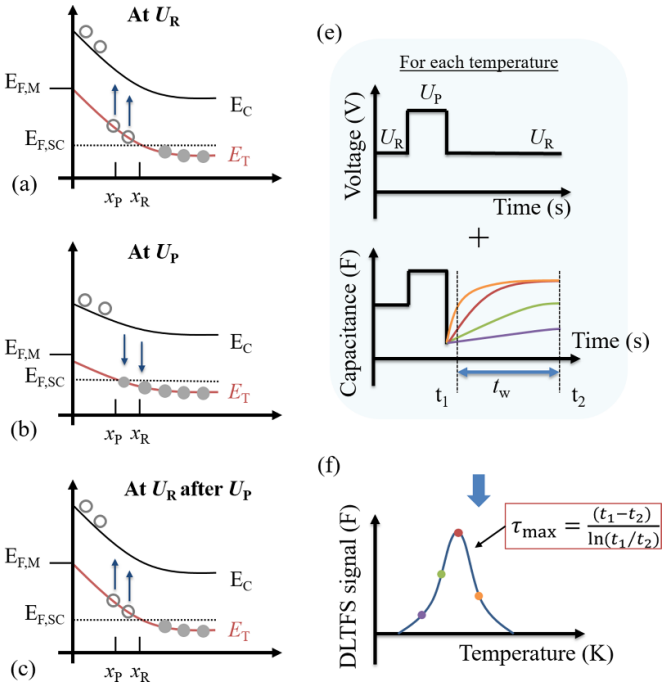

Figure 2. Principle of DLTFS. (a) First state at reverse bias voltage U_R with empty defect states within x_R, (b) a pulse voltage U_P is added to fill the defect states up to x_P, (c) after the pulse, the system goes back at reverse bias. (d) The capacitance transients are acquired at each temperature and the capacitance difference is calculated for several time windows *tw*. (e) Then, the DLTFS signal is extracted from capacitance transients as a function of the temperature.

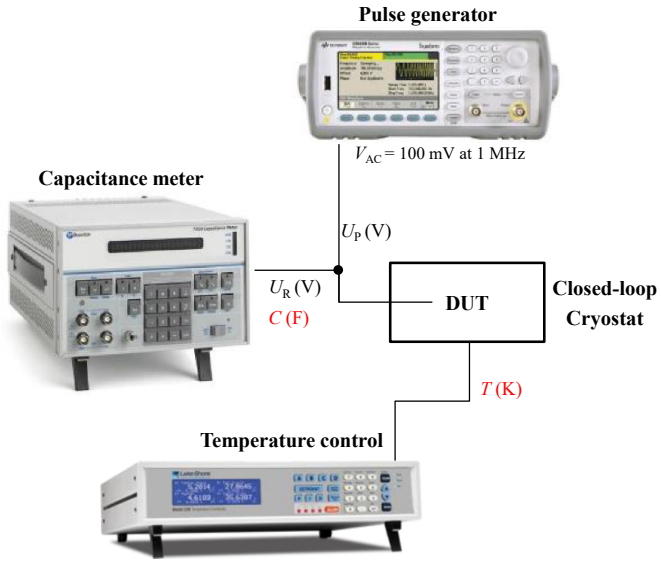

Figure 3. Schematic of the measurement setup composed of a capacitance meter (Boonton 7200), a pulse generator (Agilent 33500B), a temperature controller (Lakeshore Model 336) and a PhysTech FT-1230 HERA DLTS system (not shown). The sample is placed in a closed-loop He cooled cryostat.

These measurements are based on the observation of trap-dependent capacitance transients, originating from a depletion region in a semiconductor material [46–48]. One may visualize it in the following way: initially, the charges are trapped in those defect states at deep-level energy E_T (eV) that are lying below the Fermi level. By applying a reverse bias voltage U_R (V) (figure 2(a)), defect states emit their trapped charges (up to the depletion width x_R). Then, a pulse voltage U_P (V) (figure 2(b)) is applied and the charges are trapped again in the deep-level centers (up to the depletion width x_P). After the pulse (figure 2(c)), the defect states emit their trapped charges again with an emission time τ (s) and emission rate e (s^{-1}). The equation (1) below defines the electron emission rate e [49], where σ (m^2) is the capture cross-section, the term γT^2 (m^{-2} s^{-1}) corresponds to the product of the conduction band density of states and the thermal velocity of electrons, E_T is the defect state activation energy, E_C is the conduction band energy (eV), q is the elementary charge, k_B is the Boltzmann constant and T is the temperature.

$$e = \frac{1}{\tau} = \sigma\gamma T^2 \cdot \exp^{\frac{(E_C - E_T)}{qk_B T}}. \quad (1)$$

DLTS is based on measurements of capacitance transients that correspond to the response of the system after a voltage pulse for different time window t (from t_1 to t_2) at varying temperature (figure 2(d)). The capacitance difference ΔC (F) is extracted and converted into several coefficients (b_1 for example is used here) using Fourier transform in order to obtain the DLTFS signal (figure 2(e)).

2.3. Electrical characterization setup

The measurements have been performed through a PhysTech GmbH FT-1230 HERA DLTS system for measurement and data acquisition. The setup is composed of a Boonton 7200 capacitance bridge to apply the reverse bias voltage and measure the capacitance or conductance and of a Keysight 33500B to generate the fast pulse voltage (figure 3). Here the dynamic signal voltage and frequency are 100 mV and 1 MHz, respectively. The time windows used in this study were 100 ms, 300 ms, 600 ms, 1 s and 3 s. The sample is placed in a closed-loop Helium-cooled Janis cryostat and the temperature is controlled by a Lakeshore Model 336. The reverse bias and pulse voltage are applied between the p^+ and n contacts and are defined by U_R and U_P, respectively.

3. DC characterization

3.1. DC measurements at room temperature

In order to determine the structural type of the GaN p^+n diode, a capacitance–voltage (C–V) measurement was performed at room temperature in the bias range between −5 and 5 V and we extracted the power-law index k [50]. *pn* junctions can be broadly categorized under three structural types, an abrupt junction, a linearly graded junction, and a non-abrupt and non-linear junction. From equation (2), we can identify the structural type from the power-law index k. In this equation, V (V) is the applied voltage, V_D (V) the barrier height, A a factor dependent on parameters such as diode surface S (m^2) and

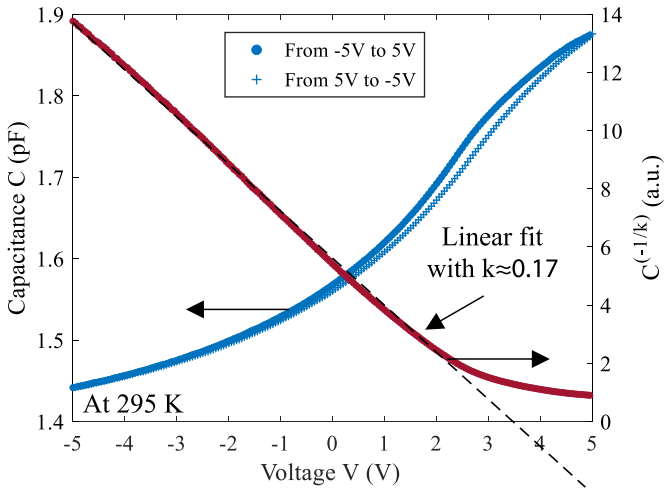

Figure 4. *C–V* characteristics at room temperature of the GaN p^+n diode showing a hysteresis for voltage between −5 and 5 V (left *y*-axis) and the $C^{-1/k}$–*V* curve with a linear fit allowing to extract the diffusion barrier of about 3.6 V (right *y*-axis).

GaN dielectric constant ε_0 and C (F) the capacitance. It is known that if $k = 1/2$ the junction is abrupt, if $k = 1/3$ the junction is linearly graded and the junction is graded and non-linear in the other cases [51].

$$V = V_{\mathrm{D}} + A\left(\frac{1}{C}\right)^{1/k}. \tag{2}$$

Using the procedure detailed by Wang *et al* [50], we find the equation (3) which is independent of A.

$$V = V_{\mathrm{D}} + k \cdot \frac{\mathrm{d}V}{\mathrm{d}\left(\frac{1}{C}\right)}\left(\frac{1}{C}\right). \tag{3}$$

Then from the plot of V against $\frac{\mathrm{d}V}{\mathrm{d}\left(\frac{1}{C}\right)}\left(\frac{1}{C}\right)$, we can extract V_{D} from the intercept of the fitting line with the *y*-axis and the power-law index k from the slope. Figure 4 shows the *C–V* and $1/C^{1/k}$–*V* curves along with its linear fit using the extracted power-law index k. We found a hysteresis in the *C–V* curve, which is indicative of defect charging effects. Besides, we observed a linear $1/C^{1/k}$–*V* curve for $k \approx 0.17 \pm 0.01$ indicating a graded and non-linear p^+n junction at room temperature. The linear fit of the $1/C^{1/k}$–*V* curve allowed the extraction of the diffusion barrier of the junction, which is about 3.6 ± 0.2 V at 295 K. This value is slightly larger than the theoretical value, of about 3.25 V at 295 K. It is possibly due to the series resistance with contribution from contact resistance and from resistance of the quasi-neutral region in the *n*-type GaN with a doping level of about 10^{16} cm^{-3}.

3.2. DC measurements—temperature dependence

Figure 5 shows the temperature dependence of the static characteristics (*C–V* and *I–V*) in the range 100 K–410 K with 10 K steps. First in figure 5(a), we observed an increase of the capacitance with temperature because of the dependence of the active Mg concentration in the *p*-GaN layer with the temperature. It is observed in the *C–T* curve obtained at a reverse bias of −5 V (figure 5(b)), where the Mg-dopants freeze-out occurs around 200 K. The freeze-out in this case is very low, which can be explained by the formation of an acceptor band instead of individual acceptor levels inhibiting the freeze-out phenomenon [52]. At higher temperatures, a decrease of the capacitance is observed for $V > 4$ V, which is related to the decrease of the fixed ionized charge density in the depletion region.

Then, in the *I–V* characteristic (figure 5(c)), an increasing current with temperature is in agreement with the temperature dependence of p^+n diode behavior [51]. First at low forward voltage between 0 and 3 V, the increase in current is related to enhanced generation-recombination current due to the increase of the intrinsic carrier density with the temperature.

Besides, a shift of the zero point of the *I–V* curve can be explained by the apparition of the non-ideal defect-assisted generation-recombination component in forward voltages and at high temperature values which is thermally activated and negligible around room temperature. At high forward voltage, above 3 V, we observed an increase of the diffusion current as carriers have more energy to pass the p^+n barrier.

4. DLTFS characterization

4.1. Effect of reverse bias and pulse voltage

In order to assess defects, and extract their parameters in terms of activation energy and capture cross-section, the DLTFS measurements were carried out in the temperature range 100 K–400 K. Pulse time $t_{\mathrm{P}} = 100$ ms and time window $tw = 600$ ms were chosen to have a strong DLTFS signal strength. Figure 6 shows the DLTFS spectra for different reverse bias U_{R} from −5 to −3 V at a fixed $U_{\mathrm{P}} = -0.5$ V (figure 6(a)) and for different pulse voltages U_{P} from −1.5 to 0.5 V at a fixed $U_{\mathrm{R}} = -5$ V (figure 6(b)). The DLTFS spectra show two positive peaks (T_1 and T_2) around 130 K and at 330 K, respectively.

When increasing U_{R} from −3 to −5 V, no temperature shift and an increase of magnitude of the first peak T_1 were observed indicating T_1 is related to bulk traps [53, 54]. For the second peak T_2, an increase its magnitude and a shift towards higher temperatures implies that it could be related to a field-dependent emission rate [53, 54]. This dependence can be explained by Poole–Frenkel effect, phonon assisted emission or band-like defects.

Now when increasing U_{P} from −1.5 to 0.5 V, we found an increase of T_1 magnitude up to −0.5 V followed by the drop for positive value of the pulse voltage. So, carrier injection is lowering the peak magnitude. This effect can be explained by the overlapping of two states (electron and hole traps) as previously reported [55]. Also, no temperature shift was noted indicating again the T_1 peak is related to bulk or extended defects. Concerning T_2 peak, we observed a large increase of the magnitude when the pulse voltage becomes positive with a

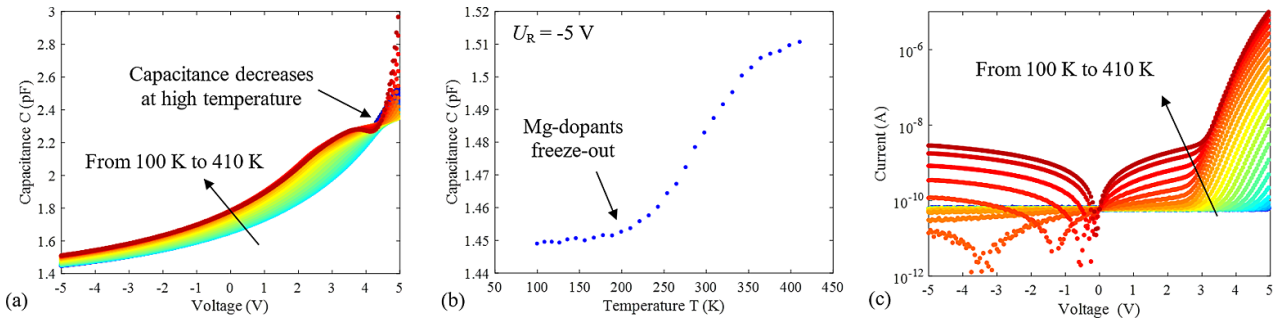

Figure 5. (a) *C*–*V*, (b) *C*–*T* and (c) *I*–*V* characteristics of the GaN p^+n diode for a temperature range from 100 K to 410 K.

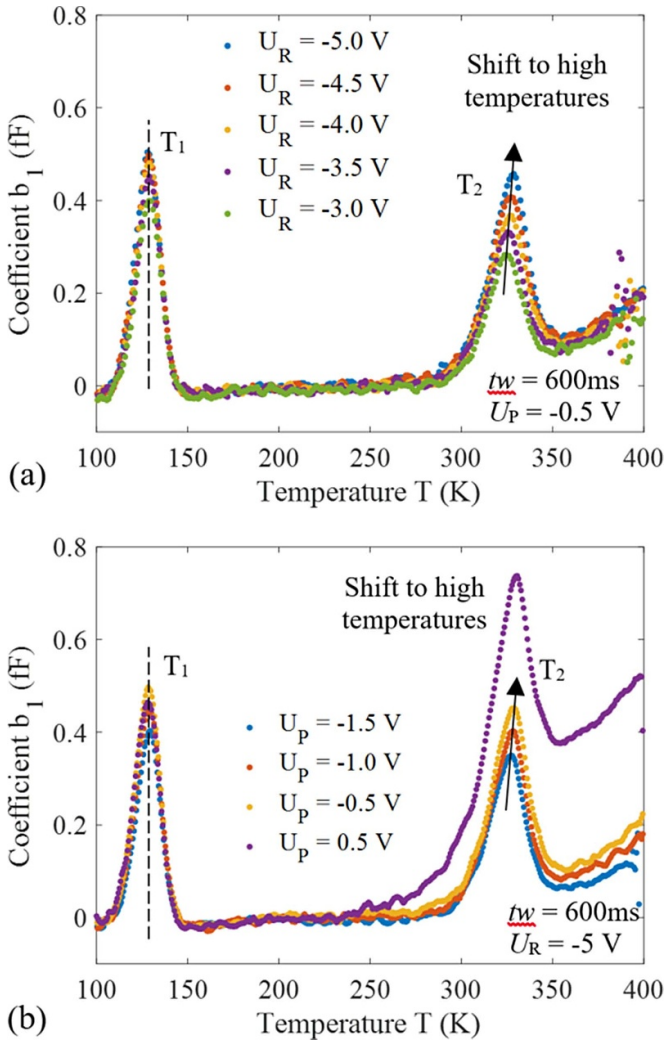

Figure 6. (a) DLTFS spectra for different reverse bias at $U_P = -0.5$ V and (b) for different pulse voltages at $U_R = -5$ V. Two peaks can be observed at 130 K and 330 K.

shift towards higher temperatures. This shift cannot be related to the Poole–Frenkel effect as the emission electric field did not change. One explanation could be that T_2 is related to several defects with different energy levels such as band-like defects.

4.2. Discussion on defect states

In DLTFS spectra, the maximum of the peaks occurs when the emission time dependence on the time window satisfies $\tau_{max} = \frac{t_1 - t_2}{\ln(t_1/t_2)}$ (figure 2(e)). The term τ_{max} is numerically extracted for each temperature knowing the time window in order to represent the Arrhenius plot, $(\ln(\tau \cdot T^2) - 1000/T)$. Then, the capture cross-section σ is calculated from the intercept of the linear fitting curve with the *y*-axis and the activation energy $E_C - E_T$ or $E_T - E_V$ from the slope. Figures 7(a) and (7) show the Arrhenius plot for both defect states at 130 K and 330 K, respectively, extracted for different values of U_R and for $U_P = -0.5$ V.

For the first defect state T_1, an activation energy of about 0.23 ± 0.01 eV and a capture cross-section of about 10^{-16} cm^2 were extracted. This defect is commonly observed in MOCVD-grown GaN and is assigned to V_N-related defects or to V_N–V_{Ga} complexes in *n*-GaN [29, 31, 32, 56]. Recently it was reported that Mg diffuses into the *n*-type GaN through the dislocations [57]. Because of diffusion of the Mg along the dislocations, the Mg doping level can be reduced to 10^{16} cm^{-3} [58]. Moreover, for this doping level of 10^{16} cm^{-3}, Mg dopants have an activation energy of about 0.25 eV [59], close to the one extracted from T_1 peak. The T_1 peak could be related to donor-type V_N-related defects and to acceptor-type diffused Mg dopants. So, the drop of the DLTFS signal can be explained by these defect states (donor and acceptor) in the *n*-GaN. It could also explain the graded and non-linear p^+n junction as identified from the $1/C^k$ (V) curves. Nevertheless, donor carbon-related defects C_N at E_V +0.25 eV as reported by Tokuda *et al* [34, 55] in *p*-GaN cannot be ruled out.

For the second defect state T_2, activation energies of about 0.89 ± 0.03 eV and 0.86 ± 0.03 eV above the valence band and a capture cross-section of about 10^{-13} cm^2 were extracted for $U_P = -1.5$ V and $U_P = -0.5$ V, respectively. This is alike to the deep acceptor level at the same energy level, at E_V +0.88 eV which has been reported and previously assigned to C_N in *n*-GaN [34, 35, 55]. The temperature shift suggests that the C_N deep acceptor state has a band-like behavior. As U_P is increased to a positive value of 0.5 V, the energy and capture cross-section lowered down to 0.70 ± 0.02 eV and 10^{-15} cm^2, respectively. So, a second component is observed and was attributed to a native point defect in GaN [56, 60]. The large increase of the amplitude indicates that both components

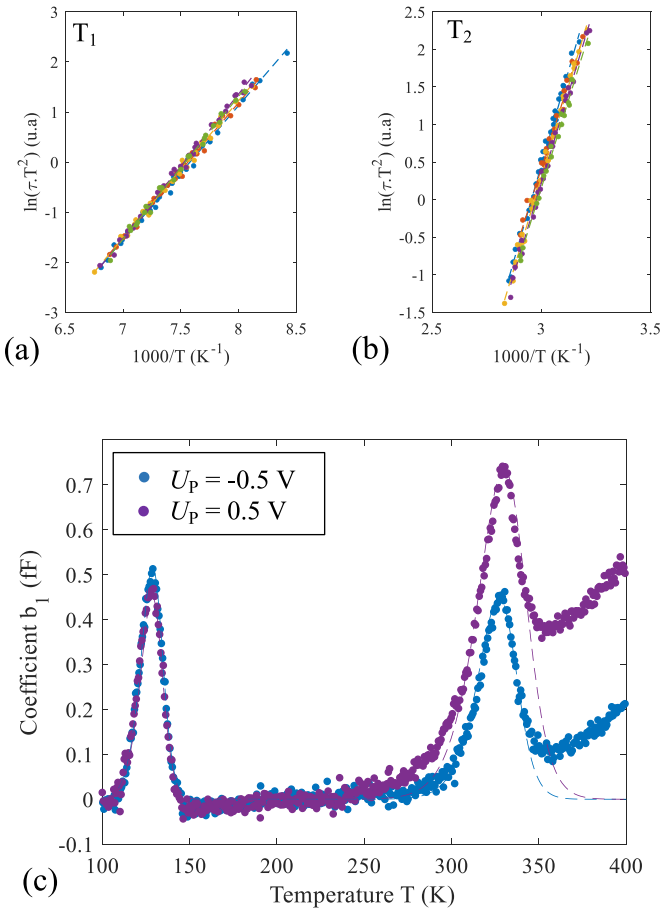

Figure 7. Arrhenius plots of the defect state (a) at 130 K and (b) at 330 K extracted for different values of U_R and for $U_P = -0.5$ V. (c) DLTFS spectra at $U_R = -5$ V for $U_P = -0.5$ V (in blue) and $U_P = 0.5$ V (in violet) and their fit using the extracted parameters.

come from the same type of defect (acceptor state). Figure 7(c) shows the DLTFS spectra at $U_R = -5$ V for $U_P = -1.5$ V (in blue) and $U_P = 0.5$ V (in violet). The fits of the experimental curves was performed using the PhysTech GmbH software with the extracted parameters. A strong agreement between the experimental curves and the corresponding fits (dashed line) is observed.

5. Conclusion

The defect state properties of Mg-doped GaN-on-Si p^+n diodes have been studied by mean of DLTFS. The effect of the reverse bias and pulse voltage showed different defect states at low and high temperature. At low temperature, two defect states with the same energy of about 0.25 eV, one above the valence band and the other below the conduction band, were observed. These defect states were attributed to V_N-related defects and to Mg-dopants diffusion in the *n*-GaN. At high temperature, two defects states were observed at energies of about 0.88 and 0.70 eV above the valence band. The first was attributed to deep acceptor C_N-related defects with a band-like behavior, while the second was assigned to native point defects.

Acknowledgments

This work was supported by Normandy region through the RIN RECHERCHE PLACENANO with contract number 18E01664/18P02478.

ORCID iDs

Y Lechaux https://orcid.org/0000-0002-9799-0842
A Minj https://orcid.org/0000-0003-0878-3276
L Méchin https://orcid.org/0000-0002-6350-1801
M Zhao https://orcid.org/0000-0002-0856-851X
E Simoen https://orcid.org/0000-0002-5218-4046

References

[1] Akasaki I, Amano H, Koide N, Kotaki M and Manabe K 1993 Conductivity controlof GaN and fabrication of UV/blue GaN light emitting devices *Physica* B **185** 428–32
[2] Green B M, Chu K K, Chumbes E M, Smart J A, Shealy J R and Eastman L F 2000 Effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's *IEEE Electron Device Lett.* **21** 268–70
[3] Weimann N G, Manfra M J, Hsu J W P, Pfeiffer L N, West K W, Lang D V and Molnar R J 2002 AlGaN/GaN HEMTs grown by MBE on semi-insulating HVPE GaN templates *60th DRC. Conf. Digest Device Research Conf.* vol 17 (IEEE) p 33
[4] Weimann N G, Manfra M J, Hsu J W P, Baldwin K, Pfeiffer L N, West K W, Chu S N G, Lang D V and Molnar R J 2003 AlGaN/GaN HEMTs grown by molecular beam epitaxy on sapphire, 6H-SiC, and HVPE-GaN templates *Inst. Phys. Conf. Ser.* **174** 223–6
[5] Maruska H P and Tietjen J J 1969 The preparation and properties of vapor-deposited single-crystal-line GaN *Appl. Phys. Lett.* **15** 327–9
[6] Mastro M A, Tsvetkov D, Soukhoveev V, Usikov A, Dmitriev V, Luo B, Ren F, Baik K H and Pearton S J 2004 RF performance of HVPE-grown AlGaN/GaN HEMTs *Solid. State Electron.* **48** 179–82
[7] Sheppard S T, Doverspike K, Pribble W L, Allen S T, Palmour J W, Kehias L T and Jenkins T J 1999 High-power microwave GaN/AlGaN HEMT's on semi-insulating silicon carbide substrates *IEEE Electron Device Lett.* **20** 161–3
[8] Gaska R, Chen Q, Yang J, Osinsky A, Asif Khan M and Shur M S 1997 High-temperature performance of AlGaN/GaN HFET's on SiC substrates *IEEE Electron Device Lett.* **18** 492–4
[9] Kumar V and Adesida I 2002 AlGaN/GaN HEMTs on sapphire *Proc. Fourth IEEE Int. Caracas Conf. on Devices, Circuits and Systems (Cat. No.02TH8611)* (IEEE) pp D048-1–6
[10] Endoh A, Yamashita Y, Ikeda K, Higashiwaki M, Hikosaka K, Matsui T, Hiyamizu S and Mimura T 2003 Fabrication of sub-50-nm-gate i-AlGaN/GaN HEMTs on sapphire *Phys. Status Solidi* C **2371** 2368–71
[11] Boutros K S, Burnham S, Wong D, Shinohara K, Hughes B, Zehnder D and McGuire C 2009 Normally-off 5A/1100V GaN-on-silicon device for high voltage applications *Tech. Dig. Int. Electron Devices Meet. IEDM* vol 29 pp 161–3
[12] Ishida M, Ueda T, Tanaka T and Ueda D 2013 GaN on Si technologies for power dwitching fevices *IEEE Trans. Electron Devices* **60** 3053–9
[13] Bisi D, Meneghini M, De Santi C, Chini A, Dammann M, Bruckner P, Mikulla M, Meneghesso G and Zanoni E 2013

Deep-level characterization in GaN HEMTs—part I: advantages and limitations of drain current transient measurements *IEEE Trans. Electron Devices* **60** 3166–75
[14] Dadgar A *et al* 2007 MOVPE growth of GaN on Si–substrates and strain *Thin Solid Films* **515** 4356–61
[15] Ishikawa H, Yamamoto K, Egawa T, Soga T, Jimbo T and Umeno M 1998 Thermal stability of GaN on (1 1 1) Si substrate *J. Cryst. Growth* **189–190** 178–82
[16] Pearton S J 2000 *GaN and Related Materials II* (Boca Raton, FL: CRC Press)
[17] Del Alamo J A and Joh J 2009 GaN HEMT reliability *Microelectron. Reliab.* **49** 1200–6
[18] Meneghesso G, Meneghini M, Tazzoli A, Ronchi N, Stocco A, Chini A and Zanoni E 2010 Reliability issues of gallium nitride high electron mobility transistors *Int. J. Microw. Wirel. Technol.* **2** 39–50
[19] Karboyan S, Tartarin J G, Labat N and Lambert B 2013 Gate and drain low frequency noise of ALGAN/GAN HEMTs featuring high and low gate leakage currents *2013 22nd Int. Conf. Noise Fluctuations, ICNF 2013* pp 2–5
[20] Tartarin J G, Astre G, Karboyan S, Noutsa T and Lambert B 2013 Generation-recombination traps in AlGaN/GaN HEMT analyzed by time-domain and frequency-domain measurements: impact of HTRB stress on short term and long term memory effects *2013 IEEE Int. Wirel. Symp. IWS 2013* pp 2–5
[21] Tartarin J G, Karboyan S, Carisetti D and Lambert B 2013 Gate defects in AlGaN/GaN HEMTs revealed by low frequency noise measurements *2013 22nd Int. Conf. Noise Fluctuations, ICNF 2013* pp 0–3
[22] Sghaier N, Trabelsi M, Yacoubi N, Bluet J M, Souifi A, Guillot G, Gaquière C and DeJaeger J C 2006 Traps centers and deep defects contribution in current instabilities for AlGaN/GaN HEMT's on silicon and sapphire substrates *Microelectron. J.* **37** 363–70
[23] Divay A, Masmoudi M, Latry O, Duperrier C and Temcamani F 2015 An athermal measurement technique for long time constants traps characterization in GaN HEMT transistors *Microelectron. Reliab.* **55** 1703–7
[24] Divay A, Duperrier C, Temcamani F and Latry O 2016 Effects of drain quiescent voltage on the ageing of AlGaN/GaN HEMT devices in pulsed RF mode *Microelectron. Reliab.* **64** 585–8
[25] Mizutani T, Okino T, Kawada K, Ohno Y, Kishimoto S and Maezawa K 2003 Drain current DLTS of AlGaN/GaN HEMTs *Phys. Status Solidi* A **200** 195–8
[26] Stuchlikova L, Kosa A, Szobolovszký R, Petrus M, Harmatha L, Delage S L and Kovac J 2017 Investigation of AlGaN/GaN Schottky structures by deep level Fourier transient spectroscopy with optical excitation *ASDAM 2016—Conf. Proc., 11th Int. Conf. Adv. Semicond. Devices Microsystems* pp 145–8
[27] Götz W, Johnson N M, Amano H and Akasaki I 1994 Deep level defects in *n*-type GaN *Appl. Phys. Lett.* **65** 463–5
[28] Hacke P, Detchprohm T, Hiramatsu K, Sawaki N, Tadatomo K and Miyake K 1994 Analysis of deep levels in n-type GaN by transient capacitance methods *J. Appl. Phys.* **76** 304–9
[29] Fang Z Q, Look D C, Wang X L, Han J, Khan F A and Adesida I 2003 Plasma-etching-enhanced deep centers in n-GaN grown by metalorganic chemical-vapor deposition *Appl. Phys. Lett.* **82** 1562–4
[30] Umana-Membreno G A, Parish G, Fichtenbaum N, Keller S, Mishra U K and Nener B D 2008 Electrically active defects in GaN layers grown with and without Fe-doped buffers by metal-organic chemical vapor deposition *J. Electron. Mater.* **37** 569–72
[31] Tokuda Y, Matuoka Y, Yoshida K, Ueda H, Ishiguro O, Soejima N and Kachi T 2007 Evaluation of dislocation-related defects in GaN using deep-level transient spectroscopy *Phys. Status Solidi* C **4** 2568–71
[32] Honda U, Yamada Y, Tokuda Y and Shiojima K 2012 Deep levels in n-GaN doped with carbon studied by deep level and minority carrier transient spectroscopies *Japan. J. Appl. Phys.* **51** 2–6
[33] Akasaki I and Amano H 2006 Breakthroughs in improving crystal quality of GaN and invention of the p–n junction blue-light-emitting diode *Japan. J. Appl. Phys.* **45** 9001–10
[34] Narita T, Tomita K, Tokuda Y, Kogiso T, Horita M and Kachi T 2018 The origin of carbon-related carrier compensation in p-type GaN layers grown by MOVPE *J. Appl. Phys.* **124** 3–9
[35] Kogiso T, Narita T, Yoshida H, Tokuda Y, Tomita K and Kachi T 2019 Characterization of hole traps in MOVPE-grown p-type GaN layers using low-frequency capacitance deep-level transient spectroscopy *Japan. J. Appl. Phys.* **58** SCCB36
[36] Takashima S, Ueno K, Matsuyama H, Inamoto T, Edo M, Takahashi T, Shimizu M and Nakagawa K 2017 Control of the inversion-channel MOS properties by Mg doping in homoepitaxial p-GaN layers *Appl. Phys. Express* **10** 121004
[37] Gupta C, Enatsu Y, Gupta G, Keller S and Mishra U K 2016 High breakdown voltage p-n diodes on GaN on sapphire by MOCVD *Phys. Status Solidi* A **213** 878–82
[38] Fu H, Fu K, Huang X, Chen H, Baranowski I, Yang T H, Montes J and Zhao Y 2018 High performance vertical GaN-on-GaN p-n power diodes with hydrogen-plasma-based edge termination *IEEE Electron Device Lett.* **39** 1018–21
[39] Hatakeyama Y, Nomoto K, Terano A, Kaneda N, Tsuchiya T, Mishima T and Nakamura T 2013 High-breakdown-voltage and low-specific-on-resistance GaN p–n junction diodes on free-standing GaN substrates fabricated through low-damage field-plate process *Japan. J. Appl. Phys.* **52** 028007
[40] Nomoto K, Hatakeyama Y, Katayose H, Kaneda N, Mishima T and Nakamura T 2011 Over 1.0 kV GaN *p–n* junction diodes on free-standing GaN substrates *Phys. Status Solidi* A **208** 1535–7
[41] Xiao M, Gao X, Palacios T and Zhang Y 2019 Leakage and breakdown mechanisms of GaN vertical power FinFETs *Appl. Phys. Lett.* **114** 163503
[42] Zhang Y, Piedra D, Sun M, Hennig J, Dadgar A, Yu L and Palacios T 2017 High-performance 500 V quasi- and fully-vertical GaN-on-Si pn diodes *IEEE Electron Device Lett.* **38** 248–51
[43] Zhang Y, Sun M, Piedra D, Azize M, Zhang X, Fujishima T and Palacios T 2014 GaN-on-Si vertical Schottky and p-n diodes *IEEE Electron Device Lett.* **35** 618–20
[44] Zhang Y *et al* 2015 Origin and control of OFF-state leakage current in GaN-on-Si vertical diodes *IEEE Trans. Electron Devices* **62** 2155–61
[45] Mase S, Hamada T, Freedsman J J and Egawa T 2017 Effect of drift layer on the breakdown voltage of fully-vertical GaN-on-Si p-n diodes *IEEE Electron Device Lett.* **38** 1720–3
[46] Simoen E, Clauws P and Vennik J 1985 The determination of deep level concentrations in high resistivity semiconductors by DLTS, with special reference to germanium *J. Phys. D: Appl. Phys.* **18** 2041–58
[47] Weiss S and Kassing R 1988 Deep level transient Fourier spectroscopy (DLTFS)—a technique for the analysis of deep level properties *Solid State Electron.* **31** 1733–42
[48] Lang D V 1974 Deep-level transient spectroscopy: a new method to characterize traps in semiconductors *J. Phys. D: Appl. Phys.* **45** 3023–32

[49] Lang D V 1974 Fast capacitance transient appartus: application to ZnO and O centers in GaP p-n junctions *J. Phys. D: Appl. Phys.* **45** 3014–22
[50] Wang C A, Fu S, Liu L, Li J and Bao J 2018 Temperature-dependent power-law analysis of capacitance-voltage for GaN-based pn junction *J. Appl. Phys.* **123** 3–8
[51] Sze S M and Ng K K 2006 *Physics of Semiconductor Devices* vol 10 (Hoboken, NJ: Wiley)
[52] Gunning B, Lowder J, Moseley M and Alan Doolittle W 2012 Negligible carrier freeze-out facilitated by impurity band conduction in highly p-type GaN *Appl. Phys. Lett.* **101** 082106
[53] Coelho A V P, Adam M C and Boudinov H 2011 Distinguishing bulk traps and interface states in deep-level transient spectroscopy *J. Phys. D: Appl. Phys.* **44** 305303
[54] Yamasaki K, Yoshida M and Sugano T 1979 Deep level transient spectroscopy of bulk traps and interface states in Si MOS diodes *Japan. J. Appl. Phys.* **18** 113–22
[55] Tokuda Y 2016 (Invited) DLTS studies of defects in n-GaN *ECS Trans.* **75** 39–49
[56] Płaczek-popko E, Trzmiel J, Zielony E, Grzanka S, Czernecki R and Suski T 2009 Deep level transient spectroscopy signatures of majority traps in >GaN p-n diodes grown by metal-organic vapor-phase epitaxy technique on GaN substrates *Physica* B **404** 4889–91
[57] Usami S, Mayama N, Toda K, Tanaka A, Deki M, Nitta S, Honda Y and Amano H 2019 Direct evidence of Mg diffusion through threading mixed dislocations in GaN p-n diodes and its effect on reverse leakage current *Appl. Phys. Lett.* **114** 232105
[58] Yi W *et al* 2020 Mg diffusion and activation along threading dislocations in GaN *Appl. Phys. Lett.* **116** 242103
[59] Brochen S, Brault J, Chenot S, Dussaigne A, Leroux M and Damilano B 2013 Dependence of the Mg-related acceptor ionization energy with the acceptor concentration in p-type GaN layers grown by molecular beam epitaxy *Appl. Phys. Lett.* **103** 1–5
[60] Ghazi H E L, Jorio A, Zorkani I and Ouazzani-Jamil M 2008 Optical characterization of InGaN/AlGaN/GaN diode grown on silicon carbide *Opt. Commun.* **281** 3314–9