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Current–voltage characteristics of AlCdO Schottky contact on the polished and unpolished p-type Si surfaces with and without light illumination

Chia-Lung Tsai [a], Cheng-Lung Tsai [a], Guan-Ru He [b], Ting-Hong Su [b], Chang-Feng You [a], Yow-Jon Lin [a,*]

[a] Institute of Photonics, National Changhua University of Education, Changhua 500, Taiwan
[b] Department of Physics, National Changhua University of Education, Changhua 500, Taiwan

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A B S T R A C T

In this study, the current–voltage characteristics of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si Schottky diodes with and without light illumination were examined. It is found that the Schottky barrier height (the series resistance) of the AlCdO/unpolished p-type Si Schottky diode is higher (lower) than that of the AlCdO/polished p-type Si Schottky diode. The power conversion efficiency of the AlCdO/p-type Si devices in the light (AM 1.5 G, 100 mW/cm^2) was improved by increasing built-in potential at the AlCdO/p-type Si interfaces and reducing the device series resistance and surface reflectivity. It is shown that the device surface roughness plays an essential role in improving the device performance.

1. Introduction

The key to resolving these problems (such as the greenhouse effect and acid rain) lies in the development of clean energies. Solar cells, which convert sunlight directly into electricity through the photovoltaic (PV) effect of semiconductors, are a key technology toward the conquest of global environmental problems [1]. Metal–semiconductor (MS) solar cells have received considerable attention in the past for their simple fabrication procedure and low cost of production compared to standard p–n junction solar cells. Among various kind of thin film solar cells, Si solar cells are thought to be the most hopeful, because Si is a safety element, and the amount of resources is huge [2–5]. In addition, to improve the properties of transparent conductive oxide (TCO), which is commonly used as a front contact in thin film silicon PV modules, is believed to be one of the most effective approaches to increase conversion efficiency and decrease production cost. Sputter of AlCdO films is a promising way to provide excellent TCO films. Instead of the widely used indium tin oxide (ITO), AlCdO is applied as the front contact of Si modules in this study. The chemical instability and the high cost due to the scarcity of in have led researchers to seek an alternative candidate for ITO [6]. We presented a simple PV device utilizing an AlCdO/p-type Si Schottky diode. This study shows that the unpolished p-type Si can help the AlCdO/p-type Si Schottky diode to produce much more carrier under illumination, which increases the conversion efficiency. This simple and efficient method did not attract wider attention and its use to improve the efficiency of PV devices has not been examined. Most of the technological processes in silicon device manufacturing require the preparation of undamaged and smooth silicon surfaces for the subsequent deposition process. However, replacing the AlCdO/polished p-type Si structure with AlCdO/unpolished p-type Si structure was utilized to optimize the light trapping properties in solar cells in this study. Light trapping is of importance in silicon solar cell for achieving a higher photocurrent.

2. Experimental details

Four-inch Si (1 0 0) wafers of p-type purchased from Guv Team International Co., Ltd were used in the experiment. The p-type wafers were doped with phosphorus to about 2×10^{15} cm^{-3}. The Si thickness was about 525 μm. The p-type Si samples were cleaned in chemical cleaning solutions of acetone and methanol. Then, the p-type Si sample was chemically etched with a diluted HF solution for 1 min, rinsed with de-ionized (DI) water and blown dry with N_2. Au (AlCdO) is applied as the back (front) contact of Si modules in this study. An Au ohmic contact was deposited onto the Si surface by electron-beam evaporation and annealed at 400 °C in nitrogen ambient for 1 min to form a large area ohmic contact. AlCdO Schottky contacts were formed through sputter coater. AlCdO films were grown by an rf

* Corresponding author.
E-mail address: rzr2390@yahoo.com.tw (Y.-J. Lin).

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magnetron sputtering system using two magnetrons, a high-purity CdO target (rf power was fixed at 30 W), and an Al target (rf power was fixed at 60 W). Targets were used in conjunction with Ar as an ambient gas for sputtering. The flow of Ar was 90 sccm. The sputtering pressure was fixed at 5×10^{-3} Torr. The substrate temperature was fixed at 400 °C. The sputtering time was 30 min. The AlCdO thickness, as estimated from the field emission scanning electron microscope, was about 190 nm. An Au ohmic contact was deposited onto the polished p-type Si surface and AlCdO Schottky contacts were deposited onto the unpolished p-type Si surface, as referred to as AlCdO/unpolished p-type Si Schottky diodes [a schematic of this device structure is shown in Fig. 1a]. An Au ohmic contact was deposited onto the unpolished p-type Si surface and AlCdO Schottky contacts were deposited onto the polished p-type Si surface, as referred to as AlCdO/polished p-type Si Schottky diodes [a schematic of this device structure is shown in Fig. 1b]. For conductivity and transmittance (T_t) measurements, the AlCdO films were simultaneously deposited on the glass substrate. The sheet resistance of the AlCdO film, as estimated from the four-point probe measurements, was about 17 Ω/□. The AlCdO films have an average optical transparency >8% in the visible range from 400 to 800 nm (shown in Fig 2). T_t was recorded using an ultraviolet–visible spectrophotometer. The surface morphology of the p-type Si and AlCdO/p-type Si samples was analyzed by atomic force microscopy (AFM), respectively. The diodes were characterized by capacitance per unit area-voltage (C–V) and current density–voltage (J–V) measurements. The C–V and J–V curves were measured using a Keithley Model-4200 semiconductor characterization system. The cell performance was measured under 100 mW/cm^2 and illumination intensity from a 150 W solar simulator with an AM 1.5 G filer. To rectify the measurement divergence, the light intensity was calibrated using a reference silicon solar cell certificated by the National Renewable Energy Laboratory.

3. Results and discussions

Fig. 3 shows AFM images of unpolished and polished p-type Si surfaces, respectively. Fig. 4 shows AFM images of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si surfaces, respectively. The root-mean-square surface roughness (R_{rms}) probed by AFM in 5 μm × 5 μm scans (shown in Fig. 3) is 100.1 and 0.2 nm for the unpolished and polished p-type Si surfaces, respectively. The root-mean-square surface roughness (R_{rms}) probed by AFM in 5 μm × 5 μm scans (shown in Fig. 4) is 79.6 and 5.6 nm for the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si surfaces, respectively. The effect of the surface roughness on the PV characteristics of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices will be discussed later.

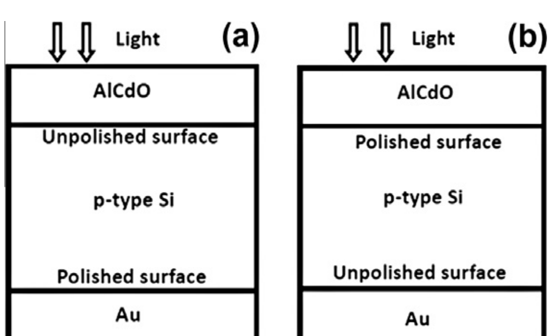

Fig. 1. Structures of the (a) AlCdO/unpolished p-type Si and (b) AlCdO/polished p-type Si devices.

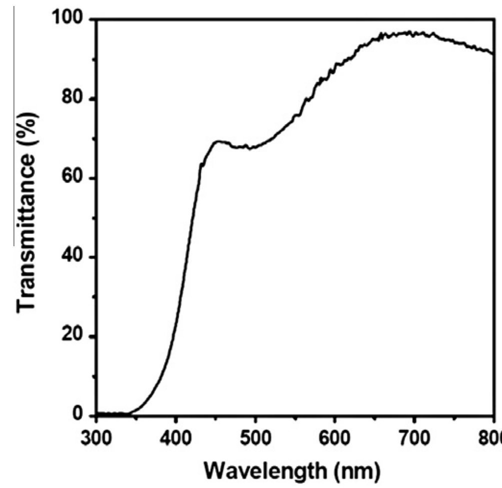

Fig. 2. Optical transmission spectrum of the AlCdO films.

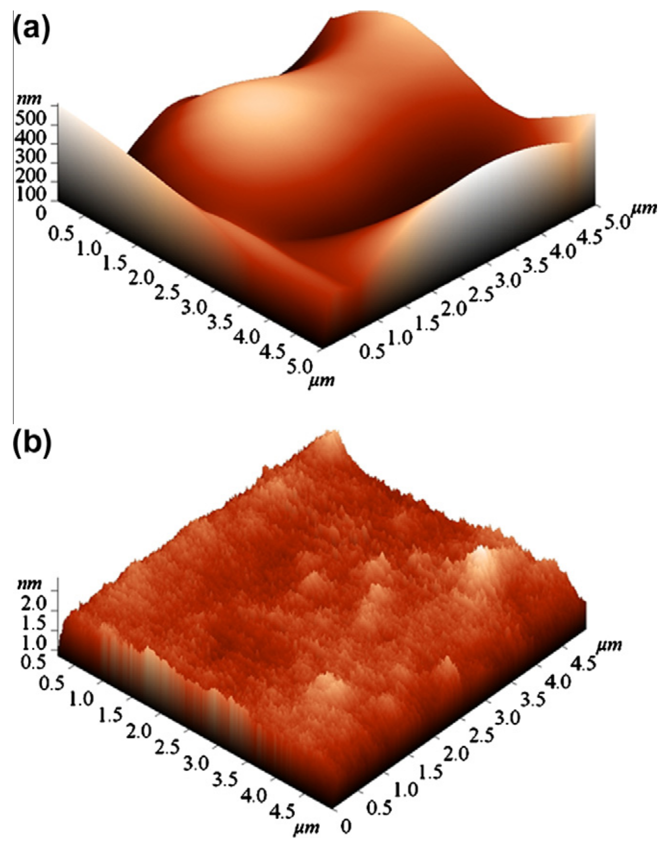

Fig. 3. AFM images of the (a) unpolished and (b) polished p-type Si surfaces.

Fig. 5 shows the J–V characteristics of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices in the dark. It can be seen that the device has a good rectifying behavior without light illumination. The rectifying J–V characteristics shown in Fig. 5 suggest that J at the positive voltage region of the AlCdO/unpolished p-type Si Schottky diode is higher than that of the AlCdO/polished p-type Si Schottky diode and the J–V curve in the negative voltage region of the AlCdO/unpolished p-type Si Schottky diode is similar to that of the AlCdO/polished p-type Si Schottky diode. This is because of the reduction in the series resistance (R_s). In practice, a high shunt (parallel) resistance and a low R_s are required simultaneously for an ideal photovoltaic device [7,8]. The R_s is attributed

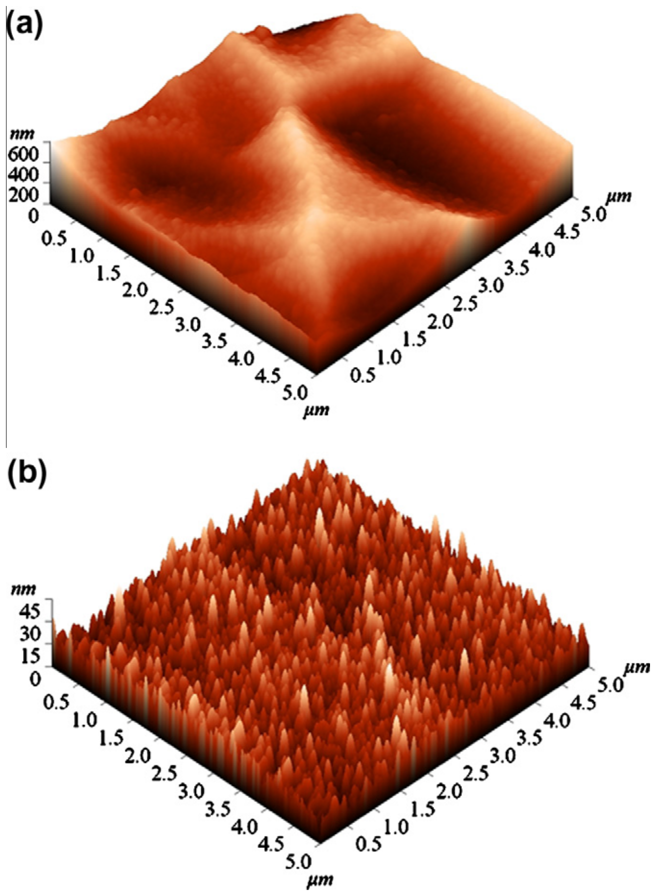

Fig. 4. AFM images of the (a) AlCdO/unpolished p-type Si and (b) AlCdO/polished p-type Si surfaces.

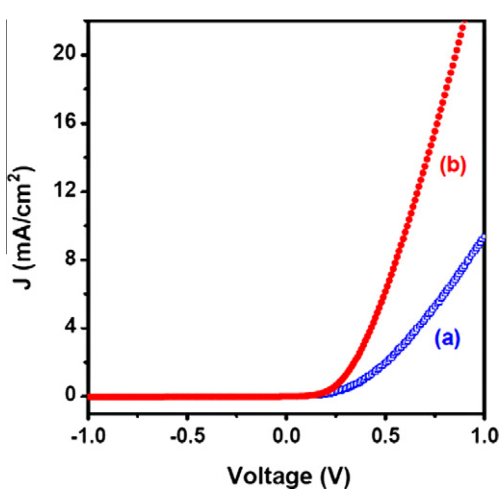

Fig. 5. *J–V* curves of the (a) AlCdO/polished p-type Si and (b) AlCdO/unpolished p-type Si devices in the dark.

to the ohmic loss in the whole device, including the resistance of the active layer and the electrodes. The shunt resistance usually reflects the degree of leakage current through the device, which relates to the overall quality of the films. Clearly, AlCdO contacts on the unpolished p-type Si surfaces do not affect the leakage current at the negative voltage. In addition, we find that the dominant conduction mechanism is the thermionic emission (TE). Based on the TE theory (qV > 3kT), the *J–V* relationship for Schottky diodes is given as follows [9,10]:

$$J = A^{*}T^{2}\exp\left(\frac{-q\phi_B}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \tag{1}$$

where $q\phi_B$ is the barrier height, q is the electron charge, k is the Boltzmann constant, T is the temperature, and A^* is the effective Richardson constant (32 cm^{-2} K^{-2} for p-type Si) [11]. The fitting curve of the *J–V* characteristics in the TE regime is shown in Fig. 6, suggesting that the process governing current flow is TE. By fitting a linear curve to the forward characteristics in Fig. 6, $q\phi_B$ and n can be calculated. $q\phi_B$ for the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices is 0.72 and 0.71 eV, respectively; while n for the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices is 1.5 and 2.0, respectively. These observations strongly support the existence of current conduction mechanisms other than the TE process, such as tunneling. Lin et al. [12] and Kim et al. [13] pointed out that the finding (the larger ideality factors) could be explained in terms of an increase in tunneling transport. Dökme et al. [11] found that this deviation in A^* may be due to the spatial inhomogeneous barrier heights and potential fluctuation at the interface that consist of low and high barrier areas. Thus, the tunneling current induced at the MS interface and this deviation in A^* may make the $q\phi_B$ uncertainty based on the TE theory.

To further confirm the $q\phi_B$ value of the AlCdO/unpolished p-type Si or AlCdO/polished p-type Si device, the *C–V* characteristics of these devices at 100 kHz were measured. Otterloo and Gerritsen [14] have shown that the *C–V* method is most accurate in determining the barrier height compared to *J–V* and photoemission methods. Among the *C–V* methods, the barrier height is most commonly calculated from the intercept voltage, determined by an extrapolation of the C^{-2} versus V curve to $C^{-2} = 0$. The barrier height so determined is $q\phi_C V$ for sufficient forward bias to cause flatband conditions in the semiconductor. The measured C^{-2} as a function of applied voltage V for the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices is shown in Fig. 7, respectively. The *C–V* relationship for a Schottky diode is given by [12,15]:

$$C^{-2} = (2/\varepsilon_s qN_A)(V_i - V) \tag{2}$$

where N_A is the carrier concentration, ε_o is the permittivity in vacuum ($\varepsilon_s = 11.7\varepsilon_o$ for Si) [16], and V_i is the x intercept at $C^{-2} = 0$. According to Eq. (2), from the slope of Fig. 7, N_A of

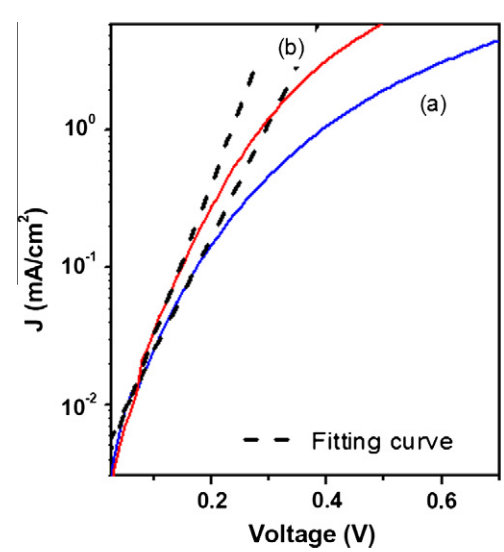

Fig. 6. *J–V* curve of the (a) AlCdO/polished p-type Si and (b) AlCdO/unpolished p-type Si devices under forward bias condition in the dark and the fitting curve to the *J–V* characteristic in the TE regime.

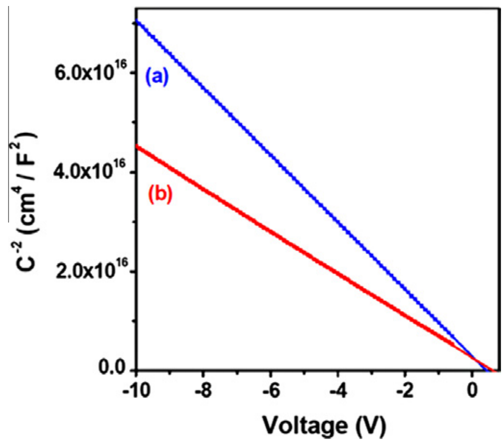

Fig. 7. C^{-2}–V curves of the (a) AlCdO/polished p-type Si and (b) AlCdO/unpolished p-type Si devices in the dark.

2.8×10^{15} (1.8×10^{15}) cm^{-3} for the AlCdO/unpolished p-type Si (AlCdO/polished p-type Si) Schottky diode was calculated. The Schottky barrier height $q\phi_C V$ is related to V_i by the relationship: $q\phi_C V = qV_i + kT + q\xi$. $q\xi$ is equal to (E_V–E_F) = kT [ln (N_A/N_V)]. E_V is the energy of the valence band edge, E_F is the energy of the Fermi level, and $N_V = 1.04 \times 10^{19} cm^{-3}$ is the effective density of states in the valence band of Si [16]. $q\phi_C V$ for the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices is 0.86 and 0.68 eV, respectively. We find that $q\phi_C V$ of the AlCdO/unpolished p-type Si Schottky diode is higher than that of the AlCdO/polished p-type Si Schottky diode. In addition, the discrepancy in the Schottky barrier height extracted from J–V and C–V measurements is attributed to the presence of the tunneling current [12,13], the A^* uncertainty resulted from spatial inhomogeneities [11] and the image-force lowering effect [17].

Fig. 8 shows the J–V characteristics of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices in the light (AM 1.5 G, 100 mW/cm^2). The important figures for the solar cell are the open circuit voltage (V_{oc}), the short circuit current density (J_{sc}) and the so called fill factor (F), which is a measure of how rectangular the J–V curve is. It is defined as

$$F = (J_m V_m)/(J_{sc} V_{oc}) \tag{3}$$

where V_m (J_m) is the voltage (current density) producing the maximum power density. The power conversion efficiency (η) is defined as the ratio between the extracted electrical power density at the maximum power density point and the power density delivered by the light source Pin:

$$\eta = (J_m V_m)/P_{in} = (FJ_{sc} V_{oc})/P_{in} \tag{4}$$

The V_{oc}, J_{sc} and F of the AlCdO/polished p-type Si device were 0.18 V, 1.3 mA/cm^2, and 22.0%, respectively, resulting in η of 0.05%. Furthermore, the AlCdO/unpolished p-type Si device exhibits a higher V_{oc} of 0.24 V, a higher J_{sc} of 6.9 mA/cm^2, a higher F of 23.7%, and a higher η of 0.39%. This increase in J_{sc} is due to an increased R_{rms} that induces the reduction in R_s and an improved light trapping [18]. The light trapping is usually achieved by scattering of the incident light at textured interfaces and subsequent internal reflection within the cell [19]. In addition, this increase in V_{oc} is due to an increased built-in potential (that is, V_i) [20]. Therefore, the increase in R_{rms} can greatly improve the PV characteristics of the AlCdO/p-type Si junction, which may be ascribed to that the increase in R_{rms} can help to produce much more carriers under illumination. On the other hand, the ITO contact was also deposition of p-type Si films for comparison. The ITO layers were deposited by electron-beam evaporation. The substrate temperature was fixed at 300 °C. Fig. 8c shows the J–V characteristics of the ITO/unpolished p-type Si device in the light (AM 1.5 G, 100 mW/cm^2). We find the higher η of the AlCdO/unpolished p-type Si device than that of the ITO/unpolished p-type Si device. In addition, η depends on the reflection and transmission coefficients of the material. Lowering surface reflectivity is one of the most important processes for improving η. The fraction of power in the incident wave that is reflected or transmitted is called the reflectance (R_r) and T_t. To conserve energy, at a given boundary, it must be true that the power incident on the boundary equals the sum of the power reflected at that boundary and the power transmitted through the boundary. That is,

$$1 = R_r + T_t \tag{5}$$

Therefore, η may be expressed as

$$\eta = \eta_{ext}\eta_{int} \tag{6}$$

where η_{ext} and η_{int}, respectively, are the external light injection and internal power conversion efficiency. Based on the result above, we find that η_{ext} depends on R_r (T_t) and η_{ext} increases with decreasing (increasing) R_r (T_t). R_r of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices is shown in Fig. 9, respectively. R_r was recorded using an ultraviolet–visible spectrophotometer. We find the

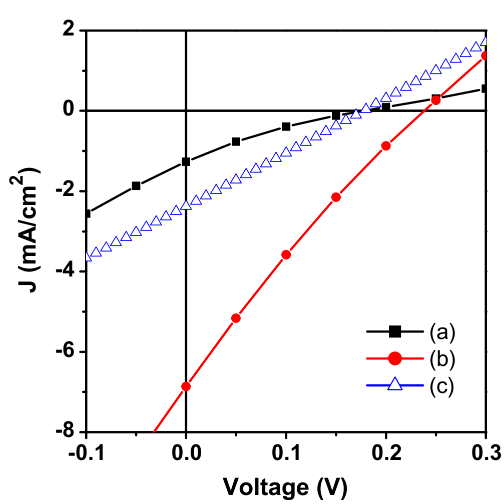

Fig. 8. J–V curves of the (a) AlCdO/polished p-type Si, (b) AlCdO/unpolished p-type Si and (c) ITO/unpolished p-type Si devices in the light (AM 1.5 G, 100 mW/cm^2).

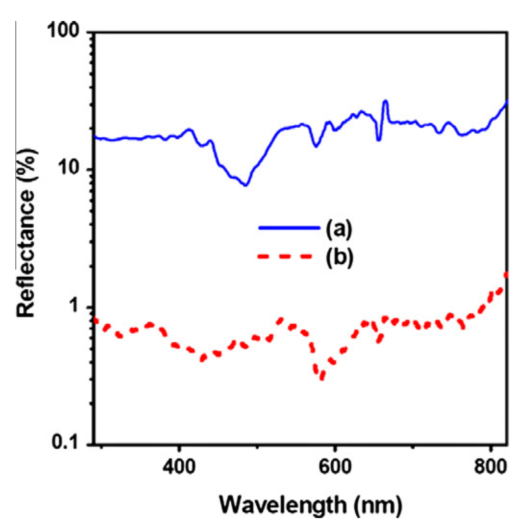

Fig. 9. R_r of the (a) AlCdO/polished p-type Si and (b) AlCdO/unpolished p-type Si devices as a function of wavelength.

lower R_r of the AlCdO/unpolished p-type Si device than those of the AlCdO/polished p-type Si device. The remarkably decreasing R_r of the device is attributed to the increase in R_{rms} and an improved light tapping [18]. The effect of the surface roughness of substrates on light scattering in solar cells has been investigated by computer modeling [21]. We suggest that the device surface roughness plays an essential role in increasing the energy conversion efficiency. Polished flat Si surfaces have a high natural reflectivity with a strong spectral dependence [3]. The minimization of reflection losses is very important for high efficiency solar cells.

4. Conclusions

This study examined the J–V characteristics of the AlCdO/unpolished p-type Si and AlCdO/polished p-type Si devices with and without light illumination. It is shown that the Schottky barrier height (the series resistance) of the AlCdO/unpolished p-type Si Schottky diode is higher (lower) than that of the AlCdO/polished p-type Si Schottky diode. As discussed above, the unpolished p-type Si can help the AlCdO/p-type Si device to produce much more carrier under illumination, which increases the conversion efficiency. It is found that interface constitutes an important part of the silicon solar cell. The enhanced conversion efficiency is ascribed to the increase in V_i and decreases in R_s and R_r. The remarkably decreasing R_r of the device may be due to a combined effect of the increased R_{rms} and an improved light trapping. We suggest that the device surface roughness plays an essential role in improving the device performance.

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