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Passivated Emitter and Rear Cell Silicon Solar Cells with a Front Polysilicon Passivating Contacted Selective Emitter

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p-Type silicon solar cells with a structure of passivated emitter and rear cell (PERC) are a mainstream product of the photovoltaic (PV) industry. Because of its low cost, PERC technology will continue to be dominant for a long time. One of the key features to improve PERC solar cell performance is the use of a selective emitter (SE), which is now mainly realized by laser doping (LD). However, SE by LD still cannot perfectly resolve recombination underneath the front metallized area. The use of a tunnel oxide passivated contact (TOPCon) can dramatically reduce recombination at the metallized area. With the help of an organic mask and etching by texturing solution, the TOPCon SE structure on PERC cells is realized. An average efficiency of 22.65% is reached on 6 in., commercial grade p-type Czochralski wafers. The average open-circuit voltage of PERC cells with TOPCon SE is 14.6 mV higher than LD SE. However, the short-circuit current is lowered by parasitic absorption of polysilicon of alignment margins, which makes cell efficiency of the two SE structures almost the same. With improved alignment precision, TOPCon SE will provide an increase in efficiency.

1. Introduction

Passivated emitter and rear cell (PERC) silicon solar cell had kept the efficiency record for over ten years[1] and started to be transferred from laboratory to industry at the beginning of 2010.[2–6] The main improvement of PERC is rear-side passivation compared with aluminum back surface field (Al-BSF) silicon solar cells. At the initial stage of industrialization of PERC cells, it has little cost advantage over Al-BSF cells because of high cost of new materials (mainly trimethylaluminum [TMA]). As more and more industrial gas vendors entered TMA market, the price went down quickly. TMA usage also went down due to process optimization. On the other hand, efficiency gap between PERC and Al-BSF cells became bigger due to higher efficiency potential of PERC cells. Nowadays, PERC cells have become the mainstream product in silicon photovoltaic (PV) industry.

Industrialization of Selective Emitter (SE) was earlier than rear surface passivation of silicon cells.[7–12] There are many methods to form the SE structure, which include patterned ion implantation,[10] laser doping (LD),[9] etch back,[8,11] silicon ink,[12] and others. LD using a phosphosilicate glass (PSG) layer as a doping precursor layer is the simplest and cheapest method, because it needs only one additional process and almost no additional materials.[9] The LD SE, therefore, has been commercialized in most PERC production lines. However, the efficiency gain by conventional SE (including LD SE) is limited by the front unpassivated surface under metal fingers.

In 2013, Feldmann et al. used a tunneling oxide and phosphorous-doped polysilicon layer at the rear side of N-type silicon solar cell and notated it as tunnel oxide passivated contact (TOPCon).[13] The TOPCon structure enabled high-quality passivation to metal–semiconductor interface. There had been some trials that using polysilicon at front side of solar cells to replace diffused junction.[14–16] Parasitic absorption of polysilicon layer induced degradation in blue response, resulting in low J_{sc}. Despite several previous research on patterning of polysilicon layer,[17,18] to the best of our knowledge, there was no report on complete solar cells with the front patterned polysilicon yet. In this work, solar cells with front patterned polysilicon were fabricated, where the front patterned polysilicon was realized by masking and etching processes. The cells were denoted as PERC with TOPCon SE, corresponding to PERC with LD SE in mass production. PERC with TOPCon SE yielded

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14.6 mV open-circuit voltage (V_{oc}) advantage over PERC with LD SE, which was fabricated as control group.

2. Experimental Section

The process sequence of PERC with TOPCon SE and LD SE is shown in **Figure 1**. Two groups of cells used $156.75 \times 156.75\ mm^2$ pseudo-square wafers with a thickness of 180 μm and a resistivity of 1 Ω cm as a substrate.

The first process of two groups of cells is alkaline texturing. Five chemical solutions were applied during the texturing process. First, wafers went through 6–8% potassium hydroxide (KOH) at 80 °C for 10 min to remove the damage layer. The second solution is $KOH + H_2O_2$ at room temperature to remove organic impurities. Then, wafers went through texturing solution (KOH + additives at 80 °C) for 7 min, and $KOH + H_2O_2$ solution again to remove additive residues. As the last step, hydrofluoric acid (HF) was applied to keep surface hydrophobic.

After texturing, tunneling oxide and 200 nm intrinsic polysilicon were deposited by a tube low-pressure chemical vapor deposition (LPCVD) tool. Tunneling oxide was grown at 580 °C for 10 min. The thickness is about 1.7 nm. The deposition temperature of intrinsic polysilicon is 600 °C with a deposition rate of ≈4 nm min. Phosphorous doping of intrinsic polysilicon was realized by a tube thermal furnace. The phosphorous diffusion process included 30 min of source deposition at 810 °C and 15 min of drive-in at 860 °C. After phosphorous diffusion, stearic acid was jetted onto the front surface on the pattern of fingers as mask. The etching process was similar with the texturing process, including five chemical solutions. First, 5% HF was applied to remove PSG of non-finger area. $KOH + H_2O_2$ was then applied to remove stearic acid mask, whereas PSG of finger area was kept as mask during polysilicon etching. We used texturing solution (KOH + additives at 80 °C for 7 min) for polysilicon etching, so that etched area still had low reflectivity. The following two solutions were the same as texturing, i.e., $KOH + H_2O_2$ and HF.

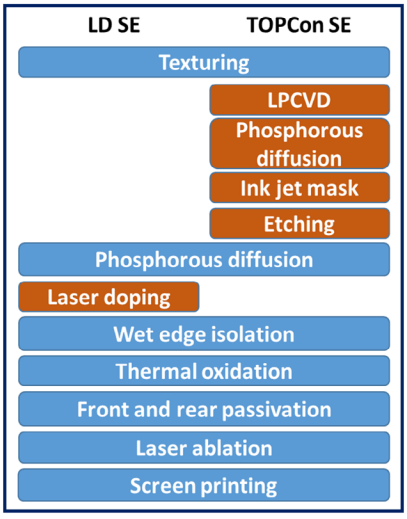

Figure 1. Process sequence of PERC with TOPCon SE and LD SE (control group).

The remaining processing steps of two group of cells were almost the same except TOPCon SE cells that had higher sheet resistance for noncontact area and omitted LD. A sheet resistance of noncontact area of TOPCon SE cells was $\approx 170\ \Omega\ sq^{-1}$. The diffusion process included 290 s of source deposition and 500 s of drive-in at 860 °C. A sheet resistance of noncontact area of LD SE cells was $\approx 135\ \Omega\ sq^{-1}$. The diffusion process included 310 s of source deposition at 780 °C, 600 s of drive-in at 860 °C, and 600 s of source deposition at 780 °C. The source deposition after drive-in was to provide enough doping source for LD. The reason to use lower sheet resistance of noncontact area for LD SE cells is that LD usually deepened junction and lower surface concentration at the same time.[19] A green laser (532 nm) with rectangular flat-top beam was used for LD. A spot size was $110 \times 110\ \mu m^2$. A pulse duration was 110 ns. A pulse frequency was set as 230 kHz, and a scanning speed was set as $26\ m\ s^{-1}$. The pulse energy density was set as $1.06\ J\ cm^{-2}$. A sheet resistance of laser-irradiated area was $95\ \Omega\ sq^{-1}$. The remaining processes of two groups of cells were standard PERC processes. An inline wet etching tool was used for edge isolation. The etching solution was $HF:HNO_3:H_20$ (1:3:1), and the etching duration is 42 s. A thin oxide layer was grown for mitigation of potential-induced degradation. An oxidation temperature was 600 °C, and a duration was 10 min. Double-side AlO_x was grown by time-separated tube atomic layer deposition (ALD) with 24 cycles.[20] The thickness was about 3.4 nm; 55 nm/40 nm of $SiON/SiN_x$ films and 80 nm of SiN_x film were deposited to front side and rear side by direct plasma-enhanced chemical vapor deposition (PECVD), respectively. A green laser was used to open a part of rear dielectric films. The opened width was about 35 μm. Ag and Al paste were screen printed to front and rear side, respectively, with nine bus-bar patterns.

3. Results and Discussion

3.1. TOPCon SE

Texturing solution was used to etch polysilicon of nonmetal area for low reflectivity in this work. **Figure 2**a shows the reflectivity post the first texture and second texture (polysilicon etching). The two reflectivity profiles are almost the same. Etched volume by the second texture is less than the first texture, because the surface for the second texture is already (111) oriental. Figure 2c is the image of cross section of a polysilicon finger taken by scanning electron microscopy (SEM). About 300 nm of film can be seen from the polysilicon finger area. It includes about 200 nm of polysilicon and 90–100 nm of $SiN_x/SiON$ stack.

Industrial LD pattern includes four cross-shaped marks for alignment between screen pattern and laser pattern. Scanning speed of laser to process marks is much slower than fingers, so that pyramids of mark area were smoothed. Smooth mark area ensured high contrast ratio to other areas for camera. During screen printing, camera can easily seize marks to calculate pattern offset. It is so-called alignment by marks. Due to high precision of alignment by marks, a width of laser-doped fingers can be as low as 120 μm. For TOPCon SE, we also processed marks by mask and etching. As both mark area and other area are textured, these marks can hardly be seized by camera due to low

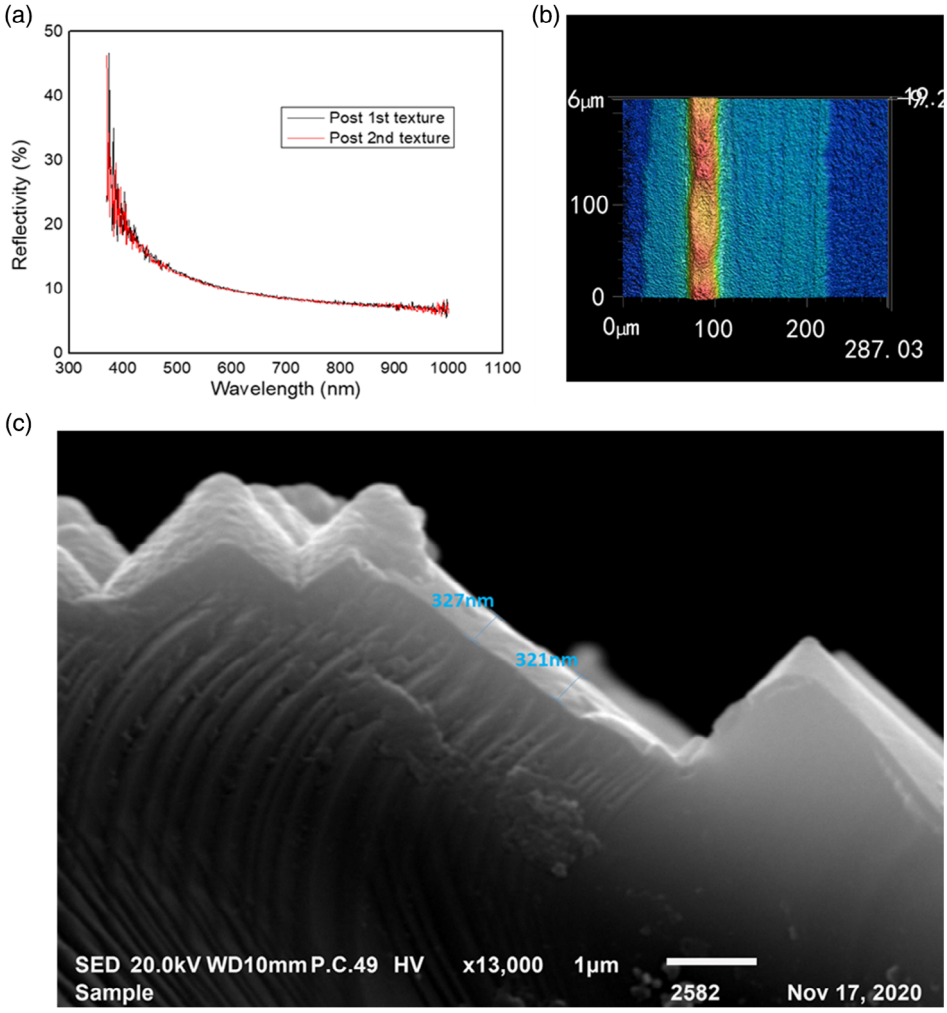

Figure 2. a) Reflectivity profiles post the first texture and the second texture (polysilicon etching). b) Image of polysilicon finger and screen-printed metal finger taken by 3D microscopy. c) Image of cross section of polysilicon finger taken by SEM.

contrast ratio. We, therefore, used another alignment method, so-called alignment by sides, which means camera of printer seizes sides of wafers to calculate pattern offset. Due to the low precision, polysilicon finger width was enlarged to about 200 μm. Figure 2b is the image of polysilicon finger and screen-printed metal finger taken by 3D microscopy. The width of polysilicon finger is about 200 μm, whereas the width of metal finger is about 35 μm.

3.2. Doping Profile

Figure 3 shows the doping profiles of light- and heavy-doped area of two groups of cells measured by electrochemical capacitance–voltage (ECV). For LD SE cells, sheet resistance and surface concentration of light-doped area are 135 Ω sq^{-1} and 5.9×10^{20} cm^{-3}, respectively. After LD, sheet resistance and surface concentration are reduced to 95 Ω sq^{-1} and 2.9×10^{20} cm^{-3}, respectively. For TOPCon SE cells, there is almost no interaction

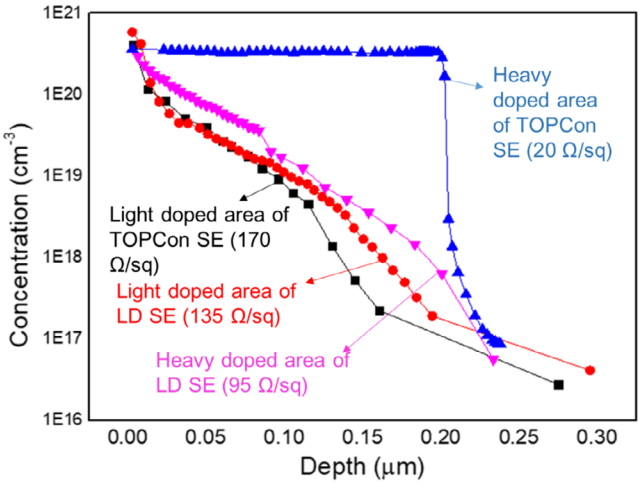

Figure 3. ECV doping profiles of light- and heavy-doped area of two groups of cells.

Table 1. Cell efficiency of LD SE and TOPCon SE cells.

Groups	Quantity	V_{oc} [V]	J_{sc} [mA cm^{-2}]	FF [%]	Eta [%]
LD SE	42	0.6822	40.78	81.44	22.66
TOPCon SE	40	0.6968	40.05	81.19	22.65

between doping profiles of light- and heavy-doped area. To balance passivation and lateral transport, we selected sheet resistance of light-doped area as 170 Ω sq^{-1}. The surface concentration is 4.1×10^{20} cm^{-3}. Heavy doping of polysilicon is helpful to both contact and passivation under metal area. We, therefore, increased both doping source (i.e., $POCl_3$) capacity and drive-in duration of the first diffusion process. The second diffusion process also drove some phosphorous atoms into polysilicon. The final sheet resistance is 20 Ω sq^{-1}, and the surface concentration is 3.6×10^{20} cm^{-3}.

3.3. Cell Efficiency

Table 1 shows the average efficiency of LD SE and TOPCon SE cells. **Figure 4** shows V_{oc} (open-circuit voltage), J_{sc} (short-circuit current density), fill factor (FF), and efficiency distribution of two groups of cells. Whereas TOPCon SE cells have similar efficiency with LD SE cells, V_{oc} of TOPCon SE is significantly improved, showing 14.6 mV higher than LD SE. However, J_{sc} is lower due to high parasitic absorption of wide polysilicon finger. **Figure 5** shows the external quantum efficiencies of LD SE and TOPCon SE cells. The blue response of TOPCon SE cells is worse than LD SE cells. FF of TOPCon SE is slightly lower than LD SE. The main reason should be the high sheet resistance of light-doped area.

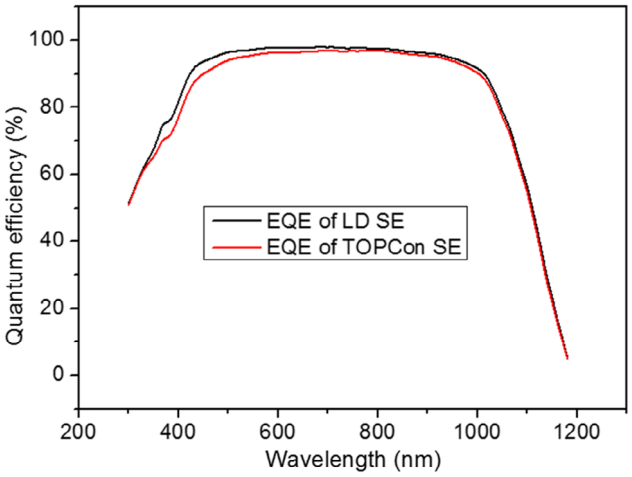

Figure 5. External quantum efficiency of LD SE and TOPCon SE cells.

Light-doped area of TOPCon SE cells should have higher collection efficiency and lower free carrier absorption (FCA) than LD SE because of the higher sheet resistance.[21] So, the actual

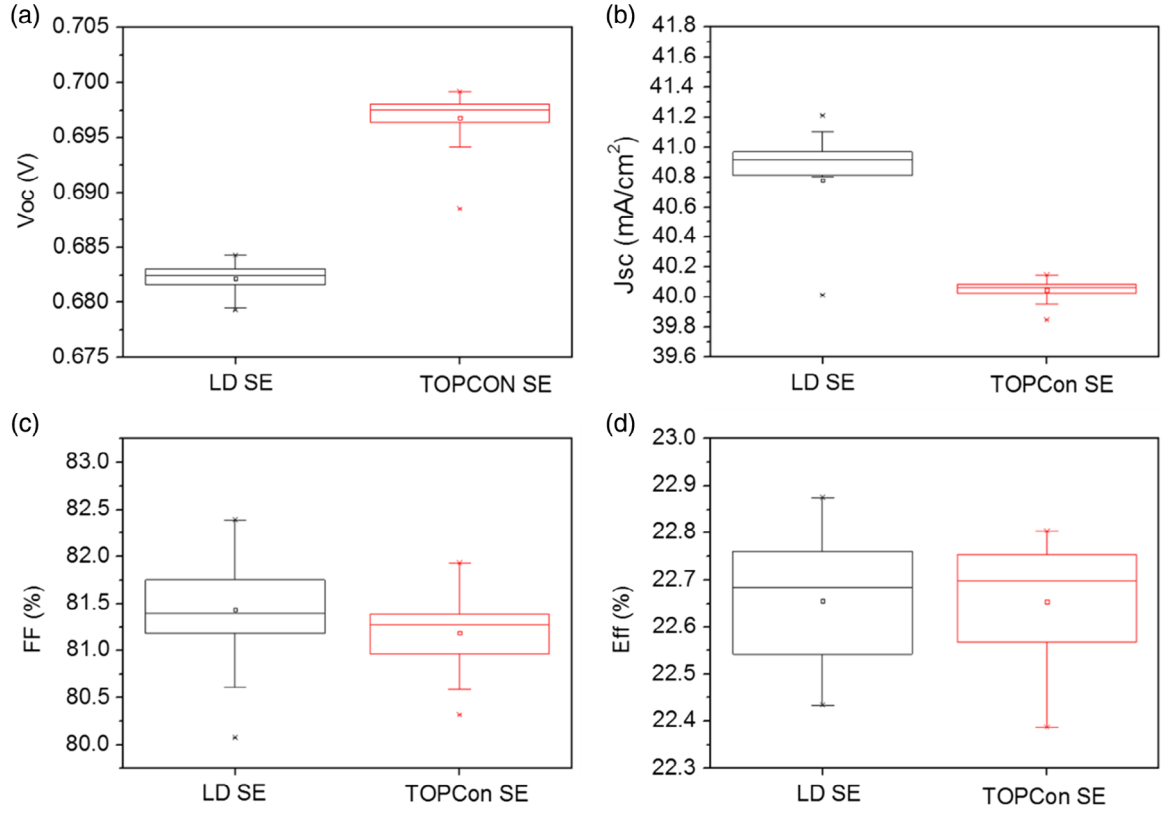

Figure 4. a–d) Box plots of: a) V_{oc}, b) J_{sc}, c) FF, and d) efficiency of LD SE and TOPCon SE cells.

J_{sc} loss due to parasitic absorption should be above 0.8 mA cm^{-2} instead of the J_{sc} gap of cells (0.73 mA cm^{-2}). If the two SE cells using the same width for alignment margin, J_{sc} loss of TOPCon SE cells can be reduced by half, which means about 0.23% of efficiency gain.

4. Conclusion

TOPCon SE PERC cells featuring localized TOPCon to passivate front metal area were fabricated in the same manner as on a conventional solar cell with four additional processes to replace LD: tunneling oxide and intrinsic polysilicon deposition, doping of polysilicon, mask, and etching by texturing solution. An average efficiency of 22.65% has been achieved, which is comparable with LD SE cells. An average V_{oc} of TOPCon SE cells was 14.6 mV higher than that of LD SE. However, parasitic absorption of polysilicon fingers resulted in lower J_{sc} and limited the efficiency. We estimate that an average efficiency can achieve 22.88% after improving alignment precision.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

passivated emitter and rear cells, selective emitter, tunnel oxide passivated contacts

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