Journal of Applied Physics ARTICLE pubs.aip.org/aip/jap

Analysis of interface trap induced ledge in β-Ga_2O_3 based MOS structures using UV-assisted capacitance–voltage measurements

Cite as: J. Appl. Phys. **135**, 195704 (2024); doi: 10.1063/5.0203022
Submitted: 8 February 2024 · Accepted: 2 May 2024 ·
Published Online: 17 May 2024

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ABSTRACT

A ledge feature in the capacitance–voltage (CV) profiles of Ga_2O_3 MOS (metal–oxide–semiconductor) capacitors is investigated using UV-assisted CV measurements. A model is presented whereby the capacitance ledge is associated with carrier trapping in deep-level states at the Al_2O_3/Ga_2O_3 interface. Following UV assisted emptying of interface traps at a constant bias, a voltage ramp toward flatband results in a CV ledge when the trap recombination current becomes equal to the quasi-static sweep charging current. The ledge continues until all the traps below the corresponding pinned surface potential have been filled. Varying the UV energy varies the ledge voltage range and allows a density of states to be determined as a function of energy. A broad interface state peak with maximum density $\sim 8 \times 10^{12}\,cm^{-2}\,eV^{-1}$ for deep trap energies lying between 2.4 and 4.1 eV below the conduction band (CB) edge is extracted. Using the conductance method, the interface trap density is also found to rise toward the CB edge in the range 0.25–0.45 eV below the CB edge, reaching a maximum density of $\sim 1 \times 10^{12}\,cm^{-2}\,eV^{-1}$. Combining these two techniques, an interface trap distribution is estimated for almost the entirety of the bandgap of Ga_2O_3. This novel technique probes deep interface states where standard methods fail to quantify interface states reliably.

I. INTRODUCTION

β-Ga_2O_3 with its ultra-wide bandgap (>4.7 eV), high breakdown field (8 MV/cm), and decent mobility (~200 cm^2/Vs) is gaining popularity for use in power semiconductor devices.[1] However, realization of efficient power devices through the exploitation of the high breakdown field of Ga_2O_3 has been challenging due to various issues, including leakage current induced by high field crowding,[2] low thermal conductivity,[3] inefficient hole conduction,[4] early dielectric breakdown,[5] and interface traps,[6] with the latter being one of the prominent causes of device instability and reduced performance. The interface of Ga_2O_3 with a range of dielectric materials and deposition conditions has been studied extensively.[7–10] Moreover, the interface traps are expected to show behaviors different from those in conventional semiconductors due to inefficient hole conduction in Ga_2O_3. Hence, a new perspective is needed to study the behavior of trap states at a Ga_2O_3–dielectric interface.

The occurrence of a "ledge" or "plateau" in CV measurement was first observed in a Si MOS structure at low temperature. Goetzberger and Irvin[11] explained the presence of the ledge by non-equilibrium conditions that arise due to a low generation rate of trapped charges during swept gate bias measurements. Sung and Lyon[12] observed a similar ledge under photo-illumination with UV light in Si MOS structures. In the past two decades, UV light has been commonly used as a tool to investigate dielectric interfaces in wide bandgap semiconductors, such as SiC[13,14] and GaN,[15–17] with similar techniques also applied to Ga_2O_3 based metal–oxide–semiconductor (MOS) structures to extract interface trap densities.[7,8,18] The presence of a "ledge" or "plateau" in CV profiles of Ga_2O_3 based MOS was observed purely under electrical stress,[2] while in other cases, it was observed when the devices were illuminated

under UV light.[8,18] For illumination with UV light above the bandgap of Ga_2O_3, the ledge has been attributed to trapped electrons at the Al_2O_3/Ga_2O_3 interface recombining with holes that were optically generated. Those authors used the Terman method[19] to estimate interface trap density from the CV ledge in the UV illuminated Ga_2O_3 MOS structures.[8,18] However, this technique has been found to be unreliable and erroneous in extracting interface trap density in SiC.[14] The Terman method assumes that the device is in equilibrium with the applied signal, in contrast to the non-equilibrium condition, which arises following exposure to UV light in wide bandgap materials. In contrast, Zhou *et al.*[7] observed a small shift in CV when exposed to above bandgap UV in an Al_2O_3/Ga_2O_3 MOS structure, which they used to extract an average interface trap density; however, an in-depth analysis has not been provided to explain the shift in CV. Hence, a model to explain the origin of the ledge or shift in CV under either above or below-bandgap UV illumination has not yet been provided.

A rigorous understanding and quantification of interface traps in Ga_2O_3 is essential to understand reliability in MOS based devices, like MOSFETs and trench Schottky barrier diodes. In this work, a comprehensive analysis on the origin of the capacitance ledge in Ga_2O_3 MOS structures is presented for the first time. The use of monochromatic sub-bandgap UV wavelengths eliminates the possibility of the ledge being due to optically generated holes (electrically generated holes are negligible). A simple equation to estimate the deep-level interface trap density by sweeping the UV illumination wavelength is discussed and compared with the shallow interface trap density extracted using the conductance method.[20] A peak interface trap density of $\sim 8 \times 10^{12}\,cm^{-2}\,eV^{-1}$ is extracted from 2.4 to 4.1 eV below the conduction band (CB) edge and is reported for the first time in Ga_2O_3 devices. Using the conductance method and the UV assisted CV technique, the interface trap distribution is estimated for almost the entire bandgap of Ga_2O_3.

II. EXPERIMENTAL SETUP

A cross-sectional schematic of a β-Ga_2O_3 MOS capacitor structure is shown in Fig. 1(a). The devices were fabricated on a (001) Halide Vapor Phase Epitaxial (HVPE) layer grown on a melt-grown Sn-doped n-Ga_2O_3 wafer from Novel Crystal Technologies, Inc. (NCT). The epitaxial region was 9.6 μm thick, having an unintentionally doped (UID) donor concentration of $2.5 \times 10^{16}\,cm^{-3}$ as measured by CV. The samples were initially cleaned with acetone,

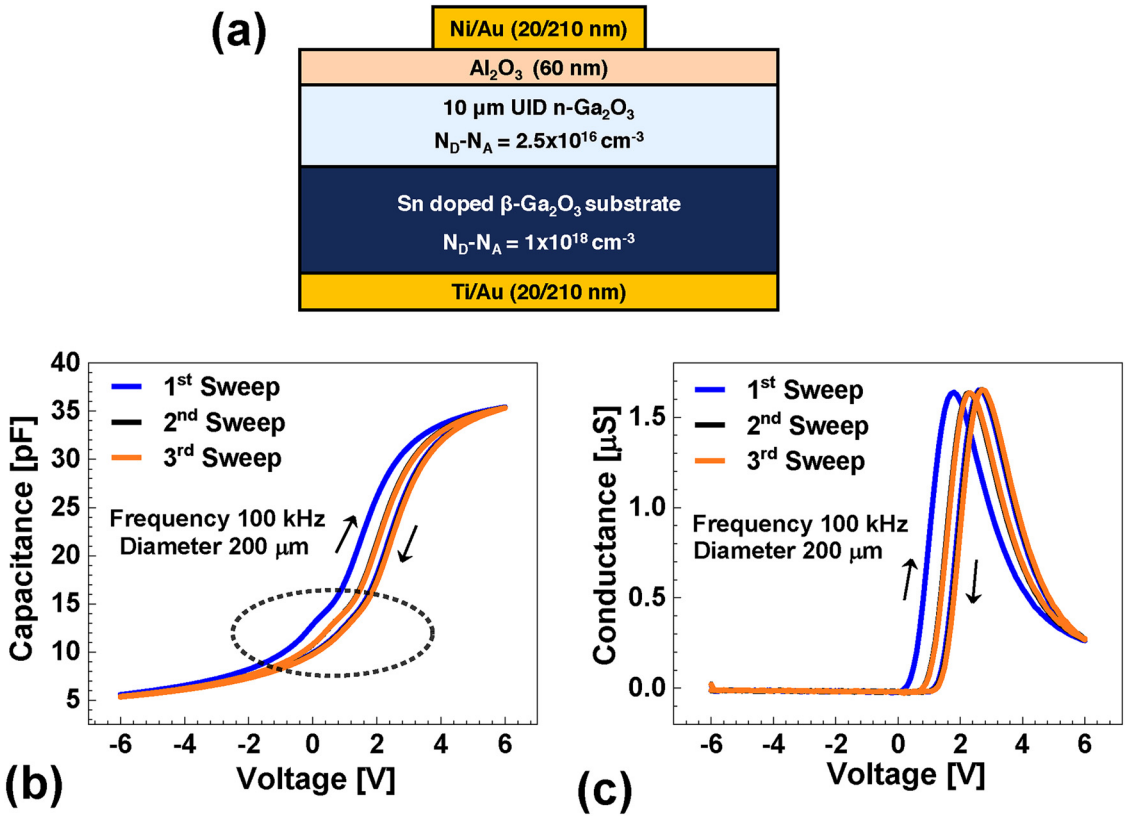

FIG. 1. (a) Cross-sectional schematic of an MOS capacitor. (b) CV characteristics of three consecutive sweeps. The dotted area points to a small ledge. (c) Conductance curve (GV) for corresponding sweeps.

isopropyl alcohol (IPA), and de-ionized (DI) water followed by 5 min in a boiling Piranha solution with a concentration ratio of 1:4 of H_2O_2 to H_2SO_4. Prior to dielectric deposition, the sample was soaked in a buffered oxide etch (1:7) for 20 min. These planar test structures were fabricated as part of a trench Schottky diode process, and the wet etch was used to round the trench corners. A 60 nm thick Al_2O_3 layer was deposited on Ga_2O_3 using thermal atomic layer deposition (ALD) at 300 °C with trimethylaluminum (TMA) and H_2O as precursors. Circular top contacts with diameters of 50, 100, and 200 μm were patterned using photolithography and formed by sputtering of Ni/Au (20/210 nm) metal contacts. No edge termination was included. The bottom contact was formed at the substrate back side by BCl_3/Ar based dry etching to remove the Al_2O_3 layer formed during ALD, followed by a blanket sputtering of Ti/Au (20/210 nm) to form an Ohmic contact.

The CV measurements were performed using a Keithley 4200A-SCS CV meter with a 30 mV AC amplitude at a range of frequencies. A Xenon based UV lamp source in combination with a tunable monochromator was used as a source for UV-assisted CV measurements, with reasonably constant power density for wavelengths from 300 to 550 nm. The constant power density ensures that the photon flux is sufficiently constant for all the wavelengths. The sub-bandgap light was shone on the top of the device at an angle less than 30° so that the illumination under the contact occurred by reflections from the back contacts. An Agilent E4980A LCR meter was used to measure the AC conductance spectra for frequencies from 100 Hz to 2 MHz and used to extract interface trap density, D_{it}, by the conductance method.[20] The leakage current was insignificant and found to be less than 10 nA/cm^2 for the range of voltages in which all the CV characteristics were measured.

III. CV CHARACTERISTICS

Figure 1(b) shows typical measured CV data for a MOS-cap structure at 100 kHz of AC frequency and a sweep rate of 5 V/s. When the dual sweep starting from −6 V was performed, there was a hysteresis associated with the CV curve, which reduced and saturated after subsequent sweeps. The flatband shift between the consecutive measurements is attributed to border charge trapping in states with de-trapping time significantly longer than the time period corresponding to the measurement frequency.[21]

A small plateau or ledge was observed in the forward sweep, which diminished during the reverse sweep. The capacitance ledge and peak in measured AC conductance occurs at two different voltage ranges [Figs. 1(b) −1 to 1 V and 1(c) 2 to 3 V, respectively], suggesting that these measurements are accessing traps in two distinct energy ranges. The peak in the measured conductance–voltage curve (GV) arises due to the inability of the trapped electrons at the interface to remain in quasi-equilibrium at the applied AC frequency.[22] This results in an RC-like phase lag from the applied AC signal, and the lost energy is seen as a peak in conductance.

IV. UV-ASSISTED CV MEASUREMENTS

For UV-assisted CV measurements, the device was first biased with a constant voltage while simultaneously illuminating with UV light for a fixed duration followed by a dual sweep CV measurement (in the dark) immediately after exposure. An example shown for −30 V bias and a UV wavelength of 300 nm (still below the bandgap of Ga_2O_3) for different exposure times is shown in Fig. 2(a). The width of the capacitance ledge (taken as the potential

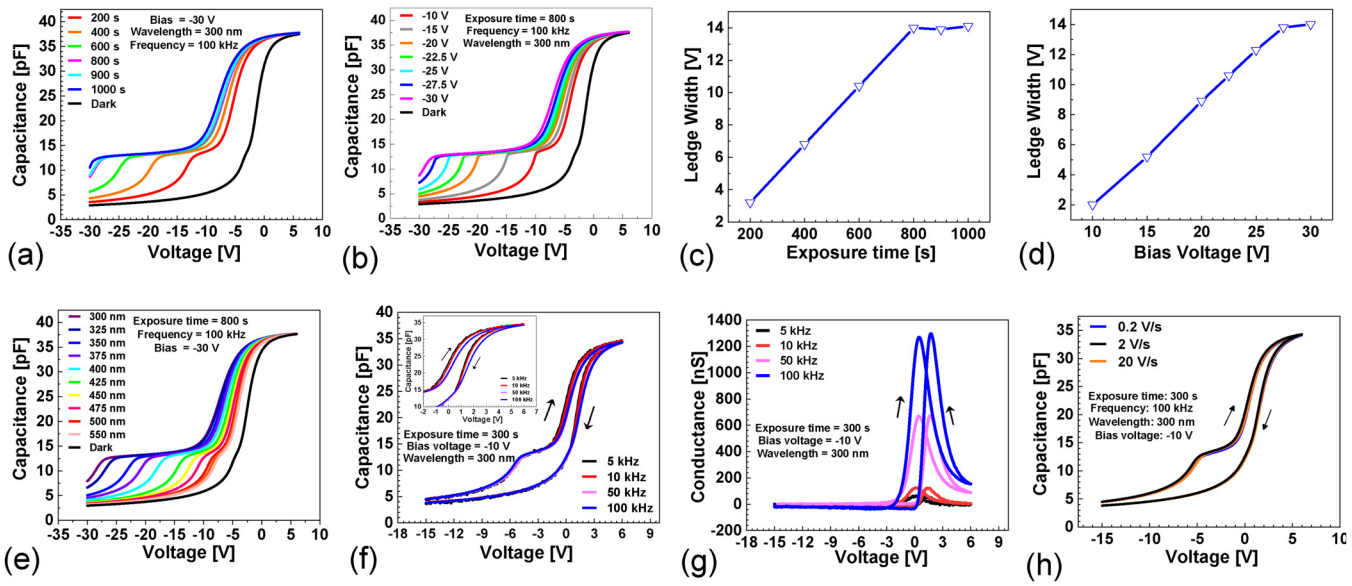

FIG. 2. UV assisted CV for a 200 μm diameter device with (a) different exposure times and (b) different bias voltages. (c) Ledge width extracted for measurements in (a). (d) Ledge width extracted for different bias voltages in (b). UV assisted CV (e) for different UV wavelengths (f) and (g) CV and GV with different measurement frequency, respectively, and (h) different sweep rate.

difference between capacitances corresponding to 12 pF and 14 pF) was observed to widen as the exposure time was increased, saturating after about 800 s of exposure time in this case. A measurement without application of any constant bias or UV light is denoted as a "Dark" curve in Fig. 2. Increasing bias voltage also resulted in an increase in the ledge width [Fig. 2(b)] before saturating at −27.5 V. Interestingly, for bias voltage less negative than −27.5 V (> −27.5 V), the ledge begins to originate from the voltage at which the device was biased at, as observed in Fig 2(b). The ledge width is extracted for CV curves with different exposure times and different bias voltages and is plotted in Figs. 2(c) and 2(d), respectively. This demonstrates that a complete saturation of ledge width is achieved with a UV exposure time of 800 s and a bias of −27.5 V.

When the wavelength of the light was swept from 300 to 550 nm [Fig. 2(e)], the width of the ledge decreased and saturated at about 450 nm. The measurement frequency had no measurable effects on the capacitance ledge, instead showing a change in slope of the CV curves from −1 to 6 V accompanied by the peak in measured AC conductance [Figs. 2(f) and 2(g)]. This supports the argument that the measurements are accessing two distinct energy ranges, the G–V peak being small time constant interface traps responding to the measurement frequency and the ledge due to deep energy traps that are sensitive to the UV wavelength and the applied bias. The measurement showed only very small changes in CV characteristics with a different sweep rate, plotted in Fig. 2(h).

V. DISCUSSION

The origin of the ledge could possibly be attributed to traps located in the bulk of the Al_2O_3, Ga_2O_3 or at the interface between Al_2O_3/Ga_2O_3. Since changes in the ledge width were observed when the device was exposed to a range of light wavelengths [Fig. 2(e)], we assume that the traps responsible for the ledge have a range of energy levels. Furthermore, the observation of saturation in ledge width suggests that the responsible states do not have a wide range of capture cross section as would occur for bulk states. Hence, we can assume that the traps are associated with the Al_2O_3/Ga_2O_3 interface. The response of interface traps can be understood with reference to different regions (Region I: −30 to −20 V, Region II: −20 to −10 V, and Region III: −10 to 6 V) of a specific CV characteristic shown in Fig. 3 with band diagram schematics in Figs. 4(a)–4(f).

Initially when −20 V bias is applied (bias lower than the saturation voltage of −27.5 V) on the device, the bands bend upward as shown in Fig. 4(a), with donor traps all occupied as indicated in the shaded region. 300 nm UV illumination results in electrons trapped in interface states with energies less than that corresponding to the illumination wavelength being excited to the CB and swept away from the interface by any band bending in the Ga_2O_3. This causes a reduction in the surface potential and increase in the electric field across the oxide due to the ionized donor traps at the interface. The surface potential drops until a steady state condition is reached when either of two limiting cases occur. Case (i): for the conditions of Fig. 3 (−20 V stress, 300 nm UV), UV generation rate equals electron capture rate and only partial ionization of the accessible trap states occurs [Fig. 4(b)]. Case (ii): for higher biases than

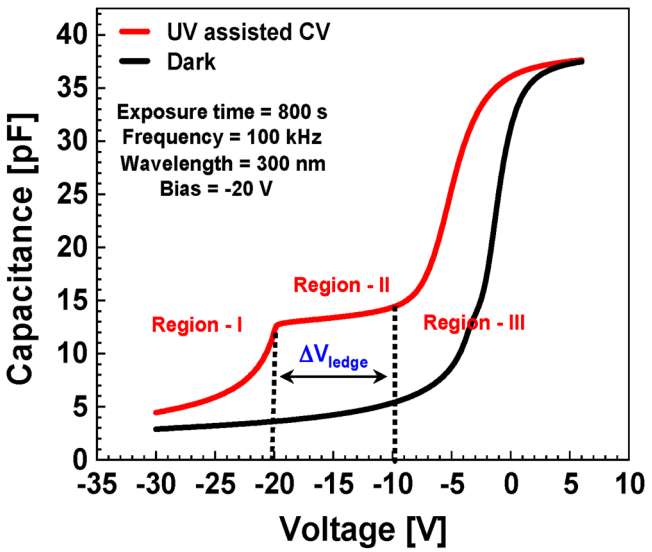

FIG. 3. A particular case of a UV wavelength depicting different regions of operations of CV characteristics.

the saturation voltage of |−27.5| V, all the UV accessible traps are emptied [Fig. 4(f) relating to −30 V stress, 300 nm UV].

When the UV illumination is turned off and the CV sweep from −30 to 6 V is performed, the different regions in Fig. 3 are explained using Shockley–Read–Hall (SRH) recombination rate, U_n (in $cm^{-2}\,s^{-1}$), given by[23,24]

$$U_n = n_s(\psi_s)\left\{1 - \exp\left(\frac{E_{f,T} - E_{f,n}}{kT}\right)\right\} \times \int_{E_v}^{E_c} c_n(E_T) n_T(E_T)(1 - f_T(E_T))\, dE_T, \quad (1)$$

where c_n is the capture probability, n_T is the density of trap states, E_T is the trap level, n_S is the carrier concentration at the interface, ψ_s is the surface potential, f_T is the Fermi–Dirac probability distribution function corresponding to the trap Fermi level, and $E_{f,T}$ and $E_{f,n}$ are the Fermi level of bulk Ga_2O_3. The integral is over the entire bandgap—from the valence band (VB) edge, E_v, to the conduction band, E_c.

A. Region I

In the region where the voltage is swept from −30 to −20 V, the relatively large surface potential [Fig 4(c)], ψ_s, leads to a low surface electron density with large capture time constant $\left(\tau = \frac{1}{c_n n_s}\right)$ and, hence, low values of recombination rates, even though there is a high density of empty states, $n_T(1 - f_T)$. Under this condition, a non-equilibrium system is attained with no change in the interface state charge. As a result, the recombination current is much lower than the quasi-static sweep current, i.e., $qU_n \ll C_m\left(\frac{dV_g}{dt}\right)$, where C_m is the measured MOS capacitance, dV_G/dt is the voltage sweep

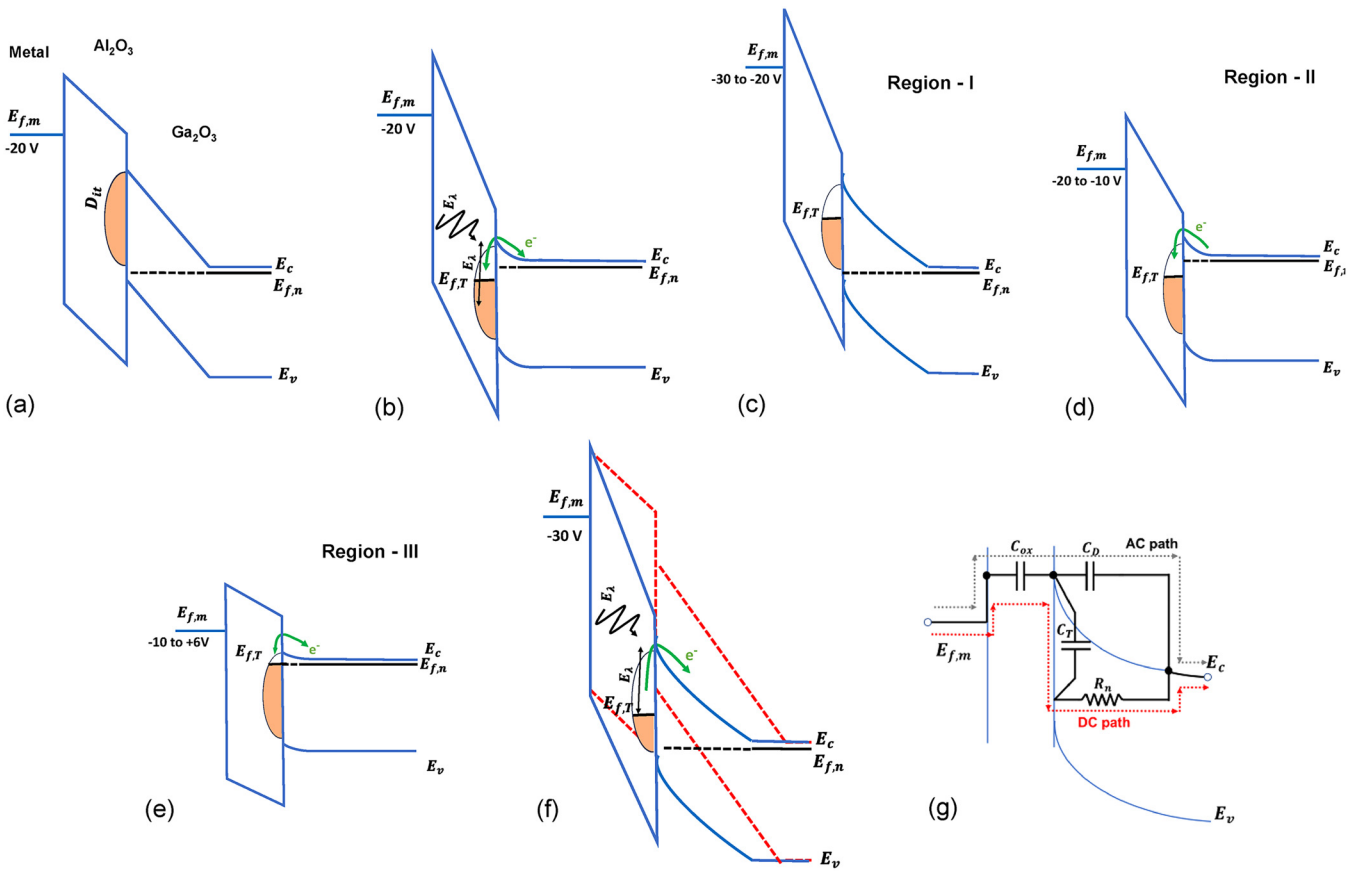

FIG. 4. (a)–(e) Band diagram to explain different regions of the CV characteristics in Fig 3. (a) When −20 V is applied, the bands move upward, but deep states do not change the charge state. (b) When −20 V bias and 300 nm UV are both applied, the field across the oxide increases compared to (a) and reduces the surface potential of Ga_2O_3 until a steady state condition is reached when a generation rate becomes equal to the recombination rate, preventing all the UV accessible deep traps from being fully emptied. (c) Region I: voltage sweep −30 to −20 V, interface trap charge is constant, and depletion width changes. (d) Region II: When the sweep is around −20 V, the interface carrier concentration is high enough for the traps to start filling and the surface potential becomes fixed leading to a ledge. (e) Region III: Around −10 V, the deep traps are filled and the device is in quasi-equilibrium with the shallow traps. (f) Complete emptying of all UV accessible traps can occur at high bias (−30 V bias) as in Fig. 2(e); the dotted lines represent the band bending without any UV illumination. (g) Equivalent circuit applicable to the ledge behavior in CV sweep.

rate, and q is the elementary charge. There is a net increase in the capacitance in this region compared to the dark condition (without any illumination) as observed between −30 and −20 V in Fig. 3. This increase arises due to a left shift of the capacitance under dark condition consistent with these traps behaving as donors with the amount of the left shift proportional to the emptied trap density (positive charges).

B. Region II

When the voltage is around −20 V, the bands are bent [Fig 4(d)] such that the carrier concentration at interface, n_S, is sufficiently high that the electrons start to recombine with the traps at a significant rate. Once there is a sufficiently high recombination rate, the quasi-static sweep current becomes equal to the recombination current, $C_{ox}\left(\frac{dV_g}{dt}\right) \approx qU_n = \frac{dQ_{ss}}{dt}$, where $\frac{dQ_{ss}}{dt}$ is the rate at which surface states are filled. The gate bias is screened and the surface potential becomes fixed, resulting in almost no change in the width of the depletion region with voltage sweep. The constant depletion width results in constant capacitance, which is observed as a ledge in the measured CV curve. The measurement is unable to directly observe the recombination of the traps. The majority carrier lifetime is inversely proportional to carrier concentration $\left(\tau = \frac{\epsilon}{q\mu n_S}\right)$.[22] At the edge of the depletion region, the carrier concentration is almost equal to the doping concentration meaning that its lifetime is small enough for it to always respond to high frequency CV measurements. By contrast, the relatively low carrier concentration at the interface corresponds to a large lifetime (~10 s), which causes trapped carriers to respond poorly to the

high frequency AC-signal. The combination of fixed surface potential as well as the fact that the 100 kHz measurement frequency probes only the edge of the depletion region causes constant capacitance in Region II as seen experimentally.

These mechanisms can be visualized simply using an equivalent circuit depicted in Fig. 4(g). The recombination current corresponding to the DC sweep flows through the capacitance, C_T, and resistance, R_n, equivalent of the traps as indicated by the dotted red "DC path" in Fig. 4(g). As previously mentioned, due to the large time constants of trapped carriers at the interface and low time constant at the depletion edge, the AC small-signal is coupled only to the depletion capacitance marked as the "AC path" in Fig. 4(g).

This non-equilibrium filling of traps due to quasi-static sweep current is not the same as the commonly observed "stretch-out" in CV curves. The stretch-out that is observed widely in Si devices during quasi-static CV measurements[25] occurs when the trap states are in quasi-equilibrium with the Fermi level. However, in this case, the Fermi levels are in non-equilibrium condition, and techniques, such as the Terman method, cannot be applied to extract interface trap density.[14]

C. Region III

Toward the end of Region II, the traps are filled and $E_{f,T}$ becomes aligned to $E_{f,n}$ corresponding to weak depletion as shown in Fig 4(e). Under this condition, the system will be in a quasi-equilibrium state. The small surface potential and the small depletion width results in a higher carrier concentration near the interface; the trapped electrons are able to respond to the measurement frequency, exhibiting an RC-like lag, which is observed as a peak in measured conductance, and a stretch-out in the CV curve as seen in Fig. 3. The shift in the flatband voltage when comparing CV curves with and without UV illumination could be because of small capture cross-sectional area traps, e.g., the presence of border traps,[21] which respond on a longer timescale than the CV sweep.

Using the model described above, the results of the measurement in Figs. 2(a)–2(h) can be explained. The increase in the ledge width in Figs. 2(a) and 2(c) under increasing exposure time is due to the finite time for electrons to be swept away from the interface, with the saturation occurring when all accessible traps are emptied.

The dependence of ledge width on applied bias [Figs. 2(b) and 2(d)] is a result of the UV induced interface charge producing a reduction in Ga_2O_3 band bending. The ledge width corresponds to the band bending for which quasi-equilibrium between UV generation and electron capture occurs (during UV illumination) and this increases with bias [Fig. 4(b)]. The trap charge increases until saturation occurs for stress exceeding $|-27.5\ \text{V}|$ when all UV accessible traps are emptied [Fig. 4(f)].

The ledge width decreases in Fig. 2(e) with the increase in the wavelength due to the decreased de-occupation of deep-level interface states, decreasing the total number of carriers excited into CB. Here, the -30 V bias ensures that all UV accessible states are emptied [as in Fig. 4(f)]. This clearly rules out the possibility of the ledge occurring due to energy localized high interface state density, which would then have a threshold photon energy below which the ledge would cease to exist and above which the ledge would remain constant irrespective of changes in photon energy.

When the frequency of the measurement was varied [Figs. 2(f) and 2(g)], there was no significant change in the behavior of the ledge observed in the CV data, as these are deep energy traps and hence, their time constants are rather large. Only those traps in weak depletion (Region III) could respond to the changes in AC frequencies of the CV measurements as these are shallow states. There were also no significant changes in CV characteristics with a sweep rate [Fig. 2(h)]. Even though the sweep rate is increased by a factor of 100, the corresponding change in surface potential in the ledge would only be about 140 mV (equivalent to a 70 mV/decade), which is not significant compared to the ledge width.[26]

An increase in the ledge width has been reported[8,18] with an increase in the dielectric thickness. This is consistent with the model presented here, as increasing oxide thickness decreases the oxide capacitance. To fill the same number of interface charges, the decreased oxide capacitance would require larger voltage swings ($Q = C_{ox}\Delta V$) since the ledge always occurs at the same surface potential energy. The ledge is, therefore, observed at more negative voltages compared to that of a thinner dielectric, manifesting as an increase in the ledge width.

VI. INTERFACE TRAP DENSITY (D_{IT})

The model presented can be used to extract interface trap density, D_{it}, using the CV data for different illumination wavelengths [Fig. 2(e)]. It is assumed that the illuminated wavelength excites all the trapped charges corresponding to the energy of the illumination, $E(= hc/\lambda)$, below the CB at the interface between Al_2O_3/Ga_2O_3. Under this assumption, a net change in the occupancy of interface traps is observed as a ledge in the CV curve. Therefore, the charge density is dependent on the energy of the exposing photon. If $N(E)\left(=\frac{Q(E)}{qA}\right)$ is the charge density that is excited for energy, E, for a small increase in the energy of the photon, ΔE, the trap density would increase as $N(E+\Delta E)$. The change in the trap density is then given by

$$N(E+\Delta E) - N(E) = \frac{Q(E+\Delta E) - Q(E)}{qA}, \tag{2}$$

where $Q(E)$ corresponds to the total charge up to energy E,

$$D_{it} \equiv \frac{N(E+\Delta E) - N(E)}{\Delta E}, \tag{3}$$

using Eq. (2), the interface trap density is given by

$$D_{it} = \frac{1}{qA} \cdot \frac{Q(E+\Delta E) - Q(E)}{\Delta E}. \tag{4}$$

The total charge at each energy can be calculated using $Q(E) = C_{ox}\Delta V$, where C_{ox} is the oxide capacitance and ΔV is width of the ledge. The density of charges released under different illumination wavelengths is shown in Fig. 5(a), corresponding to trap energies from 2.4 to 4.1 eV for wavelengths from 550 to 300 nm. Using the values obtained for charge densities in Fig. 5(a), the interface trap densities are determined using Eq. (4) with a peak D_{it}

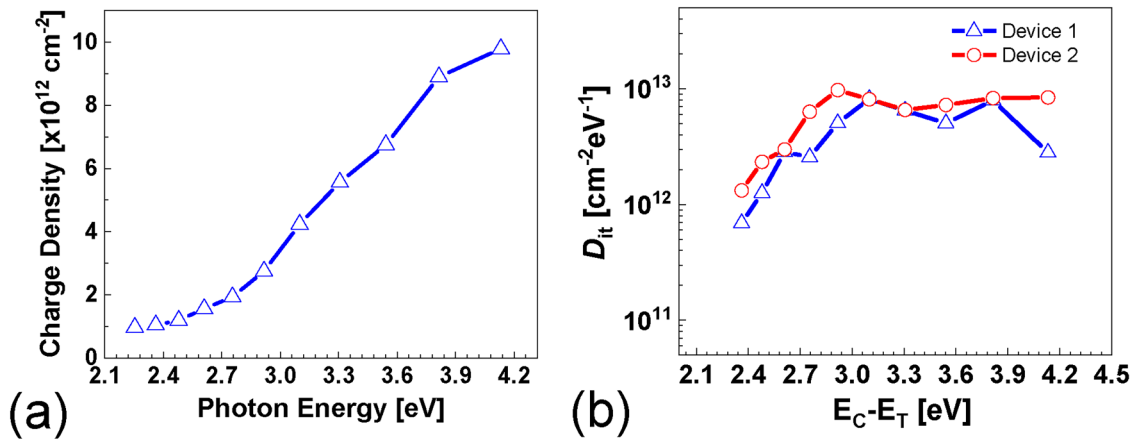

FIG. 5. (a) Net interface charge density excited by light as a function of photon energy. (b) Interface trap density, D_{it}, determined by taking the gradient of values obtained in (a) as derived using Eq. (4) for two different devices.

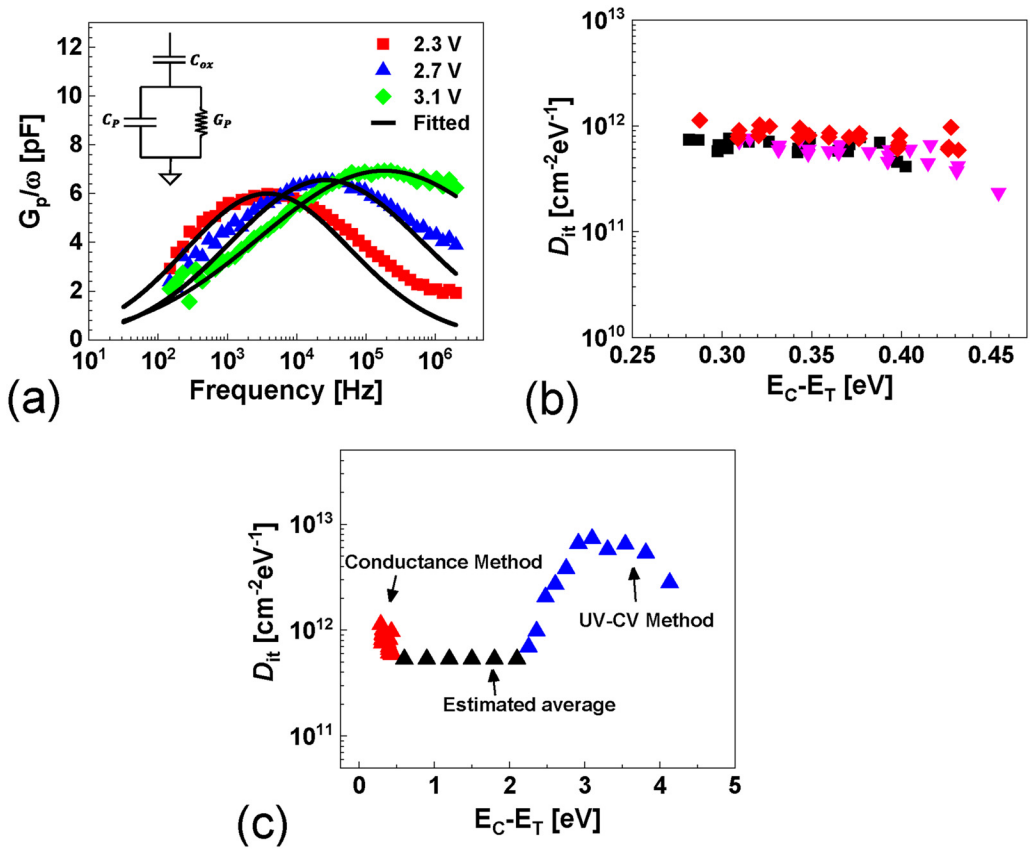

FIG. 6. (a) Experimental G_P/ω curve (scattered plot) for different DC points fitted using Eq. (5) (solid line). (b) D_{it} against trap energy extracted using Eq. (6) for three different devices. (c) D_{it} using two different techniques—conductance and photo-assisted CV methods to quantify shallow and deep energy traps, respectively.

of about $8 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, plotted in Fig. 5(b), demonstrating the presence of a broad peak in trap density 2.5–4 eV below the CB.

VII. SHALLOW TRAPS

The density of shallow interface traps was extracted using the conductance method from Nicollian and Goetzberger.[20] The frequency dispersion of the AC conductance is used to extract the D_{it} by fitting measured curves with theoretical equations. Initially, the measured capacitance and conductance, C_m and G_m, respectively, are converted to parallel capacitance and conductance model, C_P-G_P, shown in the inset of Fig 6(a). The G_P/ω is calculated using Eq. (5) where C_{ox} is the oxide capacitance and ω is the measurement frequency in radians/s,

$$\frac{G_P}{\omega} = \frac{C_{ox}^2 G_m/\omega}{(G_m/\omega)^2 + (C_{ox} - C_m)^2}. \tag{5}$$

In fitting of G_P/ω curves, we include the effects of a random distribution of the charges across the interface, which causes fluctuations in surface potential by incorporating a statistical broadening parameter σ_s. This broadening parameter σ_s is the standard deviation of surface potential in units of $k_B T/q$,

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\xi\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1 + \xi^2 \exp 2\eta) d\eta, \tag{6}$$

where $\eta = \psi_s - \psi_s$ is the deviation of the surface potential ψ_s from the mean, $\xi = \omega\tau_n$ is the frequency and electron capture time constant dependent term, and D_{it} is the interface trap density. The procedure to extract D_{it} is well explained in Nicollian and Brews.[22] The fitted G_P/ω curves are plotted against the measured curves in Fig. 6(a). The σ_s extracted from this technique was between 2 and 4 kT/q. We note that C_{ox} was determined using an ellipsometer measured thickness ($= A\epsilon_{ox}/t_{ox}$) of 59.2 nm and a relative dielectric permittivity of 10 for Al_2O_3.[27] This was essential since using the maximum measured capacitance in accumulation (as is done frequently) results in a very significant systematic error in fitting G_P/ω due to the finite depletion capacitance.[28] The extracted shallow D_{it} is plotted in Fig. 6(b). A decrease in the trap density is observed away from the conduction band edge, with a maximum density of $\sim 10^{12}\,\mathrm{cm}^{-3}$ around 0.3 eV.

Combining the UV assisted CV and conductance technique, the distribution of D_{it} across the bandgap is displayed in Fig. 6(c). Using the charge density calculated for 550 nm wavelength exposure, an average interface trap density of about $5 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ is estimated between the energies of 0.5 and 2.2 eV, indicating the presence of a significant drop in D_{it} between the near band-edge shallow states and the deep traps. This result is inaccessible without the use of the complementary UV assisted CV and conductance measurements and should aid in optimizing the interface in Ga_2O_3 based MOS structures, especially in devices, such as trench Schottky diodes and MOSFETs where the high blocking voltage could ionize these donor states. The positively charged donor states could increase the field across the oxide and lead to device breakdown and make the devices less stable and reliable. Hence, interface engineering to optimize the interface trapping is essential to achieve high power devices with high reliability.

VIII. CONCLUSION

A ledge in the photo-assisted CV characteristics of Ga_2O_3/Al_2O_3 MOS structures was observed, responding to changes in parameters, such as applied bias and wavelength of the exposed light. The origin of the ledge was attributed to the surface potential remaining fixed as a result of the bias independent recombination current, with a model presented to explain its behavior. A novel technique to quantify deep-level interface trap density by varying photon energy is presented. A broad peak in deep-level interface trap density was found between 2.4 and 4.1 eV below the CB of Ga_2O_3, with a maximum density of $\sim 8 \times 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, with a separate shallow interface state contribution rising toward the band edge with maximum density $\sim 10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. A combination of these two methods provides a useful tool to quantify traps for device optimization, modeling, and reliability studies.

ACKNOWLEDGMENTS

The work of Aditya K. Bhat was supported by the Engineering and Physical Sciences Research Council (EPSRC) Doctoral Training Program (DTP) under the Grant EP/X015882/1. Martin Kuball acknowledges financial support by the Royal Academy of Engineering through the Chair in Emerging Technologies Scheme.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Aditya K. Bhat: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Hyun-Seop Kim:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal). **Abhishek Mishra:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Matthew D. Smith:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (supporting); Writing – review & editing (equal). **Michael J. Uren:** Conceptualization (lead); Formal analysis (equal); Investigation (equal); Methodology (lead); Supervision (equal); Writing – review & editing (lead). **Martin Kuball:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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