https://doi.org/10.1063/1.359905

Mechanism for stress-induced leakage currents in thin silicon dioxide films

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(Received 30 March 1995; accepted for publication 8 June 1995)

Leakage currents introduced in the low-field, direct-tunneling regime of thin oxides during high-field stress are related to defects produced by hot-electron transport in the oxide layer. From these studies, it is concluded that the "generation" of neutral electron traps in thin oxides is the dominant cause of this phenomenon. Other mechanisms due to anode hole injection or oxide nonuniformities are shown to be unrealistic for producing these currents. Exposure of thin oxides to atomic hydrogen from a remote plasma is shown to cause leakage currents similar to those observed after high-field stress, supporting the conclusion that these currents are related to hydrogen-induced defects. © *1995 American Institute of Physics.*

I. INTRODUCTION

In the early 1980s, Maserijian and Zamani first reported the observation that currents measured on thin oxides (4–5 nm in thickness) at low applied electric fields increased after stressing at high fields.[1] The low-field current measurements were performed at low voltages, typically $\lesssim$3 V applied bias for n-type silicon (Si) or aluminum (Al) electrodes, referred to as the direct tunneling (DT) regime. As illustrated in Fig. 1(a), the DT current measured in the external circuit is produced by electrons tunneling from the cathode contact to the anode contact without entering the oxide conduction band. The stressing was performed at higher fields where the electrons tunneled first into the oxide conduction band before entering the anode contact [as shown in Fig. 1(b)]. This latter type of tunneling phenomenon, well known to the device community, is called Fowler–Nordheim (FN) tunneling. Maserijian and Zamani assumed that the increase in the DT current was caused by oxide film deterioration due to the presence of hot electrons in the oxide conduction band.[1] They further tried to relate the current increases in the DT regime to the presence of positive oxide charges generated near the anode during FN stress. They also believed that the number of positive charges generated was related to the water content of the film. Although electron heating in the oxide conduction band due to the applied field was not a well understood or accepted phenomenon until the mid-1980s,[2–8] Maserijian and Zamani argued that oscillations observed in the FN tunneling characteristics could be interpreted in terms of ballistic electron transport. Several years later their assumptions on carrier heating and their interpretation of ballistic transport in thin oxides would be shown to be correct.[6,7]

Since their seminal report, many researchers have repeated the experiments of Maserijian and Zamani obtaining similar results.[9–13] However, the interpretation of these results has been controversial with many different models being used to explain the current increases in the DT regime, currently referred to as stress-induced leakage current (SILC). Some researchers have proposed that SILC is caused by interface-state generation,[10,11] while others claim that it is due to bulk-oxide electron-trap generation.[12] Still others have proposed that it is due to nonuniformities or weak spot formation in the oxide films.[9] Also recently, the positive charge model of Maserijian and Zamani has reappeared with the charges due to trapped holes injected from the anode.[14,15] In all these cases, there has never been a concentrated attempt to correlate SILCs with *all* the different possibilities. In the study undertaken here, this correlation has been done, and it will be shown that the SILCs can be best explained by the generation of neutral electron traps in the oxide layer. These sites allow more SILC to flow through the oxide layer by acting as "stepping stones" for tunneling carriers. This phenomenon is often referred to as trap-assisted tunneling [see Fig. 1(c)]. Furthermore, the generation of these neutral sites will be demonstrated to be caused mainly by the "trap creation" (TC) phenomenon which is related to hydrogen release by hot electrons.[16–25] Trapped holes[26–29] or sites produced by trapped-hole annihilation by free electrons[30–34] will be demonstrated not to contribute to SILC for most stressing conditions. Lateral nonuniformities (LNUs) will also be shown not to be as important for SILC.

Recent remote hydrogen plasma experiments have provided strong independent support for the "trap creation" process.[35–40] Atomic hydrogen from a remote plasma has been shown to be highly reactive in the Si/SiO_2 interfacial region at room temperature, causing fast interface states[35–37] and positively charged slow states.[38,40] The charge centroid of hydrogen-induced slow states was found to be 2–3 nm away from the Si/SiO_2 interface.[40] Such distributed defects can be expected to give rise to trap-assisted tunneling. By exposing thin oxides to a remote plasma, it will be directly demonstrated that atomic hydrogen induces leakage currents similar to those observed after high-field stress.

Since the oxide deterioration producing SILC will be shown here to be caused by electron heating in the oxide layer, oxide defect formation due to hot carriers will be briefly reviewed. The production of interface states or traps by the annihilation of trapped holes and/or their presence is one component of the oxide degradation process.[26–29] The other component is due to the "trap creation" process also caused by hot electrons.[16–28] The oxide degradation process produced by these two mechanisms is schematically depicted in Fig. 2 using energy band diagrams.

Trap creation [Fig. 2(a)] occurs when any electron with energy greater than 2 eV (with respect to the bottom of the

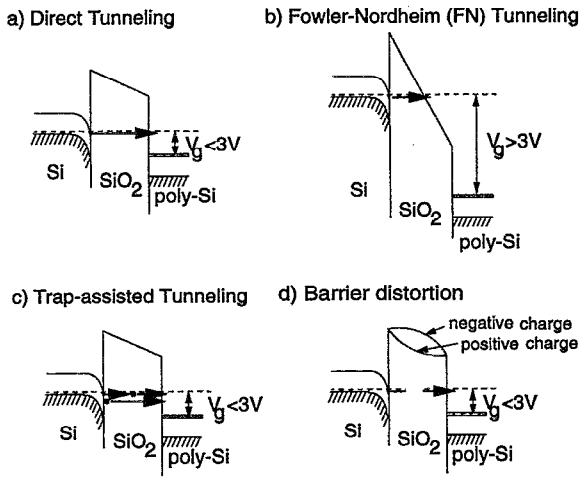

FIG. 1. Schematic energy-band diagram showing (a) direct tunneling of electrons from the cathode to the anode contact, (b) Fowler–Nordheim tunneling of electrons from the cathode to the bottom of the SiO_2 conduction band with subsequent ballistic transport through the oxide to the anode, (c) two examples of trap-assisted tunneling in the direct tunneling regime including the use of both interfacial and bulk oxide sites, and (d) direct tunneling with barrier (field) distortion caused by trapped negative and positive oxide charges.

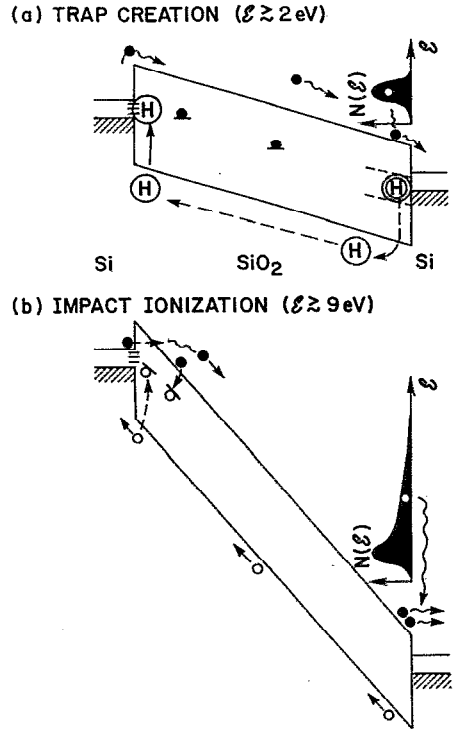

FIG. 2. Schematic energy-band diagram showing (a) trap creation near the cathode caused by mobile hydrogen release from decorated sites near the anode and (b) defect generation near the cathode caused by free-electron/trapped-hole recombination or by the presence of the holes themselves where the holes were generated in the oxide bulk by impact ionization or injected from the anode.

oxide conduction band) releases hydrogen from defect sites near the anode interface, usually leaving behind positively charged sites.[16–28] This mobile species can then move to the cathode-oxide interface where it produces interface states and a distribution of oxide electron traps near this interface. Also, generation-recombination sites and boron deactivation can be produced in the Si substrate by the hydrogen. The trap creation process is thermally activated, has a weak oxide thickness dependence (for films over 10 nm), and is observed at fields as low as 1.5 MV/cm (Refs. 16–28). It is measurable only after injection of $\gtrsim 0.001$ C/cm^2 (Refs. 26–28) under positive-gate voltages for structures which have undergone poly-Si gate processing. Some background trapping in as-fabricated bulk-oxide sites (due to the presence of water or OH) can also occur,[41] but this is not an important contribution in thin oxides for most cases.

Figure 2(b) schematically depicts how the trapped holes are introduced during FN stressing.[26–28] The high-energy tails that develop on the hot-electron energy distribution can generate holes by band-gap impact ionization, requiring an energy of $\gtrsim 9$ eV. This phenomenon has been discussed in many recent publications.[26–28] These mobile holes produced in the oxide bulk closer to the anode move under the applied field to the cathode-oxide interface where some are trapped in energetically "deep" sites (believed to be due to oxygen vacancies).[42,43] Some of the injected electrons from the cathode recombine with these trapped holes producing interface states and traps near the cathode.[26,30,31] The remainder of the trapped holes can induce "slow" interface states by their presence.[29] The hole generation/trapping process is weakly dependent on lattice temperature, has a strong oxide thickness dependence up to about 50.0 nm, occurs only at fields exceeding ≈ 7 MV/cm, and is measurable at injected fluencies as low as 1×10^{-6} C/cm^2 (Refs. 26–28). In addition to band-gap impact ionization, recent studies have shown that some hole injection from near the anode/oxide interface can still occur down to energies of 5 eV (Ref. 44). The effects of these injected holes cannot be distinguished from those due to band-gap ionization. Both phenomena (trap creation and hole generation/trapping) are dependent on oxide processing. Similar interfacial defect generation can also occur near the anode from both of these mechanisms.

This report will be divided into three major sections. In Sec. III A, the dependence of SILC on injected charge fluence, stressing voltage, sensing voltage, oxide thickness, Si-substrate doping, and temperature will be investigated. A universal dependence for SILC as a function of hot-electron energy will then be demonstrated. In Sec. III B, the defect generation in the oxide film including trapped holes, trapped electrons, positive charge near the anode and interface states (fast and slow) as a function of hot-electron energy will be compared to that of SILC. From this comparison, it will be determined that the neutral electron traps generated by the "trap creation" phenomenon produce most of the current increase observed. Finally, the results of the remote plasma experiments will be presented in Sec. III C, showing that defects produced by atomic hydrogen are responsible for the low-field leakage currents.

II. EXPERIMENT

A. Sample preparation

In these studies, many wafer sets containing both n- and p-channel field-effect transistors (FETs) of various sizes and geometries fabricated over a period of ten years were studied. The Si substrates were (100) orientation with resistivities varying from 0.1 to 30 Ω cm and oxide thickness varying from 3.7 to 5.5 nm. All gate electrodes were n-type, degenerately doped, self-aligned poly-Si with areas varying from 6.45×10^{-4} to 8.95×10^{-6} cm^2. All gate oxides were thermally grown at a temperature of 900 °C. Unless specifically discussed, the results presented in this report did not depend on device area or geometry. For the remote plasma experiments, furnace oxides with thickness varying from 3.2 to 6.2 nm were grown at 850 °C on (100) Si with a resistivity of 0.1–0.2 Ω cm. Aluminum gates, 16 nm in thickness, were deposited after hydrogen exposure using a shadow mask.

B. Measurement techniques

Current injection into the oxide from the cathode was performed using "direct" [Fig. 1(a)] or Fowler–Nordheim [Fig. 1(b)] tunneling.[17,26] The stress currents were provided by FN injection from the cathode. The FN electron currents measured in the external circuit are interface limited by the electric field near the cathode. In addition to producing traps and interface states via the "trap creation" phenomenon, Fowler–Nordheim injection was also used to produce trapped holes by hot-electron-induced band-gap impact ionization or anode-hole injection.[26–28,30] "Direct" tunneling of carriers was used to "sense" oxide deterioration produced by the hot-electron stress at larger fields.[1] These currents depend on the oxide thickness and on the shape of the trapezoidal energy barriers formed by the energy steps at the two contacts and the energy position of the SiO_2 conduction band (see Fig. 1 and Ref. 1). As will be shown here, the DT currents also depend on the density and distribution of traps sustaining trap-assisted tunneling.

A wide variety of measurement techniques have been used here to track and spatially locate the trapped oxide charge (both positive and negative) and interface states. These included high-frequency capacitance-voltage (CV),[45] current-voltage (IV),[17] and current as a function of time (It) on FET devices.[26] Additionally, quasistatic CV techniques were used on the capacitor structures needed for the atomic-hydrogen exposure studies.[36] The It and IV techniques were used to measure the magnitude of oxide charge, locate the charge spatially, and sense for lateral nonuniformities (LNUs). The CV techniques were used to measure oxide charges and interface states ("fast" and "slow"). This large number of techniques were necessary in order to locate and separate oxide charge from interface states and to determine the possible effects of LNUs.

The remote plasma system used for the hydrogen experiments has been described previously.[36,39] To study the effects of atomic hydrogen alone, special care was taken to prevent UV and VUV irradiation during exposure. The hydrogen flux onto the sample surface was calculated from the energy deposited by hydrogen recombination on the surface of a Ag foil in a bolometric sensor.[39] These measurements were performed *in situ* during hydrogen exposure. It has recently been shown that atomic hydrogen does not penetrate through thin Al or through poly-Si gates and its diffusion into the gate oxide from the device edge is extremely limited in large area (10^{-3} cm^2) capacitors because of its high reactivity at the silicon/aluminum-oxide interfaces. Therefore, gate-free samples were exposed, and then thin Al gates were deposited through a shadow mask for electrical characterization after exposure. No annealing of hydrogen induced defects occurs during metal evaporation. This was verified by performing the electrical characterization on an exposed oxide with a mercury probe prior to Al metallization.

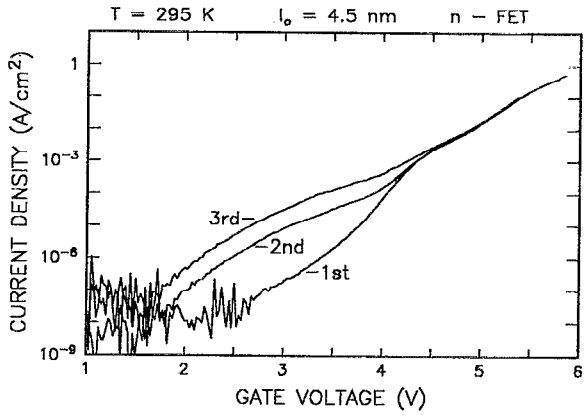

FIG. 3. Current as a function of gate voltage for an n-channel FET with a gate oxide thickness of 4.5 nm at room temperature. Three ramping sequences were performed from 1.0 to 5.38, 5.65, and 5.85 V, respectively, at a ramp rate of 0.025 V/s. A significant increase, mostly in the regime of direct tunneling current, is observed after each ramping sequence to a larger positive-gate voltage.

III. EXPERIMENTAL RESULTS

A. Stress-induced leakage currents

A typical example of the SILC phenomenon is shown in Fig. 3. The current is measured here in the external circuit from an n-channel FET with the source, drain, and substrate grounded and the poly-Si gate sequentially ramped to larger positive-gate voltages. The first ramping sequence shows the expected oscillations in the FN current above 3 V due to near ballistic transport of the electrons in the oxide conduction band.[1,6,7] Below 3 V, the electrons cannot enter the oxide conduction band and the measured currents are due to direct tunneling through the trapezoidal oxide energy barrier (see Fig. 1). As will be discussed later, this value for the energy barrier can vary by ≈0.3 eV depending on whether the substrate is in accumulation or inversion for the electrons.[46]

The current recorded with the second ramping sequence is significantly larger in the direct tunneling regime. At higher voltages, this IV characteristic appears to follow more closely the expected FN characteristic. The current in the direct tunneling regime is further enhanced in the third voltage scan. As will be shown in the sections below, the first voltage ramp must exceed ≈5 V to cause a measurable current increase during subsequent ramping sequences.[13]

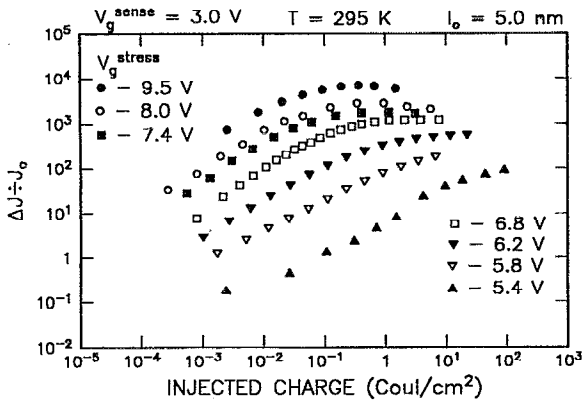

FIG. 4. Normalized current increase measured in the direct tunneling regime at a sense voltage of 3 V as a function of FN-injected electronic-charge fluence for various stressing voltages. For these data, p-channel FETs with 5.0-nm-thick gate oxides were stressed and then DT-current sensed at room temperature. These data show both linear and saturated regions from low to high charge fluence.

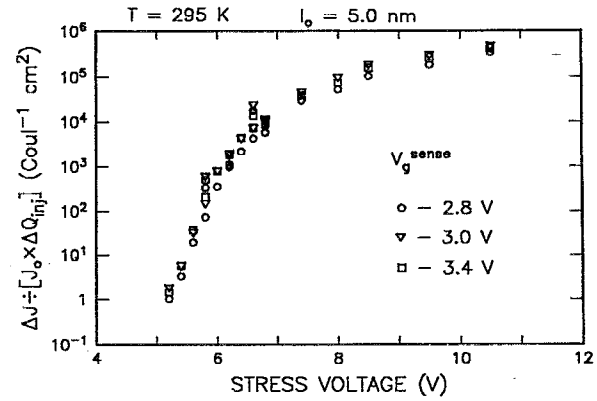

FIG. 5. Normalized SILC generation probability as a function of FN-stress voltage for sense voltages of 2.8, 3.0, and 3.4 V at room temperature. These values for the generation probabilities were determined from the slopes in the linear regions of data similar to those in Fig. 4.

Many researchers have used stepped- or ramped-voltage techniques to investigate SILCs, as depicted in Fig. 3.[1,10–13] With such measurements it is difficult to separate the effects of the oxide field from those of the injected electron fluence. To minimize this problem, SILCs were generated by stressing at constant applied field (gate voltage) for increasingly larger amounts of FN-injected electron fluence. Where possible, the starting fluence levels are kept below values necessary for any stress-induced effects to be observed. After stressing, the resulting SILC is *immediately* measured (within seconds) at a lower gate voltage where electron energy and fluence do not produce any additional oxide damage or current increases. Rapid recording of the SILCs after FN stress was used to minimize effects due to slow transient decreases in the currents in the direct tunneling regime (observed in most cases).

1. Injected electron fluence

An example of SILC measurements is shown in Fig. 4. The normalized current increase is plotted as a function of electron fluence during FN stress at various gate voltages (V_g^{stress}) for p-channel FETs with 5.0-nm-thick gate oxides. For each stress voltage, a virgin, as-fabricated device was used with all stressing and sensing being performed at room temperature. The SILCs were measured at a sense voltage (V_g^{sense}) of 3 V after each stress. The normalized current increase is defined as $\Delta J \div J_0$, where $\Delta J = J - J_0$ and the currents J_0 and J are the initial current of the as-fabricated device and the current after FN stress (SILC) measured at the indicated sensing voltage, respectively (see Fig. 3). Each data set in Fig. 4 shows two distinct regions. Initially, the SILCs increase linearly with electron fluence. At large fluence, saturation of the SILCs is observed.

2. Stress voltage and sense voltage

To investigate the dependence of SILCs on stress voltage, normalized SILC per unit of injected electronic charge (Fig. 5), in the following referred to as SILC generation probability, and SILC saturation levels (Fig. 6) have been extracted from the linear and saturation region in Fig. 4, respectively. (Later, these gate voltages will be related to electron energy.) The saturation levels shown in Fig. 6 can be interpreted as indicating a steady-state condition for the SILCs. The data in Fig. 5 increase by five orders of magnitude between 5 and 7 V suggesting a threshold for the generation of SILC at about 5 V. At this voltage, a ballistic electron in the SiO_2 will arrive at the anode/oxide interface with an energy of ≈2 eV (5 V minus the ≈3 V energy barrier at the cathode/oxide interface).[6,7] The results in Fig. 5 will be related to the "trap" creation phenomenon due to hydrogen release by electrons with energies ≳2 eV in later sections of this report.

Also shown in Figs. 5 and 6 are data for SILC generation probabilities and saturation levels obtained at other sensing voltages of 2.8 and 3.4 V (besides the 3 V used in Fig. 4). As can be seen, the ratios $\Delta J \div J_0$ are only weakly dependent on the sense voltage. This independence of $\Delta J \div J_0$ on the sensing voltage is further demonstrated in Fig. 7 for an n-FET with a gate oxide thickness of 4.5 nm in the voltage range

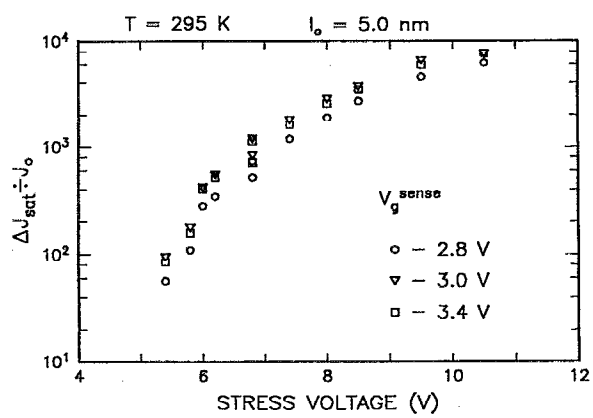

FIG. 6. Normalized SILC saturation magnitude as a function of FN stress voltage for sense voltages of 2.8, 3.0, and 3.4 V at room temperature. These values for the saturation levels were determined from the plateau regions of data similar to those in Fig. 4.

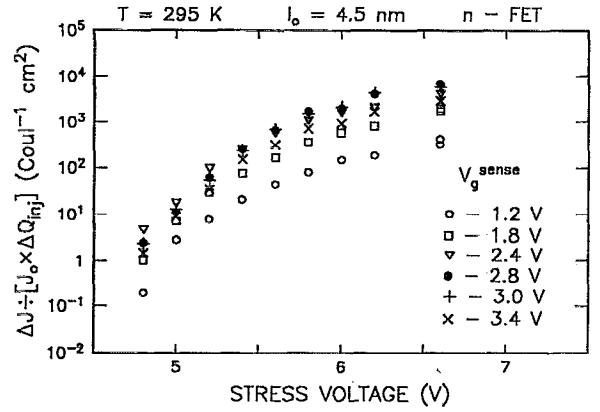

FIG. 7. Normalized SILC generation probability for various sense voltages throughout the direct tunneling regime from 1.2 to 3.4 V as a function of FN stress voltage. These probabilities were determined from SILC data at room temperature on n-channel FETs with gate oxide thickness of 4.5 nm.

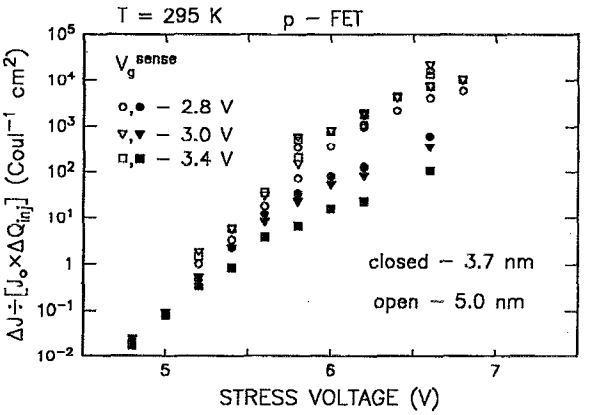

FIG. 9. Normalized SILC generation probability for p-channel FETs with varying gate oxide thickness of 3.7 and 5.0 nm as a function of FN stress voltage. These probabilities were determined from SILC data obtained with sensing voltages of 2.8, 3.0, and 3.4 V at room temperature.

from 1.2 to 3.4 V. Again, only small variations in the SILC generation probability are observed, except for the data obtained at a sense voltage of 1.2 V.

3. Oxide thickness and FET type

The effect on the SILC generation probability was studied over an oxide thickness range from 4.5 to 5.5 nm and 3.7 to 5.0 nm on n- and p-channel FETs, respectively. These data are shown in Figs. 8 and 9. No significant oxide thickness dependence is observed on the n-channel FETs (Fig. 8). However, a significant decrease (at least at larger stress voltages) in the probabilities is observed for the 3.7-nm-thick oxide p-channel FETs in Fig. 9 compared to those with gate oxides of 5 nm.

The other significant difference observed in comparing Fig. 8 (n-FETs) to Fig. 9 (p-FETs) is a shift to larger positive stress voltages to observe the SILCs on the p-FETs. As will be discussed next, this latter effect is due to differences in the effective cathode/oxide interfacial-energy barrier during FN stressing.[46]

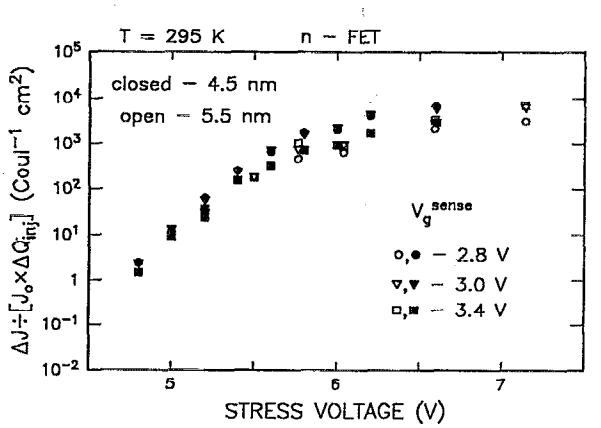

FIG. 8. Normalized SILC generation probability for n-channel FETs with varying gate oxide thickness of 4.5 and 5.5 nm as a function of FN stress voltage. These probabilities were determined from SILC data obtained with sensing voltages of 2.8, 3.0, and 3.4 V at room temperature.

4. Electron energy and gate polarity

It has previously been shown that the transport of hot electrons in oxide films for the thickness range studied here is ballistic or "near" ballistic.[6–8] The generation of SILCs can therefore easily be related to electron heating in the oxide layer because the energy which a ballistic electron (no phonon or impurity scattering) will have at the oxide/anode interface yields a good estimate for the average electron energy at this contact. This maximum kinetic energy E_{max} an electron can reach in the oxide before entering the anode contact can be calculated using the relationship

$$E_{max} = q[V_g - (\phi_{ms} + \psi_s) - \phi_b], \tag{1}$$

where q is the magnitude of the charge on an electron, ϕ_{ms} is the contact potential difference between the n^+-poly-Si gate electrode and the Si substrate, ψ_s is the Si surface potential at the substrate-Si/oxide interface, and ϕ_b is the potential barrier at the injecting cathode/oxide interface. For n- or p-channel FETs under positive voltage bias on the gate, $\phi_{ms} + \psi_s$ is ≈ 0, while for negative voltages the value is ≈ -1.3 V (Ref. 47).

The values of ϕ_b were determined from the Fowler–Nordheim IV characteristics by fitting these data to the well-known FN relationship given by

$$J_0^{FN} = AF^2 \exp(-B\phi_b^{3/2} \div F), \tag{2}$$

where J_0^{FN} is the FN current measured on a virgin as-fabricated structure, $F = (V_g - \phi_{ms} - \psi_s) \div t_0$ is the average field, and A and B are constants. The values for ϕ_b obtained for positive voltages were 2.9 V for the n-FET (electron injection from the inversion layer of the channel) and 3.2 V for the p-FET (electron injection from the accumulation layer of the n-type Si substrate). The lower-energy barrier obtained for the n-FET is due to the formation of subbands (lying above the bottom of the Si conduction band) created by the potential confinement of the channel electrons near the Si-substrate/oxide interface.[46,48] For negative-gate voltage on the p-FETs a value of 3.1 V was obtained. This latter value for ϕ_b corresponds to the voltage barrier at the n^+-poly-Si/oxide interface.

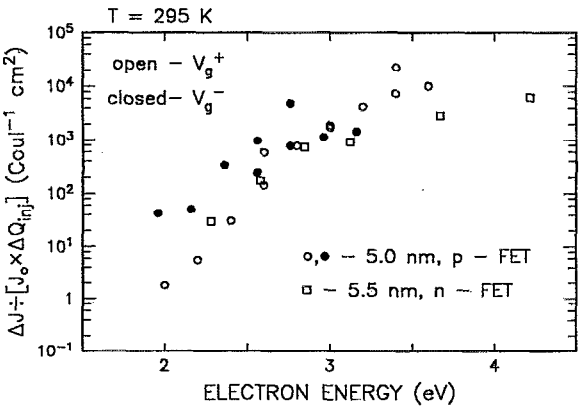

FIG. 10. Normalized SILC generation probability as a function of maximum hot-electron energy for various n- and p-channel FETs at both positive and negative FN stress voltages. Sense voltages were 3 and −4.3 V for positive- and negative-gate-polarity stressing, respectively, yielding equivalent voltage drops across the oxide layer. Some of these data were obtained from Figs. 8 and 9 for oxide thickness of 5.5 and 5.0 nm, respectively, at room temperature. This figure shows a hot electron threshold energy near 2 eV for the onset of the SILC phenomenon.

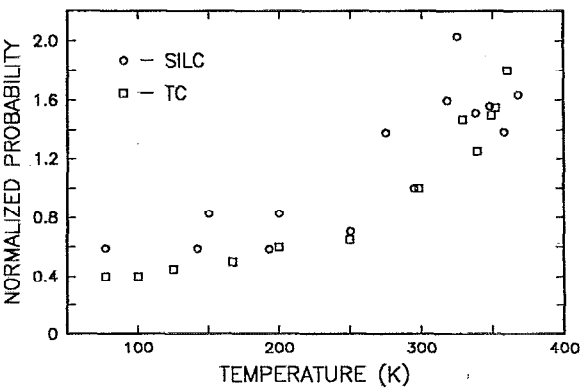

FIG. 11. Normalized SILC generation probability (open circles) and trap generation probability (open squares) as a function of temperature. For SILC measurements, n-channel FETs with gate oxide thickness of 4.5 nm, similar to those in Fig. 7, were used. For these FETs, both stressing (at 5.6 V) and sensing (at 2.8 V) were performed at the ambient temperature indicated. The electron trap creation probabilities were taken from Refs. 17 and 18. Both data sets are normalized to their room-temperature values for comparison.

Selected data from Fig. 5 to 9 have been plotted in Fig. 10 as a function of the maximum electron energy calculated via Eq. (1) and using the parameters determined above. The generation of SILCs in Fig. 10 show a threshold energy of ≈2 eV independent of voltage polarity, FET type (n or p channel), or oxide thickness in the range considered here. This energy threshold is the same as that observed for the trap creation phenomenon.[17] The fact that the SILCs do not depend significantly on oxide thickness shows that the electron energy can be calculated on the basis of quasiballistic transport[1,7] as done in Eq. (1). It also suggests that the release of the maximum energy near the anode/oxide interface is the controlling parameter, as was previously found for the trap creation phenomenon.[6,7] Similarly, the lack of a significant polarity dependence was previously observed for trap creation on poly-Si-gated structures where both interfaces are Si/SiO_2 (Refs. 17 and 26). The 2 eV threshold determined from Fig. 10 is not consistent with any threshold observed for hole generation and trapping. These thresholds are ≈9 eV for gap ionization[26,28,49–51] and ≈5 eV for anode hole injection[44] as will be discussed in a later section of this report.

5. Temperature

The temperature dependence of the SILC from 77 to 368 K was also studied and compared to that observed for trap creation (Fig. 11) or hole generation/trapping. Trap creation shows a temperature sensitivity above ≈200 K with an activation energy of about 200 meV.[17,18] However, hole generation/trapping (including any electron recombination) has a weak temperature dependence in comparison over the same range.[26] Figure 11 shows that SILCs have a temperature dependence similar to that for trap creation. Since both the stress and sense operations for SILCs can each have their own separate temperature dependence, the data in Fig. 11 (where all operations are performed at the same temperature) imply that the phenomenon producing the DT currents during the sensing operation must be weakly dependent on temperature. This is consistent with a trap-assisted tunneling process where the traps are generated by hot electrons.

B. Oxide charging and defects

From the previous discussions, the trap creation phenomenon seems to correlate well with SILCs in terms of the hot-electron energy required. However, during trap creation, many different defect sites with different processing dependencies from one wafer run to another can occur. These defects include interface states, generation-recombination centers in the Si substrate, neutral electron traps in the oxide bulk distributed away from the cathode/oxide interface, and positively charged oxide sites (mostly "slow states") near the anode/oxide interface.[16–28] Since all show the same hot-electron energy dependence with the 2 eV threshold characteristic of trap creation, it is not obvious which type or types of defects could be responsible for the SILC phenomenon. In this section, it will be shown that the neutral traps distributed away from the cathode/oxide interface correlate best with the SILCs, and that the mechanism producing the SILCs is probably due to trap-assisted tunneling through these sites.

First, it can be directly shown that the hot-electron energies required for the observation of the SILC phenomenon do not correlate with those required to generate holes in the SiO_2. Since the production and trapping of holes produced by band-gap impact ionization has been extensively discussed in previous publications and requires 9 eV (Refs. 26–28), it will not be considered further. However, anode hole injection (and trapping) requires less energy and can occur with thin oxide structures. This mode of trapped hole buildup will be reviewed here and be shown to require at least 5 eV of energy to be significant.[42] Thus, this latter form of hole production can also be ruled out in explanations for SILCs.

Using a combination of CV and It techniques for different gate polarities, the interface states and trapped oxide charges (both positive and negative) can be determined as a function of FN-injected electron fluence for various gate

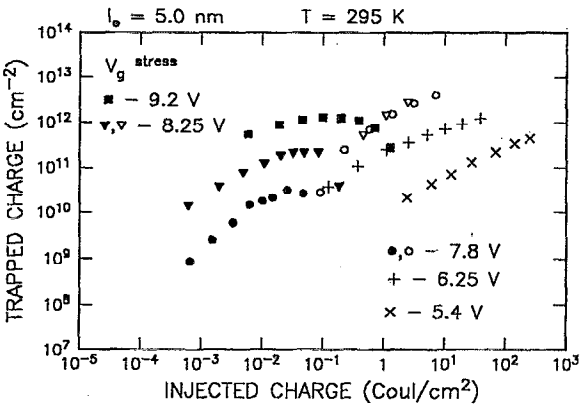

FIG. 12. Magnitude of trapped-charge buildup in 5.0-nm-thick oxide layers of p-channel FETs as a function of the FN-injected electronic-charge fluence for various applied-gate voltages at room temperature. An *as*-fabricated, virgin device was used for each voltage condition. *CV* tracking and *IV* techniques were used to determine the magnitude of the charge and spatial location. Solid symbols at low fluence represent the initial buildup of positively charged trapped holes, while open symbols represent a net negative-charge state of the oxide at larger fluence due to the additional generation and filling of neutral electron traps. The (+) and (×) symbols represent data for lower-voltage FN-injection conditions where only electron trapping is observed. The minimum detectability level here is $\approx 1\times10^9$ trapped charges/cm^2.

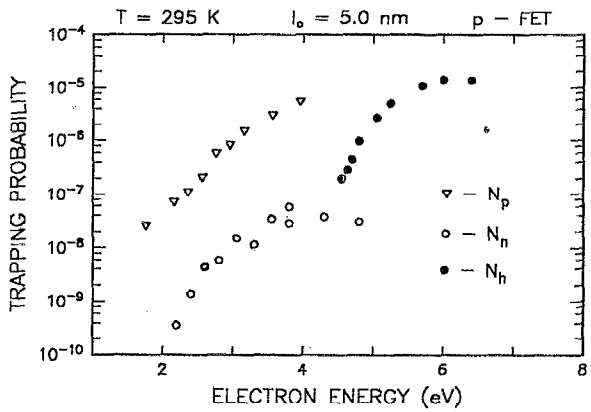

FIG. 13. Trapping probability for various charged defects in the gate oxide layer (5.0 nm in thickness) of p-channel FETs as a function of maximum hot-electron energy at room temperature. The trapping probabilities for electrons (N_n) and holes (N_h) were obtained from the slopes in the linear regions of the data in Fig. 12. The generation probabilities for the anode positive charge (N_p) were similarly determined from *CV* and *It* measurements at negative-gate voltages on these devices.

voltages (electron energies).[17,26] The *CV* technique senses the internal fields due to trapped charges up to the Si-substrate/oxide interface. An example of *CV* measurements used to sense the charge state of the oxide after FN stressing is shown in Fig. 12. These studies have been performed on devices similar to those used to obtain the SILC data. With increasing fluence, these data show a transition from a positive charge state of the oxide caused by hole trapping to a "net" negative charge state (caused mostly by trap creation). This type of characteristic has been discussed previously in structures with thicker oxide layers where most of the holes were produced by band-gap ionization.[26–28] The plateau regions for the positive charge buildup is due to a steady-state condition caused by the free-electron annihilation of trapped holes.[26–28] The negative charge state shown in Fig. 12 is the "net" sum of both the positive charges from the trapped hole steady-state condition, background electron trapping in as-fabricated sites (usually a small amount on thin films), and electron trapping in the mostly neutral traps generated during trap creation.[26–28] The interface state densities determined from the stretchout of the *hf-CV* characteristic of the devices[17] in Fig. 12 were small for this wafer set and are therefore not shown in the figure. The levels were largest after the onset of trap creation (near 1×10^{-2} C/cm^2) with values on the order of $\approx 1\times10^{10}$ interface-states/cm^2.

Similar studies to those in Fig. 12 were done using the *It* technique which uses the time dependence of the FN stress currents.[26] This technique also senses the internal fields due to trapped-charge buildup in real time. However, it is primarily sensitive to charges more than a tunneling distance ($\gtrsim$2 nm) from the cathode/oxide interface. Typically, *CV* measurements have been used in combination with *It* measurements to obtain information on the spatial distributions of trapped holes or electrons near the cathode-oxide interface. For the case shown in Fig. 12 where generated interface-state densities are small, the *It* measurements gave similar values for the density of trapped holes and/or negative charges as those determined from *CV* measurements (Ref. 26). This implies that most of the trapped-charge buildup was distributed away from the cathode/oxide interface.

The *CV-It* comparison also gives information on lateral nonuniformities in the trapped-charge distribution and on charge loss. *It* measurements are more sensitive to LNUs than *CV* measurements because of the exponential dependence of the tunneling current on the internal electric field near the cathode as shown by Eq. (2). With the presence of LNUs, *It* measurements give significantly larger values for the trapped-charge density compared to those determined from the *CV* measurements.[26,29] A similar situation occurs (comparing *It* and *CV* results) if there is any charge loss between the FN stressing pulse (during which the current transient measurement is done) and the *CV* measurements performed seconds afterward. Neither of these latter two effects (LNUs or charge loss) were significant for the results discussed here.

As done with previous data manipulation for the SILCs (see Sec. III A 2), the trapped charge verses fluence data have been converted into the trapping/generation probabilities verses electron energy shown in Fig. 13. These trapping/generation probabilities (number of trapped charges per injected electron) were determined from the slopes of data like that in Fig. 12 in the linear region at low fluence. For each type of trapped charge considered here (electrons, holes, and anode positive charges), the slopes were determined from the charging characteristics for each stress voltage condition. The stress voltages were converted into electron energies via Eq. (1) using the parameters determined in Sec. III A 4. These probabilities shown in Fig. 13 include those for holes, electrons, and positively charged sites near the anode.

As can be seen from Fig. 13, hole trapping (therefore generation) can only be detected in thin oxides at electron energies greater than $\approx$5 eV (or $V_g^{\text{stress}} \approx 8$ V, see Sec.

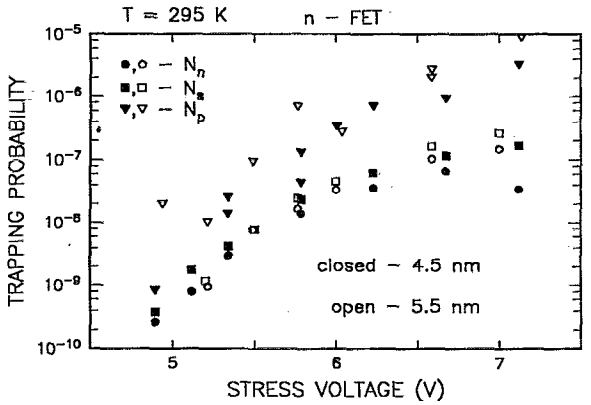

FIG. 14. Trapping/generation probability for various charged defects in the gate oxide layer (4.5 and 5.5 nm in thickness) of n-channel FETs as a function of FN stress voltage at room temperature. These probabilities for electron trapping (N_n), interface-state formation (N_s), and anode positive-charge generation (N_p) were obtained from the slopes in the linear regions of data similar to that in Fig. 12.

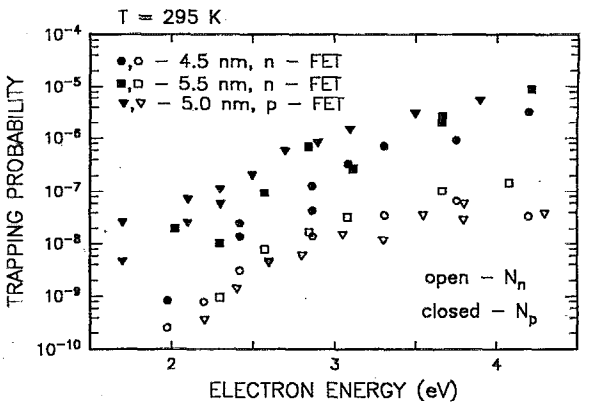

FIG. 15. Trapping probability for generated neutral-electron traps (N_n) and anode positive charge (N_p) as a function of maximum hot-electron energy for various p- and n-channel FETs with gate oxide thickness varying from 4.5 to 5.5 nm at room temperature. These probabilities were obtained from selected data from Figs. 13 and 14. The generation of both types of defects show a threshold near 2 eV, consistent with the trap creation phenomenon.

III A 4). Since SILCs appear at electron energies of ≈2 eV (see Fig. 10), hole generation/trapping by any mechanism will not be considered further.

The two other forms of charge buildup shown in Fig. 13 are characteristic of the trap creation phenomenon. The first, as shown in Fig. 12, is due to the negative-charge buildup in the neutral electron traps distributed away from the cathode/oxide interface. The second form of charge buildup is due to positively charged donor-like "slow" states created in the SiO_2 near the anode/oxide interface.[26] These could be the remnant defects produced by hot-electron "cracking" of hydrogen-decorated sites near the anode. As compared to the observation for trapped electrons and holes on these p-FET devices, the positive charges could only be observed under negative-gate voltage stressing where the anode interface is the substrate-Si/oxide surface.[26] Both the trapped electrons and the positively charged sites show approximately the same 2 eV threshold (≈5 V of stress voltage dropped across the SiO_2) characteristic of trap creation.

Comparing generation of SILCs in Fig. 10 to the charge generation in Fig. 13, a strong similarity in the energy dependence is observed, suggesting that the trap creation phenomenon is important in understanding the SILCs. However from the 5-nm-thick oxide p-FET data shown in Fig. 13 and the previous discussions, it is not obvious which defect component or components (interface states, distributed neutral-electron traps, or positively charged sites near the anode) control the SILCs.

To reduce the possibilities, the defect generation due to trap creation was compared to the SILCs for two different wafer sets fabricated about ten years apart using different Si-processing technologies. Figure 14 shows the trapping/generation probabilities for interface states, distributed electron traps, and anode positive charges measured in the more current n-FET wafer series. For direct comparison, the trapping/generation probabilities for the neutral electron traps (distributed away from the cathode) and for the positively charged sites (found near the anode) for the two wafer sets are compared in Fig. 15 as a function of electron energy. These data were obtained from Figs. 13 and 14 for the p-FETs and n-FETs devices, respectively. The data for the n-FETs in Figs. 14 and 15 show significant differences as compared to the p-FET data in Figs. 13 and 15. Particularly, the interface states and positively charged states near the anode differ in their density and/or location in the oxide.

The generation probabilities for the interface states at the Si-substrate/oxide interface for the n-FETs are much larger than those observed for the p-FETs. These interface-state-generation probabilities for the n-FETs as shown in Fig. 14 are comparable to those for electron trapping. However, as discussed earlier in this section, the number of interface states generated on the p-FETs was so small ($\lesssim 1\times10^{10}$ cm^{-2}) over the same fluence and stress voltage ranges that a generation probability could not be easily determined. If the SILCs were due to interface states, a comparably large difference in the SILCs between the two wafer sets would be expected. This is not observed (see Fig. 10), and these defect sites will not be considered further as having a significant influence on the SILCs.

The generation/trapping probabilities for the anode positive charge also show significant differences between the two wafer sets. Its buildup shows a larger asymmetry for different polarities. For example, as previously discussed, charges near the poly-Si/oxide interface could not be detected by It sensing in significant numbers for the p-FETs during positive-gate voltage FN stressing. The data shown in Fig. 15 for positive charging on the p-FETs were after negative-gate voltage stressing only. As compared to the p-FET results, positive charges for the n-FETs could be measured near the poly-Si-gate/oxide interface using It sensing with positive-gate voltages. This implies either a large number of sites, a centroid further from the poly-Si/oxide interface, or both. The positively charged defects near the anode could enhance the tunneling currents either by acting as sites that the tunneling carriers could move to before entering the anode and/or by distorting the energy barrier for the direct tunneling process, thereby enhancing the electron flow from the cathode to the anode. If the SILCs are due to a trap-assisted

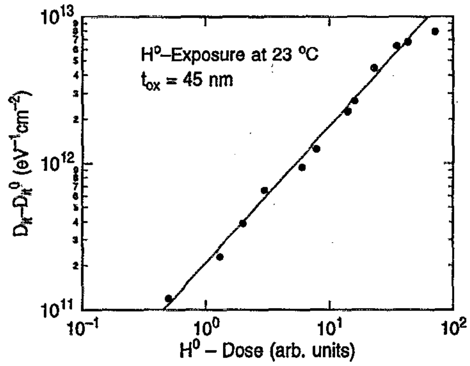

FIG. 16. Interface-state increase at mid-gap energy of the Si substrate, $D_{it}-D_{it}^0$, as a function of atomic hydrogen exposure at room temperature for a 45-nm-thick thermal oxide.

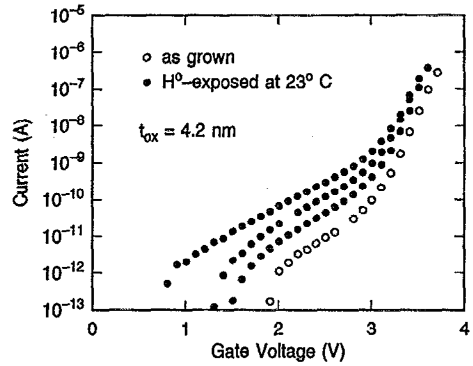

FIG. 17. Current-voltage characteristics of Al-gate capacitors with 4.2-nm-thick thermal oxides before (open circles) and after (solid circles) exposure to a remote hydrogen plasma. The leakage current in the direct tunneling regime (below 3 V) increases with increasing hydrogen dose. For each hydrogen exposure, a fresh oxide was used.

tunneling phenomenon, it would be expected that sites closer to the cathode would be more significant. Similarly, a stronger enhancement of the direct tunneling current due to field distortions would be expected for defects distributed further into the oxide. This is not observed for the SILCs measured on different wafer sets (see Fig. 10), suggesting that the anode positive charge is not its dominant cause.

The trapping/generation probabilities for the neutral sites in Fig. 15 are not only independent of oxide thickness and wafer set (n- or p-FETs), but also can be observed with a similar magnitude for either positive (as shown in this figure) or negative-gate voltage stressing.[17,26] Since the SILC generation probabilities shown in Fig. 10 had no significant polarity dependence (especially, for the p-FETs), it seems likely for the cases studied here that the neutral-electron traps generated by the trap creation phenomenon are the most important defect state responsible for the SILCs. The fact that the neutral-electron traps are distributed away from the cathode[17] also supports their importance.

For oxides $\lesssim 4$ nm, a significant decrease in generated neutral trap density was observed. This result could be in part due to less electron occupation of the sites. (Trapped electrons could tunnel directly to empty states in the contacts which are $\lesssim 2$ nm away.) However, this reduction in neutral-electron traps sensed by CV and It techniques is consistent with the corresponding reduction in SILC shown by the data in Fig. 9 for the 3.7-nm-thick oxides. This implies a reduction in the number of defects produced by the trap creation phenomenon.

C. Remote hydrogen plasma exposure

The electrical measurements reported above suggest that the release of hydrogen and its high chemical reactivity are predominantly responsible for the generation of the defects which give rise to SILCs. Independent evidence for the high reactivity of atomic hydrogen in the Si/SiO_2 interfacial region at room temperature has been provided by exposure of gate oxides to atomic hydrogen in a remote plasma.[36–40] These experiments showed that atomic hydrogen easily diffuses through thermal oxides and efficiently produces fast interface states and positively charged slow states. This is illustrated in Fig. 16 where the number of generated interface states was found to be proportional to the hydrogen fluence at the oxide surface, and the maximum number of these interface states exceed the highest numbers typically reported in electrical measurements on samples with poly-Si-gate processing. This is consistent with the finding that the trap creation process is likely limited by hydrogen release and not by the reaction in the interfacial region.[17,18]

In Fig. 17, current-voltage characteristics of Al-gate capacitors with 4.2-nm-thick oxides are shown after exposure to a remote hydrogen plasma at room temperature. With increasing hydrogen dose, an increase in the direct tunneling current is observed which is quite similar to that observed after high-field stress, as can be seen by comparing Fig. 17 with Fig. 3. In Fig. 18, the hydrogen-induced leakage currents in the direct tunneling regime (measured at 3.2 V) as a function of hydrogen dose are compared for different oxide thickness of 3.5, 4.2, and 5.2 nm. For each data point in Fig. 18, a new sample had to be used for reasons discussed in Sec. II B. The accuracy of these measurements is limited by variations in the hydrogen dose, the area of the capacitors, the oxide thickness across a wafer, the time between exposure and current measurement (some relaxation of the

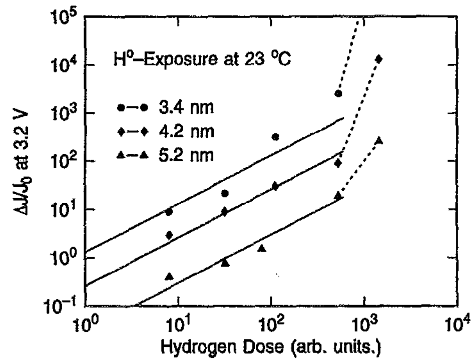

FIG. 18. Leakage current in the direct tunneling regime (measured at 3.2 V) in 3.4, 4.2, and 5.2-nm-thick thermal oxides as a function of the atomic hydrogen dose in a remote plasma. Aluminum gates were deposited after exposure. A fresh sample was used for each data point. The solid lines represent a linear dependence of the normalized current increase on hydrogen dose.

hydrogen-induced damage occurs), and the initial value of the DT currents. Within the limited accuracy of the data, the leakage currents initially increase in proportion to the hydrogen dose. This observation provides strong independent support for the correlation between "trap creation" and SILC generation suggested by the electrical measurements. At higher dose, a more rapid increase was observed. This fast degradation appears to be more severe in thinner oxides. Very large hydrogen exposures may induce weak spots in the oxide. This speculation is supported by the observation, that the capacitor yield after exposure and metal deposition rapidly decreases at these high doses. Many capacitors are partial shorts. Also, the breakdown voltage during voltage ramp measurements was found to decrease after heavy exposures. It seems that the unlimited supply of hydrogen in the plasma experiments continuously damages the interfacial regions, ultimately causing breakdown. The amount of hydrogen that can be released by hot electrons in the poly-Si-gate FETs is known to be limited, likely delaying such drastic degradation.

Atomic hydrogen is known to etch oxides and silicon at high temperatures. If this also happens at room temperature, the enhanced leakage currents might simply be due to oxide thinning. However, no homogeneous decrease in oxide thickness could be measured by ellipsometry even at the largest exposures used in this study. With such measurements, hydrogen exposure was found to cause an apparent increase in the oxide thickness at constant refractive index. This was probably caused by enhanced water adsorption on exposed samples. Using multireflection infrared spectroscopy, atomic hydrogen exposure at room temperature was observed to remove surface impurities (such as hydrocarbons) which may in turn enhance the water adhesion. This was verified by driving off adsorbed water by annealing in dry nitrogen at 200 °C for 5 mins. After annealing, identical oxide thicknesses were measured for as-grown and exposed samples. Therefore, the enhanced leakage currents and the enhanced breakdown discussed above cannot be attributed to homogeneous thinning of the gate oxide. It can, however, not be excluded that some microscopic spots might be attacked more easily by atomic hydrogen.

The DT-current response to hydrogen-induced damage differs in two other aspects from the response to high-field stress. The normalized leakage currents caused by atomic hydrogen depend on oxide thickness (see Fig. 18). A similar thickness dependence has also been observed for the interface-state degradation during hydrogen exposure.[36] This was qualitatively explained within a diffusion-reaction model which allows a larger hydrogen flux into the interfacial region in thin oxides. Such a dependence does not exist during electrical stress (see Sec. III A *3*) probably because the degradation observed here is limited by the hydrogen release from near the anode/oxide interface.[17,18]

Also, the generation of distributed bulk-oxide electron traps during atomic hydrogen exposure has not been systematically studied yet. Qualitatively, hydrogen exposed samples show a defect distribution which resembles that of electrically stressed oxide structures with Al gates which typically have much larger hydrogen concentrations than poly-Si-gate structures.[22,41] Since high densities of positively charged slow states are produced in such structures, the generated electron traps cannot be measured as accurately as on structures with poly-Si gates.

IV. DISCUSSION AND CONCLUSIONS

These studies have directly shown the relationship of SILCs to the trap creation phenomenon. They also show the relationship of the addition of a few traps to current leakage through thin insulators. Explanations for SILC involving trapped holes (at least for oxide voltage drops of less than $\approx$8 V) or LNUs are not plausible from these studies. Also, the most significant component contributing to the SILC in the experiments discussed here appears to be due to the generation of the neutral-electron traps, not the interface states and/or anode positive charge. However, for other experimental situations such as the hydrogen experiments discussed here or different oxide processing conditions, these latter two classes of defects could be as important.

Some of the SILC results discussed earlier can now be reviewed again in terms of enhancements caused by the generated traps. From Fig. 7, the lack of any significant dependence on sense voltage for the normalized SILC generation probability until $\approx$1.2 V implies that most of the traps that carry this excess current are "distributed" energetically and spatially in the SiO_2. This interpretation is consistent with past studies of the generated neutral-electron traps which were found to be nonmonoenergetic and distributed spatially away from the cathode/oxide interface.[16–28] In Fig. 10, the lack of a significant dependence on stress/sense polarity for the normalized SILC generation probability suggests that similar distributions of traps are generated during stress and carry the current away from the cathode/oxide interface during sensing. This latter interpretation is also consistent with similar observations for the polarity dependence of the generated neutral-electron traps on similar poly-Si-gated structures.[17,26]

The observation of a saturation in the SILCs (Fig. 4) and the weak dependence of the saturation level on stress voltage or electron energy (Fig. 6) is also consistent with the presence of generated neutral traps. The saturation regions can be caused by limiting the number of available empty traps that can carry the tunneling current and/or by barrier distortions caused by the trapped electrons. As these sites are generated by the hot electrons during FN stress, some sites will capture electrons as shown in Fig. 12. The saturation regions in the data for the SILCs (see Fig. 4) start to form at injected charge fluence where significant trapped-electron buildup has occurred in the generated neutral sites (see Fig. 12).[26] Any factor effecting the number of sites generated during stress and their electron occupancy should subsequently effect the SILCs during the sense measurements that follow. With increasing stress voltage, neutral site generation still continues to increase slowly in the region of injected charge fluence where the SILCs have saturated (compared Figs. 4 and 12). Possibly, the current increase due to fewer generated sites can be compensated by the field distortions caused by the trapped electrons. (As shown in Fig. 1, negative oxide charge produces a larger tunneling barrier and can energetically

change the accessibility of empty oxide sites to carriers tunneling from the contacts.) Additionally, the electron occupancy of the generated sites will decrease with increasing electric field.[26] This may contribute to the increase of the saturation level observed with increasing gate voltage (electric field) shown in Fig. 6.

Similar arguments for explaining any of the SILC results discussed above can also be made for the anode positive charges generated during trap creation. The positive charges can act as "stepping" stones for the electrons. Additionally, they can distort and lower the tunneling barrier. However, since most of this charge is near the anode,[26] it would not be expected to have as large an effect on electrons tunneling from the cathode. If these sites are "slow" donor-like states as thought by some researchers,[26,41] their occupancy by electrons would decrease at higher FN stress voltages. Electron capture on any of these positive charges during the sensing measurements would compensate distortions in the tunneling barrier and decrease the DT currents.

At large stress voltages where hole injection and trapping can be observed, the tunnel barrier will also be distorted by the presence of this positive charge [see Fig. 1(d)]. This may cause an enhancement of the SILCs (for example, in the data in Fig. 4 at $V_g^{\text{stress}} \gtrsim 7.8$ V) similar to that reported for thick oxides in the FN-tunneling regime.[26] Such distortions in the tunneling barrier may increase not only the direct tunneling current but also the trap-assisted tunneling current. The turn-around effect (decrease in the DT current) in Fig. 4 at large stress voltages and fluence may be indicative of this phenomenon since significant electron trapping can be shown to compensate the trapped holes (see Fig. 12) and thereby reduce the barrier distortions caused by their presence.

The effect of the generation of neutral-electron traps on the generation of SILC, can be quantified by comparing the data in Fig. 10 and Fig. 15. This comparison yields a linear relationship,

$$(\Delta J \div J_0)/\Delta N_n \approx 8\times 10^{-9}\ \text{cm}^2 \tag{3}$$

averaging over the full range of energies shown in these figures. The value of the proportionality constant reveals a very strong dependence of the SILC on the oxide trap density. For example, an increase in ΔN_n of 1×10^{10} traps/cm^2 (typically the lowest levels measurable with conventional CV techniques) will give a factor of 80 increase in the direct tunneling current. The number deduced from Eq. (3) is an upper limit, since the data used from Fig. 15 has no corrections for trap occupancy or generation rate. The trap occupancy at the fields used here would be expected to be less than 50% of the total number of available sites. Also since the techniques used here sense the trapped charge and not directly the trap generation, the generation probability could be larger if the observations are limited by the electron trapping probability. However, this latter possibility is not expected from previous studies.[17] Also as discussed previously, the anode positive charge which has not been considered in these calculations could have an effect on these results.

Since so few neutral trapping sites (or positive bulk oxide charges) can cause such a large increase in the direct tunneling current, future processing technologies for thin insulators would have to be tightly controlled from wafer run to wafer run. Reproducible leakage currents in thin oxides could be a major challenge in pushing silicon-based technologies to even denser memories requiring very thin insulators. A current example where as-fabricated neutral-electron traps and positive charges introduced during processing could produce larger leakage currents would be for reoxidized-nitrided films which will be discussed below.

An example where trap creation at high fields and the resulting SILCs limit device performance and memory retention is for nonvolatile memories such as the electrically erasable and programmable read-only-memory (EEPROM). Many of these types of structures have floating poly-Si gates that are used for charge storage. The electrons stored on these floating gates can leak off through any of the surrounding insulator layers in time, thereby perturbing the information stored and limiting the charge retention of the device. As these memories are made smaller, the surrounding insulators must also be decreased in thickness and charge loss due to direct tunneling becomes a major issue, particularly for oxide thickness less than 5.0 nm (Ref. 14). If the thin oxide layer between the Si substrate and floating poly-Si layer is used for charge transfer when the memory is written or erased, the device will have accelerated retention degradation due to the SILC phenomenon caused by trap creation for oxide-voltage drops over 5 V.

Although nitrided oxides have been increasingly explored as a alternate gate insulator to SiO_2, these materials could have more leakage current at low fields. As-fabricated nitrided oxides have greater numbers of energetically shallow traps than SiO_2,[19] and therefore the occurrence of larger direct tunneling currents are possible as the insulator is made thinner. Barrier lowering or distortion due to the presence of nitrogen in the film could also add to this tunneling current.[19] The occurrence of positive charges in the films, observed under most processing conditions, could also create similar increases in the currents.[19]

However, nitrided oxides can also lower trap creation rates by as much as an order of magnitude compared to SiO_2 (Ref. 19). This reduction is believed to be due the ability of the oxynitride regions to act as blocking or scavenging barriers to hydrogen after liberation by the hot electrons.[19,35] Since the as-fabricated traps in these films are mostly unoccupied at the large fields[19] used for writing or erasing these memories, more cyclability can be obtained than in structures using stoichiometric SiO_2. Therefore in nonvolatile memories, the nitrided-oxide materials would be expected to give a tradeoff between decreases in retention (due to an increase in the number of as-fabricated traps, positive charges, and the nitrogen content of the film itself) and increases in the number of write/erase operations (due to a reduction in trap creation).

ACKNOWLEDGMENTS

The author wishes to acknowledge the experimental assistance of G. Singco and critical reading of this manuscript by T. N. Theis, J. H. Stathis, and D. A. Buchanan.

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