Carrier-selective interlayer materials for silicon solar cell contacts

Muyu Xue,[1,2,a)] Raisul Islam,[2,a)] Yusi Chen,[2,a)] Junyan Chen,[3] Ching-Ying Lu,[2] A. Mitchell Pleus,[2] Christian Tae,[2] Ke Xu,[2] Yi Liu,[2] Theodore I. Kamins,[2] Krishna C. Saraswat,[1,2] and James S. Harris[1,2]

[1]*Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA*
[2]*Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA*
[3]*School of Physics, Peking University, Beijing 100871, China*

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This work presents titanium oxide (TiO_x) and nickel oxide (NiO_x) as promising carrier-selective interlayer materials for metal-interlayer–semiconductor contacts for silicon solar cells. The electron-conducting, hole-blocking behavior of TiO_x and the opposite carrier-selective behavior of NiO_x are investigated using the transmission-line-method. The Fermi level depinning effect and the tunneling resistance are demonstrated to be dependent on the interlayer oxide thickness and annealing temperature. NiO_x is furthermore experimentally demonstrated to be capable of improving the effective minority carrier lifetime by quasi-steady-state photoconductance method. Our study demonstrates that TiO_x and NiO_x can be effective carrier-selective materials for Si solar cells and provides a framework for characterizing carrier-selective contacts. *Published by AIP Publishing.* https://doi.org/10.1063/1.5020056

I. INTRODUCTION

The learning curve for photovoltaics predicts that the price of solar photovoltaic modules tends to drop 20% for every doubling of the cumulative shipped volume.[1] In the crystalline Si photovoltaic market, material cost accounts for 57% of the total module cost.[2] The use of thin film solar cells can help the continuation of price reduction by reducing the material cost and also allowing repeated using of the substrate. However, with the decreasing of cell thickness, contact recombination becomes a major concern due to the dangling bonds and the midgap defect states at the metal–silicon (MS) interface.[3–5] Moreover, metal/Si contacts suffer from the Fermi level pinning effect,[6] resulting in a high barrier for both the majority and minority carriers, which further increases the contact recombination. Such problems can be solved by forming metal-interlayer–semiconductor (MIS) carrier-selective contacts: by inserting a specific interlayer material, a large barrier is formed for the minority carriers and a reduced barrier for the majority carriers by depinning the Fermi level,[7,8] resulting in a reduction of contact recombination. For electrons, titanium oxide (TiO_x) has been reported to effectively reduce the contact recombination by forming a metal/TiO_x/n-Si structure.[9–14] For holes, PEDOT:PSS has been demonstrated as an effective hole-selective contact layer for organic solar cells[15–19] and shows compatibility with silicon heterojunction solar cells.[16,17] On the other hand, for an inorganic material system, nickel oxide (NiO_x) has also been proposed as an electron-blocking interlayer material.[20] However, a systematic experimental study has not been done to analyze and optimize the TiO_x and NiO_x MIS contacts.

The typical energy band diagrams of Al/TiO_x/n-Si, Pt/NiO_x/p-Si and the corresponding MS contacts (without oxide interlayer) are shown in Fig. 1. For MS contacts, the energy barrier Φ_B for majority carriers is high due to the Fermi level pinning effect, which also suffers from high contact recombination due to available energy states at metal–Si interface, as shown in Figs. 1(a) and 1(b). When carrier-selective interlayers are introduced, the Fermi levels at the metal–Si interface are depinned, achieving the band structures in Figs. 1(c) and 1(d). For the TiO_x/Si heterostructure, small conduction band offset ($\Delta Ec < 0.2\,eV$) and large valence band offset ($\Delta Ev > 2\,eV$) can be achieved. The NiO_x/Si heterostructure has the opposite band alignment, a low $\Delta Ev < 0.3\,eV$ (Ref. 20) and a high $\Delta Ec > 2\,eV$. In both cases, Figs. 1(c) and 1(d), the transport of majority carriers is enhanced; however, minority carriers are blocked at the contact. Furthermore, for majority carriers, both the depinning effect (barrier reduction) and tunneling resistance are affected by the interlayer material thickness. Therefore, contact resistivity ρ_c of these contact structures from both experiment and simulation was analyzed to study the majority carrier transport.

In this work, we use transmission-line-measurements (TLM) to extract contact resistivity ρ_c for different contact structures and show that TiO_x acts as an electron-selective/hole-blocking material and NiO_x with the opposite carrier selectivity. These contact structures are characterized by different annealing temperature for different interlayer thicknesses. By comparing the ρ_c of the MIS contacts with those of the corresponding MS contacts without interlayer (control), we observe an improved carrier selectivity from the asymmetry in the ρ_c of the majority and the minority carriers. Such an asymmetric behavior determines the carrier selectivity of contacts. According to this metric, we conclude that TiO_x and NiO_x can be effective carrier-selective interlayer materials for thin film Si solar cells to suppress the contact recombination.

II. TRANSMISSION LINE MEASUREMENTS

A. TLM design and device fabrication

To test the carrier-selective properties for both TiO_x and NiO_x, four types of TLM contact structures were fabricated,

[a)]M. Xue, R. Islam, and Y. Chen contributed equally to this work.

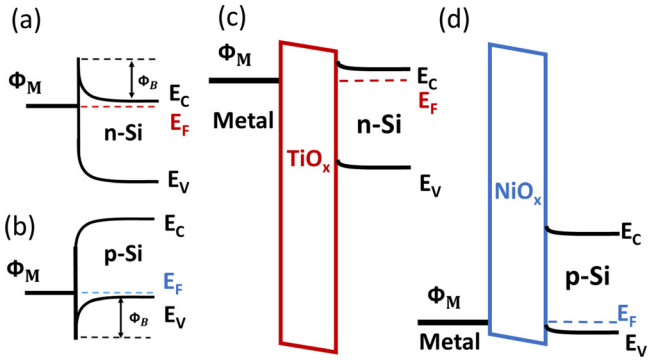

FIG. 1. Band alignment of MS junction (a) Al/n-Si, (b) Pt/p-Si and MIS junction, (c) Al/TiO_x/n-Si, and (d) Pt/NiO_x/p-Si.

as shown in Fig. 2. For TiO_x, Al/TiO_x/n-Si and Al/TiO_x/p-Si were fabricated to verify the electron-conducting and hole-blocking behavior, respectively. The corresponding control structure, Al/n-Si and Al/p-Si were also fabricated for comparison. Similarly, for NiO_x, Pt/NiO_x/p-Si and Pt/NiO_x/n-Si were fabricated to verify the hole-conducting and electron-blocking behavior, respectively, together with the Pt/p-Si and Pt/n-Si control structures. Epitaxial Si layers are grown on (100) oriented silicon substrate (with opposite doping type) by reduced-pressure chemical-vapor-deposition (RPCVD) at 1000 °C using dichlorosilane as precursor. Phosphorus (from PH_3) and boron (from B_2H_6) were used as n-type and p-type dopants, respectively. The epitaxial Si layer is 100 nm thick with the target doping level (both n-type and p-type) of 1×10^{19} cm^{-3}. The target sheet resistance for the epitaxial n-Si and p-Si is 330 Ω sq^{-1} and 530 Ω sq^{-1}, respectively. The TLM region is then defined by standard photolithography followed by reactive-ion-etching to form the TLM mesa region.

The TiO_x film is thermally grown at 200 °C using a Cambridge Nanotech Savannah atomic layer deposition (ALD) system, using Tetrakis(dimethylamido)titanium and H_2O as precursors. The NiO_x film was deposited by RF magnetron sputtering in oxygen (5 sccm flow) and Ar (45 sccm flow) ambient from a NiO_x target at a pressure of 3 mTorr.

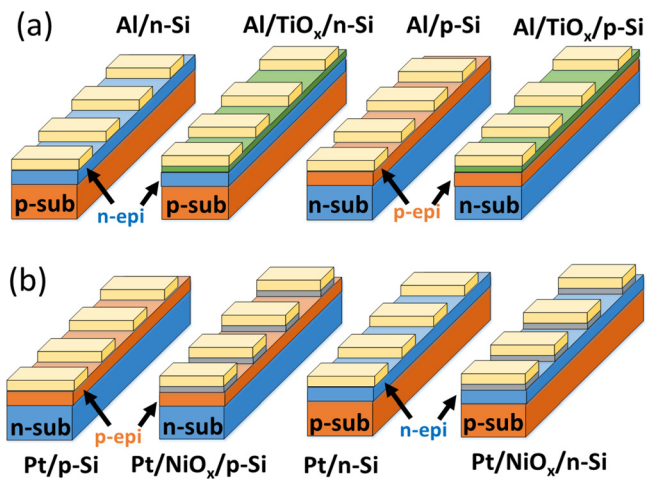

FIG. 2. Schematic of different TLM structures: (a) TiO_x and (b) NiO_x for verifying carrier-selective properties.

The metal contact region is defined by photolithography followed by metal deposition and lift-off. Rapid-thermal-annealing at different temperatures in forming gas (5% $H_2 + 95\%N_2$) is done after the device fabrication. Forming gas annealing of the contact structures is important in this study to help reduce the contact resistivity by improving the oxide–Si interface quality[13,21] and cause a related phase change of the oxide, as will be discussed in detail in this study.

The ρ_c is extracted from the TLM structure, as illustrated in Fig. 3. The linear I-V characteristics in Fig. 3(a) indicate ohmic behavior for the majority carriers due to low Φ_B, and the ρ_c is then extracted from the resistance (slope of V-I curve) according to multiple metal contact distances: 10 μm, 20 μm, …, 100 μm. For the other case, we also observe non-linear I-V characteristics shown in Fig. 3(b), indicating typical Schottky behavior due to high Φ_B or high resistance. This I-V characteristic is referred to as "non-ohmic" and the corresponding ρ_c is labeled as "infinite" (effective $\rho_c > 10$ mΩ cm^2) in this study.

B. TiO_x contacts results and discussion

The ρ_c extracted from the four kinds of TLM structures, Al/n-Si (red), Al/TiO_x/n-Si (blue), Al/p-Si (yellow), and Al/TiO_x/p-Si (green), for different annealing temperature are shown in Fig. 4(a). In these structures, the TiO_x thickness is 6 nm.

As shown in Fig. 4(a), low ρ_c (<0.6 mΩ cm^2) is obtained for both non-annealed and annealed Al/n-Si MS control structures, indicating good ohmic contacts. Because the TiO_x layer is deposited by the ALD process, the Al/TiO_x/n-Si structure without annealing cannot form an ohmic contact due to the native silicon oxide SiO_x existing at the TiO_x–Si interface.[21] However, the Al/TiO_x/n-Si contacts become ohmic and have lower ρ_c than the Al/n-Si MS control structure when annealed between 300 °C and 450 °C. This indicates that the Φ_B is reduced for electrons when TiO_x is introduced. This change can be attributed to the TiO_x film changing from amorphous as-deposited to anatase phase when annealed above 250 °C[22]) and improvement of the interface quality after annealing.

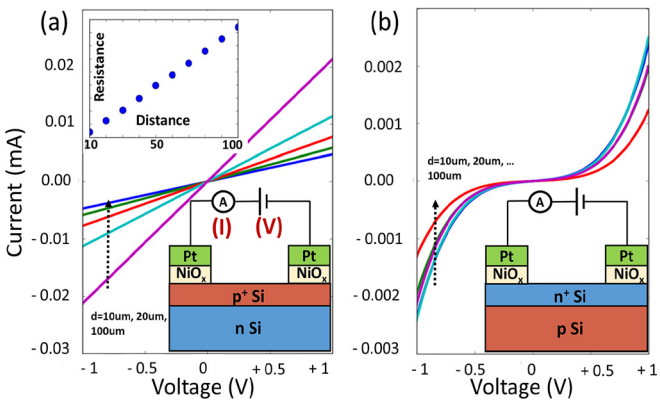

FIG. 3. Two kinds of I-V characteristics from the TLM measurement. (a) ohmic contact (linear) and (b) non-ohmic contact (non-linear).

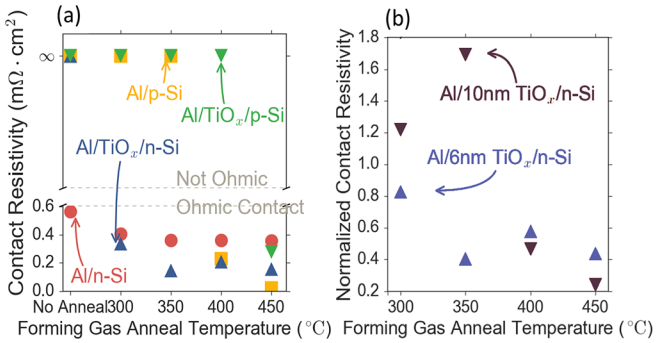

FIG. 4. (a) ρ_c for 6 nm TiO_x TLM structures, (b) normalized ρ_c of Al/TiO_x/n-Si for TiO_x = 6 nm and 10 nm, respectively.

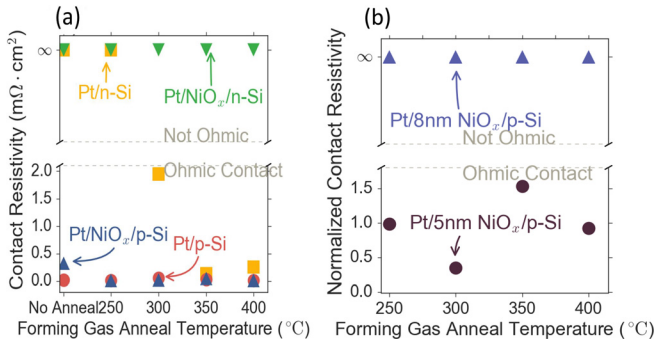

FIG. 5. (a) ρ_c for 5 nm NiO_x TLM structures, (b) normalized ρ_c of Pt/NiO_x/p-Si for NiO_x = 5 nm and 8 nm, respectively.

For holes, the as-deposited Al/TiO_x/p-Si structure does not form an ohmic contact. This contact system does not form an ohmic contact even when annealed at a temperature as high as 400 °C, showing different behavior than the Al/TiO_x/n-Si structure. This shows that the TiO_x blocks holes because of the high ΔE_V with Si. The Al/TiO_x/p-Si contact becomes ohmic only when annealed above 400 °C. This is possibly due to the formation of rutile TiO_x at an annealing temperature above 400 °C,[22,23] and also to Al-TiO_x interdiffusion under such high annealing temperatures[24,25] due to high oxygen affinity of Al relative to Ti, which degrades the TiO_x carrier selectivity.

Furthermore, to evaluate the ρ_c dependence on the TiO_x thickness, Al/TiO_x/n-Si TLM structure with 10 nm thick TiO_x was fabricated to compare with the 6 nm case. To minimize the effect of process variations associated with different batches of fabrication, the "normalized ρ_c" is defined: the contact resistivity ratio of Al/TiO_x/n-Si to the corresponding control structure Al/n-Si, which is fabricated in the same processing batch. (Similar to Pt/NiO_x/p-Si and Pt/p-Si discussed later). The normalized Al/TiO_x/n-Si ρ_c with 6 nm and 10 nm thick TiO_x interlayers is shown in Fig. 4(b). The device having 10 nm TiO_x has comparable contact resistivity to the device having 6 nm TiO_x when annealed above 350 °C. This can be due to the excess doping in TiO_x due to the oxygen vacancy creation by the forming gas anneal:[13,24] extra oxygen vacancies are generated as result of the relative higher oxygen affinity of Al than Ti, and also the reducing effect of H_2. Both effects result in higher conductivity of the TiO_x layer.

C. NiO_x contacts results and discussion

Similarly, for NiO_x, the ρ_c extracted from the TLM structures of Pt/p-Si (red), Pt/NiO_x/p-Si (blue), Pt/n-Si (yellow), and Pt/NiO_x/n-Si (green) as a function of annealing temperature is shown in Fig. 5(a), where NiO_x thickness is 5 nm.

As shown in Fig. 5(a), for Pt/p-Si control structure, low ρ_c (<0.5 mΩ cm^2) is obtained for both with and without annealing, indicating good ohmic contact behavior. Differing from TiO_x contacts, the non-annealed Pt/NiO_x/p-Si contacts show ohmic I-V behavior, and the annealing helps to reduce the contact resistivity compared with the non-annealed case. The ρ_c of Pt/NiO_x/p-Si does not show significant change for different annealing temperatures. The behavior discussed above occurs due to no fundamental phase change of sputtered NiO_x layer with annealing, and the NiO_x is still poly-crystalline,[26] with only the grain size increasing as the annealing temperature increases.[26] However, the ρ_c does not decrease substantially compared with the Pt/p-Si contact, showing a counterbalance between the reduced barrier and extra tunneling resistance.

On the other hand, for electrons, the Pt/NiO_x/n-Si does not form an ohmic contact for all annealing temperatures, proving the electron-blocking effect due to a large barrier for electrons.

The NiO_x layer was increased from 5 nm to 8 nm thickness for the Pt/NiO_x/p-Si structure. As shown in Fig. 5(b), the TLM results show that the 8 nm thick NiO_x cannot form an ohmic contact for any of the annealing temperatures considered in this study. This indicates that the increase in tunneling resistance associated with thicker NiO_x possibly arises from more severe sputtering damage accumulated at the NiO_x–sputter interface.

III. CONTACT RESISTIVITY SIMULATION

To quantitatively estimate the effective barrier Φ_B of the MIS contact discussed above, the ρ_c is modeled as a function of Φ_B and the interlayer thickness using the Tsu-Esaki model.[27,28] In this model, two paths are available for majority carriers transporting through the contact: (i) reaching the top of the barrier Φ_B then scattering through the interlayer, and (ii) directly tunneling through the interlayer, as shown in Fig. 6(a) for electrons and Fig. 6(b) for holes. Both paths are directly determined by the interlayer oxide thickness. The ρ_c of both Al/TiO_x/n-Si and Pt/NiO_x/p-Si contacts are modeled and calculated as a function of the barrier height Φ_B, for different oxide thicknesses as shown in Fig. 6.

From Fig. 6, the ρ_c increases rapidly as barrier height increases for both Al/TiO_x/n-Si and Pt/NiO_x/p-Si structures. For Al/TiO_x/n-Si contact structures, the electron energy barrier Φ_B can be estimated based on the ρ_c extracted from TLM structures with forming gas annealing. In this case, the electron energy barrier is estimated to be within the range $0.16\,\text{eV} < \Phi_{B(TiOx=6\,nm)} < 0.25\,\text{eV}$ for 6 nm TiO_x, and $0.03\,\text{eV} < \Phi_{B(TiOx=10\,nm)} < 0.06\,\text{eV}$ for 10 nm TiO_x, respectively. Similarly, for Pt/NiO_x/p-Si structure, 5 nm NiO_x was

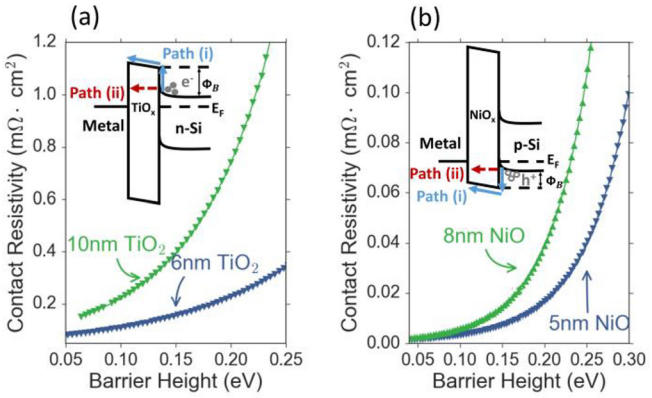

FIG. 6. Simulated contact resistivity as a function of barrier height Φ_B for different oxide thicknesses, (a) Al/TiO_x/n-Si and (b) Pt/NiO_x/p-Si.

able to form an ohmic contact and the corresponding energy barriers for holes are $0.17\,\text{eV} < \Phi_{B(NiOx=5\,nm)} < 0.26\,\text{eV}$. Based on the simulation result, the effective barrier Φ_B for majority carriers of both Al/TiO_x/n-Si and Pt/NiO_x/p-Si are effectively reduced due to the surface depinning effect.

IV. NiO_x SURFACE PASSIVATION

A. Device fabrication

The surface passivation ability of TiO_x for c-Si to improve effective minority carrier lifetime has been reported by other work.[11,29,30] The efficacy of contact passivation of NiO_x interlayers is assessed through the contact recombination factor J_{0C},[31] which is determined from the lifetime test structures. Two types of test structures were fabricated on 10 000 Ω cm float-zone (FZ) wafers, as shown in Figs. 7(a) and 7(b). Next, 100 nm thick $10^{17}\,\text{cm}^{-3}$ boron doped p+ layers were deposited on both sides of the FZ wafers using the same RPCVD process as above, with target sheet resistance of $2.0 \times 10^4\ \Omega\ \text{sq}^{-1}$. Next, for the Pt/Si test structure, Pt films with 10 nm thickness were deposited on both sides of the sample using the sputtering process described above. The Pt films are introduced in this experiment to create a Pt/p-Si MS structure similar to the TLM contact structures discussed before (to mimic the device metal contact), while still being thin enough to transmit light into the Si to allow injection-dependent carrier lifetime to be measured by the quasi-steady-state-photoconductance (QSSPC)[32] method. On the other hand, for the Pt/NiO_x/Si test structure, 5 nm NiO_x layers were deposited on both sides of the sample using the sputtering process before the deposition of 10 nm Pt films. Later, samples of both structures were annealed in forming gas under different temperatures to study the J_{0C}. The effective lifetime (total minority carrier lifetime considering effects from bulk silicon region and contacts on top and bottom) was measured by the QSSPC method in a standard Sinton WCT-120 system at 25 °C. Finally, the contact recombination factor J_{0C} was extracted using the Kane and Swanson method.[31]

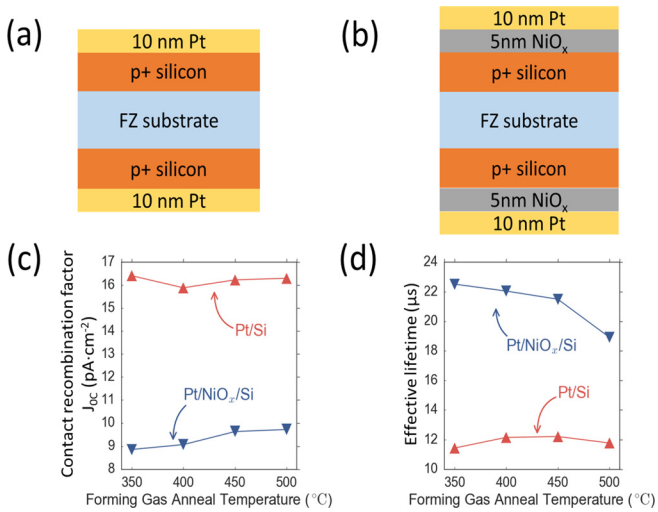

FIG. 7. Lifetime test structure schematics of (a) Pt/Si and (b) Pt/NiO_x/Si. (c) Dependence of J_{0c} on annealing temperature for the two test structures. (d) Dependence of effective lifetime on annealing temperature for the two test structures.

B. Results and discussion

The comparison of J_{0C} of the two structures is shown in Fig. 7(c), together with the J_{0C} dependence on annealing temperature. For all annealing temperatures, the J_{0C} of Pt/NiO_x/p-Si structure is significantly lower than that of Pt/p-Si structure, which is derived from the improvement of effective minority carrier lifetime shown in Fig. 7(d). At 350 °C, the J_{0C} of Pt/NiO_x/p-Si is only $8.62\,\text{pA cm}^{-2}$, which is only 52% of the J_{0C} of Pt/Si. This clearly shows the contact passivation effect of NiO_x interlayer. For the Pt/p-Si structure, annealing at different temperatures did not change the J_{0C} much, with a relative variation of within ±1.5%.

V. CONCLUSION

In summary, this work demonstrated the electron-conducting, hole-blocking behavior of TiO_x and the opposite carrier-selective property of NiO_x. For electron-selective contact, ρ_c of lower than 0.4 $\text{m}\Omega\,\text{cm}^2$ is obtained for Al/TiO_x (6 nm)/n-Si contact structures. For hole-selective contact, ρ_c of lower than 0.02 $\text{m}\Omega\,\text{cm}^2$ is obtained for Pt/NiO_x (5 nm)/p-Si contact structures. The impact of interlayer thickness and annealing was also shown. The interlayer thickness needs to be optimized to satisfy the requirements for MIS contacts to the silicon solar cell to (i) effectively de-pin the Fermi level to reduce the barrier for majority carriers and (ii) maintain a low enough resistance associated with the interlayer oxide. The metal–silicon interface passivation efficacy of sputtered NiO_x is also demonstrated experimentally by the reduction of J_{0C} due to the improvement of effective minority carrier lifetime.

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