Intrinsic threshold mechanism of phase-change memory cells by pulsed current–voltage characterization

W. Chen, Z. Li,[a] J. H. Peng, Y. F. Deng, and X. S. Miao
Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China and School of Optics and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China

(Received 30 July 2012; accepted 20 September 2012; published online 3 October 2012)

A short pulsed current–voltage (*I-V*) measurement method is proposed for phase-change random access memory (PCRAM) to investigate the self-heating behavior. The pulse widths and periods are indispensable parameters to describe pulsed *I-V* characteristics of PCRAM cells. By comparing the difference between direct current *I-V* curves and pulsed *I-V* curves, the threshold voltages of pulsed *I-V* are much higher. It implies the existence of self-heating and energy accumulation. Assume that the heating of the active region causes the change of the electronic barrier and the electronic activity, the physical model dominated by the self-heating in PCRAM cells is proposed. [http://dx.doi.org/10.1063/1.4757280]

With a growing interest in phase-change random access memory (PCRAM), there is plenty of studies to elucidate the properties of PCRAM.[1–11] The current-voltage (*I-V*) characteristic is one of the most important electrical properties of PCRAM. Normally, we explore the *I-V* characteristics of PCRAM through a direct current (DC) sweep which is step-like. Energy accumulation effect occurs in the testing procedure because the thermal energy generated by every historical increased step voltage partly remains in the cell under test (CUT) and accumulates. In fact, the energy accumulation effect of the CUT happens not only in exerted DC bias but also in a series of exerted pulses. The direct consequence of this phenomenon adversely affects the intrinsic characteristics of PCRAM cells. The resistance-current (*R-I*) and resistance-voltage (*R-V*) characteristics of PCRAM are also studied.[4–7] The CUT returns to its initial state by a fixed Reset or Set pulse after Set or Reset programming. This testing method also does not completely eliminate the effect of self-heating nor energy accumulation. Ielmini has found that the threshold voltage (V_{th}) decreases with increasing environmental temperature or with decreasing (E_C-E_F).[12–16] In fact, the conclusion that V_{th} decreases linearly with increasing environmental temperature has been demonstrated by Miao and Lee, who employ DC *I-V* and pulsed *I-V*, respectively.[11,17] In this letter, we use the model of the temperature of the active region, combining with the concepts of the band theory and the electronic activity, to investigate the dependence of the threshold switching on pulse width, pulse period, and two-state resistance ratio.

The structure of PCRAM cells consists of five layers. The phase-change layer, which consisted of a Ge-Sb-Te compound film, is sandwiched between two TiW electrodes. The feature size of the cell is 1 μm. A schematic drawing is shown in Fig. 1. From the Si substrate with SiO_2, the layer specifications are as follows: a 200 nm TiW layer, a 100 nm SiO_2 layer, a varying thickness of the phase-change material $Ge_2Sb_2Te_5$ (GST) layer followed by a 20 nm TiW layer, a 100 nm SiO_2 layer, and finally a 180 nm TiW layer. The thickness of the GST layer under study is 25 nm, 75 nm, and 150 nm, respectively.

Fig. 2(a) shows the setup of the pulsed *I-V* characterization testing system of PCRAM cells. Here, a Keithley Model 4200-SCS controls a DC bias, a pulse generator 4205-PG2, and a Tektronix DPO70604 digital scope via general purpose interface bus (GPIB). A high-speed MOSFET transistor plays the role of a switch device. The pulse generator can provide a pulse with a minimum width of 10 ns. It indirectly connects to the gate of the transistor. The required rise and fall time of the pulses are set to 10 ns. Amplitude is up to 5 V. Due to the limitation of devices, the pulse width is more than 100 ns. The DC bias module provides DC bias to the top electrode of the CUT. The bottom electrode connects to the drain. The bias tee limits the upper range of the pulse. The power divider ensures the integrity of the pulse signal.

A pulse sequence V_g with constant amplitude, width, and period is applied to the gate. At the same time, a step-like DC bias V_d varying from zero to the setting voltage is applied to the top electrode of the CUT. V_d is less than 2 V and the transistor works in the linear region. V_g is set to 5 V

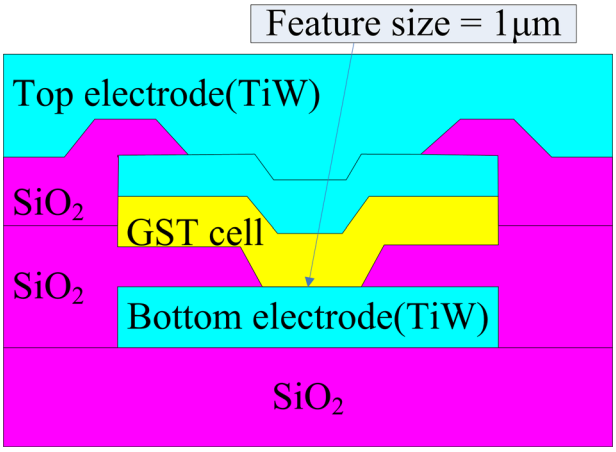

FIG. 1. Schematic figure of cross-section of the PCRAM cell structure.

[a]Electronic mail: lizhen@mail.hust.edu.cn.

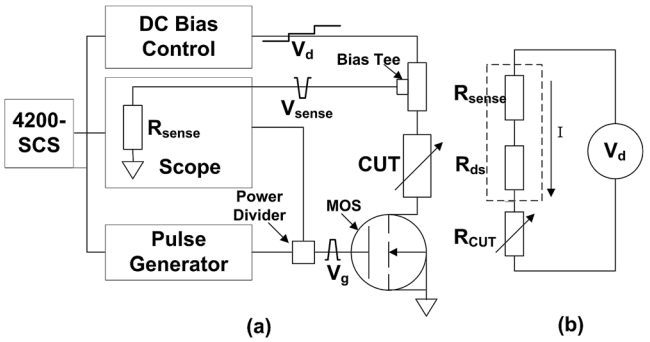

FIG. 2. (a) Circuit of the short pulsed *I-V* experiment, in which a MOSFET transistor is used as a switch. (b) A closed circuit is formed with the components of the transistor's on-resistance R_{ds}, the input impedance R_{sense}, the resistance R_{CUT} and the DC bias V_d.

so that the transistor's on-resistance R_{ds} is about 50 Ω. When the pulse is applied to the gate, the transistor switches to the on-state. A closed circuit is formed with the components of the on-resistance R_{ds}, the input impedance R_{sense}, the resistance R_{CUT} and the DC bias V_d. The corresponding small signal circuit is shown in Fig. 2(b). The current through the CUT is calculated using the voltage drop from the response across the input impedance (50 Ω) of the scope.[18,19] The voltage drop of the CUT can be calculated by using the equation $V_{CUT} = V_d\text{-}V_{ds}\text{-}V_{sense}$. We know that $R_{sense} \ll R_{CUT}$, $R_{ds} \ll R_{CUT}$, so $V_{sense} \ll V_{CUT}$, $V_{ds} \ll V_{CUT}$, $V_{CUT} \approx V_d$. Therefore, I-V curves can be obtained with the current through the CUT and the voltage drop across it. In this experiment, we vary the pulse width and pulse period to get a series of pulsed *I-V* curves.

Fig. 3 shows the pulsed *I-V* curves at various pulse widths with the fixed period of 200 μs for a 75 nm PCRAM cell. Starting from the amorphous state, the cell switches to the crystalline state after a pulse I-V testing. Then we use the same energy to switch the cell to the initial amorphous state, which is called Reset[8,9] programming in the jargon of PCRAM technology. By comparing the pulsed *I-V* curves of different pulse widths, we find the dependence of V_{th} on pulse width. Simulation shows that V_{th} decreases logarithmically with increasing pulse width.

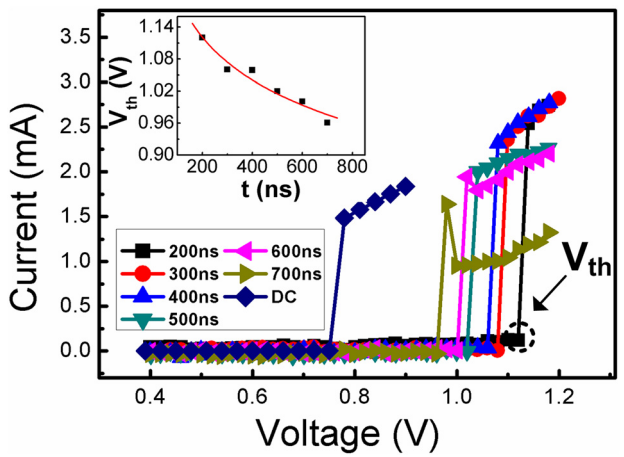

FIG. 3. Pulsed *I-V* curves of a representative cell at various pulse widths. The definition of V_{th} is denoted. The inset shows the pulse width dependence of V_{th} of the cell.

First, a 150 nm cell is tested under different pulse periods by pulsed *I-V* testing method. Then we change the thickness of the phase-change layer to 75 nm for testing. Figs. 4(a) and 4(b) show that V_{th} changes with pulse width under different pulse periods. As the period enlarges, larger V_{th} at the same pulse width is needed to drive the phase change.

Furthermore, we regulate the resistance ratio of the amorphous and crystalline state, while the thickness of phase-change layer and pulse period remain unchanged. Figs. 4(c) and 4(d) show V_{th} changes with the pulse width under different two-state resistance ratios. The result indicates that the larger the resistance ratio, the larger the V_{th} at the same pulse width.

Many models have been proposed to describe the threshold switching phenomenon in chalcogenide material. The existence of the self-heating behavior was explained by the temperature model and the transport properties of the amorphous phase. However, the heat distribution in a GST cell is still a complex problem. When a pulse is applied to the cell, we can evaluate the temperature of the active region with Joule heating and heat dissipation in simple terms as[20–23]

$$\Delta T = T - T_0 = \int \frac{W_j - W_d}{CV} dt - T_0, \tag{1}$$

where C is the heat capacity of GST, V is the heating volume, W_j is the heating power of the PCRAM cell, and W_d is the thermal dispersion rate. W_j and W_d are as follows:[20–23]

$$W_j = IU = \frac{U^2}{R}, \tag{2}$$

$$W_d = \frac{\partial Q}{\partial t} = -\Sigma \kappa \Delta T, \tag{3}$$

where κ is the thermal conductivity of GST, I and U are the current flow and voltage across a GST cell, respectively, R is the resistance of the cell during the programming process.

During a pulse, the temperature rise is calculated by

$$\Delta T_1 = \frac{L^2 W_j}{\kappa V}\left[1 - \exp\left(-\frac{\kappa t}{L^2 C}\right)\right], \tag{4}$$

where L is the thickness of the GST layer and t is the pulse width.

When the pulse ends, there is no voltage drop on the cell and only thermal dispersion happens. We use the unsteady solutions without generation based on the Cartesian with constant κ and C to calculate the thermal diffusion[24]

$$\frac{\partial T}{\partial t} = \frac{\kappa}{C}\frac{\partial^2 T}{\partial x^2}. \tag{5}$$

During a pulse cycle, the temperature rise of the active region can be calculated by using Eqs. (1)–(5). The temperature rise and decay for various voltages are extracted from the 2-D simulation results and presented in Fig. 5. When the cooling time is not enough, the temperature would not decay to the original temperature. After each periodic pulse, the temperature of the active region rises a little. Even so, the total cumulative temperature is considerable when pulse number is large. When we set larger pulse width or shorter

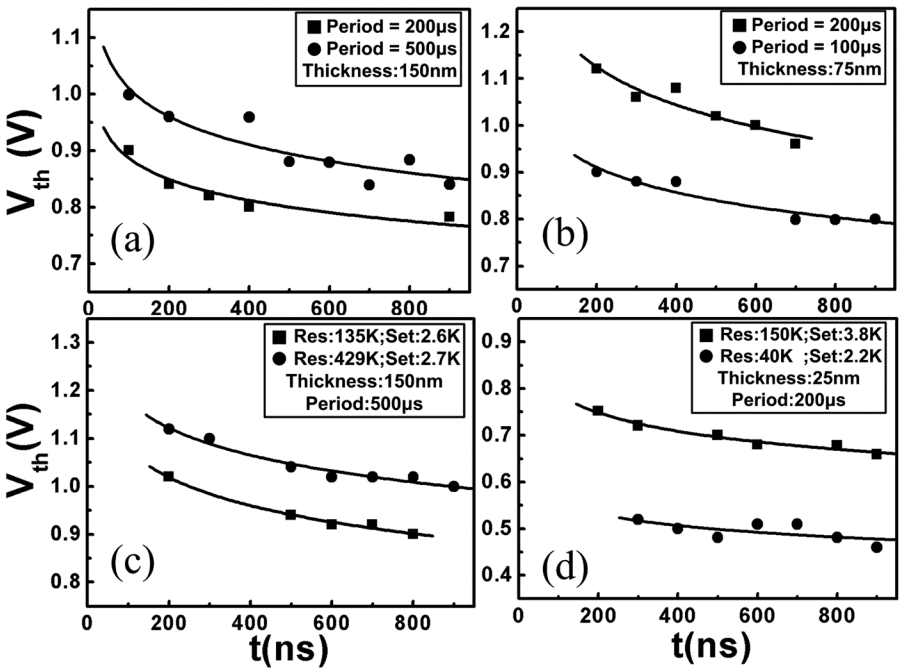

FIG. 4. The pulse width dependence of V_{th} of (a) a 150 nm cell under different pulse periods, (b) a 75 nm cell under different pulse periods, (c) different cells with 150 nm phase-change layer under the pulse period of 500 μs, (d) different cells with 25 nm phase-change layer under the pulse period of 200 μs.

pulse period, the temperature of the active region rises faster and V_{th} decreases significantly.

In order to simplify our analysis, we assume the resistivity behavior of the phase-change material in amorphous state as a semiconductor's and that in crystalline state as a conductor's. Because the resistivity in crystalline state is much lower than that in amorphous state and its Ohm linear *I-V* curve is similar to the conductor. Then we use the model of the electronic barrier to explain the relationship between V_{th} and the two-state resistance ratios of the cells with the same thickness of the GST layer. The concentration of electrons in fully amorphous state is given by

$$n = N_c \exp\left(-\frac{E_C - E_F}{K_0 T}\right). \tag{6}$$

The fully amorphous electronic resistivity is calculated by

$$\rho_{Reset} = \frac{1}{nq\mu} = \frac{1}{q\mu N_C} \exp\left(\frac{E_C - E_F}{K_0 T}\right), \tag{7}$$

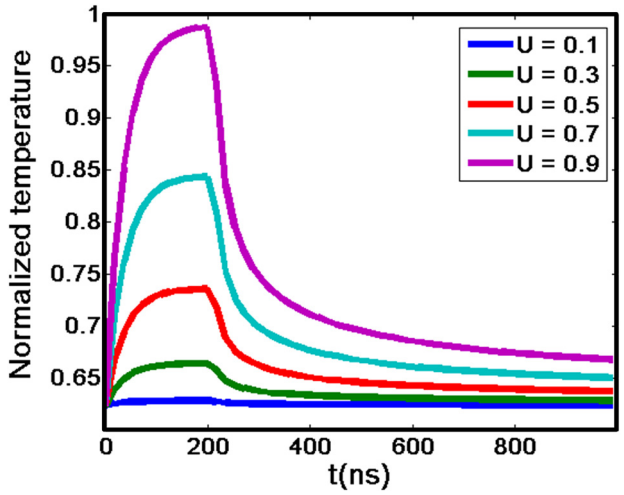

FIG. 5. Heating and cooling histories of a representative cell at different voltages.

where q is the elementary charge, μ is the electronic mobility, and K_0 is the Boltzmann constant.

The two-state resistance ratio can be calculated by

$$R_{\text{ratio}} = \frac{R_{Reset}}{R_{Set}} = \frac{L}{q\mu N_C S R_{Set}} \exp\left(\frac{E_C - E_F}{K_0 T}\right), \tag{8}$$

where L is the thickness of the GST layer and S is the contact area between the cell and the electrode. They are the same for the cells with the same thickness of the phase-change layer. Since the resistance in fully crystalline state changes a little, we assume the resistance R_{Set} of the cells with the same thickness of the GST layer is almost the same in fully crystalline state. From Eq. (8), we can know that if the Fermi level is far from the conduction band, the resistance ratio of the amorphous and crystalline state is large. The resistance ratio decreases when (E_C-E_F) decreases. Then the larger the resistance ratio is, the larger the V_{th} is.

In summary, we have investigated the dependence of the threshold switching characteristics of phase-change memory on pulse width, pulse period, and two-state resistance ratio. A function based on temperature model has been derived. We have found that V_{th} decreases with increasing pulse width and increases with increasing pulse period or increasing resistance ratio of the amorphous and crystalline state. The relationship between the threshold switching and pulse width, pulse period, two-state resistance ratio is well described by the temperature model of the active region, the band theory, and the electronic activity. In conclusion, the temperature of the active region slowly rises and the energy gradually accumulates during pulsed *I-V* testing process. Fermi level shifts closer to the conduction band and the electronic barrier gets lower when the temperature of the active region rises. When a voltage bias exceeds the barrier, the threshold switching takes place.

This work was financially support by the university funding (No. 2011TS047) of Huazhong University of Science and Technology, National High-tech R&D Program (863

Program) (No. 2011AA010404), Program of International S&T Cooperation of the Ministry of science and technology (No. 2010DFA11050), and the Ph.D. Programs Foundation of Ministry of Education of China (No. 20090142110003).

[1]O. Ozatay, B. Stipe, J. A. Katine, and B. D. Terris, J. Appl. Phys. **104**, 084507 (2008).
[2]A. Redaelli, A. Pirovano, A. Benvenuti, and A. L. Lacaita, J. Appl. Phys. **103**, 111101 (2008).
[3]S. W. Ryu, J. H. Lee, Y. B. Ahn, C. H. Kim, B. J. Choi, C. S. Hwang, and H. J. Kim, Appl. Phys. Lett. **93**, 172114 (2008).
[4]L. W. Qu, X. S. Miao, J. J. Sheng, Z. Li, J. J. Sun, P. Ana, J. D Huang, D. H. Yang, and C. Liu, Solid-State Electron. **56**, 191–195 (2011).
[5]I. V. Karpov and S. A. Kostylev, IEEE Electron Device Lett. **27**, 808 (2006).
[6]R. Zhao, L. P. Shi, W. J. Wang, H. X. Yang, H. K. Lee, K. G. Lim, E. G. Yeo, E. K. Chua, and T. C. Chong, in *The Nano-Scale IEEE Non-Volatile Memory Technology Symposium* (IEEE Conference Publications, 2007), pp. 36–39.
[7]B. J. Bae, S. H. Hong, S. Y. Hwang, J. Y. Hwang, K. Y. Yang, and H. Lee, Semicond. Sci. Technol. **24**, 075016 (2009).
[8]N. Kazuya, K. Toshiya, O. Masashi, and S. Masakuni, Jpn. J. Appl. Phys. **32**, 564 (1993).
[9]S. Braga, A. Cabrini, and G. Torelli, Semicond. Sci. Technol. **24**, 115008 (2009).
[10]D. S. Chao, C. Lien, C. M. Lee, Y. C. Chen, J. T. Yeh, F. Chen, M. J. Chen, P. H. Yen, M. J. Kao, and M. J. Tsai, Appl. Phys. Lett. **92**, 062108 (2008).
[11]X. S. Miao, L. P. Shi, H. K. Lee J. M. Le, R. Zhao, P. K. Tan, K. G. Lim, H. X. Yang, and T. C. Chong, Jpn. J. Appl. Phys., Part 1 **45**, 3955 (2006).
[12]D. Ielmini and A. L. Lacaita, Mater. Today **14**, 600 (2011).
[13]S. Raoux, D. Ielmini, M. Wuttig, and I. Karpov, Mater. Res. Soc. **37**, 2 (2012).
[14]D. Ielmini and Y. Zhang, Appl. Phys. Lett. **90**, 192102 (2007).
[15]D. Ielmini and Y. Zhang, J. Appl. Phys. **102**, 054517 (2007).
[16]D. Ielmini and A. L. Lacaita, in European Phase Change and Ovonics Science Symposium, E*PCOS, 2007.
[17]S. Lee, D. S. Jeong, J. H. Jeong, W. Zhe, Y. W. Park, H. W. Ahn, and B. K. Cheong, Appl. Phys. Lett. **96**, 023501 (2010).
[18]K. A. Jenkins, J. Y.-C. Sun, and J. Gautier, IEEE Trans. Electron Devices **44**, 1923 (1997).
[19]C. D. Young, Y. G. Zhao, M. Pendley, B. H. Lee, K. Matthews, J. H. Sim, R. Chio, G. A. Brown, R. W. Murto, and G. Bersuker, Jpn. J. Appl. Phys., Part 1 **44**(4B), 2437–2440 (2005).
[20]U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, IEEE Trans. Electron Devices **55**, 506 (2008).
[21]J. Reifenberg, E. Pop, A. Gibby, S. Wong, and K. Goodson, in *Proceedings of International Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)* (IEEE Conference Publications, 2006), p. 106.
[22]K. C. Kwong, L. Li, J. He, and M. Chan, in 9th International Conference on Solid-State and Integrated-Circuit Technology, ICSICT 2008, 20-23 October 2008.
[23]X. Li, Z. T. Song, D. L. Cai, X. G. Chen, and H. P. Chen, J. Semicond. **32**, 094011 (2011).
[24]H. S. Carslaw and J. C. Jaeger, *Conduction of Heat in Solids* (Oxford University Press, London, 1959).