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Effect of silicon oxide thickness on polysilicon based passivated contacts for high-efficiency crystalline silicon solar cells

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ABSTRACT

In this study, we have investigated the effect of SiO_x thickness (1–3 nm) on the performance of polycrystalline (poly) Si/SiO_x/monocrystalline Si (*c*-Si) passivated contacts. Our results show that for both *n*- and *p*-type contacts, there is an optimum SiO_x thickness of 1.4–1.6 nm for obtaining the highest implied open-circuit voltage (*i*-V_{oc}) values of ~739 and ~700 mV, respectively. For contacts with SiO_x thicker than 1.6 nm, the *i*-V_{oc} drops due to reduced field-effect passivation. We attribute this to the fact that a thicker SiO_x layer hinders the diffusion of both *n*- and *p*-type dopants into the *c*-Si wafer resulting in a junction that is very close to the *c*-Si/SiO_x interface, which increases carrier recombination most likely due to the presence of defects at this interface. The resistivity measured through the metal/poly-Si/SiO_x/*c*-Si stack is independent of SiO_x thickness up to 1.6 nm, and increases exponentially by several orders of magnitude with further increase in SiO_x thickness due to inefficient tunneling transport. Finally, the extent of metallization-induced degradation of the poly-Si/SiO_x/*c*-Si contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly it is not completely mitigated even for a ~3 nm thick SiO_x.

1. Introduction

Monocrystalline Si (*c*-Si) solar cells with passivated contacts based on the ultrathin SiO_x and doped polycrystalline Si (poly-Si) layers in a metal/poly-Si/SiO_x/*c*-Si structure can achieve efficiencies > 25% [1,2]. These contacts use a 1–2 nm thick tunneling SiO_x on *c*-Si, and doped poly-Si on SiO_x, to create a poly-Si/SiO_x/*c*-Si passivated contact structure [3–5]. The separation of the doped poly-Si layer from *c*-Si through SiO_x is critical as it provides a very low recombination interface to the wafer and prevents the epitaxial growth of the poly-Si layer during the required high temperature annealing of these contacts. The ultrathin ~1–2 nm SiO_x enables electrical transport via tunneling [6–8] and/or pinholes in the SiO_x layer [9–11], and is a very good surface passivation layer for *c*-Si due to the low *c*-Si/SiO_x interfacial defect densities [12,13]. Additional field-effect passivation is obtained due to the heavily doped poly-Si layer deposited on the tunneling SiO_x layer. A combination of these two passivation mechanisms leads to a very low emitter recombination current density, J_o [9,14,15]. The separation of the metal contacts from the *c*-Si absorber, via the use of the doped poly-Si/SiO_x stack helps reduce the metallization-induced carrier recombination, while enabling carrier separation and collection.

The high-temperature stability, excellent passivation, and manufacturing flexibility demonstrated by these contacts make them a suitable candidate for next-generation *c*-Si solar cell technologies. However, to incorporate them into industrial-scale manufacturing, it is important to understand their salient features while identifying the allowed processing windows for these contacts. Currently, in the literature, different techniques have been reported for the fabrication of the poly-Si/SiO_x/*c*-Si contacts. The SiO_x layer can be grown either via dry thermal oxidation [16], or by chemical oxidation with nitric acid [4,5] or UV/O_3 [17]. Even though these SiO_x films have different stoichiometry, surprisingly they show marginal effect on the final passivated contact performance [17]. The doped poly-Si film can be grown via either plasma-enhanced chemical vapor deposition (PECVD) [4,16] or low-pressure chemical vapor deposition [5]. Additionally, these poly-Si films can be doped in numerous ways such as during growth of amorphous Si (*a*-Si) [16], ion-implantation of intrinsic poly-Si [5], $POCl_3$ and BBr_3 thermal diffusion [18], or with suitable dopant pastes and inks [19]. The morphology of the doped Si layers can be either polycrystalline [16], microcrystalline [4], or an amorphous

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matrix embedded with Si nanocrystallites [20]. However, even with all these variabilities, the final contact performance is similar, with implied open-circuit voltage (i-V_{oc}) values being ~735–740 mV for phosphorous doped n-type and ~700–710 mV for boron doped p-type contacts [4,16]. The only common feature in these contacts is that the SiO_x layer is ~1.5 nm thick, and the contacts need to be annealed between 850 and 900 °C after a-Si deposition for obtaining the highest i-V_{oc} values. The loss of performance upon annealing above 900 °C has been attributed to significant SiO_x break-up, which results in localized loss of the chemical passivation provided by the SiO_x layer [21,22]. A different approach, the poly Si on oxide (POLO) [10,18] contacts reported by the Institute for Solar Energy Research in Hamelin (ISFH) have a very similar poly-Si/SiO_x stacked structure but with a thicker, ~2.2 nm, SiO_x. However, these contacts are processed at a much higher temperature of ~1000–1050 °C to achieve record high i-V_{oc} values of 748 and 729 mV for both the n- and p-type contacts, respectively [23]. For these POLO contacts, the higher temperature is quite crucial since it results in pinholes in SiO_x that provide direct conduction pathways between the poly-Si and underlying c-Si absorber resulting in very low through-contact resistivities [10,11,24].

In this study, we focus on understanding the role of the thickness of the thermally-grown SiO_x layer on the contact performance where the contact annealing temperature is limited to 850 °C. Under these conditions, we do not expect SiO_x breakup, which can significantly affect charge transport and surface passivation. We show that a SiO_x thickness within 1.4–1.6 nm leads to the highest i-V_{oc} values of ~739 and ~700 mV for n- and p-type contacts, respectively. We hypothesize that this SiO_x thickness range provides an optimum balance between the chemical passivation from the SiO_x layer and the field-effect passivation from the dopants, as both of these depend on the SiO_x thickness. We show that carrier transport through the contact reduces by several orders of magnitude when the SiO_x thickness is increased from 1.6 to 1.9 nm due to inefficient tunneling. Finally, we show that the extent of metallization-induced degradation of the poly-Si/SiO_x contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly is not completely mitigated even for a ~3 nm thick SiO_x.

2. Experimental details

As-sawn, phosphorous-doped, n-type Czochralski (n-Cz) Si(100), 8 Ω-cm resistivity, ~190 µm thick wafers (Woongjin Co. Ltd., South Korea) were subjected to a KOH based etch for planarization and saw-damage removal. The wafers were then cleaned using standard wafer cleaning procedures of piranha, RCA-1 and RCA-2 [25,26], followed by a treatment with 1% aqueous HF to remove the SiO_x formed as a result of the RCA-2 cleaning process. A dry thermal SiO_x film was then grown on the wafers in a quartz tube furnace at nearly atmospheric pressure with a 6:1 N_2-to-O_2 gas flow ratio. The thermal SiO_x thickness was varied by changing the oxidation time between 0.5 and 30 min for temperatures between 700 and 800 °C. The SiO_x thickness at each oxidation condition was determined by spectroscopic ellipsometry on single-side-polished n-Cz Si(100), 1–100 Ω-cm resistivity wafers that were loaded into the furnace at the same time as the saw-damage removed wafers.

Doped a-Si:H was then deposited on both sides of the oxidized c-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4 and H_2 were 2 and 100 standard cm^3/min (sccm), respectively. Additionally, for boron or phosphorous doping, 1 sccm of B_2H_6 (2.6% in H_2) or PH_3 (3% in H_2) were introduced into the chamber. The c-Si wafer was placed on the grounded substrate holder at a temperature of 300–350 °C with an input power to the plasma source of 8 W to grow a ~20 nm thick a-Si:H layer. The resulting samples were then annealed at 850 °C for 30 min in a quartz tube furnace under N_2 atmosphere to convert a-Si:H to a poly-Si layer via solid-phase crystallization. A hydrogen-induced passivation step followed, which involved deposition of Al_2O_3 via atomic layer deposition using trimethylaluminium and H_2O as precursors at 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 20 min. Quasi-steady-state photoconductance decay measurements were performed using a Sinton lifetime instrument (WCT-120) to extract the i-V_{oc} values [27] for symmetric test structures on saw-damage removed wafers, similar to those shown in the inset of Fig. 1. Dopant depth profiles through the poly-Si layer into the c-Si wafer were measured on single-side-polished samples via secondary ion mass spectrometry (SIMS) using 1.5 keV ion bombardment energy from an oxygen source.

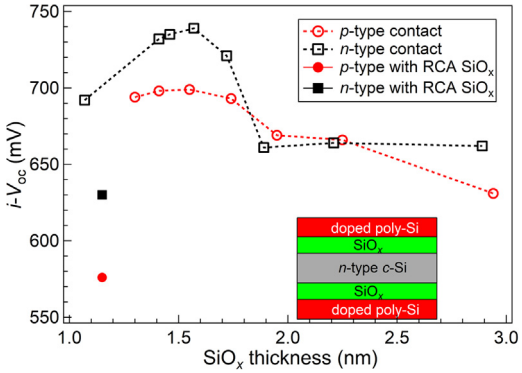

Fig. 1. Effect of thermally grown SiO_x thickness on the i-V_{oc} of symmetric n- (□) and p-type (○) passivated contact test structures shown in the inset. The i-V_{oc} for n- (■) and p-type (●) passivated contacts with ~1.15 nm thick RCA SiO_x is shown for comparison. The dashed lines are a guide to the eye.

On the symmetric poly-Si/SiO_x/c-Si/SiO_x/poly-Si structures on the saw-damage removed wafers, using suitable shadow masks, ~1 µm thick Al was deposited via electron beam (e-beam) evaporation in a tool with a base pressure of $\sim 10^{-7}$ Torr. Aluminum was deposited either as a $3 \times 2\,cm^2$ pad to determine metal-induced degradation, or as rectangular or circular pads that were much smaller in size, for resistivity measurements. Post-metallization, the n-type contact samples were annealed at 400 °C in forming gas for 5 min, since previous experiments [16] show that it results in lower metallization-induced degradation of the contact. However, the p-type contact did not require a post-metallization anneal. Metallization-induced degradation was determined using photoluminescence (PL) imaging, which measures the intensity from radiative carrier recombination in the sample under steady-state conditions at a fixed illumination intensity and wavelength [28]. The poly-Si layer sheet resistivity, and the Al to poly-Si contact resistivity was determined using the smaller rectangular Al pads with varying spacing using the transmission line method (TLM) [29]. The structure with the TLM pattern was then subjected to reactive ion etching using SF_6 with the Al pads on the front as etching masks. After etching, the poly-Si and SiO_x layers were completely removed in the unmasked regions along with a few microns of the underlying c-Si. The opposite unmetallized side of the c-Si wafer was also etched to completely remove the poly-Si and SiO_x layers. The resulting structures were utilized to determine the through-contact resistivity for the n^+-n high-low junction by TLM analysis, and the diode resistivity at 0.59 V of the p^+-n diode from its current-voltage (J-V) curve.

3. Results and discussion

3.1. Effect of SiO_x thickness on c-Si surface passivation

Fig. 1 shows the effect of SiO_x thickness on the i-V_{oc} of symmetric n- and p-type passivated contact test structures shown in the inset. Contacts with thermally grown SiO_x show an i-V_{oc} that is at least 50 mV higher than the i-V_{oc} obtained for the RCA SiO_x with a very similar thickness, implying that the SiO_x growth method affects c-Si surface passivation. Also, there is a clear trend in Fig. 1, which shows that for

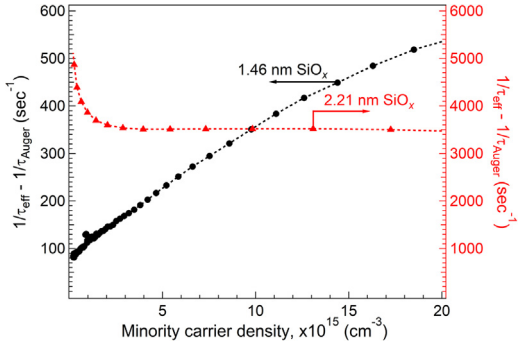

Fig. 2. The Auger corrected inverse effective lifetime versus minority carrier concentration plot for the n^+ poly-Si/SiO_x/n-type c-Si symmetric contact with SiO_x thickness of 1.46 nm (●) (left axis) and 2.21 nm (▲) (right axis). The dashed lines are a guide to the eye.

both n- and p-type contacts, the i-V_{oc} first increases, reaches a maximum of ~739 and ~700 mV for n- and p-type contacts, respectively, at ~1.5 nm SiO_x thickness, and then decreases with further increase in SiO_x thickness. While the lower i-V_{oc} for contacts with SiO_x < 1.4 nm can be attributed to poorer chemical passivation of dangling bonds on the c-Si surface, the decrease in i-V_{oc} for contacts with SiO_x > 1.6 nm is quite surprising since a thicker SiO_x layer should result in improved passivation of the c-Si wafer surface [30]. The reason for inferior passivation quality for contacts with SiO_x > 1.6 nm is attributed to lesser field effect passivation, which is discussed below.

Fig. 2 shows the Auger corrected inverse effective lifetime, $1/\tau_{eff}-1/\tau_{Auger}$, versus minority carrier concentration, Δn, curves evaluated from the Sinton lifetime instrument under high injection conditions. These measurements have been shown for n^+ poly-Si/SiO_x/n-type c-Si symmetric contacts for two different SiO_x thicknesses, 1.46 and 2.21 nm. The dependence of effective lifetime (τ_{eff}) on Δn under high injection conditions for the symmetric test structure is shown in Eq. (1),

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{bulk}} + \frac{2 \bullet J_o (N_{dop} + \Delta n)}{q n_i^2 W} \quad , \tag{1}$$

where τ_{bulk} is the bulk carrier lifetime in the c-Si substrate, W is the sample thickness, n_i is the intrinsic carrier concentration, N_{dop} is the doping concentration, q is the unit charge of an electron, and J_o is the emitter saturation current density [31]. Physically, J_o is related to the photogenerated carrier recombination associated with either a p-n or a high-low junction. Fig. 2 shows that for the contact with 1.46 nm SiO_x, the Auger corrected inverse effective lifetime increases linearly with the minority carrier concentration. The slope of this curve results in a low J_o value of 2.86 fA/cm^2, at $\Delta n = 5 \times 10^{15}$ cm^{-3}, which indicates excellent surface passivation of the wafer, and is consistent with the high i-V_{oc} of 735 mV (see Fig. 1). In contrast, the flatness of the Auger corrected inverse effective lifetime (see Fig. 2) for the contact with the 2.21 nm thick SiO_x, resulting in 662 mV i-V_{oc} (see Fig. 1), shows that the Auger corrected inverse lifetime is almost independent of Δn. Mathematically, such a relationship can be obtained if τ_{bulk} is very low such that the first term on the right-hand side in Eq. (1) dominates over the J_o term. However, we have confirmed that the different oxidation treatments do not degrade the bulk c-Si lifetime: this was verified by etching the symmetric test structures shown in the inset of Fig. 1 in KOH solution to remove the poly-Si and SiO_x layers, and a few microns of c-Si surface. The samples were then RCA-cleaned, passivated with Al_2O_3 and subjected to forming gas anneal. The i-V_{oc} on all the resulting structures was between 720 and 730 mV indicating high bulk lifetime in c-Si. The lack of dependence of the Auger corrected inverse effective lifetime on the minority carrier concentration may also suggest that $J_o \approx 0$. Therefore, Eq. (1) may no longer be valid for the 2.21 nm thick SiO_x contact likely because the SiO_x is so thick that the recombination

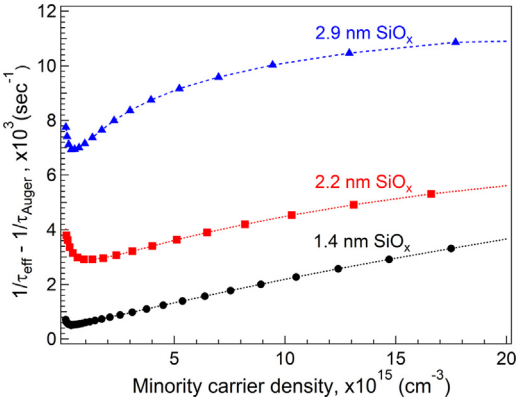

Fig. 3. The Auger corrected inverse effective lifetime versus minority carrier concentration plot for the p^+ poly-Si/SiO_x/n-type c-Si symmetric contact with SiO_x thickness of 1.4 (●), 2.2 (■) and 2.9 (▲) nm. The dashed lines are a guide to the eye.

of the photo-generated carriers is not governed by the high-low junction expected to form between the n^+ poly-Si layer and n-type c-Si wafer. The carrier recombination instead may be governed by the SiO_x passivating layer. Eq. (1) can then be modified as,

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{bulk}} + \frac{2 \bullet s}{W} \quad , \tag{2}$$

where s is the surface recombination velocity. Thus, this indicates a change in the nature of the passivated contact when the SiO_x thickness changes from 1.46 to 2.21 nm.

Fig. 3, similar to Fig. 2, shows the Auger corrected inverse effective lifetime versus minority carrier concentration curves for p^+ poly-Si/SiO_x/n-type c-Si symmetric contacts for three different SiO_x thicknesses, 1.4, 2.2, and 2.9 nm. It is evident in Fig. 3 that the plot for the contact with 1.4 nm SiO_x is increasing linearly, indicating the formation of an emitter. However, as SiO_x thickness increases the plots are less linear. For the contact with 2.9 nm SiO_x it is significantly non-linear with increasing Δn, indicating that the contact is no longer an emitter. Additionally, unlike for the n-type contact with 2.21 nm SiO_x shown in Fig. 2, the Auger corrected inverse effective lifetime for the p-type contact with 2.9 nm SiO_x (see Fig. 3) shows some dependence on the minority carrier concentration. The likely reason for the above observations is reduced dopant diffusion from poly-Si into the c-Si wafer due to a thicker SiO_x layer and is discussed below.

Figs. 4 and 5 show the phosphorous and boron depth profiles, respectively, within the poly-Si/SiO_x/c-Si stacked layers measured using SIMS. The phosphorous profiles were measured via time-of-flight SIMS, while the boron profiles via dynamic SIMS. The profiles have been plotted till the depth where the phosphorous and boron concentrations

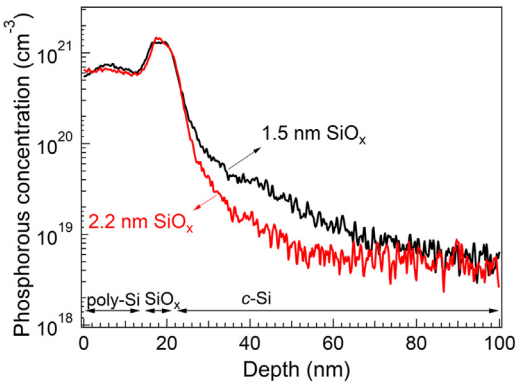

Fig. 4. SIMS depth profile of phosphorous in the n^+ poly-Si/SiO_x/n-type c-Si contact with 1.5 and 2.2 nm thick SiO_x.

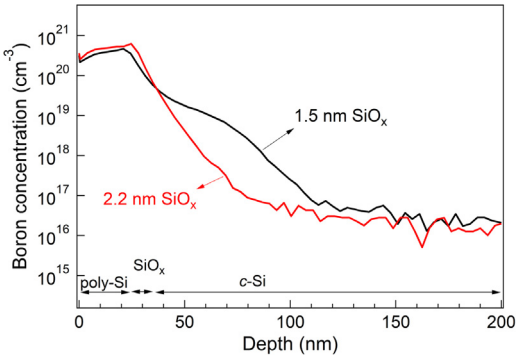

Fig. 5. SIMS depth profile of boron in the p^+ poly-Si/SiO$_x$/*n*-type *c*-Si contact with 1.5 and 2.2 nm thick SiO$_x$.

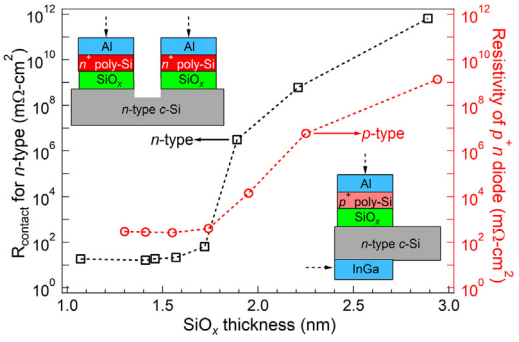

Fig. 6. Effect of thermally grown tunneling SiO$_x$ thickness on the through contact resistivity of *n*-type contact (□) (left axis), and p^+n diode resistivity of *p*-type contact (○) (right axis), on *n*-type *c*-Si wafer. Test structures for both measurements are shown in the inset with the dotted arrows showing contact points for the measurement probes. The dashed lines are a guide to the eye.

reach SIMS detection limits. The depth profiles are shown for contacts with two different SiO$_x$ thicknesses of 1.5 and 2.2 nm. Regardless of the SiO$_x$ thickness, the dopant concentration is very similar in the poly-Si film and the SiO$_x$ layer. However, the profiles within the *c*-Si region, directly underneath the SiO$_x$ layer are significantly different, with the dopants diffusing deeper into the wafer, up to ~80 nm, for the contact with the thinner, 1.5 nm, SiO$_x$ than for the contact with the marginally thicker, 2.2 nm SiO$_x$. Dopant diffusion from the poly-Si through SiO$_x$ into the *c*-Si wafer has been previously observed for similar passivated contacts, and likely occurs during the high temperature annealing step, 850 °C for this study, which is essential to obtain the high *i*-V_{oc} values [5,16,32]. As a result of this dopant diffusion, the *p*-*n* and the high-low junction depletion regions are not formed between the edge of the doped poly-Si film and the *c*-Si wafer, but instead lie completely within the *c*-Si wafer forming a diffused junction. Yang et al. [5] created similar passivated contact structures using ion implantation. In those experiments, the authors varied the dopant depth profiles into *c*-Si using ion-implantation of intrinsic *a*-Si, and concluded that both very shallow and very deep diffusion profiles result in poorer passivation compared to an intermediate dopant depth.

Relating the SIMS profiles in Figs. 4 and 5 to the Auger corrected inverse effective lifetime plots in Figs. 2 and 3 for the contact with the > 2.2 nm thick SiO$_x$, we can infer that reducing the extent of dopant diffusion into the wafer causes deviation of the contact properties from the ideal J_o behavior. This effect is quite significant for the n^+ poly-Si/2.21 nm SiO$_x$/*n*-type *c*-Si contact, as shown by the lack of dependence of Auger corrected inverse effective lifetime on Δn in Fig. 2. It is less prominent for the p^+ poly-Si/2.9 nm SiO$_x$/*n*-type *c*-Si contact, since it shows some dependence on Δn as shown in Fig. 3. This is most likely because the energy barrier for carriers to cross the junction is significantly less for a high-low junction due to a smaller band offset than for a *p*-*n* junction. Thus, the deviation of the contact properties from the ideal J_o behavior (see Figs. 2 and 3) can be inferred as a reduction in the net electric field experienced by the carriers near the *c*-Si surface, i.e., lesser field-effect passivation, and hence, lower *i*-V_{oc}. Another possible reason for the drop in *i*-Voc with increasing SiO$_x$ thickness can be due to increased voltage drop across the SiO$_x$ layer. However, the voltage drop across the SiO$_x$ layer, calculated using PC1D simulations based on the measured dopant profiles, is small and it cannot account for the *i*-V_{oc} versus SiO$_x$ thickness trend shown in Fig. 1. Hence, the likely cause for the lower *i*-V_{oc} for contacts with > 1.6 nm SiO$_x$ layer (see Fig. 1) is due the reduction in the extent of field-effect passivation. On the other hand, the lower *i*-V_{oc} for contacts with SiO$_x$ thickness < 1.4 nm can be attributed to poorer chemical passivation of dangling bonds on the *c*-Si surface [30]. To summarize, there is a balance between the extent of chemical passivation provided by the SiO$_x$ layer, which increases as SiO$_x$ thickness increases, and the extent of field-effect passivation provided due to dopant diffusion through the SiO$_x$ layer into the *c*-Si wafer, which reduces as SiO$_x$ thickness increases.

3.2. Effect of SiO$_x$ thickness on contact transport properties

Along with excellent passivation of the wafer to generate a high V_{oc}, passivated contacts should also allow for transport of the photo-generated carriers to ensure a high fill-factor and, hence, a high cell efficiency. Fig. 6 shows the resistivity through the poly-Si/SiO$_x$/*n*-type *c*-Si stack for *n*- and *p*-type contacts with different SiO$_x$ thickness for test structures shown in the inset. For the *n*-type contacts, the contact resistivity was evaluated with the TLM [29] approach, and shows that for contacts with SiO$_x$ thickness < 1.6 nm, the contact resistivity is low, and ~20 mΩ-cm^2 irrespective of SiO$_x$ thickness. However, for these *n*-type contacts, a slight increase in the SiO$_x$ thickness to 1.9 nm significantly increases the contact resistivity by 5 orders of magnitude, and this trend continues as SiO$_x$ thickness is increased further. Such a significant rise in contact resistivity is consistent with poorer tunneling transport through the SiO$_x$ layer. A similar analysis using the TLM approach is not possible for the p^+ poly-Si/SiO$_x$/*n*-type *c*-Si contact since it forms a *p*-*n* diode with the *n*-type *c*-Si wafer. However, when we measured the *J*-*V* curves across the *p*-*n* diodes for different SiO$_x$ thicknesses using test structures as shown in the inset of Fig. 6, we noticed that the forward current through the diodes with the thicker SiO$_x$ was significantly lower than the ones with thinner SiO$_x$. To quantify the extent of reduction in current, we calculated the inverse of the slope of the *J*-*V* curves at a fixed forward biasing voltage of 0.59 V and termed it as "diode resistivity," which is plotted on the right axis in Fig. 6. While this parameter does not represent true contact resistivity of the structure, it clearly demonstrates the effect of SiO$_x$ thickness on transport through the *p*-*n* diode. Similar to the *n*-type contact (see Fig. 6), the diode resistivity of the *p*-type contact is almost constant for < 1.6 nm SiO$_x$ thickness, and increases by several orders of magnitude when the SiO$_x$ thickness increases from 1.6 nm to more than 1.7 nm. We also measured the metal to poly-Si contact resistivity via TLM for test structures shown in the inset of Fig. 7. Those values (not shown) were significantly lower than the contact resistivity measured through the metal/poly-Si/SiO$_x$/*c*-Si stack shown in Fig. 6. Hence, all the observed changes in contact resistivity shown in Fig. 6 can be attributed to the effect of changes in the SiO$_x$ layer thickness. The similar behavior of the contact resistivity through the metal/poly-Si/SiO$_x$/*c*-Si stack for the *n*- and *p*-type contacts (see Fig. 6), confirms that the SiO$_x$ layer no longer allows for efficient tunneling when the SiO$_x$ thickness increases slightly beyond 1.6 nm, making them impractical for use in a solar cell. It also verifies that unlike the POLO contacts from ISFH [18], our contacts with > 1.6 nm SiO$_x$, after annealing at 850 °C, do not form sufficient pinholes within the SiO$_x$ layer to allow for direct carrier transport between the poly-Si layer and the *c*-Si substrate [11]. However, we do expect pinholes in SiO$_x$ if the contact is annealed at temperatures > 950 °C, enabling carrier conduction.

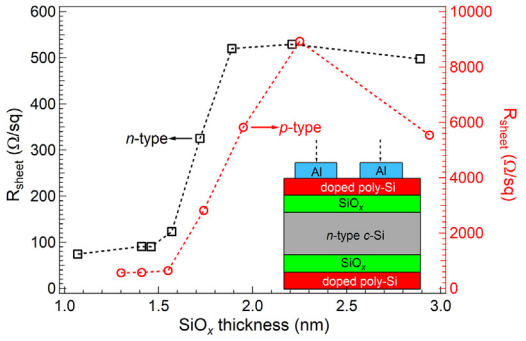

Fig. 7. Effect of thermally grown tunneling SiO_x thickness on the sheet resistivity of *n*- (□) and *p*-type (○) passivated contacts for test structures shown in the inset. The dotted arrows in the inset show the contact points for the probes during the measurement. The dashed lines are a guide to the eye.

Sheet resistivity of the contact is another important parameter, which affects lateral carrier conduction and, hence, cell efficiency. Fig. 7 shows the sheet resistivity of the *n*- and *p*-type passivated contacts with different SiO_x thicknesses determined using TLM analysis for test structures shown in the inset. For contacts with SiO_x thickness < 1.6 nm, the sheet resistivity is low and constant, ~90 and ~600 Ω/sq for *n*- and *p*-type contacts, respectively, but significantly increases with further increase in SiO_x thickness. It plateaus out at ~500 Ω/sq for the *n*-type contact with SiO_x thickness > 1.9 nm and is > 5500 Ω/sq for the *p*-type contact with a similar SiO_x thickness. We suspect that the variation of the sheet resistivity of the *p*-type contact between 5500 and 9000 Ω/sq is likely due to inaccuracies with the TLM analysis. For the contacts with the thicker SiO_x layer, the sheet resistivity values are high and constant due to the current being restricted to the thin, ~20 nm, poly-Si sheet, since the SiO_x layer is non-conducting (see Fig. 6). However, the sheet resistivity values for the contacts with SiO_x < 1.6 nm is much lower, since the SiO_x layer is conducting at these thicknesses (see Fig. 6). Thus, the effective conductive sheet in the TLM measurements for SiO_x < 1.6 nm consists of both the poly-Si sheet, as well as the sheet formed underneath the SiO_x layer within the underlying *c*-Si substrate due to dopant diffusion: dopant diffusion from the poly-Si layer into the *c*-Si substrate through the SiO_x layer for SiO_x thickness < 1.6 nm is apparent from the depth profiles shown in Figs. 4 and 5. This effectively creates two conductive sheets increasing the cross-sectional area for conduction, resulting in lower values of sheet resistivity. The effect of such a sheet, forming a diffused junction, on sheet resistivity of passivated contact is most accurately witnessed for the *p*-type contacts because the formation of the *p*-*n* diode with the *n*-type wafer restricts the current only to the poly-Si layer and the diffused sheet. In case of the *n*-type contact, a high-low junction is formed, which is a lower energy barrier for the charge carriers than a *p*-*n* junction. Therefore, for the *n*-type contact on a *n*-type *c*-Si wafer, the sheet resistivity of the wafer, which was ~280 Ω/sq, will also have some role to play in overall resistance measurement when the SiO_x layer is conducting. The significant reduction in sheet resistivity from ~5500 to ~600 Ω/sq for the *p*-type contacts (see Fig. 7) clearly shows that the diffused sheet is much more conductive than the poly-Si layer. This further signifies the importance of the formation of a diffused sheet underneath the SiO_x layer, within *c*-Si. Not only is it beneficial for obtaining lower lateral conductivity, but also for passivation as discussed in Section 3.1. The lower sheet resistivity is quite important in cell architectures with poly-Si passivated contacts at both the front- and the back-side of the solar cell [32].

3.3. Effect of SiO_x thickness on metallization-induced degradation

Fig. 8 shows the PL images for *n*- and *p*-type passivated contacts with different SiO_x thickness after metallization with Al. Darker regions in these PL images indicate lower carrier concentration, signifying greater metallization-induced damage. Note that the PL images of the samples were recorded for different shutter speeds of the CCD camera, and hence, the absolute brightness of no two samples should be directly

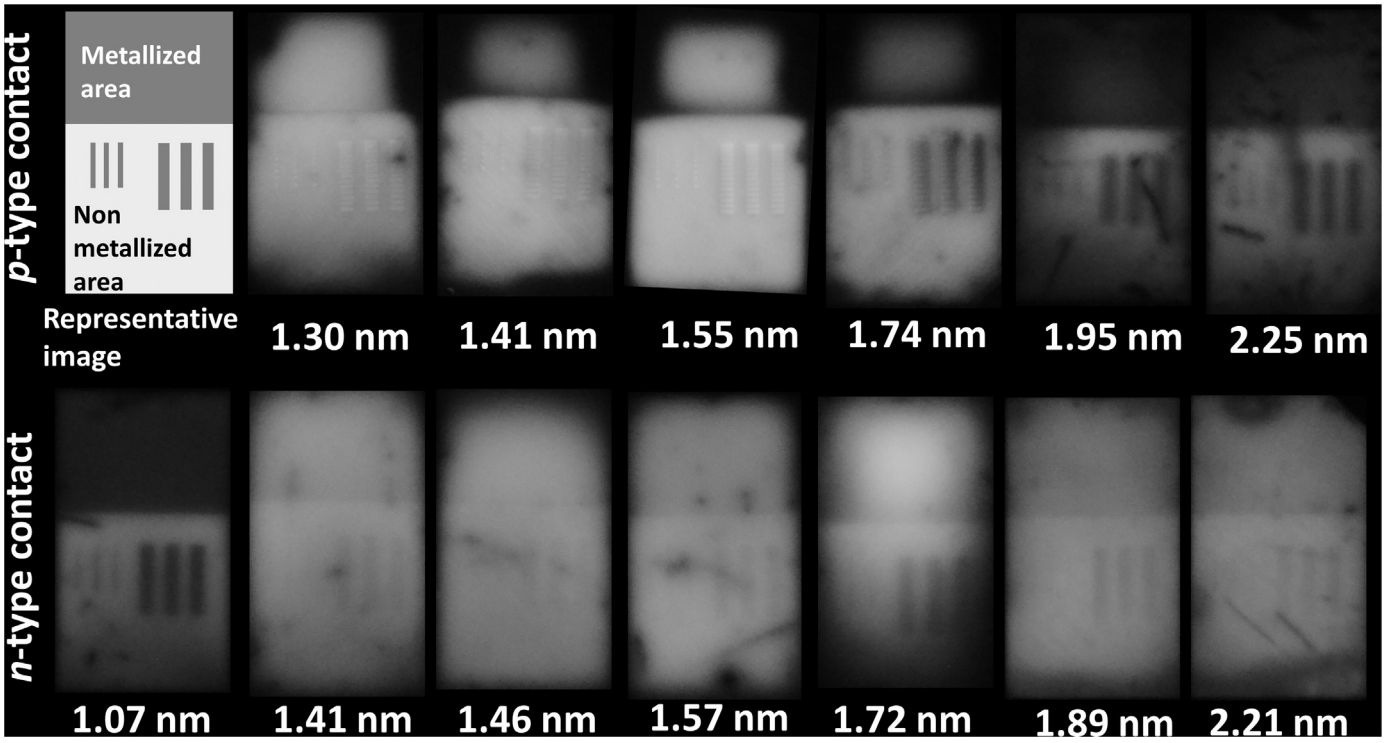

Fig. 8. Photoluminescence images of *p*- and *n*-type passivated contacts with different SiO_x thicknesses after metallization with ~1 μm thick Al deposited via *e*-beam evaporation. Also shown (top left) is a representative image of the metallized area on the samples. The images are obtained for different collection times for the detector.

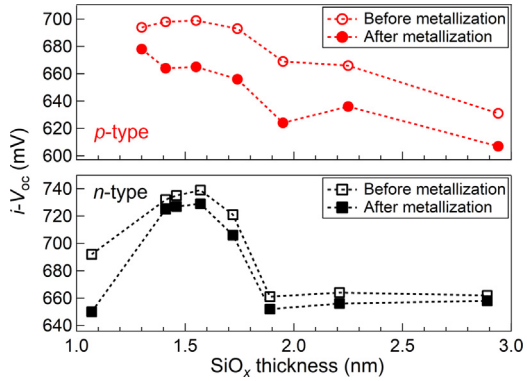

Fig. 9. Effect of thermally grown tunneling SiO_x thickness on the i-V_{oc} of samples before metallization of n- (□) and p-type (○) contacts, and after metallization of n- (■) and p-type (●) contacts. The dashed lines are a guide to the eye.

compared. Comparing the PL intensity of the metallized region on the sample, to the PL intensity prior to metallization, can be treated as a measure of the extent of metallization-induced degradation, and can be quantified as,

$$iV_{oc,\ \ before\ metal} - iV_{oc,\ \ after\ metal} = \frac{kT}{q} ln\left(\frac{I_{before\ metal}}{I_{after\ metal}}\right) \approx \frac{n'kT}{q} ln\left(\frac{J_{o,\ after\ \ metal}}{J_{o,\ before\ \ metal}}\right), \quad (3)$$

where, I is the measured PL intensity of the sample, T is the temperature of the sample, n' is the diode ideality factor, and k is the Boltzmann constant. Fig. 9 shows the i-V_{oc} values for the n- and p-type contacts before and after metallization. The i-V_{oc} values before metallization have been replotted from Fig. 1, while those after-metallization have been calculated using Eq. (3). The PL images for the p-type samples (see Fig. 8) were recorded without a mirror underneath the sample, which results in some optical effects. However, these optical effects were accounted for in the i-V_{oc} calculation after metallization. In Fig. 9, the i-V_{oc} for the n-type contact with the 1.07 nm thick SiO_x layer reduces by ~40 mV due to metallization, indicating significant metallization-induced degradation. However, the decrease in i-V_{oc} values for the n-type contacts with SiO_x thickness between 1.4 and 2.3 nm is between 7 and 15 mV indicating moderate metallization-induced degradation. In contrast, for the p-type contacts, the decrease in i-V_{oc} is between 30 to 45 mV, indicating significant metallization-induced degradation. The significant degradation for the n-type contact with 1.07 nm SiO_x is likely because such a thin SiO_x layer does not provide a sufficient barrier for creation of metal-induced defects in the c-Si substrate. Following that argument, one would expect the thicker SiO_x layer to insulate the underlying c-Si from metallization damage better, which does not seem to be the case based on the data shown in Fig. 9.

We would like to point out that since V_{oc} is not an additive term, comparing the change in i-V_{oc} for samples which have very different pre-metallization i-V_{oc}, is not a completely accurate methodology for comparing the extent of metallization-induced degradation. For example, a change in i-V_{oc} due to metallization of −10 mV indicates much more significant metallization-induced damage on a sample with a pre-metallization i-V_{oc} of 660 mV, than on a sample with a pre-metallization i-V_{oc} of 740 mV. Instead, comparing the change in J_o due to metallization is much more accurate. We approximately estimate J_o from the i-V_{oc} changes (Eq. (3)) assuming diode ideality factor $n' = 1$. For the n-type contact with the highest i-V_{oc}, the i-V_{oc} drops from 739 to 729 mV, while the J_o increases from 2.0 to 3.7 fA/cm^2 due to metallization-induced degradation. Similarly, for the p-type contact, the i-V_{oc} drops from 699 to 665 mV, while the J_o increases from 18.3 to 116 fA/cm^2. This clearly shows that our p-type contacts are much more sensitive to metallization-induced damage than our n-type contacts. Since pre-metallization J_o cannot be determined for both the n- and p-type contacts over the entire investigated SiO_x thickness range (see Figs. 2 and 3), determining change in J_o due to metallization becomes challenging. Hence, based on the above explanation, we can infer that the samples with thicker SiO_x likely show a higher extent of metallization-induced degradation. Since the poly-Si film on each sample was deposited and processed identically, it is quite interesting to observe that the extent of metallization induced degradation is affected by the buried SiO_x thickness. In order to understand the results shown in Fig. 8, we compared our results with studies on metallization of passivated emitter rear contact (PERC) solar cells [33]. For cells with diffused emitters such as the PERC architecture, it has been shown that better passivation is obtained by lowering the surface dopant concentration, but for reducing metallization-induced degradation, the concentration of dopants right underneath the metal contacts needs to be high [31,33]. However, the SIMS profiles in Figs. 4 and 5 show that the surface concentration of dopants is very similar for contacts with different SiO_x thicknesses, and thus, metallization-induced degradation should be independent of SiO_x thickness. However, Al is known to have a detrimental effect on c-Si [34] and SiO_x [35], and hence, we hypothesize that the defect-sensitive, charge-separating depletion region is closer to the deposited Al for contacts with > 1.8 nm SiO_x than for those with the < 1.6 nm SiO_x, as the thicker SiO_x inhibits dopant diffusion from poly-Si into c-Si to a greater extent (see Figs. 4 and 5). This likely makes the contacts with the thicker SiO_x layer more susceptible to metallization-induced degradation.

4. Conclusions

We have studied the effect of the thickness of thermally-grown SiO_x on passivated contact performance for c-Si solar cells. For obtaining excellent passivation of the c-Si wafer while making it less susceptible to metallization-induced degradation, the SiO_x thickness within the passivated contact should be within 1.4–1.6 nm for a contact annealing temperature of 850 °C. We speculate that the lower limit is to ensure good chemical passivation of the c-Si surface dangling bonds by the SiO_x layer, while the upper limit is to provide excellent field-effect passivation achieved by diffusion of dopants from the poly-Si layer through the SiO_x into the c-Si wafer creating a diffused junction. Even within the tunneling regime, SiO_x thickness affects the extent of dopant diffusion which has been verified by SIMS depth profiles for both boron- and phosphorous-doped contacts. This, in turn, influences the measured sheet resistivity of the contact. A marginal increase in the SiO_x thickness from 1.6 to 1.7 nm significantly increases the contact resistivity through the metal/poly-Si/SiO_x/c-Si stack, which indicates that SiO_x > 1.7 nm has poor carrier tunneling properties. Finally, the extent of metallization-induced degradation of the poly-Si/SiO_x contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly is not completely mitigated even for a ~3 nm thick SiO_x. We expect our results to change when the contact annealing temperature is increased to temperatures where pinholes in the SiO_x layer may form.

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work, or allow others to do so, for U.S. Government purposes. The authors thank Benjamin Lee, Ruy Sebastian Bonilla and Ronald Sinton for fruitful discussions, and Matthew Young for the dynamic SIMS measurements.

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.solmat.2018.05.011.

References

[1] F. Haase, F. Kiefer, S. Schäfer, C. Kruse, J. Krügener, R. Brendel, R. Peibst, Interdigitated back contact solar cells with polycrystalline silicon on oxide passivating contacts for both polarities, Jpn. J. Appl. Phys. 56 (2017) 08MB15.

[2] A. Richter, J. Benick, F. Feldmann, A. Fell, M. Hermle, S.W. Glunz, n-Type Si solar cells with passivating electron contact: identifying sources for efficiency limitations by wafer thickness and resistivity variation, Sol. Energy Mater. Sol. Cells 173 (2017) 96–105.

[3] B. Nemeth, D.L. Young, Y. Hao-Chih, V. LaSalvia, A.G. Norman, M. Page, B.G. Lee, P. Stradins, Low temperature Si/SiO_x/pc-Si passivated contacts to n-type Si solar cells, in: Proceedings of the 40th IEEE Photovoltaic Specialist Conference (PVSC), Denver, USA, 2014, pp. 3448–3452.

[4] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, S.W. Glunz, Efficient carrier-selective p- and n-contacts for Si solar cells, Sol. Energy Mater. Sol. Cells 131 (2014) 100–104.

[5] G. Yang, A. Ingenito, O. Isabella, M. Zeman, IBC c-Si solar cells based on ion-implanted poly-silicon passivating contacts, Sol. Energy Mater. Sol. Cells 158 (2016) 84–90.

[6] M.L. Green, E.P. Gusev, R. Degraeve, E.L. Garfunkel, Ultrathin (< 4 nm) SiO_2 and Si–O–N gate dielectric layers for silicon microelectronics: understanding the processing, structure, and physical and electrical limits, J. Appl. Phys. 90 (2001) 2057–2121.

[7] H.C. De Graaff, J.G. De Groot, The SIS tunnel emitter: a theory for emitters with thin interface layers, IEEE Trans. Electron Devices 26 (1979) 1771–1776.

[8] M.L. Green, T.W. Sorsch, G.L. Timp, D.A. Muller, B.E. Weir, P.J. Silverman, S.V. Moccio, Y.O. Kim, Understanding the limits of ultrathin SiO_2 and Si–O–N gate dielectrics for sub-50 nm CMOS, Microelectron. Eng. 48 (1999) 25–30.

[9] J. Gan, Polysilicon emitters for silicon concentrator solar cells, (Thesis), Stanford University, 1990.

[10] R. Peibst, U. Römer, K.R. Hofmann, B. Lim, T.F. Wietler, J. Krügener, N.P. Harder, R. Brendel, A simple model describing the symmetric *I-V* characteristics of p polycrystalline Si/n monocrystalline Si, and n polycrystalline Si/p monocrystalline Si junctions, IEEE J-PV 4 (2014) 841–850.

[11] T.F. Wietler, D. Tetzlaff, J. Krügener, M. Rienäcker, F. Haase, Y. Larionova, R. Brendel, R. Peibst, Pinhole density and contact resistivity of carrier selective junctions with polycrystalline silicon on oxide, Appl. Phys. Lett. 110 (2017) 253902.

[12] A. Aberle, S. Glunz, A. Stephens, M. Green, High-efficiency silicon solar cells: Si/SiO_2, interface parameters and their impact on device performance, Progress. Photovolt.: Res. Appl. 2 (1994) 265–273.

[13] A.G. Aberle, Surface passivation of crystalline silicon solar cells: a review, Prog. Photovolt.: Res. Appl. 8 (2000) 473–487.

[14] F.A. Lindholm, A. Neugroschel, M. Arienzo, P.A. Iles, Heavily doped polysilicon-contact solar cells, IEEE Electron Device Lett. 6 (1985) 363–365.

[15] E. Yablonovitch, T. Gmitter, R.M. Swanson, Y.H. Kwark, A 720 mV open circuit voltage SiO_x:c-Si: SiO_x double heterostructure solar cell, Appl. Phys. Lett. 47 (1985) 1211–1213.

[16] B. Nemeth, D.L. Young, M.R. Page, V. LaSalvia, S. Johnston, R. Reedy, P. Stradins, Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells, J. Mater. Res. 31 (2016) 671–681.

[17] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, J. Benick, M. Hermle, Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO_2 layers, Sol. Energy Mater. Sol. Cells 142 (2015) 123–127.

[18] U. Römer, R. Peibst, T. Ohrdes, B. Lim, J. Krügener, E. Bugiel, T. Wietler, R. Brendel, Recombination behavior and contact resistance of n^+ and p^+ poly-crystalline Si/mono-crystalline Si junctions, Sol. Energy Mater. Sol. Cells 131 (2014) 85–91.

[19] D.L. Young, B.G. Lee, D. Fogel, W. Nemeth, V. LaSalvia, S. Theingi, M. Page, M. Young, C. Perkins, P. Stradins, Gallium-Doped Poly-Si:Ga/SiO_2 Passivated Emitters to n-Cz Wafers With $iV_{oc} > 730$ mV, IEEE J-PV 7 (2017) 1640–1645.

[20] J. Stuckelberger, G. Nogay, P. Wyss, Q. Jeangros, C. Allebé, F. Debrot, X. Niquille, M. Ledinsky, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells, Sol. Energy Mater. Sol. Cells 158 (2016) 2–10.

[21] J.C. Bravman, G.L. Patton, J.D. Plummer, Structure and morphology of polycrystalline silicon-single crystal silicon interfaces, J. Appl. Phys. 57 (1985) 2779–2782.

[22] G.R. Wolstenholme, N. Jorgensen, P. Ashburn, G.R. Booker, An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations, J. Appl. Phys. 61 (1987) 225–233.

[23] R. Peibst, Y. Larionova, S. Reiter, M. Turcu, R. Brendel, D. Tetzlaff, J. Krügener, T. Wietler, U. Höhne, J.-.D. Kähler, H. Mehlich, S. Frigge, Implementation of n^+ and p^+ POLO Junctions on Front and Rear Side of Double-Side Contacted Industrial Silicon Solar Cells, in: Proceedings of the 32nd European Photovoltaic Solar Energy Conference and Exhibition, Munich, Germany, 2016, pp. 323–327.

[24] J.Y. Gan, R.M. Swanson, Polysilicon emitters for silicon concentrator solar cells, in: Proceedings of Photovoltaic Specialists Conference, Conference Record of the Twenty First IEEE, Florida, USA, 241, 1990, pp. 245–250.

[25] W. Kern, D. Puotinen, Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology, RCA Rev. 31 (1970) 187–206.

[26] K. Reinhardt, W. Kern, Handbook of Silicon Wafer Cleaning Technology, 2nd ed., William Andrew, Norwich, NY, USA, 2008.

[27] R.A. Sinton, A. Cuevas, M. Stuckings, Quasi-steady-state photoconductance, a new method for solar cell material and device characterization, in: Proceedings of Photovoltaic Specialists Conference, Conference Record of the Twenty Fifth IEEE, Washington, D.C., USA, 1996, pp. 457–460.

[28] B. Hallam, B. Tjahjono, T. Trupke, S. Wenham, Photoluminescence imaging for determining the spatially resolved implied open circuit voltage of silicon solar cells, J. Appl. Phys. 115 (2014) 044901.

[29] H. Berger, Contact resistance on diffused resistors, in: Solid-State Circuits Conference. Digest of Technical Papers. 1969 IEEE Internationa, Philadelphia, USA, 1969, pp. 160–161.

[30] D.L. Young, W. Nemeth, S. Grover, A. Norman, B.G. Lee, P. Stradins, Carrier-selective, passivated contacts for high efficiency silicon solar cells based on transparent conducting oxides, in: Proceedings of the 40th IEEE Photovoltaic Specialist Conference (PVSC), Denver, USA, 2014, pp. 1–5.

[31] D. Kane, R. Swanson, Measurement of the emitter saturation current by a contactless photoconductivity decay method, in: 18th IEEE Photovoltaic Specialists Conference, Las Vegas, USA, 1985, pp. 578–583.

[32] F. Feldmann, C. Reichel, R. Müller, M. Hermle, The application of poly-Si/SiO_x contacts as passivated top/rear contacts in Si solar cells, Sol. Energy Mater. Sol. Cells 159 (2017) 265–271.

[33] J. Zhao, Recent advances of high-efficiency single crystalline silicon solar cells in processing technologies and substrate materials, Sol. Energy Mater. Sol. Cells 82 (2004) 53–64.

[34] P.B. Ghate, Metallization for Very-Large-Scale Integrated Circuits, MRS Proceedings, **10,** 1981, pp. 371–395.

[35] T. Asuha, O. Yuasa, H. Kobayashi Maida, Effects of postmetallization annealing on ultrathin SiO_2 layer properties, Appl. Phys. Lett. 80 (2002) 4175–4177.