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Dopant segregation in SOI Schottky-barrier MOSFETs

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Abstract

We present experimental results on silicon-on-insulator Schottky-barrier MOSFETs with fully silicided NiSi source and drain contacts. Dopant segregation during silicidation was used to improve the device characteristics: on-currents, significantly higher than without dopant segregation as well as an almost ideal off-state are demonstrated in n-type as well as p-type SB-MOSFETs. Temperature dependent measurements show that the effective Schottky-barrier height in devices with segregation can be strongly lowered. In addition, we investigate the dopant segregation technique with simulations. Comparing simulations with experiments it turns out that the spatial extend of the segregation layer is on the few nanometer scale which is necessary for ultimately scaled devices. Furthermore, the use of ultrathin-body SOI in combination with ultrathin gate oxides results in an even further increased transmission through the Schottky barriers and consequently leads to strongly improved device characteristics. As a result, the dopant segregation technique greatly relaxes the requirement of low Schottky-barrier silicides for high performance transistor devices.

Keywords: Schottky barrier; Dopant segregation; Silicon-on-insulator; Barrier lowering

1. Introduction

Schottky-barrier (SB) MOSFETs have recently attracted a renewed interest as an alternative to conventional MOSFETs with doped source and drain contacts [1–5]. This interest stems from the fact that the requirements on the source and drain electrodes in terms of conductivity and abruptness can hardly be met with doped contacts in the very near future. Highly conductive contacts with almost ideal abruptness can on the other hand be realized by replacing the doped semiconductor contacts with metallic ones. In particular, silicides have received a lot of attention since their processing is compatible with CMOS technology and their formation requires only a small thermal budget. However, at a metal–semiconductor interface a Schottky barrier builds up and it is this barrier that determines the injection of carriers from the source contact into the channel. Since typical SB heights are significantly larger than a few k_BT the electrical characteristics of SB-MOSFETs are to a large extend determined by the tunneling probability of carriers through the Schottky barrier. Fig. 1 shows a typical transfer characteristic of an SB-MOSFET (black curve) and a conventional MOSFET (gray dashed curve). Looking at the conduction band profile as depicted in the inset of Fig. 1 it becomes apparent that as soon as the gate pushes the conduction band below the Schottky barrier the increase of current is determined by the change of the tunneling probability with changing gate voltage. As a result, SB-MOSFETs usually exhibit an inferior switching behavior with large inverse subthreshold slopes and smaller on-currents if compared to conventional devices with doped source and drain contacts [6]. Therefore, in order to make SB-MOSFETs a viable alternative to conventional devices the tunneling probability of carriers through the Schottky barrier has to be strongly

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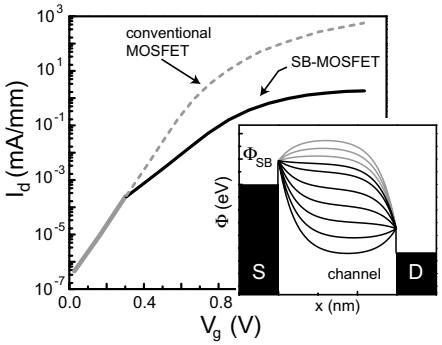

Fig. 1. Typical transfer characteristic of a conventional (gray dahsed line) and an SB-MOSFET. The inset shows the conduction band profile along the direction of current transport.

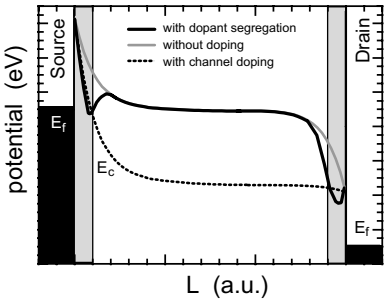

Fig. 2. Conduction band profile of an n-type SB-MOSFET without channel doping (gray line), with a uniform channel doping (dotted black line) and with highly doped interface layers (donors). These layers render the Schottky barriers highly transmissive without shifting the threshold voltage.

increased. Using dopant segregation during silicidation it has recently been shown that the performance of SB-MOSFETs can be significantly increased [6–8] and devices were experimentally demonstrated that exhibit an almost ideal off-state and improved on-state. Here we investigate the technique of dopant segregation in more detail and present experimental as well as simulation results on the electrical behavior of fully-depleted SOI SB-MOSFETs with dopant segregation.

2. Dopant segregation during silicidation

A proper ohmic contact between a metal and a semiconductor is usually made by heavily doping the semiconductor which yields a thin, highly transmissive Schottky barrier. However, as will be discussed in detail below, in a fully-depleted SOI device doping the semiconductor, i.e. the channel of the FET, results only in a shift of the threshold voltage. The injection of carriers, however, is the same such that the inverse subthreshold slope and the on-current at the same gate voltage overdrive remain unchanged. What is needed in order to improve the device behavior without shifting the threshold voltage is a non-uniform doping profile with highly doped semiconductor portions only at the interfaces between the contact electrodes and the channel. For an n-type SB-MOSFET this scenario is schematically shown in Fig. 2 which shows the conduction band profile along the direction of current transport. In case of a highly doped interface layer and provided the layer has an appropriate spatial extend a strong band bending can be expected that makes the Schottky barrier thinner thereby promoting the tunneling of carriers through the barrier. Such non-uniform doping profiles can be realized with the technique of dopant segregation during silicidation. Consider a bulk silicon sample into which arsenic or boron has been implanted. If the sample is coated with nickel and if subsequently the entire implanted part of the silicon sample is nickel-silicided the dopants redistribute and are piled-up at the silicide–silicon interface. A band bending rendering the Schottky barrier thin for electron (hole) injection results in case of arsenic (boron).

Whether dopant redistribution occurs or not is determined by the diffusivity and solid solubility of the dopants in the silicide and the presence of point defects at the silicide–silicon interface. In case of the NiSi phase, nickel atoms are the moving species, supplied by the diffusion through the growing silicide layer to the silicide–silicon interface, because the covalent bonds between the silicon atoms are softened by the diffusion of nickel atoms [9]. A significant change of volume is involved when the silicide is formed, which leads to a high strain at the interface. As a result, point defects (self-interstitial or vacancies) can be generated in order to partially relieve the stress. Due to the formation of vacancies, the diffusivity of arsenic in silicon is enhanced and arsenic moves towards the interface where it piles up at the moving interface between the silicide and the silicon. In case of dopant segregation during silicidation, the high density of strain-induced point defects can lead to a local dopant concentration higher than the solid solubility [9]. Due to its low silicon consumption, scalability to very small dimensions and due to its rather low formation temperature we will exclusively concentrate on nickel silicide in the following.

The occurrence of dopant segregation in the NiSi–silicon system was confirmed by a secondary ion mass spectroscopy (SIMS) investigation of bulk silicon samples which were implanted with arsenic and boron and subsequently the whole implanted area was fully silicided. Fig. 3 shows the depth distribution of arsenic (a) and boron (b) as measured by time-of-flight SIMS. The resulting depth profiles indicate that dopant segregation occurs at the NiSi–silicon interface for both, arsenic and boron. In case of arsenic, the dopant concentration exceeds $1\times10^{20}\,\mathrm{cm}^{-3}$ for an initial implantation dose larger than $5\times10^{14}\,\mathrm{cm}^{-2}$ (see Fig. 3a). There are three As peaks in the SIMS profile. The first one corresponds to the initial implantation peak and the second one may be due to the formation of different nickel silicide phases (such as Ni_3Si_2). The pronounced peak at a depth of ~100 nm, however, corresponds to the silicide–silicon interface indicating that the initially implanted region is totally silicided. In case of boron, the dopant concentration of boron at the

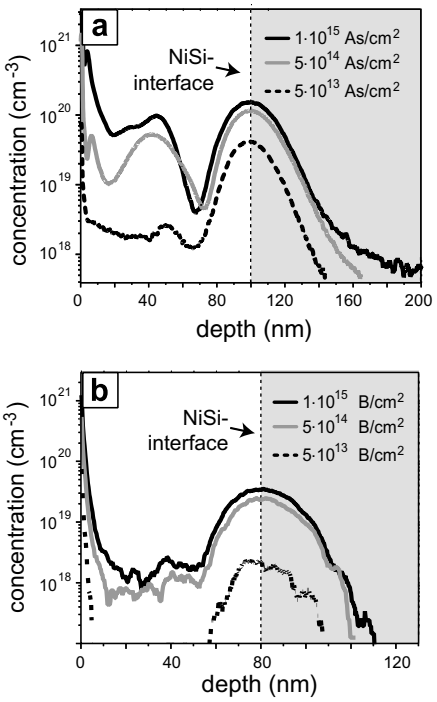

Fig. 3. SIMS profiles of the dopant distribution in NiSi/Si test samples being implanted with (a) arsenic and (b) boron. A segregation of dopants can be seen at the interface between the NiSi and the Si.

NiSi–silicon interface is almost one order of magnitude smaller for the same initial implantation dose if compared to the case of arsenic (see Fig. 3b). Moreover, no other peaks of boron in the silicide film and a larger out-diffusion length into the silicon can be observed. This may be attributed to the higher diffusivity of boron in both, silicon and the silicide. The SIMS measurements show dopant profiles comparable with conventional source/drain regions formed by standard ion implantation and thermal activation. However, it has been shown in Ref. [10] that dopant segregation during nickel silicidation at low temperatures does not change the long dopant tail of an arsenic or boron doping profile that has been activated with a high temperature spike anneal prior to silicidation, meaning that the silicidation does not result in a broadening of the dopant distribution profile. In our device fabrication we also employ a low temperature silicidation step. The important difference to Ref. [10] and to the bulk-silicon test samples is that firstly, no dopant activation has been done before the silicidation avoiding thermally activated dopant diffusion. Secondly, the junction to the channel is perpendicular to the implantation direction as indicated in Fig. 4 and this has significant consequences on the dopant distribution and the segregation behavior: The dopants are confined to the thin silicon layer since the neighboring SiO_2 layers act as diffusion barriers and sink of points defects, which significantly decrease the out-diffusion of dopants. In addition, the lateral doping profile falls off very rapidly since the gate acts as a mask for the dopants that are implanted vertically. Hence, long dopant tails as in the bulk case of Fig. 3 can

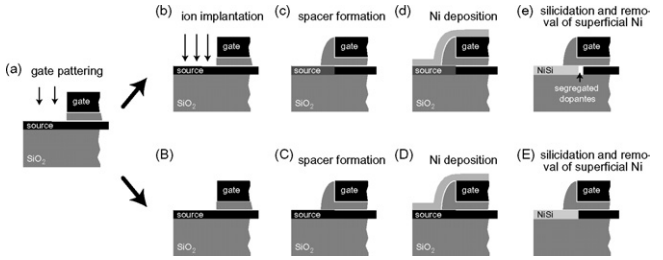

Fig. 4. Schematics of the fabrication process of SB-MOSFETs with dopant segregation (upper part) and the control samples (lower part). (a) After the gate stack formation, arsenic/boron is implanted into the source/drain areas in case of the segregation devices followed by the gate spacer formation. Subsequently nickel is deposited and the source/drain areas of the segregation device and control samples fully silicided.

be avoided by the geometrical constraints and we expect steep dopant profiles at the NiSi–silicon interface as has been experimentally verified for dopant segregation at the $CoSi_2$/silicon interface [7,11].

3. Device fabrication

Commercially available 4 in. silicon-on-insulator (SOI) wafers with a p-type doping of $1 \times 10^{15}\,cm^{-3}$ are used for the realization of thin-body SOI SB-MOSFETs with dopant segregation. To this end, the SOI is first thinned to a desired thickness of 25 nm by a cycle of dry/wet thermal oxidation, followed by diluted HF stripping. After a standard mesa isolation and RCA cleaning, a ~3.7 nm thick gate oxide was grown using wet oxidation at 600 °C for 1 h [12]. This wet oxidation scheme provides high-quality oxides while leaving the thermal budget as small as possible. A low gate leakage current density and a near ideal inverse subthreshold slope of fabricated MOSFET devices confirm that the oxidation process yields oxides comparable with high temperature oxides grown in dry oxygen in agreement with the results of Ref. [12]. Two hundred nanometer n-type poly-Si and 50 nm SiO_2 are deposited immediately after the gate oxidation using low-pressure chemical vapor deposition. The 50 nm SiO_2 on top of the poly-Si is patterned with optical lithography, followed by reactive ion etching (RIE). The poly-Si etching is done by inductively coupled plasma (ICP)-RIE using an HBr plasma which yields a very high selectivity between silicon and SiO_2 allowing for an exact etch stop and sharp edges. Two series of devices are fabricated. Devices with dopant segregation – called hereafter 'segregation devices' – are implanted with either arsenic or boron (see upper part of Fig. 4); control samples are left without any implantation (lower part of Fig. 4). To be specific, in case of the segregation devices, arsenic is implanted at 5 keV with a dose of $5 \times 10^{14}\,cm^{-2}$ leading to an implantation depth of approximately 8 nm; boron is implanted at 2 keV with a dose of $3 \times 10^{15}\,cm^{-2}$ with an implantation depth of 10 nm. Fig. 4 shows a schematic illustration of the fabrication process. After the source/drain implantation of the segregation devices, gate spacers are formed and nickel is deposited on both, the segregation and the control

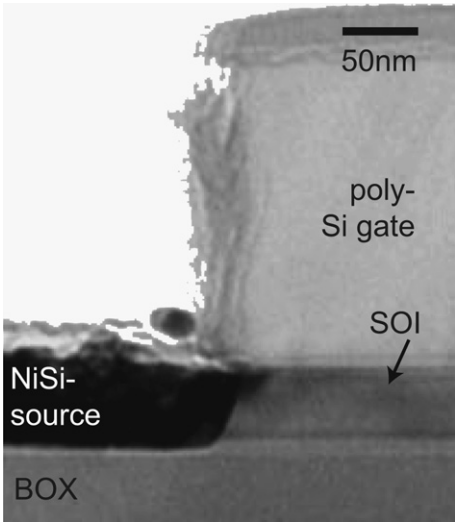

Fig. 5. Cross-sectional TEM image of a SB-MOSFET showing the silicide–silicon interface in the channel region which ensures a good gate control over the Schottky barrier and the dopant segregation layer at the contact-channel interface.

samples. Subsequently, the entire source/drain areas are fully silicided. It is important to note, that the implantation is done before the spacer formation since the dopants underneath the spacer are piled up by the moving silicide/silicon front. For the silicidation step, a temperature of 450 °C and a time of 20 s is chosen in case of the arsenic implanted and the control devices; 30 s are chosen to silicide the contacts of the boron implanted devices. This facilitates the encroachment of NiSi towards the channel beginning and hence the occurrence of dopant segregation (schematically illustrated in Fig. 4e). Subsequently, the unreacted nickel is selectively removed using Piranha. Fig. 5 shows a cross-sectional TEM image of a readily fabricated device with 25 nm SOI thickness. One can clearly see the NiSi encroachment underneath the spacer towards the channel region. No void can be seen between the contact end and the beginning of the gated channel region.

4. Measurements and discussion

Fig. 6 shows typical substhreshold characteristics of a control sample (without dopant segregation). An ambipolar behavior – typical of Schottky-barrier MOSFETs – is observed. In the n-channel operation region (towards positive gate bias), the subthreshold slope is $S_{(iii)} = 250$ mV/dec, exceeding 60 mV/dec by far since the change of drain current is determined by tunneling rather than thermal emission. In the p-channel operation region (towards negative gate bias), two subthreshold slopes can be seen with $S_{(ii)} = 70$ mV/dec and $S_{(i)} = 330$ mV/dec. $S_{(ii)}$ is close to the thermal limit meaning that the current in this gate voltage range is determined by so-called bulk-switching, i.e. thermal emission of holes over the potential barrier of the valence band at the source end of the device [6]. For more negative V_{gs} the current eventually is dominated by

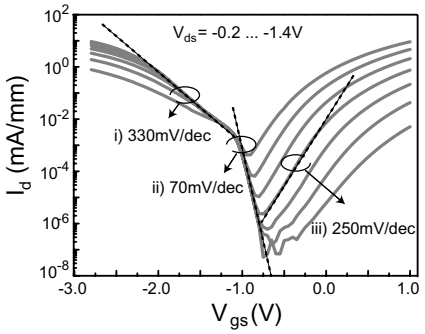

Fig. 6. Transfer characteristics of a SB-MOSFET without dopant segregation. The channel length and width are $L = 2$ μm and $W = 40$ μm, respectively. Two different slopes are observed on the p-side branch.

tunneling through the Schottky barrier for holes which manifests itself in a subthreshold slope of $S_{(iii)} = 330$ mV/dec. Such a behavior with two slopes on one branch of the ambipolar characteristics can be explained by a Fermi level pinning which is not at midgap. For NiSi the Fermi level pinning at the NiSi–silicon interface is indeed asymmetric with a barrier for holes of $\Phi^{h}_{SB} = 0.48$ eV and for electrons of $\Phi^{e}_{SB} = 0.64$ eV [13]. The large inverse subthreshold slopes observed are highly undesirable from an application point of view since in order to lower the power consumption of integrated circuits the operational voltage has to be reduced while leaving the ratio between on- and off-current of the devices constant.

Fig. 7a shows transfer characteristics of a SB-MOSFET with arsenic segregation. The ambipolar operation can still

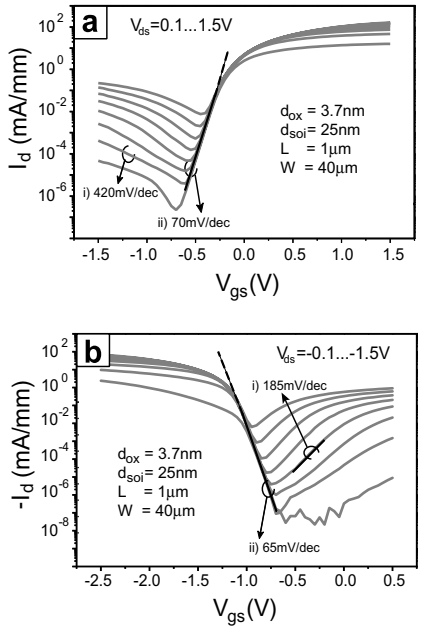

Fig. 7. Transfer characteristics of SB-MOSFETs with dopant segregation; the channel length $L = 1$ μm, width $W = 40$ μm and the oxide thickness and the SOI thickness are $d_{ox} = 3.7$ nm and $d_{si} = 25$ nm in both cases. (a) shows a device with 5 keV As^+ implantation at a dose of 5×10^{14} cm^{-2}. (b) shows a device with B^+ implantation at 2 keV and a dose of 3×10^{15} cm^{-2}.

be observed but the p-type branch is significantly suppressed and the on-current in the n-type branch has almost increased by one order of magnitude. However, the most pronounced difference of the device with dopant segregation if compared to the device without dopant segregation (cf. Fig. 6) is the inverse subthreshold slope of the n-type branch: $S_{(ii)} = 70$ mV/dec which is close to the thermal limit. In the p-type branch an inverse subthreshold slope of $S_{(i)} = 300$ mV/dec can be extracted from the characteristics. Fig. 7b shows transfer characteristics of a SB-MOSFET device with boron segregation. A similar behavior can be observed as in the case of the arsenic device: The on-current has increased approximately by a factor of 10 in the p-type branch and the n-type leakage has been decreased. But most importantly the inverse subthreshold slope of the p-type branch has improved to 65 mV/dec (see gate voltage region denoted with (ii) in Fig. 7b). However, looking at the output characteristics as shown in Fig. 8a and b a difference between the arsenic and the boron device becomes apparent. While the arsenic device shows a linear increase of current for small bias (Fig. 8a), typical of a conventional MOSFET, the boron device exhibits the non-linear increase of current for small drain-source voltages usually observed in SB-MOSFETs. The reason for this is that in case of the arsenic device the dopant concentration in the segregation layer is larger as compared to the boron device. As will become clear below the high dopant concentration in the arsenic device results in a strongly reduced effective Schottky-barrier height. In turn, off- as well as on-state characteristics show similar behavior as in a conventional device. On the other hand, in case of the boron device the dopant concentration is lower and hence the effective Schottky barrier is reduced less effectively. As a consequence, the off-state of the boron device is determined by thermal emission as indicated by a slope of 65 mV/dec whereas the on-state still shows the typical SB-MOSFET behavior.

The change from a Schottky-barrier device with ambipolar conduction and a large inverse subthreshold slope (see Fig. 6) to an n- or p-type transistor with increased on-current and almost ideal subthreshold behavior can be explained by looking at the conduction band profiles at the source Schottky contact for four different gate voltages as displayed in Fig. 9. For simplicity, we focus on the n-type transistor only but the same arguments also apply to a p-type transistor. Here, the dashed black lines (denoted 1 and 2) belong to potential distributions in the device's off-state and the gray straight lines to the on-state of the transistor (denoted 3 and 4). In case of a Schottky-barrier device without dopant segregation, the change of current with changing V_{gs} is mainly determined by an increasing tunneling probability through the source Schottky barrier as was already discussed in detail above (see the conduction band profiles in the inset of Fig. 1). Hence, the inverse subthreshold slope is rather large and the on-current low. On the other hand, the segregation layer in a device with dopant segregation leads to a strong band bending at the contact channel interface as illustrated in Fig. 9. Thus, the Schottky barrier has become so thin that the tunneling probability is strongly increased. As a result, the current in the device's off-state is not determined by the actual Schottky barrier anymore but now rather by the bulk potential in the channel similar to a conventional MOSFET. In turn, since this bulk potential follows one-to-one to changes in the gate voltage (in a fully-depleted device) this gives rise to an inverse subthreshold slope close to the thermal limit. One can associate to each gate voltage an effective Schottky barrier Φ_{SB}^{eff} as shown in Fig. 9. This means that in the off-state the segregation layer leads to an effective Schottky-barrier height which is below the bulk potential barrier in the entire off-state of the transistor. Furthermore, the on-state current will be significantly

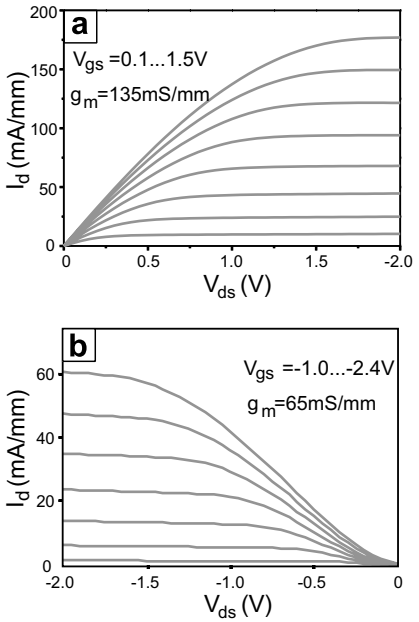

Fig. 8. Output characteristics of SB-MOSFETs with dopant segregation; (a) shows the arsenic segregation device which exhibits a linear increase of current for small bias. In contrast, the boron segregation device and (b) shows a non-linear increase of current, typical of SB-MOSFETs.

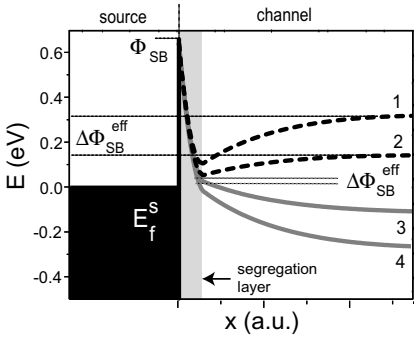

Fig. 9. Conduction band profile of the source Schottky barrier for four different gate voltages. The black dashed curves belong to the device's off-state, the gray curves to the on-state of the transistor.

increased as experimentally observed. However, in the on-state, the effective Schottky-barrier height will determine the current and the exact current level that is achievable then depends on the gate oxide and SOI layer thicknesses as will discussed in Section 5.2.

In principle, the same situation concerning the effect of the segregation layer on the Schottky barrier also occurs in devices with boron segregation. The only difference is that the segregation layer now consists of acceptors leading to a strong band bending upwards such that hole injection into the valence band is promoted in this case. However, in the particular case shown in Fig. 7b, the doping concentration for boron is only large enough to decrease the effective Schottky-barrier height in order to allow for an almost ideal off-state, but there is still a substantial barrier present at the silicide–silicon interface. A somewhat higher initial implantation dose would be required in order to increase the boron concentration in the segregation layer.

4.1. Temperature dependent measurements

In order to further study the impact of dopant segregation on the Schottky-barrier height and in particular to investigate the effective Schottky-barrier height as a function of gate voltage, we performed temperature dependent measurements of the DC characteristics. The following two-dimensional thermionic emission equation is used to extract the effective Schottky-barrier height from the measured data [14]:

$$I = WA^{**}T^{3/2}\exp\left(\frac{-q\Phi_{SB}^{eff}}{k_BT}\right)\exp\left(\frac{qV_{ds}}{k_BT}-1\right) \quad (1)$$

where Φ_{SB}^{eff} is the effective Schottky-barrier height, W is channel width, and A^{**} is the 2D effective Richardson constant; typical Arrhenius plots are employed to extract Φ_{SB}^{eff} (see [15] and references therein). Fig. 10 shows the extracted effective Schottky-barrier height as a function of gate voltage at $V_{ds} = 0.1$ V. In the device's off-state the effective Schottky-barrier height exhibits an almost one-to-one change with increasing gate voltage (for $V_{gs} < 0$ V). The reason for this is that due to the dopant segregation

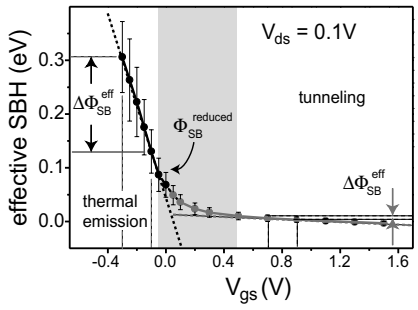

Fig. 10. Effective Schottky-barrier height of the arsenic device as a function of V_{gs} as extracted from temperature dependent measurements; the error bars result from the uncertainty in determining the slope from the Arrhenius plots.

the Schottky barrier has become so thin that it is not the Schottky barrier but the bulk potential inside the channel (which exhibits a one-to-one change with gate voltage in the off-state of fully-depleted devices) that determines the current flow, similar to a conventional MOSFET. This is exactly the behavior that was already discussed in the last section and it is this fact that gives rise to an inverse subthreshold slope close to the thermal limit as observed experimentally. On the other hand, once the device goes into the on-state ($V_{gs} > 0.3$ V), the effective Schottky-barrier height continues to decrease but with a much smaller slope (indicated in Fig. 10). The reason for this can be inferred from the conduction band profile shown in Fig. 9: For large V_{gs} (gray curves 3 and 4) the conduction band further away from the source contact is pushed below the kink in the segregation layer essentially leaving behind a reduced Schottky barrier for electron injection which is much smaller than the original barrier height. The slightly increasing transparency of this reduced Schottky barrier with changing V_{gs} on the other hand is due to the thinning of the potential distribution of the Schottky barrier with increasing gate voltage and hence is a consequence of the electrostatic control of the gate over the channel. While lowering the effective Schottky-barrier height for electron injection, the segregation layer leads to an increased Schottky barrier for hole injection resulting in a suppression of the hole leakage current as was already discussed above. In essence, the bands in a device with dopant segregation resemble the band profile in a device without dopant segregation but with a much smaller original Schottky-barrier height. The new, reduced Schottky barrier due to dopant segregation can be extracted from Fig. 10 which is determined by the point where the Φ_{SB}^{eff}–V_{gs} curve starts to deviate from the one-to-one behavior, i.e. the point where the character of the effective Schottky barrier changes from the bulk potential-like behavior to the reduced Schottky barrier [16]. In the present case the reduced Schottky barrier is found to be ~0.1 eV significantly lower than the original Schottky-barrier height of NiSi which is 0.64 eV for electron injection.

From the temperature dependent measurements we also extracted the inverse subthreshold slopes (for $V_{ds} = 0.1$ eV) at a constant current level below threshold. The result is plotted in Fig. 11 (a). As can be seen in the figure, there exists a transition region with a constant, temperature-independent inverse subthreshold slope between 120 K and 200 K. Above and below this transition region a linear relation between S and temperature can be observed. This unusual behavior can be explained as follows: For temperatures above 200 K and in case of a significantly low reduced Schottky-barrier height – as is achieved with dopant segregation – this new, reduced Schottky barrier is on the order of a few k_BT only and therefore an off-state as in a conventional MOSFET is obtained. Hence, the inverse subthreshold slope is given as $S = \frac{k_BT}{q}\ln(10)$ leading to a linear $S(T)$ as illustrated in Fig. 11b (dotted black line). However, if the temperature is low enough, the reduced

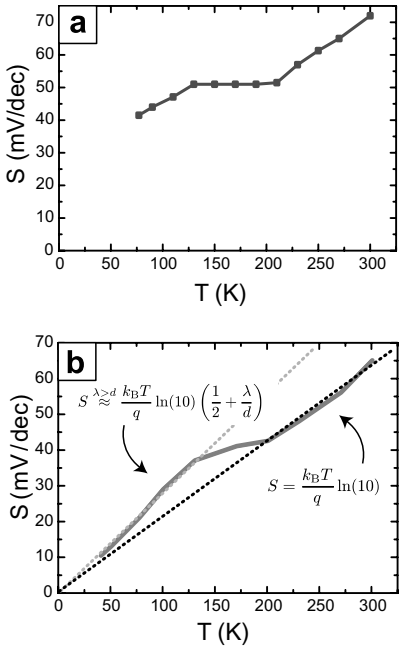

Fig. 11. Inverse subthreshold slope versus temperature as extracted from experimental data (a) as well as simulations (b). (b) also shows the expected $S(T)$ for thermal emission (dotted black line) and for tunneling (dotted gray line) as the dominant process for carrier injection.

Schottky-barrier height becomes much larger than $k_B T$. In a recent publication we showed that in this case the inverse subthreshold slope is given by $S \approx \frac{k_B T}{q} \ln(10)(\frac{1}{2} + \frac{\lambda}{d})$ where λ is the length scale on which potential variations in the channel area are screened (for details see below) and $d \approx 4$ nm is the thickness of the Schottky barrier for which the tunneling probability is significantly suppressed [17]. This means, if tunneling is the dominant process of carrier injection, a linear relation between S and the temperature is obtained, too. However, the increase of S with increasing temperature can be much larger and depends mainly on the screening length λ. This scenario is depicted in Fig. 11b (dotted gray line) and leads to the overall unusual $S(T)$ curve. In the transition region, the carrier injection changes its character from mainly thermionic (above 200 K) to mainly tunneling (below 120 K). The gray straight line in Fig. 11 belongs to a simulation using the approach described in the subsequent section. A Schottky barrier of 0.1 eV was assumed in the simulation leading to a transition region in the same range as experimentally observed. This reconfirms that with dopant segregation in the arsenic device a significant lowering of the Schottky-barrier height to a new reduced barrier of ~0.1 eV is achieved.

5. Simulations of SB-MOSFETs with dopant segregation

In order to get a better understanding of the phenomena involved in the electronic transport of SB-MOSFETs we have performed quantum simulations of SB-MOSFETs adapting the approach of Ref. [6]. Although the model is fairly simple it can reproduce the main experimental observations. A central ingredient of this approach is the reduction of the electrostatics of a fully-depleted SOI SB-MOSFET to a one-dimensional Poisson equation that captures the essential aspects of scaling of the oxide thickness d_{ox} and SOI thickness d_{si} as well as the appearance of short channel effects in laterally scaled devices. This one-dimensional Poisson equation for the surface potential $\Phi_f(x)$ is given by [18]

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\Phi_f(x) - \Phi_g + \Phi_{bi}}{\lambda^2} = \frac{\rho_{tot}(x)}{\varepsilon_{si}} \tag{2}$$

where Φ_g and Φ_{bi} are the gate potential and the built-in potential, respectively. The screening length $\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} d_{ox} d_{si}}$ is the relevant length scale on which potential variations are being screened. It sensitively depends on the channel and gate oxide thicknesses, d_{si} and d_{ox}, respectively. Eq. (2) allows easy access to a number of insights. For instance, it can be seen that a uniform channel doping leads to a constant term on the right hand side of Eq. (2) that can be incorporated into Φ_{bi} and hence only causes a shift of the threshold voltage as has been discussed above. Furthermore, in the device's off-state the charge term on the right hand side of the equation becomes approximately constant. In this case, Eq. (2) can be solved analytically showing that potential variations such as the potential distribution of the Schottky barrier are exponentially screened on the length scale λ. In turn this means that the Schottky barrier can be made "thin", i.e. more transmissive, if ultrathin-body SOI and very thin gate oxides are being used. This observation has recently been verified experimentally [19].

The effect of dopant segregation is taken into account by a step-function-like doping profile with a spatial extent l_{seg} and a dopant concentration N_{seg} right at the silicide–silicon interface as depicted in the upper part of Fig. 12. The charge in and current through the device is calculated self-consistently using the non-equilibrium Green's function formalism together with the 1D Poisson equation

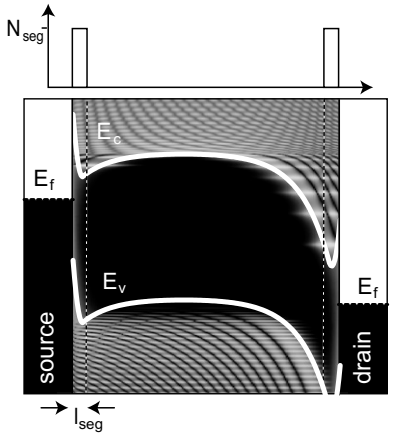

Fig. 12. Local density of states in an SB-MOSFET with dopant segregation. The segregation layer has been accounted for by a step-function-like doping concentration as illustrated in the upper part.

(2). To numerically compute the Green's functions we make use of Datta's approach [20]. We consider a one-dimensional finite difference scheme with lattice constant a and nearest neighbor hopping parameter t. A quadratic dispersion relation in the conduction and valence band is used. Because ultrathin-body SOI is considered, we assume that the first subband contributes most to the current and hence the expressions for charge and current are averaged over the direction of W only (see Ref. [21] for details). Higher subbands are accounted for by a numerical factor as in Ref. [22]. The main panel of Fig. 12 shows the local density of states in an n-type SB-MOSFET with segregation together with the conduction and valence band edges. It is apparent that the highly doped interface layer leads to strong band bending that renders the Schottky barrier thin and therefore easier to be tunneled through.

5.1. Asymmetric ambipolar characteristics

Looking at the linear output characteristics (Fig. 8a) and the almost ideal subthreshold behavior of the arsenic device, for instance, one could argue that the SB-MOSFET with arsenic segregation is rather a conventional MOSFET. It is important, however, to note that there is a difference between a conventional MOSFET and the present SB-MOSFETs with dopant segregation. This difference can be inferred from the leakage current, i.e. from the p-type branch of the n-type device (Fig. 7a) and the n-type branch of the p-type device (Fig. 7b), respectively. Although the leakage has been suppressed if compared to the ambipolar behavior of the SB-MOSFET (see Fig. 6) it still is significantly higher than in a conventional MOSFET. The reason for this is the small spatial extend of the segregation layer l_{seg}. In order to get an estimate of l_{seg} we simulated the current in the hole branch of an SB-MOSFETs with dopant segregation for various segregation layer thicknesses and doping concentrations. The following discussion is done for an n-type segregation device but also applies in case of a p-type transistor.

Fig. 13 shows the current at $V_{gs} = 0$ V and $V_{ds} = 1.0$ V as a function of l_{seg} for doping concentrations ranging from 1.2×10^{25} m^{-3} to 3×10^{26} cm^{-3}. One can clearly see in the figure that the higher the doping concentration the steeper the decrease of the current with increasing segregation length. The reason for this is that with increasing doping concentration the effective Schottky barrier for electron injection will decrease whereas the barrier for hole injection – responsible for the leakage current – increases accordingly; the same is true for increasing segregation length. If we now compare the experimental segregation device (with arsenic implantation) with the control sample a suppression of the current in the hole-branch of approximately two orders of magnitude is obtained in the segregation device. In turn, if one requires the hole current suppression to be two orders of magnitude a straight line can be drawn in Fig. 13 (dotted line). From the intersects of this line with the curve for the hole current as a function of l_{seg} one can

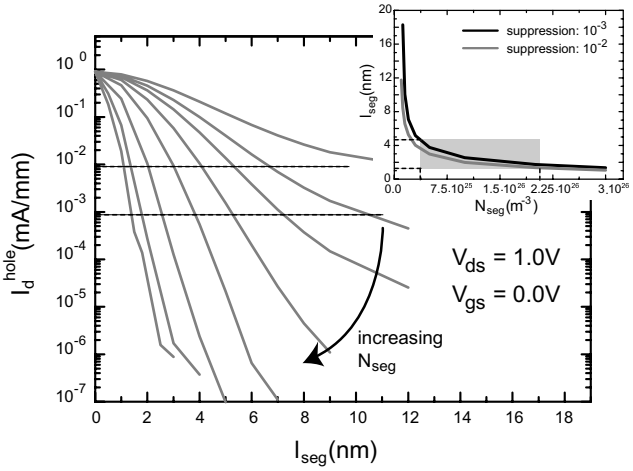

Fig. 13. Current as a function of the segregation length in the hole-branch of an n-type SB-MOSFET with dopant segregation for various doping concentrations. The inset shows the maximum l_{seg} as a function of N_{seg} leading to a current suppression of two and three orders of magnitude as extracted from the I_d–l_{seg} curves.

extract the maximum spatial extend of the segregation layer as a function of the doping concentration. This is plotted in the inset of Fig. 13 showing that the required segregation length, necessary to obtain two orders of magnitude suppression (gray line), rapidly increases if the doping concentration is below approximately 3×10^{25} m^{-3}. However, from the SIMS investigations we know that the doping concentration is rather large and is in the range illustrated with the gray shaded area in the inset of Fig. 13. Hence, the segregation length cannot be larger than a few nanometers, 2–4 nm to be specific. This is also true if a suppression of the hole current of three orders of magnitude would be assumed (black line in the inset).

The smallness of the segregation layer is an important aspect for the scalability of SB-MOSFETs with dopant segregation since in order to get highly conductive source/drain contacts the metal electrodes should extend up to the beginning of the channel. However, in this case l_{seg} must be as small as possible in order to facilitate the fabrication of ultrashort channel devices.

5.2. Dopant segregation in UTB SOI devices

In a recent paper we showed that the use of ultrathin-body SOI and very thin gate oxides is beneficial for the performance of SB-MOSFETs since the injection of carriers is significantly improved [19]. This is due to a much better gate control of the potential profile resulting in thin and transmissive Schottky barriers. Thus, it is appealing to incorporate dopant segregation into an ultrathin-body SOI device. We have therefore simulated transfer characteristics of SB-MOSFETs with dopant segregation ($N_{seg} = 2 \times 10^{20}$ cm^{-3}, $l_{seg} = 2$ nm) and a fixed Schottky barrier of 0.64 eV for two different SOI body and oxide thicknesses, namely (1) $d_{ox} = 1$ nm, $d_{si} = 5$ nm and (2) $d_{ox} = 5$ nm, $d_{si} = 25$ nm. In addition, we also simulated device charac-

teristics of control samples without dopant segregation, having the same geometrical parameters as the device (1) and (2). Since ballistic transport is assumed in the following in order to give an upper estimate of possible device performance the actual channel length is irrelevant as long as short channel effects are absent; a channel length of $L = 60$ nm in case of (1) and $L = 160$ nm in case of (2) was found to be sufficient to ensure long-channel behavior.

Fig. 14a shows transfer characteristics of two devices of type (1) and (2) without dopant segregation. A clear improvement in case of the device of type (1) can be seen which is due to the better gate control leading to an increased carrier injection [6]. Fig. 14b shows the transfer characteristics of two devices of type (1) (black line) and (2) (gray line) with dopant segregation. Both devices exhibit an almost ideal off-state showing that dopant segregation has effectively lowered the Schottky-barrier height. However, the on-state is significantly different with a much larger on-current in case of (1) with ultrathin-body SOI and ultrathin gate oxide as anticipated from the discussion above and the result shown in Fig. 14a. In other words, the reason for further improvement of the devices of type (1) is that due to the increased gate control over the potential distribution of the Schottky barrier, Φ_{SB}^{eff} can be further lowered even well in the on-state (see Ref. [23]). As a result, the dopant segregation technique greatly relaxes the requirements for low Schottky barrier electrode materials due to an increased tunneling probability through the Schottky barrier. In combination with ultrathin-body SOI and ultrathin gate oxides an even further improved on-state can be achieved allowing for high performance SB-MOSFET devices.

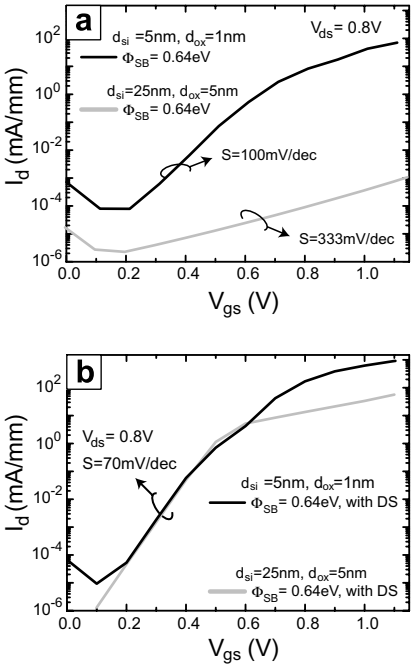

Fig. 14. (a) Transfer characteristics of SB-MOSFETs without dopant segregation for different sets of geometrical parameters. (b) shows transfer characteristics of the same two devices but with dopant segregation. A concentration of $N_{seg} = 2 \times 10^{20}$ cm^{-3} and a spatial extend of $l_{seg} = 2$ nm were assumed for the segregation layer. Geometrical parameters are as given in the figures.

6. Conclusion

In conclusion, we studied the impact of dopant segregation during silicidation on the performance of SOI SB-MOSFETs. It was shown that a highly doped interface layer results in a drastic reduction of the effective Schottky-barrier height for both, n- as well as p-type transistors. Experimental devices exhibit a significantly improved on- and off-state with an inverse subthreshold slope close to the thermal limit. Simulations show that the use of ultrathin-body SOI and ultrathin gate oxides enables a further improvement of the transistor's on-state due to a more substantial lowering of the effective Schottky-barrier height. Consequently, dopant segregation and ultrathin body/oxide devices allow to combine an excellent intrinsic performance with the specific advantages of SB-MOSFETs.

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