Midgap states in *a*-Si:H and *a*-SiGe:H *p-i-n* solar cells and Schottky junctions by capacitance techniques

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(Received 26 August 1991; accepted for publication 5 March 1992)

The midgap density of states (MGDOS) in *a*-SiGe:H alloys is investigated by capacitance measurements on *p-i-n* solar cells. Past work on thick *a*-Si:H Schottky barriers is extended to thin *a*-SiGe:H *p-i-n* cells. Four methods of determining the MGDOS from the measured capacitance are described, and each is applied to two *p-i-n* devices having 0% and 62% Ge in the *i* layers, respectively. The first method involves fitting an equivalent circuit model to the measured admittance. Close agreement is found over a wide range of temperature and frequency. The single junction model is shown to apply equally well to *p-i-n* and Schottky diodes, justifying the neglect of the *n-i* junction and thin doped layers in the *p-i-n* admittance analysis. A second method determines g_0 from the limiting capacitance at high temperature. The third and fourth methods extract g_0 from the dependence of capacitance on voltage bias. One of these is novel, presented here for the first time. Thus, a unique feature of this study is the application of several different capacitance methods to standard *p-i-n* solar cell devices. Agreement within $\pm 25\%$ is found among the values of the MGDOS from the four methods. The MGDOS increases exponentially from $(1\text{–}2)\times 10^{16}$ to $(3\text{–}4)\times 10^{17}/\text{cm}^3\,\text{eV}$ as the Ge increases from 0% to 62%, in general agreement with results of others.

I. INTRODUCTION

Despite the theoretical appeal of multijunction series-connected solar cells based on hydrogenated amorphous silicon and its alloys,[1,2] actual performance has been limited by the poor electronic properties of the low band gap *a*-SiGe:H alloys used in the rear or "scavenger" cell. The midgap density of states (MGDOS) strongly influences the recombination rate and the field profile within the device. Understanding and control of localized defects in amorphous silicon and its alloys is critical to improving the performance of such solar cells. The summary of a recent workshop on *a*-SiGe:H alloys[3] concluded that inadequate information and disagreement about midgap DOS are some of the factors which presently hinder development of *a*-SiGe:H solar cells. In particular, characterization of MGDOS in actual working *p-i-n* solar cells having *a*-SiGe:H *i* layers would be quite useful since changes in MGDOS could be directly related to changes in solar cell performance.[3] This work addresses those issues. The relation between MGDOS and Ge content in *a*-SiGe:H alloys is investigated by characterizing *p-i-n* solar cell devices, and results are compared to those reported from over a dozen other groups.

Numerous diagnostic techniques have been applied to characterize midgap states (i.e., deep levels) in semiconductors. Perhaps the simplest and most widely applied techniques are admittance measurements. The junction capacitance is directly related to the charge trapped in or released from midgap states as a consequence of time-varying excitation. The spatial and energetic distribution of states within the space charge region of a Schottky barrier or *p-n* junction is probed by varying the frequency (f), temperature (T), and bias voltage (V).

There are two basic methods of reducing the data and extracting the MGDOS: (1) equivalent circuit network analysis,[4–8] and (2) analytical admittance function method.[9,10] In the present work we unite and combine the two approaches. We show that the resulting expression for the capacitance has a clear physical interpretation under the simplifying assumption of the uniform MGDOS around the Fermi energy E_F (i.e., near midgap). This is a common assumption[4,5,8,11–13] for *a*-Si:H alloys and is clearly justified by our subsequent experimental results. The analysis is critically tested by using four methods to determine the MGDOS from experimental results.

An unusual feature of the present work is the use of *p-i-n* junctions to create the space-charge region. Most previous studies of *a*-Si:H alloys have used Schottky junctions[4–8,12,13] or crystalline silicon heterojunctions.[14,15] It has been suggested[16,17] that the interpretation of capacitance measurements on *p-i-n* cells can be obscured by space charge in the doped layers. We will show that this concern is unfounded. Use of *p-i-n* solar cells for characterization of *i* layer properties such as MGDOS, should be of interest for industrial laboratories which routinely fabricate operating devices.

II. SAMPLE FABRICATION AND MEASUREMENTS

A. Sample fabrication

The *p-i-n* devices were deposited by Hg-sensitized photo-chemical vapor deposition (CVD) as previously described.[18] The substrates were textured SnO_x and the back

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TABLE I. Device structure and *i* layer properties of samples which were characterized by circuit model fitting. All *p,n* layers nominally identical. All devices were deposited on SnO_x/glass substrates.

Run #	Device	*p-i*[a] buffer	Back contact	T_{DEP} (°C)	E_G[b] (eV)	*d* (μm)	Ge (%)
2415	*p-i-n*	GCL	ITO/Ag	205	1.74	0.56	0
3056[c]	Schottky	none	Mg/Al	230	1.75	0.58	0
2353	*p-i-n*	GCL	ITO/Ag	205	1.53	0.27	43
3188	*p-i-n*	Si	ITO/Ag	230	1.30	0.27	62
3196	*p-i-n*	Si	ITO/Ag	260	1.30	0.27	65

[a]GCL$\approx$150 Å graded *a*-SiC:H buffer; Si=100 Å *a*-Si:H buffer.
[b]E_G from Tauc plot on similarly deposited *i* layer film.
[c]#3056 had $\sim$50 Å Pt barrier on SnO_x.

contact was ITO/Ag. Cell area (A) was 0.28 cm^2. The *a*-Si:H *i* layers were deposited at 205 °C with a 4:1 He:SiH_4 ratio at 5 Torr. The *a*-SiGe:H *i* layers were deposited at 205, 230, or 260 °C with 10:1 H_2:(SiH_4+GeH_4) dilution at 5 Torr. Properties of the *a*-SiGe:H films and devices have been reported previously.[19–21] We also fabricated *a*-Si:H Schottky diodes with Pt as barrier contacts and Mg as ohmic contacts, (i.e., having no doped layers) for comparison to the *p-i-n* cells.

It is well established that thin buffer layers deposited between the *a* -SiC:H *p* layer and the *i* layer of *a*-Si:H[22–24] or *a*-SiGe:H[25] *p-i-n* cells reduces recombination near the *p-i* interface. The *a*-Si:H *p-i-n* device studied here in detail (#2415) had a graded carbon buffer layer (GCL) between the *p* and *i* layers, while the *a*-SiGe:H devices had either a GCL or an unalloyed *ungraded* *a*-Si:H buffer. Both buffers were approximately 100–150 Å thick. The device structure, *p-i* buffer, and *i* layer properties of devices analyzed in Sec. IV are given in Table I.

B. Capacitance measurements

The capacitance was measured with a Hewlett–Packard model 4274A LCR meter in the parallel admittance mode at frequencies from 0.1 to 100 kHz at temperatures from 0 to 200 °C. The rate of increase or decrease in temperature was typically 1 °C/min. Devices were at 0 V bias with δV=25 mV ac oscillator amplitude for $C(\omega,T)$ and $G(\omega,T)$ measurements. Bias voltage dependence was investigated from -2 to $+0.2$ V at constant ω, T.

We also performed measurements in the "drive-level" mode.[26] Experimentally, both the ac (δV) and dc (V_A) voltage amplitudes are varied *simultaneously* to maintain a constant maximum voltage; $\delta V + V_A = V_{MAX}$. The drive level technique differs from other capacitance measurements in that the amplitudes of the ac test signal and dc bias voltage can be comparable. For our drive level measurements, the capacitance was measured as V_A was varied from -0.15 to -0.030 V (reverse bias), and δV was varied from 0.15 to 0.030 V. Thus, the maximum positive voltage applied to the device (V_{MAX}) was maintained at 0 V for all pairs of ac and dc bias. The temperature or frequency was varied, and the entire procedure was repeated.

C. Preliminary film and device characterization

The position of the Fermi level (E_F) below the conduction band is an important parameter in admittance analysis. E_F is closely related to the activation energy (E_A) of the dark dc conductivity (σ_D) which is given by

$$\sigma_D=\sigma_0 \exp(-E_A/kT). \tag{1}$$

We find E_A=0.7 to 0.8 eV for *a*-Si:H films (band gap E_G=1.72–1.78 eV) and E_A=0.6 to 0.65 eV for *a*-SiGe:H films with Ge=60–65% (E_G=1.28–1.36 eV). Thus, E_A is a few kT above midgap in our films as commonly found by others. The prefactor σ_0 is typically 500–1500 S/cm. We apply a linear correction γT for the temperature dependence of the Fermi level[27,28] $E_F(T)=E_F(0)-\gamma T=E_A-\gamma T$. The coefficient γ is on the order of (2–4)k in *a*-Si:H (Ref. 27, 28) and *a*-SiGe:H (Ref. 29) where k is Boltzmann's constant. We will use $\gamma=2k$.

The *p-i-n* diode dynamic resistance (R_j) is related to the diode $J(V)$ characteristic by

$$R_j=\left(\frac{dV}{dJ}\right)\Big|_{V=0}=\frac{nkT}{qJ_0}, \tag{2}$$

where n and J_0 have their usual meanings as the diode quality factor and recombination current density. Equation (2) defines the small signal impedance of the junction portion of the diode.[5–7] The *a*-Si:H and *a*-SiGe:H *p-i-n* diodes were characterized as a function of voltage and temperature as previously described.[23] By defining J_0 at zero bias (V_A=0) as

$$J_0=J_{00}\exp(-qV_B/kT), \tag{3}$$

the saturation current J_{00} and qV_B are determined from an Arrhenius plot.[23] The barrier height qV_B is found to be a few kT greater than $E_G/2$ ($\sim$0.7 to 1.0 eV).

III. THEORY OF CAPACITANCE DUE TO MIDGAP STATES

In a previous work[30,31] we derived an expression for the ac capacitance at the external terminals of a *p-i-n* cell due to deep-lying states in the *i* layer under the simplifying assumption that the density of deep states is constant near the Fermi level. In this section, we repeat the key argu-

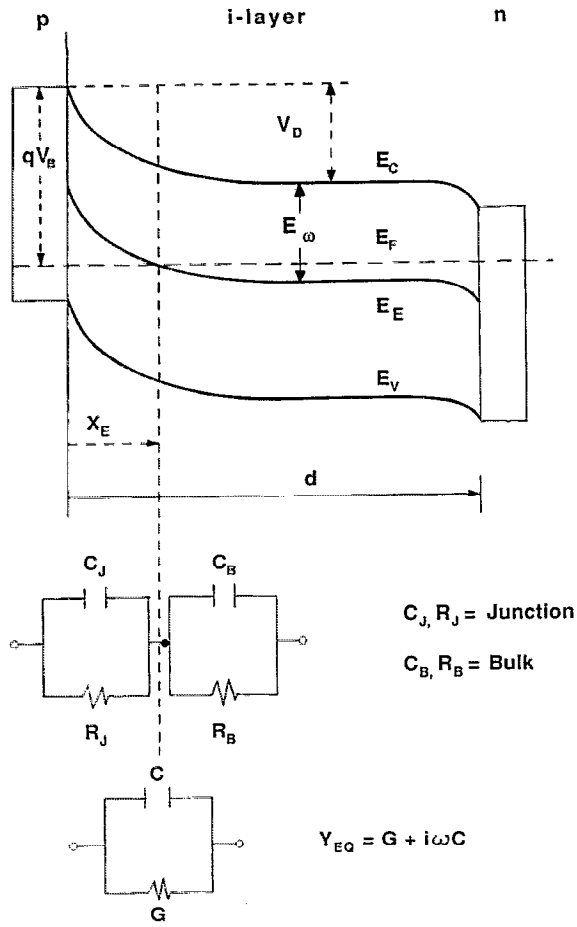

FIG. 1. (a) Band diagram of *p-i-n* junction showing barrier height V_B, Fermi energy E_F, thermal emission energy E_ω, and conduction/valence bands. (b) Lumped circuit model, (c) Equivalent admittance circuit.

ments and present the resulting expressions needed for analysis of the data in Sec. IV.

The discussion will be carried out in terms of the band diagram shown in Fig. 1(a) depicting the cell in equilibrium. We take E_C far in the interior of the i layer as the zero of energy and reckon positive energies downward. V_D is the diffusion potential (the band bending) at the p-i junction and V_B is the barrier height. E_F is assumed to be independent of bias for the small V_A considered here. The region near midgap contains a continuous distribution of localized states of density $g(E)$ which are neutral when occupied by an electron. Depopulation of these states is presumed to be the only source of volume space charge; the density of free carriers is negligible in comparison. The static charge (ρ), field (F), and potential (V) profiles can be easily derived by elementary methods,[12,31] by assuming zero-temperature Fermi statistics for the simple case that $g(E)$ is independent of energy between E_F and $E_F - qV_D$ with $g_0 = g(E_F)$. This common[4,5,8,11-13] but crucial assumption will be justified experimentally in Sec. IV. The uniform MGDOS leads to an exponential potential, field, and charge profile given by

$$V(x) = V_0 \exp(-x/L_0), \tag{4}$$

$$F(x) = F_0 \exp(-x/L_0), \tag{5}$$

$$\rho(x) = \rho_0 \exp(-x/L_0), \tag{6}$$

where $F_0 = -V_0/L_0$, $\rho_0 = -\epsilon V_0/L_0^2$, and $V_0 = V_D - V_A$ is the sum of the diffusion potential and the applied bias. ($V_A < 0$ corresponds to reverse bias.) The characteristic screening length

$$L_0 = (\epsilon/q^2 g_0)^{1/2} \tag{7}$$

will play a major role in subsequent data reduction.

Implicit in Eqs. (4)–(6) is the requirement that both potential and field vanish in the interior of the i layer and remain negligible as $x \to d$. Based on arguments and results in our previous work[30,31] we neglect any space charge at the n-i junction, and assume it is an ohmic contact consistent with numerous previous capacitance studies using metal-i-n Schottky devices.[6,8,12,13,16] Band bending within the doped layers is ignored because these layers are thin compared to the screening length L_0. Thus, we treat the p-i-n cell as having a single (p-i) junction region. The requirement for $V(x)$ and $F(x)$ to vanish as $x \to d$ will be met providing $d > 3L_0$ since truncation errors will be of order $\exp(-d/L_0)$. This assumption will be justified by the experimental results in Sec. IV. These simplifications are clearly supported by the close agreement between measured and calculated admittance behavior over a wide range of temperature and frequency as reported for these p-i-n devices.[30,31]

Now consider the effect of a small ac signal of angular frequency ω. The characteristic time τ_E of thermal release or emission from the deep states to the conduction band is

$$\tau_E = \nu^{-1} \exp[(-E/kT)], \tag{8}$$

where $E \geqslant 0$ is the depth of the state below $E_C(x)$ and ν is an attempt-to-escape frequency on the order of the peak of the phonon spectrum,[32] $\sim 10^{13}$ rad/s. The condition $\omega\tau_E = 1$, defines a contour $E_E(x)$ lying below $E_C(x)$ by an amount

$$E_\omega = E_E(x) - E_C(x) = kT \ln(\nu/\omega) \tag{9}$$

as shown in Fig. 1(a). Above this contour the filled states can equilibrate with the conduction band within the ac period; below this contour the filled states are "frozen out" and unresponsive. Figure 1 also shows a characteristic length X_E where $E_E(X_E) = E_F$, given by

$$X_E = L_0 \ln\{qV_0/[kT \ln(\nu/\omega) - E_F]\}. \tag{10}$$

For $x \leqslant X_E$, all filled states are unresponsive; for $x \geqslant X_E$, all states up to E_F can respond.

A completely general treatment[9,10,32] of the junction capacitance C_J (per area) gives

$$C_J = \frac{\epsilon\rho_E}{\epsilon F_E + X_E \rho_E}, \tag{11}$$

where F_E and ρ_E are the electric field and charge density, respectively at X_E. Equation (11) is valid for any charge or field profile. With F_E and ρ_E defined as in Eqs. (5)–(6), Eq. (11) reduces to

$$C_j=\frac{\epsilon}{L_0+X_E}. \tag{12}$$

Equation (12) has a simple physical interpretation as the series combination of two capacitors, one representing the pure dielectric (charge-free) region to the left of X_E and the other representing the modulated charge response to the right of X_E. Equation (12) can be expanded with Eq. (10) to yield

$$C_j=\frac{\epsilon/L_0}{1+\ln[qV_0/(E_\omega-E_F)]}=\frac{(\epsilon q^2 g_0)^{1/2}}{1+\ln[qV_0/(E_\omega-E_F)]}. \tag{13}$$

Note that C_j is a function of temperature and frequency through the reduced parameter $E_\omega=kT\ln(\nu/\omega)$. Limits imposed on C_j by E_ω and V_0 have been discussed.[30,31] In the limit $E_\omega>qV_B$ as occurs at either high temperature or low frequency, Eq. (13) merely recovers the dc (static) capacitance[8,12]

$$C_0=\epsilon/L_0=(\epsilon q^2 g_0)^{1/2}. \tag{14}$$

IV. FOUR METHODS TO DETERMINE g_0 FROM MEASURED CAPACITANCE

The four methods of extracting g_0 from capacitance are applied to *p-i-n* cells #2415 (0% Ge) and #3188 (62% Ge). Other samples in Table I were characterized by one or more methods.

A. Lumped circuit model of the admittance

We have previously calculated the temperature and frequency dependence of a simplified lumped element circuit model of the device, and found good agreement to the measured admittance over a wide range of temperature and frequency.[30,31] The circuit model approach (CKT) provides a very sensitive method to determine E_F, g_0, and ν by fitting the MGDOS parameters to the measured values of C and G. Only key results are given here for completeness.

The terminal admittance of the four element circuit [Figure 1(b)] was analyzed. Both G/ω and C were simultaneously fit to the measured admittance over a range of temperature and frequency, primarily by adjusting values of g_0, ν, and E_F.

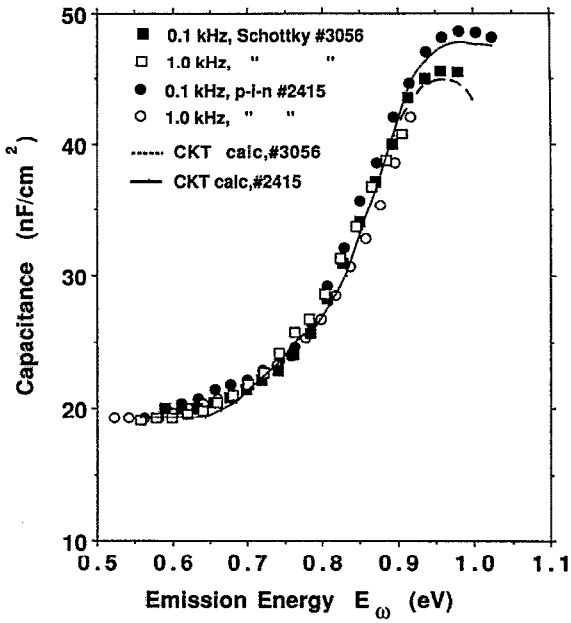

FIG. 2. Capacitance vs emission energy for *a*-Si:H devices #2415 and #3056 at 0.1, and 1.0 kHz from 0 to 200 °C. Solid line calculated from circuit model with parameters in Table II.

Figure 2 shows the measured and calculated temperature (0 to 200 °C) and frequency dependence (0.1 and 1 kHz) of the capacitance for the *a*-Si:H *p-i-n* cell (#2514) and Pt/*a*-Si:H Schottky diode (#3056). Temperature and frequency dependence are combined by plotting against the reduced parameter E_ω [Eq. (9)]. The model results were calculated with parameters listed in Table II. The $C(E_\omega)$ data in Fig. 2. is reduced to nearly a single curve showing three regions of deep state response. The capacitance well below turn-on ($E_\omega<E_F$) is the geometric capacitance of the *i* layer, ϵ/d. Above turn-on ($E_\omega>E_F$), the capacitance increases with temperature, hence E_ω, as more states respond by emitting their electrons within the ac cycle, corresponding to a decreasing X_E. The deep state response dominates for E_ω between E_F and qV_B. Finally, when $E_\omega=qV_B$, X_E goes to zero and the capacitance reaches an

TABLE II. Model input parameters for "best fit" to data.

Device #		2415	3056	2353	3188
i layer		*a*-Si:H	*a*-Si:H	*a*-SiGe	*a*-SiGe
device structure		*p-i-n*	Schottky	*p-i-n*	*p-i-n*
E_G (eV)		1.74	1.74	1.53	1.30
Parameter	Units				
d	μm	0.56	0.58	0.28	0.28
E_F	eV	0.78	0.78	0.71	0.66
V_B	V	1.0	0.95	0.90	0.75
J_{00}	A/cm^2	1.5×10^6	2.0×10^7	2×10^7	1.5×10^7
σ_0	S/cm	300	300	300	500
ϵ_r	···	12	12	14	15
ν	rad/s	5×10^{13}	5×10^{13}	2×10^{14}	3×10^{14}
g_0	(cm^3 eV)$^{-1}$	1.6×10^{16}	1.4×10^{16}	1.3×10^{17}	3.6×10^{17}

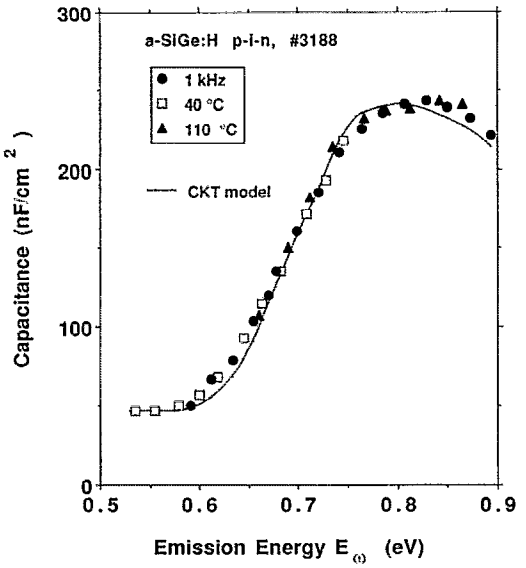

FIG. 3. Capacitance vs emission energy for *a*-SiGe:H *p-i-n* #3188. Solid line calculated from circuit model with parameters in Table II at 1 kHz from 0 to 140 °C. Measured values at 40 and 110 °C from 0.1 to 100 kHz, and at 1 kHz from 0 to 140 °C.

upper limit given by Eq. (14) ($C_{MAX}=\epsilon/L_0$). The fall-off beyond the peak is explained by the equivalent circuit.[30,31] C_J is effectively shunted by the resistive divider $(1+R_B/R_J)$.

Previous work on characterizing the MGDOS in *a*-Si:H alloys has used Schottky junctions[4–8,12,13] or heavily doped *c*-Si heterojunctions[14,15,26] to establish the space charge and band bending. The present work is unique in its use of *p-i-n* solar cell device structures. Clearly, the *p-i-n* and Schottky devices have nearly identical capacitance responses (C vs E_ω).

The only major differences between the values used to fit the *a*-Si:H *p-i-n* cell (#2415) and the *a*-Si:H Schottky cell (#3056) are those related to the junction (V_B and J_{00}). These primarily affect G/ω.[30,31] They change in the directions expected for the Schottky device. The capacitance of the Schottky device reaches its peak value at a lower energy than the *p-i-n* device because the barrier to thermal emission is lower, consistent with measurement of $J_0(T)$ and $G/\omega(T)$. As shown elsewhere[30,31] close agreement for G/ω between the circuit model and data has been found over the same range of temperature and frequency as used for the capacitance fitting. The behavior of G/ω is consistent with the *i* layer having both junction space charge and bulk regions.

The temperature and frequency dependence of the capacitance for the *a*-SiGe:H *p-i-n* device (#3188) are shown in Fig. 3 which contains the values measured at 1 kHz as T is varied from 0 to 140 °C (constant frequency) and at 40 and 110 °C as f varied from 0.1 to 100 kHz (constant temperature). The measured data reduces to a single curve when plotted against E_ω indicating that measurements at constant temperature or frequency are equivalent. The solid line was calculated at 1 kHz as T varied from 0 to 140 °C with $\nu=3\times10^{14}$ rad/s and the "best-fit" value of $g_0=3.6\times10^{17}$ cm ^{3} eV and other parameters in Table II. Note that good agreement is found over three decades of ac frequency. Results of fitting to another *a*-Si:Ge device with 43% Ge are also given in Table II.

The agreement between the measured and calculated capacitance over a wide range of f and T convincingly demonstrates the ability of the simple circuit model to accurately represent the admittance of the *p-i-n* device. Above turn-on, ($E_\omega > E_F$) agreement between the circuit model capacitance and measurement is within 10%.

B. MGDOS from the capacitance peak

A particularly simple limiting case occurs for determining g_0 from the peak or maximum value of C at low frequency or high temperature,[8] (the CMAX method). The CMAX method is the easiest of the four methods, experimentally and analytically. We calculate g_0 with Eq. (14) from the static, or dc limiting value of capacitance in which all deep states respond and X_E is zero since $E_\omega = qV_B$.

From the peak value of measured capacitance in Fig. 2–3, a value for g_0 of 3.1×10^{17} (#3188), 1.4×10^{16} (#2415), and 1.3×10^{16} (#3056) cm^{-3} eV^{-1} is found, respectively. These are in very good agreement with the value obtained from the fit of the circuit model over the full range of E_ω as just described.

The CMAX method was applied to *a*-SiGe:H *p-i-n* cells having 25% to 65% Ge. The results are given in Table III.

TABLE III. Summary of MGDOS values from four methods of capacitance analysis.

Sample #	% Ge	g_0 ($\times10^{16}$ cm^{-3} eV^{-1}) Method				
		CKT	CMAX	DCV	DL	avg
2415	0	1.6	1.4	2.2	2.0	1.8
3056	0	1.3	1.3	···	···	1.4
2352	25	3.8	3.6	···	···	3.7
2353	43	13	13	···	···	13
3188	62	36	32	38	47	38
3196	65	60	58	···	83	67

C. MGDOS from the differential capacitance-voltage method

The third method of determining g_0 is derived from the bias dependence of X_E [Eq. (10)]. The analysis is original and is presented here for the first time. It is based on the observation that for constant E_ω and small bias, X_E depends logarithmically on $V_D - V_A$. With reference to Fig. 1(a), decreasing the reverse bias band bending at $x=0$ merely "slides" X_E along the Fermi level towards $x=0$ by an amount ΔX_E due to the reduction in $V(x)$. At a constant f and T, hence constant E_ω, the difference in X_E at two different applied bias voltages V_1 and V_2 is

$$\Delta X_E = X_E(V_2) - X_E(V_1)$$
$$= L_0 \ln[(V_D - V_2)/(V_D - V_1)]. \quad (15)$$

The term $E_\omega - E_F$ cancels because it is independent of bias. Note that the slope of $\ln[(V_D - V_2)/(V_D - V_1)]$ vs ΔX_E is $1/L_0$ from which g_0 is easily determined using Eq. (7). We call this the differential capacitance voltage method (DCV). ΔX_E is obtained from the measured capacitance as follows. From Eq. (12), the capacitance at V_1 is

$$C(V_1) = \epsilon/[L_0 + X_E(V_1)] \quad (16)$$

and similarly for V_2. ΔX_E is found from

$$\Delta X_E = \epsilon[1/C(V_2) - 1/C(V_1)]. \quad (17)$$

Thus, it is the change in $C(V_2)$ relative to the value at the reference bias $C(V_1)$ which is of importance. The temperature and frequency must be selected so that the operating point is above turn-on but below the static, or saturation, capacitance; i.e., $E_F(T) < E_\omega < qV_B$. Although measurement and analysis at a single pair of f and T, hence a single value of E_ω, is sufficient to determine g_0, repeating the procedure for several values of E_ω provides another check on the validity of the assumed energy independence of g_0. This is also a check on the assumption of spatial uniformity, since X_E is swept across the i layer both by bias and by E_ω. The bias must be limited to keep $X_E(V_A)$ less than d for all V_A. We restrict our analysis to small reverse applied bias, less than -0.6 V. Forward bias is limited to voltages less than V_D to prevent flatband conditions and carrier injection.

Figure 4 shows the dependence of the capacitance on bias voltage for the a-Si:H p-i-n sample (#2415) from -2 to $+0.2$ V at several temperatures ($f=0.1$ kHz). There is negligible bias dependence at 50 °C because this temperature is below turn-on at 0.1 kHz ($E_\omega = 0.70$ eV $< E_F$). The larger bias dependence at higher temperatures implies that these devices, despite their apparent thinness, are sufficiently thick to allow X_E to be swept across the i layer for small reverse bias. We have replotted the $C(V)$ data of Fig. 4 as $1/C^2$ vs V and failed to find a linear region of reasonable slope and intercept as would occur for deep depletion.[12] We conclude that at large reverse bias, X_E exceeds d before the junction enters deep depletion. Thus, the DCV method is an appropriate tool for $C(V)$ analysis in this case.

Figure 5 plots $\ln[(V_D - V_2)/(V_D - V_1)]$ vs ΔX_E [Eqs. (15)–(17)], where V_2 is the running variable and V_1 is the operating point for the $C(V)$ data of Fig. 4 from -0.2 to $+0.15$ V. The reference bias V_1 was taken as $+0.2$ V. We obtained good linearity over the voltage range of interest with $V_D = 0.33$ V. This compares to a value of 0.23 V which is inferred from the circuit model for this same device. We do not consider this a serious discrepancy since the value of V_D affects the extent of the linear region but does not affect the slope of the linear region in Fig. 5 which is $1/L_0$, [Eq. (7)]. Data at all three temperatures have the same slope, yielding a screening length $L_0 = 0.165$ μm,

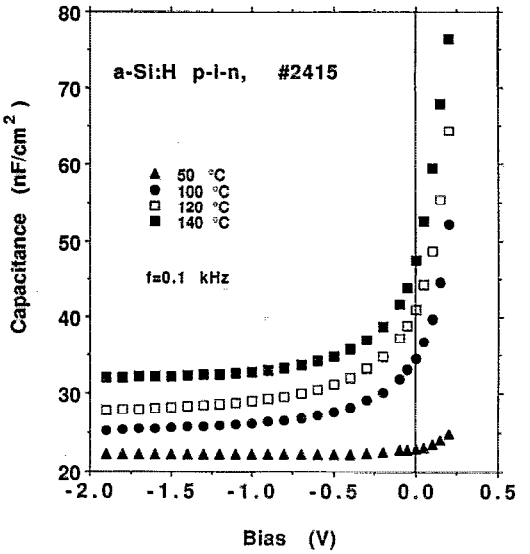

FIG. 4. Capacitance vs voltage for #2415 at 0.1 kHz at 50, 100, 120, and 140 °C.

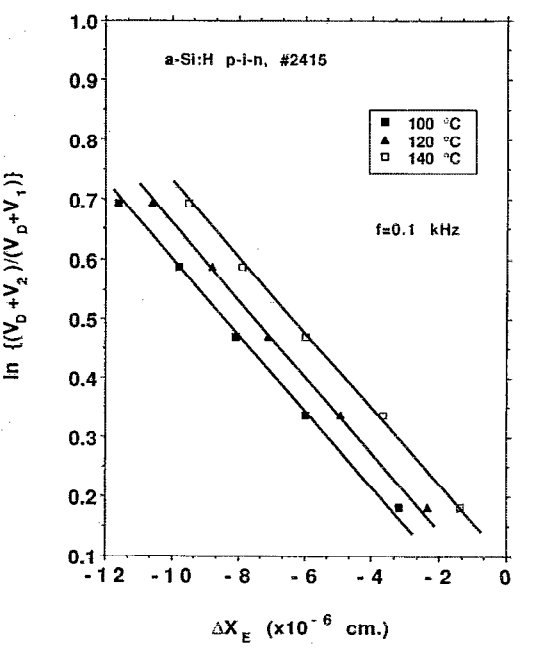

FIG. 5. Bias dependence of ΔX_E for #2415 at 0.1 kHz at 100, 120, and 140 °C. Solid lines have inverse slope (L_0) of 0.165 μm.

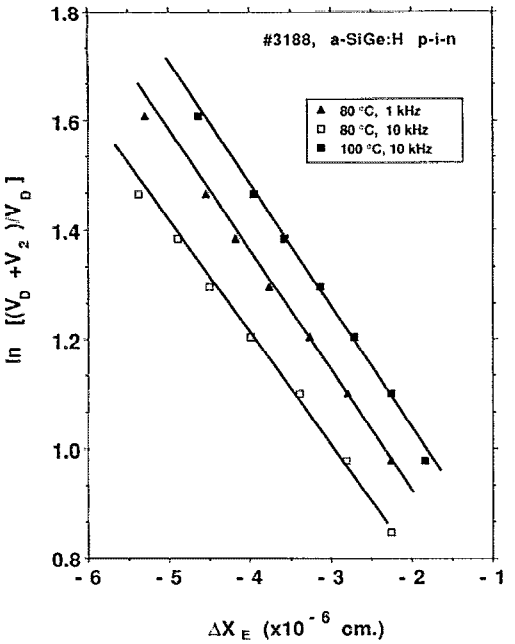

FIG. 6. Bias dependence of ΔX_E for #3188 at various temperatures and frequencies. Solid lines have inverse slope L_0 of 0.046 to 0.051 μm.

from which we calculate $g_0=2.2\times10^{16}/\text{cm}^3$ eV. This is slightly ($\sim$50%) larger than values of $(1.4\text{–}1.6)\times10^{16}/\text{cm}^3$ eV for this same sample by the CKT and CMAX methods already presented, but within the acceptable margin of error.

Similar measurements and analysis were performed on the *a*-SiGe:H *p-i-n* device (#3188). Figure 6 shows the DCV analysis for V_2 from -0.5 to -0.2 V with $V_1=0$ V. The diffusion voltage was $V_D=0.15$ V which compares to a value of $V_D=0.09$ eV from the circuit model for this same device. The $C(V)$ data were taken at three pairs of frequency and temperature. There were slight variations in L_0 (0.046–0.051 μm yielding g_0 of $3.3\text{–}4.0\times10^{17}/\text{cm}^3$ eV. This is in good agreement with the values for this same sample from the CKT and CMAX methods already presented (Table III).

The results of the DCV method are significant for a number of reasons. They clearly show that the simple expression for C_J [Eqs. (12),(13)] contains the correct bias dependence. The applied voltage changes the band bending at the surface ($V_0=V_D-V_A$), but E_F remains flat. The DCV results also justify the assumption that the MGDOS is uniform spatially across the *i* layer as well as energetically within the gap (near E_F) because X_E is swept across the *i* layer with bias and through the gap states with frequency and temperature via E_ω. Thus, a different region is probed with each set of f,T, and V_2, since each set of variables defines a different operating point for X_E. Finally, the DCV method yields values of g_0 which are within 50% of those found by other methods on the same devices at 0 V.

D. MGDOS from the drive-level capacitance method

This section presents results of the drive level (DL) method[26] which combines the temperature, frequency, and dc bias dependence of the deep state response in one technique with the ac test signal amplitude δV as an additional independent variable. This parameter (δV) was fixed in all measurements described thus far, and in other admittance methods discussed in the literature as well. The transfer function may be assumed to be linear for such small test signals. In contrast, DL is essentially a large signal technique.

The experimental procedure behind the DL method[26] was presented in Sec. II C. The DL analysis starts with the definition of the junction capacitance given by Eq. (11). However, this is only the limiting value for the case where δV is negligible compared to the dc bias and diffusion voltage. If δV (the drive level) is not negligible relative to V_0, then a series expansion in powers of δV yields[26]

$$C=C_0+C_1\delta V+C_2(\delta V)^2+\dots, \tag{18}$$

where C_0 is given by Eq. (11). The first-order coefficient is

$$C_1=\frac{dC}{dV}=\epsilon\rho_E^2/2(\epsilon F_E+X_E\rho_E)^3. \tag{19}$$

The drive level integrated defect state density N_{DL} (Ref. 26) is defined in terms of C_0 and C_1 as

$$N_{\text{DL}}=C_0^3/(2q\epsilon C_1)=\rho_E/q. \tag{20}$$

The charge density which can respond at a given E_ω is

$$\rho_E=q\int_{E_F}^{E_\omega} g(E)dE. \tag{21}$$

The coefficients C_0 and C_1 are obtained by fitting a quadratic to C vs δV. The energy dependence of N_{DL} is determined by varying E_ω. The slope of N_{DL} vs E_ω directly gives the DOS distribution, $g(E)$. A constant slope indicates a constant MGDOS over the region which has been probed by E_ω. The drive level (DL) method is experimentally the most difficult of the four methods. It is also the only one of the four methods which does not assume *a priori* a uniform MGDOS.

Figure 7 shows N_{DL} vs E_ω for the *a*-Si:H *p-i-n* cell #2415. The escape frequency ν was taken as 5×10^{13} rad/s from Table II. N_{DL} increases with E_ω because progressively deeper states are probed. A least-squares fit yields a slope $g_0=2.0\times10^{16}/\text{cm}^3$ eV, and the intercept indicates $E_F(T)=0.69$ eV. This value of g_0 is in close agreement with those obtained by the CKT, CMAX, and DCV methods on this same sample. In Fig. 8, we plot N_{DL} vs E_ω for the 1.3 eV *a*-SiGe:H *p-i-n* cell #3188. The escape frequency ν was taken as 3×10^{14} rad/s from Table II. A least-squares fit yields $g_0=4.7\times10^{17}/\text{cm}^3$ eV, and the intercept indicates $E_F(T)=0.58$ eV. The value of g_0 is slightly (30%) higher than obtained by the CKT, CMAX, and DCV methods on this same sample.

The DL method was also applied to an *a*-Si:H *p-i-n* cell having a 1.2 μm *i* layer (i.e., thicker than our photo-CVD devices) deposited by plasma-CVD at Chronar Corp.,

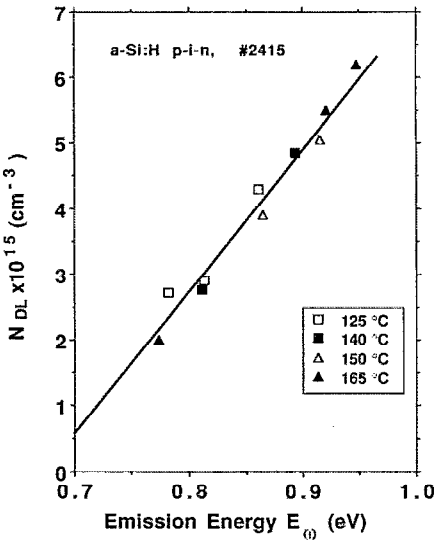

FIG. 7. Drive level charge density vs emission energy from #2415 at various frequencies (0.1 to 10 kHz) and temperatures (125 to 165 °C). Solid line is least-square fit. Slope yields $g_0=2.0\times10^{16}/\text{cm}^3$ eV and intercept $E_F(T)=0.69$ eV.

yielding $g_0=1.0\times10^{16}/\text{cm}^3$ eV and $E_F(T)=0.76$ eV. Kalina *et al.*[33] determined the MGDOS of similarly deposited *p-i-n* devices by photocurrent DLTS. They found a MGDOS of $(1.0\pm0.1)\times10^{16}/\text{cm}^3$ eV at an energy 0.8 eV below the conduction band. Thus, the DL value is in good agreement with the DLTS value.

The linearity of N_{DL} with E_ω (Fig. 7 and 8) is direct experimental proof that the MGDOS is uniform for a few tenths of an eV between E_F and qV_B below E_C. The intercept of Fig. 7 and 8 is theoretically $E_F(T)$, i.e., the threshold for thermal emission from deep states. As discussed in Sec. II C, by adding $2kT$ to $E_F(T)$ to obtain $E_A=E_F(0)$, we find $E_F(0)=0.64$ eV for the *a*-SiGe:H *p-i-n* device (#3188) and $E_F(0)=0.73$ eV for the *a*-Si:H *p-i-n* device (#2415), in good agreement with the best-fit values from the CKT method in Table II and with conductivity measurements (see Sec. II C). The value of 0.82 eV for the Chronar cell is also in good agreement with their data. We consider this to be further evidence for the overall correctness of the value of ν and the determination $E_F(T)$ with the CKT model.

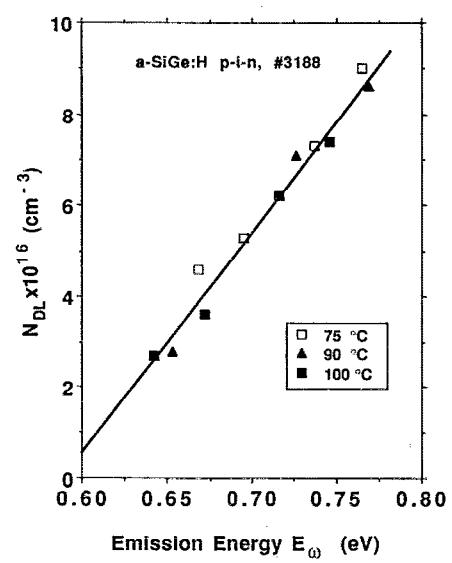

FIG. 8. Drive level charge density vs emission energy from #3188 at frequencies from 1 to 100 kHz at 75, 90, and 100 °C. Solid line is least-square fit. Slope yields $g_0=4.7\times10^{17}/\text{cm}^3$ eV and intercept $E_F(T)=0.58$ eV.

V. DISCUSSION

A. Discussion of the present results

We have shown that steady-state admittance analysis can be applied to standard *p-i-n* solar cells having various thin buffer layers, and does not require specially prepared doped *a*-Si:H Schottky barriers or *c*-Si/*a*-Si:H heterojunction structures. In fact, we have found the *p-i-n* device to be superior to the more commonly used Schottky barrier in terms of better mechanical and thermal stability, less degradation, and lower leakage current J_0.

Applying several different methods of analysis tests the self-consistency of the basic junction capacitance model, and checks the validity of different simplifying assumptions. For example, DL is the only one of the four methods which does not explicitly assume a uniform MGDOS, yet Fig. 7 and 8 from the DL analysis clearly support this simplifying assumption. The dependence of N_{DL} on E_ω (Figs. 7 and 8) is strongly related to the dependence of C on E_ω (Figs. 2 and 3) for the same devices. Together, these results demonstrate that the temperature and frequency dependence of the deep state space charge and capacitance is governed by E_ω, not f or T individually. Similarly, the assumption that E_F is independent of the small dc bias is verified (for small V_A used here) by the close agreement in g_0 and E_F found between the CKT ($V_A=0$) and the DCV and DL ($V_A<0$) methods.

The MGDOS results are summarized in Table III. The Ge content of the *i* layer is given together with the g_0 values resulting from the various analytical techniques, as well as the average g_0 value. All values are within 25% of the average. The g_0 values in Table III from the two techniques requiring applied bias (DCV and DL) are slightly higher than the CKT or CMAX values for reasons which are unclear at present. However, the differences in g_0 between the different methods are small ($\pm25\%$) compared to the factor of 20 increase in g_0 as Ge increases from 0% to 62%.

B. Ge-related defects in *a*-SiGe:H

The average g_0 from Table III has a nearly exponential dependence on Ge content, as we have discussed.[30,31] It also appears that g_0 does not depend on deposition temperature[30,31] which is known to affect the H bonding structure of the film.[19] Our results for g_0 in *a*-Si:H are consistent with those from other groups[33,34] making solar cells indicating that "device-quality" *a*-Si:H *i* layers have $g_0=1$–2×10^{16}

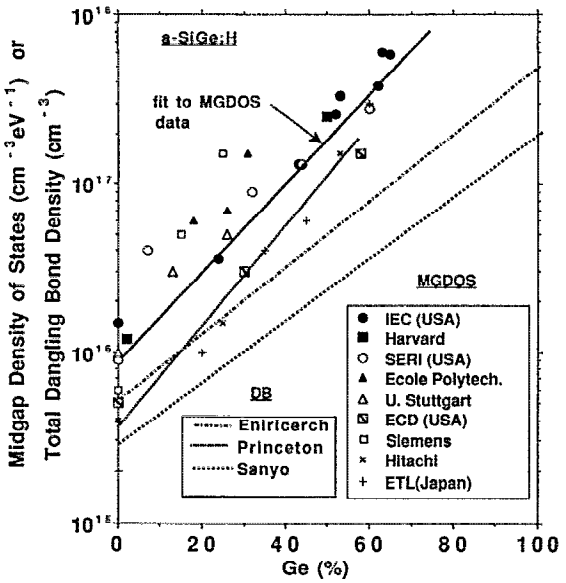

FIG. 9. Summary of results reported by 12 groups showing the Ge dependence of defects (–either MGDOS or total DB density) in *a*-SiGe:H. Characterization methods [capacitance (CAP), space charge limited current (SCLC), sub-gap optical absorption (OPT), or electron spin resonance (ESR)] and references as follows: IEC (CAP, this work); Harvard (CAP and SCLC, Refs. 13 and 36); SERI (SCLC, Ref. 39); Ecole Polytech. (SCLS, Ref. 41); U. Stuttgart (SCLC, Ref. 40); ECD (SCLC, Ref. 38); Siemens (SCLC, Ref. 37); Hitachi (OPT, Ref. 43); ETL (CAP, Ref. 15); Enitricerche (OPT and ESR, Ref. 45); Princeton (OPT, Ref. 48); SANYO (ESR, Ref. 44).

$cm^{-3}\,eV^{-1}$. These results are also consistent with the measured dangling bond defect density of $\sim 5\times 10^{15}$ cm^{-3} on these *a*-Si:H films[34,35] assuming a width of 0.3 eV.

Results similar to those in Table III for the dependence of $g(E_F)$ or g_0 on Ge content have been reported by many groups (Fig. 9). Films have been deposited by plasma-CVD or photo-CVD and characterized by SCLC,[36–41] steady-state capacitance,[13,15] transient capacitance,[15] transient photocurrent[42] and sub-band gap optical absorption spectroscopy.[43] Samples have consisted of *p-i-n* or Schottky junctions, *n-i-n* devices, coplanar electrodes, or *a*-SiGe:H/*c*-Si heterojunctions. Our results are the only ones to date obtained on actual solar cells.

Matsuura[15] and Sharma *et al.*[13] applied several capacitance methods (different from ours) to *a*-SiGe:H films having $E_G \sim 1.3$–1.35 eV (estimated Ge content of 50–55%) and found g_0 of 1–3×10^{17} $cm^{-3}\,eV^{-1}$. These results are very comparable to ours, despite differences in deposition technique, sample configuration, and measurement and analysis of capacitance data by the three groups.

Results in Fig. 9 are in generally good agreement that the MGDOS increases approximately exponentially with Ge content, by a factor of 10 to 30 with 50% Ge. Absolute values differ by about a factor of 5 at a given Ge value. The difference is much smaller than the value of 10–40 quoted elsewhere[3] and shows the same general trend is universally observed. This is surprising considering the large variation in deposition and characterization techniques which are represented. The total dangling bond density[44,45] (Si and Ge DB) in Fig. 9 also increases at a similar exponential rate with Ge, and suggests that the DBs contributing to the MGDOS have a width ΔE of ~ 0.3 eV assuming $g_0 = N_{DB}/\Delta E$. Steeper increases in DB spin density with Ge content have been reported,[46,47] but were probably due to using far-from-optimized deposition conditions.[47]

Aljishi *et al.*[48] have explained the exponential dependence of midgap defects on band gap, hence Ge, in terms of either an entropy model or kinetic model of defect equilibrium.

Various defect energy models for ranking the energy position of the Si and Ge D^0 and D^- dangling bond defect states have been proposed for the *a*-SiGe:H alloy system.[36,45,47,49] Our capacitance results (Fig. 3 and 8), show that Ge-related states which contribute to the capacitance lie 0.6 to 0.8 eV below E_C for 1.3 eV material. This is consistent with at least two of the proposed energy band models.[36,49] We feel that the differences between the various defect energy band assignments are relatively insignificant since the width of the defect bands is typically as large as the estimated separations.

C. Charged midgap defects and transport

An important consequence of the existence of two types of DBs (Si and Ge) and their possible overlap in energy is the formation of charged DBs. The charge state of a dangling bond depends on its position relative to E_F, as is well known from ESR studies on doped films. D^0 states above E_F are unoccupied, hence positively charged. Similarly, D^- states below E_F are doubly occupied, hence negatively charged.

Thus, the different proposed models[36,45,47,49] share a common feature. They show some overlap between the D^0 (Si or Ge) and D^- (Si or Ge), with E_F straddling the D^0 (Ge) distribution such that some states are above E_F and some are below E_F. These features are the source of the charged defects.

Calculations of Si and Ge dangling bond energies and widths[49] confirm that the difference between the centers of the Si and Ge D^0 bands may be only 0.1 eV, while their width is nearly 0.2 eV. It was concluded[49] that charged defect pairs are likely to form due to the overlap.

Positively charged DBs were proposed to explain the dramatic decrease in electron $\mu\tau$ product and photoluminescence upon Ge alloying.[36] Models are unclear as to whether positive or negative defects will dominate. In view of the greater degradation in electron compared to hole transport,[19,21] positively charged defects are more likely. However, some transport measurements are consistent with the formation of only neutral defects (Ge D^0) as Ge content increases[47] suggesting that the charged defect density is negligible.

Most discussion of charged defects focuses on their effect on carrier lifetime through enhanced (reduced) recombination at attractive (repulsive) centers. However, charged defects can cause potential fluctuations which increase electron scattering, thus decreasing the mobility in the extended states. Charged defects would cause an especially serious degradation in electron mobility due to their

proximity to the conduction band edge. Charged Ge dangling bonds near midgap in *a*-SiGe:H or *a*-Ge:H have been proposed[50] as responsible for potential fluctuations which degrade the electron mobility upon alloying with Ge. The decrease in electron mobility with Ge alloying is well established.[21,36,37,48,51] Thus, the increase in MGDOS may degrade both lifetime and mobility via charged defects. This connection has been extensively discussed elsewhere.[31]

D. Implications for solar cell performance

Photocarrier collection in *a*-Si:H alloy solar cells occurs largely (but not exclusively) by field-assisted drift. The fill factor (FF) is limited by voltage-dependent photocurrent collection. This problem is compounded in *a*-SiGe:H devices because both carriers have smaller $\mu\tau$ products than they do in *a*-Si:H, and because the high field space charge region is narrowed by the higher MGDOS. Thus, a higher g_0 leads to a lower screening length L_0, so that a thinner *i* layer is required to maintain a sufficient field throughout. The trade-off between increased field and reduced absorption determines the optimum cell thickness. Very thin ($\sim 0.1\ \mu$m) low band gap *i* layers are needed to maintain sufficient collection[21] at high Ge content ($>50\%$). Note that the uniform field approximation is commonly used in analysis of *a*-Si:H and *a*-SiGe:H solar cells. This is a poor approximation if $d > L_0$, since our results suggest an exponential field profile.

Results in Table II indicate another weakness with the present *a*-SiGe:H *p-i-n* design; namely, the diffusion voltage V_D is quite small (~ 0.01 V). This further limits the extent of the field penetration in the *i* layer and thus limits the collection length. Together with the small screening length, the small value of V_D limits the FF and J_{sc}.

Table II also shows that the recombination current J_{00} for *a*-SiGe:H *p-i-n* cells is much larger than for *a*-Si:H *p-i-n* devices. This is a severe limit to V_{oc}. However, improved buffer layers and grading at interfaces can increase V_{oc} by reducing the recombination current.[21,25]

VI. SUMMARY

The derivation of the capacitance for a single junction with a uniform MGDOS yields a relatively simple expression in terms of the density of midgap states g_0, the electron attempt-to-escape frequency ν, the Fermi energy E_F, and the external variables of bias, frequency, and temperature. A four element, lumped circuit model adequately describes the admittance of the *p-i-n* device. Circuit elements containing the thermal emission of deep states, thermal leakage of the diode, and the bulk conductivity and capacitance are sufficient to model the observed capacitance and conductance. The close agreement between measured and calculated capacitance and conductance over a range of frequency and temperature verifies the applicability of the circuit model to *p-i-n* devices having *a*-Si:H and *a*-SiGe:H *i* layers. The similarity between Schottky and *p-i-n* results using the same model retroactively justifies the neglect of space charge in the doped layers.

Standard *p-i-n* cells are suitable test devices for characterization of the MGDOS by capacitance. Results are not influenced by a thin buffer layer. However, the minimum *i* layer thickness for valid application of the methods described here is $3L_0$, where L_0 is the screening length.

The MGDOS was determined by four methods of analyzing the temperature, frequency, and voltage bias dependence of the capacitance. A new technique to obtain g_0 from $C(V)$ measurements was developed, called the differential capacitance voltage method (DCV). Agreement in the derived values of g_0 within $\pm 25\%$ was found among the four methods on a given device. We consider the application of and agreement between four methods on standard *p-i-n* devices to be the most novel and distinctive feature of this work.

The MGDOS increases exponentially with the Ge content of the *i* layer in substantial agreement with results from a number of studies using a variety of techniques. Our results for the increase in MGDOS are consistent with some models of others for midgap dangling bond assignments in *a*-SiGe:H. Creation of charged midgap centers is likely and supported by some transport experiments.

ACKNOWLEDGMENTS

We wish to thank R. Dozier and T. Zhou for assistance, B. Baron and J. Phillips for encouragement, J. D. Cohen for helpful discussions, and E. Koronik for manuscript preparations. This work was supported by SERI under subcontract XL-8-19092-1.

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