Schottky barrier impact-ionization metal-oxide-semiconductor device with reduced operating voltage

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In this letter, a Schottky barrier impact-ionization metal-oxide-semiconductor (SB-IMOS) device with reduced operating voltage is proposed and investigated. By introducing the silicide source and combining impact ionization with Schottky barrier tunneling, source parasitical resistance can be extremely reduced and the device performance can be improved. The device is optimized with Schottky barrier height variation additionally. Both SB-IMOS and conventional impact-ionization metal-oxide-semiconductor devices were fabricated using the standard complementary metal-oxide-semiconductor technology. SB-IMOS exhibits a 33% lower operating voltage, 43% lower threshold voltage, and improvement of ON current by 2 orders of magnitude while maintaining steep subthreshold swing of 10.2 mV/dec. © *2011 American Institute of Physics*. [doi:10.1063/1.3624707]

Recently, devices with steep subthreshold swings (*SSs*) less than 60 mV/dec have attracted much attention due to the fundamental limitation of metal-oxide-semiconductor field-effect transistor (MOSFET).[1] Impact-ionization metal-oxide-semiconductor (IMOS) is one of the promising candidates for its demonstrated ultra-low *SS* of below 10 mV/dec.[2,3] However, due to the high-field impact ionization mechanism of carrier generation and large extrinsic resistance of source, IMOS requires high operating voltages (V_{OP}) even at highly scaled dimensions.[4–6] Many methods have been proposed for the V_{OP} reduction of IMOS, such as two-spacer fabrication process,[4,5] integration with epitaxial silicon-carbon $Si_{0.99}C_{0.01}$ source and drain regions[6] and operation with depletion mode rather than inversion mode.[7] However, significant V_{OP} improvement by more simple and compatible process is still a big necessity.

In this letter, we propose a Schottky barrier IMOS (SB-IMOS) device. By introducing the Schottky barrier source, obvious V_{OP} reduction with simple complementary metal-oxide-semiconductor (CMOS)-compatible fabrication can be realized. Experimental results show that compared with conventional IMOS, SB-IMOS can have a 33% reduction of operating voltage and improved ON current while maintaining very steep *SS*.

The SB-IMOS device is schematically shown in Fig. 1(a). Compared with conventional IMOS, the source of SB-IMOS is metallike silicide region rather than heavily doped silicon. The bias conditions of normal operation are chosen as $V_G > V_D = 0V > V_S$ for n-type SB-IMOS and the polarity of the gate and source is opposite for p-type devices.

By applying a positive V_G to the structure in Fig. 1(a), an inversion layer forms under the gate and the effective length of intrinsic region is reduced. Thus, the electric field of I-region is greatly increased and eventually initiates the impact ionization. The energy band of I-region significantly drops and the source Schottky barrier is narrowed as the dotted line shown in Fig. 1(b). When V_G reaches the critical value, electrons tunneling from the source trigger the avalanche multiplication. The SB-IMOS device finally switches to the ON state. The silicide source can extremely reduce the source parasitical resistance, which makes the voltage dropped across the I-region distinctly increase, and thus can effectively reduces operating voltage as well as threshold voltage compared with conventional IMOS. Besides, the avalanche can be initiated at the source junction or the gate edge near the I-region in conventional IMOS, depending on the ratio of lateral electrical field peaks at these two locations.[8] The Schottky barrier source can increase the peak at the source junction and thus make the avalanche away from the gate oxide, which may improve the device reliability additionally.

Simulations are carried out using Synopsys TCAD SENTAURUS DEVICE SIMULATION tools.[9] To accurately simulate sub-100-nm gate length devices, impact-ionization model and band-to-band tunneling model are included. The tunneling current through Schottky barrier is considered by nonlocal tunneling model with a nonlocal distance of 5 nm. The device studied here is designed with 1-nm gate oxide thickness (T_{OX}) and 25-nm silicon film thickness (T_{Si}). The drain concentration is 1×10^{20} cm^{-3}. The channel and I-region concentrations are 1×10^{13} cm^{-3} with the intrinsic situation. The gate length (L_G) and the I-region length (L_I) are 75 nm and 45 nm, respectively. For n-type SB-IMOS, another important parameter is the source Schottky barrier height for electrons (Φ_B) which ranges from 0.4 eV to 0.8 eV (0.67 eV is default value corresponding to NiSi silicide[10]). The supply voltage is 1.0 V.

Figure 2(a) compares the transfer characteristics of Schottky barrier MOSFET (SB-MOSFET), IMOS, and SB-IMOS devices. It can be seen that although SB-MOSFET can operate at a lower drain-source voltage of 1.0 V, this device shows low I_{ON}/I_{OFF} ratio due to the high Φ_B, which can be optimized by introducing dopant segregation technology.[11–13] However, its *SS* is as high as 203.8 mV/dec, which cannot meet the requirement of low-power application. By contrast, the IMOS device shows not only the highest

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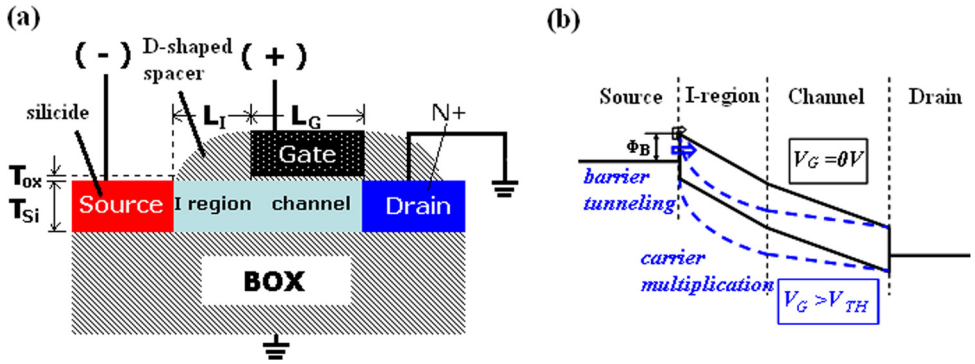

FIG. 1. (Color online) (a) Schematic of an n-type SB-IMOS device on an SOI substrate. (b) Schematic of surface energy band in the OFF state ($V_G = 0$ V) and ON state ($V_G > V_{TH}$).

I_{ON}/I_{OFF} ratio of 6 orders of magnitude, but also the lowest *SS* and I_{OFF}. Nevertheless, it requires a high V_{OP} and V_{TH} due to its working principle, which may impede its practical applications. It can be observed that SB-IMOS can reduce V_{TH} to 0.25 V while almost keeping the superior characteristics with *SS* of 2.24 mV/dec, I_{ON}/I_{OFF} ratio of $10^5 \sim 10^6$, and I_{OFF} of ~1 nA/μm. In addition, the V_{OP} of SB-IMOS can be 4.16 V compared with 4.32 V of IMOS from the output characteristics (as shown in Fig. 2(b)) due to the lower source parasitical resistance. These demonstrate that SB-IMOS has a superior performance to conventional IMOS, especially for the reduced V_{OP} and V_{TH}. Since the switching-on mechanism of SB-IMOS is combined with Schottky barrier tunneling, *SS* would degrade a little from 1.08 mV/dec of conventional IMOS to 2.24 mV/dec, yet still has great competitiveness. Additionally, I_{OFF} is slightly larger than that of IMOS mainly due to the relatively leaky silicide source, but still in a tolerant range, and can be alleviated by optimized design, especially Φ_B modulation.

The simulated *SS*, V_{TH}, and I_{OFF} of SB-IMOS with different Φ_B are compared in Fig. 3. It shows that *SS* and V_{TH} decrease as Φ_B increased, while I_{OFF} has optimized region and can reach a minimum value when Φ_B is about 0.5 eV. This is because the higher barrier height may impede carriers tunneling from source, and thus relieve the *SS* degradation caused by Schottky barrier tunneling. Moreover, when the avalanche multiplication occurs, the potential difference across the I-region remains relatively constant and the change of Φ_B will be reflected in the surface potential of channel, which makes V_{TH} decrease as Φ_B increased. As for I_{OFF}, too high or too low barrier height will increase the current of holes and thermal emission, respectively. In view of the above, the optimized Φ_B is a compromise between *SS*, V_{TH}, and I_{OFF}. From Fig. 3, it suggests that 0.6 eV might be the optimized value with *SS* of 5.20 mV/dec, V_{TH} of 0.33 V, and I_{OFF} of 3.30 nA/μm.

A p-type SB-IMOS device based on an SOI substrate has been fabricated by using a D-shaped spacer. L_I can be precisely defined by the spacer length, while the L_I of conventional IMOS is also affected by the source doping diffusion under the spacer.[14,15] The main SB-IMOS process flow which is basically compatible with the standard CMOS technology started with isolation process. Then, the gate oxide of ~4.5 nm was grown, followed by poly silicon layer deposition and patterned. After 30-nm oxide spacers were formed, the drain implantation was performed by boron ion at a dose of 5×10^{15} cm^{-2} and with an energy of 33 keV using a source-blocking mask. This was followed by a rapid thermal annealing (RTA) at 1050 °C for 10 s. Next, SiO_2 of 0.5-μm thickness was deposited and etched to form the D-shaped spacer where L_I was defined. After sputtering metal Ni and then annealing at 600 °C for 40 s, silicide source was formed together with ohmic contacts in the gate and drain. The additional mask to define the source region in conventional

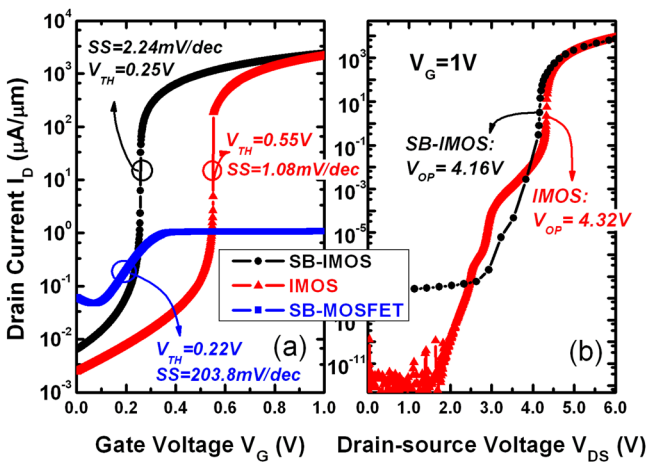

FIG. 2. (Color online) (a) Simulated transfer characteristics of SB-IMOS, IMOS, and SB-MOSFET devices. SB-IMOS and IMOS are biased as V_S of −5.0 V and V_D of 0 V. SB-MOSFET is biased as V_D of 1 V and V_S of 0 V. (b) Simulated output characteristics of SB-IMOS and IMOS.

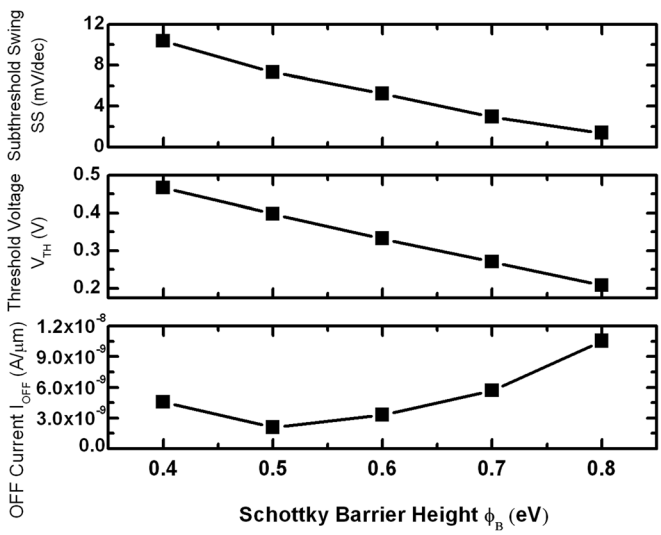

FIG. 3. Comparisons of subthreshold swings, threshold voltages, and OFF currents of n-type SB-IMOS with Schottky barrier height Φ_B variation.

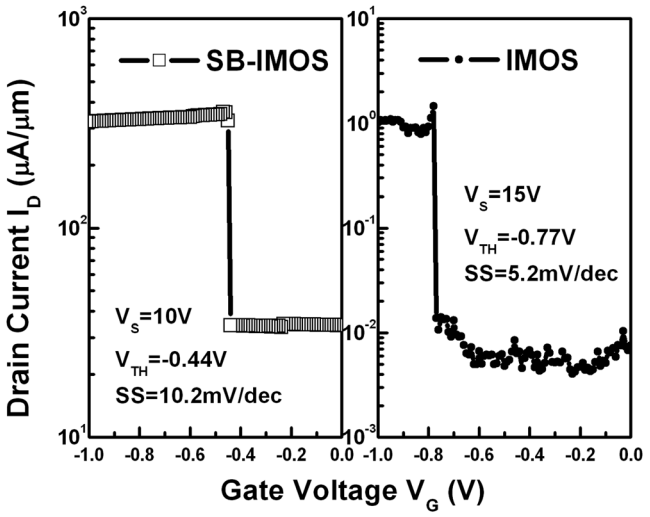

FIG. 4. Measured transfer characteristics of fabricated p-type SB-IMOS and IMOS devices.

IMOS process can be simplified for SB-IMOS. Finally, back-end steps, including contact-hole etching, metal deposition, and metal patterning steps, were performed to complete this process.

The measured transfer characteristics of fabricated SB-IMOS and IMOS devices with 2.5-μm gate length are compared in Fig. 4. It shows that by introducing a silicide source, the V_{OP} of SB-IMOS reduces by almost 33% compared with conventional IMOS; the V_{TH} reduces by 43% and the I_{ON} increases by almost 2 orders of magnitude. In comparison with the reported depletion-IMOS (D-IMOS) device for the same purpose of V_{OP} reduction,[7] the SB-IMOS device shows higher I_{ON}, reduced V_{OP} and V_{TH}, and lower SS. The I_{ON}/I_{OFF} ratio of SB-IMOS is a little inferior to those of IMOS devices due to the high leakage current of the Schottky barrier, which can be further optimized by introducing dopant-segregated Schottky barrier in the future.

In conclusion, a SB-IMOS device is proposed and fabricated. By introducing the silicide source, significant reduction in V_{OP} and V_{TH} and improvement in I_{ON} were obtained in the fabricated SB-IMOS device compared with conventional IMOS. In addition, the leakage current caused by Schottky barrier can be alleviated by optimizing the barrier height of 0.6 eV. Other optimizations, such as decreasing L_I and increasing L_G/L_I, may further reduce operating voltages and improve device characteristics.

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