THE EFFECTS OF SOLAR CELL CAPACITANCE ON CALIBRATION ACCURACY WHEN USING A FLASH SIMULATOR

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ABSTRACT

A model for investigating the dynamic behaviour of solar cells, which allows the simulation of the measurements process with flash solar simulators, is presented in this paper. This model is then applied to the simulation of measurement processes currently employed by common solar simulator types. It is shown that the cell capacitance, the series resistance and cell area can all influence the measurements, giving rise to transient errors, especially in short flash solar simulators. It is also shown that point distribution as well as scan time also have significant importance.

INTRODUCTION

Solar module calibrations are predominantly carried out by the use of flash simulators. These simulators typically trace the current-voltage (I-V) characteristic within a flash duration of several milliseconds, typically 2 or 10 ms with current solar simulators. The impact of transient errors in flash simulators can be problematic in certain cases. This problem was investigated by Friesen and Ossenbrink, who studied capacitance effects in high-efficiency solar cells [1]. Lipps et al. [2] suggested correction methods for the measured I-V curves.

The purpose of this paper is to investigate the problem on the basis of the commercial devices known to have the most significant capacitance, and investigate strategies to minimise the influence on the accuracy of the absolute calibration as identified e.g. in [3]. Five effects that have a major impact on the accuracy of the determination of electrical parameters of the PV device are identified (device capacity, series resistance, cell area, point number and sweep time) and are investigated in the following.

THEORETICAL MODEL

The total capacitance of the cell can be attributed to junction diffusion and transition carrier capacitance. Junction capacitance, which represents the charge storage in the depletion layer, dominates the cell capacitance in low bias conditions (Figure 1). For an abrupt junction it is expressed as [6]:

$$C_j = A\sqrt{\frac{q\varepsilon_s}{2(V_{bi}-V_j)}\left(\frac{N_A N_D}{N_A+N_D}\right)} \quad (1)$$

where A is the cell area, q is the elementary charge, ε_s is the electrical permittivity of the semiconductor, V_{bi} is the built-in potential, $V_j=V-IR_S$ is the voltage applied to the capacitor, V and I are the voltage and the current of the device respectively, R_S is the series resistance, N_A is the acceptor impurity concentration and N_D is the donor impurity concentration.

Diffusion capacitance corresponds to minority carrier storage in the quasi-neutral regions of the junction. Transient carrier capacitance is attributed to the existence of defect and interface states. Both of them have a dependence on the applied voltage, which allows combining the two into the strongly voltage dependent free carrier capacitance [4].

In devices based on Silicon technology, capacitance is dominated by junction capacitances at low voltages (~0-0.3V) increasing linearly, then free carrier capacitance (~0.3-0.7V) takes over and the total capacitance increases exponentially [2]. Finally, for voltages above 0.7 V total capacitance shows a rapid decrease which has been attributed to interface states [5].

To simulate this capacitive behaviour a Gaussian function has been employed, which is then multiplied by an asymmetric factor, replacing the exponential dependent free carrier capacitance used by others [2]. The advantage of this equation is that it remains applicable even for I-V sweeps going into far forward conditions. The equation relating to the total capacitance is given by the following:

$$C = C_j + C_{FC} = a \cdot A\sqrt{\frac{q\varepsilon_S}{2(V_{bi}-V_j)}\left(\frac{N_A N_D}{N_A+N_D}\right)} + C_{FC} \quad (2)$$

$$C_{FC} = C_{Gauss} \cdot C_{AF} = \\ = C_0 \exp\left(-c^2 (V_j - b)^2\right) \cdot \exp\left(\frac{\log 1/2}{b^d} V_j^d\right) \quad (3)$$

where a, C_0, b, c and d are fitting parameters: a is a fitting factor for junction capacitance, b is the centre of the Gaussian distribution (it should be emphasized though that V=b is the centre of the Gaussian distribution, but it does not indicate the peak of the resulting capacitances as the free carrier capacitance is also dependant on asymmetricity factor C_{AF}), c determines how broad the distribution is and d how intense the asymmetry will be (d≥1). The asymmetricity factor takes values from 0 to 1. The reason that b is involved in the asymmetricity factor is because it is desired to have a value of ½ for V=b, resulting in an asymmetric Gaussian distribution (Fig. 1).

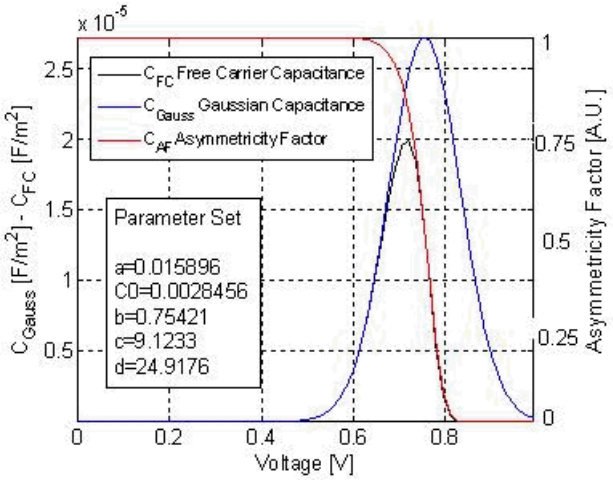


Fig. 1. Free carrier capacitance, Gaussian capacitance and Asymmetricity factor for a given set of parameters: a, C_0, b, c and d.

The addition of junction and free carrier capacitance, as parallel capacitors to the steady-state single diode model, produces the dynamic single diode (DSD) model (Fig. 2). The solution of DSD model will allow the investigation of transient errors in I-V characteristics. The modus operandi of the solution is described in the following paragraphs.

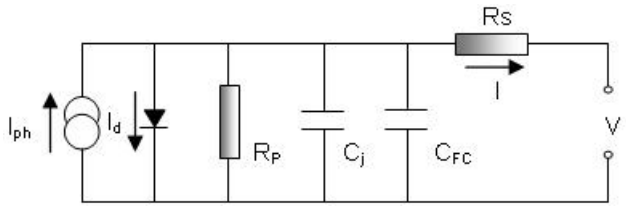


Fig. 2. Dynamic single diode model

Under illumination conditions, one can write for the currents flowing in the DSD model:

$$I = I_d + I_{sh} + I_C - I_{ph} \Rightarrow I = I_d + I_{sh} + \frac{dQ_C}{dt} - I_{ph}$$

$$\Rightarrow I = I_d + I_{sh} + \frac{d(CV_j)}{dt} - I_{ph} \Rightarrow$$

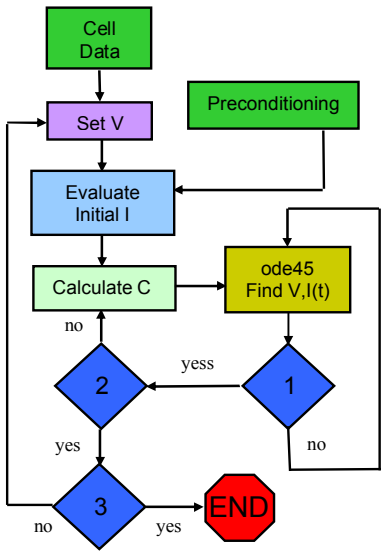
$$\Rightarrow I = I_d + I_{sh} + \frac{dC}{dt} V_j + C \frac{dV_j}{dt} - I_{ph} \quad (4)$$

where I_d is the dark current, I_{sh} the current flowing through the shunting resistance R_P, I_{ph} the photocurrent and I_C is the sum of the currents flowing through the capacitors C_j and C_{FC}. C is the sum of junction capacitance C_j and free carrier capacitance C_{FC}, Q_C is the charge accumulated to the capacitor C in time t. Taking into account that the applied voltage is ramped between measurements, but kept constant during sampling time, leads to the boundary condition of dV/dt=0 during sampling. By differentiating and re-arranging, equations (1), (2), (3) and (4), the DSD model I-V equation can be written as:

$$\frac{dI}{dt} = \frac{I - I_0\left[\exp\left(\frac{V - IR_S}{nV_T}\right) - 1\right] - \frac{V - IR_S}{R_P} + I_{ph}}{-R_S\left[C_j\left(\frac{1}{2}\frac{V_j}{V_{bi}} + 1\right) + C_{fc}\left[V_j\left(-2c^2\left(V_j - b\right) + \frac{d \cdot \log 1/2}{b^d} V_j^{d-1}\right) + 1\right]\right]} \quad (5)$$

where I_0 is the saturation current of the diode and V_T is the thermal voltage.

Equation (5) cannot be solved analytically; therefore iterative methods are employed. The solving algorithm utilises numerical differentiation formulas, and optionally, when the stiffness of the problem is high, the backward differentiation formulas, details of which can be found in [6]. Simulations were carried out in Matlab using ode15s solver. An overview of the algorithm used to determine the dynamic I-V characteristics is shown in Fig. 3.



1: Meet error tolerance?
2: Has the data point acquisition time expired?
3: Has a full I-V been recorded?

Fig. 3. Flow chart of the employed algorithm

EXPERIMENTAL APPROACH

I-V curves have been measured at two different laboratories, using similar full scale modules. Forward and reverse have been taken at different measurement speeds utilizing single and multiple short (2-5ms) or long (up to 30ms) flashes. The steady state parameters of the modules: R_S, R_P, I_0, n and I_{ph} were extracted from the long flashes, where the transient errors were shown to be minimal. The steady-state parameter extraction method of Chan and Phang [7] was employed, and the results were refined using the "Simplex" algorithm [8]. The dynamic parameters: a, C_0, b, c and d, were then extracted by fitting the short flashes.

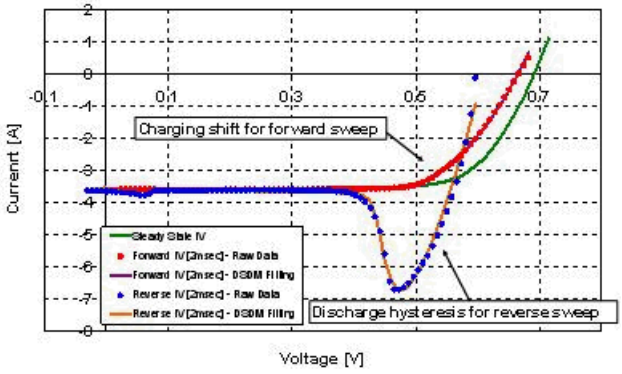


Fig. 4. Forward, reverse measurements and their fittings for 2ms flashes.

The steady-state and dynamic parameters extracted are shown in Table 1. In the following, these parameters are used in order to explain some effects of transient errors on maximum power production (P_{MPP}).

Stead-State Param.		Dynamic Param.	
I_{ph} [A]	3.679	a	0.0159
R_S [Ω]	0.0143	C_0 [Ω]	0.0028
R_P [Ω]	9.443	b	0.7542
I_0 [A]	2.641E-7	c	9.1233
n	1.5783	d	24.918

Table 1. Parameters extracted from forward and reverse sweep measurements.

EFFECTS OF CAPACITANCE AND SERIES RESISTANCE

The primary influence on the measurement accuracy is obviously the capacitance itself, which is illustrated in the following. The error here is defined as the deviation of extracted power values over the steady state values. The series resistance in the circuit, which is due to either material dependent parameters or the wiring in the solar simulator arrangement, also has an impact. In the following, voltage was amplified per 0.005 V/cell between the points, leading to a point distribution of 144 points.

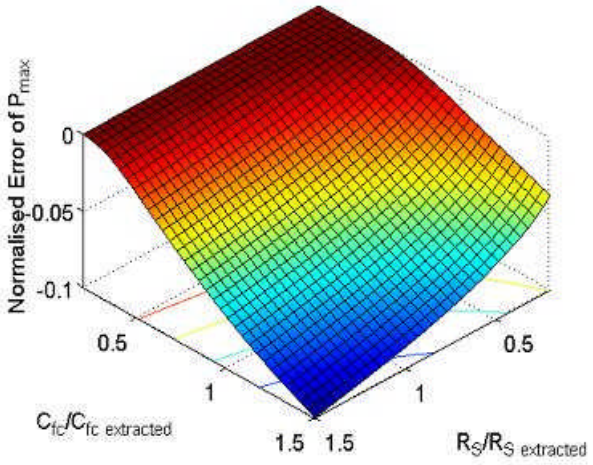


Fig. 5. Effect of series resistance and capacitance on a forward sweep.

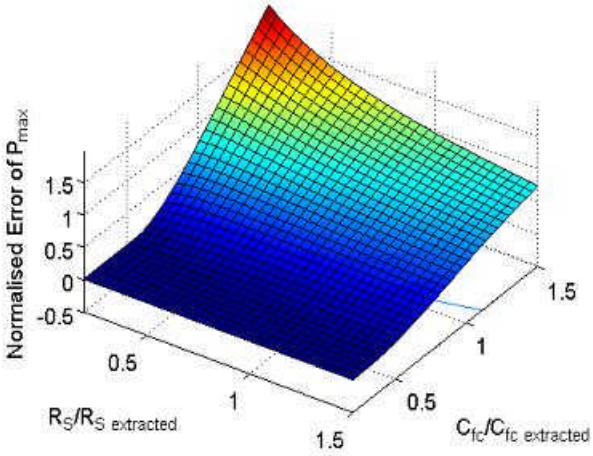


Fig. 6. Effect of series resistance and capacitance on a reverse sweep.

The effect of capacity and series resistance, normalized to the values extracted in the fitting, is shown in Fig. 5. It is shown that for forward sweeps increasing series resistance leads to increasing transient errors. The reason for this is that higher series resistances lead to lower currents for the same voltages at the junction. In contrast, a reverse sweep results in an overestimation of power production, as illustrated in Fig. 6. The effects are much more pronounced and can result in a significant overestimation of MPP. Here an increase in the series resistance leads to a decrease of the transient errors, due to the decreased discharge speed – the discharge hysteresis in the I-V characteristic gets wider but less pronounced.

EFFECT OF SWEEP TIME AND POINT NUMBERS

In this section, the effects of sweep time and point number density on the accuracy of calibration are studied. This is crucial because clearly the voltage ramp speed and the settling (integration) time must have an influence on the accuracy of device calibration.

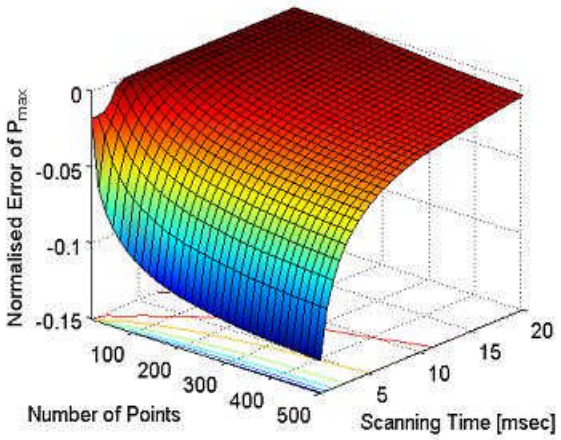


Fig. 7. Effects of scanning time and number of points on a forward sweep.

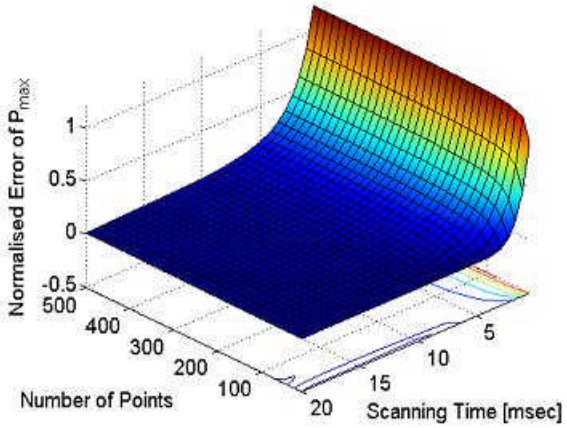


Fig. 8. Effects of scanning time and number of points on a reverse sweep.

Fig. 7 and Fig. 8 identify the effects for both forward and reverse sweeps on PMPP. It is apparent that for short flash simulators, the point number should be kept as low as possible. This will obviously incur a 'digitisation' error, due to the lack of points but minimises the capacitative transient errors.

EFFECT OF CELL AREA

Cell sizing also affects the impact of transient errors. For grid based top-contact technologies a linear increase in the cell area would cause a linear increase of the cell capacitance and a decrease of its series resistance. Fig. 9 clearly shows that scaling up the area of a cell from $0.1A_0$ to $2A_0$ –where A_0 is the cell area of the experimentally measured cell, would result in increased transient errors. As before, the MPP is significantly overestimated for reverse sweeps, while direct sweeps show an underestimation of the actual MPP.

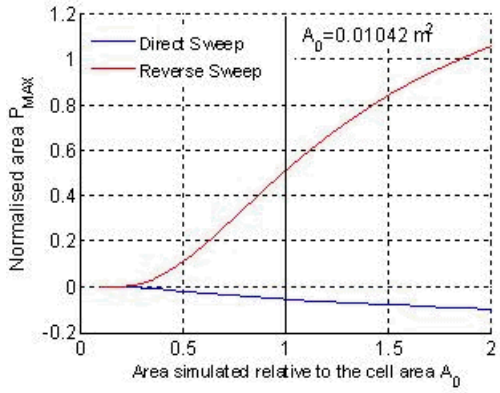


Fig. 9. Effects of cell sizing for both forward and reverse sweeps.

CONCLUSIONS

A dynamic I-V model has been presented that can represent the measurements of high capacitance solar cells to a high accuracy. Applying this model identified the total scanning time and point distribution as parameters that can be used to optimize the accuracy of a calibration procedure. It is shown in the case investigated here that a short flash solar simulator should be operated with less than 50 points and sweep time should exceed 5ms in order to reduce the underestimation of power production.

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