

Improved Surface Passivation of Rear $\text{SiN}_x/\text{AlO}_x$ Stacks in p-Type Boron-Doped Czochralski Silicon Wafers During Dark Annealing at Elevated Temperatures

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Herein, the surface passivation quality of p-type boron-doped Czochralski silicon (Cz-Si) wafers with passivated emitter and rear cell (PERC) structure during 200 °C dark annealing is investigated. During such a treatment, a reduction in the saturation current density (J_0) along with the degradation and regeneration of minority carrier lifetime can only be observed in PERC-structured wafers that fast fired at high temperatures instead of in unfired wafers, which is possibly correlated with hydrogen injected into the silicon bulk during fast firing. Besides, no notable variations in J_0 can be observed in fast-fired $\text{SiN}_x/n + /p\text{-Si}/n + / \text{SiN}_x$ symmetrical structure wafers during the same treatment, although their minority carrier lifetime undergoes degradation and regeneration cycles, demonstrating that the improved surface passivation comes from the rear surface of PERC structure. The capacitance–voltage measurement on the fabricated rear surface samples with metal-insulator-semiconductor (MIS) structure further demonstrates that the improved surface passivation is not related to field-effect passivation. By comparing the surface state density of rear surface during dark annealing, it can be concluded that the improved rear surface passivation originates from the hydrogenation of surface defects such as dangling bonds, possibly by the outdiffused hydrogen from silicon bulk during such a treatment.

1. Introduction

The conversion efficiency of commercial passivated emitter and rear cells (PERCs) fabricated on p-type Czochralski silicon (Cz-Si) has reached about 23%, which is one of the dominating solar cells technologies now and in the near future. However, boron-doped Cz-Si will always suffer from severe degradation when exposed to illumination due to the activation of boron–oxygen (B–O) complex, which is named as B–O-related light-induced degradation (LID).^[1] The B–O-related LID has been broadly investigated


and fortunately, almost solved by means of hydrogenation,^[2] by the use of other dopants such as gallium.^[3]

Then, in 2012, Ramspeck et al. reported a new kind of light-induced degradation in multicrystalline silicon (mc-Si) PERC which is activated at elevated temperatures ($>50^\circ\text{C}$), causing almost 6%_{rel} conversion efficiency loss.^[4] The light- and elevated temperature-induced degradation (LeTID) shortly attracts lots of interests from both photovoltaic (PV) industry and academia. Plenty of efforts have been put to try to reveal the underlying mechanism of LeTID, Fertig et al.^[5] and Nakayashiki et al.^[6] have demonstrated that LeTID could not be explained by either B–O-related LID or iron–boron (Fe–B) pairs. Apart from mc-Si, a study of Chen et al.^[7] has identified that the LeTID defect also presented in Cz-Si. In addition, Vargas et al.^[8] reported that LeTID defect could even be activated by thermally induced excess carriers without illumination, which makes the distinctness of B–O-related LID and LeTID be possible

in boron-doped crystalline silicon. Yli-Koski et al.^[9] and Chan et al.^[10] have found that LeTID evolution could be modulated by dark annealing (DA) pretreatments. Based on these researches, several reaction models for LeTID have been proposed, the most common one of which is related to metal impurities.^[11] However, numerous studies have also highlighted the involvement of hydrogen in LeTID defect formation and activation, particularly, Varshney et al.^[12] and Jensen et al.^[13] have evaluated the direct correlation between LeTID and hydrogen concentrations. However, more evidences are still needed to make the hydrogen-related LeTID model more convincing, especially focusing on the behavior of hydrogen-related participants during LeTID.

In this contribution, the improved rear surface passivation quality of PERC structure p-type boron-doped Cz-Si wafers during DA at elevated temperatures is investigated. By C–V measurement, the effective charge density and surface defect density located at the rear Si surface before and after DA are extracted to explore the root cause of this observation. Finally, the underlying mechanism is discussed, which may provide significant implications for the long-term stability of surface passivation in crystalline silicon PERC solar cells.

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2. Results and Discussion

Although the behaviors of LeTID defect in crystalline silicon wafers during DA have been broadly investigated in previous researches,^[8,14] more knowledge about the reaction of LeTID is still needed. **Figure 1** depicts the effective lifetime and ΔN_{leq} evolution of the Cz-Si wafers with PERC structure that unfired or fired at 750 and 850 °C during the 200 °C DA treatment. The identical observation has been reported by Chen et al.^[7] Before, only the SiN_x/H passivated Cz-Si wafers that fired at the temperature above 750 °C would present degradation and regeneration in τ_{eff} , while the τ_{eff} of the unfired Cz-Si wafers would barely change at all. In addition, the Cz-Si wafers that fired at higher temperatures will exhibit more severe degradation (higher ΔN_{leq}) with faster reaction rate constant. More discussions about the impact of peak firing temperatures on LeTID reaction under DA are presented in our previous work.^[15]

Interestingly, as plotted in **Figure 2**, the effective lifetime and ΔN_{leq} of the Cz-Si wafers with symmetrical $\text{SiN}_x/\text{n}+/p\text{-Si}/\text{n}+/\text{SiN}_x$ structure that unfired or fired at 750 and 850 °C behave similarly to the PERC-structured Cz-Si wafers, during the 200 °C DA treatment. It seems that the LeTID reactions of both sets of samples are not affected.

It has been demonstrated that, although the hydrogen-rich dielectric layers play a significant role, LeTID defect is bulk related in both mc-Si^[16] and Cz-Si.^[17] However, as plotted in **Figure 3a**, a notable reduction in J_0 of the Cz-Si wafers with PERC structure that fired at 750 or 850 °C during 200 °C DA can be observed, indicating an improving surface passivation quality, while J_0 of the unfired wafers only varies a little. Furthermore, the reduction in J_0 of the Cz-Si wafers fired at 850 °C is over 16%, which is higher than the wafers fired at 750 °C of about 12%. More importantly, the J_0 of the wafers fired at 850 °C would decrease earlier and faster than the wafers fired at 750 °C. These observations are similar with the evolution of ΔN_{leq} , as given in Figure 1, where the LeTID severity and its reaction rate are both higher in the wafers fired with higher peak temperatures. The only difference is that the reduced J_0 seems to be almost stable with only a little increase after 1000 min, as shown in Figure 3a. However, the surface passivation quality of the symmetrically structured Cz-Si wafers seems to stay unchanged during the same treatment, as shown in Figure 3b, for all the samples that unfired and fired at 750 or 850 °C, which is in good agreement to the observations of Kim et al.^[18]. This interesting result indicates that the improved surface passivation is related to the rear surface passivation of the

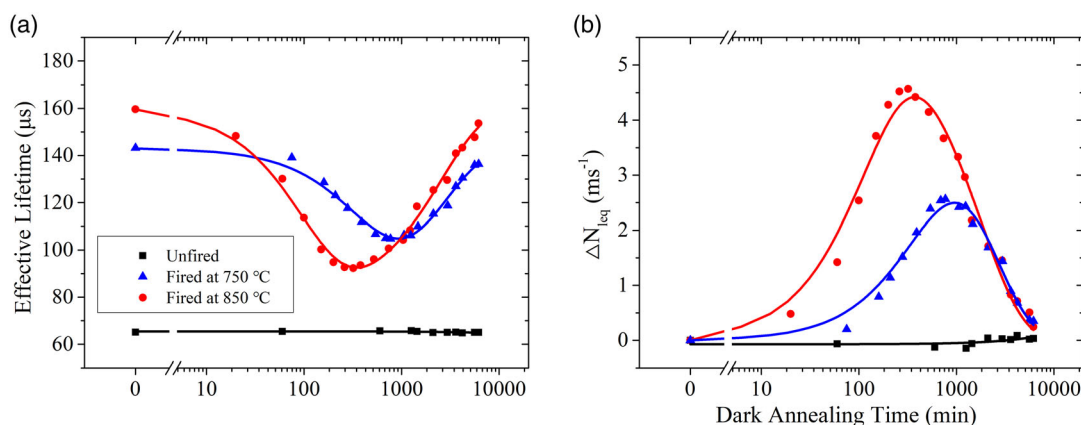


Figure 1. a) Evolution of effective lifetime and b) ΔN_{leq} of the Cz-Si wafers with PERC structure that unfired (black square) or fired at 750 (blue rectangle) and 850 °C (red circle), respectively, as a function of DA time. Solid lines are guides to the eyes.

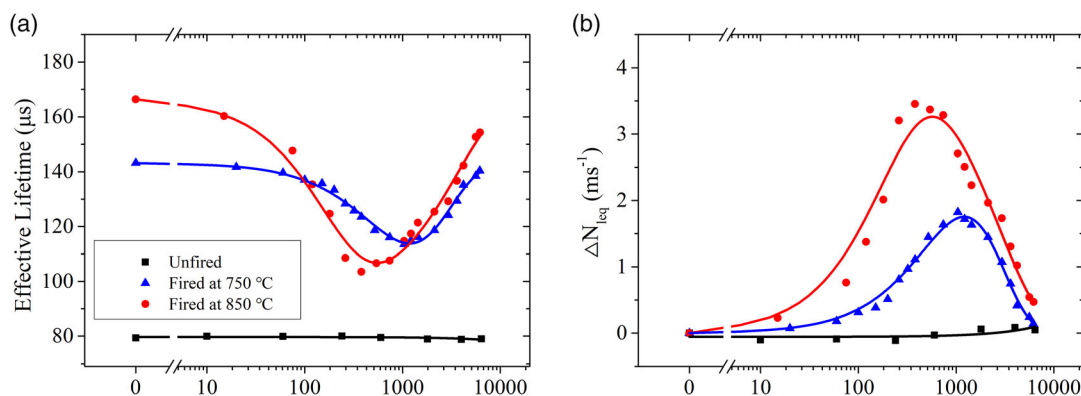


Figure 2. a) Evolution of effective lifetime and b) ΔN_{leq} of the Cz-Si wafers with symmetrical $\text{SiN}_x/\text{n}+/p\text{-Si}/\text{n}+/\text{SiN}_x$ structure that unfired (black square) or fired at 750 (blue rectangle) and 850 °C (red circle), respectively, as a function of DA time. Solid lines are guides to the eyes.

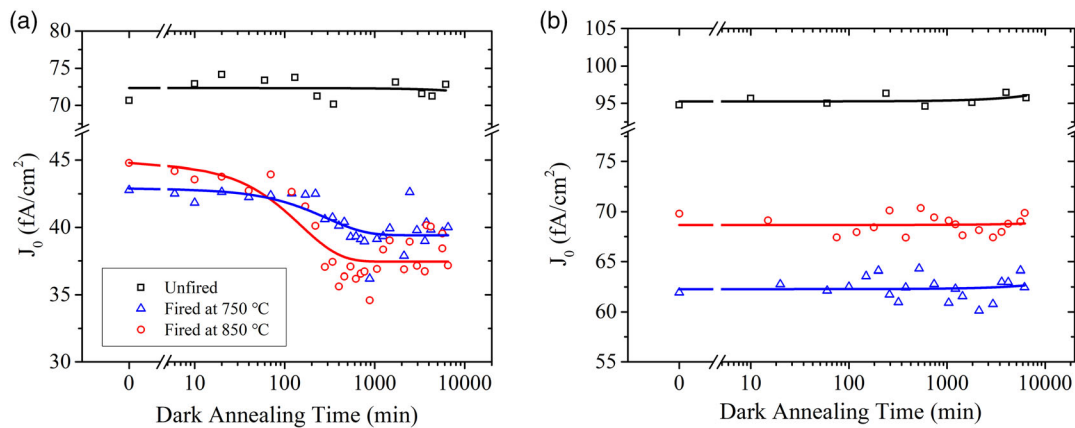


Figure 3. Evolution of J_0 of the a) PERC-structured samples and b) symmetrical $\text{SiN}_x/\text{n}^+/\text{p-Si}/\text{n}^+/\text{SiN}_x$ samples that unfired (black square) or fired at 750 (blue rectangle) and 850 °C (red circle), respectively, as a function of DA time. Solid lines are guides to the eyes.

PERC structure. It should be mentioned that the results from the asymmetric and symmetric samples might not be comparable in absolute values due to changes in sample processing that might have occurred in between the individual experiments.

Note that the observation of illuminated annealing or DA-induced variations in the surface passivation quality of dielectric layers-covered crystalline silicon wafers has been reported in the literatures before.^[8,19] However, some of the experiments were carried out during illumination which could introduce the influence of boron–oxygen complex. In addition, most of the discussions only focused on the change in J_0 , which is far away from the actual condition of the surface; as the recombination of silicon surface is quite complicated, the variations in surface states and interface charges will also induce effects.

To further explore the underlying mechanism of the enhanced surface passivation, the $C-V$ measurements during 200 °C DA are conducted on the fabricated $\text{Al}/\text{SiN}_x/\text{AlO}_x/\text{p-Si}$ metal-insulator-semiconductor (MIS) capacitor, with the results plotted in **Figure 4a**. It can be seen, when the applied bias varies from negative to positive, the capacitance of the MIS capacitor first drops

and then tends to be stable, which is consistent with the high-frequency $C-V$ characteristics of the ideal p-type semiconductor MIS structure. Comparing the $C-V$ curves after different DA time in the dark, the flat-band voltage (V_{FB}) values are relatively close within 0–1200 min. Under the assumption of fixed charges located at the Si interface, the effective charge density (Q_{eff}) can be extracted by following equation.

$$Q_{\text{eff}} = (\varphi_{\text{ms}} - V_{\text{FB}})C_i \quad (1)$$

where φ_{ms} is the difference between the work function of aluminum electrode (4.28 eV) and p-type silicon (4.99 eV), C_i is the capacitance of the insulator, and the V_{FB} is calculated from the position of the flat-band capacitance (C_{FB}) in the $C-V$ curves. The variations of the Q_{eff} with DA time is obtained, as given in **Figure 4b**.

It is shown from **Figure 3a** that the reduction in J_0 of the 850 °C-fired PERC-structured wafers mainly occurs during DA within 60–300 min, while the corresponding Q_{eff} would barely change during this period, as shown in **Figure 4b**, the negative

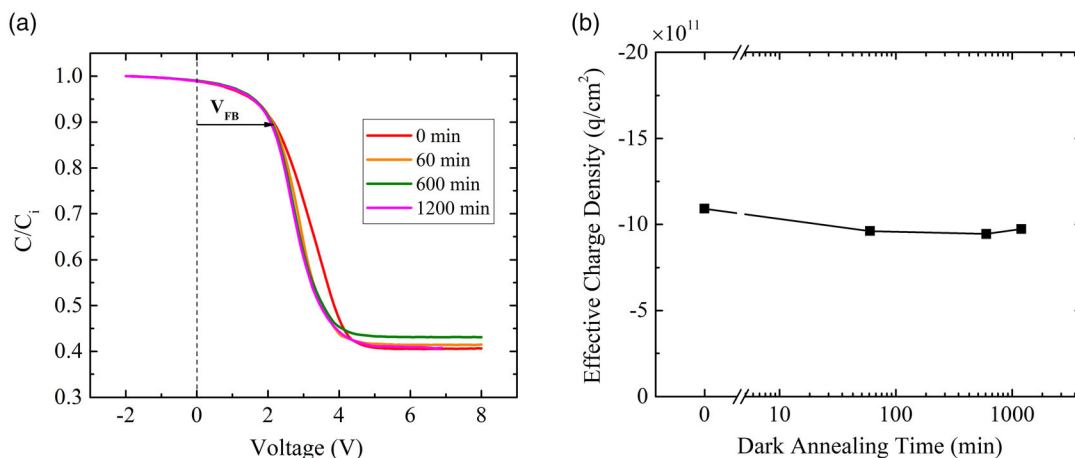


Figure 4. a) The variations of $C-V$ curves after the DA for different times at 200 °C. b) The variations of effective charge density at the Si interface as a function of DA time.

Q_{eff} only seems to drop in the first 60 min of DA and stays almost unchanged with the prolonged duration. As we know, negatively charged aluminum oxide is widely used in crystalline silicon solar cell industry to passivate the crystalline silicon surface, especially in PERC solar cells, as plenty of negative charges in rear AlO_x films can provide wonderful field-effect passivation on p-type crystalline silicon, which successfully reduced the surface recombination velocity.^[20,21] Sperber et al. also found the behavior of field-effect passivation of FZ-Si wafers to be stable during illuminated annealing,^[22] which is also similar to our condition.

On the other hand, it can be observed that the slope of the decreasing C/C_i part (2–4 V) of the C - V curves in Figure 4a would be higher after 60 min of DA, which indicates a reduced surface state density after DA. The surface state density (D_{it}) can be calculated using Terman method.^[23]

$$D_{\text{it}} = \frac{C_i}{q^2} \left[\left(\frac{d\varphi_s}{dV} \right)^{-1} - 1 \right] - \frac{C_D}{q^2} \quad (2)$$

where φ_s is the surface potential, V is the applied voltage, and C_D is the capacitance of the depletion region.

Figure 5 plots the distribution of the surface state density with energy levels of the wafer fired at 850 °C before and after DA for 1200 min, a notable decrease in D_{it} of the wafer after DA for 1200 min can be observed. This could be the root cause of the improved surface passivation quality of the wafers during DA. One reasonable speculation is that the hydrogen inside silicon bulk out-diffuses to the surface and enhances the surface passivation during DA,^[24] as only high-temperature fast firing can inject enough hydrogen into silicon bulk. According to the four state model proposed by Fung et al., after fast-firing process, the hydrogen is over saturated and will exist in molecular and B-H forms inside silicon bulk.^[25] During the DA at the temperature above 160 °C, both H_2 and B-H will dissociate into interstitial hydrogen.^[26] After a series of complicated reactions, these interstitial hydrogen atoms tend to out-diffuse toward the surface and terminate the dangling bonds of silicon surface consequently.

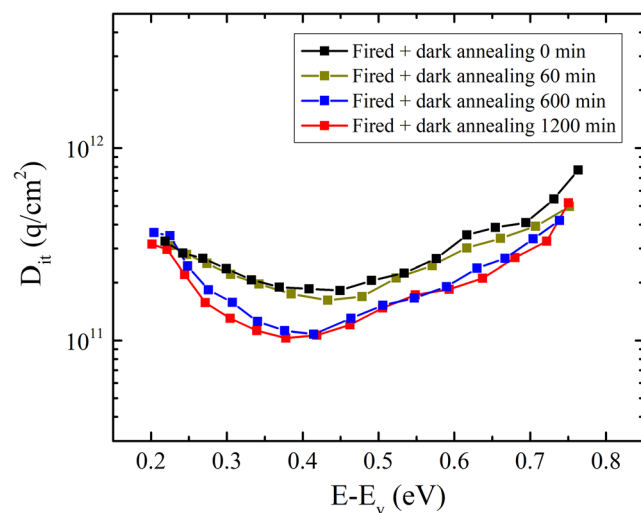


Figure 5. D_{it} as a function of the defect energy levels. Solid lines are guides to the eyes.

However, the improved surface passivation could also be induced by hydrogen from the near-surface region or from the dielectric layers. There is a study showing that AlO_x layer may suppress hydrogen in-diffusion.^[27] Note that in fast-fired PERC-structured wafers, the J_0 will decrease after ΔN_{eq} starts to increase, as plotted in Figure 1 and 3. This indicates that the improvement in rear surface passivation could be related to the behavior of hydrogen during bulk lifetime degradation and regeneration reactions. Besides, it is well accepted that higher firing temperatures will introduce more hydrogen into silicon bulk, thus, inducing more severe degradation. Note that the reduction in J_0 and the regeneration process do not fully correspond in time scale, for both the wafers that fired at 750 and 850 °C; this can be explained by the simultaneous occurrence of the degradation and regeneration,^[28] during which the interstitial hydrogen would continuously out-diffuse. In our cases, the LeTID reaction rate in the wafers fired at 850 °C is faster, which means the releasing amount and the releasing rate of hydrogen are also higher than that in the wafers fired at 750 °C. Consequently, the effect of improved rear surface passivation and its reaction rate are both more evident in the wafers fired at 850 °C.

Although some researchers have found a decreased J_0 during the LeTID process,^[29,30] there have also been some reports of degraded surface passivation quality during LeTID. For example, a notable increase J_0 , from ≈ 20 to over 90 fA cm^{-2} , along with the effective lifetime degradation of the Cz-Si wafers with symmetrical SiN_x film passivation structure during 175 °C DA has been found by Kim et al.,^[18] while a little increased J_0 , from ≈ 2 to $\approx 6 \text{ fA cm}^{-2}$, along with the effective lifetime degradation in symmetrically $\text{AlO}_x/\text{SiN}_x$ stacks-passivated wafers during same treatment, is observed, indicating that $\text{AlO}_x/\text{SiN}_x$ stacks passivation provides a better surface passivation stability during DA. Besides, fired $\text{AlO}_x/\text{SiN}_x$ stacks are expected to be in accumulation condition,^[31] which means H^+ in p-type silicon bulk will be driven toward the surface, thus, inducing improved surface passivation. Sperber et al. have also reported the similar surface degradation behavior in symmetrical SiN_x films-passivated B-doped FZ-Si during illuminated annealing.^[17] Note that all the experimental results demonstrate that the change in surface passivation quality is directly related to hydrogen. Another interesting fact is that the variations of surface passivation quality during LeTID will be significantly affected by the heavily doped layer and may be related to the impact of n^+ layers on hydrogen transportation.^[29,32] Sperber et al. have demonstrated that, during illuminated annealing at 80 °C, the symmetrical SiN_x :H-coated p-type FZ-Si wafers suffered from surface degradation, while the symmetrical P- and B- diffused wafers with SiN_x :H coatings showed an enhancement in the stability of surface passivation.^[19] This could be explained that interstitial hydrogen will be trapped in the heavily P-doped layers,^[18,32] suppressing the formation of hydrogen-related defects. The simulations made by Hamer et al. also show that the trapping of hydrogen by phosphorus leads to large concentration of hydrogen within the n^+ emitter region when annealed at 300 °C. Thus, less hydrogen will stay inside silicon bulk and out-diffuse toward the surface during prolonged DA, as compared with the symmetric passivated wafers without n^+ emitter. On the other hand, the formation of hydrogen-related defects is dependent on the concentration of hydrogen near the surface. As a conclusion, large amount

of hydrogen will be trapped in n^+ emitter after fast firing, and less hydrogen from silicon bulk (including released during LeTID reactions) will out-diffuse toward wafer surface. These out-diffusion of hydrogen will provide enhanced surface passivation instead of forming hydrogen-related defects, due to its insufficient concentration.

3. Conclusion

In this study, the variations of surface passivation of p-type boron-doped Cz-Si wafers with PERC structure during DA and its underlying mechanism have been investigated. During such a treatment, the reduction in J_0 is observed to be correlate with the degradation and regeneration of minority carrier lifetime in the fast-fired PERC structure wafers instead of in the unfired wafers, indicating an identical participant of hydrogen inside silicon bulk. However, the fast-fired $\text{SiN}_x/n^+/ \text{Si}/n^+/\text{SiN}_x$ structure samples that undergo same treatment show slight variations in J_0 , demonstrating a correlation to rear surface of PERC structure. The capacitance–voltage measurement on the fabricated rear surface samples with MIS structure rules out the impact of field-effect passivation. The decreased surface state density of rear surface after DA suggests that the improved rear surface passivation may originate from the hydrogenation of surface defects such as dangling bonds by the out-diffused hydrogen from silicon bulk during DA.

4. Experimental Section

Samples Preparation: Several p-type boron-doped Cz-Si sister wafers with a resistivity of $\approx 0.8 \, \Omega \text{ cm}$, the thickness of $\approx 180 \, \mu\text{m}$, and the size of $156 \times 156 \text{ mm}^2$ were selected, to be fabricated into the lifetime samples with PERC structure on an industrial production line including RCA cleaning, alkaline texturing, phosphorous diffusion ($\approx 140 \, \Omega \text{ sq}^{-1}$), phosphosilicate glass (PSG) removal, and rear surface polishing. Then, the $\approx 75 \text{ nm}$ SiN_x/H layer and the $\approx 10 \text{ nm}$ $\text{AlO}_x/\approx 75 \text{ nm}$ SiN_x/H stack layers were deposited on the front and rear surfaces of these wafers, respectively. Particularly, the SiN_x/H layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at $\approx 480^\circ\text{C}$, with a refractive index of 2.11 at 633 nm , while the AlO_x layer was deposited by atomic layer deposition (ALD) at $\approx 260^\circ\text{C}$. For comparison, another set of Cz-Si wafers was fabricated into the symmetrical structure of $\text{SiN}_x/n^+/\text{p-Si}/n^+/\text{SiN}_x$ by the same processing. Finally, these wafers were divided into three groups, two of them were subjected to a fast-firing belt furnace for 1 min, with the peak temperatures of 750 and 850°C for $\approx 3 \text{ s}$, respectively. The other group of samples were unfired as control set. Notably, for the ease of further treatments, these wafers were laser cleaved into $39 \times 39 \text{ mm}^2$ tokens.

LeTID Experiments: For the LeTID experiments, these three groups of samples (fired at 750 or 850°C and unfired) were subjected to a hotplate for annealing in a dark room, to avoid the influence of light-induced excess carriers. The temperature of the sample was controlled to be 200°C and monitored by a thermal couple, with the temperature inaccuracy of $\approx 3^\circ\text{C}$. The effective minority carrier lifetime (τ_{eff}) of these samples was conducted by a quasisteady-state photoconductance (QSSPC, Sinton Instruments, WCT-120) tool at an injection level of $\Delta n = 1.5 \times 10^{15} \text{ cm}^{-3}$ and at the temperature of $26 \pm 0.5^\circ\text{C}$, periodically. In this study, the evolution of τ_{eff} due to LeTID was presented with lifetime-equivalent defect density (ΔN_{leq}),^[33] which can be described by the following equation.

$$\Delta N_{\text{leq}} = \frac{1}{\tau(t)} - \frac{1}{\tau(0)} \quad (3)$$

where $\tau(t)$ and $\tau(0)$ denote the effective minority carrier lifetime measured during and before DA treatment, respectively.

To give a qualitative assessment of the surface passivation quality during LeTID experiments, the saturation current density (J_0) was extracted at an injection level of $\Delta n = 4 \times 10^{16} \text{ cm}^{-3}$ using the method proposed by Kimmerle et al.^[34]

C–V Measurement: For C–V measurement, the $\text{Al}/\text{SiN}_x/\text{AlO}_x/\text{p-Si}$ MIS capacitor was fabricated on the rear surface of the PERC-structured Cz-Si wafers that fire at 850°C , where the Al electrode with the thickness of 80 nm and the radius of 1 mm was deposited using thermal evaporation, and the InGa eutectic solution was rubbed on the backside of the wafers. The C–V measurements were carried out on deep-level transient spectroscopy (DLTS, FT1030) C–V system with a frequency of 1 MHz .

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

Czochralski silicon (Cz-Si), dark annealing, light- and elevated temperature-induced degradation (LeTID), surface passivation, surface state density

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