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Temperature and illumination dependence of silicon heterojunction solar cells with a wide range of wafer resistivities

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Abstract

Recently, the significant improvements in the surface and contact passivation of silicon (Si) solar cells as well as their bulk quality have shifted their operating point to higher injections. Hence, they are less dependent on wafer doping. This shift opens an opportunity of using high-resistivity wafers for practical photovoltaic applications, introducing a promising approach to push the cell efficiency towards the intrinsic limit and to improve the module reliability by increasing the cell breakdown voltage. Therefore, insights into the performance of Si solar cells using high-resistivity wafers at various operating temperatures are of significant interest. In this study, we investigate the temperature- and illumination-dependent performance of Si heterojunction (SHJ) solar cells using a wide range of wafer resistivities (between 3 and 1000 Ω·cm). Although a reduction in the passivation quality of the passivating contacts is observed at elevated temperature, the impact on the temperature coefficient of the open-circuit voltage (TC_{Voc})—the dominant contributor to the temperature coefficient (TC) of the cell efficiency—is very limited. Their TC_{Voc} are still dominated by the temperature dependence of the effective intrinsic carrier concentration. Furthermore, we also find that the investigated cells are more sensitive to temperature variation at lower illumination intensities. It is noteworthy that the efficiency of the cells fabricated using high-resistivity wafers is comparable to that of the reference cells at any given temperature, highlighting the potential of using high-resistivity wafers for solar cells.

KEYWORDS
high-resistivity wafers, temperature coefficient, temperature dependence, illumination dependence, passivating contacts, SHJ, silicon solar cells

1 | INTRODUCTION

It is well known that the fundamental limit of silicon (Si) solar cells, as an indirect bandgap material, is defined by the Auger recombination.[1,2] In principle, this recombination can be reduced by using high-resistivity (low doped) wafers.[1,2] However, due to the compromise between the doping density and excess carrier concentration (Δn) [or effective lifetime (τ_{eff})] at the maximum power point,[3] Si wafers with bulk resistivities below 10 Ω·cm are usually used for commercial solar cells.[4,5] This compromise can be relaxed if both the bulk quality and the surface and contacts passivation are significantly improved.

Recently, significant improvements in the quality of the passivating contacts, used to reduce the recombination at the Si-metal interfaces, have been reported.[6–10] Solar cells that integrate these contacts such as Si heterojunction (SHJ),[11,12] interdigitated back contact,[6,13] polycrystalline Si on oxide (POLO),[7] tunnel oxide passivated contact (TOPCon)[8,14] and transition-metal-oxide-based cells[9,10] exhibit high open-circuit voltages (V_{oc}) above 720 mV due to high quality passivation of both surfaces and contacts as indicated by extremely low surface saturation current densities (J_{0s})[15] below 10 fA/cm^2. These cell structures also benefit from the high bulk lifetime (τ_{bulk}) of commercially *n*-type Czochralski (Cz) substrates. Nowadays, ingot manufacturers often deliver τ_{bulk} above 3 ms across the entire ingot,[16] with the top parts reaching τ_{bulk} of 15 ms.[17] High τ_{bulk} coupled with excellent surface and contact passivation can push those solar cell operating points to the high injection regime at which Δn is usually at the order of 10^{15} cm^{-3}.[18,19] In this case, for high-resistivity wafers, their effective bulk resistivity (the bulk resistivity under the operating conditions) is significantly lower than their dark bulk resistivity as the former is defined by Δn at the high injection regime, which is remarkably higher than the doping density. Therefore, it is expected that the detrimental impacts on the fill factor (*FF*) under the operating conditions when using high-resistivity wafers for Si solar cells are no longer an issue. Hence, the above solar cell architectures may benefit from using wafers with higher bulk resistivities.[18,19]

Studies of solar cells fabricated using high bulk resistivity substrates (>10 Ω·cm), beyond the commercial resistivity range, are very limited. Glunz et al.[20] investigated the efficiencies of TOPCon cells as a function of bulk resistivity (up to 100 Ω·cm) using modelling. The simulations revealed that cell performance is independent of the bulk resistivity in the range of 5–100 Ω·cm. Jay et al.[19] reported that the efficiencies of SHJ solar cells with bulk resistivities in the range of 5–10 Ω·cm are similar to those of cells fabricated using 367-Ω·cm wafers. Simulated efficiencies of other industrially relevant cell structures with bulk resistivities in the range of 10–100 Ω·cm are shown to be comparable to those cells that use 1–10 Ω·cm wafers when the Shockley–Read–Hall (SRH) lifetimes (τ_{SRH}) of 1 and 10 ms are assumed as the dominate bulk recombination.[21] For cells fabricated on wafers with even higher resistivity (>500 Ω·cm), it has been shown by simulations that they can outperform cells made on standard wafers (<10 Ω·cm) if their τ_{SRH} is in the millisecond range.[22] This offers a great opportunity to significantly reduce the Auger recombination and hence, to push the cell efficiency of current technologies closer to the maximum theoretical efficiency. Furthermore, using high-resistivity wafers can improve the module reliability by increasing the cell breakdown voltage.[23] More importantly, there is a severe lack of experimental data of solar cells with such high bulk resistivities.

The application of high resistivity cells in the field must consider the temperature sensitivity of their electrical parameters. It is well known that the realistic operating temperatures of Si solar cells significantly deviate from the standard testing conditions (STC; at 25°C with an irradiance of 1000 W/m^2 under the AM1.5G solar spectrum), which are usually used for the characterisation and optimisation of solar cells.[24] Therefore, the temperature coefficient (TC) of high resistivity cells is a critical parameter that needs to be studied. More importantly, this parameter enables accurate evaluation of the energy yield of the power systems and hence, plays a crucial role in strategies of optimisation for solar cells and photovoltaic systems at different climatic conditions. Surprisingly, none of the previous studies determine the performance of cells with different bulk resistivities under realistic operating temperatures.

Here, we first investigate the temperature-dependent performance of SHJ solar cells fabricated using a wide range of wafer resistivities at one-sun. We then study the temperature dependence of J_{0s} of hydrogenated amorphous Si (a-Si:H)-based passivating contacts to gain a deeper understanding regarding its impacts on the TC of the open-circuit voltage (TC_{Voc})—the dominant contribution to the TC of the cell efficiency (TC_η)—of the investigated solar cells. Finally, we examine the illumination-dependent TC_{Voc} of these cells, which allows the determination of their temperature sensitivity under a wide range of illumination intensities.

2 | EXPERIMENTAL DETAILS

2.1 | Sample preparation

In this study, standard (180 ± 10 μm) and thick (380 ± 10 μm) 4-in. float zone (FZ) *n*-type Si wafers with crystal orientation of <100> and bulk resistivities of 3 Ω·cm (reference), 75 Ω·cm (medium), and ≥1000 Ω·cm (high) were used to fabricate both SHJ solar cells and test structures. The wafer surfaces were first textured using an alkaline solution, which was followed by a three-step cleaning sequence that includes the Radio Corporation of America (RCA) procedure,[25] Piranha etching[26] and hydrofluoric acid (HF) etching prior to plasma-enhanced chemical vapour deposition (PECVD).

For the fabrication of the SHJ solar cells, a stack of intrinsic and *p*-type a-Si:H [a-Si:H(*i*) and a-Si:H(*p*), respectively] layers was formed on the front side using a PECVD system. A stack of a-Si:H(*i*) and *n*-type a-Si:H [a-Si:H(*n*)] films was deposited on the rear side using the same system. The thicknesses of the a-Si:H(*i*) and doped a-Si:H films are between 6–7 and 10–15 nm, respectively. A 75-nm indium tin oxide (ITO) film was then deposited on the front side by a sputtering system through a mask to form active areas of 2 × 2 cm^2. The front grid metallisation was achieved by screen-printing of low temperature silver (Ag) paste followed by a curing process at 200°C for 30 min in

air ambient. The rear contact was formed by a full-area stack of 240-nm sputtered ITO and 240-nm sputtered Ag layers. Further details regarding the PECVD and sputtering deposition conditions can be found in Balaji et al.[27]

To investigate the temperature-dependent behaviour of the a-Si:H-based passivating contacts, symmetrical lifetime structures for τ_{eff} measurements and J_{0s} extraction were prepared. These structures were passivated with either a-Si:H(*i*/*p*) or a-Si:H(*i*/*n*) stack on both sides.

All the test structures were annealed at 200°C for 30 min in air ambient to mimic the thermal budget of the Ag paste curing process. Sketches of all the studied cells and test structures are shown in Figure 1.

2.2 | Characterisation

Current–voltage (*I*-*V*) measurements of SHJ solar cells were performed by an *I*-*V* tester from 25°C to 70°C, while Suns-V_{oc} measurements were done using a customised Suns-V_{oc} system[28,29] from 80°C to 30°C. The uncertainty associated with the temperature controller for both measurement tools is estimated at ±0.1°C. After reaching the set temperature, the solar cells were left on the heated stage for 10 min to stabilise before the measurements were done. At the completion of the temperature scan, the measurement was repeated at 25°C to ensure that the properties of the solar cells were not modified by this scan.

TCs are determined from the slopes of the linear fits of the cell parameters as a function of temperature.[30] They are normalised to the cell parameters at 25°C and presented as *relative* TCs in this study.

A spectral response system (QEX7, PV Measurements Inc.) was used to measure the external quantum efficiency (EQE) of the studied solar cells.

The symmetrical lifetime test structures were used for τ_{eff} measurements in the temperature range from 25°C to 80°C using a WCT-120TS lifetime tester (from Sinton Instruments).[31] The Kane–Swanson method[32] is used to extract J_{0s} from the τ_{eff} curves. The model of Richter et al.[33] is used to calculate the intrinsic lifetime, while the bandgap narrowing model of Schenk[34] and the model of Klaassen[35] are used to determine the effective intrinsic carrier concentration ($n_{i,eff}$) and the mobility, respectively.

Based on previous studies,[36–38] light and elevated-temperature induced degradation (LeTID) should be considered when heating and illuminating Si wafers. However, it was reported that in *n*-type FZ wafers, after 5 s of light soaking at 140°C and light intensity of one-sun, τ_{eff} reduces by less than 5%.[36] In this study, all the measurements were shorter than 5 s and at lower temperatures (25°C–80°C); hence, a significant impact by LeTID is not expected. Furthermore, the measurements at 25°C before and after the temperature scan are identical, confirming that LeTID does not affect the studied cells.

3 | RESULTS AND DISCUSSION

3.1 | Temperature-dependent performance of SHJ solar cells at one-sun

The cell parameters of the SHJ solar cells with different wafer resistivities fabricated using standard thickness and thick wafers at one-sun as a function of temperature are shown in Figure 2A–H. Overall, as expected, the V_{oc}, *FF*, pseudo fill factor (*pFF*, fill factor without the effects of series resistance), and the efficiency decrease, whereas the short-circuit current density (J_{sc}) increases at elevated temperatures.[30] The reduction of V_{oc}, *FF*, and *pFF* can be explained by the increase of $n_{i,eff}$ with increasing temperature caused by bandgap narrowing.[39] This effect also explains the improvement of J_{sc}.[30] Non-linear behaviour of *FF* in the temperature range between 25°C and 40°C, regardless of the wafer resistivity and thickness, is observed. This phenomenon commonly occurs in SHJ solar cells and is usually attributed to thermionic barriers at the heterojunctions in these cells.[40]

It is noteworthy that at a given temperature, the V_{oc} of the 180-µm-thick cells (termed hereafter as 'standard' cells, which refer only to their thickness) is higher than that of the thicker cells. The expression for the voltage (*V*) of *n*-type solar cells at high injections ($\Delta n \gg N_D$, where N_D is the dopant density) is given by:[17]

$$V_{hi} = \frac{k_B T}{q} \ln\left(\frac{(J_{ph} - J)\tau_{eff}\Delta n}{qWn_{i,eff}^2}\right) \quad (1)$$

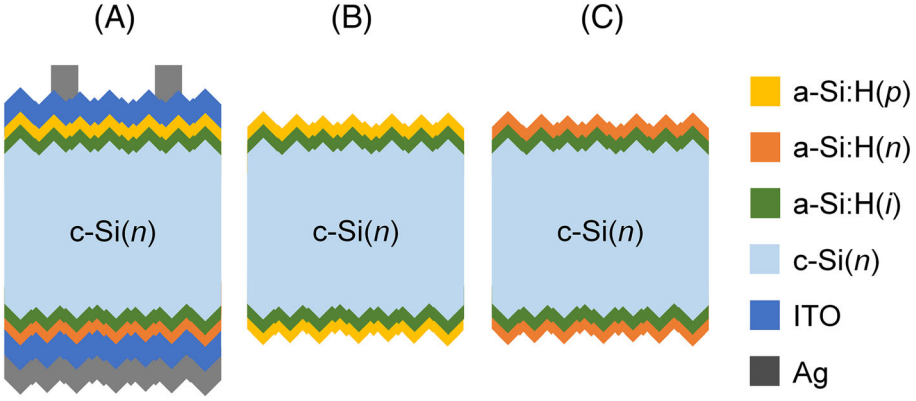

FIGURE 1 Sketches of (A) the cell structure and (B,C) symmetrical test structures for τ_{eff} measurements

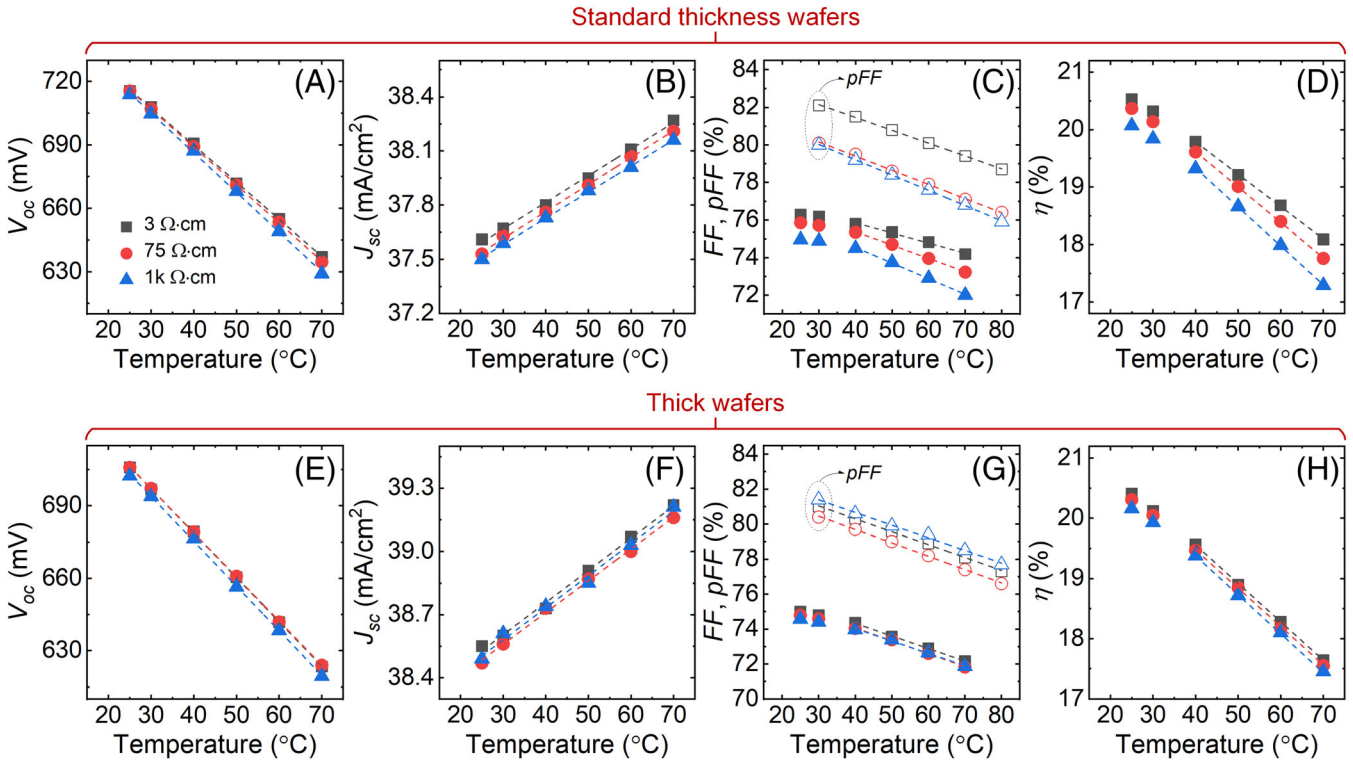

FIGURE 2 Cell parameters [V_{oc}, J_{sc}, *FF*, *pFF* (open symbols), and efficiency] of Si heterojunction (SHJ) cells using (A–D) standard thickness and (E–H) thick wafers with different wafer resistivities at one-sun as a function of temperature

where k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, J_{ph} is the photogenerated current density, J is the current density, and W is the wafer thickness. Assuming all the other parameters do not change, the reduction of the wafer thickness from 380 to 180 μm contributes to an improvement of ~20 mV in V_{oc}. However, changes in the numerator on the right side of this expression limit this improvement to the range of 10–12 mV.

Interestingly, for the standard thickness cells, the decrease of V_{oc} at elevated temperatures is less pronounced with decreasing wafer resistivity while the decrease of V_{oc} at elevated temperatures is almost identical regardless of the wafer resistivity in the case of the thicker cells. We will discuss further on these observations in the latter part of this section.

At a given temperature, J_{sc} of the thick cells is higher than that of the standard thickness cells, due to an increase in the optical absorptance at long wavelengths with increasing wafer thickness (see Appendix A, Figure A1).[41] As pointed out by Dupré et al., the temperature sensitivity of Si solar cells' J_{sc} depends on both the bandgap and the collection efficiency (f_c), as described in the following equation[24]:

$$\frac{1}{J_{sc}}\frac{dJ_{sc}}{dT}=\frac{1}{J_{sc,ideal}}\frac{dJ_{sc,ideal}}{dE_g}\frac{dE_g}{dT}+\frac{1}{f_c}\frac{df_c}{dT} \quad (2)$$

where $J_{sc,ideal}$ is the current equivalent to the sum of all photons with energy greater than the bandgap in the incident spectrum and E_g is the bandgap energy. The first term in Equation (2) represents the contribution of the bandgap narrowing to the temperature dependence of J_{sc} while the second term indicates the contribution of f_c. Although the studied cells use different wafer resistivities, the difference in the reducing rate of the Si bandgap at elevated temperature is negligible (<0.002 meV/°C, see Appendix B, Figure B1). As shown in Figure 2B,F, the increase of J_{sc} at elevated temperatures is almost identical regardless of the wafer resistivity and thickness. Hence, a similar temperature dependence of f_c for all the studied cells can be assumed.

Figure 2C,G shows *FF* and *pFF* of the investigated SHJ solar cells as a function of temperature. At STC, the *FF* of the standard thickness cells slightly decreases with increasing wafer resistivity while the thick cells' *FF* is almost identical. It can be attributed to the thickness-dependent resistive loss, which has also been reported in Sai et al.[42] At elevated temperatures, the decrease of *FF* and *pFF* is more pronounced with increasing wafer resistivity for the thinner cells. A difference between the *FF* and *pFF* trends is observed in the 3- and 1k-Ω·cm standard thickness cells. It highlights the contribution of the cells' series resistance (R_s) to the temperature dependence of *FF* and hence, the TC of the *FF* (TC_{FF}). For the thick cells, the decrease of *FF* and *pFF* at elevated temperatures is almost identical regardless of the wafer resistivity, indicating that the R_s values of these cells are less sensitive to the temperature compared to the standard thickness cells. As pointed out by Zhao et al.,[43] the temperature-dependent behaviour of Si solar cells' *FF* depends on both V_{oc} and R_s. To quantify the

contributions of these two parameters to the temperature sensitivity of the studied cells' *FF*, the following equation is used:[30,43]

$$\frac{1}{FF}\frac{dFF}{dT} = (1 - 1.02FF_0)\left(\frac{1}{V_{oc}}\frac{dV_{oc}}{dT} - \frac{1}{T}\right) - \frac{R_s}{V_{oc}/I_{sc} - R_s}\left(\frac{1}{R_s}\frac{dR_s}{dT}\right) \quad (3)$$

where

$$FF_0 = \frac{\nu_{oc} - \ln(\nu_{oc} + 0.72)}{\nu_{oc} + 1} \quad (4)$$

where FF_0 is the *FF* in the absence of R_s and shunt resistance (R_{sh}) effects and v_{oc} is the normalised V_{oc} to the thermal voltage (k_BT/q). The first term in Equation (3) reflects the contribution of V_{oc} to the temperature dependence of *FF* while the second term represents the contribution of R_s. From calculations using Equation (3), we find that the contribution of V_{oc} is dominant and accounts for more than 70% of TC_{FF}. Hence, the temperature-dependent behaviour of *FF* reflects the behaviour of V_{oc} and is dominated by the increase of $n_{i,eff}$ at elevated temperatures caused by bandgap narrowing.

The efficiency of the cells as a function of temperature is presented in Figure 2D,H. At STC, the efficiency of the standard thickness cells slightly decreases with increasing wafer resistivity, mainly due to *FF*, whereas the thick cells' efficiency is almost identical. The superior V_{oc} and *FF* of the standard thickness cells overcompensate for their lower J_{sc}, and therefore their efficiency is slightly higher than the thick cells. At elevated temperatures, as expected, the reduction in efficiency is more pronounced with increasing wafer resistivity for the standard thickness cells because of the temperature dependence of both the V_{oc} and *FF*. Meanwhile, this reduction is almost identical for the thick cells regardless of the wafer resistivity. Note that the non-linear behaviour of the efficiency in the temperature range between 25°C and 40°C regardless of the wafer resistivity and thickness is due to *FF*, as depicted in Figure 2C,G.

Figure 3A clearly shows that the V_{oc} of the standard thickness cells is more sensitive to temperatures with increasing wafer resistivity, while the thick cells' TC_{Voc} is almost independent of the resistivity. TC_{Voc} of the latter cells is nearly equal to that of the standard thickness cell with wafer resistivity of 1k Ω·cm. The obtained TC_{Voc} are comparable to those previously reported.[42] The superior TC_{Voc} of thinner cells has been also reported in the same reference.

It is well known that the temperature sensitivity of V_{oc} of a solar cell depends on both the V_{oc} and the gamma factor (γ) as described in the following equation[3]:

$$\frac{dV_{oc}}{dT} = -\frac{E_{g0}/q - V_{oc} + \gamma k_b T/q}{T} \quad (5)$$

where E_{g0} is the semiconductor bandgap linearly extrapolated to 0 K. γ represents the temperature-dependent diode saturation current density and, hence, contains information about the dominant recombination mechanism in the solar cells.[3,24,44] Since V_{oc} of the standard thickness cells at 25°C is almost identical regardless of the wafer resistivity (see Figure 2A), we hypothesise that the difference in TC_{Voc} of

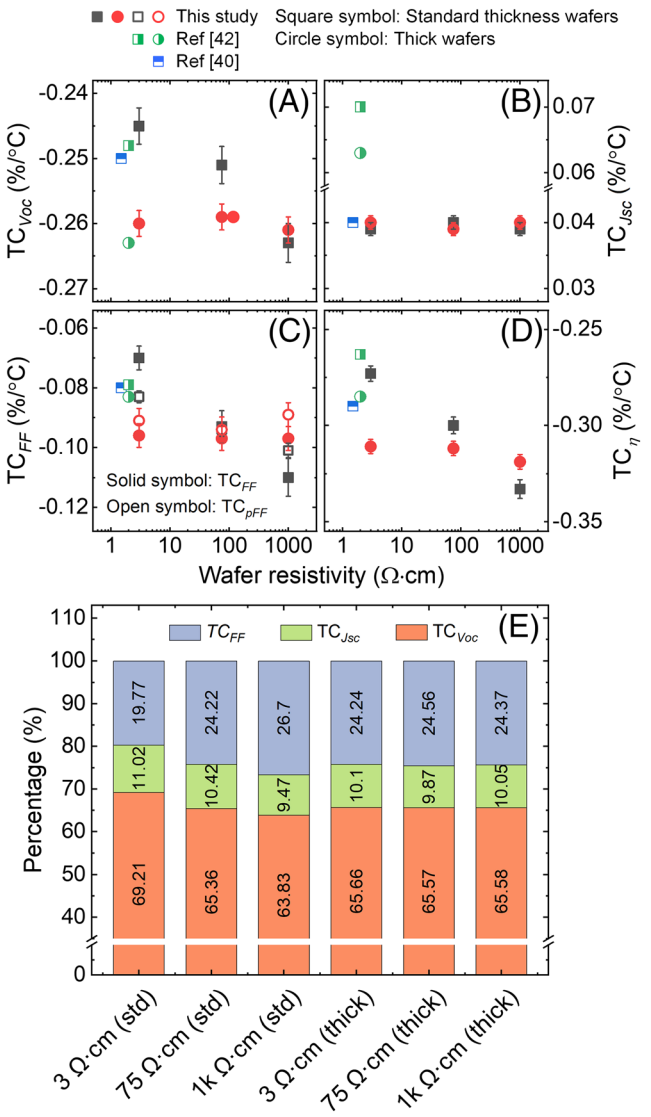

FIGURE 3 (A) TC_{Voc}, (B) TC_{Jsc}, (C) TC_{FF} and TC_{pFF} and (D) TC_η of the Si heterojunction (SHJ) solar cells extracted from linear fits of the cell parameters as a function of temperature, as shown in Figure 2. Error bars are obtained from the linear fits. Temperature coefficients (TCs) of SHJ cells reported in previous works[40, 42] are also included for comparison. The solar cells in Haschke et al.[40] were fabricated using *n*-type wafers with bulk resistivity of 1.5 Ω·cm and thickness of 180 µm. From Sai et al.,[42] we selected the TCs extracted from solar cells using *n*-type wafers with bulk resistivity of 2 Ω·cm and different thicknesses (190 and 390 µm). (E) Percentage contribution of TC_{Voc}, TC_{Jsc} and TC_{FF} to TC_η of the investigated cells

these cells might be due to different γ. To calculate γ, E_{g0} is required. E_{g0} extrapolated from E_g as a function of temperature for the different resistivity wafers are almost identical (not shown here) and are equal to 1.206 eV. Therefore, this value is applied to all the calculations of γ for the different resistivity wafers. The calculated γ of the cells at 25°C based on Equation 5 is summarised in Table 1. We observe that γ of the thick cells is less sensitive to the wafer resistivity, whereas γ of the standard thickness cells shows a larger dependence on the wafer resistivity. The performance of cells made from thinner wafers is more sensitive to the recombination at their surfaces.[45] Thus, the different γ of

the standard thickness cells may indicate a surface-related dominant recombination mechanism that might be impacted by the wafer resistivity. Ponce-Alcántara et al.[46] reported a wafer resistivity dependence of TC_{Voc} of Si solar cells, which can be justified by the relative variation of the diode saturation current density with temperature (indicating γ variation). More directly, Berthod et al.[47] attributed the wafer resistivity dependence of passivated emitter and rear (PERC) cells' TC_{Voc} to a sensible difference in the value of γ. Note that the solar cells reported in the two studies have the same wafer thickness (180–200 μm) as our standard thickness cells. These results, therefore, support the assumption above.

From Figure 3B, it seems that the TC of J_{sc} (TC_{Jsc}) is almost identical regardless of the wafer resistivity and thickness, highlighting the interesting point that was discussed above. The obtained TC_{Jsc} are comparable to that reported in Haschke et al.[40] and lower than those presented in Sai et al.[42] This difference might be due to the spectrum-dependent TC_{Jsc} when using different solar simulators.[48] The contribution of TC_{Jsc} to TC_{η} is the smallest for all the studied cells (see Figure 3E).

In Figure 3C, it can be seen that TC_{FF} of the 3-Ω·cm standard thickness cell is better than its TC of the *pFF* (TC_{pFF}), while the opposite trend is observed for the 1k-Ω·cm standard thickness cell. Meanwhile, the TC_{FF} of the standard thickness cell with the wafer resistivity of 75 Ω·cm and all the thick cells is almost identical to their TC_{pFF}. This highlights a different temperature dependence of R_s. Compared to the literature,[40,42] the obtained TC_{FF} of the 3-Ω·cm standard thickness cells is slightly better while that of the 3-Ω·cm thick cells is slightly worse. Note that Sai et al.[42] also reported better TC_{FF} for thinner cells.

As expected, the TC_{η} of all the investigated cells is dominated by TC_{Voc}, with a contribution above 60%, regardless of the wafer resistivity and thickness (see Figure 3E). It is therefore not surprising that the TC_{η} of the standard thickness cells becomes worse with increasing wafer resistivity, while it is almost identical for the thick cells. The obtained TC_{η} are slightly lower compared to the values reported in Sai et al.[42] (3-Ω·cm cells), mainly due to the higher TC_{Jsc} of the cells in this reference.

From the above discussion, we find that the temperature dependence of V_{oc} dominates that of the cell performance regardless of the wafer resistivity and thickness. Therefore, it is important to gain a deeper understanding regarding the impacts of passivating contacts on the cells' TC_{Voc} as well as knowledge regarding their performance at different illumination intensities (as usually occur in the field). In the next sections, we will focus on these two aspects.

TABLE 1 γ at STC of the SHJ solar cells with different wafer resistivities using standard thickness and thick wafers

	Gamma factor (γ)	
Wafer resistivity (Ω·cm)	Standard thickness wafers	Thick wafers
3	1.3	1.8
75	1.8	1.7
1k	2.6	1.7

Abbreviations: SHJ, Si heterojunction; STC, standard testing conditions.

3.2 | Temperature dependence of surface passivation

To assess the temperature dependence of the surface passivation, J_{0s} values were extracted from τ_{eff} measurements of symmetrical test structures and are presented in Figure 4A–D. The τ_{eff} at $\Delta n = 10^{15}$ cm^{-3} and 25°C are summarised in Table C1 (Appendix C).

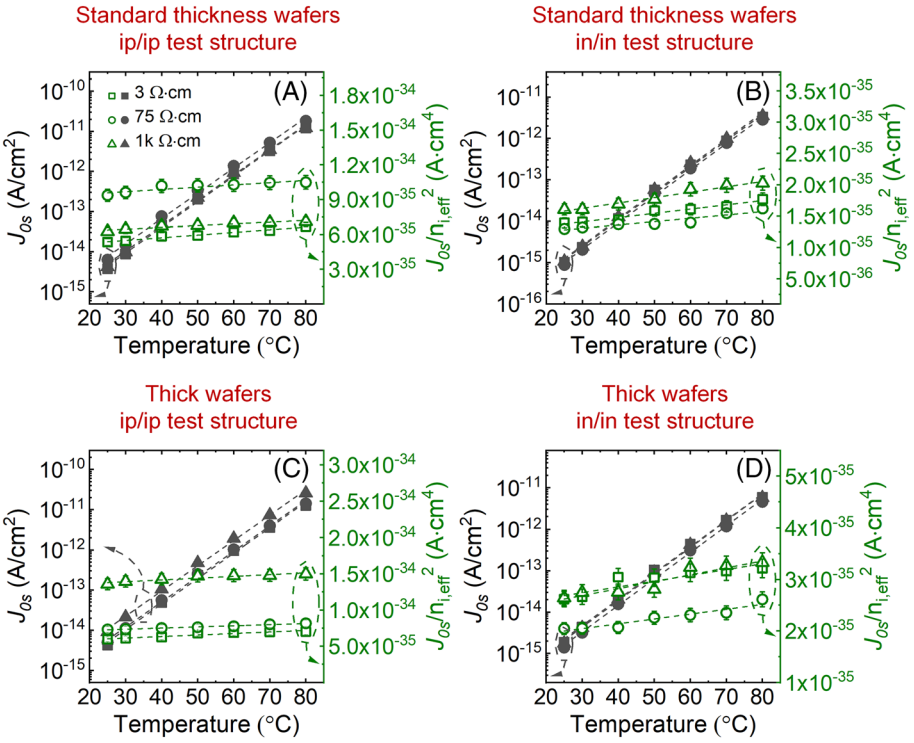

FIGURE 4 J_{0s} and $J_{0s}/n_{i,eff}^2$ ratios of (A) *ip/ip* (standard thickness wafers), (B) *in/in* (standard thickness wafers), (C) *ip/ip* (thick wafers) and (D) *in/in* (thick wafers) test structures as a function of temperature extracted from τ_{eff} measurements using the Kane–Swanson method

At 25°C, the extracted J_{0s} values are comparable to those reported in Le et al.[49] At elevated temperatures, as expected, J_{0s} significantly increases regardless of the wafer thickness or the configuration of the test structures. It is due to an increase of $n_{i,eff}$ by several orders of magnitude.[32] The $J_{0s}/n_{i,eff}^2$ ratio as a function of temperature is also presented in the figures. This ratio increases with increasing temperature indicating a slight reduction of the passivation quality at elevated temperatures. Bernardini et al.[50] also reported an increase of the surface recombination velocity of FZ *n*-type Si wafers passivated by 50-nm a-Si:H(*i*) layers with increasing temperature, which is consistent

TABLE 2 Extracted TCs of the $J_{0s}/n_{i,eff}^2$ ratio and their statistical errors determined from the standard deviation of the linear regression for the symmetrical test structures

	$TC_{J_{0s}/n_{i,eff}2}$ (%/°C)			
Wafer resistivity (Ω·cm)	Standard thickness wafers *i/p*	Standard thickness wafers *i/n*	Thick wafers *i/p*	Thick wafers *i/n*
3	0.43 ± 0.03	0.48 ± 0.05	0.35 ± 0.05	0.43 ± 0.08
75	0.21 ± 0.04	0.41 ± 0.07	0.21 ± 0.01	0.46 ± 0.06
1k	0.24 ± 0.03	0.53 ± 0.04	0.18 ± 0.03	0.51 ± 0.08

Abbreviation: TC, temperature coefficients.

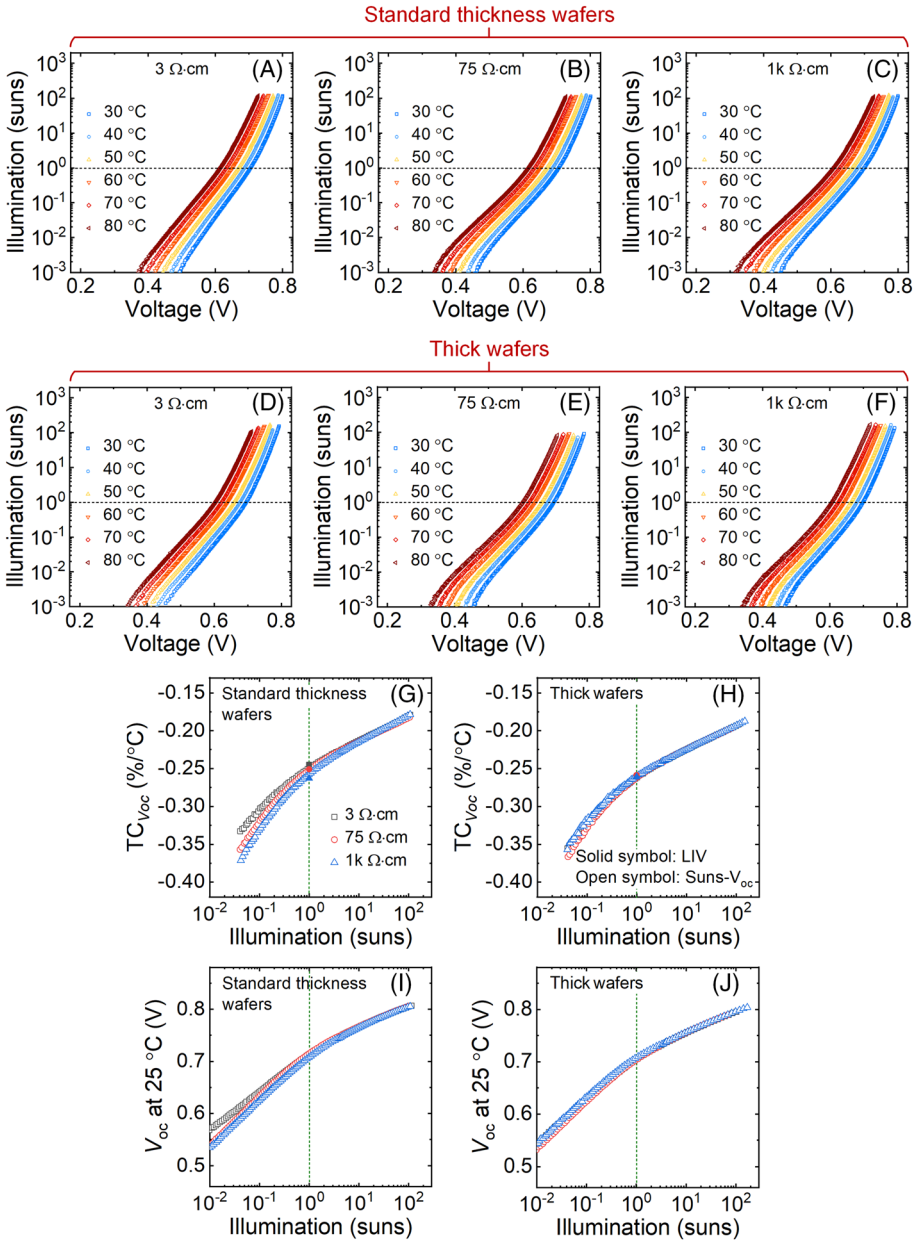

FIGURE 5 Suns-V_{oc} measurements at different temperatures for Si heterojunction (SHJ) solar cells using (A–C) standard thickness and (D–F) thick wafers. TC_{Voc} of (G) the standard thickness cells and (H) the thick cells extracted from Suns-V_{oc} (open symbols) and *I-V* (solid symbols) measurements as a function of illumination intensity. V_{oc} of (I) the standard thickness cells and (J) the thick cells extracted from Suns-V_{oc} measurements at 25°C as a function of illumination intensity

with our findings. $TC_{J_{0s}/n_{i,eff}2}$ values extracted from the linear fits of $J_{0s}/n_{i,eff}{}^2$ ratio as a function of temperature are provided in Table 2.

For standard thickness wafers, the reduction of the passivation quality of the a-Si:H(*i*/*p*)-based test structures is less pronounced for wafers with high resistivity (75 Ω·cm and above). Meanwhile, the reduction of the passivation quality of the a-Si:H(*i*/*n*)-based test structures is almost identical regardless of the wafer resistivity. Similar trends are observed for the test structures using thick wafers. Interestingly, $TC_{J_{0s}/n_{i,eff}2}$ values of the a-Si:H(*i*/*p*)-based and a-Si:H(*i*/*n*)-based test structures are almost the same for the standard thickness and thick wafers. Nevertheless, it seems the observed reduction in the passivation quality in all the cases has only an insignificant impact on TC_{Voc}. The temperature-dependent behaviour of V_{oc} and hence TC_{Voc}, is still dominated by that of $n_{i,eff}$.

3.3 | Injection and temperature dependence of SHJ solar cells

In the previous sections, we discussed the temperature-dependent performance of the investigated cells and test structures at one-sun. However, in the field, solar cells operate not only at different temperatures, but also under a wide range of illumination intensities. Therefore, insights into their performance at combinations of various temperatures and intensities are of significant interest. In this section, we use temperature-dependent Suns-V_{oc} measurements in between 0.001 and >100 suns to extract TC_{Voc} as a function of illumination intensity. This information can be used to predict the temperature sensitivity of the cells at different illumination intensities as TC_{Voc} dominates TC_{η} for all the investigated cells.

Figure 5A–F presents the Suns-V_{oc} measurements in the temperature range from 30°C to 80°C. A significant reduction of V_{oc} with increasing temperature at low illumination intensities can be observed regardless of the wafer resistivity and thickness. This reduction becomes less pronounced at higher illumination intensities (above one-sun). The extracted relative TC_{Voc} values from the Suns-V_{oc} measurements as a function of illumination intensity are presented in Figure 5G,H as open symbols. For comparison, TC_{Voc} values obtained from *I*-*V* measurements (solid symbols) at one-sun are also shown. As can be seen, TC_{Voc} values at one-sun extracted from both methods match very well (in the range of 2% and 0.2% for the standard and thick cells, respectively), supporting the observed trend of the temperature-dependent V_{oc} as discussed in Section 3.1. All the investigated cells are more sensitive to temperature variation at lower illumination intensities as indicated by the more negative TC_{Voc}. Interestingly, below one-sun, the illumination intensity dependence of TC_{Voc} is more pronounced for the standard thickness cells using higher resistivity wafers. Meanwhile, the TC_{Voc} values of the thick cells behave the same across the entire measured intensity range regardless of the wafer resistivities. To clarify this observation, the extracted V_{oc} values at 25°C are presented in Figure 5I,J. In most of the illumination range, the trend of TC_{Voc} can be explained by that of the initial V_{oc}. However, for the standard thickness cells, it seems that γ has a significant impact on their TC_{Voc} in the illumination range of 0.3–2 suns in which their TC_{Voc} become more negative with increasing wafer resistivity despite their similarly initial V_{oc}.

4 | CONCLUSION

The temperature- and illumination-dependent performance of SHJ solar cells using high wafer resistivities (up to 1000 Ω·cm) was investigated. The TCs of the main electrical cell parameters of these cells are almost independent of the wafer resistivity. Furthermore, we also found that the investigated cells are more sensitive to temperature variation at lower illumination intensities. The findings of this study demonstrate that there is no limitation in using very high-resistivity wafers for SHJ solar cells under field operating conditions. The study, therefore, set a premise for using such wafers for reducing the Auger recombination and to push SHJ solar cell efficiency towards their theoretical efficiency limit.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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APPENDIX A: EQE SPECTRA OF THE INVESTIGATED CELLS

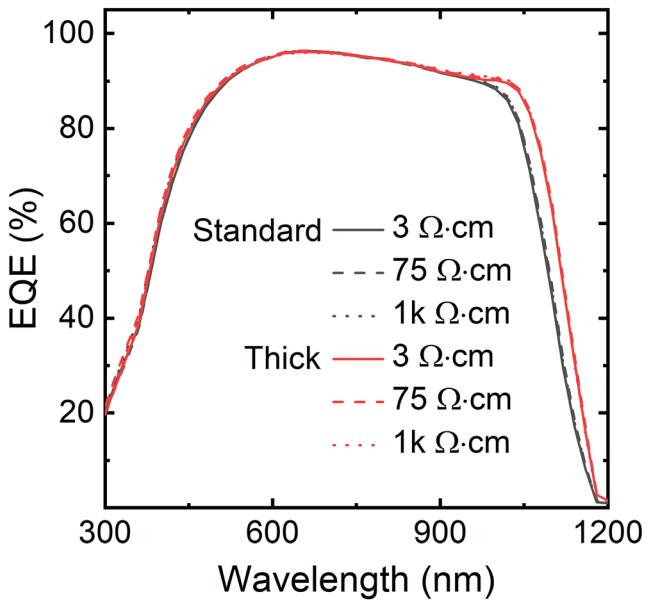

FIGURE A1 External quantum efficiency (EQE) spectra of the investigated cells

APPENDIX B: BANDGAP NARROWING OF SI AT ELEVATED TEMPERATURES

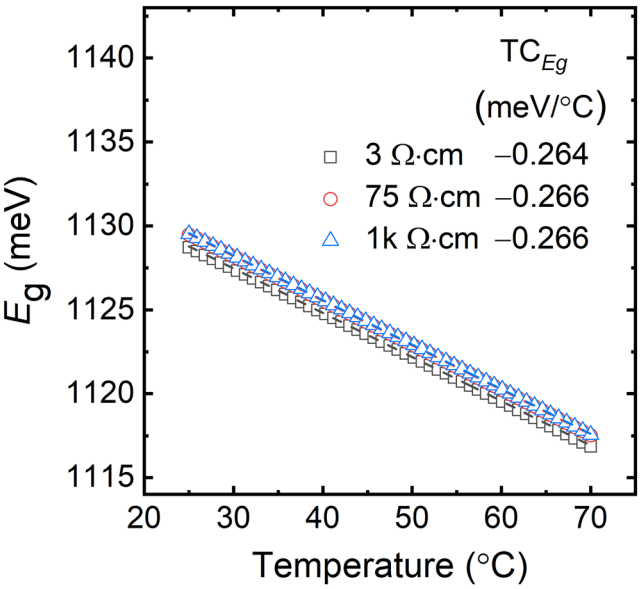

FIGURE B1 Calculated E_g of Si wafers with different bulk resistivities as a function of temperature. Temperature coefficients (TCs) of E_g are also shown.

APPENDIX C: τ_{eff} OF THE SYMMETRICAL LIFETIME TEST STRUCTURES AT $\Delta n = 10^{15}$ cm^{-3} AND 25°C

TABLE C1 τ_{eff} of the symmetrical lifetime test structures at $\Delta n = 10^{15}$ cm^{-3} and 25°C

	τ_{eff} at $\Delta n = 10^{15}$ cm^{-3} and 25°C (ms)			
Wafer resistivity (Ω·cm)	Standard thickness wafers *i/p*	Standard thickness wafers *i/n*	Thick wafers *i/p*	Thick wafers *i/n*
3	1.41	2.72	2.21	4.72
75	2.40	2.75	2.14	8.64
1k	1.48	1.28	2.45	5.52