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Temperature dependence of current–voltage characteristics of the Cd/CdS/n-GaAs/In sandwich structure

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ABSTRACT

In the present paper, Cd/CdS/n-GaAs/In sandwich structure grown by Successive Ionic Layer Adsorption and Reaction (SILAR) technique. The temperature effect on the current–voltage (*I–V*) characteristics has been investigated. For structural properties, the XRD and SEM measurements have been done and it is seen that films exhibit polycrystalline behavior. This structure has clearly demonstrated rectifying behavior by the *I–V* curves at room temperature. The temperate effect on the barrier height, ideality factor and series resistance parameters have been investigated in 80–320 K temperature range. The experimental values of barrier height and ideality factor have been calculated as 0.738 eV and 1.263 at 320 K and 0.234 eV and 4.776 at 80 K, respectively. While the ideality factor increases with decreasing temperature, the barrier height decreases. The variation of apparent barrier height and ideality factor with temperature can be explained considering lateral inhomogeneities in the barrier height in nanometer scale lengths at the CdS/n-GaAs interface. From *C–V* characteristics, built in voltage, Fermi energy level, effective barrier height and doping concentration of substrate values of this structure were calculated as a function of measurement frequency.

1. Introduction

Gallium arsenide is one of the most popular semiconductors that have intrinsic electrical properties superior to silicon, such as a direct energy gap, higher electron mobility, a high break-down voltage, chemical inertness, mechanical stability, and lower power dissipation. These advantages of gallium arsenide make it attractive for optoelectronic devices, discrete microwave devices and/or large scale integrated electronic devices [1–5]. The current transport across a metal–semiconductor junction is of interest to materials physicists and device physicists. Schottky barrier diodes (SBD) are widely studied and many attempts have been made to understand their behavior. The knowledge of the conduction mechanism across the Schottky barrier is essential in order to calculate the Schottky barrier parameters and explain the observed effects. Generally, the SBD parameters are determined over a wide temperatures range in order to understand the nature of the barrier and the conduction mechanism. Although the thermionic emission (TE) theory is normally used to extract the SBD parameters, there have been reports of certain anomalies at lower temperatures deviating from the theory. It has been known that the Schottky barrier height is temperature dependent. The SBD is practically always lower for lower temperatures. The changes are more significant at very low temperatures. On the other hand, the ideality factor of the diodes simultaneously increases with decreasing temperature [1–10]. The Schottky barrier diodes are one of the simplest metal–semiconductor contact devices in the semiconductor devices technology. The reliability and stability of the Schottky barrier diodes are dominated by the properties of the contact interface. To improve the Schottky barrier height, the formation of high-quality Schottky diode with a low ideality factor by using thin interfacial films is one of essential process for devices [11]. It is well known that interface layer has a dominant influence on the device performance, reliability and stability. Therefore, metal-interfacial layer-semiconductor or metal–insulator–semiconductor (MIS) structures are of essential importance in the device modification applications of semiconductor devices. Such sandwich structures with very thin interlayer behave electrically like Schottky contacts. The barrier heights of such devices depend on the nature of the interfacial layer, its thickness, and the specific metal used [3].

SILAR method is the trend which involves the grown of thin films from solution, ionic layer by layer at room temperature and at normal pressure. Single SILAR deposition cycle involves the immersion of the substrate alternately in cationic and anionic precursor solutions and rinsing between every two consecutive

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immersions with de-ionized water to avoid homogeneous precipitation in the solution, so that only the tightly adsorbed layer stays on the substrate. The adsorption is a surface phenomenon occurring due to attractive force between ions and surface of substrate. This attractive force is of Van der Waals type that basically originates due to the residual or unbalanced force present in the substrate. Thus, ad-atoms are held on the surface of the substrate by that residual force [12–18].

The CdS thin film has been directly formed on n-type Si substrate to obtained Cd/CdS/n-Si/Au–Sb structure by using SILAR method. An Au–Sb electrode has been used as an ohmic contact. The characteristics parameters such as barrier height, ideality factor and series resistance of Cd/CdS/n-Si/Au–Sb structure have been calculated from the forward bias I–V and reverse bias $C^{-2}-V$ characteristics. The diode ideality factor and the barrier height values have been calculated as $n=2.06$ and $\Phi_b=0.92$ eV by applying a thermionic emission theory, respectively. The diode shows non-ideal I–V behavior with an ideality factor greater than unity that can be ascribed to the interfacial layer, the interface states and the series resistance. At high current densities in the forward direction, the series resistance (R_s) effect has been observed. The values of R_s obtained from $dV/d(\ln I)$–I and $H(I)$–I plots are near to each other's ($R_s=182.24$ kΩ and $R_s=186.04$ kΩ, respectively). This case shows the consistency of the Cheung's approach. In the same way, the barrier height calculated from C^{-2}–V characteristics varied from 0.698 to 0.743 eV [18].

In this study, the SILAR method has been used for growth the CdS thin film. Firstly, structural and optical properties of CdS thin film have been investigated. Up to now, much effort has been devoted to the preparation sandwich structures. But, there has not been any report seen on preparation of such structures (on directly n-GaAs semiconductor) by means of the SILAR method. In this study, we presented how Cd/CdS/n-GaAs/In sandwich structure was prepared, calculated characteristic parameters and studied temperature effect on the structure. Cd/CdS/n-GaAs/In structure is similar to MIS structures. Firstly, structural and optical properties of CdS thin film have been investigated. Afterward, some electrical properties of the Cd/CdS/n-GaAs/In sandwich structure have been investigated in the temperature range of 80–320 K by steps of 20 K.

2. Experimental procedure

In this study, n-type GaAs (100) wafer of relatively carrier density 2.5×10^{17} cm^{-3} was used to fabricate Cd/CdS/n-GaAs/In sandwich structure. The substrate was sequentially cleaned with trichloroethylene, acetone, methanol and then rinsed in deionised water. The native oxide on the surface was etched in sequence with acid solutions (H_2SO_4:H_2O_2:H_2O=3:1:1) for 60 s, and HCl:H_2O=1:1 for another 60 s. After a rinse in deionised water and a blow-dry with nitrogen, a low resistance ohmic contact on the back side of the sample was formed by evaporating indium metal at a pressure of about 10^{-5} Torr, followed by annealing at 425 °C for 3 min in N_2 atmosphere. After ohmic contact was made, the ohmic contact side and the edges of the n-GaAs semiconductor substrate was covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed to the cationic precursor solution employed for the SILAR method. For the deposition of CdS thin film, a well-cleaned n-type GaAs substrate was immersed in the cationic precursor solution ($CdCl_2$) for 40 s, causing cadmium ions to be adsorbed on the surface of the n-type GaAs substrate. Then, the substrate was immersed in doubly distilled water for 50 s to prevent irregular precipitation. The substrate was finally immersed in the anionic precursor solution (Na_2S) for 40 s. Sulfide ions reacted with the adsorbed cadmium ions on the n-type GaAs substrate. The substrate was then immersed in double-distilled water for 50 s. Thus, one cycle of CdS film deposition is completed. For homogeneous thin film layer, this cycles have been repeated as 30 cycle. Cd dots with diameter of about 1.0 mm (the contact area=7.85×10^{-3} cm^2) were evaporated on the CdS thin film in vacuum coating unit at about 10^{-5} Torr. In this way, the Cd/CdS/n-GaAs/In sandwich structure was obtained. A schematic cross-section of the Cd/CdS/n-GaAs/In sandwich structure is shown in Fig. 1. The thickness of CdS layer was calculated to be 286 nm approximately from high frequency capacitance–voltage measurements. In order to observe the temperature effect, the I–V characteristics of device were measured in 80–320 K temperature range by using a temperature controlled Leybold Heraeus closed-cycle helium cryostat and HP4140B picoamperemeter under dark conditions.

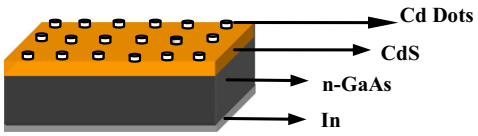

Fig. 1. Structure diagram of the fabricated device.

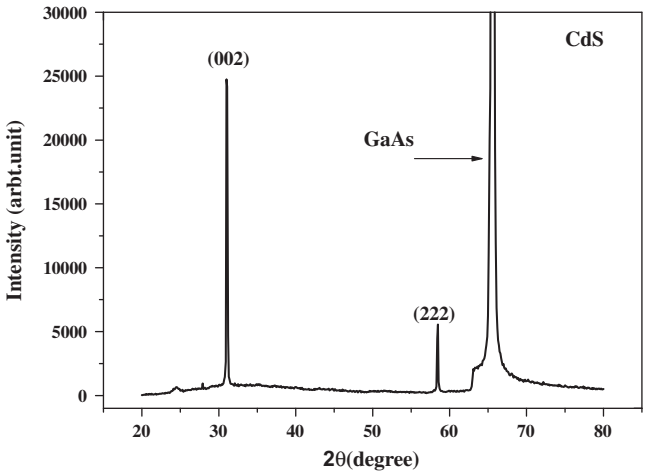

Fig. 2. XRD pattern of CdS thin films grown on n-GaAs semiconductor.

3. Results and discussion

3.1. Structural, morphological and optical properties of the CdS thin film

The structural analysis of CdS film was carried out by using XRD with varying diffraction angle 2θ, from 20 to 70°. The XRD patterns of this film grown on n-GaAs substrate are shown in Fig. 2. It is seen from the XRD patterns that the CdS film is in polycrystalline orientation along different planes and phases. These planes are (002) and (222). The plane of n-GaAs (100) substrate is clearly observed in Fig. 2 and the plane intensity is dominant when compared with the others. It is seen from Fig. 2 that, the crystallization is very high.

It is known that the surface properties of the films influence their optical and electrical properties which are important factors in applications to optoelectronic devices. Thus, it is very important to investigate the surface morphology of the films. SEM is well-known technique to study the surface morphology of thin films. Fig. 3 shows SEM image of the CdS film. It is observed that the as-deposited CdS thin film has well covered the substrate.

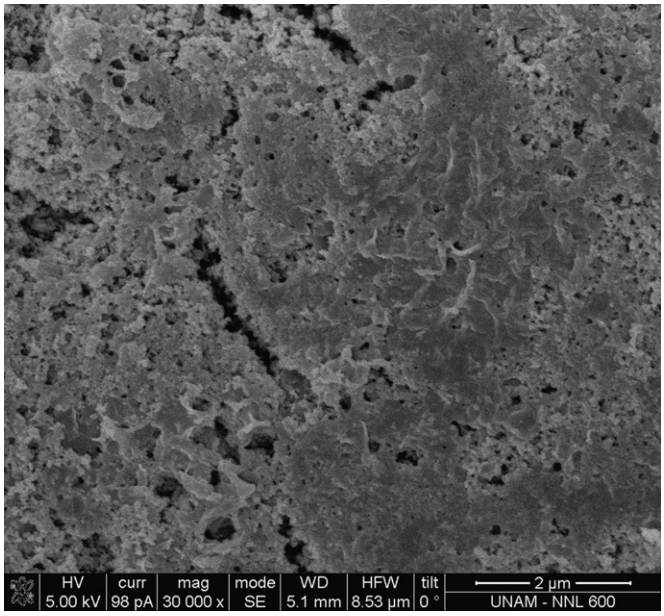

Fig. 3. SEM micrographs of CdS thin film at room temperature.

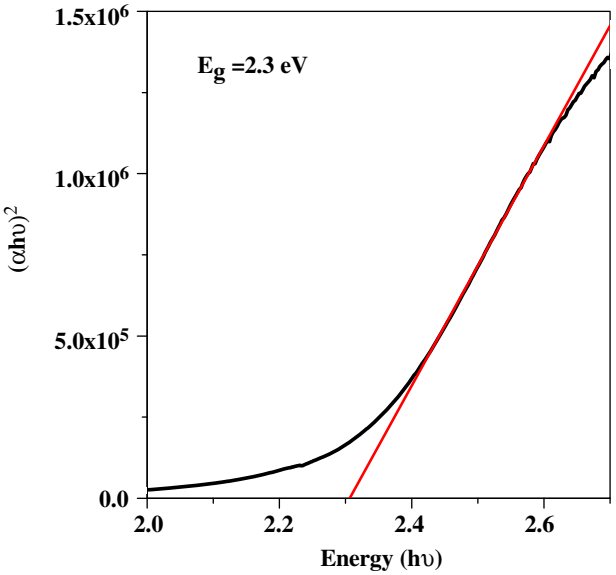

Fig. 4. Plot of $(\alpha h\nu)^2$ versus $(h\nu)$ of CdS thin film at room temperature.

Also, there are macroscopic defects like void, pinhole, peeling or cracks on the film surface. In spite of these, from the featureless surface morphology of the deposited CdS thin film, we can anticipate that these films will exhibit very low optical scattering losses and should therefore be suitable for optoelectronic applications.

The absorption measurements of CdS thin film were carried out at room temperature. The energy band gap value of thin film was calculated with the help of the optical absorption spectra. To determine the energy band gap, we plotted $(\alpha h\nu)^2$ versus $(h\nu)$ where α is the absorption coefficient and $h\nu$ is the photon energy. The theory of inter band absorption shows that at the optical absorption edge the absorption coefficient α varies with the photon energy $h\nu$ according to Ref. [17];

$$\alpha(h\nu) = B(h\nu - E_g)^{1/2} \tag{1}$$

where B is a constant, E_g is the optical band gap. Thus a plot of $(\alpha h\nu)^2$ versus $(h\nu)$ is a straight line whose intercept on the energy axis gives the energy gap, E_g. The graph $(\alpha h\nu)^2$ versus $(h\nu)$ has been given in Fig. 4. The band gap energy of film has been determined by the extrapolation of the linear region on the energy axis $(h\nu)$ as shown in Fig. 4 as 2.3 eV. This result is agreement with the literature [19–22].

3.2. Effects of sample temperature on electrical properties of the Cd/CdS/n-GaAs/In sandwich structure

The parameters of the heterocontact were obtained using a simple Schottky model which assumes a well defined fixed potential barrier at the interface over which the electrons are thermionically emitted [23]. The *I–V* equation in respect to the thermoionic emission theory in the presence of interfacial layer is given by [1]

$$I = AA^* T^2 \exp\left(\frac{-q\Phi_b}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \tag{2}$$

where A is the effective area of diode, A^* is the effective Richardson constant, Φ_b is the barrier height, T is the temperature, q is the elementary charge, k is the Boltzmann constant, R_s is the series resistance and n is the ideality factor. The saturation current I_0, may be denoted by

$$I_0 = AA^* T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \tag{3}$$

and is obtained by extrapolation of the forward or reverse bias *I–V* curves to zero applied voltage. The slope of linear portion of the *I–V* curve gives the ideality factor, which means that the deviation from the ideal *I–V* characteristics can be due to the presence of an indefinable interfacial layer that introduces the interface states located at CdS/n-GaAs interface. Ideality factor n can be written as:

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \tag{4}$$

In addition, the barrier height can be obtained from the equation,

$$q\Phi_b = kT\ln\left(AA^* T^2/I_0\right) \tag{5}$$

n and Φ_b values can be calculated from Eqs. (4) and (5). Fig. 5 shows the experimental semi-logarithmic forward and reverse bias *I–V* characteristics of the Cd/CdS/n-GaAs/In sandwich structure in the temperature range of 80–320 K by the steps of 20 K. In the forward bias case of the device, the In electrode (ohmic contact) was negatively biased with respect to the Cd electrode on the CdS thin film. As can be seen from Fig. 5, a slight saturating behavior is observed in the reverse bias because the junction-like conduction processes occurring in depletion region should limit the measured heterojunction reverse current. The experimental forward and reverse bias *I–V* characteristics of the device mention that the appropriate rectifying junction-like formulas can be applied to examine its *I–V* characteristics.

The experimental values of the ideality factor and the barrier height were determined from Eqs. (4) and (5) at each temperature. The experimental values of ideality factor and the barrier height were calculated as 1.263 and 0.738 eV at 320 K and 4.776 and 0.234 eV at 80 K, respectively. The high values of n can be attributed to the effects of the bias voltage drop across the interfacial layer (between CdS and n-GaAs) and series resistance. The ideality factor value of 1.263 at 320 K for this structure indicate that the device obey non-ideal diode. Cd/CdS/n-GaAs/In structure is similar to MIS structures. Semiconductor contacts formed under these conditions are not intimate contact because an interfacial layer separates them. Song et al. [24] have also

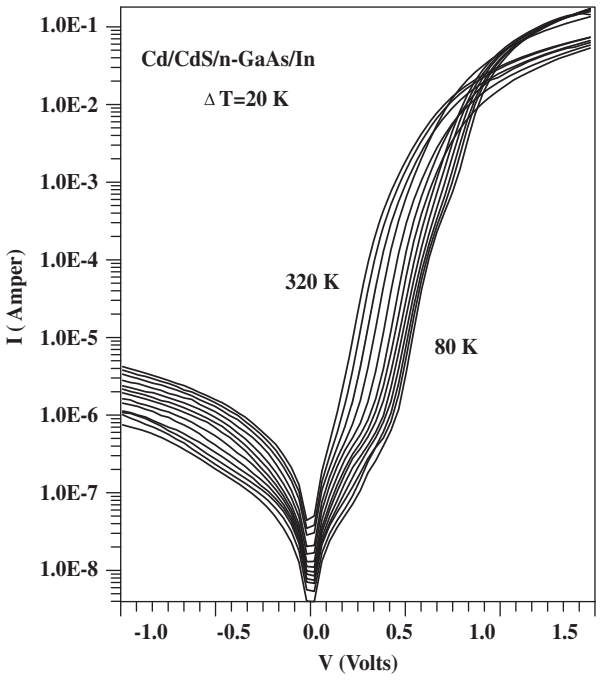

Fig. 5. Current–voltage characteristics for Cd/CdS/n-GaAs/In sandwich structure at different temperatures in the range 80–320 K.

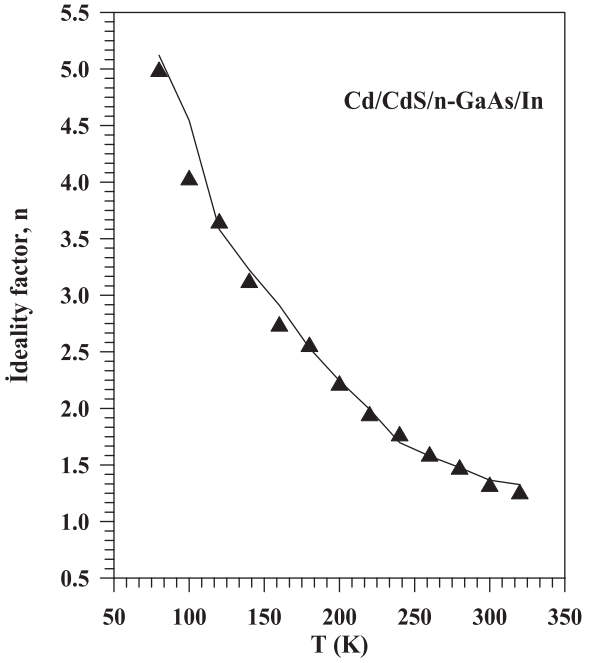

Fig. 6. Variation of ideality factor with temperature for Cd/CdS/n-GaAs/In sandwich structure.

suggested that the barrier inhomogeneities can occur as a result of inhomogeneities in the interfacial layer composition, non-uniformity of the interfacial charges and interfacial layer thickness. In such cases, the current across the junction may be greatly influenced by the presence of the barrier height inhomogeneity [25–27]. The n versus T graph has been shown in Fig. 6. As can be seen from Fig. 6, a very strong temperature dependence of ideality factor shows that the forward bias transport properties of the present device at intermediate and high bias voltage are not well modeled by the thermionic emission only even when it was modified by the incorporation of a series resistance effect. This

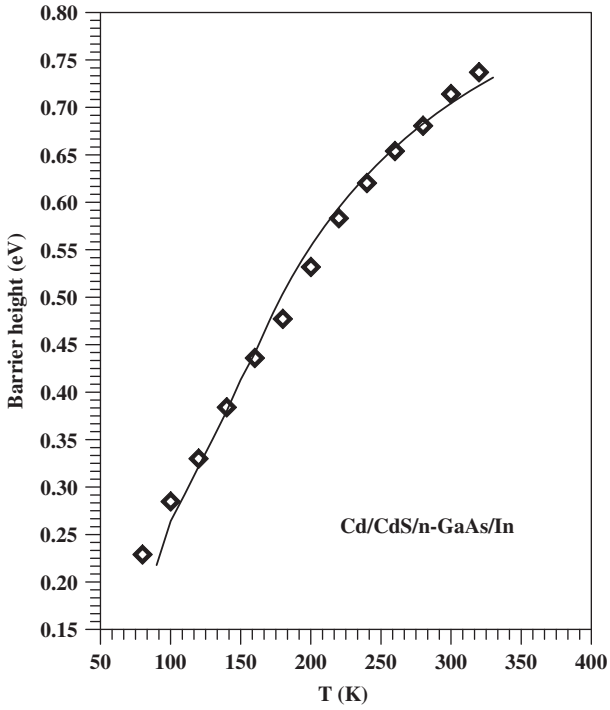

Fig. 7. Variation of apparent barrier height with temperature for Cd/CdS/n-GaAs/In sandwich structure.

suggests that the current processes occurring in the high resistivity CdS layer of the Cd/CdS/n-GaAs/In structure would be a possible alternative candidate in determining the forward current at the intermediate and high bias regimes beyond that of the low-bias diode-like behavior. Fig. 7 shows the temperature dependence of the barrier height obtained by Eq. (5). As seen in Fig. 7, when the ideality factor increases with decreasing temperature, the barrier height decreases. Image-force lowering, tunneling through the barrier, an alteration of the charge distribution near the interface and/or generation–recombination in the depletion region are the phenomena routinely invoked as the reasons for these anomalies. From our investigations on the combined effects of this process is not enough string to take into account for the measured fluctuations in the barrier height of Cd/CdS/n-GaAs/In structure over most of the temperature region. These potential fluctuations have been attributed to a variety of causes including interface roughness due to non-uniform thickness and composition of the interface layer, grain boundaries, non-uniformity of interfacial charges, etc., [28–31].

The decrease in the barrier height with decreasing temperature can be explained by the lateral distribution of barrier height, if the barrier height has a Gaussian distribution of the barrier heights over the junction area with the mean barrier height $\overline{\Phi}_b$and standard deviation σ_s. The Gaussian distribution of the barrier heights yields the following expression for the barrier height [28,30]:

$$\Phi_{ap} = \overline{\Phi}_b - \frac{q\sigma_s^2}{2kT} \tag{6}$$

where Φ_{ap} is the apparent barrier height measured experimentally. The temperature dependence of σ_s is usually small and can be neglected. The observed variation of the ideality factor with temperature in the model is given by [30]

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{7}$$

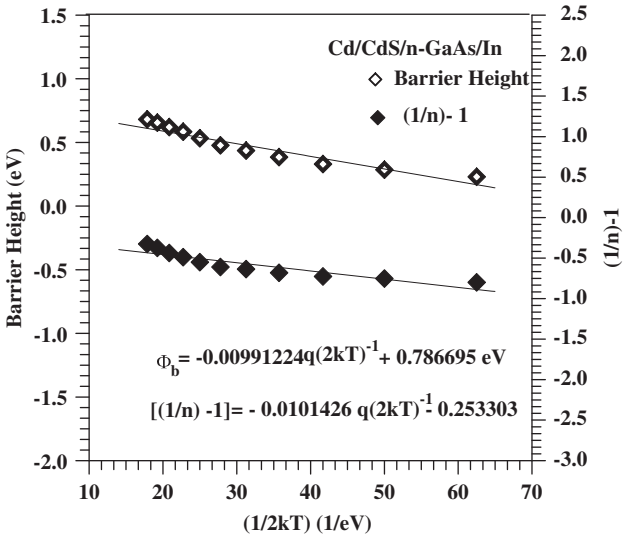

Fig. 8. Zero-bias apparent barrier height and ideality factor versus $(2kT)^{-1}$ curves of the Cd/CdS/n-GaAs/In sandwich structure according to the Gaussian barrier height.

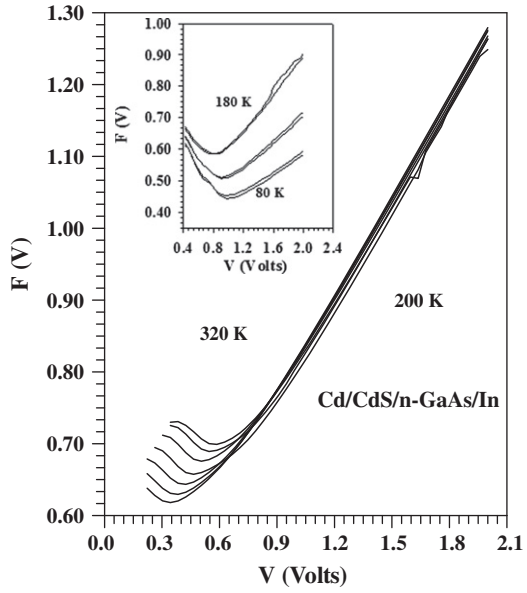

Fig. 9. $F(V)$ versus V plot of the Cd/CdS/n-GaAs/In sandwich structure at various temperature.

where n_{ap} is the apparent ideality factor and ρ_2 and ρ_3 quantify the voltage deformation of the barrier height distribution.

According to Eqs. (6) and (7), the plot of apparent barrier height versus $1/T$ (Fig. 8) should be a straight line that gives zero-bias mean barrier height $\overline{\Phi}_{b0}$ and zero-bias standard deviation σ_s from the intercept and slope, respectively. As can be seen from Fig. 8, the values of $\overline{\Phi}_{b0}$, σ_s were obtained as 0.787 eV and 0.0099 eV from the experimental apparent barrier height Φ_{ap} versus $1/T$ plot and in the same figure, the plot of apparent ideality factor n_{ap} versus $1/T$ should be a straight line that gives voltage coefficients ρ_2 and ρ_3 from the intercept and slope, respectively. The values of $\rho_2=0.253$ V and $\rho_3=0.010$ V were obtained from the experimental apparent ideality factor versus $1/T$ plot. The standard deviation is a measure of the barrier homogeneity. The lower value of σ_s corresponds to more homogenous barrier height. It was seen that the value of $\sigma_s=0.0099$ eV is small compared to the mean value of $\overline{\Phi}_{b0}=0.787$ eV, and it indicates the presence of the interface inhomogeneities.

Norde [32] proposed a method to determine value of the series resistance. Norde's function $F(V)$ has been used to obtain the values of barrier height and the series resistance. The $F(V)$ function is defined as [32]

$$F(V)=\frac{V}{\gamma}-\left(\frac{kT}{q}\right)\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{8}$$

where γ is an arbitrary constant greater than the ideality factor, $I(V)$ is current obtained from the I–V curve and the other parameters are described above. Thus, the effective barrier height and series resistance can be determined by

$$\Phi_b=F_m+\left[\frac{(\gamma-n)}{n}\right]\left[\frac{V_m}{\gamma}-\frac{kT}{q}\right] \tag{9}$$

$$R_s=(\gamma-n)\frac{kT}{qI_m} \tag{10}$$

Once the minimum of the $F(V)$—V plot is determined, the barrier height can be obtained from here, where F_m is the minimum point of $F(V)$ curve, and V_m is the corresponding voltage, I_m is the current corresponds to the minimum V_m. A plot of $F(V)$ versus V for the Cd/CdS/n-GaAs/In structure at different temperatures is shown in Fig. 9. From the $F(V)$–V plots, the some parameters of the Cd/CdS/n-GaAs/In sandwich structure, (Φ_b, R_s) have been determined. The values of barrier height and series resistance obtained from the $F(V)$–V curves are given in Fig. 10 as a function of temperature. As seen in Fig. 10, barrier height and series resistance are strongly temperature dependent and while the series resistance increases with decreasing temperature, the barrier height decreases. Since current transport across the CdS/n-GaAs interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers and therefore current transport will be dominated by current flowing through the patches of lower barrier height [33]. When the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant barrier height will increase with the temperature and bias voltage. In the other words, more electrons have sufficient energy to overcome the higher barrier when barrier height builds up with increasing temperature and bias voltage. The series resistance is an important parameter on the electrical characteristics of the rectifying contacts or junctions. This parameter is influenced by the presence of the interface layer at junction and

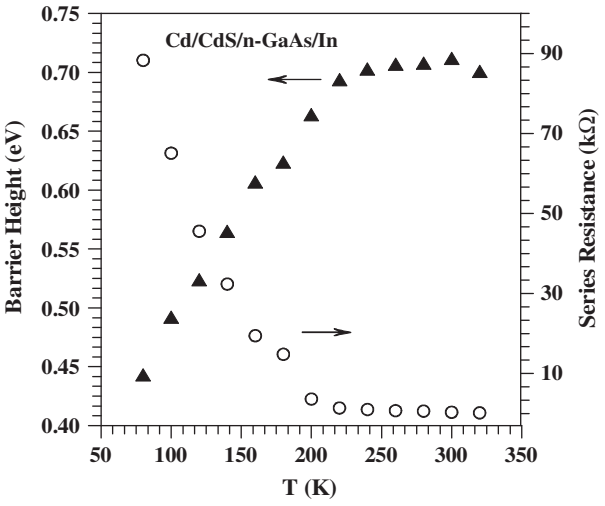

Fig. 10. Temperature dependence of the barrier height and series resistance obtained from the Norde's functions of Cd/CdS/n-GaAs/In sandwich structure.

leads to non-ideal forward bias *I–V*. In general, the forward bias *I–V* characteristics are linear on a semi logarithmic scale at low forward bias voltages but deviate considerably from linearity due to the effect of series resistance R_s and other effects. When a forward bias *V* is applied across the device, the applied voltage *V* will be shared by the interfacial layer, the depletion layer and the series resistance combination of the structure. That is, it needs the higher voltage to obtain the high value of current in the high temperature region. It is well known that the downward concave curvature of the forward bias *I–V* plots at sufficiently large voltages is caused by the presence of the effect of R_s, apart from the interface states, which are in equilibrium with the semiconductor. This kind of high series resistance behavior can be attributed to the interface states and interface layer. Both barrier height and series resistance have been strongly changed with sample temperature. At the same time, cause for the increase of the series resistance value can be attributed to the freeze-out of carriers at low temperatures. The series resistance decreases with increase in temperature. It is observed that the decrease in series resistance at low temperatures is more than at high temperatures since the slope of the curve is large at low temperatures (Fig. 10).

3.3. Capacitance–voltage (C–V) characteristics of the Cd/CdS/n-GaAs/In sandwich structure at room temperature

The *C–V* characteristics of the Cd/CdS/n-GaAs/In structure with measured at different frequencies are shown in Fig. 11. The capacitance decreases with the applied bias, which reveals that a depletion region exists at the CdS/n-GaAs junction, and the depletion region width increases with the reverse bias. For the forward biased capacitance, the peak capacitance values of the Cd/CdS/n-GaAs/In structure are 2450, 2210, 1865, 1013, 673 and 363 pF for the 10, 50, 100, 300, 500 and 1000 kHz, respectively. The peak values of the forward biased capacitance are increased as the operating frequency is decreased. The dependence of the capacitance of such a junction upon frequency can also arise due to the presence of deep lying impurities in the depletion region. Presence of deep traps in the depletion region of the junction makes the junction capacitance a complicated function of the bias voltage and the measuring frequency. The capacitance is nearly constant at the reverse bias region. In the ideal case, the *C–V* characteristics of metal–semiconductor or metal–insulator–semiconductor structures show an increase in capacitance with the increasing forward bias voltage. However, in recent years, some investigations have reported an anomalous peak in the forward bias *C–V* characteristics. Origin of the peak in the forward bias *C–V* characteristics might be attributed to the interface states, series resistance R_s and minority-carrier injection. The imperfect back-side ohmic contact of the In/GaAs causes a larger series resistance and shows an anomalous peak in the *C–V* characteristic. So the series resistance plays an important role in the appearance of anomalous peak in the *C–V* curves. As we know, the interface states will respond to the a.c signal at low frequencies but cannot follow the a.c signal at high frequencies. So capacitance measurement of high and low frequencies can determine the interface states density.

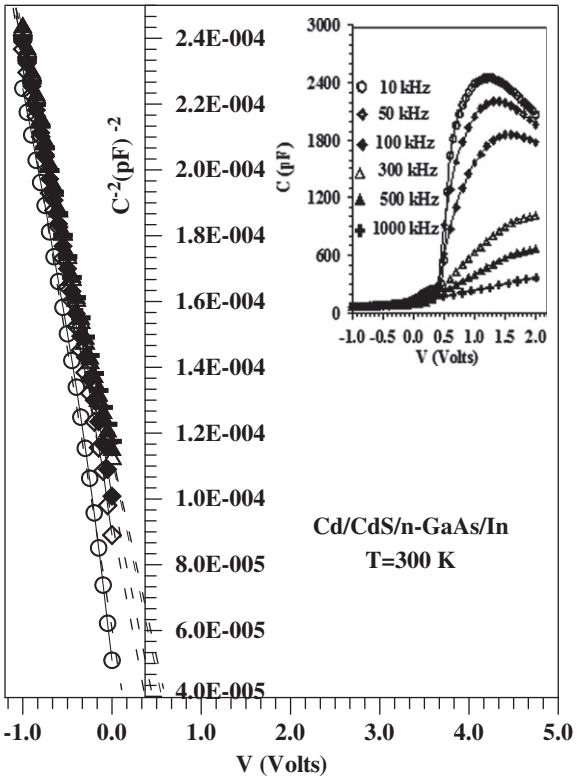

Fig. 11. The *C–V* and C^{-2}–*V* characteristics of the Cd/CdS/n-GaAs/In sandwich structure at different frequencies and room temperature.

The plots of C^{-2} versus reverse bias voltage are linear which indicates the formation of junction [34]. Therefore, it follows a standard Mott–Schottky relationship: $1/C^2=\left(2(V_{bi}-V-kT/q)/q\varepsilon_o\varepsilon_s A^2 N_d\right)$ where *C* is the diode capacitance, V_{bi} is the built in voltage, ε_s is the semiconductor dielectric constant, ε_o is the permitivity in vacuum, *V* is the applied voltage, *q* is the electronic charge, *A* is the diode active area, *kT/q* is the thermal voltage at 300 K and N_d is the free charge carrier concentration. The value of the barrier height can be calculated by $\Phi_b=V_{bi}+V_n$ equation using *C–V* data, where V_n is the potential difference between the Fermi energy level (E_f) and the bottom of the conduction band in the neutral region of n-GaAs, which is directly equal to E_f and can be calculated by knowing N_d and N_c, density of states in the conduction band ($V_n=kTln(N_c/N_d)$). From the extrapolated intercept on voltage axis V_{bi} can be estimated. Fig. 11 shows the $1/C^2$–*V* plot of the Cd/CdS/n-GaAs/In structure that was measured at the frequency range of 10–1000 kHz. For 10, 50, 100, 300, 500 and 1000 kHz frequencies, the built in voltages are calculated as 0.355 eV, 0.644 eV, 0.746 eV, 0.836 eV, 0.863 eV and 0.918 eV respectively, the values of V_n are calculated as 0.158 eV, 0.154 eV, 0.152 eV, 0.151 eV, 0.151 eV and 0.150 eV respectively and the effective barrier heights are calculated as 0.513 eV, 0.799 eV, 0.898 eV, 0.990 eV, 1.014 eV and 1.068 eV respectively. It can also be seen that the barrier heights, obtained from *I–V* measurements are different than those obtained from *C–V* measurements. According to Werner and Guttler [30], spatial inhomogeneities at interface of abrupt junction can also cause such differences in the barrier height determined from *I–V* and *C–V* measurements. According to the equation $1/C^2=\left(2(V_{bi}-V-kT/q)/q\varepsilon_o\varepsilon_s A^2 N_d\right)$, the substrate doping concentration N_d is related to the reciprocal of the slope of the $1/C^2$ versus *V* curve. For 10, 50, 100, 300, 500 and 1000 kHz frequencies, the doping concentration of substrate are calculated as $1.083\times10^{14}\,cm^{-3}$, $1.274\times10^{14}\,cm^{-3}$, $1.350\times10^{14}\,cm^{-3}$, $1.405\times10^{14}\,cm^{-3}$, $1.422\times10^{14}\,cm^{-3}$ and $1.491\times10^{14}\,cm^{-3}$ respectively. The doping profile of the device is derived from the *C-V* curve based on the definition of the differential capacitance as the differential change in depletion region charges produced by a differential change in the gate voltage.

4. Conclusion

CdS thin film has been directly growth on n-GaAs substrate by using SILAR method. For structural properties XRD and SEM measurements have been performed. The XRD and SEM studies

reveal that the films are covered well with n-GaAs substrate and exhibit polycrystalline characterization. From optical absorbance measurements the energy band gap value is found as 2.3 eV for CdS thin film. Temperature effect on the electrical characteristics of the Cd/CdS/n-GaAs/In structure has been investigated in the temperature range of 80–320 K by the steps of 20 K. It can clearly be seen that Cd/CdS/n-GaAs/In structure has good rectifying properties at different temperatures and they are manifestly temperature dependent. The obtained *I–V* barrier heights are in the range of 0.234–0.738 eV and that of ideality factor are 4.776–1.263. The increasing in ideality factor and decreasing in barrier height with decreasing temperature have been successfully explained based on the thermionic emission with the assumption of Gaussian distribution of the barrier heights at the interface. The extracted value of mean barrier height and standard deviation clearly indicates the presence of interface inhomogeneities and potential fluctuation at the interface. As a result, it can be said that this Cd/CdS/n-GaAs/In structure shows good diode behavior. According to these results, in the future, it can be used in rectifying contacts, integrated circuits, the other electronic devices and so on.

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