2D Materials

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Tunable Schottky barrier and high responsivity in graphene/Si-nanotip optoelectronic device

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Abstract

We demonstrate tunable Schottky barrier height and record photo-responsivity in a new-concept device made of a single-layer CVD graphene transferred onto a matrix of nanotips patterned on n-type Si wafer. The original layout, where nano-sized graphene/Si heterojunctions alternate to graphene areas exposed to the electric field of the Si substrate, which acts both as diode cathode and transistor gate, results in a two-terminal barristor with single-bias control of the Schottky barrier. The nanotip patterning favors light absorption, and the enhancement of the electric field at the tip apex improves photo-charge separation and enables internal gain by impact ionization. These features render the device a photodetector with responsivity (3 A W^{-1} for white LED light at 3 mW cm^{-2} intensity) almost an order of magnitude higher than commercial photodiodes. We extensively characterize the voltage and the temperature dependence of the device parameters, and prove that the multi-junction approach does not add extra-inhomogeneity to the Schottky barrier height distribution. We also introduce a new phenomenological graphene/semiconductor diode equation, which well describes the experimental I–V characteristics both in forward and reverse bias.

1. Introduction

Graphene/silicon (Gr/Si) heterojunctions are key elements of many graphene-based devices such as photo-detectors [1–3], solar cells [4–6], chemical-biological sensors [7–9], and high frequency transistors [10–14]. Such heterostructures are gaining interest from the semiconductor industry also for the potentiality to replace ultra-shallow doped junctions in modern complementary-metal-oxide-semiconductor technologies.

Despite recent progress in the deposition of Si layers on graphene [15], highest quality Gr/Si junctions are still formed by transferring large area graphene onto clean high-quality surfaces of Si single crystals [16]. Direct formation of graphene onto Si would be of higher technological relevance in the view of future applications, but this remains very challenging due to the formation of Si carbides.

Here, we apply the graphene transfer technique to implement a new concept of Gr/Si photodiode with graphene on nano-patterned Si surfaces. Through an extensive characterization, we demonstrate that devices with graphene on Si nano-tip arrays are more performant than their large area, planar counterparts.

The zero-bandgap and linear energy-momentum relationship of graphene, which result in finite density of states (DOS), have been shown to enable energy Fermi level tuning and hence Schottky barrier height control by a single anode–cathode bias [17]. Adding an electrostatic gate can further improve the barrier control in a three-terminal barristor (variable barrier device) [11]. In our approach, the coexistence on the same graphene layer of junction areas with much bigger graphene regions exposed to the field of the substrate, which acts as well-coupled back-gate especially near the tips, enables improved control of the Schottky
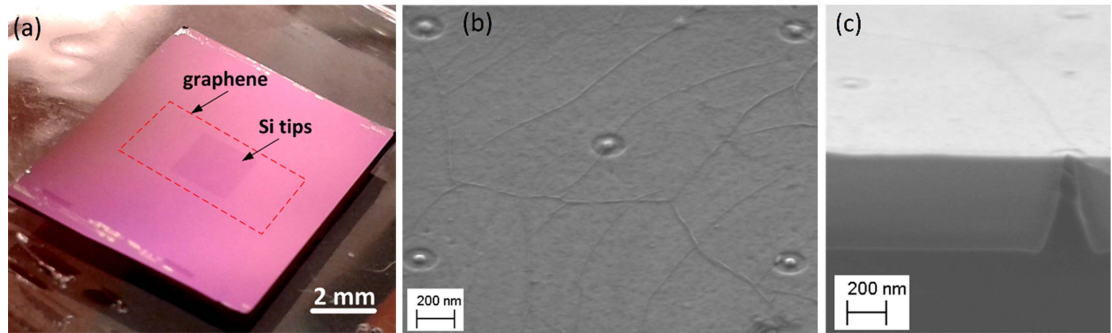
Figure 1. (a) Photograph of a single chip with a 2.5 × 2.5 mm² Si-tip array covered by a monolayer graphene transferred from Cu. (b) SEM top view of the tips emerging from the SiO₂ insulating layer and covered by graphene. The diameter of the emerging tips is ∼50 nm. Graphene wrinkles characteristic of graphene transferred from Cu are visible. (c) SEM cross-section image showing one of the Si-tips embedded in SiO₂ and covered by graphene. The tip pich size is 1.41 μm and the tip height is ∼0.5 μm.
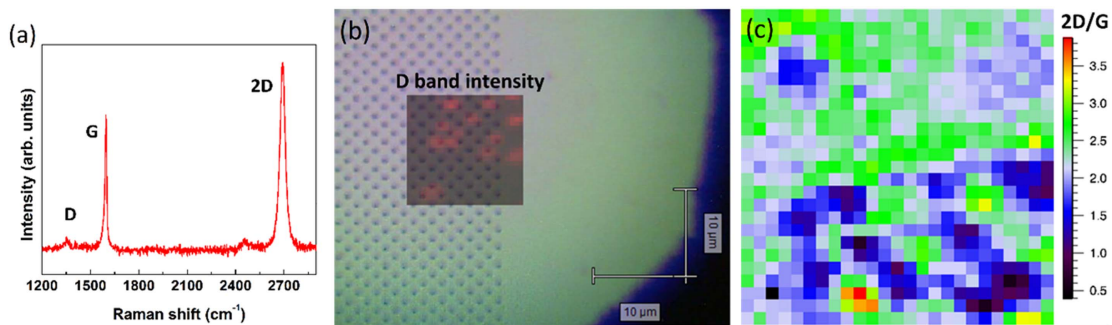
Figure 2. (a) Representative μRaman spectrum taken after graphene transfer. (b) D band intensity distribution extracted from Raman mapping measurement on an area of 12×12 μm² overlaid on optical image. (c) 2D/G intensity map taken from the same 12×12 μm² area indicated in (b).

barrier height by a single applied bias. This peculiarity makes the device an effective two-terminal barristor with linear control of the barrier height. More importantly, while preserving the barrier uniformity, the nano-textured surface enhances light collection due to multiple reflections and the tip-enhanced field favors photo-charge separation with internal gain due to impact ionization. These features result in record responsivity, which is one to two orders of magnitude higher than in planar Gr/Si junctions [1] and about one order of magnitude better than in commercial semiconductor photodetectors.
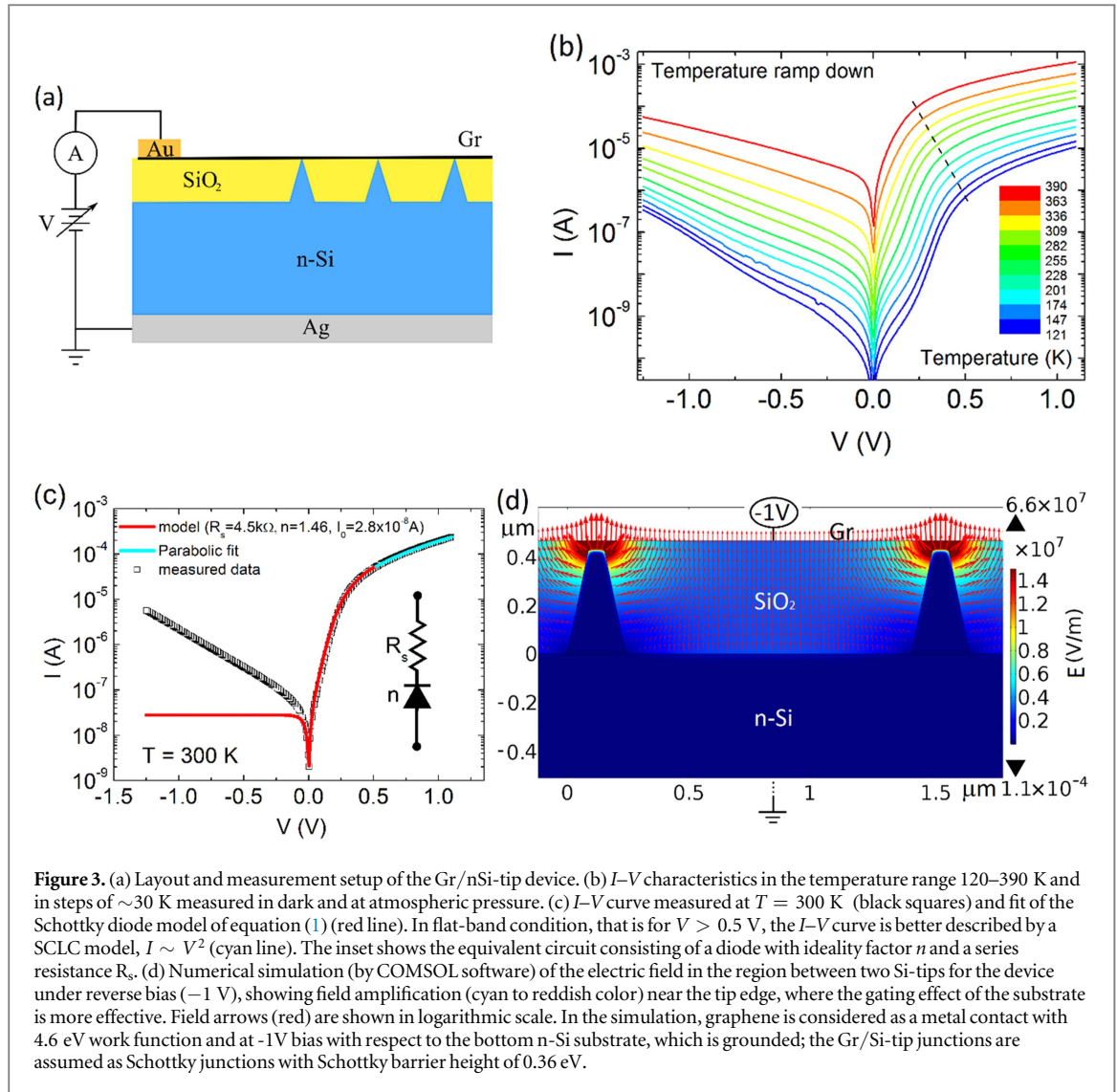
This work represents a significant advance in the realization and characterization of graphene/Si Schottky devices for optoelectronic applications.

2. Experimental details

Si-tip arrays (figure 1(a)) were prepared on degenerately doped (∼10¹⁸ cm⁻³) n-type Si wafers. Fabrication of the Si-tip array includes a SiO₂ or Si₃N₄ hardmask with photo-resist patterned by lithography, reactive ion etching of Si, plasma-enhanced chemical vapor deposition of a thick SiO₂ layer completely covering the formed Si-tips, and a chemical-mechanical planarization step to reduce the SiO₂ thickness till

revealing circular Si-tips surface of given diameter. Further details on the fabrication process can be found elsewhere [18]. Just before the graphene transfer, the Si-tip substrates were dipped in a 0.5% hydrofluoric acid solution for 10 s to remove only the native SiO₂ on Si-tips [19, 20] and enable formation of clean Gr/Si junctions. Graphene was transferred from commercially available Cu foils using a wet transfer process [21]. Immersion in deionized water and subsequent dry process by nitrogen-gas blowing helped in H-passivating the surface dangling bonds. Figure 1(b) shows a scanning electron microscopy (SEM) image taken after graphene transfer: Five Si-tips with a diameter of about 50 nm are seen underneath the graphene layer and wrinkles, characteristic of CVD graphene grown on Cu, can be clearly identified. Figure 1(c) shows a SEM cross-section of one of the Si-tips with graphene.

To evaluate the quality of graphene, Raman spectroscopy measurements with a 514 nm laser source (spot size ∼600 nm) were performed. Figure 2(a) shows a representative spectrum taken from the area between the Si-tips. Beside the characteristic 2D and G bands, a typical feature of monolayer graphene, a very small D peak related to defects is seen at about 1350 cm⁻¹. As shown by peak intensity

Figure 3. (a) Layout and measurement setup of the Gr/nSi-tip device. (b) *I–V* characteristics in the temperature range 120–390 K and in steps of ~30 K measured in dark and at atmospheric pressure. (c) *I–V* curve measured at $T = 300$ K (black squares) and fit of the Schottky diode model of equation (1) (red line). In flat-band condition, that is for $V > 0.5$ V, the *I–V* curve is better described by a SCLC model, $I \sim V^2$ (cyan line). The inset shows the equivalent circuit consisting of a diode with ideality factor n and a series resistance R_s. (d) Numerical simulation (by COMSOL software) of the electric field in the region between two Si-tips for the device under reverse bias (−1 V), showing field amplification (cyan to reddish color) near the tip edge, where the gating effect of the substrate is more effective. Field arrows (red) are shown in logarithmic scale. In the simulation, graphene is considered as a metal contact with 4.6 eV work function and at -1V bias with respect to the bottom n-Si substrate, which is grounded; the Gr/Si-tip junctions are assumed as Schottky junctions with Schottky barrier height of 0.36 eV.

mapping measurements presented in figure 2(b), the intensity of the D peak does not correlate with the positions of the Si-tips. The observed local increase in the D band intensity is most probably related to the presence of multilayer graphene islands [22]. Similarly, no particular correlation between the 2D/G peak intensity ratio and the positions of the Si-tips was revealed (figure 2(c)). Another small peak appears at 2450 cm^{-1}, generally indicated as D + D″, and interpreted as a combination of D and D″ phonons, the latter belonging to the in-plane longitudinal acoustic branch [23].

Sheet resistance of the graphene layer measured using 4-point technique beyond the Si-tip array was ~0.9 $k\Omega/\square$, a value in the range typically reported for CVD graphene on Cu [24].

The setup used for electrical measurements of the Gr/Si heterojunction is illustrated in figure 3(a). The top graphene layer was contacted with evaporated Au, while ohmic contact with the scratched bottom Si substrate was made with Ag paste. Electrical measurements were performed in a Janis probe station with pressure and temperature control. The top-injection configuration was adopted, with the biasing lead on graphene and the Ag electrode grounded. The measurements were carried out at atmospheric pressure.

3. Results and discussion

The dark *I–V* characteristics of the Gr/Si-tip heterojunctions in the temperature range 120–390 K are shown in figure 3(b). The device exhibits a rectifying behavior with the forward current at positive bias, as expected for p-type graphene on n-Si. The p-type doping is usually observed in air-exposed graphene [10, 25]. The current for a given voltage increases with rising temperature, which is typical of thermionic emission in this kind of devices. At modest positive bias, the room and higher temperature forward *I–V* curves show an almost ideal diode behavior. At lower temperatures, namely $T < 250$ K, a new feature appears in the lower bias part of the forward *I–V* curves, where the current is dominated by a leakage component that adds non-linearity to the semi-log *I–V* plot. This leakage component is usually attributed to

generation and recombination of carriers in the charge space region, field emission and thermionic field emission or surface/edge effects that may lead to local barrier lowering [26, 27]. Such component becomes relevant when the low-temperature suppresses the thermionic emission, e.g. at $T = 121$ K, where it manifests on the interval $0 < V < 0.25$ V.

To gain insight into carrier transport across the Gr/Si-tip device, we focus on the $I–V$ curve at $T = 300$ K. Figure 3(c) shows the measured data together with the best fitting curve as predicted by the Schottky model [16, 28, 29], which is described by the following $I–V$ relation:

$$I = I_0 [e^{q(V-R_sI)/nkT} - 1] \tag{1}$$

with

$$I_0 = AA^*T^2 e^{-\Phi_B/kT}, \tag{2}$$

where I_0 is the reverse saturation current, A the contact area, $A^* = 4\pi qm^*k^2/h^3$ the effective Richardson constant with m^* the electron effective mass, T the absolute temperature, Φ_B the Schottky barrier height, k the Boltzmann constant, q the electronic charge, n the ideality factor that takes into account deviations from the pure thermionic regime and effects of inadvertent interface layers, and R_s the series resistance. n takes into account that only the fraction $(V-RI)/n$ of the junction bias $V-RI$ develops across the semiconductor depletion layer, while the remainder $(1-1/n)(V-RI)$ drops on the interface layer. R_s is the lump sum of bulk Si, graphene, metal leads and contact resistances, and is dominated by graphene. The equivalent circuit, consisting of the series of a diode with ideality factor n and a resistor R_s, is shown in the inset of figure 3(c). As seen in this figure, equation (1) provides a perfect fit in the range $0 < V < 0.5$ V; at higher bias, the Gr/Si-tip diode enters a high injection regime, where the voltage drop across the series resistance strongly limits the exponential increase of the current, until the barrier reaches the flat-band condition and the $I–V$ characteristic is dominated by the series resistance. In this region, henceforth referred as flat-band, the current is better described by a quadratic relation, $I \sim V^2$, typical of space charge limited conduction (SCLC). The gating effect of the substrate increases the p-doping of graphene when $V > 0$ V and this is the origin of the quadratic dependence. Indeed, in flat-band condition, $V \approx R_sI$, and the graphene-dominated R_s is proportional to the inverse bias ($R_s \sim (qn_q)^{-1} \sim (CV)^{-1}$ where n_q is the graphene carrier density and C the gate capacitance per unit area), which makes the current to scale as V^2. The gating effect of the substrate is particularly effective around the tips, where the electric field is stronger, as shown in figure 3(d).

Figure 3(c) also evidences that, in reverse bias ($V < 0$ V), the current dramatically deviates from the constant behavior predicted by equation (1), implying that it is not the usual saturation current of a diode. Since $\ln I$ increases linearly with $|V|$, the common modeling by a simple shunt resistance seems not

appropriate in this case. A better explanation is provided by a bias dependence of the Schottky barrier, due to a combination of image force lowering and low DOS of graphene in the absence of Fermi level pinning, as we will discuss in the following.

Figure 4 shows the rectification factor r, the series resistance R_s and the ideality factor n over the explored temperature range. The rectification factor r is here defined as the ratio of the on/off current at $V = \pm V_{FB}$, $I(V_{FB})/I(-V_{FB})$, where V_{FB} is the voltage corresponding to the onset of the flat-band region (that is the region to the right of the dashed-black line in figure 3(b). Both r and V_{FB} decrease with increasing temperature. In particular, r, which is ~120 at room temperature, has a monotonic behavior with two possible regimes crossing at $T \sim 260$ K. Below this temperature, there is a reduced rate dr/dT, likely correlated with the deviation from the pure thermionic emission.

V_{FB} linearly decreases with temperature with a slope $|dV_{FB}/dT| \approx 1$ mV/K, a behavior similar to the forward voltage drop of a typical pn-diode. As the temperature increases, the flat-band condition, $V \approx R_sI(V)$, is reached at lower bias due to the strong $I(T)$ dependence, as described by equation (2). Indeed, the linear behavior of V_{FB} implies a strongly decreasing $R_s(T)$ to counterbalance the exponential growth of $I(T)$ with temperature.

We used $I–V$ data below and around V_{FB}, and followed the Cheung method [30, 31] to extract R_s and n at a given temperature from the slope and the intercept of the corresponding $dV/d(\ln I)$ versus I plot, since
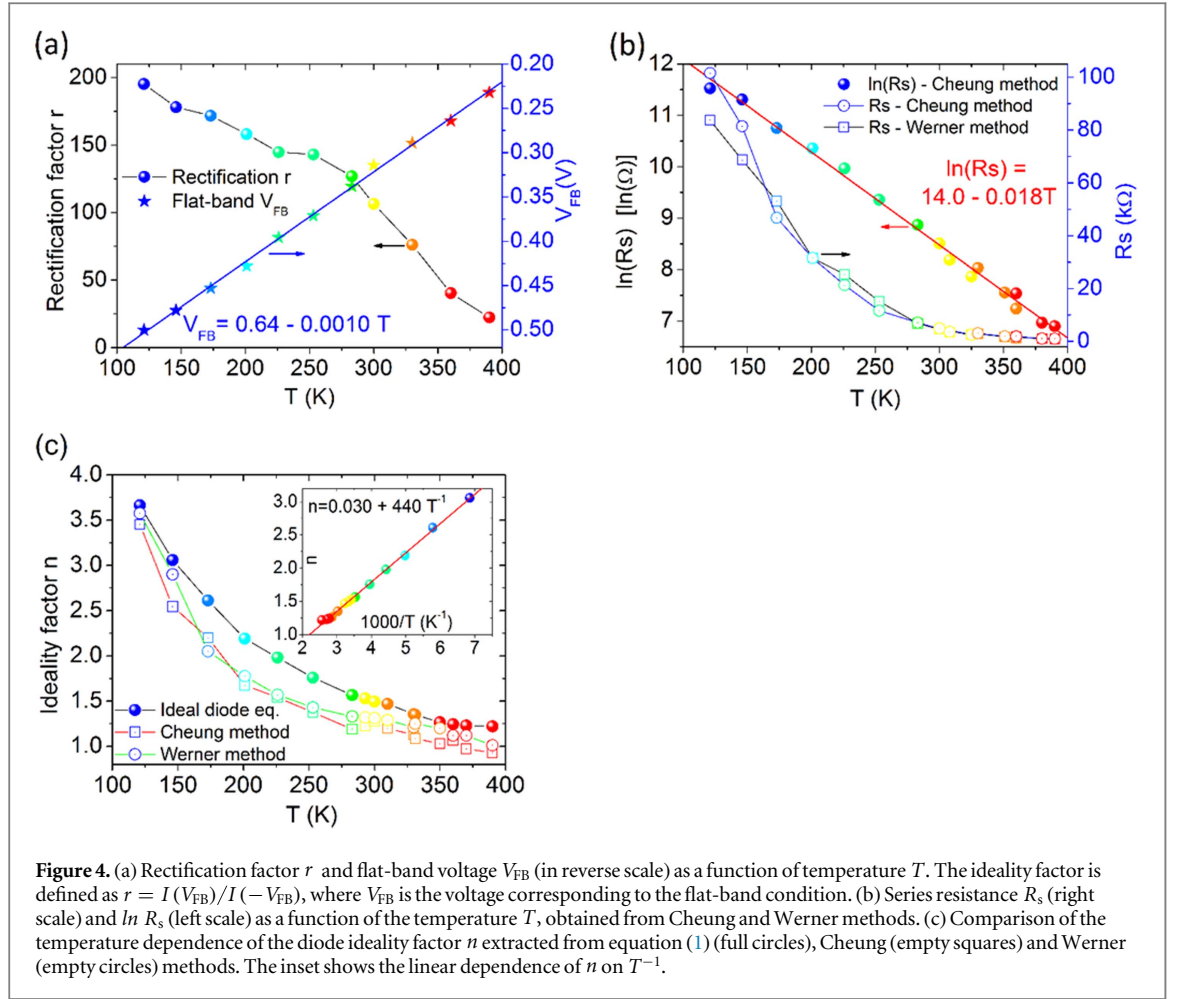
$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + R_sI. \tag{3}$$

R_s and n were also obtained from $(dI/dV)/I$ versus dI/dV plots (Werner method [32]), considering that

$$\frac{dI/dV}{I} = \frac{q}{nkT}\left[1 - R_s\left(\frac{dI}{dV}\right).\right] \tag{4}$$

Both equations (3) and (4) are valid in the limit of $V \geqslant 3nkT/q$. The consistent results are shown in figures 4(b) and (c). Remarkably, R_s exhibits the expected exponential decrease with T ($R_s \sim \exp(-\alpha T)$), that is a semiconductor behavior with negative temperature coefficient of resistance, dR_s/dT. Neither Si [33, 34] nor metals or ohmic contacts [35] can account for the negative dR_s/dT in the temperature range under investigation. The semiconductor behavior can only originate from graphene. Indeed, the resistivity of graphene, especially at the lower carrier density close to the Dirac point and in the presence of defects or impurities, has been reported to decrease with rising temperature on exfoliated or CVD monolayer graphene, both suspended [36] or deposited on substrate [37–39]. A semiconductor behavior has been reported also for bilayer and few layer graphene on substrate over a wide temperature range [40–42]. The negative temperature coefficient in

Figure 4. (a) Rectification factor r and flat-band voltage V_{FB} (in reverse scale) as a function of temperature T. The ideality factor is defined as $r = I(V_{FB})/I(-V_{FB})$, where V_{FB} is the voltage corresponding to the flat-band condition. (b) Series resistance R_s (right scale) and $ln\,R_s$ (left scale) as a function of the temperature T, obtained from Cheung and Werner methods. (c) Comparison of the temperature dependence of the diode ideality factor n extracted from equation (1) (full circles), Cheung (empty squares) and Werner (empty circles) methods. The inset shows the linear dependence of n on T^{-1}.

graphene is the result of competing mechanisms, with the thermally activated transport through inhomogeneous electron-hole puddles as the main recognized cause [39]. CVD graphene is more vulnerable to impurities or charged defects during the transfer process, and is particularly prone to develop electron-holes puddles that tend to produce a negative dR_s/dT.

The ideality factor was further estimated from the slope of straight-line fitting the thermionic part of the $ln(I)$ versus V plot (i.e. the part between 0 and $\sim V_{FB}$, after excluding the leaky portion at lower biases), which according to equation (1) and for $V \gg R_s I$ is described by
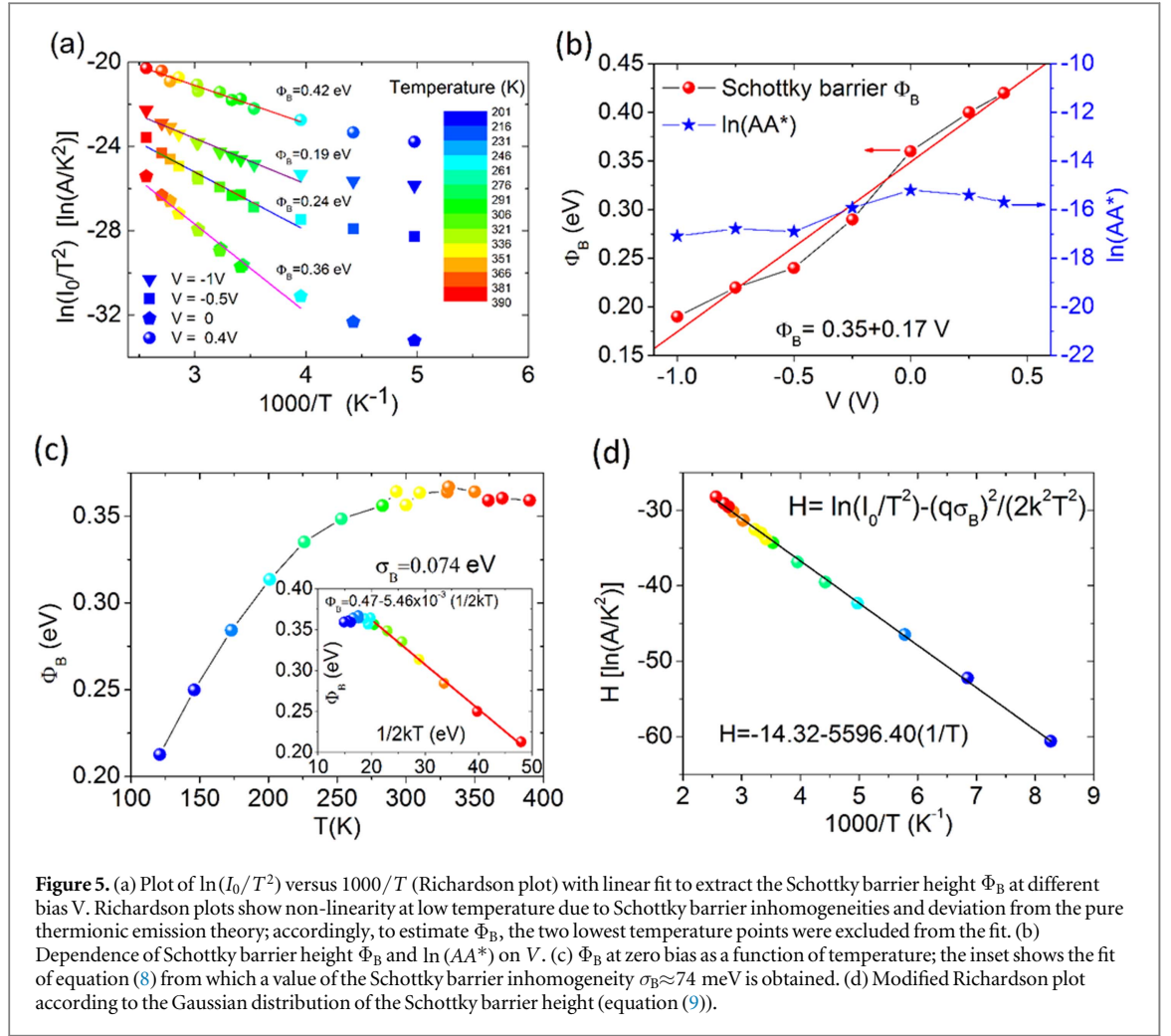
$$ln\,I = ln\,I_0 + \frac{q}{nkT}V. \qquad (5)$$

While the temperature dependence of n is the same (figure 4(c)), equation (5) provides values which are 10% to 20% higher than those obtained with Cheung and Werner methods. The slope of a fitting straight line is usually more accurate than the intercept for the estimation of diode parameters, so the method based on equation (5) is considered more reliable. n decreases with increasing temperature ($n = c + T_0/T$ with c and T_0 constants, as shown in the inset of figure 4(c)) and approaches the ideal value of 1 at the highest temperatures. This behavior confirms that the thermionic emission is the dominant

carrier conduction process at high temperatures. On the contrary, at lower temperatures, the growing n indicates that other transport phenomena, as generation-recombination in the space charge region, interface layer and neutral region or thermionic field emission, add to thermionic emission. Furthermore, the observed temperature dependence of the ideality factor is a signature of Schottky barrier spatial inhomogeneity and of deformation of the barrier when a bias voltage is applied [43].

According to equation (2), a plot of $ln(I_0/T^2)$ versus $1/T$ (Richardson plot) is a straight line, whose slope and intercept are used to evaluate the Schottky barrier height Φ_B and $ln(AA^*)$ at a given bias:

$$ln\left(\frac{I_0}{T^2}\right) = ln(AA^*) - \frac{\phi_B}{k}\frac{1}{T}. \qquad (6)$$

In reverse bias, when $e^{q(V-R_sI)/nkT} \ll 1$, $I_0(T)$ is directly measured on the curves of figure 3(b). At zero bias, I_0 is extrapolated to $V = 0\,V$ as the intercept of the straight line fitting the thermionic part of the forward I–V characteristics. In forward bias, when $e^{qV/nkT} \gg 1$ and $V \gg R_s I$, equations (1) and (2) combine to yield a slightly modified Richardson equation, that requires n to estimate the Schottky barrier height:

Figure 5. (a) Plot of $\ln(I_0/T^2)$ versus $1000/T$ (Richardson plot) with linear fit to extract the Schottky barrier height Φ_B at different bias V. Richardson plots show non-linearity at low temperature due to Schottky barrier inhomogeneities and deviation from the pure thermionic emission theory; accordingly, to estimate Φ_B, the two lowest temperature points were excluded from the fit. (b) Dependence of Schottky barrier height Φ_B and $\ln(AA^*)$ on V. (c) Φ_B at zero bias as a function of temperature; the inset shows the fit of equation (8) from which a value of the Schottky barrier inhomogeneity $\sigma_B \approx 74$ meV is obtained. (d) Modified Richardson plot according to the Gaussian distribution of the Schottky barrier height (equation (9)).

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*) - \frac{\phi_B - qV/n}{k}\frac{1}{T}. \qquad (7)$$

Examples of Richardson plots for a subset of applied biases are shown in figure 5(a), while a more complete set of measured $\Phi_B(V)$ is summarized in figure 5(b). Remarkably, $\Phi_B(V)$ exhibits a linear increase with V, and has the value $\Phi_B \approx 0.36$ eV at zero bias. Figure 5(b) depicts $\ln(AA^*)$ with a very weak dependence on V. Considering the average value $\ln(AA^*) \approx -16$ and an effective junction area of 6.079×10^{-5} cm^2 (estimated from the number of tips and conservatively assuming a circular junction area with mean radius of 25 nm and no micro-areas with missing graphene), the Richardson constant results $A^* = 0.002$ A/(K^2 cm^2), a value significantly lower than the theoretical 112 A/(K^2 cm^2) for electrons in Si. Similar low values, ranging from 10^{-3} to 10^{-1} A/(K^2 cm^2) have been reported for Gr/Si planar heterojunction [44–46] and revised Schottky diode equations, based on Landauer formalism [45] or including the massless Dirac fermion nature of carriers in graphene [47, 48], have been proposed to explain this anomaly.

The low value of A^*, the temperature dependence of n, the linear bias dependence of Φ_B as well as the deviation from linearity of the Richardson plot at low

temperatures, can be ascribed to spatial inhomogeneities in the Schottky barrier height [43], as already mentioned. Since the Gr/Si-tip device under study is made of more than 3×10^6 nanojunctions, minimal tip-to-tip variation could result in significant barrier height fluctuations. Hills and valleys in the barrier-height distribution can be caused e.g. by local effective barrier lowering due to field emission from tips with narrower radius of curvature, by inadvertent interfacial layers, by electron-hole puddles in graphene, or by surface defects or contaminates, possibly introduced during the fabrication process. An applied bias deforms the lower and higher barrier patches, causing $\Phi_B(V)$ dependence [43]. Indeed, a major disadvantage of the tip approach could be the limited shape control. Rather than a simple Si(001) plateau facet region, a tip could be a multi-facetted round shape Si structure. Different Si facets might have different work function values and further contribute to Schottky barrier inhomogeneities. Hence, to check the Schottky barrier spatial distribution, we calculated $\Phi_B(T)$ using equation (2) with the extrapolated values of $I_0(T)$ at zero bias, and studied its temperature dependence (figure 5(c)).

The decreasing barrier height with lowering temperature is easily understood considering that the

current becomes gradually dominated by electrons able to surmount the lower barrier patches, and this gives a reduced apparent barrier height. Assuming a Gaussian spatial distribution for Φ_B, with mean Φ_{Bm} and the standard deviation σ_B, the temperature dependence of the measured (apparent) barrier height Φ_B at zero applied bias is expected to follow the relation [43]:

$$\Phi_B = \Phi_{Bm} - \frac{q\sigma_B^2}{2kT}. \qquad (8)$$

The standard deviation σ_B is a measure of the inhomogeneity of the Schottky barrier height (the lower σ_B the more uniform is Φ_B), and, according to equation (8), can be extracted from the plot of Φ_B versus $\frac{1}{2kT}$, as shown in the inset of figure 5(c). As already mentioned, the Schottky barrier distribution can be deformed by the applied bias. In particular, Werner *et al* [43] have demonstrated that a linear $\Phi_B(V)$ implies a voltage independent ideality factor and that a linear n versus $1/T$ results from the narrowing of the Gaussian barrier distribution (i.e. of σ_B) with forward bias, meaning that the application of a forward bias homogenizes the barrier fluctuations. The value of $\sigma_B \sim 74$ meV at zero bias is in agreement or below what has been reported for planar Gr/semiconductor heterojunctions [44, 46, 49]. This leads to the remarkable result that the tip-geometry and the transfer process do not introduce extra-inhomogeneity. However, we point out that the measured σ_B, despite its low value, is still enough to affect the low temperature part of the *I–V* characteristics and the Richardson plots.

As consistency check, we notice that $\Phi_{Bm} = 0.47$ eV extracted from equation (8) is within 1.5 σ_B from the apparent Φ_B at high temperature estimated using equation (2). Together, equations (2) and (8), give

$$H \equiv \ln\left(\frac{I_0}{T^2}\right) - \frac{q^2\sigma_B^2}{2k^2T^2} = \ln(AA^*) - \frac{q\Phi_{Bm}}{kT}, \qquad (9)$$

which suggests a modified Richardson plot of H versus $1000/T$ from which a more accurate and higher value of $A^* = 0.015$ A/(K^2 cm^2) can be estimated, while $\Phi_{Bm} = 0.48$ eV remains practically unaffected. We remark here that A^* is possibly underestimated, given our conservative assumption of constant full-contact area between Gr and Si-tips; we also underline that Φ_{Bm} is consistent with other reported evaluations [11, 50, 51] and, as we discuss in the following, matches the prediction of Schottky–Mott theory.

The Schottky barrier height depends on the graphene work function, the Si electron affinity as well as on the interface states density and on the thickness of an inadvertent interfacial layer of atomic dimension, often due to native oxide, that is transparent to electrons but able to withstand a potential drop [16, 29, 52]:

$$\Phi_B = \Phi_{Gr} - X_{Si} - q\Delta, \qquad (10)$$

where $\Phi_{Gr} = 4.5 \div 4.6$ eV is the work function of graphene [53, 54], $X_{Si} = 4.05$ eV is the electron

affinity of Si and Δ is the potential drop across the interfacial layer. High density of interface states at a given energy in the Si bandgap usually leads to pinning of the Fermi level and can result in a significant discrepancy from equation (10). However, due to negligible interaction with chemically inert graphene, the formation of interface states is suppressed in graphene-semiconductor junctions if the Si-surface is defects-free and with saturated dangling bonds [55]. An ideal, trap free interface would result in unpinned Fermi level and yield a Schottky barrier height

$$\Phi_B = \Phi_{Gr} - X_{Si}, \qquad (11)$$

(Schottky–Mott relation) in the range $0.45 - 0.55$ eV for undoped graphene. The Fermi level unpinning enables easy modulation of the Schottky barrier, a feature that can be exploited to tune Gr/Si devices to match specific performance requests [11, 56]. Deviations from the Schottky–Mott prediction are mainly due to image force lowering [57] or hot electrons barrier lowering [58, 59]. Neglecting the field enhancement by the tip (values of the field up to 10^7 V cm^{-1} can be achieved, as shown in figure 3(d)), the maximum built-in electric field at the Gr/Si junction [29] is

$$E_m = \sqrt{(2qN|\phi_i|)/\varepsilon_{Si}} \approx 3 \times 10^5 \text{ V cm}^{-1}. \qquad (12)$$

($N = 10^{18}$ cm^{-3} is the Si doping density, $\phi_i \approx 0.3$ V is the built-in potential and $\varepsilon_{Si} = 12\varepsilon_0$ is the dielectric constant of Si) which corresponds to a Schottky barrier lowering by image force:
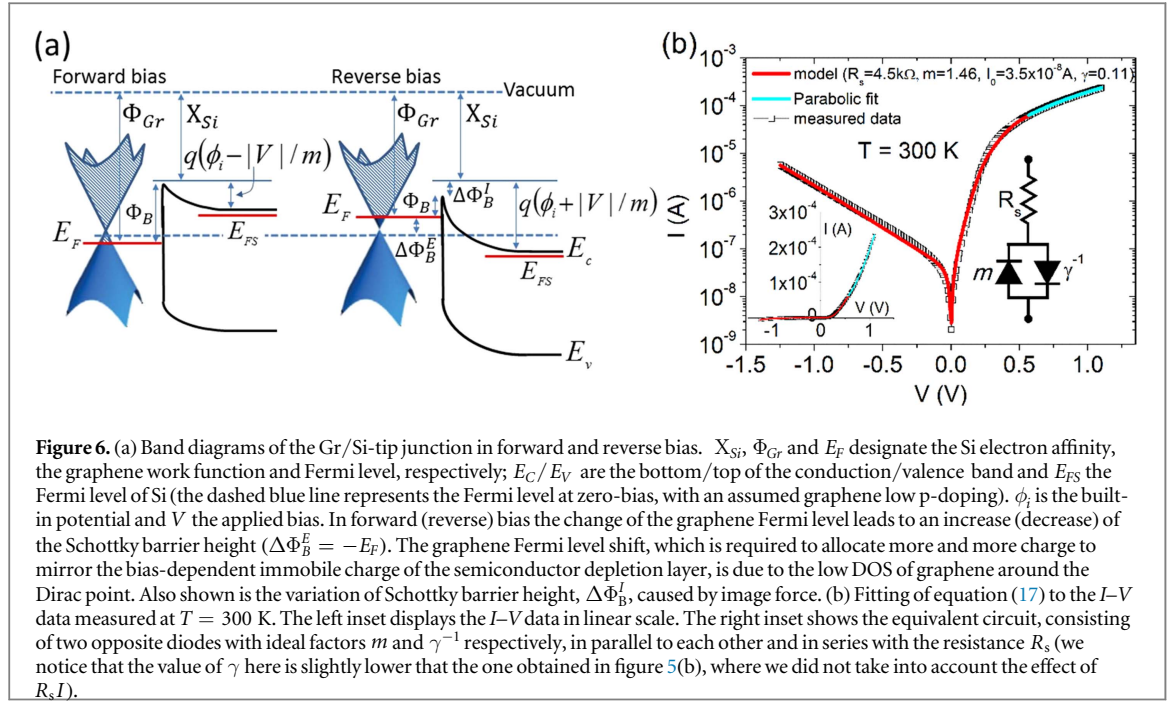
$$\Delta\Phi_B^I = q\sqrt{qE_m/(4\pi\varepsilon_{Si})}$$
$$= q\sqrt[4]{q^3N|\phi_i|/(8\pi^2\varepsilon_{Si}^3)} \approx 0.06 \text{ eV} \qquad (13)$$

When a bias is applied to the junction, $|\phi_i|$ is replaced by $|\phi_i - V/m|$ in equations (12) and (13) (m is an ideality factor—see the following), and $\Delta\Phi_B^I$ is increased (decreased) by a reverse (forward) bias, as depicted in figure 6(a). At zero bias, adding $\Delta\Phi_B^I$ from equation (13) to the measured $\Phi_B \approx 0.36$ eV brings the Schottky barrier height close to the ideal Schottky-Mott value. This result confirms the good quality of the Gr/Si-tip interfaces in the device under study.

A good quality interface also excludes the chance of Fermi level pinning. In graphene, the Fermi energy, E_F, at room temperature, is approximately related to the free carrier density n_q by a quadratic relation

$$n_q \approx n_{q0} + E_F^2/(\pi\hbar^2 v_F^2) \qquad (14)$$

(n_{q0} is the intrinsic carrier density and $v_F \approx 10^6$ m s^{-1} is the Fermi velocity of graphene). Equation (14) enables fine tuning of E_F via n_q, which can be easily controlled by an electric field (electrostatic doping). In heterojunctions with unpinned Fermi level, E_F modifies the graphene work function and hence the Schottky barrier height. P-doping of graphene increases Φ_B and n-doping decreases it, as displayed in figure 6(a) for graphene on n-type Si. The electrostatic Schottky barrier variation, $\Delta\Phi_B^E = -E_F$, adds to the image force barrier lowering $\Delta\Phi_B^I$, to set Φ_B

Figure 6. (a) Band diagrams of the Gr/Si-tip junction in forward and reverse bias. X_{Si}, Φ_{Gr} and E_F designate the Si electron affinity, the graphene work function and Fermi level, respectively; E_C/E_V are the bottom/top of the conduction/valence band and E_{FS} the Fermi level of Si (the dashed blue line represents the Fermi level at zero-bias, with an assumed graphene low p-doping). ϕ_i is the built-in potential and V the applied bias. In forward (reverse) bias the change of the graphene Fermi level leads to an increase (decrease) of the Schottky barrier height ($\Delta\Phi_B^E = -E_F$). The graphene Fermi level shift, which is required to allocate more and more charge to mirror the bias-dependent immobile charge of the semiconductor depletion layer, is due to the low DOS of graphene around the Dirac point. Also shown is the variation of Schottky barrier height, $\Delta\Phi_B^I$, caused by image force. (b) Fitting of equation (17) to the I–V data measured at $T = 300$ K. The left inset displays the I–V data in linear scale. The right inset shows the equivalent circuit, consisting of two opposite diodes with ideal factors m and γ^{-1} respectively, in parallel to each other and in series with the resistance R_s (we notice that the value of γ here is slightly lower that the one obtained in figure 5(b), where we did not take into account the effect of $R_s I$).

(figure 6(a)). Noteworthy, in the device under study, E_F modulation by electrostatic doping is achieved via the electric field (figure 3(d)) generated by the same voltage used to bias the junction.

Both $\Delta\Phi_B^I$ and $\Delta\Phi_B^E$ introduce a sublinear dependence on the applied bias V in the Schottky barrier height (roughly as the $\sqrt[4]{|V|}$ from equation (13) and $\sqrt{|V|}$ from equation (14), respectively, since $|\Delta\Phi_B^E| = |E_F| \sim \sqrt{qn} \sim \sqrt{V}$), which can be written as

$$\Phi_B(V) = \Phi_{B0} + \Delta\Phi_B(V). \tag{15}$$

$\Delta\Phi_B(V)$ is positive in forward bias and negative in the reverse bias.

The effect of electrostatic doping, $\Delta\Phi_B^E$, was first included in the diode equations (1) and (2) by Tongay *et al* [17] who obtained a reverse saturation current I_0 depending on the exponential of $\sqrt{|V|}$. A similar behavior was proposed with different approaches also by Sinha *et al* [45] and Liang *et al* [47, 48]. However, for the Gr/Si-tip device under study, the measured barrier height of figure 5(b)) shows that $\Phi_B(V)$ is better described by a linear relation. Accordingly, we write $\Delta\Phi_B(V) = \gamma q(V - R_s I)$, with γ a dimensionless constant, and the reverse saturation current as

$$\bar{I}_0 = AA^* T^2 e^{-[\Phi_{B0} + \gamma q(V - R_s I)]/kT} = I_0 e^{-\gamma q(V - R_s I)/kT}. \tag{16}$$

By re-defining the ideality factor as $1/m \equiv 1/n - \gamma = 1/n - (1/q)\,\partial\Phi_B/\partial(V - R_s I)$, equation (1) and equation (16) can be combined to obtain:

$$I = I_0 e^{q(V - R_s I)/mkT}[1 - e^{-q(V - R_s I)(1/m + \gamma)/kT}]$$
$$= I_0[e^{q(V - R_s I)/mkT} - 1] - I_0[e^{-q(V - R_s I)\gamma/kT} - 1] \tag{17}$$

which includes an ideality factor for both the forward and reverse current. From a circuital viewpoint, equation (17) corresponds to the parallel of two opposite diodes, with ideal factors m and γ^{-1} respectively, in series with the resistance R_s, as shown in the inset of figure 6(b). In forward bias, the current originates mostly from electrons injected from Si into graphene, and is controlled by the Si band-bending barrier, $q(\phi_i - V\,m^{-1})$ (figure 6(a)). The ideality factor m (which the fit of figure 6(b) shows to be $\approx n$) is predominantly caused by inadvertent interface layers and other deviations from pure thermionic emission. In reverse bias, the Schottky barrier is significantly lowered by the applied voltage because of the limited DOS of graphene (figure 6(a)). This causes an exponential increase of the electrons flowing from graphene into Si, i.e. of the reverse current, which is modeled by a diode of ideality factor γ^{-1}, which obviously takes into account the strong bias dependence of the Schottky barrier height.

Figure 6(b) shows that equation (17) provides an excellent fit to the measured data at 300 K over the whole bias range (the flat-band regime obeys a quadratic law, as explained before). The dependence of I_0 as the exponential of a linear rather than a sub-liner function of $|V|$ is likely due to the effect of Si substrate which, especially in the vicinity of the tips (figure 3(d)), acts as strongly-coupled gate that would linearly shift E_F. Consequently, the Gr/Si-tip device behaves as a barristor, with linear control of the Schottky barrier height as for the device of Yang *et al* [11], but without the need of a third gate electrode.
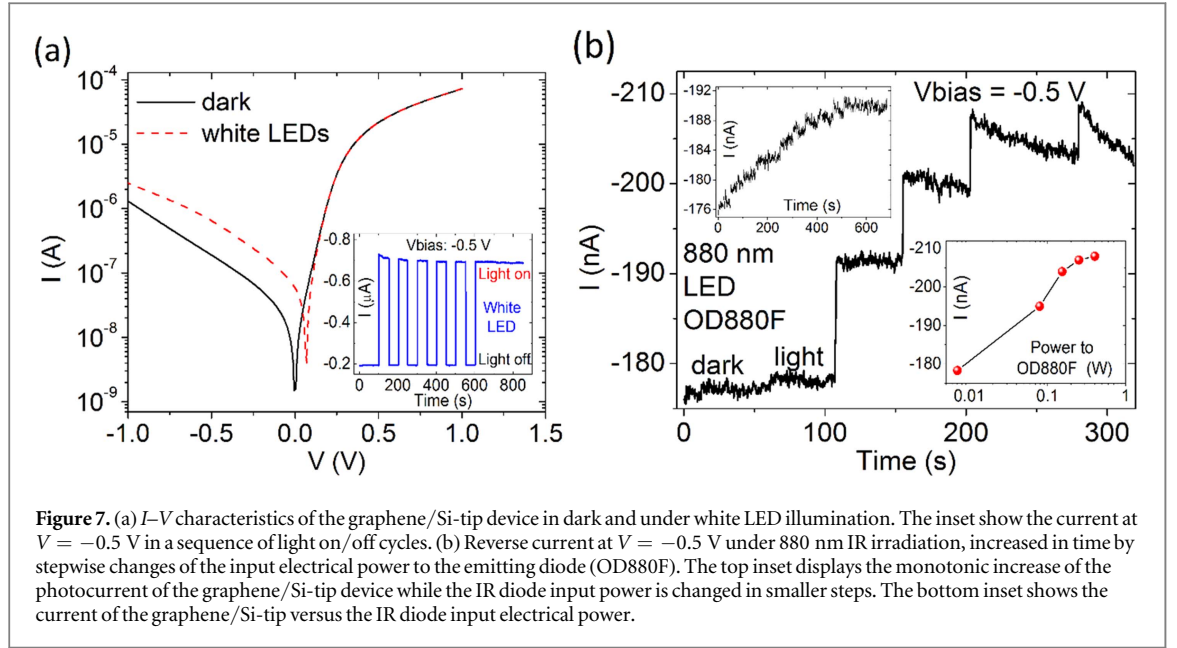
Figure 7. (a) *I–V* characteristics of the graphene/Si-tip device in dark and under white LED illumination. The inset show the current at $V = -0.5$ V in a sequence of light on/off cycles. (b) Reverse current at $V = -0.5$ V under 880 nm IR irradiation, increased in time by stepwise changes of the input electrical power to the emitting diode (OD880F). The top inset displays the monotonic increase of the photocurrent of the graphene/Si-tip device while the IR diode input power is changed in smaller steps. The bottom inset shows the current of the graphene/Si-tip versus the IR diode input electrical power.

Another important effect which can lead to a stronger V-dependence of the reverse current is the Schottky barrier lowering caused by hot electrons [58, 59] that might originate even a quadratic $\Delta\Phi_B(V)$. In this scenario, the gating effect induces abrupt band bending around the Schottky barrier that increases the lateral field, which in turn produces significant enhancement of hot carriers.

We also studied the photoresponse of the Gr/Si-tip device by shining light from the top, on the graphene layer. Figure 7(a) compares the *I–V* curves obtained in darkness and under 3 mW cm^{-2} white LED light; it shows clear photocurrent in reverse bias, and photovoltaic effect with 60 nA short circuit current (a factor ~50 higher than the dark current at zero bias) and 70 mV open circuit voltage. In reverse bias, the Gr/Si-tip device can be used as a photodetector: The electron-hole pairs generated by incident photons in the Si space-charge region and, in minor part, in the Si quasi-neutral region or in graphene are separated by the strong tip-enhanced electric field, leading to a photocurrent [20]. The inset of figure 7(a) shows the stable photoresponse when the light is switched on and off, at a bias of −0.5 V, corresponding to a responsivity $\mathcal{R}_{ph} = I_{ph}/P_0 = (I_{ligth} - I_{dark})/P_0 \approx 3$ A W^{-1} (here, I_{ph} is the photocurrent and P_0 the incident optical power). Figure 7(b) shows the photoresponse, at the same bias of −0.5 V, to the near IR radiation produced by a 880 nm LED. The Gr/Si-tip device is expected to show high sensitivity around this wavelength, since Si has an absorption peak [3] at ~930 nm. The current plateaus of figure 7(b) and of its top inset are the response of the Gr/Si-tip device to stepwise changes of electrical power fed into the irradiating diode: The photocurrent displays a monotonic growth with IR intensity (as seen also in the bottom insets of the figure). The radiation intensity in W cm^{-2} reaching the Gr/Si-tip junction was measured to be ⩽1% of the IR diode supply power. Hence, figure 7(b) shows that the minimum detectable IR intensity by the Gr/Si-tip heterojunction is less than 100 μW cm^{-2} and its responsivity is $\mathcal{R}_{ph} \geqslant 0.3$ A W^{-1} at intensity <1 mW cm^{-2}. The measured responsivity is one or two orders of magnitude higher than the values reported to date for graphene/Si planar-junctions [3, 60– 63] (with maximum of 225 mA W^{-1} at 488 nm) [1]. The graphene/Si-tip device appears also competitive when compared to semiconductor photodiodes on the market, whose typical responsivity is around 0.5 A W^{-1}, both for visible and near IR light.

The high substrate doping reduces the space-charge region where most of the photoexcitation takes place and this should suppress the responsivity. This loss can be counterbalanced by the textured surface, which on the contrary favors multiple reflections and light absorption [64]. However, the high value of responsivity is rather a result of the peculiar device geometry. The tip-enhanced electric field, other than facilitating their separation, can provide photogenerated electron-hole pairs with enough kinetic energy to cause impact ionization and initiate charge multiplication, thus enabling device internal gain. The exponential increase of the photocurrent with reverse bias can be taken as signature of internal gain since smoother rise is usually observed when the photocurrent is due only to increased photon absorption in the bias-widened depletion layer. Augmented photocharge separation and multiplication is also expected in graphene, especially in the areas near the tips. We notice that very high responsivity of 10^7 A W^{-1} have been reported by Liu *et al* [51] in more complex three-terminal Gr/Si devices with quantum gain due to photocarriers borrowed into graphene and reinvested several times in the external circuit during their lifetime. However, these devices require more complex circuitry than our multi-purpose two-terminal photodiode.

4. Conclusions

In conclusion, we have fabricated and extensively characterized a novel Gr/Si heterojunction obtained by CVD graphene transfer over a nanotip patterned Si-substrate. We have measured the relevant junction parameters and shown better performance of the Gr/Si-tip device with respect to its planar counterpart. Without adding barrier inhomogeneity, the tip geometry enables linear tuning of the Schottky barrier height, hence of the diode current, by a single applied bias, thus implementing a two terminal barristor. The textured surface improves light absorption and photo-charge collection and enables internal gain through impact ionization leading to higher responsivity.

This study represents a step forward toward the integration of graphene into existing Si technology for new generation optoelectronic devices.

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