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Analysis of semi-insulating carbon-doped GaN layers using deep-level transient spectroscopy

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ABSTRACT

Electrically active defects in carbon-doped GaN layers were studied with a metal/carbon-doped GaN (GaN:C)/Si-doped GaN (GaN:Si) MIS structure. The GaN:C layers were grown with three different carbon doping concentrations (N_C). A semi-vertical metal/semi-insulator/n-type semiconductor (MIS) device was fabricated to perform deep-level transient spectroscopy (DLTS) measurements. Two electron traps E1 and E2 with energy level at $E_C - (0.22–0.31)$ eV and $E_C - (0.45–0.49)$ eV were observed. E1 and E2 are associated with a nitrogen vacancy V_N-related defect in the strain field of extended defects and a nitrogen antisite defect, respectively. By changing the reverse bias voltage of the DLTS measurement, the location and relative defect concentration of the E1 and E2 traps could be verified. A dominant electron trap E3 with an unusual capture cross section was only observed in devices with an $N_C = 2 \times 10^{19}\,cm^{-3}$ GaN:C layer. This may charge carriers from a defect band and lead to the charge redistribution in the GaN:C layer when forward biased. A hole trap H1 with energy level at $E_V + 0.47$ eV was found for the pulse bias in the forward ON-state. H1 is suggested to correspond with the C_N induced 0/+ donor level. By analyzing the schematic band diagrams across the MIS structure, the carrier transport and defect charging mechanisms underlying the DLTS transient measurements are illustrated. The identification of the trap states in the carbon-doped GaN with different N_C gives further understanding on the carbon doping impact on electric characteristics of GaN power devices made on Si substrates.

I. INTRODUCTION

For GaN power devices, carbon is commonly used as a p-type dopant to achieve a high resistivity buffer layer, yielding a high vertical breakdown voltage. However, carbon induces various defects in the GaN buffer layer, which create deep levels in the bandgap and act as traps and generation-recombination centers that significantly affect the dynamic behavior and reliability of the devices for power and RF applications.[1–5] To investigate the relevant defects, deep-level transient spectroscopy (DLTS), a powerful technique for the characterization of electrically active defects,[6–8] is used, with some requirements for the probed semiconductor device structure. For example, the doping concentration of the semiconductor should be selected wisely considering the detection limit, and the (semi-insulating) behavior at low doping as a proper capacitance value is needed to avoid being overwhelmed by the system noise.[6–8] To get informative spectra, co-doping of C and Si to the GaN layer is most studied as it forms a metal-n-type GaN Schottky diode, which allows straightforward DLTS analysis.[9–14] Characterizing the deep levels in a GaN:C buffer used in real device structures is less straightforward because the silicon doping can have an impact on the crystal structure and on the grown-in defect distributions.[15–17]

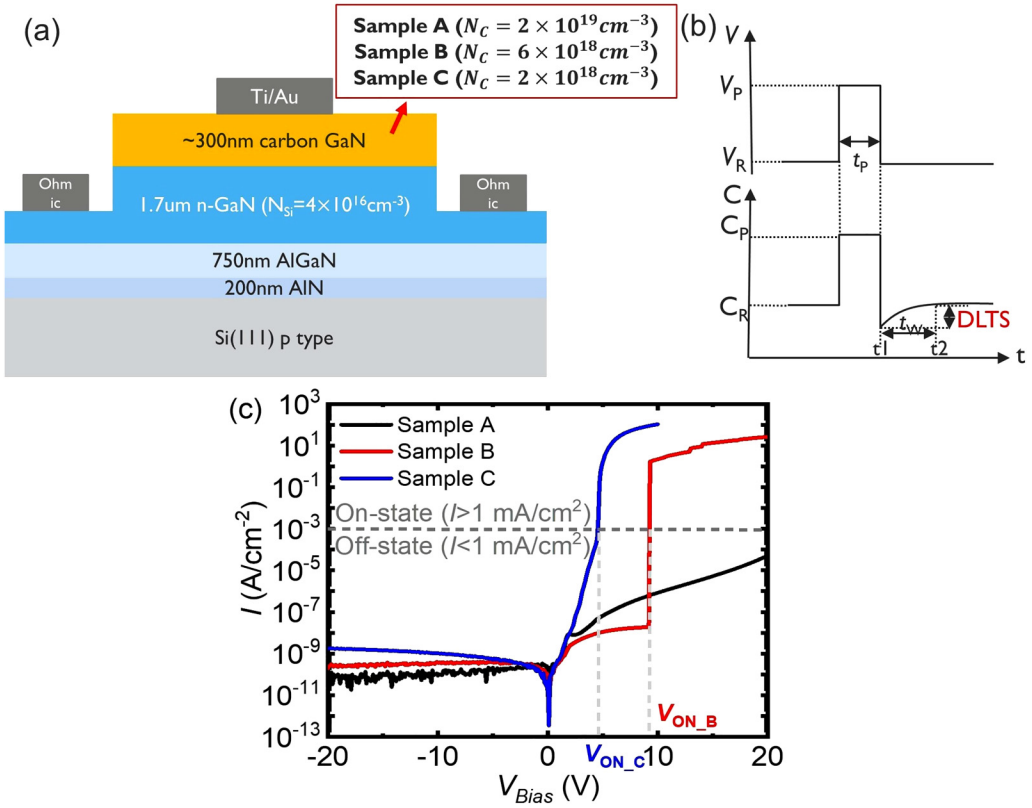

FIG. 1. (a) The cross section of the device structure. (b) The simplified scheme of the DLTS measurement principle. (c) The I–V characteristics of the three types of samples at room temperature.

In this article, a metal/carbon-doped GaN (GaN:C)/silicon-doped GaN (GaN:Si) structure grown on (111) p-type Si substrates was used to perform the DLTS measurements. Both the electron and hole carriers can be captured by defects in the GaN:C layer. By measuring the transient capacitance change after the fill voltage pulse as a function of temperature, the carrier emission process of charge trapped in the deep levels can be probed. The defect characteristics, such as activation energy and capture cross section, were obtained from a standard Arrhenius plot. For comparison, three GaN:C layers with different carbon doping concentrations (N_C) were investigated.

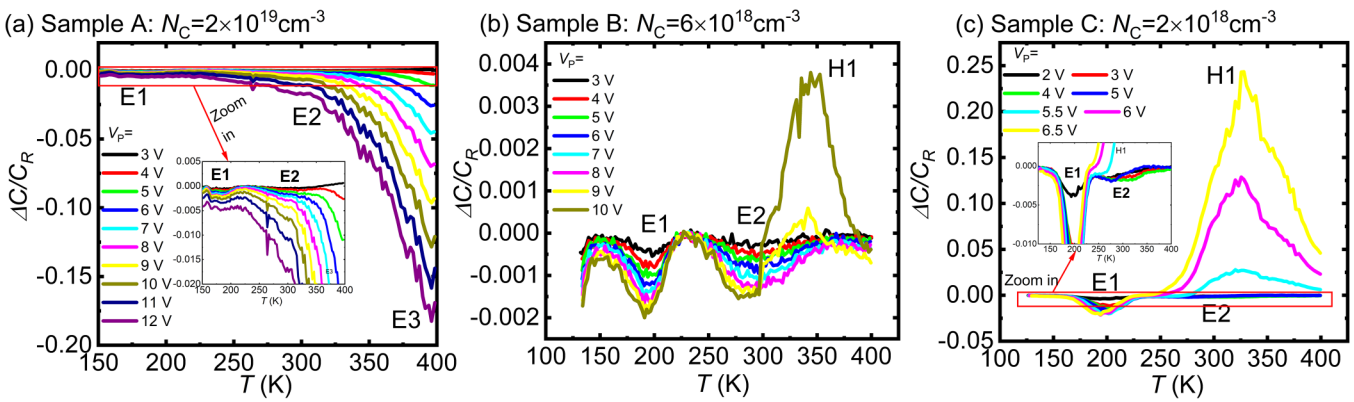

FIG. 2. The DLTS spectra as a function of V_P for (a) sample A, (b) sample B, and (c) sample C with V_R = 0 V, t_W = 9.5 Hz, and t_P = 1 ms.

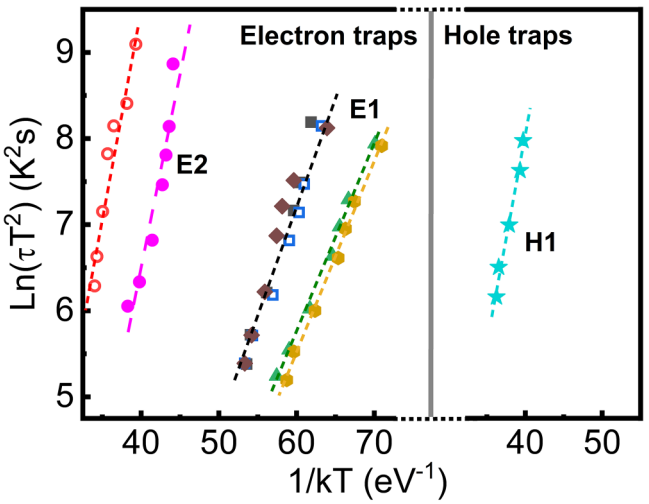

FIG. 3. Arrhenius plots of the traps measured in the three samples.

II. EXPERIMENTAL DETAILS

The device structure studied is shown in Fig. 1. The samples were grown on 150 mm (111) p-type Si substrates using metal-organic chemical vapor deposition. First, AlN and AlGaN transition layers (TLs) were grown, followed by a 1.7 μm n-type Si-doped GaN layer, with an Si doping concentration (N_{Si}) of 4×0^{16} cm^{-3}. On top of that, a 300 nm target GaN layer with different N_C was grown: $N_C = 2\times1019$ cm^{-3} for sample A, $N_C = 6\times10^{18}$ cm^{-3} for sample B, and $N_C = 2\times10^{18}$ cm^{-3} for sample C. Then, a device with metal/semi-insulator GaN:C/n-type semiconductor junction was fabricated to perform the DLTS measurements as shown in Fig. 1(a). It should be remarked that except for the Si-doped GaN bottom contact layer, the stack is similar as is used for fabricating real HEMT devices, so that little impact on the resulting defects is expected.

The DLTS was performed on the devices in a helium compressor (down to 5 K) cryostat with a Semilab DLS-83D tool using a capacitance bridge operating at 1 MHz. The capacitance transient can be measured after the bias pulse from a reverse bias V_R to a pulse bias V_P, and by scanning the temperature, the DLTS spectra can be obtained, as shown in Fig. 1(b). The detection limit of the normalized capacitance transient amplitude ($\Delta C/C$) is in the range of 10^{-4} for our setup.

The current–voltage (I–V) curves of the three samples under reverse and forward bias are shown in Fig. 1(c). The I–V characteristics show an asymmetric behavior between forward and reverse bias. In this article, we will focus on the carrier capture and emission processes under forward bias. When the forward current density $I > 1$ mA/cm^2, the device is defined as operating in the ON-state. When the forward current density $I < 1$ mA/cm^2, the device is defined as operating in the OFF-state. The corresponding turn-on voltages are called V_{ON} [as shown in Fig. 1(c)]. It should be noted that sample A operates in the OFF-state for the whole forward bias range studied, while $V_{ON\_B} = \sim9$ V and $V_{ON\_C} = \sim5$ V.

TABLE I. Characteristics of electron and hole traps for the samples.

Trap	Activation energy (eV)	Capture cross section (cm^2)
E1	0.22–0.31	9×10^{-19}–3×10^{-17}
E2	0.45–0.49	$1\sim5\times10^{-17}$
H1	0.47	3×10^{-17}

III. RESULTS AND DISCUSSION

The DLTS spectra as a function of V_P for the three types of GaN:C layers are shown in Fig. 2. Because of the different V_{ON} observed for the three samples, V_P was selected differently in order not to degrade the devices during the DLTS measurements. After each DLTS temperature scan, a C–V measurement was conducted and compared with the initial C–V curve. They are found to overlap with each other, which suggests that the DLTS measurement does not induce degradation and the measured traps exist in the virgin devices.

The y axis $\Delta C/C_R$ of the spectra can be written as

$$\frac{\Delta C}{C_R} = \frac{C_{t1} - C_{t2}}{C_R},$$

where the C_{t1} and C_{t2} are the depletion capacitances of the stack layers at the $t1$ and $t2$ are the time, respectively. The DLTS measurement time window $t_W = t2 - t1$. C_R is the steady state capacitance when the devices are biased at reverse voltage V_R. The negative value of $\Delta C/C_R$ means that electrons are captured by the traps existing in the GaN:C layer, GaN:Si layer, or at the interface between them. On the contrary, a positive value of the $\Delta C/C_R$ means holes were captured by the traps.

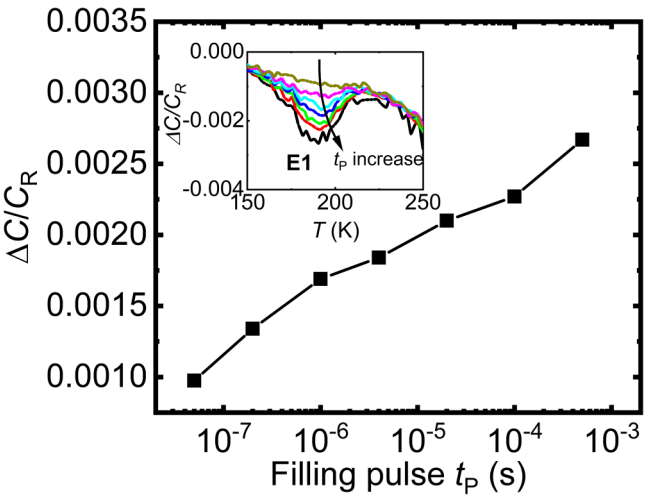

FIG. 4. Semilogarithmic plot of the DLTS signal amplitude vs filling pulse time for the trap E1.

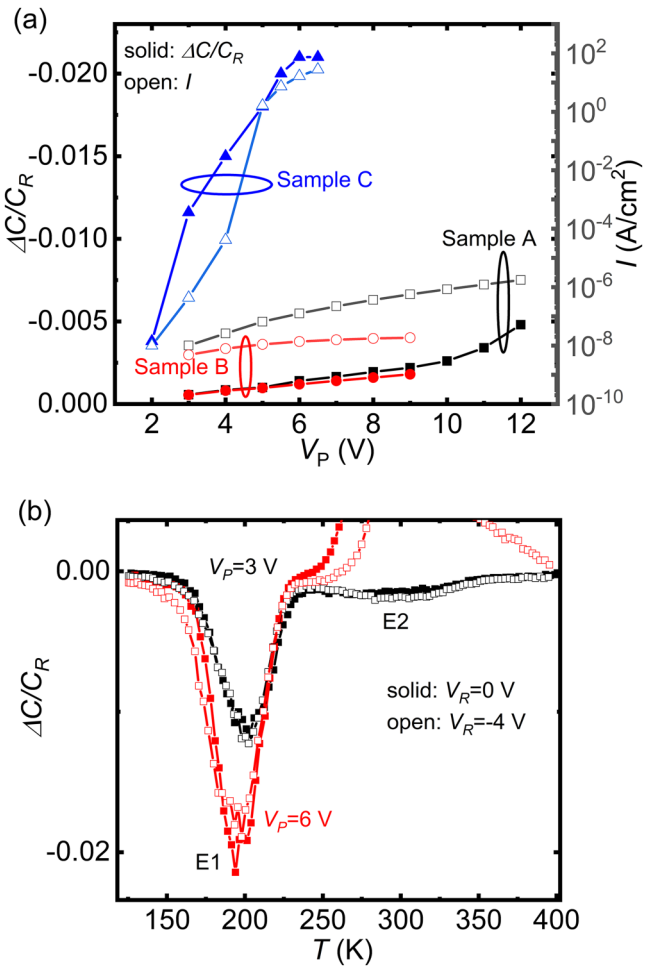

FIG. 5. (a) The DLTS peak amplitude of the trap E1 and leakage current density at different V_P (b) The DLTS spectra as a function of V_R with fixed V_P

From the spectra of the three samples, we found that the following: (i) Only (negative) electron trap peaks were observed for sample A. (ii) Two electron traps named E1 and E2, located around 190 and 300 K, respectively, are observed for all three samples. (iii) An electron trap peak named E3 with extremely high amplitude is dominant for sample A. (iv) A (positive) hole trap peak H1 was observed for samples B and C when V_P is biased beyond V_{ON}. For clarity, we will discuss the DLTS results of the V_P bias at the OFF-state and ON-state separately.

A. V_P bias at OFF-state

When the V_P bias at OFF-state, two electron traps E1 and E2, located around 190 and 300 K, respectively, are observed for all three samples. With the V_P increasing, the amplitude of the DLTS spectrum increases, meaning more electrons are captured. By changing the t_W, the carrier emission time constants (τ_e) at different temperature were obtained, and an Arrhenius plot can be constructed as shown in Fig. 3. The corresponding energy level and capture cross section of the traps derived from the Arrhenius plots are shown in Table I.

Electron traps with E1 and E2 were commonly observed in undoped,[18] intentionally n-type-doped,[19] and carbon-doped GaN layers,[9–14,20] which means that they are intrinsic defects not related to doping impurities. By changing the pulse duration t_P, one can show that the amplitude of E1 increases linearly with $\ln(t_P)$ (Fig. 4). This behavior is the fingerprint of extended defect due to the build-up of potential barrier from charging states.[21] By comparing the energy level and capture cross section with the results in the literature, E1 and E2 are thought to be associated with nitrogen vacancy (V_N) related complexes trapped in the strain field of the threading dislocations[19,22] and nitrogen antisite defects (N_{Ga}),[14,19,23–25] respectively.

The relative DLTS peak amplitude ($\Delta C/C_R$) of E1 and the leakage current density at different V_P are shown in Fig. 5(a). The amplitude of the DLTS peak has a one-to-one relation with the leakage current density. When V_P is in the OFF-state (i.e., full range of V_P in sample A and below $V_{ON\_B} = 9$ V in sample B), the

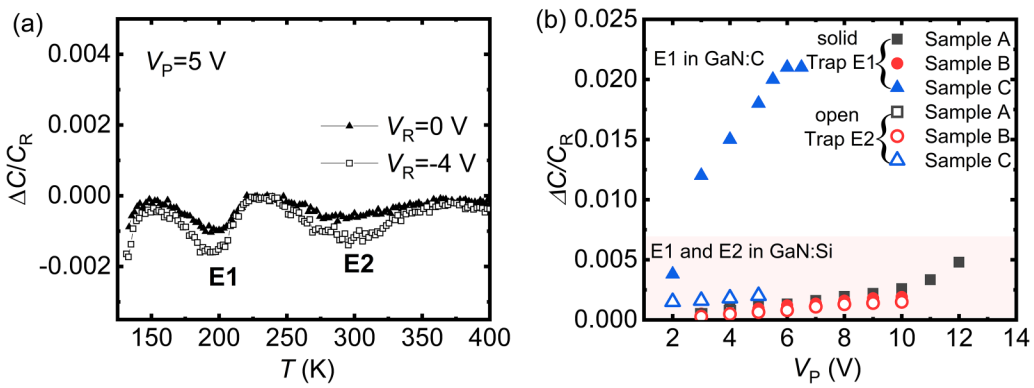

FIG. 6. (a) The DLTS spectra as a function of V_R with V_P in the OFF-state. (b) The location of the detected electron traps E1 and E2.

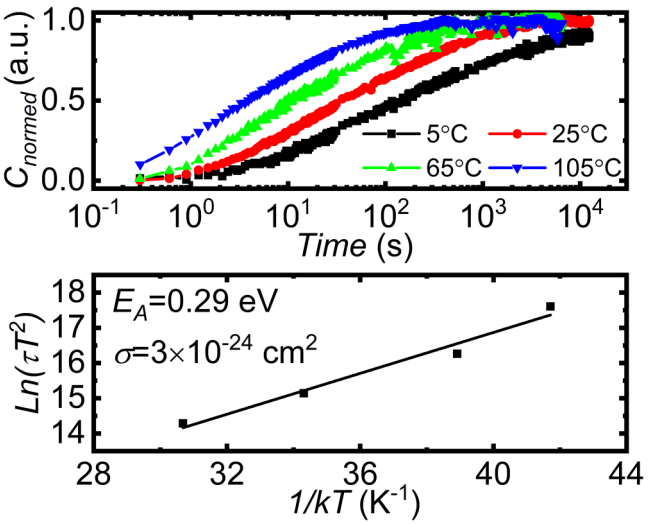

FIG. 7. Capacitance transient curves of sample A at different temperatures and the extracted Arrhenius plot.

relative amplitude of the peak is very small ($<2\times10^{-3}$), which means that the electron trap concentration (corresponding to the DLTS signal amplitude) of E1 is very low. However, when V_P is in the ON-state (jump of leakage current density at ~5 V in sample C), the amplitude of the E1 peak is ~10 times higher than the values at the Off-state. The sudden trap concentration increase of E1 is regarded as resulting from the contribution of the E1 traps in the GaN:C layer. To further verify that, spectra at $V_R = 0$ V and −4 V of sample C were compared to change the depletion width in the GaN:Si layer as shown in Fig. 5(b). The results show that the amplitude of the E1 peak changes little with V_R changing from 0 to −4 V when V_P is in the ON-state, confirming that the large trap concentration increase of E1 results from the contribution of the GaN:C layer instead of the GaN:Si layer. Meanwhile, the amplitude of the E2 peak does not increase with V_P in the ON-state, indicating that the trap E2 is only located in the GaN:Si layer. The DLTS results of V_P in the OFF-state with $V_R = 0$ and −4 V are shown in Fig. 6(a). It is found that the amplitude of E1 and E2 peaks increase with V_R changing from 0 to −4 V. Because V_R changes the depletion width of the GaN:Si layer, the sample exhibits a wider depletion width when $V_R = -4$ V in comparison to $V_R = 0$ V, and more traps in the GaN:Si layer can be detected. Thus, E1 and E2 traps can be thought to exist in the GaN:Si layer. The location and relative concentration of the detected electron traps E1 and E2 are summarized in Fig. 6(b). E1 is located in both GaN layers, while E2 is only located in the GaN:Si layer. This is also consistent with the fact that the N_{Ga} defect level was found anti-correlated with the C-related traps.[14] In other words, the E2 concentration will be suppressed in the GaN:C layer.

There is another electron trap E3 with high amplitude, which is dominant and is only observed in sample A. The peak maximum of E3 cannot be seen due to the temperature limit of the DLTS measurement system (the maximum temperature is 400 K). To extract the energy level of E3, capacitance transient measurements with a longer recovery time were performed. An unusually small activation energy of ~0.29 eV and very low electron capture cross section σ of 3×10^{-24} cm^2 were obtained from the capacitance transient measurements, as shown in the Fig. 7. The capture cross section is too small in comparison to the results in the literature, which can be understood by a defect band (DB) carrier transport model for the highly carbon-doped GaN as illustrated in Ref. 26. The electron traps E3 are thought to be the acceptor-like traps C_N (0/−1), which capture electrons from the defect band, so the activation energy between the C_N and the DB is much smaller than the activation energy ~0.9 eV between C_N and the valence band.[26,27] The extremely small σ of the trap E3 also indicates a smaller effective density of states corresponding to electron exchanges between a defect band and a deep-level trap.

The band diagram and trap charging process of the three types of GaN:C layers with V_P in the forward OFF-state are shown in Fig. 8. In the V_P stress phase, the space charge region (SCR) in the GaN:Si layer shrinks. The amount of negative charges in the GaN:Si layer is thus increased. For the highest N_C layers (sample A), the electrons move in the GaN:C layer via hopping in

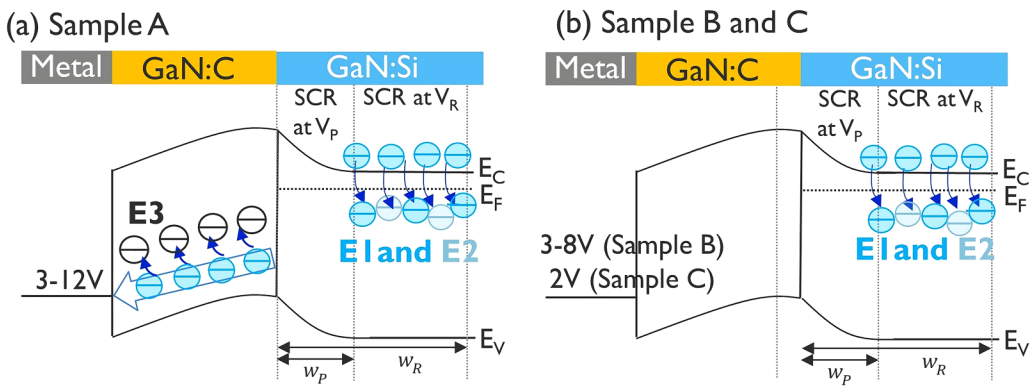

FIG. 8. The band diagram and trap charging process of (a) sample A and (b) samples B and C when V_P is in the OFF-state.

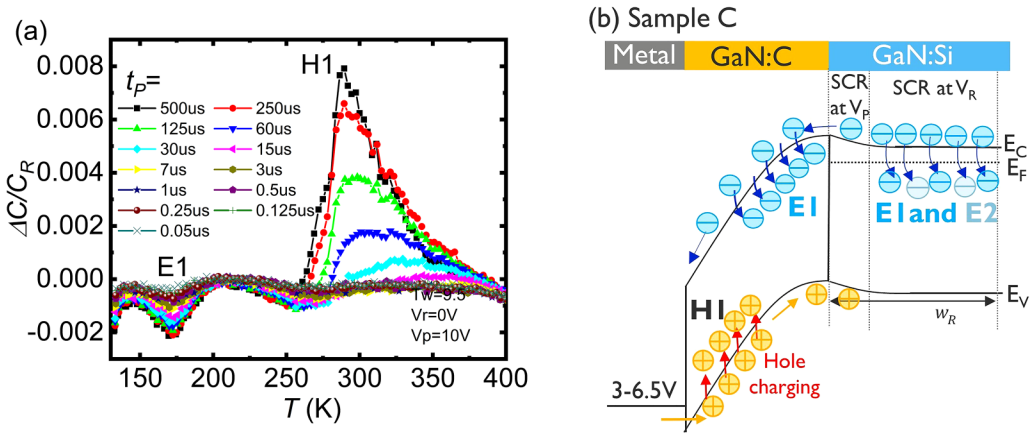

FIG. 9. (a) The DLTS spectrum of sample C with t_P changing. (b) The band diagram and trap charging process of sample C when V_P is in the ON-state.

the DB and are captured by the E3 traps. This, results in a charge redistribution across the GaN:C layer. For the lower N_C layer samples B and C, only E1 and E2 traps in the GaN:Si layer are filled.

B. V_P bias at the ON-state

A hole trap H1 around 325 K is observed when V_P is in the ON-state for samples B and C. With increasing V_P, the relative amplitude of H1 increases quickly. The energy level and capture cross section of H1 extracted from an Arrhenius plot are shown in Table I. The H1 trap can be assigned to the 0/+1 donor state of C_N,[28,29] supported by the fact that the energy level of H1 is close to the calculated energy level for the C_N donor-like state (around $E_V + 0.35$ or 0.48 eV).[30,31] Hole capture processes have been reported for a carbon-doped GaN buffer layer using DLTS[28,29,32–35] and substrate stress,[36] and a C_N (0/+) donor-like state was found in a p-type GaN layer.[29] The DLTS spectrum of sample C with the changing t_P is shown in Fig. 9. The peaks related to the H1 trap in terms of maximum temperature (T_{peak}) shift to low temperature when applying higher t_P, which indicates that the H1 trap shows band-like behavior of a discrete multi-states.[18]

The band diagram and trap charging process from V_P in the ON-state of sample C are shown in Fig. 9. When the V_P bias increases to a value higher than V_{ON}, the device is turned on. The transport of electrons in the GaN:Si layer and of holes in the GaN:C layer result in a high forward current. Under the ON-state V_P bias, the neutral C_N trap (H1) in the GaN:C layer captures a hole and changes into the +1 state. Meanwhile, more electrons are captured by the E1 trap in the GaN:C layer, resulting in an increase of the E1 DLTS peak.

IV. CONCLUSION

In summary, a metal/GaN:C/GaN:Si MIS device structure was employed to investigate the impact of carbon on the characteristics of a GaN layer. The DLTS spectra of the test structures have been studied under forward bias voltage. At forward OFF-state V_P bias, two electron traps E1 and E2 were observed for the three N_C levels studied, while another electron trap E3 was observed in the highest carbon-doped sample A, which is dominant and results from exchanging charges with a defect band. By changing the V_P and V_R, E1 was found located in both GaN:C and GaN:Si layers, while E2 is only located in the GaN:Si layer. When V_P is in the ON-state, a hole trap H1 with energy level at $E_V + 0.47$ eV was found, which is associated with the C_N (0/+1) donor-like state. Based on the deep-level information, the schematic band diagram and trap charging process in the structure under forward bias were derived.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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