Current-mode deep level transient spectroscopy of a semiconductor nanowire field-effect transistor

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One of the main limiting factors in the carrier mobility in semiconductor nanowires is the presence of deep trap levels. While deep-level transient spectroscopy (DLTS) has proved to be a powerful tool in analysing traps in bulk semiconductors, this technique is ineffective for the characterisation of nanowires due to their very small capacitance. Here, we introduce a new technique for measuring the spectrum of deep traps in nanowires. In current-mode DLTS ("I-DLTS"), the temperature-dependence of the transient current through a nanowire field-effect transistor in response to an applied gate voltage pulse is measured. We demonstrate the applicability of I-DLTS to determine the activation energy and capture cross-sections of several deep defect states in zinc oxide nanowires. In addition to characterising deep defect states, we show that I-DLTS can be used to measure the surface barrier height in semiconductor nanowires. *Published by AIP Publishing.*
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I. INTRODUCTION

Semiconductor nanowires are promising candidates for applications in nanoelectronics.[1,2] Various nanowire-based devices including field-effect transistors (FETs),[3,4] sensors,[5] axial and core-shell heterostructures,[6] and single-electron transistors[7] have been reported. The electrical properties of nanowires dramatically depend on defects located both in the nanowire core and on the nanowire surface.[8] Thus, the understanding of defect behaviour is crucial for controlling nanowire transport properties. The investigation of electrically active deep level defects in bulk semiconductors is usually carried out by means of transient techniques such as deep level transient spectroscopy (DLTS)[9] and its derivatives (e.g., photoinduced current spectroscopy—PICTS[10] and current transient spectroscopy[11]), thermostimulated current,[12] electron paramagnetic resonance, and others. Here, the term "deep level" denotes a state that is located deep in the semiconductor band gap (i.e., at energies lower than $E_C - k_BT$ and higher than $E_V + k_BT$, with E_C and E_V being the conduction band minimum and valence band maximum, respectively).

Investigation of the electrically active deep defect states in nanowires by DLTS is a challenging task, mainly due to the difficulties in measuring the very small capacitances of nanowire devices. Only a few papers have therefore been published on nanowire deep levels: DLTS in combination with PICTS was used to study catalyst-related electrical defects in an array of Si nanowires;[13] DLTS was used to study a single GaN nanowire pn-junction;[14] and low frequency noise spectroscopy (LFNS) was applied by Motayed *et al.* to investigate the effects of metal catalysts on Si nanowires.[15,16]

A different approach has been used to study nanoscale devices (such as thin film field-effect transistors), exploiting current-mode DLTS (I-DLTS) as opposed to the conventional capacitance-mode DLTS.[17] In I-DLTS, the relaxation of the current through the channel in response to a gate voltage pulse is measured. I-DLTS is a non-destructive technique which can be carried out directly on a device in a transistor geometry and does not need any additional fabrication steps. Since nanowire field effect transistors may become constituents of future electronic devices, I-DLTS is a promising technique to study them.

In this paper, we present I-DLTS measurements carried out on individual semiconductor nanowire field effect transistors. Theoretical models for conductivity relaxation driven by states on the nanowire surface are proposed. In addition to the usual characterisation of the deep traps in the semiconductor, an analytical model allows the measurement of the surface band-bending of a ZnO nanowire. These results corroborate data obtained using surface sensitive techniques such as ultraviolet photoelectron spectroscopy[18] and surface photovoltage measurements.[19]

A. Current-mode deep level transient spectroscopy in nanowires

1. I-DLTS method

In I-DLTS measurements on nanowire FETs, a fixed drain-source voltage V_{ds} is applied to the nanowire resulting in a constant current $I_{ds,0}$ through the nanowire. The gate voltage is kept at a quiescent value V_{GQ}, and a gate voltage pulse ΔV_G is applied periodically with period T_P and width t_P [Fig. 1(a)]. In n-type nanowires (like ZnO), a positive pulse ΔV_G populates discrete deep trap states with electrons, which, after the end of the pulse, get emitted from the deep traps with an emission rate e_n, contributing to the relaxation current $\Delta I(t) = I(t) - I_{ds,0}$ through the nanowire [Fig. 1(b)].

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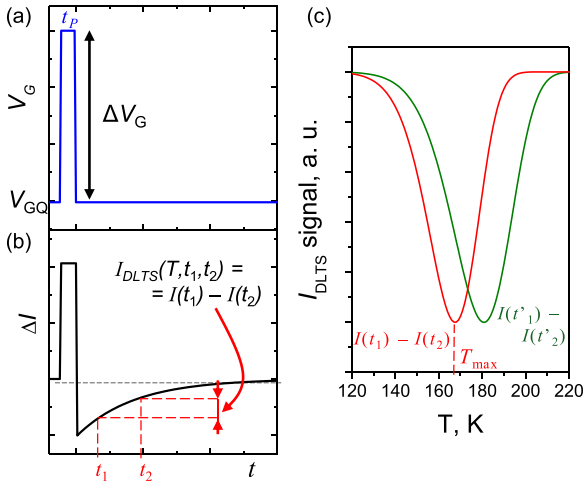

FIG. 1. I-DLTS principle of operation. (a) Time-dependence of the gate voltage; (b) time-dependence of the current through the nanowire; (c) I-DLTS spectra constructed using two different sets of times (t_1, t_2) and (t'_1, t'_2).

The I-DLTS signal is constructed by measuring the relaxation current at times t_1 and t_2 after the end of the pulse and subtracting them: $I_{\mathrm{DLTS}} \equiv I(t_1) - I(t_2)$.

The rate of carrier emission e_n from the deep traps can be expressed as $e_n \propto \sigma_0 \exp(-E_{\mathrm{dl}}/k_{\mathrm{B}}T)$, where E_{dl} is the deep trap activation energy, σ_0 the trap cross-section, and k_{B} Boltzmann's constant. Hence, the emission rate will vary with temperature T. At sufficiently low temperatures, the emission rate will be much lower than t_2^{-1}, resulting in $I(t_1) - I(t_2)$ being close to zero. Conversely, at high temperatures, the emission rate will be much higher than t_1^{-1}, also resulting in $I(t_1) - I(t_2) = 0$. At some intermediate temperature, $T_{\max}$, I_{DLTS} will reach a peak value [Fig. 1(c)]. The value of $T_{\max}$ depends on the choice of t_1 and t_2. Assuming an exponential time dependence of the current $\Delta I(t) \propto \exp(-e_n t)$, at temperature $T_{\max}$, there is an unambiguous relationship between the emission rate and the times t_1 and t_2: $e_n(T_{\max}) = \frac{\ln(t_2/t_1)}{t_2 - t_1}$.[9] By choosing different values of t_1 and t_2 and measuring the temperature at which the maximum in $I_{\mathrm{DLTS}}(T)$ occurs, we obtain the dependence of e_n on temperature. From this dependence, we can obtain the apparent cross-section of the trap σ_0 and its energy position in the band gap E_{dl}.

It will be shown later that electron emission from the electron traps generally results in a negative current transient signal as shown in Fig. 1(b). This gives rise to an I-DLTS minimum [Fig. 1(c)]. Conversely, hole emission will result in the opposite current transient sign, giving rise to an I-DLTS maximum. Semiconductor nanowires have different types of traps residing in the core of the nanowire, on its surface, and on the semiconductor-dielectric or semiconductor-metal interfaces. These traps will affect the current through the nanowire in different ways. An account of the physical phenomena that govern the dynamics of the carriers due to the deep surface trap states is given in Sec. I A 2.

2. Current through the nanowire FET

In general, surface band bending affects the conductivity of a nanowire. For example, ZnO nanowires have a surface charge depletion layer due to a negative surface charge with the dominant conductivity happening in the core of the nanowire.[18,19] InAs nanowires, on the other hand, have a surface electron accumulation layer which accounts for the main contribution to the conductivity.[20]

It can be shown (supplementary material) that the current through a back-gated nanowire FET can be expressed as

$$I_{\mathrm{ds}} = \frac{\mu_{\mathrm{eff}} C_{\mathrm{oxide}}}{L^2}[V_{\mathrm{G}} - V_{\mathrm{T}}]V_{\mathrm{ds}}; \qquad V_{\mathrm{T}} = Q_{\mathrm{ss}}/C_{\mathrm{oxide}} + q\pi R^2 N_d L/C_{\mathrm{oxide}}, \tag{1}$$

where μ_{eff} is the effective carrier mobility, V_{G} and V_{ds} are the gate voltage and drain-source voltage, respectively, V_{T} is the threshold voltage, Q_{ss} is the surface trap charge in coulombs, N_d is the concentration of ionised shallow donors, L is the distance between contacts, and R is the radius of the nanowire. In general, Q_{ss} depends on the gate voltage, and we will address this later in this paper. In this paragraph, however, we neglect the gate-voltage dependence of the surface charge. The capacitance C_{oxide} is calculated based on the model of a metallic wire above a charged plane (supplementary material). Equation (1) coincides well with the usual transistor formula in the linear regime[3,21] with the additional term $Q_{\mathrm{ss}}/C_{\mathrm{oxide}}$. Because it is usually difficult to estimate the surface state concentration, this extra term can cause ambiguity in the estimation of the ionised donor concentration N_d. In addition, the analysis is carried out on the system exhibiting axial symmetry. Since this work studies the back-gated nanowires, it should be therefore noted that the current mathematical model is only valid as a first-order approximation.

Figure 2 schematically depicts a standard ZnO nanowire with a surface depletion region due to negatively charged surface states which are attributed to the absorbed oxygen molecules. Carrier capture onto the surface states depends on the surface barrier height $qV_{\mathrm{B}} = E_b$. It can be seen in Figs. 2(a) and 2(b) that the surface barrier for electrons is affected by the gate voltage. The relationship between the gate voltage and the nanowire surface barrier height for a partially depleted nanowire can be expressed as (supplementary material)

$$V_{\mathrm{B}}(V_{\mathrm{G,eff}}) = \frac{qN_d W_d(V_{\mathrm{G,eff}})[2R - W_d(V_{\mathrm{G,eff}})]\ln(R/[R - W_d(V_{\mathrm{G,eff}})])}{2\epsilon_0 \epsilon_{\mathrm{ZnO}}}, \tag{2}$$

where W_d is the depletion region width

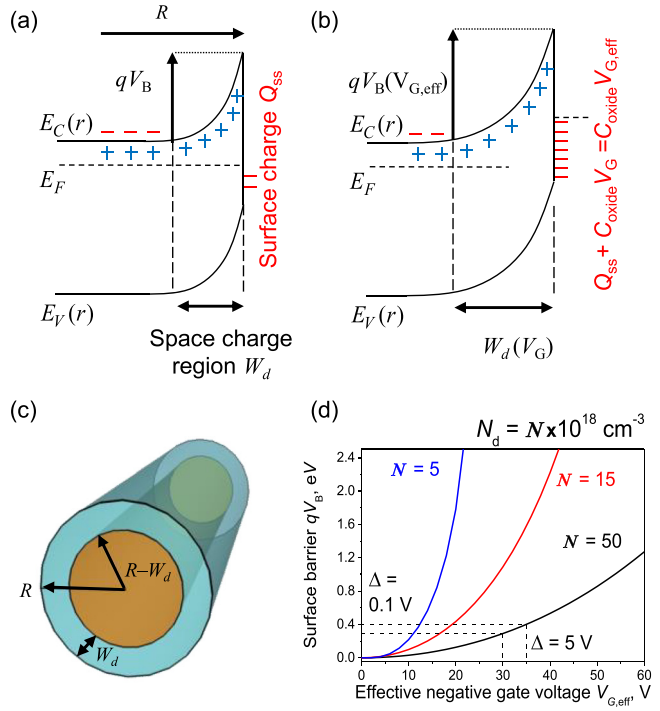

FIG. 2. Model of nanowire band bending for an n-type nanowire with a negative surface charge and surface depletion region: (a) equilibrium condition, $V_G = 0$; (b) band diagram of the nanowire under applied negative gate voltage; (c) graphic representation, with the orange region being the conductive core and blue region being the depletion region; and (d) dependence of the surface barrier voltage on the effective negative gate voltage for ZnO nanowires with different donor concentrations, according to Eq. (2).

$$W_d(V_{G,\mathrm{eff}}) = R - \sqrt{R^2 - \frac{C_{\mathrm{oxide}} V_{G,\mathrm{eff}}}{qN_d \pi L}}. \tag{3}$$

Here, $V_{G,\mathrm{eff}}$ is the effective gate voltage $V_{G,\mathrm{eff}} = Q_{ss}/C_{\mathrm{oxide}} + V_G$ and ϵ_{ZnO} the dielectric constant of ZnO. Figure 2(d) shows the dependence of the barrier height V_B on $V_{G,\mathrm{eff}}$. In particular, for a typical ZnO nanowire with a surface barrier of 0.3 eV and with a donor concentration of $N_d = 5 \times 10^{19}\,\mathrm{cm}^{-3}$, an increase in the surface barrier by 0.1 eV (i.e., from 0.3 to 0.4 V) requires the gate voltage to change by 5 V.

3. Current transient in nanowires: Emission and capture from the surface trap

Deep electron traps located in the semiconductor volume (in bulk) will affect the current and capacitance transient behaviour.[9] The current transients in thin film transistors are affected by both bulk and surface traps. Since nanowires exhibit a very high surface-to-volume ratio, the current transient will predominantly depend on the surface states. Moreover, ZnO is known to be very surface sensitive,[22] and therefore, we will consider here only the surface traps.

Let us consider surface electron traps that are uniformly distributed on the surface of the n-type nanowire (Fig. 3). These electron traps have a delta-like density of states with activation energy E_{ss}. At quiescent gate voltage bias V_{GQ}, surface traps below the Fermi energy (with activation energy $E_{ss,2}$) are filled with electrons, while those traps above the

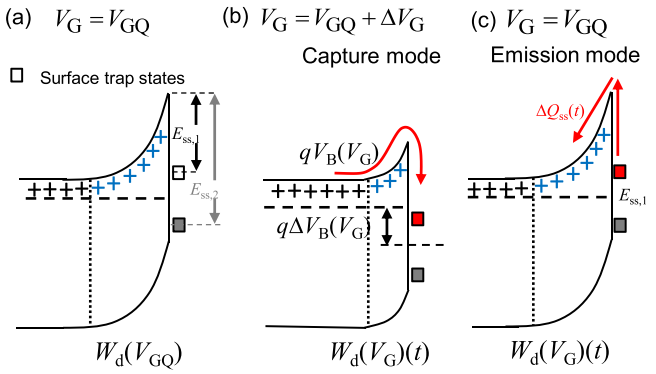

FIG. 3. Mechanism of the current transient in nanowires due to surface states: (a) quiescent gate voltage conditions V_{GQ}; (b) positive gate voltage pulse ΔV_G and electron capture onto surface states; and (c) emission of electrons from the filled traps into the conduction band at the quiescent gate voltage.

Fermi energy (with activation energy $E_{ss,1}$) are empty [Fig. 3(a)]. When a positive gate voltage pulse ΔV_G is applied, the Fermi energy changes its position, with surface traps below the Fermi energy capturing electrons. According to Shockley-Read-Hall statistics,[23,24] the capture of electrons onto the surface states follows an exponential law with capture rate c_n which depends on the surface barrier qV_B [Fig. 3(b)]. The change in time of the number of electrons captured on the surface state $n_{ss}(t)$ is

$$\begin{aligned} n_{ss}(t) &= n_{ss,\max}\,(1 - \exp(-c_n t)); \\ c_n &= \sigma_{ss}\gamma T^2 \exp(-qV_B/k_B T), \end{aligned} \tag{4}$$

where σ_{ss} is the surface state capture cross-section, $n_{ss,\max}$ the maximum possible number of trapped electrons, and $\gamma = 2\sqrt{3}(2\pi)^{3/2}h^{-3}k^2 m^*$, with m^* the effective electron mass. We assume as an approximation that the barrier height V_B is constant in time during the charge capture. It will however depend on the gate voltage as outlined in Sec. I A 2.

At the end of the positive gate voltage pulse, the number of electrons trapped on the surface traps is $n_{ss,0} = n_{ss,\max}(1 - \exp(-c_n t_p))$. When the gate voltage returns to the quiescent bias value, the filled levels start emitting electrons into the conduction band [Fig. 3(c)]. The time-dependence of the number of carriers trapped on the surface levels $n_{ss}(t)$ is

$$\begin{aligned} n_{ss}(t) &= n_{ss,0}\exp(-e_n t); \\ e_n &= \sigma_0 \gamma T^2 \exp(-E_{ss}/k_B T), \end{aligned} \tag{5}$$

where E_{ss} is the energy difference between the energy level of the surface trap and the conduction band and σ_0 is an effective minority carrier capture cross section.

The change in population of the surface levels will result in a current transient through the nanowire. Both the surface and bulk traps will effectively change the surface state charge Q_{ss} in Eq. (1). Surface charge may be represented as a sum of the constant surface charge and the transient surface charge: $Q_{ss}(t) = Q_{ss,0} + qn_{ss}(t)$. Taking into account the negative charge of electrons for the n-type nanowire, we get the current transient through the nanowire

$$\Delta I(t) = -\frac{V_{ds}\mu_{eff}}{L^2}\Delta Q_{ss}(t);$$
$$\Delta I_{emission}(t) = -\frac{\mu q}{L^2}V_{ds}n_{ss,0}\exp(-e_n t) = \Delta I_0\exp(-e_n t);$$
$$\Delta I_0 = \frac{\mu q}{L^2}V_{ds}n_{ss,0}$$
$$\Delta I_{capture}(t) = \frac{\mu q}{L^2}V_{ds}n_{ss,max}\exp(-c_n t). \quad (6)$$

The emission mode and capture mode[25] I-DLTS may be used to infer trap energies E_{ss} and the barrier height V_B, respectively. Both methods were exploited in this work. Here, we will neglect the temperature dependences of the Fermi level position and the carrier concentration. Therefore, we assume that the values of $n_{ss,0}$ and $n_{ss,max}$ are independent of temperature for given quiescent gate voltage, gate voltage pulse magnitude, and gate voltage pulse width.

The I-DLTS signal $I_{DLTS} = I(t_1) - I(t_2)$ is measured at different temperatures and different t_1 and t_2 pairs. Every pair will result in an I-DLTS peak: $I_{DLTS,max} = I_{DLTS}(T_{max})$. The magnitude of $I_{DLTS,max}$ depends on the prefactor ΔI_0 in Eq. (6). It can be shown that, if we choose times t_1 and t_2 so that t_1 varies but the ratio t_2/t_1 is fixed, then the magnitude of $I_{DLTS,max}/I_{ds,0}(T)$ [where $I_{ds,0}(T)$ is a quiescent current] corresponding to a specific trap level measured at different times t_1 will be independent of temperature. In this study, the t_2/t_1 ratio is fixed to 2 and $I_{DLTS,max}$ will therefore be equal $\Delta I_0/4$ (see supplementary material). The concentration of surface traps $N_{ss,0}$, in cm^{-2}, can be calculated from the I-DLTS signal maximum $I_{DLTS,max}$ [Eq. (6)], and the value of the quiescent current $I_{ds,0}$ [Eq. (1)] is given as follows:

$$N_{ss,0} = \frac{n_{ss,0}}{2\pi RL} = \frac{\Delta I_0}{I_{ds,0}}\frac{C_{oxide}(V_G - V_T)}{q2\pi RL} = \frac{4\cdot I_{DLTS,max}}{I_{ds,0}}\frac{C_{ss}(V_G - V_T)}{q2\pi RL}. \quad (7)$$

The concentration of bulk traps $N_{bulk,0}$, in cm^{-3}, can be calculated analogously

$$N_{bulk,0} = \frac{4\cdot I_{DLTS,max}}{I_{ds,0}}\frac{C_{ss}(V_G - V_T)}{q\pi R^2 L}. \quad (8)$$

4. I-DLTS measurement setup

The I-DLTS measurement setup is shown in Fig. 4. A ZnO nanowire field effect transistor with back-gate is used for the measurement. The drain-source voltage through the nanowire is kept constant at $V_{ds} = 0.2$ V. A negative quiescent gate voltage bias of $V_{GQ} = -10$ V keeps a large area of the n-type nanowire cross-section depleted. Gate voltage pulses ΔV_G of 10 V amplitude and 100 μs duration are applied to the gate of the nanowire FET with a repetition rate between 0.1 and 1 kHz. The current through the nanowire is probed by the differential pre-amplifier across a reference resistor whose resistance is much smaller than the nanowire resistance. The DC component of the current is filtered out, and the relaxation current is amplified. The signal is supplied to the oscilloscope, averaged, and digitised. The time value t_1 ranges from 50 μs to 4 ms.

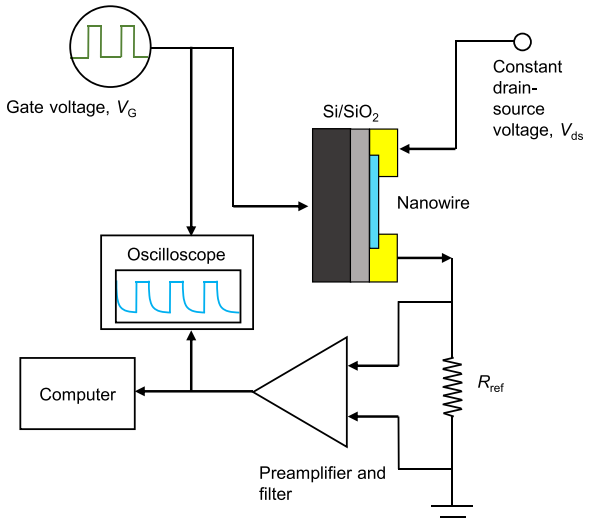

FIG. 4. I-DLTS measurement setup for the nanowire FET.

II. EXPERIMENTAL DETAILS

A. ZnO nanowire field effect transistor

ZnO nanowires were grown on $Al_2O_3(0001)$ substrates by oxygen plasma assisted molecular beam epitaxy using gold as a catalyst. Details of the growth conditions and nanowire properties are published elsewhere.[26] Nanowires are 40–100 nm thick and 1–4 μm long. The as-grown sample was ultrasonicated in 2-propanol to remove nanowires from the substrate. A droplet of the nanowire-2-propanol solution was deposited and dried on an oxidised silicon substrate with 120 nm silicon oxide thickness. Metal contacts to the nanowires were patterned by electron beam lithography. Nanowires were argon ion-beam milled for 30 s, and Ti/Au contacts were sputtered onto them [Fig. 5(a)] without breaking vacuum. The Ar ion milling was performed to remove an amorphous surface layer and thereby to decrease the contact resistance.[27] After fabricating the sample, the substrate was mounted onto the copper block of a chip carrier, which, in turn, was mounted on the end of the dip probe. Liquid helium was used to cool the sample down to 4.2 K.

Room temperature transport characteristics were measured with a Keithley 4200 semiconductor characterization system. The drain-source voltage dependence of the current of a typical ZnO nanowire is shown in Fig. 5(b), showing Ohmic behaviour. Four-point probe measurements showed a negligible contact resistance. The resistance of the ZnO nanowires ranged from 100 kΩ to 1 MΩ. The dependence of the drain source current on the gate voltage is depicted in Fig. 5(c). The on/off ratio was approximately 10^6. The field effect mobility of the nanowire was calculated from the drain-source current using Eq. (1). The nanowire effective mobility at room temperature varied from 10 to 20 $cm^2/(V\ s)$ from wire to wire. The effective room-temperature carrier concentration of the nanowires ranged from 10^{18} to 10^{19} cm^{-3}. The resistance, mobility, and carrier concentration values are in agreement with data obtained by other researchers.[3,18] The temperature

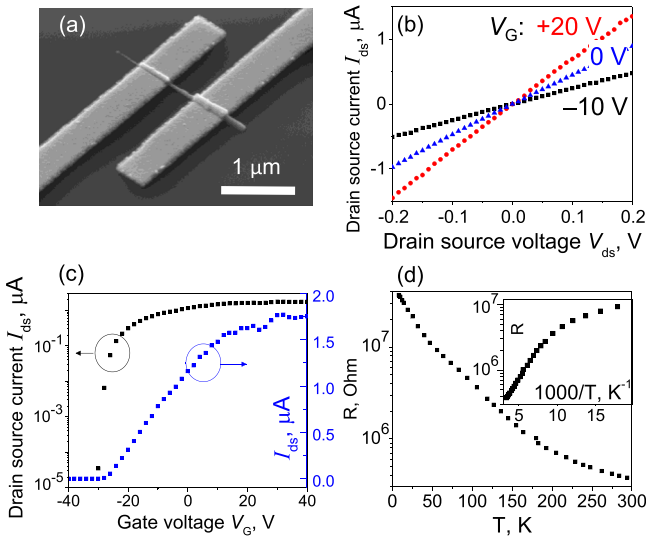

FIG. 5. (a) Scanning electron image of a connected nanowire; (b) room temperature current voltage characteristics of the nanowire at different gate voltages; (c) the gate voltage dependence of drain-source current; and (d) semi-logarithmic plot of the temperature dependence of the nanowire resistance. Inset: resistance on a logarithmic scale as a function of inverse temperature.

dependence of the 2-point probe DC resistance of a single nanowire is shown in Fig. 5(d).

B. I-DLTS: Trap characterisation

I-DLTS measurements were performed on four ZnO nanowires. The geometrical and electrical parameters of the studied nanowires are shown in Table I. Current transients at different temperatures for one nanowire are presented in Fig. 6(a). A transient drain current response to a gate voltage pulse similar to the one shown here was previously observed in ZnO nanowire FETs at room temperature in Ref. 28. Authors attributed the current transients on a time-scale of seconds to adsorption and desorption of oxygen molecules. However, no temperature dependence was carried out. Here, the time-scales are much faster (micro- and milliseconds), and the temperatures are lower. We therefore assume that the current transients in our measurements depend only on the charging and discharging of carrier traps in the nanowire, and the model for the carrier emission given above may be applied for the analysis of these data.

We shall now consider the transients in Fig. 6(a). A short negative relaxation immediately after the end of the gate voltage pulse with a time constant of approximately 50 μs is attributed to the equipment response and is similar among

TABLE I. Geometrical and room temperature electrical parameters of the nanowires used in the present study.

Nanowire	Diameter (nm)	Channel length (nm)	Mobility (cm^2/V s)	Carrier concentration (cm^{-3})
No. 1	60	500	16.1	6.5×10^{18}
No. 2	50	500	14.7	8.5×10^{18}
No. 3	64	700	15.2	3.7×10^{19}
No. 4	49	415	17	1.0×10^{19}

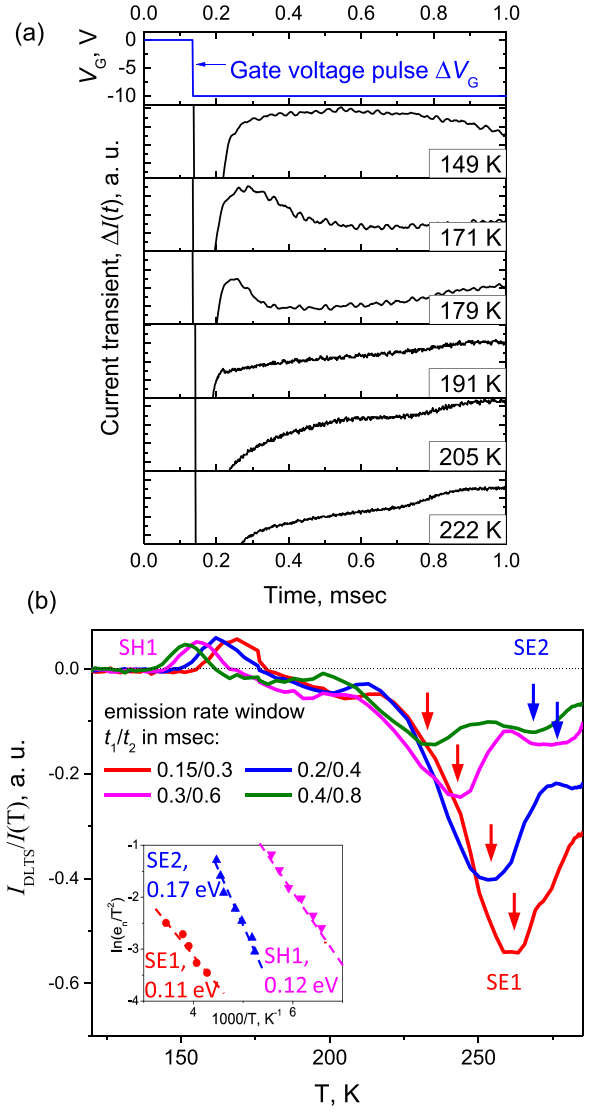

FIG. 6. (a) Current transients of nanowire No.1 at different temperatures for $\Delta V_G = 10$ V; the negative current peak at $t < 0.1$ ms is due to the equipment response; (b) I-DLTS signal normalized to static current with deep levels indicated. Inset: Arrhenius plots of levels SE1, SE2, and SH1 taken from the I-DLTS graphs in (b).

all the measured samples. The relaxation curves show the temperature-evolution of the current behaviour due to the deep trap. As expected from the exponential behaviour of the emission rate [Eq. (5)], the emission rate increases with temperature. It should be noted that the current transient in Fig. 6(a) becomes both negative and positive: negative at temperatures above 180 K, as expected from the theoretical description of the electron de-trapping [Fig. 1(a)] and positive at temperatures around 150 K, which potentially indicates an unusual behaviour of the charges: either hole de-trapping or electron trapping. The levels responsible for this behaviour are usually called in the literature "hole-like" levels[25] and will be discussed further.

I-DLTS spectra of ZnO nanowire No.1 are shown in Fig. 6(b). Peaks in this particular I-DLTS dependence may be attributed to two electron trap levels SE1 and SE2 and one level resembling a hole-like trap SH1 (which is not a real hole trap due to reasons outlined later in this paper). The

activation energies and apparent capture cross sections of these traps can be determined from the Arrhenius plots [Fig. 6(b), inset]. Parameters of the deep levels measured on four different nanowires are listed in Table II. The nanowires exhibit similar hole-like traps but different electron traps. The normalised amplitude of the traps $I_{DLTS}/I(T)$ is relatively large (reaching 0.5 for the level SE1 in nanowire No.1), which indicates a high density of surface traps.

The levels observed in this work have several pronounced traits that are not expected from simple bulk deep traps. First, whereas the I-DLTS SH1 magnitude at different rate-windows stays constant at different temperatures, absolute values of the peak magnitudes attributed to the electron traps, SE1, SE2, and SE3, rapidly increase with temperature [Fig. 6(b) shows levels SE1 and SE2]. This rapid increase in I-DLTS peak magnitude was observed in various reports and was attributed to the surface states at the ungated area of a FET.[17,29] Since the nanowire FETs in the present work are back-gated, the larger part of the nanowire surface is exposed to air, and this affects the I-DLTS signal through the nanowire surface states. This rapid increase in the I-DLTS signal does not allow accurate estimation of the concentration of the SE1, SE2, and SE3 traps.

In addition, we can compare the measured ZnO nanowire trap signatures with those of the levels studied in bulk ZnO. ZnO films, bulk crystals, and microwires have been studied by capacitance-mode DLTS with various electron trap levels observed.[30–35] Although the energies of the levels SE1, SE2, and SE3 coincide with the energies of the levels E1, E2, and E3 from these reports, the trap cross-sections are several orders of magnitude lower in the present work. This observation might indicate the existence of completely different electron traps in the bulk of nanowires or, conversely, a surface origin of levels SE1, SE2, and SE3 due to the potential cross-section reduction at the nanowire surface. This would corroborate our previous assumption of the surface origin of these levels. Level E4, however, coincides in both the energy and cross-section with the level E4 from Refs. 30, 31, and 35, where it is attributed to oxygen vacancies. The E4 trap concentration calculated using Eq. (8) is $1.3 \times 10^{17}\,cm^{-3}$ which is approximately 300 times less than the carrier concentration of the nanowire.

TABLE II. Activation energies, apparent cross-section, and concentration of trap levels derived from Arrhenius plots for four ZnO nanowires. For I-DLTS spectra and Arrhenius plots of all the nanowires (see supplementary material).

Levels	Nanowire No.	Energy (eV)	Cross-section (cm^2)	Concentration
SE1	1, 2	0.11	7×10^{-21}	–[b]
SE2	1, 2	0.15–0.2	4×10^{-19}–2×10^{-18}	–[b]
SE3[a]	1	0.25–0.3	$(1–5) \times 10^{-18}$	–[b]
E4	4	0.45	3×10^{-12}	3D, $1.3 \times 10^{17}\,cm^{-3}$
SH1	1, 3	0.12	8×10^{-19}	2D, $2.8 \times 10^{12}\,cm^{-2}$
SH2	2	0.2	3×10^{-18}	2D, $4.7 \times 10^{12}\,cm^{-2}$
SH3	3	0.2	2×10^{-19}	2D, $1.2 \times 10^{13}\,cm^{-2}$

[a]Level SE3 is in shown in Fig. 6 only at emission rate windows larger than those shown or at higher temperatures (see supplementary material).
[b]SE1, SE2, and SE3 I-DLTS peak magnitudes increase with temperature, and therefore, the existing model cannot be used for the trap concentration estimation.

Levels SH1, SH2, and SH3 show similar activation energies, temperature, and amplitude behaviour and will be examined together. Hole-like levels have been observed in some n-type FETs and are usually ascribed to the surface traps, in particular to hole-traps on the unpassivated surface of the FET (Ref. 25 and references therein). In the case of n-type ZnO nanowires, it is very unlikely for the levels SH1 to SH3 to be real hole traps; the reasons for this are as follows: For some ZnO nanowires, the amplitude of the current transient corresponding to the hole-like level is comparable to the static current through the nanowire ($I_{I-DLTS}(T_{max})/I(T_{max}) \approx 0.1$–$0.5$); assuming the hole-like level being real hole traps would indicate the concentration of holes comparable to that of electrons. On the contrary, no inversion current was observed in the FET transfer characteristics at large negative gate biases down to –60 V, indicating a negligible concentration of holes. Therefore, the levels SH1 to SH3 cannot be real hole traps. Assuming a surface origin of the SH1-SH3 traps, the trap concentration can be estimated from Eq. (7) to be between 2.8 and $12 \times 10^{12}\,cm^{-2}$, equivalent to one surface trap per 3 to 6 nm of length. Further study is needed to fully understand the origin of the levels SH1 to SH3.

Another phenomenon that can in principle account for the trapping and detrapping of electrons is tunnelling through the surface barrier. The depletion region calculated from Eq. (3) ranges from 3 to 10 nm which may be low enough for tunnelling effects to take place. It should be noted, however, that the tunnelling probability does not include any direct temperature dependence while being solely a function of the barrier height and the depletion region width. Although the temperature dependence may be included in the barrier height or depletion region width (all these values depend on the carrier concentration), we do not expect it to be exponential. Therefore, the fast temperature dependence of the emission or capture rates observed in I-DLTS curves cannot be explained by tunnelling effects.

In conclusion, all the levels observed in ZnO nanowire transistor I-DLTS, except the E4 level, appear to be surface state related. This corroborates our initial assumption about ZnO nanowires being mostly affected by the surface states. Because we cannot unambiguously determine the exact origin of the surface levels, we have to restrict our conclusions to the phenomenological description of their recharging characteristics. The only bulk level E4 is tentatively ascribed to the oxygen vacancies in the nanowire core. Independent of the traps' origin, we can extrapolate the emission rate and characteristic decay time to room temperature using Eq. (5). The time decay of electron detrapping ranges from 0.1 to 200 μs (SE1: 120 μs, SE2: 10 μs; SE3: 200 μs, E4: 0.1 μs, and SH1-SH3: 5–50 μs). These traps will therefore have different effects on the frequency response of future nanowire-transistors in electronic devices.

It should be noted that even though the nanowire bulk properties such as carrier concentration and mobility are similar among the four studied nanowires (Table I), the trap spectra vary significantly. Similar variability in nanowire electrical properties was observed previously in ZnO nanowires[36] and

was attributed to the variation in the density and occupancy of surface defects. The authors claim that this variability is intrinsic to ZnO nanowires. I-DLTS data presented in the current paper supports the predisposition of ZnO nanowires to electrical property variability.

C. I-DLTS: Surface barrier height measurement

As it was outlined in Sec. I A 3, capture mode I-DLTS may provide information on the nanowire surface barrier height. Any surface state that can trap electrons at positive gate voltages and de-trap electrons at negative gate voltages can be used for this purpose [Eq. (4)]. The surface barrier height depends on the effective gate voltage [Fig. 3(b.2), Eq. (2)], and therefore, temperature of the capture-mode I-DLTS peak will depend on the quiescent gate voltage value as well.

Capture-mode I-DLTS was carried out on nanowire sample No. 4 (Fig. 7). Figure 7(a) shows capture-mode I-DLTS spectra at two different quiescent voltages with the most prominent peaks at 220 K and 230 K. We assume that these two peaks correspond to the process of carrier capture over the surface barrier by the same surface trap level which we denote by C1. The surface barrier heights obtained from the I-DLTS measurements are 0.3 eV and 0.4 eV (for $V_{GQ} = 10$ V and $V_{GQ} = 0$ V respectively, see supplementary material). These values of the surface band bending in the ZnO nanowire

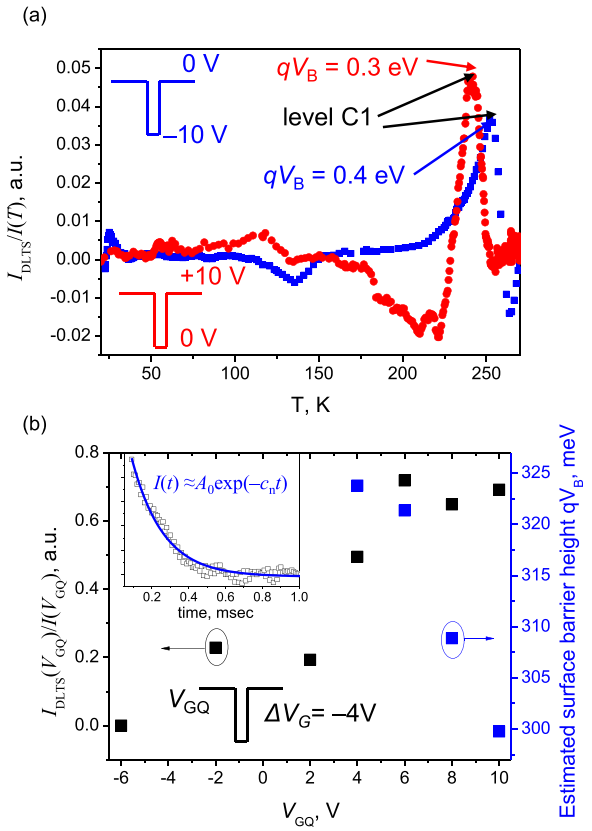

FIG. 7. (a) Capture-mode I-DLTS measurement on a ZnO nanowire with different quiescent gate voltages: $V_{GQ} = +10$ V (red) and $V_{GQ} = 0$ V (blue); the emission rate constant t_1/t_2 was 0.4/0.8 ms. Hole-like peaks are observed at 220–240 K. (b) Quiescent voltage dependence of the capture-mode I-DLTS signal and capture activation energy; the gate voltage pulse is –4 V. Inset: current transient at $V_{GQ} = 10$ V, $\Delta V_G = -4$ V; the blue line represents the exponential fit to the experimental data.

are similar to those obtained by Soudi *et al.*[19] (0.3 eV) and of the same order as data obtained by Chen *et al.*[18] (0.74 eV). The differences might arise due to different growth methods used.

According to the model in Fig. 3(b.2), the level C1 exhibits a varying capture activation energy (and consequently the surface barrier height) which depends on the quiescent voltage. The surface barrier qV_B decreases by 0.1 eV (from 0.4 eV to 0.3 eV) when the quiescent voltage increases from 0 to +10 V [Fig. 7(a)]. This value is on the same order of magnitude with that obtained from the model described in Sec. I A 2 [Fig. 2(d)]. The capture cross-section σ_{ss} stays approximately the same and is equal to 5×10^{-18} cm^2.

Figure 7(b) shows a more detailed quiescent voltage dependence of the I-DLTS signal magnitude, with a fixed gate voltage pulse of $\Delta V_G = -4$ V. The peak increases with quiescent voltage. Since the capture follows an exponential time-dependence [Fig. 7(b), inset], the capture time-constant can be inferred from the fit. It changes from 0.5 to 0.17 ms when the quiescent voltage increases from +4 to +10 V. The capture activation energy (or barrier energy E_b) is calculated using Eq. (4) for $V_{GQ} > 4$ V and plotted in Fig. 7(b) (blue squares). The barrier energy monotonically decreases from 325 to 300 meV as expected from the depletion region model.

We can estimate the surface charge concentration at $V_G = 0$ from the barrier height [Eqs. (2) and (3)]. Using a carrier concentration value of 10^{19} cm^{-3} (Table I), the surface charge density at zero gate bias is 3.5×10^{12} cm^{-2}.

III. CONCLUSIONS AND PROSPECTS

In conclusion, we have proposed and successfully implemented the I-DLTS method with gate-voltage pulsing to probe deep electronic states in individual ZnO nanowires. This method offers an effective tool to study energetics of electron trapping in nanowire surface states. As an illustration of the nanowire I-DLTS method, ZnO nanowire field-effect transistors were studied. A variety of deep levels were observed, with both electron-like and hole-like characters. A comparison with the literature showed that levels SE1, SE2, and SE3 are most likely surface trap levels, whereas E4 is a bulk nanowire level related to oxygen vacancies. Different types of I-DLTS measurement setups (emission-mode, capture-mode, and quiescent voltage dependence) were applied to the nanowire FETs. The surface barrier was estimated from the capture-mode I-DLTS to be 0.3–0.4 eV. The hole-like trap levels were discovered to affect all the nanowire FET transients.

I-DLTS in conjunction with sample post-treatment and other characterisation methods can improve understanding of the effect of gas molecule adsorption on the surface electronic structure, passivation effects in core-shell nanowires, mechanisms of water splitting on the surface of nanostructures, and incorporation of dopants in the nanowires. Numerical models may be refined to include tunnelling effects, chemical structure, and band gap tail traps. Development of a more sophisticated analysis of the quiescent gate-voltage sweeping technique on wrap-gate FETs may give information on the spatial location of defect states in nanowires with a non-uniform composition (such as axial and core-shell nanowires). Information inferred

using this method can help research into better chemical nanowire-based sensors, photodiodes, memory devices, and stable transistors. Although further development is still necessary, I-DLTS has the potential to become a versatile method for nanowire trap state analysis.

SUPPLEMENTARY MATERIAL

See supplementary material for the derivation of the equation for the current through the nanowire FET, I-DLTS peak magnitude and I-DLTS spectra, and Arrhenius plots of all the studied nanowires.

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