

Gettering in silicon photovoltaics: A review

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ABSTRACT

A key efficiency-limiting factor in silicon-based photovoltaic (PV) devices is the quality of the silicon material itself. With evolving cell architectures that better address other efficiency-loss channels in the device, the final device efficiency becomes increasingly sensitive to the contaminants in the silicon wafer bulk. However, due to cost constraints, silicon materials for PV are inherently less pure and further contamination during device fabrication is commonly found, especially in mass production environments. Metallic impurities are ubiquitous and abundant, and they are strong efficiency-loss channels in the device if not removed. Gettering is the process of removing metallic impurities to a less harmful region of the device, and is therefore an essential aspect of the cell fabrication process. This article presents an up-to-date review of the gettering techniques and processes in silicon solar cells, providing a complete picture of the possible gettering sinks and routes in various cell architectures. The article starts by explaining the common nomenclatures in gettering and summarising recent updates to the solubility and diffusivity data of the common 3d transition metals in silicon. Then the three-step gettering process (release, diffusion, capture) is explained, and its implications for solar-grade cast-grown silicon (in terms of release) and various cell architectures (in terms of diffusion) are discussed. The main focus of the article is to summarise and review the various capture approaches in the context of silicon PV. These include phosphorus diffusion, boron diffusion, selective doping via ion implantation, state-of-the-art polycrystalline-silicon/oxide passivating contact structures, dielectric films (silicon nitride and aluminium oxide), aluminium alloying, surface damaged regions including black silicon, and internal gettering in cast-grown silicon by existing crystallographic defects. Their gettering effects, current understanding of the gettering mechanisms, modelling, improvement strategies, implementation in processing and potential impacts on cell performance are reviewed.

1. Introduction

Silicon (Si) wafer-based solar cells currently account for about 95% of the photovoltaic (PV) production [1] and remain as one of the most crucial technologies in renewable energy. Over the last four decades, solar PV systems have seen a staggering cost reduction due to much reduced manufacturing costs and higher device efficiencies. The silicon wafer substrate constitutes a considerable fraction of the total cost, and its material quality is one of the key factors that determine the overall device efficiency. As other major recombination channels in silicon solar cells become better suppressed through evolving cell architectures [from aluminium back surface field (Al-BSF), to passivated emitter and rear contact (PERC), and now to passivated contacts], the efficiency of solar cells again becomes increasingly sensitive to the recombination losses in the silicon wafer bulk, as can be seen from the comparable recombination currents associated with the silicon wafer bulk and the state-of-the-art surface passivation schemes [2–4].

Metal impurities are one of the major sources of recombination in the silicon wafer bulk. They are recombination active both as point defects (as interstitial or substitutional atoms, or as metal-acceptor pairs) and as precipitates, reducing the conversion efficiency of solar cells [5–9]. Although p-type silicon substrates are more prone to metal point defects [10], n-type silicon suffers from metal-related efficiency losses as well [11,12]. In addition, many studies have shown that metal decoration of extended defects strongly increases their recombination activity, even at low contamination levels [13–17]. The presence of metal impurities, particularly in the form of precipitates, can in turn promote the growth of extended defects such as stacking faults and dislocations [14,18]. Some shunting sites in silicon solar cells are associated with metal-containing defects [19–21]. Copper (Cu) is also known to cause light-induced degradation in silicon [22].

Due to cost constraints, silicon materials for PV inherently contain a significant amount of metal impurities and defects, and further contamination can occur during the fabrication process as stringent

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clean-room environments cannot always be maintained, or even met, in PV manufacturing facilities. Gettering, the process of removing or relocating impurities to a region in the device where they have a less harmful impact on the overall device performance, is therefore a crucial part of the silicon PV technology. By reducing metal impurities in the silicon wafer bulk, gettering improves the overall cell efficiency.

Gettering is also essential in silicon microelectronic devices, where the purity requirements are even greater, although higher quality silicon materials and cleaner fabrication environments are employed. Research into gettering in silicon microelectronics has spanned for more than half a century. However the gettering techniques can be quite different in silicon PV and microelectronics. This is because in PV the whole silicon wafer bulk is part of the active device region, whereas in microelectronics only a thin surface layer is the active region. Techniques such as internal gettering by silicon oxide precipitates and proximity gettering for slow diffusing metals (by nanocavities from ion implantation or laser, for example), are not applicable in PV. The large silicon wafer bulk also means that more efficient gettering sinks are needed. In addition, the overall process temperatures are generally lower in PV. Cast-grown silicon materials such as multicrystalline silicon (mc-Si) and cast-grown monocrystalline-like silicon (known as cast-mono or quasi-mono), which constituted about 35% of the silicon PV production in 2019 [3], contain a large amount of extended defects and metal impurities that further complicate the gettering process. In addition, there are cost-saving incentives to increase the yield of cast-grown silicon ingots by using materials closer to the edges of the ingots, which contain more contaminants and defects.

Myers et al. [23] reviewed the gettering mechanisms in silicon more than 20 years ago. Claeys and Simoen's book chapter [24] is more updated, however mainly from the microelectronic perspective. Gettering in silicon PV was reviewed by Seibt et al. [25,26] about 10–15 years ago, and since Al-BSF was the predominant cell architecture in industry at the time, strong emphases were given to the phosphorus (P) diffusion and aluminium (Al) gettering techniques. Since then rapid progress has been made in developing and demonstrating alternative cell architectures both in industry and in research, as well as progress in understanding and identifying gettering mechanisms and sinks in silicon solar cells. A very brief overview can be found in Yakimov's recent book chapter [27], however too brief to cover the full progress in the field.

This article aims to provide a comprehensive and up-to-date review of the gettering techniques that are relevant to today's silicon PV technology. Topics that have already been covered in previous review articles will only be briefly mentioned and included here in order to provide a complete picture. Fresh insights into the gettering mechanisms, new gettering techniques that are associated with evolving cell architectures and features, updated modelling approaches, and strategies to improve the gettering efficiency in the context of silicon PV will be reviewed and discussed. Updates on the solubility and diffusivity data of 3d transition metals in silicon, mostly from the last two decades, will be summarised. Note that this article will only address gettering on the wafer level, that is, contamination reduction during the ingot growth process will not be covered.

This review article starts by explaining the common nomenclatures in gettering and listing recent updates on metal diffusivity and solubility data. We then proceed to describing each step in a gettering process: release, diffusion, and capture, with the focus on the capture approaches that are relevant to silicon PV. For each capture approach, current understanding of the gettering mechanism(s), effectiveness, and incorporation in solar cell fabrication processes will be summarised and discussed.

2. Gettering nomenclatures, and updates on metal solubility and diffusivity

2.1. Nomenclatures

Based on the mechanisms, gettering is generally categorised as relaxation, segregation, or injection gettering [28]. Injection gettering is only for the special case of phosphorus diffusion gettering, which will be addressed later in Sect 4.1.2.1. Note that these gettering mechanisms are not mutually exclusive, and a gettering process may involve several mechanisms in parallel.

Relaxation gettering is a process where supersaturated metals relax back to their respective solubility limits (i.e. maximum equilibrium concentrations) in silicon, through precipitation. The precipitation sites may be homogeneous or heterogeneous in the host material. Silicon oxide precipitates and structural defects (e.g. dislocations, grain boundaries, surfaces) [23] are common heterogeneous precipitation sites in silicon as they offer a high precipitation site density to promote nucleation and fast precipitation rates.

Segregation gettering, on the other hand, is driven by an enhanced solubility of metals in the capture region, and is therefore not limited by the solid solubility limit of metals in silicon. Segregation gettering is thus possible at high processing temperatures where impurities are very mobile, whereas the high impurity solubility at high temperatures hinders the onset and efficiency of relaxation gettering. The ratio of the solubility limits in the capture region and in silicon is defined as the segregation coefficient. Examples of segregation capture sites include heavily doped silicon, an alloyed Al layer, strain field near dislocations and so on [14,23], as will be detailed later in Sect 4. Note that, different to relaxation gettering which specifically refers to the precipitation mechanism, there are different types of reactions underlying the apparent enhancement of the impurity solubility in the capture region, which are all categorised as segregation gettering.

Depending on the location of the capture sites relative to the silicon substrate, gettering is also classified as internal (or intrinsic) and external (or extrinsic) gettering. There is also proximity gettering in microelectronics, but it is rarely used in PV applications. Gettering by oxide precipitates in the bulk of Czochralski (Cz) silicon, or by extended defects such as dislocations and grain boundaries within mc-Si and cast-mono Si wafer bulk, are examples of internal gettering. External gettering refers to a process where capture sites are either created external to the silicon wafer substrate (e.g. thin films deposited on silicon surfaces), or in the near-surface region of silicon wafers (e.g. dopant diffusion or implantation, Al alloying, surface damage and so on).

2.2. Updates on metal solubility and diffusivity data

All three steps in a gettering process (release, diffusion and capture) heavily depend on the metal solubility and diffusivity characteristics. In crystalline silicon, the solid solubility and diffusivity data of 3d transition metals are well documented in the literature, see, for example, reviews by Graff [5], Weber [29], and Seibt and Kveder [26] (and references therein). Readers are referred to these references for details. Some updates to the widely used references [5,29] are listed below.

Realising the significant impact of ion pairing on the effective (i.e. as-measured) diffusivity of Cu in silicon, the Cu diffusivity in intrinsic silicon was derived by Istratov et al. [30]. The effective diffusivity, which takes into account the trapping of Cu^{+} by acceptors such as boron (B) atoms, can then be modelled [30].

The diffusivity of nickel (Ni) in silicon was revised by Lindroos et al., and data in the temperature range of 665–885 °C were reported [31]. High quality float-zone silicon (FZ-Si) and a very fast cooling rate were used to minimise Ni precipitation. The new activation energy is close to the theoretical prediction from first-principles calculations [31]. Further experimental results on the solubility of Ni in silicon [32] are consistent

with the literature data, confirming the widely used Ni solubility expression from Weber's review [29].

Solubility and diffusivity data of iron (Fe) in silicon were extensively reviewed by Istratov et al. [33]. Generalised expressions were derived by consolidating numerous data in the literature, for Fe solubility in intrinsic silicon at 800–1200 °C, and for Fe diffusivity at 0–1265 °C for both neutral and ionised interstitial Fe (Fe_i^0 and Fe_i^+), although there is limited diffusivity data in the intermediate temperature range of 250–800 °C [33]. Murphy and Falster later expanded the Fe solubility data to 600–800 °C [34,35]. It was reported that the thermal history and the presence (or absence) of surface Fe silicides affect the final steady-state Fe_i concentration, which was speculated to be caused by the formation of different phases of Fe silicides [35]. Murphy and Falster also deduced the Fe diffusivity at 500–700 °C, and the data were found to agree with the generalised Fe diffusivity expression in Istratov et al. [33] within the uncertainty range [35].

From analysing the association time constant of the manganese–boron (Mn–B) pair formation in silicon at 70–120 °C, diffusivity of manganese (Mn) in Si was extracted in this temperature range by Roth et al. [36]. The reported diffusivity is only slightly faster than the literature data in a similar temperature range [36].

3. A getterting process

In general, getterting can be considered as a three-step process: release, diffusion, and capture, as shown by the schematic in Fig. 1 [37]. If not already in a dissolved and mobile state, metallic impurities need to be first released from their metal-silicide precipitates and/or metal-containing clusters [38]. Such mobile metals can then diffuse to getterting regions and become captured and trapped by the getterting sites.

3.1. Release

The release process is most relevant for the cast-grown silicon materials in PV, where only a small fraction of the total metal concentrations are present in the form of dissolved, mobile metals in the as-grown state, as shown in Refs. [39,40] for conventional mc-Si materials for PV. This is also the case for the more recently developed high-performance mc-Si and cast-mono silicon materials, where the as-grown dissolved metal concentrations, such as interstitial Fe and chromium (Cr), are only a fraction of the getterted metal concentrations, indicating the predominance of metal precipitates in such materials [41,42]. The majority of the metals exist in the form of metal-silicide precipitates and metal-rich clusters, often attached to extended defects [38,43,44]. Metal-silicide precipitates come from impurity precipitation during ingot cooling, and likely account for the majority of the precipitates in mc-Si; while larger metal-rich clusters, often oxidised and/or containing multiple

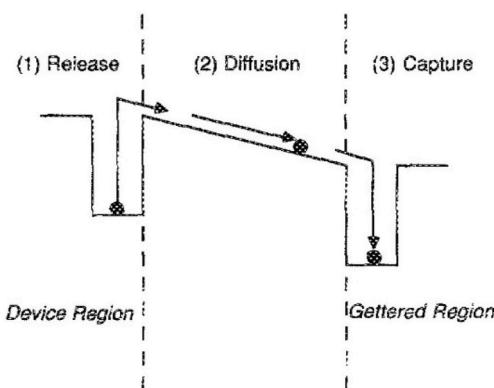


Fig. 1. A schematic of the concept of a getterting process: release, diffusion and capture. Reprinted from Ref. [37], with the permission of AIP Publishing.

metals, are suspected to be inclusions from contamination sources (e.g. crucible and crucible lining, feedstock) that were initially not fully dissolved during ingot growth [38,43]. Cz-Si materials may also contain traces of metal precipitates [37], though a much smaller concentration is expected as they generally have high bulk carrier lifetimes. No direct quantification of the metals in state-of-the-art Cz-Si in PV is available thus far.

Although metal precipitates are generally less harmful than dissolved point defects on a per-atom basis due to their clustering nature, they are still strong recombination centres in silicon [7,45–48]. Moreover, precipitate dissolution can happen during subsequent cell processes at raised temperatures, acting as an internal contamination source [49–51].

3.1.1. Model precipitate dissolution

In principle, dissolution of metal precipitates can start when the solubility limit of a given metal is higher than its actual concentration of dissolved atoms in silicon. For a diffusion-limited dissolution process, the rate of dissolution can be modelled by Ham's precipitation model in a reverse direction of reaction [52]:

$$\frac{dC}{dt} = 4\pi nrD \times (C_{eq} - C) \quad (3.1)$$

where C is the impurity concentration, C_{eq} is the equilibrium solubility limit and is a function of the precipitate properties as will be discussed below, n is the precipitate density, r is the radius of the precipitates, and D is the diffusivity of the metal impurity in silicon.

However, similar to precipitation which becomes diffusion-limited only under very high impurity supersaturation (C/C_{eq}) [53–55], Ham's model is only valid when the driving force for dissolution is so high that the process is only limited by impurities diffusing away from the dissolution site. By analogy with precipitation, the chemical driving force of dissolution is related to the ratio of solubility limit and concentration by [53].

$$\Delta f_{chem} = k_B T \ln \left(\frac{C_{eq}}{C} \right) \quad (3.2)$$

where k_B is Boltzmann constant and T is absolute temperature.

In addition to impurity concentration, there are a number of other factors affecting the dissolution behaviour of metal-containing precipitates. Firstly, precipitate size is known to affect its dissolution rate. For instance, Ostwald ripening indicates that small precipitates are preferentially dissolved and redeposited onto larger precipitates. Secondly, a binding energy may exist between getterted impurities and the getterting sites. Zhang et al. reported an activation energy of (1.47 ± 0.10) eV for the dissolution of Fe precipitates getterted at the intentionally introduced oxide precipitates in p-type Cz-Si [56], which is much higher than the diffusion energy barrier of (0.67 ± 0.02) eV for Fe in Si [33]. Thirdly, the binding energy may vary for different getterting sites. For instance, different dissolution rates of metal impurities have also been reported for oxide precipitates that were grown differently, i.e. getterting sites with different properties, which may relate to the strain field and defects around the oxide precipitates [57–59]. Lastly, the composition of the precipitates and clusters affects their dissolution. For example, Buonassisi et al. found that Cu-oxide and Cu-silicate clusters are much more difficult to dissolve than Cu-silicide [60].

A more complete model was proposed by Haarahiltunen et al. that simulates the evolution of metal precipitate growth and dissolution at heterogeneous getterting sites in silicon [61–63]. The model takes into account the nucleation process in precipitation, and is thus valid for any supersaturation ratio. The effect of precipitate size is considered by implementing size-dependent growth, dissolution, and capture radii of precipitates. The interaction of metal precipitates with getterting sites, which results in an apparent change of local solubility, is modelled by a fitting parameter.

Haarahiltunen's model was first applied to the internal gettering of Fe by oxide precipitates in Cz-Si [61,62], and later extended to gettering of Fe by extended defects in mc-Si [63], damage in boron [64,65] and phosphorus [21] ion implanted regions, and surface precipitation in heavily boron doped Si [66]. Zhang et al.'s experimental data of Fe precipitate dissolution from oxide precipitates [56] could be simulated using Haarahiltunen et al.'s model, without the need to explicitly include a binding energy between precipitates and gettering sites [62]. The same model concept has also been used by Schön et al. to simulate 2-dimensional distributions of Fe and Cr in mc-Si [67–69]. A comparison of the different models for simulating the evolution of Fe impurities during cell fabrication can be found in Ref. [70].

3.1.2. Precipitate dissolution in cast-grown silicon

As can be inferred from the discussion above, dissolution of metal precipitates in cast-grown silicon materials is very much dependent on the initial material quality, in terms of metal concentration, distribution, type, precipitate size and type, interaction with different gettering sites (e.g. extended defects), and so on. Dissolution strategies therefore vary along a cast-grown ingot, which is well known to have significantly varying concentrations and distributions of impurities and defects [39, 40,44].

In conventional mc-Si materials, the total (precipitated and dissolved) concentrations of Fe, Cu, Ni, Cr, and cobalt (Co) were reported to be generally on the order of 10^{13} cm^{-3} and 10^{14} cm^{-3} , with a few exceptions at the top and middle of the ingot [39,40]. The concentrations of Fe and Cr, and Co in some cases, are well above their solubility limits at 800°C . Coupled with the moderate diffusivities of Fe and Cr in Si, this indicates incomplete dissolution of these metal precipitates during a typical phosphorus diffusion process. The metal concentrations in Refs. [39,40] were measured by neutron activation analysis (NAA), and a later study pointed out the susceptibility of this technique to high surface metal contaminations [71]. Nevertheless, incomplete precipitate dissolution after a standard phosphorus diffusion process is often suggested from experimental and simulation studies on mc-Si wafers from the heavily contaminated regions of the ingot [69,72,73]. Generally, a complete dissolution of metal precipitates requires high temperatures and/or long durations, which is not practical in PV manufacturing due to cost constraints.

Newer generations of the mc-Si materials, as well as cast-mono silicon, generally have reduced total metal concentrations [41,42,44,74]. Therefore a more complete dissolution of metal precipitates is expected, while this again depends on the exact materials.

3.2. Diffusion

Once released, dissolved and mobile metal atoms can move around the silicon lattice in a random fashion. As some reach gettering sites and become trapped, a concentration gradient forms, and the net effect is a flow of impurities diffusing towards the gettering sites. Note that the release, diffusion and capture processes occur simultaneously.

The diffusion length L is related to the impurity diffusion coefficient, or diffusivity, D and diffusion time t via $L = \sqrt{Dt}$. For scenarios where the impurity concentration gradient is the driving force for diffusion, the change in concentration can be described by Fick's diffusion law, which in one-dimension is:

$$\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \quad (3.3)$$

Analytical solutions to Eqn (3.3) exist for certain boundary conditions, for instance, if an infinite gettering rate is assumed at the boundary. However, in most gettering scenarios, a finite gettering capacity is in place, and thus a numerical solution to (3.3) may be necessary. Hieslmair et al. outlined some numerical algorithms to solve Fick's diffusion law in the context of gettering [75].

In silicon solar cells where external gettering to regions near the wafer surfaces is a more relevant approach, the diffusion of metals through the silicon wafer bulk to reach the surface gettering sinks may in some cases limit the overall gettering effect. Fig. 2 simulates the amount of time needed to reduce the initial dissolved metal concentration by two orders of magnitude, assuming infinite surface gettering sinks, such that the process is only limited by the diffusion of metals in silicon. A typical silicon wafer thickness of $160 \mu\text{m}$ is assumed. The model in Ref. [76] was used for the simulation. The strong interaction of Cu with B dopants, which reduces the effective diffusivity of Cu, is considered [30], assuming 10^{16} cm^{-3} B doping in silicon (a base resistivity of $1.5 \Omega\text{cm}$). For other metals, the diffusivity data in intrinsic silicon are used [5,31,33,36,77].

In solar cell architectures where a high temperature step (above 800°C for tens of minutes) is required to form the heavily doped regions, the diffusion of common metallic contaminants is generally *not* the rate-limiting factor for an external gettering process, as can be seen in Fig. 2. On the other hand, the process becomes diffusion-limited during contact firing, the process of forming metal contacts through a rapid (a few seconds) anneal at temperatures above 750°C .

However, silicon heterojunction (commonly referred to as SHJ, HJT, or HIT) and novel metal compound based passivating contact (also known as dopant free passivating contact) solar cells are entirely processed at low temperatures (below $200\text{--}300^\circ\text{C}$), in which case the diffusion of metals becomes a limiting factor for external gettering, except for very fast diffusing metals such as Cu, Ni, and to some extent Co (see Fig. 2). However, Cu, Ni, and Co tend to form precipitates in silicon as their solubility limits decrease at lower temperatures, and these precipitates are recombination active [5]. External gettering sites in these low-temperature cell architectures have not been studied either. Therefore, high quality silicon substrates have been commonly used in these low-temperature cell structures. Lower quality solar-grade substrates are possible with a pre-treatment of gettering, hydrogenation, and *tabula rasa* (to dissolve grown-in oxide precipitate nuclei in Cz-Si) in some instances [78–80].

3.3. Capture

Capture sites and mechanisms are the main focus of this review article, and are detailed in Sect 4 below. Only those that are currently relevant for silicon PV are included. A schematic summary is shown in Fig. 3.

Unlike silicon microelectronic devices where most of the gettering sinks are located away from the electrically active front side of the wafers, the gettering sinks in solar cells may be on the front, back, or even both sides of the wafers, depending on the applied cell architecture, substrate type (p or n), and processing sequence (e.g. selective etching after doping). The gettering sinks may be present as full-area or localised.

It is worth noting that most of the recent gettering studies in PV used Fe as a tracer impurity in silicon, due to its easy and sensitive detection method in silicon [81,82], omnipresence in silicon materials and in equipment [83], and ease of sample preparations. However, its interaction with capture sites may not represent other metals, and its unique combination of solubility and diffusivity in silicon dictates its "release" and "diffusion" behaviours. Fe has a moderately high solubility and diffusivity in silicon [5].

4. Capture approaches

4.1. Highly phosphorus-doped silicon

Heavy phosphorus doping is commonly applied to form the n+ regions on the surface of p-type silicon wafers, typically from phosphorus diffusion at relatively high temperatures (above 800°C). Therefore gettering by highly P-doped silicon is naturally embedded in most cell

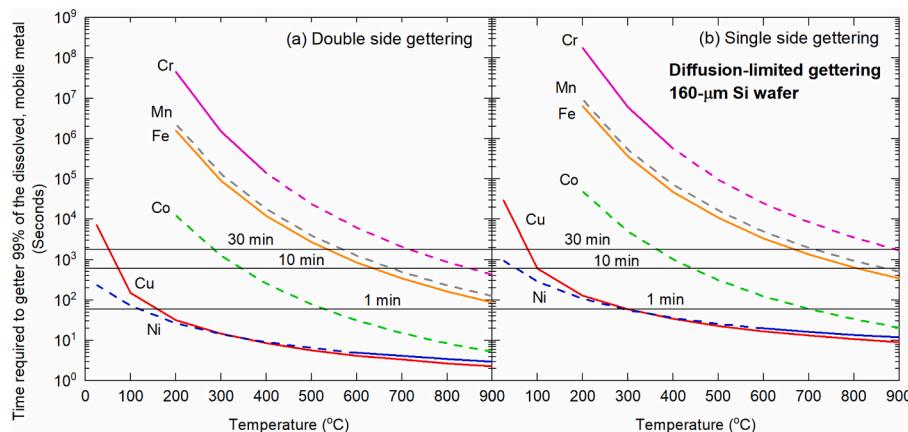


Fig. 2. Simulations of an external gettering process where gettering sinks are present on (a) both sides, or (b) one side. The gettering sinks are assumed to have an infinite gettering capacity such that the process is entirely limited by the diffusion of metals in the silicon wafer bulk (for a wafer thickness of 160 μm) to reach the surface gettering sinks. The time taken to getter 99% of the dissolved, mobile metal concentrations is simulated for a range of temperatures. The dashed lines were simulated based on an extrapolation of the available metal diffusivity data in the literature, and the solid lines were from diffusivity parameters that showed good fitting to the experimental data in the investigated temperature range (25–900 °C). The diffusivity of Cu considers the interaction of Cu with B [30], assuming a B doping concentration of 10^{16} cm^{-3} . The data of Ni [31], Co [5], Fe [33], Mn [36], and Cr [77] were used. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

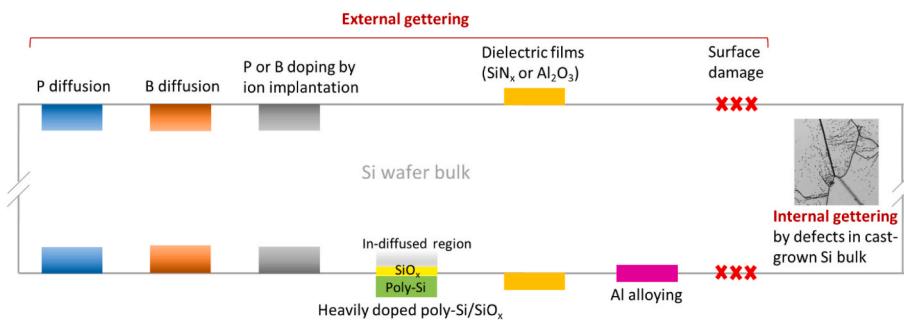


Fig. 3. A schematic of the currently relevant gettering sinks in silicon PV (not to scale). Depending on the cell architecture, the external gettering sinks can be present on the front, back, or even both sides of the wafers. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

architectures, such as the mass-produced Al-BSF and p-type PERC. **Phosphorus diffusion gettering (PDG) is the most widely used and studied gettering technique in silicon PV.** The PDG process is highly efficient, due to its combination of high capture efficiency (i.e. segregation coefficient) and high metal mobility at process conditions (temperature and time). As carrier recombination in the heavily P-doped silicon is largely dominated by Auger recombination, aggregation of gettered metal impurities in the phosphorus doped layers is unlikely to considerably degrade the p-n junction quality [84].

Despite its extensive usage, the exact mechanisms of PDG, or at least the predominant mechanism(s), remain a debated topic. A number of mechanisms have been proposed in the past several decades, as briefly summarised below, categorised as those related to high P doping (4.1.1) and those related to the diffusion process from surface P sources (4.1.2). Mechanisms 4.1.1.1, 4.1.1.2, and 4.1.2.1 have been reviewed in more details elsewhere [23,26].

4.1.1. Mechanisms related to high P doping in Si

4.1.1.1. Fermi level effect and ion pairing. A Fermi level shift by heavy doping and pairing of ionised metals with dopants contribute to an increased solubility limit of metals in heavily P-doped Si [85]. This is easy to understand in the case of metals with acceptor levels, as negatively charged metals pair with positively charged substitutional P. For metals with donor levels, such as Fe, Co, Mn, Cu, ion pairing was explained by an increased substitutional fraction of the metals which become negatively charged [85,86]. Vacancies in heavily P-doped Si [87] were proposed to assist in this transition of metals from interstitial to substitutional sites [85].

First-principles calculations predict a strong pairing reaction between Fe and vacancies [88]. Emission channelling patterns of Fe confirmed that Fe predominantly resides at substitutional sites in n+ Si [89]. The existence of Fe-P complexes in heavily P-doped Si was detected by electron-spin resonance (ESR) [90]. Further deep-level transient spectroscopy (DLTS) analysis found that vacancies and/or vacancy-phosphorus pairs likely assist in the Fe-P formation process [91]. These results indicate the likelihood of M_S-P_S (substitutional metal pairing with substitutional phosphorus) complex formation in heavily P-doped Si, at least for Fe.

However, as summarised in Myers et al. [23], the effect of Fermi level and ion pairing is limited and cannot fully explain the excellent gettering efficacy of PDG. Additional gettering mechanisms are likely present.

4.1.1.2. Metal-silicide formation at SiP precipitates. In the near-surface region where the phosphorus concentration often far exceeds its solubility limit in silicon at processing temperatures, some phosphorus atoms can precipitate to form SiP precipitates. This coincides with the so-called “dead layer”, as the region is highly recombination active.

SiP precipitates at the interface of phosphosilicate glass (PSG) and silicon were observed by high-resolution transmission electron microscopy (TEM) [92]. Ni [92], Fe [93] and platinum (Pt) [94,95] silicides have been identified close to the SiP precipitates. Metal-silicide growth in the close vicinity of SiP precipitates is believed to be associated with the injection of silicon self-interstitials during the formation of SiP precipitates [92,95,96].

4.1.1.3. Binding with P₄V clusters. More recently, *ab initio* calculations

based on density functional theory (DFT) predicted that, as P concentration exceeds its solubility limit in Si, neutral P_4V clusters are favourably formed [97]. This P_4V cluster was predicted to bind strongly with Fe, Cu, Cr, molybdenum (Mo), Ni, Ti and tungsten (W), with the metal occupying the vacancy site. Calculations also indicated that the energy gain from forming M- P_4V (where M denotes neutral interstitial metal) is higher than the formation of M- P_1V (effectively M_s-P_s) [97]. This suggests that in the presence of both electrically active P_s atoms and P_4V clusters, neutral interstitial metals in n+ Si preferentially bind with P_4V clusters. This model was used to explain the near-surface non-linear relationship between gettered metal and P profiles in secondary ion mass spectrometry (SIMS) measurements, where the concentration of gettered Fe drops much faster as a function of depth below the surface than the P concentration, as demonstrated in Fig. 4.

It should be stressed that the proposed formation of M- P_4V complexes *does not invalidate* the gettering channels of M_s-P_s ion pairing or gettering by SiP precipitates. As shown in Fig. 5, P_4V clusters only become dominant when the P concentration is approaching its solubility limit. At higher P concentrations where P atoms become supersaturated, SiP precipitates start to form, as evidenced by the TEM images in Ref. [99]. The proposed P_4V clusters, together with SiP precipitates, may explain the strong gettering effects of electrically inactive phosphorus [100].

4.1.2. Mechanisms related to P diffusion process

4.1.2.1. Injection gettering. It is well established that the in-diffusion of P into silicon experiences a transition from a vacancy-mediated diffusion mechanism to a self-interstitial one, which contributes to the kink-and-tail characteristics of typical P concentration profiles (see, e.g. Refs. [87, 101]). The injection of silicon self-interstitials from P diffusion is believed to enhance the gettering efficacy for substitutional metals, referred to as *injection gettering* [102–104].

For substitutional metals, such as gold (Au) and Pt, an injection of self-interstitials “kick-out” the atoms from substitutional into interstitial sites, making the metals more mobile. Moreover, as self-interstitials diffuse to the surface as a result of its concentration gradient, substitutional metals are effectively coupled with self-interstitials and diffuse to the surface due to the kick-out mechanism [105].

4.1.2.2. Immobile oxygen. In the last decade, Syre et al. [106] and Schön

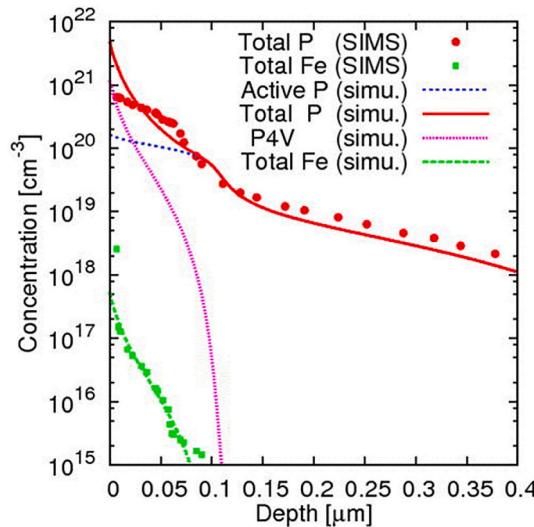


Fig. 4. Experimental (SIMS, from Ref. [98]) and simulated Fe and P profiles in silicon after phosphorus diffusion and annealing. Reprinted from Ref. [97], with the permission of AIP Publishing. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

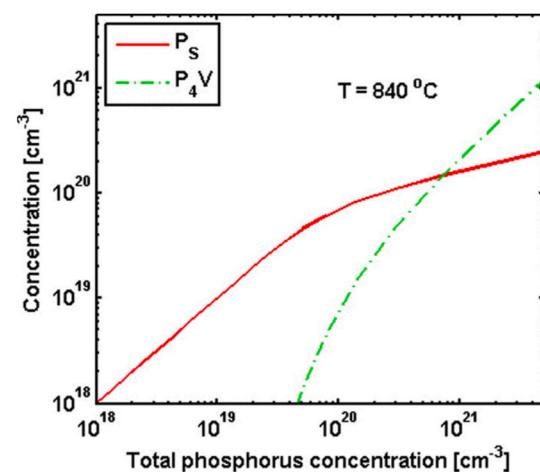


Fig. 5. Equilibrium concentrations of the electrically active substitutional phosphorus (P_s) atoms and electrically inactive P_4V clusters at 840 °C, as a function of the total phosphorus concentration. The concentrations of P_nV with $n \leq 3$ are negligible. Reprinted from Ref. [97], with the permission of AIP Publishing.

et al. [107] proposed pairing with immobile oxygen (O) complexes, sourced from the PSG and the interfacial oxide, as one of the additional mechanisms underlying PDG. It is worth emphasising that this proposed mechanism has only been shown for Fe so far.

In Syre et al. [106], SIMS measured Fe profiles showed no dependence on the depth of the P-doped regions. O profiles, on the other hand, were found to follow closely the Fe profiles. The authors therefore proposed a possible formation of Fe–O or Fe–O–V complexes. Although the proposed complex compositions do not contain P due to a lack of correlation between the P and Fe profiles, results showed that without P, no gettering action takes place. The involvement of P was speculated to be associated with the injection of vacancies during P diffusion in heavily doped regions [87]. These vacancies are believed to promote the formation of oxide precipitates, a mechanism that is similar to the generation of oxide precipitates in Cz-Si by engineering vacancy profiles [108,109]. Oxide precipitates then act as effective capture sites for Fe.

Schön et al. [107] took a similar experimental approach, and based on the SIMS profiles of the total O and P concentrations, as well as electrically active substitutional P profiles by electrochemical capacitance-voltage (ECV) measurements, they fitted the SIMS measured Fe profiles by simulated profiles of Fe–O, Fe– P_s and Fe– P_4V complexes. The Fe– P_s and Fe– P_4V profiles reflect the interactions of Fe

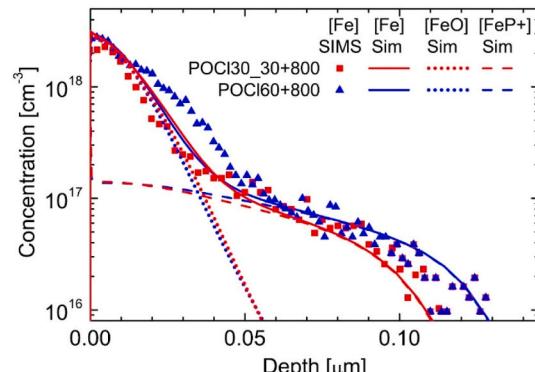


Fig. 6. Experimental (SIMS) and simulated Fe profiles after phosphorus diffusion. The dotted and dashed lines are simulations assuming Fe gettering solely by oxygen complexes (Fe–O), or electrically active phosphorus (Fe– P^+), respectively. The solid lines are simulations combining the two. Reprinted from Ref. [107], with the permission of AIP Publishing.

with electrically *active* and *inactive* P atoms, respectively. An example of the fitting is shown in Fig. 6. It was found that only a combination of Fe-O and Fe_s-P_s, or Fe-O and Fe-P₄V, can explain the measured Fe profiles, with Fe-O being the major contributor, although Fe-O alone cannot explain the SIMS Fe profiles. Oxygen in the heavily P-doped region was found to be largely immobile from analysing the SIMS O profiles. Gettering of Fe by immobile O complexes was therefore proposed as an additional mechanism for PDG. The exact composition of this immobile oxygen complex, however, could not be determined in Ref. [107].

In summary, the entire PDG process likely involves several mechanisms concurrently. The gettering efficiency and predominant mechanisms do depend on the diffusion process conditions, such as the electrically active and inactive P concentrations, possible formation of SiP precipitates, in-diffusion and formation of oxygen complexes, generation of silicon self-interstitials and vacancies and so on.

4.1.3. Modelling PDG

Modelling the complex process of PDG has been a subject of research for decades. In principle, an accurate model relies on an accurate understanding of the mechanisms at play, which to some extent is still lacking. Kveder et al. [110], Schröter et al. [111], and Seibt et al. [25], for example, have reported detailed modelling of PDG based on the understandings in the early 2000s. These models included the effects of Fermi level and metal-phosphorus ion pairing, and injection gettering. Metal-silicide formation at SiP precipitates, however, was not included. This process is less relevant for diffusion conditions that do not generate a large concentration of electrically *inactive* P. Gettering by SiP precipitates is also much more difficult to quantify, given the complexities involved in quantifying P- and metal-silicide precipitate formations.

4.1.3.1. Fe gettering as an example. In this section, we will summarise recent progresses on modelling Fe gettering by PDG. A semi-empirical model for the segregation coefficient of Fe in P-doped Si was proposed by Haarahiltunen et al. in 2009 [112]. As injection gettering is less important for interstitial metals such as Fe, the model is based on the assumption that the predominant gettering mechanism is ion pairing of negatively charged substitutional Fe with positively charged substitutional P. The pairing rate was used as a fitting parameter to fit experimental PDG results. The model was later updated by Talvitie et al. by supplementing more experimental data [98]. It was later pointed out that the segregation coefficients reported in Ref. [98] were possibly overestimated by a factor of 1.5, due to the inhomogeneous Fe distribution across the wafer thickness that resulted in a systematic overestimation [107].

A similar semi-empirical model was reported by Schön et al. [113], which is based on the same Fe_s-P_s pairing assumption but replaces singly

negatively charged Fe_s by a doubly negative charge.

In light of the more recently proposed gettering mechanisms involving possible contributions from immobile oxygen complexes and electrically inactive P₄V clusters, Schön et al. [107] proposed new semi-empirical models by fitting the experimental data by a combination of Fe-O and Fe_s-P_s, or Fe-O and Fe-P₄V. The fitting for Fe_s-P_s was based on the same model [113] but with slightly different fitting parameters. The semi-empirical model for Fe-P₄V was based on a theoretically calculated binding energy from Chen et al. [97], with the pre-factor being a fitting parameter.

Fig. 7 plots the segregation coefficients (k_{seg}) for Fe in the near-surface region of the silicon wafers after PDG, from the various semi-empirical models discussed above. Some large variations in k_{seg} can be observed in Fig. 7(a), highlighting the complexities in modelling PDG if the underlying main mechanisms are not accurately identified. In addition, a number of parameters in those models are unknown and are lumped together as fitting parameters to fit the limited experimental data at hand. Of course there are also uncertainties concerning the experimental data of SIMS and dilute Fe concentrations in silicon. Therefore these *semi-empirical* models may not accurately predict PDG results if there are variations in the exact diffusion processes (which are very common), as shown in, e.g. Ref. [114]. Uncertainties involving oxygen and P₄V clusters are even greater. Nevertheless, the trends are clear from Fig. 7 that the capture efficiency (i.e. k_{seg}) increases as temperature decreases, and it increases as P (electrically active and inactive) and immobile O concentrations increase.

4.1.4. Gettering by P ion implantation and annealing

An alternative approach to dope the silicon surface regions for junction formation or back-surface field is via ion implantation and annealing. The process offers better control of the doping position, dose and profile, and can potentially simplify the process flow, especially in the case of selective doping (e.g. IBC cells, selective emitters, and codiffusion of opposite dopants on the front and rear of a wafer).

The dopant ion implantation discussed here is to be distinguished from the gettering by intentionally induced ion implantation defects, such as cavities and lattice damage, in microelectronic applications (see, e.g. Refs. [23,24] for a review). The main purpose of dopant ion implantation in Si PV is to form high-quality junctions with minimal recombination, and therefore the process is designed to *minimise* implantation damage by using low-to-moderate implantation energy and subsequently annealing at a relatively high temperature to anneal out the implantation damage. Although, as we will see later, there is still residual damage after annealing, the gettering effectiveness and predominant gettering mechanisms are different from the intentionally induced implantation defects in microelectronic applications.

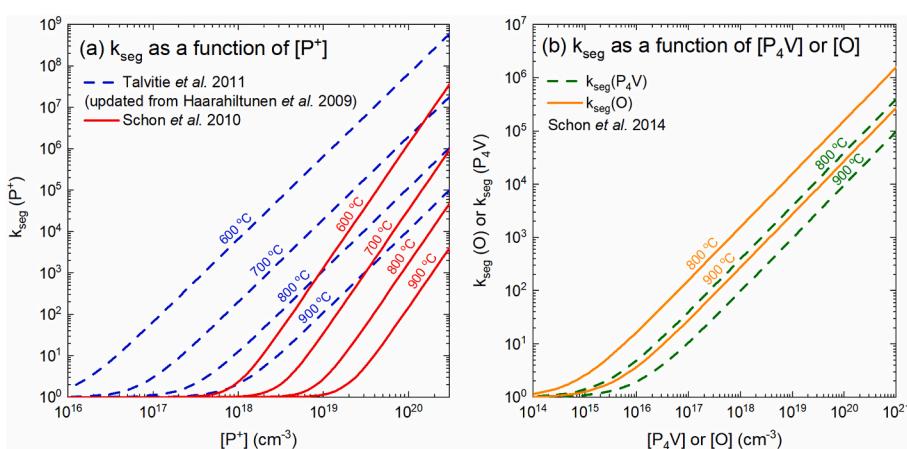


Fig. 7. Segregation coefficients of Fe in PDG as a function of (a) electrically active substitutional P⁺ concentration [98,112,113], and (b) electrically inactive P₄V cluster concentration, or immobile O concentration [107].

4.1.4.1. At processing temperatures. Studies showed that the highly P-doped regions from ion implantation and annealing (generally above 900 °C) have weaker gettering effects compared to thermal diffusion from surface P sources [115,116]. Both experimental [115] and modelling [116] results indicate that the different gettering efficiencies cannot be explained by the total concentration of electrically active phosphorus atoms, i.e. gettering due to Fermi level effect and ion pairing (4.1.1.1).

The difference was attributed to the lack of electrically inactive P in the investigated ion implanted samples [116] (see Fig. 8), as inactive P, in the form of either SiP precipitates (4.1.1.2) or the more recently proposed P₄V clusters (4.1.1.3), are believed to be effective gettering sites for metals. Of course a supersaturation of P can be intentionally created by ion implantation through doping beyond the solubility limit of P in Si, as will be shown later in some of the P-implanted poly-Si/SiO_x examples. In general, for the purpose of forming p-n junctions in c-Si, the P implanted and annealed surface regions do not contain a high concentration of electrically inactive P. The electrically active P atoms in the implanted regions, however, still possess some gettering effects (due to Fermi level effect, 4.1.1.1) as the gettering efficiency was found to correlate to the P implantation dose [115].

In addition, gettering mechanisms that are related the conventional phosphorus diffusion process (4.1.2) may have contributed to the weaker gettering effects from P ion implantation and annealing. PSG was regarded as an infinite source of oxygen during diffusion [107]. The lack of PSG in ion implanted samples may hinder the injection of oxygen and thus affect the gettering efficiency. The silicon self-interstitial and vacancy concentrations and distributions are likely very different in the implanted and diffused samples [117]. This can affect the gettering mechanisms that involve the participation of intrinsic defects, such as injection gettering for substitutional metals (although not in Ref. [116] as only Fe was studied) and the substitutionalisation of interstitial metals for pairing with P_s atoms. Further work is required to address the potential impacts of oxygen and intrinsic defects on the gettering effectiveness of ion implanted phosphorus.

4.1.4.2. Adding a low temperature anneal. Adding an extended low temperature annealing step (620–750 °C) after P ion implantation and high-temperature annealing was found to promote Fe precipitation in the P-implanted regions (i.e. relaxation gettering) [21,116]. Fe precipitates were directly observed by synchrotron-based micro-X-ray fluorescence measurements [21]. The size and distribution of the measured Fe precipitates, as well as the residual bulk Fe concentrations, were shown to be well reproduced by a heterogeneous Fe precipitation model [61,62] (previously detailed in Sect 3.1.1), confirming the predominance of precipitation gettering during low temperature annealing.

Although the formation of Fe precipitates in the heavily doped region is beneficial for reducing the bulk interstitial Fe concentration, the growth of large Fe precipitates (>1 μm) was found to degrade the

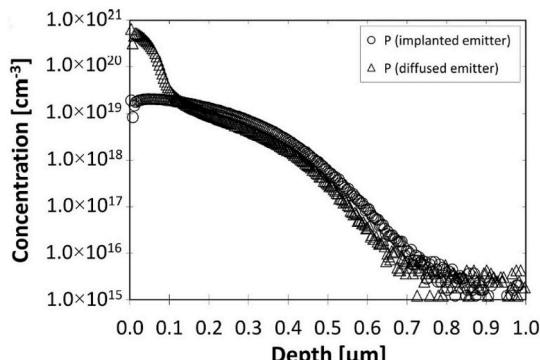


Fig. 8. SIMS total P concentration profiles in P implanted and diffused regions. Reprinted from Ref. [116], with the permission of IEEE.

junction quality by introducing shunting sites [21]. Moreover, prolonged low-temperature annealing also drives Fe precipitation on the other wafer surface and within the silicon wafer bulk for some high Fe samples [116]. Careful design of the gettering process is therefore required to achieve optimal device performance.

4.1.5. Strategies to improve gettering effectiveness

4.1.5.1. Variable temperature gettering. A variable temperature gettering scheme takes advantage of both increased “release” and diffusion at high temperatures and increased “capture” at lower temperatures. As discussed previously in Sect 3.1, cast-grown silicon materials contain a large fraction of metal impurities in the form of precipitates and clusters. To getter precipitated metals effectively and rapidly, Plekhanov et al. proposed the variable temperature gettering approach [118]. At high gettering temperatures, metal precipitates dissolve faster due to the higher solubility limits of metals in Si, and the dissolved metals diffuse faster as well. However, segregation coefficients decrease with increasing temperature (e.g. see Fig. 7). Combined with higher metal solubility limits in the silicon substrate, a higher gettering temperature results in higher residual dissolved metal concentrations. On the other hand, at low gettering temperatures, the dissolution of precipitates becomes slow and metals diffuse slower as well, although lower residual dissolved metal concentrations can be achieved.

It is worth pointing out that the enhanced “capture” at lower temperatures is also beneficial for silicon materials that only contain dissolved metals, to exploit the increased segregation coefficients and decreased metal solubility limits at lower temperatures, leading to lower residual metal concentrations.

The trade-off of a fixed gettering temperature is demonstrated in Fig. 9 [118]. The modelled recombination constant reflects the recombination strength of both dissolved and precipitated Fe in Si, and was simulated for the course of the entire gettering process. The recombination constant initially increases due to the dissolution of precipitates, and finally decreases as dissolved impurities become captured. As shown in Fig. 9, a lower constant gettering temperature results in a lower final recombination strength, at the cost of a prolonged gettering time. A

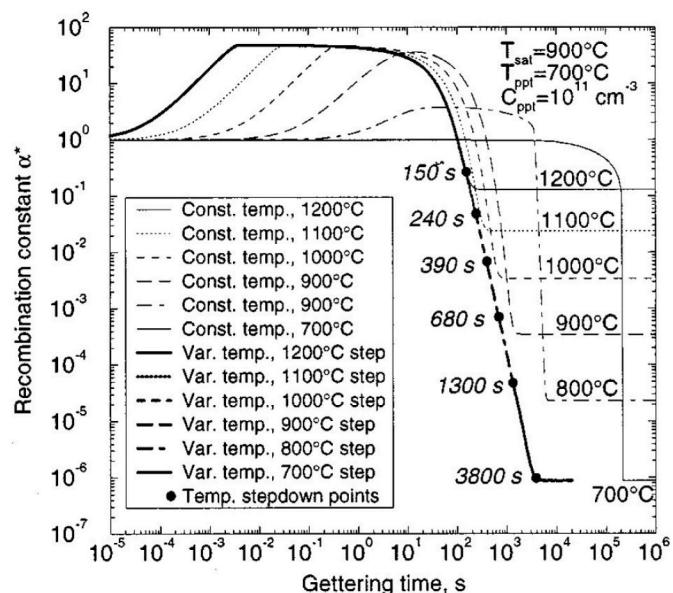


Fig. 9. Simulations of the relative integrated recombination constant of Fe point defects and Fe precipitates as a function of gettering time for different temperature profiles. The light lines are based on constant temperature profiles, and the bold line is from a variable temperature profile where the temperature decreased from 1200 to 700 °C in 100 °C steps, at the indicated stepdown times. Reprinted from Ref. [118], with the permission of AIP Publishing.

variable temperature gettering process, however, results in a much shorter overall gettering time (the scales in Fig. 9 are logarithmic).

Note that the simulation in Fig. 9 is based on Fe and an assumed Fe precipitate density. Obviously the optimum temperature-time profile varies for different metal species and differently contaminated silicon materials in terms of the dissolved and precipitated metal concentrations and their interactions with extended defects. For example, Cu and Ni have high solubilities and diffusivities in silicon, meaning that the “release” process may not require high temperatures and a typical PDG temperature around 800 °C is sufficient in most cases.

Although the model used aluminium-silicon alloying as the surface gettering layer [118], the conclusion is essentially the same for PDG and other capture sites whose segregation coefficient increases with decreasing temperature.

Based on this variable temperature gettering model, a simpler two-step gettering process, which adds a low temperature annealing step (generally below 700 °C for over an hour) after a standard phosphorus diffusion, was proposed and examined in simulation [25] and in experiments [119,120]. Improved gettering effects were demonstrated. The low temperature tail was found to *not* significantly alter the final sheet resistance of the P-doped layers.

Many have reported improved gettering efficiencies by employing a low-temperature tail after a standard P diffusion process, a slow cooling rate (which is effectively a continuous variable temperature gettering process), and/or a high-temperature dissolution step [67,121–124] (the reference list is not exhaustive). Although a low temperature anneal may also promote metal precipitation at structural defects in mc-Si and cast-mono Si, the predominant effect is found to be due to PDG [72,124, 125], as will be detailed later in Sect 4.7.

4.1.5.2. Etch back heavily doped surface layer. In conventional solar cells, surface P doping is high to ensure low contact resistance with screen printed metal contacts. However, this heavily doped layer has a very high recombination activity, and is hence also referred to as the “dead layer”. This “dead layer” presents a trade-off in cell design. However, new generations of screen printed metal contacts no longer require heavy doping to form good metal-silicon contacts, and the industry is moving towards lighter doping [1,126]. Lighter doping, especially the reduction of peak P concentration, can effectively increase cell efficiencies [127].

Heavy P doping and the “dead layer” in the near-surface region are highly efficient in impurity gettering [114]. To exploit this strong gettering effect without compromising final cell efficiency, some have suggested and experimentally implemented a chemical etch-back of the “dead layer” after phosphorus diffusion, either selectively or over the full area [126,128–130].

4.1.5.3. Size of the capture region. As the whole silicon wafer bulk is part of the active device region, the size of the capture region in relation to the bulk volume has to be considered. At steady state, the ratio of the impurity concentration in the gettering region (e.g. P-doped layers) to the gettered region (i.e. silicon wafer bulk) is a constant described by the segregation coefficient. From conservation of mass, it follows that [75, 112].

$$C_i V_w = \int_0^{V_{gett}} k_{seg}(v) C_b dv + (V_w - V_{gett}) C_b \quad (4.1)$$

where C_i is the initial impurity concentration, C_b the bulk impurity concentration after gettering at steady state condition, V_w the whole wafer volume, V_{gett} the phosphorus in-diffused gettering region volume, and k_{seg} is the segregation coefficient as a function of the volume position. For a simplified case where an effective segregation coefficient k_{seg_eff} is assumed to describe average k_{seg} in the gettering region, Eqn (4.1) can be rearranged to,

$$\frac{C_b}{C_i} = \frac{V_w}{V_w + (k_{seg_eff} - 1)V_{gett}} \quad (4.2)$$

Eqn (4.2) clearly shows that an effective gettering process relies on both the segregation coefficient and the volume ratio of the gettering and gettered regions.

For a full-area diffusion, the volume terms in (4.1) and (4.2) can be replaced by the thicknesses of the wafer and the gettering layer. As the capture efficiency (i.e. segregation coefficient) of PDG is relatively large and can be easily enhanced by reducing the processing temperatures (by adding a low temperature tail and a slow cooling rate), varying the thickness of the P-diffused region has not been an important or viable option for improving PDG. Furthermore, the thickness of the heavily doped layers affects final device efficiency and is therefore not easily changeable.

For cell architectures that incorporate localised heavily P-doped regions, commonly known as selective emitters, the volume ratio of the heavily P-doped regions to the silicon wafer bulk can limit the overall gettering effect. In addition, metals now need to diffuse laterally to reach the localised gettering sinks, increasing the effective diffusion length required for the gettering process.

4.2. Highly boron-doped silicon

Heavily boron-doped silicon, commonly from high-temperature boron diffusion, is used for forming front-side p-n junction in n-type silicon substrates, junctions in interdigitated back contact (IBC) cells, or back-surface fields in some p-type cells, for instance. N-type silicon substrates are of great interest to silicon PV as it avoids boron-oxygen related light induced degradations [22] and is more immune to some common metal point defects [10].

4.2.1. Mechanisms

Boron diffusion gettering (BDG) has not been as extensively studied as PDG. In this section we will summarise the current understandings of the BDG mechanisms. The first two mechanisms (4.2.1.1 and 4.2.1.2) have been previously reviewed in detail in Refs. [23,26].

4.2.1.1. Fermi level effect and ion pairing. Similar to highly P-doped Si, heavy boron doping increases the solubility of most transition metals in silicon through the Fermi level effect and ion pairing [23,85,131]. High boron doping shifts the Fermi level towards the valence band edge, and metals that have donor levels in the bandgap become positively charged and pair with negatively charged substitutional boron atoms. Most transition metals have donor levels in the bandgap [5], and thus an enhancement of the solubility in the p+ region is expected. An exception to this is Ni, which showed no enhancement of its solubility in heavily B-doped silicon [32]. It was thus proposed that the donor level of Ni possibly lies close to the valence band edge or within the valence band [32].

Knowing the energy level of the donor state of the metals and the activation energy for the donor-acceptor (i.e. metal-boron) pairing reaction, the enhanced solubility of metals in heavily B-doped Si due to the Fermi level effect and ion pairing can be estimated, as demonstrated in Refs. [23,131] for Fe.

The segregation effect becomes stronger at lower temperatures and higher B doping concentrations. At typical B diffusion temperatures, the gettering strength due to the Fermi level shift and ion pairing mechanism alone is quite moderate (see, for example, [23,131]), especially for Si PV devices where the heavily doped region is much thinner than the bulk substrate. This partly explains the poor gettering effect of typical boron diffusions in Si PV processes. As will be discussed below, other mechanisms that have stronger gettering effects rely on processes that deviate from “standard” boron diffusions used in cell fabrication.

4.2.1.2. Segregation into B–Si precipitates. Upon supersaturation of boron in silicon, B–Si precipitates may form. Different to the formation of metal-silicide precipitates near P–Si precipitates in PDG (Sect 4.1.1.2), metals (Fe, Co, Cu, and Au) were found to segregate into B–Si precipitates [23,132–134]. The B–Si precipitates were found to be nm-sized, granule-shaped, amorphous B-rich particles, with a possible composition of B_3Si [23,132].

Although the initial studies by Myers and co-workers [132–134] used boron ion implantation and annealing to create boron supersaturation and hence the formation of B–Si precipitates, other means to generate boron supersaturation are also possible to induce similar gettering effects. Tomita et al. [135] used highly B-doped silicon layers and reported strong gettering of Fe by electrically inactive B, with an activation energy of 2.1 eV. This is close to the activation energy of 2.27 eV deduced in Myers' work [133]. Vähäniemi et al. [136] later applied low temperature annealing after a typical boron diffusion at 930 °C, and found strong Fe gettering with an activation energy of 2.2 eV, which is again similar to the values reported by Myers et al. [133] and Tomita et al. [135]. The authors therefore attributed it to the same underlying gettering mechanism.

4.2.1.3. Boron-rich layer. During boron diffusion, a boron-rich layer (BRL) is commonly found in between the boron silicate glass (BSG, a mixture of B_2O_3 and SiO_2) and heavily boron-doped Si. This BRL is hydrophilic and insoluble in hydrofluoric (HF) acid, and is identified as a boron-rich silicon boride of possible compositions SiB_6 , SiB_4 , and/or SiB_5 (see, e.g. Refs. [137–139] and references therein). The BRL is formed from a “pile-up” of boron atoms at the silicon surfaces during diffusion, as a result of a higher influx of B from BSG into Si than the rate of B diffusion away from the Si surface into the wafer bulk [137–139].

The boron-rich layers share some similarities with the B–Si precipitates discussed above. They both result from some form of boron supersaturation, and the equilibrium form of SiB_3 (the possible composition of B–Si precipitates [132]) is SiB_6 (the possible composition of BRL [137]) [140].

However, the BRL and B–Si precipitates are different in their distribution and formation. While the B–Si precipitates were found to be nm-sized particles within the Si matrix [23], the boron-rich layers were shown to be a separate, continuous layer on the Si surface (Fig. 10). Similar microscopic images of the BRL can also be found in Refs. [139, 142–144], where the BRLs were formed through diffusion from boron tribromide (BBr_3) vapour, inkjet-printed dopant paste, spin-on dopant, and chemical-vapour-deposited pure boron layer, respectively. In addition, BRLs are formed at high diffusion temperatures, while the B–Si precipitates are generated by annealing at temperatures where boron is

supersaturated.

Therefore, BRL gettering is discussed separately to the B–Si precipitate gettering. Nevertheless, as both BRLs and B–Si precipitates demonstrate strong gettering effects that are driven by the segregation mechanism, it is possible that the two may have similar underlying reactions associated with the boron-rich silicon boride, SiB_x . In this case, similar activation energies are expected, and the results of Tomita et al. [135] and Vähäniemi et al. [136] may also be interpreted as due to the formation of BRL. However, currently there is no such data to verify their origins, e.g. activation energy of BRL gettering, size-calibrated segregation coefficients, or microscopic understanding of the gettering reactions. In addition, the study of BRL gettering has so far only been carried out for Fe in Si.

The boron-rich layers were found to have strong gettering effects for Fe in Si, even at a high temperature of 950 °C, through a segregation mechanism [121,141]. Despite its high gettering efficiency, BRL is not desirable in Si solar cells, as it inhibits good passivation of the boron diffused silicon surfaces [141,142] and may introduce dislocations and subsequent bulk degradation [139]. BRL is therefore commonly removed during diffusion by oxidising BRL into BSG through an *in-situ* thermal oxidation step after the drive-in or during the cool-down [139, 141,145]. However, such an oxidation process, *in-situ* or *ex-situ* at elevated temperatures, was found to reverse the gettering effect of BRL, driving the gettered Fe atoms back into the silicon wafer bulk [121,141, 143,146].

One way to remove the BRL without losing its strong gettering effect is to chemically oxidise the BRL at low temperatures that do not permit significant diffusion of metal impurities from the surface region back into the silicon wafer bulk, such as demonstrated for Fe at ~100 °C [141]. Room-temperature chemical etching of the BRL is also possible, as shown by Ryu et al. [142]. However the surface passivation quality does not fully recover to the same level as the high-temperature oxidised samples due to a less smooth B profile towards the wafer surfaces [141]. Another potential drawback of an *ex-situ* removal of BRL is that the presence of a thicker BRL (above 10 nm) during diffusion cool-down may generate dislocations and cause bulk degradation [139], although severe bulk degradation was not observed in Ref. [141] even for 40-nm BRLs.

4.2.1.4. Enhanced surface precipitation in B-doped Si. Surface precipitation of Fe in the heavily B-doped Si region was identified as another gettering mechanism associated with B-doped Si [147–149]. Gettering occurs during a low-temperature anneal at 600 °C after a typical boron diffusion at 930 °C. The reduction of the concentration of Fe impurities in Si was found to be due to the relaxation gettering mechanism (i.e. precipitation) [147]. However, the process is enhanced by Fe segregation into the highly B-doped Si, which is driven by the Fermi level effect and ion pairing [66,147]. The experimental results [147] can be largely reproduced by modelling the combined effects of Fe segregation to B-doped Si and surface Fe precipitation [66].

The precipitation sites were suggested to be the silicon surfaces [147]. Sharp Fe peaks towards the highly doped Si surfaces were also revealed by SIMS [149], and the actual profiles of the gettered Fe atoms are likely even narrower due to the ion knock-on artefact in SIMS measurements. Fe precipitation in heavily B-doped Si layers during an *in-situ* low-temperature annealing after boron diffusion has also been observed in Ref. [121], although the gettering effect was as not strong as in Ref. [147], possibly due to the different surface conditions and/or boron diffusion conditions.

4.2.2. Gettering by B ion implantation and annealing

Boron doping by ion implantation and annealing was shown to have some gettering effect during a fast cool-down from an annealing temperature of 1000 °C, only in the close vicinity of the implanted region [150,151]. The authors attributed the mechanism to segregation

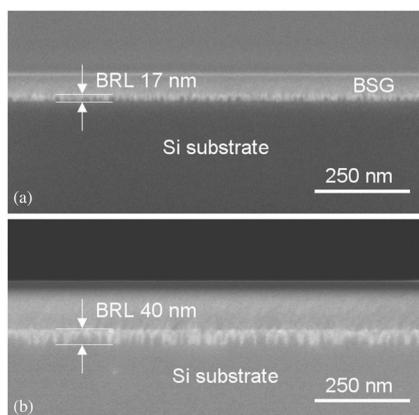


Fig. 10. SEM cross-section images showing the presence of BRL between the BSG and silicon substrate. The samples underwent BBr_3 boron diffusion with different N_2 carrier gas flows: (a) 15 sccm, and (b) 60 sccm. Reprinted from Ref. [141], with the permission of IEEE.

gettering by the Fermi level effect and ion pairing (4.2.1.1). The weak gettering effect can be explained by the low segregation coefficients of Fe in heavily B-doped Si at high processing temperatures [131] and the fast cool-down rate, similar to the inefficient gettering of boron diffusion with *in-situ* oxidation as discussed above.

A later analysis of the data [150,151] by Haarahiltunen et al. [64] argued that the process is likely driven by a combination of segregation (4.2.1.1) and precipitation gettering (4.2.1.4). Like phosphorus ion implanted samples, adding an extended low temperature anneal (550–800 °C) further promotes impurity precipitation, which becomes the predominant gettering mechanism [64,65,150–153].

The precipitation sites are the residual implantation damage after annealing. A TEM image of the residual defects is shown in Fig. 11 [64]. Moreover, Laine et al. [65] showed that an implantation damage model, which simulates the formation of defects in the implanted region based on the implantation and annealing conditions, can be used as an input for the simulation of heterogeneous precipitation of Fe in Si. The simulated results, both in terms of the Fe precipitate size and density and the remaining bulk Fe concentration after gettering, agree well with experimental results.

The test samples in both phosphorus (Sect 4.1.4) and boron ion implantation studies [21,64,65,116,150–153] were intentionally contaminated with a high Fe concentration of above 10^{13} cm^{-3} . Typical industrial silicon substrates (excluding the high contamination regions in cast-grown silicon materials) contain a much lower concentration of metal impurities. A simulation of the combined effects of segregation and precipitation indicates that effective gettering from an ion implanted phosphorus or boron layer may require an even lower annealing temperature to achieve the supersaturation level required for the onset of nucleation and precipitation [21,65], which leads to slow impurity diffusion and largely impractical cell process conditions.

4.2.3. Strategies to improve gettering effectiveness

Strategies that were previously identified for improving PDG (Sect 4.1.5) also apply to BDG. Different to phosphorus diffusions which generally give decent gettering effects even without modifying typical cell processes, typical boron diffusions have weak gettering effects. Special process conditions are required to induce strong gettering effects in BDG, such as to form boron-rich layers and B-Si precipitates, and promote precipitation of metal impurities.

Boron diffusion is commonly carried out at a higher temperature (above 900 °C) than phosphorus diffusion (above 800 °C). More dissolution of metal precipitates in cast-grown silicon materials is therefore expected, along with a higher susceptibility to process contamination, as experimentally observed in Ref. [154]. For the gettering of precipitated metals, the higher process temperature is favourable if it is followed by an efficient lower temperature gettering step, as previously discussed in the *variable temperature gettering* approach (Sect 4.1.5.1) [118]. This was experimentally observed by Vähäniemi et al. [73].

Adding an extended low-temperature anneal to a conventional boron diffusion will likely improve the gettering effect due to the following three reasons: firstly, impurity segregation due to the Fermi level effect

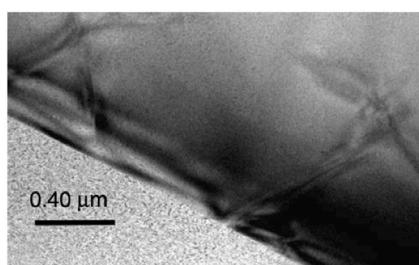


Fig. 11. TEM image of residual defects in a boron ion implanted and annealed silicon wafer. Reprinted from Ref. [64], with the permission of Springer Nature.

and ion pairing increases with decreasing temperatures [131] (4.2.1.1); secondly, annealing at a low-temperature leads to boron supersaturation and thus the possible formation of B-Si precipitates, which are very effective gettering sites [132,136] (4.2.1.2); and thirdly, a lower temperature drives impurity supersaturation and therefore promotes metal precipitation in the near-surface region [147] (4.2.1.4).

Although boron-rich layers are very effective gettering sinks (4.2.1.3), a typical boron diffusion with *in-situ* thermal oxidation oxidises the BRL and the gettered impurities diffuse back into the silicon wafer bulk [141]. An *ex-situ* chemical etching of the BRLs can retain the strong gettering effect, although at the cost of a slightly increased surface recombination activity. The increased surface recombination is partly owing to a higher surface boron concentration, which may be partially resolved by etching back the highly doped surface layers, similar to that proposed in phosphorus diffusions (4.1.5.2).

Lastly, co-doping of a phosphorus diffusion on top of a deeper boron diffused layer, as is used in certain cell architectures such as the buried emitters, was demonstrated to have good gettering effects, even for a relatively light phosphorus diffusion of $140 \Omega/\square$ [114]. The gettering effect does not seem to be affected by the underlying boron diffusions, or the dopant compensation. Even though strictly speaking this is not a strategy for improving the gettering effect of boron diffusions, it offers another approach to tackle the weak gettering effects of conventional boron diffusions with *in-situ* thermal oxidation.

4.3. Heavily doped poly-Si/SiO_x passivating contact structures

In recent years, a rapidly emerging area of active research in silicon PV is a carrier-selective passivating contact scheme based on a layer of heavily doped polycrystalline silicon (poly-Si) film on an ultrathin (1–2.5 nm) silicon oxide (SiO_x) interlayer. A schematic of the poly-Si/SiO_x structure applied on the rear side of an n-type cell is shown in Fig. 12. This carrier-selective passivating contact structure, as its name suggests, markedly reduces carrier recombination at the metal-silicon interface as well as at the non-contacted surface areas, while allowing effective carrier selection and transport (see, e.g., recent reviews in Refs. [4,155,156]). It has enabled record-breaking high efficiency solar cells to be made in the past few years, and the efficiencies are still improving. As the structure is relatively simple (no patterning required) and can be fabricated from a range of techniques and tools in a robust fashion (see, e.g., a summary in Ref. [155]), the poly-Si/SiO_x structure has attracted significant interest from both research and manufacturing industry.

Different to the SHJ passivating contact solar cells which are processed entirely at low temperatures (200–300 °C), the poly-Si/SiO_x structure is formed at high temperatures (750–1000 °C). This allows for sufficient impurity diffusion and thus has the potential to achieve concurrent gettering effects during the cell fabrication process. In addition, the P or B doped poly-Si/SiO_x structure replaces conventional doping of the c-Si surfaces for the formation of p-n junction or back-surface field. It is therefore important to consider the potential gettering effect of doped poly-Si/SiO_x structures. This area of research is still at a relatively early

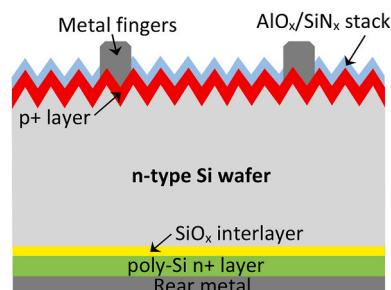


Fig. 12. A schematic of an n-type solar cell featuring a doped poly-Si/SiO_x passivating contact on the rear (not to scale).

stage.

There are multiple ways to grow the ultrathin SiO_x interlayer (from thermal, chemical, ozone, or plasma-assisted oxidation), to deposit the poly-Si film (from low-pressure chemical vapour deposition (LPCVD), plasma-enhanced chemical vapour deposition (PECVD), atmospheric-pressure chemical vapour deposition (APCVD), or physical vapour deposition (PVD)), and to dope and form the heavily doped poly-Si/ SiO_x junction (from *ex-situ* doping via thermal diffusion or ion implantation, or *in-situ* doping during film deposition and subsequent annealing or firing) [4]. These different techniques can induce very different gettering effects, as detailed below.

4.3.1. Undoped poly-Si

Intrinsic (i.e. undoped) polysilicon layers are a well-known gettering sink in microelectronics, applied either on the backside of a device [157] or directly below the active device region [158]. The effect is driven by a combination of relaxation and segregation gettering, due to the presence of a large density of extended defects in poly-Si (see, e.g. Refs. [159,160] and references therein).

In the poly-Si/ SiO_x passivating contact structure, however, the gettering effect of the poly-Si layer alone (i.e. without heavy doping) was found to be quite limited [161,162]. This can be well explained by the volume ratio of the gettering (poly-Si) and the gettered regions (Si wafer bulk), and the moderate gettering efficiency of intrinsic poly-Si layers. The moderate gettering effect of intrinsic poly-Si is sufficient in microelectronic applications as the active device region is much thinner compared to the whole silicon wafer bulk in PV.

Using the reported segregation coefficients of Fe in intrinsic poly-Si from c-Si [160,163,164], the maximum gettering effect of the intrinsic poly-Si layer on c-Si substrate can be estimated, as shown in Fig. 13 for an assumed substrate wafer thickness of 160 μm . Fig. 13 plots the fraction of Fe impurities remaining in the silicon wafer bulk after the segregation gettering reaction reaches its steady state (see Sect 4.1.5.3), thus representing the lower limit of the remaining bulk impurity concentration. It is clear from Fig. 13 that the thin intrinsic poly-Si layers (25–250 nm) cannot generate strong Fe gettering effects at typical temperatures used for the annealing/diffusion or furnace unloading processes, even if there is sufficient thermal budget for impurity diffusion. Although the segregation coefficient can vary depending on the poly-Si deposition conditions and film characteristics [165], it is unlikely to deviate too far to affect the overall gettering effectiveness given the extreme thickness ratio.

The simulation in Fig. 13 only accounts for the segregation gettering effect, and impurity precipitation can further enhance the gettering effectiveness. However, without a slow cool-down or an extended low temperature annealing, precipitation is unlikely to drastically improve the gettering effectiveness of intrinsic poly-Si layers in a typical poly-Si/ SiO_x structure formation process. The stronger gettering effect of intrinsic poly-Si/ SiO_x reported in Ref. [162] as compared to the results in Ref. [161] is possibly caused by the additional contribution from Fe precipitation as the samples experienced extended annealing at lower temperatures (temperature-time profile obtained from private communication).

4.3.2. Heavily doped poly-Si/ SiO_x structures

Although intrinsic poly-Si only has a modest gettering effect, heavy doping of the poly-Si layer (with a small degree of dopant in-diffusion through the ultrathin SiO_x interlayer into the c-Si substrate) can considerably alter the overall gettering effectiveness, depending on the dopant type, doping concentration and technique. The effects and mechanisms are somewhat similar to heavy doping of c-Si wafers in the near surface region, with additional constraints coming from the SiO_x interlayer and the poly-Si film, as will be discussed in this and the following sections. It is worth mentioning that for both P and B doped poly-Si/ SiO_x structures, gathering metal impurities in the heavily doped poly-Si layers was shown to have a negligible impact on the passivation quality of the poly-Si/ SiO_x structures [161].

4.3.2.1. Heavy P doping. Heavy P doping into the poly-Si/ SiO_x structures, from *ex-situ* thermal diffusion from poly-Si surfaces [146,161] or *in-situ* doping during the poly-Si (or then amorphous silicon) film deposition processes [76,162,166], has been reported to reduce the bulk Fe concentrations by a few orders of magnitude, which is much more efficient than the gettering effect of intrinsic poly-Si for Fe as shown in Fig. 13. P-doped poly-Si/ SiO_x structures from ion implantation and annealing were also reported to improve the minority carrier lifetime in the bulk of float-zone [167], epitaxially-grown [168], and cast-mono [169] silicon wafers, confirming a gettering effect associated with the structure formation process. Furthermore, SIMS analysis revealed a relocation of Fe atoms from the silicon wafer bulk to the heavily P-doped poly-Si layer during the gettering process [146] (see Fig. 14).

These results clearly demonstrate the predominant role of heavy P doping in determining the gettering effects and mechanisms (i.e. Sect 4.1) associated with the poly-Si/ SiO_x formation process. It is deduced

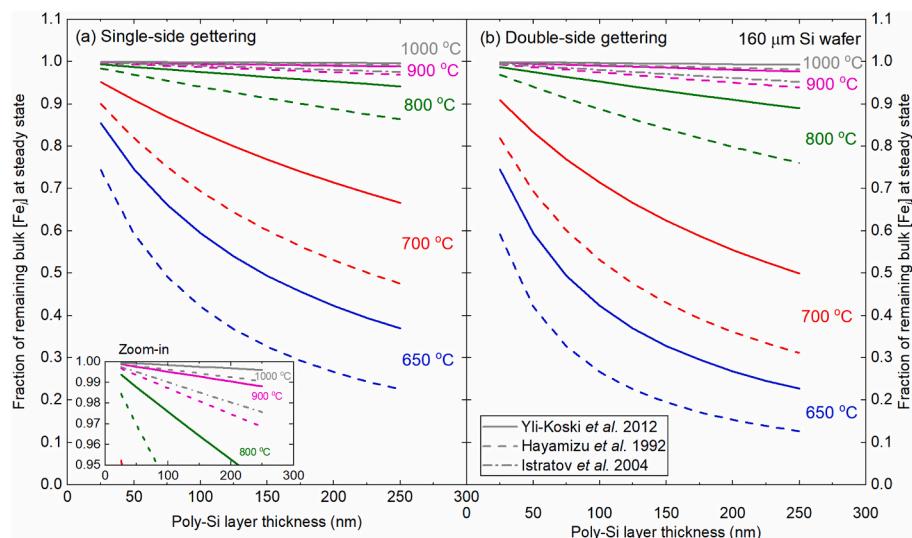


Fig. 13. Lower limit of the fraction of remaining Fe concentration in a 160- μm silicon wafer after segregation gettering by intrinsic poly-Si layer(s) on either (a) one side, or (b) both sides, estimated from the reported segregation coefficients of Fe in intrinsic poly-Si [160,163,164]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

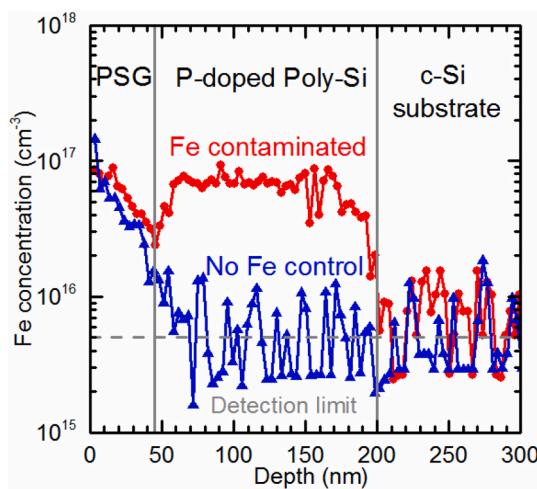


Fig. 14. SIMS analysis of the Fe distribution in phosphorus-diffused poly-Si/SiO_x passivating contact structure on silicon substrates with or without an initial Fe contamination in the silicon wafer bulk. Reprinted from Ref. [146], with the permission of American Chemical Society. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

that the doping technique would also affect the gettering effects, e.g. in a conventional phosphorus diffusion process additional gettering mechanisms may be at play (4.1.2). However no direct comparison can be made based on the limited experimental reports.

The gettering effect from P ion implanted poly-Si/SiO_x was claimed to be comparable with [168] or even superior than [169] a standard phosphorus diffusion. However, this finding *should not* be generalised, as the gettering effectiveness of both processes (poly and PDG) largely depends on the applied process conditions and the associated gettering mechanisms, as previously discussed in Sect 4.1. For instance, the very efficient gettering of P-implanted poly-Si/SiO_x in Ref. [169] had a high implanted P concentration, which equates to a volumetric P concentration of $4 \times 10^{21} \text{ cm}^{-3}$ if distributed uniformly in the reported thin 20-nm poly-Si layer. This is almost an order of magnitude higher than the P solubility limit in c-Si at the annealing temperature [170], and therefore a large concentration of electrically *inactive* P complexes or precipitates could have attributed to the overall gettering effect (4.1.1.2 and 4.1.1.3).

Compared to P diffusion directly into c-Si wafers with the same diffusion conditions, P diffusion into poly-Si/SiO_x structures showed a slightly weaker gettering effect for Fe [161], which can be explained by the ultrathin SiO_x interlayer acting as a diffusion barrier for both Fe and P (detailed later in Sect 4.3.3). The gettering effectiveness of P *in-situ* doped poly-Si/SiO_x for Fe was found to increase with increasing P concentration, poly-Si thickness, annealing time and temperature [162]. The effects of the first three parameters are easy to understand. The effect of temperature, however, may seem surprising at first, as the segregation coefficient of highly P-doped Si for Fe (or P-doped poly-Si [76] in this case) is well known to decrease with increasing temperature (see, e.g. Fig. 7). This can again be explained by the interfacial SiO_x diffusion barrier. A higher temperature allows a higher impurity flux through the SiO_x interlayer, and this may offset the weaker gettering strength of the P-doped poly-Si film for a given temperature-time profile.

4.3.2.2. Heavy B doping. Similar to P-doped poly-Si, the gettering effect of B-doped poly-Si mainly comes from heavy B doping and the associated gettering mechanisms. As previously discussed in Sect 4.2, an effective gettering by B-doped regions relies on the formation of electrically inactive B complexes, in the form of B-rich layers or B-Si precipitates, and this can also be concluded from the studies of B-doped poly-Si/SiO_x structures [135,146,166,167], as detailed below.

An *ex-situ* boron diffusion of the intrinsic-poly-Si/SiO_x structure, without an *in-situ* oxidation after dopant diffusion, was found to generate a strong gettering effect for Fe [161]. The BRL formed during the boron diffusion process (4.2.1.3) was identified as the main gettering sink [146]. A weak gettering effect of the B-doped poly-Si layer alone, due to the moderate segregation coefficients of Fe in B-doped Si (4.2.1.1) and in intrinsic poly-Si (4.3.1), was experimentally confirmed by SIMS [146].

The *in-situ* oxidation step, which is often required in B diffusion of the c-Si surfaces in order to remove the BRL for better subsequent surface passivation, is unnecessary and in fact avoided in B-diffused poly-Si/SiO_x structures, as the oxidation step can potentially oxidise the poly-Si layer. As the presence of the BRL in poly-Si/SiO_x does not seem to affect its passivation quality [161], BRL gettering can be incorporated into the structure formation process, demonstrating a clear advantage over boron-diffused c-Si junctions.

For *in-situ* boron-doped poly-Si from LPCVD [135] or PECVD [166], gettering of bulk Fe impurities and improved bulk carrier lifetimes have been observed as well. Both studies attributed the gettering effects to the electrically inactive B dopants.

As shown in Fig. 15 [135], for a total B concentration above 10^{20} cm^{-3} , the gettering efficiency increases with increasing total B concentration in the poly-Si layer, while the electrically active B concentration, as represented by the measured carrier concentration, remains at 10^{20} cm^{-3} . 10^{20} cm^{-3} is the reported solubility limit of B in c-Si at the annealing temperature of 1000 °C [171,172]. If the total B concentration is below 10^{20} cm^{-3} , that is, there is no electrically inactive B atoms, there is no gettering effect (Fig. 15). These results clearly demonstrate that the electrically inactive B atoms are the main drivers for the observed gettering effect. From the temperature-dependent gettering efficiencies, Tomita et al. extracted an activation energy of 2.1 eV. As this is close to 2.27 eV that is deduced from segregation gettering into B-Si precipitates [133], Myers et al. later attributed the phenomenon to the same B-Si segregation gettering mechanism [23].

The PECVD B-doped poly-Si in Ref. [166] was also reported to contain a large fraction of electrically inactive B atoms, and the presence of a boron-rich layer on poly-Si surfaces was confirmed. Hayes et al. interpreted the boron-rich layer as a region of extended B-Si precipitates, and therefore explained the BRL gettering in the same way as segregation gettering by B-Si precipitates. As discussed previously in Sect 4.2.1.3, BRL and B-Si precipitates share many similarities and it is possible that the two are driven by the same underlying gettering reaction. However more studies are needed to clarify their origins.

On the other hand, boron ion implantation and annealing was

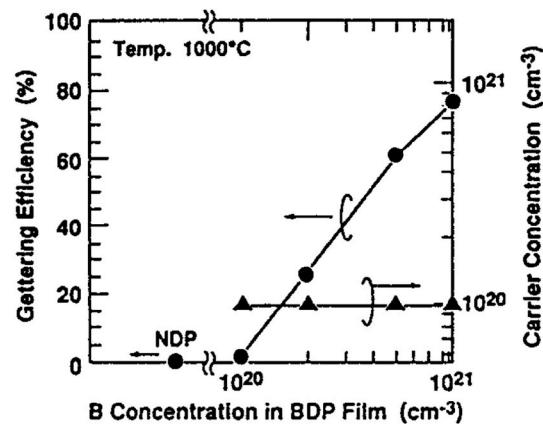


Fig. 15. Dependence of the gettering efficiency of LPCVD *in-situ* B-doped poly-Si/SiO_x on the total and electrically active boron concentrations in the poly-Si film after annealing at 1000 °C. NDP denotes non-doped poly-Si and BDP denotes boron-doped poly-Si. Reprinted from Ref. [135], with permission of Trans Tech Publications.

reported to have no observable bulk gettering effect [167]. As the implanted B concentration in Ref. [167] is close to the solubility limit of B in c-Si at the annealing temperatures [171,172], the result can be understood as the lack of electrically inactive B complexes (BRL or B–Si precipitates) that are strong gettering sinks. Though the presence of electrically inactive B in the defect-rich poly-Si layer cannot be entirely ruled out. This result again demonstrates that the segregation gettering effects of B-doped Si and intrinsic poly-Si are too small to result in substantial gettering of bulk impurities for the given sample structure, i.e. an extremely small thickness ratio of the B-doped poly-Si layer to the c-Si wafer bulk (Sect 4.2.1.1 and 4.3.1).

4.3.3. SiO_x interlayer

The main gettering sink in the poly-Si/ SiO_x structure is identified to be the poly-Si layer – either the heavily P-doped poly-Si, or the electrically inactive B complexes (BRL or B–Si precipitates) residing in the poly-Si [146]. However, the gettering rate is largely determined by the ultrathin SiO_x interlayer, which acts as a diffusion barrier for metal impurities to reach the poly-Si gettering sink from the silicon wafer bulk [76]. Different SiO_x growth techniques, which affect the stoichiometry, density and integrity (i.e. formation of pinholes) of the SiO_x after a high-temperature formation process, result in different blocking strengths of the SiO_x interlayer [76]. An example is shown in Fig. 16. In general, the blocking strength increases with increasing oxide thickness, stoichiometry, and decreasing density of pinholes [76,161,162] (the effect of pinholes to be published). The blocking strength can be characterised and modelled by the oxide thickness and the diffusivity and solubility of metals in the oxide [76].

The structure is somewhat similar to the gettering in buried oxide (BOX) based devices in microelectronics [173]. However, the oxide interlayer is much thinner in the poly-Si/ SiO_x structure (1–2.5 nm) than in BOX (hundreds of nm), which seems to have affected the diffusivity and/or solubility of Fe in oxide [76]. Moreover, as mentioned above, different SiO_x interlayers demonstrate different blocking strengths, which are related to the metal diffusivity and solubility in the SiO_x . Therefore, prior knowledge of the diffusivity and solubility in thick oxide may not be applicable for these ultrathin oxide layers and needs to be re-assessed.

Note that the SiO_x interlayer only affects the gettering rate, but not

the gettering strength of the heavily doped poly-Si layer. That is, if given sufficient thermal budget for metal impurities to diffuse through the SiO_x “diffusion bottleneck”, the full gettering potential of the poly-Si layer can be achieved, as shown in Fig. 16 by the steady state conditions.

4.4. Dielectric films

Dielectric films are an integral part of silicon-based devices, providing surface passivation, antireflection and capping/masking purposes. The most commonly used dielectric films in silicon solar cells are silicon oxide, silicon nitride and aluminium oxide. In this review, we will focus on the gettering effects of the latter two, which have not been reviewed in detail elsewhere and progresses were made in recent years. Gettering by silicon oxide, and the interaction of metals with silicon oxide and its induced defects near the oxide-silicon interface, were well studied in microelectronics, and reviews of such topics can be found in, for examples, Refs [23,24,83].

4.4.1. Silicon nitride

4.4.1.1. At temperatures above 1000 °C. The gettering effect of silicon nitride films was first reported by Petroff et al. in the 1970s [18,174] and later by others too [175,176]. They found that by annealing silicon wafers with a layer of silicon nitride on the back-side, the formation of stacking faults on the front-side during subsequent oxidations was suppressed. This was attributed to an impurity gettering effect, as NAA showed reductions of the Au and Cu concentrations [18]. In addition, metal impurities are well known to promote stacking fault formation during oxidations. The annealing step generally took place at 1000–1200 °C for 0.5–4 h in an inert gas ambient. The films of several-hundred-nanometre-thick were either from chemical vapour deposition (CVD) at 700–800 °C [18,174–176], forming stoichiometric silicon nitride (Si_3N_4), or from sputtering at 300 °C [18], forming non-stoichiometric nitride (denoted as SiN_x).

Tanno et al. [175] later found that a critical thickness of about 250 nm is required to induce the onset of effective gettering by the investigated CVD Si_3N_4 films. This thickness correlates to the appearance of cracks in the Si_3N_4 films. These cracks, along with a large bow of the silicon wafer due to a layer of thick Si_3N_4 film, are believed to create and introduce dislocations into the wafer, acting as effective gettering sites. Some of the dislocations were found to even propagate to the front-side of the silicon wafers.

The evolution of defects at the CVD Si_3N_4 -Si interface was *in-situ* studied by Jourdan et al. [177] using synchrotron x-ray topography. Upon an initial N_2 or vacuum annealing with Si_3N_4 at temperatures above 1000 °C, <100> line defects are developed, which then generate tangled dislocations during subsequent oxidation at 1000 °C. A high density of defects at Si_3N_4 -Si interface after several high temperature oxidations (950 and 1150 °C) were also observed through TEM by Partanen et al. [178].

4.4.1.2. At lower temperatures (250–900 °C). In more recent years, Liu et al. [179] reported that the silicon nitride films also possess impurity gettering effects at much lower annealing temperatures. The examined temperature range was 250–900 °C, and the films were from PECVD and were only 80 ± 10 nm thick. By annealing silicon wafers with silicon nitride (generally non-stoichiometric SiN_x) films on one or both sides, or even during the film deposition process, a reduction of the Fe impurity concentration in the silicon wafer bulk was observed [179,180].

Although this phenomenon was initially thought to be associated with the hydrogen injection from SiN_x films [181], it was later found out that the bulk Fe reduction was accompanied by an increase of the Fe concentration in or near the SiN_x films, as revealed by SIMS (Fig. 17). Within the uncertainty range, the concentration of the Fe loss from the silicon bulk roughly agrees with the Fe accumulation in or near the SiN_x

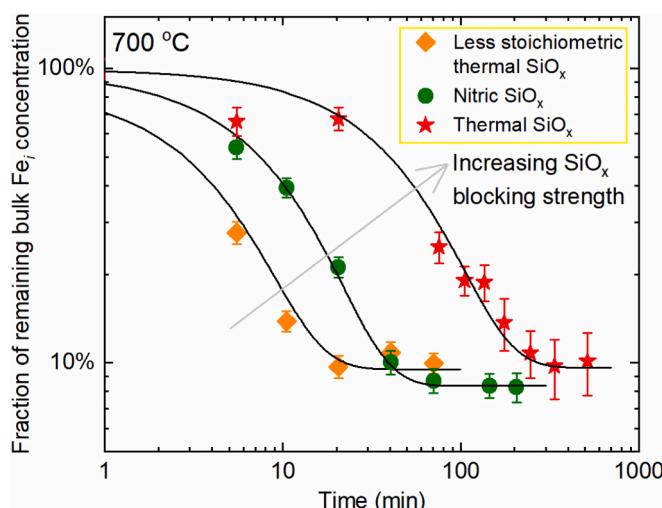


Fig. 16. Fraction of the remaining Fe concentration in the silicon wafer bulk as a function of cumulative annealing time, which demonstrates the rate of gettering by the poly-Si/ SiO_x structures. The samples had the same PECVD *in-situ* P-doped poly-Si layers but different SiO_x interlayers, and were annealed at 700 °C after a typical structure formation process. Data were from Ref. [76]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

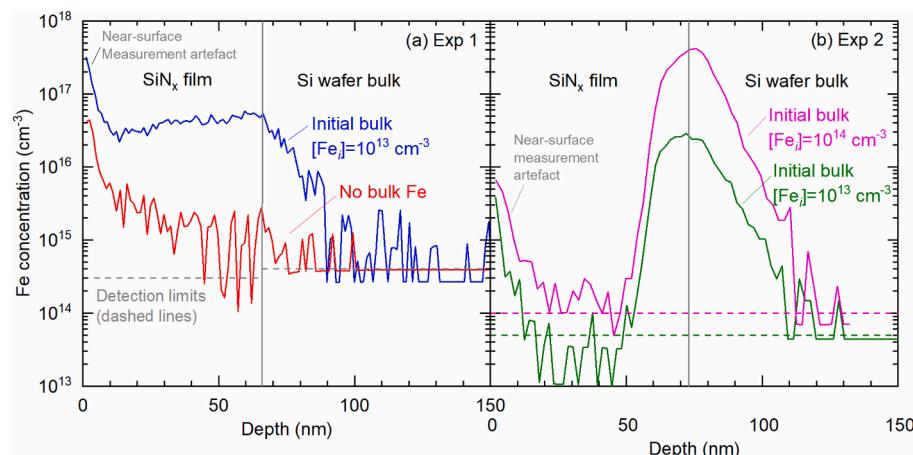


Fig. 17. SIMS profiles of the Fe concentration in PECVD SiN_x coated Si samples with or without an initial Fe contamination in the silicon wafer bulk. The SiN_x/Si samples were annealed at 700°C for 30 min. The data in (a) were from Liu et al. [179] and (b) are unpublished results. The samples in (a) and (b) underwent the same processes (but at different times), and demonstrate different Fe distribution profiles, which is yet to be understood. Nevertheless, the accumulation of Fe in or near SiN_x films is evident. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

films. Furthermore, deep level transient spectroscopy (DLTS) and minority carrier transient spectroscopy (MCTS) detected no other deep levels (such as from Fe–H complexes [182]) in the silicon wafer bulk after the gettering anneal. These findings confirm the gettering effect of SiN_x films. Gettering of other transition metals, Cu, Ni, and Cr, were also detected by SIMS [41,42].

As the remaining Fe concentration in the silicon wafer bulk can be reduced to well below the solubility limit of Fe in Si, SiN_x gettering was identified to be a segregation gettering process, at least at high temperatures [179]. Recent studies at 400°C confirmed that the gettering process is predominantly segregation at low temperatures too [183].

A wide range of silicon nitride films, from both industrial- and laboratory-scale PECVD reactors, were found to have this gettering effect, although the gettering kinetics and strengths may vary [180]. LPCVD silicon nitride films were also observed to induce similar gettering effects, however at a much slower rate, as shown in Fig. 18. Certain PECVD SiN_x films can achieve a fast gettering process that is only largely limited by the diffusion of Fe in the silicon wafer bulk to reach the surface SiN_x films, at temperatures below 700°C [179,183].

The activation energies for the SiN_x segregation gettering process were estimated to be $0.9 \pm 0.1 \text{ eV}$ for a PECVD SiN_x film and 1.6 ± 0.5

eV for an LPCVD SiN_x [183]. There seems to be a higher density of gettering sites associated with the investigated PECVD SiN_x compared to the LPCVD SiN_x [183]. However, different deposition conditions do affect the SiN_x gettering kinetics and strengths, and it is so far difficult to pinpoint a certain trait or traits of the films that determines the gettering characteristics, or to explain the different impurity distribution near SiN_x films (as can be seen in Fig. 17).

The gettering mechanism is still under investigation. Some of the early explanations from high temperature silicon nitride gettering, however, cannot explain the gettering effect of the thinner SiN_x films at lower temperatures. For instance, Jourdan et al. [177] observed that the formation of dislocations, which are believed to be the gettering sites, only appears after a further high temperature oxidation step. In addition, the formation of line defects, which are the prerequisites for dislocations, only occurs strongly above 1000°C [177]. The generation of dislocations, and thus effective gettering, also requires thick Si_3N_4 films (above 250 nm) that have cracks and can in addition induce a large bow of the silicon wafer with a single-side film deposition [175]. The films for the lower temperature (250 – 900°C) gettering studies were 70–120 nm thick and deposited on both sides of the silicon wafers [41,42,179,180]. Moreover, the gettering kinetics (see examples in Fig. 18) indicate that gettering happens straight away upon annealing, even at a very low temperature of 250°C [179], without requiring a certain anneal time for, for example, the formation of dislocations.

4.4.2. Aluminium oxide

In the initial study by Petroff et al. in the 1970s [174], a back-side 200-nm aluminium oxide (Al_2O_3) layer, from pyrolysis of aluminium chloride at 835°C , was also found to reduce the oxidation-induced stacking faults via a 1050°C 1-h anneal prior to oxidation.

More recently, Liu and Macdonald examined the gettering effect of thin Al_2O_3 films (20–80 nm) at lower annealing (i.e. gettering) temperatures of 425°C (typical passivation activation temperature) [184] and 700 – 900°C (typical metal contact firing temperatures) [185]. The Al_2O_3 films were from atomic layer deposition (ALD) at 170 – 200°C . Gettering of Fe to the interface of Al_2O_3 and Si was observed by SIMS in both temperature ranges [184,185], as shown in Fig. 19. Under certain circumstance, Fe also moves from the interface into the bulk of the Al_2O_3 film, as shown in Fig. 19(b) after a long anneal at 900°C . Such a high-temperature long anneal is uncommon in cell fabrication, and therefore in typical process conditions only gettering to the Al_2O_3 -Si interface is expected. As with SiN_x gettering, it is unclear what drives such impurity distribution changes.

ALD Al_2O_3 films require a thermal anneal to active the passivation effect of the films, which often takes place at around 425°C for minutes to tens of minutes. It was found that this activation step affects the subsequent gettering effect of Al_2O_3 films at higher temperatures

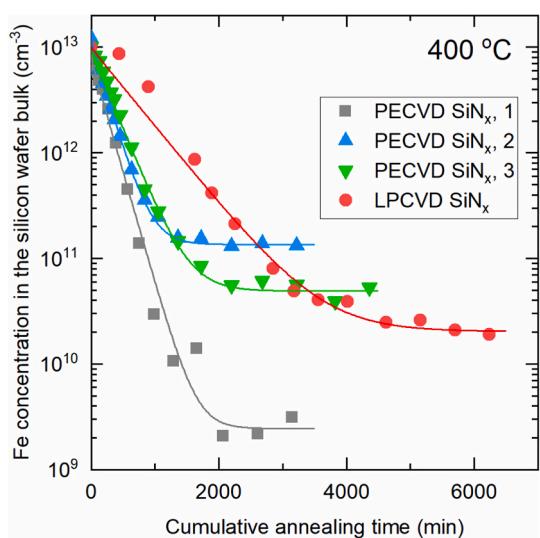


Fig. 18. Gettering kinetics of different silicon nitride films at 400°C . The symbols are experimental data and the lines are simulations assuming a diffusion barrier at the SiN_x -Si interface. Data were from Ref. [183]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

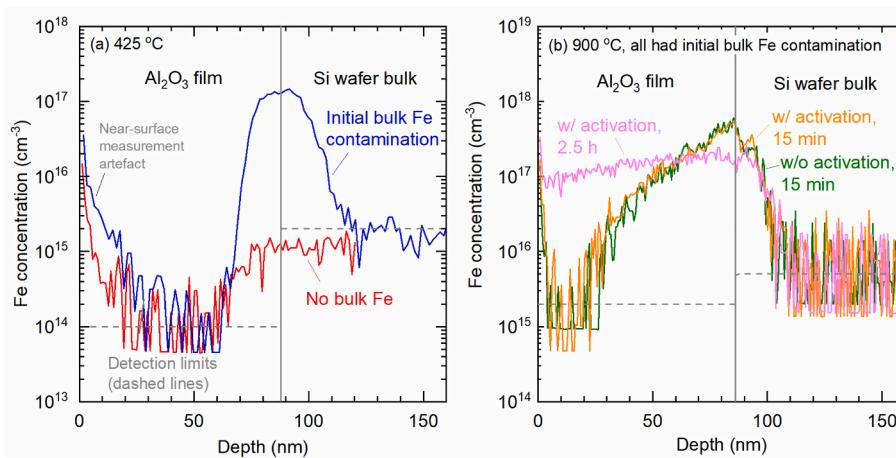


Fig. 19. SIMS profiles of the Fe concentration in ALD Al_2O_3 coated Si samples with or without an initial Fe contamination in the silicon wafer bulk. The samples in (a) were annealed at 425 °C for 18 h, and in (b) were annealed at 900 °C for either 15 min or 2.5 h, with or without a prior activation step. The samples in (b) were all initially contaminated with Fe in the silicon wafer bulk. The data in (a) were from Ref. [184] and (b) from Ref. [185]. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

(700–900 °C) [185]. An example is shown in Fig. 20, where it is clear that the as-deposited Al_2O_3 film getters more effectively than the activated film. SIMS reveals that, with or without a prior activation anneal, gettering happens at the Al_2O_3 -Si interface (see Fig. 19(b), without considering a prolonged annealing time). The main difference between the as-deposited and activated Al_2O_3 -Si interfaces is a significant reduction of the interface defect density after activation, while the fixed negative charge density is only slightly improved [186]. Therefore the difference in gettering effectiveness likely relates to the different Al_2O_3 -Si interface defect densities, with a higher defect density resulting in a better gettering effect.

An ultrathin interfacial SiO_x layer (about 1–2 nm) is known to exist between Al_2O_3 and Si [186]. This interfacial layer is critical for the surface passivation quality of Al_2O_3 films, and one commonly believed explanation for the reduction of interface defect density after activation is the hydrogen-related passivation of the interfacial SiO_x layer [187]. Therefore, impurity gettering possibly takes place at the defect sites of the interfacial SiO_x layer.

As gettering can happen at temperatures where the solubility limits of Fe in Si are much larger than the dissolved Fe concentrations in Si, as shown in Fig. 20(c), it is evident that Al_2O_3 gettering is via a segregation mechanism, at least at high temperatures [185]. At low temperatures there may be a concurrent precipitation process, although experimental verifications are needed.

Gettering by dielectric films (SiN_x , Al_2O_3) at elevated temperatures,

where metal impurities are mobile, occurs during cell processing, such as during the film deposition, Al_2O_3 activation, and contact firing processes. As can be inferred from Fig. 2 in Sect 3.2, the thermal budgets associated with these typical processes are insufficient to substantially reduce the concentration of Fe in the silicon wafer bulk. However, very fast diffusing metals such as Cu, Ni, and perhaps Co in some instances, can have a significant fraction of the bulk mobile impurities being gettered during these processes. Unintentional gettering by dielectric films at elevated temperatures may also obscure experiments studying other effects or bulk defects, and thus care must be taken to exclude the contribution from gettering.

The impact of impurity aggregation on the passivation quality of dielectric films, however, has not been examined. It is therefore unclear at this stage whether or not dielectric gettering can be exploited, or should be avoided, in future cell fabrication.

4.5. Aluminium alloying

In conventional solar cells, aluminium-silicon alloying on the back side of silicon wafers is applied to form metal contacts, either as a full-area contact in aluminium back surface field (Al-BSF) solar cells, or local contacts in PERC solar cells. As Al is a shallow acceptor in silicon, the process also results in p+ doping of the silicon surface region, and hence the term “back surface field”. Samples are typically fired to a peak temperature of 750–850 °C before being rapidly cooled down for Al

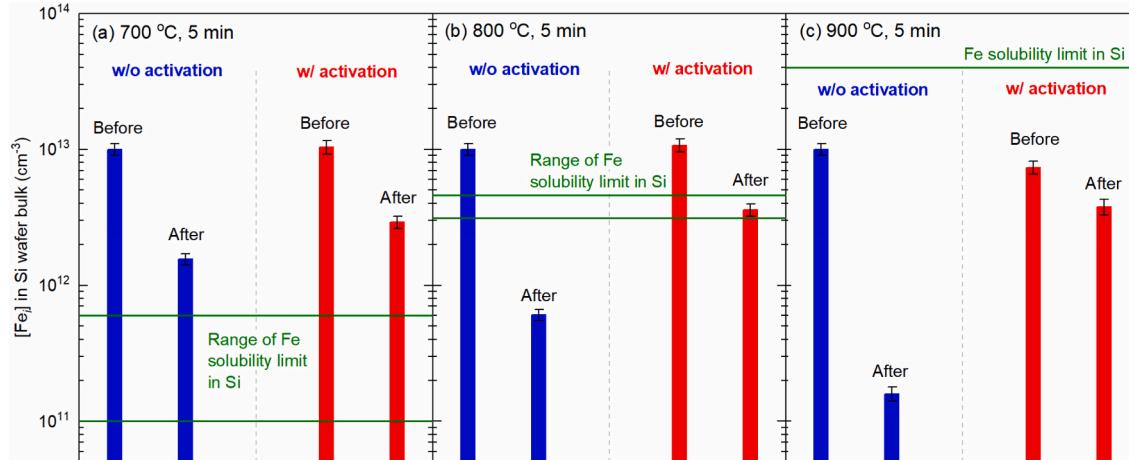


Fig. 20. Dissolved Fe concentration in the silicon wafer bulk before and after a 5-min annealing step at (a) 700 °C, (b) 800 °C, and (c) 900 °C. The silicon wafers were coated with ALD Al_2O_3 films on both sides, and the films were either in the as-deposited state (i.e. without activation), or had undergone a prior 425 °C activation step. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

metal contact formation. A liquid Al-Si alloy is formed at a temperature above the eutectic temperature of the binary Al-Si system, which is 577 °C.

Transition metals such as Cu [60,188], Co [189] and Fe [190,191] have orders of magnitude higher solubilities in the Al-Si alloy than in c-Si. This difference in solubilities drives the segregation gettering action by the backside Al layer during contact firing. The reported gettering effects were based on studies using pure Al, whereas in industry screen-printing paste containing Al and other components (such as organic compounds) is used, which may affect the gettering effect. Annealing with an Al layer was also found to inject vacancies into the silicon bulk, which is believed to benefit subsequent hydrogenation treatment [192,193].

Although Al gettering is extremely effective, the short duration of the contact firing process, which is only on the order of seconds, limits the amount of metal impurities that can be gettered to the backside Al-Si alloy during typical cell fabrication, as many have reported (see, e.g. Refs. [50,121,194]). Moreover, local Al contacts, such as on the backside of PERC solar cells, are even less effective in reducing the overall bulk impurity concentration due to the limited size ratio (see Sect 4.1.5.3). As the Al-BSF solar cells are being gradually phased out and replaced by PERC and other more advanced cell structures, Al gettering, although very effective, is unlikely to play a major role in impurity gettering during typical cell processing.

4.6. Surface damage

Damage to the silicon surface, such as from mechanical abrasion [195–199] or laser [200,201], has been well demonstrated to serve as gettering sinks in microelectronic applications. As previously discussed in a review article by Istratov et al. [83], the gettering mechanisms possibly involve a combination of segregation and relaxation reactions, in some cases accelerated by an injection of silicon self-interstitials.

In photovoltaic applications, gettering by the saw damage on silicon wafer surfaces has been observed as well [202–204]. Another type of surface damage is the so-called black silicon, which intentionally creates needle-like nanostructures on the silicon surfaces to eliminate front-surface reflection, and thus the wafers appear black. Combining phosphorus diffusion with black silicon is shown to enhance the gettering effectiveness, due to heavy doping of the nanostructured needles (especially at the tip) and larger surface area for impurity segregation [205].

In epitaxial silicon solar cells, a porous silicon layer is embedded in-between the top epitaxial layer (i.e. the active device region) and the low-quality silicon substrate. This porous silicon layer is found to not only act as a reflector to enhance light absorption in the top thin epitaxial layer, but also prevents impurities from reaching the top layer [206,207]. This gettering effect is believed to be due to impurity segregation to the void surfaces [207], similar to the chemisorption trapping mechanism of nano-cavities in microelectronics [23]. Radhakrishnan et al. [207] observed high impurity (Cu, Ni, Fe, Cr) concentrations in the porous silicon layer using SIMS and direct total reflection X-ray fluorescence (TXRF). Smaller pores were found to be more effective at gettering than larger pores, possibly due to a combination of higher binding energies and higher trap concentrations. Creating sacrificial porous silicon layers on silicon wafer surfaces was also proposed to improve the bulk materials quality of solar-grade silicon [208].

4.7. Internal gettering

Internal gettering by intentionally introduced silicon oxide precipitates in the bulk of the silicon substrates is commonly applied in microelectronics. This technique, however, is not suitable for silicon PV, because the whole silicon wafer bulk is part of the active device region and the oxide precipitates introduce strong recombination centres in

silicon [17,209,210]. In addition, in the presence of a phosphorus diffused surface region, bulk impurities are found to be preferentially gettered to the P-doped region compared to the oxide precipitates in the bulk [211].

In multicrystalline silicon where there are naturally a large amount of extended defects (dislocation, grain boundaries and microdefects, for example), internal gettering of metallic impurities to the extended defects is an inherent process during ingot growth and, to a lesser extent, during cell processing. Metal precipitates located at structural defects have been directly observed in as-grown mc-Si materials by synchrotron-based x-ray microprobe techniques [38,43,212]. Processing mc-Si wafers at temperatures where metal impurities are supersaturated and sufficiently mobile results in the precipitation gettering effect as well [213–215]. In addition to precipitation, the strain field near structural defects can give rise to an enhanced solubility for metals, and metals can also bind to the dislocation core [14]. Detailed interactions of the metals with extended defects were studied by Seibt et al. [14,53,216] and can also be found in a previous review article [26].

Annealing mc-Si wafers at a relatively low temperature (below 600 °C) was found to generally increase the *spatially averaged* effective minority carrier lifetime, resulting in an improved device performance, particularly for wafers from the so-called red-zone regions (top and bottom of an ingot, or edges of a brick) where the as-grown metal concentrations are high [124,125,215,217–223]. The increase in bulk lifetime is usually accompanied by the observation of a reduced Fe point defect concentration in the silicon wafer bulk (Fe is routinely examined due to its ease of detection), and therefore the process is often attributed to the internal gettering effect. However, it is worth pointing out that, *not all* of the reported benefits of a low temperature annealing (LTA) were solely due to internal gettering, as discussed below.

Rinio et al. [124,125] found that in the presence of a phosphorus diffused surface region, external gettering plays a more predominant role than internal gettering, and internal gettering alone shows no appreciable effect. In addition, Fe precipitates were found to be largely unchanged after the LTA, and the findings were also confirmed by a simulation of the PDG effect at low temperatures [72,125]. However, a later study by Al-Amin and Murphy [222] drew an opposite conclusion, that is, the presence of a phosphorus diffused region makes little difference to the effect of LTA. Although the contradiction may seem surprising at first, it is possible to understand the different results in terms of the driving forces for the internal and external gettering processes. Internal gettering relies on sufficient impurity supersaturation, diffusion to reach the gettering sites, and the availability of the gettering sites. On the other hand, the effectiveness of PDG depends on the P doping concentration and possibly other parameters associated with the diffusion process, such as the formation of silicon-phosphorus precipitates, phosphorus-vacancy clusters, oxygen concentrations, for example, as previously detailed in Sect 4.1, as well as sufficient impurity diffusion length to reach the surface gettering sinks. Therefore, the effectiveness of internal and external gettering during an LTA highly depends on the annealing conditions, the mc-Si material properties (in terms of the impurity type, concentration, and the type and distribution of the extended defects and pre-existing precipitates as internal gettering sites), and the properties of the phosphorus diffused layers.

The initially reported efficiency improvements in solar cells that underwent an LTA after phosphorus diffusion [217] may be partly due to the external gettering effect of PDG at low temperatures. The presence of different surface dielectric films during LTA can also affect the overall gettering effect [215,221]. The fast, diffusion-limited Fe gettering kinetics observed in Ref. [218] is possibly caused by an external gettering to the surface PECVD SiN_x films [179]. On the wafer level (i.e. after ingot solidification), without PDG or surface dielectric films (SiN_x or Al₂O₃), the kinetics of internal gettering to extended defects in mc-Si during an LTA were shown to be much slower and the effects are much less pronounced [215,220,221]. As the effect of internal gettering alone is marginal (compared to PDG, for example) on industrial mc-Si materials

and the process generally requires a very long annealing time (many hours to days) [215,220–222], internal gettering by itself may not be of interest to the PV manufacturers.

If an LTA is applied before phosphorus diffusion, reinjection of the internally gettered metals, such as via precipitate dissolution, during high temperature PDG has to be considered. While Boulfrad et al. [219] observed a reduced effectiveness of PDG after internal gettering at low temperatures, Al-Amin and Murphy [222] saw a small benefit of applying LTA prior to PDG in improving the overall material quality. This difference can again be explained by the large variations in the material properties of the mc-Si wafers, the potentially different properties and interactions of the internally gettered metals and gettering sites, and the LTA and PDG test conditions. Combing LTA and PDG therefore requires a careful, tailored design of the process conditions. Lastly, reinjection of the internally gettered metals may also occur during contact firing, which is the last high temperature step experienced by most cells.

5. Summary

Although gettering has been an old topic in silicon microelectronics since the very beginning, many of the gettering techniques in microelectronics are not applicable or effective in silicon PV. This article has presented an up-to-date review of the gettering techniques and approaches that are relevant for silicon solar cells, from conventional phosphorus diffusion and aluminium alloying to the more recently reported doped-poly-Si/SiO_x passivating contact structures and dielectric films. Gettering in solar-grade cast-grown silicon materials, which contain a large fraction of metal precipitates and a high density of crystallographic defects, has also been discussed. Recent updates to the solubility and diffusivity data of the common 3d transition metals in silicon, which are essential parameters for gettering, are also included.

As the silicon wafer bulk constitutes an important part of the active device region, external gettering is generally more effective in silicon solar cells. The external gettering routes that are most relevant for the state-of-the-art solar cells in mass production are phosphorus diffusion, to a lesser degree boron diffusion, and the emerging P- or B-doped poly-Si/SiO_x structures. Phosphorus diffusion remains as the most used and researched gettering technique in silicon PV, although its underlying mechanisms remain controversial and unresolved, resulting in large variations in the predictive modelling of PDG. Boron diffusion can be very effective under certain *unconventional* process conditions, where a high level of boron supersaturation (forming B–Si precipitates or boron-rich layers) leads to a strong segregation gettering effect. However, these conditions generally degrade the subsequent surface passivation effect. Nevertheless, such boron supersaturation is possible in the doped-poly-Si/SiO_x structures without compromising surface passivation, providing a route to concurrently achieve p+ doping and strong gettering effects. The heavily doped c-Si surfaces and/or heavily doped poly-Si/SiO_x structures are incorporated in almost all of the high-temperature cell architectures. As the two are effective gettering sinks and their underpinning gettering mechanisms are likely the same (i.e. due to heavy doping of phosphorus or boron in silicon), a better understanding and identification of the key mechanism(s) will help to further exploit the benefits of gettering in silicon PV.

The external gettering sinks involving dielectric films (silicon nitride and aluminium oxide) and aluminium alloying likely play a relatively minor and complimentary role in terms of gettering during *typical* cell fabrication processes, as the gettering process is largely limited by metals diffusing towards the surface gettering sinks, except for the very fast diffusing metals of Cu and Ni. These techniques are also much less well studied. Internal gettering by existing crystallographic defects in cast-grown silicon is significant during ingot growth, but in terms of processing on the wafer level, internal gettering, as well as gettering by surface defects, requires long annealing time and the gettering effects are quite limited, making them unsuitable for silicon PV processing.

Cell architectures that are entirely processed at temperatures below 200–300 °C, such as the silicon heterojunction and metal compound based passivating contact (also known as dopant free passivating contact) solar cells, do not provide sufficient thermal budget for most metals to diffuse to the surface gettering sinks. Gettering is therefore not possible during typical processing of such low-temperature architectures, unless a pre-treatment is carried out.

CRediT authorship contribution statement

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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