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Can we see defects in capacitance measurements of thin-film solar cells?

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Abstract

Thermal admittance spectroscopy and capacitance-voltage measurements are well established techniques to study recombination-active deep defect levels and determine the shallow dopant concentration in photovoltaic absorbers. Applied to thin-film solar cells or any device stack consisting of multiple layers, interpretation of these capacitance-based techniques is ambiguous at best. We demonstrate how to assess electrical measurements of thin-film devices and develop a range of criteria that allow to estimate whether deep defects could consistently explain a given capacitance measurement. We show that a broad parameter space, achieved by exploiting bias voltage, time, and illumination as additional experimental parameters in admittance spectroscopy, helps to distinguish between deep defects and capacitive contributions from transport barriers or additional layers in the device stack. On the example of $Cu(In,Ga)Se_2$ thin-film solar cells, we show that slow trap states are indeed present but cannot be resolved in typical admittance spectra. We explain the common N1 signature by the presence of a capacitive barrier layer and show that the shallow net dopant concentration is not distributed uniformly within the depth of the absorber.

KEYWORDS

admittance spectroscopy, capacitance, deep defects, doping profile, thin films

1 | INTRODUCTION

An accurate measurement of the net dopant concentration and a quantitative characterization of recombination-active defects in photovoltaic absorbers are critical for understanding and optimizing solar cell performance. Electrical measurements of the voltage- or frequency-dependent capacitance of a given device can in principle provide a direct quantification of the relevant shallow dopant and deep trap level parameters; see for example Ref.[1-3] These voltage- and frequency-dependent capacitance measurements are commonly performed separately and referred to as capacitance-voltage (C-V) analysis and thermal admittance spectroscopy (TAS), respectively. In the standard textbook approach, steps in the capacitance spectrum are assigned to deep defect levels, and the apparent doping concentration is derived from the slope of the "Mott-Schottky plot" of $1/C^2$ vs V, if possible at measurement frequencies beyond the capacitance step. An apparent depth dependence of the resulting doping concentration is then often attributed to charge contributions of deep trap levels[4] because their charge state depends on the band bending—and thus apparent width—of the space charge region (SCR) as discussed in more detail below. These capacitance-based measurement techniques are well established for bulk semiconductors but are challenging to interpret in thin-film devices.[5] One issue is that thin-film solar cells consist of several thin layers with corresponding

interfaces, which means that the measured device capacitance typically cannot be attributed to the SCR alone. This complex device geometry might thus require a complex electrical equivalent circuit[6-11] to even identify the SCR capacitance from the measurement. On the other hand, inter-diffusion of mobile species between the thin layers in the device stack[12-18] likely results in graded interfaces, where electronic properties could vary drastically with depth.

The resulting complexity of experimental capacitance spectra of thin-film devices has often led to considerable controversy how such measurement could be explained most appropriately. We will focus on typical Cu(In,Ga)Se_2 (CIGS) thin-film solar cells to illustrate this challenge, but our experimental approach will be equally relevant and straight-forward to adapt for other thin-film technologies with complex device stacks, for example, perovskite, $Cu_2ZnSnSe_4$ (CZTSe) kesterite, or CdTe. Solar cells based on CIGS are very flexible with respect to device architecture and elemental composition, and thus abundance of intrinsic electronic point defects, and the exact details of experimental capacitance spectra often differ substantially between individual samples. Nevertheless, two characteristic features appear to be universally observed for virtually all CIGS thin-film solar cells:

- At least one pronounced step of the frequency-dependent capacitance in TAS with an activation energy around 100 meV, which has been termed the "N1" signature in CIGS.[6,19,20] A similar capacitance step has also been reported for CZTSe[21] and CdTe.[22]
- A "U"-shaped depth-dependent doping profile,[6,17,18,23-26] resulting from a curved "Mott-Schottky" plot. The minimum apparent dopant concentration is typically in the range of a few 10^{15} cm^{-3} to 10^{16} cm^{-3} and increases toward negative bias voltages, that is, toward higher apparent depth within the absorber.

Deep defects lead to non-radiative recombination losses, and thus characterization of their capacitive response is of highest concern for the optimization of solar cell efficiency. Historically, capacitance steps in TAS have been most widely assigned to defect levels in semiconductors. Indeed, a capacitance feature in CIGS termed "N2"[19] was found to be a bulk defect and was shown to scale with the Ga content in the absorber and to adversely affect the device efficiency for high Ga concentrations.[27-29] This N2 defect level appears to be no longer present in state-of-the-art high-efficiency solar cells.[30] Defects have traditionally also been thought to cause the N1 signature in CIGS, which has been proposed as the signature of a defect level either at the interfaces[19,31] or in the bulk.[26] Electronic effects other than defect levels result in capacitance steps as well, and the N1 level has also been linked to transport phenomena in the bulk[32,33] or transport barriers at interfaces or additional layers within the device.[6,8,10,11,22,30,34,35] Note that seemingly different capacitance steps in different samples are commonly identified with the same feature, in this case, N1, if their attempt-to-escape frequency and activation energy—obtained from the temperature dependence of the inflection frequencies—lie on the same line in a Meyer-Neldel plot.[36,37] In particular for the N1 signature, literature reports scatter substantially around such a line,[20] and the Meyer-Neldel rule might in fact not be a suitable tool to classify defect signatures.[30] Furthermore, several independent signals might contribute to a single capacitive response identified as N1,[34,38,39] indicating that the dominant physical origin of the N1 signature is not necessarily the same for all solar cells—despite the similarity of the corresponding capacitance steps. A more detailed recent discussion of the various models to describe the N1 signature is presented in Ref.[30]

Apparently, a consistent and universally applicable model to describe the N1 signature is currently out of reach. In fact, such a model might not even exist because—as discussed above—the seemingly universal N1 signature might have very different physical causes in different individual solar cells. Without an unambiguous understanding of all steps in the frequency-dependent capacitance spectrum and how these might relate to potential electronic defects in the semiconductor, in particular for the ubiquitous N1 signature, any interpretation of deep defect and dopant concentrations from capacitance measurements will necessarily be uncertain. This limitation of our current understanding of capacitance-based characterization of thin-film solar cells has very relevant practical consequences: Although the net dopant concentration is one of the most important quantities defining the operation of a semiconductor device,[3] and although recombination via deep defect levels is a major limitation of solar cell efficiency, we currently have no simple experimental approach to correctly and reliably quantify these two parameters for a thin-film solar cell.

We recently presented a number of studies on the electronic properties and resulting capacitance spectra of CIGS solar cells, where we combined Hall measurements,[18,40] ac impedance measurements under varying experimental conditions (frequency, temperature, bias voltage, illumination, and time),[10,17] temperature-dependent current-voltage measurements,[30] numerical device simulations,[9,30,41] and deliberate variations in absorber chemistry[30] and layer stack architecture[10,11,17,30] in an attempt to establish a consistent understanding of the electronic properties of these particular devices. We concluded that the universality of the N1 signal and typical doping profiles—for CIGS solar cells fabricated in our laboratory—are most likely linked to the deposition of the standard CdS/ZnO buffer/window layer stack onto the CIGS absorber, resulting in most cases in a transport barrier[10,11,30] (causing a capacitance step) and formation of additional donor-type defects near the interface (reducing net dopant concentration near the interface).[17,18] We also found similar mechanisms in state-of-the-art high-efficiency solar cells fabricated at different institutes.[30] Nevertheless, these results still cannot answer all questions for the devices under investigation and do not necessarily apply to all CIGS solar cells. Such an extensive set of measurements is also certainly not a feasible approach for quick monitoring, loss analysis, and optimization of thin-film solar cells.

In this manuscript, we demonstrate how to assess capacitance measurements of thin-film devices and develop a range of criteria that allow to estimate whether deep defects are evident in the capacitance measurement. We show that a broad parameter space, achieved by exploiting bias voltage and illumination as additional experimental parameters in admittance spectroscopy, helps to verify whether deep

defects can consistently explain features observed in capacitance-based measurements.

In Sections 2 and 3 we discuss a simple analytical model of the capacitance step height in TAS, which helps to distinguish between majority and minority carrier traps and allows to constrain the energetic depth of a trap associated with the respective capacitance step. We find that a defect response and effects of interfaces or additional layers in the device can be distinguished by combining conventional TAS with photoluminescence measurements or by studying the illumination- or voltage-dependence of thermal capacitance spectra. In Section 4, we review the effect of a depleted buffer layer, Schottky-type back contact barrier, or any similar capacitive transport barrier on the temperature-dependent capacitance spectrum of a thin-film device. We focus on differences in the capacitance response between deep defects and such a transport barrier, in particular, with respect to admittance measurements under varying bias voltage and illumination. In Section 5, we then discuss the impact of slowly responding deep trap states on C-V measurements and thus experimental doping profiles, even if they do not produce a direct capacitive response at typical measurement frequencies and temperatures in TAS.

2 | ELECTRON/HOLE TRAP RESPONSE IN CAPACITANCE SPECTROSCOPY

In order to evaluate a given capacitance step in TAS as response of a deep defect, it is instructive to formulate a set of criteria describing under which conditions—and to which effect—such a defect response could be expected. The occupation probability of a defect level under steady-state conditions is determined by the energetic position E_t of the trap with respect to the electron or hole quasi-Fermi level $E_{Fn,p}$ (minority or majority carrier trap, respectively, in a *p*-type CIGS absorber). In experiment, the small-signal capacitance is probed by a small ac voltage modulation with frequency f around a fixed steady-state working point defined by the applied dc bias voltage V_{dc}. Under these conditions, the characteristic capture and emission rate of the trap will limit its ability to follow the external ac modulation at high frequencies. If the trap level cannot follow the ac modulation at high frequencies, its occupation probability becomes time-independent and is determined by the applied dc bias voltage.

As a result, charge modulation in the trap level stimulated by the external ac voltage will add a frequency-dependent capacitance step to the capacitance of the SCR, with inflection frequency f_t determined by capture/emission characteristics of the trap and with vanishing capacitance contribution toward high frequencies. Although we no longer observe a *direct* capacitive contribution at high frequencies originating from charge modulation in the traps, their steady-state occupation modifies the band bending within the SCR, as discussed below. As a result, the SCR capacitance observed at high frequencies will be modified by the presence of deep traps, even if these traps do not follow the ac modulation.

These fundamental considerations have two important practical consequences:

1. The trap level has to cross the quasi-Fermi level, and the inflection frequency has to be within the experimentally accessible measurement range to observe a capacitance step caused by a defect.
2. The SCR capacitance—and thus experimental doping profiles—will be influenced by deep defects even for measurement frequencies well above their inflection frequency, as long as the trap levels have sufficient time to equilibrate with the respective steady-state quasi-Fermi level at a given bias voltage.

We will discuss these two cases individually in more detail in Sections 3 and 5.

Note that the presence of different defects with separate energy levels results in multiple capacitance steps[42] because defects might differ in capture cross-section and because each defect level would cross the Fermi level at a different depth. To simplify the formal calculations below, we nevertheless assume a single defect level. We find empirically that the capacitance spectrum in a given frequency and temperature range is often dominated by a single capacitance step, at least in state-of-the-art Cu-poor CIGS solar cells that do not show a significant concentration of the detrimental N2 defect level. We will discuss this dominant capacitance step as the "main capacitance step" in the following. In most CIGS or similar solar cells, this step would likely be identified as the N1 signature, although, as discussed in the introduction, such a label might be misleading.

We also explicitly ignore capacitance steps related to ohmic series resistance and dielectric freeze-out. Ohmic series resistance causes a breakdown of the measured capacitance value to zero with increasing ac frequency.[43] Assuming a practically low value of series resistance for a solar cell, this occurs at high frequencies of several hundred kilohertz or above, a frequency range that we thus neglect in analysis. At low temperatures, the dielectric response of majority charge carriers in the absorber layer can become too slow to follow ac modulation ("freeze-out") due to reduced free carrier concentration or mobility. The absorber then acts as an insulator, and the capacitance drops to the geometric capacitance $C_{geo} = \varepsilon_0\varepsilon_r/d$, with d being the full absorber thickness. Because the absorber thickness is typically known, a freeze-out can be identified by the absolute value of the high-frequency capacitance.

3 | CROSS-OVER OF TRAP LEVEL AND FERMI LEVEL

In a simple analytical model of the SCR in a one-sided abrupt *p*/*n*-junction, the step in the capacitance spectrum originating from a deep trap can be expressed by the equations[1]

$$C(f) = C_d + \Delta C \frac{1}{1 + (f/f_t)^2}, \quad (1)$$

$$\Delta C = C_d \frac{N_t}{N_d} \left[\frac{1 - \frac{x_t}{x_d}}{1 + \frac{N_t x_t}{N_d x_d}} \right], \quad (2)$$

with width x_d and capacitance C_d of the depletion region (=SCR), the ionized net dopant concentration N_d at the depletion edge, the trap concentration N_t, and the location x_t, where the respective (quasi) Fermi level crosses the trap level. This location is exemplified in Figure 1, which shows band diagrams around the hetero-junction of a CIGS thin-film solar cell with CdS buffer layer and i-ZnO+ZnO:Al window layer for different operating conditions simulated using SCAPS.[44] For simulation parameters, see the Appendix. Note that these diagrams only represent a simplified view because the actual charge in the deep defects was not considered for the correct band bending.

For a majority carrier trap (trap level: blue solid line; hole quasi-Fermi level: red solid line), the cross-over point between trap and Fermi level changes notably with band bending induced by applied bias voltage but is not influenced by illumination.

For minority carrier traps (trap level: blue dashed line; electron quasi-Fermi level: red dashed line) we have to consider the position of the minority carrier quasi-Fermi level $E_{F,n} = E_{F,p} + \Delta\mu$, where $\Delta\mu$ is the quasi-Fermi level splitting in the depletion region caused by illumination or carrier injection under applied bias. In the dark, $\Delta\mu$ is mostly

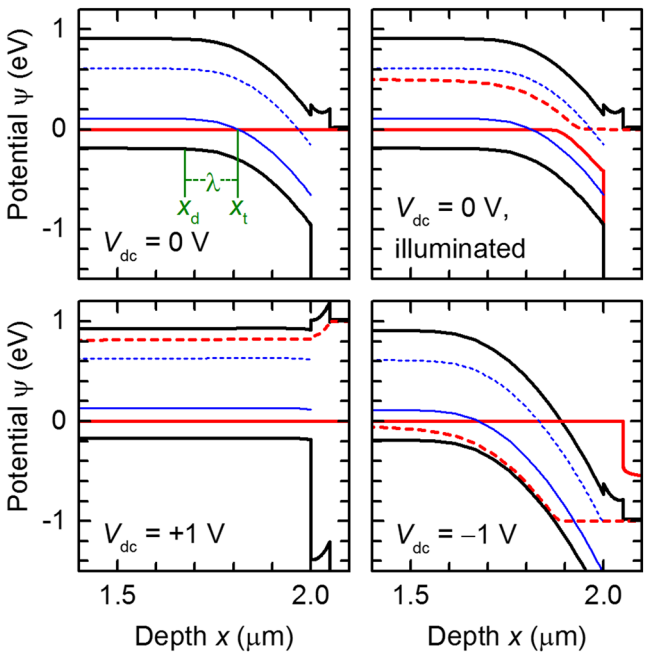

FIGURE 1 Simulated band bending in the depletion region of a CIGS/CdS/ZnO solar cell showing valence and conduction band edges (black solid lines), hole quasi-Fermi level (solid red line), electron quasi-Fermi level (red dashed line), and two defect levels 300 meV above the valence band (solid blue line) and below the conduction band (dashed blue line). Top: without applied bias voltage in the dark (left) and under one-sun illumination (right). Bottom: in the dark with applied bias voltage of +1 V (left) and −1 V (right). Green labels show the SCR edge x_d and cross-over point x_t for a majority carrier trap [Colour figure can be viewed at wileyonlinelibrary.com]

given by the applied bias voltage, which is also the cause for the change in band bending in the SCR. Accordingly, the change in surface potential at the CIGS/CdS interface is comparable with the change in electron quasi-Fermi level in the SCR, and the cross-over point between minority trap level and electron quasi-Fermi level thus only moves slightly with changes in bias voltage. In reality, the finite electric field across the CdS buffer layer means that band bending in the SCR changes somewhat less as a function of applied voltage than the quasi-Fermi level splitting $\Delta\mu$. For the trap level drawn in Figure 1, this causes the electron quasi-Fermi level to shift below the trap level at the interface for reverse bias voltages below approximately −1 V, and the minority trap no longer responds to the ac excitation at all.

For both types of traps, any trap-related capacitance step must disappear for sufficiently high forward bias voltage as shown by Figure 1, bottom left. For minority carrier traps, this might also occur for sufficiently high reverse bias voltages.

Because Equation (2) is somewhat unwieldy in its usual form, the capacitance step height is commonly neglected when extracting information about defect levels from capacitance measurements. For example, the fitting procedure proposed by Weiss *et al.*[21] treats the capacitance step height as a free fitting parameter. That model is intended to correctly separate overlapping capacitance features and identify their distinct apparent activation energies but cannot determine whether a given capacitance feature is in fact a defect nor its quantitative concentration.

In contrast, Walter *et al.*[45] had earlier developed a theoretical model to determine a defect density of states from the derivative dC/df of the capacitance spectrum, which does take into account the magnitude of the capacitance step. This model, however, assumes *a priori* that a given capacitance step is indeed caused by deep defects: The defect concentration is calculated from the capacitance derivative assuming a fixed built-in potential, whereas the energy axis is calculated independently from the attempt-to-escape frequency (obtained from an Arrhenius plot of the temperature-dependent inflection frequencies of the capacitance step). The energetic depth of the defect level and the magnitude of its capacitive contribution—proportional to defect density—are thus decoupled because both are calculated from independent quantities (capacitance and frequency). As a check for self-consistency, the Walter method only produces a common density of states at all temperatures if the correct activation energy is chosen to calculate the energy axis. In the present context, however, this only means that the chosen activation energy correctly describes the temperature-dependence of the capacitance spectrum—it does not necessarily mean that the capacitance step height is consistent with the assumed defect level, in particular, if the capacitance step is not caused by such a defect. Decock *et al.*[46] proposed an improved fitting procedure of the bias-dependent capacitance, which can provide more accurate input values for the Walter method. However, the fundamental separation between defect density and energy still remains. The problem becomes most apparent if we imagine an extremely large capacitance step: In the Walter model, the defect density N_t is directly proportional to dC/df and could then become arbitrarily high. Such a high defect concentration would however pin the

Fermi level at the defect energy E_t and thus limit the built-in potential across the *p*-type CIGS to values close to $E_t - E_{F,p}$, invalidating the calculated relation between defect concentration and capacitance step height for relatively shallow defects.

It is worth pointing out that we do not dismiss the Walter method. In their original paper,[45] Walter *et al*. presented a number of simulations and experimental examples that agree well with our considerations outlined below: Simulations for shallow tail states resulted in very low capacitance values of the order of 10^{-11} F, and experimental capacitance spectra showed dominant defect distributions at energies around 300 meV. Both observations are very different from the N1 signature we focus on in the present paper.

We conclude that it is mandatory to establish the cause of a capacitance step—i.e., deep defects or not—before attempting to quantify any defect parameters using standard methods like the Walter method. In the following, we will show that the capacitance step height provides a useful criterion for the correct interpretation and assignment of capacitance steps in admittance spectroscopy, in particular, if the corresponding activation energy is around 100 meV or lower.

It is convenient to express Equation (2) not in terms of capacitance but in terms of corresponding equivalent depth $x = \varepsilon_0\varepsilon_r/C$. Rearranging Equation (2) then yields

$$\Delta x = \frac{\varepsilon_0\varepsilon_r}{C_d} - \frac{\varepsilon_0\varepsilon_r}{C_d + \Delta C} = \lambda\frac{N_t}{N_d + N_t} < \lambda, \tag{3}$$

where $\lambda = x_d - x_t$ is the distance over which band bending in the depletion region leads to a cross-over of (quasi) Fermi level E_F and trap level E_t, see Figure 1. The depth-dependent electrostatic potential in the depletion region is found by integrating the electric field F, which is linked to the local net charge density $\varrho(x)$ by the Poisson equation $dF/dx = \varrho(x)/(\varepsilon_0\varepsilon_r)$. The required band bending over the SCR to ensure a cross-over of Fermi level E_F and trap level E_t for a *majority* carrier trap is equal to the energy difference $E_t - E_F$. Assuming a constant bulk net doping N_d, the distance λ is then given by[1]

$$\lambda = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q^2N_d}(E_t - E_F - kT)} = \sqrt{2}L_D\sqrt{\frac{E_t - E_F}{kT} - 1} \tag{4}$$

with Debye screening length L_D, Boltzmann constant k, and temperature T. The additional term kT in the square-root accounts for the exponential tail of the majority carrier distribution extending into the depletion region. From Equation (4), we find that a large step in equivalent depth is only possible for low bulk doping and/or deep trap levels. Equation (4) only provides useful insight if the correct dopant concentration and Fermi energy of the device is known, which is not necessarily the case for a simple admittance measurement. For theoretical considerations and for ease of evaluating an experimental capacitance spectrum, we can rewrite Equation (4) to find the maximum value of λ for a given trap energy E_t and any constant dopant concentration. Using the relation $N_d = p = N_v\exp(-E_F/kT)$ for the bulk majority carrier concentration, where N_v is the effective density of states at the valence band edge, we find an upper limit of the capacitance step height as a function of energetic depth of the majority carrier trap (see Appendix C) as

$$\Delta x < \lambda \le \Delta x_{max} = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q^2N_v}kT}\exp\left(\frac{E_t}{2kT} - 1\right). \tag{5}$$

Although Equation (5) no longer requires knowledge of the actual doping concentration of the device, eliminating the experimental dopant concentration N_d in the derivation of Equation (5) from Equation (4) introduces some complications: By assuming $N_d = p$, we ignore incomplete ionization of dopants at low temperatures. According to van Opdorp,[47] however, this only modifies the built-in potential and not the bias-dependent band bending relevant for Equations (4) and (5) because shallow acceptors will mostly be ionized within the SCR anyway. Equation (5) also eliminates the dependence on bulk Fermi level by implicitly assuming that Fermi level for which the capacitance step height would be maximal. In that sense, Equation (5) is indeed only applicable to estimate the *maximum* step height Δx or *minimum* trap depth. Furthermore, Equation (5) requires an assumption of N_v, which is not known precisely. In contrast, Equation (4) only requires the experimental doping concentration but in turn only yields the energetic position of the trap level relative to the bulk Fermi level.

Figure 2 shows the limiting value Δx_{max} (solid lines) as a function of energetic depth of the trap level and sample temperature, assuming typical values for CIGS of $\varepsilon_r = 10$ and $N_v = 1.5\times10^{19}$ cm^{-3} at 300 K (for an effective relative hole mass of 0.7) with a temperature dependence of $N_v \propto T^{3/2}$. As main conclusion, we find that fairly shallow traps are extremely challenging to observe in TAS. If, for example, a

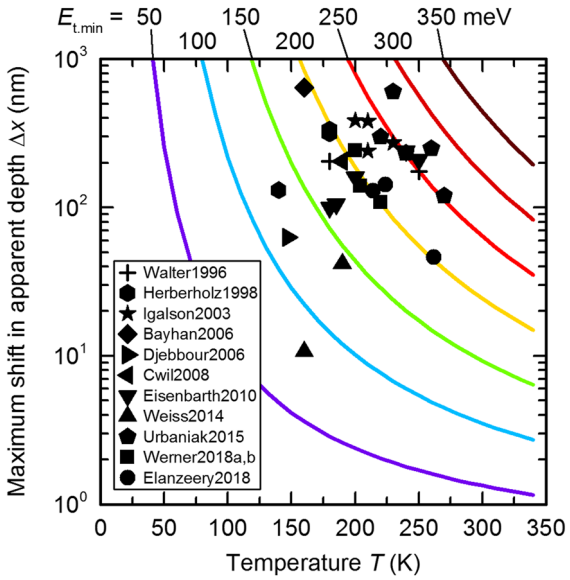

FIGURE 2 Solid lines show the maximum step height in apparent depth Δx as a function of temperature T, calculated for different deep trap levels given above the graph and assuming $\varepsilon_r = 10$ and $N_v = 1.5 \times 10^{19} cm^{-3}$ $(T/300K)^{3/2}$. Symbols show Δx extracted from experimental capacitance spectra published for different chalcopyrite and kesterite thin-film solar cells in Ref.[6,10,19,21,25,30,45,48-52] [Colour figure can be viewed at wileyonlinelibrary.com]

capacitance step is resolved in a typical temperature range of up to 200 K, the capacitive response of a shallow defect level 100 meV above the valence band would only modulate the apparent depth by less than 10 nm. Note that the capacitance step height ΔC in experiment is typically found to be virtually independent of temperature or to even increase with increasing temperature. Thus, the highest temperature where a capacitance step is still resolved typically imposes the strictest limit to the energetic depth of the trap.

In comparison with the theoretical limit for a majority carrier trap according to Equation (5), black symbols in Figure 2 show a range of experimental values for the step height in apparent depth Δx extracted from the main capacitance step in experimental capacitance spectra published in literature,[6,10,19,21,25,30,45,48-52] for different chalcopyrite and kesterite thin-film solar cells. Most data points require a trap level at least 200 or 300 meV above the valence band edge in order to consistently attribute the main capacitance step, or N1 signature, to a deep majority carrier trap. Note that reported thermal activation energies for the N1 signature are usually below 200 meV,[20] although slightly higher values are certainly possible.[30] Although differences between actual energetic depth and thermal activation energy could be explained by the Meyer-Neldel rule,[36,37,53] a limiting value imposed by Equations (4) or (5) on the actual depth of a trap provides more useful information for the interpretation of defect spectra than the thermal activation energy alone. For example, we recently demonstrated that low-temperature photoluminescence spectra of high-quality absorbers show no noticeable defect luminescence at transition energies a few hundred meV below the bandgap.[30] However, we could not fully rule out defects as origin of the N1 signature in these measurements because the thermal activation energy from TAS was too low for most samples and potential defect luminescence could thus have been obscured by the broad peak of transitions from band edges or shallow dopants.

In this regard, we find that a single measurement is insufficient to elucidate the nature of a capacitance step: The maximum capacitance step height cannot directly rule out defects because the actual energetic depth of the trap could in principle really be significantly deeper than expected from TAS measurements. Nevertheless, confining potential trap levels to energetic positions deeper within the bandgap than their thermal activation energy provides useful insight for further characterization, for example, by photoluminescence or bias-dependent admittance spectroscopy. In particular, a deeper trap level means that its related capacitance step will disappear already at moderate forward bias because the cross-over point x_t lies closer to the absorber/buffer interface.

For minority carrier traps, the majority carrier Fermi level $E_{F,p} \approx E_F$ in Equation (4) needs to be replaced with the minority carrier quasi-Fermi level $E_{F,n} \approx E_F + \Delta\mu$. Equations (4) and (5) are thus still applicable, but the effective energetic separation of the trap level from the valence band is artificially reduced to $E_t - \Delta\mu$. Because $\Delta\mu$ in the dark mainly depends on bias voltage, the capacitance step height then also changes with applied voltage. Note that this does not contradict our earlier observation that the cross-over point x_t of electron quasi-Fermi level and trap level does not change significantly with applied bias voltage because the capacitance step height, Equation (3), is determined by $\lambda(V) = x_d(V) - x_t$ rather than x_t.

From the preceding discussion, it becomes apparent that bias-dependent capacitance spectra are a useful tool to verify whether capacitance steps attributed to potential deep traps indeed disappear under flatband conditions and to distinguish between majority and minority carrier traps depending on the bias-dependence of the cross-over point between trap level and respective quasi-Fermi level. In literature, Eisenbarth *et al.*[6] find that the capacitance step height remains constant at $\Delta x \approx$ 200 nm only up to voltages close to the flatband voltage, but the capacitance step remains present even for higher voltages. Herberholz *et al.*[19] equally find quite similar step heights (315-335 nm) for several bias voltages, and we recently also published a constant step height of 140-150 nm up to 0.8 V.[10]

Figure 3 shows experimental frequency-dependent capacitance spectra representative of typical CIGS thin-film solar cells, plotted both as equivalent depth $x = \varepsilon_0\varepsilon_r/C$ and as capacitance C for different applied bias voltages and a temperature of 100 K. This temperature was exemplarily chosen for a clear representation to ensure that the inflection frequencies of the capacitance step lie well within the experimental frequency range. The standard TAS measurement as a function of temperature at zero bias voltage (not shown here) resulted in a capacitance step with activation energy E_a = 80-90 meV (resolved in a temperature range of approximately 50-200 K), comparable with the typical N1 signature.

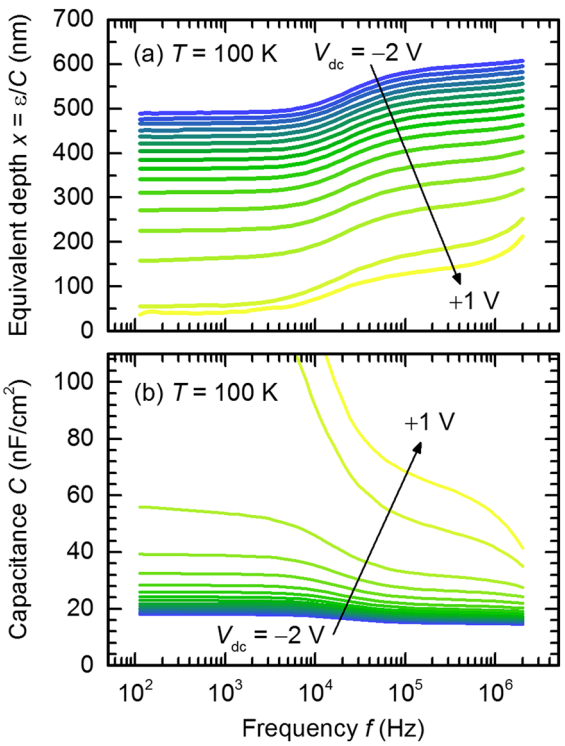

FIGURE 3 Frequency-dependent capacitance spectra of a CIGS solar cell plotted as (a) equivalent depth $x = \varepsilon_0\varepsilon_r/C$ and (b) capacitance for different applied bias voltages V_{dc} from −2 to +1 V in the dark at T = 100 K [Colour figure can be viewed at wileyonlinelibrary.com]

The main observation from Figure 3 is that the capacitance step height for this particular sample always corresponds to a change of equivalent depth of Δx = 110±10 nm, independent of experimental condition. Note that this observation is fairly obvious from the *apparent depth* shown in Figure 3(a) but not readily apparent from the typical *capacitance* spectrum shown in Figure 3(b). If a discreet majority carrier trap level was responsible for this capacitance step, the resulting capacitance step height would indeed be independent of bias voltage over a wide range, compare Equation (4). As discussed in Section 3 above, however, we would expect this capacitance step to disappear close to flatband conditions within the absorber (Figure 1, bottom left), which is not the case in this experiment. Furthermore, comparing the experimental value of Δx = 110±10 nm observed at temperatures up to 200 K with Equation (5), we find that a potential majority carrier trap would need to be at least 180 meV away from the valence band edge to explain this capacitance step. Using Equation (4) and a dopant concentration of at least 5×10^{15} cm^{-3} obtained by C-V analysis[see inset of Figure 6(a)], this energetic depth increases to at least 200 meV. These limits are at least twice as high as the experimental activation energy of 80-90 meV obtained from TAS. For minority carrier traps as alternative explanation of this capacitance step, we expect the capacitance step height to vary with bias voltage as discussed above, which apparently is not the case here. Based on these bias-dependent capacitance spectra, it is thus extremely unlikely that defects could explain the main capacitance step in TAS experiments presented here.

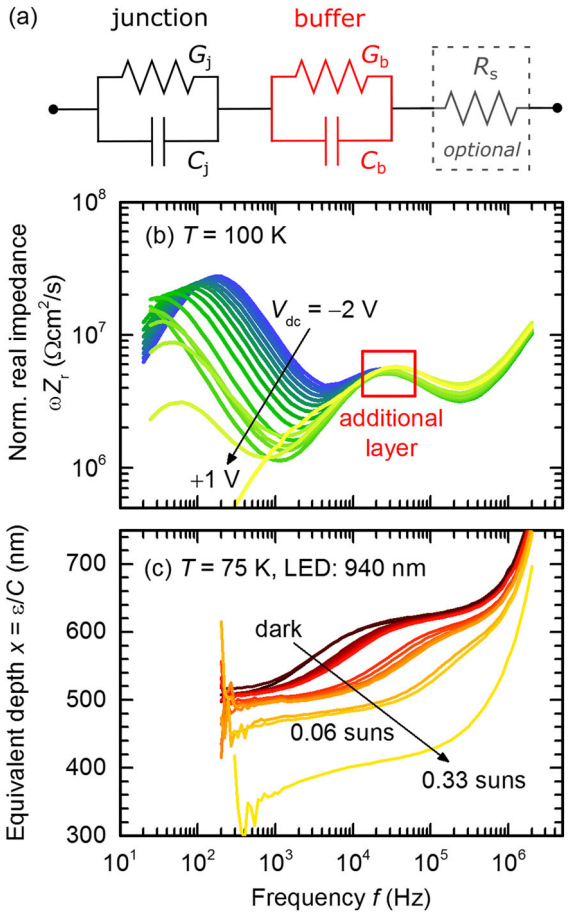

FIGURE 4 (a) Serial electrical equivalent circuit of junction, buffer layer, and lumped series resistance. (b) Frequency-dependent normalized real impedance for bias voltages between −2 and +1 V at T = 100 K. (c) Frequency-dependent capacitance spectra under illumination with an IR-LED (peak wavelength 940 nm) at T = 75 K without applied bias voltage. The equivalent illumination intensity given in the graph is estimated from the measured photocurrent density [Colour figure can be viewed at wileyonlinelibrary.com]

4 | EFFECT OF CAPACITIVE TRANSPORT BARRIERS ON DEVICE CAPACITANCE SPECTRA

Transport barriers due to a non-ohmic back contact or buffer and/or window layers have been proposed as alternative explanations for the N1 signature.[6,8,10,11,22,30,34,35] Below we will show that such barriers in a thin-film solar cell not only explain the N1 signature in TAS more naturally than defects but also agree with voltage- and illumination-dependent capacitance spectra. Certain evidence suggests that the buffer layer[10,11] or interfaces between buffer and window layers[30] are responsible for this barrier in our own measurements. Note that any other (interfacial) layers, band offsets, or non-ohmic contacts could be alternative possibilities for transport barriers in the device. For the sake of brevity, we will use the general term "barrier layer" throughout this section to refer to any such transport barriers or interlayers with capacitive impedance contributions.

A transport barrier or additional layer in the device can be modeled as an additional electrical circuit element in series with the *p/n* junction of the solar cell, as sketched in Figure 4(a). One of these elements represents the barrier layer (G_b and C_b); the other element originates from the SCR of the *p/n* junction (G_j and C_j). The lumped series resistance R_s in Figure 4(a) explains a breakdown of the measured capacitance at high frequencies but will be ignored in this manuscript. The effective frequency-dependent total capacitance of such a device shows a step[6,10,35] with inflection frequency

$$f_t(T) = \frac{1}{2\pi}\frac{G_b + G_j}{C_b + C_j} \approx \text{const} \times G_b(T), \quad (6)$$

even if all individual parameters G_b, G_j, C_b, and C_j are independent of frequency. For the right-hand-side of Equation (6), we have assumed that the barrier and junction capacitances only have a week temperature dependence and that the barrier layer is much more conductive than the (blocking) junction, $G_b \gg G_j$. As such, the temperature dependence of the inflection frequency is mainly determined by the conductivity of the barrier layer. If this conductivity is at least approximately thermally activated, the thermal capacitance spectra resulting from a barrier layer in series with the main junction will potentially look identical to those caused by the response of a deep defect level. For comparison, the temperature-dependent inflection frequency for a defect response is typically given by[1]

$$f_{\mathrm{t.def}}(T) = \frac{1}{2\pi} v_{\mathrm{th}} N_{\mathrm{c,v}} \sigma_{n,p} \exp\left(-\frac{E_{\mathrm{a}}}{kT}\right) \approx \mathrm{const} \times T^2 \exp\left(-\frac{E_{\mathrm{a}}}{kT}\right), \quad (7)$$

with thermal velocity v_{th}, effective density of states $N_{\mathrm{c,v}}$ in the conduction or valence band, and electron or hole capture cross-section $\sigma_{n,p}$ and activation energy E_{a} of the defect. The quadratic temperature term accounts for the temperature dependence of thermal velocity and effective density of states.

The *series connection* of barrier and junction elements in Figure 4(a) means that each element adds one peak at a characteristic frequency $f_{\mathrm{char}} = G_{\mathrm{b,j}}/(2\pi C_{\mathrm{b,j}})$ to the total impedance spectrum $Z(f)$. Note that these characteristic frequencies in the impedance spectrum, which are indeed specific for each individual layer, are *not* the same as the inflection frequency in the corresponding capacitance spectrum, which, according to Equation (6), depends on both elements. Accordingly, the impedance spectrum is more appropriate to study individual layers than the commonly chosen admittance or capacitance spectrum. More precisely, we find that the normalized real impedance spectrum $Re\{\omega Z(f)\}$, equivalent to the real part of the inverse complex capacitance, is typically most suited to identify both contributions from junction and buffer layer in our thin-film devices.[10] The reason is that the height of a characteristic peak in the impedance spectrum is proportional to the resistance of that circuit element, which differs drastically between barrier layer and junction, whereas the peak height is proportional to the inverse capacitance in the $\omega Z(f)$ spectrum.

Figure 4(b) shows such normalized real impedance spectra for different applied bias voltages at a temperature of 100 K, which is the same raw data represented as capacitance spectra in Figure 3. We clearly observe two distinct peaks, which react differently to changes in bias voltage:

1. Junction: The low-frequency peak (below 1 kHz) varies in magnitude and peak frequency as a result of the voltage dependence of SCR capacitance, diode current, and shunt[54] current.
2. Barrier layer: The second peak around 30 kHz is virtually unaffected by bias voltage. Because most of the applied voltage drops over the SCR ($G_{\mathrm{b}} \gg G_{\mathrm{j}}$), we indeed do not expect to see a notable voltage dependence for the barrier layer. Unlike a defect, a barrier layer would also explain why the corresponding capacitance step does not disappear at voltages above the flatband voltage in the absorber.

Such insight into individual parameters of the full device is indispensable to locate the origin of a capacitive feature. For example, Niemegeers *et al.*[55] found earlier that the N1 capacitance step is indeed linked to the CdS buffer layer but had to propose a high density of interface trap states to get a reasonable agreement between experimental capacitance inflection frequencies and those calculated for a simplified theoretical model of electron transport within the CdS layer. From impedance spectra (see Ref.[10] for more details), we find that such interface states are not present in the devices presented here and that transport across the CdS buffer layer alone explains the N1 signature in our case.

For further confirmation, we use a collimated infrared LED (peak wavelength 940 nm) to illuminate a CIGS solar cell during admittance measurements. Figure 4(c) shows capacitance spectra as equivalent depth at a temperature of 75 K and a bias voltage of practically zero (small deviations up to 40 mV due to illumination). The illumination intensity was adjusted with a set of neutral density filters and equivalent intensity values given in Figure 4(c) were estimated from the measured photocurrent density. Upon illumination, the inflection frequency of the main capacitance step shifts to higher frequencies, approximately proportional to the illumination intensity. This can be understood as a photoconductive effect: Injection of electrons from the absorber into the buffer layer under illumination increases the electron concentration in the buffer layer and thus increases its conductivity. According to Equation (6), the inflection frequency of the main capacitance step then shifts proportional to the increased buffer conductance. For a deep defect, see Equation (7), a linear shift of the capacitance step would require either a (linearly) higher capture cross-section or (logarithmically) shallower defect activation energy with increasing excess carrier density. Although the latter might occur for exponential defect distributions in band tails,[56] such extended defects near the band edges are not consistent with the voltage-independent and fairly large capacitance step height discussed in Section 3, which would require a deep but discreet or fairly narrow defect distribution. We thus conclude that the mere presence of a barrier layer is the more likely origin of the main capacitance step in admittance spectroscopy, rather than deep defects.

Besides the different interpretations of the inflection frequency discussed above, barrier layer and defect also differ in the interpretation of the capacitance values before and after the capacitance step. Here, the correct identification of the SCR capacitance is of highest importance, in particular for the correct choice of measurement condition for the determination of doping profiles from C-V measurements: For a capacitance step caused by a defect, the SCR capacitance is equal to the *high-frequency limit*, compare Equation (1). If the capacitance step is due to a barrier layer, however, the SCR at least approximately equals the *low-frequency limit* of the capacitance.[10]

5 | IMPACT OF DEEP TRAP LEVELS ON EXPERIMENTAL APPARENT DOPANT PROFILES

Apparent doping profiles for CIGS are usually found to be depth-dependent,[6,18,23-26] and the increase of apparent doping concentration toward applied reverse bias is typically attributed to the presence of deep defects.[4] In Sections 3 and 4, we have argued that deep defects are often not responsible for the main capacitance step observed in TAS. Nevertheless, as discussed in Section 2, changes in the steady-state occupation probability of deep traps within the absorber layer could still influence a C-V measurement of the doping concentration, even if these traps are too slow to be detected in a

TAS measurement. In addition, metastable changes from acceptor- to donor-type defects, or vice versa, as a reaction to different biasing conditions could result in a change of SCR capacitance over time.[57] To correctly distinguish between a *real* depth-dependent net dopant concentration and an *apparent* depth dependence caused by the different occupation probability of deep defect states in the SCR, the sweep rate of the dc voltage must be chosen carefully. To assess the physical net dopant concentration, C-V measurements can be performed with fast voltage sweep rates[58] to ensure that traps do not change their charge state even over the full duration of the C-V measurement. Here we follow an alternative approach, which in addition also provides information about the defects involved in these dynamic processes: The device is kept at a forward bias voltage close to the flatband voltage for 120 s, which ensures that the charge state of all defects reaches a well-defined steady state, that is, all defects at a given energy are either fully occupied or fully empty (depending on the type of defect) throughout the SCR. The bias voltage is then instantaneously set to the value of interest, and the resulting capacitance transient monitored as a function of time. Figure 5 shows these transients at a frequency of 10 kHz and T = 300 K expressed as apparent SCR width $x = \varepsilon_0\varepsilon_r/C$ for bias voltages in a range of +0.7 to −3.0 V.

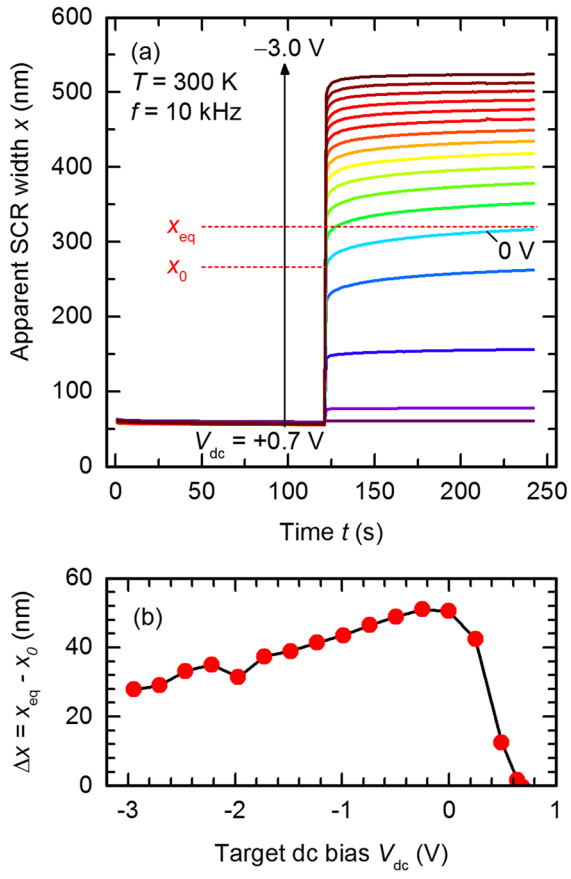

FIGURE 5 (a) Time-resolved evolution of the apparent SCR width $x = \varepsilon_0\varepsilon_r/C$ after keeping the sample above 0.7 V forward bias for 120 s and then applying a bias voltage between +0.7 and −3.0 V. Different transients nominally differ by 0.25 V, although the actual voltage in forward bias is reduced due to the high current through the device. (b) Change in apparent SCR width during the transient as a function of applied dc bias voltage [Colour figure can be viewed at wileyonlinelibrary.com]

In Figure 5, we clearly observe an initial instantaneous change in apparent SCR width, with respect to the time resolution of 1 s in these measurements, whenever the bias voltage is changed. We attribute this initial change to the quasi-instantaneous reaction of the majority carrier concentration, and the corresponding initial apparent width x_0 thus corresponds to the real SCR width of a hypothetical device free of deep defects. Such a hypothetical device would have exactly the same net dopant concentration throughout the absorber as the real device, but all defects would appear to be shallow. A Mott-Schottky plot constructed from the initial value x_0 and its bias dependence thus yields the actual net dopant concentration at the depth of the SCR edge, shown in Figure 6(a). After the initial redistribution of majority carriers, however, we indeed observe a slow charge equilibration of defects within the SCR for most bias voltages, and the apparent SCR width increases to its steady-state value x_{eq} over timescales of several seconds to minutes.

Our measurements thus clearly show evidence for the presence of slow or metastable deep trap states, and their impact on extracted doping profiles needs to be considered. In Figure 6, we compare a "slow" C-V measurement (−0.2 V steps each 30s) with an idealized "fast" measurement, where we take the initial capacitance $C = \varepsilon_0\varepsilon_r/x_0$ from the capacitance transients in Figure 5(a) as SCR capacitance of an ideal device free of the influence of deep defects. Blue circles in Figure 6(a) represent the experimental Mott-Schottky plot and corresponding apparent doping profile of the slow C-V measurement. The Mott-Schottky plot clearly deviates from a linear relation with a single well-defined slope, and the apparent doping profile (see inset) is thus not constant. In the conventional approach, such a curved graph is expected from the voltage-dependence of the cross-over point of Fermi level and trap level: In sufficient forward bias, the trap level never crosses the Fermi level, and the net ionized charge concentration in the SCR is the same as in the bulk. In sufficient reverse bias, the Fermi level crosses the trap level close to the SCR edge, $x_t \approx x_d$ in Equation (2), and the net ionized charge concentration in the SCR differs from that in the bulk by the deep trap concentration. The deep trap and net dopant concentrations could then, in principle, be estimated from the minimum and maximum values of the apparent dopant concentration in forward and reverse bias, respectively.

For most CIGS devices measured in our lab, however, this simplified model leads to several inconsistencies:

1. The apparent transition between two different slopes in the Mott-Schottky plot occurs between 0 and −1 V, see dotted lines in Figure 6(a). From the capacitance transients shown in Figure 5 for the same sample, however, we would already expect a significant contribution of deep defects over most of the fitting range of the forward bias slope in Figure 6(a).
2. The apparent dopant concentration shown in the inset of Figure 6 (a) does not saturate, which indicates that the Mott-Schottky plot is in fact *not* straight, not even in strong reverse bias. This is not easily apparent from the Mott-Schottky plot itself, where the

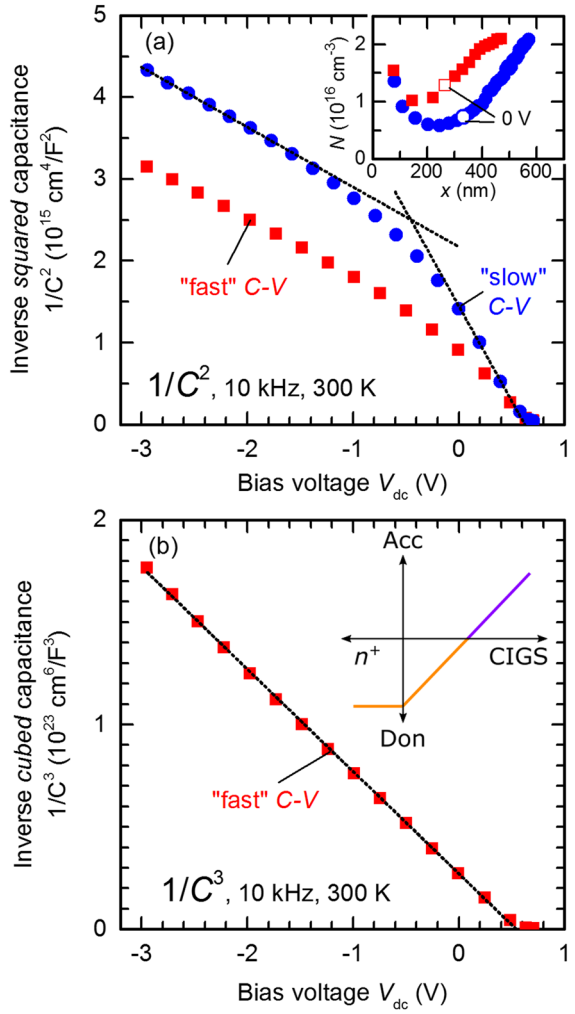

FIGURE 6 (a) Mott-Schottky plot $1/C^2$ vs V_{dc} for "slow" (blue circles, −0.2 V steps each 30 s) and "fast" (red squares, initial capacitance value from capacitance transient) C-V measurements at f = 10 kHz and T = 300 K. Dotted lines are linear fits. The inset shows the resulting apparent doping profiles, the zero-bias point is indicated by the open symbols. (b) Inverse cubed capacitance $1/C^3$ vs V_{dc} for the "fast" C-V data with a linear fit (dotted line). The inset shows a qualitative sketch of the net acceptor (violet) and donor (orange) concentration of a graded junction at the interface between *p*-type CIGS bulk and *n*-type buffer/window layers [Colour figure can be viewed at wileyonlinelibrary.com]

linear fit in reverse bias (dotted line) by eye appears to describe the experimental data quite well.

3. The "fast" C-V data reconstructed from the capacitance transients, red squares in Figure 6(a), should be free of the influence of deep defect, but the corresponding Mott-Schottky plot is also not straight.

Similar to the discussion in Section 3, a square-root-like voltage dependence of the SCR width—and thus a linear Mott-Schottky plot of $1/C^2 \propto x_d^2$ vs V_{dc}—originates from integrating Poisson's equation twice with a constant charge concentration resulting from a *depth-independent* net dopant concentration. For a graded doping profile, for example, the linearly graded profile sketched in the inset of Figure 6(b), the net dopant concentration near the junction increases linearly with depth. In that scenario, the inverse cubed capacitance $1/C^3$, rather than the inverse squared capacitance $1/C^2$, would form a straight line as a function of applied bias voltage.[47] This is indeed the case here, as demonstrated by the "fast" C-V data and corresponding linear fit shown in Figure 6(b).

A straight plot of $1/C^3$ vs V_{dc} is a useful hint to consider a doping gradient but in itself is not a definite proof for a graded dopant concentration near the absorber/buffer junction. Nevertheless, such a reduced net doping in the absorber close to the hetero-junction is able to conveniently explain a number of experimental findings:

1. The increase in SCR width during experimental capacitance transients, Figure 5(b), is less pronounced in reverse bias. This could be related to the higher net dopant concentration away from the junction, and a smaller displacement of the SCR edge could then accommodate the same amount of charge originating from a changed occupancy of the same number of deep traps. Note that the change in *capacitance* would always be lower in reverse bias even for constant shallow and deep defect distributions—$dC \propto C_d$, Equation (2)—but this does not apply to the change in *apparent depth* and thus SCR width—see Equation (3).
2. Hall measurements of CIGS absorbers yield higher dopant concentrations than C-V analysis of solar cells fabricated from comparable absorbers.[18,40] This could indicate that the reduced net dopant concentration near the junction in CIGS solar cell is a result of the solar cell fabrication process.
3. Photoluminescence measurements of CIGS absorbers before and after deposition of a CdS buffer layer suggest that the donor/acceptor compensation ratio at the CIGS surface increases upon CdS deposition while the net doping concentration decreases.[17]

The physical reason for such a doping gradient might be related to the multilayered architecture of a thin-film solar cell, where several different layers are deposited subsequently. In particular, we assume that Cd—or Zn in the case of devices with Zn(O,S) buffer layer—diffuses into the absorber and occupies sites on the Cu lattice. This is predicted to form a donor level in CIGS when Cd occupies a copper site (Cd_{Cu})[59-61] and which would additionally reduce the concentration of copper vacancies (V_{Cu}) as dominant acceptor state in CIGS.[62-65]

6 | DISCUSSION

For a meaningful characterization of thin-film solar cells using capacitance-based measurement techniques, it is important to correctly identify the underlying mechanisms behind steps in the experimental capacitance spectra. The correct interpretation of a capacitance spectrum changes dramatically whether a capacitance step is caused by deep defects or simply is a circuit response due to transport barriers or additional layers in the device stack.

Unfortunately, deep defects and buffer layers are difficult to distinguish in a classical admittance spectroscopy measurement because they result in functionally identical capacitance steps. In fact, it is common practice to record temperature-dependent capacitance spectra only at zero bias voltage and extract a thermal activation energy from an Arrhenius plot of the inflection frequencies of a given capacitance step. Other characteristics of such a capacitance step are often not taken into account, although they might be able to shed more light on the mechanisms responsible for this capacitance step. Under these circumstances, it is virtually impossible to distinguish between deep defect and circuit response.

Based on a simple analytic model of band bending in the depletion region, we demonstrated that the voltage-dependent height of a capacitance step is most conveniently expressed as a change of apparent depth $\Delta x = \varepsilon_0\varepsilon_r/C$ and is a helpful measure to identify the physical origin of a capacitance step. If traps are responsible for the capacitance step, the voltage-dependent step height allows to distinguish between majority and minority carrier traps, and the magnitude of the change in apparent depth defines a strict lower limit to the energetic depth of the trap, at least in the case of majority carrier traps. We found that fairly shallow defects below 150 meV will be extremely difficult to resolve in TAS. Furthermore, deep defects can be ruled out if the capacitance step remains present at high forward bias around the flatband voltage. On the other hand, the mere presence of a transport barrier due to a non-ohmic back contact or additional layers in the device stack naturally leads to a capacitance step. In this case, the impedance spectrum multiplied by frequency is more convenient than the admittance spectrum because it allows to isolate contributions from individual layers within the device.

We applied these criteria to experimental capacitance spectra of typical CIGS solar cells with CdS buffer layer and i-ZnO/ZnO:Al double window layer, which show the well-known N1 signature as main capacitance step. We found that deep defects would need to be fairly deep majority carrier traps, and their energetic depth would need to be severely underestimated by the thermal activation energy from an Arrhenius plot in order to explain experimental capacitance spectra at moderate bias voltage. Even defects with these properties could not explain why the N1 signature is still visible at high forward voltages. A transport barrier, for example, a depleted buffer layer, on the other hand, would naturally explain all experimental capacitance spectra. We further demonstrated that photoconductive effects in the buffer layer result in a linear shift of inflection frequency with illumination intensity, which would not be the case for a discreet defect level. We conclude that the main capacitance step in our devices, which agrees well with the N1 signature, is most plausibly explained by the presence of a buffer layer connected in series to the *p/n* junction of the device and is not related to any deep defects.

Although we thus do not observe any capacitance steps related to deep defects, such defects are still present in our CIGS devices: capacitance transients upon changing the applied bias voltage from a controlled initial state near flatband conditions revealed a quasi-instantaneous response by majority carriers at the SCR edge, followed by a comparably slow expansion of the SCR over timescales of many seconds or even minutes. We attribute this expansion to a slow equilibration of deep trap states, which now cross the Fermi level. The response time of these trap states, however, is too slow to be observed in TAS measurements in a typical frequency range above several hertz. Nevertheless, these slow trap states have a noticeable influence on experimental apparent doping profiles determined by C-V measurements, if the voltage sweep rate is slow enough to allow (at least) partial equilibration of deep traps within the measurement duration.

Mott-Schottky plots constructed from the capacitance transients, however, showed that typical depth-dependent apparent doping profiles in CIGS devices are only partially explained by these deep traps. Rather, the net dopant concentration near the buffer/absorber interface is physically reduced in the presence of a CdS or Zn(O,S) buffer layer, resulting in a graded doping profile at the electronic junction. In this case, the inverse *cubed* capacitance, rather than the inverse *squared* capacitance, is expected to yield a straight line, which was indeed observed for our CIGS devices. Thus, changes in the absorber material during processing of the solar cell front layers or during operation and aging of the device must be considered in the correct interpretation of doping profiles obtained from C-V analysis in any heterojunction solar cell: The true bulk dopant concentration in these devices might be considerably different than expected.

7 | CONCLUSIONS

The height of a capacitance step is often overlooked in the analysis of capacitance spectra in TAS, although this measure can provide a wealth of information about the origin of a capacitance step. This was shown to be particularly true if temperature-dependent capacitance spectra are recorded over a range of applied bias voltages. Additionally, illumination can be exploited as additional experimental parameter to consolidate the analysis. If the capacitance step is caused by a deep defect, the capacitance step height allows to distinguish minority and majority carrier traps and provides an independent measurement of the energy level of the trap. Even if such measurements might rule out defects as origin of any steps in experimental capacitance spectra, trap states with response times too slow to follow the ac modulation at all might however still be present in the absorber. These states might still have a significant influence on apparent doping profiles determined by a C-V measurement, although they do not appear in any capacitance spectrum. For this reason, time-resolved capacitance measurements that can resolve long transients over timescales of several seconds or more, equivalent to characteristic frequencies well below 1 Hz, are a useful addition to standard TAS measurements to study both shallow net dopant concentration and deep trap states in the absorber film.

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APPENDIX A

EXPERIMENTAL DETAILS

Polycrystalline CIGS absorbers are grown on Mo-coated soda-lime glass in a three-stage co-evaporation process. Samples chosen exemplarily for the electrical analysis have copper contents of [Cu]/([Ga]+[In]) ≈ 0.98-0.99 and gallium contents of [Ga]/([Ga]+[In]) ≈ 0.28-0.37 as determined from energy-dispersive X-ray measurements. We obtain comparable trends also for absorbers with different composition. Solar cells with an active area of 0.2-0.5 cm^2 and efficiencies above 16% under standard test conditions are fabricated with a CdS buffer layer deposited by chemical bath deposition, an rf-sputtered i-ZnO/ZnO:Al double window layer, and a Ni/Al front contact grid. The admittance spectrum is recorded in a frequency range of f = 20 Hz - 2 MHz with ac voltage amplitude of 30 mV rms, with the sample mounted in the dark in a closed-cycle cryostat. A temperature sensor glued onto an identical glass substrate besides the solar cells is used to estimate the actual temperature of the solar cell. For voltage-dependent measurements, the actual dc voltage is measured across the terminals of the device to avoid artifacts due to the finite input resistance of the LCR meter.

APPENDIX B

SIMULATION PARAMETERS

Simulations of band bending in CIGS thin-film solar cells were run in SCAPS v3.3.05[44] at a temperature of 300 K and ac frequency of 1 MHz using the material parameters summarized in Table B1. We assume flatband conditions at both back and front contacts. The trap levels drawn in Figure 1 and their corresponding charge state were not considered in the simulation. Illuminated solar cells are simulated with a 1-sun AM1.5G spectrum and absorption files for CdS and ZnO available in SCAPS, and assuming an absorption constant A = 10^5 $cm^{-1}eV^{0.5}$ for CIGS.

APPENDIX C

MAXIMUM STEP HEIGHT

Calculating the maximum step height from Equation (4) requires knowledge of the correct dopant concentration. By substituting $N_d = p = N_v\exp(-E_F/kT)$ we obtain

$$\lambda = \sqrt{\frac{2\varepsilon_0\varepsilon_r(E_t - E_F - kT)}{q^2 N_v \exp(-E_F/kT)}} = \sqrt{\frac{2\varepsilon_0\varepsilon_r kT}{q^2 N_v}}\sqrt{[\eta_t - \eta_F - 1]\exp(\eta_F)}, \quad \text{(C1)}$$

where η_t and η_F are the trap and Fermi energies E_t and E_F, respectively, normalized by kT. This step height λ is largest for that Fermi level, which maximizes the argument $[\eta_t - \eta_F - 1]\exp(\eta_F)$ in the second square-root. Taking the derivative with respect to η_F this is fulfilled if

$$[\eta_t - \eta_F - 2]\exp(\eta_F) = 0, \quad \text{(C2)}$$

or, because $\exp(\eta_F)$ is always non-zero, $\eta_F = \eta_t - 2$. The capacitance step for a sample with constant dopant concentration and majority trap level E_t is thus largest if the Fermi level is $2kT$ below the trap level. Evaluating Equation (C1) at this Fermi level then results in Equation (5).

TABLE B1 Material parameters for the different layers of a CIGS thin-film solar cell.

Parameter	CIGS	CdS	i-ZnO	ZnO:Al
Thickness [nm]	2000	50	80	200
Bandgap [eV]	1.1	2.4	3.4	3.7
Relative dielectric permittivity	10	10	9	9
Electron affinity [eV]	4.35	4.25	4.45	4.45
Eff. DOS conduction band [cm^{-3}]	7.94×10^{17}	2.2×10^{18}	2.2×10^{18}	2.2×10^{18}
Eff. DOS valence band [cm^{-3}]	1.47×10^{19}	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
Net doping concentration [cm^{-3}]	1×10^{16} (p)	1×10^{17} (n)	1×10^{18} (n)	1×10^{20} (n)
Mobility electron/hole [cm^2/Vs]	200/30	5/5	100/25	100/25