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A compact model based on the Lambert function for AlGaN/GaN Schottky barrier gated-edge termination

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ABSTRACT

A compact model based on the Lambert function is used to describe I-V-T characteristics of Schottky Barrier Diodes (SBDs) with gated-edge termination (GET) with either SiN or SiO/AlO as GET dielectric. Electrical parameters obtained from this model enable Schottky barrier height (SBH) assessment. It will be shown that fluctuations are about 17% in both cases. Similar interface state density (from ideality factor) is obtained which is consistent with previous work and validates this approach as an interesting method to model these GET-SBDs.

1. Introduction

Lateral AlGaN/GaN-based Schottky Barrier Diodes (SBDs) obtained from GaN on Si (GoS) rise a great interest lately. Introducing a dielectric layer or Gated Edge Termination (GET) above the AlGaN barrier by anode recessing improves further breakdown voltage larger than 600 V with leakage current down to 1nA/mm but at the cost of ON-state voltage (V_{TON}) or threshold voltage (V_{TH}) instability [1,2]. Indeed, it is worth observing that the GET structure (Fig. 1) and a metal–insulator-semiconductor stack are alike. Hence in-situ defects from compatibility material at the semiconductor (AlGaN-barrier)/Dielectric interface is as critical as in MOS-like devices (MOSFET or MOS-HEMT) [3]. Therefore, it is reasonable to apply reliability techniques such as positive bias temperature instability (PBTI) to assess and understand these V_{TH}-instabilities [4]. Many works have thus reported experimental electron trapping/de-trapping processes explained by defects at the AlGaN/dielectric interface [1,5,6,7].

Interestingly this trapping from in-situ defects can be fully recoverable for high enough temperatures (300C) [3] while trap creation (related to permanent V_{TH}-shift) would occur under extreme stress bias conditions [8]. The specificity of the SBD is the geometrical architecture of the GET (Fig. 1) where the increase of vertical field enhances the trapping process along the GET/AlGaN barrier interface responsible for V_{TH} degradation under voltage stress [9]. Finally, electron trapping rate and defect densities depend on the GET or dielectric material as reported in [1,2,3,9]. These defects also influence other electric parameters like the ON-resistance, ideality factor and more generally the Schottky barrier height [8,9]. To understand this influence also related to the GET dielectric, an analysis of these different electric parameters is crucial. This can be done by using a model describing the experimental electrical characteristics. For an SBD device, one can use the diode current equation solution which has been extensively studied [10–12] with capacitive component [13]. One of the best options to solve this equation is to use the Lambert function [10,14]. Among these models, only a few uses a close analytic form of the Lambert function [15] and not specifically to AlGaN/GaN SBD with GET. In this work, it is proposed a compact model using an analytic or simplified Lamb(W) to describe the experimental I-V-T characteristics. Further, the model parameters could be associated the electrical parameters of the devices. This also enables to study of the inhomogeneity of the Schottky Barrier Height (SBH)

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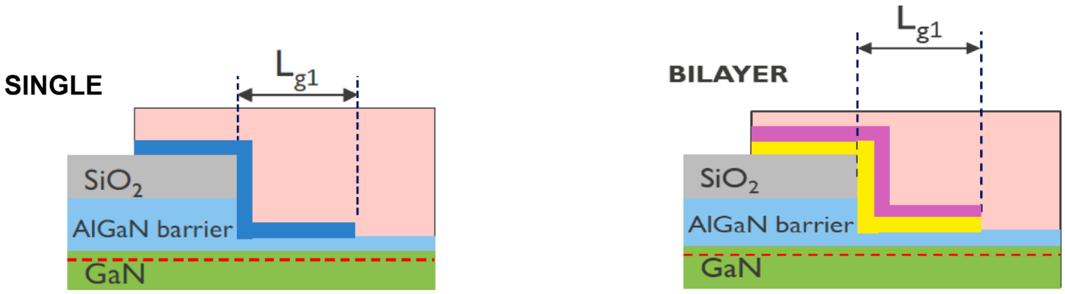

Fig. 1. The sample architecture has either a Si_3N_4 (45 nm) or SiO_2 (35 nm) onto Al_2O_3 (2.5 nm). HRTEM pictures for the Si_3N_4 device are available in [1].

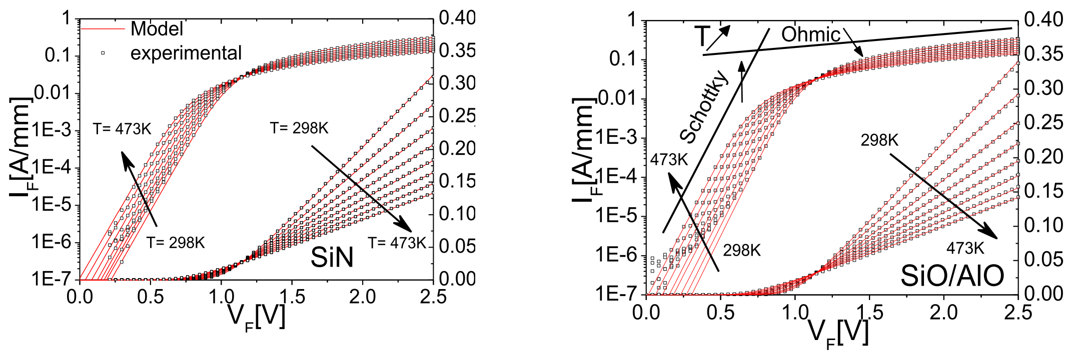

Fig. 2. Experimental I-V-T characteristics for the 2 types of diodes as shown in Fig. 1. The model (1) enables a very good description of the experimental data.

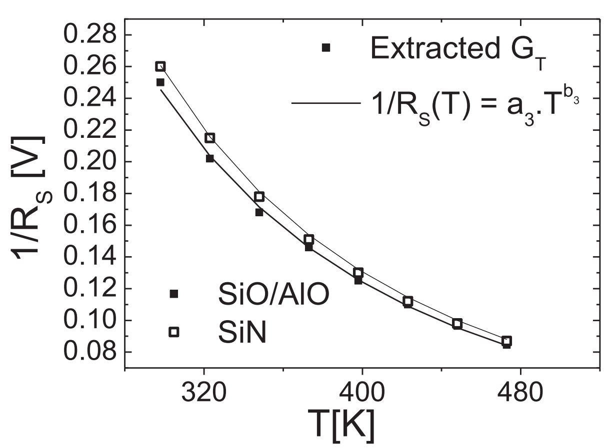

Fig. 3. Extraction of the inverse of the series conductance and fitting with a power low. Larger scattering produces a larger Ohmic effect and degrades the conductance.

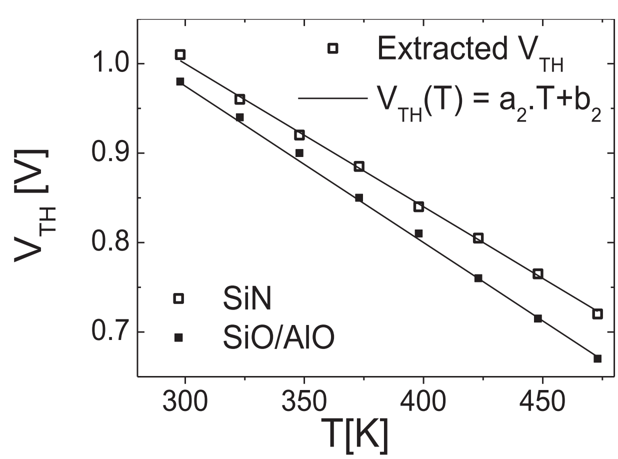

Fig. 4. V_{TH} extraction and fitting with a linear law. The increase of the current density produces an earlier onset of ohmic effect and reduce the V_{TH}.

using the model parameters for 2 different types of GET-Dielectrics: Si_3N_4 (45 nm) or SiO_2 (35 nm) onto Al_2O_3 (2.5 nm).

2. Experimental

The MOCVD epitaxial stack is grown on Si (1 1 1). It features a thick superlattice buffer designed for a 650-V platform technology with a 300-nm-thick GaN channel, a 0.5-nm-thick AlN spacer, a 10-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier, and a 5-nm-thick SiN cap. The epitaxial stack is passivated with a SiO_2 layer using high-temperature oxide deposition. The GET dielectric was either a single 45-nm thick Si_3N_4 ("SiN" in the plots) or a multilayer 35 nm SiO_2 dielectric deposited onto a 2.5 nm Al_2O_3 ("SiO/AlO" in the plots) interfacial layer (Fig. 1) [1]. Measurements were carried out on the same wafer die location to reduce the effect of the cross-wafer variability [3].

3. Modelling of the I-V-T characteristic

All I-V-T characteristics in direct regime and for temperatures ranging from 278 K to 473 K have been measured. The experimental results (Fig. 2, symbols) are consistent with SBD devices. The thermionic field emission (TFE) transport phenomenon is responsible for the current intensity increase with the temperature at a fixed bias, and the linear increase with forward regime (log-scale). For forward voltages V_F larger than 1 V, the current density is high enough to be limited by the ohmic effect (Fig. 2, linear scale) while it is inversely proportional to the temperature increase. In the ohmic regime the transport is explained by the scattering phenomenon limiting the mobility, in this specific case, related to acoustic phonons [16]. Note that the I-V is T-independent at $V_F \approx 1.2$ V suggesting the cancellation of the screening effect for the 2DEG by the electron thermal velocity. The temperature increase produces a larger current in the Schottky regime and a lower current due to

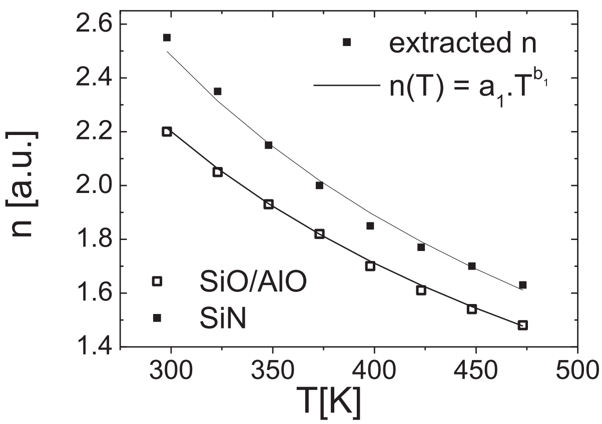

Fig. 5. Extraction of the ideality factor and fitting with a power law. The n-factor larger than the unity suggests Coulombic effects from charges in the dielectric or at the interfaces.

Table 1
Fitting parameters for different temperatures modelling.

Compact Model	n		V_{TH}		$1/R_S$	
	a_1	a_2	a_2	b_2	a_3	b_3
SiN	592	−1.05	17.5E-4	1.5	1.35E5	−2.32
SiO/AlO	323	−0.87	1.6E-4	1.48	1.6E5	2.35

the ohmic effect, yielding a reduction of the V_{TH}.

An analytic model of the I-V-T characteristics based on a simplified Lamb(W) [16,17] is used to solve the SDB transcendental current equation. This model (1) is defined as follow:

$$I_F = \frac{n.\phi_t}{R_S}\ln(1+e^u).\left\{1-\frac{\ln[(1+ln(1+e^u))]}{2+\ln(1+e^u)}\right\} \quad (1)$$

where $u = \frac{V_F - V_{TH}}{n.\phi_t}$ and $\phi_t = kT/q$. We observe that (1) displays a very good agreement with the experimental data (Fig. 1, lines). The model (1) relies on 3 parameters: the ideality factor (n), the V_{TH} (defining the Ohmic regime) and the series conductance ($1/R_S$) which can depend on V_F. These ones have a negligible V_F-dependency (Fig. 2) and have been extracted from the model (1). The results (Figs. 3-5) show a temperature (T) dependency of n, V_{TH} and $1/R_S$ that could be fitted using either a linear or power law model; the coefficients are given in Table 1. The $1/R_S$ reduction (or R_S increase) with T increase (Fig. 3) is consistent with an increase of the phonon scattering. On the other hand, the T increase produces a larger current density in the Schottky regime related to TFE and triggers in turn an earlier onset of the ohmic regime. This leads to a V_{TH} reduction consistent with Fig. 4. Finally, in Fig. 5, we obtain an n-factor that is 2 to 3 times larger than unity which suggests inhomogeneity of the Schottky barrier probably originating from coulombic defects (bulk or surface) or/and interface states [18,19].

Table 2
Value of the Heights, fluctuations, voltage deformation coefficient of the Barrier.

	$\overline{\phi_{b0}}$[eV]	σ_0[eV]	ρ_2[mV]	ρ_3
SiN	1.05	0.178	−4	−0.032
SiO/AlO	0.98	0.145	−50	−0.032

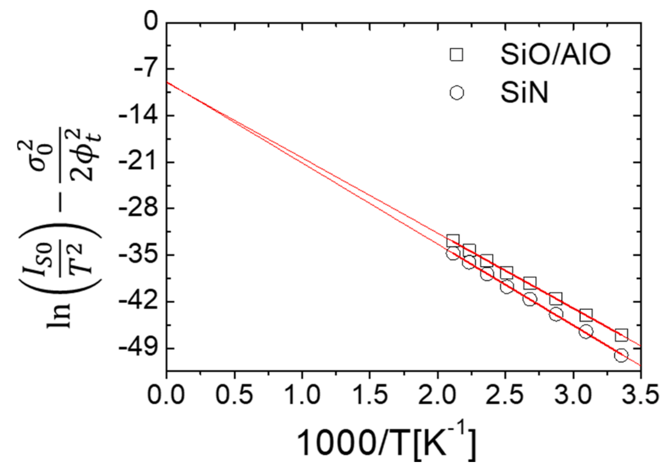

Fig. 7. Modified Richardson plot where the expression $\ln\left(\frac{I_{S0}}{T^2}\right) - \frac{\sigma_0^2}{2\phi_t^2} = \ln(S.A^*) - q\frac{\overline{\phi_{b0}}}{k_b T}$. Note that the value of the SBH ($\overline{\phi_{b0}}$) is consistent with the ones obtained in Table II.

4. Inhomogeneity of the Schottky barrier

In the TFE theory the saturation current is defined as $I_S = S.A^* T^2 e^{-\phi_b/\phi_t}$ where S is the Schottky contact area (here, 5x10^{-6}cm^2) and the Richardson constant $A^* = \frac{4\pi qk^2}{h}m$ where h and k are respectively the Planck and Boltzmann constants, and m is the mass. For a given material, as the GaN for instance, the Richardson constant is written as a function of the effective mass: $A^*_{GaN} = \frac{A^* m^*}{m}$ where m* is the effective mass of the electron; hence for GaN, A^*=*26.4* A.cm^{-2}K^{-2}[19]. The I_S is extracted at zero bias. It enables an extraction of the apparent SBH (or ϕ_b) which is temperature dependent (Fig. 6). Since the SBH is not constant, it can be described as a Gaussian distribution where the average

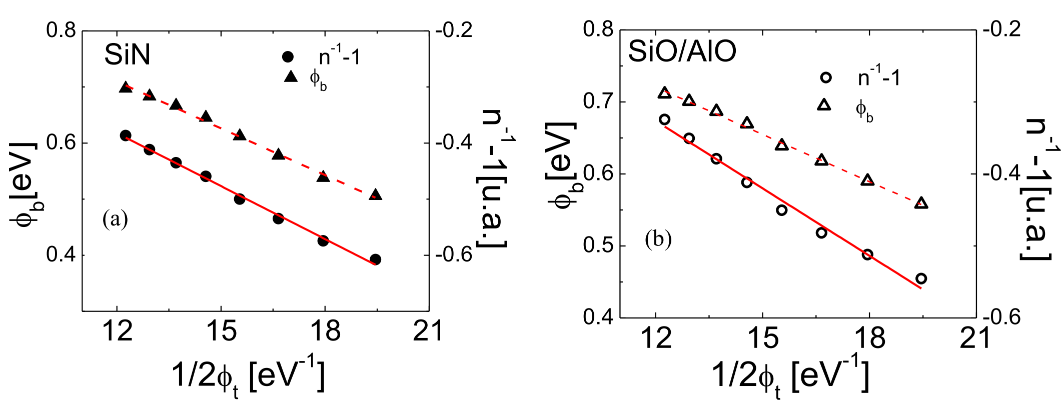

Fig. 6. Apparent SBH plot to extract the SBH for ($\overline{\phi_{b0}}$) and the fluctuations σ_0^2 for T = 0, and n^{-1}-1 plot to extract the coefficient voltage deformations. These results have been confirmed using the modified Richardson plot Fig. 7 [20 21].

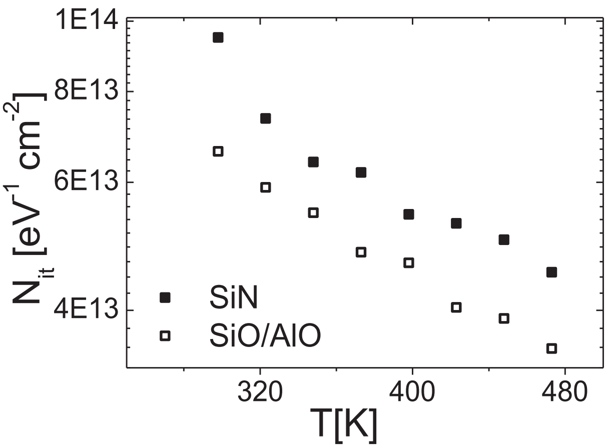

Fig. 8. Approximation of the interface state density using: $N_{it} = C_{diel}$ (n-1)/q where C_{diel} is the capacitance value per area of the GET dielectric and n is extracted using ln(I_F) vs (V_F-R_s.I_F) for $V_F = V_{TH}$.

value ($\overline{\phi_{b0}}$) and the fluctuation or standard deviation (σ_0), at T = 0, are modulated through voltage deformation coefficients ρ_2 and ρ_3 following the description (2) and (3) from the transport model from [20]:

$$\phi_b = \overline{\phi_{b0}} - \rho_2 V_F - \frac{\sigma_0^2 - \rho_3 V_F}{2\phi_t} \tag{2}$$

$$\frac{1}{n} - 1 = -\rho_2 + \frac{\rho_3}{2\phi_t} \tag{3}$$

According to (1) and (2), the plots ϕ_b vs $1/2\phi_t$ and $\frac{1}{n}-1$ vs $1/2\phi_t$ should be linear to extract the voltage deformation coefficients (ρ_2 and ρ_3) and the fluctuation (σ_0), characterizing the distribution of the non-uniform SBH[19–21]. Fig. 6 shows these plots for the Si_3N_4 (a) and for Al_2O_3/SiO_2 (b) devices featuring linear relationship, hence the parameters of these distributions could be extracted (Table 2). Note that the standard deviation of the SBH o fluctuation enables to extract the Richardson constant using the modified Richardson plot (Fig. 7). We found *28* A.cm^{-2}K^{-2} for SiO/AlO and SiN which is consistent with the value reported in the literature for GaN [19]. This result confirms the precision of the fitting parameters (Figs. 3-5) and in addition gives an interpretation physics of these parameters for the compact model (1).

From the extraction in Fig. 6 (Table 2) we obtained that the fluctuations around $\overline{\phi_{b0}}$ are similar for the 2 samples (about 17%). In both samples, these fluctuations are reduced at the same rate under bias voltage (same $\rho_3 < 0$). However, the ρ_2 is 10 larger for the devices with the Al_2O_3/SiO_2 stack as GET dielectric. It is worth noting that$\rho_2 < 0$ suggests a reduction of the apparent ϕ_b likely explained by force image originating from charge configuration specific to the dielectric layer [20,21]. This is consistent with larger current intensity increase with V_F bias. We could approximate the interface state density using the n-factor [21] as show in Fig. 8. The results suggest a somewhat larger interface states density for the Si_3N_4 at the $V_F = V_{TH}$ consistent with PBTI experiments in [3].

5. Conclusions

We successful introduced a compact model using the simplified Lambert function to describe experimental I-V-T characteristics for an AlGaN/GaN Schottky barrier diode with gated-edge termination. Electrical parameters extracted from this model along with their T-dependency enables SBH inhomogeneity assessment as a metric to describe SBD-GETs. Further this model can also be considered for electrical circuit simulation under different temperatures for a DC analyze.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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