Space-charge-limited currents in CIS-based solar cells

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(Received 21 September 2017; accepted 7 November 2017; published online 22 November 2017)

Non-linear shunts in $Cu(In,Ga)Se_2$ solar cells have been well described mathematically using the model of a space-charge-limited current, but their physical origin remained unclear so far. We study space-charge-limited currents on Cu-rich $CuInSe_2$ (CIS) devices, which represent a very suitable system: the devices always exhibit non-linear shunts with a very pronounced behavior. Here, we demonstrate a fundamental difference in the transport mechanism between the Cu-rich-based device and the conventional Cu-poor one. We discuss the location of a space-charge-limited current by comparing devices containing various component layers with Ohmic contacts. We confirm that Cu-rich CIS and cadmium sulfide layers alone do not create a non-linear shunt. Our experimental results demonstrate that the origin of the non-linear behavior is located at the interface between the absorber and buffer layers. Temperature dependent current-voltage measurements performed on Cu-rich-based CIS devices are discussed in agreement with a space-charge-limited current theory suggesting the model of an insulator with traps. https://doi.org/10.1063/1.5006040

Non-linear shunts in imperfect $Cu(In,Ga)Se_2$ (CIGS) solar cells are serious issues in terms of reproducibility and device operation.[1,2] This parasitic leakage cannot be described by a classical diode model, as it has non-Ohmic, bent behavior.[3,4] It was recently shown that in analogy to organic- and amorphous silicon-based devices, the non-linear shunt in CIGS solar cells is best described by the SCLC (space-charge-limited current) theory.[1,2,4–6] The basic model suggests the presence of a dielectric layer embedded between two injecting contacts, which provide only one type of carrier, while the other type of carrier is blocked.[7] It was thereby proposed that CIGS-based devices contain an intrinsic layer located in the CIGS absorber, which is formed due to some undefined electronic non-uniformity of the absorber.[1,4] The formation of injection contacts was explained by localized areas, where the junction is damaged by elemental diffusion from the top layers. The physical origin of space-charge-limited currents in CIGS could not be specified any closer.[1,2,4] Although simulations performed with metal/CIGS/metal devices demonstrated that a space-charge limited current is most probably located in the absorber,[5] no direct experiment exploring the location and the physical origin of SCLC has been presented. Therefore, here, we investigate SCLC on Cu-rich $CuInSe_2$ (CIS) devices. These devices represent a perfect system to study SCLC, as non-linear reverse leakage is always present, very pronounced, and at the same time, the device performance is still reliable (efficiency about 7%).[8,9] For a detailed analysis of SCLC, we compare log-log plots of the dark reverse current of various devices and discuss their temperature dependence.

CIS absorbers were co-evaporated by molecular beam epitaxy (MBE) on molybdenum coated soda lime glass using a conventional one stage process.[10] The Cu/In ratios measured by energy-dispersive X-ray spectroscopy (EDX) were 0.9 and 1.3 for Cu-poor and Cu-rich absorbers, respectively. After the deposition, a 10% aqueous solution of Potassium Cyanide (KCN) was applied to Cu-rich absorbers for 5 min in order to remove the secondary copper selenide phases followed by a potassium fluoride (KF) surface treatment performed in the MBE system for the sample labelled "Cu-rich + KF" as described in Ref. 9. In order to remove oxide from the surface of Cu-poor absorbers, a 5% KCN solution was applied for 30 s. Cadmium sulfide (CdS) buffer layers with a standard thickness of approximately 50 nm were deposited by chemical bath deposition. The samples with different CdS thicknesses were deposited by controlling the CdS deposition time or by performing a double deposition. The cells are finished with sputtered i-ZnO and biased ZnO window layers (more details are given in Ref. 11). The nickel aluminum top contact grids were prepared by electron beam deposition. IV curves were measured using a current–voltage (IV) measurement system in the dark or under the illumination using an AAA solar simulator. For the temperature dependent IV measurements, the samples were placed in a closed-cycle helium cryostat.

As demonstrated in Fig. 1(a), the Cu-rich CIS-based device exhibits a large non-linear reverse leakage. The device containing the same Cu-rich absorber, but with the post-deposition treatment (Cu-rich + KF), demonstrates a leakage of much lower magnitude similar to the Cu-poor CIS-based device (Cu-poor) shown here for comparison. At the same time, the shunts of Cu-rich + KF and Cu-poor devices are not perfectly linear, as can be seen in the inset of Fig. 1(a): the enlarged curves demonstrate a slight bending. Although the reverse leakage of the Cu-rich-based device is very pronounced and non-linear, it cannot be explained by diode breakdown as, first, it is observed at relatively low reverse bias voltages (about −0.5 V), while typically the reverse

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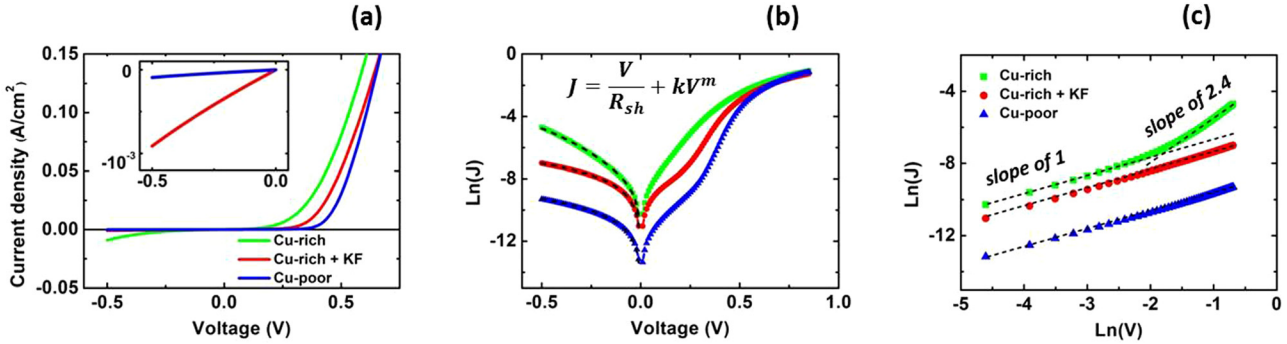

FIG. 1. Dark IV dependence of Cu-rich, Cu-rich + KF, and Cu-poor devices: (a) linear plot, (b) semi-log plot, and (c) log-log plot of reverse bias. The inset of (a) shows the enlarged reverse bias of the Cu-poor and Cu-rich + KF devices. The dashed lines of (b) represent the modelling using Eq. (1). The dashed lines of (c) correspond to the slopes of 1 and 2.4.

breakdown of CIGS devices appears at voltages below −3 V.[12] Second, it has a non-exponential, power law shape (as shown below). Because of the non-exponential behavior, the reverse bias non-linearity cannot be attributed to tunneling current either. In analogy to previous reports, here, we discuss the non-linear shunt in terms of space-charge-limited current theory.[1,2,4–6] The model of SCLC is an analogy to the vacuum diode, but the voltage dependence is parabolic in the conventional case and includes the carrier mobility μ and the dielectric thickness L ($J \sim \mu V^2/L^3$).[7,13,14] At lower voltages, the injection is negligible, and so, the Ohmic conductivity dominates, while at higher voltages, the carrier injection takes place, which results in a non-linear IV dependence.[15] Thus, in the recent reports, the dark IV reverse response of CIGS devices was described as a sum of linear (Ohmic) and non-linear (SCLC) contribution and was modelled on a semi-log scale with the following equation:[4]

$$J_{rev} = \frac{V_{rev}}{R_{sh}} + kV_{rev}^{m}, \tag{1}$$

where R_{sh} is an Ohmic resistance, k is a non-Ohmic prefactor, and m is a power exponent, which is generally considered to be equal to 2 in a classical space-charge-limited current theory and might be higher in the presence of charge trapping.[7] In the corresponding semi-log plot shown in Fig. 1(b), the dark current of the Cu-rich sample shows a symmetric dependence of a large magnitude in forward and reverse bias so that the diode-like behavior in forward bias is hardly distinguishable. Such a bent behavior cannot be described with the simple parabolic law, and the exponent was fitted to be *2.4* together with a high non-Ohmic prefactor (see Table I). In contrast, Cu-poor and Cu-rich treated cells are modelled with an m value of *2*. However, the linear term clearly dominates so that k is found to be very low, and thus, the reverse bias is mainly described by the Ohmic shunt contribution (Table I). A convenient way to clarify Ohmic and SCLC contribution is an analysis in a log-log plot. As shown in Fig. 1(c), in the log-log plot, all the devices contain an Ohmic contribution, which shows a slope of *1*. The Cu-rich-based device shows a change in the slope at higher voltages. In the non-linear region, the slope is given by *2.4*. At the same time, only the Ohmic region is found in the case of the Cu-poor and the treated devices. The bending is very slight and cannot be described by a power law. Essentially, there is no evidence of SCLC in these devices.

The next question to be discussed is the source of SCLC in the Cu-rich devices. To check if the SCLC is located in the Cu-rich CIS absorber, Ohmic contacts were prepared: the bottom contact contained molybdenum, while the top contact was Ni:Al deposited directly on the top of the absorber. The corresponding log-log plot of current with negative voltage applied to the Mo contact is shown in Fig. 2(a) and confirms the creation of Ohmic contacts: a large linear region with a slope of 1 is shown. At higher reverse voltages, a slight bending is observed, which is however not straight. There is no such clear slope change as in the case of the Cu-rich finished device. We therefore conclude that the Cu-rich CIS absorber itself is not the reason for the space-charge-limited current.

It is worth taking a deeper look at the CdS buffer layer, as CdS represents a perfect source of space charge limited currents, as discussed in the earlier literature.[13–18] When CdS is embedded between two Ohmic contacts (for example, In/CdS/In device), low barriers to the conduction band allow an easy electron injection, while the holes are blocked. The slope change in the log-log scale was observed for single crystals as well as for thin films.[17,18] To find out if the buffer and window layers represent a source of SCLC in CIS solar cells, a device where the CdS buffer layer was directly deposited on molybdenum and covered with ZnO and Ni:Al contacts has been prepared. The corresponding log-log dependence is shown in Fig. 2(a) (dark grey triangles, Mo/CdS/ZnO/Ni:Al) and demonstrates behavior with a slope of *1*. At higher reverse voltages, some deviation is observed, but again not a clear slope change as in the complete device.

TABLE I. Measured solar cell performance and fitting parameters obtained from Eq. (1).

Sample name	*Eff.* (%)	*FF* (%)	V_{oc} (mV)	J_{sc} (mA cm^2)	R_{sh} (Ohm cm^2)	k (A/V^m)	m
Cu-rich	7.1	48	356	42	324	0.05	2.4
Cu-rich + KF	9.5	58	401	41	638	4.7×10^{-4}	2
Cu-poor	12.3	64	445	43	6472	6.95×10^{-5}	2

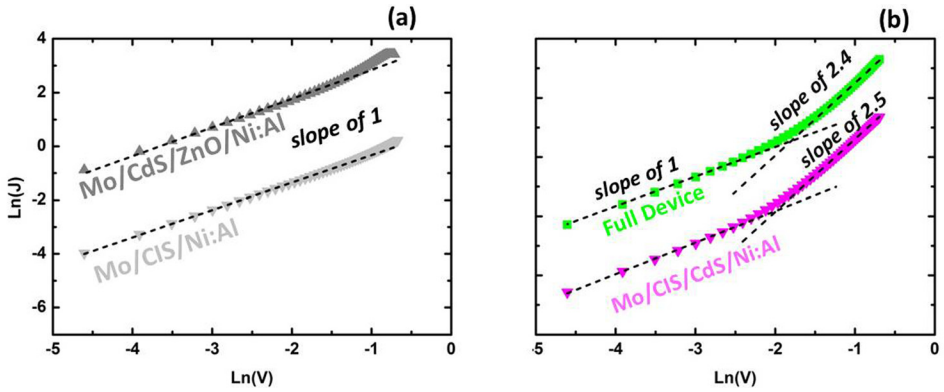

FIG. 2. Log-log plots of dark IV of (a) Mo/CdS/ZnO/Ni:Al and Mo/CIS/Ni:Al devices fitted with the slope of 1 (dashed lines) and (b) Mo/CIS/CdS/Ni:Al device and Mo/CIS/CdS/ZnO/Ni:Al (full device) reverse current fitted with the slopes of 1, 2.4, and 2.5 (dashed lines).

For a deeper understanding of the slope behavior, low temperature IV measurements were performed. Figure 3(a) demonstrates the log-log plot of the dark reverse current of a Mo/CdS/ZnO/Ni:Al device measured at temperatures of 300–130 K. Becoming less conductive at lower temperatures, the linear conductivity of the CdS layer decreases, observed in the log-log plot as a continuous down-shift of the characteristic with a slope of *1*. At lower temperatures, the curves demonstrate some bending with a slope of *1.7*, which is insufficient to be attributed to SCLC. These experimental results confirm the Ohmic conduction and the absence of SCLC in the CdS buffer layer.

With the previous experiments, we demonstrated that SCLC is located neither in the CIS absorber nor in the CdS buffer layer. At the same time, we show here that the potassium treatment removes the SCLC behavior [Fig. 1(c)]. Previously, it was published that other surface treatments, such as InSe or *ex-situ* KF, remove the non-Ohmic shunt.[8,19] The application of Bromine etching as an alternative to KCN was shown to reduce this leakage, too.[20] These observations suggest that the source of the SCLC behavior is located at the interface between CIS and CdS. To check it, a device with both Cu-rich CIS and CdS layers was prepared, while the top contact was directly deposited into CdS. Figure 2(b) presents the corresponding log-log plot of the IV dependence at reverse bias. For the Mo/CIS/CdS/Ni:Al device, a clear slope change is observed: the non-linear contribution exhibits a slope of *2.5*. The slope behavior in general is similar to the full device shown in Fig. 2(b) for comparison. The addition of window layers (full device) makes the slope steepness slightly lower. In this way, we show that to observe the SCLC, the presence of both CIS and CdS layers is necessary. This is the strong indication that the source of the SCLC behavior is located at the interface of those two layers.

It was discussed in the literature that Cd diffuses into CI(G)S,[21–24] which is in agreement with capacitance-voltage measurements performed on our devices.[25] Diffusing Cd is thought to occupy Cu vacancies and thus transforming acceptors into donors and reducing the net doping.[21] In the case of Cu-poor-based devices, there are many more Cu vacancies to be filled in comparison to the Cu-rich one. This would result in the reduction of the net-doping level but likely not in the formation of a nearly intrinsic material. It was shown that KF treatment causes the formation of a Cu-poor surface, also in the case of Cu-rich absorbers,[9] which might be the answer why the Cu-rich treated sample does not show SCLC similar to the Cu-poor-based device. A further reason for the absence of SCLC in Cu-poor- and Cu-rich-treated devices can be the higher roughness of Cu-rich absorbers,[10,20] which possibly results in more diffusion pathways. In agreement with this assumption, it was shown that flattening the Cu-rich surface improves non-linear current leakage.[20]

In this way, we suggest a new model, refined from the previous ones in the literature: the dielectric is formed at the interface between $CuInSe_2$ and CdS. Normally, this dielectric layer simply contributes to a grading in the doping level of the p-n junction. But there are locations where the junction is damaged in a way that a nearly ohmic contact is formed with the CdS or the absorber surface. In those areas, the injection into the dielectric takes place and we observe the SCLC type shunt. The higher surface roughness of Cu-rich absorbers can additionally increase the area where the junction is damaged.

Finally, to understand the SCLC behavior in depth, the low temperature IV behavior of the Cu-rich full device was analyzed. In the simplest model, SCLC has no or very weak temperature dependence, as the injection itself does not

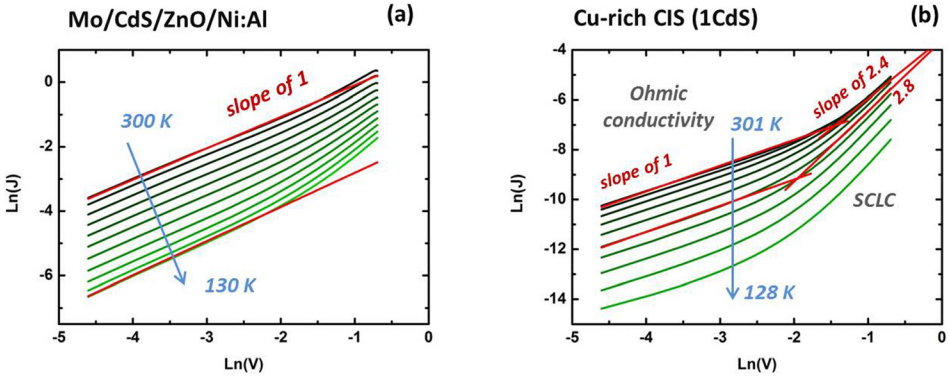

FIG. 3. Temperature-dependent log-log plots of dark reverse current of (a) Mo/CdS/ZnO/Ni:Al and (b) Cu-rich CIS-based devices.

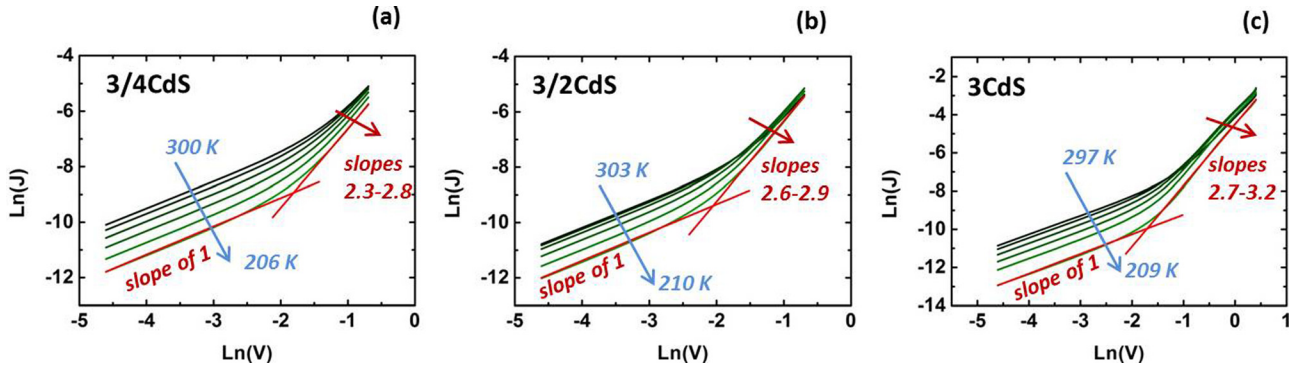

FIG. 4. Temperature-dependent log-log plots of dark reverse current of Cu-rich CIS-based devices with the CdS buffer layer of various thicknesses (a) 3/4CdS, (b) 3/2CdS, and (c) 3 CdS.

change with the temperature.[13] This is valid for a perfect insulator with no trapping states, when current-voltage behavior is parabolic ($I \sim V^2$).[7,13] In the case when SCLC is described by an exponent higher than *2*, similar to our experimental observations [Fig. 1(c)], the general model suggests the presence of trapping states.[7] Then, the injection itself does not change with the temperature, but the number of trapped charges is temperature dependent.[7] The temperature dependence for the model of an insulator with trapped carriers is given by

$$I \sim V^{(T_c/T)+1}, \tag{2}$$

where T_c is a characteristic temperature describing the trap distribution. The dependence indicates that slopes are getting steeper with the temperature decrease. The experimental temperature dependence shown in Fig. 3(b) demonstrates that while the Ohmic part decreases and gets shorter, the SCLC-related slope is becoming continuously steeper reaching a value of 2.8 at lower temperatures. At temperatures below 150 K, the current on the log-log scale becomes rounded in both Ohmic and non-Ohmic regions, indicating a different transport mechanism. The studies of SCLC in the literature based on exemplary CdS structures show a very similar behavior: on the log-log scale, the currents are getting smaller and steeper with decreasing temperature, and at lower temperatures, they demonstrate a rounded shape.[13,15] No temperature dependent log-log plots for CIGS-based devices have been published yet, but for organic devices, it was shown that SCLC theory is not valid at temperatures below 200 K.[26]

To further analyze the absorber-buffer interface, the CdS buffer thickness was varied so that the devices were investigated, which contain CdS layers with three quarters (3/4CdS), three halves (3/2CdS), and three times (3CdS) the thickness of a standard CdS layer. As demonstrated in Figs. 3(b) and 4, the increase in the CdS thickness results in a continuous increase in the SCLC-related slopes. At room temperature, the slopes correspond to 2.3, 2.5, 2.6, and 2.7 for 3/4CdS, 1CdS, 3/2CdS, and 3CdS, respectively. All the devices show a continuous increase in slope steepness with decreasing temperature in agreement with the model described above. At lower temperatures close to 200 K, the slopes correspond to 2.8, 2.8, 2.9, and 3.2, respectively. The behavior at temperatures lower than 200 K was not analyzed as the log-log dependence is rounded similar to the device shown in Fig. 3(b).

The steeper slope for thicker CdS directly indicates a change in the trapping center distribution, as it corresponds to a higher T_c in Eq. (2). According to the model,[7] higher T_c suggests a faster varying and wider trap distribution. We suggest that the number of trapped charges in the dielectric is increased for the increasing CdS thickness. This is in agreement with the model suggesting that the intrinsic layer is formed by in-diffusion of Cd.

In this contribution, a model for the non-linear shunt current of Cu-rich CIS solar cells is presented. We demonstrate that although the KF-treated and Cu-poor cells show a slight non-linearity at reverse voltages, there is no direct evidence of space-charge-limited current in these devices. The presence of a space-charge-limited current is clearly confirmed only in Cu-rich-based devices. In contrast to previous reports, where the location of the source of the SCLC was suggested to be in the absorber itself, an analysis of the Cu-rich CIS device with two Ohmic contacts does not confirm this assumption. The CdS buffer layer with two injection contacts does not demonstrate the presence of a space-charge-limited current either, which is additionally confirmed by low temperature IV analysis. We demonstrate that the space-charge-limited current is only shown in the case where both CIS and CdS layers are present and thereby suggest that the location of the intrinsic layer which causes the space-charge-limited current is at the interface between the buffer and absorber layers. Finally, we demonstrate that the temperature dependence of the Cu-rich based device is fully consistent with the model of the insulator with traps. The variation in the CdS buffer thickness results in the slope change supporting the assumption of elemental diffusion. We suggest that the intrinsic layer at the interface is formed by Cd diffusion into the absorber layer.

The authors are gratefully thankful to Finn Babbe, Thomas Schuler for discussion and technical support, and the Thin Films and Photovoltaics group (EMPA, Switzerland) for providing alternative CdS layers for comparison experiments. This research was financially supported by Luxembourgish Fonds National de la Recherche (FNR) in the frame of the CURI-K project.

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