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Organic ferroelectric transistors with composite dielectric for efficient neural computing

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ABSTRACT

Organic ferroelectric field-effect transistors (Fe-OFETs) exhibit exceptional capabilities in mimicking biological neural systems and represent one of the primary options for flexible artificial synaptic devices. Ferroelectric polymers, such as poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), given their strong ferroelectricity and facile solution processing, have emerged as the preferred choices for the ferroelectric dielectric layer of wearable devices. However, the solution processed P(VDF-TrFE) films can lead to high interface roughness, prone to cause excessive gate leakage. Meanwhile, the ferroelectric layer in neural computing and memory applications also faces a trade-off between storage time and energy for read/write operations. This study introduces a composite dielectric layer for Fe-OFETs, fabricated via a solution-based process. Different thicknesses of poly(N-vinylcarbazole) (PVK) are shown to significantly alter the ferroelectric hysteresis window and leakage current. The optimized devices exhibit synaptic plasticity with a transient current of 3.52 mA and a response time of approximately 50 ns. The Fe-OFETs with the composite dielectric were modeled and integrated into convolutional neural networks, achieving a 92.95% accuracy rate. This highlights the composite dielectric's advantage in neuromorphic computing. The introduction of PVK optimizes the interface and balances device performance of Fe-OFETs for neuromorphic computing.

Traditional computing systems follow the von Neumann architecture, where the processor and memory are separate, and data must be frequently moved between the two systems, which limits computational speed and increases energy consumption.[1–3] Artificial synapses based on ferroelectric materials exhibit deterministic resistance switching, large output signal dynamic range, and fine retention capabilities, which are instrumental in constructing high-performance neuromorphic computing systems.[4–6] Moreover, ferroelectric materials are capable of simulating the continuous update of synaptic weights in the biological brain, offering potential applications in realizing brain-like functions, such as associative learning and memory consolidation processes. In particular, the organic ferroelectric field-effect transistors (Fe-OFETs) with poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) as the dielectric layer have garnered extensive research attention due to their low crystallization temperature and nonvolatile memory (NVM) characteristics.[7,8] However, there are still some challenges faced by Fe-OFET in neuromorphic computing, including further optimization of the device manufacturing process and the balance between computing speed and memory capacity.[9,10]

In this work, we introduce a non-ferroelectric poly(N-vinylcarbazole) (PVK) passivation layer on the surface of P(VDF-TrFE) to form a composite dielectric and apply it to the structure of Fe-OFETs. The results show that the PVK layer can significantly reduce the surface roughness of the dielectric layer and gate leakage. At the same time, by changing its thickness, the ferroelectric window and on-state current can be effectively adjusted. The optimized devices can simulate synaptic plasticity, with a transient current of up to 3.52 mA at a fast response of approximately 50 ns. The current density (29.3 mA/cm) under this fast response is crucial for applications that require real-time processing or decision-making. In addition, the Fe-OFET is abstracted as a physical model and integrated into convolutional neural networks (CNNs) to evaluate the impact of the composite dielectric

on the computational performance of neuromorphic devices. The optimized Fe-OFET achieved a high accuracy of 92.95% in CNN tasks, highlighting the advantages of composite dielectrics in neuromorphic calculations. The addition of PVK not only effectively optimizes the interface but also helps to balance device performance in neuromorphic computing.

The device structure of the Fe-OFET in this study is characterized by a bottom-gate top-contact configuration, as shown in Fig. 1(a). It features a dielectric layer composed of a composite bilayer film consisting of poly(N-vinylcarbazole) (PVK) and P(VDF-TrFE). The semiconductor channel is fabricated from the polymer semiconductor poly-[2,5-bis(2-octyldodecyl)-3,6-di(thiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dionel-alt-thieno[3,2-b]thiophene] (DPPT-TT). The specific device manufacturing process is detailed in Fig. S1 and Note S1. Despite the advantages of the solution-based method in fabricating ferroelectric P(VDF-TrFE) thin films, such as cost-effectiveness, environmental benignity, and ease of processing,[11] it may lead to relatively high interfacial roughness [Fig. S2(a)], which can easily lead to excessive gate leakage and further reduce the retention performance of the memory devices. To address this issue, we introduced a PVK passivation layer and constructed a PVK/P(VDF-TrFE) composite dielectric. By using PVK solutions of different concentrations, we can achieve PVK layers of different thicknesses [inset of Figs. 1(b) and S3]. Figure 1(b) shows that the surface roughness of the composite dielectric gradually decreases with the increase in PVK thickness (Figs. S2 and S3). Furthermore, we measured the capacitance–voltage (C–V) curves of ferroelectric capacitors based on the composite dielectric with different PVK thicknesses [Fig. 1(c)]. The butterfly-like shape indicates their ferroelectric properties. When the external voltage reaches a sufficiently high level (∼20 V), almost all electric domains in ferroelectric materials are arranged along the direction of the electric field, reaching a saturated polarization state. When the PVK thickness is about 19 nm, the capacitance peak is the highest, corresponding to the optimal ferroelectric characteristics. The calculated average coercive electric field is around 80.15 MV/m.

Based on different PVK thicknesses, we constructed Fe-OFETs and measured their electrical characteristics. At different PVK thicknesses, the ferroelectric window size of the devices varies (Fig. S4). This indicates the controllability of ferroelectric windows, which can affect the switching speed of transistors, thereby affecting the speed of read and write operations.[12,13] In addition, Fig. 1(d) shows the maximum leakage of the Fe-OFETs, and a minimum leakage value appears at PVK with 19 nm. According to the thickness dependence of leakage and C–V characteristics, we can conclude that at PVK with 19 nm, the leakage and ferroelectric properties of the device reach their optimal levels. The influence mechanism of PVK thickness on the Fe-OFET's performance should be as follows. Initially, with the increase in PVK thickness, the reduction of surface defects and charge traps leads to a decrease in device leakage current. This improvement is attributed to the effective barrier provided by the passivation layer against undesired charge carrier migration and the reduction of charge traps at the interface, which, in turn, enhances the device's retention characteristics. However, further increase in PVK thickness will induce an increase in internal stress within the ferroelectric layer. This additional internal stress will affect the crystal structure and phase stability, thereby changing the polarization state and remnant polarization of the dielectric layer and, consequently, the overall performance of the device.[14,15]

The transfer characteristic of a typical Fe-OFET fabricated with the optimal process is shown in Fig. 1(e), exhibiting obvious p-type behavior and counterclockwise hysteresis with a maximum window of

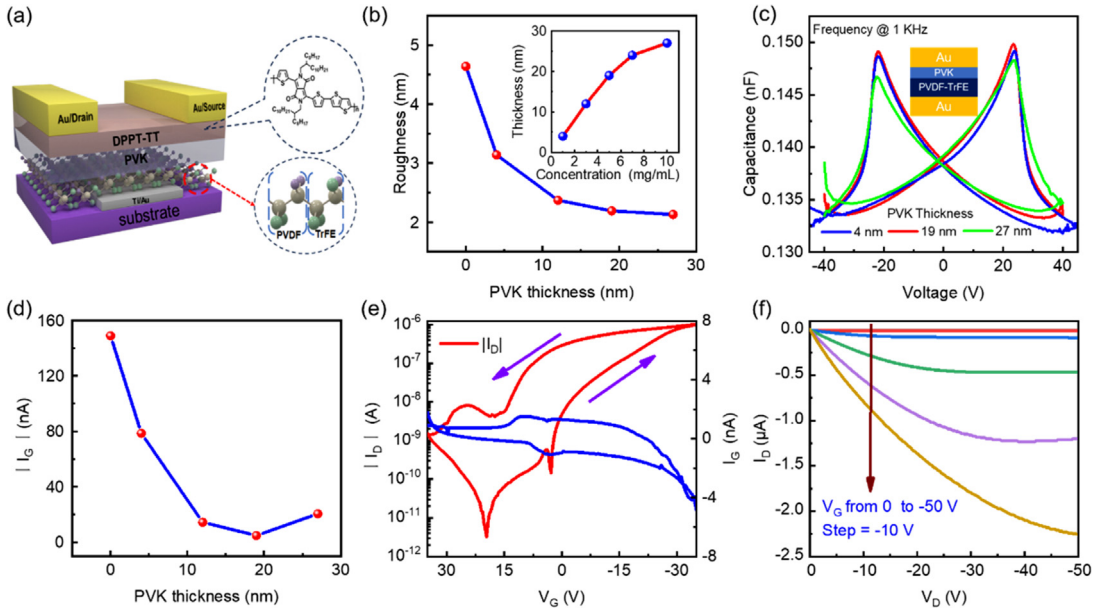

FIG. 1. (a) Schematic structure of the Fe-OFET. (b) The roughness of the composite dielectric depends on the PVK thickness. The inset shows the corresponding relationship between solution concentration and film thickness. (c) C–V curves of ferroelectric capacitors based on composite dielectric with different PVK thicknesses. (d) Maximum leakage of the Fe-OFETs with different PVK thicknesses. (e) Double-sweep I_D–V_G curve of a typical Fe-OFET at $V_D = -1$ V. The corresponding PVK thickness is 19 nm, and the blue line is the gate leakage. (f) I_D–V_D curves of the Fe-OFET.

20 V. During the process of continuously changing the V_G, the polarization state of ferroelectric materials will reverse under a certain electric field, leading to a shift in the threshold voltage (V_{TH}).[16] This polarization reversal will form two different working regions on the transfer curve, namely, high V_{TH} state and low V_{TH} state, and the separation between them constitutes a ferroelectric window. Moreover, the output characteristic measured under varied V_G is visible in Fig. 1(f). The channel current with V_D in the 0 to −20 V range is linear, which facilitates the input mapping of the array-level network later.

Fe-OFET has NVM capability and can maintain its state without external voltage.[24] This is similar to the postsynaptic potential in the biological nervous system, as shown in Fig. 2(a), which is able to maintain potential changes in the absence of continuous stimulation, thereby achieving memory functions. In the process of neural network learning, fast synaptic response can accelerate the weight adjustment process and improve learning efficiency.[25] Synaptic plasticity, a pivotal mechanism underpinning learning and memory, refers to the ability of synaptic transmission efficacy to fluctuate in response to neural activity, thereby serving as the basis for cognitive adaptation and retention.[26,27] Fe-OFET can simulate this plasticity by varying V_G, where a change in polarization state can represent a change in synaptic weight.[28,29] Under the simulation of neurotransmitters in pulsed electric fields, the polarization of ferroelectric materials can change on a timescale from nanosecond to microsecond.[30] Figure 2(b) presents the excitatory postsynaptic current (EPSC) test results of our Fe-OFET under a single pulse with a width of 10 μs and an amplitude of −30 V. Further reducing the pulse width to 1 μs, we can clearly observe the fast response of the Fe-OFET. As shown by the green curve in Fig. 2(c), a rapid response time of less than 50 ns was observed, which is 2×10^5 times faster than human synapses (≈10 ms). Meanwhile, the device can achieve a current density of 29.3 mA/cm, which means that it can complete the transition from high resistance state to low resistance state in a shorter time, which is crucial for improving the computational speed of neuromorphic devices.[31] In addition, the EPSC of the Fe-OFET can also be modulated by varying the pulse amplitude [Fig. 2(c)]. Figure 2(d) summarizes the response time of various recent artificial synapse technologies.[17–23] Our Fe-OFET has almost reached the highest level of performance, which is conducive to achieving efficient parallel processing and learning capabilities in neural network computing. Figure S5 shows the pulse-promoted paired pulse facilitation (PPF) behavior test of Fe-OFET, which is a manifestation of short-term synaptic plasticity.[32]

The design inspiration for neuromorphic devices comes from the biological nervous system, where changes in synaptic weight are achieved by altering the conductivity of postsynaptic neurons.[33,34] Variable channel conductance enables artificial neuromorphic devices to simulate this biological mechanism and achieve learning and memory functions similar to those *in vivo*.[35,36] Applying 10 consecutive pulses of −20/−25/−30/−35/−40 V to the gate, each 1 s in width, induces variable channel conductivity changes as depicted in Fig. 2(e). This is because changes in ferroelectric polarization state can affect gate dielectric capacitance, altering gate control of the channel. Polarization aligned with V_G enhances channel conductivity; opposite, it reduces it.[37,38] As shown in Fig. 2(f), our Fe-OFET is also tested with the same amplitude and different pulse widths. The results indicate that it has the characteristics of long-term potentiation (LTP).

In the realm of neuromorphic computing that emulates the neural networks of the human brain, the calibration of parameters in Fe-FETs can enhance the fidelity of synaptic weight simulation, thereby

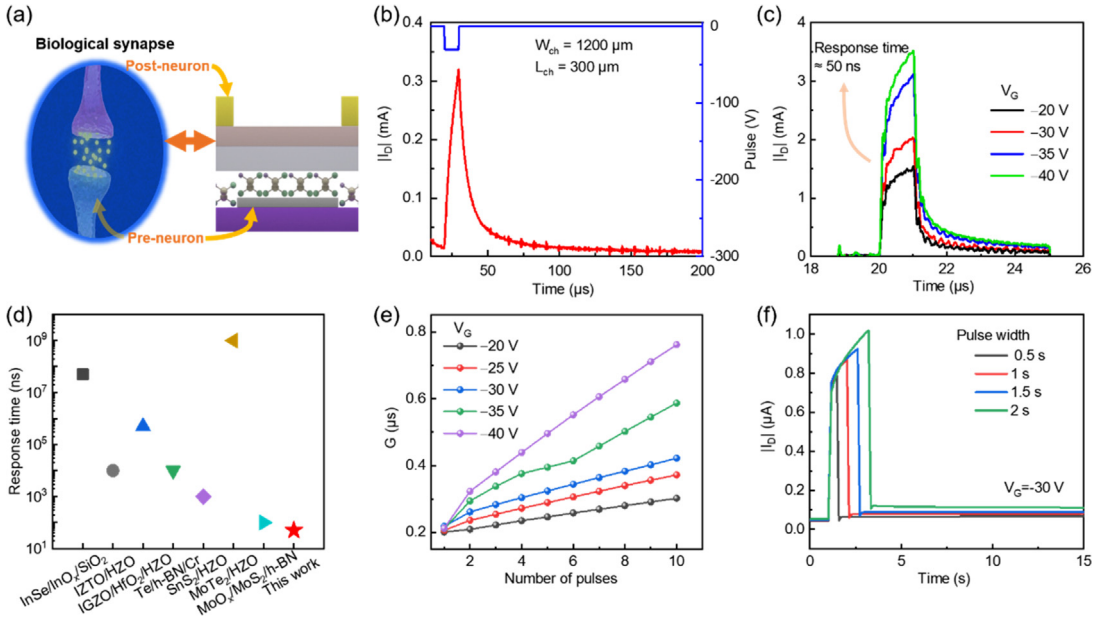

FIG. 2. (a) Diagram of neurons and synapses in a biological system. (b) Current response of the Fe-OFET under a single pulse with a width of 10 μs and an amplitude of −30 V. (c) Pulse characteristics under a single pulse with a width of 1 μs and varying amplitudes. A response time of approximately 50 ns was observed. (d) Recent reports[17–23] on the response time distribution of emerging synaptic devices. (e) Conductance change under multiple pulses with varying amplitudes. (f) Pulse characteristics under a single pulse with an amplitude of −30 V and varying widths. The V_D in the measurements was set at −1 V.

augmenting computational efficiency and learning capabilities.[39–41] Calibration is instrumental in aligning the performance of device models with their real-world counterparts, thus substantially enhancing the precision of design. In our organic ferroelectric model, we implement the approach detailed in Ref. 42, which relies on steady-state transfer rates. Here, P_u and P_D are the probabilities of upward and downward polarization, respectively, and they conform to the law of conservation of probability, expressed as $P_u + P_D = 1.0$. The polarization strength, P_{fe}, is articulated by the formula $P_{fe} = (2P_D - 1)P_S$, with P_S signifying the saturation polarization that represents the overlap of charges from both phases. The following equation outlines the calculation of current on the basis of capacitance:

$$i = \frac{dP_{fe}}{dt} + C_{fe}\frac{dV_{fe}}{dt}, \tag{1}$$

where C_{fe} and V_{fe} represent the ferroelectric capacitance and applied voltage, respectively. It is assumed that the integral turning points are $(V_{fe,i}, P_{D,i}, P_{u,i})$, and the turning point after time t is $(V_{fe,t}, P_{D,t}, P_{u,t})$. The coercive voltage $V_{c,t}$ under the small signal is expressed as

$$V_{c,t} = V_0 * \log\left[\frac{P_{u,t}\,\exp\left(V_{fe,t}/V_0\right) - P_{u,i}\,\exp\left(V_{fe,i}/V_0\right)}{P_{D,t} - P_{D,i}}\right], \tag{2}$$

where V_0 can represent the center (mean) value of a Gaussian distribution, and the standard deviation (∂) of the distribution describes the degree of dispersion of parameters around V_0. In the voltage domain, the incremental polarization is caused by the applied external voltage exceeding the coercive voltages of the corresponding domains. Assuming a Gaussian distribution of coercive voltages, we can obtain $V_0 = \sqrt{2\pi}\partial/4$.

The model is encapsulated within a Verilog-A module in a precise mathematical framework. This module is then seamlessly integrated through a netlist file, utilizing ports that ensure compatibility with the HSPICE netlist format (Fig. S6). We obtained the polarization curve of the device [Fig. 3(a)]. Given the direct proportionality between the coercive voltage and the coercive electric field, expressed as $E_c = \frac{V}{d}$, where d is the thickness of the ferroelectric film. E_c of the device can be determined to be approximately 73.8 MV/m, close to the experimental results, indicating the rationality of our model calibration. Figure 3(b) shows the program and erase behaviors of the device under a continuous and varying stimulus pulse (Fig. S7). As the program voltage shifts positively, the I_D gradually decreases, and as the erase voltage shifts negatively, the I_D gradually increases, which are consistent with synaptic excitation and inhibition behavior, respectively. Utilizing this pulse scheme, we calibrate the Fe-OFET model [Fig. 3(c)], it is observed that the trajectory of I_D changes corresponded well with experimental data. We calibrated the device at $|I_D|$ ranging from 10^{-8} to 10^{-6} A, corresponding to a memory window V_m of 13.98 V, which is approximately 1 V lower than the experimental results within the corresponding current range. Consequently, the Fe-OFET model has been effectively calibrated.

Hardware neural network training requires both write operations to strengthen synaptic connections and erase operations to weaken synaptic connections, thus simulating comprehensive long-term synaptic plasticity to improve the effectiveness and reliability of training.[43,44] We can modulate the device conductance through positive and negative pulses to simulate LTP and long-term depression (LTD),

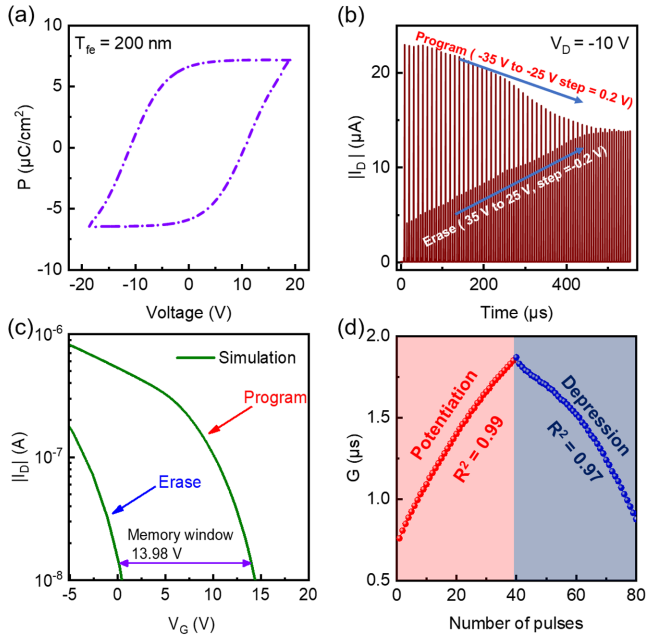

FIG. 3. (a) The polarization vs voltage (P–V) curve of the ferroelectric layer, with a thickness of approximately 200 nm. (b) The I_D of the device under continuous pulses in the model. The program pulse rises from −35 to −25 V, and the erase pulse decreases from 35 to 25 V. (c) The ferroelectric window curve of the device after calibration at −5 to 15 V. (d) Distribution diagram of the conductivity state of the device under experimental test.

as shown in Fig. 3(d). The write voltage is gradually increased linearly from −35 to −25 V, while the erase voltage is linearly decreased from 35 to 25 V, with the base V_G maintained at −10 V (blue line in Fig. S8). This pulse configuration facilitates the achievement of more linear conductance states. There is a sufficient number of distinguishable conductance states (~40), and the modulation of conductivity is highly linear with R^2 of ~0.99. These conductance states are adequate to perform complex and diverse tasks within convolutional units or networks of a certain scale. Utilizing the identical pulse configuration, we conducted a conductance state distribution test within the organic ferroelectric model (Fig. S8). The results demonstrated a significant enhancement in linearity. This improvement is conducive to performing more precise computations and decision-making within neural networks and ensures the consistency of the network's response after multiple operations.

The simulation employs the convolutional network with eight convolutional layers proposed by the Visual Geometry Group[45] (VGG8) at the University of Oxford, designed for large-scale image recognition, and the input images are from the CIFAR10 dataset, as shown in Fig. 4(a). Each image has a size of 32 × 32 and a depth of 3. VGG8 has six convolutional layers plus two fully connected layers. First, the convolutional layer extracts features from the input information map and uses convolutional kernels to obtain the product. By summing the operations on the corresponding elements, the network maps the receptive field information to the elements in the feature map. Throughout the process, pooling layers are continuously used to

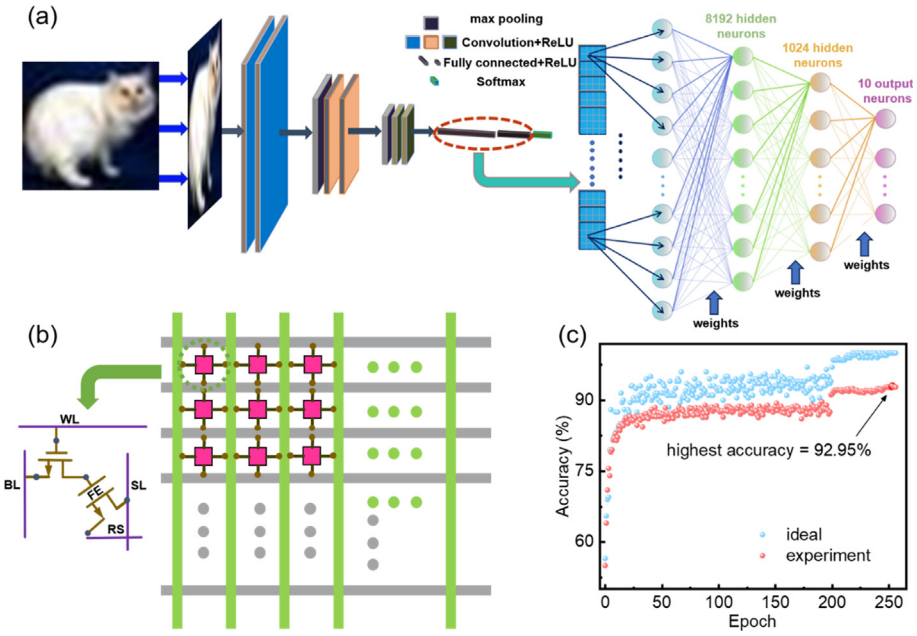

FIG. 4. (a) VGG8 network structure, the dashed part represents the fully connected layer, and the direction indicated by the arrow represents the specific structure of the fully connected layer. (b) Synaptic unit structure of Fe-OFETs with composite dielectric layer. (c) The image recognition accuracy of the device and model in CNNs.

reduce the dimensionality of the input image and compress the amount of data. Then, nonlinear features are introduced into the network. Due to the complex and nonlinear relationships typically found in data such as images, sounds, and text, the introduction of nonlinear activation functions is warranted. These functions not only enable the detection of linear features, such as edges, but also facilitate the capture of more intricate, nonlinear combinations of features. Finally, each pixel of every feature image post-convolution is sequentially flattened and subjected to a fully connected feedforward feedback process for the identification and classification of results. The final output is then generated through a softmax layer.

We have used the 1T-1Fe-OFET pseudo horizontal array structure[46] to achieve key operations such as vector matrix multiplication in neural network training, as shown in Fig. 4(b). Unlike conventional transistors used for selection control to support parallel programming across multiple columns, Fe-OFET may necessitate transitioning to distinct intermediate states and preventing programming of other unselected rows during the row-wise weight update process. Two separate input signals are used to activate write line (WL) and introduce the read voltage into read selection (RS), where RS is used to obtain the input vector. This is similar to applying a positive erase voltage to the gate to set the Fe-OFET to a lower conductive state and a negative write voltage for a higher conductive state. The conductance curves obtained post-experiment and calibration will be imported into Neurosim, employing a 1T-1Fe-OFET synaptic array architecture for image recognition to predict and evaluate the performance of our Fe-OFET with composite dielectric as a neuromorphic device. Figure 4(c) illustrates that the accuracy rates achieved by incorporating experimental and calibration parameters into convolutional neural network-based image recognition can reach 92.95% and 95.87%, respectively, which should mainly stem from the excellent polarization characteristics of the composite dielectric and the highly optimized semiconductor/dielectric interface. This indicates that our Fe-OFET exhibits significant potential in neural network computations following optimization and calibration.

In summary, we propose an Fe-OFET with a PVK/P(VDF-TrFE) composite dielectric prepared by a fully solution-based method. Our Fe-OFET can mimic synaptic behavior, featuring a rapid response of approximately 50 ns and a transient operating current of 3.52 mA. The incorporation of PVK serves a dual function, including ameliorating the interfacial characteristics and contributing to the optimization of the device's operational equilibrium, which is crucial for the execution of neuromorphic computing tasks. By abstracting the Fe-OFET into a physical model and integrating it into a CNN, a high accuracy of 92.95% can be achieved in image recognition tasks. Our Fe-OFET technology is expected to support the realization of low-power, low-cost flexible artificial neuromorphic computation and systems.

See the supplementary material for the experimental detail and supporting data.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Changqing Li: Conceptualization (equal); Data curation (lead); Formal analysis (equal); Investigation (lead); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Fuguo Tian:** Investigation (equal). **Zhongzhong Luo:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Software (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Haoyang Luo:** Investigation (equal); Software (equal). **Jie Yan:** Investigation (equal); Software (equal). **Xiangdong Xu:** Investigation (equal). **Xiang Wan:** Software (equal); Visualization (equal). **Li Zhu:** Investigation (equal). **Chee Leong Tan:** Methodology (equal); Validation (equal). **Zhihao Yu:** Formal analysis (equal); Funding acquisition (equal); Supervision (supporting). **Yong Xu:** Data curation (equal); Funding acquisition (equal); Project administration (equal). **Huabin Sun:** Conceptualization (lead); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (lead); Project administration (lead); Software (equal); Supervision (lead); Validation (equal); Visualization (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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