Deep level transient spectroscopic analysis of p/n junction implanted with boron in n-type silicon substrate

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(Received 31 October 2017; accepted 8 March 2018; published online 29 March 2018)

For P-i-N diodes implanted and activated with boron ions into a highly-resistive n-type Si substrate, it is found that there is a large difference in the leakage current between relatively low temperature furnace annealing (FA) and high temperature laser annealing (LA) for activation of the p-layer. Since electron trap levels in the n-type Si substrate is supposed to be affected, we report on Deep Level Transient Spectroscopy (DLTS) measurement results investigating what kinds of trap levels are formed. As a result, three kinds of electron trap levels are confirmed in the region of 1–4 μm from the p-n junction. Each DLTS peak intensity of the LA sample is smaller than that of the FA sample. In particular, with respect to the trap level which is the closest to the silicon band gap center most affecting the reverse leakage current, it was not detected in LA. It is considered that the electron trap levels are decreased due to the thermal energy of LA. On the other hand, four kinds of trap levels are confirmed in the region of 38–44 μm from the p-n junction and the DLTS peak intensities of FA and LA are almost the same, considering that the thermal energy of LA has not reached this area. The large difference between the reverse leakage current of FA and LA is considered to be affected by the deep trap level estimated to be the interstitial boron. *Published by AIP Publishing.* https://doi.org/10.1063/1.5011229

I. INTRODUCTION

In power semiconductors, if leakage current is considerably large, there is a possibility of device destruction due to thermal runaway.

For P-i-N diodes prepared by ion implantation of boron into a highly-resistive n-type Si substrate, it was found that there was considerable difference in the leakage current depending on the anode p^+ layer activation method[1] (Fig. 1). In the figure, "Method A" and "Method B" indicate furnace annealing (FA) and laser annealing[6] (LA), respectively. Leakage current in power devices is caused by the generation of hole-electron pairs in the depletion region.[2,3] Because the carrier generation is greatly affected by deep levels in the n-type Si substrate, we conducted this study to investigate the kind of deep level that is formed using Deep Level Transient Spectroscopy (DLTS)[4,5] technique. DLTS involves measuring deep levels (traps) and evaluating defects with a small density to ensure that the majority carrier density is not affected.

II. SAMPLE PREPARATION

Figure 2 shows the process flow for sample preparation. The anode p^+ was activated using two methods: furnace annealing (FA) or laser annealing (LA).

Electron beam irradiation[7] (EI), which is a method typically used for power semiconductor devices, was performed on the n^- substrate, on which the cathode n^+ was formed earlier, for carrier lifetime control. The cathode n^+ has the peak donor concentration of $1 \times 10^{20}\,cm^{-3}$.The electron beam was irradiated under conditions of an accelerating voltage of 4.6 MeV and an irradiation dose of 60 kGy. Then, in the case of the LA sample, annealing at several hundred degrees Celsius was conducted for optimizing the carrier lifetime. Subsequently, for activating the implanted boron of the anode, FA at 350 °C for 1 h or LA at the energy density of 1.4 J/cm^2 and the pulse width of 100 ns was performed. Regarding LA, since the temperature rise is extremely short, it is difficult to accurately measure the temperature, but it is presumed that the anode surface is momentarily heated to a temperature of 1000 °C or more.

In FA, the lifetime optimization and the boron activation are achieved by one annealing. The annealing conditions discussed above are the same as those of FA of the LA sample

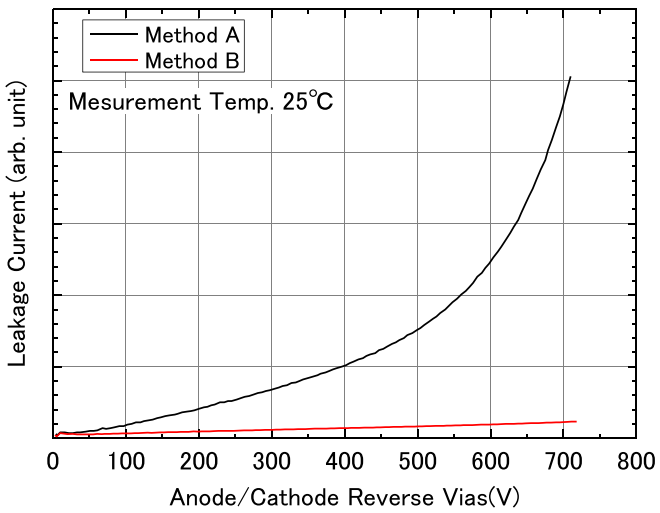

FIG. 1. Leakage current of pin diodes prepared by two different activation methods.

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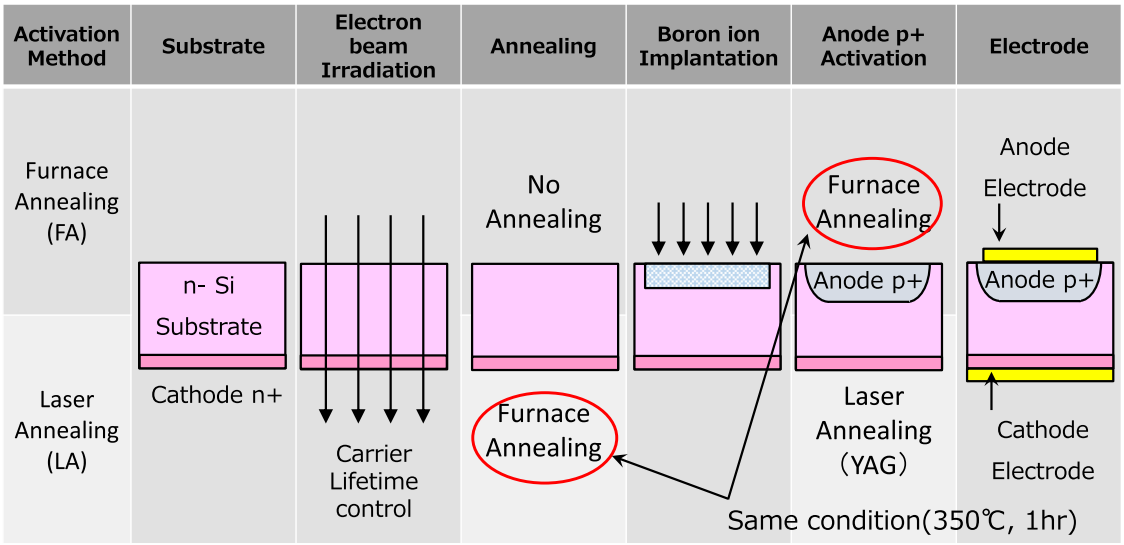

FIG. 2. Process flow for sample preparation.

for the lifetime control. In LA, the anode p^+ temperature rises sharply in a relatively short time, and the thermal energy is transmitted into the substrate. Finally, the anode and cathode electrodes are formed.

As shown in Table I, three types of samples were prepared. For investigating the effect of electron beam irradiation, only Sample 3 was not irradiated. In order to ensure that the anode peak concentration of both samples prepared by FA and LA after the activation is the same, the boron implantation amount was high in FA and low in LA.

Figure 3 shows the depth distribution of the carrier concentration measured using the spreading resistance method. In Samples 1 and 2, the anode concentrations are almost identical. On calculating the activation rates from the integrated values of the carrier concentration data, we obtained 1% and 54% for FA and LA, respectively. Furthermore, in the FA sample, 99% of boron atoms are not activated, which indicates that Sample 1 contains more interstitial boron atoms than Sample 2.

III. DLTS MEASUREMENT CONDITIONS

DLTS measurements were carried out under two conditions: in a shallow depletion region and in a deep depletion region. These measurements, including the initial voltage V_0, the reverse voltage V_R, and the calculated depths of the depletion regions are listed in Table II. Because the thickness of Si in the diodes is approximately 100 μm, the region near the middle of the n^- substrate in the thickness direction was analyzed under the deep condition.

TABLE I. Processing conditions of measured samples.

Process	Sample 1	Sample 2	Sample 3
Electron beam irradiation (EI)	Applied	Applied	Not applied
Boron ion dose amount	High	Low	Low
Boron activation	Furnace annealing	Laser annealing	Laser annealing
Leakage current	Large	Small	Extremely small

IV. RESULTS AND DISCUSSION

Figure 4 shows the DLTS signals in the shallow depletion region. Observing the curve for Sample 1 (black), which was subjected to FA, three types of traps were confirmed. In contrast, for Sample 2 (red), which was subjected to LA, the trap signals were smaller; in particular, Trap A was almost undetectable. In Sample 3, which was not irradiated using the electron beam, no trap could be confirmed.

The Arrhenius plots of the DLTS results are shown in Fig. 5. Here, ΔE_T represents the difference between the bottom of the conduction band and the trap energy level. For Trap A, $\Delta E_T = 0.50$ eV. Trap A has the deepest energy level and is located near the center of the Si band gap of 1.11 eV. Theoretically, the energy level near the middle of the bandgap predominately contributes to the leakage current.

Table III summarizes the DLTS results and the calculated trap density in the shallow region. The density of Trap

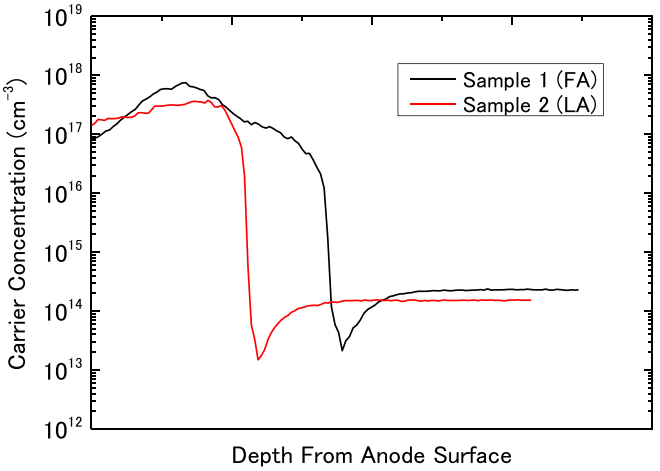

FIG. 3. Depth distribution of carrier concentration measured by the spreading resistance method.

TABLE II. DLTS measurement conditions. "+" indicates a forward bias to the p/n junction, and "−" indicates a reverse bias.

Measurement condition	V_o	V_R	n^- side depletion layer width
Shallow region	+0.3 V	−1.5 V	1 to 4 μm
Deep region	−160 V	−213 V	38 to 44 μm

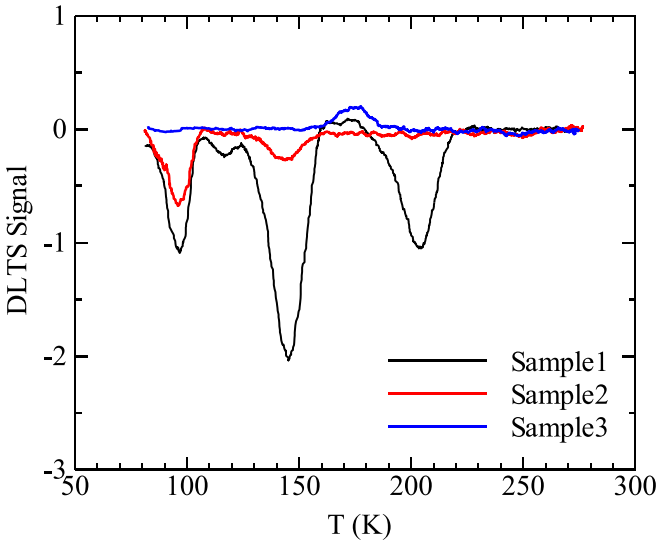

FIG. 4. DLTS signals in the shallow region.

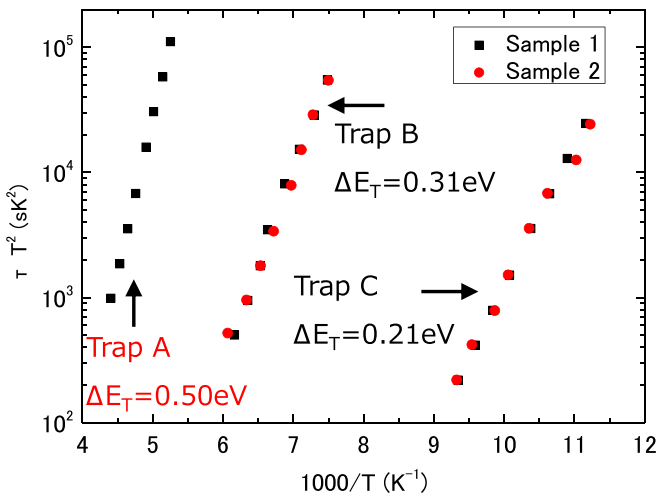

FIG. 5. Arrhenius plots of DLTS results measured in the shallow region.

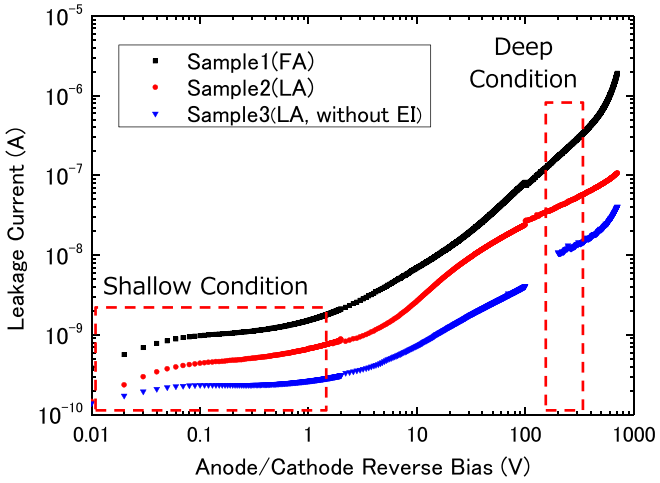

FIG. 6. Leakage current characteristics of the DLTS analyzed samples.

A with the deepest energy level was on the order of $10^{11}\,cm^{-3}$. Furthermore, in Samples 2 and 3, Trap A was undetectable. Therefore, we assume Trap A is interstitial boron[8–10] or a vacancy-substitutional phosphorus pair.[11]

Figure 6 shows the leakage current characteristics of the DLTS analyzed samples. For DLTS analysis under the shallow region condition, a voltage of 1.5 V or less was applied. As can be seen from the figure, for Sample 1 (black), which had a high trap level density, the leakage current was also large. In contrast, for Sample 3 (blue), without the electron beam irradiation, the leakage current was the smallest among the three samples. Therefore, it can be assumed that the trap level density is related to the leakage current.

The DLTS results and Arrhenius plots were measured in the deep region, and are shown in Figs. 7 and 8, respectively. In Sample 3 without EI, no trap signals caused by crystal defects were detected. In Samples 1 and 2, four kinds of traps were detected, with almost identical peaks. We, therefore, hypothesize that the high thermal energy by LA has not reached and affected this area.

Table IV summarizes the DLTS results and the calculated trap density in the deep region. Because there is no interstitial boron in this region, we assume that Trap D is a vacancy-substitutional phosphorus pair. Furthermore, the trap level density was one order of magnitude smaller than that of the shallow region, i.e., $10^{10}\,cm^{-3}$.

Figure 9 shows the superimposed DLTS signals in the shallow and deep regions for Sample 1. To make the peak heights of Trap A and Trap D the same, the signal of the deep region is multiplied by a coefficient. Consequently, the peaks of

TABLE III. Summary of the DLTS results and the trap density calculated in the shallow region.

Index		Trap A	Trap B	Trap C
ΔE_T		0.50 eV	0.31 eV	0.21 eV
Defect (presumed)		Interstitial boron (B_i)[8–10] or vacancy-substitutional phosphorus pair (V-P_s)[11]	Not identified	Vacancy-oxygen pair (V-O_i)[12]
Estimated trap density	Sample 1	$4.0 \times 10^{11}\,cm^{-3}$	$7.8 \times 10^{11}\,cm^{-3}$	$4.2 \times 10^{11}\,cm^{-3}$
	Sample 2	Not detected	$1.1 \times 10^{11}\,cm^{-3}$	$2.5 \times 10^{11}\,cm^{-3}$
	Sample 3	Not detected	Not detected	Not detected

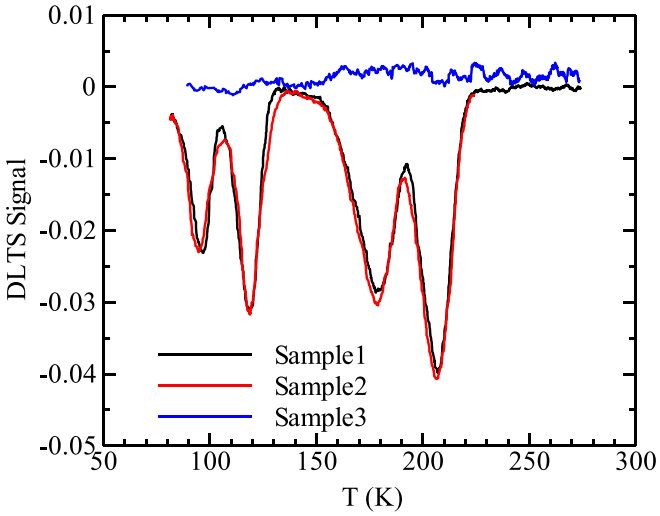

FIG. 7. DLTS result in the deep region.

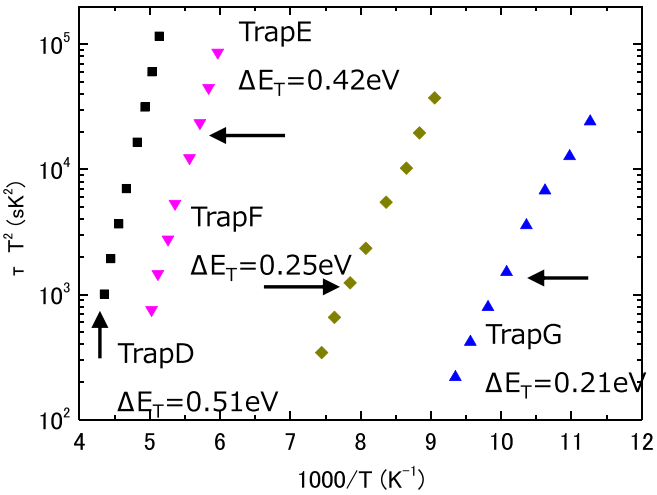

FIG. 8. Arrhenius plots of DLTS results measured in the deep region.

the Traps A and D signals are slightly shifted. Based on this observation, it is possible that Trap A is different from Trap D, or a mixture of two kinds of defects exist. Furthermore, Traps C and G are considered to be the same kind of defect.

In the deep region at the high reverse bias, Samples 1 and 2 had the same defect distribution in the n^- substrate. However, in this reverse bias range, the leakage current of Sample 1 increased more sharply than that of Sample 2, which is shown in Fig. 6; this cannot be explained only by leakage current caused by defects in the n^- substrate.

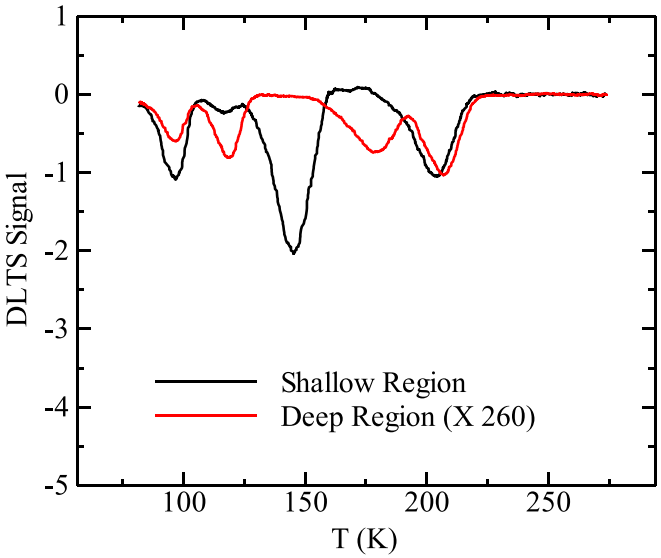

FIG. 9. Superimposed DLTS signals in the shallow and deep regions.

From the DLTS and leakage current results, we presumed the mechanism of leakage current (Fig. 10). At relatively low temperature FA, because the thermal energy is applied evenly in the entire diode, the defects in the n^- substrate are distributed almost uniformly. It is assumed that many defects caused by the boron ion implantation damage remain near the p-n junction. A percentage of the unactivated boron atoms exist as the interstitial boron in the anode p^+.

On the other hand, in LA, the high thermal energy is transmitted from the anode p^+ to the middle of the substrate, and thus the crystal defects in this region are reduced.

At the low reverse bias, these defects near the p-n junction cause a large leakage current in the FA sample.

Because the trap level densities on the cathode n^+ side are the same in the FA and LA samples, it is assumed that the sharp increase in the leakage current in the FA sample at a high reverse bias is caused by the interstitial boron in the slightly expanding depletion region of the anode p^+ side.

V. SUMMARY

In this work, we investigated the correlation between the deep defect level density in the semiconductor bandgap using DLTS and the leakage current when changing the anode activation method of the diode.

Three types of trap levels ($\Delta E_T = 0.51$, 0.31, and 0.21 eV) were confirmed in the region near the p-n junction.

TABLE IV. Summary of the DLTS results and the trap density calculated in the deep region.

Index		Trap D	Trap E	Trap F	Trap G
ΔE_T		0.51 eV	0.42 eV	0.25 eV	0.21 eV
Defect (presumed)		Vacancy-substitutional phosphorus pair (V-P_s)	Interstitial carbon-substitutional phosphorus pair (C_i-P_s)[13]	Divacancy (V_2)[14]	Vacancy-oxygen pair (V-O_i)
Estimated trap density	Sample 1	2.4×10^{10} cm^{-3}	1.8×10^{10} cm^{-3}	1.9×10^{10} cm^{-3}	1.5×10^{10} cm^{-3}
	Sample 2	Same above	Same above	Same above	Same above
	Sample 3	Not detected	Not detected	Not detected	Not detected

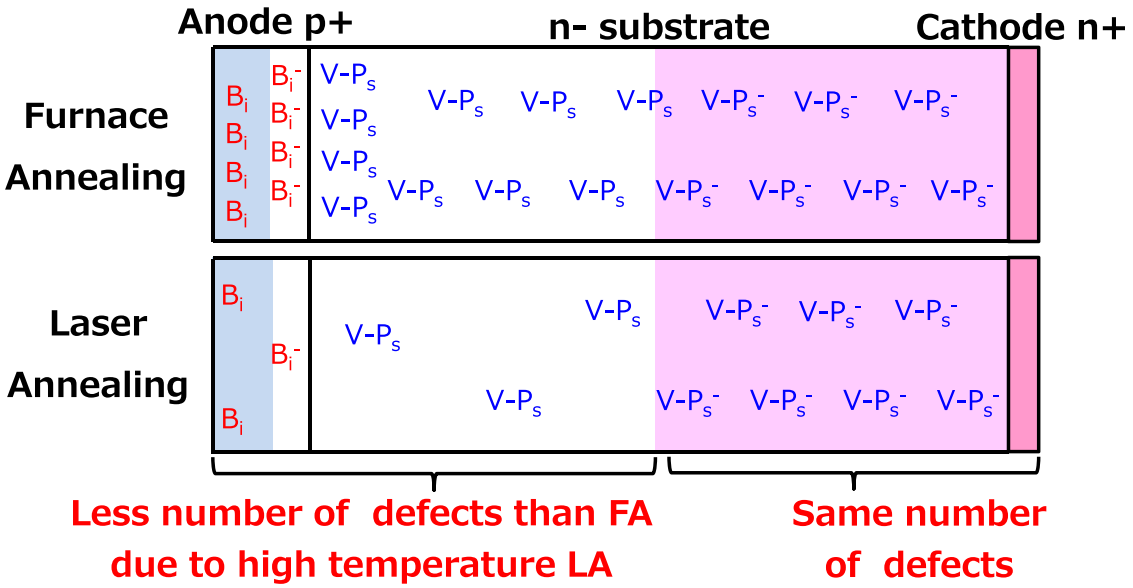

FIG. 10. Schematic cross-sectional illustration of a pin diode indicating the crystal defect distribution.

The density of these three types of traps is large in FA and small in LA. It is presumed that the leakage current at a low reverse bias is primarily caused by the trap with the deepest level, Trap A ($\Delta E_T = 0.51$ eV). In the region, away from the p-n junction, four types of almost identical DLTS signals were obtained in the FA and LA samples. It is assumed that interstitial boron in the p-layer is the reason for the increase in the leakage current of the FA sample at high reverse bias.

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