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Interface states characterization in heterojunction solar cells from *CV–GV* measurements and modeling

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ABSTRACT

A new method is proposed to extract interface states density D_{it} at the hydrogenated amorphous/crystalline silicon interfaces (aSi:H/cSi) of heterojunction solar cells – HET. This technique based on *CV* and *GV* measurements consists in adapting standard electrical D_{it} models for MOS structures to the specific case of HET solar cells. In particular, a parasitic conductance is introduced to account for the high leakage current of the diode in the forward regime. The relevance and accuracy of such an analytical model is then demonstrated by comparison with experimental results and with more complex numerical approaches. Finally, this technique enables us to demonstrate the high quality of the interface of HET solar cells which exhibit D_{it} levels below 10^{11} defects per cm^2.

1. Introduction

Solar cells with hydrogenated amorphous/crystalline Si heterojunctions – HET (aSi:H/cSi) exhibit high efficiency $\eta > 20\%$ while keeping a low thermal budget for a low fabrication cost [1]. But the performance of these photovoltaic cells strongly depends on the density of interface states D_{it} at the aSi:H/cSi interfaces (see Fig. 1). In particular, a large D_{it} density is known to favor the recombination of free carriers at the HET interfaces leading to an increase of the reverse current of the heterojunction. This phenomenon dramatically reduces the open circuit voltage of the solar cell and its efficiency, accordingly [2,3]. Therefore it is fundamental to obtain reliable techniques to extract D_{it} in these structures. In this paper we propose an adaptation of the standard *CV–GV* technique used for MOS capacitors to extract D_{it} of the aSi/cSi interface.

2. Experiment

The samples are made by depositing thin PVD intrinsic ($N_a \sim 10^{15}/cm^3$) hydrogenated amorphous layers aSi:H on polished FZ n-type crystalline Si substrates at 200 °C. An HF dip cleaning is sometimes used before the aSi deposition to remove native oxide and therefore, obtain a good passivation of D_{it} defects. The top contact is made by depositing an evaporated Al electrode (see Fig. 2). *CV–GV* characteristics are measured with an HP4284 LCRmeter at room temperature.

3. Results and discussion

3.1. D_{it} characterization in aSi/cSi structure

Fig. 3 shows band diagrams of MOS and hetero-junction aSi/cSi structures. By comparing both structures, we can consider that the intrinsic aSi layer is actually an "insulator" with a reduced bandgap of 1.7 eV and with a low density of bulk traps $N_{trap} = 10^{16}/cm^2$ [4]. This hypothesis leads us to propose a refined impedance model for the aSi/cSi structure in the depletion regime under small ac excitation (see Fig. 4). Compared to the standard model for MOS capacitor, the oxide capacitance C_{ox} is replaced by the depleted capacitance of the thin aSi film $C_{dep}{}^{aSi} = \varepsilon_{Si}/T_{aSi}$ and an additional conductance $G_{st} = dI/dV$ is considered which accounts for the static leakage current I through the structure. On the other hand, the depletion capacitance in the Si substrate $Cd = \varepsilon_{Si}/W_{dep}$ and, the interface state capacitance C_{it} and conductance G_{it} given in [5,6] are unchanged. The approximation of the aSi capacitance C^{aSi} by its depleted value $C_{dep}{}^{aSi}$ is justified in Fig. 6. Indeed, even for a very low D_{it} density of 10^{10} traps/cm^2, the variation of the trapped charge in the aSi bulk traps $\Delta Q_{trap}{}^{aSi}$ remains negligible compared to the variation of the interface state charge ΔQ_{it} and to the variation of the electron density Δn in the cSi substrate. By dividing each charge variation ΔQ by the variation of the HET surface potential $\Delta\Psi_s$, we then obtain that the capacitance associated to the aSi bulk traps $C_{trap}{}^{aSi} = \Delta Q_{trap}{}^{aSi}/\Delta\Psi_s$ is negligible compared to the D_{it} capacitance $C_{it} = \Delta Q_{it}/\Delta\Psi_s$ and to the desertion capacitance Cd also given by $q\Delta n/\Delta\Psi_s$. As a result, we deduce that the capacitance

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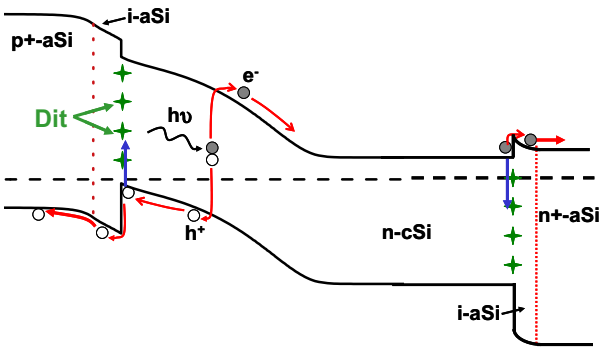


Fig. 1. Band diagram of a complete HET solar cell. Efficiency of the solar cell strongly depends on the interface state density D_{it} at the aSi:H/cSi interfaces.

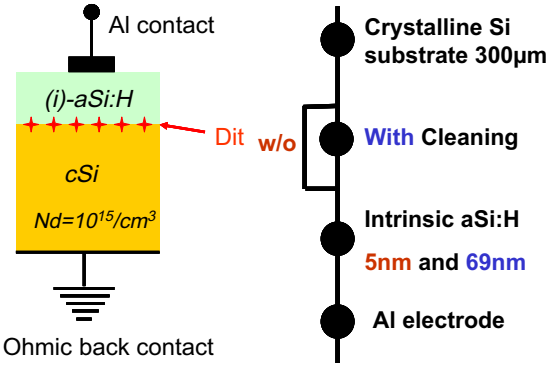


Fig. 2. Simplified hetero-structure aSi:H/cSi to characterize D_{it}. The emitter only consists of a 5 or 69 nm intrinsic amorphous layer.

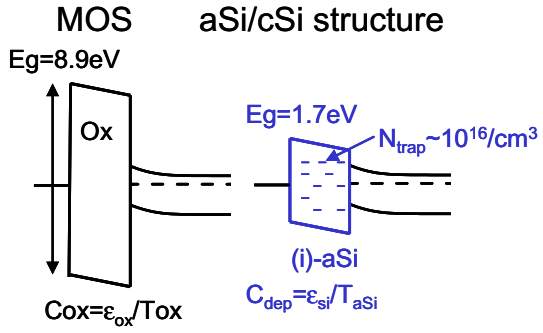
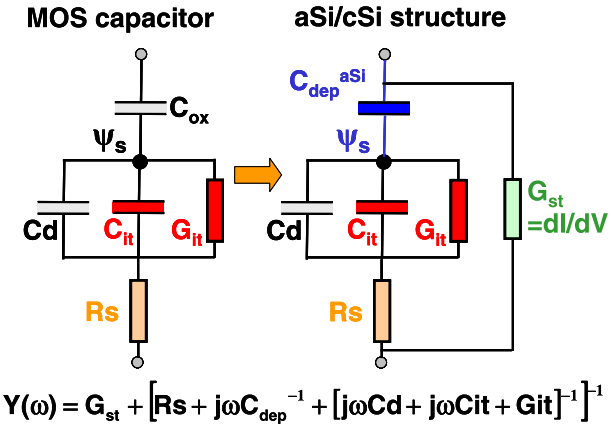


Fig. 3. Comparison of a MOS structure and of an aSi/cSi heterojunction. The intrinsic amorphous layer aSi can be seen as an oxide with a reduced bandgap E_g = 1.7 eV and with a low amount of bulk traps $N_{trap} \sim 10^{16}/cm^3$.



$$Y(\omega) = G_{st} + \left[Rs + j\omega C_{dep}^{-1} + \left[j\omega Cd + j\omega Cit + Git\right]^{-1}\right]^{-1}$$

Fig. 4. Adaptation of the impedance model under small ac signal to aSi/cSi structure.

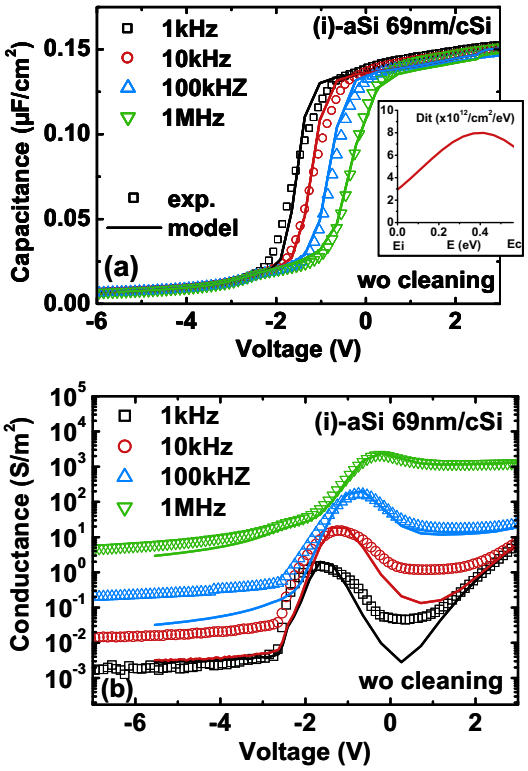


Fig. 5. (a) and (b): Comparison model-experiment of *CV* and *GV* data. Analytical aSi/cSi model presented in Fig.4. Case without interface cleaning.

C^{aSi} of the aSi film, which can be considered as the sum of C_{trap}^{aSi} and C_{dep}^{aSi}, is equal here to C_{dep}^{aSi}.

Fig. 5 (a) and (b) shows the simulations compared to measured *CV* and *GV* characteristics for the 69 nm aSi/cSi structures without the Si cleaning step. The analytical model perfectly fits the experimental data at each frequency, considering a huge density of interface states $D_{it}^{max} = 8.10^{12}/cm^2$. It can be pointed out that such high D_{it} levels at the aSi/cSi interface induces peaks in the *GV* characteristics and frequency dependence of the *CV* curves in the depletion regime [−2, 0 V], similarly to what is observed in MOS structures [5,6]. This is due to the fact that the total capacitance *C* and conductance *G* of the structure is here strongly affected by the response of the interface states. In particular, *C* is only the association in parallel of C^{aSi} and of $Cd + C_{it}$ and an analytical expression of G can be derived:

$$G = \frac{G_{it}(\omega C^{aSi})^2}{G_{it}^2 + \omega^2 (C_{it} + C^{aSi})^2}.$$

In the forward regime of the diode $V > 0$, the conductance *G* is then rather affected by the static leakage current at low frequencies i.e. $G \sim G_{st}$ and by series resistance at high frequencies.

Moreover, it is worth noticing that the large D_{it} density is due here to the lack of the Si surface preparation. Dramatic improvements can be achieved after cleaning as it is shown in the next paragraphs.

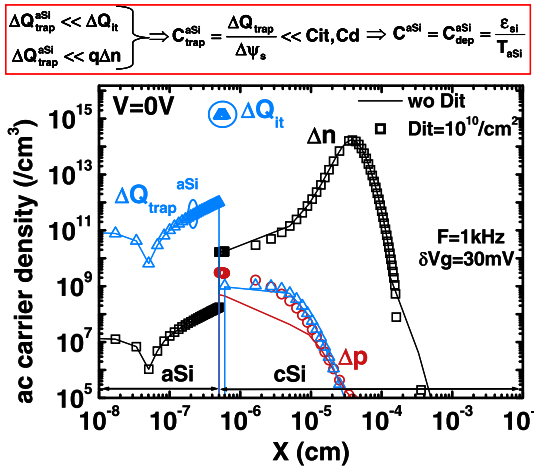


Fig. 6. Carrier density modulation under small ac signal δV given by the AFORS HET simulator. Even for very low D_{it} density $D_{it} = 10^{10}/cm^2$, ΔQ_{it} dominates over the trapped charge in the aSi layer ΔQ_{trap}^{aSi}.

3.2. Comparison to numerical models

Fig. 7 compares the *CV* electrical response of interface defects given by this analytical model to the results of the numerical simulator AFORS-HET 2.4 [7] which is dedicated to heterojunction solar cells. In spite of the simplifications made by our model on the aSi layer, a good agreement between both models is obtained in the depletion regime [−1, 0.2 V], where the interface states respond. In the forward diode regime $V > 0.2$ V, both models differ but neither of the two reproduce the experimental results. This result again confirms that our analytical model is reliable and accurate for a D_{it} extraction in these solar cells. Moreover, Fig. 8 shows that this analytical model is even more effective to extract D_{it} from *GVs* than the AFORS model for two reasons: (1) it allows a better identification of the D_{it} response on the total *GV* characteristic and (2) it better takes into account the impact of leakage current on the *GV* curve at high *V* by directly estimating G_{st} from a static *IV* measurement.

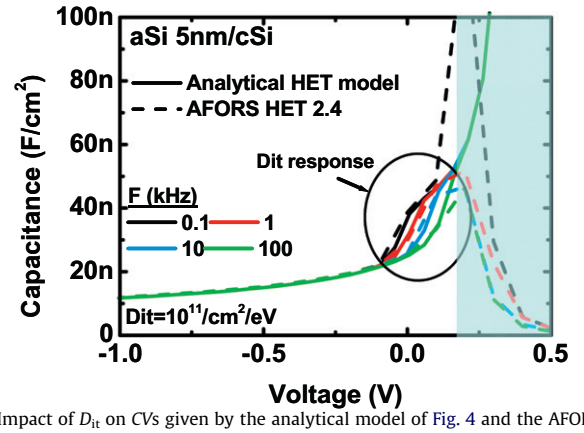


Fig. 7. Impact of D_{it} on *CVs* given by the analytical model of Fig. 4 and the AFORS-HET simulator. Good agreement between both models is observed on the D_{it} response.

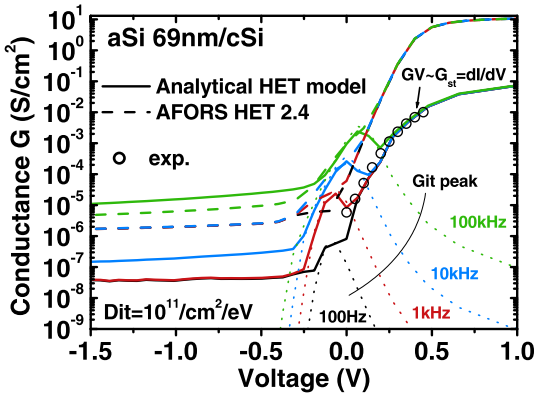


Fig. 8. Impact of D_{it} on *GVs* given by both models. The analytical model better models the impact of leakage current on *GVs*, allowing a better D_{it} extraction.

3.3. Sensitivity of the technique and D_{it} on optimized HET solar cells

The sensitivity of the technique to evaluate D_{it} in well passivated aSi:H/cSi structures (after cleaning) is shown in Figs. 9 and 10. For thin aSi films $T_{aSi} = 5$ nm, the sensitivity is rather poor since it significantly depends on the capture cross-section σ of the traps. The minimum D_{it} value detected by the technique is $\sim 10^{11}/cm^2$ and $\sim 10^{12}/cm^2$, for high and low σ, respectively. This result confirms previous results reported by other authors [8]. For the thick and low leaky aSi films $T_{aSi} = 69$ nm, the sensitivity is greatly improved even for low σ values. The resolution of the method is in this case estimated to 10^{11}charges/cm^2. Measured D_{it} are here

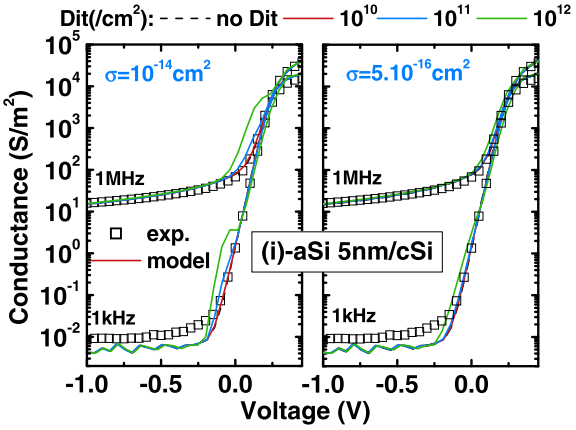


Fig. 9. Sensitivity of the analytical model to extract D_{it} in aSi 5 nm/cSi structures with cleaning. Sensitivity strongly depends on the capture cross-section of the traps σ.

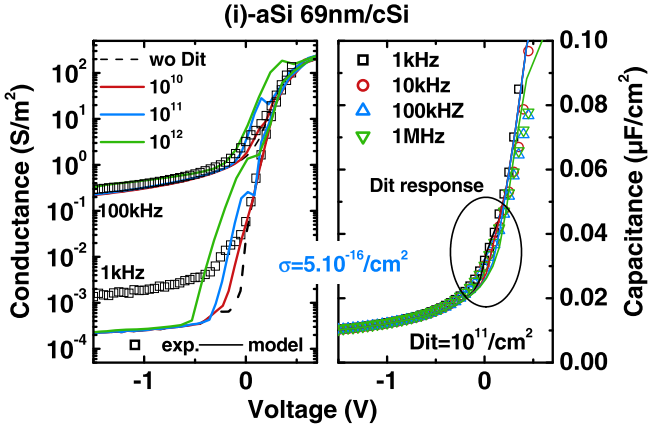


Fig. 10. Sensitivity is greatly improved in thick 69 nm (i)-aSi films with cleaning, even for low σ. Maximum D_{it} is below 10^{11} traps/cm^2 in these structures.

under the resolution. It demonstrates the high quality of the aSi/cSi interface prepared at low thermal budget in HET solar cells.

4. Conclusion

CV–GV techniques to extract D_{it} in MOS capacitors are revisited for characterizing D_{it} in aSi/cSi interfaces of solar cells. A refined analytical model is proposed and compared to numerical approaches. This model well explains experimental results and allows us to demonstrate the high quality of the (i)-aSi:H/cSi interface which exhibit D_{it} levels below 10^{11} defects per cm^2.

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