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A deep-level transient spectroscopy study of p-type silicon Schottky barriers containing a Si–O superlattice

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The presence of deep levels in a silicon–oxygen (Si–O) superlattice (SL) deposited on p-type silicon substrates has been investigated by deep-level transient spectroscopy (DLTS) on thermally evaporated Cr Schottky barriers (SBs). The SLs have been fabricated with different thicknesses of the silicon interlayers, formed by chemical vapor deposition. It is shown that a broad band of hole traps is present near the surface of the SB, which is associated with the SL. In addition, the activation energy corresponding with the peak maximum shifts to higher values with respect to the valence band and gives rise to a higher trap concentration with increasing silicon interlayer thickness. It is proposed that these states are associated with the structural defects found in similar SL structures, that is, with the epitaxial quality and not with the Si–O bonds in the atomic layers. The change in the DLT-spectra with silicon thickness could be related with the transformation of the structural defects from small self-interstitial clusters to stacking faults.

1 Introduction As the 90 nm complementary metal–oxide–semiconductor (CMOS) technology node, strain engineering has proven to be one of the essential techniques for boosting the device performance, beyond the conventional dimensional scaling. However, at the current stage it becomes more and more difficult to reach higher strain levels for enhancing the carrier mobility. This explains the interest in recent years in alternative methods for mobility boosting, like the use of a silicon–oxygen (Si–O) superlattice (SL) [1–9]. This consists of a sequence of an oxygen atomic layer (AL) and a few nanometer thin silicon epitaxial layer, extending over several periods. It is believed that the presence of the oxygen AL breaks the lattice symmetry and gives rise to a lower effective mass parallel with the oxygen planes, that is, in the transport direction [5, 6]. Crucial in the mobility enhancement of metal–oxide–semiconductor (MOS) transistors containing a Si–O SL is the good structural quality of the epitaxial layer. It has been recently shown that the presence of stacking faults in the top layers of chemical vapor deposition (CVD) grown 5-period SL have an impact on the degradation of the hole mobility [10]. This can be improved by reducing the thickness of the silicon interlayers from 3 to 1.5 nm, which also lowers the surface roughness, as evidenced by cross-sectional transmission electron microscopy (TEM) [7–10]. In addition, the lower carrier mobility compared to the reference MOSFETs has been ascribed to the presence of deep level traps [10]. A detailed deep-level transient spectroscopy (DLTS) study on MOS capacitors with 1 nm SiO_2 + 4 nm Al_2O_3 as a gate stack has revealed the presence of a broad distribution of near mid-gap hole traps in p-type silicon [11]. At the same time, it was demonstrated that the deep levels associated with the presence of the SL are quite sensitive to the thermal budget, that is, a post-deposition Forming Gas Anneal (FGA) between 300 and 500 °C [11]. This implies that the deposition of the gate stack may have changed already the observed deep levels from the as-grown state. In addition, it is hard to separate the contribution of SL traps from the ones related with the Si/SiO_2 interface, in DLT-spectra obtained on MOS capacitors. Therefore, in this study, the deep levels

associated with 5-period Si–O SL on p-type Czochralski (Cz) silicon substrates are investigated by DLTS performed on thermally evaporated Cr Schottky barriers (SBs), with the thickness of the silicon interlayer as the main variable.

2 Experimental DLTS has been performed on Cr SBs thermally evaporated on p-type Cz silicon substrates, containing a 5-period SL, with either 1, 3, or 7 nm silicon epitaxial interlayers. Prior to evaporation, an HF dip was applied to remove the native oxide. A sample with no SL (0 periods) and 11 nm epitaxial silicon deposited on the p-type Cz substrates under the same CVD conditions has also been investigated as a reference. The use of a SB in this case eliminates the thermal budget associated with the gate stack processing and at the same time, reduces the impact of possible interface states in the DLT-spectra.

The SL have been grown in a 200 mm ASM Polygon cluster, where the wafers are shuttled between an atomic layer deposition (ALD) reactor and a CVD chamber. Before the start of the deposition, a high temperature pre-epi bake in H_2 is executed in the CVD chamber to remove the native oxide. The O AL are deposited on a H-terminated Si (001) surface using O_3 as a precursor at a temperature T of 50 °C. Si epitaxial deposition is carried out based on SiH_4 in N_2 carrier gas at 500 °C, in order to preserve the integrity of the oxygen (sub) monolayer. For the growth of defect-free SLs, a careful optimization of the growth conditions is required, as described in detail elsewhere [7–10]. In order to have good structural quality epitaxial layers, it is essential to have a sub AL growth, where O atoms at dimer/back bonds can still provide a template with nucleation sites (H–Si and H–Si–O–Si) for the epitaxial ordering of silicon thereon [12].

The diameter of the Schottky barriers was 0.5 mm, yielding well-behaving current–voltage (*I–V*) characteristics at room temperature (RT) (Fig. 1). One can clearly discern the impact of the presence of the SL, resulting in a lower forward and reverse current. This suggests an increase of the SB height for increasing thickness of the silicon interlayer. On the other hand, no marked impact on the reverse capacitance–voltage (*C–V* at 1 MHz) was found. A uniform doping density profile was obtained for the SL samples with a p-type doping concentration in the range of $0.8–1.2 \times 10^{15}\,cm^{-3}$. From the steep decay of the capacitance in forward operation, it was concluded that the native oxide film has been successfully removed not to affect the Schottky barrier characteristicss.

T-scan DLTS has been performed in the range 75–300 K with different bias pulses from V_R to V_P, with a duration t_p of 1 ms typically. A sampling period t_w of 51.2 ms has been applied, which defines the hole emission time constant of the spectra. The latter are based on the b1 sine Fast Fourier Transform coefficient [11]. As an example, Fig. 2 shows the spectra for a bias pulse in depletion ($-1\,V \rightarrow 0\,V$), probing the depletion region in the silicon substrate from about 1 to 0.5 μm. In order to measure the SL states close to the surface, a forward bias

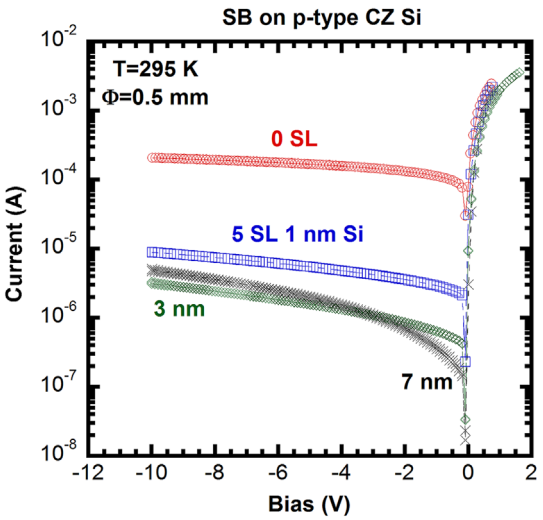

Figure 1 Current–voltage characteristic at room temperature for a 0.5 mm Cr Schottky barrier on p-type silicon, containing different Si–O superlattices: 0 (= 11 nm Si epitaxial reference) or 5 periods with 1, 3, or 7 nm between the oxygen atomic layers.

pulse from 0 to +0.7 V (approximately flat band voltage; the depletion width ranges from ~0.5 μm to the surface) is applied as well.

3 Results and discussion As can be seen in Fig. 2, there is a significant difference in the spectrum corresponding with the p-type Cz silicon substrate and with the near-surface layer, where the SL is situated. In the silicon depletion region, a minor peak appears to be present at 270 K, whose identity is unknown and not relevant for the current work, given the small concentration at the detection

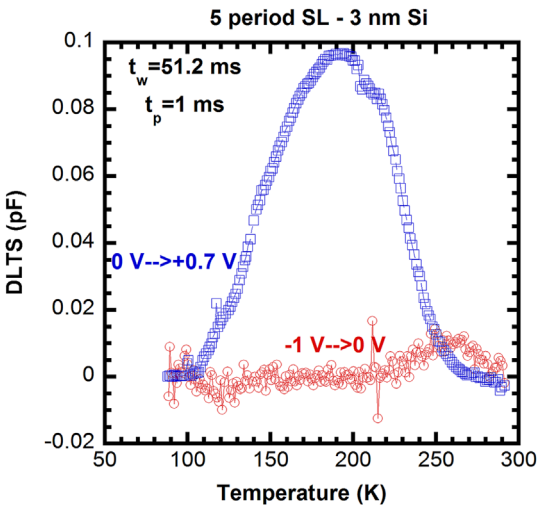

Figure 2 Temperature scanned DLT spectra for a 5-period SL sample on p-type Cz Si with 3 nm Si thickness, corresponding with a bias pulse in depletion ($-1\,V \rightarrow 0\,V$) and up to flat-band conditions ($0\,V \rightarrow +0.7\,V$). The sampling period $t_w = 51.2$ ms and the pulse duration $t_p = 1$ ms.

limit of the set-up. On the other hand, a pronounced band at ~200 K appears close to the surface. The peak is also broader as for a typical point defect, suggesting a distribution of energy levels in the silicon band gap. The peak maximum, using a standard Arrhenius analysis, corresponds with an activation energy $E_T = 0.44 \pm 0.01$ eV and a hole capture cross section of $\sigma_p = 2.0 \times 10^{-16}$ cm^2. Compared with previous results on MOS capacitors, the energy levels are closer to the valence band maximum E_V and also exhibit a higher σ_p [11].

According to the spectra of Fig. 3, another important factor determining the hole trap spectra is the thickness of the silicon layer in between the oxygen ALs. The measurements have been performed using the same pulse condition from 0 to +0.7 V for 1 ms, probing the deep states associated with the 5-period SL and demonstrating some clear trends. First of all, the 1 nm case exhibits a very broad band of hole traps, with a fairly low amplitude, that is, concentration. The peaks become narrower and higher for increasing silicon thickness, indicating overall a higher hole trap concentration. In the 7 nm case, the peak corresponds to a density on the order of 5×10^{13} cm^{-3}. However, this underestimates the true trap concentration for two reasons: one, the SL only covers a small fraction of the total depletion region at 0 V – a crude estimate indicates that it amounts to only 3–4%, so that a correction factor of 25–30 should be applied (7 nm Si). In addition, as shown in Fig. 4, the peak height is not saturated for a pulse duration of 1 ms. This implies that not all acceptor states are being filled at 1 (or even 10) ms.

Note also a minor hole trap in the no SL reference SB. Its origin is unclear for the moment but it could be related with hole traps at the silicon substrate/epi interface, for example, by an incomplete removal of native oxide or organics prior to the start of the epi deposition.

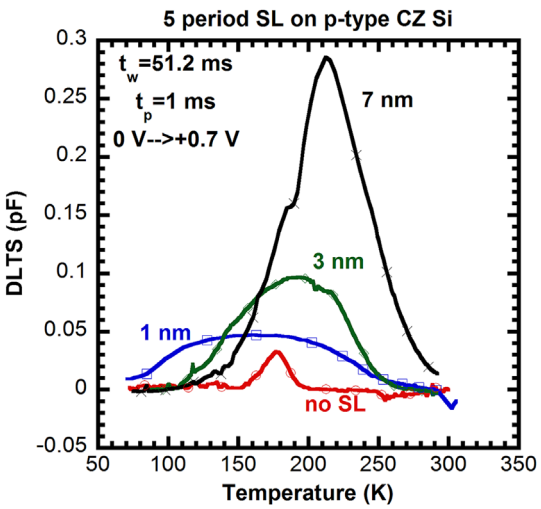

Figure 3 Temperature scanned DLT spectra for a pulse into flat-band (0 V → +0.7 V), for 5-period SL samples on p-type Si with 1, 3, or 7 nm silicon in-between the oxygen atomic layers. A 0 SL reference spectrum is also included. The sampling period $t_w = 51.2$ ms and the pulse duration $t_p = 1$ ms.

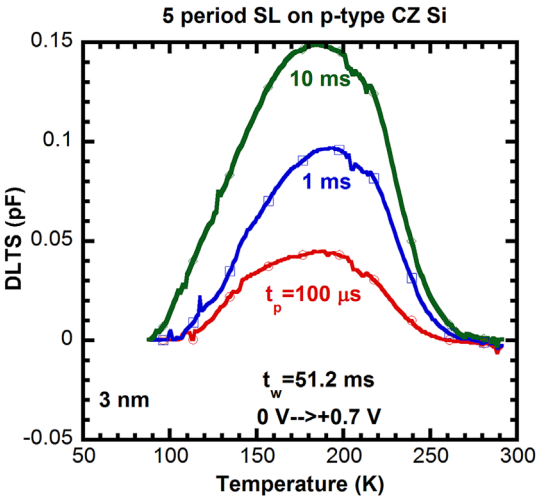

Figure 4 Temperature scanned DLT spectra for a pulse into flat-band (0 V → +0.7 V), for a 5-period SL sample on p-type Si with 3 nm silicon in between the oxygen atomic layers. The spectra have been recorded for different t_p: 100 µs, 1 ms, and 10 ms. The sampling period $t_w = 51.2$ ms.

Another obvious trend is that the activation energy of the deep levels becomes higher for a higher silicon thickness. For the 7 nm SL, a value for E_T of 0.47 eV and a $\sigma_p \sim 5 \times 10^{-14}$ cm^2 has been derived from an Arrhenius plot. The activation energy is close to the value that has been obtained on a MOS capacitor containing a 5-period SL, after FGA at 500 °C [11]. It confirms the interpretation that two types of hole traps were found in these MOS capacitors with a Si–O SL: near mid-gap states which can be easily passivated by the FGA and most probably reside at the Si/SiO_2 interface and the SL related states, which are resistant to FGA at 500 °C. The fact that these mid-gap hole traps are absent in the spectra obtained on the SBs in Figs. 2 and 3 support the idea that they are related with (near) interface states and not with the Si–O SL.

A final piece of important information is the non-saturation of the trap filling in the 100 µs–10 ms range, showing more or less a constant increase of the peak amplitude per decade of filling pulse duration. This is, in fact, the typical behavior for deep levels associated with extended defects, like dislocations [13–16] or stacking faults [17, 18] in silicon. One reason for the slightly different capture behavior of the deep levels studied here compared with typical extended defects could be the fact that the defects occur very locally close to the surface. Most likely, this requires a more refined analysis of the DLTS spectra, perhaps based on TCAD simulations considering a very local distribution of defects. Another factor which could play a role is the ratio of available free hole density and trap density. If they are of similar magnitude, the trap filling kinetics could also deviate from the pure exponential behavior expected for a point defect, especially at longer t_p. Summarizing the observations, it is concluded that

the presence of an oxygen SL creates a broad band of hole traps in p-type Si, with increasing trap density and activation energy when a thicker silicon interlayer is used, going from 1 to 7 nm.

Based on the above arguments, it is now possible to speculate on the nature of the deep hole traps which are associated with oxygen SLs in p-type Si. First of all, one could consider some type of Si–O bond or a Si dangling bond (P_b centre) to be responsible for the hole traps [1, 9, 19, 20]. However, a recent Electron Spin Resonance (ESR) study has indicated the absence of P_b centres or other paramagnetic defects in Si–O SL within the detection limit of the technique [21]. It was concluded that the oxygen AL is a well passivated surface, with small electrically active unsatisfied or dangling bonds.

There could also be an analogy or link with the defects formed during silicon oxidation or oxide precipitation, which leads to an expansion of the silicon lattice. The resulting elastic strain is usually relaxed by the emission of self-interstitials in the lattice which can agglomerate to form stacking faults [17, 18] or interstitial cluster defects, like {311} rod-like defects at $T \geq 600\,^{\circ}\mathrm{C}$ [22–24]. In p-type Si, stable interstitial clusters formed above 600 °C yield two defect signatures at $E_V + 0.33\,\mathrm{eV}$ and $E_V + 0.52\,\mathrm{eV}$ [25], comprising the range of activation energies found for the SL peaks in Fig. 3. These interstitial clusters exhibit features of extended defects over part or most of their filling kinetics, depending on their size [25].

Of course, the origin of the extended defects, that is, SFs, in the case of the Si–O SLs is related to the low-temperature epitaxial growth process [10, 12], where it has been observed that the defect density increases with the silicon thickness, as evidenced by cross-sectional TEM. It has been shown that silicon epitaxy on the oxygen AL is nucleated at oxygen-free areas, which overgrow the SL and merge to form a continuous epitaxial layer [12]. Defects can be formed at the meeting point of two silicon overgrowth regions; their size will depend on the interlayer thickness. This may also affect the corresponding deep level spectrum, as in the case of growing interstitial clusters.

The fact that we still see some trace of extended defects for the good quality 1 nm Si SL indicates that DLTS is more sensitive to small densities of interstitial clusters/SFs than cross-sectional TEM, which loses accuracy if the defect density becomes smaller than $\sim 10^8\,\mathrm{cm}^{-2}$. The evolution of the spectra with silicon thickness should then also be connected with the dominant size/nature of the extended defects, where perhaps smaller interstitials clusters occur for the 1 nm case, compared with the 7 nm Si SL, due to the lower deposition time at 500 °C.

Note finally, that the increase of the SB height with the Si thickness (Fig. 1) can be explained by the presence of a high density of hole traps near the surface which pins the Fermi level closer to mid gap than without a SL.

4 Conclusions It has been shown that the hole trap bands associated with 5-period Si–O SLs in p-type silicon shift to a higher activation energy for an increasing silicon interlayer thickness. At the same time, the density of deep level defects increases. Based on the non-saturating trap filling kinetics, it is suggested that the hole traps are associated with the extended defects (SF, . . .) formed during the CVD deposition of the silicon epi layers.

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