

# Improvements on high voltage capacity and high temperature performances of Si-based Schottky potential barrier diode\*

Wang Yongshun(王永顺), Rui Li(芮丽), Adnan Ghaffar(安恒心), Wang Zaixing(汪再兴)<sup>†</sup>, and Liu Chunjuan(刘春娟)

School of Electronic and Information Engineering, Lanzhou Jiaotong University, Lanzhou 730070, China

**Abstract:** In order to improve the reverse voltage capacity and low junction temperature characteristics of the traditional silicon-based Schottky diode, a Schottky diode with high reverse voltage capacity and high junction temperature was fabricated using ion implantation, NiPt60 sputtering, silicide-forming and other major technologies on an N-type silicon epitaxial layer of 10.6–11.4  $\mu\text{m}$  and  $(2.2\text{--}2.4) \times 10^{15} \text{ cm}^{-3}$  doping concentration. The measurement results show that the junction temperature of the Schottky diode fabricated can reach 175  $^{\circ}\text{C}$ , that is 50  $^{\circ}\text{C}$  higher than that of the traditional one; the reverse voltage capacity  $V_R$  can reach 112 V, that is 80 V higher than that of the traditional one; the leakage current is only 2  $\mu\text{A}$  and the forward conduction voltage drop is  $V_F = 0.71 \text{ V}$  at forward current  $I_F = 3 \text{ A}$ .

**Key words:** Schottky potential barrier diode; breakdown voltage;  $I$ – $V$  characteristics; NiPt60 sputtering; junction temperature

**DOI:** 10.1088/1674-4926/36/2/024013

**PACC:** 7340C; 7340L

**EEACC:** 2560H

## 1. Introduction

The Schottky potential barrier diode (SBD) is a majority carrier device operating under the mechanism of a metal–semiconductor contact potential barrier. It has many advantages such as low forward voltage drop, high frequency, low power consumption and large current capacity. The SBD is widely used in high frequency rectification, switching and protecting circuits in the low voltage and high current application regions, such as DC/AC frequency converter and switching power supply circuits.

In recent years, a great deal of research work on the SBD has been done for high frequency, high power application. Measurements of isothermal and non-isothermal DC characteristics of SiC Schottky barrier diodes were presented in 2010<sup>[1]</sup>. Static and dynamic characteristics of 1200 V SiC devices (JFETs and Schottky diodes) used in the WGS DC/AC converter were investigated in depth in 2011<sup>[2]</sup>. High modulation of the device current (on/off ratio of 10(5)) was achieved by adjusting the gate voltage to control the graphene–silicon Schottky barrier in 2012<sup>[3]</sup>. In order to reduce the electric field at the Schottky interface and decrease the reverse leakage current, a novel trench junction barrier Schottky structure was developed in 2013<sup>[4]</sup>.

In this paper, an SBD with high voltage capacity and excellent temperature performance has been successfully fabricated by using NiPt60 sputtering. Therefore, it is anticipated that a widespread application perspective will arise because of its simple manufacturing technological processes and the low price of silicon.  $I$ – $V$  characteristics of the 3 A/100 V SBD manufactured and key factors that influence the performance

of the SBD in the fabrication processes were theoretically analyzed in detail. The optimum technological processes for fabricating an SBD with excellent reverse voltage and high temperature performance are also given.

## 2. Experimental procedure

In order to study and improve the reverse voltage capability and high temperature performance, an SBD with new structure was designed and fabricated on an N-Si epitaxial layer whose thickness is 10.6–11.4  $\mu\text{m}$ , doped As concentration is  $(2.2\text{--}2.4) \times 10^{15} \text{ cm}^{-3}$  and crystal orientation is  $\langle 111 \rangle$ . The effective junction area of the SBD is  $50.5 \times 50.5 \text{ mil}^2$ . The main technological processes for fabricating an SBD with the new structure are described as follows.

(1) Initially, a 6952  $\text{\AA}$  thick  $\text{SiO}_2$  film was thermally grown on the epitaxial layer at 950  $^{\circ}\text{C}$  in oxygen atmosphere.

(2) The photo-resist pattern was determined by masking and the  $\text{SiO}_2$  film was selectively etched for the B ion implantation to form a  $\text{P}^+$  protecting ring.

(3) A B ion dose of  $6.50 \times 10^{15} \text{ cm}^{-2}$  was implanted with a flow of 1000  $\mu\text{A}$  at an energy of 56 keV.

(4) The chip was annealed at 1070  $^{\circ}\text{C}$  in  $\text{O}_2$  atmosphere for 600 min and an  $\text{SiO}_2$  film of 7335  $\text{\AA}$  was grown on the base region.

(5) The lead opening was etched by photo-resist patterning to form the Schottky contact. A NiPt60 alloy layer about of  $6.2 \times 10^{-6} \text{ cm}$  was sputtered at 75  $^{\circ}\text{C}$  in a vacuum of  $1.5 \times 10^{-6} \text{ Torr}$ .

(6) An excellent Schottky contact was formed by thermal silicide-forming treatment at 540  $^{\circ}\text{C}$  in nitrogen atmosphere

\* Project supported by the National Natural Science Foundation of China (No. 61366006), the Research Projects of Higher Education, Gansu's Ministry of Education (No. 213019), and the Fundamental Research Funds for Gansu Provincial Finance Department (No. 213048).

<sup>†</sup> Corresponding author. Email: zaixw@mail.lzjtu.cn

Received 5 July 2014, revised manuscript received 22 October 2014

© 2015 Chinese Institute of Electronics

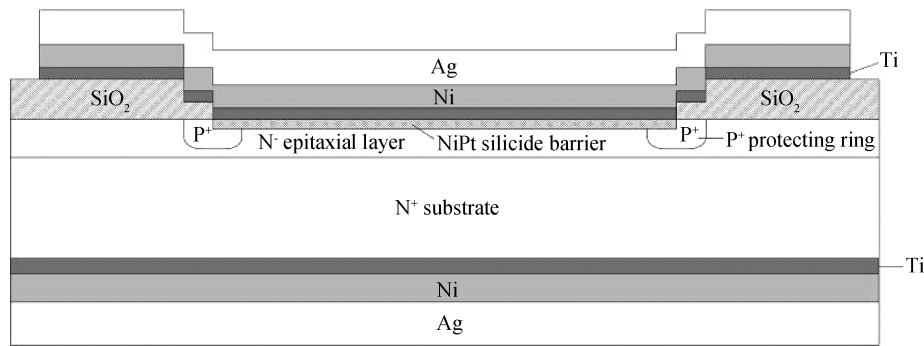


Figure 1. Cross-section of designed Schottky diode structure.

with a small amount of oxygen for 60 min.

(7) The unnecessary NiPt60 alloy not participating in the silicification reaction was removed by etching in  $\text{H}_2\text{SO}_2 : \text{H}_2\text{O}_2 = 4 : 1$  fluid.

(8) A combination metal film of  $158 \text{ \AA}$  Ti /  $5006 \text{ \AA}$  Ni /  $40000 \text{ \AA}$  Ag used as an internal Ohmic contact on the front side was evaporated at  $150^\circ\text{C}$  for 180 min.

(9) The metal electrode on the front side was reversely etched and annealed at  $420^\circ\text{C}$  in nitrogen atmosphere for 90 min to form a good Ohmic contact.

(10) The thickness of the wafer was reduced from the backside to eliminate the stress.

(11) A complex metal electrode of three layers ( $172 \text{ \AA}$  Ti /  $3012 \text{ \AA}$  Ni /  $12030 \text{ \AA}$  Ag) was evaporated on the backside at  $150^\circ\text{C}$  for 90 min.

The designed structure of the SBD is shown in Figure 1.

### 3. Device structure description and analysis

This device was designed to be surrounded with a  $\text{P}^+$  protecting ring and having metal complex field electrodes. The designed structure with the protecting ring can remarkably improve the reverse  $I$ - $V$  characteristics of the SBD. For the identical silicon substrate and epitaxial layer, an SBD without the protecting ring has low reverse breakdown voltage and large leakage current<sup>[5]</sup>. By increasing the length of the metal field electrode, the reverse breakdown voltage of the SBD was slightly raised. However, a too long metal field electrode will cause an increase in chip area and fabrication cost, and further its reverse breakdown performance is also not satisfactory<sup>[6, 7]</sup>.

The technological process for making the metal electrode of a traditional NiSi/Si SBD has been significantly improved by doping 60% Pt element into NiSi/Si potential barrier metal, forming a uniform NiPt60 alloy by low temperature magnetron sputtering. This technological process can effectively raise the temperature resistance of SBD junctions, making them normally operate in the high temperature and large current region.

A 3 A/100 V SBD can normally operate in the reversely biased mode at  $175^\circ\text{C}$ , that is  $50^\circ\text{C}$  higher than the  $125^\circ\text{C}$  of a traditional SBD. At the same time, the reverse voltage capacity of this device was also significantly improved and its operation was reliable and steady.

## 4. Results and discussion

### 4.1. Forward characteristics

Degradation testing was conducted on the designed and fabricated Schottky diode by applying voltage at  $175^\circ\text{C}$ . The forward  $I$ - $V$  characteristics of the 3 A/100 V SDB measured with a TYPE576 curve tracer at  $175^\circ\text{C}$  is shown in Figure 2, with a forward conduction voltage drop of about 0.4 V and working in the low current density region. The  $\ln I$ - $V$  relationship of SBD exhibits a linear profile and indicates an  $I$ - $V$  relationship that obeys the characteristic equation of an ideal Schottky diode.

$$I = I_S \exp \frac{eV}{nkT} \left[ 1 - \exp \left( -\frac{eV}{kT} \right) \right], \quad (1)$$

where  $n$  is the ideal factor that has magnitude 1 for the ideal condition and describing the forward  $I$ - $V$  characteristics of the Schottky junction, and  $I_S$  is the reverse saturation current expressed as

$$I_S = AA^*T^2 \exp \left( -\frac{e\Phi_B}{kT} \right), \quad (2)$$

where  $A^* = 110 \text{ A}/(\text{cm}^2 \cdot \text{K}^2)$  (for N-Si), the effective Charlie Johnson constant,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature,  $e$  is the electronic charge, and  $A$  is the junction area.

When the biased voltage is higher than  $3kT/e$  and the influence of series resistance is ignored, then the magnitude of  $n$  can be approximately expressed as

$$n = \frac{e}{kT} \frac{\partial V}{\partial \ln I}. \quad (3)$$

The height of the Schottky potential barrier can be calculated according to the following equation:

$$\Phi_B = \frac{\ln(A^*T^2/I_S)}{e/kT}. \quad (4)$$

If the forward voltage drop  $V_F$  is 0.71 V, then the forward current  $I_F$  will be 3 A. The ideal factor  $n = 1.3$  and  $I_S = 2.085 \times 10^{-9} \text{ A}$  are obtained from the curve in Figure 2; the height of the Schottky potential barrier  $\phi_B = 0.83 \text{ eV}$  is acquired by a simple calculation. The mechanism underlying the current transportation in the SBD is in accordance with thermal electronic emission.

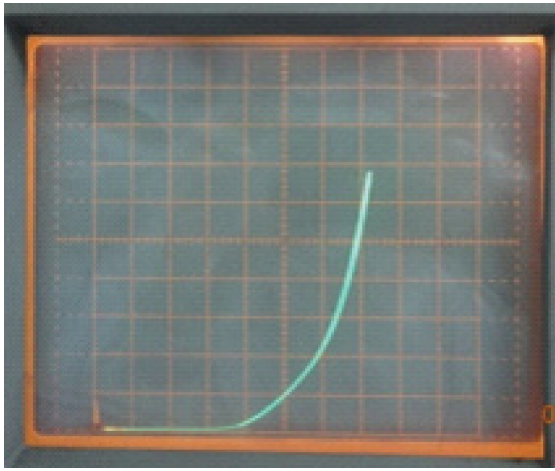


Figure 2. Forward  $I$ – $V$  characteristic of Schottky diode measured at 175 °C (500 mA/div on linear vertical axis; 100 mV/div on linear horizontal axis).

#### 4.2. Reverse characteristics

In order to reduce the electric field concentration at the border of the Schottky junction, a  $P^+$  protecting ring formed by ion implantation and a surface isolating  $\text{SiO}_2$  film covering part of the metal electrode were designed that result an increase in resistant-voltage capacity and a decrease in reverse leakage current. With the increase in reversely biased voltage, a fraction of the applied voltage is undertaken by the  $P^+$  protecting ring junction. This is equivalent to applying a voltage divider at the border of the Schottky junction<sup>[8–12]</sup> prohibiting Schottky junction breakdown because of too high electric field.

The reverse breakdown voltage is dependent on doping concentration, thickness of epitaxial layer, critical electric field and border terminal profile. It can be expressed as

$$N_D = \frac{\varepsilon_s E_C^2}{2eV_B}, \quad (5)$$

$$T_{\text{epi}} = \frac{2V_B}{E_C}. \quad (6)$$

In this experiment,  $N_D = (2.2\text{--}2.4) \times 10^5 \text{ cm}^{-3}$  is the concentration doped into the epitaxial layer,  $T_{\text{epi}} = 10.6\text{--}11.4 \text{ }\mu\text{m}$  is the thickness of the epitaxial layer,  $\varepsilon_s = 11.7$  is the relative dielectric constant of the semiconductor, and  $E_C = 3 \times 10^5 \text{ V/cm}$  is the critical electric field, so the breakdown voltage can be figured out as  $V_B = 171\text{--}121.3 \text{ V}$ . The experimentally measured reverse breakdown voltage is  $V_B = 121 \text{ V}$ . The deviation from the theoretical value comes from interface states at the Si– $\text{SiO}_2$  boundary.

If the Schottky diode is reverse biased, the depletion region between the semiconductor and NiPt silicide extends into the epitaxial layer bearing a fraction of the reverse applied voltage. The reverse leakage current can be expressed as

$$J_R \approx -J_S = A^* T^2 \exp\left(-\frac{e\Phi_B}{kT}\right). \quad (7)$$

The reverse  $I$ – $V$  characteristics measured with the TYPE576 curve tracer at 175 °C are shown in Figure 3. It can be seen from the figure that the breakdown voltage is 112 V and

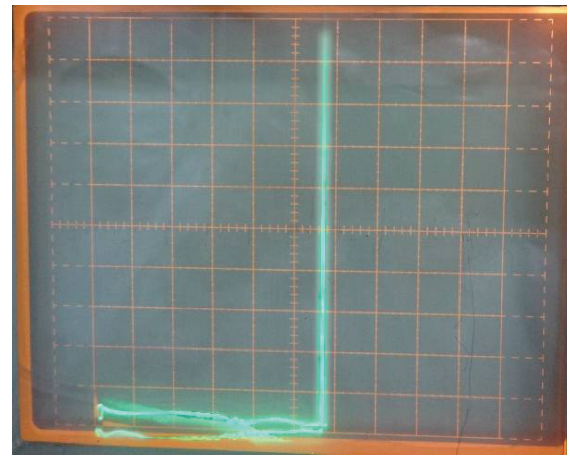


Figure 3. Reverse  $I$ – $V$  characteristics of Schottky diode measured at 175 °C (20  $\mu\text{A}$ /div on linear vertical axis; 20 V/div on linear horizontal axis).

the reverse leakage current  $I_R$  is 2  $\mu\text{A}$ . The difference from the theoretical value,  $I_R = 1.96 \times 10^{-3} \text{ }\mu\text{A}$ , may be caused by the existence of impurity contamination.

The thermal stability of the potential barrier Ni-silicide thin film has been enhanced by 100–150 °C by doping a different proportional element Pt in the fabrication process of the SBD<sup>[13–16]</sup>. The height of the potential barrier of the Schottky junction can be increased slightly by doping with Pt, with high work function.

A uniform Ni(Pt)Si film with low resistance has been successfully fabricated by NiPt60 sputtering, then metal-silicide heat treatment at 540 °C. The excellent  $I$ – $V$  characteristics and Schottky diode stability have been acquired by developing Ni(Pt)Si/Si in this work in contrast to the SBD with a traditional NiSi/Si junction. The maximum working temperature of the traditional NiSi/Si Schottky diode is 125 °C and the breakdown voltage of the SBD with the protecting ring is about 50 V<sup>[14, 15]</sup>.

The forward and reverse  $I$ – $V$  characteristics of SBDs with NiSi/Si at 125 °C and that with Ni(Pt)Si/Si film at 175 °C were simulated using a Silvaco TCAD simulator that is based on the continuity equation, Poisson's equation and physical models to calculate the carrier transport and the distribution of electric field in the device. The main physical models used in the simulation include forbidden band, mobility, generation and recombination of carriers, and collision ionization models.

The simulated forward and reverse  $I$ – $V$  characteristics of the SBD with NiSi/Si at 125 °C (dotted line) and that with Ni(Pt)Si/Si film at 175 °C (solid line) are shown in Figures 4 and 5, respectively.

It can be seen from Figure 5 that when the breakdown voltage of the 3 A/100 V Ni(Pt)Si/Si Schottky diode is 122 V, the leakage current is only  $0.5 \times 10^{-10} \text{ A}$  at 175 °C, and Schottky diode still works normally.

The breakdown voltage of the traditional NiSi/Si Schottky diode is 45 V at 125 °C, as shown in Figure 4. When the working temperature of the NiSi/Si Schottky diode is increased to 175 °C, then the electrical performance decline very quickly due to the heat concentration on the chip<sup>[16, 17]</sup>.

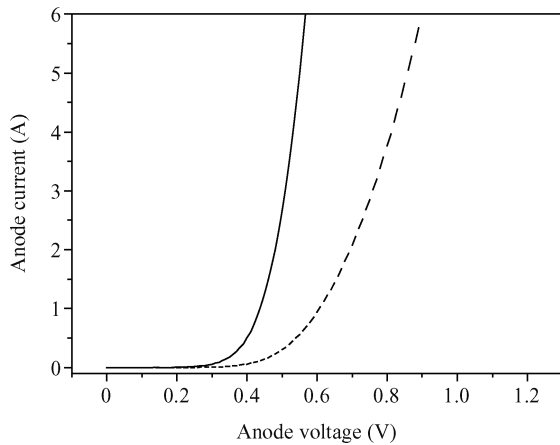


Figure 4. Forward  $I$ – $V$  characteristics of NiSi/Si Schottky diode simulated at 125 °C (dotted line) and of Ni(Pt)Si/Si Schottky diode simulated at 175 °C (solid line).

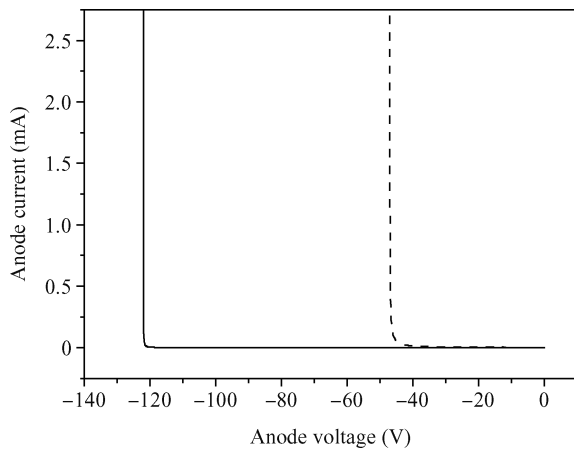


Figure 5. Reverse  $I$ – $V$  characteristics of NiSi/Si Schottky diode simulated at 125 °C (dotted line) and of Ni(Pt)Si/Si Schottky diode simulated at 175 °C (solid line).

## 5. Conclusions

The voltage-resistant capacity and the stability at high working temperature of the traditional Schottky diode have been significantly improved by doping Pt element into the traditional NiSi/Si film and designing a protecting ring. The optimum technological conditions for obtaining excellent electrical performance of the SBD have been acquired by experiments and simulation. The participation of 60% of the Pt element in the NiSi/Si film not only significantly improves the highest work temperature of the SBD but also increases the breakdown voltage. The work function of Pt and its potential barrier at the interface of the silicide are higher than those of other commonly used metals. The platinum silicide has similar electronegativity to Ag, which can eliminate the harmful positive charge at the surface. The good performance of Pt such as the steady chemical characteristics, suitable linear expansion coefficient and excellent heat and electrical conductances make it an appropriate contacting layer. The participation of the Pt element in the NiSi/Si film effectively restrains and/or

eliminates the electromigration, increasing the operational stability.

The measurement results indicate that the reverse breakdown voltage of the fabricated 3 A/100 V SBD is higher than 100 V, with a very low leakage current of 0.2  $\mu$ A and a 0.71 V forward voltage drop when  $I_F$  is 3 A. The device can still work steadily at the high temperature of 175 °C, that is 50 °C higher than the traditional SBD with NiSi/Si.

## References

- [1] Janke W, Hapka A. The current–voltage characteristics of SiC Schottky barrier diodes with the self-heating included. 16th International Workshop on IEEE Thermal Investigations of ICs and Systems (THERMINIC), 2010: 1
- [2] Adamowicz M, Gizewski S, Pietryka, et al. Evaluation of SiC JFETs and SiC Schottky diodes for wind generation systems. IEEE International Symposium on Industrial Electronics (ISIE), 2011: 269
- [3] Yang H, Heo J, Park S, et al. Graphene barristor, a triode device with a gate-controlled Schottky barrier. *Science*, 2012, 336(6085): 1140
- [4] Zhang Q C J, Duc J, Mieczkowski V, et al. 4H-SiC trench Schottky diodes for next generation products. *Material Science Forum*, 2013, 740: 781
- [5] Terry L E, Saltich J. Schottky barrier heights of nickel–platinum silicide contacts on n-type Si. *Appl Phys Lett*, 2008, 28(4): 229
- [6] Kumar V, Chen G, Guo S, et al. Field-plated 0.25- $\mu$ m gate-length AlGaIn/GaN HEMTs with varying field-plate length. *IEEE Trans Electron Devices*, 2006, 53(6): 1477
- [7] Deng X, Zhang B, Li Z, et al. Numerical analysis on the 4H-SiC MESFETs with a source field plate. *Semicond Sci Technol*, 2007, 22(7): 701
- [8] He J, Chan M, Zhang X, et al. A new analytic method to design multiple floating field limiting rings of power devices. *Solid-State Electron*, 2006, 50(7): 1375
- [9] De Souza M M, Bose J V S C, Narayanan E M S, et al. A novel area efficient floating field limiting ring edge termination technique. *Solid-State Electron*, 2000, 44(8): 1381
- [10] Bhardwaj A, Ranjan K, Chatterji S, et al. A new approach to the optimal design of multiple field-limiting ring structures. *Semicond Sci Technol*, 2001, 16(10): 849
- [11] Bae D G, Chung S K. An analytic model of planar junctions with multiple floating field limiting rings. *Solid-State Electron*, 1998, 42(3): 349
- [12] Adler M S, Temple V A K, Ferro A P, et al. Theory and breakdown voltage for planar devices with a single field limiting ring. *IEEE Trans Electron Devices*, 1977, ED-24: 107
- [13] Zhang Z, Zhang S L, Yang B, et al. Morphological stability and specific resistivity of sub-10 nm silicide films of Ni<sub>1-x</sub>Pt<sub>x</sub> on Si substrate. *Appl Phys Lett*, 2010, 96(7): 071915
- [14] Finstad T G, Nicolet M A. Silicide formation with bilayers of Pd–Pt, Pd–Ni, and Pt–Ni. *J Appl Phys*, 2008, 50(1): 303
- [15] Hoummada K, Perrin-Pellegrino C, Mangelinck D. Effect of Pt addition on Ni silicide formation at low temperature: growth, redistribution, and solubility. *J Appl Phys*, 2009, 106(6): 063511
- [16] Cojocaru-Mirédin O, Cadel E, Blavette D, et al. Atomic-scale redistribution of Pt during reactive diffusion in Ni (5% Pt)–Si contacts. *Ultramicroscopy*, 2009, 109(7): 797
- [17] Imaizumi M, Kuroda K, Matsuno Y, et al. Semiconductor device having a groove and a junction termination extension layer surrounding a guard ring layer. US Patent, No. 8304901, 2012-11-6