CURRENT–VOLTAGE, CAPACITANCE–VOLTAGE, AND CAPACITANCE–TEMPERATURE MEASUREMENTS ON $CdS/CuInSe_2$ SOLAR CELLS

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Summary

This paper reports on current–voltage, capacitance–voltage, and capacitance–temperature measurements on 9% efficient $CdS/CuInSe_2$ solar cells. Previous deep level transient spectroscopy (DLTS) measurements on the same samples have shown two traps in the $CuInSe_2$, namely a majority carrier (hole) trap whose activation energy is distributed over the range 0.65 - 0.75 eV from the valence band edge and a minority carrier (electron) trap with a sharply defined activation energy of 0.35 eV from the conduction band edge. (N. Christoforou, J. D. Leslie and S. Damaskinos, *Sol. Cells*, *26* (3) (1989) 197.) There is strong evidence from the measurements reported here that there are additional hole traps (deep acceptor states) in the $CuInSe_2$ close to the interface with the CdS, which do not participate in the DLTS measurements. Other possible interpretations in terms of a heavily doped p layer in the $CuInSe_2$ close to the CdS interface or shallow, fast-acting traps are shown not to agree with all the experimental results.

1. Introduction

In a recent paper in this journal [1], the authors have reported deep level transient spectroscopy (DLTS) measurements on 9% efficient $CdS/CuInSe_2$ solar cells. The results indicated the presence in the p-type $CuInSe_2$ films with a carrier concentration of 1×10^{15} cm^{-3} of a hole trap of concentration 5×10^{14} cm^{-3}, which is distributed in energy from 0.65 to 0.75 eV from the valence band edge, and an electron trap concentration of

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5×10^{13} cm^{-3}, which is located at 0.35 eV from the conduction band edge. While simulation studies, reported in the earlier publication [1], supported the above trap characteristics, there was the unresolved difficulty that the capacitance transient simulations needed a smaller trap concentration by a factor of 10 than that required by the capacitance *vs.* temperature simulations. In this paper, we will present evidence that this discrepancy is due to the presence of additional hole traps (deep acceptor states) with a concentration of 5×10^{15} cm^{-3} in the $CuInSe_2$ close to the interface with the CdS, which do not participate in the DLTS measurements but do affect the overall capacitance of the solar cells.

2. Experimental details

Details on the CdS/$CuInSe_2$ solar cells studied in this work were given in the previous paper [1].

Current–voltage (I–V), capacitance–voltage (C–V), and capacitance–temperature (C–T) measurements over the temperature range 100 - 350 K were carried out on the same CdS/$CuInSe_2$ solar cells used in the DLTS measurements [1]. The semi-automated system for making these I–V, C–V, C–T and DLTS measurements has been described briefly in an earlier publication [2] containing some of our preliminary results, and a more complete description is available elsewhere [3], so only the briefest description of the I–V, C–V and C–T measurements will be given here.

Current *vs.* voltage characteristics were measured in the dark using a Keithley 195A multimeter as the current meter. The resulting I–V data were fitted to obtain series and shunt resistances. The I–V data could be replotted, removing the effects of the series and parallel resistances, so that the intrinsic properties of the diode were more evident.

Capacitance *vs.* voltage characteristics were measured using a Boonton capacitance meter, model 72B-05A, which measures the capacitance at a frequency of 1 MHz. The associated software allows the C–V data to be replotted as $1/C^2$ *vs.* V plots and the ionized charge concentration in the depletion region to be calculated either as a function of bias voltage or of depth into the depletion layer. Corrections for series and shunt resistance can be applied to all plots and calculations [4].

Capacitance *vs.* temperature data are normally taken as part of a DLTS run. However, C–T measurements were also made, where the voltage was set at a fixed reverse bias value and the temperature was incremented from the starting to the final temperature while the capacitance was measured.

3. Results

Each CdS/$CuInSe_2$ sample had either 12 diodes of area 7.7 mm^2 or one large diode and four diodes of area 7.7 mm^2. Six samples were studied and

several diodes on each sample were studied in detail. The results to be presented were found in all samples studied.

Figure 1 shows a typical plot of capacitance *vs.* temperature at a constant reverse bias of −1.0 V in the dark. As can be seen, the capacitance initially shows a slow change with temperature and then a faster change with temperature. The change in capacitance is substantial, in this case almost tripling the capacitance over the temperature range 100 - 300 K.

Figure 2 shows a typical plot of $1/C^2$ *vs.* V in the dark over the temperature range 225 - 320 K. The voltage on the CdS/$CuInSe_2$ diode is varied from 0.4 V forward-biased to 1.9 V reverse-biased. The large increase in capacitance with temperature seen in Fig. 1 causes the overall value of $1/C^2$ to decrease with temperature, as can be seen in Fig. 2. The $1/C^2$ *vs.* voltage plot is not linear, as one would expect for a constant ionized impurity concentration with depth in the depletion layer, but instead has a slope that decreases with increasing reverse bias.

In an earlier publication [2] we presented a number of arguments to show that the depletion layer is almost totally within the lower carrier concentration $CuInSe_2$. Thus it is possible to use a one-sided junction approximation to obtain an estimate of how the doping density is varying within the depletion layer. This is done by calculating $N(x)$ from

$$N(x) = \frac{2}{q\epsilon_s A^2 \, \mathrm{d}(1/C^2)/\mathrm{dV}} \text{ and } x = \frac{\epsilon_s}{C(V)} \tag{1}$$

where $N(x)$ is the ionized charge concentration at position x in the depletion layer measured from the interface, q is the electron charge, ϵ_s is the semiconductor permittivity, A is the junction area, $C(V)$ is the sample capacitance at reverse bias V, and $\mathrm{d}(1/C^2)/\mathrm{dV}$ is computed at each voltage at which x is computed.

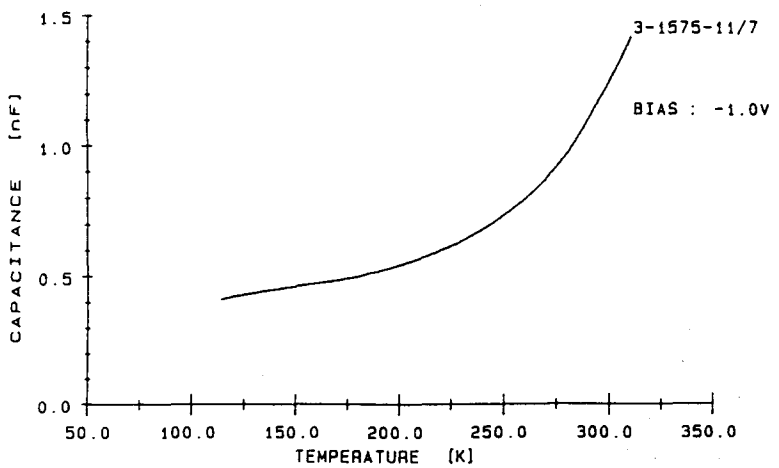

Fig. 1. Temperature dependence of the diode capacitance for sample 3-1575-11/7 at a fixed reverse bias of 1.0 V.

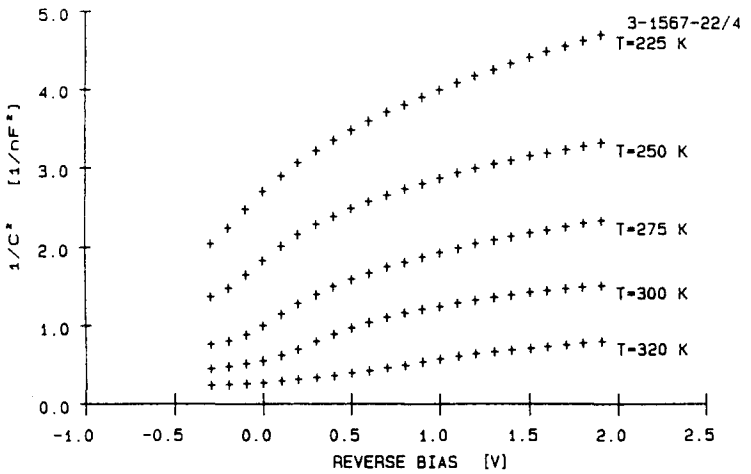

Fig. 2. Temperature dependence of $1/C^2$ *vs.* V characteristics for sample 3-1567-22/4.

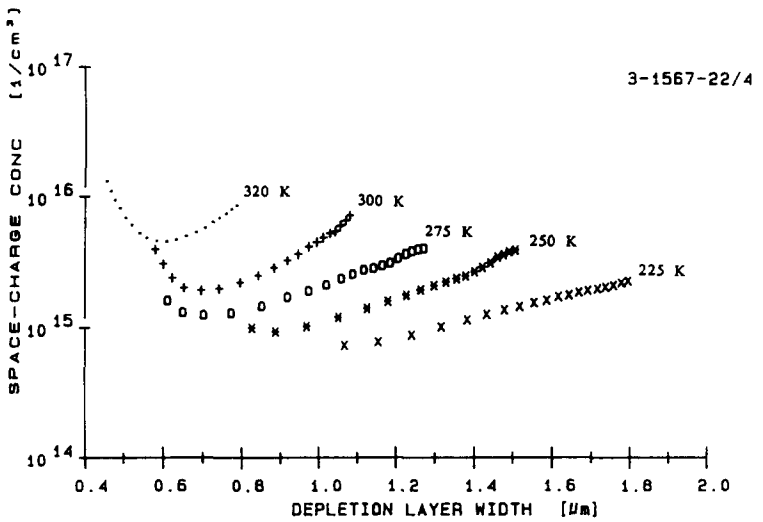

Fig. 3. Temperature dependence of the space charge concentration *vs.* depletion layer width for sample 3-1567-22/4 after the capacitance correction for series resistance.

Figure 3 shows the resulting plot of ionized charge concentration in carriers per cubic centimetre *vs.* depth in micrometres for the data and the same four temperatures as shown in Fig. 2. The dielectric constant assumed for the $CuInSe_2$ layer is 13.6 [5]. It should be noted that before the analysis of eqn. 1 is applied to the $1/C^2$ data of Fig. 2, a correction [4] for the effect of series resistance on the measured capacitance is applied to obtain the true capacitance. This correction lowers the value of the depletion depth by about 10% but does not affect the value of the space charge concentration

significantly. It can be seen from Fig. 3 that, as the temperature is increased, the depletion width becomes smaller and the carrier concentration increases.

Figure 4 shows the $1/C^2$ *vs.* V characteristic of a CdS/$CuInSe_2$ sample in the dark and when illuminated with monochromatic light of wavelengths 1.4 μm, 1.3 μm, and 1.1 μm. It should be noted that the 1.1 μm wavelength corresponds to a photon energy just above the band gap energy of $CuInSe_2$, whereas the other two wavelengths correspond to sub-band-gap radiation.

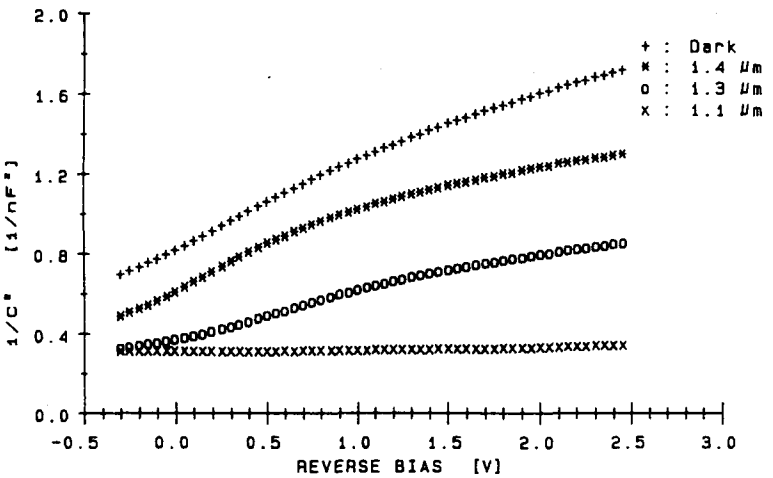

Fig. 4. Dark capacitance and photocapacitance of sample 3-1575-11/3 at $T = 170$ K for different incident wavelengths.

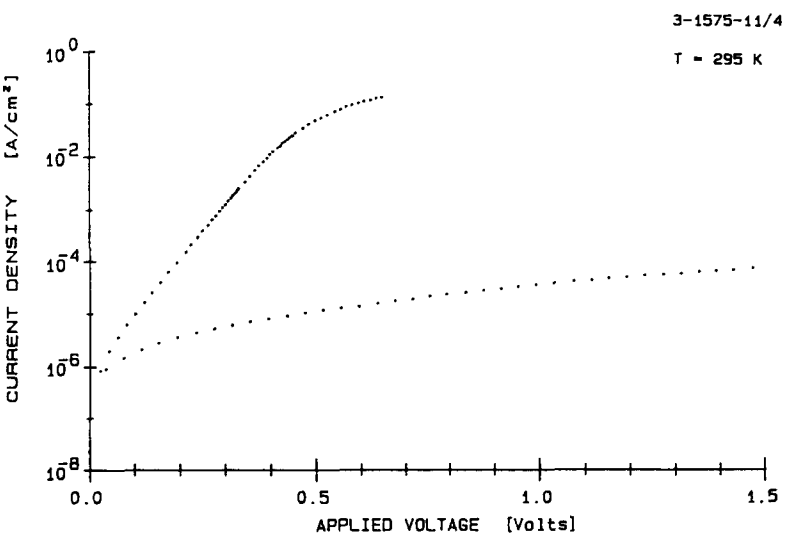

Fig. 5. Log J *vs.* V for sample 3-1575-11/4 at 295 K, where J is the current density. The bottom curve indicates the reverse bias current and the top curve shows the forward bias current.

Figure 5 shows the forward and reverse $I-V$ characteristics in the dark at room temperature for a typical $CdS/CuInSe_2$ cell. The rectification ratio, *i.e.* $I(+V)/|I(-V)|$, is about 100 at $|V| = 0.4$ V. The bending over of the forward $I-V$ characteristic is due to series resistance. Figure 6 shows the forward bias log J *vs.* V in the dark for a typical $CdS/CuInSe_2$ cell at a range of temperatures from 200 to 330 K. The flattening of the forward characteristic due to series resistance, particularly at the lower temperatures, can be clearly seen. At the lowest temperatures, deviations of the exponential increase in current with voltage at the low voltage end may be due to the presence of a second diode possibly at the $CuInSe_2$–Mo interface, which has a small barrier height and only shows up at low temperature.

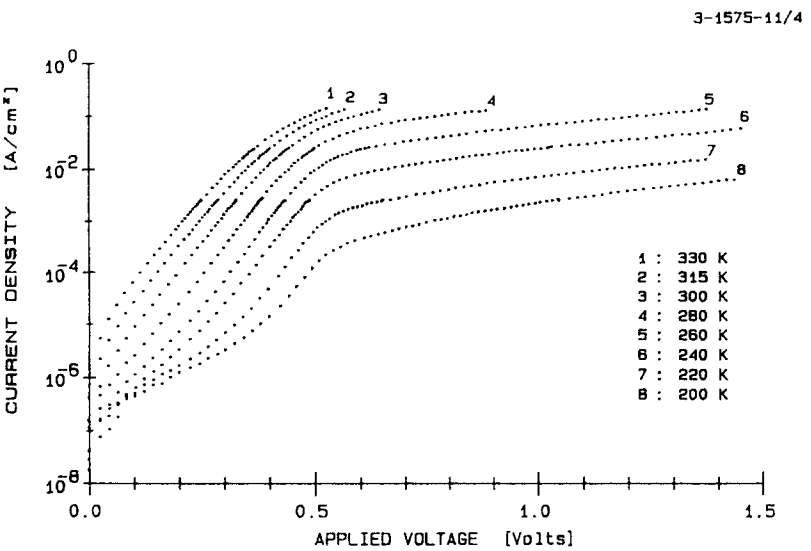

Fig. 6. Forward bias log J *vs.* V for sample 3-1475-11/4 at different temperatures.

4. Analysis and discussion

In our earlier paper [1], we argued that the origin of the discrepancy between the magnitude of the DLTS transients and the magnitude of the change in capacitance with temperature was the presence of some deep traps that could not participate in the DLTS measurements. The equilibrium occupancy of a trap depends only on trap activation energy and temperature and not on the initial conditions. Thus, if we have hole traps in the depletion layer that cannot be refilled by the filling pulse, their occupancy would still be governed by the temperature and their activation energy, and they will contribute to an increase in capacitance as they empty as the temperature increases.

Such traps (deep acceptor states), that do not participate in the capacitance transient, would have to be located in the $CuInSe_2$ just close to the interface between the CdS and the $CuInSe_2$ because the filling pulse would not be able to shrink the depletion layer sufficiently to sweep this region into the neutral semiconductor during a fill pulse, causing the traps to be refilled with holes. There would also have to be a large concentration of such traps, to effect a factor of 10 between the capacitance transient amplitude that would result if all the traps in the depletion layer were contributing and that which is measured experimentally.

We would like to show how the $C-V$, $C-T$ and $I-V$ measurements reported here support this explanation of the discrepancy in terms of the presence of a high trap concentration in the $CuInSe_2$ layer near the interface with the CdS layer.

Firstly, the spatial profile of the space–charge concentration of Fig. 3 shows that when the temperature is increased, the space–charge concentration is increased in the measurable part of the depletion layer adjacent to this interfacial region. This space–charge concentration increases as the temperature is increased, which is just the behaviour we would expect of hole traps in the upper part of the band gap that were emptying (*i.e.* acquiring a negative charge) as the temperature is increased.

Secondly, the photocapacitance measurements of Fig. 4 lend further support to the presence of a high trap concentration in the $CuInSe_2$ near the interface with the CdS. It should be noted that the measurements of Fig. 4 were made at a temperature at which we would expect that all the hole traps are filled. We see that the $1/C^2$ *vs.* V plot in the dark is very similar to what we have observed for other samples. Illumination of the CdS/$CuInSe_2$ junction by the 1.4 μm radiation causes the capacitance to increase. We associate this capacitance increase with electrons being excited from the valence band to fill some traps (*i.e.* the emptying of hole traps), with a consequent increase in negatively ionized charge and decrease in depletion width. It should be noted that the effect increases with the energy of the light, as a larger fraction of the traps in the band gap can be affected. The $1/C^2$ *vs.* V plot shows a flatter region for small positive voltages as sub-band-gap light is applied. This is particularly noticeable for the 1.3 μm plot in Fig. 4. We take this lower slope as another indication of a higher ionized charge concentration in this region near the interface.

However, the fact that for sub-band-gap light, the capacitance can still be varied with voltage indicates that sub-band gap light can only produce extra ionized charge that is comparable with the ionized charge in the bulk. With above-band-gap light, the capacitance does not change with voltage. We interpret this as follows. With above-band-gap light electron–hole pairs are created throughout the depletion layer. The electrons will tend to be driven towards the interface and the holes will be driven towards the bulk. If there are hole traps (deep acceptor states) near the interface, the electrons can be trapped by states containing holes which is equivalent to emptying a hole trap. If there is a large concentration of such hole traps close to the

interface, the depletion layer will reach its minimum value and the capacitance will reach its maximum value. The large ionized charge density associated with these empty hole traps (ionized acceptor states) close to the interface will make it almost impossible for the capacitance to change with voltage. Any increase in positive charge on the n side of the junction can be matched by negative charge on the p side of the junction by just an infinitesimal increase in the width of the depletion layer.

I–V data on these samples in the dark also indirectly support the idea of a large concentration of traps in the $CuInSe_2$ near the CdS–$CuInSe_2$ interface. I–V data such as those shown in Fig. 5 were fitted to the model of Miller and Olsen [6] using eqn. 2.

$$I = \frac{V - IR_s}{R_{sh}} + I_0\{\exp C(V - IR_s) - 1\} \tag{2}$$

where R_s is the series resistance, R_{sh} is the shunt resistance, and I_0 is the reverse saturation current, given by the product of the junction area A_J and the reverse saturation current density J_0. R_{sh} is estimated from the low-voltage reverse current, while R_s is estimated from the high forward-voltage portion of the I–V characteristic. During the fitting process, the values of R_s and R_{sh} are re-adjusted in turn several times, so that the best fit possible is achieved.

The reverse saturation current density is given by

$$J_0 = J_{00} \exp(-\phi/kT) \tag{3}$$

where ϕ is the apparent barrier height.

According to the model of Miller and Olsen, the factor C can be written as

$$C = (1 - f)B + f/(AkT) \tag{4}$$

where B is a temperature independent tunneling parameter, the value of f quantifies the degree of tunneling character of the current transport, with $f = 1$ being simple interface recombination and $f = 0$ being simple tunneling, and A is the usual diode factor.

Values of R_s, R_{sh}, C and J_0 were obtained as a function of T from fitting I–V data at different temperatures. From plots of C *vs.* $1/T$, the parameters $(1 - f)$B and f/A can be estimated. From plots of $\log(J_0)$ *vs.* $1/T$, the apparent barrier height ϕ can be found. Table 1 shows the results of this analysis, which are similar to those obtained by Miller and Olsen [6]. It is interesting to note that Miller and Olsen did their measurements on Boeing CdS/$CuInSe_2$ solar cells which were fabricated in a significantly different way from the CdS/$CuInSe_2$ solar cells used in this study, which were produced by the Institute of Energy Conversion. This indicates that these two types of cells have the same transport mechanisms in the dark.

We observe that there is an appreciable tunneling contribution to the charge transport. In addition, the apparent barrier height, being mostly between 0.55 and 0.60 eV, is slightly more than half the band gap of the

TABLE 1

Fitting parameters from the current–voltage analysis according to the model of Miller and Olsen [6]

Sample	ϕ (eV)	$B(1-f)$ (V^{-1})	J_{00} (A cm^{-2})	f/A (e)
3-1575-11/4	0.56	11.5	1.8×10^3	0.35
3-1575-11/7 A	0.61	10.7	9.6×10^3	0.37
3-1575-11/7 B	0.49	15.8	2.2×10^2	0.20
3-1575-11/9 A	0.56	11.2	1.9×10^3	0.36
3-1575-11/9 B	0.65	8.3	4.6×10^4	0.45
3-1567-22/3	0.59	11.9	4.7×10^4	0.23
3-1567-22/4	0.67	12.0	4.0×10^4	0.25
3-1706-21/4	0.55	13.8	2.0×10^3	0.26
3-1749-11/3[a]	0.65	−5.0	2.0×10^4	0.65
3-1749-32/5	0.30	18.6	4.0×10^{-1}	0.02

[a]This sample is $CdZnS/CuInSe_2$.
B denotes that the same sample was measured again 5 months after measurements A, and after these samples underwent the annealing process again.

selenide. We also note that there is a relation between ϕ and f/A. As expected, in nearly all cases the larger the value of f/A is (less tunneling), the greater the apparent barrier height. On the other hand, in the case of small f/A, *i.e.* strong tunneling, the apparent barrier height is slightly less than half the band gap. The fact that even in the case of strong tunneling, the apparent barrier height is still large for a simple tunneling process, indicates that this tunneling must occur part way up the potential barrier, as suggested by Miller and Olsen [6].

The model of Miller and Olsen assumes that the depletion layer consists of two parts. Close to the interface, the space–charge density is higher than in the part away from the interface. This high space–charge density is narrow,and it is here that the tunneling occurs. As mentioned earlier, this agreement with the model of Miller and Olsen lends support to the presence of states in the $CuInSe_2$ near the $CdS–CuInSe_2$ interface that contribute to the junction capacitance but do not participate in the DLTS measurement.

Let us now consider two alternative interpretations of the results, namely a highly doped p layer in the $CuInSe_2$ close to the interface with the CdS or the presence of a uniform distribution of shallow, faster-acting traps (acceptor states), in order to show that neither of these alternative explanations can fit all the experimental results.

Let us suppose the $CuInSe_2$ layer actually consisted of two layers, a highly doped p layer close to the interface with the CdS and a more lowly doped p layer for the rest of the $CuInSe_2$ layer. Such a combined layer would have a decreased overall depletion layer width and hence would produce a higher diode capacitance. Such an arrangement could explain the experimentally observed result that the measured diode capacitance is much

larger than the capacitance change associated with the DLTS spectrum. However, such a highly doped p layer cannot explain the temperature dependence of the capacitance results or the photocapacitance results. A highly doped p layer must have a large concentration of shallow acceptor states which will already be ionized at low temperature to give the negative ionized charge that produces the smaller depletion layer and larger capacitance. As the temperature is increased nothing further will happen, so the substantial increase in capacitance with temperature cannot be explained. Also, because all these shallow acceptor states are already ionized (*i.e.* contain an electron), the flood of electrons towards the interface with the CdS produced by above-band-gap radiation cannot be trapped and hence there should be no photocapacitance effect in contrast to the experimental result. Finally, another strong argument against the existence of a highly doped p layer in the $CuInSe_2$ layer close to the interface with the CdS is the fact that such a layer has never been seen in all the experiments that have been done on this type of $CdS/CuInSe_2$ solar cells.

Another way to try to explain away the discrepancy between the large capacitance of the diode but the small capacitance change associated with the DLTS results is to postulate the existence of fast-acting states uniformly distributed throughout the $CuInSe_2$ layer. The argument is that it is not a question of the fill pulse being unable to affect these states, but that the states are so fast that the DLTS measurement does not see them as they respond to the changes in their occupancy induced by the fill pulse. However, the problem with this explanation is that it once again cannot explain the temperature dependence of the capacitance results or the photocapacitance results. To generate the large diode capacitance these fast-acting states must be shallow acceptor states that are already ionized at low temperature. In order for these states not to be seen in the DLTS experiment, they must be very shallow indeed, *e.g.* with activation energies less than 0.1 eV. Just as in the previous case discussed, such shallow acceptor states would already be almost fully ionized at low temperature and thus could not produce the temperature dependence of the capacitance results that is observed. It is particularly important to note that the capacitance results show that the capacitance changes very slowly at low temperature and then more quickly at higher temperature. Such behaviour cannot be explained by a shallow acceptor state that is almost fully ionized already at low temperature and whose occupancy is just changing slightly as the result of the temperature being increased. The argument why such shallow ionized acceptor states would not show the experimentally observed photocapacitance effect has already been presented for the first alternative explanation considered.

5. Conclusions

Based on our $I-V$, $C-V$ and $C-T$ measurements reported here and the DLTS measurements and associated simulations reported earlier [1], we have

concluded that in addition to the two traps detected by the DLTS measurements there is a high hole trap (deep acceptor state) concentration in the $CuInSe_2$, with a value about four to five times greater than the shallow doping level concentration of 1×10^{15} cm^{-3}, that exists close to the interface between the $CuInSe_2$ and the CdS. Evidence for these states close to the interface come from several different observations.

(1) The ionized concentration profile calculated from the $C-V$ measurements shows the onset of a rapid increase as the interface is approached for high T and small positive bias.

(2) The fact that the DLTS signal is small compared with the signal expected from a high trap concentration uniformly distributed can be explained only if the majority of traps are close to the interface where they could not be filled by the fill pulse and consequently would not participate in the DLTS process.

(3) From the $I-V$ measurements, we found that in addition to interface recombination, a significant tunneling process occurs as well. For tunneling to take place there must be a very narrow portion of the depletion region with a high space charge and consequently with a rapid variation in band bending to create a narrow tunneling barrier.

(4) Photocapacitance measurements also support the existence of a high trap concentration close to the interface, particularly the fact that with above-band-gap light the capacitance does not vary with voltage. This indicates that the electrons of the electron–hole pairs created are filling all these traps close to the interface (*i.e.* emptying of hole traps) and that there are so many of these traps that the ionized charge density is so high that the depletion layer can barely increase at all as the voltage is increased.

Since the traps close to the interface do not participate in the DLTS measurements, we therefore cannot measure their activation energy. However, they have to be hole traps in the upper half of the energy gap to agree with the behaviour of the $C-T$ measurement in which they participate.

Acknowledgments

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