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A simple method for pinhole detection in carrier selective POLO-junctions for high efficiency silicon solar cells

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ABSTRACT

Polycrystalline silicon (poly-Si) layers on thin silicon oxide films have received strong research interest as they form excellent carrier selective junctions on crystalline silicon substrates after appropriate thermal processing. Recently, we presented a new method to determine the pinhole density in interfacial oxide films of poly-Si on oxide (POLO)-junctions with excellent electrical properties. The concept of magnification of nanometer-size pinholes in the interfacial oxide by selective etching of the underlying crystalline silicon is used to investigate the influence of annealing temperature on pinhole densities. Eventually, the pinholes are detected by optical microscopy and scanning electron microscopy. We present results on the pinhole density in POLO-junctions with J_0 values as low as 1.4 fA/cm^2. The stability of this method is demonstrated by proving that no new holes are introduced to the oxide during the etching procedure for a wide range of etching times. Finally, we show the applicability to multiple oxide types and thickness values, differently doped poly-Si layers as well as several types of wafer surface morphologies. For wet chemically grown oxides, we verified the existence of pinholes with an areal density of 2×10^7 cm^{-2} even already after annealing at a temperature of 750 °C (lower than the optimum annealing temperature for these junctions).

1. Introduction

Polycrystalline silicon-rich layers on thin silicon oxide films have recently received strong research interest as they form excellent carrier selective junctions on crystalline silicon substrates after appropriate thermal processing. The excellent passivation properties combined with a low specific contact resistance [1–3] have translated into solar cell efficiencies of 25.3% using the tunnel oxide passivated contact (TOPCon)-approach for one carrier polarity [4] and 25.0% with poly-Si on oxide (POLO)-junctions for both carrier polarities [5].

Since their first application to silicon bipolar junction transistors the carrier selective current transport across the POLO-junctions has been widely investigated [6,7]. An explanation based on localized carrier transport through pinholes in the interfacial oxide has been proposed [8,9] complementary to direct tunnelling for very thin oxide thickness. The break-up of the interfacial oxide film under annealing has been identified as a crucial process step in the formation of high quality junctions [10–12]. Recently, small regions showing direct contact between the crystalline silicon and the poly-Si layer were found in transmission electron microscopy (TEM) investigations of POLO-junctions with excellent passivation properties [13]. From the TEM results a diameter of 5 nm was obtained for these regions and their density was estimated to be about 1×10^8 cm^{-2}. Both values are in agreement with the proposed pinhole model [8,9].

While TEM is the best choice to determine the diameter of pinholes in the 5 nm range, it only allows a rough estimation of their density for values below 10^9 cm^{-2}. Plus, it is hard to find pinholes at all [13]. Thus, a complementary method to determine the pinhole density is required. A step in this direction was undertaken using conductive atomic force microscopy (C-AFM) [14]. However, this method is limited by the lateral conductivity of the poly-Si films, which has to be small in order to enable the required resolution. Recently we developed a new concept, which circumvents the constraints of TEM and C-AFM by combining selective etching with tetramethylammonium hydroxide (TMAH) and simple optical microscopy (OM) [15]. After a proof of concept experiment using lithographically patterned samples [15] this

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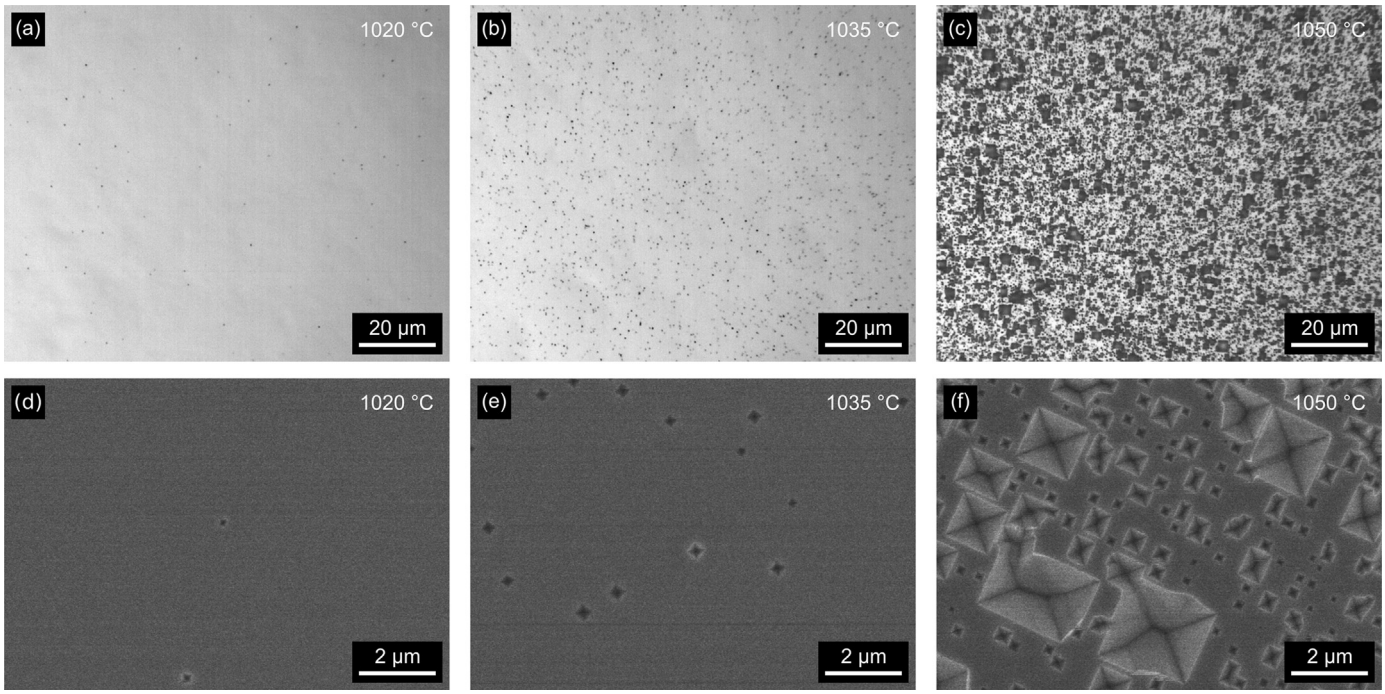

Fig. 1. OM ((a)-(c)) and SEM ((d)-(f)) images after etching of wafers annealed at 1020 °C ((a), (d)), 1035 °C ((b), (e)), and 1050 °C ((c), (f)), respectively. Etch pits are clearly visible with both methods. SEM reveals typical inverted pyramid structure.

method was recently applied to POLO-junctions correlating the pinhole density in interfacial oxide films with their excellent saturation current density and contact resistivity [16].

In this paper, we investigate the influence of annealing temperature on the pinhole density in POLO-junctions with J_0 values as low as 1.4 fA/cm^2. We study extensively the stability of the undercutting procedure to ensure that no additionally holes are generated during the etching process. Finally, we apply this method to several different substrates, oxide types and thickness values as well as differently doped poly-Si layers to demonstrate the versatility of this method.

2. Experimental

POLO-junctions were prepared on planar, shiny-etched 90 Ωcm *p*-type 290 µm-thick FZ wafers. A ~2.1 nm silicon oxide film (thickness determined by ellipsometry) was grown by dry thermal oxidation. Then a 120 nm-thick *n*-type poly-Si layer was produced by LPCVD and subsequent phosphorus ion implantation. After junction formation for 60 min in N_2 ambient at different temperatures (1020 °C, 1035 °C, and 1050 °C) J_0 values were extracted from photoconductance decay measurements.

To identify pinholes in the oxide by OM, the poly-Si layer has to be completely removed while the oxide should remain as is. This was achieved by removal of the native oxide formed on the poly-Si layer using hydrofluoric acid (HF) solution and subsequent selective etching in 15% TMAH solution at 80 °C. Overetching leads to an undercut of the oxide. The resulting etch pits in the underlying silicon are much larger than the original pinholes. So, they can readily be detected. To verify the stability of the etching process, each wafer was split into several pieces and etched for different times (120 – 360 s). Pinhole densities were counted from OM images and correlated to scanning electron microscopy (SEM) images.

3. Results and discussion

3.1. Influence of annealing temperature

The saturation current densities for the samples annealed at 1020 °C and 1035 °C are 1.4 fA/cm^2 and 1.5 fA/cm^2, respectively. A further increase of annealing temperature to 1050 °C leads to a much higher J_0 value of 55 fA/cm^2. This dramatic change is accompanied by the increase of pinhole density within the oxide. Massive dopant diffusion from the poly-Si layer into the crystalline silicon could also increase the saturation current due to related Auger recombination. However, previous reports show that the fraction of Auger recombination remains small compared to recombination at the crystalline Si/SiO_2 interface [1,17].

After etching 1.5 × 1.5 cm^2 small pieces of the samples in 15% TMAH solution at 80 °C for 240 s, the dependence of pinhole density on annealing temperature can directly be seen in the OM images in Fig. 1(a)-(c). The average areal etch pit density (EPD) increases from (a) 5.9×10^5 cm^{-2} at 1020 °C to (b) 1.3×10^7 cm^{-2} at 1035 °C while J_0 remains constant. In the framework of the model in Ref. [9], both samples possibly represent a regime, in which the pinhole area fraction is that low that the total surface recombination is dominated by the recombination in the regions with still intact interface oxide. The average EPD after annealing at (c) 1050 °C of 1.1×10^8 cm^{-2} is accompanied by a significant increase in J_0. The reader should note that these J_0 values are determined by a QSSPC measurement in the center of the wafer, which corresponds to an average over several cm^2. Local inhomogeneities on a smaller length scale are not resolved in this measurement.

In Fig. 1(d)-(f) corresponding SEM images are shown, revealing the typical inverted pyramid structure resulting from anisotropic etching of (111) and (001) planes by TMAH. For the wafer annealed at 1020 °C single etch pits with 150 nm up to 170 nm edge lengths are found. The maximum structure size increases with temperature to 480 nm after annealing at 1035 °C and up to 2.5 µm after annealing at 1050 °C (only counting not overlapping etch pits). The latter two samples also show smaller etch pits. The percentage of structures with sizes below 125 nm increases from 0% (1020 °C) to 12.6% (1035 °C) up to 23.5% (1050 °C). This indicates the augmented formation of new holes within the oxide with increasing temperature. At the same time, holes grow larger at higher temperatures. As reported before [16], the EPD observed by SEM is slightly higher in comparison to values obtained from OM. This is due to the resolution limit of optical microscopes. Nevertheless, the SEM

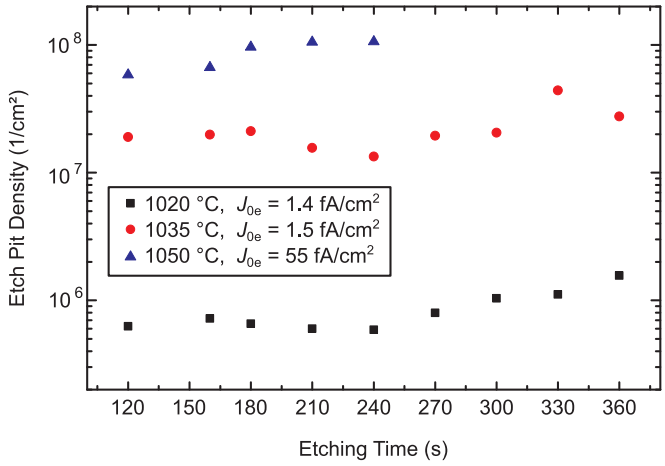

Fig. 2. EPDs for different etching times determined by OM. The resulting pinhole density is unaffected by the etching process, while the impact of annealing temperature is clearly visible.

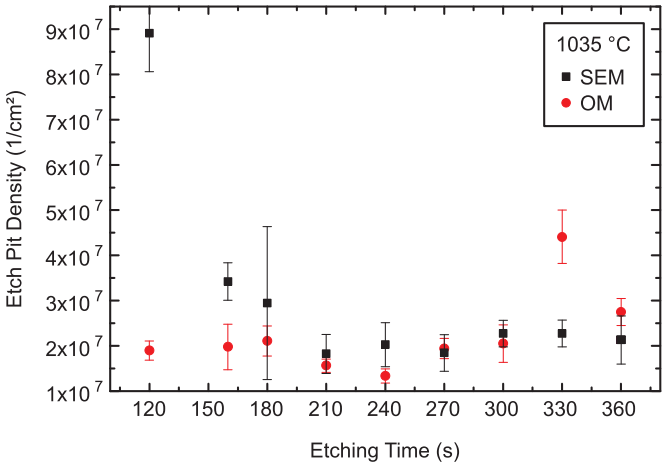

Fig. 3. EPDs for different TMAH etching times determined by SEM and OM. Short etching times lead to significant differences in EPD values obtained by SEM and OM, as the values of the OM are underestimated due to the resolution limit of optical microscopes. This effect disappears with increasing etching time and corresponding increase in etch pit size.

results confirm that the dark contrasts in OM images originate from etch pits and thus can be used to determine the pinhole density within the oxide. In this case, a pinhole density of $1.1\times10^{8}\,cm^{-2}$ already leads to etch pit coalescence for the etching time of 240 s. Higher densities will therefore lead to an increased error range.

As the size of the etch pits and therefore the detectability naturally relies on the etching time, we vary the latter from 120 to 360 s to ensure that all existing pinholes are sufficiently magnified. Fig. 2 shows the OM-counted EPDs with respect to etching time. For the wafer annealed at 1020 °C the EPDs vary only slightly from 5.9×10^{5} – $8.0\times10^{5}\,cm^{-2}$ for times up to 240 s. For longer times, the EPD seems to increase up to $1.6\times10^{6}\,cm^{-2}$ after 360 s. A similar behavior is found for the wafer annealed at 1035 °C. Only slight EPD variations of 1.3×10^{7} – $2.1\times10^{7}\,cm^{-2}$ have been observed for etching times up to 300 s. Notably, the highest EPD of $4.4\times10^{7}\,cm^{-2}$ was not found for the longest etching time.

The highest EPD of $1.1\times10^{8}\,cm^{-2}$ is found after annealing at 1050 °C. However, for short etching times, the EPD is lower. This could be due to the existence of very small etch pits shown in Fig. 1(f) that are only visible in OM after massive undercutting. The small etch pits could result from smaller pinholes generated in the oxide during annealing, for which the etching process would not only be limited by the global etch rate but also by transport of the reactants and reaction products [16]. No EPD could be determined for etching times above 240 s due to the coalescence of etch pits. As for all samples a slight increase of EPD can be found with increasing etching time, we have to ensure that no additional holes are generated due to the etching procedure.

3.2. Stability of the method

In the following we will analyze the stability of the method using the sample annealed at 1035 °C, as the EPD is high, leading to very good statistical results, while no additional uncertainties are introduced by etch pit coalescence. Additionally, the sample is probably close to the edge of the already mentioned regime where the total surface recombination is dominated by the recombination in regions with still intact interface oxide. An increase in pinhole density should therefore lead to an increase of J_0. In Fig. 3 the EPDs determined by OM and SEM are shown for different etching times. Short etching times lead to significant differences in EPD values. After etching with TMAH for 120 s, the EPD determined by SEM is almost 5 times higher than for OM. This is due to the underestimation of EPD by OM caused by the resolution limit of optical microscopes. The differences in EPD disappear with increasing etching time as the existing etch pits grow larger and become detectable by OM. The impression of increasing EPD with increasing etching times cannot be confirmed by SEM. On the contrary, the EPD is almost constant from 210 s to 360 s. Thus, no additional pinholes are introduced by the etching process. This is supported by the fact that if new pinholes would be generated within the oxide due to the etching procedure, this should again lead to a higher EPD obtained by SEM compared to OM, which is not observed.

The question remains, why the highest EPDs are obtained at the lowest etching times. As we did not etch the same area on the sample for different times but used different pieces from the same wafer, this could indicate, that EPD-variations are not due to the etching process itself but caused by an inhomogeneous pinhole distribution on the wafer. As pinhole densities are linked to J_0 values, such inhomogeneities should be revealed by infrared lifetime mappings (ILM). Fig. 4 shows the static lifetime ILM image of the wafer, which is obtained by a calibration of the dynamic lifetime ILM image [18]. The location of the samples analyzed by SEM and OM is marked with respect to the etching time. OM mappings represent the whole square-shaped sample area and should correlate well with the mean lifetime of the samples. The higher magnification of SEM compared to OM covers less investigated area, leading to a higher influence of local pinhole density variations. The

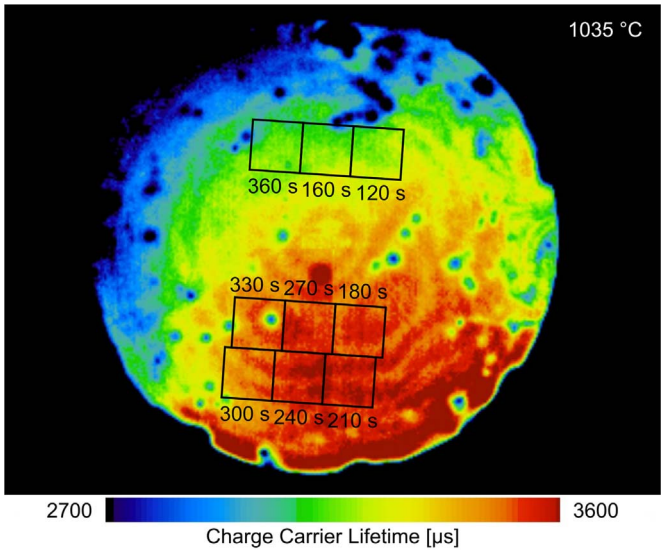

Fig. 4. Static lifetime ILM image and positions of analyzed samples with respect to etching time. OM mappings represent the whole square-shaped sample area each, while the analyzed region by SEM is much smaller. The scale bar was adapted to show small changes between the analyzed regions.

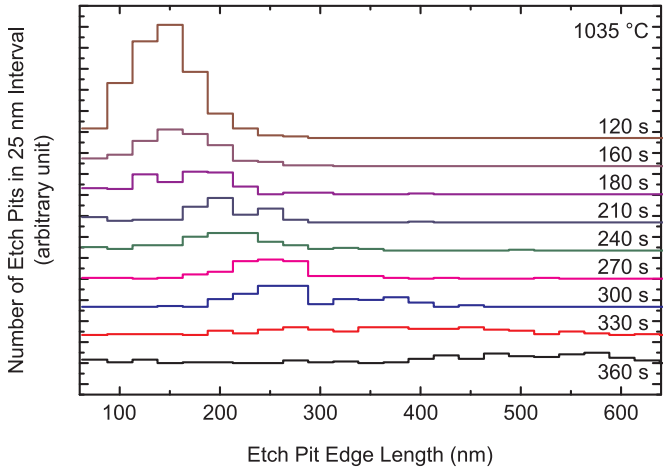

Fig. 5. EPD histogram for etch pit edge length intervals of 25 nm for different TMAH etching times. The plots are shifted in y-direction for better visualization.

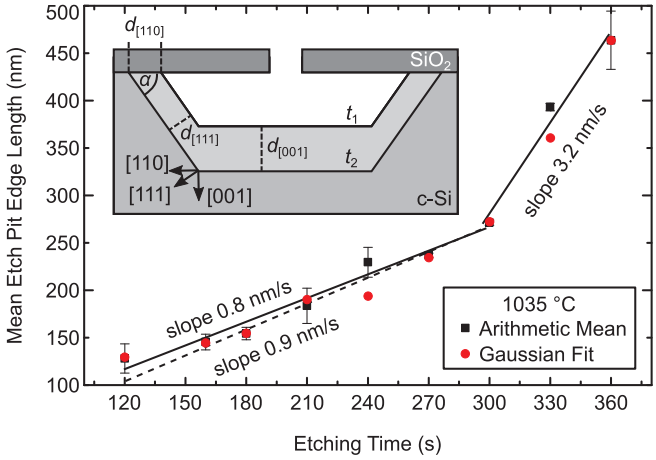

Fig. 6. Mean etch pit edge lengths (arithmetic mean and calculated center of Gaussian fit curves) for different TMAH etching times. For etching times up to 300 s two limiting linear fit curves can be applied (solid line = upper limit; dashed line = lower limit). For etching times longer than 300 s only one fit curve is applied.

regions analyzed by SEM are about 0.0005% of the areas investigated by OM and their positions on the samples are not exactly known. Please note that in Fig. 4. the scale bar was adapted to show small changes of lifetimes in the investigated regions on a high absolute lifetime level at an injection density of about 5×10^{15} cm^{-3}.

Relatively low lifetimes in the ILM image are found for the samples etched for 120 s and 160 s. However, as the etching time is not sufficient for all holes to be identified by OM, this trend can only be found in the SEM results showing increased EPDs. The lifetimes determined by ILM for samples etched for 180 s to 270 s are constantly high leading to low EPDs measured with OM and SEM. After etching for 300 s, a slightly higher EPD was determined corroborating the ILM results. The sample etched for 330 s shows a local inhomogeneity in lifetime that leads to an increased EPD determined by OM. This is not recorded by SEM as this area was probably not in the analyzed region. The sample etched for 360 s is again in an area with homogenously lower lifetimes leading to higher EPDs. Overall, we achieve a very good correlation of lifetimes measured by ILM and EPD determined by SEM and OM proving once more the connection between pinhole densities and electrical properties.

3.3. Etch pit size and etch rate development

For now, all variations in EPD seem to be solely caused by resolution reasons for short etching times or local inhomogeneities of the wafer and not by the etching process itself. If no new holes are introduced into the oxide during etching and assuming no transport related etch rate limitations, the size of the etch pits should simply increase linearly with time. In Fig. 5 the EPD histogram for etch pit edge length intervals of 25 nm for different TMAH etching times obtained by SEM are shown. The etch pit edge lengths corresponding to the maximum of the respective curves increase with etching time while the distribution broadens. After 120 s only etch pits with edge lengths up to 260 nm are found while after 360 s sizes up to 1.1 µm occur.

Almost all samples also show structures with sizes below 125 nm. Their fraction shrinks from 43% after 120 s to 2% after 270 s of TMAH processing due to the general increase of etch pit size with etching time. While the fraction remains close to 0% up to 330 s it increases again to 9% after etching for 360 s. This could indicate the introduction of new holes within the oxide caused by the etching process. However, due to the increasing sizes, we can still easily distinguish between original and newly introduced etch pits. As this effect only occurs for etching times of at least 360 s for this sample series, the suitable TMAH etching time for analyzing with OM is in the range of 210 s to 330 s and even longer for SEM for the samples shown here.

As the etch rate is also depended on the size of the pinholes within the oxide [16] we analyze the evolution of etch pit dimensions with respect to etching time. In Fig. 6 the mean etch pit lengths for all etching times are shown. Besides the arithmetic mean we also calculated the center of Gaussian fit curves applied to all data of Fig. 5. The etch pit edge lengths increase linearly up to 300 s. Two limiting fit curves can be applied to the corresponding data. The upper limit (solid line) yields a slope of 0.8 nm/s while the lower limit (dashed line) has a slope of 0.9 nm/s. After 300 s, the slope is increased by a factor of four to 3.2 nm/s.

The inset of Fig. 6 shows the geometrical model of an etch pit. The slope calculated is equal to the total enlargement of the etch pit in [110] direction per second. As the slopes of the linear fit curves for etching times up to 300 s are almost identical, the following calculations are done for the slope of 0.8 nm/s only. Half of the slope gives the etch rate in [110] direction $d_{[110]} = 0.4$ nm/s. The etch rate in [111] direction can be calculated by $d_{[111]} = \sin(\alpha) \times d_{[110]}$ with $\alpha = 54{,}74°$, resulting in $d_{[111]} = 0{,}33$ nm/s. These etch rates agree well with literature [19,20]. As *n*-poly-Si is etched by 15% TMAH solution at 80 °C with a rate of at least 20 nm/s [15], the 120 nm thick poly-Si layer is completely removed after 6 s. If we extrapolate the linear fit curves obtained for etching times of 120 – 300 s to the time of 6 s we obtain initial pinhole sizes between 1.4 nm and 21 nm for the moment the poly-Si is completely removed. With pinhole size and density we calculate a pinhole areal fraction between 0.00007% and 0.015% for this sample. For a more accurate calculation of the original pinhole size much more data is needed. However, these results are close to the pinhole diameter as proposed for the pinhole transport model [8,9] and as found in TEM investigations [13]. This again proves that the etch pits are indeed connected to pinholes.The reason for the increased slope in Fig. 6 after etching for 300 s leading to a four times higher etch rate of $d_{[110]} = 1.6$ nm/s could be linked to the etching of the interfacial oxide. With an etch rate of about 0.2 nm/min for SiO_2 [14] the 2.1 nm thick oxide layer will be completely removed after 600 s. However, as we undercut the SiO_2 layer, the oxide around a pinhole is etched from two sides leading to a complete removal above the etch pits within 300 s. This results in a strongly enhanced increase in etch pit size as possible transport limitations of the etch process due to the formerly small pinhole size are cancelled.

3.4. Process versatility

So far, we proved the stability of the TMAH etching procedure for samples with 2.1 nm thick thermal oxide and ion-implanted *n*-type poly-Si on shiny etched wafers. To demonstrate the versatility of this

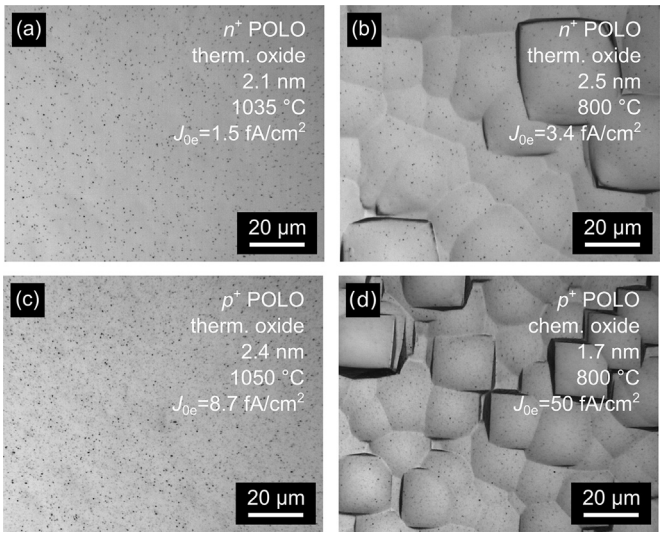

Fig. 7. OM images of samples after etching with TMAH. (a) *n*-type (ion-implanted) poly-Si on 2.1 nm thermal oxide on shiny-etched substrate annealed at 1035 °C. (b) *n*-type (*in situ* doped) poly-Si on 2.5 nm thermal oxide on damage-etched substrate annealed at 800 °C. (c) *p*-type (ion-implanted) poly-Si on 2.4 nm thermal oxide on shiny-etched substrate annealed at 1050 °C. (d) *p*-type (ion-implanted) poly-Si on 1.7 nm wet-chemical oxide on damage-etched substrate annealed at 800 °C.

method, we investigate 12 additional samples with varying oxide types (thermal or wet-chemical, the latter grown in a solution of ozone in de-ionized water) and thickness values (1.7–2.5 nm according to ellipsometry, currently cross-checked by TEM), differently doped poly-Si layers (*n*- and *p*-type, *in situ*-doped or ion-implanted) as well as different types of substrates (shiny- or damage-etched). Fig. 7 shows the OM images of four samples representing the variations mentioned, selected by comparable pinhole densities for *n*- and *p*-type samples. The sample with 2.1 nm thermal oxide and ion-implanted *n*-type poly-Si on a shiny-etched wafer annealed at 1035 °C in Fig. 7(a) shows an EPD density of 2.0×10^7 cm^{-2} and a J_0 of 1.5 fA/cm^2. The *in situ* *n*-doped layer on 2.5 nm thick thermal oxide on a damage-etched substrate annealed at 800 °C has a slightly lower pinhole density of 1.3×10^7 cm^{-2} while J_0 = 3.4 fA/cm^2 is more than twice as high. The *p*-type sample using 2.4 nm thermal oxide on a shiny-etched wafer annealed at 1050 °C (c) shows an EPD density of 1.6×10^8 cm^{-2} and a J_0 of 8.7 fA/cm^2. While the pinhole density of 2.2×10^8 cm^{-2} is only slightly higher for the *p*-type sample with wet-chemical SiO_2 on damage-etched substrate annealed at 800 °C (d), J_0 = 50 fA/cm^2 is 7 times higher than for the sample shown in (c). We conclude that comparable pinhole densities do not necessarily lead to equal J_0 values. This agrees with the model which includes not only pinhole density but also pinhole size and surface recombination velocity in passivated regions [9].

The pinhole density values of all additionally analyzed 12 samples (not all shown here) are in the range of 1.4×10^6 cm^{-2} to 3.0×10^8 cm^{-2}. The corresponding J_0 values are 1.4 fA/cm^2 up to 80 fA/cm^2. For a sample with wet-chemically grown oxide, we verified the existence of pinholes with an areal density of 2×10^7 cm^{-2} already after annealing at a temperature of 750 °C. This temperature is lower than the optimum annealing temperature for these junctions.

4. Conclusions

We find pinhole densities in the range of 1×10^6 to 3×10^7 cm^{-2} for wafers with very low J_0 values around 1.4 fA/cm^{-2}. The wafer with a J_0 value of 55 fA/cm^{-2} shows a pinhole density of 1.1×10^8 cm^{-2}, which is comparable to the value of 1×10^8 cm^{-2} estimated in [13] for a sample with J_0 = 41 fA/cm^{-2}. The relation between J_0 and the pinhole density as presented here and in Ref. [16] matches with the model reported in Refs. [8] and [9]. We prove the stability and versatility of the TMAH etching process by analyzing more than 40,000 etch pits in total in samples with multiple oxide types and thicknesses, differently doped poly-Si layers on several types of substrates. We prove the existence of pinholes even in samples with wet-chemically grown oxide annealed below their optimum junction formation temperature.

Acknowledgments

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