Conductivity and Surface Passivation Properties of Boron-Doped Poly-Silicon Passivated Contacts for c-Si Solar Cells

Audrey Morisset, Raphaël Cabal, Bernadette Grange, Clément Marchat, José Alvarez, Marie-Estelle Gueunier-Farret, Sébastien Dubois, and Jean-Paul Kleider*

Passivating the contacts of crystalline silicon (c-Si) solar cells with a poly-crystalline silicon (poly Si) layer on top of a thin silicon oxide (SiO_x) film are currently of growing interest to reduce recombination at the interface between the metal electrode and the c-Si substrate. This study focuses on the development of boron-doped poly-Si/SiO_x structure to obtain a hole selective passivated contact with a reduced recombination current density and a high photo-voltage potential. The poly-Si layer is obtained by depositing a hydrogen-rich amorphous silicon layer by plasma enhanced chemical vapor deposition (PECVD) exposed then to an annealing step. Using the PECVD route enables to single side deposit the poly Si layer, however, a blistering of the layer appears due to its high hydrogen content, which leads to the degradation of the poly-Si layer after annealing. In this study, the deposition temperature and gas flow ratio used during PECVD step are optimized to obtain blister-free poly-Si layer. The stability of the surface passivation properties over time is shown to depend on the blister density. The surface passivation properties are further improved thanks to a post process hydrogenation step. As a result, a mean implied photo-voltage value of 714 mV is obtained.

1. Introduction

Passivating the contacts of crystalline silicon (c-Si) solar cells with a poly-crystalline silicon (poly-Si) layer on top of a thin silicon oxide (SiO_x) film leads to the decrease of recombination at the metal/c-Si interface. Recently, c-Si solar cells with such poly-Si passivated contacts have shown conversion efficiencies beyond 26%.[1]

A promising way to develop the poly-Si/SiO_x structure relies on the deposition of hydrogen-rich amorphous silicon (a-Si:H) by plasma enhanced chemical vapor deposition (PECVD), followed by an annealing step required to crystallize the a-Si:H layer into poly-Si.[2–6] The PECVD approach enables to deposit the poly-Si layer on a single side of the wafer, contrarily to Low Pressure CVD technique that involves a deposition on both sides of the wafer.[7–9] However, if not optimized, PECVD of a-Si:H layer on top of SiO_x involves a blistering of the layer due to its high hydrogen (H) content which causes a severe degradation of the poly-Si layer after annealing.[4,5] Alloying the a-Si:H with carbon has been shown to solve the blistering issue.[6] Blister-free layers can be deposited without addition of carbon, as reported in ref. [3–5]. However, a detailed study of the interplay between process parameters and blistering has not been undertaken yet.

Another challenge of the poly-Si/SiO_x structure is the understanding of the transport mechanism of charge carriers through the SiO_x layer. The SiO_x layer is generally thin enough (<2 nm) to allow a transport by tunneling. However, it has been shown that the SiO_x integrity is altered upon annealing[10,11] leading to the hypothesis of a direct transport through pinholes within the SiO_x layer.[12] Recent studies focus on the detection of pinholes through SiO_x layer,[13–15] notably by means of conductive Atomic Force Microscopy (C-AFM).[16–18]

In the present study, a hole-selective poly-Si contact was developed by depositing a boron-doped a-Si:H (a-Si[B]) layer by PECVD on top of a thin SiO_x layer, followed by an annealing step to obtain the final poly-Si(B)/SiO_x structure. First, we address the optimization of the temperature and gas ratio during the PECVD step that led to blister-free poly-Si(B) layers. Then, we investigated the charge carrier transport through the SiO_x layer by means of C-AFM measurements on samples with and without SiO_x layer at the poly-Si/c-Si interface. Finally, the

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stability of the surface passivation properties over time was shown to depend on the blister density. As shown before, the addition of a hydrogenation step is beneficial to the surface passivation properties of the poly-Si/SiO_x structure.[5,6,19] In this study, the deposition of hydrogenated silicon nitride layer (SiN:H) on top of the poly-Si layer followed by a firing step helped to further improved the surface passivation properties leading to promising surface passivation properties on KOH-polished large area wafers.

2. Experimental Section

n-type 4-inch (100) Czochralski (Cz) silicon wafers with a thickness of 275 μm were used. The wafers feature mirror-polished surfaces and a resistivity in the range 1–5 Ω cm. The thin tunnel SiO_x layer was grown on both sides of the wafer by including a 10 min long chemical oxidation in ozonized DI-H_2O at the end of the standard RCA cleaning process. SiO_x layer thickness was measured by Spectroscopic Ellipsometry (SE) and was found to be 1.3 ± 0.1 nm. Subsequently, an in situ boron doped a-Si:H layer (a-Si[B]) was deposited by PECVD using silane, hydrogen, and diborane (2% diluted in hydrogen) as precursor gases. The samples were then annealed under argon atmosphere in the range 700–900 °C in order to activate dopants and crystallize the a-Si(B) layer subsequently referred to as "poly-Si(B) layer." The thicknesses of a-Si(B) (as deposited) and subsequent poly-Si(B) (once annealed) layer were evaluated by SE. The thickness of the poly-Si(B) layer was targeted in the range 15–30 nm. In the aim of simplifying the reading, since the thickness of the layer measured after deposition and after annealing were in good agreement with the targeted thickness (within 5% of error), only the targeted thickness is mentioned in the following (as d_{poly}).

Optical Microscopic observations of poly-Si(B) layers after annealing were performed. The resulting images were analyzed using the software ImageJ to assess the blister diameter and density.

Electrochemical Capacitance-Voltage (ECV) measurements were carried out in order to estimate the majority carrier (approximated as the active boron) concentration profile in the poly-Si(B) layers.

The Hall Effect technique was used to assess the electrical parameters of poly-Si(B) (doping, hole mobility, and conductivity). The conductivity of the poly-Si(B) layer was derived using the thickness estimated by SE after annealing. The Hall Effect technique was performed on $2 \times 2\,cm^2$ square pieces of sample cut with a laser (at least two squares per sample). A droplet of silver was deposited at each corner of the square to obtain an ohmic contact between the tip and the surface of the sample.

Transverse electrical conductivity analysis was conducted by C-AFM in contact mode using a platinum silicide AFM tip. The back side of the sample was polished and then glued with silver paste on an AFM metal holder. Before any C-AFM measurements the poly-Si(B) surface was exposed to 1% HF to remove the native oxide. C-AFM measurements were performed on $4 \times 4\,\mu m^2$ area with a −0.1 V polarization applied between the tip and the back contact.

The effective minority-carrier lifetime was measured by the Photo-Conductance Decay (PCD) technique as a function of the excess minority carrier density allowing to evaluate the surface passivation properties (implied open circuit voltage [iV_{oc}] and recombination current density [J_0]). The surface passivation properties were evaluated on symmetrical samples consisting in the stack: poly-Si(B)/SiO_x/c-Si/SiO_x/poly-Si(B). They were made from aforementioned 4 inch wafers but also from KOH polished n-type 156 psq Cz Si wafers with a resistivity of 6.5 Ω · cm and a thickness of 180 μm.

3. Results and Discussion

3.1. Development of a Blister-Free Poly-Si(B) Layer and Electrical Properties Evaluation

3.1.1. Blistering Reduction of the Poly-Si(B) Layer

Gas precursors used during the deposition step resulted in high H containing a-Si(B) layers.[20] For the poly-Si/SiO_x structure, it has been shown that the high H content of the deposited layer results in a blistering phenomenon of the poly-Si layer[4,5] as some hydrogen is able to stack at the poly-Si/SiO_x interface.[21]

In this study, 30 nm-thick a-Si(B) layers were initially PECV-deposited at a temperature $T_{dep} = 200\,°C$. Since H is able to diffuse from 200 °C in a-Si(B) layers,[22] the blistering phenomenon started to occur during the deposition step. It kept going during the annealing step at $T_a = 700\,°C$ resulting in a severely blistered poly-Si(B) layer. By tuning the deposition parameters, the reduction of the blistering was achieved: among other tests, the increase of T_{dep} (up to 300 °C) and reduction of deposition rate (by increasing $R = H_2/SiH_4$ gas ratio from up to 50) were found to be relevant approaches for reducing respectively blisters size and density.

Increasing the deposition temperature (T_{dep}) is known to reduce the H content of PECVD a-Si:H layers.[20] In this study, increasing T_{dep} from 220 to 300 °C resulted in a decrease of the blister diameter of 30 nm-thick poly-Si(B) layer from 30 to 13 μm. The increase of the gas flow ratio $R = H_2/SiH_4$ was then considered as a deposition rate reduction lever, allowing H to out-diffuse from the a-Si(B) layer during the deposition step. The increase of R from 6 to 50 reduced the blister density of 30 nm-thick poly-Si(B) layer from 1.5 to 0.6 mm^{-2}. **Figure 1** illustrates the reduction of blistering from $R = 25$ to $R = 50$. Decreasing the poly-Si(B) thickness to 15 nm enabled to obtain blister free poly-Si(B) layers after annealing at 700 °C (see Figure 1). The effect of the blister density on surface passivation stability over time was evaluated and is detailed below (Section 3.2.1.).

Lateral conductivity and free charge carrier (hole) mobility of poly-Si(B) layers were evaluated by Hall Effect technique as functions of T_{dep} and R optimizations (see **Figure 2**). The measurement uncertainty was reduced with the decrease of the poly-Si(B) blistering. The charge carrier mobility was slightly improved which we attributed to the blister reduction of the poly-Si(B) layer. As the doping density was measured constant at $1 \times 10^{20}\,cm^{-3}$, it resulted in an improvement of the conductivity. The final poly-Si(B) conductivity and mobility obtained after annealing at 700 °C were respectively $\sigma = 220\,S\,cm^{-1}$ and $\mu_h = 12.4\,cm^2\,V^{-1}\,s^{-1}$.

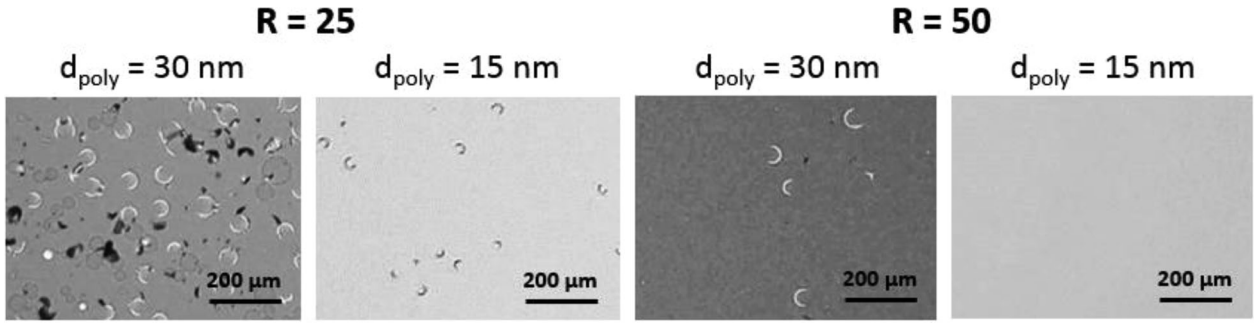

Figure 1. Optical microscope images taken at the surface of poly-Si(B) layer after annealing at $T_a = 700\,^{\circ}C$. The deposition temperature T_{dep} was kept constant at 300 °C, the gas flow ratio $R = H_2/SiH_4$ during deposition was increased from 25 to 50 resulting in the decrease of the blister density. The reduction of the thickness of the poly-Si(B) layer (d_{poly}) from 30 to 15 nm also enabled a reduction of the blister density, leading to 15 nm-thick blister-free poly-Si(B) layer.

For $T_a > 700\,^{\circ}C$, results of the Hall effect technique are not presented because of the boron in-diffusion from the poly-Si(B) to the c-Si (revealed by ECV measurements) which led to a stack of two p^+-doped regions available for current flows. An accurate evaluation of conductivity and mobility of poly-Si alone was then not possible anymore.

3.1.2. Transport Mechanism of Charge Carriers Through SiO_x Layer

The transport mechanism of free charge carriers through the SiO_x layer is not fully understood yet. The two main hypotheses are transport by tunnel effect[14] or direct transport through nanometric pinholes forming within the SiO_x layer upon annealing.[12] As there are many ways to form the poly-Si/SiO_x structure, the answer might be process-dependent.[15] The pinhole formation within the SiO_x layer has been revealed by means of a selective chemical etching coupled with microscopic observations.[13] C-AFM has also been identified as an interesting technique to investigate the existence of pinholes within the SiO_x layer.[16–18]

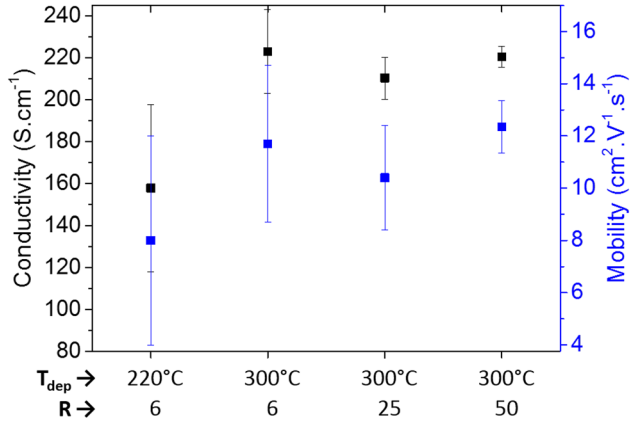

Figure 2. Lateral conductivity and free charge carrier mobility of the poly-Si(B) layer evaluated by Hall Effect technique after annealing at $T_a = 700\,^{\circ}C$ ($d_{poly} = 30$ nm). The deposition temperature T_{dep} and the gas flow ratio $R = H_2/SiH_4$ were tuned to reduce blistering of the poly-Si(B) layer after annealing which also reduced the measurement uncertainty of the lateral conductivity and mobility.

In this study, we investigated the transport of free charge carriers of our samples by means of C-AFM measurements performed after annealing at different temperature.[16] Two samples were prepared with the standard stack: poly-Si(B)/SiO_x/c-Si. The poly-Si(B) layer was developed with optimal deposition conditions $T_{dep} = 300\,^{\circ}C$ and $R = H_2/SiH_4 = 50$ and a thickness of $d_{poly} = 15$ nm to avoid any blistering of the layer. **Figure 3**(a and b) illustrates the current mapping obtained at the surface of the poly-Si(B) layer after annealing at $T_a = 700$ and $T_a = 900\,^{\circ}C$. In both cases, the current mapping obtained showed localized regions (dots) of higher current levels. The current level and the density of dots were found to be higher for $T_a = 900\,^{\circ}C$ than for $T_a = 700\,^{\circ}C$. These results are in line with the one of Lancaster et al.[16] As the density of high current dots increased with increasing T_a, one might consider that the current dots detected by C-AFM are directly mirroring pinholes within SiO_x layer.

To further investigate this point, C-AFM measurements were performed on samples without interfacial SiO_x layer, that is, on the stack: poly-Si(B)/c-Si. These samples were prepared by dipping the c-Si substrate in Hydrofluoric acid (HF) prior to the PECVD step (delay <10 min). These samples showed really poor surface passivation properties ($iV_{oc} < 600$ mV) indicating the efficacy of the HF pre-treatment to remove the interfacial SiO_x layer. Figure 3(c and d) illustrates the current mapping obtained at the surface of such samples after annealing at $T_a = 700\,^{\circ}C$ and $T_a = 900\,^{\circ}C$. The current mapping obtained were similar to the one obtained with an intentionally grown interfacial SiO_x layer. This result invalidates the previous assumption concerning high current dots/pinhole correlation. Another explanation could be that the current mapping pattern is rather linked to the surface state of the poly-Si(B). Indeed, the annealing step was performed under argon atmosphere but the furnace door was not completely sealed, resulting in a native oxide growth at the poly-Si(B) surface after annealing. The sample surface was HF cleaned before C-AFM measurement to remove the native oxide but it is possible that the native oxide growth roughened the poly-Si(B) surface[23] which would affect the current levels detected by C-AFM at the surface of the poly-Si layer.[17] Further characterizations are required to identify the origin of high current dots detected by C-AFM.

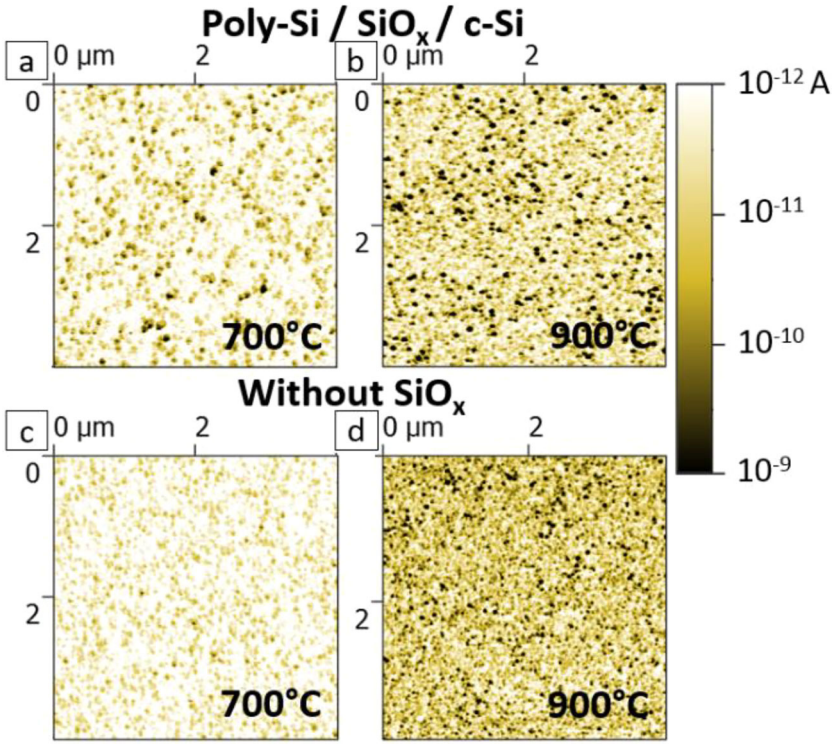

Figure 3. Current mapping measured by C-AFM at the poly-Si(B) surface of poly-Si(B)/SiO_x structure after annealing at 700 °C (a) and 900 °C (b). As the high current dots observed were likely to mirror pinholes within the SiO_x layer, samples without interfacial SiO_x layer were analyzed after annealing at 700 °C (c) and 900 °C (d) leading to similar current mapping pattern.

3.2. Surface Passivation Properties of the Poly-Si(B)/SiO_x Structure

3.2.1. Effect of the Blistering on the Surface Passivation Stability

The effect of blistering on surface passivation properties was studied on samples made from aforementioned 4 inch c-Si substrates. The poly-Si(B)/SiO_x structure was developed on both sides of the substrate so that the final sample structure was the following: poly-Si(B)/SiO_x/c-Si/SiO_x/poly-Si(B). In order to assess the effect of blistering on passivation properties, we used the same deposition conditions than samples mentioned in Section 3.1.1, resulting in poly-Si(B) layers with blister densities from 1.5 to 0 mm^{-2} after annealing at $T_a = 700$ °C (see Figure 1). **Figure 4** plots the charge carrier effective lifetime versus injection level, right after sample processing, after 24 h, and eventually 2 months of storage in the dark, under air. Samples involving a 30 nm-thick layer deposited with $R = 25$ (showing the highest blister density) exhibited the lowest initial passivation level and poorest stability (the initial iV_{oc} of 600 mV decreased down to 540 mV after 2 months of storage). The reduction of poly-Si thickness down to 15 nm led to a decrease of blister density, enhancing the initial iV_{oc} (660 mV), but it did not solve the stability issue previously observed (iV_{oc} drops to 620 mV after 2 months). The samples with a 30 nm-thick poly-Si deposited with our optimized ratio $R = 50$ exhibited an initial iV_{oc} of 665 mV which slightly decreased to 660 mV after 2 months. The reduction of poly-Si thickness to 15 nm enabled to obtain not only the highest initial iV_{oc} (670 mV) but also an excellent stability of the charge carrier effective lifetime and iV_{oc} after 2 months. To summarize, the blister density was shown to play a role in surface passivation stability over time. Only poly-Si(B) layers deposited with $R = 50$ (blister density <0.35 mm^{-2}) showed an acceptable stability. In the following, the deposition conditions: $T_{dep} = 300$ °C, $R = H_2/SiH_4 = 50$, $d_{poly} = 15$ nm, were systematically used.

3.2.2. Effect of the Annealing and Post Process Hydrogenation on Passivation Properties

The effect of the annealing temperature (T_a) on surface passivation properties was studied. As before, the poly-Si(B)/SiO_x structure was developed on both sides of afore-described KOH polished 156 psq c-Si substrates. Optimal

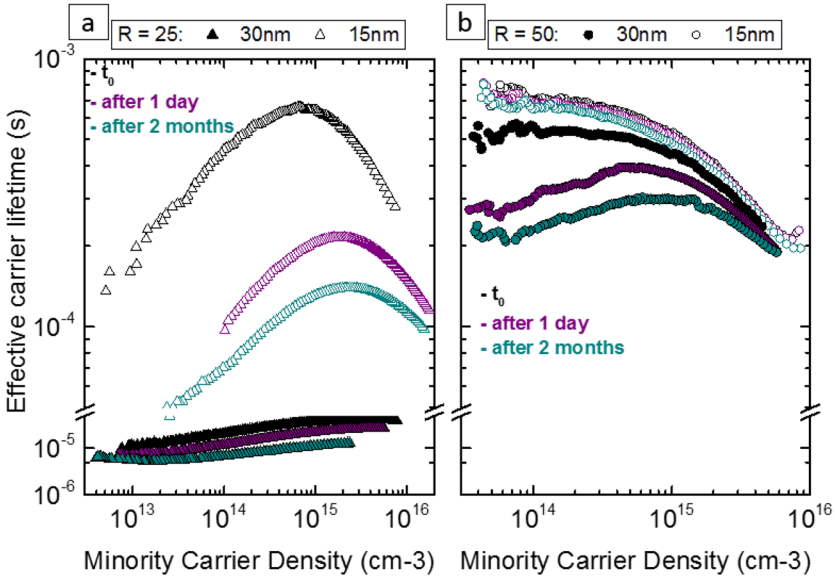

Figure 4. Effective carrier lifetime stability within time measured on symmetrical samples with poly-Si(B)/SiO_x structure. The poly-Si(B) layer was developed using different gas flow ratio R during deposition: $R = 25$ (a) and $R = 50$ (b). For each ratio R, two poly-Si(B) thicknesses were targeted: 15 and 30 nm, resulting in different blister density (see **Figure 1**). PCD measurement was carried out after processing (black symbols), after 24 h (violet symbols) and 2 months (green symbols) of storage. The blister density was shown to play a role on surface passivation stability over time.

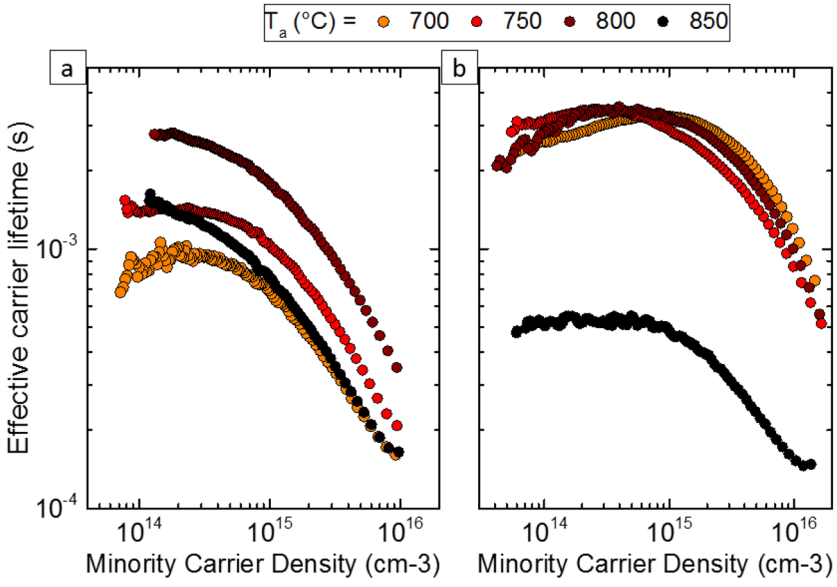

Figure 5. Effective carrier lifetime curve measured after different poly-Si(B) annealing temperature (T_a) on symmetrical samples right after annealing (a) and after a post passivation process consisting in the deposition of a SiN:H layer followed by a firing step (b).

deposition parameters defined in the previous section ($T_{dep} = 300\,°C$, $R = 50$, $d_{poly} = 15$ nm) were used. The 30 min-long annealing step subsequent to the deposition of a-Si(B) was performed at a temperature T_a varied from 700 to 850 °C. To further improve the surface passivation properties, a post process hydrogenation step was carried out, consisting in the deposition of a 70 nm-thick SiN:H layer on top of the poly-Si(B) layer followed by a firing step (800 °C, 30 s) in a conventional belt furnace. The charge carrier effective lifetime versus injection level was measured right after the annealing step and after the post process hydrogenation step (see **Figure 5**). After the annealing, the carrier effective lifetime steadily improved when T_a rose from 700 to 800 °C, probably due to the increase of the B in-diffusion in the c-Si substrate (revealed by ECV measurement) that enhanced the field-effect passivation. Beyond 800 °C, the lifetime dropped drastically due to either excessive B in-diffusion into c-Si substrate, and/or an important degradation of interfacial tunnel SiO_x layer.

The effect of the post process step (SiN:H deposition + firing) was highly positive for all samples annealed in the range 700–800 °C, allowing to obtain a mean iV_{oc} of 714 mV and a mean recombination current density J_0 of 7 fA cm^{-2}. One can notice a maximal effective lifetime improvement for samples annealed at $T_a = 700\,°C$. Beyond 800 °C, the post passivation process showed no benefit. Please note that the innocuity of such thermal annealing on wafers bulk quality was verified with monitor bare samples that were exposed to the annealing step, had then their surfaces cleaned, and were eventually double-side coated with an intrinsic a-Si passivating layer. This layer was 80 nm-thick, and granted a surface recombination velocity below 1 cm s^{-1}, so that the effective lifetime measured on such samples was assumed to be limited by the actual bulk lifetime. As can be seen on **Figure 6**, the impact of annealing temperature on substrate bulk was almost negligible and is not likely to be responsible for the effective lifetime T-dynamics previously observed.

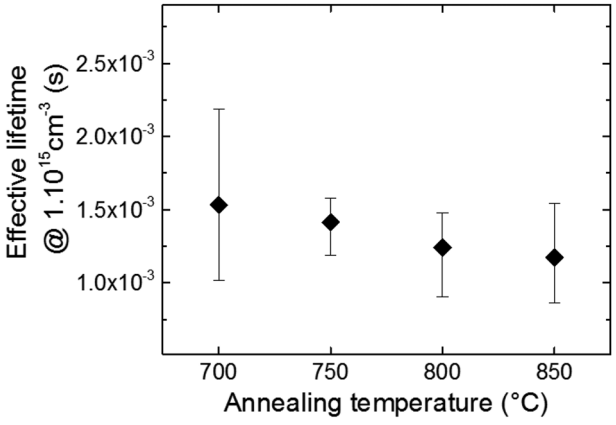

Figure 6. Monitor wafer lifetime variation when exposed to poly-Si(B) annealing thermal budget.

4. Conclusion

The study focused on the development of poly-Si(B)/SiO_x structures for passivating contacts of high efficiency c-Si solar cells. The optimization of the temperature and gas flow ratio used during the PECVD step enabled to obtain blister-free poly-Si(B)/SiO_x structures. The transport mechanism of free charge carriers through the SiO_x layer was investigated by means of C-AFM. A greater density of high current dots was detected on samples annealed at higher temperature. However, C-AFM measurements performed on samples without SiO_x layer at the poly-Si(B)/c-Si interface invalidate the direct link between these high current dots and the existence of pinholes within the SiO_x layer.

The passivation level and stability over time were shown to depend on the blister density of the poly-Si(B) layer. The stability of surface passivation properties provided by a 15 nm-thick blister-free poly-Si(B) layer was verified. The passivation level was further improved by optimizing the annealing temperature of the structure and by adding a post process hydrogenation step. A mean iV_{oc} of 714 mV was obtained on symmetrical samples made of 156 psq KOH-polished c-Si wafers. This result is promising for future device integration of the poly-Si(B)/SiO_x passivating structure.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The author declare no conflict of interest.

Keywords

C-AFM, c-Si solar cells, passivating contacts, plasma enhanced chemical vapor deposition (PECVD), poly-silicon

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[1] F. Haase, C. Hollemann, S. Schäfer, A. Merkle, M. Rienäcker, J. Krügener, R. Brendel, R. Peibst, *Sol. Energy Mater. Sol. Cells* **2018**, *186*, 184.
[2] F. Feldmann, M. Bivour, C. Reichel, M. Hermle, S. W. Glunz, *Sol. Energy Mater. Sol. Cells* **2014**, *120*, 270.
[3] Y. Larionova, M. Turcu, S. Reiter, R. Brendel, D. Tetzlaff, J. Krügener, T. Wietler, U. Höhne, J.-D. Kähler, R. Peibst, *Phys. Status Solidi A* **2017**, *214*, 1700058.
[4] Y. Tao, E. L. Chang, A. Upadhyaya, B. Roundaville, Y.-W. Ok, K. Madani, C.-W. Chen, K. Tate, V. Upadhyaya, F. Zimbardi, in *Photovolt. Spec. Conf. PVSC 2015 IEEE 42nd*, IEEE, **2015**, pp. 1–5.
[5] B. Nemeth, D. L. Young, M. R. Page, V. LaSalvia, S. Johnston, R. Reedy, P. Stradins, *J. Mater. Res.* **2016**, *31*, 671.
[6] G. Nogay, J. Stuckelberger, P. Wyss, E. Rucavado, C. Allebé, T. Koida, M. Morales-Masis, M. Despeisse, F.-J. Haug, P. Löper, F.-J. Haug, P. Löper, C. Ballif, *Sol. Energy Mater. Sol. Cells* **2017**, *173*, 18.
[7] U. Römer, R. Peibst, T. Ohrdes, B. Lim, J. Krügener, E. Bugiel, T. Wietler, R. Brendel, *Sol. Energy Mater. Sol. Cells* **2014**, *131*, 85.
[8] F. Feldmann, C. Reichel, R. Müller, M. Hermle, *Sol. Energy Mater. Sol. Cells* **2017**, *159*, 265.
[9] Y. Wu, M. K. Stodolny, L. J. Geerligs, M. Lenes, J.-M. Luchies, *Energy Procedia*. **2016**, *92*, 427.
[10] G. R. Wolstenholme, N. Jorgensen, P. Ashburn, G. R. Booker, *J. Appl. Phys*. **1987**, *61*, 225.
[11] D. Tetzlaff, J. Krügener, Y. Larionova, S. Reiter, M. Turcu, R. Peibst, U. Höhne, J.-D. Kähler, T. Wietler, in *Photovolt. Spec. Conf. PVSC 2016 IEEE 43rd*, IEEE, **2016**, pp. 221–224.
[12] R. Peibst, U. Römer, Y. Larionova, M. Rienäcker, A. Merkle, N. Folchert, S. Reiter, M. Turcu, B. Min, J. Krügener, D. Tetzlaff, E. Bugiel, *Sol. Energy Mater. Sol. Cells* **2016**, *158*, 60.
[13] D. Tetzlaff, J. Krügener, Y. Larionova, S. Reiter, M. Turcu, F. Haase, R. Brendel, R. Peibst, U. Höhne, J.-D. Kähler, T. Wietler, *Sol. Energy Mater. Sol. Cells* **2017**, *173*, 106.
[14] F. Feldmann, G. Nogay, P. Löper, D. L. Young, B. G. Lee, P. Stradins, M. Hermle, S. W. Glunz, *Sol. Energy Mater. Sol. Cells* **2018**, *178*, 15.
[15] N. Folchert, M. Rienäcker, A. A. Yeo, B. Min, R. Peibst, R. Brendel, *Sol. Energy Mater. Sol. Cells* **2018**, *185*, 425.
[16] K. Lancaster, S. Großer, F. Feldmann, V. Naumann, C. Hagendorf, *Energy Procedia*. **2016**, *92*, 116.
[17] U. Römer, *PhD Thesis*, Gottfried Wilhelm Leibniz Universität, Hannover, **2015**.
[18] Z. Zhang, Y. Zeng, C.-S. Jiang, Y. Huang, M. Liao, H. Tong, M. Al-Jassim, P. Gao, C. Shou, X. Zhou, B. Yan, J. Yeb, *Sol. Energy Mater. Sol. Cells* **2018**, *187*, 113.
[19] F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, S. W. Glunz, *Sol. Energy Mater. Sol. Cells* **2014**, *131*, 46.
[20] R. A. Street, *Hydrogenated Amorphous Silicon*. Cambridge, England **1991**.
[21] J. A. Aguiar, D. Young, B. Lee, W. Nemeth, S. Harvey, T. Aoki, M. Al-Jassim, P. Stradins, in *Photovolt. Spec. Conf. PVSC 2016 IEEE 43rd*, IEEE, **2016**, pp. 3667–3670.
[22] S. De Wolf, M. Kondo, *Appl. Phys. Lett*. **2007**, *91*, 112109.
[23] E. A. Irene, E. Tierney, D. W. Dong, *J. Electrochem. Soc*. **1980**, *127*, 705.

