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# Highly accurate tuning of current–voltage characteristic shift in a photo-sensitive three terminal metal–insulator–semiconductor device

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## ABSTRACT

We present a planar three terminal device fabricated on a silicon-on-insulator substrate. The device is based on a two-layer dielectric stack comprising $SiO_2$ tunneling and $HfO_2$ layers. A so-called gate electrode is placed between two other contacts, of the source and drain, all deposited on the insulator stack. In the dark as well as under illumination, the current–voltage characteristic can be shifted in an ideal linear manner with changes in a positive gate voltage with the shift being somewhat larger under illumination. The reason for the change of shift is the ability of high-density oxygen vacancies, arranged in the filament regions within an $HfO_2$ sublayer that was voltage stress. Namely, holes or electrons are trapped in the $HfO_2$ sublayer, respectively, from the inverted or accumulated Si layer. This process is controlled by the gate and drain bias levels. Moreover, under illumination and at negative gate and drain voltages, the device exhibits negative differential resistance caused by capture of photo-generated minority carriers induced in the depletion region of the Si after they tunnel through the $SiO_2$ layer by negative oxygen vacancies that migrate to the $SiO_2/HfO_2$ interface through the filament regions. Finally, the low level of saturation current in the dark and the ability to precisely control its value by illumination intensity, together with a large sensitivity of 80–85 A/W and 25 A/W, at 490 nm and 365 nm, respectively, allow additional applications that cannot be achieved with conventional MIS devices.



## I. INTRODUCTION

Planar metal–insulator–semiconductor field effect transistors (MISFET) fabricated on silicon on insulator (SOI) substrates with the drain and source employing Schottky contacts have been studied extensively.[1,2] This structure avoids special doping processes of the drain and source areas and, therefore, simplifies FET fabrication. In addition, such a transistor minimizes the off-state leakage current, thereby increasing the on/off ratio significantly. A modification was reported in Refs. 3–5 where in addition to the conventional planar drain, source, and front-gate electrodes, a back-gate electrode was added. Both gate electrodes are deposited on top of insulator layers, which are placed on opposite surfaces of the un-doped Si layer, with thickness of a few tens of nm. The back-gate electrode serves to control the density and type of carriers (n or p) in the channel since it can take on either bias polarity, while the front gate acts as in a conventional metal–oxide–semiconductor (MOS) FET device,[6] governing the source to the drain current flow in the channel. Such a design provides a reconfigurable n-MOSFET or p-MOSFET device and, hence, enables new functionalities.[4,7] In addition, Refs. 5 and 8–10 demonstrated that tuning the back-gate voltage controls the threshold voltage with high precision. Therefore, the main difference between single-gate and dual-gate transistors is the ability to control the transfer characteristic using the back-gate bias. For logic elements (for example, invertors), adjustment of the threshold allows precise control of the input signal at which inversion sets in as well as optimization of the noise margin.[5]

We propose and demonstrate here a three terminal planar device fabricated on an SOI substrate. It has many attributes of the dual gate structures described above but is significantly simpler and offers different functionalities. In the proposed device, all three contacts are deposited on a two-layer dielectric stack so that the fabrication is vastly simpler. Moreover, the placement of the electrodes on top of the dielectric stack ensures small leakage currents

in the off state. All three electrode regions are voltage stressed to form filamentation paths enabling the current flow through the insulator stack and, therefore, in the silicon layer. Functionally, the device reveals a unique output characteristic that exhibits on and off states, which are highly controllable by the central (gate) electrode. This feature is like to threshold voltage tuning in a dual-gate FET.[2–5] Finally, the new device is photosensitive over a wide wavelength range. Illumination affects the carrier density in the electrode regions and, hence, controls the output current level. The proposed device has a large potential for different logic circuits,[11] oscillators,[12] or memory systems,[13] where in each it can broaden the functionality.

## II. EXPERIMENTAL PROCEDURE

A schematic description of the three terminal device is shown in Fig. 1, where, for clarity, the electrodes are called the source, gate, and drain, in analogy with conventional MISFETs. The device is based on our previously published two terminal metal–insulator–semiconductor–insulator–metal (MISIM) structure, where the insulator is a stack of tunneling thermal $SiO_2$ and atomic layer deposited $HfO_2$ layers.[14] The SOI substrate includes a 2.8 $\mu$m thick phosphorous doped n-Si layer with a resistivity of 90 $\Omega$ cm grown on top of a 1.3 $\mu$m thick $SiO_2$ spacer. The Si layer was covered with a 3 nm thermal $SiO_2$ layer followed by a 19 nm thick $HfO_2$ layer deposited by atomic layer deposition. Pd/Au electrodes were deposited by electron beam evaporation without any local doping of the drain and source areas. The contact pad of the gate was placed on top of a 2 $\mu$m thick organic insulator (SU-8), while the drain, the source, and the part of the gate electrodes were deposited directly on the dielectric stack. The proposed device configuration is similar to that of a conventional flat three-terminal device with a single gate electrode located between two other electrodes. However, it differs from them in the design of the electrodes surrounding the gate. Here, the distance between the electrodes in their narrow parts is smaller than in the channel area (around of gate). Hence, the channel length varies due to the circular shape of the electrodes. The channel width was 17 $\mu$m, the gate–source and gate–drain distances were 5 $\mu$m, and inter-electrode distance at the narrowest part was 10 $\mu$m.

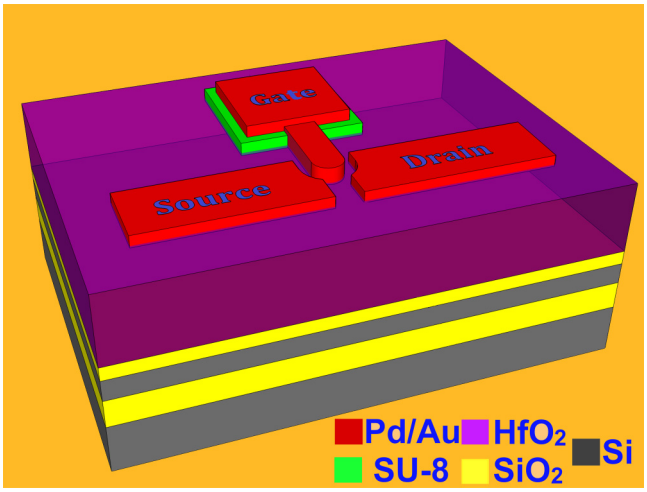


**FIG. 1.** Schematic of the electrode configuration and the structure of the device.

A filamentation path was formed in the dielectric stack[15] by voltage stressing with several millisecond long pulses having an amplitude of 12–14 V, which is close to, but lower than, the hard breakdown voltage. This process is similar to the one used in $HfO_2$[16–18] based resistive switching devices.

Once the filamentation path is formed, source and drain are Schottky-like diodes with identical electrodes formed on low-doped n type Si. The conductivity of the channel is similar to that of a regular FET, controlled by the gate voltage. Thus, the structure between any two electrodes is an MISIM diode.[14]

For optical characterization, a light emitting diode array in the 365–880 nm wavelength range was used. The illumination spot and optical window areas were, respectively, $2.85 \times 10^{-3}$ cm$^2$ and $2.65 \times 10^{-6}$ cm$^2$. Illumination does not affect the current–voltage characteristics of the unstressed structures since no current path exists before the filament paths are formed. The source electrode was grounded so that all the voltage levels stated throughout the text are referenced to its (zero) potential. The current–voltage characteristics were measured in the drain and gate voltages ($V_D$ and $V_G$, respectively) range of −5 V to +5 V using 100 mV increments and a delay time of 80 $\mu$s. An Agilent 4155C semiconductor parameter analyzer in the FET mode with a grounded source was employed for characterization.

## III. EXPERIMENTAL RESULTS AND DISCUSSION

### A. Current–voltage characteristics

Source to drain current–voltage characteristics ($I_D - V_D$) measured in the dark and under illumination are presented in Fig. 2. The source electrode was grounded ($V_S = 0$) in all cases; it injects electrons or holes, depending on the polarity of the source bias, to the n or p channel, which is formed in the silicon close to the interface under the gate dielectric stack. The dark $I_D - V_D$ characteristics, shown in Fig. 2(a), differ in several ways from those of a conventional MOSFET.[6] (i) At negative drain bias (see inset), the gate voltage has a minor effect on the absolute values of the negative source to drain current. The characteristics shift, however, toward positive drain voltages as $|V_G|$ decreases. (ii) At $V_D$ and $V_G$ larger than −2 V, $I_D$ increases sharply after an inflection point ($I_D = 0$), where the sign of the current changes from negative to positive. (iii) For $V_G > -1$ V, the characteristics are parallel and shifted from each other by exactly the change in $V_{SG}$ relative to the inflection point.

The $I_D - V_D$ characteristics under illumination, shown in Fig. 2(b), exhibit several differences compared to the dark regime. (i) For $|V_G|$ above 3 V, $I_D$ does not vary but for $|V_G|$ in the 3 to 1 V range, it rises significantly and saturated [see inset in Fig. 2(b)]. (ii) For $V_G$ larger than −1 V, the $I_D - V_D$ characteristics have symmetric branches relative to the inflection points. (iii) The slope of the saturation current is nearly independent of $V_D$.

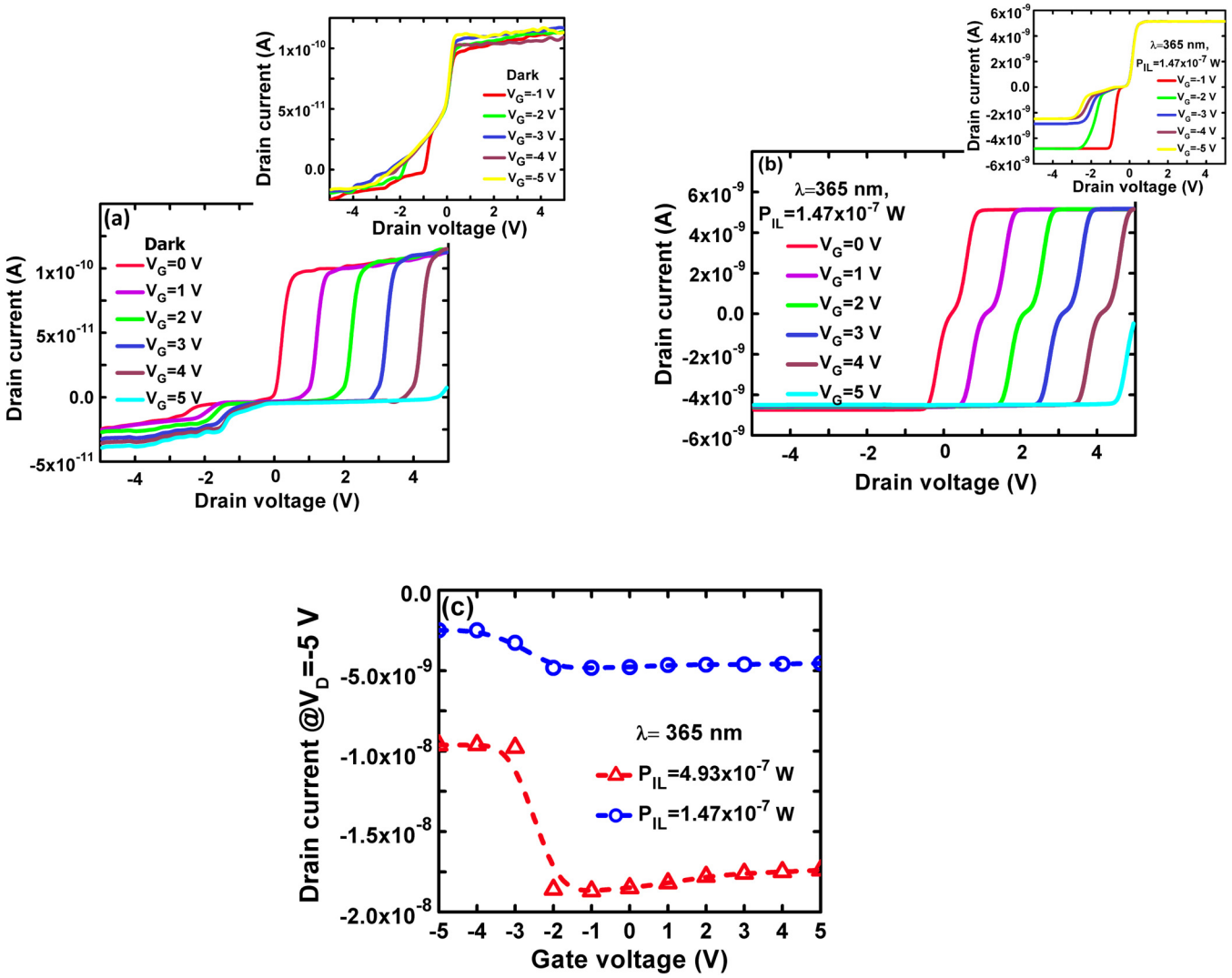


**FIG. 2.** $I_D - V_D$ characteristics measured in the dark (a) and under illumination (b) for positive gate voltages. Insets in (a) and (b) show measurements under negative gate voltages. The illumination was at 365 nm and a power of 1.47 × 10$^{-7}$ W. (c) Illumination power dependence of $I_D - V_G$ characteristics at $V_D = -5$ V.

Figure 2(c) describes the drain current dependence on the gate voltage measured at $V_D = -5$ V for various illumination intensities. The fixed drain current is non-monotonic for all illumination intensities, with a maximum in the gate voltage range of −2 V and −1 V. The nature of these curves indicates the phenomenon of negative differential conductivity (NDC), in particular, at large negative gate voltages, consistent with the inset of Fig. 2(b). For $V_G$, ranging from −1 V to +5 V, an insignificant drop from the maximum is observed, but the effect is smaller than that with negative gate voltages.

The output characteristics were also analyzed using the power exponent formalism $\alpha_D = \frac{d\ln(I_D)}{d\ln(V_D)}$ (Ref. 14) as shown in Fig. 3. Figure 3(a) shows the $\alpha_D - V_D$ characteristics in the dark for positive gate voltages. The interesting features are for positive drain voltages where the curves shift toward positive voltages in direct correspondence to the changes in the gate voltage. The maximum value of the power exponent ($\alpha_{D,max}$) exhibits a very large change from about 2 to 47. For negative drain voltages, the current is extremely low (in the pA range), and hence, the calculated $\alpha_D$ values are noisy. The behavior under illumination is similar for positive drain voltages except that $\alpha_{D,max}$ is smaller and varies between 3.5 and 35 as seen in Fig. 3(b). A strong peak occurs in all cases prior to $\alpha_{D,max}$. This peak represents the voltage of the inflection point where the current changes sign.

At negative gate and drain voltages and under illumination [insert in Fig. 3(b)], the $\alpha_D - V_D$ curves exhibit clear maxima

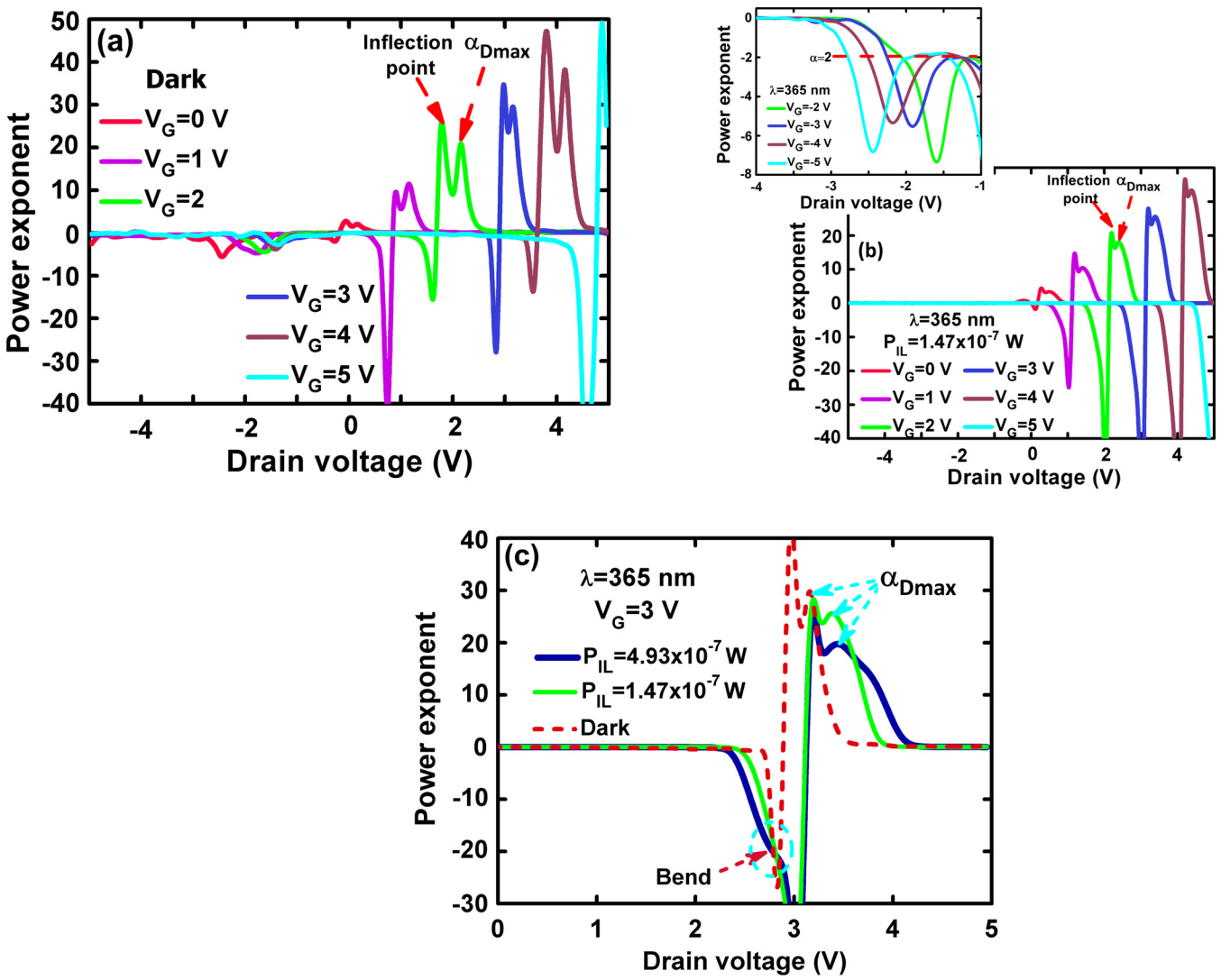


**FIG. 3.** $\alpha_D - V_D$ characteristics measured at positive gate voltages in the dark (a) and under illumination (b); peculiar parts of the $\alpha_D - V_D$ curves measured at $V_G = 3$ V and under different illumination regimes (c). The inset in (b) shows curves measured under illumination at negative gate voltages.

with values of 6–7. For large $|V_D|$ and independent of the polarity of $V_G$, $\alpha_D$reduces to zero consistent with the saturated behavior as seen in Fig. 2. The region of the $\alpha_D - V_D$ curves that correspond to negative current (for positive gate and drain voltages) does not exhibit maxima but rather bend [marked by circles in Fig. 3(c)]. This is most pronounced for large illumination intensities.

The drain voltage corresponding to the inflection points and to the power exponent maxima increases with illumination intensity ($P_{IL}$) by about 0.5 V relative to the dark regime. However, for all intensities, their shift is linear with increasing positive gate voltage, as shown in Figs. 4(a) and 4(b). The slope of $I_D - V_D$ and, therefore, $\alpha_{D,\,max}$ reduce with illumination, but their dependence on the positive gate voltage is linear [see Fig. 4(c)]. Figure 3(c) at a constant gate voltage $V_D = +3$ V clearly illustrates the variation of $\alpha_D - V_D$ trends with illumination as shown in Fig. 4(c). It is clearly seen that the illumination power causes a shift of the extreme points to the positive voltage side, reduces $\alpha_{D,max}$, and enlarges the area under the maxima.

Figure 4(d) illustrates the widening (along the drain voltage axis) of the $\alpha_D - V_D$ curves, measured at $V_G = 0$ V, with light intensity. While the curves widen by a factor of 3–3.5, their maximum values change little with intensity. In the inset, the dependence of widening of the $\alpha_D - V_D$ curves on illumination intensity is shown. In the

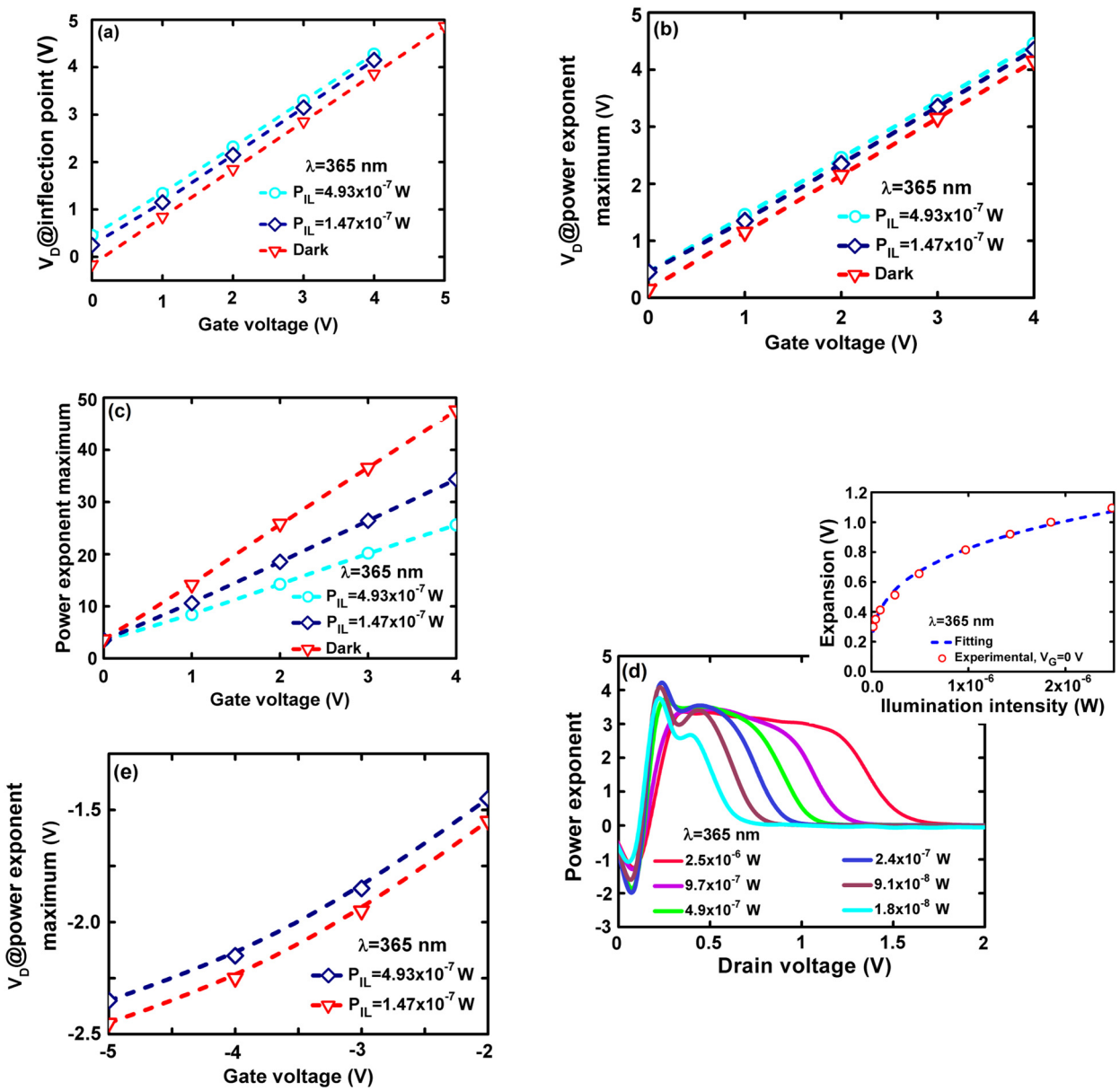


**FIG. 4.** The change with positive gate voltage of the drain voltage corresponding to the inflection points (a) and power exponent maxima (b) and power exponent maxima measured under different illumination levels (c). The peculiar parts of the $\alpha_D - V_D$ characteristics are near $V_G = 0$ V and under different illumination intensities (d); change of the drain voltage corresponding to the power exponent maxima with negative gate voltage (e). The inset shows the widening of the $\alpha_D - V_D$ curves along the drain voltage axis with illumination intensity. The symbols and dashed lines in (a), (b), and (c) are, respectively, experimental results and linear fits.

power range of $1.8 \times 10^{-8}$ W to $2.5 \times 10^{-6}$ W, the curve changes as $P_{IL}^{0.3}$, while the maximum expansion of the $\alpha_D - V_D$ curves is 1.05 V. Figure 4(e) describes the shift of the maximum value of $\alpha_D - V_D$ with negative gate voltages. The shift increases nonlinearly with $|V_G|$ and depends weakly on illumination intensity. Once more, the low current values in the dark prevent an accurate calculation of $\alpha_D$ and, therefore, determination of the corresponding $V_D$.

### B. Discussion of current flow peculiarities

To explain the behavior of the $I_D - V_D$ characteristics, we consider separately negative and positive gate voltages. For ($V_G < 0$), the $I_D - V_D$ characteristics comprise two distinct branches one for each drain voltage polarity. The source potential is always high relative to the gate, and therefore, the source can inject holes toward

the Si layer located under the gate, which is depleted of electrons, while it is inverted and, hence, filled with holes. Since $V_{SD} < 0$, a p-Si layer is also formed under the drain electrode. Such conditions result in a drain current increase with the absolute value of the gate voltage as in an ordinary p channel field effect transistors. In the present device, $I_D$ reduces with $|V_G|$. This unusual behavior, which is in a way a form of NDC, is due to different types of states located in the stressed $HfO_2$ sublayer or the $SiO_2/HfO_2$ interface that trap holes or electrons from the Si layer.

Metal oxides and, in particular, $HfO_2$ are known to contain high concentrations of neutral or ionized shallow donor or acceptor levels stemming from oxygen vacancies. Five different mono-energetic charge states for oxygen vacancies, namely, neutral $V_0$, positive $V_0^+$, $V_0^{++}$, and negative $V_0^-$, $V_0^{--}$ were theoretically considered in Refs. 19–21 and are present in the bandgap of an as-deposited monoclinic layer of $HfO_2$. With no applied voltage, these oxygen vacancies are randomly distributed in the $HfO_2$ layer between the electrodes and the tunneling $SiO_2$ sublayer as seen in the schematic model illustrated in Fig. 5(a). It was shown in Refs. 15 and 22–24 that the soft breakdown of structures based on $HfO_2$ films, under an external applied bias of about 10–15 V, causes a dissociation of Hf–O bonds and, therefore, enhances the local concentrations of the neutral or ionized shallow donor or acceptor levels, beyond the intrinsic oxygen vacancies of the as-deposited $HfO_2$ sublayer. Moreover, these vacancies have similar charge state parameters in the $HfO_2$ bandgap, as in the as-deposited $HfO_2$ film.[19–21] The theoretically predicted negative oxygen vacancy states $V_0^-$ and $V_0^{--}$ were verified[21] by optical and electrical measurements. They were also identified as the major charge trapping sites in the $HfO_2$ films.[23,25] The states with an energy of 0.3 to 0.36 eV and 0.5 eV corresponding to the shallow oxygen vacancies (single $V_0^-$ and double $V_0^{--}$, respectively) were considered in Ref. 20, 25, and 26 as being more active traps as compared to positive charged $V_0^+$ and $V_0^{++}$ oxygen vacancies that have deeper activation energies: 1.2 and 0.7 eV, respectively. Shallow traps with similar energy to the negative oxygen vacancies of 0.35 eV to 0.39 eV were extracted[14] from the current–voltage characteristics limited by the space charge mechanism of a photodetector based on diodes connected back-to-back with the structure similar to that used in the present study. In Ref. 27, for the first time, the distribution of traps in an $HfO_2$ layer was visualized, and their charge signs were identified at various applied biases on the gate electrode using high-resolution electron holography in an MIS structure, comprising a three-layer dielectric stack of $Al_2O_3/HfO_2/SiO_2$ deposited on p-Si. In contrast to those studies, it was found that not only negative charge traps presence in the $HfO_2$ layer, but also positive type traps that gather in the lower part of the $HfO_2$ film at the $SiO_2$ tunneling boundary are electrically active. The activity of positive charge traps was proven by the revelation of thin inversion (attracted electrons) at the Si interface, even without an appropriate applied gate bias.

An applied bias controls the formation of well-ordered chains of oxygen vacancies in local regions of the $HfO_2$ sublayer. The polarity of the applied voltage defines the formation of the continuously conductive filament or a break in the chain, which disturbs the carrier flow and the migration direction of oxygen vacancies.[28,29] When the top electrodes are biased negatively, positive vacancies migrate to the metallic electrode, while negative ones are gathered at the $SiO_2$ surface or vice versa.

The present structure differs from conventional resistive switching devices,[22,28,30] which are mainly metal–insulator–metal structures, by the use of metal electrodes on one side of the $HfO_2$ layer and the semiconductor that is isolated from the $HfO_2$ layer by the tunneling $SiO_2$ layer. Under applied bias, the conductive filament sites comprising traps of charged oxygen vacancies of different signs influence the depletion (inversion) or accumulation processes of carriers at the semiconductor interface.[27] On the other hand, using the tunneling process through an $SiO_2$ layer, it is possible to ensure the interaction between Si and oxygen vacancies collected at the $HfO_2/SiO_2$ interface or in the $HfO_2$ sublayer. Namely, by changing the polarity of the bias, carriers that are attracted on the Si surface can tunnel toward traps or vice versa, and the Si layer can accumulate carriers de-trapped from trap states in the $HfO_2$ layer. Therefore, a change in the concentration of carriers or their signs in the channel formed in the Si layer under different biases are expected. Different filament forming conditions are described schematically in Figs. 5(b)–5(d). The basic filamentation process is described in Fig. 5(b), while the arrangement of oxygen vacancies under negative and positive bias are illustrated in Figs. 5(c) and 5(d), respectively.

Application of a (vertical) negative electric field to gate or drain electrodes reduces the minority carrier density in the channel

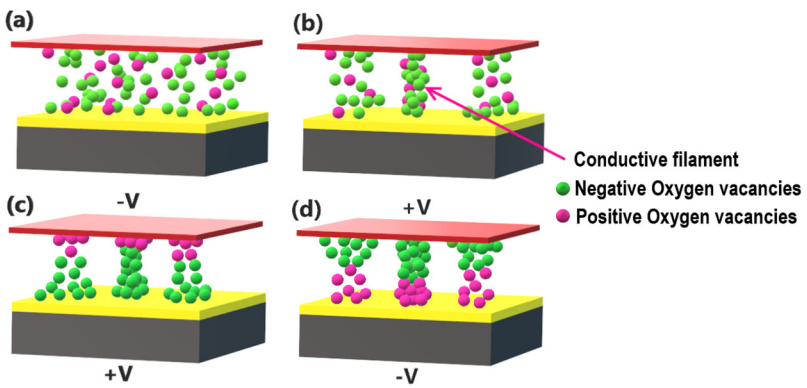


**FIG. 5.** Distribution of oxygen vacancies in the $HfO_2$ layer. (a) Random distribution within an as-deposited film. (b) Formation of the filament following voltage stress. (c) Distribution under negative bias. (d) Distribution under positive bias.

due to their direct tunneling through the thin $SiO_2$ into the $HfO_2$ and the consequent capture by negative traps accumulated at the $SiO_2$/ $HfO_2$ interface. In other words, electrons are injected from the gate to the positively charged sites and tunnel through the $SiO_2$ layer toward the inversion layer. An identical process takes place in the drain region. The result is a compensation of attracted minority carriers at the Si interface, which results in a decrease of the source to drain current that manifests itself as NDC as shown in Fig. 2(b) and its inset.

An increase in the absolute value of the negative gate voltage above 2 V causes a reduction in the drain current [see Fig. 2(c)], which can only be resulted in an increase in the probability of holes trapping from the inverted Si layer by migrated negative oxygen vacancies to the $HfO_2/SiO_2$ interface. Note that the ratio of the drain current at $V_G = -2$ V to $V_G = -5$ V is about 2 at any light intensity. A slight decrease in the absolute values in the drain current by about 1.05 times also observed with positive $V_G$ and negative $V_D$ bias values but is not caused by the capture of electrons accumulated at the Si–$SiO_2$ interface by positively charged oxygen vacancies that migrated with a positive gate voltage, but is a consequence of weak influence of the under the positive biased gate induced channel on negative drain current.

An effective capture of electrons and holes, which tunneled from an accumulated or an inverted Si interface layer through $SiO_2$ into traps in $HfO_2$, was demonstrated.[31] This process is known to induce space charge limited currents[32] in resistive switching devices and photodetectors that are based on $HfO_2$ or other metal oxides and make use of filamentation for the current path.[14,18,22,28,30]

In the inset of Fig. 3(b), in the gate voltage range of −5 V to −2 V and for negative drain voltages, ranging from −3 V to zero, the $\alpha_D - V_D$ curves exhibit a constant value of 2 and maxima. Regions with $\alpha_D = 2$ are a manifestation of Child's law due to the filling effect of traps, while the observed extrema are associated with the process of filling other level of mono-energetic traps in the filamentation regions. This is, therefore, unconditional evidence for the influence of filament sites on the behavior. Positive charges accumulated at the trap sites can also induce an internal Coulomb field, which may compensate for the external applied voltage and lead to the repulsion of minority carriers from the inversion layer. This leads to a further decrease in the source–drain current. The intensity of the trapping process is proportional to the negative gate voltage amplitude as is the current. The dark $I_D - V_D$ characteristics [shown in Fig. 2(a)] differ significantly from the characteristics under illumination. This is due to the low density of minority carriers that are almost completely captured by the $HfO_2$ layer, and therefore, their effect on the drain current is negligible.

The time constant governing the fast-transient component of the charge trapping/de-trapping processes in the $SiO_2/HfO_2$ stack is in the $\mu$s range,[26,33] which is too fast for any hysteresis to form; indeed, no hysteresis is observed in any measurement. As for the NDC, it was predicted[34] and demonstrated experimentally[35] for field effect transistors comprising a three terminal MIS system with Pt nanoparticles embedded in a gate dielectric stack. By changing the gate bias polarity, Pt nanoparticles captured holes or electrons, attracted at the Si/dielectric interface inducing NDC.

For a positive $V_D$, and negative gate potentials [see Figs. 2(a) and 2(b)], the $I_D - V_D$ curves differ. The characteristics do not depend on the absolute values of the gate voltage. Here, the electrons accumulated in the drain region prevail over the density of minority carriers in the gate–source region, and therefore, electrons determine the net current. The accumulated electrons in the drain area do not reduce as the drain voltage sweeps, in contrast to the minority carriers, which are the captured efficiency by the oxygen vacancies. Another confirmation of the fact that the current is limited by electrons is the asymmetric dark current [see Fig. 2(a)], which is lower, by more than one order of magnitude, under negative gate and drain biases compared to the positive drain bias. The difference between levels of positive and negative current branches, measured at positive drain and gate voltages, is negligible. These facts are the result of using n-type Si doped by phosphorus, where the density of holes is naturally lower than that of the electrons.

In the dark, a symmetrical characteristic is achieved only if the source and drain are two identical diodes connected back-to-back, since in this mode, only minority carriers limit the total current at both bias polarities as were observed in Ref. 14. Under illumination [see inset in Fig. 2(b)], the change of current sign from negative to positive (the inflection point) occurs at $V_D$ close to zero, independent of the negative gate voltage level and, hence, is consistent with conventional MOS FETs. However, in the dark, the characteristics behave differently [see inset in Fig. 2(a)], namely, the inflection point shifts to the positive values along the $V_D$ axis with a decrease in the absolute values of $V_G$. This will be discussed later in the paper when $I_D - V_D$ will be analyzed in the positive gate voltage mode.

For $V_G = 0$, the $I_D - V_D$ curves under all illumination levels behave as for $V_G = -1$ V, except that they are shifted to the positive voltage side and the saturation current reduces insignificantly at negative drain voltage. Consider the situation when, for any polarity of the drain bias, the gate is positively biased. In this case, the Si (under the gate electrode) is accumulated by electrons. However, the direction of migration of the negative and positive charged oxygen vacancies in the $HfO_2$ layer is opposite to the one under a negative gate bias [see Fig. 5(d)]. Namely, negative and positive oxygen vacancies migrate to the gate/$HfO_2$ and $SiO_2/HfO_2$ interfaces, respectively. Positive charged vacancies create an internal electric field, which makes possible the capture of part of the accumulated electrons at the silicon interface by traps, so they could potentially be partially compensated. However, similar to the positive drain voltage case, the ability of positive oxygen vacancies to capture accumulated electrons with the relevant drain and gate polarities is negligible compared with ability to capture holes from the inverted Si layer by negatively charged oxygen vacancies. This fact is confirmed by almost constant saturation current values measured at positive gate and drain voltages demonstrated by the $I_D - V_D$ curves shown in Figs. 2(a) and 2(b). At negative drain voltage, the drain current remains negative, but as the bias changes from negative to positive, the current sign does not change immediately. As the drain bias becomes positive, the current sign does not change immediately as is common in two terminal devices or field effect transistors. On the contrary, the inflection point shifts to larger positive drain voltages. Therefore, a positive $V_D$, which is larger than the applied $V_G$, is required to change the current sign.

The offset in changing the sign of the drain current is due to the presence of mobile traps with negative charge within the conductive filaments, which keep the drain current negative. A second

reason is the influence of the gate electrode on the direction of the current due to its asymmetric arrangement relative to other electrodes. For such an electrode configuration, the total current (in contrast to a conventional MISFET) is the algebraic sum of the current flowing directly between the source and the drain through the small gap between the electrodes and/or through a longer path, including the channel formed under the gate electrode. These two current paths act differently on the charge traps in the filament regions. In the small distance case, the influence of the gate is negligible, and the current branches are symmetric along the applied voltage axis, analogous to the $V_G = 0$ V case [see Fig. 2(b)] or two terminal back-to-back connected diodes with an equivalent structure.[14] Therefore, in the present case, minority carriers accumulated at the Si surface (reverse biased source and drain regions condition, causing the formation of the depletion region) define the current. At larger $V_G$, incorporation of the gate region becomes significant, and hence, the ranges of negative and positive current branches along the drain voltage axis change. A positive $V_D$ larger than $V_G$ is required to accumulate electrons at the Si surface in order to compensate the current due to the minority carrier flow through the small path region. The shift observed in the dark, even as the gate bias changed from −2 V to 0 V as well as the observation of the maxima [see small peaks in Fig. 3(a) at negative drain bias region], is also caused by those mobile traps.

Figures 3(c) and 4(d) clearly show the ability of precisely shifting the $I_D - V_D$ characteristics with illumination, in addition to the control by the gate voltage. The large expansion of $a_D - V_D$ with intensity, as shown in Fig. 4(d), is similar to that observed previously[14] for diodes having similar structures. The widening of the maxima and the decrease in their height [see Figs. 3(c) and 4(d)] result from that of conversion of mono-energetic levels to quasi-continuous states in the forbidden band of the $HfO_2$ film due to their interaction at high illumination intensities that have an effect that resembles the role of temperature.

The current saturation exhibiting $\alpha_D$ close to zero (see Fig. 3) is caused by a change in the capability of the electrode to supply excess carriers. In accordance with Refs. 36–39, when the current is sufficiently high or when the electric field at the metal–semiconductor interface gap is large, the real value of the effective contact concentration formed close to the semiconductor surface decreases, and therefore, the character of the current flow mechanism changes from trap to the Schottky barrier height limited. All these effects result in a non-monotonic α-V curve seen in Fig. 3. Enhancement due to illumination of local electric fields in MIS structures with ultrathin porous insulators, compared to uniform films, was discussed in Ref. 40, while a similar effect due to edge fringing fields in the vicinity of the electrodes was considered in Refs. 40–42. Thus, a comparable increase in the local electric field in the filament regions of the insulator stack is expected, corresponding to the saturation region of the current–voltage characteristics, where α is close to zero. Another interoperation of complete saturation, discussed in the literature, is associated with a large source to the drain series resistance.

### C. Photosensitivity

The photocurrent vs illumination power, measured at equal absolute values of the drain and gate voltages of 5 V, while applied bias polarities are opposite or identical is shown in Fig. 6. These characteristics that are plotted based on the data of $I_D - V_D$ measurements [see Figs. 2(c) and 2(d)] are always linear (see fitting dashed lines). The sign of the photocurrent is set by the polarity of the drain voltage. Curves measured at opposite bias polarities are almost symmetric relative to the photocurrent axis. However, at a negative voltage on both electrodes, the values of the photocurrent relative to that measured at $V_G > 0$ and $V_D < 0$ are reduced by a factor of 1.9 independent of illumination intensity. This is due to the negative differential conductivity effect.

The spectral response of the detectors is presented in Fig. 7 for a constant, $V_D = -5$ V, and three values of $V_G$ values, −5 V,

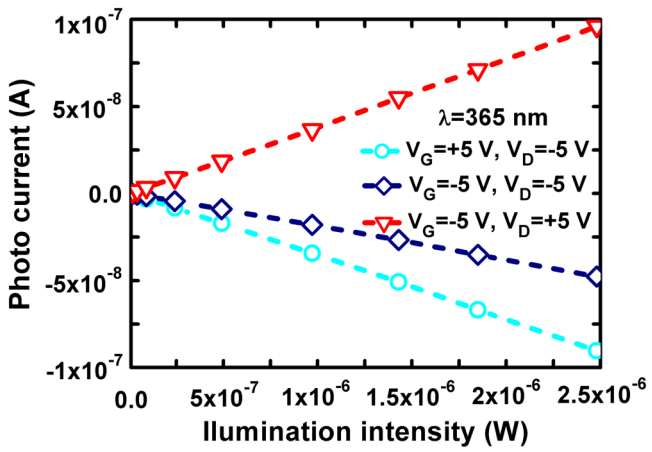


**FIG. 6.** Photocurrent vs illumination intensity, measured at different gate and drain voltages. Symbols are experimental results, while the dashed lines are a linear fit.

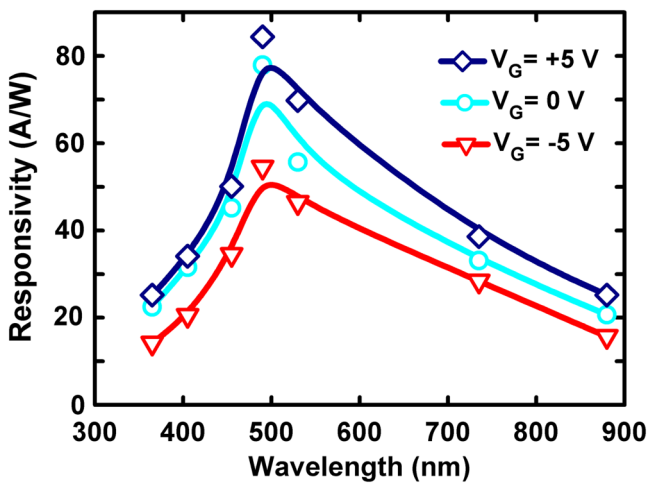


**FIG. 7.** Responsivity spectra of the device measured at different gate voltages and a power of $1.47 \times 10^{-7}$ W.

0 V, and +5 V. A total power of $1.47 \times 10^{-7}$ W was chosen for all wavelengths, and the ratio of the illuminating spot to optical area, roughly 698, was taken into consideration. The responsivity spectra, with a peak at 490 nm, are similar for all gate voltages. The maximum responsivity was 80–85 A/W, obtained at $V_G$ close to zero and +5 V. At $V_G = -5$ V, the peak responsivity was reduced. This is due to negative differential conductivity at negative gate and drain regions bias polarities. At 365 nm, responsivity is still high: 20–25 A/W. The high responsivities result from a photocurrent gain that was described in Ref. 14.

## IV. CONCLUSIONS

We reported here on a simple CMOS-compatible planar three-terminal device with electrodes formed from identical metal–insulator structures instead of Schottky metal-type source–drain electrodes and a metal–insulator gate system used in conventional Schottky field effect transistors. Silicon on an insulator, consisting of a high resistivity Si layer, was used as a substrate. Using simplified technological processes, a multi-functional device was demonstrated. The device has a very large optical response, so it can serve as an effective photodetector. The precise adjustment of the shift of the ID-VD characteristics along the axis of the drain voltage and the phenomenon of negative differential resistance, respectively, with positive and negative biases at the gate electrode, are established. These functions of the device originate from the existence of double-type trap states, which are formed during the filamentation process of a dielectric stack and the ability to regulate their charging/discharging with the applied bias polarities on the appropriate electrodes. A linear relationship between the gate voltage and the $I_D - V_D$ characteristic shift and, consequently, a current offset, a current saturation, and their ratio, as well as the slope controlled by the gate voltage, has a large potential as powerful tools in the development of universal devices and circuits. For example, the ability to tune the shift of the $I_D - V_D$ characteristics can be applied in logic gates and integrated circuits. The observed reconfigurable behavior of the device and high optical sensitivity over a wide wavelength range offer additional possible applications, which cannot be achieved by conventional MIS devices. Finally, the low level of saturation current in the dark and the ability to precisely control its value by adjusting the light intensity or the wavelength allow the developed device to be used in logic circuits requiring very low power dissipation.[43,44]

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