Sputter-Deposited Oxides for Interface Passivation of CdTe Photovoltaics

Jason M. Kephart, Anna Kindvall, Desiree Williams, Darius Kuciauskas, Pat Dippo, Amit Munshi, and W. S. Sampath

***Abstract*—Commercial CdTe PV modules have polycrystalline thin films deposited on glass, and devices made in this format have exceeded 22% efficiency. Devices made by the authors with a magnesium zinc oxide window layer and tellurium back contact have achieved efficiency over 18%, but these cells still suffer from an open-circuit voltage far below ideal values. Oxide passivation layers made by sputter deposition have the potential to increase voltage by reducing interface recombination. CdTe devices with these passivation layers were studied with photoluminescence (PL) emission spectroscopy and time-resolved photoluminescence (TRPL) to detect an increase in minority carrier lifetime. Because these oxide materials exhibit barriers to carrier collection, micropatterning was used to expose small point contacts while still allowing interface passivation. TRPL decay lifetimes have been greatly enhanced for thin polycrystalline absorber films with interface passivation. Device performance was measured and current collection was mapped spatially by light-beam-induced current.**

***Index Terms*—Cadmium compounds, photovoltaic cells, sputtering, thin films.**

I. Introduction

THE efficiency of CdTe photovoltaic cells and modules is rapidly improving, and efficiency gains are a key contributor to further reductions in levelized cost of energy [1]. Improvements in efficiency require reduction of defects in all aspects of the cell, including the front absorber interface, rear absorber interface, the "bulk" semiconductor, and grain boundaries. Historically, the most common front contact to polycrystalline CdTe has been cadmium sulfide, which is known to alloy with CdTe during processing. Total replacement of CdS with MZO window layer has enabled high-efficiency devices, and with a bandgap of 3.75 eV, MZO greatly reduces parasitic absorption in the front contact [2]. Photoluminescence (PL) and transmission electron microscopy indicate that this alloy does not detectably intermix with CdTe, and the abrupt interface, while suitable for relatively high-efficiency devices, remains far from ideal. The rear interface of CdTe has been proposed as a key limitation of device efficiency, and proper passivation of this interface could enable higher voltages [3], while other modeling suggests that both lifetime and doping in the CdTe must be increased for large improvements in the open-circuit voltage [4].

Strategies to passivate a semiconductor interface include positive conduction band offset, reduction of defect states at the interface, and fixed interface charge [5]. The use of a sputter-deposited oxide for CdTe interface passivation is attractive because of the ease and low cost with which it could be incorporated into commercial processes. However, chemical passivation of polycrystalline CdTe by another polycrystalline or amorphous material is difficult to predict. In this study, several oxides with high resistivity and high predicted conduction band offset with CdTe were grown by magnetron sputter deposition or ion-beam sputter deposition. Several candidate passivation layers were examined. Ta_2O_5, TiO_2, and SiO_2 have been successfully deposited at Colorado State University (CSU) via ion-beam sputter deposition and have been used in CdTe devices [6], [7]. MgO and high-magnesium MZO deposited by magnetron sputter deposition were selected for their higher predicted conduction band offset relative to the current MZO front contact, and Al_2O_3 was deposited both by magnetron sputter deposition and ion-beam sputter deposition.

To quickly test whether the oxides exhibited a significant passivation effect, PL emission intensity was used as a screening technique, and selected samples were measured using time-resolved photoluminescence (TRPL). One material, aluminum oxide, showed the strongest front interface passivation effect and was also tested at the rear interface. Aluminum oxide at the rear interface showed the highest lifetime and PL intensity improvement. Finally, a photolithography process was developed to micropattern these oxides and form MZO/CdTe front point contacts or CdTe/Te back contacts. Point contact CdTe solar cells were investigated via light-beam-induced current (LBIC) with 3-μm resolution, and current–voltage measurements were performed. These measurements allow the determination of lateral current flow toward point contacts to gain information about interface and bulk diffusion lengths. The use of a higher lifetime bulk absorber, $CdSe_xTe_{1-x}$, was investigated in combination with oxide interface passivation. This material and process optimization is discussed in detail in a concurrent publication [8].

Manuscript received June 9, 2017; revised November 5, 2017; accepted December 2, 2017. Date of publication January 18, 2018; date of current version February 16, 2018. This work was supported in part by the U.S. Department of Energy Photovoltaics R&D: Small Innovative Projects in Solar (DE-EE0007365) and in part by the U.S. Department of Energy, Office of Energy Efficiency and Renewable Energy, under Contract DE-AC36-08GO28308 (at NREL). *(Corresponding author: Jason M. Kephart.)*

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Digital Object Identifier 10.1109/JPHOTOV.2017.2787021

II. Methods

MZO layers were deposited with a composition of $x = 0.23$ on commercial 3.2-mm TEC 10 (Nippon sheet glass) substrates via RF sputter deposition of a mixed powder ceramic target. MgO, MZO ($x = 0.35$), and Al_2O_3 ceramic magnetron targets (Plasmaterials, Inc.) were used to deposit films via RF magnetron sputter deposition with an oxygen flow ratio of 3% O_2/Ar. Ta_2O_5, SiO_2, TiO_2, and Al_2O_3 were deposited via ion-beam sputter deposition in a Veeco spector system. These were sputtered reactively from elemental targets with partial oxygen background and oxygen assist. Transmission and reflection of films were measured, and all of the oxides were highly transparent over the solar spectrum except for TiO_2, which exhibited slight above-bandgap absorption. CdTe and $CdCl_2$ were deposited in the CSU advanced research deposition system, and completed with a 50-nm evaporated Te back contact and nickel paint. This process has been described previously [9], [10].

For oxide patterning via lift-off, a negative tone resist (Futurrex NR9-1000PY) was spin coated to a thickness of approximately 500 nm and patterned with a Suss MJB3 mask aligner. Bake, exposure, and development times were adjusted to produce the desired undercut profile and resist was removed using Futurrex RR5, followed by an oxygen plasma cleaning prior to CdTe deposition. For Al_2O_3 patterning via etching, a positive-tone resist was spin coated to a thickness of 2.1 μm and patterned. Al_2O_3 was etched in a tetramethylammonium hydroxide (TMAH) solution (Futurrex RD6) at 50 °C.

PL emission spectra were measured with the continuous-wave (cw) excitation at 520 nm, excitation power of 25 mW, and the excitation spot size of approximately 0.1 mm. Because of the difficulty in maintaining a stable calibration in PL, only measurements performed in the same session are compared. Low-temperature PL emission (LTPL) was measured with cw excitation at 632.8 nm, excitation power of 0.1 mW, and the excitation spot size of 0.2 mm. The LBIC was performed with a wavelength of 635 nm, and the system has been described previously [11]. TRPL decays were measured with excitation at 640 nm and the average excitation power of 0.1 mW (repetition rate 1.1 MHz, pulse length 0.3 ps, excitation beam diameter 0.3 mm). For TRPL, emission was collected with a 10-nm bandpass filter centered at 820 nm. Lifetimes were obtained from single-exponential fits to the tails of the TRPL decays (more detailed analysis of TRPL decay curves will be reported separately). From TCAD simulations, it was shown that such lifetimes are similar to the minority carrier lifetimes in CdTe solar cells [12].

III. Results and Discussion

A. Passivation

Polycrystalline CdTe solar cells have typically been made with a cadmium sulfide window layer, which results in sulfur alloying of CdTe; this is evident in PL signals that show both a shift in energy and alloy broadening of peaks [13]. MZO/CdTe devices were measured with LTPL, and do not exhibit alloy broadening. Fig. 1 shows the LTPL emission spectrum for a baseline MZO/CdTe device. The exciton emission peak at 1.59 eV is at the same energy as that for single crystal CdTe [14] and indicates the absence of alloying. The point defect emission with the maximum at approximately 1.55 eV is consistent with the Te-rich stoichiometry of the CdTe absorber [14]. Therefore, in the absence of absorber alloying, it is possible to analyze the absorber stoichiometry and the dominant point defects from the LTPL data. The third group of peaks in the 1.25–1.47 eV range display phonon replicas that indicate common origin of this emission. Emission of Y band with the zero-phonon line at 1.47 eV was attributed to the extended defects, such as glide dislocations [15]. A doublet peak is observed below the CdTe band-to-band peak, which is commonly seen in CdTe but has not been observed, to the authors' knowledge, in a functioning polycrystalline device. LTPL corroborates previous transmission electron microscopy (TEM) energy dispersive X-ray spectroscopy (EDS) measurements, in which Zn or Mg interdiffusion was not detectable. The MZO/CdTe interface is abrupt, and is likely defective because of the large lattice mismatch and polycrystallinity of MZO and CdTe. However, this device demonstrates that an abrupt oxide interface can make devices with V_{OC} greater than 850 mV, but further increases may require improved interface passivation.

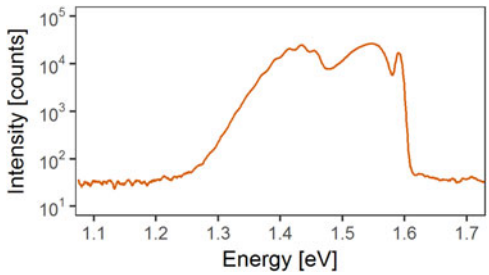

Fig. 1. LTPL indicates no alloy broadening in CdTe for an MZO/CdTe device. This is evident from the exciton emission peak at 1.59 eV. Lower energy bands are related to defects.

Candidate passivation layer materials were tested in the structure TEC 10/MZO (100 nm)/passivation layer (100 nm)/CdTe (5 μm)/Te (50 nm) with $CdCl_2$ passivation. TRPL was performed on all samples and compared with a baseline made without oxide passivation layer on the same day. SiO_2 and Al_2O_3 showed a passivation effect in PL and TRPL. TiO_2 and Ta_2O_5 caused a reduction in TRPL lifetime relative to MZO. MgO and high-magnesium MZO caused almost no change in TRPL decay lifetime. Growth of CdTe on SiO_2 was poor, and when the SiO_2 was patterned, CdTe only deposited on the exposed MZO point contacts. Al_2O_3 shows the strongest passivation effect and τ_2 in TRPL was improved from 2.8 to 5.4 ns (see Fig. 2), which suggests reduction of the interface recombination velocity by approximately a factor of two.

From the candidate materials, Al_2O_3 was selected as the most promising passivation material. For large device sets, PL emission intensity was used to compare interface passivation effect for process optimization. Over a large set of devices, PL emission intensity and TRPL show good qualitative agreement. A comparable passivation effect was seen for both magnetron and ion-beam-sputtered layers. In Fig. 3, the effect of thickness on PL emission intensity of ion-beam-sputtered layers is shown using the PL intensity of nine devices from each substrate. For

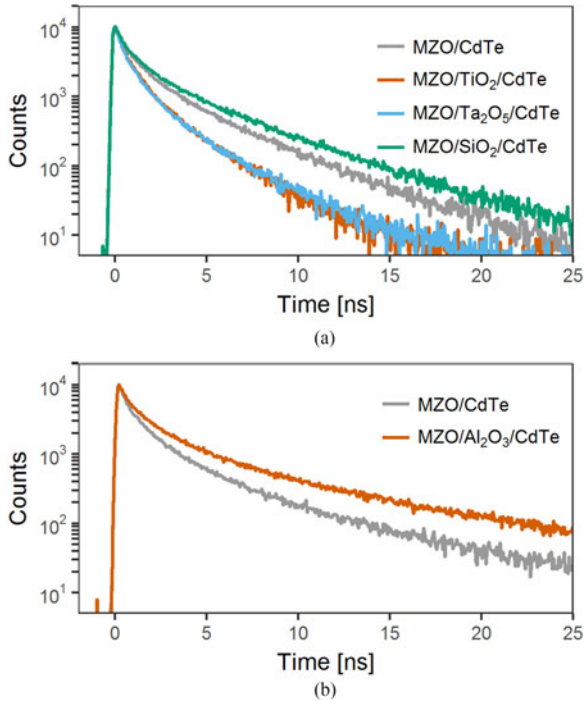

Fig. 2. TRPL data for the front interface passivation layers tested in device structures. (a) SiO_2 shows a slight improvement in TRPL decay lifetime, while others cause a decrease. (b) Al_2O_3 was the most effective passivation material tested.

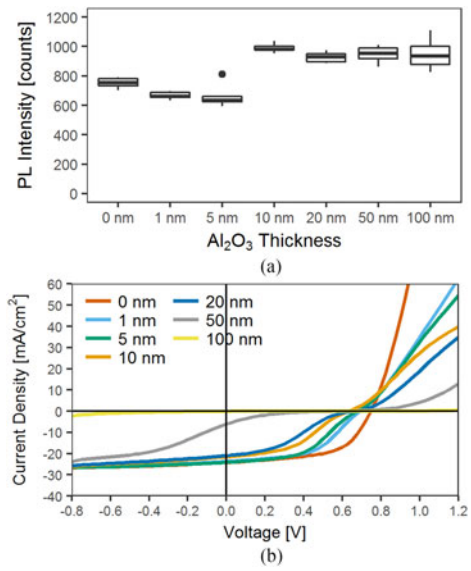

Fig. 3. (a) PL emission intensity of nine devices per substrate demonstrate that PL intensity was increased for devices with 10 nm or more of ion-beam-sputtered aluminum oxide. (b) *J–V* curves of one device at each thickness show an increasing *J–V* "kink" with increasing passivation layer thickness.

both processes, films less than 10-nm thick did not show significant passivation, while films 20 nm or thicker showed equivalent passivation [see Fig. 3(a)]. The current density–voltage curves in Fig. 3(b) clearly show a *J–V* "kink" because of a positive conduction band offset and a decline in V_{OC}.

Alumina layers were also deposited on the rear surface of CdTe; a standard thickness of 20 nm was used. When deposited

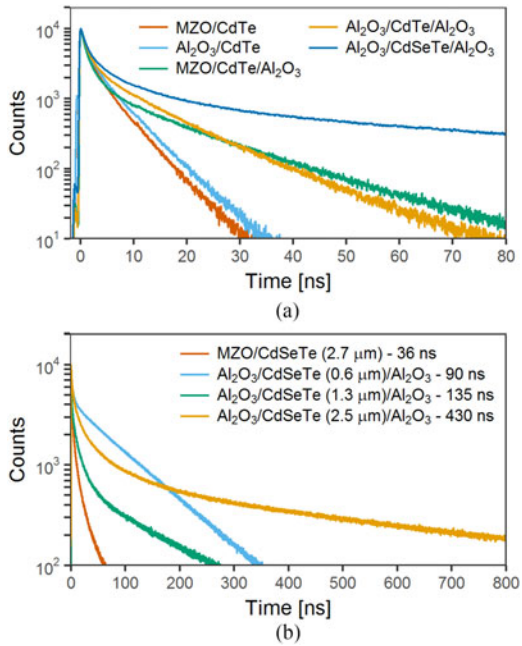

Fig. 4. (a) Aluminum oxide passivation has the strongest effect at the rear interface. With a high-lifetime CdSeTe absorber, a τ_2 of 100 ns was measured. (b) Double heterostructures made without TCO or window layer exhibit lifetimes up to 430 ns, and 90 ns with an absorber thickness of only 0.6 μm.

on the passivated CdTe, a decrease in PL intensity was observed. This was attributed to sputter damage from the alumina, and annealing at 400 °C did not improve the PL intensity above a control sample. When the $CdCl_2$ process is performed after alumina deposition, a several-fold increase in PL intensity is consistently seen. Device structures were deposited with alumina at the front, back, and both interfaces of a 2-μm absorber and measured with TRPL [see Fig. 4(a)]. From these results, the rear interface passivation has the greatest effect on decay lifetime. While front passivation repeatedly showed improvement for thicker absorbers, in this case there was little or no improvement. The linear decay τ_2 improved from 3 to 27 ns with back interface passivation. To achieve a higher lifetime, a $CdSe_xTe_{1-x}$ ($x = 0.2$) absorber with alumina passivation of both interfaces was also made. This material has been used in high-efficiency devices [16] and has been made at CSU using sublimation [8]. This structure exhibited a τ_2 of 100 ns. A second set of devices was prepared with uncoated glass rather than TEC 10 TCO-coated glass to make a true double-heterostructure with no n-type heteropartner. At the front, 100 nm of alumina was deposited to reduce potential out-diffusion from the glass, followed by CdSeTe absorbers of varying thickness, and 20 nm of alumina at the back interface. As a control, a similar structure was made with 100-nm MZO at the front and no oxide at the back interface. In this sample set, shown in Fig 4(b), a CdSeTe absorber with thickness only 0.6 μm has a τ_2 of 90 ns, while a thicker 2.5-μm absorber has a decay lifetime of 430 ns compared with 36 ns for the control sample. This is by far the highest decay lifetime of a polycrystalline CdTe or CdTe-alloy film known by the authors. Interface passivation appears to be critical to improvement of lifetime, and alumina is clearly effective for this purpose.

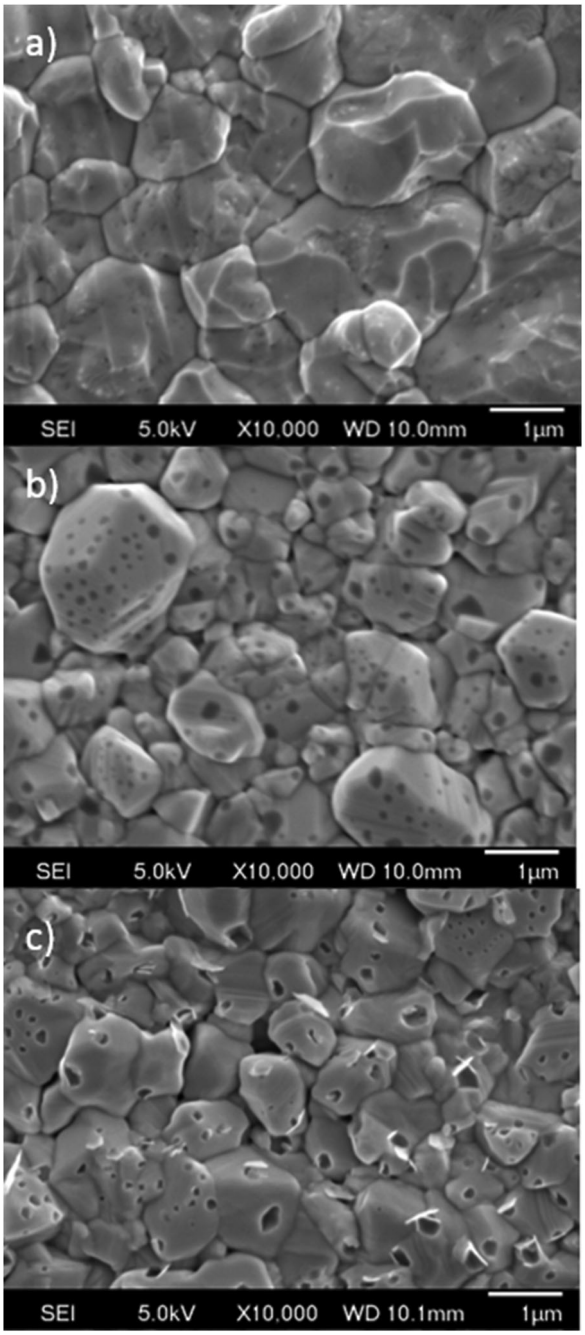

Fig. 5. SEM images for (a) $CdCl_2$-treated CdTe absorber, (b) $CdCl_2$-treated CdTe/Al_2O_3 heterostructure, and (c) $CdCl_2$-treated CdTe/Al_2O_3 heterostructure after etching to remove Al_2O_3.

The $CdCl_2$ process typically results in grain growth and recrystallization, producing a change in surface morphology. In Fig. 5(a), a $CdCl_2$-treated CdTe film with no alumina is shown. Fig. 5(b) shows a film that was $CdCl_2$-treated after alumina deposition; this film shows smaller angular facets, such as untreated CdTe, with many small spots. Scanning electron microscopy and energy dispersive X-ray spectroscopy (SEM-EDS) could not detect a deficiency of aluminum at these spots or any holes in the alumina coverage. When the alumina film is etched from this sample using TMAH [see Fig. 5(c)], the spots are clearly voids that are created under the thin alumina "skin."

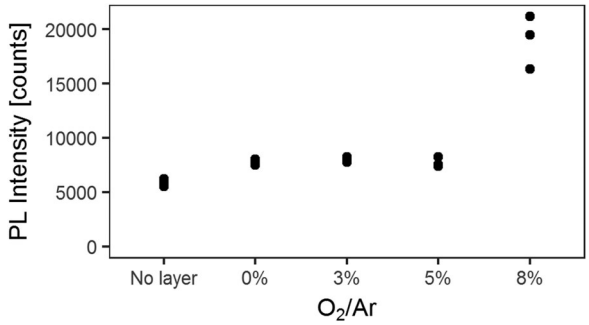

Fig. 6. PL emission intensity for samples with 20-nm-thick alumina layers at the back CdTe interface. The increase in the PL emission intensity is the highest when O_2/Ar flow was at 8%.

Further investigation is needed to understand the changes in the $CdCl_2$ treatment caused by the alumina and their effects on grain size, grain boundaries, and diffusion into and out of the CdTe film.

Effective interface passivation via field effect is well documented in crystalline silicon [5] and has been reported for a p-type Cu(In,Ga)Se_2 [17] and CZTS [18]. Alumina is one of the few materials that is capable of exhibiting negative fixed charge [19]. Negatively charged defects in the oxide repel minority electrons and reduce effective surface recombination velocity in addition to potential chemical passivation (reduction of defects at the interface). Fixed charge is a property of defects within a few nanometers of the interface, and this explains why layers thicker than 10–20 nm do not exhibit greater passivation. This also makes passivation effective for a variety of p-type semiconductors. Negative charge has been attributed to aluminum vacancies and/or oxygen interstitials in the alumina [20], and sputter-deposited alumina exhibits a large range of stoichiometry depending on the background gas [21]. To test the effect of stoichiometry on passivation, 20-nm layers of alumina were deposited by magnetron sputtering from an alumina target using a varying amount of oxygen added to the argon gas. Deposited in pure argon, the alumina is gray and with increasing oxygen flow becomes fully transparent with a declining deposition rate that was calibrated for each setpoint. Fig. 6 shows that an O_2/Ar flow of 8% produced a much higher passivation effect than lower oxygen depositions.

B. Patterning

In order to achieve passivation of the interface and still collect current from the cell, the distance a carrier must diffuse to reach a point contact should be on the order of the diffusion length or less. Assuming a mobility on the order of 100 $cm^2/V{\cdot}s$, a lifetime of 100 ns corresponds to a diffusion length of 5 μm. The point contact pattern used is a hexagonally arranged set of points with the parameters D for the point diameter and L, the point spacing. A photolithography mask was made with 32 device locations over an approximately 75 $\times$ 75 mm^2 area. These devices have a range of point sizes (1.5, 3, 6, and 10 μm) and L was chosen to allow the fractional area of point contacts to vary from 1% to 50%. The smaller the point size, the better the combination of high passivation layer coverage and short diffusion length. The 3-μm holes were the smallest that could be repeatably patterned,

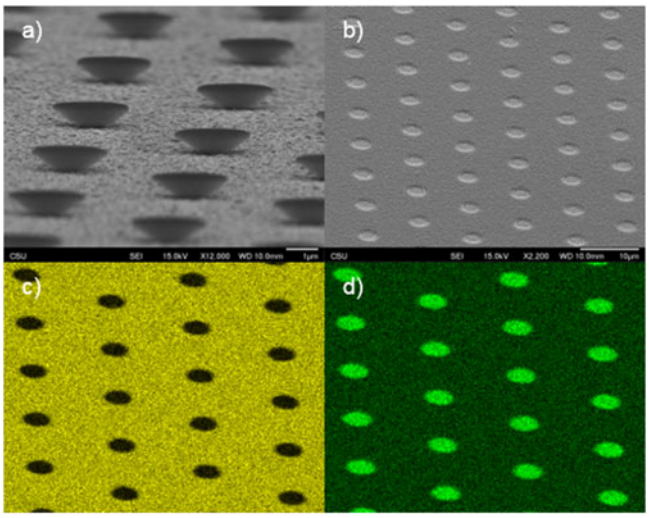

Fig. 7. (a) Patterning was demonstrated using negative resist with an undercut profile. (b) Al_2O_3 was patterned on top of MZO with 2-μm point size. (c) Al K and (d) Zn L EDS maps clearly show the desired point contacts.

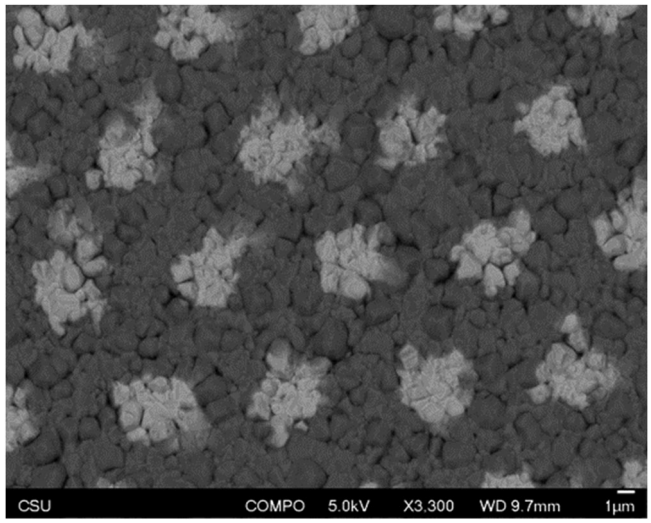

Fig. 8. Alumina was patterned on the back of CdTe with photolithography and a TMAH etching process. The backscattered electron image shows elemental contrast between CdTe (light) and alumina (dark).

but their actual size could be varied slightly by the lithography process parameters.

Patterning was successfully demonstrated on several oxide materials using a lift-off process. Fig. 7 shows SEM-EDS images of 2-μm point contacts with 10-μm spacing in an alumina film on TEC 10/MZO. Fig. 7(a) shows negative-tone photoresist with a pronounced undercut profile. Oxides were deposited on this photoresist, followed by lift-off using a resist remover. This process produces a clearly delineated Al_2O_3 layer over MZO [see Fig. 7(b)]. Al K [see Fig. 7(c)] and Zn L [see Fig. 7(d)] EDS signals demonstrate successful patterning of Al_2O_3 on MZO. Lift-off was also demonstrated with SiO_2, MgO, and Ta_2O_5. For these materials, any etchant which could remove them would more rapidly etch the underlying MZO layer.

For aluminum oxide, an alternative method of patterning using an etching process was developed. This process is specific to aluminum oxide, but has a number of advantages: It has reduced potential for interface contamination compared with the lift-off process, can be used on the front or back interface, and does not require a precise resist profile. ZnO is easily etched in acid, but much more slowly etched by alkaline solutions, and TMAH can be used to selectively etch alumina on ZnO [22]. Aluminum oxide deposited on the top of MZO was etched in a TMAH solution and did not significantly etch the MZO, even at 400% time to clear. This process was later used to pattern alumina on the back of CdTe, and does not significantly etch the CdTe either. Fig. 8 shows the alumina layer selectively etched at the back; a backscattered electron image shows the elemental contrast between the CdTe (light) and alumina (dark). Photolithography on the rough, reflective surface of CdTe produces edges that are not smooth, but the etching process repeatably patterns large areas with 3-μm spot size.

C. Devices With Patterned Oxides

The key challenges of implementing a device with patterned oxide passivation are: demonstrating effective passivation; achieving a long enough diffusion length to collect carriers; making a sufficiently ohmic back contact such that low series resistance can be achieved with reduced contact area; and higher doping throughout the absorber or near the rear interface of the absorber (considered critical to increasing voltage). So far, the lifetimes achieved in this paper would result in a diffusion length of several micrometers assuming mobilities on the order of 100 $cm^2/V{\cdot}s$, and the passivation effect is strong. No consistent improvement has been seen so far in the open-circuit voltage, and for front-patterned devices, the V_{OC} declines with increasing alumina coverage. This decline may be because of the negative charge of the passivation layer, which would tend to reduce the built-in field at the front contact and enhance it at the back contact. High lifetimes are critical to full current collection, and this effect can be seen by comparing devices with patterned alumina at the front interface and either a CdTe or a CdSeTe/CdTe graded absorber. Both sets of devices (see Fig. 9) show reduced current collection as 3-μm point contacts are spaced farther apart. The higher lifetime CdSeTe/CdTe device shows better current collection into forward bias.

LBIC is a technique in which a focused laser is rastered across a sample and the photocurrent is mapped spatially. For patterned contacts, this technique can compare collection away from the point contacts in different devices. In Fig. 10, LBIC was measured on the devices in Fig. 9 with 10-μm hole spacing and both absorbers. A bias of 0.4 V was applied to the devices to reduce the electrical field. When normalized to their maximum photocurrent values, the CdTe device shows a significant drop in collection away from the hole contacts, while the CdSeTe device has much more uniform collection. Again, these results indicate that high lifetime and diffusion length achieved by bulk and interface passivation are critical to effective current collection.

TRPL and PL results indicate that alumina passivation of the rear interface has a stronger impact on lifetime than passivation of the front interface. Additionally, negative interface charge tends to repel electrons, which is more compatible with the

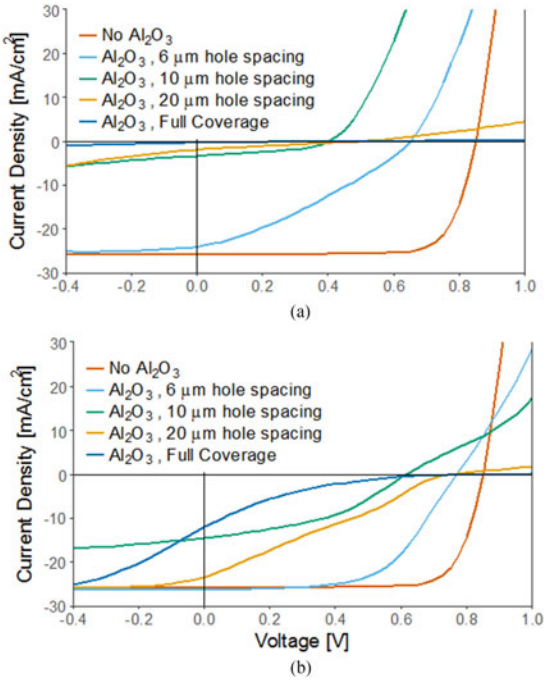

Fig. 9. *J–V* Curves for devices with patterned alumina at the front interface and (a) a CdTe absorber or (b) a CdSeTe/CdTe graded absorber. Increasing alumina coverage results in reduced V_{OC} and a barrier to current collection in forward bias. The CdSeTe device shows improved current collection in forward bias.

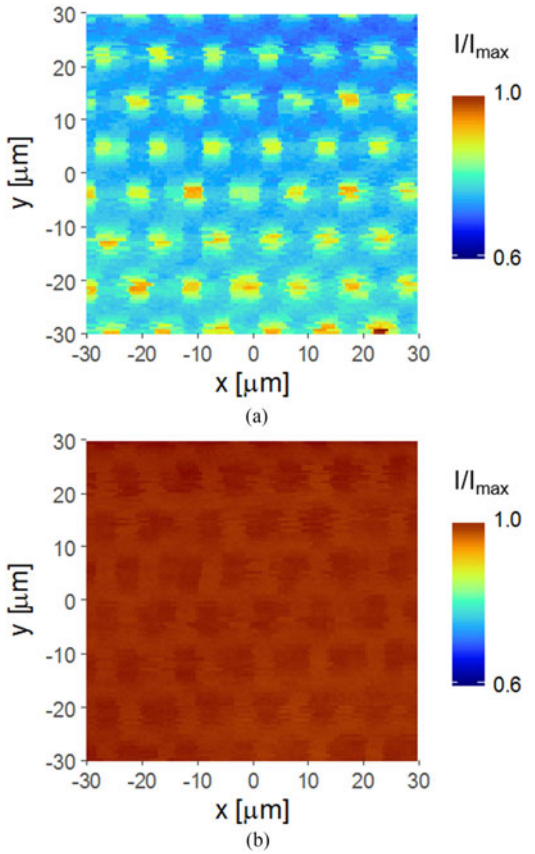

Fig. 10. LBIC map shows spatial current collection with a forward bias of 0.4 V for devices with patterned alumina at the front interface and (a) a CdTe absorber or (b) a CdSeTe/CdTe graded absorber. Point contact diameter is approximately 3 μm and spacing is 10 μm.

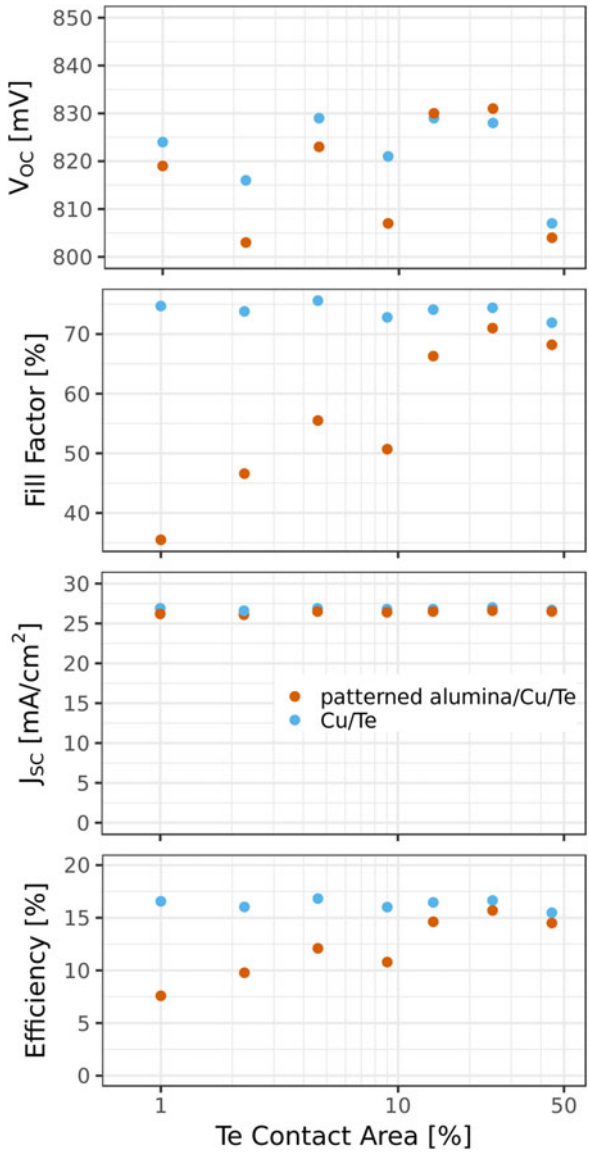

Fig. 11. Device efficiency parameters are shown for devices with alumina passivation and copper doping as a function of contact spacing for 3-μm point contacts. Baseline devices with no alumina are shown at matching substrate positions for reference (all devices have 100% Te contact area).

rear interface where holes are collected. Devices with patterned alumina, as shown in Fig. 8, have been made using graded CdSeTe/CdTe absorbers. A baseline device was made according to a high-efficiency baseline process; these devices exhibit V_{OC} near 820 mV and fill factor near 75%. This device is shown for comparison to other devices in Fig. 11. A device was made with patterned alumina with process conditions that were otherwise the same (devices with 3-μm point contacts are shown). The patterned devices have equivalent V_{OC} to the baseline device. Fill factor and short-circuit current remain high until the point contact area drops below 10%. At this point, the series resistance increases. These results indicate that the improved lifetime from back interface passivation is not sufficient in this device structure to achieve a significantly improved V_{OC}. A major reason for this may be the importance of doping in the absorber or near the back

interface of the absorber to achieve higher V_{OC} by increasing the built-in potential. To maintain high fill factor, a lower resistance back contact and/or finer patterning is needed. A combination of high lifetime, optimal doping, and more ohmic back contact will enable larger V_{OC} gains and high fill factor even with reduced point contact area.

IV. Conclusion

The ability of sputter-deposited oxide passivation layers to improve lifetime in polycrystalline CdTe and CdSeTe has been demonstrated using Al_2O_3. This material showed the best passivation effect of six candidate materials, demonstrating a dramatic increase in PL emission intensity and TRPL lifetime. Double heterostructures of CdSeTe passivated with Al_2O_3 showed the highest TRPL decay lifetimes reported to date for polycrystalline CdTe-based thin films on glass, indicating that the lifetime of polycrystalline CdTe-based thin films is not a fundamental obstacle to further efficiency improvements. To allow the photocurrent collection using passivation materials with high conduction band offset, these passivation layers have been patterned using either a lift-off or etching process. The high lifetime indicates that micrometer-scale patterning is sufficiently small to collect carriers, but devices still suffer from reduced fill factor, and no increase in open-circuit voltage or device efficiency has been observed. Further effort is needed to understand how increased lifetime can produce higher efficiency. Specifically, reductions in contact resistance and increased absorber doping are necessary to realize open-circuit voltage and efficiency improvements.

Acknowledgment

J. M. Kephart would like to thank D. Swanson for initial TRPL measurements, J. Sites and A. Huss for LBIC and PL assistance under the U.S. Department of Energy Contract DE-EE-0007543, and G. Xiong and C. Lee of First Solar, Inc., for helpful discussions and characterization. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for United States Government purposes.

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Authors' photographs and biographies not available at the time of publication.