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Electrons on dislocations

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The electrical behaviour of only a few dislocations was analysed. Such small numbers of defined dislocations were produced by hydrophobic semiconductor wafer direct bonding. The dislocation networks were placed in the channel of SOI MOSFETs where the source and drain regions of these devices act as contacts. Varying the channel width allows one to control the number of dislocations measured. Analyses of nMOSFETs proved an increase of the drain current caused by dislocations by more than one order of magnitude, while a decrease of the current is obtained for pMOSFETs. This indicates that electrons are present on the dislocation core in p-type material. The concentration of electrons on dislocations was estimated to be about 200 electrons per micrometer dislocation length, corresponding to a distance of about 5 nm between free electrons. This distance agrees with the space between Coulomb islands proved by low-temperature measurements. The investigations refer to a metallic-like conductance along dislocations caused by a two-dimensional carrier confinement.

1 Introduction The knowledge about the type, concentration, and localization of carriers (electrons, holes) on dislocations is an important issue in the further characterization of this type of crystal defects. This is especially true for dislocations in silicon as the most important material for microelectronics. The structure of the core of different dislocations and their electronic properties were described in numerous publications. A current review about the core structure of primary, non-dissociated screw and 60° dislocations was given, for instance, in [1], whereas different models of the structure and concepts of the electronic properties of 30° and 90° partial dislocations exist (e.g. [2–4]). A number of dislocation related levels in the band gap was suggested. In addition, the core structure of both partial dislocations is assumed to be negatively charged in n-type silicon, while reconstructed cores of partial dislocations in p-type and intrinsic material are neutral [4]. This interpretation is in contrast to experimental results, which among others, deduced simultaneously both acceptor and donor properties [5], or negatively charged dislocations in p-type material [6]. Also a number of deep states have been obtained for dislocations in n- and p-type material. The crucial reason for the opposed results might be the analyses of individual dislocations in the case of computer simulations while a large number of dislocations is required for experimental measurements. The characterization of a large number of dislocations, however, means also the simultaneous registration of effects caused by interactions between dislocations as well as between dislocations and point defects. A defined comparison between theoretical models and experiments is therefore possible if only a few or, in the ideal case, individual dislocations are measured. The present paper deals with the analysis of a small number of well-defined dislocations. Their electrical properties were measured directly by placing them into the channel of common electronic devices.

2 Experimental Semiconductor wafer direct bonding allows the reproducible realization of defined two-dimensional dislocation networks. The method is described elsewhere [7]. Varying the twist and tilt angles allow varying the dislocation distance within the network. SOI wafers (orientation {100}, device layer thickness about 25 nm or 40 nm (p- type, resistivity 13.5–22.5 Ωcm), buried oxide (BOX) layer thickness 60 nm) were used for hydrophobic wafer bonding resulting in the formation of Σ1 grain boun-

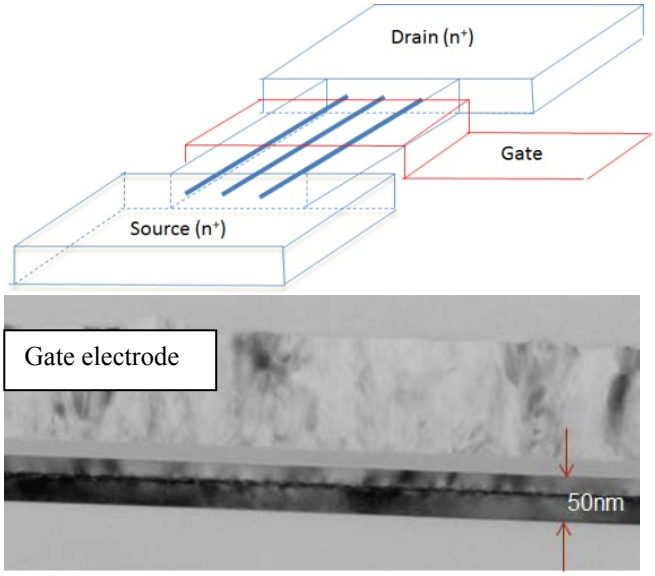

Figure 1 Scheme of an nMOSFET structure (top). Dislocations are oriented parallel to the <110> channel direction. Source and drain act as contacts. The TEM image (bottom) shows a part of the channel region below the gate with dislocations inside the channel (thickness 50 nm).

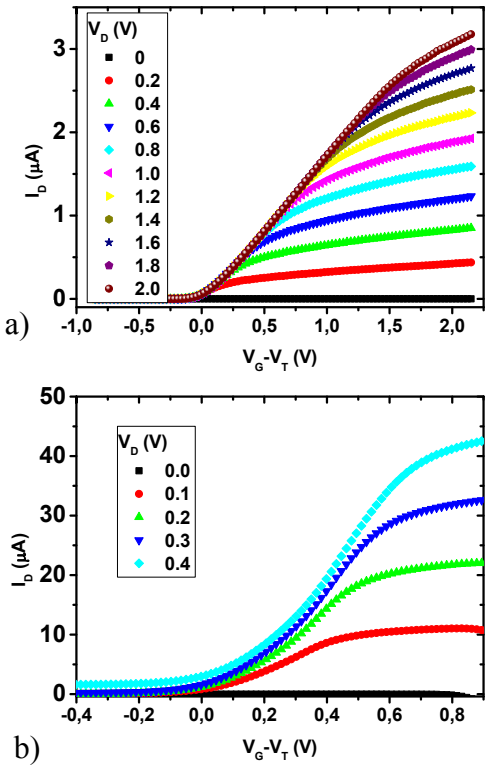

Figure 2 Drain current (I_D) vs. gate voltage (V_G) of nMOSFETs without (a) and with dislocation (b). V_G is represented as difference V_G–V_T with V_T as the threshold voltage. The channel length and width, respectively, for both devices are 1 µm.

daries. They consist of square-like meshes of screw dislocations, which, depending on the tilt angle, are superposed by a mesh of 60° dislocations. After thinning down the bonded wafers to a final thickness of 50 nm or 80 nm, n-channel as well as p-channel metal-oxide-semiconductor field-effect transistors (nMOSFETs, pMOSFETs) were prepared on such substrates (diameter 150 mm) using a standard CMOS process. Details of the process were described in [8]. The MOSFET channels were oriented parallel to both <110> directions, i.e. parallel to the dislocation lines (Fig. 1). In order to analyse the effect of different numbers of dislocations, the channel width (W) was varied from 1 µm to 10 µm. The channel length (L), however, was fixed to 1 µm. Devices prepared on SOI wafers of the same thickness of the device layer and doping level but without dislocation networks act as reference. All device measurements were carried out at room temperature and at low temperatures (T = 5 K). The structure of the dislocation network and analyses of the different dislocation types were verified by transmission electron microscopy (TEM).

3 Characteristics of MOSFETs

3.1 Analyses of nMOSFETs Previous investigations proved that dislocations form channels of higher conductance resulting in higher carrier concentrations in the

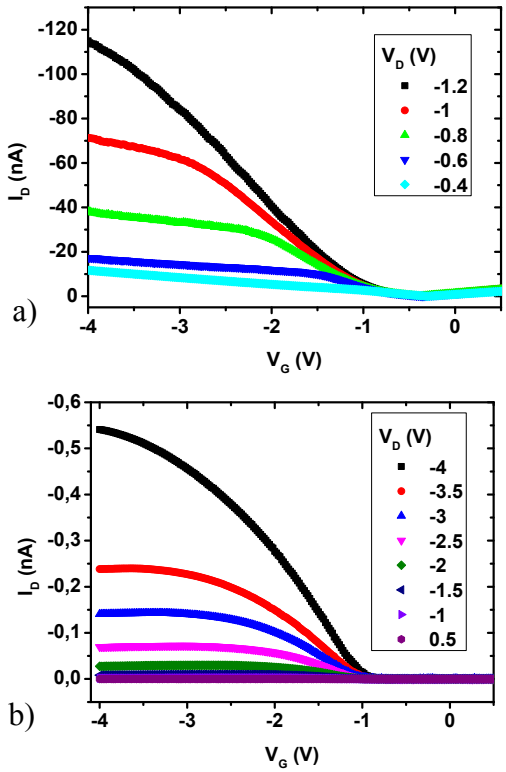

Figure 3 I_D–V_G characteristics of pMOSFETs without (a) and with dislocation (b). The channel length and width, respectively, for both devices are 1 µm. Note the different scale of I_D in comparison to Fig. 1.

silicon layer [9]. This is confirmed by analyses of nMOSFETs. Figure 2 shows the drain current (I_D) vs. gate voltage (V_G) characteristics of MOSFETS without and with dislocations in the channel. For a MOSFET without dislocations (reference sample, Fig. 2a) I_D is about 3 µA at drain voltages $V_D = V_G = 2$ V. The devices are characterized by a subthreshold slope of $S = 100$ mV/decade and a threshold voltage $V_T = -150$ mV. On the other hand, measurements of MOSFETs with dislocations result in values of I_D more than one order of magnitude higher compared to the reference even at significantly lower drain and gate voltages (Fig. 2b). Similar results were also obtained by other authors [10] and are ascribed to the presence of dislocations. The analysis of device data clearly proved that the number of dislocations in the channel characteristically controls all device parameters. Decreasing the number of dislocations in the channel causes an unexpected increase of I_D [8]. The extrapolation of data obtained from MOSFETs having as low as six up to a few hundred dislocations in the channel would expect the highest drain current even if only one dislocation exists in the channel. Besides I_D also V_T and S depend on the number of dislocations in the channel. The threshold voltage V_T increases as the number of dislocations decreases. This is caused by a decreasing effective channel length with decreasing dislocation number. Furthermore, the subthreshold slope S increases as the dislocation density increases. The increase of S is generally interpreted as a thickness effect of the device layer for short channel SOI MOSFETs and is caused by an inhomogeneous electron concentration in the layer [8].

Detailed analyses of device parameters prepared on substrates with different dislocation networks revealed a strong dependence of I_D on the dislocation type. If only screw dislocations are present in the transistor channel, the highest drain currents are measured, while against lower values of I_D result in the presence of 60° dislocations. This allows the conclusion that more carriers (electrons in the case of nMOSFETs) are transported via screw dislocations than via 60° dislocations.

3.2 Analyses of pMOSFETs Figure 3 shows the I_D–V_G characteristics of pMOSFETs without and with dislocations in the channel. The drain current measured for such devices without dislocations (reference) is about one order of magnitude lower than for equivalent nMOSFETs (Fig. 3a). This is mainly caused by the lower mobility of holes compared to that of electrons in silicon. A further reduction of I_D by a factor of 100 or more is observed if dislocations are present in the channel (Fig. 3b). The measured values of I_D are also lower by a factor of about 10^5 compared to data of equivalent nMOSFETs (Fig. 1b). In addition, also higher drain and gate voltages are required for measurements of pMOSFETs. This suggests the suppression of the transport of holes via dislocations in p-type material. It can be assumed that electrons existing on dislocations (resulting in the increase of I_D for nMOSFETs) lead to a compensation of injected holes in the case of pMOSFETs.

Measurements on numerous devices refer also to a different behaviour of pMOSFETs prepared on varying substrates containing dislocation networks of different dislocation types. Assuming the same conditions ($V_G = -3.5$ V, $V_D = -3$ V) a drain current of $I_D = -2$ nA is measured if only 60° dislocations are present, while only $I_D = -0.5$ nA is determined if screw dislocations are dominantely present in the channel.

4 Charges on dislocations The application of MOSFETs allows not only the advantageous measurement of the electronic properties of a few dislocations but also a more detailed interpretation of the data by means of device physical principles. For instance, commercially available device simulation programs make it possible to calculate the current-voltage characteristics of MOSFETs enabling conclusions about the physical reasons behind. The ATHENA/ATLAS simulation package (Silvaco) was used in the present study. Because dislocations represent conductive channels, they are assumed as thin n-type layers embedded in the 80 nm thick channel. The I_D-V_D- and I_D-V_G characteristics are calculated and compared with the experimentally measured ones by fitting the donor concentration in this thin layer. Figure 4 shows an example of the simulated I_D–V_G characteristics for nMOSFETs with dislocations in the channel. It was shown that a donor concentration of 3×10^{18} cm^{-3} in the thin layer results in an increase of I_D by one order of magnitude as proved by experimental measurements. This is caused, as Fig. 5 shows, by the formation of a conductive channel along the thin (dislocation) layer already at very low drain and gate voltages. The reference transistor without dislocations, however, is characterized by an electron concentration more than one order of magnitude lower (Fig. 5a). A conductive channel is not formed under these conditions. Since the donor concentration is equal the electron concentration, the number of electrons in the 2 nm thick layer is estimated to be 6000 for $W = L = 1$ µm. Furthermore, the behaviour of the subtreshold slope refers to an inhomogeneous electron concentration [8] which suggests that all electrons are bounded to dislocations. TEM investigations revealed that there are 30 dislocations in the channel for this specific case, which means about 200 electrons per micrometer dislocation length. This corresponds to the maximum number of electrons on a dislocation [11]. Assuming a homogeneous distribution along the dislocation line, the distance between free electrons on the dislocation core is about 5 nm. There is no evidence up to now about the locations of electrons on the dislocation core. The distance of about 5 nm is significantly smaller than the distance of dislocation nodes in the network (about 30 nm in this case) and means that electrons are located on straight dislocation segments. Moreover, kinks on dislocations could be a promising candidate. But only narrow kink-kink distances of about $d \cong 2b \cong 1.6$ nm are stable. Here b is the length of the Burgers vector. Larger kink-kink distances up to $d \cong 10b$ were calculated but it was shown that such wide kinks are intermediate states only. Therefore metallic-conduction along dislocation

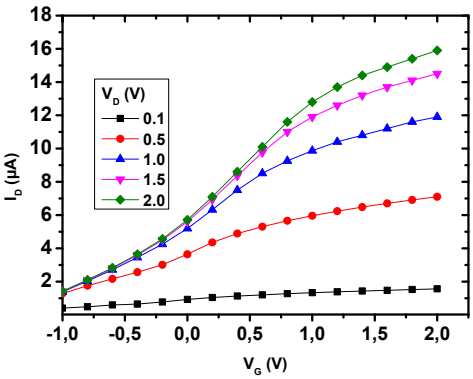

Figure 4 Simulated I_D–V_G characteristics of nMOSFETs with dislocations. Dislocations are assumed as a thin n-doped layer (2 nm thick) having a dopant concentration of $5x10^{17}$ cm^{-3}. The channel length and width, respectively, are 1 µm.

lines in the p-type material is assumed in accordance with [12]. It is caused by a two-dimensional carrier confinement along dislocations. The assumption of a metallic-like behaviour may explain also the occurrence of Coulomb blockades proved by low-temperature measurements at T = 5 K. These investigations showed a staircase-like behaviour of the conductance *G* as a function of V_G if screw dislocations are present, while periodic oscillations of *G* are obtained for mixed dislocations resulting from the reaction of screw with 60° dislocation [13]. The distances of the Coulomb islands were calculated to be about 4 nm for screw dislocations and about 8 nm for mixed dislocations. These values are in good agreement with distances of electrons of 5 nm estimated from simulations.

5 Conclusions The embedding of two-dimensional configurations of well-defined numbers and types of dislocations into channels of MOSFETs is eminently suited to analyse the electrical properties of only a few or individual dislocations. Measurements of the characteristics of nMOSFETs proved an increase of the drain current by more than one order of magnitude while a decrease of I_D is found for pMOSFETs. This indicates that electrons are present on the core of dislocations in p-type material. Device simulations revealed about 200 electrons per micrometer dislocation length corresponding to a distance between free electrons of about 5 nm. The investigations refer to a metallic-like conductance along the dislocations caused by a two-dimensional carrier confinement.

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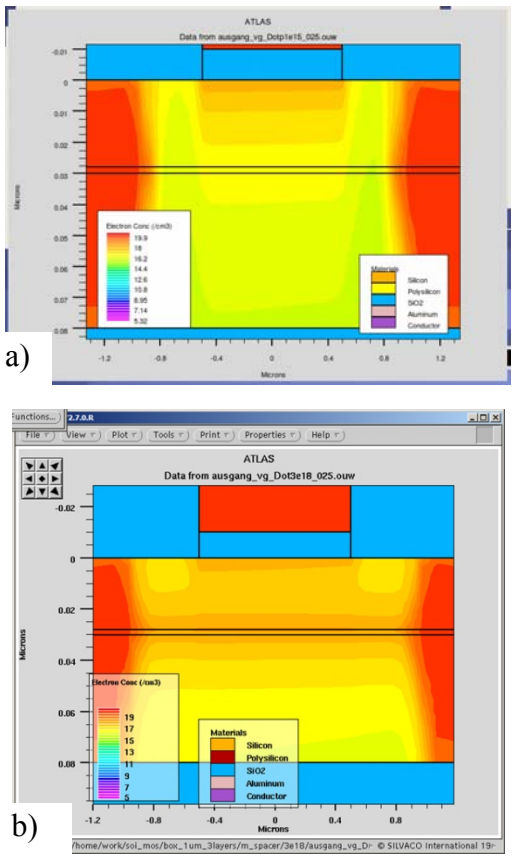

Figure 5 Simulated two-dimensional electron density in the channel of nMOSFETs without (a) and with dislocation (b) at $V_G = V_D = 0.25$ V. Dislocations are assumed as a thin n-doped layer (2 nm thick) having a dopant concentration of $3x10^{18}$ cm^{-3}. The parameters for simulation are $W = L = 1$ µm, a 80 nm thick device layer, and a 10 nm thick gate oxide. Red colour indicates the highest ($\geq 10^{19}$ cm^{-3}) and green colour the lowest electron concentration ($\leq 10^{15}$ cm^{-3}).

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