Plasma-etched, silicon nanowire, radial junction photovoltaic device

Plasma-etched, silicon nanowire, radial junction photovoltaic device

Athanasios Smyrnakis[1], Panagiotis Dimitrakis[1], Evangelos Gogolides[1]

[1] *Institute of Nanoscience and Nanotechnology, NCSR "Demokritos", Ag. Paraskevi 15341, Greece*

Keywords: silicon nanowires, photovoltaic device, radial p-n junction, spin-on dopants, cryogenic plasma etching, colloidal lithography

Abstract

A photovoltaic device based on radial p^+n junction, plasma-etched silicon nanowires (SiNWs) is demonstrated. Cryogenic Si plasma etching after colloidal lithography is employed for the fabrication of ordered, high aspect ratio and perpendicular to the substrate nanowires. Radial junction is established by boron rapid thermal diffusion from Spin-On Dopants (SOD) solution. We study the effect of SOD annealing process conditions and show that shallow p^+n junctions with depth of a few tens of nanometers and high dopant concentration are formed. Structural and electrical study of the final device is performed by current-voltage characterization under illumination, and compared to a planar Si photovoltaic device with similar p^+n junction characteristics. Short-circuit current density (J_{sc}) of 12.3 mA/cm^2, open-circuit voltage (V_{oc}) of 430 mV, fill factor (FF) of 0.64 and power conversion efficiency of 3.69% were obtained for the radial SiNW photovoltaic devices, significantly improved compared to the related figures for the corresponding planar device being 8.13 mA/cm^2, 384 mV, 0.72 and 2.24%, respectively.

1 Introduction

Silicon nanowires (SiNWs) show exceptional structural, mechanical, electrical and optical properties [1-6], and have been implemented in various applications, such as solar cells [7-9], photodetectors [10-12], field effect transistors [13, 14], biosensors and bioanalysis [15-17], catalysis [18, 19] and more. Regarding solar energy conversion, SiNWs can offer several advances in the current leading silicon photovoltaic industry. The advantages of SiNWs for photovoltaic devices involve, in brief, the strong optical absorption enhancement compared to planar and thin film approaches with antireflective coatings [20]; the short carrier collection length [21]; and the fact that they can be easily fabricated with controlled and high quality electrical characteristics. Consequently, in the last decade, an increasing number of review papers appeared in the literature regarding the integration of SiNWs in photovoltaic devices [7-9, 20, 22-29]. Today, the record efficiency for SiNW solar cells in the lab is 17.11%, reported by Lin et al. [30]. This is of course still lower compared to the industrial silicon solar cells with optimized processes. Nevertheless, the difference is not significantly high taking into account that high-efficiency Si solar cells have been achieved after huge research effort for a dozen of decades.

Both bottom-up additive fabrication approaches (vapor-liquid-solid growth, VLS) [31] and top-down subtractive fabrication techniques, including wet etching (such as metal-catalyzed electroless etching or metal assisted etching) [32], and dry plasma etching are reported [33, 34]. SiNWs can have an axial p-n junction, which is formed along their length [33-35], or a radial p-n junction, where junction is formed from the outer to the center of every wire and surrounds their entire surface [36-39]. That means that the radial SiNW p-n junction has a core-shell configuration where the core is n (p) and the shell p (n). In the latter case, the accurate control of the junction depth is crucial. Deposition of a doped Si thin film on the nanowires is the most common method for the radial junction formation. The junction should be quite shallow and its depth should not exceed the nanowire radius, so that the core remains undoped. Typical ion implantation techniques use high ion energies (>8 eV) that are not capable for short implantation depth, while ultra-shallow junctions, where the depth is a few tens of nm, require modern, sophisticated and very expensive equipment working on

low ion energies (2-3 eV). Moreover, the ion implantation technique is also almost impossible to be applied successfully in vertical nanowire structures. Given this fact, diffusion of impurities from spin-on sources by rapid thermal annealing has been an alternative, effective and low cost method for shallow junction formation. Usami et al. were the first to report a junction depth of less than 20 nm using this method [40]. Rapid thermal diffusion from SOD has been applied both in the fabrication of transistors [41] and in planar Si photovoltaic devices [42-44], showing promising electrical characteristics. The application of SOD solutions for doping of silicon nanowires is very attractive. Nevertheless, is very limited to date. We can only mention the work of Ayon at al., who reported a photovoltaic device based on radial n^+p SiNWs (phosphorus implantation from SOD) achieving photovoltaic efficiency of 11.3%, that was higher compared to the efficiency of the corresponding planar device (10.26%) [45-47]. Moreover, SOD has been applied to SiNWs for thermoelectric power generator application [48]. In both cases, Si nanopillars and nanowires were fabricated by metal-assisted wet etching techniques.

To our knowledge, there are currently no reports of SOD application on plasma etched SiNWs for radial junction formation. In our previous works we demonstrated the top-down fabrication of highly ordered, well-aligned and perpendicular to the substrate Si nanopillars [49] and high aspect ratio Si nanowires [50, 51] using cryogenic plasma Si etching process after colloidal particle self-assembly. These structures exhibited exceptional antireflective and light trapping properties [50]. In order to take advantage of these properties we fabricated an axial p^+n junction Si nanopillar photovoltaic device [34] where we tested several methods to mitigate the leakage current through the passivation of the traps on the nanowire's surface. Here, we extend our work presenting the fabrication and characterization of a photovoltaic device based on core-shell p^+n plasma-etched SiNWs. In general, such an approach is expected to improve severely the light conversion and hence the efficiency in comparison to our axial nanowire or planar PV devices. This is mainly attributed to the increased surface area that is receiving photons compared to the previous device geometries. Spin-On Dopant solution is employed to replace boron ion implantation in SiNWs and form a shallow p^+n core-shell (radial) junction. As stated above this is

the first work using SOD solution to dope plasma etched SiNWs with radial junctions. The whole fabrication process-flow combines cost-effective methods, such as the colloidal lithography nanopatterning and the SOD diffusion, with standard, clean-room processes, keeping the overall fabrication process CMOS compatible. The effect of rapid thermal annealing to the depth and diffusion profile is studied. Current-Voltage (I-V) electrical characterization of the SiNW device is performed under both dark and illumination conditions, and compared to the performance of a planar Si photovoltaic device with similar doping characteristics.

2 Experimental Details

2.1 Planar p^+n junction diode fabrication

Starting from a 100 mm n-type Si ⟨100⟩wafer (1–5 Ω cm, initial dopant concentration 10^{-15} cm^{-3}) cleaned by RCA process, a 5 nm thin SiO_2 layer on top was thermally grown following dry oxidation method at 850°C. Next, we apply the Spin-On Dopants (SOD) solution (B202 from Filmtronics, with boron concentration of 5 % w/v) on top of the oxide. SOD was spin coated at 3000 rpm for 20 s. The wafer was baked at 160 °C for 15 min on a hot plate to harden the film. Boron diffusion was conducted by rapid thermal annealing (RTA) in an atmosphere of 75% nitrogen and 25% oxygen. Temperatures of 950 °C and 1050 °C for both 15 s and 30 s were tested. Post diffusion cleanup is accomplished through the use of a buffered HF in ultrasonic bath. Then, a 500 nm SiO_2 is grown on the surface by thermal oxidation. For the fabrication of the front contact, two lithography steps were used. First, the SiO_2 layer is patterned by optical lithography to open 50 μm square windows by wet etching using HF solution. Then, a 500 nm Al film is deposited on the front surface, patterned by optical lithography and wet etched. Similarly, the back contact was made by deposition of a 500 nm Al film on the wafer's backside. Finally, Al was annealed at 320 °C in N_2 ambient for 20 min. A schematic of the planar diode is shown in the inset of Figure 2(b).

2.2 Radial p^+n junction SiNW device fabrication

Fig. 1(a)–(i) shows the process flow for the fabrication of ordered, perpendicular to the substrate Si nanowire arrays with p^+n junction along the radial direction of each wire. We start from a 100 mm n-type Si ⟨100⟩wafer (1–5 Ω cm) with a 250 nm Si_3N_4 layer and a 100 nm TEOS layer deposited on top by LPCVD, as shown in Fig. 1(b). 2×2 mm^2 square windows were patterned on TEOS by optical lithography following the mask pattern of Fig.1(j). Wet etching of the TEOS layer using buffered HF, followed by dry etching of the Si_3N_4 layer by SF_6 plasma, is performed through the 2×2 mm^2 windows (Fig.1(c)).

Then, we proceed to the fabrication of silicon nanowires into the patterned areas by colloidal particle self-assembly (colloidal lithography) and plasma etching, as described in detail in our previous articles [34, 49, 50]. All etching processes were conducted in a helicon type antenna, high density plasma reactor (MET system from Alcatel-Adixen) typically working in the inductive mode. Briefly, 520 nm polystyrene particles (purchased from Distrilab, catalog number 5052A, 10% w/w aqueous suspensions, ≤ 3% CV) were spin coated into the windows forming a uniform monolayer (Fig.1(d)). We shrink the particles using isotropic O_2 plasma etching (conditions: helicon plasma source power 1900 W, platen bias power 0 W, pressure 1.33 Pa, 100 sccm O_2 flow and temperature 15°C). The shrunk diameter of the particles is 160-200 nm (Fig.1(e)). Pattern transfer to Si was conducted by cryogenic anisotropic Si plasma etching (Fig.1(f)). The plasma conditions used are: Helicon plasma source power 1200 W, bias voltage -40 V, a gas mixture of 200 sccm SF_6 and 55 sccm O_2 gas flow at a pressure of 1.33 Pa and an electrode temperature of -105 °C. Polystyrene spheres were removed from the top of the wires through the use of a piranha solution (H_2SO_4:H_2O_2) soak (Fig.1(g)). Etching results in the fabrication of highly ordered, hexagonically packed SiNW arrays, with a diameter of 160-200 nm, a height of 3 μm (aspect ratio up to 19:1) and period of 520 nm.

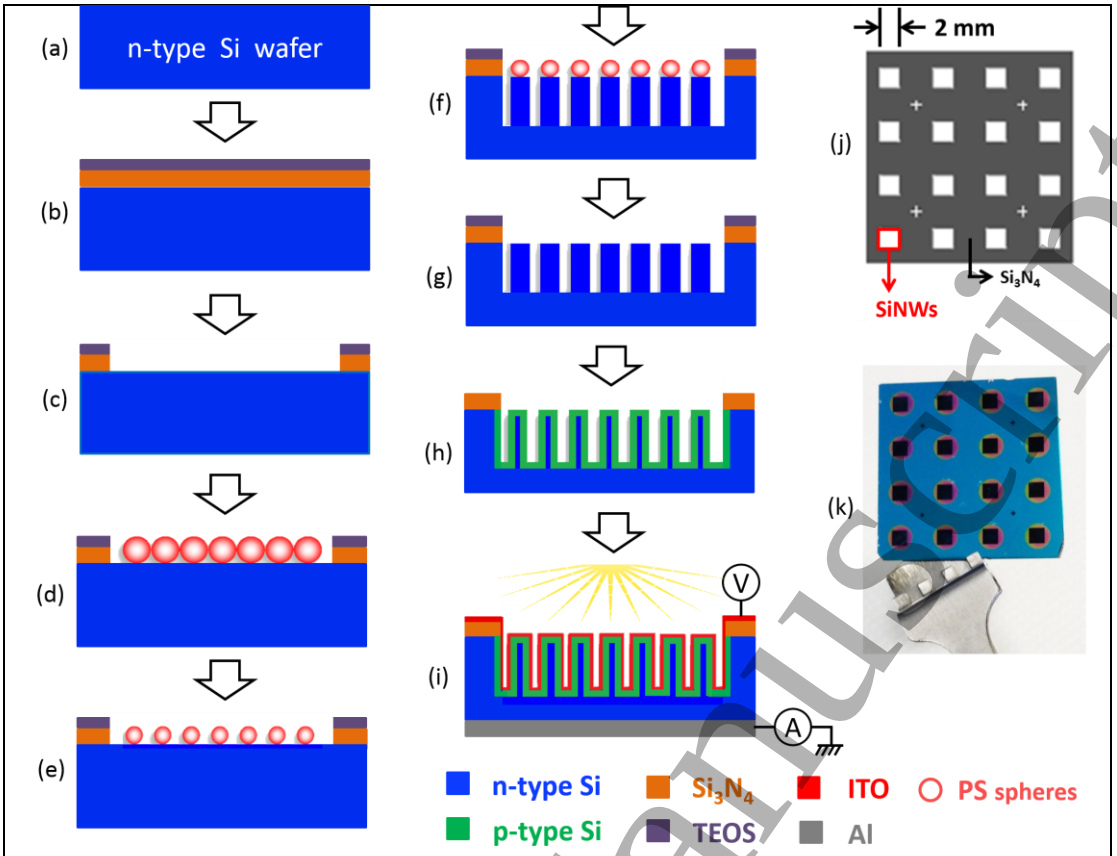


Figure 1: Process flow for the fabrication of radial p-n junction SiNW photovoltaic device. (a) Starting n-type Si wafer. (b) LPCVD of a 250 nm Si_3N_4 film and a 100 nm TEOS film. (c) Optical lithography (2×2 mm^2 mask windows) and etching of Si_3N_4 and TEOS layers. (d) Spin coating of PS colloidal spheres. (e) PS sphere shrinking by isotropic O_2 plasma etching. (f) Pattern transfer and SiNW fabrication by cryogenic etching. (g) PS sphere removal by wet etching. (h) Spin-On Dopant application and formation of p^+n radial junction by boron rapid thermal diffusion. (i) top transparent electrode (ITO) deposition and back contact Al deposition and annealing (final device). (j) Top-down schematic design of the device. (k) Photograph of the final SiNW photovoltaic device.

The next step includes the formation of the radial p^+ layer (shell) surrounding the fabricated n-type SiNWs using Spin-On Dopants solution (Fig.1(h)), following the same procedure as described in section 2.1. Prior to SOD application, a 5 nm SiO_2 oxide layer was formed on the SiNWs by dry thermal oxidation. SiO_2 thickness and

thus the resulting SiNW diameter was monitored by SEM measurements prior to oxidation, after oxidation and after SiO_2 wet etching. Rapid thermal annealing of the SOD was performed at 950 °C for 30 s. Both SOD and SiO_2 layers are removed by immersion in a buffered HF solution. The final step is the fabrication of the front and back electrical contacts (Fig.1(i)). First, we deposit a 500 nm Al layer on the back of the samples, followed by an annealing process at 320 °C for 20 min in ambient N_2. Second, we deposit a 125 nm indium tin oxide (ITO) layer by RF-Magnetron sputtering on top of the SiNWs, through a hard aluminum mask with 3 mm holes that are in alignment with the nanostructured areas of the sample, so that the SiNW areas are fully covered by the front electrical contact. Samples were soaked in buffered HF prio to Al and ITO deposition, in order to remove any native oxide formed on Si. The ITO layer is annealed at 300 °C for 30 min under argon flow. The annealing process improves the ITO resistivity by an order of magnitude, as it was measured 3.99×10^{-2} Ωcm and 1.57×10^{-3} before and after the annealing, respectively. Figure 1(k) shows a photo of the final radial p-n junction SiNW photovoltaic device. Sample areas having black colors are areas full of SiNWs. This black color is a characteristic of their extremely low reflectance, as we have shown in a previous work [50].

2.3 Process and Device characterization

Scanning Electron Microscopy (SEM instrument JSM 7401F by JEOL) was employed for the morphology characterization of both the SiNWs and the final photovoltaic device. Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was used for the measurement of boron diffusion profile, in planar control samples, allowing for the accurate extraction of the p-n junction depth. We assume the same junction depth for the p^+ shell layer surrounding the n-SiNWs.

Resistivity measurements on the Si surface were performed before and after the boron diffusion by a four-point-probe system in a homemade apparatus which consists of a probe head from Alessi and a Keysight B2902 source measure unit. Electrical characterization of the final photovoltaic device was performed in terms of I-V measurements using a probe station that includes a HP 4140B pA meter/DC voltage

source controlled by Labview Software and a HP4155B Semiconductor Parameter Analyzer. A voltage bias was applied between the top and the bottom contacts, as shown in Fig.1(i). The bottom contact was grounded, while the top-contact probe was in direct contact with ITO transparent electrode. Electrically conductive silver paint was used to strengthen contact between the probe and the ITO layer. The applied bias voltage during the I-V measurements swept from negative to positive values. The current-voltage measurements under illumination were taken at nominal conditions (Air Mass 1.5, 100 mW/cm^2).

3. Results and discussion

3.1 Shallow junction fabrication by Spin-On Dopants

The first step, before proceeding with the fabrication and characterization of the radial SiNW photovoltaic device, is to study the dopant diffusion from SOD solution to the formation of ultra-shallow p-n junctions. This study was performed on planar diodes that were fabricated as described in section 2.1. Our aim is to study the electrical behavior of the diodes, calculate the junction depth (meaning the depth of the boron diffusion in Si) and the concentration of boron dopants, in order to define the optimum conditions for rapid thermal annealing of SOD for use in the nanowire devices.

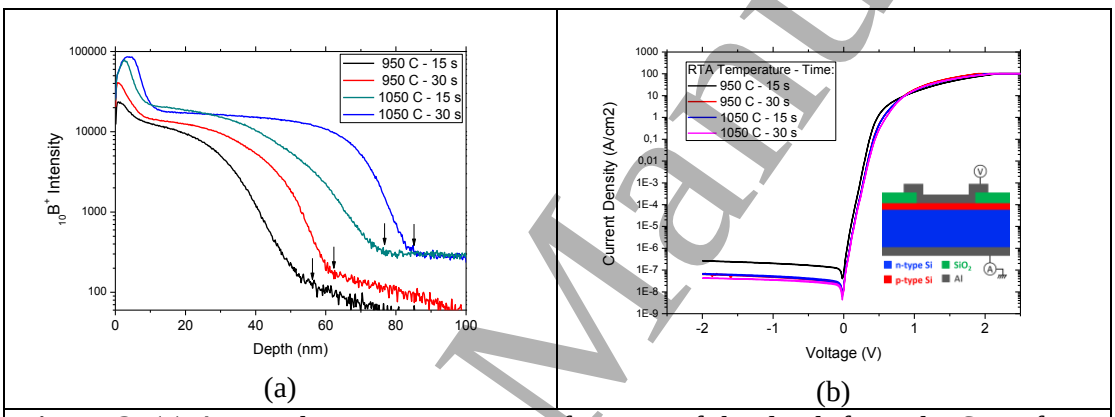
A combination of electrical 4-point-probe measurements and ToF-SIMS measurements were used for the calculation of boron dopant concentration. 4-point probe was used to measure the resistivity of the surface layer, while ToF-SIMS was used to measure the depth of boron diffusion. Table 1 shows the resistance *R* derived from the 4-point-probe measurements for the following RTA temperature and process time conditions: i) 950 °C for 15 s, ii) 950 °C for 30 s, iii) 1050 °C for 15 s, and iv) 1050 °C for 30 s. We observe that the measured resistance is ~30 Ω/□ at 950 °C and ~8.5 Ω/□ at 1050 °C, without significant dependence on processing time. Figure 2(a) shows the spectrum intensity of atomic boron as a function of the depth from the Si surface, for RTA process conditions (i)-(iv), as derived from ToF-SIMS measurements. These curves depict the boron diffusion depth profile. In all conditions

a peak in boron intensity is observed in depths up to 10 nm, which is due to a redundant amount of boron that has remained close to the silicon surface, and not diffused. For larger depths, boron intensity is stabilized until it falls rapidly to reach its minimum value. The bend point before the minimum value of each curve (marked in figure with an arrow) defines the depth of boron diffusion or the p^+n junction depth. Junction depths for each RTA condition (showed in Table 1) range from 54 nm to 85 nm, and increase with increasing temperature and increasing annealing time.

The resistivity of the diffused p^+ region in the n-type Si layer can be calculated from the equation $\rho = (t \cdot \pi/\ln 2)R = 4.532 \cdot t \cdot R$, where t is the thickness of the layer measured by ToF-SIMS and R is the resistance measured by the 4-point-probe. Note that this equation is valid when $t \ll s$, where s is the probe spacing [52]. Finally, boron concentration can be extracted from the resistivity-dopant density relationship for boron-doped silicon presented by Thurber et al. [53] The resistivity values and boron concentration for every annealing condition are also noted in Table 1. We observe that there is high dopant concentration of the order of 10^{20} atoms/cm^2, which increases with increasing rapid thermal annealing temperature. We therefore conclude that using a Spin-On Dopant solution and diffusion by rapid thermal annealing we can form shallow p^+n junctions with relatively steep profile, high impurity concentration and junction depth of several tens of nanometers (<100 nm). These diode features prove to be suitable for radial junction formation using SOD in nanowires of diameter larger than 150 nm.

Table 1: Resistance *R* (4-point-probe measurements), p^+n junction depth (ToF-SIMS measurements), resistivity ρ and boron doping concentration for various RTA conditions (temperature and process time)

	Rapid Thermal Annealing (RTA) process conditions			
	950 °C 15 s	**950 °C 30 s**	**1050 °C 15 s**	**1050 °C 30 s**
R (Ω/□)	29.9	33	8.3	8.5
Junction Depth (nm)	54	62	76	85
ρ (Ω-cm)	0.000732	0.000972	0.000286	0.000327
B doping concentration (cm^{-3})	1.76×10^{20}	1.31×10^{20}	4.68×10^{20}	4.1×10^{20}



(a) (b)

Figure 2: (a) Atomic boron intensity as a function of the depth from the Si surface, for different RTA process conditions, as measured by ToF-SIMS. The arrows show where the p-n junction depth is considered. (b) J-V characteristics in dark of planar p^+n diodes, fabricated using SOD for boron implantation for different RTA process conditions. Inset: Schematic illustration of the planar p^+n diode.

Planar diodes where also electrically characterized by dark I-V measurements made in a wafer probe station. Figure 2(b) shows the J-V characteristics of the planar p^+n diodes for the RTA temperature and SOD diffusion times (i)-(iv) as mentioned previously. In all cases, the diodes have low leakage current under reverse bias, and a sharp increase in the current in the forward bias. The sample annealed under RTA condition (i), i.e. 950 ° C for 15 s, is suffering from the highest reverse current

compared with the rest conditions (ii)-(iv). The forward J-V characteristics are almost independent on the RTA conditions. A careful observation of the J-V measurements revealed that the RTA conditions (ii), i.e. 950°C for 30 s, are the most appropriate to apply for the SiNW photovoltaic device.

3.2 Radial p-n junction SiNW device characterization

Figure 3 presents SEM images of the fabricated photovoltaic device with core-shell SiNWs. In particular, Figures 3(a) and 3(b) show in low and higher magnification (both tilted at 45°) the plasma-etched nanowires in the pre-patterned square window. The nanowires are closely-packed arranged in a hexagonal lattice (due to the colloidal lithography) and cover the whole window area. Figures 3(c) and 3(d) show the core-shell nanowires in cross-section after the deposition of the 125 nm ITO layer. The ITO film creates a uniform layer of low roughness covering the nanowires throughout their height, and extends out of the square area on the surrounding Si_3N_4 dielectric layer. Higher resolution SEM images are provided in Supporting Information. SiNWs exhibit diameters in the range of 160 to 200 nm, a height of 3 μm with a vertical and smooth sidewall profile, and a period of 520 nm. The diameter variability is due to the process of colloidal particle self-assembly that was used as an etching mask [50]. We note that, there are two morphological defects on the SiNWs: (a) a pyramid-shaped base present at the bottom of every nanowire which is due to crystal orientation dependent etching (CODE) [50, 54] and (b) the presence of small amount of roughness at the top of the wires coming from the colloidal particle etching mask and transferred to the wires during etching [50]. According to the data in Table 1, the junction depth is 62 nm and the related p^+ layer has a mean dopant concentration 1.31×10^{20} atoms/cm^3. Considering this junction depth and the diameter of the nanowires (160-200 nm), a radial junction is realized where the outer shell of the nanowires consists of p^+-type Si, while the core remains n-type Si.

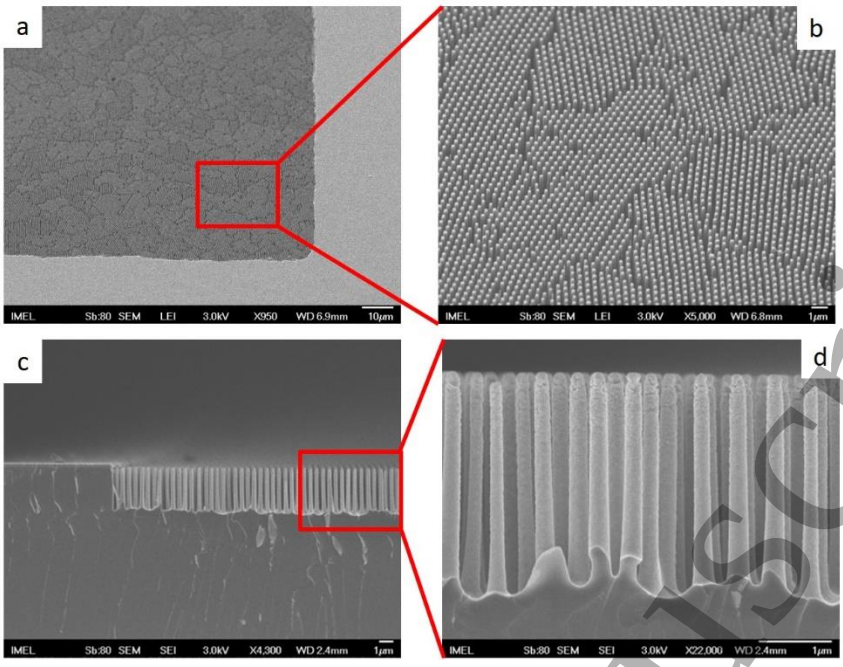


Figure 3: SEM images of the radial p-n junction SiNWs: (a)-(b) after cryogenic Si etching of the nanowires (tilted at 45°), and (c)-(d) after ITO thin film deposition on the nanowires (tilted at 90°). SiNW dimensions are: diameter 160-200 nm, height 3 μm and period 520 nm. Please refer to Supporting Information for higher resolution SEM images.

A planar p^+n junction photovoltaic device was also fabricated following the process flow illustrated in Figure 1, excluding the steps of the SiNWs fabrication (colloidal lithography and cryogenic etching). The same SOD conditions of boron implantation were employed. The aim is to compare the response of the nanostructured photovoltaic device to the corresponding planar device. Note that the planar device configuration does not have an antireflective coating to increase the absorption of light.

Electrical characterization of the radial SiNW photovoltaic device was performed in terms of current-voltage under light illumination at nominal conditions (Air Mass 1.5, 100 mW/cm^2) to demonstrate the photo-response of our devices. Figure 4 shows the photo J-V and dark J-V of both the radial SiNW device and

corresponding planar device. At short-circuit, current density is $J_{sc}(\mathrm{SiNW}) = 12.3\ \mathrm{mA/cm^2}$, and $J_{sc}(\mathrm{planar}) = 8.13\ \mathrm{mA/cm^2}$, for the nanowires and planar device, respectively. The open-circuit voltage is $V_{oc}(\mathrm{SiNW}) = 430\ \mathrm{mV}$ and $V_{oc}(\mathrm{planar}) = 384\ \mathrm{mV}$, for the two devices, respectively. We see that the radial junction SiNW photovoltaic device shows higher current density and open-circuit voltage than the non-nanostructured device, which is a result of enhanced light trapping and improved absorbance and collection of incident photons in the SiNWs [50]. From the curves of Figure 4 we can also extract the fill factor *FF*, defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}, which is also a measure of the abruptness of the I-V curve. The fill factor of the SiNW and planar device is $FF(\mathrm{SiNW}) = 0.64$ and $FF(\mathrm{planar}) = 0.72$, respectively. Planar device shows a better fill factor than the radial SiNW device, which can be attributed to the higher recombination rate in case of the nanowires due to the much higher concentration of interface states of the nanostructured core-shell Si junction. Finally, the power conversion efficiency is $\mathrm{PCE(SiNW)} = 3.69\ \%$ for the radial SiNWs και $\mathrm{PCE(planar)} = 2.24\ \%$ for the planar Si photovoltaic device. The calculated electrical characteristics of both devices are summarized in Table 2.

We conclude that the radial p^+n junction silicon nanowire photovoltaic device exhibit superior performance than the corresponding planar approach. We consider this as a promising result, although the efficiency is relatively low compared to commercial silicon solar cells. The radial junction SiNWs fabricated using Spin-On-Dopants solution for boron implantation, show promising filling factor and satisfactory photocurrent and open circuit voltage. The most important factors for current loss in such device are the high surface currents, recombination currents, and losses at the nanowire/ITO electrode interfaces. These are due to the very large total active surface area of the diode. Moreover, morphological structural defects of the SiNWs may contribute to current loss due to recombination. In the future, different design approaches may be tried for further optimization of the electrical contact fabrication and electrical characteristics of the diode, which could increase the overall performance at competitive levels.

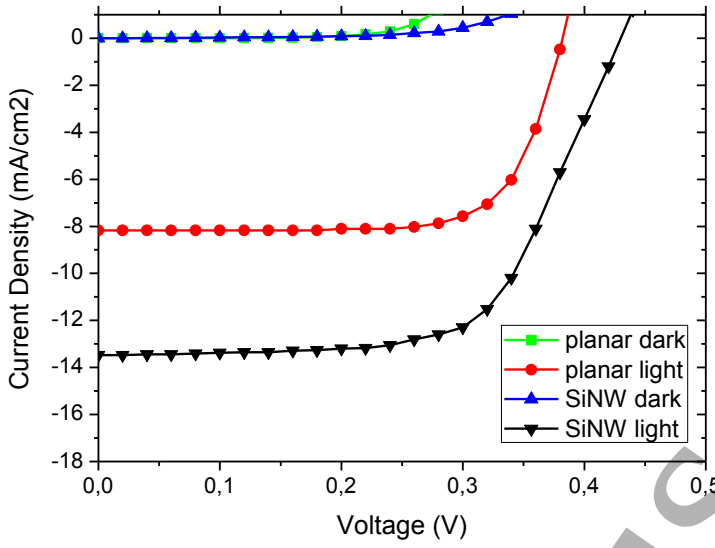


Figure 4: Characteristic J-V under illumination (Air Mass 1.5, 100 mW/cm^2) of a radial SiNW based photovoltaic device and its corresponding planar device.

Table 2: Open-circuit voltage V_{OC}, short-circuit current I_{SC}, fill factor FF and power conversion efficiency PCE, of a radial SiNW based photovoltaic device and a planar corresponding device, as derived from the J-V curves of Figure 4.

	V_{oc} (V)	J_{sc} (mA/cm^2)	*FF*	PCE %
planar PV device	0.384	8.13	0.72	2.24
radial SiNW PV device	0.430	12.3	0.64	3.69

Conclusions

The fabrication and characterization of a photovoltaic device based on radial p$^-$n junction Si nanowire arrays was demonstrated. Colloidal lithography combined with cryogenic silicon plasma etching were used for the fabrication of high aspect ratio (AR>15) nanowires, providing low-cost patterning and good structural characteristics

of the nanowires in terms of uniformity and smooth sidewall profile. For the fabrication of the radial p-n junction using SiNWs, we used Spin-On Dopant (SOD) solution for boron diffusion. This is a novel approach with regard to the use of SOD in nanowire photovoltaics. We studied the formation of shallow p-n junctions on planar diodes by use of rapid thermal annealing (RTA) for boron diffusion from SOD. Diffusion depths of a few tens of nanometers (54 nm to 85 nm) with high concentration of boron dopants were achieved. We then proceeded to the fabrication a radial SiNW photovoltaic device, proposing a process flow starting from a Si wafer. Each device consists of a 2mm × 2mm area, surrounded by dielectric material, in which SiNWs of 160-200 nm diameter, 3 μm high and 520 nm period are embedded. The electrical characterization of the photovoltaic response of the SiNWs was performed in terms of I-V measurements under illumination at normal conditions. A short-circuit current density of 12.3 mA/cm^2, an open circuit voltage of 430 mV, and a fill factor of FF = 0.64 were obtained. The final efficiency of the nanowire photovoltaic device is PCE = 3.69%, which is higher compared to a corresponding planar Si configuration without nanostructuring.

Acknowledgements

The authors would like to thank Dr. Kamil Awsiuk from the Faculty of Physics, Astronomy and Applied Computer Science of the Jagiellonian University in Krakow, Poland, for the ToF-SIMS measurements. This work was supported by a) the Research Excellence Project 'Plasma Directed Assembly and Organization - PlasmaNanoFactory' which is implemented under the 'ARISTEIA I' Action of the 'OPERATIONAL PROGRAMME EDUCATION AND LIFELONG LEARNING' (Project ID 695) and is co-funded by the European Social Fund (ESF) and National Resources, and b) the PhD fellowship programme of NCSR Demokritos which supported Dr A. Smyrnakis,

References

[1] Tsakalakos L, Balch J, Fronheiser J, Shih M-Y, LeBoeuf S F, Pietrzykowski M, Codella P J, Korevaar B A, Sulima O V, Rand J, Davuluru A and Rapol U 2007 Strong broadband optical absorption in silicon nanowire films *NANOP* **1** 013552--10

[2] Muskens O, Rivas J, Algra R, Bakkers E and Lagendijk A 2008 Design of Light Scattering in Nanowire Materials for Photovoltaic Applications *Nano letters* **8** 2638-42

[3] Garnett E and Yang P 2010 Light trapping in silicon nanowire solar cells *Nano letters* **10** 1082-7

[4] Yun Z, Rivas C, Lake R, Alam K, Boykin T B and Klimeck G 2005 Electronic properties of silicon nanowires *IEEE Transactions on Electron Devices* **52** 1097-103

[5] Schmidt V, Wittemann J V, Senz S and Gösele U 2009 Silicon Nanowires: A Review on Aspects of their Growth and their Electrical Properties *Advanced Materials* **21** 2681-702

[6] Hasan M, Huq M F and Mahmood Z H 2013 A review on electronic and optical properties of silicon nanowire and its different growth techniques *SpringerPlus* **2** 151

[7] Peng K Q and Lee S T 2011 Silicon nanowires for photovoltaic solar energy conversion *Adv Mater* **23** 198-215

[8] Song T, Lee S-T and Sun B 2012 Silicon nanowires for photovoltaic applications: The progress and challenge *Nano Energy* **1** 654-73

[9] Yu P, Wu J, Liu S, Xiong J, Jagadish C and Wang Z M 2016 Design and fabrication of silicon nanowires towards efficient solar cells *Nano Today* **11** 704-37

[10] Soci C, Zhang A, Bao X-Y, Kim H, Lo Y and Wang D 2010 Nanowire Photodetectors *Journal of Nanoscience and Nanotechnology* **10** 1430-49

[11] Bae J, Kim H, Zhang X M, Dang C H, Zhang Y, Choi Y J, Nurmikko A and Wang Z L 2010 Si nanowire metal-insulator-semiconductor photodetectors as efficient light harvesters *Nanotechnology* **21** 095502

[12] Yoon J S, Kim K, Meyyappan M and Baek C K 2017 Optical Characteristics of Silicon-Based Asymmetric Vertical Nanowire Photodetectors *IEEE Transactions on Electron Devices* **PP** 1-6

[13] Zaremba-Tymieniecki, Li C, Fobelets K and Durrani Z A K 2010 Field-Effect Transistors Using Silicon Nanowires Prepared by Electroless Chemical Etching *IEEE Electron Device Letters* **31** 860

[14] Guerfi Y and Larrieu G 2016 Vertical Silicon Nanowire Field Effect Transistors with Nanoscale Gate-All-Around *Nanoscale research letters* **11** 1-7

[15] Gao Z, Agarwal A, Trigg A D, Singh N, Fang C, Tung C-H, Fan Y, Buddharaju K and Kong J 2007 Silicon Nanowire Arrays for Label-Free Detection of DNA *Anal. Chem.* **79** 3291-7

[16] Patolsky F, Zheng G and Lieber C M 2006 Nanowire sensors for medicine and the life sciences *Nanomedicine* **1** 51-65

[17] Kim W, Ng J K, Kunitake M E, Conklin B R and Yang P 2007 Interfacing Silicon Nanowires with Mammalian Cells *Journal of the American Chemical Society* **129** 7228-9

[18] Shao M, Cheng L, Zhang X, Ma D D D and Lee S-t 2009 Excellent Photocatalysis of HF-Treated Silicon Nanowires *Journal of the American Chemical Society* **131** 17738-9

[19] Tsang C H A, Liu Y, Kang Z, Ma D D D, Wong N-B and Lee S-T 2009 Metal (Cu, Au)-modified silicon nanowires for high-selectivity solvent-free hydrocarbon oxidation in air *Chemical Communications* 5829-31

[20] Peng K-Q, Wang X, Li L, Hu Y and Lee S-T 2013 Silicon nanowires for advanced energy conversion and storage *Nano Today* **8** 75-97

[21] Kayes B M, Atwater H A and Lewis N S 2005 Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells *Journal of Applied Physics* **97** 114302

[22] Hochbaum A I and Yang P 2010 Semiconductor Nanowires for Energy Conversion *Chem. Rev.* **110** 527-46

[23] Picraux T, Campbell I, Dayeh S, Evans D and Schuele P 2010 Assessment of Silicon Nanowire Architecture for PV Application *Solar Energy Technologies Program Peer Review*

[24] Shao M, Ma D D D and Lee S-T 2010 Silicon Nanowires - Synthesis, Properties, and Applications *European Journal of Inorganic Chemistry* **2010** 4264-78

[25] Garnett E C, Brongersma M L, Cui Y and McGehee M D 2011 Nanowire Solar Cells *Annual Review of Materials Research* **41** 269-95

[26] Kapadia R, Fan Z, Takei K and Javey A 2012 Nanopillar photovoltaics: Materials, processes, and devices *Nano Energy* **1** 132-44

[27] Daiji K, Shigeo Y, Akira T, Makoto T and Makoto K 2015 Photovoltaic properties of axial-junction silicon nanowire solar cells with integrated arrays *Japanese Journal of Applied Physics* **54** 08KA9

[28] Shang A, Zhai X, Zhang C, Zhan Y, Wu S and Li X 2015 Nanowire and nanohole silicon solar cells: a thorough optoelectronic evaluation *Progress in Photovoltaics: Research and Applications* n/a-n/a

[29] Li X 2012 Metal assisted chemical etching for high aspect ratio nanostructures: A review of characteristics and applications in photovoltaics *Current Opinion in Solid State and Materials Science* **16** 71-81

[30] Lin X X, Hua X, Huang Z G and Shen W Z 2013 Realization of high performance silicon nanowire based solar cells with large size *Nanotechnology* **24** 235402

[31] Kayes B M, Filler M A, Putnam M C, Kelzenberg M D, Lewis N S and Atwater H A 2007 Growth of vertically aligned Si wire arrays over large areas (>1 cm[sup 2]) with Au and Cu catalysts *Applied Physics Letters* **91** 103110

[32] Peng K-Q, Yan Y-J, Gao S-P and Zhu J 2002 Synthesis of large-area Silicon Nanowire Arrays via self-assembling nanoelectrochemistry *Adv. Mater.* **14** 1164-7

[33] Wong S M, Yu Y H, Li Y, Li J, Sun X W, Singh N, Lo G Q and Kwong D L 2011 Boosting Short-Circuit Current with Rationally Designed Periodic Si Nanopillar Surface Texturing for Solar Cells *IEEE Transactions on Electron Devices* **58** 3224-9

[34] Smyrnakis A, Dimitrakis P, Normand P and Gogolides E 2017 Fabrication of axial p-n junction silicon nanopillar devices and application in photovoltaics *Microelectronic Engineering* **174** 74-9

[35] Lee Y-J, Yao Y-C and Yang C-H 2013 Direct electrical contact of slanted ITO film on axial p-n silicon nanowire solar cells *Optics Express A* **21** 7-14

[36] Garnett E and Yang P 2008 Silicon Nanowire Radial p-n Junction Solar Cells *J. Am. Chem. Soc.* **130** 9224-5

[37] Christesen J D, Zhang X, Pinion C W, Celano T A, Flynn C J and Cahoon J F 2012 Design principles for photovoltaic devices based on Si nanowires with axial or radial p-n junctions *Nano letters* **12** 6024-9

[38] Huang T-Y and Yen T-J 2012 Radial p-n Junction Solar Cells by Core-Shell Silicon Nanowire Arrays *MRS Proceedings* **1302**

[39] Kim D R, Lee C H, Rao P M, Cho I S and Zheng X 2011 Hybrid Si Microwire and Planar Solar Cells: Passivation and Characterization *Nano letters* **11** 2704-8

[40] Usami A, Ando M, Tsunekane M and Wada T 1992 Shallow-junction formation on silicon by rapid thermal diffusion of impurities from a spin-on source *IEEE Transactions on Electron Devices* **39** 105-10

[41] Zhu Z T, Menard E, Hurley K, Nuzzo R G and Rogers J A 2005 Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates *Applied Physics Letters* **86** 133507

[42] Ventura L, Slaoui A, Hartiti B, Muller J C, Stuck R and Siffert P 2011 Shallow-Junction Formation by Rapid Thermal Diffusion into Silicon from Doped Spin-on Glass Films *MRS Proceedings* **342**

[43] Iyengar V V, Nayak B K and Gupta M C 2010 Silicon PV devices based on a single step for doping, anti-reflection and surface passivation *Solar Energy Materials and Solar Cells* **94** 2205-11

[44] Rohatgi A, Chen Z, Doshi P, Pham T and Ruby D 1994 High-efficiency silicon solar cells by rapid thermal processing *Applied Physics Letters* **65** 2087-9

[45] Pudasaini P R, Elam D and Ayon A A 2013 Radial junction nanopillar arrays textured n-type silicon solar cells. In: *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC),* pp 2404-9

[46] Pudasaini P R and Ayon A A 2013 Nanostructured plasmonics silicon solar cells *Microelectronic Engineering* **110** 126-31

[47] Pudasaini P R and Ayon A A 2013 High performance nanopillars array silicon solar cells. In: *2013 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP),* pp 1-5

[48] Xu B and Fobelets K 2014 Spin-on-doping for output power improvement of silicon nanowire array based thermoelectric power generators *Journal of Applied Physics* **115** 214306

[49] Ellinas K, Smyrnakis A, Malainou A, Tserepi A and Gogolides E 2011 “Mesh-assisted” colloidal lithography and plasma etching: A route to large-area, uniform, ordered nano-pillar and nanopost fabrication on versatile substrates *Microelectronic Engineering* **88** 2547-51

[50] Smyrnakis A, Almpanis E, Constantoudis V, Papanikolaou N and Gogolides E 2015 Optical properties of high aspect ratio plasma etched silicon nanowires: fabrication-induced variability dramatically reduces reflectance *Nanotechnology* **26** 085301

[51] Makarona E, Skoulikidou M C, Kyrasta T, Smyrnakis A, Zeniou A, Gogolides E and Tsamis C 2015 Controllable fabrication of bioinspired three-dimensional ZnO/Si nanoarchitectures *Materials Letters* **142** 211-6

[52] Dieter S 2006 *Semiconductor material and device characterization* (Piscataway NJ; Hoboken N.J.: IEEE Press; Wiley)

[53] Thurber, Mattis, Liu and Filliben 1981 The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron-Doped Silicon

[54] Dussart R, Tillocher T, Lefaucheux P and Boufnichel M 2014 Plasma cryogenic etching of silicon: from the early days to today's advanced technologies *Journal of Physics D: Applied Physics* **47** 123001