Barrier height and ideality factor dependency on identically produced small Au/p-Si Schottky barrier diodes

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Abstract: Small high-quality Au/P-Si Schottky barrier diodes (SBDs) with an extremely low reverse leakage current using wet lithography were produced. Their effective barrier heights (BHs) and ideality factors from current–voltage (I–V) characteristics were measured by a conducting probe atomic force microscope (C-AFM). In spite of the identical preparation of the diodes there was a diode-to-diode variation in ideality factor and barrier height parameters. By extrapolating the plots the built in potential of the Au /p-Si contact was obtained as $V_{\rm bi} = 0.5425$ V and the barrier height value $\Phi_{\rm B(C-V)}$ was calculated to be $\Phi_{\rm B(C-V)} = 0.7145$ V for Au/p-Si. It is found that for the diodes with diameters smaller than 100 μm, the diode barrier height and ideality factor dependency to their diameters and correlation between the diode barrier height and its ideality factor are nonlinear, where similar to the earlier reported different metal semiconductor diodes in the literature, these parameters for the here manufactured diodes with diameters more than 100 μm are also linear. Based on the very obvious sub-nanometer C-AFM produced pictures the scientific evidence behind this controversy is also explained.

Key words: Schottky barrier diodes; conducting probe-atomic force microscope; barrier height and ideality factor
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1. Introduction

Shortly after Schottky introduced his metal–semiconductor (M–S) diode and its essential parameter, barrier height (BH) in 1938[1] Mott defined the BH of MS contact as the difference of the semiconductor electron affinity and the related metal work function[2].

The ideality factor n can be found from its forward current–voltage (I–V) characteristics[1–3]. Following the suggestion of Song *et al.* regarding the role of inhomogeneities in the interfacial oxide layer composition and thickness, in developing of the barrier inhomogeneities[4]. In the early 1990s, Tung[5–8], Werner *et al.*[9] and Biber *et al.*[10] mentioned that the BH is likely to be a function of the interface atomic structure, and the atomic inhomogeneities at the M–S interface which are caused by facets, defects, grain boundaries and mixture of different phases. Therefore, they suggested that non-ideal behavior of the Schottky barrier diodes (SBDs) could be quantitatively explained by assuming a distribution of nanometer-scale interfacial patches of reduced Schottky barrier height (SBH). Monch *et al.*[11–13] experimentally approve that the linear relationship between the effective BHs and ideality factors can be explained by lateral inhomogeneities of the BH. It was only during the last decade that by considering the inhomogeneities of the M–S interface these devices have attracted much attention and progressed to play a crucial role in constructing some useful devices in electronic technology as well as being used for technical deficiencies such as surface processing, clean room, vacuum preparation and deposition techniques to produce proper contacts.

Due to the expectation of significant deviations from conventional behavior for nano-diodes, an increasing interest is devoted to studying the effects of downscaling lateral dimensions on the electrical behavior of the MS contact and detecting the local SBH on the nanometer scale[14–22]. The ballistic electron emission microscopy (BEEM) is the traditionally used device for microscopic SBH measurements[21]. Its mechanism is based on the hot electrons injection by tunneling from the reverse biased scanning tunneling microscope (STM) tip to the metal film.

More recently Giannazzo *et al.*[23] demonstrated a conducting probe atomic force microscope (C-AFM) approach allowing both current imaging (imaging mode) across metal–semiconductor Schottky contacts and quantitative mapping (spectroscopic mode) of SBH distribution, with 10–20 nm spatial resolution and energy resolution better than 0.1 eV. In spite of the above mentioned valuable reports on the small size MS contacts only few investigated the unusual behavior of BH and the ideal factor in the small Schottky contacts[24, 25]. Nakamura *et al.*[25] reported a linear dependency of potential barrier height to ideality factor and others[25–31] mostly believe the week linear dependency of barrier height on ideality factor. Recently Aydogan *et al.*[32] mentioned that barrier heights are independent of the diode size. To our knowledge the nonlinear dependency of BH and ideality factor on the diode diameter never fundamentally studied.

In the present work, to overcome the structural limitations of BEEM an alternative approach for nanometric scale SBH measurements based on C-AFM is demonstrated. We prepared small Au/p-Si Schottky diodes by wet lithography, and obtained current–voltage characteristics for the first time for small Au/p-Si Schottky diodes using a C-AFM. We demonstrate the nonlinear dependency of BH and the ideality factor on the diode diameter and correlation between the diode BH and

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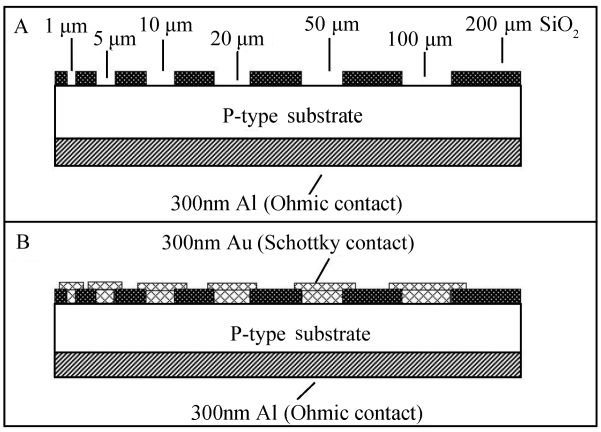

Fig. 1. Schematic drawing of Schottky contact. The sizes are not in scale. The shapes of the manufactured contacts are circular, and their diameters were 1, 5, 10, 20, 50 and 100 μm. All patterns were circular in shape for Ohmic contact used by pure Al. Schottky contact made by pure gold layer.

its ideality factor are derived and the influence of the patches, i.e. the inhomogeneities, by decreasing the diode size is also studied.

2. Experimental procedure

P-type semiconductors with born (B) impurity, crystal direction of (100) with thickness of 575 $\pm$ 15 μm, resistivity of 4–11 Ω·cm with $N_A = (1.261–3.4675) \times 10^{16}$ cm^{-3} is selected. In Fig. 1, the schematic form of an M–S contact patterns from 1 to 100 μm is shown.

The sample surfaces are polished and for cleaning the RCA method is applied. For degreasing a mixture of DI H_2O and NH_4OH and H_2O_2 with a ratio of 1 : 1 : 5 was used to wash the samples for 10 min. To remove ion particles the samples were dipped in a mixture of HCl, DI H_2O and H_2O_2 with a ratio of 1 : 1 : 6 for 10 min and then rinsed in double distilled water for 1 min. The samples were dipped in DDH_2O, HF and H_2O_2 with a ratio of 1 : 50 for 5 s for deoxidization and then washed by double distilled water for 1 min. For ohmic contact pure aluminum with resistivity of 2.7 $\mu\Omega$·cm is used. Deposition procedure is done immediately after cleaning in a vacuum chamber at 5×10^{-5} Torr, aluminum with 99.99% purity is deposited with a 300 nm thickness and the ratio of the coating was 4 Å/s. Higher deposition rates will make the deposited layer unsmoothed with poor morphology. After this stage the samples were annealed in an oven with H_2 gas at 470 ℃ for 30 min. Schottky contacts were patterned on a double PMMA-resist layer by wet lithography. Prior to the gold evaporation, the patterned samples were dipped for 5 s in $HCl : H_2O$ and rinsed in DI water, to remove oxide remnants originating from the development of the resist film in an organic solution (MIBK : IPA, 1 : 2). The Schottky contacts were made by evaporating 300 nm of gold onto the sample at a rate of 1.5 Å/s in a vacuum better than 10^{-5} Torr, with a substrate temperature of 25 ℃. Finally, a lift-off process was performed on the samples using acetone at room temperature.

In Fig. 1, the shapes of contacts are presented which all have a circular shape, and their diameters are 1, 5, 10, 20, 50 and 100 μm.

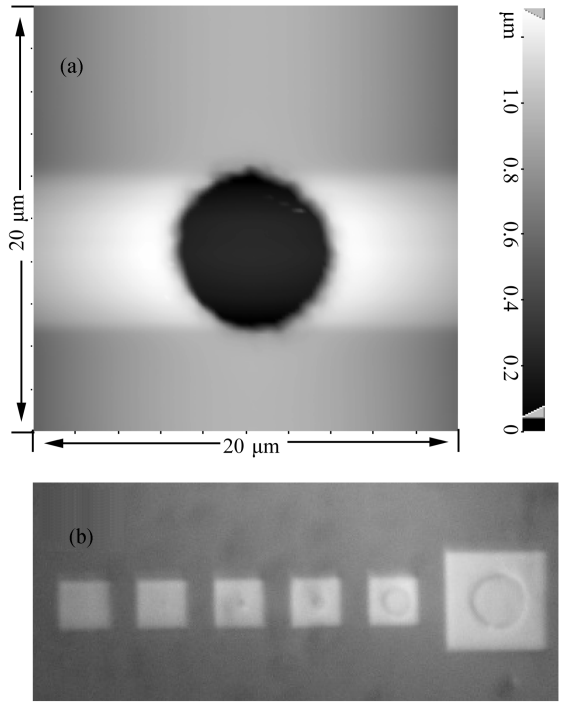

Fig. 2. (a) Small 5 μm contact and its fine pattern in the edge. (b) Microscopic images of some small circular shaped patterns made using wet lithography and 250 nm Au Schottky contacts made by evaporation system.

With wet lithography we can construct high precision samples with the radius of down to 5 μm by this method as shown in Fig. 2(a). In Fig. 2(b), the view of manufactured contacts with various dimensions is shown.

Figure 3(a) shows the AFM image after surface preparations; the surface is smooth with a maximum roughness of 5.7 nm. Figure 3(b) shows the AFM image of a produced sample a day after surface treatment. AFM analysis indicates the formation of an oxide layer immediately after the cleaning of the sample where the Schottky contact changes from MS to MIS. As it shows the surface is not smooth any more and the roughness of the surface increased to the maximum amount of 190 nm just a day after first preparation of the sample. This is 30 times more roughness than 5.7 nm in the case of Fig. 3(b).

In the positions where there is oxide, the current is very small and in the pA range and in the position where there is not any oxide, the current is in the nA range. This oxide layer causes a voltage drop across the interface. The presence of an insulating layer between the Au and the p-Si substrate is a result of exposing the front surface of the p-Si substrate to air before the evaporation of Au, and also the absorbing of water or water vapor onto the p-Si surface during the chemical etching process[2, 17, 23].

3. Theoretical background

The current versus voltage for a Schottky barrier diode is given by the following well known equation named the Richardson equation.

$$I = I_S\{\exp[q(V - IR)/nKT] - 1\}, \quad (1)$$

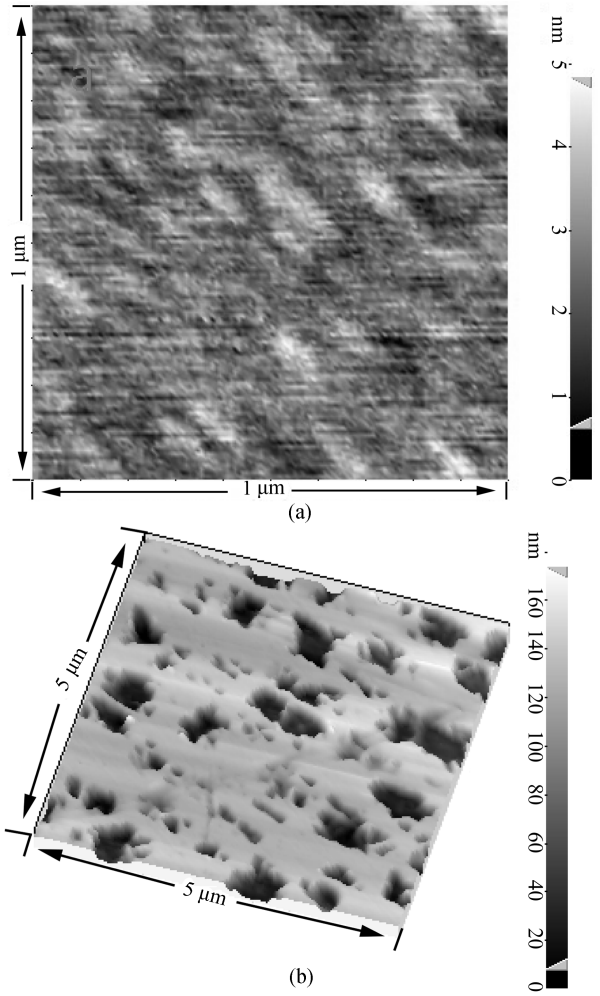

Fig. 3. (a) AFM image immediately after surface preparations, showing the smooth surface with the maximum roughness of 5.7 nm. (b) Phase image of sample a day after surface treatment. AFM analysis shows that an oxide layer is immediately formed after cleaning, therefore the Schottky contact changes from MS to MIS. It is apparent that the surface is not smooth where it has the maximum roughness of 190 nm.

I represent the forward diode current and I_s is the saturation current derived from the straight line intercept of l Au at V = 0 and it is given by

$$I_S = AA^*T^2 \exp\left(-\frac{q\phi_b}{KT}\right), \tag{2}$$

where A^* is modified Richardson constant, A is area (cm^2), K is Boltzmann's constant, T is absolute temperature, ϕ_b is barrier height in volts, q is electronic charge, n is ideality factor and R is resistance. Ideality factor (n) usually has a value greater than 1. High values of n can be attributed to the presence of the interfacial thin native oxide layer or other defects. We used Cheung's method[33] to calculate the barrier height, ideality factor and resistance:

$$\frac{dV}{d\ln I} = n\frac{kT}{q} + IR_s. \tag{3}$$

Equation (3) should give a straight line, thus, a plot of $dV/d(\ln I)$ versus I will give R_s as the slope and $n(kT/q)$ as the y axis intercept. The ideality factor and resistance were determined from the intercept and slope of Eq. (3). The obtained value of R_s was different from diode to diode, so we used an average value of R_s = 187 Ω.

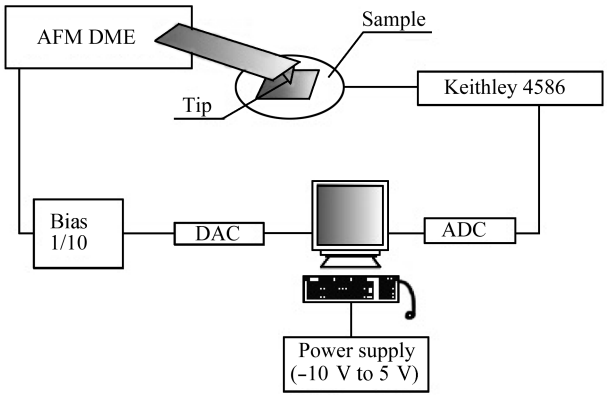

Fig. 4. Schematic C-AFM diagram of the measurement set up, including a C-AFM system and high precision Keithley pico-ampere meter.

The ideality factor is introduced to take into account the deviation of the experimental I–V data from the ideal TE model. In addition, the barrier height can be obtained from the equation:

$$q\phi_b = KT\ln(AA^*T^2/I_s). \tag{4}$$

Barrier height can also be calculated by C–V measurements. The C^{-2} is plotted against the applied voltage. From the intercept on the voltage axis, the barrier height is determined. The C^{-2} is related to voltage (V) by Eq. (5).

$$C^{-2} = 2(V_{bi} - V - kT/q)/q\varepsilon_s N_A, \tag{5}$$

where N_A is p-layer acceptors concentration and ε_s is permittivity. The V_{bi} is the built-in potential and is equal to the voltage intercept V at C^{-2} of a C^{-2} versus V plot; in this approach the barrier height is:

$$\phi_{B(C-V)} = V_{bi} + KT/q\ln\frac{N_v}{N_A}, V_p = KT/q\ln\frac{N_v}{N_A}. \tag{6}$$

V_p is the potential difference between the Fermi level and the top of the valence band in the neutral region of p-Si and can be calculated knowing the carrier concentration N_A.

4. I/V measurement

Figure 4 shows the schematic diagram of the set up that was used in this work. The I–V measurements were performed at room temperature using a commercial AFM (DME) which was converted to a conducting probe-AFM to obtain I–V characteristics. The homebuilt I–V measuring unit contains a Keithley 4586. All of the diodes were contacted with a Pt-coated tip probe.

In Fig. 5(a), we have measured and plotted the $\ln(I)$–V for forward bias from 5 to 100 μm patterns and in Fig. 5(b) we have measured and plotted the I–V for reverse bias. After each measurement, the tip is lifted from the contact and then we re-establish electrical contact. From these I–V characteristics and using Eq. (3, 4) for a Richardson constant A^* = 120

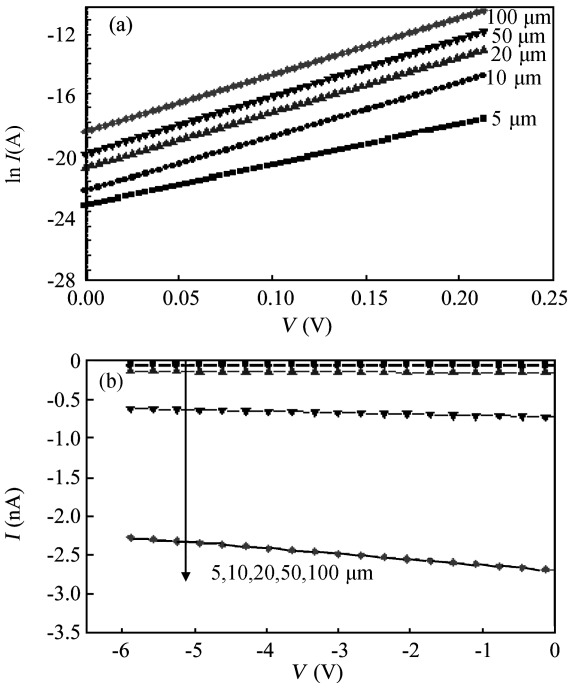

Fig. 5. I–V characteristics measurement of Au/p-Si for 5–100 μm Schottky contact at room temperature, showing a good rectifier behavior in both curves. In the inset the dependency of saturation current on diode diameter and its linear fit has been shown. (a) Forward bias. (b) Reverse bias.

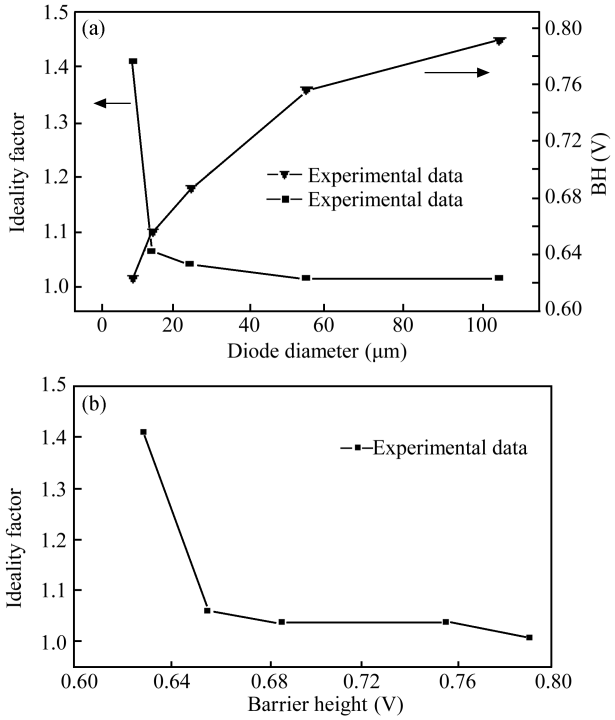

Fig. 6. (a) Dependence of ideality factor to the samples diameter. By decreasing the diode diameter, the ideality factor n increases. The dependence of barrier height to the samples diameter with decreasing diode diameter shows the barrier height decreases. (b) Dependence of potential barrier height on ideality factor.

A/(cm^2·K^2) one can calculate the effective barrier height and ideality factor.

The investigation of Fig. 5(a) shows the device exhibits a good rectification effect. From this figure we obtained the saturated currents (I_s) from $I_s = 5.5\times10^{-11}$ A to $I_s = 7.5\times10^{-9}$ A, The value of the ideality factors (n) varied from $n = 1.41$ to $n = 1.006$ was obtained from the slope of the linear region of the forward bias current–voltage characteristics and the barrier heights (ϕ_b) were from $\phi_b = 0.623$ V to $\phi_b = 0.791$ V.

The measured barrier height values depend strongly on the metal species and the diode size distribution, however there is a definite strong tendency that barrier height becomes larger as the size distribution approaches the uniform distribution of smaller diodes.

Another mechanism is the effect of the environmental Fermi level pinning on free surfaces next to the diodes. This modifies the potential distribution near the contact when the diode size is smaller than the depletion width.

Figure 6(a) shows that with the decreasing diode diameter, the ideality factor n increases, such that this factor reaches from almost its ideal number $n = 1.006$ in 100 μm diameter to $n = 1.41$ in 5 μm diameter diode. Figure 6(a) shows that this dependency is not linear, which is in good agreement with the earlier reported results[11, 13].

Figure 6(a) shows the dependency of barrier height to sample diameter. With the decrease in diode diameter, the barrier height decreases. Investigation of the related curve shows that by increasing the dimension, the diode became ideal. Figure 6(b) shows the dependency of potential barrier height to ideality factor which is nonlinear.

In the AFM picture of Fig. 7(a) the deposited Au as patches of approximately 100 to 200 nm are shown. This picture reveals that we have structural Au atoms on Si; the Au atoms are deposited on substrate homogenously. The formation of multi crystalline with various patch sizes varying from approximately 100 to 200 nm can be the main source of various BH.

Figure 7(b) shows the topographical picture of deposited Au. Small holes in the surface will cause the variation in the current and will make the electrical behavior non ideal as mentioned we believe the rout of the various BH are the result from averaged and integrated properties of these individual patches.

5. C–V measurement

The barrier height was also calculated from the C–V characteristics. Figure 8(a) shows the C–V plot of the Au /p-Si contact at 1.0 MHz. In Schottky contacts, the depletion layer capacitance can be expressed from Eq. (6). Furthermore, as one can see from this expression, the C^{-2} versus V plot is a straight line whose intercept with the V axis gives the value of V_0. V_0 is the potential difference between the Fermi level and the top of the valence band in the neutral region of p-Si and can be calculated knowing the carrier concentration N_A and it is obtained from the Eq. (5) which is $N_A = 1.35\times10^{16}$ cm^{-3}.

The value of V_p was calculated from Eq. (6) to be $V_p = 0.172$ V. By extrapolating the plot in Fig. 8(b), the built in potential of the Au /p-Si contact was obtained as $V_{bi} = 0.5425$ V. Using Eq. (6), the barrier height value was calculated to be $\phi_b = 0.7145$ V for Au/p-Si.

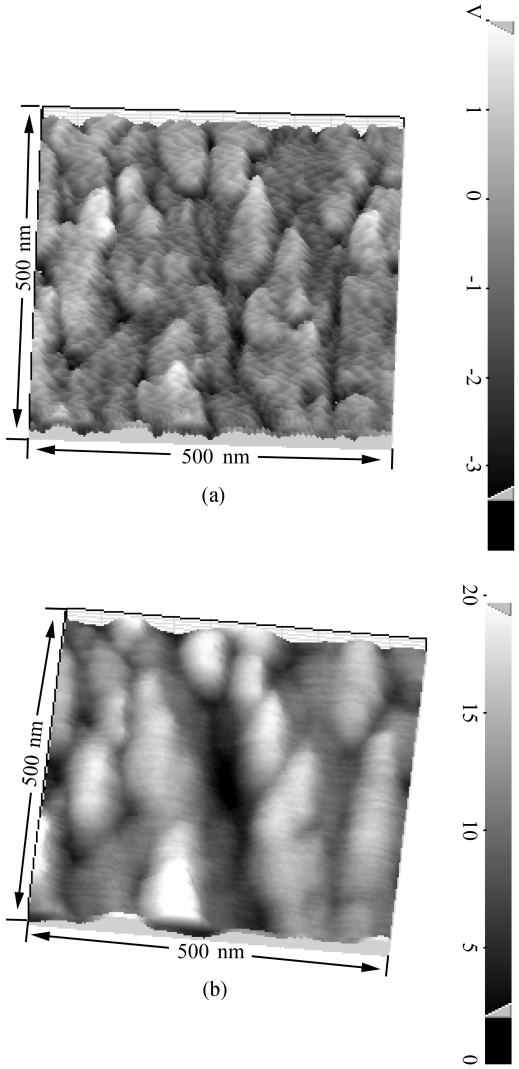

Fig. 7. (a) An AFM image of deposited Au, showing patches of approximately 100 to 200 nm which reveals that the structural Au Atoms on the Si substrate are formed and the Au atoms are deposited on substrate homogenously where multi crystalline with various patch sizes are noticed. (b) Topographical picture of deposited Au, where the small holes in the surface will cause the variation in current and will make the electrical behavior non ideal.

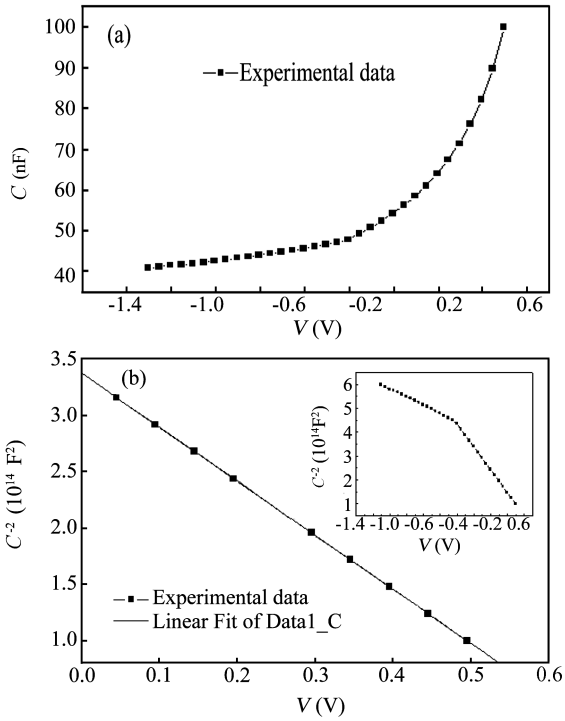

Fig. 8. (a) Capacitance–voltage (C–V) characteristics at room temperature for 100 μm sized Schottky contact at 1 MHz. (b) C^{-2}–V characteristics in forward and reverse biased region; the inset shows the linear regression curve in the reverse biased region.

6. Conclusion

In the present work by sing C-AFM an average BH of the whole contact was studied. In the manufacturing process after chemical processes by immediate and careful transferring of diodes to the coating device high quality semi-Schottky diodes were produced where their reverse leakage current was found to be extremely low, assuring a high quality rectifying behavior. We found an increasing BH with an increase in diameters and also an increase in ideality factor with decreasing diodes diameters where in contrast to larger diameter diodes the dependency of the ideality factor and BH to the sample diameter was not linear and derived an experimental relation for this new behavior. In the diodes with diameters smaller than 100 μm it is found that the dependency of potential barrier height to ideality factor is also nonlinear.

Investigation of electrical characteristics of the 5–100 μm diodes shows that by increasing the dimension, the potential barrier also increases such that it reaches from $\phi_b = 0.623$ V for 5 μm to $\phi_b = 0.791$ V for 100 μm. By decreasing the diode diameter, the ideality factor n increases and reaches from $n = 1.006$ in 100 μm diode to $n = 1.41$ in 5 μm diode. This shows that the diodes reach to their ideal whenever the dimension of the material decreases. Since each individual patch with 100 to 200 nm has its own defined parameter, the source of these different BH is the result of averaged properties of various patches.

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