# Current transport mechanisms in mercury cadmium telluride diode

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This paper reports the results of modelling of the current-voltage characteristics (I-V) of a planar mid-wave Mercury Cadmium Telluride photodiode in a gate controlled diode experiment. It is reported that the diode exhibits nearly ideal I-V characteristics under the optimum surface potential leading to the minimal surface leakage current. Deviations from the optimum surface potential lead to non ideal I–V characteristics, indicating a strong relationship between the ideality factor of the diode with its surface leakage current. Diode's I–V characteristics have been modelled over a range of gate voltages from −9 V to −2 V. This range of gate voltages includes accumulation, flat band, and depletion and inversion conditions below the gate structure of the diode. It is shown that the I–V characteristics of the diode can be very well described by (i) thermal diffusion current, (ii) ohmic shunt current, (iii) photo-current due to background illumination, and (iv) excess current that grows by the process of avalanche multiplication in the gate voltage range from −3 V to −5 V that corresponds to the optimum surface potential. Outside the optimum gate voltage range, the origin of the excess current of the diode is associated with its high surface leakage currents. It is reported that the ohmic shunt current model applies to small surface leakage currents. The higher surface leakage currents exhibit a nonlinear shunt behaviour. It is also shown that the observed zero-bias dynamic resistance of the diode over the entire gate voltage range is the sum of ohmic shunt resistance and estimated zero-bias dynamic resistance of the diode from its thermal saturation current. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4961601]

## I. INTRODUCTION

Gate controlled diode structures[1] have been used in the past as a tool in a semiconductor device technology to modulate the surface potential to study the surface related leakage current mechanisms in diodes. In HgCdTe technology too, several researchers[2–8] have used these structures to identify the conditions that would lead to high performance HgCdTe diodes with minimal surface leakage currents. Besides the discussions of optimum condition leading to minimal surface leakage currents, this paper intends to highlight a new aspect that has never been discussed before, namely, the dependence of ideality factor of the diode on the gate voltage/surface leakage currents. It is reported from a study of modelling of I–V characteristics over a large range of gate voltages that the ideality factor of the diode is near its value of unity for an ideal diode when surface potential of the diode has its optimum value corresponding to the minimal surface leakage current. Deviations of the surface potential from its optimum value result in the non-ideal I–V characteristics. The ideality factor of the diode exhibits an increasing trend with the increase of surface leakage current. The values exceeding above 2 have been observed for very high surface leakage currents.

## II. EXPERIMENTAL

A schematic diagram of the gate controlled diode used in this experiment is shown in Figure 1. Several diodes were fabricated on the vacancy doped epitaxial films of $Hg_{1-x}Cd_xTe$ ($x = 0.3019$) grown on the semi-insulating CdZnTe substrate by liquid phase epitaxy in the laboratory of Shanghai Institute of Technical Physics. Diodes were fabricated in n on p configuration by boron ion implantation using the usual photolithographic process. The passivation of the diode was carried out by coating its surface with 1000 Å thick thermally evaporated CdTe film followed by 3000 Å thick ZnS film. Metal layers of Sn (346 Å) and Au (853 Å) deposited by ion beam sputtering were used to form the gate electrode on ZnS and the contacts to HgCdTe.

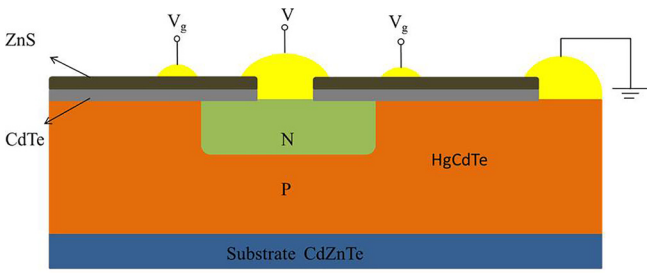


FIG. 1. Schematic side view of a mid-wave HgCdTe gate controlled diode structure.

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In addition to the gated diode, a MIS capacitor was also fabricated on the same wafer to evaluate the surface properties beneath the gate electrode. After the flip chip bonding, the fabricated sample was mounted in a low temperature Dewar for the measurement of its electrical characteristics. Next, the I–V characteristics of gated diode and capacitance-voltage (C-V) characteristics of the MIS capacitor were measured at a temperature of 82 K by a Keithley 4200 semiconductor parameter analyzer. As will be discussed later, the measured electrical characteristics were, however, not the true dark characteristics of the diode due to imperfect cold shielding in the measurement Dewar.

## III. CURRENT TRANSPORT MECHANISMS

This section provides a summary of the current transport mechanisms that have been used earlier[9–19] to model the dark electrical characteristics of the HgCdTe diodes. The well known mechanisms responsible for the transport of the dark current in a HgCdTe diode are (i) thermal diffusion current, (ii) generation-recombination (g-r) current, (iii) trap-assisted-tunnelling (TAT) current, (iv) band-to-band tunnelling current, (v) an ohmic component of current responsible for shunt like behaviour in the diodes, and (vi) avalanche multiplication current due to multiplication of the diffused carriers to the junction under the influence of applied electrical bias/electric field. In those cases where the measured electrical characteristics are not true dark characteristics, one more current, namely, the photo current generated by the background radiation received by the detector, also needs to be taken into account. In this paper, the relevant current transport equations are briefly described below.

### A. Thermal diffusion current ($I_{dif}$)

This component of the current is due to the diffusion of thermally generated minority carriers from the quasi-neutral n- and p-regions to the junction. It can be theoretically calculated from the following mathematical expression:[18,19]

$$I_{dif} = I_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right],$$
$$I_0 = Aqn_i^2\sqrt{\frac{kT}{q}}\left(\sqrt{\frac{\mu_n}{\tau_n}}\frac{1}{N_a} + \sqrt{\frac{\mu_p}{\tau_p}}\frac{1}{N_d}\right), \quad (1)$$

where $N_a$ and $N_d$ are, respectively, doping concentrations on the p and n-side of the junction, $n_i$ is the intrinsic carrier concentration, A is the junction area, $\tau_n$ is the electron lifetime, $\mu_n$ is the electron mobility, and $\tau_p$ and $\mu_p$ are, respectively, hole lifetime and hole mobility. V is the bias voltage across the diode. T, q, and k are, respectively, the temperature, electronic charge, and Boltzmann constant.

### B. Generation-recombination current ($I_{gr}$)

In this type of current, energy levels on account of the defects within the depletion region of the junction act as intermediate states (usually referred to as Shockley-Read or simply S-R centres) for the thermal generation and recombination of carriers. Sah, Noyce, and Shockley (SNS) analysed these currents and obtained the following equations:[20]

$$\mathbf{I_{g-r}} = \frac{qAn_iW}{\sqrt{\tau_{n0}\tau_{p0}}}\frac{\sinh\left(-\frac{qV}{2kT}\right)}{q\left[\frac{V_{bi}-V}{2kT}\right]}f(b), \quad (2)$$

where w is the depletion region width that is determined by

$$w = \left[\frac{2\varepsilon_0\varepsilon_s(V_{bi}-V)(N_A+N_D)}{qN_AN_D}\right]^{1/2}.$$

$V_{bi}$ is the built-in voltage of the p-n junction, $\varepsilon_0$ is the permittivity of free space, and $\varepsilon_s$ is the static dielectric constant of HgCdTe.

The function f (b) is defined by the following expression:

$$f(b) = \int_0^\infty \frac{du}{u^2+2bu+1},$$
$$b = \exp\left(-\frac{qV}{2kT}\right)\cosh\left[\frac{E_t-E_i}{kT} + \frac{1}{2}\ln\left(\frac{\tau_{p0}}{\tau_{n0}}\right)\right],$$

where $\tau_{n0} = \tau_{p0}$ is the effective lifetime in the depletion region, $E_t$ is the bulk trap energy level, and $E_i$ is the intrinsic energy level.

This g-r model[20] also predicts an apparent exp (qV/$\eta$kT) dependence of the forward current in a p-n junction. Here, $\eta$ is known as the ideality factor of the diode. As both diffusion and g-r currents are of thermal origin, the following simplified form is proposed to be used to describe the contribution of the currents of thermal origin ($I_{Th}$) in a junction,

$$I_{Th} = I_{sat}\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right]. \quad (3)$$

In the above equation, $I_{sat}$ is the thermal saturation current of the junction diode. The ideality factor $\eta$ will have a value of unity in diffusion current limited junctions. In junctions dominated by g-r currents, $\eta$ will have a numerical value of 2. According to g-r model,[20] the depletion region of these junctions is dominated by uniformly distributed single level Shockley–Read generation-recombination centres due to point defects. Still higher values of $\eta$ may also be observed[21] if the defects contributing to g-r currents are of complex nature.

### C. Trap assisted tunnelling (TAT) current

In this type of current, minority carriers tunnel from the quasi-neutral region to the empty band states on the other side of the junction via trap sites present in the depletion region of the junction. The major contribution of the TAT current is due to the tunnelling of the electrons via trap levels to the conduction band on the n-side. This current ($I_{TAT}$) is calculated using a simplified one dimensional model,[22]

$$I_{TAT} = \frac{\pi^2q^2AN_Tm_e\xi M^2}{h^3(E_g-E_t)}\exp\left\{-\frac{8\pi(2m_e)^{\frac{1}{2}}(E_g-E_t)^{\frac{3}{2}}}{3qh\xi}\right\}, \quad (4)$$

where $m_e$ is the effective mass of electrons in the conduction band, $E_g$ is the band gap, M is the matrix element associated with the trap potential, h is the Planck's constant, and $E_t$ is the position of trap level in the band gap measured from the top of valence band on the p-side. The most commonly used value of the quantity $M^2$ $(m/m_e)$ is $10^{-23}\,V^2\,cm^3$ for HgCdTe. The electric field strength $\xi$ across the depletion region is given by

$$\xi = \left(\frac{2qN_A(V_{bi}-V)}{\varepsilon_s\varepsilon_0}\right)^{\frac{1}{2}}.$$

In practical junctions, the electric field across the depletion region is variable from zero to a maximum value shown in the above equation. Normally, it is this maximum electric field that is used in the calculation of tunnelling currents.

### D. Band-to-band tunnelling current ($I_{BTB}$)

At relatively higher reverse bias voltages, the electrons may directly tunnel from the valence band on the p side to the conduction band on the n side of the junction under the influence of applied electric field $\xi$ across the depletion region of the diode. This current has been modelled in the past[13] using the simple approach outlined in Sze[23]

$$I_{BBT} = -\frac{Aq^3\sqrt{2m_e^*}\,\xi(V_{bi}-V)}{4\pi^3\hbar^2\sqrt{E_g}}\exp\left(-\frac{\pi\sqrt{m_e^*/2E_g^{3/2}}}{2q\xi\hbar}\right). \tag{5}$$

### E. Ohmic current ($I_{Sh}$)

The current–voltage characteristics of a narrow band gap material junction diode invariably contain a current component that can be calculated by applying the Ohm's law, i.e.,

$$I_{Sh} = \frac{V}{R_{Sh}}, \tag{6}$$

where V is the applied bias voltage and $R_{Sh}$ is the diode's shunt resistance. The surface leakage currents and the dislocations in the material, which intersect the junction,[24–26] are generally held responsible as a possible source of ohmic current. The contribution of ohmic currents from the two sources is not easily distinguishable. It is therefore modelled as gross contribution.

The calculation of the shunt current requires knowledge of the shunt resistance of the diode. The latter can be obtained by computing the diode's dynamic impedance (dV/dI) as a function of bias voltage. The highest (peak) value of dynamic resistance may be assumed as the shunt resistance of the diode. Note that dR/dV is zero at the peak of dynamic resistance versus voltage characteristic. Zero value of dR/dV physically signifies a resistance independent of the applied voltage, meaning a resistance that obeys Ohm's law, i.e., Ohmic shunt resistance $R_{Sh}$ of the given diode.

### F. Avalanche multiplication current

Under favourable conditions, the carriers diffusing to the edge of the depletion region of a p-n junction can undergo avalanche multiplication within the depletion layer under the influence of applied electric field. Relatively high quality junctions free from defects and dislocations and a wide depletion layer fall under this category. The avalanche multiplication current ($I_{AVM}$) is given by

$$I_{AVM} = M[I_{dif} + I_{Ph}]. \tag{7}$$

In the above equation, the voltage dependent multiplication factor M is given by

$$M = \frac{1}{(1-\alpha_e W)}. \tag{8}$$

The electron impact ionization coefficient ($\alpha_e$) is given by[27–29]

$$\alpha_e = \alpha_0 \exp\left(-\frac{b}{\xi}\right)^m. \tag{9}$$

The electric field ($\xi$) across the depletion region is same as already defined above.

In Equation (9), $\alpha_0$ and m are empirical fitting parameters.

### G. Effect of Illumination on current-voltage characteristics

The measurements of I–V characteristics of a HgCdTe diode are usually carried out at liquid nitrogen temperature by mounting it on a cold mount within a vacuum system/Dewar. If the cold shield within the measurement system is imperfect, then the incident background radiation on the diode results in the generation of photo-current ($I_{Ph}$) that consists of minority carriers. The net effect is to modify the forward characteristic of the diode that can be described by rewriting Equation (3) in the following form:

$$I_{Th} = I_{sat}\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right] - I_{Ph}. \tag{10}$$

As compared to dark, the background illuminated I–V characteristics of the diode get shifted along the current axis towards the negative values of the current by an amount equal to the value of photo-excited minority carrier current, $I_{Ph}$. Correspondingly, there is a shift in the forward characteristics along the voltage axis towards positive voltages by an amount equal to the open circuit voltage, $V_{OC}$. The following expression for $V_{OC}$ is obtained by setting the net forward junction current ($I_{Th}$) equal to zero,

$$V_{OC} = \frac{\eta kT}{q}\ln\left[\frac{I_{Ph}}{I_{sat}} + 1\right]. \tag{11}$$

In practice, the experimental values of photo-current $I_{Ph}$ and open circuit voltage $V_{OC}$ are known from the measured I–V characteristics. The thermal saturation current ($I_{sat}$) of the diode can be therefore estimated by fitting its measured forward characteristic to Equations (10) and (11) by treating the ideality factor $\eta$ as a variable parameter. However, if $V_{OC}$ is

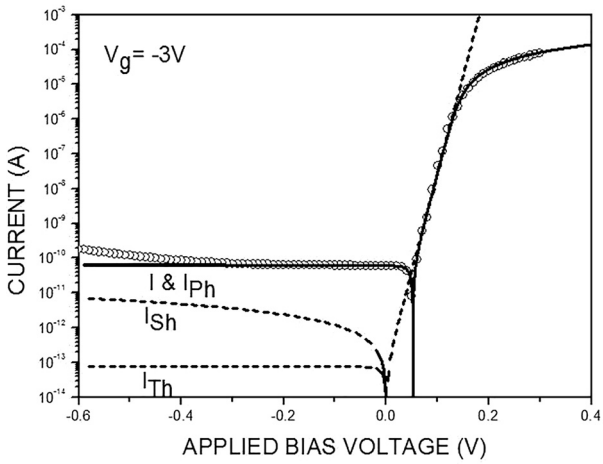


FIG. 2. Measured (open circles) current-voltage characteristics of mid-wavelength HgCdTe gated diode at 82 K for a gate voltage of −3 V. Continuous lines are the best fit of the theory to the experimental data. Broken line in the forward bias is the dark characteristic in the absence of series resistance of the diode. Broken lines in the reverse bias correspond to the calculated current contribution as marked on each of them. The resultant contribution shown by continuous line and marked by I is the sum of thermal ($I_{Th}$), ohmic shunt ($I_{Sh}$), and photo-currents ($I_{Ph}$).

not accurately known due to its small value or inappropriate measurement conditions, then the ideality factor $\eta$ and open circuit voltage $V_{OC}$ both need to be treated as the variable fitting parameters[30] whose values remain connected with each other through Equation (11). This paper will be discussing an example of a gated diode in which the open circuit voltage $V_{OC}$ is variable with the gate voltage $V_g$. As will be seen later, the highest open circuit voltage corresponds to the minimal surface leakage current. With the increase in the surface leakage current, open circuit voltage tends to decrease to negligibly a small value. The fitting of the experimental data to the theory will be thus carried out by treating both $\eta$ and $V_{OC}$ as variable parameters. While fitting the forward characteristics, the series resistance of the diode will be taken care of by using the following expression:

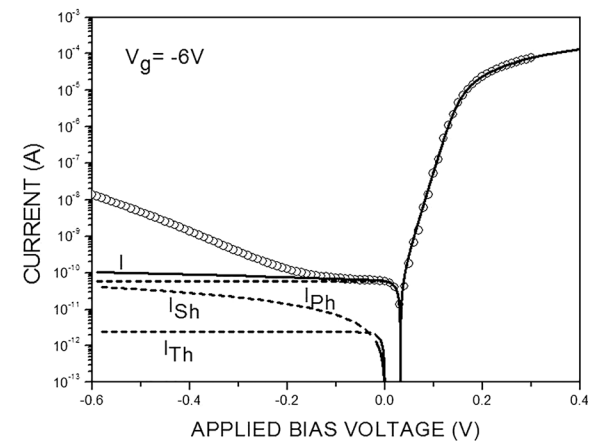


FIG. 3. Measured (open circles) current-voltage characteristics of mid-wavelength HgCdTe gated diode at 82 K for a gate voltage of −6 V. Continuous lines are the best fit of the theory to the experimental data. Broken lines in the reverse bias correspond to the calculated current contribution as marked on each of them. The resultant contribution shown by the continuous line and marked by I is the sum of thermal ($I_{Th}$), ohmic shunt ($I_{Sh}$), and photo-currents ($I_{Ph}$).

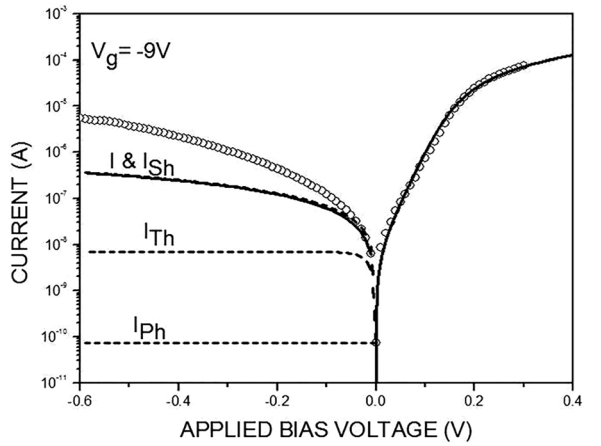


FIG. 4. Measured (open circles) current-voltage characteristics of mid-wavelength HgCdTe gated diode at 82 K for a gate voltage of −9 V. Continuous lines are the best fit of the theory to the experimental data. Broken lines in the reverse bias correspond to the calculated current contribution as marked on each of them. The resultant contribution shown by the continuous line and marked by I is the sum of thermal ($I_{Th}$), ohmic shunt ($I_{Sh}$), and photo-currents ($I_{Ph}$).

$$V_{appl} = V + I_{Th}.R_{sr}, \tag{12}$$

where $V_{appl}$ is the externally applied voltage, V is the voltage across junction, and $R_{sr}$ is the series resistance of the diode.

## IV. RESULTS AND DISCUSSIONS

The measured I–V characteristics of the gated diode are shown in Figures 2–5 by open circles. The respective gate voltages ($V_g$) are marked on each of the figures. Initially, the measured forward characteristics shown in Figures 2–5 were subjected to the best fit to Equations (10)–(12) by using the experimentally known value of the photocurrent ($I_{Ph}$) and treating the ideality factor $\eta$ and open circuit voltage $V_{OC}$ as variable fitting parameters. The series resistance ($R_{sr}$) of the

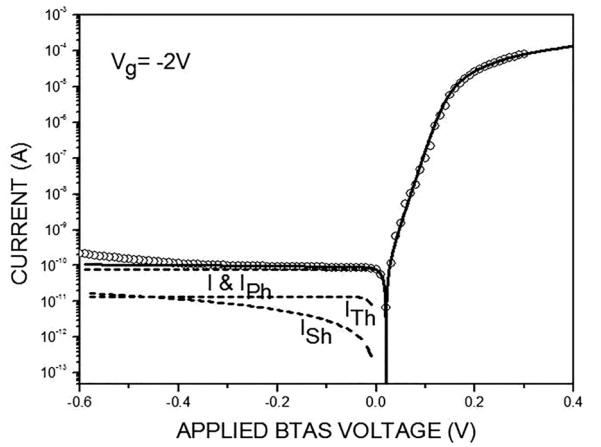


FIG. 5. Measured (open circles) current-voltage characteristics of mid-wavelength HgCdTe gated diode at 82 K for a gate voltage of −2 V. Continuous lines are the best fit of the theory to the experimental data. Broken lines in the reverse bias correspond to the calculated current contribution as marked on each of them. The resultant contribution shown by the continuous line and marked by I is the sum of thermal ($I_{Th}$), ohmic shunt ($I_{Sh}$), and photo-currents ($I_{Ph}$).

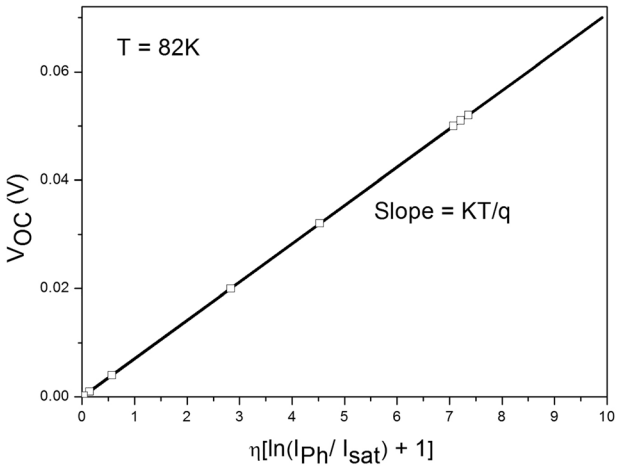


FIG. 6. Plot of open circuit voltage $V_{OC}$ versus the product $\eta[\ln(I_{Ph}/I_{sat})+1]$. The slope of the continuous line is kT/q. Open circles are the calculated points using the fitted values of $\eta$ and $V_{OC}$ obtained by fitting the forward I–V characteristics of the diode at each gate voltage.

diode is 1700 Ω. Primarily for a known value of $I_{Ph}$, the numerical values of $\eta$ and $V_{OC}$ determine the variation of the current in the low forward bias region. Similarly, $R_{sr}$ limits the current in the higher forward bias region. The continuous lines in Figures 2–5 are the best fit of the experimental data to the theory. The forward characteristic shown by the broken line in Figure 2 is diode's calculated dark characteristic without taking into account the effect of series resistance. It is shown here for the sake of comparison to effectively highlight the shift of forward characteristic of the diode towards positive voltages under the influence of background illumination. It can be observed from Figures 2–5 that $V_{OC}$ varies with the variation in gate voltage. The variation of the open circuit voltage, $V_{OC}$ as a function of the product $\eta[\ln(I_{Ph}/I_{sat})+1]$, is shown in Figure 6 by open squares. The continuous line with a slope of kT/q in this figure validates the fitted values of $\eta$ and $V_{OC}$, according to Equation (11). The variation in the ideality factor $\eta$ and open circuit voltage $V_{OC}$ as a function of applied gate voltage to the diode is, respectively, shown in Figures 7 and 8 and is discussed in the following paragraph.

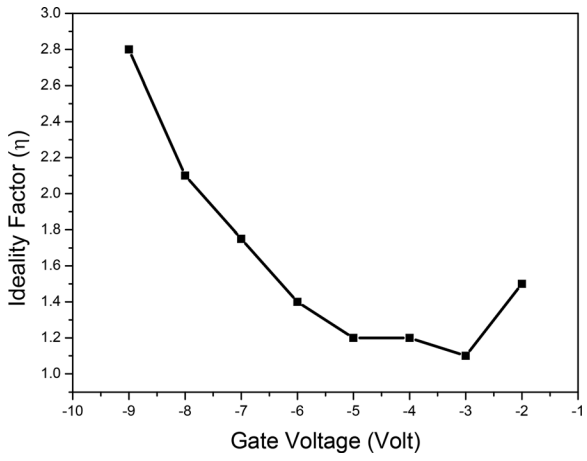


FIG. 7. Variation of the Ideality factor ($\eta$) of the diode as a function of gate voltage.

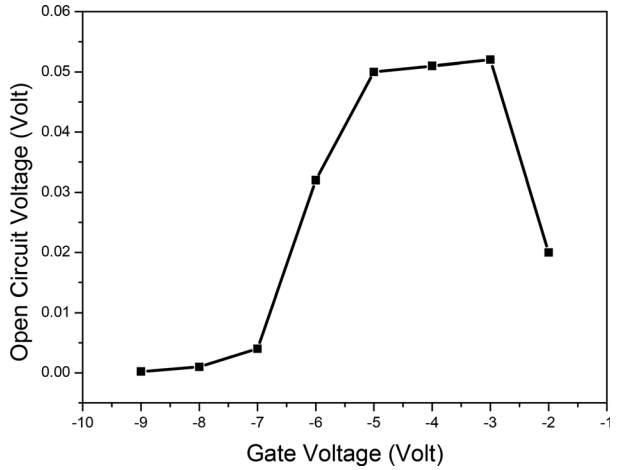


FIG. 8. Variation in the open circuit voltage ($V_{OC}$) of the diode as a function of gate voltage.

It may be observed from Figure 7 that the ideality factor $\eta$ of the diode exhibits variation as a function of gate voltage. Numerically, its value changes from its ideal value of nearly unity to a high value of 2.8. One of the obvious consequences of this observation from the present experiment is that the changes in surface potential accompanied with the variations in surface leakage currents are responsible for inducing variations in the ideality factor of the diode. It will be further discussed later that the nearly unity value of the $\eta$ is obtained under optimum passivation condition of minimum surface leakage current, which corresponds to the deeply depleted HgCdTe-passivant interface. Thus, a nearly unity ideality factor of the diode at a gate voltage of $V_g = -3$ V may be interpreted as indicating the mere absence or negligibly small number of Shockley-Read centres[20] in the depletion region of the junction and surface/interface too. In other words, the contribution from g-r currents may be ruled out in the present case, which means that the observed thermal current contribution is dominated by diffusion mechanism. Absence of the g-r current means the negligible number of point/complex defects in the depletion region of the diode. Thus the TAT currents too, which owe their origin to the existence of traps due to the defects in the depletion region, may be ruled out.

Having ruled out the contribution from g-r and TAT mechanisms in the preceding paragraph, we will now discuss the modelling of reverse bias characteristics of the diode shown in Figures 2–5. The thermal saturation current ($I_{sat}$) of the diode at each gate voltage is already known from its respective forward characteristic. It is then straightforward to calculate the thermal current components from Equation (10) that are shown by the broken lines marked with the letter $I_{Th}$ in Figures 2–5. The broken line marked with $I_{Sh}$ is the ohmic shunt current of the diode calculated using the estimated ohmic shunt resistance from the computed dynamic resistance characteristic of the diode as already discussed in Section III E. The photo-current $I_{Ph}$ is an experimentally known component of the current corresponding to the zero-bias current of the diode. The continuous line marked by I is the sum of photo-current, and thermal and ohmic shunt

currents. It can be noted from Figures 2–5 that the experimentally measured current indicated by circles is in agreement with the theoretically calculated current I in the low reverse bias range. The diode under investigation, however, exhibits an excess current in the higher reverse bias region that can be calculated from the following Equation (13):

$$I_{excess} = I_{expt} - I_{Th} - I_{Sh} - I_{ph}. \tag{13}$$

In the past, the above mentioned excess current in the low and medium reverse bias regions of the I–V characteristics of HgCdTe diodes has been interpreted[9–19] as the contribution of TAT currents that were discussed in Section III C. However, as already discussed above, the contribution from TAT currents is to be ruled out in the present case. Alternatively, the above calculated excess current can be very well described[30–32] by the following exponential function:

$$I_{excess} = I_{r0} + K_1 \exp(K_2 V), \tag{14}$$

where $I_{r0}$, $K_1$, and $K_2$ are the fitting parameters.

It has been reported earlier[30–32] that the fit of the excess current to Equation (14) yields positive sign of the first term and a negative sign for the second term. This means that during the growth of excess current both majority and minority carriers are produced. The second (exponential) term in Equation (14) exhibits the growth of minority carrier current, which can be mathematically obtained if the excess current grows in its own proportion, i.e.,

$$\frac{dI_{excess}}{dV} \propto I_{excess} \tag{15}$$

or

$$\int_{K_1}^{I_{excess}} \frac{dI_{excess}}{I_{excess}} = \int_0^V K_2 dV. \tag{16}$$

$K_2$ is the proportionality constant. Integration limits in the above equation mean the growth of excess current from an unknown value $K_1$ at zero bias voltage to $I_{excess}$ at the highest applied voltage $V$.

Equation (16) leads to the exponential term (second) of Equation (14).

The above mathematical derivation suggests that a process in which the current develops in its own proportion and results in the production of electron-hole pairs may be responsible for the growth of excess current. Physically, this process appears similar to the growth of the diode current by avalanche multiplication process. Alternatively, if the origin of excess current is associated with the shunt current of the diode, then the exponential growth of excess current indicates the nonlinear behaviour of shunt current/surface leakage current.

A plot of the calculated excess current from Equation (13) is shown in Figure 9 as a function of the applied bias and gate voltages to the diode. Figures 9(a) and 9(b), respectively, correspond to the range of gate voltages from −2 to −5 V and −5 to −9 V. Continuous lines are the best fit of the excess current data to Equation (14). It may be noted from Figure 9 that Equation (14) provides an excellent fit to the excess current of the diode over the entire range of applied bias voltages as well as gate voltages to the diode. Based on the discussions in the preceding paragraph, it can be said that the excess current of the diode may have grown by the avalanche multiplication process. It may also be recalled here that the depletion layer of the diode under discussion was already concluded above to be free from defects, which is a favourable condition for the avalanche multiplication process. It may be thus interesting to apply the theory of avalanche multiplication discussed in Section III F to the experimental data in the present case.

In diodes that have a component of shunt current, equation (7) can be rewritten as follows:

$$I_{exp} = M[I_{dif} + I_{Ph}] + \mathrm{I_{Sh}}. \tag{17}$$

In the absence of g-r current contribution $\mathrm{I_{dif}} = \mathrm{I_{Th}}$, the multiplication factor will be therefore determined by

$$M = \frac{I_{exp} - I_{Sh}}{I_{Th} + I_{Ph}}. \tag{18}$$

Equation (8) can be thus used in the following form:

$$\alpha_e w = \frac{M-1}{M}. \tag{19}$$

The following modified form of Equation (9) in terms of the applied bias voltage across the diode has been previously used[32] in case of background illuminated I–V characteristics,

$$\alpha_e \mathrm{w} = \alpha_{\mathrm{we}} \exp\left(-\frac{b}{\mathrm{V}}\right). \tag{20}$$

In the above equation, $\alpha_{\mathrm{we}}$ is a dimensionless parameter and b is in volts. The right hand side term of Equation (20) essentially represents the growth of minority carriers (electrons in

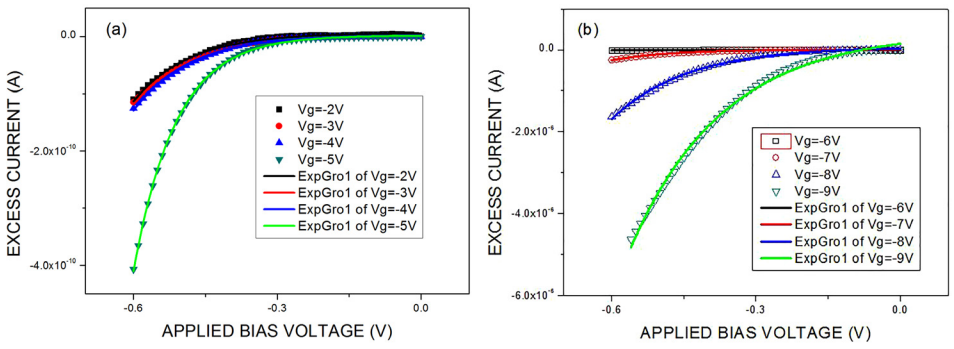


FIG. 9. Excess current versus applied bias voltage as a function of gate voltage ($V_g$). Discrete points show the calculated excess current from Equation (13) as a function of gate voltage, (a) $V_g = -2$ V, −3 V, −4 V, and −5 V and (b) $V_g = -6$ V, −7 V, −8 V, and −9 V. Continuous lines show the best fit of excess current data to Equation (14).

the present example). In the avalanche multiplication process, electron-hole pairs are generated. Thus to include the contribution of majority carriers (holes), Equation (20) will be used in the following form:

$$\alpha_e \mathrm{w} = \alpha_{\mathrm{wh}} + \alpha_{\mathrm{we}} \exp\left(-\frac{b}{\mathrm{V}}\right). \tag{21}$$

The constants $\alpha_{\mathrm{wh}}$, $\alpha_{\mathrm{we}}$, and b can be obtained by fitting the experimental data to Equation (21). Here, $\alpha_{\mathrm{wh}}$ represents the hole/majority carrier contribution.

Figures 10 and 11 are the plots of calculated $\alpha_e$w from Equation (19) versus the inverse of applied bias voltage to the diode by discrete points (circles). The continuous lines show the best fit of Equation (21) to the experimental data. The corresponding gate voltage is marked on each figure. It is observed that the theory of avalanche multiplication outlined above agrees well with the experiment at a gate voltage of −3 V. Similar agreement was also observed for gate voltages of −4 V and −5 V. However, it is clear from Figure 11 that the theory of avalanche multiplication does not agree with the experimental data at a gate voltage of −6 V. It is worth noting here that the gate voltage range from −3 V to −5 V corresponds to the minimal surface leakage currents. Whereas for negative gate voltages above −5 V, the ideality factor $\eta$ begins to increase (see Figure 7) and the open circuit voltage $V_{OC}$ decreases (Figure 8) due to the increasing surface leakage current. It is also shown in Figure 12 that zero-bias dynamic resistance of the diode exhibits a continuously decreasing trend for negative gate voltages above −5 V. This means that for higher negative gate voltages the current passing through the junction decreases and the current flowing via surface leakage current/shunt resistance path increases. Since in this gate voltage range ($-9\,\mathrm{V} < V_g < -5\,\mathrm{V}$), the avalanche multiplication of the current within the depletion region is not observable, the excess current may be alternatively growing along the shunt resistance path, which, in the present case, is the localized path of surface leakage current. As the growth of excess current can still be described very well by the exponential equation (14), we are observing the nonlinear shunt behaviour of surface leakage current. This observation shows that the small surface leakage currents can only be modelled as ohmic shunt currents. Whereas the higher surface leakage currents exhibit nonlinear shunt behaviour.

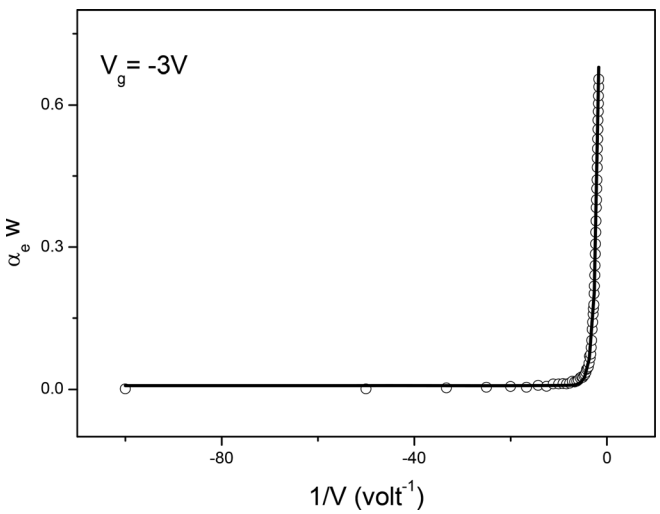


FIG. 10. Plot of $\alpha_e$W versus inverse of applied bias voltage at the gate voltage $V_g = -3$ V. Continuous line is the best fit of the experimental data to Equation (21) describing the avalanche multiplication of carriers within the depletion region.

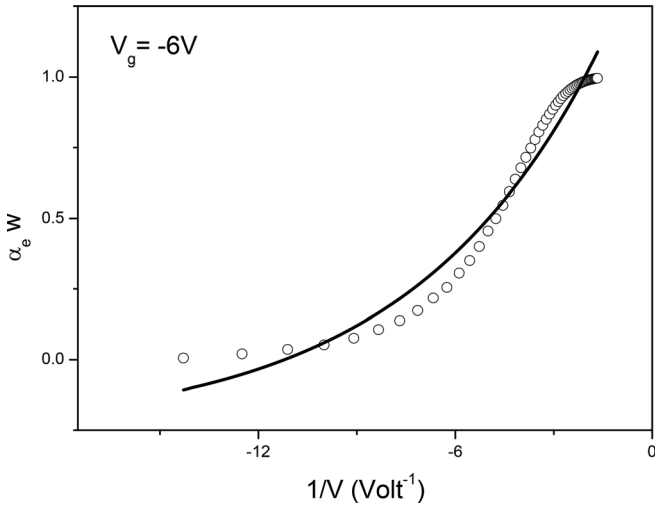


FIG. 11. Plot of $\alpha_e$W versus inverse of applied bias voltage at the gate voltage $V_g = -6$ V. Continuous line is the best fit of the experimental data to Equation (21).

Next, it may be observed from Figures 2–5 that the current mechanisms contributing to the diode current near zero bias are the thermal and shunt currents. The observed resultant zero-bias dynamic impedance of the diode will be then given by

$$\frac{1}{R_0} = \frac{1}{(R_{Th})_0} + \frac{1}{R_{Sh}}. \tag{22}$$

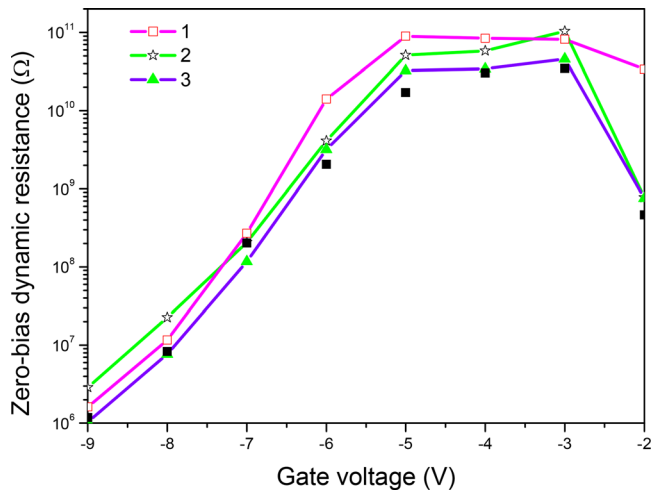


FIG. 12. Variation of zero-bias dynamic resistance of the diode as a function of gate voltage. Closed square points show the experimentally observed zero-bias dynamic resistance of the diode. Lines marked with the numbers 1 and 2 show the variation of shunt resistance ($R_{Sh}$) and calculated zero-bias resistance of the diode on account of the thermal current contribution $(R_{Th})_0$. Line marked with the number 3 shows the variation of resultant zero-bias dynamic resistance ($R_0$) of the diode.

In the above equation, shunt resistance $R_{Sh}$ may be assumed as the ohmic shunt resistance due to the small magnitude of shunt current near zero-bias. Contribution of thermal currents to the zero-bias resistance $(R_{Th})_0$ of the diode can be obtained from the thermal saturation current $I_{sat}$ of the diode as

$$(R_{Th})_0 = \frac{\eta kT}{qI_{Sat}}.$$

In Figure 12, points (closed squares) show the experimentally observed zero-bias dynamic resistance of the diode. Line marked with the number 1 is the ohmic shunt resistance ($R_{Sh}$) of the diode that was estimated from the peak dynamic resistance ($dR/dV = 0$) of the diode in its computed dynamic resistance characteristic as already discussed in Section III E. Line marked with the number 2 shows the thermal current contribution $(R_{Th})_0$ to the dynamic resistance of the diode, which has been calculated from the thermal saturation current $I_{Sat}$. The resultant zero-bias dynamic resistance of the diode on account of thermal and ohmic shunt current contributions is shown by the line marked with the number 3. It can be observed that the line marked as 3 is in good agreement with the experimental data. This shows that the experimentally observed zero-bias dynamic resistance of the diode over the entire gate voltage range ($-9\,V < V_g < -2\,V$) is the sum of ohmic shunt resistance and estimated zero-bias dynamic resistance of the diode from its thermal saturation current.

Figures 7, 8, and 12, respectively, show the observed variations in the ideality factor $\eta$, open circuit voltage $V_{OC}$, and zero-bias dynamic resistance $R_0$ as a function of the applied gate voltage to the diode. The following similarities may be noticed in regard to the variations of these three parameters with respect to the gate voltage.

$-9\,V < V_g < -5\,V$: In this gate voltage range, all the three parameters exhibit relatively fast variation. It is observed that $\eta$ decreases, whereas $V_{OC}$ and $R_0$ increase with the variation of gate voltage from $-9\,V$ to $-5\,V$.

$-5\,V < V_g < -3\,V$: In this gate voltage range, all the three parameters exhibit a plateau with very small change in their numerical values. It is interesting to note here that the experimentally observed $R_0$ and $V_{OC}$ are near to their maximum value and the ideality factor $\eta$ of the diode is near to its minimum value of unity for $V_g = -3\,V$. This range of gate voltage should be thus interpreted as the optimum condition for the operation of the diode. At the same time, the physical conditions existing at the HgCdTe-passivant interface corresponding to this gate voltage range may give us an idea of the optimum conditions that are required to be achieved during passivation of HgCdTe detectors and arrays.

$Vg > -3\,V$: $\eta$ exhibits an increasing trend, whereas $V_{OC}$ and $R_0$ exhibit a decreasing trend.

The physical conditions of the HgCdTe-passivant interface that have led to the optimum passivation in the present example can be understood by examining the capacitance-voltage (C-V) characteristics of MIS capacitor corresponding to the structure of gate electrode. Figure 13 shows the normalized high frequency (1 MHz) C-V characteristics of the gate capacitor. The capacitance corresponding to flat band

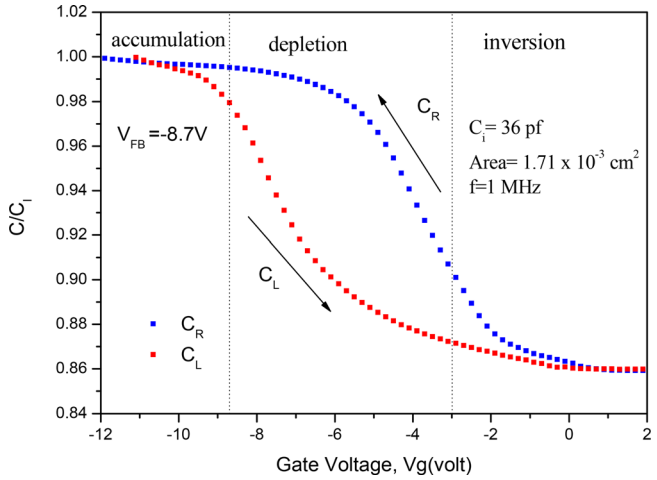


FIG. 13. Measured high frequency (1 MHz) capacitance-voltage characteristics of MIS capacitor of gate structure.

condition is $0.983\,C_i$, where $C_i$ (=36 pF) is the capacitance of insulation layer. The position of the flat band voltage $V_{FB}$ in this case corresponds to a gate voltage of $-8.7$ V. The relatively fast decrease in the capacitance of the MIS capacitor from $-8.7$ V to $-3$ V indicates the increasing depletion layer width below the gate electrode. The entire region of gate voltages from $-8.7$ V to $-3$ V is thus identified as the depletion region. The plateau region between $-5\,V < V_g < -3\,V$ in Figures 7, 8, and 12 is the deep depletion region in which the depletion width below the gate changes to a small degree only with the change of gate voltage. $V_g > -3$ V range corresponds to the inversion region. The gate voltage range $V_g < -8.7$ is the accumulation region.

According to the above assessment of the HgCdTe-passivant interface, the optimum passivation that results in the minimal surface leakage currents occurs for a deeply depleted semiconductor-insulator interface just before the onset of inversion. These findings are in full agreement with the earlier reported[7] results and can be physically understood as explained in the following paragraph.

It is known[33] that the surfaces/interfaces with flat bands are marked by very high recombination velocities. In the absence of band bending, both electrons and holes have an equal probability to diffuse to the surface/interface and recombine over there. High recombination velocity at the surface/interface leads to a low shunt resistance or a high shunt current. High surface recombination velocity further leads to the degradation of minority carrier lifetime in the base of the diode.[17] On the other hand, a deeply depleted interface at the optimum gate voltage of $-3$ V has a minimal carrier recombination velocity on account of band bending that opposes the diffusion of holes to the interface. Thus, the shunt resistance and minority carrier lifetime are highest at the optimum gate voltage. Thus, the increasing trends of $V_{OC}$ (Figure 8) and zero-bias thermal resistance and shunt resistance (Figure 12) can be clearly understood on the basis of increase in the shunt resistance and improvement in minority carrier lifetime with the change of gate voltage from $-9$ V to $-3$ V. The increasing trend of the ideality factor $\eta$ (Figure 7) with the change of gate voltage

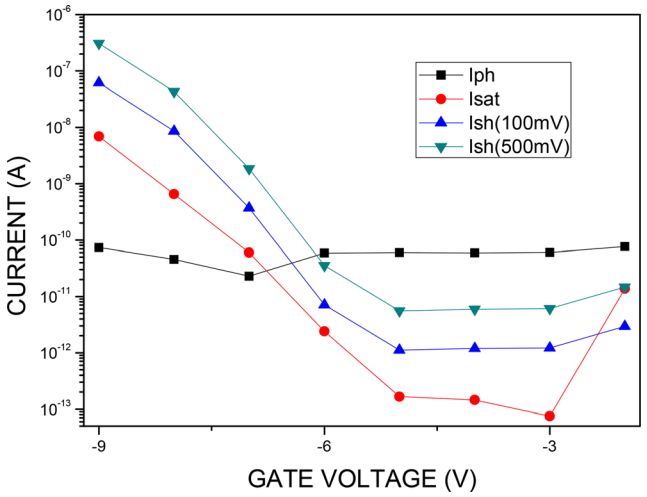


FIG. 14. Current components of the diode as a function of gate voltage.

from −3 V to −9 V is related to the increase of surface leakage current.

Above, we have discussed the variation of $\eta$, $V_{OC}$, and $R_0$ up to the optimum voltage of −3 V. The HgCdTe-passivant interface beneath the gate is inverted, if $V_g > -3$ V. Thus at a gate voltage of −2 V, the diode begins to collect more thermal current from the volume of the material around the periphery of the diode. The increase in the thermal current decreases the open circuit voltage as well as zero-bias resistance of the diode as seen in Figures 8 and 12. The increase in the ideality factor may be again related to the increasing surface leakage current.

Figure 14 presents a summary of the operative current components of the diode that are part of the observed variation of I–V characteristics of the gated diode. It may be noted that the photo-current is an experimentally measured parameter, which is practically independent of gate voltage. The variations in thermal and ohmic shunt currents show that these currents are near their minimum values in the optimum gate voltage region, which is the result of minimal surface recombination and high minority carrier lifetime. Similarly, the high values of thermal and ohmic shunt currents towards the flat band voltage condition are the result of high surface recombination and degraded minority carrier lifetime. It can also be observed from Figure 14 that the shunt current is relatively constant between the gate voltages from −3 V to −5 V. On either side of this range, the shunt current exhibits an increasing trend. For $V_g < -5$ V, it increases rather rapidly. The growth of excess current for $V_g < -5$ V was concluded above to be taking place along the shunt resistance/surface leakage current path.

## V. SUMMARY AND CONCLUSIONS

This work has presented the results of a gated diode experiment on a mid-wavelength HgCdTe diode. I–V characteristics of the diode were modelled to investigate the current transport mechanisms of the diode as a function of gate voltage. It has been shown that the ideality factor $\eta$ of the diode is strongly dependent on the surface leakage currents. Higher the surface leakage current, higher is the $\eta$ of the diode. The highest reported ideality factor in the present case is 2.8. This work has also shown that the minimal surface leakage currents are obtained for a deeply depleted HgCdTe-passivant interface just before the onset of inversion. The ideality factor is near its unity value for an ideal thermal diffusion current limited diode when the surface leakage currents are minimal. Under the ideal conditions, I–V characteristics of the diode can be very well described by (i) thermal diffusion current, (ii) ohmic shunt current, (iii) photo-current due to background illumination, and (v) excess current that grows by the process of avalanche multiplication within the depletion layer of the junction. Outside the optimum gate voltage range, the ideality factor of the diode increases with the increase in surface leakage current. The excess current in the reverse characteristics grows exponentially in its own proportion along the shunt current path, which is the localized path of surface leakage current. It has also been reported that the ohmic current model applies only to small surface leakage currents. The higher surface leakage currents exhibit nonlinear shunt behaviour. It is also shown that the observed zero-bias dynamic resistance of the diode is the resultant contribution of thermal diffusion and ohmic shunt currents. Based on the present work, it may be concluded that the higher surface leakage currents in a diode may lead to non-ideal behaviour of its I–V characteristics.

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