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Surface Photovoltage Spectroscopy as a Valuable Tool for Evaluating Oxidation Processes in the Microelectronics Industry

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In the present study, the minority carrier diffusion length (MCDL), determined by surface photovoltage spectroscopy measurements, is compared in n- and p-type Si wafers after their oxidation under different conditions using various tools (horizontal and vertical furnaces, atomic layer deposition (ALD), low-pressure chemical vapor deposition, and plasma-enhanced chemical vapor deposition). It is shown that MCDL varies significantly depending on the design of furnaces, oxidation temperatures, the type of gases used before and during oxidation, and their flow ratios. The type and crystal growth method of Si wafers used for the oxidation also play a significant role and influence MCDL. Additionally, MCDL after the deposition of alumina layers using ALD techniques is found to be significantly larger compared to that observed after the thermal oxidation of Si. The larger values of MCDL after the ALD of Al_2O_3 are detected independent of temperature and precursors used for the deposition. The origin of different MCDL values after various oxidation processes, with an emphasis on the formation of electrically active defects in Czochralski (CZ)- and float-zone (FZ)-grown Si wafers is discussed.

1. Introduction

High-temperature oxidation processes are widely used for forming gate oxides and isolating different parts of Si-based devices in the microelectronics industry. However, achieving such high temperatures becomes challenging for many technologies, especially those already containing metal layers. Therefore, also insulators deposited at significantly lower temperatures (around 200–400 °C), such as plasma-enhanced USG layers, LP-USG layers, or atomic layer deposition (ALD), are often employed in microelectronic devices.

During oxidation processes, various impurities could be unintentionally introduced into Si, acting as generation-recombination centers. Control over the purity of oxidation processes becomes of prime technological importance and is a necessary step for the reliable production of semiconductor devices. Such defects may significantly influence the minority carrier diffusion length (MCDL) and, consequently, the electrical properties of semiconductor devices. Thus, metallic impurities with a concentration of about $5 \times 10^{10}\,cm^{-3}$ could already significantly reduce MCDL in n- and p-type Si.[1–3] Several potential sources of contamination could be generally distinguished. Both Chochralski (CZ)- and float-zone (FZ)-grown Si wafers contain carbon and oxygen which are introduced during the growth. The concentration of these impurities depends significantly on the growth method and growth conditions which are different by different suppliers. While these impurities are generally electrically inactive, their pairing, especially in the presence of hydrogen inevitably present in different forms in Si, could lead to the formation of several defects with levels in the band gap of Si.[4–12] Different parts of oxidation tools and the gases used during the oxidation process might be another source of contaminations. In modern microelectronics labs and clean rooms, the contamination level is often monitored in oxidized wafers by total X-Ray fluorescence (TXRF) and vapor phase decomposition inductively coupled plasma – mass spectrometry (VPD-ICPMS) measurements. Such measurements are well suited for the analysis of impurities in SiO_2 or at the surface of Si. However, their detection limit varies significantly depending on the nature of elements, and for several of them it could be already too high for reliable functioning of semiconductor devices. In addition, TXRF and VPD-ICPMS cannot resolve whether the impurities are electrically active in Si and their application is strongly limited for the investigation of defects in high-k oxides. Both these techniques are also quite expensive and after them the oxidized wafers cannot be usually used in the production.

In this study, our recent findings about the evaluation of oxidation processes performed under different conditions in different tools by using surface photovoltage spectroscopy (SPV) measurements are summarized. In contrast to TXRF and VPD-ICPMS measurements, SPV is a contactless and

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non-destructive method, which could detect electrically active defects with a concentration of about 10^9–10^{10} cm^{-3} in Si. MCDL in Si wafers oxidized with thermal oxide are compared with those observed after the deposition of alumina layers, which are widely used as passivation layers in different semiconductor devices. The observed results will be discussed with an emphasis on the formation of different electrically active defects.

2. Results and Discussion

Figure 1 displays typical MCDL wafer maps recorded on different wafers (FZ p-type Si (a), CZ p-type Si (band d), and CZ n-type Si (c)) after wet oxidation at 960 °C in a vertical furnace. All average MCDL values recorded on these wafers are compiled in **Table 1**. The average MCDL value in FZ p-type Si is 427 ± 69 µm (Figure 1a), which is larger than the values observed in CZ p-type Si wafers but lower than those in CZ n-type Si. Additionally, MCDL values observed in wafers after oxidation with a loading (unloading) temperature of 600 °C are significantly lower than those detected at a higher loading (unloading) temperature of 750 °C. Another noteworthy feature of the oxidation in a vertical furnace is a circular pattern in the MCDL wafer map recorded in p-type Si wafers, independent of their growth type. Such a pattern was not observed in CZ n-type Si wafers.

Figure 2 displays MCDL wafer maps recorded on different wafers (CZ n-type Si (a) and FZ p-type Si (b)) after wet oxidation at 960 °C in a horizontal furnace. The average MCDL values

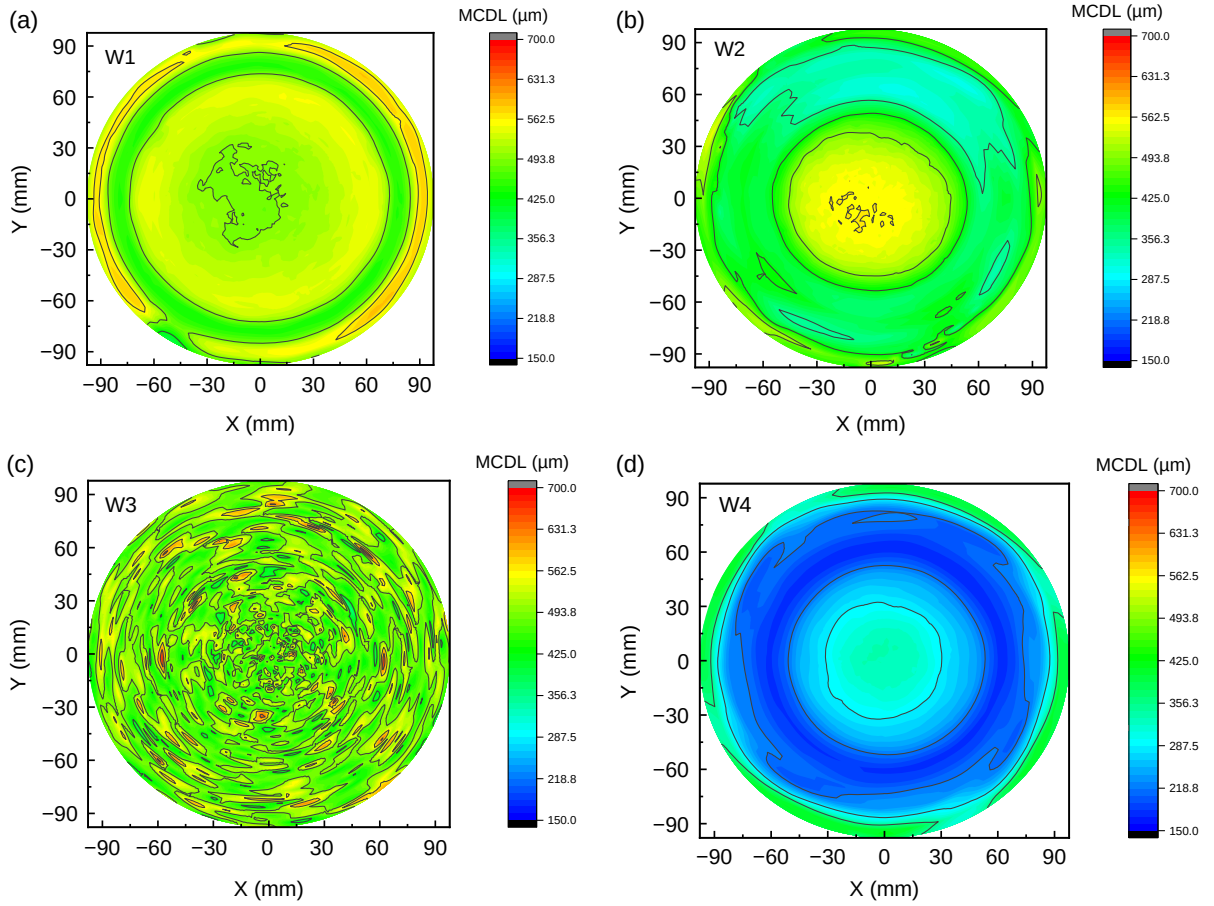

Figure 1. MCDL wafer maps were recorded on various wafers, including a) FZ p-type Si, b,d) CZ p-type Si, and c) CZ n-type Si, following wet oxidation in a vertical furnace. The loading (unloading) temperature was 750 °C for (a–c) and 600 °C for (d). The oxide thickness was 90 nm, and MCDL is expressed in µm.

Table 1. MCDL recorded in different wafers after thermal oxidation with different parameters (see the text) and after the deposition of alumina layers with different precursors.

Wafer	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MCDL [µm]	427 + 69	365 ± 25	490 ± 45	258 + 63	449 ± 25	597 ± 21	438 ± 31	632 ± 20	797 ± 54	145 ± 22	635 ± 19	618 ± 28	1454 ± 240	1342 ± 208	802 ± 100	1245 ± 218

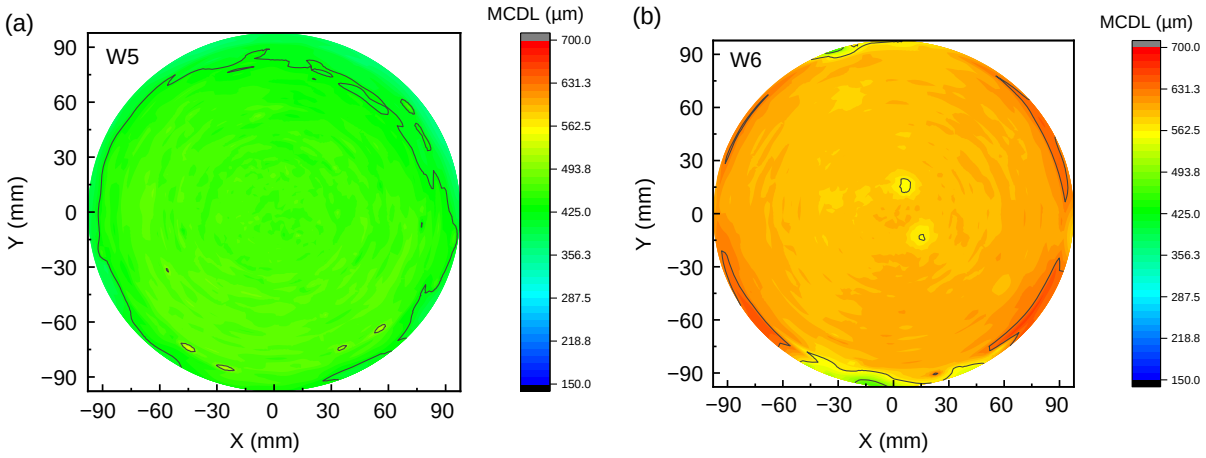

Figure 2. MCDL wafer map recorded on different wafers a) CZ n-type Si and b) FZ p-type Si) following wet oxidation in a horizontal furnace. The oxide thickness was 90 nm, and MCDL is expressed in μm.

recorded in CZ n-type Si are similar to those observed after wet oxidation in the vertical furnace. However, MCDL in FZ p-type Si wafers is 1.7 times larger compared to the values shown in Figure 1. It is important to note that all wafers used for this comparison were sourced from an identical supplier, and their properties specified in the specification are similar. Additionally, no circular pattern in MCDL wafer maps was observed after wet oxidation in the horizontal furnace.

Dry oxidation exhibits MCDL wafer maps similar to those observed after wet oxidation in the horizontal furnace (**Figure 3**). Furthermore, the average MCDL value recorded in the FZ p-type Si wafer was ≈630 μm, which is larger than those obtained after wet oxidation in vertical and horizontal furnaces.

DLTS measurements did not reveal any defects with a concentration above 10^{11} cm^{-3} near the surface or deeper within the bulk of the samples following wet or dry thermal oxidation in either horizontal or vertical furnaces. Typical DLTS spectra closely resemble those depicted in **Figure 4** for both n- and p-type Si samples. It is noteworthy that a significant increase in the DLTS signal was observed around 350 K in W5, and its shift was observed upon applying different reverse biases. Similar peaks have previously been reported in MOS structures[13] and have been correlated with the diffusion of minority carriers into the depletion region at elevated temperatures. This diffusion process results in a change in capacitance within the depletion region, consequently leading to an increase in the DLTS signal.

A comparison of the flatband voltage (V_{FB}) in n- and p-type Si wafers after their oxidation in horizontal or vertical furnaces was also conducted. V_{FB} determined in FZ p-type wafers, following their thermal oxidation in a vertical furnace, was ≈300 mV more negative compared to that obtained in Si wafers oxidized in horizontal furnaces. In contrast, a shift of V_{FB} was more positive in CZ n-type Si wafers after their oxidation in a vertical furnace. Similarly, dry oxidation in a horizontal furnace resulted in a negative shift of V_{FB} by ≈100 mV in FZ p-type Si wafers and a positive shift by around 200 mV in CZ n-type Si wafers, compared to values observed after wet oxidation in the same furnace.

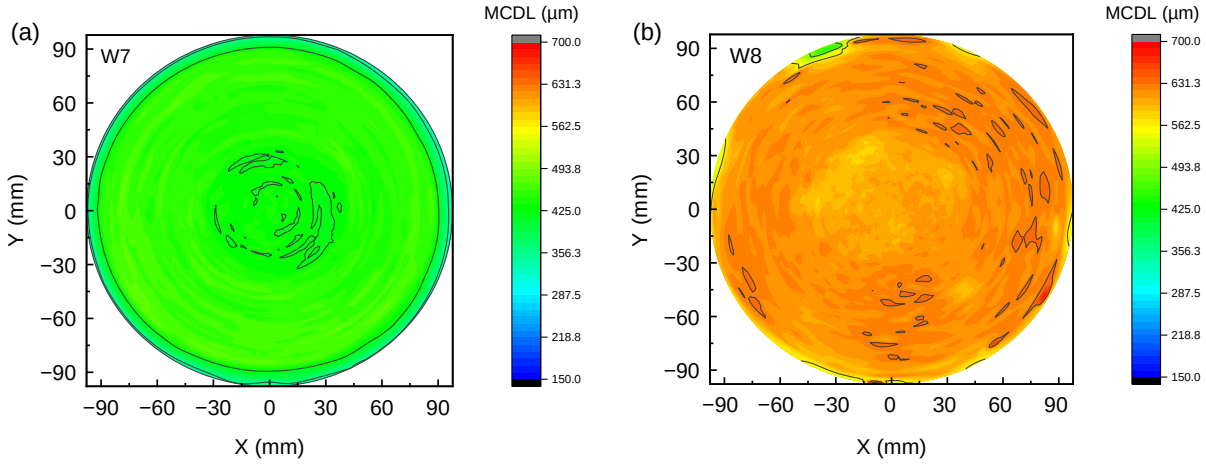

Figure 3. MCDL wafer map recorded on different wafers a) CZ n-type Si and b) FZ p-type Si following dry oxidation in a horizontal furnace. The oxide thickness was 75 nm, and MCDL is expressed in μm.

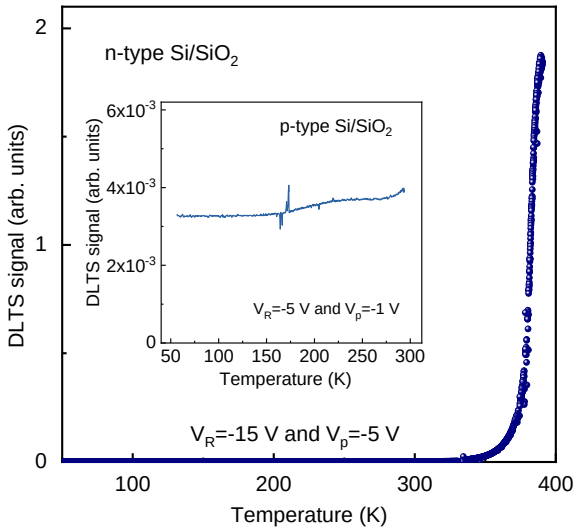

Figure 4. DLTS spectrum recorded in wafer 5. The inset shows a typical DLTS spectrum recorded in W2.

In several previous studies,[14,15] a mixture of DCE with oxygen was also used for various oxidation processes. This increases the speed of oxidation, and it could also reduce the concentration of contaminants in SiO_2 since Cl ions may bind with metal ions, leading to their neutralization. **Figure 5**a exhibits an MCDL wafer map recorded after dry oxidation with DCE on a CZ p-type wafer from the same batch as those used for the investigations in Figure 1–3. The average value of MCDL on this wafer (W9) was 797 ± 54 µm, which is larger than the values observed after wet and dry oxidations in vertical or horizontal furnaces (Figure 1–3). However, it's important to note that the flatband voltage in W9 was comparable to that observed in W8 after dry oxidation without DCE. This shows that the density of electrically active defects in SiO_2 or at the interface is not significantly influenced by using DCE together with oxygen for oxidation processes.

In contrast, the intense rinsing of a furnace with DCE, without any additional conditioning, leads to a significant reduction in MCDL in a CZ p-type Si wafer (Figure 5b). This figure shows an MCDL wafer map recorded on such a wafer after dry oxidation immediately following the intense rinsing of a horizontal furnace with DCE. The average MCDL value in this wafer was around 145 ± 22 µm, significantly lower than the values observed previously in other oxidized wafers, regardless of the type of oxidation (see Figure 1–3 and 5a).

Figure 6 displays MCDL wafer maps recorded after the deposition of PE-TEOS (a) and LP-TEOS (b) on CZ p-type Si wafers. When comparing CZ p-type Si wafers from the same batch, MCDL values after the PE- or LP-TEOS deposition were higher than those observed after thermal oxidation at around 900–1000 °C. The variation in deposition parameters such as flow and pressure did not lead to significant changes in MCDL. Similar MCDL wafer maps were observed compared to those presented in Figure 6.

In several previous studies, the passivation properties of Al_2O_3, such as the effective surface recombination velocity (S_{eff}) and the effective minority carrier lifetime ($\tau_{g,eff}$) obtained from electrical measurements, were shown to be comparable with those of thermal SiO_2 or even better.[16] Herein, MCDL observed in Si wafers after the deposition of Al_2O_3 layers were analyzed and compared with those observed in a similar type of wafers after thermal oxidation (see Figure 1–3). **Figure 7**a–d shows MCDL wafer maps recorded in CZ p-type Si wafers after the deposition of alumina layers by varying the pulse length of two different precursors, H_2O and O_3. Several characteristic features could be distinguished in this figure. Firstly, MCDL values recorded in wafers after the deposition of Al_2O_3 are significantly larger than those observed after dry or wet thermal oxidation in Figure 1–3. Secondly, MCDL values after the ALD deposition are lower at the edge of wafers, independently of precursors used for the deposition. Thirdly, higher MCDL values were observed by reducing the length of H_2O pulses and increasing the length of O_3 pulses during the ALD.

In order to confirm that the Fe concentration is not responsible for the fluctuations of MCDL observed after the deposition of oxide with different tools, the Fe concentration was determined by using SPV.[8] In all investigated wafers, it was below $7 \times 10^{10}\,cm^{-3}$, and any significant correlation between MCDL

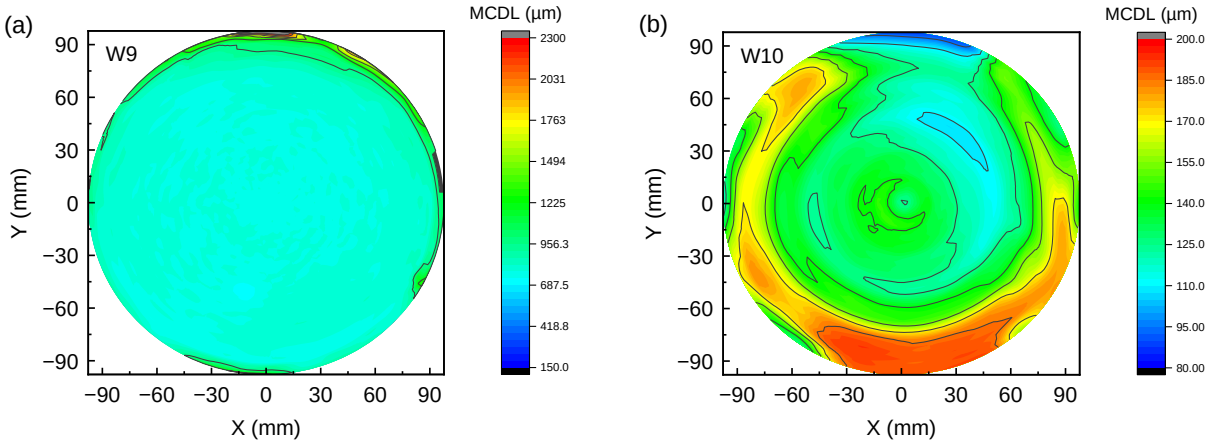

Figure 5. MCDL wafer map recorded after dry oxidation a) with and b) without DCE performed on CZ p-type Si wafers. The dry oxidation in (b) was performed immediately after the intense rinsing of a horizontal furnace with DCE without any additional conditioning of the furnace. The oxide thickness was a) 50 nm and b) 30 nm. MCDL is given in µm.

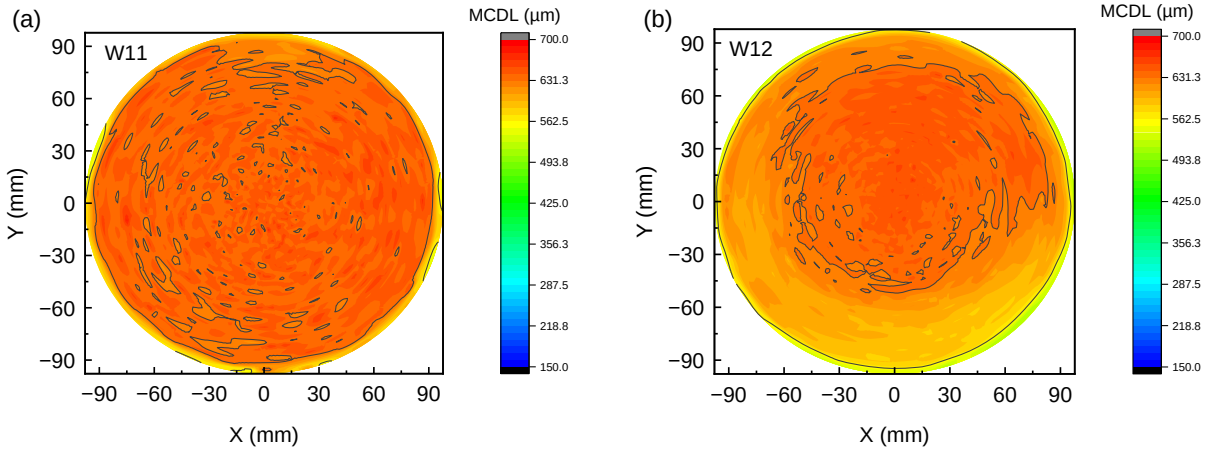

Figure 6. MCDL wafer map recorded after PE-TEOS a) and LP-TEOS b) deposition with different precursors in CZ p-type Si wafers.

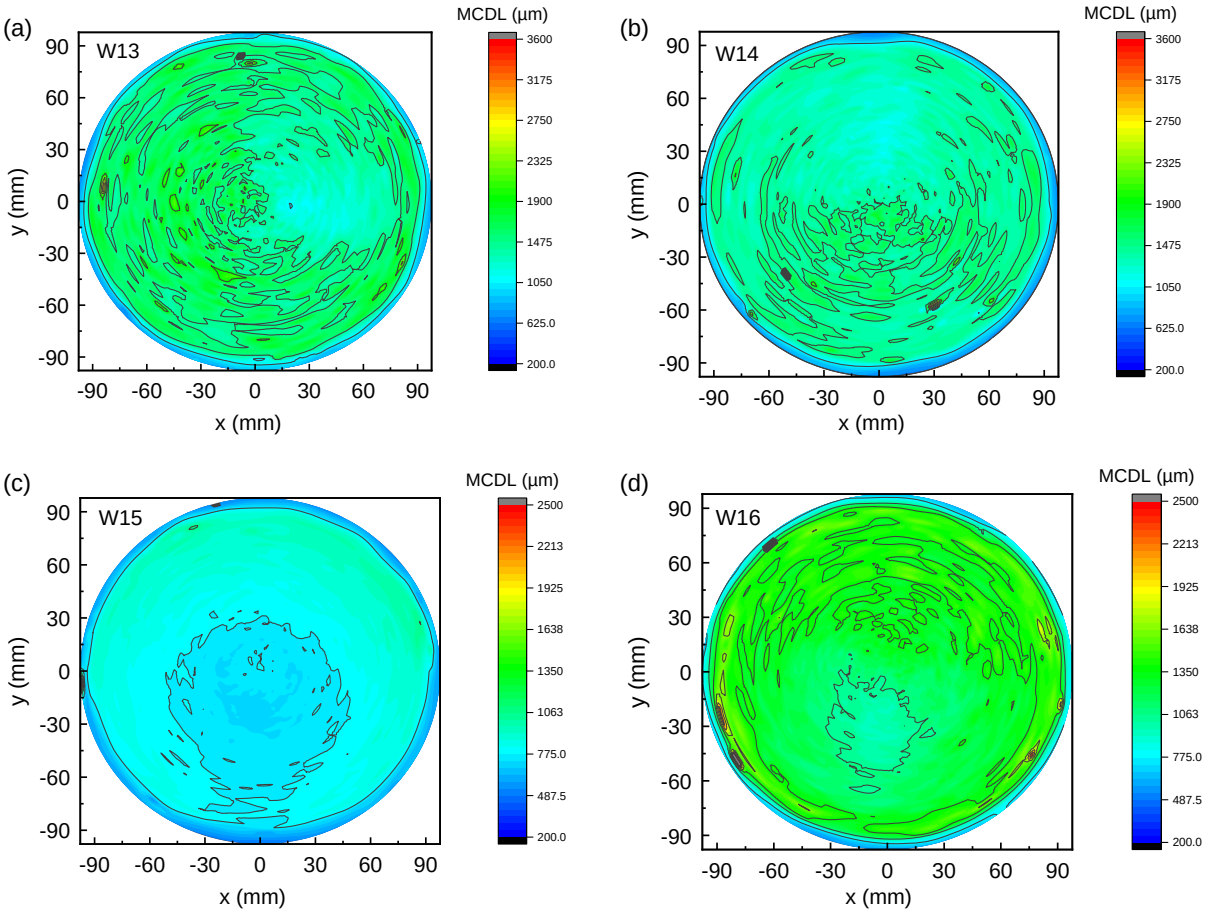

Figure 7. MCDL wafer map recorded after Al_2O_3 deposition with different precursors a,b) H_2O and c,d) O_3 by using the ALD technique. The length of H_2O or O_3 pulses was 0.05 s (a,c), 0.5 s (b) and 1 s (d). The oxide thickness was 60 nm. MCDL is given in μm.

and N_{Fe} was found. Such low values of Fe concentration are even below the detection limit of several experimental techniques, such as conventional DLTS or VPD-ICPMS techniques, which are used for the unambiguous detection of this impurity in Si with a shallow doping level of about 10^{15} cm^{-3}.

In spite of similar average MCDL values observed in p-type Si wafers after oxidation in horizontal and vertical furnaces (see Table 1), several differences in MCDL wafer maps that warrant discussion could be distinguished. Circular patterns in MCDL wafer maps were detected in all p-type Si wafers,

regardless of their growth methods, after oxidation in vertical furnaces. However, such a pattern was absent in n-type Si wafers or in both n- and FZ p-type Si wafers after wet oxidations in horizontal tools.

In previous studies, a circular pattern observed in MCDL wafer maps after a heat treatment at elevated temperatures was attributed to the presence of oxygen-related defects or oxygen clusters.[17–20] It is also plausible that the observed defects may contain H and C, which are abundant during wet oxidations or the growth of Si wafers. Different configurations of CH- and COH-complexes[9,10] introduced by these impurities can create electrically active levels in the band gap of Si, potentially causing the degradation of MCDL observed in Figure 1.

Similar circular patterns were also detected in MCDL wafer maps recorded in FZ p-type Si wafers (Figure 1b) after oxidation in a vertical furnace, whereas it was not observed after the oxidation of similar FZ Si wafers in a horizontal furnace. At first glance, this observation seems inconsistent with the assignment of MCDL degradation to O-related defects since the O-content in FZ Si wafers is significantly lower than that detected in CZ Si wafers. However, carbon is expected to be a dominant unintentional impurity introduced during the FZ growth process, while wet oxidation leads to high concentrations of O and H. At such high oxidation temperatures, both of these impurities could be easily introduced into Si. Moreover, they could also react with electrically inactive C, leading to the formation of COH- or CH-related complexes. The improved uniformity of oxides obtained in vertical furnaces is primarily attributed to the ability to rotate the wafer boat during processing. This rotation might be contributing to the circular patterns observed in MCDL wafer maps in FZ p-type Si wafers.

Previously, circular patterns in MCDL wafer maps in CZ p-type Si wafers were also observed after oxidation with large H_2/O_2 ratios (>1.2) in horizontal furnaces, whereas they did not appear at small H_2/O_2 ratios or after dry oxidation, which does not contain H.[21] This further supports the notion that O and H-related defects could be responsible for the circular patterns observed in Figure 1. Through SPV measurements, the concentration of electrically active defects after wet oxidation in the vertical furnace could be estimated to be around $3–7 \times 10^{10}\,cm^{-3}$. Such low concentrations are below the detection limit of conventional DLTS, along with its high-resolution modification Laplace DLTS, which could provide insights into the origin of these defects. This also explains the absence of DLTS peaks observed in oxidized samples.

Our findings also show that a loading (unloading) temperature of around 600 °C during a thermal oxidation is also responsible for the degradation of MCDL values in oxidized CZ Si wafers. One can interpret this observation with the formation of oxygen precipitates which are electrically active after loading (unloading) temperature whereas these defects are not there at higher temperatures. The mechanism of the formation of these defects is still not clear and further studies are necessary in order to shed light on their origin. One should note, however, that the origin of these defects is different than those influencing MCDL at higher loading (unloading) temperatures.

In good agreement with several previous studies DCE implemented into dry oxidation processes leads to an improvement of MCDL. This can be explained by the positive role of Cl which binds metal ions and leads to their neutralization. In contrast, a significant drop in MCDL values was observed after intense rinsing with DCE in horizontal furnaces without any additional conditioning. These results could be explained by the presence of Cl- or C- residues that may persist in the gas pipeline and the quartz tube wall. These defects could be unintentionally introduced into the wafers during oxidation processes performed at around 900–1000 °C. Nevertheless, the origin of these defects remains unclear.

Finally, MCDL values recorded in Si wafers after PE-TEOS and LP-TEOS oxidation were found to be significantly higher than those observed after thermal oxidation. Even higher MCDL values were observed after depositing Al_2O_3 using the ALD technique. Moreover, such a big difference in MCDL values does not depend on precursors or deposition conditions used for the deposition of the TEOS and Al_2O_3 layers. Previously, using electrical impedance measurements, we showed that the effective surface recombination velocity (S_{eff}) and, consequently, the density of interface states (D_{it}) after the deposition of Al_2O_3 is similar to those obtained after the thermal oxidation of SiO_2 ($<10^{11}\,cm^{-2}\,eV^{-1}$).[16] Hence, D_{it} cannot account for the variation in MCDL values observed between wafers subjected to thermal oxidation and those subjected to processes like Al_2O_3 deposition. However, a thermal oxidation temperature is significantly higher than the deposition temperature used for Al_2O_3 or TEOS depositions. Such higher temperatures could lead to the formation of electrically active oxygen-related defects, or they may be responsible for the in-diffusion of contaminants which might be present in low concentrations in the quartz tube walls. This is less probable at lower deposition temperatures used for TEOS or Al_2O_3 deposition. The Fe-concentration was similar in Si wafers used for thermal oxidation and TEOS or Al_2O_3 deposition and therefore it cannot be a source of different MCDL observed in such wafers.

Beyond MCDL, different types of oxidation lead to a shift in the V_{FB} measured on oxidized wafers. Typically, such a shift in V_{FB}, when measured in wafers from the same batch, is correlated with electrically active defects in SiO_2 or at the interface between Si and SiO_2. The density of interface states was comparable in wafers after oxidation in horizontal and vertical furnaces, even though V_{FB} differed significantly. A positive shift of V_{FB} is generally associated with negatively charged defects, while a negative shift of V_{FB} is attributed to the presence of positively charged defects. These defects might be correlated with O-related defects or oxygen vacancies formed during the oxidation in SiO_2, but further studies are necessary.

3. Conclusions

A comparison of MCDL values following various oxidation processes performed under different conditions in both vertical and horizontal furnaces was conducted. Wet oxidation yielded similar MCDL values in comparable types of Si wafers, regardless of the furnace used. However, distinct circular patterns in MCDL wafer maps emerged in CZ p-type Si after oxidation in a vertical furnace. These circular patterns were attributed to the introduction of O- and H-related defects during the oxidation process. Dry oxidations with DCE markedly improved MCDL values, whereas

frequent use of DCE without furnace conditioning led to a notable degradation of MCDL. Lastly, MCDL values after thermal oxidation were significantly lower than those after the deposition of alumina layers by ALD, despite using similar CZ p-type Si wafers for both oxidation processes. These results were interpreted as a consequence of higher oxidation temperatures employed during thermal oxidations, which may result in elevated concentrations of contaminants in Si wafers.

4. Experimental Section

Different n- and p-type CZ and FZ Si wafers with a thickness of ≈725 µm were utilized. The doping level in the wafers was around $1–2 \times 10^{15}$ cm^{-3}. The oxygen concentration varied from below 5×10^{16} cm^{-3} in FZ wafers to $5–7 \times 10^{17}$ cm^{-3} in CZ wafers.

Before processing, the wafers were immersed in a 1% hydrofluoric acid (HF) solution for 1 min and cleaned with an ammonia-hydrogen peroxide mixture (SC1) and hydrochloric/peroxide mixture (SC2) for 10 min. Prior to each oxidation process, the furnace was cleaned with dichloroethylene (DCE) rinsing, and additional oxidation with dummy wafers was performed at around 1000 °C.

Oxidation steps were carried out at 960 or 1000 °C with an H_2/O_2 ratio of 1. Several wafers were also oxidized directly after intensive rinsing with DCE without additional oxidation with dummy wafers. The oxide thickness was determined from ellipsometry measurements as 45 ± 3 nm (W9 and W10), 75 ± 5 nm (W7 and W8), or 90 ± 5 nm (W1–6), respectively.

Alumina layers were deposited at 300 °C using ALD in a Picosun P-300 batch reactor. Before deposition, the wafers were dipped into a dilute (1%) HF solution for 30 s to remove their native oxide. Trimethylaluminum (TMA) and ozone or de-ionized water were used as precursors for Al and O, respectively. The flow rate of TMA was 150 sccm, whereas the flow rate of O_3 and H_2O was 300 and 200 sccm, respectively. The length of the TMA pulse was constant ($t_{TMA} = 0.1$ s), whereas the length of O_3 and H_2O pulses varied in different wafers ($t_{H2O} = 0.5$ s (W11), $t_{H2O} = 0.05$ s (W12), $t_{O3} = 1$ s (W13), and $t_{H2O} = 0.05$ s (W14)). The thickness of Al_2O_3 was 60 nm.

Plasma enhanced tetraethoxysilane (PE-TEOS) and low pressure tetraethoxysilane (LP-TEOS) layers were deposited by varying different oxidation parameters (pressure, power, spacing, TEOS-flow, and temperature) depending on the type of oxide deposited on p-type Si wafers.

The contamination level in oxidized wafers was characterized by measuring the MCDL and the flat band voltage using SPV measurements[7,8] with a FAaST-230 system. The SPV method relies on the generation and separation of photogenerated charge carriers in a semiconductor material under light of varying wavelengths. The photogenerated carriers diffuse toward the surface, creating a photovoltage due to the separation of charge carriers. This photovoltage decreases exponentially with distance, governed by the MCDL. By plotting the SPV signal as a function of the absorption coefficient (α), the MCDL can be extracted.[7,8]

The flat band voltage in oxidized wafers was determined by plotting the photovoltage as a function of the applied bias voltage, both with and without illumination. The flat band voltage corresponds to the applied voltage where the SPV signal is minimized.

To avoid the effect of surface recombination, SPV signals were compared at different minority carrier injection depths, controlled by the light penetration depth beneath the surface.[8] This contrasts with the microwave detected photoconductance decay technique or photoluminescence measurements, where complete passivation of surface states is required for reliable and reproducible measurements.

SPV measurements for the determination of MCDL should be performed on Si with a depletion region. For p-type wafers, this required a positive charge on top of the oxide, whereas a negative charge was needed on n-type Si wafers. To achieve the necessary surface charge on the corresponding wafers, we used the corona charge station implemented into the SPV tool. The corona process involves generating ions in the vicinity of the surface, which then deposit onto the surface, creating a charged layer. The change in surface potential before and after corona charging provides information about the amount of charge deposited on the surface. Using the corona charge station, we charged the surface up to $\pm 5 \times 10^{10}$ q cm^{-2}, depending on the type of Si wafer. We also note that varying the corona charge between $\pm 1 \times 10^{10}$ and 5×10^{10} q cm^{-2} did not result in any significant changes in MCDL exceeding 10%. The wafer maps of MCDL also remained similar, with no significant changes observed.

Several Si wafers were broken after thermal oxidation, and several samples with a size of 1×1 cm were used for investigation using deep level transient spectroscopy (DLTS) measurements. The contacts for these measurements were prepared after removing the oxide with an HF etch followed by evaporation of Al on top of the Si, as described in refs. [9–12,22,23]. Schottky contacts were made by resistive evaporation of Al through a shadow mask onto thermally evaporated SiO_2 on the p-type sample. Ohmic contacts were made by rubbing a eutectic InGa alloy onto the backside of the samples. To confirm the quality of the contacts, *C–V* characteristics were recorded on metal-oxide-semiconductor (MOS) structures at 1 MHz. DLTS measurements were performed in different regions of p-type Si: close to the surface with a reverse bias of −5 V and a filling pulse of 0 or −1 V, and deeper in the bulk of Si by using a reverse bias of −15 V and a filling pulse of −5 V if the distribution of defects is not uniform.

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Conflict of Interest

The author declares no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

carbon or oxygen, defects, minority carrier diffusion length, Si, SPV

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