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Analysis of Process-Dependent Electrical Properties of Silicon Heterojunction Solar Cells by Quantum Efficiency and Temperature-Dependent Current Density–Voltage Measurements

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Amorphous silicon–crystalline silicon (a-Si:H/c-Si) heterojunction solar cells are fabricated by infrared (IR) radiative or resistive preheating of silicon wafers before the a-Si:H layers deposition. The cells with IR radiative or resistive preheating lead to without S-shape (WoS) or with S-shape (WS) in their light current density–voltage (J–V) characteristics, respectively. The Suns-V_{oc} analysis shows no front/back metal contact barriers for minority carriers in both cells. The light- and voltage-bias-dependent quantum efficiencies of the WS cell show the hindrance of carrier collection at the a-Si:H/c-Si interface due to the band offset, whereas more defective a-Si:H layers are observed in the WoS cell. The WS and WoS cells' temperature-dependent dark J–V characteristics reveal that the carrier transport is through tunnel-assisted recombination and tunneling, respectively. The IR preheating of wafers results in the reduction of the bandgap of a-Si:H and facilitates for minimizing the band offset at the interface, whereas, the resistive heating shows the relatively better a-Si:H/c-Si interface passivation.

1. Introduction

Amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction (SHJ) solar cells have become more promising mainly due to the high open-circuit voltage (V_{oc})/efficiency, superior temperature coefficient of V_{oc}, and also low-temperature fabrication in comparison with homojunction silicon (Si) solar cells.[1–3] The reason for the better performance of the SHJ cell is due to strongly reduced minority carrier recombination at the a-Si:H/c-Si interface, which yields better V_{oc} and further conversion efficiency.[4] The SHJ cells' crucial fabrication process steps are 1) a clean c-Si surface before a-Si:H deposition, 2) optimization of intrinsic and doped ultrathin a-Si:H layers' properties such as resistivity, defect density, energy bandgap, and position of defect energy levels, 3) the lower plasma and/or thermal damage to the c-Si surface during a-Si:H and transparent conductive oxide layers' growth, and 4) the better a-Si:H/c-Si interface.

Depending on the Si surface preparation and a-Si:H layers' process condition, the SHJ cells show a large variation in the diode quality factor (n) and reverse saturation current density (J_0). Scheer[5] has explained the role of interface defect states in SHJ cells and correlated to the activation energies obtained from the temperature-dependent J_0 values. The electronic properties of a-Si:H layers should be compatible with the Si wafer for better charge carrier collection; otherwise, the V_{oc} or fill factor (FF) will be affected. In SHJ cells, the low FF often has been observed along with a distortion in J–V graphs (the so-called S-shape), in the extreme case having an inflection point close to the V_{oc}. The S-shape in light J–V graph of the SHJ cell severely deteriorates the FF, which can be correlated to the reverse barrier formation for minority carriers either at the a-Si:H/c-Si junction or at the contacts.[6–8] Das et al.[6] have assigned the S-shape in the J–V graph of SHJ cells, either due to the energy band offset or the contact barrier, by analyzing the quantum efficiency of a device. Chavali et al.[7] have tried to provide some theoretical insights by relating FF and V_{oc} losses to the S-shape of an SHJ cell.

In this study, we have investigated two SHJ solar cells having variations in the Si wafer preheating before the deposition of undoped/doped a-Si:H layers. One approach is through the resistive and another one is through the infrared (IR) radiative preheating for achieving the desired deposition temperature. The resistive and IR radiative preheating of wafers have shown the S-shape (WS) and conventional J-shape (WoS) in the cells' light J–V characteristics, respectively. The possible diminishing electrical performance (S-shape) of an SHJ cell is explored in depth using the Suns-V_{oc}, direct current (DC) voltage- and light-bias-dependent quantum efficiencies, and temperature-dependent dark J–V measurements.

2. Experimental Section

2.1. Device Fabrication

The SHJ cells of Ag/tin-doped indium oxide (ITO)/p^+-a-Si:H/i-a-Si:H/n-c-Si/n^+-a-Si:H/ITO/Ag structures were fabricated

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using n-type monocrystalline Si wafers having (100) orientation, a resistivity of 3–5 Ω-cm, a bulk minority carrier lifetime of ≈300 μs, and a thickness of 180–200 μm as a base material. As-cut Si wafers were treated for surface damage removal, followed by micrometer-scale chemical texturing in a diluted alkaline solution. The wafers underwent standard Radio Corporation of America cleaning treatment and a brief HF (≈1%) dip before loading into the RF (13.56 MHz)-based plasma-enhanced chemical vapor deposition (PECVD) chamber for the growth of intrinsic and doped a-Si:H layers. The schematic of the deposition system for the a-Si:H and ITO layers and the fabricated device structures is shown in **Figure 1**.

The SHJ cells were fabricated on the production type of system (having six chambers including four process chambers for i-a-Si, p^+-a-Si:H, n^+-a-Si:H, and ITO layers' deposition on Si wafers of $125 \times 125\ cm^2$ size). The entry load lock (ELL) and isolation chambers (ISO) chambers have IR radiative preheating (top and bottom heating for ELL and only bottom heating for ISO chambers) arrangements for the Si wafers, and the process chambers have resistive heaters at the bottom. Although all the chambers have temperature monitors, apart from this, the temperature sensor also is installed at the entry of the i-a-Si:H chamber. The cells were fabricated with the preheating variation of Si wafers. In one case, the stainless steel (SS) carrier loaded with wafers is soaked in heat for ≈45 min at a chamber temperature of ≈180 °C by resistance heating in the deposition chamber itself. The distance between the wafer carrier and heating block is ≈2 cm. Under this preheating condition, the substrate carrier has attained only ≈140 °C. In another case, the SS carrier (holding wafers) was preheated in the ELL chamber using IR heaters for 30 min, prior to the deposition of each a-Si:H layer. This has led to the SS carrier's temperature of ≈180 °C and Si wafers' temperature was ≈300 °C due to the IR light absorption. After introducing the SS carrier in the process chamber, the wafer temperature was ≈180 °C during the a-Si:H layers deposition, whereas such temperatures cannot be achieved through the resistive preheating step in our system. The i-a-Si:H, p^+-a-Si:H, and n^+-a-Si:H layers' thicknesses are 6–8 nm, ≈10 nm, and 14–16 nm, respectively. The deposition rate is 0.12–0.14 nm s^{-1}, which is evaluated by depositing on a glass slide. The ITO of ≈80 nm was deposited using the DC magnetron sputtering system with plasma of oxygen(≈1%)-argon mixture. Low-temperature silver (Ag) paste was used for cells' front and back metal contacts using the screen printer.

2.2. Characterization

The SHJ cells' *J–V* graphs were recorded under AM1.5G illumination (1000 W m^{-2}) using Oriel Sol3A Class AAA Solar Simulator and the Keithley 2400 source measurement system. A temperature-controlled stage from Newport was used to maintain the temperature of ≈25 °C. The Suns versus open-circuit voltage (Suns-V_{oc}) graphs were recorded using the Sinton WCT−120TS measurement system. A neutral density filter of 70% (for light attenuation) was used to prevent the reference cell voltage saturation during the higher suns illumination. The cells' pseudo *J–V* graphs also were recorded from the Suns-V_{oc} system to verify the effect of series resistance on the light *J–V* characteristics. For the voltage- and light-bias-dependent external quantum efficiency (EQE) measurements of the cells, the SpeQuest quantum efficiency system from the ReRa solutions, the Netherlands, was used. This system is equipped with DC voltage and DC white light bias (halogen lamp with an intensity of ≈0.3 suns) sources. Total reflectance from the cells also was measured using an integrated sphere attached to the EQE system, for the internal quantum efficiency (IQE) estimation. The incident monochromatic light spot size of the quantum efficiency system is ≈3 mm in diameter, which also covers slightly the cell's metal fingers. The optical chopper frequency was set at 183 Hz, which is quite enough to record the response of incident photons. For the low-temperature dark *J–V* measurements, the CCS − 400 cryostat from the Janis Company, USA, was used along with the Lakeshore temperature controller. Four-wire contacts were used for the electrical measurement to eliminate any external series resistance from the measurement wires.

3. Results and Discussions

3.1. Current Density–Voltage Characteristics of SHJ Cells

Figure 2a,b shows the light *J–V* characteristics of SHJ cells WS and WoS with the resistive and IR radiative preheating of wafers before the a-Si:H layers deposition, respectively. The pseudo (under light without any series resistance effect) and dark *J–V* graphs of the cells also are shown in Figure 2. The WS and WoS cells' V_{oc} are ≈551 and ≈588 mV, and the FFs are ≈48% and ≈69%, respectively. In the case of the WoS cell, the actual FF and conversion efficiency are nearly same as the pseudo values, whereas, the WS cell has shown large

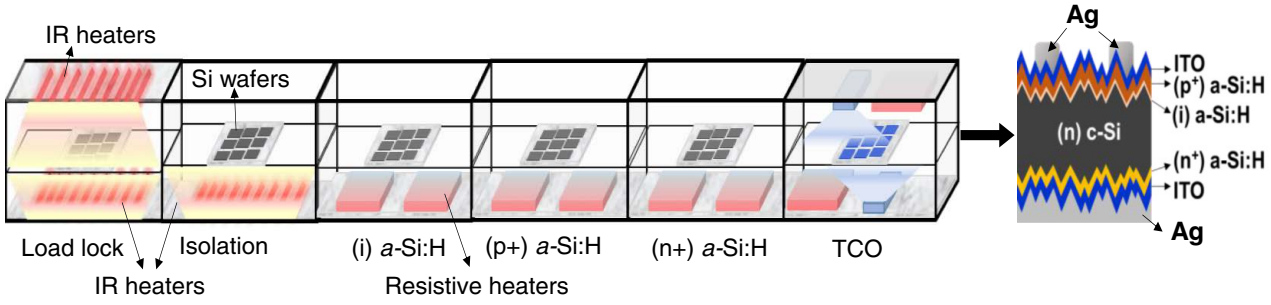

Figure 1. Schematic of SHJ device process line: ELL and ISO with IR radiative preheaters, PECVD, and sputter chambers for the a-Si and transparent conducting oxide (TCO) layers' deposition, and schematic of a fabricated SHJ cell.

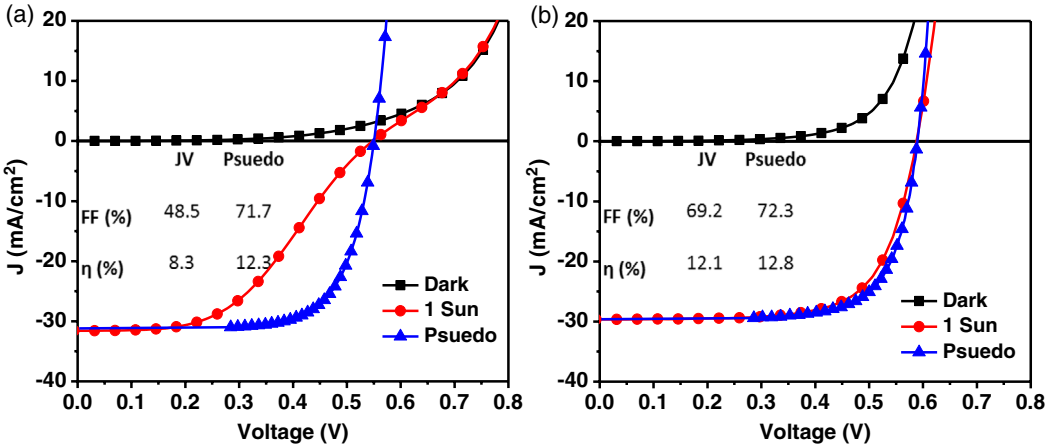

Figure 2. Current density–voltage (*J*–*V*) graphs of SHJ cells: a) WS and b) WoS under light condition; along with this, the cells' pseudo (under light without series resistance effect) and dark *J*–*V* graphs also are shown. Photovoltaic parameters observed under actual and pseudo *J*–*V* measurement conditions are also shown in the respective graphs.

variation between the pseudo and actual parameters. In the case of the WS cell, 1) the superposition principle is significantly violated,[9] and 2) in the dark condition, the current enhancement is initially slower and has taken higher voltages to reach larger currents. The huge loss of WS cell's FF gives evidence related to the blocking of photogenerated charge carriers' movement at one of the device interfaces.

3.2. Suns-V_{oc} Characteristics of Cells

The Suns-V_{oc} measurements are carried out to understand the carrier transport restriction in the WS cell (either at the main junction or at contacts). The graphs of both cells are shown in **Figure 3**a. The WS cell has shown linear behavior upto ≈100 suns without any turn around, which indicates that the contacts are ohmic in nature,[6] whereas, the graph of WoS cell has shown two different linear regions, which is an indication of the double diode behavior. A solar cell can be modeled as a DC equivalent circuit with two diodes parallel to each other for the front junction and a reverse parasitic diode in parallel with a shunt resistance for the back contact (schematically shown as an inset of Figure 3a).[10] At standard illumination, a solar cell's carrier transport is decided by the main junction, and the back contact can still provide a low shunt resistance path.[11] At the higher suns, the Schottky front/back contacts can accumulate charge carriers due to the contact resistance, leading to a decrease in the cell's V_{oc}.[10] So, in the WS cell, the reverse diode at the back contact is not significant to provide any turnaround in the Suns-V_{oc} graph, which means that the carrier transport barrier lies at the main junction of the device.

The cells' ideality factors (n_s) also are determined from the Suns-V_{oc} graphs using a single diode equation,[12] which are shown in Figure 3b. The "n_s" value of a solar cell indicates the quality of the bulk and junction interface. The *J*–*V* characteristics of the SHJ cell deviate from exponential dependence of current on voltage based on the bulk and interface defects, layer's resistivity, process shorts, energy band misalignment,

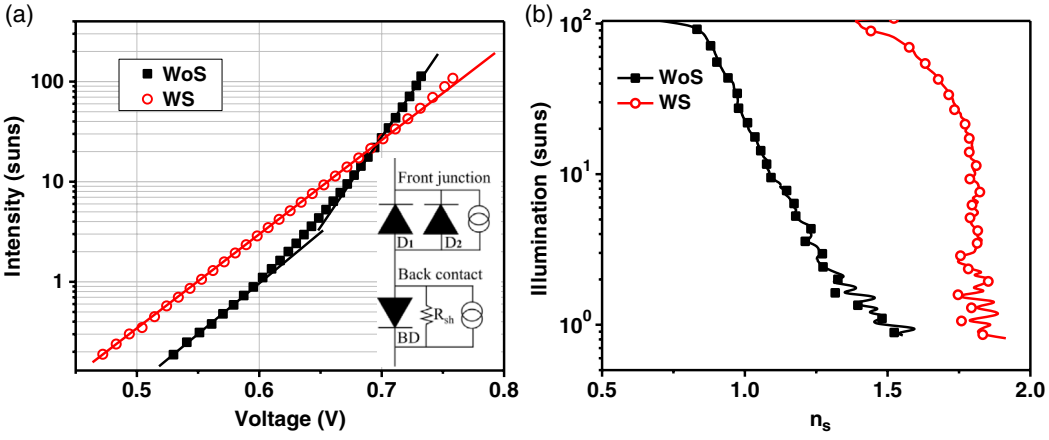

Figure 3. a) Suns versus open-circuit voltage graphs and b) illumination intensity-dependent ideality factor (n_s) of the WS and WoS cells, the n_s values are obtained by fitting data using the standard diode equation; inset of Figure 3a shows the equivalent circuit diagram with two diodes (D1 and D2) for front junction and a reverse diode (BD) in parallel with a shunt resistance for a back contact.

and contact resistance.[6,12] For Suns-$V_{oc,}$ n_s represents only the losses associated with recombination but not the resistive losses in a device. The n_s values of the WoS cell have shown linear decrement upto 20 suns, after that it is reduced to below unity, which shows that the carrier recombination is through the Auger process due to the higher carrier density,[12] whereas the n_s values of WS cell have remained constant upto 20 suns, and thereafter it has reduced slightly (value remains more than unity). Das et al.[6] have shown the value of $n_s \approx 1$ with no i-a-Si:H layer passivation and $n_s > 1$ with i-a-Si:H passivation for the SHJ cells. This difference was explained based on the surface recombination variation (SRV) at the a-Si:H/c-Si interface. Therefore, with better Si surface passivation, the diffusion of photogenerated carriers toward the rear contact will be enabled, which increases n_s more than unity due to an additional carrier recombination contribution from the rear contact. Therefore, one can infer from this analysis that the interfaces of the WS cell are passivated better than the WoS cell due to the relatively low-temperature process by the resistive preheating.

3.3. Light- and Voltage-Bias-Dependent Quantum Efficiency Analyses

To investigate cells' junction/contact barrier for the carrier collection, the voltage- and light-bias-dependent EQE analysis is conducted. The WS and WoS cells' EQE spectra without and with white light bias conditions are shown in **Figure 4**a. The important observations from the spectra without light bias are 1) EQE of the WoS cell is lower than the WS cell in the entire spectral region and 2) both the cells in the shorter wavelength region (<400 nm) have shown strong parasitic absorption. In the shorter wavelength region, the WoS cell has shown a conversion efficiency edge at a relatively longer wavelength due to the smaller energy bandgap (E_g) of a-Si:H. The process condition (IR preheating) of the WoS cell has led to a slight decrease in the E_g of a-Si:H due to the increase in deposition temperature and reduction in hydrogen content.[13] The WS cell's better spectral response from the front and back in comparison with the WoS cell is due to the better Si surface passivation by a-Si:H at relatively low-temperature deposition.

The EQE response under the white light bias condition (Figure 4a): at the shorter wavelength region, the cells have shown no variation, whereas, at the longer wavelength region, only the WoS cell has shown an enhancement and interestingly attained the WS cell's carrier collection efficiency. The light bias acts as photon doping in the a-Si:H films, which can saturate some of the bulk defect states[8] and can improve further the layer's photoconductivity.[14] It is a well-established phenomenon that the hydrogen content in the a-Si:H layer changes with deposition temperature and hence the number of bulk defect states.[15,16] Effusion of hydrogen from the a-Si:H film also was observed by De Wolf and Kondo[17] at high temperature preheating. Under the light bias condition, some of the a-Si:H layers' defect states are saturated in the WoS cell, which has led to an enhancement in carrier collection efficiency. Further, the rear Si surface passivation also is investigated from the IQE spectra by estimating the effective bulk diffusion lengths of minority carriers (L_{eff}). For this analysis, one can consider the red to IR region of the IQE spectrum of a cell, which represents the quality of the bulk Si and rear interface. For estimating the cells' L_{eff} values with and without white light bias, the graphs are plotted between inverse IQE versus absorption depth by considering 860–1050 nm wavelength region and are shown in Figure 4b. The graphs' linear regions are fitted by considering the following relation

$$\frac{1}{\mathrm{IQE}} = 1 + \frac{\cos\theta}{\alpha}\frac{1}{L_{\mathrm{eff}}} \tag{1}$$

where $1/\alpha$ is the absorption depth, and $\theta = 41.8°$ is considered for the textured cell surface.[18] The rear SRVs also are estimated using the L_{eff} values,[19] which are shown as an inset of Figure 4a. With the light bias, the WoS cell's L_{eff} is enhanced, and SRV is reduced in comparison with the WS cell. This analysis also has provided further evidence related to the more defective n^+-a-Si:H layer at the rear side of the WoS cell.

The voltage- and light-bias-dependent EQE spectra of cells are shown in **Figure 5**, which are recorded to understand the carrier injection-dependent collection efficiency. The bias voltages (for WS and WoS cells are 0.35 and 0.54 V, respectively) are decided based on photocurrent reduction to nearly half of the

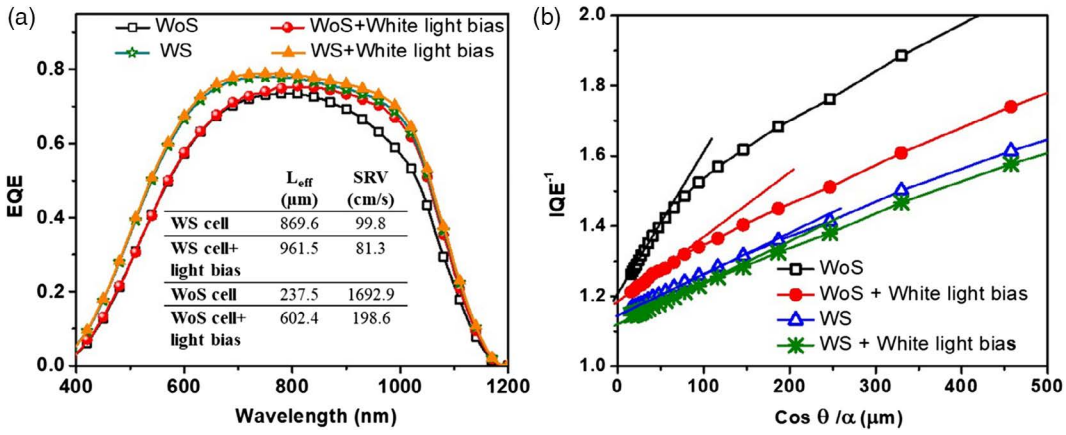

Figure 4. WS and WoS cells' a) EQE spectra without and with white light bias (≈0.3 suns) and b) graphs between IQE^{-1} and absorption depth. Estimated effective bulk diffusion length (L_{eff}) and SRV values of the WS and WoS cells from the spectra are shown as an inset.

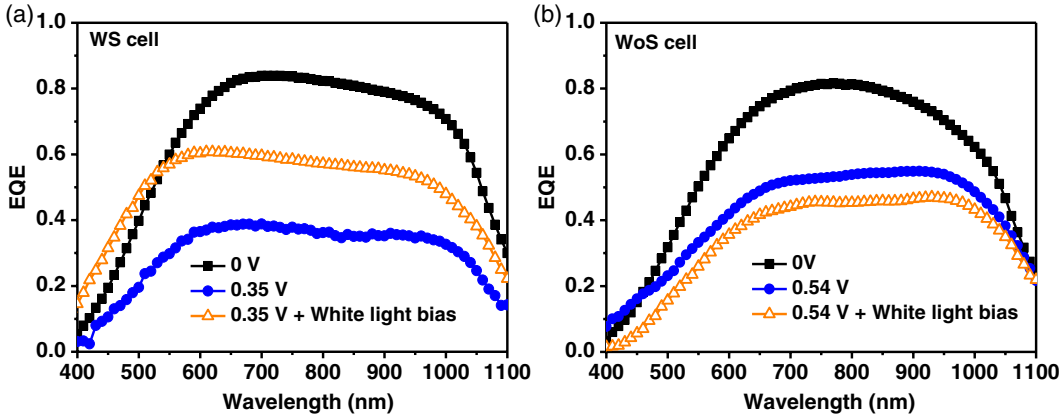

Figure 5. EQE spectra: a) without any bias, with 0.35, and with 0.35 V + light bias (≈0.3 suns) of the WS cell and b) without any bias, with 0.54, and 0.54 V + light bias (≈0.3 suns) of the WoS cell.

J_{sc} of a cell, which is after the maximum power point (MPP) in the light J–V graph. The analysis of photocurrent loss near the MPP region can reveal an SHJ device adverse mechanism.[20] With the voltage bias alone, the cells' EQE has reduced in the entire spectral region due to the reduction in the junction's depletion width and promotion of carrier injection, leading to recombination. However, with the voltage and light bias (≈0.3 suns), the cells have shown the opposite trend in the EQE response. In the case of the WS cell, an enhancement of EQE under light bias has given an indication of the valence band offset,[21] as no barrier for the charge carriers at the front/back contact is observed from the Suns-V_{oc} analysis. In the case of the WoS cell, a small variation in EQE response shows the absence of charge carrier accumulation at the junction due to the smaller valence band offset (coming from the relatively smaller E_g of the a-Si layer).

For explaining the process-dependent variation of the a-Si:H layers' E_g and number of defect states, the representative heterojunction energy band diagrams of the WS and WoS cells are shown in **Figure 6** under illumination. Figure 6a shows the WS cell; the large valance band offset at the a-Si/c-Si junction is due to the a-Si:H layers' relatively larger E_g along with the smaller number of defect states, promoting the minority carrier accumulation and further recombination. Figure 6b shows the WoS cell; the smaller band offset at the junction is due to the a-Si:H layers' relatively smaller E_g along with the larger number of defect states minimizing carrier accumulation.

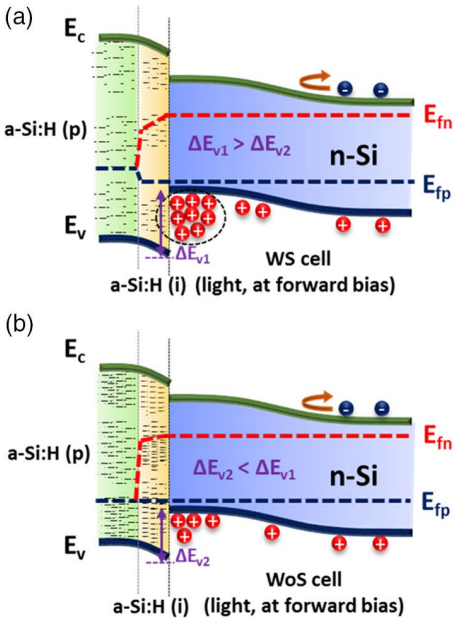

Figure 6. Representation of heterojunction energy band diagrams of cells under the illumination condition to show carrier blocking: a) WS cell's a-Si:H layers having a relatively larger E_g and smaller number of defect states and b) WoS cell's a-Si:H layers with the relatively smaller E_g and a large number of defect states.

3.4. Temperature-Dependent Dark Current Density–Voltage Analysis of Cells

To elucidate further the WS and WoS cells' carrier transport, the temperature-dependent (200–323 K) dark J–V analysis is conducted under the forward voltage bias condition (graphs are not shown here). The graphs are divided into two regions on the basis of change in a slope: one is a low forward bias (LFB) region from 0.1 to 0.5 V and another one is a high forward bias (HFB) region from 0.5 to 0.8 V. The two regions of the temperature-dependent dark J–V graphs are fitted using the Shockley diode Equation (2) for estimating the slopes (A) and reverse saturation current density (J_0)

$$J = J_0(e^{AV} - 1) \quad \text{where } A = \frac{q}{nkT} \tag{2}$$

where J is the current density at an applied voltage V at temperature T, n is the diode quality factor, q is the electronic charge of carrier, and k is Boltzmann's constant.

The slopes of dark J–V graphs for two linear regions (LFB and HFB) of cells with temperature variation are shown in **Figure 7**a. Both the cells in the LFB region do not show any significant change in the slopes with the temperature, which is a signature of the charge carrier tunneling at the a-Si:H/c-Si junction region.[11] However, the cells in the HFB region with an increase in temperature have shown a slight enhancement of the slopes,

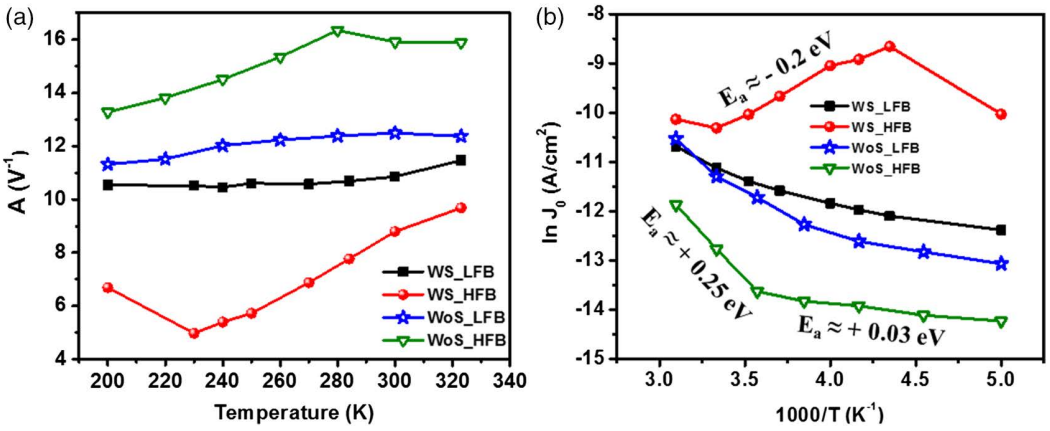

Figure 7. WS and WoS cells' a) dark *J–V* graphs' slopes (*A*) versus temperature (*T*) and b) ln J_0 versus 1000/*T* graphs. The estimated activation energy (E_a) values in the LFB and HFB voltage regions are also shown.

indicating that carrier transport is changing from tunneling to the thermally activated process. The ln J_0 versus 1000/*T* graphs also are plotted (Figure 7b) to investigate the thermal activation process by estimating the activation energies (E_a) of J_0. The cells' J_0 has reduced with a decrease in temperature (this is a generally observed phenomenon); except in the case of WS cell, the J_0 has enhanced in the HFB region, showing an opposite trend (the slope of ln J_0 versus 1000/*T* plot is negative in this case). This peculiar behavior can be explained by the tunnel-assisted recombination as the dominating transport mechanism instead of simple tunneling at the junction. In this situation, the temperature can also influence the interface recombination rate (which is the inverse of minority charge carrier's lifetime).[22] So, in the HFB region of the WS cell, the recombination can become dominant at the interface due to large band offset, which promotes imminent recombination. These SHJ cells do not follow the high-efficiency SHJ cells' characteristics,[23] where the carrier transport is through diffusion limited at the HFB region.

4. Conclusions

The SHJ cells are fabricated by the resistive or IR radiative preheating of the n-Si wafers, which has resulted in WS and WoS in the light *J–V* graphs, respectively. Due to the deposition temperature variation, we have observed 1) variation in the a-Si:H layers' electronic properties and Si surface passivation by the i-a-Si:H layer and 2) valence band offset at the junction from the device analysis. The WS cell's quantum efficiency analysis with the voltage and light bias conditions has revealed the energy barrier due to the band offset at the a-Si/c-Si interface, which has hindered photogenerated charge carrier collection. The presence of the large band offset due to the low-temperature preheating of the c-Si wafer deteriorated the FF drastically by restricting the photogenerated charge transport. In the case of the WoS cell, the loss of FF is recovered with enough preheating of the wafer, but, the quality of the front/back a-Si:H layer is deteriorated in terms of the lesser bandgap and an increase in defects in the a-Si layer. Moreover, the repeated exposure (before and after deposition) of the back a-Si:H layer to IR preheating has been affected more, which is reflected in EQE analysis. These observations are further corroborated by analyzing the temperature-dependent dark *J–V* characteristics, where the WS and WoS cells have shown carrier transport due to tunnel-assisted recombination and tunneling (in HFB and low temperature), respectively. Thus, we can conclude that the IR radiative heating is helping to avoid the S shape, but enhancing the bulk defect states, which is further limiting the overall performance of the SHJ device. This work also demonstrates the effective use of characterization techniques to diagnose the anomalous behavior of an SHJ cell's electrical properties.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

amorphous silicon, band offsets, heterojunctions, quantum efficiencies, silicon solar cells, S-shapes

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[1] S. Y. Herasimenka, W. J. Dauksher, S. G. Bowden, *Appl. Phys. Lett.* **2013**, *103*, 053511.
[2] M. Taguchi, E. Maruyama, M. Tanaka, *Jpn. J. Appl. Phys.* **2008**, *47*, 814.

[3] M. Taguchi, A. Terakawa, E. Maruyama, M. Tanaka, *Prog. Photovoltaics Res. Appl.* **2005**, *13*, 481.
[4] Y. Tsunomura, Y. Yoshimine, M. Taguchi, T. Baba, T. Kinoshita, H. Kanno, H. Sakata, E. Maruyama, M. Tanaka, *Sol. Energy Mater. Sol. Cells* **2009**, *93*, 670.
[5] R. Scheer, *J. Appl. Phys.* **2009**, *105*, 104505.
[6] U. Das, S. Hegedus, L. Zhang, J. Appel, J. Rand, R. Birkmire, 35th IEEE Photovoltaic Specialists Conf., IEEE, Honolulu, HI, **2010**, pp. 001358–001362.
[7] R. V. K. Chavali, J. R. Wilcox, B. Ray, J. L. Gray, M. A. Alam, *IEEE J. Photovoltaics* **2014**, *4*, 763.
[8] S. Mudgal, S. Singh, V. K. Komarala, *IEEE J. Photovoltaics* **2018**, *8*, 909.
[9] R. V. K. Chavali, S. De Wolf, M. A. Alam, *Prog. Photovoltaics Res. Appl.* **2018**, *26*, 241.
[10] M. A. Green, A. W. Blakers, J. Zhao, A. M. Milne, A. Wang, X. Dai, *IEEE Trans. Electron Devices* **1990**, *37*, 331.
[11] S. W. Glunz, J. Nekarda, H. Mäckel, A. Cuevas, *Proc. 22nd Eur. Photovolt. Sol. Energy Conf. 3–7 September* WIP-Renewable Energies, Munich, Germany **2007**, p. 849.
[12] O. Gunawan, T. Gokmen, D. B. Mitzi, *J. Appl. Phys.* **2014**, *116*, 084504.
[13] R. V. Kruzelecky, D. Racansky, S. Zukotynski, J. M. Perz, *J. Non. Cryst. Solids* **1988**, *99*, 89.
[14] F. Liu, C. Yan, K. Sun, F. Zhou, X. Hao, M. A. Green, *ACS Photonics* **2017**, *4*, 1684.
[15] T. F. Schulze, H. N. Beushausen, C. Leendertz, A. Dobrich, B. Rech, L. Korte, *Appl. Phys. Lett.* **2010**, *96*, 252102.
[16] T. F. Schulze, L. Korte, F. Ruske, B. Rech, *Phys. Rev. B* **2011**, *83*, 165314.
[17] S. De Wolf, M. Kondo, *J. Appl. Phys.* **2009**, *105*, 1.
[18] E. Thouti, A. K. Sharma, S. K. Sardana, V. K. Komarala, *J. Phys. D. Appl. Phys.* **2014**, *47*, 425101.
[19] R. Brendel, *Thin-Film Crystalline Silicon Solar Cells: Physics and Technology*, John Wiley & Sons, Hoboken, NJ, USA **2011**.
[20] S. Mudgal, S. Singh, V. K. Komarala, IEEE 7th World Conf. Photovolt. Energy Convers, IEEE, Waikoloa Village, HI **2018**, pp. 2158–2161.
[21] F. A. Rubinelli, J. Y. Hou, S. J. Fonash, *J. Appl. Phys.* **1993**, *73*, 2548.
[22] K. Singh, S. Mandal, S. Singh, V. K. Komarala, *AIP Conf. Proc. (Vol. 2147, No. 1)*, AIP Publishing LLC, Melville, NY, **2019**, p. 020014.
[23] T. F. Schulze, L. Korte, E. Conrad, M. Schmidt, B. Rech, *J. Appl. Phys.* **2010**, *107*, 023711.