Analysis of AlN/AlGaN/GaN metal-insulator-semiconductor structure by using capacitance-frequency-temperature mapping

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AlN/AlGaN/GaN metal-insulator-semiconductor (MIS) structure is analyzed by using capacitance-frequency-temperature (*C-f-T*) mapping. Applying sputtering-deposited AlN, we attained AlN/AlGaN/GaN MIS heterostructure field-effect transistors with much suppressed gate leakage currents, but exhibiting frequency dispersion in *C-V* characteristics owing to high-density AlN/AlGaN interface states. In order to investigate the interface states deteriorating the device performance, we measured temperature-dependent frequency dispersion in the *C-V* characteristics. As a result, we obtained *C-f-T* mapping, whose analysis gives the activation energies of electron trapping, namely the interface state energy levels, for a wide range of the gate biases. This analysis method is auxiliary to the conventional conductance method, serving as a valuable tool for characterization of wide-bandgap devices with deep interface states. From the analysis, we can directly evaluate the gate-control efficiency of the devices. © *2012 American Institute of Physics*.
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AlGaN/GaN heterojunction field-effect transistors (HFETs)[1] have been extensively developed as promising devices for high-frequency and high-power applications. However, gate leakage current is a limiting factor for practical usage of these devices. In order to solve this problem, AlGaN/GaN metal-insulator-semiconductor (MIS) HFETs, enabling effective reduction of the gate leakage currents, have been developed and studied. In particular, high-dielectric-constant (high-*k*) oxide materials, such as Al_2O_3 (Ref. 2) or HfO_2 (Refs. 3 and 4), have been investigated as a gate insulator of the MIS-HFETs. On the other hand, AlN is an important high-*k* non-oxide insulator possessing possible suitability for III–V device processing.[5,6] In addition to AlN-passivated AlGaN/GaN HFETs exhibiting good heat release properties[7–12] due to the high thermal conductivity of AlN ($\sim$10 times higher than that of Al_2O_3),[13] AlN/AlGaN/GaN MIS-HFETs, where the AlN gate insulator was sputtering-deposited, have been investigated,[7,14,15] owing to a possible high breakdown field $\gtrsim$10 MV/cm (Refs. 16 and 17) and a high dielectric constant $\sim$10 (Ref. 18) comparable to those of Al_2O_3. In particular, we showed significant suppression of gate leakage current, although frequency dispersion in the *C-V* characteristics for forward gate biases was observed.[15] This dispersion is attributed to high-density AlN/AlGaN interface mid-gap states leading to a gate-control impediment, which severely depresses the device performances. Such mid-gap states in GaN-based devices have been investigated by Terman method,[19–21] conductance method,[14,15,22–27] and deep level transient spectroscopy (DLTS).[28–31] In the previous work, we employed the conductance method for analysis of capacitance-voltage-frequency (*C-V-f*) characteristics to investigate the AlN/AlGaN interface state density and electron trapping time constant at room temperature.[15] In this work, we propose an analysis method using capacitance-frequency-temperature (*C-f-T*) mapping obtained from the temperature-dependent *C-V-f* characteristics. This method gives the activation energies of electron trapping, namely the interface state energy levels, for a much extended range of the gate biases, serving as an auxiliary tool to the conventional conductance method.

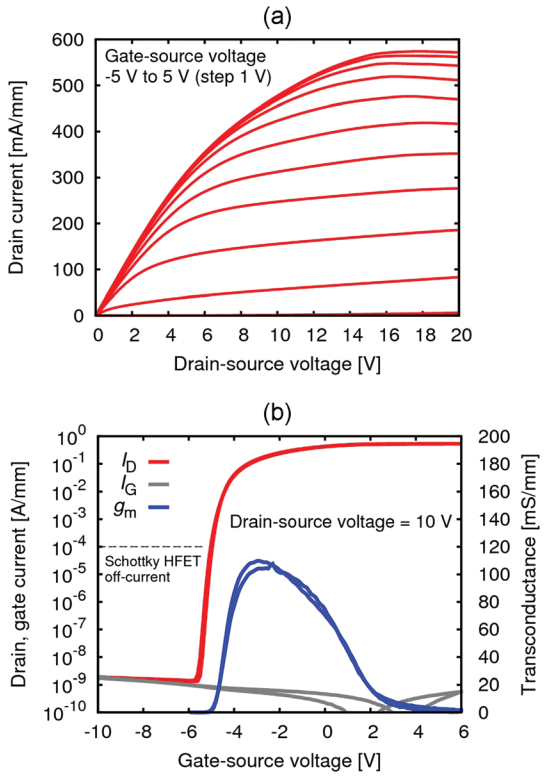

FIG. 1. Characteristics of the AlN/AlGaN/GaN MIS-HFET. (a) Output characteristics. (b) Transfer characteristics, where drain current I_D, gate current I_G, and transconductance g_m were obtained under the gate voltage sweep of $-10\,V \rightarrow +6\,V \rightarrow -10\,V$.

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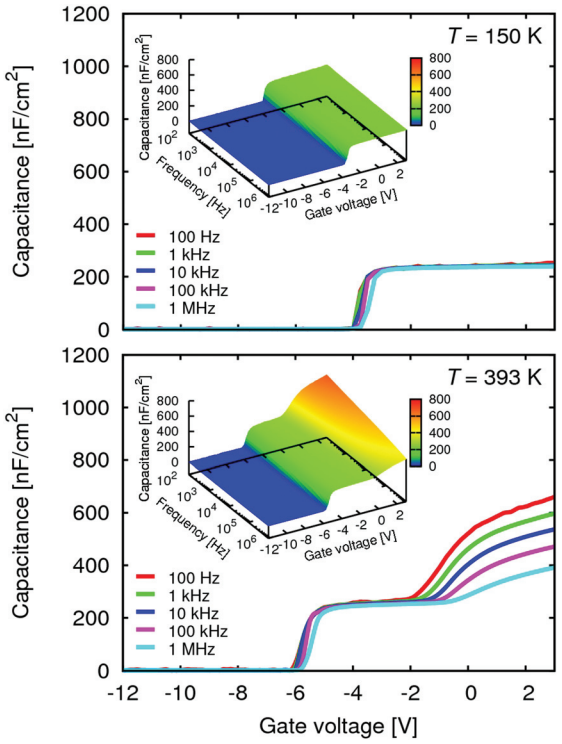

FIG. 2. *C-V-f* characteristics of the AlN/AlGaN/GaN MIS structure at 150 K (above) and 393 K (below).

Moreover, from the interface state energy levels corresponding to a wide range of the gate biases, we can directly evaluate the gate-control efficiency of the devices.

We fabricated AlN/AlGaN/GaN MIS-HFETs and MIS structures simultaneously using an $Al_{0.29}Ga_{0.71}N$ (25 nm)/GaN (3000 nm) heterostructure obtained by metal-organic vapor phase epitaxy on sapphire(0001). Hall measurements of the heterostructure show an as-grown electron mobility of 1200 $cm^2/V\text{-}s$ and a sheet electron concentration of $1.3 \times 10^{13}\ cm^{-2}$. On the heterostructure, Ti/Al/Ti/Au Ohmic electrodes were formed and device isolation was achieved by B^+ implantation. On the AlGaN surface cleaned by organic solvents, deionized water, and oxygen plasma ashing to remove surface organic contaminants, followed by oxide removal using Semicoclean (ammonium-based etchant), an AlN gate insulator of $\sim$19 nm thickness was deposited by RF magnetron sputtering at room temperature with an AlN target in Ar-N_2 ambient. The formation of Ni/Au gate electrodes completed the device fabrication. The MIS-HFETs have the gate length of 250 nm, the source-gate spacing of 2 μm, the gate-drain spacing of 3 μm, and the gate width of 50 μm, while the MIS structures have the 100 μm $\times$ 100 μm gate electrode surrounded by the Ohmic electrode.

In Figs. 1(a) and 1(b), we show output and transfer characteristics of the fabricated MIS-HFET, respectively. Owing to good insulating properties of the AlN, gate leakage currents are significantly small, 10^{-9} A/mm range or less, for both reverse and forward gate biases. The small gate leakage currents lead to small drain off-currents shown in Fig. 1(b). However, we observe a rapid decrease in the transconductance towards forward gate biases, suggesting high-density AlN/AlGaN interface states.

In order to investigate the AlN/AlGaN interface states, we measured the *C-V-f* characteristics between the 100 μm $\times$ 100 μm gate electrode and the grounded Ohmic electrode surrounding the gate of the MIS structure at temperatures from 150 K to 393 K. Figure 2 shows the *C-V-f* characteristics at 150 K and 393 K. At 393 K, we observe a significant frequency dispersion for forward gate biases, which is attributed to electron trapping at interface states, while the frequency dispersion disappears at 150 K because of much longer electron trapping time constants. To characterize the interface states quantitatively, we carried out an analysis using the conductance method[32] based on the equivalent circuit of the MIS structures depicted in the inset of Fig. 3 (top), with the insulator capacitance C_0, the semiconductor capacitance C_s, the interface state capacitance C_i, and the interface state conductance G_i. Using the interface state density D_i and the electron trapping time constant τ, we obtain[33]

$$C_i = \frac{q^2 D_i \arctan(\omega\tau)}{\omega\tau} \tag{1}$$

and

$$\frac{G_i}{\omega} = \frac{q^2 D_i \ln(1+\omega^2\tau^2)}{2\omega\tau}, \tag{2}$$

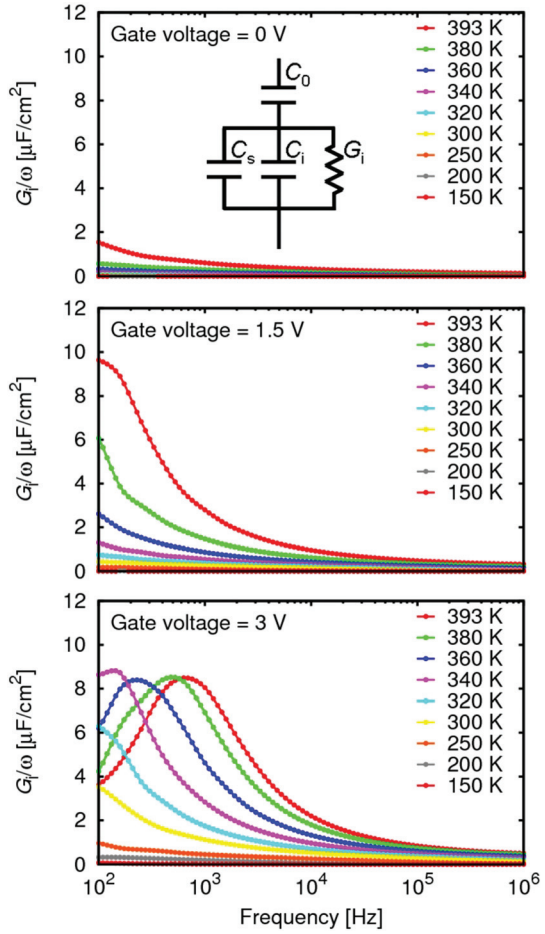

FIG. 3. Frequency dependence of G_i/ω for temperatures from 393 K to 150 K at gate voltages of 0 V (top), 1.5 V (middle), and 3 V (bottom). Top inset: the equivalent circuit of the MIS structures.

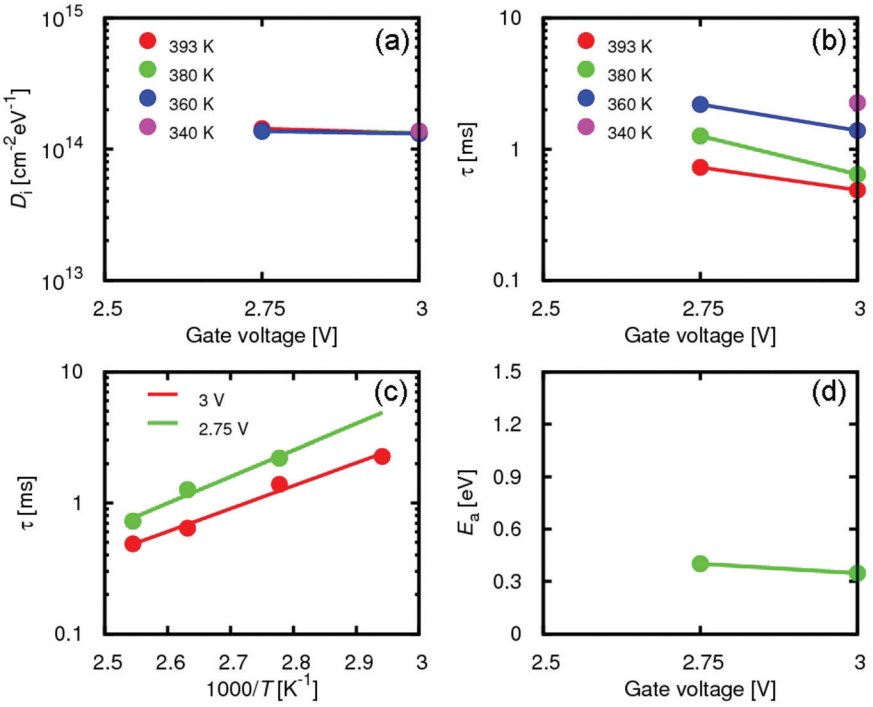

FIG. 4. (a) Interface state density D_i and (b) electron trapping time constant τ, obtained from the peak values and positions of the frequency-dependent G_i/ω based on the conductance method. (c) The Arrhenius plot of the temperature-dependent τ. (d) The activation energy E_a as a function of gate voltage, obtained from the Arrhenius plot (c).

where q is the electron charge and $\omega = 2\pi f$ is the angular frequency; G_i/ω as a function of frequency exhibits a single-peaked behavior, with the peak frequency $\sim 1/\pi\tau$ and the peak value $\sim 0.4q^2D_i$. Assuming the designed value of the insulator capacitance $C_0 = 610\,\mathrm{nF/cm^2}$, we show frequency dependence of G_i/ω, for several temperatures and gate voltages of 0 V, 1.5 V, and 3 V, in Fig. 3. As the gate voltage decreases, the number of peaks decreases due to longer time constants for deeper interface state energy levels. Thus, only a narrow range of the gate biases gives peaks in the measured frequency and temperature range; most peaks are below

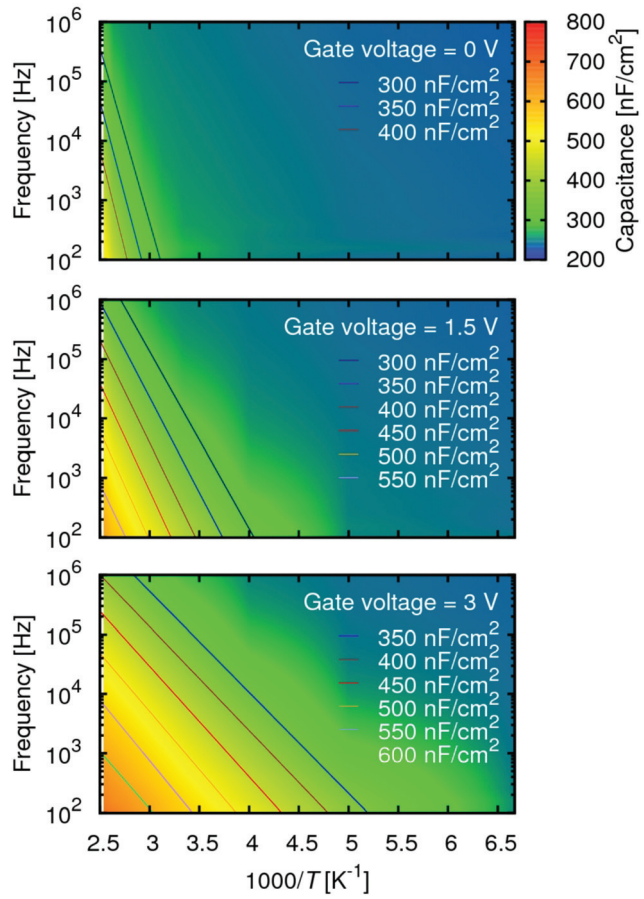

FIG. 5. *C-f-T* mappings with contours at gate voltages of 0 V (top), 1.5 V (middle), and 3 V (bottom).

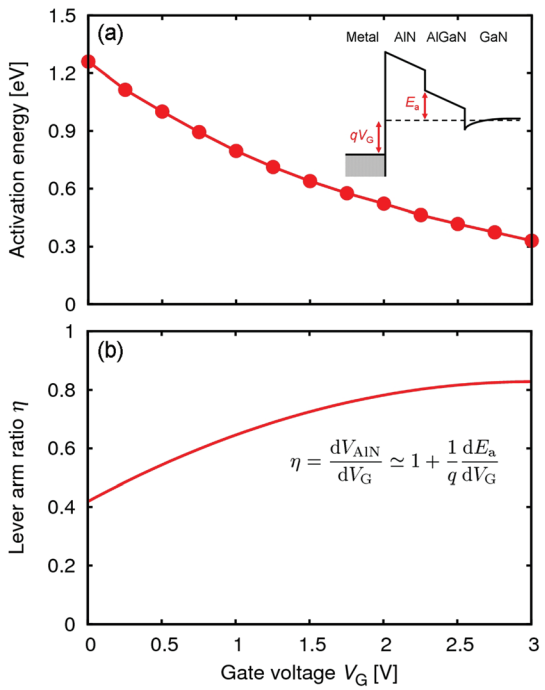

FIG. 6. (a) Gate voltage V_G dependence of the activation energy E_a extracted from the contours in *C-f-T* mappings. Inset: illustration of the bandbending and E_a. (b) Lever arm ratio $\eta = dV_{AlN}/dV_G \simeq 1 + q^{-1}dE_a/dV_G$.

100 Hz due to significantly long time constants for the wide bandgap of AlGaN/GaN systems. From the few peak positions and values, D_i and τ for temperatures of 340–393 K are obtained as shown in Figs. 4(a) and 4(b), respectively, where $D_i \sim 10^{14}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ and $\tau \sim$ ms. From the Arrhenius plot of the temperature dependence of τ shown in Fig. 4(c), given by $\tau = \tau_0 \exp(E_a/k_B T) = \tau_0 \exp(\beta E_a)$, we extracted the activation energy E_a shown in Fig. 4(d) and estimated $\tau_0 \sim 10$ ns. However, we have a problem that the conventional conductance method to investigate interface states is available only for a narrow range of gate biases, prohibiting the analysis of deeper interface states.

In order to solve the problem, we propose an analysis method using *C-f-T* mapping obtained from the temperature-dependent *C-V-f* characteristics. In Fig. 5, we show the *C-f-T* mappings at gate voltages of 0 V, 1.5 V, and 3 V, with contours. The contours exhibit a straight line behavior, which can be explained by the equivalent circuit of the MIS structures with a total admittance

$$Y = \frac{1}{Z} = \left(\frac{1}{jC_0\omega} + \frac{1}{G_i + jC_s\omega + jC_i\omega} \right)^{-1}. \qquad (3)$$

Since C_i given by Eq. (1) and G_i/ω by Eq. (2) are functions of only $\omega\tau$, the measured capacitance $C = \mathrm{Im}Y/\omega$ is a function of only $\omega\tau$. Therefore, a contour in *C- f- T* mapping, i.e., $C =$ constant leading to $\omega\tau = 2\pi f\tau =$ constant, exhibits a straight line behavior as expressed by $f \propto 1/\tau \propto \exp(-\beta E_a)$, from which the activation energy E_a corresponding to the interface state energy level can be extracted. Figure 6(a) shows the gate voltage V_G dependence of E_a extracted from the contours in the *C-f-T* mappings, with the inset illustrating the bandbending and E_a. In addition to the fact that the obtained values of E_a for the gate voltage ≥ 2.75 V are in good agreement with those obtained by the conductance method, we find that E_a can be obtained for a much extended range of the gate biases. This is due to slow $\omega\tau$ dependence of Eqs. (1) and (2); even though the frequency is far from the peak position $\sim 1/\pi\tau$, change in the *C-f-T* mapping is detectable. Furthermore, from the interface state energy levels corresponding to a wide range of the gate biases, the gate-control efficiency of the devices can be directly evaluated from the derivative dE_a/dV_G. As shown in the inset of Fig. 6(a), the gate voltage change ΔV_G is divided by the AlN gate insulator with ΔV_{AlN} and AlGaN/GaN. Since $\Delta V_G \simeq \Delta V_{AlN} - \Delta E_a/q$, we obtain a "lever arm ratio" $\eta = dV_{AlN}/dV_G \simeq 1 + q^{-1} dE_a/dV_G$ as shown in Fig. 6(b). We find that small negative values of dE_a/dV_G give large values of η near the unity corresponding to poor gate-control efficiencies. This analysis method is important as an auxiliary tool to the conventional conductance method.

In summary, we analyzed the AlN/AlGaN/GaN MIS-HFETs using *C-f-T* mapping for the investigation of AlN/AlGaN interface states. The analysis method gives the activation energies of electron trapping, namely the interface state energy levels, for a wide range of the gate biases. This method is auxiliary to the conventional conductance method, serving as a valuable tool for characterization of wide-bandgap devices with deep interface states. Furthermore, the method also enables a direct evaluation of the gate-control efficiency of the devices.

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