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Electrical transport characteristics of Sn/p-Si schottky contacts revealed from *I–V–T* and *C–V–T* measurements

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Abstract

The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of metal–semiconductor (Sn/p-Si) Schottky contacts were measured in the temperature range 150–400 K. The effect of the temperature on the series resistances R_S, ideality factors n, the barrier height Φ_b and interface state density N_{SS} obtained from the *I–V* and *C–V* characteristics were investigated. The n, Φ_b, R_S, and N_{SS} values were seen to be strongly temperature dependent. The ideality factors, series resistances and interface state densities decreased with increasing temperature for all diodes and the values of n, R_S, and N_{SS} obtained from *I–V* and *C–V* measurements were found in the ranges of 2.024–1.108, 2.083–1.121; 79.508–33.397 Ω; and 2.14×10^{13}–$0.216\times10^{13}\,\mathrm{cm^2\,eV^{-1}}$, 2.277×10^{13}–$0.254\times10^{13}\,\mathrm{cm^2\,eV^{-1}}$, respectively. The temperature dependence of energy distribution of interface state density (N_{SS}) profiles has been determined from *I–V* measurements by taking into account the bias dependence of the effective barrier height and ideality factor.
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1. Introduction

The study of the Schottky contact formation is vital for semiconductor devices. Due to the technological importance of Schottky barrier diodes (SBDs) which are of the most simple of the metal–semiconductor (MS) contact devices, a full understanding of the nature of their electrical characteristics is of greater interest. Schottky contacts are rectifying MS junctions, and their forward current consists of majority carriers injected from the semiconductor into the metal. The rectifying property of MS contacts was first described by Schottky [1] in the 1930s. The study of dependence of the Schottky diode characteristics on ambient temperature is important for practical applications and for understanding the current conduction mechanisms involved [2]. The phenomenon of Schottky contact formation at MS interfaces has been studied actively for over three decades. Schottky barrier height (SBH) on p-type Si is usually in the range 0.4–0.7 eV independent of the metallization [3–8].

At low temperatures idealities $n>1$ have been ascribed to several effects: (a) interface states at a thin oxide between the metal and the semiconductor [9,10], (b) tunneling currents in highly doped semiconductor [11], (c) image force lowering of the Schottky barrier in the electric field at the interface [12] and (d) generation/recombination currents within the space-charge region [11]. These four models describe extreme cases of Schottky contacts [14]. The ideality factor n is the result of the deformation of the spatial barrier distribution when a bias voltage is applied.

Several authors suggested many methods which can help in the determination of the series resistance [15–20]. Norde [16] has proposed a method for evaluation of the R_S from

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the forward I–V characteristics considering for an ideal Schottky contacts, namely with $n = 1$, but $n > 1$. His main idea was to determine the minimum of a function $F(V)$. There are disadvantages of this method. It considers only ideal diodes ($n = 1$), and the minimum of $F(V)$ vs. V plot may not be determined accurately [16,18]. Sato and Yasumura [17] used a function $F(V)$ similar to that of Norde [16]. Cheung et al. proposed another model and derived the diode parameters from only one single I–V measurement [19]. The Cheung's plots are determined from data of the downward curvature region in the forward I–V plot which results from the series resistance and the effects of interfacial parameters [19].

The first study on the interfaces layer in Schottky diodes was made by Cowley and Sze [21] who obtained their estimations from analysis of the barrier heights as a function of metal work function. The interface charge affects the electrical characteristics of the Schottky junctions, so that electrical measurements can be used to obtain interface charge properties. Most of the early work focused on the use of C–V characteristics to obtain this information [22]. For example, Crowell and Roberts [23] determined the energy distribution of surface state in Au–Si diodes from C–V characteristics reported by Archer and Atalla [24], but they did not consider whether the distribution was consistent with the I–V characteristics of the devices. Recently, Levine [25] has suggested that the anomalous I–V characteristics of the SBDs are consistent with a barrier model in which there is an exponential distribution of surface states and in which the barrier height is controlled by this energy distribution of surface states and the externally applied voltage. It is well known that interface properties have a dominant influence on the device performance, reliability and stability [26,27]. We have reported the density distribution of the interface state charges from the current–voltage and capacitance–voltage characteristics of the diodes with MS structure.

In this work, the I–V and C–V characteristics of Sn schottky contacts on a p-type Si substrate were measured in the temperature range 150–400 K. The temperature dependence of electrical characteristics of the main parameters such as ideality factors, barrier heights, series resistances and interface state densities obtained from different methods were investigated. The experimental results show that the dependances of ideality factors, barrier heights, series resistances and interface state densities with the main parameters were found to be strong function of temperature.

2. Experimental procedure

The diodes were prepared using p-type Si (1 0 0) wafers. A carrier concentration value of $N_A = 2.223 \times 10^{15}\,\mathrm{cm}^{-3}$ for the Si wafer was found from C–V measurements at room temperature (for 300 K), and the corresponding resistivity value was $\rho = 6.248\,\Omega\,\mathrm{cm}$. The wafer was chemically cleaned using the RCA cleaning procedure. The native oxide on the front surface of the substrate was removed in HF:H_2O(1:10) solution and finally the wafer was rinsed in de-ionized water for 30 s. Then, low resistivity ohmic back contact to p-type Si (1 0 0) wafers was made by using Al, followed by a temperature treatment at 570 °C for 3 min in N_2 atmosphere. The Schottky contacts were formed by evaporation of Sn dots with diameter of about 1.5 mm (diode area $= 1.76 \times 10^{-2}\,\mathrm{cm}^2$). All evaporation processes were carried out in a turbo-molecular fitted vacuum coating unit at about 10^{-6} mbar. The I–V characteristics of the devices were measured in the temperature range 150–400 K using a temperature controlled janes vpf-475 cryostat, which enables us to make measurements in the temperature range 77–450 K, and a Keithly 220 programmable constant current source and a Keithly 199 dmm/scanner under dark conditions. The capacitance–voltage (C–V) measurements were performed using an HP 4192A LF Impedance Analyzer. The sample temperature was always monitored by using a copper–constantan thermocouple and a lakeshore 321 auto-tuning temperature controller with sensitivity better than ±0.1 K.

3. Results and discussion

3.1. Temperature dependence of ideality factors from the forward bias I–V and the reverse bias C–V characteristics

The forward current–voltage (I–V) and the reverse capacitance–voltage (C–V) characteristics of Sn Schottky contacts on p-type Si (1 0 0) in the temperature range 150–400 K are shown in Figs. 1 and 2, respectively. While, the experimental value of Φ_{IV} decrease with a decrease in

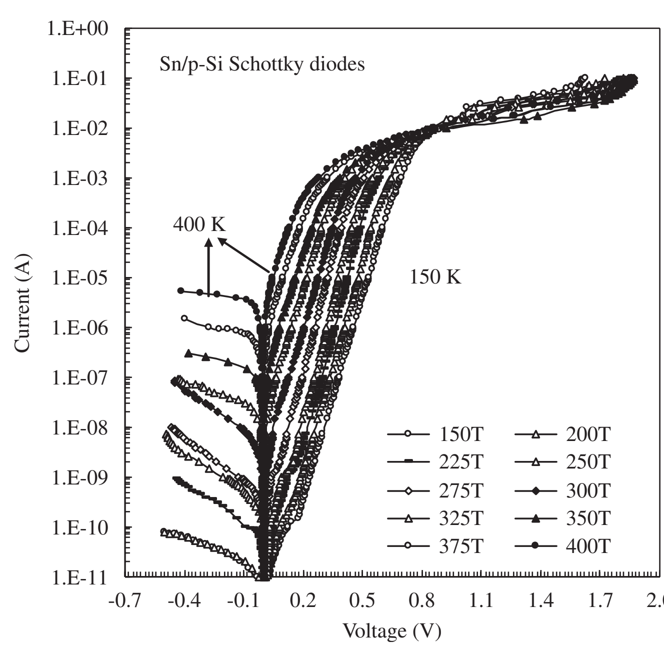

Fig. 1. Experimental forward current–voltage characteristics of the Sn/p-Si Schottky diode at various temperatures.

temperature, in contrary, experimental values of Φ_{CV} increase with a decrease in temperature. The temperature dependence of the I–V and the C–V barrier heights for the studied junctions for 10 different temperatures are in the range 0.512–1.023 eV (for 150 K) to 0.832–0.960 eV (for 400 K), respectively. In Table 1 and Fig. 3, it is shown that the ideality factors obtained from both the I–V and C–V measurements were found to increase with decreasing temperature. The barrier height Φ_{CV} obtained from C–V measurements slightly decreases with increasing temperature. This is a usual behavior of Schottky diodes, which indicates that interface states are bound to the valence band edge. This suggests that in this temperature range the current flow is dominated by thermionic emission. However, both the apparent barrier height and the ideality factor depend significantly on the temperature at low temperatures. This is the so called T_0 effect in its general meaning [28,29], which can be connected either with the lateral inhomogeneity of the barrier heights or with the domination of thermionic field emission (TFE) at low temperatures [29,30].

Current transport in Schottky contacts is due to majority carriers and it may be described by thermionic emission over the interface barrier [11]. The thermionic current can be written as;

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{kT}\right)\right], \tag{1}$$

and

$$I_0 = AA^* T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right), \tag{2}$$

where I_0 is the saturation current density, q the electron charge, V the definite forward-bias voltage, A the effective diode area, k the Boltzmann's constant, T the absolute temperature, and A^* the effective Richardson's constant of 32 $\mathrm{A cm^{-2} K^{-2}}$ for p-type Si. The slope of the I–V curve in Fig. 1 also gives the ''ideality factor'' of the contact, defined by [26]

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right). \tag{3}$$

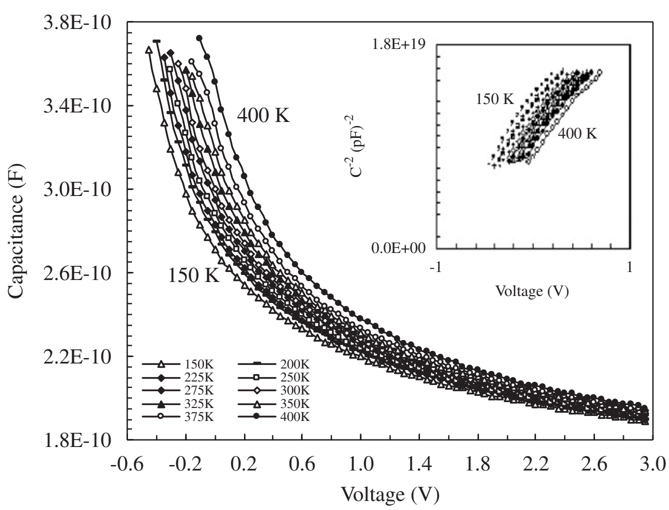

Fig. 2. The reverse bias C–V and C^{-2}–V plots of Sn/p-Si Schottky diode at various temperatures.

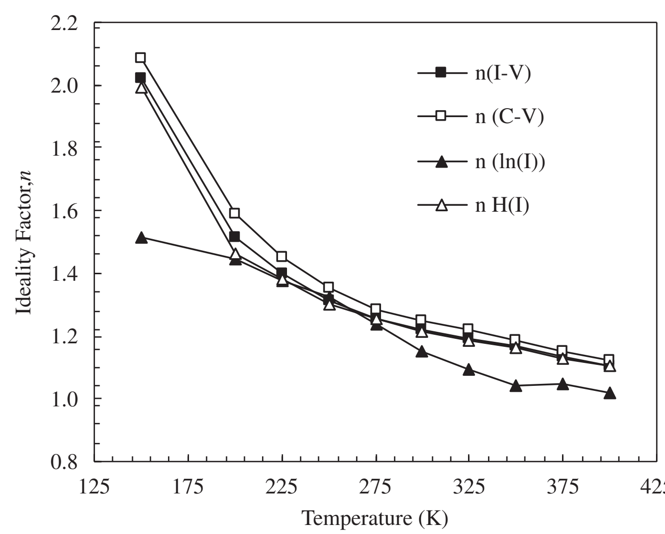

Fig. 3. Temperature dependence of the ideality factors obtained from various methods for Sn/p-Si Schottky diode.

Table 1
Temperature dependent values of various experimental parameters obtained from I–V and C–V measurements of Sn/p-Si Schottky diodes

T (K)	$\Phi_{I\text{–}V}$ (eV)	$\Phi_{C\text{–}V}$ (eV)	n from I–V	n from C–V	N from $H(I)$–I	n from dV/d(ln I)–I	R_s from dV/d(ln I)–I (Ω)	R_s from $H(I)$–I (Ω)	R_s from $F(V)$ (Ω)	N_{SS} from I–V (10^{13} $\mathrm{eV^{-1}\,cm^{-2}}$)	N_{SS} from C–V) (10^{13} $\mathrm{eV^{-1}\,cm^{-2}}$)
150	0.512	1.023	2.024	2.083	1.993	1.514	65.749	77.263	79.508	2.144	2.277
200	0.689	1.010	1.515	1.587	1.464	1.443	57.102	67.569	69.948	1.073	1.234
225	0.724	1.000	1.401	1.428	1.379	1.376	51.584	61.148	66.055	0.834	0.944
250	0.762	0.996	1.313	1.351	1.302	1.325	46.983	56.266	61.133	0.648	0.738
275	0.781	0.990	1.257	1.283	1.254	1.239	43.620	53.238	58.750	0.530	0.595
300	0.803	0.984	1.22	1.250	1.213	1.151	40.602	50.098	57.552	0.452	0.526
325	0.812	0.979	1.19	1.218	1.183	1.091	36.009	50.820	56.734	0.389	0.458
350	0.821	0.973	1.168	1.185	1.163	1.040	32.451	49.752	55.791	0.342	0.390
375	0.828	0.967	1.135	1.153	1.127	1.048	33.240	51.112	54.884	0.273	0.322
400	0.832	0.960	1.108	1.121	1.105	1.017	33.397	50.772	54.411	0.216	0.254

The experimental value of n_{IV} derived from I–V data varies from 2.024 (for 150 K) to 1.108 (for 400 K). Furthermore, as can be seen in Table 1 and Fig. 3, the values of the ideality factor obtained from I–V, C–V measurements and $\mathrm{d}V/\mathrm{d}(\ln I)-I$ and $H(I)-I$ plots are in close agreement with each other. The barrier height is determined, at each temperature from Eq. (2) according to

$$\Phi_{b0} = \frac{kT}{q}\ln\left[\frac{AA^{*}T^{2}}{I_0}\right]. \tag{4}$$

The zero bias barrier height obtained from I–V characteristics is smaller than obtained from C–V measurement, as expected.

The reverse bias capacitance measurements are made at a very high frequency (500 kHz). The C–V characteristics of the MS diodes at 500 kHz frequency are shown in Fig. 2. The C^2–V relationship applicable to intimate MS Schottky barriers on uniformly doped materials can be written as [13,31]

$$\frac{1}{C^2} = \frac{2(V_R - V_0)}{qN_A\varepsilon_S A^2}, \tag{5}$$

where V_R is the reverse bias voltage, V_0 the built-in voltage, q the electronic charge, and N_A the doping concentration. The diffusion potential or built-in potential is usually measured by extrapolating C^2–V plot to the V-axis (it has been shown in Fig. 2). An insulating layer can modify these characteristics if the potential across the layer changes with bias. The zero bias barrier height from C–V measurement is defined by

$$\Phi_{CV} = V_D + E_F - \Delta\Phi_B, \tag{6}$$

where V_D is the diffusion potential, E_F the Fermi energy and $\Delta\Phi_B$ the Schottky barrier lowering. The slope of the C^2V curve also gives the "ideality factor" of the contact, defined by

$$C_2 = \frac{N_{A(\text{experimental})}}{N_{A(\text{theoretical})}}, \tag{7}$$

$$n_{CV} = \frac{1}{C^2}, \tag{8}$$

where, $N_{A(\text{experimental})}$ are the carrier concentration values obtained from C–V measurements in the temperature range 150–400 K, and $N_{A(\text{theoretical})}$ is the carrier concentration obtained for p-Si using Eq. (10):

$$N_{A(\text{experimental})} = \frac{2}{q\varepsilon_S A^2}\frac{\mathrm{d}\ln(I)}{\mathrm{d}V}, \tag{9}$$

and

$$N_{A(\text{theoretical})} = \frac{1}{q\mu\rho}, \tag{10}$$

respectively.

Furthermore, the values of Φ_{b0} (indicated by open circles) and Φ_{C-V} (indicated by open triangles) obtained from the forward bias I–V and the reverse bias C^2–V characteristics (Fig. 2) depending on the temperature are given in Fig. 4 and Table 1, respectively. The experimental value of Φ_{b0} decreased with a decrease in temperature, as can be seen in Fig. 4. Since current transport across the MS interface is a temperature-activated process, electrons at low temperatures are able to surmount the lower barriers and therefore, current transport will be dominated by current flowing through the patches of lower SBH and a larger ideality factor [20,30]. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant BH will increase with the temperature and bias voltage [20,30].

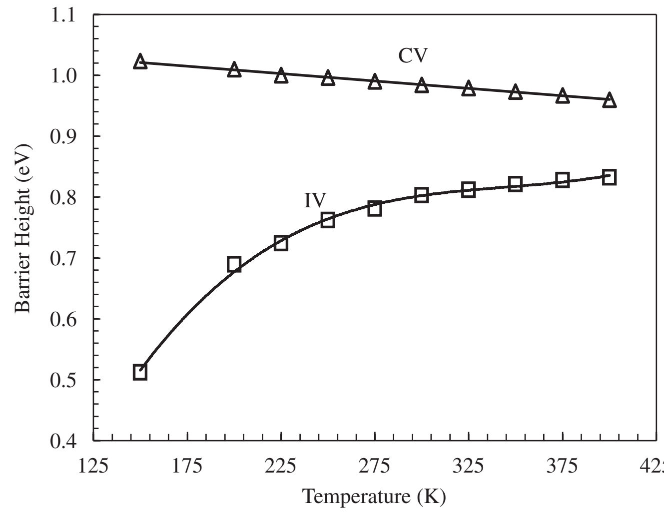

Fig. 4. Temperature dependence of the ideality factors obtained from various methods for Sn/p-Si Schottky diode.

3.2. Temperature dependence of series resistance

Temperature dependency and the series resistance effect on the electrical characteristics of the Sn/p-Si MS Schottky diode were investigated in the temperature range 150–400 K. The series resistance is a very important parameter of Schottky diode. The resistance of the Schottky diode is the sum total resistance value of the resistors in series and resistance in semiconductor device in the direction of current flow. As shown in Fig. 1, current–voltage characteristics of the Sn/p-type Si Schottky contact show rectification behavior. Here, the series resistances were evaluated from the forward bias I–V data using methods developed both by Cheung [19] and Norde [16]. The forward bias current–voltage characteristics due to thermionic emission of a Schottky contact with the series resistance can be expressed as [11,26,32] Cheung's functions:

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = IR_s + n\left(\frac{kT}{q}\right), \tag{11}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{*}T^{2}}\right), \tag{12}$$

and

$$H(I) = IR_s + n\Phi_b, \tag{13}$$

should give a straight line for the data of downward curvature region in the forward bias I–V characteristics. In Figs. 5(a) and (b), experimental $H(I)$ vs. I and $dV/d(\ln I)$ vs. I plots are presented at different temperatures for Sn/p-Si MS Schottky diode, respectively. Eq. (11) should give straight line for the data of downward curvature region in the forward bias I–V characteristics. Thus, a plot of $dV/d(\ln I)$ vs. I will give R_s as the slope and $n(kT/q)$ as the y-axis intercept. As a function of temperature, the values of n (obtained from plots $H(I)$ vs. I and $dV/d(\ln I)$) and R_s derived from Figs. 5(a) and (b) are given in Table 1. Using the n value determined from Eq. (11), a plots of $H(I)$ vs. I will also give a straight line (as shown in Fig. 5(a)) with y-axis intercept equal to $n\Phi_b$. The slope of these plots also provides a second determination of R_s, which can be used to check the consistency of this approach. Thus, for each temperature performing different plots Eqs. (11) and (13) of the I–V data we obtained three main diode parameters given in Table 1. Furthermore, Norde's functions [16]

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I}{AA^{*}T^{2}}\right), \tag{14}$$

$$R_S = \frac{\gamma - n}{I}\frac{kT}{q}, \tag{15}$$

where γ is a constant number($\gamma \geqslant n$), n is the ideality factor obtained from I–V measurements, q the electronic charge and I gives the current I_0 at the minimum point of $F(V)$ as shown Fig. 6.

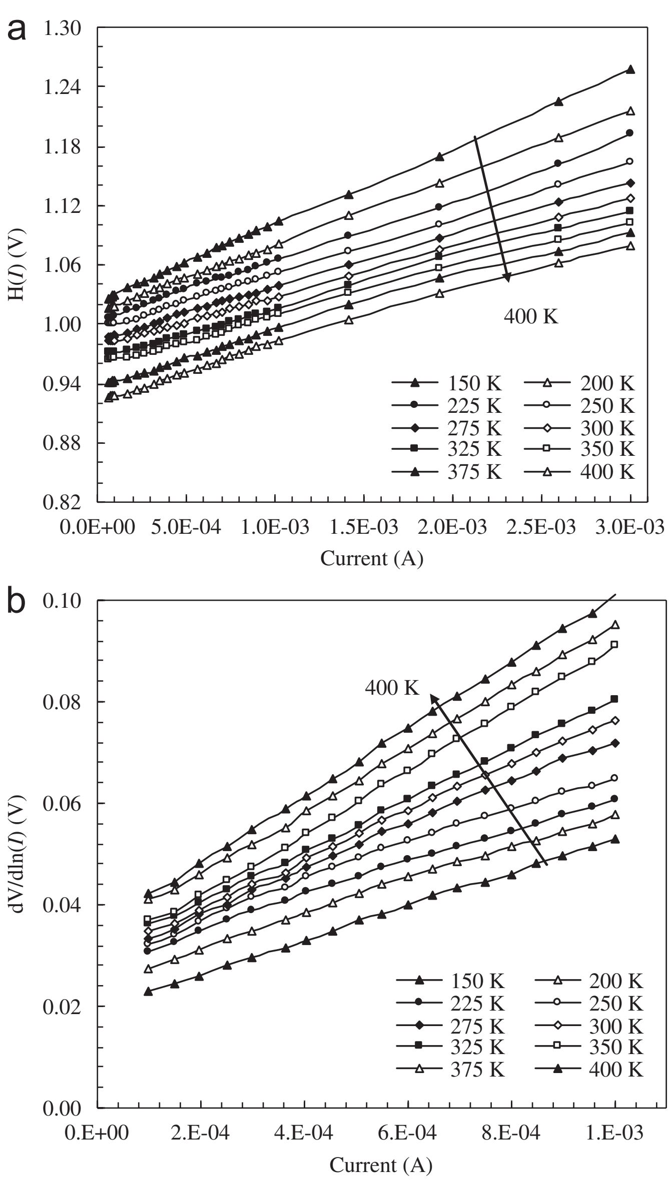

Fig. 5. (a) Plots of $H(I)$ vs. I, and (b) $dV/d\ln(I)$ vs. I for Sn/p-Si Schottky diodes at various temperatures.

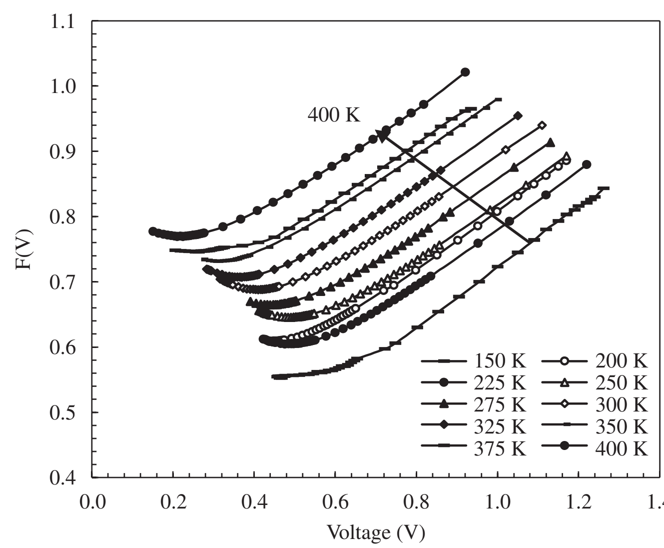

Fig. 6. Temperature dependence of $F(V)$ vs. V plot of Sn/p-Si Schottky diode.

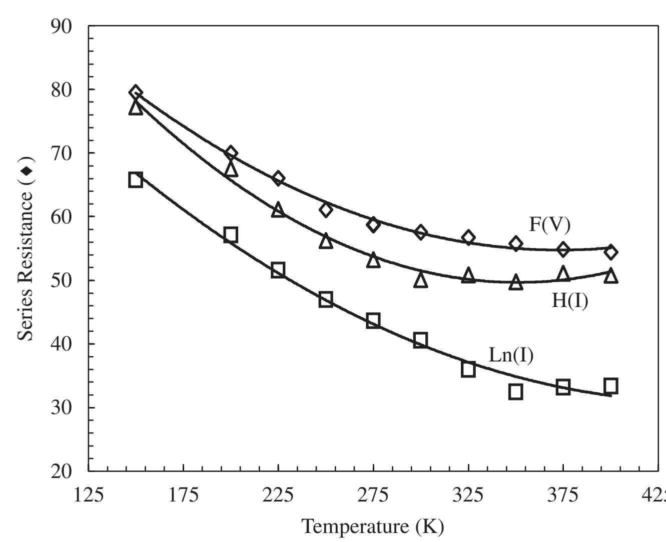

Fig. 7. Temperature dependence of the series resistances obtained from various methods for Sn/p-Si Schottky diode.

Fig. 7 shows the experimental series resistance values from the semi-log forward bias I–V characteristics as a function of temperature. These values are given in Table 1. The increase of R_S with the fall of temperature is believed to result due to factors responsible for increase of n_{IV} and lack of free carrier concentration at low temperatures [33]. Thus, for each temperature and by performing plots (Eqs. (11), (13) and (15)) of the I–V data, two main diode parameters (n and R_S) are obtained and given in Table 1. As shown in Table 1, the n and R_S values measured by different techniques are in good agreement with each other and both decrease strongly with increasing temperature.

3.3. Interface state density from I–V and C–V characteristics

The most important characteristic of the MS interface is the nature of the potential barrier between the Fermi level in the metal and the majority carrier's band edge of the semiconductor at that interface. This potential barrier is of central importance in determining the performance of semiconductor devices since electrical contacts to semiconductors necessitate MS interfaces and, depending upon the barrier height, such interfaces will exhibit a modest resistance to current flow in either direction over a large temperature range or a low resistance to current flow in one direction and high resistance to current flow in the opposite direction [34]. The charge at MS interfaces can account for the difference between the predicted and the observed Schottky barrier height. Thus, in a p-type semiconductor, the energy of the interface states E_{SS} with respect to the top of the valance band at the surface of the semiconductor is given by [20,35]

$$E_{SS} - E_V = q(\Phi_b - V), \tag{16}$$

where

$$\Phi_b = \Phi_{bf} + \left(1 + \frac{1}{n(V)}\right)V, \tag{17}$$

and the flat band barrier Φ_{bf} is the fundamental barrier, which should be used when comparing experiments with theory. It was shown earlier that the flat band barrier Φ_{bf} can be calculated from the zero bias barriers Φ_{IV} by using [35],

$$\Phi_{bf} = n_{IV}\Phi_{IV} - (n_{IV} - 1)\frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right), \tag{18}$$

where N_v is the effective density of states in the valence band. The energy distribution or density distribution curves of the interface states were obtained from experimental data of this region of the forward bias I–V (in Fig. 1) and given in Fig. 8. Fig. 8 shows the resulting dependence of N_{SS} converted to a function of E_{SS} using Eq. (16) at various temperatures. We have observed then the mean N_{SS} increases when the temperature increases. As can be seen in Fig. 8, exponential growth of the interface sate density towards the top of the valance band is very apparent. This state agrees with distribution obtained method Schottky capacitance spectroscopy and in I–V dates at literature values as range of interface state density.

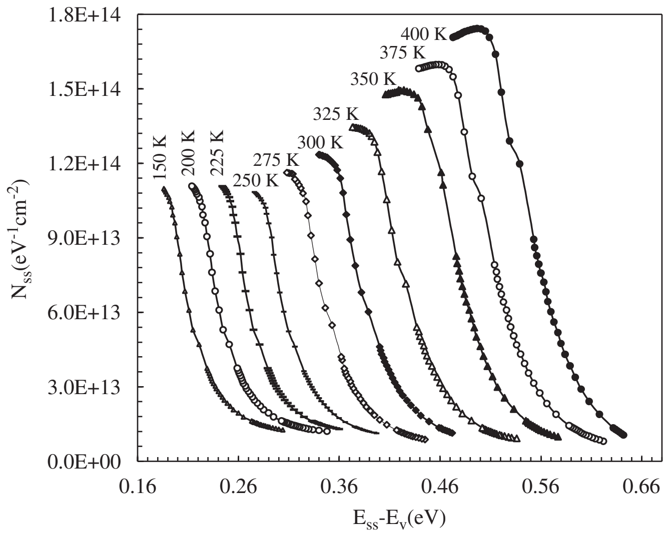

Fig. 8. Density of interface states N_{SS} as a functions of E_{SS}–E_V deduced from the I–V measurement at various temperatures.

For a real Schottky diode having interface states in equilibrium with the semiconductor, the ideality factor, n becomes greater than unity as proposed by Card and Rhodercik [10] and is given by

$$n = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W} + qN_{SS}\right], \tag{19}$$

where W is the space charge width, and N_{SS} the density of interface states in equilibrium with the semiconductor; ε_s and ε_i are the permittivities of the semiconductor and the interfacial layer, respectively. The density distribution curves of the interface states can be thus obtained from experimental data of the forward bias I–V in Fig. 1. Fig. 8 shows the resulting dependence of N_{SS} converted to a function of E_{SS} using Eq. (16) at various temperatures. The potential drop across the interfacial layer varies with bias because of the change in the charge in the interface states and thus the interface state energy distribution and it alerts the diffusion potential and therefore the depletion capacitance [11,20,26,36].

In addition the values of N_{SS} ($= D_{it}$) obtained as a function of temperature from I–V and C–V measurements are shown in Fig. 9 and are listed in Table 1. As shown in Fig. 9 and Table 1, the values of N_{SS} obtained from the both I–V and C–V characteristics were found to increase with decreasing temperature. The explanation of interface state distribution obtained from the both I–V and C–V measurements as a function temperature of a Schottky contact with the series resistance can be expressed, respectively, as below:

$$D_{it_{IV}} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n-1) - \frac{\varepsilon_s}{W}\right], \tag{20}$$

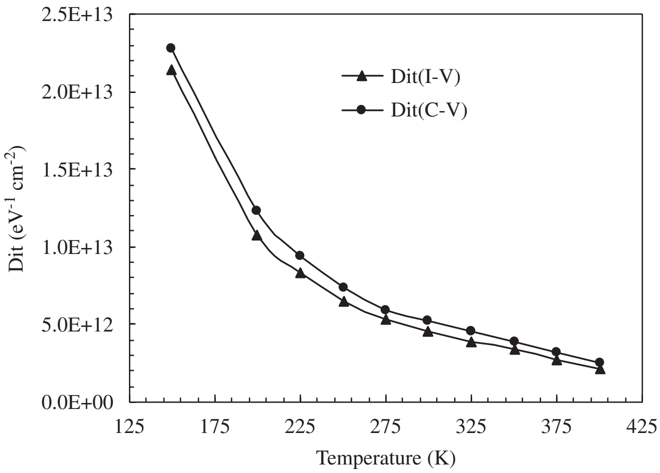

Fig. 9. Temperature dependence of interface states density N_{SS} (D_{it}) deduced from the I–V and C–V measurements at various temperatures.

$$D_{it_{CV}} = \frac{\varepsilon_i(1 - c_2)}{c_2 \delta q}, \quad (21)$$

where, W is the space charge width, D_{it} the density of acceptor-like interface states assuming over the energy range from barrier height to the Fermi level; C_2 is a parameter inverse of the well-known ideality n which is a measure of conformity of the diode to pure thermionic emission and the values of n were determined by applying the slope of the C^2 vs. V plot shown in Fig. 2 to Eq. (8), δ is the thickness of the interface layer and ε_s, ε_i are the permittivities of the semiconductor and the interfacial layer, respectively. As can be seen in Fig. 9, the interface state densities N_{SS} ($= D_{it}$) obtained from I–V and C–V measurements at different temperatures agree with each other and decrease with increasing temperature.

4. Conclusion

The current–voltage (I–V) and capacitance–voltage (C–V) characteristics of Sn/p-Si metal–semiconductor (MS) Schottky diodes were measured in the temperature range 150–400 K. While the barrier height Φ_{IV} increases, the barrier height Φ_{CV} decreases with an increase in temperature. It was seen that the barrier height deduced from I–V measurement is always smaller than the arithmetic average of the barrier height deduced from C–V measurements. This difference is mainly due to the presence of a thin compensated layer at the interface. While the zero-bias barrier height Φ_{IV} increased, ideality factor n decreased with increasing temperature. Thus, at high temperatures, this situation can be successfully explained on the basis of thermionic emission (TE) mechanism. However, the changes are quite significant at low temperature and this is the so called T_0 effect in its general meaning, which can be connected either with the lateral inhomogeneity of the barrier heights or with the domination of thermionic field emission (TFE) mechanism. The interface states at the MS interface play an important role in the determination of the characteristic parameters of the devices. The interface states density N_{SS} obtained from forward bias current–voltage characteristics at different temperatures increased with increasing temperature, and at the same, the density of interface states distribution profile as a function of E_{SS}–E_V obtained from I–V measurements increased with increasing temperature. The interface state densities have an exponential rise with bias from the midgap towards the top of the valence band of the p-Si. The exponential growth of the interface state density towards the top of the valance band is very apparent. Furthermore, we have reported that the interface state density N_{SS} obtained from the I–V and C–V measurements at different temperatures agrees with each other and decreased with increasing temperature.

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