Conducting atomic force microscopy for nanoscale electrical characterization of thin SiO₂

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(Received 24 June 1998; accepted for publication 21 September 1998)

In this work, we demonstrate the applicability of conducting atomic force microscopy (AFM) for the quantitative electrical characterization of thin (3–40 nm) ${\rm SiO_2}$ films on a nanometer scale length. Fowler–Nordheim (F–N) tunneling currents on the order of 0.02–1 pA are measured simultaneously with the oxide surface topography by applying a voltage between the AFM tip and the silicon substrate. Current variations in the F–N current images are correlated to local variations of the oxide thickness on the order of several angströms to nanometers. From the microscopic current–voltage characteristics the local oxide thickness can be obtained with an accuracy of ± 0.3 nm. Local oxide thinning of up to 3.3 nm was found at the edge between gate oxide and field oxide of a metal-oxide-semiconductor capacitor with a 20-nm-thick gate oxide. © 1998 American Institute of Physics. [S0003-6951(98)01247-9]

One of the simplest and yet most attention demanding process modules in the development and manufacturing of very-large-scale integration (VLSI) and ultralarge-scale integration (ULSI) are the gate dielectrics. A structurally and electrically homogeneous oxide is of primary importance in order to comply with the requirements for reliability and long term stability of metal-oxide-semiconductor (MOS) gate and tunneling oxides. Otherwise degradation and breakdown leads to early device failure. Even variations of oxide thickness in the angström range can have a large impact on the threshold voltage of MOS devices and lead to locally enhanced stress. With decreasing oxide thickness this problem becomes much more severe. Surface and interface roughness result in increasing oxide fields and enhance leakage currents and Fowler-Nordheim tunneling, leading to fast degradation and limiting the scaling of oxides for MOS devices.2

Extrinsic defects, like oxide thinning are often introduced by the local oxidation of silicon (LOCOS) process, which is used to isolate the active areas of separate transistors by the growth of a thick field oxide (FOX). The reduced oxide thickness at the transition region between the FOX and the gate oxide (GOX) (LOCOS boundary) leads to increased electric field in the oxide and determines the electric field the device can sustain.³

In order to overcome the problems mentioned above a technique with high lateral resolution (\sim 10 nm) for the fast assessment of oxide quality is needed. To locate and quantitatively measure the degree of oxide thinning conventional measurement techniques, like macroscopic current–voltage (I–V) and capacitance–voltage (C–V) spectroscopy, emission microscopy (EM), and transmission electron microscopy (TEM) are not adequate. There have been several attempts based on scanning probe microscopy to get microscopic electrical information on weak spots in thin SiO₂ including scanning tunneling microscopy (STM), bal-

listic electron emission microscopy (BEEM), scanning capacitance microscopy (SCM), and conducting atomic force microscopy (C-AFM).^{4–12} STM and BEEM require an expensive experimental setup, e.g., ultrahigh vacuum conditions, which make them inadequate for a routine process monitoring. SCM suffers from a limited lateral resolution (~50 nm) and sensitivity to oxide thickness. This makes C-AFM the most promising method due to its easy use, superior lateral resolution (~10 nm), and extreme sensitivity to oxide thickness.¹²

In this letter, we demonstrate the applicability of C-AFM for the localization of oxide thinning and for the quantitative determination of the local oxide thickness from microscopic I-V curves.

Figure 1 shows schematically the experimental setup for C-AFM. We used a contact AFM equipped with a two stage picoamp-amplifier (400 Hz bandwidth). $^{13-15}$ A constant voltage is applied between the conductive tip and the substrate and Fowler–Nordheim (F–N) currents are measured simultaneously with the topography at a noise level <20 fA at a typical scan rate of 0.2 Hz. Additionally, local I-V curves can be obtained.

The current through the oxide is determined by field-assisted tunneling through the barrier formed at the injecting electrode/ SiO_2 interface and can be written as

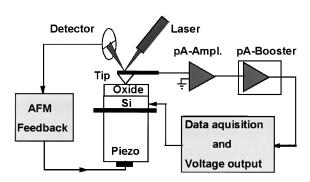


FIG. 1. Experimental setup for conducting AFM (C-AFM).

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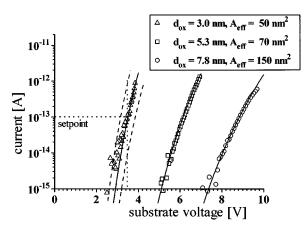


FIG. 2. Microscopic I-V characteristics (symbols) measured by conducting AFM on SiO₂ films of different thickness. The ellipsometric thicknesses $d_{\rm ox}$ are 3.0 (\triangle), 5.3 (\square), and 7.7 nm (\bigcirc). The straight lines represent the Fowler–Nordheim current fits to the experimental data. The corresponding fit parameters are shown in the inset. The dashed curves represent the I-V curves expected for a 2.7 (left curve) and a 3.3 nm oxide (right curve).

$$I = A_{\text{eff}} \frac{q^2 m_0}{8 \pi h m_{\text{eff}}} \frac{1}{t(E)^2} \frac{\beta^2 V^2}{\Phi d_{\text{ox}}^2}$$

$$\times \exp \left(-\frac{8 \pi \sqrt{2 m_{\text{eff}} q}}{3 h} v(E) \frac{d_{\text{ox}}}{\beta V} \Phi^{3/2} \right), \tag{1}$$

where $A_{\rm eff}$ is the effective emission area at the injecting electrode, q is the electron charge, h is Planck's constant, $m_{\rm eff}/m_0=0.5$ is the effective mass of the electron in the conduction band of SiO₂, $d_{\rm ox}$ is the oxide thickness, and Φ is the barrier height. Image charge lowering is taken into account by the functions v(E) and t(E). ^{16,17} For the fields of interest (10–13 MV/cm) v(E) and t(E) are \approx 0.937 and \approx 1.011, respectively. ¹⁶ The field enhancement factor β arises from the nonplanar geometry of the tip and has to be considered for injection from the tip. ¹⁰ In all measurements the substrate was biased negatively, i.e., electron injection occurred from the substrate. ¹²

Two types of samples have been used. The samples used for the I-V spectroscopy consist of device grade SiO_2 of different thickness, thermally grown on p-doped Si (100) wafers ($N_A = 10^{15} \, \mathrm{cm}^{-3}$). The oxide thicknesses d_{ox} were 3.0 ± 0.25 , 5.3 ± 0.25 , and 7.8 ± 0.25 nm as determined by ellipsometry and x-ray reflectometry. The sample used for the F-N current imaging was deprocessed from a fully processed test capacitor. The poly-Si gate was removed by a highly selective etch (selectivity against $\mathrm{SiO}_2 > 1:2000$) in KOH (10%) at room temperature.

Figure 2 shows microscopic I-V characteristics obtained on the untreated oxides of different thickness with a Si tip coated with 100 nm boron-doped diamond $(0.1~\Omega~cm)$. Individual spectra obtained on different locations of the same oxide yield nearly identical I-V curves shifted horizontally within $\pm 0.25~V$. This is in agreement with the local variations in oxide topography. The root mean square (rms) roughness was about 0.15 nm leading to a peak-to-peak roughness of 0.4–0.5 nm which corresponds to voltage shifts of about $\pm 0.25~V$.

The straight lines in Fig. 2 are the fits of the F-N Eq. (1) to the experimental I-V curves. The barrier height Φ for

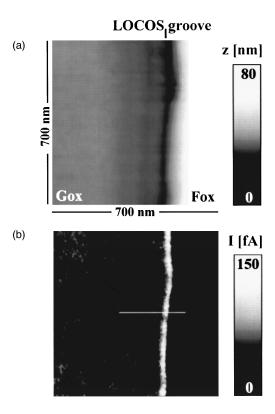


FIG. 3. Topography (a) and simultaneously measured Fowler–Nordheim current image (b) at the transition region between the gate oxide (GOX) and the field oxide (FOX) of a 20-nm-thick gate oxide at a constant tip voltage of 18.7 V. A series of I-V ramps spaced 10 nm was performed along the white line

injection from the substrate is assumed to be 3.25 eV.¹⁵ The fit parameters are $d_{\rm ox}$ and $A_{\rm eff}$. They are shown in the inset of Fig. 2. The oxide thicknesses are found to be 3.0 ± 0.3 , 5.3 ± 0.3 , and 7.8 ± 0.3 nm and are in excellent agreement with the values obtained by ellipsometry. The effective emission areas are determined to be 50 ± 20 , 70 ± 30 , and 150 ± 40 nm², respectively. $A_{\rm eff}$ values on the order of 30-250 nm² are reasonable for 3 nm $\leq d_{\rm ox} \leq 20$ nm, taking into account the angular distribution of the F–N currents emitted from the Si/SiO₂ interface of the MOS structure formed by the tip with a contact radius on the order of 2–8 nm and the substrate. From the angular distribution of the F–N current an increase of $A_{\rm eff}$ with insulator thickness is expected and in agreement with the experimental results.

The extreme sensitivity of the F-N currents to local variations in oxide thickness can be used for the localization of weak spots, like oxide thinning, in otherwise homogeneous oxides. The dashed lines in Fig. 2 represent the F-N currents expected for a 2.7 and 3.3 nm oxide calculated according to Eq. (1). The choice of a setpoint voltage, as illustrated by the dotted line in Fig. 2 for a 3 nm oxide, leads to a reduction or enhancement of the F-N current by a factor of about 10, when the local oxide thickness is increased or decreased by 0.3 nm. This sensitivity is used for the monitoring of microscopic thickness variations of thin oxides as illustrated in Fig. 3. The topography [Fig. 3(a)] and the F-N current image [Fig. 3(b)] were simultaneously recorded at the LOCOS boundary of a 20 nm gate oxide with a bulk diamond tip (boron doped). Tip voltage was 18.7 V. The characteristic shape of the LOCOS groove is clearly visible

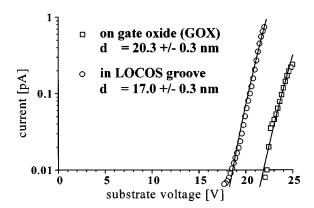


FIG. 4. Two I-V curves of a series of I-V ramps taken on a 20 nm oxide along the white line shown in Fig. 3.

in the topographical image. But due to the lack of knowledge about the precise shape of the Si beneath the oxide, no information on the homogeneity of the oxide thickness can be deduced from the topography.⁴ In contrast, in the F–N current image an excess current is measured at the LOCOS groove, whereas the current is below detection limit at the GOX and FOX regions. The excess F–N current flow clearly indicates oxide thinning at the LOCOS boundary. This has been confirmed by cross sectional transmission electron microscopy (TEM) made on similar MOS capacitors before deprocessing.⁴ Oxide thinning introduced by the preparation was also excluded by the comparison of the deprocessed oxide with those directly pulled after oxidation.

In order to quantitatively determine the amount of oxide thinning a series of I-V ramps was performed along the white line indicated in Fig. 3(b). The distance between each I-V curve was 10 nm. Two I-V curves are shown in Fig. 4. The first one was obtained at the GOX and represents the nominal oxide thickness. The other I-V curve was obtained at the LOCOS edge and represents the thinnest location of the oxide along this line. The corresponding F-N fits yield $A_{\text{eff}} = 200 \pm 50 \,\text{nm}^2$ and an oxide thickness of 20.3 ± 0.3 and 17±0.3 nm within the GOX and at the LOCOS edge, respectively. The LOCOS groove of Fig. 3(a) has a lateral extension of about 250 nm and a depth of 13 nm. With a tip radius of 20-30 nm, as measured by high resolution scanning electron microscopy, no significant increase of the tip sample contact area and thus $A_{\rm eff}$ within the groove is expected. In the F–N fit the uncertainty in A_{eff} of $\pm 50 \text{ nm}^2$ corresponds to an error in d_{ox} of only about ± 0.08 nm. Thus, the increase in current cannot be explained by an increased tip area, but is attributed to oxide thinning. The degree of oxide thinning introduced by the LOCOS process for this gate oxide is at least 3.3 nm.

Because of the small currents used in the experiments no modification of the gate oxide due to the measurement was found, neither in spectroscopy nor in F-N current imaging and the results are reproducible in detail in successive mea-

surements. To avoid the risk of excessive F-N currents we also performed measurements with a F-N current feedback. But due to the large displacement currents induced by the tip sample capacitance (≈ 0.1 pF), the results obtained are unreliable.

In conclusion, we demonstrated conducting AFM (C-AFM) to be a highly sensitive technique for the determination of the local oxide thickness with a thickness resolution on the order of 0.3 nm. The lateral resolution is about 10 nm. Fowler–Nordheim current maps simultaneously acquired with the oxide topography at constant tip-sample voltage, have been used for the detection of oxide thinning at the LOCOS edge of a 20 nm MOS capacitor. The local *I–V* curves obtained at the LOCOS edge and gate oxide reveal an oxide thickness difference of 3.3 nm. With decreasing gate oxide thickness (<5 nm) in MOS structures even variations of oxide thickness in the range of 0.1 nm will have a strong impact on the performance of ULSI circuits. Therefore, C-AFM is an important technique for the analysis and evaluation of present and future gate and tunneling oxides.

This work was partially supported by the German Bundesministerium für Forschung und Technik. The authors thank Dr. J. Vancea and Prof. Dr. H. Hoffmann of the University of Regensburg, Germany for fruitful discussions.

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