Applied Physics Letters ARTICLE scitation.org/journal/apl

Investigation of carrier compensation traps in n⁻-GaN drift layer by high-temperature deep-level transient spectroscopy

Cite as: Appl. Phys. Lett. **117**, 112103 (2020); doi: 10.1063/5.0019576
Submitted: 23 June 2020 · Accepted: 2 September 2020 ·
Published Online: 18 September 2020

Huayang Huang,[1] Xuelin Yang,[1,2,a)] Shan Wu,[1] Jianfei Shen,[1] Xiaoguang He,[1] Lai Wei,[1] Danshuo Liu,[1] Fujun Xu,[1] Ning Tang,[1,2] Xinqiang Wang,[1,2,3] Weikun Ge,[1] and Bo Shen[1,2,3,a)]

AFFILIATIONS

[1]State Key Laboratory of Artificial Microstructure and Mesoscopic Physics, School of Physics, Peking University, Beijing 100871, China
[2]Nano-optoelectronics Frontier Center of Ministry of Education, Peking University, Beijing 100871, China
[3]Collaborative Innovation Center of Quantum Matter, Beijing 100871, China

[a)]**Authors to whom correspondence should be addressed:** xlyang@pku.edu.cn and bshen@pku.edu.cn

ABSTRACT

Carrier compensation traps in n⁻-GaN drift layers grown on Si substrates were investigated using high-temperature deep-level transient spectroscopy (DLTS). The upper limit of the temperature range (700 K) allows for the study of deeper levels in the bandgap than those previously reported by conventional DLTS. Three trap states were revealed to be responsible for carrier compensation. Besides the residual carbon (C) acceptor, two deep electron traps detected in the DLTS high-temperature range, labeled E2 and E3 with energies E_C of 0.98 and 1.38 eV, respectively, were also found to have contributions to the carrier compensation. A comprehensive investigation combining with positron annihilation spectroscopy measurements revealed that E2 and E3 are related to the (–/2–) and (0/–) acceptor levels of the V_{Ga}–O_N complex, respectively. The relatively high concentrations of E2 and E3 imply that the V_{Ga}–O_N complex is an essential carrier compensation source in the drift layer and plays a crucial role in developing kV-class vertical GaN power devices.

GaN-based devices can operate at higher voltages, higher temperatures, and higher switching frequencies with higher efficiency than existing Si devices.[1–3] In recent years, vertical GaN devices on GaN substrates or Si substrates, which are promising candidates for next-generation power-switching devices, have been attracting much attention.[4–8] In vertical devices, a lightly doped thick drift layer can lower the electric field within it, thereby enabling high breakdown voltages. As a core component of vertical power devices, the drift region is not only the reverse-voltage-blocking layer but also a forward-conduction layer, which requires a stringent co-optimization for its carrier concentration, carrier mobility, and thickness. The carrier concentration and mobility in the drift layer must be precisely controlled to achieve vertical GaN devices with high breakdown voltage and low on-resistance (R_{on}). Theoretically, the net carrier concentration ($N_D - N_A$) must be controlled at around or less than $10^{16}\,cm^{-3}$ for breakdown voltages over 1 kV.[9] However, the precise control of the carrier concentration at around $10^{16}\,cm^{-3}$ is difficult because it requires not only fine doping control of donors but also the suppression of carrier compensation by deep acceptors.[10] Thus, quantitatively characterizing the carrier compensation sources and identifying their origins are essential for achieving reproducible low-concentration doping and high-performance devices.

In an unintentionally doped GaN layer or n-type GaN layer, C impurities have been regarded as the primary source of carrier compensation.[11] As previously reported,[12,13] a C-related defect H1 associated with the deep level $E_V + (0.86–0.9)$ eV might be the major source of carrier compensation. However, besides C, there may exist other sources that need to be clarified. Specifically, when the C composition is reduced to be as low as $10^{15}\,cm^{-3}$, the effect of other carrier compensation sources must be taken into account. For instance, Sawada *et al.*[14] reported that there possibly exists a hidden deep acceptor that might be associated with a trap level near the midgap in the relatively high Si doping range ($[Si] > 1 \times 10^{16}\,cm^{-3}$). However, the origins of the hidden deep acceptor are not identified and are still unclear. One of the challenges is attributed to its deep level behavior, which is beyond the temperature limit (~400 K) of the conventional deep-level transient spectroscopy (DLTS) system. Thus, it is necessary to extend the upper limit of the DLTS temperature range to identify the much

deeper trap. In this work, by using high temperature (up to 700 K) DLTS measurement (FT 1030 HERA-DLTS), the sources of carrier compensation in the metal-organic chemical vapor deposition (MOCVD)-grown n-GaN drift layer are investigated. Besides C acceptors, two deep electron traps detected in the DLTS high-temperature range, labeled E2 and E3 with energies E_C of 0.98 and 1.38 eV, respectively, were also found to have contributions to the carrier compensation.

The investigated GaN layers were grown on top of AlN/AlGaN transition layers on p-type Si (111) substrates by metal-organic chemical vapor deposition (MOCVD). More details about the growth conditions can be found elsewhere.[15] We employed a quasi-vertical $p^+/n^-/n^+$ diode structure, as shown in Fig. 1. The p^+ and n^+ ohmic contacts ensure a low series resistance that mitigates the capacitance-frequency dispersion.[16] In the DLTS-sensitive n^- GaN drift layer, C was unintentionally incorporated, and Si was adjusted accordingly to achieve the low electron concentration. The concentrations of C and Si in the n^- layer obtained from secondary ion mass spectroscopy (SIMS) are about 1.09×10^{16} and 3.16×10^{16} cm^{-3}, respectively. The Mg concentration in the p^+ layer is about 1.21×10^{19} cm^{-3}. Hall-effect measurements on a calibrated sample revealed the carrier concentrations of the p^+ layer to be 5×10^{17} cm^{-3}. Ohmic contacts were deposited by e-beam evaporation. The metal stacks of Ti/Al/Ni/Au (30/180/50/60 nm) and Ni/Au (10/50 nm) were used for the n^+ and p^+ ohmic contact.

Capacitance–voltage (C–V) measurements were first carried out to estimate the $N_D - N_A$ value. As shown in Fig. 2, the $N_D - N_A$ value can be derived from the slope of the $1/C^2$–V curve, which is 1.85×10^{16} cm^{-3}. N_D is presumably equal to [Si] when [Si] is more than 2×10^{16} cm^{-3},[14] since the formation energy is quite high and the concentration is possibly negligible for other possible donors like C_{Ga} and V_N in such n-type GaN. In our sample, [Si] is 3.16×10^{16} cm^{-3}, and so we can reasonably assume N_D to be equal to [Si]. The N_A value can then be estimated to be 1.31×10^{16} cm^{-3}.

To identify the traps contributing to N_A, which are possibly deep traps near the midgap, we carried out high-temperature (HT)-DLTS

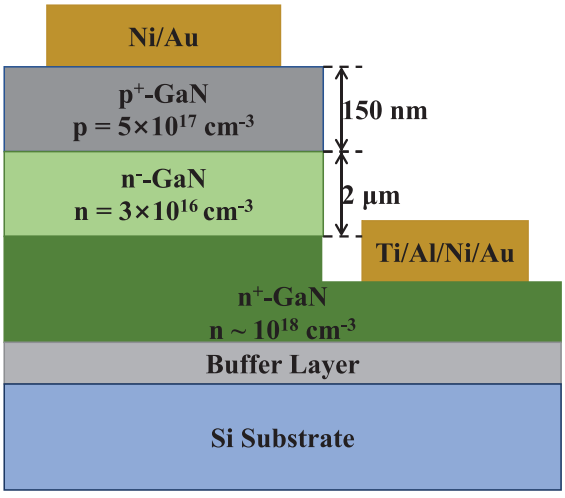

FIG. 1. The cross section of the $p^+/n^-/n^+$ diode structure.

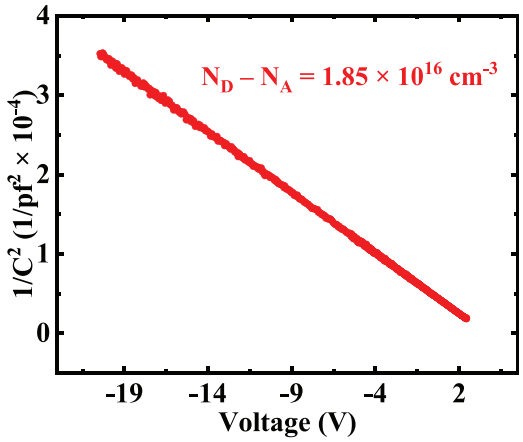

FIG. 2. $1/C^2$–V curves of the measured sample. $N_D - N_A$ derived from the slope of the curve is 1.85×10^{16} cm^{-3}.

measurements on the sample. HT-DLTS measurements in the temperature range of 300–700 K make the detection of deeper levels in the midgap possible. The DLTS signal processing method is deep level transient Fourier spectroscopy (DLTFS). The DLTS measurements were carried out with different filling pulse voltages (U_P) to detect different type traps. The condition at $U_P = 0$ V is used to detect only the electron traps, while $U_P = 4$ V is used to detect both electron and hole traps via minority carrier injection. The reverse bias was set to–5 V, and the filling pulse time was 20 μs at both conditions. The period widths (T_W) are 1, 10, and 100 ms.

The DLTS results with $U_P = 0$ and 4 V are shown in Figs. 3(a) and 3(b). Figures 3(a) and 3(b) only show the data with $T_W = 100$ ms and Fourier transform coefficient b1 for clarity, while all data with three different T_W values were included in the Arrhenius plot. In our HT-DLTS signal spectrum, positive peaks correspond to majority carrier traps, and negative peaks correspond to minority carrier traps. As shown in Fig. 3(a), the spectrum exhibits three electron traps at the energies of E_C – 0.85, 0.98, and 1.38 eV, labeled as E1, E2, and E3, respectively, in the temperature range of 300 to 700 K. The peaks of E2 and E3 are close. We fitted the DLTS peaks by the DLTFS signal function[17] to find the real peak temperatures. As shown in Fig. 3(b), a hole trap labeled H1 with the energy of $E_V + 0.86$ eV was detected. The Arrhenius plots of these electron and hole traps are shown in Fig. 4. The energy level, capture cross section σ, trap concentration N_T, and

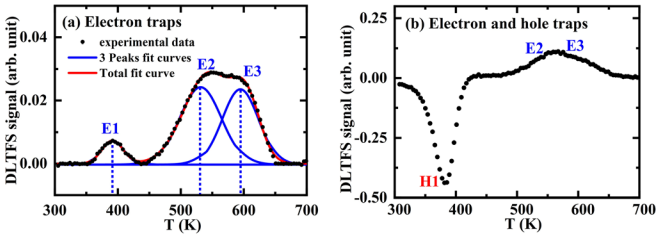

FIG. 3. The HT-DLTFS signal b1 obtained using (a) 0 V and (b) 4 V filling pulses as a function of temperature. The fit curve (blue line) of three peaks and sum of the three peak fit curves (red line) are shown in (a). $T_W = 100$ ms both in (a) and (b).

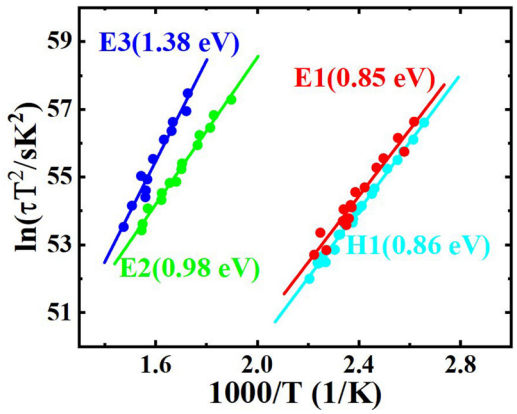

FIG. 4. Arrhenius plots of electron traps and hole traps detected in the HT-DLTS measurement.

corresponding defect of the four traps are summarized in Table I. The H1 trap concentration is determined by a method that considers the depletion layer correction and spatial distribution of the hole occupancy ratio.[18] Hole trap H1 was observed in both n-type and p-type GaN layers.[12,13] Kanegae *et al.* assigned it to the (0/–) transition level of C on a nitrogen site (C_N),[12] while Tokuda reported that V_{Ga}-related defects also have an energy level of $E_V + 0.86$ eV, which is equal to the energy level of the H1 trap.[11] In our sample, we noticed that the H1 trap concentration (1.10×10^{16} cm^{-3}) is close to the concentration of C (1.09×10^{16} cm^{-3}), but more than double the concentration of V_{Ga}-related defects (4.5×10^{15} cm^{-3}), which is derived in the positron annihilation spectroscopy (PAS) measurements. We, thus, attribute H1 to the C_N acceptor. However, the H1 trap concentration is apparently lower than the estimated N_A (1.31×10^{16} cm^{-3}). There should exist other sources besides C_N for the carrier compensation.

Electron trap E1 in GaN is reported to be dependent on substrates and correlated with dislocations.[11] This assignment is supported by the logarithmic filling time dependence of DLTS peak heights.[19,20] Here, the compensation effect of E1 could be negligible since its concentration (6.24×10^{14} cm^{-3}) is almost two orders of magnitude lower than that of the major compensation source H1 (1.10×10^{16} cm^{-3}).

We now focus on the origins of electron traps E2 and E3. We should mention that thanks to the high-temperature scanning capability, the two traps can be observed in DLTS. In fact, we noticed that the sum of the concentrations of E2, E3, and H1 is 1.35×10^{16} cm^{-3}, which is close to the estimated N_A of 1.31×10^{16} cm^{-3}. Thus, E2 and E3 might also be the sources of carrier compensation other than H1. Although the concentration of E2 and E3 is one order of magnitude lower than that of H1, they may change the breakdown voltage with hundreds of volts.[9] Specifically, we believe that the two traps would dominate the compensation when the concentration of C is further reduced. Thus, the identification of the microscopic origins of E2 and E3 is essential not only for defect physics but also for device performance improvement.

We noticed that the trap concentrations of E2 and E3 were quite close, and so there is a high possibility that E2 and E3 originate from the same point defect with different charged states. The most likely native acceptors in n-type GaN are V_{Ga}-related defects, considering that the formation energies of those defects are relatively low when the Fermi level is close to the conduction band minimum.[21–23] Xie *et al.* reported that V_{Ga}–O_N has much lower formation energy than isolated V_{Ga},[21] from first-principles density-functional theory (DFT) calculations. This means that V_{Ga}–O_N has a higher concentration than isolated V_{Ga} in the material. Saarinen *et al.* also reported that the V_{Ga}–O_N complexes are the dominant acceptor native defects in n-type GaN by combining PAS with *ab initio* theory calculations.[22] Van de Walle *et al.* theoretically predicted that V_{Ga}–O_N has two acceptor levels located at approximately 1.8 eV [(0/–) level] and 2.2 eV [(–/2–) level] above the valence band maximum.[23] Since E2 and E3 were peaked at relatively high temperatures, we need to take into account the temperature dependence of the energy gap. According to Jun *et al.*,[24] the energy gap for the epitaxial GaN layer is approximately 3.22 eV in the temperature range of 550–600 K. Thus, as shown in Fig. 5, the thermodynamic transition levels of V_{Ga}–O_N predicted by Van de Walle *et al.*[23] are E_C – 1.42 and 1.02 eV for (0/–) and (–/2–) levels, which are close to the energy levels of E_C – 1.38 and 0.98 eV of E3 and E2 extracted from the HT-DLTS measurement. Furthermore, the energy difference of E3 and E2 is equal to the predicted energy difference of (0/–) and (–/2–) transition levels of V_{Ga}–O_N, which are both 0.4 eV. The above evidence supports the option that E3 and E2 may originate from the same point defect V_{Ga}–O_N complex, while related to different defect charge states. E3 is related to the (0/–) acceptor level, and E2 is related to the (–/2–) acceptor level.

To further investigate the relationship between V_{Ga}-related defects and the E2/E3 trap, we performed Doppler broadening measurements of positron annihilation radiation. The measurements were performed at room temperature using an energy-variable slow positron beam facility at the Institute of High Energy Physics (IHEP), Chinese Academy of Science. The positron beam energy was varied from 0.18 to 28 keV. The spectra were characterized by the S parameter, defined as the fraction of annihilation events over the energy range of 510.2–511.8 keV. More details on the positron annihilation

TABLE I. Summary of trap parameters in the HT-DLTS measurement, where σ and N_T are the hole or electron capture cross section and the trap concentration. The corresponding defects are discussed in the following in this paper.

Trap label	Energy level /eV	σ /cm^2	N_T /cm^{-3}	Defect (transition level)
E1	$E_C - 0.85$	3.92×10^{-14}	6.24×10^{14}	Dislocation-related
E2	$E_C - 0.98$	5.14×10^{-15}	1.26×10^{15}	V_{Ga}–O_N (–/2–)
E3	$E_C - 1.38$	1.74×10^{-14}	1.25×10^{15}	V_{Ga}–O_N (0/–)
H1	$E_V + 0.86$	9.46×10^{-14}	1.10×10^{16}	C_N (0/–)

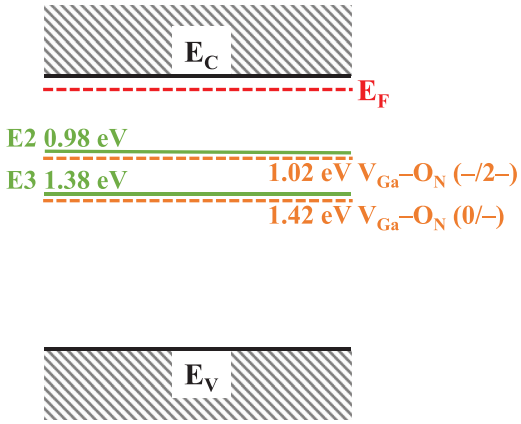

FIG. 5. Levels of V_{Ga}–O_N theoretically predicted in Ref. 21 (brown dashed lines) and E2 and E3 observed in this work (green lines).

techniques can be found in Ref. 25. Figure 6 shows the relative S parameters of the GaN sample as a function of the positron implantation energy and the corresponding positron implantation depth. The relative S parameter is defined as the ratio of measured S parameters to the characteristic value of the reference sample [HVPE (Hydride Vapor Phase Epitaxy) GaN]. One can find that the S parameters decrease rapidly with the energy increase at low energies (positron energy < 2.5 keV), which corresponds to the diffusion of positrons toward the surface.[26] Thus, the data recorded at high energy regions (positron energy > 5 keV) can be taken as the characteristic of the bulk.

The concentration of V_{Ga}-related defects can be estimated from the S parameter data using the positron trapping model. Their concentration can be determined by the following formula:[27]

$$[V_{Ga}] = \frac{N_{at}(S - S_B)}{\mu_V \tau_B (S_V - S)}, \quad (1)$$

where $\tau_B = 166$ ps is the positron lifetime in the GaN lattice, $\mu_V = 1.0 \times 10^{15}$ s^{-1} is the positron trapping coefficient in GaN,[28] and

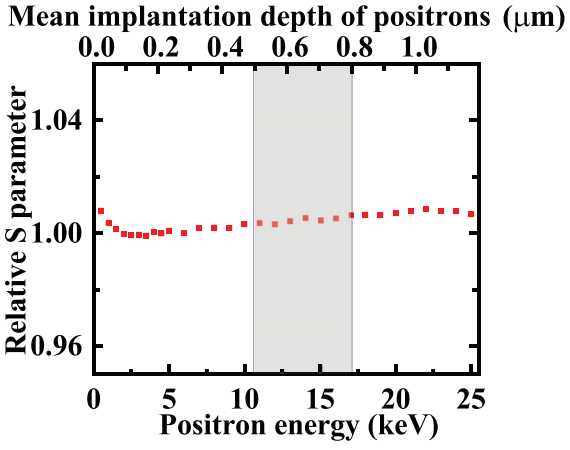

FIG. 6. Relative S parameters as a function of positron energy and implantation depth of positrons. The shaded region is the DLTS-sensitive region.

$N_{at} = 8.9 \times 10^{22}$ cm^{-3} is the atomic density of GaN. For the positions annihilated at the Ga vacancies, we take $S_V/S_B = 1.050$.[22] The DLTS sensitive depth region is 500–800 nm below the pn junction interface. We use the average S parameter in this region in the calculation. The calculated V_{Ga}-related defect concentration from the PAS measurement is 4.5×10^{15} cm^{-3}, which is higher than the E2/E3 trap concentration (1.26×10^{15} cm^{-3}) derived from the DLTS measurement. The reason may be that PAS can detect all the V_{Ga}-related defects, not only the V_{Ga}–O_N complex. There may exist neutrally charged V_{Ga}-related defects such as V_{Ga}–O_N–2H and V_{Ga}–3H detected in the PAS measurement while not detected in the DLTS measurement. In fact, theoretical calculations predicted that the V_{Ga}–O_N–2H complex may have quite low formation energy and a large concentration in GaN.[29]

Finally, we would like to comment on the formation of these point defects from the viewpoint of growth. The concentration of V_{Ga}-related defects may be high in the GaN drift layer since the growth conditions with high V/III ratios are usually used during the growth to reduce the C concentration.[15] This suggests that the contribution of compensation from C falls, while that from E2 and E3 will rise. Further investigation is required to confirm this dilemma between C and V_{Ga}-related defects.

Although the GaN samples in this work are grown on Si substrates, the conclusion may also be instructive to GaN grown on bulk GaN substrates. For GaN grown on Si substrates, the typical dislocation density is about 10^8–10^9 cm^{-2}, which is still much higher than that in the homoepitaxial GaN layer. According to the deep carbon depletion (DCD) model developed by Knetzger *et al.*,[30] the C concentration may be affected by the dislocation density due to the carbon-gathering effect. Thus, the unintentionally doped C concentration may be lower in the homoepitaxial GaN layer due to the lower dislocation density. In fact, the C concentration can be indeed reduced to 7.3×10^{14} cm^{-3} in the homoepitaxial GaN layer very recently.[31] In that case, other acceptors, such as the V_{Ga}-O_N complex, should be paid much attention when analyzing the compensation traps.

In conclusion, we investigated carrier compensation traps in MOCVD-grown n$^-$-GaN drift layers using HT-DLTS. The upper limit of the temperature range (700 K) allows for the study of deeper levels in the bandgap than that previously reported by conventional DLTS. Three trap states were revealed to be responsible for carrier compensation. Residual C is the major source of carrier compensation, while two deep electron traps detected in the DLTS high-temperature range, labeled E2 and E3 with energies E_C of 0.98 and 1.38 eV, respectively, were also found to have contributions to the carrier compensation. A comprehensive investigation combining with Doppler broadening of PAS revealed that E2 and E3 are related to the (–/2–) and (0/–) acceptor levels of the V_{Ga}–O_N complex, respectively. The relatively high concentrations of E2 and E3 imply that the V_{Ga}–O_N complex is an essential carrier compensation source in the drift layer and plays a crucial role in developing kV-class vertical GaN power devices. Further discussions show the possible dilemma between C and the V_{Ga}–O_N complex in crystal growth.

This work was supported by the National Key Research and Development Program of China (Nos. 2017YFB0402900 and 2018YFE0125700), the National Natural Science Foundation of China (Nos. 61922001, 11634002, 61521004, 61927806, and U1601210), and the Key Research and Development Program

of Guangdong Province (Nos. 2019B010128002 and 2020B010171002).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]Z. Q. Fang, B. Claflin, D. C. Look, D. S. Green, and R. Vetury, J. Appl. Phys. **108**, 063706 (2010).
[2]C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. K. Mishra, and J. S. Speck, J. Vac. Sci. Technol. B **22**, 1145 (2004).
[3]P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, Appl. Phys. Lett. **79**, 3527 (2001).
[4]Y. H. Zhang, A. Dadgar, and T. Palacios, J. Phys. D: Appl. Phys. **51**, 273001 (2018).
[5]R. A. Khadar, C. Liu, L. Y. Zhang, P. Xiang, K. Cheng, and E. Matioli, IEEE Electron Device Lett. **39**, 401 (2018).
[6]X. B. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, IEEE Electron Device Lett. **37**, 636 (2016).
[7]S. Mase, Y. Urayama, T. Hamada, J. J. Freedsman, and T. Egawa, Appl. Phys. Express **9**, 111005 (2016).
[8]I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, IEEE Trans. Electron Devices **60**, 3067 (2013).
[9]T. Kachi, Jpn. J. Appl. Phys., Part 1 **53**, 100210 (2014).
[10]T. Narita, K. Tomita, K. Kataoka, Y. Tokuda, T. Kogiso, H. Yoshida, N. Ikarashi, K. Iwata, M. Nagao, N. Sawada, M. Horita, J. Suda, and T. Kachi, Jpn. J. Appl. Phys., Part 1 **59**, SA0804 (2020).
[11]Y. Tokuda, ECS Trans. **75**, 39 (2016).
[12]K. Kanegae, H. Fujikura, Y. Otoki, T. Konno, T. Yoshida, M. Horita, T. Kimoto, and J. Suda, Appl. Phys. Lett. **115**, 012103 (2019).
[13]T. Narita, K. Tomita, Y. Tokuda, T. Kogiso, M. Horita, and T. Kachi, J. Appl. Phys. **124**, 215701 (2018).
[14]N. Sawada, T. Narita, M. Kanechika, T. Uesugi, T. Kachi, M. Horita, T. Kimoto, and J. Suda, Appl. Phys. Express **11**, 041001 (2018).
[15]J. P. Cheng, X. L. Yang, L. Sang, L. Guo, A. Q. Hu, F. J. Xu, N. Tang, X. Q. Wang, and B. Shen, Appl. Phys. Lett. **106**, 142106 (2015).
[16]D. Pons, J. Appl. Phys. **55**, 3644 (1984).
[17]S. Weiss and R. Kassing, Solid-State Electron. **31**, 1733 (1988).
[18]K. Kanegae, M. Horita, T. Kimoto, and J. Suda, Appl. Phys. Express **11**, 071002 (2018).
[19]P. Omling, E. R. Weber, L. Montelius, H. Alexander, and J. Michel, Phys. Rev. B **32**, 6571 (1985).
[20]T. Wosinski, J. Appl. Phys. **65**, 1566 (1989).
[21]Z. J. Xie, Y. Sui, J. Buckeridge, A. A. Sokol, T. W. Keal, and A. Walsh, Appl. Phys. Lett. **112**, 262104 (2018).
[22]S. Hautakangas, I. Makkonen, V. Ranki, J. Puska, K. Saarinen, X. Xu, and D. C. Look, Phys. Rev. B **73**, 193301 (2006).
[23]J. L. Lyons, A. Alkauskas, A. Janotti, and C. G. Van de Walle, Phys. Status Solidi B **252**, 900 (2015).
[24]H. Teisseyre, P. Perlin, T. Suski, I. Grzegory, S. Porowski, J. Jun, A. Pietraszko, and T. D. Moustakas, J. Appl. Phys. **76**, 2429 (1994).
[25]X. L. Yang, W. X. Zhu, C. D. Wang, H. Fang, T. J. Yu, Z. J. Yang, G. Y. Zhang, X. B. Qin, R. S. Yu, and B. Y. Wang, Appl. Phys. Lett. **94**, 151907 (2009).
[26]A. Uedono, T. Fujishima, Y. Cao, Y. Zhang, N. Yoshihara, S. Ishibashi, M. Sumiya, O. Laboutin, W. Johnson, and T. Palacios, Appl. Phys. Lett. **104**, 082110 (2014).
[27]F. Tuomisto, J. Phys.: Conf. Ser. **265**, 012003 (2011).
[28]F. Tuomisto and I. Makkonen, Rev. Mod. Phys. **85**, 1583 (2013).
[29]J. L. Lyons and C. G. Van de Walle, npj Comput. Mater. **3**, 12 (2017).
[30]M. Knetzger, E. Meissner, J. Derluyn, M. Germain, and J. Friedrich, Microelectron. Reliab. **66**, 16 (2016).
[31]T. Ciarkowski, N. Allen, E. Carlson, R. McCarthy, C. Youtsey, J. S. Wang, P. Fay, J. Q. Xie, and L. Guido, Materials **12**, 2455 (2019).