Dry etch damage in n-type crystalline silicon wafers assessed by deep-level transient spectroscopy and minority carrier lifetime

Eddy Simoen,[a] Hariharsudan Sivaramakrishnan Radhakrishnan, Md. Gius Uddin, Ivan Gordon, and Jef Poortmans[b),c)]
Imec, Kapeldreef 75, B-3001 Leuven, Belgium

Chong Wang and Wei Li
School of Optoelectronic Information, University of Electronic Science and Technology of China, 610054 Chengdu, Sichuan, People's Republic China

(Received 21 February 2018; accepted 29 May 2018; published 13 June 2018)

This paper compares the electrically active damage in dry-etched n-type float-zone silicon, using NF_3/Ar or H_2-plasma exposure and assessed by deep-level transient spectroscopy (DLTS) and recombination lifetime analysis. It is shown that the NF_3/Ar-plasma damage consists of at least four different types of electron traps in the upper half of the band gap, which can be associated with vacancy- and vacancy-impurity-related complexes. In the case of H_2-plasma damage, it is believed that the accumulation of point defects results in a gradual disordering of the near-surface layer. These defect levels also act as recombination centers, judged by the fact that they degrade the minority carrier lifetime. It is finally shown that lifetime measurements are more sensitive to the etching-induced damage than DLTS. *Published by the AVS*. https://doi.org/10.1116/1.5026529

I. INTRODUCTION

Plasma-based dry etching, which is nowadays a standard technique in microelectronics processing, is also finding more and more its way into the fabrication of silicon solar cells. It has been applied to remove native oxide layers[1] from the surface before the deposition of a passivation layer, for texturing the silicon surface to produce nanoscale surface textures such as inverted nanopyramids[2] as well as black silicon,[3,4] or for the patterning of thin films such as hydrogenated amorphous silicon (a-Si:H) films in the heterojunction interdigitated back-contact solar cell technology.[5] In addition, plasma-assisted deposition processes are routinely used in photovoltaics (PV), for the fabrication of SiN_x passivation and antireflective coating layers[6] or for the low-temperature chemical vapor deposition of silicon epitaxial layers[7] and a-Si:H thin films. During plasma-assisted processes, the substrate is subjected to the bombardment by energetic ions, which displace lattice atoms upon impact, thus creating crystalline damage and contamination by elements coming from the reaction chamber.[2,6–10] The amount of damage depends on various parameters, such as the reactive ions, the gas pressure, the applied power, the wafer temperature, etc. These defects usually give rise to energy levels in the band gap, so that according to the Shockley-Read-Hall (SRH) theory, they can determine the recombination lifetime of the material[2,6,7] and, hence, the dark current of devices[11,12] and circuits,[13,14] as well as the open-circuit voltage and power conversion efficiency of solar cells.

Numerous studies have been performed in the past in order to identify the nature of the dry-etch-induced damage in silicon, relying on structural, chemical, and electrical analyses.[2,6–14] Among the electrical characterization techniques, deep-level transient spectroscopy (DLTS) is well recognized as one of the most powerful, given its high sensitivity and defect profiling capabilities.[15,16] It has been applied to study plasma damage in Ar-ion-[17–19] and RF-hydrogen plasma-exposed n-type silicon.[20–22] In most cases, several kinds of electron traps in the upper half of the silicon band gap have been revealed, using a Schottky barrier (SB) on n-type silicon. Most of them have been identified as being vacancy-related: the A center (V-O), the divacancy (V_2), etc., and thus consist of complexes between intrinsic point defects and impurities, which may be present in the starting material (oxygen, carbon, etc.) or introduced during the etching step (fluorine, argon, nitrogen, and hydrogen). By deep-level profiling, it has been shown that the observed traps occur much deeper than the expected end-of-range of the energetic ions, which is typically a few nanometers,[18–20] demonstrating significant diffusion of the created native point defects and impurities.

It is the aim of this work to report on a detailed study of the electron traps observed by DLTS on Al SBs fabricated on n-type float-zone (FZ) silicon wafers, which have been subjected to either NF_3/Ar- or H_2-plasma etching. It is shown that the main factor determining the near surface traps is the type of plasma, i.e., NF_3/Ar versus H_2. While in the first case, at least four prominent electron traps have been detected, increasing in concentration with the plasma power, the hydrogen-plasma etching reveals a different dominant level, developing in a continuum of states for higher plasma power. The observed traps in the near surface region also impact on the recombination lifetime, as will be shown by photoluminescence (PL) and quasi-steady-state photoconductance (QSSPC) measurements. Finally, the process

[a)]Also at Department of Solid State Sciences, Ghent University, Krijgslaan 281 S1, B-9000 Gent, Belgium; electronic mail: eddy.simoen@imec.be
[b)]Also at Department of Electrical Engineering, KU Leuven, Kasteelpark Arenberg 10, B-3001 Heverlee, Belgium.
[c)]Also at Universiteit Hasselt, Campus Diepenbeek, Agoralaan-gebouw D, B-3590 Diepenbeek, Belgium.

conditions will be identified, corresponding to deep-level concentrations below the detection limit of DLTS and suitable for PV processing.

II. EXPERIMENTAL DETAILS

N-type FZ silicon wafers, with 150 mm diameter and resistivity of 3 Ωcm, have been subjected to different dry etching steps. During plasma etching, the substrate temperature was 175 °C. In the case of the NF_3/Ar plasma exposure, the selected conditions were (200/100 sccm, 5 min, 250 W); (200/100 sccm, 5 min, 800 W); and (10/100 sccm, 5 min, 250 W) (samples A–C). The hydrogen-plasma process conditions were: (3 min, 50 W); (3 min, 600 W); and (40 s, 50 W) (samples D–F). A wafer without dry etching has been included as a reference (G); the native oxide was removed by diluted hydrogen fluoride (HF). Two different references (G1 and G2 quarter wafers) have been used for the lifetime (τ) measurements, resulting in slightly different τ values. Circular aluminum SBs with different diameter (1, 2, 3 mm) and thickness of 150 nm have been prepared by thermal evaporation through a shadow mask. Before metal deposition, the native oxide was removed by a short HF dip.

The SBs have been mounted in a liquid nitrogen flow cryostat for DLTS analyses. Before cooling the sample, the current–voltage and capacitance–voltage (C-V) measurements have been carried out at room temperature, the latter at a fixed frequency f of 1 MHz. SBs with good C-V characteristics have been selected for DLTS, as can be judged from Figs. 1(a) and 2(a). The fact that the capacitance drops immediately when biasing in forward operation indicates that negligible oxide is left after the HF etch. Likewise, SBs were selected with as low as possible reverse current for DLTS, in order not to compromise the measurements. It was noted that the leakage current for the H_2-etched samples was usually larger than for NF_3/Ar, with sample D showing excessive reverse current, as will be shown below. The doping density N_{dop} of the n-type substrate has been derived from a $1/C^2$ versus reverse bias V_R plot, yielding, except for condition F, reasonably uniform concentration profiles [Figs. 1(b) and 2(b)] versus the depletion depth. The latter parameter is calculated from

$$W(V_R) = A\varepsilon_{Si}\varepsilon_0/C(V_R), \quad (1)$$

with ε_{Si} and ε_0 the dielectric constant of silicon and the permittivity of vacuum, respectively. A is the area of the SB.

DLTS has been performed by varying the temperature T from 75 K to room temperature using a fast-Fourier transform (FFT) DLTS system. Different bias pulses from V_R to V_P (pulse bias) have been applied in parallel, probing different parts of the near surface depletion region. As can be seen from Fig. 1(b) or 2(b), the depth range is typically between 1 and 4 μm, when changing the reverse bias from 0 to −4 V. In order to fill the near-surface electron traps adjacent to the SB, one has to apply a V_P in forward bias. In principle, a V_P to flat-band voltage (∼+0.7 V) enables to fill traps at or close to the SB/Si interface, where the highest dry-etch damage is expected. In some cases, measurements have been performed

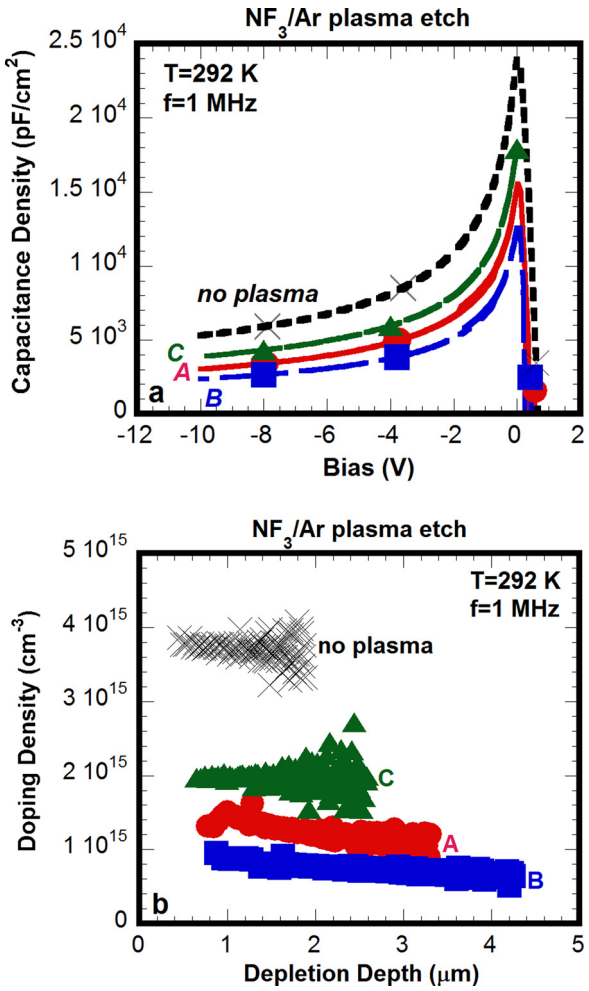

FIG. 1. (Color online) (a) Capacitance divided by the Schottky barrier area A vs bias for the NF_3/Ar-plasma etched samples. (b) Corresponding doping density profiles vs depletion region width.

for different pulse times t_p in order to study the electron capture kinetics. The bias pulse was applied with a sampling period t_w which was typically 51.2 ms.

Lifetime measurements have been executed on another part of the same wafer as for DLTS. Any dry etch residual contamination on the surface of the samples was cleaned using a short HF dip of 2 min, which produces a H-terminated surface, suitable for high quality passivation. A stack of intrinsic and doped hydrogenated amorphous silicon [a-Si:H (i/n^+)] was deposited using plasma-enhanced chemical vapor deposition at 175 °C on both surfaces of the wafer, which results in very high quality surface passivation with a surface recombination velocity typically <2 cm/s. In order to determine the minority carrier lifetime in the samples, steady-state PL and QSSPC measurements were then performed on these passivated samples using a commercially available PL imaging tool (LIS-R1) from BT Imaging. For PL measurements, the wafer is irradiated with 808 nm laser light. The absorbed light is converted into electron-hole pairs which recombine via various pathways. The photons emitted by radiative recombination are detected by a charge-coupled-device camera placed above the sample to produce a PL image. The higher the PL intensity, the higher the minority carrier lifetime in the sample. For

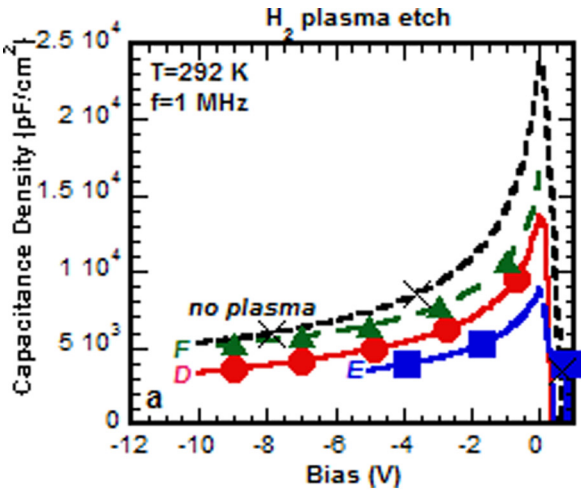

FIG. 2. (Color online) (a) Capacitance divided by the Schottky barrier area A vs bias for the H_2-plasma etched samples. (b) Corresponding doping density profiles vs depletion region width.

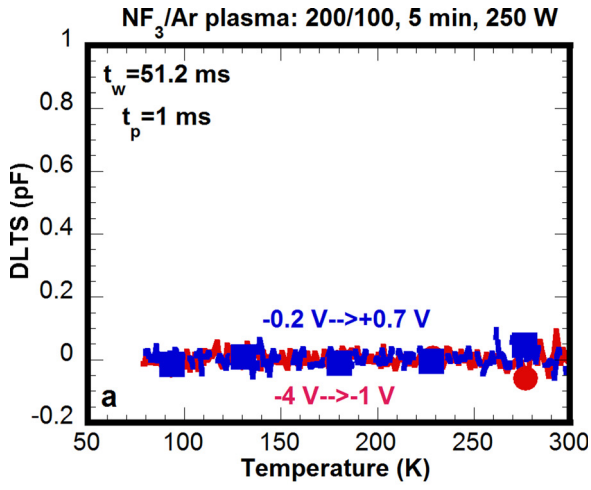

FIG. 3. (Color online) (a) DLT-spectra for two bias pulses for an NF_3/Ar-plasma etched sample (A: 200/100 sccm/sccm; 5 min, 250 W). (b) DLT-spectra for two bias pulses for an NF_3/Ar-plasma etched sample (C: 10/100 sccm/sccm; 5 min, 250 W).

QSSPC measurements, a coil placed directly underneath the sample measures changes in its conductivity as the laser intensity is varied. The changes in the conductivity and hence the minority carrier density in the sample are used to determine the minority carrier recombination lifetime versus the injection level, defined by the excess carrier density Δn.

III. RESULTS

First, the deep-level transient (DLT)-spectra of the NF_3/Ar-etched samples will be described, followed by the H_2-plasma samples. Finally, the impact of the dry etch conditions on the recombination lifetime is investigated and compared.

A. Dry etch damage by NF_3/Ar

According to Fig. 3(a), no detectable electron traps are found in the range from 1 to 4 μm (bias pulse from -4 to -1 V) in sample A. The same applies for a pulse from -0.2 V to $+0.7$ V, probing the region adjacent to the SB. This means that dry etching with an etching time of 5 min and a power of 250 W yields negligible surface damage according to DLTS. In fact, similar flat spectra have been obtained for the reference sample G, not subjected to dry etching. It also implies that the deposition of the SB by thermal evaporation does not introduce a detectable amount of electron traps in the n-type silicon wafers. It has been well established that the deposition of a metal SB on silicon can introduce deep levels in the underlying substrate,[23,24] which is obviously not the case here.

Increasing the dilution of NF_3 in Ar by modifying the NF_3/Ar flow ratio from 200/100 to 10/100 sccm results in the observation of two small peaks, just above the detection limit of DLTS in Fig. 3(b), for a bias pulse close to the surface. Electron traps E1 ($\sim$80 K) and E2 ($\sim$120 K) are present close to the Al SB, with E1 most likely corresponding with the V-O center. However, other SBs on the same wafer yield no detectable deep levels, showing the nonuniformity of the electrically active damage across the exposed surface. The sample-to-sample variation of the DLT-spectra across a wafer has been noted before for CHF_3/Ar-plasma etching of n-type Czochralski silicon[18] and will be further illustrated by the PL lifetime maps reported below.

Sample B, where the plasma power is increased to 800 W, exhibits the clearest DLT-spectrum [Fig. 4(a)] with at least four pronounced electrons traps, labeled E1 to E4, and some

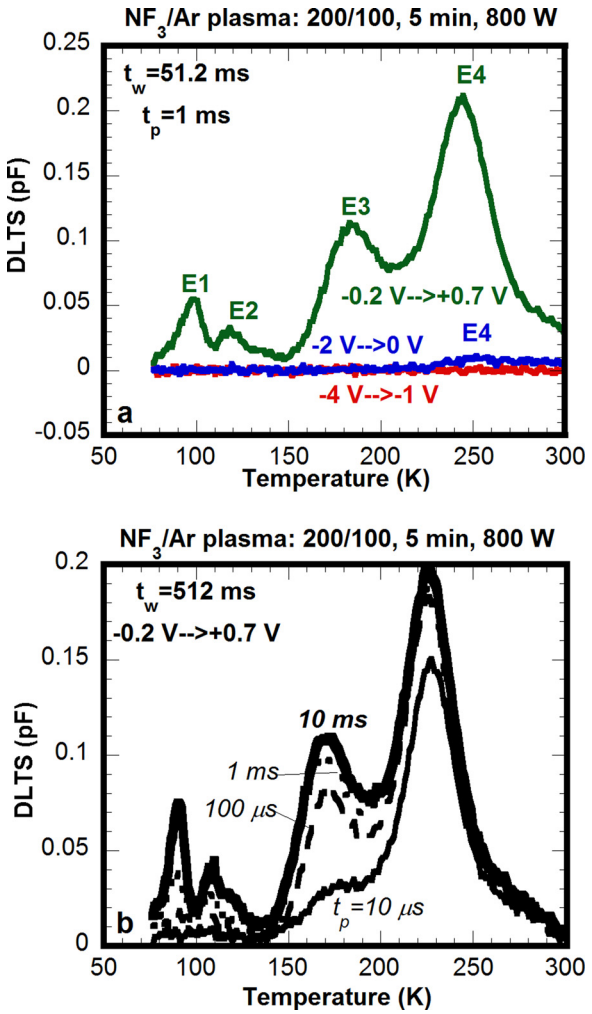

FIG. 4. (Color online) (a) DLT-spectra for two bias pulses for an NF_3/Ar-plasma etched sample (B: 200/100 sccm/sccm; 5 min; 800 W). (b) DLT-spectra for sample B, corresponding with different pulse durations in the range of 10 μs–10 ms, for a bias from -0.2 V $\rightarrow$ $+0.7$ V.

additional shoulders to the right of peak E2 and E4. In the past, up to ten different traps have been found in Ar-plasma exposed n-type silicon,[18–20] although not all of them could be assigned to the etching.[18] Since the not etched reference is defect-free, we believe that the deep levels reported in Fig. 4(a) are introduced by the dry etch process. The corresponding Arrhenius plot is represented in Fig. 5, while the trap signatures are given in Table I. The activation energy (E_T) is derived from the slope of a least-square linear fit to the data points in Fig. 5, while the intercept provides a value for the prefactor K_T.

In Fig. 4(b), the electron capture kinetics is investigated, showing the spectra for different pulse times, in the range between 10 μs and 10 ms. Obviously, the deeper levels E3 and E4 show a saturation of the peak amplitude for longer pulses, which is not so evident for the shallower ones E1 and E2. This could point in the first instance to a smaller electron capture cross section for E1 and E2, compared with E3 and E4. A roughly one decade smaller σ_n can also be derived from the K_T values in Table I, considering the inverse relationship between both parameters.

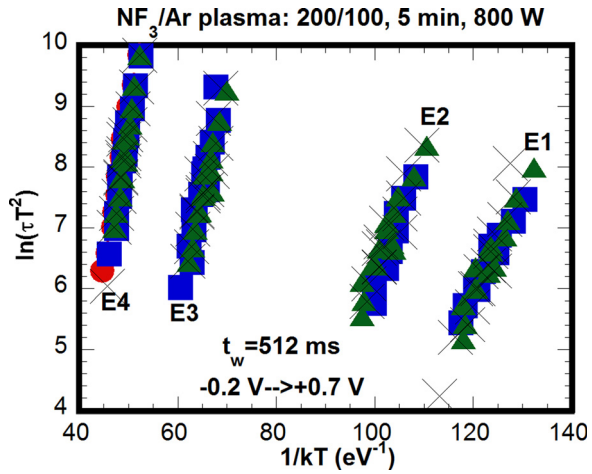

FIG. 5. (Color online) Arrhenius plot corresponding with Fig. 4(b) for an NF_3/Ar-etched n-type silicon sample (B: 200/100 sccm/sccm; 5 min and 800 W). The symbols correspond with the different t_p values.

B. Dry etch damage by H_2 plasma

Already a short 40 s H_2-plasma etch at 50 W generates measurable damage in the n-type FZ substrates, close to the surface. An electron trap E5 is observed in Fig. 6(a), which is different compared to the levels found in the NF_3/Ar-etched samples of Fig. 4. The peak widens for a longer etching time [Fig. 6(b)], as a shoulder of shallower levels develops in the spectra to the lower-temperature side. This feature increases significantly with electron capture time (pulse duration), somehow similar to the behavior of extended defects[16,25–27] or electron traps in amorphous silicon (a-silicon).[28] The presence of a heavily disordered, a-silicon-like region near the surface has been suggested before, in the case of a few hundreds to 1 keV Ar-implantation in n-type silicon.[20] This resulted in the presence of broad DLTS peaks above 200 K, associated with the presence of a distribution of electron traps in the near-surface silicon layer. Further proof of the heavily damaged nature of the near-surface layer is the observation that the reverse current of these particular SBs (sample D) is very high. This gives rise to an unreliable, negative DLT-signal, as indicated in Fig. 6(b). Similar observations have been reported in the past for heavily damaged dry-etched SBs,[19] rendering the study of the underlying deep-levels quite challenging if not inaccurate. Fortunately, the leakage current is thermally activated and its negative impact on the spectra disappears upon cooling the sample, as indicated in Fig. 6(b). The corresponding Arrhenius plot of peak E5 is shown in Fig. 7, yielding an activation energy of 0.45 eV. This is close to the value for the P-V pair.[17] On the

TABLE I. Activation energy and prefactor derived from the Arrhenius plot of Fig. 5.

Peak	Activation energy (eV)	K_T (sK^2)
E1	0.182	1.15×10^{-7}
E2	0.202	9.0×10^{-7}
E3	0.365	9.5×10^{-8}
E4	0.523	2.5×10^{-8}

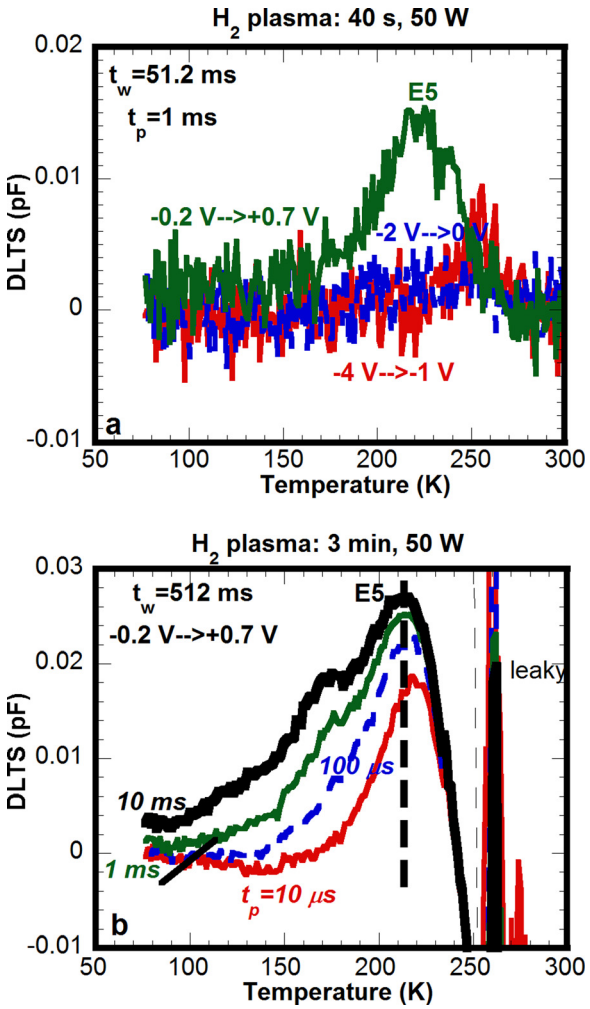

FIG. 6. (Color online) (a) DLT-spectra for three bias pulses for the H_2-plasma-etched sample F (40 s, 50 W). (b) DLT-spectra for a pulse from −0.2 to +0.7 V and different pulse durations for the H_2-plasma etched sample D (3 min, 50 W).

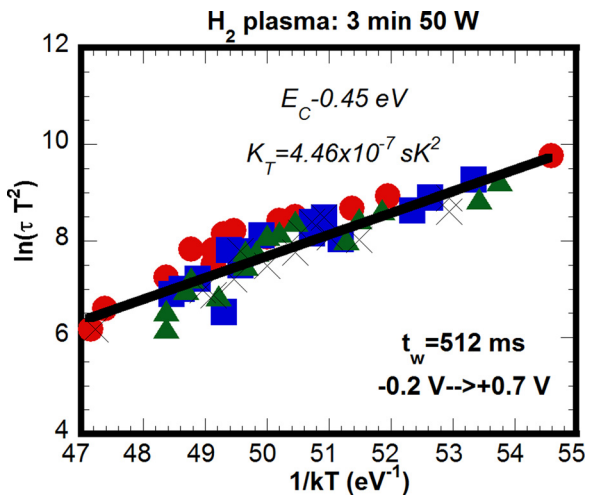

FIG. 7. (Color online) Arrhenius plot corresponding with the spectra of Fig. 6(b) for sample D: $t_p = 10\,\mu$s (red circles); 100 μs (blue squares); 1 ms (green triangles), and 10 ms (X).

other hand, there is little evidence for the levels found in Ref. 22 at E_C–0.17 eV, E_C–0.22 eV and E_C–0.32 eV.

Further increasing the plasma power to 600 W gives rise to a broad spectrum of electron traps in the near-surface layer [Fig. 8(a)], showing a more or less continuous increase in the trap amplitude (signal height) with t_p [Fig. 8(b)]. This again points to a highly disordered, amorphouslike material adjacent to the Schottky barrier. However, the reverse current is not compromising the spectra in this case.

Overall, it can be concluded that the electron traps created by the two kinds of dry etching are different, whereby in the NF_3/Ar case mainly point defects are being created, while the layer becomes more disordered for high power H_2-plasma exposure. This could be related to the different sputtering rates for the two different plasmas: in the first case, the removal rate keeps more or less pace with the creation of displacement damage in the near surface layer[19]—the observed defects, particularly at high power, could be associated with in-diffused native point defects (and possibly ions from the plasma), which become trapped at some distance from the surface, beyond the end-of-range. In the second case, there is insufficient removal of the damaged silicon, so

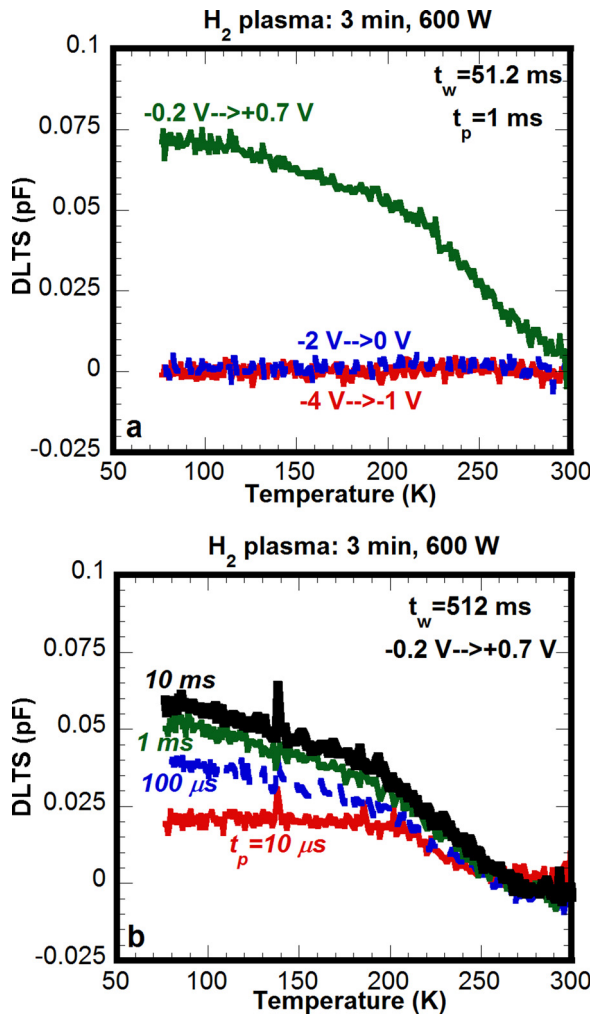

FIG. 8. (Color online) (a) DLT-spectra for three bias pulses for the H_2-plasma-etched sample E (3 min, 600 W). (b) DLT-spectra for a pulse from −0.2 to +0.7 V and different pulse durations for the same sample E.

that the damage accumulates, resulting in an amorphouslike layer for higher etching times and power. This is in line with past observations where it has been shown that D defects can be detected by electron spin resonance in SF_6/O_2 etched n-type silicon,[2] which corresponds with a dangling bond type of defect in a disordered environment.[29,30]

C. Lifetime measurements

The PL lifetime maps in Fig. 9 evidence a reduction in the recombination lifetime τ of the NF_3/Ar-etched wafers, even for the process conditions, yielding no measurable defects in the spectra [e.g., Fig. 3(a)]. For the case with high power etching at 800 W (sample B), this lifetime degradation is particularly noticeable from the low PL signal from this sample. The same conclusion can be drawn from the injection-level dependent QSSPC data of Fig. 10. Similar results have recently been obtained for CF_4/O_2 reactive ion etching of n-type FZ silicon substrates.[31] However, given the uncertainties associated with the minority carrier lifetime measurements, the lifetimes of samples dry-etched at a low power of 250 W, with different flows, could be comparable to that of the reference sample. Such high lifetimes are sufficient to ensure high open-circuit voltages and efficiencies in solar cells. These deductions correlate well with DLTS results where strong deep levels were mainly observed for sample B, compared to samples A and C. It should be emphasized that the observed differences cannot be explained by different surface recombination velocities, as all the samples were cleaned and passivated together after the plasma treatment. The differences in lifetime should thus come from SRH centers in the silicon wafers.

The corresponding PL maps for the H_2-etched samples are represented in Fig. 11, while the injection-level dependent lifetime curves are given in Fig. 12. Here, a marked

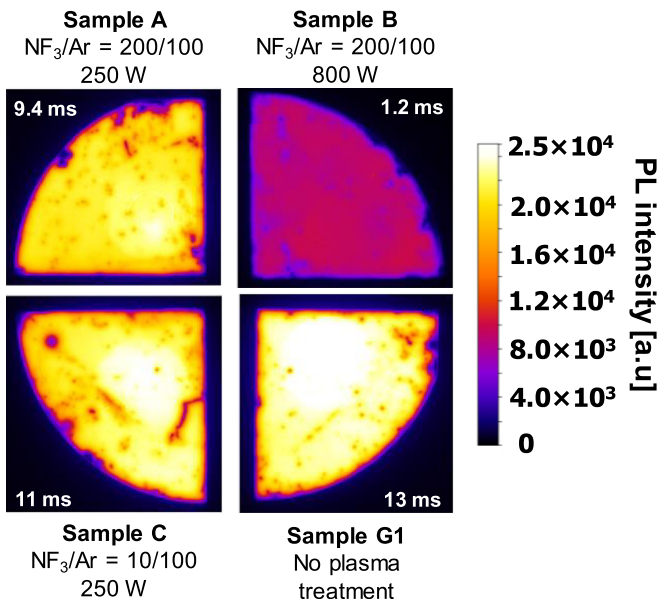

FIG. 9. (Color online) Uncalibrated PL maps of n-type silicon treated with three different NF_3/Ar plasma conditions, compared with reference (without any plasma treatment). The minority carrier lifetime values taken at an injection level of 10^{15} cm^{-3} (from Fig. 10) for each condition is also indicated.

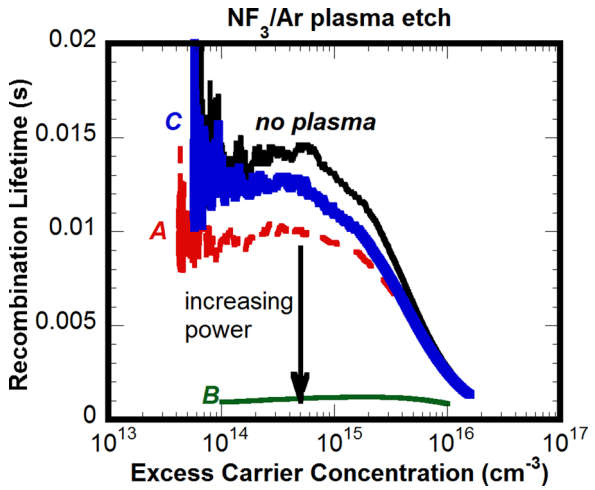

FIG. 10. (Color online) QSSPC recombination lifetime as a function of the injection level Δn for the NF_3/Ar-plasma treated n-type Si wafers, compared with a reference (without any plasma treatment).

degradation of τ is observed, even for the least aggressive H_2-plasma exposure (40 s, 50 W). The degradation is significantly worse at high power (600 W), and the longer the exposure of the silicon substrate to the H_2 plasma, the greater the degradation. At the same time, comparing the injection-level (Δn) dependence in Figs. 10 and 12 clearly shows a different behavior. As the dependence of τ on Δn strongly depends on the specific recombination center,[32–34] it confirms the different nature of the responsible deep levels, caused by the different plasmas in n-type silicon.

IV. DISCUSSION

The first issue which needs to be clarified is the apparent impact of the dry etching on the doping density, suggested

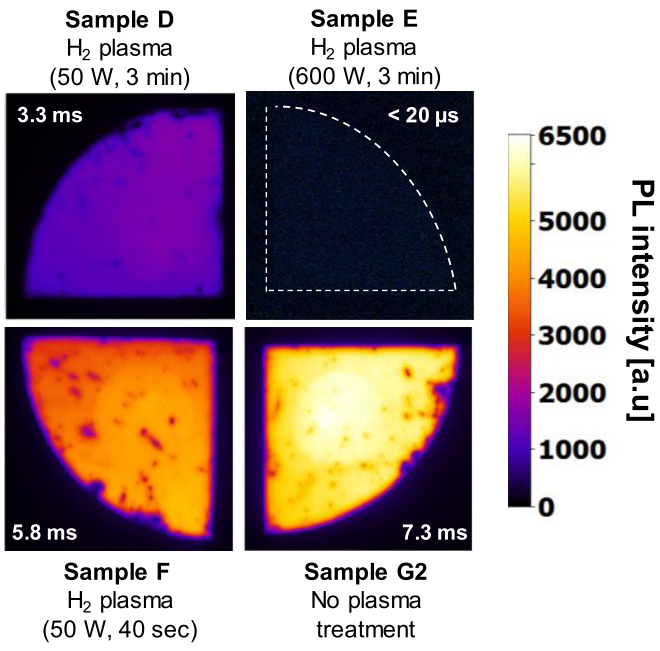

FIG. 11. (Color online) PL maps for the H_2-plasma treated n-type silicon wafers, compared with reference (without any plasma treatment). The minority carrier lifetime values taken at an injection level of 10^{15} cm^{-3} (from Fig. 12) for each condition is also indicated.

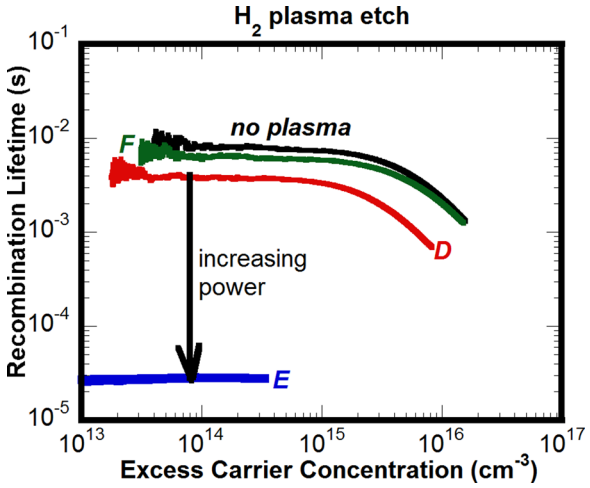

FIG. 12. (Color online) QSSPC recombination lifetime in function of the injection level Δn for the H_2-plasma treated n-type Si wafers, compared with the wet etched reference.

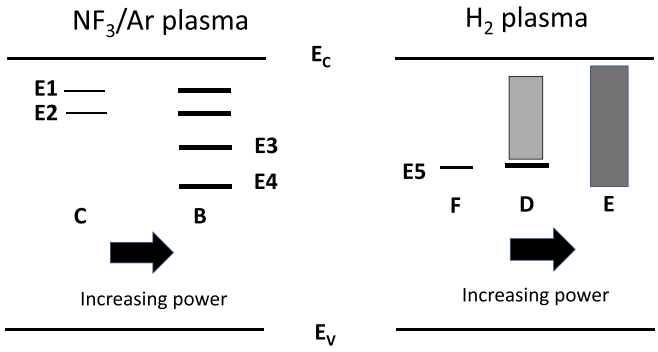

FIG. 13. (Color online) Schematic representation of the main DLTS results for the NF_3/Ar plasma and the H_2 plasma exposed samples. The lines give the approximate position of the deep levels E1–E5 in the band gap of silicon and the thickness of the lines represents the concentration. The boxes for samples D and E represent a continuous distribution of disordered states close to the surface. E_C is the bottom of the conduction band and E_V the top of the valence band.

by Figs. 1(b) and 2(b). It has been shown in the past that Ar-plasma damage of n-type silicon results in an increase in the donor concentration close to the exposed silicon surface by introducing damage-induced shallow donors, which at the same time reduces the Schottky barrier height.[19,20] Deeper in the substrate, a compensation of the n-type doping density has been reported,[19] which can originate from the compensating action of the dry-etch-induced deep electron traps, which have predominantly an acceptor character. This means that they are negatively charged when the Fermi level is close(r) to the conduction band, compensating the positive space charge of the ionized shallow donors. In the case of a H_2-plasma, the introduction of a high density of hydrogen can passivate the shallow dopants by a pairing reaction.[35] The doping profiles in Figs. 1(b) and 2(b) are rather uniform, showing no clear evidence for such compensation. While the etched samples apparently show a lower doping density than the nonetched material, it is believed that this is related to the doping nonuniformity across the wafer, rather than a defect- or impurity-related compensation. Indeed, measuring the C-V characteristics of several SBs on the same sample yields a similar dispersion of the doping density as in Figs. 1(b) and 2(b). Moreover, the trap concentrations in Fig. 4, on the order of 1% cannot be responsible for a pronounced reduction of the doping density at depths of 1 μm and more.

Another question is the nature of the observed electron traps in Fig. 4 for NF_3/Ar plasma and Figs. 6 and 8 (H_2 plasma). The main observations derived from DLTS have been summarized in Fig. 13, showing schematically the evolution of the observed deep levels with plasma conditions. Both from the Arrhenius plots in Figs. 5 and 7 and from the peak maximum positions in the spectra clearly different defects are involved in the two cases. This could point to etch-specific complexes, incorporating either Ar (F) or hydrogen.[18,19,22] The level E1 is one of the most prominent electron traps introduced during ion implantation or irradiation experiments in n-type silicon and corresponds with the V-O center.[17–20] The fact that the peak amplitude is rather small can be explained by considering the low oxygen content in FZ silicon wafers.

A level similar to E2 has been reported before in 1 keV Ar-irradiated and sputter etched n-type silicon, with activation energy of 0.201–0.203 eV.[19] It has been ascribed to a V_2O acceptor level in 1 keV He-bombarded material.[36] More recent studies have identified two acceptor levels for V_2O: the single acceptor (0/-) at E_C–0.43 eV and the double acceptor (-/=) at E_C–0.23 eV.[37,38] The single acceptor should occur in between E3 and E4 in the spectra of Fig. 4.

There are several candidate vacancy-related electron traps for level E3 at E_C–0.365 eV. The second acceptor level of the trivacancy has been placed at E_C–0.35 eV (Ref. 39) or 0.36 eV.[40,41] The closely related trivacancy-oxygen complex gives rise to a double acceptor state at E_C–0.34 eV.[40,41] The corresponding single acceptor has an activation energy in the range of E_C–0.46 eV, hidden by peak E4. The latter has a too high activation energy to correspond with V_3(0/-) or V_3O(0/-), casting some doubt on this interpretation for the E_C–0.365 eV level. Alternatively, the electron trap could correspond with the tetravacancy found at E_C–0.37 eV.[39]

Several DLTS studies report on radiation-induced deep levels in n-type silicon with activation energy higher than 0.5 eV, appearing in the spectra close to room temperature.[18,20,36,42–45] These deep states have been assigned to higher-order vacancy clusters (e.g., the pentavacancy),[36,45] possibly stabilized by Ar atoms, nanocavities (bigger vacancy cluster)[42] or even a disordered silicon region.[20] The thermal stability of these clusters is usually higher than for the more simple radiation-induced point defects (V_2, V-O,…), so that they are harder to remove by a thermal treatment after dry etching. We tentatively assign the E4 trap to a higher-order vacancy cluster. In fact, the shoulder noticeable at room temperature in Fig. 4 could well correspond with the D3 level of Ref. 45 at E_C–0.64 eV. Comparing with the case of H_2-plasma etching, one can conclude that more complex point-defects are formed in the case of NF_3/Ar-plasma etching, corresponding to higher-order vacancy clusters, possibly incorporating Ar atoms, which are harder to remove by a thermal post-treatment.

Comparing the trend derived from the DLT-spectra of Figs. 3, 4, 6, and 8 and the lifetime data from Figs. 10 and 12, one can derive a qualitative agreement, especially for the H_2-plasma treated samples. This means that increasing the amount of dry-etch damage, corresponding with increasing DLTS peak height and width, gives rise to a reduction of τ. The same is also true for the NF_3/Ar plasma case, although no detectable deep levels were observed in Fig. 3(a) for sample A, while a slight lifetime reduction is observed in Figs. 9 or 10. Given the DLTS detection limit of $\sim 10^{-4}$ times the background doping density, the minimum detectable trap concentration is in the range of a few times $10^{11}\,cm^{-3}$. The observation that recombination lifetime measurements are more sensitive than DLTS does not come as a surprise: the theoretical limit for the minority carrier lifetime in 5–10 Ωcm silicon is determined by band-to-band recombination and amounts to 0.5 s.[46] This means that the detection limit for deep levels is on the order of $10^7\,cm^{-3}$, which is much lower than for DLTS. The fact that the recombination lifetime in Fig. 10 is slightly degraded even for the samples dry-etched at a power of 250 W compared to the reference wafer, suggests that the corresponding electron traps are below the $\sim 10^{11}\,cm^{-3}$ detection limit for DLTS or that hole traps in the bottom half of the band gap dominate τ. The latter can normally not be detected in a SB on n-type silicon, unless an optical injection pulse is employed.[16]

V. CONCLUSION

It has been shown that the nature of the dry-etch damage derived from DLTS on n-type FZ silicon wafers, subjected to an NF_3/Ar- or a H_2-plasma, is different. In the former case, a number of electron traps is found in the near surface region, which are assigned to vacancy- and vacancy-impurity clusters. For H_2-plasma etching, more simple point defects are found for less aggressive conditions, while this develops into an amorphouslike, highly damaged silicon top layer for exposures at higher power or longer times. While DLTS is useful for the identification of the responsible deep levels, lifetime measurements are shown to be more sensitive to lower damage levels. The combination of both techniques can be helpful in order to define optimized etch conditions (or postetch treatments) for solar cell applications.

ACKNOWLEDGMENTS

Part of this work has been financed through the H2020 EU project NextBase under Contract No. 727523.

[1]M. Tang *et al.*, IEEE J. Photovoltaics **6**, 10 (2016).
[2]C. Trompoukis, A. Stesmans, E. Simoen, V. Depauw, O. El Daif, I. Gordon, R. Mertens, and J. Poortmans, Phys. Status Solidi RRL **10**, 158 (2016).
[3]H. Savin, P. Repo, G. von Gastrow, P. Ortega, E. Calle, M. Garín, and R. Alcubilla, Nat. Nanotechnol. **10**, 624 (2015).
[4]M. M. Plakhotnyuk, M. Gaudig, R. Schmidt Davidsen, J. M. Lindhard, J. Hirsch, D. Lausch, M. S. Schmidt, E. Stamate, and O. Hansen, J. Appl. Phys. **122**, 143101 (2017).
[5]H. Sivaramakrishnan Radhakrishnan *et al.*, *Proceedings of the 43rd IEEE Photovoltaic Specialists Conference (PVSC)* (2016), p. 1182.
[6]T. Tachibana, D. Takai, T. Kojima, T. Kamioka, A. Ogura, and Y. Ohshita, ECS J Solid State Sci. Technol. **5**, Q253 (2016).
[7]B. Demaurex, R. Bartlome, J. P. Seif, J. Geissbühler, D. T. L. Alexander, Q. Jeangros, C. Ballif, and S. De Wolf, J. Appl. Phys. **116**, 053519 (2014).
[8]S. J. Fonash, J. Electrochem. Soc. **137**, 3885 (1990).
[9]K. Uejima and T. Umeda, Appl. Phys. Lett. **104**, 082111 (2014).
[10]T. Iwai, K. Eriguchi, S. Yamauchi, N. Noro, J. Kitagawa, and K. Ono, J. Vac. Sci. Technol., A **33**, 061403 (2015).
[11]D. Misra and E. L. Heasell, J. Electrochem. Soc. **136**, 234 (1989).
[12]M. Okigawa, Y. Ishikawa, Y. Ichihashi, and S. Samukawa, J. Vac. Sci. Technol., B **22**, 2818 (2004).
[13]J. P. Carrère *et al.*, Solid-State Electron. **65-66**, 51 (2011).
[14]T. Morimoto, H. Ohtake, and T. Wanifuchi, J. Vac. Sci. Technol., B **33**, 051811 (2015).
[15]D. V. Lang, J. Appl. Phys. **45**, 3023 (1974).
[16]E. Simoen, J. Lauwaert, and H. Vrielinck, *Semiconductors and Semimetals*, in edited by L. Romano, V. Privitera, and C. Jagadish (Elsevier, San Diego, 2015), Vol. 91, p. 205.
[17]J. Garrido, E. Calleja, and J. Piqueras, Solid-State Electron. **24**, 1121 (1981).
[18]G. Adegboyega, I. Perez-Quintana, A. Poggi, E. Susi, and M. Merli, J. Vac. Sci. Technol., B **15**, 623 (1997).
[19]P. N. K. Deenapanray, F. D. Auret, and G. Myberg, J. Vac. Sci. Technol., B **16**, 1873 (1998).
[20]S. Zhu, C. Detavernier, R. L. Van Meirhaeghe, F. Cardon, A. Blondeel, P. Clauws, G.-P. Ru, and B.-Z. Li, Semicond. Sci. Technol. **16**, 83 (2001).
[21]A. Szekeres, S. S. Simeonov, and E. Kafedjiiska, Physica B **170**, 231 (1991).
[22]A. Szekeres, S. S. Simeonov, and E. Kafedjiiska, Semicond. Sci. Technol. **9**, 1795 (1994).
[23]F. D. Auret, R. Kleinhenz, and C. P. Schneider, Appl. Phys. Lett. **44**, 209 (1984).
[24]C. Christensen, J. Wulff Petersen, and A. Nylandsted Larsen, Appl. Phys. Lett. **61**, 1426 (1992).
[25]W. Schröter, J. Kronewitz, U. Gnauert, F. Riedel, and M. Seibt, Phys. Rev. B **52**, 13726 (1995).
[26]D. Cavalcoli, A. Cavallini, and E. Gombia, Phys. Rev. B **56**, 10208 (1997).
[27]W. Schröter and H. Cerva, Solid State Phenom. **85-86**, 67 (2002).
[28]E. Simoen, V. Ferro, and B. J. O'Sullivan, J. Appl. Phys. **116**, 234501 (2014).
[29]E. Simoen, D. Visalli, M. Van Hove, M. Leys, G. Borghs, A. P. D. Nguyen, and A. Stesmans, Phys. Status Solidi A **209**, 1851 (2012).
[30]A. Masolin, E. Simoen, J. Kepa, and A. Stesmans, J. Phys. D. **46**, 155501 (2013).
[31]T. Rahman *et al.*, Prog. Photovoltaics Res. Appl. **26**, 38 (2018).
[32]S. Rein, T. Rehrl, W. Warta, and S. W. Glunz, J. Appl. Phys. **91**, 2059 (2002).
[33]J. Schmidt, Appl. Phys. Lett. **82**, 2178 (2003).
[34]W. Warta, Phys. Status Solidi A **203**, 732 (2006).
[35]S. J. Pearton, J. W. Corbett, and T. S. Shi, Appl. Phys. A **43**, 153 (1987).
[36]F. D. Auret, P. N. K. Deenapanray, S. A. Goodman, W. E. Meyer, and G. Myburg, J. Appl. Phys. **83**, 5576 (1998).
[37]G. Alfieri, E. V. Monakhov, B. S. Avset, and B. G. Svensson, Phys. Rev. B **68**, 233202 (2003).
[38]M. Mikelsen, E. V. Monakhov, G. Alfieri, B. S. Avset, and B. G. Svensson, Phys. Rev. B **72**, 195207 (2005).
[39]M. Ahmed, S. J. Watts, J. Matheson, and A. Holmes-Siedle, Nucl. Instrum. Methods Phys. Res. A **457**, 588 (2001).
[40]V. P. Markevich *et al.*, Phys. Rev. B **80**, 235207 (2009).
[41]N. Ganagona, L. Vines, E. V. Monakhov, and B. G. Svensson, J. Appl. Phys. **116**, 124510 (2014).
[42]V. Raineri, G. Fallica, and S. Libertino, J. Appl. Phys. **79**, 9012 (1996).
[43]P. K. Giri and Y. N. Mohapatra, J. Appl. Phys. **84**, 1901 (1998).
[44]P. K. Giri and Y. N. Mohapatra, Semicond. Sci. Technol. **15**, 985 (2000).
[45]Y. Nakano, M. Ishiko, and H. Tadano, J. Vac. Sci. Technol., B **20**, 379 (2002).
[46]A. A. Istratov, H. Hieslmair, and E. R. Weber, Appl. Phys. A **70**, 489 (2000).