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Trap characteristics of hafnium oxide-based ferroelectric field-effect transistors measured by using a current transient method

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ABSTRACT

The trap characteristics and polarization effect on the trapping behavior in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric field-effect transistors were analyzed. The current transient that corresponds to the trapping/detrapping of charge carriers was measured and the exact time constant spectra were extracted. In accordance with the different time constants and activation energies as well as the dependence of the trapping behavior on the filling conditions, traps that originated from the oxygen vacancies in the $Hf_{0.5}Zr_{0.5}O_2$ layer and from the Si/SiO_2 interface trap states were identified. The detrapping peaks in time constant spectra showed a consistent changing trend with the variation of remanent polarization, confirming that the positive polarization enhanced the trapping of charge carriers injected from channel side to the ferroelectric layer.

Ferroelectric field-effect transistors (FEFETs) have attracted substantial attention in the fields of memory[1] and neuromorphic devices.[2] Doped HfO_2 films are promising candidates for high-performance FEFETs because of their advantages, including fast switching, low power consumption, good retention, and high complementary metal–oxide–semiconductor compatibility.[3] However, there are inherent defects and traps that might be located at various positions within the devices. For example, HfO_2 materials are characterized by high intrinsic defect densities (10^{12} to 10^{14} cm^{-2}).[4,5] These defects can function as charge carrier traps and fixed charges,[6–8] which correspond to instability in the device electrical performance and undermine reliability. Degradation of FEFET devices, including endurance failure, retention loss, and imprint, are all closely related to trapping behavior.[9–11] Some recent work has identified charge trapping and trap generation as primary causes for endurance failure, even before fatigue of polarization in the HfO_2 ferroelectric layer.[6,12,13] Therefore, an increasing body of research has been carried out to study the trapping and detrapping behaviors in FEFETs.[6,14] Various methods have been used for analysis, including fast sweeping operation,[15] the quasi-static split capacitance–voltage technique,[16] pulsed I_D–V_G measurements,[17] and subthreshold swing analysis.[18] Nevertheless, detailed understanding of the characteristics of traps is still needed. Identifying various traps, their corresponding distributions, and activation energies remains incomplete; such work would provide valuable and direct information for understanding the trapping mechanism as well as for improved control and optimization of FEFET devices.

In this work, the present authors characterized the traps in FEFETs based on measuring the current transient, which depends on the trapping and detrapping of charge carriers. This transient method as proposed here has previously been used to analyze the trap characteristics in $BiFeO_3$ thin-film capacitors[19] and low-temperature polysilicon thin-film transistors.[20] FEFETs exhibit a complex device structure and material composition, especially in terms of the polarization effect, which requires refined measurement techniques and improved analysis methods. The trapping/detrapping behaviors that originate from various types of traps within the device should be distinguished and the underlying trapping mechanisms should be revealed. The effect of the polarization state in the ferroelectric layer on the trapping behaviors needs to also be investigated.

The n-channel FEFETs were fabricated on p-Si(100) substrates. The gate stack consisted of 75-nm W, 10-nm TiN, 10-nm $Hf_{0.5}Z_{0.5}O_2$ (HZO), and 0.7-nm SiO_2, as illustrated by the inset of Fig. 1(a). The HZO thin film was grown at 300 °C by atomic layer deposition,

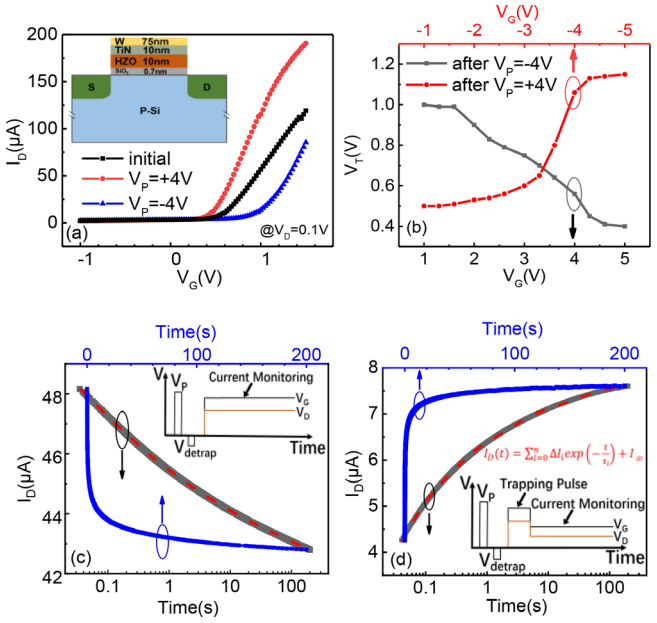

FIG. 1. (a) Transfer I_D–V_G curves for HZO FEFET after positive and negative gate polarization voltages. The inset shows the schematic of the device structure. (b) Transition of the threshold voltage as a function of the gate polarization voltages after setting to low and high V_T states. (c) The trapping and (d) detrapping drain current transient of I_D with respect to time (black solid: experimental data and red dashed: fitting curve). The insets show the voltage sequence diagrams used in the experiment.

followed by deposition of TiN and W as the top gate electrode. The structure was treated by rapid thermal annealing at 550 °C for 1 min for crystallization. The channel length and width of the transistors were 100 and 150 μm, respectively. The electrical characteristics of the devices were measured with a semiconductor parameter analyzer (B1500A, Agilent Technologies, USA). In addition, the TiN/10-nm HZO/TiN capacitors were fabricated and the ferroelectric properties of the HZO thin films were evaluated. The polarization–voltage hysteresis loops of the capacitors were measured with a Radiant Precision workstation. The temperature variation experiments were performed with a vacuum probe station and a precision temperature source (Scientific Instrument model 9700).

The transfer I_D–V_G curves measured after application of the gate polarization voltage $V_P = \pm 4$ V are shown in Fig. 1(a). The threshold voltage V_T was determined as a gate voltage, corresponding to a specified value of the drain current (10^{-7} A × width/length).[21] The positive and negative V_P set a low V_T and high V_T, respectively, which typically originate from the polarization switching of a HZO thin film that can modulate the channel conductivity.[22] After setting to the high V_T state by $V_P = -4$ V, a sequence of positive gate voltages was applied. Figure 1(b) shows the V_T transition as a function of the gate voltages, demonstrating a gradual change to a low V_T state, which started at +1.6 V and completed at +4.3 V. Conversely, after applying a $V_P = +4$ V, the transition of threshold voltage from low to high V_T started at −1.6 V and completed at −4.3 V. Therefore, the switching of the polarization in the HZO layer was when the magnitude of the gate voltage was between 1.6 and 4.3 V for the device.

In the trapping experiment, a sequence of voltage [inset in Fig. 1(c)] was applied to measure the current transient. To ensure the experiment was carried out under the same polarization state, a 500-μs-long $V_P = 4$ V pulse was first applied on the gate. Then, a pulse with 500-μs-long $V_{detrap} = -1$ V, which cannot switch the polarization, was applied to expel the electrons[15,23] that were trapped during the polarization in a manner that obtained the same initial conditions. Subsequently, the current transient was measured at $V_G = 2$ and $V_D = 0.5$ V over a period of time. Figure 1(c) displays the change in the drain current I_D with respect to time in linear and logarithmic scale, demonstrating a decreasing trend that corresponds to the trapping of charge carriers. Regarding the detrapping experiments, the V_P and V_{detrap} pulses were performed following the same process as that in the trapping experiment. Then, both the gate and drain voltages (e.g., $V_G = 2$ and $V_D = 2$ V) were synchronously pulsed for 5 s. Immediately after the trapping pulse was removed, the current was monitored under the voltages ($V_G = 0.8$ and $V_D = 0.1$ V) over 200 s, which was sufficiently small to not perturb the trapping or detrapping states of the device. Figure 1(d) indicates an increasing current transient which eventually reached a steady state. This corresponded to the detrapping process as a result of charge carriers release from trap sites after the trapping process. A detrapping (trapping) current transient was assumed to involve several independent processes of releasing (capturing) charge carriers, each contributing to an exponential increase or decrease in the current. The current vs time data $I_D(t)$ can be fit with the following equation:[24]

$$I_D(t) = \sum_{i=0}^{n} \Delta I_i \exp\left(-\frac{t}{\tau_i}\right) + I_\infty, \tag{1}$$

where τ_i is the time constant of different traps, n is the number of traps with different τ, ΔI_i is the amplitude that affects the current change, and I_∞ is the steady current. Figures 1(c) and 1(d) indicate that Eq. (1) fits the experimental results well. To evaluate the time constant, a method was used based on the Bayesian deconvolution that had been proposed by Szekely for extracting heat time constants from thermal transients.[25,26] This method can prevent small ripples and performs well in terms of distinguishing close peaks.

First, a logarithmic variable is introduced for the time,

$$z = \ln t. \tag{2}$$

The time constant spectrum of traps is then defined as

$$\Delta I(z) = \lim_{\delta z \to 0} \frac{magnitudes\ related\ to\ the\ time\ constants\ between\ z\ and\ z+\delta}{\delta z}. \tag{3}$$

Now, the current transient can be expressed in Eq. (4), and the time constant spectrum in Eq. (3) exists in integral form in the following equation:

$$I_D(t) = \int_{-\infty}^{\infty} \Delta I(\tau)\left(\exp\left(-\frac{t}{\exp(\tau)}\right)\right) d\tau + I_\infty. \tag{4}$$

This is a generalization of the summation used in Eq. (1). Using Eq. (2), the transient current is converted into

$$I_D(z) = \int_{-\infty}^{\infty} \Delta I(\tau)(\exp(-\exp(z-\tau)))d\tau + I_\infty. \quad (5)$$

This is the convolutional integral equation of $\Delta I(\tau)$. Differentiating z on both sides of Eq. (5) then gives

$$\frac{d}{dz} I_D(z) = \int_{-\infty}^{\infty} \Delta I(\tau)(\exp(z-\tau-\exp(z-\tau)))d\tau. \quad (6)$$

Here, we define a function W(z) as follows:

$$W(z) = \exp(z - \exp(z)). \quad (7)$$

Then, $\frac{d}{dz} I_D(z)$ in Eq. (6) can be represented by

$$\frac{d}{dz} I_D(z) = -\Delta I(z) \otimes W(z), \quad (8)$$

where $\otimes$ is the symbol of the convolution operation. The time constant spectrum $\Delta I(z)$ is then expressed as

$$\Delta I(z) = \left(-\frac{d}{dz} I_D(z)\right) \otimes^{-1} W(z). \quad (9)$$

Finally, the time constant spectrum can be solved completely via deconvolution.

Figures 2(a)–2(c) show the extracted time constant spectra, with the magnitude of the trapping or detrapping plotted as the y axis with respect to lg(t) as the x axis. There were multiple peaks on the spectra with different time constants. The peak amplitude represents the trapping or detrapping degree that contributed to the change in current transients. It is closely related to the number of trapped charge carriers; the time constant indicates the time when the maximum number of charge carriers were captured or released. The three peaks were between 100 ms and 10 s, which is consistent with the reported time range of spontaneous detrapping.[12,23]

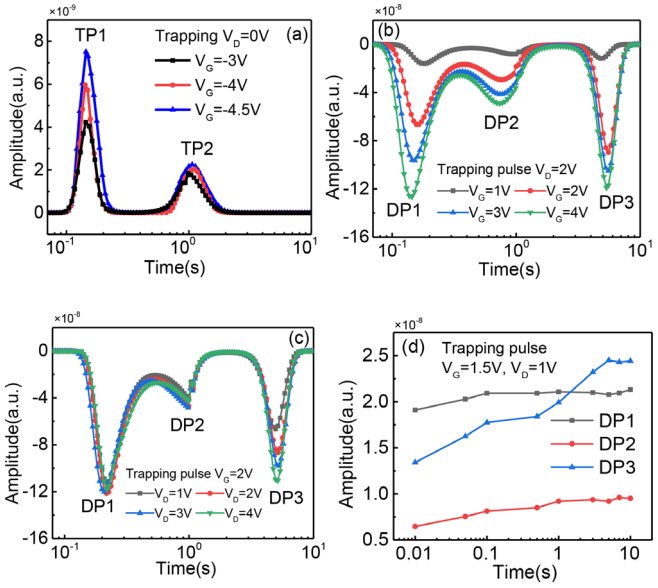

FIG. 2. (a) Time constant spectra for the gate trapping transients of I_G under the off-state trapping voltages with $V_D = 0$ V and different $V_G = -3$ to -4.5 V. (b) Time constant spectra for the drain detrapping transients of I_D. Trapping pulses: 5 s, $V_D = 2$ V, and $V_G = 1$–4 V; current monitoring: $V_G = 0.8$ and $V_D = 0.1$ V. (c) Time constant spectra for the drain detrapping transients. Trapping pulses: 5 s, $V_G = 2$, and $V_D = 1$–4 V; current monitoring: $V_G = 0.8$ and $V_D = 0.1$ V. (d) Change in the peak amplitude (DP1, DP2, and DP3) with increasing trapping time for constant trapping voltages of $V_G = 1.5$ and $V_D = 1$ V.

Different trapping conditions were applied to study the filling states of different traps within the device. Figure 2(a) shows the trapping time constant spectra derived from the current transient of I_G (gate leakage current) under the off state ($V_D = 0$ and $V_G < 0$ V). Two trapping processes (labeled TP1 and TP2) were identified. When different values of V_G (-3 to -4.5 V) were applied, the peak values of TP1 and TP2 increased with decreasing V_G; the time constant for each trapping process did not change. Because all of the trapping in the $V_G < 0$ and $V_D = 0$ state should be caused by the gate leakage current, TP1 and TP2 can be derived to be associated with the injection of electrons from the gate and trapping inside the gate oxide layer. Figure 2(b) shows the time constant spectra extracted from the detrapping transient of I_D measured after the on-state trapping pulses ($V_D = 2$ and $V_G = 1$–4 V). The spectra exhibited a negative peak because of the negative ΔI_i [Eq. (1)] for detrapping. DP1 and DP2 exhibited a time constant that was consistent with TP1 and TP2, respectively. It is reasonable to hypothesize that such detrapping originates from the same traps associated with TP1 and TP2; whereas after the on-state trapping, the detrapping now resulted from these traps that captured the injected electrons from Si under the positive electric field and their peak amplitude increased with increasing V_G. In addition, there was a third detrapping process, labeled as DP3, indicated in the spectra after the on-state trapping pulse. Furthermore, Fig. 2(c) shows that the amplitude of DP3 increased with increasing trapping voltage V_D when V_G was maintained at 2 V, indicating that DP3 should correspond to the trapping of channel electrons that are related to channel current. In contrast, DP1 and DP2 remained almost constant at various V_D, which could be attributable to the constant gate voltage for the injection of electrons. The dependence of the detrapping behavior on the time duration of the trapping pulse was also studied. The amplitude of detrapping first increased with increasing trapping pulse duration and then remained nearly constant when the pulse was longer than the time constant for each trapping/detrapping process, which was ~0.1 s for DP1, ~1 s for DP2, and ~5 s for DP3. Regarding the constant trapping voltage with a brief pulse duration, the injection of charge carriers was small, such that filling of the traps did not saturate. As the trapping pulse duration increased to the extent that it was longer than the time constant, the filling status of the traps under this voltage condition was almost complete, such that the filling status did not change, resulting in a stable detrapping amplitude.

The traps' activation energy were identified by performing current transient experiments at various temperatures. It can be seen from Fig. 3(a) that the time constant of DP1, DP2, and DP3 shifted rightward with decreasing temperature, indicating that they were thermally activated. The polarization of ferroelectric materials is relatively stable when the temperature decreases below room temperature.[27] Figure 3(b) also confirms that the remanent polarization of the TiN/HZO/TiN capacitor was almost unchanged within 303–283 K. Therefore, the polarization variation is not the reason that underpins the shift of the time constant. On the basis of the Arrhenius plots, DP1, DP2, and DP3 exhibited activation energies E_a of 0.34, 0.18, and

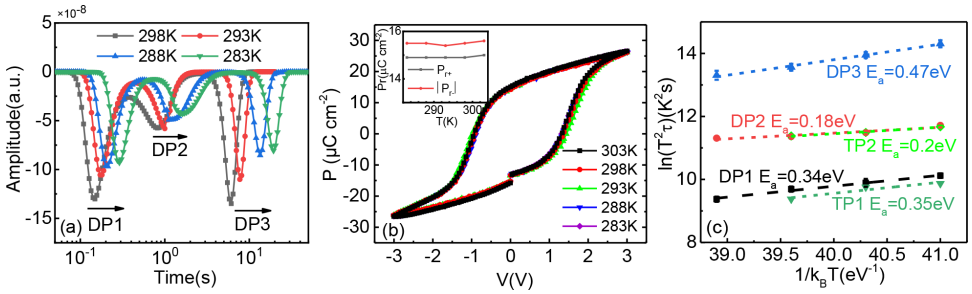

FIG. 3. (a) Change in time constant spectra for the detrapping current transient after 5-s $V_G = 2$ and $V_D = 1$ V trapping pulse as a function of decreasing temperature. (b) P–V hysteresis loops of TiN/HZO/TiN measured at a 1-kHz triangular sweep voltage at various temperatures below room temperature. The inset shows the change in remanent polarization with decreasing temperature. (c) The Arrhenius plot of the time constant, used to derive the activation energy of traps.

0.47 eV, respectively, as shown in Fig. 3(c). The E_a of TP1 and TP2 was figured out to be 0.35 and 0.2 eV, confirming the same nature of DP1/TP1 and DP2/TP2, respectively. The measured activation energies of DP1 and DP2 are consistent with oxygen vacancies in hafnium-based gate stack devices. Such vacancies are the dominant intrinsic defects in bulk HfO_2 thin films, which can trap injected electrons, forming $V_O^{\cdot}$ (sometimes referred to as V^{-}) and $V_O^{\times}$ (sometimes referred to as V^{2-}) vacancies.[4,7] They are relatively shallow with energies in the range of 0.2–0.3 eV with respect to the bottom of the conduction band.[4,28] In addition, although the thermal activation energies of $V_O^{\cdot}$ and $V_O^{\times}$ are very similar, $V_O^{\times}$ exhibits a slightly lower energy (0.1–0.2 eV) than $V_O^{\cdot}$ oxygen vacancies because of electron repulsion,[4] which corresponds to the difference in E_a between DP1 and DP2. Recently, the oxygen vacancy defects were studied by the first principles calculations in the orthorhombic-$Hf_{0.5}Zr_{0.5}O_2/SiO_2/Si$ gate stack.[29] We would like to note that the calculated values of defect levels may not be directly corresponding to the thermal activation energy of oxygen vacancies. Because the thermal activation of a trap is a phonon assisted process, during which the significant lattice relaxation occurs associated with the change in the charge state of the vacancy. Compared with the defect levels in the first principles calculations,[29] the measured E_a of oxygen vacancies are 0.5–1.0 eV smaller, which might be attributed to the lattice relaxation energy.[4,7] However, it should be noted that the calculated defect levels of $V_O^{\cdot}$ and $V_O^{\times}$ vacancies also differ by 0.1–0.25 eV,[29] which is in good agreement with our measured energy difference between DP1 and DP2.

Regarding DP3, a trap located near its energy level has been reported for Si/SiO_2 interface trap states.[30–32] On the basis of the activation energy and the dependence of trapping/detrapping characteristics on filling conditions in Fig. 2, a schematic of the trapping behavior in the device and the corresponding band diagram are shown in Figs. 4(a) and 4(b). The oxygen vacancies $V_O^{\cdot}$ and $V_O^{\times}$ are considered as the physical origin for the detrapping behavior of DP1 and DP2, respectively, located in the HZO layer. In the on-state (trapping pulse $V_G > 0$ V), electrons can be injected by tunneling[12] and become trapped in the HZO region. Concomitantly, the channel electrons can also be captured by the traps at the Si/SiO_2 interface (DP3) under the action of positive gate voltage. The rise of V_G leads to an increase in all three trapping and following detrapping processes. In addition, as V_D increases, the electric field at the region near the drain side increases, which facilitates the trapping process of DP3. However, in the off-state (trapping pulse $V_G < 0$ V, $V_D = 0$ V), there is a lack of inversion channel electrons. The gate leakage current injects electrons and only the trapping in the HZO layer (TP1/DP1 and TP2/DP2) takes place.

We further investigated the polarization effects on the trapping behavior. Before the detrapping experiments were performed, a pre-poling voltage of −4 V was first applied on the gate. Then, various poling voltages V_P were applied in the voltage sequence diagram [inset of Fig. 1(d)]. The same trapping pulse with 5-s-long $V_G = 1.5$ and $V_D = 1$ V and a monitoring voltage of $V_G = 0.8$ and $V_D = 0.1$ V were used for measurements of the current transient under different polarization states. It can be seen in Fig. 5(a) that the peak amplitude of DP1 and DP2 increased with increasingly positive V_P from 2 → 4 V. Such an increasing poling voltage can align the polarization as follows: gradually pointing from the gate to the Si substrate [P_{r+} in Fig. 4(c)]. Figure 5(c) shows the measured P–V loops of the FEFET. From 3 to 4 V poling voltage, the positive remanent polarization increased from a value of 9.2 to a value of 16.3 μC cm^{-2}. Meanwhile, the detrapping peaks under the corresponding polarization state increased by 44% and 31% for DP1 and DP2, respectively. The total percentage increase in DP1 and DP2 was close to the 77% increase in remanent polarization. As a comparison, different negative V_P voltages were applied on the gate after application of the +4 V pre-poling voltage. Figure 5(b) indicates that the peak amplitude of DP1 and DP2 decreased with decreasing negative poling voltage (−2→−3.5 V), which gradually switched the positive polarization (by +4 V pre-poling) in the negative direction. The change in the trapping and detrapping behaviors, thus,

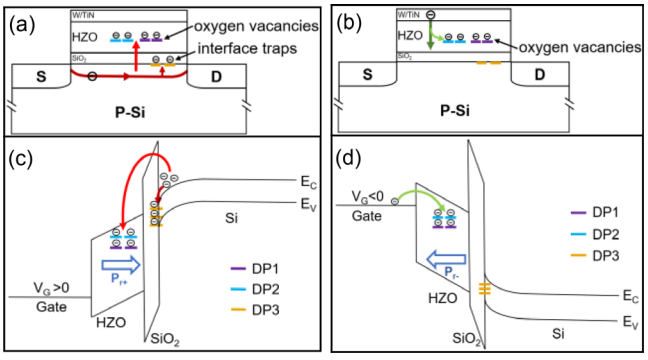

FIG. 4. Schematic of trapping behavior and corresponding energy band diagram for the (a) and (c) on-state and (b) and (d) off-state, respectively. Red and green arrows represent the electron flow. Polarization is shown by blue arrows.

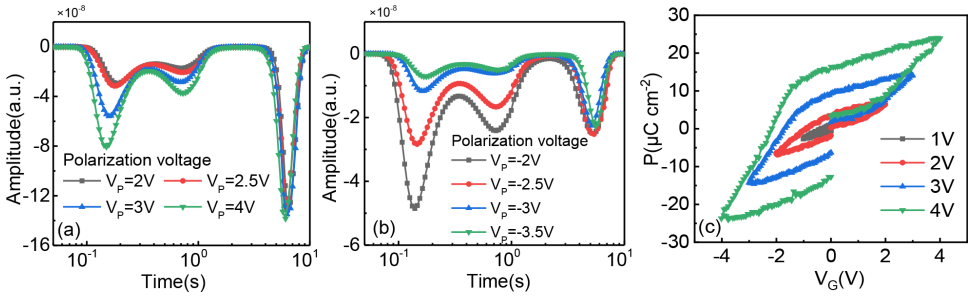

FIG. 5. Time constant spectra under various polarization states caused by the (a) positive and (b) negative gate poling voltages V_P. The same measurement conditions for the detrapping current transient were used: 5-s $V_G = 1.5$ and $V_D = 1$ V trapping pulse and $V_G = 0.8$ and $V_D = 0.1$ V monitoring voltage. (c) P–V characteristics of the FEFET measured at 1-kHz triangular waveforms when the S/D was connected.

corresponded to the polarization state in the ferroelectric layer. As the positive polarization increased, the induced electric field in the SiO_2 layer became increasingly strong.[12,22] Such a large electric field forced a substantial band-bending of the SiO_2 layer, which facilitated injection of electrons from the channel side through tunneling. An increasing number of electrons were trapped in the HZO layer, resulting in larger detrapping peaks. However, when an increasingly negative poling voltage was applied, the positive polarization decreased and even reversed. The band-bending of the SiO_2 layer was alleviated, such that the injection of electrons decreased under the positive trapping pulse, and thus, the detrapping peak became smaller. DP3 seems to not have been affected by the polarization state [Figs. 5(a) and 5(b)]. This observation can be understood in terms of the fact that DP3 was located at the Si/SiO_2 interface and captured the channel electrons, which were not affected by the tunneling behavior of the electrons.

In summary, a current transient technology was applied for the characterization of traps in HZO FEFETs. The method consisted of measuring the trapping/detrapping transients and extracting the corresponding time constant spectra. Three types of detrapping peaks were identified. Their peak amplitudes exhibited a dependence on the trapping voltages and time durations, and they were thermally activated with different activation energies. The distribution and physical originations of the traps were determined based on their trapping characteristics. The polarization state was revealed to affect the trapping behavior in the HZO layer but exhibited a little effect on the trapping of interface traps. This work has provided a useful method for characterizing and analyzing traps in FEFETs. It allows us to further our understanding of the trapping and detrapping mechanism in ferroelectric film-based field-effect transistors.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yilin Li: Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Yerong Sun:** Resources (equal). **Shiwei Feng:** Methodology (equal); Resources (equal). **Hui Zhu:** Conceptualization (equal); Formal analysis (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Xing Liu:** Resources (equal). **Xiaolei Wang:** Resources (equal). **Hao Xu:** Resources (equal). **Shijie Pan:** Methodology (equal); Software (equal). **Jinjuan Xiang:** Resources (equal). **Lixing Zhou:** Resources (equal). **Zhiwen Yao:** Resources (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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