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DEFECTS IN SEMICONDUCTORS AND THEIR EFFECTS ON DEVICES ☆

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Abstract—The classification of defects in semiconductors and their electronic properties are discussed. The sources of dislocations in bulk crystals and defects in epitaxial layers have been identified. Some of the approaches used to lower the density of dislocations in crystals and layers are presented. Effects of defects on devices are also considered.

Keywords: Semiconductors; Defects; Devices; Electrical properties; Dislocations

1. INTRODUCTION

Using dimensionality as a criterion, defects in semiconductors can be divided into four different categories: zero-, one-, two- and three-dimensional. The respective examples are vacancies or interstitials, dislocations, stacking faults or grain boundaries and precipitates.

It is widely recognized that the performance, yield, reliability and degradation behavior of minority carrier devices are adversely affected by the presence of defects [1]. Brantley and Harrison [2] have observed that when a compressive load is applied to diffused GaAs electroluminescent diodes, their degradation rate increases by an order of magnitude and the degradation is accompanied by the multiplication of dislocations. The study of Roedel *et al*. [3] has correlated the reduction in external quantum efficiency of silicon-doped GaAs light emitting diodes (LEDs) with dislocation densities and has demonstrated that the line imperfections act as nonradiative recombination centers.

That dislocations and stacking faults play an important role in the degradation of laser diodes is well documented [4–9]. Darkline defects (DLDs) observed in degraded GaAlAs/GaAs lasers appear to originate from existing dislocations. DLDs oriented along the ⟨110⟩ directions evolve by dislocation glide, whereas the ⟨100⟩ DLDs develop by glide and climb. The work on optically degraded InGaAsP epilayers that are used in light emitters for lightwave communication systems indicates that nonluminescent regions contain dislocation networks that appear to form by glide [7]. Dutt *et al*. [8] have shown that dislocations and stacking faults have deleterious effects on the performance of GaAlAs/GaAs LEDs. The recent study of Guha *et al*. [9] has also demonstrated that stacking faults play a significant role in the degradation of ZnSe-based lasers.

It is apparent from above that defects have deleterious effects on the performance and reliability of devices. To enhance the device performance, we need to understand the origins and reduction of defects in semiconducting substrates and epitaxial layers. Therefore, we briefly cover in this article the electronic properties of defects in semiconductors, the sources of defects in bulk crystals and epitaxial layers, some of the approaches developed for defect reduction and the effects of defects on devices.

2. ELECTRONIC PROPERTIES OF DEFECTS

Elemental semiconductors, such as Si and Ge, crystallize in the diamond-cubic structure in which atoms are tetrahedrally coordinated and are covalently bonded. This structure consists of two interpenetrating f.c.c. sublattices that are displaced from each other by $a/4\langle 111\rangle$, where a is the lattice parameter. Both sublattices are occupied by the same type of atoms. On the other hand, III–V and II–VI semiconductors crystallize in the zinc-blende structure that also consists of two interpenetrating f.c.c.

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sublattices. One of the sublattices consists of only group III or II atoms, whereas group V or VI atoms occupy the second sublattice. The bonding in these semiconductors is partly covalent and partly ionic and the ionic component increases in going from III–V semiconductors to II–VI semiconductors.

2.1. Point defects

For the sake of discussion, let us consider the case of Si. A Schottky vacancy can be formed by removing one of the atoms from the crystal interior and bringing it to the surface. Its formation would produce four unpaired electrons, i.e. dangling bonds, that impart electronic properties to vacancies. There is a tendency for the pairing of these unpaired electrons. As a result, vacancies tend to exhibit acceptor-like behavior, and a distinct energy level within the band gap is associated with the pairing of each of the four unpaired electrons. Consequently, a vacancy in silicon can have four distinct energy levels associated with it. Experimentally, the acceptor levels at 0.11 and 0.4 eV below the conduction band edge have been identified in silicon [10]. A donor level at 0.35 eV from the valence band edge has also been observed and is attributed to bond distortion.

A Schottky interstitial can also exist in semiconductors. Such a defect can be formed by inserting an atom into one of the many interstitial sites within the diamond-cubic and zinc-blende structures. Since these structures are loosely packed, the energies of formation of interstitials are low in comparison with those for vacancies. For example, in silicon the respective formation energies are 1.1 and 2.3 eV.

An interstitial has four valence electrons that are not involved in covalent bonding with the adjoining atoms. The successive loss of these unpaired electrons to the conduction band could, in principle, produce four different donor levels within the band gap. Experimentally, only a singly ionized donor level at 0.9 eV below the conduction band edge is seen in silicon.

In addition to the types of defects discussed above, anti-site defects can form in III–V and II–VI compound semiconductors. It refers, for example, to an arsenic atom occupying the position of a gallium atom on the gallium sublattice and vice versa.

The situation regarding energy levels of point defects in compound semiconductors is quite complex and is not well understood. There are two reasons. First, the perfection as well as the purity of these materials is not comparable to that of silicon. Second, it is difficult to maintain stoichiometry during the growth and processing of III–V compound semiconductors because the vapor pressures of group V species are fairly high.

2.2. Line defects

The complexities of the diamond-cubic and zinc-blende structures are manifested in the structure of line defects. Since two interpenetrating sublattices are present, narrowly and widely separated {111} planes exist in the two structures. As a result, two types of $a/2\langle 110\rangle$ glide dislocations can form: glide and shuffle set [11, 12]. The extra half-planes of glide set dislocations terminate between the narrowly separated {111} planes, whereas termination occurs between the widely separated {111} planes for the shuffle set dislocations. The study of Gomez and Hirsch [13] has shown that dislocations belong to the glide set. In addition, Haasen [14] has suggested that two types of edge dislocations terminating either at a row of group III atoms or at a row of group V atoms are possible in compound semiconductors, and they are referred to as α and β dislocations.

The cores of the glide and shuffle set dislocations are associated with dangling bonds [11, 12]. Following Read [15–17], we can speculate on the electronic behavior of these dislocations in n- and p-type silicon. In n-type materials, dangling bonds can accept electrons from energy states in the conduction band to form pairs. Thus, dislocations behave as acceptors. On the other hand, we can argue that dislocations will act as donors in p-type silicon.

The above discussion assumes that dislocations are not dissociated into Shockley partials and reconstruction-induced elimination of dangling bonds does not occur [11]. Hirsch [18] has evaluated the occurrence of reconstruction at partials and finds that the cores of 30° partials are likely to be reconstructed, whereas the situation is not clear for 90° partials. The implication being that the electrical activity of dislocations could vary with their orientation.

A number of workers [19–22] have observed energy levels associated with dislocations in deformed silicon. Haasen and Schröter [19] and Labusch and Schröter [20] have shown that 60° dislocations in deformed p-type silicon introduce a band of levels at ~0.34 above the valence band edge. On the other hand, Grazhulis *et al*. [21] found a band of levels at 0.42 and 0.67 eV above and below the valence band and conduction band edges in deformed n- and p-type silicon. At present, it is difficult to fully reconcile various experimental observations with our understanding of dislocation structures. Furthermore, the electronic behavior of dislocations in compound semiconductors is not well understood because it is difficult to maintain their stoichiometry and purity [23].

2.3. Stacking faults, subgrain and grain boundaries

The formation of intrinsic and extrinsic stacking faults in the diamond-cubic and zinc-blende structures does not create dangling bonds at the fault–

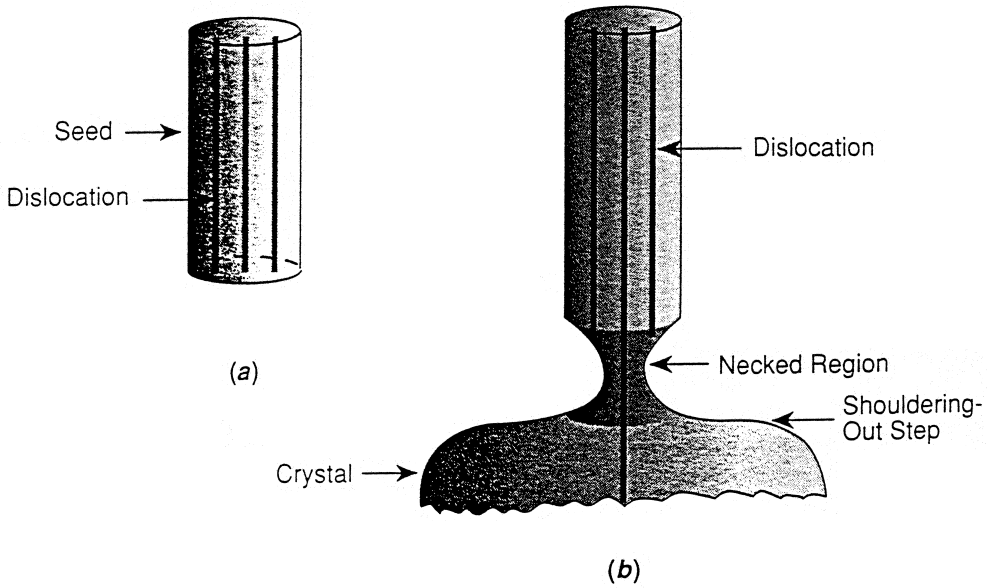

Fig. 1. (a) Schematic showing three dislocations in a seed crystal and (b) elimination of two of the dislocations by the formation of a necked region. After Mahajan and Sree Harsha [23].

matrix interfaces. Consequently, the fault surfaces are expected to be electrically inactive. However, dangling bonds exist along the bounding Shockley and Frank partials, and could cause electrical activity.

If we treat subgrain boundaries and grain boundaries as an assemblage of dislocations of appropriate Burgers vectors, we can then model the electrical behavior of these two-dimensional defects in terms of that of different dislocation configurations. Similarly, we can attribute the electrical activity of various types of precipitates to the associated interfacial dislocation structures.

3. SOURCES OF DEFECTS IN BULK CRYSTALS AND EPITAXIAL LAYERS AND THEIR REDUCTION

3.1. Bulk crystals

Multilayer epitaxial structures are required for many devices. For example, in optoelectronic devices four to five layer structures are used. These multilayers are grown on substrates that are obtained from single crystals. These substrates are a major source of dislocations in epitaxial structures [1, 23].

Dislocations in bulk crystals could originate from three different sources: (i) dislocations present in a seed crystal could propagate into a growing crystal, (ii) point defects could cluster to form dislocation loops during the cool down, and (iii) under the influence of thermal-gradient-induced stresses, dislocations present in the peripheral regions of a growing crystal could propagate into the interior of the crystal.

Two distinct situations arise when melt solidifies on a dislocated seed crystal: (i) Burgers vectors of the dislocations are inclined to the seed surface, and (ii) Burgers vectors of the dislocations are parallel to the seed surface. In the first case dislocations will be replicated into the newly formed crystal when the melt freezes epitaxially because of the presence of growth-spiral steps at the emergence point of dislocations at the seed–melt interface. In the second case, Beam *et al.* [24] have shown that dislocations will also be replicated because protrusions and depressions are produced at the surface where dislocations emerge. Therefore, all the dislocations present in the seed will be incorporated into the as-grown crystal. The cold seed is also thermally shocked when it is dipped into the melt during the Czochralski (CZ) growth, leading to dislocation multiplication. Therefore, we need approaches to prevent the propagation of dislocations from the seed and to reduce thermal shock.

The two approaches currently used for the growth of high-quality crystals are based on the original ideas of Dash [25, 26]. The use of small-diameter seeds reduces the magnitude of the thermal stresses because the radial temperature gradient is shallower for small seeds. Dash has also shown that the formation of a neck by an initial rapid pull can prevent the propagation of dislocations from the seed into the crystal. This is schematically illustrated in Fig. 1. Figure 1(a) shows three dislocations in a seed crystal. In the presence of a neck, only the central dislocation can propagate into the as-grown crystal as shown in Fig. 1(b); the other two terminate at free surfaces and are eliminated from the crystal. After forming the neck, the melt temperature is reduced and stabilized so that the desired ingot diameter can be produced. The central

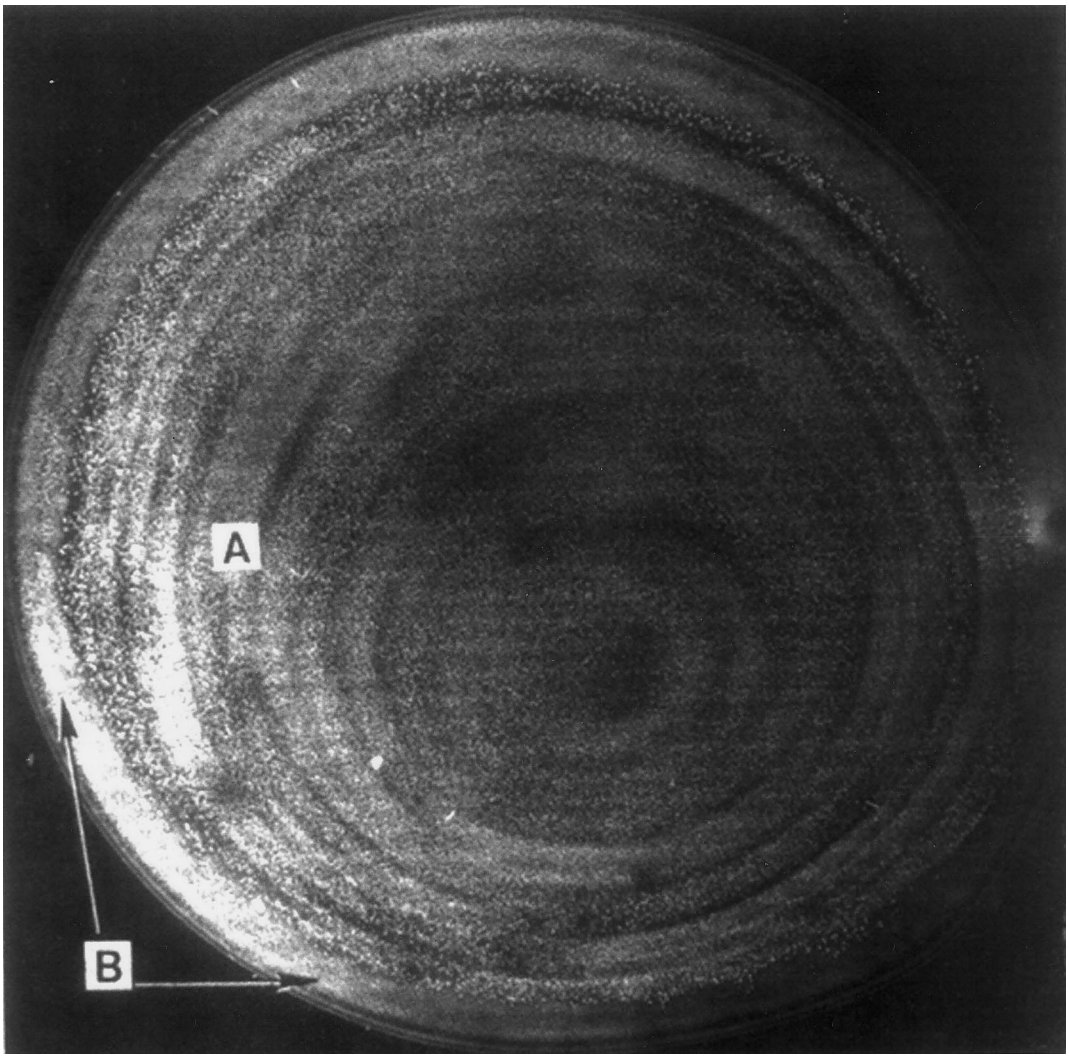

Fig. 2. X-ray transmission topograph of a copper-decorated transverse section taken from a dislocation-free float zone silicon crystal. A and B refer to A- and B-swirl defects. After deKock [31].

dislocation can also be eliminated if it could climb out of the crystal. To enhance the probability of climb, Dash has suggested that initially a crystal should be grown at a faster rate to incorporate nonequilibrium concentrations of point defects. These point defects could facilitate climb.

Since crystals are grown from the melt, the excess concentration of point defects is incorporated into a crystal. Clustering of excess point defects into faulted dislocation loops during the cool down can eliminate the supersaturation. The driving force for the formation of these loops is the overall reduction in the energy of the system. The energy change ΔE associated with the clustering of n interstitials into a dislocation loop of radius R is given by [23]

$$\Delta E = -4\pi nr^2\gamma + 2\pi R^2 E_{\mathrm{SFE}} + \pi RGb^2 \qquad (1)$$

where r is the radius of the interstitial, γ is the surface energy of an interstitial, E_{SFE} is the stacking fault energy of the crystal, G is the shear modulus and b is the Burgers vector of the dislocation that bounds the faulted loop. Since a large number of interstitials are involved in the formation of a loop, the first term in equation (1) generally dominates, leading to clustering. The faulted loops may grow further by the absorption of interstitials and unfault into perfect dislocation loops to minimize the energy of the system [1, 23, 27, 28]. These loops are referred to as microdefects in silicon. Vacancies could also cluster together into either dislocation loops or voids [29].

deKock [30] has identified two types of microdefects, termed A- and B-swirl defects, in as-grown float zone (FZ) silicon crystals. Figure 2 shows the distribution of A and B swirls revealed by X-ray topography of a transverse FZ silicon slice. A-type defects are absent in the peripheral region that is ~2 mm wide, but B swirls are still present. In longitudinal sections of FZ crystals, swirls are distribu-

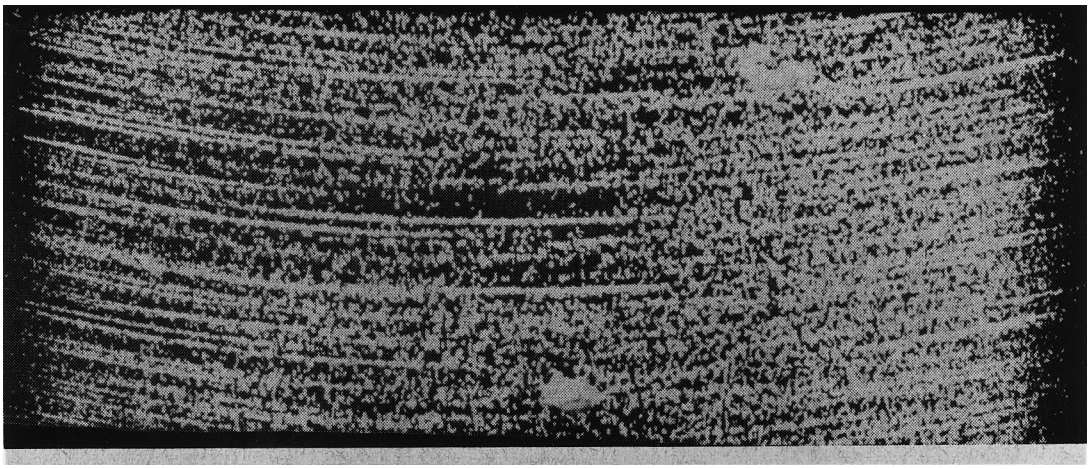

Fig. 3. X-ray topograph of longitudinal section of a lithium-decorated, dislocation-free float zone silicon crystal. After deKock [31].

ted in a striated pattern as shown in Fig. 3. This pattern resembles that of impurity striations observed in as-grown crystals [23]. This result is understandable if we assume impurities serve as heterogeneous nucleation centers for the swirls.

Transmission electron microscopy studies have shown that A swirls are perfect prismatic dislocation loops, interstitial in character [27, 28]. A typical example of an A swirl is shown in Fig. 4. B swirls have not been unambiguously identified. Furthermore, the distributions of microdefects in FZ and CZ crystals are very similar [31].

The formation of swirls can be suppressed by imposing either low [32] or high pulling rates [30, 31]. These effects are illustrated in Fig. 5. When the growth rate is low, the supersaturation of point defects may not occur because they may have enough time to migrate to various sinks. However,

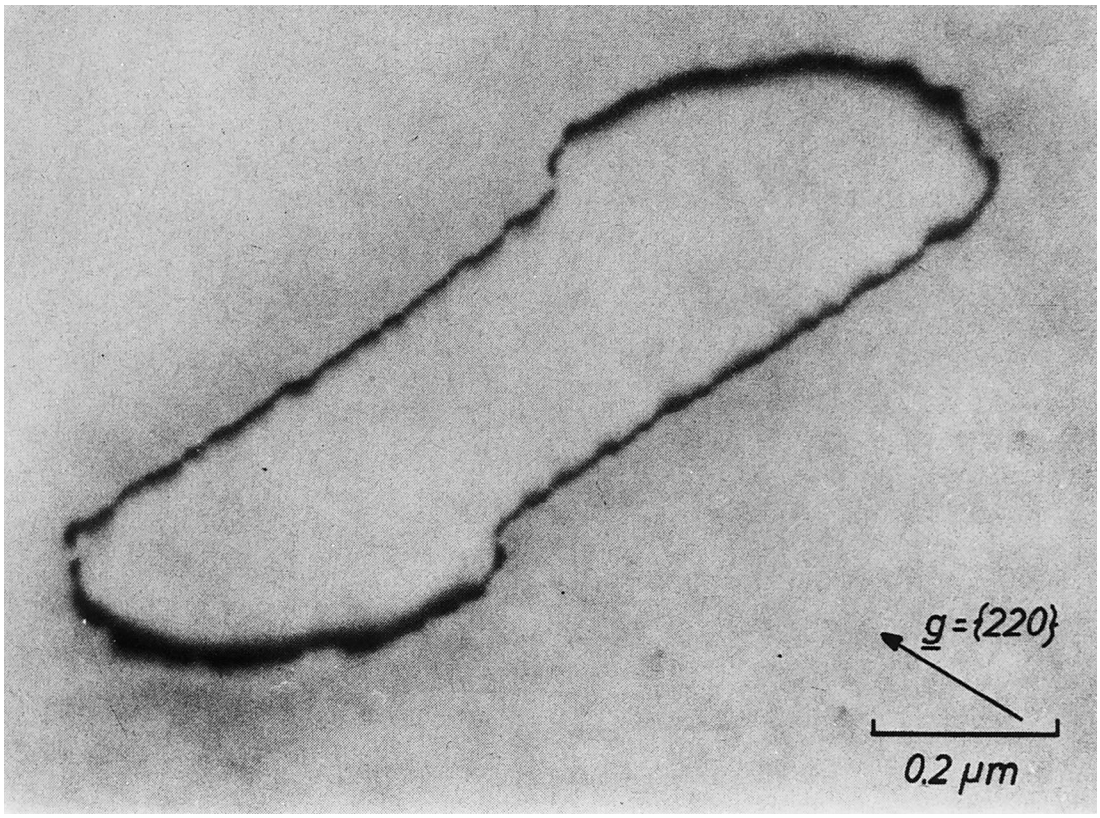

Fig. 4. Micrograph showing detailed nature of an A-swirl defect. After deKock [31].

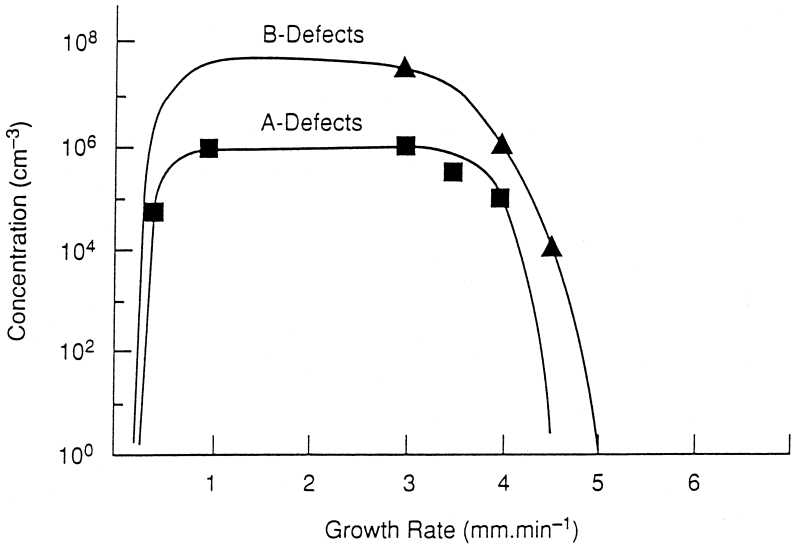

Fig. 5. The influences of growth rate on the concentrations of A- and B-swirl defects in float zone silicon. After deKock [31].

at higher growth rates the concentrations of point defects will exceed the equilibrium values, but they may not have enough time to cluster to form microdefects.

Thermal-gradient-induced stresses are a major source of dislocations in III–V crystals [1, 23, 33]. Dislocations resulting from the condensation of point defects may undergo multiplication, resulting in highly dislocated crystals. Figure 6 shows the etch-pit distribution observed on the (001) plane of

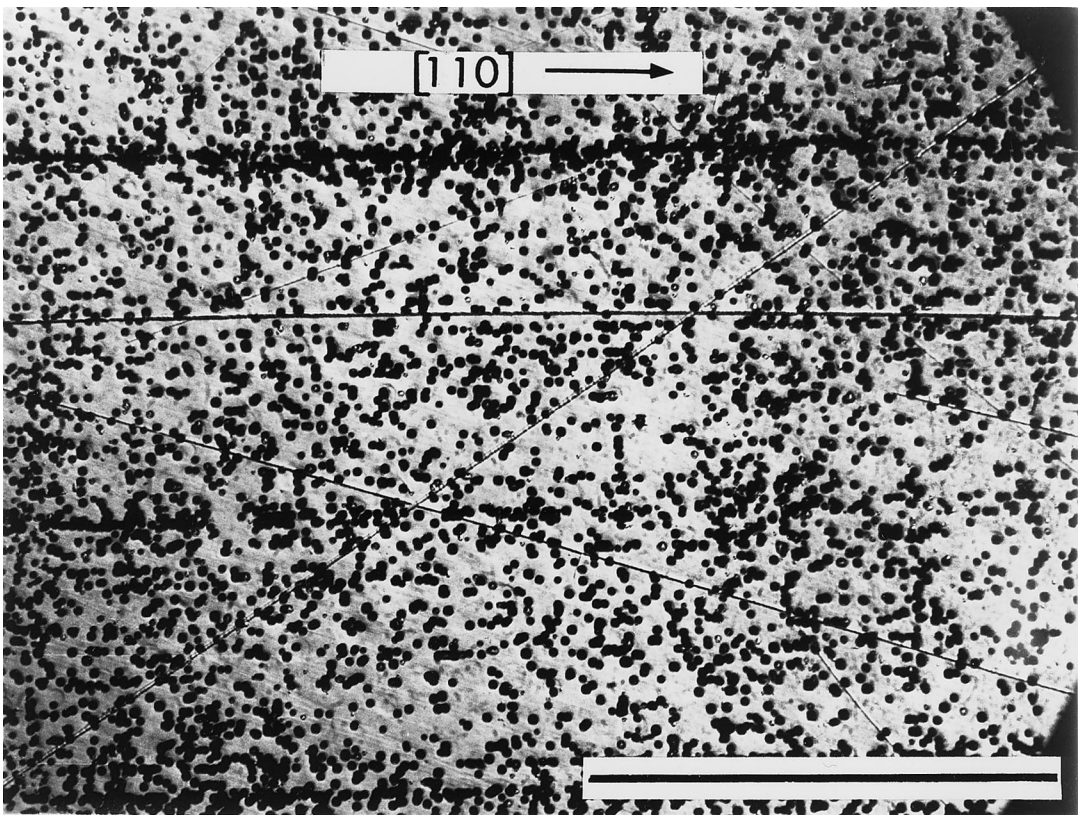

Fig. 6. Dislocation etch-pit distribution observed on a (001) slice of highly dislocated sulfur-doped InP wafer. Marker represents 0.1 mm. After Mahajan [1].

a highly dislocated InP crystal [1]. The observed alignment of etch pits along the [110] and [1$\bar{1}$0] directions is consistent with the idea that dislocations are slip induced.

One approach to grow crystals of compound semiconductors with lower dislocation densities is to reduce the magnitudes of the thermoelastic stresses to levels where $a/2\langle 1\bar{1}0\rangle\{111\}$ slips are not activated. This stress level is very difficult to achieve because yield stresses of compound semiconductors at high temperatures are very low [34–36]. So the accepted approach is to strengthen the matrix by the addition of impurities [37–39]. These impurities can be either isoelectronic in nature or act as dopants in the host lattice.

When an impurity is added to a tetrahedrally coordinated crystal, the bond lengths in the tetrahedron either increase or decrease depending on the covalent tetrahedral radius of the impurity. For example, consider the replacement of some of the gallium atoms by the indium atoms on the group III sublattice of GaAs. Ehrenreich and Hirth [40] visualize that this substitution could lead to tetrahedral units consisting of an indium atom bonded to four arsenic atoms, i.e. InAs(4), within the GaAs matrix. Since the In–As bond length is greater than the Ga–As bond length, the volume of the InAs(4) tetrahedral unit is larger that that of the GaAs(4) unit. Therefore, the formation of InAs(4)As units produces distortions in the lattice, causing strengthening. As a result, the probability of dislocation multiplication under the influence of thermal-gradient-induced stresses is reduced, yielding more perfect crystals.

The situation is much more complicated when an impurity can also act as a dopant in the host lattice. In addition to the size effect discussed above, electronic effects become significant. The ionized dopant atoms could interact with charged point defects as discussed in Section 2 and this could prevent them from clustering into potential dislocation sources. The work of deKock *et al.* [41] on microdefect formation in CZ silicon indicates that the point defect–dopant interaction is electronic in nature and does not depend on the size of the dopant atom. A similar situation could exist in compound semiconductors.

3.2. Epitaxial layers

The sources of defects in epitaxial layers can be broadly split into two different categories: growth-process-independent and growth-process-dependent [1, 23]. The respective examples are threading dislocations and hillocks observed in III–V epitaxial layers grown by organometallic vapor phase epitaxy.

3.2.1. Growth-process-independent defects

3.2.1.1. Threading dislocations. Dislocations present in the underlying substrate constitute the major source of dislocations in homoepitaxial and lattice-matched heteroepitaxial layers [1]. We can comprehend this result if we treat the substrate in epitaxial growth and the seed in crystal growth as equivalent. As discussed in Section 3.1, dislocations terminating at a substrate surface and whose Burgers vectors are either inclined or parallel to the surface will be replicated into the overgrowth. Insofar as threading dislocations are concerned, their density in the epitaxial layer will be equal to that in the substrate. It is therefore important that the bulk crystals should contain as few dislocations as possible, i.e. the crystals should be highly perfect.

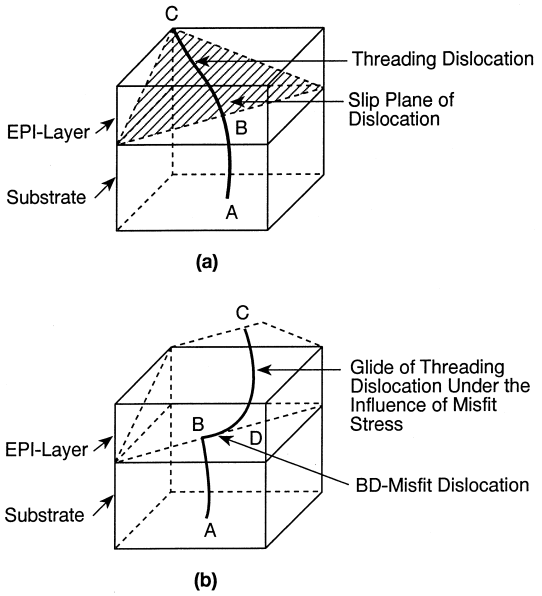

Fig. 7. Schematic illustrating how the glide of (a) a threading dislocation ABC under the influence of misfit stress leads to the formation of (b) a misfit dislocation BD that lies along the line of intersection of the glide plane within the layer with the substrate surface. After Matthews [42].

3.2.1.2. Misfit dislocations. When misfit between the epilayer and the underlying substrate exceeds a critical value, misfit dislocations are observed at the epi–substrate interface. We can show that if the unconstrained lattice parameters of the substrate and the epilayer are, respectively, a_1 and a_2, the separation (S) between the geometrically necessary misfit dislocations is given by [1]

$$S = (a_2 a_1)/(|a_2 - a_1|). \tag{2}$$

The linear density ρ of the misfit dislocations, i.e. the number per unit length, is given by [1]

$$\rho = (|a_2 - a_1|)/(a_2 a_1). \tag{3}$$

The above discussion assumes a linear misfit and could be extended to a two-dimensional situation.

An interesting question is how do these misfit dis-

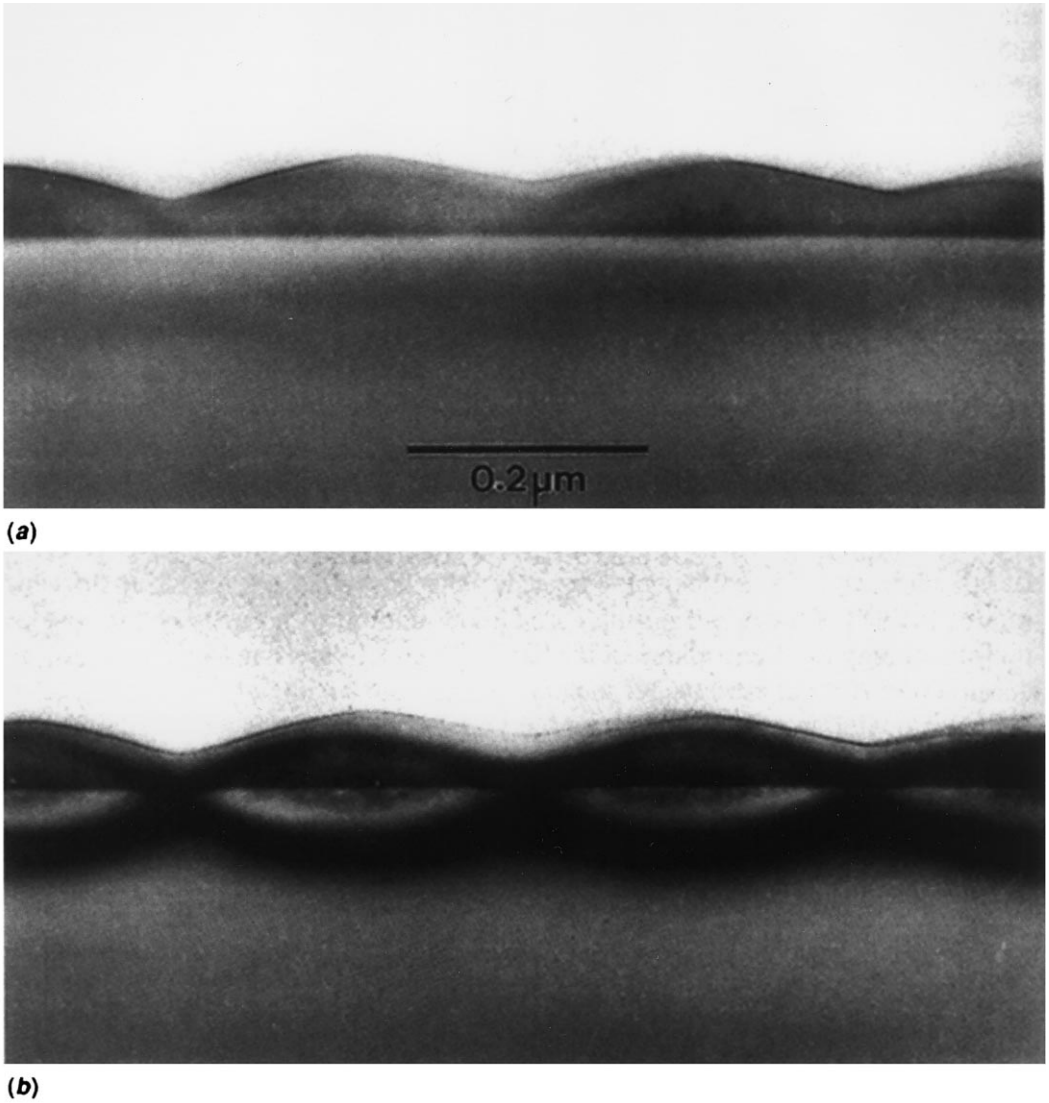

Fig. 8. Undulations observed on the surface of a silicon–germanium layer grown on (001) silicon under different operating reflections: (a) only undulations are visible, and (b) both undulations and strain contrast are seen. After Cullis *et al.* [43].

locations form? A model proposed by Matthews [42] is schematically shown in Fig. 7. He envisages that when the epilayer reaches a critical thickness, a threading dislocation BC in the layer undergoes glide, resulting in a misfit dislocation BD that lies along the line of intersection of the glide plane in the epilayer with the substrate surface. If the length of the threading dislocation is l, the stress required to glide BC is given by Gb/l, where G is the shear modulus and b is the Burgers vector of the dislocation. Initially, l is very small. Therefore, the stress required for the glide of BC is very high. As the layer thickens, this stress is reduced. Dislocation BC would begin to glide when the resolved component of the misfit stress in the glide plane and its glide direction exceeds Gb/l.

Matthews' model can adequately explain the origin of misfit dislocations in slightly mismatched systems when layers are grown on dislocated substrates. This situation may not be realized in some cases, for example during the growth of SiGe layers on macroscopically dislocation-free silicon substrates. We find that initially SiGe layers grow pseudomorphically in a planar fashion [43]. However, with additional growth nonplanar morphology develops that is shown in Fig. 8 [43]. In Fig. 8(a) the surface undulations are visible, but not the associated strain. However, both features are observed in Fig. 8(b). These undulations are caused by elastic distortions of the growing surface and relax elastic stresses within the heterostructure [43]. The nucleation of dislocation loops in the compressive regions of the undulations and their subsequent

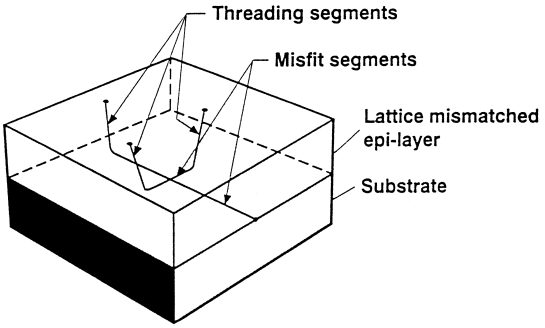

Fig. 9. Schematic showing formation of misfit dislocations by the glide of half-loops. After Xie *et al.* [49].

glide to the layer–substrate interface leads to plastic relaxation [44].

The situation in large lattice mismatched systems, such as Ge/Si, GaAs/Si, GaSb/GaAs and GaN/sapphire, is much more complex because the growth nucleates in the form of islands. For example, in the GaSb/GaAs system both 90° and 60° $a/2\langle 110\rangle$ misfit dislocations are seen [45]. The relative preponderance of the two types of dislocations depends on the growth temperature. The 90° dislocations dominate at lower growth temperatures and could nucleate at the island edge–substrate interface [45], whereas the 60° dislocations could nucleate from steps present on the surfaces of islands. Results of LeGoues *et al.* [46] and Eaglesham and Hull [47] on the Ge/Si system can be rationalized in a similar fashion. Furthermore, the difference in island shape could be responsible for the introduction of 90° and 60° misfit dislocations.

As discussed earlier, the substrate dislocations are primarily responsible for threading dislocations in lattice matched systems. The question is how do threading dislocations form in lattice mismatched systems? They could evolve in two ways [48]. First, if the strain relaxation occurs by the nucleation of dislocation loops from surface steps, the inclined segments of the gliding loops will be left as threads in the layer. Second, threading dislocations could form during the coalescence of islands [45, 48].

Depending on the mismatch the density of threading dislocations may vary between 10^6 and $10^{10}/\text{cm}^2$. These values are high for reliable minority carrier devices [1]. Therefore, we need to reduce the density of threading dislocations. Several schemes have been proposed to lower the density of threading dislocations in lattice mismatched layers: (i) graded buffer layers [49], (ii) growth on compliant substrates [50], and (iii) lateral epitaxial overgrowth [51]. For the sake of conciseness, we will only discuss the first approach. The reader is referred to the listed articles for details on others.

To explain the conceptual framework of the graded buffer layer scheme, we will imagine the growth of material B on substrate A. For the sake of simplicity we will assume A and B have lattice mismatch, but have the same crystal structure. In this growth approach, the composition of the layer is either uniformly or step graded from A to B. As a result, the strain energy builds up gradually in the layer. When the strain energy reaches a critical value, dislocation loops could nucleate from surface steps. The glide of these loops could relax the misfit stresses. Since the mismatch is small, a few dislocation loops are required to relax it. Therefore, the side segments of the loops could glide over long distances, resulting in long lengths of misfit dislocations and a few threading dislocations. This situation is schematically illustrated in Fig. 9 [49]. During additional growth, these processes will be repeated at various levels in the layer, resulting in misfit dislocations that are distributed over the layer thickness. This assessment is consistent with the results of Xie *et al.* [49].

In the ungraded growth of B on A, the strain energy buildup is very rapid. Therefore, at a critical thickness a large number of loops must nucleate simultaneously to accommodate the mismatch. These loops can only glide over short distances, but they produce the same total length of misfit dislocations as in the case of the graded buffer layer. Therefore, we reckon that the total length of misfit dislocations in the two cases is the same, a feature of the mismatch between A and B, but the threading dislocation density is much lower in the graded buffer layers.

3.2.1.3. Stacking faults and twins. Stacking faults and twins in epitaxial layers can form in two ways: (i) by growth accidents on facets of islands, and (ii) by misfit stress-induced deformation. In both cases faults and twins lie on {111} planes and are bounded by $a/6\langle 11\bar{2}\rangle$ partials. The recent study of Narayanan *et al.* [52] has shown that stacking faults and twins observed in GaP layers grown on (001) silicon substrates are caused by the presence of {111} facets on GaP islands.

The formation of misfit-induced stacking faults and twins in heteroepitaxial layers is easier to understand. In the case of the diamond-cubic and zinc-blende structures, $a/2\langle 110\rangle$ dislocations could dissociate into two Shockley partials. Under the influence of the misfit stress, one partial can glide toward the surface and generate a stacking fault while the second partial stays at the interface and accommodates a portion of the misfit.

3.2.2. Growth-process-dependent defects. Certain types of macroscopic "defects" in epitaxial layers are specific to a particular growth technique. This is not surprising because the underlying approach and the conditions prevailing at the growth interface in each growth technique are different. We have chosen two examples to highlight the relationship between the origins of defects and the prevailing growth conditions: (i) formation of hillocks during

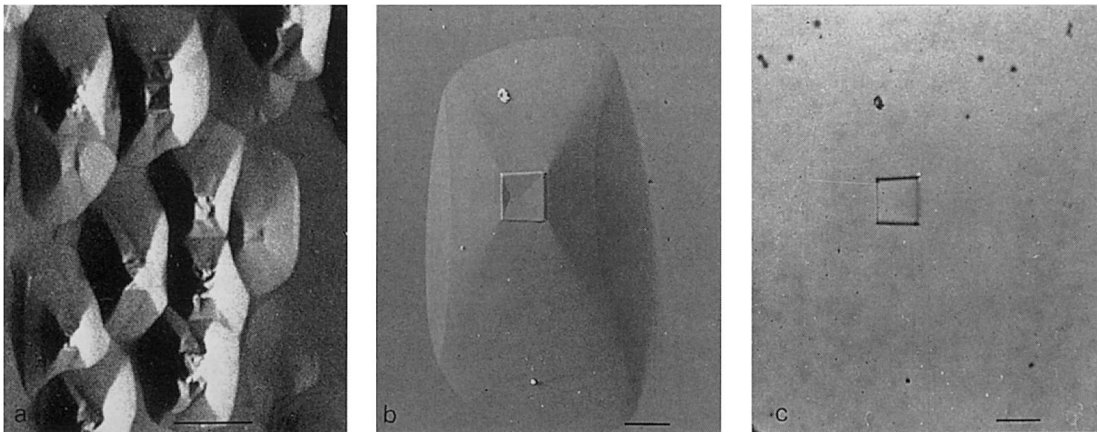

Fig. 10. SEM images of rectangular hillocks observed in InP layers: (a) overview, and (b), (c) secondary electron and EBIC images, respectively, of an individual hillock. After Gleichmann *et al.* [53].

vapor phase epitaxy, and (ii) evolution of oval-shape defects during molecular beam epitaxy.

3.2.2.1. Hillocks. Figure 10 is reproduced from the study of Gleichmann *et al.* [53]. Figure 10(a) shows SEM images of rectangular hillocks observed in a (001) InP homoepitaxial layer grown by organometallic vapor phase epitaxy. The secondary-electron image of one of the hillocks depicted in Fig. 10(b) reveals its topology and the presence of stacking faults. The electron-beam-induced-current image shown in Fig. 10(c) indicates that the faults are electrically active. Transmission electron microscopy examination of the hillocks has shown that the hillocks are highly defective regions and consist of dislocations and stacking faults. These results are quite generic.

An interesting question concerns the origin of these defective regions. Based on their results on the homoepitaxial growth of CdTe, Snyder *et al.* [54] have suggested that nucleation centers for hillocks may be produced by the clustering of tellurium atoms. We reckon that a similar situation may arise in the growth of InP discussed above. The presence of these clusters may lead to local defective growth consisting of dislocations and stacking faults. Since these defects can accentuate growth, hillocks may form.

3.2.2.2. Oval defects. A number of investigators [55–58] have observed macroscopic "defects" in molecular beam epitaxial layers that are in the shape of an oval, and are thus termed "oval defects". A typical example, reproduced from the work of Bafleur *et al.* [56], is shown in Fig. 11. They have reported that the ovals consist of dislocations, stacking faults, twins and polycrystalline regions.

The evidence to date tends to indicate that group III metal droplets may be responsible for the formation of oval defects [55]. Figure 12 shows schematically a generic model for the evolution of oval defects from liquid droplets [59]. Figure 12(a) shows a group III metal droplet on a (001) surface of a III–V semiconductor. The droplet will dissolve the underlying substrate to produce a dissolution pit

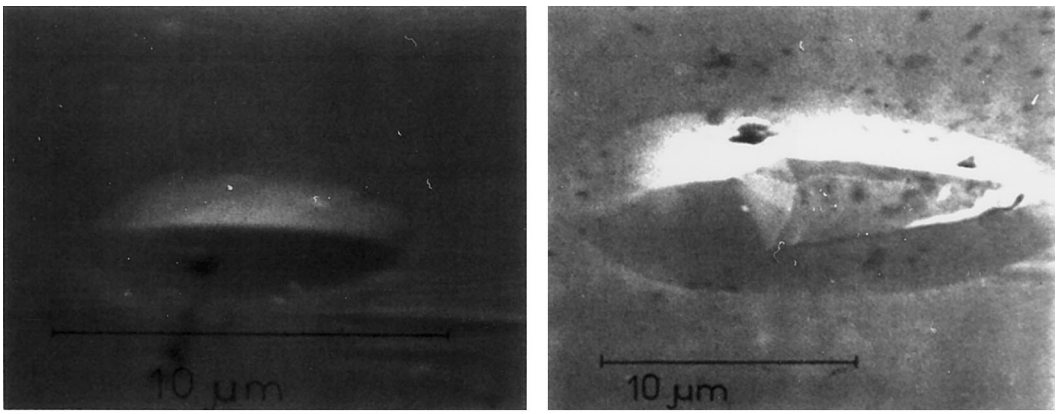

Fig. 11. Scanning electron micrographs showing oval defects on the surface of a (001) GaAs homoepitaxial layer grown by molecular beam epitaxy. After Bafleur *et al.* [56].

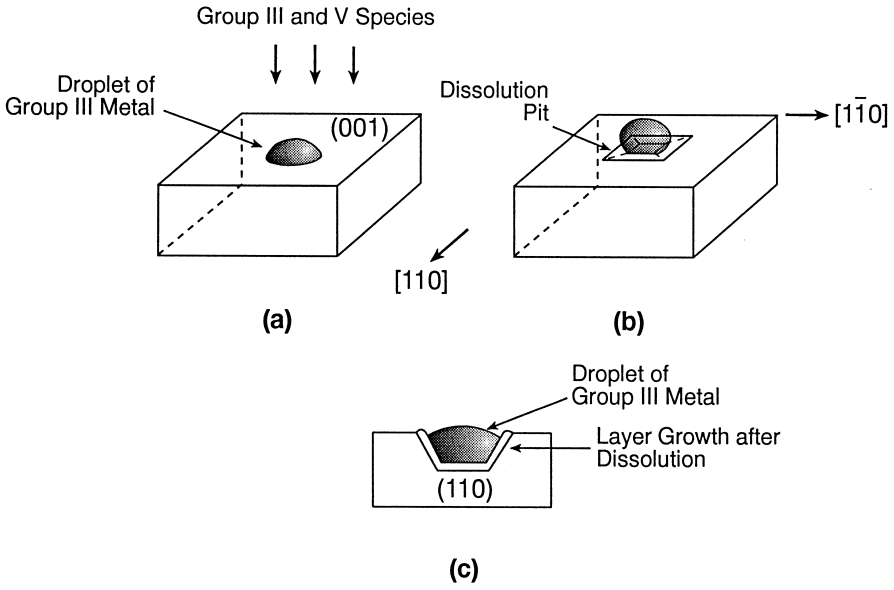

Fig. 12. Schematic showing the formation of an oval defect during the growth of a III–V homoepitaxial layer by MBE: (a) a group III metal droplet on a (001) III–V substrate, (b) a pit resulting from the dissolution of the substrate, and (c) epitaxial growth on exposed $\{111\}_{III}$ and $[\bar{1}\,\bar{1}\,\bar{1}]_V$ facets and (001) plane in the presence of group V flux could result in an oval defect. After Mahajan [59].

which is bounded by $\{111\}_{III}$ and $\{\bar{1}\,\bar{1}\,\bar{1}\}_V$ planes as shown in Fig. 12(b) [1, 23]. This equilibrates the activities of group V species in the droplet and the semiconductor In addition, the pit is asymmetric because, in the presence of the group III droplet, $\{\bar{1}\,\bar{1}\,\bar{1}\}_V$ planes are removed at a faster rate than $\{111\}_{III}$ planes. Concomitantly, the droplet is exposed to group III and V species required to grow the layer. These group V species may diffuse through the droplet and combine with group III species to form a III–V layer which deposits epitaxially on the pit facets, Fig. 12(c). Alternatively, polycrystalline semiconducting regions may form on the droplet surface through which group V species must diffuse. If the growth ceases before the droplet is completely converted into the semiconductor, polycrystalline and twinned regions may form during the cool down, resulting in an oval defect.

4. EFFECTS OF DEFECTS OF DEVICES

Defects have a dramatic effect on the performance of minority carrier devices, such as solar cells, light emitters, bipolar transistors, photodetectors, etc., whose action is governed by the migration of minority carriers. The carrier traps associated with point defects, dislocations, partials bounding stacking faults and grain boundaries reduce the minority carrier lifetime as well as their diffusion length, and thus the device behavior is significantly affected. On the other hand, the effects of defects on the performance of the majority carrier devices, such as metal-oxide-semiconductor field-effect transistors, are not that dramatic.

We have chosen two examples to highlight the effects of defects on devices: (i) the influence of dislocations on current (I)–voltage (V) characteristics of InP photodiodes, and (ii) the role of dislocations in the degradation of GaAlAs/GaAs light emitters. Figures 13(a) and (b) show the reverse bias I–V characteristics of InP diodes containing different dislocation densities fabricated on Fe- and S-doped substrates, respectively [60]. The diodes were produced by the diffusion of Cd into n-type InP layers. When the dislocation density is increased from $2.2 \times 10^7/cm^2$ to $1.5 \times 10^8/cm^2$, the breakdown voltage is substantially reduced; and at a given reverse bias, the leakage current dramatically increases. Since these diodes were fabricated by diffusion, Beam *et al.* [60] envisage that space charge cylinders develop around the dislocations. At higher dislocation densities these cylinders may begin to overlap and thereby produce high-leakage currents.

Threading dislocations play an important role in the rapid degradation of GaAlAs/GaAs lasers. Figure 14 shows scanning electron microscope images of non-luminescent regions observed in degraded GaAlAs/GaAs lasers [61]. These regions are labeled as DLDs (for darkline defects) in Fig. 14 and are oriented along the ⟨100⟩ and ⟨110⟩ directions in the active region. The dark spot defects (DSDs) on the figure have been attributed to the migration of the contact metal into the device [61]. When we examine DLDs by transmission electron microscopy, we observe that they evolve from the

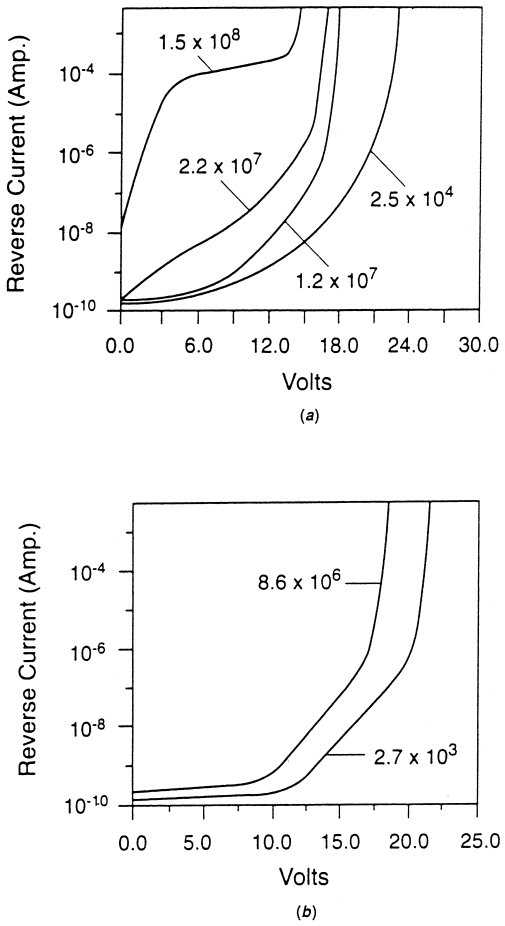

Fig. 13. Reverse *I–V* characteristics of InP diodes containing different dislocation densities fabricated on (a) Fe-doped and (b) S-doped substrates. After Beam *et al*. [60].

existing threading dislocations. We envisage that during the laser operation, dislocations in the active layer undergo nonradiative, recombination-enhanced glide and climb, resulting in the observed structures.

For a given dislocation density, the light-emitting devices containing InGaAsP active layers appear to be more degradation resistant than the GaAlAs devices. Mahajan [1] has argued that since InGaAsP layers are phase separated and atomically ordered, the multiplication of dislocations by non-radiative, recombination-enhanced glide and climb is difficult. This example suggests that in addition to defects, microstructures of mixed active layers could affect the performance and reliability of devices.

5. SUMMARY

1. Four types of defects are possible in semiconductors. These defects are electrically active.
2. The sources of dislocations in bulk crystals are: dislocations in seed crystals, excess point defects and thermal gradient-induced stresses. Necking of the crystal after seeding and addition of dopants or isoelectric impurities have been used to lower the dislocation densities.
3. The sources of defects in epitaxial layers can be classified into two categories: growth-process-independent and growth-process-dependent defect. The graded buffer layer approach that is used to reduce threading dislocations in lattice mismatched layers is discussed.
4. Defects have dramatic effects on the performance and reliability of minority carrier devices. These effects are discussed using a couple of examples.

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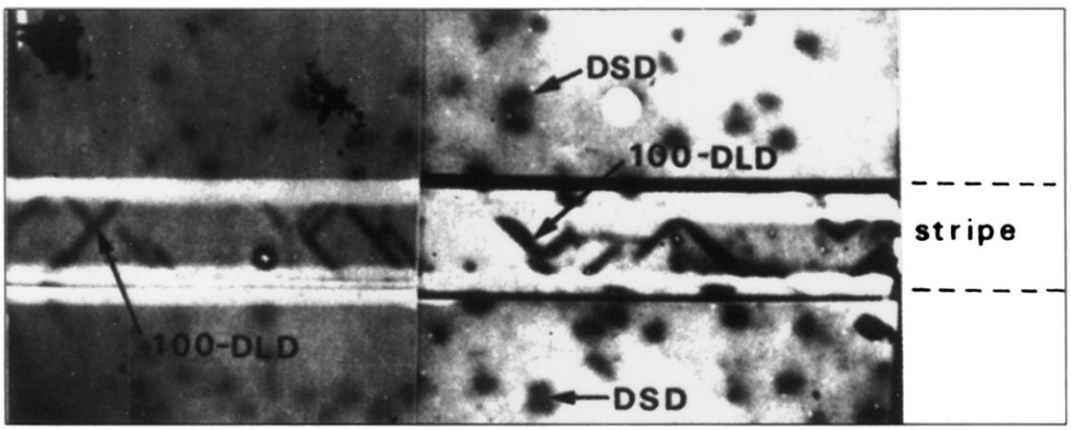

Fig. 14. SEM images of degraded GaAlAs/GaAs lasers. ⟨100⟩ and ⟨110⟩ DLDs appear with the active laser stripe. Many DSDs appear outside the stripe. After Ishida and Kamejima [61].

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