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Investigation of nano patches in Ni/n-Si micro Schottky diodes with new aspect

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ABSTRACT

High-quality Ni/n-Si Schottky barrier diodes (SBDs) with low reverse leakage current were produced using a molybdenum (metal) mask. An identical preparation of the diodes shows a diode-to-diode variation in the ideality factor and barrier height parameters. Topological, phase and potential distribution investigations of the surface before and after preparation of the thin metal film for ohmic and Schottky contacts with a Conducting Probe Atomic Force Microscope (CP-AFM) show that thin metal film deposited on Ni/n-Si Schottky diode (SD) consists of many nano patches. Investigation of the patches in the ohmic contact side shows that these ohmic contacts also consist of nano patches in the range 20–40 nm with a variation in the potential distribution reaching about 1 V, resulting in different electrical behaviors in different regions of the contact surface. Even with sufficient care in the preparation and cleaning of the contact surface there is a potential difference of about 0.5 V between different parts of the semiconductor surface, which is one of the sources of different electrical behaviors of the substrate. These patches are sets of parallelly connected and electrically cooperating nano contacts with size between 20 and 40 nm. The barrier heights (BH) and ideality factor (n) are affected by the potential distribution on the surface. There is a spot field between the patches with different local work functions, which are in direct electrical contact with the surrounding patches. It is shown that in the real metal–semiconductor (MS) contacts, patches with quite different configurations, various geometrical sizes and local work functions are randomly distributed on the metal surface. The relation between ideality factor (n) and potential barrier height (BH) depends on the distribution of patches and their work functions.

1. Introduction

The most important feature characterizing a Schottky barrier diode (SD) is its barrier height (ϕ_B). The potential barrier height (BH) of the ideal Schottky diodes equals the difference in the work function of the metal (ϕ_M) and the semiconductor electronic affinity (χ_S)[1–3]. Several theories exist, which can explain only some of the experimental facts. So there is a need for new experiments, which may yield more insight into the mechanisms for determining ϕ_B. The spatial variation of barrier heights in the inhomogeneous Schottky diodes is described mainly by the Gaussian distribution function and the zero-bias barrier height vs. ideality factor for many Schottky barrier diodes. In the past, the Gaussian distribution of the barrier heights has been widely accepted to correlate with the experimental data [3–7]. Simulation studies on the I–V characteristics of the inhomogeneous diodes with a Gaussian distribution of barrier heights have similar results to those observed in

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the experimental data [8–11]. Analysis of the Schottky barrier diodes' *I–V* characteristics, based on the thermionic emission theory, usually reveals an abnormal decrease in the barrier height (ϕ_B) and an increase in the ideality factor (n) with decreasing temperature [12–14].

In a metal–semiconductor (M–S) close (near) contact, potential difference appears between the contact surfaces of the metal and semiconductor and the adjacent free surfaces of the metal and the semiconductor [15]. The electric field covers the entire semiconductor contact region, but additional electric field covers the outlying semiconductor contact region. When the contact surface width of the interface is several micrometers, the field caused by the limitedness of contact surface completely encompasses the entire contact region of the semiconductor. Furthermore contact area, including its outlying region, is always heterogeneous in this situation; because of the emissive heterogeneity in the contact outlying region of semiconductor an additional electric field appears. In such a narrow contact the basic and additional electric fields caused by the limitedness of the contact area and emissive heterogeneity have a combined effect, both on the potential barrier height formation and current transportation.

Theoretical and experimental data for the values of work functions received by different methods are collected for many chemical substances and chemical compounds (polycrystalline and monocrystalline) in Ref. [16]. Work functions values for elementary substances and chemical compounds are in the range of 2–6 eV. At the same time it is firmly established that the sides of the monocrystalline having various crystallographic orientations possess different values of work function. The difference in the work function depending on the crystallographic orientation is nearly 1 eV.

The existence of these patches is shown theoretically in Refs. [9,15,17], where their effects are mathematically analyzed on the electrical character of the diode. In these works, there have been good agreement between the experimental results and the theory of Tung. The development of atomic force microscopy (AFM) techniques for the surface investigation provides a qualitatively new level of investigations for the topology, structure and electro–physical properties of the free surface of semiconductors [18–25].

In Refs. [22–24] it has been shown that the additional electric fields on free surface of the metal–semiconductor exist up to 500 μm; this additional electric field will affect the electrical character of diodes. One of the effective parameter in deviation of the *I–V* curve with the Schottky–Mott model is the effect of an additional electric field and the interaction of patches with different work functions and the spot electric field produced between them.

2. Theory

An Inhomogeneous metal electrode surface is schematically presented in Fig. 1a. On the surface along the OX axis, seven patches with local work functions Φ_{M1}, Φ_{M2}, Φ_{M3}, Φ_{M4}, Φ_{M5}, Φ_{M6}, Φ_{M7} (Fig. 1b) are displayed. Under the condition $\Phi_{M1} > \Phi_{M2} < \Phi_{M3} > \Phi_{M4} < \Phi_{M5} > \Phi_{M6} < \Phi_{M7}$, variations of the local work functions along the OX axis are presented in Fig. 1c. We assume that in each patch the local work function remains constant. It is clear that such a constancy of the work function actually should not occur because the patches with different local work functions are in direct electrical contact with surrounding patches. As a result of different local work function in each patch a

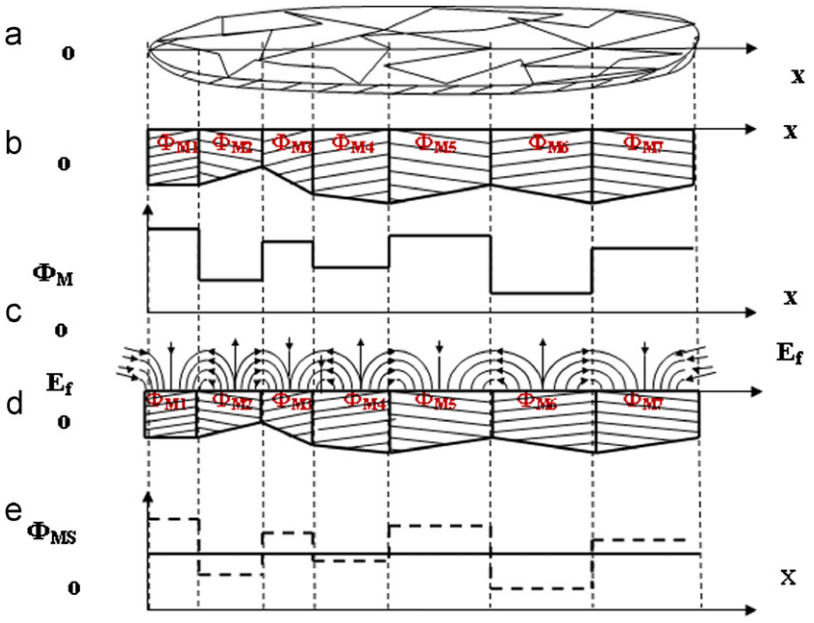

Fig. 1. (a) Schematic diagrams of inhomogeneous surface, (b) surfaces containing various microcrystals, (c) various local work functions, (d) local work functions along x axis and electric spot field E_f and (e) averaged work function.

potential difference between the surfaces of patches, the so-called electrostatic spot field E_f, is formed (Fig. 1d).

The direction of the spot field is such that it decelerates electrons emitted by the areas possessing smaller work functions but accelerates the electrons with larger work functions. So the average work function ($\overline{\Phi}_M$) remains constant along the OX axis (see a continuous line in Fig. 1e). In the absence of an external electric field, the total work function (Φ) required to remove the electron is identical for all parts of the surface and is determined by the following equation:

$$\overline{\Phi}_M = \frac{\int_s \Phi_M(s)\,ds}{A} \tag{1}$$

where A is the surface of the emitter, $\Phi_M(s)$ is the local work function of the individual surface and $\overline{\Phi}_M$ is the work function averaged over the total surface of diode.

The spot fields on the patches with small local work functions ($\Phi_M < \overline{\Phi}_M$) are almost the same as an external restraining field between the flat electrodes, and they reduce the current density emitted from those patches. On the contrary, they enhance the current density emitted from those patches with a large local work function ($\Phi_M > \overline{\Phi}_M$). Upon close contact of metal with the monocrystalline semiconductor, the spot field penetrates into the semiconductor and actively participates in the formation of potential barrier height and current transport. Details of this theory have been investigated in Refs. [15,18].

The current–voltage of the inhomogeneous Schottky barrier (SB) diode characteristic is described by [17] as.

$$I_{SB}^{inh} = AA^*T^2 \exp\left(-\frac{e\phi_{I-V}^{inh}}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right)-1\right] \tag{2}$$

where I_{SB}^{inh} is the total current of inhomogeneous Schottky barrier diodes, ϕ_{I-V}^{inh} is the inhomogeneous Schottky barrier height from the I–V curve at zero-bias, V is the applied voltage, T is the absolute temperature, k is Boltzmann's constant and e is the electron charge.

With n being an ideality factor serving as a measure of conformity of the diode to pure thermionic emission, the saturation current (I_s) is given by

$$I_S = AA^*T^2 \exp\left(-\frac{e\phi_{I-V}^{inh}}{kT}\right) \tag{3}$$

where A is the diode area and A^* is the effective Richardson constant, which is equal to 120 A/cm^2 K^2 for n-Si.

The barrier height can be obtained from Eq. (3) as

$$\phi_{I-V}^{inh} = (kT/e)\ln(AA^*T^2/I_s) \tag{4}$$

And the ideality factor can be obtained from Eq. (2) as

$$\frac{dV}{d\ln(I)} = n\frac{kT}{q} \tag{5}$$

The ideality factor, which accounts for the dependence of barrier height ϕ_{I-V}^{inh} on the applied voltage can be written as [9–19].

$$\frac{d\phi_{I-V}^{inh}}{dV} = 1-\frac{1}{n} \tag{6}$$

where $d\phi_{I-V}^{inh}/dV$ is the change in the barrier heights with the bias voltage. We assume that ϕ_{I-V}^{inh} is linear in applied voltage as approximated in Ref. [17] or equivalently

$$n = \frac{1}{1-d\phi_{I-V}^{inh}/dV} \tag{7}$$

If $d\phi_{I-V}^{inh}/dV$ is constant, the ideality factor should be constant. Eq. (7) is used to relate the ideality factor to the barrier heights. Linear relationship between barrier height and ideality factor has been confirmed theoretically [6,12,13,18,21] and experimentally [14,15]. Although the data between the barrier heights and ideality factors are randomly distributed or have a non-linear relationship, some authors have explained a linear relationship between barrier heights and ideality factors on the sets of identically prepared diodes [6,12,21].

Barrier height can be calculated by capacitance–voltage (C–V) measurements. C^{-2} is plotted against the applied voltage. From the intercept on the voltage axis, the barrier height is determined. C^{-2} is related to voltage by

$$C^{-2} = 2(V_{bi}-V-kT/q)/q\varepsilon_s N_D \tag{6}$$

where N_D is the n-Si donor's concentration, ε_s is the permittivity and V_{bi} is the built-in potential, which is equal to the voltage intercept V at $C^{-2}=0$. In this approach the barrier height is

$$\phi_{B(C-V)} = qV_{bi} + qV_n \tag{7}$$

V_n is the potential difference between the Fermi level and the edge of the conductance band in the neutral region of n-Si and can be calculated by knowing the carrier concentration N_D. V_n is given by

$$V_n = (kT/q)\ln(N_C/N_D) \tag{8}$$

3. Experimental details

n-type Si with B impurity and crystal direction of (1 1 1) with thickness of 275 ± 15 μm and resistivity of 4–11 cm was selected. The sample surfaces were polished. For cleaning the Radio Corporation of America (RCA) method was applied as follows.

For degreasing a mixture of DIH_2O, NH_4OH and H_2O_2 in the ratio of 1:1:5 was used to wash the surface for 10 min. To remove ion particles, the samples were dipped in a mixture of HCL, DIH_2O and H_2O_2 in the ratio of 1:1:6 for 10 min and then rinsed in double distilled water for 1 min. For deoxidization, the samples were dipped in DDH_2O, HF and H_2O_2 in the ratio of 1:50 for 5 sec and then washed with double distilled water for 1 min. For better cleaning of samples' surface, we used a plasma cleaner at a voltage of 1 kV for 20 min under pure Argon ions. For making ohmic contact we used high purity indium with an electron beam gun coating system model EMS-160 made by High Vacuum Technology Center (ACECR-Sharif University Branch-Iran). Indium has a low work function and it has a very good contact for connecting the ohmic n-type semi-conductors. Because of phase formation during coating, it creates non-smooth surface

on the substrate. Experiences have shown that the use of ceramic boats with deposition rate below 4 angstroms per second (Å/s) solved this problem. Deposition procedure was done immediately after cleaning the substrate by the RCA method. Rate of coating was 2 Å/s in a vacuum chamber of 5×10^{-5} Torr. The coating rate was monitored by quartz and the final deposition was 150 nm. After this stage the samples were annealed in an atmospheric controlled furnace with H_2 gas at 450 °C for 20 min. After ohmic contact, the sample surface was washed with acetone and distilled water and cleaned with a plasma arc cleaner. For making the Schottky contact we used the electron beam gun coating system at 4×10^{-5} Torr. We coated 120 nm Ni using circle masks with an area of 0.2 mm^2. *I–V* measurements were performed at room temperature using a commercial homebuilt *I–V* measuring unit containing a Keithley 4586 with a probe station. The barrier height and carrier concentration N_D were also calculated from the *C–V* characteristics at 1.0 MHz. For image measuring, we used the STM mode with 1 nm tunneling current. For this purpose we used DME AC-AFM with cantilever height 160 μm, width 45 μm, thickness 45 μm, force constant 42 N/m, resonance frequency f=285 kHZ and tip curvature radius ≥10 nm made from $PtIr_5$ materials.

4. Results and discussion

Topological, phase and potential distribution investigation of the surface before and after preparation with the CP-AFM shows that even with sufficient care in the preparation and cleaning of the contact surface there is a potential difference of about 0.2 V between different parts of the semiconductor surface, which is one of the sources of different electrical behaviors of the device. Tiny polycrystalline areas and microscopic impurities on the surface are one important reason for this difference, which are not detectable with the conventional equipment.

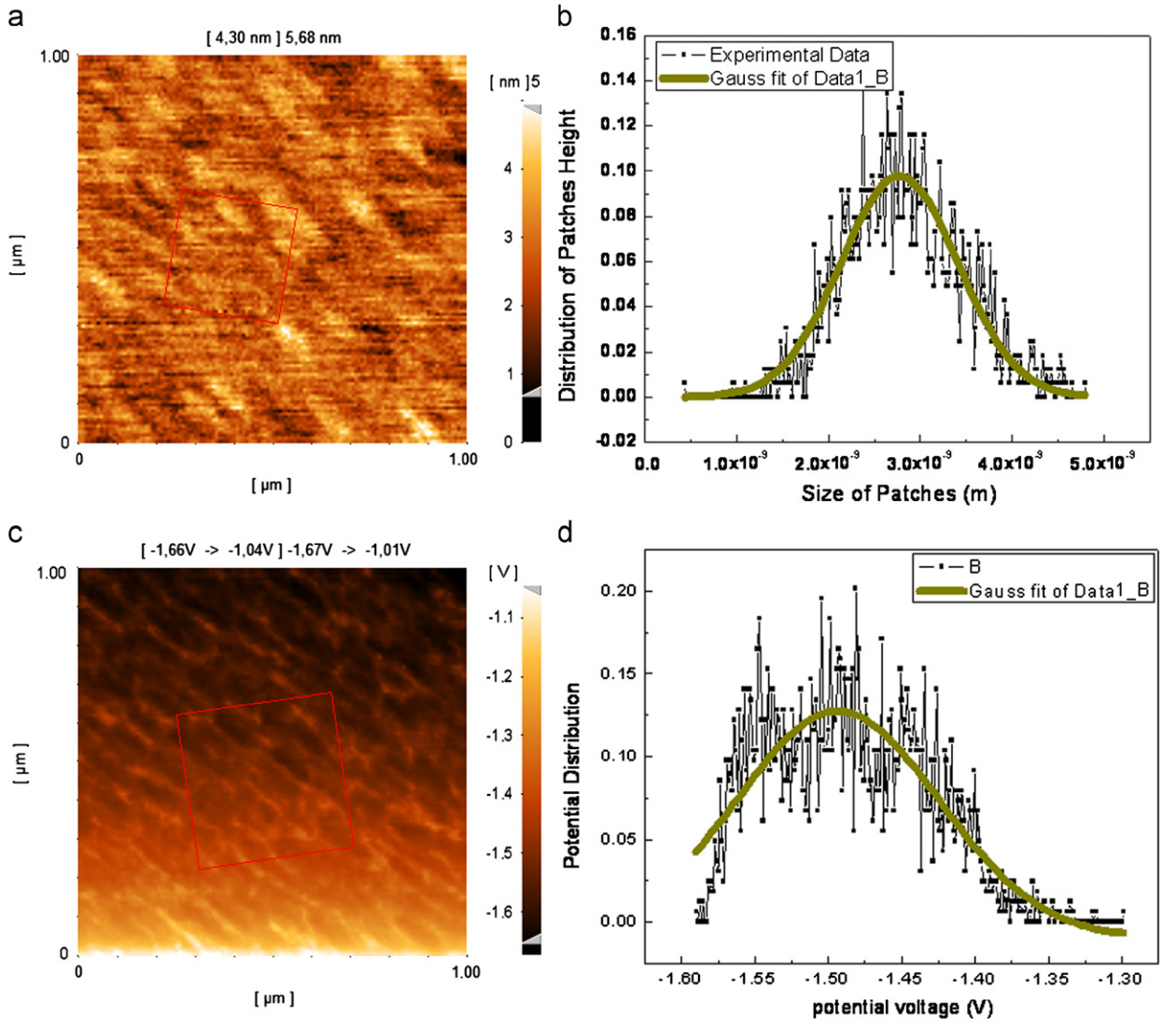

Fig. 2. (a) Topographic picture of surface after preparation and (b) random distribution of patches height. Average patch height is 3 nm. (c) The phase image and (d) potential distribution of the same surface as shown in Fig. 2b. Potential changes are in the range of 0.2 V.

Fig. 2a shows the AFM topology of the Si surface after the cleaning process. The average surface roughness is shown in Fig. 2b, which has been selected randomly as 16% of the area in Fig. 2a. By applying a Gaussian distribution function fit to Fig. 2b, we get the average patch heights as 3 nm. Fig. 2c shows the potential mapping (phase image) and Fig. 2d shows the potential distribution with a Gaussian fit. Potential changes are in the range of 0.2 V.

Investigation of the patches in ohmic contact side shows that these ohmic contacts consist of nano patches in the range of 20–40 nm with a variation in the potential distribution reaching about 0.5 Vt, resulting in different electrical behaviors in different regions of the contact surface. Fig. 3a shows an AFM image taken from the surface of indium. Grain sizes are in the range of 100–200 nm. Fig. 3b shows the phase image and Fig. 3c shows the potential distribution of the same surface. Investigation of the figures shows that the patches with the same work function have the same potential magnitude and the potential distribution in every patch is nearly Gaussian with its peaks at the center and decreases with increasing distance from the peak center, which is caused by the interacting spot field of the neighboring patches.

Topological, phase and potential distribution investigations of the thin Ni film deposited on n-Si Schottky diode (SD) shows many nano patches. With the help of (CP-AFM), it was shown that metal surface consist of nano patches in the range of 20–40 nm with a variation in the potential distribution reaching about 1 V; these patches are sets of parallelly connected and electrically cooperating nano contacts.

Fig. 4a shows the phase image and Fig. 4b shows the magnitude of voltage swept across 3 lines shown in Fig. 4a. In both current and phase image we clearly see that the variation in surface topography is in the range 50–100 nm and these variations are indicative of variations in BH and ideality factor.

In Fig. 5a the forward and the reverse bias currents vs. voltage of two randomly selected sample diodes are shown. As shown in this figure, the I–V characteristics exhibit a very good Schottky behavior. Fig. 5b shows C^{-2} vs. V plot of the Ni /n-Si contact at 1 MHz for 2 samples of devices.

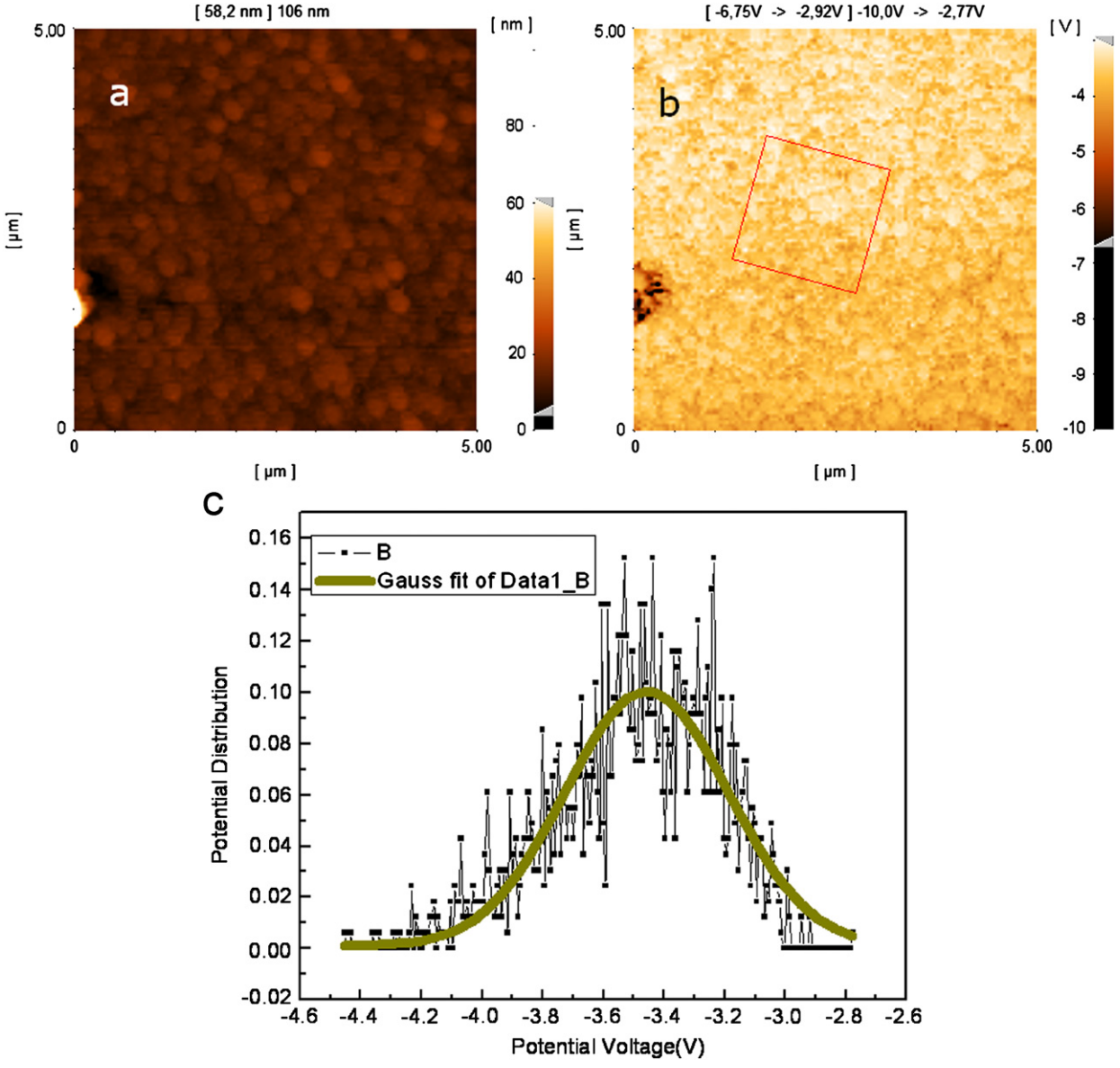

Fig. 3. (a) AFM image taken from the surface of indium. Grain sizes are in the range of 100–200 nm, (b) the phase image and (c) the potential distribution of the same surface. The potential distribution is in 1 V range.

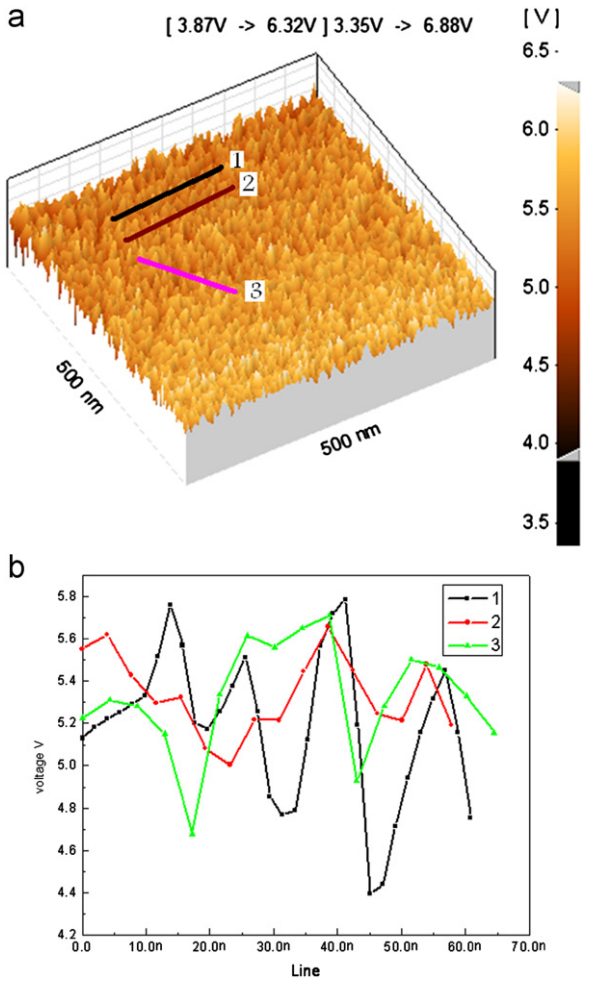

Fig. 4. (a) Phase image and (b) the magnitude of voltage (which is a function of phase variation) swept across 3 lines as in Fig. 4a. The variation in voltage is approximately in the range of 20–40 nm; the patches in different directions did not have the same size; however their average sizes are in the 30 nm range.

From these I–V characteristics and using Eqs. (4) and (5), we calculated the saturating currents, the effective barrier height and ideality factor for each contact. We obtained the saturating currents from $I_s = 2 \times 10^{-9}$ to 3.5×10^{-7} A. The value of the ideality factors (n) varied from $n = 1.1$ to 1.6, which was obtained from the slope of the linear region of the forward bias current–voltage characteristics and the barrier heights (Φ_B) were obtained from $\Phi_B = 0.513$ to 0.615 eV. The variation of barrier height obtained from I–V is attributed to various degrees of heterogeneity of contacts in measurements.

As one can see from Fig. 5b the C^{-2} vs. V plot is a straight line, whose intercept with the V axis gives the value of $V_{bi}v_{bi}$ is the potential difference between the Fermi level and the top of the valence band in the neutral region of n-Si and can be calculated from the carrier concentration N_D and is obtained from Eq. (7), which is $N_D = (1.35–1.5) \times 10^{16}$ cm^{-3}. Using Eq. (7), the barrier height calculated as $\Phi_{B(C-V)} = (0.714–0.726)$ eV.

Fig. 6a shows the current image and Fig. 6b and c shows the magnitude of two currents swept across two lines: line 1 inside contact and line 2 from inside contact toward the outside of the contact. The variation in current is approximately in the 100–200 nm range.

Fig. 7 shows the dependency of barrier height on ideality factor. As shown in Fig. 7 the dependency of ideality factor on the barrier height is linear. The formation of multi-crystallites with various patch sizes can be the main source of various BH.

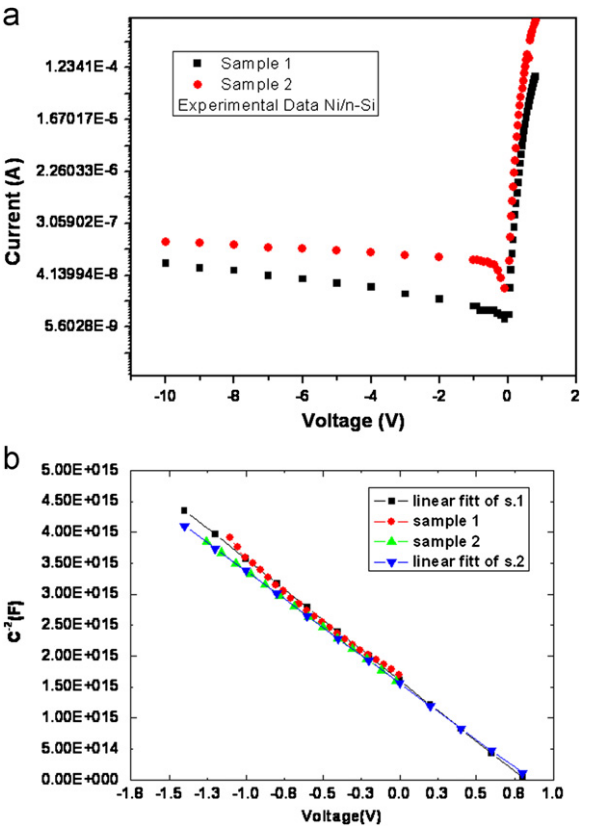

Fig. 5. (a) Forward and reverse bias currents vs. voltage characteristics of the Ni/n–Si structure at room temperature for three sample diodes (inset shows the diode array, the diodes are of the same diameter.) (b) C^{-2} vs. V plot of the 2 samples of devices at 1 MHz.

5. Conclusion

High-quality Schottky diodes were produced where their reverse leakage current was found to be low, thereby assuring a high quality rectifying behavior. Topology measurement of the surface of thin metal film with CP-AFM showed that Ni/n–Si Schottky diode (SD) consists of many different size patches. These patches are sets of parallelly connected and electrically cooperating nano contacts with size between 20 and 40 nm. Every individual patch acts as an individual diode with different characteristics. Between these individual diodes, there is a spot field distribution. It is verified that the patches with different local work functions are in direct electrical contact with surrounding patches, which results in an electrostatic spot field. Study shows that the potential distribution after surface preparation is not identical on the entire semiconductor surface. Potential change of semiconductor surface is one of the parameters affecting diode's characteristics. Investigations indicate that the differences in crystallography of coated metal, having different potential distributions, cause the current flow to have different behaviors.

So in real metal–semiconductor (MS) contacts, patches with quite different configurations, various geometrical sizes and local work functions are randomly distributed on the surface of metal; hence direction and intensity of spot field

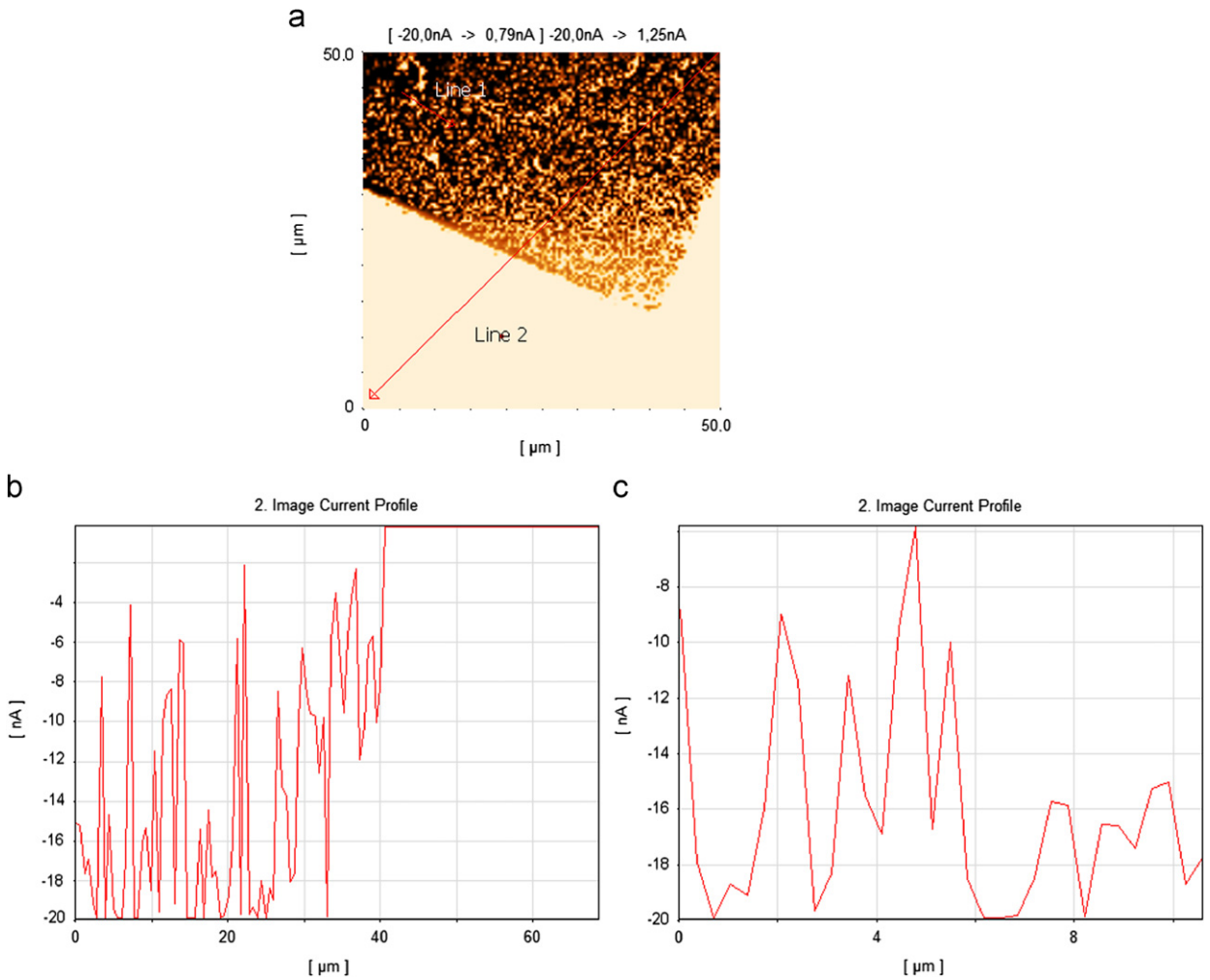

Fig. 6. (a) Current image and (b) and (c) magnitude of two currents swept across two lines 1 and 2. The variation in current is approximately in the range of 50–100 nm.

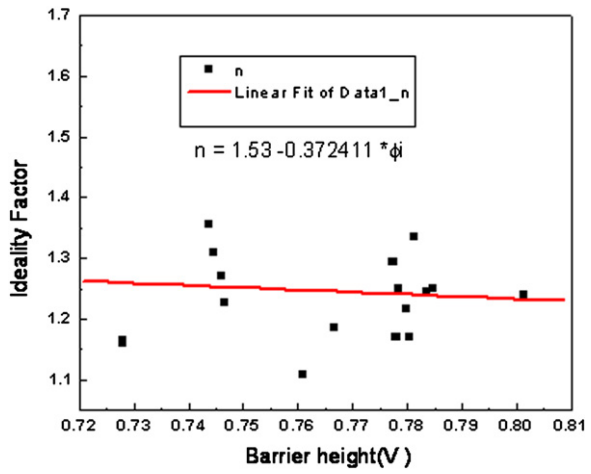

Fig. 7. Dependency of barrier height on ideality factor.

are non-uniformly distributed along the surface of metal. The topology of surface of thin metal film by the atomic force microscope (AFM) showed that there is a granular structure with sizes of approximately 20–40 nm, which means that Ni/n type Si SD consists of parallelly connected nano-contact diodes. Each of them has its own electrical characteristics. In a contact the potential differences, which consist of summation of potential difference, interaction of each individual patch with each other and peripheral electrical field, determines the effective potential difference of each contact. These will depend not only on the substrate material and the type of metalized material, but also on the surface preparation, method of coating and dimension of work piece.

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