Temperature dependence of the current in Schottky-barrier source-gated transistors

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The temperature dependence of the drain current is an important parameter in thin-film transistors. In this paper, we propose that in source-gated transistors (SGTs), this temperature dependence can be controlled and tuned by varying the length of the source electrode. SGTs comprise a reverse biased potential barrier at the source which controls the current. As a result, a large activation energy for the drain current may be present which, although useful in specific temperature sensing applications, is in general deleterious in many circuit functions. With support from numerical simulations with Silvaco Atlas, we describe how increasing the length of the source electrode can be used to reduce the activation energy of SGT drain current, while maintaining the defining characteristics of SGTs: low saturation voltage, high output impedance in saturation, and tolerance to geometry variations. In this study, we apply the dual current injection modes to obtain drain currents with high and low activation energies and propose mechanisms for their exploitation in future large-area integrated circuit designs. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4921114]

I. INTRODUCTION

A. Schottky barrier source-gated transistors (SB-SGTs)

Source-gated transistors (SGTs)[1–3] are formed by deliberately engineering a potential barrier at the source of a staggered-electrode thin-film field effect transistor (TFT). The depletion region which forms at the source barrier extends across the semiconductor layer when a small (usually below 2 V) reverse bias is applied to the drain, leading to source pinch-off and drain current saturation at significantly lower drain voltage in comparison to a conventional TFT. Figure 1(a) shows a schematic cross-section of a *n-type* SGT under positive gate and drain bias.

The source barrier is reverse biased, and as the reverse bias increases, the depletion envelope widens until all the negative charge at the drain end of the source is depleted. In this condition, the drain current is saturated, as any further increase in V_D is dropped across the depleted region and has little effect on the field and voltage distribution at the source barrier.[2,4] Regardless of the current injection mechanism at the source,[3,5,6] the intentional use of a source barrier in an otherwise conventional TFT structure leads to major differences in the transistor (output) characteristic: low-voltage saturation,[2,3,7–10] flat saturated output characteristics,[3,7,9,11] tolerance to geometrical variations,[4,12] bias stress stability,[13] and improved current levels in low mobility materials.[14] Both digital[15] and analog applications[14,16–19] could benefit from using these devices, in terms of amplification, energy efficiency, uniformity of electrical performance, and reliability. Figures 1(b) and 1(c) show, respectively, output and transfer characteristics measured on an *n-type* polysilicon SGT with Schottky source barrier. Note the low saturation voltage, flat characteristics, and exponential dependence of drain current on gate voltage above threshold and in saturation.

B. Temperature behavior of drain current in FETs and SGTs

The field and voltage distributions in a SGT are two-dimensional, and it is therefore difficult to find a simple analytical expression for the current for all geometries. A lumped circuit model is shown in Figure 1(d), but the value of each component can only be found using 2-D computer analysis. Essentially, there are two current sources, with different characteristics: I_1 is the current crossing the barrier in the high field (depleted) region at the drain end of the source; I_2 is the current crossing the source barrier in the low field region (bulk) of the source contact. A complication occurs because the low field current, I_2, can be restricted by the fully depleted region at the drain end of the source. This effect is the same as the action of a junction field-effect transistor (JFET).

The drain current is therefore determined by two mechanisms, and which one dominates is determined by device geometry, the source barrier height, and the gate biasing condition. For low barriers and long sources, we expect the current to be restricted by the JFET action and by the resistive path through the semiconductor in the bulk region of the source. For high barriers and short sources, the current should be determined by the field dependence of the barrier at the end of the source.[5]

All of these mechanisms are temperature activated, because there is a barrier, either at the source contact or at the JFET, which determines current flow, and we expect the general Arrhenius expression to be relevant

$$I_D \propto \exp\left(-\frac{q\phi_B}{kT}\right), \tag{1}$$

where ϕ_B is the effective barrier for carrier transport.

For a Schottky barrier source, the field dependence of the barrier height is determined by image force lowering and

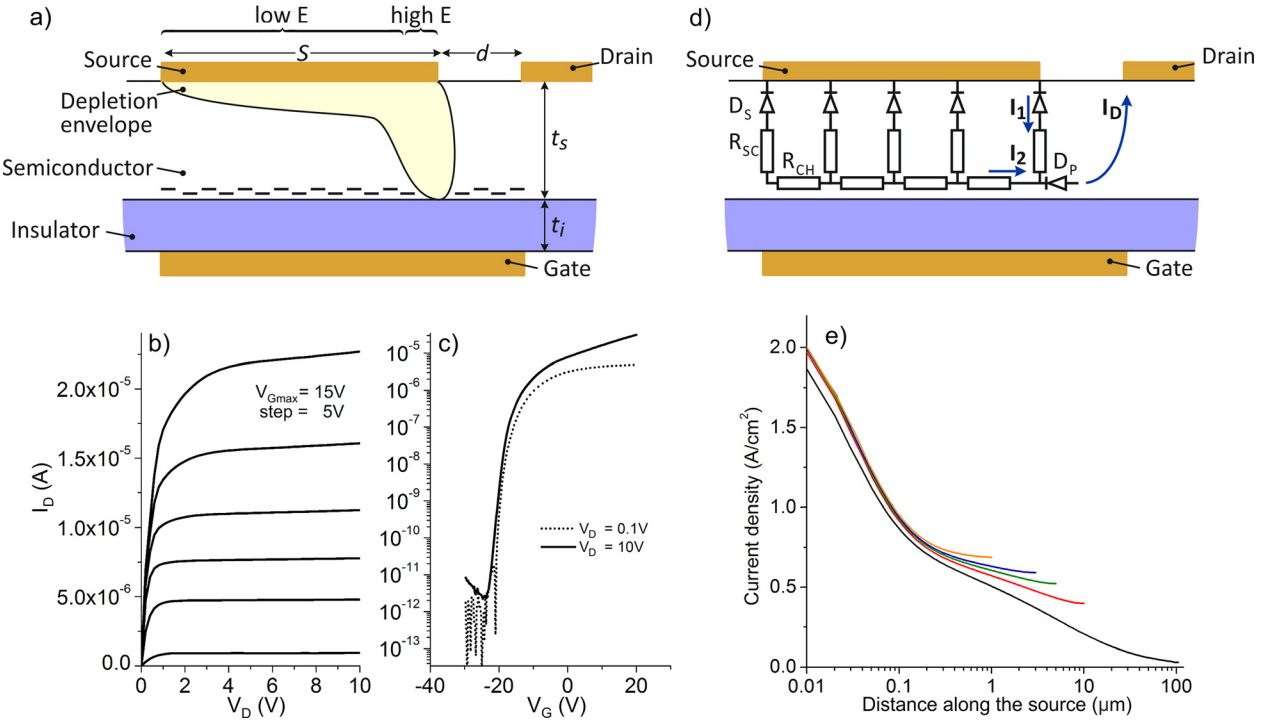

FIG. 1. (a) Schematic cross-section of an n-type bottom SGT under positive gate and drain biases, showing the envelope of the depletion region under the source; measured (b) output and (c) transfer characteristics of a polysilicon *n-type* SGT, fabricated as described in Ref. 7; (d) The same cross-section as (a) showing the distribution of current restriction elements within the semiconductor and at the source metal-semiconductor contact, along with the two distinct components of drain current (after Ref. 3); (e) simulated current density crossing the source-semiconductor interface at every distance along the source contact away from the edge closest to the drain, illustrating the decreasing current density with distance for long sources, as a result of the resistive network shown in (d).

quantum mechanical tunneling through the barrier.[20] It has been shown that when field E_S is high, the barrier lowering can be approximated by

$$\Delta\phi_B \approx \alpha E_s, \tag{2}$$

where α is an effective barrier lowering constant. A general equation for barrier lowering is

$$\Delta\phi_B \approx \alpha E^{\gamma} + \beta \frac{q}{4\pi\varepsilon_S} E^{0.5}, \tag{3}$$

where the first term is more accurate at high fields, and the second, more accurate at low fields.

From (1), the activation energy (E_A) for current transport is

$$E_A = -\frac{\partial(\ln I)}{\partial\left(\frac{1}{kT}\right)}, \tag{4}$$

where I is the current, k is Boltzmann's constant, and T is temperature.

Determination of E_A enables us to estimate the temperature coefficient of the drain current (TC) and its dependence on source length. Clearly, a low E_A leads to low temperature dependence. As a guide, for a 30 K increase above room temperature, $\Delta E_A = 30$ meV represents a doubling of current, and an order of magnitude increase has an associated ΔE_A of approximately 64 meV.

SGTs with high Schottky source barriers tend to have large positive TC. Crystalline MOSFETs have a small negative TC resulting from the increased phonon scattering at high temperature with an associated reduction in carrier mobility.[21] In a disordered-semiconductor thin film field effect transistor, this behavior is usually overcompensated by the change of carrier trapping with temperature, leading to a small, positive TC.[21] A large positive TC can be detrimental to circuit operation, first through the positive feedback potentially leading to catastrophic failure which might result as temperature is increased, and second in the unfavorable changes in electrical characteristics, which could necessitate compensation circuitry, complex designs, and larger design margins. In this study, we investigate means of controlling the TC of SGT drain current through leveraging of device-specific physics in their design.

II. SIMULATION SETUP

The structure was defined in Silvaco Atlas as a two-dimensional cross-section. For consistency with previous studies,[2–6,9,22] we analyzed an *n-type* amorphous silicon device with default atlas material parameters and the following properties: ohmic drain contact; nominal source barrier height set by choosing the work function of the metal to be higher by $\phi_{B0} = 0.5$ eV than the semiconductor electron affinity (actual value will be affected by interface properties); source-drain gap $d = 5\,\mu$m; device width $W = 1\,\mu$m; eight exponentially spaced values for source length S: 0.2, 0.5, 1.2, 2.9, 7, 17, 41, 100 μm; semiconductor thickness $t_S = 100$ nm; and insulator (SiO_2) thickness $t_i = 100$ nm.

We are investigating the effect of source length, and almost all the source is subject to a low field because most of

the drain potential is dropped across the pinch-off region at the end of the source (Figure 1). For this reason, the simulation parameters in Eq. (3) were set to $\alpha = 0$ and $\beta = 1$, and therefore confined to image force lowering, which is dominant at low fields.

In order to achieve good resolution in the important area around the edge of the source closest to the drain, meshing in the x direction was kept constant at 5 nm at that point, and allowed to vary as a proportion of S at the other edge. The ambient temperature range considered was 300–360 K.

III. RESULTS AND DISCUSSION

A. Modes of operation and source geometry

As outlined in Section I B, there are two distinct modes of operation of the SGT. The first mechanism is specific to the area of the source in which pinch-off occurs in the semiconductor (Figure 1(a)) and has a high dependence on electric field (from gate *or* drain). As the semiconductor is depleted in this region (first few tens to hundreds of nanometers from the edge of the source closest to the drain inwards), the electric field can penetrate to the metal-semiconductor contact and contribute to barrier lowering from Schottky effect and tunnelling. Thus, at high electric field, the barrier in this region of the source can be modulated, and since the reverse current of the contact is exponentially dependent on effective barrier height,[20] large changes in current (I_1) can be effected by changing the potential on the gate. The drain bias, however, has a similar effect on this area of the source, so without purposeful screening of the source edge from drain electric field,[11] output characteristics have a drain voltage dependence of the current in saturation.[5,9]

The second mechanism involves the whole area of the source (for the benefit of visualization, we will call this the "bulk" of the source, as opposed to the "edge" referred to above). The current here (I_2 in Figure 1(d)) is controlled by the combination of a distributed resistive network in the semiconductor under the source and the JFET-like region at the semiconductor-insulator interface where pinch-off occurs (D_p). The resistance in the x direction is represented by the accumulation layer created by the applied gate bias at the semiconductor-insulator interface. In the y direction, the resistance is given by the average resistivity of the semiconductor and its thickness (Figure 1(d)).[3,9] The reverse biased source barrier (D_s in Figure 1(d)) plays a role in current control, not as a current-limiting mechanism, but rather as a non-linear potential drop. Simply, the second mechanism is a two-dimensional potential gradient problem, in which (for V_G above "threshold") $V_{SAT1} = (V_G - V_T) \cdot C_i \cdot (C_i/C_S)$ is applied to the anode of D_p ("floating source" of the parasitic FET which forms between this point and the ohmic drain) in Figure 1(d).[3,23]

Figure 1(e) shows the current density J_S crossing the source-semiconductor interface for different source lengths. The total drain current will be the integral of J_S across the length of the source. The biasing condition considered (V_G, V_D) ensures that the device is operating in saturation and that the current is controlled by the source. The plot shows the current density injected *at that point* of the source vs. position along the source, starting at the edge closest to the drain. Five curves are presented, for devices with source lengths of 1, 3, 5, 10, and 100 μm, respectively. In the first ~200 nm of the source, current injection has a very similar profile, regardless of S. This is the region where the first injection mechanism (I_1) dominates. Further along the source length, the curves diverge when S changes.

As an example, consider the curves for $S = 1$ and 10 μm. The current injected at $x = 1$ μm by the shorter source is larger. This is due to the potential drop produced by current flowing in the accumulation layer (R_{ch} chain) (Figure 1(d)). In the $S = 10$ μm device, the total current injected between $x = 10$ μm and $x = 1$ μm flowing between $x = 1$ μm and $x = 0$ creates a potential drop at $x = 1$ μm, which does not exist for the $S = 1$ μm device. The total current is higher in the longer-source device owing to the larger injection area.

Following the analysis above, we can see that increasing S further leads to a condition where the potential in the channel at the far end of the source reaches a value for which no voltage is dropped across the respective *Rsc* and no current is injected by that region of the source (Figure 1(e)). Increasing S beyond this value (S_{SAT}) does not lead to an increase in total current. The value of S_{SAT} depends on the resistivity of the semiconductor channel (magnitude of R_{ch}), which in turn is modulated by applied gate bias. Figure 2(a) shows the change in S_{SAT} with V_G and the saturation of the current with increasing S above S_{SAT}.

B. Source length and its influence on mode of operation

Changes in device operation are observed, depending on which of the two current injection mechanisms dominates. The transconductance of the drain current (g_m, Figure 2(b)) shows a definite kink when switching between modes of operation.[5] A longer S allows more current to be injected from the bulk of the source, pushing the gate voltage at which the kink occurs to higher values. This is due to the fact that more barrier lowering needs to occur for longer S in order for current I_1 (Figure 1(d)) to increase enough to compete and overtake I_2. For a given S, at V_G below the kink in g_m, I_2 dominates, while above, I_1 dominates.

C. Activation energy of drain current

1. Source length and activation energy

The observations above and in Ref. 5 have significant implications on the temperature dependence of drain current. We plot the activation energy (E_A) of I_D vs. gate bias for different values of S. Neglecting the low-voltage, sub-threshold range of V_G, a large range of E_A is observed. The nominal value for the barrier height (metal work function minus semiconductor electron affinity) in the model was $\phi_{B0} = 0.5$ eV, but the effective barrier (ϕ_{B0}') will depend on surface characteristics and is expected to be higher. Importantly, E_A decreases with S and for the largest S activation energy is ~0.3 eV, significantly smaller than ϕ_{B0}'. Shorter values of S produce curves which initially dip substantially below ϕ_{B0}' but later increase back towards ϕ_{B0}' at high V_G.

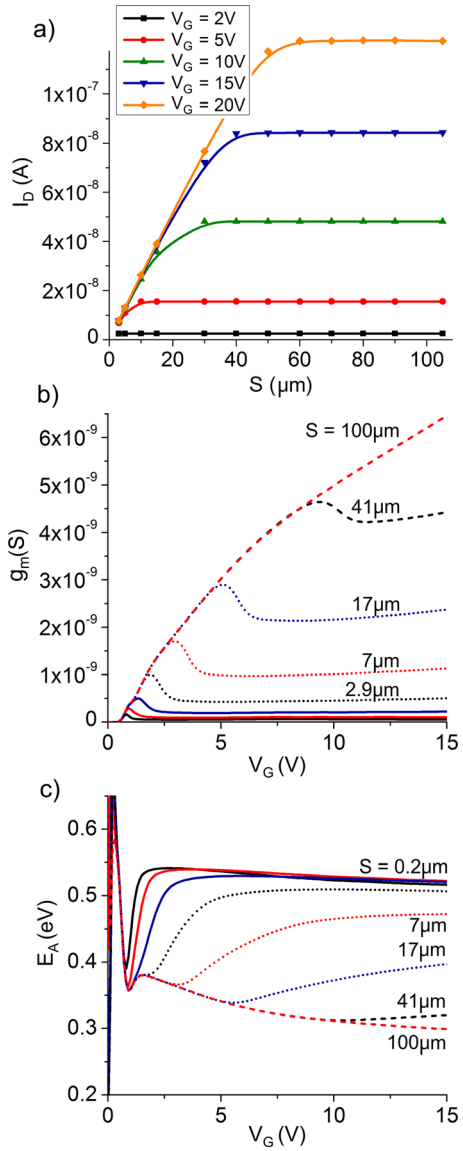

FIG. 2. Simulation of SGT electrical behavior with changes in source length. (a) Dependence of saturated drain current on gate bias and source electrode length, S; (b) Transconductance, g_m shows a kink in its gate voltage dependence. The kink occurs at higher voltages for longer S and is due to the change of dominant current injection mechanism. Bottom to top $S = 0.2$, 0.5, 1.2, 2.9, 7, 17, 41, 100 μm; (c) The activation energy of drain current shows similar behaviour to transconductance, with corresponding kinks at the same gate voltages. Top to bottom $S = 0.2$, 0.5, 1.2, 2.9, 7, 17, 41, 100 μm. For all panels $\phi_{B0} = 0.5$ eV, $\alpha = 0$, and $\beta = 1$.

The deviation from the curve of minimum E_A happens for different values of S at the same V_G as the kink in transconductance, since the change in mode of operation (and current control mechanism) brings about a change in thermal properties of the injected current. For very short S, the current has a high E_A which decreases somewhat with V_G, according to the field-dependent barrier lowering model enabled in the simulator ($\beta = 1$).

In brief, Figure 2(c) shows that depending on the dominant injection mechanism, the current can have significantly different activation energy. The envelope at higher E_A is the activation energy for I_1 while the lower envelope is for I_2. Current I_1, dominant for short sources or very high V_G, has as expected, an activation energy close to the effective barrier height ϕ_{B0}', which is pulled down as V_G increases. Current I_2, conversely, has a very low activation energy which cannot be explained by the properties of the barrier and must be imparted by the current restriction mechanisms of I_2.

2. Effects of other parameters on activation energy

Figure 3 shows the activation energy of drain current vs. V_G for SGTs with extreme values of source length: 0.2 and 100 μm, for three values of nominal barrier height ϕ_{B0}, in the absence of field-induced barrier lowering ($\beta = 0$). For the short source device, in which I_1 dominates and is controlled exclusively by the barrier, E_A correlates with ϕ_{B0}. With no field-dependent barrier lowering, E_A does not change with V_G above threshold. Increases in ϕ_{B0} translate in equal increases of E_A. For the long source (I_2 dominates), smaller increases in E_A are seen than the respective increases of ϕ_{B0}. We explain this as a consequence of current control in this mode of operation: an increase in ϕ_{B0} reduces the voltage drop available across the semiconductor; with little change to the resistance R_{sc}, the current injected from a point in the bulk of the source is less for higher ϕ_{B0}, following the reduction in potential difference between the two sides of the semiconductor. In this mode of operation, there is also significant modulation of E_A with V_G, which will be discussed in Sec. III C 3.

In Figure 3, the lack of field-induced barrier lowering is unrealistic. Supplementary Figure SF1(a)[24] shows the effect of enabling field-dependent barrier lowering ($\beta = 1$). A FET with the same geometry and characteristics was simulated for comparison. Its drain current activation energy (Supplementary Figure SF1(b)[24]) is small but positive, consistent with current understanding of these devices.[21]

3. Split source didactical model

In order to be able to graphically show the effect of I_1 and I_2, the following structure was studied: the source of the device in Figure 1(d) was split into two electrodes ($S_1 = 0.2$ μm and $S_2 = 95$ μm) separated by a 4.8 μm gap (Figure 4(a)). In the first approximation, S_1 is injecting I_1 and S_2 is injecting I_2. The functional difference between this structure and the original is the gap between S_1 and S_2, which

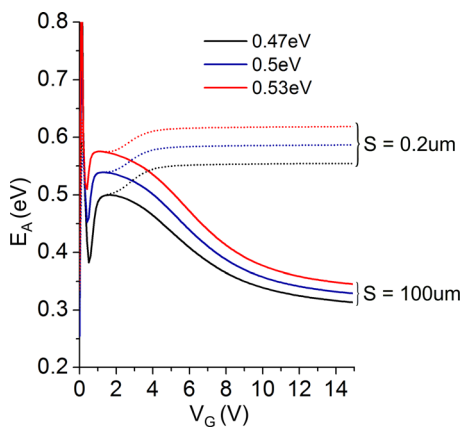

FIG. 3. Simulated activation energy vs. gate voltage plots for thee source barrier values and extreme source lengths ($\phi_{B0} = 0.5$ eV, $\alpha = 0$, and $\beta = 0$).

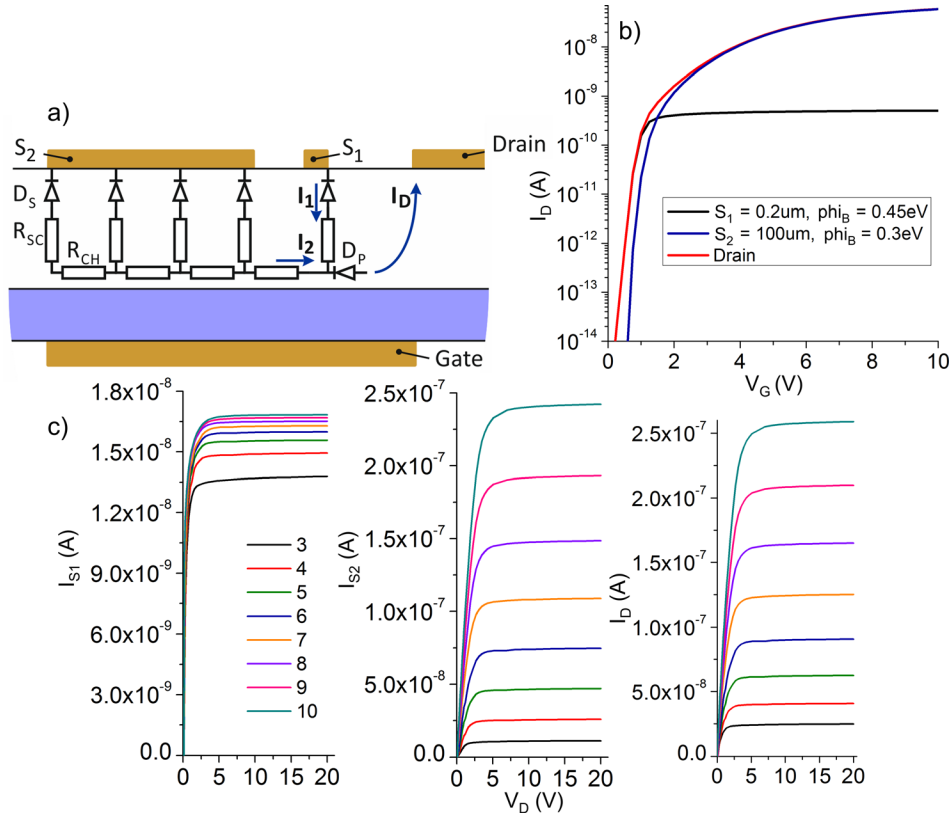

FIG. 4. (a) schematic cross-section of the didactical structure, showing the location and relative size of the two source electrodes; (b) simulated transfer characteristics for the structure in (a) showing the contribution of the currents injected by electrodes S_1 and S_2 to the total drain current, for $V_D = 5$ V; (c) output characteristics of same showing the saturation profile and the relative magnitude of the S_1, S_2, and drain current, for barrier lowering coefficients $\alpha = \beta = 0$ and eight gate bias values.

introduces a R_{ch} component which was not present in Figure 1(d), potentially lowering the magnitude of I_2 somewhat by the discussed potential drop. However, this effect can be discounted in the present qualitative discussion. More importantly, the edge of S_2 closest to S_1 does not induce pinch-off during operation, so there is no I_1-type component originating form S_2, and the I_2-type component injected by S_1 is comparatively small, given its size.

While this type of structure is impractical to fabricate with current technology, the simulation allows us to identify and understand contributions from the edge and the bulk of a continuous source electrode in a practical device.

The transfer characteristic in Figure 4(b) shows the contribution to drain current of the currents injected by S_1 and S_2 (again, for practical purposes equivalent to I_1 and I_2). S_1 and S_2 are both at 0 V potential. The drain current is the sum I_1 and I_2. At very low gate bias, it is made up exclusively of I_1. With the increase in V_G, I_1 becomes limited by the reverse saturation current of the contact at S_1 (for simplicity, no barrier lowering was considered in this theoretical study; $\beta = 0$). At the same time, S_2 increases as the accumulation layer becomes more conductive and surpasses I_1 (at a voltage where the kink in the g_m characteristic occurs, see Figure 2(b)), eventually becoming the dominant component of I_D.

In Figure 4(c), output-like characteristics are drawn for I_1, I_2, and I_D, for different values of V_G. We notice the low modulation of I_1 and its low magnitude at high V_G. I_D is exclusively composed of I_2 at high gate bias. The change in saturation voltage V_{SAT1} with V_G is, to a good approximation, only controlled by the electrostatics of the semiconductor-insulator stack and remains unchanged regardless of the proportion of I_1 and I_2.

Supplementary Figure SF2[24] illustrates the composition of I_D in terms of I_1 and I_2 at different gate biases, showing graphically that I_D has only slight dependence on I_1, particularly at high V_G, and that is almost entirely made up of I_2, apart from the very low current region at low V_G.

Given that I_1 and I_2 have very different activation energies, the temperature coefficient of the drain current will be defined by the dominant of the two. Figure 5(a) shows the activation energy vs. gate voltage plot for drain current in a device with constant $\phi_{B0}(S_1) = 0.45$ eV and varying $\phi_{B0}(S_2)$ from 0.2 to 0.55 eV. When $\phi_{B0}(S_2)$ is high, I_2 contribution is low and E_A is given by S_1. As $\phi_{B0}(S_2)$ decreases, I_2 becomes higher and dominates in the composition of I_D. This is a similar effect to that obtained by increasing S in the original structure. The activation energy of I_1 and I_2 are plotted together with that of I_D in Figure 5(b). We see how drain current E_A switches between the two as I_2 increases with V_G. The composition of drain current is shown graphically in the cross-section in Figure 5(c), obtained by probing across the device 2.5 nm into the semiconductor at the insulator interface. Current builds up along the length of S_2 and it plateaus as it crosses the gap between S_2 and S_1. The contribution of S_2 is added on to form the total current which passes through the accumulated channel and is collected at the drain. The relative magnitude of I_1 and I_2 dictates the dominant mode of operation, and also the activation energy of I_D.

D. Implications for device design

The easiest way of ensuring dominance of I_2 over I_1 is through sizing of the source electrode. Longer S shifts the ratio of I_1 and I_2 in the composition of drain current towards

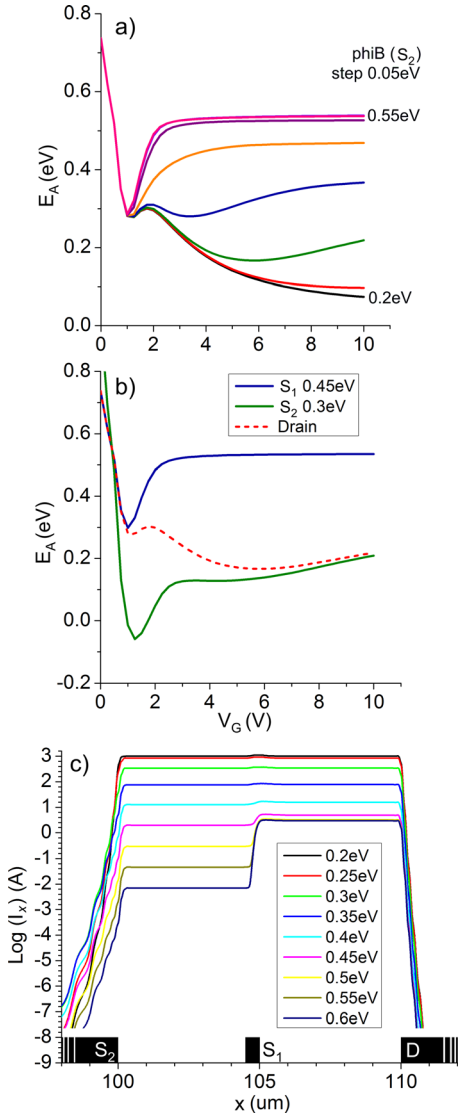

FIG. 5. Simulated behavior of SGT with split source. (a) Activation energy of drain current vs gate voltage for different values of potential barrier at electrode S_2, while keeping $\phi_{B0}(S_1) = 0.45$ eV constant; (b) Activation energies of the currents at electrodes S_1, S_2, and D, showing that the drain current activation energy approaches that of the current of S_2 when S_2 contributes the largest proportion of drain current; (c) Cutline at the insulator-semiconductor interface showing total current in the X direction vs. position, for varying $\phi_{B0}(S_2)$ and constant $\phi_{B0}(S_1) = 0.45$ eV, illustrating the contribution of S_1 and S_2. $\alpha = \beta = 0$ throughout. $S_2 = 95\ \mu$m.

the latter. Thus, the activation energy of drain current tends to that of I_2, which is lower. Extremely long values of S have no effect, as the current tends to saturate with S due to resistive effects in the semiconductor (Figure 1(d)).

For the geometries and biasing conditions considered, which originate in practical devices studied extensively in the past, we found that values of source length, S, in the 30–50 μm range are best suited for obtaining low temperature coefficient of drain current. From a fabrication point of view, such S is not wasteful of layout area, considering the conventional sizing of (doped) contact region and design rules for contact metallization. Furthermore, source-drain gap can be made as small as the technology will allow in SGTs while maintaining flat saturated characteristics, saving area in the same direction as S.

Relatively long S is preferred for a related reason: I_1 is electric field-dependent; I_2 is less so. When I_2 dominates, the flatness of the output characteristics is superior without the need for a specially designed field relief structure.[5,11] Long source devices should have improved intrinsic gain characteristics.

Saturation voltage, V_{SAT1},[7] remains low compared to conventional FETs, even when S is large. A slight increase in V_{SAT1} may be observed for long S, as the current below saturation follows the FET linear region envelope (longer S entails total current injected at the source, which is closer to the FET channel conductance envelope for that particular gate and drain bias combination).

E. Implications for circuit design

The gate overlaps the whole area of the source. The capacitance introduced by large S (large source-gate overlap) may indeed lower the operating frequency of such devices. However, we expect the utility of SGTs to be in localized areas of circuits such as bias and signal generation, initial signal amplification, and active loads to high gain stages, where their other characteristics will play a major role and where speed is not the principal requirement.

Source-drain gap is inconsequential in SGTs over a large range. With changes in S, however, come (modest) changes in current and temperature coefficient. Longer values of S, then, ensure that processing variations resulting from poor registration or thermal expansion/shrinkage of the substrate during fabrication are easily tolerated. First, the total drain current changes very little with changes in S around a certain value S_{SAT}. Second, as a proportion of total S, variations in the micron range are comparatively small. Together, these result in superior matching of electrical characteristics of devices in different parts of the substrate, and improved consistency across substrates and fabrication runs.

A similar benefit in terms of uniformity of performance across a large area arises from the lower temperature coefficient of the drain current for devices with longer S. Different parts of the chip are prone to temporal and areal variations in temperature during operation. Temperature dependence is minimized when S is long, permitting more relaxed design margins, simpler or no temperature compensation and improved operating temperature window.

Finally, the low increase in effective saturation voltage, V_{SAT1}, with S suggests that longer-source SGTs are still capable of being used in power-efficient designs, with low series voltage drop, meaning lower power supply levels or, conversely, the ability to design with additional cascaded devices between the rails, such as in cascade architectures.

IV. CONCLUSION

Thin-film source-gated transistors are field-effect devices with construction very similar to conventional transistors. A source barrier deliberately engineered at the source radically changes the operation of such devices, allowing them to achieve low saturation voltage and high output impedance in saturation, along with stability under bias stress and tolerance to geometrical variations. Numerous analog as

well as digital applications can benefit from the energy efficiency and gain characteristics of such devices.

Two mechanisms for current injection at the source have been identified. First, the first few hundreds of nm of the source from the edge closest to the drain operate in a high electric field, high activation energy, and high barrier modulation regime. The temperature coefficient of this current (I_1) is comparatively high, unless substantial barrier lowering occurs under electric field. Second, the remaining area (bulk) of the source (I_2) injects current in a low electric field, low activation energy, low *source* (metal/semiconductor) barrier modulation regime, which is controlled by a resistive network in the source region of the semiconductor, along with a JFET-like component in the pinch-off region at the edge of the source closest to the drain, on the semiconductor-insulator interface. I_2 has a low temperature coefficient.

In this paper, we have described how the activation energy of total drain current depends on the activation energies of I_1 and I_2, but also, importantly, of the ratio of I_1 and I_2. In order to reduce the temperature coefficient of drain current, the low-activation energy I_2 is required to be significantly greater than I_1. In this way, drain current activation energy approaches that of I_2.

Notably, lowering the activation energy of drain current by a simple method such as increasing S will simplify design of SGT-containing circuit blocks in a large-area system where spatial temperature variations are likely to occur, reducing the need for compensation circuitry. At the values of S needed, process variations of S and d are well tolerated, with no practical changes in electrical characteristic.

The simple structure and design parameters of SGTs, in conjunction with its operating characteristics, recommend these devices as powerful circuit design tools for future energy-efficient, high performance large area electronic systems.

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