

Progress, challenges, and opportunities for HgCdTe infrared materials and detectors

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This article presents a review on the current status, challenges, and potential future development opportunities for HgCdTe infrared materials and detector technology. A brief history of HgCdTe infrared technology is firstly summarized and discussed, leading to the conclusion that HgCdTe-based infrared detectors will continue to be a core infrared technology with expanded capabilities in the future due to a unique combination of its favourable properties. Recent progress and the current status of HgCdTe infrared technology are reviewed, including material growth, device architecture, device processing, surface passivation, and focal plane array applications. The further development of infrared applications requires that future infrared detectors have the features of lower cost, smaller pixel size, larger array format size, higher operating temperature, and multi-band detection, which presents a number of serious challenges to current HgCdTe-based infrared technology. The primary challenges include well controlled p-type doping, lower cost, larger array format size, higher operating temperature, multi-band detection, and advanced plasma dry etching. Various new concepts and technologies are proposed and discussed that have the potential to overcome the existing primary challenges that are inhibiting the development of next generation HgCdTe infrared detector technology. © 2015 AIP Publishing LLC.

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Over the past several decades, HgCdTe, a ternary II-VI semiconductor alloy, has continually demonstrated superior performance in the most demanding applications of infrared (IR) technology, both for IR sensing and imaging. Because of its tuneable bandgap over a wide spectral range, high absorption coefficient, high carrier mobility, and long carrier lifetime, HgCdTe has maintained its position as the material of choice for fabricating IR photodetectors with high performance over a wide spectral range, including the short-wave IR (SWIR: 1–3 μm), mid-wave IR (MWIR: 3–5 μm),	8

long-wave IR (LWIR: 8–14 μm), and very-long-wave IR (VLWIR: 14–30 μm) bands.¹ The primary focus of HgCdTe technology development has been on imaging focal plane array (FPA) demonstration for night vision, and intelligence, surveillance, reconnaissance (ISR) applications. High performance HgCdTe infrared detectors and their FPAs are now being manufactured by a number of large companies and institutes in the USA, UK, France, Germany, Israel, and other countries, such as Raytheon, CEA-LETI, Teledyne, DRS, Sofradir, AIM, Selex, and others.

Despite its unparalleled device performance, such as high detectivity (mid- 10^{11} ~ mid- 10^{12} cmHz $^{1/2}$ W $^{-1}$), high quantum efficiency (>70%), and fast response time (several ns), HgCdTe IR detector technology suffers from a number of major limitations, including *high cost, limited array size, low operating temperature, and material fragility*. Consequently, other competing IR technologies have been regularly proposed to replace HgCdTe to overcome the limitations of HgCdTe-based IR detectors, including lead salt alloys, InSb, quantum well IR detectors, quantum dot IR detectors, and type II superlattice based detectors. Although significant effort has been devoted to developing these alternative IR technologies,^{1–10} at this stage they still cannot compete with HgCdTe IR detectors for applications in *high performance* IR systems due to their respective limitations.

The most promising and recent competitor to HgCdTe IR technology are IR detectors and FPAs based on III-V type II superlattices, such as InAs/GaSb and InAs/InAsSb.^{2,11,12} Theoretically, type II superlattice-based IR detectors provide good quantum efficiency due to the strong absorption of normal incident light. In addition, because of the type II band alignment, such detectors have the potential to reduce Auger dark current, and thus to increase the operating temperature.² However, such type II superlattice IR detectors suffer from a major limitation, at least at present, related to the short Shockley-Read-Hall carrier lifetime (<100 ns experimentally). Despite an intensive research effort over the last decade, little improvement has been made in this area, and most of the reported InAs/GaSb superlattice-based detectors perform approximately one to two orders of magnitude lower than comparable state-of-the-art HgCdTe detectors, primarily due to the lower quantum efficiency and shorter minority-carrier lifetime.^{2,11,12}

At the present time, it is quite likely that HgCdTe-based IR technology will continue to dominate the high performance end of the IR systems market, at least in the foreseeable future. However, HgCdTe IR technology has its own set of limitations, as briefly discussed previously. Therefore, it is appropriate at this time to undertake a complete review on recent progress and current status, and to discuss the current and future challenges and solutions to these challenges, which will facilitate the further development of this strategically important technology. In this work, we will present a review on the recent progress, current status, and future challenges for HgCdTe IR detector technology, including materials and devices. Based on this review, we will propose and discuss various new concepts and technologies that are currently in development for overcoming the current primary challenges of HgCdTe IR detectors.

II. CURRENT GLOBAL SCENARIO FOR HGCDTE INFRARED MATERIALS AND DETECTORS

After several decades of development, significant progress has been achieved in this strategically important research area, including HgCdTe material growth, device architecture, device fabrication processes, and device applications, for both single detector devices and multi-pixel FPAs, which will be discussed in Secs. II A–II D.

A. Material growth of HgCdTe

The growth of single-crystal HgCdTe material presents significant challenges due to the relatively high vapour pressure of Hg, which makes it difficult to control the stoichiometry and composition of the HgCdTe material during growth as well as during any subsequent thermal treatment.^{1,13} Despite this challenge, significant advances have been made in this area since the discovery of HgCdTe in 1959. The growth method for crystalline HgCdTe crystal has gradually evolved from bulk crystal growth to growth of epitaxial layers on transparent insulating substrates. With the increasing demand for fabricating HgCdTe detectors with larger area FPAs and complex device architectures, epitaxial growth now dominates the material growth of HgCdTe.

In general, there are two main epitaxial growth techniques applied for HgCdTe: liquid phase epitaxy (LPE) and vapour phase epitaxy (metal-organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE)). LPE is the most traditional and mature technology and has been used widely for industrial production for several decades. In order to achieve higher crystal quality and growth efficiency, HgCdTe materials are usually grown on (111) CdZnTe (4% Zn) substrates, which are lattice matched to HgCdTe. The HgCdTe materials obtained via LPE show high crystalline quality, typically demonstrating X-ray diffraction full-width-half-maximum (XRD FWHM) of 25–40 arc sec, an etch pit density (EPD) of 1×10^4 – 1×10^5 cm $^{-2}$, and a residual doping of $<1 \times 10^{15}$ cm $^{-3}$.^{14,15} The LPE method has been successfully applied to growing HgCdTe detectors in various spectral detection bands, including SWIR, MWIR, LWIR, and VLWIR. It is expected that LPE will continue to be an important growth method for HgCdTe, especially LWIR HgCdTe. However, this method doesn't allow the epitaxial growth of complex detector structures, such as multi-band detectors and barrier detectors. As a result, significant attention has shifted to MOCVD and MBE growth of HgCdTe, which will be discussed later. The current effort in this area is focused on providing flatter and more uniform epilayers across large-area wafers, which is required for improving the performance and imaging quality of large-area FPAs.^{14,15}

In comparison to LPE, MOCVD and MBE allow the growth of larger area wafers and more complex device structures with good lateral homogeneity, and abrupt and complex composition and doping profiles, which are essential requirements for the development of advanced HgCdTe detectors and FPAs. Specifically, vapour phase epitaxy enjoys the flexibility in engineering the material and device parameters during growth, such as bandgap energies, incorporation of heterostructures and multiple layers, control of doping

profiles, use of alternative substrates, formation of passivation layers, and *in-situ* annealing. In particular, vapour phase epitaxy has been an indispensable tool for developing dual-band IR detectors that integrate two detectors onto a single pixel, which is a complex device structure. Nowadays, the material quality obtained with vapour phase epitaxy is comparable to that routinely obtained with LPE. MOCVD growth of HgCdTe is mainly conducted in the UK (Selex) and Poland (Vigo), while MBE growth is undertaken in many other countries, including USA, France, Russia, Germany, Israel, China, Norway, South Korea, and Australia. Because of the higher popularity of MBE growth for HgCdTe materials, this review will mainly focus on MBE growth of HgCdTe material for IR detector applications.

In comparison to III-V semiconductors, the MBE growth of HgCdTe material is a very challenging task because of the critical growth parameters required for achieving high crystalline quality. For example, the optimum temperature window for growth is less than 5 °C. The typical growth conditions used at The University of Western Australia (UWA) are as follows: growth temperature of 185 °C–190 °C, Hg flux (beam equivalent pressure (BEP)) $\sim 2 \times 10^{-4}$ Torr, CdTe flux (BEP) 4×10^{-7} Torr, and Te flux (BEP) 10^{-7} – 10^{-6} Torr. The Cd mole fraction in HgCdTe is controlled *via* tuning the flux ratio of Te to CdTe. After several decades of development, MBE has become a relatively mature technology for growing HgCdTe on CdZnTe and other alternative substrates. Indium incorporation is typically used for extrinsic n-type doping and arsenic incorporation for extrinsic p-type doping. Although indium n-type doping has been well accepted by the research community, arsenic p-type doping is still a controversial topic in the community due to the amphoteric nature of the arsenic impurity in HgCdTe. As a result, well controlled p-type doping is still a very challenging task, which will be discussed in Section III. It should be noted that as-grown HgCdTe materials usually demonstrate p-type behaviour due to the presence of intrinsic Hg vacancies,¹⁶ which can serve as carrier scattering centres. Thus, they play a significant role in reducing the carrier mobility and lifetime, which are the two main material parameters that determine the quantum efficiency of detectors. In addition, intrinsic Hg vacancies can also compensate any n-type dopants in the material, especially at very low doping concentration, and thus can seriously reduce the efficiency of extrinsic n-type doping. Therefore, low temperature (~ 250 °C for 24 h) post-growth annealing under a high Hg vapour overpressure is commonly performed to eliminate intrinsic Hg vacancies (as low as 10^{13} cm^{-3} level) and thus optimize the structural and electronic properties of the material.¹⁶ Note that the purpose of this low temperature anneal is only to eliminate Hg vacancies, and is not necessary for the activation of n type dopants, such as indium.

Generally, MBE HgCdTe is grown on lattice matched (211)B CdZnTe (4% Zn) substrates due to the higher growth efficiency and crystalline quality. Apart from CdZnTe substrates, other alternative substrates, such as Si, Ge, and GaAs,¹⁷ have received significant attention over the years due to the limitations of high cost, small size, and limited suppliers of CdZnTe substrates, although there has been

renewed effort in growing large ingots of CdZnTe.¹⁸ However, the crystal quality of HgCdTe grown on alternative substrates is not as good as that grown on lattice matched CdZnTe substrates, especially for LWIR HgCdTe materials, which needs to be improved further. Despite the challenges of p-type doping and non-ideal substrates, it is expected that MBE growth of HgCdTe will continue to be the technique of choice for future HgCdTe growth, considering the great flexibility that is offered.

B. Device architectures for HgCdTe detectors

With the progress of material growth techniques over the past several decades, HgCdTe detector architectures have also developed from the initial simple photoconductor structure to standard p-n junction photodiode structure and, more recently, to more complex detector. HgCdTe-based photoconductors were the standard detector structures used in the early days (1960s) of the IR industry. HgCdTe photoconductors can provide reasonably high performance and thus have been used in various IR applications, including single detectors and small FPAs. Single element HgCdTe photoconductors are still widely used in spectroscopy instruments nowadays, such as Fourier transform IR spectrometers. However, because of their low impedance and high-power dissipation, HgCdTe photoconductors were only used for making small FPAs, typically <200 elements in a linear array format.

With the increased requirements for high quality imaging, large format HgCdTe two-dimensional (2D) FPAs were needed, which cannot be met with HgCdTe photoconductors due to their high power dissipation. In contrast, photovoltaic detectors are p-n junction diodes operating under reverse-bias conditions, and thus have high impedance and very low power dissipation, which provides an excellent device structure for fabricating high performance large format 2D FPAs. Apart from very low power dissipation, photodiode detectors also have advantages of negligible 1/f noise and easy multiplexing to a silicon readout integrated circuit (ROIC).^{1,13} Furthermore, the response of photodiodes remains linear over a significantly higher photon flux range compared to that of photoconductors. As a result, photodiodes have become the dominant device structure for IR imaging applications.

For photodiode device structures, the critical region is the p-n junction, which can be formed using different approaches, including intentional extrinsic p and n type doping, ion implantation, Hg diffusion, impurity diffusion, and type conversion. For example, n-on-p homojunctions can be formed by implanting n type dopants into p-type HgCdTe (intrinsic Hg vacancy doped p type) or by conversion of the p-type material into n-type using techniques such as plasma processing and ion milling.¹ If the HgCdTe materials are grown using MBE or MOCVD, the p-n junction can be formed during the growth process *via* *in-situ* extrinsic p and n type doping.

Regarding the fabrication technology of p-n junction photodiodes, there are generally two classes of processing structure used: mesa structures and planar structures, which

are illustrated in Figure 1. The processing procedure of a planar device structure usually involves surface passivation, window etch, p-n junction formation, followed by metal contact deposition, whereas that of mesa device structures usually involves p-n junction formation, mesa isolation etching, followed by surface passivation and metal contact formation. Despite their relatively simple fabrication and passivation processes (p-n junction is not exposed to air), planar device structures suffer from some serious limitations in FPA applications, including high cross-talk and low pixel density. Because of the long diffusion length for minority carriers in HgCdTe materials (up to $\sim 50 \mu\text{m}$),¹⁹ significant cross-talk can exist between pixels if the distance between pixels is close to or less than $50 \mu\text{m}$. This seriously limits the pixel density and thus the FPA format size, which is not acceptable for high performance IR imaging applications. In addition, planar device structures cannot take advantage of *in-situ* grown junctions and extrinsic doping process that have become available with modern epitaxial growth technologies, which tends to limit the device structure to simple p-n junctions. In contrast, the mesa device architecture can overcome the main disadvantages of planar device structures. By etching the mesa down to the absorption layer, each individual pixel is well isolated from all the others, and the diffusion of minority carriers is physically suppressed, which relinquishes the requirement of a large distance between pixels in order to reduce cross-talk. Thus, mesa-isolated device structures are suitable for fabricating FPAs with small pixel size, high pixel density, and lower cross-talk. In addition, mesa device structures also allow the utilization of complex heterostructures and high quality *in-situ* extrinsic doping, which are required by modern IR applications, such as multi-band IR detectors. Therefore, mesa device structures have become the architecture of choice for fabricating modern FPAs with the combined features of small pixel size, high pixel density, low cross-talk, and complex heterostructures. Thus, this review will mainly focus on IR detectors based on mesa-isolated device structures.

Over the years, several kinds of photodiodes have been developed, including p-n junction photovoltaic diodes (both homojunction and heterojunction) and MIS photo-capacitors.^{1,13} Among them, p-n junction photovoltaic diodes have attracted more attention and have become the mainstream technology. In general, there are two groups of p-n junction diodes: one is an n-on-p junction diode and the other is a p-on-n junction diode, where the latter device has been demonstrated to have higher device performance: that is lower

dark current and thus higher operating temperature.²⁰ Both n-on-p and p-on-n junction diodes have been successfully applied in fabricating HgCdTe FPAs with large format size. However, the current state-of-the-art photodiode detectors suffer a main limitation—low operating temperature, usually liquid nitrogen temperature, due to the relatively large dark current. Such low operating temperature seriously limits their range of applications. Ideally, IR detectors should operate at thermoelectrically cooled temperatures (e.g., 250 K) or room temperature. Though significant progress has been achieved in this area, the operating temperature of current HgCdTe detectors is still much lower than 250 K. So, it still presents a large challenge to fabricate HgCdTe detectors to operate at high operating temperatures above 250 K or room temperature, which will be discussed in Section V.

Apart from the challenge of low operating temperature, another challenge in the device architecture of HgCdTe detectors is multiband detection, which is required for future IR imaging applications. In comparison to single band detection, the device structure is much more complicated. Although some advances have been made, it is still very challenging to fabricate high performance multi-band HgCdTe detectors, which will be discussed in Section VI.

C. Device processing and surface passivation of HgCdTe detectors

Regarding the parameters that impact on the performance of IR detectors, especially FPAs, there are several main determining factors, such as material quality, device architecture, device processing, and surface passivation. To achieve high performance HgCdTe detectors, it is critical to develop a reliable fabrication process and passivation technology. The fabrication of modern mesa-isolated IR FPAs is far more challenging than single element detectors and requires the fabrication of well-isolated pixels with high aspect ratios, smooth sidewalls, and high uniformity, where etching plays a critical role. In the early days of IR technology development, devices were fabricated mainly *via* wet chemical etching, since the arrays were smaller and the distance between pixels was relatively large, e.g., $\sim 50 \mu\text{m}$.¹³ The widely used wet etchants are generally based on alcohol solutions of Br₂ and Br₂-HBr, including Br₂-lactic acid, Br₂-ethylene glycol, and HBr-H₂O₂.^{21,22} Wet chemical etching can produce smooth (RMS roughness of 2–3 nm) and damage-free surfaces if the process is well controlled.^{21,23} However, wet etching is isotropic and commonly results in

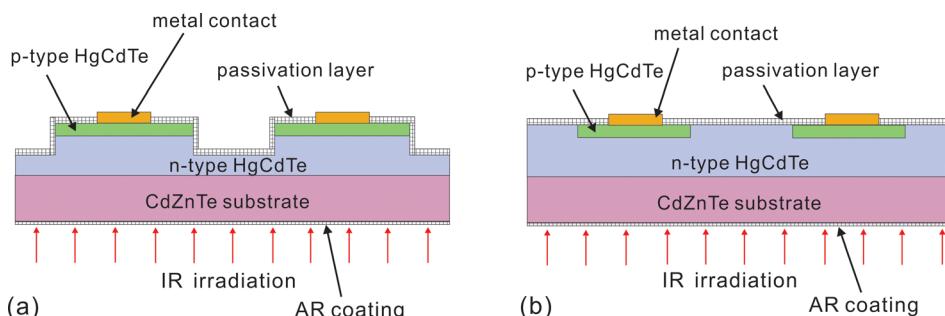


FIG. 1. Schematic diagram of (a) mesa structure and (b) planar structure of p-on-n HgCdTe photodiodes.

non-uniform etch rates, which are not suitable for fabricating HgCdTe IR FPAs with large format size.

For the fabrication of large format FPAs, it is desirable to have well-isolated pixels with deep, narrow sloped trenches with high aspect ratio, smooth surfaces, and high uniformity. Such practical requirements have prompted the development of dry etching technologies for HgCdTe, which commenced from the late 1980s.^{24,25} Currently, dry etching technology is dominated by plasma etching using a hydrocarbon/H₂ based methyl radical etching chemistry. Plasma etching enables anisotropic features and physical surface manipulation that are not possible using wet chemical processes. Dry processes also make possible a high degree of manufacturing process uniformity, run to run uniformity, and operator-independence that handling wet chemicals does not permit.²⁶ There are two main plasma generation systems widely used: electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) processes. ICP systems allow for large systems to be produced while maintaining uniformity over large sample areas. Although the current plasma dry etching technology of HgCdTe materials is not as well studied as other III-V and group IV semiconductors like GaAs, GaN, InP, and Si, significant advances have been made in this area since its first report in the late 1980s.^{24,25} Various processing parameters of plasma etching have been studied and optimized to achieve clean and smooth surface as well as to reduce the wafer damage and etching lag, such as substrate temperature, plasma gases used, RF power, DC bias, chamber pressure, Ar/H₂ gas ratio, photoresist parameters, and ion angular distribution (IAD). Nowadays, plasma etching has been successfully applied to the production of large FPAs of HgCdTe detectors. For example, Raytheon have fabricated an MWIR HgCdTe photodiode array of $2\text{ k} \times 2\text{ k}$ format and a dual colour FPA with a unit cell of $20\text{ }\mu\text{m}$.^{27,28} However, the features required for next generation HgCdTe IR FPAs, such as ultra-small pixels ($<=5\text{ }\mu\text{m}$) and multi-band detection, present challenges to current plasma etching technology, which will be discussed in Section VII.

Apart from mesa etching, another important step in detector fabrication is surface passivation, which can reduce recombination-generation centers and interface trap charges in devices, and thus reduce surface leakage current, resulting in lower dark current and thus higher device performance. Note that surface passivation is more critical in determining the performance of mesa structure-based detectors since the p-n junction is exposed to air during the fabrication process. In addition, surface passivation can also improve the thermal and chemical stability of the device. Over the years, various

materials have been studied to passivate HgCdTe detector surfaces, including ZnS, silicon dioxide, and CdTe.^{1,13,29} ZnS material was traditionally a widely used material for passivating HgCdTe detectors, which was also the common antireflection coating material for HgCdTe detectors. However, ZnS passivation suffers from long term stability issues during vacuum baking. Since the late 1980s, the focus of surface passivation has shifted towards the use of CdTe. Apart from its excellent quality, CdTe passivation is stable during vacuum packaging bake cycles and shows little effect from the radiation found in space applications. High quality CdTe surface passivation technology has made possible the full-scale production of “second-generation” devices. Though ZnS and CdTe have been successfully applied in the production of IR FPAs, it is still a challenging task to achieve very high quality surface passivation, which will be discussed in Section VC.

D. Application of HgCdTe detectors in focal plane arrays

Because of their increasing application, IR imaging FPAs have become the focus of IR technology development. Over the past several decades, HgCdTe-based IR detector FPAs have progressed significantly from “first generation” scanned linear arrays to “second generation” systems based on 2D arrays. In the 1960s, small linear FPAs (<200 elements) were developed and produced, which were based on HgCdTe photoconductors.^{1,13} In a linear FPA, an image is generated by scanning the scene across the linear array of detectors using a mechanical scanner, the schematic structure of which is shown in Figure 2(a). The linear scanning system does not include multiplexing functions on the focal plane, and these are usually referred to as “first generation” systems.

After the development of HgCdTe photodiode technology in the later 1970s, 2D photodiode FPAs were developed for IR imaging applications, which is the state-of-the-art FPA technology nowadays. The effort in this area was initially focused on MWIR and LWIR spectral band imaging (mainly for military applications), and later extended to SWIR for starlight imaging, and VLWIR for space-borne remote sensing beyond $15\text{ }\mu\text{m}$. In comparison to a linear array, a 2D FPA consists of more detector elements on the focal plane, thus providing higher sensitivity and spatial resolution. In general, two classes of array format have been developed and produced over the last several decades: *2D scanning format* and *2D staring format*, with the schematic structures shown in

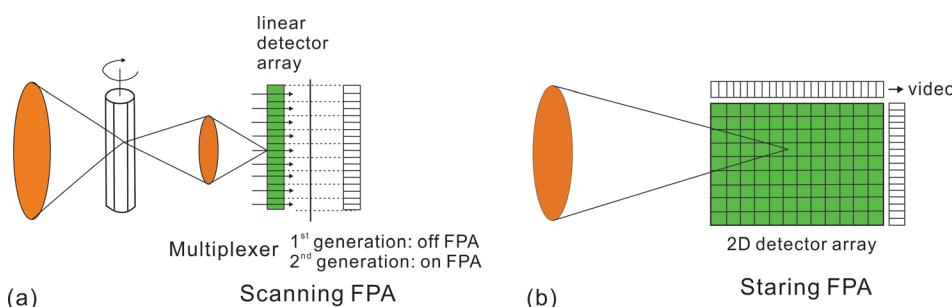


FIG. 2. Schematic structures of (a) scanning and (b) staring focal plane array systems. Reproduced with permission from A. Rogalski, Rep. Prog. Phys. **68**, 2267 (2005). Copyright 2005 IOP Publishing.

Figure 2.^{1,13,30} A 2D scanning format system is an intermediary system between a 1D linear scanning format system and a 2D staring format system. A 2D scanning system still relies on a scanned detector linear array, but with multiplexing functions through time–delay-and-integration (TDI) signal processing, which can be either on or off the focal plane. Such 2D scanning systems allow a 2D array up to 480×6 elements, which are much more than that of 1D scanning system, but much less than that of 2D staring format systems.

2D staring format systems are the current mainstream FPA technology. Compared with scanning format systems, staring format systems have increased the number of pixels much more dramatically, well beyond one megapixel. The 2D arrays are usually flip-chip bonded to readout circuit chips, and staring arrays are scanned *electronically, instead of mechanically*, by the circuits integrated with the arrays. The ROICs can undertake various signal processing functions, including pixel deselecting, anti-blooming on each pixel, subframe imaging, output preamplifiers, and others functions. Apart from flip chip bonding, loophole interconnection technology has also been used to integrate detector arrays with readout circuit chips, which can offer more stable mechanical and thermal features than the flip-chip hybrid architecture.^{1,13,31}

Over the years, various linear arrays (up to 960 elements), 2D scanning arrays with TDI (with up to 480×6 pixels), and 2D staring arrays (up to 2048×2048 pixels) have been developed with a wide range of spectral responses.³² Pixel sizes ranging from $15\text{ }\mu\text{m}$ (the current state-of-the-art technology) to over $50\text{ }\mu\text{m}$ have been demonstrated and used for production.^{27,28,33–35} Teledyne has developed the world's largest HgCdTe SWIR FPA for astronomy and low background applications.^{34,35} The format of the imaging module is a hybrid 2048×2048 FPA with a unit cell size of $18 \times 18\text{ }\mu\text{m}^2$ and with a side dimension of 37 mm. With the development of advanced IR imaging applications, larger and larger format HgCdTe FPAs are required. Though the processing of IR FPAs with format larger than 2048×2048 is possible with advances in plasma etching technology and small pixel technology, it is very challenging to make very large format HgCdTe FPAs due to the difficulty in large scale hybrid integration with multiplexing electronics. The discussion on large scale hybrid integration is interesting, but beyond the scope of this paper.

E. Challenges for future HgCdTe infrared technology

With the increased demand of various IR industry sectors, especially for military applications, more enhanced features are demanded for the future development of IR detectors, which are well above what current state-of-the-art IR detectors can offer. Generally, the new features include^{1,2,13} (1) high performance, high resolution cooled imagers having multi-colour bands, (2) medium- to high-performance uncooled imagers, (3) larger array format size with smaller area pixels, and (4) lower cost. IR detectors with these new features are usually referred to as “third generation” IR detectors.

As discussed in Section I, HgCdTe IR detectors will continue to dominate the high performance end of the IR market in the foreseeable future, although some other competing IR technologies have been developed. Therefore, HgCdTe will still be the material of choice for developing “third generation” IR detectors and their FPAs. In particular, a mesa isolated device architecture with the features of p⁺ on n, high aspect ratio plasma etching, extrinsic p and n doping, and vapour phase epitaxy, is the technology of choice for “third generation” IR systems because of (1) precise control of dopant concentration and profile; (2) small area pixels with high fill factor; and (3) multi-band detection. However, it is a very challenging task to develop “third generation” HgCdTe detectors and their FPAs considering the various limitations in current HgCdTe IR technology, such as high cost, limited array size, and low operating temperature. The next several sections of this paper will focus on discussing the challenges and potential opportunities that exist in developing “third generation” HgCdTe IR detectors. These challenges include:

- (1) *p-type doping;*
- (2) *lower cost and larger array format size for FPAs;*
- (3) *higher operating temperatures;*
- (4) *multi-band detection;*
- (5) *advanced plasma dry etching technology.*

III. p-type DOPING IN HgCdTe

The development of “third generation” IR detectors relies on the fabrication of advanced detector architectures with complex heterostructures, where the control over doping (both n-type and p-type) in the heterostructures is a must. Stable and well controlled n-type extrinsic doping of as-grown HgCdTe can be readily achieved over a wide range of dopant concentrations (10^{14} – 10^{19} cm^{-3}) through in situ incorporation of indium or iodine.^{16,36–38} However, well controlled p-type doping in HgCdTe is very difficult. Though as-grown HgCdTe materials typically show p-type behaviour due to the existence of intrinsic Hg vacancies, it is not so straightforward to make use of Hg vacancy doping because (i) the density profile of Hg vacancies cannot be well controlled, (ii) they are not stable against diffusion,^{39–41} and (iii) they significantly degrade carrier mobility⁴² and act as Shockley–Read–Hall (SRH) recombination centers, thus shortening carrier lifetimes.^{37,43–47} Therefore, similar to n-type doping, p-type doping is preferred to be undertaken via extrinsic impurity doping. However, it is very challenging to achieve stable and well controlled extrinsic p-type doping in MBE grown HgCdTe.

Like HgTe and CdTe materials, HgCdTe has a zinc-blende structure with two interpenetrating face-centered cubic lattices offset by $(1/4,1/4,1/4)\text{a}_0$ in the primitive cell, as illustrated in Figure 3.⁴⁸ The cations (Cd or Hg) form the yellow sublattice, while the Te anions form the purple sublattice. In theory, p-type extrinsic doping can be achieved by replacing anion atoms (Te) with group V atoms, or replacing cation atoms (Hg/Cd) with group I atoms, while n-type extrinsic doping can be achieved by replacing anion atoms (Te)

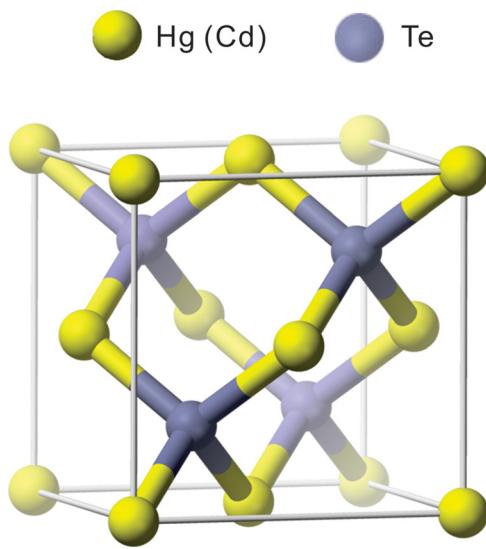


FIG. 3. Schematic unit cell of HgCdTe crystal.

with group VII atoms, or replacing cation atoms (Hg/Cd) with group III atoms. Table I presents the possible dopants for p-type and n-type doping in HgCdTe. Experimentally, extrinsic p-type doping could be achieved by the *ex-situ* implantation or diffusion of Group I or Group V ions, or *in situ* incorporation of Group I or Group V ions during growth. However, the *in situ* incorporation of dopants during growth is preferable to *ex-situ* implantation or diffusion because of the flexibility in controlling doping profile. Ion implantation or diffusion do not allow precise control over doping profiles and also induce considerable material damage, which reduces minority carrier lifetime and carrier mobility. Moreover, the high-temperature anneal required to mitigate the ion damage and/or for the in-diffusion of dopants is detrimental and leads to undesirable diffusion across junction interfaces.¹⁶

As shown in Table I, either Group I or Group V elements can act as acceptors (p-type dopants) in HgCdTe, when Group I elements are located on cation (Hg or Cd) sites, or Group V elements on anion (Te) sites. However, the MBE growth of HgCdTe is usually undertaken under Te-rich conditions,^{36,38,41,49–52} such that Hg vacancies are the dominant native point defect in as-grown HgCdTe, which is the reason why as-grown HgCdTe exhibits weak p-type behaviour. Therefore, in equilibrium, dopant atoms in as-grown HgCdTe are less likely to be located on Te sites than on cation sites. On cation sites, Group I atoms act as singly ionized p-dopants, whereas Group V atoms form neutral complexes or act as donors rather than acceptors.^{36,37,39–41,51–60} Thus, Group I elements would appear to provide a better extrinsic dopant and were the first to be tried as extrinsic p-dopants. However, although they show around 100% activation

efficiency as-grown and give excellent transport properties and minority carrier recombination lifetimes, they readily diffuse out of doped regions during further MBE growth or during post-growth annealing. This behaviour would appear to prevent their use in FPA technology and hence restrict their usefulness as acceptors (with the possible exception of gold), especially for the abrupt junctions required for modern detectors with complex heterostructures.

In comparison, Group V elements have a low diffusivity which allows for the growth of stable, well controlled p-n junctions and precisely controlled dopant profiles. In recent times, the focus of p-type doping has been on *in-situ* doping with Group V elements, especially arsenic (As).^{36,51–67} In the process of As-doping, cracked As atoms, instead of uncracked As₄ molecules, are used as the doping source, since the cracked As atoms are mostly chemisorbed in atomic or diatomic form and thus have a higher sticking coefficient.⁶⁸ The use of cracked As has led to high incorporation efficiency, although it still does not consistently facilitate the dopant activation of As atoms.

Regarding As doping in HgCdTe materials, it should be noted that As is an n-type dopant in as-grown materials since it resides on the Hg/Cd lattice sites, and hence needs to be transferred to Te lattice sites - a process usually referred to as activation. In general, annealing is required to activate As as a p-dopant by transferring it to Te lattice sites. The standard activation anneal is as follows: a 10 min anneal at ~425 °C, followed by a 24 h anneal at ~250 °C under a Hg overpressure to fill the Hg vacancies created during the 425 °C anneal. The first anneal induces Te evaporation, which allows the As atoms to fill the resultant Te vacancies in the second-stage anneal. This annealing procedure yields almost complete activation of the As up to concentrations $\geq 10^{18} \text{ cm}^{-3}$ with the doping abruptly saturating when the Te vacancies created during the first-stage anneal are filled. The doping concentration depends on the first-stage annealing temperature.^{60,63,64} However, this annealing significantly negates the low-temperature-growth advantages of MBE. Therefore, attempts have been made to obtain p-type activation of As either as-grown or after only a low-temperature anneal. The most promising approach has been planar doping, in which the Hg flux is never shut off, and the As flux is shut off all the time, except periodically when the CdTe and Te fluxes are briefly shut off. This approach⁶⁹ gives full p-activation of the As either in the as-grown material^{66,69} or after anneals at ≤ 300 °C.^{56,67} Various two-stage-anneal procedures with $T \leq 300$ °C in both stages also give full activation in some cases,^{52,54,57,65} although not consistently.

Although significant progress has been made, the success of arsenic doping in HgCdTe is still limited because of (1) short τ_{SRH} lifetimes and (2) strong Hg/Cd interdiffusion during high-temperature As-activation annealing. Note

TABLE I. Possible dopants for p-type and n-type doping in HgCdTe.

	p type dopant (group V element on Te sites)	p type dopant (group I element on Hg/Cd sites)	n type dopant (group III element on Hg/Cd sites)	n type dopant (group VII element on Te sites)
Elements	N, P, As, Sb, and Bi	Li, Na, Cu, Ag, and Au	B, Al, Ga, In, and Ti	F, Cl, Br, I, and At

that such interdiffusion is enhanced with decreasing Cd composition and also by p-doping.⁷⁰ This interdiffusion presents a challenge for heterojunctions if subjected to standard As-activation annealing. Therefore, p-type doping in HgCdTe is still an unresolved issue for advanced HgCdTe detector architectures with complex structures.

To achieve efficient p-type doping in HgCdTe without high temperature ($>250^{\circ}\text{C}$) post-growth annealing, it is essential to create metal rich or Te deficient conditions, which will allow the group V atoms to occupy the Te lattice sites. In this section, three potential approaches will be discussed for addressing the p-type doping issue in HgCdTe: (1) Group V element doping under cation-rich background, (2) external energy-assisted group V element doping, and (3) full n-type device architectures.

A. Group V element doping under cation-rich background

With LPE growth, it has already been demonstrated that efficient p-type doping (both As and Sb) in HgCdTe can be achieved without high temperature post-growth annealing if the HgCdTe materials are grown under cation rich conditions.⁷¹ In contrast to LPE growth, which can be undertaken under Hg rich or Te rich conditions, the MBE growth of HgCdTe is usually undertaken under Te-rich conditions. However, cation rich MBE growth conditions can be created via Cd overpressure during MBE growth. In a U.S. patent,⁷² it is claimed that the p-type doping of an MBE-grown II-VI semiconductor can be achieved by using a Group II-V compound as the dopant with a beam equivalent pressure less than 10^{-6} Torr. Regarding the Group II-V compound dopant, the Group II material is selected from either Cd or Hg, while the Group V material can be selected from As, Sb, or P. With a group II-V compound as the dopant, metal vacancies in the lattice structure are tied up by the Group II constituent of the dopant combination, leaving the Group V dopant available to enter the Group VI sublattice and produce p-type doping. The doping concentration can be changed by controlling the MBE cell temperature of the Group II-V combination. This doping technique deserves to receive some research interest as a possible pathway to achieve efficient p-type doping without any high temperature post-growth anneal.

Note that another advantage of using a group II-V compound as a p-type dopant is that the group V element is mostly chemisorbed in atomic or diatomic form, which is similar to the situation with the use of cracked group V

elements such as As. This allows much higher (orders of magnitude) sticking coefficients for the group V atoms, and thus high dopant incorporation.¹⁶

B. External energy-assisted group V element doping

Apart from using cation rich conditions, another approach that facilitates efficient p-type doping with group V atoms is to create Te-deficient conditions during the *in-situ* doping process. As mentioned previously, the MBE growth of HgCdTe is generally carried out under Te-rich conditions. Therefore, some external energy is required to create the Te-deficient condition for efficient p-type doping with group V atoms. External photo illumination provides an effective technique to create Te-deficient conditions during MBE growth of HgCdTe. Some encouraging results have already been demonstrated in the efficient p-type doping of both CdTe and HgCdTe materials. In the work of Tiwari *et al.*,⁷³ laser illumination was undertaken during *in-situ* p-type doping of CdTe with Sb. The growth kinetics showed that laser illumination induced Te desorption such that Sb-dopants were incorporated at desorbed Te-sites. External photo-assisted MBE growth has also been used for p-type doping of HgCdTe. In the work of Antoszewski *et al.*,⁷⁴ efficient p-type doping with Sb was described for MWIR HgCdTe by using laser illumination during the MBE growth. The Sb-doped samples were grown with a Sb cracker cell and external laser illumination at CMTEK Ltd., Australia, and characterized by the research group at The University of Western Australia. A typical example (Figure 4) is a $\text{P}^{+}/\pi/\text{N}^{+}$ double-heterojunction structure consisting of three MBE-grown HgCdTe layers: a $0.51-\mu\text{m}$ -thick heavily n-type In-doped layer with Cd content $x = 0.34$, a $5.7-\mu\text{m}$ thick lightly p-type Sb-doped layer with $x = 0.2$, and a $1.51-\mu\text{m}$ -thick heavily p-type Sb-doped $x = 0.39$ layer, all grown on a CdZnTe substrate with $0.46-\mu\text{m}$ -thick $x = 0.4$ buffer layer and a thin CdTe capping layer. High-resolution mobility spectrum analysis (HR-MSA) of the as-grown $\text{P}^{+}/\pi/\text{N}^{+}$ sample (without post-growth anneal) showed that the P^{+} HgCdTe layer presents a hole concentration of $\sim 2 \times 10^{17} \text{ cm}^{-3}$ and a hole mobility of $\sim 200 \text{ cm}^2/\text{V s}$, and the lightly Sb-doped π HgCdTe layer presents a hole concentration of $\sim 2 \times 10^{15} \text{ cm}^{-3}$ and a hole mobility between $1000 \text{ cm}^2/\text{V s}$ and $2000 \text{ cm}^2/\text{V s}$.⁷⁴

Although detailed knowledge about photo-assisted p-type doping with group V elements is not complete, it presents a promising solution to efficient p-type doping in HgCdTe. The early work on this doping technique is worthy

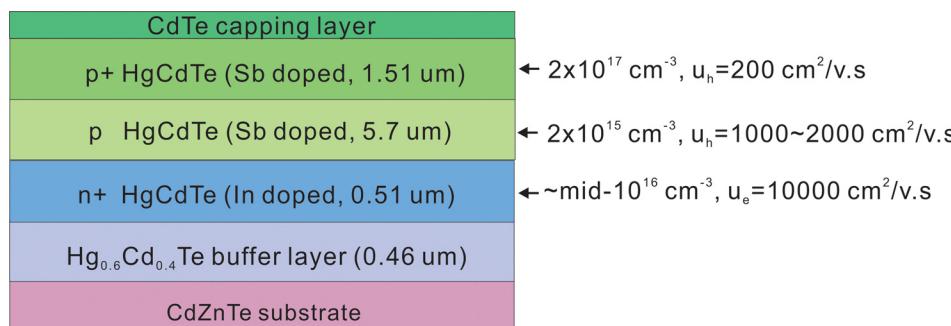


FIG. 4. Schematic structure of the Sb-doped sample studied in Ref. 74.

of being revisited. More recently, first principle theoretical calculations have been undertaken to understand the mechanism of Sb doping, which can be viewed as a new initiative in this field.⁷⁵

Note that the most critical aspect of this doping technique is to develop external approaches to create Te-deficient growth conditions. Apart from laser illumination, other external energy could also be utilized for this purpose, such as high energy electron irradiation.⁷⁶

C. Full n-type device architecture

Another potential solution to the difficulty of p-type doping in HgCdTe is to use a fully n-type detector architecture that eliminates the need for p-type doping. Recently, a new n-type-barrier-n-type (nBn) device architecture has been proposed for fabricating IR detectors, which is analogous to a photoconductor with the inclusion of a barrier in the conduction band. This new detector structure consists of two n-type layers with a high electron barrier and zero hole barrier sandwiched in-between and, thus, there is no need for p-type doping within the detector structure. The nBn detector structure was first proposed by Maimon and Wicks in 2006⁷⁷ and has been widely researched for fabricating type II superlattice IR detectors with great success.^{78–83} However, the development of nBn HgCdTe IR detectors has serious challenges due to the difficulty in achieving the zero valence band offset (hole barrier) requirement with HgCdTe materials,^{84–86} which is a necessary criterion for achieving optimum nBn detector performance. The details of nBn HgCdTe detector architectures and how to achieve an ideal structure will be discussed in Section V F. If the nBn device architecture can be successfully developed for the production of HgCdTe detectors, the p-type doping issue may finally be resolved.

IV. LOWER COST AND LARGER ARRAY FORMAT SIZE OF HgCdTe DETECTORS

A. Cost, format size, and yield issues

Two of the requirements for next generation HgCdTe IR detectors are lower cost and larger array format size. The single dominant factor that impacts on the high cost of HgCdTe-based FPAs is very low yield, particularly due to the absence of large-area, high quality, lattice matched substrates. It is generally well known, although not widely acknowledged, that the very low pixel-yield on a FPA, and the corresponding low FPA yield on a wafer, is dominated by defects resulting from the relatively low quality buffer/substrate starting materials. For current state-of-the-art HgCdTe IR technologies, high performance HgCdTe IR detectors are generally grown on lattice matched CdZnTe substrates. However, for lattice matched CdZnTe substrates, there are no suppliers of epi-ready substrates and the defect density of the substrates, in terms of EPD, is one to two orders of magnitude higher than that of other commercially available epi-ready substrates (for example, \sim low 10^3 cm^{-2} for GaAs). During epitaxial growth, these substrate defects will evolve into defects in the HgCdTe epi-layers (such as threading dislocations and point defects),

which results in “dead” pixels in the FPAs due to the excessive dark current that results whenever the pixel active area coincides with an electrically active defect. Note that a “dead” pixel is defined as a defective pixel that delivers either no signal or a signal that is out of specification. Thus, a high defect density leads to very low yield and, as a result, very high cost for current-generation HgCdTe FPAs. Apart from the cost issue, a high defect density also limits the array size of a FPA, since the probability of success in fabricating a functioning FPA decreases dramatically with increasing area.

In addition to relatively lower crystal quality, CdZnTe substrates also suffer two other limitations, these being high cost and small wafer size. For example, a piece of $1 \text{ cm} \times 1 \text{ cm}$ CdZnTe substrate costs approximately \$300, and the maximum wafer size for commercially available CdZnTe substrates is currently limited to $6 \text{ cm} \times 6 \text{ cm}$. Another disadvantage of CdZnTe substrates is that there are very few commercial suppliers that can provide high quality CdZnTe substrates. Therefore, there is a strong incentive to replace CdZnTe substrates with alternative high quality, large area, and low cost substrates in order to enhance FPA yield, increase wafer size, and thus increase the number of fully functional FPAs per wafer in order to reduce the overall cost. Apart from alternative substrates, other technologies that are also being investigated to reduce the cost and/or increase the array size of HgCdTe detectors will also be discussed in Sec. IV C.

B. Alternative substrates

Over the past two decades, several alternative substrates have been studied to replace CdZnTe for growing HgCdTe materials, such as Si, Ge, and GaAs.^{87–91} All these substrates have the features of high crystal quality (in terms of EPD), large wafer size, lower cost, and ready availability. Among them, Si as an alternative substrate has attracted more attention due to its compatibility with the Si readout circuit in a flip-chip bonded configuration. However, all these alternative substrates present a very large lattice and CTE (coefficient of thermal expansion) mismatch with HgCdTe materials. Figure 5 shows the lattice and CTE mismatch

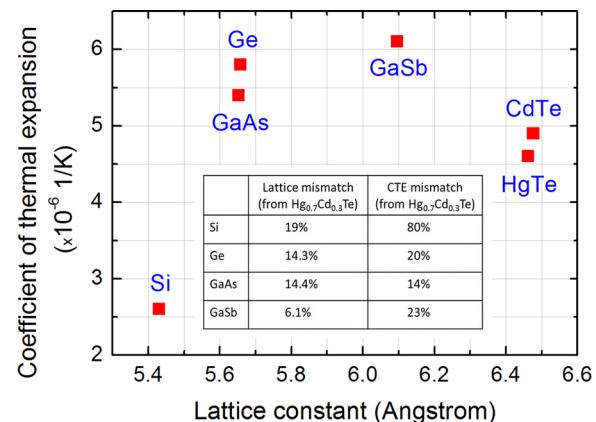


FIG. 5. Room temperature lattice constant and CTEs of several semiconductors used as substrates for HgCdTe MBE growth. The inset shows the lattice and CTE mismatch between four potential alternative substrates and HgCdTe. Reproduced with permission from Lei *et al.*, J. Electron. Mater. **43**, 2788 (2014). Copyright 2014 Springer.

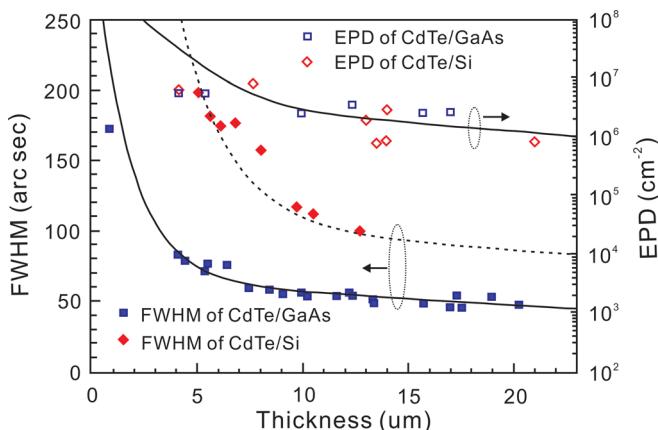


FIG. 6. XRD FWHM and EPD values for CdTe buffer layers grown on GaAs and Si in relation to CdTe buffer layer thickness. Reproduced with permission from He *et al.*, J. Cryst. Growth **301–302**, 268 (2007). Copyright 2007 Elsevier.

between HgCdTe and the substrates being discussed.⁹² The large lattice and CTE mismatch between HgCdTe and alternative substrates lead to a high defect density in the MBE-grown HgCdTe epilayers, which not only reduces the carrier mobility and lifetime (and thus degrades detector performance) but also leads to a high density of defective/dead pixels in the FPA. A common approach to reducing dislocations in the HgCdTe layer is to grow a thick CdTe buffer layer in order to relax and block the penetration of dislocations propagating from the lattice mismatched substrate/CdTe interface.^{88,90,93} Figure 6 shows the relationship between the FWHM of the XRD peak of the CdTe buffer layer as a function of the CdTe buffer layer thickness.⁹⁰ It can be observed that a CdTe buffer layer with an appropriate thickness ($>10\text{ }\mu\text{m}$) can effectively block the penetration of dislocations, leading to high crystal quality of the CdTe buffer layer grown on Si (XRD FWHM $\sim 60\text{ arc sec}$). For Si alternative substrates, a ZnTe nucleation layer and an As passivation layer are also applied to suppress the formation of micro-twin defects and to improve the crystal quality of the CdTe buffer layer and the subsequently grown HgCdTe epilayer.^{17,90} Apart from a CdTe buffer layer, other technologies have also been studied to reduce the dislocation density in HgCdTe epilayers, including thermal cyclic annealing, dislocation gettering, compliant substrates, and selective-area growth on nanopatterned substrates.

Thermal cyclic annealing has been demonstrated to be effective in reducing the dislocation density in the CdTe

buffer layer and HgCdTe layers grown on alternative substrates.^{93–96} Figure 7 shows the XRD FWHM and EPD values of MBE-grown HgCdTe/CdTe/Si epilayers after various cycles of post-growth annealing (each cycle represents 5 min of annealing at 400°C). After cyclic thermal annealing, the XRD FWHM can be reduced from 90 arc sec to 50 arc sec , and the EPD can be reduced from $6 \times 10^6\text{ cm}^{-2}$ to $8 \times 10^5\text{ cm}^{-2}$, indicating improved crystal quality.⁹⁴ Dislocation densities as low as $2.3 \times 10^5\text{ cm}^{-2}$ have been reported for HgCdTe layers grown on GaAs alternative substrates with post-growth cyclic thermal annealing between 300 and 490°C , which is almost as low as those obtained for HgCdTe layers grown on CdZnTe.⁹⁶ It should be noted that although this post-growth annealing is very effective in reducing the dislocation density and improving the material quality, it suffers a major limitation due to interdiffusion of elements, which degrades the sharpness of hetero- and homojunctions required for advanced detector designs.

Apart from thermal cycle annealing, reticulated structures can also be used to getter dislocations and thus reduce dislocation density within the optically active regions of HgCdTe layers grown on alternative substrates.^{97–99} In the work of Stoltz *et al.*,¹⁰¹ mesa structures were produced on HgCdTe layers (grown on CdTe/Si) with near-vertical side-walls by using plasma etching and then subjected to four thermal cycle anneals between 494°C and 250°C . During the annealing, the reticulated surfaces enable stress-free regions for dislocations to glide to these edges produced by plasma etching and enable the movement of deleterious dislocations, thereby allowing the reduction of dislocations within the HgCdTe device active areas. Using this technique, the EPD for HgCdTe layers grown on Si was reduced from $1.1 \times 10^7\text{ cm}^{-2}$ to $3.35 \times 10^5\text{ cm}^{-2}$, rendering the EPD of HgCdTe layers grown on this highly lattice mismatched substrate comparable to that of HgCdTe grown on lattice matched CdZnTe.

Growth on compliant substrates and selective-area growth on nanopatterned substrates present two other possible approaches to reducing the dislocation density in CdTe and HgCdTe layers grown on alternative substrates.¹⁷ A compliant substrate is one that is made much thinner than the epilayer grown upon it and that is free to slide against a thicker “handle” substrate.¹⁰⁰ The most common example of a compliant substrate is the Si-on-insulator (SOI) structure with a Si layer $\sim 10\text{ nm}$ thick floating on a SiO_2 layer on a Si handle wafer. Such SOI compliant substrates were used for growing SiGe epilayers with significant success.^{101,102}

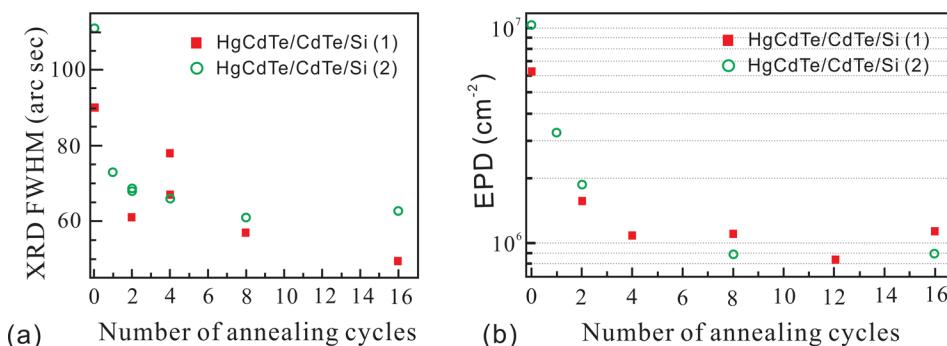


FIG. 7. (a) XRD FWHM and (b) EPD values for MBE-grown HgCdTe/CdTe/Si epilayers *vs* post-growth annealing cycle. Note each cycle represents 5 min of annealing at 400°C . Reproduced with permission from Farrell *et al.*, J. Electron. Mater. **39**, 43 (2010). Copyright 2010 Springer.

TABLE II. Typical XRD FWHM and EPD values for CdTe and HgCdTe epilayers grown on CdZnTe, Si, and GaAs substrates reported in Ref. 110. Reproduced with permission from Benson *et al.*, J. Electron. Mater. **41**, 2971 (2012). Copyright 2012 Springer.

As-grown (211) B	CdZnTe substrate	HgCdTe/CdZnTe	CdTe/Si	HgCdTe/Si	CdTe/GaAs	HgCdTe/GaAs
XRD FWHM (arc sec)	8	12	50	80	30	80
EPD (cm^{-2})	5×10^4	3×10^4	5×10^6	4×10^6	2×10^6	2×10^6

However, the study of growth of CdTe on such substrates has only recently commenced,¹⁰³ and more effort is needed in this area if it is to be developed as an alternative substrate technology. Selective-area growth on nanopatterned substrates has been quite successful for MOCVD growth of various epilayers on substrates with large lattice mismatch, such as GaAs on Si (4% lattice mismatch),¹⁰⁴ GaN on Si (22% mismatch),^{104–106} and CdTe on Si (19% mismatch).^{107,108} The epilayers obtained via selective-area growth exhibit much lower dislocation density in comparison to those grown using standard planar growth. MBE selective area epitaxy of CdTe on nanopatterned Si substrates was recently studied and resulted in some promising results.¹⁰⁹ However, more effort is needed in these two approaches before any meaningful results can be achieved.

Due to intensive study over the past two decades, significant advance has been achieved in growing HgCdTe on Si, Ge, and GaAs alternative substrates, with Table II summarizing the material quality of CdTe and HgCdTe grown on CZT, Si, and GaAs substrates.^{90,110} Obviously, there is still a substantial gap between the material quality of CdTe and HgCdTe grown on alternative substrates compared to epilayers grown on CZT, especially long-wave HgCdTe materials. Despite this, Si, Ge, and GaAs alternative substrates have been used for producing MWIR HgCdTe detectors and their FPAs with performance comparable to those grown on CZT substrates. However, the performance of LWIR HgCdTe detectors and their FPAs grown on alternative substrates is still much lower than those on CZT. This is mainly manifested in higher dark currents due to the large number of dislocations existing in the device structures caused by the large lattice and CTE mismatch between HgCdTe and these alternative substrates.^{90,91,110} Therefore, in order to address these problems, and further enhance the device performance of HgCdTe detectors, it is highly desirable to develop new alternative substrate technologies with better matching of both lattice constant and CTE to the corresponding values for HgCdTe.

Most recently, GaSb has been proposed as a new alternative substrate for growing high quality HgCdTe materials

for next generation IR detectors, given that epi-ready high quality substrates are now readily available in large wafer sizes.⁹² As shown in Fig. 5, GaSb presents a much smaller lattice constant mismatch with HgCdTe compared with Si, Ge, and GaAs. In addition, the CTE mismatch between GaSb and HgCdTe (23%) is also much smaller than that between Si and HgCdTe and is comparable to that between HgCdTe and both Ge and GaAs. Therefore, in principle, GaSb provides a better choice as an alternative substrate for the epitaxial growth of CdTe/HgCdTe epitaxial layers for IR detector applications. As shown by the experimental work from Teledyne and RDECOM,⁸⁸ reduced lattice mismatch between the CdTe buffer layer and substrate can facilitate an improvement in the crystal quality of the buffer layer and the subsequent HgCdTe layer, and the dislocation density nucleated in the buffer layer will act as the lower limit on the ultimate dislocation density achievable in the subsequently grown HgCdTe layer. For example, when the lattice mismatch with HgCdTe decreases from 19% for Si to 14.4% for GaAs, the dislocation density in as-grown HgCdTe epitaxial layers was found to decrease from $1.8 \times 10^7 \text{ cm}^{-2}$ for Si to $4 \times 10^6 \text{ cm}^{-2}$ for GaAs.⁸⁸ Thus, the smaller lattice mismatch of 6.1% for GaSb should significantly drive down the dislocation density to meet the dislocation density criteria for fabricating high performance LWIR detectors (less than $5 \times 10^5 \text{ cm}^{-2}$).⁸⁷ And, indeed, for GaSb on GaAs heterostructures with a similar lattice mismatch of 7.8%, a dislocation density less than 10^5 cm^{-2} has already been demonstrated.¹¹¹

Since GaAs alternative substrates are also III-V based materials, have been developed for more than two decades, and have been utilized for manufacturing MWIR HgCdTe detectors, a direct comparison of the main wafer characteristics between GaAs and GaSb will provide a direct indication as to whether or not GaSb alternative substrates are feasible. Table III compares the main characteristics of commercially available GaAs and GaSb substrates, which clearly indicates that GaSb substrates have similar IR transmission and commercial availability to GaAs substrates, although GaSb substrates have better material quality in terms of narrower XRD FWHM, as well as lower EPD values. Note that

TABLE III. Main characteristics of GaAs and GaSb as alternative substrates for growing HgCdTe. Reproduced with permission from Lei *et al.*, J. Electron. Mater. **43**, 2788 (2014). Copyright 2014 Springer.

(211)B wafer	XRD FWHM (arc sec) ^a	EPD (cm^{-2}) ^b	IR transmission (%) ^c	Max. diam. (in.) ^d	Unit price (USS for 2 in. wafer)
GaAs	24–30	<5000	48–55	6	~150
GaSb	20–25	<3000	47–52	4	~550

^aFor omega scan (according to Wafer technology, UK).

^bFrom Wafer technology, UK.

^cFor 2–15 μm wavelength range (according to Wafer technology, UK).

^dSome manufacturers can provide even large size wafers.

TABLE IV. Selected material characteristics for MBE-grown CdTe buffer layers on GaAs and GaSb substrates at UWA. Reproduced with permission from Lei *et al.*, J. Electron. Mater. **43**, 2788 (2014). Copyright 2014 Springer.

Alternative substrate	CdTe buffer layer thickness (μm)	XRD FWHM (arc sec)	RHEED pattern during CdTe buffer layer growth	Etch pit density ($\times 10^6 \text{ cm}^{-2}$)
GaAs	6–7	60–75	Long and uniform streaks	3–50
GaSb	3–7	55–71	Long and uniform streaks	5–30

although GaSb substrates are of relatively higher cost than GaAs, a smaller lattice mismatch will allow the growth of HgCdTe materials with higher crystal quality than GaAs can provide, which will not only make low cost and large format LWIR FPAs possible, but further drive down the cost of MWIR FPAs due to higher FPA yield. Therefore, GaSb substrates have the potential to become an alternative substrate technology for the growth of HgCdTe epitaxial layers.

Recent effort on MBE growth of CdTe buffer layers directly on GaSb substrates has demonstrated that CdTe buffer layers on GaSb substrates can provide material quality comparable to CdTe on GaAs substrates. Table IV presents some characteristics of CdTe buffer layers grown on both GaSb and GaAs substrates, demonstrating comparable crystal quality and defect density.⁹² Note that the main material characteristics of the CdTe buffer layers grown on GaAs at UWA are comparable to those of state-of-the-art CdTe buffer layer technology on GaAs reported recently.^{89,112,113} Figure 8 shows representative XRD rocking curves and surface images (after EPD etching) of CdTe buffer layers on GaSb and GaAs substrates. As observed, even such preliminary data indicate that high quality CdTe buffer layers can be grown on GaSb substrates.

HgCdTe epilayers have been grown on these CdTe/GaSb substrates despite the fact that the growth conditions

of CdTe buffer layers on GaSb had not been fully optimized. Table V shows selected statistical material characteristics of HgCdTe epilayers grown on both CdTe/GaSb and CdTe/GaAs substrates.¹¹⁴ Generally, HgCdTe layers grown on GaSb substrates demonstrate material quality comparable to those on GaAs substrates developed at UWA in terms of reflection high-energy electron diffraction (RHEED) pattern during material growth, XRD FWHM, and EPD. These results are extremely encouraging considering this is a recent effort, and much higher quality CdTe buffer layers and HgCdTe layers are expected on GaSb by optimizing their growth conditions and using proper post-growth annealing.

C. Small pixel technology

Apart from alternative substrates, which can provide an increase in wafer size and thus array format size, as well as an increased number of FPAs per wafer, another approach to increasing array format size is to reduce pixel size. With smaller pixel area, more FPAs can be processed out of a single HgCdTe wafer, thus also reducing the FPA cost. Smaller pixel size is a long-term goal of the IR community. The pixel size can be described using either a linear measurement or an area measurement. A linear measurement that is approximately the width of a pixel is usually termed the pixel pitch.

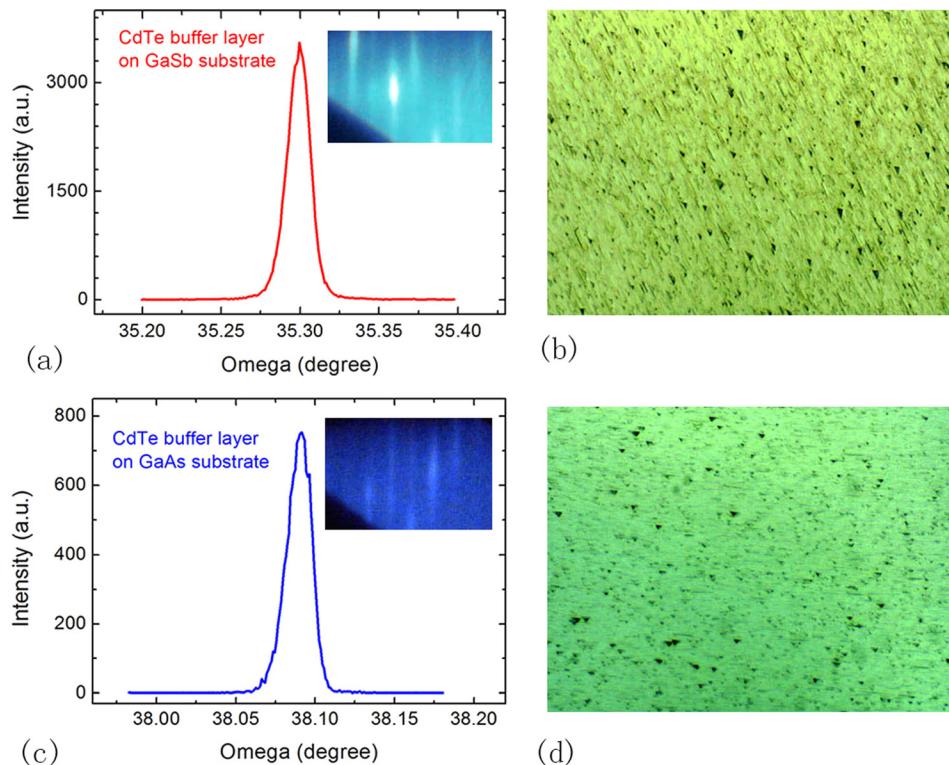


FIG. 8. Representative XRD rocking curves and surface images (after EPD etching) of CdTe buffer layers on ((a) and (b)) GaSb and ((c) and (d)) GaAs substrates grown at UWA via MBE. Insets of (a) and (c) show representative RHEED patterns during the growth of CdTe buffer layers on GaSb and GaAs, respectively. The size of images (b) and (d) is $95 \mu\text{m} \times 65 \mu\text{m}$. Reproduced with permission from Lei *et al.*, J. Electron. Mater. **43**, 2788 (2014). Copyright 2014 Springer.

TABLE V. Selected material characteristics for MBE-grown HgCdTe layers on GaAs and GaSb substrates at UWA. Reproduced with permission from Lei *et al.*, J. Electron. Mater. **44**, 3180 (2015). Copyright 2015 Springer.

Alternative substrate	x value of $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ layer	HgCdTe layer thickness (μm)	CdTe buffer layer thickness (μm)	XRD FWHM (arc sec)	RHEED pattern during HgCdTe layer growth	Etch pit density ($\times 10^6 \text{ cm}^{-2}$)
GaSb	0.27–0.32	4.5–5.3	5.3–5.7	122–139	Long and uniform streaks	2–10
GaAs	0.26–0.32	5.7–6.7	5.7–6.7	98–155	Long and uniform streaks	8–40

For a given wafer size, the pixel density or array format size is proportional to the inverse of the square of the pixel pitch. Therefore, a reduction in the pixel pitch by half will result in a fourfold increase in pixel density/array format size.

Since the invention of HgCdTe photoconductors and photodiodes, the device processing technology has advanced rapidly, and the detector pixel size has decreased significantly from over $50 \mu\text{m}$, to $30 \mu\text{m}$, and to the current state-of-the-art $15 \mu\text{m}$. In the past several years, the fabrication technology with $15 \mu\text{m}$ pixel size has also become standard and has been commercialized via industrial production of HgCdTe FPAs by companies such as Teledyne, DRS, AIM, and Leti-Sofradir.^{14,115,116} Most recently, there has been a strong drive to develop FPAs with pixel size approaching the optical wavelength scale (Nyquist limit). This impetus is initiated by the US Advanced Wide FOV Architecture for Image Reconstruction and Exploitation (AWARE)-Lambda Scale detector program, which was proposed by Dr. Nibir Dhar of the Defense Advanced Research Projects Agency (DARPA). In that program, detector pixel size is proposed to be reduced to $5 \mu\text{m}$ for LWIR and MWIR HgCdTe detectors.^{19,117,118} Such small pixel sizes will significantly increase pixel density and thus array format size, resulting in better image quality and improved image resolution.

With current semiconductor processing technology such as high resolution lithography and dry etching, the fabrication of FPAs with pixel pitch down to $5 \mu\text{m}$ is readily achievable. For example, DRS has demonstrated full size 1280×720 pixel MWIR and LWIR HgCdTe FPAs with pixel size of $5 \mu\text{m}$.¹¹⁸ Like Si CMOS FPAs, it is expected that the pixel pitch will be reduced further in the future. Though it is not a challenge to fabricate small pixels with current semiconductor processing technology, the real challenge with this small pixel technology is how to maintain the FPA performance while reducing the pixel size. In particular, lower quantum efficiency and higher cross-talk between pixels present two serious challenges with decreasing pixel pitch. Other challenges and requirements, such as interconnect density and high charge capacity of the ROIC, will be not covered here and will be discussed elsewhere.

With reduced pixel size, the material volume (especially absorber region) of each detector element is reduced significantly, which decreases the detector quantum efficiency and thus degrades the array image quality. Generally, there are two approaches to maintain the quantum efficiency while reducing pixel size: (1) maintaining a sufficiently thick HgCdTe absorption layer; and (2) developing a photon-trapping technology. Because a thicker HgCdTe absorption layer is not beneficial for reducing the dark current of HgCdTe detectors,^{119–121} the more appropriate approach is a

photon trapping technology, which is also an important approach to reducing dark current and enhancing the detector operating temperature, which will be discussed in detail in Section V E.

Crosstalk is a phenomenon that occurs when an optical signal impinging on one circuit is received or causes an undesirable effect in another circuit or channel, including both optical and electrical cross-talk.¹²² For low-doped n-type HgCdTe materials, the minority-carrier diffusion length is of the order of $30 \mu\text{m}$ to $50 \mu\text{m}$, much longer than the targeted pixel pitch ($5 \mu\text{m}$), which can cause significant cross-talk between pixels.¹⁹ How to suppress cross-talk? The fundamental idea is to confine the light electromagnetic wave/carriers well within the pixels, and thus isolate pixels from each other, promoting in-pixel signal collection. Some techniques can be applied to suppress cross-talk in FPAs with small pixels, including micro-lens integration,¹²³ photon trapping structures, proper mesa isolation, and proper design of device geometry and layer structure (e.g., composition, doping, and layer thickness).¹²² For example, pillar-array photon trapping structures were found to be effective in reducing the electrical cross-talk in small pixel ($6 \mu\text{m}$ pixel size) HgCdTe photovoltaic arrays.¹²⁴ Though some progress has been made in suppressing cross-talk in small pixel FPAs, the challenge will become more and more serious with further reduction in pixel size. Thus, more effort is needed to develop an appropriate technique to suppress cross-talk in small pixel HgCdTe FPAs.

V. HIGHER OPERATING TEMPERATURE (HOT) HgCdTe DETECTORS

A. Dark current and operating temperature

Dark current mechanisms: One of the primary limitations of current HgCdTe IR technology is the requirement for low operating temperatures (usually $\sim 77 \text{ K}$), to reduce the high dark current density that is inherent in all narrow bandgap detectors. Figure 9 illustrates the main dark current mechanisms in a reverse-biased HgCdTe photodiode,¹ which can be classified into two groups:

- (1) inherent mechanisms, which depend only on the intrinsic material properties:
 - (a) diffusion current due to Auger or radiative recombination in the n-region or p-region,
 - (b) band-to-band tunnelling current,
- (2) defect-related mechanisms which require surface or bulk defects located within the depletion region or within a diffusion length of either side of the depletion region:

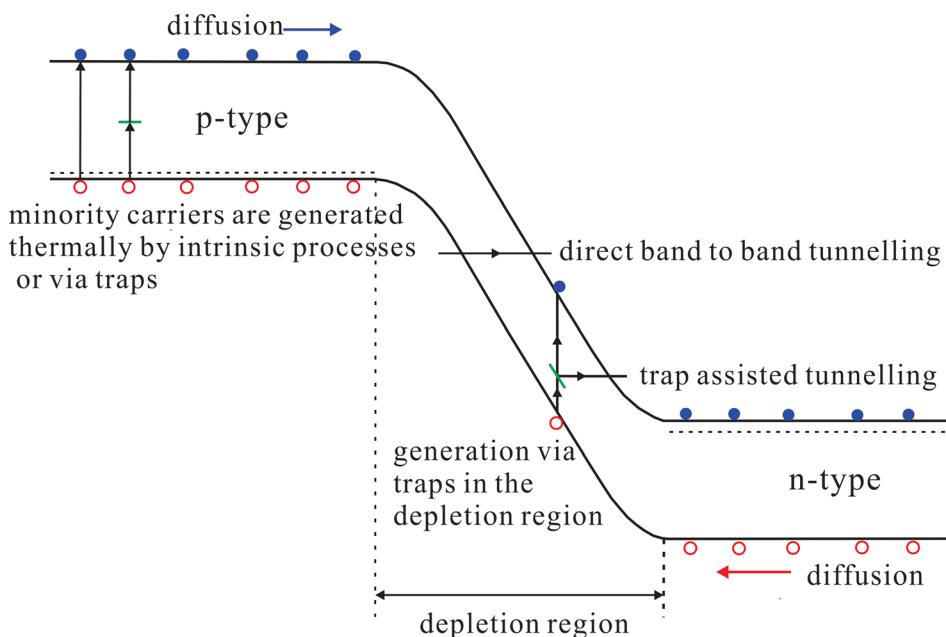


FIG. 9. Energy band diagram illustrating the main dark current mechanisms for a reverse-biased HgCdTe photodiode. Reproduced with permission from A. Rogalski, Rep. Prog. Phys. **68**, 2267 (2005). Copyright 2005 IOP Publishing.

- (a) diffusion current due to SRH recombination in the n-region or p-region,
- (b) generation–recombination within the depletion region,
- (c) trap-assisted tunnelling,
- (d) surface generation current from surface states.

Rule 07: Before discussing approaches to suppress and eliminate these dark current mechanisms, it is essential to evaluate ideal HgCdTe detector behaviour in terms of dark current performance, which can serve as a reference for discussing the

performance of real HgCdTe detectors. In the HgCdTe community, the “Rule 07” relationship is widely used to evaluate state-of-the-art HgCdTe dark current performance, which is an empirical relationship and valid for a wide range of dark currents (over 13 orders of magnitude), a broad range of cut-off wavelength (from SWIR to LWIR), and a wide temperature range (from room temperature to liquid nitrogen temperatures).^{125,126} The “Rule 07” relationship describes the saturation dark current density of an ideal HgCdTe detector which is a diffusion-limited diode device. The “Rule 07” relationship can be described as follows:^{125,126}

$$J = J_0 e^{C \left(\frac{1.24q}{k\lambda_e T} \right)}, \text{ where}$$

$$\lambda_e = \lambda_{cutoff}$$

$$\text{for } \lambda_{cutoff} \geq \lambda_{threshold}$$

$$\lambda_e = \lambda_{cutoff} / \left(1 - \left(\frac{\lambda_{scale}}{\lambda_{cutoff}} - \frac{\lambda_{scale}}{\lambda_{threshold}} \right)^{Pwr} \right) \text{ for } \lambda_{cutoff} < \lambda_{threshold},$$

where $J_0 = 8367 \text{ A/cm}^2$, $Pwr = 0.5441$, $C = -1.1624$, $\lambda_{scale} = 0.2008 \mu\text{m}$, $\lambda_{threshold} = 4.6351 \mu\text{m}$, k is Boltzmann’s constant ($1.3802 \times 10^{-23} \text{ J/K}$), and q is the electronic charge ($1.6021 \times 10^{-19} \text{ C}$).

The dark current density given by “Rule 07” represents the saturation dark current density of an ideal diffusion limited HgCdTe diode. Therefore, one of the main aims of current HgCdTe research is to achieve a saturation dark current density approximating the Rule 07 relationship for a given HgCdTe detector with a particular cut-off wavelength at a given temperature. Figure 10 shows the saturation dark current density of the best HgCdTe detectors fabricated by Teledyne Imaging Sensors against Rule 07 as reported in Ref. 126.

Operating temperature issue: For a single element detector, the most important performance parameter for sensing applications is detectivity, which represents the signal-to-noise ratio. However, for an FPA the most important performance parameter for imaging application is the noise-equivalent temperature difference (NETD) and the associated pixel uniformity. NETD, the temperature difference which would produce a signal equal to the average noise signal of a FPA, is an important attribute for evaluating image quality and detection range (the ability to see smaller objects at greater distances in all weather conditions). An FPA with better NETD performance is more apt at detecting slight differences in temperature between objects, which provides more details and more accurate images, and is essential in

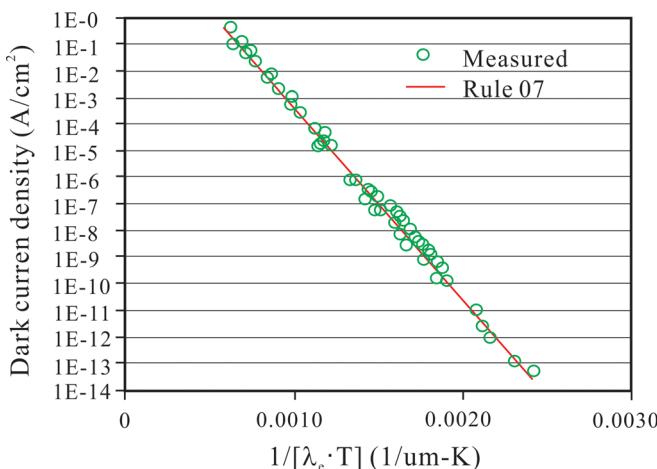


FIG. 10. Dark current density of HgCdTe diodes measured at Teledyne Imaging Sensors in comparison to the Rule 07 relationship. Reproduced with permission from W. E. Tennant, J. Electron. Mater. **39**, 1030 (2010). Copyright 2010 Springer.

various IR applications. However, the NETD of a FPA is heavily affected by the dark current.

At low temperatures, the dark current is dominated by the diffusion limited dark current component, while at high temperatures the dark current is dominated by defect-related dark current components. With increasing operating temperature, more and more defects become electrically active, leading to a significant increase of the dark current, which changes the NETD distribution of a FPA. Figure 11 shows the NETD histograms of a 640 × 512 MWIR ($\lambda_{\text{cut-off}} = 5.3 \mu\text{m}$ at 80 K) HgCdTe FPA with a pixel size of 15 μm fabricated by CEA-LETI/Sofradir.¹²⁷ It is observed that at a low temperature such as 88 K, the NETD distribution has a Gaussian distribution. However, with increasing temperature, a tail starts to appear on the high NETD side of the distribution. This causes some pixels to be out of specification, thus lowering the FPA operability and pixel uniformity. Note that the operability is defined as the number of pixels with NETD value less than two times the mean NETD. At 88 K, the operability is equal to 99.9%, with a mean NETD value of 11.7 mK and a dispersion of 1.28 mK, which means that only 327 pixels are out of range. As the operating temperature increases, the mean NETD remains stable below 11.8 mK for FPA temperatures between 88 K and 130 K, and slightly increases to 13.2 mK at 150 K.

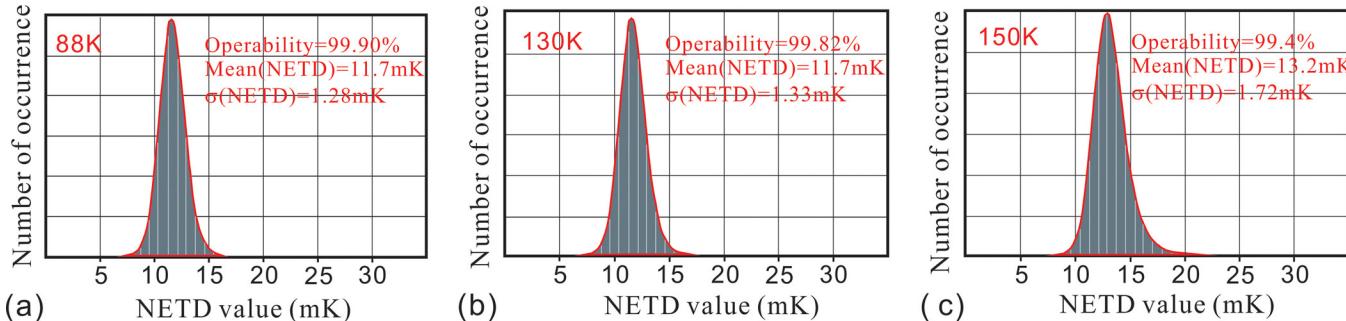


FIG. 11. NETD histograms of p-on-n MWIR FPAs (fabricated by CEA-LETI/Sofradir) operating at different temperatures: (a) 88 K, (b) 130 K, and (c) 150 K. Reproduced with permission from Mollard *et al.*, J. Electron. Mater. **43**, 802 (2014). Copyright 2014 Springer.

operability was greater than 99.8% between 88 K and 130 K, corresponding to only 650 out-of-range pixels. At 150 K, the operability is reduced to 99.4%, corresponding to 1960 out-of-range pixels, with a dispersion of 1.72 mK. With further increases in operating temperature, additional pixels will be out of specification. These out-of-range pixels are referred to as defective pixels and are caused by the high dark current flowing through the devices as a consequence of defects in the HgCdTe material. Such an increase in the number of defective pixels with increasing temperature is also consistent with measurements on a 640 × 512 MWIR HgCdTe FPA with a pixel pitch of 15 μm fabricated at AIM,¹²⁸ as shown in Figure 12.

As discussed above, the increasing number of defective pixels with increasing temperature due to high dark current seriously limits the operating temperature of HgCdTe detectors and their FPAs. To reduce the number of defective pixels and thus enhance the operating temperature, part or all of the defect-related dark current mechanisms shown in Figure 9 must be suppressed or eliminated. Therefore, any approaches which can suppress or eliminate one or more of these dark current mechanisms will be helpful in reducing defective pixels and enhancing the operating temperature of FPAs. Since defects in the material play a critical role in determining the device dark current, especially at high temperatures, there is a strong incentive to reduce and eliminate the impact of defects to achieve higher operating temperature. Generally, there are two possible approaches: one is to improve growth and post-growth processing techniques to reduce the defect density, and even eliminate the defects; the other is to develop new detector device architectures which are less sensitive to the presence of defects. Some specific approaches will be discussed in Secs. V B–V F, including p-on-n device architectures, high quality passivation, dislocation reduction in detector structures, material volume reduction in detector structures, and barrier detectors.

B. p on n device architecture

As discussed in Section II B, for backside-illuminated HgCdTe photodiode detector technologies, there are two main device architectures: n-on-p or p-on-n (either planar or mesa isolated). For these devices, the absorption layer (p- or n-type, respectively) is sandwiched between the substrate and a highly doped thin contact layer (n⁺- or p⁺-type,

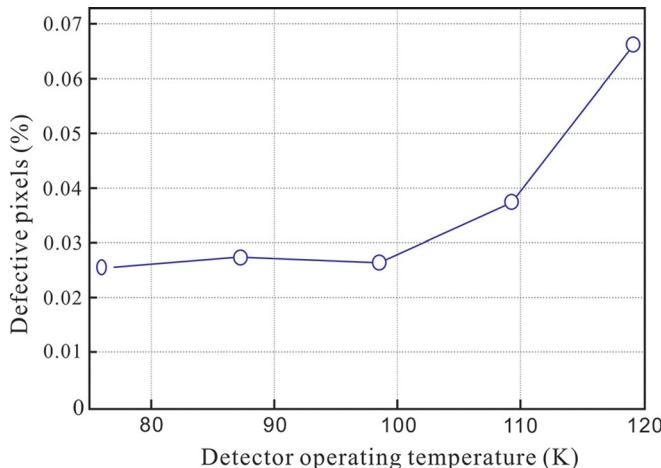


FIG. 12. Percentage of defective pixels in a 640×512 MWIR HgCdTe FPA (fabricated by AIM) operating at different temperatures. Reproduced with permission from Breiter *et al.*, Opt. Eng. **50**, 061010 (2011). Copyright 2011 SPIE.

respectively), which is obtained by ion implantation or extrinsic impurity doping. The n-on-p detector structure is the diode technology that was developed in the early days and has been used for industrial mass production for decades (see DRS, Sofradir, AIM, etc.^{1,129,130}). As described in Ref. 127, n-on-p photodiodes can be formed in p-type bulk-grown material using Hg vacancies as acceptors, and n+-type doping can be obtained by boron-ion implantation. During implantation, Hg atoms diffuse inwards, annihilate Hg vacancies, and form an n-region beneath the n+ implanted layer. This n-on-p architecture has been used for fabricating HgCdTe detectors covering all spectral ranges from SWIR to VLWIR with great success. However, the use of Hg vacancies (V_{Hg}) as the p-type dopant in the active layer is known to degrade the minority carrier lifetime, and the resulting detector exhibits higher dark current than for the case of extrinsic p-type doping.

To reduce the dark current, a backside illuminated p-on-n detector architecture was proposed around the mid-1980s.²⁰ In the subsequent two decades, the p-on-n detector technology was developed and is now used for industrial production. In the p-on-n detector technology, the n-type absorber layer is indium (In)-extrinsically doped, and the minority-carrier lifetime is governed by Auger-1 recombination due to the lower minority-carrier diffusion length (lower mobility of holes) in the n-type region of p+-on-n junctions with a thick n-type absorber region. Also, the diffusion-limited R_0A product of such junctions is larger than for n+-on-p devices, which is shown in Figure 13. Thus, the p-on-n architecture allows improved operability at a higher temperature. Such a p-on-n detector structure has become the mainstream device architecture for HgCdTe IR detectors with the application of advanced epitaxial methods, such as MBE and MOCVD, which makes *in-situ* p-type extrinsic doping easier. In recent years, both planar and mesa/trench p-on-n detectors have been developed and mass produced in organizations around the world, including the USA and France.^{1,127,131} For example, such p+-on-n detector structures were developed and used for fabricating both MWIR

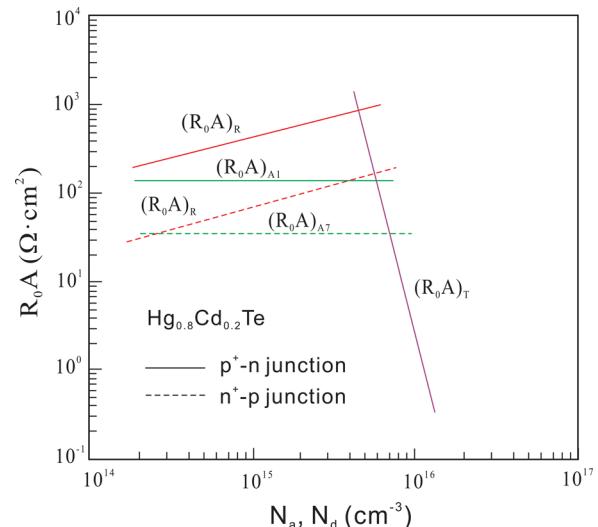
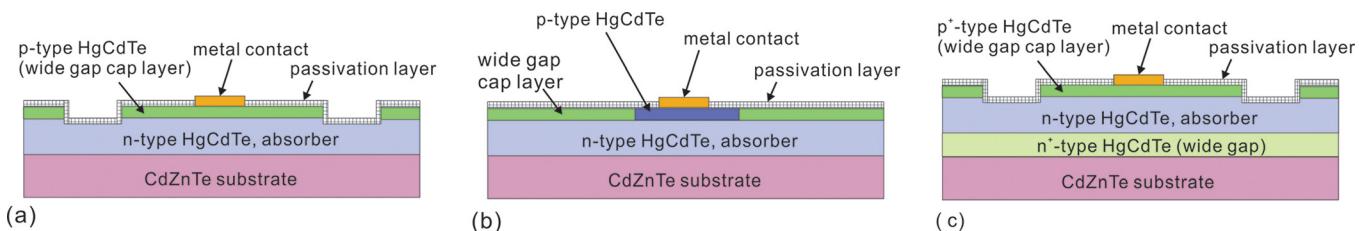


FIG. 13. R_0A product component (due to diffusion current with radiative $(R_0A)_R$ and Auger processes $(R_0A)_A$, and due to band to band tunnelling $(R_0A)_T$) vs dopant concentration for a one-side abrupt junction produced in LWIR $Hg_{0.8}Cd_{0.2}Te$. Reproduced with permission from A. Rogalski, Rep. Prog. Phys. **68**, 2267 (2005). Copyright 2005 IOP Publishing.

and LWIR FPAs at CEA-Leti,¹²⁷ which demonstrated enhanced operating temperature in comparison to n-on-p detectors. Their MWIR HgCdTe p+-on-n detector arrays have demonstrated an operating temperature as high as 150 K (with an operability of 99.4%), while their LWIR HgCdTe arrays can operate at temperatures as high as 110 K (with an operability of 99.5%).

Apart from standard p+-on-n detector structures, some extended p+-on-n concepts were also proposed for HgCdTe IR detectors, especially LWIR detectors, such as double-layer heterojunction (DLHJ),^{131,132} double layer planar heterostructure (DLPH),^{132,133} and non-equilibrium P+/v/N+ detectors.¹³⁴ In a DLHJ p+-on-n structure (see Figure 14(a)), the base n-type layer is sandwiched between the CdZnTe substrate and the wider-gap regions, which can significantly reduce the thermal leakage currents.^{131,132} The DLPH design (see Figure 14(b)) was introduced to eliminate the sidewall leakage observed in etched mesa devices and to reduce the contributions of surface defects.^{132,133,135} In a non-equilibrium P+/v/N+ design (see Figure 14(c)), the middle, lightly n-type-doped (v active) region acts as an absorber contacted by heavily doped, wider bandgap regions. When reverse biased, this P+/v/N+ design reduces the carrier concentration in the central absorber layers well below thermal equilibrium and, thus, suppresses Auger processes and effectively reduces the dark current.¹³⁴ Therefore, such “extracted” devices can operate at higher temperatures for the same detector sensitivity, in comparison to standard photodiodes at lower temperatures.

As noted above, though significant progress has been made in the development of p+-on-n detectors, the operating temperature of current p+-on-n HgCdTe FPAs is still much lower than 250 K. Therefore, further effort is needed to extend the concept and optimize the design to achieve even higher operating temperature *via* optimized doping and band-gap engineered structures.

FIG. 14. Schematic structures for (a) DLHJ, (b) DLPH, and (c) P⁺/v/N⁺ p-on-n HgCdTe detectors.

C. Passivation

Defect-related dark current mechanisms constitute a major component of the dark current in HgCdTe detectors, including diffusion current due to SRH recombination in the n-region and p-region, generation–recombination within the depletion region, trap-assisted tunnelling, and surface generation current arising from surface traps. To reduce the dark current and increase the detector operating temperature, it is essential to suppress these defect-related dark current mechanisms, in which passivation plays a critical role. In general, depending on whether the defects are located at the semiconductor surface or are located in the bulk, there are two different passivation approaches: one is surface passivation, which is targeted at reducing surface/interface defect recombination centres and interface trapped charges; the other is bulk passivation, which is targeted at passivating bulk defect recombination centres. With proper passivation, defect-related dark current mechanisms can be suppressed significantly, resulting in improved operating temperature. In addition, surface passivation also improves the thermal and chemical stability of the device. Note that in comparison to photoconductors, passivation of photodiodes is much more critical, since the same thin film layer must stabilize simultaneously regions of n and p-type conductivity, as well as depleted regions with high built-in electric field. The passivation of p-type materials is even more challenging due to its tendency for surface type inversion.¹³⁶

Surface passivation: Surface passivation of HgCdTe detectors has been studied for several decades, and various passivation techniques have been developed. In general, there are three classes of passivation technologies: native films (oxides, sulfides, fluorides), deposited dielectrics (ZnS, SiO_x, SiN_x, polymers), and *in-situ* grown wide bandgap material (CdTe and CdZnTe) acting as the passivant.¹³⁶

Initially, native films such as anodic oxide were developed for passivating HgCdTe photoconductors. However, this native film passivation technology has limitations.¹³⁶ For example, the anodic oxide, which can effectively passivate n-type photoconductors, is not useful for passivating p-type regions since it results in the formation of inversion layers. In addition, due to the large fixed positive charge, anodic oxides of HgCdTe are not suitable for photodiode devices. Low temperature grown native films, although presenting good interface properties with HgCdTe, have problems of porosity and adherence to the HgCdTe surface and therefore have not been used widely in industrial production. Later, the focus shifted to passivating photodiodes with dielectric films such as ZnS, SiO_x, and polymers. However,

these dielectric films also suffer from some limitations. For example, the excellent surface properties of silicon oxide passivation could not be maintained when the device was heated in vacuum for extended periods of time, a procedure required for good vacuum packaging integrity.¹³ Also surface charge build up was created when operating in a space-radiation environment. ZnS, a common antireflection coating for HgCdTe photoconductors, was used with intermittent success, but also lacked stability during vacuum baking.^{13,137}

Recent efforts have focused primarily on passivation with wide bandgap II-VI materials, such as CdTe. Among all the passivation materials that have been studied thus far, cadmium telluride (CdTe) is now established as the most advantageous material because it has high resistivity and is near lattice-matched with HgCdTe, which reduces dangling bonds.^{138–141} It also has good chemical compatibility with HgCdTe, is mechanically more robust than HgCdTe, and is transparent to IR radiation. CdTe passivation is also stable during vacuum packaging bake cycles and shows little effect from the radiation found in space applications. Due to these favourable features, CdTe has become the most important and widely used passivant for HgCdTe IR detectors.¹⁴² For CdTe surface passivation of HgCdTe detectors, low temperature is required for passivation layer deposition to prevent mercury depletion from the surface. Hence, conventional methods such as vacuum evaporation at room temperature are typically used for CdTe deposition on planar detectors.¹⁴³ With the increase in complexity of detector structures, other methods of deposition such as chemical vapor deposition (CVD) and atomic layer deposition (ALD) have attracted increased attention for their potential to obtain improved conformal coverage for high-aspect-ratio structures. CdTe passivation films can also be deposited by metal-organic chemical vapour deposition (MOCVD) and MBE.^{144–146} As shown in Figure 15, the conformal deposition of CdTe on the side-walls of high-aspect ratio mesa diode structures on HgCdTe has been demonstrated via the ALD method, and the passivation quality is better than that obtained via MBE.¹⁴⁷ With the development of small pixel and multi-band FPAs, the uniform deposition of passivation layers on small-area pixels with deep mesa isolation and high aspect ratio will become a very challenging task. It is expected that conformal deposition techniques such as ALD will lead the development in this area.

In addition, SiN_x dielectric thin films have also been explored for passivating the surface of HgCdTe IR detectors,^{148,149} with a recent study indicating that Si-rich SiN_x thin films have surface passivation performance comparable to CdTe thin films.¹⁴⁹ The SiN_x thin films were deposited on

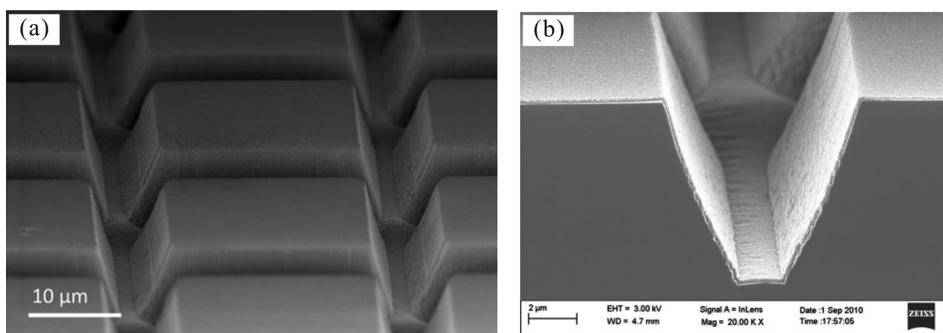


FIG. 15. (a) Top-view SEM image and (b) cross-sectional SEM image of an HgCdTe FPA passivated with CdTe layer deposited *via* the ALD method. Reproduced with permission from LiCausi *et al.*, J. Electron. Mater. **40**, 1668 (2011). Copyright 2011 Springer.

the HgCdTe surface with ICPECVD at 100 °C, and the SiN_x/HgCdTe interface characteristics were investigated employing capacitance-voltage measurements. It was found that after passivating with Si-rich SiN_x thin films, the interface trap densities were in the range of mid-10¹⁰ cm⁻² eV⁻¹, and fixed negative interface trap densities in the range of ~10¹¹ cm⁻², which is comparable to results obtained on HgCdTe surfaces passivated with CdTe thin films. The correlation between hydrogen bond density ([Si-H] and [N-H] bonds) and surface passivation performance has also been studied. [Si-H] and [N-H] bond densities and the [Si-H]/[N-H] bond density ratio were identified as potential measures of surface passivation performance at the interface of SiN_x/HgCdTe, and SiN_x films with high [Si-H] and low [N-H] bond densities have been identified as having better surface passivation performance, and thus being suitable for passivating HgCdTe devices. In addition to surface passivation, hydrogen introduced during the ICPECVD deposition of the SiN_x thin films contributes to the bulk passivation of HgCdTe, which will be discussed later in this section. Other potential advantages of SiN_x passivation layers over ZnS or CdTe include SiN_x being a more robust and chemically resistant layer that can be deposited with low-temperature processing technology that is based on low-cost industry-standard CVD techniques. Thus, SiN_x thin films could provide an alternative surface passivation technique to CdTe.

Apart from surface passivation with thin films, other methods, such as Cd-rich anneals, can also be used to passivate the surface of HgCdTe. In the work of Wan,¹⁵⁰ HgCdTe materials were annealed in an MBE chamber at 140 °C under Cd-rich conditions. With this anneal, the photoconductive response lifetime of the HgCdTe material was enhanced from 4 μs to 15 μs (at 100 K). Such a significant lifetime enhancement was attributed to the annihilation of surface recombination centers and metal vacancies in the material. As this passivation process is rate-limited by compositional interdiffusion, instead of gas-phase diffusion, it has the capability of conformal coverage of high aspect ratio surfaces, which is required by modern IR FPA technology.

Bulk passivation: Apart from surface passivation, bulk passivation also plays an important role in reducing the leakage current in HgCdTe detectors, especially for HgCdTe detectors grown on alternative substrates. For HgCdTe detectors grown on alternative substrates such as Si, there are a large number of threading dislocations generated in the epilayer due to the large lattice and CTE mismatch between HgCdTe and the substrates. These dislocations can introduce

defect states in the bandgap which act as SRH recombination centers and increase diode leakage current.^{151,152} Therefore, it is essential to passivate these defect states in the material in order to minimize the effects of threading dislocations. Hydrogen is reported to effectively passivate defect states in HgCdTe epilayers and thus significantly reduce the leakage current.^{153–159} In earlier studies, hydrogen was introduced into HgCdTe by using electrochemical methods^{153,154} and, more recently, hydrogen has been introduced into HgCdTe using ECR plasma hydrogenation.¹⁵⁵ The defect–hydrogen complexes may involve several hydrogen atoms and host-lattice structural rearrangements, and the attachment of hydrogen to dangling bonds is expected to eliminate defect gap states.

Although the mechanism of hydrogen bulk passivation is still not fully understood, some encouraging results have already been demonstrated. In the work of Carmody *et al.*,¹⁵⁶ HgCdTe/CdTe/Si layers passivated with hydrogen demonstrate lifetimes comparable to those grown on CdZnTe, even though their dislocation densities were higher. This is due to the fact that the incorporated hydrogen passivates both scattering and recombination centers and thus increases the carrier lifetime and mobility.^{157,158} In the work of Boieriu *et al.*,¹⁵⁹ hydrogen via an inductively coupled plasma (ICP) was used to incorporate hydrogen into LWIR HgCdTe/Si photodiodes. The fully fabricated devices exposed to ICP showed statistically significant increases in zero-bias impedance values, improved uniformity, and decreased dark currents.

Despite significant progress in this field, especially with the application of standard ZnS dielectric films and advanced *in-situ* CdTe passivation, defect-related leakage current still represents an on-going issue for HgCdTe IR detectors, especially for LWIR HgCdTe detectors. Because of the narrower bandgap, LWIR HgCdTe detectors are more sensitive to defect-related leakage current, and passivation quality still needs to be improved for LWIR HgCdTe detectors. One potential approach for better passivation quality is hybrid passivation.^{159,160} For example, CdTe or ZnS thin films can be combined with hydrogen passivation to improve the passivation quality of the detector devices. In the work of Hu *et al.*, *in-situ* CdTe passivation and high-density hydrogen plasma modification were combined together to improve the surface quality of typical n⁺-on-p HgCdTe LWIR photodiode detectors, and the maximum dynamic resistances of the device passivated *via* this hybrid passivation method were increased by 1–2 times in comparison to devices passivated with conventional ZnS passivation.¹⁶⁰

D. Dislocation reduction in detector structures

As discussed above, passivation acts as an effective approach to passivate defect centers and render them inactive as recombination centers. Clearly, if the defect density can be reduced, then any defect-related leakage current will also be reduced. Generally, there are two processes which can potentially introduce defects into the detector structure. One is during the epitaxial growth of the HgCdTe layers, and the other is during the device fabrication process.

During the epitaxial growth of HgCdTe, especially on alternative substrates like Si, dislocations can be generated in the epilayers due to the lattice constant and CTE mismatch. Some techniques can be applied to reduce the dislocation density, including growth condition optimization, cyclic thermal annealing, and dislocation gettering, which were discussed in Section IV B.

Apart from epitaxial growth, device processing, especially dry etching processes, can also introduce structural damage and defects in the HgCdTe layer, especially since HgCdTe is a relatively soft material. In modern device processing technology, plasma dry etching is now widely applied in the fabrication of HgCdTe photodiode FPAs, especially small pixel FPAs. However, the plasma can cause significant surface damage to HgCdTe and induce a high density of defects, leading to large leakage currents, lower operating temperature, as well as lower pixel yields. Therefore, appropriate techniques need to be applied to suppress/reduce plasma damage in HgCdTe. Ye *et al.* reported a multiple mask technique, integrating a patterned silicon dioxide (SiO_2) film over a patterned thick photoresist film to reduce the plasma damage to HgCdTe during mesa dry etching with inductively coupled plasma (ICP).¹⁶¹ By using this multiple mask technique, the dynamic resistance in the zero-bias and low-reverse-bias regions of HgCdTe photodiode arrays was improved by one- to twofold compared with devices using a simple mask of patterned SiO_2 . This suggests that the multiple mask technique is effective in reducing plasma damage to the HgCdTe mesa, and thus defect-related leakage current of the resultant detectors. With the development of small pixel and multi-band FPAs, the impact of plasma damage could be more significant due to the deep and small mesa structures required, which have a higher area/volume ratio in comparison to the current state-of-the-art HgCdTe FPAs. More effort is needed to develop appropriate techniques to reduce surface damage caused by dry etching.

E. Material volume reduction in detector structures

As discussed above, one of the major components of photodiode dark current is the inherent thermal generation

current: that is, the diffusion current caused by the diffusion of thermally generated minority carriers to the edge of the p-n junction depletion layer. Such thermally generated dark current is directly proportional to the material volume of the detector.^{119–121} In addition, two other dark current components, trap-assisted tunnelling current and band-to-band tunnelling current, are directly proportional to the p-n junction area and, thus, the effective volume of the device.^{119–121} Therefore, these dark current mechanisms can be effectively suppressed by reducing the device volume. Generally, there are two approaches to reducing the material volume of the detector: one is to reduce the thickness of the absorption layer; the other is to reduce the pixel size. The reduction of absorption layer thickness appears to be the easiest and most reliable way to achieve a reduction in material volume. However, reducing the thickness of HgCdTe absorber material will also reduce light absorption and, thus, lower the quantum efficiency, which is not acceptable. The material volume reduction must be undertaken without reducing light absorption, which is a big challenge that needs to be addressed. As discussed in Section IV C, small pixel pitch FPAs are currently readily achievable in terms of device processing technology, but also present significant challenge in terms of low light absorption and, thus, lower quantum efficiency. These challenges will be addressed as follows.

Reduction of the absorption layer thickness: For standard HgCdTe detectors, most of the light is absorbed in the absorption layer ($>5\ \mu\text{m}$ thick, usually $\sim 10\ \mu\text{m}$), leading to a high quantum efficiency. However, if the absorption layer is reduced to less than $1\ \mu\text{m}$, light absorption in the layer will decrease significantly. Therefore, maintaining high light absorption in a thin HgCdTe layer becomes the critical point in this approach. Several potential methods can be used to maintain the light absorption efficiency while reducing the thickness of the HgCdTe absorber layer, including (1) multiple-pass radiation and (2) plasmonic enhanced light absorption.

Multiple-pass radiation can be achieved with a backside reflector, the schematic structure of which is shown in Figure 16(a).¹⁶² More efficient light absorption can be achieved by utilizing interference phenomena to set up a resonant cavity within the detector by using two dielectric layers on the front and rear surface of the detector, the schematic structure of which is shown in Figure 16(b). Interference occurs between the waves reflected at the rear and at the front surface of the semiconductor.¹⁶² The thickness of the semiconductor is properly chosen to set up standing waves in the structure that peak at the front surface and have nodes at the back surface. The quantum efficiency oscillates as a function of the thickness of the structure, with peak absorption occurring at

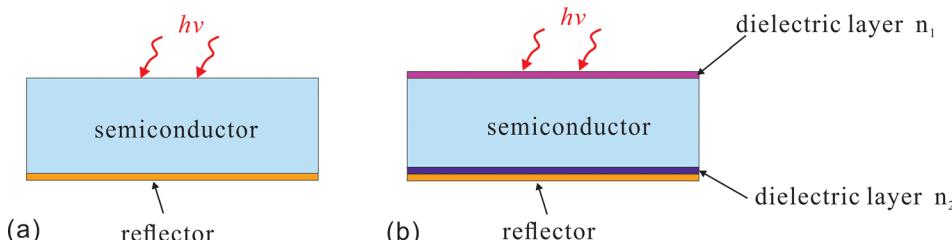


FIG. 16. Schematic structures for achieving (a) multiple-pass and (b) resonant cavity radiation in a detector. Reproduced with permission from A. Daniels, *Field Guide to Infrared Systems, Detectors, and FPAs*, second ed., pp. 75–76 Copyright 2010 SPIE Press.

thicknesses corresponding to an odd multiple of $\lambda/4n$, where n is the refractive index of the semiconductor. Higher gain can be obtained in structures sandwiched between two dielectric layers and supplied with a backside reflector. The gain in quantum efficiency increases with n . Such cavity designs significantly enhance the absorption and allow for high quantum efficiency. It should be noted, however, that interference effects modify the spectral response of the device, such that the gain within the optical cavity is achieved only in a narrow spectral region, which can be detrimental for imaging applications. Another issue is that optical resonance occurs mostly for perpendicular incidence and is less effective for oblique incidence, thus limiting the use of these approaches with fast optics.

Plasmonic enhanced light absorption approaches utilize the resonance enhanced light absorption effect offered by metallic structures to enhance light absorption in thin HgCdTe layers. Such plasmonic structures have been widely studied for enhancing the device performance of III-V IR detectors.^{163,164} For example, a 160% increase in signal-to-noise ratio was observed for an InAs/InGaAs quantum-dots-in-a-well heterostructure FPA by using a two dimensional metal hole array on top of the FPA. However, little work has been reported on HgCdTe detectors. In one recent theoretical work,¹⁶⁵ a plasmon-based HgCdTe detector is discussed, which is comprised of a thin semiconducting region (340 nm thick) sandwiched between a bottom metallic mirror and top metallic strips or dots. The metal-semiconductor-metal system defines a horizontal plasmonic cavity, where waveguide resonances of Fabry-Pérot-type¹⁶⁶ take place for specific optogeometrical parameters, leading to significant field and absorption enhancement within the semiconductor. A high quantum efficiency on a broad angular and spectral range is expected. Figure 17 shows the schematic structure, absorption spectra, and angular behaviour of a 340 nm continuous HgCdTe layer coupled to a 2D square metallic dot array. The cavity can be used alone or arranged in an array, and its resonant frequency can be adjusted by the dimensions of the metallic dot/strip. For HgCdTe at $\lambda = 9 \mu\text{m}$, the simulations showed a 75% quantum efficiency for a semiconducting layer thickness of only 340 nm. This approach is very promising in reducing the dark current while maintaining high quantum efficiency. Our research group at the University of Western Australia is working on a similar approach by patterning a thin layer of small gold gratings

and patches on the surface of HgCdTe, the results of which will be reported elsewhere.

Reduction of pixel size: The reduction of pixel size presents another method to reduce the detector material volume, with or without a reduction in the absorption layer thickness. However, by reducing the pixel size, the light absorption/collection efficiency is decreased due to the reduced horizontal absorption area. For example, if the pixel dimension is reduced from $20 \mu\text{m}$ to $10 \mu\text{m}$ without reducing the pixel pitch ($40 \mu\text{m}$), the horizontal absorption area is reduced from its previous area, resulting in reduced collection of electron-hole pairs and, thus, lower quantum efficiency. Therefore, techniques must be applied to maintain light absorption while reducing the pixel size, with three potential approaches being investigated: (1) photon-trapping structures, (2) special detector geometry design, and (3) micro-lens design.

Photon-trapping structures: As demonstrated in III-V IR detectors, photonic crystal structures can be used to effectively enhance the light absorption in detectors with small material volume. Recent work on quantum dot infrared photodetectors (QDIPs) has shown that with the application of photonic crystals, the absolute IR photoresponse of a QDIP was enhanced by 130%, and the signal/noise ratio was enhanced by 160%.^{163,167} Similarly, this indicates that photonic crystal structures can be used to reduce the absorption volume of HgCdTe detectors while still maintaining high quantum efficiency. Wehner *et al.*¹⁶⁸ presented a theoretical and experimental study on the effect of photonic crystal structures on the performance of MWIR HgCdTe detectors with reduced material volume. Their work showed that with proper photonic crystal design, such as shape and size of the pillars and holes in the photonic crystal structure, lower dark current can be achieved by reducing the detector volume without an appreciable decrease in quantum efficiency. In contrast, detectors with the same reduced volume but without photon trapping capability exhibited reduced dark current and also reduced quantum efficiency. Liang *et al.*¹¹⁹ presented a further theoretical study on the effect on photonic crystal structures on LWIR HgCdTe detectors with reduced absorption volume. Their simulation indicated that with proper design of the detector and the photonic crystal period, high quantum efficiency can be obtained for HgCdTe detectors with low volume fill factor, which applies to both MWIR and LWIR detectors. According to their simulations, to maintain the quantum efficiency over a wide range of

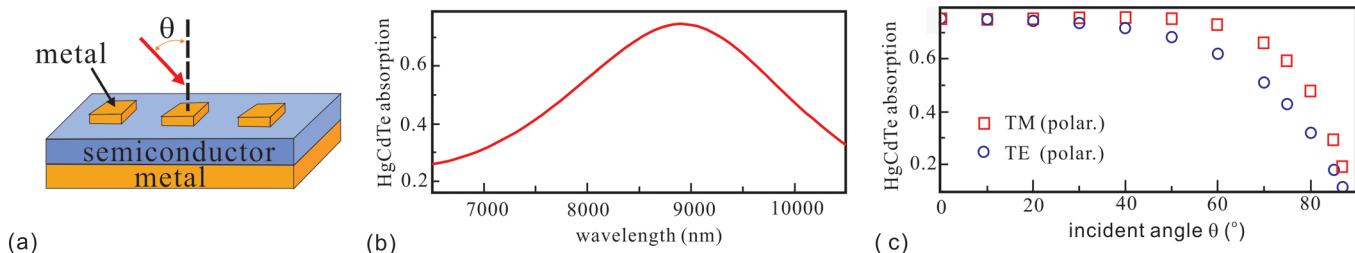


FIG. 17. (a) Schematic structure, (b) absorption spectra, and (c) angular response of a 340 nm continuous HgCdTe layer coupled to a 2D square metallic dot array. Note that the metallic dots are 40 nm thick and $980 \text{ nm} \times 980 \text{ nm}$ in area. The angular behaviour is for the cut-off wavelength of $9 \mu\text{m}$. Reproduced with permission from Appl. Phys. Lett. **94**, 181104 (2009). Copyright 2009 AIP Publishing LLC.

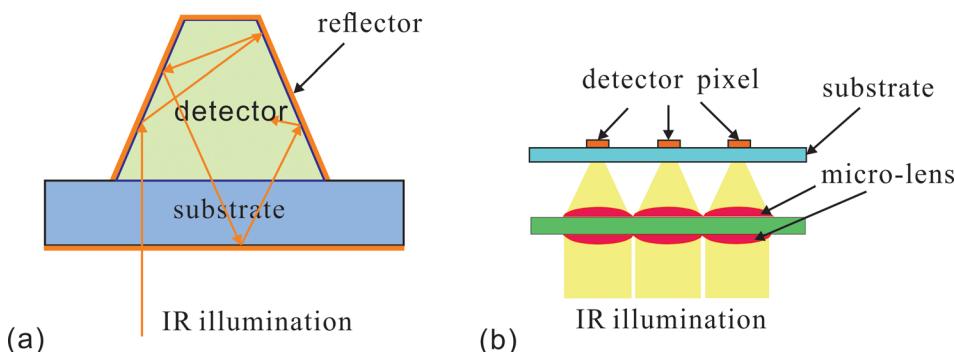


FIG. 18. Schematic (a) truncated pyramid geometry and (b) micro-lens structures for enhancing light absorption in detectors with reduced material volume.

volume fill factor for a target detector wavelength, only the period of the photonic crystal structure needs to be changed. This indicates the potential for practical device applications.

Special detector geometry design: Photon trapping structures, such as photonic crystals, are based on fine structures to modulate the light field and thus increase the light absorption. Such fine structures are typically on the scale of several microns, and thus their fabrication can require a complex process. Apart from photon trapping structures, some simple mesa geometry designs can also be used to increase the light absorption in detectors with reduced material volume. Figure 18(a) shows a detector with a truncated pyramid geometry. By choosing a proper angle between the bottom surface and the mesa sidewall, the incoming light impinging on the bottom surface will be reflected several times by the sidewalls of the device. If combined with reflectors on the sidewall/front surface/bottom surface, all the light can be absorbed by the material. With appropriate design of the mesa geometry, an absorption efficiency as high as 90% has been demonstrated in SELEX's Hawk HgCdTe FPAs.¹⁶⁹ Such a simple mesa geometry design provides a reliable way to reduce the material volume while still maintaining high quantum efficiency for HgCdTe detectors and, most importantly, the structure is compatible with current mainstream processing technology with pixel pitch larger than 10 μm .

Micro-lens for focusing light: As shown in Figure 18(b),^{170,171} an array of pixel-size micro-lens structures placed on the back-side of the substrate can be used to focus the incident light onto a small area, which will increase the light collection efficiency of the individual small-area detectors in an FPA. By choosing an appropriate radius of the micro-lens, the light incident angle can be tuned to achieve the optimum light collection efficiency. Similar micro-lens structures have been studied for other detector technologies and solar cells, which have shown encouraging results.¹⁷²

Note that there is no clear separation between the different approaches discussed above. They can be combined together for achieving even lower dark current while maintaining high quantum efficiency. For example, a pyramid geometry detector can be combined with a micro-lens array design to reduce the detector material volume even further without sacrificing detector quantum efficiency.

F. Barrier detectors

Apart from the various approaches discussed above, a relatively new device based on a unipolar nBn structure has been recently proposed to suppress dark current and thus enhance the operating temperature. Figure 19 shows the schematic energy band diagram of an nBn detector,^{77,173} which comprises an n-type narrow band gap absorber region coupled to a thin wide bandgap barrier layer, followed by a narrow bandgap contact region. The thin n-type semiconductor on one side of the barrier constitutes a contact layer for biasing the device, while the thick n-type narrow bandgap semiconductor on the other side of the barrier is the photon absorbing layer whose thickness should be comparable to the absorption length of light in the device, typically several microns (usually $>5 \mu\text{m}$, but 10 μm preferred). The critical point to the application of this nBn device architecture is to have almost zero valence band offset so that there is no hole barrier present throughout the heterostructure, while maintaining a large conduction band offset (electron barrier). Such a barrier arrangement allows photogenerated minority carrier holes to flow to the contact unimpeded, even at very low bias, while the majority carrier dark current, re-injected photocurrent, and surface current are blocked by the large energy barrier in the conduction band. Because there is no high field depletion region present in the device structure, the nBn detector can effectively suppress and reduce dark

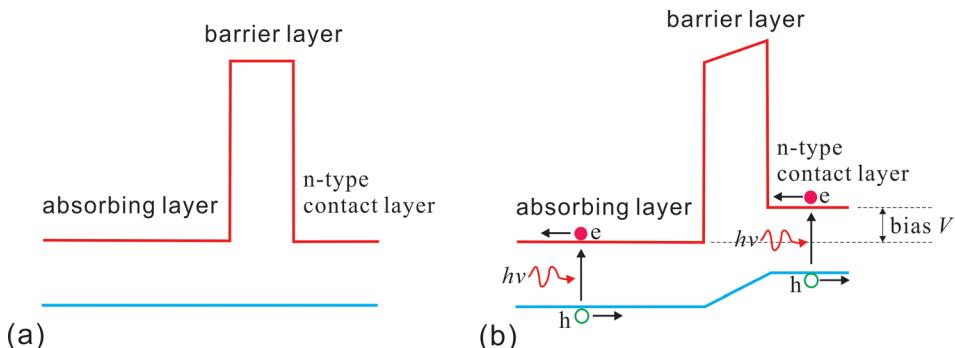


FIG. 19. Schematic energy band diagram of an ideal nBn detector under (a) zero bias and (b) illumination and low reverse bias V . Reproduced with permission from Appl. Phys. Lett. **89**, 151109 (2006). Copyright 2006 AIP Publishing LLC.

current (especially those associated with SRH processes and tunnelling mechanisms) and noise without impeding the photocurrent (signal). In addition, the large energy barrier in the conduction band can also suppress and reduce surface leakage current, which mitigates the stringent need for high quality surface passivation. The term “unipolar barrier” has been used to describe a barrier that can block one carrier type (electrons for nBn) but allows for the unimpeded flow of the other (holes for nBn). Because of the barrier design, the nBn detector offers two important advantages. First, it behaves like a photoconductor except for the presence of the barrier. Therefore, its fabrication process is much simpler and more robust compared with that of a photodiode. This should lead to much higher pixel yield for nBn detectors and their FPAs, and thus can significantly reduce the cost. Second, for an nBn detector there is no depletion region, and only a very low voltage is required for biasing. Therefore, defect related dark current (especially SRH current) as well as tunnelling dark currents can be effectively suppressed and eliminated, leading to higher operating temperatures. To a certain extent, nBn detectors behave similar to photoconductors in that they are relatively insensitive to point defects, which should also result in improved uniformity and higher pixel yield in comparison to photovoltaic detectors.

The nBn device architecture was first proposed by Maimon and Wickst⁷⁷ and has been widely studied for III-V IR detectors, such as MWIR and LWIR InAs/GaSb type II superlattice detectors.^{78–80} Furthermore, significant progress has already been made in InAs/GaSb type II superlattice nBn detectors. Megapixel MWIR and LWIR type-II superlattice FPAs based on an nBn device architecture have been demonstrated with excellent imaging quality.^{81–83} The potential of barrier detectors operating at relatively high temperatures was demonstrated recently by the high performance MWIR InAsSb-AlAsSb type II superlattice nBn detectors reported by Jet Propulsion Lab, which show a detectivity of 1×10^9 cm Hz^{1/2} W⁻¹ at 300 K, and 5×10^9 cm Hz^{1/2} W⁻¹ at 250 K.¹⁷⁴

However, the application of an nBn device architecture to HgCdTe presents a serious challenge due to the difficulty in realizing an ideal nBn band diagram using CdTe or HgCdTe materials (zero valence band offset and no hole barrier, combined with a large conduction band offset with an effective electron barrier). Figure 20 shows the schematic energy band diagram of an nBn HgCdTe detector with high x value Hg_{1-x}Cd_xTe alloy as the barrier layer. Although some work has been undertaken on HgCdTe nBn

devices, the existence of a valence band offset in HgCdTe-based nBn detectors seriously limits the device performance.^{84–86,175,176} At low bias, the valence band barrier inhibits minority carrier holes flowing between the absorber and the contact cap layer. Depending on the wavelength of operation, a relatively high bias, typically greater than the bandgap energy of the narrow bandgap absorbing layer, is required to be applied to the device in order to collect all of the photogenerated carriers, which can lead to the formation of a depletion layer and strong band-to-band and trap-assisted tunnelling due to the resulting high electric field. Therefore, present strategies for developing HgCdTe nBn detectors are focused on reducing and even completely eliminating the valence band offset between the absorbing layer and the barrier layer, which will lead to lower operating bias, lower dark current, and the ability to operate at higher temperatures. There are several potential approaches being investigated, including appropriate doping of the barrier and use of a superlattice barrier.

One approach to reducing the valence band offset is to dope the HgCdTe barrier layer to be p type with an appropriate doping profile and concentration. Such an architecture is similar to that proposed by White in 1983, in which a p-type barrier is interposed between two narrow gap n-type regions.¹⁷⁷ By using the proper doping profile of both p type and n type, the valence band offset in the barrier can be significantly reduced or even completely removed, thus meeting the band alignment requirements for an ideal nBn detector structure. In principle, such a doping profile is possible with advanced epitaxial technologies such as MBE and MOCVD.

Another approach to reduce or even eliminate the valence band offset is to use a superlattice-based HgCdTe barrier. Figure 21(a) shows the energy band diagram of the HgTe, HgCdTe, and CdTe semiconductor alloys.¹⁷⁸ For bulk materials, a large valence band discontinuity is present between HgCdTe and CdTe or HgTe. However, with HgTe/CdTe SLs, the highest hole energy level in the wide bandgap SL can be tuned to exactly match the valence band edge of the narrow bandgap HgCdTe absorber and top contact layers by tuning the HgTe QW thickness to achieve zero valence band discontinuity in a HgCdTe nBn detector structure while still maintaining a high electron band discontinuity. This is clearly indicated by the decrease of the hole energy level and the fast increase of the electron energy level as the HgTe QW thickness is decreased below 6 nm, as shown in Figure 21(b).¹⁷⁹ More importantly, HgTe and CdTe are nearly

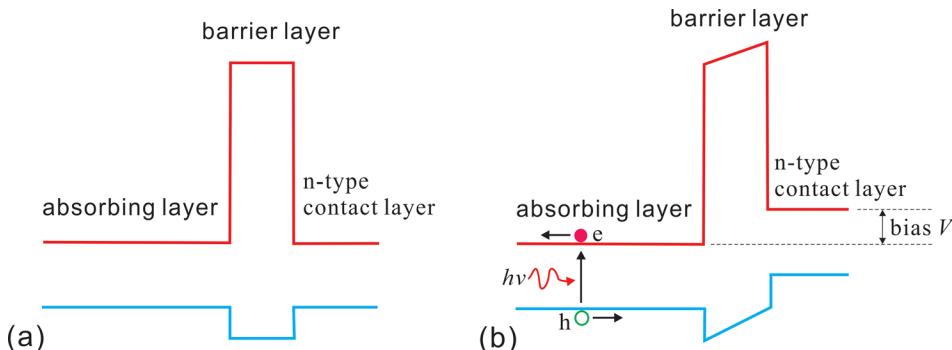
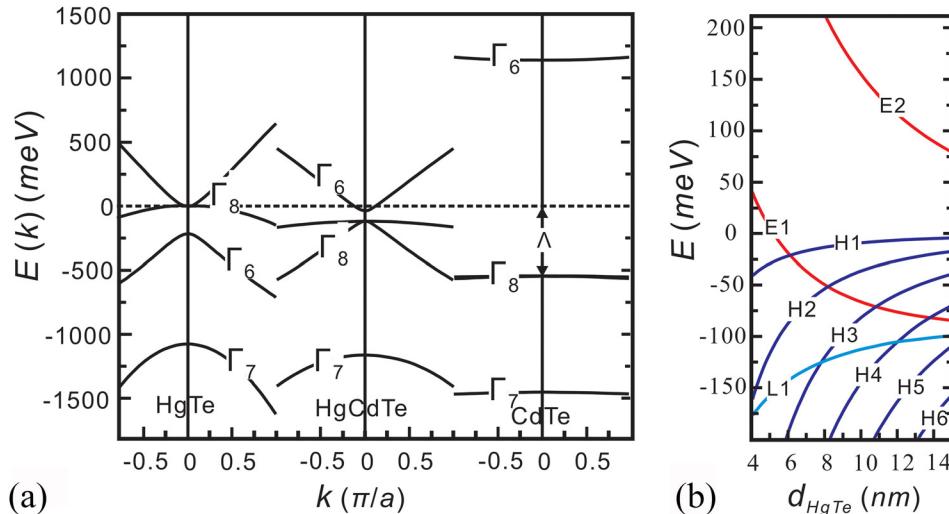


FIG. 20. Schematic energy band diagram of an nBn HgCdTe detector with high x value Hg_{1-x}Cd_xTe alloy as the barrier layer: (a) zero bias and (b) under illumination and low reverse bias V.



lattice-matched to HgCdTe, guaranteeing the epitaxial growth of high quality HgCdTe heterostructures.

Our research group at The University of Western Australia is working on both of the above two approaches, the results of which will be reported elsewhere. Apart from the standard nBn device structures, there are other extended barrier detector concepts. Klipstein *et al.*¹⁸⁰ proposed a wide range of barrier detector structures, which can be generally classified into two groups: XB_nn and XB_pp detectors, the schematic energy band diagrams of which are shown in Figure 22. In the case of the first group (XB_nn), all have the same n-type B_nn structural unit, but use different contact layers (X), where either the doping or material composition (x value of $Hg_{1-x}Cd_xTe$) is varied. In the case of the second group (XB_pp), they are polarity-reversed versions of the n-type detectors. Some work has been undertaken on extended barrier detector structures, such as the pB_nn structure. However, nBn still presents the simplest and most reliable device architecture for production when considering the unsolved complex p-type doping issues in HgCdTe. It needs to be emphasized that, in comparison to photovoltaic detectors, the successful development of a HgCdTe-based nBn device technology without a valence band barrier would have the following characteristics:

- (1) low dark current, high impedance, and diffusion limited performance comparable to photovoltaic detectors;

FIG. 21. (a) Low temperature energy band diagrams of HgTe, HgCdTe, and CdTe semiconductors. Reproduced with permission from J. Garland, *Mercury Cadmium Telluride: Growth, Properties and Applications*, Copyright 2011 John Wiley & Sons Ltd; (b) 4 K energy levels in HgTe/CdTe SLs vs HgTe QW thickness. Reproduced with permission from J. Electron. Mater., **32**, 608 (2003). Copyright 2003 Springer.

- (2) low bias voltage and the absence of high field depletion regions and associated tunnelling-related dark currents;
- (3) absence of surface related dark currents and less stringent surface passivation requirements;
- (4) a much simpler and more robust fabrication technology, and a much higher level of tolerance to point defects, which has the potential to improve pixel yield and reduce FPA costs.

Note that there is still a long way to go in order to achieve MWIR and/or LWIR HgCdTe FPAs operating at room temperature, or at least above thermoelectrically cooled temperatures. Although all of the approaches discussed in Section V will contribute to a reduction of dark current, and thus an enhancement of operating temperature for photovoltaic detectors, any future advances could render barrier detectors as the most promising approach to achieve HgCdTe FPAs operating at close to room temperature.

VI. MULTI-BAND HgCdTe DETECTORS

One of the desirable features of “third generation” IR detectors is the capability of multi-band detection. Systems that sense in multiple IR spectral bands can discriminate both absolute temperature and the unique signature of objects in the field, thus improving target detection (especially in cluttered environments) and reducing false alarm

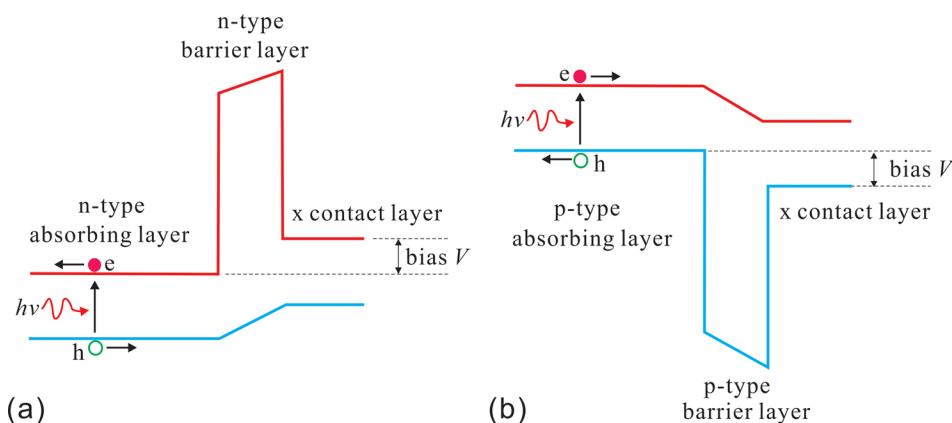


FIG. 22. Schematic energy band diagram of (a) XB_nn and (b) XB_pp detectors. Note that the X contact layer can be of different doping conditions and materials (x value of $Hg_{1-x}Cd_xTe$). Reproduced with permission from Klipstein *et al.*, Reducing the cooling requirements of mid-wave IR detector arrays, SPIE Newsroom. Copyright 2011 SPIE.

rates. Therefore, multiband detection combined with advanced colour processing algorithms can further improve sensitivity compared to that of single-band devices. In early development, dual band sensors were made by using two photovoltaic focal planes and a beam splitter.¹³ This design suffers a major difficulty in aligning the optical system to a precision such that the exact same image feature can be accurately compared on the two focal planes at the pixel level. It also has the drawbacks of dual vacuum enclosures and cooling systems. Instead of this design, recent focus in developing multi-band FPAs has shifted toward integrating multi-band functionality onto a single pixel, which is usually termed multi-colour detection. Currently, the technology development has focused on dual-colour detectors. Generally, there are two variants of dual-colour detector structures: (1) simultaneous dual colour detectors and (2) sequential dual colour detectors. Apart from these two traditional approaches, MEMS (microelectromechanical systems) tunable filters integrated with the IR sensor technology (also termed adaptive FPA technology – AFPA) also provide another important approach to achieve multi-band detection, which will also be discussed later in this section.

Simultaneous two-colour detectors: For this class of dual-colour detectors, the photovoltaic devices generally consist of a stack of two detector layers separated by a wide bandgap common electrode.¹³ Figure 23(a) shows the schematic structure of a simultaneous two-colour detector developed in the USA. The detector/band 1 and detector/band 2 alloy compositions can be any two x-values as long as the detector/band 1 has a higher x-value than detector/band 2. That is, the longer cut-off wavelength HgCdTe layer is on the top for backside illumination. Ideal devices, in which optical detection takes place simultaneously and the optically sensitive area is co-located, are difficult to fabricate on normal pixel sizes, for example, $<15\text{ }\mu\text{m}$, which is the state of

the art pixel size for single color FPAs. The pixel size of dual color detectors is usually much larger, $\sim 50\text{ }\mu\text{m}$ or so. Signals are read from the p-type barrier layer and both Band 1 and Band 2 layers, allowing extraction of two independent signals from both bands simultaneously. Note that the meaning of “simultaneously” must be defined by the system user, since it is frequently the case that the length of signal integration may be different for each band. Figure 23(b) shows the top-view SEM image of a typical simultaneous two-colour pixel, which has already been demonstrated in Raytheon imaging systems based on 2D FPAs.¹³

Apart from the above-described simultaneous two-colour detector structures developed in the USA, a pseudo-planar two colour detector architecture has been developed for achieving simultaneous detection by CEA-LETI in France,¹⁸¹ see schematic structure in Figure 23(c).¹⁸¹ In comparison with the simultaneous two-colour detector structures shown in Figures 23(a) and 23(b), this pseudo-planar two colour detector structure has the following main features: (1) the pixel is a simple superposition of two standard pixels with the MWIR device at a lower level than the LWIR detector. The realization and control of the entire fabrication process are more industry-standard and rely on existing know-how of standard pixel fabrication; (2) the hole etching step to contact the MWIR device, which is a key technical issue, is easier to perform than the deep trench etching needed for electrically isolating the pixels in Figures 23(a) and 23(b), because of the lower aspect ratio. Its geometry also allows high performance diodes in the LWIR bands to be more readily achieved, because of its shallower depth and larger size; (3) the lower MWIR absorption layer can be made as thick as necessary to optimize the quantum efficiency, since it does not need to be etched through to delineate the pixels; and (4) there is no electrical crosstalk, since the pixels are electrically independent and no current is

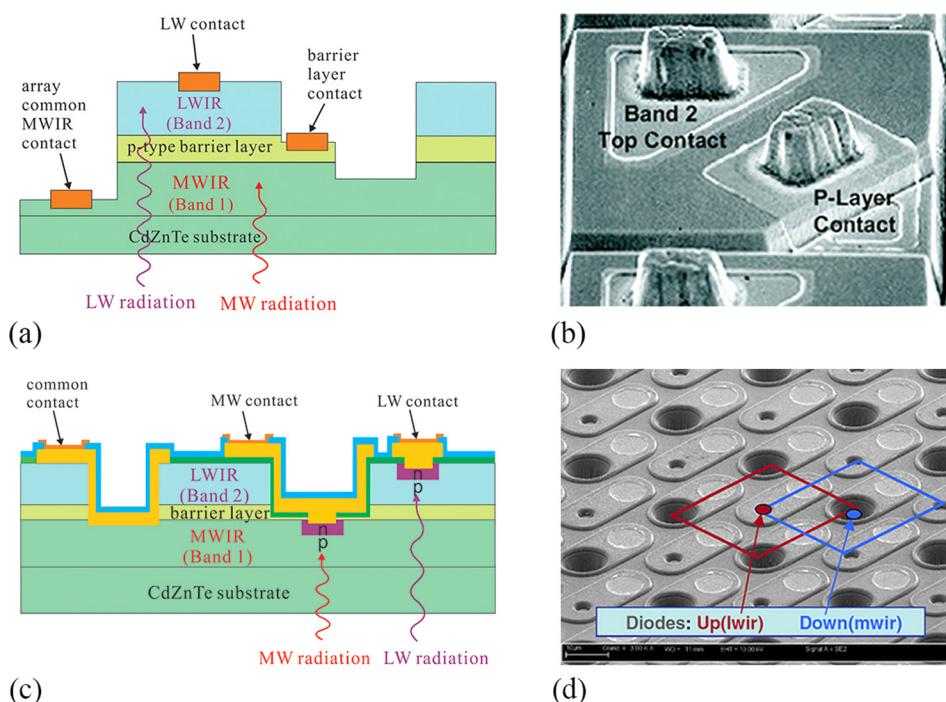


FIG. 23. (a) Schematic sample structure. (b) Top-view SEM image of simultaneous two-colour detectors developed at Raytheon. Reproduced with permission from P. Norton, Opto-Electron. Rev. **10**, 159 (2002). Copyright 2002 Springer; (c) schematic sample structure and (d) top-view SEM image of the pseudo-planar simultaneous two-colour detectors developed at CEA-LETI. Reproduced with permission from Destefanis *et al.*, J. Electron. Mater. **36**, 1031 (2007). Copyright 2007 Springer.

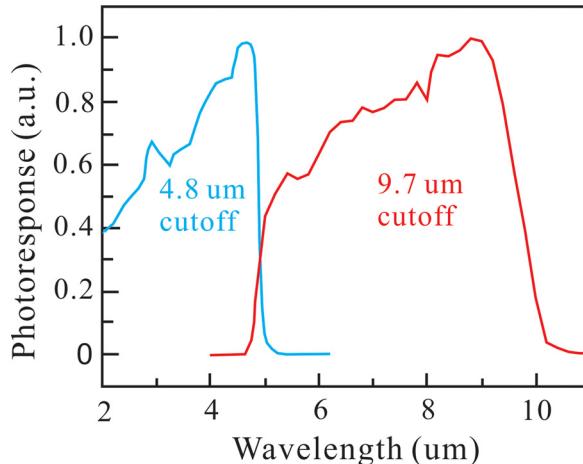


FIG. 24. Photoresponse spectra of a simultaneous LWIR and MWIR two-color HgCdTe infrared detector with cutoff wavelengths of $\lambda_{1,\text{cutoff}} = 4.8 \mu\text{m}$ and $\lambda_{2,\text{cutoff}} = 9.7 \mu\text{m}$. Reproduced with permission from Hu *et al.*, Opt. Lett. **39**, 5184 (2014). Copyright 2014 Optical Society of America.

flowing through either diode. Figure 23(d) shows a top-view SEM image of a pseudo-planar two-colour detector array developed at CEA-LETI,¹⁸¹ which has been successfully applied in the production of simultaneous dual-colour HgCdTe FPAs at Sofradir, France. In the recent work of Hu *et al.*,¹⁸² a 128×128 LWIR and MWIR two-colour photovoltaic HgCdTe FPA with a similar pseudo-planar structure has also been demonstrated to have ultralow spectral cross talk. Figure 24 shows the photoresponse spectra of the simultaneous LWIR and MWIR two-color HgCdTe infrared detector. The MWIR detector has a cutoff wavelength of $4.8 \mu\text{m}$ and a peak detectivity of $3.2 \times 10^{11} \text{ cmHz}^{1/2}$, while the LWIR detector has a cutoff wavelength of $9.7 \mu\text{m}$ and a peak detectivity of $4.3 \times 10^{10} \text{ cm Hz}^{1/2}$. LW-to-MW cross talk was observed to be 1.25%, while MW-to-LW cross talk was observed to be 0.7%.

Architectures for simultaneous detection allow one pixel to address both detection bands and thus provide both temporal and spatial coherence. However, it should be noted that the “simultaneous” two colour photovoltaic detector structures suffer from a major disadvantage: large pixel size due to the requirement of two contacts per pixel, which limits the pixel density and thus the array format size.

Sequential two-colour detectors: The “sequential” approach is also termed a bias-selectable detector^{13,183,184}

that needs only one contact per pixel, and is compatible with small pixel sizes. In this case, each band is read in turn by reverse biasing the diode from which the signal is desired. This is an elegant technique but suffers an operational disadvantage of non-simultaneous integration. Typical devices include p-n-N-P or n-p-P-N sandwich structures with each p–n junction being in a different composition material. Figure 25 shows the schematic device structure and top-view SEM image of a sequential two-colour detector. The wavelength band can be selected by the bias polarity applied between the two contacts, such that the diode that is reverse-biased at any particular time is the optically active device.

Apart from standard p-n junction based “sequential” two-colour detectors, nBn detector architectures provide an alternative strategy for realizing sequential two-colour detectors. If the top n-type contact layer is replaced with a second thick n-type absorption layer with a lower x value (longer cut-off wavelength), a back-side illuminated two-colour IR detector can be formed. Similar to the case shown in Figure 25(a), the LWIR absorption layer is placed on top of the MWIR absorption layer for back illumination. By switching the bias polarity, either LWIR or MWIR band detection can be switched on.⁸⁰

Sequential two-colour HgCdTe detectors have successfully been demonstrated in imaging systems.^{183,184} In the work of Smith *et al.*,¹⁸³ a sequential 256×256 LW/MW two-colour HgCdTe FPA was demonstrated with an MWIR cutoff wavelength of $5.5 \mu\text{m}$ and an LWIR cutoff wavelength of $10.5 \mu\text{m}$, as shown in Figure 26.

Over the past decade, significant advances have been made in this field, and both simultaneous and sequential dual colour FPAs have been demonstrated and produced. The current technology development in this field is to reduce pixel size, and thus provide larger array format, combined with lower cross talk, which are possible with further development of the detector processing technology. In addition, three colour detectors and their FPAs are also under development.

Adaptive focal plane array technology: Apart from simultaneous and sequential multi-band detector technology, tuneable MEMS filter-based IR FPA technology provides another approach to achieve multi-band detection.^{185,186} Because of the real-time tuneable resonant wavelength of the MEMS filter, MEMS filter-based multiband detection

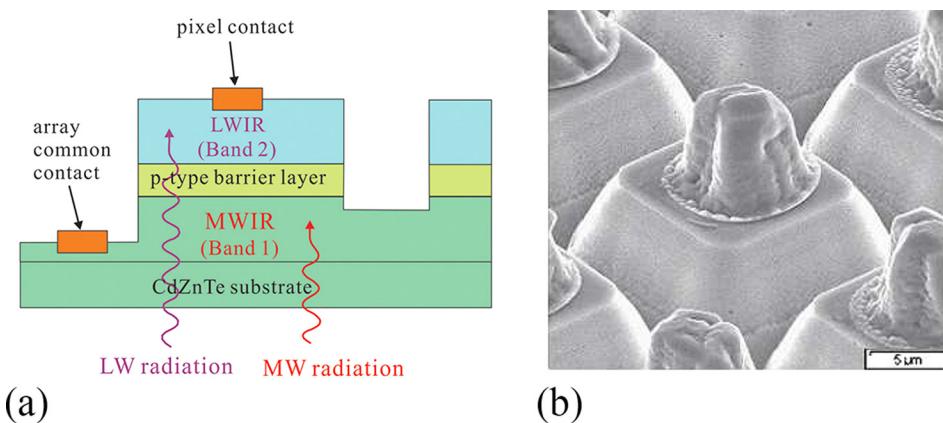


FIG. 25. (a) Schematic device structure and (b) top-view SEM image of sequential two-colour detectors. Reproduced with permission from Smith *et al.*, J. Electron. Mater. **35**, 1145 (2006). Copyright 2006 Springer.

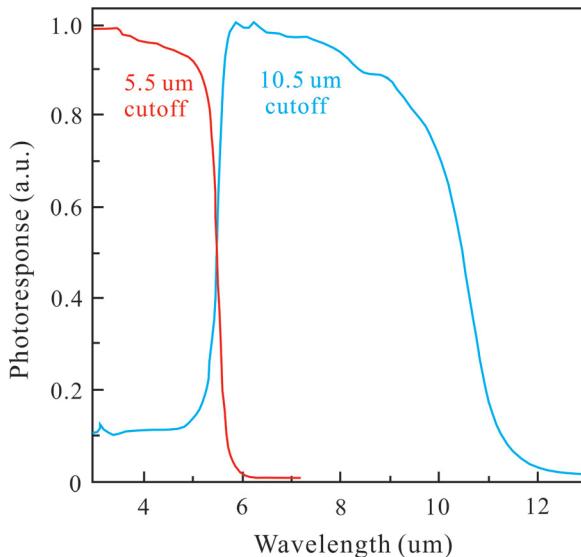


FIG. 26. Photoresponse spectra of a sequential LWIR and MWIR two-colour HgCdTe infrared detector with cutoff wavelengths of $\lambda_{1,\text{cutoff}} = 5.5 \mu\text{m}$ and $\lambda_{2,\text{cutoff}} = 10.5 \mu\text{m}$. Reproduced with permission from Smith *et al.*, J. Electron. Mater. **35**, 1145 (2006). Copyright 2006 Springer.

technologies have also been termed as adaptive focal plane array (AFPA) technologies. The core component of this AFPA technology is the integration of MEMS-based tunable optical filters with IR FPAs, such that the narrow band of wavelengths selected from the scene of interest is transmitted through the MEMS filter and onto the IR FPA. Regarding how the MEMS filter technology is integrated with the HgCdTe FPA, there are two main approaches: hybridization and monolithic integration, which will be discussed below.

Tunable MEMS optical filter: The MEMS optical filters are electrostatically actuated Fabry–Perot tunable filters. Figure 27 shows the general concept and an example simulated transmission spectrum of a MEMS-based optical filter.^{187,188} A Fabry-Perot filter requires that its two mirrors must be placed parallel to each other with a spacing, d , which determines the specific wavelengths transmitted through the filter. When moving the top mirror downwards, the spacing, or optical cavity length d , will reduce and the wavelength of light transmitted can thus be varied. In the *tunable optical filter* design, the tuning of the cavity length is performed by applying a voltage between two electrodes, which generates an electrostatic attraction that moves the

upper mirror closer to the fixed lower mirror. By controlling the voltage applied to the MEMS filter, the resonant wavelength of the MEMS filter, and thus the wavelength band of transmitted light, can be selected.^{187,188} This is particularly important for identifying targets in deep hide, where the image bands of different targets are very close, and thus their difference cannot be clearly distinguished with conventional broadband multi-colour detectors.

In recent years, significant effort has been devoted to designing and fabricating tuneable MEMS filters.^{187–193} Figure 28 shows the measured optical spectral transmission of tuneable MEMS filters developed by our research group at the UWA, including SWIR, MWIR, and LWIR.^{187–189} Note that the optical materials and mechanical structure of these MEMS filters need to be optimised according to the wavelength region of interest, as detailed in Refs. 187–189. For the MWIR MEMS filter, a tuning range of 900 nm is achieved with 17 V bias, which is almost 50% of the 3–5 μm MWIR region.^{187,188} The SWIR MEMS filter presents a tuning range of 800 nm with only 22.4 V bias. For the LWIR MEMS filter, a very wide tuning range of 3 μm is achieved with a bias of 160 V.¹⁸⁹

Monolithically integrated filter/detector: A monolithically integrated filter/detector technology integrates a small-area tuneable MEMS optical filter onto each single pixel of the FPA, as shown by the schematic diagram in Figure 29(a).^{193,194} By controlling the bias applied to each individual MEMS filter, one can achieve wavelength band selection at the individual pixel level. This is an exceptional idea for achieving AFPAs with wavelength control down to the individual pixel level, where the wavelength sensitivity of each pixel can be independently tuned. Over the past decade, significant progress has been made in this area. Antoszewski *et al.*¹⁹⁴ at the UWA initially demonstrated an SWIR HgCdTe detector monolithically integrated with a non-tunable Fabry-Perot filter in 2005, which operated at a centre wavelength of $\sim 1.95 \mu\text{m}$. Soon after that, Musca *et al.* at the UWA demonstrated an SWIR HgCdTe detector monolithically integrated with a tuneable MEMS filter.¹⁹³ This monolithically integrated system of MEMS filter/HgCdTe detector showed a wide tuning range of optical transmission from 1850 nm to 2200 nm by controlling the bias from 7.5 V to 0 V, as shown in Figure 29(b). The full-width at half-maximum of the MEMS optical filter transmission was approximately 100 nm over a tuning range of 2.2–1.85 μm .

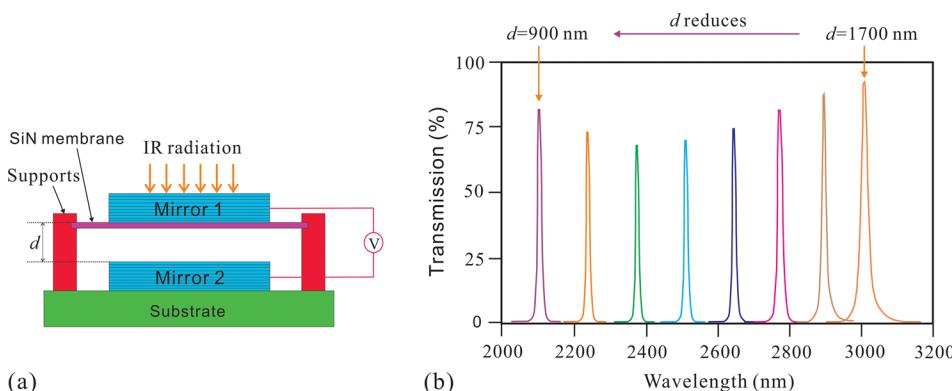


FIG. 27. (a) Schematic concept and (b) simulated transmission spectra with different spacing d for an SWIR tuneable MEMS optical filter.

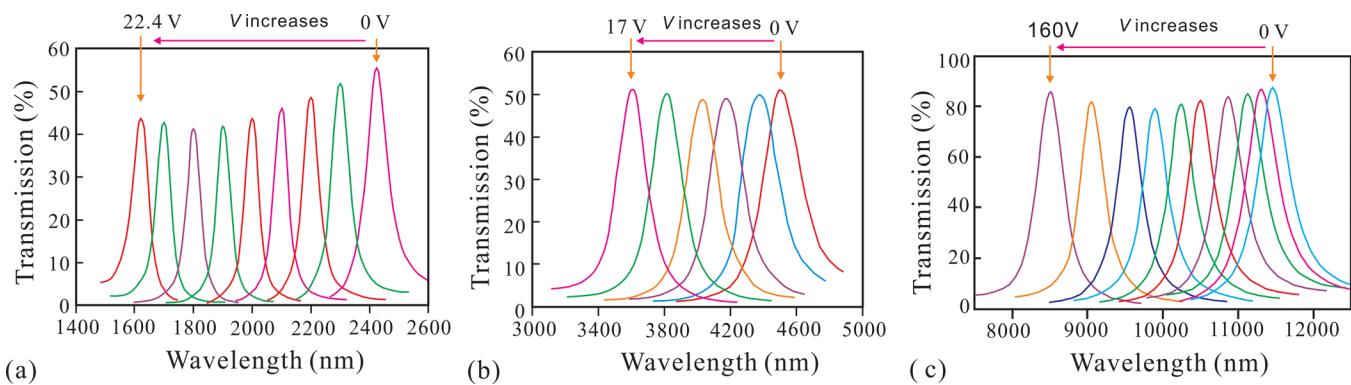


FIG. 28. Optical spectral transmission of tuneable (a) SWIR, (b) MWIR, and (c) LWIR MEMS filters developed at UWA for multi-spectral imaging applications.

Despite significant progress, the design and fabrication of monolithically integrated filter/detector structures is very complicated and very challenging. The primary challenges or issues that need to be addressed for this monolithic technology include^{187,188} (1) fill factor of the MEMS filter. Fill factor of a filter is defined as the ratio of the effective functional optical area over the total area occupied by the filter. A low fill factor for the MEMS filter will affect the overall resolution of 2D FPAs for imaging applications. However, the high pixel density in modern FPA technology presents a serious challenge to achieve high fill factor for MEMS filters integrated on individual pixels of the FPA. (2) Compatibility with HgCdTe detector processing requirements. In particular, all process temperatures need to be kept below 125 °C to avoid any damage to the HgCdTe detector material. Such low processing temperatures are not desirable for fabricating high performance MEMS filter structures in terms of material quality and robustness. Because of these issues, the research effort on AFPA technology has gradually shifted to the technology of hybrid integration of filter/detector structures.

Hybrid integrated filter/detector: In a hybrid integrated filter/detector technology, a large-area tuneable MEMS optical filter is fabricated separately and then hybridized onto the FPA or a section of the FPA. Since the MEMS filter is fabricated separately, its fabrication does not suffer from the limitation of low processing temperature for HgCdTe materials, and the fabrication technology can be optimised without any of the constraints imposed by a monolithic approach. The integration of a large-area tuneable MEMS filter that covers the entire FPA or section of the FPA provides close to 100% fill factor for the filter. In the work of Gunning *et al.*,¹⁹¹ a dual band adaptive HgCdTe FPA is demonstrated using this

hybrid integration structure comprising of an array of large-area MEMS tuneable filters, mated to a dual band (MWIR/LWIR) HgCdTe FPA. The MEMS filters provide narrow-band tuning in the LWIR (8.0–10 μm) as well as simultaneous broadband imaging in the MWIR (3–5 μm). Figure 30(a) shows the schematic structure of the adaptive FPA fabricated by Gunning *et al.*¹⁹¹ The filter characteristics, including LWIR passband bandwidth and tuning range, are determined by the integral thin film reflector and antireflection coatings. The nominal dimension of each MEMS filter is between 100 μm and 200 μm on a side and each filter covers a small subarray of detector pixels. Employing a dual-band FPA with 20 μm pixel pitch results in each MEMS filter covering a detector subarray ranging from 5 × 5 to 10 × 10 pixels. Figure 30(b) shows the room temperature spectral transmission of a filter in the dual-band adaptive FPA illustrating filter tuning for various actuation voltages. Note that the LWIR passbands shown in Figure 30(b) exhibit an apparent low peak transmission and have measured bandwidths of 200–300 nm. These results are all artifacts of the measurement system, since the filter is illuminated with a conical beam having angles of incidence ranging from about 12°–25°. Other measurements and analysis of the spectra indicate that the peak transmission values at normal incidence range between 80% and 90%. The modulation in the LWIR peak heights is caused by a corresponding modulation of the passband width at normal incidence. This modulation results from less than optimum antireflection coating of the outer surface of the moveable mirror membrane, which sets up interference in the silicon mirror support membrane. The large amplitude modulation in the MWIR is likewise caused by residual reflections from the antireflection coating.

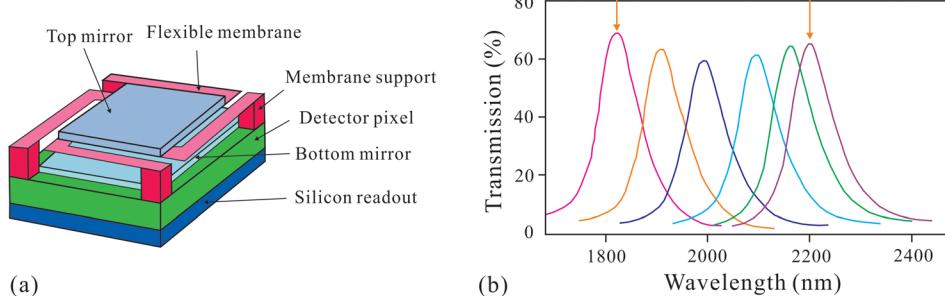


FIG. 29. (a) Schematic diagram of monolithic integration of a tuneable MEMS filter with an IR detector, and (b) optical spectral transmission of a tuneable SWIR MEMS filter monolithically integrated on an SWIR HgCdTe detector. Reproduced with permission from Musca *et al.*, IEEE Electron Device Lett. **26**, 888 (2005). Copyright 2005 IEEE.

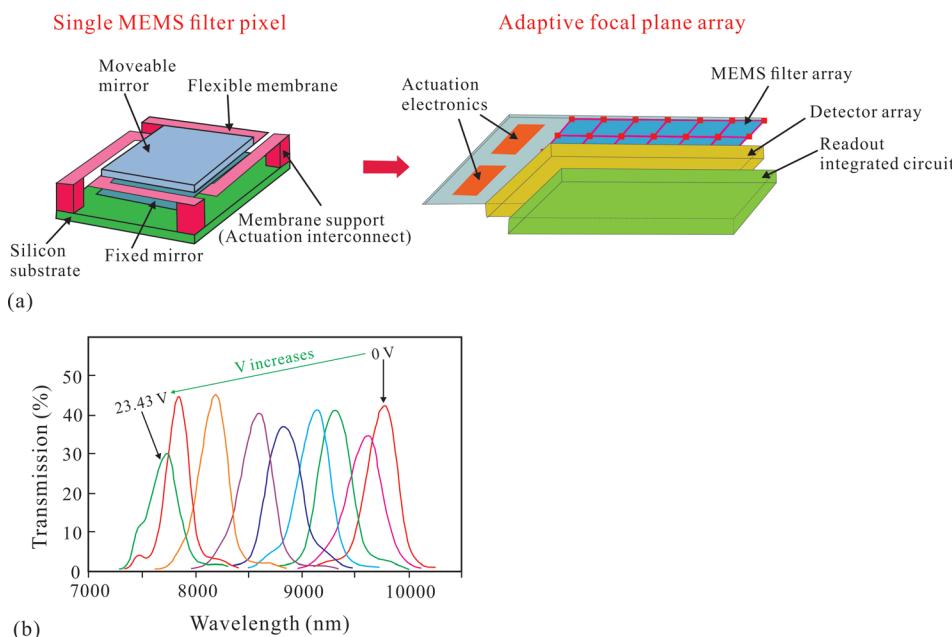


FIG. 30. (a) Schematic structure of the hybridized AFPA; (b) room temperature spectral transmission of the MEMS filter in the dual band adaptive FPA illustrating filter tuning in the LWIR band for various actuation voltages. Reproduced with permission from Gunning *et al.*, Proc. SPIE 6232, 62320F (2006). Copyright 2006 SPIE.

Numerous hybridized filter-detector technologies have also been developed at the UWA, including SWIR, MWIR, and LWIR wavelength bands (see Figure 28 and Refs. 187–189). These technologies are currently being extended to large area tuneable filter designs (multi-mm × multi-mm) in order to provide wavelength tuning capabilities to large-area 2D imaging FPAs.

The realization of adaptive concepts offers the potential approach to achieving real-time tuneable multiband detection which, under some circumstances, is more beneficial than broad-band multi-colour detection. This can result in dramatic improvements in critical military missions involving reconnaissance, battlefield surveillance, and precision targeting.^{185,186} Despite the great advances that have been made, it is still very challenging to fabricate these HgCdTe-based AFPAs. The main challenges or issues that need to be addressed include that:^{187,188} (1) the movable mirror plate needs to remain parallel or flat even at the maximum tuning range to achieve the required optical performance, especially for large-area MEMS optical filters; (2) a larger tuning range (parallel plate deflection) is required to enable a broader spectrum of light to be detected. The tuning range is determined by the tuning mode and the structure rigidity; (3) the membrane structure needs to be robust to any residual stress gradients which could be introduced into the structure during fabrication; and (4) the tuneable filters need to be capable of operating at cryogenically cooled temperatures, especially for the LWIR band. Obviously, the current research effort in this field is relatively small compared with that of other multi-band detection technologies, and more effort is required in order to address the significant technological challenges that still exist in this field.

VII. ADVANCED PLASMA DRY ETCHING TECHNOLOGY

For third generation IR technology, HgCdTe detectors and their FPAs are expected to have even smaller pixel size

(approaching the wavelength scale: Nyquist limit), higher pixel density, larger array format, as well as multi-band detection functionality, the fabrication of which is still very challenging for current plasma dry etching technology. To electrically and optically isolate individual small pixels (eliminating electrical and optical crosstalk between pixels), a smooth, highly anisotropic, low-damage plasma-etch process is needed to etch across the junctions without damaging them. For next generation IR detectors, new mesa and trench structures can be as deep as 10 μm (even several tens of micrometres for multi-junction structures), but as narrow as only 3–5 μm, which is very challenging. Because of the weak chemical bonds and narrow bandgap of HgCdTe materials, ion bombardment during plasma etching can also induce damage to the materials and, thus, some electrically active defects in the device structures, which will degrade the detector performance. In addition, third generation detectors may also require the fabrication of advanced optical architectures on the backside to enhance light absorption in the detectors, such as micro-lens and antireflective structures. All these challenges need to be addressed in order to fabricate next generation IR detectors and their FPAs.

Deep mesa and trench structures with high aspect ratio: There are two issues to be addressed in order to achieve the deep mesa and trench structures with high aspect ratio that are required by next generation IR detectors. One is etch lag and the other is lateral photoresist etching. In plasma etching of HgCdTe materials, the depth of an etched trench becomes smaller as its width becomes narrower. This phenomenon is usually called etch lag, which should be reduced or eliminated in actual device fabrication.²⁶ The etch lag is controlled by the IAD of the plasma, which is the distribution of ion motion relative to the normal of the HgCdTe material surface.^{195–197} One way to decrease the IAD and minimize etch lag is to increase the DC bias on the HgCdTe sample. Decreasing the IAD of the plasma allows for deeper, higher aspect ratio structures in the semiconductor.^{195–199} Another way is to use a multiple mask technique,¹⁶¹ which refers to

the mask combining a thin high selectivity mask such as SiO_2 and a thick low selectivity mask, generally of photoresist. With thin SiO_2 on top of the thick photoresist layer, the IAD of the plasma can be significantly reduced, which enables the etching of deep structures with high aspect ratio.²⁶

Another phenomenon that can cause issue with the plasma etching of HgCdTe is lateral photoresist etching. Large IAD can cause the photoresist to laterally erode, which causes the trench to bloom open, and can be more detrimental than the etch lag phenomenon.²⁶ Such an effect can be minimized by several techniques, including increasing the sample bias,¹⁹⁵ using thicker photoresist,²⁰⁰ hardening the resist,^{201,202} and careful resist development to create steep initial sidewalls in the resist.²⁰² By minimizing etch lag and reducing lateral photoresist removal, the aspect ratio and depth of features processed in HgCdTe can be greatly improved.^{195,200,203}

Plasma damage: As discussed in Section VD, plasma dry etching can cause structural damage to HgCdTe material, degrading its electrical properties. Such plasma damage should be minimized to achieve high detector performance. One way to minimize the plasma damage is to decrease the DC bias, which directly controls the sheath size of the plasma, and therefore the bombardment energy of the ions. As a result, it can greatly affect the bombardment energy of the plasma and the resulting damage to the sample. However, a large DC bias is needed for reducing the IAD of the plasma, which is desirable for etching deep structures with high aspect ratio. Therefore, care is needed when etching HgCdTe at higher biases, and a proper trade-off must be used when applying the DC bias. Another potential way to minimize plasma damage is to use a multiple mask technique,¹⁶¹ which has been discussed in Section VD.

Dual side processing: For current state-of-the-art HgCdTe detector technology, single side processing is sufficient since the active device structure incorporates only one or two junctions, and thus it is relatively easy to etch across the junctions and make metal contacts from a single side. However, future HgCdTe detectors may have absorber layers greater than $30 \mu\text{m}$ thick, with as many as four or more p-n junctions per pixel. Thus, contact vias for metallization to multiple diodes will be needed. Single sided processes limit the number of active device layers that can be accessed through these layers. Dual side plasma processing will enable designs that allow for a greater number of vias to be produced and deeper pixel delineation through these thick absorber layers.²⁰⁴ Figure 31 shows an example of a dual side plasma process flow proposed in Ref. 204. In addition to producing multiple vias, dual side processing will also allow complex structures like microlenses and anti-reflective structures²⁶ to be added to layers for enhancing light absorption in the detector active layer, which is required for fabricating next generation HgCdTe FPAs.

VIII. SUMMARY AND CONCLUSIONS

In summary, the current status of HgCdTe IR detectors and their future development trends have been reviewed and discussed in this work. It is predicted that HgCdTe -based IR

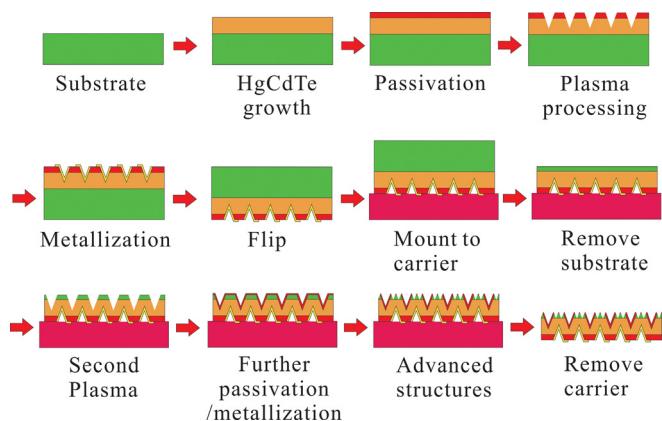


FIG. 31. Example of a dual side plasma process flow. Reproduced with permission from A. J. Stoltz and P. R. Norton “Dry etch development for a dual, front and backside, processing of ii-vi compound semiconductors,” in *Proceedings of the 2008 International Conference on Compound Semiconductor Manufacturing Technology*. Copyright 2008 CS MANTECH.

technology will continue to dominate the high performance end of the IR system market in the near future. The further development of IR applications requires that future IR detectors and their FPAs have features of lower cost, larger array format size, higher operating temperature, and multi-band detection, which are usually referred to as “third generation” infrared detectors. Although some advance has made in this direction, it is still a very challenging task to develop “third generation” HgCdTe IR detectors. However, opportunities co-exist with challenges. In this paper, various new concepts and technologies have been reviewed and discussed that have the potential to overcome the challenges existing in developing “third generation” HgCdTe IR detectors. In particular, the following technologies are expected to receive more attention: (1) efficient p-type doping without high temperature post-growth annealing; (2) new alternative substrates, such as GaSb , to improve epilayer quality and increase wafer size; (3) reduced pixel area and increased array format size; (4) high quality passivation (both surface and bulk); (5) reduction of detector material volume to reduce detector dark current; (6) barrier detector architectures to simplify fabrication processes, enhance detector yield, reduce detector dark current, and increase operating temperature; (7) high performance multi-color detectors and their FPAs; and (8) advanced plasma processing technology.

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