Microelectronic Engineering 87 (2010) 2218–2224

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Structural, electrical and magnetic characterizations of Ni/Cu/p-Si Schottky diodes prepared by liquid phase epitaxy

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ARTICLE INFO

Article history:
Received 17 October 2009
Received in revised form 5 January 2010
Accepted 8 February 2010
Available online 14 February 2010

Keywords:
Schottky diodes
Liquid phase epitaxy
Electrical and magnetic characterizations

ABSTRACT

In this paper, we have investigated the structural, electrical and magnetic characterizations of Ni/Cu/p-Si Schottky diode prepared by liquid phase epitaxy (LPE). Current density–voltage (*J–V*), capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) measurements were performed to determine the conduction mechanisms as well as extracting the important diode parameters. Rectifying properties were obtained, which definitely of the Schottky diode type. At low voltages, ($0 < V \leqslant 0.4$ V), current density in the forward direction was found to obey the diode equation, while for higher voltages, ($0.5 < V \leqslant 1.5$ V), conduction was dominated by a space-charge-limited conduction (SCLC) mechanism. Analysis of the experimental data under reverse bias suggests a transition from electrode-limited to a bulk-limited conduction process for lower and higher applied voltages, respectively. Diode parameters such as, the built-in potential, V_b, the carrier concentration, *N*, the width of the depletion layer, *W*, of the Ni/Cu/p-Si Schottky diode were obtained from the *C–V* measurements at high frequency (1 MHz). The capacitance–frequency measurements showed that the values of capacitance were highly frequency dependent at low frequency region but independent at high frequencies. The Ni/Cu/p-Si Schottky diode showed magnetic properties due to the effect of Ni in the heterostructure.

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1. Introduction

Development of modern electronic technologies is determined by new semiconductor materials which make the integrated devices possible to work in broad ranges of frequencies and temperatures [1]. The metal–semiconductor (MS) contacts have an important role in modern electronics [2–4]. During recent years, application of the surface and interface science techniques has shown clearly that interfaces formed between metals and semiconductors are complex regions whose physical properties depend on the preparation conditions of the surface because in many cases, contact metals are deposited onto surfaces covered by unknown contaminants which may cause the interface states and can affect the mechanical and electrical properties, performance, reliability and stability of metal–semiconductor (MS) devices [4–6].

Growth of Cu on Si is subject of extensive research not only due to the basic scientific interest but also due to the technological significance as one of the most relevant metal/semiconductor interface for modern devices technology. Peculiar feature of the Cu/Si interface is the large lattice misfit of about 15% [7–9]. At the interface, Silicide layer is known to be formed which plays a key role in overcoming the lattice mismatches [7–10]. On the top of silicide interlayer an epitaxial Cu films grow in the layer-by-layer.

Interfaces between thin metal layers and semiconductors are used in optical detector, solar cells [11] and chemical sensors [12–14]. The transport properties of such Schottky diodes and the dependence of transport parameters on metal thickness and preparation are of essential importance for the device performance.

M/Si (M = Ni, Fe] system has been extensively studied, using Cu as a buffer, because of the interestingly low resistivity of the metal silicide phase along with its compatibility with Si integrated circuit technology [15]. Moreover, thin Ni films grown on Si substrates are a typical material that shows the magnetic anisotropy depending on the thickness of films [16].

There are various methods of preparing Ni/Cu on single crystalline Si such as vacuum-based deposition (sputtering, thermal evaporation) or the wet chemical deposition (sol–gel, electrodeposition, ...) techniques [16–18]. In this work, deposition of Ni/Cu onto Si substrate was carried out by applying a liquid phase epitaxy (LPE) which has many advantages in fabricating metal films on semiconductor substrates. In general, it is well known that we can expect that thin metal films grown by LPE will exhibit very different structural characteristics comparing with that obtained by vacuum or wet chemical deposition techniques. However, to the best of our knowledge there is a little report on the growth of such diode by LPE technique.

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0167-9317/$ - see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2010.02.006

Our epitaxial Ni films were grown by liquid phase epitaxy. The substrate is the reconstructed surface of Si (1 1 1) covered by a Cu buffer layer, 30 nm thick, which completely relaxes the mismatch with the Si [19]. These processes are developed for their implementation in the fabrication of magnetic micro-actuator devices in Si technology [19], based on the integration of LPE onto Si substrates. In principle, Cu and Ni are well suited for microsystem applications in Si technology, owing to their low resistivity, low cost and ease to grow electrochemically in a well-controlled way. Ni has also interesting magnetic properties for the development of magnetic sensors and actuators microsystems, and is easier to deposit electrochemically than other magnetic alloys, such as Ni–Fe [20]. Additionally, the growth of Ni/Cu multilayer structures on Si have a good epitaxial structure. In this paper, in order to achieve a better understand of the diode structure, SEM and XRD were studied. The current density–voltage and capacitance–voltage characteristics as well as capacitance–frequency characteristics in dark were measured. Also, the aim of this research was to establish magnetic characteristics of the Ni/Cu/p-Si Schottky diode.

2. Experimental procedure

2.1. Diode fabrication technique

In the present work, liquid phase epitaxy (LPE) was used for preparation Ni/Cu/p-Si heterostructure. The LPE technique was employed to grow layers of Ni/Cu on p-Si substrate single crystalline wafers using indium as a solvent. The multibin boat made of special graphite hardness is held in a fixed position within a silica tube, and a thermocouple is fixed under the boat. The system is usually evacuated to 10^{-2} Pa. Prior to the growth run, purified argon is passed through the tube .The technique of LPE is described in detail elsewhere [20–22]. The boat was loaded with the p-Si substrates single crystal with orientation (1 1 1). The two growth solution contained indium with Cu pieces and indium with Ni pieces. The loaded boat was heated up to 1073 K and kept at this temperature for 30 min to homogenize the solution and then cooled down with a cooling rate of 0.5 K/min for deposited copper layer on Si as a seed layer for the deposited Ni layer.

3.2. Characterization techniques

X-ray diffraction measurements have been taken by using analytical X'Pert PRO MRD diffractometer System having Cu K_α, as a radiation source of wavelength $\lambda = 1.540598$ Å with $2\theta = 30°–80°$ at the scan speed 0.5 K/min for the determination of Ni/Cu/p-Si heterostructure. The analysis has been performed by using Powder X Software.

Scanning electron microscope model JOEL14775 was used to study the surface morphology of the Ni/Cu/p-Si heterostructure.

Ohmic contacts of gold (Au) and Al were deposited on Ni and p-Si, respectively, by thermal evaporation under a vacuum of 10^{-4} Pa. The devices had an active area of $\sim$1 cm^2.The schematic diagram of the device is shown in Fig. 1.

In order to measure the electrical properties of the devices, electrical contacts were equipped with copper wires mechanically applied to the two metal electrodes using thermosetting silver paint. The current flowing through the sample was determined using a stabilized power supply and a high-impedance Keithley 617 electrometer. Electrical properties were performed in dark over the temperature range 305–398 K. The temperature was measured directly by means of chromel–alumel thermocouple connected to hand-held digital thermometer. The capacitance–voltage (C–V) measurements were performed at high frequency of 1 MHz and the capacitance–frequency measurements were done at various

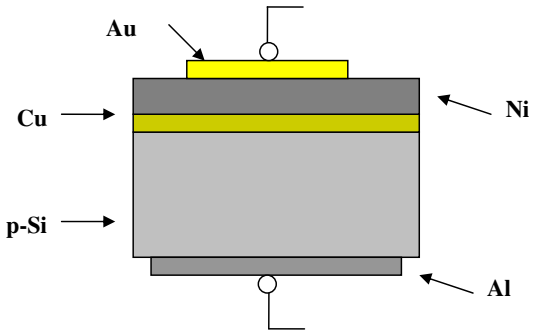

Fig. 1. Schematic diagram of Ni/Cu/p-Si Schottky diode.

frequencies by using HIOKI 3532-50 LCR Hi-TESTER impedance analyzer at different temperatures in dark at room temperature (305 K).

The magnetic properties of Ni/Cu/p-Si device has been determined using a vibrating sample magnetometer under a maximum applied field of about 10 kOe.

3. Results and discussion

3.1. structural characterizations

Fig. 2a shows the surface topography of the epilayers of Ni/Cu/p-Si structure prepared by liquid phase epitaxy (LPE). It is clear

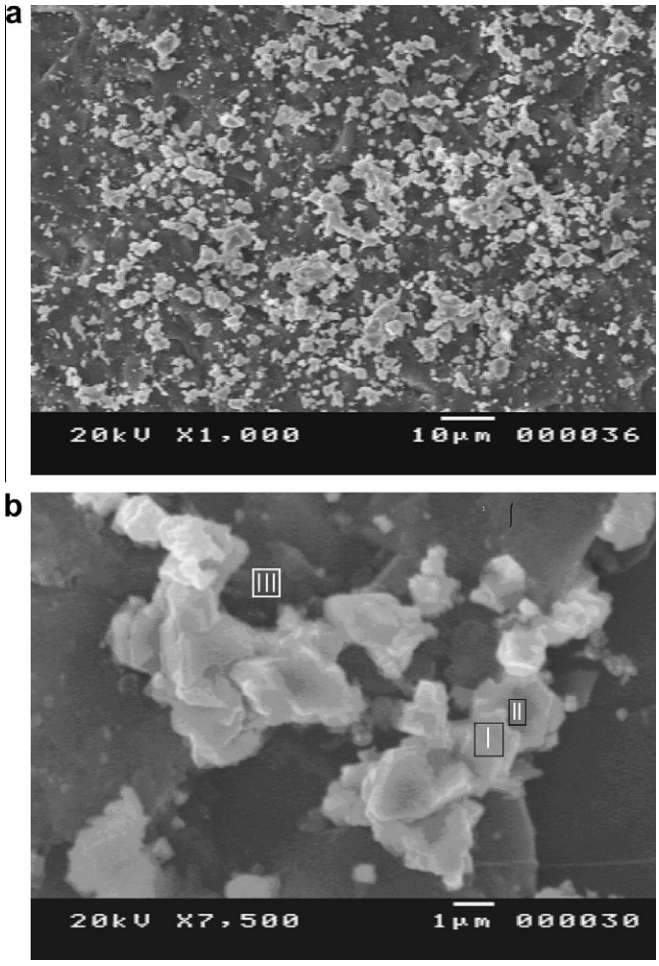

Fig. 2. SEM of of Ni/Cu/p-Si Schottky diode at different magnifications (a) 1000× (b) 7500×.

from SEM image that the film posses a nearly uniform defined structure of grains with size of 1–5 μm. Also, SEM micrograph shows a high island nucleation density and the islands appear not identified shape and are randomly distributed across the surface due to the high agglomeration. The high magnification (7500×), shown in Fig. 2b, illustrates three well identified regions. Region I which has a highest brightness referred to the upper layer, i.e. Ni , while region II represents the copper layer and finally, region (IIII) can represent the CuSi buffer layer between the Si wafer surface and Cu epilayer.

Fig. 3. shows the X-ray diffraction trace for the Ni/Cu/p-Si heterostructure. The indexing for the diffraction peaks was made on the pattern. As observed, The XRD pattern is corresponding to the planes of the structure of Si, Cu, Ni and copper silicides, $Cu_{0.83}SiO_{2\ 0.17}$. No additional diffraction peaks associate with other formation has been observed indicating the high quality for the growth. It is well known that the silicides layer play an important role in decreasing the mismatch between Cu and Si, and is considered a seed layer for formation and growth of Cu and Ni. The results of XRD confirm the above obtained by scanning electron microscope.

3.2. Forward bias characteristics

Electrical characteristics of Ni/Cu/p-Si Schottky diodes were monitored as a function of forward and reverse bias conditions at studied temperature interval (305–398 K) and illustrated in Fig. 4. The forward bias corresponds to the case where the p-Si is connected to the positive output of the current source. These characteristics exhibit a remarkable rectifying behavior of the devices in dark. This behavior can be understood by the formation of Schottky contact , in which the barrier at the interface limits the forward and reverse carriers flow across the junction, where the built-in potential could be developed [23,24].

The rectification ratio was calculated for the investigated device versus temperature at different voltages as shown in the inset of Fig. 4. The rectification has been confirmed [25–29] as a result of the formation of the Schottky junction at the interface of Cu/p-Si and the ohmic contact at p-Si/Al. At the Schottky junction, electrons transfer from Cu to p-type semiconductor (p-Si) until the electronic potentials of Cu and p-Si come to be in equilibrium

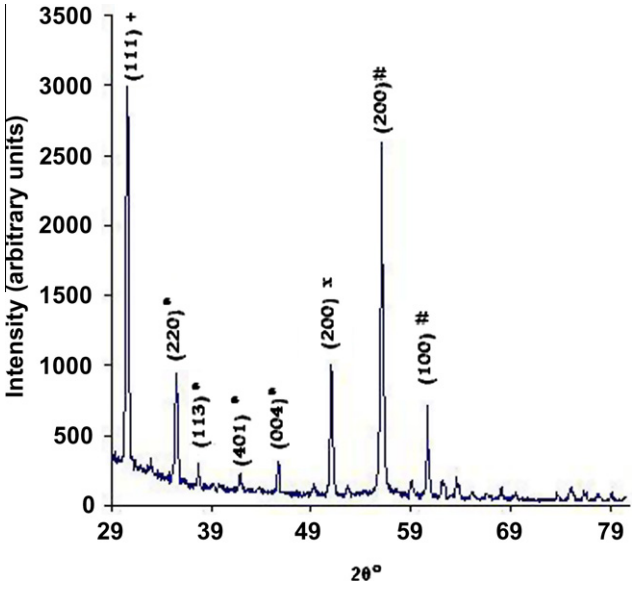

Fig. 3. XRD of Ni/Cu/p-Si Schottky diode, $^{+}$Si, $^{*}Cu_{0.83}SiO_{2\ 0.17}$, ^{x}Cu, $^{\#}$Ni.

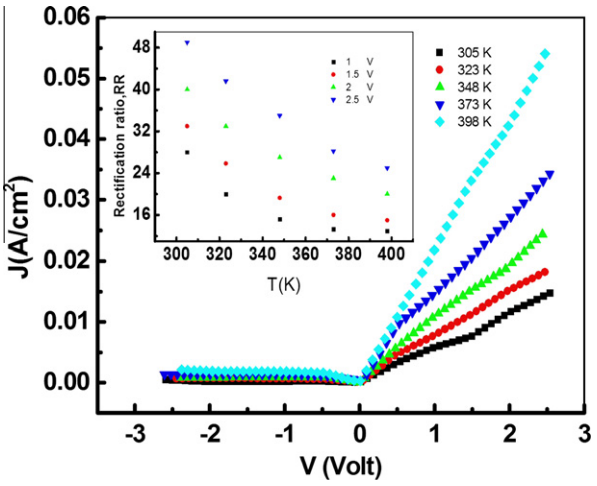

Fig. 4. *J–V* characteristics of Ni/Cu/p-Si Schottky diode at different temperatures in the range 305–398 K. the inset shows the temperature dependence of *RR*.

[30]. This is caused by the difference of work function of Cu and p-Si, resulting in the built-in potential V_b. The transferred electron fills up p-type acceptors and forms the insulating depletion layer with negative space charges and built-in field. As depicted in the inset of Fig. 4, Ni/Cu/p-Si Schottky diodes have a clear rectifying property and became deteriorate as ambient temperature increases. This behavior may be attributed to the decrease of the built –in potential as the temperature increases. As explained in [31–34], since current transport across the metal/semiconductor (MS) interface is a temperature-activated process; electrons at low temperatures are able to surmount the lower barriers and therefore the current transport will be dominated by current flowing through the patches of lower Schottky barrier height and a larger ideality factor. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant barrier height will increase with the temperature and bias voltage. An apparent increase in the ideality factor and a decrease in the barrier height at low temperatures are caused possibly by other effects such as inhomogeneities of thickness and non-uniformity of the interfacial charges. This gives rise to an extra current such that the overall characteristics still remains consistent with the Thermionic emission process.

Current transport in Schottky contacts is due to majority carriers and it may be described by thermionic emission over the interface barrier [15] .The thermionic current can be written as

$$J = J_0 \exp\left[\left(\frac{qV}{\eta kT}\right) - 1\right] \tag{1}$$

where, q is the electron charge, V is the applied voltage, k is the Boltzmann's constant, T is the temperature, η is the ideality factor and J_0 is the reverse saturation current density and given as;

$$J_0 = A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \tag{2}$$

where, A is the diode area, A^* is the Richardson constant, and Φ_B is the barrier height. Ideality factor of Ni/Cu/p-Si Schottky diodes was calculated from the slope of the linear part of the forward bias semilogarithmic J–V characteristic and can be expressed as

$$\eta = \frac{q}{kT}\left(\frac{dV}{d\ln J}\right). \tag{3}$$

Moreover, Φ_B can be extracted through determination of J_0 which was the extrapolated value of forward $\ln J$–V curve. Therefore, Φ_B could be estimated through the following equation

$$\Phi_B = \frac{kT}{q}\left(\frac{\ln A^* T^2}{J_0}\right). \quad (4)$$

In the voltage region $0 < V \leqslant 0.4$ V of Fig. 4, the ideality factor and barrier heights were calculated, using Eqs. (3) and (4), respectively. Temperature variations of ideality factor and barrier height of Ni/Cu/p-Si are depicted in Figs. 5 and 6, respectively. Obviously, the ideality factor decreases as the temperature increases and the barrier height increases as the temperature increases. This type of dependency on temperature can be figured out due to the inhomogeneous of barrier height and/or the interfacial layer of the metal-semiconductor [17]. The barrier heights of Ni/Cu/p-Si changed between 0.69 eV and 0.76 eV while the ideality factor varied between 1.88 and 1.59 as the temperature increases between 305–398 K. Case of η greater than unity ($\eta > 1$) implies Schottky diode is not ideal [35,36]. One reason for that might be the density of the interface state exists between metal and semiconductor junction. The other reason for that may be attributed to either recombination of electrons and holes in the depletion region, and/or the increase of the diffusion current due to increasing applied voltage [37].

Several authors [38–40] reported that the decrease in the barrier height, BH value and the increase in the ideality factor with decreasing temperature have obeyed the single-Gaussian distribution (GD) of the BHs, which is caused by the presence of the spatially inhomogeneous potential at the MS interface. Also, as stated in [40–42], the BH is likely a function of the interface atomic structure, and the atomic inhomogeneities at the MS interface which are caused by non-uniformity of the interfacial charges, grain boundaries, multiple phases, facets, defects, a mixture of different phases and inhomogeneities in the composition of the interfacial layer thickness, etc.

The series resistance is a very important parameter of the Schottky diode. The series resistance of the Ni/Cu/p-Si Schottky diode is investigated in the temperature range 305–398 K. Here, the series resistance was evaluated from forward bias J–V data using the method developed by Cheung [43]. One can also obtain the series resistance of the Schottky diode using approaches described in [44–46]. The forward bias J–V characteristics due to thermionic emission of a Schottky contact with series resistance can be defined as

$$\frac{dV}{d(\ln J)} = JR_s + \eta\left(\frac{kT}{q}\right), \quad (5)$$

Fig. 7 shows the experimental plot of $dV/d(\ln J)$ versus J for different temperatures for the Ni/Cu/p-Si Schottky diode. Eq. (5) should give a straight line for the data of the downward region

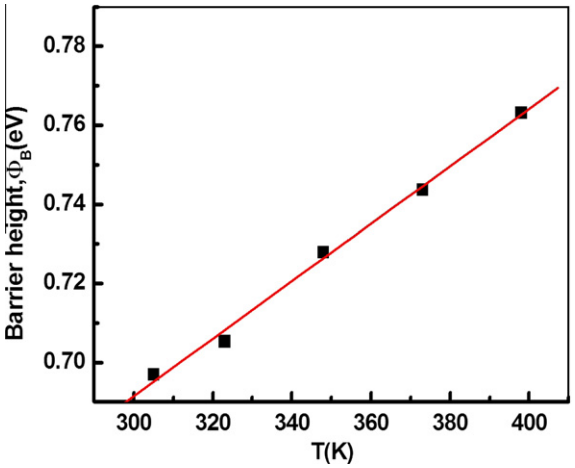

Fig. 5. Temperature dependence of Φ_B.

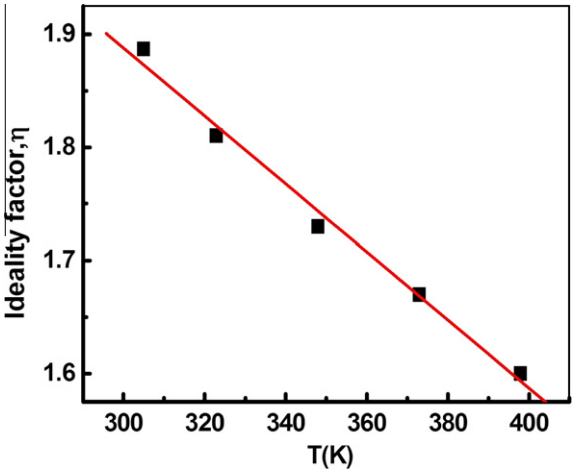

Fig. 6. Temperature dependence of η.

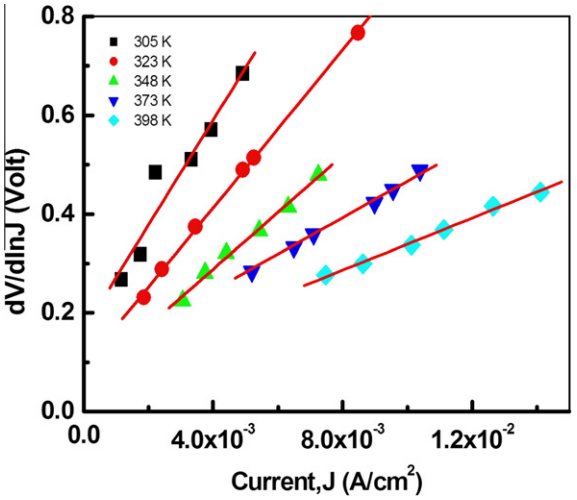

Fig. 7. Experimental $dV/d(\ln J)$–J curves of Ni/Cu/p-Si Schottky diode at different temperatures in the range 305–398 K.

in the forward bias J–V characteristics. Thus, a plot of $dV/d(\ln J)$ versus J will give R_S as a slope and $\eta(kT/q)$ as the y-axis intercept. Thus, the series resistance (R_S) values are calculated from Eq. (5) for each temperature and given in Table 1. As shown in Table 1, the increase of R_S with fall in temperature is believed to result due to factors responsible for the increase of ideality factor and lack of free carrier concentration at low temperatures [47].

At relatively high forward voltages ($0.5 \leqslant V \leqslant 1.5$ V), a different mechanism is operating. As observed in Fig. 8, the current shows a power-law exponent of the form $J \alpha V^m$. *The* m values are calculated from the slopes of the $\ln J$–$\ln V$ characteristics and changes between 2.4 and 3.7. This suggests a SCLC mechanism [48], where current increases superlinearly, i.e., $m > 2$ suggests that the traps are exponentially distributed. The slope m was found to decrease with increasing the temperature. The temperature dependence of m value is shown in the inset of Fig. 8, where linearity in the figure is observed. This linearity confirms a SCLC model controlled by an exponential distribution of traps. The power-law dependence between current and voltage is characterized by space-charge-limited currents. Therefore, the current is expressed as [48,49]

$$j = \frac{e\mu N_V}{d^{2l+1}}\left(\frac{\varepsilon\varepsilon_0}{eP_0kT_t}\right)^l V^{l+1} \quad (6)$$

Table 1
Some electrical parameters of Ni/Cu/p-Si Schottky diode.

T (K)	R_s (Ω cm^2)	T_t (K)	β_1 (eV m$^{1/2}$ V$^{-1/2}$)	β_2 (eV m$^{1/2}$ V$^{-1/2}$)
305	106	823.5	3.4×10^{-5}	2.4×10^{-5}
323	80	671	2.7×10^{-5}	2.1×10^{-5}
348	57	597.8	4.5×10^{-5}	1.9×10^{-5}
373	38.5	478.5	5.5×10^{-5}	1.7×10^{-5}
398	26.5	408.7	4.5×10^{-5}	1.8×10^{-5}

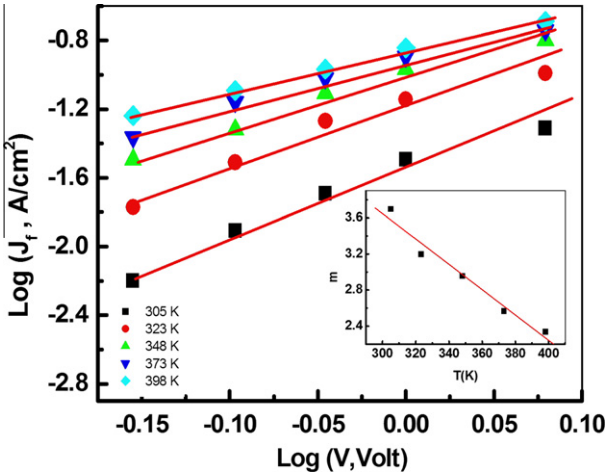

Fig. 8. J–V characteristics at high voltage region ($0.5 < V \leqslant 1.5$ V). The inset shows the temperature dependence of the slope m.

where, ε is the dielectric constant of the semiconductor, ε_o is the permitivity of free space, e is the electronic charge, μ is the mobility of carrier charges, N_V is the effective density of states in valence band edge, d is the thickness, l is a parameter given by $l = T_t/T$, T_t is a characteristic temperature of the exponential distribution of the traps [48].

3.3. Reverse bias characteristics

Under reverse bias conditions, the J–V characteristic at different temperatures in the range 305–398 K, shown in Fig. 4, exhibits lower current levels when compared with the J–V characteristic obtained under forward bias, indicating the existence of a current limitation mechanism, induced either by the Schottky or the Poole–Frenkel effect. Current density–voltage expressions for both mechanisms are given as [50]

$$J = A^{**}T^2 \exp\left(\frac{\Phi_s}{kT}\right) \exp\left(\frac{\beta_s V^{1/2}}{kTd^{1/2}}\right), \tag{7}$$

for Schottky effect, and

$$J = J_0\left(\frac{\beta_{PF} V^{1/2}}{kTd^{1/2}}\right), \tag{8}$$

for the Poole–Frenkel effect. In Eqs. (7) and (8), Φ_s is the Schottky barrier height at the injecting electrode interface, $J_0 (= \sigma_0 F)$ is the low-field current density, and Φ_s and Φ_{PF} are, respectively, the Schottky and Poole–Frenkel field-lowering coefficients. Theoretical values for both Φ_s and Φ_{PF} are given by

$$2\beta_s = \beta_{PF} = \left(\frac{e^3}{\pi\varepsilon}\right)^{1/2}, \tag{9}$$

Since $\varepsilon = 1.044 \times {}^{-10}$ F m^{-1} [51], the theoretical values of $\beta_S = 1.10 \times 10^{-5}$ and $\beta_{PF} = 2.20 \times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$ were calculated. It is evident from Eqs. (7) and (8) that the experimental values for the coefficient β can be obtained by plotting the reverse bias characteristic in the form of semilog J versus $V^{1/2}$ as shown in Fig. 9. It can be seen from the figure that the curve consists of two distinct linear sections. From the slope of the lower voltage section a value of β_1 was derived. A value for the coefficient β_2 was also calculated from the gradient of the linear portion of the curve in the higher voltage range. The values of β_1 and β_2 were listed in Table 1 for the temperature range 305–398 K. Nevertheless, the derived value of β_1 from the lower voltage region is at variance with that expected for the Schottky effect, being 3.7 times the theoretical value for β_S. This difference may be attributed to a thermally assisted tunnelling field emission of carriers occurring at the peak of the barrier where the effective barrier width is very narrow. Alternatively, other workers [52,53] have explained this difference in terms of a Schottky depletion region extending only in a distance d_S and not across the entire Si layer.

The value of β_2 derived from the higher voltage range is in good agreement with that expected for the Poole–Frenkel effect being $\sim$0.9 the theoretical value of β_{PF}. This difference may be attributed to the non-uniform electric field within the bulk of the Si layer [54].

3.4. Capacitance–voltage characteristics

Fig. 10 shows the C^{-2}–V characteristics of the Ni/Cu/p-Si Schottky diode measured in dark at room temperature (305 K) and at frequency 1 MHz. From this point of view we can obtain information about the depletion region extending in the p-Si side. It is clear that C^{-2} increases linearly with increasing the reverse applied voltage indicating that the junction is an abrupt junction. The relation between the junction capacitance, C, and the reverse applied potential for an abrupt junction can be given by the Schottky equation [36]:

$$C^{-2} = \frac{2(V_b - V - kT/e)}{e\varepsilon NA^2}, \tag{10}$$

where, V_b is the built-in potential, N is the free carrier concentration, A is the effective area ($\approx 10^{-4}$ m^2) and ε is the dielectric constant of p-Si .The carrier concentration can be estimated experimentally from the relation:

$$\frac{d(C^{-2})}{dV} = \frac{-2}{e\varepsilon NA^2} \tag{11}$$

where, $\frac{d(C^{-2})}{dV}$ is the slope of the straight line and the intercept with the horizontal asymptote gives the built-in potential, V_b. The

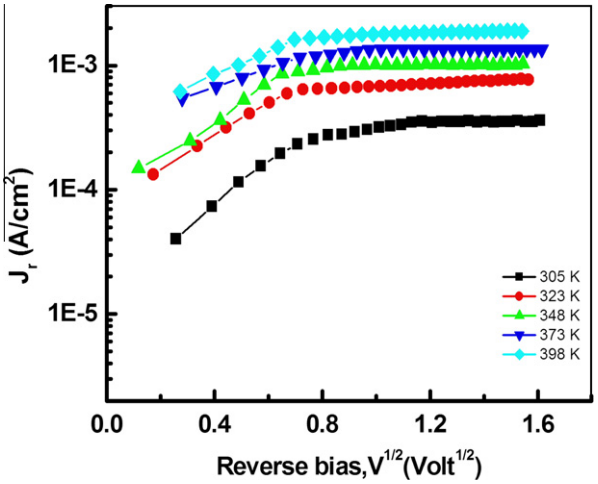

Fig. 9. Plot of J_r vs. $V^{1/2}$.

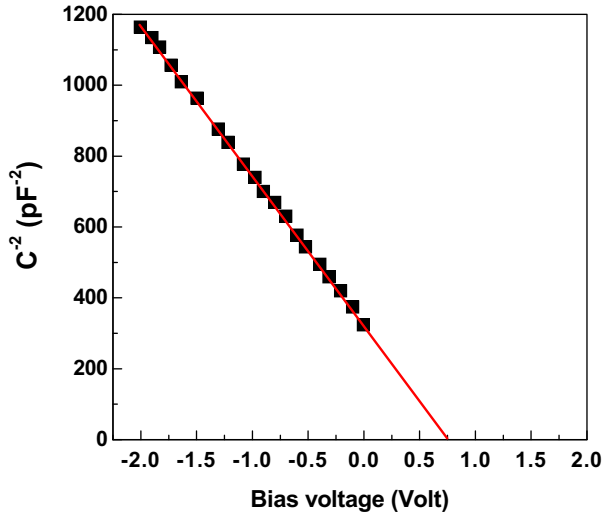

Fig. 10. The variation of $1/C^2$ versus bias voltage at 305 K.

asymptote is interpreted to represent the series geometrical capacitance. The carrier concentration and the built-in potential were estimated to be 9.4×10^{14} cm^{-3} and 0.75 V, respectively. The value V_b obtained from the C–V measurements is in agreement with the value of the potential height, Φ_b, that obtained from the J–V measurements at 305 K. The width of the depletion layer, W, is related to the junction capacitance at $V = 0$ V, C_0 by the relation [36,55]:

$$W = \frac{\varepsilon A}{C_0} \tag{12}$$

and the maximum electric field is given by

$$E_{max} = \frac{2V_b}{W} \tag{13}$$

The values of W and E_{max} are estimated to be 0.75 μm and 2 V/μm, respectively.

3.5. Capacitance–frequency characteristics

Fig. 11 shows the capacitance measurements as a function of frequency in the range 40 Hz–1 MHz. In idealized case, C–f characteristics are usually frequency-independent. In general, the interface states in equilibrium with the semiconductor do not contribute to the capacitance at sufficiently high frequencies because the charge at the interface states cannot follow the ac signal. In this case, the capacitance of the diode is the only space charge capacitance [56]. The capacitance–frequency measurements give the density distribution of the interface states, the energy distribution of the interface states and the time constants for rectifying contacts. As can be seen in Fig. 11, the capacitance is highly dependent on frequency especially at high frequencies. When the frequency was increased further, the capacitance remained almost constant up to a certain value in the higher side of the frequency scale .The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states that can follow the ac signal. The frequency dependence is due to the particular features of a Schottky barrier, impurity level, high series resistance, etc. At high frequency, the measured capacitance is dominated by the depletion capacitance of the Schottky diode, which is frequency-independent. As the frequency is decreased, the total diode capacitance is affected not only by the depletion capacitance, but also by the bulk resistance and the dispersion capacitance, [15,57]. The higher values of capacitance at low frequency are due to the excess capacitance resulting from the interface states in equilibrium with the p-type Si that can follow the ac signal.

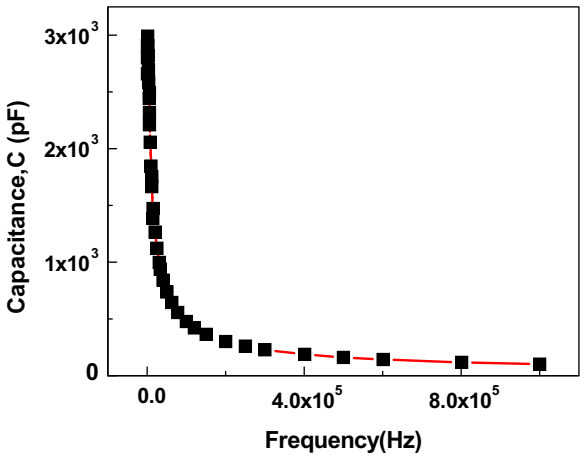

Fig. 11. The frequency dependence of capacitance at 305 K.

3.6. Magnetic characteristics

The magnetic properties of a Ni/Cu/p-Si heterostructure are usually characterized by a DC hysteresis loop, which gives the behavior of a material when excited by an external magnetic field. Fig. 12 shows a typical hysteresis loop for a ferromagnetic material.

The initially demagnetized sample material (point O in Fig. 12) is subjected to a positive external magnetic field of strength H, inducing an internal magnetic field of strength B. The applied field is gradually increased, giving the magnetization curve. When no further increase in magnetic induction or magnetization is achieved by increasing the applied magnetic field (point C), the material is said to be saturated. This is the point of maximum or saturation induction (B_{max} = 0.187 emu/g). If the applied magnetic field is then gradually reduced to zero, two phenomena are observed. The first is that the decrease in the internal field takes place along a different curve. The second is that there remains a field of strength (B_r = 0.43 emu/g) in the material. This is referred to as remanence. This remaining flux density can be cancelled by applying a negative magnetic field, at which point the applied field is called the coercive force (H_C = 353 Oe). By progressively increasing the applied field in the negative range, the material once again

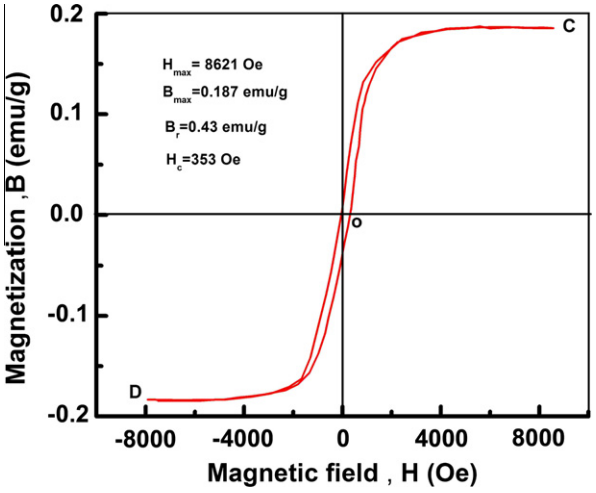

Fig. 12. Hysteresis loop of Ni/Cu/p-Si heterostructure.

reaches saturation (point D). If this cycle of applied field is then reversed, the hysteresis loop is closed (line DC).

The area of the *B–H* loop shown in Fig. 12 represents the work done to change the magnetization of the material, or the *hysteresis losses*: the larger the loop, the greater the losses. These losses are related to the level of defects in the material structure, which restrict the movement of magnetic domains.

4. Conclusion

The structural characteristics of Ni/Cu/p-Si heterostructure prepared by LPE were identified using SEM and XRD. The electrical properties were investigated through *J–V* and *C–V* measurements. The ideality factor of Ni/Cu/p-Si Schottky diodes decreased with the increase in temperature but the barrier height increased. Two different conduction mechanisms were identified for the investigated diode at low and high forward bias. Under reverse bias the current is induced by the Schottky or the Poole–Frenkel effect at low and high reverse bias, respectively. There is an agreement between V_b obtained from the *C–V* measurements at high frequency and Φ_b obtained from *J–V* measurements at 305 K. The capacitance–frequency dependence of Ni/Cu/p-Si showed higher value of capacitance at lower frequencies and decreased with increase in frequency. The magnetic properties of the Ni/Cu/p-Si heterostructure were observed through the hysteresis loop. However, the exact nature of magnetic behavior of this structure needs further study.

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