Impact of Defect Engineering on High-Power Devices

*Jan Vobecký**

Prof. J. Vobecký
Hitachi – ABB Power Grids
Fabrikstrasse 3, Lenzburg, CH-5600, Switzerland
E-mail: jan.vobecky@hitachi-powergrids.com

Prof. J. Vobecký
Department of Microelectronics
Faculty of Electrical Engineering
Czech Technical University in Prague
Technická 2, CZ-166 27, Praha 6, Czech Republic
E-mail: vobecky@fel.cvut.cz

Keywords: silicon, silicon carbide, defect engineering, contamination, diode, thyristor, IGBT

Abstract. Processing of electrical power at megawatt to gigawatt level in the industry, traction, and transmission and distribution requires high-power devices with blocking capability up to 10 kV. The mainstream ones require high purity silicon wafers with the lowest possible defect content (contamination) and maximal homogeneity of resistivity and thickness. To satisfy current ratings in typical range 1 - 6 kA, single diode or thyristor may occupy nearly the whole 100 to 150 mm silicon wafer. Beside the doping profile optimization and gettering in the front-end processes, the devices are subject to defect engineering to adjust uniformly or locally the recombination lifetime of carriers. In IGBTs, it is also about dopant activation below 500 °C. Satisfaction of all extremal demands laid on those devices would not be possible without the knowledge developed by defect engineering community in the past decades. Some relevant industrial examples of screening the contamination in typical production of silicon high-power devices are demonstrated as well as the advanced defect engineering methods for increasing device functionality and power density.

This article has been accepted for publication and undergone full peer review but has not been through the copyediting, typesetting, pagination and proofreading process, which may lead to differences between this version and the Version of Record. Please cite this article as doi: 10.1002/pssa.202100169.

1. Introduction

Power electronics is the key enabler of clean energy generation and transmission, bulk storage, and efficient utilization. The importance of energy savings grows with the magnitude of processed power. The minimization of the energy loss of a given high-power system then goes hand in hand with increased voltage ratings, provided that individual components enable it both technically and costwise. We further focus on power semiconductors, one of the key enablers for state-of-the-art green technologies. We concentrate on the silicon devices, which dominate the industrial segments with the highest possible power ratings.

Thanks to the commercial introduction of the Float-Zone Neutron Transmutation Doped (FZ NTD) silicon with a more uniform distribution and a tighter tolerance of the resistivity in the late 1970s, the field of power semiconductors passed the 2.5 kV level.[1] In the coming decades, the maximal industrial voltage ratings have saturated at about 10kV level, which became a practical limit for silicon technology dictated by cost efficiency. Continuous development of silicon ingot pulling technology towards larger wafer diameters increased the production efficiency of silicon high-voltage diode and Insulated Gate Bipolar Transistor (IGBT) chips (BiMOS = Bipolar MOS) and allowed for record high current ratings of discrete diodes and thyristors (Bipolar). At present, the mainstream of industrial BiMOS high-power devices is represented by power modules with fast recovery diode and IGBT in the voltage classes from 3.3 to 6.5 kV rated between 1 and 3.6 kA, while targeting 5 kA in the future. While the high-voltage segment is running on 150 and 200 mm wafers, the lower voltage classes are already produced at 300 mm wafers. The mainstream of industrial high-power bipolar devices is represented by hermetic hockey-puck housings with circular wafers 50 to 150 mm in diameter, voltage ratings between 4.2 and 8.5 kV, and current rating up to 6.5 kA. The production of all those devices requires a deep knowledge of defect engineering principles. Some relevant examples are illustrated below.

2. Starting Silicon

The blocking capability in the kV range requires deep p-n junctions and surface passivation of junction termination (JT) by thin layers with high electrical strength. The BiMOS chips are terminated by a planar JT produced at a flat surface before sawing to individual chips. As the diffused planar JT structures must be at least equally deep as that of the blocking junction in the bulk, the depth of blocking junctions of contemporary BiMOS devices are typically in units of μm with maximum around 25 μm in the diodes. Then the defect engineering activities are rather about the identification of possible contamination sources, lifetime engineering to increase the dynamic safe operation area (SOA), and processing of doping layers (buffers) with low thermal budget represented by hydrogen shallow donors and laser annealing.

The large area discrete bipolar devices amount 50 – 150 mm in diameter and are provided with JT manufactured by mechanical grinding at the wafer edges just before passivation, testing and packaging. Such termination structures require bocking junctions 40 – 180 μm deep depending on the voltage class between 1 and 10 kV, design of the JT (positive or negative bevel), and application (50/60 Hz or fast). The diffusion species are Boron, Gallium, Aluminum and Phosphorus. They can be deposited at wafer surface from liquid or gas sources to provide the highest possible surface concentration of dopants. The resulting high injection efficiency is the prerequisite of the lowest possible ON-state voltage drop. The Boron, Aluminum and Phosphorus can be also implanted with the advantage of a good control of low doping concentrations and minimal contamination. The disadvantage is a lower activation of dopants, especially with the Aluminum. Anyway, it is only the Aluminum, which provides the junction depths above 50 μm at a reasonable diffusion time. Despite this, the drive-in time of Aluminum doping layer for the voltage classes of 6.5 kV and above can still amount at 40 to 70 hours depending on diffusion temperature, which is typically 1200 °C and not much higher.

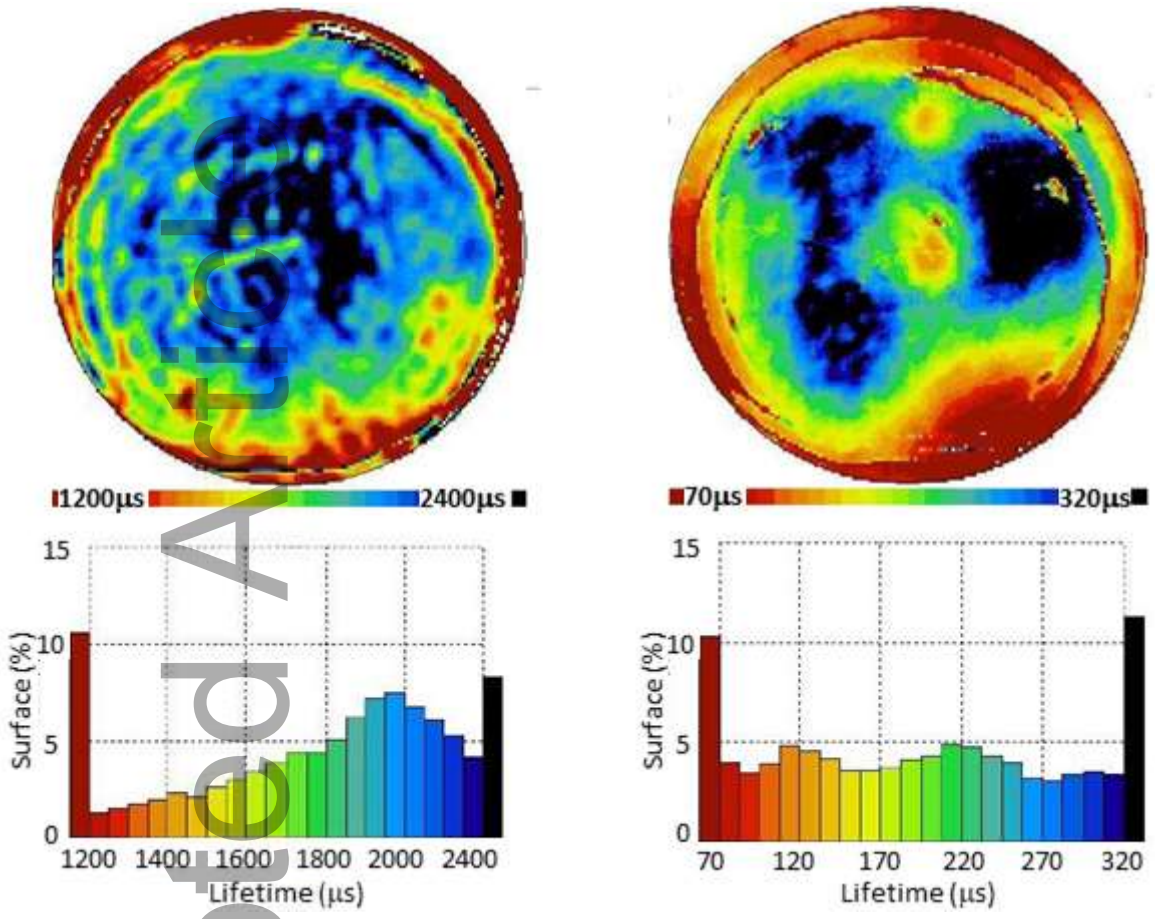

Figure 1. Lifetime profile of 150 mm Silicon FZ NTD wafer before (left) and after oxidation step at 1100°C (right).

The long diffusions require starting silicon with minimal concentration of grown-in defects to minimize their possible decoration by metal contaminants in subsequent production [2, 3, 4]. To minimize the concentration of defects in devices with very high thermal budget, the wafers can be pre-processed using oxidation and gettering by surface Phosphorus layer from $POCl_3$. **Figure 1** illustrates the effect of oxidation step at bare wafers. The spatial distribution of carrier lifetime is obtained from microwave photoconductance decay (µ-PCD) measurement from Semilab. After oxidation, the lifetime profile flattens out as well as the profile of resistivity (not shown here). The low lifetime rings at the wafer edges are still to be removed by matching the ratio of pulling rate to

temperature gradient at the solidification interface during crystal pulling (relative to the critical limit for producing the larger densities of interstitial clusters - B-defects) to a dissolution anneal at appropriate temperature and ambient and $POCl_3$ gettering prior to the front-end process in Bipolar production line to avoid the decoration of the remaining interstitial clusters by contaminants in subsequent high-temperature diffusion steps. Of great importance is also the contamination-free surface treatment during wafering process.

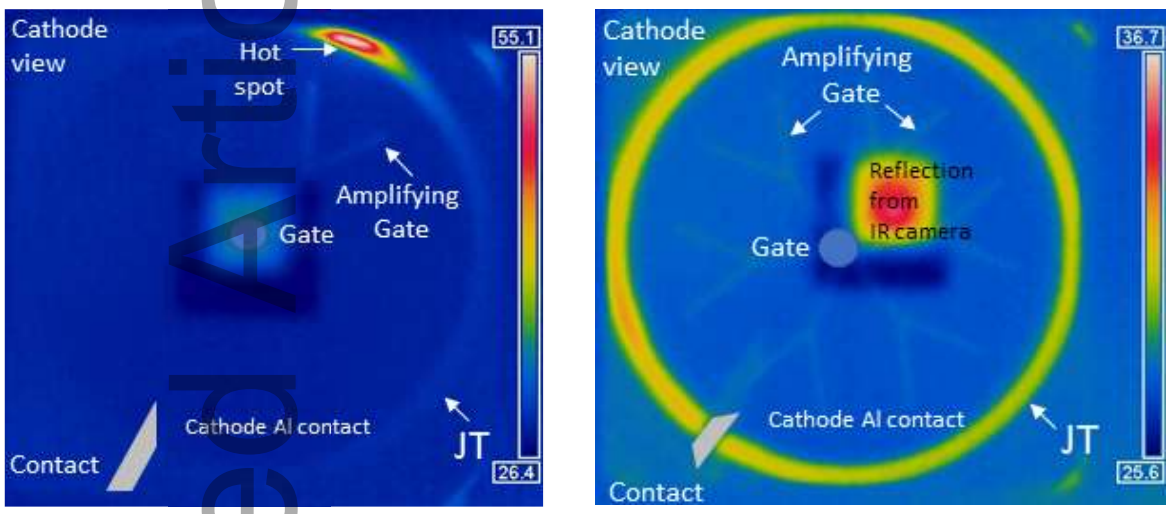

Figure 2a. Infrared image of a thyristor for HVDC produced at silicon wafer 150 mm in diameter. Single hot spot at junction termination (JT) detected already at1/3 of rating voltage (left). A uniform heating of JT by leakage current at full blocking voltage of the same device design above 7 kV (right). The artifact of a square shape is caused by the reflection from objective of the IR camera.

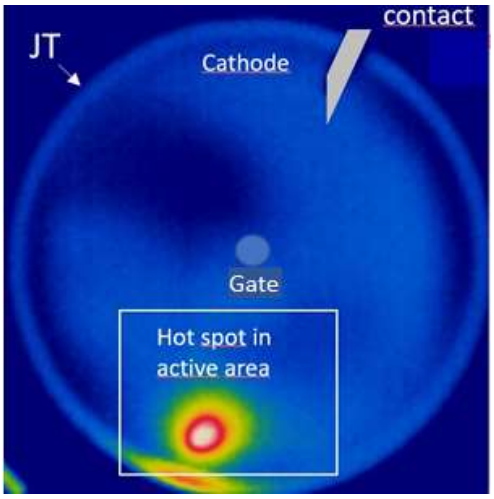

Figure 2b. Infrared image of a thyristor for HVDC showing hot spot in the bulk below the rating voltage due to an inapropriate starting silicon.

Though the wafers qualified for a volume production are guaranteed to have lifetime over 300 μs with minimal inhomogeneity contrary to the Figure1, the radial resistivity variation can still amount up to 8%, the resistivity of delivered wafers lies in the band of about ±6%, and thickness within ±10 μm. On top of it come the variations added during the long diffusions and that of the JT. Therefore, every device produced for the High-Voltage Direct Current (HVDC) is exposed up to the maximal blocking voltage and simultaneous checking by infrared camera – see **Figure 2**. This way one can check, if there are no hot spots in the active region outside the JT up to the maximal forward and reverse blocking voltage. In opposite case, we would be either facing a contamination issue or use other than FZ NTD silicon or select wrong resistivity and thickness of starting silicon wafer – see **Figure 2b**. The optimal devices show uniform infrared pattern along at least a big portion of the JT or optimally at full radial length as shown in the **Figure 2a** (right). The hot spot at the JT at the left figure would be acceptable, if it appeared well above the maximal rating blocking voltage.

3. Contamination Screening of Bipolar Devices

The high-power bipolar devices for GW power transmission are processed from silicon with resistivity ranging between 250 and 1500 Ohm.cm and are therefore sensitive to contamination, typically caused by fast diffusing metals. The contamination manifests itself by moving the electrical parameters outside the technical specification, what can be discovered only after the wafers left the production line. It is therefore important to create a baseline contamination profile of devices within the specification, which then serves as a reference for situations when contamination takes place. On top of it, a sophisticated system for backwards tracing of every single wafer and device through all production tools is the prerequisite of successful identification of reasons for contamination. It can be for example a sudden leak of a diffusion oven, contamination of wafer boats and tubes, failure of temperature sensor, corrosion of sensors or heat shields, temporarily overloaded exhausts, temporarily lower quality of gases, deionised (DI) water, doping chemicals, etc.

The baseline contamination profile of silicon devices can be achieved by combining the classical defect engineering characterization tools like open circuit voltage decay (OCVD) for immediate checking of reduced carrier lifetime, Capacitance-Voltage (C-V) and Deep Level Transient Spectroscopy (DLTS) tools for identification of point defects responsible for contamination[5, 6, 7]. Eventually, spreading resistance profiling (SRP) tool can be used to disclose a doping compensation, inappropriate diffusion temperature, etc.

The fact that the OCVD, C-V and DLTS require a p-n or Schottky junction complicates the screening of thyristor production. **Figure 3** shows the solution for the cases when final silicon wafer does not occupy the whole wafer and allows for having a dedicated test structures at wafer periphery to be laser cut after production. The test structures are optimized in area to accommodate the measuring range of capacitance bridge of the available DLTS tool as well as the size of its cold finger. They must also show a minimal leakage current not to influence the defect identification. For this reason, a special care must be devoted to junction termination after the

laser cut. On the other hand, the screening of BiMOS chips with area about 1 cm^2 including the JT does not require any extra effort.

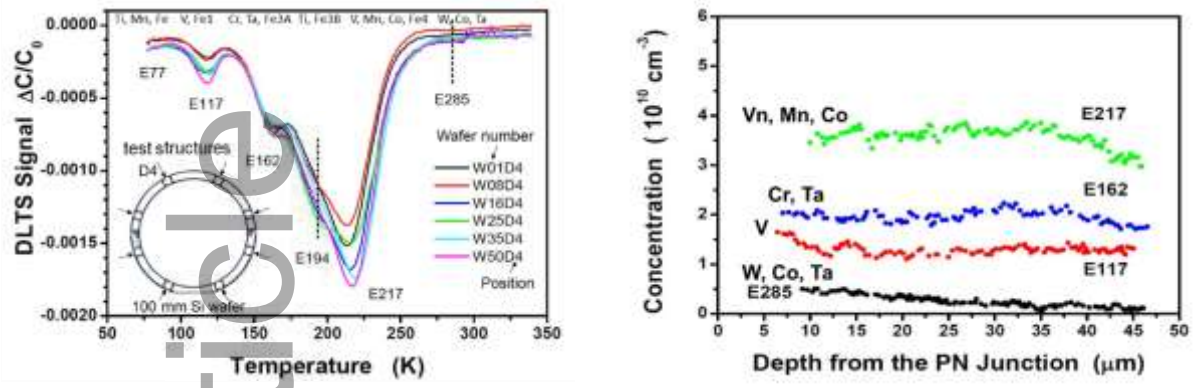

Figure 3. Majority carrier DLTS spectra from 100 mm thyristor wafers, rate window 260 s^{-1} (left). The inset shows the placement of diode test structures relative to wafer flat. Tentative contaminants are assigned to individual DLTS peaks. Profiles of deep levels from the same diodes and tentative contaminants are shown on the right. *By courtesy of P. Hazdra.*

Figure 3 shows the DLTS spectra and deep level profiles of perfectly working thyristor with nominal blocking voltage of 5.2 kV (baseline case). The concentration level of contaminants is at the level of intrinsic concentration and about three orders of magnitude below the phosphorus concentration of starting wafer. There is no detectable impact on device characteristics. This is the result of using high quality starting silicon with a proper surface treatment and several gettering steps implemented within the high-temperature processes at T > 1100 °C.

To understand, where could the small amounts of contaminants come from, the purity of chemicals is subject to regular screening. For example, the lowest concentration of a defect detected as the electron level E77 in Figure 3 (left) is tentatively assigned to Titanium or Manganese or Iron. **Table 1** shows the concentration of Titanium measured in the DI water across the fab by the Inductively Coupled Plasma Mass Spectrometer ICP – MS 7500 cs from Agilent. The concentration measured at the source of the deionized water (DI) water at 0.1 ppt, which corresponds to the concentration of 5.10^9 cm^{-3} in silicon, is at the level measured by the DLTS.

Apparently, a negligible contamination is added on the line from DI water production to the clean room as long as there is no contact with metals like stainless steel prior to high-temperature operations. This suggest the data for the Spin Rinse Dryer (SRD) tool with metallic parts, where severalfold increase of the Titanium concentration was detected at the outlet DI water.

Location	Titanium Content (ng/l = ppt)
DI water source	0.10
Bench rinser prior to diffusion	0.15
SRD tool (probe from the drain port)	0.36

Table 1: Concentration of Titanium in DI water measured by ICP – MS. *By Courtesy of ATU GmbH, Germany.*

Long-term experience with screening the contamination in both Bipolar and BiMOS fabs shows that the best characterization methods are the ones directly reflecting the electronic properties of analysed semiconductor structures like OCVD, C-V and DLTS. This is because their output gives us directly the content and parameters of electrically active contaminants (deep energetic levels), which can be entered directly to a device simulator of Technology Computer-Aided Design (TCAD) platform. This allows us to understand their impact on device operation by direct comparison with tested electrical parameters summarized in product specification. All this is on the contrary to the methods giving a chemical composition like SIMS, ICP-MS, etc., which are suitable rather for analysis of materials and chemicals, because we do not know, how big portion of the detected contaminants is electrically active. Another important factor in fighting the contamination is the overall knowledge of possible contaminant species. On top of the metals, the interpretation of analytical results requires also the knowledge of the effect of other groups of elements, like for example mono-chalcogenides[8, 9]. Contrary to the metals, their impact on power

devices is mild. However, it can be sufficient to move device parameters out of specification. If the analysis would target only the notorious contaminants, one could fail in identification of some peculiar cases.

4. Lifetime Control in Bipolar Devices

Thanks to the research in defect engineering since 1970s, the control of carrier lifetime in power devices became a standard practice. The original techniques of metal diffusion like gold or platinum within the front-end production were replaced by implantation techniques after the front-end processes. The implanted elements are hydrogen, helium and in certain devices also platinum and boron. Of utmost importance is the electron irradiation to reduce the excess carrier concentration in the bulk, when it is beyond the reach of emitter engineering at sub-surface doping. A rigorous way of entering the concentration profiles of radiation defects from process to device simulation (TCAD) made computer-aided design of irradiated devices available since 1994[10]. Despite all the existing knowledge tried-out on all possible devices, one can still find novel concepts. As shown below, it may require an advanced combination of defect engineering and device physics know-how.

In 1976, Bartko and Sun filed their patent on reducing the switching time of thyristors by protons and alpha particles [11]. Being aware of increasing leakage current with increasing irradiation dose for the ion range placed into the lower-doped part of a reverse biased p-n junction, they claimed "the placement of the depth of maximum defect generation in the higher impurity concentration region adjoining blocking PN junction." Indeed, the leakage current of reverse biased devices with ion range in the low-doped N-base of the PNP internal transistor section grows immediately from zero voltage compared to the unirradiated ones as shown in **Figure 4** at the right (labe1 "1."). However, if we place the proton defect peaks symmetrically into both the anode and blocking junctions[12], more precisely to the beginning and the end of the low-doped N-base, the

growth rate of the leakage current with increasing voltage slows down - see the labe1 “2.” on **Figure 4** right. The reason is the reduced diffusion length of holes injected into the N-base of the PNP transistor section at the cathode side by increased recombination rate at deep levels from the proton irradiation [13]. Under forward blocking, the two defect peaks hit the regions with the highest impact on reducing the amplification factor of the leakage current of both internal PNP and NPN transistors. The unique feature of this concept is that the leakage current can be made equally low under both the reverse and forward blocking. This represents a paradigm from generally much higher forward leakage currents to equally high forward and reverse leakage currents in thyristors [14]. On top of it, the commutation turn-off time t_q can be lowered down to 50%, so that the original claim by Bartko and Sun is also fulfilled [15]. Hereby we obtain a new generation of thyristors with increased maximal junction temperature, faster turn-off and better reliability.

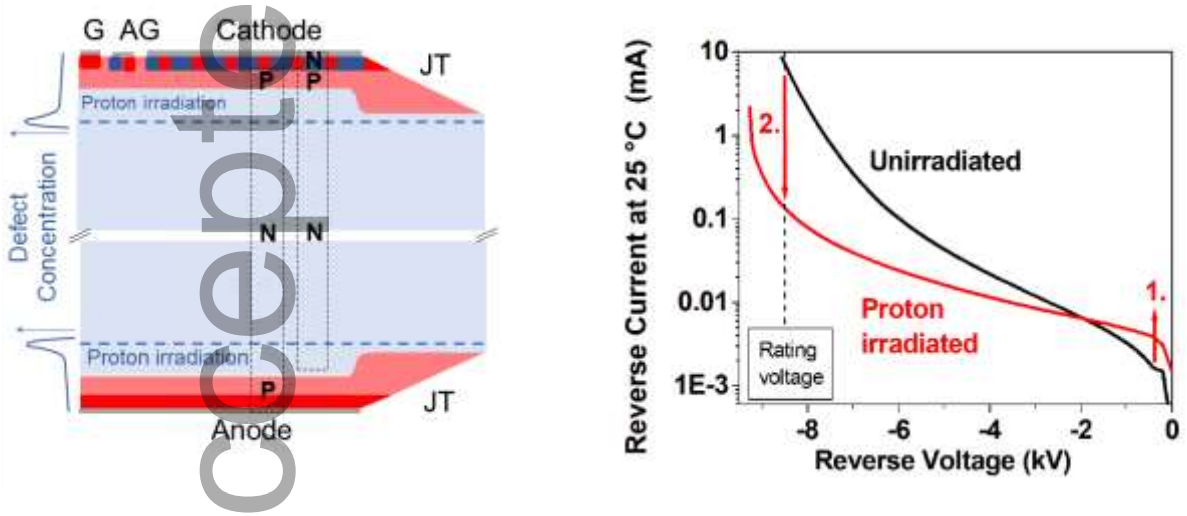

Figure 4. Thyristor with symmetric proton irradiation through anode and cathode with ion range in the low-doped N-base (left). Reverse blocking I-V curves before and after proton irradiation (right).

The above described concept can be exploited further**. Figure 5** (left) shows the classical concept of Bidirectional Control Thyristor (BCT), where two antiparallel connected thyristors are

integrated in one silicon wafer. To provide the commutation turn-off capability, they must be spatially separated to avoid a cross-talk. As a result, each device occupies only half of the wafer with all negative consequences on parameters like a lower surge current I_{TSM}, higher thermal resistance R_{th}, and lower cycling capability (reliability).

Figure 5 (right) shows the new thyristor concept called Bidirectional Phase Control Thyristor (BiPCT). Here the anode and cathode regions of the two antiparallel thyristors are interdigitated in a way that each thyristor occupies the whole wafer area. The surface P-type regions share the function of cathode short on one side and anode region at the opposite side. The key enabler of commutation turn-off capability is the double-side proton irradiation in the N-base region close to the two p-n junctions, which ensures the fast removal of excess carriers during turn-off [16]. Without proton irradiation with localized impact on excess carrier concentration, the device would never turn off. Thanks to the proton irradiation, the device shows very low commutation turn-off time $t_q < 100$ µs. The new device improves all parameters, which can benefit from doubling the device area except for the ON-state voltage drop. Hereby we obtain a new thyristor concept which corresponds to the continuous trend of increasing power density in power electronics.

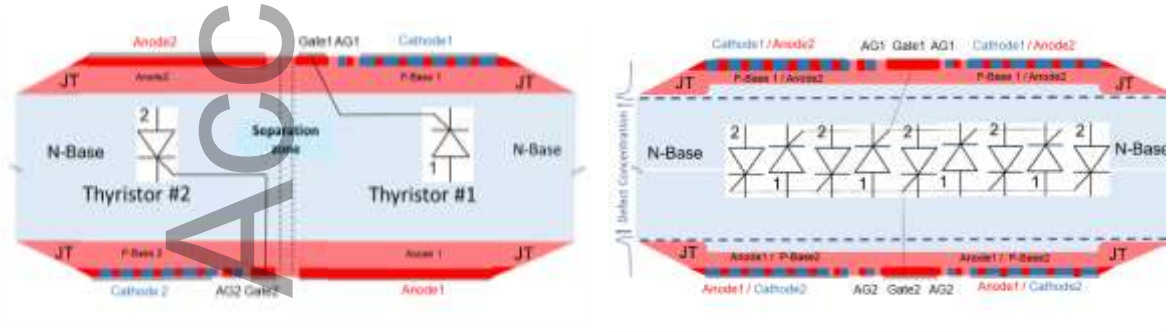

Figure 5. Classical Bidirectional Phase Control (BCT) requires separation of two anti-parallel thyristors to provide turn-off capability (left). Bidirectional Phase Control Thyristor (BiPCT) can turn-off by voltage commutation thanks to the symmetric proton irradiation and utilise the whole wafer for both antiparallel thyristors (right).

5. Defect Engineering in BiMOS Devices

Fast recovery diode, IGBT and reverse conducting IGBT belong to the BiMOS mainstream in silicon. The principles of lifetime control using the electron and ion irradiation, originally developed for discrete bipolar devices, apply also to the BiMOS chips. Relevant practical differences lie in a way how to shield the planar junction termination from ion irradiation otherwise leading to an increased leakage current [16]. Significant difference can be also found in the temperature of the post-irradiation annealing. As the chips, previously irradiated at wafer level, are bonded to a substrate at temperatures around 350 °C, the post-irradiation annealing takes place also at this temperature. Consequently, there is a considerable difference in the irradiation doses and the spectrum of radiation defects between the chips annealed at 350 °C and discrete devices typically annealed below 300°C [18].

One of the most interesting defect engineering topic in the BiMOS field is the low-temperature processing of hydrogen N-type buffer regions for stopping the electric field in IGBTs. The knowledge about hydrogen shallow donors dates back to 1970s[19]. Both the positive and negative effects of modified N-base doping of power diodes and thyristors after proton implantation have been reported in 1985 [20]. The later industrial utilization of the hydrogen donors reflected in patents on IGBTs filed shortly after the year 2000 [21]. That time the low-voltage (LV) IGBT moved from thick wafer “non-punch through” to thin wafer “soft-punch through” concept. Hereby the final wafer thickness of the LV IGBTs went below 250 μm for 1700 V class and below 150 μm for 1200 V class. The attractiveness of the hydrogen donors consisted in the fact that one could substitute the classical phosphorus diffusion above 1000 °C, which was technically complicated at thin wafers with already finished MOS part, by proton implantation followed by low temperature activation below 500 °C. This way the 1200 V IGBT with 100 μm thickness representing the ultimate limit for this voltage class was achieved in 2008 [22]. The reduction of thickness was enabled by replacing the phosphorus buffer diffused at high temperatures at thick

starting wafer by about five times thinner "hydrogen buffer" produced at low-temperature on the wafer with finished MOS part, which was grinded down to the final thickness as shown in **Figure 6**.

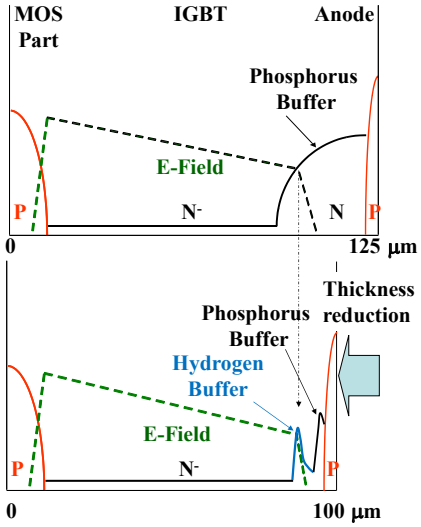

Figure 6. Doping profile of 1200 V IGBT with classical phosphorus buffer from pre-diffused wafer (top). The Controlled Punch-Through (CPT) IGBT with combined hydrogen and phosphorus buffer with five times reduced thickness. The hydrogen buffer stops the electric field, the implanted phosphorus buffer reduces (controls) the amplification of leakage current during blocking (bottom) [22].

Nowadays, one can find industrial IGBTs utilizing the multi-energy proton implanted hydrogen buffer produced at 150 and 200 mm FZ-NTD as well as on 300 mm m:CZ wafers [23, 24]. The proton implanatation is composed of three different energies between 0.5 and ≈1.1 MeV with three different doses ranging between 1.10^{12} and 1.10^{14} cm^{-2}. The motivation for more proton energies is the flexibility to adjust a wider field stop profile with softer turn-off without voltage overshoots and oscillations [23, 24].

The state-of-the-art industrial 1200 V silicon IGBTs are qualified up to the maximal junction temperature T_{jmax} = 175 °C. The technology and design of the field-stop buffer plays a dominant role in achieving this limit. The buffer constitutes the key N-type part of the emitter-base P-N

junction of the internal P-N-P transistor, which determines the amplification of leakage current by transistor effect. On one hand, a higher N-type doping concentration can reduce the amplification of leakage current and support high T_{jmax}. On the other hand, an increased concentration of deep levels in the buffer can increase the generation of leakage current and prevent us from achieving a higher T_{jmax}. A possibility to reach T_{jmax} = 200 °C with 1200 V IGBTs has been analyzed in the previous study, by comparing the capability of different buffer designs to pass important static and dynamic electrical tests at 200 °C [25].

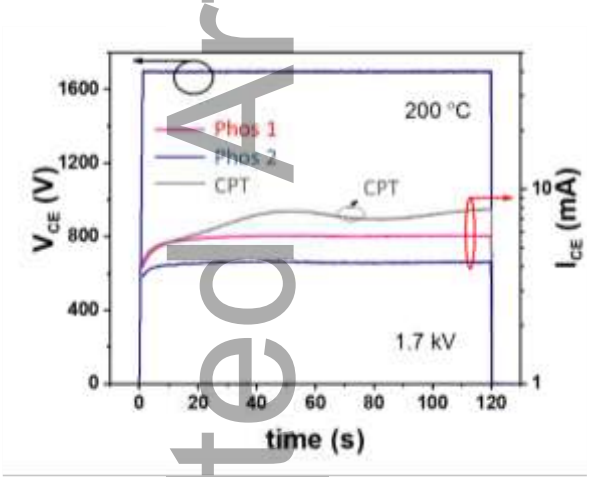

Figure 7a. DC blocking stability test of 1.7 kV thin wafer IGBT chip with area of 1 cm^2 at 200 °C. Thin phosporus buffers Phos 1 and Phos 2 are stable. Leakage current I_{CE} of thin CPT buffer does stabilize in time [25].

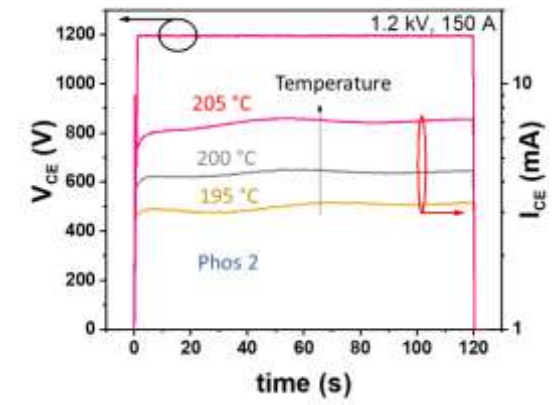

Figure 7b: DC blocking stability of thin phosporus buffer Phos 2 of 1.2 kV IGBT 150 A 1 cm^2 chip around 200 °C [25].

It has been found that only the devices with leakage current below 10 mA at 200 °C pass the standard single shot turn-off and 10 µs short circuit tests at 200 °C. These tests have been passed by all buffer types using the classical phosphorus diffusion at starting thick wafer or after wafer thinning with activation by laser annealing. From hydrogen buffers only the thinner ones, like the CPT from **Figure 7** or multi-energy one with reduced thickness, have passed. In the blocking

stability test at 200 °C, when 1200 or 1700 V is applied for several minutes as shown in **Figure 7a**, even the CPT buffer with reduced thickness shows a thermal instability contrary to the Phosphorus buffers produced by (1) implant & laser anneal or (2) epitaxy growth. This means that thin phosphorus buffers activated at high temperatures have chance to operate at T_{jmax} = 200 °C, while the hydrogen buffers activated below 500 °C can satisfy the usually required safety margin of 10 – 15 °C over the specified T_{jmax} = 175 °C.

The reasons for a lower thermal capability of devices with hydrogen buffers were studied by DLTS and C-V characterization of special diode test structure shown in **Figure 8** [25]. One micrometer thick boron anode activated at high temperatures emulated the anode of IGBT with minimal defect content. Junction termination was substituted by the anode metal contact with edges far away fom the chip edge and passivated by silicon dioxide. The hydrogen buffer emulating that of the CPT IGBT resulted from 700 keV proton implantation with dose 5.10^{13} and 1.10^{14} cm^{-2} annealed at several temperatures between 300 and 500 °C. Only the cases with the lowest concentration of deep levels and still close to the processing conditions of the hydrogen buffer are shown in **Figure 8** and **Figure 9** to illustrate the remaining defect content after processing.

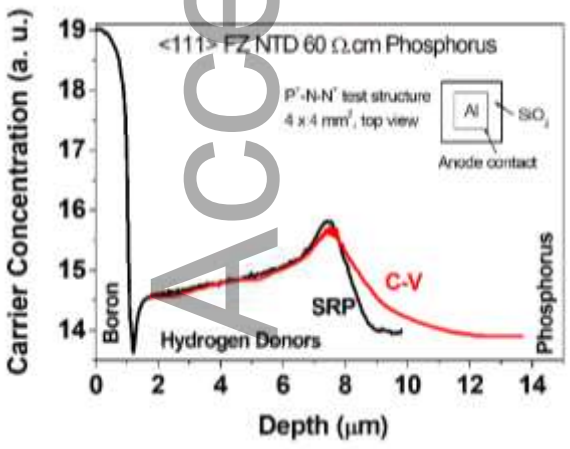

Figure 8. Spreading resistance (SRP) and C-V profiles after 700 keV proton implantation

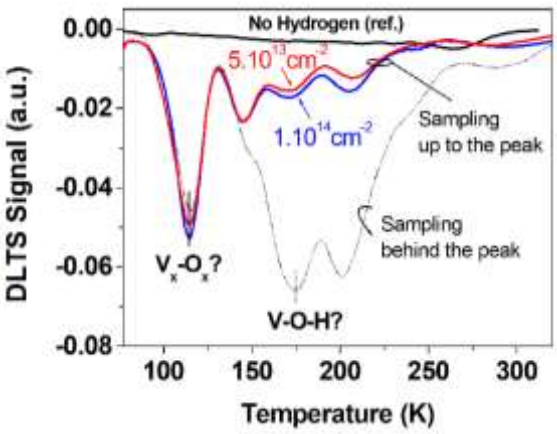

Figure 9. Majority carrier DLTS spectra of device from Figure 8 before (ref.) and after

and annealing at 500 °C of diode test structure with dimensions according to the inset.

700 keV proton implantation to two doses and annealing at 500 °C [26]. Sampling depth up to and behind is shown for the implantation dose of 5.10^{13} cm^{-2}.

Figure 9 suggests that the deep level at E_C – 0.21 eV could be a higher-order V_x-O_x complex with an apparent capture cross section of 1.10^{-14} cm^{-2} as is typical for annealing after high dose implantation above 400 °C. The DLTS sampling behind the proton range with increased concentration of hydrogen atoms revealed the enhancement of the peak at T = 175 K (dashed line). It is likely the V-O-H centre resulting from hydrogenation of vacancy-oxygen pairs. As those deep energy levels in the silicon bandgap are located in the region first reached by the space charge region of the blocking junction (P-well – N-drift) of IGBT, it can explain the enhanced leakage current of IGBTs with hydrogen buffer.

The annealing behavior of the recorded deep levels and its impact on the recombination properties of the diode test structures is further illustrated by measured ON-state voltage drop V_F in **Figure 10**. The measurements are performed at chip with reduced contact area, what implies a limited precision of V_F tested at current of 30 A at about 10 %. Beside this and usual scatter between samples, the annealing of the not implanted reference sample at 400 °C and above can be influenced by the activation of oxygen thermal donors (dashed line). The implanted chips show the typical annealing of radiation defects above 350 °C. At this temperature, the concentration of hydrogen donors in the depth between 7 and 8 μm in Figure 8 reaches its maximum in the range of 5.10^{15} to 1.10^{16} cm^{-3} for the dose 1.10^{14} cm^{-2}. Considering the measurement scatter, we can say that the V_F recovers to its original value after annealing at 400 °C and above for the lower proton implantation dose, and at 450 °C and above for the higher one. The deep level dominating the high-level carrier lifetime in the N-type Silicon and hereby the V_F is the V_x-O_x in Figure 9, which is

positioned closer to the conduction band. The proximity to the conduction band is in favour of re-emission of captured electrons back to the conduction band (trapping) with positive effect on low V_F.

The recombination dynamics vs. annealing temperature is more complex as show the OCVD waveforms in **Figure 11**. Since the concentration of deep levels in the reference not implanted sample is low, the recombination rate of free carriers is also low and the corresponding open circuit voltage decay is slow at both high and low level injection. The high-level injection corresponds to the region of higher OCVD voltage at the beginning of the waveform. The low-level one corresponds to the voltages below ≈0.4 V towards the tail, which is for the reference sample outside the graph. After annealing, the irradiated region around the anode p-n junction recovers from the radiation defects and the sharp voltage decay of the not annealed sample changes with increasing annealing temperature to a slower one up to 400 °C. While the voltage decay in the region of high-level injection, responsible for the decreased V_F, gets closer to the reference sample, the voltage decay corresponding to the low-level injection stays steep and becomes even steeper above 400°C. This observation agrees with the appearance of the energetically deeper deep levels in **Figure 9** tentatively assigned to the V-O-H centre with relatively high capture cross section of 1.10^{-14} cm^{-2}. The deeper lying deep levels may increase the leakage current when approached by the space charge region of a reverse blocking junction.

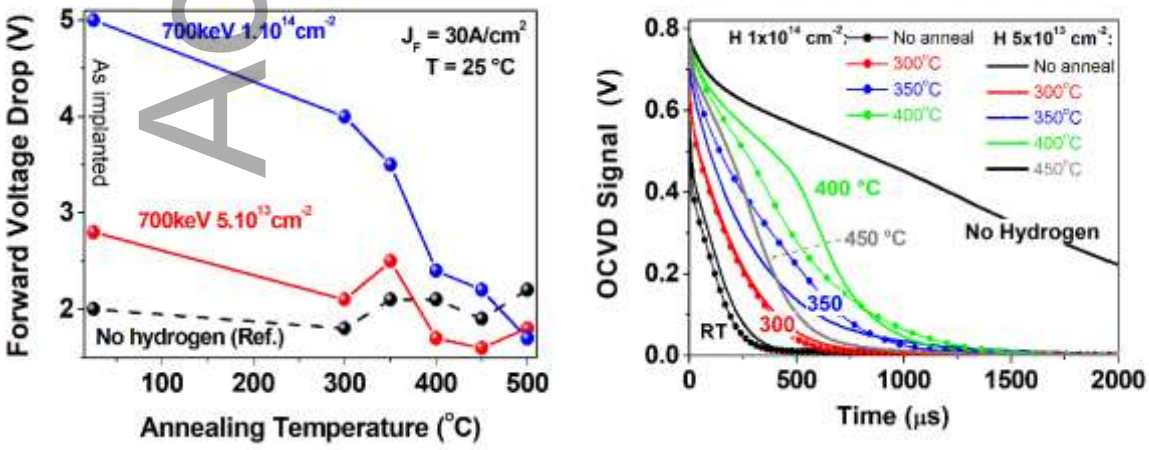

Figure 10. Forward voltage drop of the test structures from Figure.9 for different annealing temperatures and proton implantation doses.

Figure 11. OCVD waveforms of the test structures from Figure.10 for different annealing temperatures and proton implantation doses. No anneal = RT.

The evolution of buffers for IGBT has showed that the sophisticated techniques of defect engineering at low processing temperature can facilitate the production of new generations with improved electrical ratings and reduced production cost. To achieve the ultimate ratings like exceptionally high operation temperatures, one should utilize high-temperature processes and designs leading to the lowest possible residual defect content. It does not inevitably mean to stay with the classical thermal processes. It can be achieved using the latest laser annealing techniques tuned for the minimal defect content.

5. Conclusions

The importance of defect engineering for design and technology of high-power semiconductor devices for industry, traction, and transmission and distribution has been illustrated on several Bipolar and BiMOS examples. In the bipolar sector with the highest power ratings, where devices may occupy the whole 100 mm or 150 mm wafer, the high uniformity of the lateral resistivity and carrier lifetime of float-zone wafers belongs to key enablers of high production yield. This must be supported by sophisticated methodology for screening from the contamination before and during high-temperature processes including a system of early disclosure, backwards tracing and mitigation. Continuous development of fine-patterned devices with increased functionality and steadily growing power densities benefits from advances in the design and technology for local lifetime control.

The power ratings of BiMOS devices have also shown a steady growth and reached the level, which was in the past possible only with bipolar devices. On one hand, this has been achieved by massive paralleling of chips enabled by progress in packaging technologies. On the chip side, it has been supported by reduced silicon thickness (lower losses) towards the theoretical limit, increased junction temperature, and integration of antiparallel structures on the same chip. In all of them, the defect engineering discussed in this paper played an important role. This will continue also in the future high-power devices serving in the systems up to GW levels, which will benefit from the cost-effective co-existence of silicon Bipolar and BiMOS device concepts.

Acknowledgments

Pavel Hazdra and Volodymyr Komarnitskyy are acknowledged for characterization using OCVD, C-V and DLTS techniques.

References

[1] M. Schnöller, *IEEE Trans. on Electron Devices*. **1974**, 21, 313.

[2] V. V. Voronkov, *Journal of Crystal Growth,* **1982**, 59, 625.

[3] E. Dornberger, W. von Ammon, J. Virbulis, B. Hanna, T. Sinno, *Journal of Crystal Growth,* **2001**, 230, 291.

[4] H. - J. Schulze, B. O. Kolbesen, *Solid-State Electronics.* **1998**, 42, 2187.

[5] S. R. Lederhandler, L. J. Giacoletto, Measurement of minority carrier lifetime and surface effects in junction devices, *Proceedings of the IRE* **1955**, 43, 477.

[6] D.V. Lang, *Journal of Applied Physics,* **1974**, 45, 3023.

[7] D. K: Schroeder, *Semiconductor Material and Device Characterization*, A John Wiley & Sons, Hoboken, New Jersey, **2006**.

[8] H. G. Grimmeiss and E. Janzen, *Chalcogen-Related Defects in Silicon*, in: *Materials, Properties and Preparation,* edited by T. S. Moss and S. Mahajan, *Handbook on Semiconductors,* vol. 3b, Amsterdam: North-Holland , **1994**.

[9] P. Pichler, *Intrinsic Point Defects, Impurities, and Their Diffusion in Silicon,* Springer Verlag Wien GmbH, **2004**

[10] P. Hazdra and J. Vobecky, *Solid-State Electronics*, **1994**, 37, 127.

[11] J. Bartko, K. H. Sun, (Westinghouse Electric Corporation) *US 4,056,408*, **1977**.

[12] H. Mitlehner, F. Pfirsch, H. J. Schulze, *A Novel 8 kV Light-Triggered Thyristor with Overvoltage Self Protection,* presented at ISPSD´1990, Tokyo, May, **1990**, 289.

[13] J. Vobecky, V. Botan, U. Meier, K. Tugan, M. Bellini, presented at ISPSD´2018, Chicago, May, **2018**, 156.

[14] J. Vobecky, *Thyristors*, in *Modern Power Electronic Devices: Physics, Applications, and Reliability*. (Ed: F. Iannuzzo), IET, Stevenage, United Kingdom **2020**, Ch.3.

[15] J. Vobecky, presented at PCIM`2019, Nuremberg, May **2019**, 749.

[16] J. Vobecky, *IEEE Transactions on Electron Devices,* **2020**, 67, 2844.

[17] B. Boksteen, C. Papadopoulos, D. Prindle, A. Kopta, C. Corvasce, presented at ISPSD´2018, Chicago, May, **2018**, 28.

[18] P. Hazdra. V. Komarnitskyy, *Microelectronics Journal*, **2006**, 37, 197.

[19] Y. Zohta, Y. Ohmura, and M. Kanazawa, *Jpn. J. Appl. Phys.*, **1971**, 10, 532.

[20] D. Silber, W. – D. Wondrak, W. Wondrak, B. Thomas, and H. Berg, presented at IEDM`1985, Washington, December **1985**, 162.

[21] R. Francis, C. Ng (International Rectifier Corporation) *US 6,482,681 B1*, **2002**.

[22] J. Vobecky, M. Rahimo, A. Kopta, S. Linder, presented at ISPSD´2008, Orlando, May, **2008**, 76.

[23] F.-J. Niedernostheide, H.-J. Schulze, H. P. Felsl, F. Hille, J. G. Laven, M. Pfaffenlehner, C. Schäffer, H. Schulze, W. Schustereder, presented at ISPSD´2016, Prague, May, **2016**, 351.

[24] H.-J. Schulze, H. Öfner, F.-J. Niedernostheide, F. Lükermann, A. Schulz, *Physica Status Solidi A*, **2019**, 216, 1900235.

[25] E. Buitrago, A. Mesemanolis, M. Andenna, C. Papadopoulos, C. Corvasce, J. Vobecky, M. Rahimo, presented at ISPSD´2019, Shanghai, **2019**, 47.

[26] J. Vobecky, C. Corvasce, E. Buitrago, M. Andenna, B. Boksteen, G. Paques, presented at SSDM´2019, Nagoya, **2019**, 451.

Processing of electrical power at megawatt to gigawatt level in the industry, traction, and transmission and distribution requires high-power devices with blocking capability up to 10 kV. The mainstream ones require high purity silicon wafers with the lowest possible defect content (contamination) and maximal homogeneity of resistivity and thickness. To satisfy current ratings in typical range 1 - 6 kA, single diode or thyristor may occupy nearly the whole 100 to 150 mm silicon wafer. Beside the doping profile optimization and gettering in the front-end processes, the devices are subject to defect engineering to adjust uniformly or locally the recombination lifetime of carriers. In IGBTs, it is also about dopant activation below 500 °C. Satisfaction of all extremal demands laid on those devices would not be possible without the knowledge developed by defect engineering community in the past decades. Some relevant industrial examples of screening the contamination in typical production of silicon high-power devices are demonstrated as well as the advanced defect engineering methods for increasing device functionality and power density.