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The roles of carrier concentration and interface, bulk, and grain-boundary recombination for 25% efficient CdTe solar cells

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CdTe devices have reached efficiencies of 22% due to continuing improvements in bulk material properties, including minority carrier lifetime. Device modeling has helped to guide these device improvements by quantifying the impacts of material properties and different device designs on device performance. One of the barriers to truly predictive device modeling is the interdependence of these material properties. For example, interfaces become more critical as bulk properties, particularly, hole density and carrier lifetime, increase. We present device-modeling analyses that describe the effects of recombination at the interfaces and grain boundaries as lifetime and doping of the CdTe layer change. The doping and lifetime should be priorities for maximizing open-circuit voltage (V_{oc}) and efficiency improvements. However, interface and grain boundary recombination become bottlenecks for device performance at increased lifetime and doping levels. This work quantifies and discusses these emerging challenges for next-generation CdTe device efficiency. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4984320]

I. INTRODUCTION

The maximum open-circuit voltage (V_{oc}) for a solar cell structure is determined by the bandgap. However, V_{oc} in most thin-film solar cell technologies does not approach this theoretical limit due to recombination and/or low doping. For the past two decades, the hole density in typical polycrystalline (px) CdTe has been in the low $10^{14}\,cm^{-3}$ range, and carrier lifetimes have been on the order of nanoseconds. Multiple modeling studies predict V_{oc} and efficiency enhancements with increased doping and lifetime.[1–3] However, with the exception of recent analysis on homojunction epitaxial CdTe devices,[3] most published modeling studies have limited the parameter space to values considered practical at the time (e.g., lifetime < 10 ns) and have not detailed the paths to $>25\%$ efficiency. Recent efforts on both single-crystal and polycrystalline CdTe report significant increases in carrier density[4] and lifetime[5,6] beyond the values considered practical in most earlier models. As these limitations on carrier lifetime and doping are overcome, other bottlenecks, such as grain boundary (GB) and interface recombination, become more important. Recent studies have indicated that CdTe interface and grain boundary (GB) recombination are often on the order of 10^5 cm/s,[7–12] but most previously published models do not include surface and interface recombination due to the expected dominance of bulk recombination. In this work, we present numerical simulations to quantify the roles of hole density, lifetime, interface recombination, grain size, and grain-boundary recombination in achieving $>25\%$ efficiency. The results indicate that next-generation CdTe solar efficiency requires simultaneously improving bulk, interface, and grain-boundary properties.

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II. MODEL

The simulations are performed using Sentaurus Device software[13] to solve the Poisson and electron and hole continuity equations. The model device consists of three semiconductor layers: SnO_2, CdS, and CdTe [Fig. 1(a)]. The principal properties of each layer are listed in Table I. In Sec. III A, the bulk absorber properties are uniform, representing either a single crystal or averaged values over multiple grains and grain boundaries in a polycrystalline material. In Sec. III B, the model includes the impact of grain interiors and grain boundaries to quantify the importance of grain size and grain boundary passivation. The model inserts the electron and hole lifetimes into the Shockley-Read-Hall (SRH) recombination equation. At the interface, electron, and hole interface recombination velocities are inserted into the SRH equation.[13] Figure 1(b) shows the calculated equilibrium band diagrams for an absorber carrier density of $p = 2 \times 10^{14}\,cm^{-3}$ (red) and $p = 2 \times 10^{16}\,cm^{-3}$ (blue). In addition to the change in built-in potential and the space-charge region (SCR) width, the hole density alters the junction band bending, the absorber inversion, the carrier distribution throughout, and consequently the impact of interface recombination, which will be discussed later in more detail.

In high-injection conditions, excess carrier densities are similar or greater than those of the equilibrium carriers, and the effective SRH recombination lifetime is given by the sum of $\tau_e + \tau_h$, rather than just the minority carrier lifetime.[22] This is typically operative in the depletion region for CdTe solar cells. Lifetime measurements on CdTe solar cells are generally measured through the glass into the depletion region with high-injection conditions and in these circumstances measure $\tau_e + \tau_h$.[22] Some models have chosen a large τ_h (e.g., $\sim 1\,\mu s$) relative to τ_e. In practice, this will produce much longer PL decay times (e.g., up to 1 μs) than have been observed experimentally,[23] leading to overly large estimates of the V_{oc} for a given lifetime. This also leads to

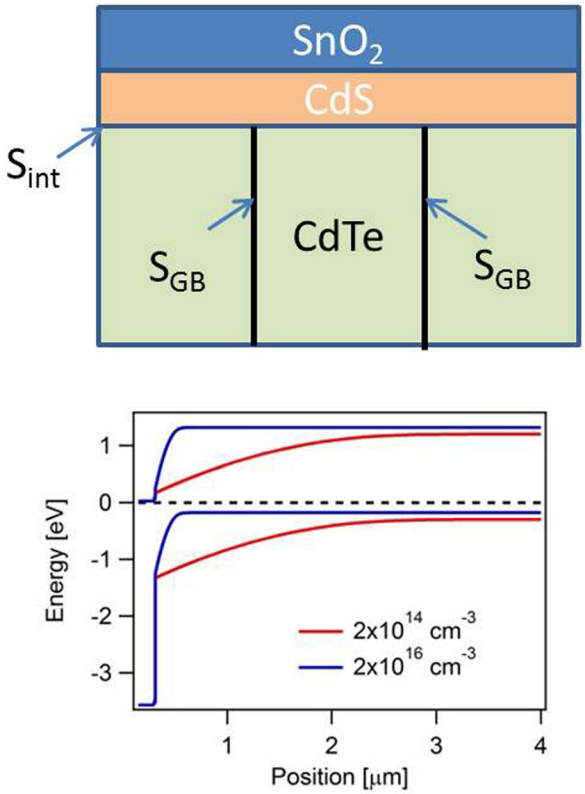

FIG. 1. (a) A schematic of CdTe solar cell used in the model. (b) Simulated equilbrium band diagrams for two different carrier densities [$p = 2 \times 10^{14}\,cm^{-3}$ (red) and $p = 2 \times 10^{16}\,cm^{-3}$ (blue)].

overestimating the influence of back contact properties, such as band offsets, barriers, and surface recombination, on device performance. The CdTe electron and hole lifetime values chosen here accurately replicate experimental TRPL curves and their correlation to V_{oc}, as well as CV and QE data simultaneously.[24] A 1-d SCAPS version of this model is able to predict experimental V_{oc} values as a function of lifetime and hole density for a wide range of hole densities and lifetimes ranging from standard V_{oc} values to above 1 V,[25] which overlaps with the material properties considered here.

Unless stated otherwise, the conduction-band offset at the CdS/CdTe interface is set at -0.1 eV,[26] and the conduction-band minima of CdS and SnO_2 are aligned. The back surface recombination velocity is set to 10^5 cm/s.[8] Alloying within the absorber or buffer layer is not modeled here. In practice, junction formation and carrier recombination in the vicinity of the junction may be altered by diffusion of sulphur or other elements in different window layers. The impact of graded junctions with ternary/quaternary compounds will be a topic of future analysis. To account for high current densities observed in today's highly efficient devices, which either have ternary/quaternary compounds or in which CdS is partially or completely consumed, a very thin CdS layer ($d = 10$ nm) is modeled.

We performed parameter sensitivity analysis to determine the influence of the evolving CdTe material properties reported in the literature on device performance. The impact of some parameters is minimal. For example, reported values for the CdTe dielectric constant are between 9.4 and 10.6 but affect the efficiency by less than 0.1% absolute. While absorber grading is already being performed experimentally, it was outside the scope of the model. A parameter sensitivity analysis at the back contact within reasonable experimental values found that it is not strongly limiting until the bulk lifetime, the hole density, and the front interface recombination are significantly improved as addressed in this paper. Reported electron mobility measurements range between $1000\,cm^2/V.s$ for single crystal CdTe[27,28] to less than $100\,cm^2/V.s$ for px CdTe.[29,30] Hall measurements of px CdTe can report hole mobilities of $<1\,cm^2/V.s$ because the distance between lateral contacts may include transport across hundreds to thousands of grain boundaries. Experimentally, the films used in devices are just a few microns thick and often have a columnar grain structure; this results in a much higher effective mobility in the transverse direction. In practice, the bulk hole mobility of $\sim 1\,cm^2/V.s$ would impede the carrier collection, and result in short-circuit current density (J_{sc}) and fill-factor (FF) losses that are generally not experimentally observed. We have chosen a value of $\mu_e = 320\,cm^2/V.s$, based on the measured mobility values in Ref. 31, and previous modeling analysis.[32] As an example, for minority-carrier lifetime $\tau = 10$ ns, and doping $p = 2 \times 10^{14}\,cm^{-3}$, variation of minority-carrier mobility from $1000\,cm^2/V.s$ to $80\,cm^2/V.s$ decreases the efficiency by 0.9% absolute. Based on these analyses, we focused on the effects of varying lifetime, hole density, interface recombination, grain size, and grain-boundary recombination.

III. RESULTS

A. Carrier density, lifetime, and interface recombination

First, we explore the impact of carrier density and carrier lifetime on device performance. Contour plots assuming a very low recombination rate at the CdTe/CdS interface are

TABLE I. Critical parameters used in the CdTe device model.

	CdTe	CdS	SnO_2
Thickness (nm)	4000	10	300
Band gap (eV)	1.5 (Refs. 14 and 15)	2.4	3.596 (Ref. 16)
Carrier density (cm^{-3})	p: 10^{14}–10^{17} (varied)	n: 1.1×10^{18}	n: 10^{18}
Relative dielectric constant	10.2 (Refs. 17 and 18)	8.4 (Ref. 16)	12.2 (Ref. 16)
Effective mass e/h	0.096 (Refs. 19 and 20)/0.35 (Ref. 19)	0.25/0.7 (Ref. 16)	0.30 (Ref. 21)/1
Mobility e/h (cm^2/V s)	320/80	160/15 (Ref. 16)	10/2.5
Lifetime e/h (ns)	$\tau_e = \tau_h$ (1 ns–200 ns) (varied)	$0.1/10^{-3}$	$\tau_e = \tau_h = 0.1$

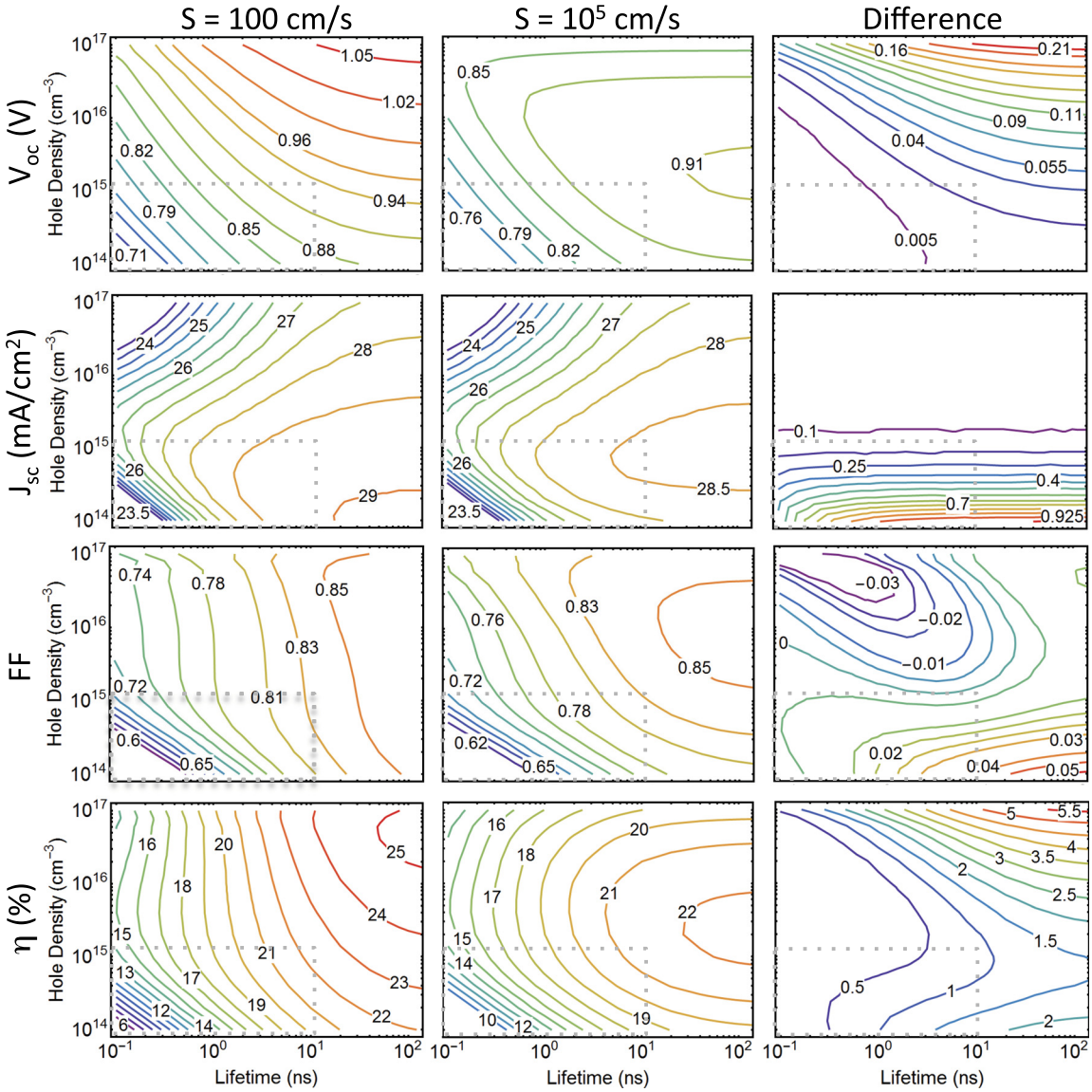

FIG. 2. Calculated impact of hole density and lifetime on cell parameters: V_{oc}, J_{sc}, FF, and efficiency when: (a) $S_{int} = 100$ cm/s, (b) $S_{int} = 10^5$ cm/s. (c) Difference in cell parameters due to interface recombination [e.g., $\Delta V_{oc} \equiv V_{oc}(S_{int} = 100\,\text{cm/s}) - V_{oc}(S_{int} = 10^5\,\text{cm/s})$].

shown in Fig. 2(a). These results expand previous modeling analysis[1,2] to higher lifetimes and carrier densities. The observed trends in V_{oc} are largely consistent with expectations from basic device physics and intuition, i.e., a simultaneous increase in the hole density and lifetime will result in higher V_{oc}. (The surprising decrease in V_{oc} with high doping for high S and lifetime is explained later in the text in conjunction with Fig. 4.) Increased hole density increases the built-in potential, and thus, the V_{oc}, while SRH recombination increases the saturation current density, and thus, logarithmically decreasing V_{oc}. For $\tau > 10$ ns, the steepness of the V_{oc} vs. τ dependence decreases, and the benefit of lifetime on V_{oc} slowly saturates for high lifetimes.[2,23,33,34]

High J_{sc} and FF require good carrier collection. Carrier collection is a balance of collecting carriers by drift through the space charge region, diffusion to the space charge region, and the absorption depth. The SCR contracts with increasing hole density, the diffusion length increases with lifetime, and the optical absorption remains constant. In an ideal solar cell, it is assumed that the collection probability within the space-charge region (SCR) is equal to 1, i.e., all the carriers generated within this region are collected, due to a narrow SCR and relatively long diffusion length. In some of the cases analyzed in Fig. 2(a) (hole densities on the order of 10^{14} cm^{-3}, and $\tau < 1$ ns), the SCR is broad, relative to the diffusion length. In this case, ideal space-charge collection assumptions are no longer valid, and some carriers will recombine in the SCR rather than be collected, and the field can assist collection. These tradeoffs explain part of the J_{sc} and FF loss in the lower left part of Fig. 2(a). For low lifetimes ($t < 1$ ns) and high hole densities, the diffusion length is small, and the SCR is narrow. Here, J_{sc} losses can occur due to the incomplete collection in the quasi-neutral region in the absence of field drift. These complex interactions contribute to the observed trends. Combining all of this together indicates that ultimately, to obtain $V_{oc} > 1$ V and $\eta > 24\%$ it is critical to achieving both high lifetime ($\tau > 10$ ns) and doping ($p > 10^{16}$ cm^{-3}).

The above discussion assumes a very low CdTe/CdS interface recombination. In practice, CdTe/window interfaces can have a high recombination velocity $S_{int} > 10^5$ cm/s (Refs. 23, 35, and 36) that presents a serious limitation to device performance. Figure 2(b) illustrates similar contour plots to Fig. 2(a), but assuming $S_{int} = 10^5$ cm/s. Figure 2(c) shows the difference in cell parameter values caused by S_{int}. By comparing the plots, one can notice that the lower left corners of the graphs (highlighted with gray rectangles) look very similar. For devices with carrier lifetimes <2 ns and hole densities on the order of 10^{14} cm^{-3}, the impact of interface recombination on performance is modest, and interface passivation is not required for this level of device performance. Previous modeling studies remain accurate despite neglecting S_{int} because the lifetimes and doping levels in those studies were low. As the minority carrier lifetime and doping improve, the interface recombination starts limiting the performance, and thus, efforts towards its passivation become necessary. In a device with a poorly passivated junction interface, $S_{int} = 10^5$ cm/s, the V_{oc} does not increase above 0.9 V even for bulk lifetimes >100 ns and hole density >10^{16} cm^{-3}; hence, the efficiency does not surpass 22% [Fig. 2(b)].

To further explore the impact of interface recombination in high efficiency CdTe devices and to emphasize the interdependence of parameters, the combined impact of S_{int} and τ are compared for two hole densities: (a) when the hole density has a typical px CdTe value of $p = 2 \times 10^{14}$ cm^{-3} [Fig. 3(a)], and (b) when the hole density is increased to levels required for $V_{oc} > 1$ V, $p = 2 \times 10^{16}$ cm^{-3} [Fig. 3(b)]. Four general regions, divided by $S_{int} = 10^4$ cm/s and $\tau = 10$ ns, can be distinguished in these plots. The region #1 represents many px CdTe devices with high S_{int} and low τ. Region #2 shows the impact of a high bulk lifetime with high interface recombination. Region #3 shows a well-passivated interface with a low lifetime. Region #4 represents high bulk lifetime and low interface recombination.

CdTe carrier lifetimes are typically measured optically, using single photon excitation time-resolved photoluminescence (TRPL). The excitation undergoes Beer-Lambert absorption, such that a near surface component can often be separated from a more "bulk" component. In the case of high surface recombination relative to the bulk, the interface recombination can be approximated as $\tau_S = 1/\alpha.S_{int}$, where α is the optical absorption coefficient.[8,34,37] Thus, as the excitation wavelength is altered the absorption depth can be tuned with the absorption depth ranging from 30 to 450 nm with excitations of 400 to 800 nm. This allows one to have single photon TRPL measurements more or less sensitive to surface recombination. Typical TRPL measurements excite near 650 nm, which corresponds to depths of ~220 nm.[7] We can then use this approximation as a simple parametric measure to compare the recombination rates at the interface and in the bulk. The solid gray line distinguishes where the recombination is dominant: below the gray line, $\tau_S > \tau_b$, and above it, $\tau_S < \tau_b$. Estimates of bulk lifetimes from single photon TRPL range from 10's of ps to 10's of ns. Interface and grain boundary recombination velocity are often on the order of 10^5 cm/s.[5,7–9,23]

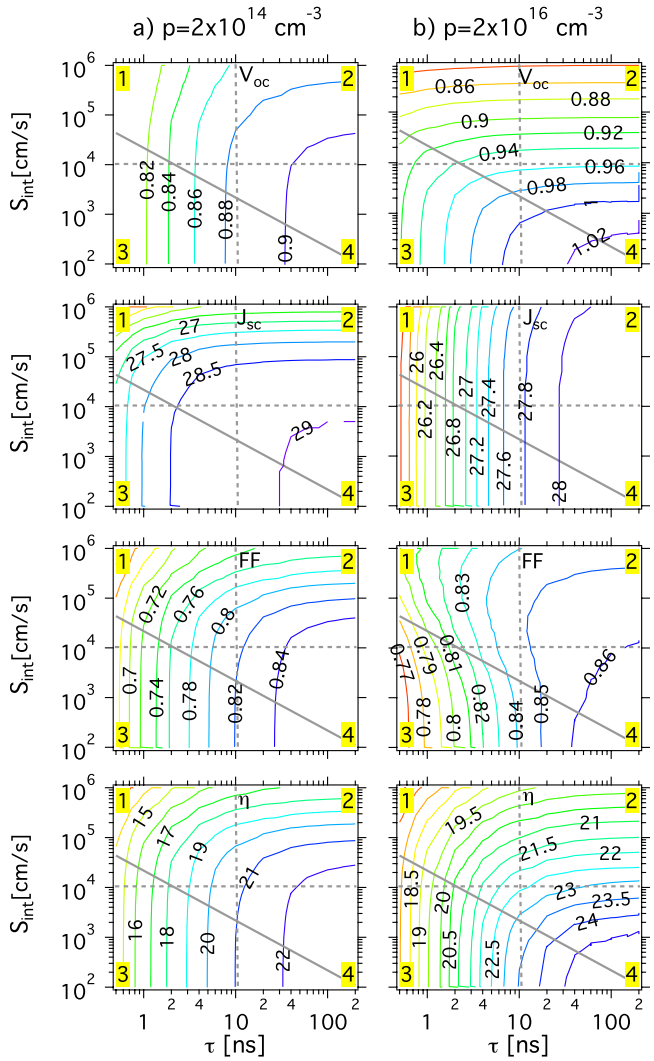

FIG. 3. Contour plots of calculated V_{oc} (V), J_{sc} (mA/cm^2), FF and η (%) as a function of S_{int} and τ for: (a) $p = 2 \times 10^{14}$ cm^{-3} and (b) $p = 2 \times 10^{16}$ cm^{-3}. The four regions are divided by $\tau = 10$ ns and $S_{int} = 10^4$ cm/s. The solid gray line represents a correlation between S_{int} and τ (below the gray line, $\tau_S > \tau_b$, and above the gray line $\tau_S < \tau_b$).

In region #1 (high S_{int} and low τ), for low doping [Fig. 3(a)], the contour lines are close to vertical. V_{oc} depends more strongly on τ_b, and less on S_{int}. Recombination throughout the SCR limits V_{oc}, and although S_{int} is high, it does not affect performance. In the same region for high doping [Fig. 3(b)], the contour curves become horizontal for $S_{int} > 10^5$ cm/s. It means that for $p = 2 \times 10^{16}$ cm^{-3}, $\tau < 10$ ns, and $S_{int} > 10^5$ cm/s, the interface recombination dominates performance, and improving the bulk lifetime without addressing the interface will not be very useful.

The J_{sc} dependence on τ and S_{int} is different from V_{oc}. For low doping [Fig. 3(a)] and high S_{int} (>2×10^4 cm/s), the electric field is weak. Therefore, some of the photogenerated carriers will recombine at the interface and not be collected, so interface recombination impacts J_{sc}. In a highly doped sample, for the same regions 1 and 2, the strong electric field enables carrier collection; S_{int} up to 10^6 cm/s is not enough to compete with the drift, and as a result, the J_{sc} is nearly independent of S_{int}.

In all cases, the J_{sc} is slightly lower for the higher doped sample due to the narrower SCR. In region #1, for $p = 2 \times 10^{16}\,cm^{-3}$, some of the carriers generated outside of the SCR are not collected, resulting in less J_{sc}. The FF behavior follows the V_{oc} and J_{sc} trends.

In region #3, τ_S is often greater than τ_b, so contour lines are generally vertical, indicating that interface recombination does not impact device performance significantly. This is also true for region # 4 below the gray line. As grain boundaries and surfaces are known to lead to increased recombination and typical px-CdTe devices are measured to have $\tau_S \ll \tau_b$, this region has been difficult to reach experimentally. High lifetime and low interface recombination do create the best results, but even if this is accomplished in a poorly doped sample the maximum V_{oc} is 0.9 eV and the efficiency does not exceed 22%.

The V_{oc} is limited by the recombination rate, which is determined by the defect density and the number of carriers available for recombination. For a specific defect density, the maximum recombination rate typically occurs when the densities of electrons and holes are comparable, i.e., when the Fermi level is located at, or near the middle of the band gap.[38] Drift and diffusion around the interface will affect the electron and hole concentrations and recombination. Consequently, as the region where the electrons approach the hole density shifts toward the interface, the influence of the interface recombination increases. The position where the electron density is equal to the hole density (e = h) as a function of doping at light and 0.8 V bias is shown in Fig. 4(b). Whereas e = h is not particularly critical, but plotting this helps illustrate that the region where electrons and holes are most available to recombine with one another shifts towards the interface with increased doping, thus making the interface recombination rate stronger, and interface passivation more important. As a result, unlike the behavior observed for low S_{int} [red curves in Figs. 4(c) and 4(d)] where the V_{oc} and efficiency increase logarithmically with increased doping, for high interface recombination, the V_{oc} reaches a maximum value, then starts to level off, and eventually decreases with increased doping [Fig. 4(c)]. The

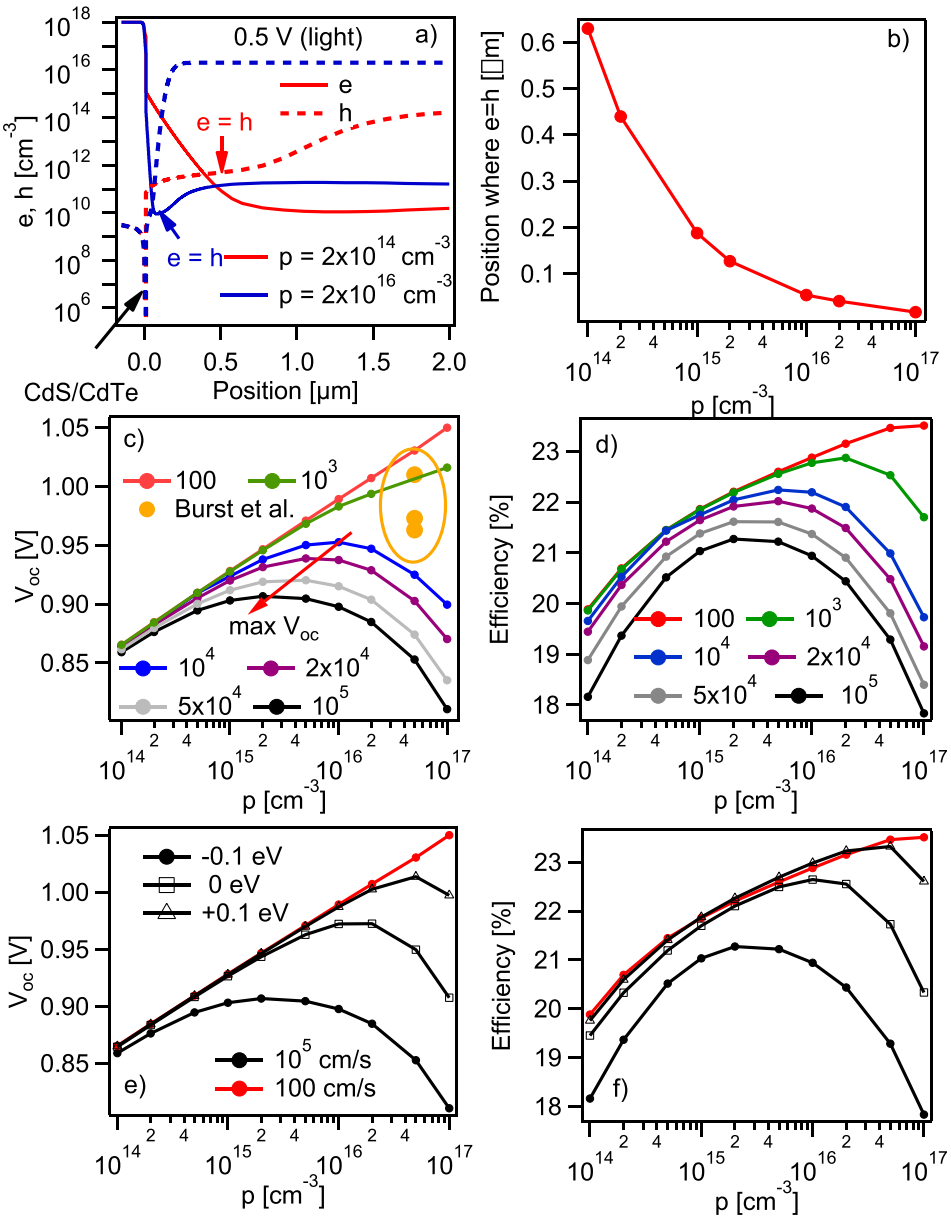

FIG. 4. (a) Calculated electron (solid lines) and hole density (dashed lines) as a function of position under 0.5 V forward bias and light. (b) A position in the absorber where e = h as a function of doping. Calculated impact of absorber doping on (c) V_{oc}, (d) efficiency, for different values of interface recombination velocity. Experimental values for the best V_{oc} are shown with orange circles. Calculated impact of absorber doping on (e) V_{oc}, (f) efficiency for different band alignments. For (e) and (f), CBO is −0.1 eV for S = 100 cm/s.

efficiency trends follow V_{oc} [Fig. 4(d)] and the J_{sc} trends with S_{Int} described earlier. Experimental V_{oc} values by Burst *et al.*[4,39] are shown in Fig. 4(c). The interface recombination must be below 10^4 cm/s for these samples to achieve the measured voltages close to and above 1 V. The simulations here assume a highly doped TCO and a very thin CdS layer, so the band bending occurs primarily inside the CdTe absorber. If the buffer layer is thicker with a low electron concentration, some of the space charges will be located in the buffer, and the S_{int} impact can be significantly higher.

The calculations presented above assume a conduction-band offset of −0.1 eV (Refs. 31 and 40) at the CdS/CdTe interface. The optimal band alignment to suppress interface recombination is between +0.1 and +0.3 eV.[41] Tailoring band alignment can change the density of carriers available for recombination, and alter the importance of interface passivation. The band alignment can be altered by alloying either of the junction partners: CdS or CdTe.[40]

This is illustrated in Figs. 4(e) and 4(f). In the presence of an unpassivated interface ($S_{int} = 10^5$ cm/s), the aligned bands (CBO = 0 eV) increase the optimal doping from $p = 2 \times 10^{15}\,cm^{-3}$ to $2 \times 10^{16}\,cm^{-3}$, and maximum V_{oc} from ~900 mV to >950 mV. As the CBO increases, the maximum possible V_{oc} is higher, the device performance tolerance to interface recombination increases, and higher doping improves cell performance further. For CBO = +0.1 V, for example, the optimal doping is $p = 5 \times 10^{16}\,cm^{-3}$ and $V_{oc} > 1$ V is possible. The impact of band alignment in CdTe devices was studied in detail in Ref. 41.

Research on $Cu(In,Ga)Se_2$ (CIGS) devices has considered the band offset and interface recombination issues. CIGS devices perform best for compositions with around 30% Ga/(In + Ga) ratio. It may be possible that point defect, stoichiometry, and/or lattice match issues contribute to this finding. Another suggested mechanism is that the conduction-band offset at the CIGS/CdS interface is positive,[42] which creates absorber inversion and suppresses interface recombination. Decreased or negative offset due to either CIGS or buffer layer alloying can increase interface recombination and lower V_{oc}.[43,44] This has been described as the main conversion efficiency loss in wide band gap CIGS devices.[45,46] In addition to developing methods for interface passivation and alloying the buffer layer with an element that will increase its band gap in the conduction band, the interface recombination rate can also be decreased by alloying the absorber layer in the vicinity of the junction with an element that will increase the band gap in the valence band and create a hole barrier. Buried junctions may also displace the peak electron and hole recombination populations from the metallurgical interface. Similarly, the results in Fig. 4 indicate that band offset engineering in CdTe may offer methods to reduce the impact of interface recombination.

B. Grain size and grain boundaries in polycrystalline materials

While very often during device performance analysis one approximates the absorber as a uniform medium with averaged properties, the optimization of deposition methods requires knowledge of the relative impact of recombination on the grain interior and the grain boundaries. To explore the separated impact of grain size, grain boundary recombination, and intra-grain lifetime on device performance, we create a model with two columnar grain boundaries [Fig. 1(a)]. Figures 5(a)–5(d) show calculated V_{oc}, J_{sc}, FF, and efficiency as a function of the grain-boundary recombination velocity (S_{GB}) for 1 μm grains (green), 3 μm grains (red), and 20 μm grains (black). The intra-grain lifetime is 1 ns (L = 0.9 μm), 10 ns (L = 2.64 μm), or 100 ns (L = 9.1 μm).

For 1 μm grains (green curves in Figs. 5(a)–5(d), the grain size is comparable to or lower than the diffusion length for all analyzed lifetimes, and therefore, the average lifetime of the material is dominated by the region with the highest recombination.[47]

S_{GB} has a very strong impact on device performance, and the slopes of the green curves are steep. For the samples with 1 μm grains and $S_{GB} > 10^5$ cm/s, the cell performance is dominated by S_{GB}, which reduces the benefit of increased bulk lifetime (green curves converge to similar values of V_{oc} and efficiency for $S_{GB} = 10^6$ cm/s).

For large-grain samples (20 μm) the bulk lifetime is very important. In this case, the increased bulk lifetimes can alter the efficiency from 19% to 24%.

These modeling results agree with the experimental time-resolved photoluminescence measurements by Jensen *et al.*[48] For a small grain size, the grain boundary recombination dominates the TRPL signal and performance. As the grain size increases, the impact of grain boundaries on TRPL lifetime and device performance decreases. Figure 5(e) shows that V_{oc} scales with grain size and inversely with S_{GB}; in other words, it directly scales with the effective, or aggregate, absorber lifetime. In this model, the grains are two-dimensional, and adding a third dimension would increase the ability of the grain boundaries to influence the recombination and performance.

C. Quantification of performance increase by different optimization routes

To summarize the above analysis, we quantify how the improvement of various electronic parameters individually and simultaneously impacts the V_{oc} and efficiency. Improving the material properties: hole density, lifetime, and interface passivation are beneficial to the device performance. However, the magnitude of the improvement is convoluted with the different material properties. The results in Fig. 6 emphasize the interdependence of material enhancements.

We start from a common pX CdTe device, namely, $\tau = 1$ ns, $p = 2 \times 10^{14}\,cm^{-3}$, and $S_{int} = 10^5$ cm/s. This device has a $V_{oc} = 0.81$ V, $\eta < 16\%$, and is labeled in the figure with "1 ns." Next, we calculate the V_{oc} and efficiency improvement by increasing only the aggregate bulk lifetime [Fig. 6(a)]. As discussed previously, altering the grain size and grain boundary recombination can strongly influence the aggregate lifetime (which is what TRPL measures). Such an increase in the lifetime from 1 to 10, or 100 ns results in V_{oc} increase by 60 and 75 mV, respectively, and efficiency improves to 20%.

The importance of doping and interface passivation for a specific carrier lifetime is shown in Figs. 6(b)–6(d). In a 1 ns device [Fig. 6(b)], an improved interface passivation from $S_{int} = 10^5$ cm/s to $S_{int} = 100$ cm/s (low S_{int}) provides an insignificant V_{oc} increase. Increased hole density from $p = 2 \times 10^{14}$ to $p = 2 \times 10^{16}\,cm^{-3}$ (high p), without additional surface passivation increases V_{oc} by 70 mV. However, the hole density and surface passivation together yield a more significant improvement. The higher impact of joint S_{int} and p increase is more prominent for the devices with $\tau = 10$ ns and $\tau = 100$ ns, as shown in Figs. 6(c) and 6(d).

Only the combination of three parameters: high aggregate lifetime, low interface recombination by passivation and/or offset engineering, and high hole density can lead to $V_{oc} > 1$ V and efficiency towards 25%. A combination of any two parameters alone is insufficient to achieve these results.

Increased lifetime in high efficiency CdTe devices increases the diffusion length, and thus, many highly efficient devices are "electronically thin" (i.e., the diffusion length is longer than the absorber thickness). In these absorbers, considerably more carriers reach the back contact, making losses due to back contact recombination more impactful. In addition to the recombination at the back contact, the back contact barrier is a known problem in px CdTe devices. In this work, we have concentrated on the front interface and absorber properties, as they are crucial for the next steps in device performance. Once achieved, the passivated back contact configurations, back surface fields, texturing, and other approaches to further increase performance can represent the next phase of efficiency improvements, which will be the subject of future analysis.

IV. CONCLUSIONS

Numerical simulation analysis was used to explore the material properties required to increase the performance of polycrystalline CdTe solar cells towards 25%. While the community has achieved a range of aggregate carrier lifetimes, voltages across the community are lower than

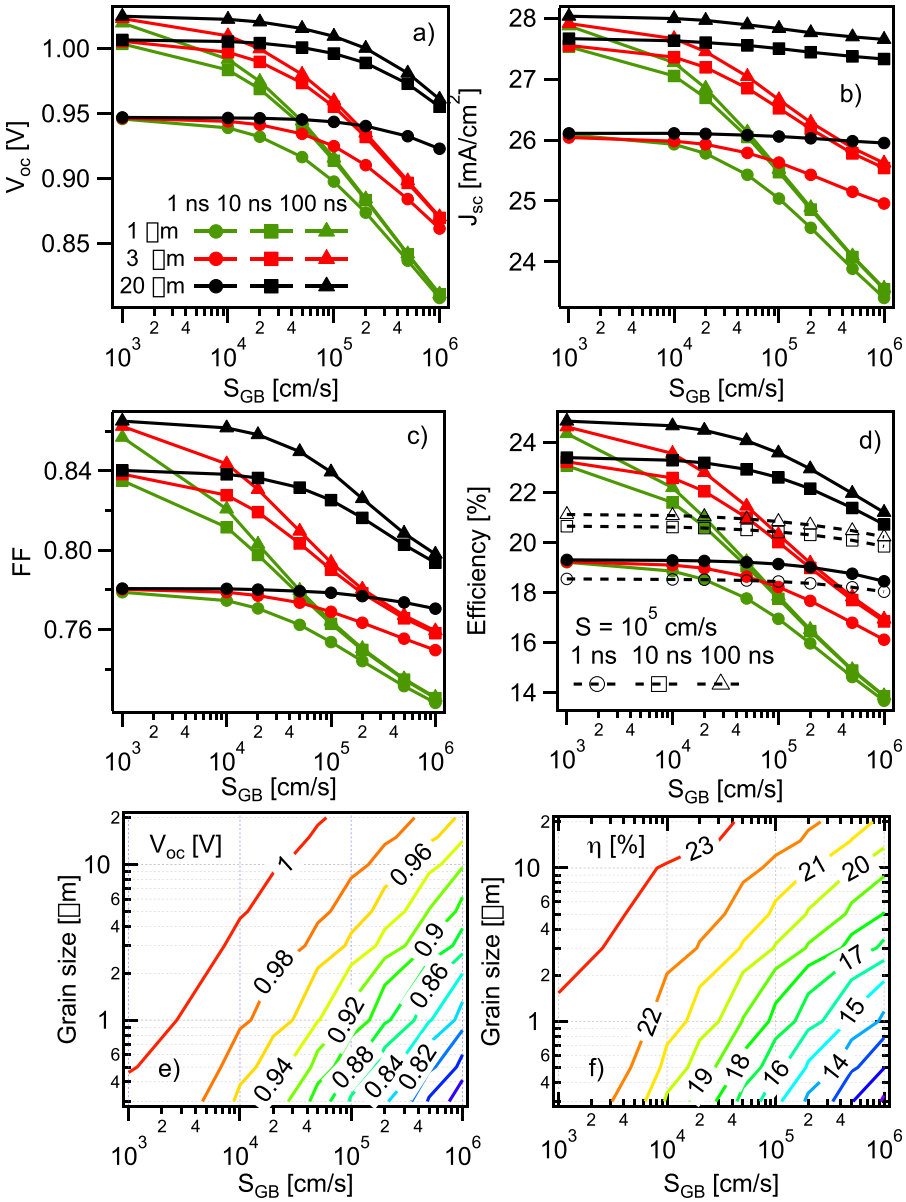

FIG. 5. (a)–(d) Simulated cell performance as a function of grain boundary recombination velocity (S_{GB}) for grain sizes: 1 μm (green), 3 μm (red), and 20 μm (black); bulk lifetimes: 1 ns (circles), 10 ns (squares), and 100 ns (triangles). $S_{int} = 100$ cm/s and $p = 2 \times 10^{16}$ cm^{-3}. To re-emphasize the impact of S_{int}, the efficiency for 20-μm grains when $S_{int} = 10^5$ cm/s is shown with dashed lines in (d). (e) and (f) Simulated contour plots showing the combined impact of grain size and grain boundary recombination on V_{oc} and efficiency for $\tau_b = 10$ ns.

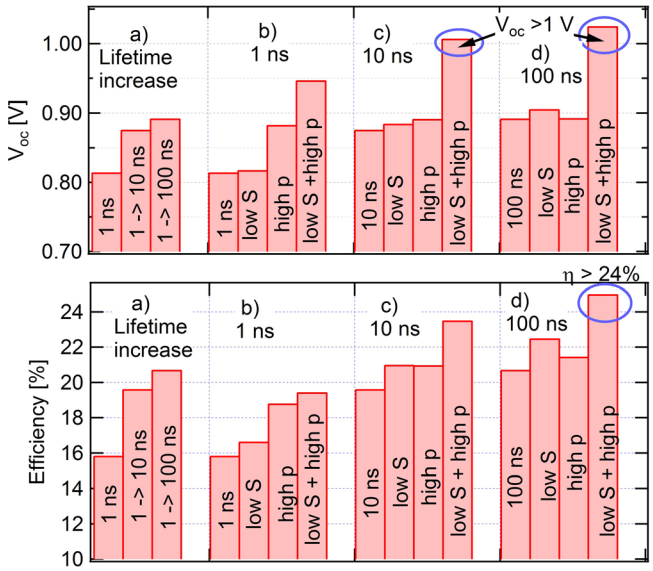

FIG. 6. Calculated V_{oc} and efficiency enhancements as a result of improvement of different parameters separately, and in combination. The 1, 10, and 100 ns cases assume high interface recombination of $S_{int} = 10^5$ cm/s and $p = 2 \times 10^{14}$ cm^{-3}. Low S_{int} corresponds to a change in interface recombination velocity to $S_{int} = 100$ cm/s; and high p corresponds to $p = 2 \times 10^{16}$ cm^{-3}.

theoretically possible. Increasing the hole concentrations will be critical in moving the technology forward. However, these results indicate that it is necessary but not sufficient to have a high quality absorber with a high lifetime and hole density. As absorber doping is increased, the deleterious impact of interface recombination velocity (S_{int}) increases. For example, $S_{int} = 10^5$ lowers V_{oc} by 20–30 mV at $p = 2 \times 10^{14}$ cm^{-3} but for $p = 2 \times 10^{16}$ cm^{-3}, the impact of S_{int} is very high, and can make a difference between 880 mV and >1 V. Careful band offset engineering by alloying of either absorber or emitter layer can minimize the impact of interface recombination. Creating a buried heterojunction can also mitigate the interface recombination by decreasing the density of holes in the vicinity of the interface. As these issues are overcome, small grains and GB recombination can create a bottleneck to higher efficiencies. Consequently, achieving conversion efficiency >25% requires simultaneous optimization of multiple CdTe material properties including high hole density, high carrier lifetime, reduced interface recombination, and large grains with low S_{GB}.

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