# Influence of high-temperature GaN annealed surface on the electrical properties of Ni/GaN Schottky contacts

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In this work, the electrical properties of Ni/GaN Schottky contacts formed on high-temperature annealed (1100–1200 °C) GaN surfaces were studied. Although the morphology of the GaN surface was not changing after annealing, a worsening of the electrical behavior of the Schottky contact occurred, with a reduction in the barrier height and an increase in the leakage current. Moreover, a different temperature dependence of the reverse electrical characteristics of the Schottky diodes was observed. In particular, for the sample annealed at 1150 °C for 5 min, one-dimensional variable-range-hopping conduction was one of the dominant carrier transport mechanisms. The presence of a high density of interface states was indicated as a possible reason of this electrical behavior. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3006133]

## I. INTRODUCTION

Wide band gap semiconductors have recently attracting a rising interest for applications in high power, high frequency, and high temperature electronic devices. Among them silicon carbide (SiC) is surely the most mature both in terms of material quality and device processing particularly for high power devices. On the other hand, gallium nitride (GaN) and related materials are more suitable for high frequency application heterojunction devices due to the formation of a high mobility two-dimensional electron gas (2DEG) at the AlGaN/GaN interfaces. However, in the past few years, the improvement of the crystal quality of GaN-based materials has made them competitive to SiC also for high power devices achievement. Furthermore, some scientific works had already demonstrated high voltage GaN Schottky diodes.[1–4] Recently, Liu *et al.*[5] reported the first reliable and packaged high voltage (>600 V) GaN Schottky barrier devices, opening interesting perspective for the material in the field of power diodes. In particular, through an optimal epitaxial growth process, GaN epilayer with a very low density of the conductive dislocations ($10^3$ $cm^{-2}$) on the surface allowed to obtain diodes with a leakage current of 180 $\mu$A at the reverse bias of 600V and with a forward current of 6A at $V_F$ = 1.7 V. According to these promising results GaN Schottky diodes were considered as alternative to SiC-based devices offering the same performance benefits at a significantly lower cost, when GaN is grown by heteroepitaxy on cheap substrates like silicon or sapphire.

However, several critical problems deserve a deeper scientific investigation for achieving a further improvement in the technology of GaN power diodes. For example, a critically opened issue is the high leakage current of Schottky contacts, basically ascribable to two main factors. One includes the presence of defects in the bulk GaN, charged surface states, or metal induced gap states, which enhance the tunneling current through the metal/GaN Schottky barriers.[6,7] In this context, the knowledge of current transport mechanisms through the contact in relation to the presence of these defects can help understand the physical causes of the high leakage. The other factor is the breakdown initiated in the depletion region near the electrode corners, for which the employment of edge terminations, such as mesas, field plates,[8,9] and implanted guard rings[10] can improve the reverse characteristics, by smoothing out the electric field distribution around the device periphery. Although in SiC edge terminations in power Schottky diodes have enabled a significant reduction in the leakage current, improving the breakdown voltage,[8–10] these methods are still little developed in GaN.

For *n*-type GaN device active layer a highly resistive layer around the Schottky contact periphery can be formed by ion implantation of a *p*-type dopant species. Even though ion-implanted edge termination can be a solution for increasing the breakdown voltage, few reports about this method in GaN are present in literature.[11,12] The most used *p*-type dopant is magnesium (Mg) because of its shallowest ionization level (170 meV).[13] However, in order to obtain a *p*-type compensation of Mg-implanted *n*-type GaN layers, rapid annealing processes at high temperatures (1100–1200 °C) are required.[14] In this case, however, appropriate protective capping layers ($SiO_2$, AlN, etc.) must be used to prevent the sample surface degradation upon annealing.[13] Beyond the knowledge of Mg-dopant electrical activation upon annealing, in the implementation of *p*-type implanted guard rings it is equally important to understand how the electrical behavior of metal/GaN Schottky barriers is influenced by the properties of the high temperature annealed material surface. In this context, Lee *et al.*[15] observed that the reverse diode characteristics were significantly degraded even after an annealing at 900 °C. The increase in the leakage current was attributed to the preferential loss of nitrogen from the GaN surface after high temperature annealing. The nitrogen loss results in the increase in the surface carrier concentration, thus enhancing the tunneling mechanism at the metal/GaN

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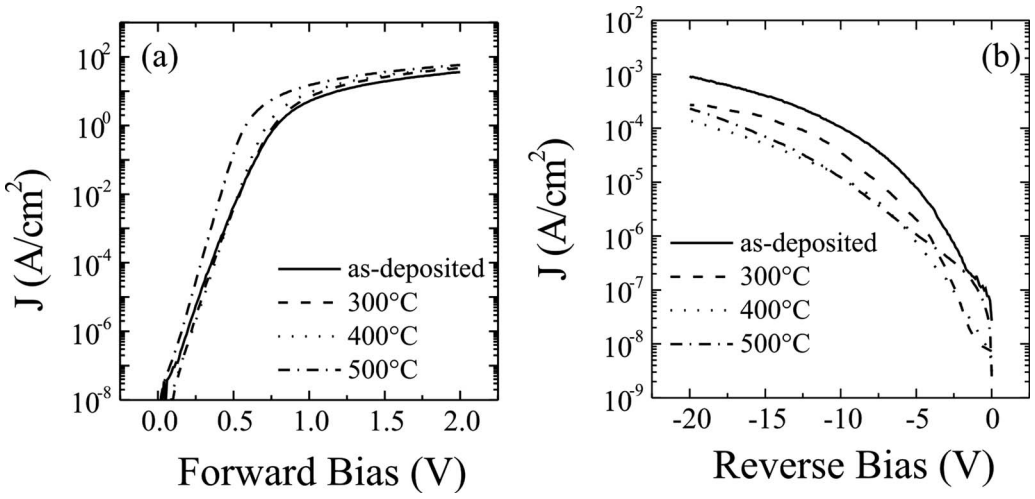


FIG. 1. Forward (a) and reverse (b) *J-V* characteristics of the Au/Ni/GaN diodes, both before and after different annealing processes.

interface and, hence, increasing the leakage current.[15] The outdiffusion of nitrogen from GaN surface for annealing temperature above 800 °C was later demonstrated by means of the Rutherford backscattering spectrometry analyses.[16] In these works, however, the surface was not protected by an opportune capping layer during annealing.

In this work, the temperature dependence of the electrical characteristics of Ni/GaN Schottky contacts was investigated, considering possible carriers transport mechanisms through the metal/GaN interface. In particular, the electrical behavior of Ni/GaN Schottky contact formed on high temperature annealed (1100–1200 °C) GaN surface was discussed in terms of surface morphology and interface states density in the annealed samples.

## II. EXPERIMENTAL

Si-doped (*n*-type) GaN epitaxial layers, 3 $\mu$m thick with a concentration $N_D=3.8\times10^{16}$ cm$^{-3}$ (as determined by capacitance-voltage measurements), on a heavily doped $n^+$ GaN layer ($N_D=2\times10^{18}$ cm$^{-3}$), grown by Lumilog on sapphire substrates, were used in this work. In order to study the electrical properties of Schottky contact formed on high temperature annealed (1100–1200 °C) GaN surface, Schottky diodes were fabricated on three different GaN samples: one was not subjected to annealing (nonannealed sample), another was subjected to an annealing at 1150 °C for 5 min (1150 °C sample), and another to 1200 °C for 30 s (1200 °C sample). The annealing processes, performed in $N_2$ atmosphere, were chosen considering our previous systematic results obtained for Mg-dopant electrical activation. Contrary to other previous works,[15,16] in our case a $SiO_2$ protective layer was used during high temperature annealing to limit the surface degradation and removed before fabricating the Schottky diodes. These diodes consisted of a large area ring-shaped Ohmic contact, formed by the sputtering of a Ti/Al/Ni/Au multilayer and subsequent annealing at 750 °C in Ar,[17] and a circular Ni/Au bilayer (with radius of 220 $\mu$m) as Schottky contact. Postdeposition annealing processes in the range 300–500 °C in Ar atmosphere were performed using a Jetfirst Jipelec rapid furnace.

The current-voltage (*I-V*) characteristics of the Schottky diodes were measured at different temperatures, ranging between 25 and 175 °C, using a temperature controlled Suss Microtec probe station equipped with an Agilent 4155C parameter analyzer. Capacitance-voltage (*C-V*) measurements were performed with an Agilent 4284A parameter analyzer, in the frequency range of 0.1 kHz–1 MHz to determine the densities of interface states in the three samples.[18] The morphology of the GaN surface was evaluated by means of a Veeco Dimension 3100 atomic force microscopy (AFM) operating in tapping mode.

## III. RESULTS AND DISCUSSION

### A. Electrical properties of Ni/GaN Schottky contacts

The current-voltage measurements were performed on several Au/Ni/GaN Schottky diodes, before and after postdeposition annealing processes between 300 and 500 °C. The current density–voltage (*J-V*) characteristics under forward and reverse bias of the Au/Ni/GaN diodes, both before and after annealing, are reported in Figs. 1(a) and 1(b) in a semilogarithmic scale. The curves reported in Fig. 1 for each annealing temperature are averaged over several measurements acquired on different diodes and hence they describe well the average electrical behavior of the contact.

The forward characteristics did not show any significant change up to the annealing temperature of 400 °C, while an improvement of the ideality factor is clearly visible at 500 °C. This improvement can be attributed to the combined effects of metal/semiconductor interfacial reaction and of different phases formed between two metals during annealing, as reported by Sun *et al.*,[19] who detected the formation of compounds, such as $Ni_4N$ and $AuGa_2$, at the GaN/metal interface under similar annealing conditions. On the other hand, under reverse bias, the leakage current decreased after annealing at 300 °C, but it did not show any significant change at higher annealing temperatures. The values of $\Phi_B$ and $n$ were determined from a fit of the linear region of the forward *I-V* curves, where $qV>3kT$, according to the thermionic emission model:[20]

TABLE I. Barrier height and ideality factor determined from the *J-V* curves of Fig. 1(a) for the as-deposited and annealed samples.

| | As-deposited | 300 °C | 400 °C | 500 °C |
|---|---|---|---|---|
| Barrier height (eV) | 0.89 | 0.92 | 0.92 | 0.88 |
| Ideality factor | 1.31 | 1.19 | 1.24 | 1.07 |

$$I = AA^*T^2 \exp\left(-\frac{\Phi_B}{kT}\right)\exp\left(\frac{qV}{nkT}\right) = I_S \exp\left(\frac{qV}{nkT}\right), \qquad (1)$$

where $A$ is the contact area, $A^*$ is the Richardson constant, $T$ is the absolute temperature, $q$ is the electron charge, $k$ is the Boltzmann constant, $\Phi_B$ is the Schottky barrier height, and $n$ is the ideality factor. For this calculation, the theoretical value of the Richardson's constant for GaN ($A^*$ =26.9 A cm$^{-2}$ K$^{-2}$) (Ref. 21) was used.

The values of the barrier height and of the ideality factor determined from the *I-V* curves at different annealing temperatures are summarized in Table I. For the as-deposited contact a Schottky barrier height $\Phi_B$=0.89 eV and an ideality factor of $n$=1.31 were found. Clearly, a deviation of the experimental value of barrier height (0.89 eV) from the ideal Schottky–Mott barrier (1.01) occurs, which can be related to the intrinsic metal/GaN interface properties such as the presence of material defects[22] and/or surface states induced by the Ni deposition process.[23] As can be seen, while the barrier height was almost insensitive to the annealing process, the ideality factor strongly improves upon annealing at 500 °C, decreasing from 1.24 to 1.07.

In order to get further insights on the carrier transport through the metal/GaN contact and on the electrical parameters, the forward and reverse current-voltage characteristics were measured between 25 and 175 °C (*J-V-T*). Figure 2(a) shows the forward *J-V* characteristics of the Ni/GaN diodes annealed at 500 °C. This postdeposition annealing temperature has been chosen for our analysis because the diodes exhibited the best characteristics in terms of ideality factor ($n$=1.07) at room temperature.

As can be seen, the forward current of the diodes at a fixed bias increases with increasing temperature. From the experimental data reported in Fig. 2(a), the values of the saturation current $I_S$ were determined at each temperature, and a "conventional" Richardson's plot,[20] $\ln(I_S/T^2)$ versus $1/kT$, is reported in Fig. 2(b). From the fit of the experimental data, a Schottky barrier height $\Phi_B$=0.86 eV and a Richardson's constant $A^*$=9 A cm$^{-2}$ K$^{-2}$ were extracted. Although the value of $A^*$ found with this analysis is lower than theoretical value (26.9 A cm$^{-2}$ K$^{-2}$), it is higher than other values reported in literature for Ni/GaN contacts.[6,24,25] This anomaly, often observed in other semiconductor materials,[26] can be attributed to different factors. As an example, in our previous work on Pt/Au Schottky barriers, it was demonstrated that a significantly low value of the Richardson's constant ($4\times10^{-3}$ A cm$^{-2}$ K$^{-2}$) could be related to the formation of a laterally inhomogeneous Schottky barrier, where the presence of material surface defects plays an important role in the electrical properties of the contact.[27]

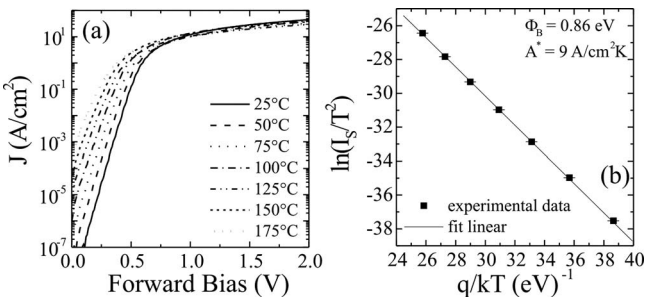


FIG. 2. Forward *J-V* characteristics of the Ni/GaN diodes at increasing temperatures in the range of 25–175 °C for the sample annealed at 500 °C (a). Extracting from (a) the saturation current $I_S$ at each temperature, the conventional Richardson's plot $\ln(I_S/T^2)$ vs $1/kT$ is also reported (b).

From the *J-V-T* curves, the values of the Schottky barrier height $\Phi_B$ and of the ideality factor $n$ of the diodes were determined at the different measured temperatures and are summarized in Table II. While for the ideality factor, a weak dependence on the measure temperature can be observed ($n$ decreases from 1.07 at 25 °C to 1.03 at 175 °C), the barrier height is almost independent of temperature ($\Phi_B$ =0.89–0.90 eV).

In Fig. 3 the reverse characteristics between 25 and 175 °C are reported. It is possible to notice that the higher the reverse bias is, the weaker is the temperature dependence of the reverse leakage current. Obviously, the dominant transport mechanism depends both on temperature and bias.

The occurrence of a transport mechanism in a metal/semiconductor interface can be described by the ratio between the characteristic energy $E_{00}$ and the thermal energy $kT$. The characteristic energy $E_{00}=(h/4\pi)\sqrt{(N_D/m^*\varepsilon)}$ is a parameter related to the probability that the electrons tunnel the barrier. In particular when $E_{00}\ll kT$ the thermionic emission (TE) dominates, thermionic field emission is dominant if $E_{00}\sim kT$, while the field emission transport occurs for $E_{00}\gg kT$. In our case, since $E_{00}$=2.5 meV and $kT$ ranges between 25.9 and 38.8 meV, the condition $E_{00}\ll kT$ is satisfied, and the TE is expected to be the dominant transport mechanism. Hence, the theoretical curves of TE mechanism, given by the relation:

$$J = A^*T^2 \exp\left(-\frac{\Phi_B - \Delta\Phi_B}{kT}\right) \qquad (2)$$

were superimposed to the experimental reverse characteristics of the contacts at 25 and 175 °C.

In Eq. (2) $\Delta\Phi_B$ represents the barrier lowering due to the image force between an electron and a surface of the metal.[20] In particular, in Fig. 3(a) the theoretical TE curves at 25 °C and at 175 °C were calculated using the barrier height extracted from the forward characteristics and the experimental Richardson's constant (9 A cm$^{-2}$ K$^{-2}$).

As can be seen, at room temperature a strong discrepancy between the experimental and TE model is observed, meaning that a pure thermionic carrier transport cannot justify the electrical *I-V* characteristics. This latter could be ascribed to the presence of other transport mechanisms, whose occurrence is correlated with the material quality and the presence of defects.[28,7] On the other hand, at 175 °C with, the TE mechanism becomes dominant for lower reverse bi-

TABLE II. Schottky barrier height and of the ideality factor determined from the *J-V-T* curves of Fig. 2(a).

| | 25 °C | 50 °C | 75 °C | 100 °C | 125 °C | 150 °C | 175 °C |
|---|---|---|---|---|---|---|---|
| Barrier height (eV) | 0.89 | 0.89 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 |
| Ideality factor | 1.07 | 1.06 | 1.06 | 1.05 | 1.05 | 1.04 | 1.03 |

ases (up to −5 V), as can be seen from the better agreement of the calculated curves with the experimental data.

### B. Effects of high-temperature annealed surface on the electrical behavior of the contacts

As previously pointed out, the employment of Mg ion-implanted guard ring edge termination is a possible solution to improve the reverse characteristics of the GaN-based power Schottky diodes. However, annealing temperatures between 1150 and 1200 °C are necessary to obtain the electrical activation of Mg implanted *n*-type GaN.[14] Since such thermal processes could influence the behavior of Schottky contacts, the morphology of high-temperature annealed GaN samples was correlated with the electrical properties of Ni/Au Schottky diodes fabricated on these surfaces. For this purpose, the Schottky contacts were fabricated on three different GaN samples: one that was not subjected to annealing (nonannealed sample), another one was subjected to 1150 °C for 5 min (1150 °C sample), and another to 1200 °C for 30 s (1200 °C sample).

The current density–voltage (*J-V*) characteristics under forward and reverse bias of the as-prepared Au/Ni/GaN diodes, for all three samples, are reported in Figs. 4(a) and 4(b) in a semilogarithmic scale.

As can be clearly seen, the annealing processes have a significant effect on the electrical behavior. In fact, thermal annealing leads both to a worse linearity and to a shift toward left for the forward curves, accompanied by an increase in the reverse leakage current.

The sample annealed at 1200 °C for 30 s exhibits a better electrical behavior than the sample annealed at a lower temperature (1150 °C) but for a longer time (5 min). This result suggests the detrimental effect of the annealing time on the electrical properties of the Schottky barrier. Moreover, it is possible to notice that the forward current above 1 V in the nonannealed sample is higher than the other samples, indicating a lower value of the on-resistance of the diodes. In particular, from the value of the forward current [Fig. 4(a)] it can be seen that the on-state resistance of the nonannealed contact is about a factor of 7 lower than in the case of the annealed samples. A possible explanation to this behavior can be an increase of the contact resistance of the Ohmic contacts fabricated on the annealed surface. However, it cannot be ruled out that morphological and/or compositional changes in the epilayer due to high temperature annealing can affect the electrical properties of the near-surface region, leading to the experimentally observed increase in the device on-resistance.

The values of $\Phi_B$ and $n$ were determined from a fit of the linear region of the forward *I-V* curves. A significant decrease in the barrier height and increase of the ideality factor from the nonannealed to the annealed ones was observed. This behavior is particularly evident for the sample annealed at 1150 °C. Indeed, the barrier height decreases from 0.89 eV for the nonannealed sample to 0.57 eV for the sample annealed at 1150 °C, while the ideality factor increases from 1.31 to 3.3.

Thereafter, a postdeposition annealing at 500 °C for 60 s was carried out for all three samples with the aim to achieve an almost ideal behavior of the Au/Ni/GaN Schottky barrier, has already shown in Sec. III A. From the *J-V* characteristics under forward and reverse bias for the three samples (not reported here), an improvement in the nonannealed and 1200 °C annealed samples was observable, although the

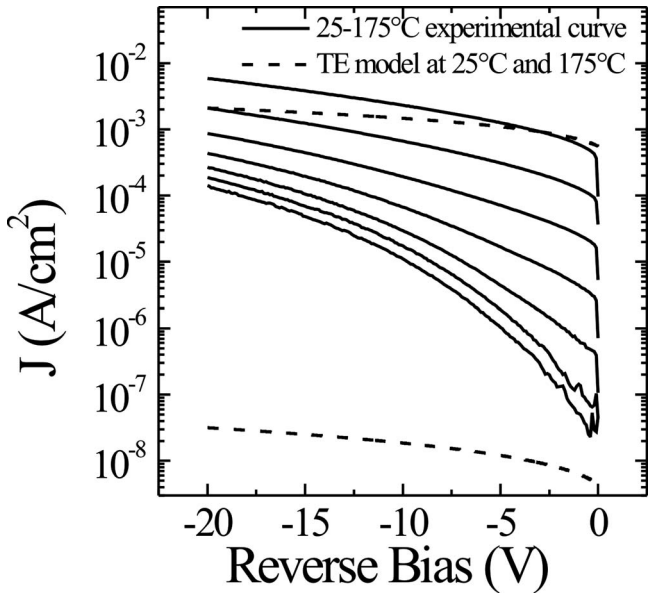


FIG. 3. Reverse *J-V* characteristics of the Ni/GaN diodes at increasing temperatures in the range of 25–175 °C for the sample annealed at 500 °C. Moreover, the respective TE curves obtained by Eq. (2) at 25 and 175 °C are superimposed.

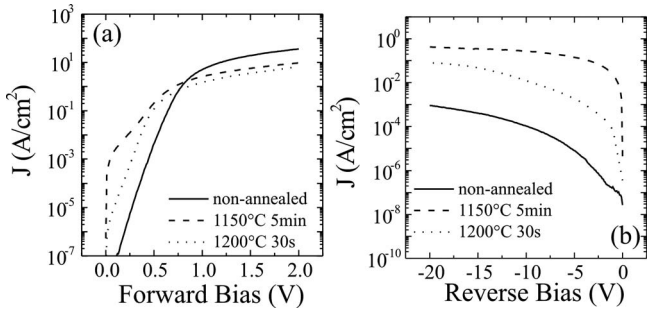


FIG. 4. Forward (a) and reverse (b) *J-V* characteristics of the as-deposited Au/Ni/GaN Schottky diodes for the nonannealed, 1150, and 1200 °C samples.

TABLE III. Barrier height and ideality factor of the as-deposited and of the annealed at 500 °C Au/Ni/GaN Schottky contact for the nonannealed, 1150, and 1200 °C samples.

| As-prepared Schottky contact | Ideality factor | Barrier height (eV) |
|---|---|---|
| Nonannealed | 1.31 | 0.89 |
| 1200 °C for 30 s | 1.36 | 0.76 |
| 1150 °C for 5 min | 3.3 | 0.57 |

| Schottky contact annealed at 500 °C | Ideality factor | Barrier height (eV) |
|---|---|---|
| Non-annealed | 1.07 | 0.88 |
| 1200 °C for 30 s | 1.27 | 0.91 |
| 1150 °C 5 min | 3.4 | 0.61 |

electrical properties remained strongly dependent of the initial high-temperature process seen by the surface. In particular, the sample whose surface was not subjected to high temperature thermal annealing before Schottky metal deposition (nonannealed) preserved better characteristics than the high temperature annealed samples, either in terms of forward bias linearity and reverse leakage current density. Also in this case the nonannealed sample had the smallest on-state resistance. Table III summarizes the values of the barrier height and the ideality factor of the as-prepared contact and of the contact subject to the postdeposition annealing at 500 °C, for all three annealed surfaces. Clearly, a different behavior is observed after post-deposition annealing at 500 °C for the three samples. In particular, while for the nonannealed sample and 1200 °C sample postdeposition annealing at 500 °C can lead to an improvement in the electrical parameters, in the case of the sample annealed at 1150 °C for 5 min both the ideality factor and the barrier height remain almost unchanged.

The surface morphology of GaN surface was evaluated by means of AFM to check if any surface modification due to high-temperature annealing (prior to metal deposition) can be related to the different electrical characteristics of the contacts. The AFM images of GaN surface of the nonannealed sample and of the samples annealed at 1150 °C and 1200 °C are shown in Figs. 5(a)–5(c), respectively. The images were acquired after high temperature annealing and removal of the $SiO_2$ protective layer. Surprisingly, the annealing process does not significantly change the morphology of GaN, both roughness and morphology of the three sample are comparable. In particular, the average surface roughness (rms) of the nonannealed, 1150, and 1200 °C samples are 2.5, 3.2, and 2.8, respectively. This result demonstrates that the worse electrical characteristics of the contacts formed on high temperature annealed surface is not strictly related to the surface morphology, that in turn, is almost completely preserved in the presence of the $SiO_2$ capping layer. A similar result was obtained in silicon carbide (SiC) by Roccaforte *et al.*,[29] who observed that Ni/SiC Schottky contacts fabricated on surfaces with a similar morphology (rms =0.3 nm) can exhibit a different electrical behavior (ideality factor and barrier height). However, for high surface roughness values (>10 nm), a significant lowering of the barrier height with a poor ideality factor occurs.

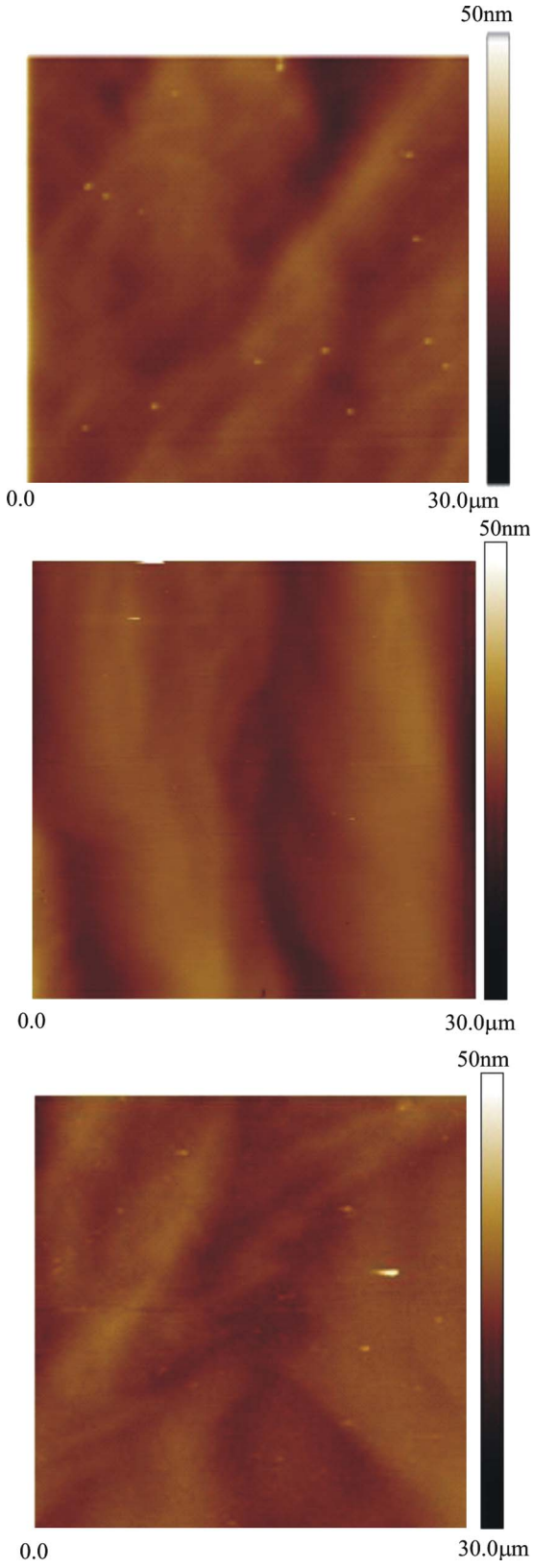


FIG. 5. (Color online) AFM images of the GaN surface for the nonannealed sample (a), and for the samples annealed at 1150 °C for 5 min (b) and at 1200 °C for 30 s (c).

The forward and the reverse current-voltage characteristics were measured at several temperatures (*J-V-T*). From the reverse *J-V* characteristics of the Ni/GaN diodes annealed at 500 °C for all three samples a different temperature depen-

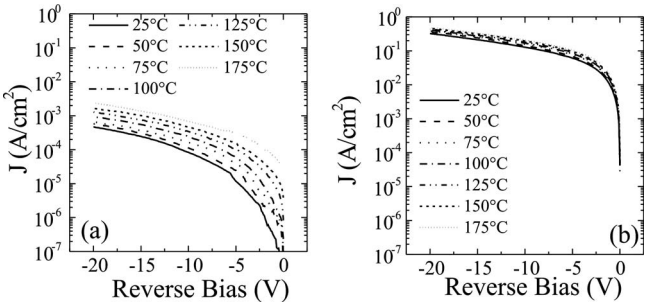


FIG. 6. Reverse *J-V-T* characteristics of the Ni/GaN diodes annealed at 500 °C respectively for the sample annealed at 1200 °C (a) and at 1150 °C (b).

dence can be observed [Figs. 3, 6(a), and 6(b)]. In particular, the nonannealed sample (Fig. 3) shows a stronger temperature dependence of the leakage current with respect to the samples annealed at 1200 °C [Fig. 6(a)] and at 1150 °C [Fig. 6(b)]. The weak temperature dependence of the reverse leakage for the 1150 °C sample suggested the predominance of a transport mechanism based on tunneling conduction, such as one-dimensional variable-range-hopping mechanism.[30] This latter can be favored by the presence of material defects that induce deep levels near the metal/semiconductor interface. In this case, the most probable path for electron is through deep levels situated at larger distance but having smaller energy differences [Fig. 7(b)]. According to the expression of the reverse saturation current for the hopping conduction, $J \propto \exp(-T_0/T)^{1/4}$,[30] where $T_0$ is the characteristics temperature, the logarithm of current density $J$ at a bias of −20 V is reported as a function of $(T)^{-1/4}$ [Fig. 7(a)]. As can be seen, for the sample annealed at 1150 °C this plot exhibits an almost linear behavior with respect to nonannealed samples, meaning that in this sample the hopping conduction is one of the dominant mechanisms. For the sample annealed at 1200 °C, instead, the linear behavior was not observed for all temperature range.

This electrical behavior of the Schottky contacts formed on high temperature annealed GaN surface can be related to the formation of a high density of interface states induced by the thermal process. This assumption was supported by capacitance-voltage measurements at different frequencies, carried out for all three samples [Fig. 8] using the Schottky

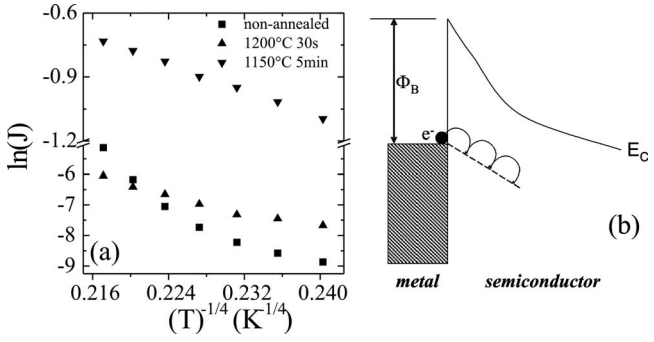


FIG. 7. Logarithm of current density $J$ at a bias of −20 V as a function of $(T)^{-1/4}$ for the nonannealed, 1150, and 1200 °C samples (a). Schematic of the energy band diagram showing the one-dimensional variable-range-hopping conduction (b).

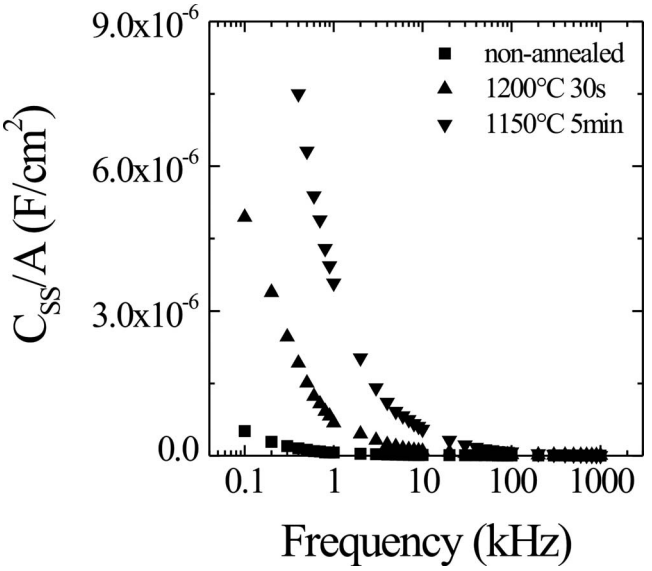


FIG. 8. Interface state capacitance $C_{SS}$ as a function of the frequency for the nonannealed, 1150, and 1200 °C samples.

capacitance spectroscopy (SCS) method.[18] Indeed, the frequency dependent capacitance-voltage measurements enable to obtain information on the interface states in a Schottky contact. Basically, the SCS method allows to determine the variation in the interface state capacitance as a function of the forward bias at low frequency measurement. At sufficiently high frequencies (1 MHz) the interface states do not contribute to the capacitance because the charge at the interface states cannot follow the ac signal. Hence, in this case, the measured capacitance is only due to space-charge capacitance $(C_{SC})$:

$$C = C_{SC}. \tag{3}$$

On the other hand, at low frequencies, the contribution of the interface states to diode capacitance decreases toward high frequencies. Therefore, the capacitance is given by the sum of the space-charge capacitance and the interface capacitance $(C_{SS})$:

$$C = C_{SC} + C_{SS}. \tag{4}$$

The interface state density $N_{SS}$ is related to $C_{SS}$ by the following equation:[31]

$$C_{SS} = AqN_{SS}\frac{\arctan(\omega\tau)}{\omega\tau}, \tag{5}$$

where $A$ is the diode area, $\tau$ is the time constant, and $\omega$ is equal to $2\pi f$, with $f$ the frequency. Hence, fitting the experimental curve $C_{SS}$-$f$ with the previous equation can be obtained $N_{SS}$.

Figure 8 shows the interface state capacitance as a function of the frequency for all three samples. As can be seen, the sample annealed at 1150 °C for 5 min presents a higher value of $C_{SS}$ at 0.1 kHz than the sample annealed at 1200 °C for 30 s, which in turn, has a value larger than the nonannealed sample. Using Eq. (5) the following interface state densities were obtained: $6\times10^{12}$ $eV^{-1}$ $cm^{-2}$ for the nonannealed sample, $3.7\times10^{13}$ $eV^{-1}$ $cm^{-2}$ for the sample an-

nealed at 1200 °C for 30 s, and $2.4\times10^{14}$ $eV^{-1}$ $cm^{-2}$ for the sample annealed at 1150 °C for 5 min. The fact that the interface states density increases in Schottky contacts fabricated on the annealed GaN surfaces can also explain the previously observed increase of the leakage current.

However, besides the presence of interface states, it cannot be ruled out that the worse electrical behavior of the Schottky contacts upon annealing above 1100 °C is due to stoichiometric changes (nitrogen or gallium loss[16]) occurring in our GaN surface, even in the presence of a $SiO_2$ cap layer.

## IV. CONCLUSION

The influence of high temperature annealed surface on the electrical properties of Ni/GaN Schottky contacts is reported. In particular, a comparison of the surface morphology of GaN, subjected to different annealing processes, with the electrical characteristics of Ni/Au Schottky diodes fabricated on the annealed surface was reported. Although, no significant morphological changes occurred on the GaN surface upon annealing, a worsening of the electrical behavior of the Schottky barrier was observed. In particular, a reduction in barrier height, from 0.89 to 0.57 eV, and an increase in the leakage current (at −20 V), from $9.2\times10^{-4}$ to 0.42 $A/cm^2$, was observed for the sample annealed at 1150 °C for 5 min. The temperature dependence of the reverse characteristics of Schottky contacts allowed to demonstrate the predominance of one dimensional variable-range-hopping conduction when the contact is fabricated on a high temperature annealed surface. This electrical behavior was related to the formation of a high density of interface states at the metal/GaN interface.

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