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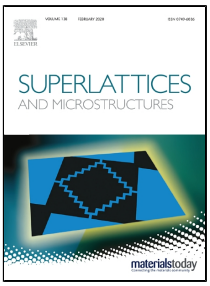

A review of the top of the barrier nanotransistor models for semiconductor nanomaterials

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A review of the top of the barrier nanotransistor models for semiconductor nanomaterials

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Abstract

The modelling and simulation of low-dimensional nanoelectronic devices is important, because the semiconductor industry has scaled transistors down to the sub-10 nm regime. The top of the barrier (ToB) transistor model has been developed and used to model transistors that are composed of various semiconducting materials. In this paper, a brief overview of the ToB transistor model is presented. The main objective of this paper is to provide a focused review on the device modelling milestones that have been achieved using the ToB transistor model. The accuracy of a few of these models is assessed by computing the normalised root mean square deviation. The ToB transistor model is widely used for computational studies on low-dimensional field-effect transistors with various channel materials, such as ultra-thin-bodies, two-dimensional materials and one-dimensional materials. The ToB transistor model is also useful for extensive research in circuit-level simulations. In summary, this nanoscale model helps researchers to identify and evaluate the potential nanomaterials for future nanoelectronic applications.

Keywords: nanoelectronics; more than Moore; ballistic transport; device modelling; top of the barrier

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1. Introduction

Advances in the semiconductor industry are governed by Moore's Law, manifesting that the number of transistors per die is doubled at a regular interval (every two years) [1], as shown in **Fig. 1**. Various strategies for the further miniaturisation of transistors are outlined in the International Roadmap for Devices and Systems (IRDS) [2]. Meanwhile, the semiconductor industry based on silicon (Si) technology achieved the 7 nm technology node in 2018, and is expected to deliver 5 nm and 3 nm technology nodes in the near future [3]. Besides the continuous scaling of the Si-based metal-oxide-semiconductor field-effect-transistors (MOSFETs), "More than Moore" devices are rigorously being researched [2, 4-6]. As a result, transistors based on other low-dimensional materials [7-9] have also been explored. These include, graphene [10-14], carbon nanotubes (CNTs) [15-20], phosphorene [21-24], silicene [25-28], transition metal dichalcogenides (TMDs) [29-35] and III-V semiconductors [36-41].

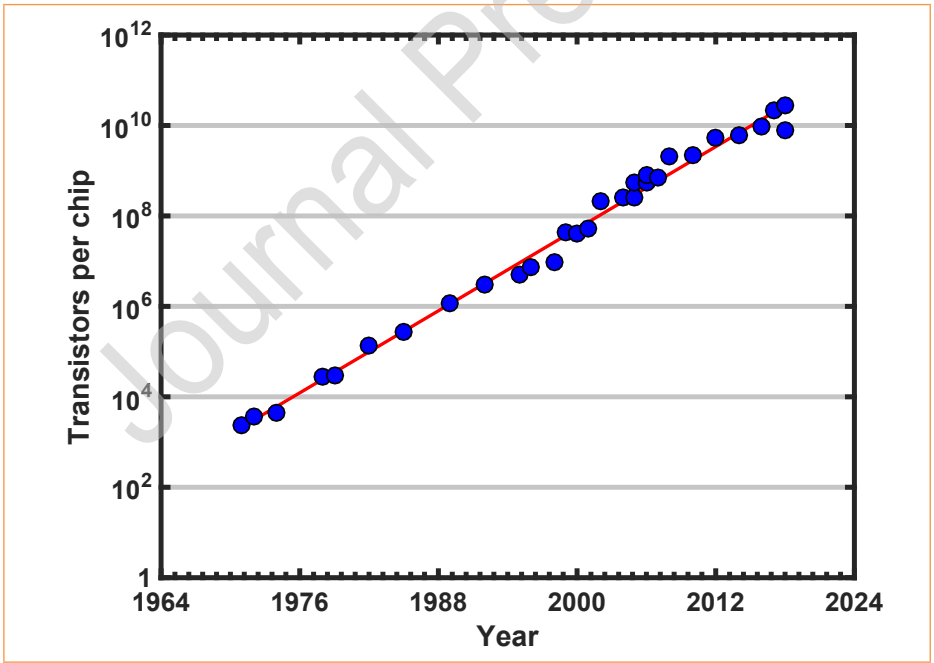


Fig. 1. The number of transistors in a microprocessor chip (or die) over the past five decades, adapted from [1].

Velocity overshoot and ballistic transport have become dominant factors in nanoscale MOSFETs [42]. In this microscopic regime, conventional drift-diffusion transistor models are no longer suitable for describing the carrier transport properties within the channel regions, where the electric field is intensively high [43]. Modelling and simulation are important to provide guidance and theoretical explanations on the operation of nanoscale MOSFETs. Thus, a compact ballistic transistor model is required to describe the essential physics behind the nanoscale MOSFETs. The ballistic nanoscale transistor model [44] was developed by A. Rahman *et al.* in 2003, which is commonly known as the top of the barrier (ToB) transistor model in the literature. The ToB transistor model can be simply solved numerically using software such as MATLAB.

There are various conventional (*e.g.* [45-48]) and recent (*e.g.* [49-57]) theoretical transistor models in the literature. The relationship between the conventional and nanoscale theoretical models of the MOSFETs have been reviewed in [42]. However, the milestones achieved for a particular theoretical model are rarely discussed. The main objective of this paper is to provide a focused review of the transistor models (with various channel materials) based on the ToB transistor model. This paper presents a brief overview of the ToB transistor model in **Section 2**. In **Section 3**, the studies that have developed various transistor models based on the ToB transistor model are systematically reviewed. Subsequently, the model comparison and conclusion are clearly described in **Sections 4** and **5** respectively.

2. Overview of the top-of-the-barrier transistor model

2.1 The ballistic MOSFETs

The ToB transistor model was developed based on the $10\ nm$ double-gate MOSFET, as shown in **Fig. 2**. An n-channel MOSFET is a three terminal (source, drain, and gate) device where the drain bias lowers the Fermi level in the drain, and the gate voltage lowers the potential energy barrier in the channel. These conditions are achieved when

the source is grounded. The energy band diagrams corresponding to variations in the drain bias and gate voltage are shown in **Fig. 3**.

The non-equilibrium Green's function (NEGF) simulation has largely contributed to the development of the ToB transistor model. The plot of the potential barrier potential versus position in the channel (**Fig. 4**) from the NEGF simulation under on-state conditions (high gate voltage and drain bias) shows that the ToB in the channel occurs closer to the source end (where the electric field is almost zero) of a ballistic MOSFET [58]. A. Rahman *et al.* showed that velocity saturation occurs in this particular region [44]. As current is the product of the charge and carrier velocity, the ToB is of great significance to the current-voltage (I-V) characteristics and device performance of a ballistic MOSFET.

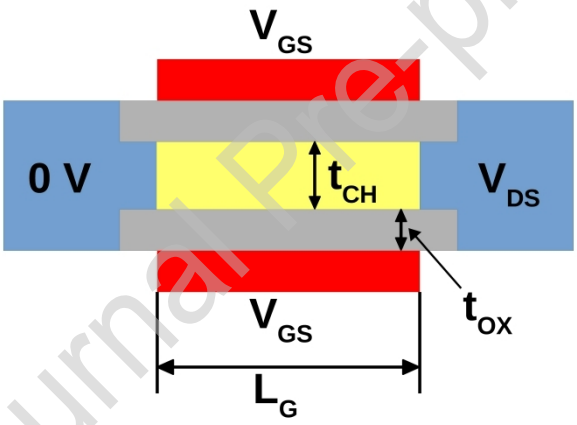
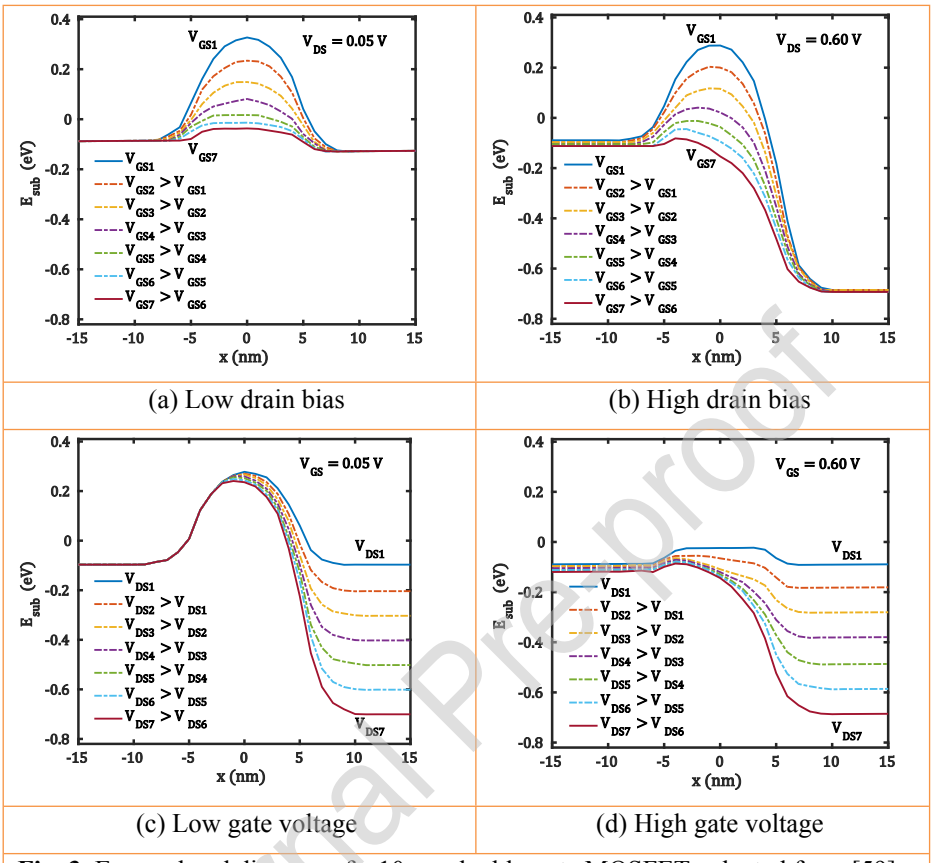


Fig. 2. Structural model of the double-gate MOSFET (n-channel), where V_{GS} is the gate voltage, V_{DS} is the drain bias, L_G is the gate length, t_{CH} is the channel thickness, and t_{OX} is the oxide thickness.



(a) Low drain bias (b) High drain bias

(c) Low gate voltage (d) High gate voltage

Fig. 3. Energy band diagram of a 10 nm double-gate MOSFET, adapted from [59].

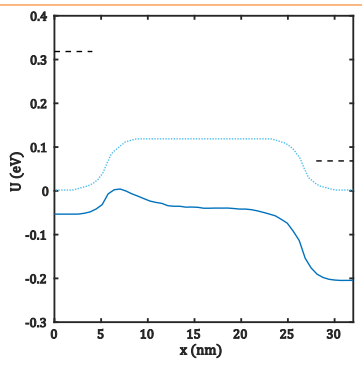
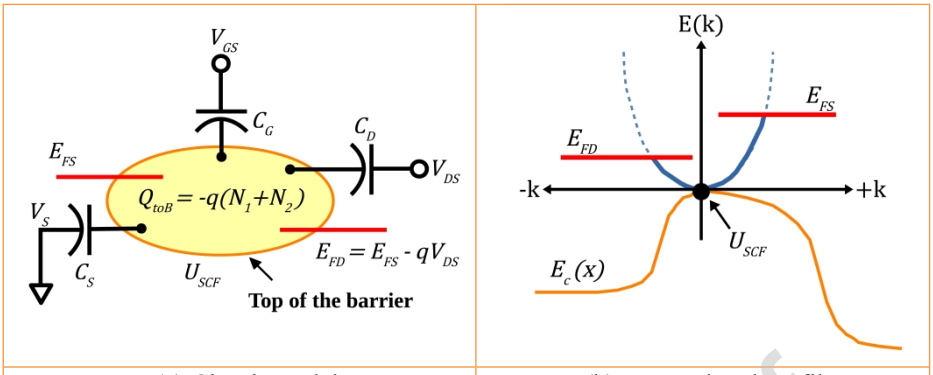


Fig. 4. The potential profile in a nanoscale device, adapted from Fig. 9A in [58].



(a) Circuit model | (b) Energy band profile

Fig. 5. Schematic diagram of the (a) circuit model of a ballistic transistor and (b) energy band profile, indicating how the states are filled at the ToB by the two Fermi levels.

2.2 The model and procedures

A simplified two-dimensional (2D) circuit model of a ballistic MOSFET is shown in **Fig. 5**(a). The gate voltage (V_{GS}) and drain bias (V_{DS}) are applied to the gate and drain terminals, respectively, while the source terminal is always grounded ($V_s = 0\ V$). The circuit model consists of three capacitors, the gate capacitor (C_G), source capacitor (C_S), and drain capacitor (C_D). The mobile charge is placed at the ToB. The local density of states (LDOS), source Fermi energy level (E_{FS}), drain Fermi energy level (E_{FD}), and self-consistent potential at the ToB (U_{SCF}) are used to determine the mobile charge. **Fig. 5**(b) depicts the filling of the electron states at the ToB by E_{FS} and E_{FD}.

The ToB includes the treatment of the quantum capacitance naturally through the self-consistent gate electrostatics (the quantum capacitance is the effective capacitance owing to the finite density of states, particularly in low-dimensional materials [60]). The equilibrium electron density at the ToB when no bias is applied is

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F)\, dE\,, \qquad (1)$$

where $D(E)$ is the LDOS and $f(E-E_F)$ is the equilibrium Fermi-Dirac function. The Fermi-Dirac function describes the probability of occupancy of each states at a given temperature, T [61], and is given by

$$f(E) = [1 + \exp(\frac{E - E_F}{k_B T})]^{-1}, \quad \textbf{(2)}$$

where k_B is the Boltzmann constant.

When the gate voltage and drain bias are applied, the positive velocity states are filled by the source according to **Eq. (3a)** and the negative velocity states are filled by the drain according to **Eq. (3b)**, creating a non-equilibrium condition. These conditions are described by

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E - U_{SCF}) f(E - E_{FS})\, dE, \quad \textbf{(3a)}$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E - U_{SCF}) f(E - E_{FD})\, dE, \quad \textbf{(3b)}$$

where $E_{FS} = E_F$ and $E_{FD} = E_F - qV_{DS}$. To simplify the numerical procedures, changes in the variables are used (*i.e.* shifting the Fermi energy instead of shifting the energy levels in the LDOS) to re-express **Eqs. (3a)** and **(3b)** as

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_S(E_S)\, dE, \quad \textbf{(4a)}$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_D(E_D)\, dE, \quad \textbf{(4b)}$$

where the source and drain Fermi functions can now be defined as

$$f_S(E_S) \equiv f(E + U_{SCF} - E_{FS}), \quad \textbf{(5a)}$$

and

$$f_D(E_D) \equiv f(E + U_{SCF} - E_{FD}), \quad \textbf{(5b)}$$

respectively. The electron density at the ToB is evaluated as $N_{ToB} = N_1 + N_2$, provided that the LDOS, $D(E)$, locations of E_{FS} and E_{FD} are defined, and U_{SCF} is known. The bias induced charge, ΔN is obtained by subtracting the equilibrium electron density, N_0 from the non-equilibrium electron density filled by the source and drain, N_{ToB}, given

by $\Delta N = (N_1 + N_2) - N_0$. The self-consistent potential is obtained by solving the Poisson equation involving the bias induced charge, ΔN due to the terminal voltages

$$U_{SCF} = -\frac{q}{C_\Sigma}(Q_t - q\Delta N)\,, \quad \textbf{(6)}$$

where q is the constant for electric charge and $C_\Sigma = C_G + C_D + C_S$ is the total capacitance. The stored charge at the terminals [62], Q_t is defined as

$$Q_t \equiv V_G C_G + V_D C_D + V_S C_S\,, \quad \textbf{(7)}$$

The two non-linear **Eqs. (4)** and **(6)** with two unknowns namely N and U_{SCF}, can be solved iteratively using numerical software such as MATLAB. After solving the unknown values, the drain current can be evaluated using Landauer-Büttiker ballistic current transport equation [44], given by

$$I_{DS} = \frac{q}{2}\int_{-\infty}^{+\infty} |v(E)|D(E)[f_S(E_S) - f_D(E_D)]dE\,, \quad \textbf{(8)}$$

where $|v(E)|$ is the average velocity. The complete procedure for computing the particular value of I_{DS} at the selected values of V_{GS} and V_{DS} is summarised in the flow chart illustrated in **Fig. 6**.

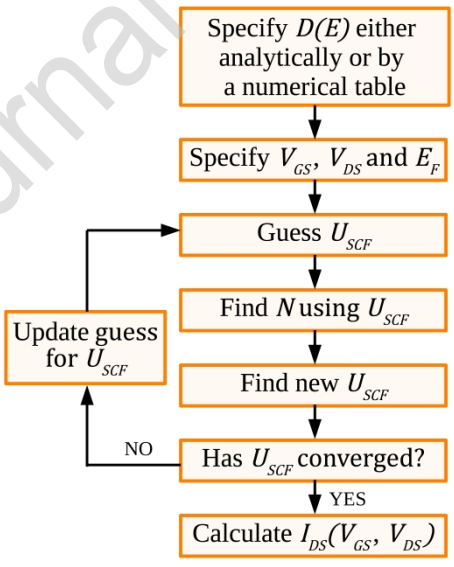


Fig. 6. The simulation flow chart for the ToB transistor model, adapted from [63].

3. The transistor models

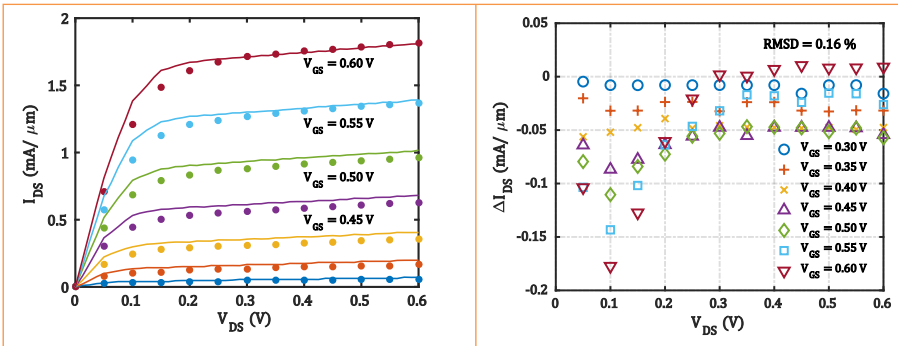
Theoretical studies are important for explaining the experimental results. In addition, they can provide a guideline and framework before the fabrication of expensive devices. In this section, previous theoretical works that have studied the ToB transistor model are reviewed. This section is divided into four subsections by classifying the type of materials, namely Si and germanium (Ge), carbon-based materials, graphene-like materials, and III-V compound semiconductors. The performance of the transistors is commonly measured using the device metrics [64] such as the threshold voltage (V_t) drain-induced barrier lowering (DIBL), subthreshold swing (SS), and on-current to off-current ratio (I_{on}/I_{off}). The performance of the published models (for a few selected works where the benchmarks of the results were available) is evaluated using the normalised root mean square deviation (RMSD) [65, 66], given as

$$RMSD = \frac{\sqrt{(\sum_{i=1}^{N}(a_i - b_i)^2)/N}}{\max(a_i,b_i) - \min(a_i,b_i)} \times 100\%, \quad (9)$$

where $\boldsymbol{N}$ is the total number of data, and $\boldsymbol{a_i}$ and $\boldsymbol{b_i}$ are the values of the $\boldsymbol{i^{th}}$ data in the compared models.

3.1 Silicon and germanium

Si and Ge are well-established semiconductors in the industry [67]. Several groups have employed the ToB transistor model to simulate Si-based [44, 68-70] and Ge-based [71] MOSFETs within the ballistic limit. Rahman *et al.* [44] demonstrated that the ToB transistor model is accurate at both the low and high gate and drain biases by comparing their results with the nanoMOS numerical simulator [72]. **Fig. 7**(a) depicts a comparison between the results of the ToB transistor model and nanoMOS simulator with the same transistor parameters (Si body thickness of $1.5\ nm$, silicon dioxide thickness of $1.5\ nm$, doping concentration of the source and drain of $10^{20}\ cm^{-3}$, and gate workfunction of $4.25\ eV$).



(a) I-V characteristics (b) RMSD

Fig. 7. Comparison between the ToB transistor model [44] and nanoMOS simulator [72]. The solid lines in (a) represent results of the ToB transistor model, while the filled dots in (a) represent the results of the nanoMOS simulator.

Complementary to the work of Rahman *et al.* [44] (which focused on the n-channel MOSFETs where electron conduction is the main concern), Ramesh *et al.* [68] discussed the application of the ToB transistor model to p-channel MOSFETs (where hole conduction is the main concern). In contrast to the energy band diagram based on the conduction band shown in **Fig. 5**(b), the ToB transistor model based on the valence band is illustrated in **Fig. 8**. Thus, the ToB transistor model is useful for simulating both the n-channel and p-channel MOSFETS and the results can be combined to form the complementary metal-oxide-semiconductor (CMOS) transistor technology [73].

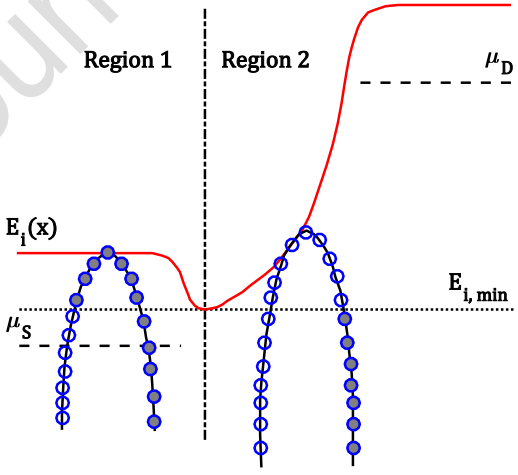
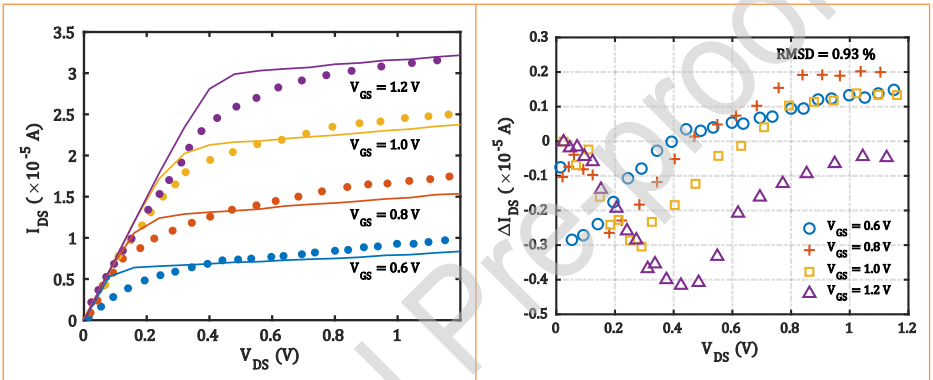


Fig. 8. The energy band profile for hole conduction (in p-channel MOSFETs) [68].

The ToB model was employed by Chin *et al.* [69] to investigate the I-V characteristics of Si nanowire FET (SiNWFET) with a nanowire diameter of $16\ nm$ and channel length of $10\ nm$. They showed that their simulation results were in agreement with the experimental results published by Li *et al.* [74], as shown in **Fig. 9**(a). The performance metrics of the simulated $10\ nm$ SiNW indicated a DIBL of $88.66\ mV/V$, SS of $88.80\ mV/dec$, and I_{on}/I_{off} of 10^4, which were all very close to the experimental measurement.



(a) I-V characteristics (b) RMSD

Fig. 9. Comparison of the I-V characteristics of SiNWFET between the ToB model [69] and experimental measurement [74]. The solid lines in (a) represent the results of the ToB transistor model, while the filled dots in (a) represent the experimental measurement.

Besides gate-controlled FET devices, Zhang *et al.* [70] used the ToB transistor model to simulated p-channel pressure-controlled (pressure sensors) SiNWFETs with various channel orientations. They investigated the SiNW orientations in [100], [110], and [111] directions. They calculated the band structure of the SiNWs using $k \cdot p$ theory. The structure of their model is shown in **Fig. 10**. Their results showed that SiNWs with different orientations possessed different hole transport effective masses (the transport effective masses are parameters obtained from the parabolic band structure assumptions [25, 67, 75]). They concluded that the orientations of the channel materials played important roles with respect to the carrier density and injection velocity, which are both affected by the hole transport effective masses.

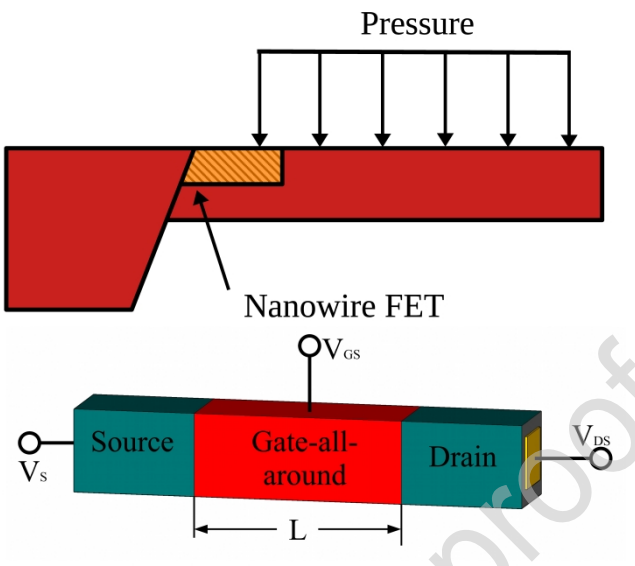


Fig. 10. Schematic diagram of the SiNWFET pressure sensor [70].

Tanaka *et al.* [71] modelled the p-channel Ge nanowire FET (GeNWFET) using the ToB transistor model. The model was modified to account for phonon and surface roughness scattering in the channel and source-to-drain direct tunnelling (quasi-ballistic hole transport regime) as shown in **Fig. 11**. In their work, the "backscattering rate" was taken into account by calculating the sum of scattering probability where the states move with negative velocity. Moreover, various orientations of GeNWs were also included in their studies. The valance band structures were calculated using $sp^3d^5s^*$ tight-binding (TB) approach with spin-orbit coupling. They concluded that GeNW with $[110]/(001)$ orientation exhibits a higher hole mobility as compared with the $[110]/(1\bar{1}0)$ orientation in the quasi-ballistic transport regime, which is consistent with previous published results [76]. The results showed that the ToB transistor model could accurately describe the MOSFETs in both the ballistic and quasi-ballistic transport regimes.

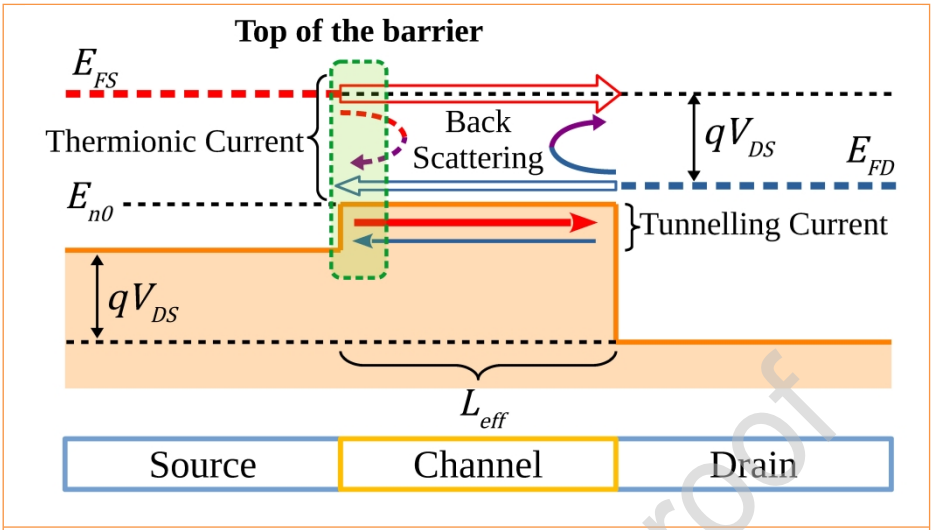


Fig. 11. Schematic diagram of the quasi-ballistic carrier transport in a GeNW p-channel MOSFET with the flat channel potential barrier approximation [71].

3.2 Graphene and carbon nanotubes

Researchers have also used the ToB transistor model to perform simulations on two carbon-based materials that were awarded the Nobel Prize: graphene [77-82] and CNTs [66, 83-87]. The success of graphene and CNTs is remarkable in the semiconductor industry. Interestingly, the CNT-based CMOS microprocessor (consisting of more than 14,000 CMOS CNTFETs) has also been successfully fabricated and programmed to run 32-bit instructions [88].

Zhao *et al.* [77] investigated the graphene nanoribbon FETs (GNRFETs) in the armchair orientations. They obtained the band structure profile using 3-nearest-neighbour TB approach. **Fig. 12** shows a comparison of the performance of the armchair GNRFETs with a width, N_A of 19 (from $N_A = 3p + 1$ GNR family) and 21 (from $N_A = 3p$ family). These GNRFETs have silicon dioxide (SiO_2) thickness of $10\,nm$. The results showed that GNRFET with $N_A = 19$ (or width of $2.21\,nm$) exhibited a higher quantum capacitance and lower on-current than the GNRFET with

$N_A = 21$ (or width of $2.46\,nm$). Moreover, the GNRFET model was extended to include the edge scattering effect, which significantly reduced the on-current.

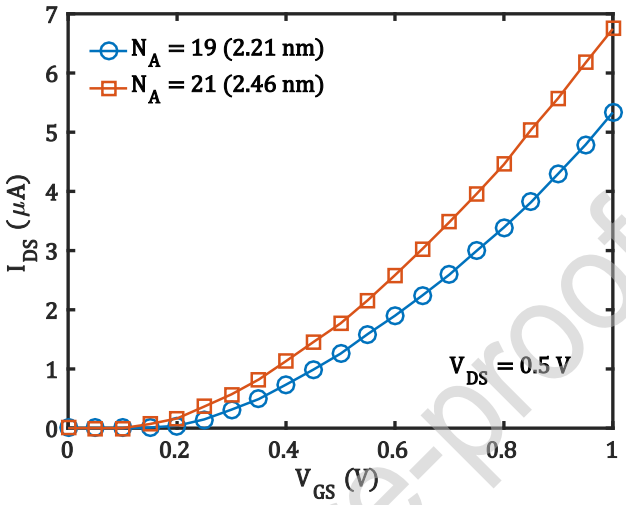


Fig. 12. Plots of the ballistic $I_{DS} - V_{GS}$ characteristics of GNRFET with $N_A = 19$ ($3p + 1$ GNR family) and $N_A = 21$ ($3p$ GNR family) [77].

Owing to the higher on-current of the $3p$ GNR family, Tsuchiya *et al.* [78] performed simulations involving GNRFET with varying $N_A = 3p$ widths. They extracted the values of the band gap and electron transport effective mass of the $3p$ GNR family using first-principle band structure calculations based on density function theory (DFT), as depicted in **Fig. 13**. They concluded that a proper selection of the GNR width is important to achieve a finite band gap and optimum switching delay. These results are consistent with the digital logic circuit level simulations of GNRFET using the combination of the ToB transistor model and spice simulation by Tan *et al.* [80], where it was found that the switching time of the GNRFET devices was lower when GNRFET widths were larger.

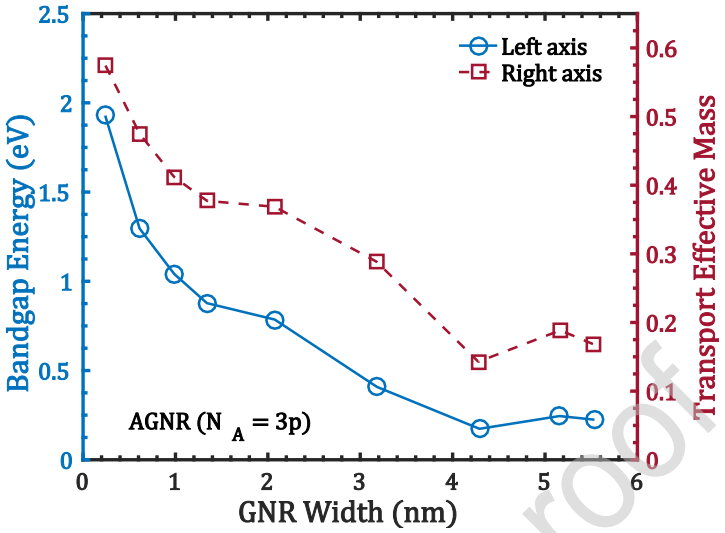
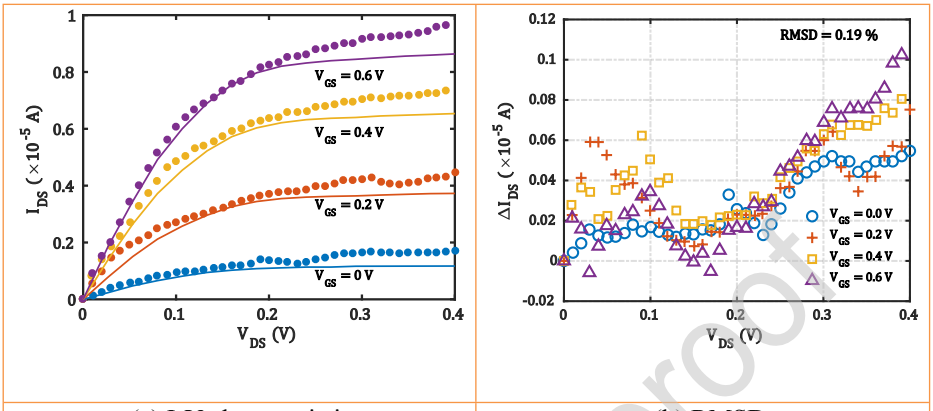


Fig. 13. Plots of the band gap and electron transport effective mass for $N_A = 3p$ GNRs [78].

Besides investigations of the pristine monolayer GNRFETs, the ToB transistor model was also used to simulate the bilayer GNRFETs [79] and non-ideal monolayer GNRFET incorporating vacancy defects [82], where both group using the TB approach to compute the band structures. They found that the band gap of the bilayer GNR is larger but significantly degrades the I-V characteristics of the GNRFETs due to the deceleration of electrons [79]. Modelling of the vacancy defect is also important, as it is an unpreventable process during fabrication [89]. Nazari *et al.* [82] reported that the introduction of 3 single vacancy (3SVs) defects to the $N_A = 12$ GNRFET improved the I-V characteristics in terms of the DIBL and SS. The improvement in DIBL ranged from $112\ mV/V$ (pristine GNRFET) to $53\ mV/V$ (3SVs GNRFET) and for SS is from $239\ mV/decade$ (pristine GNRFET) to $147\ mV/decade$ (3SVs GNRFET).

Kazmierski *et al.* [66] extended the ToB transistor model to reduce the computational cost, specifically for the CNT transistors. They compared their model with the experimental data from [90], as shown in **Fig. 14**(a). By improving the ToB transistor model, they reduced the CPU time by more than 40% for the simulation of an n-type CNT transistor at $T = 300\ K$ (with a nanotube diameter of $1.6\ nm$ and oxide thickness

of 50 nm). In addition, this model can also be used to account for the strained CNTs, tunnelling effect, and phonon scattering.

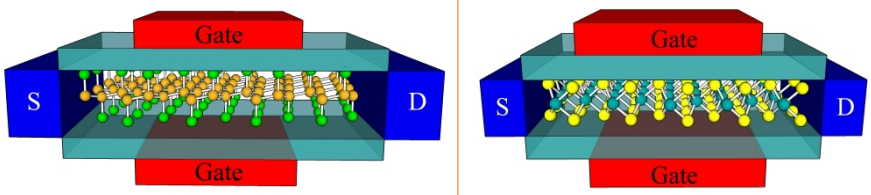


(a) I-V characteristics (b) RMSD

Fig. 14. Comparison between the simulation results [66] and experimental data [90] of a CNT transistor. The solid lines in (a) represent the results of the ToB transistor model, while the filled dots in (a) represent the experimental measurement.

3.3 Graphene-like two-dimensional materials

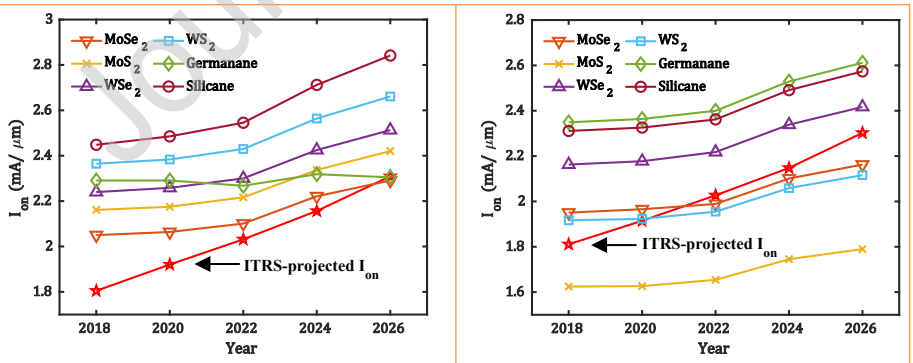
Catalysed by the rise of mechanically exfoliated graphene in 2004, many other graphene-like 2D materials (which means that the materials are in honeycomb lattice arrangements) have been rigorously explored. The 2D materials that have been commonly used as channel materials for the ToB transistor models include phosphorene [91], germanene [92, 93], silicene [92, 93], and TMDs [94-96]. Phosphorene, germanene, and silicene are monolayers of honeycomb lattices that purely consist of phosphorus (P), Ge, and Si respectively. TMDs are also denoted as MX_2, where M is a transition metal atom such as molybdenum (Mo) or tungsten (W), and X is a chalcogen atom such as sulphur (S), selenium (Se), or Tellurium (Te) [97]. **Fig. 15** illustrates examples of the double-gate MOSFETs with graphene-like materials as the conducting channels.



(a) Silicane/Germanane (b) 2D TMD

Fig. 15. Schematic structures of the double-gate graphene-like MOSFET devices (adapted from [93]).

Low *et al.* [93] performed simulations for silicane and germanane (silicane and germanane are the hydrogenated versions of silicene and germanene, respectively [98]) using the ToB transistor model. They used DFT in the general gradient approximation with the Perdew-Burke-Ernzerhof exchange-correlation function to obtain the electronic band structures of silicane and germanane. Their on-current results were compared with that of the other TMDs, and the values projected by the International Technology Roadmap for Semiconductors (ITRS 2.0) [99] are plotted in **Figs. 16**(a) and (b) for the n-channel and p-channel MOSFETs, respectively. Silicane exhibits the highest on-current for the n-channel MOSFET, while germanene exhibits the highest on-current for the p-channel MOSFET. Their results showed the prospective applications of 2D materials in the future MOSFET devices.



(a) n-channel MOSFET (b) p-channel MOSFET

Fig. 16. Assessment of the on-currents in various MOSFETs using graphene-like 2D materials as the conducting channels [93].

Hosseini *et al.* [96] performed simulations on strained-TMD MOSFETs using the ToB transistor model. The electronic band structures of the channel materials was modelled using the DFT with the local density approximation. The relationship between the strain and I_{on}/I_{off} ratio of various TMD MOSFETs is shown in **Fig. 17**. The device metrics of the MoS_2 MOSFET models of various channel lengths are compared with the first-principle calculations from [100], as shown in **Table 1**. Although the device metrics do not fit exactly to the results from the first-principle calculations, the overall trends for the first-principle calculations and ToB transistor model data are consistent. This further confirms that TMDs offer great opportunities in further nanoelectronic applications. However, the fabrication of these devices is still in the infancy stage [33].

Table 1. Comparison between the results from the first-principle calculation [100] and ToB transistor model [96] for MoS_2 at various channel lengths. The applied voltages are $V_{DS} = 0.5\ V$, $V_{GS}(off) = 0\ V$ and $V_{GS}(on) = 0.8\ V$.

Channel length (nm)	First-principle calculation [100]		ToB transistor model [96]	
	I_{on}/I_{off} ratio	SS (mV/dec)	I_{on}/I_{off} ratio	SS (mV/dec)
10	2.3×10^7	65	4.7×10^7	67
8	9.3×10^5	75	1.6×10^6	78
6	1.8×10^4	98	4×10^{-2}	102

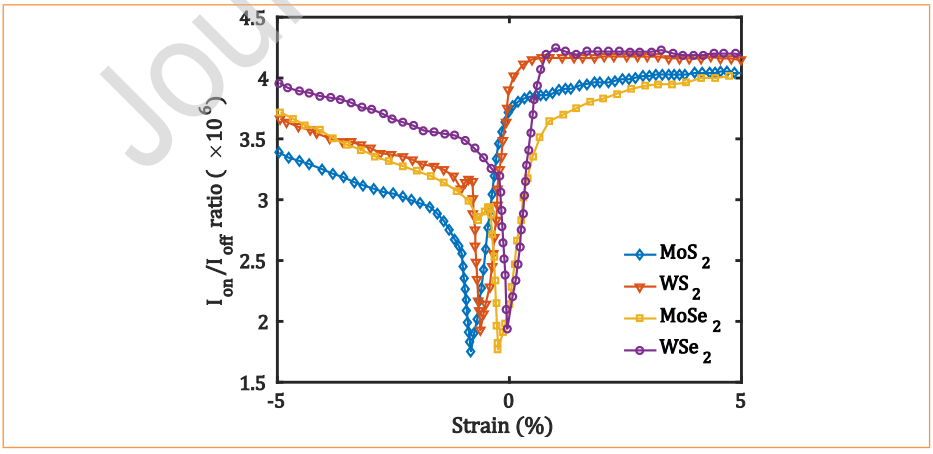
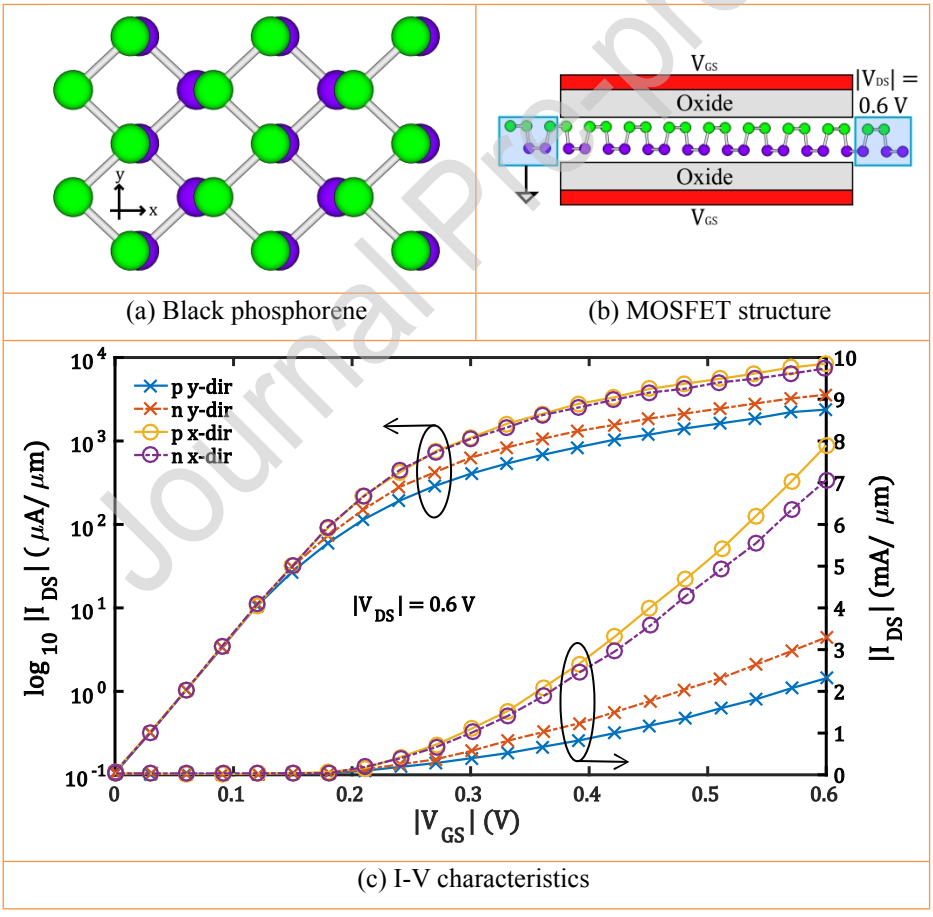


Fig. 17. The I_{on}/I_{off} ratio for various TMDs under biaxial strain at the supply voltage of 0.8 *V* [96].

Lam *et al.* [91] investigated the n-channel and p-channel monolayer black phosphorene (BP) FETs in both the x- and y-directions, as shown in **Figs. 18**(a) and (b). The atomic structure of BP was modelled using DFT implemented in Vienna Ab initio Simulation Package (VASP). The results for the monolayer BP FET are plotted in **Fig. 18**(c). It can be observed that the monolayer BP in the x-direction (or "armchair" edge) exhibits a higher on-current than that in the y-direction (or "zigzag" edge) due to a higher DOS and higher injection velocity. Moreover, they concluded that the proposed BP FET models outperformed both the n-channel and p-channel FETs with MoS_2 and Si as the conducting channels.



(a) Black phosphorene

(b) MOSFET structure

(c) I-V characteristics

Fig. 18. The I-V characteristics of the monolayer black phosphorene (BP) MOSFET shown using the linear and logarithmic scales on the same plot [91].

3.4 III-V compound semiconductors

The III-V compound semiconductors have been applied in different devices according to their energy gap, as shown in **Fig. 19**. The compound semiconductors shown in **Fig. 19** include aluminium phosphide (AlP), aluminium arsenide (AlAs), gallium phosphide (GaP), gallium arsenide (GaAs), indium gallium arsenide (InGaAs), indium phosphide (InP), aluminium antimonide (AlSb), gallium antimonide (GaSb), indium arsenide (InAs), and indium antimonide (InSb). The common types of transistors using these materials are high-electron-mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) [101]. The ToB transistor model has also been used to simulate various transistors [102-108] with III-V compound semiconductors as the conducting channels.

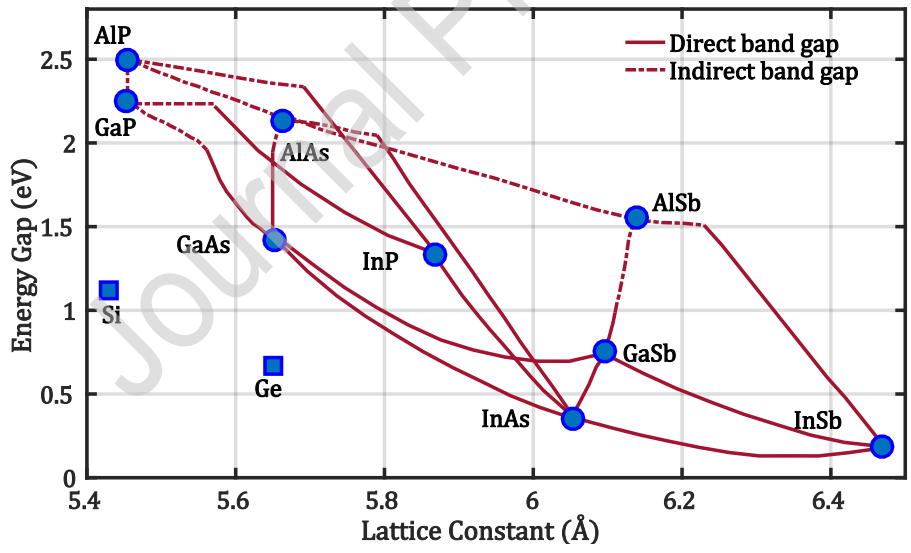


Fig. 19. The band gap and wavelength versus the lattice constant for common III-V compound semiconductors [101].

The ToB transistor model was applied to simulate ultra-thin-body (UTB) III-V p-channel MOSFETs by Chang et *al.* [108]. They obtained the valence band structures for all the materials using the $k \cdot p$ method. They solved the eight-band strain-dependent $k \cdot p$ Schrödinger and Poisson equations self-consistently. Via the simulation, they found that the effective oxide thickness (EOT) for the classical capacitance limits is $0.5\ nm$, and the I-V transfer characteristics are essentially affected by the transport effective masses of the conducting channels. The transport effective masses depend on several factors such as the type of materials, transport directions, and strain effects. Their results also showed that the on-current is enhanced by the lower transport effective mass. The I-V transfer characteristics within the ballistic transport regime of various p-channel MOSFETs with group IV and III-V conducting channels (with a body thickness of $4\ nm$, EOT of $0.5\ nm$, and drain bias of $-0.5\ V$) are shown in **Fig. 20**.

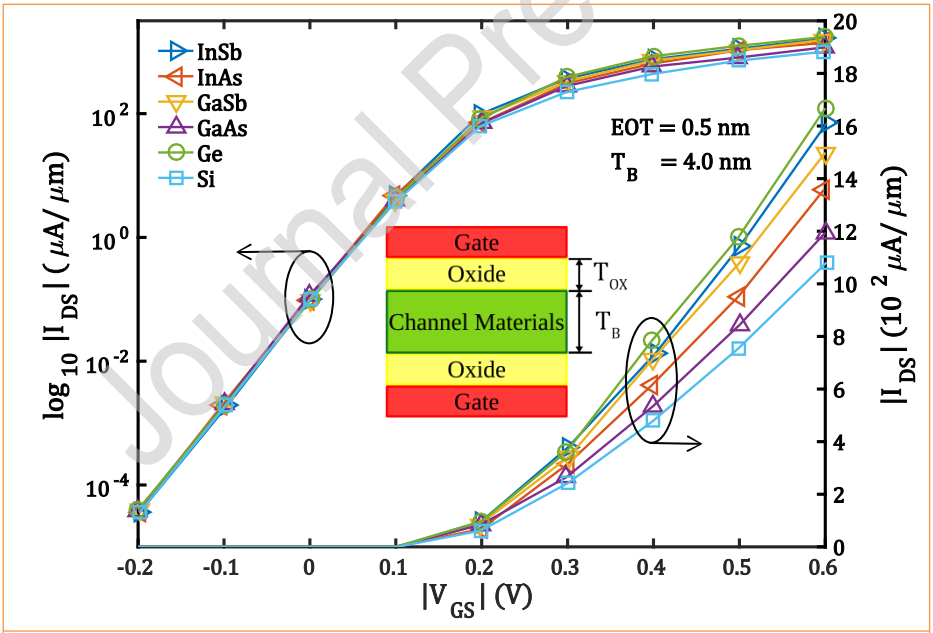


Fig. 20. The I-V transfer characteristics of ultra-thin-body (UTB) p-channel MOSFETs with various group IV and III-V conducting channels within the ballistic transport regime [108].

4. Model comparison

We can observe rom **Section 3** that the ToB transistor model has been applied to simulate various low-dimensional materials at the device level including UTB bulk materials, 2D materials, and one-dimensional (1D) materials. **Table 2** summarises the RMSD calculations from the simulation results obtained by Rahman *et al.* [44], Chin *et al.* [69], and Kazmierski *et al.* [66], as depicted in **Figs. 7**(b), **9**(b), and **14**(b), respectively. The ToB transistor models produce a higher normalised RMSD percentage when they are benchmarked with the experimental data. Overall, the RMSD percentage is close to zero. Thus, this indicates that the ToB transistor model can produce accurate results. In addition, this model is simple and easy to use because it requires the user to specify only the DOS of the semiconductor either analytically or by a numerical table. The DOS can be derived from the band structure of a semiconductor using various nanotechnology computational modelling approaches such as the ab initio, semi-empirical, and atomistic methods [109].

Table 2. The benchmarks of the ToB transistor model based on the RMSD calculations.

Ref.	Research group	Benchmark	Material	RMSD
[44]	Rahman *et al.*	NanoMos Simulator [72]	Bulk Si	0.16 %
[69]	Chin *et al.*	Experiment [74]	SiNW	0.93 %
[66]	Kazmierski *et al.*	Experiment [90]	CNT	0.19 %

The device metrics of the ToB transistor models with various channel materials are summarised in **Table 3**. The t_{CH} parameter represents the channel thickness for the bulk materials and nanowire diameter of the nanowire materials. Furthermore, t_{CH} is not available for all monolayer 2D materials. The device metrics were extracted from the published models, and all unavailable data are marked with a dash (-). From **Table 3**, we can observe that most of the published works have computed the I_{on}/I_{off} ratio to evaluate the performance of the FET models. It is recommended that the other device metrics should also be extracted to obtain further insights on the performance of the FETs.

Among all the materials summarised in **Table 3**, MoS_2 with a gate length of $10\ nm$ exhibits the highest I_{on}/I_{off} ratio up to the order of 7 (from [96]), while GaAs UTB with a gate length of $10\ nm$ exhibits the lowest I_{on}/I_{off} ratio only up to 9.0×10^3. In contrast, opportunities remain for applying the ToB transistor model to other graphene-like 2D materials such as silicene [4] and boron nitride [110, 111], because there is a minimal amount of similar work available in the literature. In term of the SS (the typical value is $\geq 60\ mV/dec$ [112]), MoS_2 FET performs better than SiNW, GNR, and CNT FETs.

Table 3. Performance of the ToB transistor model for different materials.

Ref.	Device parameters (refer to **Fig. 2**)				Device metrics			
	Channel material	t_{OX} (nm)	L_G (nm)	t_{CH} (nm)	V_t (V)	SS (mV/dec)	DIBL (mV/V)	I_{on}/I_{off} ratio
[69]	SiNW	2.5	10.0	16.0	-	88.8	88.7	1.0×10^4
[78]	GNR	1.5	10.0	-	-	-	-	$\sim 3.0 \times 10^4$
[81]	GNR	1.5	10.0	-	0.40	~ 83.9	~ 51.1	$\sim 4.5 \times 10^4$
[82]	3SVs GNR	1.0	15.0	-	-	147.0	53.0	-
[87]	CNT	1.1	60.0	1.5	-	74.4	39.4	9.2×10^3
[91]	Phosphorene	3.0	20.0	-	0.20	-	-	$\sim 1.0 \times 10^4$
[96]	MoS_2	3.0	10.0	-	0.50	67.0	-	4.7×10^7
[108]	GaAs	0.5	10.0	4.0	0.23	-	-	$\sim 9.0 \times 10^3$
[108]	GaSb	0.5	10.0	4.0	0.21	-	-	$\sim 11.0 \times 10^3$
[108]	InAs	0.5	10.0	4.0	0.24	-	-	$\sim 10.0 \times 10^3$
[108]	InSb	0.5	10.0	4.0	0.22	-	-	$\sim 12.0 \times 10^3$

5. Conclusion

The demand for low-dimensional materials is rapidly growing, particularly in the semiconductor industry where transistor sizes are in the sub-$10\ nm$ regime. In summary, an overview of the ToB transistor model and its applications were reviewed in this paper. The ToB transistor model is simple and easy to use. We showed that the model is relatively accurate via RMSD calculations. In addition, the model shows good

agreement with the data from the theoretical simulations and experimental measurements. The ToB transistor model, which incorporates various low-dimensional channel materials, was also summarised and discussed. The modelling and simulation of low-dimensional electronic devices for nanoelectronic applications is important to predict their performance and understand the essential physics behind the devices. The results from the device level models can be further explored and applied in circuit-level simulation.

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References

[1] M.M. Waldrop, More than Moore, Nature, 530 (2016) 144-148. https://doi.org/10.1038/530144a

[2] IEEE, International Roadmap for Devices and Systems (IRDS). https://irds.ieee.org/, 2018. (Accessed 28 August 2019).

[3] D. Akinwande, C. Huyghebaert, C.-H. Wang, M.I. Serna, S. Goossens, L.-J. Li, H.-S.P. Wong, F.H. Koppens, Graphene and two-dimensional materials for silicon technology, Nature, 573 (2019) 507-518. https://doi.org/10.1038/s41586-019-1573-9

[4] M.W. Chuan, K.L. Wong, A. Hamzah, S. Rusli, N.E. Alias, C.S. Lim, M.L.P. Tan, 2D Honeycomb Silicon: A Review on Theoretical Advances for Silicene Field-Effect Transistors, Current Nanoscience, In Press (2019). https://doi.org/10.2174/1573413715666190709120019

[5] P. Ye, T. Ernst, M.V. Khare, The last silicon transistor: Nanosheet devices could be the final evolutionary step for Moore's Law, IEEE Spectrum, 56 (2019) 30-35. https://doi.org/10.1109/MSPEC.2019.8784120

[6] F. Najam, K.C. Lau, C.S. Lim, Y.S. Yu, M.L.P. Tan, Metal oxide-graphene field-effect transistor: interface trap density extraction model, Beilstein journal of nanotechnology, 7 (2016) 1368-1376. https://doi.org/10.3762/bjnano.7.128
[7] M. Chhowalla, D. Jena, H. Zhang, Two-dimensional semiconductors for transistors, Nature Reviews Materials, 1 (2016) 16052. https://doi.org/10.1038/natrevmats.2016.52
[8] S. Balendhran, S. Walia, H. Nili, S. Sriram, M. Bhaskaran, Elemental analogues of graphene: silicene, germanene, stanene, and phosphorene, Small, 11 (2015) 640-652. https://doi.org/10.1002/smll.201402041
[9] A. Molle, J. Goldberger, M. Houssa, Y. Xu, S.-C. Zhang, D. Akinwande, Buckled two-dimensional Xene sheets, Nature materials, 16 (2017) 163. https://doi.org/10.1038/nmat4802
[10] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, A.A. Firsov, Electric field effect in atomically thin carbon films, Science, 306 (2004) 666-669. https://doi.org/10.1126/science.1102896
[11] F. Salimian, D. Dideban, Comparative study of nanoribbon field effect transistors based on silicene and graphene, Mater. Sci. Semicond. Process., 93 (2019) 92-98. https://doi.org/10.1016/j.mssp.2018.12.032
[12] H. Mohamadpour, A. Asgari, Graphene nanoribbon tunneling field effect transistors, Physica E: Low-dimensional Systems and Nanostructures, 46 (2012) 270-273. https://doi.org/10.1016/j.physe.2012.09.021
[13] S.-M. Lee, J.-H. Kim, J.-H. Ahn, Graphene as a flexible electronic material: mechanical limitations by defect formation and efforts to overcome, Mater. Today, 18 (2015) 336-344. https://doi.org/10.1016/j.mattod.2015.01.017
[14] V.K. Arora, A. Bhattacharyya, Unified bandgap engineering of graphene nanoribbons, Physica status solidi (b), 251 (2014) 2257-2264. https://doi.org/10.1002/pssb.201451005
[15] X. Yang, J. Ni, Electronic properties of single-walled silicon nanotubes compared to carbon nanotubes, Physical Review B, 72 (2005) 195426. https://doi.org/10.1103/PhysRevB.72.195426
[16] S. Iijima, T. Ichihashi, Single-shell carbon nanotubes of 1-nm diameter, Nature, 363 (1993) 603. https://doi.org/10.1038/363603a0
[17] M.K.Q. Jooq, A. Mir, S. Mirzakuchaki, A. Farmani, Semi-analytical modeling of high performance nano-scale complementary logic gates utilizing ballistic carbon nanotube transistors, Physica E: Low-dimensional Systems and Nanostructures, 104 (2018) 286-296. https://doi.org/10.1016/j.physe.2018.08.008
[18] H.C. Chin, A. Bhattacharyya, V.K. Arora, Extraction of nanoelectronic parameters from quantum conductance in a carbon nanotube, Carbon, 76 (2014) 451-454. https://doi.org/10.1016/j.carbon.2014.04.055
[19] M.T. Ahmadi, R. Ismail, M.L. Tan, V.K. Arora, The ultimate ballistic drift velocity in carbon nanotubes, Journal of Nanomaterials, 2008 (2008). https://doi.org/10.1155/2008/769250
[20] E. Shahrom, S.A. Hosseini, A new low power multiplexer based ternary multiplier using CNTFETs, AEU-International Journal of Electronics and Communications, 93 (2018) 191-207. https://doi.org/10.1016/j.aeue.2018.06.011

[21] A. Carvalho, M. Wang, X. Zhu, A.S. Rodin, H. Su, A.H.C. Neto, Phosphorene: from theory to applications, Nature Reviews Materials, 1 (2016) 16061. https://doi.org/10.1038/natrevmats.2016.61
[22] H. Sarvari, C. Liu, A.H. Ghayour, P. Shenavar, Z. Chen, R. Ghayour, Atomistic quantum transport simulation of multilayer phosphorene nanoribbon field effect transistors, Physica E: Low-dimensional Systems and Nanostructures, 91 (2017) 161-168. https://doi.org/10.1016/j.physe.2017.04.015
[23] M.G. Menezes, R.B. Capaz, Tight binding parametrization of few-layer black phosphorus from first-principles calculations, Computational Materials Science, 143 (2018) 411-417. https://doi.org/10.1016/j.commatsci.2017.11.039
[24] H.V. Phuc, N.N. Hieu, V.V. Ilyasov, L.T. Phuong, C.V. Nguyen, First principles study of the electronic properties and band gap modulation of two-dimensional phosphorene monolayer: Effect of strain engineering, Superlattices Microstruct., 118 (2018) 289-297. https://doi.org/10.1016/j.spmi.2018.04.018
[25] M.W. Chuan, K.L. Wong, A. Hamzah, S. Rusli, N.E. Alias, C.S. Lim, M.L.P. Tan, Electronic properties and carrier transport properties of low-dimensional aluminium doped silicene nanostructure, Physica E: Low-dimensional Systems and Nanostructures, 116 (2020) 113731. https://doi.org/10.1016/j.physe.2019.113731
[26] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, D. Akinwande, Silicene field-effect transistors operating at room temperature, Nature nanotechnology, 10 (2015) 227. https://doi.org/10.1038/NNANO.2014.325
[27] J. Zhao, H. Liu, Z. Yu, R. Quhe, S. Zhou, Y. Wang, C.C. Liu, H. Zhong, N. Han, J. Lu, Rise of silicene: A competitive 2D material, Prog. Mater Sci., 83 (2016) 24-151. https://doi.org/10.1016/j.pmatsci.2016.04.001
[28] Y.-C. Fan, T.-H. Fang, T.-H. Chen, Stress waves and characteristics of zigzag and armchair silicene nanoribbons, Nanomaterials, 6 (2016) 120. https://doi.org/10.3390/nano6070120
[29] Q. Luan, C.-L. Yang, M.-S. Wang, X.-G. Ma, First-principles study on the electronic and optical properties of WS2 and MoS2 monolayers, Chinese Journal of Physics, 55 (2017) 1930-1937. https://doi.org/10.1016/j.cjph.2017.08.011
[30] H.S. Lee, S. Park, J.Y. Lim, S. Yu, J. Ahn, D.K. Hwang, Y. Sim, J.H. Lee, M.J. Seong, S. Oh, Impact of H-Doping on n-Type TMD Channels for Low-Temperature Band-Like Transport, Small, 15 (2019) 1901793. https://doi.org/10.1002/smll.201901793
[31] J. Dong, Y. Zhao, G. Ouyang, The effect of alloying on the band engineering of two-dimensional transition metal dichalcogenides, Physica E: Low-dimensional Systems and Nanostructures, 105 (2019) 90-96. https://doi.org/10.1016/j.physe.2018.08.025
[32] O.V. Yazyev, A. Kis, MoS2 and semiconductors in the flatland, Mater. Today, 18 (2015) 20-30. https://doi.org/10.1016/j.mattod.2014.07.005
[33] Q.H. Wang, K. Kalantar-Zadeh, A. Kis, J.N. Coleman, M.S. Strano, Electronics and optoelectronics of two-dimensional transition metal dichalcogenides, Nature nanotechnology, 7 (2012) 699. https://doi.org/10.1038/NNANO.2012.193

[34] F. Najam, M.L.P. Tan, R. Ismail, Y.S. Yu, Two-dimensional (2D) transition metal dichalcogenide semiconductor field-effect transistors: the interface trap density extraction and compact model, Semicond. Sci. Technol., 30 (2015) 075010. https://doi.org/10.1088/0268-1242/30/7/075010
[35] B. Wei, C. Lu, Transition metal dichalcogenide MoS2 field-effect transistors for analog circuits: A simulation study, AEU-International Journal of Electronics and Communications, 88 (2018) 110-119. https://doi.org/10.1016/j.aeue.2018.02.025
[36] Z. Ahangari, Performance investigation of a semi-junctionless type II heterojunction tunnel field effect transistor in nanoscale regime, Micro & Nano Letters, 13 (2018) 1165-1169. https://doi.org/10.1049/mnl.2017.0877
[37] P. Aguirre, M. Rau, A. Schenk, 2D and 3D TCAD simulation of III-V channel FETs at the end of scaling, Solid·State Electron., 159 (2019) 123-128. https://doi.org/10.1016/j.sse.2019.03.043
[38] C. Navarro, S. Karg, C. Marquez, S. Navarro, C. Convertino, C. Zota, L. Czornomaz, F. Gamiz, Capacitor-less dynamic random access memory based on a III–V transistor with a gate length of 14 nm, Nature Electronics, 2 (2019) 412-419. https://doi.org/10.1038/s41928-019-0282-6
[39] J.A. Del Alamo, Nanometre-scale electronics with III–V compound semiconductors, Nature, 479 (2011) 317. https://doi.org/10.1038/nature10677
[40] F. Gao, S.C. Tan, J.A. del Alamo, C.V. Thompson, T. Palacios, Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaN/GaN HEMTs, IEEE Trans. Electron Devices, 61 (2013) 437-444. https://doi.org/10.1109/TED.2013.2293114
[41] A. Issaoun, A.B. Kouki, F.M. Ghannouchi, A simple large signal model for III–V HBT devices exceeding VBIC performances, AEU-International Journal of Electronics and Communications, 60 (2006) 367-375. https://doi.org/10.1016/j.aeue.2005.05.017
[42] M.S. Lundstrom, D.A. Antoniadis, Compact models and the physics of nanoscale FETs, IEEE Trans. Electron Devices, 61 (2014) 225-233. https://doi.org/10.1109/TED.2013.2283253
[43] K. Natori, Ballistic metal-oxide-semiconductor field effect transistor, J. Appl. Phys., 76 (1994) 4879-4890. https://doi.org/10.1063/1.357263
[44] A. Rahman, J. Guo, S. Datta, M.S. Lundstrom, Theory of ballistic nanotransistors, IEEE Trans. Electron Devices, 50 (2003) 1853-1864. https://doi.org/10.1109/TED.2003.815366
[45] H.K.J. Ihantola, J. Moll, Design theory of a surface field-effect transistor, Solid·State Electron., 7 (1964) 423-430. https://doi.org/10.1016/0038-1101(64)90039-5
[46] H.C. Pao, C.-T. Sah, Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors, Solid·State Electron., 9 (1966) 927-937. https://doi.org/10.1016/0038-1101(66)90068-2
[47] J.R. Brews, A charge-sheet model of the MOSFET, Solid·State Electron., 21 (1978) 345-355. https://doi.org/10.1016/0038-1101(78)90264-2
[48] B.J. Sheu, D.L. Scharfetter, P.-K. Ko, M.-C. Jeng, BSIM: Berkeley short-channel IGFET model for MOS transistors, IEEE Journal of Solid-State Circuits, 22 (1987) 558-566. https://doi.org/10.1109/JSSC.1987.1052773

[49] C.C. Enz, F. Krummenacher, E.A. Vittoz, An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications, Analog integrated circuits and signal processing, 8 (1995) 83-114. https://doi.org/10.1007/BF01239381
[50] M. Chan, K.Y. Hui, C. Hu, P.K. Ko, A robust and physical BSIM3 non-quasi-static transient and AC small-signal model for circuit simulation, IEEE Trans. Electron Devices, 45 (1998) 834-841. https://doi.org/10.1109/16.662788
[51] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. Van Langevelde, G.D. Smit, A.J. Scholten, D.B. Klaassen, PSP: An advanced surface-potential-based MOSFET model for circuit simulation, IEEE Trans. Electron Devices, 53 (2006) 1979-1993. https://doi.org/10.1109/TED.2005.881006
[52] Y. Taur, T.H. Ning, Fundamentals of modern VLSI devices, Cambridge university press, 2013. https://doi.org/10.1017/CBO9781139195065
[53] Y. Tsividis, C. McAndrew, Operation and modeling of the MOS transistor, Oxford Univ. Press, New York, 2011. https://books.google.com.my/books?id=oYmYPwAACAAJ
[54] M. Miura-Mattausch, H. Ueno, M. Tanaka, H. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, N. Nakayama, HiSIM: A MOSFET model for circuit simulation connecting circuit performance with technology, in: Digest. International Electron Devices Meeting, IEEE, 2002, pp. 109-112. https://doi.org/10.1109/IEDM.2002.1175790
[55] D. Klaassen, A unified mobility model for device simulation—I. Model equations and concentration dependence, Solid·State Electron., 35 (1992) 953-959. https://doi.org/10.1016/0038-1101(92)90325-7
[56] V.K. Arora, M.L. Tan, I. Saad, R. Ismail, Ballistic quantum transport in a nanoscale metal-oxide-semiconductor field effect transistor, Appl. Phys. Lett., 91 (2007) 103510. https://doi.org/10.1063/1.2780058
[57] B. Buvaneswari, N. Balamurugan, 2D analytical modeling and simulation of dual material DG MOSFET for biosensing application, AEU-International Journal of Electronics and Communications, 99 (2019) 193-200. https://doi.org/10.1016/j.aeue.2018.11.039
[58] S. Datta, Nanoscale device modeling: the Green's function method, Superlattices Microstruct., 28 (2000) 253-278. https://doi.org/10.1006/spmi.2000.0920
[59] M. Lundstrom, Z. Ren, Essential physics of carrier transport in nanoscale MOSFETs, IEEE Trans. Electron Devices, 49 (2002) 133-141. https://doi.org/10.1109/16.974760
[60] P.R. Bandaru, H. Yamada, R. Narayanan, M. Hoefer, The role of defects and dimensionality in influencing the charge, capacitance, and energy storage of graphene and 2D materials, Nanotechnology Reviews, 6 (2017) 421-433. https://doi.org/10.1515/ntrev-2016-0099
[61] M. Lundstrom, C. Jeong, Near-Equilibrium Transport: Fundamentals and Applications, World Scientific Publishing Company, 2013. https://doi.org/10.1142/7975
[62] T.J. Kazmierski, D. Zhou, B.M. Al-Hashimi, A fast, numerical circuit-level model of carbon nanotube transistor, in: 2007 IEEE International Symposium on Nanoscale Architectures, IEEE, 2007, pp. 33-37. https://doi.org/10.1109/NANOARCH.2007.4400855

[63] D. Supriyo, Lessons From Nanoelectronics: A New Perspective On Transport - Part A: Basic Concepts, World Scientific, 2017. https://doi.org/10.1142/10440
[64] M. Lundstrom, J. Guo, Nanoscale transistors: device physics, modeling and simulation, Springer Science & Business Media, 2006. https://doi.org/10.1007/0-387-28003-0
[65] T. Chai, R.R. Draxler, Root mean square error (RMSE) or mean absolute error (MAE)?–Arguments against avoiding RMSE in the literature, Geoscientific model development, 7 (2014) 1247-1250. https://doi.org/10.5194/gmd-7-1247-2014
[66] T.J. Kazmierski, D. Zhou, B.M. Al-Hashimi, P. Ashburn, Numerically efficient modeling of CNT transistors with ballistic and nonballistic effects for circuit simulation, IEEE Transactions on Nanotechnology, 9 (2009) 99-107. https://doi.org/10.1109/TNANO.2009.2017019
[67] D.A. Neamen, Semiconductor physics and devices: basic principles, New York, NY: McGraw-Hill, 2012. http://refhub.elsevier.com/S1386-9477(18)30117-6/sref48
[68] R. Venugopal, Z. Ren, M.S. Lundstrom, Simulating quantum transport in nanoscale MOSFETs: Ballistic hole transport, subband engineering and boundary conditions, IEEE Transactions on Nanotechnology, 2 (2003) 135-143. https://doi.org/10.1109/TNANO.2003.817229
[69] H.C. Chin, C.S. Lim, M.L.P. Tan, Phonon scattering effects in drain-current model of carbon nanotube and silicon nanowire field-effect transistors, Science of Advanced Materials, 8 (2016) 1028-1035. https://doi.org/10.1166/sam.2016.2687
[70] J.-H. Zhang, Q.-A. Huang, H. Yu, S.-Y. Lei, Orientation Effects in Ballistic High-Strained P-type Si Nanowire FETs, Sensors, 9 (2009) 2746-2759. https://doi.org/10.3390/s90402746
[71] H. Tanaka, J. Suda, T. Kimoto, Analysis of ballistic and quasi-ballistic hole transport properties in germanium nanowires based on an extended "Top of the Barrier" model, Solid-State Electron., 123 (2016) 143-149. https://doi.org/10.1016/j.sse.2016.04.015
[72] Z. Ren, R. Venugopal, S. Goasguen, S. Datta, M.S. Lundstrom, nanoMOS 2.5: A two-dimensional simulator for quantum transport in double-gate MOSFETs, IEEE Trans. Electron Devices, 50 (2003) 1914-1925. https://doi.org/10.1109/TED.2003.816524
[73] A.V. Krishnamoorthy, D.A. Miller, Scaling optoelectronic-VLSI circuits into the 21st century: a technology roadmap, IEEE Journal of selected topics in quantum electronics, 2 (1996) 55-76. https://doi.org/10.1109/2944.541875
[74] M. Li, K.H. Yeo, S.D. Suk, Y.Y. Yeoh, D.-W. Kim, T.Y. Chung, K.S. Oh, W.-S. Lee, Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate, in: 2009 Symposium on VLSI Technology, IEEE, 2009, pp. 94-95. https://ieeexplore.ieee.org/document/5200646
[75] V.K. Arora, Nanoelectronics: Quantum engineering of low-dimensional nanoensembles, CRC Press, 2015. https://doi.org/10.1201/b18131
[76] H. Tanaka, S. Mori, N. Morioka, J. Suda, T. Kimoto, Geometrical and band-structure effects on phonon-limited hole mobility in rectangular cross-sectional

germanium nanowires, J. Appl. Phys., 116 (2014) 235701. https://doi.org/10.1063/1.4904844
[77] P. Zhao, M. Choudhury, K. Mohanram, J. Guo, Computational model of edge effects in graphene nanoribbon transistors, Nano Research, 1 (2008) 395-402. https://doi.org/10.1007/s12274-008-8039-y
[78] H. Tsuchiya, H. Ando, S. Sawamoto, T. Maegawa, T. Hara, H. Yao, M. Ogawa, Comparisons of performance potentials of silicon nanowire and graphene nanoribbon MOSFETs considering first-principles bandstructure effects, IEEE Trans. Electron Devices, 57 (2010) 406-414. https://doi.org/10.1109/TED.2009.2037365
[79] R. Sako, H. Tsuchiya, M. Ogawa, Influence of band-gap opening on ballistic electron transport in bilayer graphene and graphene nanoribbon FETs, IEEE Trans. Electron Devices, 58 (2011) 3300-3306. https://doi.org/10.1109/TED.2011.2161992
[80] M.L.P. Tan, H.C. Chin, L.L. Lim, W.S. Wong, E.L.M. Su, C.F. Yeong, Nanoscale device modeling and circuit-level performance projection of top-gated graphene nanoribbon field-effect transistor for digital logic gates, Science of Advanced Materials, 6 (2014) 569-576. https://doi.org/10.1166/sam.2014.1778
[81] M.A. Eshkalak, R. Faez, S. Haji-Nasiri, A novel graphene nanoribbon field effect transistor with two different gate insulators, Physica E: Low-dimensional Systems and Nanostructures, 66 (2015) 133-139. https://doi.org/10.1016/j.physe.2014.10.021
[82] A. Nazari, R. Faez, H. Shamloo, Modeling comparison of graphene nanoribbon field effect transistors with single vacancy defect, Superlattices Microstruct., 97 (2016) 28-45. https://doi.org/10.1016/j.spmi.2016.06.008
[83] Z. Arefinia, A.A. Orouji, Investigation of the novel attributes of a carbon nanotube FET with high-κ gate dielectrics, Physica E: Low-dimensional Systems and Nanostructures, 40 (2008) 3068-3071. https://doi.org/10.1016/j.physe.2008.04.005
[84] A. Kumar, M. Husain, A. Khan, M. Husain, Effect of parametric variation on the performance of single wall carbon nanotube based field effect transistor, Physica E: Low-dimensional Systems and Nanostructures, 64 (2014) 178-182. https://doi.org/10.1016/j.physe.2014.07.018
[85] J.-M. Park, S.-N. Hong, Contact and channel resistances of ballistic and non-ballistic carbon-nanotube field-effect transistors, Journal of the Korean Physical Society, 68 (2016) 251-256. https://doi.org/10.3938/jkps.68.251
[86] S.G. Shirazi, G. Karimi, S. Mirzakuchaki, Temperature Dependence of IV Characteristics for CNT Based pin TFET and nin MOSFET, ECS Journal of Solid State Science and Technology, 5 (2016) M44-M50. https://doi.org/10.1149/2.0291606jss
[87] M.L.P. Tan, Long channel carbon nanotube as an alternative to nanoscale silicon channels in scaled MOSFETs, Journal of Nanomaterials, 2013 (2013) 162. https://doi.org/10.1155/2013/831252
[88] G. Hills, C. Lau, A. Wright, S. Fuller, M.D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, Modern microprocessor built from complementary

carbon nanotube transistors, Nature, 572 (2019) 595-602. https://doi.org/10.1038/s41586-019-1493-8
[89] S. Li, Y. Wu, Y. Tu, Y. Wang, T. Jiang, W. Liu, Y. Zhao, Defects in silicene: vacancy clusters, extended line defects, and di-adatoms, Sci. Rep., 5 (2015) 7881. https://doi.org/10.1038/srep07881
[90] A. Javey, R. Tu, D.B. Farmer, J. Guo, R.G. Gordon, H. Dai, High performance n-type carbon nanotube field-effect transistors with chemically doped contacts, Nano Lett., 5 (2005) 345-348. https://doi.org/10.1021/nl047931j
[91] K.-T. Lam, Z. Dong, J. Guo, Performance limits projection of black phosphorous field-effect transistors, IEEE Electron Device Letters, 35 (2014) 963-965. https://doi.org/10.1109/LED.2014.2333368
[92] S. Kaneko, H. Tsuchiya, Y. Kamakura, N. Mori, M. Ogawa, Theoretical performance estimation of silicene, germanene, and graphene nanoribbon field-effect transistors under ballistic transport, Applied Physics Express, 7 (2014) 035102. https://doi.org/10.7567/APEX.7.035102
[93] K.L. Low, W. Huang, Y.-C. Yeo, G. Liang, Ballistic transport performance of silicane and germanane transistors, IEEE Trans. Electron Devices, 61 (2014) 1590-1598. https://doi.org/10.1109/TED.2014.2313065
[94] S. Mohammad Tabatabaei, M. Noei, K. Khaliji, M. Pourfath, M. Fathipour, A first-principles study on the effect of biaxial strain on the ultimate performance of monolayer MoS2-based double gate field effect transistor, J. Appl. Phys., 113 (2013) 163708. https://doi.org/10.1063/1.4803032
[95] N. Harada, S. Sato, N. Yokoyama, Computational study on electrical properties of transition metal dichalcogenide field-effect transistors with strained channel, J. Appl. Phys., 115 (2014) 034505. https://doi.org/10.1063/1.4861726
[96] M. Hosseini, H. Karami, Strain effects on the DC performance of single-layer TMD-based double-gate field-effect transistors, Journal of Computational Electronics, 17 (2018) 1603-1607. https://doi.org/10.1007/s10825-018-1227-4
[97] A. Eftekhari, Tungsten dichalcogenides (WS 2, WSe 2, and WTe 2): materials chemistry and applications, Journal of Materials Chemistry A, 5 (2017) 18299-18325. https://doi.org/10.1039/C7TA04268J
[98] M. Houssa, E. Scalise, K. Sankaran, G. Pourtois, V. Afanas' Ev, A. Stesmans, Electronic properties of hydrogenated silicene and germanene, Appl. Phys. Lett., 98 (2011) 223107. https://doi.org/10.1063/1.3595682
[99] ITRS, International Technology Roadmap for Semiconductors (ITRS 2.0). http://www.itrs2.net/, 2012. (Accessed 28 August 2019).
[100] Z. Ni, M. Ye, J. Ma, Y. Wang, R. Quhe, J. Zheng, L. Dai, D. Yu, J. Shi, J. Yang, Performance Upper Limit of sub-10 nm Monolayer MoS2 Transistors, Advanced Electronic Materials, 2 (2016) 1600191. https://doi.org/10.1002/aelm.201600191
[101] B.R. Bennett, R. Magno, J.B. Boos, W. Kruppa, M.G. Ancona, Antimonide-based compound semiconductors for electronic devices: A review, Solid·State Electron., 49 (2005) 1875-1895. https://doi.org/10.1016/j.sse.2005.09.008
[102] Y. Liu, N. Neophytou, G. Klimeck, M.S. Lundstrom, Band-structure effects on the performance of III–V ultrathin-body SOI MOSFETs, IEEE Trans. Electron Devices, 55 (2008) 1116-1122. https://doi.org/10.1109/TED.2008.919290

[103] M.A. Khayer, R.K. Lake, Modeling and performance analysis of GaN nanowire field-effect transistors and band-to-band tunneling field-effect transistors, J. Appl. Phys., 108 (2010) 104503. https://doi.org/10.1063/1.3510502
[104] N. Takiguchi, S. Koba, H. Tsuchiya, M. Ogawa, Comparisons of performance potentials of Si and InAs nanowire MOSFETs under ballistic transport, IEEE Trans. Electron Devices, 59 (2011) 206-211. https://doi.org/10.1109/TED.2011.2172615
[105] K. Shimoida, Y. Yamada, H. Tsuchiya, M. Ogawa, Orientational dependence in device performances of InAs and Si nanowire MOSFETs under ballistic transport, IEEE Trans. Electron Devices, 60 (2012) 117-122. https://doi.org/10.1109/TED.2012.2228199
[106] K. Shimoida, H. Tsuchiya, Y. Kamakura, N. Mori, M. Ogawa, Performance Comparison of InAs, InSb, and GaSb n-Channel Nanowire Metal–Oxide–Semiconductor Field-Effect Transistors in the Ballistic Transport Limit, Applied Physics Express, 6 (2013) 034301. https://doi.org/10.7567/APEX.6.034301
[107] K. Jansson, E. Lind, L.-E. Wernersson, Ballistic modeling of InAs nanowire transistors, Solid·State Electron., 115 (2016) 47-53. https://doi.org/10.1016/j.sse.2015.10.009
[108] P. Chang, X. Liu, S. Di, G. Du, Evaluation of ballistic transport in III–V-based p-channel MOSFETs, IEEE Trans. Electron Devices, 64 (2017) 1053-1059. https://doi.org/10.1109/TED.2017.2655261
[109] S.M. Musa, Computational Nanotechnology: Modeling and Applications with MATLAB®, CRC Press, 2012. https://doi.org/10.1201/9781315217567
[110] W.H. Lim, A. Hamzah, M.T. Ahmadi, R. Ismail, Performance analysis of one dimensional BC2N for nanoelectronics applications, Physica E: Low-dimensional Systems and Nanostructures, 102 (2018) 33-38. https://doi.org/10.1016/j.physe.2018.04.005
[111] D. Golberg, Y. Bando, Y. Huang, T. Terao, M. Mitome, C. Tang, C. Zhi, Boron nitride nanotubes and nanosheets, ACS nano, 4 (2010) 2979-2993. https://doi.org/10.1021/nn1006495
[112] M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Company, 2017. https://doi.org/10.1142/9018

Title of manuscript: A review of the top of the barrier nanotransistor models for semiconductor nanomaterials

Highlights

- A focused review of nanotransistor model for nanoelectronics.
- Overview of the top of the barrier approach.
- The milestones of the nanotransistor model for semiconductor nanomaterials.
- Model comparison based on the benchmark and performance.