Modelling the inhomogeneous SiC Schottky interface

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(Received 17 September 2013; accepted 21 November 2013; published online 9 December 2013)

For the first time, the I-V-T dataset of a Schottky diode has been accurately modelled, parameterised, and fully fit, incorporating the effects of interface inhomogeneity, patch pinch-off and resistance, and ideality factors that are both heavily temperature and voltage dependent. A Ni/SiC Schottky diode is characterised at 2 K intervals from 20 to 320 K, which, at room temperature, displays low ideality factors ($n < 1.01$) that suggest that these diodes may be homogeneous. However, at cryogenic temperatures, excessively high ($n > 8$), voltage dependent ideality factors and evidence of the so-called "thermionic field emission effect" within a T0-plot, suggest significant inhomogeneity. Two models are used, each derived from Tung's original interactive parallel conduction treatment of barrier height inhomogeneity that can reproduce these commonly seen effects in single temperature I-V traces. The first model incorporates patch pinch-off effects and produces accurate and reliable fits above around 150 K, and at current densities lower than 10^{-5} A cm^{-2}. Outside this region, we show that resistive effects within a given patch are responsible for the excessive ideality factors, and a second simplified model incorporating these resistive effects as well as pinch-off accurately reproduces the entire temperature range. Analysis of these fitting parameters reduces confidence in those fits above 230 K, and questions are raised about the physical interpretation of the fitting parameters. Despite this, both methods used are shown to be useful tools for accurately reproducing I-V-T data over a large temperature range. © *2013 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4842096]

I. INTRODUCTION

Schottky barriers, formed at the interface between a metal and a low-doped semiconductor, are easily formed and highly prevalent, occurring in numerous electronic devices. The Schottky diode operates with very fast switching speeds and low turn-on voltages when compared to a *PiN* diode, due to its reliance only on majority carrier transport, free of the recombination mechanism. This makes the Schottky diode a popular choice in applications such as switched mode power supplies, RF, voltage clamping, and now extensively also in power electronics, where the latest silicon carbide (SiC) Schottky diodes from Cree, Inc.,[1] are capable of blocking voltages up to 1700 V. Schottky barriers also find use as the gate of high electron mobility transistors (HEMT), where one of the most popular combinations is AlGaN/GaN, with the Schottky barrier being formed to the GaN top layer,[2–4] though many other III-V combinations have been suggested.[5] Despite having been studied academically for over 70 years, a question remains open about how, on the nanometre scale, current passes through a metal-semiconductor interface, and how this then impacts on device characteristics across wide temperature and voltage ranges, and across interfaces of differing quality and uniformity.

4H-SiC is a SiC polytype of great interest for power electronics due to its wide bandgap, high thermal conductivity and high breakdown electric field. This means that compared to Si, higher power, higher switching frequencies and higher operating temperatures are achievable. SiC is also of great interest for a study such as this into metal-semiconductor inhomogeneity, with several authors having previously reported these effects.[6–23] Its inhomogeneity is likely due to the material quality, with a basal plane dislocation density typically two orders of magnitude higher than in Si, with other defects such as carrots, growth pits, and micropipes also prevalent.[6,7] Furthermore, due to the requirement for lightly doped epitaxy, any Schottky diode will be formed on material 4°–8° off the (0001) axis, leaving atomic terracing on the surface. Less specific to SiC, further sources of interfacial inhomogeneity can include processing remnants (dirt, contamination), native oxide, an uneven doping profile, crystal defects, and grain boundaries.[24–26]

We may define a "homogeneous" metal-semiconductor Schottky contact as one that behaves in an entirely predictable manner, regardless of temperature, voltage or contact area. The turn-on characteristics of a homogeneous Schottky diode can be characterised using the thermionic emission (TE) equation, which predicts that as the diode turns on, it will have a linear response on a semi-log I-V plot, with a single Schottky barrier height (SBH), Φ, and an ideality factor, n, approaching 1, with Φ and n remaining reasonably temperature and voltage independent. The TE equation[27] is

$$I = AA^{*}T^{2}\exp(-\beta\Phi)[\exp(\beta V_{A}/n) - 1], \qquad (1)$$

where A represents the contact area, A^* is the Richardson constant (146 A cm^{-2} K^{-2} for 4H-SiC), T is the temperature, V_A is the applied voltage, and $\beta = q/kT$, with q the electron charge and k the Boltzmann constant.

When the turn-on characteristics of an inhomogeneous Schottky diode are modelled using Eq. (1), many widely reported effects occur. Most common is the presence of large ideality factors, often at low temperature.[8,9,28,29] Furthermore, Φ and n are often shown to have significant temperature[10,30] or voltage dependencies.[24,25] Often reported,[6,8,11,12,30] especially at metal-SiC interfaces, are double turn on effects (double bumps) where the diode can seemingly be characterised as two diodes with parallel conduction paths, a sure sign that a single barrier height such as that in Eq. (1) cannot always hold true. A final very common sign of inhomogeneity is the variability of device characteristics from chip to chip, or even within a batch of diodes on the same chip.[6,8,31]

Over the years, several models[24,32–35] have emerged to incorporate inhomogeneity, explaining the effects of inhomogeneity. These all involve a shift in thinking away from the notion of a single homogeneous barrier Φ, across the entire area A, as in Eq. (1). Instead, these parallel conduction methods presume that multiple areas of different barrier height will exist at any interface, producing dominant areas of current conduction. These techniques will be briefly summarised in Sec. IV but it is the Tung model[24,25] that has emerged as the most complete of these methods. The Tung model not only incorporates parallel conduction methodology but also the idea that neighbouring patches of different barrier height will interact. This interaction is referred to as pinch-off, due to the way the areas of low SBH are masked by those higher barriers surrounding it. Since Tung's papers,[24,25] many authors[6,8,11,13–15,21,26,28,30,31] have cited his models in light of evidence of SBH inhomogeneity, particularly when large and temperature dependent ideality factors are present. As an analysis tool, the model has been used to provide linearity to modified Richardson plots.[13,14,21,28,29] It has also been used to recreate I-V-T responses,[13,21,26,30] though these models have often neglected the effects of resistance on areas of low SBH, while little fitting has been attempted across such a vast temperature range or at cryogenic temperatures.

In this paper, we attempt for the first time, to fully recreate and parameterise the I-V-T response of a Ni/4H-SiC Schottky diode that presents signs of inhomogeneity across a 20 K to 320 K temperature range. Over a temperature range this wide, both the cause and effect of inhomogeneity changes subtly, requiring a model as complex as Tung's to be simplified due to significant redundancy. Using two implementations of Tung's equations, we are able to reproduce the full I-V-T response for the first time. We are also able to assess the validity of each model within different temperature ranges and universally, showing the inherent temperature dependencies of the models' fitting parameters (including mean barrier height, number and distribution of patches, resistivity) and whether any physical meaning can be applied to these findings.

The choice of 4H-SiC in this particular study is due to its relative inhomogeneity and its wide bandgap, which brings on the effects of carrier freeze-out at higher temperatures than would be the case for Si. This makes it an interesting case-study for any metal-semiconductor regime, and the use of cryogenic temperatures will take the interface inhomogeneity to extreme lengths. However, of secondary interest to the reader, may well be the performance of the wide bandgap material at cryogenic temperatures, an area that has very infrequently been reported before,[36,37] despite evidence of very fast switching times and reduced parasitic effects. More widely, the use of power electronic devices at cryogenic temperatures has previously been considered[38,39] for use in space, and in the co-location of power conversion circuitry next to the superconducting field winding of a synchronous machine.

II. EXPERIMENTAL DETAILS

Mesa terminated SiC Schottky diodes with field plates were fabricated for this work. The substrate was an n-type (0001) Si face, 4° off axis, 4H-SiC wafer, purchased from Cree, Inc., with a 10 μm, lightly n-type doped (1.4×10^{15} cm^{-3}) epitaxial layer. Prior to device formation, the wafer was cleaned using a standard RCA2 clean (H_2O:HCl:H_2O_2, 5:1:1) followed by a hydrofluoric acid dip to remove any oxide formed during the RCA2 process. This cleaning process has been demonstrated[40] to be of high quality, providing minimal reverse leakage current. 2 μm thick Ni back contacts were sputtered before rapid thermal annealing (RTA) for 30 s at 800 °C in argon ambient. Ni front contacts were formed overlapping a thin oxide field-plate, then terminated using 3 μm CF_4-plasma etch to form mesa structures. The front contacts were not annealed, leaving a Ni/SiC interface, instead of a Nickel silicide interface as considered elsewhere.[41] The devices were characterised using a fully automated closed-cycle-cryostat test setup, which allowed current-voltage (I-V) measurements to be taken between 20 and 320 K at 2 K intervals.

Automated I-V characterisation and analysis were performed on the Ni/SiC Schottky diodes at 2 K intervals from 20 to 320 K and the full I-V-T results are presented in Figure 1. In Sec. III, we will analyse the I-V-T full dataset using conventional TE analysis. In Sec. IV, the Tung model is fully explained before in Secs. V and VI, we will fully reproduce the I-V-T characteristics using the Tung model without and with resistive effects.

III. CONVENTIONAL THERMIONIC EMISSION ANALYSIS

We first consider the results of conventional barrier height (Φ_{eff}) and ideality factor (n) extraction, which was performed on the I-V-T data presented in Figure 1, using the TE equation of Eq. (1). Figures 2(a) and 2(b) show the temperature dependence of these parameters, and a minima of $n < 1.01$ at 312 K with $\Phi_{eff} = 0.935$ eV, suggests a very good diode. However, with decreasing temperature, the ideality factor increases steeply and the barrier height drops. This relationship has been seen in Si,[30,35] GaN,[29,42] and GaAs[28] Schottky diodes, and at heterojunction Schottky interfaces.[26] In the specific case of a Ni/4 H-SiC interface, the exact shape of the temperature dependencies of Figures 2(a) and 2(b) has

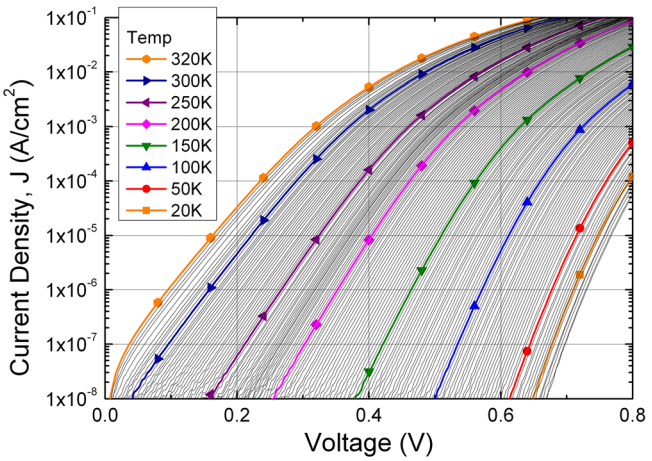

FIG. 1. The I-V-T response of the Ni/SiC Schottky diode measured at 2 K intervals from 20 to 320 K.

been seen previously.[9,10,13,14,17] It is caused by the assumption of interfacial homogeneity built into the TE equation, where the current is presumed to pass over one voltage independent barrier height that exists across the entire contact area. A barrier height that tends to 0 eV at 0 K is of course implausible, as no band alignment theory would permit this behaviour. Furthermore, the ideality factor is particularly troubling when one considers Figure 2(b) with values of $n > 5$ at temperatures of 30 K or less, confirming its status as little more than a correction factor for the homogeneity presumed in the barrier height and area.

It is possible to classify the particular form of homogeneity on display by constructing a T0 plot (nkT/q vs. kT/q), such as that shown in Figure 3(a). The solid black line is the response of a perfect diode with ($n = 1$) across the temperature range, while the shapes represent the effects of plotting the ideality factors of Figure 2(b). This is the characteristic shape[24,43] of an interface dominated by thermionic field emission (TFE). However, the diodes presented here are formed on a lightly doped (1.4×10^{15} cm^{-3}) epitaxial layer, and hence a calculation[26] of the characteristic tunneling energy E_{00}, suggests there is no chance of any actual tunneling current, even at 20 K. This same "TFE Effect" has previously been seen for another inhomogeneous Ni/SiC Schottky diode.[10]

A final consideration when applying Eq. (1) to the Ni/SiC dataset is the current density at which one chooses to take the measurement. The ideality factor of a homogeneous diode will have little reliance on voltage, indeed specific RTA of a Ni/SiC interface has been shown[41] to produce very homogeneous Ni_2Si/SiC diodes in which the extracted ideality factor varies little across the linear region, right across the temperature range. Here, the Ni/SiC diodes presented were produced without a topside anneal (though the backside was annealed to produce an ohmic contact). In Figure 3(b), for each temperature shown, the ideality factor is plotted against the current density at which it is extracted and significant curvature is shown, suggesting that the barrier height is likely to have some voltage dependence. Even the room temperature responses show some increase in ideality factor at current densities way below that which one would expect conventional ohmic effects to take place (given the large contact size and clean interfaces). All the responses display an increase in the n–J gradient suggesting that by 1 mA/cm^2, series resistance is dominant.

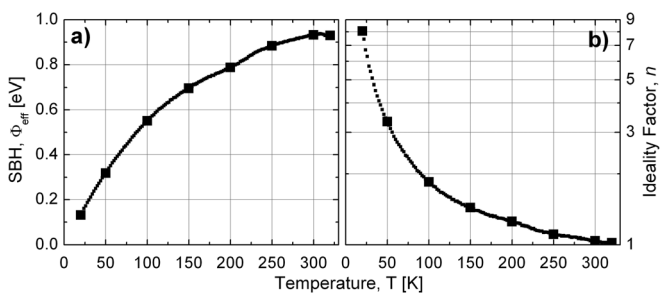

FIG. 2. Conventional barrier height and ideality factor extraction was performed on the I-V-T dataset of Figure 1. (a) and (b) show the temperature dependence of these values at a constant current density of 3×10^{-7} A cm^{-2}.

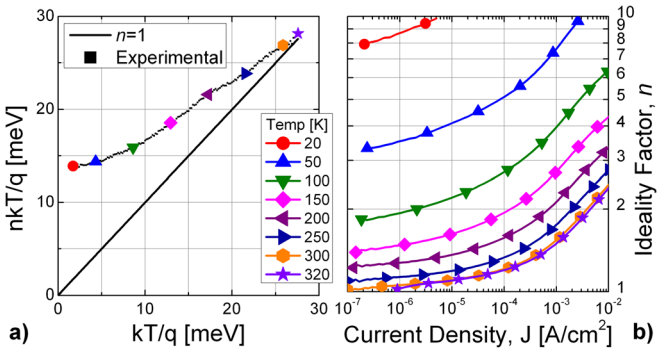

FIG. 3. (a) A T0 plot is used to classify metal-semiconductor inhomogeneity. The inverse slope of the experimental data (nkT/q) plotted against kT/q shows a TFE association, though in actuality this is not due to any tunnelling mechanism. (b) shows how the ideality factor depends on the current density at which it is measured as well as the temperature.

IV. PARALLEL CONDUCTION METHODOLOGY AND THE TUNG MODEL

Parallel conduction methodology originated from a need to explain the effects seen in Sec. III, and begun by challenging the notion that a single barrier height might exist for an entire interface. In 1980, the first parallel conduction model was proposed,[32] stating that a metal-semiconductor interface is comprised of two or more discrete barrier heights operating in parallel. It was later suggested[33] that most contacts were indeed "multiphase," causing the variations in reported barrier heights from apparently identical metal-semiconductor regimes, and in the variation from measurements techniques (i.e., where a C-V extracted SBH will always exceed that from I-V analysis). A subsequent study[34] formalised the barrier height distribution as Gaussian, before Werner and Güttler[35] first showed a quantitative link between the barrier height fluctuation and the ideality factor, whilst describing how both depended on applied voltage. This explained values of n greater than 1, and the fluctuation of n and Φ with temperature. This was not yet, however, a complete model capable of describing, or reproducing, a full I-V or I-V-T response, as they did not at the time know of the cause of

these effects, barrier height pinch-off, which Tung first described[24] in 1991. The Werner/Güttler equations remain a popular analysis tool, however, having been used for several SiC studies.[10,20,23] A more recent attempt to model SiC Schottky diodes[22] using a similar non-interacting parallel conduction model concluded that discrepancies between forward and reverse barrier heights were attributable to the absence of pinch-off effects.

Tung's papers introduced the patch pinch-off[24,25] concept, creating a new model that modified the thermionic emission equation based on the idea that neighbouring patches of different barrier height will interact. Consider the situation in the inset of Figure 4(a), where many regions of small area, or patches, exist at the interface with a barrier height Δ lower (or higher) than its neighbouring areas of average higher barrier height Φ_B^0. Figures 4(a) and 4(b), are models of the space charge region beneath the interface (after Tung[24]), showing the two different energy levels, that must meet and flatten out before reaching uniform, flat-band, bulk conditions. A low barrier height patch is considered to be pinched-off when an electron passing through the space charge region, towards the interface, must pass over a potential higher than $\Phi_B^0 - \Delta$ before it reaches the interface. The amount a patch is pinched-off varies with the size of Δ, temperature, patch size, and applied voltage. At high temperature and low voltage, pinch-off is likely to be minimal, and Werner and Güttler's non-interacting parallel conduction model holds true. However, with increasing voltage or decreasing temperature, the surrounding areas of high potential have a greater influence, leaving a potential hill, or saddle-point (ϕ) greater than $\Phi_B^0 - \Delta$ some tens of nanometres into the semiconductor. A patch parameter γ is introduced in this model ($\gamma = 3\left[\Delta R_0^2/4\right]^{1/3}$), encompassing the barrier height Δ and radius, R_0 of an individual patch. The magnitude and distribution of this parameter across the interface dictates the total distribution of patch area and barrier height.

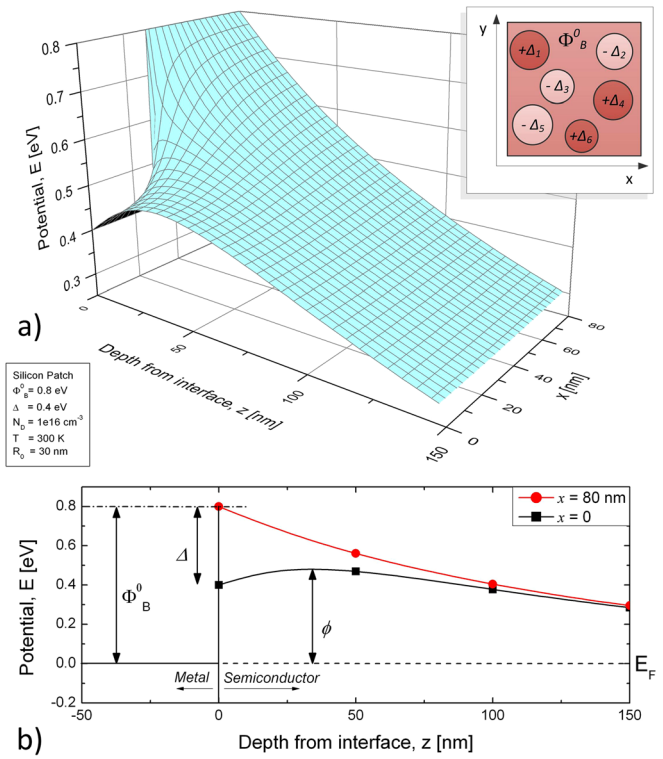

FIG. 4. (a) A 3-dimensional representation of SBH pinch off in a silicon patch. The saddle point is 30 nm into the Si from the interface. Inset: A two dimensional representation of the interface as it is modelled herein, with its patches of varying size and barrier heights. (b) Conventional band diagrams taken from the same interface, showing some of the parameters used herein.

The prospect of fully recreating and parameterising the full I-V-T response of the inhomogeneous Ni/4 H-SiC Schottky diode is a challenge due to the changing nature of the interface with temperature. Over a temperature range this wide, both the causes and effects of inhomogeneity change subtly, with localised interactions between patches the dominant mechanism at high temperature, but resistance dominant at low temperature. If one were to attempt to fit the full Tung model over this entire dataset, too many free parameters would lead to significant redundancy, and hence, we seek to simplify the model. Two implementations of Tung's equations are therefore used. The first, in Sec. V, is for temperatures above 200 K that considers only pinch-off effects of a patch. The second, in Sec. VI, is designed for lower temperatures and is a new derivation from Tung's equations that also includes resistive effects. In partnership, these two techniques are able to reproduce the full I-V-T response.

V. THE TUNG MODEL WITH PINCH-OFF EFFECTS ONLY

The high ideality factors, the TFE effect of Figure 3(a), and the ideality factor-current dependence seen in Figure 3(b), can all be explained by modelling the dataset using Tung's equations.[24,25] Most authors[6,8,11,13,15,26,28,30,31] using this model operate at non-cryogenic temperatures, and without the extreme ideality factors we have seen, and this is justifiable. At high temperatures (above around 200 K), the large number of active dopants and thermally excited carriers mean that the majority of an interface will be conducting, regardless of patch barrier height. Therefore, the effects of resistance on any given patch will be minimal as the current is well shared across the interface, and resistance can be applied globally. Under these conditions, the majority of the inhomogeneity on display, such as the slight n–J dependence below 1 mA/cm^2 in Figure 3(b), can be attributed to pinch-off, with a local voltage dependent rise in a patch's saddle point, resulting in a slight global increase in barrier height.

In our case, ignoring resistance means that the responses of 200 K or above should be well reproduced, but the large ideality factors and n–J dependence at cryogenic temperatures must be accounted for by the band bending effects of pinch-off alone, without ohmic effects. Tung's model, without considering resistance is as follows:

$$\begin{aligned} I &= A[(1-C_p)J_{\text{background}} + C_p J_{\text{patches}}] \\ &= AA^*T^2 \exp\left(-\beta\Phi_B^0\right)\left(\exp[\beta V] - 1\right) \\ &\quad \times \left\{1 - C_1 A_{\text{eff}} + C_1 A_{\text{eff}} \exp\left(\frac{\beta^2\sigma_\gamma^2 V_{bi}^{2/3}}{2\eta^{2/3}}\right)\right\}. \end{aligned} \quad (2)$$

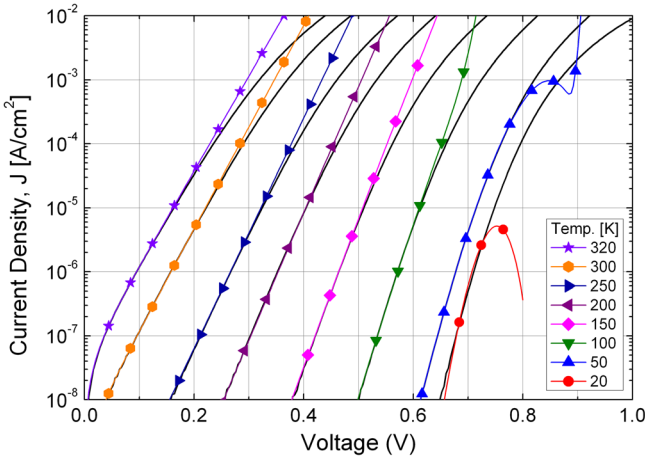

FIG. 5. (a) Results from the Tung-model fitting, without resistance effects included. The solid black lines are the results from Figure 1, the shapes are the fitting data. The dependence of this model on pinch-off effects only results in unphysical characteristics at the lowest temperatures shown.

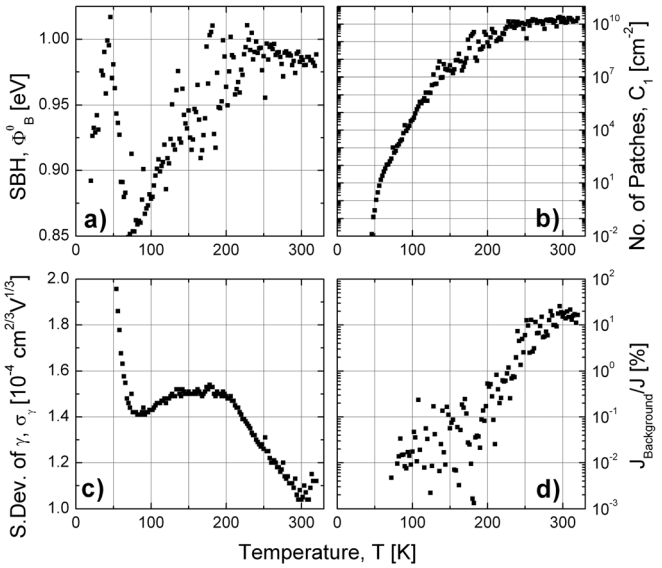

FIG. 6. (a), (b), and (c) are the fitting parameters used to fit the experimental data using pinch-off effects only, respectively, Φ^0_B, C_1, and σ_γ for the full temperature range. In (d), the percentage of the total current coming from the background current at each temperature is shown. This shows that below 230 K, more than 99% of the current is modelled as passing through a patch of lower than average SBH.

All the values are fully defined in Appendix. Equation (2) is a modified version of Tung's original as justified elsewhere.[30,31] Efforts to fit the I-V-T response of Figure 1 with Eq. (2) are shown in Figure 5. This was achieved using the exact process laid out in Ref. 30, where a least squares fitting algorithm is used to optimise the background barrier height (Φ^0_B), the number of patches (C_1) and standard deviation of patches (σ_γ) for each temperature. The best achievable fits are shown and the success of this method is in the ability to reproduce the experimental data at temperatures above 100 K and up to a current density of 10^{-5} A cm^{-2}. Within these bounds, the voltage dependence of the ideality factor (as shown in Figure 3(b)) may be accurately reproduced using just the voltage and temperature dependent patch area, A_{eff}, and barrier height. Outside of this range, at 100 K and below, and at a current density greater than 10^{-5} A cm^{-2}, it is no longer just these patch pinch-off effects that must be accounted for, but also the effects of resistance, which is not reproducible with Eq. (2). At low temperature, unrealistic, non-physical responses are the consequence of attempting to reproduce the high and extremely voltage dependent ideality factors with pinch-off effects alone.

The fitting parameters used to produce the fitting in Figure 5 are shown in Figures 6(a)–6(c), and they all follow a similar trend to that seen when this technique was applied to Si diodes with double bumps.[30] Figure 6(d) shows the contribution of the background current to the total current density, showing that at the lowest temperatures modelled, almost all of the current is passing through a patch, whereas at room temperature, as much as 25% of the total current comes from the homogeneous background current. At 230 K, the percentage coming from $J_{background}$ is around 1%. Looking at all the fitting parameters this appears to be something of a transitional temperature. Above this value, the fitting parameters are somewhat predictable; the patch density, C_1, shown in Figure 6(b), barely strays from a value of 10^{10} cm^{-2}, σ_γ in Figure 6(c) has a steady negative temperature correlation, and Φ^0_B shown in Figure 6(a) has a very slight negative temperature correlation, which, as we will see in Sec. VII B, is what Tung's fundamental theory predicts. Below 230 K, the fitting parameters can be seen to be much less predictable, and particularly difficult to justify. In particular, C_1 drops away, to values lower than 10^{-2} cm^{-2} at temperatures below 50 K, which if taken quite literally would equate to one patch conducting per 70 000 of these diodes, though greater than 99% of the current is supposed to come through such patches. Clearly, this is an extreme case highlighting flaws in a model that is missing a key component in patch resistance to operate at these low temperatures. The behaviour of both σ_γ and Φ^0_B changes drastically below 230 K, with both being affected greatly by carrier freeze-out below 80 K.

VI. THE TUNG MODEL WITH RESISTANCE AND PINCH-OFF

The reason for the poor fitting at low temperature and high current (at 100 K and below and at a current density greater than 10^{-5} A cm^{-2}) appears to stem from the effects of resistance in an interface made up of a very wide distribution of barrier heights, the result of significant interface inhomogeneity. Unlike at high temperature, as the amount of free carriers begin to reduce, the current will preferentially flow through the few barriers with the lowest barrier height, and local resistance effects become more dominant. This leads to the high and apparently voltage dependent ideality factors. Furthermore, at cryogenic temperatures, carrier freeze-out increases both series resistance and turn-on voltage, the latter meaning that a large voltage is required to raise the current to measurable values, increasing pinch-off effects, and worsening the impact of resistance.

Building resistance into the patch pinch-off model is not as simple as replacing V in Eq. (2) with (V–IR) as one would do with the Eq. (1) and as it has been implemented for other

SiC Schottky diodes using the Tung model.[14] This is because the resistance, like the barrier height will be localised, being greatest in patches that have been pinched off. Tung's review of Schottky contacts,[25] presented the following equation to take into account the increased resistive effects within pinched-off patch areas:

$$\begin{aligned} I &= \sum_{i}^{\text{“not p-o”}} I_{i,npo} + \sum_{i}^{\text{“p-o”}} I_{i,po} \\ &= A^{*}T^{2} \sum_{i}^{\text{“not p-o”}} A_i \exp(-\beta\Phi_i)\left[\exp\left(\beta V_A - \beta I_i \frac{\rho t}{A_i}\right) - 1\right] \\ &\quad + A^{*}T^{2} \sum_{i}^{\text{“p-o”}} A_{i,\text{eff}} \exp(-\beta\Phi_{i,\text{eff}}) \\ &\quad \times \left[\exp\left(\beta V_A - \beta I_i \frac{\rho}{4\sqrt{A_{i,\text{eff}}/\pi}}\right) - 1\right], \end{aligned} \tag{3}$$

where $I_{i,npo}$ is the current contribution of any non-pinched-off area, $I_{i,po}$ is from pinched-off patches, ρ is the resistivity of the material in Ω-cm, β is the inverse thermal energy q/kT, and V_A is the applied voltage. The first half of the equation, $I_{i,npo}$, is a catch-all for any interfacial area that remains mostly voltage- and temperature-independent, covering both patches that do not pinch off and the "background" current, which was represented in the first term of Eq. (2). Without pinch-off effects, the current contribution of these areas is modelled as the sum of each contact area (A_i), with a barrier height (Φ_i), limited by the conventional (V_A–IR) association with resistance, as one would expect if using Eq. (1). As such, the total resistance is made up from the resistivity ρ, the contact area, and the drift region thickness, t. The second half of the equation refers to the patches that will pinch-off, their effective area and potential barrier being linked to both temperature and voltage.

Equation (3) is difficult to meaningfully reproduce unless it is simplified, as combining a statistical array of pinched-off patches with another of non-pinched-off patches, and a background current as in Eq. (2) leaves too many unknowns and significant redundancy to solve. The priority is fitting to the temperatures below 230 K when the previous method was inconsistent, and entirely unphysical at the lowest temperatures. Hence, to simplify matters, we first choose to disregard any background current, because Figure 6(d) showed how the responses below 230 K have background contributions of less than 1%. This assumption is likely to have little effect at these low temperatures, but will increasingly add uncertainty at the highest temperatures, as the background contribution increases up towards 25% at room temperature. We also choose to disregard non-pinched-off patches. Pinch-off occurs when a patch that has a SBH of $\Phi_B^0 - \Delta$ at its interface, is surrounded by areas of greater potential. If Δ is large enough, or if significant voltage or low enough temperatures are present, then any electron approaching this patch is likely to have to overcome a potential barrier higher than that at the patch interface. As we will see in the forthcoming sections, the effects of temperature on pinch-off are very significant, suggesting that even the shallowest of patches (those with very low Δ) will suffer some pinch-off effects. Indeed, it is difficult to think of a patch not suffering some pinch-off, unless its area is significantly large, in which case one might expect the double bump phenomena to be present. Therefore, without double bumps in this response, and in line with Eq. (5), in which all the patches are presumed to pinch-off, only the second half of Eq. (3) is modelled. As such, we should be able to approximate the experimental data right across the temperature range, but especially well at the temperatures below 230 K, which is where Equation the previous method produced the least accurate fitting. We therefore rewrite Eq. (3) as follows:

$$\begin{aligned} J[V_A, T] &\approx \sum_{\gamma=0}^{\infty} J_\gamma \approx A^{*}T^{2} \sum_{\gamma=0}^{\infty} A_\gamma \exp(-\beta\Phi_\gamma) \\ &\quad \times \left[\exp\left(\beta V_A - \beta I_\gamma \frac{\rho}{4\sqrt{A_\gamma/\pi}}\right) - 1\right], \end{aligned} \tag{4}$$

where J_γ is the total current passing through patches of patch parameter γ per cm^2. The switch from current to current density (and hence area to areal density) aids the modelling of different sized contacts. γ dictates both the barrier height (Φ_γ) and areal density (A_γ) of an individual patch as follows:

$$\begin{aligned} A_\gamma &= P(\gamma) C_T A_{\text{eff}} \\ &= P(\gamma) C_T \frac{4\pi\gamma}{3\beta}\left(\frac{\eta}{V_{bi}}\right)^{2/3}, \end{aligned} \tag{5}$$

$$\Phi_\gamma = \Phi_B^0 - \gamma\left(\frac{V_{bi}}{\eta}\right)^{1/3}. \tag{6}$$

Note that both Φ_γ and A_γ are affected by applied voltage through the built-in potential (V_{bi}), and by temperature via the inverse thermal energy (β) and in η ($\eta = \epsilon_s/qn_{no}$) due to the carrier freeze-out of free carriers n_{no}. The total patch density is C_T (cm^{-2}) and the γ distribution $P(\gamma)$ throughout these patches is presumed to be Gaussian with a standard deviation (σ_γ), such that

$$P(\gamma) = \frac{d}{\sigma_\gamma\sqrt{2\pi}} \exp\left(-\frac{\gamma^2}{2\sigma_\gamma^2}\right), \tag{7}$$

where d is the practical sample width of the Gaussian that ensures that $\int_{\gamma=0}^{\infty} P(\gamma) = 0.5$ (representing one half of the Gaussian distribution, as patches of barrier height greater than the average are ignored).

Equation (4) can be used to reproduce the experimental I-V-T data given the optimisation of four parameters: Φ_B^0, C_T, ρ, and σ_γ. To achieve this, Eq. (7) first needs to be discretised, and Figure 7 shows the methodology used here to achieve this. The continuous function is sampled at widths of $d = 6 \times 10^{-6}$ cm$^{2/3}$ V$^{1/3}$ up to a limit of $\gamma = 3 \times 10^{-3}$ cm$^{2/3}$ V$^{1/3}$, a value large enough that the patch's tiny areal density A_γ will not contribute any significant current. In Figure 7, we can see a sampled distribution of 1×10^6 patches, with the σ_γ used for the 100 K plot we will see below. The inset shows how statistically insignificant the patches at the top end of our γ distribution are. For each of these discrete gamma values, a total interfacial patch density A_γ and a barrier height is acquired from Eqs. (5) and (6),

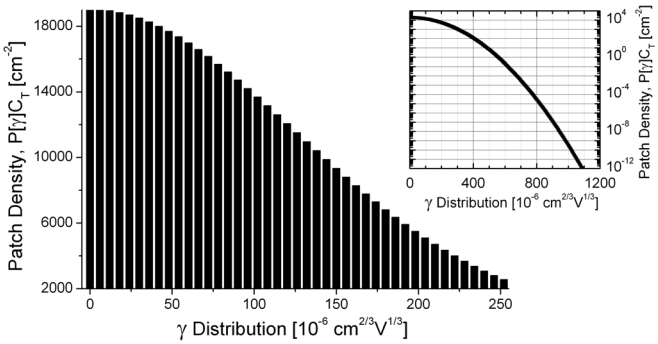

FIG. 7. The patches at an inhomogeneous interface are presumed to have a Gaussian distribution of the patch parameter, γ, as dictated by Eq. (7). Displayed is the half of the patch parameter distribution ($P[\gamma] \times C_T$ vs γ) that is responsible for patches of low barrier height (positive values of γ), as modelled in the 100 K fit, with $\sigma_\gamma = 1.257 \times 10^{-4}\,\mathrm{cm}^{2/3}\,\mathrm{V}^{1/3}$, the sample width, $d = 6 \times 10^{-6}\,\mathrm{cm}^{2/3}\,\mathrm{V}^{1/3}$, and the total number of patches $C_T = 1 \times 10^6\,\mathrm{cm}^{-2}$. In the inset, this same distribution is continued to extreme values of γ, where the contribution from these patches becomes insignificant.

before the patch current density, J_γ is calculated and summed in Eq. (4) to produce the total current passing through patches at this interface.

As with the fitting parameters used in the previous model, non-varying, temperature independent fitting parameters were not possible, so a least squares algorithm[30] was employed to find the combination of the parameters which best match with the experimental data. Unfortunately, Φ_B^0 and C_T, perform very similar roles as they both directly influence the saturation current, though C_T also influences the resistive part of the response. In order to separate these values, it was first assumed, like elsewhere,[13] that the value of C_T should not vary with temperature, unlike the mean background barrier height, which is influenced by Fermi level and bandgap dependencies. Following several simulations, a fixed value of $C_T = 1 \times 10^6\,\mathrm{cm}^{-2}$ was chosen. This value was found to give the most accurate fits over the entire temperature range given its subtle influence on resistance. Furthermore, this value was found to represent a total patch area $\left(\sum_{\gamma=0}^{\infty} A_\gamma\right)$ of between 5%–10% of the total contact area, a value that is of a similar magnitude to other studies.[13,26]

Figure 8 shows the fitting of the IV data at three temperatures 100, 200, and 300 K using Eq. (4) and fitting parameters we will refer to later. Shown in the Figure are the contributions from the patches at the interface with seven discrete patch parameter, γ, values shown. Their summation, along with all the other discrete γ values not shown, results in the total patch current shown. At 100 K, the combined effect of series resistance on the patches can be observed. At the lowest current shown, the patches with the largest γ dominate, due to their reduced barrier height Φ_γ and large individual patch area, A_γ. However, $P(\gamma)$ dictates that there are very few of these patches and hence with limited total area, the amount of current they can carry soon becomes limited by series resistance. With these patches saturated, the patches with the next largest γ become dominant, until these suffer similarly, and so on. Under this regime, we can observe how these patches are responsible for the curvature

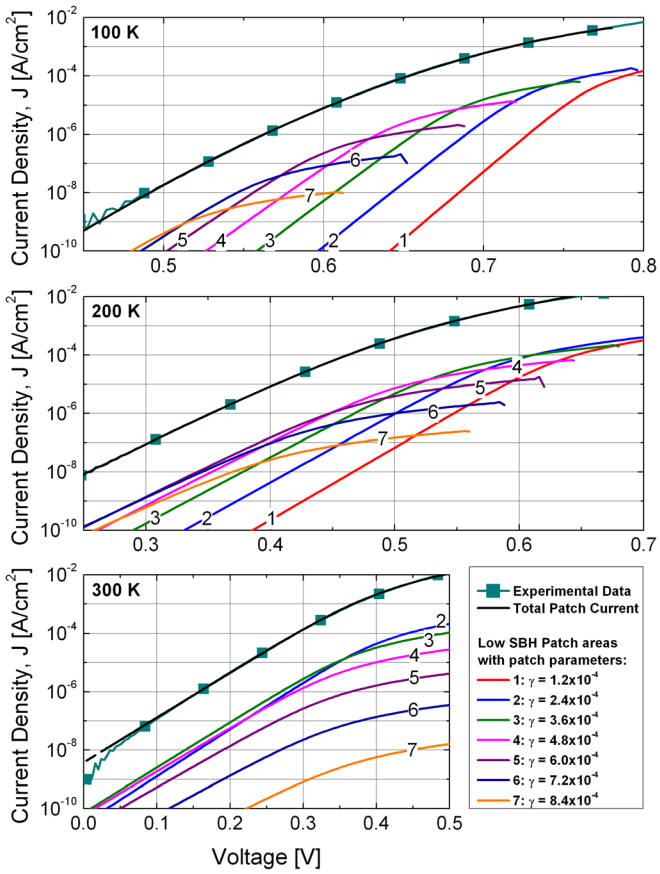

FIG. 8. The 100, 200, and 300 K experimental I-V plots from Figure 1, with fitting to this data performed by the simulated Tung model of Eq. (4). The numbered solid lines are the current contributions from patches with the discrete γ values listed in $\mathrm{cm}^{2/3}\ \mathrm{V}^{1/3}$. For all three fits, $C_T = 10^6\,\mathrm{cm}^{-2}$, $d = 6 \times 10^{-6}\,\mathrm{cm}^{2/3}\,\mathrm{V}^{1/3}$. ρ, σ_γ, and Φ_B^0 are individually fit at each temperature.

of the 100 K plot of Figure 8, a response with a large ideality factor that increases with current from $n = 2$ at a current density of 1 μA/cm^2 to $n > 4$ at 100 μA/cm^2. Both the magnitude of n and this current dependence are the net result of the continuously saturating patches, rather than the voltage-dependent pinch-off effects of the collective patches. Therefore, at low temperature, the reproduction of these responses is heavily influenced by the resistivity of the layer-ρ in Eq. (4).

At the higher temperatures of 200 and 300 K, these same resistive effects occur but at increasingly large current, as patches with much lower γ and hence much greater area are dominant. The resistive effects are still fairly evident in the 200 K plot, and can just be seen in the 300 K plot as patch areas 2 and 3 overlap at around $1 \times 10^{-5}\,\mathrm{A\ cm}^{-2}$. However, before this occurs, we can observe in the 300 K plot that patch area 3 is largely dominant for around 5 decades of current density. Therefore, the slight n–J dependence witnessed at these higher temperatures in Figure 3(b), below around $1 \times 10^{-5}\,\mathrm{A\ cm}^{-2}$ is dictated by the voltage-dependent pinch-off of these specific dominant patches, and is much reduced compared to those extracted at low temperature. At these higher temperatures, the transition between a pinch-off regime and one in which resistance is dominant in a given I-V plot, is suggested in Figure 3(b), where the 300 K

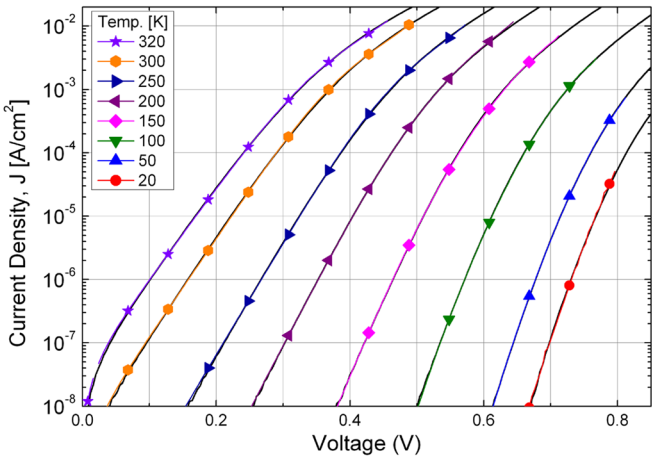

FIG. 9. Results from the Tung-model fitting with resistance effects included. The solid black lines are the results from Figure 1, the shapes are the fitting data.

ideality factor appears to rise sharply at around 10^{-4} A cm^{-2}. This appears to be the case for all the *n–J* responses at temperatures of 200 K or more.

Figure 9 shows the selected results of fitting to the Ni/SiC I-V-T results using Eq. (4) over the full temperature range and Figure 10 shows the fitting parameters that were used at every temperature interval. Visually, one can confirm that a good reproduction has been achieved across the full temperature and current range. The model has succeeded in reproducing the patch pinch-off effects as the previous model did. However, it has also succeeded in reproducing the experimental data outside this region above 1×10^{-5} A cm^{-2} and at the temperatures below 150 K, where local resistive effects dominate. The model has a maximum voltage limit of 0.8 V above which it cannot operate as V_{bi} tends to 0 and an imposed limit was to exclude any part of a response

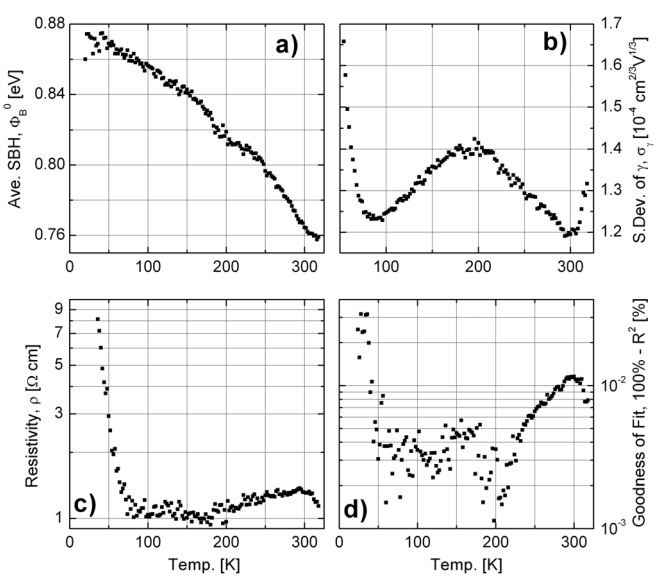

FIG. 10. The fitting parameters of (a) Φ_B^0, (b) σ_γ, and (c) ρ used within the Tung model of Eq. (4) with resistive effects included, to achieve the best possible reproduction of the experimental results. (d) shows the quality of fit, R^2 values better than 99.99% achieved between 50 and 280 K.

where $n > 10$, with the presumption that this was well into the region where conventional ohmic effects could be fit. The least squares output, the goodness of fit statistics, shown in Figure 10(d) confirms that a faithful reproduction has occurred across the temperature range, a value of $R^2 > 99.99\%$ having been achieved at most temperatures.

Just as the fitting and interpretation of the non-resistive method began to worsen below 150 K, the resistive model suffers similarly above around 230 K. Despite the appearance of good fits at the higher temperatures, the quality of the fits shown in Figure 10(d) can be seen to worsen and the fitting parameters, especially σ_γ appear to buck the trend of those from 100 to 200 K. As indicated earlier, the contribution of the background current ($J_{\text{background}}$) to the total current in Eq. (2), begins to become more significant at temperatures of 230 K and greater, rising from 1% to around 25% at 320 K. As this model considers only the pinched-off patch current, this increased error and reduced confidence in the result is to be expected.

With this specific Ni/SiC Schottky diode the value of 1% background current at 230 K represents an approximate transition between the modelling methods, a point above which the so-called background current cannot be ignored but below which the resistive effects of pinched-off patches must be considered. Of course this is quite an arbitrary threshold and in both regimes the fitting around these values remain more than adequate despite the change that begins to occur in the two sets of fitting parameters. Data from another Ni/SiC diode of this same batch but with a smaller contact area also showed a deterioration in the fitting at 230 K and confirmed the trends seen in Figure 10. However, fitting data from other Schottky datasets are required to confirm whether this transition occurs universally.

VII. THE FITTING PARAMETERS OF THE RESISTIVE MODEL AND THEIR TEMPERATURE DEPENDENCE

Figures 10(a)–10(c) shows the fitting parameters of Φ_B^0, ρ, and σ_γ used to create the fitting shown in 9, and over the full temperature range at 2 K intervals. We will address each of these and try to interpret any physical meaning or trends from them.

A. Series resistance and temperature

In Figure 10(c), the resistivity values are too low to be considered true physical values. N-type semiconductor resistivity may be approximated by

$$\rho = (q n_{no} \mu_n)^{-1}, \tag{8}$$

where n_{no} is the number of active, free carriers and μ_n is the electron mobility. At 300 K, the resistivity fitting parameter ρ is 1.3 Ω cm, but according to Eq. (8), the drift region of the SiC diode alone (ignoring possible contact resistance) would, in an ideal case, have a resistivity $\rho \approx 5$ Ωcm. Despite this, the relative shape of the response is as one might expect given the temperature dependencies of n_{no} and μ_n. At temperatures of approximately 80 K and above, all the dopant electrons are activated and in the conduction band, and hence n_{no}

remains stable at $n_{no} \approx N_D = 1.4 \times 10^{15}\,\mathrm{cm}^{-3}$. Therefore, ρ has a slight positive correlation with T due to the negative temperature dependence of the carrier mobility,[27] μ_n. Below 77 K, carrier freeze-out occurs, the thermal energy being too low to sustain even the dopant electrons and hence n_{no} decreases exponentially. This causes ρ to reach nearly 100 Ω cm at 20 K. Carrier freeze-out has a significant effect on the model, as n_{no} is a key parameter affecting η and V_{bi}.

B. Mean barrier height and temperature

In Figure 10(a), a negative correlation exists between the mean barrier height and the temperature across the full temperature range. This remains unaffected by carrier freeze-out, unlike the other two parameters. The negative correlation is well explained by the temperature dependence of the patch pinch-off effect, which occurs when an electron passing through the semiconductor towards the interface, must pass over a potential hill, or saddle point, higher than the barrier height of a patch at the interface, defined as $\Phi_B^0 - \Delta$. The potential along the z-axis from the centre of a circular patch is given by[24]

$$V(0,z) = V_{bi}\left(1 - \frac{z}{W}\right)^2 + V_n + V_A - \Delta\left(1 - \frac{z}{\left[z^2 + R_0^2\right]^{1/2}}\right), \quad (9)$$

and incidentally, was used to produce the profiles shown in Figure 4. W is the depletion width, which gets much wider during carrier freeze-out, Δ is the potential difference between Φ_B^0 and the patch barrier height, and R_0 is the radius of the patch. Tung showed[24] that a decrease in R_0 or an increase in applied voltage (V_A) will increase the saddle point, thus increasing pinch-off effects. He also stated that the effects vastly increase at lower doping, at carrier freeze-out in our case. Figure 11(a) shows the effects of temperature, which has a big impact on the saddle point and the pinch-off effects, largely due to the effects of carrier freeze-out on the depletion width. Figure 11(a) shows this relationship, for a single patch imagined to sit 0.4 eV below the surrounding area of uniform 1 eV barrier height. This

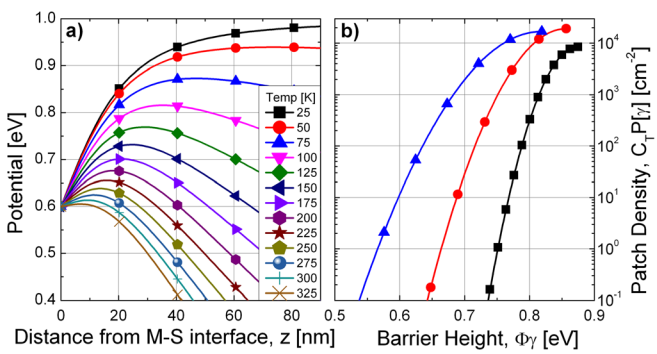

FIG. 11. (a) A simulation of patch pinch-off, the saddle point increasing as temperature drops. The simulation parameters are $R_0 = 25$ nm, $\Phi_B^0 = 1$ eV, $\Delta = 0.4$ eV, and $V_A = 0$ V, (b) the density of patches ($P(\gamma)C_T$) plotted against Φ_γ for the γ distribution of four temperatures, all taken at 10 μA/cm^2.

Figure demonstrates the same barrier height-temperature relationship as that in Figure 10(a), where lowering the temperature increases pinch-off effects, so globally increasing the average barrier height.

C. Standard deviation of the patch parameter and temperature

In Figure 10(b), the temperature dependency of σ_γ is shown. Minima at 80 and 300 K surround a peak at 200 K, while below 80 K, the effects of carrier freeze-out are extreme, with σ_γ increasing exponentially to a value of $2 \times 10^{-3}\,\mathrm{cm}^{2/3}\,\mathrm{V}^{1/3}$ at 20 K. Of most interest here is the positive correlation between temperature and σ_γ in the region of relative stability between 80 and 200 K (above freeze-out but below the temperature at which background current will skew these results). This positive correlation agrees with the simple model introduced in Figure 11(a), where the effects of pinch-off will effectively homogenise the interface, narrowing the distribution of barrier heights as those patches with entirely different values of Δ will all tend to Φ_B^0. This can be seen in Figure 11(b) where, at a nominal current density of 10 μA/cm^2, the barrier height distribution is shown increasing but narrowing with decreasing temperature.

Below 80 K, the number of free carriers, n_{no}, drops exponentially causing an increase in η ($\eta = \epsilon_s/qn_{no}$). From Eq. (6), this means that even a patch with a very large patch parameter, γ, will result in a very small Δ. The net result is that σ_γ exponentially increases below 80 K to maintain a barrier height distribution. However, it is unlikely that there is a physical reason for this exponential increase in the patch parameter, rather that such freeze out effects are not adequately compensated for in the model. Despite this, the net result, seen in Figure 11(b), is an interface that continues to show the effects of pinch-off, the narrowing and increasing distribution from 100 K down to 40 K meaning that the barrier energies are becoming more homogeneous.

VIII. FURTHER STATISTICS AND MODEL OVERVIEW

Figure 11(b) portrays well the distribution of barrier energies amongst the patches. However, from the simulation data such as that in Figure 8, we know that only a small proportion of these patches will be contributing any significant current at a given voltage (or total diode current). Therefore, it is possible to further scrutinise the simulation data and particularly the patch current density, J_γ, from Eq. (4), to determine the number of patches that actually contribute any significant current. Plotted in the inset of Figure 12, is the patch current J_γ plotted against the respective barrier height Φ_γ for the 200 K distribution of Figure 11(b) (at a total current density of 10 μA/cm^2). Despite the mean barrier height of the 200 K distribution being 0.82 eV, the inset of Figure 12 shows that the majority of the current comes from patches of much lower barrier height. In fact, it was calculated that 99% of the 10 μA/cm^2 flowing through the diode was passing through just 8% of the patches—the 80,000 patches/cm^2 with the lowest barrier height. This same calculation was carried out across the full range of current densities and at 40, 100, and 200 K, and the results are plotted in the main

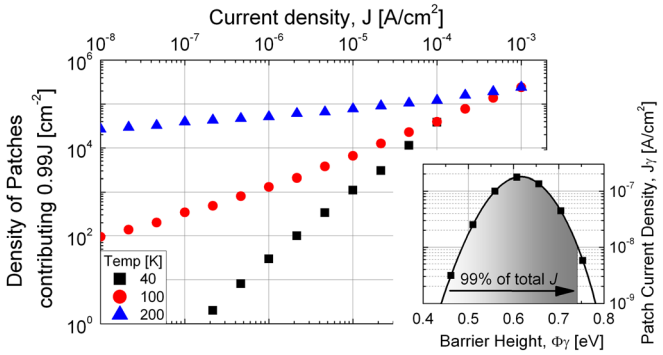

FIG. 12. Inset: The current density contribution (J_γ) plotted against Φ_γ for the γ distribution at 200 K and 10 μA/cm^2. 99% of the total current density is found to come from 80,000 patches/cm^2 of low barrier height. Main: the results of this same calculation are plotted for all current densities modelled at 40, 100, and 200 K.

part of Figure 12. As one might expect, as the total current passing through the diode increases, so too does the total number of contributing patches. However, there is a very obvious difference in the rate of increase at the different temperatures. At 200 K, there is little effect from pinch-off, resulting in a large σ_γ. Hence, the total current flowing is well shared between a few patches of low barrier height, and numerous patches with a higher barrier, and therefore, there is a very large amount of contributing patches even at low current densities. This can be seen when referring back to Figure 8, where the 200 K plot can be seen to be made up of contributions from many different patches. This results in relatively low ideality factors, because the effects of resistance on any individual patch are well masked. At 100 K, pinch-off effects mean that there are now fewer patches with a very low barrier energy, and hence, the patch distribution narrows. Therefore, at any low current density, the total current is dominated by very few patches of a similar barrier height. Again referring back to Figure 8, the 100 K plot can be seen at any given current density comprising of very few patches, which suffer resistive effects as soon as they become dominant. This means that the total current passing through the diode is almost always dominated by local patch resistance and hence the very large ideality factors at these low temperatures. This trend continues down to 40 K, with the barrier height distribution of Figure 11(b) continuing to narrow as pinch off effectively homogenises the interface, resulting in fewer patches of low barrier.

Despite the success of this technique in reproducing the I-V-T data, particularly those responses with high ideality factors, a model such as this relies a great deal on the statistical distribution of the patch parameter, γ. Therefore, though the general thesis as explained in the last paragraph may, in principle, be accurate, a physical interpretation of the parameter values attained does not always hold up to scrutiny. The patch densities of Figure 12, especially at low temperature, are one such example of this. For example, any patch density less than 666 cm^{-2} will imply that there is less than one such patch in the diode tested. In the extreme case of the 40 K plot, the patch density drops below 1 cm^{-2} at 100 nA or less. In part, a weakness may exist in the modelling parameters, for instance a total patch density of $C_T = 1 \times 10^6$ cm^{-2} is likely way too low, being chosen originally for the excellent fits provided. However, such a statistical model is unlikely to be accurate given the physical realities of such a contact. Local clusters of one barrier height around dirt or some other physical inhomogeneity could conceivably lead to localised non-Gaussian patch distributions, or other variations from the normal distribution. Therefore, the parameters extracted should not be expected to correspond closely to physically measurable quantities but are most useful in indicating trends as a function of temperature and for comparison between systems.

IX. CONCLUSIONS

An I-V-T dataset, made up of I-V sweeps at 2 K intervals from 20 to 320 K, has been measured for a Ni/SiC Schottky diode and was accurately reproduced using an inhomogeneous patch model. We conclude that at temperatures above around 230 K, the linear region of the log(J)-V plot is more accurately reproduced using the standard Tung model that includes the so-called background current, which does not flow through a low SBH patch. Non-linearity at these higher temperatures is well described by voltage-dependent pinch-off effects. However, we have shown that the effects of resistance cannot be ignored at temperatures below the 230 K threshold, and at current densities greater than 10^{-5} A cm^{-2} at temperatures across the entire range. Hence, a simplified model was derived from Tung's original equations presuming that background current was minimal, and that the current was passing through resistive, pinched-off patches. This simplified model produced a very faithful reproduction of the experimental results. However, close scrutiny of the fitting data used in both methods leaves questions about what physical interpretation should be drawn from the fitting parameters of either model.

The Ni/SiC diode in question displayed TFE-like inhomogeneity, which, in the absence of any tunneling contribution is better explained by the resistive nature of low SBH patches. This supposed TFE behaviour, extracted from T0 plots, is very common across Schottky contacts of any material. It is therefore expected that the resistive implementation of Tung's model can be successful for Schottky diodes of any material at these very low temperatures. However, provided that the ideality factors are not excessively high, or greatly voltage dependent, the resistive elements can be ignored when fitting to the linear region of diodes operating at a single temperature, or over a range of temperatures.

ACKNOWLEDGMENTS

Peter Gammon would like to gratefully acknowledge the financial support from the Royal Academy of Engineering. This work was supported in part by EPSRC Grant No. EP/J001074/1 and by the European Community as an Integrating Activity "Support of Public and Industrial Research Using Ion Beam Technology (SPIRIT)" under EC Contract No. 227012 (Project 181 IonSiC).

APPENDIX: THE TUNG MODEL

Here, we shall fully define the constants and fitting parameters used in Eq. (2), which is repeated here for convenience

$$\begin{aligned} I &= A[(1-C_p)J_{\text{background}} + C_p J_{\text{patches}}] \\ &= AA^*T^2 \exp\left(-\beta\Phi_B^0\right)(\exp[\beta V]-1) \\ &\quad \times \left\{1 - C_1 A_{\text{eff}} + C_1 A_{\text{eff}} \exp\left(\frac{\beta^2\sigma_\gamma^2 V_{bi}^{2/3}}{2\eta^{2/3}}\right)\right\}. \end{aligned} \tag{A1}$$

$J_{\text{background}}$ and J_{patches} are, respectively, the current density contributions from the background (non-patch) current and the current density from the patches. C_1 is the areal density of patches in cm^{-2}, C_p is the percentage area taken up by low barrier patches, $C_p \approx C_1 A_{\text{eff}}$. σ_γ is the standard deviation of the patch parameter γ amongst the patches, presuming a Gaussian distribution. V_{bi} is the built in potential given by $V_{bi} = \Phi_B^0 - V_n - V$ and $\eta = \epsilon_s/qn_{no}$. ϵ_s is the permittivity of the semiconductor, β is the inverse thermal energy $\beta = q/kT$, with q the electron charge and k the Boltzmann constant, and V_n is the energy difference between the Fermi level and the conduction band. A_{eff} is the localised effective area of a single patch, a temperature dependent variable defined[24,31] as

$$A_{\text{eff}} = \frac{4\pi\gamma\eta^{2/3}}{9\beta V_{bi}^{2/3}}. \tag{A2}$$

At 300 K, the number of free carriers within the conduction band, n_{no}, may all be presumed to be from the nitrogen dopants ($N_D = 1\times10^{16}\,\text{cm}^{-3}$), with the wide bandgap of SiC making the intrinsic carrier concentration (n_i) negligible. However, the wide bandgap means that dopant freeze-out at the lower temperatures does have to be considered. Hence, from Sze,[27] n_{no} was found given that

$$n_{no} = N_C \exp\left(-\frac{E_C - E_F}{kT}\right), \tag{A3}$$

$$\approx \frac{N_D}{1 + 2\exp[(E_F - E_D)/kT]}, \tag{A4}$$

where N_D is the dopant density, N_C is the density of states in the conduction band, E_F is the Fermi level, E_C is the lower conduction band edge, and E_D the nitrogen donor energy,[44] which lies 0.052 eV below E_C. Along with n_{no}, N_C was also considered temperature dependent, as was E_F and V_n, with temperature related equations for each found in.[27]

[1] B. Ozpineci and L. Tolbert, "Silicon carbide: smaller, faster, tougher," IEEE Spectrum **48**(10), 45 (2011).
[2] A. Fontserè, A. Pérez-Tomás, M. Placidi, J. Llobet, N. Baron, S. Chenot, Y. Cordier, J. C. Moreno, M. R. Jennings, P. M. Gammon, C. A. Fisher, V. Iglesias, M. Porti, A. Bayerl, M. Lanza, and M. Nafría, Nanotechnology **23**, 395204 (2012).
[3] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, Appl. Phys. Lett. **63**, 1214 (1993).
[4] N. Miura, T. Nanjo, M. Suita, T. Oishi, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa, and T. Jimbo, Solid-State Electron. **48**(5), 689 (2004).
[5] P. M. Smith, IEEE Trans. Microwave Theory Tech. **44**(12), 2328 (1996).
[6] D. Defives, O. Noblanc, C. Dua, C. Brylinski, M. Barthula, and F. Meyer, Mater. Sci. Eng., B **61**, 395 (1999).
[7] K.-Y. Lee and Y.-H. Huang, IEEE Trans. Electron Devices **59**, 694 (2012).
[8] B. J. Skromme, E. Luckowski, K. Moore, M. Bhatnagar, C. E. Weitzel, T. Gehoski, and D. Ganser, J. Electron. Mater. **29**, 376 (2000).
[9] L. Calcagno, A. Ruggiero, F. Roccaforte, and F. La Via, J. Appl. Phys. **98**, 023713 (2005).
[10] M. E. Aydin, N. Yildirim, and A. Turut, J. Appl. Phys. **102**, 043701 (2007).
[11] I. Nikitina, K. Vassilevski, A. Horsfall, N. Wright, A. G. O'Neill, S. K. Ray, K. Zekentes, and C. M. Johnson, Semicond. Sci. Technol. **24**, 055006 (2009).
[12] X. Ma, P. Sadagopan, and T. S. Sudarshan, Phys. Status Solidi A **203**, 643 (2006).
[13] F. Roccaforte, F. La Via, V. Raineri, R. Pierobon, and E. Zanoni, J. Appl. Phys. **93**, 9137 (2003).
[14] L. Boussouar, Z. Ouennoughi, N. Rouag, A. Sellai, R. Weiss, and H. Ryssel, Microelectron. Eng. **88**, 969 (2011).
[15] D. J. Ewing, L. M. Porter, Q. Wahab, X. Ma, T. S. Sudharshan, S. Tumakha, M. Gao, and L. J. Brillson, J. Appl. Phys. **101**, 114514 (2007).
[16] F. Giannazzo, F. Roccaforte, F. Iucolano, V. Raineri, F. Ruffino, and M. G. Grimaldi, J. Vac. Sci. Technol. B **27**, 789 (2009).
[17] F. Roccaforte, F. Giannazzo, and V. Raineri, J. Phys. D: Appl. Phys. **43**, 223001 (2010).
[18] S. Shivaraman, L. H. Herman, F. Rana, J. Park, and M. G. Spencer, Appl. Phys. Lett. **100**, 183112 (2012).
[19] S. Bellone, L. Di Benedetto, and A. Rubino, J. Appl. Phys. **113**, 224503 (2013).
[20] L. Huang, F. Qin, S. Li, and D. Wang, Appl. Phys. Lett. **103**, 033520 (2013).
[21] A. F. Hamida, Z. Ouennoughi, A. Sellai, R. Weiss, and H. Ryssel, Semicond. Sci. Technol. **23**, 045005 (2008).
[22] M. Furno, F. Bonani, and G. Ghione, Solid-State Electron. **51**, 466 (2007).
[23] L. Zheng, R. P. Joshi, and C. Fazi, J. Appl. Phys. **85**, 3701 (1999).
[24] R. T. Tung, Phys. Rev. B **45**, 13509 (1992).
[25] R. T. Tung, Mater. Sci. Eng. **35**, 1 (2001).
[26] P. M. Gammon, A. Pérez-Tomás, V. A. Shah, G. J. Roberts, M. R. Jennings, J. A. Covington, and P. A. Mawby, J. Appl. Phys. **106**, 093708 (2009).
[27] S. M. Sze and K. K. Ng, "Si Dopant and freeze-out calculations," in *Physics of Semiconductor Devices* (Wiley, New York, 2007), pp. 23–26.
[28] D. Korucu, A. Turut, and H. Efeoglu, Physica B **414**, 35 (2013).
[29] K. Sarpatwari, S. E. Mohney, and O. O. Awadelkarim, J. Appl. Phys. **109**, 014510 (2011).
[30] P. M. Gammon, E. Donchev, A. Pérez-Tomás, V. A. Shah, J. S. Pang, P. K. Petrov, M. R. Jennings, C. A. Fisher, P. A. Mawby, D. R. Leadley, and N. McN. Alford, J. Appl. Phys. **112**, 114513 (2012).
[31] H. J. Im, Y. Ding, J. P. Pelz, and W. J. Choyke, Phys. Rev. B **64**, 075310 (2001).
[32] I. Ohdomari and K. N. Tu, J. Appl. Phys. **51**, 3735 (1980).
[33] J. L. Freeouf, T. N. Jackson, S. E. Laux, and J. M. Woodall, J. Vac. Sci. Technol. **21**, 570 (1982).
[34] Y. P. Song, R. L. Van Meirhaeghe, W. H. Laflere, and F. Cardon, Solid-State Electron. **29**, 633 (1986).
[35] J. H. Werner and H. H. Güttler, J. Appl. Phys. **69**, 1522 (1991).
[36] L. Cheng, I. Sankin, J. N. Merrett, V. Bondarenko, R. Kelley, S. Purohit, Y. Koshka, J. B. Casady, and M. S. Mazzola, in Proceedings of the ISPSD, 2005.
[37] M. Shanbhag and T. Chow, in Proceedings of the ISPSD, 2002.
[38] Y. Yang, A. J. Forsyth, S. Dimler, D. Wu, C. H. Tan, C. Jia, and W. Bailey, IET Power Electron. **5**, 739 (2012).
[39] A. J. Forsyth, S. Y. Yang, P. A. Mawby, and P. Igic, IEE Proc.: Circuits Devices Syst. **153**, 407 (2006).
[40] A. Pérez-Tomás, M. R. Jennings, M. Davis, J. A. Covington, P. A. Mawby, V. Shah, and T. Grasby, J. Appl. Phys. **102**, 014505 (2007).
[41] F. Roccaforte, F. La Via, V. Raineri, P. Musumeci, L. Calcagno, and G. G. Condorelli, Appl. Phys. A: Mater. Sci. Process. **77**, 827 (2003).
[42] J.-H. Shin, J. Park, S. Jang, T. Jang, and K. S. Kim, Appl. Phys. Lett. **102**, 243505 (2013).
[43] A. Saxena, Surf. Sci. **13**, 151 (1969).
[44] W. Gotz, A. Schoner, G. Pensl, W. Suttrop, W. J. Choyke, R. Stein, and S. Leibenzeder, J. Appl. Phys. **73**, 3332 (1993).