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Effect of Si nanoparticles on electronic transport mechanisms in P-doped silicon-rich silicon nitride/c-Si heterojunction devices

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ABSTRACT

We successfully fabricated hetero-junction (H-J) devices from P-doped silicon-rich SiN_x embedded with Si nanoparticles on a p-type crystalline Si substrate at low temperature. High-resolution transmission electron microscopy (HRTEM) analysis indicates that the thin films contain nano-crystallites. The H-J devices showed a good rectification ratio at room temperature. Three distinct regions of temperature dependent J-V characteristics curve can be identified, where different current density variations are indicated. In the low voltage range, the current across the interface of H-J follows an ohmic behavior. In the intermediate range of voltage, the current transport mechanism shows a transition from the phosphorus diffusion to tunneling dominant due to the silicon nanoparticle size and interface of HJ device changed, while the space-charge-limited current (SCLC) dominates the conduction mechanism in the high voltage range and the density of trapping states also affects the electron transport proceeding. At last, the proper size of silicon nanoparticle can reduces the interface charge density of H-J, which is confirmed via the numerical C-V matching technique and we propose a new energy band diagram to fit the HJ device embedded by the silicon nanoparticles.

1. Introduction

Silicon nano-crystals have caused wide public concern over the recent years [1] owing to their quantum confinement effect [2,3], self-purification [4] and increase of donor ionization energy [5] and others, which make the holistic material has a series of unique physical properties and potential applications in the field of light-emitting devices, optical detectors and photovoltaic devices [6,7]. In the past few years, along with development of the third generation high efficient solar cell material and its deep research, the dielectric matrix, such as silicon-rich SiN_x/SiO_x (SRN/SRO), embedded by silicon nanocrystals was gradually used to prepare tandem solar cell, intermediate-band solar cell and multiple exciton generation solar cell for they indicated a more reliable and tunable band gap [8–10]. Silicon nanocrystals (SiNCs) embedded in SiN_x/SiO2 can be easily prepared by a variety of methods. In addition, the silicon dot size and the density of dots are also closely related to the processing temperature [11] due to the thermodynamical unstability of SRN/SRO, the excess silicon atoms crystallize as SiNCs embedded in the dielectric matrix with high-temperature annealing, forming of the light-emitting SRN/SRO embedded by SiNCs [12,13]. For many nano-sized objects, the properties can be inevitably tailored via controlled doping with impurity atoms [14,15] and many doping works have been devoted to optical studies of SiNCs embedded in SiNx/SiO2 matrix [16–18]. However, the higher potential barrier (9.0 ev) of SiO_x could reduce carrier injection efficiency compared with non-stoichiometric SiN_x which has advantage in tuning a lower band gap from 2.5 to 5.3 eV by adjusting the nitrogen content [19,20].

Recently, there are many reports about silicon-rich silicon nitride which contains nanoparticles. For instance, Huang and SO have prepared silicon-rich silicon nitride and silicon oxide films, doping with phosphorus, boron and antimony atoms, via the co-sputtering technique with annealing at 1100 °C [9,21]. These results indicate higher conductivities for the nitride/oxide materials and effectively improved the properties of tandem solar cell. Unfortunately, a significant amount of issues including doping and electronic transport mechanisms still need to be discussed. Doping of SiNCs with various impurities is difficult due to the large impurity formation energy [22,23] and the effects of introduction of impurity to SiNCs embedded in dielectric matrix are also multi-faceted. Take phosphorous for example, it leads to either relaxation effects or the charge compensation and filling defect [24,25]. In addition, the doping of P will hinder the growth of silicon

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quantum dots and then affect free carriers generation [26,27]. Therefore, there is a competitive relationship between the above two impacts on the optoelectronic properties of SiNCs devices. For the silicon quantum dots, which can be tunable by adjusting the silicon content and annealing time or temperature [9,28], the confinement effect causes its band gap to enhance and carriers transport mechanism become more complicated, thus significantly impact the performance of nano-silicon devices. These studies have mainly focused on the influences of surrounding host, doping mechanisms and photoelectron excitation principle. However, the effects of nano-particles on the P-doped silicon-rich SiN_x are not yet fully investigated especially about the current transport mechanisms. Furthermore, the electron transport mechanism across the phosphorous-doped silicon-rich SiN_x/p-type c-Si heterojunction interface is of significance importance for the deeply studied of the device characteristics, which should also be clarified. While this work has a great potential for improving the performance of nano-crystalline silicon devices and is still worth to discuss.

In this paper, P-doped SiNx embedded by silicon nano-crystals prepared by using PECVD at low temperature and electronic transport mechanisms of n-type silicon-rich nc-SiN_x:H embedded by silicon nano-crystals/p-type crystalline Si hetero-junction devices studied by current-voltage characteristics that depend on the temperature and capacitance-voltage techniques. The actual microstructure changes of the n-type nc-SiN_x:H film were obtained by using the high-resolution transmission electron microscope (HRTEM). Moreover, the effect of embedding the silicon crystals on the performance of nc-SiN_x:H H-J devices is investigated. The results show that the grain size of nano-crystalline silicon is of significant importance for the transport mechanism and electrical properties.

2. Experimental

In this study, we successfully fabricated n-type nc-SiN_x:H films embedded by Si nanocrystals via a well-known radio frequency plasma-enhanced chemical vapor deposition technique (RF - PECVD) at low temperature. The n-type nc-SiN_x:H films were grown using a gas mixture of SiH_4, NH_3, H_2 and PH_3, where the pH_3/(SiH_4+PH_3) doping ratio, the SiH_4/H_2 gas flow rate ratio and the H_2 gas flow rate have been set at 1.25%, 1%, and 100 sccm, respectively. Films with different stoichiometry was deposited by varying the gas flow rate ratio as R= $NH_3/(SiH_4+H_2+PH_3)$ in the range 0–0.1. In the meanwhile, for devices, the substrates were p-type crystal silicon with (100)-orientation and the resistivity was 1–10 Ω cm, and then 350 nm thick n-type nc-SiN_x:H films were deposited on the p-type Si substrate by RF-PECVD. At last, ohmic contacts were made by evaporating pure aluminum and the area of these devices is 1.0×1.0 cm^2.

For the silicon nitride thin film, the content ratio (x) of nitride and silicon was measured by using JXA-8230 EPMA. Structural changes in the films induced by different nitrogen incorporation were investigated using JEM-2010F transmission electron microscopy (TEM) with 200 kV accelerating voltage. For hetero-junction devices, dark I-V curves dependent on temperature were collected with keithley 2400 semiconductor characterization system from 190 K to 290 K, and the C-V curves were obtained at room temperature by using the Aglient B 1500A semiconductor parameter analyzer at a fixed frequency of 1 MHz with 10 mV ac voltage and voltage sweep rate 0.03 V/s. Lastly, all measurements were carried out in an electromagnetic shielding environment during the testing process.

3. Results and discussions

Electron probe micro analyzer can be used for quantitative analysis of the types and contents of the element in the film. Table 1 shows the content ratio x (N/Si) of different R samples. It is observed that the content ratio x is larger with the R increased. However, these results are all less than the stoichiometric ratio of the silicon nitride thin film (x∼1.33). Therefore, these films prepared by this method are the silicon-rich silicon nitrides.

Fig. 1 displays comparisons of the TEM and SAED pictures of different R samples. These pictures show that the microstructure of film was changed pronouncedly with the increase of N incorporation. It can be seen from picture that (a) N type nc-Si:H contains large amounts of different crystal orientations crystalline silicon particles, whose grain size was measured to be 6 nm, approximately. Both pictures of (b) and (c) reveal that numerous black dots are embedded within the amorphous silicon based matrix. The SAED patterns of the samples show diffused diffraction rings which are indexed as three oriented crystalline silicon as (111), (220), and (311), respectively. On the other hand, except for the diffraction rings and diffused aureoles, there are additional bright dots in the R=0 sample. However, the patterns of (b) and (c), consisting of rings instead of dots, reveal that there are disordered mono-crystalline structures in the host matrix. Therefore, the black dots could be attributed to mono-crystalline silicon quantum dots (QDs), and the surrounding host matrix could be attributed to amorphous silicon-rich SiN_X.

Once the devices were prepared, which are shown in Table 2, and the I-V curves at room temperature of different silicon nanoparticle size devices were obtained by using an Agilent B5100A parameter analyzer, as shown in Fig. 2(a). Compared to the current – voltage characteristic (I-V) of nc-Si H-J devices, which have a high rectifying ratio at room temperature (on the order of 9561:1 at ± 1 V), the HJ devices of nc-SiN_x embedded by silicon nanoparticles with different sizes have obvious changes such as the rectifying ratio. Table 3 shows specific rectifying ratios of H-J devises which displays that D2 device has higher rectifying ratio than others and the value is decreases with nanoparticle size reduces, however, these values all of the above are better than silicon-rich SiN_x/c-Si(1000:1 at ± 1 V and room temperature) [48] and nc-Si:H/c-Si (760:1 at 300 K) [47], which indicates that the proper size of silicon nanoparticle can enhance I-V characteristic for the corresponding H-J device. Moreover, we can see that, the current densities of H-J devices (D2-D5) are all higher than that of D1 device in the low forward bias region, as shown in Fig. 2(b). Such result suggests that the changes of rectifying behavior and current density might be related to the size reduction of silicon nanoparticle which attributed to the effect of nitrogen incorporated on the films microstructure, inhibiting the silicon crystalline grains growth.

Fig. 2(b) shows dark I-V characteristics of these different nanoparticle size devices: the ln(I)-ln(V) plot (in the inset the equivalence circuit diagram of HJ device is showed) at room temperature with both polarities. Three distinctly different regions can be identified in the ln(I)-ln(V) plot. In the first region (V < 0.25 V), Fig. 3(a) and (c) show the reverse and low forward currents of D1 and D3 devices. They are almost the same and the relationship between ln I and ln V gives a slop of approximately 1 which is same as the published hetero-junction device (n-SiC_x:H

Table 1
Content ratios x (N/Si) of different R deposited films.

	R=0.02	R=0.04	R=0.06	R=0.08
x(N/Si)	0.16	0.32	0.58	0.76

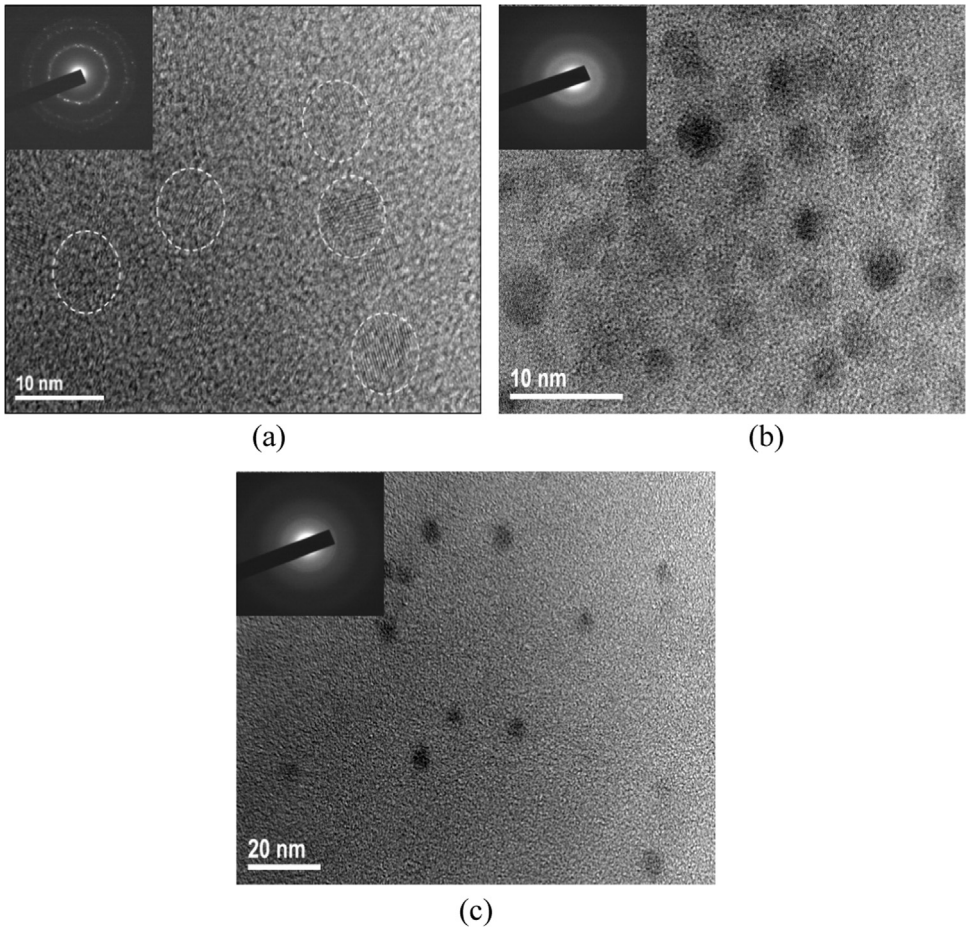


Fig. 1. Comparisons of the patterns of high-resolution TEM and SAED for different R samples(a:R=0,b:R=0.02,c:R=0.04).

Table 2
Silicon nanoparticle sizes and gas flow rate ratio R of different H-J devices.

	D1	D2	D3	D4	D5
R	0	0.02	0.04	0.06	0.08
Grain size (nm)	6.3	4.8	3.03	2.1	1.5

Table 3
Rectification ratios and shunt resistors of different silicon nanoparticle size H-J devices.

	D1	D2	D3	D4	D5
Rectification ratio	9.561×10^3	1.15×10^4	3.148×10^3	1.894×10^3	1.3×10^3
R_{sh} (Ω cm^2)	2.92×10^5	–	1.95×10^5	1.13×10^5	9.04×10^4

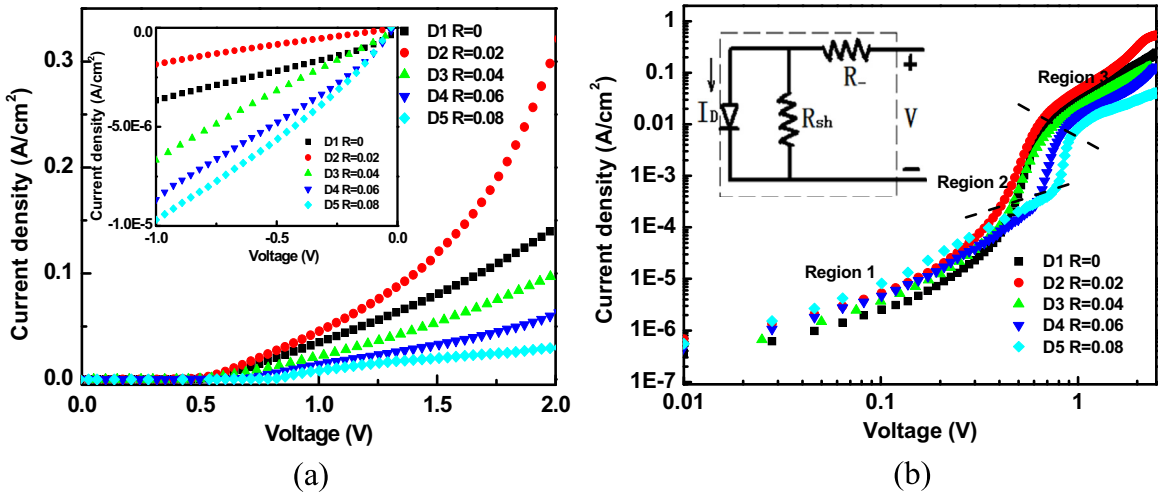


Fig. 2. Dark current-voltage curves of n-type SiN_x:H/p-type c-Si hetero-junction devices with different silicon nanoparticle sizes: (a) the forward I-V curves and the inset is the reverse I-V curves. (b) The forward ln current vs ln voltage characteristics at room temperature.

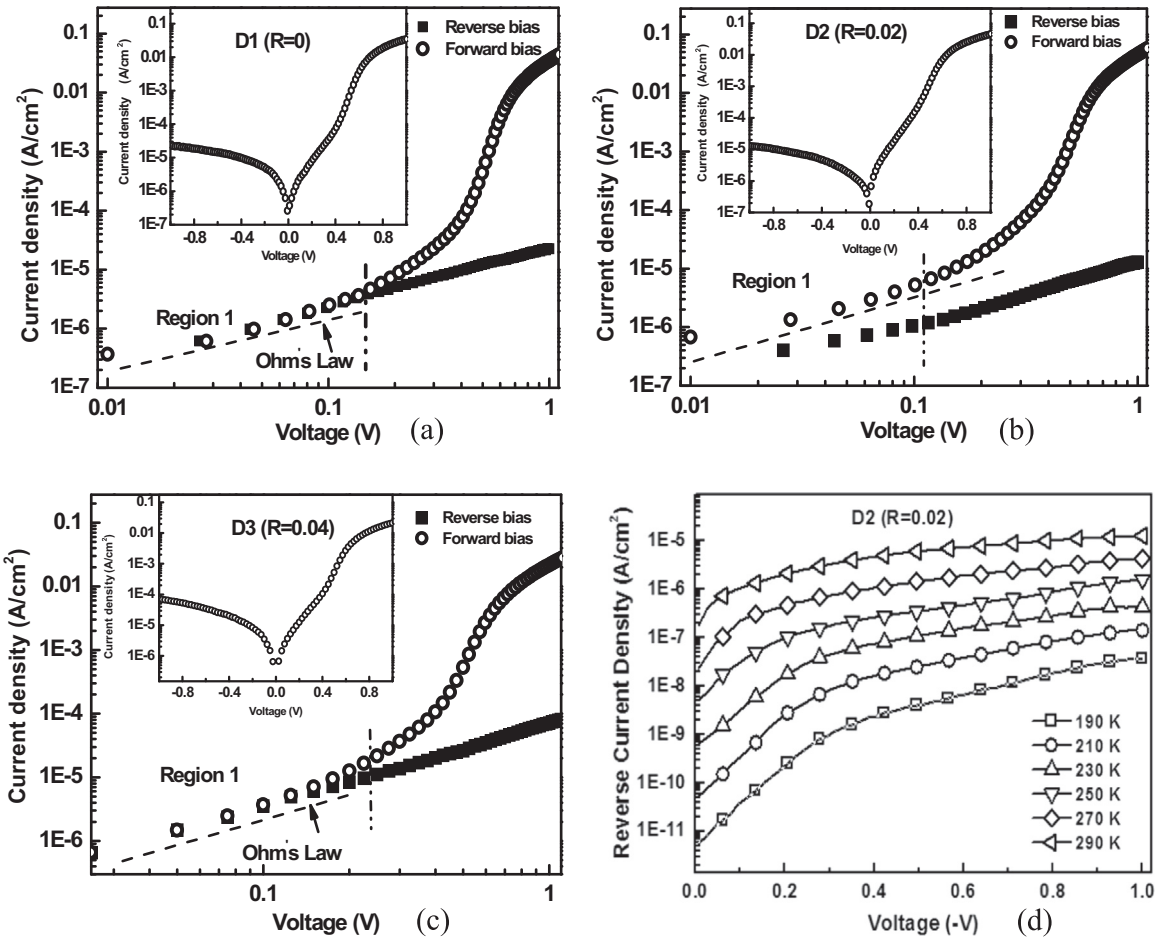


Fig. 3. Reverse and low forward currents – voltage curves of D1 (a), D2 (b) and D3 (c) devices, and the reverse I-V curves in the bias region of −1-0 V for different temperatures of D2 (d).

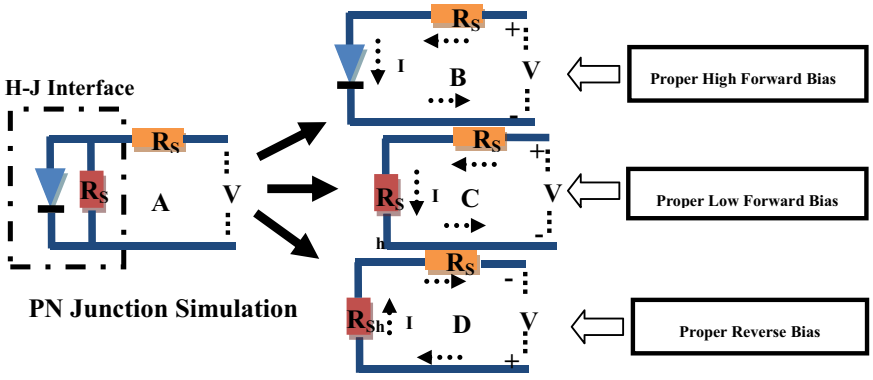


Fig. 4. The equivalent circuit diagrams of H-J device in different applied voltages.

/p-crystalline Si) [49], but it is not apparent in D2 device (b). Song and Marsal et al. thought it attributed to an Ohmic shunt resistance R_{sh} which can characterize the leakage current which can shunts the junction and is affected by the bulk interface defect states [35,49].

As we known, the hetero-junction interface can be equivalent to an ideal diode and a shunt resistance which much higher than series resistance of H-J device. The equivalent circuit diagrams are nearly same at proper low forward bias and proper reverse bias, which is showed in Fig. 4, then the shunt resistance is given by Ohm's law $R_{sh}=V/I$ [49]and the R_{sh} values were calculated respectively shown in the Table 3. For D1 and D3 devices, these R_{sh} values were higher than Si-NC:SiC/c-Si heterojunctions ($1.90\times10^5\ \Omega\ cm^2$) [49].

However, it is not parallel between ln I and ln V for the D2 device and the corresponding leakage current density is 18.5 μA/cm² at −1 V bias and room temperature. This value is lower than silicon-rich SiN_x /c-Si H-J diode (38.4 μA/cm²) [48] and better than poly-SiC_x:H/p-crystalline Si H-J device (5×10^{-4} A/cm²)[50]. Fig. 3(d) shows the reverse I-V curves in the bias region of −1-0 V for different temperatures of D2. It can be seen that the leakage current has a linear dependence on voltage, which indicates that the tunneling current, shown as Fig. 5, playing a dominated role and causing R_{sh} cannot be observed.

At the intermediate voltages (V∼0.25–0.75V), there is an

exponential relationship between the current and voltage and the dark current might be mainly derived from the recombination current formed in the space charge region or the interface. In general, there are two models for explaining the current transport mechanisms through the junction: recombination-limited (or a diffusion mechanism) models and tunneling-limited model. At large voltages ($V > 0.75$ V), the slops of the I-V curves are reduced and deviated from exponential behavior. Furthermore, with carefully inspecting Fig. 2(b), the plots of region 2 for D2-D5 devices move to higher bias region with silicon nanoparticle size reduces, which may arise from the effects of passivation on the H-J device interface state alongside the resistance are enhanced and the size and density of silicon nanoparticle reduce when R increases, therefore, the threshold voltage increases.

From a liner fit to Fig. 2(b) by using Eq. (1), we obtain the n, J_o and series resistance (R_s) as listed in Table 4. It can be seen that, the ideality factor n increases at first and then decreases. Moreover, when the nanoparticles sizes on the order of 5 nm (as D2 device), n is above 2, but is lower than InGaN/AlGaN double hetero-structure diode (ideality factor $n \sim 5$), which is mainly attributed to the tunneling composite of carriers in the interface of H-J device [54,55]. The tunneling path mainly generated by the nanocrystalline silicon clusters and defects in the silicon-rich SiN_x side due to the defect density of p-type c-Si substrate is lower than prepared films. When the size of nanoparticle decreases which is because of R increasing, the densities of silicon cluster and silicon dangling bonds are reduced. In addition, the component of SiN_X increases and the carrier interface recombination decreases. Therefore, n is decreased significantly when silicon nanoparticles size reduces for our own devices. Furthermore, the R_s is on the order of 201 Ω when the size of silicon grain is approximated 5 nm, which is lower than other devices and better than silicon-rich SiN_x/c-Si H-J diode (1000 Ω) [48]. In addition, the saturation current density J_0 of D2 device, which was found by extrapolating the forward current curves to zero voltage, is 2.033×10^{-7} A/cm^2 at room temperature. This value is larger than other devices , but they all lower than previous results reported in the literature, such as n-type β-SiC/p-type c-Si H-J device ($\sim 1.0 \times 10^{-6}$ A/cm^2) [56].

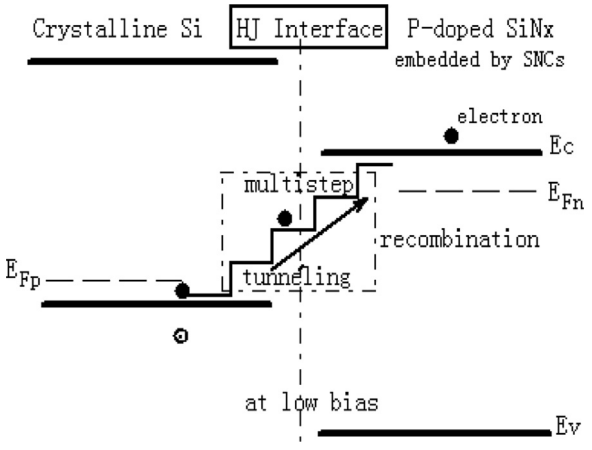


Fig. 5. Proposed multistep recombination tunneling model for the D2 device at low bias.

Table 4
Summary of n, series resistors R_S and J_0 obtained from I-V analysis for different silicon nanoparticle size H-J devices.

	D1	D2	D3	D4	D5
n	1.836	2.05	1.97	1.75	1.13
J_0 (A/cm^2)	1.206E-7	2.033E-7	1.3E-7	6.875E-8	2.58E-8
R_s (Ω)	406	201	682	939	1265

In order to further clarify the impact of Si nano-crystals embedded in the n-type SiN_xH film on HJ devices and determine the specific transport mechanism of devices with different size of nanoparticle in the intermediate voltages. We used the well-known rectifying hetero-junction model to fit the current-voltage curve, the relation between the current and voltage obeys the following formula [29,30]:

$$J = J_0 \exp[A(V - IR)] \quad (1)$$

where J_0 is represented as the saturation short circuit current density, A is a temperature – dependent coefficient and R is the total series resistor which is often assumed to be independent of bias.

In general, there are two models for explaining the current transport mechanisms through the junction [31,32]:

1) If the tunneling mechanism plays a major role for the current, A is a constant independent of the temperature.
2) When the transport is completed primarily by the carrier recombination or a diffusion mechanism in the depletion layer, J_0 and A are given by

$$A = \frac{q}{nkT} \quad (2)$$

A depends linearly on 1/T, k is the Boltzmann constant and n is the ideality factor.

$$J_0 \infty \exp(-E_g/nkT) \quad (3)$$

Eq. (3) is a linear relationship between $\ln J_0$ and 1/T, where E_g is the band gap in the carrier recombination region.

We can attribute regions 2 of these different silicon nanoparticle size devices to the recombination-dominant, and diffusion mechanism or tunneling-dominant transport mechanisms, respectively, based on the fitting results of I-V curves. Fig. 6(a)–(c) reveal typical I-V characteristics dependent on the temperature for D1, D2 and D3 devices, respectively. The insets are the I-V curves from 0.25 V to 0.75 V in the T range (190–290 K). For the D1 device, the slope of I-V curve in the region 2 is temperature dependent. However, it is temperature independent for the D2 device. Moreover, the slope becomes temperature dependent gradually with the decrease of silicon nanoparticle size.

Next, it is necessary to determine which transmission mechanism plays a dominant role by analyzing the measured results in the region 2. Fig. 6(d) shows the relationships between A and 1/T for D1-D5 devices. The parameter A is independent on temperature which can be evidenced by the constant value in the T region for the D2 device. It suggests that the current is mainly dominated by the tunneling mechanism across the junction. As we know, this current transport model is mainly because of the quantum dots. In c-Si, the crystalline silicon size is too large to generate quantum dot, while in the nc-SiN_x:H layer, since many silicon nanoparticles embedded in it, the effect of quantum dots on the mechanism is obvious, so it is reasonable that the tunneling current occurs in the nc-SiN_x:H side of the depletion region. However, the influence of silicon nanoparticles embedded in nc-SiN_x:H on the H-J device interface cannot be neglected. Therefore, it is necessary to further confirm the actual mechanism for our devices, and this discussion is showed at behind. Whereas for other devices, A depends linearly on 1/T, implying a different mechanism compared with D2 device. In addition, be carefully inspecting the slopes of A-1/T curves (D1, D3, D4 and D5) are different, which indicate the silicon nanoparticles affect the mechanisms in the hetero-junction devices.

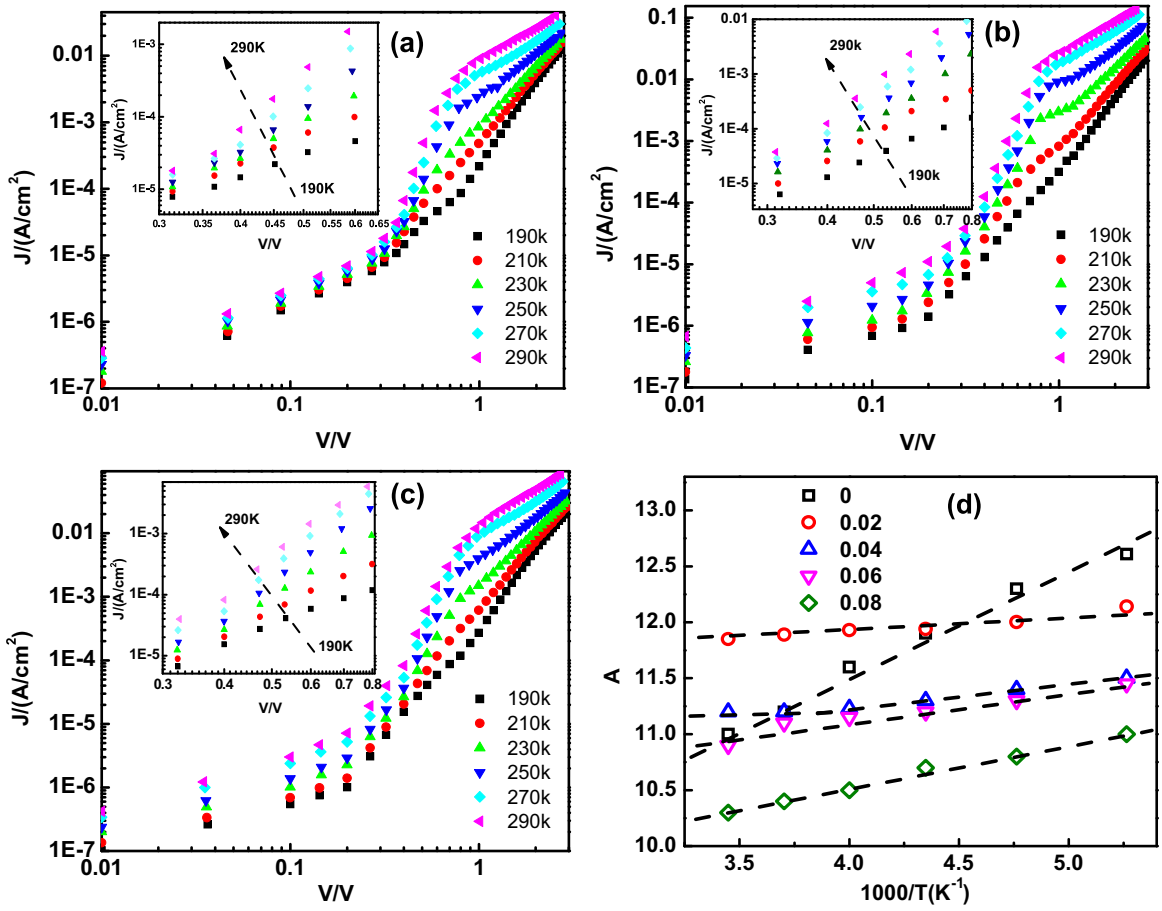


Fig. 6. I-V curves of n-type SiN_x:H/p-type c-Si hetero-junction devices R=0 (a), R=0.02 (b), R=0.04 (c) measured at various temperature (190–290 K) and the insets are the I-V curves from 0.25 V to 0.75 V. (d) shows the temperature dependence of preexponential term (A) in region 2 for these devices.

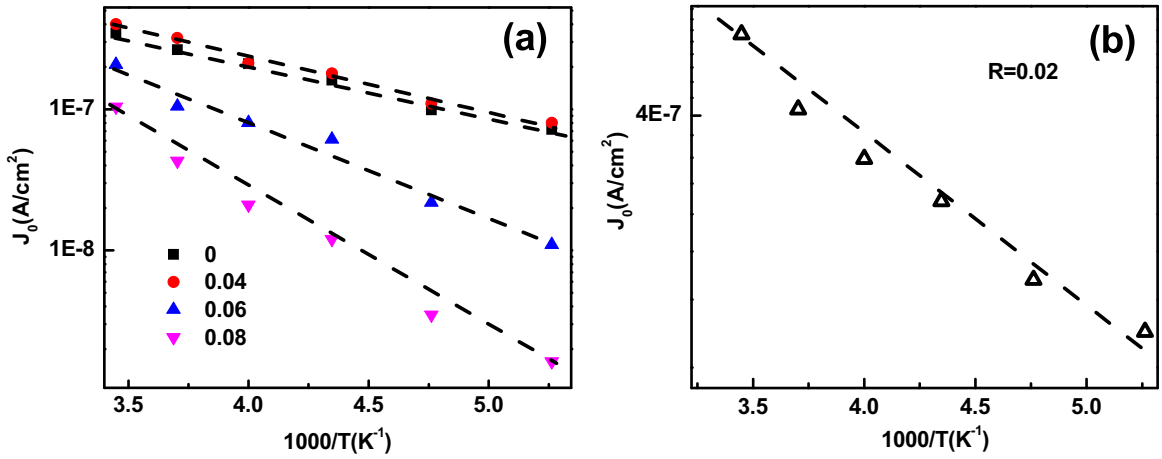


Fig. 7. Temperature dependence of the saturation current density J_0 of D1, D3, D4 and D5 devices (a) and the D2 device (b).

In order to find out the main transport mechanisms of these devices, except for D2 device. Fig. 7(a) displays the relationships between the saturation current density J_0 and 1/T for the different silicon nanoparticles size devices (R=0, 0.04, 0.06 and 0.08). It can be seen that, J_0 depends exponentially on 1/T, which leads to activation energies of 0.4ev, 0.41ev, 0.6ev and 0.68ev from the equation $J_0 = J_{00} \exp(-E_a/nkT)$, where the J_{00} is weakly dependent on the temperature [33]. We found the results are different from the half of the measured band gap of nc-Si:H and nc-SiN_x:H, respectively. For our own samples, phosphorus was more likely to diffuse because of the low base concentration. Therefore, the results suggest that the diffusion mechanism played a dominate role for the current transmission in the interface of H-J device.

For the D2 device, we studied the relation between J_0 and the temperature to determine the more precise tunnel transmission mechanism in the depletion region. Fig. 7(b) shows the J_0-1/T curve of D2 device. We find an interesting phenomenon that J_0 value dependence on temperature as well, suggesting that the holes existing in the valance band of c-Si substrate might transport to the localized states which were generated possibly due to the defects in the band gap of the p-doped nc-SiN_x:H (E_T) by multi-tunneling and then these holes are emitted to the valence band of

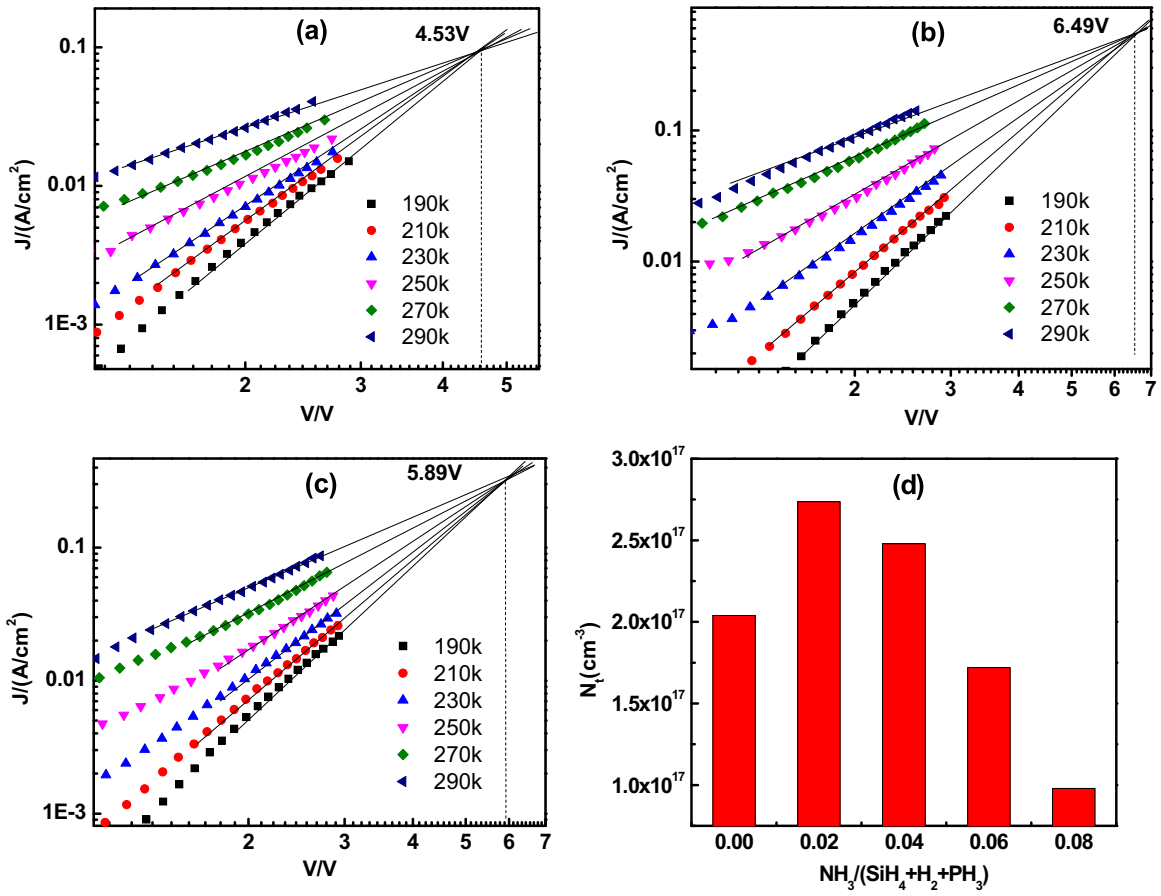


Fig. 8. Space charge limited current (SCLC) model results compared with the experimental data at various temperatures for the devices D1 (a), D2 (b), D3 (c), and the trap density of devices with different silicon nanoparticle size (d).

p-doped nc-SiN_x:H from the E_T [34,35]. Therefore, the current transmission mechanism was also affected by the multi-tunneling and emission models, which is similar to the a-Si/c-Si and β-SiC/Si hetero-junction diodes [36,37]. By combine results in above, we found that the carriers tunneling and holes multi-tunneling with emission concurrently dominated the current transmission mechanism.

Fig. 8(a), (b) and (c) show current-voltage curves of D1, D2 and D3 devices, respectively, in the large voltage region 3 with different temperature (from 190 K to 290 K). We find that these plots have common features for example, the linear relationship of log J – log V and the reduction of slope with the temperature increased. Moreover, the curves can be extrapolated to a single point, which abide by power law [38,39].

In our case, the substrate p-type c-Si has a large number of holes and we can assume the carrier mobility is constant. Therefore, the current and voltage characteristics can be described by [40–43]:

$$J = \mu_p N_c q^{1-l}\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{V^{l+1}}{d^{2l+1}}\right)\left(\frac{l}{l+1}\frac{\varepsilon_s\varepsilon_0}{Nt}\right)^{l} \quad (4)$$

where Nc is the density of states in the relevant band, μ_p is the hole mobility, q is the elementary charge, Nt is the trap density, d is the sample thickness, and $l=T_t/T$ (T is the measurement temperature and T_t is the characteristic temperature). Taking D2 device for example, the data converges to Vc=6.49 V (see Fig. 8(b)) corresponding to the general form of Eq. (4), and the Tt/T+1 is increases linearly as a function of 1000/T, as shown in Fig. 9.

Meanwhile, from the slope of Tt/T+1 – 1/T curve Tt is

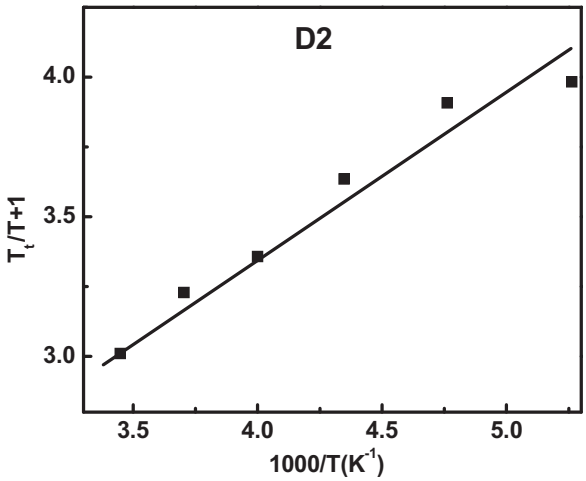


Fig. 9. Space charge limited current (SCLC) model fitting parameter $T_t/T+1$ as a function of 1/T.

determined to be 460 K, which is in the Tt region (310 − 1300K) of amorphous silicon [41]. Therefore, the characteristics from 190 K to 290 K can be explained by using a SCLC model assumed with exponentially distributed traps.

Eq. (4) can be rewritten in the Arrhenius form:

$$J \propto \exp\left[-\frac{E_t}{KT}\ln\left(\frac{qN_t d^2}{2\varepsilon_s\varepsilon_0 V}\right)\right] \quad (5)$$

Here, the activation energy is:

$$E_a = E_t \ln\left(\frac{qN_t d^2}{2\varepsilon_s \varepsilon_0 V}\right) \quad (6)$$

At the crossover voltage point, $E_a = 0$. Therefore,

$$V_c = \frac{qN_t d^2}{2\varepsilon_0 \varepsilon_s} \quad (7)$$

We obtain the Nts value of these devices using Eq. (7), as shown in Fig. 8(d). It can be seen that the N_t increases at first and then decreases with silicon nanoparticle size reduces. These results indicate that the trap density is associated with the doping densities of phosphorus and silicon nanoparticles. When the silicon nanoparticle size reduces to 5 nm, the trap density is approximate $2.7*10^{17}\ cm^{-3}$, which is nearly same with nc-Si:H/c-Si H-J device ($2.3 \times 10^{17}\ cm^{-3}$) [38], and then reduces with silicon nanoparticle size continue decreases. M. A. Rafiq suggested that the trapping states may be weakly affected by the defect states of nanocrystal [38]. Therefore, they may be attributed to defect states within silicon-rich SiN_x especially about the surface of the a-Si clusters. At last, it can be find proper size of silicon nanoparticles can be reduce the trapping states, but the dielectric matrix such as silicon-rich SiN_x has more significantly effect on them.

Furthermore, one interesting phenomenon you can see from the Figs. 2 and 8 is that current density shows the same changing rule as the trap density. Specifically, the current density is increased with increasing trap density. In addition, the current density of D2 device shows a growth with the increasing temperature, shown as Fig. 3(d). These results are consistent with that Nasyrov et al reported [57]. They suggested that the direct electron tunneling between traps plays a dominant role in the charge transport process due to a high concentration traps and a small trap-to-trap separation in silicon-rich silicon nitride. Therefore, the interpretation of charge transport property not only includes the SCLC model, but also includes a trap assisted model, shown as Fig. 10 (a), which can be described as electron tunneling between traps without emission into the conduction band. Meanwhile, with decrease of the density of traps, the electron transport proceeding is changed. Specifically, the electron, which was captured by a trap, emits from the trap into conduction band, and followed with subsequent capture at another trap, shown as Fig. 10 (b), hence, the current density reduces.

With the above parameters, the interface charge density in the space charge region of H-J device and the energy band gap can be obtained by using capacitance - voltage (C-V) measurement of the devices embedded nano-crystalline silicon [44–46]. Meanwhile, the Anderson model can model the capacitance of ideal H-J diode [47,51]. For our own devices, these deposited films embedded by silicon nanoparticles are all highly doped, therefore, our samples are all aniso-type H-J devices and the capacitance of these hetero-junction devices can be given by [47]:

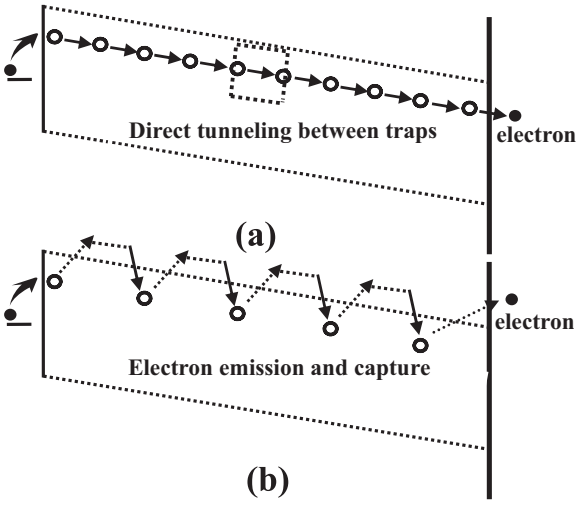


Fig. 10. Electron direct tunneling between traps without emission into the conduction band (a), and the electron, which is captured by a trap, subsequent emission from the trap into conduction band, and followed with subsequent capture at another trap (b).

$$C^2 = \frac{q\varepsilon_1\varepsilon_2 N_1 N_2}{2(\varepsilon_1 N_1 + \varepsilon_2 N_2)(V_{bi} - V)} \quad (8)$$

where, ε_1 and ε_2 are the dielectric constant of c-Si and nc-Si:H, respectively. V_{bi} is the build-in voltage and V is the applied voltage bias. N_1 and N_2 are the doping concentration and defect concentration, respectively.

In order to research the junction interface and the material characteristics of deposited film embedded by silicon nanoparticles, we can linearly fit the curve of C^{-2} versus V. As we know, the valence band discontinuity ΔE_V and conduction band discontinuity ΔE_C of the anisotype H-J device can be obtained by [47]

$$\Delta E_C = qV_D - E_{g1} + \delta_1 + \delta_2 \quad (9)$$

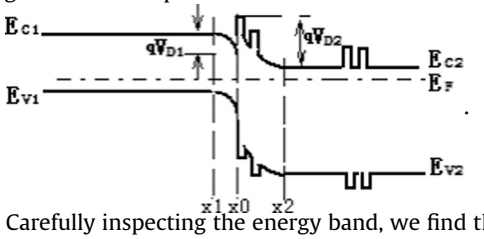
$$\Delta E_V = E_{g2} - (qV_D + \delta_1 + \delta_2) \quad (10)$$

where, E_{g1} and E_{g2} are the forbidden band gap of c-Si and deposited material respectively. δ is the difference in energy between the Fermi level and the valence-band maximum or the conduction-band minimum[47]. δ1 and δ2 are calculated by

$$\delta_1 = kT \ln\left(\frac{N_1}{N_V}\right) \quad (11)$$

$\delta_2 = kT \ln(\frac{N_2}{N_C})$ (12).

Fig. 11 (a) shows the capacitance versus bias voltage of different silicon nanoparticles size devices. In the high voltage range, for the HJ devices, the capacitance were also affected by the defect states in the interface region, so we can find that the change of capacitance value occurs with the nanoparticle size reduces. Fig. 11 (b) shows the plot of C^{-2} versus V, there is a nearly linearity fit between them, which confirms the formed hetero-junction is a typical abrupt model. Therefore, in our case, the energy band diagram can be depicted as follow:



Carefully inspecting the energy band, we find that the junction is discontinuous, which can be explained by the defect states in the interface, and which can be deduced from the slope of C^{-2}-V curve. Fig. 12 shows the Anderson model fitted C^{-2}-V curve and experiment data per H-J device, we can see that the fitted line is nearly same with experiment data in the low forward bias, but an interesting phenomenon is generated with the bias increase, which illustrates that the experiment data deviates from fitted line and the difference between experiment data and fitted data is change with the silicon nanoparticle size. Such as specific, it is lower than others when the nanoparticle size is 5 nm and then increases with nanoparticle size decreases. Kamjoo and Lu et al. think the difference can be attributed to interface charge in the H-J device [47,52]. It was reported that, Nemirovsky has successfully simulated the interface charge density (σ) of the H-J device via a C-V matching methodology [53], which can be written as follows:

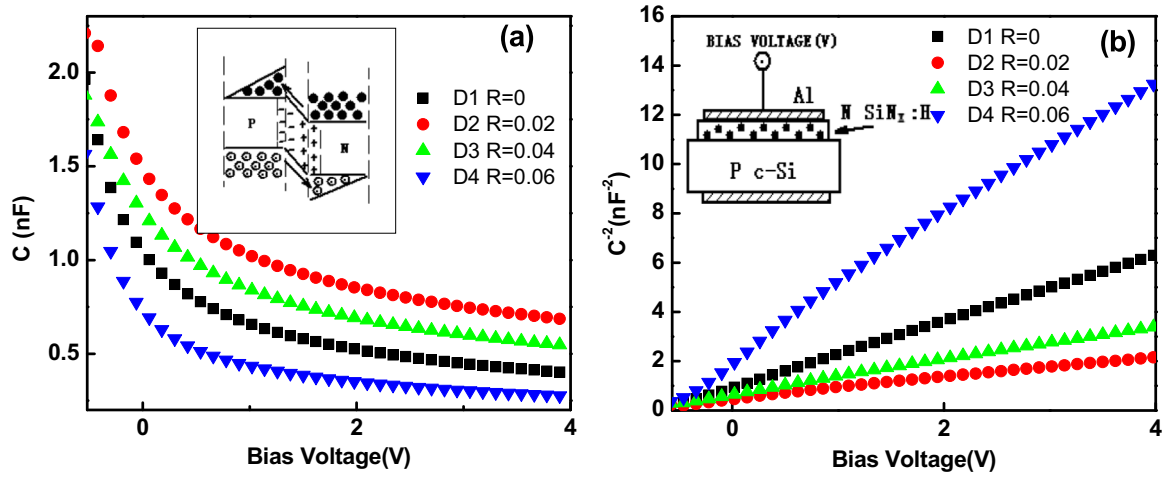


Fig. 11. C-V characteristics of the hetero-junction devices (a). The inset shows the source of the capacitance of the hetero-junction (p-N). C^{-2}-V curves of the hetero-junction devices (b).

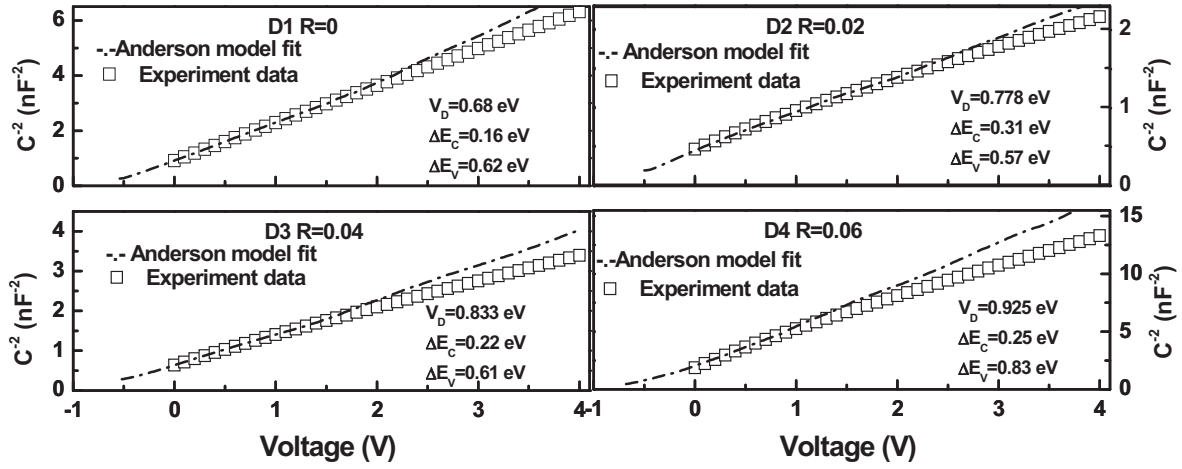


Fig. 12. The Anderson model fitted C^{-2}-V curve and experiment data per H-J device.

$$E_{FC1} - E_{FC2} - \Delta E_C - qV = q\left[V_{D2}(V) - V_{D1}(V)\right] \tag{13}$$

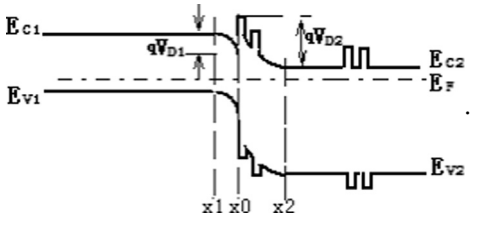
$$Q_1\left[V_{D1}(V)\right] + Q_2\left[V_{D2}(V)\right] + q\sigma = 0 \tag{14}$$

$$\frac{1}{C_t} = \frac{1}{C_1\left[V_{D1}(V)\right]} + \frac{1}{C_2\left[V_{D2}(V)\right]} \tag{15}$$

where, $E_{FC1,2}$, $Q_{1,2}$ and $C_{1,2}$ are represent the differences between the conduction band level and the Fermi energy level, the charges and capacitances on the each side of H-J device respectively. V_{D1} and V_{D2} are band bendings on each side of the H-J device interface [47].

Fig. 13 (a) presents the simulated result which is agreement with the experiment data for the D1device. Moreover, the interface charge densities are showed in Fig. 13 (b). It is find that the value is 5.85×10^{10} cm^{-2} for D2 device which is relatively low compared with nc-Si:H/c-Si H-J device ($\sim 1.20 \times 10^{11}$ cm^{-2}) [47], while it implies that the proper size of silicon nanoparticle embedded in dielectric matrix can reduce the interface defect states and enhance the electric characteristic of H-J device.

Furthermore, from the Fig. 2(a) we can see the current of D2 device is significantly higher than D1 device in the high voltage range. Considering the existence of silicon nanocrystals (Si NCs), we can assume that quantum well (QW) might be formed and its restriction caused the carriers were accumulated in there. Meanwhile, as we know, under the bias voltage, the energy band of quantum wells will be tilted, which would significantly reduce the restriction effect on the carriers and increase the transmission capacity and the collected chance for the carriers, therefore, the device current will increase significantly with the bias voltage increased. Nevertheless, the interface traps for the carriers will occur too, so if the QW is not appropriate (depends on the size of Si NCs), the current will not increase significantly with increasing bias voltage. From the above, the proposed mechanism model is a fit for our experiment results. Therefore, the energy band diagram of n-type nc-SiN$_x$:H/p-type c-Si HJ device embedded by Si NCs can be amended as:



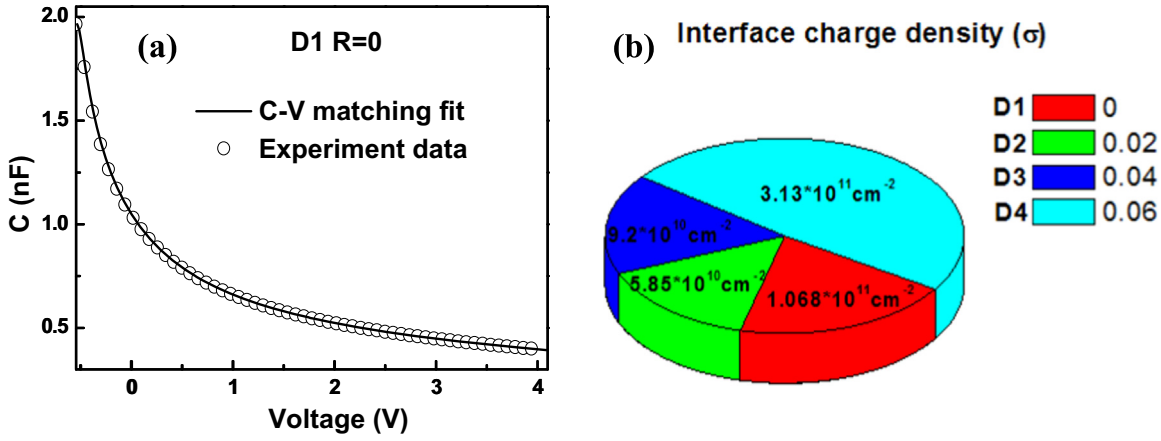


Fig. 13. Simulated C-V matching result for the D1 device (a) and the interface charge densities of different silicon nanoparticle size devices (b).

4. Conclusion

We fabricated the silicon-rich SiN_x/c-Si heterojunction by depositing the n-type nc-SiN_x:H film with embedded the silicon nano-crystals on the p-type c-Si substrate using the RF-PECVD and the conduction mechanisms of HJs have been studied and compared. The results showed that the HJs have good rectification ratios and the silicon nanoparticles significantly modify the electrical behavior of the HJ devices. We obtain the current transport mechanisms of HJ devices by temperature- and bias-dependent current-voltage characteristic analysis. The results indicate that proper size of silicon nanoparticles lead the multistep recombination tunneling mechanism plays a dominant role in the HJ interface region at low bias. In the intermediate range of voltage, there is a significant influence of silicon nano-crystal grains size on the current transport mechanism and the effect of HJ interface on it should not be neglected as well. We found that the phosphorus can diffuse into the crystalline silicon and the mechanism then is changed from diffusion to tunneling dominant mechanisms with the decrease of grain sizes. In the large voltage range, we can explain the mechanism by using a SCLC model assumed with exponentially distributed traps, where the traps density can correlate with the crystal grain size and also affects the electron transport proceeding. Lastly, the interface charge density of HJ device is reduces and then increases with the grain size decreases via the c-v matching methodology simulating. By considering that there are large amounts of silicon nano-crystals in the nc-SiN_x:H film, we amend the quantum structure to the previous HJ model and provide an energy band diagram suitable for our actual samples.

Acknowledgements

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