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Characterizing defects in p–n junctions: an analysis of admittance spectroscopy

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Abstract

Admittance spectroscopy (AS) is a well-established non-destructive electrical characterization technique, characterized by its rapid response times, high accuracy, and independence from stringent rectification characteristics. Despite its potential as a powerful tool for defect analysis and performance evaluation in semiconductor devices, particularly those with p–n junction structures, existing research remains insufficiently in-depth. Defect analysis issues in various p–n junction-based devices are investigated in this paper, including solar cells, light-emitting diodes, and laser diodes. The principles and features of AS are systematically compared with those of deep-level transient spectroscopy. Several case studies on defect analysis and device performance evaluation are presented, providing researchers with a rapid understanding of the methodology. Additionally, common characterization challenges, such as carrier freezing, the extraction of carrier mobility, and negative capacitance, are addressed in detail, with strategies for analyzing these phenomena using AS. This tutorial aims to elucidate the mechanisms underlying defects in p–n junctions and provide guidance for device performance analysis.

Keywords: admittance spectroscopy, p–n junction, defect characterization, capacitance

1. Introduction

The p–n junction is a fundamental semiconductor device structure crucial in various key applications. As the core element of diodes, the p–n junction enables current rectification, signal modulation, and voltage regulation due to its unidirectional conductivity [1, 2]. In optoelectronics, the p–n junction is the essential component of light-emitting diodes (LEDs) and solar cells, where the recombination of electrons and holes generates light, or their separation produces current. These properties are extensively utilized in lighting, communication, and energy conversion technologies [3–5]. Moreover, in power

electronic devices such as rectifiers, power transistors, and varactor diodes, the p–n junction's high voltage and large current capabilities are vital to developing modern power electronics systems [6].

While p–n junction devices are widely utilized across multiple fields, their performance remains influenced by material defects and manufacturing processes [7]. During semiconductor device fabrication, doping is intentionally introduced to enhance material properties, but the occurrence of undesirable defects is unavoidable. Particularly, deep-level defects, which include point defects (such as impurities, vacancies, and interstitial atoms) and extended defects (such as dislocations and grain boundaries), notably affect the performance and reliability of semiconductor devices [8, 9]. For instance, deep-level defects can serve as non-radiative

Table 1. Defect issues in typical p–n junction devices: impacts and research methods.

Affected Devices	Defect impact	Research methods
LEDs	Lowers quantum efficiency (non-radiative recombination); Increases leakage current; Causes efficiency droop at high power.	AS [14–17], DLTS [18], I–V [19–21], Electroluminescence [22], photoluminescence [23], optical differential lifetime [24]
Solar cells	Reduces carrier lifetime; lowers open-circuit voltage; Increases series resistance.	AS [25–28], DLTS [29], I–V [30], photoluminescence [31–33]
Other p–n Junction Devices	Alters doping profiles; accelerates aging; limits maximum voltage.	AS [34–36], DLTS [37], I–V [37–39]

recombination centers or create leakage channels, leading to reduced photoelectric conversion efficiency and light-emitting efficiency in optoelectronic devices [8, 10, 11]. Table 1 presents defect issues, their specific impacts, and the corresponding research methods encountered in several typical p–n junction devices. In recent years, various defect characterization techniques have been compared and discussed [8], including defect morphology observation, chemical composition analysis, structural analysis, optical characterization, and electrical characterization. Among these, electrical characterization methods exhibit several advantages: they are non-destructive, compatible with encapsulated components, and suitable for operando monitoring. While current–voltage (I–V) and capacitance–voltage (C–V) measurements are the most widely used techniques for evaluating macroscopic device characteristics, admittance spectroscopy (AS) [12] and deep-level transient spectroscopy (DLTS) [13] have become the predominant methods specifically designed for analyzing deep-level defects. Compared to DLTS, AS offers unique advantages, including high sensitivity in the frequency domain and adaptability to a wide range of devices.

This paper focuses on the application of AS in characterizing deep-level defects in p–n junctions and provides an overview of recent research progress in this area. The article explores the basic principles of AS and its specific applications to key defect-related issues, using typical problems in p–n junction devices as examples.

2. Principles and measurement methods of AS

2.1. Fundamental principles

AS is an electrical characterization technique initially introduced by Losee [12] and further developed in GaP Schottky barriers by Vincent et al [40]. A DC voltage bias is initially applied, which can alter the band bending within the depletion region, thereby affecting the crossing point between the trap level and the Fermi level. Subsequently, an alternating current signal with a fixed amplitude and varying frequency is applied to modulate trap occupancy, which in turn triggers carrier exchange between the trap levels and the conduction or valence bands, leading to changes in the admittance of

the junction. Through such measurements, AS enables the characterization of carrier dynamics and trap energy levels (E_T) in semiconductors. The voltage-bias dependence analysis performed by Werner et al [41] provides a valuable approach to differentiate the origin of capacitance steps in AS measurements, while simultaneously enabling indirect determination of trap states' carrier type (electrons or holes).

DLTS, complementary to AS, is a technique for characterizing trap states [13]. The method analyzes thermal emission of trapped carriers by monitoring capacitance transients following the application of voltage pulses. By varying the sampling times and temperature, DLTS generates a spectrum where peaks correspond to different defect levels, providing information about trap concentrations (N_T), activation energies (E_a), and capture cross-sections (σ).

The energy band diagrams characterized by AS and DLTS are shown in figures 1(a) and (b) respectively. In the diagrams of a p–n junction, E_{Cp} and E_{Vp} represent the conduction band minimum and valence band maximum of the p-region, while E_{Cn} and E_{Vn} represent the corresponding values for the n-region. E_{T1} and E_{T2} denote two different donor and acceptor levels, and pp' and nn' indicate the boundaries of the space charge region (SCR). Under reverse bias, the quasi-Fermi levels for electrons (E_{Fn}) and holes (E_{Fp}) replace the unified Fermi level (E_F) under equilibrium conditions.

In the AS measurement, an AC signal with different amplitudes and frequencies is applied, and carrier exchange between E_T and the conduction or valence bands occurs in a region where E_T intersects with the Fermi level. This intersection lies at a distance λ from the edge of the depletion region, where $\lambda = [2\varepsilon(E_F - E_T)/q^2 N_d]^{1/2}$ (here, ε is the permittivity, q is the elementary charge, and N_d is the donor concentration), as shown in the yellow region of figure 1(a). In the n-region, donor levels experience filling (solid orange circles) and emission (hollow orange circles), with a similar process occurring in the p-region. Based on the level at which the trap is located, a corresponding characteristic relaxation time constant will be exhibited. As a result, a peak will appear in the conductance spectrum, and the emergence of this peak is closely related to the dynamic behavior of the trap.

Conversely, the traps detected by DLTS are situated within the depletion region that changes with the filling pulse, as
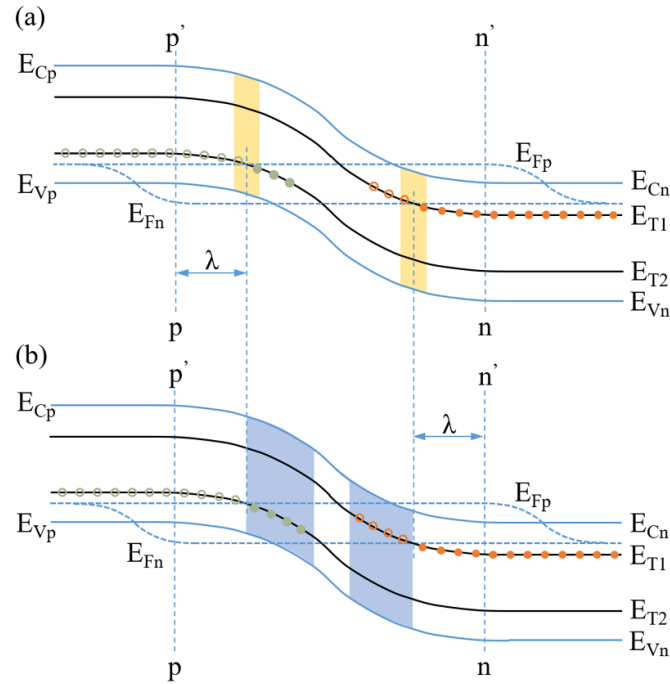
Figure 1. Schematic illustration of the principle: (a) AS and (b) DLTS.

Table 2. Comparison of features between DLTS and AS [42–44].

Feature	AS	DLTS
Device requirement	Lower requirements for junction quality	Requiring high-quality junctions
Detection position	Signal determined by E_T–E_F regions; small reverse biasing preferred; typical $E_T > 100$ meV	Measures space charge in depletion regions; large reverse biasing preferred; E_T could beyond mid-gap
Emission rate	Enables faster rate windows (60 ns to 1 ms); capable of detecting defects with changing configurations.	Lower rate windows (100 μs (best 5 μs) to 5 s)
Measurement range	No minority carrier injection; no dilution limit; more sensitive to interface states.	Possible minority carrier injection; distinguishes between electron and hole traps; exists a dilution limit $N_D > N_T$; mainly suitable for bulk defect analysis.
Capture coefficients	Unable to quantify electron and hole capture coefficients.	Measurement of electron and hole capture coefficients within a limited temperature range.
Influence of electric field	Response originates from defect levels intersecting the Fermi level near the edge of the depletion region; experimental data indicate comparatively negligible electric field effects, making the results largely stable and less susceptible to electric field variations.	Peak position or amplitude can be influenced by the electric field; signal arises from the space-charge region, and may include contributions from the Poole-Frenkel effect.

depicted by the blue area in figure 1(b). When the filling pulse ends, the carriers in the trap level experience thermal emission. The transient change in capacitance over time is recorded, forming the DLTS signal. By analyzing the time-dependent capacitance signal, key trap parameters such as emission rate, trap level, capture cross-section, and defect concentration can be determined.

Table 2 highlights the differences between AS and DLTS across several key aspects. DLTS, particularly when combined with optical injection, can probe defects close to or even below the mid-gap, which is especially advantageous for wide-bandgap semiconductors. In contrast, when probing relatively shallow levels, the detectable energy depth can be estimated from the carrier response time constant (τ), which depends on

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material parameters and varies slightly with the specific formulation used. For DLTS, τ is limited by the minimum achievable rate window of the instrument, generally on the order of a few tenths of a millisecond. By comparison, AS can employ much higher frequencies (typically up to ~100 MHz), corresponding to τ values down to the nanosecond regime, which makes it more sensitive to relatively shallow levels.

Another important distinction is that DLTS typically requires high-quality rectifying contacts, as excessive leakage currents can invalidate measurements, whereas AS relies on equivalent-circuit analysis to extract defect-related capacitance and conductance, making it more tolerant of non-ideal conditions. A notable example is the 'Mg freeze-out' effect: at low temperatures, the capacitance drops sharply, causing DLTS signals to be dominated by free-carrier fluctuations rather than trap emissions. In such cases, DLTS becomes unsuitable, while AS remains viable. Although these limitations exist, it is worth noting that emerging correction methodologies [45] may further improve the resolution and accuracy of DLTS in future applications.

Finally, AS offers unique benefits in detecting highly compensated layers, such as molecular beam epitaxy (MBE)-grown GaN [46]. In these materials, even when deep-level defects dominate the space-charge region, AS remains effective because the space-charge regions of Schottky contacts on high-resistivity MBE-GaN layers tend to break down at high frequencies. With its broader modulation frequency range, particularly its ability to extend to extremely low frequencies (down to the mHz range) [47], AS ensures the integrity of Schottky contacts, mitigating the influence of space-charge region quality issues on detection. Moreover, AS exhibits its exceptional sensitivity to interface trap states [48], utilizing an averaging response method to effectively analyze complex or densely distributed interface traps, thereby providing a clear insight into the energy distribution characteristics of interface defects.

2.2. Equivalent circuit modeling and series resistance (R_s) calculation

The quantitative analysis of AS data is commonly performed using an equivalent circuit model [49]. This method simplifies complex electrical behaviors into combinations of circuit components, such as series resistance (R_s), parallel capacitance (C_p), and parallel conductance (G_p), providing a clear representation of the device's frequency response. Researchers commonly utilize the equivalent circuit model of MOS structures to study the admittance properties of similar configurations, such as the p/MQW/n+ structure (illustrated in figure 2) [16, 50, 51]. In this circuit, C_{sc} is the capacitance of the depleted p-type GaN region in parallel with C_{QW} and R_{QW}, where C_{QW} and R_{QW} represent the capacitance and resistance of the quantum well (QW), respectively. C_I is the capacitance
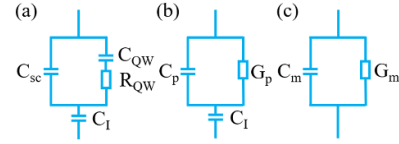

Figure 2. (a) Equivalent circuit of an InGaN/GaN LED structure modeled as a MOS capacitor, (b) simplified parallel circuit representation, (c) real admittance component measurements in parallel circuit mode. Reproduced from [16], with permission from Springer Nature.
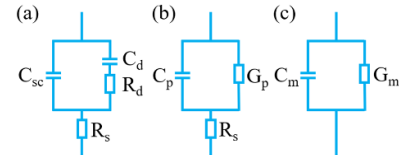

Figure 3. (a) Equivalent circuit of a typical p–n junction structure, (b) simplified parallel circuit representation, (c) real admittance component measurements in parallel circuit mode.

of the wells and barriers considered as insulating interfacial layers in series with the depleted region. C_p and G_p represent the parallel capacitance and parallel conductance, both of which are frequency-dependent. C_m and G_m represent the capacitance and conductance obtained from actual measurements. However, when dealing with typical p–n junction structures, the traditional MOS equivalent circuit model may encounter limitations in describing actual characteristics, making it insufficient to fully reflect their frequency response and defect state behavior.

In admittance measurements, R_s can introduce significant errors, compromising the extraction of interface properties and doping profiles while also limiting the sensitivity of the small-signal steady-state method. To reduce the impact of R_s, measurements can be conducted at low frequencies to effectively minimize its influence or pre-measurement corrections can be applied to ensure the accurate extraction of the required information.

Taking these considerations into account, we proposed an equivalent circuit model tailored for p–n junctions, integrating the R_s to more accurately represent the conductive characteristics of p–n junctions, as illustrated in figure 3. In this circuit, C_d and R_d represent the capacitance and resistance of the defects, respectively. This was achieved by matching the impedance of the simplified circuit with that of the measurement circuit,

$$Z_{\text{simplified}} = R_s + \frac{1}{G_p + j\omega C_p} \tag{1}$$

$$Z_{\text{measured}} = \frac{1}{G_m + j\omega C_m} \tag{2}$$

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The expressions for C_P and G_P/ω can be derived as follows:

$$C_p = \frac{C_m}{(G_m R_s - 1)^2 + \omega^2 R_s C_m^2} \tag{3}$$

$$\frac{G_p}{\omega} = \frac{G_m(1 - G_m R_s) - \omega^2 R_s C_m^2}{(G_m R_s - 1)^2 + \omega^2 R_s C_m^2}. \tag{4}$$

To facilitate comparison, the expressions for C_P and G_P/ω shown in figure 2 are presented here.

$$C_P = \frac{-C_I \left[(C_m^2 - C_m C_I)\omega^2 + C_m^2 \right]}{\omega^2 (C_m^2 - C_{sc}^2) C_m^2} \tag{5}$$

$$G_P/\omega = \frac{G_m C_I^2 \omega}{C_m^2 + (C_m - C_I)^2 \omega^2}. \tag{6}$$

The following sections will provide a detailed explanation of commonly used methods for extracting R_s, categorized into three main approaches. The first approach focuses on extracting the R_s from the forward bias I–V curve. This method is based on the significant influence of R_s on the I–V characteristics of devices, particularly under high forward bias conditions, where the presence of R_s induces non-linear behavior that compromises measurement accuracy.

Originally developed by Norde [52], this method is used to determine the R_s and barrier height values. Norde introduced the following function:

$$F(V) = \frac{V}{2} - \frac{kT}{q} \ln\left(\frac{I}{AA^*T^2}\right), \tag{7}$$

where k is the Boltzmann constant, T is the absolute temperature, A is the diode area, and A^* is the effective Richardson constant.

The effective Schottky barrier height is given by

$$\Phi_b = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \tag{8}$$

and

$$R_s = \frac{kT}{qI_0}. \tag{9}$$

Here, $F(V_{min})$ is the minimum value of $F(V)$, V_{min} is the corresponding voltage, and I_0 is the current when $V = V_{min}$. However, the Norde method has limitations when applied to non-ideal diodes with high R_s (ideal factor $n > 1$), as it requires a more complex evaluation process [53]. This method was originally only applicable to ideal Schottky contacts with an ideal factor of $n = 1$.

Cheung [54] introduced an alternative method for determining the R_s, with the function expressed as follows:

$$\frac{dV}{d(\ln I)} = IR_s + n\frac{kT}{q}, \tag{10}$$

$$H(I) = V - n\frac{kT}{q} \ln\left(\frac{I}{AA^*T^2}\right), \tag{11}$$

and

$$H(I) = IR_s + n\Phi_{b,0}, \tag{12}$$

where $dV/d\ln(I)$ is the slope of the linear region of the $\ln(I)$ versus V plots, $\Phi_{b,0}$ is the actual barrier height derived from the low-voltage region of the forward I–V characteristics. By plotting $dV/d\ln(I)$ versus I and $H(I)$ versus I, straight lines are obtained, with their slope indicating the value of R_s.

Later, Werner [55] introduced another method for calculating R_s and confirmed the reliability of Cheung's proposed approach. Based on the comparative discussion in the supplementary materials, it is recommended to employ Cheung's methodology [54].

Under forward bias for $V_d = V - IR_s \gg kT$, the thermionic diode current I_d is given by

$$I_d = I_s \exp\left(\frac{\beta}{n}\right)(V - IR_s). \tag{13}$$

Equation (13) yields for the small signal conductance $G = dI_d/dV$:

$$\frac{G}{I_d} = \frac{\beta}{n}(1 - GR_s). \tag{14}$$

Equation (14) shows that a plot of G/I_d versus conductance G (here termed as plot A) yields a straight line with y-axis intercept β/n, x-axis intercept $1/R_s$, and slope $-\beta R_s/n$.

From (14) two other possibilities for plots can be derived: The first plot is obtained by solving (14) for $1/G = R_{dr}$, the differential resistance of the I/V curve. This transformation yields:

$$R_{dr} = \frac{n}{\beta I_d} + R_s. \tag{15}$$

Equation (15) suggests a plot of the differential resistance R_{dr} versus inverse current $1/I_d$. A straight line with slope β/n and y-axis intercept R_s is obtained.

The second approach involves calculating R_s using admittance measurements performed in the strong accumulation state [56–60]. At a specified frequency, the capacitor is biased to achieve a strong accumulation state. The admittance Y_{ma} is described by the following equation:

$$Y_{ma} = G_{ma} + j\omega C_{ma}, \tag{16}$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance in a strong accumulation region.

The equation for determining R_s is as follows:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}. \tag{17}$$

The third approach involves estimating R_s based on the frequency dependence of capacitance measurements [61, 62].
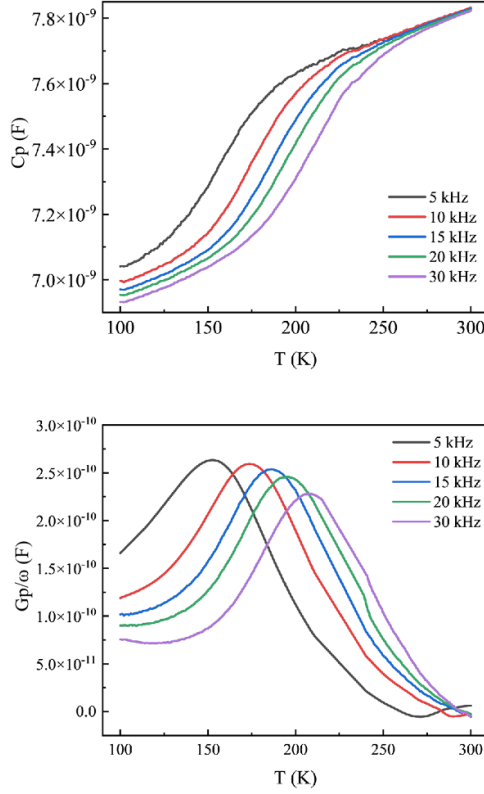
$$C(f) = C_0 / \left[1 + (2\pi f C_0 R_s)^2\right], \tag{18}$$

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Figure 4. AS obtained through temperature scan at various frequencies.

Figure 5. AS obtained through frequency scan at various temperatures.

where f is the frequency of the testing signal in capacitance measurement, $C(f)$ is the capacitance at frequency f, and C_0 is the capacitance on the low-frequency plateau of the C–f dependence.

The approximate value of R_s can be determined by fitting capacitance data across different frequencies. In practical applications, this method offers the advantage of conducting measurements under low-frequency conditions, effectively minimizing the impact of R_s. As the frequency increased, R_s can introduce substantial measurement errors and may even result in inaccuracies in identifying trap types. By reducing such interference, this approach enhances the accuracy of capacitance measurements. Details of R_s calculation approach employed in this work are available in the supplementary materials.

2.3. Representation of modified AS

After selecting an appropriate equivalent circuit and relevant parameters (such as R_s), the AS signals related to defects, C_p and G_p/ω, can be calculated using equations (3) and (4) and plotted accordingly. Typical AS characterization employs two modes: temperature scans at a fixed frequency (as shown in figure 4) and frequency scans at a fixed temperature (as shown in figure 5). The data in figures 4 and 5 are derived from our experimental measurements on LED samples.

Temperature scan measurements of AS generally offer notable advantages. Firstly, the conductance curve as a function of
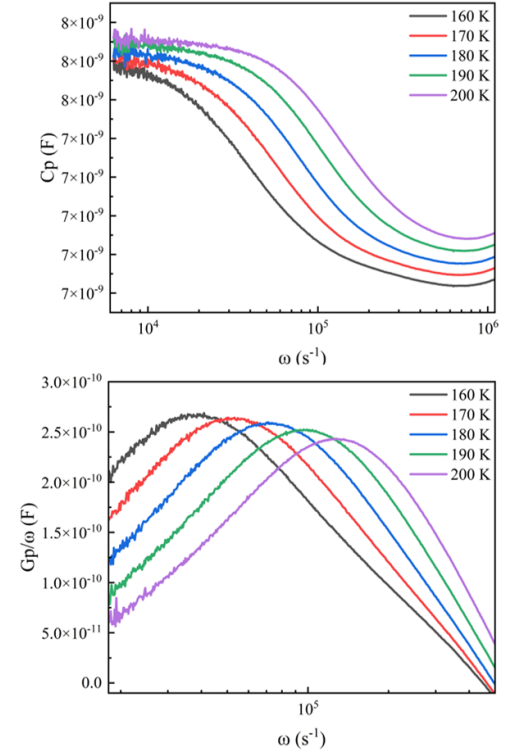
temperature exhibits distinct peaks, which are easier to measure and more accurate compared to frequency scan. Secondly, the temperature-dependent curve is recorded at a single frequency, avoiding the need to correct phase shifts introduced by the experimental circuit at the start of the experiment. As a result, temperature scan admittance measurements yield more precise and continuous curves while significantly reducing measurement time. Due to these benefits, admittance measurements of deep levels in junctions are typically conducted by measuring conductance as a function of temperature at a fixed frequency.

Apart from the two common formats mentioned earlier, other representations include conductance-frequency $(G - f)$ [63, 64], derivative of conductance concerning frequency $(\mathrm{d}G/\mathrm{d}f - f)$ [65], normalized capacitance-frequency $(C/C_\infty - f)$ [63, 64], and negative differential admittance-frequency $(-\Delta B - f)$ [66]. These analytical approaches are primarily derived from fundamental mathematical and physical equations.

2.4. Extraction of trap parameters

When deep-level defects exist in the sample, frequency resonance maximizes the carrier exchange between the deep-level defects and the valence (or conduction) band, resulting in a peak in conductance. This conductance peak is observed on the admittance spectrum. During frequency scan, the peak occurs when the frequency ω of the AC bias matches the emission rate e_p of holes from the trap level, expressed as $\omega = e_p$. In temperature scan, the condition changes to $\omega/1.98 = e_p$ [67].
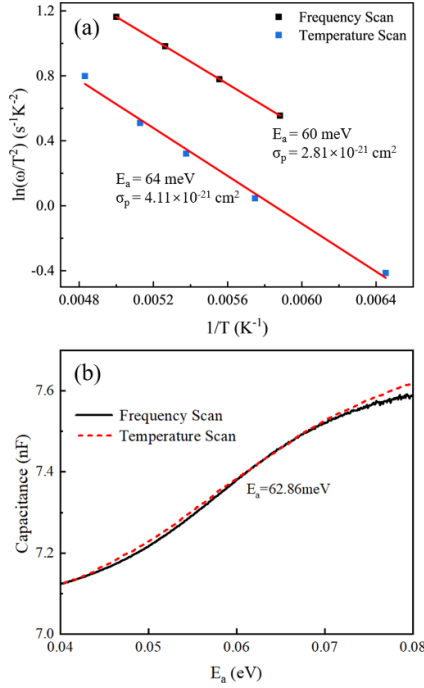
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Figure 6. Comparison of E_a extraction methods: (a) conventional Arrhenius plot analysis versus (b) enhanced Arrhenius-transformed methodology.

Taking holes as an example, the emission rate of holes from the trap level can be expressed as:

$$e_p = 2\sigma_p \cdot \nu_{th} \cdot N_\nu \exp\left(-\frac{E_a}{kT}\right) = \alpha \cdot T^2 \exp\left(-\frac{E_a}{kT}\right), \quad (19)$$

where E_a is the activation energy of the impurity level, σ_p is the hole capture cross-section of the impurity level, ν_{th} is the thermal velocity, and N_v is the density of states in the valence band.

The peak values are then used to construct an Arrhenius plot of $\ln(e_p/T^2)$ versus $1/T$, as presented in figure 6. Linear regression analysis of this plot yields the activation energy E_a (from the slope) and capture cross-section σ_p (from the intercept) of the trap state. Notably, our analysis reveals that conventional single-variable approaches (using either temperature-dependent or frequency-dependent peak values alone) may introduce slight discrepancies in the derived defect energy levels, as evidenced by the two distinct lines in figure 6(a). To overcome this limitation, Li [68] pioneered an innovative data processing methodology that integrates both frequency and temperature variables into a unified parameter. This advanced approach enables comparative analysis of the E_a profiles from different scanning modes, where their intersection point yields more accurate E_a values, as experimentally validated in figure 6(b).

AS can also be employed to investigate the band offset phenomenon, namely QW emission [69]. According to emission-recombination theory, the QW is modeled as a single 2D trap, with the assumption that the 3D equilibrium density above the well remains unaffected by the presence of the QW. The time

response τ is expressed as:

$$\tau = \frac{A\rho_{eq}}{c_n n_{eq}} \quad (20)$$

with

$$\rho_{eq} = \frac{m^* kT}{\pi \hbar^2} \exp\left(\frac{E_F + qV_{QW} - E_1}{kT}\right), \quad (21)$$

$$n_{eq} = 2\left(\frac{m^* kT}{2\pi \hbar^2}\right)^{3/2} \exp\left(\frac{E_F + qV_{QW} - E_2}{kT}\right), \quad (22)$$

where ρ_{eq} (respectively, n_{eq}) is the 2D-carrier density in the well (respectively, 3D density above the well) in thermal equilibrium. c_n is the classical capture coefficient in the QW. m^* is the effective mass of the electron in the well layer, $\hbar$ is the reduced plank constant, V_{QW} is the potential drop between the well and the lower contact, E_1 is the bound lower state level and E_2 is the level quasi-resonant with the quantum barrier conduction band.

A quantum-well capture velocity ν_{QW} defined as $\nu_{QW} = c_n/A$. Given equation (19), this quantum-well capture velocity is related to the time constant τ through the relation

$$\nu_{QW} = \frac{\rho_{eq}}{\tau n_{eq}}. \quad (23)$$

Building on the above derivation, the time response τ of the QW can be formulated as:

$$\tau = \frac{1}{\nu_{QW}}\left[\frac{2\pi \hbar^2}{m^* kT}\right]^{1/2} \exp\left(\frac{E_2 - E_1}{kT}\right). \quad (24)$$

By analyzing the frequency of the oscillating test signal, peaks corresponding to the maximum carrier emission are observed at different temperatures. This corresponds to the optimal thermal emission condition of charge carriers for the level that satisfies the following condition:

$$\omega\tau = 1 \quad (25)$$

$$\omega = \nu_{QW}\left[\frac{2\pi \hbar^2}{m^* kT}\right]^{-1/2} \exp\left(-\frac{E_2 - E_1}{kT}\right). \quad (26)$$

The activation energy ($E_a = E_2 - E_1$) of carriers transitioning from the quantum confinement level in QWs is determined using the Arrhenius plot, which relates the temperature dependence of the parallel conductance peak frequency as $\ln(\omega)/T^{1/2} = f(1/T)$. The slope provides the activation energy E_a, while the intercept yields the QW capture velocity ν_{QW}.

When interpreting AS features, it is crucial to distinguish whether the observed capacitance response originates from deep-level defects or from transport barriers. This issue has been extensively discussed in the context of thin-film solar cells such as Cu(In, Ga)Se$_2$ (CIGS), where the origin of a frequently observed admittance feature—commonly referred to as the 'N1' signature [70]—remains under debate and may be attributed to either deep-level defects or capacitive transport

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barriers. The distinction can be made more reliably by introducing multiple parameters for cross-validation. Specifically, if the equivalent depth variation of the capacitance step (Δx) significantly exceeds the theoretical limit expected for shallow defects (e.g. >100 nm), while its amplitude remains stable under different bias conditions—even persisting under flatband conditions—this provides strong evidence that the feature arises from a transport barrier rather than from defects [41]. Additional supporting indicators include the emergence of a bias-independent peak in the normalized real impedance spectrum (Re[ωZ]) and a linear shift of the capacitance-step inflection frequency under illumination, which can be attributed to the photoconductive effect of the barrier layer [71].

3. Characterization and analysis of specific features in p–n junction

3.1. Dopant freeze-out

The dopant freeze-out problem refers to the phenomenon in which carriers in a semiconductor material are 'frozen' in a certain position and unable to move freely due to insufficient thermal energy to overcome barriers or traps under low-temperature conditions, thereby affecting the conductivity of the semiconductor. This issue is typically investigated using AS.

Monirul et al [28] employed AS to investigate the E1 defect in GaInNAsSb-based solar cell structures and its connection to carrier freeze-out. The steady-state capacitance C displayed three distinct capacitance steps in figure 7(a), while the differential capacitance (dC/dln$\omega - T$) exhibited three peaks corresponding to these steps in figure 7(b), reflecting the electrical response of trap level in the n-GaInNAsSb layer.

To understand the nature of the low-temperature capacitance step in figure 7 (corresponding to the E1 admittance peak)—whether it signifies trap centers or free carrier freeze-out—the authors conducted bias-dependent admittance measurements on the E1 peak, as shown in figure 8. Under reverse bias, the capacitance and conductance of the E1 peak exhibited clear bias dependence: the capacitance decreased from its low-frequency value (C_{lf}) to its high-frequency value (C_{hf}), accompanied by a conductance peak at the capacitance step. As the frequency increased, the capacitance values converged. Importantly, the characteristic frequency of the E1 conductance response was observed to shift to higher values with increasing reverse bias [28]. This behavior excludes the possibility that E1 originates from interface traps, since the response frequency of interface states is expected to decrease as the Fermi level moves deeper under reverse bias [72], which contradicts the experimental results. Instead, based on the derivation of equation (5), the conductance characteristic frequency under carrier freeze-out conditions is proportional to the depletion width. Because reverse bias broadens the depletion region, the corresponding response frequency increases, in agreement with the experimental observations. Therefore, the E1 signal was attributed to carrier freeze-out.

AS analysis further supports this interpretation. The conductance behavior of the E1 peak reflects the capture and
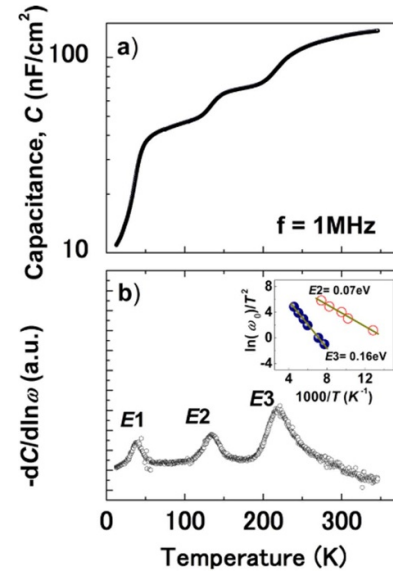

Figure 7. (a) Steady-state capacitance C as a function of temperature, measured under a 1 MHz AC modulation. (b) Differential capacitance spectrum (dC/dln$\omega - T$) showing three characteristic peaks: E1, E2, and E3, with the inset displaying the Arrhenius plots for E2 and E3. Reprinted from [28], with the permission of AIP Publishing.
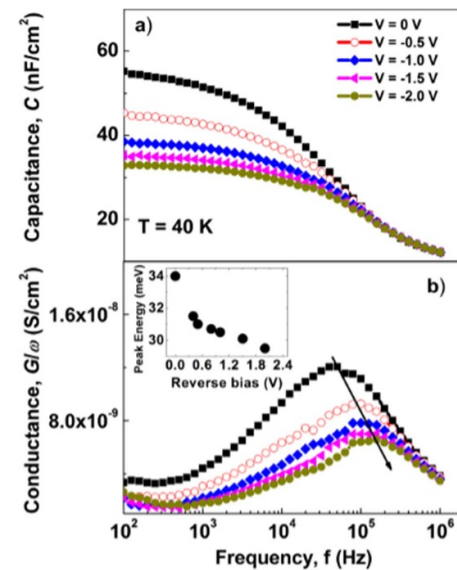

Figure 8. (a) Reverse bias dependence of the E1 peak in the capacitance spectrum at 40 K; (b) normalized conductance G/x as a function of modulation frequency f and the influence of reverse bias, with arrows marking the peak shifts induced by bias. The inset illustrates the bias-induced shift of the E1 peak on the energy scale. Reprinted from [28], with the permission of AIP Publishing.

release of carriers near the intersection of the trap level and the Fermi level. At low frequencies, carriers can follow the AC modulation voltage; however, as the frequency increases, their response lags, leading to a phase delay in the conductance (G) and energy loss. With further increases in frequency, carriers freeze out and can no longer respond, thereby exhibiting the freeze-out effect. At low temperatures, the capacitance is
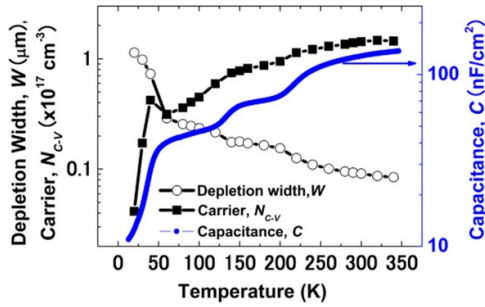
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Figure 9. Temperature-dependent depletion width and the carrier concentration at 0 bias voltage, measured with 1 MHz of frequency. Reprinted from [28], with the permission of AIP Publishing.

primarily ==governed by the depletion capacitance (C_d), and as the frequency increases, the carrier freeze-out effect becomes more prominent, causing== the capacitance to approach the geometric capacitance. The phase lag characteristics observed in the conductance further reinforce the attribution of the E1 peak to carrier freeze-out.

To gain further insights into the E1 peak, the authors present a definitive analysis of carrier freeze-out in the n-GaInNAsSb layer. As the pre-eminent experimental method for characterizing this phenomenon, they monitor the net doping concentration as a function of temperature (figure 9). The data reveals a classic signature of freeze-out: below 50 K, a pronounced drop in carrier concentration NC − V coincides with the turning point in the $C(T)$ curve, while the depletion width (W) progressively increases. This inverse correlation confirms that the carrier freeze-out directly causes an expansion of the depletion region, thereby firmly establishing its connection to the E1 peak. The same information can be extracted by plotting the net doping concentration as a function of measurement frequency at fixed temperatures, as frozen-out carriers cannot respond to high-frequency signals. Together, temperature and frequency dependence form a complete toolkit for rigorously diagnosing this fundamental semiconductor behavior.

Lee *et al* [17] studied three differently sized GaN blue LEDs using AS. The C–f dependence of the 100 μm LED at room temperature shows that the capacitance roll-off begins at approximately 10 kHz, as shown in figure 10(a). Measurements of C–T, G/ω versus temperature T, and the temperature derivative of capacitance dC/dT at different frequencies led the authors to conclude that the observed step phenomenon is related to a freeze-out of states with ionization energy ∼0.06 eV ==(figure 10(b) shows G/ω versus T plots at different measurement frequencies)==. This phenomenon, typically observed in blue GaN/InGaN LEDs, is associated with nitrogen-vacancy states in the GaN barrier layers of the QWs [73]. Below 200 K, the rapid drop in capacitance, attributed to the freeze-out of Mg acceptors, is a common feature of GaN blue LEDs [73–75], with an activation energy of 0.13 eV measured in this temperature range.

Polyakov *et al* [76] investigated standard blue GaN/InGaN multiple QW (MQW) LEDs (reference LED [77, 78]) and LEDs incorporating embedded SiO$_2$ nanoparticles (SiO$_2$-LED) using AS and related methods. As shown in figure 11(a),
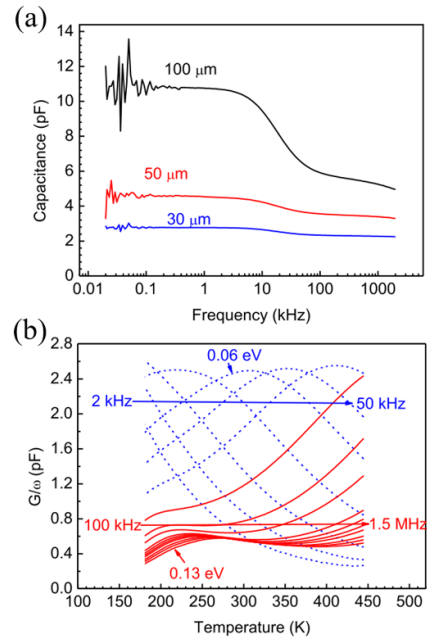

Figure 10. (a) Room temperature C−f characteristics for the three diode diameters. (b) G/ω as a function of temperature for the 100 μm diode. The blue dashed line (2–50 kHz) represents an activation energy of 0.06 eV, while the red solid line (10 kHz–1.5 MHz) corresponds to an activation energy of 0.13 eV. Reprinted from [17], Copyright (2022), with permission from Elsevier.

the C − V curve of the SiO$_2$-LED exhibits a 120 nm shift in the QW peak at 86 K compared to high-temperature data. Temperature-dependent capacitance measurements at various frequencies for both types of LEDs, shown in figure 11(b), reveal that above 150–200 K, the capacitance stabilizes at a plateau, corresponding to a SCR with a thickness equal to the MQW region. At low temperatures, capacitance steps are observed, and AS analysis identifies two distinct steps associated with traps with activation energies of 0.1 eV and 21–27 meV, respectively. The changes in low-temperature capacitance suggest that after these two traps freeze out, the capacitance corresponds to a thickness of 120 nm, closely matching the thickness of the p-GaN layer in the sample. Based on this, the authors conclude that the first step is due to Mg freeze-out, which causes the p-GaN layer to behave as an insulator at high frequencies [79]. Consequently, the position of the QW peak shifts at low temperatures, with a depth approximately corresponding to the thickness of the p-GaN layer.

These findings suggest that Mg freeze-out significantly influences low-temperature capacitance, rendering reliable DLTS measurements infeasible even at the lowest frequency of 10 kHz. This phenomenon gives rise to various complications in the low-temperature segment of DLTS spectra. It begins with the emergence of false quasi-peaks, which are a result of significant capacitance variations with temperature during the temperature sweep. This ultimately leads to the misattribution of peaks observed in DLTS and AS to traps located within the p-type or n-type regions of the diode.
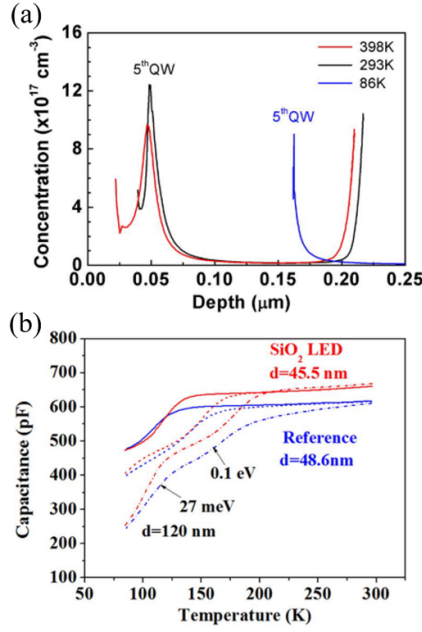
Figure 11. (a) Concentration profiles calculated from C–V characteristics measured on SiO2 LED at 293 K (black line), 398 K (red line), and 86 K (blue line) at 1 MHz. (b) Capacitance as a function of temperature for the reference LED (blue line) and the SiO2 LED (red line). Measurements were performed under a 2 V forward bias at frequencies of 10 kHz (solid line), 100 kHz (dash-dotted line), and 500 kHz (dotted line). © 2016 Polyakov *et al* [76]. Published on behalf of The Electrochemical Society by IOP Publishing Limited.

3.2. The extraction of carrier mobility

Carrier mobility is a critical parameter that quantifies the ability of carriers to move under an applied electric field, providing an accurate representation of their transport properties and playing a crucial role in determining semiconductor device performance. AS is widely employed to extract resistivity and mobility in various semiconductor materials [80–82]. Compared to other techniques, such as the Hall effect [83–85] and the pulsed laser time-of-flight (TOF) method [86, 87], the primary advantage of AS lies in its ability to be directly applied to finished devices, such as solar cells [88, 89].

In the case of dispersive transport, the mobility of charge carriers varies with the electric field or frequency. Sanjoy Paul *et al* [90] employed AS to extract the resistivity, hole mobility, and temperature dependence in the Cu (In, Ga) Se$_2$ solar cells. As shown in figure 12, the C–f plot reveals a step-like transition characterized by an inflection point frequency (ω_p), which appears as a minimum in the $\omega dC/d\omega - f$ curve. Below ω_p, the capacitance C approaches the depletion capacitance $C_d = \varepsilon A/W$, while above ω_p, the semiconductor behaves like a capacitor $C_g = \varepsilon A/t$. The inflection point frequency ω_p can be determined using expression (27) [89, 91].

$$\omega_p = \frac{C_g}{C_d \rho \varepsilon} = \frac{W}{t} \frac{1}{\rho \varepsilon}, \tag{27}$$

where depletion width $W \approx \sqrt{(2\varepsilon(V_{bi} - V)/qN_a)}$, and V_{bi} is the built-in potential, N_a is the acceptor density, determined
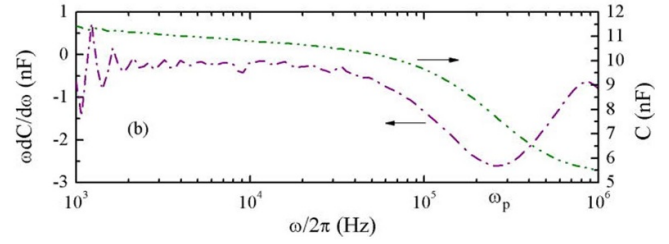

Figure 12. The frequency-dependent capacitance and differential capacitance $\omega dC/d\omega$ spectra used to extract the inflection frequency ω_p. Reprinted from [90], with the permission of AIP Publishing.

through C–V measurements. t is the thickness, ρ is the resistivity

Upon substitution and simplification, the bias-dependent inflection point frequency ω_p for the n^+-p junction can be expressed as:

$$\omega_p^2 = \frac{W^2}{t^2}\left(\frac{1}{\rho\varepsilon}\right)^2 = \frac{2}{q\varepsilon N_a \rho^2 t^2}(V_{bi} - V). \tag{28}$$

Based on equation (28), the ω_p^2 plot is constructed, where the slope is used to determine the resistivity ρ and mobility μ:

$$\rho = \sqrt{\frac{2}{q\varepsilon N_a t^2 \times \text{Slope}}} \tag{29}$$

and

$$\mu = \frac{1}{qN_a\rho} = \sqrt{\frac{\varepsilon t^2 \times \text{Slope}}{2qN_a}}. \tag{30}$$

The authors examined the frequency-dependent capacitance and differential capacitance spectra of CIGS solar cells under various biases at a measurement temperature of 203 K. As shown in figure 13, the results reveal a step-like transition in the depletion capacitance at the inflection point frequency ω_p, with ω_p increasing as the bias voltage rises. This shift is essential for the extraction of resistivity and carrier mobility. Using the linear relationship between ω_p^2 and bias voltage V, the resistivity and mobility of the CIGS solar cell were calculated to be 1.86×10^4 $\Omega\cdot$cm and 0.19 cm^2 V $\cdot$ s, respectively, as illustrated in figure 14(a). Moreover, the impact of temperature on resistivity and mobility was investigated, with results shown in figure 14(b). The analysis indicates an exponential variation in both resistivity and mobility with increasing temperature. Over the range of 133–300 K, the resistivity decreases from 8.21×10^6 $\Omega\cdot$cm to 3.83×10^3 $\Omega\cdot$cm, while the mobility increases from 7.55×10^{-3} cm^2 V^{-1} $\cdot$ s to 4.08 cm^2 V^{-1} $\cdot$ s.

The authors [90] compared the hole mobility obtained by the AS method with the results reported by Dinca *et al* [87] they found that the mobility measured by AS (4.08cm^2 V $\cdot$ s^{-1}) was significantly higher than the value reported by Dinca *et al* using the TOF method (0.6 cm^2 V $\cdot$ s^{-1}). This discrepancy can be partly attributed to the intrinsic challenges of the TOF approach: estimating the transit time of photogenerated charge
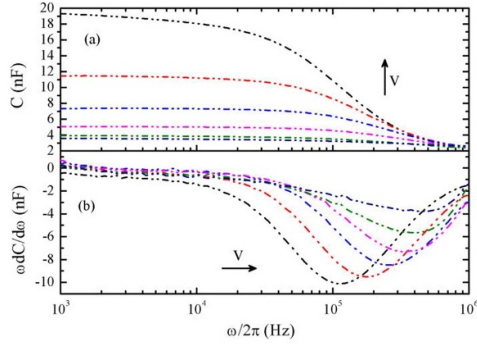
Figure 13. Bias voltage V dependence of capacitance and differential capacitance spectra plotted against the frequency of the CIGS solar cell at $T = 203$ K. The voltage change is from 0.4 to 0.1 V with voltage step $\Delta V = 0.1$ V. Reprinted from [90], with the permission of AIP Publishing.
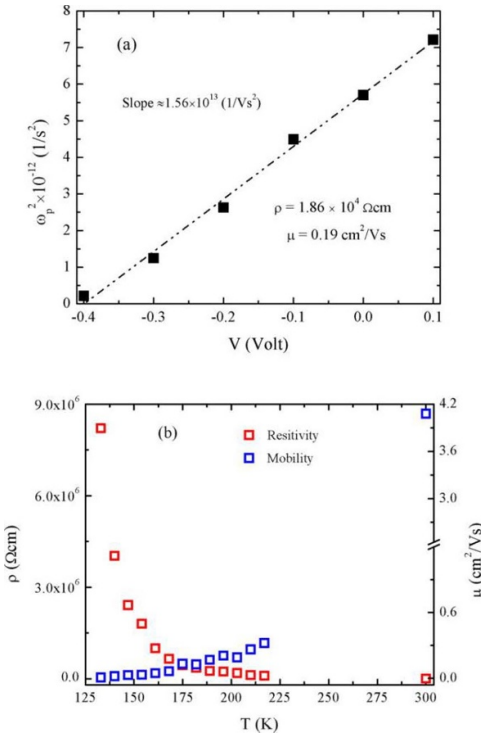

Figure 14. (a) Linear relationship between ω_p^2 and bias voltage V at 203 K for extracting resistivity and hole mobility; (b) temperature-dependent variations of resistivity and mobility within the range of 133–300 K. Reprinted from [90], with the permission of AIP Publishing.

carriers is nontrivial, yet it is the key parameter in evaluating mobility for a given film thickness and electric field. In practice, trapping and multiple-trapping processes occurring during carrier transport can distort the transient signal, thereby reducing the apparent hole mobility. Furthermore, the AS results indicate that hole mobility exhibits a strong temperature dependence, whereas Dinca *et al* reported only a weak temperature dependence. Additionally, the temperature-dependent resistivity and mobility exhibit Arrhenius behavior, with an activation energy of 120 meV. This phenomenon is
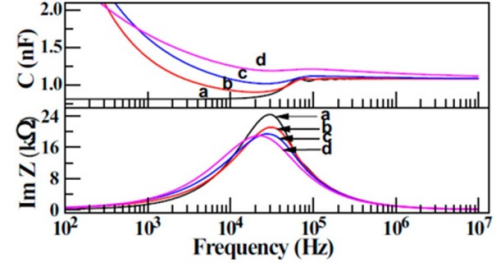

Figure 15. Comparisons of simulated spectra of normalized capacitance C/C_{geo} (top) and the normalized $-Z''$ (here depicted as Im Z) (bottom) versus frequency for increasingly dispersive transport (M, α). Lines: (a) nondispersive, (b) low dispersion, (c) moderate dispersion, and (d) highly dispersive. Reprinted from [97], with the permission of AIP Publishing.

believed to be directly associated with potential fluctuations induced by grain boundaries. The observed potential fluctuation aligns closely with values estimated through optical and microscopy techniques.

In the case of non-dispersive transport, the mobility of charge carriers is considered to be constant and does not change with the electric field or frequency. Martens *et al* [92] introduced a method to extract carrier mobility μ for non-dispersive transport based on the peak position of the negative differential admittance $-\Delta B(\omega) = -\omega(C - C_0)$, as described below [66, 93]:

$$\tau_{\text{dc}} = \kappa \frac{d^2}{(V - V_{bi})\mu_{\text{dc}}}, \qquad (31)$$

where κ is a numerical factor that relates the AC transit time τ_t to an average dc transit time τ_{dc}, i.e. $\tau_{\text{dc}} = \kappa \tau_t$. In the literature, the numerical factor varies significantly across different materials, typically ranging from 0.29 to 0.75 [63, 66, 92, 94–96]. Tsang *et al* [66] found values of $\tau_{\text{dc}} = 0.56\tau_t$ for both dispersive and nondispersive transport. Currently, there is no simple and validated method to accurately determine these factors, except by simulating the peak frequency for a known transit time and then correcting the numerical factor accordingly. It should be noted that these numerical factors originate from non-uniform electric fields in the device; in uniform electric fields, these factors would no longer exist. d is the thickness of the semiconductor layer. The transit time τ_t is obtained by maximizing $-\Delta B$ concerning ω, using the relation $\omega\tau = 1$.

Tripathi *et al* [97] showed that the $-Z''$ spectrum offers a clearer representation of electrical transport characteristics compared to $C(f)$ or $-\Delta B$ spectra, effectively eliminating artifacts in the analysis. Figure 15 compares simulated capacitance spectra and $-Z''$ spectra (denoted as Im Z) for varying degrees of transport dispersion. The mobility can be determined using equation (31).

3.3. Negative capacitance (NC) issue

NC refers to the phenomenon where the capacitance value of a device becomes negative under specific conditions such as frequency, temperature, or bias voltage. This phenomenon has
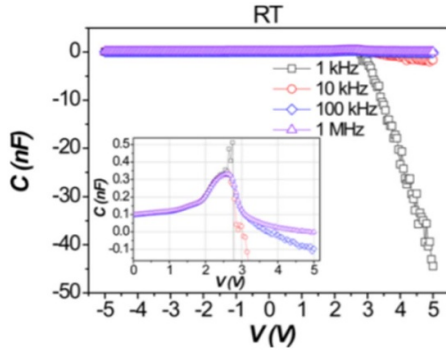
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Figure 16. The frequency-dependent NC of a μLED chip with dimensions of 300 μm $\times$ 300 μm. Reprinted from [103], with the permission of AIP Publishing.

Figure 17. *C*–*V* characteristics of the SiQD-Hex LED measured at AC signal frequencies between 200 Hz and 1 MHz. © 2022 IEEE. Reproduced from [102]. CC BY 4.0.

Figure 18. (a) Frequency-dependent capacitance of the polymer LED plotted as a function of bias voltage, (b) double-logarithmic plot of the negative differential susceptance $-\Delta B(\omega) = -\omega(C{-}C_0)$ of a PLED ($L = 150$ nm) at $V{-}V_{bi} = 0.3$ V for two temperatures. Reprinted from [92], with the permission of AIP Publishing.

garnered increasing attention in the study of admittance spectra of p–n junction devices [98–100]. Although the physical origin of NC is still controversial, a widely accepted mechanism involves trap-assisted recombination, where the delayed replenishment of charges in sub-bandgap states leads to a phase lag between current and voltage, thereby producing the NC effect [101, 102]. It not only reveals the internal electrical characteristics of the device but also provides a crucial theoretical basis for optimizing device performance.

The NC phenomenon typically exhibits significant frequency dependence. At low frequencies, the NC effect is more pronounced, while it gradually weakens at high frequencies. Bourim *et al* [103] found that in InGaN/GaN MQW blue LEDs, the NC decreases to deep negative values with decreasing frequency, as shown in figure 16. Mock *et al* [102] investigated the NC phenomenon in silicon quantum dot LEDs (SiQD-LEDs) through frequency scanning and found that the NC value decreases with increasing modulation frequency, as shown in figure 17, because deeper trapped charges cannot follow high-frequency AC signals. Martens *et al* investigated the capacitance frequency dependence of polymer LEDs (PLEDs) through AS, and they also found that the NC phenomenon weakens with increasing frequency, as shown in figure 18(a). Due to the finite relaxation time τ_r, NC is more pronounced at low frequencies and gradually disappears with increasing frequency. Furthermore, in figure 18(b), the authors revealed the frequency characteristics of the NC phenomenon by plotting the differential magnetization curves $-\Delta B(\omega) = -\omega(C{-}C_0)$ for PLEDs and hole-type devices. Two distinct relaxation peaks were observed in the frequency response of the PLED device: the high-frequency peak corresponds to hole migration, while the low-frequency peak corresponds to electron migration. This indicates that in PLEDs, holes play a dominant role in charge distribution due to their significantly higher mobility compared to electrons.

The NC is affected by the forward bias voltage through the regulation of the carrier injection and recombination processes. Bourim *et al* [103] found that the NC of InGaN/GaN LEDs increases with increasing forward bias voltage, as shown in figure 16. Martens *et al* [92] found that at zero bias, the capacitance of PLEDs is almost unaffected by frequency and
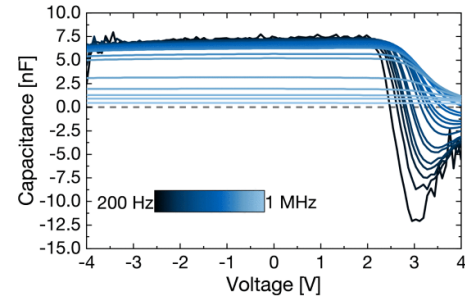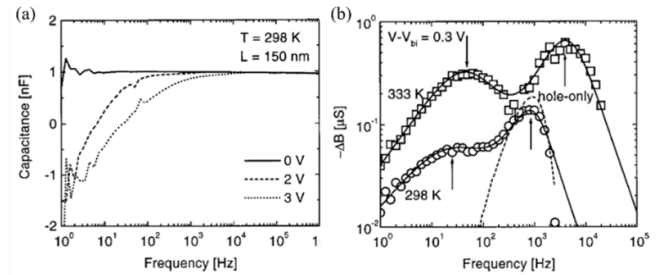
is equal to the geometric capacitance $C_0 = \varepsilon A/L$, as shown in figure 18. However, under applied bias, a NC contribution develops and exhibits a frequency shift toward higher values as the bias increases. Bisquert *et al* [104] also investigated the NC phenomenon of PLEDs through AS. When the bias voltage changes, electrons are first injected into the polymer bulk through interface states step by step. Due to the thermodynamic nonequilibrium state between the interface states and the metal Fermi level, this process induces a significant NC phenomenon in the low-frequency range.

Temperature variations significantly alter NC behavior by modulating the thermal motion of charge carriers and the activity of trap states. Bourim *et al* [103] found that as the temperature rose from -190 °C to room temperature, the NC amplitude of InGaN/GaN LEDs increased markedly, as shown in figure 19. However, this temperature dependence was only evident at low frequencies below 10 kHz. As the frequency increased, the influence of temperature on the NC became relatively minor, as shown in the inset of figure 19. They also discovered that under high injection current, the normalized value of NC exhibited dispersion with increasing chip area. Yet, after correcting for R_s, NC became independent of the area, as depicted in figures 20(a) and (b). The authors believe that the inductive process giving rise to NC is uniformly distributed throughout the device area, with no localized conductive paths. Without correction, the observed differences in the normalized NC distribution in the low-frequency region could be explained by the self-heating effect of the LED p–n junction.
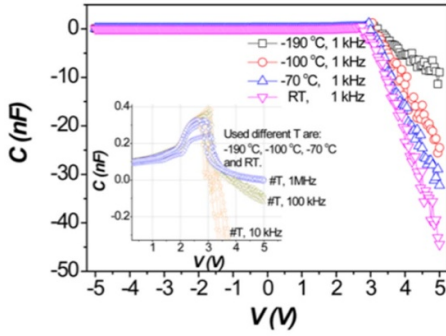
Figure 19. The temperature-dependent NC of μLED chips measured under a 1 kHz AC signal is shown, with the inset illustrating the temperature independence of NC with increasing frequency. Reproduced from [103], with permission from Springer Nature.
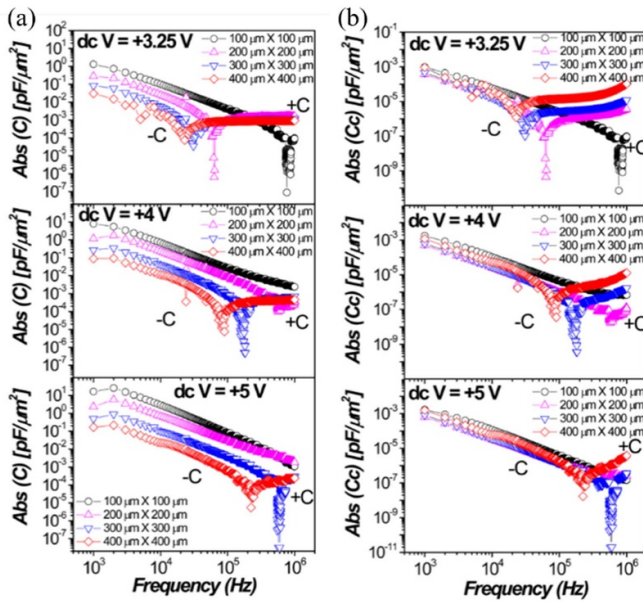

Figure 20. (a) Absolute normalized capacitance and (b) absolute corrected normalized capacitance versus frequency for μ-LED chips with different areas under various DC biases. Reproduced from [103], with permission from Springer Nature.

For large-area LED chips, the self-heating temperature caused by the injected current is higher, leading to carriers escaping from the QWs to the quasi-neutral region of the semiconductor [105, 106]. The temperature scanning experiment conducted by Mock *et al* [102] showed that as the temperature increased, the amplitude of NC in SiQD-LEDs decreased and the C–V curves shifted to the left overall, as illustrated in figure 21. They attributed this trend to the Poole-Frenkel emission effect driven by temperature, which caused free charge carriers to escape from the quantum dots, reducing the number of charge carriers available for radiative recombination. This, in turn, led to a decrease in electron-hole recombination and a reduction in the NC signal.

When discussing the relationships between factors such as frequency, temperature, and voltage with NC, various research teams have also presented their own hypotheses. Bourim *et al*
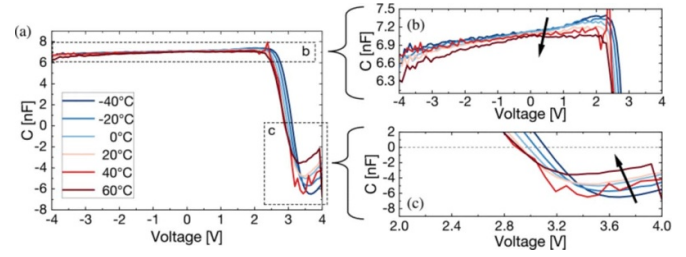

Figure 21. (a) C–V characteristics of the SiQD-Hex LED measured at various temperatures with a fixed AC signal frequency of 1 kHz. (b) Magnified view of the reduction in the positive capacitance peak. (c) Magnified view of the decrease in NC, with the gray line representing 0 nf. © 2022 IEEE. Reproduced from [102]. CC BY 4.0.

[103] presented a mechanism to explain the inductive process in the p–n junction of LEDs, which is attributed to the difference in the mobility of charge carriers (electrons/holes) in the active region of the MQW-LED device. This difference leads to a monotonic change in the recombination rate of electron-hole pairs. Since electrons have higher mobility and can quickly enter the conduction band of the QW, while holes respond more slowly, the recombination process becomes dependent on the response time of holes, thereby exhibiting an inductive conduction process. This mechanism is similar to the frequency-dependent characteristics of minority carriers in MOS structures [107]. Mock *et al* [102] attributed the NC phenomenon in SiQD-LEDs mainly to trap-mediated recombination processes, in which charges from defect sub-bandgap states contribute to recombination. However, due to the insufficient replenishment rate, current flows to re-establish equilibrium, lagging behind the applied voltage and exhibiting an 'inductive' characteristic, which results in the NC phenomenon. Martens *et al* [92] observed that in PLEDs, the reorganization of holes in the space-charge distribution with increasing bias is affected by hysteresis, leading to an 'inductive' characteristic, namely, the NC phenomenon. Bisquert *et al* [104] proposed a kinetic model to explain this phenomenon, suggesting that NC primarily originates from the stepwise injection process of interface states in a non-equilibrium condition. As the voltage changes, electrons in the interface states gradually inject into the bulk material, causing the current to lag behind the voltage and exhibit an inductive characteristic, i.e. the NC phenomenon.

4. Conclusion

This tutorial provides a systematic overview of the application of AS in defect characterization of p–n junction devices, with illustrative examples of its utility in analyzing defects in optoelectronic devices such as solar cells, LEDs, and LDs. A detailed comparative analysis between AS and DLTS is presented, emphasizing the superior high-frequency sensitivity of AS and its broader applicability across diverse device architectures. Additionally, an equivalent circuit model for p–junctions is proposed, incorporating the influence of R_s, which

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facilitates precise extraction of critical electrical parameters in semiconductor device characterization.

The study comprehensively addresses key challenges in semiconductor research through AS methodologies, including dopant freeze-out phenomena under low-temperature conditions, accurate extraction of carrier mobility, and identification of the origins of NC—persistent issues that have hindered progress in semiconductor device optimization. By elucidating these challenges, the discussion not only deepens the mechanistic understanding of AS techniques but also expands their potential applications. These advancements offer robust theoretical and practical foundations for advancing defect characterization in semiconductor devices, ultimately contributing to performance enhancement strategies for next-generation electronic and optoelectronic technologies.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

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