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Defect Analysis in Semiconductor Materials Based on p-n Junction Diode Characteristics

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Abstract. This paper aims at reviewing the possibilities of using p-n junction diodes for lifetime and defect analysis in semiconductor materials. In a first part, the theoretical basis of lifetime extraction based on p-n junction current-voltage and capacitance-voltage characteristics will be discussed. In the next parts, these methods will be applied to different cases relevant for advanced semiconductor materials and device processing. First, the impact of the initial interstitial oxygen content and thermal pre-treatment of Czochralski silicon substrates on the carrier generation and recombination lifetime is discussed. A comparison will also be made with epitaxial and Float-Zone silicon. In a next part, the impact of proton-irradiation damage on the diode behavior will be presented. In the final part, the application of the technique on SiGe and Ge based p-n junctions is described. Whenever possible and useful, the information extracted from p-n junction characteristics will be compared with direct lifetime measurements using microwave techniques. Additional defect information has also been gained from other well-known techniques like Deep-Level Transient Spectroscopy (DLTS), Electron-Beam-Induced Current (EBIC), etc and will be correlated with the p-n junction results. The review is wrapped up in a summary followed by an outlook on future evolution and requirements.

Introduction

Since the early days of semiconductor electronics, it is well-known that the presence of defects has a key impact on the electrical and optical properties. Especially in a material with an indirect band gap (E_g), like silicon or germanium, deep levels assist in the generation or recombination of carriers through different mechanisms, schematically represented in Fig. 1. This is an uncontrolled source of charges and current, giving rise to excess noise (fluctuations), a decreased carrier lifetime and diffusion length and unwanted leakage current in, e.g., a p-n junction. The origin of such defect levels is manifold and their control during wafer and IC production mandatory in order to achieve acceptable device yields. On the other hand, for certain applications a short carrier lifetime is desirable. This has led to the discipline of defect engineering, which is the science – sometimes still considered more an art – of the controlled introduction of well-defined defects at specific sites in the semiconductor device structure or at critical process steps. Its mirror image, namely, the controlled and permanent removal of electrically active defects from active regions is termed gettering.

It is clear from the foregoing that techniques to monitor and, if possible, identify deep levels are an essential part of successful yield engineering and processing. As will be shown below, one of the most sensitive probes for electrically active defects is the leakage current – and in general, the current-voltage (I-V) characteristic - of a p-n junction. The main advantage is that it is a relatively fast and simple technique, based on a device structure which is well understood. It is in fact one of the standard test structures available during the development of front-end process modules, since source and drain junctions are an essential part of the Metal-Oxide-Semiconductor (MOS)

transistor. When analyzing the reverse or leakage current of a p-n junction, one typically monitors the defects in the bulk depletion region with width W_A or at the surrounding surface (depletion width W_P) (Fig. 1). These are the relevant centers for transistor operation. At the same time, the forward or reverse I-V characteristic can also be used for the analysis of the minority carrier diffusion length (L_n or L_p) or of the recombination lifetime (τ_n or τ_p). This generally carries information over a much larger region in the substrate, beyond the active device region (depletion depth). In this way, a p-n junction can also be employed for semiconductor materials studies. Drawbacks of the p-n diode technique are its "destructive" nature in the sense that a number of processing steps are required which by themselves can introduce defects or alter the electrical material properties and the fact that it is basically a non-spectroscopic technique, i.e., it is difficult if not impossible to identify the responsible generation-recombination (GR) centers. However, the same remark goes for the other sensitive electrical techniques, like, lifetime measurements, Hall effect versus temperature, or even Deep- Level Transient Spectroscopy (DLTS), which in spite of its name is to be considered a quasi-spectroscopic technique. Nevertheless, also I-V measurements can provide us with some information on the defect parameters – the concentration N_T (in cm^{-3} for bulk traps), the energy level E_T and the capture cross section for electrons (σ_n) or holes (σ_p) – under certain experimental conditions.

In the following, the physics of the diode analysis technique is outlined first and next illustrated by different examples. For the basic p-n junction theory, the Reader is referred to the literature [1,2].

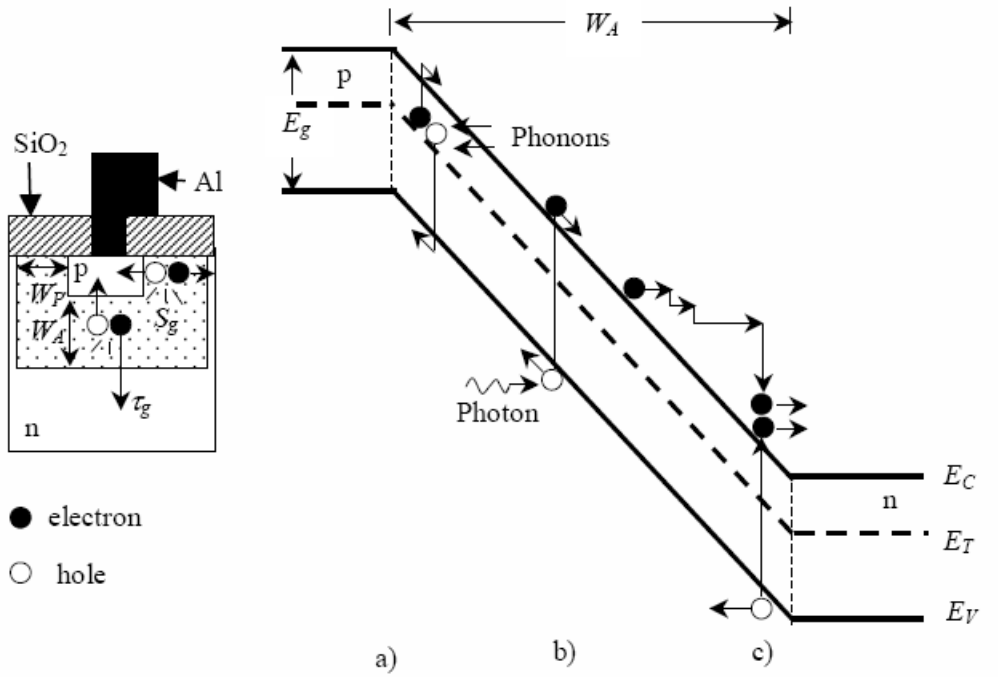


Fig. 1. Reverse biased junction with generation-recombination mechanisms: a) multi-phonon generation via generation-recombination (GR) centers; b) optical electron-hole pair (ehp) generation; c) impact ionization. E_V and E_C are the top of the valence band and the bottom of the conduction band, respectively. S_g is the surface generation velocity and τ_g the generation lifetime.

Theoretical basis and principles of the p-n junction techniques

In this section, the theory of the non-ideal p-n junction with defect levels is summarized, based on the Shockley-Read [3] and Hall [4] theory, often termed SRH theory (see also Ref. [5]). It relies on the depletion approximation and in the first instance considers only thermal carrier transitions, i.e., the phonon transitions labeled a) in Fig. 1. Moreover, one assumes GR processes in the substrate

only, which is acceptable for a large-area, deep diffused junction. For state-of-the-art planar, shallow junctions, used in ULSI technology, one should also account for the contribution of the peripheral (or lateral) depletion region and surface (interface) states to the diode current, as already indicated in Fig. 1. As is discussed below, it is possible to separate these different geometrical components by combining measurements on junctions with different perimeter (P) to area (A) ratio. Finally, ways to separate the physical components – the ideal, diffusion and the non-ideal, defect-related current – are pointed out.

SRH Theory for a One-Dimensional p-n Junction. The current-voltage characteristic of a one-dimensional p-n junction can in good approximation be written as follows:

$$I = \left[\frac{Aqn_i W_A}{2\tau_r \exp\left(\frac{qV}{2kT}\right) + \tau_g} \right] \left[\exp\left(\frac{qV}{kT}\right) - 1 \right]. \quad (1)$$

In Eq. (1), q is the elementary charge, T the absolute temperature and k Boltzmann's constant. The intrinsic carrier concentration, n_i, is given by [1]:

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{kT}\right). \quad (2)$$

N_C and N_V are the effective density of states in the conduction and valence band. At 300 K, n_i equals 10^{10} cm^{-3} for Si [6] and $2 \cdot 10^{13}$ cm^{-3} for Ge.

In reverse operation for an applied bias V >> kT/q, Eq. (1) readily reduces to the well-known expression for the reverse generation current:

$$I_{gen} = \frac{Aqn_i W_A}{\tau_g}. \quad (3)$$

From this follows immediately that the reverse current of a diode increases linearly with the depletion width W_A and inversely proportional with the generation lifetime τ_g. For an abrupt, asymmetric junction, W_A is found from the depletion approximation [1]:

$$W_A = \sqrt{\frac{2\varepsilon_S (V + V_{bi})}{qN_{dop}}}. \quad (4)$$

In Eq. (4), ε_S is the permittivity of the semiconductor substrate, V_{bi} the built-in potential and N_{dop} the doping density of the lowly doped substrate. Equivalent expressions can be found in the literature for symmetric abrupt junctions, i.e., where the doping density of the n- and p-type regions are comparable [1,2]. In practice, the depletion region can be derived from the measured differential capacitance of a reverse-biased junction, through $W_A = C/A\varepsilon_S$. Note that Eq. (4) predicts a $\sim\sqrt{V + V_{bi}}$ bias dependence of the reverse generation current of a lowly doped substrate. For higher N_{dop} values, above ~10^{16} cm^{-3} typically, the maximum electric field in the junction becomes sufficiently high for field-assisted carrier generation mechanisms to become important [7-9]. This is for example the case for CMOS source/drain junctions that are typically fabricated in a highly doped well region and a dedicated treatment can be found in Ref. [10].

When the reverse bias is not much higher than kT or for higher temperatures, the ideal diode current may not be negligible compared with the thermal generation current. In that case, one can write for the reverse current:

$$I_R=I_{diff}+I_{gen}. \quad (5)$$

I_{diff} is the saturation value for the ideal diffusion current, which is given by [1,2]:

$$I_{diff} = Aqn_i^2\left(\frac{D_n}{L_nN_A}+\frac{D_p}{L_pN_D}\right). \quad (6)$$

In Eq. (6), N_A and N_D are the doping density in the p- and n-side of an abrupt junction, assumed to be uniform. The diffusion length is related to the diffusion coefficient through the relation $L=\sqrt{D\tau}$, with τ the minority carrier lifetime (electrons in p-type; holes in n-type region). For an asymmetrical p-n junction, i.e. $N_A<<N_D$ or $N_D<<N_A$, one of the terms in Eq. (6) can be neglected so that I_{diff} is inversely proportional to the minority carrier diffusion length or to $\sqrt{\tau}$. In other words, from the saturation diffusion current one can in principle extract the minority carrier lifetime in the substrate. A procedure to separate I_{diff} from a reverse I-V characteristic will be outlined below.

It should, finally, be remarked that Eq. (6) predicts no bias dependence. In other words, if the reverse current is not varying with bias, this indicates the dominance of the ideal diffusion current. Moreover, I_{diff} appears to be thermally activated in the first instance, with activation energy given by E_g. Therefore, for a good-quality silicon diode, the reverse current at higher temperatures, typically above 50°C starts to become dominated by the diffusion current.

Connection with Defect Parameters. The generation and recombination lifetime can be expressed in the following way [11,12]:

$$\tau_g = 2\tau_r \cosh[(E_T-E_i)/kT]. \quad (7)$$

In Eq. (7) E_i is the intrinsic level position ~$E_g/2$. It is clear that from Eq. (7) follows that when $E_T \neq E_i$
τ_g is higher than $2\tau_r$ (recombination lifetime). In addition, substitution in Eq. (7) shows that the generation current is thermally activated with activation energy E_T or E_g-E_T. This implies that from the activation energy of the generation current, one can in principle derive a value for the trap level position, with respect to mid gap. Unfortunately, as most common metal contaminants give rise to deep levels close to the middle of the band gap in Si [13] or Ge [14] this generally leads to a value E_T~$E_g/2$, without the possibility to identify the responsible centers. A combination with other techniques, like DLTS is then necessary to identify the deep levels.

The recombination lifetime in case of low carrier injection, also called minority carrier lifetime, is given by:

$$\tau_r=\tau_n=1/N_T\sigma_n v_{thn} \qquad \tau_r=\tau_p=1/N_T\sigma_p v_{thp}. \quad (8)$$

In Eq. (8), v_{thn} or v_{thp} are the thermal velocity of electrons and holes, respectively. This is in the range of 10^7 cm/s at 300 K for both Ge and Si [1]. As mentioned before, τ_r can be derived from the saturation diffusion current. Unfortunately, only the $N_T\sigma$ product can be found from that, so that additional information coming from other techniques is required for defect identification and/or parameter extraction. Combining measurements of the diffusion current on a p^+-n and n^+-p junction

should in principle yield the σ_p/σ_n ratio, provided the same trap density (and level) dominates the low-injection lifetime.

On the other hand, if τ_g and τ_r can be derived from the generation and diffusion current, respectively, their ratio corresponds to $2\cosh(E_T\text{-}E_i/kT)$ according to Eq. (7). In other words, from this, one can try to estimate the energy position of the GR centers, provided they dominate both the generation and recombination lifetime in the p-n junction.

Finally, a useful quantity is the generation current per defect center, given by:

$$I_{defect} = \frac{qn_i\sigma_{n,p}v_{thn,p}}{2\cosh\left(\frac{E_T - E_i}{kT}\right)}. \qquad (9)$$

This expression allows to estimate the leakage current activity of a known impurity [13,15]. In this way, it is possible to identify substitutional Fe, Ni and most likely also Co as very efficient leakage current generation centers in germanium [15].

Separation of Physical Leakage Current Components. A simple technique to separate the diffusion from the generation current has been proposed by Murakami and Shingyouji [16] and is schematically represented in Fig. 2. It is valid for a p-n junction obeying the simple SRH theory (Eqs (2) to (5)). As shown in Fig. 2, the combination of an I-V and a high-frequency C-V on the same junction eliminates the bias voltage and yields the graphical representation of Eq. (5). From the slope of the linear fit, the generation lifetime can be extracted while the intercept gives the saturation diffusion current. The current density is given by J=I/A. This is valid as long as the generation lifetime (or near mid gap defect concentration) is constant with depth. If this is not the case, the derivative of J with respect to the depletion depth, i.e., $\partial J/\partial W_A$ should give an idea of the τ_g or N_T profile [10,17].

The saturation diffusion current can also be derived from the ideal part of the forward current, by extrapolation to 0 V, as pointed out before [18]. Corrections have been proposed for the diode geometry and ideality factor $m \neq 1$, leading for the saturation diffusion current density to [18]:

$$J_{diff} \approx \frac{0.5m}{1-0.5m} J_{A0} \qquad (10)$$

J_{A0} is the forward volume current density extrapolated from the exponential part of the forward I-V characteristic, corrected for the peripheral component, as will be outlined below. In this way, the recombination lifetime can be extracted [18,19].

It has, finally, been pointed out that by a graphical representation of Eq. (1) for not too high forward bias, one can derive both lifetimes simultaneously [20]. An example for a silicon p-n junction on a Czochralski (Cz) grown wafer with a high initial interstitial oxygen (O_i) density is given in Fig. 3. It clearly demonstrates the much higher generation lifetime compared with the recombination lifetime.

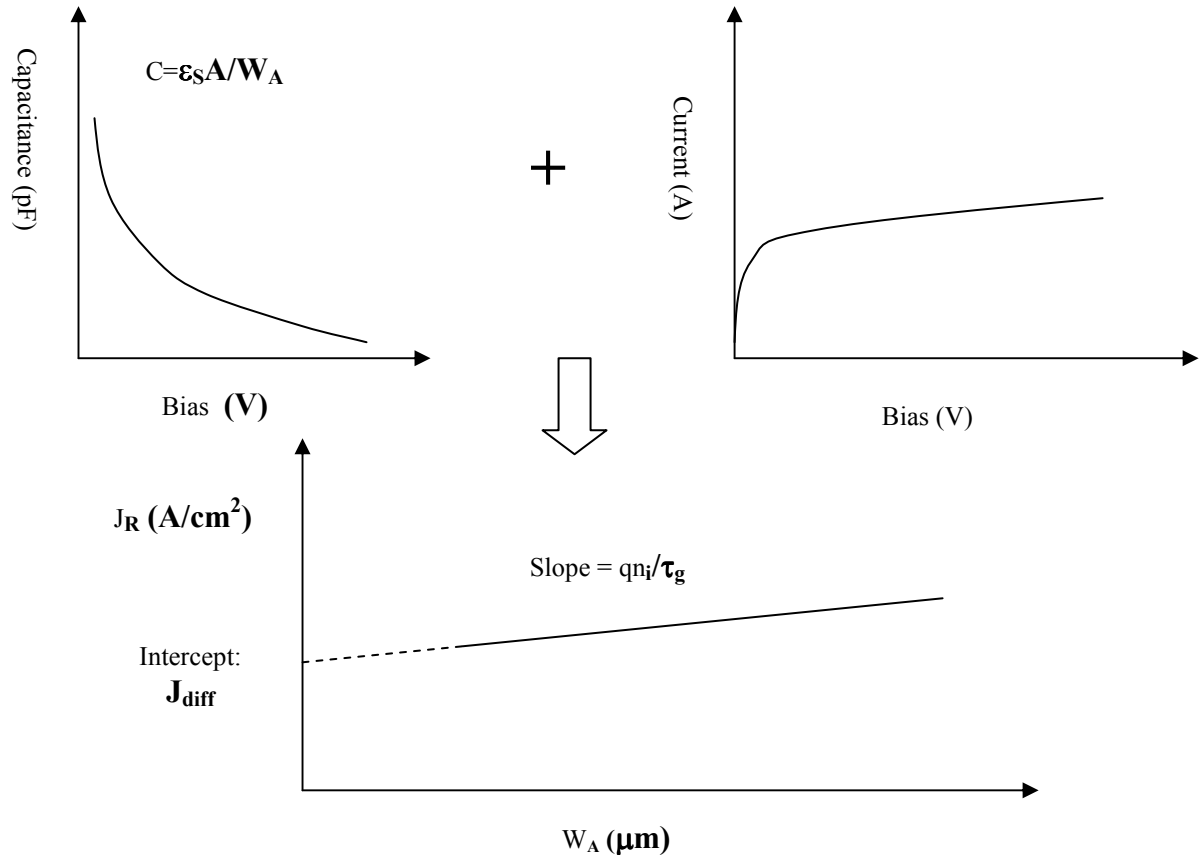


Fig. 2. Schematic representation of the separation method based on a reverse I-V and C-V measurement on a p-n junction.

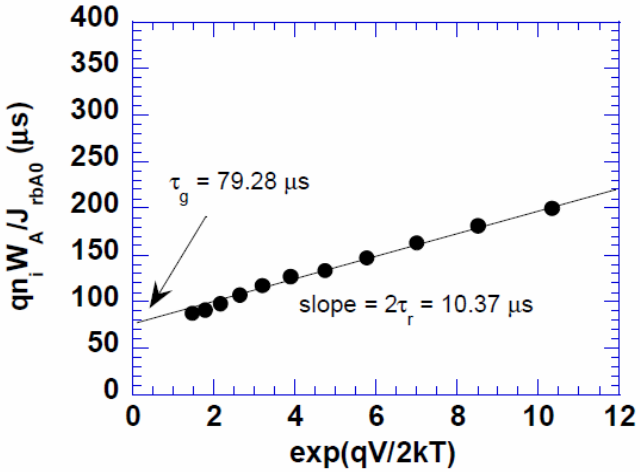


Fig. 3. Simultaneous extraction of the generation and recombination lifetime in an n^+-p junction fabricated in a low void density and high interstitial oxygen concentration Cz silicon substrate (after Poyai *et al.* [20]).

Geometrical Current Components in Planar p-n Junctions. As indicated in Fig. 1, the leakage current through a p-n junction is not only determined by the vertical carrier flow but also by a lateral contribution that is usually governed by surface generation through interface states. In the case of silicon, passivation of the surface is usually accomplished by growth of an SiO_2 layer giving low densities of interface traps N_{sT} (cm^{-2}). A similar expression like Eq. (1) for bulk GR can be established for the peripheral current component, yielding:

$$I = \frac{A_s q n_i S_r \left[\exp\left(\frac{qV}{kT}\right) - 1 \right]}{2\left[\exp\left(\frac{qV}{2kT}\right) + \cosh\left(\frac{E_{sT} - E_i}{kT}\right) \right]}. \quad (11)$$

In Eq. (11), $A_s=PW_p$ is the area where interface state generation occurs, E_{sT} is the energy level and S_r the surface recombination velocity (in cm/s). The latter parameter is again given by $S_r=N_{st}v_{th}\sigma_s$ and related to the surface generation velocity through:

$$S_g = \frac{S_r}{2\cosh\left(\frac{E_{sT} - E_i}{kT}\right)}. \quad (12)$$

A shallow planar p-n junction with area A, perimeter P and number of corners n_C will have different geometrical components which add up to the total forward or reverse current. This means that the following equation is valid:

$$I=AJ_A+PJ_P+n_CI_C+I_{par}. \quad (13)$$

In Eq. (13), J_A, J_P and J_C are the area (A/cm^2), the perimeter (A/cm) and the corner current density (A/corner), respectively. I_{par} is a parasitic component, related to the measurement system. One popular way to separate the different geometrical components is by measuring different adjacent p-n junctions on the same test chip and combining the measured I–V characteristics assuming that the current densities are uniform within the structures. This can be performed numerically, by solving a set of four equations for four diodes. If corner and parasitic components can be neglected one can rely on a simpler graphical approach combining the area current densities at a specific bias, i.e., J=I/A versus P/A for different geometries. The slope yields J_P and the intercept gives J_A for the set of diodes under study. An example is given in Fig. 4, for a reverse bias V_R=-1 V.

Regarding the size and shape of the test structures, one should keep in mind the detection limit of the measurement system. Assuming that a reverse current of the order of 1 pA can be reliably measured and for a typical leakage current density in the range of 1 nA/cm^2 (silicon), one arrives at a minimum area in the range of 10^{-3} cm^2, i.e., 10^5 μm^2. This means that for the evaluation of high-lifetime substrates rather large area p-n junctions are required. A large perimeter structure can be obtained by connecting several fingers together (finger- or comb-structure). The number of corners can be enhanced by measuring several small square diodes in parallel.

Separation of Surface from Bulk Components Using a Gated Diode. Instead of using a variety of structures, with the risk of local process variations, it is also possible to employ a single structure for analyzing both the bulk and surface generation currents. This can be achieved by using a gated diode [21,22], schematically represented in Fig. 5, whereby the n^+-p junction is surrounded by a region gated by a thin SiO_2 layer. Usually, the p-n junction is biased at a fixed reverse or forward voltage, while the gate is swept from accumulation to inversion. It means that in the case of a p-type substrate, the gate bias starts from sufficiently negative bias to accumulate the holes at the surface. In this way, the effect of carrier generation by surface states at the thin-SiO_2/Si interface is canceled by the high hole density, so that no lateral current is generated. In this case, only bulk generation current, described by Eq. (3), is collected at the contacts.

Gradually changing V_G to more positive values repels the holes from the surface and causes a depletion of the surface region. Carrier generation at and near the peripheral interface will start to

contribute to the peripheral leakage, giving rise to an increase of the total reverse current, as depicted by the measurement of Fig. 6 [23].

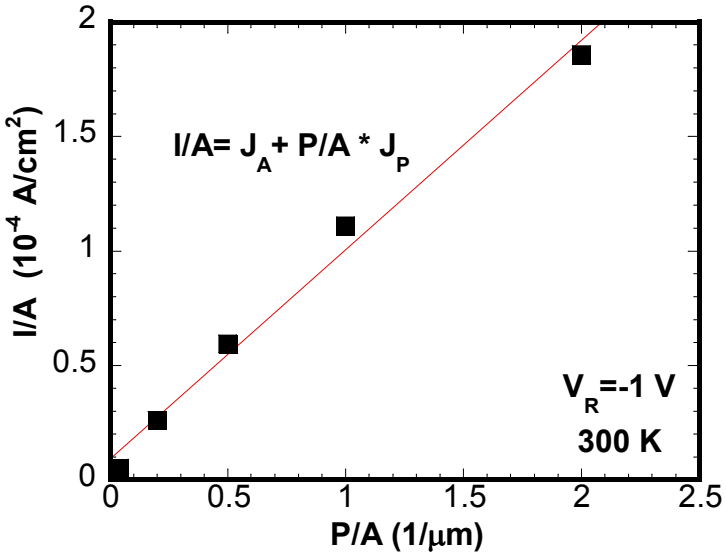


Fig. 4. Current density (■) versus P/A ratio at V_R=-1 V and 300 K for a set of different geometry recessed $Si_{0.8}Ge_{0.2}$ p^+-n junctions, with a recess and junction depth of 70 and 80 nm, respectively. The line is a least-squares fit through the data points.

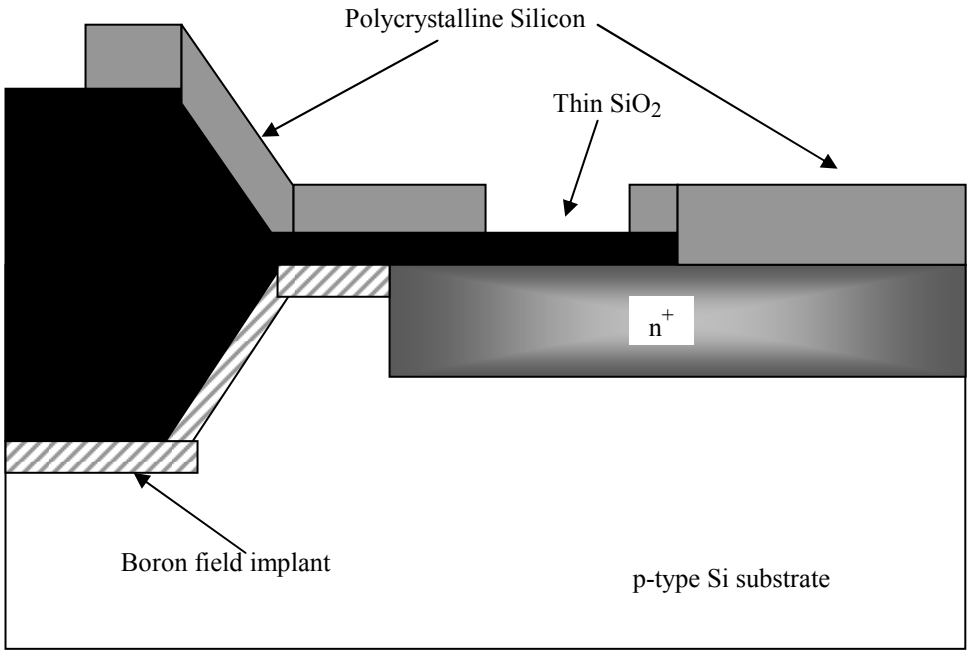


Fig. 5. Schematic representation of a gated n^+-p diode in a p-type silicon substrate. The boron field implantation is employed to avoid surface inversion by the fixed positive charge in the thick SiO_2 field-oxide region.

As a result, a step-like increase in the collected reverse (or forward) current is obtained. The decrease in the current for a gate bias near 0 V can be explained by the fact that the SiO_2/Si interface becomes inverted, whereby a high density of electrons now screens the surface-state generated

carriers from the substrate. A higher reverse current than in accumulation is observed, since the generation area now includes also the gated region, with area A_s [21-23].

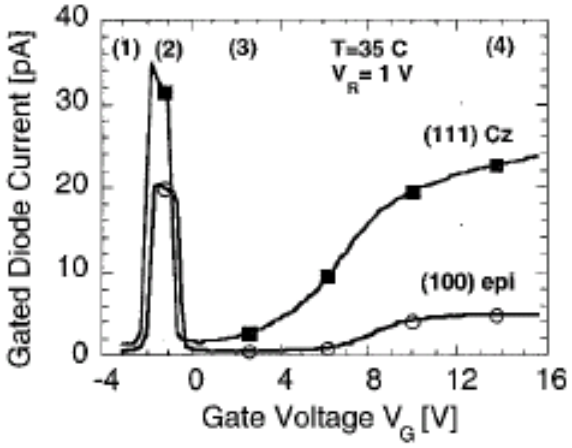


Fig. 6. Four current regimes for a gated diode: the interface under the "thin-oxide" gate is: (1) in accumulation; (2) in depletion; (3) in inversion, respectively, and (4) thick-oxide interface is in depletion. Different ratios for the "thin" and "thick" gated-diode currents are observed for (111) Cz and (100) epitaxial Si diodes, measured at V_R=1 V and T=35 ^oC (after Czerwinski *et al.* [23]).

The generation current at V_R can be derived from region (1) or (3) in Fig. 6, accounting for the appropriate area. The surface generation or recombination velocity then follows from the step amplitude (region (2)), according to equation [21,22]:

$$I_{gen,s} = qn_iA_s\, S_g = qn_iA_s(\pi/2)\sigma_s v_{th}(kTD_{Ts}). \quad (14)$$

In Eq. (14), D_{Ts} is the surface-state density per unit of energy and area (in $eV^{-1}cm^{-2}$). That both methods, i.e., the single-junction gated-diode and the multiple-junction variable geometry technique are compatible with each other is demonstrated by the results of Fig. 7, obtained on n^+-p junctions fabricated in different Si starting materials [23]. As pointed out, the peripheral current of a standard p-n junction, surrounded by thick field oxide is more closely related to the gated-diode current in region (4) of Fig. 6 [23]. Moreover, it has been demonstrated that this feature can be exploited to analyse the peripheral and corner leakage current associated with the field isolation [24,25]. In addition, the method has been applied to the study of neutron-irradiation defects in silicon gated diodes [25]. It is also evident from Fig. 7 that (111) substrates yield a higher surface generation current than (100), which can be ascribed to the 3 times higher density of interface states at the (111) SiO_2/Si interface compared with the (100) orientation [26].

Lifetime and defect analysis in silicon p-n junctions

In this section some of the proposed p-n junction methods are applied to diodes fabricated in silicon substrates. Examples will be given where the substrate quality – albeit after diode processing – is evaluated. In other cases, processing or operation-induced defects can be analyzed.

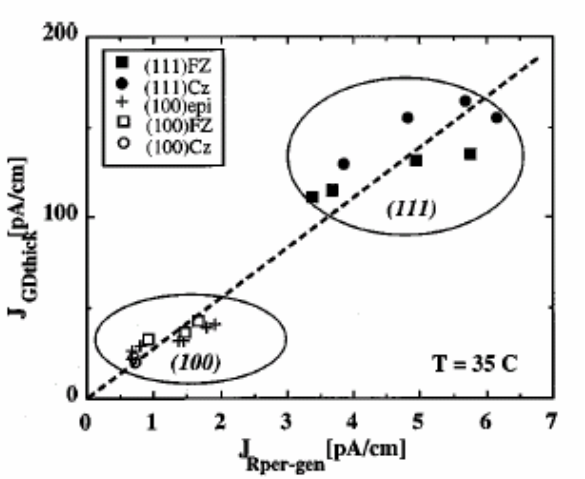


Fig. 7. The peripheral reverse generation current density J_{Rper_gen} for a standard p-n junction *vs* the gated diode current density at depletion under the thick oxide $J_{GDthick}$, for different silicon substrates. The gated diode current, measured at 35°C, is normalized by subtraction of the current at inversion under the thin gate (after Czerwinski *et al.* [23]).

Substrate Effects. In many practical cases, processing is performed on silicon material with non-uniform electrical parameters. This is schematically represented in Fig. 8 for an Internally Gettered Czochralski (IG Cz) and an epitaxial (epi) silicon wafer. An IG Cz wafer is characterized by a thin (~10 μm) defect-lean Denuded Zone (DZ) close to the front and back surface and by a defective region in the interior of the material (Fig. 8a). The bulk defects consist of oxide precipitates and associated secondary extended defects like stacking faults and dislocation loops. In the second case, a lowly doped epitaxial p-type layer, typically, a few μm up to 10 μm thick is deposited by Chemical Vapor Deposition (CVD) on a highly doped p^+ substrate (Fig. 8b). In both cases, the lifetime will be non-uniform and depends on the properties of the different layers and their interfaces. The resulting expression for the diffusion current I_{diff} becomes quite complicated and can in first approximation be represented by [27]:

$$J_{diff} = qD_n \frac{n_i^2}{N_A L_n} F_d \,. \tag{15}$$

Equation (15) is valid for an asymmetric n^+-p junction, where F_d is a correction factor depending on the electrical properties of the different layers and interfaces.

Under certain assumptions, a simple expression can be developed for F_d, namely, when the interface recombination and the difference in electron mobility between the different layers can be neglected. In that case, it turns out that [27]:

$$F_d = \frac{(1+\Phi)\exp(\beta) + (1-\Phi)\exp(-\beta)}{(1+\Phi)\exp(\beta) - (1-\Phi)\exp(-\beta)} \,. \tag{16}$$

In Eq. (16), we have that $\beta = D_n/L_n$ and $\Phi = \exp(q\phi/kT)$, with ϕ the Fermi potential difference between the highly doped substrate and the epitaxial layer. In the limit of high potential difference ($\Phi >> 1$), F_d reduces to [27]:

$$F_d \approx \tanh\left(\frac{D_n}{L_n}\right). \tag{17}$$

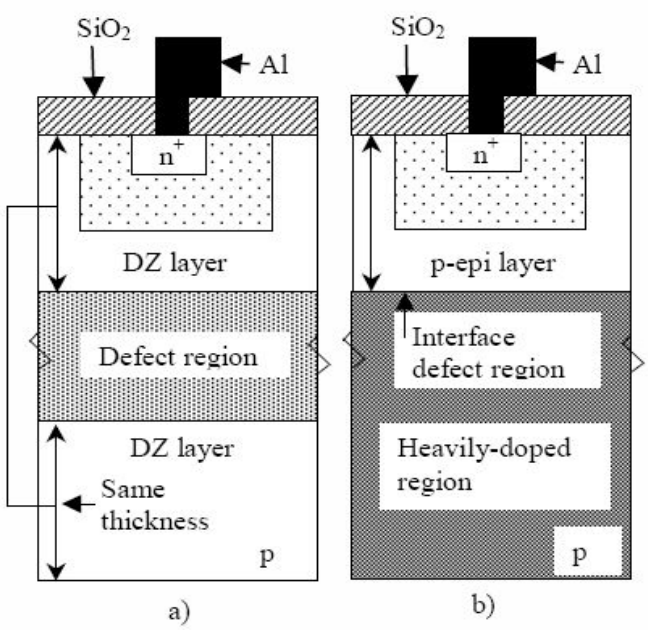


Fig. 8. Schematic representation of an n^+-p junction in a p-type IG Cz (a) or a p/p^+ epitaxial silicon (b) wafer.

This is a simple expression which can be calculated for an epi or IG wafer. As can be seen in Fig. 9, F_d is larger than 1 for an IG wafer due to the generation of minority carriers by the extended defects in the defective zone, while F_d is smaller than 1 for the epitaxial wafer, which is related to the efficient recombination of electrons in the highly doped p^+ substrate. This tells us that the electrical quality (effective diffusion length) of the epitaxial layer is superior compared to that of the DZ of an IG Cz wafer.

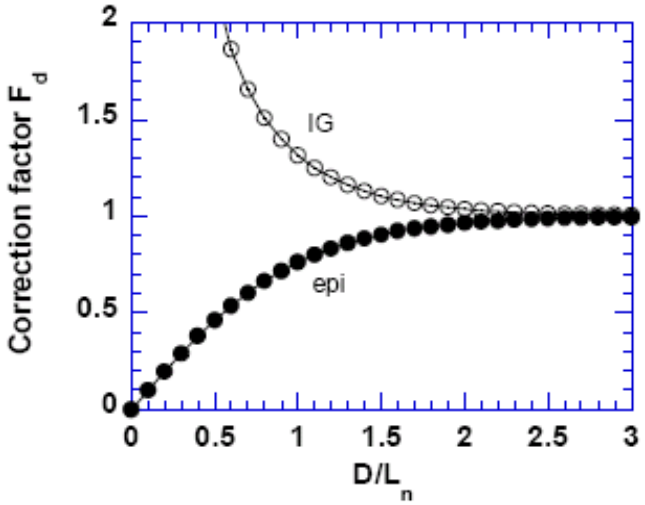


Fig. 9. Correction factor F_d, defined by Eq. (17) and calculated for an IG and epi wafer versus D_n/L_n ratio for the defect-free top layer.

It is generally not easy to determine the diffusion length (lifetime) of the good-quality top layer of an epi or IG wafer. In many cases the effective diffusion length is much larger than the layer thickness, so that with traditional front-surface excess carrier excitation and collection it is difficult to derive L_n. One has to rely either on Electron-Beam-Induced Current (EBIC) on bevelled samples or other cross-sectional lifetime techniques [28] in order to accomplish this goal. Here, it has been shown that based on the extraction of the diffusion current from the forward I-V of a p-n junction, one can fairly easily determine L_n of the epitaxial layer [29]. The principle is outlined in Fig. 10: rearranging Eq. (15), one arrives at:

$$\frac{J_{Adiff}}{F_d} = qD_n \frac{n_i^2}{N_A L_n}. \qquad (18)$$

In other words, plotting $J_{Adiff}/\tanh(D_n/L_n)$ and the linear function of D_n/L_n given by the right-hand side of Eq. (18) versus L_n should yield two curves which cross each other at the experimental L_n value. One only needs to know the doping density of the epitaxial layer, e.g., from a high-frequency C-V plot, and J_{Adiff} from the technique outlined above to arrive at a value for the diffusion length of the epitaxial layer. In the case of Fig. 10, one obtains an L_n~150 μm which is indeed much larger than the thickness of the epi layer.

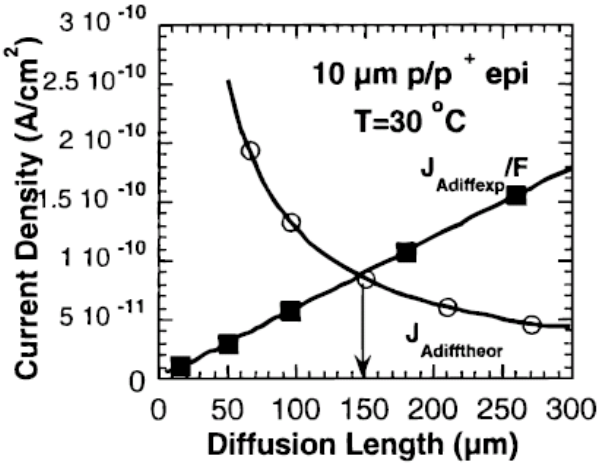


Fig. 10. Determination of the effective diffusion length in the epitaxial layer, using the diffusion current extracted from n^+-p junction diodes. Here, J_{Adiff}=6 pA/cm^2 at 30 °C and N_A=7·10^{14} cm^{-3} (after Claeys *et al.* [29]).

Processing-Induced Defects. Figure 9 already illustrates the poorer lifetime of Cz Si compared to epi material. This is related to the high density of oxide precipitates in the interior of the substrate. Cz silicon contains usually a high concentration of interstitial oxygen denoted by [O_i], coming from the quartz crucible that contains the silicon melt. This oxygen is present in supersaturation at conventional processing temperatures and will precipitate during thermal treatments. Typical [O_i] values for state-of-the-art large-diameter wafers are in the range 8×10^{17} cm^{-3}. IG is mostly obtained by performing first a high-temperature oxygen out-diffusion step thus removing the excess oxygen from a surface near layer by out-diffusion and, second, a low-temperature oxide-precipitate nucleation step. During further processing, usually beginning with a high-temperature field oxidation, oxide precipitates grow in the bulk of the wafer, while the near-surface layers remain relatively free from extended defects and form a DZ, in which the active device regions will be defined.

It is clear that the presence of these oxide precipitates and their associated extended defects can have an important impact on the electrical properties of the substrate and more in particular on the carrier lifetime. A systematic study, relying on p-n junction lifetime analysis has been performed in the past [18,19,30-34]. Figure 11 e.g. summarizes the effect of the initial interstitial oxygen concentration and the pre-treatment – either no (no); a nucleation step only (nucl) or an IG sequence (IG) [19] - on the generation and recombination lifetime of p-type Cz wafers, derived from the forward and reverse I-V, respectively. It is clear that the lifetimes are degraded for higher interstitial oxygen concentration [O_i], while a nucleation pre-treatment is also detrimental for achieving good lifetimes.

In order to further understand the lifetime behaviour, additional analysis techniques have been employed. It was for example shown that in a high [O_i] wafer, the generation lifetime profile is related to the concentration profile of an electron trap at 0.43 eV from the conduction band (Fig. 12), derived from DLTS on the same junctions [19,34]. There exists also a clear correlation with the density of extended defects observed by Transmission Electron Microscopy (TEM) [19] or by Laser Scattering Tomography (LST) [31,32,35]. This is illustrated in Fig. 13 [33]. In addition, it has been shown that there is a good agreement with recombination lifetime data derived by Light-Induced Absorption (LIA) or MicroWave infrared Absorption (MWA), as represented in Fig. 14 [32,33,36].

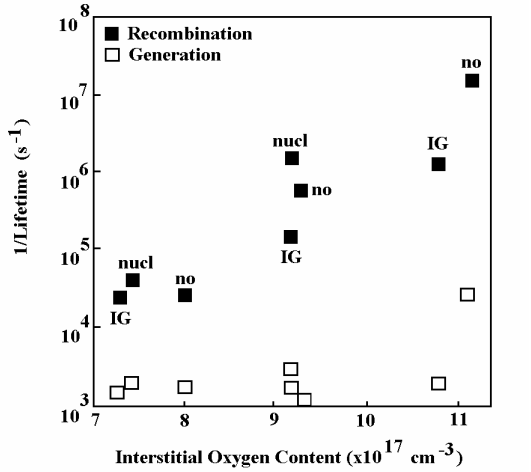


Fig. 11. Inverse τ_g and τ_r for p-type Cz wafers as a function of the initial interstitial oxygen content and thermal pretreatment.

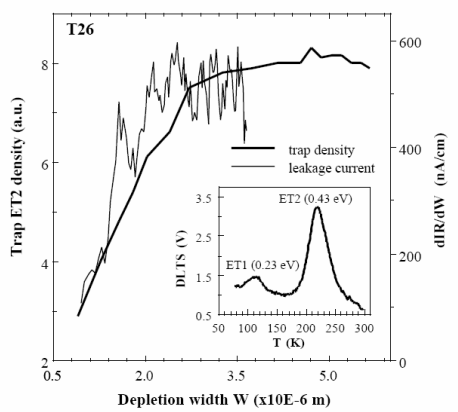


Fig. 12. Depth profile of the density of minority carrier trap ET2 and of the derivative of the leakage current (dI_R/dW) with respect to the depletion width for a high oxygen content wafer with 5×10^{10} cm^{-3} oxygen-related precipitate/dislocation complexes (PD's) in the substrate. The PD lean zone of about 3 μm near the wafer surface is clearly reflected in the depth profiles (after Vanhellemont *et al.* [19]).

The results of Fig. 13 suggest a direct correlation between the measured leakage current and the density of extended defects derived from LST. Assuming a linear relationship between both parameters, one can make a simple first-order estimate of the leakage current generated per light-scattering defect. For the high-oxygen (HO no) substrate, a leakage current density of 9.6 nA/cm^2 was derived [19]. This corresponds with an N_{LST} density of ~2×10^{10} cm^{-3} in Fig. 13. A leakage current of about 1 fA per defect, for a depletion depth of ~5 μm (Fig. 12) is thus obtained. This is a similar value as obtained for metal-related point defects in silicon [13] and in fact quite low for an extended defect, suggesting that they are not decorated by metals and thus clean processing.

The electrical activity of the oxide precipitates has also been measured directly by EBIC [37], using the same p-n junctions. It was demonstrated that at 300 K, the defects show low activity. They

became strongly active at 80 K, indicating that shallow levels (e.g., electron trap ET1 in Fig. 12) dominate the electrical activity below 300 K.

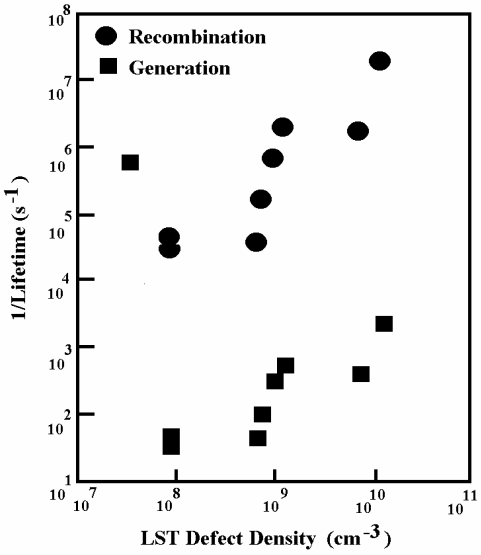


Fig. 13. Inverse τ_g and τ_r determined from I-V characteristics on p-type Cz Si substrates as a function of the density of LST defect density (after Claeys *et al.* [33]).

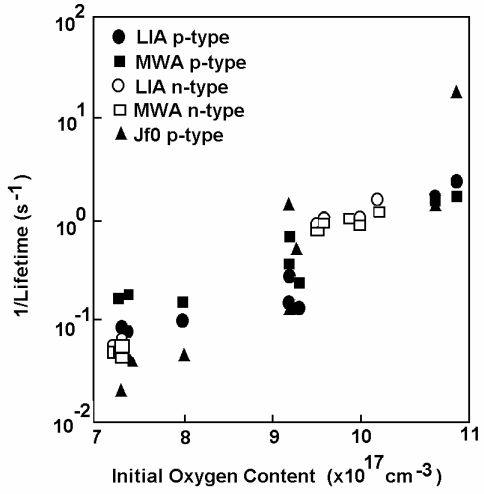


Fig. 14. Inverse of the recombination lifetime measured by electrical and optical/microwave techniques as a function of the initial oxygen content. An exponential relation between both parameters is observed (after Claeys *et al.* [33].

It was, finally, established that there exists also a correlation between the lifetime extracted from a p-n junction and the 1/f noise spectral density S_I, with $S_I \sim \tau^{0.18\pm0.05}$ [38].

Proton-Irradiation-Induced Defects in FZ Si p-n Junctions. When operating semiconductor devices in a radiation-harsh environment, degradation of the diode characteristics occurs due to the creation and build-up of radiation damage [39]. One particular damage type is the so-called displacement or lattice damage whereby upon collision with an energetic particle an atom is knocked off its lattice site, giving rise to a vacancy (V) and an interstitial (I) – a so-called Frenkel pair. Most of the generated pairs recombine quickly after their formation but due to their high mobility, some vacancies and interstitials escape and become trapped by impurities and dopants present in the material. For not too high a particle fluence, one generally observes that the device degradation increases proportionally to the proton fluence and can be described in terms of a

damage coefficient. This has for example been found for the leakage current of Si p-n junctions, exposed to 10 MeV protons (H^+) [40]. A linear increase was found up to a fluence of 7.9×10^{10} H^+/cm^2.

In the case of n-type Float-Zone (FZ) silicon, the dominant radiation defects are the Phosphorus-Vacancy (P-V or E center) and the di-vacancy (V_2) [39]. The latter has a donor level in the lower and two acceptor states in the upper half of the band gap, at E_V+0.19 eV and E_V-0.42 eV and E_C-0.23 eV, respectively [40]. These levels can be detected by DLTS. From the increase of the trap concentration with proton fluence, an average introduction rate of ~4 cm^{-1} has been derived in p- and n-type FZ silicon [40]. Moreover, upon extraction of the recombination (forward I-V) and generation lifetime (reverse I-V), one can derive the position of the effective generation centers with respect to the intrinsic level position, using Eq. (7). This yields the result of Fig. 15 [40], showing that $|E_T-E_i|\approx0.115$ eV (p-type Si) or ≈0.125 eV (n-type Si), respectively. From this, one can identify V_2 as the dominant leakage current generation center in proton irradiated p- and n-type FZ silicon.

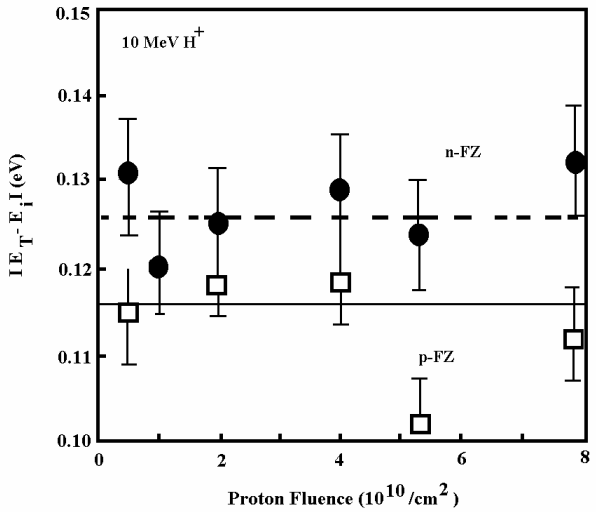


Fig. 15. Energy position of the generation centers, derived from the generation/recombination lifetime ratio for n- and p-type FZ Si, as a function of 10 MeV proton fluence. The accuracy is estimated to be ±5 % (after Simoen *et al.* [40]).

Lifetime and defect analysis in high-mobility substrates.

Scaling of CMOS technology is currently facing tremendous challenges related to the implementation of novel materials and device architectures. One of the problem areas, related to the so-called high-κ dielectrics is the degradation of the low-field mobility in a silicon inversion layer. This can be overcome by combining a high-κ gate with a so-called high-mobility substrate, ranging from strained silicon (sSi), over SiGe to germanium [41,42]. In this section, we will discuss the application of diode analysis to p-n junctions fabricated in several of these promising materials.

Thin Strain Relaxed Buffer Layers. Electron mobility is enhanced by inducing tensile strain. This can be achieved by an expansion of the lattice, like in strained silicon (sSi) deposited on a so-called Strain-Relaxed Buffer (SRB). This SRB is a SiGe layer which serves to change the lattice parameter from the Si substrate to the larger one of SiGe. The standard way to obtain a relaxed SiGe layer is by employing an epitaxially deposited step-graded buffer layer, changing the Ge content from 0 % up to typically 20 % with a gradient of 5 %/μm. Relaxation occurs through the introduction of misfit and threading dislocations (TDs), whereby the density of the latter should be controlled to an acceptable amount in the range of a few 10^6 cm^{-2}. The drawback of such an approach is the rather thick SiGe layer, giving rise to significant self-heating of the devices. From a

viewpoint of scaling, there is a strong interest in so-called thin SRBs, wherefore different methods are being proposed [43-48]. One possible strategy is to employ a thin SiGe layer doped with C, serving as a nucleation layer for the relaxation-induced dislocations [49]. The layer scheme is represented in Fig. 16. In this way, SRBs of only a few hundreds of nm can be fabricated not only uniformly but also selectively, with a TD density in the range of a few 10^6 up to 10^7 cm^{-2}, which is acceptable from a circuit operation point of view [50].

One of the concerns related to the use of sSi is the electrical activity of the TDs. This can be investigated directly by fabricating p-n junctions, as represented schematically in Fig. 16. It is immediately clear from the I-V curves of Fig. 17 that both the forward and reverse current increase with increasing TD density. The thick SRB junction has been fabricated in a commercial step-graded buffer layer, while the thin SRB corresponds to the C-doping approach [50,51]. For the n^+-p junctions a linear increases of the leakage current density with TD density is observed in Fig. 18, while a sub-linear increase has been found for the p^+-n junctions [51]. Based on these studies it can be derived that a single TD contributes on the average 10 pA at 1 V bias and 300 K [50]. Moreover, a good agreement with MWA lifetime measurements has been established [52,53].

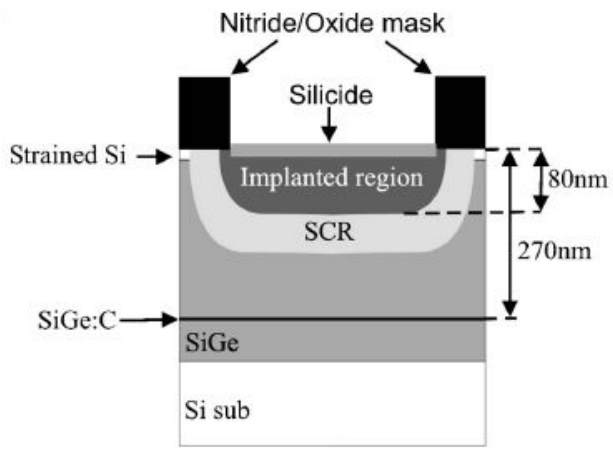


Fig. 16. The structure of the epitaxial layers, showing the position of the C-doped layer and the position of the junction. An oxide/nitride mask was used to pattern the junctions. After junction formation, a three-step nickel silicidation (10 nm Ni) was used to decrease the contact resistance.

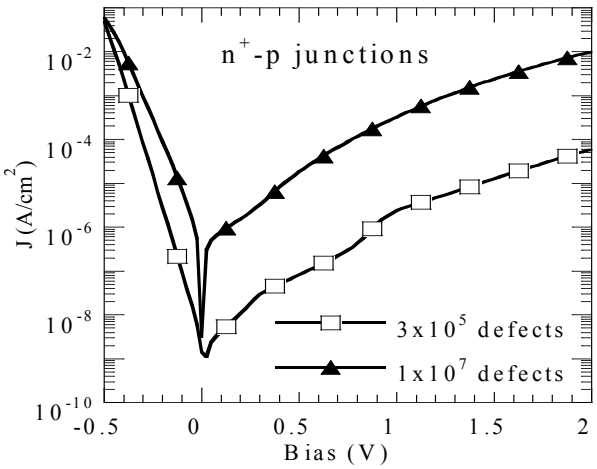


Fig. 17. Current characteristics for a thick (3×10^5 cm^{-2}) (□) and a thin SRB (1×10^7 cm^{-2}) (▲) n^+-p junction at 300 K.

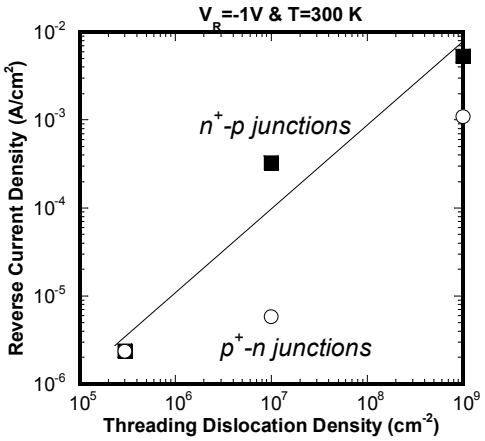


Fig. 18. Reverse current density in function of the TD density for n^+-p (■) and p^+-n (o) junctions. T=300 K, V_R=-1 V and the depth of the carbon-doped layer is larger than 270 nm.

However, it has been demonstrated that the TDs are not the only parameter determining the I-V in SRB junctions [51,53-55]. An important role is also played by the presence of the C-doped layer and its associated defects: it is known that a C doped SiGe layer relaxes by the formation of β-SiC precipitates [56,57]. When these defects are present in the depletion layer, they gives rise to a higher leakage current. In other words, I_R will increase with smaller distance between the junction and the C-layer (d_C). This is shown in Fig. 19 for n^+-p junctions with a constant TD density (TDD~10^7 cm^{-2}), yielding a close to exponential dependence of I_R on d_C for different reverse biases.

It has, finally, been demonstrated that also the temperature of the dopant activation anneal has a marked impact [55]. This points to the importance of residual well-implantation defects on the leakage current. Overall, the reverse current of SRB junctions with a C-doped layer consists of different contributions, which interact with each other. Optimization of I_R requires a low TD density, a high Rapid Thermal Anneal temperature (1100°C) and a C-layer outside the depletion region for realistic operation biases (<2 V). At the same time, it has been noted that the overall contribution of a single TD on the off-state current at 100°C is in the range of 1 nA, well below the specifications of the ITRS roadmap [50].

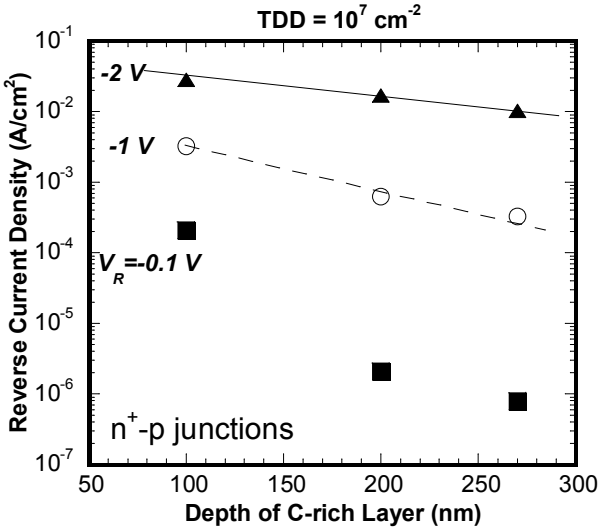


Fig. 19. Reverse current density at different V_R in function of the depth of the C-doped layer for n^+-p junctions. T=300 K and TD density is 10^7 cm^{-2}.

Recessed SiGe Source/Drain Junctions. The use of a sSi substrate comes down to a global strain engineering approach. One can also locally implement strain in the inversion channel of a MOSFET by the use of strained cap layers (SiN, silicides), by relying on the strain introduced by Shallow Trench Isolation (STI) or by the introduction of recessed SiGe source/drain regions [58-

62]. In the latter approach, the silicon source-drain regions are dry-etched and replaced by epitaxial SiGe layers, having a larger lattice parameters. A Transmission Electron Microscopy (TEM) cross section image of a p-channel MOSFET with recessed S/D is given in Fig. 20. The SiGe S/Ds will execute a compressive stress on the adjacent silicon channel, thereby enhancing the mobility of holes (pMOSFETs).

The resulting strain will depend on the Ge percentage and on the recess depth of the epitaxial layer. A higher mobility enhancement is expected for higher x and higher etch depth. At the same time, however, one should be concerned with the resulting leakage current, which is a sensitive monitor for the defects induced by the recessed S/D junction processing. As shown by Fig. 21, the reverse volume current density J_A increases one decade for every 5 % increase in Ge content [63]. This can be understood by the TEM-micrograph of Fig. 22, showing a high density of dislocations penetrating the underlying depletion region for the x=30 % case, while no defects where observed for the 10 % junctions [63].

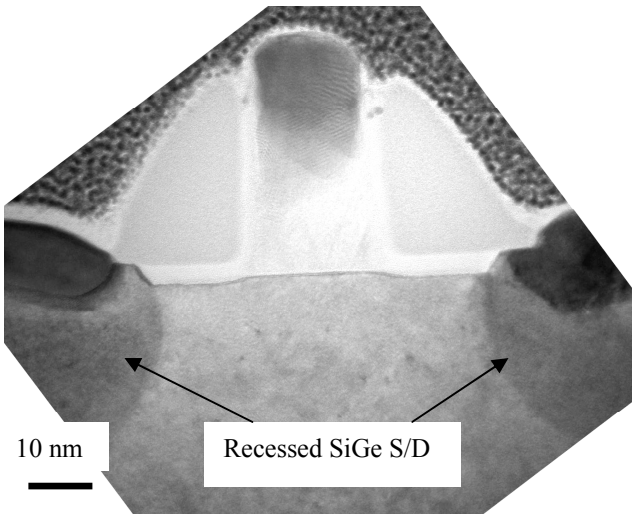


Fig. 20. TEM cross section view of a p-MOSFET with recessed SiGe source-drain regions.

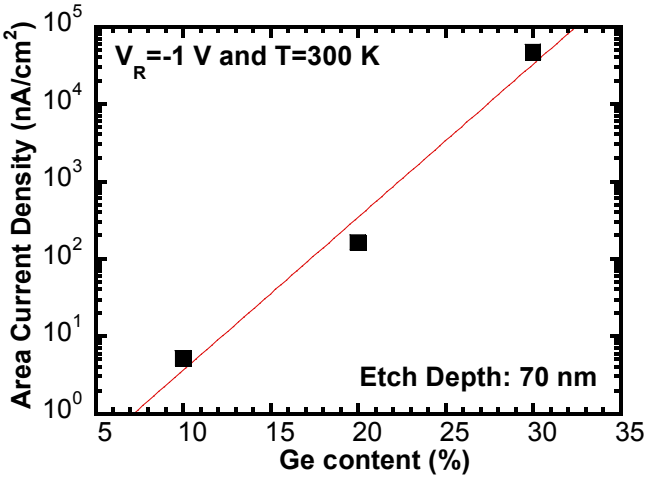


Fig. 21. Area leakage current density at -1 V and 300 K of recessed SiGe p^+-n junctions as a function of the Ge content.

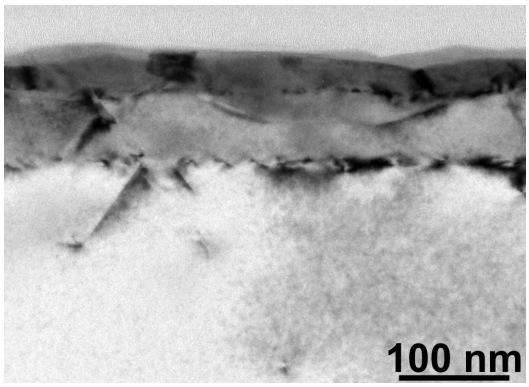
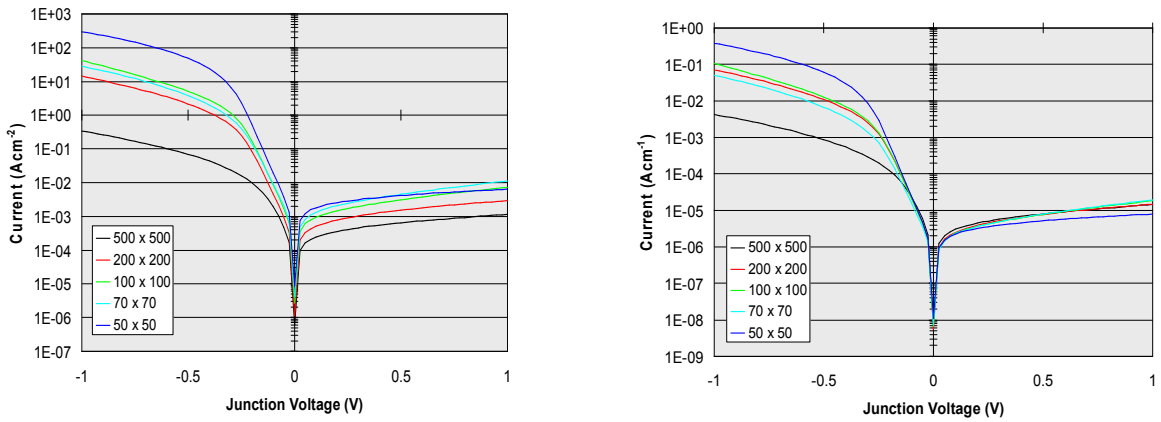


Fig. 22. TEM cross section view of a 30% Ge recessed S/D junction, showing a high density of dislocations penetration from the epitaxial interface into the underlying silicon substrate.

Besides the Ge percentage, also the recess depth [64] and the doping of the S/D regions by implantation play an important role in the leakage current of the junctions.

Germanium p-n Junctions. Perhaps one of the more promising routes towards high-mobility substrates is germanium, offering a two times improvement in electron and four times in hole mobility. A challenging field is the fabrication of shallow junctions with sufficiently low sheet resistance and leakage current [65-69]. It has been shown that as long as a non-optimized annealing is performed, the leakage current will be governed by ion-implantation-induced damage [66]. This originates from vacancy-related deep levels, as revealed by DLTS [65]. At the same time, there is more and more experimental evidence that after annealing above 400°C, only interstitial-related clusters remain present in the material, with similar peak positions in DLTS [70]. However, Rapid Thermal Annealing at 500°C or higher normally suffices for the junction leakage to become dominated by perimeter effects, as illustrated in Fig. 23 for n^+-p junctions on 5×10^{16} cm^{-3} doped p-type Cz Ge substrates. As can be seen, area-normalisation does not yield a constant leakage current density, while there is a reasonable overlap for the current divided by the junction perimeter in Fig. 23b. It clearly points to the fact that the passivation of surface states by a good quality dielectric is key for the improvement of the junction leakage in Ge based CMOS [66].



(a) **(b)**

Fig. 23. I-V characteristics of Ge n^+-p junctions normalized by area (a) and by perimeter (b). The dimensions are in μm. Surface passivation was by oxygen-lean Si_3N_4.

Conclusions and outlook

The examples given above have clearly illustrated the possibilities and versatility of the junction technique for substrate and defect analysis in semiconductors. Ultimately, it enables to extract both the generation and recombination lifetime from a single measurement, while some idea about the relevant defect parameters can also be obtained. A further identification should then be obtained in combination with more spectroscopic techniques like DLTS, lifetime measurements as a function of temperature, etc… However, one often finds that diode I-V is more sensitive than most of the other techniques, leaving much room for speculation on the defect origin. In that case, dedicated junctions have to be prepared in order to find the origin of the defect-related problem.

While the history of defect studies based on p-n junction analysis is already more than half a century old, there is still room for improvement and new developments. As has been touched upon already above, heterostructures become more and more an integral part of CMOS devices, e.g., the recessed SiGe on silicon source/drain diodes. One should also investigate germanium on silicon or III-V-on-Ge epitaxial layers, which will most likely be implemented in future scaled devices. In many cases, a p-n junction will exist at the epitaxial interface, which opens up the possibility for characterization, using the methods outlined above, However, there will also be specific problems associated with the band offsets and possible interface states [71,72]. This means that the physics becomes more involved and the interpretation of the electrical parameters less transparent. Probably, one has to rely on a combination of a semi-empirical, analytical approach and numerical device simulation for exploiting the junction tool to its full capabilities.

A final trend which is ongoing already since the start of CMOS scaling is the fact that practical junctions become shallower and shallower, reaching depths well below 100 nm. In that case, one can no longer neglect the contribution of the highly doped region to the forward and reverse current. Again, a dedicated approach is required to analyse the characteristics in terms of the relevant generation and recombination lifetimes.

Acknowledgements

Over the years, we had the chance to work together with many colleagues, who contributed to the results discussed above either by assisting with the measurements or by stimulating discussions and a continuous interest. In particular, we wish to thank: A. Poyai, A. Czerwinski, G. Eneman, P. Verheyen, R. Loo, R. Delhougne, E. Gaubas, A. Kaniava, M. Bargallo, P. Clauws, M. Libézny, G. Kissinger, W. Seifert, M. Kittler, A. Satta, B. De Jaeger, S. Sonde, G. Nicholas, H. Bender and A. Benedetti.

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