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Research paper

SPICE model for the current-voltage characteristic of resistive switching devices including the snapback effect

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ABSTRACT

Under certain conditions, the current-voltage (*I-V*) characteristic of transition metal oxide (TMO)-based resistive switching (RS) devices exhibits the so-called snapback effect. This effect is not always observable and is a feature associated with the abrupt reduction of the voltage drop across the device caused by the formation of a filamentary pathway spanning the insulating layer. Since the device electrical behavior must always comply with the load line constraint, the current increases following a trajectory dictated by the circuit series resistance. When the voltage drop across the device reaches the minimum value required to induce the ion movement, the filament starts to expand laterally with the consequent current increase. Remarkably, this phase develops at a fixed voltage drop between the device terminals. In this work, a simplified SPICE model for the intrinsic *I-V* curve of RS devices based on the memdiode concept (diode + memory) which includes the snapback effect is proposed. A thorough analysis of the role played by the model parameters related to that aspect is presented. Simulations are compared with experimental data obtained from Ta_2O_5-based RS devices.

1. Introduction

On some occasions, the *I-V* curve of memristive structures exhibits the so-called snapback (SB) phenomenon [1]. This corresponds to the combined effect of a reduction of the voltage drop across a metal-insulator-metal (MIM) device caused by the formation of a filamentary pathway spanning the insulating layer and the presence of a series resistance in the considered circuit. SB was first observed in SiO_2-based metal-insulator-semiconductor (MIS) structures subjected to current ramps [2]. In those experiments, abrupt reductions of the voltage drop across the MIS structure were observed as the current was progressively increased. The SB phenomenon was explained in terms of the formation of multiple percolation paths across the SiO_2 layer. Similar effects were observed in HfO_2-based devices [3]. In this case, the filaments were reported to exhibit quantum properties. In the context of MIM resistive switching (RS) devices, the SB effect has also been the focus of attention of numerous papers, both from the experimental [4] and theoretical [5] viewpoints. SB takes place when the device is initially in the high resistance state (HRS), which corresponds to a filament formed by oxygen vacancies with a gap. This filament is completed by the thermal- and field-induced movement of these vacancies caused by the application of an external potential. The SB effect occurs in the SET region ($V > 0$) and is triggered at a current level called I_{SET} (see Fig. 1). The negative slope of the *I-V* curve is dictated by the load line associated with the series resistance *R* (internal or external). A remarkable feature shows up when the experimental *I-V* curve is plotted using the series resistance correction *V-I·R* as the new voltage axis. This alternative plot represents the intrinsic *I-V* characteristic (blue line in Fig. 1). Under such transformation, for an appropriate *R* value, the current increases following a vertical trajectory until the degradation stops and the low resistance state (LRS) of the device is reached. This vertical line is located at a voltage value often referred to as the transition voltage (V_T), which is a characteristic parameter of the oxide material and measurement conditions [1]. V_T corresponds to the minimum voltage required to induce the displacement of the oxygen vacancies. The steep current increment corresponds to the lateral expansion of the filament. In the RESET region ($V < 0$), the filament starts its dissolution process at $-V_T$ (intrinsic *I-V*) and the device returns to HRS following again the load line (see Fig. 1). Another *I-V* curve which deserves a brief comment is that corresponding to an abrupt set condition which can arise as a consequence of adding a new series resistance to the experimental data (red line in Fig. 1). This behavior is typical of many memristive structures and reveals the roles played by the circuit series resistance and the location of the voltage probe with which the electrical characterization is performed. Contrary to what was observed in SiO_2 [2], in many TMOs, the above described cycle is observable and completely repeatable [6,7].

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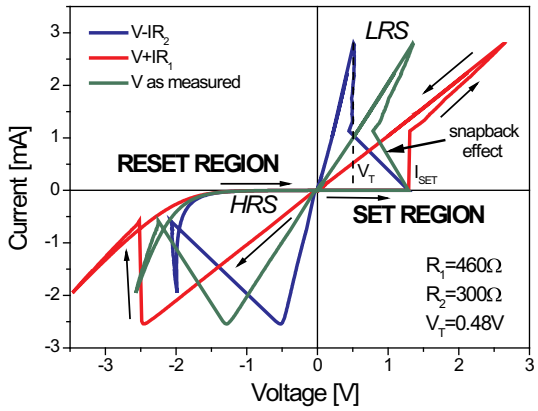

Fig. 1. Experimental *I-V* curves for a Ta_2O_5-based RS device, as measured (in green line) and after the transformation dictated by the series resistance (in blue and red lines). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

However, it must be pointed out that the SB effect is not always detected and its visibility seems to depend on the combined action of several factors: the particular features of the TMO (in particular the V_T value), the value of the series resistance, the magnitude of the HRS current previous to the occurrence of the SB effect, the trigger point I_{SET}, etc.

In this work, a recently proposed SPICE model for RS devices [8] is used to model the conduction characteristics of Ta_2O_5-based memristors. That published version did not include the SB phenomenon. The model is based on the memdiode concept, i.e. a diode system with hysteretic properties [9] and is used to identify the key parameters that control the SB effect. In this work, for the sake of simplicity, we will consider exclusively the time-independent version of the model. Therefore, the effects associated with the input signal frequency or with subthreshold current or voltage pulses are not included in this treatment. Here, we focus the attention on how the SB effect is introduced in the model formulation by means of a simple change. The device script for the LTSpice IV simulator is provided in the Sup. Mat. file. We show that the memdiode model allows us to accurately represent the *I-V* curves of Ta_2O_5-based memristors with SB effect. In Section 2, the devices investigated and the measurement setup are described. In Section 3, simulation and experimental results are compared. The model parameters related to the SB effect are varied so as to show their particular effect on the *I-V* curve. The conclusions of this work are presented in Section 4.

2. Devices and measurements

The experimental part of this study was carried out using Pt (30 nm)/Ta_2O_5(8 nm)/Ta(50 nm) structures [10]. The Ta_2O_5 switching layer was formed by annealing of the Ta bottom electrode for 30 min in oxygen at the partial pressure of 5 mbar at 400 °C. Ta_2O_5 films are amorphous with composition close to stoichiometry, as inferred from X-ray diffraction and XPS measurements (not shown here). The size of the RS structure is 5 × 5 μm. Measurement of the electrical characteristics was performed by application of quasi-static *I-V* sweeps using the Keithley 4200 Semiconductor Characterization System. The experimental voltage was taken at an intermediate point in the circuit so that the measured *I-V* characteristic also shows some partial SB effect. In order to obtain the intrinsic *I-V* curve, a 760 Ω series resistance with respect to the *I-V* curve with abrupt set transition needs to be used. This is the *R* value required to achieve a current increase at a fixed bias (V_T = 0.48 V). These values are independent of any model formulation. The *I-V* cycle-to-cycle stochastic variations are not considered in this work.

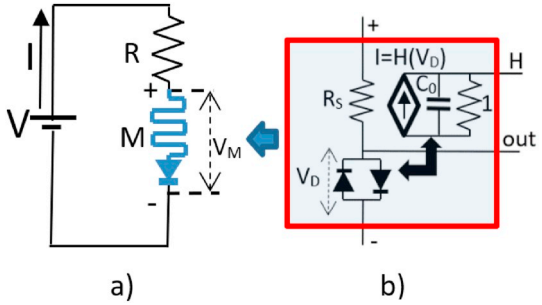

Fig. 2. Schematic for a) the measurement circuit and b) the internal implementation of the memdiode model. Notice that the series resistance can be placed outside or inside the memdiode structures. *H* and out are non-physical device terminals.

3. Experimental and simulation results

The memdiode model was originally presented in [9] and later extended in [8]. Since then it has been simplified and improved taking into account the versatility of a circuit simulator. Physically, the memdiode deals with a potential barrier that controls the flow of electrons through the device. Instead of the barrier height, the diode current amplitude factor I_0 is used as the reference variable. This factor changes because of the aggregation (SET) or elimination (RESET) of vacancies, defect sites, quantum filaments, etc., according with two well-defined and flexible transition functions. Since the memdiode is in fact a behavioral model, a precise identification of the microscopic physical aspects of the problem is not required. Following Chua's memristive approach [11], the memdiode model relies on two equations (see Fig. 2b), one for the electron transport expressed as two anti-parallel connected diodes with a single series resistance and a second equation for the memory state of the device λ which follows a hysteresis operator or hysteron. The first equation is simply expressed as:

$$I = sgn(V_D)\cdot I_0(\lambda)\cdot[exp(\alpha(\lambda)\cdot abs(V_D)) - 1] \quad (1)$$

where $V_D = V_M - IR_S(\lambda)$. V_M is the voltage drop across the memdiode, $I_0(\lambda) = I_{min}(1-\lambda) + I_{max}\lambda$, α a fitting constant, and R_S an internal series resistance. I_{min} and I_{max} are the minimum and maximum values of I_0, respectively. Both α and R_S can adopt a similar dependence on λ if required. *abs* is the absolute value and *sgn* the sign function. The diode inverse current in (1) is neglected. Because of R_S, as I_0 changes from I_{min} to I_{max} and vice versa in (1), the *I-V* curve changes its shape from exponential (HRS) to linear (LRS) as experimentally observed in many RS devices. It is also worth mentioning that for convenience, the series resistance can be placed inside or outside the memdiode model (see Fig. 2a). In this work, the series resistance is exclusively placed in the external circuit (the two cases are illustrated in the Sup. Mat. file). λ is a control parameter that runs between 0 and 1 and gives the memory state of the device. The hysteron reads:

$$\lambda(V_D(t)) = min\{\Gamma^-(V_D(t)), max[\lambda(V_D(t-dt)), \Gamma^+(V_D(t))]\} \quad (2)$$

min and max are the minimum and maximum functions, respectively. $\Gamma^+(V_D) = \{1 + exp[-\eta^+(V_D - V^+)]\}^{-1}$ and $\Gamma^-(V_D) = \{1 + exp[-\eta^-(V_D - V^-)]\}^{-1}$ are the positive and negative ridge functions, respectively. η^+ and η^- are the transition rates and V^+ and V^-, the SET and RESET voltages. $V_D(t-dt)$ is the voltage a timestep before $V_D(t)$. In the LTSpice environment, the hysteron is implemented using a voltage-controlled current generator and the λ value is stored in the capacitor C_0 (see Fig. 2b). $\Gamma^+(V_D)$ and $\Gamma^-(V_D)$ define the outer boundaries of the hysteron (green line in Fig. 3). Any point inside this mathematical structure is a possible state of the device. The initial value used in (2), λ_0, determines whether the device starts in LRS ($\lambda_0 = 1$), HRS ($\lambda_0 = 0$) or in any other intermediate state. Now, the SB effect is introduced in the model as an abrupt displacement of Γ^+ to a lower voltage value.

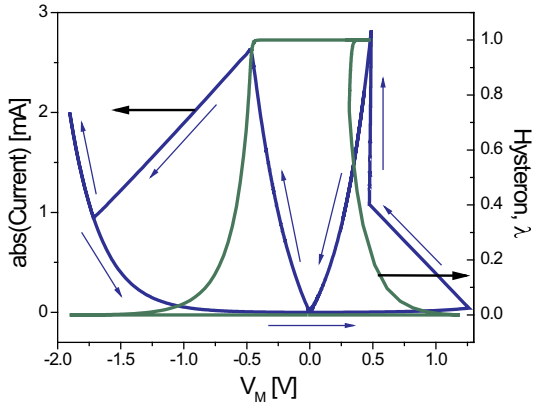

Fig. 3. Model results for the *I-V* and hysteron curves.

This reduces the state space of the device causing a current increase that must follow the circuit load line. In particular, the SET voltage change is modeled through the simple expression:

$$V^{+}(V_D) = V^{+}H(I_{SET} - I) + V_T H(I - I_{SET}) \quad (3)$$

where H is the Heaviside function and $V_T < V^{+}$. (3) expresses the formation of the conducting filament and provides the abrupt reduction of V^{+} toward V_T. (3) has no effect on the negative side of the *I-V* curve. The final results are current and memory loops as those illustrated in Fig. 3. In Fig. 4, experimental and model results for the intrinsic *I-V* curve are compared. Fig. 5 illustrates the current evolution and the voltage distribution along the circuit as a function of time. Some special points are indicated in the figure.

Finally, Fig. 6 illustrates what happens when the model parameters especifically associated with the SB effect are modified. For a complete revision about the rest of the model parameters see Refs [8,9]. Each parameter performs a well-defined action on the *I-V* curve: R affects the slope of the load line (Fig. 6a), I_{SET} the trigger point for the SB effect (Fig. 6b), and V_T the voltage at which the lateral expansion of the filament occurs (Fig. 6c). Our findings can be summarized as follows: the vertical current increase associated with the lateral expansion of the filament cannot be observed when: the series resistance R or R_S is small, I_{SET} is high and the SB effect takes place at a high voltage, and when V_T is low. Notice that similar conditions can be met in different ways. The fact that many compact models for RS devices do not include the SB effect along with the vertical current increase does not mean that they are incorrect. This only means that they are valid under special circumstances.

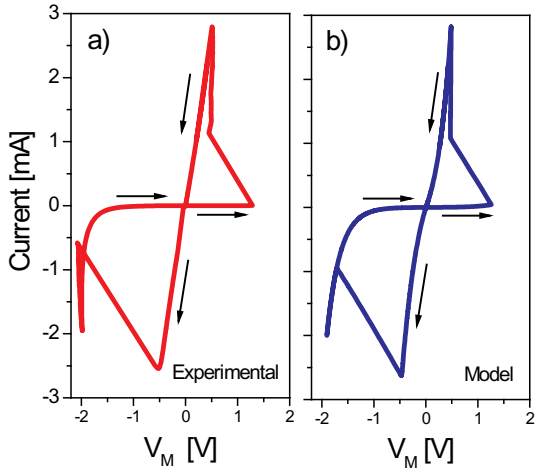

Fig. 4. Comparison between experimental and model results.

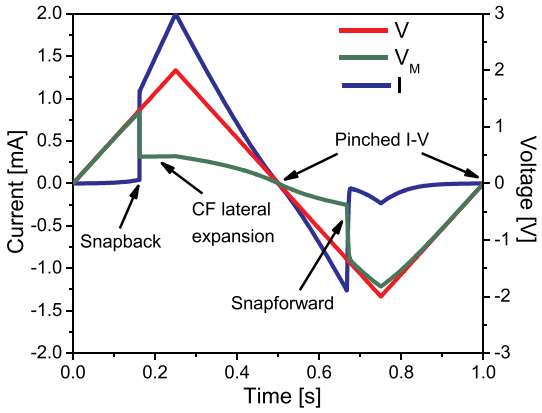

Fig. 5. Model results for the evolution of the current and voltage distribution as a function of time for a 2V signal amplitude.

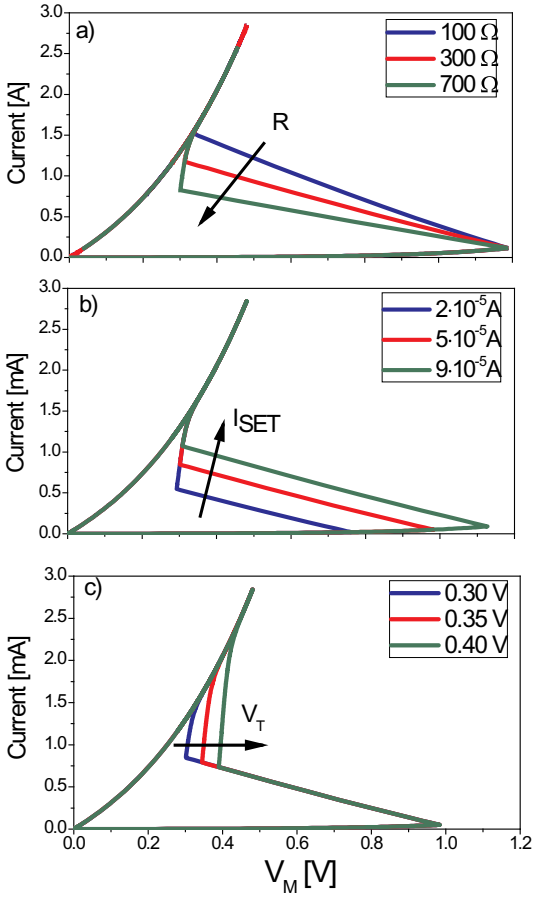

Fig. 6. Effects of the model parameters on the simulated *I-V* curves: a) Series resistance R, b) trigger point I_{SET}, and c) transition voltage V_T.

4. Conclusions

A simplified SPICE model for resistive switching devices including the snapback effect was proposed. Simulations were compared with experimental data obtained from Ta_2O_5-based devices. The model, which is based on a diode-like conducting structure with hysteretic properties, allows to identify the fundamental parameters that drive the current increase during the SET process. The relevance of the series resistance effect in the understanding of the *I-V* curves of these devices has been highlighted.

Conflict of interests

There are no conflict of interests.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mee.2019.110998.

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