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Determination of current transport characteristics in Au-Cu/CuO/n-Si Schottky diodes

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ABSTRACT

In this study, the material properties of CuO thin films fabricated by sputtering technique and electrical properties of CuO/n-Si structure were reported. Temperature-dependent current-voltage (I-V) measurement was carried out to determine the detail electrical characteristics of this structure. The anomaly in thermionic emission (TE) model related to barrier height inhomogeneity at the interface was obtained from the forward bias I-V analysis. The current transport mechanism at the junction was determined under the assumption of TE with Gaussian distribution of barrier height. In this analysis, standard deviation and mean zero bias barrier height were evaluated as 0.176 and 1.48 eV, respectively. Depending on the change in the diode parameters with temperature, Richardson constant was recalculated as 110.20 $Acm^{-2}K^{-2}$ with the help of modified Richardson plot. In addition, density of states at the interface were determined by using the forward bias I-V results.

1. Introduction

In recent years, transition metal oxides have great importance in many electronic device applications due to their unique material properties as an interfacial layer at metal-semiconductor (MS) diodes [1,2]. These properties are subject of interest for various applications as transistors, photovoltaics and gas sensors [2–5]. Among these metal oxides, copper oxide (CuO) which is the member of the family of II–VI oxide semiconductor with p-type semiconductor characteristics is getting wide attention as a promising candidate in various microelectronic and optoelectronic applications. In this case, the advantages of abundance and non-toxicity attract a broad spectrum of applications due to cost-effectiveness in the mass production and large-scale applications [6–8]. In addition, it shows highly effective optical characteristics in visible light with a direct band gap in the interval of 1.3 eV–2.1 eV and therefore it is widely used in the photovoltaics and photodetectors [7–10]. In addition, it is a class of material in gas sensors in the case of chemical sensitivity and high absorption of reactive gases [11,12].

CuO/Si diode is of considerable interest in the integration of optoelectronic devices based on the suitable material properties, cost-effective fabrication and constituent materials, and non-toxicity of CuO thin film and the cheapness of n-Si wafer substrate with well-known material parameters [9]. In literature, variety of deposition techniques including thermal evaporation [13], sputtering [6–8,11], chemical vapor deposition [14], chemical bath [15], spin coating [16], spray pyrolysis [17], sol-gel [9], electro deposition [18] and successive ionic layer adsorption and reaction method [12,19] have been reported for the synthesis of CuO thin films. Although CuO-based devices have been studied in the analysis of dark I-V characteristics [8,12,20], photocurrent response [5,21,22] and sensitivity to gas molecules [11,12], detailed understanding on the device characteristics including investigation of main diode parameters and dominant carrier transport mechanisms have still not been achieved.

There has been considerable interest in the experimental studies of MS type Schottky diodes and electrical characteristics of these diode structures can be modified by interlayer between metal and semiconductor [23,24]. In this case, the performance of these devices is mainly influenced by the formation and characteristics of the interface states, and also series resistance (R_s) and interface layer thickness [23–27]. According to the literature, various models have been proposed to describe the effects of interface state and carrier transport across this layer. Among these, TE theory is found to be the most

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appropriate model to investigate the parameters for these diodes. On the other hand, depending on the possible barrier in homogeneities at the interface and (R_s) effect, I-V characteristics usually deviate from the ideal TE model, and determination of the current transport mechanism becomes more complicated [27].

In the present study, CuO films were coated onto glass and n-type silicon substrates by RF magnetron sputtering technique with the advantageous on control of both deposition rate and atomic composition in the deposition of thin films at low substrate temperatures [6]. Material characteristics of the deposited CuO film layer were investigated via X-ray diffraction (XRD), scanning electron microscope (SEM) imaging and energy dispersive X-ray spectroscopy (EDS) analysis. Hall Effect measurement was also performed at room temperature to determine the electrical properties of the films by using Nanomagnetic Hall Effect system at a magnetic field strength of 0.9 T. In literature, although there are several works on the fabrication and characterization of CuO/Si type of diode structure, the formation of Schottky barrier and interface properties have not been extensively reported. Since, temperature-dependent electrical measurements are mostly required to give detailed information on the conduction process at the interface, I-V measurements were performed in the wide temperature range in between 220 and 360 K to investigate the formation of barrier height and conduction mechanisms in this structure.

2. Experimental details

CuO thin films were deposited on soda-lime glass (SLG) and one-side polished n-type silicon wafer with a resistivity values of 1–10 Ω-cm using single CuO target (99.9% pure Kurt J. Lesker) by RF magnetron sputtering technique [28]. SLG substrates were ultrasonically cleaned using acetone, isopropyl alcohol and hydrogen peroxide solutions, and wafer substrates were chemically cleaned applying standard RCA procedures for removing contaminants [29]. Prior to the deposition steps, the native oxide layer was etched on the surface of the Si wafer using a diluted hydrogen fluoride solution. Al elemental evaporation and after this deposition step, 450 °C subsequent annealing under nitrogen atmosphere were performed to form ohmic back contact on the wafer substrate [5]. After loading the substrates to the single magnetron sputtering system, the base vacuum was lowered to about 10^{-5} Pa, and during the deposition, it was kept at 10^{-1} Pa under pure argon flow to the chamber. The substrates were maintained at room temperature and the deposition were performed with 100 W sputter power under 5 sccm argon flow after the pre-sputtering as a process to clean the target surface in a pure argon plasma. The deposition rate and thickness of the deposited film on the substrates were measured in-situ quartz crystal connected to Inficon XTM/2 deposition monitor. As a result of several optimization processes on the deposition parameters, CuO thin film layer was deposited on substrate surfaces with about 1.0 Å/s deposition rate and final thickness was measured by Dektak 6 M profilometer as about 250 nm. The crystallinity of the deposited films was investigated by Rigaku Miniflex X-ray diffraction (XRD) system equipped with Cu-Kα radiation source (λ = 1.54 Å). Top-view surface image was obtained by Zeiss EVO15 model scanning electron microscope (SEM) and the atomic percentage of the elements in the composition was determined by energy dispersive X-ray spectroscopy (EDS) detector attached to SEM. Optical measurements were carried out by PerkinElmer Lambda 45 UV/VIS/NIR spectrophotometer in the wavelength range of 300–1000 nm. Following to deposition of CuO/Si/Al layers, the fabricated diode structures were completed with elemental Cu-Au front metal contact deposition through front surface of the CuO film with dot-patterned (with the radius of 700 μm) Cu masks (see Fig. 1). In this diode, thermally evaporated Au layer was used as a front metal contact on the CuO film layer, however, at the interface, very thin Cu was evaporated on the CuO thin film surface to increase the sticking probability and durability of this contact. In the literature, there are many works about single layer metal contact [30–33]. On the other hand,

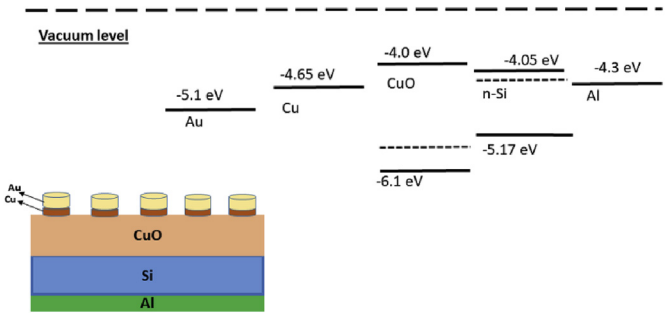

Fig. 1. The schematic diagram for Au-Cu/CuO/n-Si/Al Schottky diode.

metal contacts such as Cu-Au was found to be increase the hardness of the contact material [34,35].

After contact deposition step, the samples were annealed at 100 °C under the nitrogen atmosphere to enhance the top contact behavior. I-V measurements were carried out using a compact system controlled by Labview software and Keithley 2401 sourcemeter. For the temperature-dependent measurement, the samples were mounted on cold head of Closed Cycle Cryogenics helium cryostat and sample temperature was controlled by LakeShore 331 temperature controller. The measurement temperature was in the temperature range of 220–360 K increased by 20 K steps under dark condition.

3. Results and discussion

The elemental analysis and surface morphology of the CuO thin films were studied by EDS and SEM measurements, respectively. According to the EDS analysis given in Fig. 2(a), atomic percentage of Cu and O was found as 40–60% in the structure by ignoring the atomic percentage of Si. In addition, from the 10 × 10 μm^2 scan area of SEM given in Fig. 2 (b), a uniform surface was observed. The crystallinity nature of the sputtered film layer and crystalline phases in this structure were investigated from the XRD profile given in Fig. 2 (c). From this XRD pattern, the deposited thin film was found in polycrystalline behavior with two distinct peaks as shown. In a close agreement with the literature, this structure was found to be oriented along (111) direction as the main peak orientation and the second characteristic peak indicated (020) orientation direction [2,6–8,21].

In order to investigate optical properties of the deposited CuO thin films, optical transmission measurement was carried out at room temperature in the wavelength range of 300–1000 nm. As shown in Fig. 3, the transmission values were found in between 20 and 40% in the visible region with 80% maximum value in the whole spectrum. Additionally, the optical band gap of the films was estimated by a Tauc plot given in Fig. 3 as an inset [36] and the extrapolation of the linear part of this plot shows about 2.1 eV band gap energy for these samples [2,8,21]. The band gap of the film indicates that these films are transparent to the incident solar radiation when compared to the ideal band gap of the absorber layer and n-Si layer.

The deposited Au-Cu/CuO/Si/Al sandwich structure includes the oxide CuO semiconductor layer at MS interface. According to the results of room temperature Hall Effect measurement, it shows a p-type conductivity characteristic. The conductivity value was extracted from four-point probe Van der Pauw measurement as about 10^1 $(\Omega\,cm)^{-1}$ and the Hall mobility and carrier concentration of this layer, were calculated as about 4 cm^2/V.s and 10^{19} cm^{-3}, respectively. These experimental results are comparable to the literature [20].

The current transport properties and the diode parameters of CuO/n-Si structure were determined by studying the temperature-dependent I-V results using thermionic emission (TE) theory. The temperature dependence of the diode's I-V characteristics in the temperature range of 220–360 K is illustrated in Fig. 4.

The current through the junction barrier at the region of forward

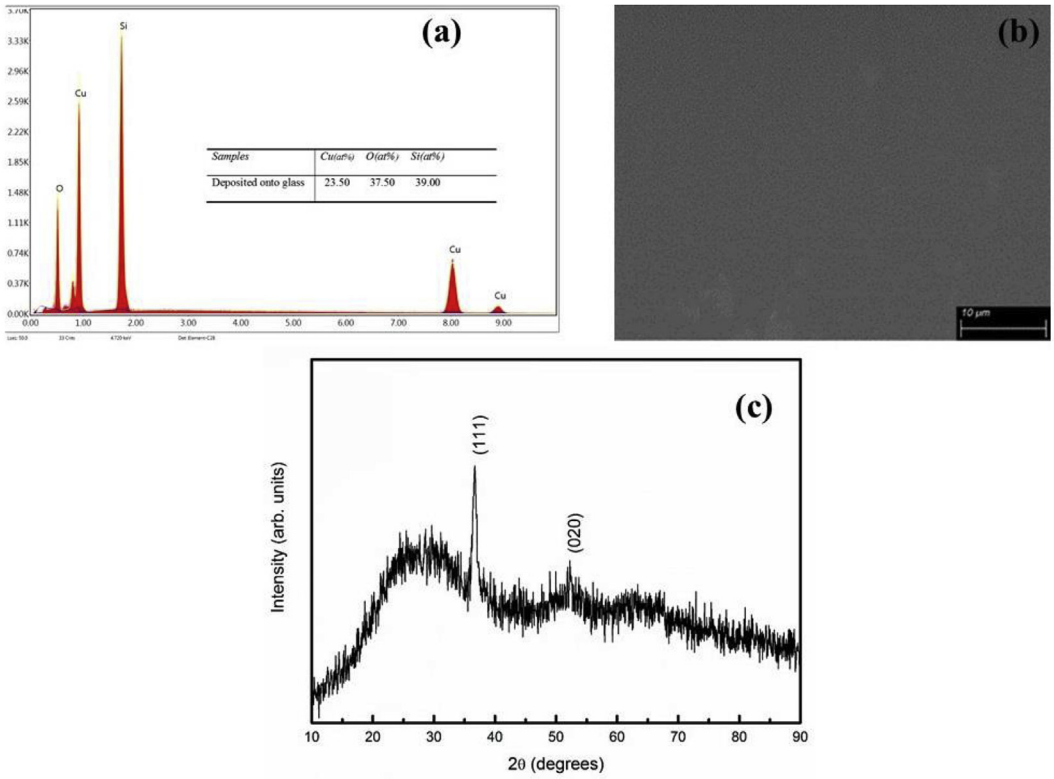

Fig. 2. EDS results (a), SEM image (b) of CuO thin films deposited onto Si substrates and XRD results of CuO thin films deposited onto glass substrate.

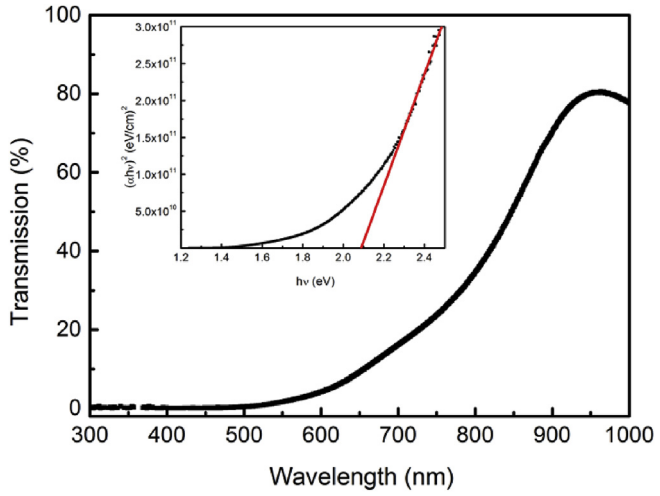

Fig. 3. Transmission spectrum and characteristics Tauc plot (inset) of CuO thin films deposited onto glass substrate.

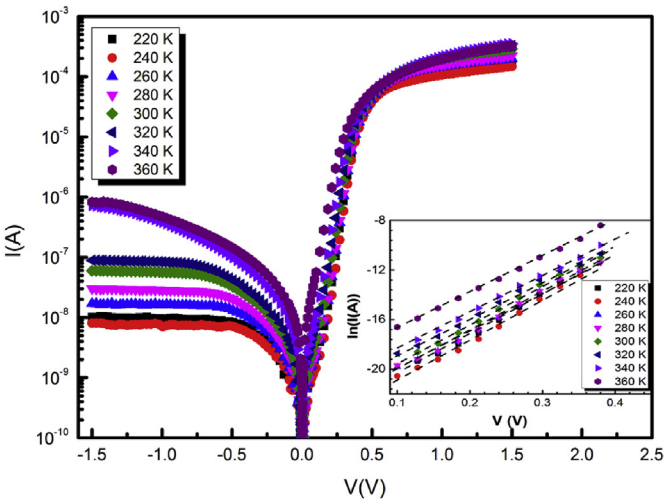

Fig. 4. Temperature dependent I-V plots of CuO/n-Si Schottky diode. Inset shows the selected linear region of ln(I)-V plots in the voltage range of 0.1 and 0.4 V.

bias could be stated with the deviation from ideality as [37,38];

$$I = I_0\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

where I_0 is the reverse saturation current, q is the electronic charge, V is the applied forward bias voltage, IR_s term is the voltage drop under the series resistance effect (R_s), n is the ideality factor, k is the Boltzmann constant and T is the ambient temperature. I_0 can be expressed as;

$$I_0 = AA^*T^2\exp\left(-\frac{q\varnothing_{b0}}{kT}\right) \quad (2)$$

Here, A and A* are the effective diode area and Richardson constant, respectively; and $\varnothing_{b0}$represents the zero bias barrier height. Using Eq. (2), A* was determined by using the nearly free electrons in vacuum with TE assumptions [39].

n is also an indicative parameter for the determination of the dominant current transport mechanism in the junction. From Eq. (1), the *n* values can be obtained from

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right) \quad (3)$$

n values for each temperature were deduced from the linear region of Fig. 3 using Eq. (3) and these values are listed in Table 1. The change in these values with the temperature is also given in Fig. 5. As seen from the figure, *n* values decreases with increasing temperature.

$\varnothing_{b0}$ could be obtained from the I_0 value as;

Table 1
The device parameters obtained from temperature dependent I-V characteristics.

T(K)	Ideality factor (n)	Saturation Current (I_o(A)×10^{-11})	Zero Bias Barrier Height ($\varnothing_{b0}$(eV))	Interface States (D_{it}) ($eV.cm^2$)$^{-1}$x10^{13}
220	1.56	4.02	0.67	6.85
240	1.47	7.30	0.72	5.76
260	1.38	9.13	0.78	4.65
280	1.33	8.73	0.84	3.70
300	1.29	35.33	0.87	3.61
320	1.26	94.80	0.91	3.52
340	1.22	175.00	0.95	2.69
360	1.17	334.75	0.99	2.10

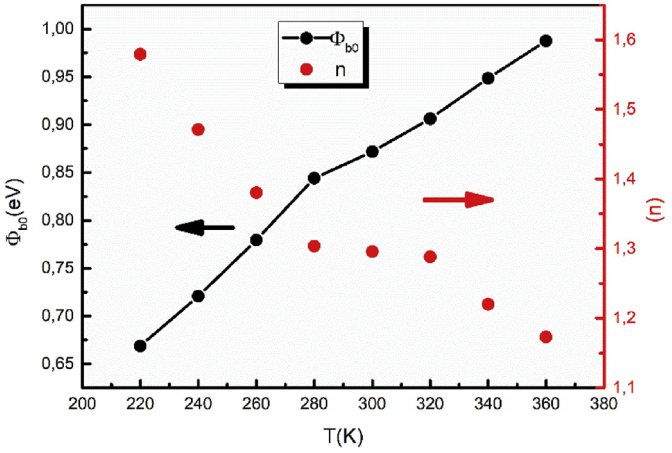

Fig. 5. Variation of $\varnothing_{b0}$and n with temperature for CuO/n-Si Schottky diode.

$$\varnothing_{bo} = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_o}\right) \quad (4)$$

The calculated $\varnothing_{b0}$ values for each temperature are tabulated in Table 1 and the variation of $\varnothing_{b0}$ with the temperature is shown in Fig. 5. It is indicated that $\varnothing_{b0}$ values increase with increasing temperature. The rise in $\varnothing_{b0}$ could be correlated with the free carriers having sufficient energy to exceed the barriers, so they can contribute to the conduction with increasing temperature [40].

As inferred from Fig. 4 and Table 1, $\varnothing_{b0}$ and n values are inversely proportional to each other with increasing temperature. This variation might be due to the formation of non-homogeneity in the barrier height. In addition, the higher than unity value of $n$can be the indication of laterally inhomogeneity in diode structures [37]. Therefore, the additional current transport mechanism to TE model could be required to analyze the current flow in the junction. It is found that there is a linear correlation in between the obtained $\varnothing_{b0}$ and n values as illustrated in Fig. 6. This inverse linear behavior can be ascribed to the lateral inhomogeneity in the barrier height according to the Tung's approach [28,41]. A laterally homogeneous value of barrier height (lateral barrier height) was determined as about 1.13 eV for the junction from the extrapolation of this linear correlation to n = 1.

The ascertained deviations from the analysis of I–V characteristics on the application of the TE model in the current flow characteristics of the fabricated structure could be modeled Gaussian distribution (GD) of the barrier height at the junction interface [42]. TE mechanism with GD of the barrier height is applied due consideration of barrier inhomogeneity with localized low barrier patches at the interface. Therefore, by utilizing standard statistical distribution, the current transport theories for homogeneous barrier height was widened with covering the effect of inhomogeneous barrier formation and the distribution of the inhomogeneity in the barrier height. The temperature

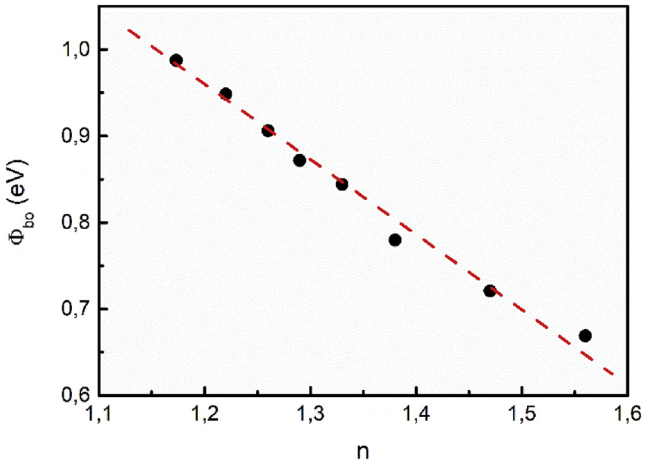

Fig. 6. Relation between $\varnothing_{b0}$ and n for CuO/n-Si Schottky diode.

dependence of $\varnothing_{b0}$distribution could be given in terms of GD as

$$\varnothing_{ap} = \bar{\varnothing}_{b0} - \frac{q\sigma_s^2}{2kT} \quad (5)$$

where $\varnothing_{ap}$ represents the apparent barrier height from the modification of barrier height expression [43], σ_s represents the standard deviation in T variation of barrier height and $\bar{\varnothing}_{b0}$represents the mean value [36]. At this point, σ_s is used in order to determine the deviation from the homogeneity of barrier height in the junction [36]. Using the plot of $\varnothing_{b0}$ vs q/2kT having a linear relation, $\bar{\varnothing}_{b0}$ and σ_s values were determined as 1.48 eV and 0.176 (about % 18), respectively. Hence, it is indicated the existence of an interfacial inhomogeneity with a GD of barrier height at the interface [28,42].

In addition, this modification could be applied to ideality factor n as the distribution functions in barrier height expression. Hence, the modified ideality factor n could be expressed as,

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \quad (6)$$

where, n_{ap} is an apparent ideality factor which describes the barrier distribution with having any voltage dependence [42]. The parameters labeled as ρ_2 and ρ_3 represents the bias dependence of $\bar{\varnothing}_{b0}$ and σ_s, respectively. These parameters point out the voltage deformation of the barrier height distribution. As a matter of fact, Eq. (6) implies the effect of temperature on n and it could be used as a measurement for the homogenization of the barrier distribution [39,42].

The parameters were calculated from the slope and intercept of the linear relation given in Fig. 8 as, ρ_2 = 0.0198 V and ρ_3 = 0.160, respectively.

Besides, Richardson constant for this sample could also be obtained experimentally using the results of the GD of barrier height with the relation as given below [39,44],

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\varnothing}_{b0}}{kT} \quad (7)$$

Fig. 9 shows a straight line which belongs to I-V relation with the modification under the assumption of GD. The slope of this straight line gives $\bar{\varnothing}_{b0}$ and extrapolation value is used to determine A^* for a given diode area A [45,46], As shown in both Figs. 7 and 9, $\bar{\varnothing}_{b0}$ value was found to be about 1.48 eV A^* was calculated as 110.20 A/cm^2K^2 and this value is in a good agreement with the expected value for the active semiconductor layer as 112 A/cm^2K^2 [24].

Another device parameter effects the device performance is the value of series resistance (R_s) that is the total resistance of bulk of the semiconductor, contact wires and ohmic contacts. There are several

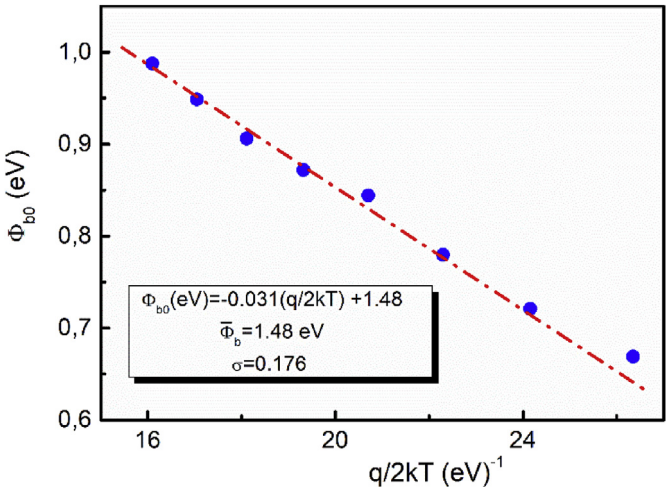

Fig. 7. Plot of $\varnothing_{b0}$ vs q/2kT for CuO/n-Si Schottky diode.

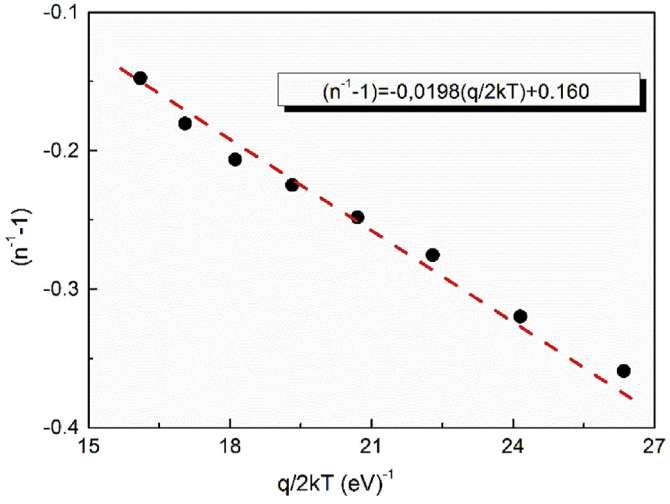

Fig. 8. Plot of $(n^{-1} - 1)$ vs q/2kT for CuO/n-Si Schottky diode.

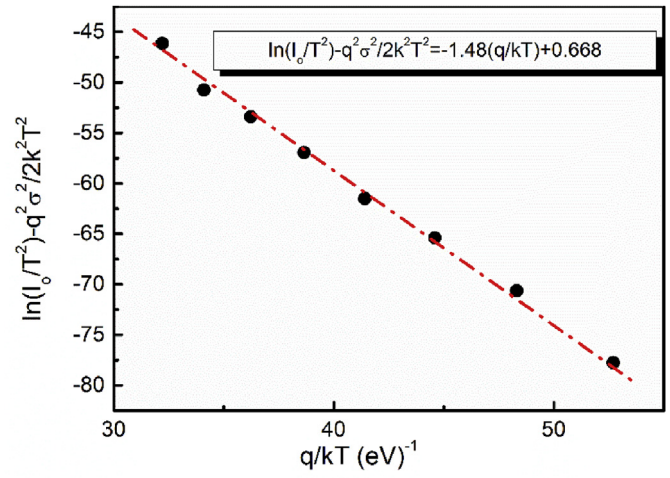

Fig. 9. Plot of $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ vs q/kT for CuO/n-Si Schottky diode.

methods to determine the R_s value of a diode such as Ohm's law ($R_s = dV_i/dI_i$), Cheung's functions and Norde method [47,48]. In this work, the modified Norde method was utilized to find out the values of both R_s and $\varnothing_{b0}$. Fig. 10(a) illustrates the voltage dependence F(V) versus V(V) plot for CuO/n-Si Schottky diode at different temperatures.

According to this alternative method, $\varnothing_{b0}$and R_s values could be determined by using the expression as given;

$$F(V) = \frac{V}{Y} - \frac{kT}{q}\left[\ln\left(\frac{I(V)}{AA^*T^2}\right)\right] \tag{8}$$

where Y is an integer and should be chosen greater than n [39]. In addition, $\varnothing_{b0}$ value is given as;

$$\varnothing_{b0} = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{9}$$

where $F(V_0)$ and V_0 are denoted as the minimum point of F(V) and the minimum voltage corresponds to $F(V_0)$, respectively.

$$R_s = \frac{kT(\gamma - n)}{qI_0} \tag{10}$$

Also, R_s value is given as;where $I_0$the minimum current is corresponding to $F(V_0)$.

Using Eqs. (9) and (10), $\varnothing_{b0}$ and R_s values were determined for each temperature and listed in.

Table 2. As can be seen from Table 2, there is a slight difference in the $\varnothing_{b0}$values obtained from TE analysis and Norde Method, which could be originated from Norde Method with by the assuming the barrier in the junction as an ideal diode (taking n = 1) [49].

In addition, Rs values have been calculated from both Cheung Method and parasitic resistance calculation "$R_i = dV_i/d(I_i)$" in order to compare the values obtained from Norde Method and listed in Table 2. Fig. 10 (b) illustrates the plots of the dV/dln(I) versus I and H(I) versus I for different temperatures in a wide range from 220 to 360 K. These plots were used to determine the R_s values from Cheung method. Fig. 11 illustrates the temperature dependence of R_s values using each different method. As seen from the figure, there is a slight difference in the values of series resistance calculated from Cheung and Norde methods. This difference could results from the calculation methods. For instance; while Cheung's functions can only be applied for the non-linear region of the forward bias I–V curve, Norde functions can be applied for the whole forward region of I–V curve of the diode [46]. Moreover, the values of R_s decrease with increasing temperature, which is related to the lack of free carrier concentration at low temperatures [37].

The distribution of localized interface state density (D_{it}) is another parameter to determine the performance of the devices. In order to investigate the values of D_{it} under the consideration of their values in equilibrium with semiconductor, the forward bias I-V results could be used [50]. When the n values greater than unity which is the non-ideal diode case, this behavior could be expressed as;

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{w_D} + qD_{it}\right) \tag{11}$$

where δ is the interfacial insulator layer thickness calculated from high frequency Capacitance –Voltage (C-V) characteristics as few nanometer [24]. $\varepsilon_i = 3.9$ and $\varepsilon_s = 11.8$ are the permittivity of interfacial insulator layer and semiconductor layer, respectively. W_D is the width of the space charge region which was calculated from C^{-2} vs V graph as 100 nm [24,42]. D_{it} values were obtained as a function of $E_c - E_{ss}$ values. The energy of the interface states E_{ss} with respect to the top of the conduction band at the surface of semiconductor can be expressed as

$$E_c - E_{ss} = q(\Phi_e - V) \tag{12}$$

where, Φ_e represents the effective barrier height ant it has voltage dependence with the possible interface states in the diode structure [39].

Fig. 12 illustrates that interface state densities show a falling tendency with increasing temperature. This temperature dependency could be explained as interface layer's restructuring and the reordering with the effect of temperature [25]. Moreover, there is a clear shifting

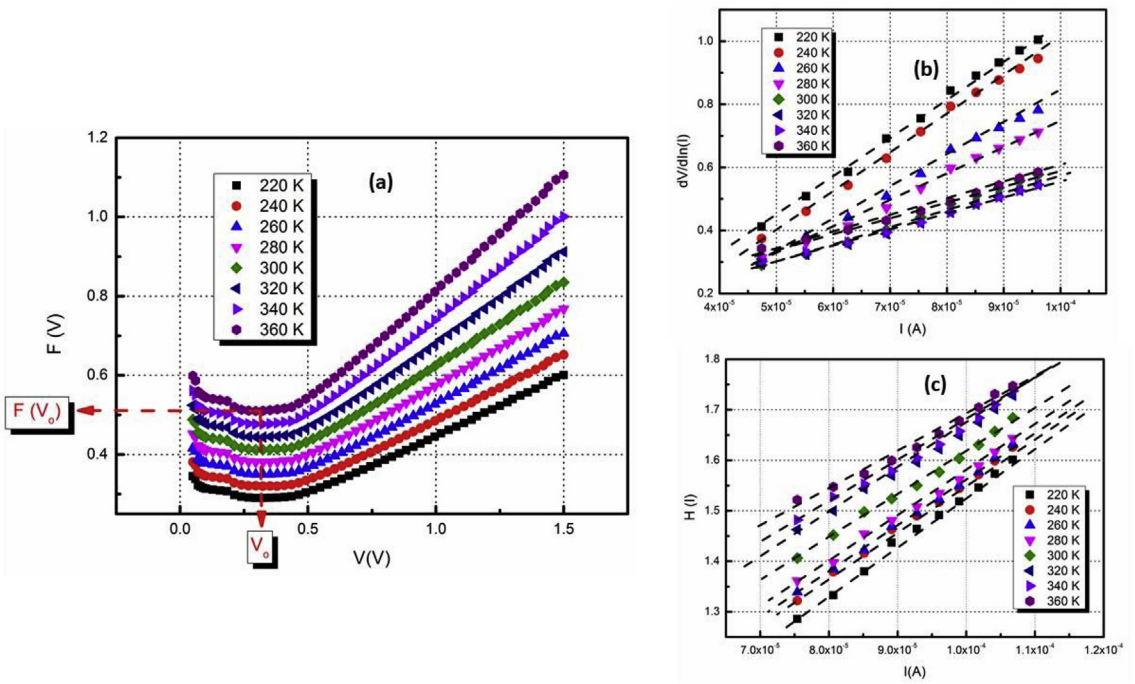

Fig. 10. (a)F(V) versus V plot (b) dV/In(I) versus I (c) H(I) versus I for CuO/n-Si Schottky diode.

Table 2
Norde and Cheung parameters for CuO/n-Si Schottky diode.

T(K)	I_0 (A)	V_0 (V)	$\varnothing_{b0}$ (Norde) (eV)	R_S- F(V) (kΩ)	R_S-dV/In(I) (kΩ)	R_S-H(I) (kΩ)
220	2.3×10^{-6}	0.32	0.37	11.9	12.4	10.0
240	2.3×10^{-6}	0.32	0.42	10.2	12.1	9.38
260	2.7×10^{-6}	0.32	0.45	9.99	10.0	9.12
280	2.9×10^{-6}	0.32	0.49	8.89	8.60	8.72
300	4.3×10^{-6}	0.32	0.53	5.46	6.11	8.44
320	5.8×10^{-6}	0.32	0.58	3.40	5.31	8.14
340	7.4×10^{-6}	0.32	0.63	2.30	5.10	7.66
360	1.3×10^{-6}	0.32	0.69	1.02	5.05	7.27

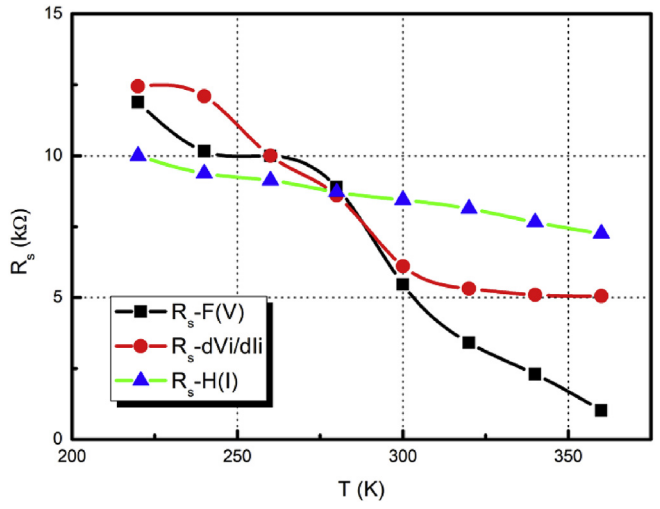

Fig. 11. R_s versus T plots for CuO/n-Si Schottky diode obtained from Norde and Cheung method.

towards the conduction band in the D_{it} curves given in Fig. 12 (a), which could be considered due to the interfacial layer at different temperature [43].

4. Conclusion

In this work, CuO/n-Si Schottky diode was fabricated by RF magnetron sputtering technique. Also, SEM, XRD and transmission measurements were carried out for CuO thin films deposited onto soda lime glass substrate to determine the material properties of CuO thin films. The deposited film was in polycrystalline nature with (111) direction as the main orientation direction. The optical band gap of the films was estimated as 2.1 eV by a Tauc plot. The current transport properties of CuO/n-Si Schottky diode was examined with TE method analyzing temperature-dependent forward bias I–V in the temperature range of 220–360 K. Analysis showed that both $\varnothing_{b0}$ and I_0 tend to increase while the ideality factor n decreases with the increasing temperature. This tendency was regarded to be depended on interface states, interfacial layer and series resistance. The deviation from the TE method was observed and this situation was evaluated with a GD of the barrier height. According to the modification of I-V analysis with Gaussian theory, the Richardson constant was determined as 110.20 A/cm^{2}K^2 and this value is consistent with the literature. The modified Norde method was used to find the values of both R_s and $\varnothing_{b0}$. The values of R_s was found to have a sharp decreasing trend with increasing temperature, which was indication of the lack of free carrier concentration at low temperatures. In addition, $\varnothing_{b0}$ values increased with increasing temperature as observed from TE method analysis. The interface state densities D_{it} values were determined by using the forward bias I-V results. It was found that interface state densities had a decreasing behavior with increasing temperature. This temperature dependence was considered as interface layer's restructuring and the reordering with the effect of temperature.

Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

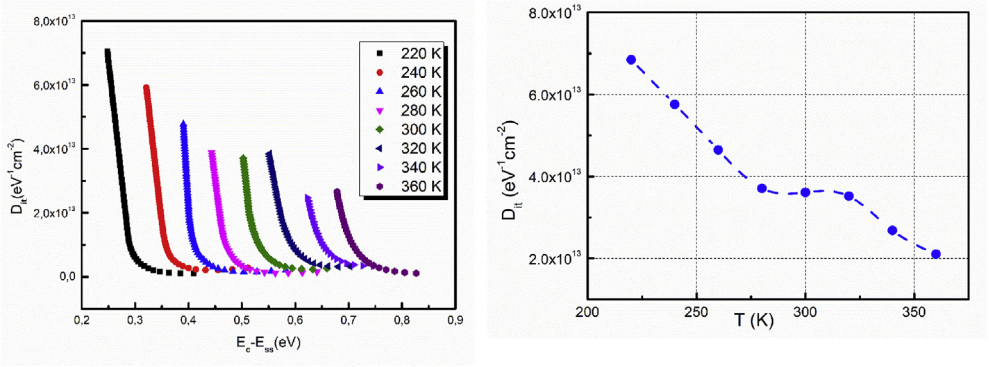

Fig. 12. (a) D_{it} versus E_c –E_{ss} and (b) variation of D_{it} values with respect to T obtained from the I–V analysis.

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