

Control of grown-in defects and oxygen precipitates in silicon wafers with DZ-IG structure by ultrahigh-temperature rapid thermal oxidation

Susumu Maeda,^{1,a)} Haruo Sudo,¹ Hideyuki Okamura,¹ Kozo Nakamura,² Koji Sueoka,³ and Koji Izunome¹

¹Base Technology, Technology, GlobalWafers Japan Co., Ltd., 6-861-5, Seiro-machi Higashiko, Kitakanbara-gun, Niigata 957-0197, Japan

²Regional Cooperative Research Organization, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

³Faculty of Computer Science and System Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

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A new control technique for achieving compatibility between crystal quality and gettering ability for heavy metal impurities was demonstrated for a nitrogen-doped Czochralski silicon wafer with a diameter of 300 mm via ultra-high temperature rapid thermal oxidation (UHT-RTO) processing. We have found that the DZ-IG structure with surface denuded zone and the wafer bulk with dense oxygen precipitates were formed by the control of vacancies in UHT-RTO process at temperature exceeding 1300 °C. It was also confirmed that most of the void defects were annihilated from the sub-surface of the wafer due to the interstitial Si atoms that were generated at the SiO₂/Si interface. These results indicated that vacancies corresponded to dominant species, despite numerous interstitial silicon injections. We have explained these prominent features by the degree of super-saturation for the interstitial silicon due to oxidation and the precise thermal properties of the vacancy and interstitial silicon. *Published by AIP Publishing*. https://doi.org/10.1063/1.5011243

I. INTRODUCTION

Recently, large-scale integration (LSI) devices, such as high-sensitivity complementary metal—oxide—semiconductor (CMOS) image sensors or 3D structure devices, require silicon wafers with high sub-surface quality and cleanliness. ^{1–5} This is due to the fact that electronic devices are installed in the surface of silicon wafers. Thus, the subsurface of a silicon wafer is required to not include any grown-in defects, such as void defects, and as-grown oxygen precipitates, i.e., the denuded zone (DZ). Essentially, Czochralski (Cz) silicon (Si) wafers include void defects since they are generally obtained from vacancy dominant crystals. In order to avoid these grown-in defect in the silicon wafers, wafer makers have developed various methods including epitaxial growth silicon wafer, batch annealed silicon wafer, and grown-in defect free silicon wafers.

Silicon wafers also possess an intrinsic gettering (IG) ability due to oxygen precipitates that aid them in avoiding the unintentional contamination of heavy metals from the subsurface. Oxygen precipitates also play a role in mechanically strengthening silicon wafers such that they resist deformation of the silicon wafer in device processes, such as over lay issue, since oxygen precipitates act as obstacles with respect to the dislocation movement in the wafer.

The structure of the DZ and IG zone in these silicon wafers is termed as "DZ-IG." They can be realized in a batch type furnace anneal by combining thermal budget and atmosphere in the furnace. The DZ-IG structure obtained by such

batch type furnace annealing mainly originates in the out diffusion of interstitial oxygen atoms in silicon wafers during the batch furnace annealing. On the other hand, Rapid Thermal Process (RTP) is a very effective tool for controlling the DZ-IG structure in the silicon wafers due to the vacancy concentration profile. With respect to previous studies for DZ-IG control by using RTP, Falster et al.8 first reported that vacancies installed by RTP enhance oxygen precipitation and the profile controls DZ-IG structure in a silicon wafer. They first experimentally demonstrated a vacancy depth profile after RTP by using a combination of platinum diffusion and Deep Level Transient Spectroscopy evaluation methods. Kissinger et al. found that the density of oxygen precipitates was proportional to the third power of vacancy concentration induced by RTP. Akhmetov *et al.* 10 also experimentally identified by precise differential Fourier Transform Infrared (IR) spectroscopy that vacancy-oxygen complexes formed by RTP were VO₄. Akatsuka *et al.*¹¹ reported that RTP with the atmosphere of argon and nitrogen enhances oxygen precipitation, while that with oxygen atmosphere suppresses it. They proposed the reason why using an oxygen atmosphere in RTP suppresses oxygen precipitation, that is, interstitial silicons are injected by the oxidation reaction and interstitial silicons become supersaturated and vacancies disappear, and then oxygen precipitation are suppressed.

Because the temperature of above-mentioned RTP studies is until 1280 °C, oxygen precipitation behavior after RTP with oxygen atmosphere above 1300 °C has not been examined. Additionally, there are few data for void defect annihilation by RTP.

Araki *et al.* ^{12–14} reported the behaviors of oxygen precipitation and void defect annihilation at above 1300 °C in RTP

a) Author to whom correspondence should be addressed: Susumu_Maeda@sas-globalwafers.co.jp

with oxygen atmosphere. They have shown that RTP above 1300 °C with an oxygen atmosphere enhanced oxygen precipitation and void defects were annihilated. They speculated that vacancy and interstitial silicon worked simultaneously to nucleate oxygen precipitates and to annihilate void defects, respectively. However, the mechanism of these types of features was not quantitatively understood from the view point of point defect analysis.

In this paper, we proposed a mechanism of formation of DZ-IG structure and void defect annihilation by Ultra High Temperature Rapid Thermal Oxidation (UHT-RTO) exceeding 1300 °C. Experimental results show notable oxygen precipitation and void defect annihilation after UHT-RTO. We have explained the experimental results by the degree of super-saturation for the interstitial silicon due to oxidation and the precise thermal properties of the vacancy and interstitial silicon. Furthermore, numerical simulation for the point defect behavior dealing with oxidation of the silicon crystal surface is proposed on the UHT-RTO processes.

II. EXPERIMENT

The samples used in the study were mirror-polished (001)-oriented Cz-Si wafers lightly phosphorous doped with resistivity 50 Ω cm and a diameter of 300 mm. The oxygen and nitrogen concentrations in the silicon wafers were $1.1-1.3\times10^{18}\,\mathrm{cm}^{-3}$ (according to the old ASTM) and $2.3-6.4\times10^{14}\,\mathrm{cm}^{-3}$, respectively. The purpose of nitrogen doping is to suppress void defect size in the as grown Cz-Si crystal and to make it easy to completely annihilate void defects by UHT-RTO as mentioned in Sec. IIIB. Furthermore, in order to reduce the void defect size, the structure of the hot zone in a pulling furnace is carefully and precisely designed, and the cooling rate for a temperature range of $1100-1000\,^{\circ}\mathrm{C}$ in the growing crystal is estimated as approximately $5.3\,\mathrm{K/min}$ by using a global heat transfer simulator, namely, CGSim. 15

The RTP was conducted with a soak time of 30s at each maximum temperature corresponding to the range of 1100–1350 °C, for a pure oxygen gas (O₂) atmosphere. The cooling rate from the maximum temperature to 700 °C was fixed at approximately 120 K/s. The two purposes of this study are as follows: (1) to investigate the effect of RTP on the oxygen precipitation behavior due to residual vacancies by RTP and (2) to investigate the effect of RTP on void

defect annihilation. With respect to purpose (1), the silicon wafers were annealed in a vertical batch furnace in pure O2 gas at 780 °C for 3 h, and this was followed by annealing at 1000 °C for 16 h (2 step anneal) to nucleate and grow oxygen precipitates after each RTP treatment. Silicon wafers after 2-step annealing were etched off in dilute hydrofluoric acid to remove oxide film and cleaved along the (110) direction through the center. The oxygen precipitates were evaluated in the center of the wafers by using the infrared (IR) tomography method employing Raytex MO-441. The detection limits for the size and the density were 25 nm and 1×10^6 cm³, respectively. On the other hand, with respect to purpose (2), chemical-mechanical polishing was used to remove material from the wafer surface to a depth of approximately 6 μ m after each RTP treatment to unify the surface condition. Average and maximum sizes of void defects in an as grown crystal were 48 nm and 90 nm, respectively, as evaluated by MO441. We have also investigated void defect annihilation by RTP with argon atmosphere, to identify the atmosphere effect by next reason. Because the argon atmosphere is considered to be a neutral on surface reaction of silicon wafer, the point defect generated in the silicon wafer heated in argon atmosphere is generally thought to be the thermal equilibrium concentration, while that heated in oxygen atmosphere is thought to be super-saturated with interstitial silicon. Subsequently, the densities of void defects that are not annihilated by RTP were inspected as Light Point Defects (LPDs) by using the laser scattering method employing KLA-Tencor Surfscan SP3. The detection limit for the size of the void defect was 40 nm. Here, the size of the void defect corresponds to length of one side of regular octahedron.

III. RESULTS

A. Oxygen precipitation behavior by UHT-RTO

Figure 1 shows the sectional view of each silicon wafer after RTP and 2-step annealing as obtained by IR tomography. Figure 2 also shows the density-distribution of oxygen precipitates in the depth direction of the silicon wafers shown in Fig. 1. In the images shown in Fig. 1, the upper side corresponds to the surface of the silicon wafers, and the bottom side is $330 \, \mu m$ from the surface (that is near the center of depth). The width of each image is approximately $260 \, \mu m$. Small black dots in the images correspond to the scattering images

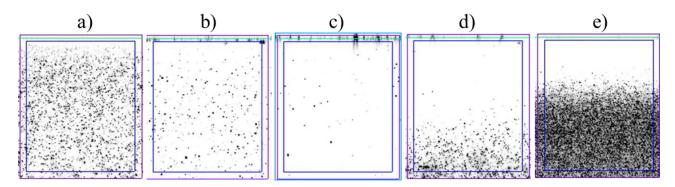


FIG. 1. Sectional images of scattering infrared method for oxygen precipitates in silicon wafers after Rapid Thermal Oxidation and 2 Step anneal, $780 \,^{\circ}\text{C} \times \text{H} + 1000 \,^{\circ}\text{C} \times 16\text{H}$, RTO temperature of (a) $1100 \,^{\circ}\text{C}$, (b) $1200 \,^{\circ}\text{C}$, (c) $1250 \,^{\circ}\text{C}$, (d) $1300 \,^{\circ}\text{C}$, and (e) $1350 \,^{\circ}\text{C}$.

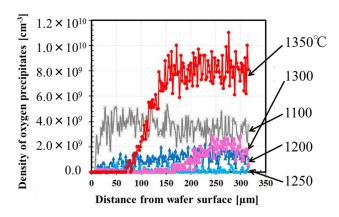


FIG. 2. Distribution of oxygen precipitation density after Rapid Thermal Oxidation and 2 Step anneal, $780\,^{\circ}\text{C} \times 3\text{H} + 1000\,^{\circ}\text{C} \times 16\text{H}$, obtained by the scattering infrared method.

by oxygen precipitates. In the case of RTP temperature corresponding to 1100°C [Fig. 1(a)], oxygen precipitates are uniformly distributed in the silicon wafer from the surface to the bulk, and the density gradually decreases with increases in temperature corresponding to 1250 °C as shown in Figs. 1(b) and 1(c), respectively. We have thought that the defects shown in Figs. 1(a)-1(c) were un-dissolved as grown oxygen precipitates by the RTO treatment. This is a feature of oxygen precipitates in Cz-Si crystal doped with nitrogen since the size of as grown oxygen precipitates increases by nitrogen doping. 16 We assumed that re-formed oxygen precipitates by 2 step anneal in these RTP temperature ranges (1100, 1200, and 1250 °C) were absent since effective vacancies for an oxygen atmosphere in RTP at these temperature were absent, similar to the report by Akatsuka. 11 In contrast, in the case of 1300 °C, new re-formed oxygen precipitates appeared in the bulk of the silicon wafer [Fig. 1(d)]. Furthermore, they were significantly enhanced by increasing the RTO temperature by 50 °C until 1350 °C [Fig. 1(e)]. It is important to note that an outstanding DZ-IG structure is obtained in which oxygen was not precipitated near the surface, while oxygen is precipitated remarkably in the bulk of the silicon wafers by UHT-RTO above 1300 °C.

An important feature of these oxygen precipitates that is mentioned here is well reproduced in the depth profile shown in Fig. 2. It should be noted that the density of oxygen precipitate for RTO temperature of 1350°C appears to saturate at approximately $8 \times 10^9 \,\mathrm{cm}^{-3}$ in the bulk of the wafer. This is due to the detection limit of the higher density side with the evaluation apparatus, MO441. As shown in Fig. 1(e), scattered light images overlap each other, and the apparent density is saturated to $8 \times 10^9 \,\mathrm{cm}^{-3}$ when the density was above $5 \times 10^9 \,\mathrm{cm}^{-3}$. Precise density should be evaluated by using an alternate method. We will report this type of reliable data on the density by using Transmission Electron Microscopy (TEM) in near future. It is widely known that oxygen precipitates inducted after RTP are assisted by residual vacancies introduced by RTP.8-11 However, Akatsuka et al.11 reported that oxygen precipitation by RTP with O₂ atmosphere under 1280 °C was suppressed, since interstitial silicon atoms are injected from the oxidation surface, and they become dominant in the silicon wafer after RTP. Nevertheless, our experimental results that oxygen precipitation was enhanced by the RTP with oxygen atmosphere above 1300 °C suggest that the vacancies became dominant point defect species. These prominent features for oxygen precipitation are discussed in Sec. IV on point defect behavior.

B. Void defect annihilation by UHT-RTO

Figure 3 shows the relationship between LPD densities and the RTP temperatures with an LPD map that shows the distribution in the wafer. The vertical axis denotes LPD density exceeding 40 nm. In the case without RTP, the level of LPD density was approximately 30 cm⁻². We confirmed the origin of the LPDs by Scanning Electron Microscopy (SEM) wherein almost all LPDs were void defects. In the case of temperatures from 1100 °C to 1200 °C, the LPD density hardly decreased independent of the atmosphere in the RTP. In contrast, the LPD density decreased when the temperature was above 1300 °C, and it significantly decreased due to O₂-RTP than that for Argon-RTP. In the case of O₂-RTP, most of the void defects were annihilated, and the level of the density was void-free, namely noise level. However, in the case of Argon-RTP, void defects remained in the center of the wafer as shown in the LPD map. Because RTO above 1300 °C enhances the annihilation effect of void defects, it is thought that interstitial silicon atoms in RTP with oxygen atmosphere are in the state of super saturation, while that in RTP with argon atmosphere correspond to thermal equilibrium state. These prominent features of void defect annihilation are discussed in Sec. IV.

IV. DISCUSSION

As mentioned above, the experimental results for oxygen precipitation suggested that vacancies were dominant in the silicon wafers conducted in RTO above 1300 °C. Conversely, the experimental results for void defect annihilation suggested that interstitial silicon was super-saturated in the UHT-RTO wafers. Initially, it appears that the two results are contradictory. This section discusses the prominent feature by using a point defect model that considers the oxidation of silicon.

It is widely accepted that interstitial silicon atoms are generated at the interface between oxide film and silicon crystal during oxidation. ^{17–19} Majority of the interstitial silicon

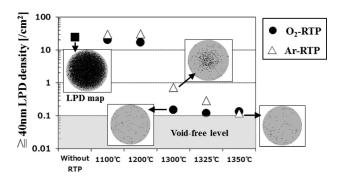


FIG. 3. Relation between the maximum temperature in RTP and LPD density at the surface of silicon wafers after the Rapid Thermal Process. A few of the images of LPDs map for the complete silicon wafer. Size of LPDs evaluated here exceeds 40 nm.

generated is spent for the formation of oxide film although a few are injected to the silicon crystal. Taniguchi *et al.* ¹⁹ reported the dependence of super-saturation of interstitial silicon in the silicon crystal surface, namely C_I above C_I^{eq} , on the growth rate of the oxide film or dXo/dt as follows:

$$\frac{C_{I}}{C_{I}^{eq}} = \frac{A1 (dX_{o}/dt) + A2}{(dX_{o}/dt)^{0.5} + A2},$$
(1)

where C_I denotes the concentration for interstitial silicon, C_I^{eq} denotes the thermal equilibrium concentration for interstitial silicon, Xo denotes the thickness of the oxide film, t denotes oxidation time, and A1 and A2 in Eq. (1) denote parameters related with physical properties for oxidation of silicon. They are expressed as follows:

$$A1 = \frac{\theta}{a_{\rm I} C_{\rm I}^{\rm eq}},\tag{2}$$

$$A2 = \frac{K_I}{a_I},\tag{3}$$

$$a_{\rm I} = m \left(\frac{NK^{\rm O}D_{\rm I}^{\rm O}}{K_{\rm L}}\right)^{0.5}. \tag{4}$$

Here, θ denotes mole of silicon atoms ejected as interstitial silicon at oxidation interface for each mole of silicon oxidized into S_iO_2 , K_I denotes reaction constant for annihilation of interstitial silicon at oxidation interface, m denotes segregation coefficient for interstitial silicon at the oxidation interface, N denotes number of oxidant molecules incorporated into a unit volume of oxide layer, K^O denotes reaction constant between oxidant and interstitial silicon in oxide layer, D_I^O denotes diffusion constant for interstitial silicon in oxide layer, and K_L denotes reaction constant for formation of oxide layer. Nakamura²⁰ determined parameters A1 and A2 by using data for the oxidation of silicon as reported by Dunham¹⁸ and Suezawa *et al.*²¹ as follows:

A1 =
$$6.473 \times 10^4 \exp\left(\frac{1.62}{k} \left(\frac{1}{T} - \frac{1}{1150}\right)\right) (s/cm)^{0.5}$$
, (5)

$$A2 = 4.45 \times 10^{-5} \exp\left(-\frac{E}{k} \left(\frac{1}{T} - \frac{1}{1150}\right)\right) (cm/s)^{0.5}. \quad (6)$$

The activation energy term in Eq. (6), E, is set to 6.0 eV for temperature over 1150°C, and 0.55 eV for less, respectively. The lines in Fig. 4 show the dependence of super-saturation of the interstitial silicon on the growth rate of oxide film at each oxidation temperature as obtained by Eq. (1) with A1 and A2.²⁰ Supersaturation of interstitial silicon increases with increases in the growth rate of oxide film although it decreases with increases in the oxidation temperature. We experimentally investigated the growth rate of oxide film in our RTP by using methods similar to those reported by Kotani and Omura.²² Dots in Fig. 4 denote C_I/C_I^{eq} for each RTO temperature obtained from the growth rate of oxide film at the end of the soak. Basically, this value of C_I/C_I^{eq} is quickly attained uniform in the whole of silicon wafer, since diffusion of interstitial silicon is very fast. Thus, there is no difference of the supersaturation regardless of the wafer position at the end of

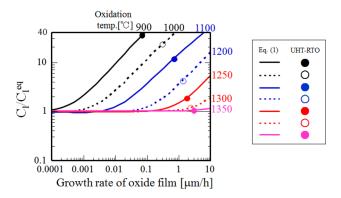


FIG. 4. Dependence of the super-saturation of interstitial silicon on the growth rate of oxide film. Lines for each oxidation temperature are derived from Eq. (1) proposed by Taniguchi *et al.* Dots express C_1/C_1^{eq} derived from the growth rate of oxidation film for the end of soak in our RTO apparatus.

soak of the RTP process. Figure 5 shows the dependence of super-saturation of interstitial silicon on the oxidation temperature in our RTP obtained from dots in Fig. 4. Evidently, $C_{\rm I}/C_{\rm I}^{\rm eq}$ decreases rapidly with increases in the RTO temperature and approaches 1.0. This corresponds to the thermal equilibrium state for intrinsic point defect. Concentration of interstitial silicon is estimated from Fig. 5 using the value for the thermal equilibrium concentration for interstitial silicon. ²³

Figure 6 shows the relation between oxidation temperature and intrinsic point defect concentration. The blue solid line shows the thermal equilibrium concentration of interstitial silicon as reported, ²³ and this increases with increases in the temperature. The concentration of interstitial silicon at the end of duration of the RTP as obtained by Eq. (1) is denoted by a blue dashed line. As shown in the figure, interstitial silicon is evidently in the state of super saturation in all temperature ranges although its degree gradually reduces, and the concentration approaches the thermal equilibrium value with increases in the temperature. Conversely, the red solid line denotes the thermal equilibrium concentration for vacancy, ²³ and it slightly exceeds that for interstitial silicon. The concentration of vacancy (denoted red dashed line) is derived from the mass action law that is given as follows:

$$C_V C_I = C_V^{eq} C_I^{eq}, \tag{7}$$

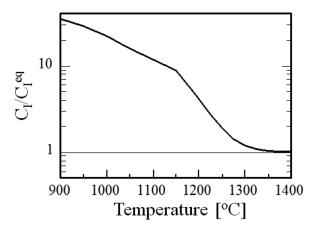


FIG. 5. Dependence of the super-saturation of interstitial silicon on oxidation temperature in our RTO at the end of $30\,\mathrm{s}$.

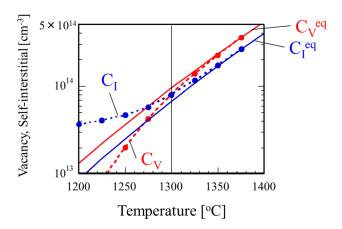


FIG. 6. Relation between oxidation temperature and intrinsic point defect concentration. Solid lines show the thermal equilibrium concentration of the point defect and the broken line denotes the real concentration.

where C_V denotes the vacancy concentration and C_V^{eq} denotes the thermal equilibrium concentration for vacancy. Evidently, the vacancy is under-saturated although it approaches the thermal equilibrium with increases in the temperature in a manner similar to that of interstitial silicon. With respect to the actual concentration, the vacancy is lower than that of interstitial silicon when the temperature is lower than $1300\,^{\circ}$ C. However, the difference gradually reduces with increases in the temperature, and the vacancy concentration exceeds that for interstitial

silicon when the temperature is above 1300 °C. Thus, it is notable that a specific relation of the point defects, namely vacancy, is dominant although interstitial silicon is supersaturated when the temperature is above 1300 °C. The reason as to why interstitial silicon and vacancy approach the thermal equilibrium with increases in the oxidation temperature is as follows. With increases in the temperature, the generation of interstitial silicon decreases since the compressive stress in the oxide film that is the driving force of the interstitial silicon generation in the oxide film decreases. This is due to lowering viscosity of oxide film with increases in the temperature. Finally, excess interstitial silicon due to oxidation does not generate when the temperature is near the melting point. Thus, this state corresponds to thermal equilibrium.

Next, our numerical simulation model for point defect in UHT-RTO that considers oxidation of silicon is introduced. A silicon wafer was modeled as a dimension in the depth direction [denoted Z in Eq. (8)] from the surface to the center of wafer thickness, and this is approximately 380 μ m. The RTP process was entirely simulated from the beginning of the ramping up temperature (700 °C) to the end of cooling down with proper time step based on the temperature. A pure O_2 atmosphere in RTP is postulated in the simulation. The boundary condition for interstitial silicon at the interface between oxide film and surface of silicon wafer is given by Eq. (1). Vacancy concentration at the interface between oxide film and surface of silicon wafer is determined by the mass action

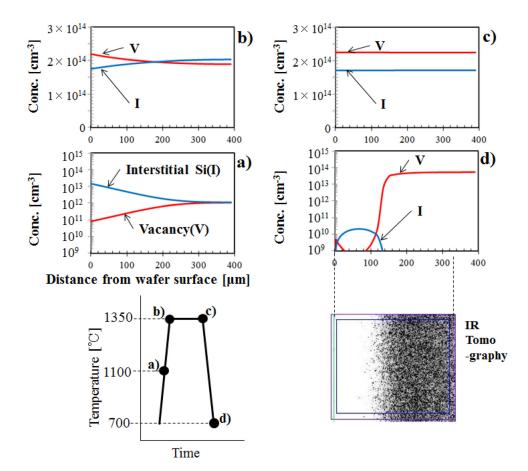


FIG. 7. Change in the point defect distribution in the wafer depth direction during RTP with 1350 °C as obtained by the numerical simulation. During heating (a), reaching the maximum temperature (b), end of soak (c), and end of cooling (d). Corresponding image of IR tomography [Fig. 1(e)] is also shown.

law as expressed in Eq. (7). The boundary condition for the point defects at the center of the wafer thickness is given by the symmetry condition. (That means no flux of point defect, $dC_{I,V}/dZ=0$ at the center of wafer thickness.) The initial condition for the concentration of point defects is set to thermal equilibrium value at $700\,^{\circ}\text{C}$ that is initial temperature, from the surface to the center of wafer thickness. Given these boundary conditions, the diffusion of interstitial silicon and vacancy was calculated by considering pair annihilation and pair generation based on the following equations:

$$\frac{\partial C_{I,V}}{\partial t} = D_{I,V} \frac{\partial^2 C_{I,V}}{\partial Z^2} - K_{IV} \left(C_V C_I - C_V^{eq} C_I^{eq} \right), \tag{8}$$

$$K_{IV} = 4 \pi \left(D_V + D_I \right) a_c \exp \left(-\frac{\Delta G_{IV}}{kT} \right),$$
 (9)

where D_V denotes the diffusion constant for vacancy, D_I denotes the diffusion constant for interstitial silicon, a_c denotes the critical distance between vacancy and interstitial silicon atom where pair annihilation occurs, and ΔG_{IV} denotes the barrier energy for pair annihilation. Nakamura $et\ al.^{23}$ investigated thermal properties for intrinsic point defects in detail to fit behavior of grown-in defects in an as-grown silicon single crystal. In Ref. 23, although there are several combinations of thermal properties for point defects in Table 2, those listed in the 4th column from the top were used in this study. a_c was set 0.543 nm in this study. Additionally, ΔG_{IV} was set as zero similar to Ref. 9, and this implies that the time constant for

pair annihilation is mainly determined by encounter probability between vacancy and interstitial silicon. Effect of nitrogen and oxygen forming their complex with vacancy was ignored in the study. The results of numerical simulation for RTP temperature corresponding to 1350 °C are shown in Fig. 7. Each figure in Fig. 7 shows the change in the distributions of point defect concentration in the depth direction of silicon wafer when the RTP process progresses as denoted by (a), (b), (c), and (d) in Fig. 7. During the temperature increase [Fig. 7(a)], oxidation begins, and interstitial silicon atoms are actively introduced from the oxidation interface. Vacancy concentration at this moment is considerably low when compared to that for interstitial silicon. However, when the temperature reaches a maximum, the vacancy concentration exceeds that for interstitial silicon in the vicinity of the surface although the state mainly corresponds to a non-equilibrium state where the concentration of interstitial silicon slightly exceeds that of vacancy in the deep region of the silicon wafer [Fig. 7(b)]. At the end of the duration, both concentrations become almost steady, and the concentration of vacancy exceeds that of interstitial silicon in the complete wafer [Fig. 7(c)]. Finally, vacancies dominantly remain in the bulk of the silicon wafer when the process was completed, as shown in Fig. 7(d), since rapid cooling commences from the state of vacancy dominant [Fig. 7(c)] and pair annihilation (Pair annihilation reduces vacancies and interstitial silicon atoms by the same number.) is the main reaction of the point defect. It should be noted that the interstitial silicon dominant region was developed from the surface to

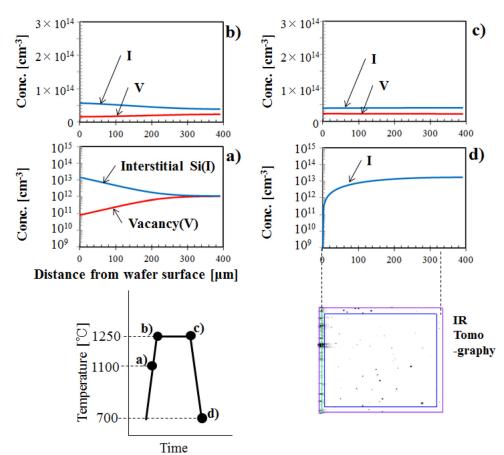


FIG. 8. Change in point defect distribution in the wafer depth direction during RTP with 1250 °C as obtained by the numerical simulation. During heating (a), reaching the maximum temperature (b), end of soak (c), and end of cooling (d). Corresponding image of IR tomography [Fig. 1(c)] is also shown.

a depth of approximately $100 \,\mu\text{m}$ in the silicon wafer. This is due to the injection of interstitial silicon by the oxidation of silicon during the RTP cool down. Thus, significant oxygen precipitation occurs in the bulk of the wafer in accordance with the vacancy profile and apparent DZ is observed since their effective vacancies in the subsurface are absent as shown in the IR tomography image in Fig. 7.

Conversely, the results for RTO temperature at 1250 °C are shown in Fig. 8. During heating [Fig. 8(a)], the distribution of point defect concentration is the same as that at 1350 °C [Fig. 7(a)] since the condition of heating up in RTP was unified. When the temperature reaches a maximum [Fig. 8(b)], the concentration of interstitial silicon considerably exceeds that for vacancy [Fig. 8(b)] since the temperature is lower and super-saturation of interstitial silicon is well emphasized in this temperature range as shown in Figs. 5 and 6. This is in contrast to the case at 1350 °C. The situation involves maintaining interstitial silicon dominant to the end of duration as shown in Fig. 8(c). Finally, interstitial silicon remains dominantly in the silicon wafer when the process is completed as shown in Fig. 8(d). Thus, oxygen precipitation does not occur after subsequent annealing as shown in the IR tomography image in Fig. 8. Our numerical simulation model explains our experimental results for oxygen precipitates. More precise simulation results that consider nitrogen and oxygen that form their complexes with vacancy will be reported in another paper.

Void defects that are widely known as Crystal Originated Particles (COPs) are aggregates of vacancies. Typical morphology corresponds to an octahedron with the size corresponding to several tens of nanometers. They include oxide film on the inner wall. With respect to the elimination of void defect by RTP, they commence from the dissolution of the oxide film at the inner wall. The use of UHT-RTO with temperature above 1300 °C leads to significant advantages since oxygen solubility significantly exceeds the oxygen concentration in the silicon wafer. Thus, the oxide film easily dissolves in the complete silicon wafer, while that for conventional batch anneal (Typically, temperature of batch anneal is 1200 °C.) is simply limited to the subsurface due to the out diffusion of interstitial oxygen. After the oxide film is removed and if interstitial silicon is in the state of super saturation, then interstitial silicon atoms are injected to the void defect, and elimination is finally completed. Although vacancies are dominant when the temperature is above 1300 °C, interstitial silicon is in the state of super-saturation as shown in Figs. 5 and 6 such that the void defect disappears quickly. Numerical simulation for void defect elimination will be reported in another paper.

V. CONCLUSION

In this study, we demonstrated the formation of the DZ-IG structure in silicon wafer by using UHT-RTO technology. An apparent DZ-IG structure was observed in UHT-RTO temperatures corresponding to 1300 °C and 1350 °C. Thus, the subsurface region corresponded to the denuded zone, and a bulk region with a high density of oxygen precipitates was present. The annihilation effect of void defects in UHT-RTO above 1300 °C exceeded that of Ar-RTP. These experimental results indicated that vacancies were dominant and interstitial silicons were super-saturated in UHT-RTO temperatures corresponding to 1300 °C and 1350 °C. We explained our experimental results by point defect model that considers the oxidation reaction of silicon.

¹T. Hattori, *Ultraclean Surface Processing of Silicon Wafers* (Springer-Verlag, Berlin, Heidelberg, 1998), p. 39.

²P. S. D. Lin, R. B. Marcus, and T. T. Sheng, J. Electrochem. Soc. **130**, 1878 (1983).

³K. Saga, Electrochem. Soc. Trans. **69**(8), 57 (2015).

⁴K. Okonogi, K. Miyoshi, and A. Toda, NEC Res. and Dev. **42**(1), 59 (2001).

⁵J. F. Shepard, Jr., W. A. Muth, and S. MacNish, "Experimental investigation of the rapid thermal process slip window," in *18th IEEE Conference on Advanced Thermal Processing of Semiconductors* (2010), p. 28.

⁶K. Sueoka, S. Sadamitsu, Y. Koike, T. Kihara, and H. Katahama, J. Electrochem. Soc. **147**, 3074 (2000).

⁷K. Araki, H. Sudo, T. Aoki, T. Senda, H. Isogai, H. Tsubota, M. Miyashita, H. Matsumura, H. Saito, S. Maeda, K. Kashima, and K. Izunome, Jpn. J. Appl. Phys., Part 1 49, 080205 (2010).

⁸R. Falster, M. Pagani, D. Gambaro, M. Cornara, M. Olmo, G. Ferrero, P. Pichler, and M. Jacobet, Solid State Phenom. 57, 129 (1997).

⁹G. Kissinger, J. Dabrowski, A. Sattler, C. Seuring, T. Müller, H. Richter, and W. von Ammon, J. Electrochem. Soc. 154(6), H454 (2007).

¹⁰V. Akhmetov, G. Kissinger, and W. von Ammon, Physica B 404, 4572 (2009).

¹¹M. Akatsuka, M. Okui, N. Morimoto, and K. Sueoka, Jpn. J. Appl. Phys., Part 1 40, 3055 (2001).

¹²K. Araki, S. Maeda, T. Senda, H. Sudo, H. Saito, and K. Izunome, ECS J. Solid State Sci. Technol. 2(3), P66 (2013).

¹³K. Araki, S. Maeda, T. Senda, H. Sudo, T. Aoki, and K. Izunome, ECS Solid State Lett. 3(9), P114 (2014).

¹⁴K. Araki, H. Sudo, and S. Maeda, ECS Solid State Lett. 4(9), P63 (2015).

¹⁵V. V. Kalaev, J. Cryst. Growth 303, 203 (2007).

¹⁶S. Maeda, K. Nakamura, K. Hayashida, and K. Sugisawa, in *Proceedings of the Silicon Technology Division* (Japan Society of Applied Physics, 2000), Vol. 68, p. 13.

¹⁷S. M. Hu, Appl. Phys. Lett. **43**, 449 (1983).

¹⁸S. Dunham, J. Appl. Phys. **71**, 685 (1992).

¹⁹K. Taniguchi, Y. Shibata, and C. Hamaguchi, J. Appl. Phys. **65**, 2723 (1989).

²⁰K. Nakamura, in 190th Proceedings of the Silicon Technology Division (Japan Society of Applied Physics, 2016).

²¹M. Suezawa et al., Appl. Phys. Lett. **93**, 101904 (2008).

²²Y. Kotani and Y. Omura, Jpn. J. Appl. Phys., Part 1 **39**, 4549 (2000).

²³K. Nakamura, T. Saishoji, and J. Tomioka, Solid State Phenom. 82–84, 25 (2002).