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Fabrication of Crystalline Si Thin Films for Photovoltaics

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Crystalline Si (c-Si) thin films have been widely studied for their application to solar cells and flexible electronics. However, their application at large scale is limited by their fabrication process. As reviewed in this paper, many approaches have been studied, but only some of them have been made into large-scale industrial production. The standard wire sawing of Si ingots cannot be scaled down to produce thin c-Si wafers and films due to the brittle nature of c-Si material, the resulting significant thickness variations, and the waste of material. Therefore, techniques based on the kerf-less processes including "top-down" and "bottom-up" approaches have been developed in recent decades. In this review, photovoltaic applications of thin c-Si wafers with thicknesses ranging from 50 µm down to 1 µm are presented first. Then, methods to fabricate c-Si thin films based on both approaches are detailed, including slim-cut, "smart-cut," epi-free, as well as various growth processes such as molecular beam epitaxy, liquid phase epitaxy, ion beam, and chemical vapor deposition processes at a wide range of growth temperatures, from 1000 °C down to 150 °C. The advantages and disadvantages of these methods are presented and compared.

1. Introduction

In the field of photovoltaic solar energy, a wide variety of materials such as perovskite,[1–3] hydrogenated amorphous Si (a-Si:H),[4,5] copper indium gallium selenide,[6–8] and III-V materials[9–16] have been used as light absorption materials. However, their commercialization is limited by scale up issues, reduced conversion efficiency, poor stability, and/or the use of toxic and/or scarce materials.[17,18] In contrast, c-Si solar cells have taken the leadership of industrial PV because they are cheap to produce, have a life of more than 30 years (SunPower has announced recently 40 years warranty) and have reached a high power conversion efficiency of up to 26.7%.[19,20] However, the standard wafer production method wastes a lot of Si material throughout the wire sawing process. According to the ITRPV report, the kerf loss of diamond multiwire sawed Si wafers in 2021 was around 60 µm per Si wafer, as shown in **Figure 1**, for a wafer thickness of roughly 160 µm. Wafer thinning is the part of the standard Si wafer processing.[21] Among the various methods to achieve that, mechanical thinning of wafers consists in removing Si material by using a grinding wheel; a polishing pad and water or chemical abrasive slurry. This includes mechanical grinding[22,23] and chemical mechanical polishing.[23–25] Wafer thinning realized via the chemical etching through a wet chemical etching agent[26] or dry gas plasma chemical reactions with Si material.[27] However, a significant part of the original material is lost during the thinning process. Even though this thickness is expected to be reduced to 140 µm in the next decade, the kerf losses will remain important and thickness reduction below that value will be extremely challenging due to the brittle nature of c-Si and handling issues. However, from an optical point of view, thicknesses well below 100 µm would be sufficient to achieve high conversion efficiencies and thus allow for a significant material usage and cost reduction.[28]

Figure 2a shows an interference microscope image of a wafer cut with a 100 µm wire with diamond particle sizes of 10–20 µm, while Figure 2b is a similar image on a wafer cut with a wire with a diameter of 120 µm and particle sizes of 12–25 µm (other cutting parameters remain unchanged). It can be seen that even a small increase in diamond particle size leads to the removal of large chunks of Si.[29] As shown in Figure 2c, a scanning electron microscopy (SEM) image of the surface of a poly-Si wafer displays micron-scale saw marks that are produced by diamond particles scratching the Si surface. Continuous scratching of the poly-Si surface by diamond abrasive particles may result in brittle cracking or chipping.[30] Another issue with sawing thin Si wafers is that the wafer thickness after thinning varies significantly.[31] Currently, the wire sawing process with a kerf width of about 60 µm results in a total thickness variation of about 18 µm. Therefore, the standard wafering is not suitable to produce c-Si thin wafers (<50 µm).

To further reduce the wafer thickness, alternative technologies are needed. In the past few decades, a number of novel concepts have been developed to produce kerf-less c-Si wafers with thicknesses below 50 µm and have been successfully applied, as shown in **Figure 3** and **4**. On the other hand, c-Si films with

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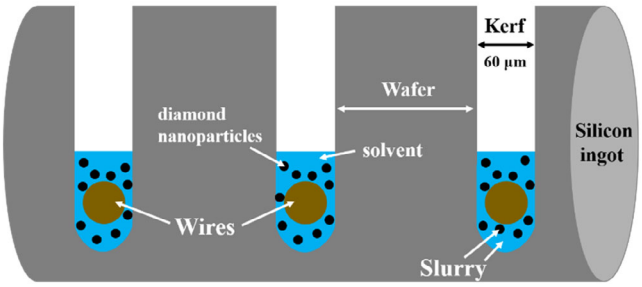

Figure 1. Schematic diagram of traditional diamond multiwire saw for cutting Si wafers. The large brown dots represent diamond the wires. The slurry is made of a solvent (blue) and diamond nanoparticles (black dots).

a thickness of ≤50 μm, which is equivalent to a quarter of the thickness of the standard c-Si solar cell substrate, can also be used to achieve the mechanical flexibility.[32] Within the "top-down" methods (Figure 3), we can see a 50 μm solar cell processed on an exfoliated c-Si layer obtained by electroless and electrodeposit-assisted stripping, which achieved a power conversion efficiency of 14.5%.[33] Similarly, a 48 μm kerf-less c-Si film produced by proton implant exfoliation technique has been used in solar cells with an efficiency of 14.1%.[34] In addition, the random Si nanohole arrays and laser fired contact process were applied to the kerf-less c-Si film with an efficiency of 17.1%.[35] 25 μm c-Si films produced by spalling technology were used as the absorption layer of the solar cell, achieving an efficiency of 12.5%,[36] while the efficiency of the solar cells using the improved intrinsic thin layer of a-Si/c-Si (25 μm) heterojunction was 13.3%.[37] The efficiency of 1 μm c-Si solar cells prepared by the "Epifree" process was 2.6%, which could be increased to 4.1% after passivation.[38] Nano texturation of such kind of solar cells can further increase their efficiency to 8.6% with an effective thickness of only 830 nm.[39]

The second approach to produce thin c-Si solar cells shown in Figure 4 is based on c-Si films prepared by "bottom-up" methods. The efficiency of c-Si solar cells (50 μm) produced by plasma-assisted epitaxy growth and subsequent hydrogen annealing to form a self-organizing nanogap which allows to detach the epitaxial layer from the parent substrate is 11.4%.[40] Solar cells with a 40 μm c-Si absorber produced from the epitaxial process based on porous Si developed by Brendel[41,42] have reached an efficiency of 20.44%.[43] The efficiency of epi-PECVD heterojunction c-Si solar cells on glass by anodic bonding and mechanical cleavage is 7.3%, and the J_{sc} produced by ultra-thin (5.5 μm) epitaxial layers is 21.5 mA cm^{-2}.[44] With the application of inverted nanopyramids on the front side of 3 μm c-Si solar cell, J_{sc} could be further boosted to 25.3 mA cm^{-2}.[45]

Ultrathin solar cells have the unique advantage to be at least ten times thinner than conventional solar cells, resulting in efficient material savings, shorter deposition times, and being more tolerant to defects because the required diffusion length for photogenerated carriers is reduced. For Si solar cells, decreasing the wafer from 160 to 50 μm can reduce both manufacturing cost and capital expenditure.[46] Furthermore, for thicknesses as low as 10 μm, the conversion efficiency is expected to exceed 28.5%.[47,48] However, as the c-Si thickness decreases, the complexity of strategies for enhancing light absorption increases significantly. Solar cells with thicknesses less than 10 μm require delicate fabrication techniques to create absorber layers (epitaxial growth, recrystallization, and layer transfer) and submicron textures with new geometries. Moreover, several technical challenges hinder the realization of practical devices. In this article, different fabrication methods for c-Si ultrathin solar cells are reviewed, and their advantages and disadvantages are compared.

2. "Top-Down" Approaches

In order to avoid material losses during the thinning process, more efficient methods for fabricating thin c-Si wafers are desirable. With kerf-less lift-off processes, wafer thicknesses of less than 100 μm can be achieved with minimal Si waste. Such kind of wafers and foils are much thinner than existing wafers (160–180 μm), and allow producing flexible devices. There are many ways to prepare c-Si thin films, among which stress-induced lift-off (slim-cut) or spalling technology,[49–56] smart-cut technology,[57–59] and epifree technology[38,60] are the most developed. These technologies have been brought at industrial level by companies such as Siltectra and Fraunhofer ISE[61] for slim-cut.

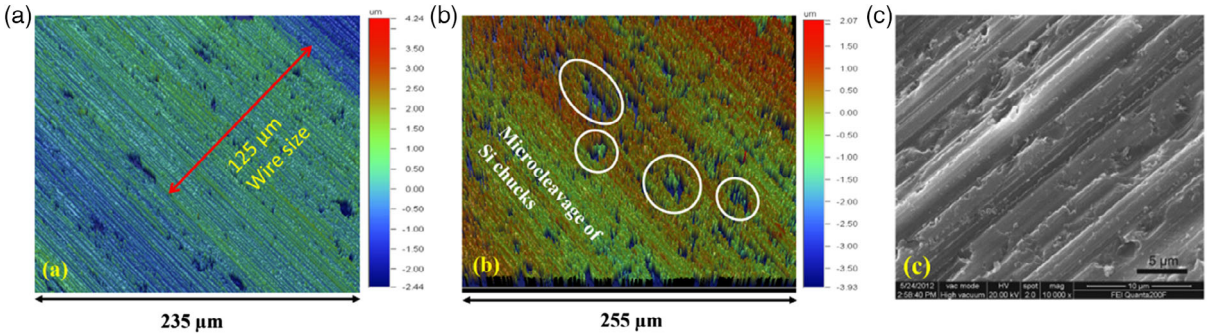

Figure 2. Interference microscope image of a Si wafer cut by a wire of a) 100 μm (diamond size = 10–20 μm) and b) 120 μm (diamond size = 12–25 μm). The microcleavage areas are indicated by white circles. Reproduced with permission.[29] Copyright 2016, AIMS Press. c) SEM image of a polycrystalline Si cut by diamond wire saw. Reproduced with permission.[30] Copyright 2014, Elsevier.

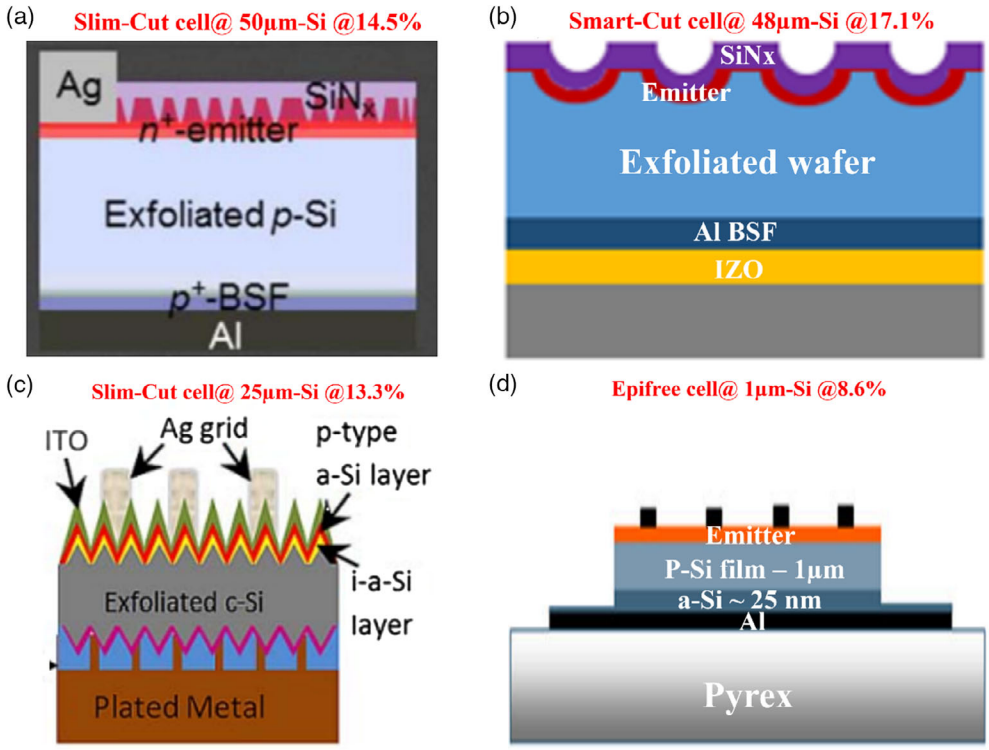

Figure 3. Solar cell applications of c-Si films (<50 µm) prepared by "top-down" approaches. a) Highly stressed Ni film is electrodeposited as the stress layer for lift-off of the Si thin film and Si solar cells are prepared with a 50 µm thick spalled Si layer. Reproduced with permission.[33] Copyright 2018, IOP Science. b) As-cleaved wafers after proton implantation were annealed in N_2 at 900 °C for 10 min and solar cells are produced based on the exfoliated-thin wafers. Reproduced under the terms of the CC-BY license.[35] Copyright 2018, Springer Nature. c) Single heterojunction solar cells with a 25 µm c-Si layer exfoliated by electrochemically deposited metal stress layers. Reproduced with permission.[37] Copyright 2014, The Optical Society. d) High-quality c-Si film obtained by the epifree process is separated by anodic bonding to prepare solar cells. Reproduced with permission.[38] Copyright 2010, Wiley-VCH.

2.1. Slim-Cut

The stress-induced lift-off method (Slim-cut) produces thin Si foils by applying external stress layers, which have different thermal expansion coefficients compared to c-Si. Tanielian first described the stress-induced stripping technology of monocrystalline Si thin films in 1985.[62] Several techniques can be used to deposit the metallic layers, including screen-printed metal paste,[51] electrochemical deposition,[36] thermal evaporation,[53] and sputter-deposition.[63] The method consists of four steps: 1) depositing a stress-inducing layer on a Si wafer, 2) heat-treating the stress-induced layer, 3) crack initialization and detach the thin Si layer, and 4) chemical cleaning to remove the stress-inducing layer.

Screen printing[64] of a metal paste requires screen presses and belt heating furnaces to apply a metal paste[49,51,65] as a stress-inducing layer to obtain high-quality wafers in the thickness range of 50 µm. **Figure 5** shows an example of the film after being stripped from the parent substrate. However, the application of this method is severely limited by the high temperatures (≈900 °C) required to generate stress and the occurrence of spontaneous fracture upon cooling.[63,66] Layer spalling of prefabricated devices is not possible because spontaneous fracture almost always results in film cracking at high temperatures.[67]

Compared to screen-printed metal paste, electrodeposited and thermally evaporated metal films have stronger adhesion and greater stress, which is beneficial for stripping films. In this way, the temperature required to induce a high enough stress is lower than in the previous case. The basic principle of the exfoliation process is displayed in **Figure 6**a. After the electroplating process is completed, the exfoliation is carried out in two different ways, namely spontaneous exfoliation and controlled exfoliation. For the former method, a rapid thermal annealing (RTA) system was used at different temperatures (300–400 °C) for 5 min. After cooling in the RTA system, the Si layer spontaneously fell off due to the propagation of subsurface cracks. During the controlled spalling process, laser and mechanical wedge form an initial subsurface crack at or near the edge of the stress layer, then the locally separated Si is gripped with tweezers and stretched it in the vertical direction. Subsequently, the Si was completely exfoliated from the c-Si donor matrix.[68] During annealing, an internal stress develops due to the thermal expansion mismatch between the metal layer and the c-Si substrate, which causes a thin c-Si layer to peel off from the substrate. The processing temperature can be reduced to 350 °C and the substrate hardly degrades. The thickness of the metal layer, annealing temperature, laser, and mechanical notch parameters can control the thickness of the detached layer. In order to control the stripping process, water bath directional cooling[53] has been

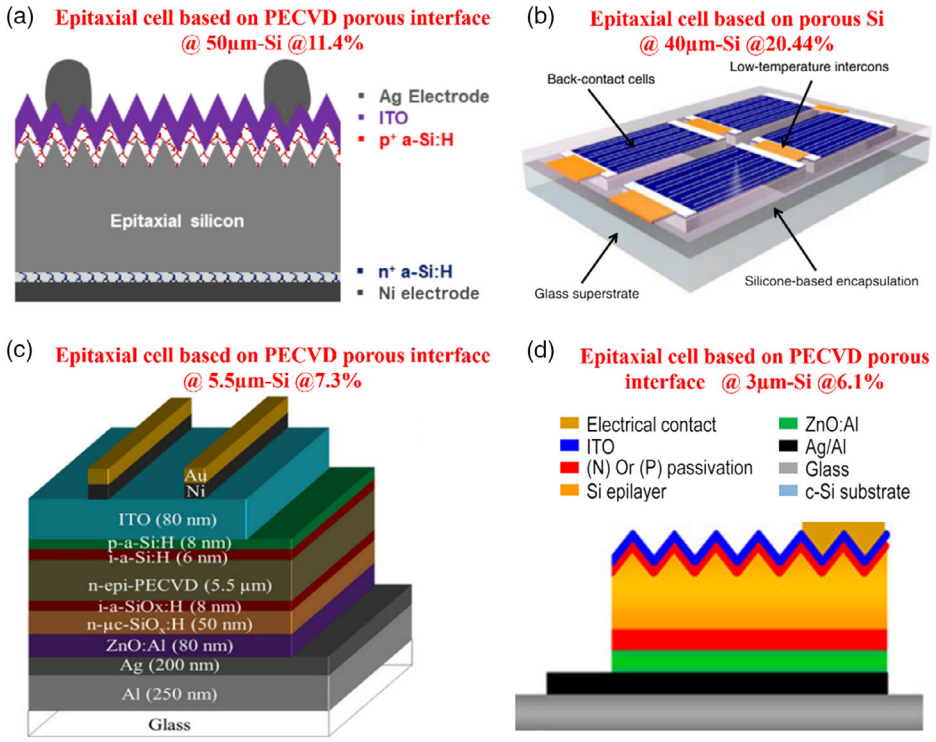

Figure 4. Solar cell applications of c-Si films (<50 µm) prepared by "bottom-up" approaches. a) High-quality Si thin films formed by epifrees process based on self-releasing seed layer, then anodic bonding and detachment from the parent wafer to prepare solar cells. Reproduced with permission.[40] Copyright 2021, Wiley-VCH. b) Deposition and lift-off of epitaxial Si based on porous Si substrates and fabrication of solar cells. Reproduced with permission.[41] Copyright 2012, Wiley-VCH. Ultrathin PECVD epitaxial Si solar cells on glass via low-temperature transfer process with c) planar surface and d) texturation of inverted pyramids. Reproduced with permission.[44] Copyright 2016, Wiley-VCH. Reproduced with permission.[45] Copyright 2016, American Chemical Society.

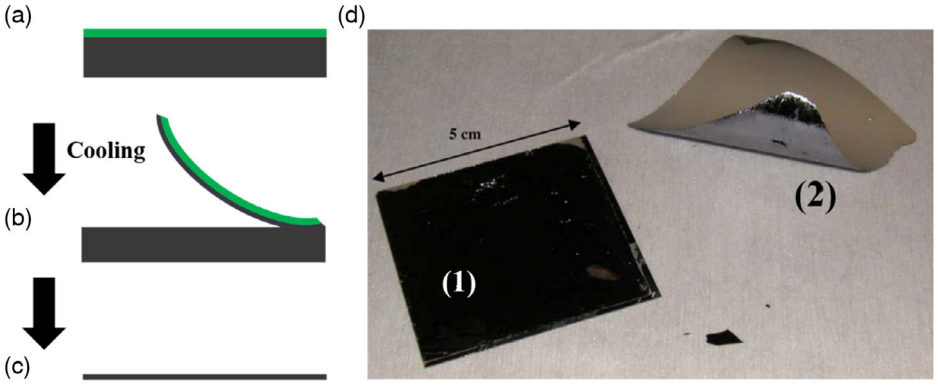

Figure 5. Schematic process flow of a screen printed metal paste used to produce a Si film. a) Deposition of metal. b) Cooling induced stress and stripping of the top layer. c) Cleaning by chemical etching and removal of residual stress. d) Photographs of the stripped structure. The parent substrate 1) can be reused and the top Si layer 2) remains attached to the stress-inducing layer. Reproduced with permission.[51] Copyright 2007, Springer Nature.

proposed to enhance thermal stress (see Figure 6b). The portion of the sample above the water surface is heated by a halogen lamp, and the heated material is then slowly immersed in water. Rapid cooling of the immersed part leads to the thermal stress and stripping (see Figure 6c). This method prevents spontaneous spalling of the top and sides of the sample, thus controlling the direction of cracking. However, the total thickness variation is considerable. As shown in Figure 6d, the average thickness of Si layer is about 60 µm, and the total thickness variation is about ±10 µm.

Nevertheless, the use of metal films requires a temperature of 350 °C to activate stress, resulting in the eventual degradation of the electrical properties of Si films.[65] Therefore, low-temperature treated epoxy was developed[52,55,56,66,67,69] and was found to be effective for Si separation in large areas.[69] The slim-cut foil was obtained by cooling the sample from 150 °C to room

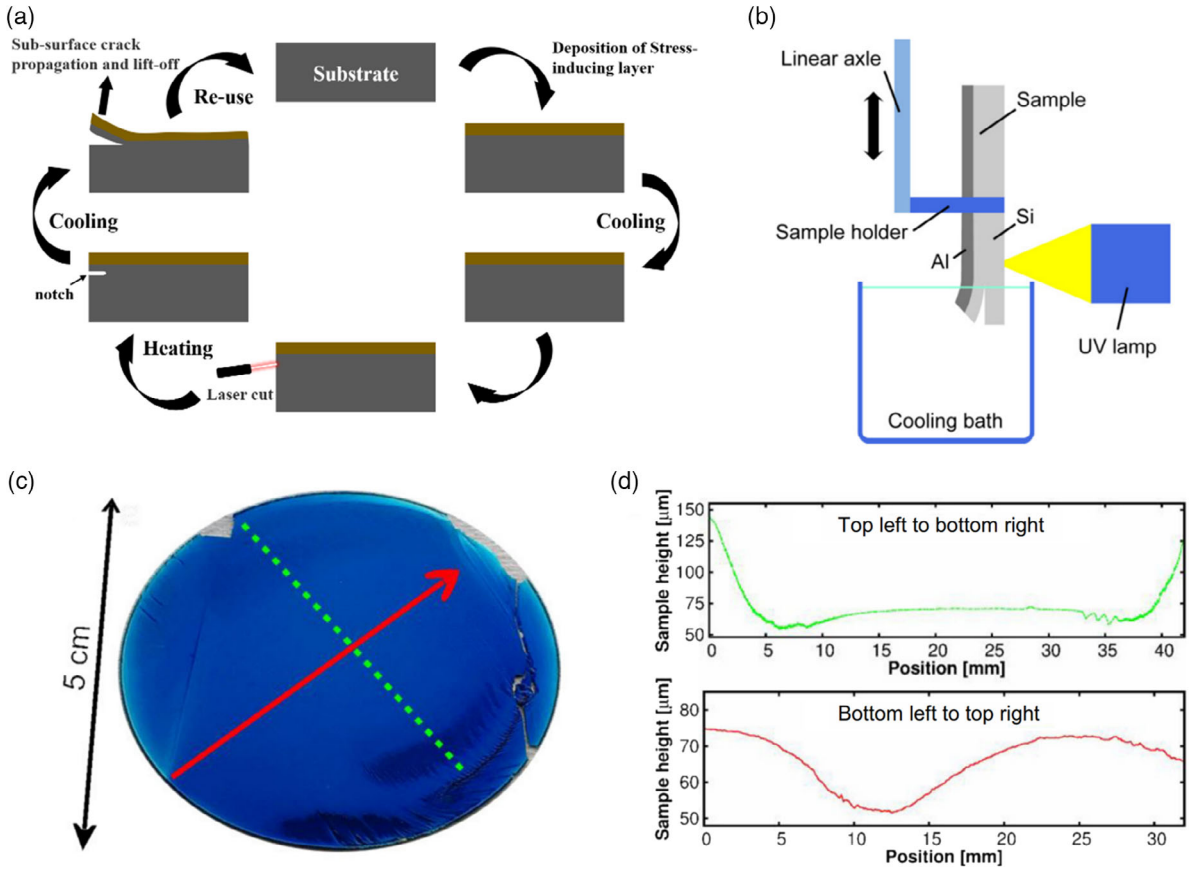

Figure 6. a) Metal-assisted stripping process diagram: the metal layer is deposited first. Then, it is cooled to room temperature and stripping is initiated by a laser cut with a laser. Finally, during the thermal cycle, the thin layers detach. b) Illustration of directional water bath cooling. c) Photos of the detached Si layer (2 in. in diameter) and d) profilometer height profiles measured along the marked lines. Reproduced with permission.[53] Copyright 2014, Elsevier.

temperature using a stress-induced epoxy layer. The thickness of the peeled sheet depends on the thickness of the polymer layer. The Si wafer had an initial thickness of 775 μm and was split into 300 and 475 μm thick wafers along (100) plane. The advantage of this method is to reduce metal contamination in Si as well as to reduce the process temperature to below 150 °C.[69] In addition, because the temperature is much lower than the brittle to ductile transition temperature (730 °C),[70] plastic deformation and diffusion of impurities into the foil are avoided. However, the cracks that initiate the spalling process are activated only after the rapid cooling step, which also causes thickness irregularities on the foil[52,56] (see **Figure 7**c[55]). The total thickness variation (TTV) of the foil is of the order of 50 μm, and it requires expensive grinding steps before further processing. On the contrary, the laser-assisted spalling process has the potential to reduce the TTV significantly (see Figure 7d).

Recently, stress-induced selective region-stripping methods have been proposed.[71] This method includes the deposition of a van der Waals (vdW) buffer on a substrate; the deposition of a thin film material on the vdW buffer layer, which is followed by the deposition of an adhesion layer, stressor layer, and handle layer. Several types of forces can be applied, for example, rolling and bending to active the crack boundary, which is initiated by the laser cutting or the mechanical scribing.

2.2. Smart-Cut

In the case of the smart-cut technique, ion implantation of hydrogen[57–59,72–76] or helium[59,74,75] is used. The molecular dynamics simulation shows that the hydrogen concentration region and the depth of the maximum hydrogen concentration are mainly determined by the implantation energy, while the implantation temperature and hydrogen ion dose have little effect on them. In addition, higher hydrogen ion dose and implantation temperature generally lead to higher defectivity.[77] Implanted atoms produce a weak layer in a region around the mean ion penetration depth. Due to the splitting of the weak layer, the transfer of the film can be accomplished, as shown in **Figure 8**a. It has been found that blistering (Figure 8d) and platelets or microcavities (insets in Figure 8b), which are usually induced by high-dose implantation (typically around 10^{17} cm^{-2}) around ambient temperature, can also be obtained by thermal activation at around few hundred degrees after implantation of a medium dose of about 10^{16} cm^{-2}.[73] However, to separate

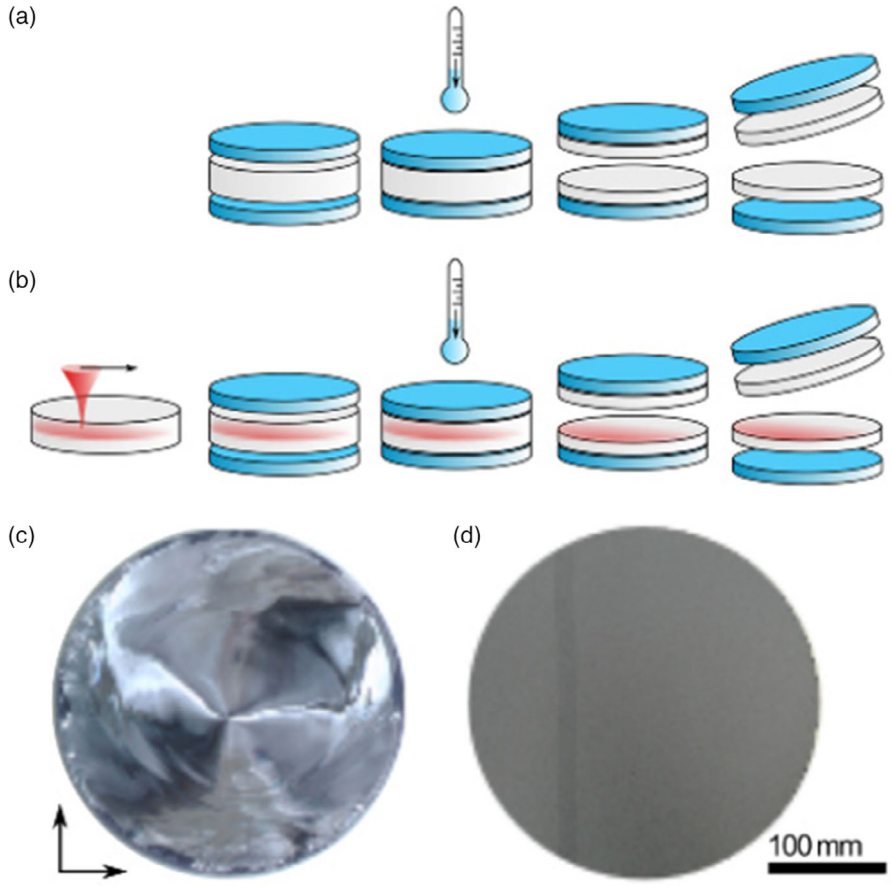

Figure 7. a) Schematic diagram of spalling based on a stress-induced polymer layer and c) image of spalling separated Si wafer (300 mm). b) Schematic diagram of laser-assisted spalling based on stress-induced polymer layer and d) image after spalling. Reproduced under the terms of the CC-BY license.[55] Copyright 2018, MDPI.

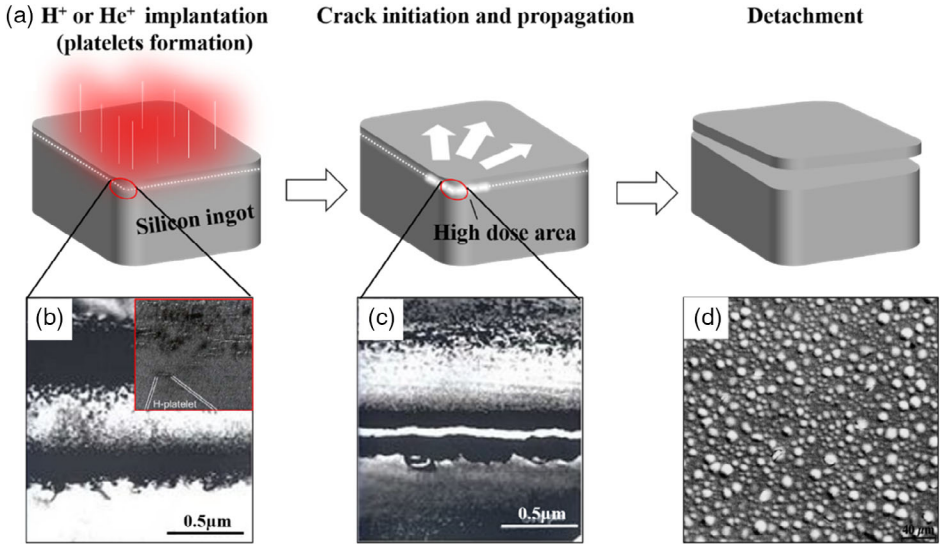

Figure 8. a) Process diagram of smart-cut technique. b) Cross-sectional image of H^+ (He^+) implanted area. Inset in (b) is the cross-section TEM image of H-platelets. Reproduced with permission.[157] Copyright 2000, AIP. c) Microcrack formation. Reproduced with permission.[59] Copyright 2003, Martin Luther University. d) Blistering on Si surface caused by hydrogen injection and annealing. Reproduced with permission.[73] Copyright 1999, Taylor & Francis.

the c-Si thin layer, a high-temperature annealing (>600 °C) and a high-dose hydrogen ion implantation (10^{17} cm^{-2}) are required, which leads to high costs associated to MeV implanter and implantation-induced damage to the c-Si material.[57] Currently, the Smart Cut technology combined with ion implantation is used to fabricate high-quality crystalline thin films on different substrates. Accordingly, the application of wafer bonding technology has also been greatly developped. Among them, Si-on-insulator (SOI) wafers, which have been widely used in various electronic products and photonic devices, are one of the most successful business cases. The top Si thin film of SOI wafers can be used as a functional layer for electrical and optical designs. Due to the advantage of being able to transfer high-quality crystalline thin films without considering lattice mismatches, wafer bonding in combination with ion implantation or laser irradiation is more flexible in the processing and heterogeneous integration of power chips.[78]

2.3. Epifree

The "Epifree" method involves the lift-off of a high-quality c-Si film generated by the recombination of cylindrical macropore arrays in Si during annealing.[38] As shown in **Figure 9**a, the objective of this method is to produce high-quality c-Si films during annealing by merging cylindrical macropore arrays in Si. Under a detachable, micron-scale, flawless thin layer, arrays of pores of the right size can join together at high temperatures to form a giant void region. Toshiba was the first to discover this phenomena known as "empty-space-in-Si" (ESS).[60] Three typical self-organizing sequence architectures for ESS creation are schematically described below. SEM was used to observe the formation of ESS in various shapes, as illustrated in Figure 9: c) sphere, e) pipe, and f) plate. The epitaxy-free method requires a combination of deep ultraviolet (DUV) photolithography, reactive ion etching (RIE), and annealing under H_2 at 1100 °C, which greatly increases the thermal budget.

Table 1 provides a compilation of three top-down methods used to produce c-Si thin films. The basic principles involved in each method as well as their advantages and disadvantages are summarized. Methods based on the "top-down" approach take advantage of metal-induced stress layer or from the formation of a weak interface. The SLIM-cut technology has the lowest processing temperature of them all, with the stress-induced epoxy resin layer requiring only 150 °C, but the c-Si film has numerous flaws and a rough surface. In the case of Epifree technology, the processing temperature is as high as 1100 °C with quite complex process, even though the crystalline quality of the c-Si film is very good. The smart-cut technique, which has been successfully commercialized by Soitec, is widely used due to its excellent process control and low wafer damage.

3. "Bottom-Up" Approaches

Epitaxial growth is a "bottom-up" semiconductor crystal film fabrication process, referring to the formation of a film having the same crystalline orientation as the substrate.[79–87] Epitaxial films can be ultrathin (nm) and of higher quality than the substrate, while film thickness and doping can be precisely controlled. According to the deposited materials, epitaxy can be divided into homo epitaxy[79] and hetero epitaxy,[88,89] as illustrated in **Figure 10**. Good epitaxial quality can be achieved if the epitaxial material has a very small lattice mismatch with respect to the substrate, such as Ge and GaAs, which have only 0.1% lattice mismatch. Stress (see Figure 10a), on the other hand, results

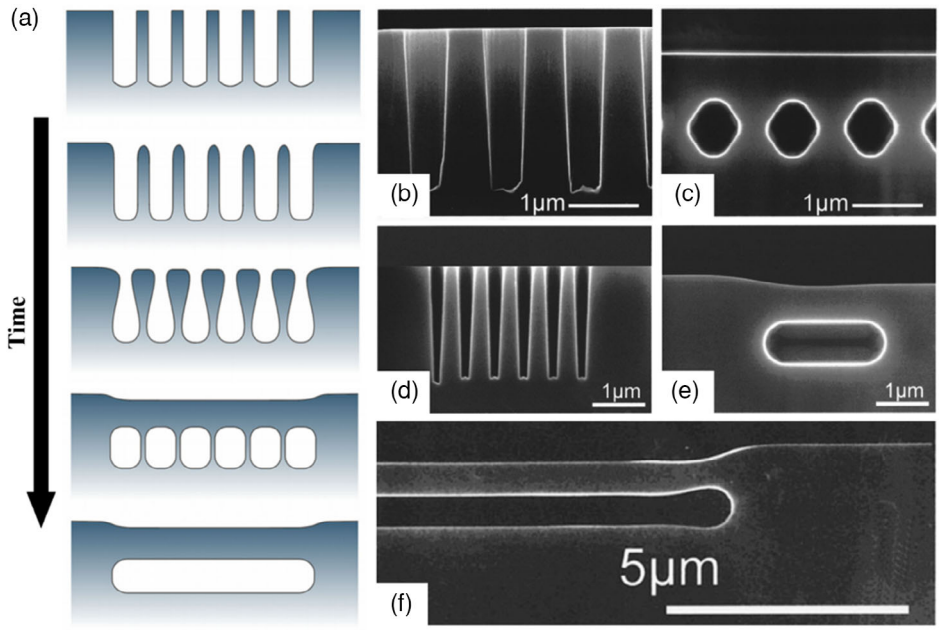

Figure 9. a) Pore reorganization and consolidation after high-temperature annealing using ESS technology. Reproduced with permission.[38] Copyright 2010, Wiley-VCH. b) Initial shape of the rectangular slot. c) Annealing under H_2 turns the groove into a hollow sphere. d) Six trenches in a row. e) Formation of tubular voids from six grooves via annealing. f) SEM images of ESS plates. Reproduced with permission.[60] Copyright 2000, AIP.

Table 1. Comparison of "top-down" methods for preparing c-Si thin films.

Methods	Principles	Process temperatures [°C]	Advantages	Disadvantages	References
SLIM-cut	Stress induced by a screen-printed metal paste (Al and Ag)	≈900	Simple process	High thermal budget, electrical degradation, and metal contamination	[49,51]
	Stress-induced by halogen lamp furnace heating (Al and Ag)	≈700	Simple process	High thermal budget, electrical degradation, metal contamination, and film cracking	[65]
	Stress-induced by an electrodeposited metal (Ni and Al)	≈350	Low thermal budget and simple process	Metal contamination and film cracking	[36,50,53,54,67]
	Stress-induced by an epoxy resin layer	≈150	Low thermal budget, small plastic deformations, and less impurity diffusion	Large TTV[a)], roughness and defects	[52,55,56,66,67,69,158]
Smart-Cut	Fragile interface produced by implantation of hydrogen or helium	≈600	Small TTV[a)] and controllable thickness	Implantation-induced damage and high costs	[57-59,72–76]
Epifree	Annealing induced reorganization of cylindrical macropore arrays in Si	≈1100	High-quality monocrystalline film	High thermal budget and complex process	[38,60]

[a)]TTV: Total thickness variation.

from the lattice mismatch and thermal expansion coefficient differences.[90] Three epitaxial growth mechanisms[90] can be distinguished according to the lattice parameters and the strength of the interaction between the adsorbed atoms and the surface (chemical potential),[91] as shown in Figure 10b. In Volmer–Weber (VW) growth mode, the adsorbed atoms interact more strongly with other adsorbed atoms than with these of the substrate, forming three-dimensional atomic clusters or islands. The Frank van der Merwe mechanism is a two-dimensional (2D) growth mode that forms a complete layer before the subsequent one grows. The adsorbed atoms preferentially attach to surface steps, forming a smooth and continuous layer of atoms. The third mechanism corresponds to Stranski–Krastanov growth mode, which is a combination of two-dimensional layer-by-layer growth up to a certain thickness, followed by three-dimensional (3D) island growth. The chemical and physical properties of substrates and films, such as surface energy and lattice parameters, influence the critical layer thickness for transition from layer-by-layer to island growth. Detailed information on the physical mechanisms and processes of Si epitaxial growth can be found in the following book.[92]

A variety of approaches have been used to study the epitaxial development of c-Si thin films on c-Si substrates. Because a clean Si substrate surface favors the growth of high-quality epitaxial Si, various wafer treatment methods have been developed to improve the epitaxial layer quality. For example, wafer surface cleaning methods such as HF-based wet cleaning,[93,94] plasma-based dry cleaning with SiF_4,[95,96] Ar,[97] H_2,[98,99] and combined wet and dry cleaning[100] have been studied. Many techniques have been developed to prepare c-Si thin films by epitaxial methods. Based on the melt-assisted epitaxial growth (see **Figure 11**a), wafer equivalent techniques such as string ribbon growth have been studied,[101–103] where the central part of the ribbon produces a large number of dislocations (see Figure 11b)[104] and twin boundaries.[101] In addition, there are methods based on liquid-phase epitaxy (LPE)[105,106] as shown in Figure 11c, such as the epi-lift technique, which can grow a Si epitaxial layer on a c-Si substrate with partial mask.[107] LPE growth rates range from a few microns/hour to tens of microns/hour and substrate temperatures range from 800 to 1000 °C. Although LPE is a relatively simple method of Si layer production, the presence of impurities and the breakage of the film[105] are significant disadvantages. Moreover, changes in doping levels during growth may also be caused by the cooling process.[106]

When considering the epitaxy from a gas precursor, high-temperature approaches (between 800 and 1200 °C), such as chemical vapor deposition (CVD)[108,109] (see **Figure 12**a), are commonly used because thermal activation helps incoming Si atoms to settle in crystalline sites. However, high-temperature methods face a number of challenges, including high thermal budget, dopant diffusion, thermal mismatch, and incompatibility with low-cost substrates. In fact, additional energy should be provided to maintain epitaxial growth and compensate for the low mobility of adsorbed species. More than two decades ago, Nagamine et al. and Tsai et al. demonstrated epitaxial growth using radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD) at a substrate temperature as low as 150 °C,[110,111] and Eaglesham et al.[112] used molecular beam epitaxy (MBE)[113,114] (see Figure 12d) to produce Si epitaxy even at room temperature, but this monocrystalline growth could only be sustained for a few nanometers before epitaxial breakdown occurs as shown in Figure 12e.[115] Teplin et al. used the hot wire CVD (HWCVD) technique to grow epitaxial Si films at intermediate temperatures.[116] However, when the substrate temperature was reduced below 550 °C,[117] epitaxial growth was observed to break down into polycrystalline and amorphous phases. In recent years, many kinds of epitaxial growth techniques have been developed. For example, ultrahigh vacuum low pressure chemical vapor deposition (UHVLPCVD) at high temperatures in the range of 700–960 °C,[118–120] reduced pressure chemical vapor deposition (RPCVD) at temperatures below 700 °C,[100] pulsed DC magnetron sputtering deposition[121] at substrate temperature

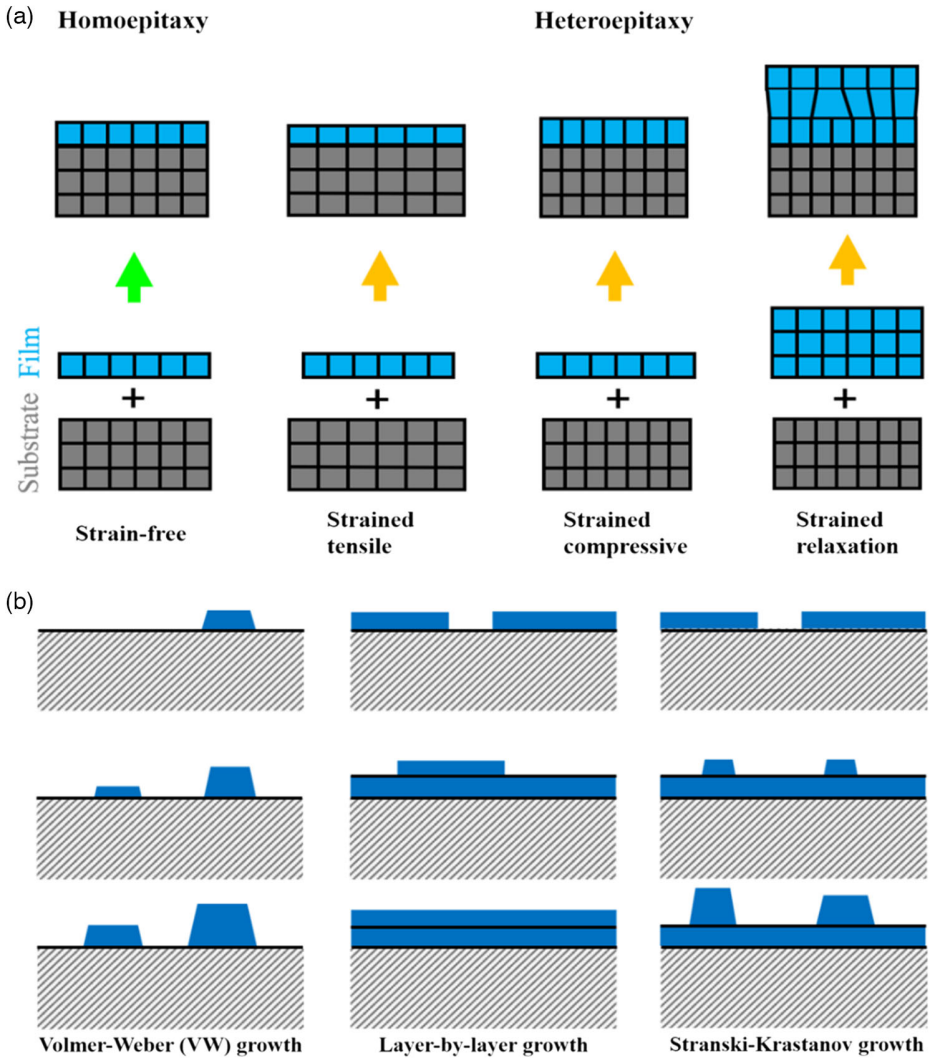

Figure 10. a) Homoepitaxy and heteroepitaxy growth schematic. Reproduced with permission.[90] Copyright 1996, IOP Science. b) Schematics of the cross section for different epitaxial growth modes from left to right: Volmer–Weber (island formation), Frank van der Merwe (layer-by-layer), and Stranski-Krastanov (layer-by-layer followed by island growth).

below 500 °C[122] (see Figure 12f,g), high-vacuum electron cyclotron resonance plasma deposition epitaxy with temperatures in the range of 450–525 °C,[123] ion beam epitaxy using temperatures of above 300 °C,[124–127] electron cyclotron resonance plasma CVD (ECR-CVD) using temperatures as low as 285 °C,[128] laser-enhanced chemical vapor deposition at temperatures as low as 250 °C[129] and plasma-enhanced chemical vapor deposition (PECVD) (see Figure 12b,c) using temperatures in the range of 700 °C and down to 150 °C.[44,79,95,109,130–132] It should be emphasized that PECVD is the only technique that has allowed to produce thick c-Si films at low temperatures.

Regardless of the application and manufacturing technology, in order to process the thin and fragile epitaxial c-Si films, they must be transferred to foreign carriers such as glass[79] or to flexible substrates such as metal foil,[133] plastic[134] and polyimide.[135] Therefore, porous and weak interfacial layers are essential for the transfer of epitaxial Si films.[80,136–150] The most widely used method to achieve this is to grow the epitaxial Si on a porous Si. The porous Si layer transfer technology provides the opportunity to obtain monocrystalline films on low-cost substrates. It is used for epi-Si lift-off by NexWafe, Crystal Solar[151] and Amberwave.[152] A c-Si wafer is used as a starting material. The porous Si layer produced via electrochemical etching can feature a double porosity structure, with a low-porosity layer on top and a high-porosity layer underneath as presented in **Figure 13**a. After annealing the porous structure at high temperature (see Figure 13b), the residual material in the low-porosity layer becomes monocrystalline, allowing the deposition of a high-quality epitaxial Si layer on top of it, while the high-porosity layer transforms into a void structure allowing to separate the epitaxial layer from the original Si substrate.[145] The parent substrate can be reused for the growth of another film. Theoretically, the number of reuses is in the hundreds.[147] However, this method requires the electrochemical etching of two layers of

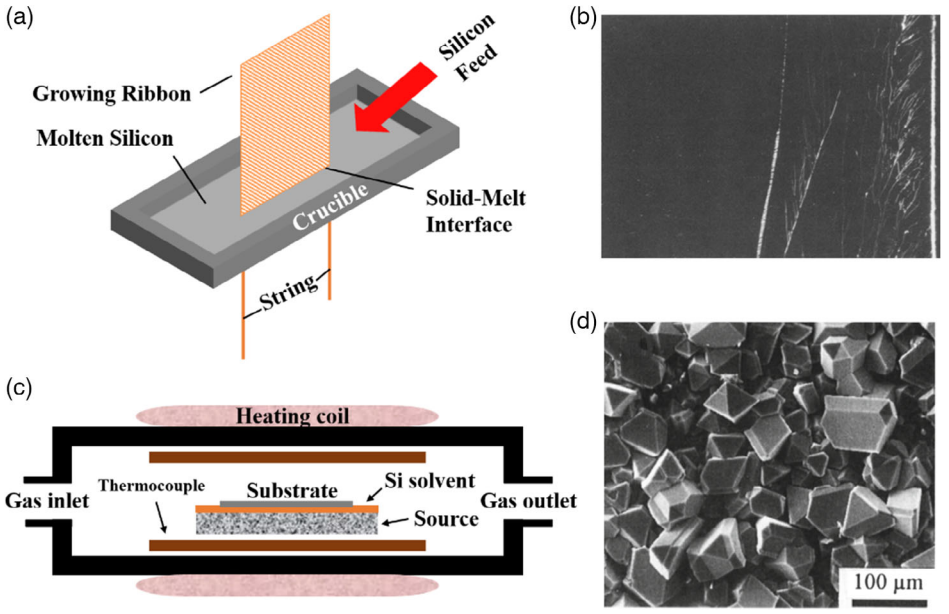

Figure 11. a) Si string ribbon growth process. b) Distribution of grain sizes for Si string ribbon growth. Reproduced with permission.[104] Copyright 1948, IOP Science. c) Schematics of the liquid-phase epitaxy system. d) SEM images of large faceted Si crystals grown from indium solution on the poly-Si seeding layer by LPE at 900 °C. Reproduced with permission.[105] Copyright 2011, Springer Nature.

porous Si with different porosity and sintering at temperatures higher than 1000 °C,[150] which greatly increases the complexity and thermal budget of the process.[41]

Despite all these approaches, a simpler bottom-up method that would avoid ion implantation, high-temperature annealing, or electrochemical etching should be of great interest. This can be obtained via an ultrathin porous epitaxial be produced by PECVD just before epitaxial growth.[95,132] This technology has been shown to be able to produce a hydrogen-rich Si interface layer[44,79] and Si-germanium alloy interface layer.[109] As a result, a brittle epi-PECVD/wafer interface is created, allowing for facile layer detachment. The quantity of hydrogen incorporated, which can be controlled via the PECVD process parameters, determines the degree of interface weakening.

Figure 14a depicts the process flow of the effective interface modification method based on in situ H-containing plasma treatment, which begins with a c-Si parent wafer and ends with an epi-PECVD Si layer bonded to glass. Anodic bonding is compatible with the transfer method of producing a fragile interface, based on hydrogen incorporation. This process only requires an annealing temperature of 350 °C to detach the epitaxial Si film from the parent c-Si wafer. The resulting 1.5 μm-thick epi-PECVD Si transferred onto a glass substrate is shown in Figure 14b, while Figure 14c shows the high-angle annular dark-field STEM (HAADF-STEM) image, where the defect-free atomic periodicity is clearly visible, and the interface with the glass is well defined, revealing that the crystalline quality of the transferred layer is unaffected by the transfer process. The ability to manufacture low-cost monocrystalline thin films on inexpensive substrates via epi-PECVD opens up the prospect of reusing the single-crystal parent substrate for multiple epitaxial growths.[153,154] However, the challenge of this procedure is that the hydrogen-rich interface should not only ensure a high crystal quality of the epitaxial Si film but also a perfect delamination of the epitaxial Si film. The interface engineering based on PECVD hydrogen injection has been applied to atmospheric pressure chemical vapor deposition with faster deposition rate and higher temperature, but a large number of defects was introduced into the epitaxial layer.[109]

Interestingly, PECVD-induced surface porosity can be further transformed into nanogaps with a post hydrogen annealing at 900 °C for 10 min,[40] as shown in **Figure 15**. The key point of this method is to use plasma-epitaxial Si as the self-releasing seed layer of a high-temperature epitaxial (HTE) film of high quality deposited at a higher rate than in the case of low-temperature epitaxy. The nanoscale voids in plasma epitaxial Si can be transformed into a self-organizing nanogap at the interface upon hydrogen annealing. The interfacial nanogap serves as an ideal self-release plane, and the surface of plasma epitaxial Si serves as an excellent seed layer for subsequent HTE growth. Notably, plasma-epi Si growth, nanogap formation, and HTE can be conducted in a single reactor. After HTE, the epitaxial wafer is separated from the substrate by applying a mechanical force, and the substrate can be reused. The separated epitaxial wafers (50 μm) can then be processed to make semiconductor devices.

Besides hydrogen ion implantation or PECVD with a hydrogen plasma, hydrogen atoms can also be introduced by post-deposition H_2 plasma treatment. For example, plasma hydrogenation of strained Si/SiGe/Si heterostructures[155] with a two-step approach including the growth of the strained intermediate SiGe film by MBE, together with post-deposition plasma hydrogenation. The drawback of this technique is its long hydrogenation time as it uses a hydrogen plasma at 250–300 °C for 1 h and then at 300–350 °C for two more hours, as well as being limited to thin layers.[155]

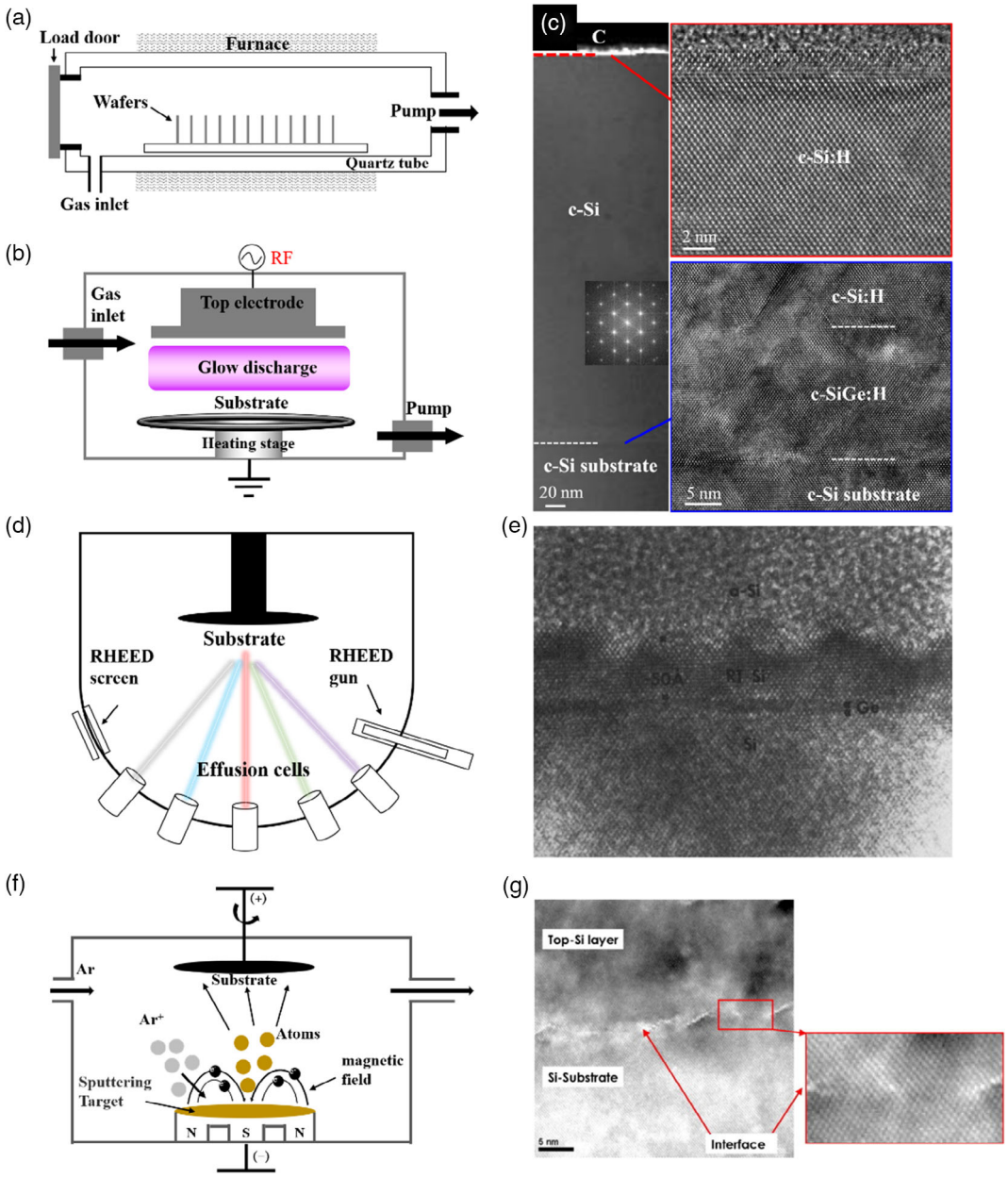

Figure 12. a) Vapor-phase Si deposition system (thermal chemical vapor deposition reactor). b) Schematic diagram of a PECVD reactor. c) Cross-sectional ADF-STEM image of epi-PECVD film. Inset in (c) shows the FFT of the image. HRTEM images (right) showing the surface of the c-Si layer and its interface with the c-Si substrate, respectively. Reproduced with permission.[109] Copyright 2021, Elsevier. d) Schematic of an MBE system. e) Cross-sectional TEM micrograph of a thin epitaxial Si layer which suffered a breakdown into an amorphous phase, obtained by MBE. Reproduced with permission.[115] Copyright 1983, Springer Nature. f) Schematic diagram of a magnetron sputtering reactor. g) TEM micrograph of a Si epitaxial layer grown using pulsed DC magnetron sputtering deposition. Reproduced with permission.[122] Copyright 2008, Elsevier.

A comparison of "bottom-up" approaches for preparing c-Si thin films is summarized in **Table 2**. Among them, melt-assisted epitaxial growth and LPE methods have high growth rates but require high temperatures and often lead to poor crystal quality of epitaxial films. The deposition temperature of the MBE method reaches around 1000 °C, which is unsuitable for thick film growth and mass production. Although the deposition temperature of the pulsed DC magnetron sputtering method is only about 500 °C, the ion bombardment will cause damage to the epitaxial film. In contrast, VPE becomes an appealing deposition technique, combining high throughput and low material consumption.[156] However, CVD is incompatible with low-cost substrates due to the high deposition temperature. PECVD, which is compatible with other semiconductor process equipment, is increasingly gaining popularity because it combines the advantages of

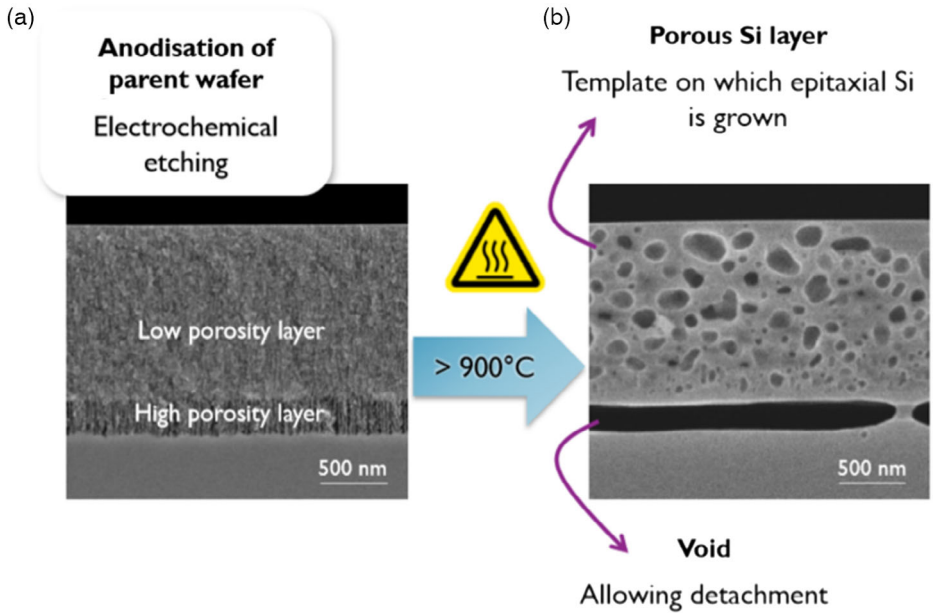

Figure 13. a) Two mesoporous Si layers of different porosities prepared by anodic etching. b) Porous Si layer and large void layer formed after annealing in H_2 at 1130 °C. Reproduced with permission.[80] Copyright 2016, Springer Nature.

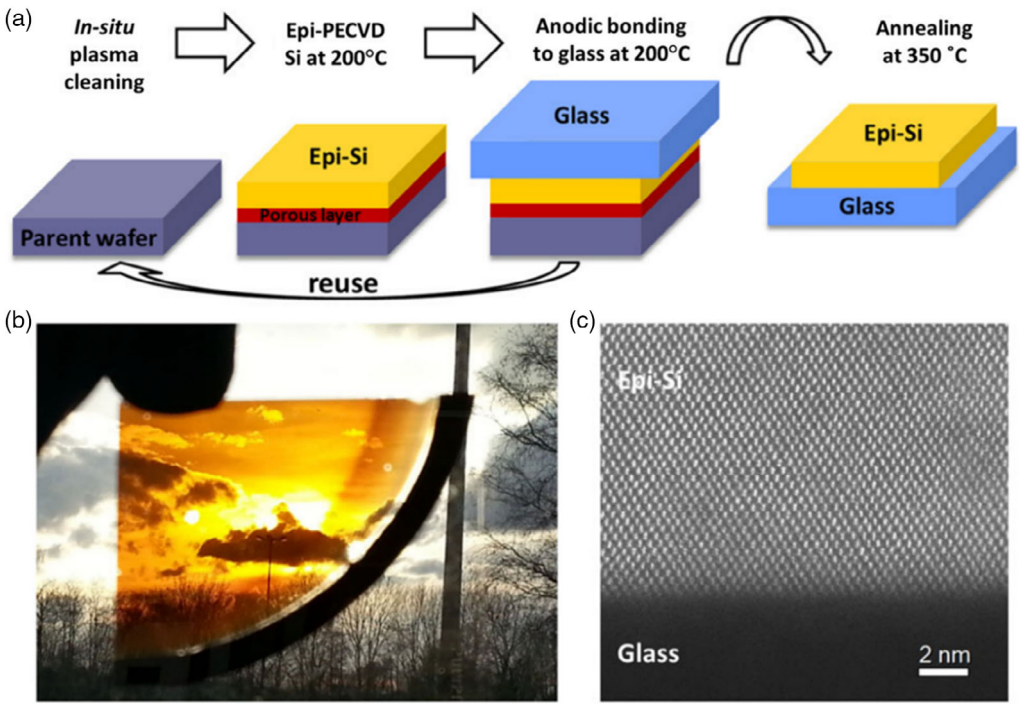

Figure 14. a) Schematic diagram of epi-PECVD growth and transfer of a c-Si layer. b) Sunlight penetrates through an epi-PECVD Si layer (one quarter of a 4 in. wafer) bonded to a glass. c) HAADF-STEM image of the epi-PECVD Si/glass-bonded interface. Reproduced with permission.[44] Copyright 2016, Wiley-VCH.

a low thermal budget, thick film growth, and excellent crystal quality. However, the low temperature limits the growth rate. For example, the growth rate is around 12 nm min^{-1} for PECVD, while it is only 0.14 nm min^{-1} in the case of ion beam epitaxy. Note that the high-temperature epitaxial growth rate such as APCVD is around 4 µm min^{-1} at 1050 °C (Table 2). Comparison of "bottom-up" approaches for preparing c-Si thin films.

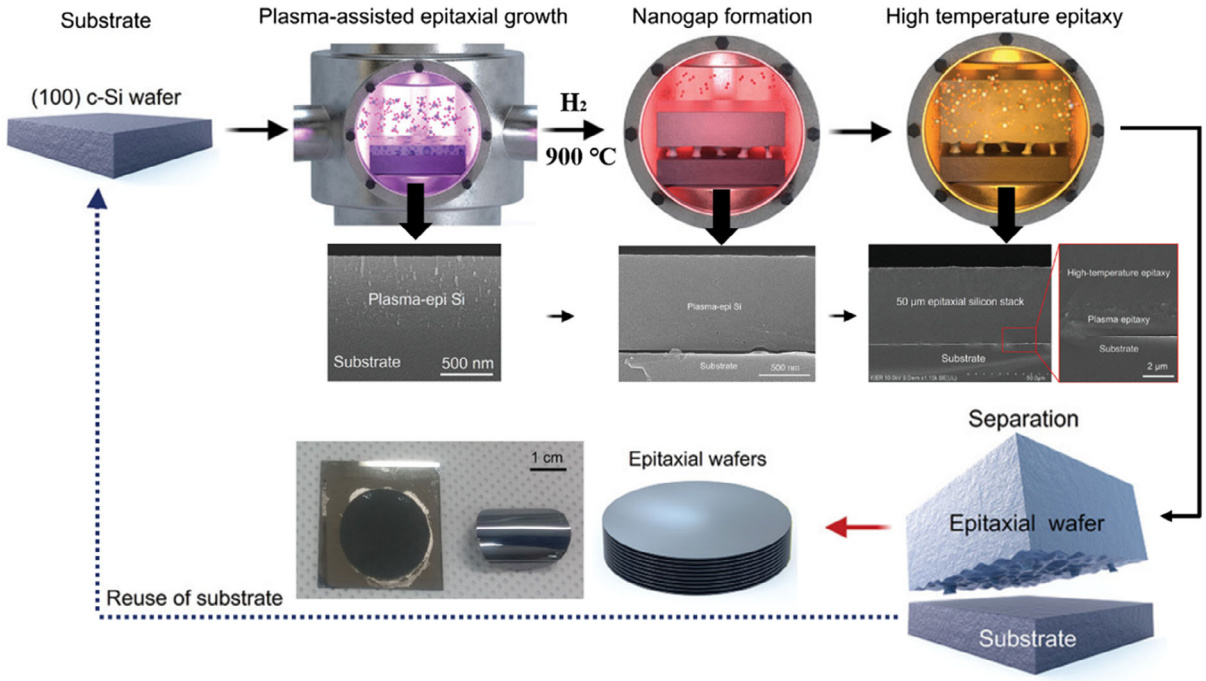

Figure 15. Schematic diagram of a fully bottom-up method for growing Si wafers using plasma-assisted epitaxial Si seed layers. Reproduced with permission.[40] Copyright 2021, Wiley-VCH.

Table 2. Comparison of "bottom-up" approaches for preparing c-Si thin films.

Categories	Process temperatures [°C]	Advantages	Disadvantages	References
Melt-assisted epitaxy	900–1400	Stable growth and easy for mass production	Large number of dislocations and twin boundaries	[101–103]
Liquid-phase epitaxy	800–1000	Simple process	Impurities contamination and discontinuous film	[105,106]
Molecular beam epitaxy	800–1200	Strict control of membrane composition, thickness and impurity concentration	Slow growth rate, not suitable for thick film growth, and mass production	[84,112–114]
Ion beam epitaxy	Above 300	Low thermal budget	Narrow epitaxial window, low growth rate, and ultrahigh vacuum	[124–127]
Pulsed DC magnetron sputtering deposition	Below 500	High deposition rate and large area	Ion bombardment damage and large roughness	[121,122]
Chemical vapor deposition	800–1200	Simple process	High thermal budget, incompatibility with low-cost substrates	[108,109]
Hot wire CVD	500–800	High deposition rates	High thermal budget	[116,117]
Low-pressure CVD	700–960	High deposition rates	High thermal budget	[118–120]
Reduced pressure CVD	Below 700	Uniform film and large area	Low deposition rate	[100]
Electron cyclotron resonance plasma CVD	250–550	High deposition rate and low thermal budget	Ion bombardment	[128]
Laser-enhanced CVD	150–700	High deposition rate and localized deposition	High technical difficulty	[159]
Plasma-enhanced CVD	150–200	Ultralow deposition temperature and convenient doping process	Low growth rate	[44,79,95,109,130–132]

4. Summary and Perspectives

In summary, there is a strong interest on thin c-Si films. Indeed, they open many possibilities, in particular in the field of photovoltaic solar energy conversion where absorber layers of a few tens of microns combined with efficient light trapping schemes would be sufficient to achieve conversion efficiencies close to these of current c-Si solar cells. As a matter of fact, the need for developing thin wafers is becoming a necessity. As on the one hand, the growth of the PV market is putting a strong

pressure on materials resources, and on the other hand, the development of thin film technologies (perovskite solar cells in particular) is a serious contender to bulk c-Si solar cells. As presented in this review paper, many approaches have been studied at the research level, involving both top-down and bottom-up fabrication methods. However, as summarized in Table 1, and 2, each method has some advantages and limitations, with some of them having scaled up to the industrial level, but none of them having made it into solar production. At this stage, it is difficult to determine if some of the presented methods will move to the solar cell production level. The choice of a production method will most likely be determined by the targeted device, which should take into account various factors such as the required material crystalline quality, the required thickness, the processing temperature, as well as the productivity.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

bottom-up, crystalline Si thin films, photovoltaics, top-down

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[1] E. A. Alharbi, A. Y. Alyamani, D. J. Kubicki, A. R. Uhl, B. J. Walder, A. Q. Alanazi, J. Luo, A. Burgos-Caminal, A. Albadri, H. Albrithen, M. H. Alotaibi, J.-E. Moser, S. M. Zakeeruddin, F. Giordano, L. Emsley, M. Grätzel, *Nat. Commun.* **2019**, *10*, 3008.
[2] J. Y. Kim, J.-W. Lee, H. S. Jung, H. Shin, N.-G. Park, *Chem. Rev.* **2020**, *120*, 7867.
[3] M. A. Green, A. Ho-Baillie, H. J. Snaith, *Nat. Photonics* **2014**, *8*, 506.
[4] M. I. Kabir, S. A. Shahahmadi, V. Lim, S. Zaidi, K. Sopian, N. Amin, *Int. J. Photoenergy* **2012**, *2012*, 460919.
[5] H. Kang, *IOP Conf. Ser. Earth Environ. Sci.* **2021**, *726*, 012001.
[6] Y. B. M. Yusoff, *Comprehensive Guide on Organic and Inorganic Solar Cells* (Eds: M. Akhtaruzzaman, V. Selvanathan), Academic Press, Cambridge, MA **2022**, pp. 85–113.
[7] M. Singh, J. Jiu, T. Sugahara, K. Suganuma, *ACS Appl. Mater. Interfaces* **2014**, *6*, 16297.
[8] Zhou, J.; Li, C., *E3S Web Conf.* **2021**, *267*, 02031.
[9] A. Aho, R. Isoaho, M. Raappana, T. Aho, E. Anttola, J. Lyytikäinen, A. Hietalahti, V. Polojärvi, A. Tukiainen, J. Reuna, L. Peltomaa, M. Guina, *Progr. Photovolt. Res. Appl.* **2021**, *29*, 869.
[10] P. Albert, A. Jaouad, G. Hamon, M. Volatier, C. E. Valdivia, Y. Deshayes, K. Hinzer, L. Béchou, V. Aimez, M. Darnon, *Progr. Photovolt. Res. Appl.* **2021**, *29*, 990.
[11] J. Chen, C. E. Packard, *Sol. Energy Mater. Sol. Cells* **2021**, *225*, 111018.
[12] V. Raj, T. Haggren, W. W. Wong, H. H. Tan, C. Jagadish, *J. Phys. D: Appl. Phys.* **2021**, *55*, 143002.
[13] Y. Shoji, R. Oshima, K. Makita, A. Ubukata, T. Sugaya, *Sol. Energy* **2021**, *224*, 142.
[14] A. Cavalli, N. Alkurd, S. Johnston, D. R. Diercks, D. M. Roberts, B. E. Ley, J. Simon, D. L. Young, C. E. Packard, A. J. Ptak, *IEEE J. Photovolt.* **2022**, *12*, 337.
[15] B. Conrad, B. H. Hamadani, *IEEE J. Photovolt.* **2022**, *12*, 798.
[16] H. Mizuno, K. Makita, H. Sai, T. Mochizuki, T. Matsui, H. Takato, R. Müller, D. Lackner, F. Dimroth, T. Sugaya, *ACS Appl. Mater. Interfaces* **2022**, *14*, 11322.
[17] P. Cheng, X. Zhan, *Chem. Soc. Rev.* **2016**, *45*, 2544.
[18] L. Meng, J. You, Y. Yang, *Nat. Commun.* **2018**, *9*, 5265.
[19] M. A. Green, Y. Hishikawa, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, A. W. Y. Ho-Baillie, *Progr. Photovolt. Res. Appl.* **2018**, *26*, 3.
[20] K. Yoshikawa, H. Kawasaki, W. Yoshida, T. Irie, K. Konishi, K. Nakano, T. Uto, D. Adachi, M. Kanematsu, H. Uzu, K. Yamamoto, *Nat. Energy* **2017**, *2*, 17032.
[21] J. W. Balde, in *Foldable Flex and Thinned Silicon Multichip Packaging Technology*, Springer, Berlin, Germany **2003**.
[22] R. Teixeira, K. De Munck, P. De Moor, K. Baert, B. Swinnen, C. Van Hoof, A. Kuttel, *ECS Trans.* **2007**, *9*, 113.
[23] G. Li, C. Xiao, S. Zhang, R. Sun, Y. Wu, *J. Mater. Process. Technol.* **2022**, *301*, 117453.
[24] J. Seok, C. P. Sukam, A. T. Kim, J. A. Tichy, T. S. Cale, *Wear* **2004**, *257*, 496.
[25] K. C. Cadien, L. Nolan, in *Handbook of Thin Film Deposition*, 4th ed. (Eds: L. K. Seshan, D. Schepis), William Andrew Publishing, Norwich, NY **2018**, pp. 317–357.
[26] N. Watanabe, T. Miyazaki, M. Aoyagi, K. Yoshikawa, in *14th Electronics Packaging Technology Conf. (EPTC)*, IEEE, Piscataway, NJ **2012**, pp. 355–359.
[27] I. J. Afa, G. López, P. R. O. Villasclaras, *J. Optoelectron. Eng.* **2015**, *3*, 7.
[28] I. Massiot, A. Cattoni, S. Collin, *Nat. Energy* **2020**, *5*, 959.
[29] Bhushan Sopori, S. Devayajanam , P. Basnyat, *AIMS Mater. Sci.* **2016**, *3*, 669.
[30] W. Chen, X. Liu, M. Li, C. Yin, L. Zhou, *Mater. Sci. Semicond. Process.* **2014**, *27*, 220.
[31] J. Walters, K. Sunder, O. Anspach, R. P. Brooker, H. Seigneur, in *IEEE 44th Photovoltaic Specialist Conf. (PVSC)*, IEEE, Piscataway, NJ **2016**, pp. 0724–0728.
[32] H.-D. Um, I. Hwang, D. Choi, K. Seo, *Acc. Mater. Res.* **2021**, *2*, 701.
[33] C. Yang, K. Moon, J.-W. Song, J. Kim, J.-H. Lee, J.-H. Lim, B. Yoo, *J. Electrochem. Soc.* **2018**, *165*, D243.
[34] H.-S. Lee, J. Suk, H. Kim, J. Kim, J. Song, D. S. Jeong, J.-K. Park, W. M. Kim, D.-K. Lee, K. J. Choi, B.-K. Ju, T. S. Lee, I. Kim, *Sci. Rep.* **2018**, *8*, 3504.
[35] H.-S. Lee, J. M. Choi, B. Jung, J. Kim, J. Song, D. S. Jeong, J.-K. Park, W. M. Kim, D.-K. Lee, T. S. Lee, W. S. Lee, K.-S. Lee, B.-K. Ju, I. Kim, *Sci. Rep.* **2019**, *9*, 19736.
[36] R. A. Rao, L. Mathew, S. Saha, S. Smith, D. Sarkar, R. Garcia, R. Stout, A. Gurmu, E. Onyegam, D. Ahn, D. Xu, D. Jawarani, J. Fossum, S. Banerjee, in *37th IEEE Photovoltaic Specialists Conf.*, IEEE, Piscataway, NJ **2011**, pp. 001504–001507.
[37] M. M. Hilali, S. Saha, E. Onyegam, R. Rao, L. Mathew, S. K. Banerjee, *Appl. Opt.* **2014**, *53*, 6140.
[38] V. Depauw, Y. Qiu, K. Van Nieuwenhuysen, I. Gordon, J. Poortmans, *Progr. Photovolt. Res. Appl.* **2011**, *19*, 844.
[39] V. Depauw, C. Trompoukis, I. Massiot, W. Chen, A. Dmitriev, P. R. Cabarrocas, I. Gordon, J. Poortmans, *Nano Futures* **2017**, *1*, 021001.
[40] J.-E. Hong, Y. Lee, S.-I. Mo, H.-S. Jeong, J.-H. An, H.-E. Song, J. Oh, J. Bang, J.-H. Oh, K.-H. Kim, *Adv. Mater.* **2021**, *33*, 2103708.

[41] F. Dross, K. Baert, T. Bearda, J. Deckers, V. Depauw, O. El Daif, I. Gordon, A. Gougam, J. Govaerts, S. Granata, R. Labie, X. Loozen, R. Martini, A. Masolin, B. O'Sullivan, Y. Qiu, J. Vaes, D. Van Gestel, J. Van Hoeymissen, A. Vanleenhove, K. Van Nieuwenhuysen, S. Venkatachalam, M. Meuris, J. Poortmans, *Progr. Photovolt. Res. Appl.* **2012**, *20*, 770.
[42] R. Brendel, R. Auer, H. Artmann, *Progr. Photovolt. Res. Appl.* **2001**, *9*, 217.
[43] S. Kommera, in *28th European Photovoltaic Solar Energy Conf. and Exhibition*, WIP, Munich, Germany **2013**.
[44] R. Cariou, W. Chen, I. Cosme-Bolanos, J.-L. Maurice, M. Foldyna, V. Depauw, G. Patriarche, A. Gaucher, A. Cattoni, I. Massiot, S. Collin, E. Cadel, P. Pareige, Roca, P. I Cabarrocas, *Progr. Photovolt. Res. Appl.* **2016**, *24*, 1075.
[45] A. Gaucher, A. Cattoni, C. Dupuis, W. Chen, R. Cariou, M. Foldyna, L. C Lalouat, E. Drouard, C. Seassal, P. Roca i Cabarrocas, S. Collin, *Nano Lett.* **2016**, *16*, 5358.
[46] Z. Liu, S. E. Sofia, H. S. Laine, M. Woodhouse, S. Wieghold, I. M. Peters, T. Buonassisi, *Energy Environ. Sci.* **2020**, *13*, 12.
[47] L. C. Andreani, A. Bozzola, P. Kowalczewski, M. Liscidini, L. Redorici, *Adv. Phys. X* **2019**, *4*, 1548305.
[48] S. Bhattacharya, I. Baydoun, M. Lin, S. John, *Phys. Rev. Appl.* **2019**, *11*, 014005.
[49] F. Dross, A. Milhe, J. Robbelein, I. Gordon, P.-O. Bouchard, G. Beaucarne, J. Poortmans, in *33rd IEEE Photovoltaic Specialists Conf.*, **2008**, IEEE, Piscataway, NJ, pp. 1–5.
[50] H.-S. Yang, J. Kim, S. Kim, N. S. A. Eom, S. Kang, C.-S. Han, S. H. Kim, D. Lim, J.-H. Lee, S. H. Park, J. W. Choi, C.-L. Lee, B. Yoo, J.-H. Lim, *Front. Chem.* **2018**, *6*, 600.
[51] F. Dross, J. Robbelein, B. Vandevelde, E. Van Kerschaver, I. Gordon, G. Beaucarne, J. Poortmans, *Appl. Phys. A* **2007**, *89*, 149.
[52] P. Bellanger, P.-O. Bouchard, M. Bernacki, J. Serra, *Mater. Res. Express* **2015**, *2*, 046203.
[53] R. Niepelt, J. Hensen, A. Knorr, V. Steckenreiter, S. Kajari-Schöder, R. Brendel, *Energy Proc.* **2014**, *55*, 570.
[54] R. A. Rao, L. Mathew, D. Sarkar, S. Smith, S. Saha, R. Garcia, R. Stout, A. Gurmu, M. Ainom, E. Onyegam, D. Xu, D. Jawarani, J. Fossum, S. Banerjee, U. Das, A. Upadhyaya, A. Rohatgi, Q. Wang, in *38th IEEE Photovoltaic Specialists Conf.*, IEEE, Piscataway, NJ **2012**, pp. 001837–001840.
[55] F. Kaule, M. Swoboda, C. Beyer, R. Rieske, A. Ajaj, W. D. Drescher, S. Schoenfelder, J. Richter, *MRS Commun.* **2018**, *8*, 127.
[56] S. Schoenfelder, F. Kaule, S. Schindler, K. Petter, R. Lantzsch, C. Beyer, J. Richter, in *33rd European Photovoltaic Solar Energy Conf. and Exhibition*, WIP, Munich, Germany **2017**.
[57] M. Bruel, B. Aspar, A.-J. Auberton-Hervé, *Jpn. J. Appl. Phys.* **1997**, *36*, 1636.
[58] B. Aspar, H. Moriceau, E. Jalaguier, C. Lagahe, A. Soubie, B. Biasse, A. M. Papon, A. Claverie, J. Grisolia, G. Benassayag, F. Letertre, O. Rayssac, T. Barge, C. Maleville, B. Ghyselen, *J. Electron. Mater.* **2001**, *30*, 834.
[59] V. H. I. Radu, in *Layer Transfer of Semiconductors and Complex Oxides by Helium and, or Hydrogen Implantation and Wafer Bonding*, Martin-Luther-University of Halle-Wittenberg, Halle, Germany **2003**.
[60] I. Mizushima, T. Sato, S. Taniguchi, Y. Tsunashima, *Appl. Phys. Lett.* **2000**, *77*, 3290.
[61] B. Andreas, R. Stefan, in *NexWafe GmbH – Fraunhofer ISE Starts a New Spin-Off Company – Kerfless Wafer Technology to Bring Cost of Photovoltaics Down and Reduce Waste.*, *Vol. 15*, Fraunhofer Institute for Solar Energy Systems ISE, Freiburg **2015**.
[62] M. Tanielian, S. Blackstone, R. Lajos, *J. Electrochem. Soc.* **1985**, *132*, 507.
[63] S. Bedell, K. Fogel, P. Lauro, D. Shahrjerdi, J. Ott, D. Sadana, *J. Phys. D: Appl. Phys.* **2013**, *46*, 152002.
[64] A. Masolin, in *Fabrication and Characterization of Ultra-Thin Silicon Crystalline Wafers for Photovoltaic Applications Using a Stress-Induced Lift-Off Method*, Katholieke Universiteit Leuven, Leuven, Belgium **2012**.
[65] P. Bellanger, A. Masolin, D. Pera, L. Costa, J. Poortmans, R. Mertens, J.M. Serra, in *27th European Photovoltaic Solar Energy Conf. and Exhibition*, WIP, Munich, Germany **2012**, pp 1042–1044.
[66] P. Bellanger, M. C. Brito, D. M. Pera, I. Costa, G. Gaspar, R. Martini, M. Debucquoy, J. M. Serra, *IEEE J. Photovolt.* **2014**, *4*, 1228.
[67] Serra, J. M.; Bellanger, P.; Lobato, K.; Martini, R.; Debucquoy, M.; Poortmans, J. in *IEEE 39th Photovoltaic Specialists Conf. (PVSC)*, IEEE, New York City, United States **2013**, pp 0177–0180.
[68] Y. Lee, B. Gupta, H. H. Tan, C. Jagadish, J. Oh, S. Karuturi, *iScience* **2021**, *24*, 102921.
[69] R. Martini, M. Gonzalez, F. Dross, A. Masolin, J. Vaes, D. Frederickx, J. Poortmans, *Energy Proc.* **2012**, *27*, 567.
[70] J. Samuels, S. G. Roberts, P. B. Hirsch, *Mater. Sci. Eng. A* **1988**, *105–106*, 39.
[71] M. R. Snure, E. W. Blanton, J. L. Brown, A. M. Hilton, US20220216109A1, **2022**.
[72] Q. Y. Tong, K. Gutjahr, S. Hopfe, U. Gösele, B. Lee, *Appl. Phys. Lett.* **1997**, *70*, 1390.
[73] M. Bruel, *Mater. Res. Innov.* **1999**, *3*, 9.
[74] C. Lagahe, N. Sousbie, S. Sartori, H. Moriceau, A. Soubie, B. Aspar, P. Nguyen, B. Blondeau, *Proc. Electrochem. Soc.* **2003**, *19*, 346.
[75] R. E. Hurley, S. Suder, H.S Gamble, *Vacuum* **2005**, *78*, 167.
[76] C. Himcinschi, I. Radu, F. Muster, R. Singh, M. Reiche, M. Petzold, U. Gösele, S. H. Christiansen, *Solid-State Electron.* **2007**, *51*, 226.
[77] B. Wang, B. Gu, H. Zhang, X. Feng, *Acta Mech. Solida Sinica* **2016**, *29*, 111.
[78] Z. Ren, J. Xu, X. Le, C. Lee, *Micromachines* **2021**, *12*, 946.
[79] J. An, Z. Zheng, R. Gong, T. B. T. Nguyen, H. Jun, M. Chrostowki, J.-L. Maurice, W. Chen, P. Roca i Cabarrocas, *Appl. Surf. Sci.* **2020**, *518*, 146057.
[80] T. Bearda, I. Gordon, H. S. Radhakrishnan, V. Depauw, K. Van Nieuwenhuysen, M. Xu, L. Tous, M. Filipic, S. K. Jonnak, A. Hajijafarassar, X. Liu, M. Debucquoy, Y. Abdulraheem, J. Szlufcik, J. Poortmans, *MRS Adv.* **2016**, *1*, 3235.
[81] Kawano, M.; Yamada, S.; Tanikawa, K.; Sawano, K.; Miyao, M.; Hamaya, K., *Appl. Phys. Lett.* **2013**, *102* , 121908.
[82] Y. B. Cheng, C. K. Chia, Y. Chai, D. Z. Chi, *Thin Solid Films* **2012**, *522*, 340.
[83] J. Yang, P. Jurczak, F. Cui, K. Li, M. Tang, L. Billiald, R. Beanland, A. M. Sanchez, H. Liu, *J. Cryst. Growth* **2019**, *514*, 109.
[84] G. R. Booker, B. A. Joyce, *Philos. Mag.***1966**, *14*, 301.
[85] D. Buca, S. F. Feste, B. Holländer, S. Mantl, R. Loo, M. Caymax, R. Carius, H. Schaefer, *Solid-State Electron.* **2006**, *50*, 32.
[86] Y. Nakamura, T. Miwa, M. Ichikawa, *Nanotechnology* **2011**, *22*, 265301.
[87] Y. Nakamura, A. Murayama, M. Ichikawa, *Cryst. Growth Des.* **2011**, *11*, 3301.
[88] Y. Yasuda, *Jpn. J. Appl. Phys.* **1971**, *10*, 45.
[89] Y. Du, B. Xu, G. Wang, S. Gu, B. Li, Z. Kong, J. Yu, G. Bai, J. Li, W. Wang, H. H. Radamson, *J. Mater. Sci. Mater. Electron.* **2021**, *32*, 6425.
[90] M. Opel, *J. Phys. D: Appl. Phys.* **2011**, *45*, 033001.
[91] K. Oura, V. G. Lifshits, A. Saranin, A. V. Zotov, M. Katayama, in *Advanced Texts in Physics*, Springer, Berlin **2003**.
[92] R. K. W.D. Crippa, D. L. Rode, E. Weber, M. Masi, in *Silicon Epitaxy*, Academic Press, Cambridge, MA **2001**.

[93] K. Madiomanana, M. Bahri, J. B. Rodriguez, L. Largeau, L. Cerutti, O. Mauguin, A. Castellano, G. Patriarche, E. Tournié, *J. Cryst. Growth* **2015**, *413*, 17.
[94] A. Ishizaka, Y. Shiraki, *J. Electrochem. Soc.* **1986**, *133*, 666.
[95] M. Moreno, G. Patriarche, *J. Mater. Res.* **2013**, *28*, 1626.
[96] R. Cariou, W. Chen, J. L. Maurice, J. Yu, G. Patriarche, O. Mauguin, L. Largeau, J. Decobert, *Sci. Rep.* **2016**, *6*, 25674.
[97] T. Ohmi, T. Ichikawa, T. Shibata, K. Matsudo, H. Iwabuchi, *Appl. Phys. Lett.* **1988**, *53*, 45.
[98] H. W. Kim, *J. Mater. Sci.* **2004**, *39*, 361.
[99] H. Kim, in *Wafer Surface Cleaning for Silicon Homoepitaxy with and Without ECR Hydrogen Plasma Exposure*, Massachusetts Institute of Technology, Cambridge, MA **1994**.
[100] J. Jung, B. Son, B. Kam, Y. S. Joh, W. Jeong, S. Cho, W. J. Lee, S. Park, *Materials* **2021**, *14*, 3733.
[101] R. L. Wallace, J. I. Hanoka, A. Rohatgi, G. Crotty, *Sol. Energy Mater. Sol. Cells* **1997**, *48*, 179.
[102] E. M. Sachs, D. Ely, J. Serdy, *J. Cryst. Growth* **1987**, *82*, 117.
[103] R. Janoch, R. Wallace, J. I. Hanoka, in *Conf. Record of the Twenty Sixth IEEE Photovoltaic Specialists Conf.*, IEEE, Piscataway, NJ **1997**, pp. 95–98.
[104] T. F. Ciszek, J. L. Hurd, M. Schietzelt, *J. Electrochem. Soc.* **1982**, *129*, 2838.
[105] J. Kühnle, R. B. Bergmann, J. Krinke, J. H. Werner, *MRS Proc.* **1996**, *426*, 111.
[106] A. Ur Rehman, S. Lee, S. Lee, *Electron. Mater. Lett.* **2015**, *11*, 295.
[107] K. J. Weber, A. W. Blakers, K. R. Catchpole, *Appl. Phys. A* **1999**, *69*, 195.
[108] S. M. Gates, C. M. Greenlief, S. K. Kulkarni, H. H. Sawin, *J. Vac. Sci. Technol., A* **1990**, *8*, 2965.
[109] J. An, J.-L. Maurice, V. Depauw, P. Roca i Cabarrocas, W. Chen, *Appl. Surf. Sci.* **2021**, *546*, 149056.
[110] Nagamine, K.; Yamada, A.; Konagai, M.; Takahashi, K., *Jpn. J. Appl. Phys.* **1987**, *26*, L951.
[111] C. C. Tsai, G. B. Anderson, R. Thompson, *J. Non-Cryst. Solids* **1991**, *137–138*, 673.
[112] D. J. Eaglesham, H. Gossmann, M. Cerullo, *Phys. Rev. Lett.* **1990**, *65*, 1227.
[113] S. I. Stenin, B. Z. Kanter, A. I. Nikiforov, in *Growth of Crystals* (Eds: E. I. Givargizov, S. A. Grinberg, D. W. Wester), Springer US, Boston, MA **1992**, pp. 69–76.
[114] Y. Ota, *Thin Solid Films* **1983**, *106*, 1.
[115] H.-J. Gossmann, *J. Miner. Metal Mater. Soc.* **1991**, *43*, 28.
[116] C. W. Teplin, K. Alberi, M. Shub, C. Beall, I. T. Martin, M. J. Romero, D. L. Young, R. C. Reedy, P. Stradins, H. M. Branz, *Appl. Phys. Lett.* **2010**, *96*, 201901.
[117] S. Lee, K. Ahn, B. T. Ahn, *J. Electrochem. Soc.* **2007**, *154*, H778.
[118] B. Meyerson, E. Ganin, D. Smith, T. Nguyen, *J. Electrochem. Soc.* **1986**, *133*, 1232.
[119] B. S. Meyerson, *Appl. Phys. Lett.* **1986**, *48*, 797.
[120] W. Zhang, N. Lloyd, K. Osman, J. Bonar, J. Hamel, D. Bagnall, *Microelectron. Eng.* **2004**, *73*, 514.
[121] L. Bailey, G. Proudfoot, B. Mackenzie, N. Andersen, A. Karlsson, A. Ulyashin, *Phys. Status Solidi A* **2014**, *212*, 42.
[122] P. Plantin, F. Challali, O. Carriot, F. Lainat, M. Ancilotti, G. Gadot, P. Brault, *Microelectron. Eng.* **2008**, *85*, 636.
[123] S. J. DeBoer, V. L. Dalal, G. Chumanov, R. Bartels, *Appl. Phys. Lett.* **1995**, *66*, 2528.
[124] H. Khan, H. Frey, *Surf. Coat. Technol.* **1999**, *116*, 472.
[125] P. C. Zalm, L. J. Beckers, *Appl. Phys. Lett.* **1982**, *41*, 167.
[126] R. A. Zuhr, B. R. Appleton, N. Herbots, B. C. Larson, T. S. Noggle, S. J. Pennycook, *J. Vac. Sci. Technol. A* **1987**, *5*, 2135.
[127] J. W. Rabalais, B. Al, K. J. Boyd, D. Marton, J. Kulik, Z. Zhang, W. K. Chu, in *Proc. of 11th Int. Conf. on Ion Implantation Technology*, **1996**, pp 682–685.
[128] K. Sasaki, H. Tomoda, T. Takada, *Vacuum* **1998**, *51*, 537.
[129] K. B. Sanjay, *Proc.SPIE* **1993**.
[130] R. Shimokawa, M. Yamanaka, I. Sakata, *Jpn. J. Appl. Phys.* **2007**, *46*, 7612.
[131] T. Kitagawa, M. Kondo, A. Matsuda, *Appl. Surf. Sci.* **2000**, *159*, 30.
[132] M. Moreno, P. Rocai Cabarrocas, *EPJ Photovolt.* **2010**, *1*, 10301.
[133] Y. Gao, M. Asadirad, Y. Yao, P. Dutta, E. Galstyan, S. Shervin, K.-H. Lee, S. Pouladi, S. Sun, Y. Li, M. Rathi, J.-H. Ryou, V. Selvamanickam, *ACS Appl. Mater. Interfaces* **2016**, *8*, 29565.
[134] J.-H. Ahn, H.-S. Kim, J. Lee, Z. Zhu, E. Menard, R. G. Nuzzo, J. A. Rogers, *IEEE Electron Dev. Lett* **2006**, *27*, 460.
[135] P.-Y. Hsieh, C.-Y. Lee, N.-H. Tai, *J. Mater. Chem. C* **2015**, *3*, 7513.
[136] H.S. Radhakrishnan, T. Bearda, M. Filipic, K. Van Nieuwenhuysen, V. Depauw, I. Gordon, M. Debucquoy, J. Szlufcik, J. Poortmans, in *33rd European Photovoltaic Solar Energy Conf. and Exhibition* **2017**, pp. 740–744.
[137] A. Hajijafarassar, K. Van Nieuwenhuysen, I. Sharlandzhiev, V. Depauw, H. Sivaramakrishnan Radhakrishnan, T. Bearda, I. Gordon, J. Szlufcik, Y. Abdulraheem, J. Poortmans, L. Magagnin, in *32nd European Photovoltaic Solar Energy Conf. and Exhibition* **2016**, pp. 313–316.
[138] J. Govaerts, C. Trompoukis, H.S. Radhakrishnan, L. Tous, S. Granata, E. Carnemolla, R. Martini, A. Marchegiani, M. Karim, I. Sharlandzhiev, T. Bearda, V. Depauw, K. Van Nieuwenhuysen, I. Gordon, J. Szlufcik, J. Poortmans, *Energy Proc.* **2015**, *77*, 871.
[139] R. B. Bergmann, T. J. Rinke, R. M. Hausner, M. Grauvogl, M. Vetter, J. H. Werner, *Int. J. Photoenergy* **1999**, *1*, 839258.
[140] K. V. Nieuwenhuysen, I. Gordon, T. Bearda, C. Boulord, M. Debucquoy, V. Depauw, F. Dross, J. Govaerts, S. Granata, R. Labie, X. Loozen, R. Martini, B. O. Sullivan, H. S. Radhakrishnan, K. Baert, J. Poortmans, in *38th IEEE Photovoltaic Specialists Conf.*, IEEE, Piscataway, NJ **2012**, pp. 1833–1836.
[141] C. Solanki, R. Bilyalov, J. Poortmans, J. Nijs, R. Mertens, *Sol. Energy Mater. Sol. Cells* **2004**, *83*, 101.
[142] H. S. Radhakrishnan, R. Martini, V. Depauw, K. V. Nieuwenhuysen, M. Debucquoy, J. Govaerts, I. Gordon, R. Mertens, J. Poortmans, *IEEE J. Photovolt.* **2014**, *4*, 70.
[143] R. Brendel, J. H. Petermann, D. Zielke, H. Schulte-Huxel, M. Kessler, S. Gatz, S. Eidelloth, R. Bock, E. G. Rojas, J. Schmidt, T. Dullweber, *IEEE J. Photovolt.* **2011**, *1*, 9.
[144] N. Milenkovic, M. Driesen, B. Steinhauser, J. Benick, S. Lindekugel, M. Hermle, S. Janz, S. Reber, in *IEEE 43rd Photovoltaic Specialists Conf. (PVSC)*, IEEE, Piscataway, NJ **2016**, pp. 0058–0061.
[145] R. B. Bergmann, *Appl. Phys. A: Mater. Sci. Process.* **1999**, *69*, 187.
[146] C. Sanchez-Perez, M. Hernandez-Castro, I. Garcia, *Appl. Surf. Sci.* **2022**, *577*, 151907.
[147] I. Sharlandzhiev, *Manifold Reuse of Silicon Substrate in the Layer Transfer Process with Porous Silicon*, Instituto Superior Tecnico, Lisboa, Portungal **2015**.
[148] N. Milenkovic, M. Driesen, E. Gust, S. Janz, S. Reber, *Energy Proc.* **2014**, *55*, 552.
[149] S. Zhang, Z. Lu, J. Sheng, P. Gao, X. Yang, S. Wu, J. Ye, M. Kambara, *Appl. Phys. Express* **2016**, *9*, 055506.
[150] C. C. Chiang, B. T. H. Lee, *Sci. Rep.* **2019**, *9*, 12631.
[151] E. Kobayashi, Y. Watabe, R. Hao, T. S. Ravi, *Progr. Photovolt. Res. Appl.* **2016**, *24*, 1295.

[152] L. Wang, A. Lochtefeld, J. Han, A. P. Gerger, M. Carroll, J. Ji, A. Lennon, H. Li, R. Opila, A. Barnett, *IEEE J. Photovolt.* **2014**, *4*, 1397.
[153] C. H. Lee, D. R. Kim, X. Zheng, *ACS Nano* **2014**, *8*, 8746.
[154] Q. Lin, H. Huang, Y. Jing, H. Fu, P. Chang, D. Li, Y. Yao, Z. Fan, *J. Mater. Chem. C* **2014**, *2*, 1233.
[155] L. Shao, Y. Lin, J. K. Lee, Q. X. Jia, Y. Wang, M. Nastasi, P. E. Thompson, N. D. Theodore, P. K. Chu, T. L. Alford, J. W. Mayer, P. Chen, S. S. Lau, *Appl. Phys. Lett.* **2005**, *87*, 091902.
[156] J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, R. Brendel, *Progr. Photovolt. Res. Appl.* **2012**, *20*, 1.
[157] J. Grisolia, G. Benassayag, A. Claverie, B. Aspar, C. Lagahe, L. Larbi, *Appl. Phys. Lett.* **2000**, *76*, 852.
[158] J. Serra, P. Bellanger, P. O. Bouchard, M. Bernacki, *Phys. Status Solidi C* **2014**, *11*, 1644.
[159] S. Banerjee, in *Laser-Enhanced CVD for Low-Temperature Si Epitaxy*, Vol. *1804*, SPIE, Bellingham, WA **1993**.

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