

Revolutionizing brain-computer interfaces: Compact and high-speed wireless neural signal acquisition

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ABSTRACT

A brain–computer interface (BCI) facilitates the connection between the human brain and external devices by decoding neurophysiological signals, thereby enabling seamless interaction between humans and machines. However, existing neural signal acquisition systems often suffer from limited channel counts, low sampling rates, and challenges in miniaturization and wireless bandwidth, which restrict their ability to support large-scale and real-time neural recordings. Given the rapid advancements in BCI technologies and the increasing demand for high-resolution neural data, there is an imperative need for BCI systems that are high-throughput, high-speed, and miniaturized. This paper presents a wireless neural signal acquisition system based on FPGA technology, supporting 1024 channels at 32 kSPS and employing a stacked architecture for compact, low-power wireless transmission. Following the creation of the functional prototype, laboratory electrical performance tests were conducted. The system exhibited a noise voltage of $8.56 \mu\text{V}_{\text{rms}}$, which is in close proximity to the $6 \mu\text{V}_{\text{rms}}$ specified by the chip. In addition, the system accurately captured weak sine wave inputs in both time and frequency domains, confirming its ability to record weak bioelectrical signals. Subsequent animal experiments involving mice implanted with EEG electrodes demonstrated that the system could reliably acquire brain neural signals in real time. The maximum and minimum values of signal-to-noise ratios among the channels were measured at 28.66 and 30.56 dB, thereby providing additional validation for the system's signal quality and consistency.

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I. INTRODUCTION

Brain–computer interface (BCI) technology establishes a direct communication pathway between the brain and external devices by analyzing neurophysiological signals such as electroencephalography (EEG) and electrocorticography (ECOG) in real time. As a groundbreaking method of human–computer interaction, BCI has demonstrated significant application value in neurorehabilitation

(e.g., motor function restoration), intelligent prosthetic control, and fundamental neuroscience research (e.g., the analysis of neural coding mechanisms).^{1,2} Based on the method of signal acquisition, brain neural signal acquisition systems can be classified into two types: non-invasive and invasive. Non-invasive systems collect signals using head-mounted electrode arrays, offering advantages such as high safety and ease of use; however, they typically suffer from low signal-to-noise ratio (SNR) and limited spatial resolution. These

systems are primarily used in basic research, including cognitive function assessment, emotional state monitoring, and clinical auxiliary diagnosis of epilepsy and sleep disorders.^{3,4} In contrast, invasive systems implant microelectrode arrays surgically into the brain to directly record neuronal electrical activity. These systems provide high SNRs (typically >30 dB) and sub-millimeter spatial resolution and are commonly employed in clinical applications such as precise localization of epileptic foci and deep brain stimulation (DBS) therapy.^{5,6} Brain neural signals can be acquired using high-throughput systems, where the number of channels determines the comprehensiveness and resolution of brain information. As the demand for channel density increases in neuroscience research, current systems face a series of technical challenges, including high throughput, signal quality, device miniaturization, and high-speed wireless data transmission.^{7,8}

In the realm of wireless communication, Bluetooth Low Energy (BLE) is widely utilized in physiological signal monitoring systems due to its low power consumption and portability. For instance, Alfian *et al.* proposed a BLE-based diabetes monitoring system that combines real-time data processing with machine learning algorithms, using a multilayer perceptron (MLP) for patient classification and a long short-term memory (LSTM) for blood glucose prediction. Their experiments demonstrated the system's efficiency and accuracy.⁹ Similarly, Perez-Diaz-de-Cerio *et al.* developed a BLE-based runner tracking system that employs broadcast mode to ensure reliable detection in dense environments, validating its low power consumption and high detection rate.¹⁰ However, due to the inherently limited sampling rate of BLE protocols (typically <1 kSPS), they fall short of supporting real-time transmission of EEG signals across thousands of channels.¹¹ To overcome this limitation, a lossless compression algorithm based on co-travel encoding has been proposed, enabling high-rate wireless transmission during high-throughput signal acquisition.¹²

In the field of high-throughput transmission, existing neural signal acquisition systems generally operate with fewer than 256 channels. For example, Itoh *et al.* proposed a 12-channel noninvasive active electrode array that enabled stable EEG and cortical auditory evoked potential (CAEP) recordings in awake horses, demonstrating the feasibility of reliable acquisition under complex hair conditions using brush-type active electrodes; however, its limited channel coverage and spatial sampling density constrain fine-grained source localization and large-scale network analysis.¹³ Liu *et al.* developed a 32-channel microneedle dry-electrode patch, which significantly reduced skin-electrode contact impedance by penetrating the stratum corneum, thereby achieving high-quality EEG, ECG, and EMG recordings without conductive gel. This design highlights advantages in miniaturization and wearability, but the overall channel capacity and system bandwidth remain restricted by front-end integration and data link throughput.¹⁴ Sohrabpour *et al.* investigated the influence of electrode number on epileptic source localization accuracy, showing that increasing channel counts markedly reduces localization error and provides better support for surgical planning, while also indicating diminishing marginal returns at higher channel densities, underscoring the need to optimize electrode configurations under acceptable complexity and cost.¹⁵ With the rising demand for higher decoding accuracy, high-density electrode arrays (>1000 channels) are increasingly

required to enhance spatial sampling and whole-brain network representation. Such systems, by improving coverage density and spatial resolution, can substantially strengthen the global characterization of neural activity and provide essential hardware support for analyzing dynamic coding mechanisms in neuronal populations, such as oscillatory synchronization and cross-regional information transfer.^{16,17} Nevertheless, scaling EEG systems toward the kilochannel level faces multiple bottlenecks. First, to achieve stable gains in source imaging, denser and more uniform electrode coverage over the scalp is required, but this is constrained in practice by electrode placement time, individual head geometry, and hair conditions.¹⁸ Second, in high-density arrays, channel crosstalk, reference schemes, and spatial registration accuracy exert stronger influences on source localization, thereby necessitating higher common-mode rejection ratio (CMRR), low-noise front ends, and precise electrode position information.^{19,20} Finally, although clinical-grade 256-channel HD-EEG has already been used for routine recordings (e.g., at 1 kHz sampling rate), issues of device bulk, wiring complexity, long-term wearing comfort, and large-scale data throughput and management remain major obstacles to further scaling toward kilochannel systems.^{21,22}

To address the aforementioned challenges, this study presents a high-throughput, high-speed wireless neural signal acquisition system that offers several key advantages. It features a modular PCB design that integrates up to 1024 channels while maintaining overall device miniaturization. A co-travel encoding-based compression algorithm is implemented to achieve low-power, bidirectional data transmission over Bluetooth Low Energy (BLE), effectively meeting the requirements for real-time monitoring of high-throughput neural signals. The system also adopts a mixed-signal circuit design that leverages the advantages of both analog and digital circuits to optimize signal acquisition and amplification, improve common-mode rejection, and enhance resistance to interference. Furthermore, FPGA-based parallel processing is employed to take full advantage of its high computational concurrency, enabling real-time signal processing and feedback and ensuring the system's high efficiency and responsiveness.

In this study, the performance of the proposed system was validated through both laboratory electrical tests and animal experiments. The laboratory tests demonstrated that the system is capable of wirelessly acquiring and recording weak neural signals with high fidelity. In animal experiments, the system successfully achieved real-time acquisition and wireless transmission of weak neuroelectrical signals at a high sampling rate and with high throughput, offering a practical solution for multi-channel, high-speed wireless neural signal acquisition.

II. MATERIALS AND METHODS

A. Overall system design

The overall design framework of the high-throughput, high-speed wireless brain neural signal acquisition system is illustrated in Fig. 1. The system consists of five main modules: an EEG signal acquisition and processing module, an implant-side wireless transceiver module, a power routing and intelligent management module, an external wireless transceiver module, and a host computer-based human-computer interaction interface. Among them, the EEG signal acquisition and processing module integrates

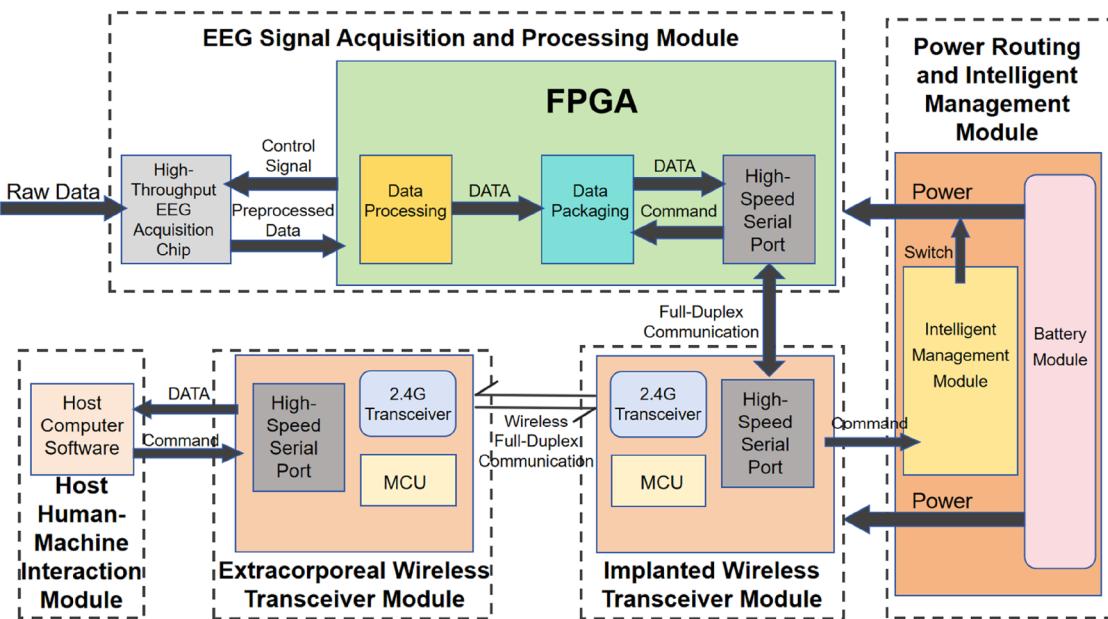


FIG. 1. Overall design framework.

a high-throughput EEG acquisition chip and an FPGA-based master control unit.

The system operates as follows: the host computer first sends operational instructions to the external wireless transceiver module, which forwards them to the implant-side transceiver via full-duplex wireless communication. These instructions are then delivered to the FPGA's RX interface via a serial connection. The FPGA subsequently issues control signals to the designated high-throughput EEG acquisition chip, which acquires, transmits, and preprocesses 256-channel raw data. The preprocessed data are then sent back to the FPGA for further processing and packaging. Once the data are packaged, they are transmitted through the FPGA's serial TX interface to the implant-side wireless module, which then sends them to the external transceiver module. Finally, the data are transmitted to the host computer, where they are decoded, analyzed, and displayed in real time as waveform signals.

The host computer software is used to control and monitor the real-time streaming data received by the personal computer (PC). Given the large number of channels and the substantial volume of data collected by the system, two data transmission modes—raw data mode and spike mode—are implemented with corresponding functionalities. Prior to using the host software, the user simply needs to connect the wireless data receiver to the PC, select the spike mode, and perform peak potential detection for each channel. Channels exhibiting frequent spike events can then be switched to raw data mode to display the single-channel neural signal waveform in real time. In addition, the received raw data can be exported and stored for offline processing and analysis using dedicated data processing software.

B. Core module design

1. Data acquisition and processing module

The data acquisition and processing module comprises a main board and daughter boards. Serving as the core control unit, the main board manages data acquisition and transmission and coordinates the operation of the daughter boards. It is equipped with an FPGA chip, a NOR flash memory chip, and a high-throughput EEG acquisition chip. The FPGA sends control signals to the EEG acquisition chip and processes the incoming signals, while the flash chip stores the HDL configuration code, ensuring the program is retained even after power loss. The acquisition channels of the EEG chip connect to a ZIF interface, which receives neural signals and transmits preprocessed data to the FPGA.

The FPGA chip employed in this system uses a fine-pitch Ball Grid Array (BGA) package with 324 pins. It offers 126 800 logic cells and supports high-density I/O configurations with a total of 63 400 configurable logic blocks. It also integrates 135 RAM-based logic blocks for high-speed data buffering and DSP slices for efficient digital signal processing. The core operating voltage ranges from 1.0 to 1.8 V, with a minimum operational threshold of 0.95 V.

The selected NOR flash chip consists of multiple independently erasable and programmable memory units, offering features such as non-volatility, low cost, and power-down retention. It operates at 1.8 V and is used to solidify the FPGA configuration program.

The system integrates four 256-channel neural signal acquisition chips to construct a 1024-channel recording array. Each 256-channel acquisition chip is designed using a modular digital architecture [IC REF: An expandable 36-channel neural recording

ASIC with modular digital pixel design technique], occupying an area of $5 \times 5 \text{ mm}^2$ and consuming $55 \mu\text{W}$ per channel at 1.8 V. Figure 2 illustrates the functional block diagram of this chip. It supports simultaneous acquisition of up to 256 neural signals and includes a high-performance low-noise amplifier (LNA) with an input-referred noise of $6 \mu\text{VRms}$, suitable for capturing weak extracellular signals from the cerebral cortex. Each channel integrates a bandpass filter (BPF) and an analog-to-digital converter (ADC), enabling on-chip filtering in the 300 Hz to 10 kHz range and digital conversion with up to 12-bit resolution at a sampling rate of 32 kSPS. The integrated ADC ensures real-time digitization of EEG signals at high sampling rates, enhancing temporal resolution and enabling accurate tracking of dynamic neural activity. This highly integrated chip design combines amplification, filtering, digitization, and data transmission in a single compact unit, simplifying system architecture, improving stability, and offering advantages in miniaturization, low power consumption, and high integration.

2. Implantable wireless data transceiver modules

The implantable wireless data transceiver module employs a low-power, highly integrated Bluetooth chip (CH582M, WCH, Shenzhen, Guangdong, China) as its main controller. This chip integrates a 2.4 GHz wireless communication module, RF receiver, control link, and antenna matching network. It features built-in flash

memory ranging from 64 to 128 KB and 4 KB of SRAM and supports multiple power-saving modes, including sleep and standby. The wireless data transceiver module is responsible for transmitting high-throughput neural data to the host computer and receiving control commands in return. In addition, the transceiver board incorporates PMOS-based power control circuitry. Upon receiving a wireless power-on instruction from the host computer, the Bluetooth chip activates the PMOS circuit to supply power to the data acquisition mainboard, thereby initiating the system. Conversely, when data acquisition is not required, the host computer can issue a power-off command to disable the mainboard's power, thereby conserving energy and prolonging battery life.

3. Power routing and intelligent management module

The power routing module consists of a battery board for battery installation and a power distribution system integrated into the wireless data transceiver board. Designed to meet the multi-voltage power supply demands (1.0, 1.8, 3.3 V) of the system—particularly the low-noise requirements of the FPGA and high-precision acquisition chips—the module utilizes a hybrid power architecture to achieve high-performance power conversion. At its core, the system employs the latest generation of power management chipsets from Texas Instruments (TI): the TPS63070, a high-efficiency

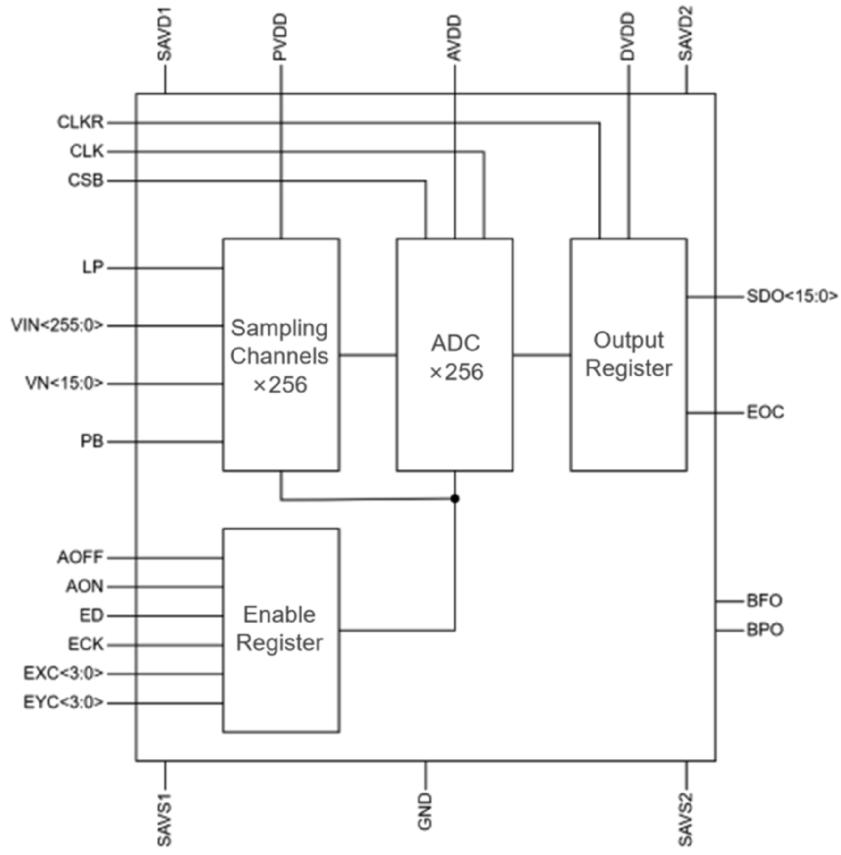


FIG. 2. Functional block diagram of the acquisition chip.

synchronous buck-boost converter, and the TPS74901, an ultra-low-dropout (LDO) linear regulator. Together, they form a stable and efficient power supply system.

The TPS63070 functions as the main DC/DC converter [Fig. 3(a)], featuring wide input voltage support (2–16 V) and precise output regulation (2.5–9 V). It converts the standard 3.3 V input to supply stable power for both the low-power Bluetooth chip and the

high-throughput neural signal acquisition chip. It can provide up to 2 A of continuous current in both buck and boost modes, effectively compensating for battery voltage fluctuations. Complementing this, the TPS74901 LDO regulator provides dual precision outputs (1.0 and 1.8 V) from a 0.8–5.5 V input range, tailored to meet the low-noise requirements of the FPGA. This topology combines the high efficiency of switching regulators with the ultra-low noise benefits of

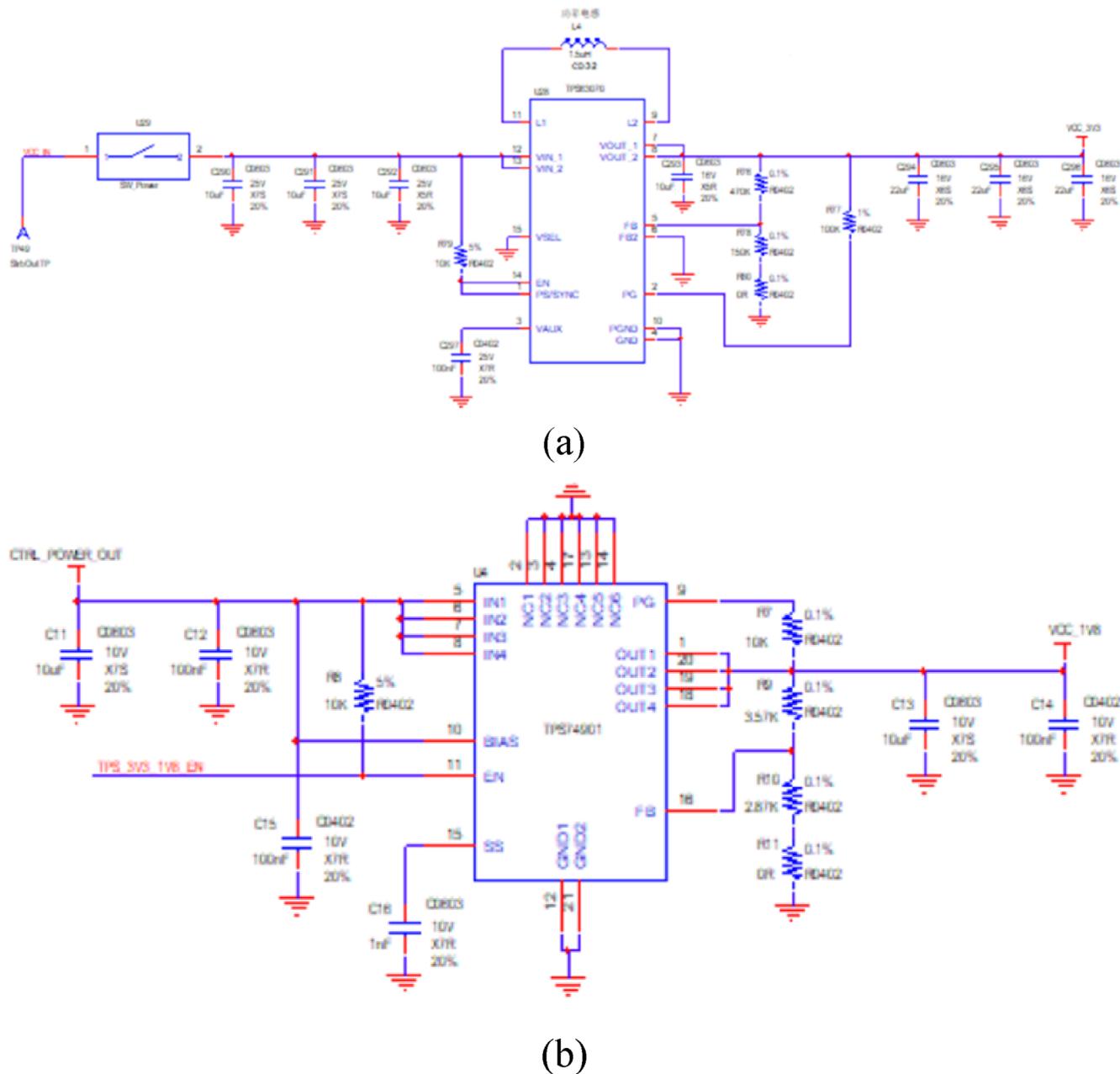


FIG. 3. Power module power conversion system circuit. (a) DC/DC power module core circuitry. (b) LDO power module core circuitry.

linear regulators. Both components are packaged in compact QFN housings (TPS63070: $2.5 \times 3 \text{ mm}^2$; TPS74901: $5 \times 5 \text{ mm}^2$), enabling efficient, multi-voltage power management in a miniaturized design suitable for implantable biomedical systems.

C. PCB design and functional prototyping

To meet the high-precision requirements of brain-computer interface (BCI) hardware for neural signal acquisition, the system adopts a ten-layer high-density PCB stack to optimize mixed-signal design. The stack follows an alternating “signal-ground-power” configuration: layers 2, 4, 7, and 9 are continuous copper ground planes, forming a comprehensive electromagnetic shielding structure. The top layer (L1) and layer 3 (L3) serve as the high-speed digital signal layer and the microvolt-level analog signal layer, respectively. The digital signal layer supports the parallel bus communication between the FPGA and the 256-channel acquisition chip. By inserting a ground layer (L2) between these signal layers, over 20 dB of cross-layer isolation is achieved. Power distribution is also layered: analog power (1.0, 1.8, 3.3 V) is routed through layers L5 and L8, while digital power (1.0 V/1.8 V) is distributed via layers L6 and L10. Using plane segmentation techniques, the inter-domain crosstalk in the power layers is suppressed to below 1 mV.

At the same time, a multidimensional, collaborative PCB layout strategy is employed. For mixed-signal isolation, physical separation zones wider than 3 mm are used, with analog and digital domains strictly partitioned and interconnected using ferrite beads. For signal routing, the high-speed parallel bus between the FPGA and the 256-channel acquisition chip is precisely length-matched within ± 5 mil. EEG signals at the microvolt level are transmitted via shielded ribbon traces (4 mil width, $50 \Omega \pm 5\%$ impedance), accompanied by adjacent ground lines and grounding vias spaced every 200 mil. These measures suppress inter-channel crosstalk to below -60 dB. The power supply architecture further enhances signal integrity. The digital power domain is meshed with copper planes and equipped

with a composite decoupling capacitor array (0.1 and $10 \mu\text{F}$). The analog power plane maintains a continuous copper layer and incorporates an LC+RC π -filter network to reduce power supply noise effectively.

Due to space constraints caused by integrating four 256-channel acquisition chips on a single PCB, the system employs an FPC (flexible printed circuit) connection between the main board and daughter boards. To achieve miniaturization and lightweight design while supporting 1024-channel high-speed acquisition, a stacked architecture is used. The implantable device consists of a data acquisition and processing main board, two acquisition daughter boards, a wireless data transceiver and power management board, and a battery board [Fig. 4(a)].

As the core control unit, the main board ($5.3 \times 5.3 \text{ cm}^2$) houses an FPGA that controls both its own two acquisition chips and the two additional daughter boards. The main board integrates an FPGA, two 256-channel acquisition chips, two FPC interfaces, and four ZIF connectors. Each 3 mm 39-pin FPC interface connects to a daughter board to transmit FPGA control signals. Each 2 mm 71-pin ZIF interface connects to the electrode array, with one interface serving 68 channels; each 256-channel chip is linked to two ZIF connectors. Each daughter board ($2.9 \times 2.9 \text{ cm}^2$) functions solely as a data acquisition unit, equipped with one 256-channel acquisition chip, one FPC interface, and two ZIF connectors. These boards receive control signals from the FPGA via the FPC connection and route data to the electrode arrays through ZIF connectors. The wireless data transceiver and power management modules are integrated onto a circular PCB (diameter: 3.5 cm), powered by a battery board (diameter: 2.5 cm) carrying a 5 V rechargeable Li-ion battery with a 90 mAh nominal capacity. The system operates continuously for 30–40 min under active conditions. The wireless and power management board integrates a low-power Bluetooth chip (CH582M), a buck-boost converter (TPS63070), and two low-dropout linear regulators (TPS74901). The Bluetooth chip wirelessly transmits acquired data to the host receiver. The TPS63070 regulates battery voltage to a stable 3.3 V output, which is then further stepped

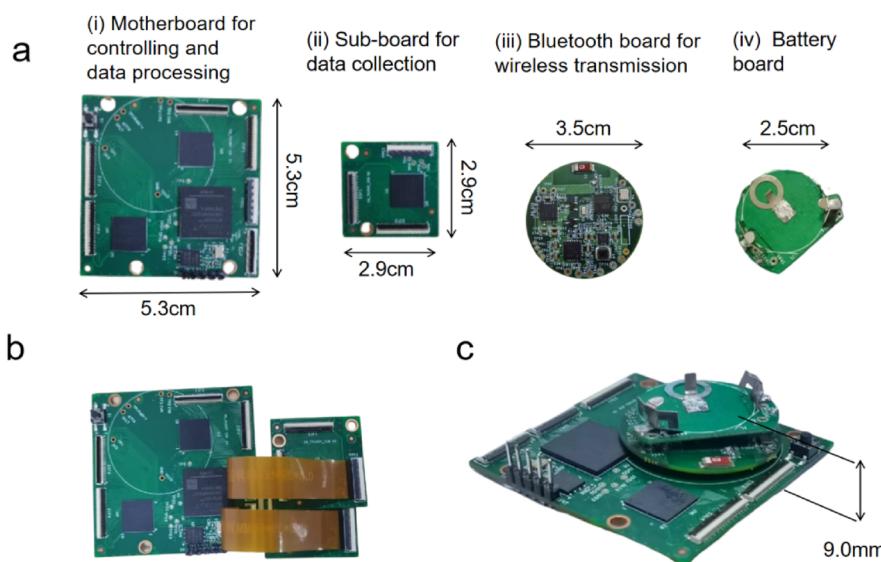


FIG. 4. Architecture of the high-throughput brain neural signal acquisition system: (a) hardware composition: motherboard for controlling and data processing, sub-board for data collection, Bluetooth board for wireless transmission, and battery board; (b) connection between the motherboard and the sub-board via an FPC interface; and (c) stacked architecture of the motherboard for controlling and data processing, the Bluetooth board for wireless transmission, and the battery board.

down by two TPS74901 regulators to 1.8 and 1.0 V to supply the entire system.

The main board and daughter boards are connected via FPCs [Fig. 4(b)], which relay control signals from the FPGA to the acquisition chips. The wireless/power board and battery board are sequentially soldered and stacked onto reserved contact pads on the main board [Fig. 4(c)], with pad-through-hole positions standardized across the design. The final assembled system measures $5.3 \times 5.3 \times 0.9 \text{ cm}^3$, fulfilling the requirements for standard laboratory experiments in mice.

On the host side, the control software provides both real-time data acquisition and playback functionalities. During real-time acquisition, a power-up command is first issued, and the acquisition process begins only after a “power-up complete” signal is received from the implant terminal. If the implant terminal reports a low-power warning, the host interface displays an “insufficient power” alert and halts data acquisition. The host can also manually terminate data collection by issuing a stop command as needed. Real-time acquisition supports two working modes: spike mode [Fig. 5(a)] and raw data mode [Fig. 5(b)]. In spike mode, peak potential detection is performed across all channels. If a specific channel exhibits a high frequency of spikes, the system can switch to raw data

mode to display the corresponding waveforms in real time. Meanwhile, the collected data can be recorded for subsequent analysis. The playback function allows users to review waveform data and export specific segments for offline processing. The user interface is designed with usability in mind, offering a user-friendly and efficient human-computer interaction experience.

D. Spike detection algorithm

One of the most commonly used median-based estimation formulas in contemporary peak sorting algorithms is

$$Thr = 4 \times \text{median}\left(\frac{|x|}{0.6745}\right). \quad (2.1)$$

The constant 0.6745 is derived from the inverse cumulative distribution function of the standard normal distribution at a probability of 0.75. This method assumes that the background noise follows a standard Gaussian distribution. Even if the actual noise distribution deviates from Gaussian, Quiroga demonstrated that the threshold obtained using Eq. (2.1) is more accurate than those derived from using 3–5 times the standard deviation.²³

However, in certain conditions, such as relatively low signal-to-noise ratios or low peak firing frequencies, Shi *et al.* found that the accuracy of Eq. (2.1) is not high. Consequently, an improved version was proposed, as follows:²⁴

$$Thr = \frac{\text{median}\left\{\frac{|x|}{0.6745}\right\} \sqrt{2 \log_2(n)}}{1.6}. \quad (2.2)$$

In this context, n represents the length of the detected data. By incorporating n , Eq. (2.2) reduces the interference caused by confounding noise introduced by the recording environment, making it more suitable for adaptive thresholding algorithms. Under conditions with even lower signal-to-noise ratios, Zhao *et al.* proposed a new estimation, given as follows:²⁵

$$Thr = \text{median}\left(\frac{|x|}{0.6745}\right) \sqrt{\frac{\log_2(n)}{n} \left(\frac{\ln n}{\ln 2}\right)^3 q}. \quad (2.3)$$

Equation (2.3) mitigates the interference caused by noise fluctuations, where q serves as a fluctuation factor. A properly selected value of q can enhance the robustness of the defined threshold. The aforementioned estimation methods all rely on the median of the data. To identify a more optimal threshold, we propose combining two statistical indicators as a unified threshold metric: the median of background noise μ_{med} and the mean of background noise μ_{mean} . As shown in Eqs. (2.1)–(2.3), despite varying complexity, these threshold estimation formulas essentially consist of a scaled median. Based on this observation, we define a new threshold expression incorporating both μ_{med} and μ_{mean} in the form of Eq. (2.4),

$$Thr = \alpha \mu_{\text{med}} + \beta \mu_{\text{mean}}, \quad (2.4)$$

$$ACC = \frac{TDS}{TDS + MS + FA} \times 100\%. \quad (2.5)$$

In Eq. (2.4), α and β are corresponding the parameters, and selecting appropriate values for them allows for the calculation of an optimized threshold. Using MATLAB software, α and β are determined

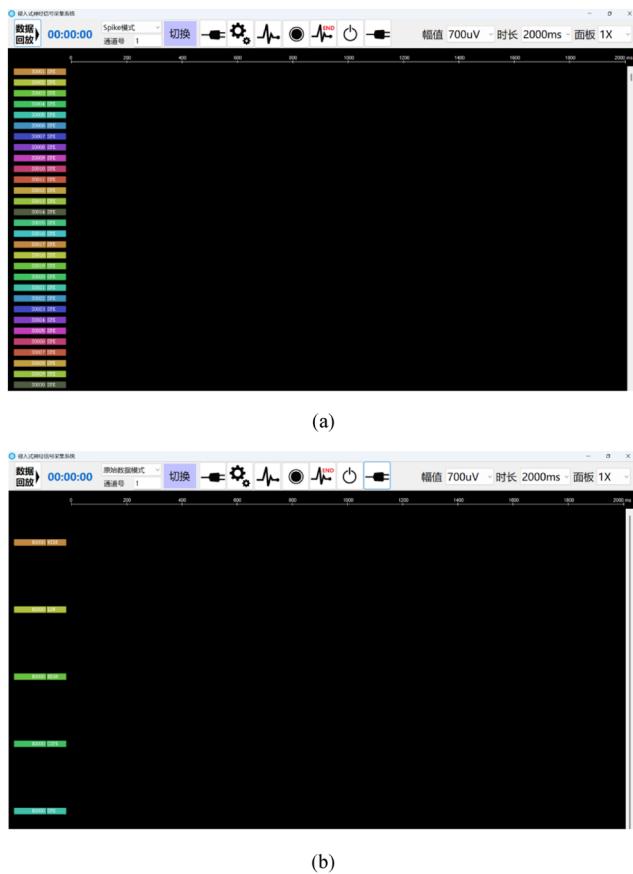


FIG. 5. Upper computer software interface. (a) Spike mode interface. (b) Raw data mode interface.

by performing a scanning test within the range of 1–5. Their performance is evaluated using an accuracy metric defined by Eq. (2.5).²⁶ In this equation, TDS denotes the number of true detections—i.e., the number of correctly detected spike potentials within a sequence; MS represents the number of misdetections, corresponding to noise signal peaks incorrectly identified as spikes; and FA refers to the number of false negatives, i.e., actual spike potentials that were missed during detection.

III. RESULTS

A. Laboratory electrical tests

To verify the system's capability in recognizing, post-processing, sampling, analog-to-digital conversion, and transmitting weak electrical signals, a series of electrical performance debugging procedures were conducted. A photo of the experimental setup is shown in Fig. 6.

Due to the low voltage amplitude of EEG signals, the original EEG waveform is often obscured by background noise. Therefore, a system noise test was first performed. All acquisition channels were grounded, and the noise voltage was evaluated by calculating the standard deviation of the output data. This provided a quantitative measure of the system's noise performance. Figure 7 shows the waveform recorded during the noise test. The system's noise voltage was calculated to be $8.56 \mu\text{V}$, which is close to the $6 \mu\text{V}$ value specified in the acquisition chip's datasheet. These results demonstrate the feasibility of using the proposed system for reliable EEG signal acquisition.

To further verify the signal acquisition performance of the system, a signal generator was used to output sine waves with peak-to-peak amplitudes of 2 mV at frequencies of 800 and 1100 Hz , respectively, under high-impedance conditions. These signals were attenuated to a peak-to-peak amplitude of $600 \mu\text{V}$ using a precision voltage divider module to simulate weak bioelectrical signals and were then input into each acquisition channel for performance testing.

The sampling rate was set to 32 kHz , and real-time data transmission was achieved at 2.5 Mbps via the UART serial port of the FPGA. Subsequently, the data were wirelessly transmitted using

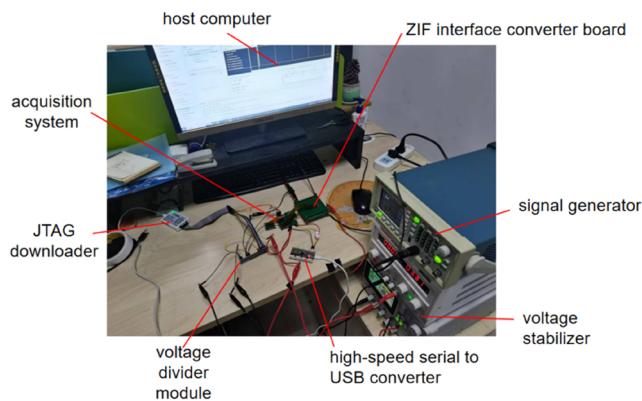


FIG. 6. Functional verification experiment site diagram of high-throughput, high-speed brain neural signal acquisition system.

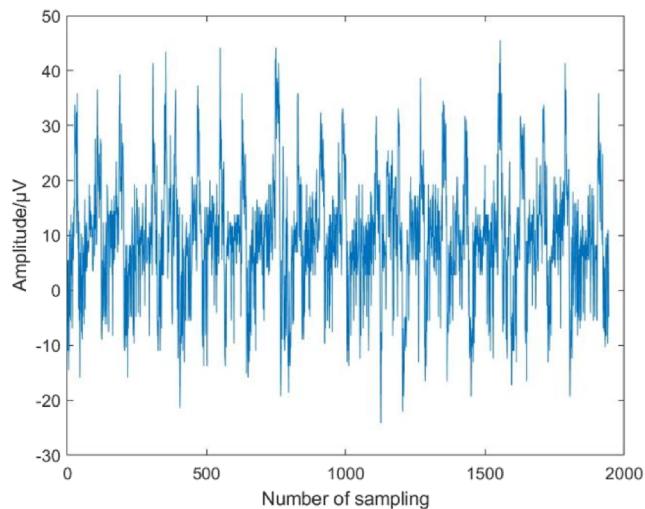


FIG. 7. Noise test of the EEG signal acquisition system.

a low-power Bluetooth module. According to the communication protocol between the FPGA and the host software, a power-up command is first issued via the serial port to activate the power supplies of both the main and daughter boards through the wireless data transceiver and power management module. Once a “power-on complete” response is received from the motherboard, the host sends the mode selection and channel configuration commands, followed by the acquisition command. Each data frame consists of a 2-byte header, a 4-byte timestamp, a 2-byte channel identifier, 80 bytes of acquired data, and a 2-byte tail indicating spike detection results.

After data acquisition, time- and frequency-domain analyses were performed in MATLAB, as shown in Fig. 8. In the time domain, when 800 and 1100 Hz sine waves were input, the corresponding output waveforms are presented in Figs. 8(a) and 8(c), respectively. The signal amplitudes ranged from ± 200 to $\pm 300 \mu\text{V}$, and the waveforms were smooth, continuous sinusoids with no significant distortion or aberrations, indicating high signal fidelity. In the frequency domain, Figs. 8(b) and 8(d) show the corresponding spectral results. The spectra clearly exhibit prominent peaks at 800 and 1100 Hz for their respective input signals, with no significant harmonic components detected, suggesting minimal harmonic distortion. Although some low-frequency noise is present, its amplitude is negligible and does not affect the dominant frequency components. In conclusion, the results of the bench-top electrical testing demonstrate that the system can reliably acquire 800 and 1100 Hz sine wave signals with high stability and purity in both the time and frequency domains, verifying the robustness of the test system and the high quality of signal acquisition.

B. Experimental animal studies

To further validate the functionality of the system, animal experiments were conducted. Mice provided by the Shanghai Institutes for Biological Sciences, Chinese Academy of Sciences, were used in these experiments. A bilaterally symmetric 128-channel

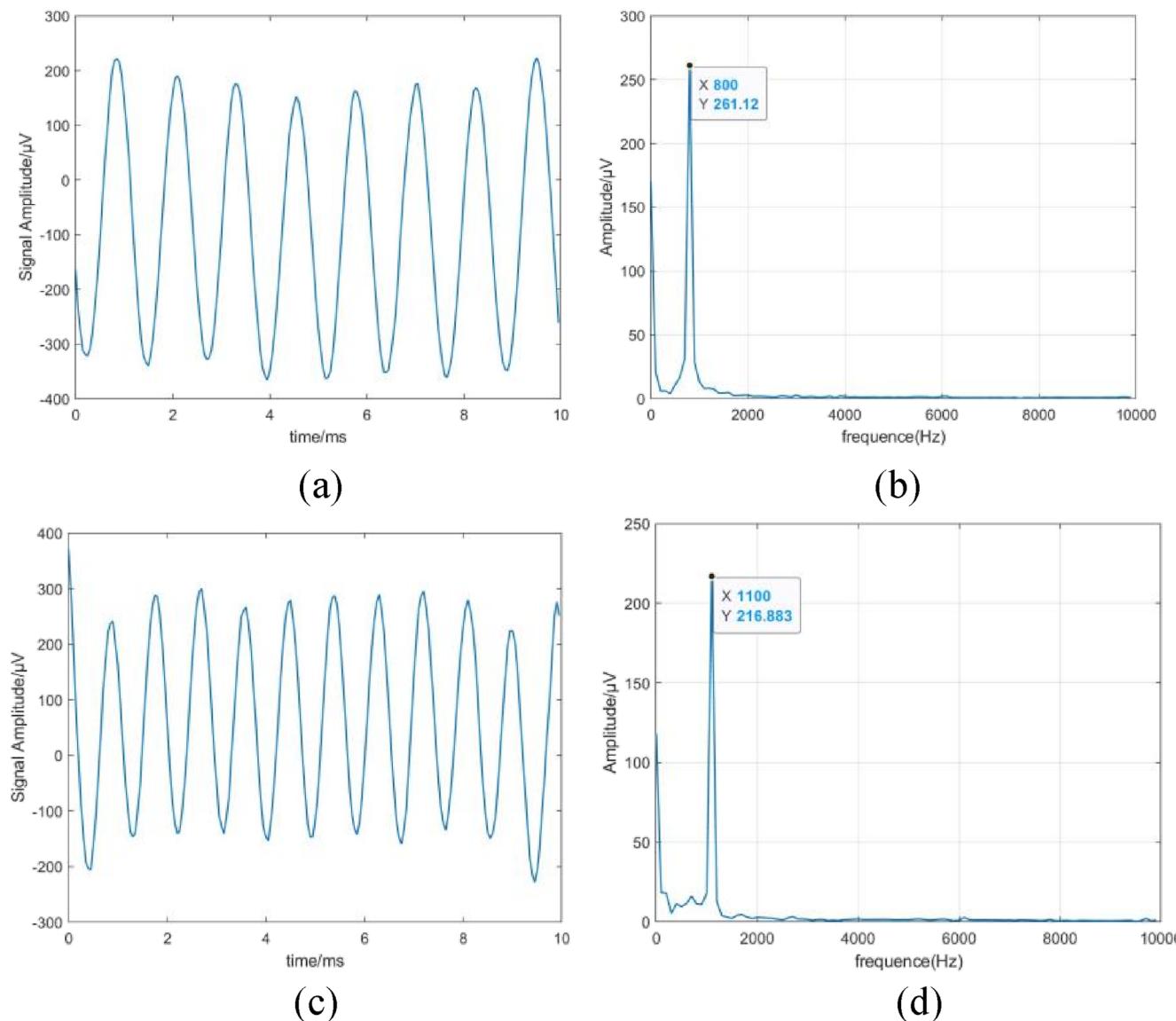


FIG. 8. Performance test results plotted in time-frequency domain waveforms. (a) Time-domain waveform of 800 Hz sine wave. (b) Frequency spectrum of 800 Hz sine wave. (c) Time-domain waveform of 1100 Hz sine wave. (d) Frequency spectrum of 1100 Hz sine wave.

electrode array was implanted in the active regions of the brain, with 64 channels distributed on each hemisphere. The experimental setup is shown in Fig. 9. During the procedure, the mice were secured on the surgical platform such that the implanted electrodes shared a common ground with the platform. The electrode array on one hemisphere was connected to the ZIF (Zero Insertion Force) connector on the system board, and the implantable device was fixed on the dorsal side of the mouse's head. To ensure a common ground among the acquisition system, the electrodes, and the surgical platform, the ground wire of the acquisition system was connected to the platform via a shared metal grounding frame. The

system was initialized through the graphical user interface (GUI) on the host computer, enabling real-time monitoring, acquisition, and recording of multichannel neurophysiological signals.

After completing the animal experiments, the recorded data were exported from the host computer and analyzed. The raw signals were high-pass filtered using MATLAB, and spike detection was performed by setting a threshold at three times the negative standard deviation of the signal's mean amplitude. Spike waveforms with distinct morphological features were extracted using an automated algorithm. Subsequent morphological and time-frequency analyses of the identified waveforms confirmed the

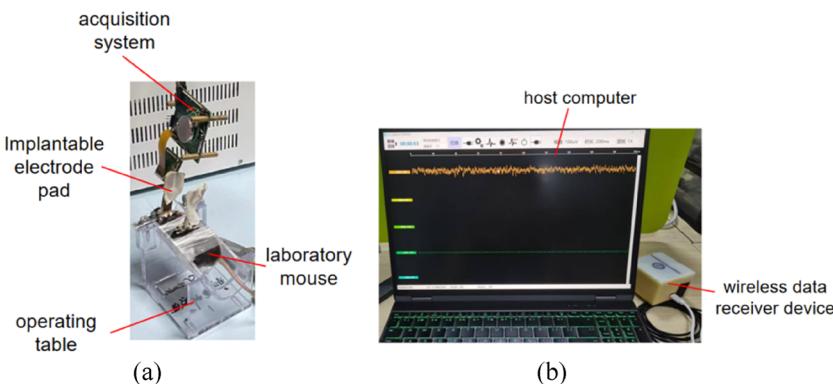


FIG. 9. Field diagram of mouse brain neural signal acquisition experiment. (a) Animal experiment operating table. (b) Upper computer and data receiving device.

system's capability for reliable neural signal acquisition and feature extraction.

After exporting the raw data obtained from animal experiments through the upper computer acquisition system, the EEG signal waveforms were plotted using MATLAB, as shown in Fig. 10. The original EEG waveform was primarily dominated by large-scale low-frequency interference. To address this, the data were high-pass filtered in MATLAB to remove low-frequency noise below 300 Hz, resulting in the waveform shown in Fig. 11. Subsequently, peak potential signals were identified and superimposed according to a predefined peak potential threshold.

The peak potential signal is divided into three components: resting potential, action potential, and after-potential. The resting potential represents the normal state, while the action potential is characterized by a brief period of significant potential change and recovery on the neuron's cell membrane, with an amplitude range

of 50–100 μ V. Following this, the recovery phase forms the after-potential, which is slightly higher than the resting potential. Peak potentials are typically identified based on the waveform characteristics of these three components. The waveform of the peak potential signal, as superimposed by the peak potential threshold, is shown in Fig. 12. This waveform is distinguished by the presence of a distinct “spike” component below the peak potential threshold, with a significant difference in amplitude compared to the surrounding signal, resulting in a clear and identifiable waveform feature. The waveforms of the two superimposed signals are similar to the standard peak potential morphology, with three potential waveform characteristics: a peak level of ~60 μ V on the left side and a peak level of ~70 μ V on the right side. The signal-to-noise ratios (SNRs) of each channel of the acquisition system have the maximum and minimum values of 28.66 and 30.56 dB, respectively, to further verify the signal quality and consistency.

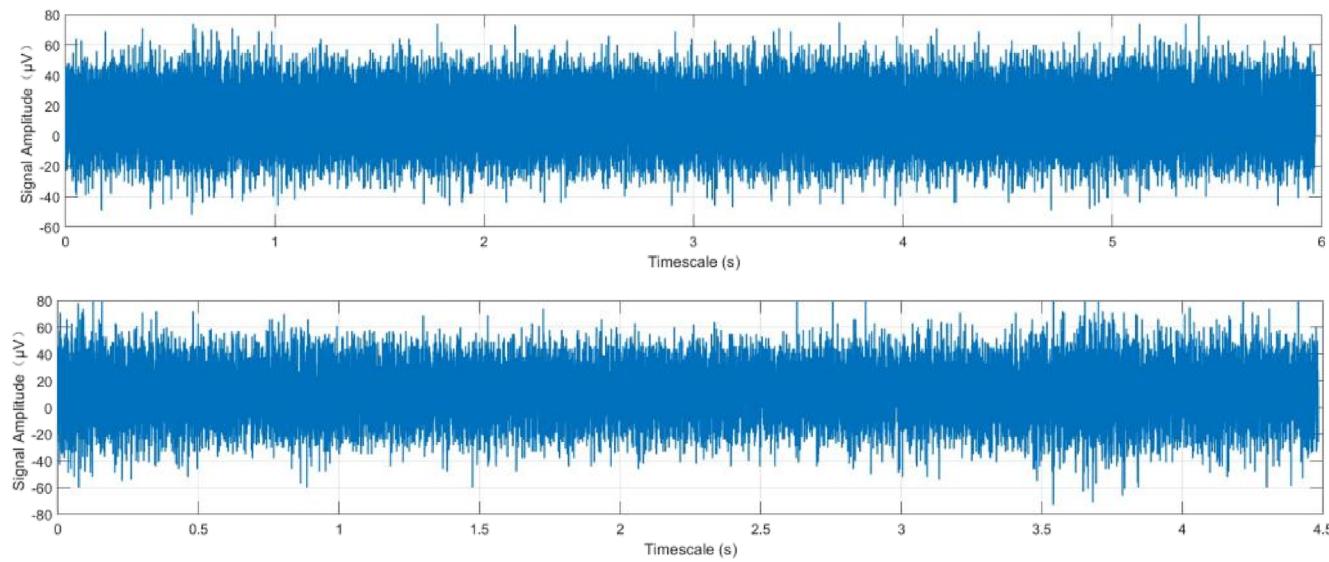


FIG. 10. Raw data waveform of the upper computer acquisition system.

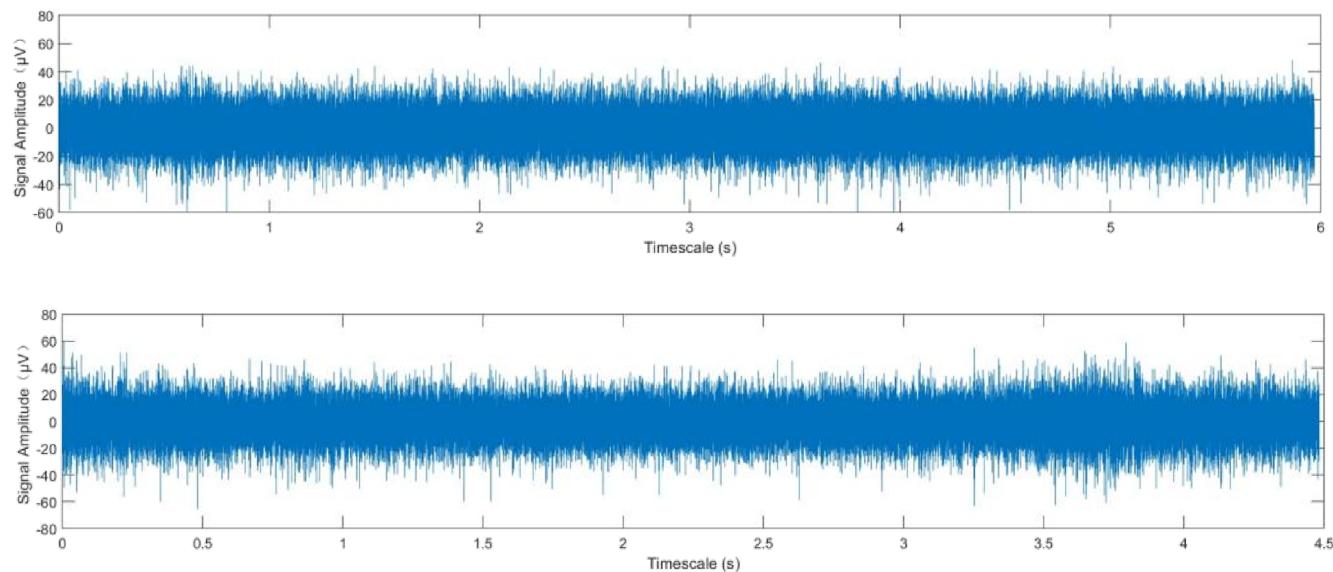


FIG. 11. High-pass filtered waveform of the acquired data.

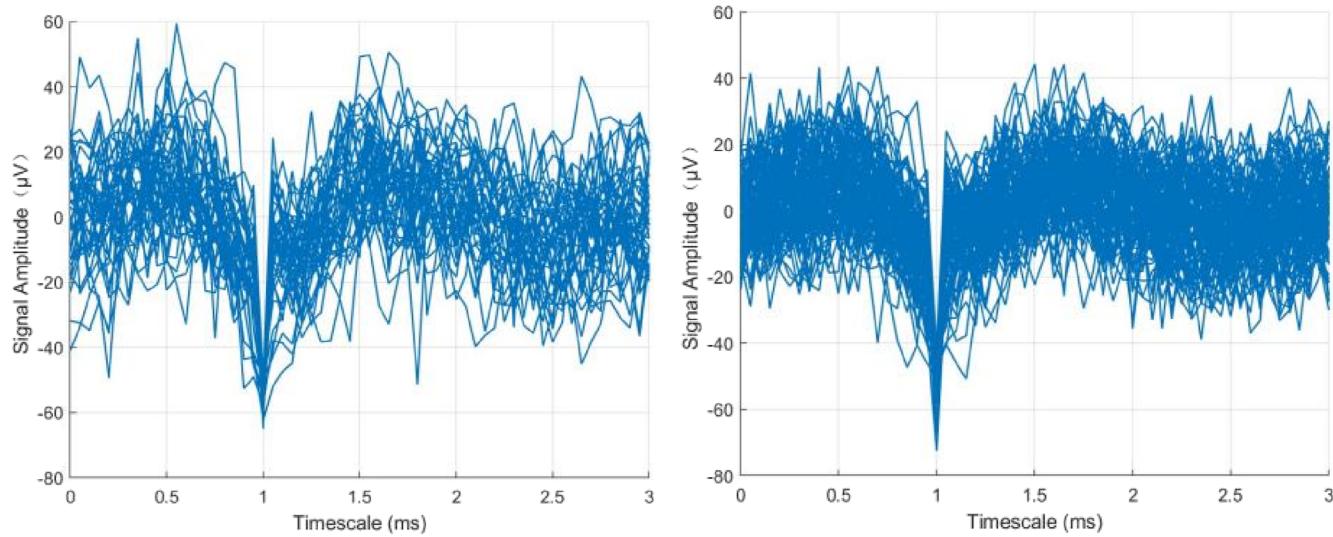


FIG. 12. Superposition of peak potential signals.

IV. DISCUSSION

In this study, a 1024-channel high-speed wireless brain-computer interface (BCI) system was developed to enable high channel-count integration, high-speed wireless transmission, and optimized signal quality, thereby advancing research in brain-computer interface technologies. The system features a modular PCB design and a mixed-signal circuit architecture that support simultaneous acquisition across 1024 channels, aligning with the current trend toward high-density electrode arrays. As noted by Wang *et al.*, high channel-count systems (exceeding 1000

channels) can significantly enhance the spatial resolution of neural signals, providing a robust hardware foundation for investigating the dynamic encoding mechanisms of neural populations.²⁷

In the field of wireless transmission, the system adopts an improved compression algorithm based on co-travel coding to enable real-time transmission of high-throughput signals via low-power Bluetooth (BLE), thereby meeting the requirements of high sampling rate wireless transmission. This approach is similar to the selective Huffman coding-based compression/decompression scheme proposed by Jas *et al.*, which achieves a compression ratio

close to that of optimal Huffman coding while maintaining a minimal decoder area overhead.²⁸ To address the amplitude shift observed in high-frequency signals (e.g., 1100 Hz)—which may result from high-frequency attenuation in the voltage divider circuit or environmental electromagnetic interference—an adaptive filtering algorithm is applied to enhance the signal-to-noise ratio (SNR) and effectively reduce noise, as demonstrated in the study by Panda *et al.* Their work provides a valuable reference for improving the anti-interference capability of this system.²⁹

Animal experiments validated the system's effectiveness in multi-channel acquisition under dynamic conditions; however, some channels exhibited signal degradation due to motion artifacts. Megalingam *et al.* found that such artifacts distort EEG signals in dynamic environments, and their artifact removal method based on an empirical error model led to a maximum accuracy improvement of 20% and an average improvement of 18% in EEG signal quality.³⁰ Despite its high-speed multi-channel acquisition capability, the system's endurance is currently limited. A 5 V rechargeable lithium-ion battery with a nominal capacity of 90 mAh provides only 30–40 min of operation, restricting its clinical applicability. Li *et al.* developed a prototype wireless neurophysiological acquisition system that significantly reduces the power consumption of the Bluetooth module, and this power reduction remains largely unaffected by changes in sampling rate, payload size, or transmission interval.³¹ Their approach offers an effective path for extending the operational time of the system.

In conclusion, this study provides a valuable reference for the development of non-invasive, high-density, high-speed wireless brain–computer interface systems. By addressing key challenges such as power consumption, noise suppression, and adaptability to dynamic environments, the system contributes to advancing both research and clinical translation of BCIs. In future work, integrating multimodal signal fusion techniques (e.g., EEG-fNIRS joint analysis³²) and deep learning algorithms³³ may further enhance decoding performance and system utility.

V. CONCLUSION

In this study, a 1024-channel high-speed wireless brain–computer interface (BCI) system was successfully developed for high-throughput neural signal acquisition, offering improved spatial resolution and signal integrity. The system operates at a high sampling rate of 32 kHz and transmits data via low-power Bluetooth (BLE), while employing optimized mixed-signal circuitry and an FPGA-based parallel processing architecture to enhance anti-interference performance and ensure high efficiency and real-time capability. *In vitro* experiments demonstrated that the system can reliably acquire weak neural signals with peak-to-peak amplitudes of 600 μ V and frequencies of 800 and 1100 Hz at a 32 kHz sampling rate. Furthermore, animal experiments validated the system's feasibility in real-time, multi-channel neural signal acquisition under dynamic conditions.

To achieve lightweight and miniaturized integration, the system adopts a modular stacked architecture based on ten-layer PCB technology, enabling the integration of 1024 channels while effectively suppressing interference. A dual power-supply chip-based power conversion design further reduces analog power noise, providing a stable platform for weak signal acquisition. However,

the system's battery life and high-frequency noise suppression capabilities remain areas for further improvement.

Future research will focus on the implementation of adaptive filtering algorithms, dynamic power management, motion artifact compensation, and enhanced compatibility with higher-density electrode arrays. The successful development of this system provides critical hardware support for investigating the dynamic coding mechanisms of neural populations and advancing neuroscience research. Ultimately, it paves the way for the clinical translation of brain–computer interface technologies.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Ethics Approval

All procedures were in accordance with the Animal Care and Use Committee of the Center for Excellence in Brain Science and Intelligence Technology, Chinese Academy of Sciences, Shanghai, China (NA-056-2023).

Author Contributions

All authors contributed equally to the study. They read and approved the final paper.

Mingfeng Liu: Writing – original draft (lead). **Xudong Guo:** Writing – review & editing (lead). **Liling Cao:** Software (equal). **Haipo Cui:** Project administration (equal). **Zihao Li:** Writing – original draft (supporting). **Yong Lin:** Software (equal). **Ziming Yin:** Software (equal). **Wentao Quan:** Methodology (equal). **Chengcong Feng:** Supervision (equal). **Tianyu Ma:** Validation (equal). **Zhengtuo Zhao:** Supervision (equal). **Liu Yang:** Supervision (equal). **Lei Yao:** Writing – review & editing (supporting). **Xuan Zhang:** Supervision (equal). **Gang Wang:** Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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