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Electronic properties of graphene/p-silicon Schottky junction

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Abstract

We fabricate graphene/p-Si heterojunctions and characterize their current–voltage properties in a wide temperature range. The devices exhibit Schottky diode behaviour with a modest rectification factor up to 10^2. The Schottky parameters are estimated in the framework of the thermionic emission theory using Cheung's and Norde's methods. At room temperature, we obtain an ideality factor of about 2.5 and a Schottky barrier height of $\sim$0.18 eV, which reduces at lower temperatures. We shed light on the physical mechanisms responsible for the low barrier, discussing the p-doping of graphene caused by the transfer process, the exposure to air and the out-diffusion of boron from the Si substrate. We finally propose a band model that fully explains the experimental current–voltage features, included a plateau observed in reverse current at low temperatures.

Keywords: Schottky junction, graphene, p-type silicon, diode, photoresponse, barrier height

(Some figures may appear in colour only in the online journal)

1. Introduction

Since its discovery, graphene has been the subject of great interest by the scientific community, to the point that it was thought it could replace traditional semiconductor materials in a new generation of electronic devices. Graphene is a bidimensional layer of carbon atoms arranged in a honeycomb lattice, that possesses gapless band structure and unique thermal [1], electrical and optical properties [2, 3]. It has very high electron mobility, ambipolar behaviour and can form low contact resistance with many metals [4–7]. For these reasons, it has been largely exploited to realize new faster electronic devices such as diodes or transistors [8–10]. Recently, much of the attention has been focused on the graphene/semiconductor junction, especially in the form of graphene/silicon (gr/Si), because it leads to diodes with several novel versatile functionalities [11, 12] and provides an excellent platform to study the physical phenomena occurring at the interface between a gapless 2D material and a 3D semiconductor. The gr/Si junction shows current–voltage characteristics similar to metal/semiconductor Schottky diodes and is well described by the thermionic emission theory modified by the modulation of the Schottky barrier caused by the low-density of states in graphene [13]. Moreover, the gr/Si junction has been demonstrated to be suitable for sensible and voltage tuneable two-terminals photodetectors [13, 14].

To date, most research activities and applications have been dealing with gr/n-Si junctions, while very limited investigations have been focused on graphene deposited on p-type silicon, caused by the difficulty in the realization of devices with good rectification and long-time stability. In fact, the p-doping of graphene, caused by the air exposure and the transfer process, moves the graphene Fermi level close to top level of the silicon valence band; on p-Si substrate, this condition is favourable to the formation of ohmic or low Schottky barrier contacts with limited rectification [13]. Chen *et al* fabricated gr/p-Si junctions using mechanically exfoliated graphene on low-doped substrates (10^{14}–10^{15} cm^{-3}) and observed a Schottky barrier of 0.44 eV at room temperature, reduced to 0.13 eV at 100 K [15]. They also observed that the

room temperature Schottky barrier slightly increased after vacuum annealing at 200 °C for 20 h, which they attributed to a change of the graphene doping from p to n-type. Indeed, the Schottky barrier height between graphene and the underlying silicon substrate can be modified by individually doping the graphene. An *et al* realized gr/p-Si junctions based photodetectors using chemical vapour deposition (CVD) grown graphene on medium-doped Si (10^{16} cm^{-3}) and measured a barrier height of 0.47 eV and a peak responsivity of 0.13 A W^{-1} [16]. They also studied the effect of interfacial native oxide layers and demonstrated that they strongly increase the ideality factor (~9) and suppress the reverse current.

In this paper, we investigate the electrical and optical properties of gr/p-Si junctions on low-doped substrates ($\sim 10^{15}$ cm^{-3}). A schematic of the device is shown in figure 1(a). Using CVD-grown graphene, we fabricate and study air exposed devices that show a 10^2 rectifying ratio. From current–voltage (*I–V*) versus temperature measurements we find that the ideality factor and the series resistance decrease for increasing temperature. The reverse dark current strongly increases with the bias, but exhibit a plateau at low temperatures which is caused by the Si band gap supressing the transport of majority carriers (holes). The limited rectification corresponds to low Schottky barrier height (SBH), ~0.18 eV, which is caused by the p-type doping of air-exposed graphene. This value is verified and confirmed by three different methods, giving a solid precedent in the electrical characterization of gr/p-Si junctions. Boron atoms from the Si substrate, which can diffuse in the graphene lattice at high temperature, can further contribute to the p-type doping of graphene and reduce the barrier height. Finally, experimental characterization of the device under illumination shows a photoresponsivity up to 2 A W^{-1}.

Our study provides important insights into the transport phenomena occurring at the gr/p-Si Schottky junctions.

2. Materials and methods

Starting from a lightly p-doped silicon substrate, with boron doping of 4.5 $\times 10^{14}$ cm^{-3}, a layer of ~50 nm of SiO_2 was deposited by CVD. In the next step, a 10 μm wide trench was patterned by photolithography, to remove the SiO_2 by hydrofluoric acid (HF), thereby revealing the Si substrate in the trench. Subsequently, a commercial CVD grown graphene layer of 1 × 0.4 cm^2 was transferred on the substrate.

The transfer process consists of several steps: It starts by spin-coating a graphene/Cu stack by PMMA (poly(methyl methacrylate)); after that, a solution of ammonium persulfate (20–50 mg ml^{-1} in water), iron(III) chloride (80–120 mg ml^{-1} in water), and a 2:1:1 solution of $H_2O/H_2SO_4/H_2O_2$ are used to wet etch the copper; then, the polymer/graphene stack is washed with distilled water several times in order to eliminate traces of the etch solution; finally, the gr/PMMA stack is transferred to the substrate, immersed in an acetone bath to remove the PMMA support and rinsed in isopropyl alcohol [17].

The ohmic contacts on the gr/Si device were realized by evaporating Ti/Au through a mask on the graphene and by depositing Ag paste on the exposed Si (trench), after properly scratching the surface. The current–voltage (*I–V*) characteristics were measured with the two-probe method using a Keithley 4200 Semiconductor Characterization System (4200-SCS) and a cryogenic Janis Probe Station at the controlled pressure of about 5 mbar.

3. Results and discussion

Figure 1(b) illustrates the *I–V* characteristics measured in the temperature range from 400 K to 180 K. In order to stabilize the thermal conditions, the electrical measurements were delayed by 20 min at each temperature step. The voltage was applied to the gr (anode) while the Si substrate (cathode) was grounded (we have reversed the voltage in figure 1(b) for convenience in the data analysis). Below 1 V, the forward as well as reverse currents increase exponentially with the applied voltage, although the reverse currents increase with about a half the rate. The device demonstrates rectification behaviour, with a modest rectification factor of few tens at ∓ 0.5 V, which increases to $\sim 10^2$ at lower temperatures ($\sim$200 K). The anomalous increase of the dark reverse current with the voltage has been widely studied and is associated with the modulation of the graphene Fermi energy by the applied anode–cathode voltage, which reduces the Schottky barrier for carrier injection from graphene to silicon [13, 16]. Remarkably, the device shows an unusual feature at low temperatures, which is the appearance of a plateau in the reverse current (figure 1(b)), which extends at higher reverse biases while reducing the temperature.

The forward-bias *I–V* characteristics can be described using the thermionic emission theory [10]:

$$I = I_0 \left(e^{\frac{qV}{nkT}} - 1 \right) \tag{1}$$

$$I_0 = AA^* T^2 e^{-\frac{q\phi_B}{kT}} \tag{2}$$

where I_0 is the saturation current at zero bias, q is the electron charge, n is the ideality factor, k is the Boltzmann constant, T is the temperature, A is the gr/Si junction area, A^* is the Richardson constant (≈ 32 A cm^{-2} K^{-2} for p-doped silicon) and $q\phi_B$ is the SBH. For $qV > nkT$, equation (1) can be rewritten as

$$\ln I = \ln I_0 + \frac{qV}{nkT} \tag{3}$$

which corresponds to a straight line whose intercept and slope can be used to extract the reverse current I_0 and the ideality factor. The ideality factor n is a phenomenological parameter related to the quality of the junction. A value greater than 1 indicates the presence of oxide patches, surface roughness or defects that cause inhomogeneity in the SBH and create deviations from the pure thermionic emission transport. We show in figure 1(c) the extracted behaviour of n versus T. At higher temperatures the ideality factor is smaller meaning that the thermionic emission is the main current transport process, while at lower temperatures the increasing values of n suggest

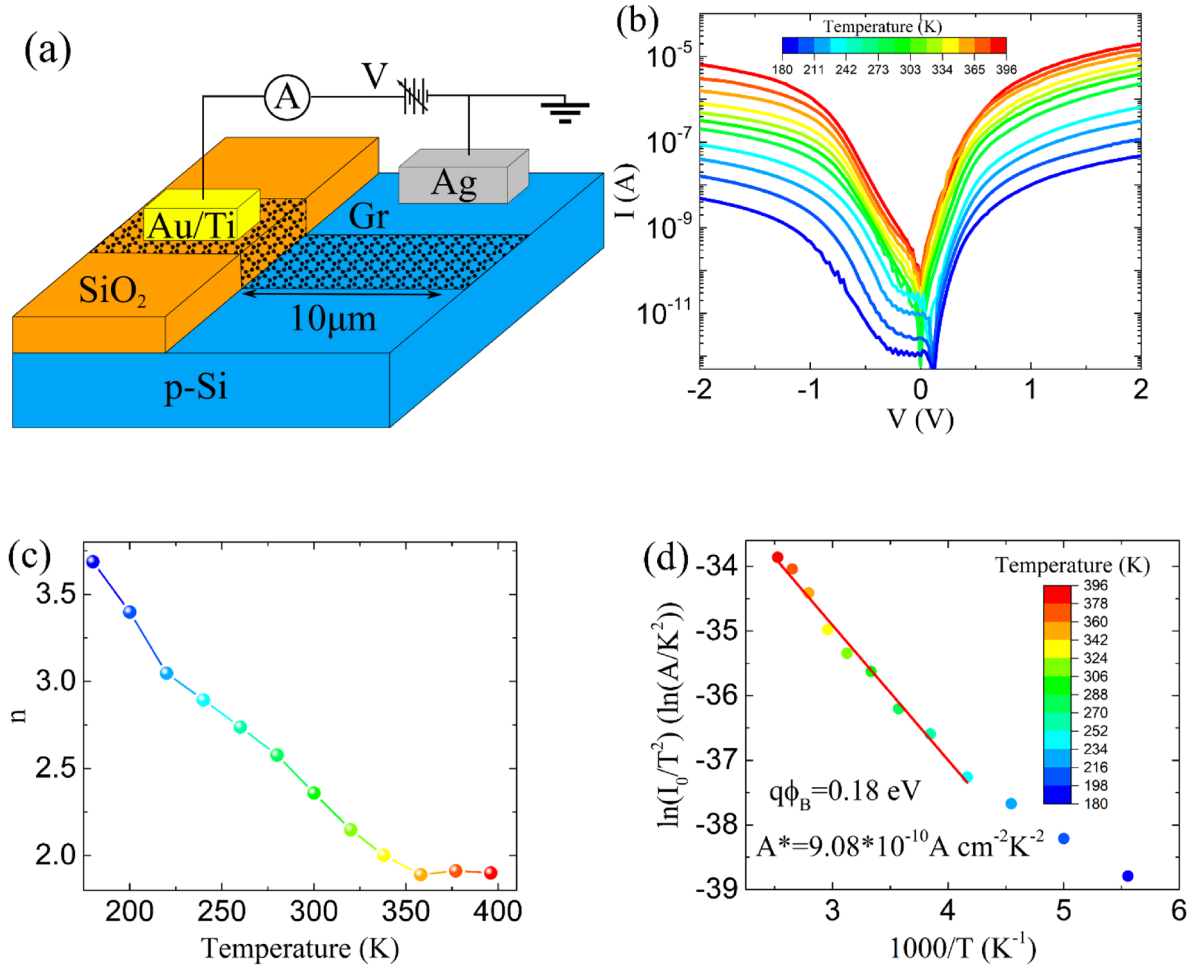

Figure 1. (a) 3D schematic view of the gr/p-Si device. (b) *I–V* characteristics of the gr/Si junction measured from 400 K to 180 K at 5 mbar. The voltage was applied to graphene (anode), while the Si substrate (cathode) was grounded; we have reversed the voltage in the figure for the convenience of the analysis. (c) Ideality factor versus temperature and (d) Richardson plot of $\ln\left(I_0/T^2\right)$ versus $10^3/T$. Some points have been excluded from the fit since significant deviation from thermionic behaviour usually occurs at low temperatures.

that other transport mechanisms, such as tunnelling, recombination and diffusion might be involved.

Rewriting equation (2) as

$$\ln\left(\frac{I_0}{T^2}\right) = \ln AA^* - \frac{q\phi_B}{kT}, \tag{4}$$

a linear behaviour is expected for the plot of $\ln\left(\frac{I_0}{T^2}\right)$ versus $\frac{1}{T}$, known as the Richardson plot. This is shown in figure 1(d), and is used to extract the SBH and the Richardson constant from the slope and the intercept, respectively. We obtained $q\phi_B = 0.18\,\text{eV}$ and $A^* = 9.08 \cdot 10^{-10}\,\text{A cm}^{-2}\,\text{K}^{-2}$. The points at lower temperatures are excluded from the fitting, since significant deviation from thermionic regime occurs at low temperatures. The low value of the Richardson constant can be explained by the presence of an insulator layer at gr/Si interface [18, 19]. Such dielectric layer introduces a tunnelling attenuation factor, $\exp\left(-\chi^{\frac{1}{2}}\delta\right)$, in equation (2) as:

$$I_0 = AA^* \exp\left(-\chi^{\frac{1}{2}}\delta\right) \exp\left(-\frac{q\phi_B}{kT}\right), \tag{5}$$

where χ is the mean barrier height, expressed in eV, and δ is the thickness, expressed in Å, of the insulating layer. A native SiO_2 layer can easily grow at the interface during the fabrication process in the time window between HF etch and/or during graphene transfer procedure. To consider the presence of an insulating interlayer, we can accordingly redefine the Richardson constant as:

$$A^{**} = A^* \exp\left(-\chi^{\frac{1}{2}}\delta\right) \tag{6}$$

where $\chi \approx 3\,\text{eV}$ for SiO_2. Using for A^{**} the value extracted from the Richardson plot, we can estimate a thickness of the insulating layer $\delta \sim 16$ Å. The presence of an oxide layer of the estimated thickness at the gr/Si interface is confirmed by the x-ray photoemission spectra, shown in figure 2, which compares Si trench regions covered and uncovered by graphene.

At high forward or reverse bias, $|V| > 1\,\text{V}$, the *I–V* characteristics are dominated by a series resistance, R_S, that can be extracted using Cheung's method, which also constitute an alternative approach to estimate the SBH [20]. By taking

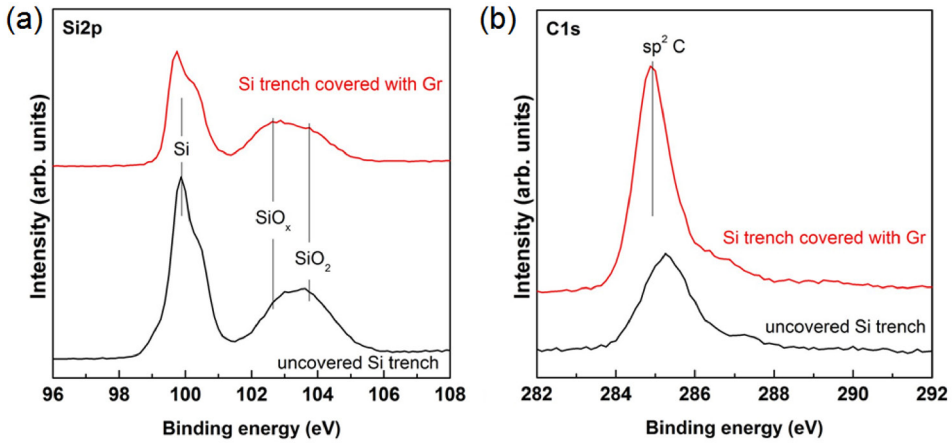

Figure 2. Si 2p (a) and C 1s (b) x-ray photoelectron spectra acquired on graphene-covered Si trench and on uncovered Si trench. Exposure to ambient conditions causes oxidation of the Si junction areas underneath Gr where mostly Si sub-oxides are formed (SiO_x, $x < 2$). On the uncovered areas Si oxidizes mostly to SiO_2.

into account the voltage drops caused by the series resistance, equation (1) can be rewritten as

$$I = I_0 \exp\left(\frac{q\,(V - IR_S)}{nkT} - 1\right). \tag{7}$$

In forward bias, for $V - IR_S > nkT/q$, equation (7) becomes

$$I = I_0 \exp\left(\frac{q\,(V - IR_S)}{nkT}\right) \tag{8}$$

from which two equations can be derived

$$\frac{dV}{d\ln(I)} = IR_S + n\left(\frac{kT}{q}\right) \tag{9}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{**}T^2}\right) \tag{10}$$

where $H(I)$ is defined as

$$H(I) = IR_S + n\phi_B. \tag{11}$$

From the intercept and the slope of the linear plot (equation (9)), we can estimate n and R_S, as shown in figure 3(a), and in turn we can calculate $H(I)$ using equation (10) for the experimental I–V data. $H(I)$ versus I plot is shown in figure 3(b). We extract then the series resistance and the SBH using the slope and the intercept of the fitting straight line. We obtain $q\phi_B = 0.17\,\text{eV}$ and a series resistance $\sim 500\,\text{k}\Omega$ at room temperature. The value of $q\phi_B$ is consistent with that estimated previously from the Richardson plot. Cheung's method can be iterated at every measurement temperature. Figure 3(c) shows the temperature dependence of the SBH and the ideality factor so obtained. The Schottky barrier height increases with temperature and reaches a maximum value around 270 K, after which it becomes temperature insensitive. The decrease of the SBH with decreasing temperature is an indication of spatial inhomogeneity of the graphene/Si junction, the SBH presenting peaks and valleys [21, 22]. At higher temperature, the carriers possess enough energy to overcome the SBH peaks, while at lower temperature they are forced to pass through the valleys and a lower SBH is measured. Similarly, the larger values of n with decreasing temperature indicates that transport mechanisms other than thermionic emission might become relevant at lower temperatures [22].

Figure 3(d) shows that the series resistance decreases exponentially with the temperature. A decreasing resistance with raising temperature is typical for a semiconductor. However, we attribute the strong decrease of the resistance mainly to the graphene layer, since the Si resistivity does not change that much within the measured temperature range [23]. The negative temperature-dependence of the resistivity of graphene is caused by thermal generation of the electron–hole pairs and carrier scattering by acoustic phonons [24, 25].

Further on, another way to determinate the Schottky diode parameters is to use the modified Norde's method [26, 27]. This method is based on the auxiliary function

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{*}T^2}\right) \tag{12}$$

where γ is an arbitrary constant greater than the ideality factor. The SBH and series resistance can be determined as

$$q\phi_B = F(V_{min}) + \frac{\gamma - n}{n}\left(\frac{V_{min}}{\gamma} - \frac{kT}{q}\right) \tag{13}$$

$$R_s = \frac{(\gamma - n)\,kT}{qI_{min}} \tag{14}$$

where $F(V_{min})$ and V_{min} are the coordinates of the minimum point in the plot $F(V)$ versus V (displayed in figure 4(a) for different γ values), I_{min} is the current value at the voltage V_{min}, n is the ideality factor.

The accuracy of this method is strictly related to the independence from the parameter γ. Figure 4(b) displays the SBH and the series resistance, obtained from equation (14) with the ideality factor used for equations (3)–(9), and shows that the extracted value is independent of γ. Norde's method provides a SBH, $q\phi_B = 0.17\,\text{eV}$ and a series resistance $R_S \sim 600\,\text{k}\Omega$ at room temperature, consistent with the ones extracted using the other two methods.

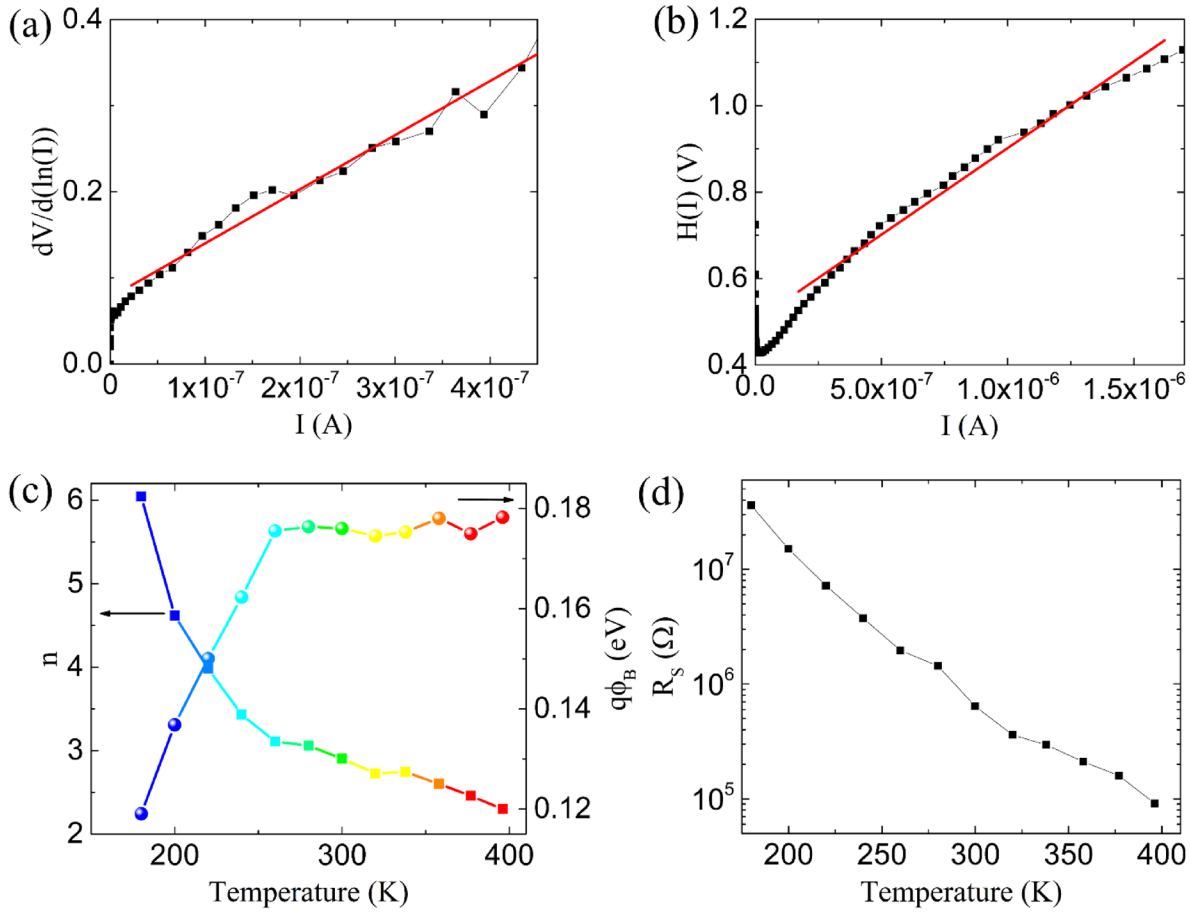

Figure 3. Cheung's plot of (a) dV/dln(I) versus I and (b) $H(I)$ versus I at 300 K. (c) Ideality factor and Schottky barrier height and (d) device series resistance versus temperature extracted from Cheung's method for $|V| > 1$ V.

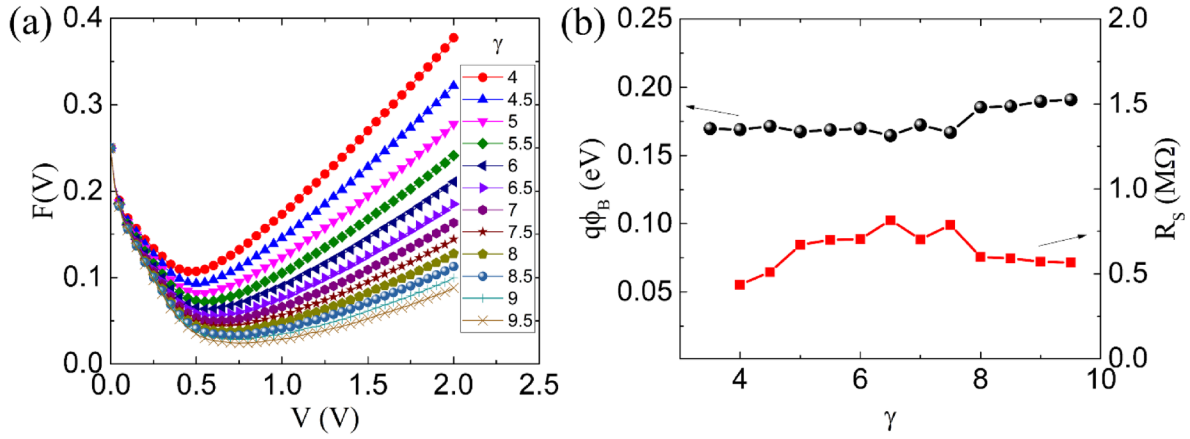

Figure 4. Modified Norde's method (a) $F(V)$ versus V plot for different values of γ, (b) the SBH (black circle) and the series resistance R_S (red square) computed from the Norde's method.

Three different methods, namely Richardson's, Cheung's and Norde's, have consistently showed SBH and R_S values, as summarized in table 1. The low SBH is due to the well-known p-type doping of graphene. Many causes have been reported to contribute to the p-doping of graphene. The transfer of the graphene process, as described before, involves the use of PMMA and chemicals, which can leave residues on the graphene sheet, thereby resulting in p-type doping [28]. Air

Table 1. Gr/p-Si Schottky barrier parameters at room temperature extracted by Richardson's, Chueng's and Norde's methods.

Method	n	$q\phi_B$(eV)	R_s(kΩ)
Richardson's	2.5	0.18	—
Cheung's	2.9	0.17	500
Norde's	—	0.17	600

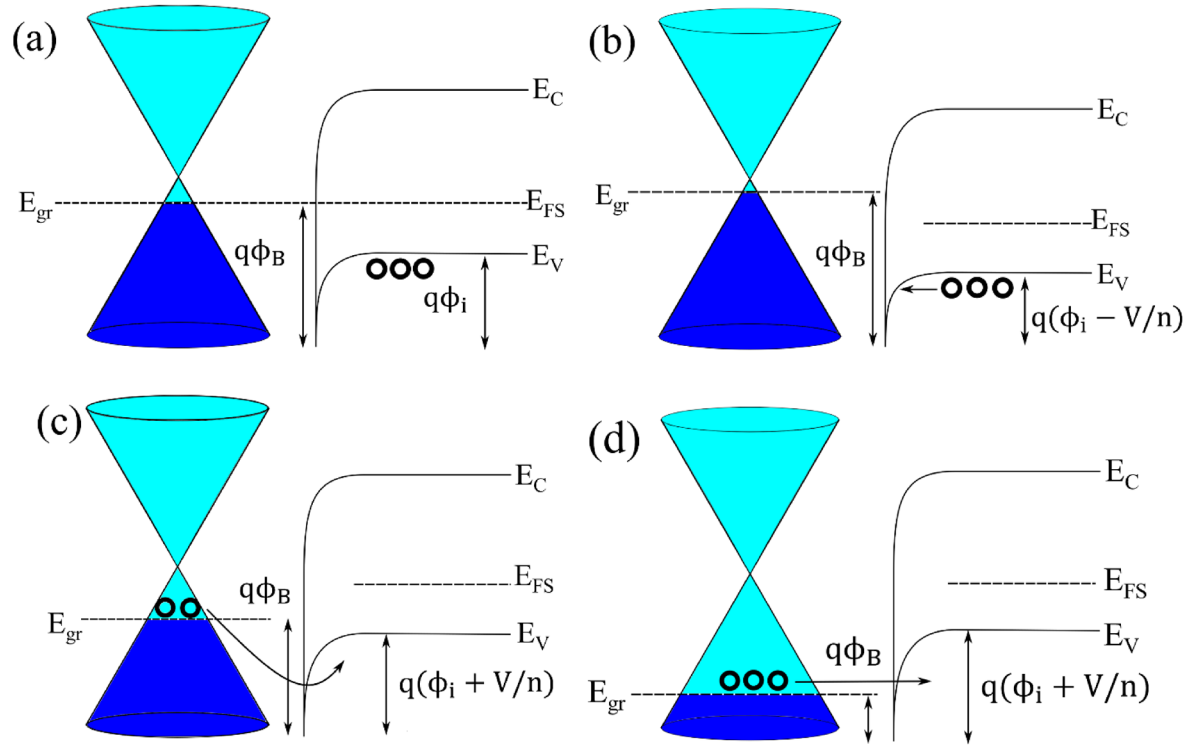

Figure 5. Band diagram of the gr/Si heterojunction, with symbols having the usual meaning, in (a) unbiased condition, (b) forward bias and reverse bias with (c) lower and (d) higher applied voltage. Charge carriers (holes) are shown as open circles. The interfacial tunnelling oxide layer is not shown for simplicity.

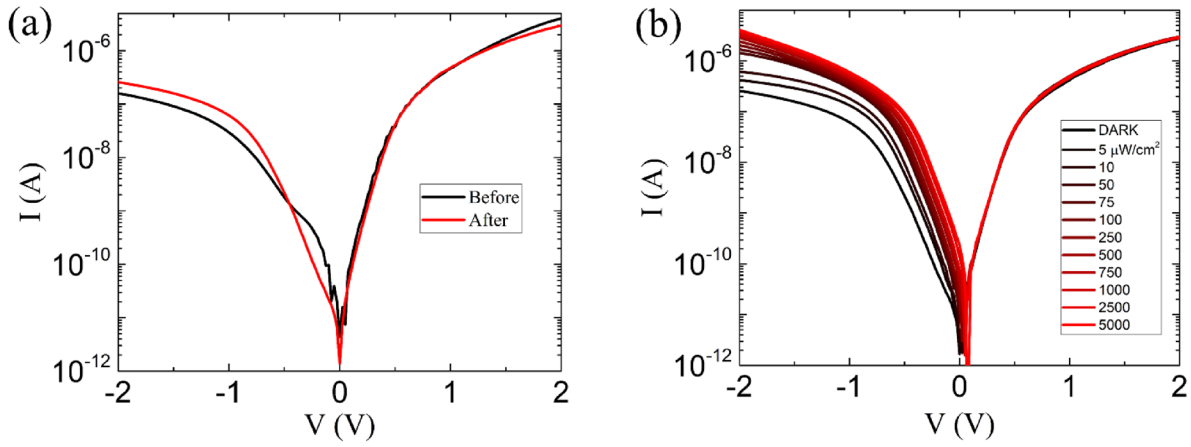

Figure 6. (a) Room-temperature *I–V* characteristics of the device measured before and after the temperature ramp up. (b) *I–V* characteristics of the gr/Si junction under different illumination levels from a white LED array.

exposure is a well-known cause of graphene p-doping [5]. An additional source can be the boron diffusion from the substrate into the graphene layer during the temperature ramp up, as we will discuss in the following.

To explain the observed *I–V–T* behaviour we propose the band model shown in figure 5. The band alignment in unbiased condition is pictured in figure 5(a), showing graphene and Si lightly p-doped. In forward bias, i.e. for a negative voltage applied to the graphene contact with respect to Si, the Fermi level of graphene (E_{gr}) is raised with respect to the Si Fermi energy (E_{FS}), causing the barrier height ($q\phi_i$) for holes moving from Si to graphene to be reduced by the amount qV/n (where V is the applied voltage and n the ideality factor), as shown in figure 5(b). Furthermore, due to the low density of states of graphene, the Fermi level of graphene is up-shifted with respect to the double cone, that is graphene becomes less p-doped, since there is reduced negative space-charge at the Si interface to mirror in graphene. This condition results in increased SBH, $q\phi_B$, as shown in figure 5(b). In reverse bias, which is for positive voltage on graphene, the Fermi level of graphene is lowered with respect to that of Si. The graphene Fermi level is down-shifted along the double cone, because the p-doping of graphene increases to counterbalance the augmented negative space-charge in Si. This situation corresponds to a decreasing SBH, as shown in figures 5(c) and (d) for raising reverse bias at low and high voltages, respectively.

The decreasing SBH due to bias (likely contributed also by image force barrier lowering [29], here not explicitly pictured) is the cause of the exponentially increasing reverse current, as reported also elsewhere [13, 16, 29–32]. The Si bandgap suppresses the injection of holes from graphene until the reverse bias aligns E_{gr} with the upper level of the Si valence band (E_V), as shown in figure 5(c). However, the suppression of current, which manifests itself as a plateau in the reverse *I–V* characteristics, becomes evident only at lower temperatures, when the Fermi distribution function becomes more step-like and the Fermi window for conduction is reduced.

Otherwise stated, at lower temperatures, the current due to hot holes (with energy below E_{gr}) is negligible and very low current is detected until the reach of the $E_{gr} - E_V$ alignment condition. After that, energy states become available in Si, and injection of holes from graphene can take place, thus originating the observed high reverse current.

Figure 6(a) shows a comparison of the *I–V* characteristics measured at room temperature before and after the high temperature ramp up to 400 K. The *I–V* characteristic of the as-produced device presents at room temperature a small knee in reverse bias down to ~ -0.4 V (black line in figure 6(a)), which disappears after the device is subjected to the high temperature measurement cycle. This feature is more evident as plateau at low temperature, as previously shown in figure 1(b). Referring to the band model of figure 5, the disappearance of the plateau suggests that the p-doping of graphene has increased after the high temperature annealing (made before the temperature ramp down) favouring the E_{gr} to Si E_V upper-level alignment condition (figure 5(d)). Since the device was kept in the probe-station chamber at constant pressure during the *I–V–T* measurements, the temperature annealing treatment is likely the main cause of this extra doping. Indeed, a recent study has demonstrated that p-doping of graphene on boron-doped Si substrates occurs after a 3 h annealing at the temperature of 400 K, by incorporation of B or Si atoms in graphene vacancy sites [33]. This process likely took place in our device, which was subjected to similar annealing conditions. This extra doping can explain the slightly lower gr/p-Si SBH measured in the present work compared to other studies [15, 16] and why the reverse curve of the device shows a clear plateau only at the lowest temperatures.

Finally, figure 6(b) shows the current voltage characteristics of the device under different illumination levels by a white LED system, measured at room temperature and 5 mbar. A photocurrent appears only in reverse bias, thus confirming the Schottky behaviour of the junction. At the reverse bias of 0.5 V and with the incident optical power $P_{opt} = 5\,\mathrm{mW\,cm^{-2}}$, the device exhibits a responsivity $R = \frac{(I_{ph} - I_{dark})}{P_{opt} \cdot S} \approx 0.05\,\mathrm{A\,W^{-1}}$ (I_{ph} and I_{dark} are the currents in dark and under illumination, S is the gr/p-Si junction surface). At higher voltages the responsivity increases until reaching the value of $2\,\mathrm{A\,W^{-1}}$ at -2 V. Despite the good responsivity the use of the device as photodetector is hindered by the high dark current which results in high power consumption and reduced sensitivity to low intensity radiation.

We remark that the reverse current of the device increases with increasing light intensity up to almost exceeding the forward current. Such behaviour in gr/Si junctions has been already discussed [30–32, 34]. The parasitic gr/SiO_2/Si MOS (metal oxide semiconductor) capacitor, which is in parallel with the gr/Si Schottky diode, acts as a reservoir of photogenerated minority carriers which accumulate at the Si/SiO_2 interface under reverse bias. These photon-induced charges diffuse to gr/Si junction region and greatly enhances the reverse current.

4. Conclusions

In conclusion, we have studied the electrical and optical properties of the gr/p-Si heterojunction and consistently estimated the relevant Schottky parameters by several methods. The gr/p-Si diode showed a rectifying ratio up to 10^2, an ideality factor of ~2.5, a SBH of ~0.18 eV and a responsivity up to $2\,\mathrm{A\,W^{-1}}$. We have explained the origin of low Schottky barrier height by p-doping of graphene caused by the transfer method, exposure to air and by incorporation of B or Si heteroatoms into the graphene at high temperature. We have proposed a model to explain the observed *I–V* characteristic, including the appearance of a plateau in reverse current at low temperatures.

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