APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

High aspect ratio silicon etch: A review

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(Received 4 November 2009; accepted 12 July 2010; published online 9 September 2010; corrected 10 September 2010)

High aspect ratio (HAR) silicon etch is reviewed, including commonly used terms, history, main applications, different technological methods, critical challenges, and main theories of the technologies. Chronologically, HAR silicon etch has been conducted using wet etch in solution, reactive ion etch (RIE) in low density plasma, single-step etch at cryogenic conditions in inductively coupled plasma (ICP) combined with RIE, time-multiplexed deep silicon etch in ICP-RIE configuration reactor, and single-step etch in high density plasma at room or near room temperature. Key specifications are HAR, high etch rate, good trench sidewall profile with smooth surface, low aspect ratio dependent etch, and low etch loading effects. Till now, time-multiplexed etch process is a popular industrial practice but the intrinsic scalloped profile of a time-multiplexed etch process, resulting from alternating between passivation and etch, poses a challenge. Previously, HAR silicon etch was an application associated primarily with microelectromechanical systems. In recent years, through-silicon-via (TSV) etch applications for three-dimensional integrated circuit stacking technology has spurred research and development of this enabling technology. This potential large scale application requires HAR etch with high and stable throughput, controllable profile and surface properties, and low costs. © *2010 American Institute of Physics*. [doi:10.1063/1.3474652]

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I. INTRODUCTION TO HIGH ASPECT RATIO SILICON ETCH

High aspect ratio (HAR) silicon etch is also known as deep silicon etch, deep trench silicon etch, silicon deep reactive ion etch, and HAR trench silicon etch.

Since the invention of the integrated circuit (IC) in 1958, silicon etching has been an important technology for the semiconductor industry. Early on, silicon etch meant mainly isotropic wet etch. From the late 1960s, anisotropic silicon etch became an important technology in silicon semiconductor processing.[1] Based on process methods, HAR silicon etching can be divided into two categories, i.e., wet etch and plasma etch. Other potential technologies for HAR silicon processing include laser drilling,[2] and ultrasonic drilling.[3]

A. Wet etch

In the 1960s, silicon etch was found to be orientation-dependent and concentration-dependent in some chemical solutions.[1,4–8] Silicon used in semiconductors has a single-crystal structure and exhibits different etch rates for individual crystal orientation. When aqueous KOH solution is used for wet etch, etch rates vary for different planes. Etch rates on planes of {111}, {100}, and {110} have been obtained through many studies.[1,8–11] Silicon etch rates at {111} surface

is significantly slower than those on {110} and {100} surfaces under suitable chemical compositions. For example, the etch rate on {110} surface can be several hundred times of the etch rate on {111} surface. A rectangular groove with vertical sidewalls and an aspect ratio of several hundred to one can thus be etched on {110} surface using a suitable mask. Although this phenomenon is well documented, the underlying mechanism has not been widely explored.

Crystal surface properties determine the difference in surface density of silicon bonds, bonding energy of silicon atoms, and interstitial space on the interface between silicon and silica. These properties influence oxidation rates on each crystal plane. Both oxidation and etch rates on {111} are slower than {110}. The oxidation occurs at the interface between silicon and its oxide, which involves interstitial water molecules in the silica film and silicon at the interface. The high silicon bond density on {111} surface results in a dense oxide in this surface and, therefore, makes the oxidation and etch slower than surface {110} and {100} but the etch on {110} and {100} can continue owing to the low density oxide.

Silicon etch is not a diffusion-limited reaction but an activation-limited one. When silicon is immersed in a KOH solution with an oxidizing agent, silicon oxidation and etch back occur simultaneously. The apparent etch rate results from the difference between the etch and oxidation reaction rates. This makes the apparent etch rates on different surfaces (e.g., {110, 100, and 111}) significantly different. It as reported that a dense oxide layer was immediately formed on the {111} surface upon immersion in the liquid.[8]

Even though orientation-dependent silicon etch can have an aspect ratio as high as 600, this deep etch technique is inherently limited to the fabrication of structures such as deep grooves. This fundamentally limits the applications of this technique.

B. Plasma etch

Plasma etch is a gas-solid chemical reaction that takes place in the presence of a plasma, an electrically neutral mixture of molecules, atoms, ions, electrons, and photons.

To create a stable environment, energy must be coupled into the plasma to sustain the ionization. Electrons are very light particles in plasma. When the same force (e.g., the electric force in an electric field) acts on an electron and a much heavier ion, the resulting speed is considerably different. The result is that the speed of the electron will be much higher than that of the ion. If the collisions are not numerous enough at low density conditions, i.e., low pressure, the mean kinetic energy, or temperature of the electrons will be higher than that of the much heavier ions.

In the boundary area of plasma between the bulk plasma and a solid surface, known as the sheath, the properties and charges are different from the plasma's bulk region, mainly due to the mobility difference between the negative charged electrons and the positively charged ions noted above. The electrons accumulate near the solid surfaces, which results in the existence of a neutral bulk plasma and non-neutral plasma near the wall in the sheath. In the low pressure plasma conditions used for HAR etching, the mean free path of the electrons is much longer than the sheath thickness, hence the sheath can be treated as a collisionless region.

The potential drop across the sheath is a function of the relative masses of electrons and ions, electron temperatures, and reactor chamber design. The result is that the ions have an accelerating voltage across the plasma sheath, enabling an anisotropic etch mechanism. When a dc voltage or a capacitively driven radio frequency voltage is applied to a surface (cathode), the potential drop across the plasma sheath is enhanced and made adjustable.

The potential drop across the sheath, approximately equal to dc bias, is one of the most important characteristics of plasma etching. It supplies anisotropic bombardment energy, which significantly reduces the undercut compared with wet etching. This important effect results from the anisotropic energy of supply to the etch surface. The reactive but electrically neutral radicals are not accelerated toward the etch surface by the dc bias. The electrically-charged ions are accelerated toward the etch surface by the dc bias and this ion bombardment creates an anisotropic etch mechanism.

C. Etch and passivation

It is extremely difficult to obtain a good quality HAR silicon trench only relying on anisotropic bombardment supplied by plasma environment. That means passivation on trench sidewall to control lateral etch is a necessary approach, which can be carried out simultaneously with etch in one step or separately in an individual passivation step.

One successful process using trench sidewall passivation is cryogenic etch process proposed in 1988.[12] One advantage of cryogenic etch is relatively high selectivity owing to the relative low photoresist (PR) etch rate. Etch rates of 500–1000 nm/min were reported with reactive ion etch (RIE) and microwave plasma etching. The etch temperature range was (−130)–(−100) °C, with pressure of about 10 mTorr.[13] To ensure low wafer temperature, liquid nitrogen or helium was placed in direct contact with the wafer, which required with an excellent seal.[13,14] Cryogenic plasma etch relies on lowering temperatures during plasma treatment to yield less sidewall etching and increasing the dry etch resistance of organic PR masks and hence increases selectivity.[12] To prevent cracking from the low temperature, the PR is generally hard-baked before etching.[13]

Cryogenic plasma etch was the first practical etch technique for aspect ratios up to 30:1. The technique successfully balances bottom and sidewall etch rates to give the desired sidewall angle. Plasma etch under cryogenic conditions is primarily a chemical reaction. Molecules and atoms absorb plasma energy and dissociate to form ions and very reactive neutral radicals. In a fluorine-based chemical system, the fluorine atom is believed to be the radical responsible for the silicon etch.

The cryogenic process uses SF_6 and O_2 to form a protective, 10–20 nm, layer of oxide–fluoride compound (SiO_xF_y) to suppress on the sidewall etching while simultaneously enhancing the bottom etch rate by ion bombardment.[13] The low temperature reduces erosion of the

protective sidewall layer. However, obtaining a straight sidewall for aspect ratios beyond 30:1 is difficult using cryogenic etch.

In order to obtain the necessary anisotropy, attempts were made to avoid lateral etching by coating the sidewalls with a polymer film formed from the etch gases.[15] However, ceramic materials were also deposited on the wafer inadvertently by the erosion of the chamber wall around the cathode.[16] This material tended to be deposited only near the aperture of the feature, about 3 μm from the trench opening, while sidewall protection near the bottom of the feature relied only on the decomposition of carbon-containing chemicals.[16] The resulting trench profile suffered from irregular and rough sidewalls, which were unsatisfactory. For example, when used for MEMS applications, it made mold release difficult and induced unwanted friction in mechanical structures such as axles.

Time-multiplexed alternating process is a common method which very successfully uses passivation for HAR silicon etch by alternating sidewall passivation and etch steps. Because of its capability for HAR feature fabrication, this approach becomes a popular technology in HAR silicon etch. More details about this method will be discussed in the following sections.

Simultaneous passivation and etch at room or near room temperature are also applied on single step HAR silicon etch process using chemicals similar with those used in cryogenic process. It is challenge to control this passivation and keep balance between lateral and vertical etch rates.

D. Microelectromechanical systems (MEMS)

For MEMS and through-silicon-via (TSV) etch applications, the required trench depth has a wide range, from a few to several hundred micrometers, which is much deeper than those found in IC wafer processing.[13,17]

In the 1980s, many studies were performed to explore the use of deep silicon etch for MEMS micromachining,[12,16,18] and volume manufacturing began in the 1990s. Before the mid-1990s, etch for both semiconductor films and micromachining was mainly limited to films of only a few micrometers in thickness. In MEMS, this is known as "surface" micromachining.

MEMS development spurred research into plasma etch deep into the bulk silicon, i.e., deep silicon etch, to enable the fabrication of piezoresistive pressure and acceleration sensors, microvalves, and micropumps, and implantable neural probes and stimulators.[19] At that time, the basic requirements for deep silicon etch were high etch rate (3 μm/min), HAR (30 or higher), and high etch rate selectivity between silicon and the mask material such as PR.[20]

This intensive MEMS development resulted in significant progress being made in silicon deep trench etch in the mid-1990s. Applications proliferated, including silicon molds,[21,22] silicon pillars,[23] ridges, optical gratings,[24–26] attenuators,[27] Fresnel lenses,[28] silicon nanopillar arrays (Fig. 5) for biotechnology applications,[29] microturbines,[30,31] accelerometers,[32,33] acoustic filters,[34] and gyroscopes,[35,36] as well as complementary metal-oxide semiconductor (CMOS)-based microphones (late 1990s). For more information on secondary effects and issues in HAR etch for MEMS applications, see Refs. 37–40.

E. TSVs

The development of TSV structures, where two or more chips are joined by vertical interconnects running through the stack has resulted in further intensive studies into deep silicon etch.[41] TSV etch makes the via holes for connecting the vertically stacked chips. Although etching completely through the substrate is not required because a thinning step is used during the packaging process, an etch depth of more than 100 μm is necessary. For cost reasons, TSV etch requires high etch rate to enable high throughput, and smooth sidewalls to ensure the optimal fill of conducting materials in subsequent processing. These requirements make deep silicon etch for TSV very challenging.

The use of TSVs for stacked-chip applications has a large potential market. It was estimated that three-dimensional (3D) packaging is equivalent to two generations of lateral feature size shrinking.[42] When TSV etch occurs before the fabrication of active circuit features such as transistors, the process is called "via-first." Conversely, it is called "via-last" if the TSV is etched after the active features are complete. Obviously, the via-last process will etch through not only silicon but also all the layers deposited during prior wafer processing.

After the via is etched, the hole is typically lined with a dielectric "sleeve" (e.g., SiO_2), deposited by chemical-vapor deposition (CVD), and then filled with electroplated copper or tungsten.[43]

The first high volume application of TSVs was the production of CMOS image sensors using a via-last approach. After fabrication of the sensor array, the wafer is thinned using a grinding process, inverted bonded to a glass carrier. The contacts are then formed from the backside. TSVs are predicted to be in use for stacked chips by 2010.[44]

TSVs typically are large features, with diameters 1–50 μm and depths up to 150 μm with aspect ratios up to 15:1 depending on the application and integration scheme.

F. HAR small features for IC fabrications

The requirement for a deep silicon etch for silicon diode array fabrication was reported in the early 1970s.[45,46] Later, plasma deep silicon etch was used for capacitors and isolation.[47–50] This early deep silicon etch was for making deep holes and trenches in silicon substrates to enhance charge storage in dynamic random access memory (DRAM),[51–53] and for HAR α-Si gate etch.[54]

In 2006, a very small feature with HAR (11 nm wide and 87 nm high) was etched to form a silicon fin for a multiple gate field effect transistor (MuGFET, also called FinFET) device.[55] This extremely small feature HAR silicon etch shows the potential applications in this promising technology. Other example is for fabrication of shallow trench isolation features between metal-oxide-semiconductor field-effect transistor (MOSFET) transistors or DRAM cells which can be more than 15 μm deep and 100–600 nm wide.[56]

G. Challenges of HAR silicon etch

The success of HAR silicon etch depends on controlling the lateral etch rate and enhancing the vertical etch rate. Controlling the etch rates in these two directions relies on the ion incidence angle distribution and the dependence of the silicon and passivation layer etch rates upon the ion angle. Ideally, the vertical bombardment energy should be high enough to achieve the desired vertical etch rate, while the lateral bombardment component should not be strong enough to significantly etch through the passivation layer and allow lateral etching.

The key challenges of deep silicon etch are to achieve HAR with smooth, usually vertical, sidewall profiles, obtain high etch rate and selectivity, and control loading effects, aspect ratio dependent etching (ARDE), micrograss, tilting, and notching. Each of these aspects will be discussed in the following sections.

II. TIME-MULTIPLEXED ALTERNATING PROCESS

The time-multiplexed alternating process for HAR silicon etch, which alternates etching and polymerization steps, was invented by Laemer and Schilp. The patent was assigned to Robert Bosch GmbH in 1996, so it is also known as the Bosch method.[57] The time-multiplexed process allowed a much higher aspect ratio to be obtained with very high etch selectivity. Since this method was first proposed, many modified versions have been studied.[58–62] The original etch gas was SF_6 and polymerization gases were CHF_3 and Ar. Other etch gases included NF_3 and CF_4. The passivation mechanism is not limited to polymer deposition; oxygen and hydrogen have been reported for this purpose.[56,63] The time-multiplexed etch process has proven popular for HAR trenches in MEMS and TSV applications.

Each polymerization step is followed by an etch step which rapidly removes the polymer layer on the bottom of the feature while partially removing the polymer layer on the sidewall (Fig. 1).[64] The partial polymer removal protects the sidewall. Etch and passivation steps are alternated until the desired etch depth is reached. The polymer is teflonlike and approximately 50 nm is deposited on the sidewall and base. Although etch and polymerization are performed alternately, there is a gas flow overlap due to the gas residence time in the etch chamber. This phenomena makes it possible to operate the time-multiplexed method with continuous flows of SF_6 and C_4F_8 by reducing the durations of each step.[65] Continuous gas flow reduces the sidewall "scallop" profiles that tend to form as a result of the alternating etch and passivation steps.

The original time-multiplexed etch process typically used SF_6 gas flow rate of up to 100 SCCM (SCCM denotes cubic centimeter per minute at STP), a chamber pressure of 1–10 mTorr, microwave power for plasma generation of 300–1200 W and 3–5 W bias power applied to the cathode. Later, C_4F_8 replaced CHF_3 as a passivation gas for better passivation performance and inductively coupled plasma (ICP) was widely used instead of microwave plasma.

For the time-multiplexed process, the balance of etch and passivation is critical to achieving anisotropic etch and process stability, and can be adjusted by either the etch or the polymerization process. For a fixed etch step, the overall etch rate is a function of the polymer step, depending on C_4F_8 flow rate and polymerization step, or pulsing, time (Fig. 2).[20] It can be seen in Fig. 2(a) that the overall etch rate drops with an increase in C_4F_8 flow rate but above the optimal condition (circled), the etch rate drops sharply, i.e., the optimum flow rate is where the maximum anisotropic etch rate with stable polymerization is achieved. When the C_4F_8 flow rate is higher than the optimal condition, the etch pulse is not long enough to penetrate the bottom polymer. Below the optimal

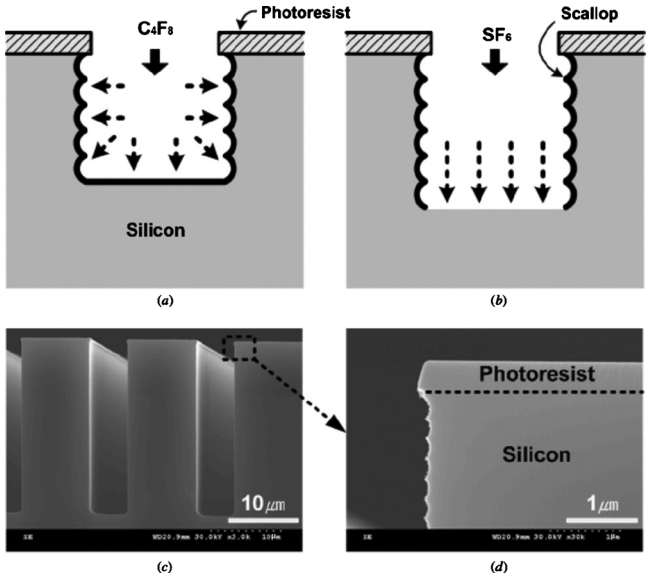

FIG. 1. Schematic of Bosch method. (a) Sidewall passivation using C_4F_8, (b) silicon isotropic etching using SF_6 gas, (c) SEM image of deep trenches, (d) magnified SEM image of the sidewall with nanoscallops.

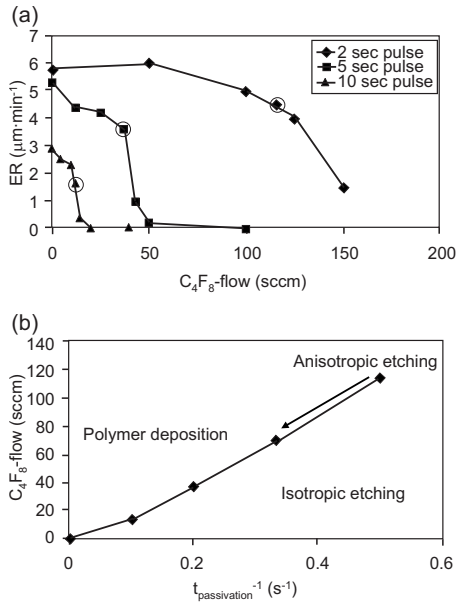

FIG. 2. Etch rate as a function of the C_4F_8 flow for several passivation pulse times at a given etching pulse (a) at the encircled points the profile is anisotropic and the etch rate goes down. These points have been drawn in a C_4F_8 flow vs inverse passivation pulse time plot (b). It gives a linear relation dividing regimes of isotropic etching and polymer deposition. At the boundary of these regimes, etching is anisotropic.

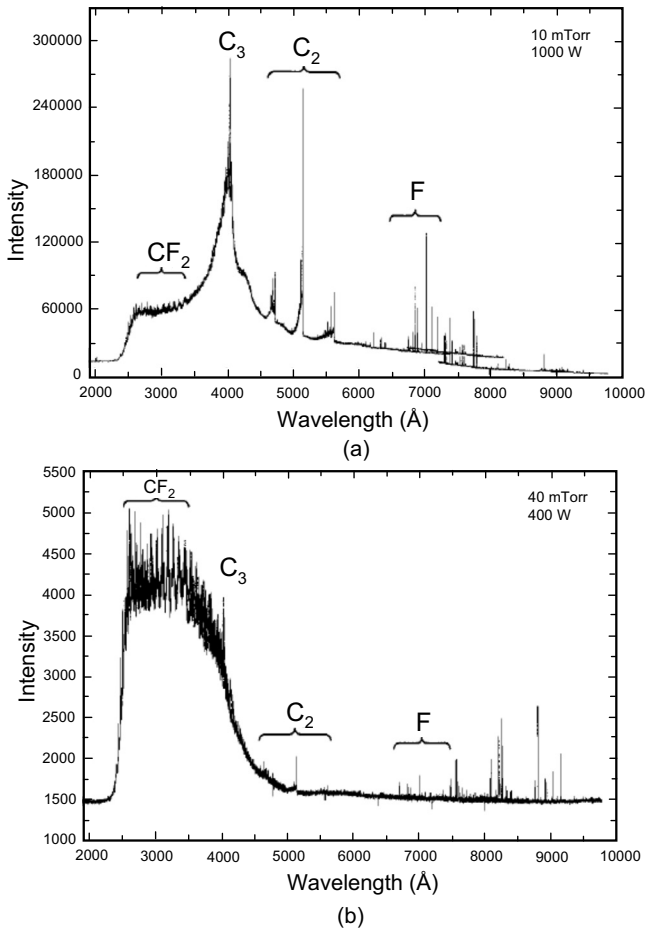

FIG. 3. OES results during C_4F_8 polymerization, (a) low pressure and high power plasma and (b) high pressure and low power plasma.

condition, the sidewall polymer is also completely etched through and isotropic etch results. Two regions on the plot of C_4F_8 flow rate versus pulse frequency are identified [Fig. 2(b)]. These two regions are the polymer deposition region and isotropic region. Along the dividing line between these two regions, anisotropic etch is achieved. The narrowness of this region means process stability is difficult to achieve for the time-multiplexed etch process, i.e., the "process window" is narrow.

Polymerization rate and polymer etch resistance are important parameters because they influence the overall etch rate and profile. However, polymers are not a single stoichiometric compound but a mixture of organic chemicals. It was reported that two polymer film composition regimes were found, one of which has a high fluorine-to-carbon ratio (F/C=1.6) occurs at low pressure and high rf power. The other regime has a low ratio (F/C=1.2) at high pressure and low rf power process conditions.[66] Optical emission spectroscopy (OES) results (Fig. 3) indicate a high content of C_3, C_2, and F in the plasma which corresponds to a high F/C ratio in the deposited film, while a low F/C ratio in film (poor CF_2) corresponds a high content of CF_2 in plasma.[66] This means that CF_2-rich plasma produces CF_2-poor film. The optimal F/C ratio for this study is 1.45 to give the best balance between deposition rate and etch resistance.

Polymer etch resistance is critical to overall etch rate and selectivity. It was found that a low F/C ratio film is more etch resistant than one with a high ratios.[66] However, the etch-to-deposition rate of a low F/C film is undesirably high during the deposition step. A low etch-to-deposition rate in the deposition step is preferred during process optimization even though it corresponds to a low etch resistance in the etch step to maximize the overall etch rate.

The main advantages of the time-multiplexed etch process are the controllable and stable profile; high etch selectivity; high etch rate; and HAR. Disadvantages include the scallop-shape profile resulting from the alternating etch and polymerization processes, and micrograss.

Table I shows a range of published time-multiplexed silicon etch process conditions and results. The table indicates a variety of process conditions which exhibit a reasonable balance of etch and deposition rates.

Process performance is affected by many parameters among which gas flow rate, pressure, and applied rf power are the most critical.[65] As pressure increases, the concentrations of atomic fluorine and other radicals increase, resulting in a higher etch rate. However, high pressure reduces ion energy, sheath width, and dc bias across the plasma sheath, which tends to result in isotropic profiles.[65] Conversely, higher bias power will increase the dc bias and ion directionality, which promotes anisotropy. However, increasing bias power or ion bombardment energy increases the PR etch rate faster than the silicon etch rate, leading to lower etch selectivity.

After the etch process is complete, the passivation film can be removed by plasma ashing or by immersion in ethoxy-nonafluorobutane ($C_4F_9OC_2H_5$).[69]

C_4F_6 was investigated as an alternative gas for passivation.[72] When C_4F_8 is used, there was a measurable silicon etch rate in the passivation step under certain process conditions but no silicon etch was observed when C_4F_6 was used. The reason was that the low F/C ratio of the fluorocarbon film tended to slow the etch rate of the film.[72,76,77] The polymer deposition rates in C_4F_8 and C_4F_6 plasmas are also different (Fig. 4).[78] Due to the difference in polymer properties resulting from use of C_4F_6, the process parameters should be adjusted to obtain the desired profile. Under experimental conditions, the anisotropy of the silicon trench using C_4F_6 passivation gas was found to be comparable to or better than that with C_4F_8.[72]

It was reported that sub-40 nm silicon pillar arrays fabricated using time-multiplexed deep silicon etch achieved with 1.5 μm depth, an aspect ratio of 50:1, or even 60:1 (Fig. 5).[73]

A. Etch rate

Silicon etch rate increases with pressure in the low pressure region due to the increase in atomic fluorine concentration. However, increasing pressure further results in an etch rate decrease because ion energy and radical flux decrease in high pressure plasma.[65] Thus, there is a particular pressure at which maximum etch rate is observed. The silicon etch rate is almost independent of the C_4F_8 flow rate and RIE power during passivation.[65]

TABLE I. Comparison of time-multiplexed ICP-RIE etch processes.

	Passivation step						Etch step						
Process	Pressure (mTorr)	Gas	Flow rate (SCCM)	Source (W)	Bias (W)	Time (s)	Pressure (mTorr)	Gas	Flow rate (SCCM)	Source (W)	Bias (W)	Time (s)	Rate (μm/s)
Bosch Ref. 57	7.5–75	CHF_3 Ar	<100	300–1200	0	⋯	7.5–75	SF_6 Ar	<100	300–1200	3–5	⋯	2–20
Ref. 65	⋯	C_4F_8	90	⋯	2	⋯	⋯	SF_6	136	⋯	12	⋯	3.3
Ref. 67	17	C_4F_8	120	1000	0	5	40	SF_6 O_2	260 26	2800	16	6.5	⋯
Ref. 58[a]	20	C_4F_8	40	600	0	30	20	SF_6	40	600	−70 V	60	⋯
Ref. 68	17	C_4F_8	85	600	0	5	26	SF_6	130	600	20	6	3.0–3.5
Ref. 69	⋯	C_4F_8	80	600	0	9	⋯	SF_6	130	600	15	11	2.5–3.0
Ref. 70	⋯	C_4F_8	200	1500	0	1	⋯	SF_6	250	1500	80[b]	3	⋯
Ref. 64	⋯	C_4F_8	100	600	0	6	⋯	SF_6 O_2	130 13	600	12	7	⋯
Ref. 71	10	C_4F_8	95	625	0	5	20	SF_6 O_2	125 7	650	11	5	1.25
Ref. 72	50	C_4F_8 or C_4F_6	20	200	−50 V	⋯	5	SF_6	5	200	−100 V	⋯	⋯
Ref. 73	20	C_4F_8	85	600	0	5	20	SF_6 O_2 Ar	30 5	600	600	7	⋯
Ref. 74	22	C_4F_8 Ar SF_6	70 40 1	850	0	5	24	SF_6 Ar	100 40 Ar	850	8	7	⋯
Ref. 75[c]	50	C_4F_8	10	200	−50 V	120	5	SF_6	4	200	−200 V	120	⋯
Ref. 69	⋯	C_4F_8	80	600	0	9	⋯	SF_6	130	600	15	11	2.5–3.1

[a]Modified Bosch process with a transition step added (at −5 °C).
[b]260 kHz low frequency, 10 ms on, 90 ms off.
[c]Faraday cage, placed between the wafer and the plasma source, was used for this recipe to improve selectivity.

Overall etch rate decreases with an increase in aspect ratio.[17] Etch rate in the time-multiplexed etch process is very sensitive to feature size, increasing with an increase in feature dimensions. This property, ARDE, further explored below, tends to produce negative profiles on large open areas.[13]

Increasing cathode temperature also increases etch rate.[68] However, higher temperature causes higher sidewall etch rate and lower polymer deposition rate, leading to sidewall erosion and undercut profiles.[40] Adding argon helps increase ion bombardment, which increase the etch rate and anisotropy, thus improving sidewall profile.[68]

The chemical reaction fundamentals determine that silicon etch rate increases with plasma power by enhancing dissociation in the plasma and SF_6 flow rate by raising the concentration of reactants at the wafer surface. However, the values of these parameters can affect etch characteristics such as sidewall profile and selectivity, so other parameters will probably have to be modified to compensate.

The effect of the total silicon area exposed to the plasma (loading) on etch rate were explained by the rate equation

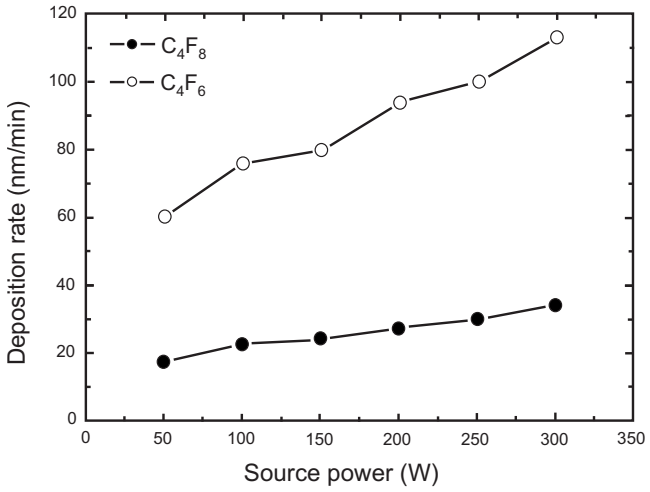

FIG. 4. Polymer deposition rate comparison in C_4F_8 and C_4F_6 plasma at the same condition.

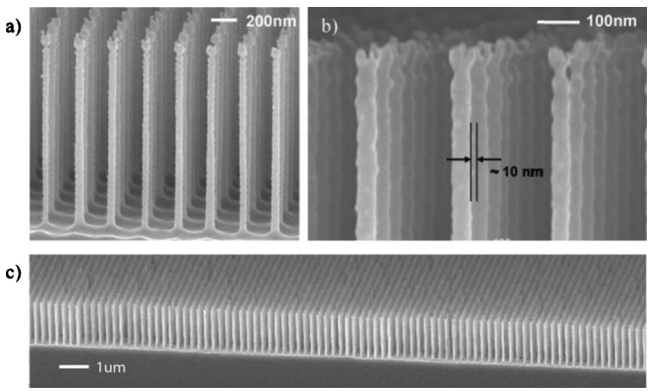

FIG. 5. Arrays of vertical silicon (100) nanopillars. (a) Silicon nanopillars as narrow as 40 nm diameter and 1.5 um tall with vertical sidewalls arrayed on an ordered 235 nm pitch grid. (b) Higher magnification view showing sidewall roughness less than 10 nm peak-to-peak. (c) Wide field view showing a large area array with long range order.

proposed by Mogab.[79] Silicon etch is a chemical reaction in a plasma environment. The greater the surface area, the lower the etch rate for the same features at the same kinetic conditions.[79]

In 1999, a maximum etch rate of 10 μm/min was obtained, while adjusting process conditions to improve the profile reduced the etch rate to 6 μm/min. This result was achieved at room temperature with the etch rate increasing from center to edge by 10%–15% in the ICP-RIE reactor.[80] Later, an etch rate in excess of 20 μm/min became practical.[81]

B. Etch rate uniformity

Etch rate uniformity is also a critical parameter. All factors affecting etch rate can cause etch rate nonuniformity, including plasma power, gas flow, temperature, and pressure distribution. Plasma density is higher at points closer to the rf power coils, resulting in an increase in local etch rate. Therefore, etch rate uniformity is strongly affected by the etch tool design. Process changes such as increasing the flow rate of the C_4F_8 passivation gas, decreasing the SF_6 flow rate, and cooling the wafer to a temperature of about 5 °C may improve etch rate uniformity but at the expense of reduction in the overall etch rate.[17]

Etch rate uniformity deteriorates when pressure or average loading increase. Empirically, it has been found that etch rate uniformity may improve when a small amount of oxygen is present in etch step.[17]

According to fundamental kinetics, etch rate uniformity on a wafer is affected by temperature uniformity. Etch rate sensitivity to temperature is dependent on the etch reaction activation energy. The higher the activation energy, the more influence the temperature has. Because silicon etch reaction is a highly exothermic reaction (−176 kcal/mol Si), heat release and its effects on etch uniformity should be considered. However, no systematic studies were found that related etch rate uniformity effects to wafer temperature distributions.

Another parameter affecting etch rate uniformity is the local concentration of the reaction radical, i.e., the atomic fluorine. Etch rate is not only dependent on the gas flow pattern but also on the local consumption rate and transport phenomena. The flow pattern plays an important role in determining the macro scale etch rate pattern distribution, while the mass transfer in the plasma sheath and in the trench determine the local reaction rate. The flow pattern generally is not affected by the desired etch depth but the local reaction rate depends on the trench depth or aspect ratio. In other words, the etch trench depth uniformity is a function of etch depth and feature dimension.

Ideally, a uniform instant etch rate through the whole etch period would be achieved. In practice, this is not necessary, because it is the final, or time-averaged, etch rate uniformity that is important. Instead, a small number of process steps with constant process parameters can be used. Each step does not have instant etch rate uniformity but in combination, good overall (final) etch depth uniformity is achieved. For example, a fast etch rate step with a certain uniformity signature may be combined with a slower step with the opposite signature to give good overall etch depth uniformity.

It was reported that etch rate uniformity could be improved by cooling the material being etched, putting the etching into an ion-activated reaction rate-limited regime, where the ion energy, not the local concentration of reactants, dominates the etch rate.[82]

However, other researchers have found that increases in SF_6 flow or rf power, or decreases in chamber pressure tend to improve etch rate uniformity.[83]

Of course, hardware design plays an important role in final etch trench depth uniformity. If the hardware is not uniform, no amount of process tuning can produce a satisfactory result. The cathode must have uniform temperature distribution and the ICP source must produce a uniform ion density across the wafer.

C. Selectivity

Another important etch rate parameter is the relative silicon etch rate with respect to mask (typically PR) etch rate, i.e., the etch selectivity. If the PR is fully depleted before the end of the etch process, the top surface of the substrate will be damaged. The PR etch rate increases significantly when high RIE, or bias, power is applied to the cathode. Therefore, the bias power, which is related to bombardment strength, is the important parameter for selectivity determination. That etch rate increases with bias power is well known but a high bias power tends to increase PR erosion, so PR thickness becomes the limiting factor. Recently, new PR materials formulated for ultrathick (12 to 100 μm) applications was reported.[84] It is expected that the new ultrathick PR will be helpful in enhancing etch rate by allowing higher bias power to be used.

D. Profile

A straight and smooth profile is generally required for HAR silicon etch but for some silicon mold fabrication and TSV applications, a sloped sidewall angle (e.g., around 85°) is preferred. The characteristic scalloped shape resulting from the time-multiplexed process can be problematic for downstream processing, so profile control is critical.

The shape of the scallops is determined by many process parameters. When the process is well controlled, the peak-to-valley distance on scallop profile can be in the range of 50 nm.[65] It was reported that the ratio of power to pressure had a significant influence on the scallop shape, with a higher ratio tending to produce a smoother profile.[65]

Sidewall slope is dependent on the ratio of the etching and passivation step times. A relatively long etch cycle compared with passivation tends to give a reentrant profile. Similarly, too short an etch time results in a positive slope.[85]

The etch and passivation cycles are often maintained for only a few seconds (e.g., 3–5 s) to suppress sidewall scalloping. Owing to the residence time, the short cycle time results in some overlap of the gases with consequent mixing during the step transition. It was believed that this gas mixing in the plasma environment promoted polymerization.[65] However,

this mixing of gases may make it difficult to control the profile angle by varying the etching and passivation time periods. Therefore, a third step was sometimes introduced to completely evacuate the reactant gases between steps.[58] Adding a third step made the creation of sloped sidewalls for mold release simple.

Etch profile tends to change with trench depth or aspect ratio. A practical strategy to solve this problem is create a multistep process recipe to change the bias power or dc bias voltage according to the depth. It was reported that bias voltage was varied from −70 V for 0–20 μm etching, −80 V for 20–30 μm etching, and to −90 V for 30–40 μm etching to achieve a vertical profile.[58] The variation in voltage with etch step time can improve the overall profile but there may be noticeable transition in the profile between the different steps. Adding more steps or continuously changing bias voltage with time can be used to obtain a smoother profile.

Profile angle and sidewall surface roughness are very important for most applications. When HAR silicon etch is used for silicon mold fabrication, a wavy profile can make demolding difficult. A postpassivation step using C_4F_8 was reported to be effective for reducing the root mean square sidewall roughness of the silicon master mold trenches by about half and thus reducing the friction coefficient of the silicon surface sixfold.[22]

A scalloped profile can cause problems for the subsequent metal fill in TSV applications. To achieve the least scalloped profile possible, a wet etch has been used to smooth the surface after dry etch.[86] Postetch wet processing using KOH and isopropyl alcohol (IPA) can reduce the sidewall roughness to 6 nm but the process is complicated.[83] Adding oxygen in etch step may also result in a smoother surface but can lower etch selectivity.[68] A conventional time-multiplexed etch process produces a high sidewall ripple of 100–200 nm. Optimization of etch and passivation time reduces the sidewall ripple to about 10 nm at the expense of sidewall profile angle.[86,87] Because the etch rate reduces as the depth increases (because of ARDE, described below), the scallops on the upper part of the trench sidewalls are deeper and further apart than lower down, i.e., the surface roughness decreases with depth. Therefore, TSV is sometimes etched by a steady-state one step recipe for the first part and then by a time-multiplexed recipe to etch to the final depth in order to reduce the trench sidewall roughness. However, trenches made by this method show a clear transition between the two process regimes.

There are several critical challenges for the development and adoption of 3D integration technologies. One of them is the formation of reliable TSVs. Creating HAR TSVs is more challenging because there is normally insufficient space between features to accommodate a tapered sidewall.[45] Because the intrinsic scalloped profile may cause intermittent barrier and seed layer coverage leading to intervia electrical leakage current,[88] the addition of a smoothing isotropic dry etch process after the time-multiplexed trench etch was studied to help to smooth the scallops and taper the via profile to prevent void formation during the copper electroplating process. Via tapering helps conformal deposition of isolation dielectric, copper diffusion barrier metallization, copper seed metallization over the sidewalls of the TSV, and bulk metal filling processes such as electroplating.[68] Recent progress in thin wafer manufacturing and handling capability allow shallower vias to be used (50–100 μm).

Process conditions for the tapering profile isotropic etch were reported to be: 12 mTorr pressure, 180 SCCM SF_6, 18 SCCM O_2, 700 W ICP power, 20 W RIE power, and process time of 10 min.[68] This process is not truly isotropic as wet process but the result is a smooth tapered profile.[68,89]

Whether or not to use a tapered profile is mainly dependent on the bulk conductor fill process. Usually, metallization for filling the via employs CVD tungsten or electroplated copper; for these, tapered profiles are preferred because they allow higher fill rates than nontapered TSVs.[90]

Due to the importance of surface roughness in MEMS and TSV applications, sidewall smoothness has received much attention. The sidewall ripple results mainly from the isotropic etch in a time-multiplexed process. Therefore, process parameters eliminating the isotropic property are helpful in smoothing the sidewall surface. Anisotropic etch with high bias power in the etch step can help to minimize the sidewall ripple but it will decrease the selectivity.[91] To solve this problem, using a Faraday cage above the cathode in the etch step was tested, resulting in a lower ion-to-radical ratio.[75,92] With this configuration, sidewall roughness was improved without significant decrease in selectivity. The method has not been widely accepted for production for the Faraday cage above the wafer may introduce defectivity issues.

Another common method for controlling sidewall smoothness is to reduce etch and polymerization step times but the suitable ratio of the etch and deposition times should be kept to ensure the vertical sidewall profile. Due to the change in etch performance with aspect ratio, continuous control and adjustment of etch parameters as the etch progresses is a suitable strategy.[93]

Profile tilting, where the etch does not proceed normal to the wafer surface, is caused by "boundary distortion" or local differences in radical density and ion bombardment angle, typically at the edge of the wafer.[94] Increasing the sheath thickness by using lower process pressure, can improve tilting.

Profile angle changes with feature size are also an issue. If the process is optimized to give a vertical profile on a certain critical feature size, features larger than critical feature size may have a reentrant profile, while ones smaller than critical feature size will have positive profile angle. The phenomenon may be reduced by changing process parameters such as chamber pressure.

E. ARDE

ARDE, loosely referred as to RIE lag, exists in all etch processes but is of particular concern when fabricating HAR structures. In HAR etch applications in MEMS or TSV, features with a wide variation in sizes have to be etched simultaneously. Also, an ideal process would tolerate different features from wafer to wafer without modification. For TSV etch, via dimensions for the via-first process are about

1–20 μm with aspect ratios of 3:1 to 10:1, while via dimensions for the via-last process are about 20 to 50 μm with aspect ratios of 3:1 to 15:1.[44] This wide range indicates the difficulty of etching these features in one process condition.

Depletion of the fluorine content at the trench bottom is the root cause for ARDE.[95] The dominant process parameters are thus SF_6 flow rate and its dissociation.[65] The flux of radical species into the deep trench is key for etch kinetics, which is governed by Knudsen transport.[95]

ARDE is also affected by pressure and temperature. It was reported that ARDE could be improved by increasing pressure[96,97] and decreasing temperature.[96]

ARDE can cause large features to be etched through earlier than small features, which may cause etching on the layer beneath, or even leakage of cooling fluid for some applications. It should be noted that ARDE is not always undesirable: some special applications intentionally make use of ARDE, such as the fabrication of slope electrodes.[98]

ARDE is a result of transport phenomena. The higher the aspect ratio, the more difficult it is for reactants to reach the trench bottom and for byproducts to escape. This mass transfer rate varies with etch progress, leading etch rate to decrease with etch progress. One strategy to overcome ARDE is to change the etch parameters as the etch progresses. Increasing the bombarding bias power gradually once the etch depth is deeper than a predetermined value was reported.[58] Lower pressure tends to tighten the angular ion distribution, improving mass transfer to the bottom of the trench and consequently ARDE.[99] In high pressure plasma RIE tools the angular ion distribution is wider, thus ARDE is worsened.[100]

The mass transfer rate to the bottom of a deep trench decreases significantly with increasing aspect ratio. For a given set of process parameters, the apparent etch rate will fall to zero at some maximum value of aspect ratio. This maximum achievable aspect ratio is known as the "critical aspect ratio."[20,74,101] Both simulations and experimental results demonstrate that the critical aspect ratio depends on the relative flux of neutral species and ions at the trench opening during the polymer etch step.[101] The relationship between etch rate and aspect ratio is shown on Fig. 6.[101] Note that this model breaks down at very HARs.[101]

ARDE, as an effect of mass transfer, is attributable to many parameters, including topographical effects such as ion shadowing, neutral shadowing, charging, and Knudsen transport of neutrals.[102] The etch rate depends on aspect ratio largely due to depletion of fluorine radicals and some redeposition of passivation polymer. Both higher ion flux and ion energy are found to be critical to enabling the time-multiplexed etch process to attain a higher achievable aspect ratio.[20] Efficient removal of the passivation layer at the trench bottom by adjusting the plasma chemistry also improves the achievable aspect ratio.[20]

Studies on ARDE at a variety of trench widths and lengths reported that the etch rate was mainly determined by the trench width rather than by the length.[40] This indicates that the etch rate is determined mainly by the shorter edge of the rectangular shape rather than by the area, although the

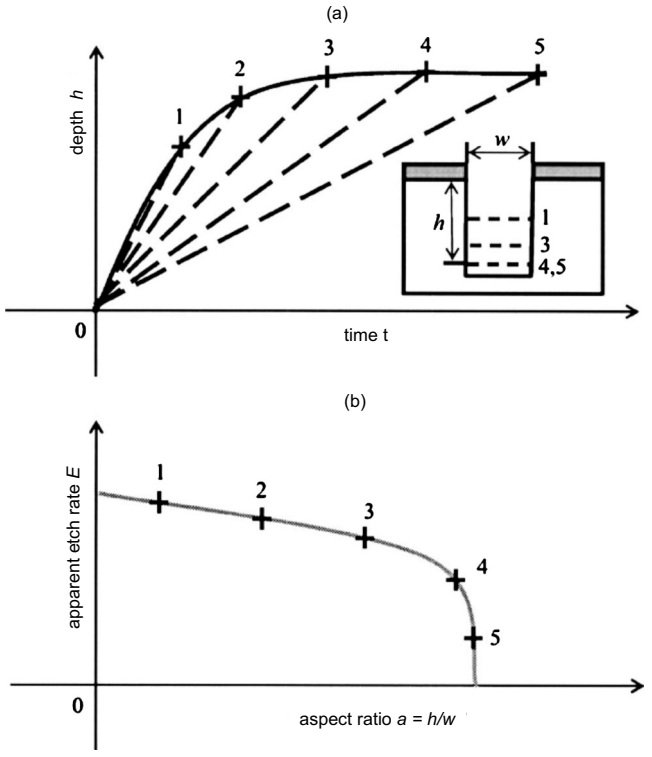

FIG. 6. Conceptual depiction of (a) the evolution of the depth of silicon trench as a function of time, and (b) apparent etch rate vs aspect ratio.

length or area has some influences on the etch rate (Fig. 7).[40] ARDE for different pattern shapes were also reported with similar results.[103]

ARDE in a time-multiplexed process was studied in detail by examining ARDE phenomena in three stages of a process cycle: polymer deposition, polymer etch, and silicon etch.[104,105] It was found that both deposition and silicon etch are aspect ratio dependent, while both deposition and etch rates are reduced in smaller features. The polymer etch rate in the etch step is almost independent of feature dimensions. Based on these phenomena, a compensation method between deposition and etch was proposed by adjusting the relative times of deposition and etch steps at certain process conditions. Using this technique, a very small ARDE effect was obtained (2% to 3% across a width range of 2.5–100 μm with 2 μm/min etch rate).[104] Cross-sectional SEM images showing ARDE results are shown in Fig. 8.

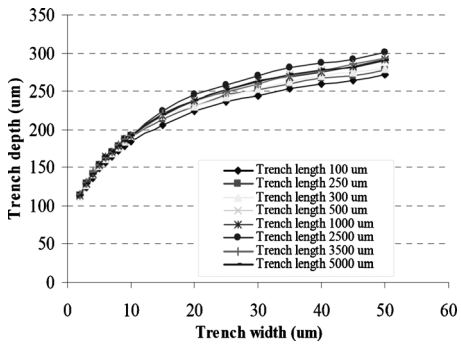

FIG. 7. Trench depth vs trench width and length.

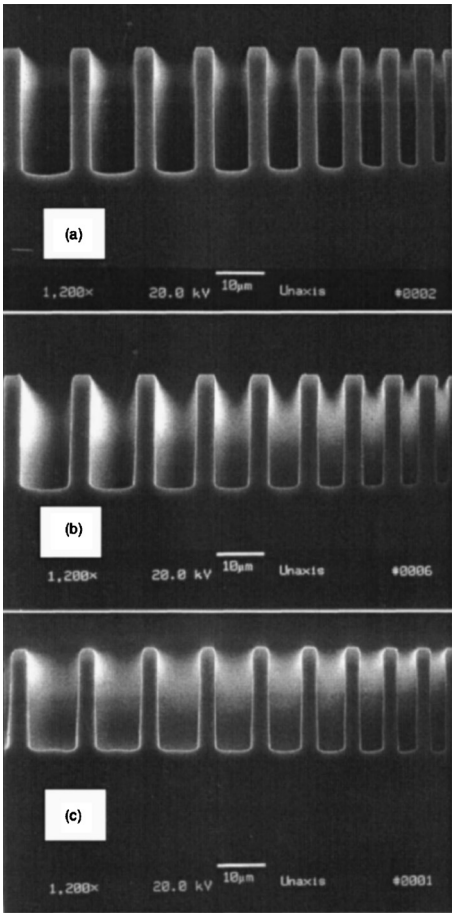

FIG. 8. The effect of ARDE under different process conditions on features with widths from 2.5–10 μm, (a) normal ARDE lag (~10%), (b) optimized ARDE lag (<2%), and (c) inverse ARDE lag (−5%).

F. Loading effects

The loading effect is an etch rate variation phenomenon resulting from differences in pattern density, i.e., the area of exposed silicon.[102] It occurs on both features of the same size and on features with different dimensions. Reactant depletion is the root cause of the loading effect. When the loading effect and ARDE occur together, investigation becomes difficult.

Differences in etch rate between features over a small area on the wafer is referred to as microloading. Owing to depletion of the reaction radicals, the etch rate decreases when the surrounding load increases. This introduces a critical distance beyond which etch rate is not significantly influenced by pattern density. It was reported that, under these experimental conditions, this critical distance was about 4.5 mm, and for an etch depth of 60 μm, a 10% pattern density increase can cause a 1 μm etch depth decrease in features within the critical distance.[67] This is the main reason that little work has been done to understand pattern density dependencies for distances larger than 5 mm, known as "die-to-die" effects.[106] When bulk concentration is adequate, the loading at a specific location affects the consumption of reactants, causing etch rate changes. When pressure decreases, the consumption of reactants has less effect. It was reported that loading effects of silicon etch decrease at low pressure.[99]

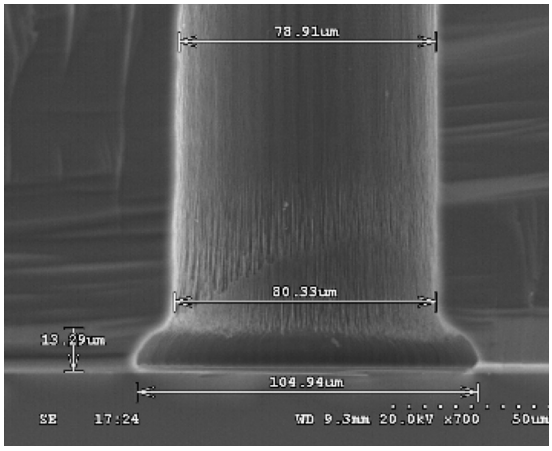

FIG. 9. Notching observed at the interface between the silicon and the SiO_2 layer.

G. Micrograss

Micrograss is the term used to describe the formation of microcolumns of silicon owing to residual polymer left on the bottom surface after the etch process. An obvious first approach for remedying this might be to increase the bias power to remove the base polymer and then the grass but increasing bias power may have some side effects. Higher bias power may attack the passivation on the sidewalls, creating a bottling shape in the sidewall.[13]

By increasing the etch step length, micrograss can be controlled without creating sidewall profile issues.[13] Other parameters that can be changed to reduce grass include temperature,[58] ICP power, and pressure.[13] When temperature is low (e.g., −10 °C), the passivating layer deposition rate is high and its etch rate is low. These effects may cause micrograss, so higher temperature enhances the removal of micrograss.[58]

Micrograss is also influenced by feature size or aspect ratio because of the difference in passivating layer deposition. Compared with open areas, micrograss is less likely to occur in small features because of the difficulty of depositing the passivating layer. It was reported that at an 80 μm etch depth, micrograss occurs on an open area but not on the bottom of a 10 μm wide features.[58]

H. Notching

Notching is a common phenomenon in time-multiplexed etch processes, which produce a special lateral etch on the boundary between silicon and the underlying layer, as shown in Fig. 9.[107] The reason is charge accumulation.[40] It occurs only where silicon is underlain by a dielectric layer. Originally, notching was observed when etching silicon on insulator structures for MEMS fabrication where the insulator layer is applied the back side of the wafer. In certain TSV applications, an etch stop layer (commonly silicon dioxide or aluminum) is used to prevent cooling helium leakage, which may introduce notching when wafer is etched through.

Notching becomes more severe when there is significant microloading, because the loading effect requires moderate overetch, where the etch continues for a certain time after the

etch stop is exposed to allow complete clearing of the trench bottoms across the entire wafer. One technique to prevent notching is to increase the thickness of polymer during the period of overetch by increasing the length of the deposition step.[13] Pressure also affects notch formation. When pressure is increased, ion energy is reduced, resulting in a low sputtering rate of polymer, which reduces the notching.[13]

Another method to control notching is to apply intermittent, or pulsed bias rf power to the cathode.[108,109] Bias pulsing reduces ionic charging of the insulator beneath the silicon layer by allowing charge to dissipate during the "off" cycle, so that notching on the bottom can be controlled.[108,110,111] When a conductive material such as aluminum is used as an etch-stop layer, no notching occurs.[40]

Because of ARDE, large features are etched through first. Overetch is necessary to etch all the features through. During overetch, the exposed stop layer on etched-through features is etched. Because the stop layer is much thinner than the wafer, etch selectivity of silicon to the stop layer becomes very significant to avoid etching though the stop layer. Therefore, it is required that the etch-stop layer underlying large features should not be penetrated before the etch depth in small features has reached the interface of the etch-stop layer.

A two-step technique to prevent notching without bias pulsing has been reported. The first step uses a time-multiplexed process to etching as deep as possible without etching through. The second step completes the final small part of the trench using a continuous etch using an etch gas (SF_6) and a passivating gas (C_4F_8) together.[107]

It should be noted that charge build-up during HAR etch is not always a problem. For example, in MEMS fabrication, notching has been used for *in situ* releasing of a HAR beam.[112]

III. STEADY-STATE ETCH PROCESSES

A. RIE

In the early development of deep silicon etch, RIE was used in isolation, i.e., without any form or source plasma such as ICP. This produces an anisotropic etch but the inherently low plasma density results in a low etch rate. Because the plasma density depends on the bombardment strength in RIE reactors, producing a highly anisotropic etch always requires strong bombardment, resulting in excessive PR erosion, forcing the use of either thick PR or a hard mask (e.g., oxide mask).[113]

Passivating the trench sidewall by dissociating gas reactants in a plasma environment is a common strategy. In the early 1990s, it was reported that a mixture of SF_6 and C_2ClF_5 was used for etch and passivation to achieve aspect ratios up to 50 and silicon to PR selectivity of 28.[113,114] Under the same etch conditions, more anisotropic trench profiles were obtained using a resist mask than using an oxide mask.[113,114] The possible reason was that more radicals containing carbon were generated during etching with PR than with an oxide mask, which then reacted on the sidewalls to form polymeric films that impeded lateral etching.[113–115]

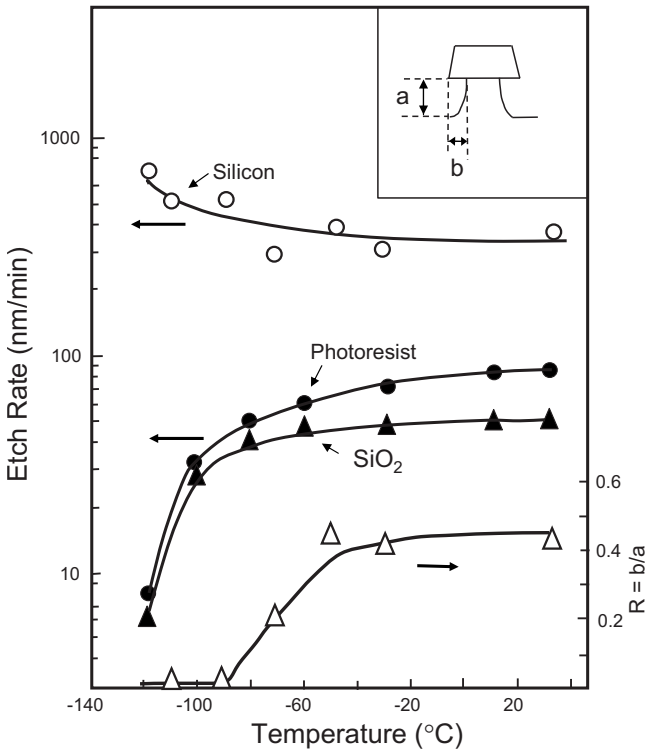

FIG. 10. Etch properties at cryogenic processes.

Sidewall passivation using dissociation of reactants is more easily controlled than passivation by dissociation of resist because resist coverage changes with the wafer pattern (loading). In the RIE mode, higher fractions of exposed silicon (high loading) have lower selectivity.[114]

It was reported that adding oxygen or hydrogen resulted in higher trench surface roughness. Conversely, decreased power or increased pressure would produce smoother surfaces.[116]

B. Cryogenic etching

The cryogenic process attempts to control the etch reactions on trench bottom and sidewall surfaces separately and achieve high silicon etch rate and high silicon-to-resist selectivity by lowering the cathode, and hence the wafer, temperature.[12] The main characteristics of the cryogenic processes are shown in Fig. 10.[12] A HAR silicon trench created using a cryogenic etch process is shown in Fig. 11.[117]

Figure 10 indicates that the silicon etch rate increases and PR etch rate decreases when temperature is reduced, especially below −100 °C. Good anisotropy without silicon undercut was achieved when temperature dropped below −100 °C. Therefore, cathode temperatures below −100 °C became the norm for cryogenic etch and this condition became the starting point for further process optimization.

However, low temperature alone cannot guaranty anisotropy. Even at temperatures below −120 °C, isotropic etch was obtained.[118] After the addition of oxygen, anisotropic etch was generally obtained. Sidewall passivation plays an important role in reducing lateral etch. It was reported that

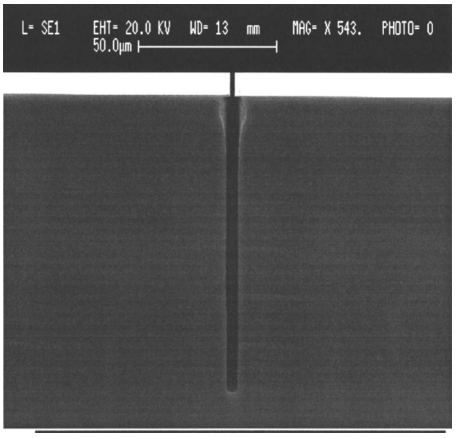

FIG. 11. Cross-sectional SEM image of silicon etch by using helicon reactor with cryogenic process (1999).

ion bombardment might dominate the cryogenic etch process in most cases, because surface chemical reaction rates are greatly reduced by the low temperature.[119]

The cryogenic process uses SF_6 and O_2 gases to passivate and etch simultaneously. The passivation film consists of SiO_xF_y. Compared with teflon-type polymer passivation found in the time-multiplexed process, SiO_xF_y passivation film is more difficult to etch, requiring high bombardment energy to clear the passivation layer from the trench bottom surface and allow vertical silicon etch without visible lateral etch. Although higher bombardment energy generally increases the resist etch rate, the low temperature found in the cryogenic process ensures that a low resist etch rate is achieved. An important advantage of cryogenic processing is its low sidewall surface roughness.

The cryogenic process has a high etch rate when feature sizes are larger than 1 μm.[86] When SiO_2 is used as a hard mask, a selectivity of 750 can be achieved.[86] Temperature and oxygen flow rate are the key parameters responsible for the profile. A decrease in oxygen flow will reduce the passivation, enhancing isotropic etch. Conversely, too high an oxygen flow rate may cause a "pinch-off" of the trench, where at some particular depth, formation of oxide at sides of the trench bottom causes a narrowing of the trench. Reducing the temperature tends to produce more passivation and improve profile verticality.[86] Increasing the bias power or reducing the pressure both make the sidewall profile more vertical.

When PR is used as a soft mask, selectivity is a challenge for cryogenic processing. A resist modified by gallium ion implantation and then oxidized to form a gallium oxide was developed, which improved the etch selectivity significantly. Gallium-ion-implanted silicon has also been used as an etch mask, which can produce HAR features as small as 40 nm.[14] An example recipe for the cryogenic process is: 60 SCCM SF_6, 13 SCCM O_2, 600 W ICP power, 5 W RIE power, 10 mTorr and −115 °C, resulting in an etch rate of 2.85 μm/min.[120]

Cryogenic processing uses a hardware configuration similar to that of the time-multiplexed etch process except that helium or liquid nitrogen is used to cool the wafer below −100 °C. The etch chamber usually consists of ICP coils for plasma generation and a cathode for bombardment control.

Deep silicon trenches were also etched under cryogenic conditions using an electron cyclotron resonance (ECR) plasma process in a SF_6 and O_2 gas environment.[121] The etch rate decreased significantly with an increase in oxygen flow rate, and the fluorine/oxygen ratio played an important role in varying the etch profile from a positive to a negative slope.

A helicon plasma reactor using helium and liquid nitrogen for cooling has also been used.[122] For a 2 μm wide, 50 μm deep trench, a 5 μm/min etch rate was obtained. The wafer surface temperature strongly affected the profile with low temperature having better anisotropy. Note that a temperature difference of 10 °C between the chuck and the wafer is common, even though helium and liquid nitrogen cooling was used.[122]

Cryogenic etch is not widely used today because of the practical difficulty of maintaining the very low wafer temperature. The reactor hardware is complex, and the time taken to cool the wafer down from ambient temperature for processing, and back to ambient after processing results in a very slow process with low manufacturability.

C. Near-room temperature high density plasma (HDP) etch

In an effort to overcome the shortcomings of the RIE-only and cryogenic approaches, reactors using two plasma sources, e.g., ICP and RIE, were explored at room or near room temperatures. The use of chlorine instead of fluorine as the etch gas was also explored, because the lower reactivity of chlorine results in less sidewall erosion.

In the 1990s, ECR HDP using 2.45 GHz microwave power found application in near room temperature HDP silicon etch.[99,123,124] This process used chlorine radicals and a 13.56 MHz bias electrode to control bombardment strength. However, the lower reactivity of chlorine results in lower etch rate, even with strong bombardment. So although the etch profile was good, the low etch rate (i.e., 0.31 μm/min or less) made this process unsuitable for volume manufacturing. In 1998, Cl_2 was used in an RIE-ICP etch tool for micromachining a silicon field emitter and HAR resonators with controlled profiles and HARs. In this application, the low etch rate problem might not be a problem.[125]

In 2000, a steady-state etch process was reported that used HBr and O_2 and SF_6.[81,126] HBr alone and $SF_6/HBr/O_2$ were examined using an ICP-RIE configuration, HBr only having a lower etch rate. The process conditions using $SF_6/HBr/O_2$ were: 10–30 mTorr, 600–1000 W ICP power, 15–44 W RIE power, $(SF_6+O_2)/HBr$ ratio of 1 to 3, and total flow of 170 SCCM. This process showed a high etch rate (>3 μm/min) and good trench depth uniformity (nonuniformity <1%). Trenches from 0.6 to 10 μm wide etched by this process is shown are Fig. 12.[127]

The trench profile is very sensitive to pressure, with a higher pressure giving a more tapered sidewall. The primary reason for this is that higher pressure increases sidewall

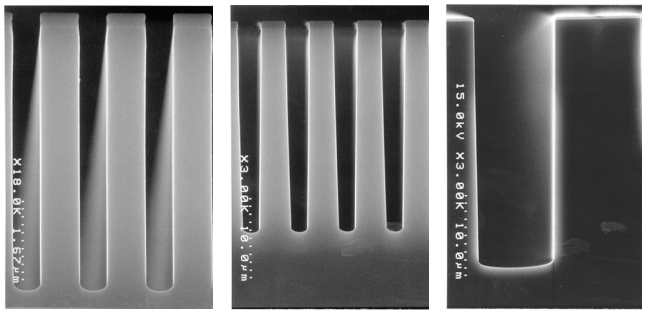

FIG. 12. HAR trench of 1 μm wide and 7 μm using one step silicon etching sampled at wafer center (left) and edge (right).

polymer deposition. However, higher pressure may increase trench depth nonuniformity by worsening plasma uniformity at higher pressures.

SF_6/O_2 ratio is a sensitive parameter for etch rate and trench profile. High SF_6/O_2 ratio tends to result in high etch rate and vertical profile, mainly because the high ratio relatively increases etchant species (fluorine) and reduces passivating species (oxygen). However, if the ratio is too high silicon lateral etch (isotropic etching) will occur and selectivity will decrease. High bias power also reduces the selectivity.

It was found that a very high source power can stop the etch process completely.[81] The mechanism may be that high power increases a fast silicon surface oxidation at the expense with silicon-fluorine reactions. This effect can be mitigated by increasing the fluorine content (raising the SF_6/O_2 ratio), increasing the ion energy (RIE power), or both.

A HAR result using this method is a trench with about 90:1 aspect ratio and 90 nm critical dimension (CD) (Fig. 13).[128]

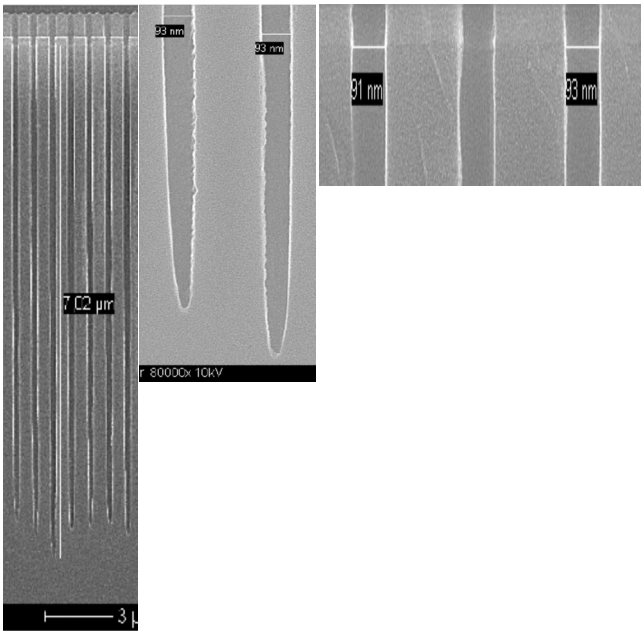

FIG. 13. HAR trench etched by a single step etch process at near room temperature.

A process using the same etchants was reported for MEMS applications. In this case, however, a magnetically-enhanced RIE bias power system was used in combination with an ICP source.[112]

Yet another simultaneous etch and passivation process used the same gases as the time-multiplexed etch process, SF_6 and C_4F_8.[107,127] When etch gas and passivating gas are introduced into the plasma chamber together, the etch and passivation occur simultaneously. This makes it possible to find process conditions in which an anisotropic profile can be obtained, as shown in Fig. 14.[127] Variety of profiles were obtained by varying the ratio of passivating gas (C_4F_8) to etch gas (SF_6) for silicon etch, as shown in Fig. 15 for an ICP-RIE reactor.[107]

The profile changes with the ratio of C_4F_8 to SF_6, from isotropic etch profile at 0% C_4F_8 [Fig. 15(a)] to anisotropic vertical profile at 75% C_4F_8 [Fig. 15(f)]. The disadvantage of this process is a low etch rate (about 1.6 μm/min).[107] With improvement of the etch reactor and the process to increase etch rate, this steady-state etch may have a promising future in MEMS and TSV applications where moderate sidewall slope makes bulk metal fill easy.

In 2004, SF_6 and O_2 gas were used for steady-state HAR silicon etch, achieving a vertical profile, 20:1 aspect ratio, and 1.3 μm/min etch rate for 0.35 μm holes. It was found that the etch rate was determined by the fluorine-to-ion ratio and influenced by pressure, with a maximum etch rate occurring at 25 mTorr.[129] At high pressure, the fluorine-to-ion ratio is high, so the etch rate is ion-limited, and at low pressure, the fluorine-to-ion ratio is low, so the etch rate is neutral-limited. Profile is mainly determined by the fluorine-to-oxygen ratio. A high fluorine-to-oxygen ratio tends to produce isotropic etch and vice versa.

Recently, simultaneous etch with passivation has made significant progress in terms of etch quality and etch rate. TSV sidewall roughness specifications are becoming more stringent, so more attention is being paid to this technology, making it a strong alternative method to currently popular time-multiplexed process.

IV. ETCH METHOD AND EQUIPMENT

Reactor designs differ mainly in the plasma generation method. Common methods are ECR, ICP, helicon wave, helical resonator, microwave surface wave, and capacitive coupling, most of which have been examined for HAR silicon etch.

Very early reactors used two parallel plates. The lower one usually held the wafer. 13.56 MHz rf power, chosen because of its wide availability, was capacitively coupled to either the upper or lower electrode. The former configuration is commonly called plasma etch (PE) mode and the latter RIE mode. The main difference between these two modes is the bombardment strength, with RIE having stronger bombardment and hence lower selectivity. The rise in temperature owing to the relatively strong bombardment in RIE mode further reduces selectivity.

Using a parallel capacitively coupled plasma with $SF_6/CHF_3/O_2$ gases, an etch rate of 2.5–2.8 μm/min was

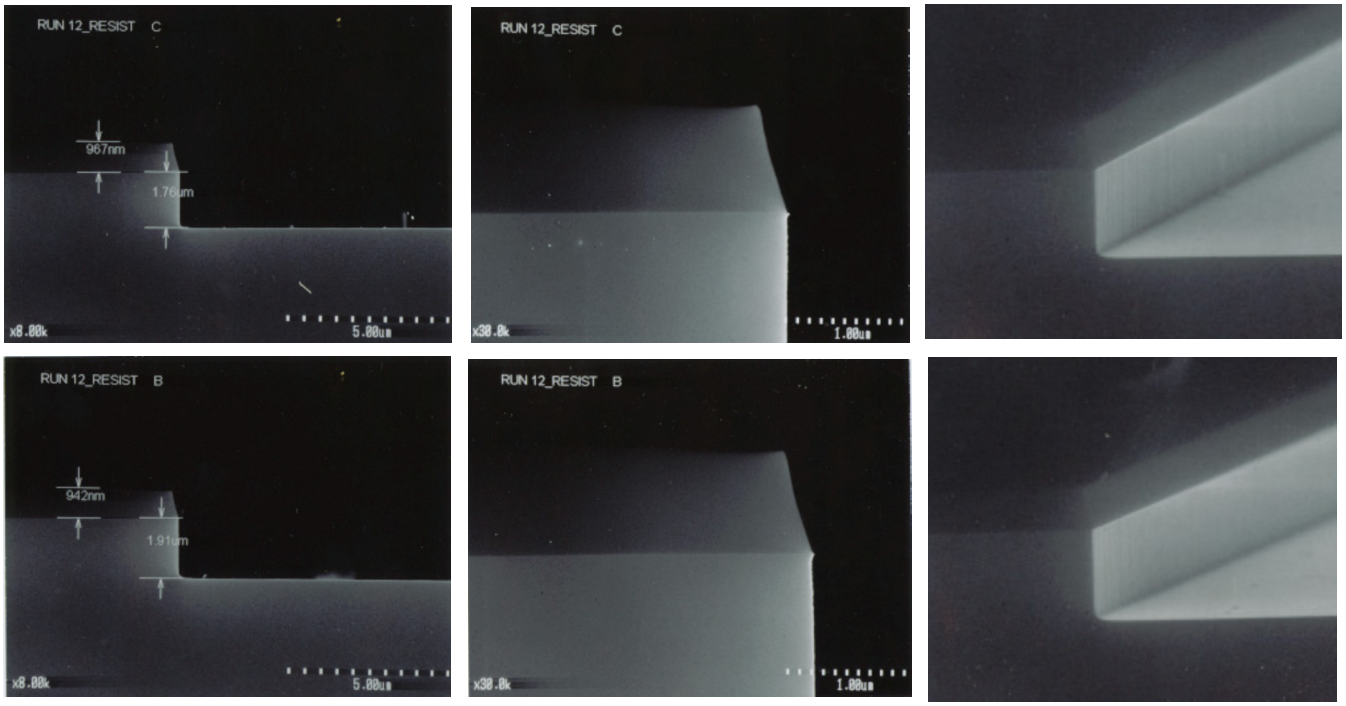

FIG. 14. (Color online) A MEMS part with a vertical profile etched by a single step etch process at near room temperature.

reported but the anisotropy was only 0.5 (see Fig. 10), insufficient for most MEMS and TSV applications.[130] It was reported that a magnetron RIE (MRIE) tool with a rotary cathode achieved a submicron HAR pattern but at a low 0.3 μm/min etch rate.[131] In another study, an RIE reactor, with a magnetic field and a narrow gap between the electrodes to increase plasma density, achieved an etch rate of 1.6 μm/min.[132] In another experiment, to achieve a high etch rate, ferromagnetic materials were inserted inside the pedestal of an RIE reactor, producing a 10 μm deep trench for a submicron capacitor at an etch rate of 6 μm/min in 1992.[47]

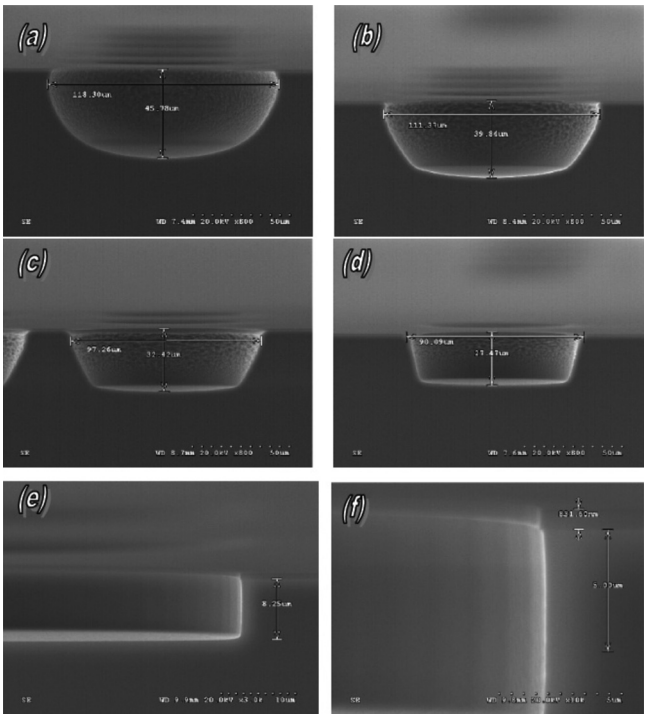

FIG. 15. Profile changes with C_4F_8 contents balanced with SF_6 in a steady-state silicon etching, (a) 0% C_4F_8, (b) 10% C_4F_8, (c) 20% C_4F_8, (d) 30% C_4F_8, (e) and (f) 75% C_4F_8.

To increase etch rate, more etch radicals must be produced by dissociation in the plasma. This dissociation depends on plasma density. The phenomenon was understood in the 1980s and since then strategies for improving HAR silicon etch have been to decouple bombardment energy and plasma density with a variety of chemicals to improve the anisotropy for HAR. Combined with RIE, several HDP generation methods were investigated, including ICP, magnetron ion etch (MIE), MRIE,[131] microwave ECR,[99,123] as well as magnetic neutral loop discharge.[133]

The reactor configuration is driven by the evolutions of the etch process evolution. A dc plasma discharge confined by multipolar magnetic surface layer was reported in 1985 using SF_6 and O_2.[134] In 1992, a comparison of deep trench silicon etching using MIE and RIE in SF_6/O_2 plasma was reported.[135] The study showed that RIE produces a smoother trench surface while the MIE shows better sidewall angle and etch rate.[135]

Before cryogenic processing was proposed in 1988, processes developed using microwave plasma, ECR plasma, and magnetron-type RIE were force to make compromised between anisotropy, selectivity, and etch rate.[12] Both RIE and ECR can achieve anisotropic profiles but the etch rate is usually low when aspect ratio increases. By using cryogenic processing, SF_6/O_2 etchants and SiO_2 hard mask in a helicon reactor, an aspect ratio of 20 to 50:1 with an etch rate of 5 μm/min was reported in 1999.[117]

The helicon plasma source was proposed in 1982 and was widely studied.[117,136] Its main advantages are high

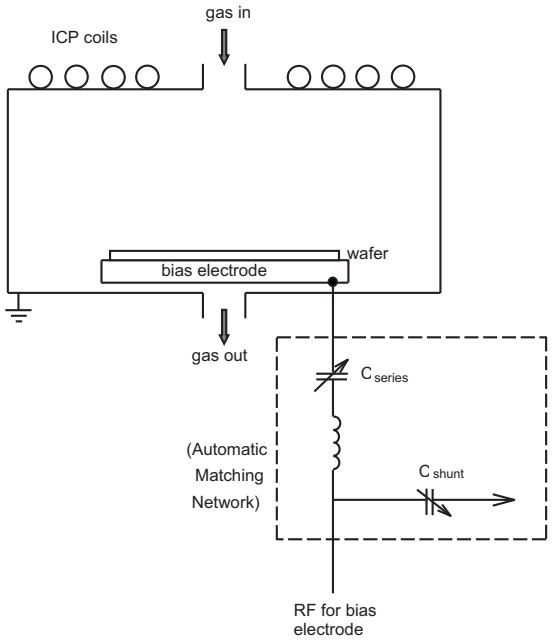

FIG. 16. Diagram of a typical ICP-RIE reactor.

plasma density, independent control of plasma density and ion energy, and low pressure operation. In the mid-1980s, a multipolar helicon plasma source discharge was used for anisotropic silicon etching in a SF_6 and oxygen system.[134,137]

Since the mid-1990s, the ICP-RIE configuration has come to dominate HAR silicon etch (Fig. 16). The main advantages of this configuration are simplicity, low cost, and good process stability allowing straightforward process optimization.

There is no systematic comparison among different etch tool configurations but it was reported that MRIE etch rates of silicon substrate were insensitive to the loading in the range from 10% to 50%, in contrast to ICP etching at their experimental conditions.[112] However, the etch rate of this MRIE configuration was rather low.

Although many characteristics can be improved by optimization, some issues, such as tilting, is mainly solved by modifying the reactor hardware.

V. THEORETICAL ANALYSIS

A. Thermodynamics

The most important use of thermodynamics is to determine the overall reaction products and spontaneity under predetermined conditions, more specifically, under constant pressure and temperature. Gibbs energy change analysis is a well known method. For HAR silicon etch, theoretical analysis is focused on etch and passivation.

HAR silicon etch generally uses fluorine-containing chemicals (e.g., SF_6) for etch owing to good byproduct volatility, and C_4F_8 for sidewall passivation. Cl_2 chemistry for silicon etch exhibits a slow etch rate,[33,138] low selectivity to SiO_2 hard masks and low byproduct volatility.[139] Br-containing gases have also been used but byproduct volatility and etch rate are even worse than chlorine-containing gases.[140] Mixtures of ClF_3 and SF_6 were also studied in the early 1990s but detailed follow-up data are lacking.[141]

Besides SF_6 gas, NF_3 and SiF_4 were studied and proved to have a high etch rate but HCl, HBr, and $SiCl_4$ demonstrated better anisotropy at the expense of a relatively low etch rates.[142] Oxygen is helpful in building the passivation layer on the sidewall but too high an oxygen flow rate will produce very thick passivation on the trench bottom which is difficult to etch, resulting in a low, or even zero, etch rate.

For steady-state ICP-RIE deep silicon etch, $SF_6/HBr/O_2$, XeF_2, and BrF_3 were investigated.[81,143,144] However, to date, there is no systematic comparison between these fluorine-containing gases, and SF_6 is the most popular gas for HAR silicon etch.

A computer model using the Gibbs energy minimization (GEM) method to determine the reaction products and spontaneity was reported.[145] By using GEM, overall silicon etch reactions were obtained for different reactants. When silicon is etched by SF_6 gas at 20 mTorr, we have the following spontaneous etch equations:

$$\mathrm{Si} + 2\mathrm{SF}_{6(g)} = \mathrm{SiF}_{4(g)} + 2\mathrm{SF}_{4(g)} \quad T > 100\ ^\circ\mathrm{C},$$

$$2\mathrm{Si} + 2\mathrm{SF}_{6(g)} = 2\mathrm{SiF}_{4(g)} + \mathrm{S}_2\mathrm{F}_{2(g)} \quad T < -30\ ^\circ\mathrm{C}.$$

The equations show that all byproducts are volatile and silicon-containing product is SiF_4 gas but the sulfur-containing product depend on temperature. When temperature is above 100 °C, the equilibrium product is SF_4 gas but when it is less than −30 °C, the product is S_2F_2 gas. From −30 to 100 °C, both products can exist.

When NF_3 gas is used at constant pressure and temperature conditions, the overall spontaneous etch reaction is:

$$3\mathrm{Si} + 4\mathrm{NF}_{3(g)} = 3\mathrm{SiF}_{4(g)} + 2\mathrm{N}_{2(g)}.$$

It is generally believed that atomic fluorine is the reactive radical but at room temperature both SF_6 and NF_3 are thermodynamically stable gases. The plasma environment may be responsible for dissociating the reactants to form the atomic fluorine.

Several chemicals function as passivating agents among which octofluorocyclobutane (C_4F_8) is very common. During sidewall passivation, C_4F_8, a cyclic fluorocarbon, breaks down in the plasma to produce CF_2 and longer chain radicals.[13] These radicals are believed to be responsible for polymerization on sidewall and base surfaces.

C_4F_8 is a perfluorocarbon, which is not an environmentally friendly gas. Therefore, use of environmentally benign gases, such as unsaturated fluorocarbons, was reported.[72] Deep silicon etching using SF_6/C_4F_8 and SF_6/C_4F_6 were compared, showing different performance.[13,78] C_4F_6 gas can produce thicker, more strongly bonded fluorocarbon films than C_4F_8 because more CF_2 radicals and lower F/C ratio fluorocarbon films were generated in the C_4F_6 plasma, according to OES and x-ray photoelectron spectroscopy (XPS) measurements.[72] However, it is difficult to obtain the overall passivation reaction owing to the lack of thermodynamic data on organic compounds.

The spontaneity of the polymerization depends on the overall Gibbs energy change in the process, resulting from volume and surface Gibbs energy changes, the former being negative and the latter positive.[146]

The original condensed polymer particles (seeds) must be larger than a certain size before spontaneous reactions will occur. However, polymer is difficult to form in gas phase, because of the surface Gibbs energy. It is much easier to form polymer on a surface, such as a feature sidewall or trench bottom because of the lower surface energy.

Thermodynamic parameters are keys to the spontaneity of polymerization. The most important is temperature, with low temperatures the most favorable. Thermodynamic etch reaction products are also helpful for determining kinetic mechanisms and rate equations formulae. Unfortunately, there is insufficient data to determine the byproduct compositions for etch and passivation reactions.

B. Kinetics

Plasma etch kinetics is focused on etch rate and mechanism. Consequently, understanding and measuring elementary reaction radicals in a plasma environment become critical. Experimentally, it is very challenging to measure ions and reactive radical densities. Generally, ion density is measured using a Langmuir probe and densities of free radicals are estimated using an optical emission spectrum. In a time-multiplexed etch process with passivation, the polymerization characterization is also important to the overall process. It was reported that the polymer layer deposition and sputtering were also monitored with *in situ* ellipsometry.[20]

The reaction mechanism in a time-multiplexed etch process was studied and the following dissociation reaction proposed:[89]

$$SF_6 + e^- \rightarrow SF_5^+ + F + 2e^-,$$

where atomic fluorine and SF_5^+ are the dissociation products in the plasma environment. The silicon etch reaction is:[89]

$$Si_{(s)} + 4F_{(g)} \rightarrow SiF_{4(g)}.$$

The passivation is caused first by the dissociation of C_4F_8:[89]

$$C_4F_8 + e^- \rightarrow C_3F_6 + CF_2 + e^-.$$

Then CF_2 is adsorbed to form a teflonlike polymer on the solid surfaces:[89]

$$nCF_2 \rightarrow (CF_2)_n.$$

It should be noted that although the etch mechanism proposed in above equations is plausible, there is no direct proof for this assumption.

The kinetics of etch reaction and polymerization are helpful in improving the etch process and increasing the overall etch rate. Because polymerization contributes negligibly to the overall etch rate, it is preferred to have a fast polymer deposition and long etch time to obtain a high etch rate.

Polymerization consists of two steps: a gaseous reaction in the plasma environment to form the gaseous monomers for the polymer and the polymerization itself, similar to crystallization processes of nucleation and growth. When plasma density and chemical flow rate are sufficiently high, mass transfer may be the rate control step.

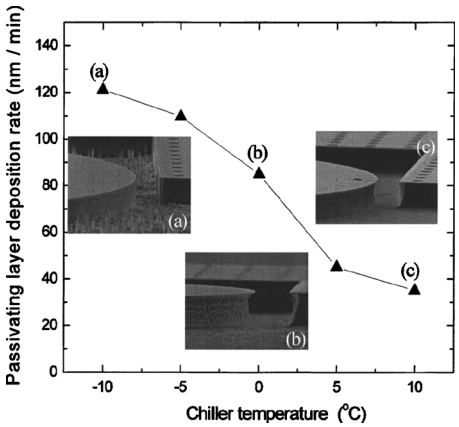

FIG. 17. Polymer deposition rate vs temperature.

Kinetically, lower temperatures result in more seeds to grow polymer. The overall polymerization rate depends on the seed creation rate and the seed growth rate. When the seed creation rate rather than growth rate is a control step, the overall polymerization rate will increase with the decrease in temperature (Fig. 17).[58] When the polymer deposition rate is too high, micrograss results [Fig. 17(a)]. Conversely, too little polymerization results in undercutting from isotropic etch [Fig. 17(c)].

Etch rate is determined by radical formation in plasma, mass transfer from bulk plasma to trench surface and activation on the reaction surface. The mass transfer in deep trench is believed to be the rate-control step, usually described by the conductance model.[15,103] Average etch rate over one etch /passivation cycle in the time-multiplexed process, by definition, can be expressed as:[104]

$$r_A = r_e\left[1 - \frac{\tau_d}{\tau}\left(1 + \frac{r_d}{r_p}\right)\right],$$

where r_e is silicon etch rate at the trench bottom; τ_d and τ are passivation and overall time durations in one cycle; r_d and r_p are polymer deposition rates during the passivation step and polymer etch rate during the etch step, respectively. Clearly, the etch rate, r_A is a function of aspect ratio because r_e, r_d, and r_p are all determined by aspect ratio.

Assuming that the etch rate is proportional to the reactant flux, the etch rate during silicon etch step can be expressed as:[18]

$$r_e = r_{eo}\left(\frac{K}{K + S - KS}\right)$$

where r_{eo} is silicon etch rate at zero aspect ratio; K is transmission probability, i.e., the probability that a randomly directed particle incident on one end of a tube will exit the other end; and S is the reaction probability. K is a function of aspect ratio. The model and experimental results are in good agreement (Fig. 18).[103] For the time-multiplexed process, the polymer deposition and etch rates are also dependent on as-

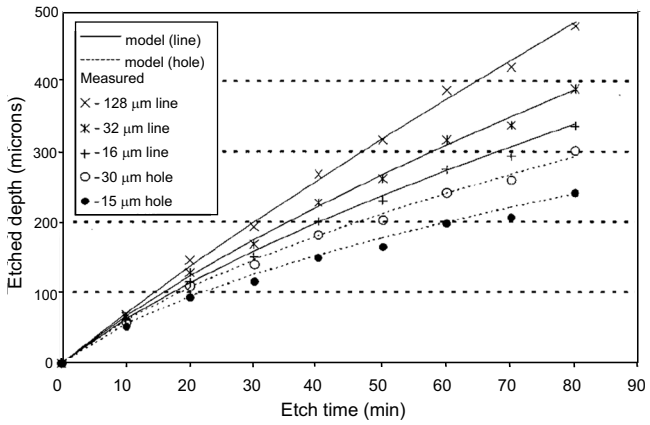

FIG. 18. Comparison between model-calculating and experimental results.

pect ratio but there is no satisfactory equation for them so far.

Mass transfer to the trench bottom is a function of aspect ratio. It was reported that the fluorine-containing ion current decreases with an increase in aspect ratio.[147] This relationship between ion current versus aspect ratio follows the same trend as etch rate versus aspect ratio but it has not been proved that fluorine-containing ion current plays an important role in determining the silicon etch rate.

Three components determine the chemical reaction rate in plasma environments: physical sputtering rate, chemical reaction rate, and ion assisted reaction rate. To maintain high selectivity of etched material to PR, bias power and physical sputtering rate should be minimized. Therefore, anisotropic etch is mainly determined by the etch rate balance between chemical reaction and ion assisted etch rates at the trench bottom and sidewall.

Chemical etch reaction at the sidewall is strongly dependent on the temperature, according to kinetic theory. Because average ion incidence angle to the bottom surface deviates only a few degree from normal, ion assisted etch on the sidewall is relatively small compared with bottom etch. Hence sidewall etch rate is mainly determined by chemical etch rate and decreases with temperature. However, the bottom etch rate behaves differently. Owing to the almost vertical bombardment, ion assisted etch rate at the trench bottom plays a much more important role than on the sidewall, especially when temperature decreases. This mechanism indicates that a decrease in temperature causes a significant reduction in sidewall etch rate but not on the trench bottom. However, only reducing temperature cannot guaranty the HAR silicon quality. Partial oxidation of trench sidewall by producing SiO_xF_y passivation layer enhances the sidewall etch control.[13] This explains why cryogenic etch processing can improve feature anisotropy at HARs.

Etch kinetics at ambient temperature or near room temperature become more and more important owing to the fact that this HAR etch method has advantages such as smooth sidewall angle, HAR, high selectivity, and easy operation for production. Current etchant is generally $SF_6/O_2/SiF_4$. Because of the relatively high oxidation rate of silicon at room or near room temperature compared with cryogenic process, strong bombardment is required to obtain a moderate etch rate at trench bottom, which may cause a high PR erosion rate. At well controlled etch conditions, a modified layer on top of PR can be formed, which reduce the PR erosion rate, resulting in an acceptable etch selectivity.

VI. CONCLUSIONS

HAR or deep silicon etch has been employed in many applications since the very early days of silicon etch in the 1970s. Currently, deep silicon etch is used mainly for MEMS and TSV applications. It is predicted that TSV etch will become a critical process for 3D IC stacking technology. Other applications include deep silicon etch for DRAM capacitors.

Anisotropic silicon etch had limited applications and the HAR etch process was in the research and development stage before 1990. Three inventions played important roles in deep silicon etch. The HDP environment realized by introducing the ICP-RIE configuration, which enabled independent control of plasma density and bombardment strength. Cryogenic processing which made deep silicon etch practical as an industrial practice. Even though achieving a wafer temperature below −100 °C is costly and makes process control complicated, this process has some special etch properties, such as steady-state process control and low trench sidewall surface roughness which are essential for some applications. Lastly, the time-multiplexed process, which repeats pairs of passivation-etch steps to obtain HARs and straight sidewall profiles. Important advantages are high etch rate and selectivity, although the time-multiplexed process suffers the intrinsic disadvantage of scalloped sidewalls and high sidewall surface roughness. Since its introduction, many process modifications have been proposed to overcome this drawback. Besides above three inventions, gradual progress on single step etch at room or near room temperature using SF_6/O_2 as well as other gases proves today that this approach has many special advantages (e.g., smooth trench sidewall, high etch rate and selectivity). The performance makes this method have good application potentials.

Much progress has been made in deep silicon etch over the last twenty years but challenges remain. In TSV etch, further increases in etch rate are needed for large volume production. Other challenges include controlling sidewall roughness, tilt, sidewall angle, microloading, notching, micrograss, and ARDE.

In the future, more fundamental work will be necessary to meet the increasing demands on HAR etch. The etch and passivation mechanisms are not well understood and practical rate equations need to be established. Progress in these areas will allow higher throughput processing and lower costs, critical benefits in the semiconductor industry.

ACKNOWLEDGMENTS

The authors would like to thank Richard Lewington of Applied Materials for his editorial contributions to this paper.

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