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Fast and accurate methods for the performance testing of highly-efficient c-Si photovoltaic modules using a 10 ms single-pulse solar simulator and customized voltage profiles

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Abstract
Performance testing of highly efficient, highly capacitive c-Si modules with pulsed solar simulators requires particular care. These devices in fact usually require a steady-state solar simulator or pulse durations longer than 100–200 ms in order to avoid measurement artifacts. The aim of this work was to validate an alternative method for the testing of highly capacitive c-Si modules using a 10 ms single pulse solar simulator. Our approach attempts to reconstruct a quasi-*steady-state* I–V (current–voltage) curve of a highly capacitive device during one single 10 ms flash by applying customized voltage profiles—in place of a conventional V ramp—to the terminals of the device under test. The most promising results were obtained by using V profiles which we name '*dragon-back*' (DB) profiles. When compared to the reference I–V measurement (obtained by using a multi-flash approach with approximately 20 flashes), the DB V profile method provides excellent results with differences in the estimation of P_{max} (as well as of I_{sc}, V_{oc} and FF) below $\pm 0.5\%$. For the testing of highly capacitive devices the method is accurate, fast (two flashes—possibly one—required), cost-effective and has proven its validity with several technologies making it particularly interesting for in-line testing.

Keywords: photovoltaic module, calibration, highly efficient c-Si, capacitive effects

(Some figures may appear in colour only in the online journal)

1. Introduction

Overall global production capacity of photovoltaic (PV) cells and modules has reached 37.2 GW_p in 2011 [1]. The significant increase in industrial production is nowadays accompanied by a large number of '*new*' technologies and concepts entering the market, including *thin film* technologies and *highly efficient* c-Si solar cells.

As an increase in the efficiency of the modules is one of the main drivers to reduce the overall cost of PV, extensive research has been devoted to improve solar cell performances. For c-Si solar cells, several approaches have been investigated and are commercially available today. Among them are *back-surface fields*, *back-contact* solar cells and *heterojunctions* between crystalline and amorphous Si layers.

For these technologies, however, the presence of highly doped back-surface field layers, sophisticated back-contact structures or intrinsic semiconducting layers significantly increases the capacitance of the solar cells/modules, consequently complicating the performance testing of these devices [2–9].

The so-called *sweep-time effects* in fact originate from capacitance effects present in the solar PV device, in particular from the voltage-dependent capacitance. The capacitance of a PV solar cell is the sum of the *diffusion capacitance* (C_{diff}) and the *depletion layer capacitance* (C_{depl}). Because distortions are only observable at voltages close to or greater than the *maximum power point voltage* (V_{mpp}), where C_{depl} can be neglected, the biggest contribution to the observed sweep-time effects originates from the C_{diff} [3, 6, 10]. For some PV technologies and devices and very fast *I–V* (current–voltage) sweeps, the presence of the C_{diff} gives rise to a significant capacitive current which must be either added to or subtracted from the photo-generated current of the PV solar module.

In particular, the testing of *highly efficient* and *highly capacitive c-Si modules* with pulsed solar simulators may be affected by strong measurement artifacts and lead, depending on pulse duration, to under- or overestimations of the measured power of over $\pm 20\%$ [3–5].

Consequently, these devices usually require characterization under natural sunlight, a steady-state solar simulator or pulse durations longer than 100–200 ms in order to avoid measurement artifacts. The latter are offered only by a few manufacturers and are generally expensive. Conventional flashers (with pulse durations in the range from 5 to 20 ms) may be used to test these devices only by applying particular approaches such as the *multi-flash* (MF) or *sectional* ones [6, 11–13] that require a larger number of flashes (about 20 flashes for the MF) and are therefore time-consuming and in the long term will induce accelerated ageing of the lamps. A modification of the MF approach is proposed by Sinton and coworkers which suggests applying a slightly modulated voltage signal to the module during the light pulse. This maintains a constant charge in the solar cell and avoids transient effects [8, 14, 15].

In addition to the cost-reduction potential and the possibility for PV manufacturers to further differentiate their products, the transition towards highly efficient concepts/approaches will possibly gain additional momentum also due to the fact that several patents about the HIT (heterojunction with intrisic thin layer) technology developed by Sanyo (one of the most highly capacitive—and consequently difficult to test—technologies) have just expired or are just about to [16].

Consequently, in the short–medium term (3–10 years) a pronounced increase in the share of highly efficient/highly capacitive c-Si devices on the overall PV market can be expected. This increase will be followed by the need to further improve the capabilities of accurately and efficiently testing these particular devices.

This work presents the main outputs of the MPVT (multi-purpose PV tester) project [17], which aimed at developing a novel electronic load (EL) for an *I–V* measurement set-up and at validating two reliable and fast alternative methods for the testing of highly capacitive c-Si modules using a 10 ms single pulse solar simulator.

The first method (Method 1), presented in this work, attempts to reconstruct a quasi-*steady-state I–V* curve of a highly capacitive device during a single 10 ms flash by applying a *customized voltage profile* (CVP)—in place of a conventional voltage ramp—to the terminals of the device under test.

The second approach (Method 2) attempts to reconstruct a *steady-state I–V* curve of a highly efficient PV device by first tracing a slow-speed (>200 ms) dark *I–V* curve followed by a *translation* and *reconstruction* procedure. This method—well known for solar cells [13]—has now been validated and slightly adapted to be effective on a module level and will be presented in a following paper.

2. Experimental set-up

I–V testing of a set of PV modules was performed at standard test conditions (STC: 1000 W m^{-2}, 25 °C, AM1.5)—according to the relevant IEC 60904 set of standards—using a Pasan IIIB solar simulator (flash unit) and two different ELs developed by Pasan.

(1) The reference measurements on the capacitive PV modules were carried out using the MF method and a Pasan BV66 EL available at SUPSI and part of its ISO-17025 accreditation system.
(2) A novel EL from Pasan (HIGH-LIGHT, HL)—partly developed within the MPVT project—was used to validate the novel measurement methods used for the testing of highly capacitive devices. The HLEL, among other features, allows us to import and generate CVPs.

Compared to the BV66 EL the new HL EL presents some advantages, mainly: (i) extended voltage and current ranges; (ii) four quadrant drive; (iii) improved converter resolution (16 versus 12 bits); (iv) faster acquisition (5 versus 12 μs per point). These last parameters allow a better definition and consequently a better acquisition of specific waveforms that are applied to the device under test.

With the exception of the two ELs and of two calibrated shunt resistors (one for each EL), the same testing equipment was used to perform the *I–V* measurements. This includes: a calibrated c-Si reference cell, the same *flash unit* (lamps) of the Pasan IIIB, cables and connectors, and temperature sensors. The accepted temperature measurement range is 25 $\pm$1 °C. The overall combined measurement uncertainty for the *I–V* measurement of c-Si modules in combination with our conventional (BV66 EL) testing equipment corresponds to $\pm 2.4\%$ ($k = 2$) on the measured power P_{max}. The measurement repeatability associated with our *I–V* measurement set-up corresponds to $< \pm 0.8$. A simple layout of the *I–V* measurement set-up is shown in figure 1.

Prospective differences between the two measurement set-ups (i.e. ELs) may therefore be ascribed only to differences in the calibration of the electrical measurement channels (*I* and *V*, ~0.2%) of both ELs and to temperature variations.

Several commercially available conventional and highly efficient c-Si PV modules from different producers were used to validate the method (including *Sanyo HIT/HIP* and *Sunpower*'s back-contact technologies). The devices investigated are listed below in table 3.

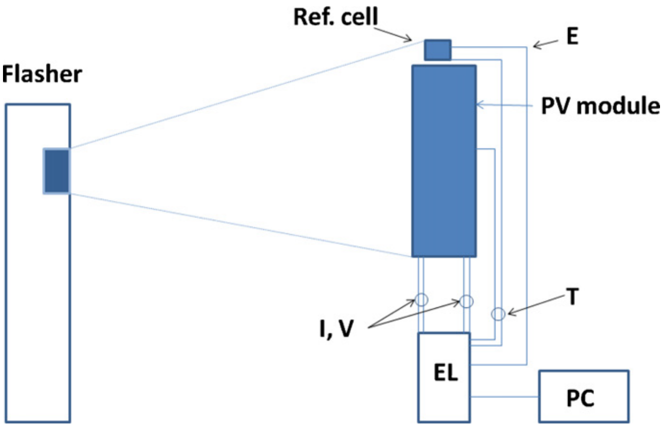

Figure 1. Layout of the *I*–*V* measurement set-up: a flasher is used as a light source; a reference cell is used to check the irradiance (E). *I* and *V* signals of the device under test are connected to an EL, which is connected to a PC. The temperature of the PV module and of the reference cell is carefully monitored. Two different ELs were used in this work.

The basic relations between the electrical quantities of the *I*–*V* curve of a PV solar device are briefly recalled in the appendix.

3. The method

I–*V* characteristics of PV modules are usually tested by applying linear voltage (*V*) ramps to the terminals of the module and by measuring the current (*I*) flow. For highly capacitive devices, however, due to the slow response to external signals of the device, strong measurement artifacts will be introduced in the *I*–*V* curve [3–11].

Our approach attempts to reconstruct a quasi-*steady-state* *I*–*V* curve of a highly capacitive device during a single 10 ms flash by applying a CVP—in place of a conventional linear ramp—to the terminals of the device under test.

Several *V* profiles were tested. The idea behind the method recalls the MF approach [6, 11–13]. The aim is in fact to obtain a given number of plateaus with stable values for *I* and *V* signals—as for the MF approach—during one single pulse. So the pulse duration sets the temporal limit of the *I*–*V* curve. The measurement parameters were tailored to use a PASAN IIIB—with 10 ms pulse duration—as solar simulator.

Within the MPVT project the most promising results were obtained using tailored *V* profiles which we name DB profiles.

DB *voltage profiles* (shown below in figure 5) are a combination of different profiles: (1) a *staircase*-like and (2) a *parabolic*-like profile, with (3) the superposition of an *overshoot* on each stair (constant voltage level).

The MF approach generally requires a number of approximately 20 measurement points (flashes) to reconstruct a *sound* *I*–*V* curve, fit the curve and obtain the PV parameters (short-circuit current I_{sc}, open-circuit voltage V_{oc}, maximum power point P_{max} and fill factor FF) of the module. Similarly, our DB profile contains a number of about 20 *stairs*. A higher number of stairs would be favorable but does not generally allow us to obtain stable values for *I* and *V* for most highly capacitive devices.

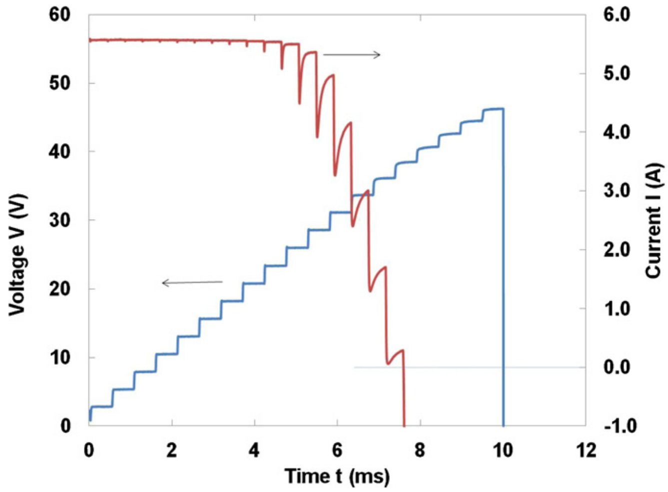

Figure 2. Temporal profile of a staircase-like *V* profile with 20 stairs and current flow at the terminals of the module for a highly efficient c-Si PV module (Sanyo HIT).

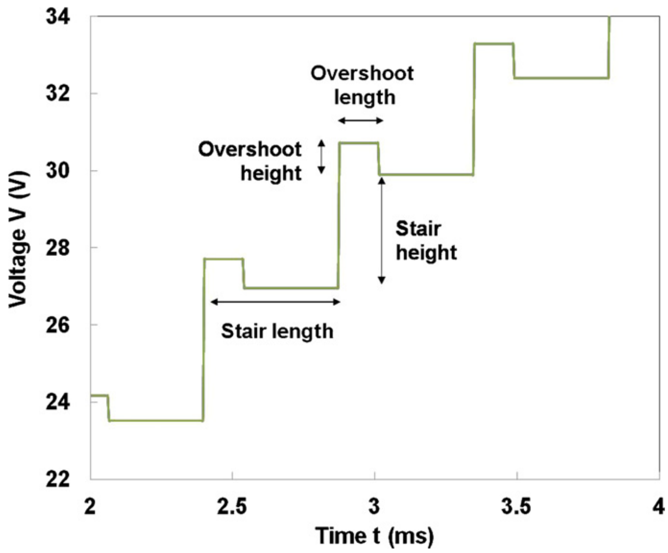

Figure 3. Magnification of the *DB* voltage profile of figure 5 showing stairs (constant voltage levels) and the overshoot needed to stabilize the current signal.

Nevertheless, as figure 2 shows, applying a *staircase-like V profile* during a single 10 ms flash to a highly capacitive device allows obtaining stable *I* plateaus in the part of the curve from I_{sc} to approximately 85% of the V_{mpp} only, i.e. for voltage levels where the module's capacitance is relatively low. For higher voltage levels (and higher capacitances), however, the current *I* does not follow *V* in due time, so that it is not possible to obtain stable pairs of (*I*, *V*) values and consequently reconstruct an *I*–*V* curve with this *V* profile.

In order to do so, we superimpose on top of the initial part of each stair a voltage *overshoot* (see figure 3). This overshoot is required to provide additional energy ($\Delta E = \frac{1}{2}C(V) \times V_{ov}^2$ with $C(V)$ the capacitance of the module and V_{ov} the voltage overshoot) for a very short time to the capacitor—in the equivalent circuit of the PV device—and load it. The overshoot compensates for the slow response of the device and consequently increases its temporal response.

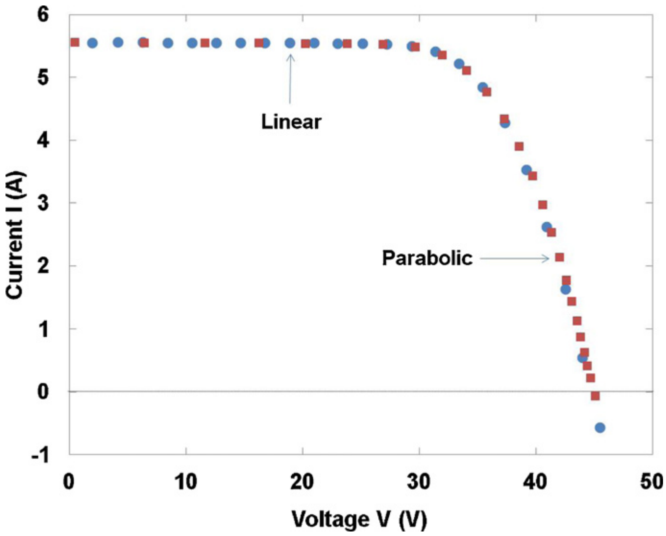

Figure 4. *I–V* characteristics with 24 (*I*, *V*) measurement points of a *conventional* (non-capacitive) c-Si PV module obtained during one single flash by applying (1) a conventional *linear V* ramp and (2) a *parabolic-like V* profile to the terminals of the PV module. Due to the diode-like behavior of a PV module, measurement points are denser close to I_{sc} for the linear *V* ramp and become denser close to V_{oc} for the parabolic-like profile.

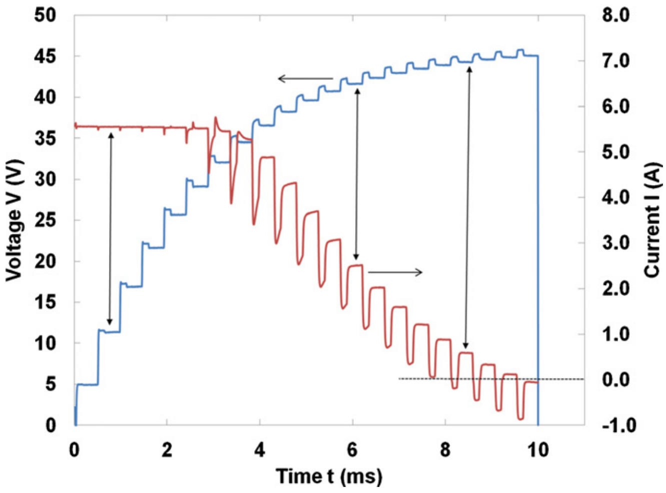

Figure 5. DB voltage profile and current measured at the terminals of a Sanyo PV module (A3) during one single flash. The arrows in the plot indicate stable values of *I–V* pairs.

The *height H* and *duration D* (as a percentage of the stair's length) of the overshoot need to be tailored for each type of PV module to obtain stable *I/V* plateaus.

Furthermore, the *height* of the overshoot can optionally be modulated during the sweep with a linear signal (from 0 to *H*). In this way, no *V* overshoot will be present close to I_{sc} conditions—where the capacitance of the module is low—and the highest values will be reached close to V_{oc}, when the capacitance of the module becomes higher and additional energy is required to load the PV module's equivalent circuit's capacitor. As shown in section 4 (results), the modulation of the overshoot height provides the most satisfactory results.

Besides the number of stairs (which sets the temporal duration of each stair), the height of each stair can be tuned. A relatively simple but effective way is to superimpose the staircase-like profile on a *parabolic-like profile*.

Due to the diode-like behavior of a solar cell/module ($I \sim \exp(V)$), for a typical *I–V* characteristic obtained by applying a linear *V* ramp, in fact the measurement points tend to be more and less dense, respectively, close to I_{sc} (where generally due to the flatness of the characteristics only a few points are needed to obtain a good fit of the *I–V* curve) and to V_{oc}.

A parabolic profile allows us to modulate the height of the stairs and to reduce the distance of the measured points for $V > V_{mpp}$, where the strong increase of the current with *V* increases too strongly the distance between (*I*, *V*) pairs and complicates the reconstruction of a good *I–V* curve. In particular, a higher number of points allow a more precise value of V_{oc} to be obtained using a linear fit.

This effect is shown in figure 4, which compares the *I–V* characteristics—with 24 (*I*, *V*) measurement points—of a *conventional* (non-capacitive) c-Si PV module obtained (during one single flash) by applying (1) a conventional *linear V* ramp and (2) a *parabolic-like V* profile to the terminals of the PV module. For both profiles the number of measurement points around V_{mpp} is enough to fit the curve and obtain precise values of P_{max}, V_{mpp}, I_{mpp} and FF.

To reconstruct a full *I–V* curve—and obtain the module's PV parameters—both reference MF and DB profile measurement points were fitted with a 10th grade polynomial (for the determination of P_{max}, V_{mpp}, I_{mpp}) and two linear regressions in order to obtain V_{oc} and I_{sc}.

In the case of the curve tested with the DB method, an additional transient (10 ms) direct *I–V* curve is measured to obtain the I_{sc} ($V = 0$) value used in the fit. In this way we reduce the errors in the estimation of I_{sc} that would possibly be introduced by simply using a linear fit of the *I–V* measurement points close to I_{sc}. Thus, the method foresees an overall number of two 10 ms flashes to trace an accurate *I–V* curve. A careful choice of the measurement parameters may possibly avoid this second flash.

4. Results

Among all test devices, the one which required the most careful choice of the measurement parameters is the SANYO PV module with HIT technology. For this reason, in the following we will show in detail the results relative to this particular technology.

Figure 5 shows the results of DB *V* profile applied to the test device and of the current flowing at its terminals. A discrepancy between the imposed voltage and the voltage profile effectively measured at the terminals of the modules can be observed (see figure 6). As figure 5 shows, a DB profile with 20 stairs allows stable plateaus to be obtained for the *I* signal as well. These intervals are well defined in the initial (close to I_{sc}) and in the last part (close to V_{oc}) of the curve. However, due to transient effects, they show some spikes around V_{mpp}. This region is in fact the most sensitive to a careful choice of the measurement parameters (overshoot height and length, number of stairs, etc). Nevertheless, with a fine tuning of these parameters and rejecting *I* intervals affected by transient effects

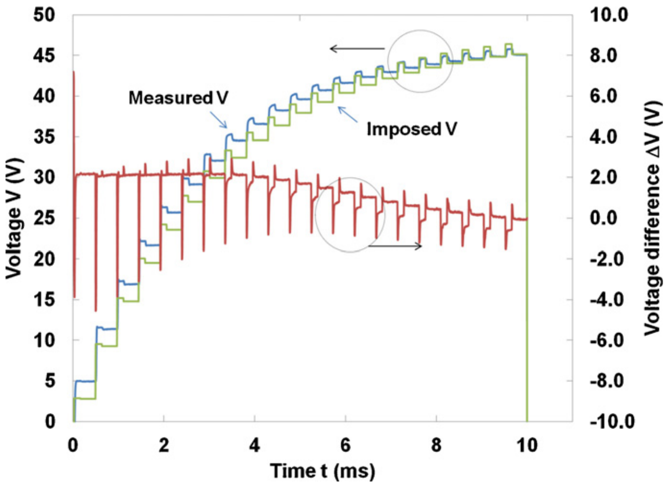

Figure 6. Imposed voltage and V signal effectively measured at the terminals of the test device. The difference between the two signals is plotted as well.

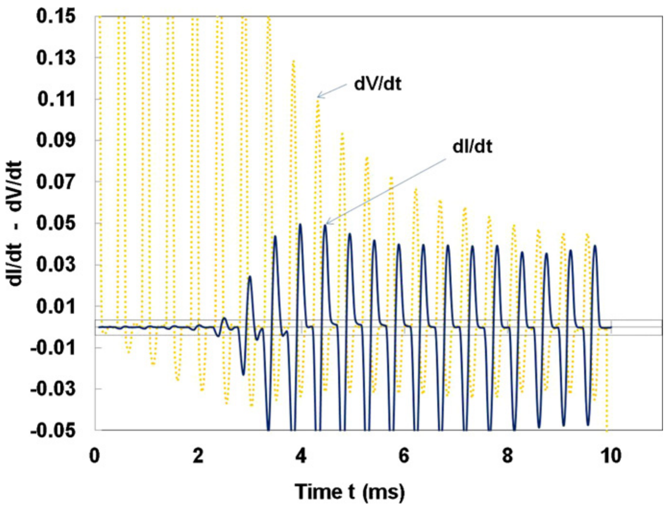

Figure 7. Values of $\mathrm{d}I/\mathrm{d}t$ (solid line) and $\mathrm{d}V/\mathrm{d}t$ (dotted line) for the I and V signals of figure 5. In order to select stabilized intervals for the current I and voltage V signals, a derivative is applied to both signals and the ranges where $\mathrm{d}I/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$ are close to 0 are selected. A dotted rectangle (not to scale) represents the arbitrarily selected intervals.

(i.e. selecting narrower I plateaus) it is still possible to find stable current values around V_{mpp} as well.

The basic idea of the method is to extrapolate—from the values shown in figure 5—some intervals with corresponding stabilized plateaus for I and V. In order to select these stabilized intervals, we apply a derivative to both I ($\mathrm{d}I/\mathrm{d}t$) and V ($\mathrm{d}V/\mathrm{d}t$) signals and select the ranges where $\mathrm{d}I/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t = 0$.

Due to signal noise and delay, the following arbitrary ranges are used in most measurement intervals: $|\mathrm{d}I/\mathrm{d}t| < 0.0025$ and $|\mathrm{d}V/\mathrm{d}t| < 0.0015$. (For this particular test device only a larger tolerance on a sub-set of measurement points around V_{mpp} is used: $|\mathrm{d}I/\mathrm{d}t, \mathrm{d}V/\mathrm{d}t| < 0.0035$.)

For the device under test, the values of $\mathrm{d}I/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$ and the corresponding values of stable I–V pairs are shown in figures 7 and 8, respectively.

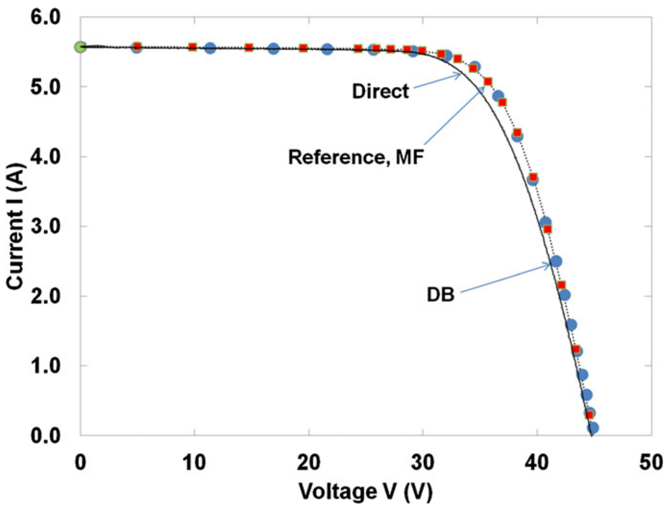

Figure 8. MF (21 flashes) reference I–V curve (red dots) with relative fit (dotted line) and I–V curve reconstructed using the DB V profile (blue dots) applied during one single 10 ms flash. A direct transient I–V curve (black solid line) is shown for comparison and is used for the exact determination of I_{sc} (green dot).

Table 1. Measured PV parameters and variation relative to reference obtained with a MF measurement (MF, BV66 EL, 21 flashes) and with a single DB V profile (HL EL, 1 flash) for the SANYO HIP (A3) test device.

Module 11–229A3 (SANYO HIT)	P_{max} (W)	I_{sc} (A)	V_{oc} (V)	FF (%)
Reference MF (21 flashes)	181.41	5.581	44.90	72.38
DB-profile (1 flash)	181.71	5.569	45.00	72.50
Variation relative to ref. meas.	0.17%	−0.22%	0.22%	0.16%

For the test device, figure 8 shows (1) I–V pairs of the reference MF measurement (21 flashes with the conventional BV66 EL) and relative fit, (2) I–V pairs obtained by applying a DB profile within a single 10 ms pulse and, for comparison, (3) a *direct* (measured from I_{sc} to V_{oc}) transient I–V curve (10 ms, HL). The transient I–V curve is swept applying a linear voltage ramp during a single pulse and for non-capacitive devices constitutes the common practice of measuring an I–V curve. Furthermore, this last measurement is used for the exact determination of the I_{sc} for the DB measurement.

In the MF reference measurements, with the aim of getting a denser number of points around V_{mpp} and improving the fitting procedure, the interval between measurement points is selected arbitrarily (i.e. non-constant V increase).

The relative variation to the reference measurement (MF) of the PV parameters measured by applying DB profiles are listed in table 1.

When compared to the reference I–V measurement (MF), as table 1 clearly indicates, the *DB V profile* method provides excellent results with differences in the estimation of $P_{max} < \pm 0.5\%$, i.e. well below the measurement repeatability associated with our set-up ($\pm 0.8\%$ for P_{max}). Similar accuracy is obtained for all other PV parameters as well (I_{sc}, V_{oc} and FF).

Table 2. Optimal choice of the measurement parameters used to generate the *DB V ramp* used to test SANYO highly capacitive PV modules.

Measurement parameter	Value
Height of overshoot	1.3 V
Length of overshoot	30% of stair
Number of steps	21
Linear modulation of overshoot	yes
Measurement points	2000 (∼ 10 ms)
V_{min}	−5 V
V_{max}	45 V
Data analysis range for dV/dt	± 0.0015
Data analysis range for dI/dt	± 0.0025 (± 0.0035 around mpp)

As a proper choice of the measurement parameters is critical for obtaining a good *I–V* curve and reproducible results, as an example the parameters used for the DB profile shown in figure 5 are listed in table 2. Laboratory experience indicates that the same set of measurement parameters may be used to test modules of the same type (with similar electrical characteristics), a feature which makes this measurement method particularly interesting for in-line testing.

In order to show the applicability of the method and its repeatability to different c-Si technologies, table 4 shows the relative variation to the reference measurement of the PV parameters of a set of selected test devices (listed in table 3) measured by applying DBs. The reference measurement is an MF measurement for all capacitive devices and a *direct* (from I_{sc} to V_{oc}) *I–V* sweep for the conventional c-Si device.

The previously shown plots are relative to the measurements of the SANYO A3 test device. For a given module type, table 3 also reports the differences (average of all devices) in the measured P_{max} between a direct (I_{sc} to V_{oc}) 10 ms *I–V* curve sweep and the reference MF measurement.

As table 4 indicates, the *DB V profile* method provides excellent results for all test devices (conventional c-Si modules and highly capacitive devices) with differences in the estimation of P_{max} $< \pm 0.5\%$ (below the long-term measurement repeatability of the system $\pm 0.8\%$). The measurement repeatability associated with each single PV parameter (I_{sc}, V_{oc}, FF) is generally lower ($< \pm 0.8\%$ for I_{sc}, $\sim \pm 0.4\%$ for V_{oc}, $\sim \pm 0.3\%$ for FF).

As mentioned in more detail in section 2, the reference MF and the DB measurements were performed on the same

Table 4. Relative variation (%) of the measured PV parameters of the test devices listed in table 3 obtained by comparing the single-flash DB V profile (HL EL) method to the reference measurement (MF and direct *I–V* curve for capacitive or conventional PV modules, respectively). All plots shown above (as well as table 1) are relative to the measurements of the Sanyo A3 test device.

PV module	P_{max} (W)	I_{sc} (A)	V_{oc} (V)	FF (%)
Sanyo HIP180NE1				
A1	0.2%	−0.2%	0.3%	0.1%
A2	0.5%	−0.3%	0.5%	0.2%
A3	0.2%	−0.2%	0.2%	0.2%
Suntechnics, STM 210F				
B1	−0.2%	−0.4%	0.2%	0.0%
B2	0.0%	−0.4%	0.4%	0.0%
B3	−0.2%	−0.5%	0.5%	−0.2%
Sunpower, SPR-225-WHT-I				
C1	−0.1%	−0.4%	0.2%	0.2%
C2	−0.1%	−0.5%	0.3%	0.0%
Sharp, NT175E1				
D1	−0.3%	−0.4%	0.6%	−0.5%

set of modules and the same equipment with the exception of using two different ELs.

Although each measurement channel (for *I* and *V*) is properly calibrated, for both ELs small offsets may exist, as well as errors associated with the measurement of the electrical signals (e.g. ±0.2% for the *I* and *V* signals with the HL EL; something slightly higher for the BV66 EL).

This may partly explain the systematic underestimation (overestimation) of the measured I_{sc} (V_{oc}) compared to the reference MF measurement.

Moreover, concerning V_{oc}, all MF reference measurements were performed on the same day, whereas DB measurements were performed on different days. As V_{oc} is quite sensitive to temperature variations, and our measurement procedure accepts module's temperatures in the 25 ± 1 °C range, differences in the module's temperature (e.g. 24.1 and/or 25.9 °C) would be translated on differences in the measured V_{oc}.

Finally, as long as the same connectors were used for all measurements FF discrepancies need to be ascribed to statistical errors only. Moreover, as the FF is purely a geometrical factor, slight variations on the measured V_{oc} and/or I_{sc} may be reflected on the estimated FF.

Besides the interesting results obtained with the CVP method, still there is room for further improvement which will

Table 3. List of the c-Si PV modules used for the validation of the DB testing methods.

PV module (producer,) type, ID code	Technology	Note	Difference in P_{max} between direct 10 ms *I–V* sweep and reference MF (average of all devices)
Sanyo, HIP180NE1 A1, A2, A3	Highly efficient c-Si (HIT/HIP cells)	Highly capacitive (pulse duration >100 ms required [3]).	−3.6%
Suntechnics, STM210F B1, B2, B3	Highly efficient c-Si (Sunpower back-contact cells)	Highly capacitive (pulse duration >100 ms required [3]).	−2.3%
Sunpower, SPR22WHT-I C1, C2	Highly efficient c-Si (Sunpower back-contact cells)	Highly capacitive (pulse duration >100 ms required [3]).	−1.6%
Sharp, NT175E1 D1	Conventional c-Si (possibly with back-surface field)	Not capacitive with 10 ms pulse duration.	−0.2%

be the subject of future work. In particular, the method may slightly be improved (1) by selecting a voltage profile (other than the linear or parabolic ones shown in figure 4) which should allow us to obtain a denser number of points around V_{mpp}, consequently, allowing a better fit of P_{max} and FF and (2) by modulating the height of the overshoot with a triangular (or parabolic) rather than a linear signal. This should allow stable I plateaus to be obtained around V_{mpp}, but avoiding transient effects in the I plateaus of the last part of the I–V curve when approaching V_{oc}, which sometimes disturb the measurement.

5. Conclusions

When compared to the reference I–V measurements (multi-flash), the *dragon-back V profile* method provides excellent results with differences in the estimation of $P_{max} < \pm 0.5\%$ (as well as of I_{sc}, V_{oc} and FF), i.e. with an uncertainty below the measurement repeatability associated with our measurement set-up. The method has provided excellent results for all devices under test including conventional c-Si modules and highly capacitive devices.

For the testing of highly efficient and highly capacitive devices the method is fast (two 10 ms flashes—possibly one—required) and cost-effective. Nevertheless, a careful choice of the measurement parameters and of some parameters used for the data analysis is required. The same parameters may, however, be used for the testing of modules of the same type proving excellent repeatability.

A commercial product offering this feature could ease and considerably speed the *indoor performance testing* (particularly the in-line testing) of highly efficient and highly capacitive c-Si PV modules.

A second approach (Method 2) to reconstruct a *steady-state* I–V curve of a highly efficient PV module investigated in the MPVT project will be presented in a following publication. This latter approach is based on the measurement of a slow-speed *dark* I–V curve followed by a *translation* and *reconstruction* procedure.

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Appendix

The basic relations between the electrical quantities of the I–V curve of a PV device (solar cell or module)—such as the ones shown in figure 8—are briefly recalled here [18].

For each point on the I–V curve, the product of the current and voltage (IV) represents the power output for that operating condition. The *maximum power point* (P_{max}) of the I–V curve corresponds to the maximum value of that product. That is when

$$d(I \cdot V)/dV = 0 \tag{A.1}$$

P_{max} is located on the knee of the I–V curve and the corresponding I and V values are defined as I_{mpp} and V_{mpp}, respectively.

The fill factor (FF) is a measure of the junction quality and parasitic resistances of a PV device and is defined by:

$$FF = (V_{mpp} \cdot I_{mpp})/(V_{oc} \cdot I_{sc}) \tag{A.2}$$

The nearer the FF to unity, the higher the quality of the cell (a value between 70% and 75% is considered good for commercially available solar modules, such as the ones tested in this work). This relation holds for P_{max}:

$$P_{max} = V_{oc} \cdot I_{sc} \cdot FF \tag{A.3}$$

where I_{sc} is the *short-circuit current* and V_{oc} the *open-circuit voltage* of the cell/module.

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