

A review on the mainstream through-silicon via etching methods

Haoming Guo^a, Shengbin Cao^{a,*}, Lei Li^a, Xiaofeng Zhang^b

^a School of Materials Science, Shanghai Dianji University, Shanghai, People's Republic of China

^b School of Mechanical Engineering, Shanghai Dianji University, Shanghai, People's Republic of China



ARTICLE INFO

Keywords:

Through-silicon via (TSV)

Etching methods

Wet etching

Laser drilling

DRIE

ABSTRACT

Currently, 3D integration is considered to be the most promising development direction for chip industry. It relies on the through-silicon via (TSV) structure to achieve mechanical and electrical interconnection in the vertical direction. The manufacturing of TSV is usually accomplished by etching technique, which can produce a hole with high aspect ratio by removing the material from a specific area physically or chemically. At present, the mainstream TSV manufacturing methods include KOH wet etching, laser drilling, deep reactive ion etching and photo-assisted electrochemical etching. However, a cross-sectional comparison of their characteristic was lacking in the literature. This review aims to provide a comprehensive summary for four kinds of mainstream TSV etching methods, i.e., KOH wet etching, laser drilling, deep reactive ion etching and photo-assisted electrochemical etching, including their etching mechanism, process, parameters and hole structure. Finally, this paper summarizes and prospects the four methods for TSV etching, providing researchers and engineers with an extensive and updated understanding of the principles and applications for these four mainstream TSV etching methods.

1. Introduction

In the past, Moore's Law guided integrated circuit (IC) industry towards a goal of low power and high performance [1]. However, it is difficult to improve IC performance by reducing feature size continually as the IC industry meets its turning point now. There will be many problems such as the decrease in thermal dissipation and the increase in leakage current and static power consumption when the size of complementary metal-oxide-semiconductor (CMOS) devices drops below 100 nm [2]. Fortunately, the emergence of three-dimensional integrated circuit (3D IC) solved these problems, which means multiple modules can be integrated into one system, effectively improved system integration level and performance while reducing power consumption, realizing the continuation of Moore's Law [3].

The concept of 3D IC was first proposed by William Shockley and Richard Feynman in the 1960s, aiming to stack multiple wafers vertically. The wafers are connected by vertical structures that allow transmission of electrical signals. William Shockley invented this vertical structure in 1958 and named it Through-Silicon Via (TSV) [4]. Communications between inter-layer chips are implemented through the internal conductor material (such as copper, tungsten or polysilicon) in the TSV.

At present, 3D IC is the mainstream method, making TSV become the dominion part of IC industry. Primarily, the vertical interconnection of circuits needs to be realized through TSV, which makes the vertical communication possible. Besides, TSV is necessary for the multichip connection vertically to achieve the multi-functional and improved performance in a limited area. Eventually, using TSV for vertical interconnection is an effective way to achieve the high-performance chip manufacturing under the background of the feature size cannot be reduced continually. Besides, the application of TSV structure in solid state disk (SSD) has been realized, which has greatly improved the capacity of SSD chips [5]. Now TSV is playing a pretty important role in the field of 3D IC, which is bringing compelling possibilities for the more powerful chips manufacturing.

Till now, TSV structure has developed a variety of shapes such as square, rectangle, cylinder, oval, etc., meeting different applications [6]. According to the different sequence of transistor manufacturing and metal interconnection processes, TSV can be divided into three types: Via-First, Via-Middle and Via-Last [7].

In the process of Via-First, TSVs are made before CMOS devices manufacturing, making efficient high aspect ratio TSV fabrication available. According to the interconnection sequence, this process can be divided into two types: front end of line (FEOL) and back end of line

* Corresponding author.

E-mail address: caosb@sdju.edu.cn (S. Cao).

(BEOL). FEOL process means using deep reactive ion etching to make holes before CMOS manufacturing, which cause more than 1000 °C on the wafer. To match the thermal coefficient of expansion, polycrystalline silicon is used for padding, which has high parasitic resistance [8]. BEOL process is basically the same as FEOL. The only difference between FEOL and BEOL process is that copper and tungsten are used for padding in the back end of line process [9]. Since high temperature is necessary in Via-First process, limiting the selection of filling materials, making the whole fabricate process must be designed together with IC wiring.

In the process of Via-Middle, TSVs are made between FEOL and BEOL. Wafers only need to be exposed at the temperature less than 400 °C during this process, making good mechanical properties available [10]. However, since the thermal coefficient of expansion for metal is much higher than silicon, the mechanical expansion may damage vertical structure during heating process.

In the process of Via-Last, TSVs are made after CMOS devices manufacturing, FEOL process and BEOL process. Laser drilling is used for etching in this procedure, then filling the hole by electroplating copper so as to complete the TSV manufacturing [11]. Although the temperature during BEOL process is about only 200 °C, which is much lower than Via-First and Via-Middle process, it is a complicate procedure. The multiple etching layers making it hard to achieve high aspect ratio.

No matter which method is used for TSV manufacturing, etching is

necessary. Since different etching methods determines the electrical and mechanical characteristic of TSV, it is significant to choose a suitable etching process for TSV fabrication. For example, KOH wet etching can achieve shallow TSV etching better, which means it is unworthy if we use DRIE for this purpose. This paper aims to help readers have a better understanding of the characteristics of the four TSV etching techniques.

Fig. 1 indicates the roadmap for four kinds of mainstream through silicon via etching methods. The roadmap can be grouped into two categories: wet etching and dry etching. For wet etching process, KOH wet etching was the mainstream silicon etching method before other techniques appear. With the feature of anisotropy etching, this method is capable of shallow hole manufacturing, using mask to prevent other areas from etching. However, the etching process changed when electric current and ultraviolet light were introduced into semiconductor etching process, which was called photo-assisted electrochemical etching (PAECE). Deep groove manufacturing is available by this method. Dry etching method appeared later for high aspect ratio TSV fabrication, using laser or plasma to remove materials. Both these two methods were born for vertical deep hole manufacturing, meeting the need of electrical connections in vertical direction. In the future, the mainstream TSV etching methods will go along these paths continually, which depends on the hole structure, aspect ratio and the cost during the etching process.

To date, there was no cross-sectional comparison for mainstream

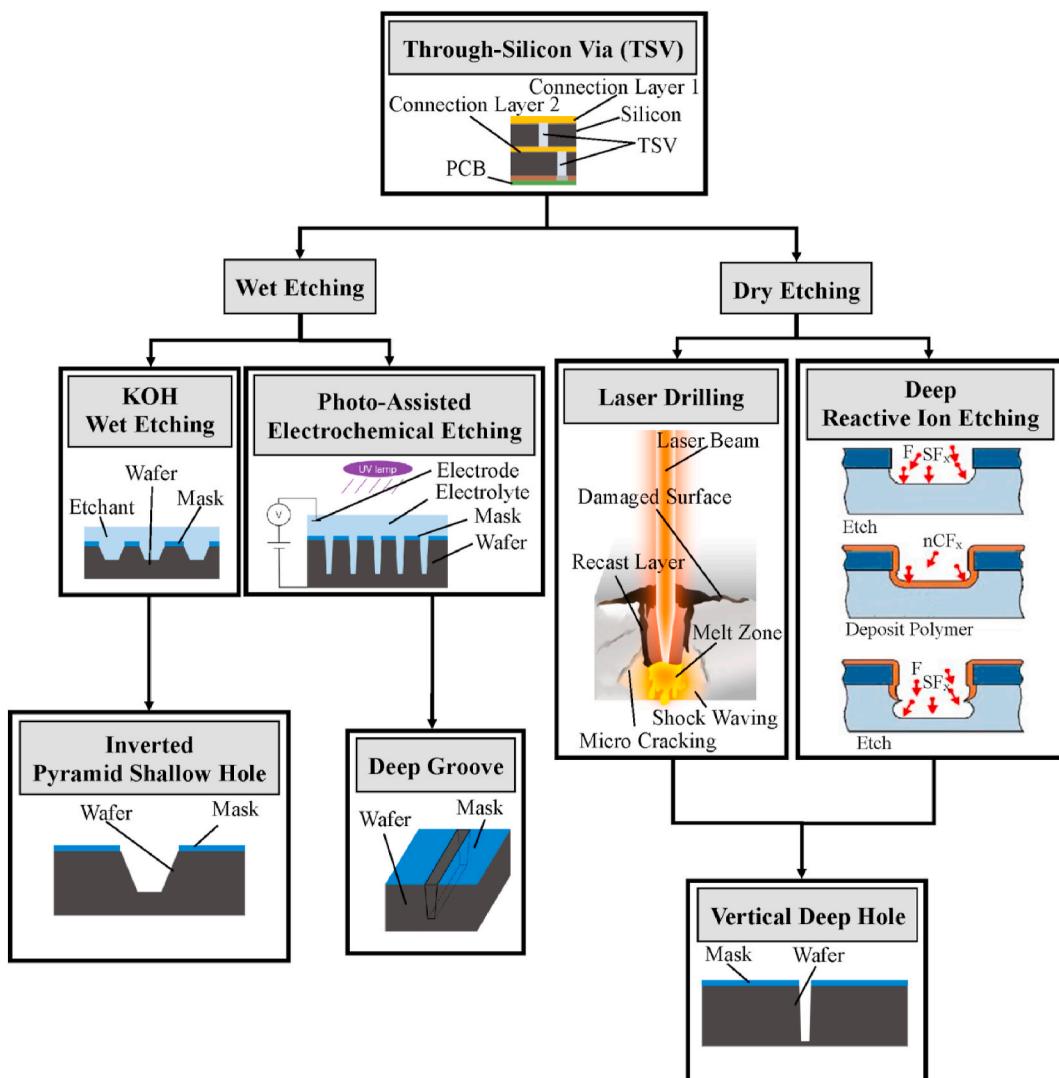


Fig. 1. Roadmap for four kinds of mainstream through silicon via etching methods.

TSV etching methods existed in the literature. The existing reviews for etching techniques only focus on single method. In this paper, four mainstream TSV etching methods are briefly reviewed, pointing out their difference and feasible development for semiconductor etching in the future. In the last section we summarize the characteristics of four mainstream TSV etching methods and the feasible improvement in the future.

2. Overview for four kinds of TSV etching methods

2.1. KOH wet etching

The mechanism of KOH wet etching is that potassium hydroxide solution reacts with silicon wafer, removing the material which is not protected by the mask. Chemical Equation (1) shows the reaction of KOH wet etching.



During this etching process, only silicon is removed and other materials on the substrate are not damaged, making anisotropic wet etching available [12]. Fig. 2 (a) is the concept graph of wet etching. The side wall of the hole etched by KOH solution is not vertical, which depends on the crystal orientation of wafer. For wet etching, there are other available agents, such as HNA solution [13] and TMAH solution [14]. Although KOH wet etching is usually used for micromachining in MEMS manufacturing for silicon cantilever beams or trapezoidal structure, it is not the best way to make high aspect ratio TSVs by this method. We consider this method in this topic is mainly because this is an efficient promising and low cost technique for wafer etching. KOH wet etching was also the only means of micro hole manufacturing before other etching methods appear [15]. Anisotropy is the main feature of KOH wet etching due to the use of potassium hydroxide [16]. Complex equipment is not necessary during the etching process, making low cost mass production available. Due to the use of wet chemical solution, there are no additional damage on the substrate, which is the main advantage. The only problem is that the K^+ in solution may contaminate the CMOS

devices that fabricated on the wafer before etching. In the past, some scholars tried to use plasma enhanced chemical vapor deposition to deposit a protective layer for protection [17], now another hard mask layer polydimethylsiloxane [18] is used to protect the CMOS device before wet etching, aiming to avoid ion pollution. The process of wet etching is mainly affected by temperature, stirring power, concentration and solution [19].

2.2. Laser drilling

Laser drilling (LD) is a physical etching method, using high energy laser to remove material from specified area [20]. During this process, heat affected zones are inevitable since the melt and evaporation of material needs high temperature caused by laser [21]. Fig. 2 (b) is the concept graph of laser drilling. The side wall of TSV made by laser drilling is almost vertical, making it feasible for high aspect ratio TSV manufacturing. This method is also available for precise brittle material etching because only the local material is melt during this process. However, the density of hole is limited because of the existence of heat affected zone [22]. Mask is not necessary during the laser drilling process, making it efficient and inexpensive. There were scholars tried to use a mask for splashing protection [23], which is a feasible way to prevent slag splashing. Currently, the feasibility research for the application of nanometer metal barrier layer in laser drilling process is ongoing, aiming to achieve the manufacturing of smaller micro via by laser [24]. The process of laser drilling is mainly affected by the exposure times, laser energy density and transmittance of material [25,26].

2.3. Deep reactive ion etching

Deep reactive ion etching (DRIE) was invented by Bosch, using SF_6 as a reactive gas to etch silicon while release C_4F_8 periodically as a passivation gas for side wall protection to achieve high aspect ratio vertical TSV etching [27]. The chemical equations are as follows [28]:

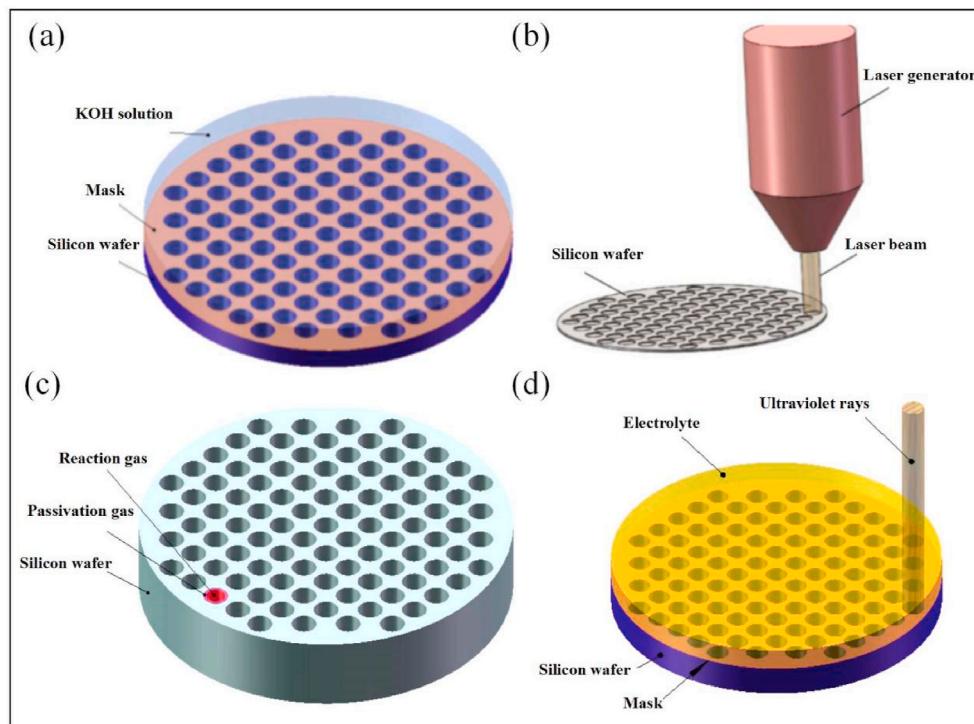
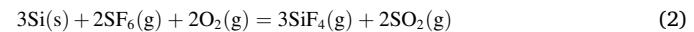


Fig. 2. Conceptual graphs of four methods (a) KOH wet etching (b) Laser drilling (c) Deep reactive ion etching (d) Photo-assisted electrochemical etching.



Fig. 2 (c) is the concept graph of DRIE. This method is mainly used for high aspect ratio vertical columnar structures etching, such as vertical cylindrical via on silicon substrates. Basically, DRIE is an inductively coupled plasma (ICP) etching method, which is a combination of physical and chemical removal of materials. The process of DRIE mainly affected by electrode power, reactant gas flow and the pressure of cavity.

2.4. Photo-assisted electrochemical etching

The mechanism of photo-assisted electrochemical etching (PAECE) is using ultraviolet light for electrochemical etching process enhancement, accelerating hole-electron pair generation to achieve high speed etching. **Fig. 2 (d)** is the concept graph of PAECE. The photo-assisted electrochemical etching is mainly used for the manufacturing of grooves with high aspect ratio, such as the capacitor structure in microelectromechanical systems [29]. Local material will be dissolve during the etching process because of the oxidization caused by electrochemistry while ultraviolet light will accelerate the oxidation reaction on the silicon surface, significantly improve the etching efficiency. PAECE is a sort of wet etching method since etchant is necessary, which may cause environmental contamination. The process of PAECE is mainly affected by the electrolyte solution, duration, voltage and illumination [30,31].

3. Comparison of four kinds of TSV etching methods

3.1. Etching mechanism

From the perspective of mechanism, etchant is necessary in both KOH wet etching and PAECE process, making chemical contamination possible. In KOH wet etching process, the H atoms on the surface of Si–H bonds are replaced by the OH⁻ ions, it is due to the OH⁻ ions have higher electronegativity of oxygen compared to hydrogen. This process oxidized the silicon atoms on the surface. Then the higher electronegativity of oxygen makes the Si–Si back bonds vulnerable, and the polar water molecules attack the weakened Si–Si back bonds, thus turning themselves into H⁺ and OH⁻ ions. Finally, the OH⁻ ions attach to the Si atoms those have been separated and the H⁺ ions attach to the Si atoms on the next layer of the substrate, forming the Si–H bonds, making the etching process complete [32]. The process is shown in **Fig. 3 (a)**.

In photo-assisted electrochemical etching, the oxidation process is different. Due to the existence of electric current, the Si–H bonds are broken via thermal decomposition, leaving two electrons in the conduction band of silicon. At this point, the negatively charged OH⁻ ion cannot attach to the silicon surface. The H₂O molecule on the Si surface will accept two electrons and dissociate into H⁺ and OH⁻ ions. These OH⁻ ions eventually attach to the Si atoms to form Si–OH bonds. Due to the photoelectric effect of semiconductors, the irradiation of ultraviolet light will produce additional electrons, thus accelerate the reaction. **Fig. 3 (b)** indicates the oxidation process of Si in photo-assisted electrochemical etching.

In the aspect of etching rate, 15 μm/min can be achieved by using boiling KOH (20 wt%) for wet etching [33]. Some scholars have used the PAECE process to achieve a maximum etching rate of about 10 μm/min [34,35].

On the contrary, laser drilling is a dry etching method, making it high efficiency and environmentally friendly. “Photothermal” and “photochemical” are the main mechanisms for laser drilling, the material removal process can be either one or a combination of two processes [36]. Photochemical process is often referred as a non-thermal process because of the separation of material is caused by the breaking of atomic bonds. However, in photothermal process, the absorbed laser energy is contribute to the vibration of the lattice, increasing the local temperature, making materials to be melt and evaporate. The mechanism of laser

drilling is shown in **Fig. 3 (c)**. TSV manufacturing speed has achieved 2000 holes per second by using laser drilling, which is increasing in the next decades [37].

DRIE is an etching process combining both physical and chemical methods. **Fig. 3 (d)** shows the etching mechanism of DRIE. The plasma gas is controlled by an electromagnetic field to bombard the surface of silicon wafer for material removal. The DRIE process can achieve a maximum etching speed of about 10 μm/min now [7]. **Table 1** compares the characteristics of four etching methods.

3.2. Etching process

From the perspective of etching process, KOH wet etching use etchant for micro hole manufacturing, making it sensitive to the temperature, which is the impact factor of local reaction rate, making overall etching process out of synchronism easily. At the same time, the heat released by local reaction also accelerates the local etching process, increasing the unevenness of etching process. It can be seen from chemical equation (1) that hydrogen is produced during the reaction, which may create micro masks, blocking the reaction from proceeding. In addition, accurate etching depth control is difficult for wet etching because the surface morphology of silicon wafer is affected by the flow of etchant. The structure of hole for KOH wet etching is related to the crystal orientation, making it not available for vertical high aspect ratio TSV etching. **Fig. 4** provides the variation of KOH wet etching rates with the concentration of KOH solution, ultrasonic stirring power and temperature. It can be found that the etching rate grows up when the temperature increase under the same concentration of KOH solution. It is also clear that both the etching rate and roughness rise up with the growth of ultrasonic stirring power [33]. The balance of etching rate and the roughness of surface is the key to this method.

For laser drilling, the high temperature caused by the laser may damage the material around the hole, which is called heat affected zone [53]. Therefore, these areas need to be reserved in advance in the process of design. Because of the existence of heat affected zone, many areas are wasted, which means laser drilling is not suitable for high density TSV manufacturing.

For DRIE, using plasma to bombard the wafer surface for vertical high aspect ratio TSV etching making the etching process efficient. Fluorine is the key to achieve good anisotropy and high etching rate [8]. The main advantage of DRIE is the good construability during the etching process due to its complex control system, making this method requires complex equipment. **Fig. 5 (a)** shows the variation of Si etching rate with the flux of fluorine radicals. It can be seen that the etching rate of Si increases as the rise in the flux of fluorine radicals. **Fig. 5 (b)** indicates that a hole with smaller diameter is easier to achieve the higher aspect ratio.

For PAECE, the N or P region of the P–N junction can be selectively etched by using different light intensity and change voltage bias on units and P–N junction [34]. During the etching process, etching rate can be controlled by adjusting the etching current or light intensity, making precision etching available.

3.3. Hole structure

From the perspective of hole structure, the side wall of KOH etching is not vertical since the etching direction depends on the crystal orientation of silicon wafer, making the window of hole larger than the bottom just like an inverted pyramid [57,58]. Although using this method can achieve an aspect ratio up to 600, this etching technique is limited by its non-vertical side wall feature [59].

Most of the holes made by the laser drilling are taper. In the meantime, substrate contamination and side wall carbonation residue may happen during the drilling process [60]. Currently, people can achieve TSV manufacturing for more than 100 aspect ratio by using laser drilling [61]. Compared with laser drilling, the side wall of TSV made by DRIE

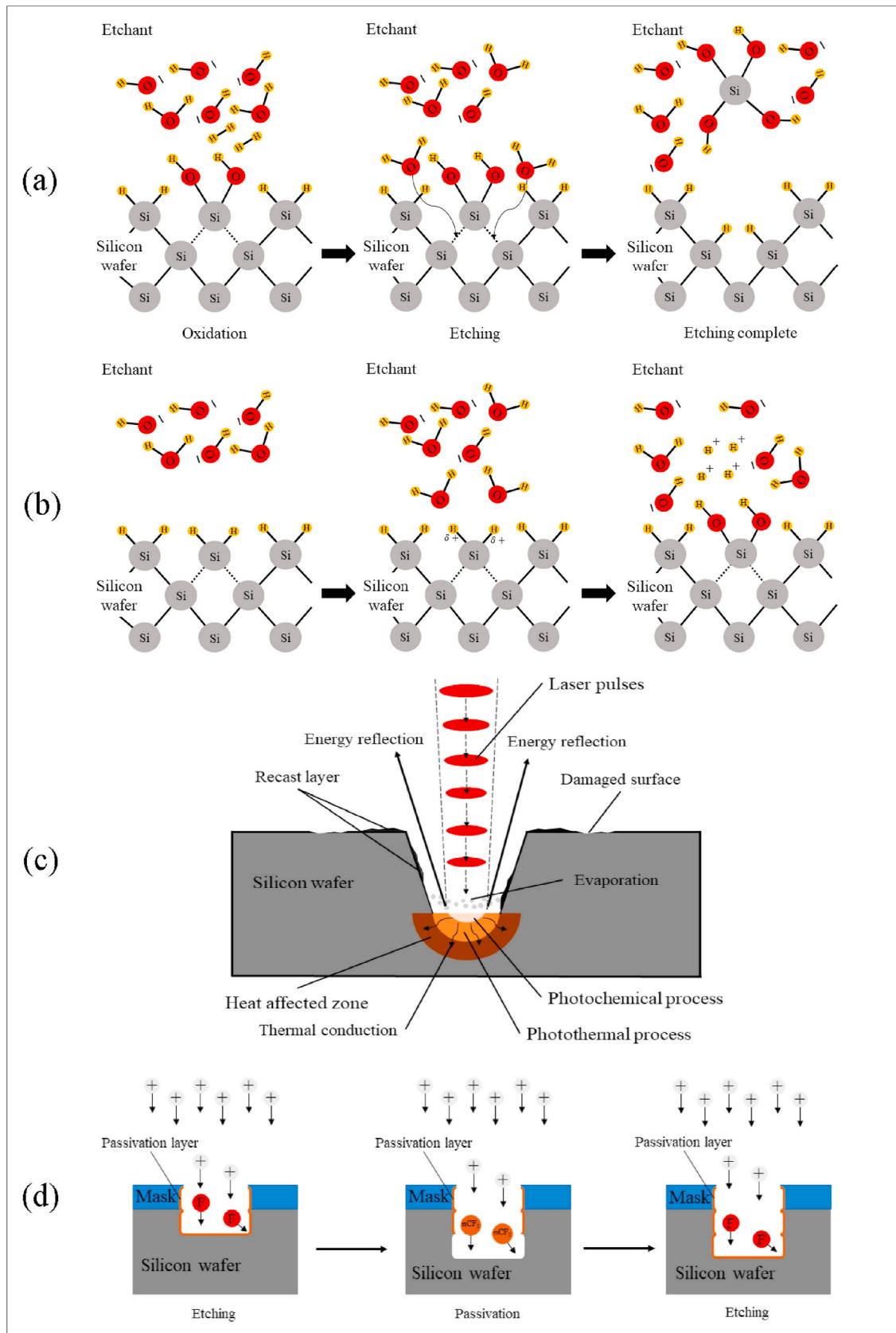


Fig. 3. The mechanism for four kinds of etching methods: (a) Etching mechanism of alkali solution [12]. (b) Oxidation mechanism in PAECE process [12]. (c) Material removal mechanism of laser drilling [38]. (d) Etching mechanism of DRIE.

Table 1

The main characteristics of four kinds of TSV etching methods.

Method	Advantages	Disadvantages	Factors
KOH Wet Etching	Anisotropy, Low cost, Simple equipment [39,40]	Microbubbles block the reaction, Difficult to control the etching depth, Side wall tilt [41, 42]	Temperature, Stirring power, Concentration [33]
Laser Drilling	Without mask, High efficiency, Positioning etching, High aspect ratio [37,43]	Substrate damage, Heat affected zone, Slag splashing, Side wall carbonation residue [22,44]	Exposure times, Laser energy [45,46],
DRIE	Anisotropy, Good controllability, Vertical side wall, High aspect ratio [47]	Scallop-shaped defects, High cost, Complex equipment, Ion damage [48–50]	Voltage, Gas flow rate, Pressure [28]
PAECE	Low cost, High efficient, Low temperature [51]	Be sensitive to temperature, Difficult to control the etching depth, Isotropy (acid electrolyte) [52]	Concentration, Current intensity, Etching time, Light intensity [30,31]

technique is smoother. There are less damage on the silicon wafer during this process since substrate contamination and side wall carbonation residue do not happen. Due to its unique etching process, DRIE technique is born for high aspect ratio TSV manufacturing [56,62]. However, the scallop-shaped defects that on the side wall cannot be avoid completely [50], and it became more severe as the increase of the etching rate, which affect the smoothness of dielectric layer [64]. Some scholars reported that they have successfully achieved 160:1 aspect ratio TSV manufacturing by using DRIE [56]. PAECE is available for high aspect ratio groove etching and there were some applications based on

this technique [63,64]. For grooves, the maximum aspect ratio can reach 120:1 [65].

Fig. 6 (a), (b) and (c) describe the etching depth and diameter for PAECE and laser drilling respectively. For PAECE, etching depth increase first and then stable at self-terminating depth as time goes up. It is also clear that the self-terminating depth is related to the light intensity, which is deeper when light intensity become more powerful. The diameters for both entrance and exit are mainly affected by total pulse energy during laser drilling process, which can be notice that when the total pulse energy exceed 3J, both entrance and exit diameters increase significantly while ratio of entrance and exit decrease.

Fig. 7 compares the morphology of the holes made by the four kinds of TSV etching methods. Fig. 7 (a) and (b) indicate the unique shape of the hole manufactured by KOH wet etching, which has the sharp edges and non-vertical side walls. Fig. 7 (b), (d) and (e) show three kinds of side wall damage for KOH wet etching, laser drilling and DRIE respectively, it is clear that the side wall of the hole etched by KOH wet etching has the best surface quality. By comparing Fig. 7 (c), (f) and (g), it is clear that the surface damage occurs during the laser drilling, DRIE and PAECE processes. The higher aspect ratios can be found in Fig. 7 (d), (e) and (g). Fig. 7 (g) and (h) show the groove made by the photo-assisted electrochemical etching.

3.4. Etching parameter

Table 2 compares the difference between four techniques in three key etching parameters. From the prospective of maximum etching rate, KOH wet etching was the dominant, followed by PAECE and DRIE. For the value of maximum aspect ratio, KOH wet etching is still the most competitive technique. Although KOH wet etching seems to be the most prospective means of TSV etching technique, it is not popular in TSV manufacturing industry now because of its non-vertical side wall. For major defects, side walls for both laser drilling and DRIE are damaged during the etching process, which cannot be completely eliminate, affecting the process of dielectric deposition in the next step. Fortunately, the current research on the removal of this defect has made

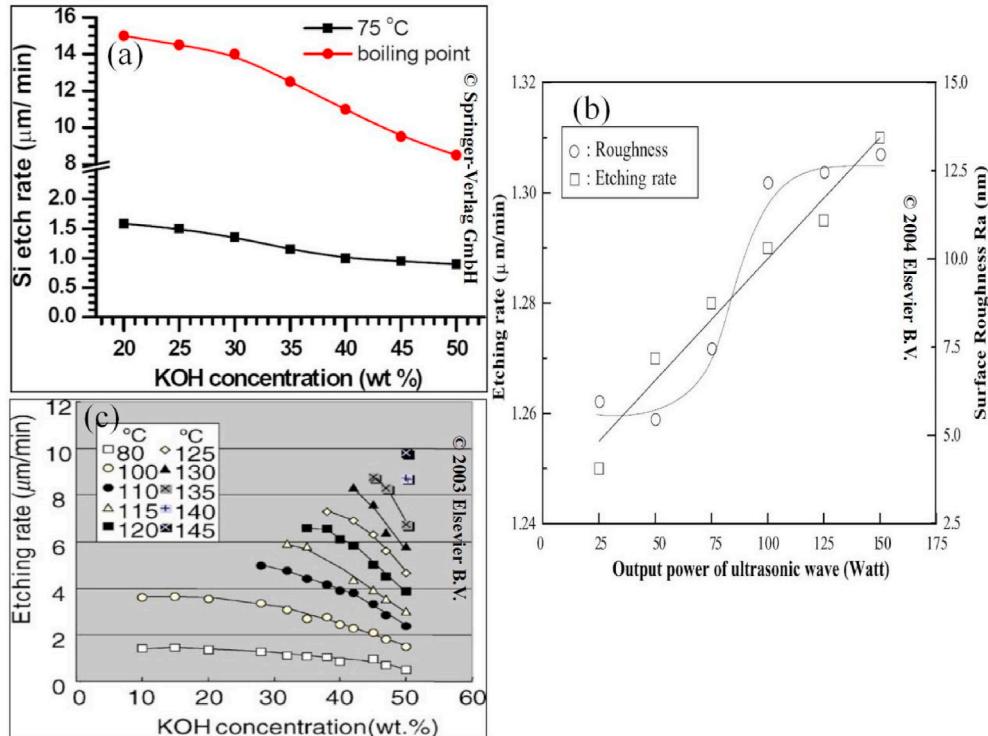


Fig. 4. The variation of the KOH wet etching rates with (a) ultrasonic stirring power [33], (b) concentration of KOH solution [54], and (c) temperature [55].

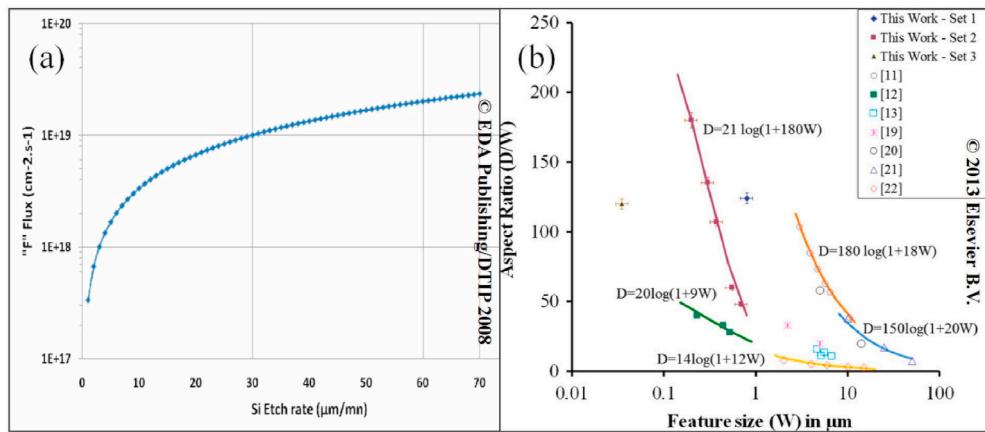


Fig. 5. Etching rate of DRIE affected by (a) fluorine radical flux [8], and (b) feature size [56].

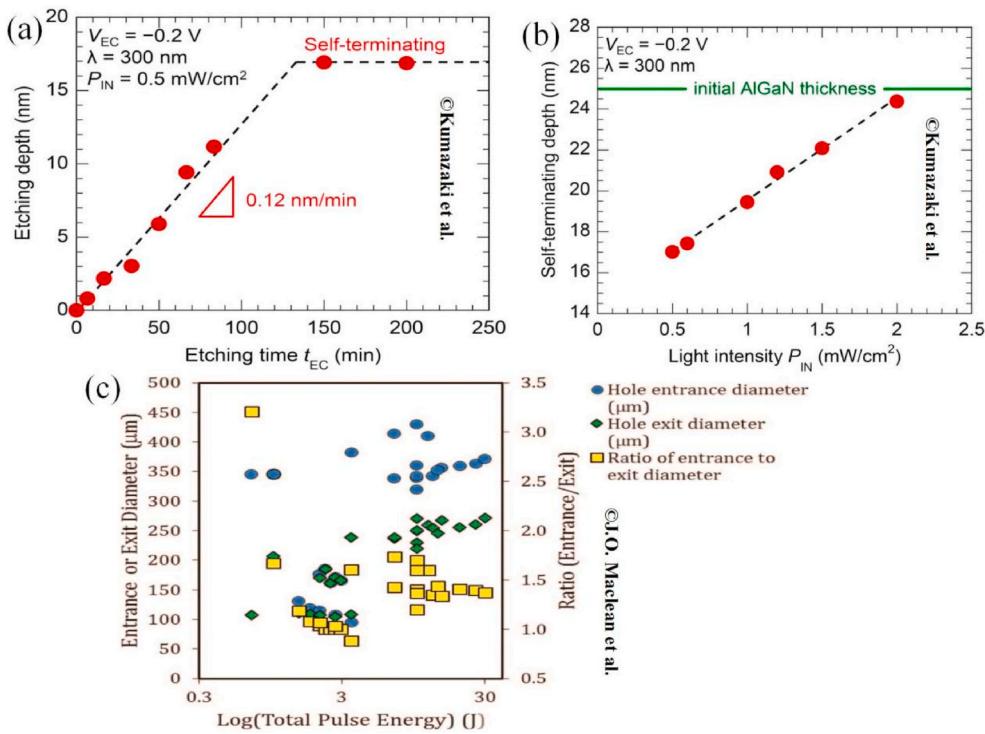


Fig. 6. Comparison for laser drilling and PAECE, (a) and (b) [63], (c) [66].

progress [71].

Although DRIE is the most controllable and promising means of TSV etching technique, the complex equipment makes it difficult to cut costs. This method has a moderate etching rate and being able to achieve high aspect ratio TSV etching. Otherwise, sidewall defects can be partly eliminated by improving the etching process. We can also control the amount of plasma bombarding on silicon surface by adjusting the electrode power. PAECE is another promising technique. The ultraviolet light enhances the generation of electron-hole pairs, accelerating the oxidation process and etching rate. This method is more suitable for groove etching rather than cylindrical structure, however, it also provides a new idea of manufacturing for future CMOS device such as capacitor.

4. Future development

In the near future, the four traditional etching techniques will still be

the mainstream, but the etching parameters will be optimized continually.

For wet etching, people are paying attention to the improvement of etching rate and hole structure. High-speed controllable wet etching will be the future. The improvement of etching solution is the core, and it has been noticed that adding NH_2OH to KOH can effectively increase the etching rate of silicon. Now it has been proved that when 15% NH_2OH is added in 20 wt % KOH, the etching rate is 4 times faster than the original under the same circumstance [73]. The laser-assisted method can also increase the local etching rate, which indicates that the external light can also accelerate the etching process, which may be related to the photoelectric effect of the semiconductor [74]. For the control of hole structure, some scholars have put forward a method of using "confinement mask" to control the etching depth, which makes the control of etching depth no longer depend on the control of etch period. The angle of sidewall can be also controlled by using different metal masks and different concentrations of hydrofluoric acid [57]. These new methods

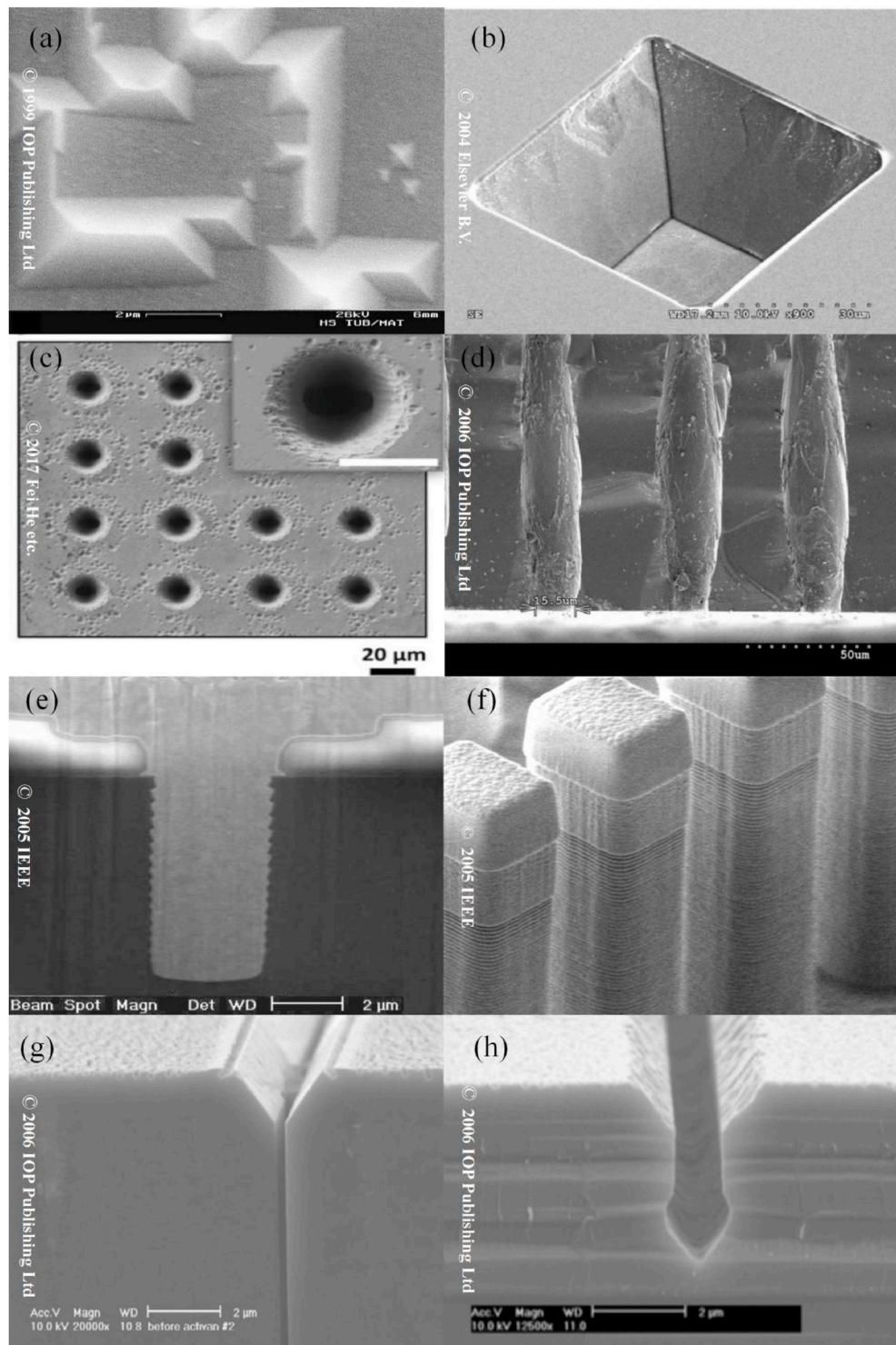


Fig. 7. Four types of hole structures. (1) KOH wet etching: (a) SEM micrograph of plateaus with rectangular micro pyramids at the transitions between neighboring plateaus [67]. (b) Defective microstructures resulting from ultrasonic agitation during the etching process [54]. (2) Laser drilling: (c) SEM images of TSVs fabricated in 100 μm-thick Si substrates [61]. (d) Holes drilled with 60 pulses of 168 μJ energy at a 60 kHz repetition rate [68]. (3) DRIE: (e) TEM picture of 6 μm deep silicon via after copper electroplating showing the sharp edges of the scallops formed during the deep RIE process. (f) Deep silicon trenches formed by combination of BOSCH/smooth etch process after dynamic parametric ramping process [69]. (4) Photo-assisted electrochemical etching: (g) SEM photograph of the results according to the light intensity. (h) SEM photographs of the etching result for different DC biases in the case of DMF-based 5% HF solution [70].

fill the blank of poor control of wet etching, which indicates that the modification of local etching morphology can be achieved through changing local reactant concentration. In addition, we consider that replacing the solvent of KOH solution or using modified etching solution is another feasible direction for improving the wet etching process, because we already have study like this on metal assisted chemical etching (MACE) process [75]. In conclusion, we believe that the future development of wet etching should focus on the design of chemical reaction between solution and materials, the intervention of external energy and the control of local reactant concentration during the etching

process, so as to improve the etching rate and achieve a better control of hole structure. In the future, it is possible to use laser and ultrasonic vibration with a micro metal mask to make high speed controllable wet etching come true.

For laser drilling, avoiding thermal damage is always the priority, harmless laser drilling will be the future. In addition, existing study shows that the emergence of top-hat beam technology has already realized a better cylindricity [60]. If this process can be improved to achieve a deeper etching depth in the future, it may replace other high aspect ratio TSV manufacturing processes. At the same time, it has been

Table 2

Comparisons of the key etching parameters.

Etching parameters	Maximum Etching rate	Maximum Aspect ratio	Major defects
KOH Wet Etching	15 $\mu\text{m}/\text{min}$ [33]	600:1 [59]	Non-vertical side wall, Low etching rate
Laser drilling	2000 vias/sec [37]	\	Slag splashing, Side wall carbonation residue
DRIE	10 $\mu\text{m}/\text{min}$ [7]	107:1 [72]	Scallop-shaped defects
PAECE	10 $\mu\text{m}/\text{min}$ [34, 35]	125:1 [70]	Difficult to control the etching depth

found that different media may be used to achieve different etching effects. There was a team compared the laser drilling effect of air medium and water medium. They found that the change of water layer thickness and laser focus would affect the roundness of hole, the taper of side wall and the depth of hole [76]. There were also researchers using water-assisted femtosecond laser etching achieved high quality holes without crack, splash and heat affected zones [77]. In addition, the drilling mechanism of water-assisted femtosecond laser on alumina ceramics has been studied, and it has been proved that both the drilling efficiency and the quality of the holes have been significantly improved [78]. Modifying the characteristics of the laser source is another way to reduce the defects of the hole. Z-L. Li and his team successfully achieved blind hole etching with small taper and flat bottom by using modified Gaussian laser beam, and there were no obvious defects in the hole [79]. It has also been proposed to use a deep ultraviolet laser with high peak power as a light source to reduce the heat-affected zone. In addition, the combination of nanosecond laser and picosecond laser drilling is also considered to be a feasible means for reducing the aperture (increase the aspect ratio) and eliminating cracks [80]. In conclusion, we believe that the future of laser drilling will be the improvement of optical medium and alternate drilling with different laser frequencies. Because the types of lasers are limited, changing light source may not be the best solution to reduce the heat affected zone. Therefore, step-by-step ultrafast laser drilling using liquid media may be a feasible approach to achieve high-speed, high aspect ratio, and low defect TSV manufacturing.

From the perspective of etching process, DRIE has good controllability, but the problem of side wall defect still needs to be solved. In the future, the core of DRIE improvement will be the elimination of side wall defects, which has already been studied by some researchers [83,84]. The development of PAECE should focus on the control of the etching position. Although the PAECE technique has been used in the past to manufacture high aspect ratio grooves as an experiment, it is now commonly used to manufacture porous semiconductors [81,82]. In order to achieve a controllable groove etching process we may need to change the electrode placement and lighting condition.

In terms of new etching technologies, the future development will mainly focus on chemical or physical-chemical combination to achieve TSV etching, and the traditional single etching mode will be gradually abandoned. For example, there were researchers use magnetic field to attract metal catalysts deposited on silicon surface to achieve a faster etching rate in high aspect ratio grating structure manufacturing [85]. At the same time, the emergence of new etching technology will provide the conditions for the finer TSV manufacturing. With the improvement of the integrated circuits, the feature size and the diameter of TSV decreases continuously. The traditional TSV etching processes will not be able to meet the requirements when the feature size of IC less than 3 nm in the future, so people need new etching technology to achieve the manufacturing of TSV. Thermal Atomic Layer Etching is that feasible solution to achieve atomically accurate material removal and realize TSV manufacturing in a very small scale [86,87].

5. Conclusions

This review summarized the researches of mainstream semiconductor etching methods for TSV manufacturing. The mechanism of KOH wet etching, laser drilling, deep reactive ion etching, photo-assisted electrochemical etching and the factors that influence the etching process and hole structure were expounded in detail. The hole structure is determined by etching methods: KOH wet etching is promising in shallow hole manufacturing, PAECE is capable of deep groove fabrication and both laser drilling and DRIE techniques are suitable for making high aspect ratio vertical deep holes. Scientific evaluation of the different TSV etching methods will be helpful for researchers to have a better understanding of these methods. At the same time, the defects of each hole structure manufactured by these four methods are pointed out which should be paid attention to in the further studies. Moreover, we compared key etching parameters for these four etching techniques so as to make a cross-sectional comparison for the features of these four mainstream TSV etching methods, laying a foundation for researchers and engineers to carry out the follow-up studies. The future research directions are also listed base on the latest research. These four kinds of semiconductor etching methods will be the main TSV etching technique continually. There are many modifications for the etching process so as to eliminate defects and achieve the goal of specific hole structure, which is a feasible direction for the future. At the same time, the emergence of new techniques such as metal-assisted chemical etching and atomic layer etching may realize the manufacturing for smaller TSVs. In a word, the guidelines are described in the review, which promote the development and application of the four kinds of mainstream TSV etching methods.

Author statement

I have made substantial contributions to the conception or design of the work; or the acquisition, analysis, or interpretation of data for the work; AND I have drafted the work or revised it critically for important intellectual content; AND I have approved the final version to be published; AND I agree to be accountable for all aspects of the work in ensuring that questions related to the accuracy or integrity of any part of the work are appropriately investigated and resolved.

All persons who have made substantial contributions to the work reported in the manuscript.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This work is supported by the Open Project of the State Key Laboratory of Non-ferrous Metal Material Preparation and Processing (No:19AZ02).

References

- [1] G.E. Moore, Electronics 114 (1965) 117.
- [2] K. Seshan, Chapter 2 - limits and hurdles to continued CMOS scaling, handb. Thin Film Deposition, fourth ed., 2018, pp. 19–41.
- [3] Z. Wang, J. Microelectromech. Syst. 24 (2015) 1211–1244.
- [4] S. William, US Pat, 1962.
- [5] K. Parat, C. Dennison, IEEE Int. Electron Devices Meet (2015) 3.
- [6] I.H. Jeong, A. Eslami Majd, J.P. Jung, N.N. Ekere, Metals 10 (2020) 467.
- [7] W.-W. Shen, K.-N. Chen, Nanoscale Res. Lett. 12 (2017) 1–9.
- [8] M. Puech, J.-M. Thevenoud, J.M. Gruffat, N. Launay, N. Arnal, P. Godinat, Proc. DTIP MEMS and NOEMS (2008) 109–114.
- [9] D.H. Triyoso, T.B. Dao, T. Kropewnicki, F. Martinez, R. Noble, M. Hamilton, Integrated Circuit Design and Technology, 2010, pp. 118–121.
- [10] E. Beyne, IEEE Trans. Compon. Packag. Manuf. Technol. 6 (2015) 983–992.

- [11] M. Aoki, F. Furuta, K. Hozawa, Y. Hanaoka, H. Kikuchi, A. Yanagisawa, T. Mitsuhashi, K. Takeda, Proc. IEDM. (2013) 25–29.
- [12] P. Pal, V. Swarnalatha, A.V.N. Rao, A.K. Pandey, H. Tanaka, K. Sato, Micro Nano Syst. Lett. 9 (2021) 1–59.
- [13] T. Guan, F. Yang, W. Wang, P. Liu, Z. Fan, L. Cheng, Z. Chen, R. Yu, Q. Zhao, D. Zhang, Conf. Nano/Micro Eng. Mol. Syst. (2018) 397–400.
- [14] X. Cheng, Y. Li, H. Liu, Y. Zan, Y. Lu, Q. Zhang, J. Li, A. Du, Z. Wu, J. Luo, J. Mater. Sci. Mater. Electron. 31 (2020) 22478–22486.
- [15] K.E. Bean, IEEE Trans. Electron. Dev. 25 (1978) 1185–1193.
- [16] M. Tautz, A. Weimar, C. Graßl, M. Welzel, D. Díaz Díaz, Phys. Status Solidi 217 (2020) 2000221.
- [17] J. Han, Y.J. Yin, D. Han, L. Dong, Mater. Res. Express 4 (2017) 96301.
- [18] S. Gupta, A. Vilouras, R. Dahiya, Microelectron. Eng. 221 (2020) 111157.
- [19] P. Pal, K. Sato, Micro Nano Syst. Lett. 3 (2015) 1–42.
- [20] J.O. Maclean, J.R. Hodson, K.T. Voisey, Proc. SPIE (2015), 965704-1–6.
- [21] Y. Liu, R. Zhang, W. Li, J. Wang, X. Yang, L. Cheng, L. Zhang, Int. J. Adv. Manuf. Technol. 96 (2018) 1795–1811.
- [22] C. Wang, Q. Wang, Q. Qian, B. Di, IOP Conf. Ser. Mater. Sci. Eng. (2020) 22067.
- [23] C.C. Ho, Y.H. Luo, Y.J. Chang, J.C. Hsu, C.L. Kuo, J. Laser Micro/Nanoeng. 11 (2016) 41.
- [24] F. Liu, R. Zhang, G. Khurana, B.H. Deprospo, R.R. Tummala, M. Swaminathan, IEEE Trans. Compon. Packag. Manuf. Technol. 10 (2020) 1411–1418.
- [25] H.-J. Wang, T. Yang, J. Eur. Ceram. Soc. 41 (2021) 4997–5015.
- [26] S. Sarfraz, E. Shehab, K. Saloniatis, Adv. Transdisciplin. Eng. 6 (2017) 51–56.
- [27] F. Laermer, A. Schilip, US Pat, 1996.
- [28] F. Laermer, S. Fransila, L. Sainiemi, K. Kolari, Handb. Silicon Based MEMS Mater. Technol., third ed., 2020, pp. 417–446.
- [29] Y. Lei, X. Liu, J. Li, J. Guo, H. Niu, J. Micromech. Microeng. 26 (2016) 65011.
- [30] K.P. Beh, F.K. Yam, L.K. Tan, S.W. Ng, C.W. Chin, Z. Hassan, Jpn. J. Appl. Phys. 52 (2013), 08JK03.
- [31] S. Yaakob, M.A. Bakar, J. Ismail, N.H.H.A. Bakar, K. Ibrahim, J. Phys. Sci. 23 (2012) 17–31.
- [32] M.A. Gosálvez, Helsinki Univ Technol (2003) 8–9.
- [33] S. Dutta, N. Gupta, I. Yadav, R. Pal, K.K. Jain, D.K. Bhattacharya, R. Chatterjee, Microsyst. Technol. 25 (2019) 3091–3096.
- [34] R. Micak, H.L. Tuller, P. Greiff, J. Sohn, Proc. - IEEE Int. Conf. Micro Electro Mech. Syst. (MEMS) (1993) 225–229.
- [35] R. Micak, H.L. Tuller, P. Greiff, J. Sohn, L. Niles, Sens. Actuators, A A. 40 (1994) 49–55.
- [36] W.W. Duley, Cambridge Univ Press (2005) 78–80.
- [37] R. Rieske, R. Landgraf, K.J. Wolter, Electron. Compon. Technol. Conf. (2009) 1139–1146.
- [38] J.-P. Desbiens, P. Masson, Sens. Actuators A Phys 136 (2007) 554–563.
- [39] A.V.N. Rao, V. Swarnalatha, P. Pal, Micro Nano Syst. Lett. 5 (2017) 1–9.
- [40] A.V.N. Rao, V. Swarnalatha, A. Ashok, S.S. Singh, P. Pal, ECS J. Solid State Sci. Technol. 6 (2017) 609.
- [41] H. Ekinci, R.K. Dey, B. Cui, J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom. 37 (2019) 62001.
- [42] J. Wang, F. Zhong, H. Liu, L. Zhao, W. Wang, X. Xu, Y. Zhang, H. Yan, Sol. Energy 221 (2021) 114–119.
- [43] H. Uchtmann, C. He, A. Gillner, J F. Dorsch, S. Kaierle, H. Uchtmann, C. He, A. Gillner, Int. Soc. Opt. Photon. 9741 (2016) 974106.
- [44] H. Zhu, Z. Zhang, K. Xu, J. Xu, S. Zhu, A. Wang, H. Qi, Materials 12 (2019) 41.
- [45] P. Laakso, R. Penttilä, P. Heimala, J. Laser Micro/Nanoeng. 5 (2010) 273–276.
- [46] X. Lv, Y. Pan, Z. Jia, Z. Li, X. Ni, AIP Adv. 8 (2018) 55025.
- [47] K. Booker, Y.O. Mayon, C. Jones, M. Stocks, A. Blakers, J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom. 38 (2020) 12206.
- [48] T. Xu, Z. Tao, H. Li, X. Tan, H. Li, Adv. Mech. Eng. 9 (2017), 1687814017738152.
- [49] A. Alsolami, A. Zaman, I.F. Rivera, M. Baghelani, J. Wang, IEEE Sens. Lett. 2 (2018) 1–4.
- [50] J. Fu, J. Li, J. Yu, R. Liu, J. Li, W. Wang, W. Wang, D. Chen, Mater. Sci. Semicond. Process. 83 (2018) 186–191.
- [51] T. Sato, M. Toguchi, ECS Meet. Abstr., IOP Publishing., 2020, p. 1223.
- [52] R. Radzali, M.Z. Zakariah, A. Mahmood, A.F.A. Rahim, Z. Hassan, Y. Yusof, AIP Conf. Proc. 1875 (2017) 20003.
- [53] L.S. Jiao, S.K. Moon, E.Y.K. Ng, H.Y. Zheng, H.S. Son, Appl. Phys. Lett. 104 (2014) 1–5.
- [54] C.R. Yang, P.Y. Chen, Y.C. Chiou, R.T. Lee, Sens. Actuators, A A. 119 (2005) 263–270.
- [55] H. Tanaka, S. Yamashita, Y. Abe, M. Shikida, K. Sato, Sens. Actuators, A A. 114 (2004) 516–520.
- [56] J. Parasuraman, A. Summanwar, F. Marty, P. Basset, D.E. Angelescu, T. Bourouina, Microelectron. Eng. 113 (2014) 35–39.
- [57] R. Kirchner, V. Neumann, F. Winkler, C. Strobel, S. Völkel, A. Hiess, D. Kazazis, U. Küntelmann, J.W. Bartha, Small 16 (2020) 2002290.
- [58] M.D. Kumar, H. Kim, J. Kim, Sol. Energy 117 (2015) 180–186.
- [59] B. Wu, A. Kumar, S. Pamarthi, J. Appl. Phys. 108 (2010).
- [60] V. Nasrollahi, P. Penchev, A. Batal, H. Le, S. Dimov, K. Kim, J. Mater. Process. Technol. 281 (2020) 116636.
- [61] F. He, J. Yu, Y. Tan, W. Chu, C. Zhou, Y. Cheng, K. Sugioka, Sci. Rep. 7 (2017) 1–9.
- [62] Y. Tang, A. Sandoughsaz, K.J. Owen, K. Najafi, J. Microelectromech. Syst. 27 (2018) 686–697.
- [63] Y. Kumazaki, K. Uemura, T. Sato, T. Hashizume, J. Appl. Phys. 121 (2017) 184501.
- [64] H.-C. Kim, H. Kwon, J. Korea Inst. Information, Electron. Commun. Technol. 9 (2016) 155–161.
- [65] G. Sun, J.I. Hur, X. Zhao, J. Microelectromech. Syst. 20 (2011) 876–884.
- [66] O.J. Maclean, J.R. Hodson, C. Tangkijcharoenchai, S. Al-Ojaili, S. Rodsavas, S. Coomber, K.T. Voisey, Laser Eng. 39 (2018) 1–2.
- [67] H. Schröder, E. Obermeier, A. Steckenborn, J. Micromech. Microeng. 9 (1999) 139–145.
- [68] B. Tan, J. Micromech. Microeng. 16 (2005) 109.
- [69] N. Ranganathan, K. Prasad, N. Balasubramanian, Z. Qiaoer, S.C. Hwee, Electron. Compon. Technol. Conf. 1 (2005) 343–348.
- [70] H.C. Kim, D.H. Kim, K. Chun, J. Micromech. Microeng. 16 (2006) 906–913.
- [71] Z.A.S. Mohammed, M.A.S. Olampo, D.P. Poenar, S. Aditya, Mater. Sci. Semicond. Process. 63 (2017) 83–89.
- [72] F. Marty, L. Rousseau, B. Saadany, B. Mercier, O. François, Y. Mita, T. Bourouina, Microelectron. J. 36 (2005) 673–677.
- [73] A.V.N. Rao, P. Pal, A.K. Pandey, P.K. Menon, H. Tanaka, K. Sato, Symp. Des. Test, Integr. Packag. MEMS MOEMS. (2020) 1–5.
- [74] K.P. Luong, R. Tanabe-Yamagishi, N. Yamada, Y. Ito, Int. J. Electr. Mach. 25 (2020) 7.
- [75] R. Guo, Q. Huang, S. Wang, J. Xu, J. Cao, H. Lin, J. Phys.: Conf. Ser. 1549 (2020) 32065.
- [76] E.G. Zahrani, B. Azarhoushang, J. Wilde, A. Zahedi, Procedia CIRP 95 (2020) 938–943.
- [77] W. Wang, H. Song, K. Liao, X. Mei, Int. J. Adv. Manuf. Technol. 112 (2021) 553–562.
- [78] N. Ren, K. Xia, H. Yang, F. Gao, S. Song, Ceram. Int. 47 (2021) 11465–11473.
- [79] Z. Li, O. Allegre, W. Guo, W.Y. Gao, B.H. Li, Q.L. Feng, X.P. Wu, L. Li, Laser Eng. (2020) 367–381.
- [80] X. Jia, Y. Chen, H. Wang, G. Zhu, X. Zhu, Opt. Laser. Technol. 130 (2020) 106351.
- [81] N.S. Mohd Razali, A.F. Abd Rahim, R. Radzali, A. Mahmood, J. Electr. Electron. Syst. Res. 18 (2021) 84–88.
- [82] O. Volovlikova, S. Gavrilov, P. Lazarenko, Micromachines 11 (2020) 199.
- [83] J.S. Park, D.-H. Kang, S.M. Kwak, T.S. Kim, J.H. Park, T.G. Kim, S.-H. Baek, B. C. Lee, Micro Nano Syst. Lett. 8 (2020) 1–8.
- [84] S. Frasca, R.C. Leghziel, I.N. Arabadzhiev, B. Pasquier, G.F.M. Tomassi, S. Carrara, E. Charbon, Sci. Rep. 11 (2021) 1–6.
- [85] T.K. Kim, J.-H. Bae, J. Kim, Y.-C. Kim, S. Jin, D.W. Chun, ACS Appl. Electron. Mater. 2 (2020) 260–267.
- [86] S.M. George, Acc. Chem. Res. 53 (2020) 1151–1160.
- [87] K.J. Kanarik, S. Tan, R.A. Gottscho, J. Phys. Chem. Lett. 9 (2018) 4814–4821.