Applied Physics A (2024) 130:303
https://doi.org/10.1007/s00339-024-07451-5

Applied Physics A
Materials Science & Processing

Metal–semiconductor junction in silicon nanostructures: role of interface traps

Sudipta Chakrabarty[1,2] · Suman Santra[1] · Syed Minhaz Hossain[1]

Received: 20 September 2023 / Accepted: 12 March 2024 / Published online: 13 April 2024

Abstract
Silicon nanostructures have been prepared on Si wafer using electrochemical etching process. The transformation of aluminum/nanostructured Si junction from Schottky to Ohmic nature has been observed by varying the annealing temperature. This phenomenon has been explained by the temperature dependent shifting of energy levels of defects states instrumental in trapping charges within the forbidden band gap of Si nanostructures. The Aluminum (Al)/nano-Si junction shows asymmetric nature at room temperature and then changes to ohmic at moderate annealing temperature. Finally, at high temperature the junction becomes rectifying in nature. This transition has been explained on the basis of Fermi level pinning due to the modification of distribution of the non-stoichiometric silicon oxide related defect states present at the nanocrystalline Si core-oxide shell interface.

Keywords Silicon · Nanostructure · Surface states · Interfacial traps

1 Introduction

To study the electrical transport properties of a material, establishing metal contact is the first and foremost requirement. The conditions for obtaining ohmic or rectifying metal contact are primarily dependent on the relative work function of the metal and the semiconductor as well as the type of the semiconductor as discussed in standard text books [1]. Though the transport properties of charge carriers for bulk semiconductors are dependent on the properties like the band gap, carrier mobility, defect density, carrier concentration etc. at a given temperature, the final electrical output is grossly dependent on the metal contact at the surface [2]. Hence, for bulk semiconductor the quality of the surface plays important role in determining the I–V characteristics of a piece of semiconductor. But the scenario becomes very crucial when the system under consideration has dimension in the nanoscale leading to very large surface to volume ratio [3–5]. Due to quantum confinement effect the band gap and hence the semiconductor work-function becomes a function of system size [6–8]. Consequently, the quality or the nature of the metal-nano semiconductor contact becomes size dependent [4, 7, 9–11]. Also, the surface/interface states that arise due to the dangling bonds of the semiconductor, controls the pinning of fermi level at the surface owing to enormous surface to volume ratio. Hence, the band bending at the interface is determined by the density and location of the surface states that affect the characteristics of metal/semiconductor junction in case of nanostructured semiconductor [12].

It has been a challenge to study the electronic properties of nanocrystalline Si with establishment of ohmic metal contacts due to inherent structural and surface morphological complexities. Although some works dealing with different metal contacts on silicon nanostructure (SiNS) have been published [13, 14], still there is no comprehensive literature exists that states clearly the role of interface trap states in forming an ohmic or a rectifying contact under suitable conditions specially for low dimensional systems.

The charge transport through Silicon nanostructures exhibits fascinating I–V characteristics like asymmetric

Sudipta Chakrabarty and Suman Santra contributed equally to this work.

✉ Syed Minhaz Hossain
shminhaz@physics.iiests.ac.in

[1] Department of Physics, Indian Institute of Engineering Science and Technology, Shibpur, Howrah 711103, West Bengal, India

[2] Department of Physics, Brainware University, Barasat, Kolkata 700125, West Bengal, India

[15, 16], hysteretic [5, 17], non-linear [18], and exhibit resistive switching [17, 19–22]. Different charge transport mechanisms dominate at different range of temperature and bias. Fowler–Nordheim tunnelling through the oxide barrier, Pool–Frenkel emission and trap controlled space-charge-limited conduction are the observed mode of charge transport [5, 18, 22–28]. Silicon nanostructures have a huge surface to volume ratio and hence contain a lot of surface states unless passivated suitably [7, 29–31]. Due to the reduced size the surface of silicon nanostructure becomes chemically reactive [32] and hence, gets oxidized easily leading to formation of a core–shell nanostructure [7]. The core–shell nanostructures are very popular for their interesting properties like semiconductivity, metallicity, magnetism etc., where the dominant role is played by either shell or core materials or from both [33–35]. However, freshly prepared silicon nanocrystalline core gets easily oxidised in ambient air leading to development of a nonstoichiometric oxide shell around it [6, 7, 36]. The core–shell interface is enriched with high density of defects/surface states [5, 16, 22, 26, 37, 38].

It is well-known that a metal–semiconductor junction with high concentration of surface/interface states may behave in a very different way than a metal-bulk semiconductor junction [1, 10, 37]. Whether the contact will behave like a Schottky junction or an ohmic junction depends on the relative position of the Fermi level and the work functions of the semiconductor and the metal respectively [1, 10]. It is also well-known that the position of the Fermi level near the junction depends largely on the quality of the interface [1, 10]. For low density of interface defect states the nature of the junction is determined primarily by the type (p or n) and density of the dopant atoms [39]. On the other hand, for a semiconducting surface like porous Si with large surface to volume ratio can have a lot of mid-gap defect states at the metal–semiconductor interface [40–43]. Concentration and location of these states determine the position of the Fermi level and hence the nature of the junction [12].

In this work, several Si nanostructures have been prepared using electrochemical etching of p-Si wafer using the well-known technique described elsewhere [32, 38, 44]. Aluminium contact pads of thickness ~ 100 nm have been deposited by thermal evaporation in vacuum (~10^{-6}mbar) chamber on the top of the SiNS layer. I–V characteristics of the device have been studied in top–bottom geometry. In this geometry, the contacts are taken from the top aluminium pad on nanostructured Si layer and the bottom aluminium layer (already deposited for electrochemical etching) below the p-Si substrate.

Annealing temperature has been varied from room temperature to 500 °C in inert (nitrogen) environment. I–V measurements have been performed after each annealing step. Significant variation of the contact from non-ohmic to nearly symmetric and then to rectifying nature has been observed. An optimised annealing temperature has been obtained where the I–V characteristics show nearly symmetric nature and the contacts behave almost like an ohmic one for a small range of applied bias. If the annealing temperature is raised further then the characteristics becomes rectifying in nature. To investigate the effect of annealing on the chemical bonds and effective optical band gap of the nanostructures, FTIR and PL studies have been employed after each annealing step. The modification of I–V characteristics has been explained on the basis of Fermi level pinning due to surface/interface states and its variation as a function of annealing temperature.

2 Experimental

Si nanostructures have been synthesized using electrochemical etching technique on electro-polished, (100), B doped, p-Si wafer of resistivity ~ 8–10 Ω-cm with aluminium (Al) coating at its back side. The electrochemically synthesized samples contain silicon nanostructures embedded in non-stoichiometric silicon oxide matrix [22, 32, 40, 44]. Current density has been varied between 10 and 20mA/cm^2 while the etching time has been kept fixed at 5 min for all the samples. The concentration of electrolyte solution (24% HF and Ethanol (Merck) taken in 1:1 volumetric ratio) has also been kept fixed. Thickness and porosity of the synthesized layers have been measured by gravimetric method [5, 26, 44, 45] using a digital balance (METTLER TOLEDO ME204). The detailed procedure of these studies are reported elsewhere [22].

X-ray diffraction (XRD) (Bruker D8 advance) and Atomic Force Microscopy (AFM) (Veeco DI CP II) have been performed for the structural characterization of the Si nanostructured layer. Chemical characterisation of the samples has been performed using Fourier Transform Infrared spectroscopic (FTIR) (Shimadzu IRAffinity 1S) analysis. Photoluminescence (PL) emission spectrometer (Avantes Ava-spec) was employed to get an idea about the average optical band gap of the samples.

Aluminum metal pads of circular shape with diameter of 1 mm and thickness of 100 nm have been deposited on the top surface of the nanostructured Si layer using thermal evaporation technique (HHV) maintaining a deposition rate ~ 2 Å/s monitored by a thickness monitor (DektakXT) to form the device for I–V measurement. Field Emission Scanning Electron Microscopy (FESEM) (Σigma Zeiss) has been employed to investigate the device structure.

The samples are annealed from 100 °C to 500 °C with temperature gap 100 °C. At each annealing step, I–V characteristics along with PL and FTIR spectra have been recorded. Figure 1 shows the schematic cross-section of the device for top–bottom geometry for I–V measurements. I–V characteristics have been recorded using Keithley-4200 ACS to

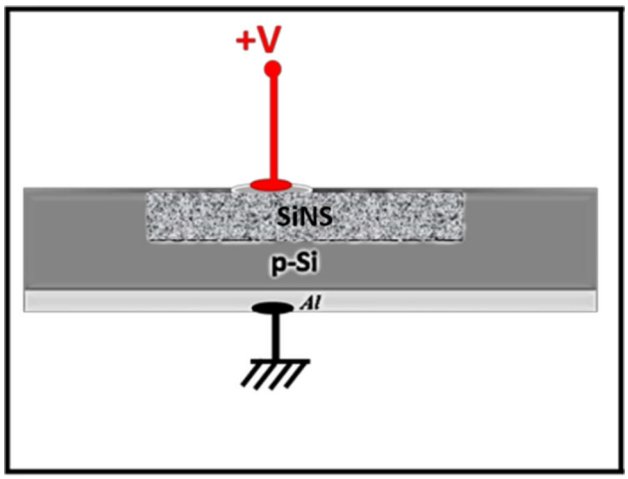

Fig. 1 Schematic cross-section of the device with electrical connection in top–bottom geometry

study the charge conduction through the devices made with the nanostructured Si samples.

3 Results

As mentioned above, three different samples have been prepared using electrochemical etching process. Table 1 provides the detailed description of the synthesized samples prepared with fixed etching time and electrolyte concentration. Porosity and thickness of the nanostructured layer is found to vary in the range ~ 65–85% and ~ 200–300 nm respectively.

3.1 Structural characterization

For structural characterizations of the nanostructured layers AFM and XRD have been employed. Figure 2a shows a 3-dimensional AFM topographic image of the SiNS present in PS3 on Si substrate. Random distributions of rod-like prolate nano structures are prominent from the surface undulations [5, 22, 26]. The average particle size is ~ 10*nm* [22].

Figure 2b shows the XRD pattern of the samples for 2θ varying between 50° and 80°. In nanocrystalline material, as a consequence of disruption of the long-range crystallinity the line width of the XRD peak gets broadened with respect to the peak for bulk Si crystals as observed usually [5, 8, 46, 47]. The average crystallite size measured from this peak broadening by using the Scherrer equation [48] is between 4 and 6 nm as listed in Table 1. It is well known that Scherrer equation is reasonable in size estimation for the strain-free systems [5, 47]. In case of highly strained nanostructured Si, this method provides only an order of magnitude estimation of the crystallite size [47, 49].

Average optical band gap has been estimated from the measured PL emission spectra. PL spectrum of the nanostructured Si layers under excitation of 405 nm UV LASER (1 mW) is shown in Fig. 2c. The wavelength corresponding to the peak of the spectrum gives an idea of effective optical band gap for the luminescent samples. PL measurements cannot provide the average electronic band gap or crystallite size of the nanostructures as the emission is not always channelized through band-to-band transition. However, it gives an idea of the average optical band gap of the Si nanocrystals in presence of mid gap defect states, as described elsewhere [5, 11, 22, 38, 44]. From Fig. 2c the blue shift in PL for Si nanostructure layers from PS1 to PS3 is prominent signifying a gradual decrease from PS3 to PS1. Effective optical band gaps of the samples have been found in the range of 2.0*eV*.

The details of the chemical bonds in the samples have been investigated through FTIR spectroscopy. At room temperature, FTIR spectra of the nanostructured Si layer is shown in Fig. 2d and the detailed descriptions of the bonds are listed in Table 2. The broad peak near ~ $1050cm^{-1}$ convoluted with ~$1155cm^{-1}$ indicates the presence of highly stressed SiO_x-Si bonds. This peak signifies the formation of nanocrystalline Si core–shell structure where the shell is compound of non-stoichiometric silicon oxide [18, 20, 50]. The presence of Si-H_x and O-SiH_x bonds is evident from the peaks near 804 cm^{-1} to 878 cm^{-1} region [5, 38]. A summary of all these peak positions and their interpretations have been given in Table 2 along with a comparative analysis of the bonds present in the three layers. The peak at ~ 610 cm^{-1} corresponds to the presence of Si–H bonds [5, 38]. These are likely to be developed due to electrochemical synthesis in HF solution whereas the Si–O–Si bonds can be created due to the oxidation after exposure to the ambient air.

Table 1 Description of the synthesized nanostructured Si layers for different etching parameters along with the estimated average particle size

Sl. no	Device name	Current density during etching (mA/cm^2)	Time of etching (min)	Estimated porosity	Thickness (nm)	Crystallite size (nm)
1	PS1	10	5	(65 ± 5)%	230 ± 2	6.3 ± 0.2
2	PS2	15		(72 ± 5)%	260 ± 3	5.4 ± 0.1
3	PS3	20		(81 ± 6)%	300 ± 3	4.2 ± 0.1

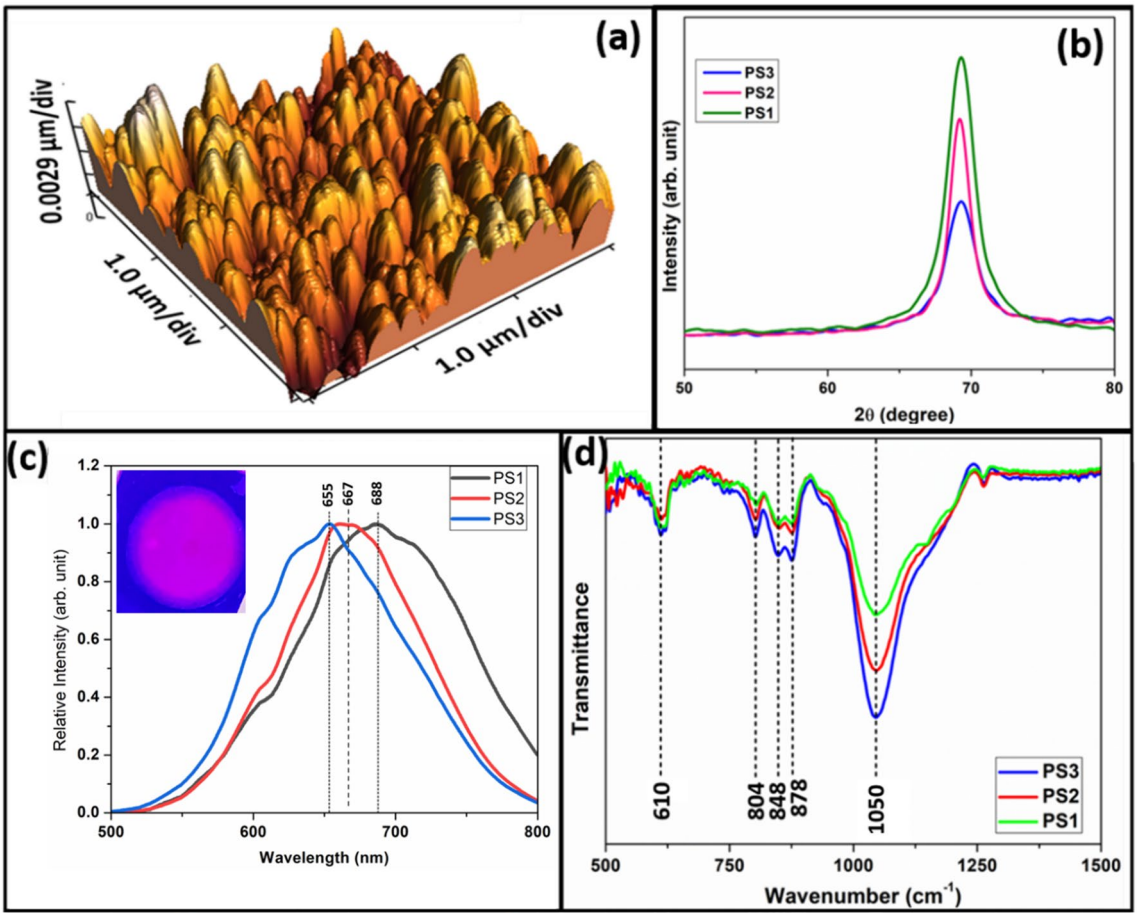

Fig. 2 **a** 3D topographic AFM image of the samples with inset showing the phase contrast image highlighting the core–shell structures of Si, **b** XRD patterns of the three nanostructured Si layers containing SiNS, **c** PL spectrum of the three different nanostructured Si layers showing the emission peak ~ 655 nm to ~ 688 nm under excitation of 405 nm UV laser with an inset showing the photograph of PL emission from a Si wafer containing Si nanostructures, **d** FTIR spectroscopic image of the SiNS in three different devices showing peaks near 610 cm^{-1} for Si–H bonds, Si–H_x and O–SiH_x bonds indicated by the peak near 804 cm^{-1} to 878 cm^{-1} and a broad peak around ~ 1050 cm^{-1} convoluted with 1155 cm^{-1} for highly stressed SiO_x–Si bonds

Table 2 Details of FTIR peaks for three different nanostructured Si layers

Wavenumber (cm^{-1})	Bonds	Type	Remarks
610	Si–H	Rocking [5, 38]	Present in all three samples
810 to 880	Si–O–Si O_3–Si–H in $SiO_{1.9}$	Bending [5, 38]	Lowest in PS1 and gradually increases in PS2 and PS3 respectively
1050 convoluted with 1155	Si–O–Si	Stretching [5, 22, 38]	Highest in PS3 but gradually decreases in PS2 and PS1 respectively

Aluminum metal has been deposited on the samples to form the devices for electrical characterization. The Cross-sectional FESEM image of the device containing the sample PS3 is shown in Fig. 3. The formation of SiNS on the Si substrate is clearly visible and the thickness of the layer is ~ 250 nm. Thickness of the deposited aluminum has been found to be of the order of100*nm*.

3.2 Effect of annealing temperature

After annealing at different temperatures, FTIR measurements have also been performed and the recorded spectra are shown in Fig. 4 for the sample PS3. All the samples show similar trend with increasing annealing temperature. The peak near 610 cm^{-1} due to Si–H bonds remain visibly

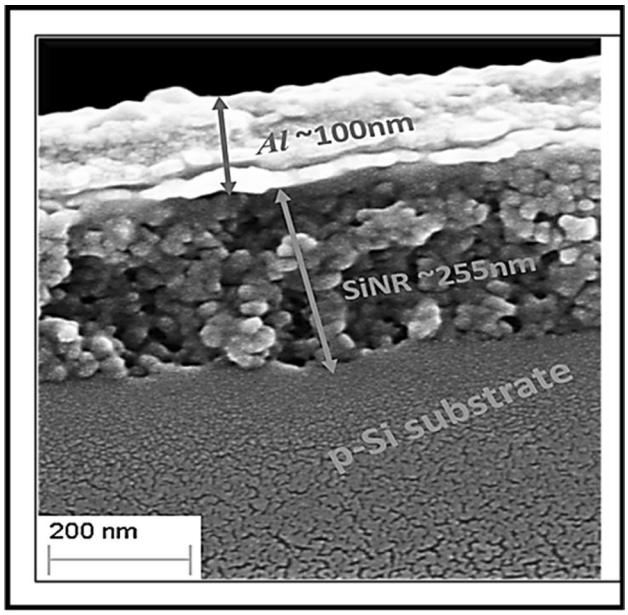

Fig. 3 FESEM image of the cross-section (with a tilt of stub at ~15°) of the device showing the SiNS-rich PS3 layer of thickness ~ 250 nm on p-Si substrate and aluminum coating on the top surface having thickness ~ 100 nm

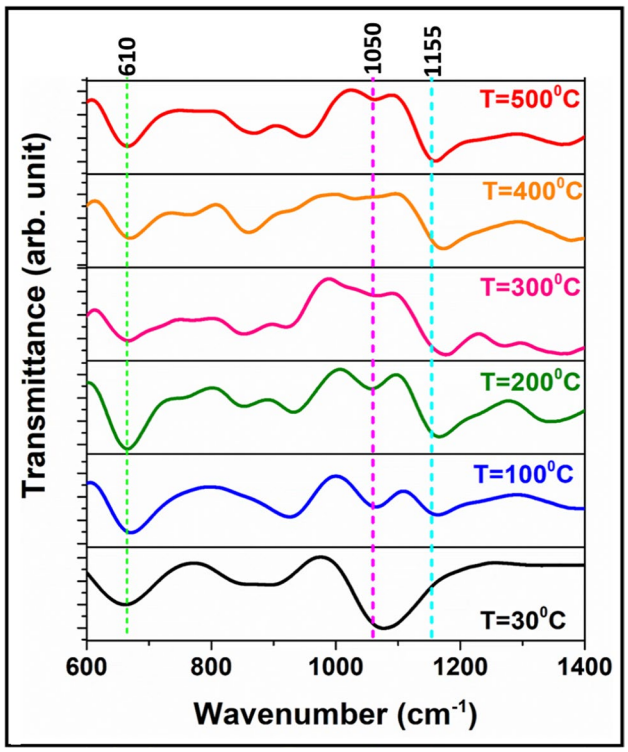

Fig. 4 FTIR spectra of the PS3 sample at different annealing temperatures showing the decrease in Si–O–Si bond at 1050 cm^{-1} with increasing temperature

unaffected during annealing. The interesting part is the decrease of Si–O–Si bonds indicated by peak at ~ 1050 cm^{-1} whereas the peak at ~ 1158 cm^{-1} seems to get deconvoluted with increasing temperature. This indicates the decrease of concentration of Si–O-Si related defect states within the forbidden gap.

Effect of annealing temperature on the PL spectra of the samples has been investigated. After each annealing step PL of the SiNS layer has been recorded as shown in Fig. 5 for the sample PS3. It is clearly visible that the main peak is near 655 nm along with some shoulders at ~ 607 nm, ~ 627 nm and ~ 670 nm resulting in a convoluted broad emission spectrum in the orange red region. Hence, to understand different radiative channels we have deconvoluted the spectra as a function of energy as shown in the plot inset Fig. 5a. The positions and relative intensities of the contributory radiative channels are listed in Table 3.

From Table 3, it is evident that the relative intensities for peak 1 and peak 3 decreases with increasing annealing temperature whereas the intensity of peak 4 is almost fixed. Another notable point is at higher annealing temperatures contribution of Peak 2 dominates over the other peaks.

3.3 Electrical characterization

It is well known that aluminum on p-Si forms ohmic contact when annealed at an elevated temperature [1]. But the scenario may become very different when the system under consideration has nano-dimensional features leading to large surface to volume ratio. Due to the presence of high concentration of surface/interface states, the semiconductor Fermi level is likely to get pinned at different positions within the band gap and hence the semiconductor work-function gets modified [12]. Consequently, the quality or the Ohmic nature of the metal/Nano-semiconductor junction is likely to be modified. Keeping this in mind we have varied the annealing temperature after deposition of aluminum and have recorded the I–V characteristics in search of an optimized range of temperature where the junction behaves like an ohmic one.

I–V characteristics of the devices in top–bottom geometry at every annealing step have been recorded with voltage sweep from + 3 V to − 3 V applied on the top aluminum contact with respect to the grounded p-Si wafer and the results are shown in Fig. 6. Initially, at room temperature (25°C), the device shows a non-ohmic nature with higher conductance for positive bias on the top metal. With increasing annealing temperature ranging up to 500°C, the conductance is found to decrease for positive bias and increase for negative bias. This means that the characteristics become more symmetric with respect to bias direction with increasing temperature as expected. At annealing temperature 200°C the contact behaves almost symmetrically and the I–V characteristics show fairly ohmic nature. Asymmetry

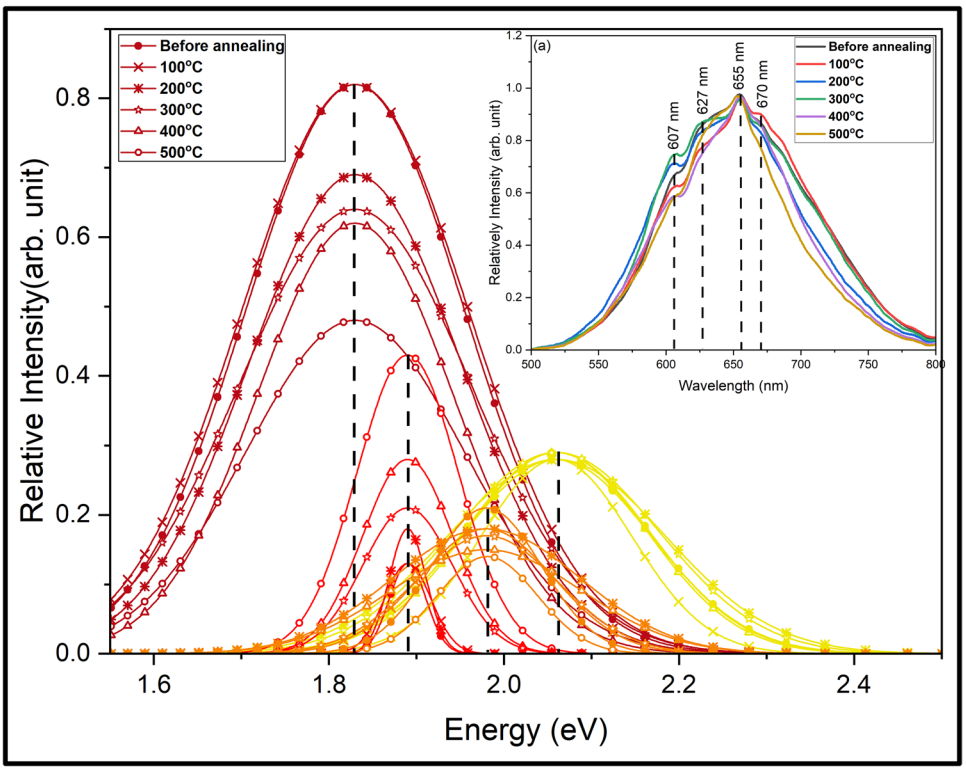

Fig. 5 Deconvoluted PL spectra of the samples after annealing at different temperatures showing the emission peaks at ~ 1.83 eV, ~ 1.89 eV, ~ 1.98 eV and ~ 2.06 eV under excitation of 405 nm UV laser with inset showing original PL spectrum as recorded during measurements

Table 3 Position and relative intensities of the contributing peaks in the PL spectra

Annealing temperature	Peak 1		Peak 2		Peak 3		Peak 4	
	Energy (eV)	Relative Intensity (arb. unit)	Energy (eV)	Relative Intensity (arb. unit)	Energy (eV)	Relative Intensity (arb. unit)	Energy (eV)	Relative Intensity (arb. unit)
Unannealed	1.83	0.82	1.89	0.13	1.98	0.21	2.06	0.28
100 °C	1.83	0.82	1.89	0.13	1.98	0.18	2.06	0.28
200 °C	1.83	0.69	1.89	0.18	1.98	0.18	2.06	0.28
300 °C	1.83	0.64	1.89	0.21	1.98	0.17	2.06	0.29
400 °C	1.83	0.62	1.89	0.28	1.98	0.15	2.06	0.29
500 °C	1.83	0.48	1.89	0.43	1.98	0.14	2.06	0.29

in the I–V graph is found to show up again when annealed further at 400°C to 500°C and the junction behaves fairly like a Schottky junction where higher current flows for a negative bias applied on the top aluminum pad.

4 Discussions

It is mentioned earlier that the Ohmic or rectifying (Schottky) contact is established between a metal and a semiconductor through suitable selection of materials by considering the values of their relative work functions [1, 10]. But the situation becomes non-trivial for defect/surface states enriched nanostructured system. In case of such systems high density of surface/interface states lead to modification of Fermi level within the band gap. Again, the band gap becomes size dependent for nanostructured materials [12]. As a result, an expected ohmic contact in bulk material may get modified to a Schottky junction in case of nano-dimensional system.

To understand the mechanism behind transition from non-ohmic to rectifying nature through an ohmic phase, we have plotted log$I$ vs. V for three representative annealing steps as shown in Fig. 7. The characteristics clearly show higher conductance when a positive bias is applied on top aluminum pad in room temperature before annealing (Fig. 7(a)). Symmetry in conductance for both biasing direction is clearly evident from Fig. 7b when the sample is annealed at $200^{o}C$.

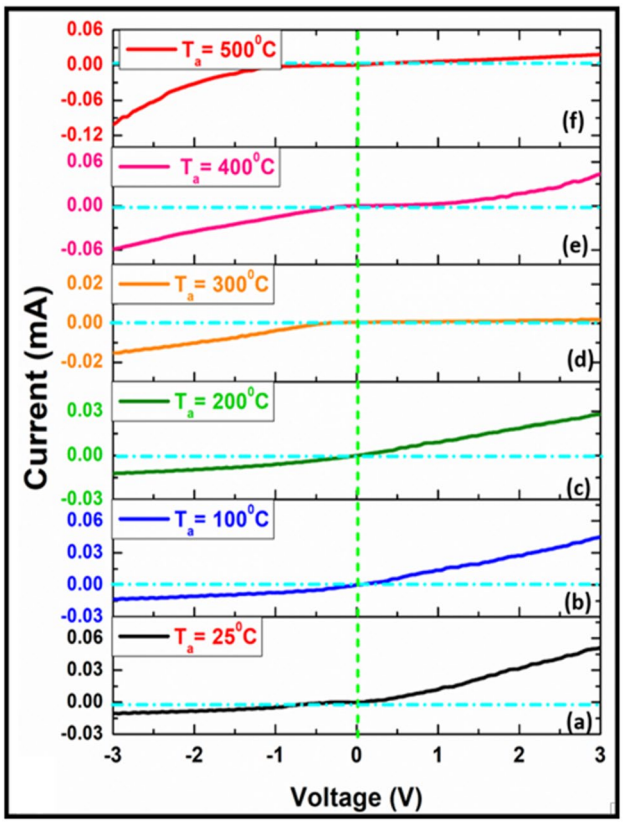

Fig. 6 I–V characteristics through the Si nanorods recorded after different annealing temperature

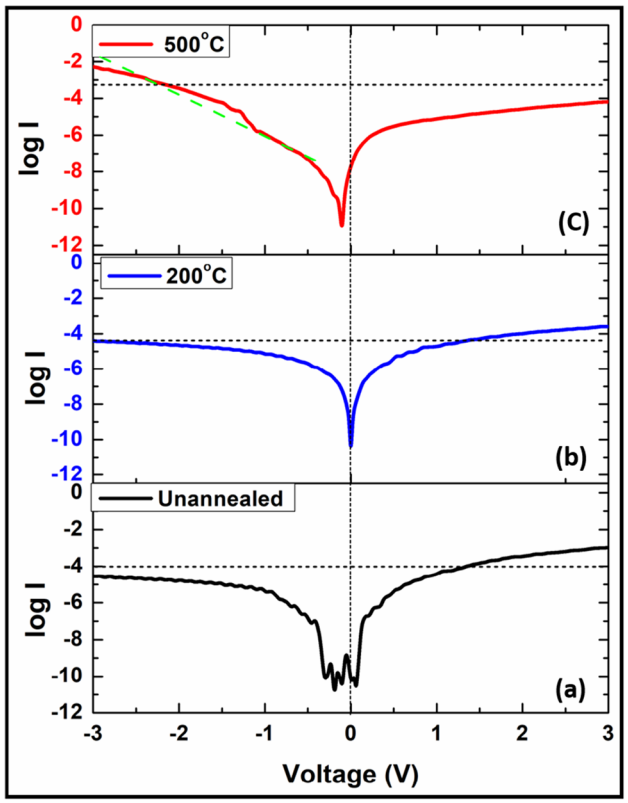

Fig. 7 log$I$*vs*.V characteristics through the Si nanorods in top–bottom geometry at different temperatures. The horizontal lines in each graph has been drawn at the maximum current under negative bias as guide to eye for comparing relative conductance

After that in higher annealing temperature, conductance becomes higher for the application of negative bias on top aluminum contact as shown in Fig. 7c. Moreover, a linearly increasing trend is prominent in this biasing direction which indicates formation of Schottky junction where the I–V relation is governed by Eq. (1) [1]

$$I = AT^2 e^{-\frac{q\Phi_B}{K_B T}} e^{\frac{qV}{\eta k_B T}} \tag{1}$$

where A is the Richardson constant ($120A/cm^2K^2$ for free electrons), Φ_B is barrier height and η is the ideality factor.

The change in the nature of I–V characteristics with increasing annealing temperature as shown in Fig. 6 can be explained by considering the pinning of Fermi level at different energies within the band gap. The band structure of oxidized nanostructured Si has been considered after calculation of Wolkin et al. [51] where, oxide related electron and hole traps determines the intensity and peak position of the luminescence spectrum. A schematic band diagram shown in Fig. 8 leads to four different radiative transition channels. The highest peak ($2.06eV$) is to be due to intra-band transition whereas the lowest energy peak ($1.83eV$) is expected to be due to the recombination of an electron trapped below the conduction band and a hole trapped above the valence band. On the other hand the two other peaks ($1.89eV and 1.98eV$) involve recombination of photo-excited carriers after relaxation at the respective band edges with that captured at the oxide related trap states [1] as shown in Fig. 8.

From Table 3, it is obtained that the intensities of peak 1 and peak 3 (with energies $1.83eV and 1.98eV$ respectively) get reduced gradually with increasing annealing temperature. These two transitions are mediated via electron traps located below the conduction band edge as shown in Fig. 8. Hence, it is evident that the electron trap assisted radiative transitions get reduced with increasing annealing temperature.

It is expected that with increasing temperature the shallow defects get saturated before the deep level ones. In FTIR spectra (Fig. 4), the intensity of Si–O–Si related peak at $1050cm^{-1}$ is found to decrease at higher annealing temperatures. Hence, the reduction of peak intensity for these two peaks can be correlated and may be interpreted as the reduction of electron capturing shallow defect states during annealing.

With the decrease of electron capturing defect states, charge transport through the system is likely to be dominated by hole capturing defect states located above the valence band edge. It supports the increase of intensity of radiative

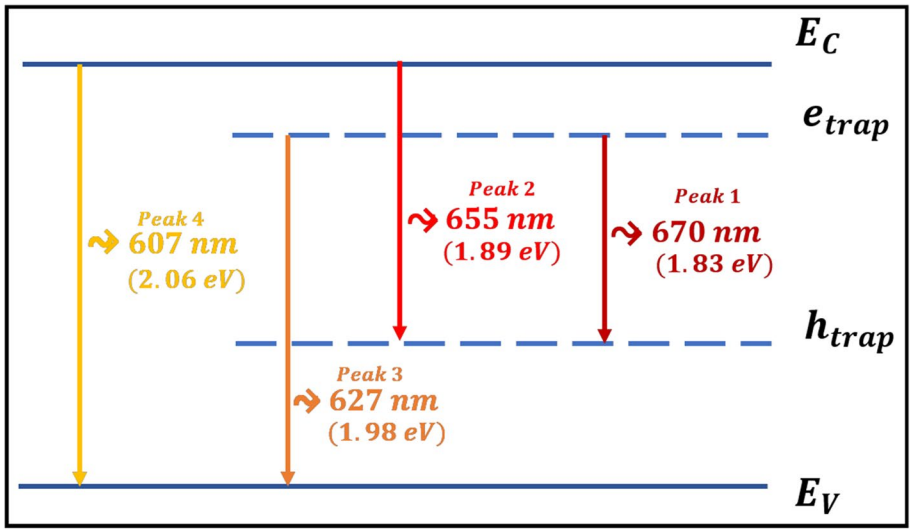

Fig. 8 Schematic energy band diagram of oxidized nanostructured Si and defect related energy states responsible for broad PL spectrum with four different peaks

transition between conduction band edge and hole capturing defect states denoted as peak 2 (1.89eV) as obtained in Table 3.

It is already known that for p-type semiconductor ohmic contact is developed at metal–semiconductor interface for the condition $\varphi_m > \varphi_S$ where φ_m and φ_S are the work functions of metal and semiconductor respectively [1]. Though aluminum and p-Si form ohmic contact satisfying this condition, nanostructured Si containing Si nanostructures having a different average band gap may not satisfy the condition for Ohmic contact. Besides, nano-Si is enriched with defect states (as evident from the FTIR spectra) which has a great impact on Fermi level position [10, 12] and hence on band bending. In the porosity range of our samples, it is likely that a lot of oxide related trap states are present below the conduction band edge which leads to pinning of the Fermi level above the middle of the band gap of the oxidized nanostructured silicon as shown in Fig. 9 though it is synthesized from p-type Silicon. The location of the pinned Fermi level depends on the location as well as on the concentration of the surface states given by the following formula for donor-like surface states [12].

$$\varepsilon_F^* = \frac{1}{2}(\varepsilon_C + \varepsilon_{SS}) - \frac{1}{2}k_B T \ln \frac{N_C}{\zeta N_{SS}} \tag{2}$$

here ϵ_F^* is the pinned position of Fermi level due to the existence of surface states (donor type) of concentration N_{SS} along with carrier concentration N_C. ζ is a factor for conversion of volume concentration to surface concentration.

The schematic band diagram of Fig. 9a shows an upward bending of the nanostructured Si band at the nanostructured Si/aluminum junction as the surface of Si nanostructure is behaving like an n-type semiconductor due to fermi level pinning near the electron trap populated region below the conduction band [52] and consequently explains the non-ohmic nature of I–V characteristics at room temperature as shown in Fig. 6a and b.

Hence, with increasing temperature, defect states move downward. Accordingly, the location of Fermi level is also expected to move downward as shown in Fig. 9b where the upward bending of nanostructured Si band is reduced near the aluminum contact resulting the surface to be a nearly intrinsic in nature [53]. The nature of band bending explains the nearly ohmic nature of nanostructured Si/aluminum contact at ~ 200°C as shown in Fig. 6c and d.

Above this temperature the concentration of oxide related defect states is expected to get reduced sufficiently such that the location of Fermi level is determined only by the dopant atoms (B atom in this case) present in nanostructured Si layer. Hence the surface of Si nanostructure behaves as p-type where the Fermi level is located near the valence band edge of nanostructured Si after annealing it above 200°C as shown in Fig. 9c. If the Fermi level of nanostructured Si goes below that of aluminum, the band bending gets reversed resulting in Schottky-like I–V characteristics depicted in Fig. 6e.

The fundamental physics driving this phenomenon has been studied before [12]. The limitation of accounting all the developed barriers in case of nanostructures, especially in surface state enriched systems, has also been reviewed by Zimin [54] which predicts that one may get both ohmic and non-ohmic I–V characteristics in the vicinity of the origin in case of porous Si depending upon different physical parameters like the thickness of the layer. Our results are also in good agreement with the above prediction at different annealing temperatures. It is evident from the literature that the change in energy and concentration of surface states with temperature variation is accountable for the observed I–V characteristics in heterostructure junction [27, 55–57].

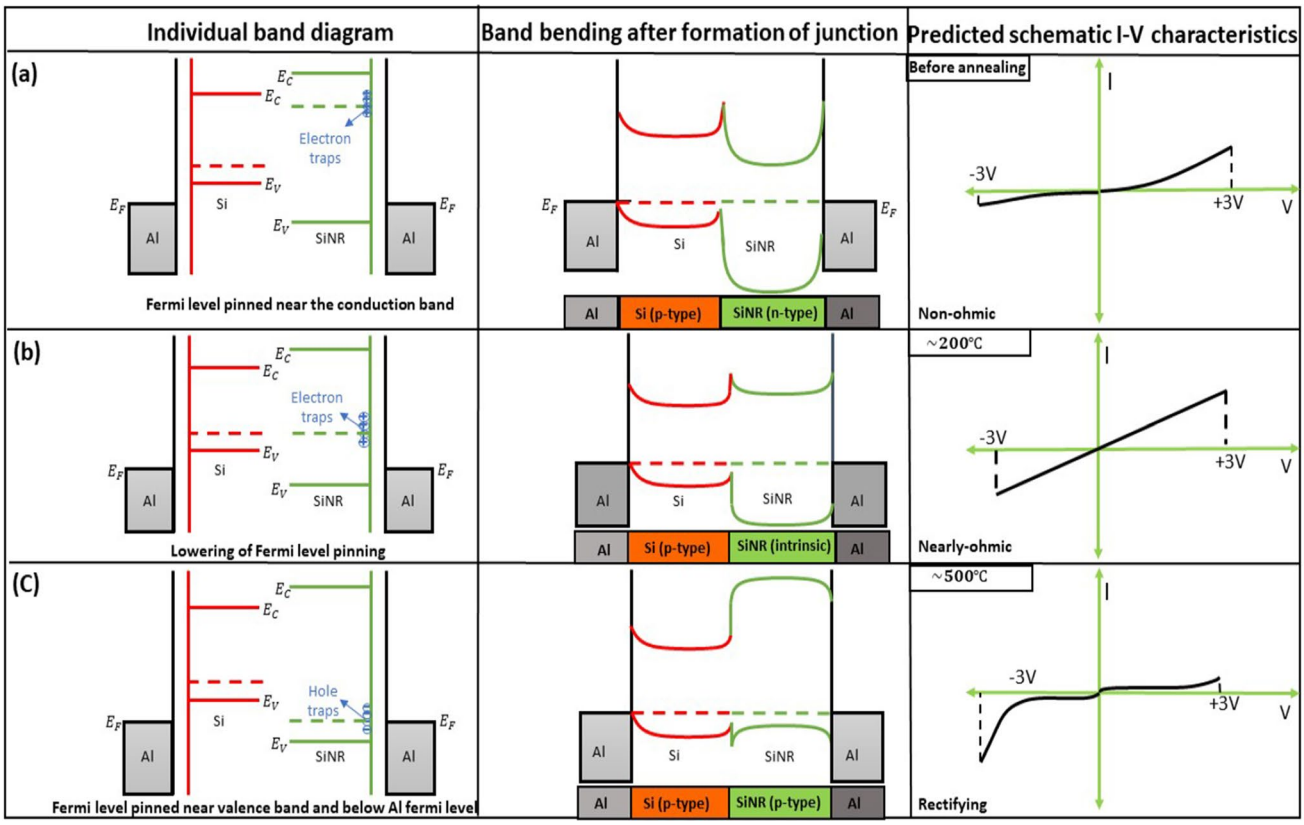

Fig. 9 Predicted I–V curves originated from the schematic band diagram leading to different band bending for the different location of electron/hole traps (**a**) Pinning of Fermi level near the electron trap states below the conduction band causes non-ohmic contact, (**b**) Annealing leads to saturation of shallow electron traps causing lowering of Fermi level and formation of ohmic contact, (**c**) Further annealing saturates most of the electron traps leading to pinning of Fermi level near valence band below metal Fermi level causes rectifying contact

However, the nature of the junction is expected to be independent of using different orientation of the bulk Si substrate as the I–V characteristics is primarily governed by the location and density of the surface states [15].

5 Conclusion

Studies on the dependance of band bending upon the concentration as well as the position of surface states leads towards the formation of ohmic contact at nano-Si/aluminum junction. As evident by FTIR and PL data, with a variation of post deposition annealing temperature, the concentration of surface states can be varied and hence the position of fermi level pinning on the surface of Si nanostructures also varies. The nearly symmetric I–V characteristic has been achieved around the temperature 200°C for an applied voltage from $+3V$ to $-3V$. Also, in this study a qualitative explanation has been predicted for the asymmetric, ohmic and rectifying natures of I–V characteristics as obtained experimentally at different annealing temperatures. This work would be helpful in studying the role of surface/interface states almost inevitable in case of low dimensional semiconducting system. However, the phenomena could be understood conclusively by measuring the energy and concentration of the trap states by implementing direct methods like ESR, XPS and DLTS that warrants a separate study. The work could be fine-tuned by deriving I–V characteristics from first-principle calculations in presence of trap states. The study may be extended to find the nature of the contact as a function of core and shell dimension of the nanostructures as well as the metal work-function at different range of applied bias.

Acknowledgements One of the authors Sudipta Chakrabarty acknowledges DST, Government of India for INSPIRE Fellowship (Id: IF160962).

Author contributions All the authors contributed significantly to this study. Nanostructure synthesis and device fabrication was done by Sudipta Chakrabarty. Both the authors Sudipta Chakrabarty and Suman Santra had the lead role in data collection, analysis and initial drafting of the manuscript. Syed Minhaz Hossain supervised the whole work and contributed significantly in planning of the experiment and data analysis followed by manuscript finalization.

Funding The authors have no relevant financial or non-financial interests to declare.

Data availability All data generated or analyzed during this study are included in this published article. Additionally, the data will be available through the communication with corresponding author.

Declarations

Conflict of interest The authors have no competing interests to disclose relevant to the content of this article.

References

1. B. G. Streetman and S. K. Banerjee, *Solid state electronic devices*, Seventh. Edinburgh Gate: Pearson Education Limited, 2016.
2. R. Tsu, Phenomena in silicon nanostructure devices. Appl. Phys. A Mater. Sci. Process. **402**, 391–402 (2000). https://doi.org/10.1007/s003390000552
3. R. Rahighi, O. Akhavan, A.S. Zeraati, S.M. Sattari-esfahlan, All-carbon negative differential resistance nanodevice using a single flake of nanoporous graphene. ACS Appl. Electron. Mater. **3**(8), 3418–3427 (2021). https://doi.org/10.1021/acsaelm.1c00396
4. B.J. Pawlak, T. Gregorkiewicz, C.A.J. Ammerlaan, Experimental investigation of band structure modification in silicon nanocrystals. Phys. Rev. B **64**(115308), 1–9 (2001). https://doi.org/10.1103/PhysRevB.64.115308
5. S. Chakrabarty, G. Das, M. Ray, S.M. Hossain, Optically enhanced trap assisted hysteretic I–V characteristics of nanocrystalline silicon based p-i-n heterostructure. J. Appl. Phys. (2020). https://doi.org/10.1063/1.5127653
6. M. Ray et al., Luminescent core-shell nanostructures of silicon and silicon oxide: nanodots and nanorods. J. Appl. Phys. **107**(6), 064311–064321 (2010). https://doi.org/10.1063/1.3330658
7. M. Ray, S. Sarkar, N.R. Bandyopadhyay, S.M. Hossain, A.K. Pramanick, Silicon and silicon oxide core-shell nanoparticles: structural and photoluminescence characteristics. J. Appl. Phys. **105**(7), 074301 (2009). https://doi.org/10.1063/1.3100045
8. S. Dhara, P.K. Giri, Size-dependent visible absorption and fast photoluminescence decay dynamics from freestanding strained silicon nanocrystals. Nanoscale Res. Lett. **6**, 1–7 (2011). https://doi.org/10.1186/1556-276X-6-320
9. B.J. Abdullah, Size effect of band gap in semiconductor nanocrystals and nanostructures from density functional theory within HSE06. Mater. Sci. Semicond. Process. (2022). https://doi.org/10.1016/j.mssp.2021.106214
10. S.M. Sze, K.N. Kwok, *Physics of semiconductor devices*, 3rd edn. (Wiley, 2007)
11. S.M. Hossain et al., Subband gap photoresponse of nanocrystalline silicon in a metal-oxide-semiconductor device. J. Appl. Phys. **104**(7), 074917 (2008). https://doi.org/10.1063/1.2999561
12. N. Sato, *Electrochemistry at metal and semiconductor electrodes*, 1st edn. (Elsevier Science B.V, Amsterdam, 1998)
13. K.-M. Lee, J.-D. Hwang, K.-S. Keum, K.-S. No, W.-S. Hong, The hysteresis characteristics of low temperature (≤ 200 °) silicon nanocrystals embedded in silicon-rich silicon nitride films. ECS Trans. **35**(18), 47–52 (2011). https://doi.org/10.1149/1.3647903
14. J.J. Yang, M.D. Pickett, X. Li, D.A.A. Ohlberg, D.R. Stewart, R.S. Williams, Memristive switching mechanism for metal / oxide / metal nanodevices. Nat. Nanotechnol. **3**, 429–433 (2008). https://doi.org/10.1038/nnano.2008.160
15. D.B. Dimitrov, Current-voltage characteristics of porous-silicon layers. Phys. Rev. B **51**(3), 1–5 (1995)
16. S. Chakrabarty, S.M. Hossain, Negative differential resistance in Si nanostructure: role of interface traps. Phys. Scr. **98**(8), 85909 (2023). https://doi.org/10.1088/1402-4896/ace138
17. U. Ghanta, M. Ray, N.R. Bandyopadhyay, S.M. Hossain, Unipolar resistive switching and tunneling oscillations in isolated Si–SiO x core–shell nanostructure. Nanotechnology **27**(45), 455702 (2016). https://doi.org/10.1088/0957-4484/27/45/455702
18. F.K.M. Ben-Chorin, F. Moiler, Nonlinear electrical transport in porous silicon. Phys. Rev. B **49**(4), 6–9 (1994)
19. S. Yu, X. Guan, H.P. Wong, Conduction mechanism of TiN / HfOx / Pt resistive switching memory: a trap- assisted-tunneling model. Appl. Phys. Lett. **99**(063507), 2011–2014 (2011). https://doi.org/10.1063/1.3624472
20. C. Liu, Y. Shih, S. Huang, Unipolar resistive switching in a transparent ITO/SiOx/ITO sandwich fabricated at room temperature. Solid State Commun. (2013). https://doi.org/10.1016/j.ssc.2013.01.008
21. S. Chakrabarty, S. Mandal, U. Ghanta, J. Das, and S. Minhaz, "Current Controlled Switching in Si / PS / a-Si Heterostructure," *Mater. Today Proc.*, p. accepted for publication, 2017.
22. S. Chakrabarty, S. Mandal, S. Biswas, A.K. Pramanick, M. Ray, Trap-assisted switching in silicon nanocrystal based p-i-n device. IEEE Trans. Device Mater. Reliab. **18**(4), 620–627 (2018). https://doi.org/10.1109/TDMR.2018.2878466
23. G. Lin, C. Lin, C. Lin, Enhanced Fowler-Nordheim tunneling effect in nanocrystallite Si based LED with interfacial Si nanopyramids. Opt. Express **15**(5), 2555–2563 (2009)
24. E. Miranda, F. Palumbo, Analytic expression for the Fowler—Nordheim V—I characteristic including the series resistance effect. Solid State Electron. **61**(1), 93–95 (2011). https://doi.org/10.1016/j.sse.2011.03.015
25. M. Theodoropoulou et al., Transient and AC electrical conductivity of porous silicon thin films. Phys. status solidi **283**(1), 279–283 (2003). https://doi.org/10.1002/pssa.200306481
26. U. Ghanta, S. Singh, M. Ray, N.R. Bandyopadhyay, S. Ganapathy, S.M. Hossain, Electrical transport through array of electrochemically etched silicon nanorods. Phys. status solidi **214**(6), 1600879 (2017). https://doi.org/10.1002/pssa.201600879
27. A.K. Ray, M.F. Mabrook, A.V. Nabok, S. Brown, Transport mechanisms in porous silicon. J. Appl. Phys. **84**, 3232 (1998). https://doi.org/10.1063/1.368476
28. F.C. Chiu, A review on conduction mechanisms in dielectric films. Adv. Mater. Sci. Eng. **2014**, 1–18 (2014). https://doi.org/10.1155/2014/578168
29. P. Mishra, S. Nozaki, R. Sakura, H. Morisaki, H. Ono, K. Uchida, Capacitance-Voltage (C-V) hysteresis in the Metal-Oxide-Semiconductor capacitor with Si nanocrystals deposited by the gas evaporation technique. MRS Online Proc. Libr. **686**(54), 1–6 (2001). https://doi.org/10.1557/proc-686-a5.4
30. M. Yang, T. Kim, T. Lee, S. Hong, Nanoscale enhancement of photoconductivity by localized charge traps in the grain structures of monolayer MoS2. Sci. Rep. **8**(15822), 1–9 (2018). https://doi.org/10.1038/s41598-018-34209-w
31. N. Sghaier, M. Troudi, L. Militaru, A. Kalboussi, A. Souifi, Traps identification in silicon nanocrystals memories by low noise technique. Mater. Sci. Eng. C **28**(5–6), 882–886 (2008). https://doi.org/10.1016/j.msec.2007.10.050
32. S.M. Hossain, S. Chakraborty, S.K. Dutta, J. Das, H. Saha, Stability in photoluminescence of porous silicon. J. Lumin. **91**(3–4), 195–202 (2000). https://doi.org/10.1016/S0022-2313(00)00225-8
33. Y. Bhattacharjee, S. Bose, Core–shell nanomaterials for microwave absorption and electromagnetic interference shielding: a review. ACS Appl. nano Mater. **4**, 949–972 (2021). https://doi.org/10.1021/acsanm.1c00278
34. R.G. Chaudhuri, S. Paria, Core / shell nanoparticles: classes, properties, synthesis mechanisms, characterization, and applications.

Chem. Rev. **112**, 2373–2433 (2012). https://doi.org/10.1021/cr100449n|
35. S. Singh, V. Kaur, N. Kumar, "Core–shell nanostructures: an insight into their synthetic approaches," in *Metal Semiconductor Core-shell Nanostructures for Energy and Environmental Applications: Chapter-2*, Elsevier Inc., 2017, pp. 35–50.
36. S. Godefroo et al., Classification and control of the origin of photoluminescence from Si nanocrystals. Nat. Nanotechnol. (2020). https://doi.org/10.1038/nnano.2008.7
37. S. Chatbouri, M. Troudi, A. Kalboussi, A. Souifi, Interface traps contribution on transport mechanisms under illumination in metal–oxide–semiconductor structures based on silicon nanocrystals. Appl. Phys. A Mater. Sci. Process. **124**(2), 1–9 (2018). https://doi.org/10.1007/s00339-017-1533-x
38. S. Chakrabarty, J. Das, S.M. Hossain, Origin of photo-enhanced hysteretic electrical conductance in nanostructured silicon-based heterojunction. J. Phys. D Appl. Phys. **55**(27), 275101 (2022). https://doi.org/10.1088/1361-6463/ac6238
39. Y. Liu et al., Approaching the Schottky-Mott limit in van der Waals metal–semiconductor junctions. Nature **557**, 696–700 (2018). https://doi.org/10.1038/s41586-018-0129-8
40. S. Chakrabarty, S. Mandal, U. Ghanta, J. Das, S.M. Hossain, Current controlled switching in Si/PS/a-Si heterostructure. Mater. Today Proc. **5**, 9790–9797 (2018). https://doi.org/10.1016/j.matpr.2017.10.168
41. P. Schmuki, L.E. Erickson, D.J. Lockwood, Light emitting micropatterns of porous si created at surface defects. Phys. Rev. Lett. **80**(18), 4060–4063 (1998). https://doi.org/10.1103/PhysRevLett.80.4060
42. H.W. Lau et al., Defect-induced photoluminescence from tetraethylorthosilicate thin films containing mechanically milled silicon nanocrystals. J. Appl. Phys. (2014). https://doi.org/10.1063/1.1899244
43. P. Bamola et al., Role of defects and interfacial interactions in ion irradiated noble metal based TiO2 hybrid nanostructures for improved photocatalytic investigation. Surfaces Interfaces **33**, 102878 (2023). https://doi.org/10.1016/j.surfin.2023.102878
44. O. Bisi, S. Ossicini, L. Pavesi, Porous silicon: a quantum sponge structure for silicon based optoelectronics. Surf. Sci. Rep. **38**(1–3), 1–126 (2000). https://doi.org/10.1016/S0167-5729(99)00012-6
45. S.M. Hossain, J. Das, S.K. Dutta, H. Saha, Mechanism and simulation of uniform nanowires of porous silicon growth on p- Si substrate. Int. J. Nanosci. **05**(01), 69–90 (2006). https://doi.org/10.1142/S0219581X0600419X
46. T. Matsumoto, M. Maeda, H. Kobayashi, Photoluminescence enhancement of adsorbed species on Si nanoparticles. Nanoscale Res. Lett. **11**(7), 1–6 (2016). https://doi.org/10.1186/s11671-015-1220-9
47. M. Zhao, J. Zhang, W. Wang, Q. Zhang, Potential spark erosion approaches to silicon nanoparticles production. Nanomaterials **11**(594), 1–15 (2021). https://doi.org/10.3390/nano11030594
48. U. Holzwarth, N. Gibson, The Scherrer equation versus the 'Debye–Scherrer equation.' Nat. Nanotechnol. **6**, 534 (2011). https://doi.org/10.1038/nnano.2011.145
49. J. Jakubowicz, K. Smardz, L. Smardz, Characterization of porous silicon prepared by powder technology. Phys. E **38**, 139–143 (2007). https://doi.org/10.1016/j.physe.2006.12.017
50. M. Achref, A.J. Bessadok, L. Khezami, S. Mokraoui, M. Benrabha, Effective surface passivation on multi-crystalline silicon using aluminum / porous silicon nanostructures. Surfaces Interfaces **18**, 100391 (2019). https://doi.org/10.1016/j.surfin.2019.100391
51. M.V. Wolkin, J. Jorne, P.M. Fauchet, G. Allan, C. Delerue, Electronic states and luminescence in porous silicon quantum dots: the role of oxygen. Phys. Rev. Lett. **82**(1), 197–200 (1999). https://doi.org/10.1103/PhysRevLett.82.197
52. W.H. Lee, C. Lee, Y.H. Kwon, C.Y. Hong, H.Y. Cho, Deep level defects in porous silicon. Solid State Commun. **113**, 519–522 (2000)
53. J. Mizsei, J.A. Shrair, I. Zo, Investigation of Fermi-level pinning at silicon / porous-silicon interface by vibrating capacitor and surface photovoltage measurements. Appl. Surf. Sci. **235**, 376–388 (2004). https://doi.org/10.1016/j.apsusc.2004.05.110
54. S.P. Zimin, Classification of electrical properties of porous silicon. Semiconductors **34**(3), 359–363 (2000)
55. D. Hamri, A. Teffahi, A. Djeghlouf, A. Saidane, A. Mesli, Temperature dependent transport characterization of iron on n-type (111) Si0.65Ge0.35 Schottky diodes. J. Alloys Compd. (2018). https://doi.org/10.1016/j.jallcom.2018.05.336
56. C.S. Oh et al., Thermal distributions of surface states causing the current collapse in unpassivated AlGaN / GaN heterostructure field-effect transistors. Appl. Phys. Lett. **86**(012106), 10–13 (2005). https://doi.org/10.1063/1.1844610
57. C. Wang, S.K. Behura, V. Berry, Temperature dependent device characteristics of graphene / h-BN / Si heterojunction. Semicond. Sci. Technol. **35**, 075020 (2020)