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# The electrical characterization of Ag/PTCDA/PEDOT:PSS/p-Si Schottky diode by current–voltage characteristics

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ABSTRACT

The Ag/PTCDA/PEDOT:PSS/p-Si Schottky diode has been fabricated by adding a layer of organic compound 3,4,9,10-perylene tetracarboxylic dianhydride (PTCDA) on top of the p-Si for which the junction characteristics have been investigated. The electronic properties of the device have been studied by the conventional *I–V* and the Norde's methods. For conventional *I–V* measurements the rectifying behavior has been observed with a rectification ratio of 236. The barrier height and ideality factor values of 0.81 eV and 3.5, respectively, for the structure have been obtained from the forward bias *I–V* characteristics. Various electrical parameters such as reverse saturation current, series resistance and shunt resistance have been calculated from the analysis of experimental *I–V* results and discussed in detail. The barrier height and the series resistance determined by the Norde's function are found in good agreement with the values calculated from conventional *I–V* measurements. The charge conduction mechanism has also been discussed.



## 1. Introduction

Reliable and well controlled contacts are needed for almost all semiconductor devices. Metal–semiconductor (MS) structures serve the purpose in the form of Schottky barrier diodes (SBD) [1]. SBD plays a vital role in the device performance [2] and is the most widely used contact in semiconductor electronic devices, such as field effect transistors, solar cells and photodetectors etc. [3,4]. Certain parameters, such as barrier height, ideality factor and series resistance, determine electronic properties of the Schottky diode. Complete information about the nature of the diode can be obtained from these parameters. For the understanding of the electrical properties of the Schottky diode it is extremely important to study the interface properties, which mainly control the performance of the Schottky diode [4–6]. In general, the physical properties of the metal/semiconductor interface depend on the surface preparation methods, which ultimately affect the performance, electrical properties, stability and reliability of the MS devices [7,8]. The introduction of non-reactive organic thin films at the MS interface can reduce the states during metallization process [7]. Forrest et al. [9] and Antohe et al. [10] introduced the organic interfacial layer by sublimation in metal–interface–semiconductor (MIS) structure for determining the ideality factor and barrier height. Cakar et al. obtained the ideality factor and barrier height by adding pyronine-B on the Si-substrate [11]. The *I–V* curves were determined for the devices fabricated from thin films formed by the anodization method and the diode parameters were obtained [12,13]. Furthermore, in some studies, the investigation on the interfacial layer for the estimation of barrier height data [14], effect of interfacial layer on the ideality factor [15] and Schottky contacts [16] has been reported. The organic/inorganic semiconductor diodes can provide a useful tool for passivating interface states, surface damages and contamination in order to ultimately enhance the performance of the devices based on semiconductors [10,17,18].

Among a plethora of organic semiconductors, perylene and its derivatives constitute a family of promising candidates due to their electronic, luminescent and electrochemical properties [19]. A detailed study on the thin films of PTCDA has shown its use in a variety of electronic and optoelectronic applications [20,21]. Due to the organic semiconducting behavior, PTCDA has been employed in the application of organic thin film transistor (OTFT), organic light emitting diodes (OLED) and organic solar cells (OSC) [22–24]. It has been reported that PTCDA has a high crystallinity and low intermolecular distance, which give rise to strong $\pi$–$\pi$ overlap and promising transport properties [25]. Many researchers have explored PTCDA for its electronic properties on different substrates, film thicknesses and growth conditions [21].

The purpose of this study is to introduce an organic thin film of PTCDA as an interfacial layer between metal and semiconductor to form an MIS structure. Furthermore, the semiconductor organic

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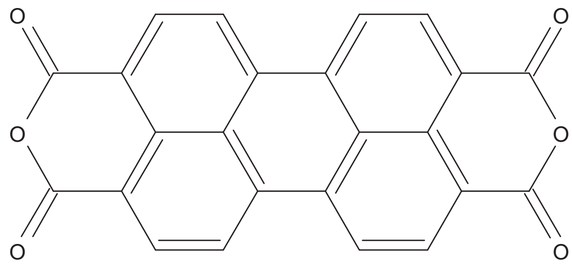


**Fig. 1.** Molecular structure of PTCDA.

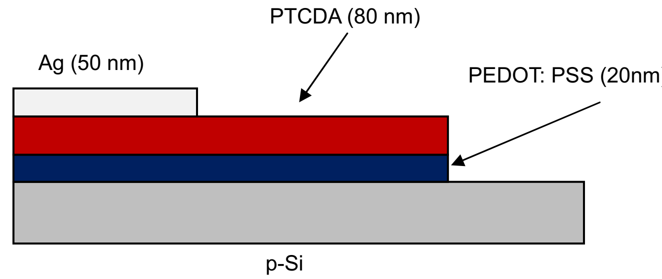


**Fig. 2.** Cross sectional view of Ag/PTCDA/PEDOT:PSS/p-Si Schottky diode.

thin film (PTCDA)/semiconductor (Si) contact has been investigated for rectifying behavior. In this study the electrical properties of PTCDA/p-Si MIS structure have been investigated through *I–V* characteristics under dark at room temperature. The aim of this paper is to extract the electronic parameters through different *I–V* methods and study the charge transport mechanism through the device.

## 2. Experimental

The PTCDA is chemically known as 3,4,9,10-perylene tetracarboxylic dianhydride and its chemical structure is shown in Fig. 1. The samples were prepared on cleaned and polished p-type Si wafer with (1 0 0) orientation. To remove the native oxide from the front surface of the p-type Si substrate, a solution of HF:$H_2O$ with a solution strength of 1:10 was used. Later the substrate was cleaned in acetone using ultrasonic bath for 5 min followed by drying with a stream of nitrogen gas. Further oxide layer was removed by treating the p-Si with plasma ashing using JLS Designs Plasmaline TEGAL having CESAR RF Power Generator ~300 W for 2 min in a clean room. A buffer layer of 20 nm PEDOT:PSS film was spin coated on p-Si substrate at the rate of 2000 rpm for 20 s. The PEDOT:PSS layer was, then, annealed at 50 °C for 2 h using a hot plate, in the nitrogen environment, to let the moisture fully evaporate from the buffer layer. A thin film (~80 nm) of PTCDA was thermally deposited on pre-coated PEDOT:PSS layer using thermal evaporation. Finally, the Ag rectifying metal contact of 50 nm was deposited on the PTCDA/p-Si structure through a shadow mask. For thermally deposited layers the pressure inside the chamber was $10^{-6}$ mbar with a deposition rate of 0.1 nm/s. The thickness of the film was monitored by Quartz Crystal Oscillator installed inside the evaporation chamber. The cross-sectional view of the fabricated Ag/PTCDA/PEDOT:PSS/p-Si MIS device is shown in Fig. 2. The current–voltage (*I–V*) measurements were made using Keithley 236 SMU system.

## 3. Results and discussion

The electrical characterization of the device Ag/PTCDA/PEDOT:PSS/p-Si was obtained through the current–voltage measurements at room temperature. The forward and reverse bias *I–V* characteristics of the device are shown in Fig. 3. The *I–V* measurements are extremely important as they provide information about junction parameters such as reverse saturation current, rectification ratio, ideality factor, barrier height, series and shunt resistances. The exponential behavior of *I–V* curves in the forward region strongly depends on the properties of organic active layer employed in the studied device. In the exponential region, the slope of the *I–V* characteristics depends on two parameters, i.e. ideality factor '$n$' and the reverse saturation current $I_o$. The information about the recombination process occurring in the device and the shape of the interfaces can be acquired through ideality factor [26]. However,

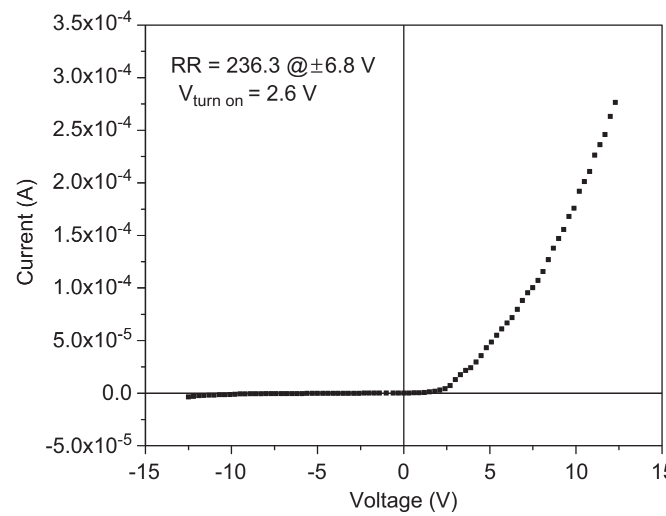


**Fig. 3.** Current–voltage characteristics of Ag/PTCDA/PEDOT:PSS/p-Si.

the saturation current gives the number of charge carriers the capability of overcoming the barrier in the reverse bias [27,28]. It is well-known that for an ideal diode the ideality factor should be close to unity while the saturation current should be in picoscale. The investigated device exhibits exponential behavior for the applied voltages greater than 2.5 V. The dependence of exponential curve on this applied voltage with the reverse saturation current in nanoscale and the ideality factor (~3.5) smaller than the value (~5.8) reported for PTCDA/n-Si [29] can be ascribed to the formation of better depletion region between p-Si and PTCDA.

The non-linear and asymmetric *I–V* curves of Fig. 4 reveal that the device exhibits rectifying behavior. The rectification ratio (RR) of the investigated device was found to be 236 at ±6.8 V. The value of the turn on voltage was 2.6 V. The reverse saturation current was determined from the semi-log current–voltage characteristics, shown in Fig. 4 and was found to be 1.32 nA. The reverse saturation for the present device is consistent with the values reported for PTCDA/n-Si in the literature [29].

The current through a uniform metal–semiconductor interface due to the thermionic emission theory can be employed to extract characteristic parameters of the Ag/PTCDA/PEDOT:PSS/p-Si device. The forward bias current of the device due to thermionic emission can be expressed as

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{kT}\right)\right] \quad (1)$$

where

$$I_o = AA^* T^2 \exp\left(\frac{-q\Phi_{B0}}{kT}\right) \quad (2)$$

is the saturation current, $\Phi_{B0}$ is the potential barrier height, $A^*$ is the effective Richardson constant equal to 32 A $cm^{-2}k^{-2}$ for p-type Si.

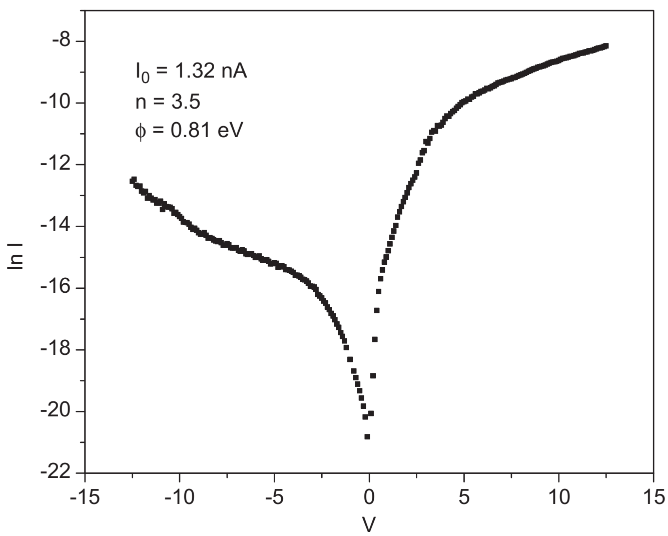


**Fig. 4.** Semi-log forward and reverse bias *I–V* characteristics of Ag/PTCDA/PEDOT:PSS/p-Si diode at room temperature.

*A* is the effective area of the diode, '*n*' is the ideality factor, *k* is the Boltzmann constant and *T* is the room temperature. The ideality factor '*n*', which is a measure of diode conformity, is taken into consideration to determine the deviation of the experimental *I–V* data from the ideal thermionic model. The ideality factor '*n*' can be determined from the following expression:

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{3}$$

The value of '*n*' was obtained from the slope of linear region of the forward bias ln *I* versus *V* plot according to Eq. (3). The value of '*n*' was found to be 3.5.

For an ideal diode the ideality factor should be close to unity but in most organic semiconductor/inorganic interfaces the value of '*n*' deviates from unity and is observed to be much greater than one. The high value of '*n*' can be attributed to a number of factors such as the perylene layer on p-Si surface, the effect of bias voltage drop across the organic/inorganic interface [30] and the secondary mechanisms at the interface. Another reason for the deviation may be either recombination of charge carriers in depletion region and/or the rise of the diffusion current for elevating voltages [31]. Moreover, the large value of '*n*' suggests that the diode does not obey an ideal Schottky diode behavior rather it follows a metal–insulator–semiconductor (MIS) configuration. The insulating layer on the p-Si surface can, probably, be formed (1) during the conventional polishing and chemical etching technique [8], (2) when the p-Si substrate is exposed to air and water vapors are adsorbed on the surface of the p-type Si substrate prior to the deposition of the organic layer [10,32] and (3) during the metal-evaporation process [8,33].

The experimental value of $\Phi_{B0}$, which exists at the metal–semiconductor interface, is obtained from the *y*-intercept of the semi-log forward bias *I–V* characteristics. The value of $\Phi_{B0}$ was calculated as 0.81 eV for the device, which is significantly greater than the typical value of 0.58 eV for the conventional Al/p-Si Schottky diode [34]. The barrier height value of about 0.81 eV indicates that contact potential barrier height exists at the interface between PTCDA and p-Si.

The Ag/PTCDA/PEDOT:PSS/p-Si Schottky diode with ideality factor value of 3.5 and barrier height value of 0.81 eV is comparable to the Schottky diodes, employing organic layers on the semiconductor substrates, previously reported in the literature. The values of barrier height and ideality factor of 0.73 eV and 2.0, respectively, for Sn/PTCDA/p-Si MIS diodes fabricated by sublimation, have been reported by Forrest et al. [17]. For a β-carotene layer on Si substrate, Aydin et al. obtained the values of 0.80 eV and 1.32 for $\Phi_{B0}$ and *n*, respectively [35]. For the structure Sn/methyl-red/p-Si/Al the barrier height and ideality factor values of 0.73 eV and 3.22 were obtained respectively. For the device with poly[2-methoxy-5-(20-ethylhexyloxy)-1,4-phenylenevinylene] (MEH-PPV) on the p-Si substrate, the $\Phi_{B0}$ and '*n*' values determined from the *I–V* characteristics were 0.80 eV and 1.88 respectively [8]. The barrier height of 0.79 eV with an ideality factor of 2.65 was determined from the *I–V* data of polymer/InSe(:Err) diodes fabricated from a thin film of metallic polypyrrole (MPP) by the anodization method [12]. Saglam et al. [13] also fabricated the diode by forming an MPP thin film on the p-Si substrate by the anodization method. They measured the *I–V* characteristics and obtained the barrier height $\Phi_{B0}$ value of 0.68 eV with an ideality factor '*n*' value of 2.

The series and shunt resistances, $R_s$ and $R_{sh}$, are very important for the device. The series resistances, as low as zero, ensure that high current will flow through the device while the shunt resistances approaching infinity correspond to small leakage current in the device. The series resistance can be obtained at positive voltages where the *I–V* curve becomes linear. The slope of *I–V* characteristics around 0 V gives the shunt resistance. A plot of junction resistance versus voltage is shown in Fig. 5. The series and shunt resistances are obtained from the graph of Fig. 5. The values of $R_s$ and $R_{sh}$ are found to be equal to 13.7 kΩ and 137 MΩ, respectively.

Furthermore, the values of barrier height and series resistance of the device have been evaluated by the analysis of Norde's method [36]. The Norde's function can be expressed as

$$F(V) = \frac{V}{\gamma} - \frac{KT}{q}\ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{4}$$

where $\gamma$ is a dimensionless quantity having a first integral value greater than '*n*'. The value of $\gamma$ in this case is '4' for the device reported here. A graph of *F*(*V*) versus *V* is shown in Fig. 6, which is used to obtain the minima on the *x* and *y* axes. The following expressions are used to determine the barrier height and series resistance:

$$\Phi_{BO} = F(V_o) + \frac{V_o}{\gamma} - \frac{kT}{q} \tag{5}$$

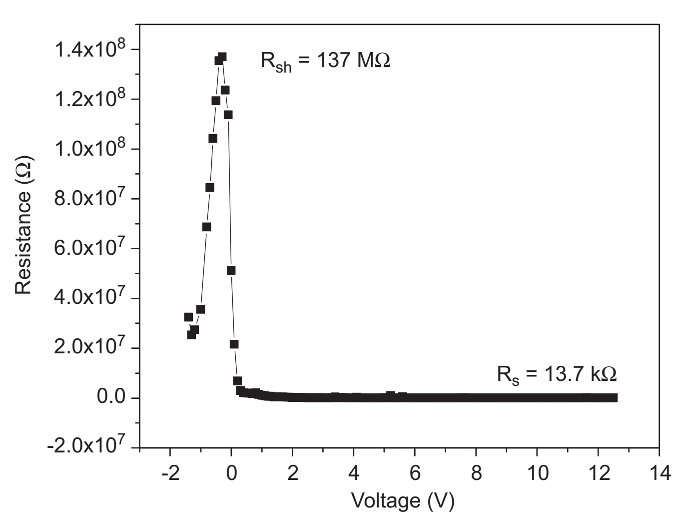


**Fig. 5.** Junction resistance, $R_s$, versus voltage for Ag/PTCDA/PEDOT:PSS/p-Si diode.

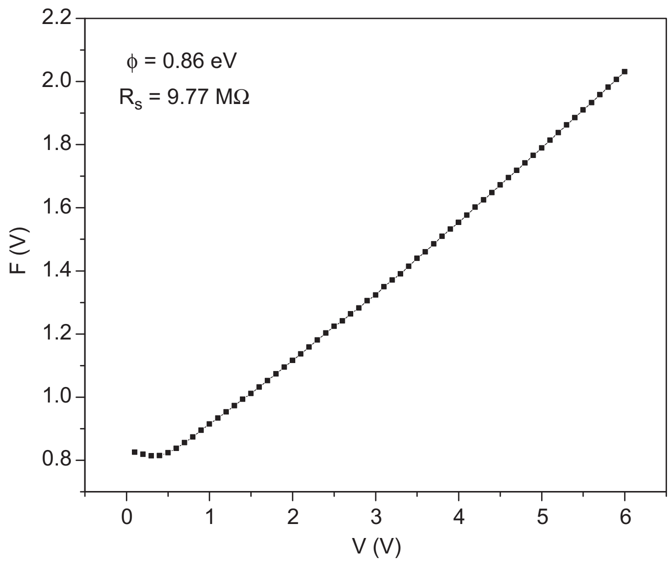


**Fig. 6.** *F*(*V*) versus voltage plot of Ag/PTCDA/PEDOT:PSS/p-Si diode.

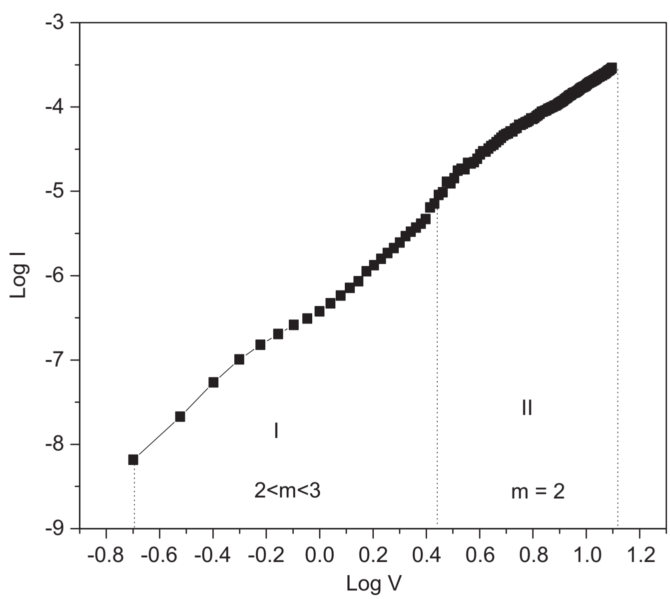


**Fig. 7.** Forward bias log(*I*) versus log(*V*) plot of the Ag/PTCDA/PEDOT:PSS/p-Si diode.

and

$$R_s = \frac{kT(\gamma - n)}{qI_o} \quad (6)$$

where $V_o$ is the minimum voltage and $F(V_o)$ is the corresponding minimum value of $F(V)$. The barrier height and series resistance calculated by Norde's method are 0.86 eV and 10 kΩ, respectively, which are in good agreement with the values calculated by the conventional *I–V* method.

The analysis of the forward bias *I–V* curves is extremely useful in providing sufficient information about the transport mechanisms controlling the conduction process in the investigated device. The experimentally measured *I–V* data, shown in Fig. 3, is re-plotted in terms of log(*I*)–log(*V*) and is shown in Fig. 7. The curves indicating different conduction mechanisms can be characterized by two distinct regions in Fig. 7. As seen from the figure, the current follows a power law of the form $J$–$V^m$. It can be observed from the figure that in region I, the slope lies between 2 and 3. In this region the dominant transport mechanism is Trap-Charge-Limited current (TCLC) with exponential distribution of traps as the slope in this region is greater than 2. In the presence of traps, the current density can be expressed as [37]

$$J_{TCLC} = \frac{9\varepsilon_o \varepsilon_r \theta \mu V^2}{8d^3} \quad (7)$$

where $\varepsilon_o = 8.85 \times 10-14\ \mathrm{F\ cm^{-1}}$ is the relative permittivity of the free space and $\varepsilon_r = 3.4$ is the relative permittivity of PTCDA [29], $\mu$ is the hole mobility, $d$ is the thickness of the film and $\theta$ is the trapping factor.

In the forward bias characteristics, the second region corresponds to the Space-Charge-Limited current (SCLC) controlled by a single dominating trap level for the value of slope of log(*I*)–log(*V*) curves equal to 2. The current density in this region can be given as

$$J_{SCLC} = \frac{9\varepsilon_s \mu V^2}{8d^3} \quad (8)$$

## 4. Conclusion

In conclusion, Ag/PTCDA/PEDOT:PSS/p-Si structure was obtained by depositing the PTCDA layer on p-Si substrate. The experimentally measured *I–V* characteristics of the device showed rectifying behavior. The Schottky diode parameters such as ideality factor, barrier height and series resistance were found to be 3.5, 0.81 eV and 13.7 KΩ, respectively. The values of ideality factor and the barrier height obtained for our device are comparable to the results achieved for PTCDA reported by Forrest et al. [17]. In the literature, a device with a thin film of PTCDA on n-Si surface was fabricated [29] and the ideality factor of the diode was 5.8, whereas, the ideality factor of Ag/PTCDA/PEDOT:PSS/p-Si was 3.5, which is lower than the '*n*' value obtained for PTCDA/n-Si. The barrier height and series resistance have been verified by Norde's method. The charge transport properties have also been investigated, which show that the space-charge limited current is dominant in the region where the voltage is above 2.5 V.

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## References

[1] S. Sze, Physics of Semiconductor Devices, 2nd ed., Wiley-Blackwell, New Jersey, USA, 1981.
[2] M. Okutan, E. Basaran, F. Yakuphanoglu, Appl. Surf. Sci. 252 (2005) 1966.
[3] R.L.V. Meirhaeghe, W.H. Laflere, F. Cardon, J. Appl. Phys. 76 (1994) 403.
[4] E. Rhoderick, R. Williams, Metal–Semiconductor Contacts, Oxford, Clarendon, 1988.
[5] P. Hanselaer, W. Laflere, R. Van Meirhaeghe, F. Cardon, J. Appl. Phys. 56 (1984) 2309.
[6] P. Hanselaer, W. Laflére, R. Meirhaeghe, F. Cardon, Appl. Phys. A: Mater. Sci. Process. 39 (1986) 129.
[7] Ş. Karataş, C. Temirci, M. Çakar, A. Türüt, Appl. Surf. Sci. 252 (2006) 2209.
[8] M.E. Aydin, F. Yakuphanoglu, J.H. Eom, D.H. Hwang, Phys. B: Conden. Matter 387 (2007) 239.
[9] S.R. Forrest, M.L. Kaplan, P.H. Schmidt, W.L. Feldmann, E. Yanowski, Appl. Phys. Lett. 41 (1982) 90.
[10] S. Antohe, N. Tomozeiu, S. Gogonea, Phys. Status Solidi (a) 125 (1991) 397.
[11] M. Çakar, Y. Onganer, A. Türüt, Synth. Met. 126 (2002) 213.

[12] B. Abay, Y. Onganer, M. Sağlam, H. Efeoğlu, A. Türüt, Y.K. Yoğurtçu, Microelectron. Eng. 51–52 (2000) 689.
[13] M. Sağlam, D. Korucu, A. Türüt, Polymer 45 (2004) 7335.
[14] A.M. Cowley, S.M. Sze, J. Appl. Phys. 36 (1965) 3212.
[15] H. Card, E.H. Rhoderick, J. Phys. D: Appl. Phys. 4 (1971) 1589.
[16] H.-H. Tseng, C.-Y. Wu, Solid-State Electron. 30 (1987) 383.
[17] S. Forrest, M. Kaplan, P. Schmidt, J. Appl. Phys. 56 (1984) 543.
[18] S. Forrest, P. Schmidt, J. Appl. Phys. 59 (1986) 513.
[19] P. Gawrys, D. Boudinet, M. Zagorska, D. Djurado, J.-M. Verilhac, G. Horowitz, J. Pécaud, S. Pouget, A. Pron, Synth. Met. 159 (2009) 1478.
[20] W.R. Salaneck, K. Seki, A. Kahn, J.J. Pireaux, Conjugated Polymer and Molecular Interfaces: Science and Technology for Photonic and Optoelectronic Application, Marcel Decker, New York, 2002.
[21] S. Heutz, A. Ferguson, G. Rumbles, T. Jones, Org. Electron. 3 (2002) 119.
[22] J. Xue, S.R. Forrest, Phys. Rev. B 69 (2004) 245322.
[23] L. Chkoda, C. Heske, M. Sokolowski, E. Umbach, Appl. Phys. Lett. 77 (2000) 1093.
[24] S.R. Forrest, L.Y. Leu, F.F. So, W.Y. Yoon, J. Appl. Phys. 66 (1989) 5908.
[25] T. Ogawa, K. Kuwamoto, S. Isoda, T. Kobayashi, N. Karl, Acta Crystallogr. Sect. B: Struct. Sci. 55 (1999) 123.
[26] M. Tucci, D. Caputo, J. Non-cryst. Solids 338 (2004) 780.
[27] G. Sharma, D. Saxena, M. Roy, Thin Solid Films 467 (2004) 220.
[28] T. Kılıçoğlu, Thin Solid Films 516 (2008) 967.
[29] A. Farag, W. Osiris, I. Yahia, Synth. Met. 161 (2011) 1805.
[30] İ. Dökme, T. Tunç, İ. Uslu, Ş. Altındal, Synth. Met. 161 (2011) 474.
[31] M. El-Nahass, K. Abd-El-Rahman, A. Farag, A. Darwish, Org. Electron. 6 (2005) 129.
[32] A. Turut, F. Koleli, J. Appl. Phys. 72 (1992) 818.
[33] T. Kılıçoğlu, M.E. Aydın, Y.S. Ocak, Phys. B: Condens. Matter 388 (2007) 244.
[34] E.H. Rhoderick, Metal–Semiconductor Contacts, Clarendon Press, Oxford, England, 1978.
[35] M.E. Aydın, T. Kılıçoğlu, K. Akkılıç, H. Hoşgören, Phys. B: Condens. Matter 381 (2006) 113.
[36] H. Norde, J. Appl. Phys. 50 (1979) 5052.
[37] A. Farag, I. Yahia, T. Wojtowicz, G. Karczewski, J. Phys. D: Appl. Phys. 43 (2010) 215102.