



Temperature dependence of photovoltaic performance of silicon heterojunction solar cells based on gallium- and phosphorous-doped silicon wafers



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ABSTRACT

Silicon-based solar cells (SCs) are widely used in space applications, particularly for powering satellites in low Earth orbit (LEO), where their photovoltaic (PV) performance is strongly influenced not only by charged-particle irradiation but also by extreme temperature fluctuations. Under such conditions, the reliability and efficiency of SCs are critical for long-term operation. In this study, we investigate the temperature dependence of the PV performance of silicon heterojunction (HJT) SCs fabricated on gallium- and phosphorus-doped crystalline silicon (c-Si) wafers under the AM0 spectrum (136.7mW/cm²) in the temperature range of 173–373 K. The experimental results show that the short-circuit current density (J_{sc}) of both cell types increases linearly with temperature, exhibiting positive temperature coefficient (TC)s of 0.054 %/K for n-type and 0.058 %/K for p-type wafers, whereas the open-circuit voltage (V_{oc}) decreases. For n-type HJT SCs, V_{oc} demonstrates a more complex behavior: it increases from 0.547 V at 373 K to 0.693 V at 223 K, after which the increase slows down, reaching 0.815 V at 173 K. This behavior was successfully explained using a theoretical model that showed good agreement with the experimental data. At low temperatures (T < 233 K), n-type HJT SCs exhibited an s-shaped light current–voltage characteristics (J-V curves) near V_{oc} , attributed to an unfavorable potential barrier at the (p^+)a-Si:H/(n)c-Si-heterojunction caused by a high valence band offset (ΔE_V). The TC of the maximum output power (P_{max}) was –0.31 %/K for n-type (273–373 K) and –0.20 %/K for p-type HJT SCs (173–373 K), indicating that p-type SCs exhibit a more favorable TC of P_{max} , making them promising candidates for LEO applications.

1. Introduction

At present, SCs based on single-crystalline technology have become dominant in silicon-based production, including amorphous, micro-amorphous, polycrystalline, micro-, nano-, and multicrystalline silicon (Si) types (Sopian et al., 2017; Ballif et al., 2022). Their share in the global PV market accounts for more than 95 % due to mature fabrication technology, abundant raw materials, cost-effectiveness, and reliable performance (Ballif et al., 2022; Kostylyov et al., 2025; Stefani et al., 2023). Single-crystalline SCs continue to offer stable, durable, and efficient light-to-electricity conversion, especially for terrestrial applications (Stefani et al., 2023; Fischer et al., 2022).

HJT SCs have attracted considerable attention among silicon-based PV technologies owing to their high-efficiency architecture and superior interface properties (Stefani et al., 2023; Razzaq et al., 2022). These devices combine the advantages of c-Si with thin intrinsic and doped hydrogenated amorphous silicon (a-Si:H) layers in relatively simple and low-temperature manufacturing processes (Razzaq et al., 2022; Wolf et al., 2012; Chavali et al., 2018; Taguchi, 2021). HJT SCs exhibit high V_{oc} and improved output power, primarily due to superior interface passivation and reduced surface recombination losses (Razzaq et al., 2022). As a result, they have achieved high conversion efficiencies of 27.1 % for n-type cells and 26.6 % for p-type cells by LONGi lab. compared to PERC (Passivated Emitter and Rear Contact) and

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conventional homojunction cells (Lv et al., 2025; Ru et al., 2024; Kan-neboina, 2022). Recently, LONGi introduced new silicon heterojunction back-contact (HBC) SCs based on HJT technology, which set a new world record for c-Si SCs by achieving a conversion efficiency (η) of 27.3 % (Su et al., 2025; Green et al., 2024).

Historically, heterojunctions based on *a*-Si/*c*-Si were first investigated by W. Fuhs and co-workers in 1974 (Fuhs et al., 1974). A few years later, intrinsic *a*-Si:H layers were shown to provide excellent surface passivation for *c*-Si wafer (Pankove and Targ, 1979). The first practical *a*-Si:H/*c*-Si HJT SCs were fabricated in the 1990s by Sanyo Company, where deposition of a boron-doped *a*-Si:H layer on the front side of an *n*-type *c*-Si wafer and an aluminum (Al) back contact resulted in a conversion efficiency of 12.3 % and a modest fill factor (FF) of 74 % (Taguchi et al., 1990). A year later, the company patented the *a*-Si/*c*-Si heterojunction SCs under the trademark HIT (Heterojunction with Intrinsic Thin layer) (Tanaka et al., 1992). Since then, HJT technology has advanced considerably, demonstrating continuous improvements in both efficiency and stability, and within a relatively short period, achieving record-breaking performance levels. Currently, HJT SCs have a higher bifacial coefficient compared to other silicon-based PV technologies (Joseph et al., 2025). These advantages make HJT SCs highly attractive not only for terrestrial applications but also for space applications, where efficiency and stability are essential.

Since the launch of the first Soviet satellite, Sputnik 1, on October 4, 1957, for space exploration (Verduci et al., 2022), Si SCs have been widely adopted as a primary power source for satellites, owing to their long-term operational stability (Utamuradova et al., 2025a,b), mature fabrication technologies (Sark, 2016), and favorable power-to-mass ratio (Verduci et al., 2022; ur Rehman et al., 2016; Kaltenbrunner et al., 2015). In space environments, where conventional energy storage systems such as electrochemical batteries and fuel cells are unsuitable for long-term missions due to their limited capacity, safety issues, and their heavy weight (Verduci et al., 2022; Datas and Marti, 2017). Therefore, radiation-tolerant, high-efficiency, and lightweight SCs are essential for powering spacecraft systems.

In recent years, HJT SCs have gained increasing interest for space missions – especially for deployment in LEO (500–2000 km), in addition to their widespread use in terrestrial applications (Verduci et al., 2022; Utamuradova et al., 2024). However, SCs operating in LEO face not only high-energy particle radiation but also extreme temperature fluctuations (Lu et al., 2019; Matsuda et al., 1982; Buitrago-Leiva et al., 2024).

To date, most studies have evaluated the performance of SCs under standard test conditions (STC) at the AM1.5G (100 mW/cm²) radiation spectrum and within moderate temperature ranges (from 10 °C to 80 °C), with limited data available for temperatures below 0 °C (Le et al., 2021; Singh et al., 2008; Haschke et al., 2017; Le et al., 2023). In terrestrial applications, the PV performance of SCs is primarily governed by ambient temperature, and typically, each 1 °C increase above 25 °C results in a measurable decrease in η (Bamisile et al., 2025). In contrast, when these SCs are employed to power spacecraft in LEO, they are subjected to severe cyclic temperature variations along with radiation exposure. According to (Thirsk et al., 2009; Cardinaletti et al., 2018), spacecrafts in LEO travel at about 8 km/s, and complete one orbit around the Earth every 90 min. When a spacecraft enters the sunlit side of Earth's orbit, the temperature on the surface of SCs can reach over 100 °C (373 K) due to direct solar irradiation. Approximately 45 min later, as the spacecraft enters, exits, or remains within Earth's umbra, the temperature drops to around - 100 °C (173 K). Thus, this repeated light-dark transition every 45 min causes periodic fluctuations in the power output of solar modules. Therefore, performing detailed temperature-dependent measurements is crucial for assessing the operational stability and reliability of HJT SCs under AM0 conditions relevant to space environments.

Based on the above discussion, one of the urgent tasks is to study the temperature dependence of the output PV performances of HJT SCs fabricated on gallium-doped (*p*-type) and phosphorus-doped (*n*-type) *c*-

Si substrates under AM0 spectrum (136.7 mW/cm²) in the temperature range of 173–373 K, and to determine which cell type demonstrates superior suitability for operation in space environments, particularly under thermal conditions typical of LEO.

In this study, all HJT SCs were fabricated on both *n*-type (phosphorus-doped) and *p*-type (gallium-doped) *c*-Si substrates using the standard fabrication process originally optimized for *n*-type HJT SCs. It should be noted that the same fabrication process was applied to the *p*-type HJT SCs without specific optimization.

2. Material preparation and methods

2.1. Sample preparation

The investigated HJT SCs were fabricated at the R&D Center of Thin Film Technologies in Energetics (Saint-Petersburg, Russian Federation). To conduct the study, HJT SCs (Fig. 1) were created on phosphorus-doped *n*-type and gallium-doped *p*-type *c*-Si substrates grown by the Czochralski (Cz) method. The substrate parameters were as follows: for *n*-type *c*-Si, the donor concentration was $N_d \geq 10^{15} \text{ cm}^{-3}$, the thickness was ~125 μm, and the initial bulk minority carrier lifetime was $\tau_{\text{bulk}} \geq 1 \text{ ms}$; for *p*-type *c*-Si, the acceptor concentration was $N_a \geq 4.2 \times 10^{16} \text{ cm}^{-3}$, the thickness was ~135 μm, and $\tau_{\text{bulk}} \geq 0.2 \text{ ms}$. Both types of substrates had the same crystallographic orientation, namely (100).

Before depositing intrinsic and doped hydrogenated amorphous silicon (*a*-Si:H) layers onto the *n*-type and *p*-type *c*-Si substrates to form the heterojunctions, the substrates underwent a wet chemical cleaning procedure. Afterward, to minimize incident-light reflection and enhance the J_{sc} of the HJT SCs, the *c*-Si substrates were subjected to pyramidal surface texturing (Ataboev et al., 2021). Subsequently, thin intrinsic *a*-Si:H buffer layers (~5 nm thick) were deposited on both the front and rear surfaces of the textured *n*-type and *p*-type *c*-Si substrates using the Radio-Frequency Plasma-Enhanced Chemical Vapor Deposition (RF PECVD) method in a Gen5 KAI-1200 system (Oerlikon, Switzerland). The intrinsic *a*-Si:H layers were deposited using high-purity (99.999 %) monosilane gas (SiH₄) with a flow of 40 sccm as the precursor. The purpose of this layer is to passivate dangling bonds at the surfaces and defects in the bulk of *c*-Si (by forming Si-H bonds), thereby reducing recombination losses of photogenerated charge carriers and enhancing the overall performance of the HJT SCs (Wolf et al., 2008; Pankove et al., 1979; Hammann et al., 2025; Vikhrov et al., 2018).

Using the same method to form a *p*-*n*-junction, *p*-type and *n*-type *a*-Si:H layers were deposited on the front side of the *i*-*a*-Si:H coated *n*-type and *p*-type *c*-Si substrates, respectively. Simultaneously, to create the back-surface field (BSF), *n*-type and *p*-type *a*-Si:H layers were deposited on the rear sides of *i*-*a*-Si:H deposited *n*-type and *p*-type *c*-Si substrates. The thicknesses of both the front and rear *p*-type and *n*-type *a*-Si:H layers were kept identical, measuring ~10–15 nm. The purpose of the BSF is to provide additional field-effect passivation by reflecting and accelerating minority charge carriers from the *a*-Si:H/*c*-Si interface at the rear side, thereby further reducing recombination losses. To achieve *p*-type and *n*-type conductivity in the *a*-Si:H layers, respectively, the monosilane (SiH₄) gas was diluted with high-purity (99.999 %) diborane (B₂H₆) and phosphine (PH₃) gases. All *a*-Si:H layers were deposited at a low temperature of 180–185 °C using a glow discharge plasma with a power of 200 W and a frequency of 40.68 MHz. This low-temperature processing prevents degradation of the bulk minority carrier lifetime, which typically occurs during high-temperature processing of low-quality *c*-Si substrates (Maydell et al., 2006). The thinnest of the *p*-type and *n*-type *a*-Si:H layers is dictated by the inherently low electrical conductivity (i.e., high resistivity) of doped *a*-Si:H as well as parasitic light absorption within these layers. This parasitic absorption leads to a reduction in both the J_{sc} and the fill factor (FF) of HJT SCs (Sark, 2016; Maydell et al., 2006; Saive et al., 2017; Jensen et al., 2002). Further, transparent conductive oxide (TCO) layers composed of indium tin oxide (ITO – 90 wt% In₂O₃ and 10 wt% SnO₂) were deposited on the front and rear

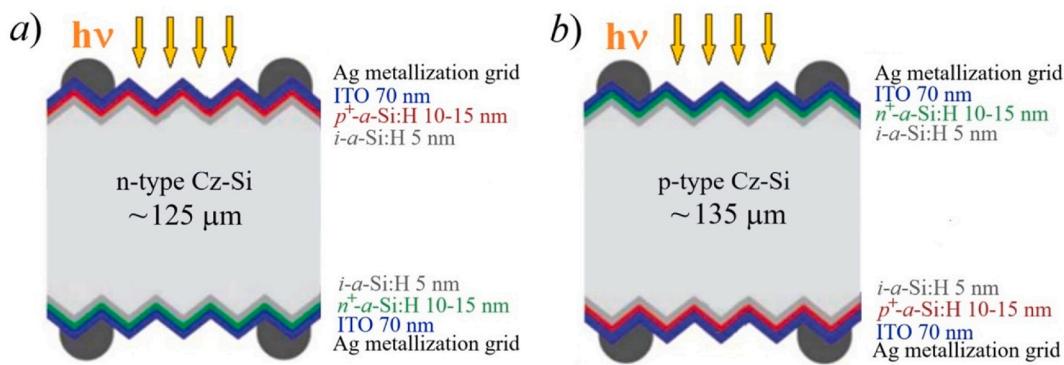


Fig. 1. A cross-sectional view of the finished HJT SCs based on *n*-type (a) and *p*-type (b) c-Si substrates.

surfaces of the photosensitive heterostructures using Radio-Frequency (RF) magnetron sputtering. The deposited ITO layers enable efficient charge carrier transport and collection at both electrodes. Furthermore, these TCO layers serve dual functions: enhancing lateral carrier conduction while simultaneously acting as an anti-reflection coating on both sides of the SCs (Razzaq et al., 2022; Wolf et al., 2012). To collect photogenerated charge carriers from the heterostructure surfaces, low-temperature silver (Ag) paste with Busbar-type contacts was screen-printed onto both the front and rear sides of the photosensitive heterostructures. The limited thermal budget is primarily determined by the thermal instability of the *a*-Si:H surface passivation. At elevated temperatures (>250 °C), chemical passivation deteriorates due to the breaking of Si–H bonds at the *a*-Si:H/c-Si interface, resulting in an increased density of interface defect states (Li et al., 2018). The “Busbar” type contacts had a height of ~ 25 μm, a width of ~ 45 μm, and were patterned with a pitch of ~ 1.36 mm. These parameters were measured using a KLA/Tencor Alpha-Step D-120 profilometer. Subsequently, the fabricated HJT SCs underwent thermal annealing at 200 °C for 20 min in ambient air. This step served two primary purposes: (1) to stabilize the *a*-Si:H layers before electrical characterization, and (2) to cure the screen-printed Ag contacts. Annealing at this temperature is also crucial, as it promotes hydrogen migration within the *a*-Si:H layer toward the *a*-Si:H/c-Si heterointerface, thereby significantly reducing the density of dangling bonds at the interface (Seif et al., 2015; Olibet et al., 2007).

2.2. Characterization and measurement of performances

To perform experiments, both *n*-type and *p*-type c-Si-based samples with an area of 1×1 cm 2 were cut from full-sized HJT SCs (original dimensions: 15.6×15.6 cm 2). No additional passivation of the lateral surfaces or edge isolation was performed after laser cutting. A solid-state “MiniMaker2” diode laser, with a wavelength of 1064 nm and a maximum power of 20 W, was used for cutting the samples. During laser scribing, the laser parameters were set as follows: a scribing speed of 200 mm/s, a pulse repetition rate of 20 kHz, and a pulse duration of 10 ns, while the laser power was maintained at 90 % of its maximum value. To minimize edge shunting in the samples, laser scribing was performed prior to the mechanical cleaving of the HJT SCs. The scribing process was carried out on the rear side of the *p-n*-junction for both substrate types, which helped to reduce potential damage to the contact layers and maintain photoelectric conversion efficiency.

According to previous studies (Witteck et al., 2016; Han et al., 2022), considerable attention has recently been devoted to improving the overall efficiency of PV modules compared with conventional full-cell designs. One of the most effective approaches involves dividing standard SCs into half-cells, thereby reducing the cell current and minimizing resistive losses. Moreover, this design mitigates the performance degradation of PV modules under partial shading conditions, which would otherwise increase resistance and potentially lead to module

failure. Therefore, two main techniques are currently widely employed for SC separation: laser scribing with mechanical cleaving (LSMC) and thermal laser separation (TLS). However, despite their technological advantages, it has been reported (Lv et al., 2025) that the cutting process can slightly deteriorate the electrical performance of SCs due to enhanced edge recombination, reduced passivation quality, and increased series resistance. In the present study, the above-mentioned LSMC method was applied, and a significant degradation in the electrical performance of the HJT SCs was observed after the cutting process. To assess the effect of laser cutting on the PV performance of HJT SCs, light J-V curves were measured before and after cutting under STC (AM1.5G spectrum, 100 mW/cm 2 , 25 °C), using a SCIENTECHEM UM-UHE-NL solar simulator and a Keithley SM2460 source meter. The measurement was conducted at the “Photoelectronics” laboratory of S. A. Azimov Physical-Technical Institute, Academy of Sciences of the Republic of Uzbekistan. The obtained results are presented in Table 1. Where, V_{OC} – open-circuit voltage, J_{SC} – short-circuit current density, FF – fill factor, η – conversion efficiency, R_s – series resistance, R_{sh} – shunt resistance, k – bifacial coefficient of SC. Bifacial coefficient (k) is defined as the ratio of power generated from the rear surface to that generated from the front surface (Joseph et al., 2025).

As evidenced by the data presented in Table 1, the key PV parameters of HJT SCs based on *n*-type and *p*-type c-Si exhibit a noticeable decrease after laser cutting.

To study the effect of temperature on the output PV performance of HJT SCs, light J-V curves were measured using a liquid nitrogen cryostat (Janis VPF-100) in the temperature range of 173–373 K, with a 20 K step. During the measurements, the samples were illuminated using a class AAA pulsed solar simulator (SS-80AAA simulator) under AM0 spectral conditions (136.7 mW/cm 2). The J_{SC} and V_{OC} were recorded using a Keithley SM2460 Source Meter.

Temperature stabilization during the measurements was achieved using a liquid nitrogen cryostat equipped with temperature monitoring and active heating control. A Lake Shore Model 335 temperature

Table 1

Output parameters of HJT SCs based on *n*-type and *p*-type c-Si before and after cutting, measured under AM1.5G at room temperature.

Type	V_{OC} , V	J_{SC} , mA/cm 2	FF, %	η , %	R_s , Ω·cm 2	R_{sh} , Ω·cm 2	k , %
Before cutting (15.6 × 15.6 cm2)							
<i>n</i> -c-Si	0.738	37.2	82.1	22.5	2.2×10^{-3}	6011	93.4
<i>p</i> -c-Si	0.731	37.9	76.6	21.2	3.1×10^{-3}	1080	87.1
After cutting (1 × 1 cm2)							
<i>n</i> -c-Si	0.69	36.1	73.8	18.4	2.1	1350	82.5
<i>p</i> -c-Si	0.686	36.9	67.5	17.1	2.3	454	70.4

controller was used, providing a control accuracy of ± 0.1 °C. Each light J-V curve measurement was conducted after the target temperature was reached and maintained for 4–5 min under the AM0 spectrum (136.7 mW/cm²). After completing the full temperature cycle, an additional measurement was carried out at 25 °C to verify that thermal cycling had not induced any changes in the electrical properties of the HJT SCs. Temperature coefficients of the output parameters of the HJT SCs, such as V_{OC} , J_{SC} , FF , P_{max} and η were extracted from the slopes of the linear regions of the experimental temperature-dependent curves.

For the investigation, about 20 HJT SCs samples of each type of conductivity were fabricated. These samples exhibited similar parameters within a margin of error of no more than 2 %. From these, two samples with an area of 1×1 cm² – one based on *n*-type and the other on *p*-type c-Si were selected for temperature-dependence measurements.

This study focuses on characterizing the temperature-dependent performance of *n*-type and *p*-type c-Si HJT SCs across a broad operational range (173–373 K), without considering radiation effects. Future studies will focus on examining the combined impact of radiation and temperature on the operational capabilities of the HJT SCs.

3. Modeling the temperature dependence of the open-circuit voltage

It is well established that the key PV parameters of HJT SCs, such as the V_{OC} , J_{SC} , FF , P_{max} and η exhibit significant temperature dependence (Kumar and Jain, 2025; Acharyya et al., 2024). Among these parameters, V_{OC} is the most temperature-sensitive, decreasing pronouncedly with increasing temperature. This in turn leads to a significant reduction in the η of the HJT SCs (Le et al., 2021).

The complex temperature dependence of the experimental V_{OC} for HJT SCs fabricated on *n*-type c-Si substrates, as shown in Fig. 6a, was interpreted using the previously developed current transport model for the HJT SCs (Panaiotti and Terukov, 2019; Sachenko et al., 2015). This method, which relies on the experimental J_{SC} values, allows the calculation of SC performance characteristics under arbitrary carrier injection levels and any ratio of the carrier diffusion length (L_{diff}) to the substrate thickness (d).

According to (Panaiotti et al., 2020), the HJT structure is considered as a p^+ -*n*- n^+ -diode, with the c-Si substrate acting as its base (Fig. 2). Furthermore, the p^+ -*n*- and *n*- n^+ -heterojunctions form sufficiently high potential barriers for electrons and holes, respectively (Panaiotti et al., 2020):

$$J_p(x=0) \approx J \text{ and } J_n(x=d) \approx J, \quad (1)$$

Where, $J < 0$ denotes the projection of the total current density vector J onto the x -axis (Fig. 2), while J_p and J_n – represent the x -components of the hole and electron current densities, respectively. Here, the x -axis is oriented from the p^+ -*n*-heterojunction toward the *n*- n^+ heterojunction (Fig. 2).

The space charge region (SCR) of the p^+ -*n*-heterojunction extends only a few micrometers into the c-Si substrate, so the thicknesses of the quasi-neutral *n*-base and the substrate itself are practically identical. Owing to the extremely weak electric field in the *n*-base at current

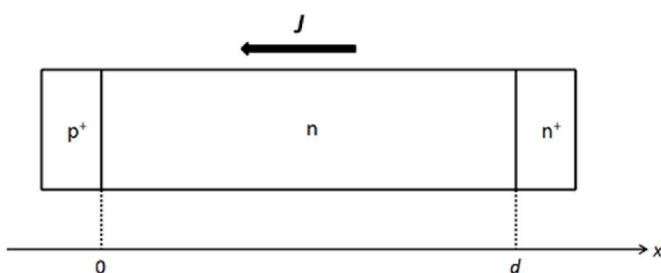


Fig. 2. Structure of HJT SCs.

densities relevant to HJT SCs, carrier transport is governed primarily by diffusion, and the drift contribution can be neglected. Under both maximum power point and open-circuit conditions, the concentrations of excess charge carriers, Δp , can become comparable to or even significantly exceed the donor doping concentration N_d . Therefore, calculations must simultaneously account for both the reduction in carrier lifetime due to Auger recombination mechanisms and the ambipolar nature of their diffusive transport.

The spatial distribution of the excess hole concentration - $\Delta p(x)$ within the *n*-base can be determined by solving the one-dimensional steady-state continuity equation for holes within the diffusion approximation, subject to appropriate boundary conditions:

$$\frac{d\Delta p}{dx} = -\frac{J - J_{surf}}{qD} \text{ at } x = 0, \frac{d\Delta p}{dx} = 0 \text{ at } x = d, \quad (2)$$

where, q – elementary charge, $J_{surf} > 0$ – the projection of the total surface recombination current density vector onto the x -axis. $J_{surf} = qS_0\Delta p(x=0) + qS_d\Delta p(x=d)$, S_0 and S_d – surface recombination velocity on the front and rear surfaces of substrate,

$$D = D_p \frac{2b\Delta p + bN_d}{\Delta p(b+1) + bN_d}, \quad (3)$$

– ambipolar diffusion coefficient (Utamuradova et al., 2025a,b), D_p – diffusion coefficient of holes, b – ratio of electron and hole mobilities in c-Si ($b = \mu_n/\mu_p$).

Numerical estimates reveal that within the considered current density range, the values of D and $L_{diff} = \sqrt{D\tau}$ exhibit weak dependence on the coordinate x , where $\tau = [\tau_0^{-1} + \tau_{Auger}^{-1}]^{-1}$ – the resulting bulk carrier lifetime in the *n*-base. $\tau_{Auger} = [C_n(N_d + \Delta p)^2 + C_p(N_d + \Delta p)\Delta p]^{-1}$ – carrier lifetime under Auger recombination, $C_n = [2.8 \cdot 10^{-31} + (2.5 \cdot 10^{-22})/(N_d + \Delta p)^{0.5}]$ cm⁶/s, $C_p = 10^{-31}$ cm⁶/s (Sachenko et al., 2015). In this case, the continuity equation for holes has an analytical solution, which can be employed to drive the J-V curves of the HJT SCs (Panaiotti and Terukov, 2019; Panaiotti et al., 2020).

$$J = -J_{SC} + \frac{qD\Delta p(x=0)}{L_{diff}} \tan h\left(\frac{d}{L_{diff}}\right) + J_{surf}. \quad (4)$$

The voltage V drops across the HJT SC structure is predominantly determined by the forward bias applied to the p^+ -*n* heterojunction (Panaiotti and Terukov, 2019; Sachenko et al., 2015; Panaiotti et al., 2020):

$$V = \frac{kT}{q} \ln \left\{ \frac{\Delta p(x=0)[\Delta p(x=0) + N_d]}{n_i^2(T)} \right\}, \quad (5)$$

where, $n_i(T)$ – the intrinsic equilibrium carrier concentration in the substrate at a given temperature T , k – Boltzmann constant.

Under open-circuit conditions ($J = 0$) mode, the excess carrier concentration is uniform across all cross-sections of the substrate ($(\Delta p(x) = const)$ and,

$$\Delta p(V_{OC}) = \frac{J_{SC}}{q \left[\frac{D}{L_{diff}} \tanh \left(\frac{d}{L_{diff}} \right) + S \right]}, \quad (6)$$

where, $S = S_0 + S_d$.

Open circuit voltage V_{OC} can be estimated as

$$V_{OC}(T) = \frac{E_g(T)}{q}$$

$$q \frac{kT}{q} \ln \left\{ \frac{N_{CO} N_{VO}}{\left[\frac{J_{SC}(T)}{q \left(\frac{d}{L_{diff}} \tan h \left(\frac{d}{L_{diff}} \right) + S(T) \right)} \right] \left[N_d(T) + \frac{J_{SC}(T)}{q \left(\frac{d}{L_{diff}} \tan h \left(\frac{d}{L_{diff}} \right) + S(T) \right)} \right]} \left(\frac{T}{T_0} \right)^3 \right\}, \quad (7)$$

where, N_{CO} and N_{VO} – effective density of states in conduction and valence band at $T_0 = 300 K$.

If $L_{diff} = \sqrt{D \cdot \tau} \gg d$, expression (7) has a following form:

$$V_{OC}(T) = \frac{E_g(T)}{q} - \frac{kT}{q} \ln \left\{ \frac{N_{CO} N_{VO}}{\left[\frac{J_{SC}(T)}{q \left(\frac{d}{\tau(T)} + S(T) \right)} \right] \left[N_d(T) + \frac{J_{SC}(T)}{q \left(\frac{d}{\tau(T)} + S(T) \right)} \right]} \left(\frac{T}{T_0} \right)^3 \right\}. \quad (8)$$

Using the above expression, the more complex experimental $V_{OC}(T)$ dependence can be consistently interpreted.

4. Results and discussion

For investigating the effect of temperature on PV performance of HJT SCs fabricated on n-type and p-type c-Si substrates, light J-V curves were measured under AM0 spectrum (136.7 mW/cm^2) in the temperature range of 173 – 373 K (Fig. 3 a and 3 b). As shown in Fig. 3 a and 3 b, ambient temperature has a pronounced impact on the shape of the light J-V curves. Specially, the J_{SC} increases slightly with rising temperature, while the V_{OC} exhibits a decreasing trend. The obtained results reveal that at temperatures below 233 K , the light J-V curves of HJT SCs fabricated on n-type c-Si substrate exhibit an s-shaped behavior near the V_{OC} (Fig. 3 a). As the temperature increases, this s-shaped behavior progressively diminishes in the vicinity of V_{OC} . However, this s-shaped behavior is not observed in the light J-V curves for HJT SCs fabricated on p-type c-Si substrates within the investigated temperature range (see Fig. 3 b). It is well established that the appearance of s-shaped behavior in the light J-V curves at low temperatures leads to a significant reduction in both the FF and η of HJT SCs due to increasing series resistance (R_s) (Gudovskikh et al., 2010; Saive, 2019).

To investigate the origin of the s-shaped behavior observed in the light J-V curves of the HJT SCs, energy band diagrams were constructed for the SCs fabricated on n-type (Fig. 4 a) and p-type (Fig. 4 b) c-Si substrates. In the HJT SCs, the main potential barrier responsible for the separation of photogenerated charge carriers between the base and

emitter is formed at the p^+ -n-heterojunction for n-type c-Si and n^+ -p-heterojunction for p-type c-Si, respectively. Consequently, this part of the heterostructure is illustrated in the corresponding energy band diagram (Fig. 4 a and b). These energy band diagrams were constructed using the Anderson model under thermal equilibrium conditions at room temperature. The conduction band offset (ΔE_c) and valence band offset (ΔE_V) at the a-Si:H/c-Si heterointerface were calculated using the Anderson model (Anderson, 1962). The calculation yielded values of approximately 0.15 eV and 0.45 eV , respectively. These calculations utilized electron affinity values of 4.05 eV for c-Si and 3.9 eV for a-Si:H (Gudovskikh et al., 2005; Lu et al., 2011). The ΔE_V was calculated using the following equation,

$$\Delta E_V = (E_{g1} - E_{g2}) - \Delta E_c, \quad (9)$$

where, $E_{g1} = 1.72 \text{ eV}$ and $E_{g2} = 1.12 \text{ eV}$ represent the bandgaps of a-Si:H and c-Si, respectively, at room temperature (Gudovskikh et al., 2005). Also, the band gap of thin a-Si:H layers was determined using Tauc's method, derived from the spectral dependence of $(ahv)^{1/2}$ on hv (Abdulraheem et al., 2014).

As described by equation (9), the ΔE_V is determined by the bandgap difference between the two contacting semiconductors and the ΔE_c . Since the bandgaps of both semiconductors exhibit temperature dependence, the ΔE_V consequently varies with temperature. For the investigated heterostructure, $\Delta E_V = 0.45 \text{ eV}$ at room temperature, however, this value increases at lower temperatures due to the enhanced bandgap difference ($E_{g1} - E_{g2}$) (Gal et al., 1985; Tanaka and Yamasaki, 1987). According to (Jensen et al., 2002; Descoeuilles et al., 2013; Schmidt et al., 2004), the optimal valence band offset should be $\Delta E_V = 0.45 \text{ eV}$ for achieving the highest values of V_{OC} and FF at room temperature, as this offset minimizes carrier recombination at the a-Si:H/c-Si heterointerface.

First, let us consider the fundamental physical processes occurring in HJT SCs fabricated on n-type c-Si substrates through analysis of their energy band diagram (Fig. 4 a). It is well known that under illumination, electron-hole pairs generated in the n-type base of the HJT SCs are separated by the built-in electric field of the p^+ -n-heterojunction. The photogenerated holes (minority carriers in n-type c-Si, denoted by a circled plus symbol (\oplus)) are injected into the p^+ -region (emitter) under the built-in electric field (Fig. 4 a). In this case, as illustrated in Fig. 4 a, holes experience a spike that acts as an energy barrier to hole transport (Lu et al., 2011). To contribute to charge transport, holes must overcome the barrier of $\Delta E_V = 0.45 \text{ eV}$, which arises at the p^+ -n-heterojunction due to band alignment between the two types of semiconductors brought into contact (Zeman and Zhang, 2012). As temperature decreases, the ΔE_V increases, as a result, the spike-barrier impedes hole transport, reducing the fraction of holes that overcome the potential barrier. Consequently, holes accumulate near the front (p^+) a-Si:H/(n)

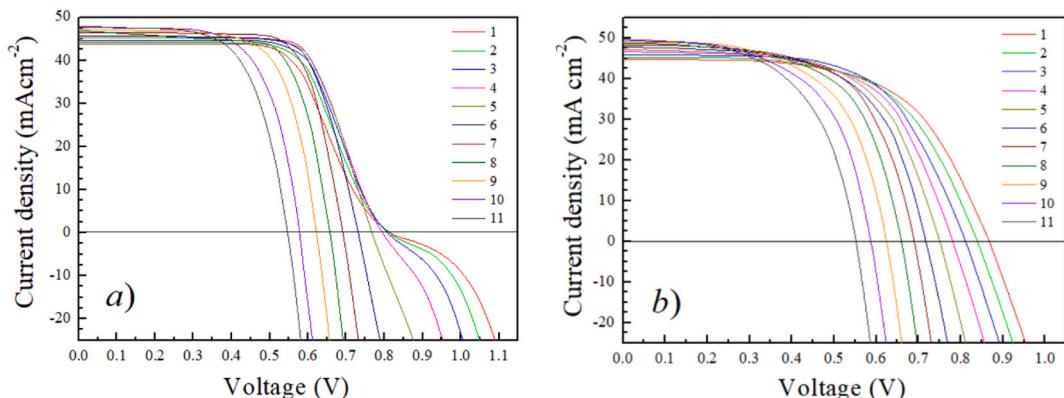


Fig. 3. Light J-V curves of HJT SCs based on n-type (a) and p-type (b) c-Si substrates under AM0 spectrum (136.7 mW/cm^2) in the temperature range of 173 – 373 K . T, K: 1–173, 2–193, 3–213, 4–233, 5–253, 6–273, 7–293, 8–313, 9–333, 10–353, 11–373.

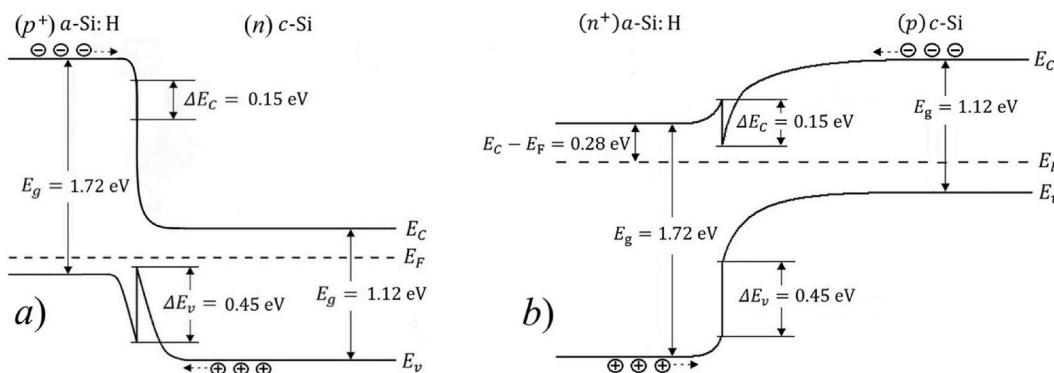


Fig. 4. Energy band diagrams of HJT SCs based on *n*-type (a) and *p*-type (b) c-Si substrates, illustrated at room temperature. In the band diagram, holes are denoted by a circled plus symbol (\oplus), while electrons are indicated by a circled minus symbol (\ominus) for clarity.

c-Si-heterojunction, inducing the s-shaped behavior in the light J-V curves at cryogenic temperatures (Fig. 4 a) (Chavali et al., 2018; Gal et al., 1985; Tanaka and Yamasaki, 1987). Consequently, at low temperatures, the R_s increases, leading to a reduction in the FF due to the temperature-dependent shift in the energy barrier (ΔE_V). This effect causes a pronounced displacement of the maximum power point (MPP) toward lower voltages, characteristic of s-shaped light J-V curves.

Under illumination, electron-hole pairs are also generated in the base of p-type c-Si HJT SCs, and minority carriers (electrons) are driven into the n^+ -region (emitter) under the built-in electric field (Fig. 4 b). In doing so, they overcome a relatively low potential barrier (spike) of approximately 0.15 eV. At low temperatures, this barrier does not significantly impede carrier transport, therefore, no s-shaped behavior is observed in the light J-V curves (Fig. 3 b).

According to the results reported in (Conley et al., 1966; Sze and Ng, 2006; Burgelman et al., 2005), the disappearance of the s-shaped behavior in the light J-V curves near V_{OC} is attributed to a reduction in the potential barrier due to increased doping levels in the base or emitter layer. As a result, in addition to thermionic emission, carriers can drift through a spike barrier by tunneling (trap-assisted tunneling). With higher doping concentrations, the SCR becomes narrower, leading to an increase in the tunneling current (Zeman and Zhang, 2012).

Capacitance–voltage (C–V) measurements conducted at 100 kHz and 300 K using a Semetrol LLC instrument revealed that the SCR width in the n-type c-Si-based HJT SCs was $\sim 0.422 \mu\text{m}$. At reduced temperatures, this configuration suppresses hole tunneling between the n-base and p⁺-emitter regions. Therefore, the observed s-shape behavior in the light J-V curves at lower temperatures is attributed to a parasitic potential barrier caused by the ΔE_V .

Fig. 5 presents the temperature dependence of the J_{SC} of HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under AM0 spectrum (136.7 mW/cm²). The experimental results demonstrate that the J_{SC} increases linearly with increasing temperature for both types of HJT SCs. It is well known that, with increasing temperature, the bandgap of c-Si narrows (Bludau et al., 1974), which causes a shift in the absorption coefficient toward the longer wavelength region. As a result, the substrate absorbs a broader spectrum of infrared radiation, thereby enhancing electron-hole pair generation in the photoactive region (Haschke et al., 2017; Ataboev et al., 2019; Shockley and Queisser, 1961).

As illustrated in Fig. 5, the J_{SC} of the HJT SCs based on p-type c-Si substrates (curve 2) is higher than that of cells based on n-type substrates (curve 1). This difference is attributed primarily to the variation in substrate thickness: the p-type wafer has a thickness of $\sim 135 \mu\text{m}$, which is approximately 10 μm greater than that of the n-type wafer ($\sim 125 \mu\text{m}$). It is well established that longer-wavelength photons (particularly those in the near-infrared region) are more effectively absorbed in thicker substrates, whereas in thinner substrates they are

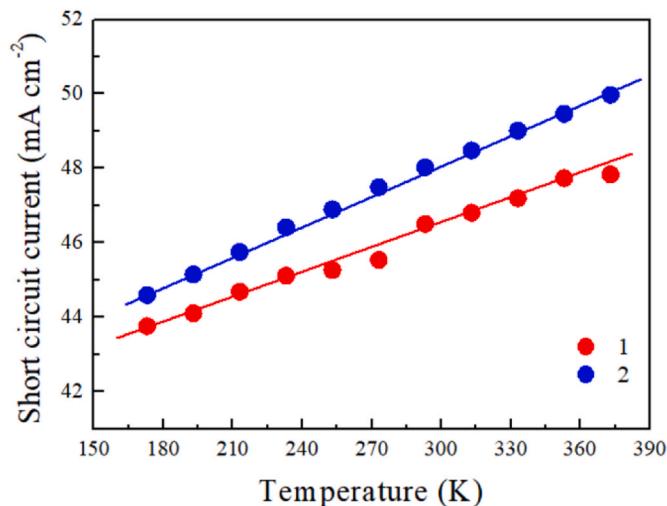


Fig. 5. Temperature dependence of short-circuit current density of HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under AM0 spectrum (136.7 mW/cm²).

more likely to pass through without generating electron-hole pairs. Consequently, the increased optical path length in the thicker substrate enhances photon absorption, leading to higher photocurrent generation (Tiedje et al., 1984).

Based on the experimental results, the temperature coefficient of the short-circuit current density (TCJ_{sc}) was extracted from the slope of the linear region of the J_{SC} versus temperature characteristics for HJT SCs based on n-type and p-type c-Si substrates. The calculated TCJ_{sc} values are 0.054 %/K and 0.058 %/K for n-type and p-type c-Si substrates, respectively. These values are in good agreement with the previously reported data in (Haschke et al., 2017; Le et al., 2023).

Fig. 6a and 6b present experimental results of the temperature dependence of the open-circuit voltage - $V_{OC}(T)$ for HJT SCs based on n-type and p-type c-Si substrates under AM0 spectrum (136.7 mW/cm²). As seen in Fig. 6 a and 6 b, the experimental $V_{OC}(T)$, demonstrates more complex behavior for HJT SCs based on n-type c-Si (Fig. 6 a, blue circles), whereas for p-type c-Si-based HJT SCs, $V_{OC}(T)$ exhibits an approximately linear dependence (Fig. 6 b).

As shown in Fig. 6a, the V_{OC} decreases linearly from 0.693 V to 0.547 V as the temperature increases from 293 K to 373 K. When the solar cell is cooled from 293 K to 173 K, the V_{OC} initially rises linearly, reaching 0.795 V at 233 K, after which the increase slows down and approaches saturation. Within this temperature range (173–233 K), V_{OC} rises by merely 20 mV (from 0.795 V to 0.815 V). At relatively high temperatures ($T > 233$ K), the shape of the V_{OC} curve is consistent with the classical

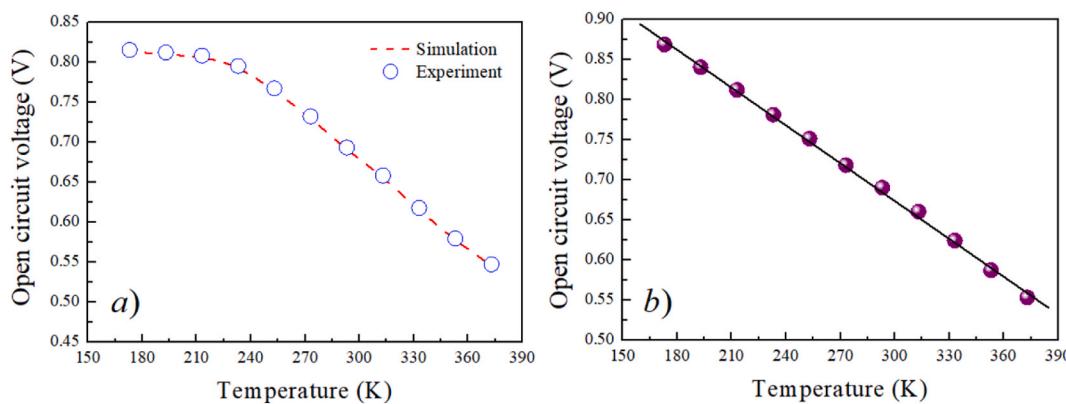


Fig. 6. Temperature dependence of open-circuit voltage of HJT SCs based on n-type (a) and p-type (b) c-Si substrates under AM0 spectrum (136.7 mW/cm^2). Red dashed line – simulation results; blue circles – experiment results. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

theoretical model described in (Le et al., 2023).

For HJT SCs fabricated on p-type c-Si substrates, the V_{OC} increases linearly from 0.553 V to 0.8684 V as the temperature decreases from 373 K to 173 K (Fig. 6 b). Within the investigated temperature range, no V_{OC} saturation is observed for these HJT SCs. This behavior is likely associated with the intrinsic band structure and charge carrier transport mechanisms within the heterojunction (Bivour et al., 2014). The observed decrease in V_{OC} with rising temperature from 173 K to 373 K is primarily attributed to the temperature-induced narrowing of the Si bandgap (Bludau et al., 1974), the exponential increase in the reverse saturation current, and the rise in the intrinsic carrier concentration (n_i) (Löper et al., 2012), as described by Equation (5).

The observed nonlinear saturation behavior in the experimental $V_{OC}(T)$ at low temperatures was analyzed using the theoretical framework presented in the previous section.

Fig. 6a shows the experimental (blue circles) and theoretical (red dashed line) $V_{OC}(T)$, which demonstrates good agreement between the measured data and the simulation results. The model parameters – including J_{SC} , surface $S(T)$ and bulk $\tau(T)$ recombination velocity, and donor concentration $N_d(T)$ in Equation (8) were all extracted from experimental measurements. In modeling the $V_{OC}(T)$ (Fig. 6a, red dashed line), the temperature dependence of the Si bandgap was taken according to the method described in (Bludau et al., 1974). The J_{SC} values at various temperatures were obtained experimentally under AM0 (136.7 mW/cm^2). Donor concentration, charge carrier mobility, and substrate resistivity were measured using the Hall effect method with the Ecopia HMS Hall effect measurement system in the temperature range of 173–373 K.

The total recombination velocity, including both surface ($S = S_0 + S_d$) and bulk $\tau(T)$ components, was estimated at different temperatures using the method proposed in (Panaiotti and Terukov, 2019; Panaiotti et al., 2020). In calculating the theoretical $V_{OC}(T)$ (Fig. 6a, red dashed line), the temperature-induced variations in both bulk $\tau(T)$ and surface $S(T)$ recombination velocities were taken into account during the heating of the HJT SC samples. In the theoretical modeling of the $V_{OC}(T)$ using Equation (8), the carrier lifetime (τ) was employed as a key fitting parameter.

Within the investigated temperature range, the parameters J_{SC} , N_d and S exhibit a monotonic increase with rising temperature. Notably, the total surface recombination velocity $S(T)$ in n-type HJT SCs increased from 7.7 cm/s at 173 K to 18.7 cm/s at 373 K, which is in good agreement with the data reported in (Bernardini and Bertoni, 2019).

During the modeling of the theoretical $V_{OC}(T)$, the carrier lifetime (τ) was found to increase with temperature in the range of 173 K–373 K, which is in good agreement with previously reported data (Seif et al., 2015; Bernardini and Bertoni, 2019). Furthermore, the modeled τ value demonstrates good agreement with experimental measurements

obtained by photoconductance decay method (PCD) at room temperature. The experimentally determined τ was $\sim 271 \mu\text{s}$, while the calculated value of τ at the same temperature was $267 \mu\text{s}$ (Utamuradova et al., 2025a,b).

The temperature coefficients of the open-circuit voltage (TCV_{OC}) for HJT SCs based on n-type and p-type c-Si substrates were determined from the slopes of the linear regions of the experimental $V_{OC}(T)$ dependencies. For the n-type c-Si HJT SCs, TCV_{OC} was $-0.23 \%/\text{K}$ in the 233–373 K temperature range, and $-0.024 \%/\text{K}$ in the 173–233 K range. In contrast, the p-type c-Si HJT SCs exhibited a TCV_{OC} of $-0.182 \%/\text{K}$ across the entire 173–373 K temperature range. Notably, the obtained values are significantly lower than those reported for other c-Si SC technologies (Le et al., 2021; Haschke et al., 2017).

Fig. 7 presents experimental results showing the temperature dependence of the FF (a) and R_s (b) for HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under the AM0 spectrum (136.7 mW/cm^2). It is well known that the FF is one of the key performance indicators of SCs, reflecting the quality and ideality of the p–n-junction. It is defined by the following expression (Sze and Ng, 2006):

$$\text{FF} = \frac{J_m V_m}{J_{sc} V_{oc}}, \quad (10)$$

where, J_m and V_m – current density and voltage at maximum power point.

As shown in Fig. 7 a (curve 1), the FF of the HJT SCs based on n-type c-Si increases linearly from 65 % to approximately 75 % as the temperature rises from 173 K to 273 K. However, beyond 273 K, the FF decreases linearly, reaching 65.53 % at 373 K. The initial increase in FF with rising temperature is attributed to the decrease in the parasitic potential barrier caused by the ΔE_V (Fig. 4 a) and R_s of the SCs (Fig. 7 b, curve 1).

The decrease in R_s is particularly pronounced in the low-temperature region, where its value decreases from $\sim 13.8 \Omega \text{ cm}^2$ at 173 K to $\sim 2.5 \Omega \text{ cm}^2$ at 273 K with rising temperature (Fig. 7 b, curve 1). Within this temperature interval, R_s decreases at a relatively high rate of $-0.817 \%/\text{K}$, indicating enhanced carrier transport due to reduced resistive losses. This value is in good agreement with the data reported in (Le et al., 2021). In the higher-temperature range of 273–373 K, R_s exhibits a slight decrease ($-0.41 \%/\text{K}$) from $\sim 2.5 \Omega \text{ cm}^2$ at 273 K to $\sim 1.3 \Omega \text{ cm}^2$ at 373 K. The shunt resistance (R_{sh}) exhibits only minor variations in the temperature range of 173–273 K. In the studied temperature range, R_s of p-type c-Si HJT SCs decreases slightly from $\sim 4.9 \Omega \text{ cm}^2$ to $\sim 2 \Omega \text{ cm}^2$.

In HJT SCs, the R_s is determined from the slope of the J-V curve at the open-circuit voltage point, while the R_{sh} is derived from the slope at the short-circuit current point (Singh and Ravindra, 2011).

The R_s of an SC comprises multiple resistive components connected

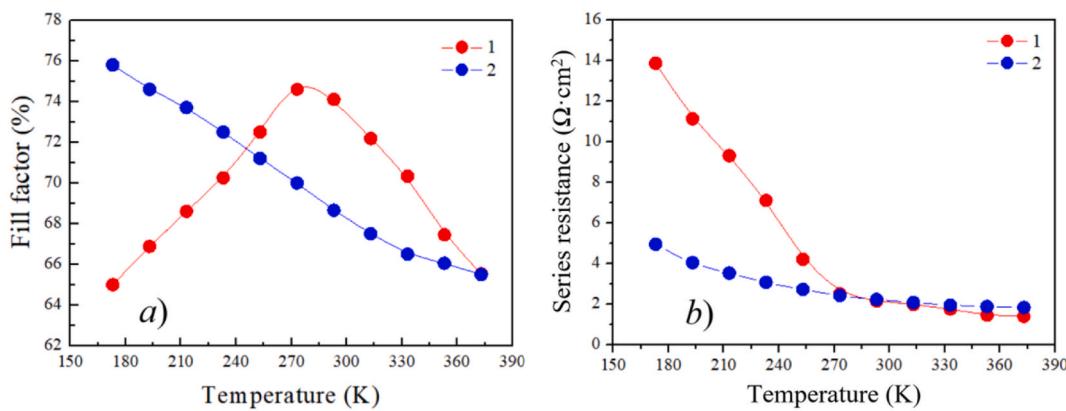


Fig. 7. Temperature dependence of the fill factor (a) and series resistance (b) of HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under AM0 spectrum (136.7 mW/cm^2).

in series with the p – n-junction, including the bulk resistances of the p-type and n-type semiconductor regions, the metal-semiconductor contact resistances, and other related contributions. Conversely, the R_{sh} characterizes current leakage mechanisms, including surface recombination currents, bulk defect-assisted tunneling, and peripheral leakage at device edges (Ataboev et al., 2019; Fahrenbruch and Bube, 1983).

The decline in FF of n-type c-Si HJT SCs at higher temperatures is most likely attributed to a decrease in R_{sh} , which is connected in parallel with the p – n-junction and consists of parasitic leakage paths that lead to increased current losses and reduce the maximum output power of the PV device. Furthermore, as described by Eq. (10), FF is influenced by the V_{OC} , which exhibits a linear decrease with rising temperature.

The observed reduction in the FF of p-type c-Si HJT SCs with increasing temperature (Fig. 7a, curve 2) is primarily attributed to the competing effects of decreasing V_{OC} and R_{sh} . Although the decrease in R_{s} would generally lead to an improvement in FF, its beneficial effect is outweighed by the more pronounced degradation in V_{OC} , resulting in an overall decline in FF (Büyükbaba-Uluşan et al., 2025).

The temperature coefficient of the fill factor (TCFF), determined from the slope of the linear decline in FF, was found to be -0.14 \% /K for n-type c-Si HJT SCs in the temperature range of $273\text{--}373 \text{ K}$, and -0.077 \% /K for p-type c-Si HJT SCs over the investigated temperature range.

Fig. 8 shows the temperature dependence of the maximum output power $P_{\text{max}}(T)$ (a) and conversion efficiency $\eta(T)$ (b) of the HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under the AM0 spectrum (136.7 mW/cm^2). P_{max} is determined by the product of J_{sc} , V_{oc} and FF.

As shown in Fig. 8 a (curve 1), the P_{max} of n-type c-Si HJT SCs decreases linearly from $\sim 25 \text{ mW/cm}^2$ to $\sim 17.2 \text{ mW/cm}^2$ with increasing temperature from 273 K to 373 K . Upon cooling the SCs from 273 K to 173 K , P_{max} initially exhibits a slight increase, reaching a peak of $\sim 25.2 \text{ mW/cm}^2$ at 233 K , followed by a linear decline to $\sim 23.2 \text{ mW/cm}^2$. This behavior of P_{max} is primarily associated with the temperature dependencies of key PV parameters such as V_{OC} , FF, R_{sh} and R_{s} , which collectively have the most significant impact on the $P_{\text{max}}(T)$ characteristics (Green, 2003). In the temperature range of $173\text{--}273 \text{ K}$, J_{sc} exhibits only a slight decrease, while V_{oc} increases marginally by 20 mV with decreasing temperature. However, the simultaneous increase in R_{s} results in elevated resistive losses, ultimately leading to a net decrease in the P_{max} . For temperatures above 273 K , the linear degradation in P_{max} is primarily driven by significant reductions in both V_{oc} and FF, which are adversely affected by thermal-induced carrier recombination and resistive effects.

In the studied temperature range, P_{max} of p-type c-Si HJT SCs exhibits a linear decrease, declining from $\sim 29.4 \text{ mW/cm}^2$ at 173 K to $\sim 18.1 \text{ mW/cm}^2$ at 373 K . As previously noted, this reduction in P_{max} with increasing temperature is directly linked to the temperature dependence variations of key PV parameters, such as, V_{oc} , FF, R_{sh} and R_{s} .

The temperature coefficients of the $P_{\text{max}}(\text{TCP}_{\text{max}})$ for n-type c-Si HJT SCs were evaluated to be -0.31 \% /K in the $273\text{--}373 \text{ K}$ range and -0.15 \% /K in the $173\text{--}233 \text{ K}$ range, while the corresponding coefficient for p-type c-Si HJT SCs was -0.2 \% /K over the $173\text{--}373 \text{ K}$ interval. These results demonstrate that the investigated p-type c-Si HJT SCs exhibit the lowest TCP_{max} among various silicon-based PV technologies (Le et al., 2021; Haschke et al., 2017). The relatively low TCP_{max} of HJT SCs,

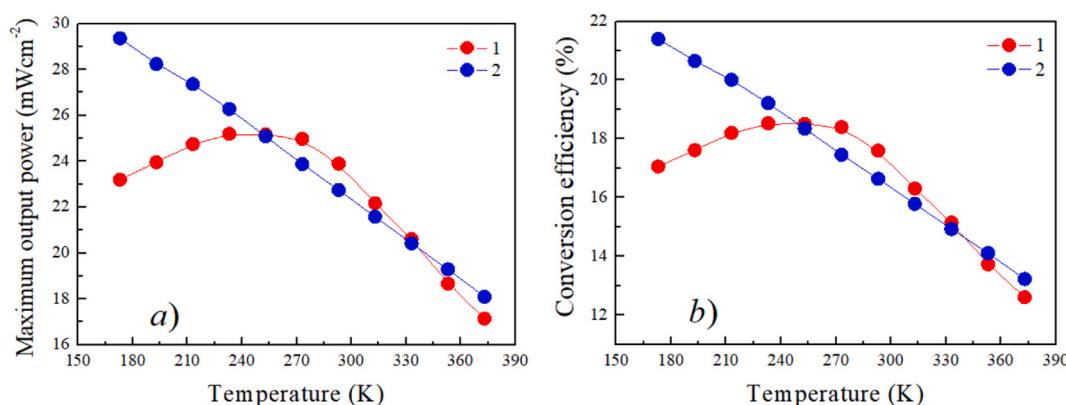


Fig. 8. Temperature dependence of the maximum output power (a) and conversion efficiency (b) of HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under AM0 spectrum (136.7 mW/cm^2).

compared to other silicon-based PV technologies, can be attributed to the presence of i-a-Si:H passivation layers on both surfaces of the c-Si substrate. This configuration results in a reduced T_{OC} , which accounts for over 60 % of the overall $T_{CP_{max}}$ variation due to its dominant influence compared to other PV parameters such as J_{sc} and FF (Le et al., 2021).

Thus, the experimental results clearly indicate that, at low temperatures, the P_{max} of n-type c-Si HJT SCs decreases, whereas p-type c-Si HJT SCs exhibit a more stable linear increase, highlighting a distinct temperature-dependent behavior between the two cell types.

The following analytical expressions have been derived for the key PV parameters by applying linear fits to the experimental data presented above. These expressions are valid for the temperature range of 273–373 K for n-type HJT SCs and 173–373 K for p-type HJT SCs:

$$\underbrace{\frac{1}{P_{max}^{25^\circ C}} \frac{dP_{max}}{dT}}_{TCP_{max}} = \underbrace{\frac{1}{V_{OC}^{25^\circ C}} \frac{dV_{OC}}{dT}}_{TCV_{OC}} + \underbrace{\frac{1}{J_{sc}^{25^\circ C}} \frac{dJ_{sc}}{dT}}_{TCJ_{sc}} + \underbrace{\frac{1}{FF^{25^\circ C}} \frac{dFF}{dT}}_{TCFF}, \quad (11)$$

where, $P_{max}^{25^\circ C}$, $V_{OC}^{25^\circ C}$, $J_{sc}^{25^\circ C}$ and $FF^{25^\circ C}$ – the maximum output power, open-circuit voltage, short-circuit current density and fill factor at $25^\circ C$ (298 K). Substituting the temperature coefficients of V_{oc} , J_{sc} and FF into Equation (11) yields a $T_{CP_{max}}$ of $-0.316\text{ \%}/\text{K}$ for n-type HJT SCs, and $-0.202\text{ \%}/\text{K}$ for p-type HJT SCs. Consequently, the value of $T_{CP_{max}}$ calculated from Eq. (11) was $1.5 \div 2\%$ higher than the value extracted from the experimental $P_{max}(T)$ curve (Fig. 8a).

Fig. 8 b shows the experimental results for the temperature dependence of the conversion efficiency $\eta(T)$ of the HJT SCs based on n-type (curve 1) and p-type (curve 2) c-Si substrates under AM0 (136.7 mW/cm²). η of the HJT SCs is defined as the ratio of the P_{max} to the incident light power (P_{rad}), which is expressed by the following equation (Sze and Ng, 2006):

$$\eta = \frac{P_{max}}{P_{rad}} \cdot 100\% = \frac{J_{sc} V_{oc} FF}{P_{rad}} \cdot 100\%, \quad (12)$$

where, $P_{rad} = 136.7\text{ mW/cm}^2$.

As shown in Fig. 8 b, the η of the HJT SCs based on n-type and p-type c-Si substrates exhibits a temperature dependence similar to that of the P_{max} . The η of n-type c-Si HJT SCs reaches its maximum value of $\sim 18.53\%$ at 233 K. Beyond this point, with increasing temperature, η decreases. In contrast, the η of p-type c-Si HJT SCs decreases linearly from $\sim 21.4\%$ at 173 K to $\sim 13.23\%$ at 373 K. According to (Dubey et al., 2013), the η of HJT SCs can be calculated using the following expression, which is valid in the temperature range of 233–373 K for n-type c-Si HJT SCs and 173–373 K for p-type c-Si HJT SCs,

$$\eta_c = \eta_{ref} [1 - \beta_0 (T_c - T_{ref})], \quad (13)$$

where, T_c and T_{ref} – represent the temperature of the HJT SCs and the reference (room) temperature (298 K), respectively; η_c and η_{ref} – are the conversion efficiencies of the HJT SCs at T_c and T_{ref} . β_0 – is the temperature coefficient of η , which is equal to -0.0031 K^{-1} for n-type c-Si HJT SCs and -0.002 K^{-1} for p-type c-Si HJT SCs. As the HJT SC temperature increases, the difference $T_c - T_{ref}$ grows, resulting in a linear decrease in η .

5. Conclusion

This study presents a comprehensive investigation of the temperature dependence of the PV performance of HJT SCs fabricated on Gallium- (p-type) and Phosphorus-(n-type) doped c-Si wafers under the AM0 spectrum (136.7 mW/cm²) in the temperature range of 173–373 K.

The main findings of this work can be summarized as follows:

The J_{sc} of both cell types increases linearly with temperature, exhibiting positive temperature coefficients of $0.054\text{ \%}/\text{K}$ for n-type and $0.058\text{ \%}/\text{K}$ for p-type substrates. This behavior is attributed to the

temperature-induced narrowing of the c-Si bandgap and the corresponding shift of the absorption coefficient toward longer wavelengths.

The V_{OC} demonstrates distinct temperature behavior for each cell type. For n-type HJT SCs, V_{OC} shows a complex, non-linear dependence: it increases from 0.547 V at 373 K to 0.693 V at 223 K, beyond which the rate of increase diminishes, saturating near 0.815 V at 173 K. In contrast, the V_{OC} for the p-type SCs decreases linearly from 0.868 V at 173 K to 0.553 V at 373 K. A developed theoretical model successfully explains the $V_{OC}(T)$ behavior for n-type SCs, showing excellent agreement with experimental data.

A notable s-shaped distortion in the light J-V curves near V_{OC} was observed exclusively in n-type HJT SCs at temperatures below 233 K. This phenomenon is attributed to a significant valence band offset (ΔE_V) at the (p⁺) a-Si:H/(n) c-Si-heterointerface, which creates a parasitic potential barrier that impedes hole transport at cryogenic temperatures. This distortion leads to a reduction in both FF and η at low temperatures due to an increase in series resistance.

The temperature coefficient of the maximum output power was determined to be $-0.31\text{ \%}/\text{K}$ for n-type SCs in the temperature range of 273–373 K, and a more favorable $-0.20\text{ \%}/\text{K}$ for p-type SCs across the entire 173–373 K range.

The experimental results conclusively demonstrate that HJT SCs based on p-type (gallium-doped) c-Si substrates exhibit superior and more stable temperature performance compared to their n-type counterparts, particularly in the critical low-temperature regime. The absence of s-shaped J-V curves, coupled with a smaller (less negative) temperature coefficient for P_{max} , makes p-type HJT SCs a highly promising and reliable technology for power generation in space applications, especially for satellites operating in LEO, where they must endure extreme temperature fluctuations between approximately 173 K and 373 K. These cells present a promising candidate for powering small, lightweight, and cost-effective satellites in the coming years.

Future work will focus on investigating the combined effects of temperature and high-energy particle radiation on the performance and degradation of these HJT SCs to fully assess their long-term viability for space missions.

CRediT authorship contribution statement

O.K. Ataboev: Writing – original draft, Resources, Methodology, Investigation, Conceptualization. **ShB. Utamuradova:** Writing – original draft, Conceptualization. **I.E. Panaiotti:** Writing – review & editing, Supervision, Methodology, Formal analysis. **E.I. Terukov:** Writing – review & editing, Resources, Conceptualization. **D.A. Malevskiy:** Supervision, Investigation, Formal analysis. **A.I. Baranov:** Methodology, Investigation, Conceptualization. **A.V. Troshin:** Resources, Methodology, Investigation, Conceptualization.

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Declaration of competing interest

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Data availability

Data will be made available on request.

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