A Novel Simple CBCM Method Free From Charge Injection-Induced Errors

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***Abstract*—In this letter, we propose a charge injection-induced error-free charge-based capacitance measurement method (CIEF CBCM). This novel method uses only one n/pMOS pair to characterize the small interconnect capacitance. It has the simplest test structure among various CBCM methods. More importantly, the CIEF CBCM method is free from the errors induced by charge injection. Besides, only one additional pad is needed for one additional capacitor under the test by this method, and it is the most efficient method for process characterization and monitoring.**

***Index Terms*—Capacitance measurement, charge-based capacitance measurement method (CBCM), charge injection, charge injection-induced error-free (CIEF), interconnect capacitance.**

I. Introduction

CHARGE-BASED capacitance measurement (CBCM) [1] was first proposed in 1996 to characterize on-chip interconnect capacitance with subfemtofarad resolution. It is getting more and more attentions because the intermetal capacitances have become the bottleneck in the design of fast chips. Consequently, correct characterization and modeling for interconnect capacitance become more important [2], [3]. Following the concept of CBCM, the single-pattern driver (SPD) method [4], which is free from mismatch and allows all the coupling capacitance extractions, was proposed. However, errors from charge injection always exist, and limit the resolution of CBCM methods [4]. To decrease the impact of charge injection, an improved CBCM scheme [5] employing pass gates was proposed. The errors resulting from charge injection are suppressed by more complex circuit design but still exist. In this letter, we propose a charge injection-induced error-free CBCM method (CIEF CBCM), which has a very simple structure and also allows the coupling capacitance extractions as SPD. More importantly, CIEF CBCM is completely free from the errors induced by charge injection.

II. Test Structure and Extraction Algorithm

The test structure of CIEF CBCM and its extraction algorithm are shown in Fig. 1. It comprises a n/pMOS pair in a pseudo-inverter configuration and they are driven by nonoverlapping signals. The capacitance under the test is placed between the drain sides and one probe pad, to which we can directly apply a pulse or a fixed bias. The capacitance can be extracted by a two-step measurement. At the first step, we force the probe pad to ground. At this step, not only the capacitor under the test ($C_{\rm DUT}$), but also all the parasitic capacitors at the drain sides ($C_{\rm par}$) are charged and discharged between $V_{\rm dd}$ and ground. We record the charging current through pMOS

$$I_1 = (C_{\rm DUT} + C_{\rm par}) \cdot V_{\rm dd} \cdot f \tag{1}$$

where f is the frequency of the nonoverlapping clock signals.

At the second step, we apply a pulse to the probe pad as shown in Fig. 1. The pulse rises up from ground to $V_{\rm dd}$ before pMOS is turned on. When the drain sides are charged up by pMOS, there will be no charges at the both sides of the capacitor under the test because there is no voltage drop on it. Only the current which charges up the parasitic capacitors is recorded as follows:

$$I_2 = C_{\rm par} \cdot V_{\rm dd} \cdot f. \tag{2}$$

Then we let the pulse on the probe pad fall down to ground before nMOS is turned on to avoid any charges on both sides of the capacitor when the drain sides are discharged to ground. Under such operations, the capacitance under the test can then be extracted by subtracting I_2 from I_1 as follows:

$$C_{\rm DUT} = \frac{(I_1 - I_2)}{V_{\rm dd} \cdot f} \tag{3}$$

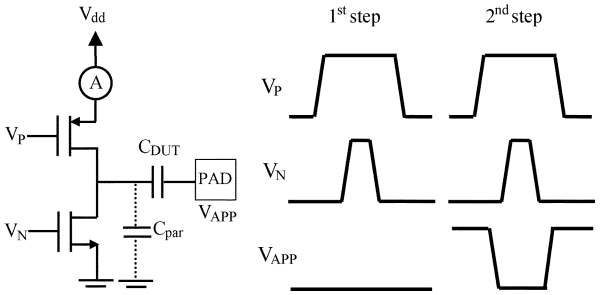

Fig. 1. Proposed CIEF CBCM structure and the two-step extraction algorithm.

III. Free From Errors Induced by Charge Injection

However, in reality, charge injection, which occurs when the MOSFET transistors are turned off, will make the integrated current different from what is expected to be and limit the resolution of conventional CBCM and SPD methods.

To give an insight into the charge injection effect, we performed some SPICE simulations of the conventional CBCM and CIEF CBCM. Taking the phase of pMOS switching off as the example, we simulate the potential at the drain terminal as well as the current flowing back through pMOS in the conventional

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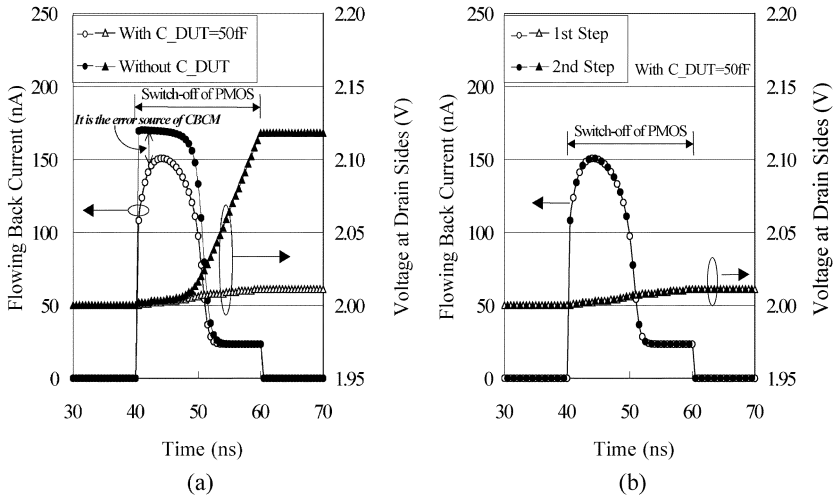

Fig. 2. (a) Simulated potential at the (triangles) drain terminal and the (circles) flowing back current in the conventional CBCM method. The open symbols are for the condition with $C_{\rm DUT} = 50$ fF and the filled symbols are for the condition without $C_{\rm DUT}$. The rampup function from GND to $V_{\rm dd} = 2$ V is from 40–60 ns to turn off the pMOS. (b) Simulated potential at the (triangles) drain terminal and the (circles) flowing back current in CIEF CBCM. The open symbols are for the condition at the first step measurement and the filled symbols are for the condition at the second step measurement.

CBCM method as shown in Fig. 2(a). We turn off pMOS by applying a ramp-up function from 40 ns to 60 ns at the gate electrode. Before the switching-off, the potential at the drain terminal keeps at $V_{\rm dd} = 2$ V. But it follows the ramp-up at the instant of pMOS switch-off due to the voltage coupling through $C_{\rm gd}$ of pMOS. At the same time, there is a current flowing back to $V_{\rm dd}$ and will be recorded by the current meter until pMOS is completely turned off. This unwanted current, which is induced by charge injection, would alter the total integrated current. With or without the capacitor under the test, the charge injection-induced currents are different [6] as shown in the figure. They cannot be completely canceled out when subtraction. It contributes a part of the error in the conventional CBCM method.

Fig. 2(b) shows the simulated voltage overshoots and the flowing-back currents at the first and second steps in CIEF CBCM. There is no difference because the capacitor combination at two steps is the same. The only difference is the potential applied to the probe pad when pMOS switches off. It is ground at the first step and $V_{\rm dd}$ at the second step. It makes no difference on charge injection behavior because they both are dc bias during this phase [6]. As a result, the charge injection-induced currents can be completely cancelled out in CIEF CBCM and do not contribute any error. Similarly, charge injection happens at the phase of nMOS switching-off. It is more apparent that the charge injection-induced currents are cancelled out again in CIEF CBCM because during this phase, not only the capacitor combination but also the bias condition is the same at first and second steps when nMOS is turned off.

Fig. 3 shows the simulated errors due to charge injection of the conventional CBCM method, SPD, and CIEF CBCM. From the figure, we may find that both the conventional CBCM and SPD suffer the similar charge injection-induced errors. The errors increase with the decreasing capacitance under the test and limit the resolution of CBCM methods.

Ideally, CIEF CBCM shows the perfect results and is completely free from the errors induced by charge injection. However, in practice, the limitation of the measurement system would limit the resolution of the method. If we can get current

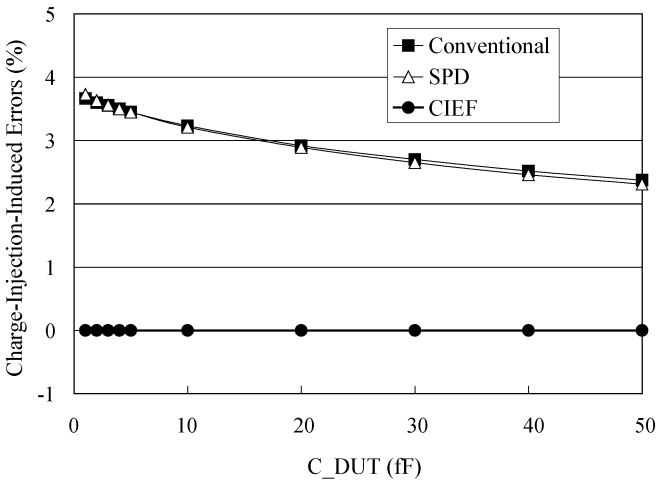

Fig. 3. Simulated charge injection-induced errors versus $C_{\rm DUT}$ for the conventional CBCM, SPD, and CIEF CBCM. The width and length of MOSFETs are 10 and 0.6 μm.

with accuracy as small as a picoampere under the measurement system, attofarad resolution can be achieved when CIEF CBCM is operated under the frequency of the megahertz range.

IV. Least Layout Area-Consuming Test Structure and Results

A test chip was fabricated using an industrial 0.25 μm, triple metal technology. The multifinger Metal 1 structures sandwiched between Metal 2 and Poly plates, as shown in the insert of Fig. 4(a), are used to extract the coupling capacitance between Metal 1 lines. Fig. 4(a) shows the extracted coupling capacitances versus the set number of Metal 1 parallel lines. It shows perfect linearity and can be extrapolated to the origin. Fig. 4(b) shows the extracted coupling capacitances of a set of Metal 1 lines with different overlapped lengths. Similarly, it shows good linearity and is extrapolated to one positive value at y-axis, which should come from the fringe capacitors at edges of the parallel lines.

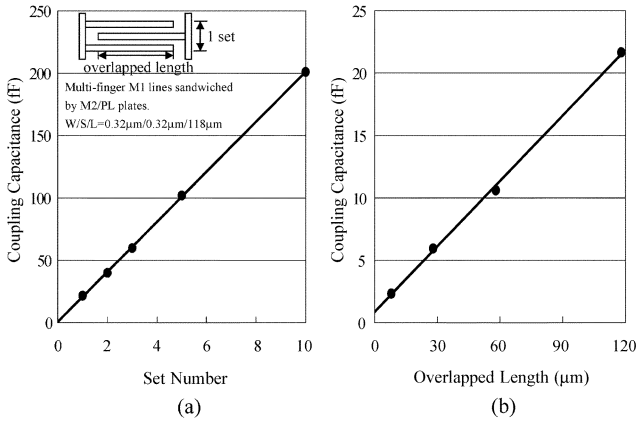

Fig. 4. (a). The measured coupling capacitance versus set number. The insert shows the test structure of multifinger Metal 1 lines sandwiched between Poly and Metal 2 plates. The width/spacing/overlapped length of Metal 1 lines are $0.32/0.32/118$ μm. (b) Measured coupling capacitance versus overlapped length of Metal 1 lines.

In the test chip, by CIEF CBCM, the pseudo-inverter can be shared and only one probe pad is needed for each additional capacitor characterization. By CIEF CBCM, we can extract 20 different interconnect capacitors in one 24-pad spine. Compared to the conventional CBCM and SPD, both methods need additional two probe pads for each additional capacitor characterization. CIEF CBCM occupies the least layout area and is the most efficient method for process characterization and monitoring.

V. Conclusion

In this letter, we propose one novel CBCM method, which is free from the errors induced by charge injection. By the proposed method, charge injection-induced errors are not the limitation of CBCM methods any more. Besides, it has the simplest test structure because it uses only one n/pMOS pair to characterize the small interconnect capacitor. With the common n/pMOS pair, only one additional pad is needed for one additional capacitor under the test. It is the most efficient method for process characterization and monitoring because the least layout area is consumed.

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