Vacuum 84 (2010) 363–368

Contents lists available at ScienceDirect

Vacuum

journal homepage: www.elsevier.com/locate/vacuum

Analysis of surface states and series resistance in Au/n-Si Schottky diodes with insulator layer using current–voltage and admittance–voltage characteristics

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ARTICLE INFO

Article history:
Received 27 April 2009
Received in revised form
6 July 2009
Accepted 6 July 2009

Keywords:
MS diodes
Insulator layer
Surface states
Relaxation time
Frequency dependence

ABSTRACT

In order to good interpret the experimentally observed Au/n-Si (metal–semiconductor) Schottky diodes with thin insulator layer (18 Å) parameters such as the zero-bias barrier height (Φ_{bo}), ideality factor (n), series resistance (R_s) and surface states have been investigated using current–voltage (I–V), capacitance–frequency (C–f) and conductance–frequency (G–f) techniques. The forward and reverse bias I–V characteristics of Au/n-Si (MS) Schottky diode were measured at room temperature. In addition, C–f and G–f characteristics were measured in the frequency range of 1 kHz–1 MHz. The higher values of C and G at low frequencies were attributed to the insulator layer and surface states. Under intermediate forward bias, the semi-logarithmic Ln (I)–V plot shows a good linear region. From this region, the slope and the intercept of this plot on the current axis allow to determine the ideality factor (n), the zero-barrier height (Φ_{bo}) and the saturation current (I_S) evaluated to 2.878, 0.652 and 3.61×10^{-7} A, respectively. The diode shows non-ideal I–V behavior with ideality factor greater than unity. This behavior can be attributed to the interfacial insulator layer, the surface states, series resistance and the formation barrier inhomogeneity at metal–semiconductor interface. From the C–f and G–f characteristics, the energy distribution of surface states (N_{ss}) and their relaxation time (τ) have been determined in the energy range of $(E_c - 0.493E_v)$–$(E_c - 0.610)$ eV taking into account the forward bias I–V data. The values of N_{ss} and τ change from 9.35×10^{13} eV^{-1} cm^{-2} to 2.73×10^{13} eV^{-1} cm^{-2} and 1.75×10^{-5} s to 4.50×10^{-4} s, respectively.

1. Introduction

The metal–semiconductor (MS) Schottky diodes with thin insulator layer have an important role in a great variety of fields of modern electronics. The existence of an insulator layer such as SiO_2, SnO_2 and Si_3N_4 transform the MS Schottky diode into a MIS or MOS structure and in capacitance–voltage characteristics, the slope and the intercept voltage will deviate from those expected for an ideal Schottky diode [1,2]. The thickness of insulating layer must be precisely controlled during the fabrication process and it must be homogeneous. When a voltage is applied across the MS or MIS structure the combination of the interfacial insulator layer, depletion layer and series resistance of the device will share this applied voltage. Localized surface states at semiconductor/insulator interface can be divided into two groups and are dependent on the thickness of the interfacial insulator layer. One of these groups communicates most readily with the metal, the other group with the semiconductor [1–3].

The communication of surface states with the metal decreases with increasing insulator layer thickness. Surface states originate from defects such as dangling bounds at the insulator/substrate interface with energy states in the Si forbidden band gap and are dependent on the chemical composition of the interface [2–5]. This is observed that the capacitance decreases with increasing frequency. This effect is obtained at low and intermediate frequencies. Since in these frequencies, the surface states can follow the ac signal and yield an excess capacitance, which depends on the relaxation time of the surface states and the frequency of the ac signal.

Especially the surface states, insulator layer thickness and series resistance of device play an important role on the electrical characteristics. Therefore, ignoring the insulator layer thickness, density of surface states and series resistance of the sample can lead to significant errors in the devices characteristics [4–9]. There are a few methods [1,4,5,10,11], which could help to determine the density of surface states. Among them the more common one is the conductance method, developed by Nicollian and Goetzberger [4] and current–voltage (I–V) method in the forward bias [1]. In the

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0042-207X/$ – see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.vacuum.2009.07.003

conductance method, the forward and reverse bias *C–V–f* and *G/ω–V–f* measurements give the important information about the distribution of surface states. In recent years, some investigations [12–14] have been reported an anomalous peak in the forward bias (*C–V*) characteristics. Among these very interesting work is presented by Chattopadhyay and Raychaudhuri [12], and they have been shown that the presence of an insulator layer at metal–semiconductor interface and series resistance, the forward bias *C–V* characteristics should exhibit a peak. The peak value of the *C* and its position especially depend on localized density of states at semiconductor/insulator interface, doping concentration, series resistance of device, and the thickness of the interfacial insulating layer [12,14]. The series resistance of device can be obtained from various methods [5,15,16] by admittance–voltage and current–voltage characteristics.

The purpose of this paper is determination of the energy distribution of the surface states (N_{ss}) and their relaxation time (τ) in Au/n-Si (MS) Schottky diode. The energy distribution of N_{ss} and τ is obtained from measured forward bias *I–V* and *C–V* and *G/ω–V* characteristics. In addition, the high frequency *C–V* and *G/ω–V* values were corrected for the effect of series resistance (R_s) to obtain the real MS capacitance and conductance.

2. Experimental procedure

The metal–semiconductor (Au/n-Si) Schottky diodes were fabricated on n-type (P-doped) single crystals silicon wafer with <111> surface orientation, 280 μm thick, 2″ diameter and 4.45 Ω cm resistivity. The Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol and then etched in: first H_2SO_4, H_2O_2 and 20% HF solution, then $6HNO_3$:1HF:$35H_2O$ and 20% HF solution. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of 18 MΩ cm resistivity. After surface cleaning processes, high purity (99.999%) gold (Au) metal with a thickness of 2500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer in liquid nitrogen trapped oil-free ultra-high vacuum system in the pressure of 1×10^{-6} Torr. The ohmic contact was performed by sintering the evaporated Au back contact at 450 °C for 30 min in flowing dry nitrogen ambient at rate of 1 lt/min. This process served to sinter the Au on the upper surface of the Si wafer. After this process, circular dots of 2 mm in diameter and 2500 Å thick Au rectifying contacts were deposited onto surface of the wafer through a metal shadow mask in liquid nitrogen trapped in the same vacuum system and pressure. The thickness of the metal layer was monitored with quartz crystal thickness monitor. The interfacial insulator layer thickness was estimated to be about 18 Å from measurement of the insulator capacitance in the strong accumulation region. The capacitance–voltage (*C–V*) and conductance–voltage (*G/ω–V*) are carried out in the frequency range of 1 kHz–1 MHz by using an HP 4192A LF impedance analyzer (5 Hz–13 MHz). During the measurements the small ac signal of 50 mV peak to peak from the external pulse generator is applied to the sample to meet the requirement [5]. In addition, the forward and reverse bias current–voltage (*I–V*) characteristics of structures were measured at room temperature using a Keithley 220 current-source and a Keithley 614 electrometer. All measurements were controlled with the help of a microcomputer.

3. Results and discussion

3.1. Current–voltage (I–V) characteristics

When a metal–semiconductor Schottky diodes with a thin interfacial insulator layer and series resistance are considered, it is assumed that the current (*I*) across a Schottky diode ($V \geq 3$ kT/q) can be described by [2]

$$I = I_s\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

where I_s is the reverse saturation current and defined by

$$I_s = AA^*T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \quad (2)$$

and the quantities Φ_{Bo}, R_s, *n*, *T*, *A*, A^* and *k* are the zero-bias barrier height, series resistance, ideality factor, temperature in K, area of rectifier contact, effective Richardson constant equal to 112 A cm^{-2} K^{-2} for n-type Si and Boltzmann constant, respectively [2].

The experimental forward and reverse bias *I–V* characteristics of the selected one Au/n-Si Schottky diode with thin insulator layer at room temperature is shown in Fig. 1. As can be seen from Fig. 1, the *I–V* characteristics show a good rectifier behavior and rectification ratio has a factor of 342 achieved between the reverse and forward bias current at ±4 V. Moreover, the soft or slightly non-saturating behavior observed as a function of bias in the experimental reverse bias branch can be commonly explained in terms of the spatial inhomogeneity of Schottky barrier height [17–19] and the image force lowering of SBH [20]. In addition, while the forward bias *I–V* characteristics are linear on a semi-logarithmic scale at low forward bias voltages, but deviate considerably from linearity due to the effect of series resistance R_s and surface states when the applied voltage is sufficiently large [21].

The experimental values of I_s, Φ_{Bo} and *n* were derived from intercept and slope of the linear region of the forward bias Ln (*I*) vs *V* plot as 3.61×10^{-7} A, 0.652 eV and 2.878, respectively. The ideality factor refers to linear part of Ln (*I*) vs *V* characteristics where the value of R_s can be assumed equal zero. This value of the ideality factor shows that the device obeys a MS configuration. Therefore, the high values of *n* can be attributed to effects of the bias voltage drop across the interfacial insulator layer and,

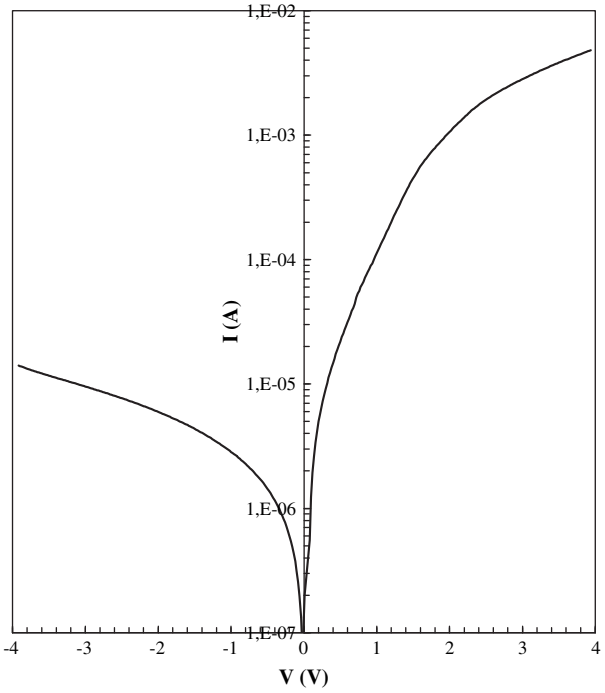

Fig. 1. The forward and reverse bias *I–V* characteristics of the selected one Au/n-Si Schottky diode at the room temperature.

Table 1
The energy distribution of the surface states N_{ss} obtained from experimental data of the forward bias (I–V) characteristics for Au/n-Si Schottky diode.

V (V)	n_V (V)	Φ_e (eV)	$E_c - E_{ss}$ (eV)	N_{ss} (eV^{-1} cm^{-2})
0.08	2.350	0.655	0.576	$3.07E+13$
0.12	2.634	0.684	0.565	$3.72E+13$
0.16	2.663	0.709	0.550	$3.79E+13$
0.20	2.852	0.739	0.540	$4.22E+13$
0.24	3.134	0.773	0.534	$4.86E+13$
0.28	3.378	0.807	0.527	$5.41E+13$
0.32	3.617	0.841	0.522	$5.96E+13$
0.36	3.852	0.876	0.517	$6.49E+13$
0.40	4.078	0.911	0.512	$7.01E+13$
0.44	4.300	0.947	0.508	$7.51E+13$
0.48	4.511	0.983	0.504	$8.00E+13$
0.52	4.704	1.018	0.500	$8.43E+13$
0.56	4.918	1.055	0.496	$8.92E+13$
0.60	5.104	1.091	0.493	$9.35E+13$

therefore, of the bias voltage dependence of the barrier height [2,13,17,22,23]. Also voltage dependent ideality factor n_V can be written from Eq. (1) as

$$n_v(V) = \frac{qV}{kT\ \ln(I/I_o)} \tag{3}$$

The effective barrier height Φ_e can be given by taking into considering the applied bias voltage and series resistance effect.

$$\phi_e = \phi_{bo} + \beta(V - IR_s) = \phi_{bo} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{4}$$

where β is the voltage coefficient of the effective barrier height Φ_e. The expression for the surface state densities as deduced by Card and Rhoderick [1] is reduced to

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1)) - \frac{\varepsilon_s}{W_D}\right] \tag{5}$$

where ε_s and ε_o are the permitivities of the insulator layer and the semiconductor, respectively, δ the thickness of insulator layer and W_D is the width of the space-charge region. The interfacial insulator layer thickness δ was obtained from high frequency (1 MHz) C–V characteristics using the equation for insulator layer capacitance ($C_{ox} = \varepsilon_i A/\delta$). Thus, in n-type semiconductors, the energy of the surface states E_{ss} with respect to the bottom of the conductance band at the surface of semiconductor is given by

$$E_c - E_{ss} = q(\Phi_B - V) \tag{6}$$

Thus, the energy distribution profile of surface states were obtained by substituting the voltage dependent n_V values, $\varepsilon_i = 3.9\varepsilon_o$, $\delta = 18$ Å and $W_D = 4.5 \times 10^{-4}$ cm in Eq. (5) and is given in Table 1 and Fig. 2, respectively.

As can be seen from Table 1 and Fig. 2, the increase in the surface state density from midgap towards the bottom of conductance band is very apparent. The magnitude of N_{ss} at $E_c - 0.493$ and $E_c - 0.576$ (eV) have changed in the range from 9.35×10^{13} to 3.07×10^{13} eV^{-1} cm^{-2}

The average value of the surface states is of the order of 2×10^{14} eV^{-1} cm^{-2}. Similar results have been reported in the literature [24–28] and Hanselaer et al. [29] shows that the surface states of Schottky diode with the presence of an interfacial insulator layer is lower than that of Schottky barriers without an interfacial insulator layer.

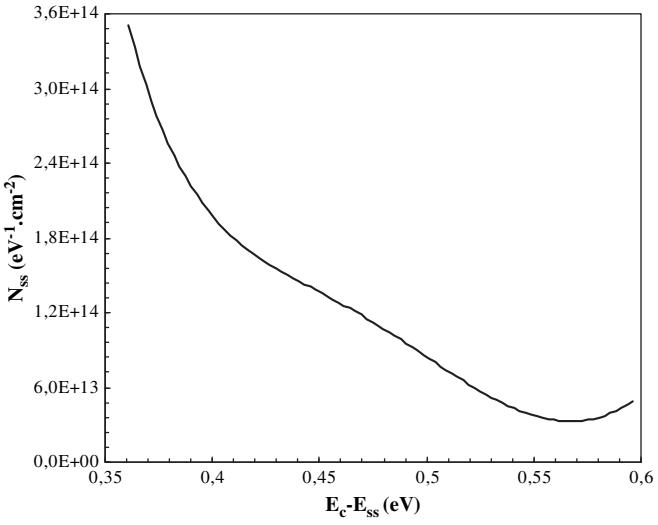

Fig. 2. The energy distribution profile of surface states obtained from the forward bias I–V characteristics of Au/n-Si Schottky diode.

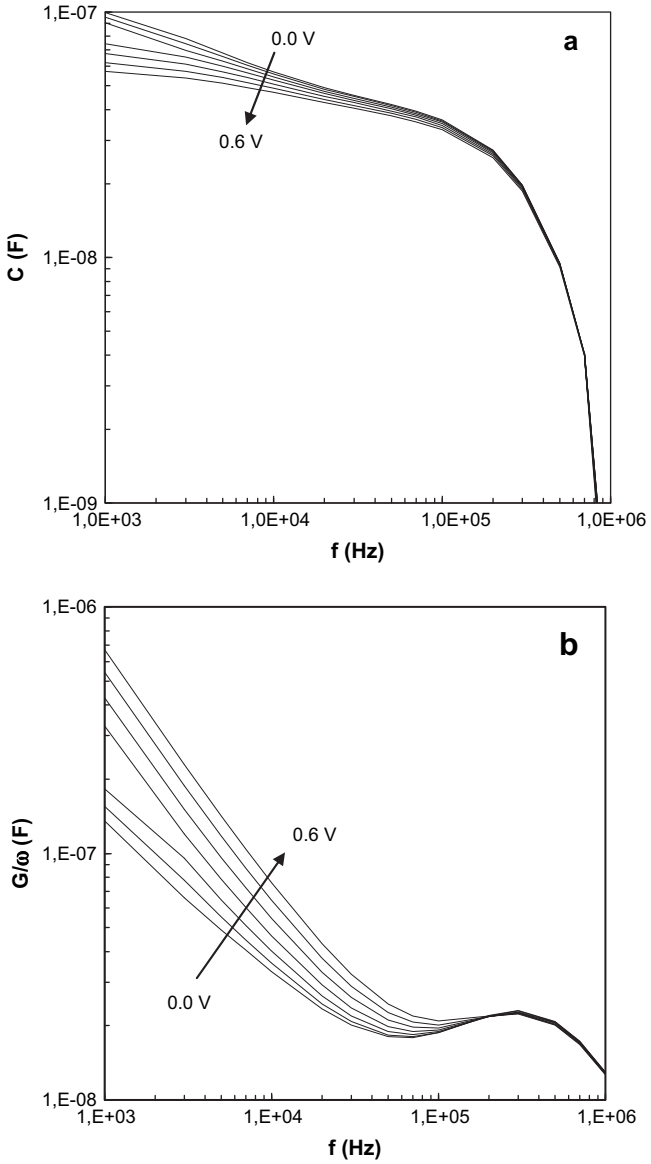

Fig. 3. (a) Capacitance–frequency and (b) conductance–frequency characteristic with bias as a parameter for Au/n-Si Schottky diode.

3.2. Capacitance–frequency (C–f) and conductance–frequency (G/ω–f) characteristics

According to Nicollian and Goetzberg [4,5] and Werner et al. [30] the surface state capacitance (C_{ss}) and conductance (G_{ss}) for a MS and MIS structures can be described as

$$C_{ss} = \frac{AqN_{ss}}{\omega\tau}\arctan(\omega\tau) \tag{7}$$

$$G_{ss} = \frac{AqN_{ss}}{2\tau}\,\mathrm{Ln}\left(1+\omega^2\tau^2\right) \tag{8}$$

where τ is time constant of the N_{ss} and can be written as

$$\tau = \frac{1}{\nu_{th}\sigma_s N_D}\exp\left(\frac{qV_d}{kT}\right) \tag{9}$$

where A is the contact area, σ_s is the cross-section surface states, ν_{th} is the thermal velocity of carriers and N_D the doping concentration. The conductance of surface G_{ss} is given by [4,5,30]

$$G_{ss} = \frac{qI_{dc}}{AkT}\frac{\omega^2 C_i(C-C_{HF})}{G^2+\omega^2(C-C_{HF})^2} \tag{10}$$

The value of interfacial insulator layer capacitance (C_{ox}) is obtained from high frequency (1 MHz) C–V cures as

$$C_{ox} = C_{ma}\left[1+\left(\frac{G_{ma}}{\omega C_{ma}}\right)^2\right] = \frac{\varepsilon_i\varepsilon_0 A}{d_{ox}} \tag{11}$$

where $\varepsilon_i = 3.9\epsilon_o$ [2] and ε_o ($=8.85\times10^{-14}$ F/cm) are the permitivities of the interfacial insulator layer and free space, respectively. Fig. 3(a) and (b) shows the measured capacitance and conductance values, respectively, as a function of frequency, in the voltage range of 0.0–0.6 V with steps of 0.1 V. It can be seen from Fig. 3 (a) and (b), both the values of capacitance and conductance are higher at the low frequencies with respect to the high frequencies and they are become almost constant up to 100 kHz. These behaviors can be attributed that at low frequencies, the charges at surface states can easily follow an ac signal and the number of them decreases with increasing frequencies.

In order to achieve a better understanding, the effects of series resistance on the C–V and G/ω–V characteristics, all C–V and G/ω–V measurements were corrected using Eq. (13). As an example, the voltage dependent series resistance profile was obtained from the following equation [5] at 500 kHz and is given in Fig. 4.

$$R_s = \frac{G_m}{G_m^2+(\omega C_m)^2} \tag{12}$$

Finally, by comparing the imaginary and real parts of corrected admittance ($Y_c = G_c + j\omega C_c$) one obtains the corrected capacitance (C_c) and conductance (G_c), respectively, as

$$C_c = \frac{\left[G_m^2+(\omega C_E)^2\right]C_m}{a^2+(\omega C_m)^2}, \quad G_c = \frac{G_m^2+(\omega C_m)^2 a}{a^2+(\omega C_m)^2} \tag{13}$$

where $a = G_m - [G_m^2+(\omega C_m)^2]R_s$ and C_m and G_m represent the measured capacitance and conductance measured across the terminal of the diode. As can be seen from Fig. 4, the values of R_s between −3 V and +5 V voltage range are almost constant at strong and week accumulation regions but at depletion and inversion

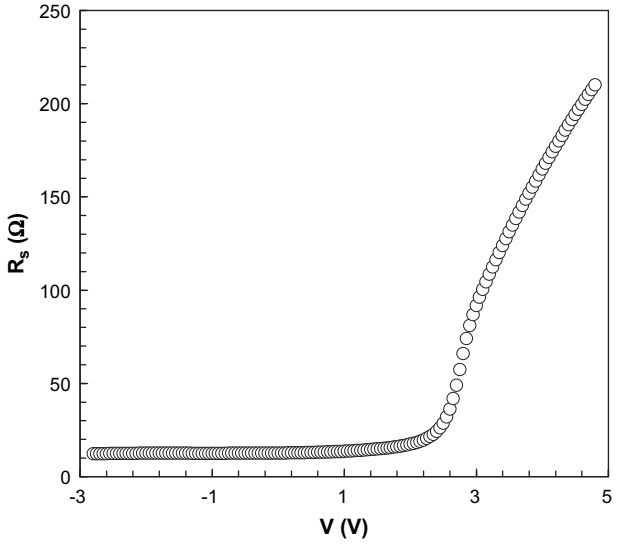

Fig. 4. R_s vs V plots of Au/n-Si Schottky diode for 500 kHz frequency at room temperature.

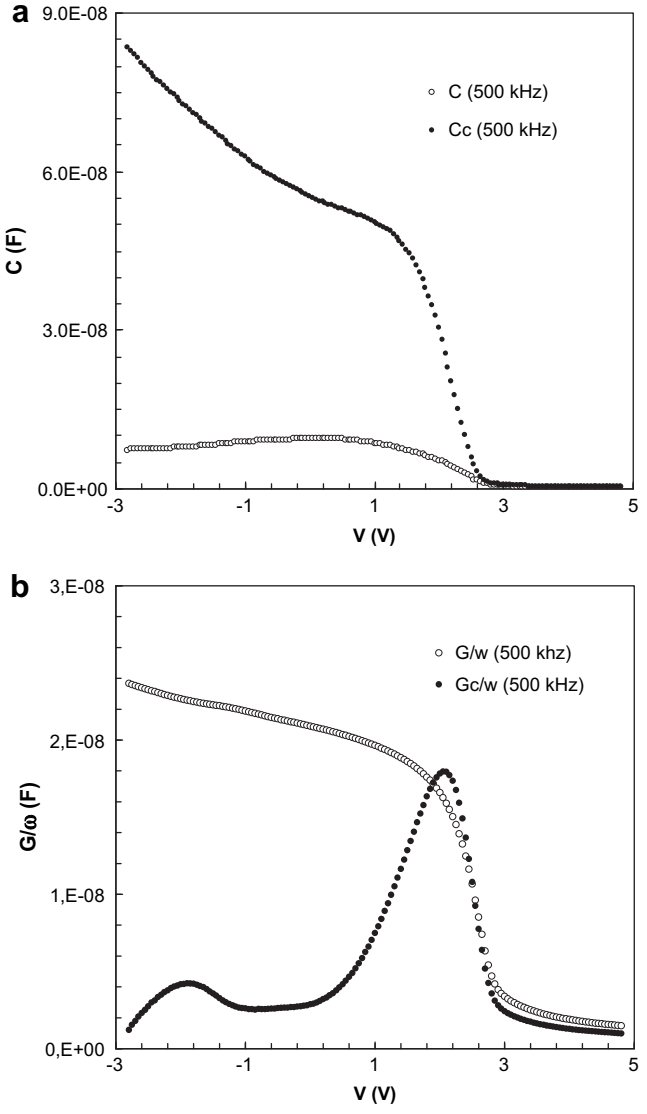

Fig. 5. The voltage dependent plot of the corrected (a) C_c–V and (b) G_c–V plots of Au/n-Si Schottky diode for 500 kHz frequency at the room temperature.

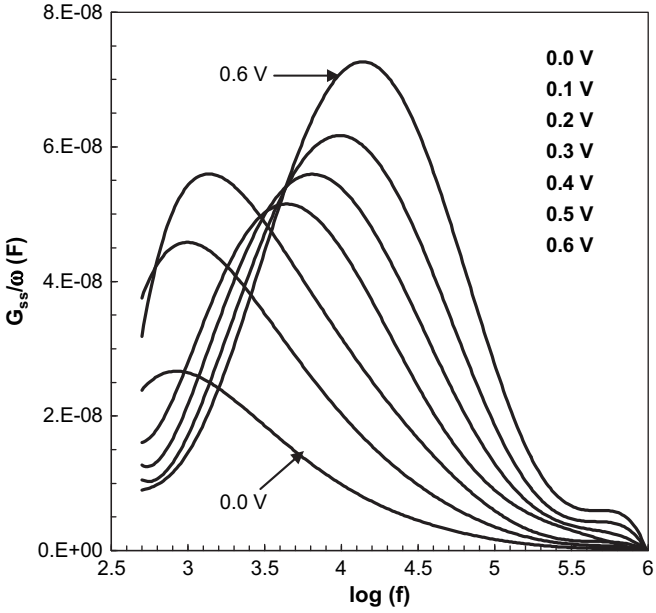

Fig. 6. Measured G_{ss}/ω–f with bias voltage as parameters for Au/n-Si Schottky diode.

regions increases with increasing bias voltage according to literature. Such behavior of R_s is very significant demanded that special attention be given to effects of the series resistance in the application of the admittance-based measurement methods (C–V and G/ω–V). Before and after correcting C–V and G/ω–V plots are given in Fig. 5(a) and (b), respectively. As can be seen in Fig. 5(a) and (b), when the correction was made on the C–V plot for the effects of R_s, the values of the corrected capacitance increases from inversion towards accumulation region. On the other hand, the plot of the corrected conductance (G_c/ω–V) gives two peaks, proving that the charge transfer can take place through the interface. In this case, we can say that the values of R_s are very effective especially in the accumulation region.

The C–V and G–V characteristics of Au/n-Si Schottky diode in the frequency range of 1 kHz–1 MHz are used to characterize the surface state density (N_{SS}) and their lifetime. In the equivalent circuit of diode, the surface states are represented by a capacitance

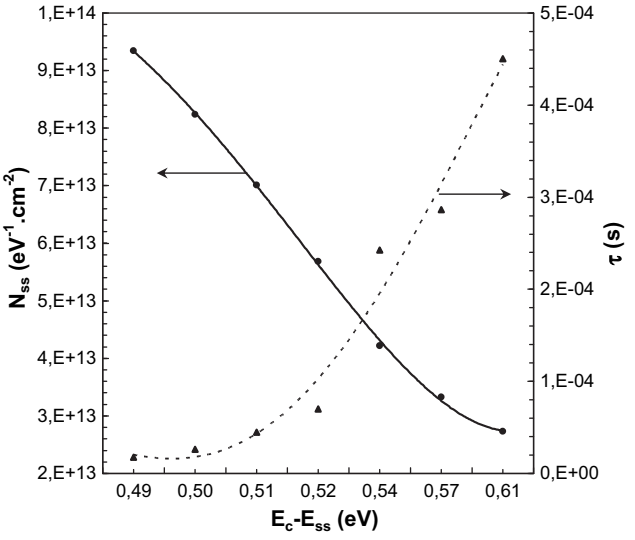

Fig. 7. The energy distribution curves of the surface states and their relaxation times obtained from experimental G_{ss}/ω vs ω characteristics for Au/n-Si Schottky diode.

Table 2
The experimental parameters obtained of Au/n-Si Schottky diode at the room temperature.

V (V)	$E_c - E_{ss}$ (eV)	N_{ss} (eV^{-1} cm^{-2})	τ (s)
0.0	0.610	$2.73E+13$	4.50E − 04
0.1	0.570	$3.32E+13$	2.87E − 04
0.2	0.540	$4.22E+13$	2.43E − 04
0.3	0.525	$5.69E+13$	7.01E − 05
0.4	0.512	$7.01E+13$	4.50E − 05
0.5	0.502	$8.24E+13$	2.63E − 05
0.6	0.493	$9.35E+13$	1.75E − 05

C_{ss} and conductance G_{ss} in parallel with the semiconductor space-charge capacitance C_{sc} and in series to interfacial insulator layer capacitance C_i. The G_{ss}–log f plot of Au/n-Si Schottky diode with thin insulator layer was obtained from the measured forward bias I–V (Fig. 1), C–f (Fig. 3a) and G/ω–f (Fig. 3b) with the help of Eq. (10) is given in Fig. 6. As can be seen from Fig. 6, the G_{ss}/ω–log f plot shows a peak for each bias due to the N_{ss} contribution and the peak position shifts from low frequency to high with increasing bias voltage. At this peak $[\partial(G_{ss}/\omega)/\partial(\omega\tau)] = 0$ and this maximum condition gives $\omega\tau = 1.98$ and it is corresponding to values of $0.403qAN_{ss}$ [4,28,30]. In addition to the peak values increase with increasing bias voltage. In the peak position, the values of surface states (N_{ss}) can be calculated from Eqs. (8) and (10) as

$$N_{ss} = \frac{(G_{ss}/\omega)_{max}}{0.403qA} \tag{14}$$

The energy distribution of surface states (N_{ss}) and the relaxation time (τ) have been determined in the energy range of $(E_c - 0.493E_v)$–$(E_c - 0.610)$ eV taking into account the forward bias I–V data. As can be seen from Fig. 7 and Table 2, these values of N_{ss} and τ change from 9.35×10^{13} eV^{-1} cm^{-2} to 2.73×10^{13} eV^{-1} cm^{-2} and 1.75×10^{-5} s to 4.50×10^{-4} s, respectively. It is clear that the surface states (N_{ss}) have an exponential increase with bias from the midgap towards the bottom of conductance band. On the other hand, the relaxation time has an exponential increase with bias from the bottom of conduction band towards the midgap of Si. Thus, it is seen that the both N_{ss} and τ are bias-dependent. Such behaviors of N_{ss} and τ were also observed in the literature in recent years [28,30–32].

As seen from Figs. 2 and 7, there are a good agreement in the density of surface states (N_{ss}) profiles of the Au/n-Si (MS) Schottky diode obtained from the forward bias I–V measurements and admittance (C–V and G/ω–V) measurements, respectively. However, the admittance method yields lower density of interface states (N_{ss}) than I–V method. The above explanations show that the value of R_s should been taken into account in determining the interface state density distribution profiles in the admittance and I–V methods. Therefore it is necessary to obtain the reliable and acquired results on surface states (N_{ss}) and other main electrical parameters of MS structure.

4. Conclusion

In this study the distribution of the interface state and their relaxation time profile have been obtained from the C–f, G/ω–f characteristics in the frequency range of 1 kHz–1 MHz from the forward bias I–V data. The values of ideality factor and barrier height have been calculated from the forward bias I–V characteristics as 2.878 and 0.652 eV, respectively, at room temperature. The higher values of C and G/ω at low frequencies were attributed to the localized surface states at metal–semiconductor interface. The energy distribution of surface states (N_{ss}) and their relaxation time

(τ) have been determined in the energy range of ($E_c - 0.493E_v$)–($E_c - 0.610$) eV taking into accounts the forward bias *I–V* data. The surface states (N_{ss}) showed an exponential increase with bias from the midgap towards the bottom of conductance band the relaxation time has an exponential increase with bias from the bottom of conduction band towards the midgap of Si. These changes in N_{ss} and τ range from 9.35×10^{13} to $2.73 \times 10^{13}\,eV^{-1}\,cm^{-2}$ and 1.75×10^{-5} s to 4.50×10^{-4} s, respectively.

Acknowledgments

This work is supported by Gazi University Scientific Research Project (BAB), FEF-Research Project FEF 05/2009-34 and FEF 05/2009-56.

References

[1] Card HC, Rhoderick EH. J Phys D Appl Phys 1971;4:1589.
[2] Sze SM. Physics of semiconductor devices. 2nd ed. New York: John Wiley & Sons; 1981.
[3] Cowley AM, Sze SM. J Appl Phys 1965;36:3212.
[4] Nicollian EH, Goetzberger A. Bell Syst Tech J 1967;46:1055.
[5] Nicollian EH, Brews JR. MOS physics and technology. New York: John Wiley & Sons; 1982.
[6] Chattopadhyay P, Daw AN. Solid State Electron 1986;29:555.
[7] Cova P, Singh A, Masut RA. J Appl Phys 1997;82:5217.
[8] Quennoughi Z. Phys Status Solidi A 1997;60:127.
[9] Tataroğlu A, Altındal Ş. J Alloys Compd 2009;479:893.
[10] Castagne R, Vapaille A. Surf Sci 1971;28:157.
[11] Hill WA, Coleman CC. Solid State Electron 1980;23:987.
[12] Chattopadhyay P, Raychaudhuri B. Solid-State Electron 1992;35:875.
[13] Altındal Ş, Tataroğlu A, Dökme İ. Sol Energy Mater SolCells 2005;85:345.
[14] Bülbül MM, Zeyrek S, Altındal Ş, Yüzer H. Microelectron Eng 2006;83:577.
[15] Sato K, Yasamura Y. J Appl Phys 1985;58:3656.
[16] Cheung SK, Cheung NW. Appl Phys Lett 1986;49:85.
[17] Chand S, Kumar J. Semicond Sci Technol 1995;10:1680.
[18] Tung RT. Phys Rev B 1992;45:13509.
[19] Sullivan JP, Tung RT, Pinto MR, Graham WR. J Appl Phys 1991;70:7403.
[20] Kampen TU, Park S, Zahn DRT. Appl Surf Sci 2002;190:461.
[21] Chattopadhyay P, Helder DP. Appl Surf Sci. 1999;143:287.
[22] Karataş Ş, Altındal Ş, Türüt A, Özmen A. Appl Surf Sci 2003;217:250.
[23] Tataroğlu B, Altındal Ş, Tataroğlu A. Microelectron Eng 2006;83:2021.
[24] Tataroğlu A, Altındal Ş. Microelectron Eng 2008;85:233.
[25] Akkal B, Benamara Z, Gruzza B, Bideux L, Bachir Bouiadjra N. Mater Sci Eng C 2002;21:291.
[26] Çetinkara HA, Türüt A, Zengin DM, Erel Ş. Appl Surf Sci 2003;207:190.
[27] Türüt A, Sağlam M. Physica B 1992;179:285.
[28] Akkal B, Benemara Z, Bideux L, Gruzza B. Microelectron J 1999;30:673.
[29] Hanselaer PL, Laflere WH, Van Meirhaeghe RL, Cardon F. Appl Phys A 1986;39:129.
[30] Werner J, Ploog K, Queisser HJ. Phys Rev Lett 1986;57:1080.
[31] Bera MK, Chakraborty S, Saha S, Paramanik D, Varma S, Bhattacharya S, et al. Thin Solid Films 2006;504(1–2):183.
[32] Altındal Ş, Kanbur H, Yücedağ İ, Tataroğlu A. Microelectron Eng 2008;85:1495.