Current-voltage characteristics of metal-oxide-semiconductor devices containing Ge or Si nanocrystals in thin gate oxides

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(Received 16 February 2009; accepted 1 July 2009; published online 18 September 2009)

Current-voltage characteristics were measured, electrically modeled, and calculated for gate oxides, which contain nanocrystals (NCs) in different distributions, sizes, and densities. Ge and Si NCs were synthesized embedded in separate thin SiO_2 layers by ion implantation at different fluences and subsequent annealing. It was found that the currents through the NC containing thin gate oxides are strongly related to the NCs' location and are not driven by ion implantation induced oxide defects. Charging of the NCs determines the internal electrical fields, which is confirmed by simultaneous current and capacitance measurements. Depending on the implanted fluence the Ge NCs were mainly detected in the oxide center or close to the Si/SiO_2 interface. The Si NCs were fabricated in the oxide center sandwiched between two oxide regions denuded of NCs. The processes of Si NC formation, growth and dissolution are discussed by means of kinetic lattice Monte Carlo simulations. © *2009 American Institute of Physics*. [doi:10.1063/1.3190520]

I. INTRODUCTION

Due to a potential application for memory devices,[1] (mainly Si or Ge) nanocrystals (NCs) embedded typically in ≤ 30 nm thin oxide layers are intensively studied in the past decade,[2–5] especially for the case of a short (<5 nm) tunneling distance between the NCs and the Si substrate. Such devices still suffer mainly from weak data retention (less than hours) since for real nonvolatility more than 10 years are required. Tunneling barrier and work function engineering are under discussion to improve the charge storage performance using layered barriers[6] with alternative oxide materials such as HfO_2 or Al_2O_3 and/or metal (e.g., Au, Pt, and W) NCs,[7] respectively, and also double stacked storage nodes.[8] Although attention is focused on the programming and storage behavior, current-voltage (*I-V*) characteristics are of great interest with respect to the oxide stability and the role of leakage currents during write and erase operations. Such characteristics involve all charging and decharging mechanisms such as the injection of holes and electrons from the Si substrate or gate electrode as well as their injection and ejection to/from the tiny semiconductor NCs. Different charge transfer mechanisms were discussed considering charging (or noncharging) currents in memory structures containing a floating gate,[9] a Si_3N_4 trapping layer,[10] or Si NCs (Ref. 11) embedded in the gate oxide. For Si implanted oxides charge trapping is supposed to be dominant[12] neglecting the final spatial distribution of charge conducting sites such as the formation of NCs. More reliable, a transient electrical model was developed to describe programming characteristics of Ge NCs embedded in thin gate oxides.[13] Enabled by this model it was possible to determine individual tunneling distances (tunneling oxide thickness) between the Si substrate and the NCs from electrical capacitance-voltage (*C-V*) measurements.[14] Here, this transient model[13] is extended to evaluate the *I-V* characteristics for 20 nm thin gate oxides with embedded Ge or Si NCs prepared by ion beam synthesis (IBS).[2,15–18] Despite a similar initial profile of Ge and Si impurities in SiO_2 after the ion implantation, the final distributions of the NCs are quite different. Since after Ge^+ implantation a narrow layer of Ge NCs was obtained in vicinity to the Si/SiO_2 interface during annealing (a favored configuration for NC memory devices),[19] a broad layer of Si NCs formed in the oxide center sandwiched between two oxide layers in the case of Si implantation. The determination and localization of the embedded NCs are a few of the particular challenges to give a reliable electrical model to explain the charge transfer characteristics of such oxides. These structural data were derived from transmission electron micrographs and discussed by means of kinetic lattice Monte Carlo (KLMC) simulations in order to understand the role of a close Si substrate for the Si NC formation.[20,21] Respective *I-V* characteristics were calculated based on a detailed electrical model with significant agreements to measurements obtained on metal-oxide-semiconductor (MOS) capacitors with Si and Ge NCs embedded in the gate oxides.

II. EXPERIMENTAL DETAILS

$^{74}Ge^+$ or $^{28}Si^+$ ions were implanted with different energies and fluences (summarized in Table I) into 20 nm thick gate oxides, which were thermally grown on ⟨100⟩ *p*-Si substrates with a resistivity of 10 Ω cm. After standard cleaning in H_2O_2/H_2SO_4, rapid thermal annealing was carried out between 950 and 1050 °C for 30 or 120 s in Ar atmosphere. MOS capacitors were prepared in 3×10^{-4} cm^2 (Ge) and

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TABLE I. Low (LD) and high fluence (HD) ion implantation and annealing parameters.

Ion	Energy (keV)	LD (cm^{-2})	HD (cm^{-2})	Annealing
$^{74}Ge^+$	12	5×10^{15}	1.5×10^{16}	950 °C/1050 °C, 30 s
$^{28}Si^+$	6	7×10^{15}	2.0×10^{16}	1050 °C, 30 s/120 s

1×10^{-3} cm^2 (Si) size by Al sputtering, photolithographic patterning, and furnace annealing at 400 °C for 15 min in N_2. The NCs' distribution in the gate oxide is characterized by bright and high angle annular dark field (HAADF) high-resolution (HR) transmission electron microscopy (TEM) using a Philips CM300 microscope operating at 300 kV. Energy-filtered TEM (EF-TEM) investigations were performed to detect tiny Si NCs using a Gatan image filter in a 200 keV FEI Tecnai 20 FEG microscope with a 5 eV window and 18 eV onset at a collection angle of 15 mrad. The Ge, Si, and O profiles were characterized by Rutherford backscattering spectrometry (RBS) using 1.7 MeV He^+ ions; the incident angle was set to 70° to improve the depth resolution (scattering angle is 170°). The current-voltage (*I-V*) characteristics of the MOS capacitors were obtained by a Keithley 237 voltage source. A Keithley 590 capacitance-voltage (*C-V*) analyzer working at 100 kHz and a Keithley 617 electrometer were combined (using a Keithley 590-1 coupling box) to provide simultaneous capacitance and current acquisition during a stepwise voltage sweep (see Fig. 1).

III. MODELING OF *I-V* CHARACTERISTICS FOR GATE OXIDES WITH EMBEDDED NCS

A MOS structure is electrically modeled for both gate voltage polarities as shown in Fig. 2 with two parallel NC layers embedded in a gate oxide with NC densities $N_{nc1,2}$ and same NC sizes $d_{nc1,2}$ within each layer. The NC layers are separated to the Si substrate and to each other by the tunneling oxides d_{tox1} and d_{tox2}, respectively, and to the gate electrode by the top-oxide d_{top}. Tunneling of electrons or holes from Si electrodes through oxides of different size can generally be described by the equations[22–24]

$$J_{\text{DT-FN},c} = \frac{q^3(m_{\text{Si},c}/m_{\text{ox},c})}{8\pi h\phi_{b,c}} E_{\text{tox}}^2 \Theta_{\text{ox},c}, \tag{1}$$

with

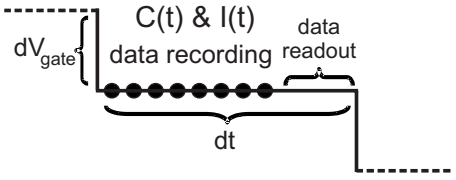

FIG. 1. Sequence of the simultaneous capacitance and current measurements during a stepwise gate voltage sweep performed with $dV_{gate}=-0.5$ V. During a time period of $dt=7$ s at constant gate voltage, capacitance and current data are recorded in intervals of 300 ms followed by a data readout from the measurement instruments.

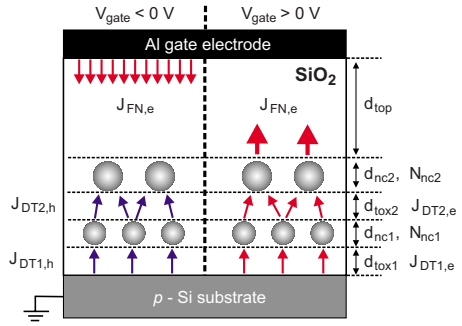

FIG. 2. (Color online) Schematic of a NC containing gate oxide with two embedded NC layers of different NC sizes and densities. The flux of electrons and holes is indicated by colored arrows (red and blue, respectively) depending on the V_{gate} polarity.

$$\Theta_{\text{ox},c} = \exp\left(-\frac{8\pi\sqrt{2m_{\text{ox},c}}[\phi_{b,c}^{3/2} - [\Gamma^{3/2}\times H(\Gamma)]]}{3hq|E_{\text{tox}}|}\right),$$

$$\Gamma = (\phi_{b,c} - |qV_{\text{tox}}|) \quad \text{and} \quad c = e|h,$$

whereas the Heaviside function $H(x)$ enables a continuous transition between direct tunneling (DT) [$H(x)=1$ for $\Gamma>0$, i.e., $J_{\text{DT-FN}}=J_{\text{DT}}$] and Fowler–Nordheim (FN) tunneling [$H(x)=0$ for $\Gamma\leq0$, i.e., $J_{\text{DT-FN}}=J_{\text{FN}}$]. Θ_{ox} is the transmission probability for charge carriers through the respective oxide according to a parabolic dispersion relation with respect to Wentzel–Kramers-Brillouin approximation.[10,22,24,25] h is Planck's constant, q the magnitude of electron charge, and m_0 the free electron mass. Depending on the gate voltage polarity, holes ($V_{gate}<0$ V) or electrons ($V_{gate}>0$ V) are injected from the accumulated or inverted *p*-Si substrate toward the NCs. $V_{tox1,2}$ and $E_{tox1,2}=V_{tox1,2}/d_{tox1,2}$ are the voltage drop and the electric field across the tunneling oxides, respectively; the same holds for the top-oxide voltage drop V_{top} with $E_{top}=V_{top}/d_{top}$. Values for the tunneling barrier height ϕ_b and the effective hole or electron masses in the Si substrate m_{Si} and in the oxide m_{ox} are summarized in Table II (h and e indicate holes and electrons, respectively). m_{Si} has

TABLE II. Summarized parameter for the tunneling barriers ϕ_b and the effective hole and electron masses for DT and FN tunneling.

	Emitting electrode	Tunneling barrier	Effective masses
FN	Si (inv.)	$\phi_{b,e}=2.9$ eV [a]	$m_{ox,e}=0.5m_0$ [a] $m_{Si,e}\approx m_0$ [b]
	Al	$\phi_{b,e}=3.2$ eV [c]	$m_{ox,e}=0.5m_0$ [a] $m_{Al,e}=m_0$ [a]
DT	Si (acc.)	$\phi_{b,h}=4.5$ eV [d,e]	$m_{ox,h}=0.32m_0$ [d,e] $m_{Si,h}\approx m_0$ [d]
	Si (inv.)	$\phi_{b,e}=2.9$ eV	$m_{ox,e}=0.42m_0$ [f] $m_{Si,e}\approx m_0$ [b]
DT	Ge NC	$\phi_b=f(d_{nc})$ [g]	$m_{Ge,h}=0.324m_0$ [c] $m_{Ge,e}=1.64m_0$ [c]

[a]Reference 22.
[b]Reference 24.
[c]Reference 26.
[d]Reference 13.
[e]Reference 25.
[f]See Fig. 3.
[g]See Table IV.

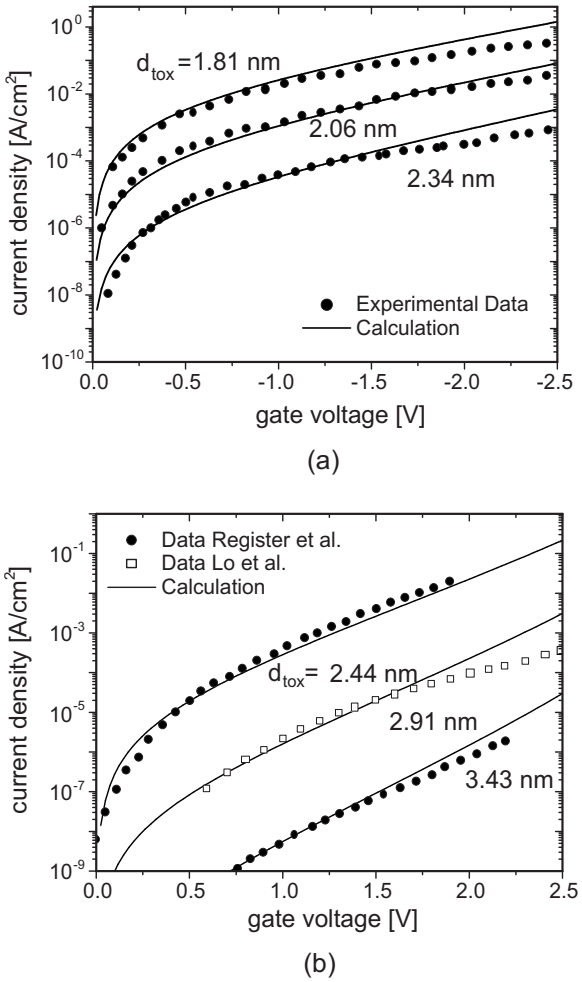

FIG. 3. Calculated DT currents of holes (a) and electrons (b) according to Eq. (1) with $H(x)=1$ in comparison to experimental data with the same oxide thicknesses (hole current: Refs. 27–29; electron current: Refs. 30 and 31). The best fit is achieved for $\phi_{b,h}=4.5$ eV with $m_{ox,h}=0.32m_0$ (Ref. 25) (a) and $\phi_{b,e}=2.9$ eV with $m_{ox,e}=0.42m_0$ (b) [$m_{Si,e}=0.916m_0 \approx m_0 \approx m_{Si,h}$ (Refs. 13 and 24)].

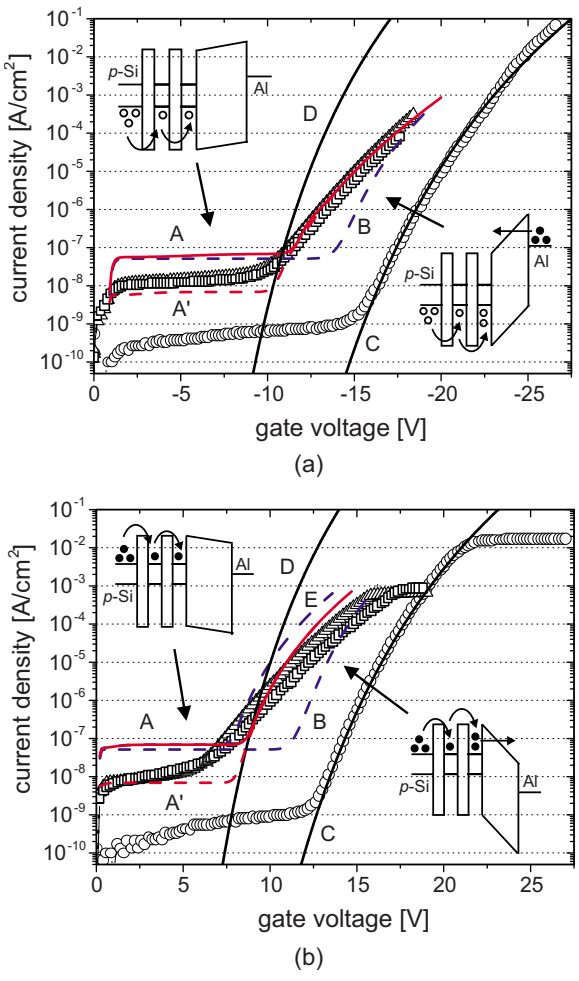

FIG. 4. (Color online) *I-V* characteristics for the Ge LD implanted oxides annealed at 950 °C (□) and 1050 °C (△) and the unimplanted reference (○) for comparison, all for each gate voltage polarities in (a) and (b), respectively. The red and blue lines (curves A, B, and E) reflect the results of the model calculations related to Ge NC containing oxides. The straight black lines (curves C and D) show the calculated FN currents [using Eq. (1)] for pure oxides of different thicknesses without NCs. Used structural and electrical parameters are summarized in Tables II–IV. Sweep rates are 0.25 V/s for the measurements and calculations, reduced to 0.025 V/s for calculations of curves A′ ($V_{fb}=-0.8$ V and $V_t=0.1$ V for all calculations). For curve E the electron barrier height is set to $\phi_{b,e}=2.7$ eV, which corresponds to a Ge NC size of about 1 nm for NC layer 2. The insets reflect schematically the charge transfer processes for the respective current components.

to be replaced by m_{Al} or m_{Ge} if the charges are ejected from the Al gate electrode or the Ge NCs, respectively. For the DT regime ϕ_b and m_{ox} are verified in Fig. 3 by means of recently published current-voltage data using Eq. (1) with $H(x)=1$. In order to validate ϕ_b and m_{ox} for FN tunneling of electrons, reference data (unimplanted oxides) are fitted in Figs. 4–6 (curves C) using Eq. (1) with $H(x)=0$ and a gate oxide thickness of $d_{ox}=20.5$ nm (or 20.7 nm, respectively).

The total current density J_{tot} has three different components describing the charging/discharging of the gate oxide from the electrodes. The first layer of NCs is charged from the substrate side by $J_{DT1}=f(V_{tox1},d_{tox1})$ [see Eq. (1) in the DT regime]. $J_{FN,e}$ describes the charge exchange with the gate electrode through the top-oxide by a FN mechanism if $d_{top}>5$ nm. Here, the current through the oxide J_{ox} besides the NCs is negligible in most cases,

$$J_{tot}=R_{nc1}J_{DT1}+J_{FN,e}+(1-R_{nc1})J_{ox}\approx R_{nc1}J_{DT1}+J_{FN,e}. \quad (2)$$

The relative portion of area covered by NCs R_{nc} (surface coverage ratio), given by the ratio of the square NC surfaces A_{nc} to the total capacitor area A_{tot}, is a key factor of memory programming characteristics and not only the dot density N_{nc},[32]

$$R_{nc}=A_{nc}/A_{tot}=\frac{\pi}{4}d_{nc}^2N_{nc}. \quad (3)$$

The charge density on the first NC layer Q_{nc1} determines the current density $J_{DT2}=qnfT$ from the first NC layer to the second.[25,33] There, T is the oxide transparency, f the impact frequency against the barrier, and n is the density of charge carriers available for tunneling; thus $qn=Q_{nc1}$. With $\varepsilon_{ox}\varepsilon_0E_{tox2}=Q_{nc1}$ Eq. (1) changes with $H(x)=1$ (DT is dominant with $d_{tox2}\approx 2$ nm) to

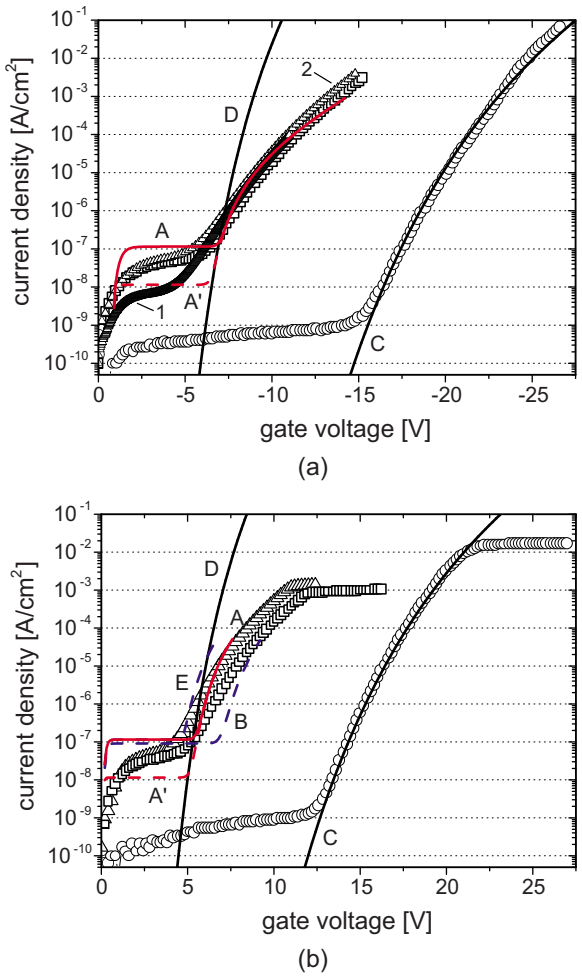

FIG. 5. (Color online) Measured and calculated *I-V* characteristics for the Ge HD implanted samples (for details, see caption of Fig. 4). In (a) data for different sweep rates are shown for 0.025 V/s (1 and A′) and 0.25 V/s (2 and A).

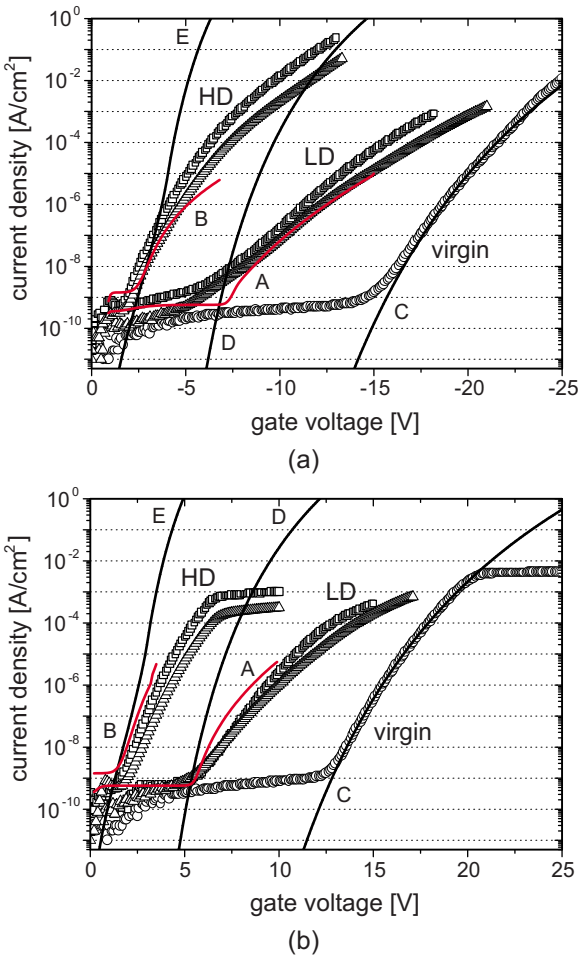

FIG. 6. (Color online) Measured and calculated *I-V* characteristics for the Si implanted [fluence LD and HD, annealed at 1050 °C for 30 s (□) and 120 s (△)] and for the unimplanted oxides (○) for both gate voltage polarities with respect to Eqs. (1) and (2), solved for 1% capacitor area, and Table V. The calculated characteristics for Si NC containing oxides are indicated by red lines (A and B) and for single oxides by black lines (C–E) with $V_{fb}=-0.8$ V, $V_t=0.1$ V, and $m_{ox}=0.5m_0$. Measurements and simulations were performed for 0.125 V/s sweeps.

$$J_{DT2}=\frac{q^3(m_{nc}/m_{ox})}{8\pi h\phi_b}\frac{Q_{nc1}}{\varepsilon_{ox}\varepsilon_0}|E_{tox2}|\Theta_{tox2}, \tag{4}$$

with $\Theta_{tox2}=f(V_{tox2},d_{tox2})$. In the same way we find for the current from layer 2 to the gate electrode

$$J_{FN,e}=\frac{q^3(m_{nc}/m_{ox})}{8\pi h\phi_b}\frac{Q_{top}}{\varepsilon_{ox}\varepsilon_0}|E_{top}|\Theta_{top}. \tag{5}$$

m_{nc} is the effective mass of charge carriers in the NCs. The effective mass of holes in Ge NCs $m_{Ge,h}$ is set to its bulk value as a sum of the effective masses of light and heavy holes[27] $m_{nc,h}=m_{Ge,h}=m_{Ge,lh}+m_{Ge,hh}=(0.044+0.28)m_0=0.324m_0$;[26] for electrons $m_{nc,e}=m_{Ge,e}=1.64m_0$.[26]

The current through the gate oxide with embedded NCs is calculated as a function of sweep time. Thus, the actual NC charge areal density Q_{nc} on each layer is iteratively calculated using

$$Q_{nc1,2}(t_{i+1})=Q_{nc1,2}(t_i)+dQ_{nc1,2}(t_i), \tag{6}$$

$$dQ_{nc1}(t_i)=[R_{nc1}J_{DT1}(t_i)-R_{nc2}J_{DT2}(t_i)]\Delta t,$$

and

$$dQ_{nc2}(t_i)=[R_{nc1}J_{DT2}(t_i)-J_{FN,e}]\Delta t.$$

The equations hold for small time increments Δt so that the potentials within the gate oxide do not change significantly between the time steps t_i and t_{i+1}. For the case $V_{gate}\lessapprox 0$ V a radiative (e.g., band to band with light emission) or nonradiative recombination (e.g., Auger) of electron hole pairs in the NCs of layer two (Q_{nc2}) is assumed. Thus,

$$V_{tox1}=\frac{d_{tox1}}{d_{tot}}\left[V'_{gate}+\frac{Q_{nc1}}{\varepsilon_{ox}/(d_{k2}+d_{top})}+\frac{Q_{nc2}}{\varepsilon_{ox}/d_{top}}\right],$$

$$V_{top}=\frac{d_{top}}{d_{tot}}\left[V'_{gate}-\frac{Q_{nc1}}{\varepsilon_{ox}/d_{k1}}-\frac{Q_{nc2}}{\varepsilon_{ox}/(d_{tot}-d_{top})}\right],$$

$$V_{tox2}=\frac{d_{tox2}}{d_{k2}}\left[V'_{gate}-\frac{d_{k1}}{d_{tox1}}V_{tox1}-V_{top}\right] \tag{7}$$

with

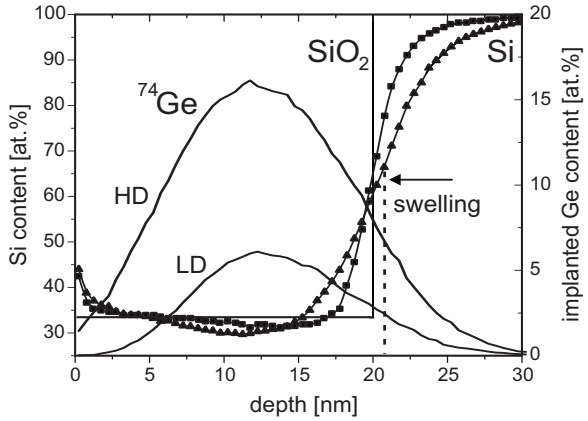

FIG. 7. Si content (left ordinate) and Ge profiles (right ordinate) after Ge ion implantation into 20 nm SiO_2. The Si content is obtained from TRIDYN calculations (Ref. 35) [LD (■) and HD (▲)] taking sputtering and swelling effects into account (dashed line). The box shape profile indicates the Si concentration before implantation. The implanted Ge profiles (right ordinate) are given by straight lines.

$$d_{\mathrm{tot}} = d_{k1} + d_{k2} + d_{\mathrm{top}},$$

$$d_{k1} = d_{\mathrm{tox1}} + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{nc}}} d_{\mathrm{nc1}},$$

$$d_{k2} = d_{\mathrm{tox2}} + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{nc}}} d_{\mathrm{nc2}},$$

assuming for simplicity that the charges in the NCs (electrons or holes) are located at the NC/SiO_2 interface toward the gate electrode. As shown by electron density calculations, this is a reasonable approximation for biased tiny spherical Si nanodots embedded in SiO_2.[34] $\varepsilon_{\mathrm{ox}}$ and $\varepsilon_{\mathrm{nc}}$ are the dielectric constants for SiO_2 and the NC material (bulk value), respectively,

$$V'_{\mathrm{gate}} = V_{\mathrm{gate}} - V_x(t_0). \tag{8}$$

$V_x(t_0)$ is the initial flat-band (V_{fb}) or threshold (V_t) voltage for the uncharged state disregarding the exact Si substrate surface potential.

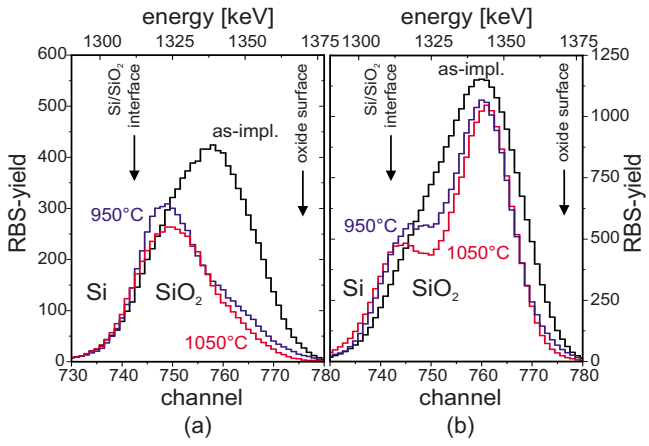

FIG. 8. (Color online) Ge profiles as obtained by RBS for the lower and the higher fluence implanted samples in (a) and (b), respectively. With annealing about 40% (LD) or 25% (HD) of the initially implanted Ge amount disappeared. The data are smoothed for clarity averaging five adjacent.

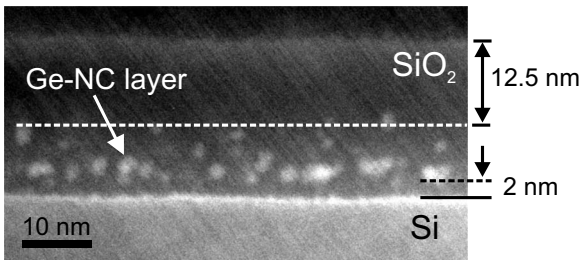

FIG. 9. HAADF STEM micrograph after Ge implantation LD in 20 nm SiO_2 and annealing at 950 °C for 30 s. Bright spots indicate Ge NCs of about 2 nm size arranged in a layer close to the Si/SiO_2 interface in a very high density and also a few NCs distributed close to these toward the oxide bulk.

IV. GE NC CONTAINING GATE OXIDES

A. Structural data for Ge implanted gate oxides

After ion implantation (Fig. 7) the peak concentration of Ge in the oxide reaches of about 7 (LD) or 16 at. % (HD). IBS of Ge NCs in thin SiO_2 is associated with a significant redistribution (and also a partial loss) of the implanted Ge as shown in Fig. 8; its physical origin has been described elsewhere.[19] Depending on the implantation fluence, a layer of tiny Ge NCs (d_{nc}=2 nm) is formed in vicinity to the Si/SiO_2 interface or a layer of bigger ones (d_{nc}=4 nm) in the oxide center as shown in Figs. 9 and 10, respectively. In both cases during annealing a top-oxide region forms without Ge NCs. In order to transfer these structures into a one-dimensional electrical model, the statistical distribution of Ge NCs is simplified into two parallel NC layers as shown schematically in Fig. 2. The thicknesses of the oxides and NC layers are summarized in Table III as deduced from the TEM micrographs in Figs. 9 and 10. Ideal DT charge conduction is assumed from layer to layer, although probably also trap-assisted tunneling mechanisms may be involved in the real system. Although hardly detectable in Fig. 10, a high concentration of Ge precipitates enables an effective charge exchange between the main NC layer and the Si substrate similar to an intermediate layer of tiny NCs. The d_{nc} and N_{nc} values for both layers are deduced from the TEM micrographs to calculate R_{nc} (see Table IV). The evaluation of the band gap energy of tiny Ge NCs in Table IV and thus of the tunneling barriers ϕ_b for electron and holes emission from

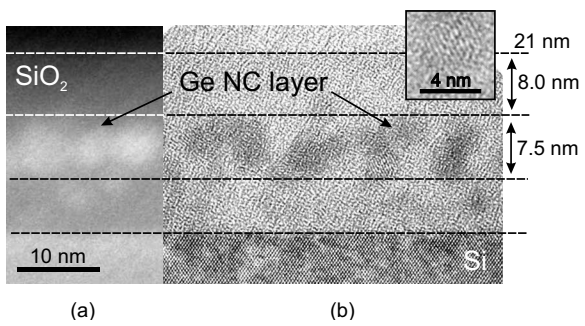

FIG. 10. Merged TEM micrographs obtained at HAADF (a) and high resolution bright field (b) conditions for the same high fluence Ge implanted sample (HD) annealed at 950 °C for 30 s. A high density of Ge NCs in 4 nm size is detected in the oxide center and also smaller ones (or just precipitates) between this NC layer and the Si substrate.

TABLE III. Structural parameters used in the calculation of the current-voltage characteristics (distances in nanometer). Letters A–E refer to the simulated *I-V* curves in Figs. 4 and 5.

Fluence	Curve	d_{tox1}	d_{nc1}	d_{tox2}	d_{nc2}	d_{top}	d_{ox}
LD	A/E	2.0	2.0	2.3	2.0	12.5	20.8
	B	2.0	2.0	⋯	⋯	16.8	20.8
	C	⋯	⋯	⋯	⋯	⋯	20.5
	D	⋯	⋯	⋯	⋯	⋯	16.8
HD	A/E	2.0	2.0	2.0	7.5	8.0	21.5
	B	2.0	2.0	2.0	6.0	9.5	21.5
	C	⋯	⋯	⋯	⋯	⋯	20.5
	D	⋯	⋯	⋯	⋯	⋯	8.0

the Ge NCs needs a more detailed discussion. Due to quantum confinement the band gap energy of tiny NCs increases with decreasing NC size. This effect is significantly quenched considering oxygen passivated NCs as in the present case of Ge NCs embedded in SiO_2.[36] As shown in Fig. 11, Ge NCs of 2 nm size have a band gap energy of about 1.1 eV, which leads to tunneling barrier heights of $\phi_{b,e} \approx 2.9$ eV and $\phi_{b,h} \approx 4.5$ eV with respect to SiO_2 using the Ge bulk electron affinity (χ=4.0 eV) and the bulk energy gap of E_g=0.67 eV (Ref. 26) as a reference (see Ref. 13 for details).

B. Current-voltage (*I-V*) characteristics

In Figs. 4 and 5 measured *I-V* characteristics for both gate voltage polarities are shown for the virgin (reference) and Ge implanted oxides superimposed with the calculation results. For negative gate voltages the minority carrier generation in the Si substrate is stimulated by light exposure. Nevertheless, the generation rate limits the number of electrons available for tunneling leading to a saturation of the tunneling currents in Figs. 4(b) and 5(b).

Especially in Figs. 4(a) and 5(a) the calculated *I-V* characteristics (labeled as A) show significant agreements with the measured data (symbols). As schematically shown in the insets of Fig. 4(a), at negative V_{gate} the Ge NCs in both layers are positively charged by DT of holes from the *p*-Si substrate. As a consequence V_{gate} drops mainly across d_{top} where finally electrons are injected from the metal gate side by FN tunneling indicated by the rapidly rising current at V_{gate}=−10 or −6 V in Figs. 4(a) and 5(a), respectively. These electrons get trapped at the Ge NCs and compensate the positive charges, e.g., by radiative recombination of electron-hole pairs. Accordingly, for positive V_{gate} [Figs. 4(b) and 5(b)], the NCs are charged by electrons, which are emitted at high gate voltages from individual NCs toward the gate electrode (high current region). On the contrary to homogenous emission of electrons from an equal potential metal gate electrode (V_{gate}<0 V), in this case the curved surfaces of the tiny NCs cause an inhomogeneous emission due to enhanced electrical fields near the NC/top-oxide interface.[39] This might explain the slight differences between the calculated characteristic and the measured data in Figs. 4(b) and 5(b). Individually deviating NC sizes with different $\phi_{b,e}$ have to be taken into account (curve E for smaller NCs) as well as the emission of electrons at high gate voltages from NCs that are located deeper in the oxide (curves B for a single NC layer). However, the high current part of the *I-V* characteristics is related to the FN emission of electrons from the gate electrode or from the NCs side across d_{top} depending on the V_{gate} polarity. Thus, the onset for this FN current coincidences with calculated characteristics for FN tunneling through a pure thermally grown oxide (curves D in Figs. 4 and 5) with a thickness similar to top-oxide thicknesses d_{top} as deduced from the TEM of the Ge NC containing oxides (see Table III). Hole FN tunneling can be neglected due to the high barrier toward SiO_2. The annealing temperature has only a marginal influence on the shape of the *I-V* characteristics.

TABLE IV. Ge NC sizes d_{nc} and densities N_{nc} as deduced from the STEM images in Figs. 9 and 10 in a two layer approximation together with the relative NC capacitor area ratios R_{nc} and tunneling barrier heights ϕ_b obtained using Eq. (3) and Fig. 11, respectively. E_g is the Ge NC band gap energy.

Fluence	Layer	d_{nc} (nm)	N_{nc} (cm^{-2})	R_{nc}	E_g (eV)	$\phi_{b,e}$ (eV)	$\phi_{b,h}$ (eV)
LD	1	2.0	3×10^{12}	0.1	1.1	2.9	4.5
	2	2.0	3×10^{11}	0.01	1.1	2.9	4.5
HD	1	2.0	1×10^{12}	0.03	1.1	2.9	4.5
	2	4.0	5×10^{12}	0.6	0.9	3.0	4.6

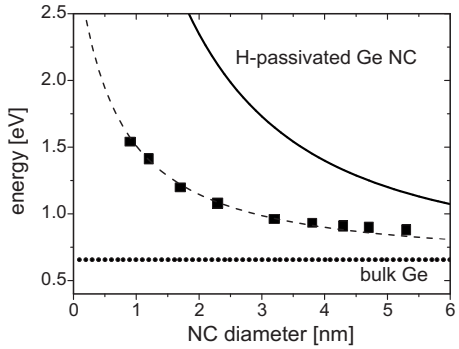

FIG. 11. Calculated quantum confinement of H-passivated Ge NCs after Niquet *et al.* (Ref. 37) (straight line) as function of NC size in comparison to measured photoluminescence (PL) data (Ref. 38) for oxygen passivated Ge NCs (■).

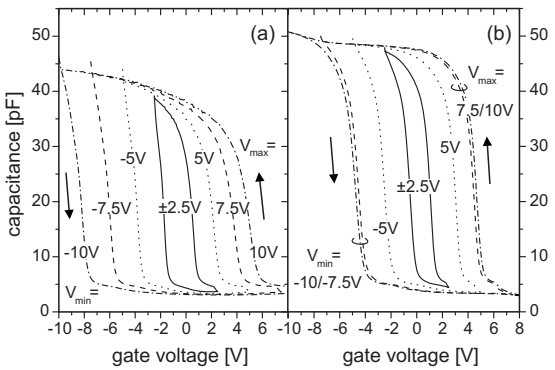

FIG. 12. *C-V* hysteresis characteristics for Ge implanted gate oxides, LD (a) and HD (b), both annealed at 950 °C for 30 s. Sweep direction is $V_{min} \rightarrow V_{max} \rightarrow V_{min}$ for ±2.5 V/±5 V/±7.5 V/±10 V amplitudes.

For both polarities the measured *I-V* characteristics reveal in the low voltage range [e.g., $-10\ \mathrm{V} < V_{\mathrm{gate}} < 6\ \mathrm{V}$ in Fig. 5(a)] a nearly constant current, which is for the NC containing gate oxides about 100 times higher than for the unimplanted oxides. This current level decreases proportional to the sweep rate in both simulation (labeled as 1 and 2) and measurement (A and A′) in Fig. 5(b). The FN tunneling current is not affected by the sweep rate. Both for the unimplanted reference and for the implanted oxide, this nearly constant current can be described by a displacement current, which is $J_{\mathrm{dpl}} = C_{\mathrm{ox}}(dV_{\mathrm{gate}}/dt)$ for the reference. $C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/d_{\mathrm{ox}}$ is the oxide capacitance and dV_{gate}/dt is the sweep rate. The measured J_{dpl} value for the unimplanted reference is about two orders lower than the theoretical value of $J_{\mathrm{dpl}} = 4.2 \times 10^{-8}\ \mathrm{A/cm^2}$ because V_{gate} is not swept constantly but stepwise. Thus, J_{dpl} decreases exponentially during the delay time after each voltage step of 0.5 V (see Fig. 1), which is performed to achieve a higher current resolution. For the NC containing oxides J_{dpl} corresponds to the nonequilibrium charging current of the top-oxide through $d_{\mathrm{tox1,2}}$. With the changing voltage drop across the tunneling oxides with time during the stepwise charging process, also the resistance of $d_{\mathrm{tox1,2}}$ changes according to Eq. (1). This variable resistance of the tunneling oxides defines the time constant of charging and also of the decay of J_{dpl} after each voltage step. A higher low voltage current for the Ge HD implanted compared to the Ge LD implanted sample reflects the different tunneling or charging resistances and/or mechanisms. In the latter case a well-defined NC layer with a higher NC density is charged, whereas in the first case (HD) the current is probably more related to a trappinglike conduction.

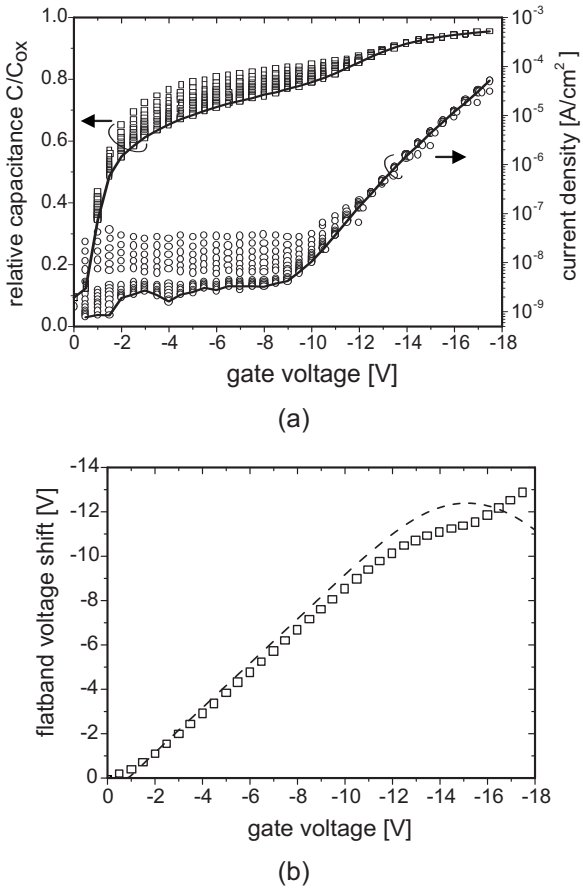

FIG. 13. (a) *C-V* and *I-V* data simultaneously recorded as a function of sweep time for the Ge LD implanted sample annealed at 950 °C for 30 s (sweep rate is about 0.07 V/s). Straight lines connect the last datum of each branch. (b) Flat-band voltage shift ΔV_{fb} calculated from capacitance-voltage data from (a) and Ref. 13 using Eq. (9) (□). The broken line corresponds to the simulated current-voltage curve A in Fig. 4(a).

C. Simultaneous *C-V*/*I-V* measurements

C-V characteristics were obtained to reveal the charging behavior of the Ge NC containing gate oxides (see Fig. 12). Already very small sweep amplitudes of ±2.5 V create a significant *C-V* hysteresis. Holes as well as electrons are rapidly stored at the NCs in similar amount where the *C-V* characteristics shift continuously with the applied voltage (see Ref. 13 for details). Thus, the characteristics for the Ge LD implanted oxide in Fig. 12(a) do not reach the expected maximum capacitance value of about $C_{\mathrm{ox}} = 50$ pF. This rapid shifting in the *C-V* curves enables a novel measurement where during the voltage sweep capacitance and current data are simultaneously recorded to trace the charging of the NCs as a function of sweep time and the applied gate voltage V_{gate} [see Fig. 13(a)]. The vertical branches in the *I-V* characteristic reflect the exponentially decaying charging current with time at constant V_{gate}, which is mirrored in the *C-V* characteristic confirming the interpretation of the *I-V* characteristics in previous chapter. Continuous charging of the Ge NCs with holes leads to a simultaneously decreasing flat-band voltage, i.e., the *C-V* characteristic follows the applied gate voltage. In Fig. 13(b) the corresponding flat-band voltage shift ΔV_{fb} is shown as a function of V_{gate}, which is calculated from the capacitance data in Fig. 13(a),

$$\Delta V_{\mathrm{fb}}(V_{\mathrm{gate}}, t) = V_{\mathrm{meas}}(C_{\mathrm{meas}}, t) - V_0(C_{\mathrm{meas}}). \tag{9}$$

Related to the same capacitance data C_{meas}, the corresponding voltage values from the measured characteristic in Fig. 13(a) (V_{meas}) are referenced to voltage data V_0 from the *C-V* characteristics for the uncharged state (obtained from the same sample at $dV_{\mathrm{gate}}/dt = 100\ \mathrm{V/s}$ shown in Ref. 13). ΔV_{fb}, i.e., the total charge stored in the NCs, saturates with increasing FN current [symbols in Fig. 13(b)], which limits the shifting of the *C-V* characteristic as indicated by the hump in Fig. 13(a). Holes captured in the NCs are compensated with electrons injected from the gate electrode. For the same reason the *C-V* hysteresis in Fig. 12(b) saturates at ±7.5 V sweep amplitudes for the Ge HD implanted sample. However, the trend of the characteristics in Fig. 13(b) is similar comparing the data deduced from the continuous capacitance-current measurements with the results from the simulated current-voltage curves. Thus, the validity of the presented electrical model for the charge transfer through NC containing gate oxides is clearly confirmed. Deviations can be explained by uncertainties defining the exact position of stored and compensated charges within the gate oxide and/or the different sweep rate. For further decreasing V_{gate}, a decreasing charge amount is shown in Fig. 13(b) (dashed line) as the electron current is higher than the number of available

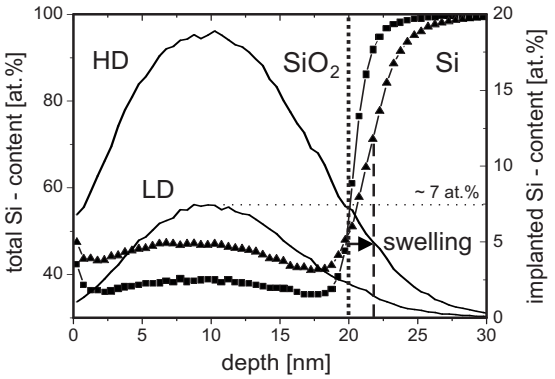

FIG. 14. Total Si content after Si ion implantation into 20 nm SiO_2 [LD (■) and HD (▲)] as obtained from TRIDYN calculations (Ref. 35) taking sputtering and swelling effects into account (dashed line). The dotted line indicates the pristine position of the Si/SiO_2 interface. The implanted Si profiles (right ordinate) are given by straight lines.

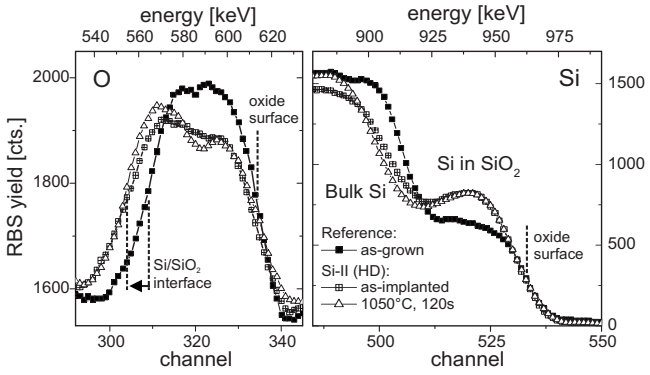

FIG. 15. RBS data related to the oxygen and silicon signals for the high fluence Si implanted oxide (HD) in the as-implanted state (⊞) and after annealing at 1050 °C for 120 s (△) in comparison to the as-grown reference sample (■). The elemental composition of the oxide changes after Si ion implantation by an enhanced Si signal and a reduced O yield with respect to the unimplanted reference.

and refilling holes in the NCs in the simulations in Fig. 4(a). This behavior is not reproduced from the data extracted from Fig. 13(a) since a reliable interpretation of the recorded data is not possible if C_{meas} approaches C_{ox} for $V_{gate} < -14$ V.

V. SI NC CONTAINING GATE OXIDES

A. Formation of Si NCs in thin gate oxides after Si ion implantation

Ion profile calculations in Fig. 14 reveal a broad distribution of implanted Si in SiO_2 (line). However taking surface sputtering and a redistribution of oxide atoms during implantation into account, a nearly constant total Si content throughout the oxide can be expected (symbols). For Si HD implantation, the incorporation of additional Si in SiO_2 causes a considerable fluence dependent oxide swelling, which corresponds to a broadening of the oxygen signal in the RBS spectra in Fig. 15 (see Ref. 40 for details). A three-dimensional KLMC simulation was used to simulate the redistribution of excess Si and the formation of Si NCs from a SiO_x layer ($x<2$) during annealing.[21,41] For the simulation the initial configuration was deduced from the calculated TRIDYN Si data LD (Fig. 14), which leads to a cross-section image as shown in Fig. 16(a). With increasing simulation (or annealing) time, Si monomers bundle to precipitates mainly in the upper half of the oxide and grow to NCs later on. Despite considerable mixing of the Si/SiO_2 interface during implantation (see Fig. 14), a flat interface between the oxide and the Si substrate reconstructs during annealing. From Gibbs–Thompson's rule, assuming the Si substrate as a crystal of infinite radius, the equilibrium concentration of Si monomers around the embedded Si NCs in oxide is higher than directly above the Si substrate, leading to a diffusion of Si monomers from the NCs toward the Si substrate. Some Si NCs located closer to the substrate dissolve, whereas those in the upper oxide region ripen. This behavior is confirmed by the redistribution of oxygen during annealing in the RBS spectra in Fig. 15 for Si HD implantation. The development of a small valley and a little hump in the oxygen profile corresponds to a formation of Si NCs next to the oxide center and a formation of a region denuded by Si NCs close to the Si/SiO_2 interface, respectively. Such a denuded zone exists also in the case of Ge implantation. There, contrary to the Si implantation case, the small Si precipitates close to the Si/SiO_2 interface [see Fig. 16(b)] caused by the interface mixing are stabilized by the flux of Ge monomers from the oxide center toward the Si substrate.[19] Thus, in Figs. 9 and 10 the size of the denuded zone corresponds to d_{tox1}, which increases with annealing time.[14]

For the present Si implanted samples Si NCs of 2–4 nm size were detected mainly about the oxide center using HR- and EFTEM in Figs. 17 and 18. As predicted by KLMC simulation, actually a denuded oxide zone separates the Si NCs from the Si substrate, but, in contradiction, the amount of remaining excess Si forming NCs is much lower than

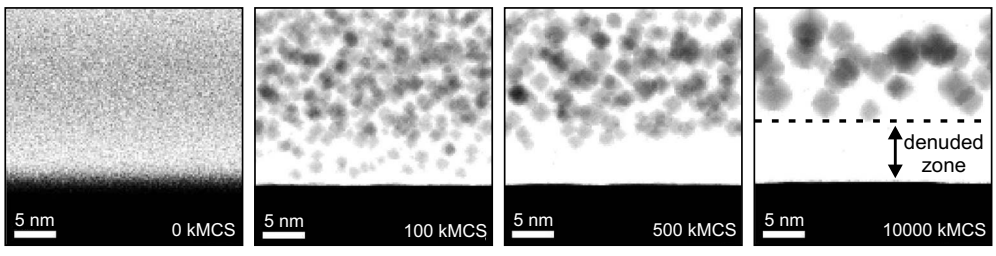

FIG. 16. Cross-section presentation of a KLMC simulation for the Si LD implanted gate oxide. The initial distribution of Si excess atoms is deduced from TRIDYN calculations in Fig. 14. With proceeding simulation/annealing time (increasing MC steps) the formation and ripening of Si NCs in the oxide can be traced leading to reconstruction of a flat Si/SiO_2 interface, which is finally separated to the NCs by a denuded zone.

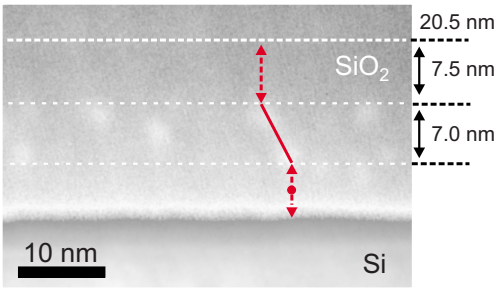

FIG. 17. (Color online) Cross-section EFTEM micrograph for the Si LD implanted sample annealed at 1050 °C for 30 s. Some small Si NCs ($\leq$2 nm) are visible by bright spots mainly in the oxide center enclosed by two oxide regions denuded of NCs toward the oxide surface and the Si substrate. By conventional HR bright field TEM imaging, these tiny Si NCs were not detectable. A red line indicates a localized charge transfer through the oxide across a small portion of NCs.

expected. However, in the simulation a loss of excess Si from sample handling and annealing after ion implantation was not included.[19,42] When a damaged thin gate oxide is exposed to humid air after implantation, moisture (e.g., O_2 and H_2O) penetrates the porous oxide, which leads—together with residual oxygen from the annealing ambient—to a significant reduction in Si available for NC formation due to oxidation of excess Si. Most sensitive to penetrating oxidants, in the experiment a NC-free region (3–7 nm) forms close to the oxide surface (see Figs. 17 and 18), similar to a passivation of bare Si surfaces. This oxide layer can be considered as an efficient top-oxide barrier. Assumedly, the denuded zone between the Si NCs and the Si substrate has not that quality. As shown in Fig. 16(b) incorporated Si precipitates possibly remain in this layer during annealing and enable a considerable charge conduction

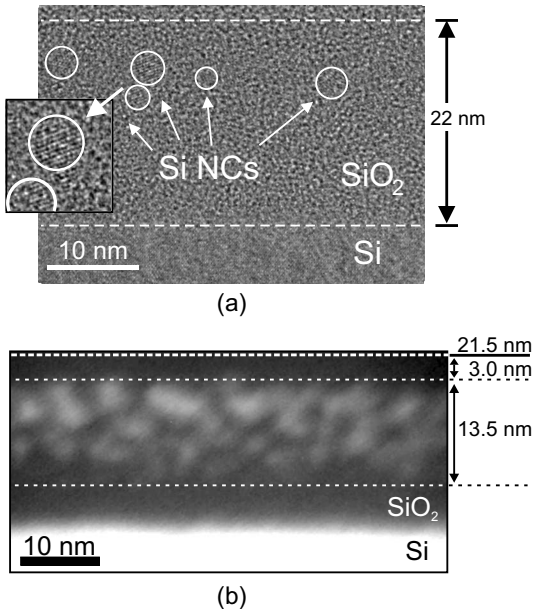

FIG. 18. Cross-section TEM micrographs of a Si HD implanted sample annealed at 1050 °C for 30 s obtained (a) at high resolution bright field conditions and (b)—enabling a much more detailed view on the NC distribution—by EF imaging. In (a) at the top region of the oxide layer Si NCs formed with the evidence of Si (111) lattice fringes. About two-thirds of the oxide is filled with Si NCs, visible by bright spots, in a high density, and enclosed by two oxide regions denuded of NCs.

TABLE V. Structural parameters used in the calculation of the *I-V* characteristics in Fig. 6 for the Si^+ implanted oxides (LD and HD) and for the unimplanted reference (virgin). Oxide and NC layer sizes are in nanometer.

Fluence	Curve	d_{tox1}	d_{nc1}	d_{tox2}	d_{nc2}	d_{top}	d_{ox}
LD	A	2.0	1.0	2.5	7.0	7.5	20.0
HD	B	1.8	1.0	2.0	13.5	3.0	21.3
⋯	C	⋯	⋯	⋯	⋯	⋯	20.7
(LD)	D	⋯	⋯	⋯	⋯	⋯	7.5
(HD)	E	⋯	⋯	⋯	⋯	⋯	3.0

through this oxide zone similar to a trap-like conduction. Thus, the respective structural parameters needed for the *I-V* characteristic calculations are deduced from Figs. 17 and 18 and summarized in Table V. Within the denuded zone a traplike state is considered in d_{nc1} of 1 nm size, dividing the denuded zone into the sections d_{tox1} and d_{tox2}.

B. *C-V* hysteresis of Si NC containing gate oxides

In *C-V* hysteresis measurements a sweep amplitude higher than 7.5 V (LD) or 2.5 V (HD) has to be applied to show a considerable charging of the Si implanted oxides (see Fig. 19). Positive and negative charges are generated or trapped in the oxide applying negative and positive gate voltages, respectively. Thus, a dominating charge exchange between the Si NCs and the Si substrate can be considered. Whereas the hysteresis increases with increasing gate voltage above a threshold value nearly symmetrically in Fig. 19(a) (LD fluence), the flat-band voltage shift saturates for the Si HD implantation at a comparably low level. This limitation indicates re-emission of trapped electrons toward the gate or compensation of stored holes by electrons injected from the gate. Best observable in the difference of the maximum capacitance values C_{max} comparing Figs. 19(a) and 19(b), the content of remaining nonoxidized Si merged into Si NCs is much higher for the higher Si fluence. As a consequence the actual oxide dielectric constant changes from $\varepsilon_{ox}=3.9\varepsilon_0$ (virgin oxide) to effectively about $4.35\varepsilon_0$ for the Si HD implanted sample ($\varepsilon_{Si}=11.8\varepsilon_0$). For the lower Si fluence, oxide

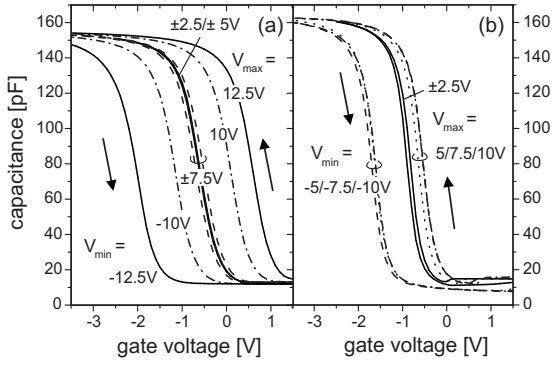

FIG. 19. *C-V* hysteresis characteristics for the Si LD (a) and HD (b) implanted gate oxides annealed at 1050 °C for 120 and 30 s, respectively (the complemental samples show similar charging behavior). Sweep direction is $V_{min} \rightarrow V_{max} \rightarrow V_{min}$ for $\pm$2.5 V/$\pm$5 V/$\pm$7.5 V/$\pm$10 V/($\pm$12.5 V). Using quasistatic and conductance *C-V* methods (not shown) at midgap, a Si/SiO_2 interface trap density of $D_{it} \lesssim 1\times10^{11}$ cm^{-2} eV^{-1} was obtained indicating a sufficient reconstruction of the Si/SiO_2 interface for both fluences.

growth (e.g., by oxidation) compensates the effect of remaining excess Si in the oxide ($C_{max} \approx \varepsilon_{ox}/d_{ox}$) as C_{max} is similar to the virgin oxide (not shown).

C. *I-V* characteristics for the Si implanted oxides

For the Si ion implanted and annealed oxides, the currents increase rapidly already above $|V_{gate}| \approx 2$ V (HD) or $|V_{gate}| \approx 5$ V (LD) as shown in Fig. 6. Below this voltage the current level is similar to the virgin oxide without significant enhancements, which coincidences with the missing *C-V* hysteresis is this regime (Fig. 19). Apparently, on the contrary to the characteristics for the Ge implanted oxides (Figs. 4 and 5), the charging does not affect homogenously large area portions. Considerable charge trapping occurs only at high currents (Fig. 6), e.g., at ±12.5 V (LD) or ±5.0 V (HD) bias, as confirmed by the *C-V* hysteresis measurements in Fig. 19. However the obtained V_{fb} shift is five to ten times lower than for the Ge implanted oxides. Changes in the *I-V* characteristic with increasing annealing time are of minor relevance. At high current densities ($J > 1 \times 10^{-6}$ A/cm^2), the slopes weaken only slightly in the semilogarithmic plot.

Apparently, for the present Si implanted samples the charging occurs not rather homogenously across a high density of NCs close to the Si substrate, as in the case of Ge containing gate oxides, but across rare defects or traps located in the denuded zone as indicated in Fig. 17. Figure 16(b) shows a considerably high density of such Si precipitates in this region, which disappear bit by bit during further annealing/simulation time. Thus, in a first approximation, the current through the gate oxide for Si implanted oxides J_{Si} occurs locally across about 1% of the MOS capacitor area. However, the transient enhanced model as derived in Ref. 13 is only valid for rather homogenously charged oxides. Thus, Eqs. (1)–(8) were used to calculate the current only at the involved areas with $R_{nc1}=R_{nc2}=1$ and $J_{Si}=0.01J_{tot}$ [Eq. (2)]. A band gap energy of 1.4 eV (Ref. 36) for about 3 nm tiny Si NCs leads to a tunneling barrier of about 3.0 eV for electron ejection from Si NCs.[13] With these assumptions and the structural data from Table V, the calculated *I-V* characteristics show significant agreements, qualitatively and quantitatively, with the measurements. Again, the onset of the high current regions in Fig. 6 coincidences with the characteristics related to MOS capacitors containing only the top-oxide layer d_{top}.

VI. CHARGE STORAGE IN GE AND SI NC CONTAINING OXIDES

For the embedded Ge NCs initially large programming windows are obtained (about 8 V) in Fig. 20, which decay within the first seconds to a more stable state holding about 1 V for more than minutes. Thus, two different charge loss mechanisms can be considered: The first loss (short term storage) is considerably attributed to a spontaneous reemission of electrons (or holes) from the NCs band edges toward the Si substrate. Also injection of holes (or electrons) from the substrate side has to be taken into account leading to a charge compensation in the NCs. A different backtunneling barrier height for electrons and holes ($\phi_{b,e} < \phi_{b,h}$)

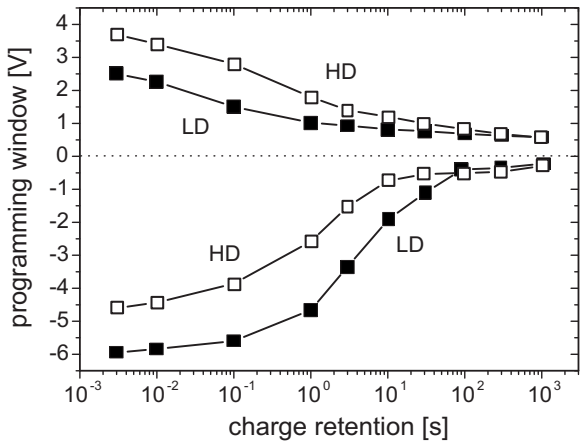

FIG. 20. Retention data for Ge implanted oxides for both fluences, LD and HD, after programming pulses of ±8 V applied for 100 ms. The programming window reflects the difference of the actual $V_{fb}(t)$ to the initial (uncharged) state with the positive and negative voltage branch indicating storage of electrons and holes, respectively.

(or, alternatively, a shorter generation time of holes than of electrons from a *p*-Si substrate) causes slightly different time scales of charge decay. Capture of electrons at self-interstitial defect sites located at or in the Ge NCs (Ref. 43) might be responsible for the long term storage as well as the different relative band gap position of the Ge NCs in comparison to the Si substrate (hole storage).[13]

On the contrary to the Ge implanted samples, stored electrons and holes hold in the present Si NC containing structures at least for hours as shown in Fig. 21. According to the presented model of charge conduction, the rare small traps embedded in the denuded zone between the NCs and the Si substrate limit efficiently the loss toward the substrate electrode. From extrapolations quasinonvolatility up to real nonvolatility can be predicted depending on the implanted Si ion fluence. For the Si LD implanted sample the programmed and the erased states should be distinguishable from each other up to days and months ($>10^6$ s) even if this device has been previously treated with 10^5 write/erase cycles. Especially for the Si LD sample, device cycling wid-

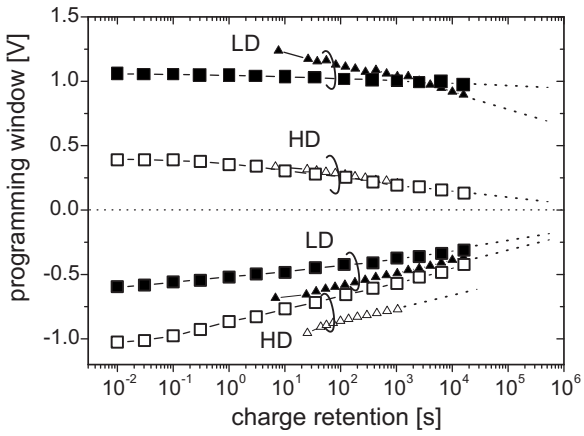

FIG. 21. Charge retention characteristics for the Si implanted samples (LD and HD with filled and open symbols, respectively), representing the behavior after 10 (squares) and 10^5 (triangles) write/erase cycles after applied voltage pulses of ±12.5 V (LD) and ±5 V (HD) for 100 ms.

ens slightly the programming windows with the consequence of an increased charge decay with retention time. During cycling at high electrical fields and high current stress needed in the write/erase operations, oxide traps are generated, which mediate a charge transfer toward the NCs but enable also a faster escape of charges from the NCs toward the substrate or gate electrode.

VII. SUMMARY

An electrical model has been developed to describe current-voltage characteristics for thin NC containing gate oxides. IBS of Ge and Si NCs in SiO_2 leads to different spatial distributions, varying from narrow NC layers close to the Si substrate to broad layers spanning around the oxide center. From these structural data current-voltage characteristics were calculated, which show significant qualitative and quantitative agreements with measurements, considering significant charging of the NCs. Oxide layers denuded of NCs, which form self-organizing during annealing, work efficiently as charge tunneling barriers. Thus, ion implantation induced oxide traps are not responsible for the charge transfer through the oxide. However, in some cases a trap-assisted conduction is proposed between the Si substrate and the NC layers or between NCs. Monte Carlo simulations reveal that these traps might evolve from dissolving Si (or Ge) precipitates in the oxide close to the Si/SiO_2 interface, for instance. Ion profile calculations related to NC synthesis in thin gate oxides are not suitable to predict the final NC distribution since also redistribution and oxidation effects have to be taken into account. The obtained charge retention in the NC containing gate oxides spans from seconds or minutes (Ge NCs) to the perspectives of quasinonvolatility (Si NCs) with a charge retention of months or more depending on the number of performed write/erase cycles before measurement.

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