Microelectronic Engineering 193 (2018) 1–6

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Shallow Si N + P junction diodes realized via molecular monolayer doping

Astha Tapriya [a], Brian Novak [a], Scott Williams [b], Santosh Kurinec [a,*]

[a] Department of Electrical and Microelectronic Engineering, Rochester Institute of Technology, Rochester, NY 14623, USA
[b] School of Chemistry, Rochester Institute of Technology, Rochester, NY 14623, USA

ARTICLE INFO

Article history:
Received 30 November 2017
Received in revised form 29 January 2018
Accepted 5 February 2018
Available online 6 February 2018

Keywords:
Monolayer doping
Ultra shallow junctions
Unified diode model

ABSTRACT

A conformal and controlled semiconductor doping is needed for applications in next generation nanoscale devices, low contact resistivity metal semiconductor junctions such as selective emitters in solar cells. Molecular monolayer doping (MLD) in silicon is a novel technique based on the formation of self-assembled monolayer of dopant – containing molecules on surface of crystalline silicon, followed by rapid thermal anneal. The technique is capable of forming ultra-shallow junctions with high atomic accuracy and minimum defects in silicon. A container and process was developed which successfully doped 6 in. diameter silicon wafers using MLD for the in-house CMOS fabrication facility. The phosphorus monolayer is grafted on hydrogen terminated p-type silicon followed by rapid thermal anneal. Average sheet resistance ~670 Ω/sq. and junction depth ~25 nm are achieved. N + P junctions are fabricated using MLD and current-voltage characteristics are measured and analyzed using unified diode model.

1. Introduction

As device dimensions shrink and move from planar to three-dimensional structures, low junction depths and conformal doping profiles are desired. The industry has relied on ion implantation to push the boundary of semiconductor doping, however effects such as transient enhanced diffusion caused by lattice damaged have impeded the creation of the desired ultra-shallow junctions [1–3]. The uniformity and control over the dose of the dopants is compromised when using solid source diffusion. Use of spin on dopant results in the formation of 'skin' that needs to be etched. Therefore, there is a need for well-defined, uniform nanoscale dopings in advanced Si structures such as nanoscale MOSFETS, FinFETs and shallow emitters for photovoltaic devices and bipolar junction transistors (BJT). There have been tremendous efforts in recent years to develop new technologies for introducing dopants in the semiconductor with minimum damage and ability to form shallow junctions. Molecular Monolayer Doping (MLD) is one such technique, which involves the formation of a self-assembled monolayer on the surface of hydrogen-terminated silicon by forming covalent bonds between dopant containing chemistry and silicon [4–6]. The dopants are diffused into the semiconductor by thermal treatment. The covalent bonds formed at the surface help to control the dopant dose. The technique results in high atomic accuracy, minimum defects, and no crystalline damage.

A diffusion profile is characterized in terms of two main parameters – sheet resistance, R_s and junction depth, x_j. It is important to realize complete dopant activation. For a given dose, shallower junctions have higher sheet resistance. Fig. 1 shows R_s-x_j map of data reported in literature using different approaches [1]. These include ion implantation (I/I) followed by ultra-short anneals (spike, flash, rapid thermal). The target values desired in the ITRS (International Technology Roadmap for Semiconductors) [7] are also shown in Fig. 1.

Successful FinFETs have been demonstrated using MLD for source and drain junctions with sub-5 nm junction depth with an abruptness of 0.6 nm/dec [6]. However, diode characteristics of MLD created junctions are not reported. In this paper, authors have investigated MLD created N + P diodes for considering their applications in realizing shallow emitters and for lowering the contact resistivity of metal semiconductor junctions.

2. Experimental

P-type (100) silicon substrate with resistivity of 5–10 Ω cm was used for MLD doping of phosphorus. Fig. 2 shows the schematic of the MLD process flow. The native oxide from the surface of silicon was etched using 1% HF to form hydrogen terminated silicon surface, which was then immediately transferred in dopant containing chemistry. The n-type phosphorus dopant source diethyl 1-propylphosphonate (DPP) was mixed with solvent mesitylene in ratio 1:25 v/v. The dopant-containing adsorbate usually contains alkene or alkyne but DPP lacks that

* Corresponding author.
E-mail address: skkemc@rit.edu (S. Kurinec).

https://doi.org/10.1016/j.mee.2018.02.008
0167-9317/

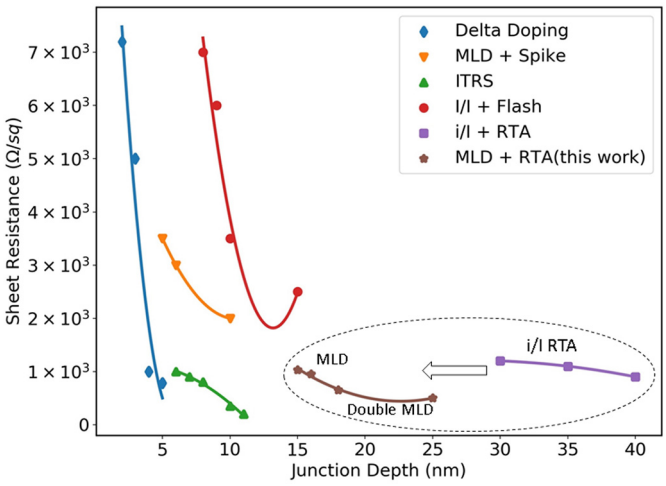

Fig. 1. Sheet resistance versus junction depth for various doping techniques. Here depth refers to the distance from the surface at which the doping density falls to 10^{18} cm^{-3}.

and still has demonstrated to function as phosphorus source. It seems plausible that DPP forms monolayer using adsorption on the surface of hydrogen terminated silicon. The samples were reacted with DPP and mesitylene for 2.5 h at 170 °C. After the reaction was completed the chemistry was left to cool down. The samples were cleaned using toluene, acetone, methanol and DI water in the given order to remove any physisorbed material on the surface of silicon.

The chemistry preparation and reaction was carried out in a controlled inert environment. The setup to carry out the reaction had following requirements - high temperature to increase the reaction rate; reflux system to condense evaporated chemistry; and inert environment to ensure no oxygen is in the system to react with silicon. The most important aspect of this system is the design of the reflux condenser. It serves to bring argon into and out of the test tube, which keeps the ambient above the mixture inert. Secondly, it is wrapped with a jacket for cold water to flow through (Fig. 3). This allows for any vapors from the mixture to be condensed back, keeping the solution in a steady state.

The samples were capped with 50 nm of SiO_2 (tetraethyl orthosilicate TEOS) using plasma enhanced chemical vapor deposition (PECVD). The capping layer ensures that there is no loss of the dopant molecules into surrounding during anneal. The dopants were thermally

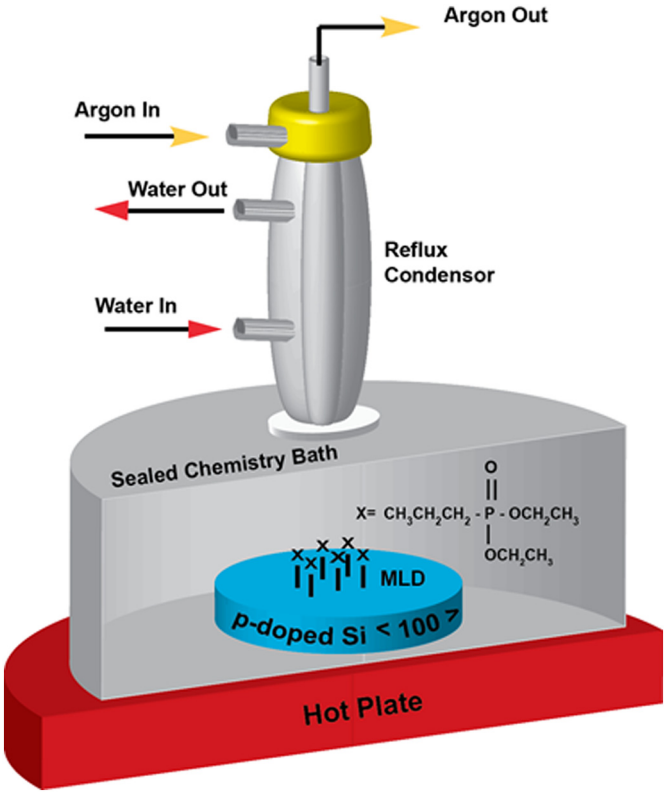

Fig. 3. Schematic diagram of phosphorus MLD process set up.

diffused using rapid thermal annealing (RTA) followed by etching of capping oxide using buffered oxide etch (BOE). Since the dose is limited by the dopant adsorption, multiple MLD steps may be performed. We carried out second MLD after removing the capping oxide followed by the same anneal.

Diode and transmission line measurement (TLM) structures were fabricated using photolithography, etch, deposition and thermal processes as depicted in Fig. 4. The predefined levels for photolithography were MESA isolation, contact cut and metal. The N+ region was formed on p type silicon using MLD process followed by MESA isolation and contact cut lithography using SiO_2 as the insulating oxide. Nickel with 7 nm thickness was sputter deposited using a Perkins Elmer 4400 RF

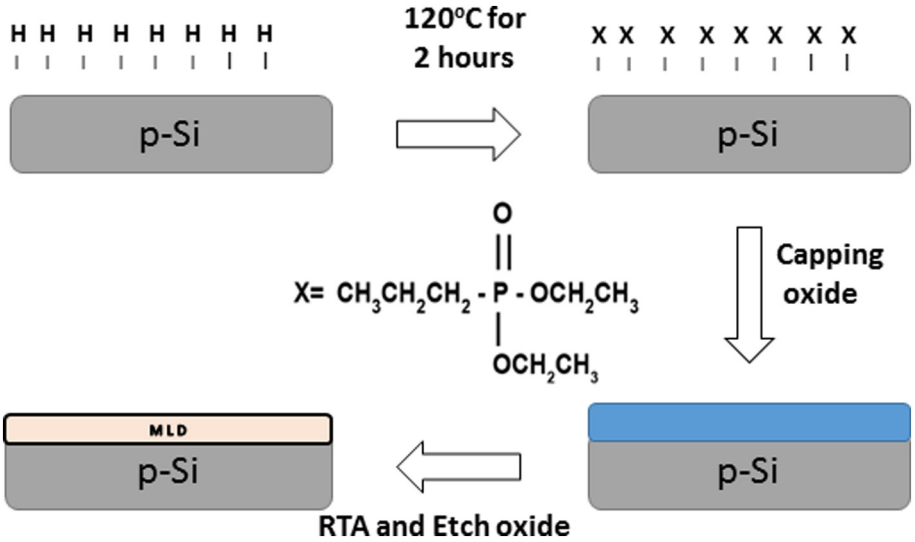

Fig. 2. Schematic showing the monolayer doping (MLD) process.

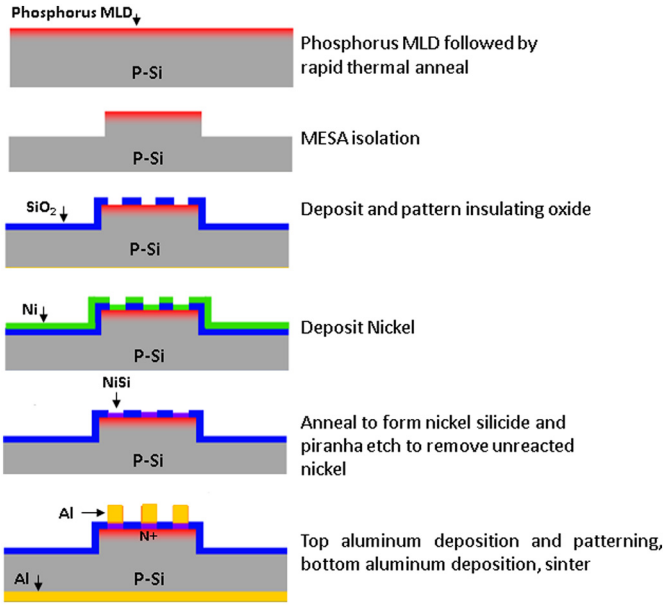

Fig. 4. Process flow for diode and TLM structure fabrication.

sputter system equipped with 200 mm diameter Ni target at 500 W power and 800 mTorr argon pressure. The Ni thickness was confirmed by X-ray reflectometry measurements [8]. A rapid thermal anneal at 550 °C for 1 min in nitrogen to form nickel silicide was performed. The unreacted nickel was etched using piranha solution at 90 °C. It is reported that Ni forms a low resistivity phase NiSi at this condition. Ni was kept thin to minimize Si consumption while forming a low resistivity contact and barrier for aluminum, which tends to spike through the silicon. The aluminum metal was sputter deposited followed by lithography, etch and sinter at 400 C in forming gas.

3. Results and discussion

3.1. Elemental analysis

The surface of monolayer sample was characterized using X-ray photoelectron spectroscopy (XPS) for presence of phosphorus on the surface of silicon. The samples were analyzed after the reaction between DPP and hydrogen terminated silicon. Silicon carbide, silicon and silicon dioxide were detected as seen in Fig. 5. The phosphorus peak is observed at 131.5 eV binding energy. The carbon to phosphorus ratio is 6:1 similar to ratio of these elements present in DPP.

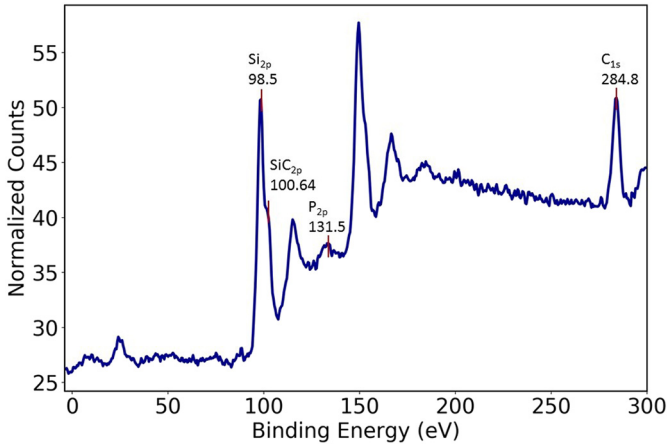

Fig. 5. X-Ray photoelectron spectroscopy of phosphorus MLD silicon sample.

Secondary ion mass spectroscopy (SIMS) measurement was used to characterize the doping profile of a sample that was subjected to phosphorus MLD twice and is shown in Fig. 6. The surface concentration is 5.6×10^{21} cm^{-3} that sharply decreases to 10^{18} cm^{-3} at 26 nm depth. The peak ~10 nm is due to the first MLD and the profile also shows characteristic kink and tail feature due to concentration dependent diffusivity of phosphorus observed in conventional doping techniques as well [9].

The dose is calculated from the area under the curve, which gives a value close to 1×10^{15} cm^{-2}. This is quite close to the theoretical maximum for full adsorption on (100) silicon surface having a bond density of 6.78×10^{14} cm^{-2}. With double MLD the expected dose ideally should be twice this value.

3.2. Electrical analysis

The sheet resistance was measured using 4-point probe (CDE Resmap tool). Fig. 7 shows the effect of annealing conditions on the sheet resistance. The sheet resistance is very high due to the incomplete activation of phosphorus for 900 C anneals, whereas at higher temperature and longer diffusion time the junction depth and activation both increase, thus decreasing the sheet resistance value. Similar experimental results were reported by Ho et al. [4].

For subsequent processing in this study, 1000 C for 5 min RTA was used for each MLD step for device fabrication. The average sheet resistance of 1130 Ω/sq. was obtained using single MLD which reduced to an average value of 670 Ω/sq. for double MLD. A contour map of sheet resistance across the double MLD doped 6 in. diameter wafer is shown in Fig. 8. An average sheet resistance of 670 Ω/sq. with standard deviation of 4% was achieved. Sheet resistance was also measured using transmission line measurements, which also give the specific contact resistivity of the metal-n + Si contacts.

Fig. 9 shows the TLM structure schematic and a data set of a typical test. Four-probe method (passing current through two probes and measuring voltage across the other two probes and extracting resistance from the I-V data) was used to determine resistance between the pads that eliminated the probe contact resistance. Resistance was then plotted versus pad spacing as shown in Fig. 9, which plots one such measurement for a pad width of 160 μm. Sheet resistance determined from the TLM measurements on a number of die locations across the wafer is obtained as 612 ± 81 Ω/sq., The specific contact resistivity of Al/NiSi-n + Si contact obtained from the transfer length is ~2.85 $\times 10^{-5} \pm 2.00 \times 10^{-5}$ Ω cm^2. The error observed in the measurement is typical. Error in the TLM method can be classified into two main types - random error and systematic error. Random error measures the difference between the mean determined from a large number of trials and a single measurement of the parameter in consideration. Systematic error is a consistent shift of means of a parameter that cannot be reduced by taking a large number of trials [10]. The sheet resistance obtained from the TLM measurements is not very different from the 4-point measurements. The observed difference may be attributed to the probe penetration and spacing effects [11].

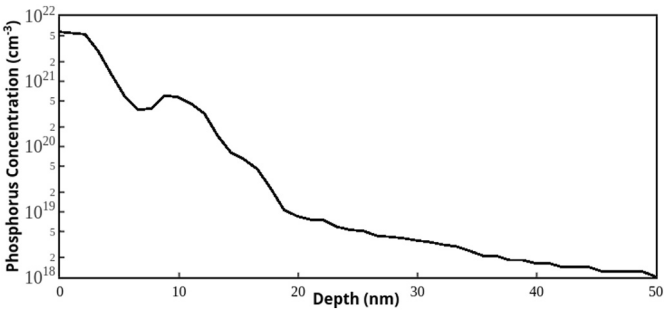

Fig. 6. Phosphorus concentration versus depth profile in double MLD sample using SIMS.

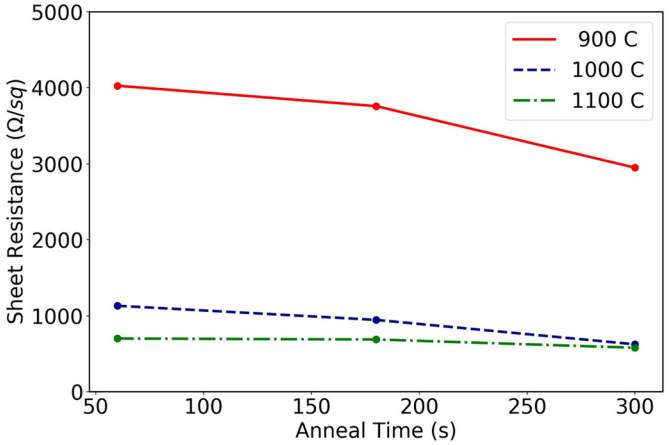

Fig. 7. Sheet resistance versus anneal time and temperature.

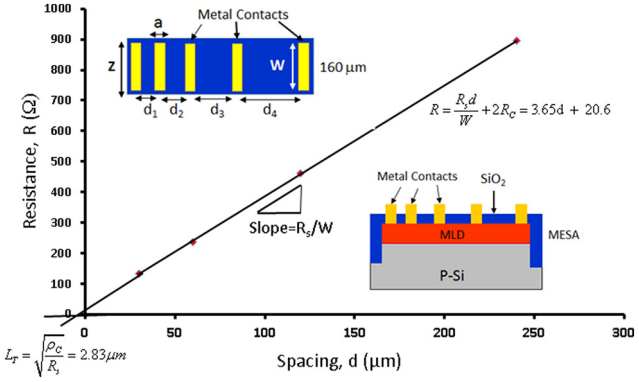

Fig. 9. TLM measurements using the structures shown in the insets (top and side views).

Diode J-V characteristics were obtained using HP4145 semiconductor parameter analyzer. The forward and reverse bias current density versus voltage characteristics of diodes in different die location is shown in Fig. 10. The diode area of the n + contact was 118 μm × 120 μm whereas the backside of the substrate was used as the P side contact.

Diodes exhibit consistent J-V curves in the neutral region, however, variations in leakage and space charge recombination current and parasitic resistance are observed. In reverse bias, it is observed that the current changes slowly with the voltage. The depletion region current increases with the reverse bias, which follows an approximate $-V^{1/2}$ relationship.

The diode parameters are extracted showing three distinct regions (Fig. 11). First region is due to the dominance of the space charge recombinations with an ideality factor close to two and is also affected by shunt leakage. The second region is that of an ideal diode; the current should increase one order magnitude when voltage is increased by 60 mV. We observe 90 mV giving an ideality factor of 1.5. This is due to the series resistance effect.

Unlike the TLM measurements, diode J-V measurement is a two-probe measurement and sensitive to probe contact. This variation is attributed to the probe-pad contact and substrate contact to the chuck. A minimum parasitic resistance of 264 Ω was determined from the linear part of the J-V curve as shown in Fig. 11. This value of resistance is expected since it includes the spreading resistance of a small contact on a semiconductor substrate. According to the Cox-Strack method [12], the resistance of a contact of area πa^2 on a substrate of thickness t is given by

$$R = R_C + R_{SPR} + R_B = \frac{\rho_C}{\pi a^2} + \frac{\rho}{2\pi a}\tan^{-1}\left(\frac{2t}{a}\right) + R_B \quad (1)$$

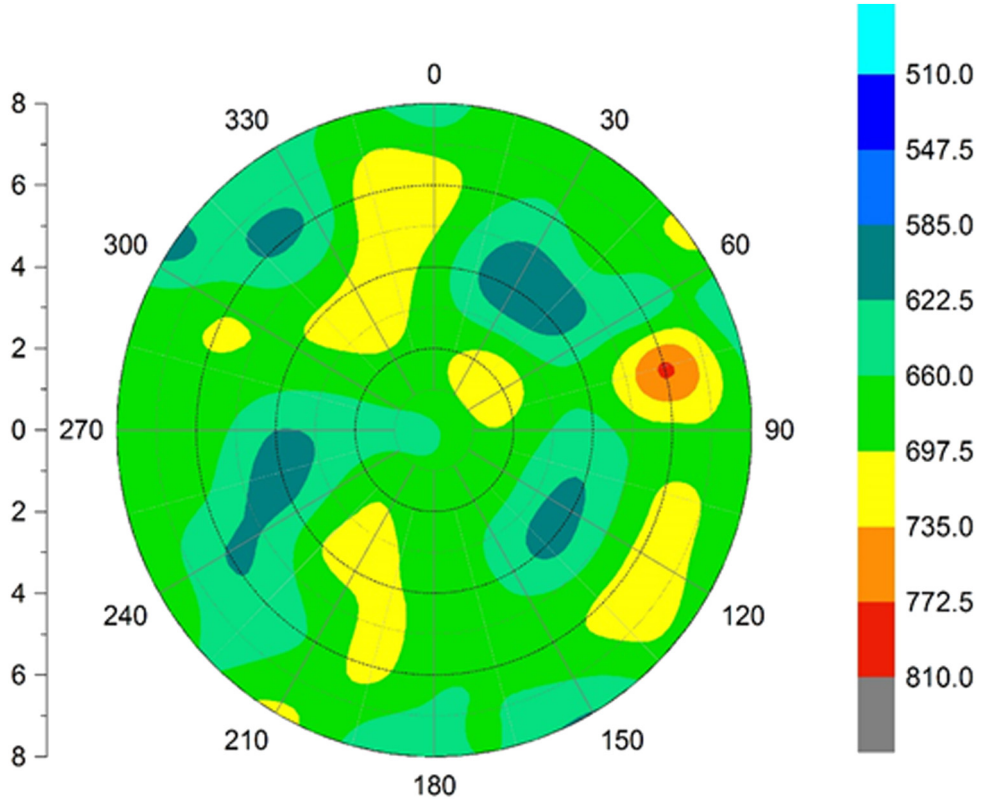

Fig. 8. Sheet resistance contour map on a MLD doped 6-inch diameter wafer.

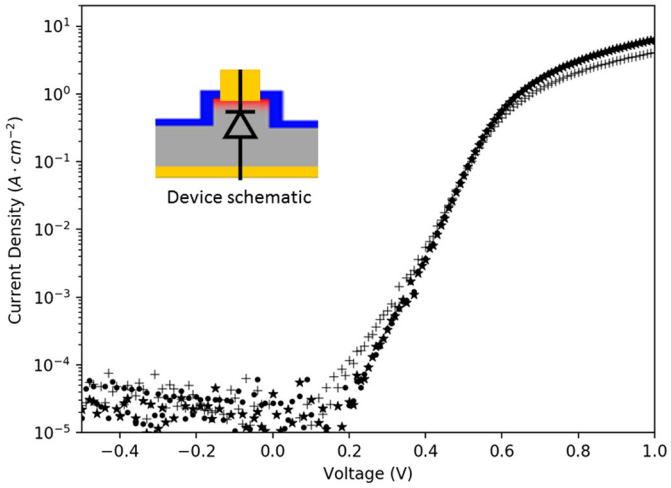

Fig. 10. J-V characteristics of diodes in different die locations.

where R_C is the contact resistance, R_{SPR} is the spreading resistance and R_B is the back contact/probe resistance. ρ_C is the specific contact resistivity and ρ is the substrate resistivity. With a value of ρ_C for Al/NiSi/n + silicon contact of ~3×10^{-5} Ω cm^2 measured, most of the contribution to resistance comes from the spreading and back contact resistance. For a wafer of thickness $t = 625$ μm, R_{SPR} ~ 250 Ω close to the extracted value of 264 Ω. The difference is attributed to the back contact of the wafer with the chuck of the probe station.

High injection level effects and series resistance dominate in the third region. With the substrate doping of 1.9×10^{15} cm^{-3}, onset of high-level injection happens when injected minority carrier concentration at the edge of the space charge region (in P side) is equal to the majority carrier concentration. This gives a value of this voltage, $V_{hl} = 0.63$ V.

The generalized equation of J-V characteristics of a one sided N + P long diode using unified model is given in Eq. (2) [13]. It takes into account the high-level injection region and series resistance.

$$J = \frac{qn_i x_p}{2\tau_n}\left(1-\frac{V}{V_{bi}}\right)^{1/2}\left[\exp\left(\frac{qV}{2kT}\right)-1\right] + \frac{qD_n}{L_n}\left[\sqrt{2n_i^2\left(\exp\left(\frac{q(V-AJR)}{kT}\right)-1\right)+N_A^2}-N_A\right] \quad (2)$$

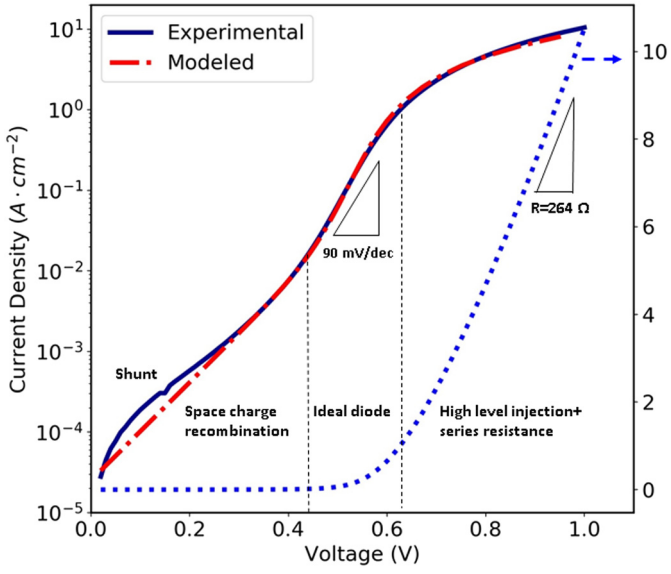

Fig. 11. J-V characteristics of the diode with parasitic resistance of 264 Ω, extracted from the linear J-V plot at resistive region.

Table 1
Parameters used in diode calculations.

Temperature, T, °K	300
Intrinsic carrier concentration, n_i, cm^{-3}	10^{10}
Substrate doping, N_A, cm^{-3}	1.9×10^{15}
Diode area, A, cm^2	1.416×10^{-4}
Electron diffusion coefficient, D_n, cm^2 s^{-1}	35
Minority carrier lifetime, τ_n, *sec*	1.63×10^{-7} fitting parameter

The J-V characteristics using unified model were calculated using Eq. (2), with the series resistance of 264 Ω. The parameters and their values used in calculations are provided in Table 1. The calculated values are compared with the experimental data in Fig. 11. The minority carrier lifetime (τ_n) is calculated ~0.16 μs in the substrate that fits the experimental data. This value is very close to the specified value of the starting wafer showing that MLD did not cause minority carrier lifetime degradation.

4. Conclusions

Monolayer doping of phosphorus has been carried out in a laboratory run process to create ultra-shallow junctions in six-inch diameter p type silicon substrates. To the best of the authors' knowledge, electrical results on diodes have been reported for the first time in this work. Sheet resistance in the range of 500–800 Ω/sq. with a junction depth (at 1×10^{18} cm^{-3}) in the range of 20–30 nm is reported. The forward diode characteristics clearly show the three distinct regions–depletion region recombinations, quasi-neutral region recombinations and high level/series resistance region. Specific contact resistivity of Al/NiSi/n + Si of the order of 10^{-5} Ω cm^2 is achieved making it an attractive process for forming selective emitters.

Acknowledgements

The authors acknowledge Dr. Michael Pierce, School of Chemistry & Materials Science, Rochester Institute of Technology for XPS support and Dr. David Young of National Renewable Energy Laboratory (NREL), Golden, Colorado for help in SIMS measurements. Special thanks are due to Dr. Miron Cristea, Politehnica University of Bucharest for application of the unified diode model in our calculations.

References

[1] Craig M. Polley, Warrick R. Clarke, Jill A. Miwa, Giordano Scappucci, Justin W. Wells, David L. Jaeger, Maia R. Bischof, Richard F. Reidy, Brian P. Gorman, Michelle Simmons, Exploring the limits of N-type ultra-shallow junction formation, ACS Nano 7 (6) (2013) 5499–5505.
[2] P.S. Peercy, The drive to miniaturization, Nature 406 (2000) 1023–1026.
[3] E. Vogel, Technology and metrology of new electronic, materials and devices, Nat. Nanotechnol. 2 (2007) 25–32, https://doi.org/10.1038/nnano.2006.142.
[4] Johnny C. Ho, Roie Yerushalmi, Gregory Smith, Prashant Majhi, Joseph Bennett, Jeffri Halim, Vladimir N. Faifer, Ali Javey, Wafer-scale, sub-5 nm junction formation by monolayer doping and conventional spike annealing, Nano Lett. 9 (2) (2009) 725–730, https://doi.org/10.1021/nl8032526.
[5] Johnny C. Ho, Roie Yerushalmi, Zachery A. Jacobson, Zhiyong Fan, Robert L. Alley, Ali Javey, Controlled nanoscale doping of semiconductors via molecular monolayers, Nat. Mater. 7 (1) (2007) 62–67, https://doi.org/10.1038/nmat2058.
[6] I. Ok, K.-W. Ang, C. Hobbs, R.H. Baek, C.Y. Kang, J. Snow, P. Nunan, S. Nadahara, P.D. Kirsch, R. Jammy, Conformal, low-damage shallow junction technology (Xj ~ 5 nm) with optimized contacts for FinFETs as a solution beyond 14 nm node, 12th International Workshop on Junction Technology, 2012, https://doi.org/10.1109/iwjt.2012.6212804.
[7] Semiconductor Industry Association, International Technology Roadmap for SemiconductorsTable FEP12; available at http://www.itrs.net 2011.
[8] A. Marshall, K. Florent, A. Tapriya, B.G. Lee, S.K. Kurinec, D.L. Young, Nickel silicide metallization for passivated tunneling contacts for silicon solar cells, 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR 2016, pp. 2479–2482, https://doi.org/10.1109/PVSC.2016.7750089.
[9] W. Scotten, Jones, Diffusion in Silicon, IC Knowledge LLC, April 25, 2008.

[10] Sidhant Grover, Effect of Transmission Line Measurement (TLM) Geometry on Specific Contact Resistivity Determination, Rochester Institute of Technology, 2016 Thesis. Accessed from http://scholarworks.rit.edu/theses/9343.
[11] Robert J. Hillard, Robert G. Mazur, William J. Alexander, C. Win Ye, Mark C. Benjamin, John O. Borland, Measurements of ultra-shallow junction (USJ) sheet resistance with a non-penetrating four point probe, MRS Online Proceeding Library Archive, January, 2011https://doi.org/10.1557/PROC-810-C11.6.
[12] R.H. Cox, H. Strack, Ohmic contacts for GaAs devices, Solid State Electron. 10 (1967) 1213–1218.
[13] Miron Cristea, Unified model for p-n junction current-voltage characteristics, Open Eng. 1 (2011)https://doi.org/10.2478/s13531-011-0006-9.