Microelectronic Engineering 85 (2008) 2256–2260

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Analysis of electrical characteristics of Au/SiO_2/n-Si (MOS) capacitors using the high–low frequency capacitance and conductance methods

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ARTICLE INFO

Article history:
Received 7 April 2008
Accepted 6 July 2008
Available online 12 July 2008

Keywords:
MOS capacitor
Surface potential
Interface states
High–low frequency capacitance method
Conductance method

ABSTRACT

The purpose of this paper is to analyze electrical characteristics in Au/SiO_2/n-Si (MOS) capacitors by using the high–low frequency (C_{HF}–C_{LF}) capacitance and conductance methods. The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements have been carried out in the frequency range of 1 kHz–10 MHz and bias voltage range of (−12 V) to (12 V) at room temperature. It was found that both C and G/ω of the MOS capacitor were quite sensitive to frequency at relatively low frequencies, and decrease with increasing frequency. The increase in capacitance especially at low frequencies is resulting from the presence of interface states at Si/SiO_2 interface. Therefore, the interfacial states can more easily follow an ac signal at low frequencies, consequently, which contributes to the improvement of electrical properties of MOS capacitor. The interface states density (N_{ss}) have been determined by taking into account the surface potential as a function of applied bias. The energy density distribution profile of N_{ss} was obtained from C_{HF}–C_{LF} capacitance method and gives a peak at about the mid-gap of Si. In addition, the high frequency (1 MHz) capacitance and conductance values measured under both reverse and forward bias have been corrected for the effect of series resistance (R_s) to obtain the real capacitance of MOS capacitors. The frequency dependent C–V and G/ω–V characteristics confirm that the N_{ss} and R_s of the MOS capacitors are important parameters that strongly influence the electrical properties of MOS capacitors.

1. Introduction

The elementary structure used in the majority of electronic devices and modern semiconductor technology is the metal-oxide-semiconductor (MOS) structures. The performance of the MOS structures is strongly affected by the presence of oxide layer at metal/semiconductor (M/S) interface and interface states located at the semiconductor/oxide interface. Interface states at the Si/SiO_2 interface have been still investigated and have attracted much attention their effects on the reliability and quality of MOS structures [1–8]. However, satisfactory understanding of all details has still not been achieved. In real MOS structures, the localized interface states exist at the Si/SiO_2 interface and the device behavior is different from an ideal case due to the presence of these localized interface states. The reason for their existence is the interruption of the periodic lattice structure at the surface, surface preparation, formation of insulator layer and impurity concentration of semiconductor [9–13].

Since the interface state capacitance (excess capacitance) depends on strongly on the frequency and applied bias voltage, the C–V and G/ω–V characteristics are strongly affected [1–3]. Therefore, it is important to include the effect of frequency and applied bias voltage in the investigation of electrical characteristics of MOS or MIS structures. Capacitance–voltage (C–V) and conductance–voltage (G/ω–V) techniques are widely used for the electrical characterization of the $Si/Si0_2$ interface in MOS structures. Useful parameters such as oxide thickness, flatband and mid-gap voltages and, in particular, the interface states can be extracted from a simple capacitor structure. The interface states usually cause a bias shift and frequency dispersion of the C–V and G/ω–V curves [1,2]. The measurement techniques for determining the interface state density such as the classical quasi-static (QS) capacitance–voltage (CV) [5], surface admittance [13], the high–low frequency (C_{HF}–C_{LF}) capacitance [10–12] and conductance techniques have been developed and among them the more important ones are high–low frequency capacitance and conductance technique [14].

High–low frequency capacitance method, as developed by Kar and Dahlke [10], the interface state density is extracted from its capacitance contribution to the measured C–V curve. In the equivalent circuit of MOS capacitor, the oxide capacitance (C_{ox}) is in series with the parallel combination of the interface capacitance (C_{it}) and the depletion (space charge) layer capacitance (C_{sc}). Because interface states do not follow high frequencies in inversion and depletion region, the measured high frequency capacitance in this region do not contain interface state capacitance. The interface state capacitance can be determined by subtracting the depletion layer capacitance (extracted from the measured high frequency

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0167-9317/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2008.07.001

capacitance C_{HF}) from the depletion layer capacitance in parallel with the interface state capacitance (extracted from the measured low frequency capacitance C_{LF}). However, the conductance method, as developed by Nicollian and Goetzberger [3] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and the majority carrier band of the semiconductor when a small ac signal is applied to the MOS capacitor.

In the present study, we have investigated the experimental frequency and voltage dependent of the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of Au/SiO_2/n-Si (MOS) capacitor by considering the interface state density (N_{ss}) and series resistance (R_s) effects. The energy density distribution profile of N_{ss} was obtained from the high–low frequency (C_{HF}–C_{LF}) capacitance methods. The capacitance and conductance measurements of the structure have been carried out in the frequency range of 1 kHz–10 MHz and at room temperature.

2. Experimental detail

The Au/SiO_2/n-Si (MOS) capacitors used in this study were fabricated using n-type (P-doped) single crystals silicon wafer with <1 1 1> surface orientation having thickness of 280 μm, 2" diameter and 1 Ω cm resistivity. For the fabrication process, Si wafer was degreased in organic solvent of $CHCICCl_2$, CH_3COCH_3 and CH_3OH, etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionised water for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ-cm. Immediately after surface cleaning, to form ohmic contacts on the back surface of the Si wafer, high purity gold (Au) metal (99.999%) with a thickness of ~2000 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer in the pressure of $\sim 2 \times 10^{-6}$ Torr in vacuum pump system and the evaporated Au was sintered. The oxidations are carried out in a resistance-heated furnace in dry oxygen with a flow rate of a 1.5 lt/min and the oxide layer thickness is grown at the temperatures of 900 °C during 2 h. To form the Schottky contacts, the circular dots of ~2 mm diameter and ~2000 Å thick Au are deposited onto the oxidized surface of the wafer for through a metal shadow mask in a liquid nitrogen trapped vacuum system in a vacuum of $\sim 2 \times 10^{-6}$ Torr. The interfacial oxide layer thickness was estimated to be about 500 Å from high frequency (1 MHz) measurement of the interface oxide capacitance in the strong accumulation region for MOS structure [1,2].

The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements were carried out using a HP 4192A LF impedance analyzer (5 Hz–13 MHz). The C–V and G/ω–V characteristics of Au/SiO_2/n-Si (MOS) capacitors were measured in the frequency range of 1 kHz–10 MHz at room temperature. A low-distortion oscillator generated the ac signal with the amplitude attenuated to 50 mV_{rms} to meet the small signal requirement for oxide capacitors [2]. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Result and discussion

Several experimental methods have been developed for the study of the semiconductor/oxide (Si/SiO_2) interface states essentially based on differential capacitance measurement [1,2,4,21]. Among these methods, the high–low frequency (C_{HF}–C_{LF}) capacitance method comes from the fact it permits determination of many properties of the insulating interface layer, the semiconductor substrate, and interface easily. In this method [4,11,15,16], the interface state density is extracted from its capacitance contribution to the measured experimental capacitance–voltage (C–V) curve. In the equivalent circuit of MOS capacitor, the oxide capacitance C_{ox} is in series with the parallel combination of the interface state capacitance C_{it} and the space charge capacitance C_{sc}: The interface state capacitance C_{it} can be determined by subtracting the space charge capacitance C_{sc} (extracted from the measured high frequency capacitance C_{HF}) from the space charge capacitance in parallel with the interface state capacitance (extracted from the measured low frequency capacitance C_{LF}) and is given as

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_{sc} \tag{1}$$

At high frequencies, surface states cannot respond to the ac excitation, so they do not contribute to the total capacitance directly, but stretch out of the C–V curve occurs. Therefore, the equivalent capacitance is the series connection of oxide capacitance C_{ox} and space charge capacitance C_{sc}, is given as

$$C_{HF} = \frac{C_{sc}C_i}{C_{sc} + C_i} \tag{2}$$

Thus, combining Eqs. (1) and (2), the interface state density N_{ss} is calculated from [11,12]

$$qAN_{ss} = C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right]^{-1} \tag{3}$$

This integration is performed numerically from the flat band to strong accumulation and to strong inversion as in [5]. For the MOS capacitor with an oxide layer thickness of 500 Å determined from oxide capacitance C_{ox}. The measured high–low frequency curves are shown in Fig. 1. In the high frequency, the N_{ss} cannot follow the ac signal and consequently do not contribute appreciably to the MOS capacitance. This situation may be different at low and intermediate frequencies, depending on the relaxation time and of N_{ss} and the frequency of the ac signal [17]. The high-frequency capacitance of the semiconductor portion of MOS capacitor in the depletion or inversion state is given approximately by the capacitance of a plane-parallel condenser whose thickness is the width of the depletion layer. In this case, because the change in charge corresponding to an infinitesimal change in surface potential consists only of majority carriers (electrons) at the edges of the depletion layer, the change in electric field within the depletion layer is constant.

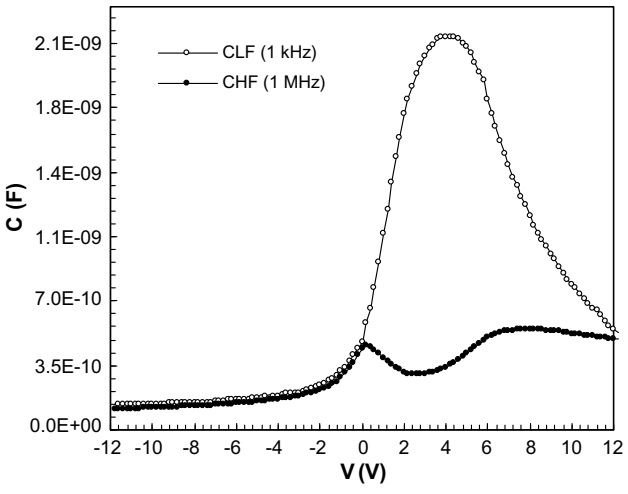

Fig. 1. The measured high–low frequency (C_{HF}–C_{LF}) capacitance plots of the MOS capacitor at room temperature.

Surface potential versus applied voltage for the MOS capacitor is shown in Fig. 2. The energy position in the n-Si band gap is calculated as

$$E_c - E_{ss} = q(\varphi_s - \phi_F) \quad (4)$$

where ϕ_F is the position of Fermi energy level [$\phi_F = \frac{kT}{q}\ln(N_C/N_D)$].

The surface potential as a function of bias is found from the numerical integration of the lowest measurable frequency capacitance–voltage curve according to [5]

$$\Psi_s = \int_{V_a}^{V_i} [1 - C_{LF}/C_{ox}]dV_G + \Psi^* \quad (5)$$

where V_a is the bias voltage in strong accumulation when the capacitance is equal to the oxide capacitance C_{ox} and the integration constant Ψ^* was found by extrapolating the $C_{sc}^{-2} - \Psi_s$ curve in the depletion region (0.28 eV) to $C_{sc}^{-2} = 0$ [2,5,18–20]. Thus, the density of interface states distribution profiles of the sample was obtained from the high–low capacitance measurements is shown in Fig. 3. As can be seen in Fig. 3, the interface states distribution profiles over accessible band-gap energy gives a peaked structure about at mid-gap energy of Si.

Fig. 4a and b shows the measured C–V and G/ω–V characteristics of Au/SiO_2/n-Si (MOS) capacitor, respectively. The applied voltage range was between −12 V and +12 V. The three regimes of accumulation, depletion and inversion are clearly shown for each ac frequency, verifying a typical MOS behavior. It is shown that there is the significantly larger frequency dispersion in C–V and G/ω–V curves, indicating existence of interface states that are in thermal equilibrium with the semiconductor and cannot communicate with the metal. Usually, at the semiconductor/oxide (Si/SiO_2) interface there are various kinds of states with different lifetimes. If the C–V or G/ω–V measurements are carried out at very high frequency (ω) such that carrier lifetime (τ) is much larger than $1/\omega$ the charge at the interface states cannot follow an ac signal [17].

In addition, the C–V characteristic of the Au/SiO_2/n-Si capacitor in Fig. 4a consists of two peaks. The first peak located at low forward bias region due to the N_{ss} contribution shifts from the high forward bias voltage to the low bias voltage as increasing frequency. However, the second peak shown at high bias disappears when the frequency decreases. This behavior of second peak is due to the influence of the series resistance, R_s. The values of both two peaks increase with increasing frequency

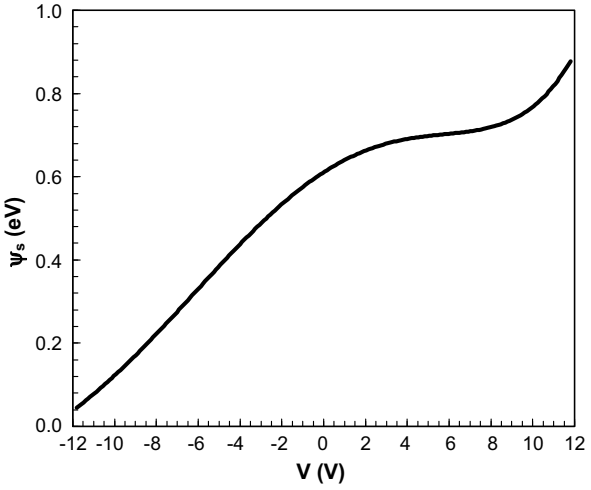

Fig. 2. The surface potential vs gate bias plot of the MOS capacitor at room temperature.

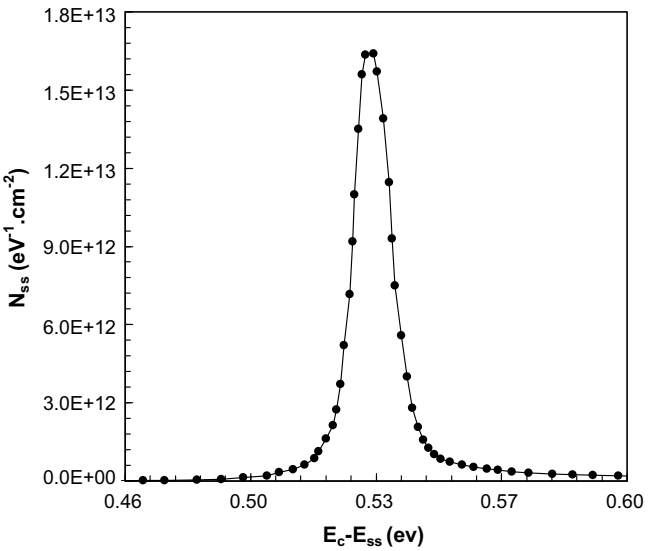

Fig. 3. The density of interface states distribution profiles of the MOS capacitor at room temperature.

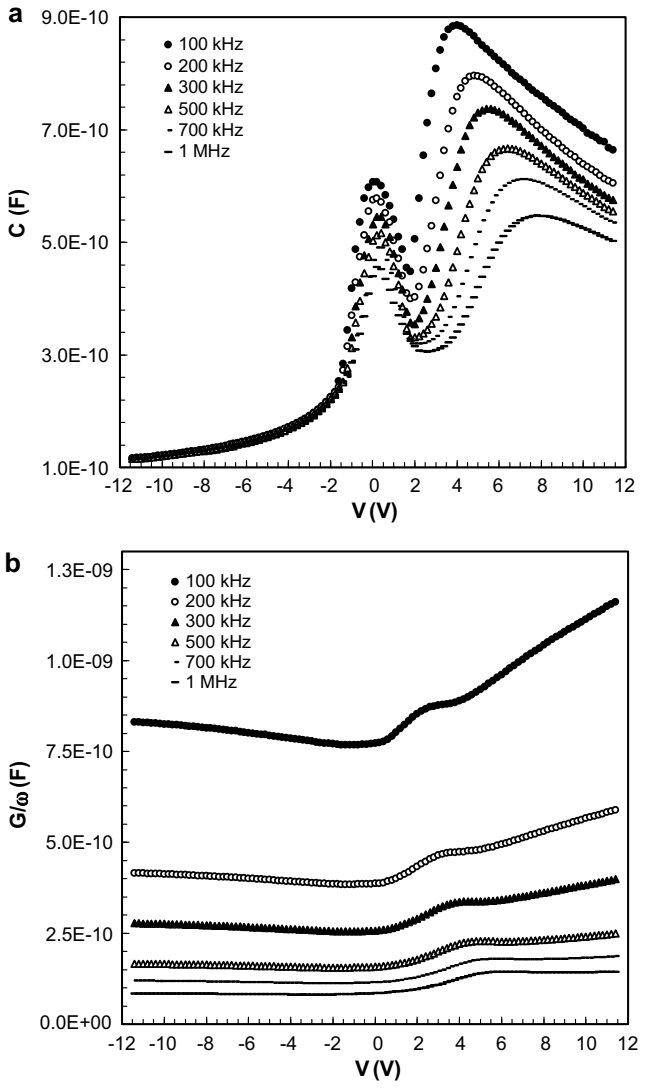

Fig. 4. (a,b) The measured C–V and G/ω–V characteristics of MOS capacitor, respectively, measured at various frequencies at room temperature.

and while the first peak located at low biases shift towards the accumulation region the second peak towards the inversion region [21–24]. Similar results have been reported in the literature [22,25–28] both experimentally and theoretically. Among them Green et al. [25] have reported frequency dependent an anomalous peak in the forward bias C–V characteristics at depletion region. The origin of this peak has been ascribed to N_{ss} by Ho et al. [26]. However, Werner et al. [27] and Bati et al. [28] have shown that the observed peak in the forward bias C–V curves is due to R_s. On the other hand, Chattopadhyay et al. [22] have shown theoretically that the peak value of the C–V curves of MIS Schottky diodes varies with both N_{ss} and R_s.

The real series resistance (R_s) of MOS structures can be determined from the measured capacitance (C_{ma}) and conductance (G_{ma}) in strong accumulation region at high frequency ($f \geqslant 500$ kHz) [2,3,9,24,29]. The measured impedance (Z_{ma}) at strong accumulation of MOS structure using the parallel RC circuit [2,22] is equivalent to the total circuit impedance as

$$Z_{ma} = \frac{1}{G_{ma} + j\omega C_{ma}} \tag{6}$$

Comparing the real and imaginary part of the impedance, the series resistance is given by [2,30]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \tag{7}$$

The voltage dependent series resistance profile of MOS capacitor is calculated from measured C–V and G/ω–V measurements according to Eq. (7) and shown in Fig. 5 for various frequencies. These very significant values demanded that special attention be given to effects of the series resistance in the application of the admittance-based measured methods (C–V and G/ω–V). As can be seen in Fig. 5, the series resistance gives a peak depending on frequency in the bias voltage range about 1.5 V to 3 V. These peaks move to strong accumulation region with decreasing frequency. It is clearly seen that the series resistance is almost independent of the voltage above 500 kHz.

The corrected capacitance (C_c) and corrected equivalent parallel conductance (G_c) values of the MOS structures corrected for series resistance are obtained as a function of angular frequency from the direct measured C_m and G_m according to

$$C_c = \frac{[G_m^2 + (\omega C_m)^2]C_m}{a^2 + (\omega C_m)^2} \tag{8}$$

and

$$G_c = \frac{[G_m^2 + (\omega C_m)^2]\,a}{a^2 + (\omega C_m)^2} \tag{9}$$

where $a = G_m - [G_m^2 + (\omega C_m)^2]R_s$.

To obtain the real diode capacitance C_c and conductance G_c/ω, the high frequency capacitance measured under forward and reverse bias was corrected for the effect of series resistance using Eq. (8) and (9), respectively. When the correction was made on the C–V plot for the effect of series resistance, the values of the corrected capacitance increased with increasing voltage, especially under forward bias, as seen in Fig. 6a. As seen from Fig. 6b, the plot of the corrected conductance gives a peak, proving that the charge transfer can take place through the interface.

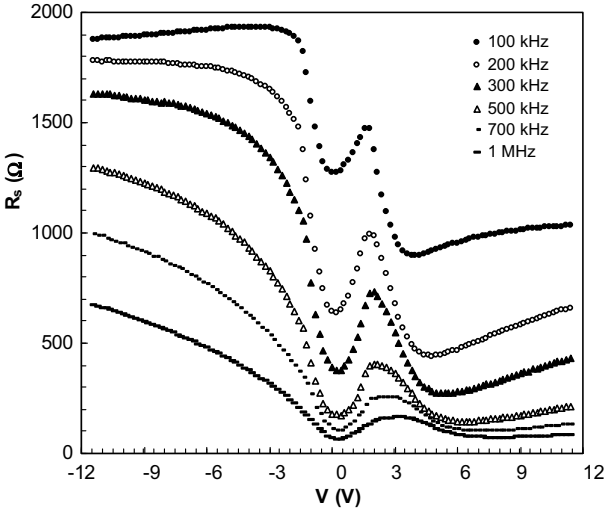

Fig. 5. The variation of the series resistance as a function of voltage for various frequencies at room temperature.

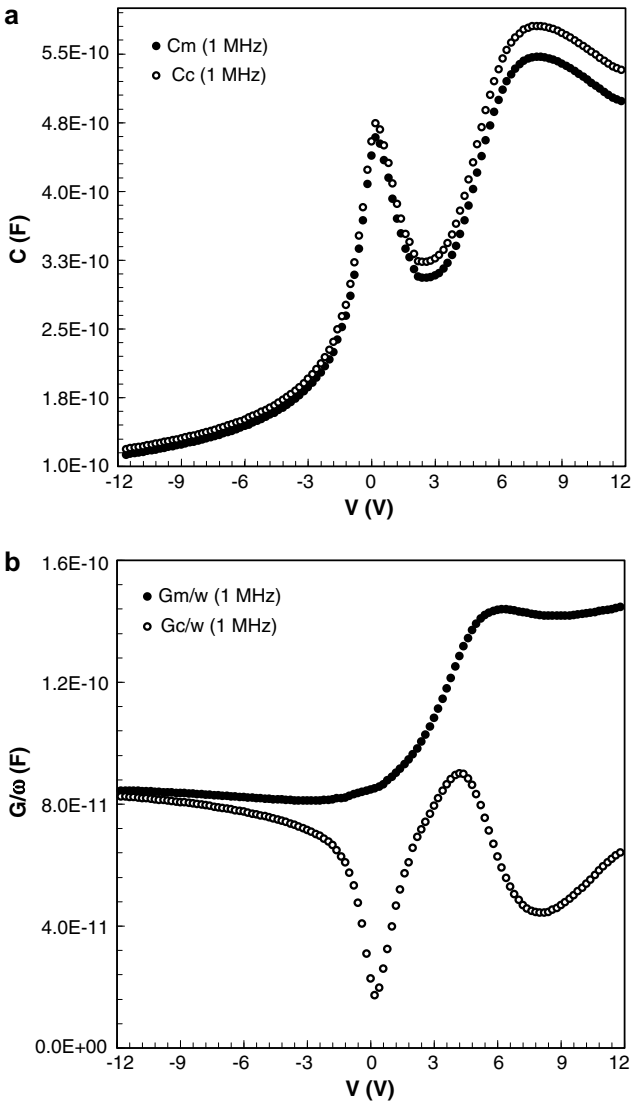

Fig. 6. The voltage dependent plots of the corrected (a) the high frequency (1 MHz) capacitance and (b) conductance curves at room temperature.

4. Conclusion

The electrical properties of the $Au/SiO_2/n$-Si capacitors have been investigated by using the forward and reverse bias C–V and G/ω–V characteristics in the frequency range of 1 kHz–10 MHz at room temperature. The experimental results confirmed that both the measured C and G/ω varies with applied voltage and frequency, and decreases with increasing frequency in depletion and accumulation region due to a continuous distribution of interface states between Si/SiO_2 interface and series resistance of MOS capacitors, respectively. The interface states density (N_{ss}) have been determined by taking into account the surface potential as a function of applied bias obtained from the lowest measurable frequency C–V curve. The energy density distribution profile was obtained from the high–low frequency (C_{HF}–C_{LF}) capacitance method and gives a peak over accessible band-gap energy of Si. Also, the C–V and G/ω–V curves of MOS capacitor show a dependence of series resistance and therefore the measured capacitance (C_m) and conductance (G_m) at high frequency were corrected for the effect of series resistance. In summary, the C–V and G/ω–V characteristics confirm that the R_s and N_{ss} are useful quantity for correcting non-ideal electrical properties of MOS structures. It is clear that ignoring the R_s and N_{ss} can lead to significant errors in the C–V and G/ω–V characteristics.

Acknowledgments

This work is supported by Turkish of Prime Ministry State Planning Organization Project Number 2001K120590, Gazi University Scientific Research Project (BAB), FEF-Research Project FEF 05/2008-19 and FEF 05/2008-23.

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