Photoluminescence intensity modulation by charge carrier injection in silicon nanocrystals at room temperature

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Hysteretic intensity modulation of the photoluminescence (PL) of silicon nanocrystals (Si-NCs) embedded in silicon oxide (SiO_2) is observed in metal-oxide-semiconductor (MOS) structures at room temperature during gate voltage sweeps of ± 3 V. This PL intensity modulation is correlated with simultaneous current density measurements in the different operating regimes of these MOS devices. In particular, PL intensity enhancement is shown to result from electron injection into the oxide. The different mobilities of the charge carriers in SiO_2 and the competing effects of charge trapping in the Si-NC and the surrounding oxide defects are used to explain the observed PL modulation. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3067864]

Since the discovery of photoluminescence from porous silicon in 1990,[1] silicon nanostructures— and especially silicon nanocrystals (Si-NCs)—have been extensively studied due to their high potential for optoelectronic devices. The emitted photoluminescence (PL) spectrum can be modulated either statically (e.g., by selecting Si-NC mean size and spatial distribution during fabrication[2]) or dynamically (e.g., by applying an external electric field[3,4]). In the latter case, some modulation effects (wavelength shifts and intensity fluctuations) have been observed in structures such as porous silicon,[5–10] CdSe NCs,[11] and Si-NC embedded in relatively thick silicon oxide (SiO_2) layers[12,13] or submitted to low temperatures.[13,14] The use of Si-NC submitted to external electric field in devices such as optical memories[15,16] and solar cells[17] is also considered.

In this article, Si-NC PL modulation is investigated at room temperature by biasing metal-oxide-semiconductor (MOS) structures in which Si-NC are embedded in a thin ($\sim$50 nm) SiO_2 layer. This thin oxide layer allows current to flow even at low gate voltages V_G ($-3\ \text{V} < V_G < 3\ \text{V}$). The effect of the dominant oxide layer charge carrier (electrons or holes) on the Si-NC PL is evaluated by studying MOS structures produced from two differently doped Si substrates (*n*-Si and *p*-Si). A qualitative model based on MOS dynamics is presented to interpret the PL modulation as a function of oxide layer bias.

The studied MOS diodes were obtained from the dry oxidation of *n*-Si (3 Ω cm) and *p*-Si (10 Ω cm) substrates, yielding SiO_2 layers with thicknesses of 57 nm on the *n*-Si substrate (sample A) and 46 nm on the *p*-Si substrate (sample B), as determined by ellipsometry. Both oxides were implanted at a fluence of 2.5×10^{16} cm^{-2} with a 25 keV Si^+ ion beam, followed by a second implantation at a fluence of 1.0×10^{16} cm^{-2} with a 15 keV Si^+ ion beam; the calculated implantation depth profile using the stopping and range of ions in matter (SRIM) software indicates an approximately Gaussian distribution of excess Si with a majority of implanted ions lying in the lower half of the oxide layer between the center of this layer and the Si/SiO_2 interface.[18] These samples were annealed at 1050 °C (sample A) and 1100 °C (sample B) under N_2 ambient for 1 h. Hydrogen passivation was then carried out at 500 °C for 30 min in a forming gas of H_2 (5%) and N_2 (95%). Finally, a 15 nm thick circular semitransparent Au gate electrode was deposited by thermal evaporation on top of the oxides (with a diameter of 2 mm for sample A and 3 mm for sample B), and an Ag back electrode was deposited over the doped Si substrates previously etched with a 5% HF buffered solution, yielding a positive-channel MOS (*p*-MOS) structure for sample A and a negative-channel MOS (*n*-MOS) structure for sample B.

Both samples were photoexcited using a 405 nm laser diode (50 mW) incident at a 45° angle on the Au electrode. The resulting PL emission was collected normal to the surface with a telescope focused on the laser spot and optically coupled to a QE65000 OceanOptics spectrometer. All spectra were acquired with a 15 s integration time and corrected for system response. A spectrum was taken for each direct current (dc) gate voltage applied to the MOS electrodes. The integrals of the acquired spectra in the Si-NC PL region (600–1000 nm) are presented with respect to the applied gate voltage V_G in Figs. 1(a) and 2(a). The electric field strength E is evaluated by the relation $E=V_G/(d\times\varepsilon_{r\text{SiO}_2})$, where d is the oxide thickness and $\varepsilon_{r\text{SiO}_2}$ is the static dielectric constant of the oxide; the latter is calculated by the effective medium approximation using the proper dielectric functions[19] and implantation profiles,[18] yielding average values of $\varepsilon_{r\text{SiO}_2}=8.1$ for sample A and $\varepsilon_{r\text{SiO}_2}=8.3$ for sample B. The simultaneously measured current densities J are also reported as a function of V_G in Figs. 1(b) and 2(b). The theoretical values of the flatband voltage (V_{FB}) and threshold voltage (V_T) were calculated, giving $V_{\text{FB}}=0.7$ V and $V_T=-0.06$ V for sample A and $V_{\text{FB}}=0.08$ V and $V_T=0.8$ V for sample B, as indicated by the dashed lines separating the different MOS operating regimes in Figs. 1 and 2. Finally, the typical (normalized) PL spectra are shown in Fig. 1(c) for sample A and Fig. 2(c) for sample B.

Even though the acquired PL spectra showed no noticeable wavelength shift during successive gate voltage sweeps, small but reproducible integrated PL intensity variations were measured. A plot of these variations as a function of the applied gate voltage V_G following the path ABCD produces

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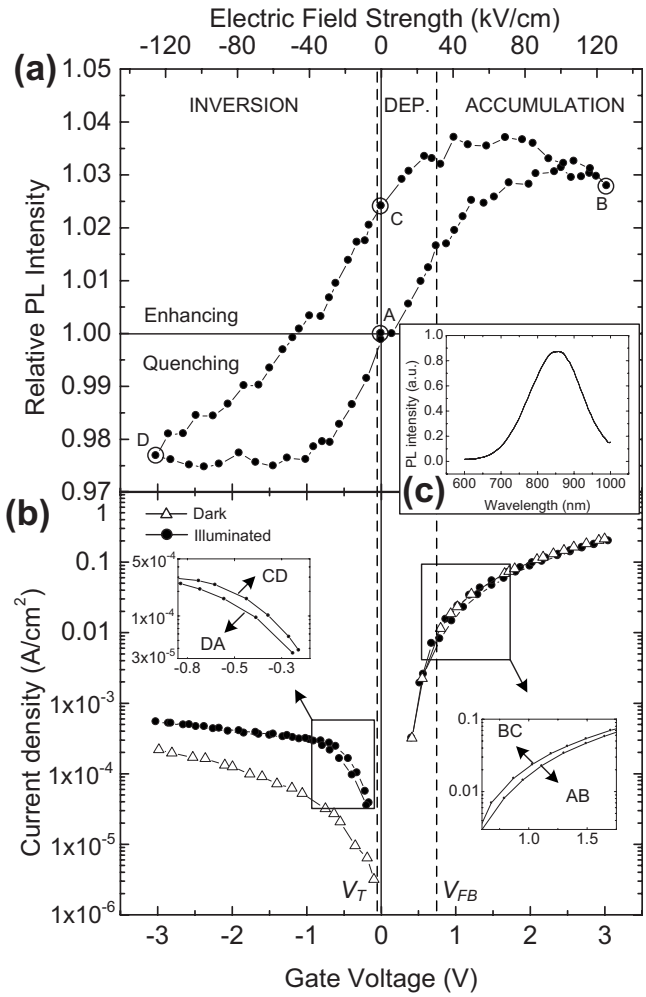

FIG. 1. Relative PL intensity (a) and current density (b) as functions of the applied voltage (and electric field strength) for sample A (*p*-MOS, *n*-Si substrate). The PL spectrum at point A (0 V) is shown in (c). The threshold and flatband voltages are V_T=−0.06 V and V_{FB}=0.7 V, respectively. The insets in (b) show the small current density hysteresis between different paths.

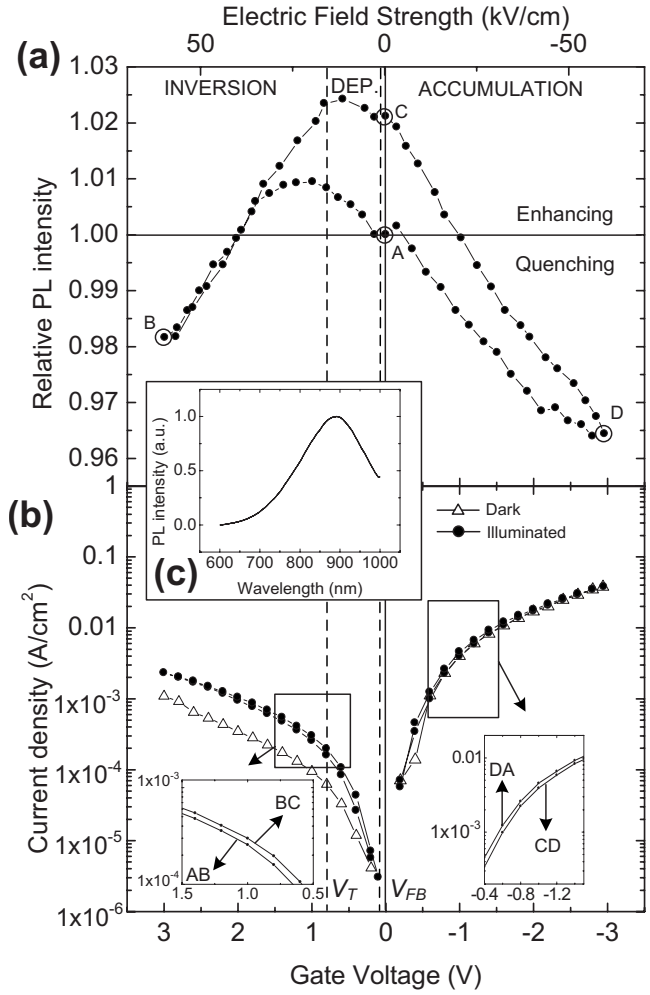

FIG. 2. Relative integrated PL (a) and current density (b) as functions of the applied voltage (and electric field strength) for sample B (*n*-MOS, *p*-Si substrate). The PL spectrum at point A (0 V) is shown in (c). The threshold and flatband voltages are V_T=0.8 V and V_{FB}=0.08 V, respectively. The insets in (b) show the small current density hysteresis between different paths.

the hysteresis curves shown in Figs. 1(a) and 2(a). The absence of wavelength shift in the PL spectra indicates that the applied electric field is too weak to generate the quantum-confined Stark effect at room temperature, which is often invoked to explain PL attenuation,[13] or any NC size-selective PL quenching processes.[12] In the present case, the observed modulations are interpreted to be the result of two different effects related solely to the tunnel transport of charge carriers in the oxide under the effect of the applied electric field: charge carrier trapping and detrapping in nonradiative recombination traps (consisting of structural defects at the Si-NC/SiO_2 interface and in the surrounding oxide)[17] and Si-NC charging resulting in fast Auger nonradiative electron-hole recombination.[16] For the samples used here, the Si-NC density is much greater near the Si/SiO_2 interface than the opposite SiO_2 layer near the Au electrode, as indicated by the Si^+ implantation profile.[18] Consequently, only charge carriers injected through (or extracted from) the Si/SiO_2 interface, having a greatest effect on Si-NC PL, will be considered in our analysis.

During the first part of the PL hysteresis loop (path AB), there is a small but steadily increasing electron injection from the Si substrate to the oxide in the depletion regime for both MOS structures; the electrons are majority charge carriers for sample A and minority carriers for sample B. Due to their relatively high mobility in SiO_2 (μ_e=10–20 $cm^2/V\,s$ in thermal SiO_2 without Si-NC at room temperature[20]), the injected electrons will efficiently start to fill nonradiative recombination traps, resulting in a linear increase in the PL intensity. However, upon reaching the accumulation regime in sample A (inversion regime in sample B), electrons begin to accumulate in the substrate near the Si/SiO_2 interface, enhancing charge injection in the oxide. As a result, an increasing number of Si-NC will be charged, promoting Auger nonradiative recombination, thus acting against electron trapping and eventually leading to PL quenching (at V_G=2.5 V for sample A and V_G=1 V for sample B).

For the path BC, the gradual decrease in V_G first leads to an increase in the PL intensity (until the depletion regime is reached), due to the smaller charge injection in the Si-NC and, consequently, to a lesser NC charging effect. Once in the depletion regime, the negative charge injection from the substrate dramatically decreases and detrapping of electrons in the nonradiative recombination traps (attributed mostly to nonradiative recombination with photogenerated holes)

dominates, giving rise to a linear decrease in PL. A small hysteresis between the current density curves for paths AB and BC is observed, which is attributed, for both samples, to the electron trapping that occurred in the AB path. Also, the flatband voltage V_{FB} of sample A and the threshold voltage V_T of sample B are slightly shifted to higher values in the path BC due to the negative charge ΔQ_n trapped in the oxide in the path AB, as can be seen by the small shift in the onset of the linear PL decrease to higher gate voltage values than the calculated V_{FB} in Fig. 1(a) and V_T in Fig. 2(a).

Path CD, which corresponds to holes injection from the substrate, presents an almost linear decrease in the PL intensity. Since holes have a low mobility in the oxide ($\mu_{h^+} = 10^{-5}$ $cm^2/V\,s$ in thermal SiO_2 without Si-NC at room temperature[20]), the trapping in the oxide surrounding the Si-NC is much less pronounced than in the case of electrons. Injected holes will therefore mostly tunnel between Si-NC, increasing the electron accumulation in the Si-NC, which promotes nonradiative Auger recombination, thus decreasing the PL intensity. At the same time, trapped electrons from paths AB and BC will be untrapped and injected back in the substrate, resulting in further PL quenching.

Finally, for path DA, the PL intensity of sample A exhibits a plateau between $-3\ V < V_G < -1\ V$ and an increase for $-1\ V < V_G < 0\ V$. While the plateau is attributed to a balance between the effects of Si-NC charging by injected holes and hole detrapping by recombination with photogenerated electrons, the increase comes from the threshold voltage V_T shift to lower values due to the positive charge ΔQ_p trapped in the oxide during the path CD, as can be seen by the PL increase onset shift to $V_T \approx -0.9$ V in Fig. 1(a). Consequently, the depletion regime in which electrons from the substrate start to fill the nonradiative recombination traps leads to this linear increase in the PL intensity (as in the beginning of path AB) for $-1\ V < V_G < 0\ V$. The small hysteresis in the *J-U* curves between paths CD and DA is attributed to the transfer of detrapped electrons from the oxide to the substrate, which adds to the current density during path CD. For sample B, the PL intensity increases along path DA due to the dominant effect of the decrease in Si-NC hole charging over trapped holes recombination with photogenerated electrons. In this case, the small hysteresis in the *J-U* curve between paths CD and DA is attributed to the (small) hole trapping occurring in path CD.

In conclusion, PL from Si-NC embedded in SiO_2 layers of *n*-MOS and *p*-MOS structures has been measured at room temperature during low gate voltage sweeps. Resulting PL intensity modulation was correlated with electrons and/or holes exchanges between the Si substrate and the oxide layer in the different MOS operating regimes (inversion, depletion, and accumulation). The large difference between electron and hole mobilities in SiO_2, together with two main competing phenomena occurring during charge transport in the oxide layers containing Si-NC, i.e., nanocrystal charging and charge carriers trapping/detrapping in structural defects at the Si-NC/SiO_2 interface and in the surrounding oxide, is proposed to explain the reproducible hysteretical behavior of the PL intensity with gate voltage variation.

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