Electrical conduction mechanisms of Au/NiO/heavily doped p-type Si memory devices

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The fabrication of memory devices based on the Au/NiO/heavily doped p-type Si (p^+-Si) structures and their current-voltage characteristics were reported. The Au/NiO/p^+-Si devices show hysteresis behavior. The fitting data of the temperature-dependent off-state current–voltage curves demonstrated that the carrier transport mechanism of the Au/NiO/p^+-Si device was attributed to the space change limited conduction. However, the difference between the temperature-dependent on-state currents in the forward-bias and reverse-bias regions was found. The different electrical conduction mechanisms (hopping conduction and Ohmic conduction with metal-like behaviors) were discussed. This phenomenon is related to the different interfacial characteristics between Au/NiO and NiO/p^+-Si. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4871693]

Nowadays, resistive random access memory is one of the most promising candidates for next generation memory devices because of their high-density storage, great scalability, low power operation, and simple metal–oxide–metal structures.[1–14] Recently, reliable and reproducible resistive switching in NiO thin films has been reported.[1–4,14] Calka *et al.* investigated origins of the resistivity change during the forming of NiO based resistive random access memories in a non-destructive way using hard x-ray photoelectron spectroscopy (XPS).[1] They suggested that conduction may occur via defects such as electrons traps and metallic nickel impurities.[1] Chien *et al.* stated that the disproportionation and comproportionation reactions of $3NiO \leftrightarrow Ni + Ni_2O_3$ accounted for the resistive switching of NiO_x.[2] Kinoshtia *et al.* found that the resistance change was suggested to originate in the generation and recovery of defects by the migration of oxygen ions for p-type NiO_x samples.[3] The effect of Ni^{3+} concentration on the resistive switching behaviors of NiO memory devices was researched by Ma *et al.*[4] However, the relationship between the interfacial characteristics and the resistive switching of NiO memory devices is still not clear. Memory devices with a simple sandwich structure [that is, Au/NiO/heavily doped p-type Si (p^+-Si)] were fabricated in this study. For Au/NiO/p^+-Si devices, the resistive switching characteristics are studied using current-voltage (I-V) measurements under various temperature conditions.

Four-inch p^+-Si (100) wafers purchased from Woodruff Tech Company were used in the experiment. Resistivity of p^+-Si wafer is about 0.001 Ω cm. The p^+-Si film thickness was about 525 μm. The p^+-Si samples were cleaned in chemical cleaning solutions of acetone and methanol, rinsed with de-ionized water, and blow-dried with N_2. Next, the p^+-Si sample was chemically etched with a diluted HF solution for 1 min, rinsed with de-ionized water, and blow-dried with N_2 (referred as the as-cleaned p^+-Si). A NiO layer was deposited on the as-cleaned p^+-Si substrate. A NiO layer was also deposited on the as-cleaned glass substrate for obtaining the carrier concentration, mobility, and conduction type from the Hall measurements in the van der Pauw configuration. The electrodes were fabricated by depositing Au metal on the NiO layer through a shadow mask. NiO films were prepared by sol–gel spin coating method. $Ni(CH_3COO)_2{\cdot}4H_2O$ (48.089 g) was dissolved in 50 ml of 2-methoxyethanol. HCl was added to the solution as a stabilizer. The concentration of nickel acetate was 0.5 M. The solution was stirred at 60 °C for an hour and then aged for 24 h at room temperature to obtain the sol–gel. The solution was dropped onto the as-cleaned p^+-Si substrates, which was rotated at 2500 rpm for 30 s. The solution dropped onto Si substrates was dried at 150 °C for 5 min on a hotplate in air, and dried again at 350 °C for 5 min on a hotplate in air. The procedures from coating to drying were repeated ten times. The films were then inserted into a furnace and annealed in air at 400 °C for 60 min. The NiO film thickness was about 360 nm. Then, the electrode was fabricated by depositing Au metal on the NiO layer through a shadow mask. The I–V curves were measured using a Keithley model-4200-SCS semiconductor characterization system. The I–V characteristics of the devices were measured in the temperature range of 300–400 K using a temperature controlled cryostat. According to the Hall measurement at room temperature, the hole concentration and mobility in the NiO film were 7.6×10^{15} cm^{-3} and 1.5 cm^2/V-s, respectively. XPS study is used to determine the chemical bonding and reaction at the NiO/p^+-Si interface.

To discuss and investigate the electrical conduction mechanism for Au/NiO/p^+-Si devices, the forward-bias and reverse-bias I-V curves are measured and compared under various temperature conditions. Figure 1(a) shows the temperature-dependent log (I)-V characteristics of Au/NiO/p^+-Si devices. Figure 1(b) shows the temperature-dependent linear I-V characteristics of Au/NiO/p^+-Si devices. In the forward-bias region, electrons are injected from Au to the NiO layer. In the reverse-bias region, electrons are injected from the p^+-Si layer to the NiO layer. By sweeping the voltage (the measuring loops follow $-10 \rightarrow +10 \rightarrow -10$ V cycles), hysteresis of I-V curve is obtained. This indicates different resistance states [high resistance state (HRS) and

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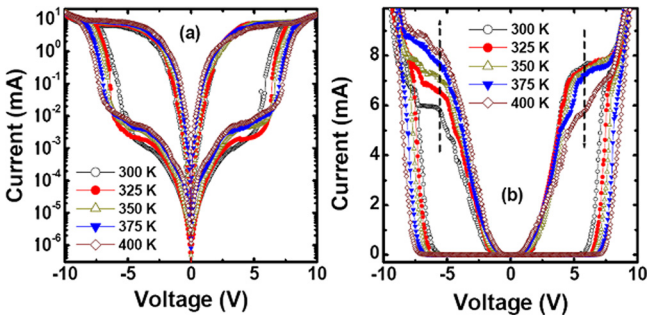

FIG. 1. (a) Log (I)-V curves of Au/NiO/p^+-Si devices as a function of temperature and (b) linear I-V curves of Au/NiO/p^+-Si devices as a function of temperature.

low resistance state (LRS)] occur during the voltage sweeping. The temperature dependence of I-V characteristics both in HRS and LRS was measured to identify the current conduction mechanism in the Au/NiO/p^+-Si structure. To clarify the origin of a resistive switching behavior, the off-state and on-state current conduction mechanisms were investigated. Figure 2 shows the off-state double-logarithmic I-V plots in the forward-bias and reverse-bias regions, respectively. There were no observable changes in the off-state currents in the forward-bias and reverse-bias regions. The slope was nearly constant as 2 (that is, $\eta = 2$ for $I \alpha V^{\eta}$), which represented that the current of HRS in the Au/NiO/p^+-Si devices exhibits the space change limited conduction (SCLC) behavior.[13] However, we found that the on-state current decreases with increasing temperature in the forward-bias region and the on-state current increases with increasing temperature in the reverse-bias region. An interesting observation is found, i.e., a lower on-state current density in the forward-bias region is obtained in a higher temperature. This finding is far different from the normal I-V characteristics of dielectrics in which the higher current density is obtained in a higher temperature. This phenomenon is related to the different interfacial characteristics between Au/NiO and NiO/p^+-Si. The details of this mechanism are discussed later.

To clarify the origin of a resistive switching behavior, the forward-bias on-state current conduction mechanism was investigated. The forward-bias I-V curves of LRS are compared under various temperature conditions. To determine whether the Ohmic conduction dominates the forward-bias LRS behavior for Au/NiO/p^+-Si devices, analysis was conducted according to the equation of $V = IR$ (R is the resistance).[13] This model can be distinguished via the linear I-V correlation.[5,13] Figure 3 shows the forward-bias on-state current of the Au/NiO/p^+-Si device measured within a temperature range from 300 K to 400 K. As can be observed in Fig. 3, the current conduction of the LRS first follows the Ohmic law at high fields [the voltage is higher than ~5 V, as shown in Fig. 3(a)] and then there is a deviation from the Ohmic conduction at low fields [the voltage is lower than ~3 V, as shown in Fig. 3(b)]. This indicates that there are two conduction mechanisms involved in the current conduction of the LRS, depending on the voltage applied. We found that the high-field I-V curve is linear and the current of LRS decreases with the increase of temperature, indicating that current conduction represents Ohmic conduction with metal-like behavior due to phonon scattering of the electrons transportation in the filament.[5,6] We infer the formation of the metallic Au nano-phase in NiO near the Au/NiO interface during the top electrode evaporation. The Ohmic conduction with metal-like behavior in the forward-bias region may result from the induced continuous metallic filaments by contacts of excessive metallic Ni phases in NiO with Au nano-phases in NiO near the Au/NiO interfaces.[14] However, the low-field current of LRS increases with the increase of temperature, indicating that the dramatic temperature dependence of the conduction of the LRS at low fields observed in the present study suggests that the SCLC can be excluded as the main conduction mechanism.[5] To determine whether the hopping conduction dominates the low-field LRS behavior, analysis was conducted according to the log (I)-V relationship.[5] Figure 3(c) shows the linear log (I)-V curve at low fields, indicating that the low-field current of LRS exhibits the hopping conduction behavior. This behavior resulted from the discontinuous metallic filament influenced by electrical fields.[14] We deduce that the conduction

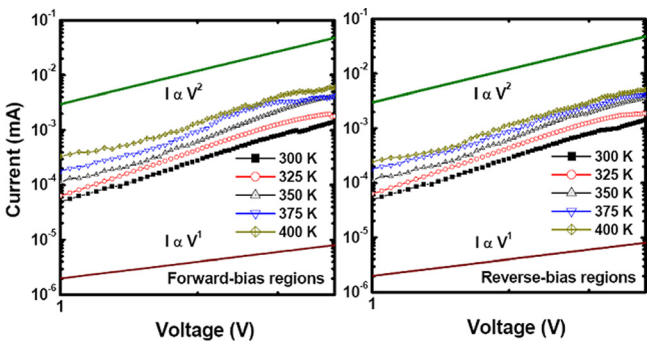

FIG. 2. The log (I)-log (V) curves of HRS of Au/NiO/p^+-Si devices as a function of temperature in the forward-bias and reverse-bias regions, respectively.

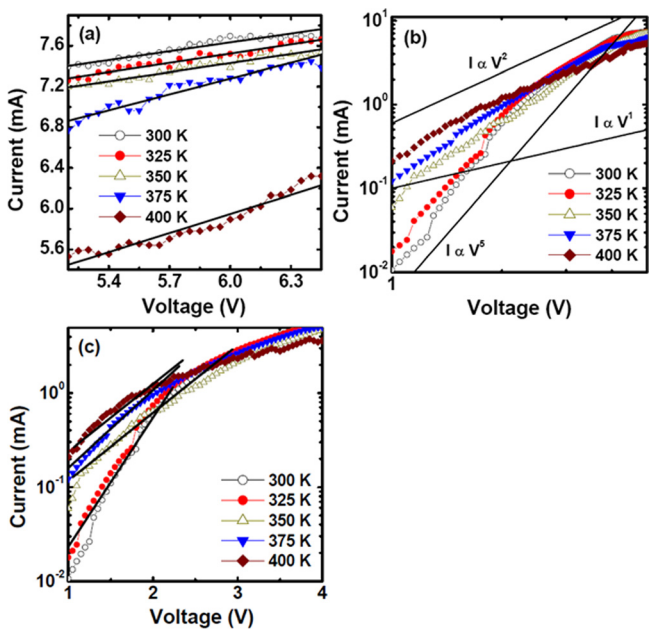

FIG. 3. The forward-bias on-state I-V curves of Au/NiO/p^+-Si devices as a function of temperature at (a) high and (b) low fields and (c) the forward-bias on-state log (I)-V curves of Au/NiO/p^+-Si devices as a function of temperature at low fields.

of LRS at low fields is due to the electron hopping between the states (the metallic Ni phase and the metallic Au nanophase) and the thermal excitation of the electrons trapped in the states into the conduction band of NiO.

To clarify the origin of a resistive switching behavior, the reverse-bias on-state current conduction mechanism was investigated. The reverse-bias I-V curves of LRS are compared under various temperature conditions. To determine whether the hopping conduction dominates the reverse-bias LRS behavior for Au/NiO/p^+-Si devices, analysis was conducted according to the log (I)-V relationship.[5] Figure 4(a) shows the reverse-bias on-state current of the Au/NiO/p^+-Si device measured within a temperature range from 300 K to 400 K. The linear log (I)-V curve is found, indicating that the current of LRS in the Au/NiO/p^+-Si devices exhibits the hopping conduction behavior.[6,7] The hopping conduction of leakage current is attributed to the presence of the defective interlayer. This could be due to the fact that the interfacial reaction between NiO film and p^+-Si substrate is thermodynamically favorable.[15,16] We infer that heat treatment at 400 °C on Si substrate in NiO deposition may lead to the formation of a $NiSi_xO_y$ layer at the NiO/p^+-Si interfaces. Chakraborty *et al.* found that an additional layer of SiO_2 formed at the NiO/Si interface which has a large impact in the resistive switching.[15] Dais *et al.* found that distinct phase formation and phase separation occur at the NiO/Si interface, accompanied by the build-up of a lateral nano-scale undulated structure (that is, the formation of $NiSiO_3$).[16] Trap states close to the porous low-*k* dielectric materials/p-type Si interfaces were considered to affect interfacial barriers with contacts and consequently electrical leakage and reliability in these materials.[17] These interfacial traps were investigated for metal/insulator/silicon capacitor structures composed of carbon-doped oxide low-*k* dielectric films with gold counter-electrodes by Atkin *et al.*[17] The hopping conduction can be expressed as[6,7]

$$I = Sqa_m n_e v_f \left[\exp\left(\frac{qa_m V}{2dkT} - \frac{\phi_t}{kT}\right)\right], \quad (1)$$

where S is the contact area, q is the electronic charge, a_m is the mean hopping distance, n_e is the density of space charge, v_f is the intrinsic vibration frequency, d is the film thickness, T is the absolute temperature, k is Boltzmann's constant, and ϕ_t is the barrier height of hopping. The ϕ_t extracted from the Arrhenius plot [Fig. 4(b)] is about 90 meV. To the hopping conduction, the conduction current increases with temperature, and this is resulted from thermally excited electrons hopping from one trap state to another trap state in the defective interlayer. The above results revealed that the interfacial property influences on the on-state I-V curve by controlling the interfacial reaction that serve to induce the different temperature-dependent resistive switching characteristics. This Letter opens the possibility of tuning the resistive switching characteristics of memory devices by interface passivation.

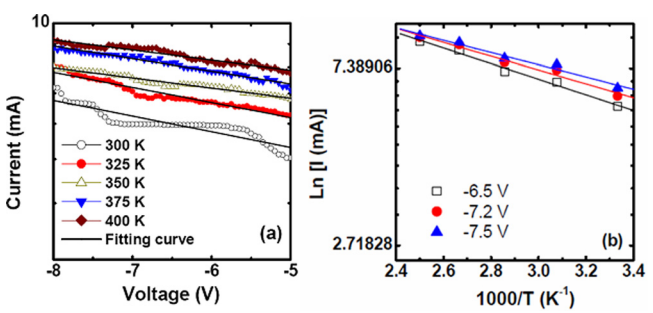

FIG. 4. (a) The reverse-bias on-state log (I)-V curves of Au/NiO/p^+-Si devices as a function of temperature and (b) the reverse-bias on-state ln (I)-1000/T curves of Au/NiO/p^+-Si devices at V = −6.5, −7.2 and −7.5 V.

Figure 5(a) shows the Si 2p core-level spectra at the NiO/p^+-Si interfaces, respectively. Figure 5(b) shows the Si 2p core-level spectra at the as-cleaned p^+-Si surfaces. The peak positioned at ~99.4 eV is attributed to Si–Si bonds, which are deconvoluted for Si $2p_{3/2}$ and Si $2p_{1/2}$.[18,19] The peak positioned at ~103 eV is attributed to Si–O bonds.[19] The Si-O bonds were found at the NiO/p^+-Si interfaces. However, no Si-O bonds were found at the as-cleaned n-Si surfaces. This implies that sol-gel techniques to deposit NiO onto Si substrates induce the Si-O bonding at the NiO/p^+-Si interface. In addition, the Si-O spectra are deconvoluted for SiO_2 and SiO_x ($NiSi_xO_y$). The 103.9-eV peak attributed Si–O bonds in pure SiO_2 and the 101.3-eV peak related to the SiO oxidation state were reported previously.[20,21] Thus, SiO_x ($NiSi_xO_y$), as shown in Fig. 5(a), is a nonstoichiometric compound. We suggested the presence of nonstoichiometric and stoichiometric SiO_x at the NiO/p^+-Si interface. A SiO_x layer may influence the electronic conduction through the device. We believe the temperature-dependent on-state current in the reverse-bias region has a relation to interface states; and, such result can be attributed to a SiO_x ($NiSi_xO_y$) layer at the NiO/p^+-Si interface. These results implicate that a SiO_x ($NiSi_xO_y$) interlayer, which impedes a p^+-Si contact with the metallic Ni phase in NiO, may lead to the formation of discontinuous metallic filament, resulting in the hopping conduction.

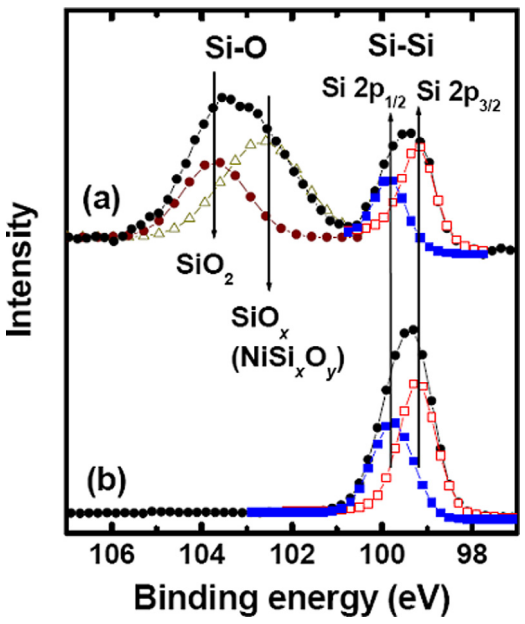

FIG. 5. (a) Si 2p core-level spectra at the NiO/p^+-Si interfaces and (b) Si 2p core-level spectra at the as-cleaned p^+-Si surfaces.

In summary, the fabrication of Au/NiO/p^+-Si memory device has been demonstrated. Memory mechanisms are described on the basis of the I–V results. The off-state carrier transport mechanism of the Au/NiO/p^+-Si device was attributed to the SCLC. However, the fitting data of the temperature-dependent on-state I–V curves in the forward-bias region demonstrated that the on-state carrier transport mechanism related to the memory effect of the Au/NiO/p^+-Si device was attributed to the Ohmic conduction with metal-like behaviors (the hopping conduction) at high (low) fields while the corresponding mechanism of the reverse-bias on-state I–V curves was related to the hopping conduction. The results revealed that the interfacial property influences on the on-state I-V curve by controlling the interfacial reaction that serves to induce the different temperature-dependent resistive switching characteristics.

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