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Understanding the trap-induced frequency dispersion in the *C–V* curve of AlGaN/GaN hetero-structure

Priyanka Nautiyal[1,*], Peyush Pande[2], Virender Kundu[1], Vikas Joshi[2] and Mayank Chaturvedi[3]

[1] Department of Electronics Science, Kurukshetra University, Kurukshetra, India
[2] Department of Electronics and Communication, Graphic Era University, Dehradun, India
[3] Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Australia

E-mail: priyankanautiyal2507@gmail.com

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Abstract

This article investigates the trapping mechanism in AlGaN/GaN heterostructure. For our study, the traps within the AlGaN layer are introduced at the interface and near the interface of AlGaN/GaN, in the SILVACO TCAD tool. Frequency-dependent capacitance-Voltage (*CVF*) curves are obtained to study the impact of traps on device performance. From the *CVF* curve, it is found that the existence of interface traps introduces a shift in capacitance along the gate voltage axis. These traps introduce the threshold voltage (V_{TH}) shift. Furthermore, a detailed study of near-interface traps (NITs) is done based on tunneling mechanisms. For our investigation, the NITs are positioned at 0.5 nm, 1 nm, and 1.5 nm away from the AlGaN/GaN interface. The response of the NITs reduces the capacitance value in the accumulation region. The response of the NITs is explained through the capacitance charge model and border trap model. For NITs placed 0.5 nm away from the interface, the frequency dispersion in the accumulation region becomes evident. On the contrary, the dispersion reduces significantly, as the NITs goes deeper upto 1.5 nm. The results indicate that the NITs nearer to the interface respond to high frequencies. Further, the temperature dependent capacitance–voltage analysis is done for both interface and NITs, to understand the effect of temperature on frequency dispersion.

Keywords: interface traps, near-interface traps, threshold voltage shift, AlGaN/GaN hetero-structure

1. Introduction

In recent years, increasing global energy consumption and device miniaturization have expanded the deployment of wide band gap semiconductors (WBGs) in the power industry [1]. So far, silicon has been dominating the semiconductor industry since 1960 with the invention of Silicon (Si) MOSFET in BELL Labs. Thereafter, this technology has developed to the extent that it has reached its technological limits. To overcome these limitations WBGs have emerged as a strong contender for Si. This is due to their superior material properties including high breakdown field, thermal conductivity, mobility, and saturation velocity [2]. Replacing Si with WBGs is the most promising approach to obtain enhanced power devices with low switching losses, small size, high switching frequency, operating temperature, power density, and breakdown voltage for next-generation power applications [3].

Among WBGs, especially GaN has gained a significant amount of importance, in the industry of power devices. The highest band gap, mobility, and the ability to form hetero-structures [4–6], among other WBGs, make GaN

* Author to whom any correspondence should be addressed.

a major competitor of Si-based technology. High electron mobility transistors (HEMTs) utilizing GaN material possess all the properties mentioned above. The presence of 2-dimensional electron gas (DEG) at the interface, as a result of piezoelectric and spontaneous polarization, creates a conductive channel without any doping. The absence of doping lowers the impurity scattering of the device, thereby increasing the electron mobility in GaN HEMTs. Thus, the unique properties of AlGaN/GaN heterostructure make them promising devices for high-power applications.

Despite having superior material properties and significant development in device processing techniques, still these devices suffer from long-lasting reliability and performance issues. Typically, these issues are associated with the existence of traps at different locations, which limits the market penetration of GaN technology. The inherent device structure, high temperature, and high voltage operation contribute to the generation of defects on the surface, in bulk, or at the interface of the GaN device [7, 8]. Further, various studies proved that the traps introduced during the fabrication and the growth process results in bulk and interface trapping [9–11]. In the literature, mostly the interface and near interface trap are analyzed for dielectric layer, on Si and SiC based devices [12, 13]. In this regard GaN devices are not much explored. Therefore, our study analyses the interface trap at the AlGaN/GaN interface, and the NITs in AlGaN layer because the AlGaN layer act as a dielectric layer owing to its high band gap and high dielectric constant. The AlGaN layer here is treated as an insulator like in MIS and MOS devices. Additionally the dislocation at the AlGaN/GaN hetero-structure due to lattice mismatch and nitrogen deficiency in the AlGaN layer [14, 15] creates interface and near-interface traps (NITs). Further, these traps become active when the gate voltage becomes greater than V_{TH} due to quantum confinement effect [16, 17]. Thus, degrading the device's reliability and performance by introducing threshold voltage (V_{TH}) instability and reduced channel density respectively [18–21]. Therefore, it is necessary to understand the trapping effect, for realizing a reliable GaN device. In this regard, many research groups have studied the trapping mechanisms and their impact on device reliability, performance, and stability [22–27]. However, the trapping-related issues are either reported for interface traps or bulk traps. For NITs, not much work has been reported so far in the literature for GaN devices.

For studying the trapping effect on device parameters generally, current-voltage (*I*–*V*) [22, 28] and capacitance-voltage (*C*–*V*) [29, 30] analysis is carried out. However, very few studies have explored the frequency and distance-dependent impact of NITs, through *C*–*V* analysis. Hence, it becomes extremely important to analyze the trap behavior through *C*-*V* characteristics. Mainly, the focus of the paper is to investigate the NITs as these traps become a dominant factor in degrading the device's performance. Moreover, to enhance our understanding, the traps which become active in the depletion region are differentiated from the traps which become active in the accumulation region.

In this article, a detailed simulation study is done to examine the trap behavior, through frequency-dependent *C*-*V* analysis in AlGaN/GaN hetero-structure. Further, temperature dependent capacitance voltage (CVT) analysis is done for different temperature (25 °C, 50 °C and 100 °C), using 1 MHz measuring signal. The commercially available 2-dimensional TCAD tool, provided by SILVACO is used for device simulations. For investigating the NITs, the traps are placed at three different depths in the AlGaN layer: (a) 0.5 nm (b) 1 nm, and (3) 1.5 nm away from AlGaN/GaN interface. Multi-frequency *C*-*V* analysis is done, for the traps at the interface and the NITs placed at different depths, with frequencies between 10 kHz to 1 MHz.

2. Simulation setup

This section deals with the device dimension details and the physical model used to realize AlGaN/GaN hetero-structure. Further, the capacitance calculation and trap-related parameters are discussed.

2.1. Device details and simulation models

To investigate the near-interface trapping effect, the device under consideration is a simple AlGaN/GaN hetero-structure. It consists of ohmic gate contact, a 25 nm thick AlGaN layer with 27% of Al content, a 2 μm thick GaN layer with doping concentration of 1×10^{13} cm^{-3} and Sapphire substrate. The sheet concentration of piezoelectric charges that create 2DEG at the AlGaN/GaN interface is 1.68×10^{13} cm^{-2}. Channel width and length for the device is 95 μm and 10 μm, respectively. Figure 1 illustrates the schematics of the AlGaN/GaN hetero-structure. The device dimensions used for simulations are in the range of a practical AlGaN/GaN structure reported in [31].

Normally, the interface trap density is expressed as the trap states per unit area of the interface per unit energy (cm^{-2} eV^{-1}) and the bulk/border trap density (NITs) is expressed as the trap states per unit volume per unit energy (cm^{-3} eV^{-1}). The interface trap density mentioned in [31] is a volumetric trap density (cm^{-3}eV^{-1}). Therefore, to distinctly demonstrate the influence of interface and NITs on *C*–*V* characteristics, we have excluded the consideration of volumetric interface trap density (cm^{-3} eV^{-1}) for interface trap, as mentioned in [31]. Instead, we modeled equivalent interface trap density as a sheet of traps at AlGaN/GaN interface (cm^{-2} eV^{-1}).

Further, the sapphire substrate just provides the mechanical support and is electrically idle. It does not affect the device performance. In simulation self-heating effect is not considered, as the focus of the study is to analyze the trap behavior. Thus, a simplified model is employed to simulate a AlGaN/GaN hetero structure, without considering the substrate. The models used for simulations are well calibrated with the experimental work [31]. The models are as follows: For the numerical simulation study, the Poisson equation, the continuity

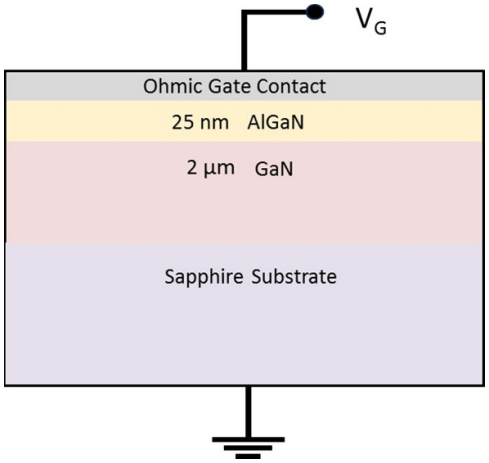

Figure 1. The schematic structure of AlGaN/GaN heterostructure on Sapphire substrate.

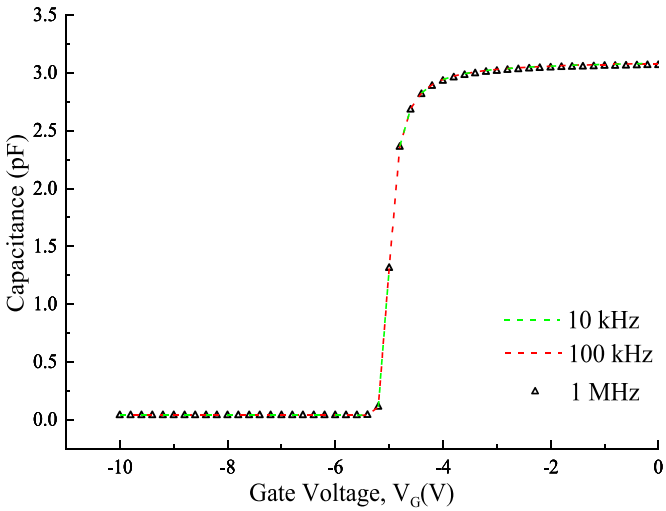

Figure 2. The simulated frequency-dependent *C*–*V* curve for no trap in AlGaN/GaN heterostructure.

equation, and the transport equation are solved in SILVACO ATLAS. To evaluate the impact of a flow of electrons into and out of the traps, Shockley–Read–Hall (SRH) model [32, 33] is adopted.

Additionally, a built-in polarization model is used to evaluate the total polarization charges of 2-DEG present at the hetero-structure interface. For low-field mobility in GaN, the model given by Albrecht *et al* [34] is used for electrons and holes.

2.2. Capacitance calculation

The capacitance value varies as applied gate voltage (V_G) changes in AlGaN/GaN hetero-structure. Based on V_G applied, the *C*–*V* behavior defines the regions of operations. These are the accumulation region, the depletion region, and the inversion region. Initially, for $V_G < V_{TH}$ in the *C*–*V* curve, the 2-DEG present at the interface is completely pinched off. With the rise in gate voltage, a rise in capacitance value is observed. The device starts conducting as V_G goes above V_{TH}. Thus, the rise in capacitance represents channel building and conduction in the device.

The following equation extracts the barrier capacitance $C_{AlGaN}(Max),(F)$ in TCAD tool:

$$C_{AlGaN}(Max),(F) = \frac{8.85 \times 10^{-12} \times A_{eff} \times \varepsilon_{AlGaN}}{t_{AlGaN} \times 10^{6}} \quad (1)$$

where, ε_0 is the free space permittivity ε_{AlGaN} is the relative permittivity of the $Al_{0.25}Ga_{0.75}N$ layer, A_{eff} is effective area of capacitance and, t_{AlGaN} is the thickness of the AlGaN layer. The constant (ε_0) is approximately equal to 8.854×10^{-12} F m^{-1}. The AlGaN barrier capacitance (C_{AlGaN}) can be calculated by using the ideal dielectric constant of the $Al_{0.25}Ga_{0.75}N$ ($\varepsilon_{AlGaN} = 8.81$) and AlGaN thickness ($t_{AlGaN}$) of 25 nm and effective area (A_{eff}) of $95 \times 10\mu m^2$.

The estimated AlGaN layer capacitance obtained for the device under consideration is 3.1187 pF. Figure 2 depicts the simulated *C*–*V* curve for AlGaN/GaN hetero-structure for different frequencies. As observed in figure 2, the capacitance value obtained in the accumulation region through simulations for different frequencies is almost equal to the calculated capacitance value. Further, as per equation (1), the AlGaN barrier capacitance is proportional to the material properties and dimension of the AlGaN layer. Thus, it can be inferred from equation (1) and figure 2, that there is no relation between capacitance and frequency. But when the traps are present in the AlGaN layer (mentioned in section 3), the variation in capacitance value is observed with frequency. Hence, the capacitance dependency on frequency is discussed in the article.

2.3. Trap implementation

In AlGaN/GaN hetero-junction, both AlGaN and GaN possess different band gaps, due to which a discontinuity is observed in the energy band gap of the two materials. Therefore, the transport mechanism in hetero-junction is different from homo-junction, as the charge carrier needs to overcome the potential barrier. To overcome the barrier, tunneling becomes the main transport mechanism. Further, the increased band mismatching and presence of traps in semiconductors introduce an additional transport mechanism called, trap-assisted tunneling [35].

The presence of traps creates the discrete energy level which lies in the forbidden energy band gap of the semiconductor. Hence, the AlGaN layer incorporating the traps, not only influences recombination statistics but also assists the electron transport through an energy barrier. To investigate the trapping mechanisms in AlGaN/GaN hetero-structure the models related to traps are discussed here. The interface trap is modeled as a single discrete trap level within the GaN band gap. To activate the interface traps, the INTTRAP

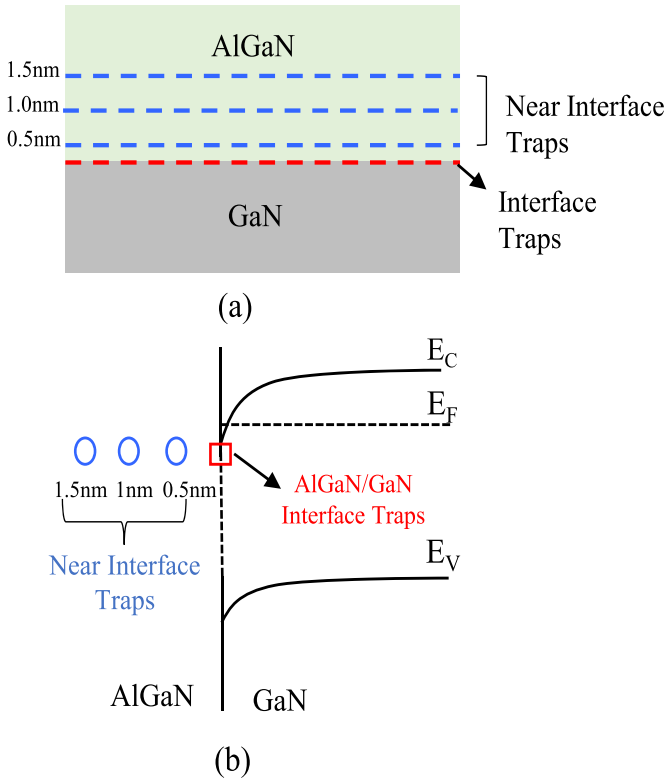

Figure 3. (a) The schematic diagram of interface traps and near-interface traps in AlGaN/GaN heterostructures. (b) Band diagram illustrating the simulated trap details close to the conduction band.

statement is used in SILVACO. The trap-assisted tunneling model is used, as the tunneling mechanism becomes dominant due to NITs. This model is based on trap-to-band phonon-assisted tunneling. Consequently, to enable the trap-assisted tunneling in SILVACO, TRAP.TUNNEL is specified in the model statement. In our models, only acceptor type of traps having a constant density, energy level, and uniform distribution are considered for both interface and NITs.

Study performed by Yang *et al* [36] observed the presence of electrically active traps in the bulk AlGaN layer and at the AlGaN/GaN interface positioned at an energy level of 0.5 eV below the conduction band minimum of AlGaN. Thus, an acceptor trap at energy level of 0.5 eV is used in our simulations. The acceptor trap either becomes negatively charged when occupied by an electron or becomes neutral when unoccupied. These types of traps are normally positioned below the conduction band edge. NITs are taken into account, with reference to their distance from the AlGaN/GaN interface. For our simulations, the traps (interface and NITs) are distributed uniformly at the interface and at different depths in AlGaN layer, with details mentioned in figure 3.

The trap-related parameters used in simulations are mentioned in table 1. The NIT density considered for simulations is well comparable to the value 10^{18}–10^{22} cm^{-3} eV^{-1}, observed in the literature [31, 37, 38]. Other trap parameters adopted, are according to the existing literature [39–41].

3. Results and discussion

3.1. Capacitance-voltage (C–V) characterization

This section investigates the behavior of interface and near-interface in the AlGaN/GaN hetero-structure through *C–V* analysis. Frequency dependent capacitance voltage (CVF) analysis is done with measuring signal frequency in the range of 5 KHz–1 MHz. Temperature dependent capacitance voltage analysis (CVT) is done for temperature in the range of 25 °C–100 °C using 1 MHz measuring signal.

3.1.1. Interface traps. Figure 4 shows the capacitance simulations for AlGaN/GaN hetero-structures, with interface traps and no traps. It is observed that the *C–V* curve shifts only along the gate voltage axis for interface traps. The *C–V* curve gets shifted, in accordance with the surface potential variation [42]. The surface potential value decides the amount of charge trapping at the interface.

3.1.1.1. CVF analysis. To investigate the effect of frequency on capacitance, multi-frequency *C–V* curves are obtained for four different frequencies: 5 KHz, 10 KHz, 100 KHz, and 1 MHz (see figure 4). The dispersion in the depletion region reveals the A.C. response of interface traps. Interface traps are mostly active in the depletion region, as they are present above the Fermi level. Thus, an exchange of charges takes place between active interface traps, and carriers present at the AlGaN/GaN channel.

A similar hump, as obtained in figure 4, is observed in [43], suggesting the presence of oxygen-related interface traps in AlGaN/GaN HEMT. In existing literature, traps are predominantly observed within the energy ranges of 0.43 eV to 0.50 eV [44–47] and 0.71 eV to 0.82 eV [48–52]. However, their precise origin remains unclear. A study [53] explores the source of these traps. It suggests that traps within the energy range of 0.43–0.50 eV are linked to oxygen-related defects and surface imperfections within the AlGaN barrier layer. Conversely, traps in the energy range of 0.71–0.82 eV are primarily attributed to carbon (C), iron (Fe), surface-related defects, and dislocations within the GaN buffer layer.

The observed hump is due to the placement of traps at particular energy level of 0.5 eV. To observe this, the C-V curve (see figure 5) is obtained for interface traps placed at two distinct energy level.

The observation is specifically done at 5 KHz, where the maximum hump is seen. It is evident that the hump in the *C–V* curve, at an energy level of 0.5 eV, is attributed to the close proximity of the interface traps to the conduction band edge. Conversely, when these traps move away from the conduction band edge, the hump starts to reduce and at an energy level of 1.2 eV no such hump is observed. Therefore, the distinctive hump is a consequence of the specific energy level positioning of the interface traps. In our simulation, we have placed these traps at defined energy levels, leading to the observed hump. This is in contrast to experimental measurements, where the

Table 1. Trap parameters.

Trap type and location	Carrier capture cross-section (SIGN, SIGP)	Energy level (E.Level)	De-Genrarcy factor	Trap density (N_A)
Acceptor type near-interface traps (NITs) in the AlGaN layer	3.4×10^{-15} cm^2	0.5 eV from AlGaN CB	2	1.5×10^{21} cm^{-3} eV^{-1}
Acceptor type trap at AlGaN/GaN interface	1×10^{-15} cm^2	0.5 eV from GaN CB	1	5×10^{12} cm^{-2} eV^{-1}

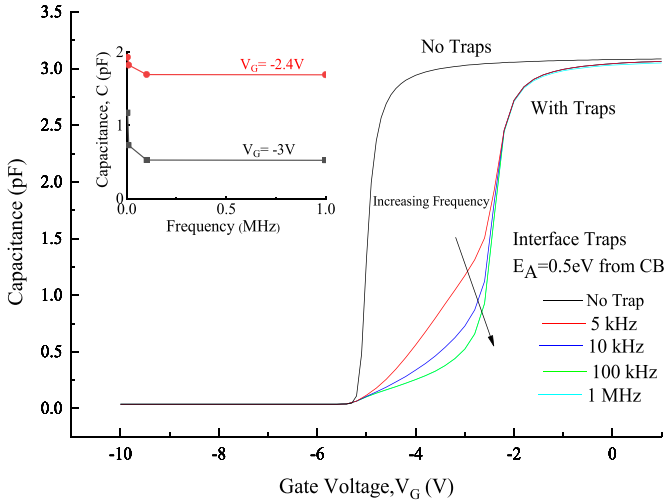

Figure 4. Frequency-dependent *C–V* characteristics of AlGaN/GaN interface traps. Inset depicts the simulated capacitance-frequency curve for different V_G.

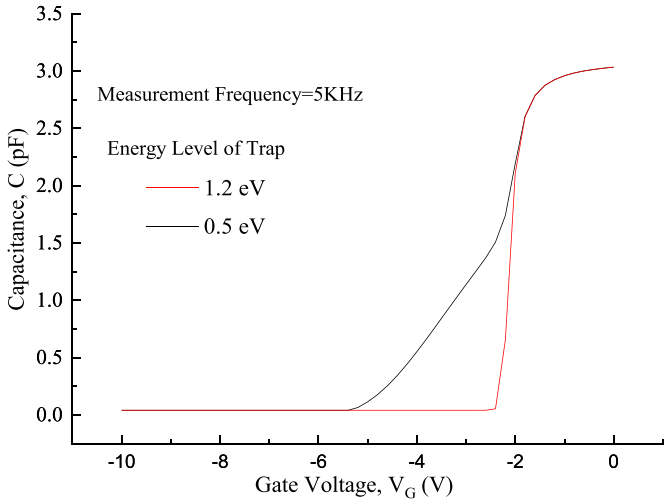

Figure 5. *C–V* curve for interface traps placed at two distinct energy level.

exact location of the traps remains uncertain, as it relies on the quality of the material and the fabrication techniques utilized.

The interaction between the interface traps and the charge carriers introduces the dispersion in the *C–V* curve, as the response time (time constant, τ) of the interface trap is dependent on temperature, capture cross-section, thermal velocity, and surface Fermi level [54].

The equation is given by:

$$\tau = \frac{1}{v_{\text{th}}\sigma_n n_i}\exp\left(\frac{q(\varphi_B - \varphi_s)}{kT}\right) \tag{2}$$

here, σ_n, v_{th}, n_i, k, T, φ_B and φ_s represent the cross-section of traps, the average thermal velocity, intrinsic carrier concentration, Boltzmann constant, absolute temperature, the potential difference between the intrinsic Fermi level and Fermi level, and band bending, respectively. Further, the inset of figure 4 depicts the capacitance frequency curve for 5 kHz–1 MHz frequencies at $V_G = -2.4$ V and -3 V. As seen from the inset, a drastic reduction in capacitance value is observed for frequencies between 0–100 KHz thereafter, it becomes constant. This concludes that the interface traps respond to lower frequencies, and it reduces as the frequencies of the AC input signal increases.

Additionally, the shift in the *C–V* profile indicates that the interface traps contribute to the V_{TH} instability in AlGaN/GaN structure. From *C–V* plot, the V_{TH} value of -5.22 V is obtained for AlGaN/GaN hetero-structure without trap. It is the voltage where the capacitance value is 90% of the 2-DEG plateau capacitance [55].

The threshold voltage is extracted from *C–V* curve by drawing a tangent in the partial depletion region and extrapolating it towards V_{GS} (see figure 6) [56]. Figure 7 shows the variation in V_{TH} with varying frequencies. Thus, for realizing reliable and safe GaN devices it is important to understand the interface trap behavior. Contrary to the depletion region, the interface traps in the accumulation region do not contribute any change in the *C–V* curve. In the accumulation region, due to Fermi-level pinning, the interface traps mostly lie far beneath the Fermi-level, in the energy band gap. Hence, these traps do not give any response, when an A.C. input signal is applied.

3.1.1.2. CVT analysis. Figure 8 shows the temperature dependent *C–V* dispersion for interface traps. In CVT analysis, as the temperature rises, a shift in the pinch-off voltage

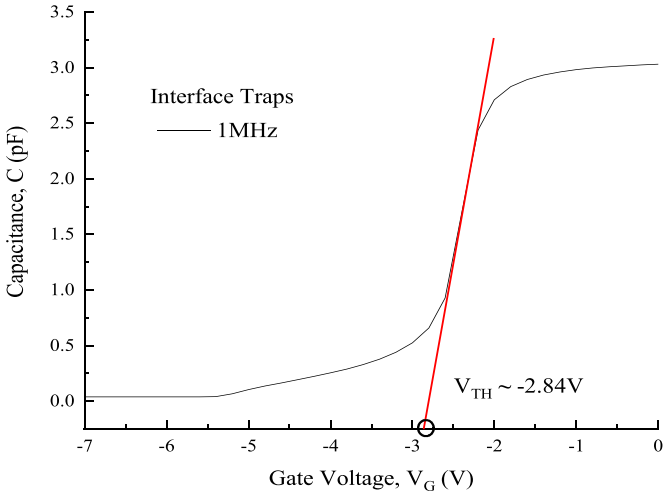

Figure 6. Threshold voltage (V) extraction from *C–V* curve, for interface trap simulated at 1 MHz frequency.

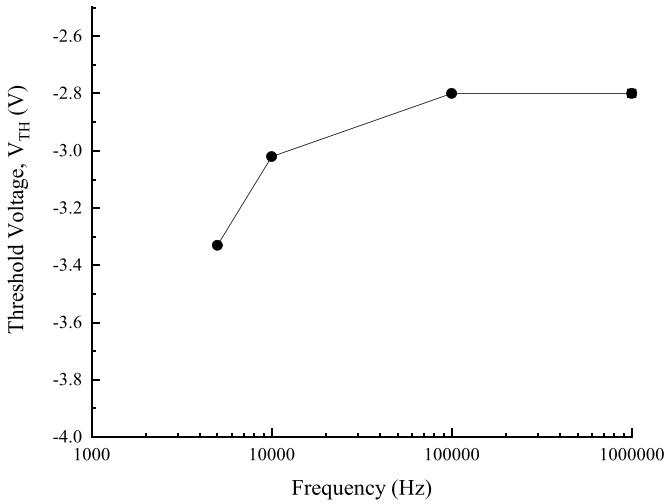

Figure 7. Threshold voltage shift with respect to change in frequency for interface trap.

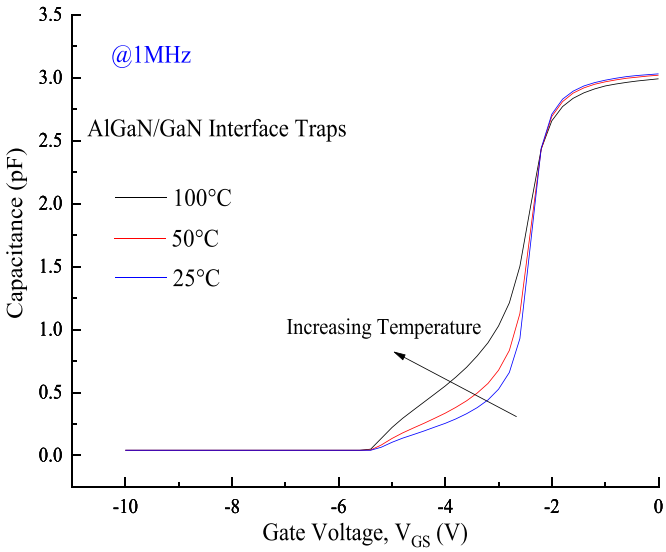

Figure 8. Temperature-dependent *C–V* characteristics of AlGaN/GaN interface traps.

towards negative value is observed. The dependency obtained is as observed in [30, 57].

3.1.2. Near- interface traps

3.1.2.1. CVF analysis. A frequency-dependent *C–V* plot for AlGaN/GaN hetero-structure is shown in figures 9(a)–(c), for NITs positioned at 0.5 nm, 1 nm, and 1.5 nm respectively, away from the interface. Due to NITs, the frequency dispersion in the *C–V* curve is evident in the accumulation region. It is seen from figures 9(a) and (b), the NITs nearer to the interface respond significantly, as compared to the NITs placed deeper into the AlGaN (see figure 9(c)). The response of the NITs determines the capacitance value in the accumulation region.

In this regard, the distributed border trap model proposed by Yuan *et al* [58, 59] analyzes the frequency-dependent *C–V* behavior. As per the model, the NITs placed in the AlGaN layer, capture and emit charge carriers from the mobile carrier present in the GaN conduction band through tunneling. Figure 9(d) shows the tunneling of charges between NITs and the carriers of the GaN channel. In the accumulation region, the pinning of the Fermi level at the bottom of the GaN conduction band eases the flow of electrons from GaN to the NITs in the AlGaN layer via tunneling. The time constant (τ_{NITs} is the average time needed by an empty NIT to capture an electron) is exponentially proportional to the depth (b) of NITs from the AlGaN/GaN interface. τ_{NITs} can be given as follow [58]:

$$\tau_{NITs} = \tau_0 e^{2kb} \tag{3}$$

where, τ_0 is the time constant of the trap at the same energy level, and k is the attenuation coefficient of the tunneling mechanism. According to equation (3) the deeper

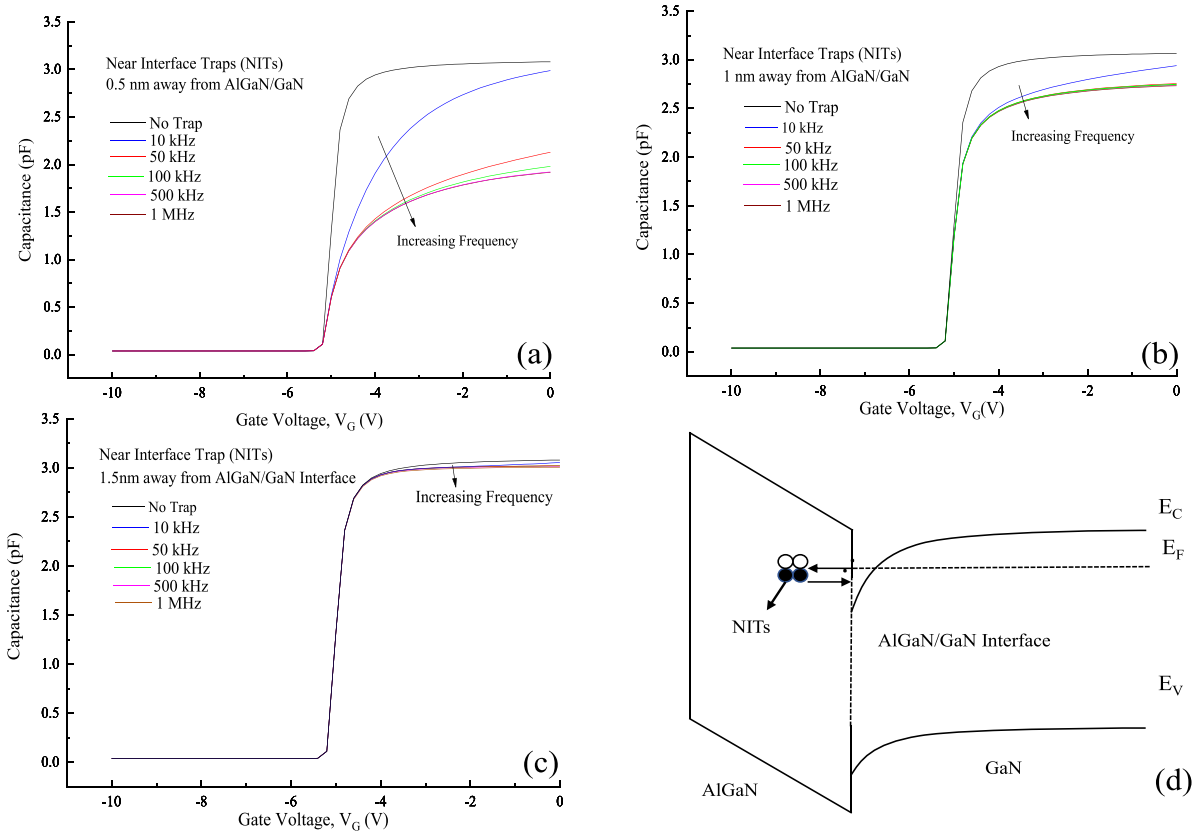

Figure 9. Frequency-dependent *C–V* characteristics for NITs positioned at (a) 0.5 nm, (b) 1 nm, (c) 1.5 nm away from AlGaN/GaN interface in the AlGaN layer, and (d) Band diagram showing exchange of charges between NITs and GaN conduction band through the tunneling mechanism, when biased in accumulation region.

NITs will have large τ_{NITs} values, while the NITs closer to the interface will have small τ_{NITs}. When the A.C input signal of frequency(f_{in}) is applied, the deep NITs having a time constant greater than the frequency of the input signal$\left(\tau_{\mathrm{NITs}} > \frac{1}{f_{\mathrm{in}}}\right)$, hardly respond. Only the NITs closer to the interface will exchange charges through tunneling, for which the time constant is smaller than the input ac signal frequency $\left(\tau_{\mathrm{NITs}} < \frac{1}{f_{\mathrm{in}}}\right)$ [60].

Similar frequency dispersion is observed for both interface and NITs [61–63]. Since these are experimental work thus, one can observe the combined effect of both the interface and near interface traps, depicting the dispersion in both depletion and accumulation region. Moreover, in experimental work, the nature and formation of trap states are significantly influenced by both the quality of the material and the techniques used in device fabrication.

To understand the inter-dependency of NITs' distance from the AlGaN/GaN interface, with the frequency of applied A.C signal, the change in capacitance is plotted in figure 10. Here, the change in capacitance (ΔC) indicates the response of NITs. As can be seen in figure 10, ΔC is significant for closer NITs at 1 MHz and it reduce as the NITs go deeper. After evaluating the response of NITs at different depths and for various frequencies, it can be concluded that the NITs nearer to the AlGaN/GaN interface are mainly observed at higher frequencies.

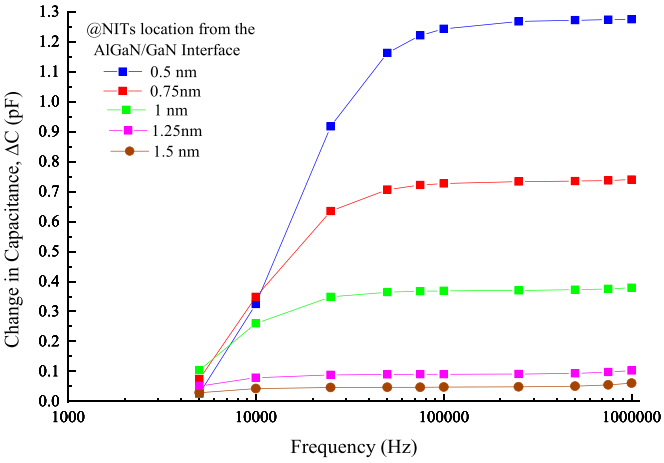

Figure 10. Change in capacitance plotted as a function of frequency for NITs positioned at different depths from AlGaN/GaN interface in the AlGaN layer.

3.1.2.2. CVT analysis. Figure 11 illustrate the temperature independent effect of near interface traps in AlGaN/GaN heterostructure.

In NITs the capture and release of charge carriers from the channel take place through tunneling, which is a temperature independent mechanism [17, 64]. The observed result (see

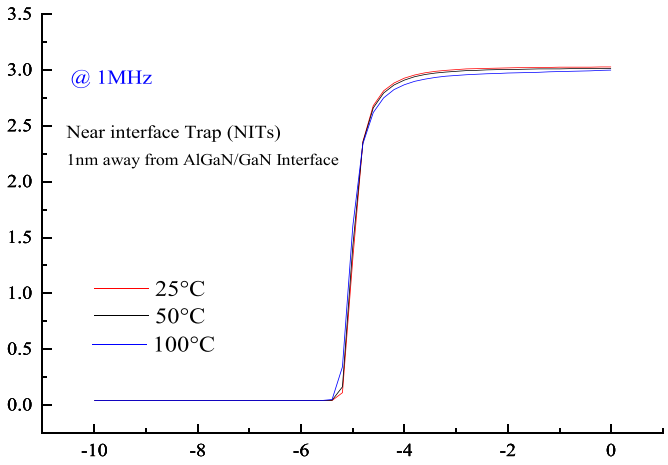

Figure 11. Effect of temperature on *C*–*V* curve for near-interface traps (NITs).

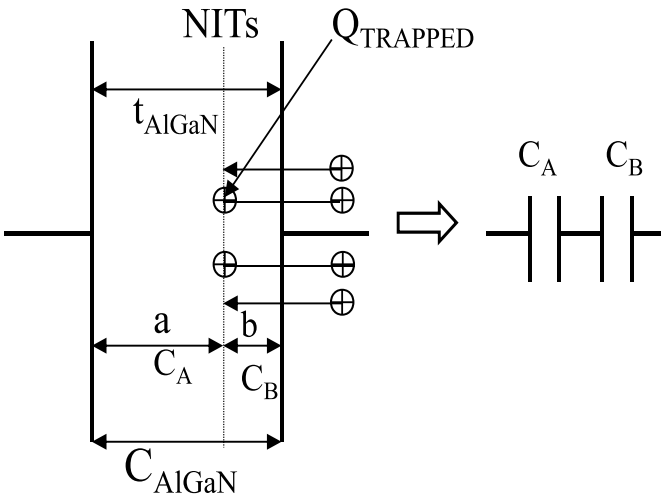

Figure 12. The HEMT capacitor is represented through the capacitance charge model [64].

figure 11), confirms that NITs are not activated by temperature [65, 66].

3.2. Mathematical model

The capacitance charge model shown in figure 12 is used to understand the capacitance behavior in the presence of NITs [64].

The trapping and de-trapping process of NITs, in AlGaN/GaN hetero-structure, can be modeled as two capacitors C_A and C_B. C_A and are formed when NITs get occupied with the charges. When these traps are active, the AlGaN/GaN capacitance C_{AlGaN} is the series combination of C_A and C_B

The model includes the following equations:

The electric field across C_A can be calculated as:

$$E_A = \frac{Q_{\text{BACK\_CONTACT}}}{\varepsilon_{\text{AlGaN}}}. \tag{4}$$

The voltage across C_A is given by:

$$V_A = E_A \times a \tag{5}$$

here, E_A electric field for C_A, $Q_{\text{BACK\_CONTACT}}$ is per unit charge at back contact of GaN capacitor, $\varepsilon_{\text{AlGaN}}$ is AlGaN permittivity, V_A is the voltage across the capacitor C_A, and a is the thickness of C_A

Gauss law is used here for enclosing the charge trapped in NITs (at the C_A/C_B interface):

$$E_A + E_B = \frac{Q_{\text{TRAPPED}}}{\varepsilon_{\text{AlGaN}}} \tag{6}$$

where E_B electric field for C_B, $Q_{Trapped}$ is the charge trapped in NITs per unit area. Substituting equations (4) in (6) gives:

$$E_B = \frac{Q_{\text{TRAPPED}}}{\varepsilon_{\text{AlGaN}}} + \frac{Q_{\text{BACK\_CONTACT}}}{\varepsilon_{\text{AlGaN}}}. \tag{7}$$

Similarly, the voltage (V_B) across the capacitor C_B having thickness b is given as:

$$V_B = E_B \times b. \tag{8}$$

Thus, the total voltage (V_{TOTAL}) across the AlGaN/GaN capacitor is:

$$V_{\text{TOTAL}} = E_A \times a + E_B \times b. \tag{9}$$

Substituting E_A from (4) and E_B from (7) in (9) and rearranging gives:

$$V_{\text{TOTAL}} = \frac{Q_{\text{BACK}_{\text{CONTACT}}}}{\varepsilon_{\text{AlGaN}}}(a+b) + \frac{Q_{\text{TRAPPED}}}{\varepsilon_{\text{AlGaN}}}b \tag{10}$$

where $(a+b)$ is the total thickness of AlGaN (t_{AlGaN}). Equation (10) shows that an extra term ($\frac{Q_{\text{TRAPPED}}}{\varepsilon_{\text{AlGaN}}}b$) is added to the total voltage. This term is due to the charge trapping at NITs, placed at a distance b from the positive plate of the capacitor. Thus, an increase in the total voltage across the AlGaN/GaN capacitor is observed, which in turn reduces the capacitance. In case of deeper traps, the charge trapped (Q_{Trapped}) in NITs become negligible. Therefore, the term ($\frac{Q_{\text{TRAPPED}}}{\varepsilon_{\text{AlGaN}}}b$) added to the total voltage become less dominant.

Thus, not much variation in capacitance value is observed as the trap goes deeper. Hence, it can be concluded that though the response of NITs reduces the capacitance value in accumulation, this variation becomes insignificant as the traps go deeper.

4. Conclusion

In this work, the frequency-dependent *C*–*V* (CVF) and temperature dependent (CVT) analysis is done for interface and NITs. A good agreement is obtained in simulated and calculated capacitance value. Interface traps become dominant in the depletion region. A shift in the *C*–*V* curve along the gate voltage axis is observed for interface traps, which results in

device V_{TH} instability. Frequency dispersion in the accumulation region is demonstrated when NITs are introduced in the AlGaN layer of the hetero-structure. The analysis done for NITs is based on the tunneling mechanism. The response of the NITs reduces the capacitance value in the accumulation region, which degrades the device's performance. The capacitance charge model is used to explain the variation in capacitance value.

Further, the frequency and the distance-dependent of NITs are explained through the border trap model. We found that as the trap goes deeper (i.e. 1.5 nm) into the AlGaN layer, they become less dominant. This creates negligible frequency dispersion in the *C–V* curve. However, the dispersion significantly rises, when the NITs are placed close to the interface (i.e. 0.5 nm). Finally, the change in capacitance that corresponds to the response of NITs is calculated for various NITs positioned at different frequencies. In CVT analysis, it is found that the frequency dispersion for interface traps is temperature dependent, while for NITs the frequency dispersion is temperature independent.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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ORCID iDs

Priyanka Nautiyal https://orcid.org/0000-0001-5552-6972
Vikas Joshi https://orcid.org/0000-0002-8949-0258
Mayank Chaturvedi https://orcid.org/0000-0002-6585-8927

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