

Interpretation of the I - V , C - V and G/ω - V characteristics of the $Au/ZnS/n$ - $GaAs/In$ structure depending on annealing temperature

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ABSTRACT

The Zinc Sulphide (ZnS) thin film, which is included in the Au/n - $GaAs/In$ diode as the interface layer, was grown on the n - $GaAs$ semiconductor substrate by the spray pyrolysis method. First, to reveal some structural, surface and optical properties of the ZnS thin film, XRD, SEM and absorption measurements were taken. It was determined that the ZnS thin film completely covering the surface of the n - $GaAs$ semiconductor substrate has a hexagonal structure and a forbidden energy range of 3.83 eV. Later, the current-voltage (I - V), the capacitance-voltage (C - V) and the conductance-voltage (G/ω - V) measurements of the $Au/ZnS/n$ - $GaAs/In$ structure were taken at room temperature, and various important parameters of the structure were calculated with different methods. In order to reveal the effects of annealing temperature on the I - V , C - V and G/ω - V measurements of $Au/ZnS/n$ - $GaAs/In$ structure, the device was annealed at 100, 200 and 300 °C respectively for 5 min in nitrogen gas environment. The characteristic parameters were calculated again and the results were interpreted comparatively. At the same time, with the help of the C - V and G/ω - V characteristics, the dependence on applied bias voltage and frequency of the parameters such as dielectric constant, dielectric loss, loss tangent, ac electrical conductivity and real and imaginary part of electric modulus of the diode have been revealed. After thermal annealing at 200 °C, it has been determined that the ideality factor, turn-on voltage and leakage current values are at minimum level and the barrier height and rectification ratio values are at maximum level. In other words, it has been revealed that the optimum thermal annealing temperature for this device is 200 °C.

1. Introduction

II-VI group thin films such as ZnS are getting great attention today as they have potential applications in a wide range of electronic devices such as nano-electronics, optoelectronics and photovoltaics [1–4]. Especially ZnS with a wider band-gap is preferred as a non-toxic buffer layer in solar cells [3]. ZnS, which has a cubic crystal structure in its most stable state, has two types of crystal structures, hexagonal wurtzite and cubic zinc blende [5]. Due to its high dielectric constant, excellent insulating properties and stable chemical structure, ZnS thin films can be also used for the passivation of the semiconductor surface in metal-semiconductor rectifier contacts. Although it can be produced by many methods [6–11], one of the most common methods used in the production of ZnS thin films is spray pyrolysis, because of its simplicity, low cost, high capacity to deposit smooth, uniform and homogeneous thin films over a large area [4,12]. In this method, carrier gas flow rate,

solution flow rate, substrate temperature, scanning speed and distance between substrate and nozzle can be easily adjusted to obtain high quality doped and undoped ZnS thin films. Deposition rate and thickness of the films can be easily controlled by changing the spraying parameters.

In metal-semiconductor rectifier junctions, the effects of the interface layer on the electrical characteristics of the junction is well known, and the behavior of the junctions produced using different interface layers has been extensively investigated in recent years [13–22]. When such a thin layer is placed between the metal and the semiconductor, both the electrical and dielectric properties of the junction can be modified. Placing such an interfacial layer in the junction can increase its performance and stability by reducing the magnitude of the interfacial states and dislocations present on the semiconductor surface at the junction interface [23,24]. Generally, the capacitance of these structures is independent of frequency, especially at frequencies greater than 1

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MHz. But, due to the frequency dependence of the *ac* signal, there is a capacitance arising from the interface states in addition to the depletion layer capacitance. The capacitive behavior of the junction differs from the ideal case due to the capacitance resulting from the interface states and often referred to as excess capacitance. Since this excess capacitance is strongly dependent on the applied bias voltage and frequency, the *C-V* and *G/ω-V* characteristics of the device are significantly affected. Therefore, in the investigation of the electrical and dielectric properties of the device, the effects of the applied bias voltage and frequency must be taken into account. In low frequency application signals, the frequency response of parameters such as the dielectric constant, dielectric loss and loss tangent is very dominant, and their physical source is still under investigation [25]. At the same time, the values of the parameters that characterize the performance of the junction are highly related to the thickness and morphological structure of the interface layer used. Therefore, the interfacial layer must be perfectly homogeneous, free from defects such as pin-holes with high dielectric breakdown, and provide a very high quality interfacial layer/semiconductor interface without unsaturated bonds [26,27]. It is now well known that such properties are required to develop novel microelectronic devices.

To summarize, a nontoxic ZnS is one of the most important materials for both device applications and basic research. ZnS have outstanding quality for device applications as it is a material with wide band gap, high dielectric constant, excellent insulating properties, stable chemical structure and direct transition [1–4]. In this study, the ZnS thin film was used as the interfacial layer in the *Au/n-GaAs* junction. These types of devices have important application in a wide variety of the optoelectronic devices, bipolar integrated circuits and high frequency applications. It is well-known that interface properties have a dominant influence on the device performance, reliability and stability. The stability of the barrier height value can be supplied by processes like the formation of thin layer between metal-semiconductor interfaces or by annealing the metal-semiconductor contact. It is probable that the ZnS thin film forms a physical barrier between the metal and *n-GaAs* semiconductor substrate, which prevents the metal from directly contacting the *GaAs* surface. Therefore, in this study, ZnS thin film has been used with this aim in the *Au/n-GaAs* structure. Considering the information presented above, the *Au/ZnS/n-GaAs/In* structure was produced under laboratory conditions in the present study and its electrical and dielectric properties were investigated depending on the thermal annealing. The structure, whose ideality factor, barrier height, series resistance, leakage current and rectification ratios were determined by the *I-V* measurements, and the dependence of its parameters such as dielectric constant, dielectric loss, loss tangent, *ac* electrical conductivity and real and imaginary part of electric modulus on applied bias voltage and frequency was revealed with the help of the *C-V* and the *G/ω-V* measurements.

2. Experimental procedure

In this study, the *Au/ZnS/n-GaAs/In* structure was produced using *n*-type *GaAs* semiconductor with (100) surface orientation and about $2.5 \times 10^{17} \text{ cm}^{-3}$ carrier concentration and electrical characteristics such as the *I-V*, *C-V* and *G/ω-V* of this structure were investigated depending on annealing temperature. Before the ohmic contact was made, the *n-GaAs* wafer was chemically cleaned using the standard cleaning method [28]. To obtain low resistance ohmic contact, indium metal was evaporated on the back surface of the *n-GaAs* wafer under vacuum (10^{-6} Torr), and then the *In/n-GaAs* junction was thermally annealed at 450°C for 3 min in flowing nitrogen in a quartz tube furnace. To place the desired interface layer into the structure, ZnS thin film was grown by spray pyrolysis method on the cleaned and polished surface of *n-GaAs* substrate with ohmic contact with indium metal. The spray solution was prepared by mixing $\text{CH}_4\text{N}_2\text{S}$ and ZnCl_4 chemical materials. S^{2-} and Zn^{2+} ions were sourced from cationic and anionic precursors. Deionized water served as a solvent. The substrate temperature was set at 450°C .

The nozzle-to-substrate distance was optimized to be 30 cm. The other deposition parameters were a solution flow rate of 5 mL/min and 90° angle of the spray nozzle with respect to the substrate. In addition, air was used as a gas carrier under 3 bar pressure. Next, to determine the contact area of structure and to perform the electrical measurement, Au metal was evaporated onto the ZnS in a vacuum-coating unit at 10^{-6} Torr and the contact area was determined as $7.85 \times 10^{-3} \text{ cm}^2$. Thus, the *Au/ZnS/n-GaAs/In* structure was obtained. The process steps of the manufactured structure were summarized in Fig. 1. The *I-V*, *C-V* and *G/ω-V* measurements of the *Au/ZnS/n-GaAs/In* structure were measured using HP 4140B picoammeter and HIOKI IM 3536 (4 Hz-8 MHz)/LCR meter at the frequency range of 30 kHz-3MHz with DC power supply at room temperature and in the dark., respectively. In order to observe the effects of the thermal annealing, the structure was annealed at 100, 200 and 300°C respectively for 5 min in nitrogen gas environment. Electrical measurements were repeated under the same conditions after each annealing process. In the evaluation of the device characteristics, a naming was made as follows:

- D0: Characteristics of as-deposited *Au/ZnS/n-GaAs/In* structure.
- D1: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 100°C
- D2: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 200°C
- D3: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 300°C

3. Results and discussion

3.1. XRD, SEM and UV-Visible absorption analysis of ZnS thin film

As stated in the introduction part of the article, ZnS thin films can exist in a cubic (zinc blende type) or hexagonal (wurtzite) phase. The XRD spectra of ZnS thin film prepared at the substrate temperature of 450°C are shown in Fig. 2. The XRD pattern shows preferential orientation at 20 equal to 28.30. According to standard JCPDS data (File No. 36–1450), this peak can be indexed as the (002) reflection of the hexagonal ZnS phase and the other peaks located at different 20 angles can be also indexed as reflections (100), (101) and (100), (012), (110) (022) and (013), respectively. The presence of different peaks in the XRD pattern indicates that the film has a polycrystalline nature. At the same time, apart from the characteristic peaks of ZnS, (002) reflection which may belong to hexagonal ZnO was also detected. This situation has been attributed to the occupation of some S sites in the ZnS lattice by oxygen atoms in the air which is used as carrier gas. This observation suggests that the films are single phase and oxygen atoms might have substituted S site without changing the hexagonal structure. Oxygen from carrier gas may diffuse through voids in the film and oxidize during the film formation [1,29,30].

SEM is a good technique to examine the surface topography of thin films. The surface microstructure of the ZnS thin film as observed by SEM was shown in Fig. 3 (a). It is seen from the image captured that the deposited film is uniform throughout the entire surface. The film covered the surface of the *n-GaAs* semiconductor substrate well, without voids or cracks. It is clear from the image that there are agglomerations of small sized grains and these grains are randomly oriented on the substrate, consistent with the polycrystalline observed in the XRD pattern. At the same time, the closely packed nano-grains showed good adhesion and homogeneous distribution on the substrate. Therefore, it can be easily said that the ZnS thin film produced based on morphological findings can be used as a good interface layer in the metal-semiconductor rectifier junctions.

Optical measurements are one of the most common methods used to determine the energy band gap value of thin films. In this method, the spectrometer gives the film absorption depending on the wavelength of the light used. The relationship between absorption coefficient (α), band gap energy (E_g) and photon energy ($h\nu$) is as $\alpha h\nu = B(h\nu - E_g)^{1/2}$ [5].

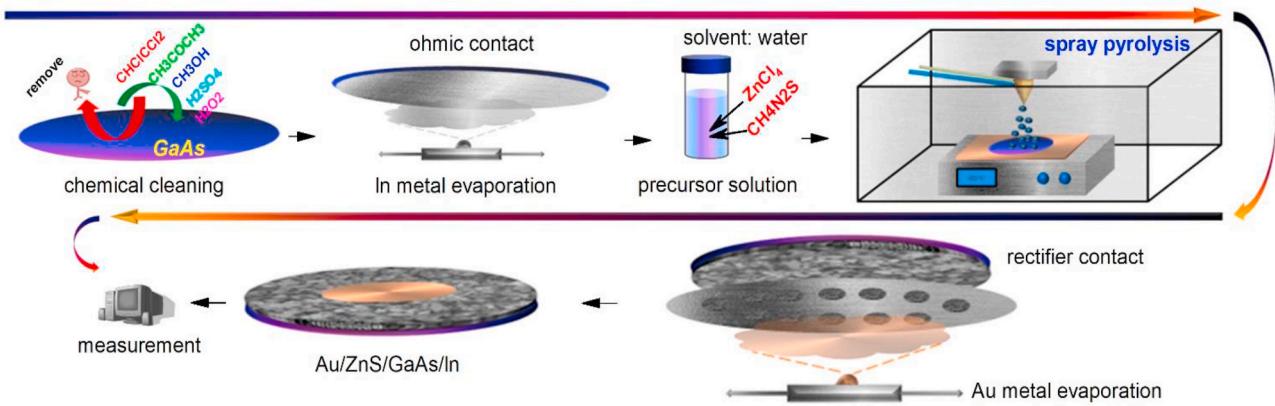


Fig. 1. Summary of the process steps of the manufactured device.

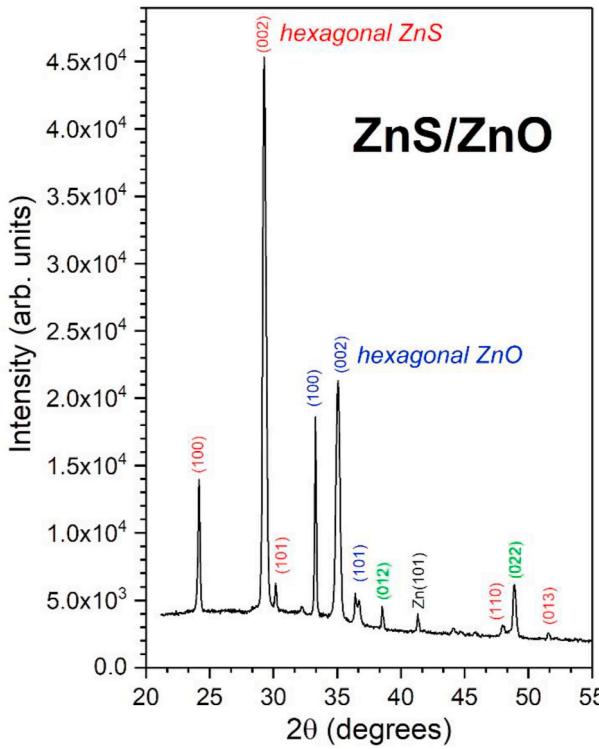


Fig. 2. XRD pattern of ZnS thin film.

Where B is an energy independent constant, but generally depend on the refractive index and the effective masses of the hole and electron respectively. According to this equation, the energy band gap value of the thin film can be determined by extrapolating the straight portion of the $(ahv)^2$ versus $h\nu$ plot to $(ahv)^2 = 0$. The absorbance-energy plot of the ZnS thin film obtained by spray pyrolysis method was presented in Fig. 3 (b). The energy band gap value obtained from this graph corresponds to 3.83 eV and this value is very close to the energy band gap values obtained for ZnS thin films in the literature [4,11,31–34]. The wide band gap energy (as 3.83 eV) of ZnS thin film can be shown as a reason why it is preferred as the interface layer in devices such as Schottky barrier diodes.

3.2. Analysis of the I-V characteristics of the Au/ZnS/n-GaAs/In structure depending on thermal annealing

The importance of thermally stable and reliable metal-

semiconductor junctions in device technology is well known. The performance of these junctions depends on the quality of the interface between the metal and the semiconductor surface. In such junctions, the quality of the interface can be increased by processes such as surface passivation and thermal annealing. Therefore, in order to obtain a high-performance device in this study, both the ZnS thin film was used as the interface layer in the $Au/n\text{-GaAs}$ junction and this structure was thermally annealed at low temperatures such as 100, 200 and 300 °C respectively for 5 min in nitrogen gas environment.

The forward and reverse bias the I - V and the $\ln(I)$ - V characteristics of the $Au/ZnS/n\text{-GaAs}/In$ structure were given in Fig. 4 (a) and (b) as a function of thermally annealing, respectively. In a practice diode, the turn-on voltage can be defined using the point where the diode begins to transmit exponentially. Using Fig. 4 (a), the turn-on voltage values of the device were calculated for each annealing temperature and it was observed that it decreased significantly after heat treatment at 200 °C. The relationship between the turn-on voltage and the annealing temperature was shown in Fig. 5 (a). That is, the diode voltage required to produce a certain current was decreased after thermal annealing at 200 °C. At the same time, using the $\ln(I)$ - V characteristics given in Fig. 4 (b), the diode leakage current and rectification ratio values were calculated and their changes depending on the annealing temperature were given in Fig. 5 (a). The rectification ratio values of the $Au/ZnS/n\text{-GaAs}/In$ structure were determined as the ratio of the forward bias current to the reverse bias current at the application voltage of 0.7 V for each annealing temperature. It was observed that the largest rectification ratio and the smallest leakage current normalized values were reached by thermal annealing at 200 °C. After thermal annealing at 300 °C, the leakage current of the diode increased, and hence the rectification ratio decreased. In other words, considering the turn-on voltage, leakage current and rectification ratio parameters together, we can say that the appropriate thermal annealing for this structure is 200 °C. Again, based on the graph given in Fig. 4 (b) and using the thermionic emission $[n = (q/kT)(dV/dlnI)]$ and $\Phi_b = (kT/q)\ln(AA^*T^2/I_0)$ [35,36], Norde $[\Phi_b = F(V_0) + (V_0/\gamma) - (kT/q)]$ and $R_s = kT(\gamma - n)/qI$ [37] and Mikhelashvili $[\beta = qV_m(\alpha_{max} - 1)/kT\alpha_{max}^2]$, $\Phi_b = kT[(\alpha_{max} + 1) - \ln(I_{T_m}/ST^2A^*)]$ and $R_s = V_m/(I_{T_m}\alpha_{max}^2)$ [38] methods, the ideality factor, barrier height and series resistance values of the structure were calculated as a function of the annealing temperature. Details on the calculation of these parameters can be found in the given references. The $F(V)$ - V curves obtained from the Norde method were given in Fig. 4 (c) and the α_{max} - V curves obtained from the Mikhelashvili method were also given in Fig. 4 (d). Variations of the ideality factor, barrier height and series resistance depending on the annealing temperature were shown in Fig. 5 (b), (c) and (d), respectively. As can be seen from these graphs, the lowest values of the ideality factor and the highest values of the barrier height were reached in the thermal annealing at 200 °C. In the thermal annealing at 300 °C, while

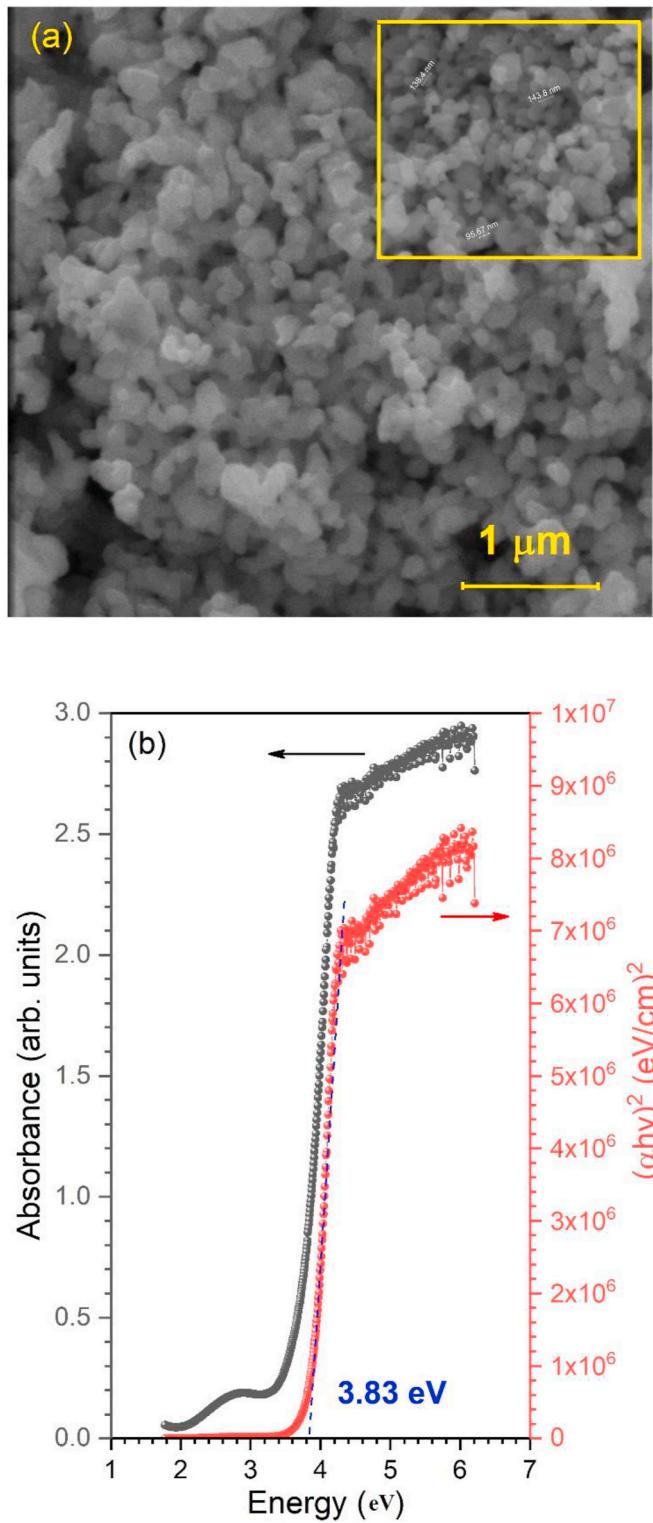


Fig. 3. a) SEM images of the ZnS thin film on *n*-GaAs substrate, b) The absorbance-energy plot for ZnS thin film.

the values of the ideality factor increased, the barrier height values decreased. We can say that the series resistance changes similarly. In practice, since it is desired that the ideality factor is low and the barrier height is high, we can say that thermal annealing at 200 °C is quite suitable for this structure. The fact that the ideality factor value is greater than one indicates that apart from thermionic emission, transport mechanisms such as recombination, tunneling and interface traps,

which are effective on the diode, should also be taken into account [39]. The increase in barrier height up to 200 °C thermal annealing may be associated with the increase in film homogeneity. In other words, voids and cracks, which are rarely found on the surface of the ZnS film, may have decreased in thermal annealing up to 200 °C and thus the surface homogeneity of the film may have increased. The decrease in the defects and interfacial states in the interface region depending on film surface homogeneity can be seen as the reason for the increase in barrier height of the structure. Conversely, the decrease in barrier height in thermal annealing at 300 °C may be most likely associated with the deterioration of the surface homogeneity of the film, possibly due to changes in film stoichiometry, and hence renewed defects and interface conditions.

3.3. Analysis of the C-V characteristics of the Au/ZnS/n-GaAs/In structure depending on thermal annealing

With the help of the C-V measurements, the nature of the diode's space-charge region can be investigated. Since charges or traps located in the interface are sensitive to the frequency of the applied *ac* signal, making the C-V measurements depending on the frequency can provide detailed information about this region. Therefore, the forward and reverse bias the C-V characteristics of the as-deposited and annealed at different temperatures the Au/ZnS/n-GaAs/In structure were measured at room temperature in the frequency range of 30–3000 kHz. The C-V characteristics of the device are shown in Fig. 6 for D0, D1, D2 and D3. Since the width of the depletion layer changed with applied bias voltage, the capacitance under the reverse bias increased slowly with decreasing bias voltage. As can be seen in Fig. 6, the C-V characteristics of the as-deposited and annealed structure have also an anomalous peak. These peaks in the capacitance curves may be related to the distribution of deep traps in the gap, series resistance and interface states [40]. The peak values of the capacitance in these characteristics both decreased with increasing frequency and the positions of the peaks shifted towards lower voltages. The decrease in capacitance with increasing frequency is due to the inability of the interface states to respond to high frequencies. As can be found in many studies in the literature, the shift in the peak positions may be caused by interface states that response differently at low and high frequencies [41–46]. In each graph in Fig. 6, the voltage values corresponding to the peak values of the capacitance are shown on the graphs. While the magnitudes of the peak values of the capacitance depending on the frequency in D0, D1 and D2 are almost the same, in D3 the capacitance has decreased significantly. This change can be attributed to structural changes occurring in the junction with thermal annealing at 300 °C.

In metal-semiconductor rectifier junctions, the space charge region capacitance per unit area is given by the relation $C^{-2} = 2(V_d + V)/q\epsilon_s A^2 N_d$ [35,36]. Where q is the electronic charge, ϵ_s is the dielectric constant of semiconductor, A is the effective area of the junction, N_d is the concentration of ionized donor atoms in the n-type semiconductor and V_d is the diffusion potential at zero bias and is determined from the extrapolation of the linear C^{-2} - V plot to the V axis. From the C^{-2} - V plots, the values of the barrier height can be obtained by the relation $\Phi_b = V_d + V_n$. Where V_n is the potential difference between the Fermi level and the bottom of the conduction band in the neutral region of semiconductor and can be calculated from $V_n = kT \ln(N_c/N_d)$ relation knowing the N_d [47]. The plots of $1/C^2$ as a function of bias voltage for the as-deposited and annealed the Au/ZnS/n-GaAs/In structure are shown in Fig. 7. As can be clearly seen from these graphs, the C^{-2} - V curves displayed linear behavior over a wide range of bias voltage for D0, D1, D2 and D3. Linearity of C^{-2} - V plots indicates a uniform doping density throughout the active regions of samples. The changes of V_d , N_d , V_n and Φ_b parameters obtained from these graphs depending on the annealing temperature and measurement frequency are given in Fig. 8. The obtained ionized donor atoms concentrations were found in the range of 2.282×10^{17} - 2.825×10^{17} cm⁻³ for D0, 2.086×10^{17} - 2.397

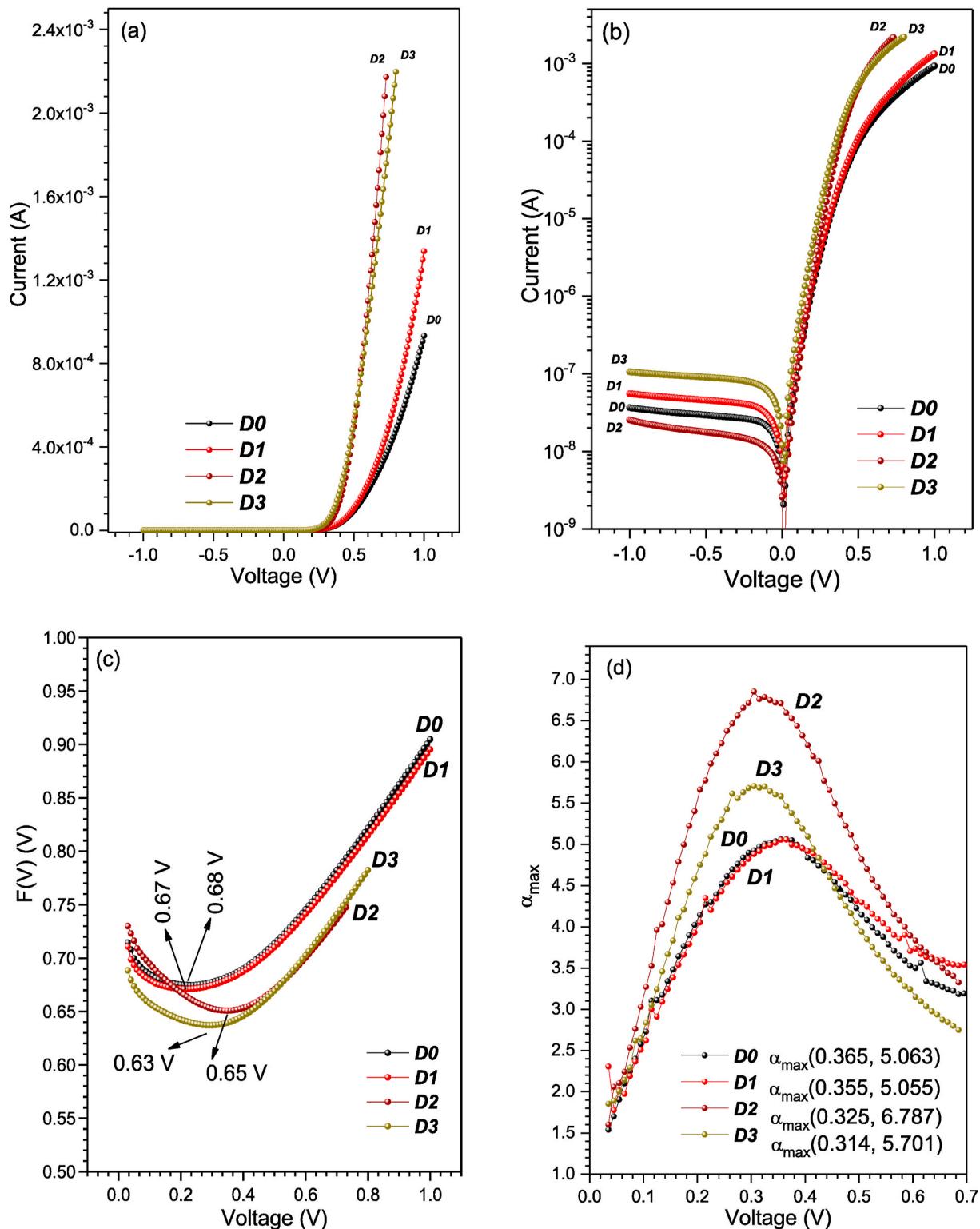


Fig. 4. (a) The forward and reverse bias I - V , (b) $\ln(I)$ - V , (c) $F(V)$ - V (Norde method) and (d) α_{\max} - V (Mikhelashvili method) characteristics of the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure as a function of thermal annealing.

$\times 10^{17} \text{ cm}^{-3}$ for D1, 2.320×10^{17} – $2.586 \times 10^{17} \text{ cm}^{-3}$ for D2 and 3.524×10^{17} – $4.232 \times 10^{17} \text{ cm}^{-3}$ for D3 for the 30–3000 kHz frequency range, respectively, which is similar to the value provided by the manufacturer. Then the barrier heights were calculated in the range of 0.437–0.824 eV for D0, 0.439–0.635 eV for D1, 0.556–0.702 eV for D2 and 0.683–1.145 eV for D3 for the 30–3000 kHz frequency range, respectively. It can be seen from Fig. 8 that the values of barrier height increase with increasing

frequency. The higher the barrier height at higher frequencies is due to the ZnS interface layer. Since the presence of a sufficiently thick interface layer leads to a high, intercept point (V_d), higher values of the barrier height at higher frequencies can be attributed to the ZnS interface layer. Other important parameters that may cause this situation can be listed as the maximum electric field in the junction, the depletion region width, interface states and the image force effect [48]. Again, the

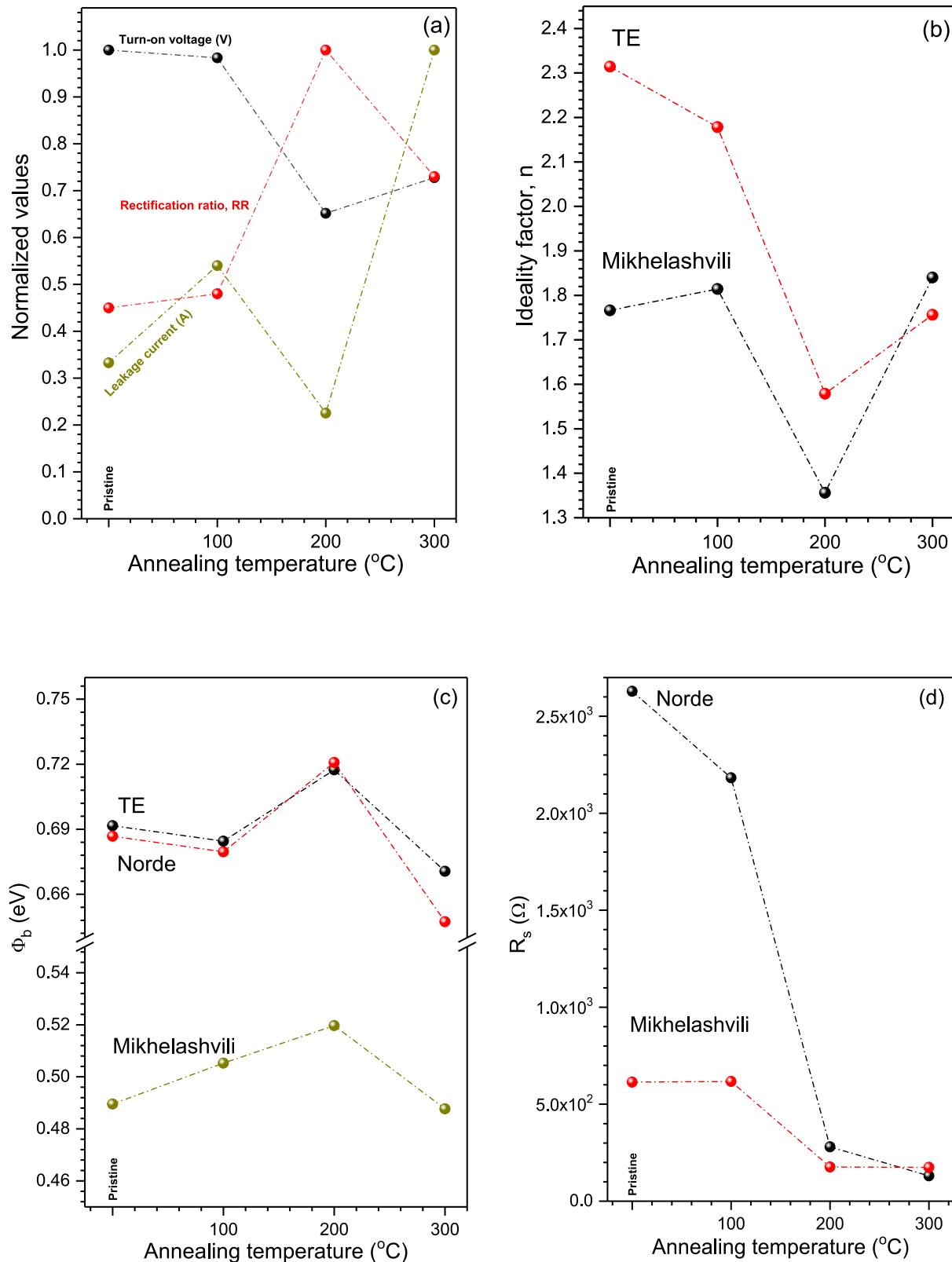


Fig. 5. (a) The changes of the values of turn-on voltage, leakage current and rectification ratio, (b) The changes of the values of the ideality factor obtained from thermionic emission and Mikhelashvili methods, (c) The changes of the values of the barrier height obtained from thermionic emission, Norde and Mikhelashvili methods and (d) The changes of the values of the series resistance obtained from Norde and Mikhelashvili methods with the annealing temperature for the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure.

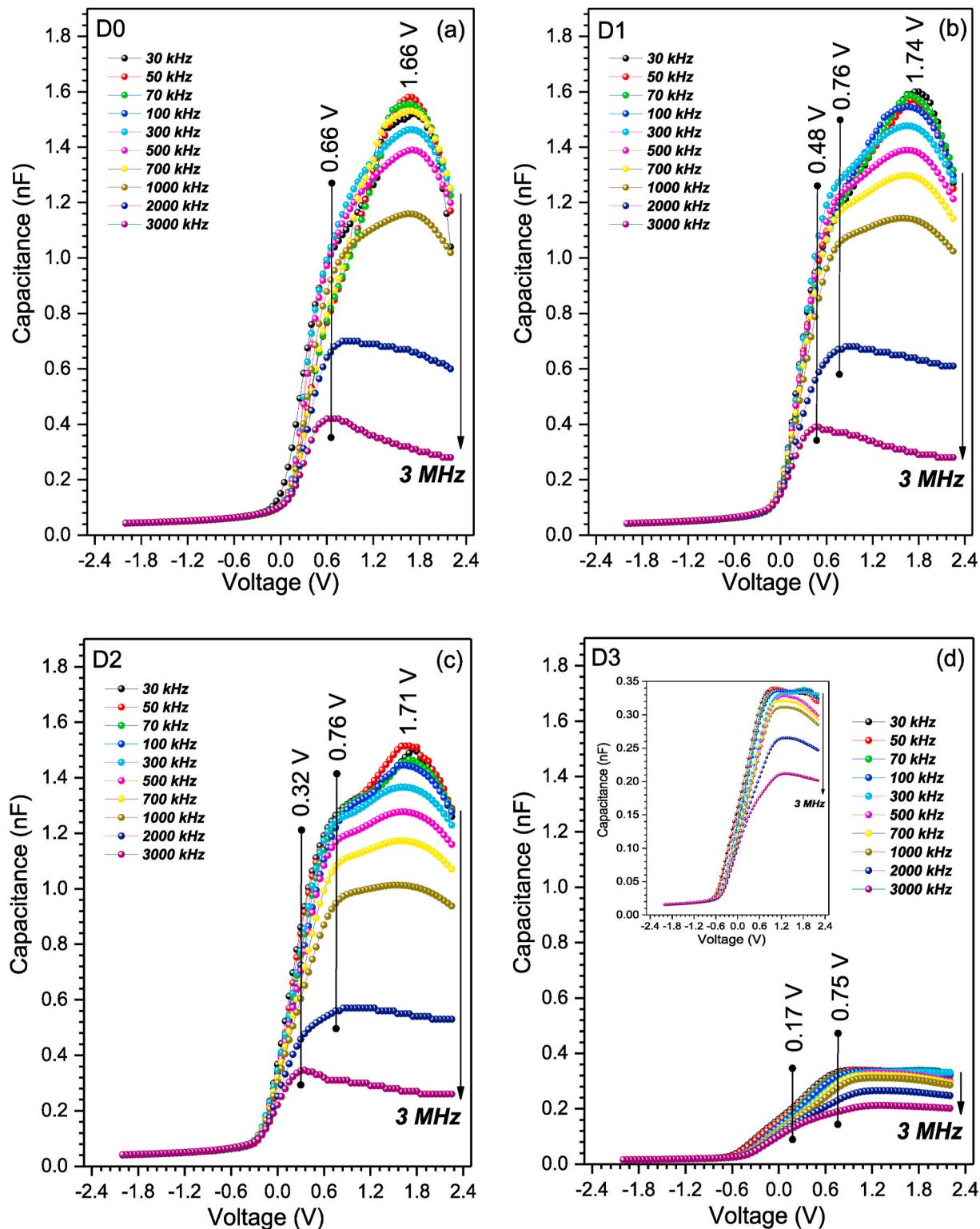


Fig. 6. The C-V characteristics of the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure measured at $T = 300 \text{ K}$ in the frequency range of 30–3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. The maximum of the capacitance axis has been changed in the inset in the D3.

graphs in Fig. 8 show that the values of parameters such as V_n , N_d , V_d and ϕ_b are strongly dependent on frequency because of the quality of the ZnS interface layer. It can be clearly stated that the thickness of the interfacial layer placed in the junction and the uniformity of the barrier height are very important in the C-V and the G/ω -V characteristics.

3.4. Frequency and voltage effects on the dielectric properties and electrical conductivity of the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure depending on thermal annealing

As known, while conductivity is related to the motion of free electrons, dielectric constants are related to the behavior of bound electrons. We can say that the dielectric constant is a measure of the extent to

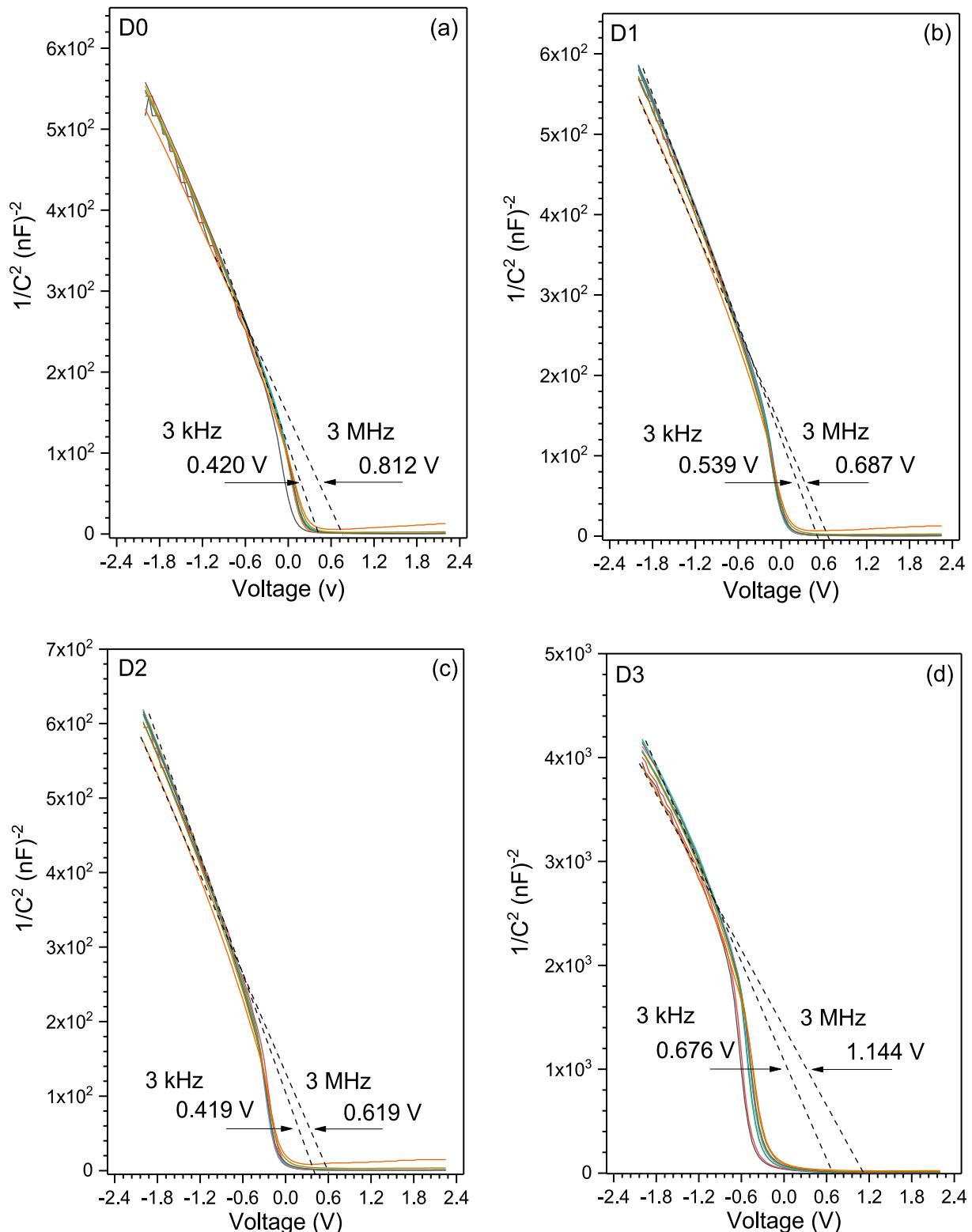


Fig. 7. The C^{-2} -V characteristics of the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure measured at $T = 300 \text{ K}$ in the frequency range of 30–3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3.

which a substance concentrates the electrostatic lines of flux. Dielectric constant can also be expressed as the ratio of the amount of electrical energy stored in an insulator when static electric field is applied to the dielectric material with respect to the vacuum. Apart from vacuum, the response of dielectric materials to external fields generally depends on the frequency of the imposed field. The dependence on this frequency is

due to the fact that the polarization of a material does not respond immediately to the applied field. Therefore, the dielectric constant is usually expressed as a complex function of the frequency of the applied field. The response of materials to alternating fields is characterized by a complex dielectric constant consisting of real and imaginary parts. When an electric field is applied to a dielectric medium, the current flowing

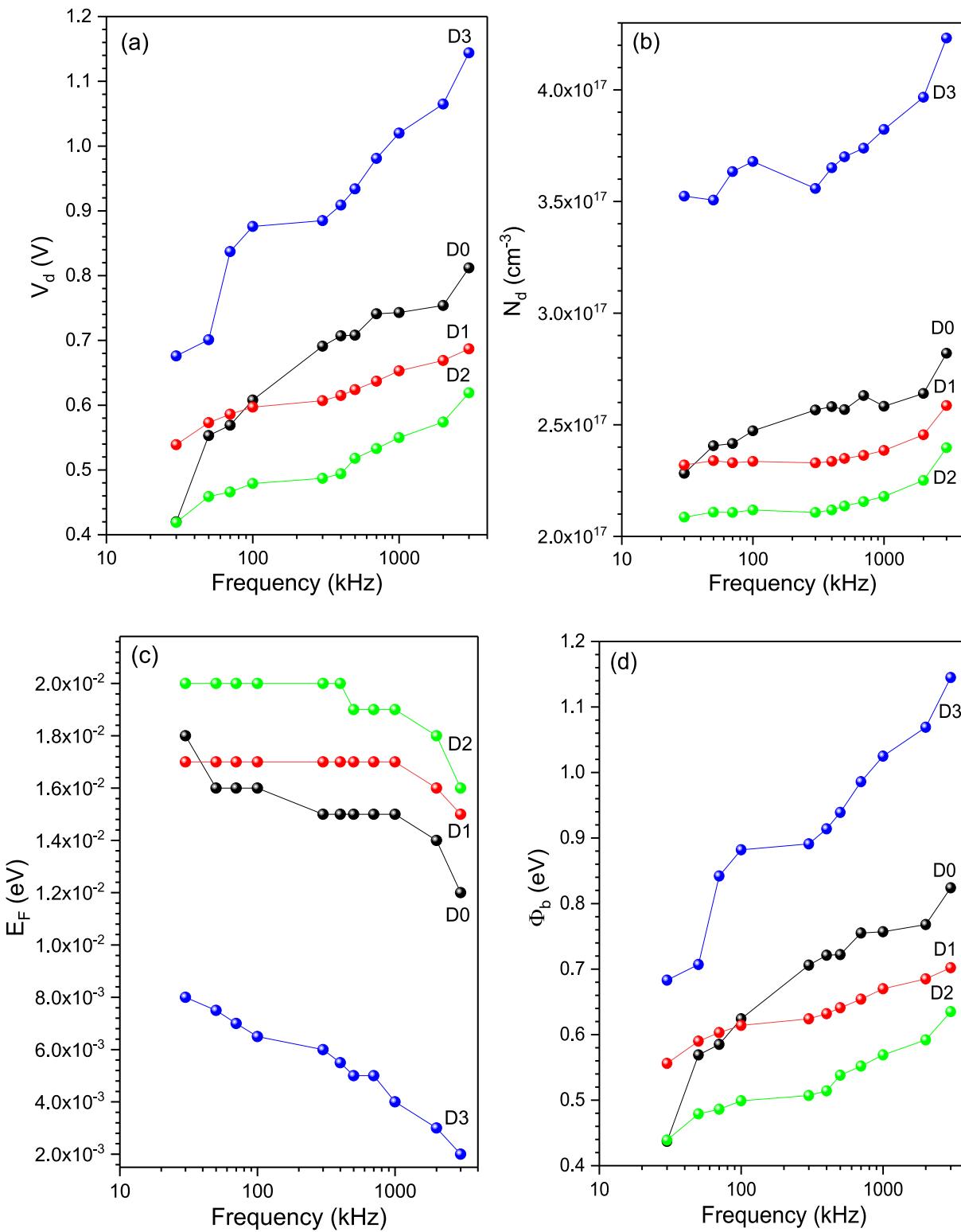


Fig. 8. The changes of the V_n , N_d , Φ_b and V_d values obtained from the C^{-2} - V characteristics depending on thermal annealing and frequency for (a) D0, (b) D1, (c) D2 and (d) D3.

through the real dielectric is the sum of conduction and displacement currents. While the conduction current is extremely small in good dielectrics, the displacement current can be thought of as the elastic response of the dielectric material to any change in the applied electric field. As the magnitude of the electric field increases, a displacement current flows and, the additional displacement is stored as potential energy in the dielectric. Unlike, when the electric field is decreased, the

dielectric releases some of the stored energy as a displacement current. There are two types of losses in all dielectrics except vacuum. One of them is a conduction loss and the other is a dielectric loss. While the conduction loss represents the flow of actual charge through the dielectric, the dielectric loss is due to the rotation or motion of atoms or molecules in the alternating electric field.

It is very important to consider the admittance data analysis method

in the characterization of metal-interface layer-semiconductor structures. Investigating the role of interfacial states in different polarization mechanisms in dielectric materials, taking into account the G/ω -V properties in a wide frequency range, may contribute to a better understanding of possible current conduction mechanisms through the dielectric medium. At the same time, studying the dielectric loss can also

contribute to understanding the dissipation of energy in the form of heat through dielectric materials [49]. The capacitance and conductance expressions for such structures are derived by Nicollian and Goetzberger [50]. The G/ω -V characteristics of the Au/ZnS/n-GaAs/In structure obtained by considering this method are given in Fig. 9 at variable frequencies and annealing temperatures. As it can be clearly seen from

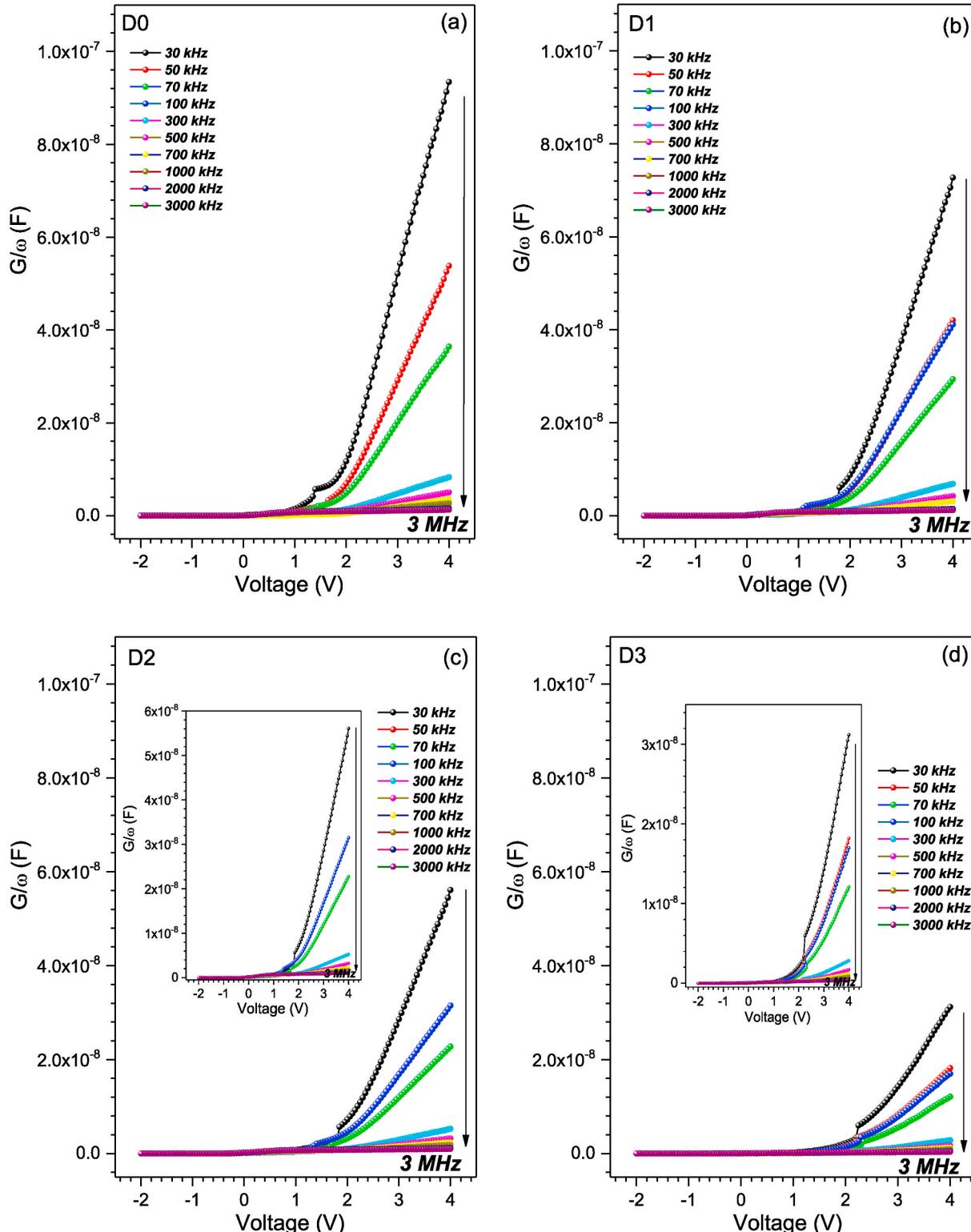


Fig. 9. The G/ω -V characteristics of the Au/ZnS/n-GaAs/In structure measured at $T = 300$ K in the frequency range of 30–3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. The maxima of the G/ω axis have been changed in the inset in the D2 and D3.

these graphs, the measured G/ω was quite sensitive to applied bias voltage and frequency especially in the positive bias voltages. The G/ω values are decreasing rapidly with increasing frequency. Again, the decrease in the G/ω values with increasing frequency is due to the inability of the interface states to respond to high frequencies. Therefore, the variation of G/ω -V characteristics with frequency may be attributed the existence of interface states [50]. The conductance is associated with the losses originating from the exchange of majority carriers between ZnS/n -GaAs interface and majority carrier band of semiconductor when an ac signal is applied to structure [51].

Details of the calculation of dielectric parameters such as complex dielectric permittivity, ac conductivity and complex electrical modulus of diodes with interfacial layer from measured capacitance and conductance data are widely available in the literature [43,49–52]. Generally, the dielectric constant is defined as a measure of the energy/charge stored in the material by electrical polarization. As stated in above references, the complex dielectric constant or permittivity ϵ can be written as $\epsilon = \epsilon' - i\epsilon''$, considering the real ($\epsilon' = Cd_i/A\epsilon_0$) and imaginary ($\epsilon'' = Gd_i/\omega A\epsilon_0$) components. Where i is the square root of -1 , C is the measured capacitance, G is the measured conductance, A is the junction area, d_i is the interfacial layer thickness and ϵ_0 is the permittivity of free space (8.85×10^{-12} F/m). ϵ'' is a measure of how dissipative or loss a material to an external electric field. This parameter is also called the loss factor and its value is always greater than zero and is usually much smaller than ϵ' . It can be said that the energy losses in the material are caused by the orientation of the molecular dipoles or the conduction of ionic and slow polarization currents. The static permittivity is a good approximation for altering fields of low frequencies, and as the frequency increases a measurable phase difference δ emerges between the electric field and the electric flux density. The $\tan \delta$, which is known as dissipation factor or dielectric loss tangent can be expressed as $\tan \delta = \epsilon''/\epsilon'$. Another important parameter used to investigate the polarization and relaxation process in ionic-electronic conducting materials is the complex electric modulus expressed as $M = \frac{1}{\epsilon} = M' + iM'' = \frac{\epsilon'}{(\epsilon')^2 + (\epsilon'')^2} + i\frac{\epsilon''}{(\epsilon')^2 + (\epsilon'')^2}$. That is, the complex electric modulus, M , is expressed as the reciprocal of the complex dielectric permittivity, ϵ . The M' and M'' are the real and imaginary components of M , respectively. Thus, the relationship between the above parameters and ac electrical conductivity can be expressed as $\sigma_{ac} = \omega C \tan \delta (d_i/A) = \epsilon'' \omega \epsilon_0$ [53]. According to this equation, ac electrical conductivity is directly proportional to dielectric loss. Figs. 10–12 shows the variation of the ϵ' , ϵ'' and $\tan \delta$ as a function of frequency in the range 30 kHz–3000 kHz with varied voltages from 0 V to 1 V, respectively. At the same times, the changes of the ϵ' , ϵ'' and $\tan \delta$ with $\ln(\omega)$ are presented in inset these graphs. It is seen from these graphs that all three parameters are strongly dependent on both applied bias voltage and frequency. High values of dielectric constant at low and moderate frequencies can be explained by the interface polarization model. Especially at these frequencies, dipoles have enough time to align by the electric field before the field changes. Space charge polarization due to an accumulation of space-charges between interfacial layer and semiconductor can be also demonstrated by causing high values of ϵ' at low frequencies [54]. In the high frequency region, the dielectric constant values are low as the contribution of atomic and electronic polarization is negligible. That is, dipoles cannot follow the field at high frequencies. It can also contribute to polarization at charges in interface traps. But, this contribution is usually negligible at high frequencies. Again, $\epsilon' - \ln(\omega)$ graphs confirm that ϵ' is very sensitive to both applied bias voltage and frequency. The dielectric loss factor which depends upon various structural factors and shows energy dissipation in dielectric material is due to the relaxation losses at high frequencies. It was previously stated that dielectric loss occurs when the electrical polarization in the dielectric cannot follow the varying electric field. An applied field can change this energy difference by producing a net polarization which lags behind the applied field because the tunnel transition rates are finite. This kind of the polarization which is not in

phase with the applied field is called dielectric loss [55]. As can be seen from the $\tan \delta - \ln(\omega)$ graphs in Fig. 12, $\tan \delta$ values decrease at low frequencies, remain almost constant at moderate frequencies and increase with increasing frequency at high frequencies. It can also be said that $\tan \delta$ values increase with increasing bias voltages. These results reveal that the $\tan \delta$ parameter is closely related to conductivity. The increase in electrical conductivity can be explained by the increase in eddy currents. While the values of the ϵ' , ϵ'' and $\tan \delta$ parameters changed in almost the same magnitude and style for D0, D1 and D2, their values decreased significantly in the case of D3. Therefore, the changes of M' and M'' parameters obtained from ϵ' and ϵ'' data in the range 30 kHz–3000 kHz frequency with varied voltages from -2 V to 4 V can be seen in Figs. 13–16 (a). The M'' -V changes are given in inset of these graphs. Graphs of M'' versus M' are also given in Figs. 13–16 (b). The applied bias voltage and frequency dependence of these modulus values is clearly seen in the graphs. From these profiles, it can be said that both components of complex electric modulus are sensitive to changes in frequency. In fact, the observed spectra of ϵ' and ϵ'' shown in Figs. 10 and 11 are the indication of such frequency and voltage dependent profiles of M . The values of M' decrease significantly with increasing forward bias voltages. It can be seen in inset Figs. 13–16 that the M'' -V plots have a peak at 0.11 , -0.05 , -0.21 and -0.05 V applied bias voltages for D0, D1, D2 and D3, respectively. The values of M' and M'' reach a maximum constant value corresponding to $M_\infty = \frac{1}{\epsilon_\infty}$ due to the relaxation process. The frequency dependence of the complex electrical modulus components can be interpreted by the contribution of interface trap charges which are effective in depletion and accumulation regions. These results can be attributed to the specific distribution of charges in the surface states and relaxation times due to thermal annealing [56,57]. The changes of M'' versus M' are plotted in Figs. 13–16 (b) at discrete excitation frequencies within 30–3000 kHz. Generally, while M' values increase for all frequency values, M'' values increase and reach a maximum value and then decrease again. That is, the changes for M'' versus M' are almost semicircular, and the reduction in the radii of these diagrams explains the change in the conductivity of the space charge region in the device. Additionally, semicircle width is the value of the recombination resistance and the maximum imaginary impedance corresponds to the product from which the electron lifetime was calculated [52].

Figs. 17–20 shows the σ_{ac} -V, σ_{ac} - $\ln(\omega)$ and $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots obtained from the G/ω -V data of the $Au/ZnS/n$ -GaAs/In structure as a function of applied bias voltage and frequency for D0, D1, D2 and D3, respectively. As stated above, the ac conductivity is directly proportional to dielectric loss. From these graphs it is clear that, σ_{ac} is dependent on the frequency and applied bias voltage. The values of ac electrical conductivity increase with increasing frequency and they have a maximum value in accumulation region. This increase is the result of the increasing eddy current, that cause increases the energy $\tan \delta$ [58]. It can be seen from the σ_{ac} -V plots that the conductivity is nearly frequency independent at low frequency (up to 500 kHz). However, as the frequency increases from 500 kHz to 3000 kHz the conductivity becomes more and more frequency dependent. The basic fact that ac conductivity in disordered solids is a function of increasing frequency is well known from solid state physics. Since transport takes place on infinite paths, the ac conductivity is nearly constant at low frequencies. At regions where the conductivity is strongly dependent on frequency, the transport is dominated by contributions from hopping infinite clusters. Then, the region of saturation is reached where the high frequency cutoff begins to play a role [59]. Compatible with the change in the G/ω -V plots, while the change of σ_{ac} values in D0, D1 and D2 are almost the same, in D3 its values has decreased significantly. The σ_{ac} - $\ln(\omega)$ plots at various positive bias voltages are given in inset Figs. 17–20 (a) for D0, D1, D2 and D3, respectively. It can be seen from these graphs that σ_{ac} values increase almost exponentially with increasing both frequency and positive bias voltages for D0, D1 and D2, respectively. However, in D3, the change in

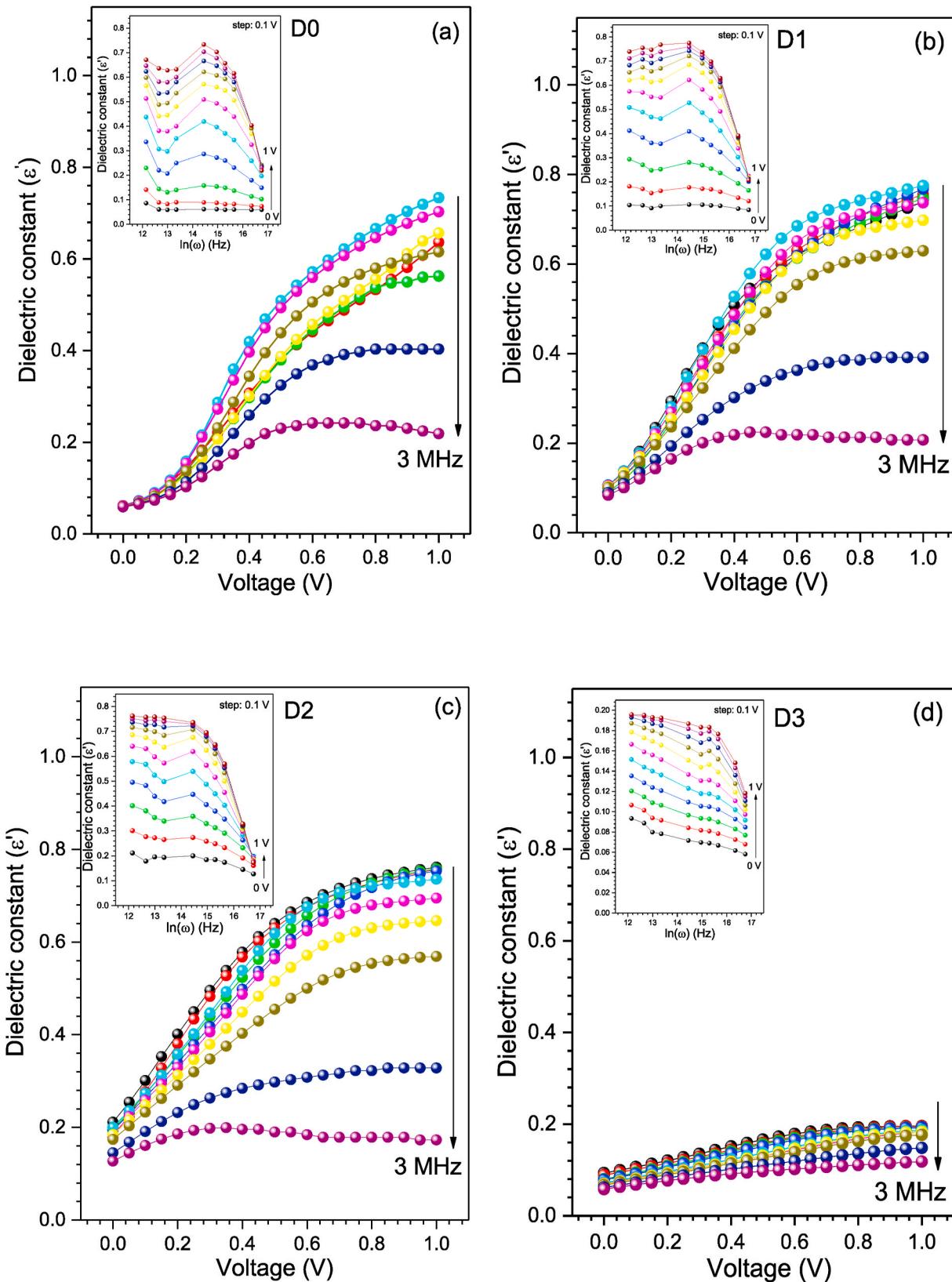


Fig. 10. The ϵ' - V plots of the $\text{Au}/\text{ZnS}/n\text{-GaAs}/\text{In}$ structure at various frequencies for (a) D0, (b) D1, (c) D2 and (d) D3. The ϵ' - $\ln(\omega)$ changes are given in inset of the graphs.

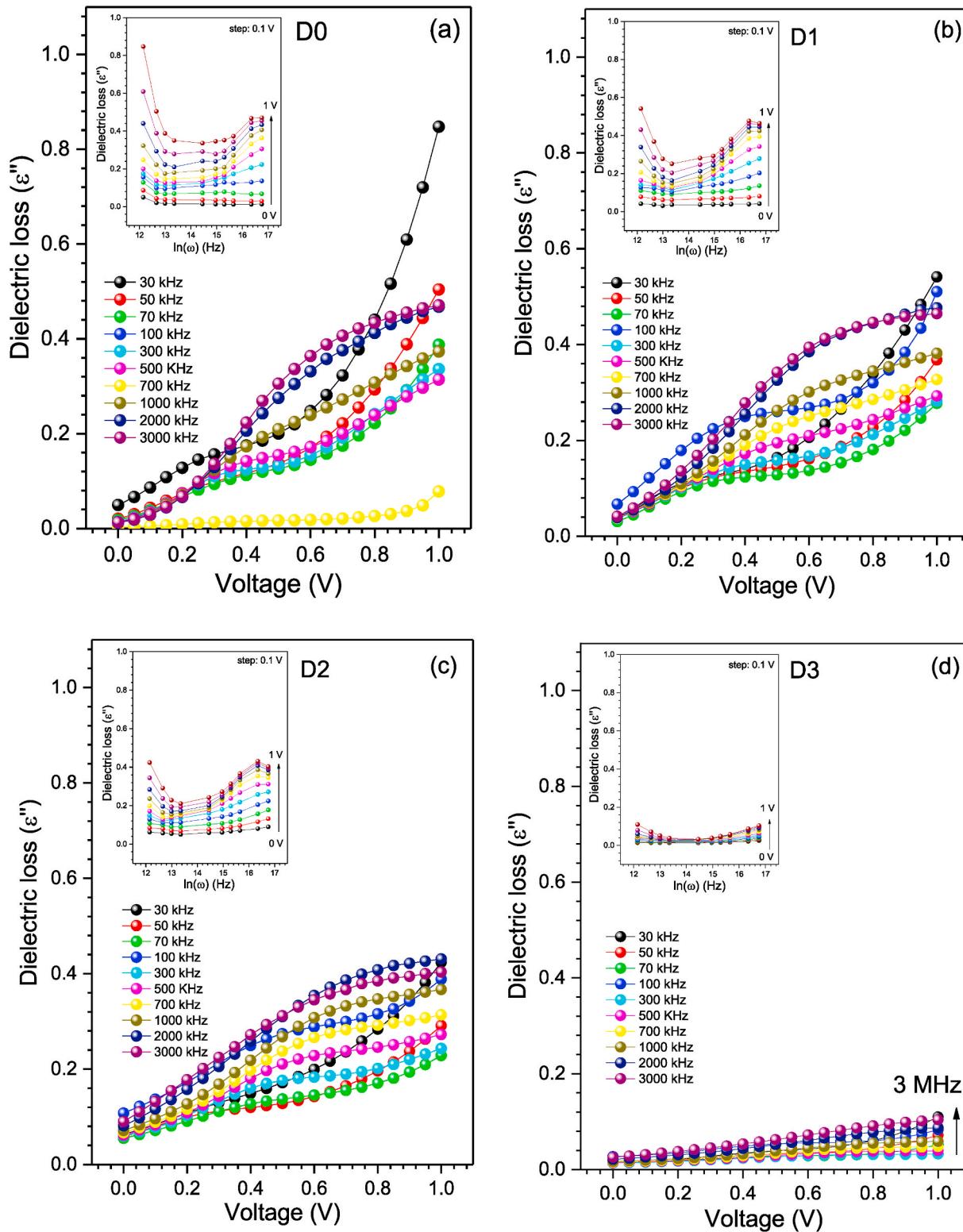


Fig. 11. The ϵ'' -V plots of the Au/ZnS/n-GaAs/In structure at various frequencies for (a) D0, (b) D1, (c) D2 and (d) D3. The ϵ'' - $\ln(\omega)$ changes are given in inset of the graphs.

the σ_{ac} values is less. We can say that the increase in σ_{ac} values with increasing frequency is caused by the relaxation phenomenon due to mobile charge carriers and charge hopping mechanism. Likewise, the change in ac conductivity with frequency can also be caused by polarization effects [54]. Figs. 17–20 (b) shows the $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0–4 V for D0, D1, D2 and D3, respectively. In all graphs, while

there is a single slope with linear change at low voltages, two linear regions with different slopes are observed at large voltages. Based on these results, we can say that dc conductivity is dominant in regions where the conductivity is almost independent of frequency, and ac conductivity is more dominant in other regions.

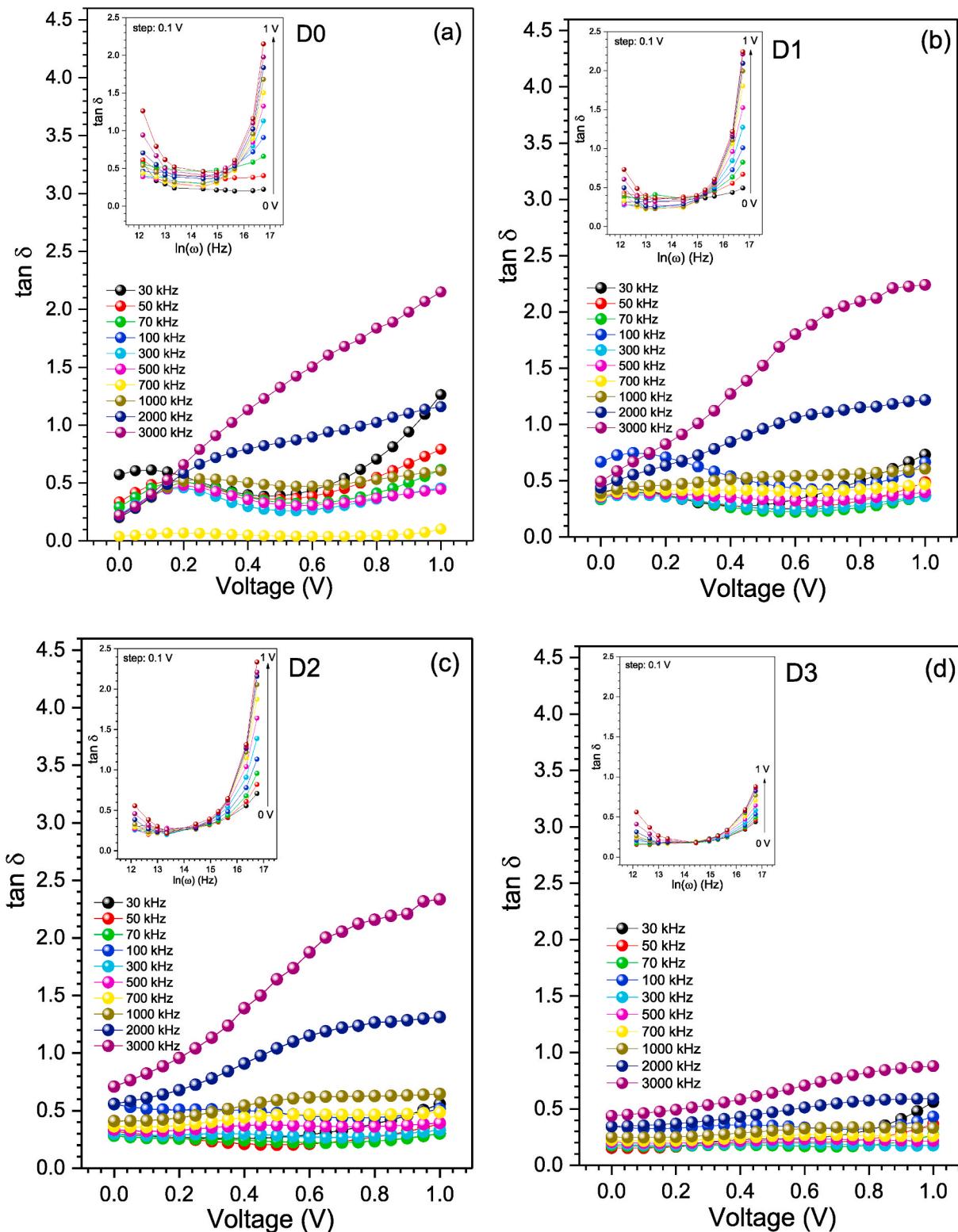


Fig. 12. The $\tan \delta$ - V plots of the $Au/ZnS/n$ -GaAs/In structure at various frequencies for (a) D0, (b) D1, (c) D2 and (d) D3. The $\tan \delta$ - $\ln(\omega)$ changes are given in inset of the graphs.

4. Conclusions

To investigate the current conduction mechanism and the interface nature of the $Au/ZnS/n$ -GaAs/In structure produced under laboratory conditions, the forward and reverse bias I - V , C - V and G/ω - V characteristics of this structure were studied in the room temperature

depending on thermal annealing at 100, 200 and 300 °C, respectively. From XRD, SEM and absorption measurements, it was determined that the ZnS thin film is in hexagonal crystal structure, covers the surface of the n -GaAs substrate almost homogeneously and the forbidden energy gap is 3.83 eV. From the analysis of the I - V characteristics, it was determined that while the diode turn-on voltage, leakage current and

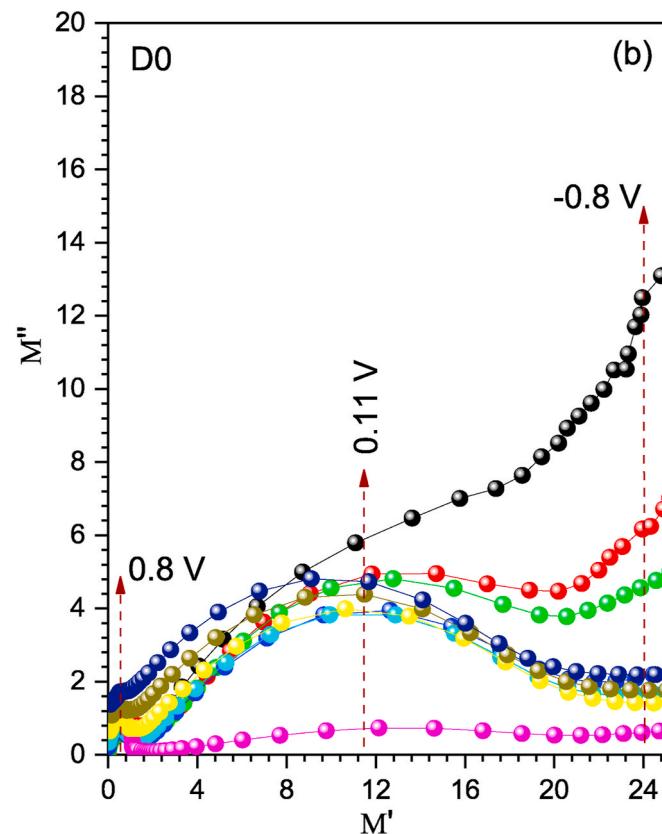
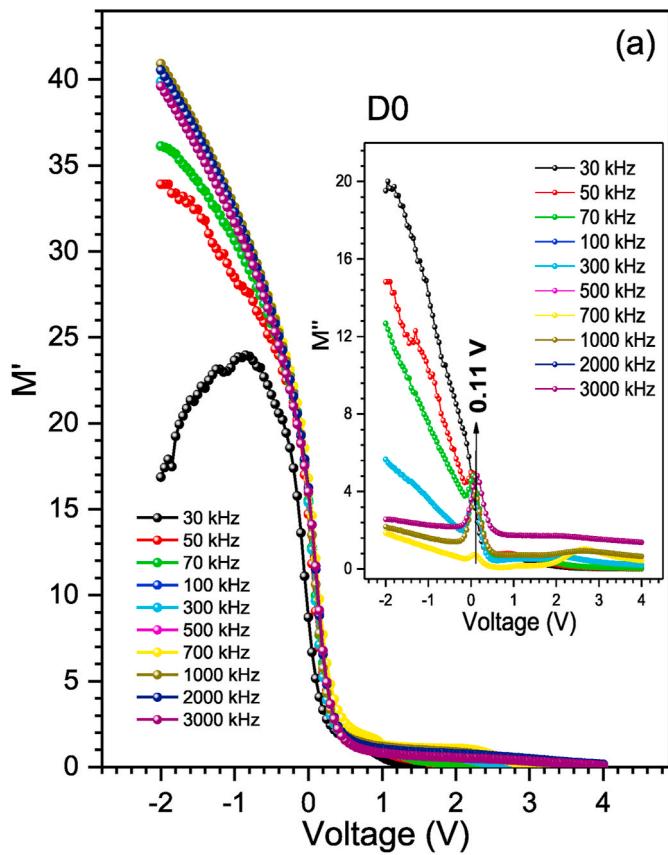


Fig. 13. a) The M' - V and M'' - V plots of the $Au/ZnS/n$ -GaAs/In structure as a function of voltage at various frequencies b) Changes of M'' versus M' for D0.

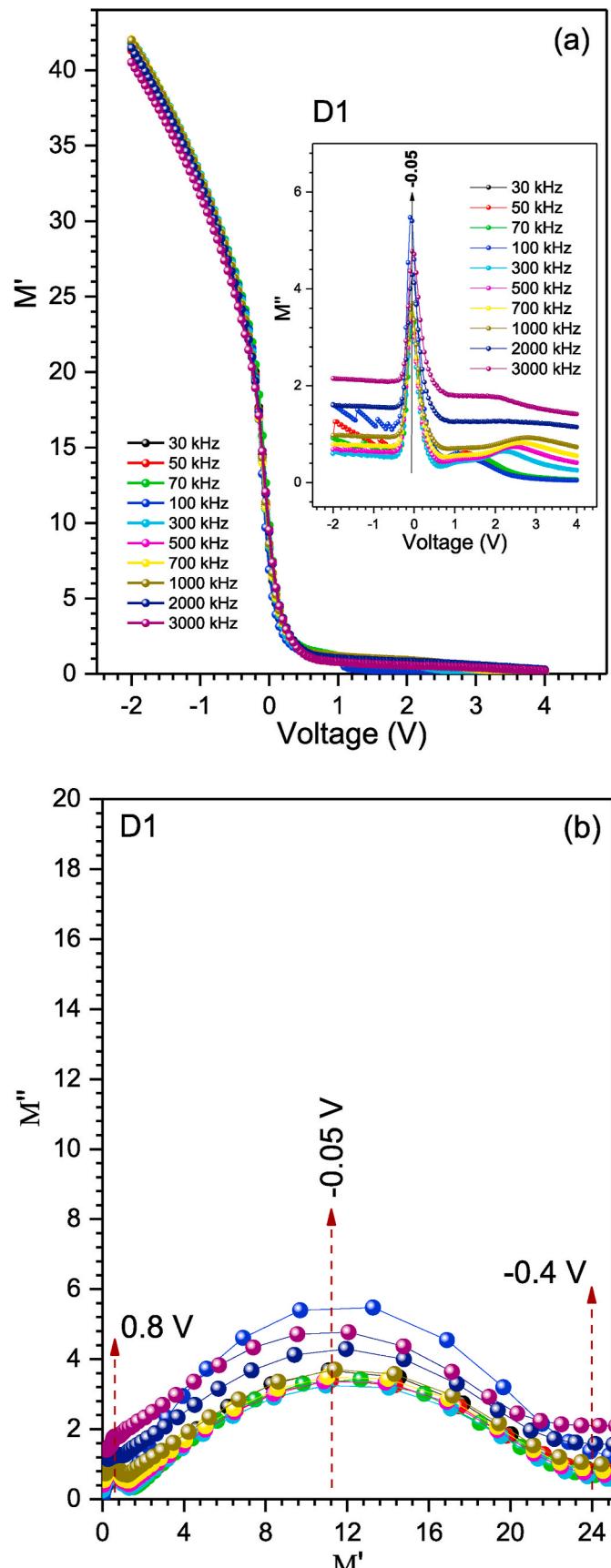


Fig. 14. a) The M' - V and M'' - V plots of the $Au/ZnS/n$ -GaAs/In structure as a function of voltage at various frequencies b) Changes of M'' versus M' for D1.

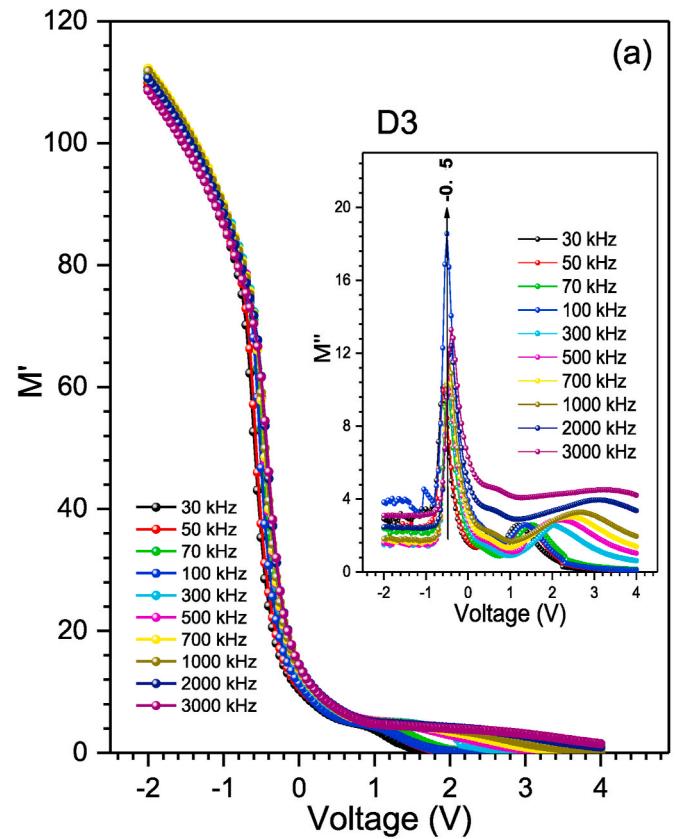
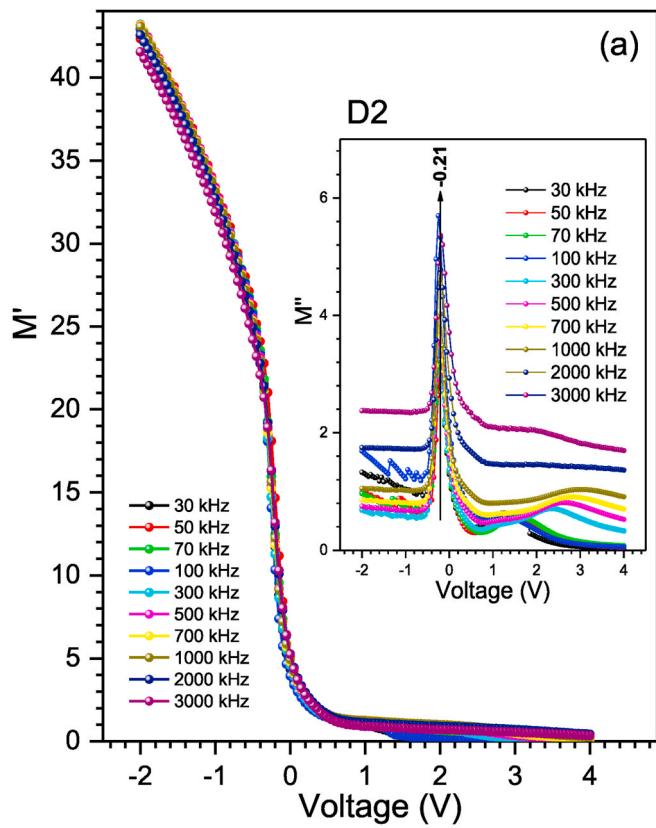


Fig. 15. a) The M' - V and M'' - V plots of the $Au/ZnS/n$ -GaAs/In structure as a function of voltage at various frequencies b) Changes of M'' versus M' for D2.

Fig. 16. a) The M' - V and M'' - V plots of the $Au/ZnS/n$ -GaAs/In structure as a function of voltage at various frequencies b) Changes of M'' versus M' for D3.

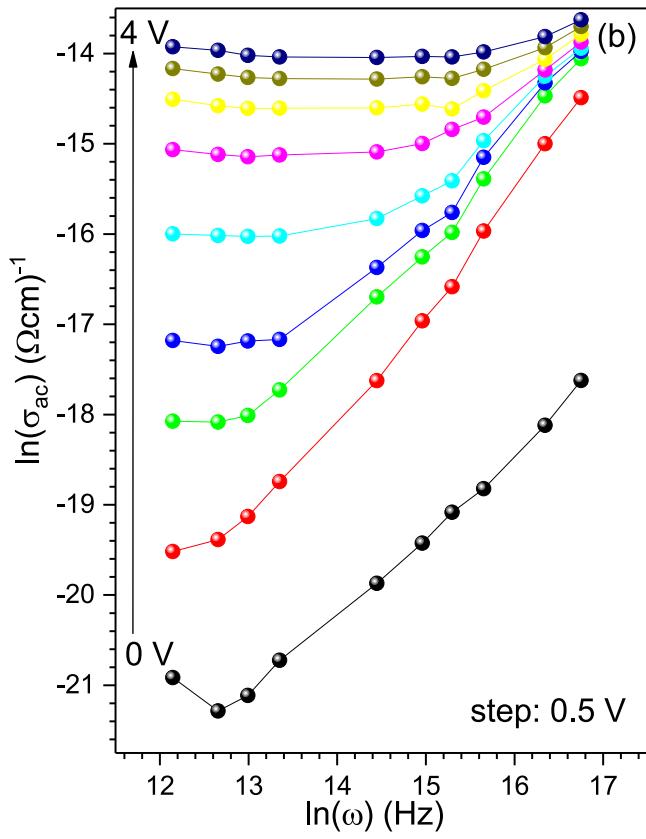
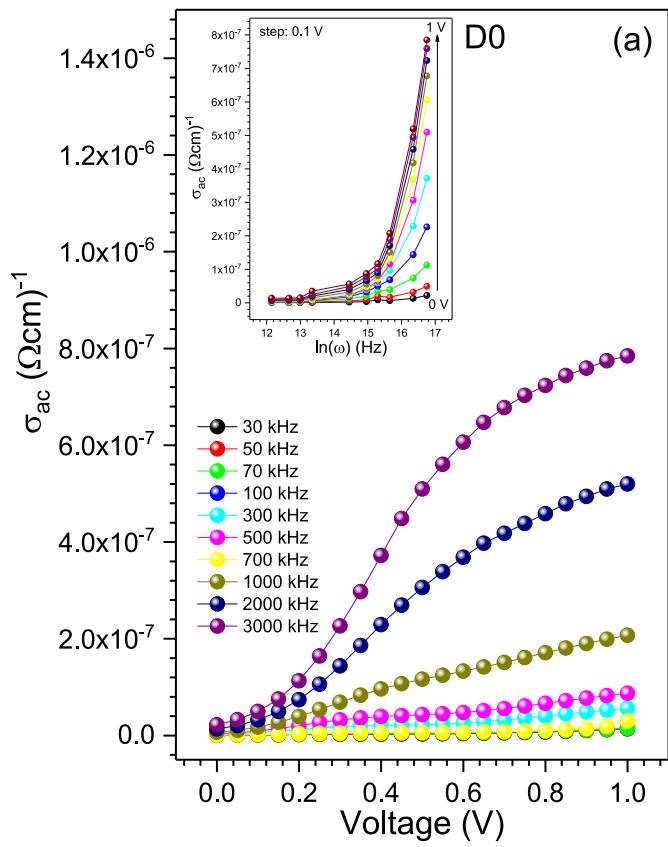


Fig. 17. For D0 at $T = 300$ K a) The σ_{ac} - V plots of structure depending on the frequency. The σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0–4 V of structure.

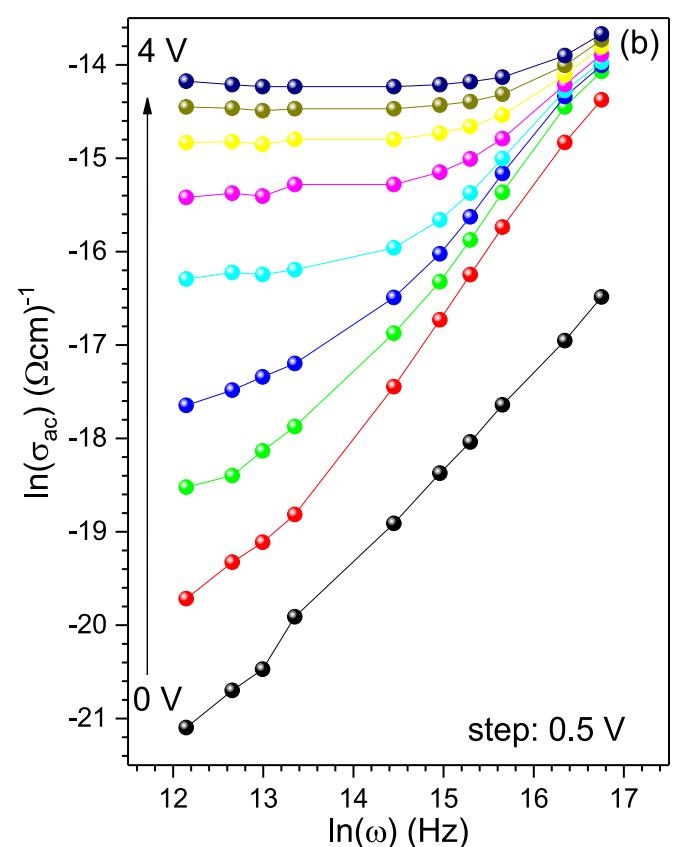
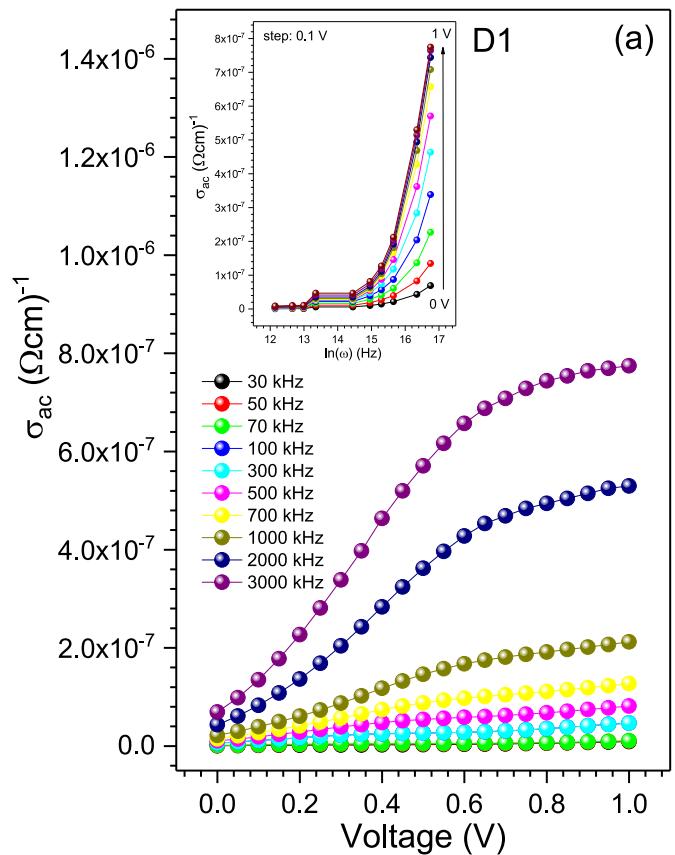


Fig. 18. For D1 at $T = 300$ K a) The σ_{ac} - V plots of structure depending on the frequency. The σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0–4 V of structure.

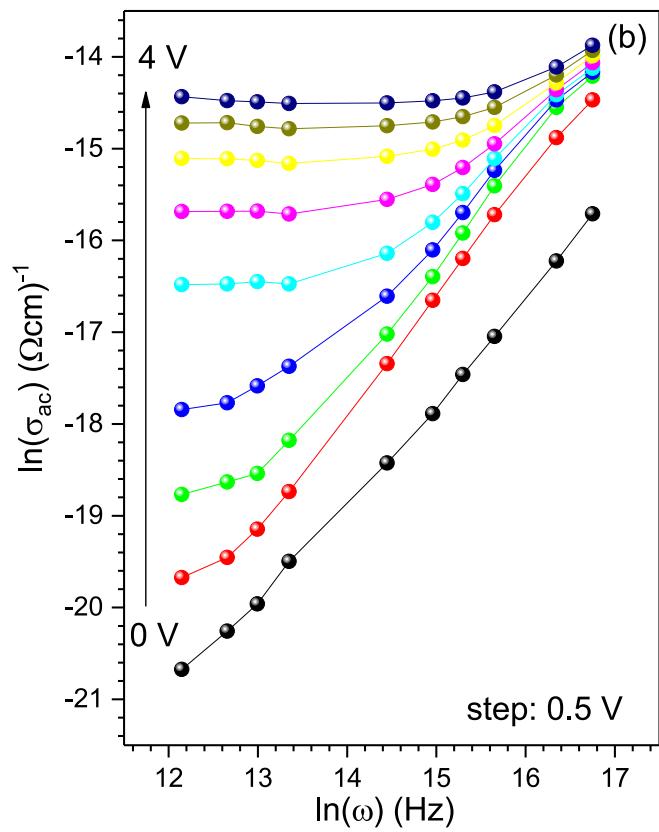
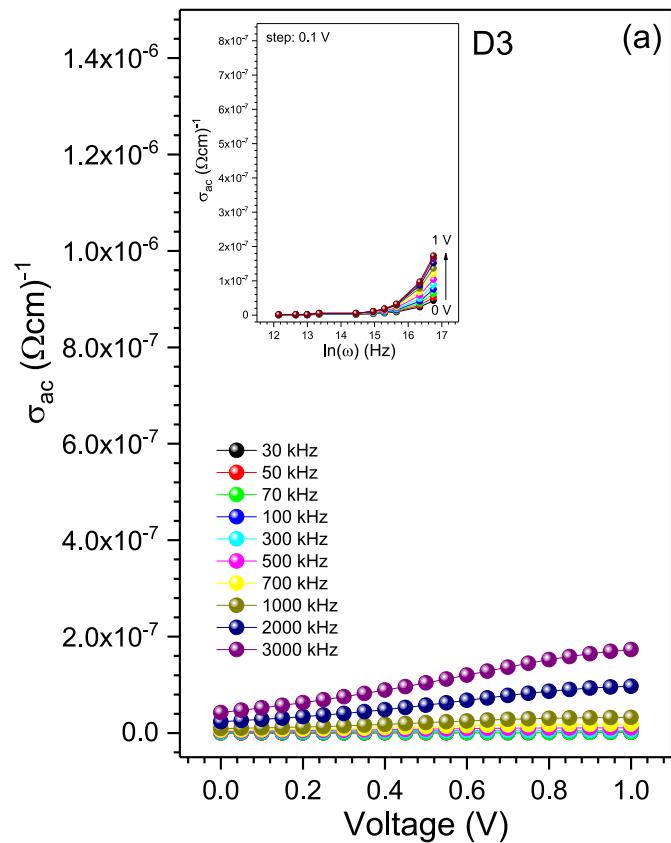
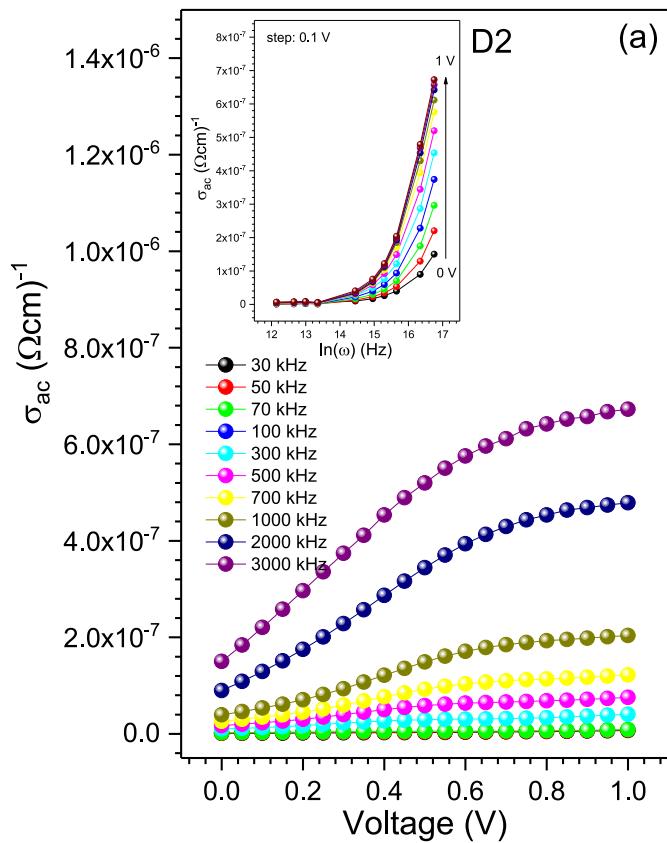


Fig. 19. For D2 at $T = 300$ K a) The σ_{ac} - V plots of structure depending on the frequency. The σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0–4 V of structure.

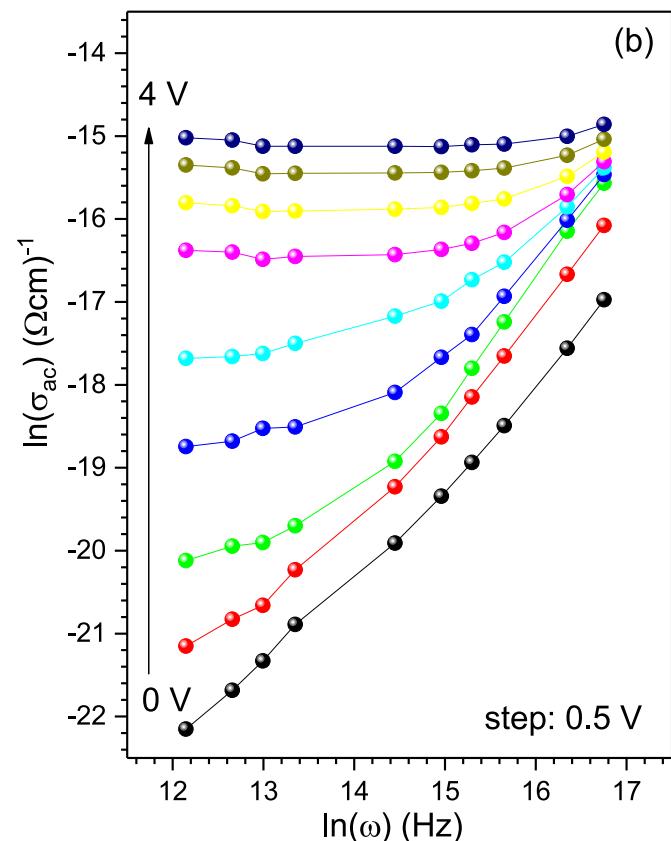


Fig. 20. For D3 at $T = 300$ K a) The σ_{ac} - V plots of structure depending on the frequency. The σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0–4 V of structure.

ideality factor values were decreased by thermal annealing up to 200 °C, barrier height and rectification ratio values were increased. From the C–V characteristics, diode parameters such as V_n , N_d , V_d and Φ_b have been calculated based on thermal annealing as a function of frequency. At the same time, both the frequency and voltage dependent of the ϵ' , ϵ'' , M' , M'' , $\tan \delta$ and σ_{ac} values of this structure were investigated by using the C–V and G/ω –V measurements in the frequency range of 30–3000 kHz. It has been observed that all of these parameters are strongly dependent on frequency and voltage. While the values of the ϵ' , ϵ'' and $\tan \delta$ parameters changed in almost the same magnitude and style for D0, D1 and D2, their values decreased significantly in the case of D3. These results may be most likely associated with the deterioration of the surface homogeneity of the film due to changes in film stoichiometry, and hence renewed defects and interface conditions. The change in ac conductivity with frequency has also been attributed to polarization effects within the device. It has been revealed that the optimum thermal annealing temperature for this device is 200 °C.

Credit author statement

A. Baltakesmez, Conceptualization, Methodology, Investigation. **B. Güzeldir**, Conceptualization, Visualization, Investigation, Writing-reviewediting. **M. Sağlam**, Conceptualization, Visualization, Investigation, Writing – review & editing. **M. Biber**, Methodology, Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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