Separation and analysis of diffusion and generation components of *pn* junction leakage current in various silicon wafers

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An analytical method to separate the diffusion and generation components of *pn* junction leakage currents is developed. The voltage dependence between reverse current and capacitance in *pn* junctions is measured, and an approximately linear relationship between current density (J) and depletion width (W) is derived. In this relationship, the diffusion component corresponds to linearly extrapolated value of J at $W=0$, and the generation component corresponds to the rate at which J increases with W as voltage is applied. This method allows both components of the leakage current to be obtained for Czochralski, epitaxial, and intrinsic gettering wafers. Separated diffusion components strongly depend on silicon wafers mainly due to the change of minority carrier density and the diffusion of minority carriers. On the other hand, the generation component increases with increases in the electric field applied to the junction for all wafers. We found that this electric field effect on the generation component can be explained by the Poole–Frenkel mechanism.

I. INTRODUCTION

The leakage current of *pn* junctions is one of the main parameters affecting the performance of devices such as photodiodes, charge coupled devices (CCDs), and dynamic random access memories (DRAMs). It is also related to the fundamental properties of silicon materials such as recombination lifetime, generation lifetime, and surface recombination velocity. It is well known that there are three major components in *pn* junction leakage: diffusion, generation, and surface generation components. The first two components are proportional to the area of the junction, and thus are called area components. The latter is proportional to the perimeter of the junction, and is thus called a perimeter component. Area and perimeter components can be separated by using junctions with the same area and different perimeters, as is well known.[1] However, it is not possible to separate the two area components, and only one of them is considered to dominate by the results of temperature dependence measurements.[2]

In this study, we develop a simple method to separate the diffusion and generation components of *pn* junction leakage current by measuring the voltage dependence of current and capacitance. By applying this method, the two components of *pn* junction leakage current were calculated for Czochralski (CZ), intrinsic gettering (IG), and epitaxial (EPI) wafers and the physical meaning of the differences in each components in various wafers were examined.

II. SEPARATION OF DIFFUSION AND GENERATION COMPONENTS

The three major components of *pn* junction leakage current are expressed as follows:

(1) Diffusion component

$$J_{\mathrm{diff},n}=qD_n\frac{n_i^2}{N_A L_n}\left[\exp\left(\frac{qV}{kT}\right)-1\right], \tag{1}$$

where q is the electron charge, D_n is the diffusion constant of electrons, n_i is the intrinsic carrier density, N_A is the acceptor density, and L_n is the diffusion length of electrons.

(2) Generation component

$$J_g=q\frac{n_i}{\tau_g}W\left[\exp\left(\frac{qV}{2kT}\right)-1\right], \tag{2}$$

where τ_g is generation lifetime and W is the depletion width.

(3) Surface generation component

$$J_{sg}=qS_0 n_i W_S\left[\exp\left(\frac{qV}{2kT}\right)-1\right]L/A, \tag{3}$$

where S_0 is the surface recombination velocity and W_s is the depletion width at the Si/SiO_2 interface, L is the perimeter length of the junction, and A is the junction area.

The diffusion current is caused by generation in the neutral region and diffusion to the depletion region, as derived by Shockley.[3] The generation current is caused by generation in the depletion region, as derived by Sah *et al.*[4] The surface generation current is caused by generation in the depletion region at the Si/SiO_2 interface, and is discussed comprehensively by Grove and Fitzgerald.[5] Although the latter component is dominant in small junctions, in this study we will consider relatively large junctions (1.8 mm square), neglecting the third component.

By comparing Eqs. (1) and (2), it can be seen that these formulae should differ in terms of the dependence of current on temperature and voltage. As is well known, measuring the temperature dependence and calculating the

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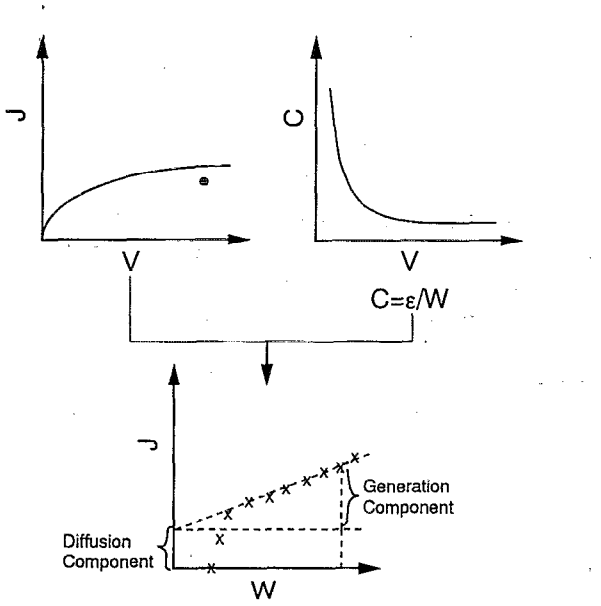

FIG. 1. Schematic representation of the separation of diffusion and generation currents using a J-W plot.

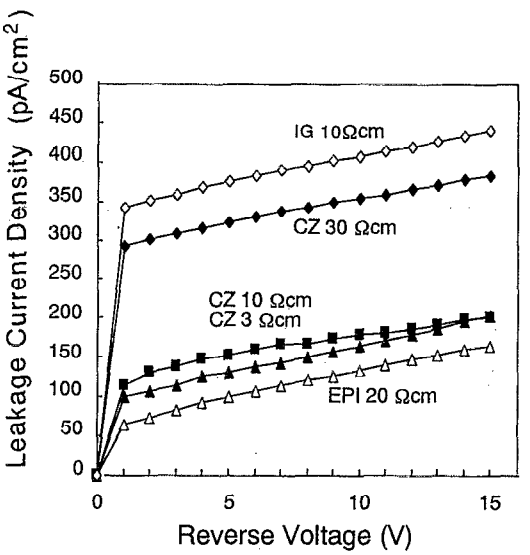

FIG. 2. J-V characteristics of reverse biased n^+p junctions formed in CZ, EPI(p/p^+), and IG wafers.

current activation energy is one way of determing whether diffusion or generation is the dominant process. In typical pn junctions used in the sources or drains of metal oxide semiconductor field effect transistors (MOSFETs), it is known that the generation component is dominant. However, at relatively low substrate densities or low diffusion lengths (IG wafer), both components are significant at a certain temperature. In this study, we propose another way of separating the two components, which involves identifying their differing contributions to the voltage dependence. If $V > kT/q$ is valid, the exponential factors in Eqs. (1) and (2) can be neglected under reverse bias conditions. With this approximation, the generation component is proportional to W, whereas the diffusion component is independent of W. Consequently, if a J-W plot can be obtained, the diffusion component corresponds to the extrapolated value of J at $W=0$, and the generation component corresponds to the rate at which J increases with W, when a reverse bias voltage is applied, as explained schematically in Fig. 1. To obtain W at a certain voltage, high frequency capacitance-voltage (C-V) measurements can be used with the relation $C=\epsilon/W$. As a result, the diffusion and generation components can be separated using a J-W plot produced by J-V and C-V measurements.

III. EXPERIMENTS

The silicon wafers used in this experiment were 5 in. B-doped p-type wafers with (100) orientation. Some were CZ wafers with a registivity of 1, 10, and 25 Ω cm, respectively. The other was an EPI wafer with a resistivity of 20 Ω cm, a P^+ substrate with a registivity of 0.01 Ω cm, and the thickness of epitaxial layer 17 μm. In IG wafer heat treatment was applied by subjecting the wafers to an atmosphere of N_2 for 60 min at 1150 °C, followed by ramping from 550 to 950 °C to form nuclei of oxygen precipitates, and 24 h at 1000 °C in O_2 to grow the oxygen precipitates, as a result denuded zone of 26 μm and defect region having bulk micro defects (BMD) of 7×10^9 cm^{-3} are formed. n^+p junctions were formed by $POCl_3$ solid-state diffusion, and a 600 nm field oxide layer was formed for the diffusion mask at 1100 °C for 110 min in wet O_2. Phosphorus was then deposited at 900 °C for 20 min, followed by a drive-in process at 1000 °C for 60 min in wet O_2, which results in junction depth with 2 μm. Al(1.5% Si) electrodes were formed by sputtering, and Al gate-controlled (guard ring) diode structures[2,6] were used to suppress the effects of channel currents due to surface inversion instead of local oxidation of silicon (LOCOS) isolation. J-V and C-V measurements were made using a current meter, and a capacitance meter, respectively.

IV. RESULTS AND DISCUSSION

Figure 2 shows the measured J-V characteristics of reverse biased n^+p junctions in various kinds of wafers. In the current-voltage (I-V) measurement, voltage was applied from 15 to 0 V with 1 V voltage step. Hold time was 60 s at 15 V and step delay time was 1 s at each voltage steps. Figure 3 shows the J-W plot calculated from the J-V and C-V measurements. As discussed above, these plots show approximately linear relationships. The leakage current is lower for the epitaxial wafer and higher for the IG wafers than it is for the CZ wafers, and also that depends on the resistivity(doping density) of the substrates. It is clear from this figure that even for the same depletion width, leakage current depends on the characteristics of the wafers. By using J-W characteristics, both components can be separated, furthermore, the gradient g and intercept J_{diff} at $W=0$ make it possible to calculate the generation lifetime (τg) and recombination lifetime (τr) using the following relationships:

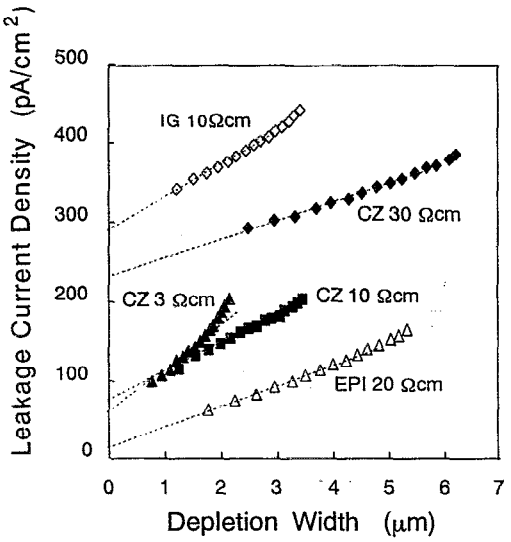

FIG. 3. *J-W* plots calculated from *J-V* and *C-V* measurements of CZ, EPI(p/p^+), and IG wafers

$$\tau_g=\frac{qn_i}{g}, \quad \tau_r=\frac{q^2n_i^4}{J_{\text{diff}}^2 N_A^2} D_n. \tag{4}$$

These calculated values are listed in Table I, and correspond to the values measured by other techniques such as MOS *C-t*, step recovery, and the photoconductive decay method.[7] Because this method involves steady state measurements, it has the advantage that it takes less time than other transient techniques. We will discuss the physical meaning of the differences in each component in the next sections.

A. Analysis of diffusion components

In CZ wafers, the diffusion component is smaller when resistivity is lower (higher doping) as summalized in Table I. As is well known, the differences between the diffusion components can be explained quantitatively by the proportionality between the diffusion component and the minority carrier density in equilibrium (n_{p0}) and by the relationship $n_{p0}=n_i^2/N_A$, where n_i is intrinsic carrier density, between this carrier density and the doping density of the substrate (N_A). Although calculated τ_r are a little small for 3 Ω cm wafer, those are nearly the same for CZ wafers having different resistivity.

The diffusion component is smaller in the epitaxial wafer than it is in the CZ wafers as a result of heavily doped region. On the other hand, that of IG wafers is made large as a result of bulk microdefects. These experimental results are consistent with the results in an earlier paper.[8] We also proposed earlier[9] that Schockley formula in (1) cannot be applicable in case of IG, EPI, and silicon on insulator-(SOI) wafers, and derived modified expression of Schockley formula as follows, by solving the diffusion equation of minority carriers assuming the continuity of charge and current at the boundaries

$$J_{\text{diff},n}=qD_n\frac{n_i^2}{N_A L_n}\left[\exp\left(\frac{qV}{kT}\right)-1\right]F. \tag{5}$$

Here, we call F a correction factor. As discussed in detail in the article, F can be approximated for IG and EPI wafers, respectively.

$$F\sim\coth\left(\frac{D}{L_n}\right)(\text{IG wafers}), \tag{6}$$

$$F\sim\frac{N_A/N_A'-1+\exp(D/L_n)}{\exp(D/L_n)}(\text{EPI wafers}), \tag{7}$$

where D is the distance from the edge of the depletion region to the boundary between denuded zone and defect region for IG wafers, or between epitaxial layer(acceptor density N_A) and heavily doped region (acceptor density N_A'), and L_n is the diffusion length of minority carriers in denuded zone or epitaxial layer, respectively. When we assume 93 μm as a L_n of the DZ layer in the IG wafer, which is the L_n of CZ 10 Ω cm wafer, and D is estimated at 22 μm by the DZ layer width (26 μm), junction depth (2 μm), and depletion width (2 μm), F can be calculated to 4.3. Furthermore, when we assume 98 μm as a L_n of epitaxial layer, which is the L_n of CZ 30 Ω cm wafer (we neglected the small registivity difference here), and D is estimated to 13 μm by the epi layer width (17 μm), junction depth (2 μm), and depletion width (2 μm), F can be calculated to 0.12. These calculated values explain quanti-

TABLE I. Leakage current measured at $V=5$ V, and separated diffusion and generation component, and calculated recombination lifetime (τ_r), and generation lifetime (τ_g).

Wafer type	Total (pA/cm^2)	Diffusion (pA/cm^2)	Generation (pA/cm^2)	N_A ($\times10^{15}$ cm^{-3})	D_n[a] (cm^2/s)	L_n (μm)	τ_r (μs)	τ_g (ms)
CZ 3 Ω cm	125	55	70	4.6	29	38	0.51	4.1
CZ 10 Ω cm	150	70	80	1.7	33	93	2.6	5.8
CZ 30 Ω cm	325	225	100	0.55	36	98	2.7	9.3
EPI 20 Ω cm	95	20	75	0.72	34	790	185[b]	9.3
IG 10 Ω cm	375	290	85	1.7	33	23	0.15[c]	5.8

[a]These values were obtained in Ref. 2, Fig. 4-11.
[b]Effective lifetime due to heavily doped region.
[c]Effective lifetime due to defect region.

tatively how diffusion component is lower for P/P^+ epitaxial wafers and why that is higher for IG wafers compared to normal CZ wafers.

From the above results, the difference in the diffusion component of various wafers can be explained by considering the diffusion equation of minority carriers. No big difference was observed between τ_n (or L_n) of the CZ wafer, that of the epitaxial layer of the EPI wafer, and that of the DZ layer of the IG wafer.

B. Analysis of generation components

Another important feature of Fig. 2 is the different slopes of the J-W plot: The slope is greater when the resistivity is lower, which results in lower τ_g as shown in Table I. Furthermore, if we see the figure carefully, the J-W plot is not a straight line but increasing slightly with increasing W. The increment of leakage current with increasing depletion width corresponds to the generation component of leakage current, and the gradient corresponds to generation lifetime. These phenomena suggest that generation lifetime depends on the voltage applied to the junction. To see the voltage dependence of leakage current in detail, we analyzed the data as follows.

It has long been known[4] that the generation component of leakage current in a pn junction can be expressed as in Ref. 2. By the approximation at $|V| > kT/q$, the following approximation is valid:

$$J_g \sim q \frac{n_i}{\tau_g} W. \tag{8}$$

If the generation lifetime is a function of the depth of the depletion region, Eq. (1) can be written in the integral form:

$$J_g \sim q n_i \int_0^W \frac{dX}{\tau_g(X)}. \tag{9}$$

Differentiating both sides with respect to W, we have

$$\tau_g(W) = q n_i \epsilon_s \epsilon_0 \frac{d(1/C)/dV}{dJ_g/dV}, \quad W = \epsilon_s \epsilon_0 / C, \tag{10}$$

where C is capacitance per unit area, and where ϵ_0 and ϵ_s are the permittivities of vacuum and silicon, respectively. It should be noticed here that, if there is some amount of diffusion component in the leakage current, this component is automatically dropped by differentiating with V.

This expression can be used to measure the depth profile of generation lifetime $\tau_g(x)$ by using an n^+p or p^+n junction. A similar approach using a MOS capacitor[10] and a MOS tunnel diode[11] to measure the depth profile of generation lifetime of IG wafers and epitaxial wafers has already been reported. Figure 3 shows the depth profile of generation lifetime calculated by using Eq. (10).

If $\tau_g(x)$ can be assumed to be nearly constant at the surface region in silicon, however another important factor is the variation of electric field within the depletion region in the junction. The generation component J_g can be expressed as follows, given the simple relationship between electric field E and depletion width W under the constant doping density:

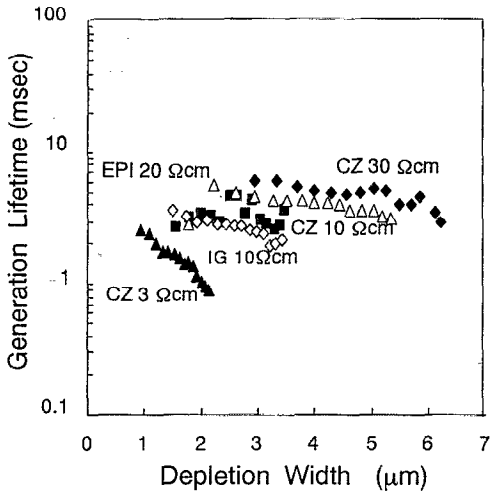

FIG. 4. Calculated depth profile of generation lifetime for CZ, EPI(p/p^+), and IG wafers.

$$J_g \sim \frac{\epsilon_s \epsilon_0 n_i}{N_A} \int_0^{E_{\max}} \frac{dE}{\tau_g(E)}, \quad E_{\max} = \frac{q N_A W}{\epsilon_s \epsilon_0}, \tag{11}$$

$$E(X) = -\frac{q N_A}{\epsilon_s \epsilon_0}(X - W), \tag{12}$$

where N_A is the acceptor density of the substrate. Again by differentiating both sides of the formula by W, we get

$$\tau_g(E) = q n_i \epsilon_s \epsilon_0 \frac{d(1/C)/dV}{dJ_g/dV}, \quad W = q N_A / C. \tag{13}$$

Figure 4 shows the electric field dependence of generation lifetime calculated from the leakage current by using Eq. (13). Significantly, the variation of generation lifetime with the increase of applied electric field is well fitted by the field dependence expected from the Poole–Frenkel-type field emission, and for all wafers the variation of generation lifetime with the change of substrate resistivity has approximately the same slope, suggesting that the resistivity dependence of generation lifetime can be explained by the same Poole–Frenkel mechanism.

In general, generation lifetime is a function of both x and E, so the separation of these contributions is not possible. Paz and Schneider[12] considered both effects: the field effect and the depth profile effect on the measurement of generation lifetime by using a MOS capacitor. We, however, speculate that the effect of the depth profile is negligible in our experiments, since the generation lifetime for various kind of wafers—such as CZ, EPI, IG—all show similar Poole–Frenkel-type field dependence. We think that the depth profile seen in Fig. 4 is an artificial effect and the field dependence seen in Fig. 5 is a real effect.

As discussed by Hurkx *et al.*,[13] when the electric field is strong, Zener tunneling or trap-assisted tunneling is dominant, but when the field is weak, the Poole–Frenkel

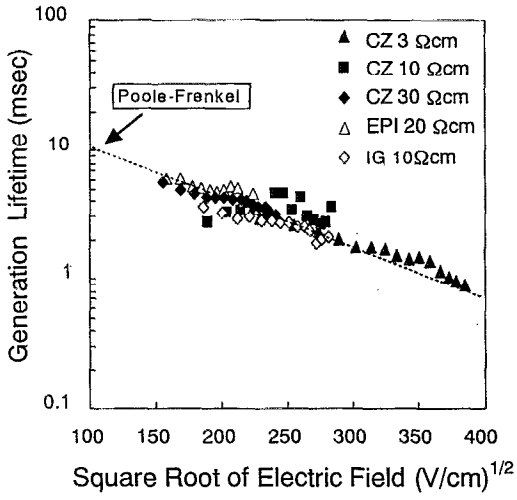

FIG. 5. Electric field dependence of generation lifetime calculated from the measured leakage current of CZ, EPI(p/p^+), and IG wafers.

effect can greatly increase the emission probability.[14] This field dependence means that in both CZ and EPI wafers the localized state controlling the generation lifetime has a Coulomb-type potential, although the physical origin of this control is not yet known.

Judging from the above results, the defects which are responsible for the generation may not be the kinds of crystal defects which are characteristic in CZ or EPI crystals, but can be metal impurities contained in both CZ and EPI wafers.

V. CONCLUSIONS

We have developed a simple analytical method to separate the diffusion and generation components of *pn* junction leakage current. Using this method, it is possible to make a more precise characterization of *pn* junction leakage in LSI processes. This technique also makes it possible to estimate the lifetimes in silicon materials.

The differences in diffusion components can be understood quantitatively by considering the diffusion equation of minority carriers. On the other hand, the voltage dependence of the generation component of *pn* junction leakage current can be explained by the Poole–Frenkel effect. Consequently, the effect of various substrate wafers on the leakage current of *pn* junctions can be analyzed by both the differences in diffusion components and generation components.

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[1] K. Ohyu, T. Itoga, Y. Nishioka, and N. Natsuaki, Jpn. J. Appl. Phys. **28**, 1041 (1989).
[2] A. S. Grove, *Physics and Technology of Semiconductor Devices* (Wiley, New York, 1967).
[3] W. Shockley, Bell Sys. Tech. J. **28**, 435 (1949).
[4] C. T. Sah, R. N. Noyce, and W. Shockley, Proc. IRE **45**, 1228 (1957).
[5] A. S. Grove and D. J. Fitzgerald, Solid State Electron. **9**, 783 (1966).
[6] T. Giebel and K. Goser, IEEE Electron Device Lett. **10**, 76 (1989).
[7] D. K. Schroder, IEEE Trans. Electron Devices **ED-29**, 1336 (1982).
[8] J. W. Slotboom, M. J. J. Theunissen, and A. J. R. de Kock, IEEE Trans. Electron Devices **EDL-4**, 403 (1983).
[9] Y. Murakami, H Abe, and T. Shingyouji (unpublished).
[10] P. U. Calzolari, S. Graffi, and C. Morandi, Solid State Electron. **17**, 1001 (1974).
[11] S. Kar, Appl. Phys. Lett. **25**, 587 (1974).
[12] O. Paz and P. Schneider, IEEE Trans. Electron Devices **ED-32**, 2830 (1985).
[13] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 331 (1992).
[14] G. Vincent, A. Chantre, and D. Bois, J. Appl. Phys. **50**, 5485 (1979).