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Structural, electrical, and surface morphological characteristics of rapidly annealed Pt/Ti Schottky contacts to n-type InP

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We have investigated the electrical and structural properties of Pt/Ti metallization scheme on n-type InP as a function of annealing temperature using current–voltage (*I–V*), capacitance–voltage (*C–V*), Auger electron spectroscopy (AES), and X-ray diffraction (XRD) measurements. Measurements showed that barrier height of as-deposited Pt/Ti Schottky contact is 0.62 eV (*I–V*) and 0.76 eV (*C–V*). Experimental results indicate that high-quality Schottky contact with barrier height and ideality factor of 0.66 eV (*I–V*), 0.80 eV (*C–V*), and 1.14 can be achieved after annealing at 400 °C for 1 min in N_2 atmosphere. Further, it is observed that the barrier height slightly decreases to 0.55 eV (*I–V*) and 0.71 eV (*C–V*) after annealing at 500 °C. Norde method is also employed to calculate the barrier height of Pt/Ti Schottky contacts. The obtained values are in good agreement with those obtained by *I–V* measurements. These results indicate that the optimum annealing temperature for the Pt/Ti Schottky contact is 400 °C. According to AES and XRD analysis, the formation of indium phases at the Pt/Ti/n-InP interface could be the reason for the increase of Schottky barrier height (SBH) after annealing at 400 °C. Results also showed the formation of phosphide phases at the interface. This may be the reason for the decrease in the barrier height after annealing at 500 °C. The AFM results showed that the overall surface morphology of Pt/Ti Schottky contact is reasonably smooth.

1 Introduction Indium phosphide (InP) has gained much attention recently due to its growing technological applications in practical devices such as high-speed field-effect transistors [1, 2], high speed charge-coupled devices [3], and electro-optics [4]. InP is an attractive substrate material for these devices because of its large electron mobility and large saturated drift velocity of electrons. Metal–semiconductor (M–S) contacts form the basic building blocks of the compound semiconductor technology. The performance of M–S contacts depends pre-dominantly on the choice of the metal, the doping density of the semiconductor and the quality of the semiconductor surface before the deposition of the metal. Schottky barrier contacts to n-type InP that have been investigated so far have all yielded barrier heights in the range of 0.33–0.55 eV [5–7]. Such a low barrier height gives rise to reverse leakage currents which are detrimental to device performance. In order to design contacts with improved thermal and electrical stability, as well as desirable morphologies, it is important to have a through understanding of the reactions of the contact metals with InP. A study of the reactions of metal/InP contacts can be useful for predicting and understanding the behavior of more complicated contacts, such as multi-component contacts to InP and contacts to alloy semiconductors that contain In and P. Intimate metal evaporation on n-type InP yields poor barrier height. Many investigations have been undertaken in order to improve the electrical behavior of the contact (a decrease of the leakage current, an increase of barrier height), which strongly depends on the semiconductor surface preparation and on the metal.

Several metal schemes have been used to form Schottky contacts to n-type InP in the past [8–20]. Some of them were thermally treated and the effects of annealing were studied. These studies, however, were mainly concerned with the stability of the Schottky barriers and characterizing their electrical property changes due to annealing. Sato et al. [9]

reported that the Pt/n-InP Schottky diodes formed by the electrochemical process gave higher SBH values (0.86 eV) than those formed by the conventional electron beam deposition process (0.44 eV). Jeng et al. [10] found that the barrier height of Ni/n-InP Schottky diode was enhanced with reduced reverse leakage current density after inserting a thin Pr interlayer between Ni and InP layers. Chen et al. [11] fabricated novel high-sensitive Pd/InP Schottky diode hydrogen sensors by electroless plating technique and reported that the electroless plated Pd/InP diode exhibits good rectification performances. Horvath et al. [12] reported that the best Schottky barrier height (SBH) of 0.83 eV was achieved for Au/n-InP Schottky diode using HCl:H_2O surface treatment. Huang and Cai [13] fabricated a high performance double metal Schottky structure on n-InP using Pt and Al. They reported that the electrical characteristics improved due to the formation of aluminum-oxide and the obtained barrier height was 0.74 eV. Cetin and Ayyildiz [14] fabricated Au, Al and Cu Schottky diodes on InP surfaces and investigated the influence of the air-grown oxide on the electrical performance. Bhaskar Reddy et al. [15] studied the influence of rapid thermal annealing (RTA) on electrical and structural properties of Pt/Au Schottky contacts to n-InP and they reported that the maximum barrier height was found to be 0.51 eV [current–voltage (*I–V*)] and 0.89 eV [capacitance–voltage (*C–V*)] for the contact annealed at 300 °C. They found that the formation of intermetallic compounds at the interface may be the reason for the increase of barrier height after annealing at 300 °C. Soylu et al. [16] investigated the effect of annealing on Au/pyronine-B/MD/n-InP Schottky diode. They reported that the barrier height and ideality factors were 0.60 eV and 1.041, 0.57 eV and 1.253 after annealing at 100 and 250 °C. Ashok et al. [17] studied the electrical, structural and morphological characteristics of rapidly annealed Pd/n-InP (100) Schottky structure. They reported that the formation of phosphorus–oxygen compounds at the interface may be responsible for the variation in barrier heights with annealing temperature. Cetin and Ayyildiz [18] prepared Au and Cu/n-InP Schottky diodes and reported that the effective barrier height of Au and Cu Schottky contacts were 0.48, 0.404 eV and 0.524, 0.453 eV from *I–V* and *C–V* measurements. Huang and Horng [19] investigated the electrical and structural properties of Pt/Al/n-InP Schottky diodes. They reported that the double metal contact structure provides better rectification characteristics than conventional single metal/n-InP Schottky diodes. Recently, Sankar Naik et al. [20] studied the effect of annealing temperature on electrical and structural properties of double metal structure Ni/V Schottky contacts to n-InP. They reported that the BH decreased with annealing temperature compared to the as-deposited one. They also found that the formation of phosphide phases at the interface may be the reason for decrease in the barrier heights upon annealing.

The main goal of the present work is to fabricate and investigate the electrical, structural, and surface morphological properties of Pt/Ti Schottky layers on n-type InP. In this work, titanium (Ti) is selected as the first Schottky layer because it has low work function as well as to provide the lowest forward voltage drop. Platinum (Pt) is used as the second Schottky layer because it has high work function, high reliability and high reactivity with InP. There is a serious lack of information about the effect of annealing, especially RTA, on the electrical characteristic of near noble metal/InP Schottky contacts. In the processing of integrated circuits, devices are usually subjected to annealing. From a device point of view, it is important to know what happens to metal contacts when they are annealed. The main purpose of this work is to explore the effects of RTA on the electrical, structural, and morphological characteristics of Pt/Ti Schottky contacts on n-type InP. In the present study, we used RTA because of its importance and emerging wide applications in the micro-electronic industry.

2 Experimental procedure

In the present work, Pt/Ti/n-InP Schottky diodes are prepared by using a cleaned and polished n-InP with (111) orientation [(Liquid Encapsulated Czochralski (LEC) grown undoped n-InP wafer] and carrier concentration is about $4.9–5.0 \times 10^{15}$ cm^{-3}. Before making the Ohmic contact, the samples are initially degreased with warm organic solvents like trichloroethylene, acetone, and methanol by means of ultrasonic agitation in sequence of 5 min each step to remove the undesirable impurities and followed by rinsing in deionized (DI) water. Thereafter, the samples are etched with HF (49%) and H_2O (1:10) to remove the native oxides from the substrate. The wafer is then dried with high-purity nitrogen and inserted into the deposition chamber immediately after the etching process. Ohmic contact of thickness 700 Å is formed with indium (In) on the unpolished surface (backside) of the InP wafer under a vacuum pressure of 8×10^{-6} mbar by thermal evaporation technique. To obtain, the low resistance Ohmic contact the samples are annealed by RTA at 350 °C for 1 min in nitrogen atmosphere. The samples are immediately loaded into the vacuum chamber of the e-beam evaporation system. Metal Ti and Pt layers were sequentially deposited on the InP substrate surface (polished side) in a vacuum of pressure 5×10^{-6} Torr. Ti layer thickness is ~20 nm and Pt layer thickness is ~30 nm. The diameter of the Schottky contact is 0.7 mm. The metal layer thickness and the deposition rates monitored with the help of a digital crystal thickness monitor. Various temperature anneals are used to study the thermal study of Schottky contacts. An RTA system is used in short-time annealing and the annealing temperature ranged from 200 to 500 °C. The annealing time is 60 s. The *I–V* and *C–V* characteristics of Pt/Ti Schottky contacts are measured using Keithly source measuring unit (Model No 2400) and automated DLTS (DLS-83D) system at room temperature. Auger electron spectroscopy (AES: UG: micro lab 350) depth profile has been performed to examine the intermixing of the metal and InP layers before and after annealing. X-ray diffraction (Siefert XRD PW 3710 using Cu K_α radiation) measurements have been made for Pt/Ti Schottky contacts to characterize the interfacial reactions between the metal and InP layers. Finally, atomic force microscopy (AFM) has also been employed to characterize the surface morphology of the Pt/Ti Schottky contacts before and after annealing temperature.

3 Results and discussion

3.1 Electrical properties of Pt/Ti Schottky contacts One of the most widely used methods to determine the SBH of an M–S contact is the *I–V* measurement. In an undoped semiconductor, the current I across a Schottky barrier diode (SBD) under bias voltage V with the zero-bias effective barrier height $q\phi_{\mathrm{bo}}^{\mathrm{eff}}$ is usually described by the thermionic emission theory [21]:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right], \tag{1}$$

where I_0 is the saturation current which is determined by

$$I_0 = AA^*T^2 \exp\left(\frac{-q\phi_{\mathrm{bo}}^{\mathrm{eff}}}{kT}\right), \tag{2}$$

where k is the Boltzmann's constant, T the absolute temperature, A the area of the diode, A^* the effective Richardson constant, $\phi_{\mathrm{bo}}^{\mathrm{eff}}$ the effective SBH at zero-bias, and n is the ideality factor. The theoretical A^* value of $9.4\,\mathrm{A\,cm^{-2}\,K^{-2}}$ is used for n-type InP [22]. The saturation current I_0 is determined by extrapolating the linear region of the forward-bias semi-log *I–V* curves to the zero applied voltage and the $\phi_{\mathrm{bo}}^{\mathrm{eff}}$ values are calculated from Eq. (2). From Eq. (2) we can write as

$$\phi_{\mathrm{bo}}^{\mathrm{eff}} = \frac{kT}{q}\ln\left(\frac{A^*AT^2}{I_0}\right). \tag{3}$$

The ideality factor n is a measure of conformity of the diode to pure thermionic emission and if n is equal to one, pure thermionic emission occur, However, n has usually a value greater than unity. The values of n were determined from the slope of the linear region of the forward bias *I–V* characteristics using the relation [21]

$$n = \frac{q}{kT}\frac{\mathrm{d}V}{\mathrm{d}(\ln I)}. \tag{4}$$

Note that n depends on the current flow at the interface and is equal to 1 for an ideal diode.

The *I–V* characteristics of the Pt/Ti/n-InP Schottky diodes (SBDs) as a function of annealing is shown in Fig. 1. The value of barrier height for the as-deposited Pt/Ti Schottky contact is calculated as 0.62 eV (*I–V*). The estimated SBHs for the samples annealed at 200, 300, 400, and 500 °C are 0.60, 0.63, 0.66, and 0.55 eV, respectively. It is noted that the barrier height increases with increase in annealing temperature up to 400 °C. However, the barrier height slightly decreases when the contact is annealed at 500 °C. A maximum barrier height of 0.66 eV (*I–V*) can be achieved for contact annealed at 400 °C for 1 min in N_2 atmosphere. For a typical as-deposited Pt/Ti Schottky contact, the leakage current is 4.236×10^{-6} A at -1 V, whereas for the contact annealed at 400 °C, it is observed that the leakage current slightly decreases to 1.123×10^{-6} A at -1 V. However, the leakage current is increased for the sample annealed at 500 °C and the corresponding value is 1.03×10^{-5} A at -1 V. It is found that the reverse leakage current decreases for the contact annealed at 400 °C. This indicates that the electrical properties are improved as compared to the as-deposited and annealed at 200, 300, and 500 °C samples. Based on the above results, the optimum annealing temperature for the Pt/Ti Schottky contact is 400 °C. The ideality factor is obtained from the plot of natural log of current *versus* forward bias voltage for small forward currents where the effect of series resistance is small. The calculated values are 1.51 for as-deposited, 1.40, 1.14, and 1.93 for the contact annealed at 300, 400, and 500 °C, respectively. The values of ideality factors are indicative of non-ideal behavior, suggesting the transport mechanisms, other than just thermionic, are probably present in these diodes. Our data clearly show that the diodes have ideality factor that is greater than 1. The higher values of ideality factor are probably due to the potential drop in the interface layer and the presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers [23]. The other reason for higher values of ideality factor n could be attributed to the inhomogeneous barrier height. Another possibility is that the ideality factor is higher than unity and this may be attributed to the oxide layer grown on the semiconductor, suggesting that the potential barriers at real M–S interfaces depend much more the applied voltage than predicted ideal contacts.

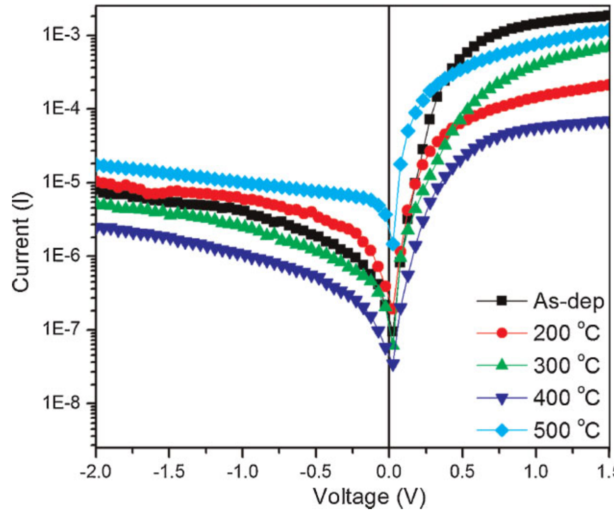

Figure 1 (online color at: www.pss-a.com) *I–V* characteristics of the Pt/Ti/n-InP Schottky structure as a function of annealing temperature.

The series resistance R_s is evaluated from the forward *I–V* measurements using a method developed by Cheung and

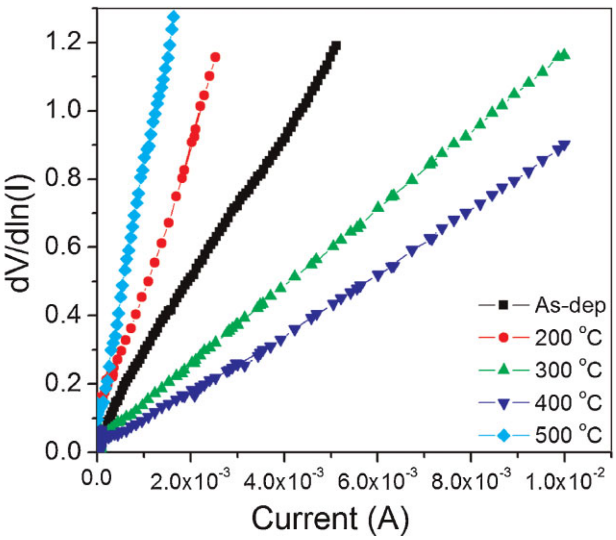

Figure 2 (online color at: www.pss-a.com) Plots of dV/dln(I) *versus* I for the Pt/Ti/n-InP Schottky diode as a function of annealing temperature.

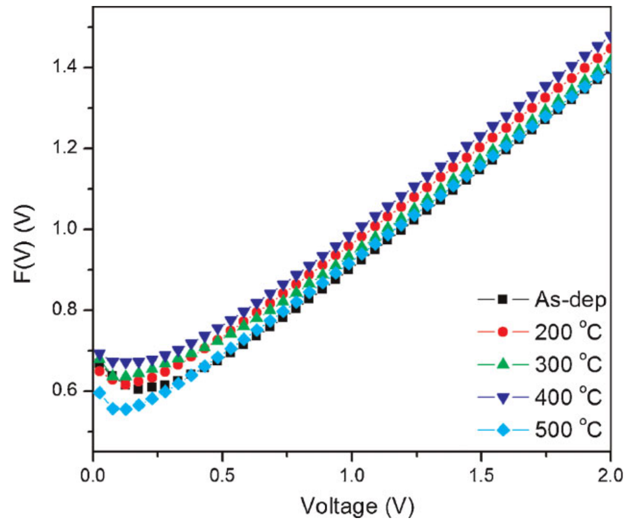

Figure 3 (online color at: www.pss-a.com) Plot of $F(V)$ *versus* V for Pt/Ti Schottky contacts to n-InP annealed at different temperatures.

Cheung [24]. The forward bias I–V characteristics due to thermionic emission of a Schottky contact with the series resistance can be expressed as Cheung's function given by

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = \frac{nkT}{q} + IR_{\mathrm{s}}. \tag{5}$$

The plot's experimental dV/d(ln$I$) *versus* I for the different annealing temperature is shown in Fig. 2. The series resistance value R_s is obtained from the slope and the nkT/q value from the y-intercept. The estimated series resistance (R_s) is in the range $R_s = 83$–$715\,\Omega$ for different annealing temperature. As an alternate method to conventional analysis, Norde method is employed [25], to compare the SBH of Pt/Ti Schottky contacts to include the effect of high series resistance which hinders the accurate evaluation of barrier height from the standard ln(I) *versus* V plot. In this method, a function $F(V)$ is plotted against V. $F(V)$ is given by

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right). \tag{6}$$

The effective SBH is given by

$$\phi_{\mathrm{b}} = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q}, \tag{7}$$

where $F(V_{\min})$ is the minimum value of $F(V)$, and $V_{\min}$ is the corresponding voltage. A plot of $F(V)$ *versus* V for the contacts annealed at different temperatures is shown in Fig. 3. The extracted SBHs are 0.66 eV for as-deposited, 0.65 eV for 200 °C, 0.67 eV for 300 °C, 0.70 eV for 400 °C, and 0.59 eV for 500 °C annealed contacts. It is noted that these values are in good agreement with those obtained by I–V method.

C–V measurements are commonly used to determine the effective SBH of an MS diode, since the intercept of a straight line in a $1/C^{-2}$ *versus* V plot with the voltage axis can be used to calculate the effective SBH and the slope of the line gives the semiconductor doping density [26]. Figure 4 shows the plot of $1/C^{-2}$ as a function of reverse bias voltage for the as-deposited and annealed Pt/Ti Schottky contacts. The junction capacitance can be measured at a frequency of 1 MHz. Thus, for an SBD fabricated on an n-type semiconductor, the depletion layer capacitance can be expressed as [27]

$$\frac{1}{C^{2}} = \frac{2(V_{\mathrm{bi}} + V_{\mathrm{r}} - kT/q)}{q\varepsilon_{\mathrm{s}}\varepsilon_{\mathrm{o}}A^{2}N_{\mathrm{i}}}, \tag{8}$$

where A is the surface area of the diode, ε_s the static dielectric constant equal to 12.4 for n-type InP [28], V_r the

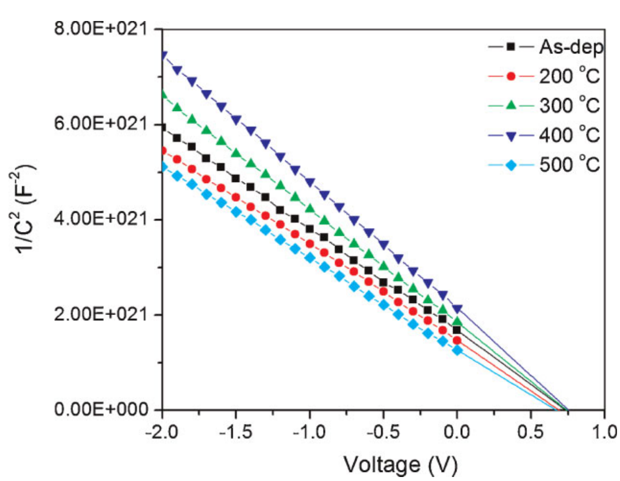

Figure 4 (online color at: www.pss-a.com) Plot of $1/C^2$ *versus* V for Pt/Ti Schottky contacts to n-InP annealed at different temperature.

Table 1 The reverse leakage currents, effective SBHs (ϕ_{bo}^{eff}), ideality factor (n), and series resistance of Pt/Ti Schottky diodes on n-InP as a function of annealing temperature.

sample (°C)	leakage current at −1 volt	Schottky barrier height (SBH) ϕ_{bo}^{eff} (eV)			ideality factor "n"	series resistance R_s (Ω)
		I–V	Norde	*C–V*		
as-dep	4.236×10^{-6}	0.62	0.66	0.76	1.51	224
200 °C	6.439×10^{-6}	0.60	0.65	0.73	1.72	393
300 °C	2.673×10^{-6}	0.63	0.67	0.78	1.40	113
400 °C	1.123×10^{-6}	0.66	0.70	0.80	1.14	83
500 °C	1.031×10^{-5}	0.55	0.59	0.71	1.93	715

applied voltage, N_i the concentration of the non-compensated ionized donors, $\varepsilon_0 = 8.825 \times 10^{-14}$ F/cm. The x-intercept of the plot between $(1/C^2)$ *versus* V is V_o which is related to built in potential $V_{bi} = V_0 + kT/q$, where T is the absolute temperature, N_i is the related to the slope of C^{-2} *versus* V. The curve can be obtained from the expression

$$N_i = \frac{2}{q\varepsilon_s\varepsilon_o A^2}\left[\frac{1}{d(C^{-2})/dV}\right]. \tag{9}$$

The BH deduced from capacitance is from

$$\phi_b = V_0 + V_n + \frac{kT}{q}, \tag{10}$$

where V_n referred to as the Fermi level potential, is the energy difference between the Fermi level and the bottom of the conduction band and is given by $V_n = kT/q\ln(N_c/N_i)$. The density of states in the conduction band edge is given by $N_c = 2(2\pi m^* kT/h^2)^{3/2}$, where $m^* = 0.078 m_0$ and its value is 5.7×10^{17} cm^{-3} for n-InP [22]. As from the C^{-2} *versus* V plot, a straight line is obtained for the as-deposited and annealed Pt/Ti Schottky contacts. The intercept of the plot with the x-axis gives the value of V_0. The linearity of the plot indicates a uniform doping concentration and constant density is interface state. The calculated carrier concentration of Pt/Ti Schottky contacts are 4.074×10^{15} cm^{-3} for the as-deposited and 4.378×10^{15}, 3.664×10^{15}, 3.279×10^{15}, and 4.480×10^{15} cm^{-3} for the contacts annealed at 200, 300, 400, and 500 °C, respectively, as determined from the slope of the curves. These values are slightly lower than the values given by the manufacturer. Due to defects in semiconductor and the presence of deep lying impurities on the depletion region the capacitance can vary for rectifying contacts. The variation in the carrier concentration with annealing temperature can be attributed to the effect of traps. The obtained barrier heights of Pt/Ti Schottky contact for as-deposited and annealed samples at 200, 300, 400, and 500 °C are 0.76, 0.73, 0.78, 0.80, and 0.71 eV, respectively. It is observed that the barrier heights calculated from the experimental *C–V* measurements are lower for the higher doping concentration as compared to lower concentration. Such dependence on the doping level can be expected due to the electric field dependence of the dipole layer between the semiconductor and the metal. Table 1 shows the values of SBHs (*I–V*, Norde, and *C–V*), reverse leakage current, ideality factors, and series resistance for as-deposited and annealed Pt/Ti Schottky contacts.

In order to compare the barrier heights that are obtained from *I–V*, Norde, and *C–V* methods, a plot drawn between the barrier heights and annealing temperature is shown in Fig. 5. It can be seen clearly from Fig. 5 that the barrier height of the Pt/Ti Schottky diode improved upon annealing at 400 °C. However, there is a slightly decrease of SBH of Pt/Ti Schottky contact after annealing at 500 °C. The most satisfying result obtained here is the contact annealing at 400 °C with ideality factor of 1.14 and BH of 0.66 eV (*I–V*) and 0.80 eV (*C–V*). According to the *I–V*, Norde, and *C–V* measurements, the variation in the BHs of Pt/Ti Schottky contact after annealing, suggest that Pt/Ti films may react with InP. This is confirmed by AES and XRD examinations. It can also be seen from Fig. 5 the C^{-2}–V curves gave barrier height values higher than those derived from *I–V* measurements. The reasons for the discrepancy between the *I–V* and

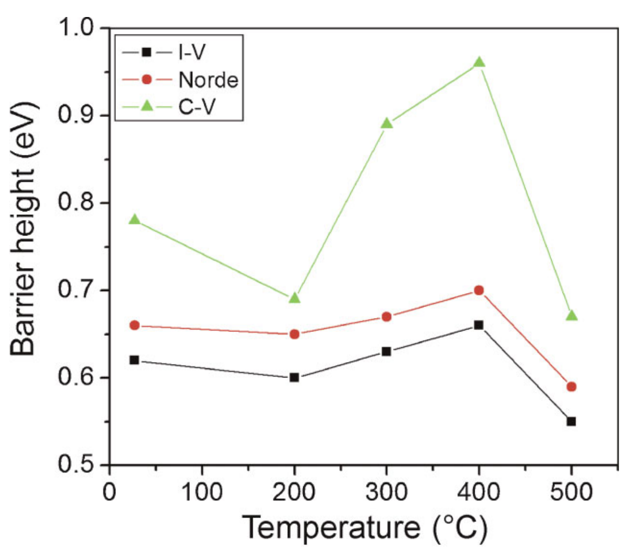

Figure 5 (online color at: www.pss-a.com) Plot of barrier heights against annealing temperatures for the Pt/Ti Schottky contacts on n-type InP.

C–V measured SBHs are explained as follows. Since the *I–V* method involves the flow of electrons from semiconductor to metal, the barrier height determined from this method will logically yield the lower barrier height or a combination of low and high barrier heights. This is known as parallel [29] or mixed phase [30] contact. Another reason might be partly due to image-force barrier lowering effect [31]. The current distribution on the contact dots may not be uniform which can cause error in area in the *I–V* method. Some reports showing that the discrepancy between BHs measured by different techniques might be associated with the instrumentation problems, namely, the way to determine true space-charge capacitance from *C–V* data or a large series resistance, which could affect the value determined from *I–V* data [32]. Song et al. [33] reported that the inhomogeneities in the interfacial oxide layer composition, non-uniformity of the interfacial layer thickness and distribution of interfacial charges can also cause such difference in the barrier height determined from *I–V* and *C–V* techniques.

3.2 Structural and morphological properties of Pt/Ti Schottky contacts The Pt/Ti contact structure is examined by AES depth profile in order to investigate the intermixing of the metals and InP layers before and after annealing at 500 °C. Figure 6(a–c) shows the Auger sputter depth profile results obtained for the as-deposited, 400 and 500 °C annealed samples. The results show some changes in the metallization structure after annealing. As can be seen from Fig. 6(a), the as-deposited layers exhibit a relatively sharp interface, indicating the absence of inter-diffusion into InP. For the sample annealed at 400 °C Fig. 6(b), a small amount of indium is out-diffused into the metal layers. This is indicating the possibility that In reacts with Pt and Ti form Pt– and Ti–In intermatalic compounds during annealing temperature. For the sample annealed at 500 °C, Fig. 6(c) it is observed that some amount of indium (In) is out-diffused into the metal layers. However, it is noted that a small amount of phosphide is also out-diffused into the metal layers which indicates the formation of phosphide phases at the metal/semiconductor interface.

In order to confirm further the interfacial reactions between the metal and InP layers during RTA, XRD measurements are performed. Figure 7 shows the XRD plots of Pt/Ti Schottky contacts. Figure 7(a) shows the XRD plot of the as-deposited sample. In addition to the characteristic peaks of InP (111), (222), there are other peaks observed which are identified as $Pt_{52}In_{48}$ ($\bar{6}01$) and In_9Pt_{13}(555). For the contact annealed at 400 °C, Fig. 7(b), additional peaks are observed compared with that of the as-deposited one. These phases are identified as In_2Pt (111), Ti_3In_4 (220), $Pt_{52}In_{48}$ ($\bar{2}01$), Pt_3In_2 (116), and In_3Pt_4 (642). This is indicative of the formation of new interfacial phases, as expected from AES depth profile [Fig. 6(b)]. After annealing at 500 °C, Fig. 7(c), extra peaks are observed in addition to the peaks observed in the as-deposited and 400 °C annealed sample, which indicate the formation of new interfacial phases. These phases are identified as $Ti_{17}P_{10}$ (311) and PtP_2 (331).

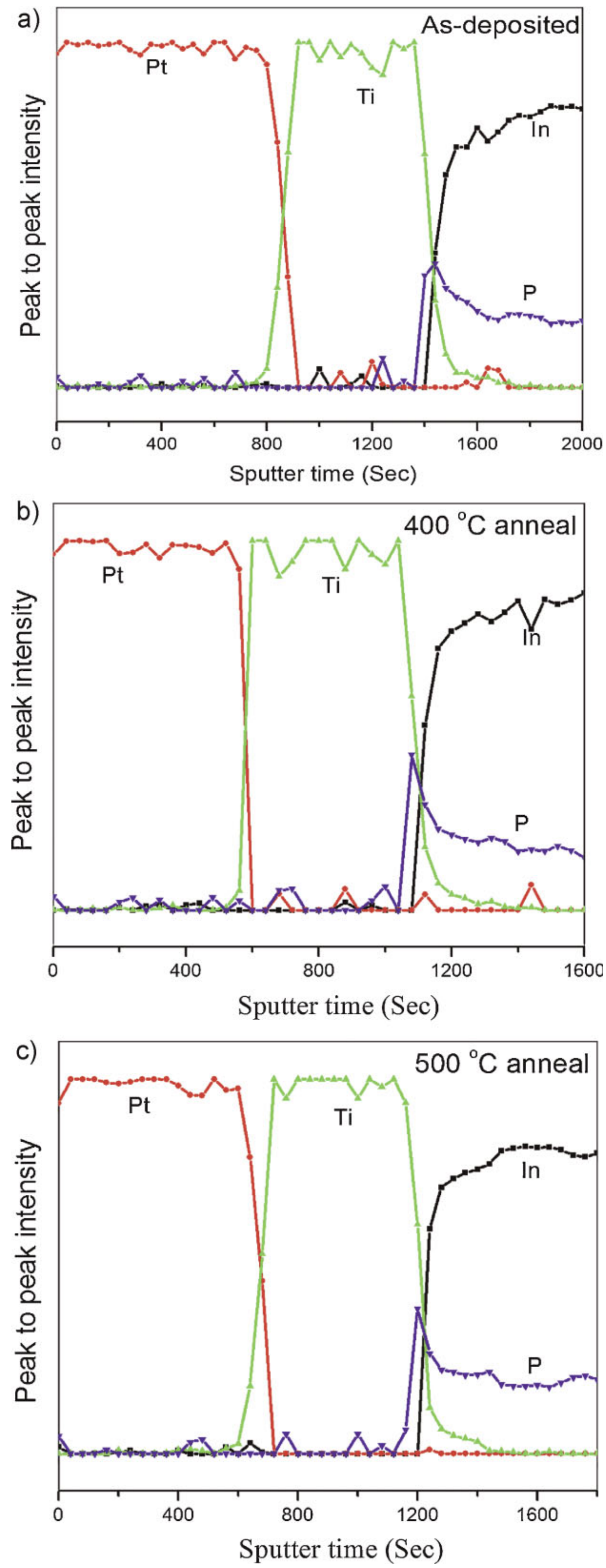

Figure 6 (online color at: www.pss-a.com) Auger depth profiles of the Pt/Ti Schottky contacts to n-InP: (a) as-deposited, (b) annealed at 400 °C, and (c) annealed at 500 °C.

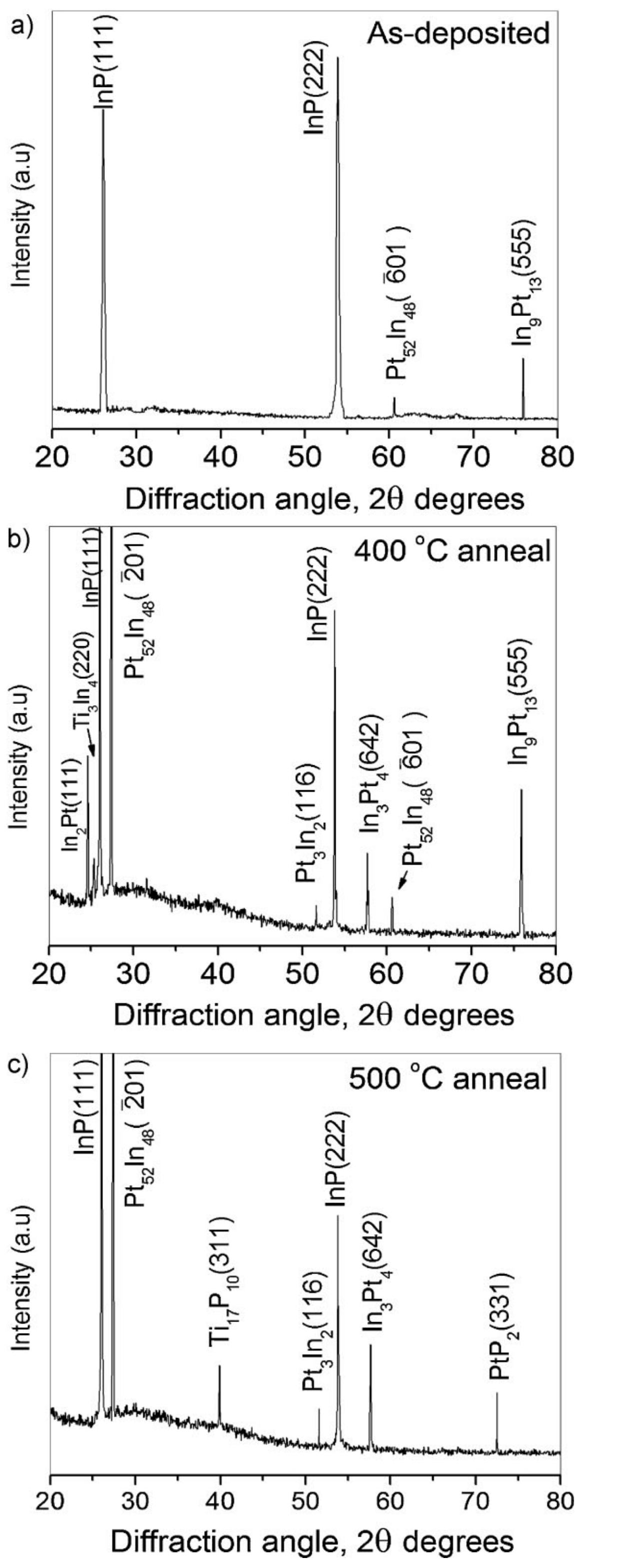

Figure 7 The XRD plot of the Pt/Ti Schottky contacts on n-type InP: (a) as-deposited, (b) annealed at 400 °C, and (c) annealed at 500 °C.

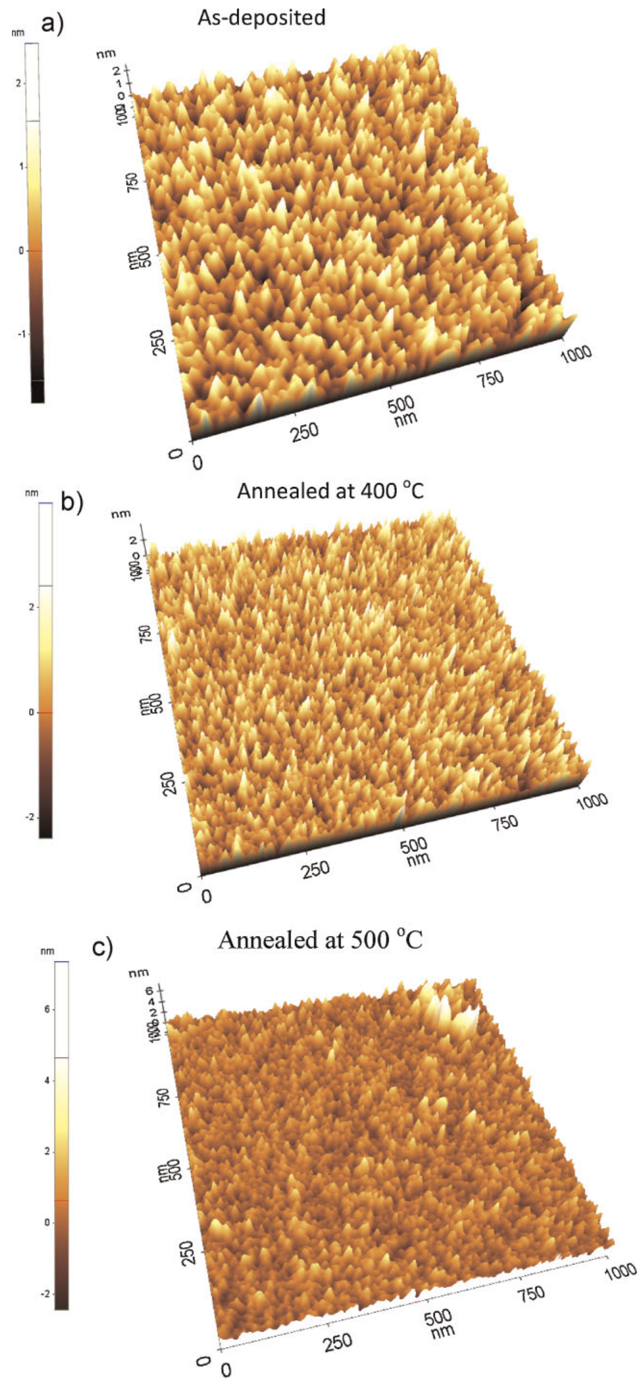

Figure 8 (online color at: www.pss-a.com) AFM micrographs of the Pt/Ti Schottky contacts to n-InP: (a) as-deposited, (b) 400 °C annealed, and (c) 500 °C annealed.

The AFM is employed to characterize the surface morphology of the Pt/Ti Schottky contacts before and after annealing at 500 °C. AFM images of the Pt/Ti Schottky contact for the as-deposited and annealed at 400, 500 °C are shown in Fig. 8. The scanned area of the sample is $1 \times 1\ \mu m^2$. The surface morphology of the as-deposited Pt/Ti Schottky contact is fairly smooth with a root-mean-square (RMS) roughness of 0.477 nm as shown in Fig. 8(a). When the contact is annealed at 400 °C, Fig. 8(b), the surface morphology of the Pt/Ti Schottky contact is slightly improved with an RMS roughness of 0.638 nm. With further increase in annealing temperature up to 500 °C, Fig. 8(c), it is observed that the surface morphology of the contact is slightly increased with an RMS roughness of 0.693 nm as compared to the as-deposited and 400 °C annealed contacts. These results indicate that the Pt/Ti Schottky contact does not suffer from the thermal degradation during annealing temperature.

It is well known fact that the interface states and chemical reaction between the M–S surfaces may play an important role in determining the electrical properties of the devices. The improved SBH of the Pt/Ti contact upon annealing could be ascribed to the interfacial reaction occurring between metal and InP layers. According to the results of AES and XRD, the out-diffusion of the indium (In) from the InP into Pt/Ti layers and participates in the formation of indium phases at the interface. The formation of In_2Pt (111), Ti_3In_4 (220), $Pt_{52}In_{48}$ ($\bar{2}01$), Pt_3In_2 (116), In_3Pt_4 (642), $Pt_{52}In_{48}$ ($\bar{6}01$), and In_9Pt_{13} (555) [as shown by XRD in Fig. 7(b)], which leads to the accumulation of indium vacancies at the InP surface region. As a result, the increase in negative charges at the interface that probably arise due to electron traps localized at the InP surface. This induces an increase in the value of the SBHs of the Pt/Ti Schottky contact extracted from the *I–V* characteristics for the contact annealed at 400 °C. Another possibility is that the increase in barrier height might be due to the reduction of non-stoichiometric defects in the metallurgical interface [34]. The region involving the defects can be reduced due to the inter-diffusion of metal into InP. The presence of these phases at the interface causes the variance in leakage current. The increase in the SBH is always accompanied by a corresponding reduction in the reverse leakage current. This finding is consistent with the results previously reported by Bhaskar Reddy et al. [35] and Janardhanam et al. [36]. They reported that the formation of indium phases at the interface could be the reason for increase of SBHs upon annealing temperature. At the 500 °C annealing temperature, the preferential out-diffusion of phosphorous leads to a loss of P from the surface and loss P from the surface may lead to change in the interface state density distribution. In this case a positive charge state may exists at the interface due to loss of phosphorous from the surface. This may reduce the barrier height in the 500 °C annealed sample than compared to the 400 °C annealed sample. According to Duboz et al. [37] the lower value of the barrier height for sample annealed at higher temperature can be attributed to reduction in the density of interfacial defects. Also, the researchers have found that the Fermi level at metal/GaN interfaces is pinned by defects. The modification of the defects density by annealing could change the pinning at the Fermi level what could resulted in change of the barrier height. Van de Walle et al. [38] have also explained the barrier height change for annealed metal/n-GaAs SBDs by the relation between the equilibrium interface charge and barrier height values.

4 Conclusions Electrical, structural, and morphological properties of Pt/Ti Schottky contacts on n-type InP have been investigated by means of *I–V*, *C–V*, AES, XRD, and AFM measurements. The extracted value of barrier height of as-deposited Pt/Ti SBD is 0.62 eV (*I–V*) and 0.76 eV (*C–V*). It is noted that the barrier height of the Pt/Ti SBD increases with increase in annealing temperature up to 400 °C. Experimental results show that a good rectification is achieved after annealing at 400 °C. A maximum barrier height 0.66 eV (*I–V*) and 0.80 eV (*C–V*) is obtained on the Pt/Ti Schottky contact at 400 °C for 1 min in nitrogen atmosphere. However, further increase in annealing temperature up to 500 °C, the barrier height decreased to 0.55 eV (*I–V*) and 0.71 eV (*C–V*). Norde method is also employed to obtained the barrier heights of 0.66 eV for as-deposited, 0.65, 0.67, 0.70, and 0.59 eV for 200, 300, 400, and 500 °C annealed contacts, which are in agreement with those obtained from the *I–V* method. From the above observations, the optimum annealing for the Pt/Ti Schottky contact is 400 °C. Based on AES and XRD results, it is clear that the formation of indium phases at the Pt/Ti/n-InP interface may be the reason for the increase in the barrier height for the 400 °C annealed contact. It is observed that the phosphide phases are formed at the Pt/Ti/n-InP interface after annealing at 500 °C as evidenced from the XRD analysis. This may be the reason for decrease in barrier height of the Pt/Ti Schottky contact. The AFM results showed that there is no significant degradation in the surface morphology (RMS roughness of 0.693 nm) of the contact even after annealing at 500 °C as compared to the as-deposited one.

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References

[1] Y. Imai, T. Ishibashi, and M. Ida, IEEE Electron Device Lett. EDL **2**, 67 (1981).
[2] L. Messick, Solid-State Electron. **23**, 551 (1980).
[3] D. L. Lile and D. A. Collins, Appl. Phys. Lett. **37**, 552 (1980).
[4] S. Y. Wang, S. H. Lin, and Y. M. Huang, Appl. Phys. Lett. **51**, 83 (1987).
[5] N. Newman, T. Kendelewicz, L. Bowman, and W. E. Spicer, Appl. Phys. Lett. **46**, 1176 (1985).
[6] T. Kendelewicz, N. Newman, R. S. List, I. Lindau, and W. E. Spicer, J. Vac. Sci. Technol. B **3**, 1206 (1985).
[7] R. Thouhami, S. Ravelet, M. C. E. Yagoub, and H. Baudrand, J. Appl. Phys. **94**, 6574 (2003).
[8] H. Hasegawa, T. Sato, and T. Hashizume, J. Vac. Sci. Technol. B **15**(4), 1227 (1997).
[9] T. Sato, C. Kaneshiro, and H. Hasegawa, Jpn. J. Appl. Phys. **38**(2b), 1103 (1993).

[10] M.-J. Jeng, H.-T. Wang, L.-B. Chang, Y.-C. Cheng, C.-M. Lee, and Ray Ming Lin, Jpn. J. Appl. Phys. **38**, L1382 (1999).
[11] H.-I. Chen, Y.-I. Chou, and C.-Y. Chu, Sens. Actuators B **85**, 10 (2002).
[12] Zs. J. Horvath, E. Ayyildiz, V. Rakovics, H. Cetin, and B. Podor, Phys. Status Solidi C **2**, 1423 (2005).
[13] W.-C. Huang and D.-R. Cai, International Workshop on Junction Technology, Shanghai, 2006, p. 295.
[14] H. Cetin and E. Ayyildiz, Physica B **394**, 93 (2007).
[15] M. Bhaskar Reddy, V. Janardhanam, A. Ashok Kumar, V. Rajagopal Reddy, P. Narasimha Reddy, C.-J. Choi, R. Jung, and S. Hur, J. Mater. Sci. Mater. Electron. **21**, 804 (2010).
[16] M. Soylu, B. Abay, and Y. Onganer, J. Phys. Chem. Solids **71**, 1398 (2010).
[17] A. Ashok Kumar, V. Janardhanam, and V. Rajagopal Reddy, J. Mater. Sci. Mater. Electron., DOI 10.1007/s10854-010-0225-5.
[18] H. Cetin and E. Ayyildiz, Physica B **405**, 559 (2010).
[19] W.-C. Huang and C.-T. Horng, Appl. Surf. Sci. **257**, 3565 (2011).
[20] S. Sankar Naik, V. Rajagopal Reddy, C.-J. Choi, and J.-S. Bae, J. Mater. Sci. **46**, 558 (2011).
[21] E. H. Rhoderick, Metal–Semiconductor Contacts (Clarendon, Oxford, 1978).
[22] C. W. Wilmsen, Physics and Chemistry of III–V Compound Semiconductor Interfaces (Plenum Press, New York, 1985).
[23] D. T. Quan and H. Hbib, Solid-State Electron. **36**, 339 (1993).
[24] S. K. Cheung and N. W. Cheung, Appl. Phys. Lett. **49**, 85 (1986).
[25] H. Norde, J. Appl. Phys. **50**, 5052 (1979).
[26] S. M. Sze, Semiconductor Devices, Physics and Technology (Wiley, New York, 1985).
[27] A. Van der Ziel, Solid State Physics Electronics, second ed. (Prentice-Hall, Englewood Cliffs, NJ, 1968).
[28] A. N. Donald, Semiconductor Physics and Devices (Irwin, Boston, 1992).
[29] I. Ohdomari and K. N. Tu, J. Appl. Phys. **51**, 3735 (1980).
[30] J. L. Freeouf, T. N. Jackson, S. E. Laux, and J. M. Woodal, Appl. Phys. Lett. **40**, 634 (1982).
[31] S. M. Sze, Physics of Semiconductor Devices, second ed. (Wiley, New York, 1981).
[32] R. T. Tung, Mater. Sci. Eng., R **35**, 1 (2001).
[33] Y. P. Song, R. L. Van Meirhaeghe, W. H. Laflere, and F. Cardon, Solid-State Electron. **29**, 633 (1986).
[34] W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, Phys. Rev. Lett. **44**, 420 (1980).
[35] M. Bhaskar Reddy, V. Janardhanam, A. Ashok Kumar, V. Rajagopal Reddy, and P. Narasimha Reddy, Phys. Status Solidi A **206**, 250 (2009).
[36] V. Janardhanam, A. Ashok Kumar, M. Bhaskar Reddy, V. Rajagopal Reddy, P. Narasimha Reddy, A. K. Balamurugan, and A. K. Tyagi, Phys. Status Solidi A **206**, 2658 (2009).
[37] J. Y. Duboz, F. Binet, N. Laurent, E. Rosencher, F. Scholz, V. Harle, O. Briot, B. Gil, and R. L. Aulombard, Mater. Res. Soc. Symp. Proc. **449**, 1085 (1996).
[38] V. Van de Walle, R. L. Van Meirhaeghe, W. H. Laflere, and F. Cardon, J. Appl. Phys. **74**(3), 1885 (1993).