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Perspective on the future of silicon photonics and electronics

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ABSTRACT

Silicon photonics is advancing rapidly in performance and capability with multiple fabrication facilities and foundries having advanced passive and active devices, including modulators, photodetectors, and lasers. Integration of photonics with electronics has been key to increasing the speed and aggregate bandwidth of silicon photonics based assemblies, with multiple approaches to achieving transceivers with capacities of 1.6 Tbps and higher. Progress in electronics has been rapid as well, with state-of-the-art chips including switches having many tens of billions of transistors. However, the electronic system performance is often limited by the input/output (I/O) and the power required to drive connections at a speed of tens of Gbps. Fortunately, the convergence of progress in silicon photonics and electronics means that co-packaged silicon photonics and electronics enable the continued progress of both fields and propel further innovation in both.

I. INTRODUCTION

Silicon photonics research and commercialization has intensified as both photonic component performance and photonic integration complexity have been dramatically improved and expanded in the past decade. It enables a wide range of applications from datacom and telecom to sensors including light detection and ranging (LIDAR), gyroscopes, biosensors, and spectrometers. The key drivers for using silicon for photonics include the advantages of low-loss silicon waveguides with compact size and excellent uniformity, resulting from the high quality and mature processing of the silicon CMOS ecosystem. Modern CMOS packaging techniques, including those originally developed for the cell phone and IT industries, are being applied to silicon photonic integrated circuits (PICs), resulting in much lower costs and far improved scalability. Figure 1 shows the evolution of datacom transceivers through five generations of technology. Datacom transceivers using silicon photonics have rapidly moved from product introductions to multi-million units per year.[1] As data rates increase from 100 Gbps to Tbps, integrated electronics is essential to reduce both the system-level power consumption and the device-level capacitance of connecting the transmitter modulators as well as the receiver photodetectors. Target power requirements have dropped from thousands of pJ/bit to sub-pJ/bit over the past decade.[2] A key element of the interconnect, the semiconductor laser, will likely move from disaggregated architectures to be integrated on the PIC. This enables scaling from one laser per PIC to potentially thousands of lasers per PIC with wavelength division multiplexing (WDM), thus enabling Pbps-scale data connections. Concurrently, PICs are evolving from pluggable transceivers at the periphery of the board to co-packaged optics and electronics, and to 3D integrated PICs and electrical integrated circuits (EICs).

This paper describes these trends, including the progress in silicon photonic devices and PICs, and the evolution from separate ICs to 3D integrated PIC/EICs. The economic and performance drivers for this transformation are described along with the fundamental limits and challenges that need to be solved. We conclude with a discussion on the future evolution beyond this decade, where many new applications of co-packaged silicon photonics and electronics become possible and ubiquitous.

II. APPLICATIONS

The rise of the digital economy and the associated exponential growth of data has bolstered innovations in computing, storage, and

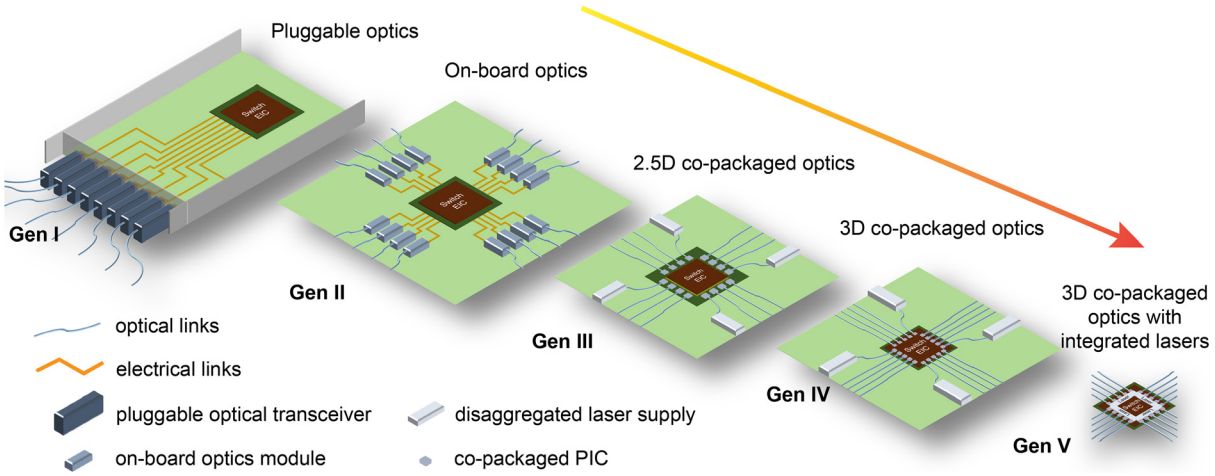

FIG. 1. Generations of optics and the evolution of co-packaging technologies used in data center applications. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip.

networking technologies and systems. Never before has the need been greater to analyze, store, and move data. The advent of mega-scale data centers and cloud computing has in turn driven innovations in "as a service" business models, including infrastructure, software, platform, and function-as-a-service (XaaS). To maximize efficiency and utilization of computation resources, traditional server architectures have been disaggregated. Pools of resources including general computation, specialized computation, i.e., video acceleration, AI/ML (artificial intelligence/machine learning) training and inference, HPC (high performance computing), and data storage are all connected by high performance fabrics with up to petabytes per second of cross-sectional bandwidth. The interconnect is beginning to dominate fabric cost and power consumption, creating a true driver and business case for integrated silicon photonic I/O.

Silicon photonics lends itself to applications that require high-bandwidth, low-cost, and long-distance interconnect capabilities. A natural first volume application for commercial silicon photonics was data center optical interconnects, enabling scale-out computing systems as part of the traditional data center infrastructure and ecosystem of pluggable optical transceivers. The true goal of silicon photonics, however, is to co-package using heterogeneous integration with other networking, storage, and computation application-specific integrated circuits (ASICs) to enable semiconductor optical I/O directly from the silicon chip itself. Figure 2 shows current and future applications of silicon photonic integrated I/O.[3] The first application of a true co-packaged technology is connecting fabric switches in scale-out fabrics. The silicon photonics chiplet is heterogeneously integrated with 25.6 Tb/s and 51.2 Tb/s switch silicon as an optical I/O, creating a true system on a chip (SoC). Similar to the heterogeneous integration of embedded DRAM in package, a photonic co-packaged switch enables the highest performance electrical signal integrity, most efficient use of system silicon, and lowest system power consumption on a single

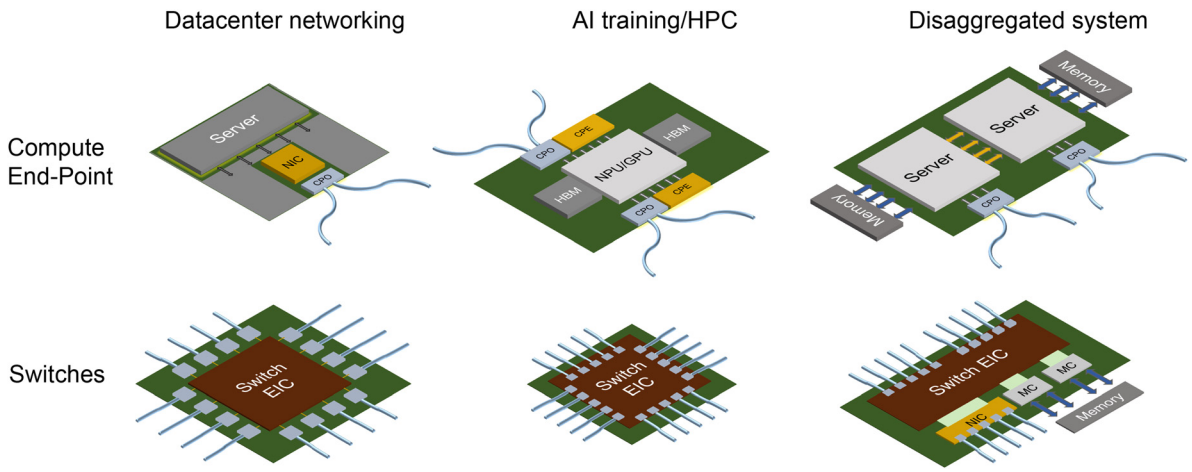

FIG. 2. Applications of co-packaged optics in different systems (with compute end-point and switches). CPO: co-packaged optics; CPE: co-packaged electronics; NIC: network interface card; NPU: network processing unit; GPU: graphics processing unit; HBM: high bandwidth memory; MC: memory control.

substrate. Similarly, integrated silicon photonics can be used in HPC fabrics, where silicon photonics can provide high-density, low-latency interconnects. A third example of future applications of photonic interconnects are in scale-up compute fabrics, such as graphics processing unit (GPU) or AI/ML training and inference clusters, where workloads are balanced across multiple specialized compute chips.[4] Ultimately, as the bandwidth to the server node continues to scale, and the distance copper can transmit reduces, there will be a use case for optical I/O off the network interface card (NIC) or directly from the server itself. Additionally, silicon photonics integration has also emerged in coherent optical systems, where state-of-the-art silicon PICs and tunable lasers are integrated with coherent digital signal processors (DSPs) and deployed in data center interconnects connecting data centers within regional zones.[5,6]

III. STATE-OF-THE-ART

A. Electronic integration and limitations

When Moore's law was initially proposed,[7] it was an economic argument about the cost of integrating a transistor on chip. One way of looking at that is by examining the number of transistors that can be put on a single die, as shown in Fig. 3. While many have claimed the end of Moore's law for well over a decade,[8–10] this metric of transistors per die has continued at its exponential rate, and in the case of specialized chips like GPUs and field-programable gate arrays (FPGAs) have even sped up in rate. In the early decades of transistor scaling, this exponential reduction in cost and size also came with an increase in individual transistor performance, as the smaller transistors achieved through device scaling also had the benefit of reducing device parasitic capacitance. A good indicator of individual transistor device performance is the transit frequency (f_t) of the transistor, the frequency where the current gain goes to unity. As seen in Fig. 4, this unity current gain frequency scaled exponentially with smaller device nodes up through about the 45 nm CMOS node in the mid to late 2000s, where it stalled out. While this is partly due to limitations in the materials themselves at the transistor level, it was also due to a shift in priorities at the die level based on maximum thermal dissipation that could be removed at a reasonable cost, and the rise of mobile computing as a dominant market driver for new nodes. Essentially, low power

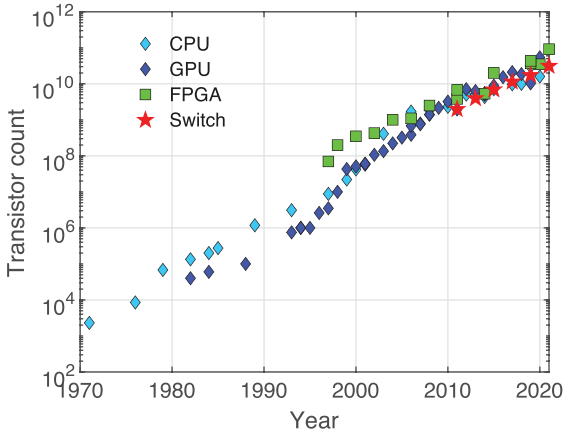

FIG. 3. Transistor count of CPU, GPU, FPGA, and switch die and their release dates.

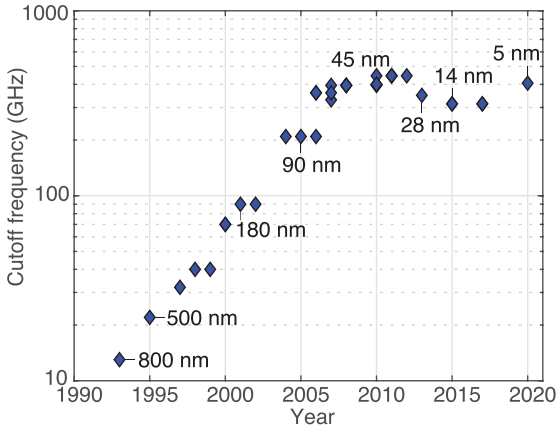

FIG. 4. Transistor node f_t and year when commercial chip released.

performance became the top priority over individual transistor performance in many applications. While this has been a great trend in leading to a revolution in mobile and Internet of Things (IoT) applications, it poses significant challenges for the high performance computing and high speed-wireline applications. Given that individual chips are still increasing in complexity at exponential rates, continued performance improvements of the I/O at exponential rates are also required. At the same time, the die size has not increased meaningfully during this period, leading to a bottleneck caused by how much data can get in and out through the perimeter of the chip itself.

High performance electronic serializer/deserializer (SerDes) blocks have filled in this gap to date. These high speed wireline links are now capable of 112 Gb/s pulse amplitude modulation 4-level (PAM-4) consuming less than 7 pJ/bit per transmitter receiver pair[11,12] but are doing so by increasing the proportion of the chip dedicated to I/O both in area and power. Since 2010, while the ASIC core power has gone up by 8×, SerDes power has gone up by 25×, a trend that is not sustainable into the future.[13]

A reality of electronic wireline is that while it may be more efficient to initially create the signal compared with optical communication, the need for retimers to counteract metal losses in longer transmission lines means that at some transmission distance, optical communication through a low loss fiber becomes more efficient. For long-haul communications measured in kilometers, this has been true for decades. However, as the data rate, and frequency of transmission increase, the power consumption required to scale the copper-based communications rises faster than that of optical solutions. This trend reduces the distance of iso-performance above which optical links overtake copper links in performance/watt. Looking into the future, step functions in integrated photonic performance that would accompany higher levels of integration, including laser and amplifier integration on-chip, could reduce this distance to on-board and even within-package distances.

B. Photonic integration

Silicon photonics uses integrated photonic devices on a common low-cost Si substrate. Compared to InP substrates, the cost is much

reduced (>10× lower) and can scale up to 300-mm diameter wafer process using standard CMOS facilities.[14] For a Si PIC, Si also provides low loss waveguides interconnecting various photonic elements completing certain functions, including lasers, modulators, photodetectors, and other passive devices [arrayed-waveguide gratings (AWGs), Mach–Zehnder interferometers (MZIs), phase tuners, etc.]. The number of devices on a single Si PIC keeps increasing thanks to the high device yield and the application driven requirements for large scale PICs in areas including high-speed transceivers, LIDAR, optical computing, and quantum photonics (Fig. 5). With ever-increasing number of channels, low optical loss and/or amplification are necessary to facilitate the optical signal quality in a large-scale PIC. Silicon photonics provides a low loss platform with an order of magnitude lower loss than InP platforms and forms the backbone for recent progress in optical transceivers, LIDARs, etc. With on-chip lasers and amplifiers, the PIC capacity can be increased dramatically without being limited by the high device and coupling loss. Figure 5 summarizes the evolution of the number of photonic devices integrated on a single waveguide for platforms including monolithic InP, monolithic Si, and heterogeneous InP/Si or GaAs/Si. The expectation is that the integration level of heterogeneous integrated InP/Si platform, with on-chip laser and amplifier gain, will increase dramatically in the coming years.

C. Photonic interconnect co-packaging roadmap

Over the last 20 years, the interconnect of core communications ASICs (application-specific integrated circuits) with optical transmission links have become increasingly disaggregated. The vast majority of optical ports are deployed as independent optical sub-systems physically plugged into a front panel of a host system. These front panel pluggable optical links have provided great benefit to the optical industry and have successfully been deployed in mass volume. Figure 6 shows the progress over the past three years and projections for the next three years.

However, as the density and speed of optical links have increased manyfold, the paradigm of front panel pluggables has shown to have some drawbacks. Specifically, the power and cost have not scaled as effectively as core digital logic within the ASICs. An increasing portion of both the power and cost of the system are dedicated to the interconnect channel between the ASICs and the optics. The electrical interconnect of the ASIC off its own package, through a printed circuit board (PCB), and through a connector on the pluggable module has resulted in a power hungry and costly electrical link. At higher data rates, these links often require advanced PAM-4 signaling as well as full re-timing inside the optical modules. In current state-of-the-art systems, about 50% of the power in an optical module goes to this re-timing function. This can represent more than 25% of the power consumption of the overall system. Eliminating this unneeded power and associated cost of the high loss electrical links between the ASICs, and the optical sub-system provides a pathway to much more power-efficient and cost-efficient system for future scaling of optically enabled systems.

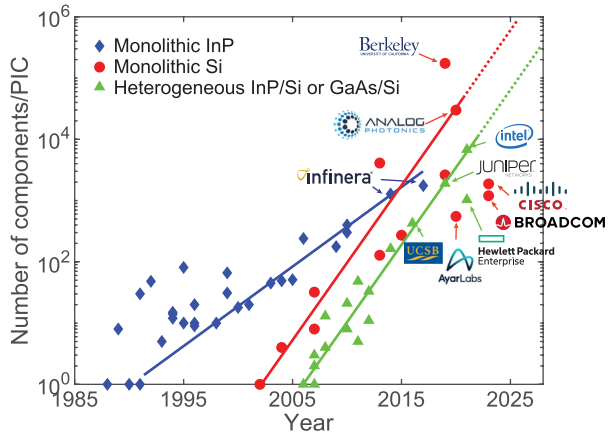

FIG. 5. The number of photonic components integrated on a single waveguide over time for three photonic integration platforms: InP substrate with integrated lasers, Si substrate without integrated lasers, and Si substrate with integrated lasers.

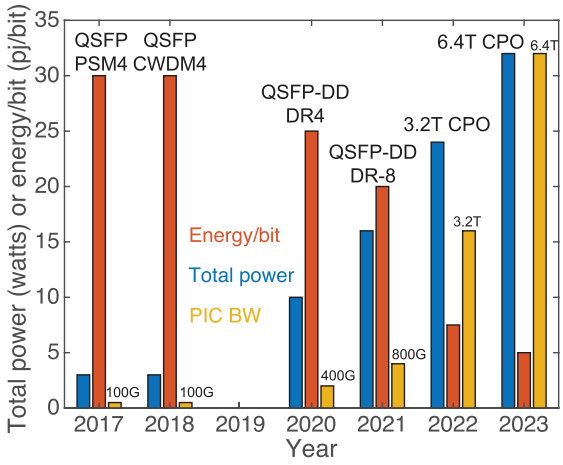

FIG. 6. The evolution of PIC bandwidth, power efficiency, and total power consumption.

Although the elimination of the high loss electrical channels provides significant benefits to the overall system, there are many challenges in accomplishing a new paradigm of packaging optics directly with ASICs. Packaging multiple ASICs from heterogeneous process nodes in a single package and on a single substrate has been successfully deployed by the semiconductor industry in volume, utilizing low power and cost-efficient chip to chip interconnects. Optical links present a number of unique challenges to accomplishing this same feat. First, the physical area and volume of optical components have traditionally been much larger than could fit within a semiconductor package. Pluggable modules occupy an order of magnitude more volume in the system compared to the size of the ASICs with which they communicate. As subsequent discussion will show, the advent of high-density silicon photonics for optical communications solves this first problem. Second, the overall system reliability of co-packaged optics must meet the same standards as expected of the core semiconductor ASIC. Optical components and front panel pluggable systems generally have a much higher failure rate than semiconductors in the field.

The pluggability of the optical modules allows for field serviceability of these modules when they fail without the need to replace the entire system. Integrated silicon photonics is a way to address the discrete, more failure prone nature of traditional optical modules. Fully

integrated solutions, with silicon being the primary medium of the technology, provide a pathway for optical level reliability consistent with the failure rates of the core ASICs to which they are attached. Finally, optical components have a unique challenge in that optical fibers need to be attached to the chips. No other semiconductor component has this unique challenge of a mechanical fiber attachment to the chip, while maintaining sub-micron precision opto-mechanical alignment. High-volume die attachment machines used in the semiconductor industry have not been optimized for the forces and interference of a large number of fibers attached to a chip. To deal with this issue, silicon photonics provides a way to enable direct optical connectors to the silicon waveguides, although significant development work must be done to realize this potential. This allows for standard semiconductor packaging machines to co-package these chips with ASICs. Only known good dies are used both for the optics and the ASICs alleviating any issues with multi-part yields. Once a complete package is assembled with ASICs and silicon photonics, optical fibers can be attached as part of the overall box system assembly.

D. Co-packaging challenges

The need for integrating photonics and electronics has been clear for the past decade, but several issues have limited its implementation: (1) integration incompatibility, (2) design incompatibility, (3) yield, (4) reliability, and (5) fiber attach. We describe progress on each of these issues over the past decade. State-of-the-art CMOS ICs are made on 300 mm wafers, while InP photonics has been using 2″, 3″, or 4″ InP wafers (50.8, 76.2, or 101.6 mm, respectively) and GaAs photonics recently made the transition from 3″ or 4″ GaAs wafers to 150 mm. It was the development of silicon photonics with high quality components that has enabled 2.5 and 3D integration of ICs and PICs with modern packaging that only exists at the 300 mm wafer level. A large number of foundries now fabricate PICs in 300 mm CMOS facilities. In a few cases, EICs and PICs have been integrated on the same wafer.[15] The issue of whether the EICs (typically at a 7 nm node) and PICs (typically at a 45 nm or higher node) should be on the same wafer or integrated via 2.5D or 3D is primarily an issue of cost. PICs are often large and do not require the expensive wafer area of high speed electronics (5–22 nm required for modern photonic rates of 26 Gbaud and above). Further, as the die size of large switching chips approaches the size of a reticle, there simply is not room (at any cost) for photonics on the same chip; this drives 2.5 and 3D integration of known good die.

The issue of design integration has been largely solved and is discussed below. In terms of yield, photonics has historically not had sufficient yield be able to integrate hundreds of devices together; however, with the development and fabrication of silicon photonics with modern, highly reproducible CMOS tools, yields have dramatically improved over the past decade, and PICs with over 10000 elements have been demonstrated (Fig. 5).

The reliability, field serviceability, and replaceability of photonic components have been an industry concern and requirement for the past 30 years. The advent of silicon photonics CMOS-based wafer-scale manufacturing has enabled a great reduction in the defect rate of photonic devices: reliability has been increased to just 30 dppm for 100G transceivers.[16] The field data have now reached the point where photonic integration has reduced the failure rate dramatically below that of traditional, nonintegrated solutions. Electronic integration has enabled complex ICs with billions of transistors, something that could never be done with discrete transistors due to cost, yield, size, and reliability issues. Similarly, 1.6 Tbps optical engines are expected to have far lower cost and size, as well as improved yield and reliability, compared to 4 × 400G.[16] Presently, the difficulty of laser integration and the reliability of lasers has meant that most PICs use disaggregated lasers on a separate pluggable, field replaceable module. However, PICs with four integrated lasers have been commercialized and have failure in time (FIT) of just 2, so laser integration will happen, particularly when the number of lasers required increases from one to hundreds. The final impediment to co-packaging has been fiber attach, which as discussed above, has been solved.[1]

IV. SILICON PHOTONICS EVOLUTION PATH

Integrated silicon photonics provides a pathway for almost all the key building blocks for communications and interconnects using optical channels. It allows for the use of high-volume semiconductor equipment developed for the silicon IC industry. As the basic fabric of the silicon photonics chip, low loss (<1 dB/m loss attained) waveguides[17] interconnecting all photonic components allow for a mix and match of various functional devices to create an optical chip. These waveguides include silicon, silicon dioxide and silicon nitride, or combinations of the three depending on the application. Coupling to these waveguides with optical fiber to form optical I/O is another key technology that provides a basic building block of chip-based applications. These input and output couplers include tapers to enlarge the mode and match it better to that of single mode fibers, and can be either edge based or vertical (through gratings or 45° mirror-like structures).

Based on the waveguiding system, photonic devices with different functionalities including modulators and photodetectors can be integrated and interconnected on the silicon photonic platform monolithically. In addition, heterogeneous integration with III-V materials provides the required gain medium for on-chip optical amplifiers and lasers. Here, we briefly review the recent progress of modulators, amplifiers, and lasers.

A. Modulator progress

One critical element of silicon photonics that has been a key to success in commercializing the technology is the optical modulator. Here, a number of different technologies have been developed to provide high speed modulation of light from an electrical source. The most common approach that has been proven in mass production is the Mach–Zehnder modulator (MZM).[18] This modulator is relatively temperature insensitive and provides very high bandwidth of modulation. Extensive work has also been done on using ring resonators to modulate light. These ring modulators can provide lower power consumption and still very high bandwidths. An example is using arrays of ring modulators to achieve 1 Tbps transmitters with under 20 fJ/bit.[19] Another advantage of ring modulators is the much reduced footprint compared with MZMs. Ring modulators are also advantageous together with multi-wavelength laser sources, which can help address scalability issues. They are, however, not as temperature insensitive as MZMs and require more fabrication precision. Temperature control is critical to align the ring modulators to the laser wavelengths.[20,21]

To further extend the bandwidth of optical modulators, heterogeneous integration provides the capability of using III-V materials and lithium niobate. Thin-film lithium niobate on SOI waveguides has

enabled over 100 Gbps modulators that are on par with state-of-the-art modulator performance using lithium niobate on insulator.[22,23] This could lay the foundation for high-capacity optical communication systems in the coming years, and the high efficiency is critical in enabling potential Pbps interconnects capacity at reasonable power consumption. Recent progress in monolithic growth of germanium quantum well modulators is also offering an alternative approach without heterogeneous modulator integration, but significant work has to be done to integrate with SOI waveguides.[24,25]

B. Optical amplifiers

The need for amplification, particularly integrated gain, has been known for 100 years and was key to advanced electronic integrated circuits in use today. Similarly, optical amplification in fiber optic networks was essential for the transition from short, single wavelength links to the long-distance, dense wavelength division multiplexing (DWDM) networks of today with bandwidth distance products that are 1000× times larger than before. For integrated photonics, integrated gain in PICs has been essential for all of the large, complex InP PICs,[26] but has been unavailable in early Si PICs because Si has an indirect bandgap, and consequently is an inefficient light emitter. Efficient light emission requires single crystal direct bandgap material (eliminating sputtering or evaporation); epitaxial growth has been difficult due to the lattice mismatch (discussed below). High quality amplifiers and lasers have been implemented by bonding III-V materials onto Si. Gains of 40 dB with saturation powers of 100 mW have been demonstrated.[27,28] Optical amplifiers are being used to boost the signal level without requiring an off-chip bulky and expensive erbium/praseodymium-doped fiber amplifier (EDFA or PDFA). The expansion of complexity is clear; if a typical optical element has a loss of 1 dB, and the maximum loss allowed by signal to noise reduction is 30 dB, then the maximum number of elements on a waveguide is 30. On the other hand, with the inclusion of integrated optical amplifiers with gains of 30 dB, the allowable complexity becomes orders of magnitude larger. This is essential for many DWDM architectures that use AWG splitters and combiners, linear arrays of modulators. It is also essential for optical phased arrays for LIDAR or free space communication where up to 1000 emitters are desired (corresponding to 30 dB splitting loss). An additional advantage of integrating the optical amplifier with the rest of the PIC on a monolithic substrate is to eliminate the coupling loss between the PIC and amplifier, resulting in lower noise and larger amplification.[29]

C. Laser integration

Silicon PICs today mostly use disaggregated lasers. This "optical power supply" is a separate III-V chip fiber coupled to the silicon PIC and avoids the difficulty of integrating III-V and Si processing. It is widely used today and works well but requires the additional system complexity of connecting and cooling the remote laser sources. Integrated solutions can further leverage the semiconductor approach of chip-level integration. A hybrid integrated solution is to use a gain chip placed next to a Si PIC chip, which can be used to power a circuit,[30] stabilize a laser (through self-injection locking), or generate a comb of frequencies for DWDM.[31]

Clearly, if integrated optical amplifiers are possible, then on-chip lasers are available. Heterogeneous integration uses bonding of III-V layers on Si and has been developed for a variety of single wavelength DFB (distributed feedback) laser arrays, CWDM (coarse wavelength division multiplexing), or DWDM lasers with parallel channels for higher capacity interconnects.[32] This is now a commercially available technology and being implemented in advanced silicon photonics foundries. Another potential deployable technology is laser soliton microcombs as the multiwavelength source providing large channel-count and low-noise comb lines.[33] Monolithic solutions using epitaxial III-V growth may be integrated with Si PICs in the future, as discussed below.

D. Optical coupling techniques progress

In parallel with other on-chip device performance progression, optical coupling strategies for efficient light I/O to the Si photonic chip are also making rapid progress.[34] A high coupling efficiency is important in lowering the overall system power budget and affects the on-chip integration level if an optical amplifier is not available. As stated before, the two main techniques are based on in-plane coupling using edge couplers and out-of-plane diffraction coupling using grating couplers. In-plane edge couplers are broadband, highly efficient, and polarization independent. They limit the optical I/O packaging to be on die level, however, and they are sensitive to the chip facet quality. Grating couplers offer wafer-scale optical packaging, and substantial improvements have been done in improving their coupling efficiency. But their limited bandwidth is still not comparable with that of edge-couplers and they also require rigorous polarization treatment.

E. Silicon photonics and electronics ecosystem

One of the key enabling characteristics of silicon photonics is the technological overlap with the heavily invested semiconductor industry. Tools, processes, and simulation models can be shared readily between what was traditionally photonics design and IC design tools and processes. Even the design and tool methodologies are taken from the silicon EDA (electronic design automation) industry and applied to photonics. The concept of a PDK (process design kit) traditionally used in the semiconductor industry to model and design transistor based circuits can now be applied to a host of photonic components with a similar parametric design environment. The major EDA vendors have embraced this vision to provide specialized co-design tools that allow for seamless interaction of electronic and photonic design. In addition to the toolkit as processes being adopted to reflect the larger semiconductor industry, the business models and segmentation of responsibilities can also be adopted to further drive efficiencies. Foundry-based silicon photonics manufacturing services are being offered in a similar way to foundry-based manufacturing in the CMOS industry. The separation of design from manufacturing and process control allows for a wider set of possible designs and markets to be addressed. Finally, the integration of photonic PICs and CMOS-based ASICs can leverage packaging technologies developed for semiconductor to semiconductor integration. These technologies include copper pillar stacking, UBM (under bump metallization), TSVs (through silicon vias), and under fill passivation. All these elements provide for an advanced eco-system of technologies and processes, which allows seamless integration of photonics and semiconductor ICs.

F. Architecture

Short- and medium-reach communications' channels within data centers have evolved to meet the increasing needs for bandwidth and distance. Originally, data centers used multimode fibers to optically interconnect different elements. Simple OOK (on/off keying) was used at increasing frequencies to add more bandwidth as it was needed. With the advent of hyper scale data centers, the physical reach capability of multimode fiber was surpassed (150 m at 25 Gbit/s) and increasingly single mode fiber was deployed to achieve the required distance (up to 2 km). Increasing baud rates of simple OOK were used initially to increase the bandwidth per fiber. When more bandwidth was needed per fiber, the use of CWDM technologies allows for quadrupling the bandwidth with four wavelengths without the need to increase the baud rate. This was very successful, and one of the key high-volume applications of initial silicon photonics was 100G CWDM4 using four lanes of 25 Gbps. In recent years, the use of more advanced PAM-4 signaling became the standard to further increase the bandwidth per lane. In this approach, each symbol contains two bits of information coded by different levels of the optical signal. With current state-of-the-art systems in data centers, data are transmitted at 112 Gbps using a combination of a 53 GBaud line rate with PAM-4 signaling. This again can be coupled with CWDM technology to further increase the bandwidth per fiber. At the same time that this advance was taking place in intra-data center fiber communications, inter-data center and long-haul communications continued to advance using coherent communications with quadrature amplitude modulation (QAM)-based transmission. Recently, coherent communications using Si PICs have scaled down in power and cost to achieve cost effective communications in medium distance (40–80 km) links between data centers. The continued cost reduction and simplification of coherent systems could result in these Si PICs being used for 2 km links inside data centers as well. The timing of such an intercept depends on the economic cost and power efficiency of simplified coherent systems vs the continued progress of PAM-4 and CWDM type links. The current state-of-the-art still has a 4–5× cost premium for coherent links vs PAM-4 direct-detect links for 2 km applications.

V. INTEGRATED SILICON PHOTONICS EXAMPLES IN THE INTERCONNECT INDUSTRY

Initial mass deployment of silicon photonics for communications has been packaged into front panel pluggable transceivers. This allowed for seamless integration of this new technology with existing communication systems. The silicon photonic chip replaced the key active and passive elements present in discrete transceiver implementations. The key elements are a robust fiber coupling attachment of the fiber to the chip. Both vertical and horizontal based coupling have been used to achieve the beam expansion needed to couple to single mode fiber. With the light coupled onto the PIC waveguides, low loss waveguides route the optical signals to their respective transmitter and receiver components, described earlier.

A. Broadcom

Broadcom is developing both 25.6 Tb/s and 51.2 Tb/s co-packaged switches, utilizing the switch ASIC SerDes to directly drive the PICs, eliminating the need for system-level re-timers, high cost PCBA materials, and utilizing the existing silicon packaging ecosystem for industry standard substrates (Fig. 7). The density of the photonic

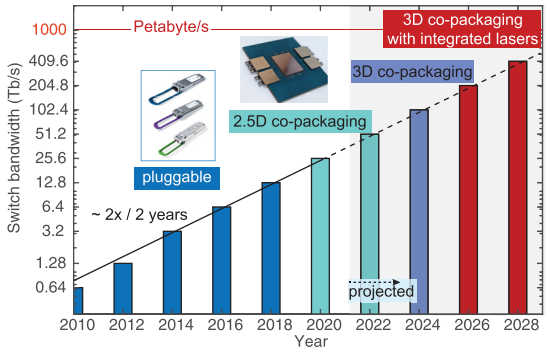

FIG. 7. Switch bandwidth evolution and outlook over the years with four generations. Inset pictures show commercially available pluggable transceivers from Intel and a 2.5D co-packaged PICs and switch from Broadcom. The year indicates when the technology is first deployed.

PIC matches the switch I/O. Broadcom has integrated BiCMOS electronics in a 2.5D stack allowing for exceptional signal integrity between the photodiodes and their respective transimpedance amplifiers as well as the interconnect between the modulator drivers and the modulators. This two chip stack between electronics and photonics does not rely on any intermediate substrate or carrier improving the density of the system. A high-density optical connector is implemented to allow for detachable fiber connection from the chip to the external fibers. Broadcom has PIC versions for 8, 32, and 64 channels of 112 Gbps communications, with integration of optical coupling, waveguides, modulators, and photodiodes. Semiconductor manufacturing processes are used to integrate all of the various semiconductor chips.

B. Intel

In the Intel co-packaging approach, heterogeneous lasers are integrated onto the photonic chiplet (or photonic engine). This is possible because heterogeneously integrated lasers exhibit excellent reliability, on the order of 2 failures per billion device hours (2 FIT).[35] Besides the improved process control made possible through using a high-volume CMOS line, these lasers also have inherent design advantages, including the lack of exposed facets, low coupling losses to silicon waveguides, smaller junction temperature increases, and ∼5× lower current densities compared to other typical III-V based directly modulated lasers. With such low failure rates, arrays of 16 lasers and co-packaged switches based on such arrays can exhibit low aggregate failure rates as well. Nevertheless, it is prudent to introduce redundancy to allow for the possibility of a single laser failure. In the 1.6 Tbps chiplet design that Intel used in the March 2020 12.8 Tbps co-packaged switch demonstration,[36] there are in fact 32 lasers (two for each channel), and subsequent 2 × 1 Mach–Zehnder switches can switch to the second laser should the primary laser degrade in performance or fail.[16]

C. Cisco

Cisco is a major player in silicon photonics for datacom and telecom with the acquisitions of optical companies including Lightwire, Luxtera, and Acacia Communications. Key technology elements

include carrier depletion and SISCAP (semiconductor-insulator-semiconductor capacitor) phase modulator based CMOS opto-electronic Mach–Zehnder interferometers, integrated germanium photodiodes, and a vast array of passive photonic elements. The photonic transmitter and receiver circuitry are integrated in single silicon photonic PICs, which are mated with corresponding transmitter (drivers) and receiver transimpedance amplifier (TIA), ADC (analog-digital converter)/DSP (digital signal processor)] circuits implemented in advanced CMOS nodes. They have multiple internally developed hybrid laser integration schemes and fiber/FAU (fiber array unit) align/attach technologies that have been proven in volume manufacturing scale for IMDD (intensity modulation direct detection) and coherent transceivers in C-Band, S band, and O-Band.

They have built and proven large scale silicon photonic PICs with tight electronics integration and multiple laser/FAU integration schemes across a wide variety of DC and DCI (data center interconnect) applications for both faceplate pluggable and on-board-optics modules. Their technology platform was developed with industry leading foundries and OSATs (outsourced semiconductor assembly and tests). It enables standard wafer level manufacturing flows to provide complete assembly solutions from SiP chipset to optical module and co-package optics integration. Cisco's broad array of silicon photonics technologies lend themselves to the multitude of Switch Co-Packaging approaches being proposed in the industry.

D. Hewlett-Packard enterprise

For HPC applications, co-packaged optics is necessary for data rate scaling and power management and reduced latency. Memory-centric architectures demand large-bandwidth and agile interconnects to support dynamic traffic inside and outside HPCs using silicon photonics-based DWDM solutions to arrive at the optimum trade-off between bandwidth density, energy efficiency, latency, volume manufacturability, and cost.[37] DWDM connectivity favors high-radix switch network enablement.[38] In HPE first generation links, 1 Tb/s aggregated bandwidth was realized from a 32–64 channel link, and 16–40 Gb/s/channel data rates, which achieved low-power operation with direct ASIC drivers without (de)serializers in the CPO configuration. Robust and low-noise quantum dot (QD) comb lasers, energy-efficient and low-loss silicon microring modulators, and highly sensitive avalanche photodetectors are the elements of such a compact DWDM interconnect.[39] The second generation HPE platform is based on heterogeneous III-V-on-Si integration, where InAs/GaAs QD comb lasers and process-compatible metal-oxide-semiconductor capacitor (MOSCAP) microring modulators are included,[40] and robust SiGe avalanche photodiodes (APDs)-based receivers offer much better sensitivity.[41]

VI. FUTURE EVOLUTION OF INTEGRATING SILICON PHOTONICS AND ELECTRONICS

A. Si photonics material and functionality—Heterogeneous integration

Silicon photonics foundry process technology is a key enabler for future device progress and integration. Low loss waveguides are a key enabler for connecting various optical components within the PIC. The ability to have access to both SiO_2-based waveguides as well as Si_3N_4-based waveguides greatly enhances the ability of the PIC to scale to many components. The Si_3N_4-based waveguides allow for temperature-insensitive components such as CWDM muxes and demuxes critical for many applications. Highly reliable Ge photodiodes are widely used across various designs. The continued process control of these key components drives the future yield and reliability critical for scaling. The heterogeneous integration of III-V material such as InP has been demonstrated by both Intel and Juniper. Integrated lasers on a Si PIC are considered as the go-to solutions as the switch capacity keeps increasing beyond 200 Tbps within this decade. Temperature-insensitive lasers with Si_3N_4 cavity together with Si_3N_4 AWGs could potentially enable DWDM systems, in contrast to CWDM systems currently deployed in data centers.[42]

The progress in hybrid (adjacent chips) and heterogeneous integration has been very rapid. Advances in these areas use the advantages of silicon and silicon nitride in terms of better processing (higher temperatures and better lithography) to achieve orders of magnitude loss reduction (down to 0.1 dB/m). One metric that has seen tremendous progress is the semiconductor laser linewidth as shown in Fig. 8. It is clear that with the adoption of low loss waveguides (Si_3N_4 and Si), the linewidth of hybrid integrated lasers and heterogeneous integrated lasers are much narrower than monolithic III-V lasers. The narrow linewidth can potentially enable DSP-free coherent links for telecom and datacom applications. Heterogeneous laser linewidth is being improved dramatically and only lags the hybrid integration by 3 years. This high-performance narrow linewidth laser is expected to be a key enabler in next-generation Si photonics applications.

B. Monolithic laser integration

Monolithic integration of optical gain and lasers with silicon photonics using epitaxial growth has been a goal for the past 30 years. This has been a difficult goal due to three problems: (1) growing a polar compound on a nonpolar Si substrate results in antiphase domains, (2) the large lattice mismatch between most III-Vs and Si results in a high threading dislocation density (TDD), which degrades performance and defect migration reduces lifetime and reliability, and (3) the difference in thermal expansion coefficients results in strain, cracking, and defect migration during cooldown. Consequently, the performance of heteroepitaxially grown lasers has lagged far behind native substrate lasers, and the room temperature lifetime has been

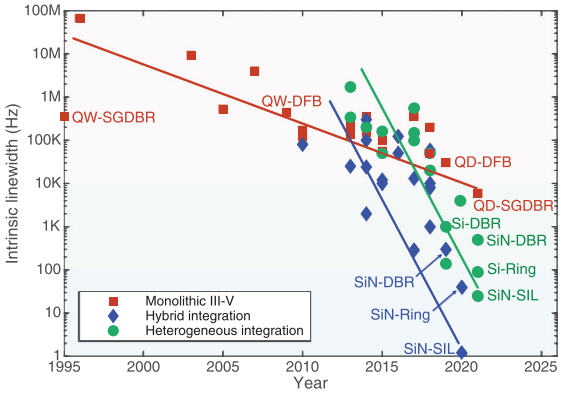

FIG. 8. Semiconductor laser linewidth progression for three different integration approaches. SGDBR: sampled grating distributed Bragg reflector; SIL: self-injection locking.

limited to just 1000 h for quantum well lasers on Si substrates. Recently, tremendous progress has been made in solving all three problems. GaP, GaAs, or AlAs layers have been used to eliminate antiphase domains.[43] The use of strained layer superlattices and thermal anneals has resulted in the reduction of the TDD from 5×10^8 to just $1 \times 10^6/\text{cm}^2$.[44] The third problem has been mostly solved by improved templates, and higher confinement in the separate confinement heterostructure (SCH) so the total epitaxial thickness is reduced from 8 μm in the past to just 3 μm. Further, the growth of InAs quantum dots results in trapping of dislocations, and the darkline defect growth that destroyed QW lasers has been largely mitigated. Consequently, the room temperature lifetime of QD lasers on silicon has increased from just 1000 h to over 100×10^6 h. However, the high temperature lifetime of lasers of silicon, which is critically important for data center applications, has been much shorter. Fortunately, the mechanism limiting the high temperature lifetime has been recently identified, namely, propagation of threading dislocations during cooldown, causing a high density of misfit dislocations in the active layer.[45] The solution to this problem is the inclusion of blocking layers on either side of the active layer so the misfit dislocations do not occur in the active layer and do not result in carrier recombination.[46] Consequently, the high temperature (80 °C) reliability of monolithic QD lasers grown on silicon is now 22 years, and the performance of QD lasers has also dramatically improved. Whether lasers are integrated at all, and whether they are hybrid, heterogeneous, or monolithically integrated with the PIC depends on many issues, including process integration, packaging, yield, reliability, and cost.

C. Application-driven silicon photonic integrated circuits

Data-intensive applications supported by 5G networks and distributed edge computing will also come to benefit from the economics and scale of integrated silicon photonics, both as a data transport technology as well as a sensing technology. As the radio access network transforms to accommodate significantly higher throughput, silicon photonics-based connectivity will find use cases in the radio baseband units and front, mid, and back-haul network transport.[47] In autonomous driving, FMCW (frequency modulated continuous wave) LIDAR has emerged as a key next-generation technology based on its capability to measure both velocity and range with high resolution. These systems require dense integration of multiple optical components including lasers, amplifiers, phase and amplitude control, low-noise photodiodes, mode converters, and optical waveguides. Intel recently demonstrated that their hybrid silicon platform can enable such optical integration on a silicon chip in a scalable high-volume manufacturing process, thus enabling chip-scale solid-state LIDAR.[29,48] The use of silicon photonics elements as the compute platform itself is also starting to gain attention, especially as Moore's law struggles to scale with workloads and power consumed in AI/ML applications. Neuromorphic photonics promises orders of magnitude improvements in both speed and energy efficiency over digital electronics.[49] Another emerging field in silicon photonics is programable photonic circuits that implement programmability in large and complex Si PICs for varied optical functions and benefits the device configuration and control.[50] Finally, the use of silicon photonics is one of a few promising methods that could realize the potential of quantum computing.[51]

VII. CONCLUSIONS

High speed data processing and transport form two key pillars of modern computing systems. Photonics and optical fibers provide the connectivity necessary for scaling systems requiring physical reach both in scale-up and scale-out applications. The growth of transistor counts on individual silicon dies continues to expand but is not enough to cover the applications needed for the future, where thousands of nodes can form a compute system. Connecting these thousands of compute and fabric silicon elements at a power and cost that is required for these applications is becoming increasingly inefficient using historical architectures. The technology of silicon photonics provides a pathway to massively reduce the cost, complexity, and power required for creating these photonic connections. The use of co-packaging and integration of photonics with large ASIC I/Os allows for elimination of complex and power hungry electrical links from the ASICs to the optical devices. The semiconductor foundation of silicon photonics also enables the continued scaling in bandwidth and reduction of power to the ever increasing needs of high bandwidth interconnects.

AUTHORS' CONTRIBUTIONS

N.M. and C.X. contributed equally to this manuscript. All authors contributed to the manuscript and figures. J.E.B. supervised the project.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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