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On the intersecting behaviour of experimental forward bias current–voltage (I–V) characteristics of $Al/SiO_2/p$-Si (MIS) Schottky diodes at low temperatures

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Abstract

In this study, we have investigated the intersection behaviour of forward and reverse bias current–voltage (I–V) characteristics of $Al/SiO_2/p$-Si Schottky diodes in the temperature range of 79–325 K. The crossing of the experimental semi-logarithmic $\ln(I)$–V curves appears as an abnormality when seen with respect to the conventional behaviour of ideal Schottky diodes. Experimental results show that this crossing of $\ln(I)$–V curves is an inherent property of even Schottky diodes. The ideality factor n was found to decrease, while the zero-bias Schottky barrier height (SBH) Φ_{B0} increases with increasing temperature. The conventional Richardson plot is found to be nonlinear in the temperature range measured. However, the $\ln(I_0/T^2)$ versus $1000/nT$ plot gives a straight line corresponding to activation energy 0.233 eV. It is shown that the values of series resistance R_s estimated from Cheung's method were strongly temperature dependent and abnormally increased with increasing temperature. In addition, the temperature dependence of energy distribution of interface states density N_{ss} profiles was obtained from the forward bias I–V measurements by taking into account the bias dependence of the effective barrier height Φ_e and ideality factor n. All these behaviours indicate that the thermionic emission (TE) cannot be the main current transport mechanism, especially at low temperatures.

1. Introduction

It has been well known that there are currently a vast number of reports on experimental studies of metal–semiconductor (MS), metal–insulator–semiconductor (MIS) Schottky barrier diodes (SBDs) and solar cells of I–V characteristics which are still intensively studied [1–14]. In addition, there are a vast number of theoretical studies on these devices [15–19]. The analysis of I–V characteristics of the SBDs only at room temperature does not give detailed information about their current transport mechanisms or the nature of barrier formation at the MS interface. However, the temperature dependence of the I–V characteristics allows us to understand different aspects of device characteristics. In general, the forward bias I–V characteristics of these devices deviate from the ideal TE theory [3–6, 8, 20]. It was often observed that the ideality factor n was found to decrease, while the zero-bias SBH Φ_{B0} increases with increasing temperature. The changes are more significant especially at low temperatures. Therefore, at low temperatures the standard TE theory fails to apply these results. Especially at low temperatures ($T < 150$ K), the lower barrier patches carry a larger fraction of the current because of the

lower temperature dependence of the current through these patches. The decrease in the SBH, at low temperatures, leads to nonlinearity in the conventional Richardson plot. Lately, the nature of origin of the decrease in the SBH and increase in ideality factor with a decrease in temperature in some studies [6, 15, 20–24] have been successfully explained on the basis of a TE mechanism with Gaussian distribution of the SBH. The other parameter that exhibited in some cases abnormal behaviour is the R_s. Chand and Kumar studied its temperature dependence in Pd_2 Sip-Si (111) Schottky diodes [4]. They attributed the sharp increase of the series resistance below 110 K to the lack of free charge carries in semiconductor at low temperatures. Practically the same temperature dependence of series resistance was reported in [25] and the importance of R_s influence on the evaluated barrier parameters was demonstrated on experimental structures [26]. Also the effect of forward bias *I–V* curves intersection was studied by Chand [15, 27] and Chand and Bala [28]. They discussed the so-called analytically and numerically generated *I–V* curves in their works. In addition, Horvath *et al* studied its temperature dependence in $Al/SiO_2/p$-Si Schottky diodes [14]. They observed the forward bias *I–V* curves intersection at room temperature.

In this study, the experimental forward and reverse bias *I–V* characteristics of $Al/SiO_2/p$-Si Schottky diodes with an insulator layer are reported in the temperature range of 79–325 K. The barrier height, ideality factor and series resistance were extracted from forward bias *I–V* measurements. The zero-bias barrier height decreases practically linearly with decreasing temperature to relatively low values. The series resistance R_s estimated from Cheung's method was strongly temperature dependent and abnormally increased with increasing temperature. This behaviour could be expected for semiconductors in the temperature region where there is no carrier freezing-out which is non-negligible at low temperatures. In addition, we investigated the reason of the intersecting of Ln *I–V* curves.

2. Experimental procedure

The $Al/SiO_2/p$-Si (MIS) structure was fabricated on a quarter of 2 inch diameter float zone ⟨100⟩ p-type (boron doped) single crystal silicon (Si) wafer having a thickness of 350 μm with 0.8 Ω cm resistivity. For the fabrication process the Si wafer was degreased in organic solutions of $CHClCCl_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 an H_2O_2 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionized water of resistivity of 18 MΩ cm for a prolonged time. Preceding each step, the wafer was rinsed thoroughly in de-ionized water. The high purity aluminium (Al) with a thickness of ≈2000 Å was thermally evaporated from tungsten filament onto the whole back side on the p-Si wafer at a pressure of $\approx 1 \times 10^{-6}$ Torr in liquid nitrogen trapped oil-free ultra high vacuum pump system. The ohmic contact was formed by sintering the evaporated Al back contact at 700 °C for 45 min in a flowing dry oxygen ambient at a rate of 1 lt min^{-1}. This process served both to sinter the Al and to form the required thin interfacial oxide layer (SiO_2) on the upper surface of the p-Si wafer. After oxidation, circular dots of 1 mm diameter and 2000 Å thick

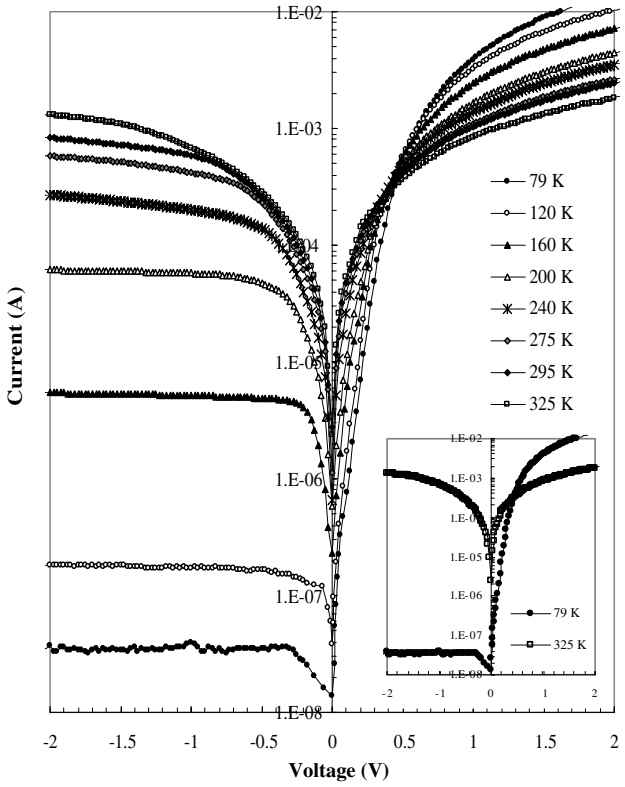

Figure 1. The forward and reverse *I–V–T* characteristics of the $Al/SiO_2/p$-Si Schottky diode.

Al contacts were deposited onto the oxidized surface of the wafer through a metal shadow mask in liquid nitrogen trapped vacuum system. The interfacial layer thickness was estimated to be about 35 Å from high frequency (1 MHz) measurement of the oxide capacitance in the strong accumulation. The *C–V* measurements were performed at 1 MHz by using HP 4192A LF impedance analyser (5 Hz to 13 MHz) and test signal of 40 mV_{rms}. *I–V* measurements were performed by the use of a Keithley 220 current source, a Keithley 614 electrometer. The sample temperature was always monitored by using a copper–constantant thermocouple and a Lakeshore 321 auto-tuning temperature controller with sensitivity better than ±0.1 K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

Figure 1 shows the forward and reverse bias semi-logarithmic *I–V* characteristics of the $Al/SiO_2/p$-Si structure, measured as a function temperature.

As shown in figure 1, the experimental *I–V* curves exhibit excellent rectification characteristic especially at low temperatures. The forward bias *I–V* characteristics are linear on a semi-logarithmic scale at low forward bias voltages but deviate considerably from linearity due to the effect of series resistance (R_s), the interfacial insulator layer (SiO_2) and the interface states (N_{ss}) when the applied voltage is sufficiently large. As can be seen in figure 1, an interesting feature of the forward bias semi-logarithmic *I–V* curves is the almost common intersection point of all the curves at a certain bias

Table 1. Temperature dependent values of various parameters determined from the forward bias *I–V* characteristics of the studied Al/SiO_2/p-Si Schottky diode.

T (K)	n (I–V)	Φ_{B0} (I–V) (eV)	Φ_{B0} ($H(I)$) (eV)	n (dV/dLnI)	R_s (dV/dLnI) (Ω)	R_s ($H(I)$) (Ω)
79	5.50	0.196	0.155	7.045	161.58	140.62
120	4.60	0.295	0.241	4.222	244.46	186.53
160	4.54	0.376	0.305	3.891	259.71	235.01
200	4.37	0.461	0.376	3.026	397.87	384.89
240	4.32	0.540	0.428	2.986	484.95	484.19
275	4.12	0.614	0.484	2.580	655.14	654.19
295	4.00	0.656	0.514	2.354	721.93	719.81
325	3.72	0.724	0.568	1.630	973.33	976.30

voltage and for this voltage point the current through the diode is temperature independent. Similar results have been obtained recently by simulation of forward bias *I–V* curves of Schottky diodes [15, 16, 19, 28]. It was found that the presence of series resistance in diode causes bending due to current saturation and plays subtle role in keeping this crossing hidden. In addition, Chand [15] reported that this crossing of forward bias Ln *I–V* curves for a homogeneous Schotkky diode can only be realized in curves with zero series resistance. Osvald [29] showed theoretically that the presence of the R_s is a necessary condition of intersection of *I–V* curves. However, Horvath *et al* reported that they found an intersection point in the forward bias *I–V* characteristics of Al/SiO_2/Si structure with SiC nanocrystals by experiment [14]. For our sample, the R_s is shown to play a crucial role in effecting forward bias *I–V* curves of SBD and show the intersection behaviour of the forward bias *I–V* curves. This behaviour of the crossing of *I–V* curves appears as an abnormality when seen with respect to the conventional behaviour of SBDs.

According to the TE theory, the forward bias *I–V* relationship for Schottky diode is given as follows [30, 31]:

$$I = I_0\left[\exp\left(\frac{qV_D}{nkT}\right) - 1\right] \tag{1}$$

where V_D is the voltage across the MIS structure and is described as $V_D = V - IR_s$, where V is the definite forward bias voltage, the IR_s term is the voltage drop across series resistance of the device, n is the ideality factor, k is the Boltzmann constant and T is the temperature in Kelvin. I_0 is the reverse saturation current and expressed as

$$I_0 = A^*AT^2\exp(-q\Phi_{B0}/kT) \tag{2}$$

where the quantities A^*, A, Φ_{B0} are the effective Richardson constant that equals 32 A cm^{-2} K^2 for p-type Si, the diode area and the zero-bias barrier height, respectively. The saturation current I_0 was obtained by extrapolating the linear portion of the Ln *I–V* curve to the intercept point with the current axis at zero bias at each temperature and the zero bias barrier height Φ_{B0} values were calculated from equation (2). The ideality factor was calculated from the slope of linear region of ln *I–V* plots at forward bias. The change in n and Φ_{B0} with temperature is seen in table 1. As shown in table 1, the Φ_{B0} and n determined from semi-log forward *I–V* plots were found to be a strong function of temperature. The values of ideality factor n were found to increase, while the values of Φ_{B0} decrease with decreasing temperature. As explained in [4, 20, 27, 32], since the current transport across the MS interface is a temperature-activated process, electrons at a low temperature are able to surmount the lower barrier and therefore the current transport will be dominated by the current flowing through the patches of lower Schottky barrier height and a larger ideality factor. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant barrier height will increase with the temperature and bias voltage.

The downward concave curvature region (non-ideal behaviour) of the forward bias *I–V* plots at a sufficiently large voltage has been attributed to the presence of N_{ss}, which equilibrates with the semiconductor, apart from the R_s effect of the neutral region in the Schottky diode [3, 22, 26, 33, 34]. Furthermore, the ideality factor, the barrier height and the series resistance values have also been determined by analysis of Cheung and Cheung [34] in the high current range where the *I–V* characteristic is not linear. From equation (1), the following function can be written as

$$\frac{dV}{d\,\mathrm{Ln}\,I} = n\frac{kT}{q} + IR_s \tag{3}$$

$$H(I) = V + n\frac{kT}{q}\,\mathrm{Ln}\left(\frac{I}{AA^*T^2}\right) \tag{4}$$

and $H(I)$ is given as follows:

$$H(I) = n\Phi_{B0} + IR_s. \tag{5}$$

In figure 2, experimental dV/d(LnI) versus I and $H(I)$ versus I plots as a function of temperature are presented for Al/SiO_2/p-Si MIS structure. Equation (3) should give a straight line for the data of downward curvature region in the forward bias *I–V* characteristic. Thus, a plot of dV/d(LnI) versus I will give R_s as the slope and nkT/q as the y-axis intercept. From figure 2(*a*), using equation (3), the values of n and R_s were found at different temperatures presented in table 1. Using the n value determined from equation (3), and the data of downward curvature region in the forward bias *I–V* characteristic in equation (4), a plot of $H(I)$ versus I will also lead to a straight line (figure 2(*b*)) with the y-axis intercept being equal to $n\Phi_{Bo}$.

The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of this approach. From figure 2(*b*), using equation (5), the values of Φ_{B0} and R_s were calculated at different temperatures (table 1). As shown in table 1, the Φ_{B0} and R_s values obtained by different techniques are in good agreement with each other and increase strongly with increasing temperature. These behaviours are an obvious disagreement with the reported

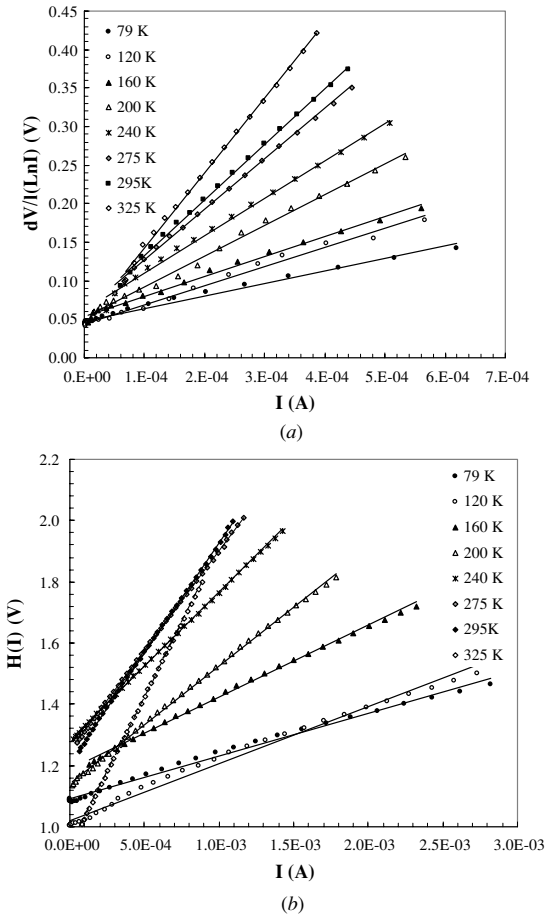

Figure 2. The characteristics of the $Al/SiO_2/$ p-Si Schottky diode at different temperatures: (*a*) $dV/d\ln(I)$ versus I and (*b*) $H(I)$ versus I.

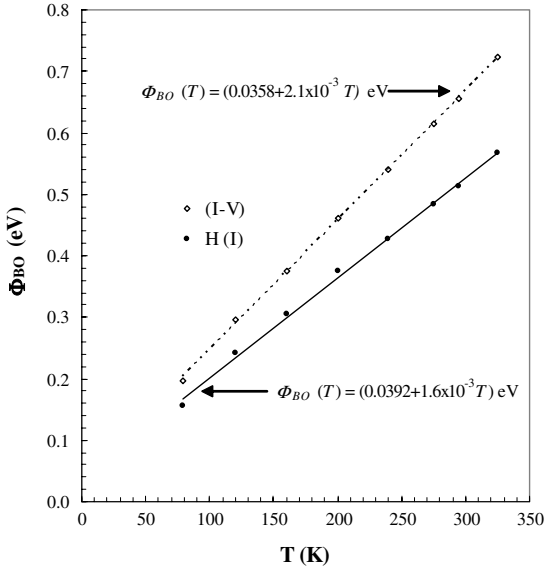

Figure 3. Temperature dependent zero-bias barrier height obtained from forward bias *I–V* characteristics for the studied $Al/SiO_2/$ p-Si Schottky barrier diode.

negative temperature coefficient of both the Φ_{B0} and R_s (figures 3 and 4, respectively).

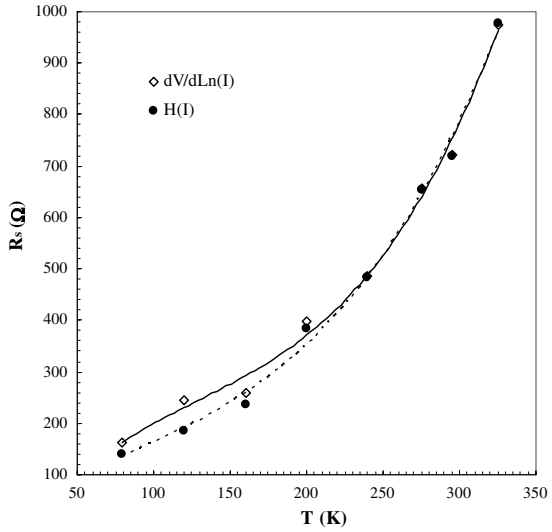

Figure 4. The temperature dependence of the R_s for the studied $Al/SiO_2/p$-Si Schottky diode.

As can be seen in table 1 and figure 4, the R_s calculated from the Cheung function shows an unusual behaviour that it increases with increase of temperature. Such temperature dependence is an obvious disagreement with the reported negative temperature coefficient of the R_s. Sharp increase of the R_s below 120 K was attributed to the lack of free charge at low temperatures. At higher temperatures, the contact resistance and the resistance of outer connections are probably the prevalent sources of the R_s. The series resistance increases with increasing temperature as could be expected for semiconductors in the temperature region where there is no carrier freezing out which is non-negligible only at low temperatures [30]. Similar temperature dependence was obtained both experimentally [35] and theatrically [16].

To determine the barrier height in another way, the conventional Richardson plot can be used and equation (2) can be rewritten as

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(AA^*T^2) - \frac{q\Phi_{B0}}{kT}. \tag{6}$$

Figure 5 shows the energy variation of $\ln(I_0/T^2)$ versus $1000/T$ and $1000/nT$. While $\ln(I_0/T^2)$ versus $1000/T$ is found to be nonlinear, the $\ln(I_0/T^2)$ versus $1000/nT$ plot gives a straight line. The experimental data of $\ln(I_0/T^2)$ versus $1000/nT$ plot are fit asymptotically with a straight line, yielding an activation energy of 0.233 eV, and the Richardson constant (A^*) value of 1.9×10^{-9} A cm^{-2} K^{-2} is determined from the intercept at the ordinate of this experimental plot, which is much lower than the known value of 32 A cm^{-2} K^{-2} for p-Si.

The density distribution curves of the interface state N_{ss} in equilibrium with the semiconductor can be determined from the forward bias *I–V* characteristics at each temperature. The effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and the interface states located between interfacial insulator layer and semiconductor, and is given by [2, 3, 9]

$$\Phi_e = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right) V. \tag{7}$$

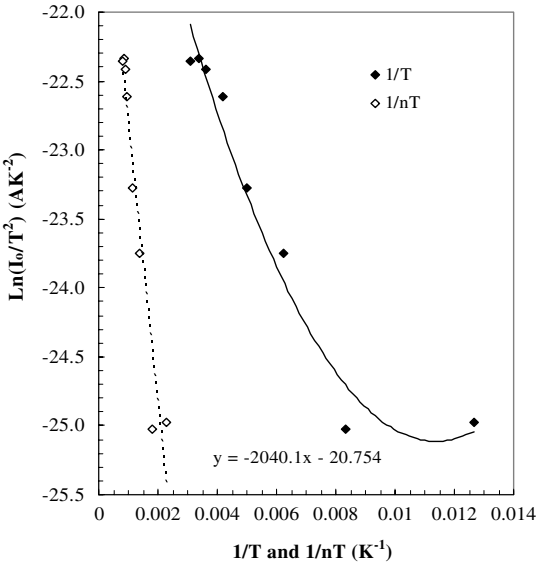

Figure 5. Richardson plots of the $\ln(I_0/T^2)$ versus $1000/T$ and $1000/nT$ for the studied Al/SiO_2/ p-Si Schottky diode.

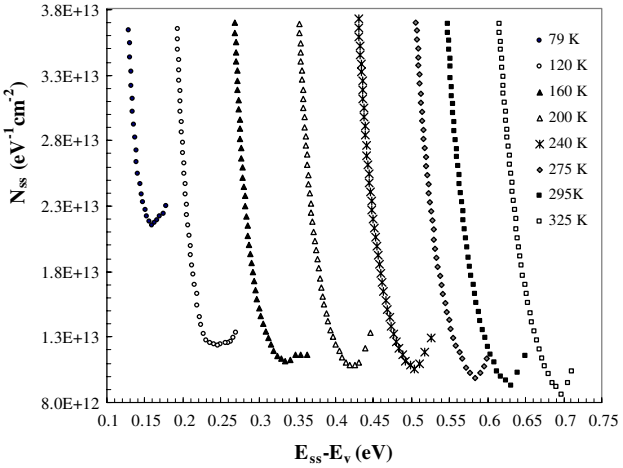

Figure 6. Density of interface states N_{ss} as a function of $E_{ss} - E_v$ deduced from the *I–V* data at various temperatures for the studied Al/SiO_2/ p-Si Schottky diode.

For the MIS diode having interface states N_{ss} in equilibrium with semiconductor, the ideality factor n becomes greater than unity and can be written as

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right]. \tag{8a}$$

This expression for the N_{ss} as deduced by Card and Rhoderick [1] is reduced to

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1)\frac{\varepsilon_s}{W_D}\right] \tag{8b}$$

where ε_s and ε_i are the permittivities of the semiconductor and the interfacial layer, respectively, δ is the thickness of the insulator layer, W_D is the width of the space charge region and N_{ss} is the density of the interface states in equilibrium with the semiconductor. For each temperature, the values of N_{ss} were obtained from equation (8*b*) by substituting $\delta = 35$ Å, $\varepsilon_i = 3.8\varepsilon_0$, $\varepsilon_s = 11.8\varepsilon_0$ [30]. The thickness of the film was calculated from capacitance measurements (1 MHz) and found to be about 35 Å, and this can usually make the values of ideality factor greater than unity [31]. It is seen in figure 6 that the values of interface states density for each temperature adequately high are of the order of 10^{13} eV^{-1} cm^{-2}. In a p-type semiconductor, the energy of interface states N_{ss} with respect to the top of valance band E_v at the surface of the semiconductor is given by

$$E_{ss} - E_v = -q(\Phi_e - V). \tag{9}$$

From figure 6 for all temperatures it is seen an exponential increase in the interface state density from midgap towards the top of valance band. We have observed then that the values of N_{ss} increase with decreasing temperature. This case is a result of molecular restructuring and reordering of the metal–semiconductor interface under the effect of temperature [36].

4. Conclusions

The forward and reverse bias *I–V* characteristics of the Al/SiO_2/p-Si (MIS) Schottky barrier diode were measured in the temperature range of 79–325 K. Using the evaluation of the experimental forward bias *I–V* characteristics reveals an increase of the Φ_{B0} and a decrease of the ideality factor with increasing temperature; the changes are quite significant at low temperatures. The activation energy of 0.233 eV obtained from Ln (I_0/T^2) versus $1/nT$ corresponds to the barrier height at low temperature. The temperature dependence of energy distribution of N_{ss} profiles was obtained from the forward bias *I–V* measurements by taking into account the bias dependence of the effective barrier height Φ_e and ideality factor n. At the same time, the N_{ss} values as a function of $E_{ss} - E_v$ decreased with increasing temperature. It was seen to appear a minimum and shifting towards the valance band in the N_{ss} plots. The improvement obtained by the temperature effect is probably due to thermal restructuring and reordering of the Si/SiO_2 interface. For our sample the R_s is shown to play a crucial role in effecting forward bias *I–V* curves of SBD. The values of R_s show an unusual behaviour that it increases with increase of temperature. Sharp increase of the R_s below 120 K was attributed to the lack of free charge at low temperatures. Also, the forward bias *I–V* curves show the intersection behaviour. This behaviour of the crossing of *I–V* curves appears as an abnormality when seen with respect to the conventional behaviour of SBDs. In conclusion, the TE theory cannot be the decisive current mode in SBDs at low temperatures.

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