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PHYSICAL CHARACTERISTICS OF AL/N-CDS THIN-FILM SCHOTTKY DIODE AT HIGH TEMPERATURES

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ABSTRACT
Cadmium sulphide (CdS), a member of group II-VI semiconductors, is a promising material based on its applications. The present investigations describe the preparation and electrical characterization of CdS thin films. CdS thin films with thickness of 1000 nm were deposited by vacuum evaporation at room temperature. Characteristic parameters of Schottky junctions formed by a thermal vapor deposition of 500 nm of Al films on pre-coated CdS glass substrates were obtained experimentally from the I-V characteristics in the temperature range of 303–393 K. Diode parameters, such as the zero-bias barrier height φ_{b0}, flat band barrier height Φ_{bf}, ideality factor η, and series resistance R_S were investigated using the thermionic emission method.

Keywords: Barrier characteristics; Diode; High temperature I-V; Schottky junction

1. INTRODUCTION
Metal-semiconductor (MS) structures are important research tools in the characterization of new semiconductor materials; at the same time, the fabrication of these structures plays a vital role in constructing useful technological devices (Reddy et al., 2011). The physical properties of the interfaces between metals and semiconductors depend on surface preparation conditions (Rhoderick & Williams, 1988; Sarpatwari, 2009). Many models have been developed to understand the origins and behaviors of potential barriers at the interfaces of MS contacts. Significant efforts are being made to arrive at a more realistic interpretation of characterizing parameters of real Schottky diodes (Margaritondo, 1999; Mathai et al., 2010). Until now, the current-voltage (I-V) measurement method has been used widely to explore the trap states in the Schottky diode by evaluating the diode ideality factor (Jang et al., 2005). The use of CdS thin film polycrystalline semiconductors has attracted interest for an expanding variety of applications in various electronic and optoelectronic devices (Gupta et al., 2009; Kumar et al., 2011; Chand & Kumar, 1997). Cadmium sulphides are compound semiconductors with a wide range of potential applications (Kathirvel et al., 2011; Saikia et al., 2012). These materials have existed in cubic or hexagonal forms; they are wide-direct-band gap semiconductors (Mahdi et al., 2009). Many techniques have been used for the deposition of CdS thin films. These include thermal evaporation, sputtering, chemical bath deposition, spray pyrolysis, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy, electro deposition, and photochemical deposition (Barote et al., 2011; Ogah et al., 2008; Guneria et al., 2010; Rusu et al., 2005). MS contacts are used frequently in integrated circuits and light detectors, and as solar cells.

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Schottky barrier diodes (SBDs), such as Al/CdS, which has a rectifying nature, are among the simplest MS contact devices (Barote et al., 2011). Thus, the primary objectives of this study are the preparation of Schottky diodes and the examination of its electrical parameters. Electrical properties depend highly on chemical composition. For this study, we carried out energy dispersive analysis of X-rays (EDAX). Based on I-V characteristics of the Al/n-CdS junction at high temperatures, we calculated junction parameters, such as barrier height, ideality factor, series resistance, and saturation current.

2. EXPERIMENTAL

CdS films of 1000 nm thickness were evaporated thermally and deposited on chemically and ultrasonically cleaned glass substrates with the help of a vacuum coating unit (12A4D, HHV). All components of the vacuum chamber were cleaned first with acetone. A clean evaporation source (molybdenum boat) was fixed in the filament holder inside the chamber. A CdS charge formed with a purity of 99.99% was kept in the molybdenum boat. The glass substrate was cleaned by acetone and ultrasonic vibrations. The substrate was kept on the substrate holder, and the crystal monitor was placed near it to measure the thickness during the deposition process. The chamber was evacuated at a pressure greater than 1.33×10^{-3} Pa with the combination of rotary and diffusion pumps. A vacuum of 1.33×10^{-3} Pa was attained in the vacuum chamber; to obtain the Schottky barrier, Al film of 500 nm was deposited on CdS thin films using thermal evaporation, then I-V measurements were characterized to analyze the parameters of the Al/n-CdS junction.

The EDAX of the grown crystals in the present investigation was carried out using the electron microscope (Make: Philips, Model: XL 30 ESEM) at the Sophisticated Instrumentation Center for Applied Research and Testing (SICART). The stoichiometric proportion of the constituent elements data was obtained from EDAX.

The I-V-T data were acquired using Keithley's 4200 semiconductor characterization system, along with Lakeshore's Closed Cycle Refrigerator (CCR 75014). The temperature was monitored and controlled by a Lakeshore temperature controller (Model 340) with an accuracy of ±0.1K. I-V data were taken from 300 K down to 40 K at intervals of 20 K. Therefore, the measured I-V characteristics were in the temperature range of 300–40 K.

3. RESULTS AND DISCUSSION

3.1. EDAX

EDAX of prepared films was carried out using the electron microscope at SICART. The results are shown in Figure 1.

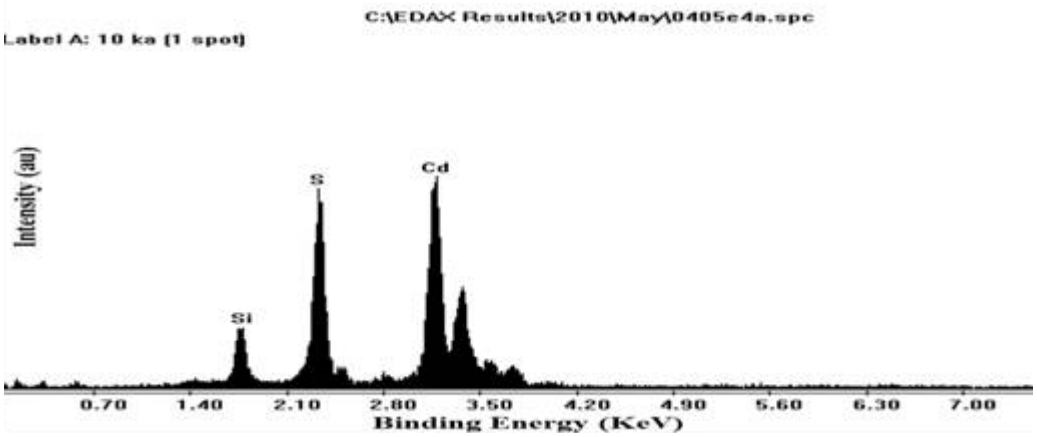

Figure 1 EDAX results of vacuum-evaporated CdS thin film at room temperature

The stoichiometric proportion of the constituent elements obtained from EDAX was in agreement with expected values (Table 1).

Table 1 Elemental proportion of Cd and S in CdS thin films characterized by EDAX

Elements	Wt % obtained from EDAX	Wt % calculated theoretically
Cd	69.39	77.80
S	22.37	22.19
Si	8.24	-

It is seen from the results shown in Table 1 that the film deposited was nearly stoichiometric, and the presence of Si was attributed to the glass substrate.

3.2. Current-voltage (I-V) Measurements of Al/n-CdS Schottky Diode at Varied Temperatures

Various methods are used to determine Schottky barrier parameters; these include current-voltage (I-V) analysis, capacitor-voltage (C-V) analysis, photoelectron spectroscopy, activation energy method, etc. (Farag et al., 2009; Lakshmi et al., 2012; Sze, 1985; Werner, 1988). The I-V analysis method is the simplest of all methods since it involves direct measurement of current voltage and provides first-hand information about the nature of the developed barriers across the interface. For this study, the I-V-T data were acquired using Keithley's 4200 semiconductor characterization system. The nature of the I-V characteristics of Al/n-CdS Schottky diodes at high temperatures are shown in Figure 2.

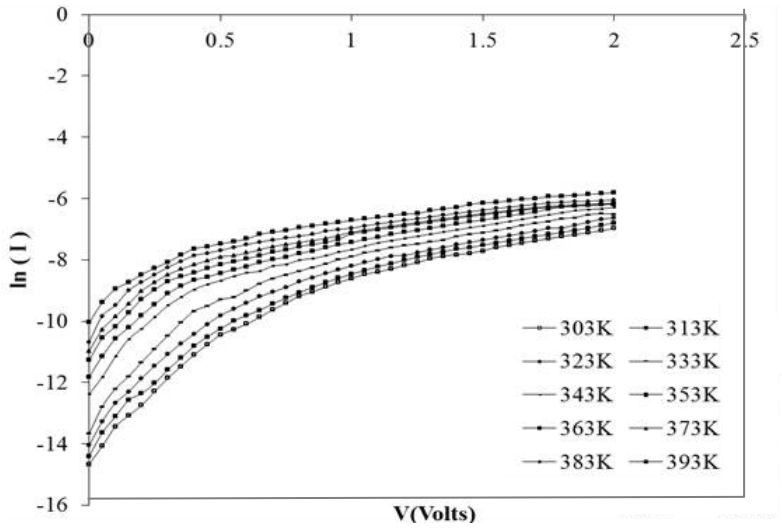

Figure 2 I-V characteristics of Al/n-CdS Schottky diode at high temperatures

From Figure 2, it is seen that the current under forward bias was significantly high. Current transport through the SBD was due to majority carriers and adherence to the thermionic emission model (Rhoderick & Williams, 1988; Tung, 2001) at low forward biases V.

Based on the thermionic emission theory, the current-voltage characteristics are given by the relationship shown below:

$$I = I_0 \exp\left(\frac{qv}{\eta kT}\right)\left(1 - \exp\left(\frac{-qv}{kT}\right)\right) \quad (1)$$

where V is the applied voltage drop across the junction barrier, q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature in Kelvin, η is the diode ideality factor, and I_0 is the saturation current—expressed (Tugluoglu et al., 2004; Patel et al., 2010) as:

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_{bo}}{kT}\right) \quad (2)$$

where A is the diode area and A* is the Richardson constant 23.4 $A \cdot cm^{-2} \cdot K^{-2}$ for n-type CdS (Patel et al., 2010). By using the value of I_o, the barrier height Φ_{b0} can be evaluated using the following equation:

$$\Phi_{bo} = \frac{kT}{q}\left(\frac{AA^*T^2}{I_0}\right) \quad (3)$$

where Φ_{b0} is the zero-bias barrier height, q is the electron charge, k is Boltzmann's constant, T is temperature, V is the forward-bias voltage, A is the effective diode area, and A* is the Richardson constant of 23.4 $Acm^{-2}K^{-2}$. The ideality factor η can be written as:

$$\eta = \left(\frac{q}{kT}\right)\left(\frac{dv}{d\ln(I)}\right) \quad (4)$$

Also, the flat band barrier height Φ_{bf} is given by:

$$\Phi_{bf} = \eta\Phi_{b0} - (\eta - 1)\left(\frac{kT}{q}\right)\ln\left(\frac{N_C}{N_A}\right) \quad (5)$$

where N_c and N_A are effective density of states and carrier concentration, respectively.

The electrical I-V measurements of the Al/n-CdS Schottky diode were taken in the temperature range of 303–393K. The experimental values of Φ_{b0} and the ideality factor were determined from intercepts and slopes of the forward bias lnI versus voltage (V) plot according to the thermionic theory. The values of ideality factors, zero-bias barrier height, and flat band barrier height varied from 3.465eV, 0.502eV, and 0.838eV to 1.299eV, 0.559eV, and 0.585eV, respectively (Table 1). From Figure 3, it can be seen that the values of η, Φ_{b0}, and Φ_{bf} were functions of temperature in the range of 303–393K. Furthermore, we noted that the flat band barrier height and ideality factor decreased with an increase in temperature, while the zero-bias barrier height increased with an increase in temperature. Since the current transport across the MS interface is a temperature-activated process, electrons at low temperatures are able to surmount the lower barriers; therefore, current transport is dominated by the current flowing through the patches of lower schottky barrier height (SBH) and a large ideality factor. In this research, we noted that as the temperature increased, a greater number of electrons exhibited sufficient energy to surmount the higher barrier, as shown in Figure 3 (Naik & Reddy, 2012).

The zero-bias barrier height φ_{b0} decreased with decreasing temperature, and the flat band barrier height φ_{bf} increased with decreasing temperature, as shown in Figure 3. Various factors can contribute to a reduction in the zero-bias barrier height at lower temperatures, such as non-homogeneity present at the Al/n-CdS interface, generation and recombination currents in the space charge region, the effect of the image force, and, at low temperatures, tunneling processes and thermally assisted tunneling processes from states in the forbidden gap. The ideality factor

η tended to decrease, showing decreasing non-ideal behavior with increasing temperature (Figure 3).

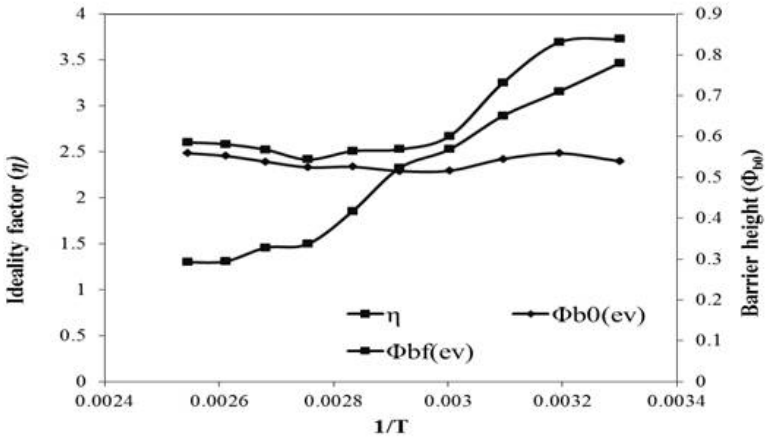

Figure 3 Variations of η, φ_{b0}, and φ_{bf} based on temperature

This behavior may have been due to current transport across the Al/n-CdS interface as a result of a thermally activated process; at low temperatures, electrons are able to surmount the lower barriers (Karadeniz et al., 2005). Therefore, current transport is dominated by the current flowing through patches with a lower Schottky barrier height and a greater ideality factor. The value of an ideality factor greater than one is associated with Fermi level pinning at the interface (Brillson, 1978; Tersoff, 1985) or relatively large voltage drops in the interface region. An interfacial oxide layer may be the possible cause for a higher value of the ideality factor.

Table 2 Ideality factor, series resistance, and Schottky barrier heights of Al/n-CdS Schottky diode in the temperature range of 303–393 K

Temperature (K)	η	φ_{b0} (eV)	φ_{bf} (eV)	Rs (Ω)
303	3.465	0.502	0.838	1710
313	3.158	0.508	0.830	1695
323	2.891	0.512	0.731	1467
333	2.529	0.515	0.601	1381
343	2.325	0.516	0.568	1072
353	1.853	0.524	0.564	974
363	1.497	0.526	0.543	961
373	1.457	0.538	0.567	955
383	1.308	0.552	0.581	922
393	1.299	0.559	0.585	769

The series resistance R_S of the neutral region of the semiconductor bulk (between the depletion region and ohmic contact) and the variation of series resistance is shown in Figure 4. From these curves, it was deduced that the series resistance decreased when the temperature increased from 303 K to 393 K. Generally, a resistance series decreases when the temperature increases, and it tends toward a constant value.

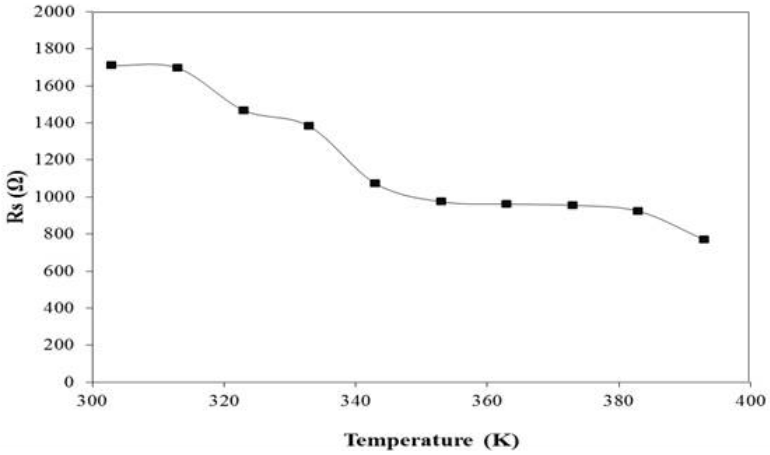

Figure 4 Variation of series resistance for Al/CdS Schottky diode at different temperatures.

4. CONCLUSION

The CdS thickness of 1000 nm was deposited using CdS in charge form. The Schottky barrier Al films of 500 nm were deposited on CdS thin films using the thermal evaporation technique at room temperature. The I-V measurements of the Al/n-CdS Schottky diode were investigated in the range of 303–393K, and the parameters of this diode—ideality factor, flat band barrier height, zero-bias barrier height, and series resistance—were evaluated using the thermionic theory. The zero-bias barrier height increased and the flat band barrier height, ideality factor, and series resistance decreased with increases in temperature.

5. ACKNOWLEDGEMENT

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