

Dislocations in Crystalline Silicon Solar Cells

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Dislocation is a common extended defect in crystalline silicon solar cells, which affects the recombination characteristics of solar cells by forming deep-level defect states in the silicon bandgap, thereby reducing the lifetime of minority carrier. Hence, reducing the impact of defects on device performance is an effective strategy to optimize the performance of photovoltaic devices. This article reviews the observation and engineering of dislocation in Si solar cell. The structure and deformation of Si can be directly observed by chemical etching combined with electron microscopy. Also, more information about dislocation is obtained indirectly by monitoring the electrical and optical properties of Si. The classification, density, distribution of dislocations, and their interactions with other defects in Si can affect the lifetime of minority carriers and thereby reduce the performance of Si solar cells. In order to achieve higher cell efficiency, crystals with less or even no dislocation should be obtained. In addition to the specification of controlling the relevant parameters during the growth of silicon ingots to obtain the minimum dislocation density, it is necessary to study the behavior of dislocation in Si wafers under the combined action of external stress, temperature, and other defects.

1. Introduction

Solar cells have attracted extensive research attention in recent years due to their unique advantages, such as mature technology of fabrication, renewable and clean energy resources, gradually decreased cost, and most expectable energy for carbon neutrality.^[1] Crystalline silicon solar cells, including monocrystalline and polycrystalline silicon, have captured 90% of the market share by 2018.^[2] However, the compromise between cost and efficiency is holding back further market share of solar cells. To achieve the goal of grid parity, it is necessary to increase the efficiency of solar cells at a minimal cost.^[3] However, along with the cost reduction through the optimization of production process

and structural innovation of the solar cells, the efficiency and long-term stability of the crystalline solar cells are never satisfactory. The key factor influencing the performance of solar cells is the existence of defects, especially in crystalline silicon. **Figure 1** provides an overview of the passivation emitter rear contact (PERC) solar cell, which is currently the most commonly used solar cell. It can be clearly seen that the recombination caused by defects is still an urgent problem for solar cells.

Therefore, dislocations, i.e., one of the most detrimental types of defects limiting the performance of crystalline silicon solar cells, have been widely studied by several research groups. According to the calculation results, a reduction of two orders of magnitude in dislocation density increases the energy conversion efficiency of a polycrystalline silicon solar cell by about 50%.^[4] Even in recent years, monocrystalline silicon cells

have gradually taken over the solar cell market and dislocations still render a significant impact on the performance of commercial solar cells. Several studies have contributed to the inhibition of dislocation formation in the crystal growth process. Moreover, the techniques of reducing dislocation density in Si are dislocation passivation and gettering treatments of fast-diffusing metal impurities from dislocations. However, as metallic impurities and oxide precipitates are attracted to the dislocation core, the density of the dislocation cannot be effectively controlled.^[5] Therefore, it is urgent to find a new dislocation density control scheme. Meanwhile, reviewing recent work related to dislocations to understand the principle and basic activities of dislocation is quite helpful.

This article is divided into the following respects: observation of dislocations, including optical and electrical methods; the impact of dislocations on the performance of crystalline silicon solar cells, such as the combined effects of dislocation and other defects; and control of dislocation density as a part of dislocation engineering.


2. Observation of Dislocations

2.1. Optical Observation Methods

2.1.1. Chemical Etching Processes

The most commonly used method to directly observe dislocations is chemical etching, where hydrofluoric acid (HF) or a similar chemical is employed to dissolve SiO₂ on silicon and etch the

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 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aesr.202300240>.

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DOI: 10.1002/aesr.202300240

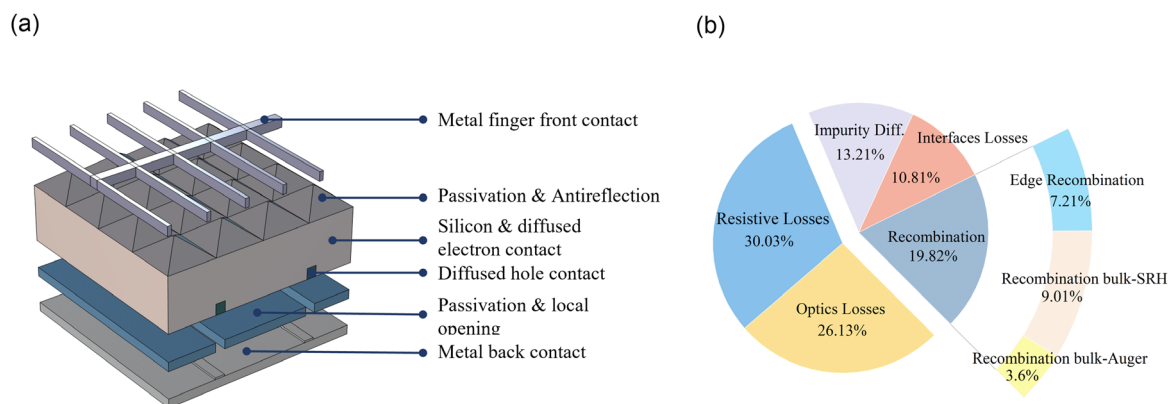


Figure 1. a) The typical structure of PERC solar cell and b) the efficiency loss pie chart contained in the device. It can be seen that recombination caused by defects (including edge recombination, doping defect recombination, and so on) accounts for about 45%.

Si surface. As most atoms near the defect sites deviate from the equilibrium position, the atomic diffusion rate is faster than the nondefect area. Hence, the rate of chemical reaction is faster than elsewhere and etch pits are formed around crystal defects.^[6]

The so-called dash-etching, containing HF and nitric acid (HNO₃), can reveal dislocations in different orientations, but it requires a long time to etch.^[7] Due to the strong corrosiveness of HNO₃, several etchants that utilize oxidants instead of HNO₃ have been developed, such as Sirti etchant (HF mixed with chromium oxide [CrO₃] in water), Wright etchant (CrO₃ and Cu(NO₃)₂·3H₂O in a mixture of water, HNO₃, HF, and acetic acid), and Secco etchant (K₂Cr₂O₇ in water mixed with HF).^[8–10] The Sirti etchant and Wright etchant form uneven etching pits depending on the surface or grain orientation.^[10] However, it cannot be ignored that all of these etchants contain metal oxides, which may leave the remaining metal ions to contaminate the sample and clean processing area.

It is reported that when a suitable etching agent is used, it can effectively form etch pits even after a long-term boron diffusion gettering to depinning the dislocations.^[11] When crystal defects are decorated by metallic defects, the defect etching process has a tendency to be accelerated, which may be caused by the reduction of the activation energy due to the decoration of metallic defects.

Etching pits are usually observed using an optical microscope or scanning electron microscopy.^[12] Figure 2 shows a clear image of potential-induced degradation-shunting (PID-s) induced by extended defects, such as stacking fault, which will be discussed in detail in the next section.^[13] As the size of etch pit has a limitation on spatial resolution, there is an upper limit to the observation of dislocation density. So, it is necessary to select a microscope with an appropriate resolution according to the actual situation.

2.1.2. Microscopic and Spectroscopic Analyses

There are a considerable number of microscopic analysis methods that can be used to observe defects, including dislocations, in silicon solar cells. Electron back-scattering diffraction (EBSD) analysis can be used to observe the defect topography and crystallographic properties of the sample surface.^[14] The relationship

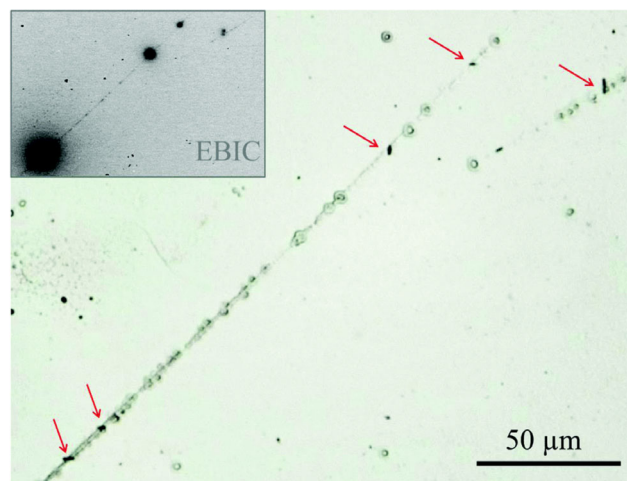


Figure 2. Optical microscopy of etch marks after delineation of PID-shunts by defect etching. The short black lines (marked by red arrows) are etch grooves. The long grayish lines, accompanied by ring-like marks, are slight scratches on the solar cell surface. The inset shows the electron beam-induced current (EBIC) image of the same PID-shunts. Reproduced with permission.^[13] Copyright 2016, Elsevier.

between dislocations and intergranular boundaries within polycrystalline silicon bulk has been systematically investigated by E. Schmid et al. using EBSD approach, and the energy and structure of the intergranular boundaries have been identified as key to further understanding the correlation between dislocations and grain boundaries (GBs).^[15] Transmission electron microscopy (TEM) can directly observe local dislocations, mainly using the diffraction effect of atoms on electron beams in crystals, by making the sample into a thin film that the electron beam can pass through.^[16,17] The diffraction beam is blocked using an optical grating; hence, the image brightness mainly depends on the intensity of the transmitted beam. When the electron beam passes through the dislocation distortion region, a large diffraction is generated and the corresponding transmission beam intensity is weaker than the base region. The dislocation line is, therefore, represented as a relatively black line and the orientation

distribution of the dislocations can be directly observed according to the arrangement of these lines. In addition, according to TEM analysis, it is possible to observe dislocation activities, such as the movement of dislocations and fixed kinks, and obtain different information, such as kink formation energy and mobility, which is associated with dislocation movement.^[18] The activity between dislocations and interaction between dislocations and defects, such as GBs, can also be analyzed and observed using in situ TEM and high-resolution TEM (HRTEM).^[19,20] X. L. Wu et al. used the HRTEM giving a scrutiny on the partial dislocation-mediated process in nanocrystal with nonequilibrium GBs and finding a large number of deformation twins and few stacking faults.^[20] In combination with selected-area electron diffraction, TEM allows the study of defects such as dislocations in the damaged layers induced by nanoindentation, nanogrinding, and nanoscratching in the silicon wafer.^[21–23] Combined with secondary ion mass spectrometry (SIMS), TEM can reveal the interactions between point defects in silicon and pre-existing extension defects through related changes in transient-enhanced diffusion of boron.^[24] Similar work has been published in recent years, in which the interaction of sodium ions with extended defects such as dislocations has been studied with the help of TEM and energy-dispersive spectrometer. Twenty years ago, Fall et al. have already used electron energy loss spectroscopy to detect information about dislocation-related electron energy levels near dislocation cores.^[25] Also, as early as 1999, Golan et al. have used atomic force microscopy (AFM) to detect information associated with the structure and deformation of silicon, including defects and dislocations, destroying the periodic structure of crystalline silicon.^[26]

Spectroscopic analyses, such as Raman, infrared, and X-Ray, can also directly observe dislocation activity by analyzing information such as peak position, peak width, and so on. T. W. Lin et al. applied infrared photoelasticity measurement to provide stress mapping in monocrystalline photovoltaic samples; residual stress and crystalline defects in silicon wafers could deteriorate solar cell reliability and performance.^[27] Hence, researchers used this method to show the residual stress mappings in monocrystalline silicon wafers and photoelastic images combined with dislocation-based numerical modeling and dislocation structures. The presence of defects also affects vibration of the crystal lattice, which is reflected in the infrared absorption spectrum of the crystal, thus some defect information could be revealed by corresponding changes of the infrared absorption spectrum. Raman scattering is sensitive to the local atomic environment and can obtain information through the vibration of atoms.^[28] The environment around a single atom renders a strong influence on its dynamics. In real crystals, the appearance of dislocations is often accompanied by the formation of other extended defects like GBs and other faults, which could have a great impact on the atomic environment. Hence, the existence of these defects alters the Raman spectrum. D. Ge et al. carried a study of HRTEM and Raman spectrum on the detailed structural information in nanoindentation and nanoscratch research.^[22] White-beam X-Ray can monitor nucleation growth and movement of dislocations in silicon at high temperatures.^[29] Danilewsky et al. have shown that microcracks in silicon wafers and surrounding grain fields exist as sources of dislocation loops. The combination of synchronous X-Ray imaging, micro-Fourier

mapping, and electrical characterization revealed the formation of movement of dislocations in monophotovoltaic silicon, showing that the dislocations are formed at or near sub-GBs and their movement is hindered by precipitation.^[30]

2.2. Response Behavior Monitoring of Photons and Electrons in Si

Apart from the optical observation methods, there are also methods to indirectly obtain dislocation information by monitoring the optical and electrical properties of silicon, which are influenced by the presence of dislocations, using photons and electrons. X-Ray diffraction (XRD) or neutron diffraction can be used to obtain average information on relatively large samples which is relative to the sample size in direct observations.^[31] Any change in crystal structure affects the average information obtained by XRD, especially dislocations, which are extended defects that disrupt the periodicity of the crystal on a larger scale. XRD analysis of monocrystalline and polycrystalline powders can obtain microscopic information, such as dislocation density, dislocation characteristics, and grain size.^[32] This method hypothesizes that the crystals with expansion defects can be composed of some smaller crystals, which are dislocated. Hence, XRD peaks of dislocated crystals with smaller crystalline peaks can be broadened, asymmetric, and shifted, revealing anisotropic broadening. Also, processing of XRD data, such as full width at half maxima analysis, peak shift, and anisotropic broadening, provides microstructural parameters, such as dislocation density (ρ) and arrangement of dislocations (M).^[32] Zribi Z. calculated the dislocation density by using XRD experiments and made a comparison with the EBSD calculated results which was quite different; thus, the scale difference and sensitivities of the methods could be explained.^[33] Arulanantham A.M.S. et al. also used XRD to calculate the dislocation density; in addition, the size of crystallites, texture coefficient, and strain of the thin film of solar cells could also be obtained.^[34] H. Wu et al. conducted a detailed study on the effect of thermal annealing on defects of metallurgical grade silicon; their XRD spectra data before and after annealing at different position of silicon ingots show a clear change in peak intensity, indicating the preferred growth orientation.^[35]

EBIC is a technique which uses a beam of electrons to locally generate electron-hole pairs in materials and detects the corresponding currents and defects acting as recombination sites show weaker EBIC signals. However, laser-beam-induced current (LBIC) is a technique to generate electron-hole pairs by light beam and characterize the geometry, minority carrier diffusion length, quantum efficiency, and reflectivity of solar cells. EBIC and LBIC with high spatial resolution can be used to study recombination characteristics of the extended defects, such as dislocations and stacking faults, in semiconductors.^[36,37] Trails, recombination properties, and moving velocity of dislocations were investigated using EBIC and LBIC. They conclude that the dislocation type is not a unique parameter that determines the recombination properties of defects and the dislocation bending in the near-surface could also affect other defects formation.^[37] In their other work, a comparative research of 2D defects in solar cells was demonstrated, which shows that the LBIC

contrast of 2D-extended defects in crystals with large diffusion length could be a few times higher than that in EBIC.^[38] Thus, LBIC can reveal GBs with a lower recombination velocity which means a clearer observation and further research of dislocations. A. Schieferdecker et al. used LBIC combined with other methods based on photon and electron response like photoluminescence (PL) and electroluminescence to improve production materials.^[39] With the aid of the LBIC mapping, researchers found that a high density of dislocations in the silicon reduces the short-circuit current in the bulk of the solar cells, which again shows the effect of dislocations on solar cells performance. The EBIC test image of monocrystalline silicon clearly shows the site of surface of PID-s, as shown in **Figure 3**. PID-s in crystalline silicon cells is generally caused by stacking faults.^[40]

Other methods based on the response of photon can also indicate related information of dislocations. After the material absorbs photons, the electrons rise to the conduction band and leave holes, the two reach quasiequilibrium after relaxation. Then, a PL spectrum of the intensity or energy distribution of light at different wavelengths is obtained through compound luminescence. It can be realized that the PL is closely related to the energy band structure; thus, extended defects like dislocations that alter the energy band structure of materials could be detected by PL mapping. Low-temperature high-resolution PL spectroscopy is quite sensitive to the presence of dislocations, and the presence of dislocations can be indirectly detected by measuring the recombination characteristics of the sample, taking the effect of dislocations on device performance, as discussed in the next section.^[41] A new PL technology with 3D visualization was developed by Yusuke Hayama et al.; by processing PL images, they obtained a 3D visualization of dislocation clusters in multicrystalline Si (mc-Si) ingots, which give a intuition of the

generation, propagation, and annihilation of these dislocation clusters and the relationship between the source region and crystal orientation.^[42]

Deep-level transient spectroscopy (DLTS) is considered to be suitable to identify these defects, such as metallic impurity precipitates and oxide precipitates, in Czochralski silicon (CZ-Si) or float-zone silicon (FZ-Si) and the electrical properties of dislocations decorated by impurities, i.e., Ni impurities.^[43–46] DLTS combined with EBIC can recognize the effect of electrostatic barrier near the charged dislocation in silicon on the ability to reconstruct the dislocation-related deep energy-level center distribution.^[47] DLTS combined with LBIC can also recognize the electroactive defects, such as vacancies generated from dislocation movement, in silicon and the recombination properties associated with dislocations under the influence of metallic impurities, such as Fe.^[48,49]

Hence, it can be seen that these measurement methods combined with multiple techniques may reveal the optical and electrical behavior of dislocations. Sarau et al. have used a technique that combines micro-Raman, EBIC, defect etching, and EBSD to study internal stress and successfully explained the effects of these defects on stress that could not be clearly revealed by a single technique.^[50] Harvey et al. have utilized a combination of dark lock-in thermography (DLIT), TEM, and EBIC to determine the location of stacking faults step-by-step from the site of PID-s (**Figure 4**), providing an alternative method for studying the microscopic mechanism of PID.^[51]

3. Influence of Dislocations on Electrical Performance and Stability of Si Solar Cells

Extended defects, such as dislocations and GBs, play an important role in the performance of crystalline silicon solar cells as centers of recombination and impurity accumulation. The efficiency of solar cells is subject to the influence of defects on minority carriers, rendering a negative effect and compromising the efficiency of solar cells.^[52,53] Also, the interactions between moving impurities and extended defects can seriously affect the recombination activities of the solar cells.^[52] The effect of dislocations on photovoltaic devices is primarily discussed in this section, and the effect of dislocations in conjunction with other extended defects, such as stacking faults, will be discussed at the end of the section.

The presence of extended defect, such as dislocations in crystalline Si, destroys the periodic structure of the crystals, creates hanging bonds, and induces deep energy-level defect states in the bandgap of Si.^[53–55] Defects, especially point defects, have the commonality that could bind and release electrons, which could form deep energy-level defects in the bandgap, while dislocation extended defects have a stronger ability to bind electrons. Also, the hydrogen atoms model could be used to calculate that they form a local state in the bandgap. Deep energy-level impurities can produce multiple ionization and form corresponding energy levels. Also, when the concentration of deep-level impurities is high enough, several dense energy levels are formed, i.e., the formation of energy bands induced by defects. Due to the advancement of the process, in general, fewer dislocations exist in silicon and their effect on electrical behavior is not as significant as the

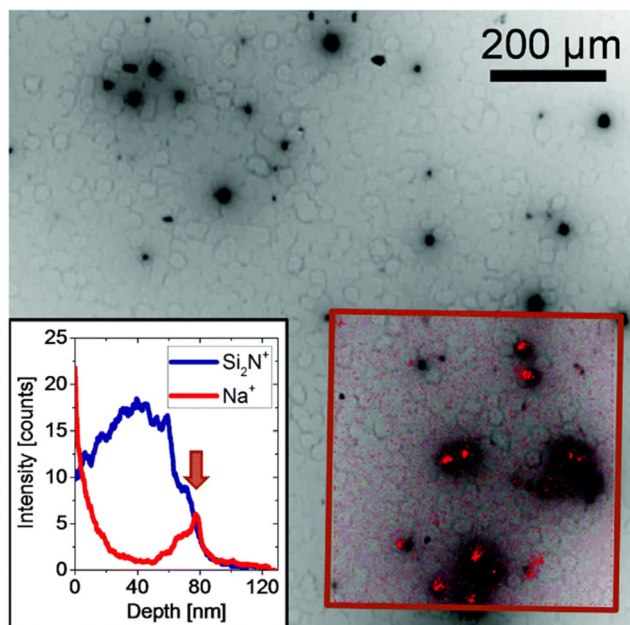


Figure 3. An EBIC image of a monocrystalline silicon cell region with a high density of PID-shunts acquired at an acceleration voltage of 30 kV. The inset shows the distribution of Na at the Si₂N₄/Si interface measured by the ToF-SIMS. Reproduced with permission.^[40] Copyright 2014, Elsevier.

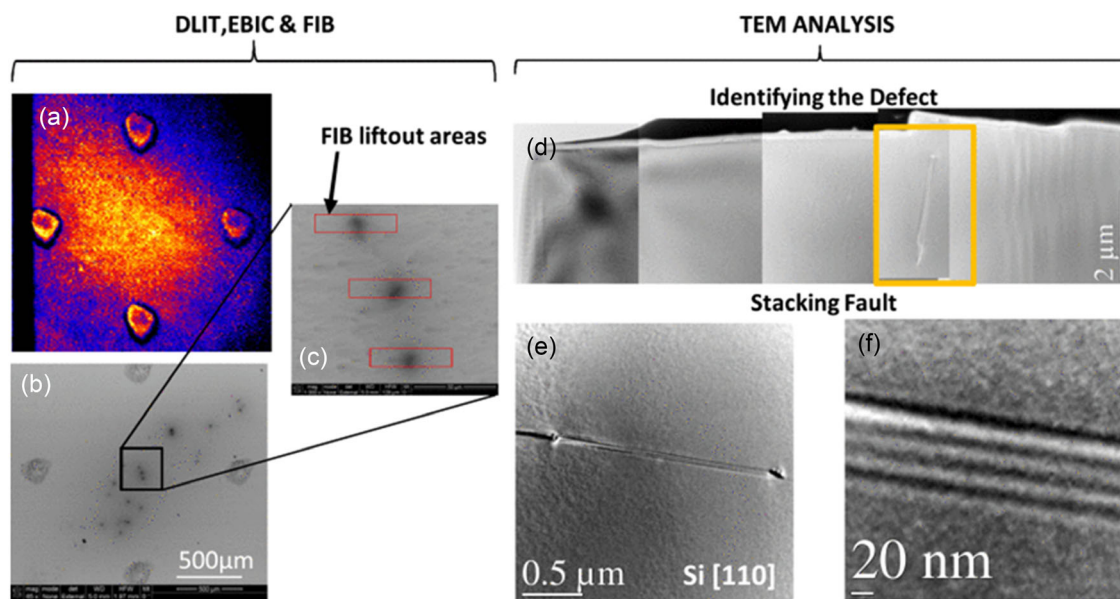


Figure 4. a) DLIT image of the shunted area; the laser marks for area marking are also visible. The marks are approximately 1 mm apart. b) EBIC image of the same area as shown in (a). c) Higher magnification EBIC scan of the three center dark spots in (b). The small rectangular boxes (red online) show the areas where FIB samples were removed for TEM analysis; the long edge of the rectangle is 50 μm . d) Low-resolution TEM image compilation of a FIB sample as shown in (c); a box is drawn around the subsurface structural defect which was identified. e) Higher magnification image of the defect identified in (d), which is now identified as a stacking fault. f) HRTEM image of the subsurface stacking fault defect, which presumably contributed to the PID-s identified from the DLIT image. Reproduced with permission.^[51] Copyright 2016, Elsevier.

shallow energy-level impurities. However, the effect of dislocations on carrier recombination is quite significant and dislocations act recombination centers. The energy levels formed by dislocations in the bandgap capture excess carriers (photogenerated electrons and holes) generated by the photovoltaic effect of the monocrystalline solar cells, leading to carriers recombination, greatly reducing the carrier lifetime and increasing the parameters related to recombination in the solar cells (J_{02} and n_2 in a two-diode model).^[56–58] Hence, it can be concluded that the lifetime of minority carriers decreases due to recombination with increasing dislocation density, which is consistent with Donolato's theory, stating that dislocation density only renders significant impact on carrier lifetime after reaching a certain level.^[59] Also, samples with different initial minority carrier lifetimes exhibit a similar attenuation trend.

Not only the density of dislocations affects the performance of the device, but the distribution of dislocations also affects the performance of solar cells to a certain extent. Sopori et al. utilized the network approach to describe the methodology for regulating defects in photovoltaic devices, showing that the generation of dark currents in photovoltaic devices depends on the density of local defects.^[60] When crystal defects, such as dislocations and defect clusters, accumulate in a certain place, they extend deep into the substrate due to the so-called filamentous effect that influences the band structure of the silicon substrate and generates additional shunt paths in the device to affect the performance parameters, such as voltage and current, of the monocrystalline solar cell.^[61] For polycrystalline silicon solar cells with several crystal defects, though the overall dislocation density may not be high, the presence of local areas with high dislocation density still exhibits a

relatively large impact on the short-circuit current (I_{sc}). Dislocations along different crystal directions also exhibit different effects on device performance and the minority carrier lifetime of germanium, which belongs to the fourth main group along with silicon and is higher than [110] crystal direction in the [211] crystal direction, exhibits a better tolerance to dislocation density.^[62]

The type of dislocations can also have an impact on the performance of the solar cells. Dislocations are divided into edge dislocations and screw dislocations. Edge dislocations appear inside crystals as extra atomic halfplanes, while screw dislocations appear on the surface of the crystals. This leads to the fact that edge dislocations generally affect the reduction and recombination of carrier lifetimes inside the crystals, while screw dislocations mainly affect the recombination activity of the surface. Interestingly, both types of dislocations deteriorate device performance but the opposite effect occurs when such dislocations meet to form a dislocation loop. The formation of dislocation loops hinders the movement of dislocations, and thermal annealing to reduce the density of dislocations also leads to the formation of dislocation loops.^[63] Overall, dislocation loops curb the deterioration of dislocations on device performance to a certain extent. Hydrophobic wafer bonding causes the formation of dislocation networks in the bonded interface, rendering a unique impact on the properties of crystalline silicon.^[64] The characterization of dislocation network shows that it can achieve long-distance transport of minority carriers and high conductivity in carrier-conducting layers, thereby improving device performance.^[64,65]

Not only dislocations render a malignant effect on the performance of crystalline silicon solar cells, but the presence of dislocations also causes additional deterioration to the performance

of photovoltaic devices under the modification or joint action of other defects. For commercial *p*-type crystalline silicon (*p*-type c-Si) solar modules, the long-term performance and stability are affected by the influence of so-called PID effect which induced by the high electric potential difference between front glass and solar cell in photovoltaics (PV) modules.^[66] The most common type of PID in *p*-type c-Si solar cells is PID-s, which obviously associates with the recombination parameters of solar cells, such as parallel resistance and dark saturation current.^[13,58,67] PV modules affected by severe PID-s could suffer 20% losses off their operation power over the course of 1 year.^[68] Studies have shown that sodium ions (Na^+) play a major role in the PID-s effect in the presence of 2D-extended defects stacking faults bounded by a modified Frank partial dislocation.^[68] A simple experiment with high voltage in a high humidity and high-temperature environmental stress could be performed to simulate the formation of PID-s and the role played by the associated extended defects, for the purpose of forming PID and accelerating this process.^[69] PID-s could be located by EBIC images followed by preparation of focused-ion-beam (FIB) cross-sectional sample for TEM as mentioned in the previous section. In **Figure 5**, Na atoms statistically distribute in the stacking faults. This distribution of Na atoms could induce an ohmic channel across the *n*-*p* junction and corresponding recombination energy levels, thereby the performance of solar cells will be deteriorated especially in the case of insufficient irradiation. W. Luo et al. give a PID mechanism-based c-Si.^[66] Na-ions accumulate in the silicon oxide layer between the anti-reflection (AR) layer, which is mainly composed of SiN_x and crystalline silicon substrate under the electrostatic action of the electric field in the AR layer due to the potential difference between module frames and cells. Na-ions penetrate deeper along the stacking faults in

the cell, which throughout the $\text{n}^+\text{-p}$ in the silicon substrate by diffusion is caused by the difference of concentration of Na-ion, as shown in Figure 5.^[40,68,70] Researchers found that the penetration of Na-ions promotes the growth of stacking faults, while the size of original stacking faults remains unchanged. In their subsequent work, good agreement between PID-s points and surface tiny scratch locations is revealed by the combination of EBIC, chemical etching, and optical microscope to locate the PID-s point and detect related signature.^[13] Therefore, based on their research, a hypothesis was proposed that sodium ions induce the formation of stacking faults in the presence of surface defects and dislocations. S. P. Harvey et al. investigated a significant accumulation of sodium at the surface of a polysilicon mini-module using combination methods of PL, time of flight secondary ion mass spectrometry (ToF-SIMS), and TEM, consistent with prior observation.^[51] In the presence of dislocations or surface scratches, the entry of sodium ions could lead to the formation of stacking dislocations. Faults could be named partial dislocations in a certain sense, and when the modulus of the dislocation is less than 1, the burgers vector of the dislocation sweeps across a plane to form a fault. Partial dislocations in real crystals are related to stacking faults. When the fault energy is low, a screw dislocation will be prone to form two partial dislocations (a dislocation that the burgers vector is not equal to an integer multiple of the lattice vector) and a sandwiched piece of stacking fault. Therefore, it is known that the probability of formation of faults in crystals is related to the fault energy, and the higher the fault energy, the lower the probability of formation. In sum, the participation of sodium ions in the presence of surface scratches or dislocations leads to the formation and growth of stacking faults. However, in real crystals, the stacking faults are formed together with partial dislocations under certain conditions, which seems to be an explanation of the source of stacking faults as well as the reason why PV modules are often affected by PID.

The combined effect of other metallic impurities and dislocations can also increase the impact on device performance. According to EBIC results, some metallic impurities that are segregated or precipitated in dislocations, such as iron, nickel, copper, and gold, determine the recombination activities of dislocations in monocrystalline silicon.^[46,71] Dislocations, combined with Fe atoms that diffused into the device, increase hole-electron recombination due to the diffusion of Fe atoms, forming deep impurity levels in the bandgap.^[49] However, different forms of impurities render different degrees of influence and precipitated Fe atoms exhibit a lesser impact on carrier lifetime degradation than interstitial Fe atoms in polycrystalline silicon.^[72] Ni atoms produce deep energy levels in dislocations; however, all nickel atoms are not collected by dislocations.^[46] Hence, a small portion of Ni atoms is redistributed along dislocations by the electric field, which is consistent with the combined action of Fe atoms with dislocations to facilitate recombination of charge carriers. Also, electron transport along no atoms appears to be related to deep energy levels.^[73] Copper-dislocation interactions, similar to other metallic impurities, cause dislocation peaks in DLTS to broaden or generate new energy levels.^[74] As a typical deep-level impurity, gold ionizes many times to form a deep energy level, which affects the electrical properties of Si.

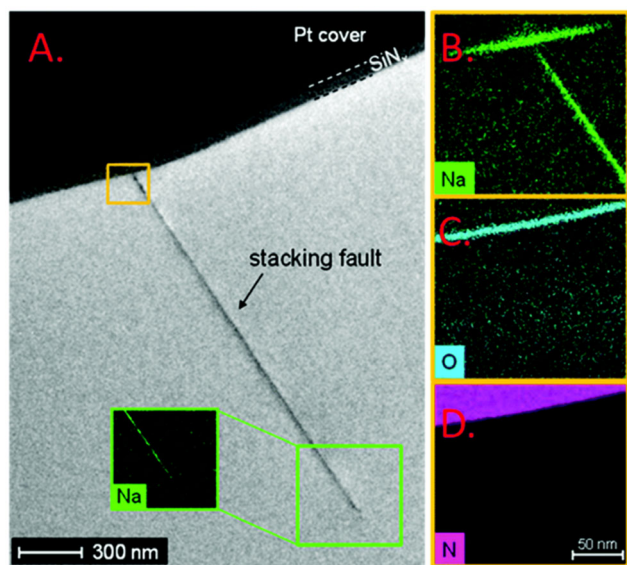


Figure 5. On the left is a brightfield TEM image of a stacking fault affected by PID. The small images on the right represent energy dispersive X-ray spectroscopy (EDX) mappings acquired in STEM mode at this stacking fault near the interface between Si and SiN_x . A Na-EDX map of the lower part of the stacking fault is shown in the inset on the left. Reproduced with permission.^[40] Copyright 2014, Elsevier.

4. Strategies to Reduce the Adverse Effects of Dislocation in Si Solar Cells

In the manufacturing of solar cells, two techniques are used to lessen internal defects and enhance cell efficiency. One is to reduce crystal defects by passivation layers, such as $\text{SiN}_x\text{:H}$ ^[75] or a-Si:H^[76] layers on the wafer surface, where H atoms in the passivation layers combine with hanging bonds on the wafer surface and internal defects, reducing the recombination ability of electrons and holes.^[75,76] The second is gettering treatments for wafers. During the processing of Si solar cells, precipitates may be dissolved or formed at different temperatures, depending on their solubility and diffusivity, and the gettering process can be used to remove transition metallic impurities by attracting them into a “sink” with higher solubility, such as *P*-diffused layer and liquid Al–Si layer coated on the polycrystalline silicon wafer surface.^[77,78] Though the introduction of H atoms can effectively improve the quality of wafers with high defect density, it may not be sufficient to eliminate the adverse effect of some types of oxygen precipitates at GBs and dislocations on the minority carrier lifetime. Naerland et al. have shown that the gettering treatment of phosphorus could effectively remove interstitial Fe atoms and increase minority carrier lifetime.^[79] Meanwhile, Choi et al. have indicated that the gettering treatment of P and Al at 820 °C could reduce the dislocation density of polysilicon wafers by 60% and 55% without influencing the minority carrier lifetime in polycrystalline silicon.^[78] However, a higher dislocation density may inhibit the gettering effect. Therefore, researchers are trying to explore ways called “dislocation engineering” to inhibit the generation and promote annihilation of existing dislocations during the growth process of silicon ingots.

4.1. Inhibiting Dislocation Generation during the Growth of Si Ingots

At present, the silicon used in silicon solar cells is either single-crystal, polycrystalline or amorphous. Amorphous silicon solar cells are composed of 10–20 nm amorphous silicon thin films deposited on a monocrystalline silicon substrate by the chemical vapor deposition method, where the internal defects are

passivated by H atoms.^[80] The process from metallurgical-grade silicon feedstock to solar-grade crystalline ingots is often referred to as the Siemens process, which is an expensive and energy-intensive part of the silicon PV chain. Moreover, there are two main techniques used to produce silicon ingots: the directional solidification (DS) method for polysilicon ingots and the CZ process for monocrystalline silicon ingots. The CZ process uses approximately 4 times more power than the DS technique.^[81] Figure 6 shows three different techniques for growing silicon ingots.

4.1.1. Monocrystalline Si Growth by the CZ Process

The mature process of growing monocrystalline silicon by the CZ method occupies the main market share. In this method, seed crystals are introduced into a crucible containing fused silicon in a single-crystal furnace for nonuniform nucleation and, then, the hot field is controlled to rotate seed crystals and slowly pull them upward. The monocrystalline Si grows under the seed crystals according to the crystal orientation of the seed crystals. The growth process includes seeding, necking, shouldering, equal-diameter growth, and crystal pulling completion.^[82] There are two main reasons for the introduction of dislocations during the growth of monocrystalline silicon ingots: dislocation heredity in seed crystals and stress introduction.^[83]

When seed crystals contain dislocations and dislocations outcrop on the growth surface, the dislocations will extend from the seed crystals to the newly grown crystals with the crystal growth until they intersect the crystal surface because dislocations cannot be interrupted in the crystal, which is called dislocation heredity. Dislocation heredity will only increase the length of dislocation lines but not the number of dislocation lines. The seed crystals provide the growth basis for monocrystalline silicon. When seed crystals get in contact with molten Si, sudden thermal shock produces a dislocation density of $10^3 \sim 10^4 \text{ cm}^{-2}$. The larger contact area and lower seed temperature are, more abundant dislocations are generated. Therefore, it is meaningless to use dislocation-free seed crystals. The dislocations in the seed crystals can be removed by combining them with necking and shrinking processes. The orientation of seed crystals renders a significant influence on the exclusion of dislocations. Si belongs

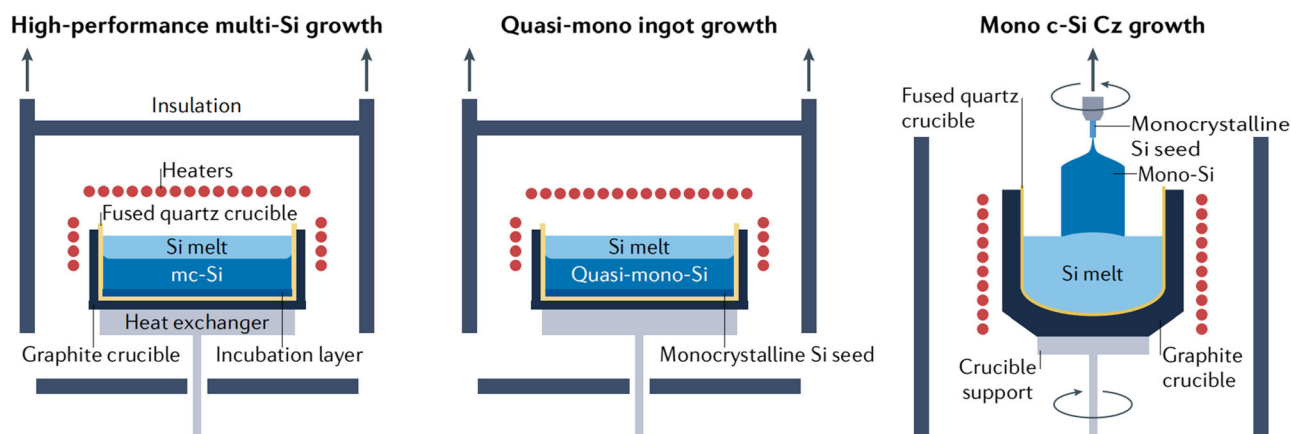


Figure 6. Different techniques for growing silicon ingot (left panel is the DS method of multi-Si, middle panel is the DS method of quasi-monocrystalline, right panel is the CZ method of monocrystalline). Reproduced with permission. Copyright 2022, Springer Nature.^[81]

to the diamond structure with a slip plane system of {111}. Hence, the dislocations are mostly on {111} planes. In order to easily discharge dislocations from the body, the minimum angle between the growth axis and {111} plane should be the maximum. The minimum angle between [100] and [111] crystal orientation and {111} plane is the largest, which is conducive to the removal of dislocations. **Table 1** presents the angle between {111} planes and the growth of crystal orientation.

The growth of monocrystalline Si without dislocations by the CZ method is mainly dependent on the necking-down technique. The thermal field and growth parameters are adjusted to make the solid-liquid interface relatively flat or Ω -shaped. In order to prevent the generation of thermal stress and dislocation increment, it is necessary to preheat the seed crystals, introduce crystal growth at high temperatures, and prevent a significant change in the diameter of the thin necks. As long as dislocations are eliminated during the shrinking necking and the thermal field of a single-crystal furnace is suitable, dislocation-free growth can be maintained even if the shoulder is placed flat. The method improves the utilization rate of monocrystalline Si ingot and the drawing rate. At present, the growth technology of monocrystalline Si by the CZ method is quite mature and it is generally not difficult to produce monocrystalline Si ingots without dislocations as long as the technical conditions are strictly mastered. In addition, high-purity monocrystalline Si can be prepared by FZ methods.^[84]

4.1.2. Growth of Polycrystalline Si by the DS

DS is a method of growing polycrystalline Si ingots by controlling temperature gradient and slowly solidifying molten Si along the direction opposite to the heat flow in a crucible. Each solidification requires a new crucible, which contains seed crystals at the bottom that promote crystal growth.^[85] Due to the thermal stress caused by the thermal field heterogeneity in the crucible, plastic deformation occurs during the growth of polysilicon, which leads to the generation and growth of dislocations. The local shear stress around GBs is considered to be dependent on the relative orientations to construct the GBs owing to the anisotropic elastic constants in Si. E. Schmid et al. found that {111} and {211} families of crystal plane participate in the plastic deformation and recovery process during growth, respectively, but the dislocation is mainly generated on the {211} slip plane, which may be caused by excessive shear stress on the slip plane.^[86] Dislocation slip and increment are always accompanied by deformation and stress release. The grain size increases gradually in the DS process of polysilicon ingots, which leads to the increase of stress between grains. The accumulation and release of stress lead to the rapid growth of dislocations in Si ingots.^[87] In addition, external stresses caused by crucible confinement can also result

in a high dislocation density at the bottom and peripheral parts of the ingot.^[88] The stress produces dislocations and, once dislocations are formed, a stress field is generated for each dislocation.

Most of the dislocations originate from the bottom of the ingot and affect the formation of subsequent dislocation clusters. Oriwol et al. have indicated that the bottom of the ingot generally determines the GBs characteristics of the entire ingot, whereas the dislocation density at the top is a result of the cumulative impact of GBs.^[89] Dislocations occur in grains, GB intersections, and GB lines, where the probability of occurrence is 2.7%, 5.6%, and 91.7%, respectively.^[89] Hence, a GB is an important source of dislocation formation. GBs with different orientations are related to the generation and annihilation of dislocations. Σ 3 GB has high symmetry and low GB energy in the initial solidification stage, which plays a dominant role in all types of GBs, and Σ 3 GB is easy to form large grains and reduce GBs, thus reducing the probability of dislocations.^[90,91] Random angle GBs are more likely to deposit impurities than Σ 3 GB, but the disordered structure of random GBs can release stress and reduce the generation and proliferation of dislocations.^[92] While there are various mechanisms for generating dislocations, including condensation of point defects, this means that dislocation density could be changed by controlling the GB structures formed at the initial stage of crystal growth.^[93] M.G. Tsoutsouva et al. and Y. Hayama et al. believe that sub-GBs and small-angle GBs with angular deviation with less than 10 degrees are likely to be the source of dislocation clusters.^[30,42]

In order to reduce the generation and proliferation of dislocations, it is necessary to pay attention to the solid-liquid interface, seed crystals, impurities, thermal field, and preparation technology during the solidification process of polysilicon ingots. Several important findings have been reported so far: 1) Dislocations often occur at GBs and spread with crystal growth; 2) Dislocations are introduced near the solid-liquid interface during crystal growth and initially generated dislocations serve as a source for more dislocations; 3) Dislocations often occur only in one grain at the GBs and generally do not penetrate multiple unit cells; and 4d) Rapidly solidified wafers process higher defect density than slowly solidified wafers.

The solid-liquid interface in the DS process is an excessive region of long-range order and disorder of Si atoms, and the evolution of internal atoms determines the separation of impurities and crystal growth. Therefore, the control of solid-liquid interface is the key to obtain high-quality crystals.^[94] Convex interfaces, which are convex toward the melt side, can push impurities to the peripheral region, and both convex and concave interfaces tend to produce twins in the crystals, increasing grain tilt and GBs. Moreover, dislocations are easily generated at the GBs, and the flat solidification interface can be obtained by adjusting the thermal field gradient and pulling rate. Then, columnar grains can be obtained that are highly parallel to the growth direction.^[95,96] Furthermore, grain size decreases with increasing solidification rate due to interface instability. In directionally solidified polysilicon ingots, unevenly distributed high-density slip dislocations exist and twins are generated at the GBs, which is caused by the polyhedral growth habit of Si melt at the front of the solid-liquid interface. Twinning usually originates from normal GBs. Dislocation and twins are highly correlated with the height of crystal characteristics and the size and density of

Table 1. The angle between {111} plane and the growth of crystal direction.

Crystal direction	<100>		<111>		<110>		<211>	
Number of {111} plane	4	1	3	4	2	1	1	2
Angle between {111} plane and the growth of crystal direction	55°44'	90°	19°28'	0°	35°16'	0°	70°32'	28°08'

dislocation clusters and twins vary with crystal height in polycrystalline Si ingots.^[97,98]

The bottom of a crucible used for DS contains seeds that affect the growth of crystals. These are made of little amounts of Si, SiC_x, SiN_x, SiO_x, and other high-temperature materials, usually only a few millimeters, called seed crystals.^[81] This kind of small-size seed is easier to avoid large grain nucleation than large-size seed crystals, ensuring uniform and dense Si melt, reducing horizontal stress, solidification from the seed surface, and reducing dislocation generation. This Si is referred to as high-performance polycrystalline (HP-multi) materials. Alternatively, Stoddard et al. have found that the utilization of monocrystalline seeds leads to a monocrystalline structure, i.e., quasi-mono or cast-mono materials, in major regions of ingots.^[99] Shilong Liu et al. produced low dislocation density cast-mono-crystalline silicon ingots using a new seed pavement method and the average efficiency of solar cells was increased from 20.63% to 21.81%.^[100] Ervik et al. have shown that there are three different dislocation formation mechanisms at seed crystals:^[101] 1) The scratch on the surface of seed crystals forms dislocation cores above 900 °C; 2) A sub-GB is formed at the seed grain interface, forming a highly asymmetric distorted region, which is prone to dislocations; 3) At the junction of seed crystals and Si, plastic deformation occurs due to the sintering of some contact points and dislocation structure changes. Dislocation forms symmetrically around these points and grows into dislocation clusters on the contact surface.

Dislocations require a certain amount of energy during their movement to overcome the obstacles encountered, which is called activation energy. Therefore, intentional doping in the DS process of polysilicon ingots can not only produce high-quality p(n)-type semiconductors, but also effectively inhibit dislocation generation. Boron is common in polysilicon doping due to its segregation coefficient of close to 1. However, due to its small atomic radius, boron is easy to form point defects of the boron-oxygen complex with oxygen, which affects minority carrier lifetime.^[102] Gallium doping can effectively inhibit light-induced degradation, but dislocations proliferate rapidly with the increase of ingot height.^[103] Germanium can effectively pin dislocations in Si and improve its mechanical strength.^[104] According to some certain atomic-scale calculations, when a dislocation encounters a vacancy or self-interstitial atom in Si, its slip velocity decreases slightly, allowing dislocations to climb up and down, which leads to pairwise annihilation of dislocations in opposite directions and reduces dislocation density.^[105]

Some researchers have tried to reduce dislocation density during the growth of polysilicon ingot by altering process conditions. When molten Si crystallizes, its crystal volume expands by about 10%. Extrusion from the crucible introduces shear stress into the sliding plane of the crystal, resulting in dislocations. The solid-liquid interface is the key to obtain high-quality crystals. By adjusting process parameters, the solid-liquid interface is controlled as a plane state and polycrystalline Si ingots containing well-oriented columnar grains parallel to the growth direction are obtained. Some researchers have utilized dendritic growth at the beginning of crystal growth to control grain size and orientation to obtain high-quality polysilicon.^[94] Moreover, thermal stress inside the crystal can be reduced by the doping effect and impurities with lower activation energy can accelerate the paired annihilation of dislocations. Some electroactive impurities can

control the Fermi level to induce the saturation of hole-like defects and inhibit the formation of dislocations.^[106] Polycrystalline Si ingots with quasi-monocrystalline properties can be obtained using single-crystal seeds. A quasi-monocrystalline silicon ingot grown by DS methods was sliced and fabricated into solar cells, and it was found that the dislocation density increased significantly and the cell performance decreased rapidly as the wafers approached the top of the ingot.^[100] PL images of as-cut wafers and solar cells from the bottom to the top of one brick show that the dislocation and other defect densities increase rapidly with the direction of ingot growth. At the same time, the efficiency of the fabricated solar cells decreases with the rapid decrease in the ingot growth direction, and the difference in cell efficiency between the top and bottom wafers is close to 2%.^[100] The dislocation density of the polycrystalline Si ingots grown by DS can be reduced by thermal annealing; however, the minority carrier lifetime and resistivity of the ingot decrease with the increase of annealing temperature, which is unfavorable to the preparation of solar cells.^[107] Hence, some low-temperature annealing processes combined with gettering treatments can improve the electrical properties of Si materials while reducing dislocation density.^[78]

4.2. Reducing Dislocation Density and Improving Performance after Si Ingot Growth

From Si ingots to Si wafers that can be used in solar cells, cutting, thinning, and mechanical polishing are required. The initial method is proposed in the 1980s, to cut through Si using a slurry of Si carbide particles in a glycol solution.^[108] Significant kerf losses, i.e., wire diameter plus 2 times the diameter of SiC_x particles, up to 120~200 μm, were experienced during this procedure. Diamond wire (steel wire with diamond particles), which was introduced from 2015 to 2019, reduced kerf losses to 50~70 μm and greatly lowered wafer prices in recent years.^[109] The wafer surface shows traces of diamond wire cutting and requires further mechanical polishing before being used in solar cells. Also, huge external stresses are introduced during the given step, which can create new dislocations and other defects inside the wafer. Therefore, it is necessary to study appropriate technology to minimize irreversible damage to wafers. At the same time, the processed wafer can also be used to reduce dislocations and other defects inside the wafer through thermal annealing, doping, and other technologies.

4.2.1. Methods and Physical Mechanisms to Reduce Wafer Dislocations

Researchers have conducted numerous modeling and simulation investigations on the movement of dislocations inside wafers. In addition, some researchers have studied the influence of stress and temperature on the motion rate of dislocation inside wafers through simulation experiments, and demonstrated that dislocation mobility increased with the increase of temperature and stress, which is compatible with Peierls-Nabarro model prediction.^[110] However, another atomic simulation study has shown that dislocation mobility decreases with increasing temperature, which is due to interactions between dislocations and thermal

phonons. When applied stress exceeds the Pells stress, which decreases with increasing temperature, dislocations start to move. Li et al. have shown that, at relatively low temperatures (around $T < 227$ K), the dislocation velocity monotonically increases with increasing stress but velocity is not particularly sensitive to temperature variations.^[110] However, the velocity is extremely sensitive to temperature at high temperatures (around $T > 227$ K), and it no longer increases monotonically with an increase in tension.

The general theory for reducing the density of dislocations inside a wafer is that there is a driving force that causes dislocations to spread outward or annihilate in pairs by thermal annealing. Moreover, high temperatures allow dislocation movement to be unconstrained by the sliding plane of crystals and only annealing temperatures above 1000 °C are required to achieve this effect in polycrystalline Si.^[105] However, the lifetime of minority carriers in polycrystalline Si wafers suddenly decreases after high-temperature treatment, which may be due to the presence of a high concentration of metallic impurities precipitated during annealing.^[107] Gettering treatments with P and Al at low temperatures can improve the electrical properties of polycrystalline Si wafers while reducing dislocation density.^[78] In general, the movement of dislocations within wafers needs to overcome a certain amount of activation energy; hence, high temperature and appropriate external stress can increase the dislocation migration rate and reduce dislocation density. **Figure 7** presents the relationship between the physical mechanism for reducing dislocation density and process technology.

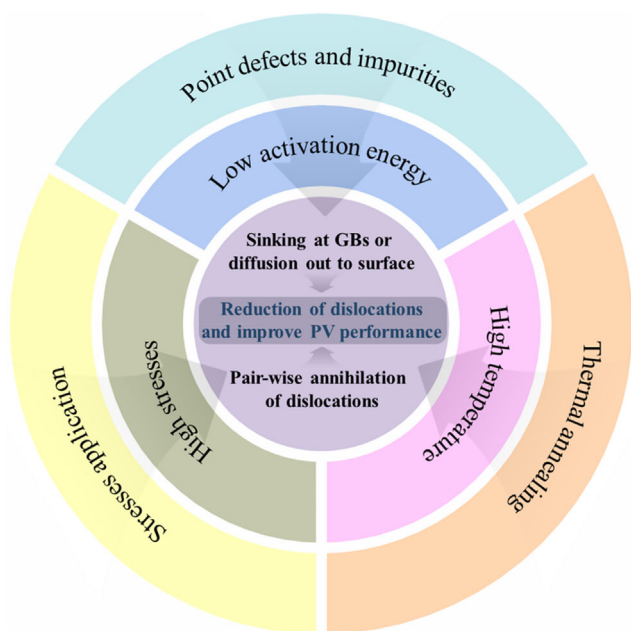


Figure 7. A pie chart for dislocation density reduction process. The outermost layer of this pie chart is the techniques to reduce the dislocation density, the second layer is the driving forces corresponding to a certain technology, the innermost layer is the physical mechanism of dislocation reduction, and the innermost rectangle is the purpose of dislocation engineering.

4.2.2. Damage to Si Wafers and Slip Annihilation of Dislocations Caused by External Stress

From the Si ingots grown to the wafers which can be used to fabricate solar cells, excessive machining is required. The breaking of Si wafer and cracking of Si ingot directly lead to the waste of material cost. So, the diamond line slicing process determines the production cost of the entire Si solar cell industry. In the last few decades, the simulation of diamond wire-cutting Si ingot and the deformation mechanism of Si wafers under various mechanical loads have been investigated extensively.

Due to the brittleness of Si, microcrack damage is easily left on the surface of diamond cutting. Microcrack damage of Si wafers has been investigated extensively. Suzuki et al. have utilized diamond wire sawing to cut monocrystalline Si and found that using smaller diamond abrasions and increasing sawing period could significantly reduce the depth of microindentation on the surface.^[111] As observed by cross-sectional TEM images, the surface damage layer is generally composed of an amorphous layer, a dislocation layer with GBs, and microcracks.^[23] By establishing a model of the stress field in brittle materials with a single wear particle, the nucleation location and propagation direction of radial and intermediate cracks are predicted, and the model is in good agreement with the experiment.^[112] Gupta et al. have conducted slicing experiments on single-crystal alumina using an electroplated diamond-wire saw, and the results indicated that the surface roughness and subsurface damage degree of the slicing surface decreased with the decrease of diamond abrasive size, an increase of linear velocity, and an increase of abrasive distribution uniformity.^[113] Moreover, the depth of subsurface crack became deeper with the increase of wear degree of diamond-saw wire.

The penetration of diamond particles into materials is assumed to be the nanoindentation process. Researchers have looked at the impact of external stress, loading rate, and needle shape on the development of subsurface microstructure using nanoindentation technology. Wu et al. have shown that, when the hydrostatic pressure exceeds the threshold value, the Si-I phase of the diamond structure would be transformed into the Si-II phase of the isomorphic structure with metallic β -Sn during the loading process under nanoindentation.^[23] Moreover, the Si-II phase could be transformed into an amorphous Si phase or high-pressure Si phases such as Si-XII and Si-III phases during the unloading process. Si-XII phase is a rhombohedral structure, while Si-III phase is a body-centered cubic structure. **Figure 8b,c** and **d** shows micro-Raman spectra obtained from several nanoscratch site, as marked in **Figure 8a**. In contrast to the only normal load used in nanoindentation, nanoscratches involve both lateral and normal forces during deformation.^[114] Therefore, conducting systematic investigations of the deformation of monocrystalline Si wafers caused by nanoscratches may be beneficial to increase the productivity of the machining process. The typical cross-sectional TEM images of the nanoscratches made by the 3 μ m conical tip under 1, 2, and 6 mN are shown in **Figure 9**. As shown in **Figure 9**, all TEM specimens show an amorphous Si area and a damaged crystalline region, which is damaged by nanoscratches. Huang et al. have shown that the phase transition (mainly amorphous) occurs with the

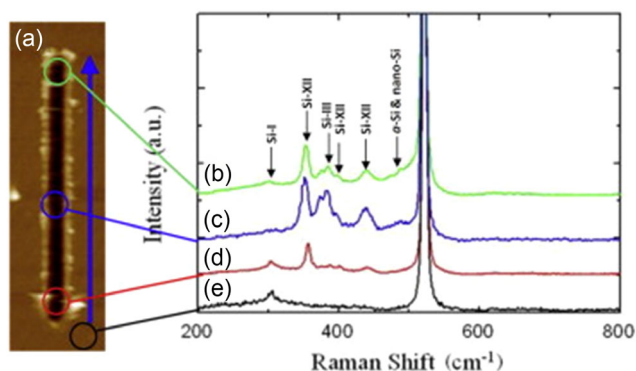


Figure 8. a) AFM image of a scratch made with a load of 6 mN; b–d) micro-Raman spectra acquired from different locations of the nano-scratch as marked in (a); e) micro-Raman spectra acquired from the Si substrate. Reproduced with permission.^[23] Copyright 2010, Elsevier.

increase of normal loading of nanoscratches.^[115] At the boundary between the phase transition zone and protocrystalline Si, partial dislocation emission takes place when the scratch load surpasses the threshold value, forming stacking defects. Dislocations elongation and density are mostly dependent on applied stress and indenter shape, but they are completely independent of scratch velocity. Therefore, amorphous and dislocation nucleation are two main physical behaviors during nanoscratches processes. Additionally, the amorphous process occurs slightly before or concurrently with the formation of twin structures or stacking faults. According to thorough molecular dynamics studies of the nanoindentation of monocrystalline Si, the inelastic deformation of monocrystalline Si is entirely caused by the amorphous

phase transition and the commencement of this inelastic deformation can be accurately anticipated by the stress. In addition, a nondamaging and chemical-free Si polishing technique was developed based on the stress-controlled phase transition mechanism.

The wire-cutting Si wafer also needs to be further mechanically polished or thinned, in which nanogrinding technology can be used to remove impurities from the Si wafer. However, this may lead to microstructural changes in the wafer subsurface, thereby introducing residual stress in the processed wafer, which prevents further wafer thinning and polishing. Based on the simulation and experimental results of nanoscratches, it can be inferred that the final surface structure of the monocrystalline Si wafer is affected by the accumulated stress of repeated scratches during the nanogrinding processes.^[115] Repeated scratches lead to an increase in the temperature of Si substrate, thereby changing the conditions of Si amorphous and dislocation nucleation. In addition, during nanogrinding processes, amorphous Si produced by large diamond grains can be removed by small diamond grains, reducing the depth of amorphous Si layer.

Samuels et al. have indicated that the shear stress could move dislocations within some crystal slip planes over the temperature of brittle-to-ductile transition, i.e., 530–660 °C, which is determined by the dopant concentration and strain rate.^[116] Additionally, in contrast to tension, which is a vacancy-opening mode, compression is a form of vacancy-closing mode. As a result, atoms might migrate to compression regions, while vacancies might diffuse to tension regions. Hence, dislocations might be easily annihilated through annealing under a small magnitude of compressive stress. Therefore, sufficient stress can enhance the slip of dislocations, causing dislocations to spread outward from the outer surface or annihilate in pairs.

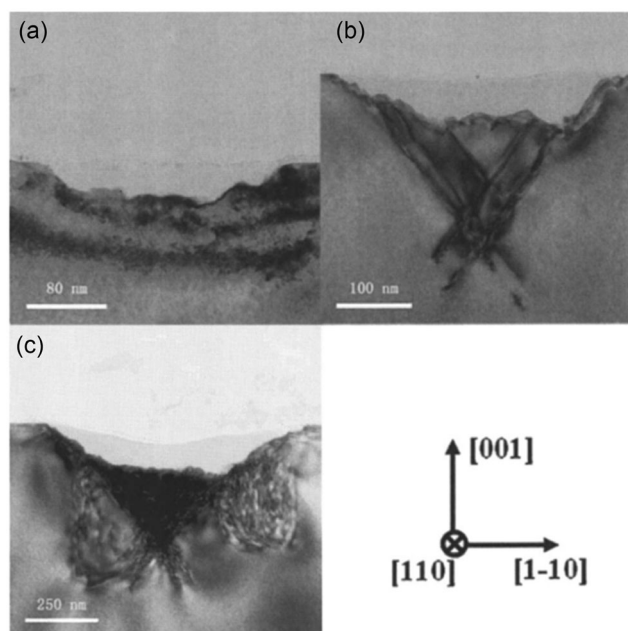


Figure 9. TEM images of nanoscratches made using the 3 μm conical tip at different loads of a) 1 mN, b) 2 mN, and c) 6 mN. Reproduced with permission.^[115] Copyright 2009, American Vacuum Society.

4.2.3. Effect of Thermal Annealing on Dislocations

Gumbsch et al. have shown that GBs and dislocations in monocrystalline Si wafers could migrate within a certain crystal slip plane at around 600 °C.^[117] However, Takeuchi et al. have discovered that dislocations could be eliminated from Si wafers at $T > 1000$ °C by external diffusion to the surface or pair annihilation without being constrained by slip planes.^[118] Wu et al. have discovered that small-angle GBs gradually decreased and disappeared with increasing annealing temperature in polycrystalline Si wafers.^[35] Subcrystalline and small grains were swallowed by subcrystalline merger or phagocytosis mechanism, increasing the grain size due to recrystallization and grain growth of polycrystalline Si at high temperatures. As shown in Figure 10, the dislocation density in upgraded metallurgical grade silicon (UMG-Si) marginally reduces during annealing. Also, dislocation density varies with the height of Si ingot being lowest in the middle and highest at the top both before and after annealing.^[97] At the same time, Wu et al. also indicated that the optimal growth orientations were obtained for grains at each height position of polysilicon ingots, which were $\langle 533 \rangle$, $\langle 111 \rangle$, and $\langle 533 \rangle$.^[35] The optimal growth orientation improves the mechanical properties of polysilicon by better matching its strength, plasticity, and ductility.

The dislocation density, minority carrier lifetime, and resistivity of the polysilicon wafer with high-impurity concentration are

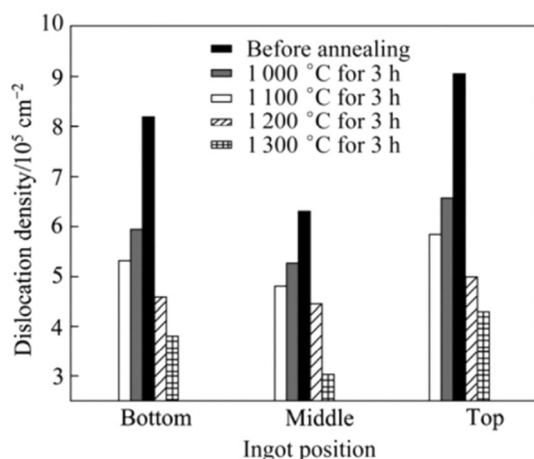


Figure 10. Dislocation density of UMG-Si before and after annealing. Reproduced with permission.^[35] Copyright 2011, Elsevier.

found to decrease with the increase of temperature after annealing at 1000–1400 °C. As shown in **Figure 11**, Buonassisi et al. have discovered that the minority carrier diffusion length of the rapid thermal processing (RTP) sample at low temperatures (860 °C and 120 s) is 20% more effective than the RTP sample at high temperatures (1000 °C and 20 s).^[119] Consequently, the electrical characteristics of Si are not primarily constrained by dislocation density. Buonassisi et al. have indicated that the structure, chemical status, and spatial distribution of high concentrations of metallic impurities affect minority carriers recombination in polysilicon materials.^[119] Therefore, appropriate annealing temperature can transfer the structure or chemical state of harmful impurities in Si, where the minority recombination ability is weakened. For example, Pickett et al. have shown that interstitial Fe atoms in Si were precipitated by annealing at 400–500 °C, thereby improving the electrical properties of polysilicon wafers.^[120] At the same time, the ability of minority carriers to recombine, which is almost independent of the total impurity concentration, can be greatly altered by even slight changes in the structure or chemical state of the metallic impurities. **Figure 12** (Buonassisi et al.) indicates that high-temperature RTP significantly lowers the average metallic content of FeSi₂ precipitates by 50%; however, some large FeSi₂ precipitates still

persist after low-temperature RTP. As demonstrated in X-ray beam induced current images and **Figure 11**, the recombination activity of intragranular regions increases with decreasing Fe content at structural flaws, indicating that neighboring areas are contaminated by dissolved Fe. Therefore, the concentration of metallic impurities in the same polysilicon wafer long- and short-lifetime areas is not significantly different from one another.

Bertoni et al. have indicated that the precipitation of impurities during high-temperature processes could cause significant pollution of polysilicon wafers.^[107] As a result, the electrical characteristics of wafers are negatively impacted, negating the benefits of the dislocation density reduction. However, Takeuchi et al. have found that the dislocations could not readily move at temperatures below 1000 °C because dislocation slip was inhibited by restricted vacancy migration.^[118] Hence, researchers have tried annealing dislocations at a low temperature of 820 °C with additional driving forces to stimulate dislocation movement, called gettering treatment. After P gettering at 820 °C, it is observed that the dislocation density of polycrystalline Si with an intermediate concentration of metallic impurities decreased by more than 60% and the dislocation size also decreased significantly.^[78] Choi et al. have explained that the net unidirectional impurity flux might drive dislocations to “sink” sites, resulting in a drop in overall dislocation density. Additionally, it has been found that the amount of drop in dislocation density diminishes with increasing gettering temperature. This may be because the higher annealing temperature creates a reduced driving force for impurity segregation. It is also observed that the magnitude of dislocation density reduction decreases with increasing gettering temperature, which may be due to the weaker driving force of impurity segregation at high annealing temperatures. Moreover, this phenomenon is not significantly observed in high-purity polysilicon wafers. In summary, the improvement in the electrical performance of Si wafers induced by gettering treatments at low temperatures depends on the simultaneous reduction of impurity concentration and dislocation density. Meanwhile, Song et al. demonstrated that postfiring hydrogenation step could further enhance the passivation of dislocation clusters in the *p*-type cast-mono-like silicon solar cells. The above result indicates that dislocation passivation by hydrogen needs a relatively long treatment time at low temperature compared with fast-firing process.^[121]

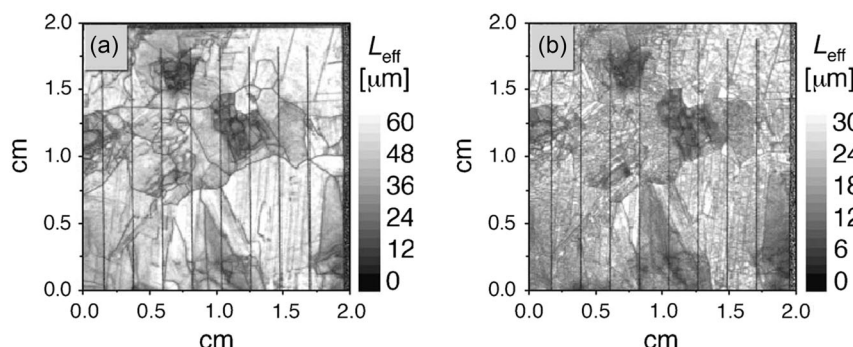


Figure 11. LBIC maps of minority carrier diffusion length in a) a low-temperature RTP (860 °C and 120 s) solar cell and b) a high-temperature (1000 °C and 20 s) RTP cell.^[119] Reproduced with permission. Copyright 2005, AIP Publishing.

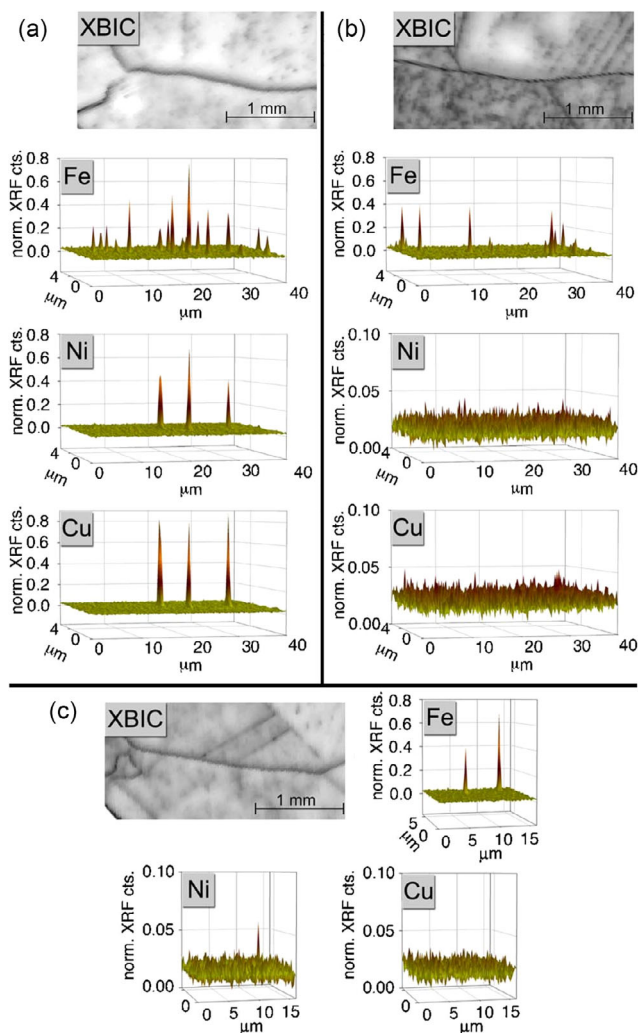


Figure 12. (Color online) Synchrotron-based analysis of the metal content and distribution at GBs in three sister wafers: a) unprocessed material (as grown), b) high-temperature RTP (1000 °C and 20 s), and c) low-temperature RTP (860 °C and 120 s)^[103]. Reproduced with permission.^[119] Copyright 2005, AIP Publishing.

4.2.4. Effect of Point Defects and Impurities on Dislocations

The dislocations need to be given a certain amount of energy to overcome obstacles during movement. The activation energy of dislocation movement may be affected by point defects that are present inside the wafer, such as vacancies, self-interstitial defects, and other impurities. Some of these defects are beneficial, but most of them hinder dislocation movement. Atomic-scale simulation studies show that the slip rate decreases when dislocations in Si wafers encounter vacancies or self-interstitial clusters, resulting in dislocations climbing up or down.^[122] This promotes pair annihilation of dislocations in opposite directions, reducing dislocation density in the wafer. Abe et al. have shown a correlation between the temperature and growth rate of Si ingot and the number of vacancies and self-clearance impurities in monocrystalline Si.^[123] The formed crystals still possess

vacancies with a minor temperature gradient at the solid–liquid interface. Moreover, self-interstitial atoms in Si produce frank dislocation rings under a substantial thermal gradient. **Table 2** summarizes the relationship between different types of defects and dislocation behaviors.

Nakai et al. have found that self-interstitial atoms clump together during crystal formation to produce stacking defects and dislocations are thought to be generated by the edges of stacking defects.^[124] Based on the size and density of faults, it is estimated that the total concentration of self-interstitial atoms that resulted in the stacking faults was roughly 10^{13} cm^{-3} . Research shows that stacking faults provide a powerful barrier to crystal dislocation movement and sub-GB formation in polysilicon.^[125] It appears that dislocations are produced by stepped and curved stacking fault edges. Theoretical studies have shown that defects and impurity formation energy at accumulated stacking faults are lower than inherent defects in crystals. The segregation of impurities at stacking faults can affect the mechanism of dislocation movement, thereby influencing the plasticity of crystals. Therefore, stacking faults are crucial for plasticity and the formation of dislocation microstructure in polysilicon. Ravi et al. have reported that dislocations were generated by stacking faults when boron oxide-modified CZ-Si was annealed at 900 °C.^[126] The mechanism for dislocation generation is the nucleation of precipitation at stacking faults and the recurrence growth generated by climbing forces after the stacking fault grows and continues to precipitate. These findings imply that

Table 2. Studies of relationships between different defects and dislocation physics behaviors.

Type of defects	Authors	Materials	Results
Stacking faults	Nakai et al. ^[124] Kivambe et al. ^[125]	CZ-Si mc-Si	Stacking faults are formed by the agglomeration of self-interstitial atoms during crystal growth Stacking faults provide a powerful barrier to crystal dislocation movement and sub-GB formation. Meanwhile, stepped and curved stacking fault edges appear to generate dislocations
H elements	Martsinovich et al. ^[127] Ogawa et al. ^[128]	N/A n-CZ-Si	H atoms can effectively reduce the activation energy of dislocation slip (from 2.2 eV to 1.2 eV) Hydrogen could enhance the motion of dislocation
O elements	Zeng et al. ^[132]	CZ-Si	The pinning effect of oxygen precipitates was shown to depend on its density and size at high temperatures
N elements	Alpass et al. ^[140]	NFZ-Si	The locking strength of the dislocation of nitrogen is different from that of oxygen in silicon. The locking strength at 550 °C depends on the temperature of the previous annealing, peaking at 600–700 °C and approaching zero at 1000 °C
Impurities	Choi et al. ^[178]	mc-Si	Under the additional driving force provided by P or Al gettering layer, impurities such as Cu, Ni, and Fe are reduced, and dislocation density is reduced by about 60%

stacking fault growth involves partial dislocation climbing caused by defect precipitation and it may be connected to dislocation formation.

Hydrogen, oxygen, and nitrogen are common nonmetallic impurities in Si and some studies have shown that these impurities could significantly affect dislocation movement. First-principles calculations and elastic theory studies show that the lowest energy structure for H to accumulate in Si is the hydrogenated slip dislocation ring.^[127] So, it can be concluded that dislocations are passivated by H atoms. Song et al. demonstrated that the open-circuit voltage and short-circuit current density of the cast-monocrystalline silicon solar cell were increased, leading to an absolute efficiency enhancement of 0.6% after laser-enhanced hydrogen passivation.^[121] With an increase in H concentration, point defects become less likely to occur and H atoms can significantly lower the activation energy of dislocation slide (from 2.2–1.2 eV), improving the slip speed of dislocations. Some room-temperature experiments show that hydrogen is adsorbed to dislocations and diffuses along dislocations, changing the electronic state near dislocations. Ogawa et al. have discovered that hydrogen atoms improve the passivation property of CZ-Si even at room temperature.^[128] So, hydrogen supplied from surface or ambient water can likely improve dislocation movement. At high temperatures, hydrogen can also enhance the slip of dislocations, as hydrogen can also be easily transferred into Si or even just boiling water, rendering a substantial impact on the electrical characteristics of the device.^[128,129] At the same time, hydrogen adsorption and desorption render a significant effect on electronic characteristics of dislocations, and dopants that induce different Fermi levels in relation to the level of dislocations can also change the mobility of dislocations.^[130] Therefore, changes in the electronic properties of the material will also be directly related to the changes in mechanical properties. The loading and unloading curves of CZ single-crystal Si wafers are separated by indentation test after boiling water treatment. This phenomenon is the direct evidence of plastic deformation of CZ-Si wafers, indicating that H enhances the movement of dislocations.^[128] In addition, in hydrogen-rich environments, dislocations in Si may be more mobile at room temperature.

Oxygen is an unavoidable impurity in Si materials, which is mainly caused by oxidation in air and dissolution of oxygen atoms in the crucible during growth. The results of the first experiment in 1975 on the interaction between oxygen and dislocations in CZ-Si show that interstitial O atoms and silicon dioxide do not render any pinning effect on dislocations.^[131] Subsequent studies using various electron microscopy techniques have shown that the oxygen element or more precisely oxygen precipitates could effectively inhibit the movement of dislocations in Si. Zeng et al. have shown that oxygen precipitates might immobilize dislocations produced at high temperatures in CZ-Si.^[132] It has also been demonstrated that the size and density of oxygen precipitates affect the pinning effect of dislocations. Greater pinning of dislocation is seen for larger oxygen precipitates, and the higher the oxygen precipitate density is, the deeper this relationship is. On the other hand, Jurkschat et al. have discovered that oxygen precipitates, with low densities of $10^8 \sim 10^{10} \text{ cm}^{-3}$, did not influence dislocation movement, while the precipitates with a size of $> 200 \text{ nm}$ acted as new dislocation sources.^[133] In addition, it has also been demonstrated that

injecting a high density of tiny oxygen precipitates could improve the mechanical characteristics of Si by reducing the bending of Si wafers caused by dislocation slip. Senkader et al. have indicated that the amount of stress necessary to unlocking the pinning of dislocation depends on the number of oxygen atoms in the dislocation nucleus.^[134] Also, the stress necessary to unlock a dislocation at a specific annealing temperature exhibits three different states over time in CZ-Si. The unlocking stress rises linearly with annealing time before reaching the saturation level, where the saturation status is a function of temperature and oxygen concentration. The unlocking stress starts to climb with increasing annealing time, which is connected to the precipitation of oxygen at dislocations. Based on Zeng et al.'s study, small second-phase particles dispersed throughout a ductile matrix have been shown to reduce dislocation movement and boost the material's strength.^[132] The second-phase particles in CZ-Si can be regarded as oxygen precipitates. At the same time, oxygen precipitates also contribute significantly to the accumulation of hazardous metallic contaminations. However, Nitecki et al. and Hirano et al. have discovered to occasionally cause punched-out dislocations that are harmful to the mechanical strength of CZ-Si wafers.^[135,136] Moreover, if oxygen precipitates enter into the active region, it will raise the leakage current of device. Zeng et al. have shown stress field interactions between precipitates and dislocations—which are more effective for platelet oxygen precipitates and perhaps less effective for polyhedral oxygen precipitates—frequently and effectively causing dislocation locking in CZ-Si.^[137]

Similar to oxygen, nitrogen also renders a complex influence on the mechanical characteristics of Si. Jastrzebski et al. have demonstrated that nitrogen might improve FZ-Si wafer performance only in specific conditions and at concentrations that are close to the solubility limit.^[138] This phenomenon is reflected in the increased mechanical strength of nitrogen-doped Si wafers in the float zone. Giannattasio et al. have indicated that the oxygen content of FZ-Si is frequently below the detection threshold and appreciable dislocation locking could not be detected in high-purity FZ-Si crystals at any annealing temperature or duration.^[139] It is possible to increase the mechanical strength of FZ-Si wafers by doping nitrogen and other chemical substances into FZ-Si crystals. After annealing, N impurities render a severe locking effect on fixed dislocations. This locking amplitude is comparable to O atoms during the CZ process despite N concentration in FZ-Si (about 10^{15} cm^{-3}) being two orders of magnitude lower than the typical concentration of O atoms in CZ-Si. With longer annealing times, the unlocking stress initially rises. It is important to note that the locking strength of dislocations due to nitrogen is different from oxygen in Si. Previous studies have shown that the locking strength of oxygen diminishes with increasing annealing temperature, while this is not the case with nitrogen at all temperatures. Alpass et al. have demonstrated that the nitrogen-induced locking strength at 550°C depends on the prior annealing temperature, peaking at $600 \sim 700^\circ\text{C}$ and decreasing to zero at 1000°C . At $T > 600^\circ\text{C}$, nitrogen disperses at interstitial positions in Si crystals and does not interrupt dislocation movement.^[140] However, Sumino et al. have demonstrated that N aggregates slow-moving dislocations and quiescent dislocations at high temperatures in CZ-Si.^[141] The clustered N atoms form clusters or complexes that possess high energy interactions with dislocations and strongly lock the dislocations. N-doping not

only affects the concentration of vacancies in CZ-Si, but also provides manufacturers with additional control over the O precipitation process in monocrystalline Si ingot grown by the CZ methods. Nowadays, Si ingots produced using the float zone technique are often doped with nitrogen, improving mechanical strength by pinning dislocations.^[142]

The effect of excessive metallic impurities in Si on electrical properties is also important. Nickel and copper impurity precipitates in polycrystalline Si mainly occur at dislocations and a small amount at GBs and microdefects.^[143] The precipitation is easily dissolved even at low temperature, indicating that the strain field of structural defects is not enough to stabilize the precipitation. Long-time gettering treatment can dissolve all measurable precipitation, but does not significantly improve the minority carrier diffusion length. These results indicate that, when metallic impurities interact with structural defects in Si, it is a difficult task to completely remove these impurities. However, under some specific conditions, impurities play a positive role in eliminating dislocations. For example, at 820 °C, under the additional driving force provided by P or Al gettering layer, different impurities such as Cu, Ni, and Fe are reduced and dislocation density is reduced by about 60% in polysilicon.^[78] According to X-ray fluorescence spectrometer spectra, Cu atoms have successfully diffused from the external Cu film to the gettering layer during both the Al and P gettering processes, which occurred in the presence of an external Cu film. As shown in **Figure 13**, Choi et al. have confirmed this hypothesis through two distinct experiments, where the presence of an inspiratory layer produces a net unidirectional flux of impurities to induce dislocation slips in the favored direction and subsequently vanish at the GB or surface. The increased lifetime of minority carriers after P gettering treatment may be the result of the decrease in dislocation density and impurity concentration.

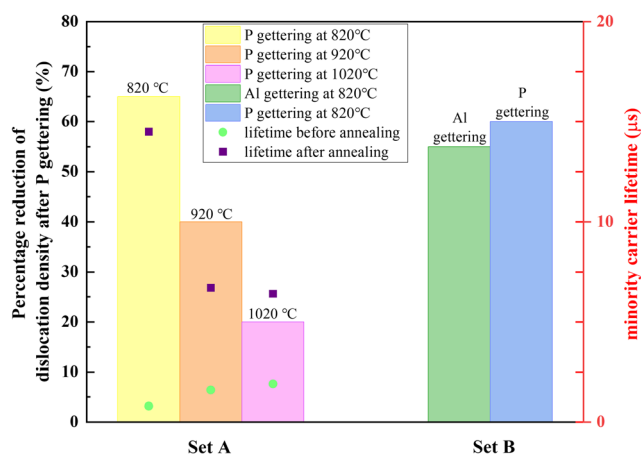


Figure 13. The data of optical microscope dislocation etch pit images indicate that 65%, 40%, and 20% dislocations in mc-Si with moderate impurity content (set A) are removed after P gettering at 820, 920, and 1020 °C, and values of minority carrier lifetime measured by μ -PCD increase from ~0.8 to 14.5 μ s, 1.6 to 6.7 μ s, and 1.9 to 6.4 μ s. 55% and 60% dislocations in mc-Si with low impurity content and an external 5 nm thick Cu layer (set B) are removed at 820 °C during Al and P gettering. The data are obtained from ref. [78].

5. Conclusion

This article reviews recent articles related to dislocations in crystalline Si solar cells. As a typical crystal defect, dislocations destroy the periodic structure of crystalline Si to produce additional dangling bonds, inducing deep energy levels in the bandgap of Si and affecting the performance of crystalline Si solar cells, especially the recombination performance, which seriously reduces the lifetime of minority carriers and suggests that the energy level generated by dislocation may play the role of a recombination center. There are several methods to directly or indirectly observe the activities and topography of dislocations, and it can be seen that some behaviors are not easy to be observed by a single technique, and are gradually revealed with the widespread use of observation methods combined with multiple techniques. Through the characterization of various methods, it can be found that dislocations affect not only the carrier lifetime of the device, but also the optical and electrical properties of the solar cell in the case of modification by other defects. Metallic impurities, such as iron, nickel, copper, and gold, whether precipitated or interstitial, can form additional impurity energy levels in the bandgap and influence electrical properties. In particular, when impurities accumulate in a certain area, dislocations extend deep into the Si substrate, creating a so-called filamentary effect that affects the band structure of Si. Also, the joint effect of dislocation and Na-ions is discussed. Na-ions penetrate dislocations to form or promote the growth of stacking faults, resulting in a PID effect that seriously affects the long-term stability of the device. When different types of dislocations meet to form a dislocation loop, the opposite effect is produced, which is a method used in dislocation engineering.

Dislocation engineering can inhibit dislocations in Si ingot by regulating the technological parameters during crystal growth. Dislocation annihilation in the grown crystal is mainly affected by temperature, stress, and activation energy of dislocation movement. Even if the dislocation density in the wafer decreases with increasing annealing temperature, annealing at high temperatures for an extended period adversely contaminates the wafer and impairs its electrical performance. Hydrogen, oxygen, nitrogen, and other nonmetallic impurities can effectively passivate or nail dislocations in the wafer, improving the electrical properties and mechanical strength of the Si. At 1000 °C, the dislocations in the wafer are constrained by the slip planes and cannot move freely. However, if supplemented by additional driving forces, such as appropriate unidirectional flux of impurities, the dislocation density can be reduced and the minority carrier lifetime of the wafer can be improved.

Overall, in recent years, a lot of research on dislocations in solar cells has been carried out and fruitful results have been achieved. More work is also being performed to explain some of the open-ended questions. Some examples of open problems are as follows: 1) clear understanding of the specific mechanism of the interactions between impurities and dislocations and related electrical structures; 2) exploration of dislocation engineering with lower energy consumption; and 3) visualization of the specific situation of dislocation interactions with other defects through theoretical simulations. The technology to truly develop dislocation-free photovoltaic devices at low cost is still a long way off.

Acknowledgements

This work was financially supported by LONGi Green Energy Technology Co., Ltd., the National Natural Science Foundation of China (grant no. 61804070), the Science and Technology Projects of Gansu Province (grant no. 21JR7RA467), and the Fundamental Research Funds for the Central Universities (grant no. lzujbky-2023-14).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

carrier transport, crystalline silicon, dislocations, solar cells

Received: November 29, 2023
Published online: December 27, 2023

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