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Review Article

Defect engineering for shallow n-type junctions in germanium: Facts and fiction

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An overview is given on the status of n-type dopant activation and diffusion in Ge, based on a standard ion implantation and annealing scheme. Emphasis is on defect engineering approaches to optimize either or both parameters. A detailed discussion is given on the use of co-implantation by neutral or other n-type dopants. As a case study, the impact of the C ion implantation energy and dose on n-type junctions in p-Ge by P + C co-implantation will be given. It is demonstrated that for fixed P implant conditions, there exist an optimum energy and dose for achieving a minimum junction depth by the formation of C–PV complexes. An alternative approach is the use of self-interstitial management at the end-of-range of the P implantation. Finally, an overview is given of alternatives for obtaining shallow, highly activated n-type junctions in Ge. They rely on: non-standard implantation schemes, ultra-short annealing methods or relying on *in situ* doped epitaxial deposition.

1 Introduction Achieving highly activated shallow n-type junctions in germanium remains challenging, in spite of the research efforts spent in the past decade (for recent overviews, see Refs. [1, 2]). Especially in the case of ion implantation, followed by a standard thermal anneal, a limited maximum activation level ($\sim 5 \times 10^{19}\,cm^{-3}$ for P) and concentration-enhanced dopant diffusion are well-known issues. The latter leads to a deep box-like profile, with a knee-concentration of around $2 \times 10^{19}\,cm^{-3}$ for P, forming the boundary between intrinsic and extrinsic or enhanced diffusion at the activation temperature [3–6]. An active level of $5 \times 10^{19}\,cm^{-3}$ at a junction depth x_j of 50 nm corresponds with a sheet resistance R_s of about 150 Ω sq^{-1} [7]. Keeping the same R_s, the active concentration needs to increase to a level of $2 \times 10^{20}\,cm^{-3}$ for an x_j of 20 nm, required for future technology nodes. This indicates that the active n-type dopant level must be increased and the concentration-enhanced diffusion is to be suppressed in order to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). It should be remarked that the roadmap targets with respect to junction depths and sheet resistance of junctions are the same, irrespective of the channel material, Si or Ge. This only translates in a lower active doping level for Ge because of the higher mobility. The active levels mentioned in the text are for Ge, based on the calculations of Duffy [7]. The same is valid for the specific contact resistivity.

Dopant diffusion in semiconductors is mediated by the intrinsic point defects (PDs): vacancies (V) or self-interstitials (I). It is well-established that in Ge, except for the case of B, a vacancy mechanism dominates dopant diffusion [1, 2, 8, 9]. The transport is governed by the negatively charged DV pair (D: donor) [1, 2], both in intrinsic and extrinsic conditions. Concentration-enhanced diffusion occurs, as a consequence of a Fermi level shift toward the conduction band with increasing active n-type concentration. This lowers the formation energy of doubly negatively charged vacancies and gives rise to more DV pairs. In a first approximation, it also explains the saturation of the active level in the $3–5 \times 10^{19}\,cm^{-3}$ range [10]. Considering the increasing binding energy of the DV pairs going from PV, over AsV to SbV explains the higher

activation enthalpy of P compared to As and Sb in Ge [8]. The lower effective diffusivity of P makes it the number one candidate for shallow junctions in Ge. At the same time, the highest active levels have been found for P compared with As, using standard ion implantation and rapid thermal annealing (RTA) [3–6]. Again, the DV pairs play a role in the de-activation, since they give rise to compensating acceptors and at the same time, can cause further dopant clustering by Coulomb attraction between $(DV)^-$ and D^+, yielding a neutral D_2V complex [2].

Given the prominent role of vacancies in dopant diffusion, it is clear that somehow, we need to control their formation in order to meet the targets of the ITRS roadmap. In addition, it should be kept in mind that besides the equilibrium vacancy concentration, dictated by the Fermi level at the annealing temperature, excess vacancies will also be created by the atomic displacements during ion implantation [10–12]. The excess vacancies escaping recombination with interstitials or diffusion to the Ge surface will tend to cluster at about half of the end-of-range (EOR) of the implantation during annealing. The fact that multiple implantation and multiple annealing schemes result in a higher active level [13] evidences the role played by the implantation damage, although the effect is less important than can be anticipated based on calculated damage profiles [10, 14] or has been found absent for the case of 90 keV As implants [9].

Based on the extensive knowledge which has been gathered on this topic, several schemes for point-defect engineering have been proposed [2, 15]. Most of these methods rely on controlling the excess vacancy (V) and dopant-vacancy pairs which are responsible for the fast transport and moderate activation [16, 17]. It is the aim of the present paper to critically review the different proposed schemes, with their weak and strong points and discuss their feasibility for Ge-based CMOS and photonic devices. Emphasis is on two methods, namely, co-implantation with another species in order to introduce a more efficient vacancy trap than the group V dopant atoms (Section 2) and self-interstitial injection to recombine with excess vacancies (Section 3). In the last part (Section 4), the use of more advanced ultrafast annealing schemes (flash and laser annealing), implantation techniques (hot and cryo implantation), and implantation-less doping for shallow n^+ junctions in germanium will be discussed.

2 Co-doping

2.1 Literature review The first method concerns the use of co-implantation with inactive impurities like F, C, or N. From first-principles density functional theory (DFT) calculations it is expected that F is the best choice, given the highest binding energy with V, due to its large electronegativity [18]. The calculated binding energy of F_nV is higher than for DV pairs. Diffusion control can be achieved by the competing trapping of excess vacancies and by trapping of DV pairs by the implanted F atoms. However, DFT calculations also point out that the penalty paid for achieving a shallow junction is the reduced degree of activation, as the formed F-, N-, or C-DV clusters are inactive or may form the nuclei for further DV clustering and inactivation. In this section, an overview of the literature will be presented, followed by a detailed study for the case of C + P co-implantation.

The theoretical predictions have triggered several experimental studies of co-doping with F [7, 19]. The obtained results are rather contradictory and not convincing about a positive role of F in dopant activation or diffusion control. It has been shown that the F (35 keV; 1×10^{15} at cm^{-2}) implantation enriches the Ge substrate with Vs, causing an accelerated diffusion of As (50 keV; 3×10^{13} at cm^{-2}) within the layer amorphized by the As and F implantation, which recrystallizes during furnace annealing in the 450–600 °C range (1 h) [20]. At the same time, F forms complexes with Ge interstitials in the EOR region, next to the originally amorphized Ge layer. These act as a sink for V and cause an abrupt stop for the As diffusion at 450 °C anneal [20]. This effect is lost and only enhanced diffusion of As compared with the reference As-only implant is found at 500 °C, due to the complete loss of the F dose by out-diffusion. It implies that the thermal window for F co-implantation in Ge is rather narrow. Similar results have been obtained for P + F ion implantation after RTA for 1 s at 600 °C [7]. Application of a Ge pre-amorphization implant (PAI) at 150 keV (1×10^{14} at/cm^2) before a 15 keV 1×10^{15} at/cm^2 P and 10 keV 1×10^{15} at/cm^2 F implant did not result in a marked effect on the P diffusion at 500 °C 3 min anneal under an inert atmosphere [19]. This was also confirmed by El Mubarek [22].

Overall, it can be concluded that the impact of F on dopant diffusion is rather limited to temperatures below 500 °C – only operational at 400–450 °C – and is related to the stabilization of the excess interstitials at the EOR region by forming F-I clusters. These create a sink for excess vacancies, which terminates the enhanced diffusion of P (and P-V pairs) at the EOR. The limited stability (dissolution) of the clusters at higher temperature explains the absence of any beneficial effect of F at or above 500 °C [20].

With respect to dopant activation, it has been observed that the F–I clusters formed at the end-of-range act as compensating acceptors [21]. At the same time, it has been demonstrated that co-implantation of As with F, followed by an RTA at 500 °C for 10 s reduced the compensating V-related acceptors, created either during ion implantation or in a chemical vapor deposited (CVD) epitaxial Ge layer [23]. It is believed that F effectively passivates these V-related acceptors, which anneal out at 600 °C.

Carbon was one of the first co-dopants which triggered the interest of both experimentalists [24, 25] and theoreticians [26, 27]. It has been demonstrated that, both for P ion implantation [24] and for *in situ* doped molecular beam epitaxy (MBE) multilayers of P, As, or Sb, the presence of C retards the diffusion of the dopants in germanium. DFT calculations have shown that the

interaction between C and DV pairs leads to energetically favorable and relatively immobile complexes [26–28], whereby the association between V, Sb, and C leads to more stable complexes than with As or P. Recently, a simple C-DV cluster model has been implemented in a commercial technology computer aided design (TCAD) package (Sentaurus), yielding satisfactory agreement between measured secondary ion mass spectrometry (SIMS) and simulated profiles [29]. The drawback of this is that these complexes are electrically neutral or even compensating acceptors, so that the sheet resistance of the resulting shallower n^+ junctions may be compromised. However, little information is available on the electrical performance of C co-implanted n^+ junctions in Ge. This will be addressed in more detail in the next section.

An additional motivation for the use of C co-implantation is the fact that it leads to a more stable nickel germanide and may induce dopant segregation at the metal/semiconductor interface [30]. This is advantageous to lower the contact resistivity, by the combined reduction of the Schottky barrier height and the enhanced tunneling through the narrower depletion region (higher field) induced by the higher active doping density.

The use of nitrogen as a co-implantation species in germanium was explored in Ref. [31] and further investigated by Thomidis et al. [32]. A strong suppression of the diffusion of low-energy implanted (11 keV; dose 1×10^{15} at cm^{-2}) P by a 10 keV, 5×10^{14} at cm^{-2} N co-implantation has been achieved, following 30 s RTA at 550, 600, and 650 °C in N_2. Figure 1 illustrates the impact of N + P co-implantation on the concentration-enhanced diffusion, yielding about 50 nm shallower n^+ junctions [31]. While the positive impact of N on the diffusion of n-type dopants in Ge was originally ascribed to its ability to trap vacancies [31, 33], more recent experiments have pointed out an alternative mechanism [32]. The observed anomalous diffusion has been ascribed to an interstitial-mediated diffusion of nitrogen. This N diffusion toward the surface appears to depend on the formation of nitrogen PD clusters (most likely involving Ge interstitials) at the EOR damage region. These supposed N_nI_m clusters stabilize the presence of excess interstitials at the initial annealing stages and act as a source of I injection during cluster dissolution, which may retard the PV-mediated diffusion [34]. The existence of such clusters has been derived from the presence of "kinks" in the nitrogen SIMS profiles at the former amorphous/crystalline (a/c) interface, i.e., at the EOR region. This suggests some trapping of nitrogen atoms by the self-interstitial clusters which usually form at the EOR, as evidenced by cross-sectional TEM.

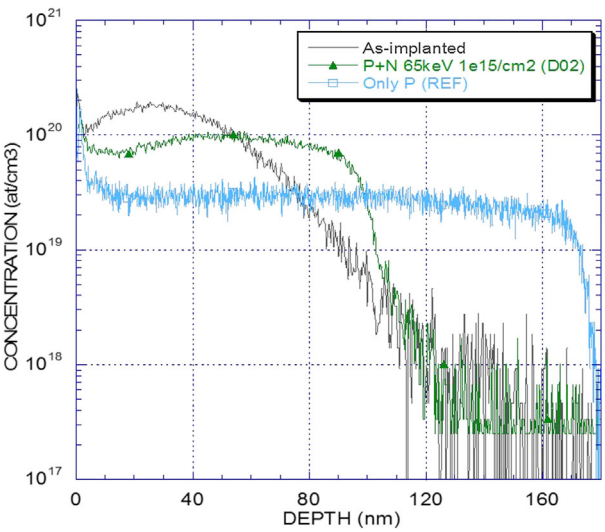

Figure 1 SIMS P profiles as-implanted and following a 600 °C 60 s RTA, with (green line) 40 keV 1×10^{15} at cm^{-2} or without (blue line) nitrogen co-implantation. A 120 keV 1×10^{15} at cm^{-2} Ge PAI has been applied in both cases.

More recently, it has been demonstrated that even during millisecond non-melt laser annealing, the diffusion of P is retarded when co-implanted with N [35]. At the same time, it was observed that the active level was lower for the P + N case. According to DFT calculations, this can be ascribed to the formation of P–N complexes [35]. This also indicates that the possible role of N-related shallow donors in Ge is negligible, as this would lead to a higher active concentration. They can add active concentration if the ground state is shallow enough and the concentration is high enough, similar as P or As. Such donors are known better in silicon and may also form in Ge.

From the above literature, it is clear that the exact diffusion retardation mechanism induced by N is still a matter of discussion, whereby DFT points to the vacancy trapping mechanism and some experimental results conclude differently. Most likely, the annealing (atmosphere, cap layer) and the implantation conditions (proximity of the EOR to the Ge surface, set by the implantation energy) [34] play a role in the interaction between N and the implantation-induced native point defects. It has for example been demonstrated by B diffusion studies under high-temperature 2.5 MeV proton irradiation that the Ge surface is not an efficient sink for self-interstitials. This could be related to the presence of donor-like interface states which reflect the positively charged Is [36].

Based on DFT calculations [2, 18, 37, 38], one can expect that the co-implantation of P with As or Sb may also result in shallower junctions, based on the fact that the binding energy between Sb and As with V is higher, leading to a more efficient V-trapping, compared with P. In this way, the vacancies are consumed more by the co-implant species, while P experiences slower diffusion. The available free vacancies are in first order suppressed for a higher [As]/[P] of [Sb]/[P] concentration ratio (square brackets denote chemical concentration). At the same time, this will lead to a higher P clustering and de-activation, when considering thermodynamic equilibrium conditions [37]. This implies that the co-implantation conditions have to be carefully

optimized in order to meet the goal of a shallow, highly activated n^+ junction in Ge.

Experiments on P + As concurrent and successive co-doping, using furnace anneals from 700 to 750 °C for 30 min in N_2 did not result in any changes in the P diffusion profile [39]. In the successive case, one species is implanted and annealed, followed by the same sequence for the second species. Moreover, a loss of activation was found for all co-implants, indicating close to equilibrium conditions. The absence of a positive co-doping effect indicates that the higher binding energy of AsV pairs does not improve the fast diffusion of P at the rather high (and long) furnace anneals used in this study. An additional factor which should be further considered in the co-doping of Group V dopant species is the impact of the lattice strain associated with the different species.

The case is different for P + Sb co-implants, as was first successfully demonstrated by Kim et al. [40, 41] and later by Thareja et al. [42]. Dopant activation over 1×10^{20} cm^{-3} has been reached [40–42], yielding Ge n^+p diodes with an on/off current ratio of 10^5 and significantly reduced specific contact resistivity ($\rho_c \sim 8 \times 10^{-7}\,\Omega\,cm^2$) [42]. An active level of 8.6×10^{19} cm^{-3} has been demonstrated for P + Sb co-implants in more recent investigations [43, 44]. P and Sb co-implantation has also been employed to increase the thermal robustness of NiGe contacts, whereby the dopant ion implantation took place after the germanidation [45]. The improved activation and diffusion control indicates that the role of Sb is to capture the excess vacancies at the expense of PV pairing, so that the enhanced diffusion of P is reduced and also the activate level improved by less PV complex formation. In addition, the difference in atomic radii of P and Sb gives rise to a stress compensation effect, which may add to an improved n^+ junction formation in Ge.

While ion implantation is the preferred technique to control the effect of co-doping, it is clear that one should keep in mind that the conditions (energy and dose) of the co-implant should be carefully fine-tuned in order not to aggravate the problem. If too high a dose/energy is used, the associated implantation damage will add on top of the one of the dopant species and operate as an additional source of vacancies or interstitials. This will be made clear in the following section.

2.2 The case of C co-doping In order to gain more insight in the effect of C co-doping, a systematic study with respect to the implantation parameters (C dose and energy) has been undertaken as described in more detail elsewhere [46]. Besides the chemical profiles by SIMS, electrical characterization has been carried out to derive the active level. The experiments have been performed on 200 mm Ge virtual substrates, consisting of 1.5 μm non-intentionally doped Ge epitaxial layers grown by reduced pressure chemical vapor deposition (RPCVD) on Si. Before the implantation, no extra surface preparation or cleaning was employed. All samples received a Ge PAI at 20 keV, 6×10^{14} at cm^{-2}, followed by C implantation at different energies ranging from 3 keV to 20 keV and doses varying from 5×10^{14} to 2×10^{15} at cm^{-2}. P was implanted with a fixed condition using an energy of 5 keV and dose of 2×10^{15} at cm^{-2} and was completely contained in the pre-amorphized Ge layer, to reduce ion channeling. During annealing, to prevent out-diffusion of the implanted dopants, all samples were capped with a 20 nm thick SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) at 280 °C. The annealing process was carried out in N_2 ambient at 600 °C for 60 s.

The main results are summarized in Fig. 2, showing that there is a clear impact of the C co-implantation on the resulting SIMS profile of P (Fig. 2a). The shallowest junction is obtained for the 8 keV C implantation (dose 1×10^{15} at cm^{-2}) [46]. In all co-doped cases, a shallower P profile has been achieved compared with the P only condition, which shows the traditional box-like profile after RTA [3–6]. The optimum condition corresponds with a

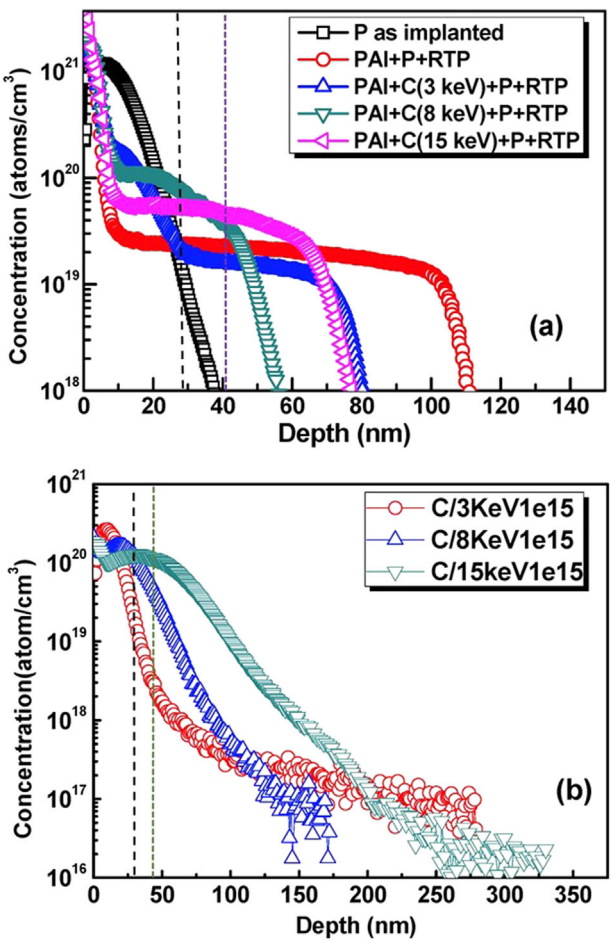

Figure 2 Contribution of carbon co-implantation to phosphorus diffusion in germanium. (a) P SIMS profiles under various C co-implant energy after annealing (the carbon dose is 1×10^{15} at cm^{-2}). (b) C distribution in Ge after annealing. The a/c interface is indicated by the vertical dashed lines. It is approximately 34 nm, except for the 15 keV C case, where it increases to 41 nm [46].

C profile in Fig. 2b, which is straddling the a/c interface at about 34 nm depth. For the 3 keV condition, the C profile is completely contained in the a-Ge layer and, while there is some slowing of the P diffusion, the amount of C atoms below the a/c interface in the crystalline Ge is not enough to stop all PV pairs from diffusing in the Ge virtual substrate. At the same time, this should not be a problem for the deeper C co-implants, but still they are less effective in controlling the P diffusion than in the 8 keV case.

In order to explain the observed trends, SRIM simulations have been carried out, as shown in Fig. 3, comparing the expected as-implanted P and C profiles with the damage created during the implantation. The two vacancy profiles correspond with the PAI damage and the vacancy profile created by the C implantation (as the P is implanted in an a-Ge layer, there will be negligible contribution to the V profiles). A detailed analysis of these simulation results has shown that the optimum C condition corresponds with the presence of a sufficient carbon concentration below the a/c interface, while at the same time, the associated damage should be small enough, i.e., the concentration of carbon ion-implantation-induced vacancies below the interface in the c-Ge should not overwhelm the Ge PAI damage [46]. In this way, one assures that there are sufficient C atoms below the a/c interface to trap PV pairs.

At the same time, the associated ion implantation damage is small enough, not to act as an additional source of vacancies and enhanced P diffusion during the anneal. This implies that not only the C energy but also the dose should be optimized, as shown in more detail elsewhere [46]. This is among others demonstrated by the impact on the electrical activation [46]. In the best case (8 keV C; 1×10^{15} at cm^{-2}), no activation penalty is paid, yielding a similar active level than for the P only condition, with average active concentrations in the range of 2–3 $\times 10^{19}$ cm^{-3} [46].

2.3 Summary co-doping Finally, a summary of part of the literature data on the use of co-implantation for n-type dopant optimization in Ge is provide in Table 1.

3 Self-interstitial injection A second class of methods to control the extrinsic P diffusion relies on native point defect management by creating an excess self-interstitial concentration. Besides trapping vacancies in more stable complexes than the DV ones, another pathway is to recombine Vs with Is [47]. In silicon, thermal oxidation of the surface is a source of self-interstitial injection. However, this is not the case for Ge at typical implant annealing temperatures, due to the volatility of GeO. This means that an alternative source of Is has to be created. An elegant solution to that problem has been proposed in the context of the study of B diffusion in Ge [47, 48]. As sketched in Fig. 4, it consists of a deep oxygen implantation (235 keV, 4×10^{14} at cm^{-2}), followed by a 650 °C furnace annealing [48]. This causes the formation of GeO_x nanoclusters, which, due to the lower density of GeO_x compared with Ge, will release the elastic stress by

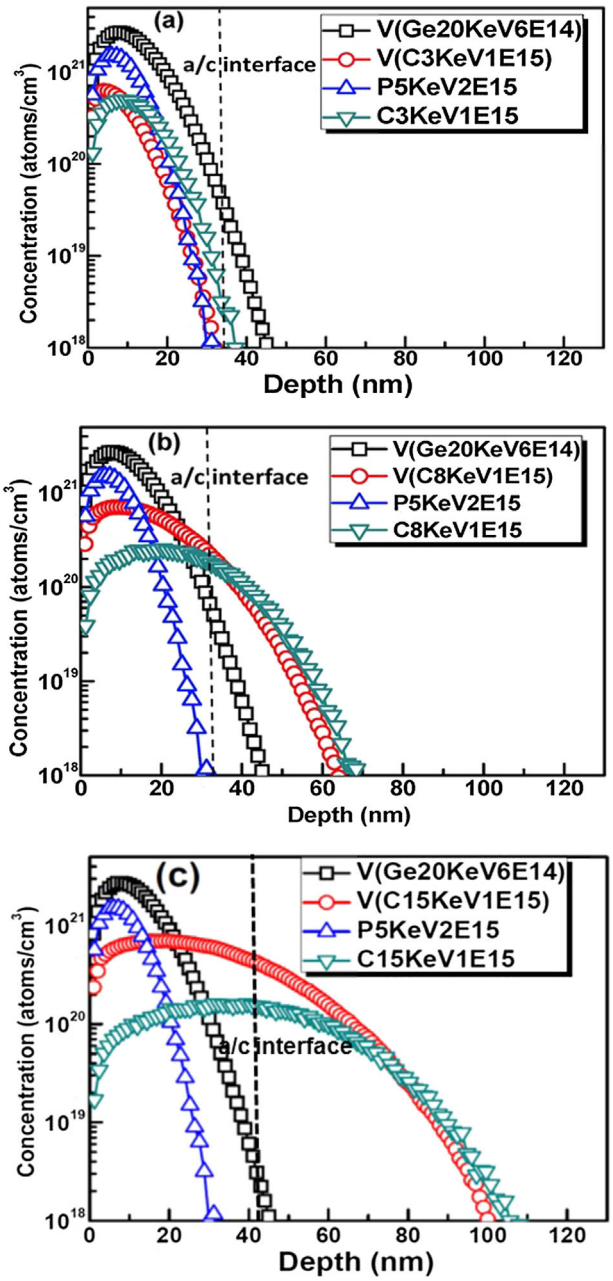

Figure 3 SRIM simulation results of the as-implanted P and C profiles and of the damage (vacancy V) profiles, corresponding with the Ge pre-amorphization implantation (Ge at 20 keV and 6×10^{14} at cm^{-2}). The profiles have been calculated for a fixed C dose of 1×10^{15} at cm^{-2} and an energy of (a) 3 keV; (b) 8 keV; and (c) 15 keV. In each case, the a/c interface is indicated by the dashed line.

self-interstitial injection. This leads to a significant broadening of B doping spikes (deposited by MBE) after 30 min annealing and lasts up to 2 h treatment [48], indicating the I-mediated enhanced diffusion of B.

As shown in the right diagram of Fig. 4, one could apply the same method for the diffusion control of n-type dopants.

Table 1 Co-implantation and annealing conditions for n-type doping in Ge. R, rapid thermal annealing; F, furnace annealing; and L, laser annealing.

Co-implant species (energy, keV, dose at cm^{-2})	Ge PAI	anneal (°C)	Ref.
$F(35, 1\times10^{15}) + As(50, 3\times10^{13})$	no	400–500F	[21]
$F(40, 1\times10^{15}) + P(30, 6\times10^{13})$	no	400–500F	[22]
$F(40, 1\times10^{15}) + P(30, 1\times10^{15})$	no	400–500F	[22]
$N_2^+(65, 1\times10^{15}) + P(40, 1\times10^{15})$	yes	600R	[31]
$N_2^+(10, 5\times10^{14}) + P(11, 1\times10^{15})$	no	550–650R	[32]
$N_2^+(30, 1\times10^{15}) + P(30, 1\times10^{15})$	no	750–800L	[35]
C(not specified) + $P(25, 4\times10^{15})$	no	650R	[24]
$P(90, 6\times10^{14}) + Sb(65, 6\times10^{14})$	no	500R	[42]
$P(50, 1\times10^{15}) + Sb(65, 1\times10^{15})$	no	500–600R	[45]
P(30, 5e14) + $As(65, 5\times10^{14})$	no	600–750F	[39]

So far, this idea has not been tested out. For application in advanced CMOS technology, the oxygen should be implanted at lower energies, closer to the junction to be more effective. At the same time, the formation of GeO_x precipitates/nanoclusters can introduce deep states in the band gap which can enhance the drain/substrate leakage current, when present in the depletion region. However, it has recently been reported that the off-state current and electron mobility of Ge nMOSFETs can be improved by the presence of oxygen in the substrate [49, 50]. ^{16}O ions have been intentionally implanted in Ge (100) wafers at a dose of 1×10^{13} and 1×10^{14} at cm^{-2} with 100 keV energy, resulting in a reduced leakage current of the formed n^+p junctions [50].

This indicates that the presence of oxygen reduces or modifies the density of processing-induced deep states in the depletion region, such that the generation lifetime is increased. Whether this also impacts on the depth of the P-implanted junctions (50 keV, 1×10^{15} at cm^{-2}), annealed for 30 s at 600 °C has not been reported and deserves further investigation. It demonstrates, however, that there is some potential for oxygen-related defect engineering in Ge n-channel devices. It should be remarked that, on the other hand, no impact of oxygen implantation on Ge pMOSFETs was noticed [49, 50].

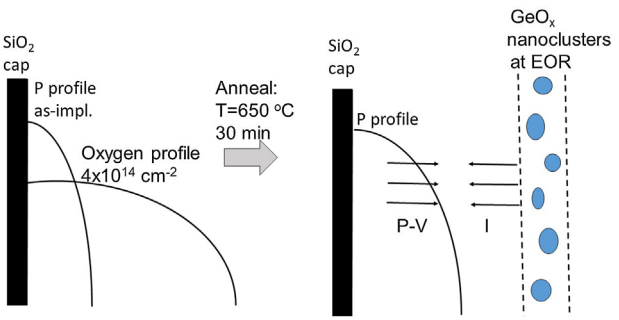

Figure 4 Schematic representation of using oxygen nanoclusters as a source of germanium self-interstitials for P diffusion control. This is based on the original concept by Mirabella et al. [47] for studying transient-enhanced diffusion (TED) of B in oxygen co-implanted Ge.

Whether oxygen implantation is practical for advanced Ge bulk FinFETs remains to be seen. However, one should realize that during ion implantation, excess self-interstitials will be injected in the Ge substrate in the vicinity of the EOR region [51, 52]. For an amorphizing implant, the solid-phase epitaxial regrowth (SPER) results in a recrystallization of the damaged layer, starting from the a/c interface, while the excess interstitials will cluster in the vicinity of the a/c interface to form so-called EOR defects [14, 53–56]. However, observation of EOR defects in Ge after standard RTA anneals in the range of 500–600 °C typical for n-type dopant implantation activation, is not that obvious [5, 6]. The reason is that interstitial clusters are rather unstable in Ge, dissolving at fairly low temperatures, i.e., between 450 and 550 °C [53] or even lower (400 °C) [55]. It has been shown that the surface proximity plays a decisive role in the thermal stability of the EOR damage [56, 57]. As a rule, the shallower the implantation energy, the lower the dissolution temperature of the interstitial clusters becomes. This means that during typical RTA steps for n-type dopant activation, no interstitial EOR damage is formed, so that they cannot be employed as interstitial sources for vacancy annihilation.

A possibility to overcome this problem is to rely on a two-step annealing strategy, combining a low temperature step in the range 350–400 °C to form the interstitial clusters and recrystallize the implanted layer by SPER. A second higher temperature step, i.e., at 500 °C may be required to enhance the active concentration, in case this is not achieved by the SPER step. The EOR damage formed during the first step can then be used as a source of interstitials to suppress the enhanced n-type dopant diffusion. This has in principle already been validated for the case of P + F and P + N co-implantations where the interstitial clusters are stabilized by the presence of the co-implant species [20, 34].

4 Alternative implantation, annealing, and doping schemes

4.1 Alternative implantation schemes It is clear from the foregoing that in order to control the diffusion and activation of n-type dopants in Ge, one should be in the first instance concerned with the ion-implantation-induced point defects. This has led to the idea of applying multiple implant and multiple annealing (MIMA) schemes [13], where one high-dose and highly damaging implantation, followed by an anneal is replaced by two (or more) lower-dose implants and anneals. This reduces the amount of excess vacancies at each process sequence more effectively than in the single-step case and results in a higher active concentration [13]. The MIMA technique has also been applied to reduce the contact resistivity ρ_c to n-Ge [58]. Combining several 50 keV P^+ implants to a dose of 5×10^{14} cm^{-2} and RTA at 500 °C for 30 s led to a low ρ_c of 3.8×10^{-7} Ωcm^2 for a

Ti/Al direct contact on n-Ge by the achieved higher active concentration. Very low ρ_c values of $3 \times 10^{-8}\,\Omega cm^2$ have been obtained by combining a two-step P implantation, with NiGe [59]. While this method nicely illustrates the impact of the implantation damage on the active dopant level in n-type Ge, from a CMOS integration viewpoint it is less practical, given the low(er) throughput, so alternatives have been looked for.

Another practical reason to avoid high-dose, amorphizing implantations in Ge is the observation that in the case of a FinFET architecture, annealing usually results in an imperfect recrystallization of the lattice, giving rise to the presence of extended defects in the corners of the fins [60]. The reason is that for the case of a narrow fin, recrystallization occurs both from the (100) surface plane and in the (110) sidewall planes, whereby there is no crystalline template available for the latter case. This results in the formation of (111) stacking faults and twin boundaries where the two crystallization fronts meet [60]. A possible solution to this problem is the use of so-called hot implants [61], which have the advantage to suppress the damage formation by dynamic annealing, making it harder to amorphize the material. Initial studies on 400 °C P implantation in Ge and GeSn indicate that damage annealing occurs but an additional annealing step is required to enhance the dopant activation [62]. Other studies revealed that for a 10 keV As^+ implantation at a dose of 1×10^{15} at cm^{-2} and 400 °C, a residual amorphous Ge layer has been found, however, much smaller than for the room temperature reference condition [63].

Alternatively, one can consider the use of cold or cryogenic implantations [63–65], resulting in a more uniform damage profile and a thicker a-Ge layer, with less point defects below the a/c interface in the end-of-range region. In the case of 10 keV As^+ implants at −50 °C this has led to the lowest sheet resistance after activationannealing at 600 °C, compared with RT or 400 °C implantations [63]. Combining with heavy ion (Xe or Ar) PAI prior to the As^+ implantation yielded the best results. Using Ar or Xe results in less excess vacancies in the Ge substrate, as a lower dose is required for amorphization. Superior n^+p junctions have been processed after a 2.2×10^{15} at cm^{-2}, 90 keV P implantation at −100 °C, followed by 400 °C RTA, with a five times reduction in leakage current compared with standard room temperature implants [66]. Gate-last Ge nMOSFETs processed with the cryo-implanted junctions yielded a five times lower off-current and a higher on-current compared with RT and 400 °C P implantations.

4.2 Annealing schemes Besides changing the ion implantation method, one can also consider alternative annealing schemes in order to impact the diffusion and/or activation of n-type dopants in Ge. Experiments with proton irradiation during annealing have demonstrated the importance of electron-hole pairs created by ionization damage on the self-diffusion and dopant diffusion [36, 67, 68]. Of course, this is more of fundamental than of practical interest.

A more realistic approach is to investigate low-temperature SPER of an amorphous Ge layer as an alternative for dopant activation. The principle relies on the recrystallization from the a/c interface, using the c-Ge as a template for the regrowth, which should occur for temperatures of about 300 °C and higher. It has been shown that dopant segregation into the a-Ge occurs during annealing at 350 °C [69], so that more dopants become trapped in the near surface region, resulting hopefully in a metastable activation beyond the equilibrium solid solubility at the annealing temperature. A detailed study confirms the metastable activation of P by SPER at either 400 or 500 °C up to a maximum of $7 \times 10^{19}\,cm^{-3}$ [70]. Subsequent annealing at 400 °C resulted in an increase in the sheet resistance confirming the metastable activation. At the same time, no clear impact of co-implantation with F was found [70].

While it has been shown that traditional RTA or even spike annealing does not result in metastable activation above the solid solubility of the dopants, this could be achieved by ultra-short ms flash-lamp annealing [71] and laser annealing (LA) [72–81]. In the first case, the highest active level for P (3 keV, 3×10^{15} at cm^{-2}) of $6.5 \times 10^{19}\,cm^{-3}$ has been obtained after a 3 ms 97 kJ flash, without any pretreatment (Ge PAI or 400 °C for 240 s preheating) [71]. For laser annealing, a high substitutional (active) fraction beyond $1 \times 10^{20}\,cm^{-3}$ has particularly been noticed for Sb implantations [75–77], yielding well performing Ge nMOSFETs [76] and n^+p diodes [77]. It was at the same time reported that for a melt laser annealing high concentrations of vacancies and Sb_mV_n complexes are formed in the implanted layer, leading to a significant deactivation [79]. Pulsed laser annealing has also been applied to 3×10^{15} at cm^{-2}, 40 keV As implants, showing a record maximum active level of $1 \times 10^{20}\,cm^{-3}$ for 10 pulses at $650\,mJ\,cm^{-2}$ [80].

Given these promising results, LA has been implemented to fabricate low contact resistivity ohmic contacts to n-type Ge [43, 81]. It has been shown that an active Sb level of $1.9 \times 10^{19}\,cm^{-3}$ could be reached after LA at $0.4\,J\,cm^{-2}$ power, resulting in a specific contact resistivity for NiGe/n^+-Ge of $1.9 \times 10^{-8}\,\Omega cm^2$ [43]. LA also improves the I_{on}/I_{off} ratio and the leakage current of Ge n^+p junctions [82–84], reaching values of 10^7 and a low leakage current density of $8.3 \times 10^{-5}\,A\,cm^{-2}$ [83]. It also allowed the successful fabrication of Ge nMOSFETs, with a ten times better I_{on}/I_{off} performance than for devices with RTA and a peak electron mobility of $603\,cm^2\,V^{-1}s^{-1}$ [85–87].

Quite recently, microwave annealing has been applied to dopant implanted Ge [88, 89]. An example is shown in Fig. 5 for the case of P and P + C co-implantation. It has also been demonstrated that the RTA temperature could be reduced significantly between 120 and 150 °C to reach the same active P level as with standard RTA [88].

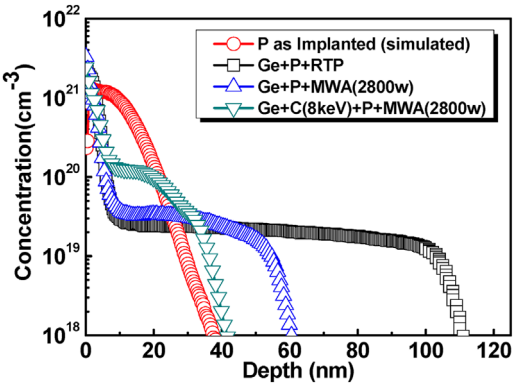

Figure 5 SIMS P profiles after 5 keV P implantation to a dose of 2×10^{15} at cm^{-2}, following RTP at 600 °C for 60 s or micro-wave annealing (MWA) at a power of 2800 W.

4.3 Alternative doping schemes In order to avoid the issue of implantation-induced point defects, one can apply other methods to introduce the n-type dopants in Ge. A first possible choice is the application of solid-state source diffusion, for example, from phosphor-doped silicon glass (PSG), which was investigated early in Ref. [90]. A technique gaining more and more popularity is *in situ* doping during CVD of epitaxial Ge layers, using PH_3 as a dopant precursor [91–96]. This allows the fabrication of steep profiles, with little diffusion since typical CVD temperatures are in the range of 350–400 °C. Combination of *in situ* P doping and LA resulted in an active P concentration of $\sim 3 \times 10^{20}$ cm^{-3} and a specific contact resistivity of 1.5×10^{-8} Ωcm^2 between NiGe and n$^+$ Ge [96]. It has also been demonstrated that a Si delta layer deposited by CVD can be used to control the diffusion of P in n-Ge [97]. Employing a delta-doped P layer [98] or a so-called atomic layer doping (ALD) [98–101] by exposure to PH_3 at low temperatures (RT to 400 °C), followed by a diffusion anneal yields abrupt and highly activated n-type profiles in Ge and is a promising route for future technology developments of Ge nMOSFETs and photonic devices (lasers [102]).

It has been proposed to use an *in situ* doped CVD Ge layer as a source of solid phase doping, whereby the dopants are out-diffused from the layer during deposition at 450 °C, which is subsequently removed by wet etching [103]. Besides CVD of *in situ* As-doped Ge, the feasibility for employing gas-phase doping by metal organic vapor phase epitaxy (MOVPE) with tertialybutylarsine (TBA) as As source has been demonstrated [104, 105]. High-performance GeO_2/Ge nMOSFETs have been fabricated in this way, with an electron mobility of 1020 cm^2 V^{-1}s^{-1} [103]. High active Sb concentrations ($\sim 2 \times 10^{20}$ cm^{-3}) were also achieved by MBE at a growth temperature of 160 °C [106].

Finally, the use of a spin-on dopant source, followed by RTA has been employed to form Ge nMOSFETs [107], showing improved performance compared with standard ion-implanted counterparts, with an I_{on}/I_{off} ratio of 10^4–10^5, a low subthreshold swing of 111 mV/decade and a high peak effective electron mobility of 679 cm^2 V^{-1}s^{-1}.

5 Conclusions In conclusion, it can be stated that in recent years, improved fundamental and practical insight in the diffusion and activation of n-type dopants in Ge has been gathered. Activation above equilibrium solubility has been achieved in a number of cases and even demonstrated in planar n-channel transistors. However, implementation in a realistic Ge nFinFET integration scheme remains challenging and more exploratory and development work is needed to achieve this goal.

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References

[1] J. Vanhellemont and E. Simoen, Mater. Sci. Semicond. Process. **15**, 642 (2012).
[2] A. Chroneos and H. Bracht, Appl. Phys. Rev. **1**, 011301 (2014).
[3] C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat, Appl. Phys. Lett. **83**, 3275 (2003).
[4] C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat, Appl. Phys. Lett. **87**, 091909 (2005).
[5] A. Satta, E. Simoen, R. Duffy, T. Janssens, T. Clarysse, A. Benedetti, M. Meuris, and W. Vandervorst, Appl. Phys. Lett. **88**, 162118 (2006).
[6] A. Satta, E. Simoen, T. Janssens, T. Clarysse, B. De Jaeger, A. Benedetti, I. Hoflijk, B. Brys, M. Meuris, and W. Vandervorst, J. Electrochem. Soc. **153**, G229 (2006).
[7] R. Duffy and M. Shayesteh, ECS Trans. **45**, 189 (2012).
[8] S. Brotzmann and H. Bracht, J. Appl. Phys. **103**, 033508 (2008).
[9] M. Naganawa, Y. Shimizu, M. Uematsu, K. M. Itoh, K. Sawano, Y. Shiraki, and E. E. Haller, Appl. Phys. Lett. **93**, 191905 (2008).
[10] E. Simoen and J. Vanhellemont, J. Appl. Phys. **106**, 103516 (2009).
[11] M. Koike, Y. Kamata, T. Ino, D. Hagishima, K. Tatsumura, M. Koyama, and A. Nishiyama, J. Appl. Phys. **104**, 023523 (2008).
[12] S. Koffel, R. J. Kaiser, A. J. Bauer, B. Amon, P. Pichler, J. Lorenz, L. Frey, P. Scheiblin, V. Mazzocchi, J.-P. Barner, and A. Claverie, Microelectron. Eng. **88**, 458 (2011).
[13] J. Kim, S. W. Bedell, and D. K. Sadana, Appl. Phys. Lett. **101**, 112107 (2012).
[14] S. Koffel, N. Cherkashin, F. Houdelier, M. J. Hytch, G. Benassayag, P. Scheiblin, and A. Claverie, J. Appl. Phys. **105**, 126110 (2009).
[15] H. Bracht, Phys. Status Solidi A **211**, 109 (2014).
[16] H. Bracht and S. Brotzmann, Mater. Sci. Semicond. Process. **9**, 471 (2006).
[17] A. Chroneos, H. Bracht, R. W. Grimes, and B. P. Uberuaga, Appl. Phys. Lett. **92**, 172103 (2008).
[18] A. Chroneos, R. W. Grimes, and H. Bracht, J. Appl. Phys. **106**, 063707 (2009).

[19] R. Duffy, M. Shayesteh, M. White, J. Kearney, and A.-M. Kelleher, ECS Trans. **35**, 185 (2011).
[20] G. Impellizzeri, S. Boninelli, F. Priolo, E. Napolitani, C. Spinella, A. Chroneos, and H. Bracht, J. Appl. Phys. **109**, 113527 (2011).
[21] G. Impellizzeri, E. Napolitani, S. Boninelli, J. P. Sullivan, J. Roberts, S. J. Buckman, S. Ruffell, F. Priolo, and V. Privitera, ECS J. Solid State Sci Technol. **1**, Q44 (2012).
[22] H. A. W. El Mubarek, J. Appl. Phys. **114**, 223512 (2013).
[23] W.-S. Jung, J.-H. Park, A. Nainini, D. Nam, and K. C. Saraswat, Appl. Phys. Lett. **101**, 072104 (2012).
[24] G. Luo, C.-C. Cheng, C.-Y. Huang, S.-L. Hsu, C.-H. Chien, W.-X. Ni, and C.-Y. Chang, Electron. Lett. **41**, 1354 (2005).
[25] S. Brotzmann, H. Bracht, J. Lundsgaard Hansen, A. Nylandsted Larsen, E. Simoen, E. E. Haller, J. S. Christensen, and P. Werner, Phys. Rev. B **77**, 235207 (2008).
[26] A. Chroneos, B. P. Uberuaga, and R. W. Grimes, J. Appl. Phys. **102**, 083707 (2007).
[27] A. Chroneos, R. W. Grimes, B. P. Uberuaga, and H. Bracht, Phys. Rev. B **77**, 235208 (2008).
[28] A. Chroneos, Phys. Status Solidi B **244**, 3206 (2007).
[29] N. Zographos and A. Erlebach, Phys. Status Solidi A **211**, 143 (2014).
[30] Q. Liu, G. Wang, N. Duan, H. Radamson, H. Liu, C. Zhao, and J. Luo, ECS J. Solid State Sci Technol. **4**, 119 (2015).
[31] E. Simoen, A. Satta, A. D'Amore, T. Janssens, T. Clarysse, K. Martens, B. De Jaeger, A. Benedetti, I. Hoflijk, B. Brijs, M. Meuris, and W. Vandervorst, Mater. Sci. Semicond. Process. **9**, 634 (2006).
[32] C. Thomidis, M. Barozzi, M. Bersani, V. Ioannou-Sougleridis, N. Z. Vouroutsis, B. Colombeau, and D. Skarlatos, ECS Solid State Lett. **4**, 47 (2015).
[33] A. Chroneos, J. Appl. Phys. **105**, 056101 (2009).
[34] D. Skarlatos, M. Bersani, M. Barozzi, D. Giubertoni, N. Z. Vouroutzis, and V. Ioannou-Sougleridis, ECS J. Solid State Sci. Technol. **1**, 315 (2012).
[35] S. Stathopoulos, L. Tsetseris, N. Pradhan, B. Colombeau, and D. Tsoukalas, J. Appl. Phys. **118**, 135710 (2015).
[36] S. Schneider, H. Bracht, J. N. Klug, J. Lundsgaard Hansen, A. Nylandsted Larsen, D. Bougeard, and E. E. Haller, Phys. Rev. B **87**, 115202 (2013).
[37] A. Chroneos, R. W. Grimes, H. Bracht, and B. P. Uberuaga, J. Appl. Phys. **104**, 113724 (2008).
[38] H. A. Tahini, A. Chroneos, R. W. Grimes, and U. Schwingenschlögl, J. Appl. Phys. **113**, 073704 (2013).
[39] P. Tsouroutas, D. Tsoukalas, and H. Bracht, J. Appl. Phys. **108**, 024903 (2010).
[40] J. Kim, S. W. Bedell, S. L. Maurer, R. Loesing, and D. K. Sadana, Electrochem. Solid-State Lett. **13**, H12 (2010).
[41] J. Kim, S. W. Bedell, and D. K. Sadana, Appl. Phys. Lett. **98**, 082112 (2011).
[42] G. Thareja, S.-L. Cheng, T. Kamins, K. Saraswat, and Y. Nishi, IEEE Electron Device Lett. **32**, 608 (2011).
[43] H. Miyoshi, T. Ueno, K. Akiyama, Y. Hirota, and T. Kaitsuka, in: IEEE Symp. on VLSI Technology, Dig. of Tech. Papers (IEEE, New York, 2014), p. 1.
[44] H. Miyoshi, T. Ueno, Y. Hirota, J. Yamanaka, K. Arimoto, K. Nakagawa, and T. Kaitsuka, Jpn. J. Appl. Phys. **53**, 04EA05 (2014).
[45] Z. Li, X. An, M. Li, Q. Yun, M. Lin, M. Li, X. Zhang, and R. Huang, IEEE Electron Device Lett. **34**, 596 (2013).
[46] J. Liu, J. Luo, E. Simoen, G. L. Wang, N. Y. Duan, W. W. Wang, D. P. Chen, J. F. Li, C. Zhao, and T. C. Ye, ECS J. Solid State Sci. Technol. **5**, 315 (2016).
[47] S. Mirabella, D. De Salvador, E. Napolitani, E. Bruno, and F. Priolo, J. Appl. Phys. **113**, 031101 (2013).
[48] G. G. Scapellatto, S. Boninelli, E. Napolitani, E. Bruno, A. J. Smith, S. Mirabella, M. Mastromatteo, D. De Salvador, R. Gwilliam, C. Spinella, A. Carnera, and F. Priolo, Phys. Rev. B **84**, 024104 (2011).
[49] C. H, Lee, T. Nishimura, T. Tabata, C. Lu, W. F. Zhang, K. Nagashio, and A. Toriumi, in: Tech Dig. Int. Electron Devices Meeting, IEDM'13, p. 32 (2013).
[50] A. Toriumi, C.-H. Lee, and T. Nishimura, ECS Trans. **69**, 287 (2015).
[51] Y. Kawamura, Y. Shimizu, H. Oshikawa, M. Uematsu, E. E. Haller, and K. M. Itoh, Physica B **404**, 4546 (2009).
[52] E. Napolitani, E. Bruno, G. Bisognin, M. Mastromatteo, D. De Salvador, G. G. Scapellato, S. Boninelli, F. Priolo, V. Privitera, and A. Carnera, Phys. Status Solidi A **211**, 118 (2014).
[53] D. P. Hickey, Z. L. Bryan, K. S. Jones, R. G. Elliman, and E. E. Haller, Appl. Phys. Lett. **90**, 132114 (2007).
[54] D. P. Hickey, Z. L. Bryan, K. S. Jones, R. G. Elliman, and E. E. Haller, J. Vac. Sci. Technol. B **26**, 425 (2008).
[55] F. Panciera, P. F. Fazzini, M. Collet, J. Boucher, E. Bedel, and F. Cristiano, Appl. Phys. Lett. **97**, 012105 (2010).
[56] S. Boninelli, G. Impellizzeri, A. Alberti, F. Priolo, F. Cristiano, and C. Spinella, Appl. Phys. Lett. **101**, 162103 (2012).
[57] N. Ioannou, D. Skarlatos, C. Tasmis, C. A. Krontiras, S. N. Georga, A. Christofi, and D. S. McPhail, Appl. Phys. Lett. **93**, 101910 (2008).
[58] Z. Li, X. An, Q. Yun, M. Lin, M. Li, M. Li, X. Zhang, and R. Huang, IEEE Electron Device Lett. **34**, 1097 (2013).
[59] M. Koike, Y. Kamimuta, E. Kurosawa, and T. Tezuka, Appl. Phys. Express **7**, 051302 (2014).
[60] R. Duffy, M. Shayesteh, B. McCarthy, A. Blake, M. White, J. Scully, R. Yu, A.-M. Kelleher, M. Schmidt, N. Petkov, L. Pelaz, and L. A. Marqués, Appl. Phys. Lett. **99**, 131910 (2011).
[61] B. Wood, F. Khaja, B. Colombeau, S. Sun, A. Waite, M. Jin, H. Chen, O. Chan, T. Thanigaivelan, N. Pradhan, H.-J. Gossmann, S. Sharma, V. Chavva, M.-P. Cai, M. Okazaki, S. Munnangi, C.-N. Ni, W. Suen, C.-P. Chang, A. Mayur, N. Variam, and A. Brand, ECS Trans. **58**, 249 (2013).
[62] V. R. D'Costa, L. Wang, W. Wang, S. L. Lim, T. K. Chan, L. H. Chua, T. Henry, W. Zou, C. Hatem, T. Osipowicz, E. S. Tok, and Y.-C. Yeo, Appl. Phys. Lett. **105**, 122108 (2014).
[63] H. Murakami, S. Hamada, T. Ono, K. Hashimoto, A. Ohta, H. Hanafusa, S. Higashi, and S. Miyazaki, ECS Trans. **64**, 423 (2014).
[64] A. Renau, in: Proc. IEEE Workshop on Junction Technology (IEEE, New York, 2010), p. 1.
[65] B. Colombeau, B. Guo, H.-J. Gossmann, F. Khaja, N. Pradhan, A. Waite, K. V. Rao, C. Thomidis, K.-H. Shim, T. Henry, and N. Variam, Phys. Status Solidi A **211**, 101 (2014).
[66] P. Bhatt, P. Swarnkar, A. Misra, J. Biswas, C. Hatem, A. Nainani, and S. Lodha, IEEE Trans. Electron Devices **62**, 69 (2015).

[67] H. Bracht, S. Schneider, J. N. Klug, C. Y. Liao, J. Lundsgaard Hansen, E. E. Haller, A. Nylandsted Larsen, D. Bougeard, M. Posselt, and C. Wündisch, Phys. Rev. Lett. **103**, 255501 (2009).
[68] S. Schneider and H. Bracht, Appl. Phys. Lett. **98**, 014101 (2011).
[69] E. Simoen, A. Brugère, A. Satta, A. Firrincieli, B. Van Daele, B. Brijs, O. Richard, J. Geypen, M. Meuris, and W. Vandervorst, J. Appl. Phys. **105**, 093538 (2009).
[70] R. Duffy, M. Shayesteh, M. White, J. Kearney, and A.-M. Kelleher, Appl. Phys. Let. **96**, 231909 (2010).
[71] C. Wündisch, M. Posselt, B. Schmidt, V. Heera, T. Schumann, A. Müklich, R. Grötzschel, W. Skorupa, T. Clarysse, E. Simoen, and H. Hortenbach, Appl. Phys. Lett. **95**, 252107 (2009).
[72] S. Heo, S. Baek, D. Lee, M. Hasan, H. Jung, J. Lee, and H. Hwang, Electrochem. Solid State Lett. **9**, G136 (2006).
[73] P. Tsouroutas, D. Tsoukalas, I. Zergioti, N. Cherkashin, and A. Claverie, Mater. Sci. Semicond. Process. **11**, 372 (2008).
[74] P. Tsouroutas, D. Tsoukalas, I. Zergioti, N. Cherkashin, and A. Claverie, J. Appl. Phys. **105**, 094910 (2009).
[75] E. Bruno, G. G. Scapellato, G. Bisognin, E. Carria, L. Romano, A. Carnera, and F. Priolo, J. Appl. Phys. **108**, 124902 (2010).
[76] G. Thareja, J. Liang, S. Chopra, B. Adams, N. Patil, S.-L. Cheng, A. Nainani, E. Tasyurek, Y. Kim, S. Moffatt, R. Brennan, J. McVittie, T. Kamins, K. Saraswat, and Y. Nishi, in: Tech. Dig. Int. Electron Devices Meeting, IEDM'10 (IEEE, New York, 2010), p. 245.
[77] G. Thareja, S. Chopra, B. Adams, Y. Kim, S. Moffatt, K. Saraswat, and Y. Nishi, IEEE Electron Device Lett. **32**, 838 (2011).
[78] G. Hellings, E. Rosseel, E. Simoen, D. Radisic, D. Hjorth Petersen, O. Hansen, P. Folmer Nielsen, G. Zschätzsch, A. Nazir, T. Clarysse, W. Vandervorst, T. Y. Hoffmann, and K. De Meyer, Electrochem. Solid-State Lett. **14**, H39 (2011).
[79] E. Bruno, G. G. Scapellato, A. La Magna, M. Cuscunà, E. Napolitani, S. Boninelli, F. Priolo, G. Fortunato, and V. Privitera, Appl. Phys. Lett. **101**, 172110 (2012).
[80] R. Milazzo, E. Napolitani, G. Impellizzeri, G. Fisicaro, S. Boninelli, M. Cuscunà, D. De Salvador, M. Mastromatteo, M. Italia, A. La Magna, G. Fortunato, F. Priolo, V. Privitera, and A. Carnera, J. Appl. Phys. **115**, 053501 (2014).
[81] C. Wang, C. Li, S. Huang, W. Lu, G. Yan, M. Zhang, H. Wu, G. Lin, J. Wei, W. Huang, H. Lai, and S. Chen, Appl. Surf. Sci. **300**, 208 (2014).
[82] C. Wang, C. Li, S. Huang, W. Lu, G. Yan, G. Lin, J. Wei, W. Huang, H. Lai, and S. Chen, Appl. Phys. Express **6**, 106501 (2013).
[83] C. Wang, C. Li, G. Lin, W. Lu, J. Wei, W. Huang, H. Lai, S. Chen, Z. Di, and M. Zhang, IEEE Trans. Electron Devices **61**, 3060 (2014).
[84] M. Shayesteh, S. O'Connell, F. Gity, P. Murphy-Armando, R. Yu, K. Huet, I. Toqué-Tresonne, F. Cristiano, S. Boninenelli, H. Hartmann Henrichsen, P. Folmer Nielsen, D. Hjorth Petersen, and R. Duffy, IEEE Trans. Electron Devices **61**, 4047 (2014).
[85] W. B. Chen, C. H. Wu, B. S. Shie, and A. Chin, IEEE Electron Device Lett. **31**, 1184 (2010).
[86] W. B. Chen, B. S. Chie, A. Chin, K. C. Hsu, and C. C. Chi, in: Tech. Dig. Int. Electron Devices Meeting, IEDM'10 (IEEE, New York, 2010), p. 420.
[87] W. B. Chen, B. S. Chie, and A. Chin, IEEE Electron Device Lett. **32**, 449 (2011).
[88] C. Wang, C. Li, G. Lin, W. Lu, J. Wei, W. Huang, H. Lai, S. Chen, Z. Di, and M. Zhang, IEEE Trans. Electron Devices **61**, 3060 (2014).
[89] M. H. Tsai, C.-T. Wu, and W.-H. Lee, Jpn. J. Appl. Phys. **53**, 041302 (2014).
[90] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, in: Tech. Dig. Int. Electron Devices Meeting, IEDM'03 (IEEE, New York, 2003), p. 437.
[91] G. D. Dilliway, R. van den Boom, B. van Daele, F. E. Leys, T. Clarysse, B. Parmentier, A. Moussa, C. Defranoux, A. Benedetti, O. Richard, H. Bender, E. Simoen, and M. Meuris, ECS Trans. **3**, 599 (2006).
[92] J. M. Hartmann, J. P. Barnes, M. Veillerot, J. M. Fédéli, Q. Benoit à la Guillaume, and V. Calvo, J. Cryst. Growth **347**, 37 (2012).
[93] H.-Y. Yu, E. Battal, A. K. Okyay, J. Shim, J.-H. Park, J. W. Baek, and K. C. Saraswat, Current Appl. Phys. **13**, 1060 (2013).
[94] S. Huang, C. Li, C. Chen, C. Wang, G. Yan, H. Lai, and S. Chen, Appl. Phys. Lett. **102**, 182102 (2013).
[95] Y. Moriyama, Y. Kamimuta, Y. Kamata, K. Ikeda, A. Sakai, and T. Tezuka, Appl. Phys. Express **7**, 106501 (2014).
[96] S. H. Huang, F.-L. Lu, W.-L. Huang, C. H. Huang, and C. W. Liu, IEEE Electron Device Lett. **36**, 1114 (2015).
[97] Y. Yamamoto, P. Zaumseil, J. Murota, and B. Tillack, ECS J. Solid State Sci. Technol. **3**, 1 (2014).
[98] G. Scappucci, O. Warschkow, G. Capellini, W. M. Klesse, D. R. McKenzie, and M. Y. Simmons, Phys. Rev. Lett. **109**, 076101 (2012).
[99] W. M. Klesse, G. Scappucci, G. Capellini, J. M. Hartmann, and M. Y. Simmons, Appl. Phys. Lett. **102**, 151103 (2013).
[100] G. Scappucci, G. Capellini, W. M. Klesse, and M. Y. Simmons, Nanoscale **5**, 2600 (2013).
[101] Y. Yamamoto, R. Kurps, C. Mai, I. Costina, J. Murota, and B. Tillack, Solid-State Electron. **83**, 25 (2013).
[102] Y. Cai, R. Camacho-Aguilera, J. T. Bessette, L. C. Kimerling, and J. Michel, J. Appl. Phys. **112**, 034509 (2012).
[103] W.-H. Tu, S.-H. Hsu, and C.-W. Liu, IEEE Trans. Electron Devices **61**, 2595 (2014).
[104] K. Morii, T. Iwasaki, R. Nakane, and S. Takagi, IEEE Electron Device Lett. **31**, 1092 (2010).
[105] M. Takenaka, K. Morii, M. Sugiyama, Y. Nakano, and S. Takagi, Jpn. J. Appl. Phys. **50**, 010105 (2011).
[106] M. Oehme, J. Werner, and E. Kasper, J. Cryst. Growth **310**, 4531 (2008).
[107] M. Jamil, J. Mantey, E. U. Onyegam, G. D. Carpenter, E. Tutuc, and S. K. Banerjee, IEEE Electron Device Lett. **32**, 1203 (2011).

