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Correlation between solar cell efficiency and minority carrier lifetime for batch processed multicrystalline Si wafers

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ABSTRACT

Among the key parameters that ultimately control the performance of a solar cell, the "Minority carrier lifetime" plays the most crucial role. In the process chain involved in conversion of a wafer to a solar cell, each process contributes to change in the carrier lifetime. Hence performance of a particular process can be quantified based on the measure of carrier lifetime before and after the specific process. In an industrial production line, measure of carrier lifetime can be used for real time diagnosis. This paper deals with how to model the overall performance of a production line based on minority carrier lifetime of the wafers used to fabricate the cell. We have shown in this paper that the processing of wafers which were segregated based on their minority carrier lifetime results in increase in yield of the production line. Segregated processing also resulted in improvement of electrical performance of the batch processed solar cells.

1. Introduction

People on the shop floor of photovoltaic production lines are pondered with the thought that "If they could predict the electrical output for wafers based on any/all of the specifications like wafer supplier, thickness, resistivity, carrier lifetime, etc." before processing the wafers they could minimize the trail runs and also opt not to run a batch of wafers. The correlation between as-grown silicon material properties and the final solar cell performance is of utmost importance for material selection in solar cell production lines and for process development [1–5]. Among the most critical parameters, which control the performance of a wafer that is converted to a solar cell is the minority carrier lifetime [6,7]. In any production line since the tool sets are fixed the processing sequence itself limits the carrier lifetime of the final cell and also the carrier lifetime itself limits the performance of the solar cells [8]. In order to predict the useage of wafers in the production line the specification of average carrier lifetime for a batch wafers is commonly used by cell manufacturers as a quality specification. A more accurate but time consuming method involves taking into consideration the spatial variation in lifetime on the wafer for quality analysis [9].

The quasi-steady-state photo-conductance (QSSPC) technique estimates the bulk lifetime despite the overwhelming effect of high surface recombination velocity on unpassivated wafers and hence can be used to estimate the deviation in the final performance of the solar cells from wafers with different lifetimes [10]. For multicrystalline silicon, the correlation between the spatially resolved carrier lifetime and the spatially resolved monochromatic solar cell efficiency has been investigated by means of microwave-detected photoconductance decay (MW-PCD) measurements [11]. The comparison of as-grown Si wafers with

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efficiencies calculated from MW-PCD lifetime mappings showed a qualitative agreement, even though quantitative deviations were found.

In the present work we investigate on the correlation between carrier lifetimes of the incoming microcrystalline wafers to the electrical parameters of the solar cells produced from a production line where the same process sequence is undergone by wafers batch after batch. We try to find a quantitative relation between the minority carrier lifetime and the process capability factor of a production line.

2. Theoretical modeling

We first developed a program that was intended to serve as a tool for approximating the electrical performance for a batch of wafers before they undergo any processing. The program takes into account some constants that can change if the wafer source or if the processing equipment or if the process parameters change. The model is based on both theoretical formulas and experimental data acquired from the production line. A program was developed where the minority carrier lifetime (MCL) of a wafer serves as the input quantity and in return the electrical parameters are generated as the output from the program. The kernel of this program is the basic diode (solar cell) equations and formulas [12]. MCL can be used to calculate excess carrier concentration (Δn_{av}) in the cell using equation

$$J_{ph} = q\Delta n_{av} W/\tau_{eff} \quad (1)$$

where J_{ph} is the photocurrent density, q is the electronic charge, Δn_{av} is the average excess carriers generated and W is the thickness of the wafer [1]. The open circuit voltage (V_{oc}) can be calculated if the base/absorber doping concentration is known, using the equation [13]

$$V_{oc} = (kT/q)\ln\{(\Delta n(0)[N_a + \Delta p(0)]/n_i^2\} \quad (2)$$

where kT/q is the thermal voltage=0.026e, N_a is the bulk doping concentration and n_i is the intrinsic carrier concentration. Using open circuit voltage (V_{oc}), fill factor (FF) can be calculated using equation [13]

$$FF = [V_{oc} - (kT/q)\ln\{(q(V_{oc}/kT) + 0.72\}]/[V_{oc} + (kT/q)] \quad (3)$$

From carrier lifetime and thickness, it is also possible to find surface recombination velocity using equation

$$\tau = (W/2S) + (W^2/3D_n) \quad (4)$$

where W is the thickness of wafer, S is the surface recombination velocity (assumed to be equal at both surfaces), D_n is the electron diffusion constant and τ is the MCL [14].

The modeling of the line processes is based on the MCLA. It is assumed that the contribution to MCL from each process is constant. This contribution can be measured in terms of change in MCL by the specific process in the production line. For example, if process results in increase in MCL by 20 μs, then the contribution of process capability is 20 μs in enhancing the cell's overall electrical performance. This contribution can be put as a process capability factor (PCF), which changes only when process parameters are changed. Measuring MCL before and after the process will determine PCF for any process in the line. If change in MCL from whole line is calculated, then this change can be defined as line capability factor (LCF).

Open circuit voltage is the most important parameter is directly related to the MCL. The dependence of V_{oc} and MCL is logarithmic and both are related to each other by the number of the excess carriers generated. Eq. (1) relates MCL and excess carriers generated. If MCL is known, then the excess carriers generated can be calculated assuming the photo-generated current density (J_{ph}) to be constant for AM1.5 spectrum, which depends on some parameters such as thickness, etc. Still the variation in J_{ph} is very less and it can be accurately estimated using available computer programs or published tables and graphs [7]. Eq. (1) gives average excess carriers generated, but Eq. (2) takes excess carriers at junction as input. Both Δn_{av} and $\Delta n(0)$ are equal if surfaces are passivated and minority carrier diffusion length is greater than wafer thickness. When MCL is low, then $\Delta n(0)$ can be approximated as $\Delta n_{av}(W/L_{eff})$. In case of high rear surface recombination velocity, $\Delta n(0) = 2\Delta n_{av}$ is a better approximation [13]. The number of excess carriers at the junction is then substituted into the Eq. (2) for V_{oc} and the value can be estimated. Here, one more assumption is taken $\Delta n(0) = \Delta p(0)$, i.e. number of excess electrons and holes at the junction are equal. Using these theoretical formulas we get theoretical V_{oc}. This voltage is due to the MCL of raw wafers only. Since these wafers are processed in line, line capability factor comes into picture. For basic version of the model this factor is just the extra MCL that is added by the processes. This gives us the predicted V_{oc}. Since this is directly related to the LCF there is significant variation in V_{oc} with fluctuation of the processes.

Efficiency is the most important electrical parameter for the solar cell industry. This is because it incorporates V_{oc}, short circuit current (I_{sc}) and FF

$$Efficiency = \{(V_{oc})(I_{sc})(FF)\}/P_{in} \quad (5)$$

For the basic version of this program, we have assumed two constants which can be changed depending on the process line the program is used to justify: (i) fill factor and (ii) I_{sc}. Once the baseline for a production line is understood these can be changed to improve the accuracy of the program. These assumptions give the linear relation between V_{oc} and efficiency. If actual efficiency vs. V_{oc} is plotted then it is observed that linear trend line gives the best fit for the graph. This shows that assumption is valid. It can be theoretically estimated that for every 1 mV increase in V_{oc}, a 0.024% increase in efficiency will be delivered [3].

Using this model we theoretically studied the effect of lifetime on the efficiency of the cells. We selected the production lines baseline efficiency to first obtain the LCF, i.e. we compared the theoretical value of V_{oc} with the actual value of V_{oc} obtained, to quantify the actual change in carrier lifetime for the wafers because of processing in the production line. Fig. 1 shows the theoretical dependence of efficiency of the solar cells on lifetime of carriers for the raw wafers based on our model. We represent the predicted change in moving over to wafers with higher

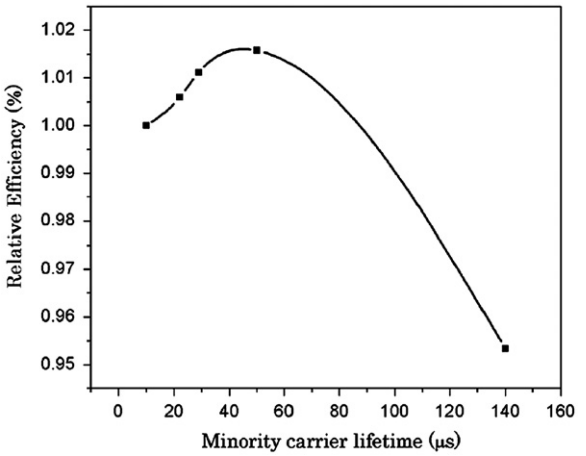

Fig. 1. Theoretical dependence of carrier lifetime on cell efficiency.

carrier lifetime as input wafers compared to the regular production line wafers in Fig. 1. We have assumed that all parameters remain constant and only the carrier lifetime of the incoming raw wafers is varied. As can be seen from Fig. 1 the efficiency increases as the lifetime increases initially, then it saturates and beyond $\sim$60 μs it decreases. Thus it was understood that processing of wafers with higher carrier lifetime would result in improvement of the cell efficiency.

3. Experimental

Experiments were carried out on 125 mm^2 multicrystalline wafers of 180 ± 5 μm thickness. These wafers were boron doped with base resistivity of 0.8 ± 0.3 Ωm. The carrier lifetime for the raw wafers varied from 0.5 μs to 5 μs and the average minority carrier diffusion length was found to be 30 ± 10 μm.

Lifetime measurements on as-grown mc-Si wafers were carried out using a commercially available MW-PCD measurement system from Semilab (WT-2000). In this system the excess carriers are generated by 200 ns light pulses from a 904 nm diode laser (penetration depth is about 30 μm in silicon). A constant injection level is adjusted by means of an additional white bias light of 1/3 suns. This bias light ensures injection conditions in areas of low lifetime which are similar to the injection condition at the maximum power point (MPP) voltage in the solar cell. The transient decay of the laser-excited excess carriers is measured point-by-point by microwave reflection and the lifetime is determined by fitting an exponential to the measured decay curve. Details of the measurement principle can be found in Ref. [15].

A visualization tool to locate losses in a solar cell can be very helpful in troubleshooting a non-optimal production line. Therefore, the Corescan technique has been developed, in which three different methods are incorporated, the Corescan, Shuntscan and the V_{oc} scan [16]. In the V_{oc} scan method a potential probe centered in a light beam is scanned over the front surface of a cell without front side metallization, while the cell is in open circuit condition. The metallization has to be omitted to avoid smearing out of the potential. With the V_{oc} scan, a kind of local V_{oc} is measured, although the values measured can be considerably lower than for uniform illumination [17,18]. Wafers from different batches were subjected to V_{oc} scan to make a qualitative diagnosis of the processed wafers.

Light-beam-induced-current (LBIC) measurements provide a direct link between the spatial non-uniformities inherent in the solar cells, and the overall performance of these cells [19]. Based on the LBIC measurements several types of effects that alter cell performance can be traced to specific local-area features. The most common LBIC features are local optical blockages that reduce the photocurrent over small, well-defined areas. The second major category of LBIC features is a leakage path, which could be either a filamentary shunt or a weak diode. The latter tends to be very bias dependent. In either case, the actual flaw can be very small, but the photocurrent reduction will spread over a much larger area [20,21]. LBIC measurements with 3 laser LBIC head (982, 948 and 887 nm) was performed on the solar cells in the present work. The lateral resolution for the measurement was 0.25 mm. The LBIC-DL maps provide a map of diffusion length over the surface of the solar cells. The passivation of the surface and upper part of the bulk are represented by averaging the response for the three wavelengths used for the study. We have also investigated the internal quantum efficiency (IQE) of the cells using the LBIC measurement at 982 nm.

4. Results and discussion

4.1. Ingot performance based on minority carrier lifetime (MCL)

This experiment was carried out to identify the way MCL changes from ingot to ingot and in turn how it affects solar cell efficiency. This helped us to compare different ingots before any processing of wafers. Wafers from two ingots were selected randomly from the lot of wafers. The wafers were divided into two batches with each batch having wafers from a single ingot. The average lifetime of the carriers in the two ingots compared varied by $\sim$1.5 μs. Fig. 2 compares the performance of wafers from two ingots processed in the same production line. In the figure T7 represent cells with efficiency $>16\%$ and cells in the T2 grade are considered as rejected cells. The ingot with higher average MCL had more number of cells with higher efficiency. Thus it could be concluded that ingot to ingot variation was playing a crucial role in determining the individual cell efficiency and the efficiency of the production line as a whole [22–24]. Table 1 represents the difference in the electrical parameters for solar cells manufactured using wafers from the two ingots.

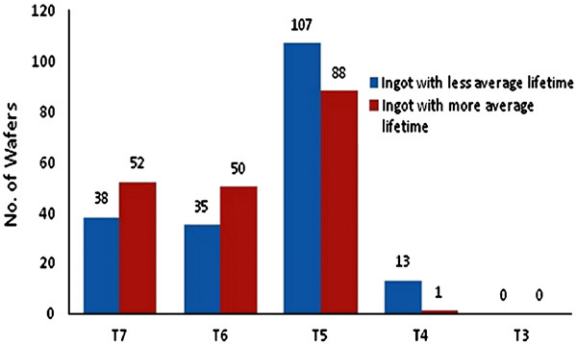

Fig. 2. Efficiency distribution for wafers from two different ingots.

Table 1
Difference in the electrical parameters for solar cells manufactured using wafers from two ingots having different average carrier lifetimes.

Electrical parameters	Difference in the electrical parameters of the cells from two different ingots
ΔEff (%)	0.23
ΔV_{oc} (V)	0.002
ΔI_{sc} (A)	0.01
ΔFF (%)	0.74
ΔR_s (Ω)	0.001
ΔR_{sh} (Ω)	**−23.358**

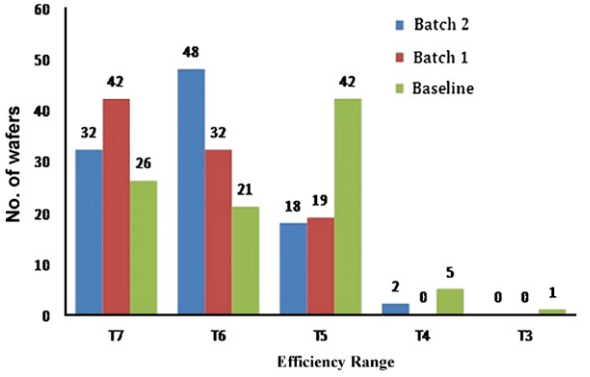

Fig. 3. Efficiency distribution of wafers from same ingot with different average lifetime.

Table 2
Difference in electrical parameters of the trail batches with respect to the baseline batch.

Electrical parameters	**Difference in electrical parameters of the Batch 1 cells with respect to baseline Batch 3**	**Difference in electrical parameters of the Batch 2 cells with respect to baseline Batch 3**
Eff (%)	**0.17**	**0.23**
V_{oc} (V)	**0.0015**	**0.0017**
I_{sc} (A)	**0.010**	**0.030**
FF (%)	**0.28**	**0.69**
R_s (Ω)	**−0.001**	**−0.001**
R_{sh} (Ω)	**5.76**	**−16.44**

4.2. *Effect of processing wafers with specific MCL*

In this experiment, a strict control over MCL and thickness was maintained by segregating the incoming wafers from the same ingot and subjecting the wafers to the same processing sequence. Wafers with strict control over thickness (± 2 μm) were taken, and then they were separated into two batches (Batch 1 and Batch 2 each having 100 wafers) where Batch 1 had wafers with an average lifetime of 5.17 ± 1 μs and Batch 2 had wafers with average lifetime 1.75 ± 1 μs. Another batch (Batch 3) containing the same number of wafers was used as the baseline which contained wafers that were not segregated based on their lifetime, i.e. they contained wafers with lifetime varying randomly. Both of the batches (Batch 1 and Batch 2) showed better performance than the baseline batch, which indicated that the sorted wafers were responding better to the process line. The distribution in efficiency grading for the cells from the two batches along with the baseline is shown in Fig. 3. The nomenclature for the cell grades in Fig. 3 are same as that used in Fig. 2. It was observed that for the batch of wafers having larger MCL, the efficiency distribution shifted towards higher grades. Thus it was observed that processing wafers with higher MCL could deliver batches with higher efficiency [24–26]. It was also observed that the batches with higher lifetime had higher fill factor. The comparison of the electrical parameters for the cells of batches 1 and 2 are shown in Table 2 as compared to that of baseline wafers (batch 3).

Fig. 4 shows the diffusion length map for sample solar cells taken from the T7 grade and the T3 grade using the Light Beam Induced Current (LBIC) technique. Fig. 4a shows the LBIC-DL map for the solar cell from the T7 grade. As can be seen from Fig. 4a the average diffusion length was measured to be ~387 μm for T7 grade cells where as for the sample cell from the T3 grade the diffusion length was only ~109 μm (Fig. 4b). The photocurrent is directly proportional to the diffusion length (DL) and hence an improvement in DL would result in improved electrical performance [25–28]. In Fig. 4a and b, the histogram for the distribution of diffusion length measured over the surface of the solar

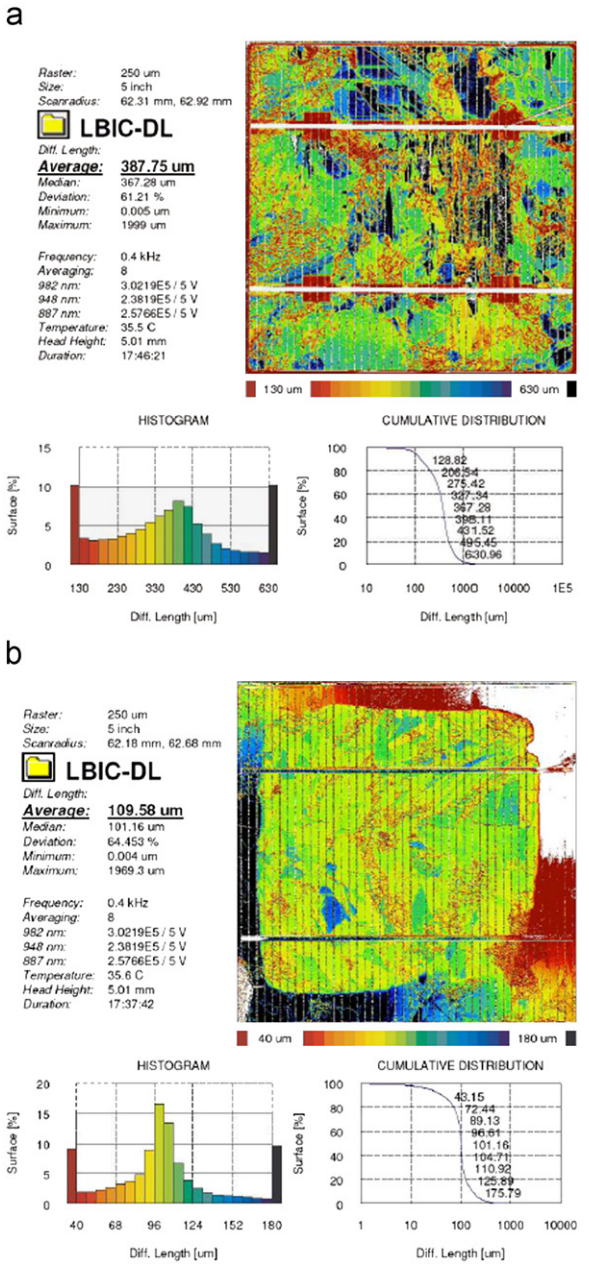

Fig. 4. LBIC-Diffusion length map for (a) solar cell of T7 grade and (b) solar cell of T3 grade.

cells of grade T7 and T3 is also shown. It was observed that for cells with T7 grade the diffusion length varied from 130 to 630 μm where as in the T3 grade cells the diffusion length varied from 40 to 180 μm. Since the diffusion length is directly proportion to the carrier lifetime we could conclude that improvement in lifetime of the carriers resulted in improved electrical performance of the solar cells.

Fig. 5a and b shows the LBIC –IQE maps measured at 982 nm for the cells from the T7 and T3 grade respectively. The IQE map shows a one-to-one correspondence to the LBIC-DL map. Regions having large diffusion lengths showed very high values of quantum efficiency. For the cells from the T7 grade (Figs. 5a and 4a) regions which had quantum efficiency values in the range >95% had diffusion length of the order of ~630 μm. For the cells from T3 grade (Figs. 5b and 4b) maximum quantum efficiency values in the range >10% was observed at certain regions which had a diffusion length of the order of ~70 μm only. Thus it could be concluded that passivation of the wafers was playing the major role in determining the ultimate performance of the solar cells [29].

Fig. 6 shows the V_{oc} mapping done using the correscan technique on wafers from the two batches (Batch 1 and 2) after SiN coating [17,18]. As can be seen the wafer from batch 2 (Fig. 6a) has higher V_{oc} compared to the wafer from the batch 1 (Fig. 6b). The V_{oc} map shows that there is homogeneity in junction formation for cells from both of the batches. Larger magnitude of minority carrier lifetime results in improvement in the open circuit voltage [30–32].

The life line of most production lines are fed by the critical parameter called the "yield" which in simplest reference would represent the ratio of the number of wafers processed to the number of useable solar cells fabricated from these wafers. In the batches with segregated wafers an average increase in yield of 3% was observed with respect to the baseline. Fig. 7 shows the comparison in yield for Batch 1, 2 and the baseline. In these trial batches (Batch 1 and 2) the electrical fails were lower than the baseline which was the main reason for the yield improved. The increase in electrical performance could also be ascribed to the line process recipe responding better to the narrow band of wafer spec because of batch processing at some process stations.

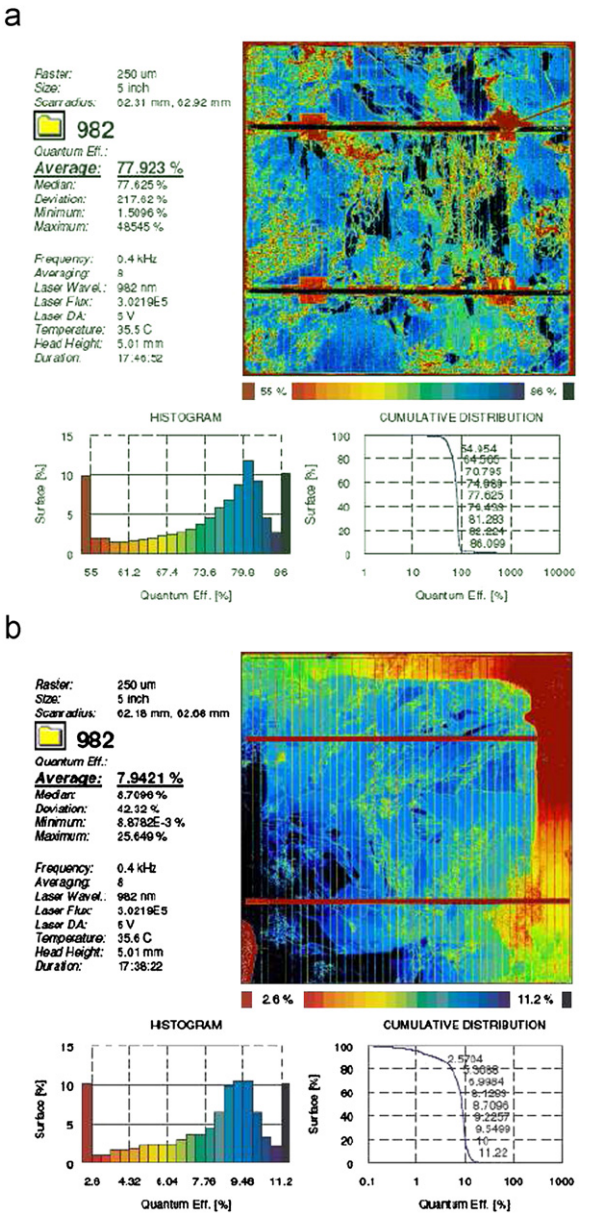

Fig. 5. Histogram representing surface distribution of diffusion length over (a) solar cell of T7 grade and (b) solar cell of T3 grade.

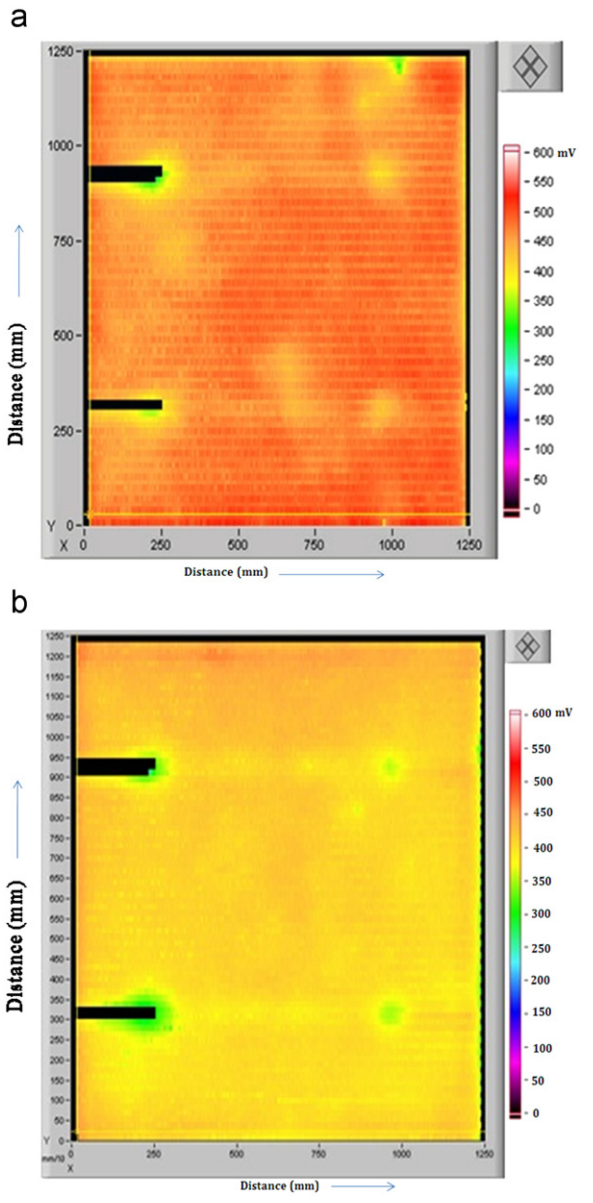

Fig. 6. V_{oc} map for wafer from (a) Batch 2 and (b) Batch 1.

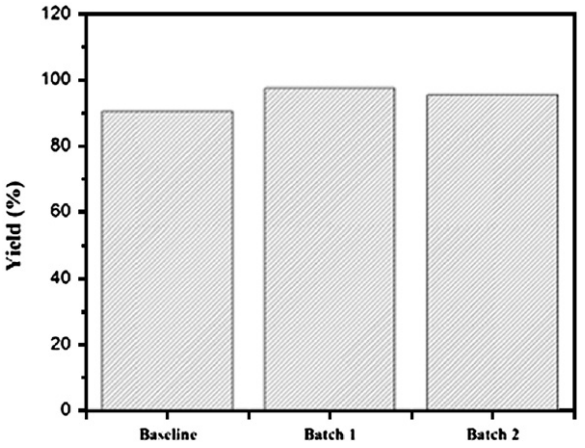

Fig. 7. Process yield for the trial batches and the baseline.

5. Conclusions

We thus conclude that segregation of wafers based on their lifetime and limiting them to a very narrow band could be used to improve the cell efficiency and line yields in photovoltaic production lines. Since minority carrier lifetime can be measured at any stage during the process sequence of converting the wafer to a solar cell, this transport property can be exploited in production line for real time performance monitoring. Minority carrier lifetime of raw wafers can be used to predict performance of the solar cells if the processing steps are known. This performance prediction can be further used to reject the wafers whose performance is below the critical limit, which can save time and cost of processing these wafers. We have demonstrated that processing of wafers after subjecting them to segregation based on minority carrier lifetime results in improvement of yield (number of wafers converted into useful solar cells) of the batch of wafers. Production lines equipped with tools that can manage real time segregation hold the future in the race for more efficient cell lines.

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