Phys. Status Solidi C **13**, No. 10–12, 718–723 (2016) / **DOI** 10.1002/pssc.201600018

physica status solidi c
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Comparison between Si/SiO_2 mid-gap interface states and deep levels associated with silicon-oxygen superlattices in p-type silicon

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Received 19 April 2016, revised 10 May 2016, accepted 10 May 2016
Published online 18 May 2016

Keywords interface states, silicon, dangling bonds, silicon-oxygen superlattice, deep level transient spectroscopy.

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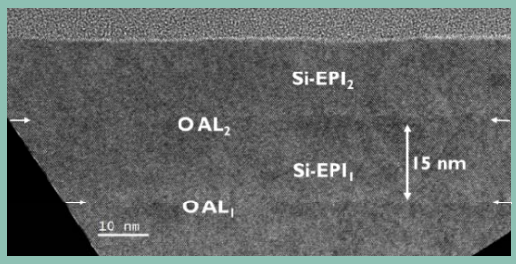
In this paper, the deep levels found by deep-level transient spectroscopy in Si-O superlattices on p-type silicon substrates are compared with the band of near mid-gap hole traps typically observed at the Si/SiO_2 interface. In addition, the impact of a post-deposition Forming Gas Annealing is investigated. A large similarity between the two material systems is reported, which indicates that similar silicon-oxygen bonds may be responsible for the deep hole traps.



TEM cross section of a two layer Si-O superlattice on a p-type silicon substrate.

1 Introduction

The Si/SiO_2 interface is by far the most studied, considering its huge technological importance. Especially the electrically active surface states have been intensively investigated by different techniques, like charge-pumping or deep-level transient apectroscopy [1-4]. In the case of an unpassivated interface, the well-known dangling-bond or P_b centers give rise to two peaks in DLTS: a donor band in p-type silicon centered at 0.28 eV above the valence band and an acceptor band at a symmetrical position with respect to the bottom of the conduction band E_C, i.e., at E_C-0.3 eV [1-4]. The P_b donor band is illustrated in Fig. 1 for the case of a 5 nm thermal oxide on a p-type Czochralski (Cz) silicon substrate. Additionally, as shown in Fig. 1, quite often, a band of hole traps near the middle of the gap is associated with the p-Si/SiO_2 interface [5-7]. These deep levels can at least partly be passivated by a forming gas anneal (FGA) [7]. However, their origin is as yet unclear and deserves further study.

The aim of the present work is to shed some light on this unidentified band of mid-gap states at the Si/SiO_2 interface by performing a detailed DLTS analysis of p-type epitaxial silicon samples containing silicon-oxygen superlattice (SL) layers with a different number of periods, deposited by chemical vapour deposition [8, 9]. Such structures are of interest for possible high-mobility channel applications [10]. As will be shown, in the metal-oxide-semiconductor (MOS) capacitors with a SL layer, a broad band of states is found around the middle of the band gap, which behaves similar like the mid-gap Si/SiO_2 states reported before [5-7]. The density-of-states increases roughly proportional with the number of SL periods and reduces significantly after FGA at 400 °C or 500 °C. Occasionally, the P_b donor has also been observed in the DLT-spectra. Finally, the observed deep levels will be discussed in terms of possible Si-O bonding configurations.

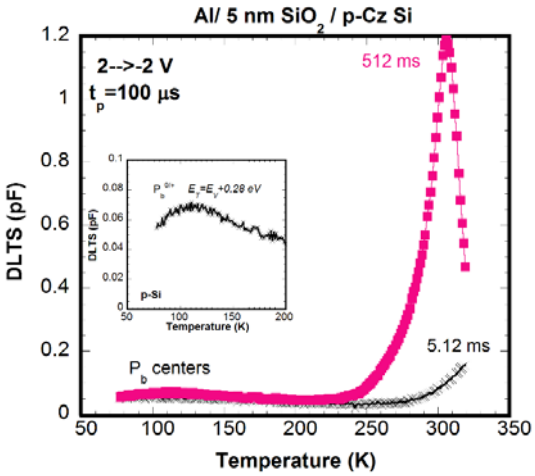


Figure 1 DLT-spectrum of an Al/SiO_2/p-Cz Si MOS capacitor with 5 nm thermal SiO_2 as a gate dielectric. A bias pulse from depletion to accumulation, i.e., 2 V to -2 V has been applied to fill the hole traps. The pulse duration was 100 µs, with a sampling period of 512 ms (red curve) or 5.12 ms (black curve). The inset shows a blow up of the peak around 120 K, associated with the silicon dangling bond donor state at the p-Si/SiO_2 interface.

2 Experimental details DLTS has been performed on MOS capacitors fabricated on p-type Cz silicon substrates. The structure of the Si-O SL samples is shown in Fig. 2, whereby the gate stack consists of 1 nm SiO_2 and 4 nm of Al_2O_3 formed by atomic layer deposition (ALD) at 300 °C using trimethyl aluminium (TMA) and H_2O chemistry. Details of the Si-O SL growth by combined chemical vapour deposition (CVD) of the 3 nm silicon layers and O_3 exposure for the oxygen (sub)monolayers have been described before [8, 9]. Samples with 0, 2 and 5 periods have been investigated. The 0 SL sample is a reference with an 11 nm CVD silicon epi layer, grown at 500 °C using SiH_4. Before epi, an *ex situ* HF/H_2O wet etch and an 850 °C pre-epi bake in 40 Torr H_2 is performed. Further details on the SL growth and characterization can be found elsewhere [8, 9].

Additional capacitors have been prepared on thermally oxidized p-type Cz silicon and on 5 nm Al_2O_3 deposited on p-Si by ALD at 200 °C with H_2O as oxygen precursor and TMA as aluminium precursor, using Al as gate metal [7]. It is known from X-ray photo-electron (XPS) spectroscopy that the deposition of Al_2O_3 on p-Si results in a thin interfacial SiO_2 layer, so that the actual gate stack is Al/Al_2O_3/SiO_2/p-Si. Both for the references and the Si-O SL capacitors post-deposition forming gas annealing (FGA) (10% H_2 in N_2) has been applied at various temperatures in the range 300 to 500 °C.

DLTS has been performed on 500 µm diameter capacitors, biasing the gate electrode from depletion to accumulation in order to fill the traps with holes. Both isothermal frequency and temperature scans (75 K-320 K range) have been applied, using in most cases a saturating pulse duration t_p, i.e., a pulse duration filling all the hole traps in the spatial observation window selected by the reverse bias V_R and the pulse bias V_P. By using different V_P values, one can separate the contribution of traps in the depletion region from those present at the Si/SiO_2 interface (or in the gate stack) [11]. The doping density of the silicon substrate has been derived from the slope of a $1/C^2$ versus V_R plot.

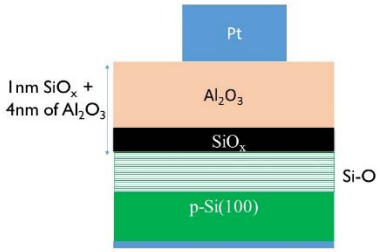


Figure 2 Schematic representation of the MOS capacitors fabricated on the SL samples on p-type Si. A Pt gate electrode was deposited in this case.

3 Results As shown in Fig. 3 for a 2 SL capacitor, a broad peak is obtained typically, which widens for a V_P going more into accumulation. As indicated in the figure, it is believed that the hole traps in the 2.5 V-->0.5 V spectrum predominantly occur in the epi silicon depletion region close to the surface, while, on the contrary, interface states mainly contribute to the broad peaks for the other pulse conditions. The fact that the peak maximum shifts to a higher sampling period in Fig. 3 indicates that deeper hole traps appear in the "interface" spectrum. Based on the filling kinetics as a function of t_p, it has been shown before that the traps behave like point defects, with a saturation of the DLTS amplitude at about 1 µs [12]. This implies that a pulse duration of 1 ms should be more than sufficient to fill all traps in the observation window.

In Fig. 4, a comparison is made of the temperature-scan spectra obtained for a 5 period SL capacitor before (as-deposited) and after FGA. In addition, the results for a p-type silicon epi reference sample are shown as well. It is evident that the insertion of the 5 oxygen atomic layers (ALs) introduces a pronounced peak near room temperature, which is absent in the reference capacitor [12]. Moreover, FGA reduces the hole trap concentration, i.e., the peak amplitude by a factor of two roughly. A more detailed study reveals that not only the amplitude but also the activation energy and the hole capture cross section, derived from an Arrhenius plot at the peak maximum are reduced [12]. Finally, the trap concentration increases with the number of periods (compare Figs. 3 and 4).

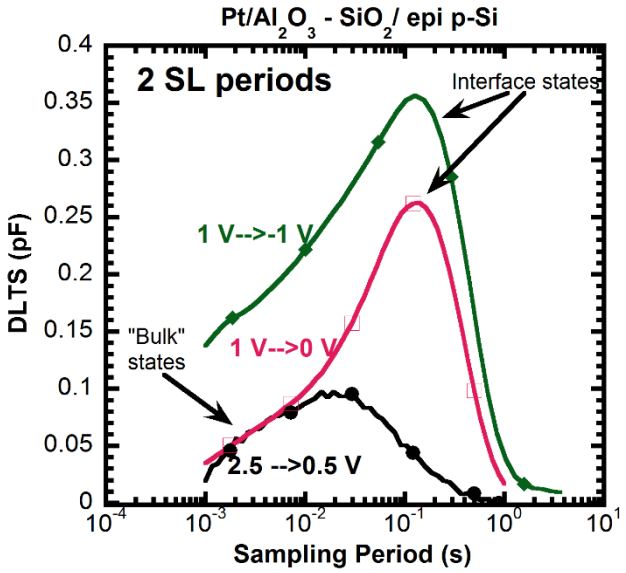


Figure 3 Isothermal DLT-spectra at room temperature for a 2 period SL sample. A fixed pulse duration of 1 ms has been employed, varying its period from about 1 ms to 10 s. Different bias pulses have been used to distinguish bulk-like hole traps from true interface states.

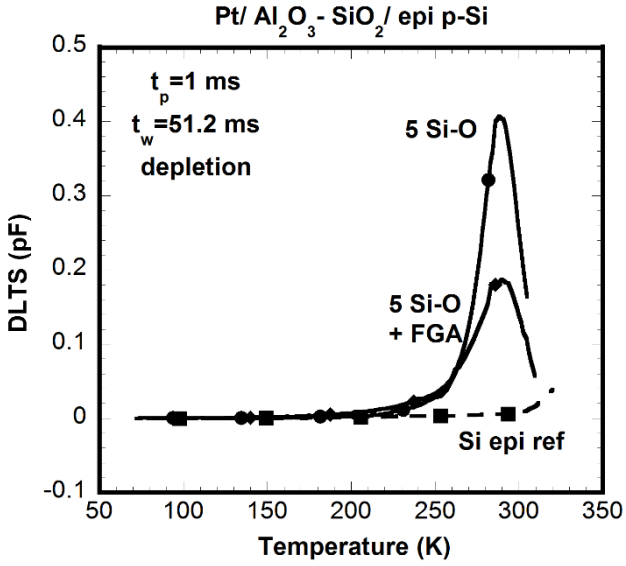


Figure 4 T-scan DLT-spectra at a sampling period t_w=51.2 ms, a pulse duration t_p=1 ms and a bias pulse in depletion, comparing an as-deposited 5 period SL capacitor with a Si epi reference and a 5 period sample after FGA at 500 °C for 5 min.

Additionally, in some cases, the donor state of the P_b centre has been observed, for biases pulses emphasizing the detection of interface traps (Fig. 5).

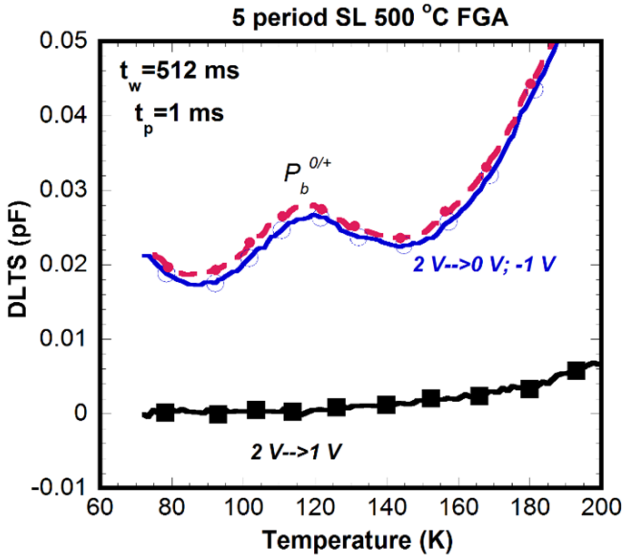


Figure 5 T-scan DLT-spectra of a 5 period SL capacitor after FGA. A t_w=512 ms and t_p=1 ms has been employed and various bias pulses. For a pulse from 2 V--> 0 V or -1 V, the presence of dangling bond donors at the Si/SiO_2 interface is observed.

4 Discussion Comparing Fig. 1 with Fig. 4, it is evident that similar DLT-spectra are obtained for an Si/SiO_2 and a 5 period Si-O SL capacitor, corresponding with a mid-gap band of hole traps. This is shown in more detail in Fig. 6, representing the density-of-states (DOS) versus the activation energy E_T-E_V (E_T: trap energy level; E_V: valence band maximum). The energy scale has been derived from

$$E_T = E_V + kTln\left(\sigma_p \times 3.33\times 10^{21} T^2 \tau_0\right) \text{ (p-Si)}, \qquad (1)$$

assuming a fixed hole capture cross section σ_p=1×10^{-15} cm^2, while τ_0 is the hole emission time constant corresponding with the isothermal measurement. In addition, kT is the thermal energy with k being the Boltzmann constant and T the temperature. The DOS is calculated from the DLTS amplitude, as described previously [6, 12]. It is also clear from Fig. 6 that FGA at 350 °C for 30 min drastically reduces the DOS and at the same time shifts the distribution toward a more mid-gap position. A qualitatively similar behavior has been noted recently for the hole traps in Si-O SL capacitors [12]. This indicates that at least part of the mid-gap hole traps at the interface (or at the Si-O layers) can be passivated, like the P_b centers. In addition, similar spectra have been obtained on "Al_2O_3" capacitors on p-Si (Fig. 7), exhibiting similar changes upon a FGA [7].

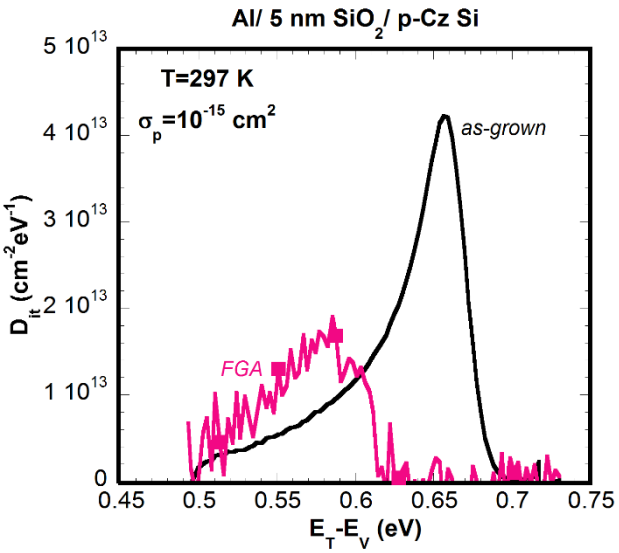


Figure 6 DOS versus activation energy derived from the DLT-spectrum for a 5 nm SiO_2 MOS capacitor at room temperature, assuming a fixed hole capture cross section of 1×10^{-15} cm^2. Spectra before and after a FGA are represented.

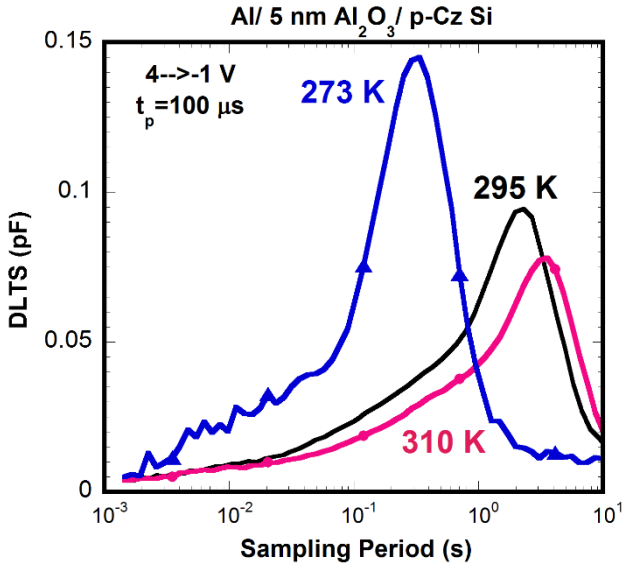


Figure 7 Isothermal DLT-spectra for a 5 nm Al_2O_3 capacitor on p-type Cz Si at three different temperatures. A pulse from 4 V to -1 V was applied for 100 µs.

From this, we conclude that besides the well-known P_b centres, there appears to exist a second type of states, behaving as hole traps and with activation energy at or even above mid-gap, which are typical for the Si/SiO_2 interface. As such, the Si-O SL can be considered as a stacking of internal Si-O interfaces, with similar types of bonding configurations between silicon and oxygen [9].

Of course, we cannot completely neglect the possibility that the near mid-gap peaks are related to so-called "generation transients" in a MOS capacitor, which occur after the application of a pulse from deep depletion into accumulation [13, 14]. Minority carrier generation by deep levels at the interface or in the depletion region plus carrier diffusion from the neutral substrate will give rise to a capacitance increase by the build-up of an inversion layer after the pulse. It has, for example, been suggested that the up-going trace around 300 K for the epi reference sample in Fig. 4 can be ascribed to the generation transient [12]. This transient translates into a mid-gap peak in DLTS and is also used as the basic signal for generation lifetime measurements on a MOS capacitor, the so-called Zerbst technique. Therefore, measurements have also been performed on Schottky barriers (SBs), directly deposited on the SL layer. In principle, this should yield spectra which are less sensitive to interface states and do not exhibit generation transients. As will be shown in detail elsewhere, similar deep-level bands have been detected in the SB samples, ruling out the assignment of the mid-gap hole traps to minority carrier generation in the p-type substrates.

Another possible source of deep levels in the case of the SL samples can be the CVD deposition of Si epi layers on a p-type Cz substrate. As CVD is performed at rather low temperatures, one can expect some incorporation of a non-equilibrium density of native point defects, i.e., vacancies and self-interstitials. Most DLTS studies on silicon epi layers in the past are concerned with as-deposited n-type silicon [15-17], while for p-Si, a band of minority electron traps in the upper half of the bandgap at E_C-0.3 eV has been reported, corresponding with the Si-Si interface [18]. This was confirmed on *in situ* B-doped p^+ epi layers deposited on n-type Cz Si substrates by CVD [19, 20]. The observed majority electron traps have been ascribed to the presence of oxygen and/or carbon at the interface, due to insufficient pre-epi cleaning. However, it is clear from the DLT-spectrum for the epi reference sample in Fig. 4 that the combined *ex situ* and *in situ* cleaning procedure was adequate to suppress the formation of deep levels in the layer or at the interface with the substrate.

However, another experimental fact to be added in the discussion is represented by Fig. 8, showing spectra for a reference p-Cz Si capacitor with the same stack as the SL samples, however, without epi layer. It is evident that similar deep hole traps as in the case of Fig. 4 or 7 have been obtained. Moreover, FGA yields a significant (order of magnitude) reduction in the trap concentration and a reduction of the peak activation energy and hole capture cross section (Fig. 9). It indicates that the quality of the starting substrate (Cz versus epi) plays a crucial role in the formation of the hole traps and not so much the Si/SiO_2 interface itself. This suggests that the responsible defects reside *inside* the silicon substrate in close vicinity of the interface and not at the interface itself. Anyhow, a more systematic study of the impact of the p-type silicon substrate, combining SiO_2 on floating zone (FZ), Cz and epi material seems necessary to further clarify this point. It could also explain

why the deep hole traps have not been systematically found in the past [1-7].

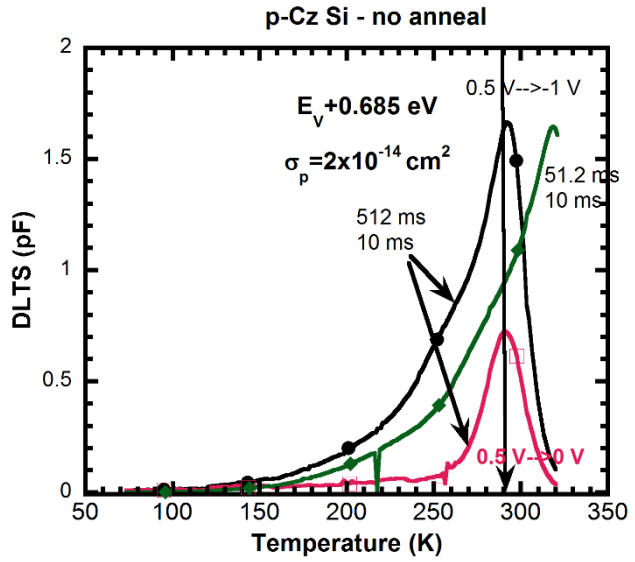


Figure 8 DLT-spectra corresponding with an as-deposited Pt/5 nm Al_2O_3/p-Cz Si capacitor. The activation energy and hole capture cross section derived from an Arrhenius plot in the peak maximum is 0.685 eV and 2×10^{-14} cm^2.

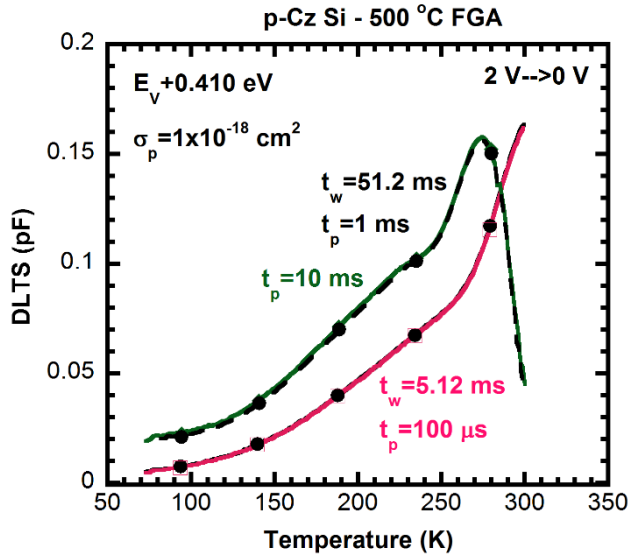


Figure 9 DLT-spectra corresponding with a Pt/5 nm Al_2O_3/p-Cz Si capacitor after 500 °C FGA for 5 min. The activation energy and hole capture cross section derived from an Arrhenius plot in the peak maximum is 0.410 eV and 1×10^{-18} cm^2.

From the foregoing, it is concluded that the implementation of a Si-O superlattice introduces deep hole traps in the layer, which resemble those at the Si/SiO$_2$ interface. At the same time, the deep levels appear to be sensitive to a FGA in the 300-500 °C range. This implies that the fabrication of a MOS capacitor by ALD at 200 °C could somehow modify the intrinsic defect states of the SL layer. DLTS results obtained on SBs indicate that deep-level bands are indeed present in the spectra, but with shallower activation energy. It implies that at least two types of defects can be formed, deeper states which can be easily passivated (or annealed out) by a FGA and less deep hole traps, which remain stable even after a 500 °C heat treatment.

The sensitivity to a heat treatment in the range of 300 to 500 °C points in the direction of so-called oxygen thermal donors (OTDs) as a possible origin of the observed hole traps [21-24]. However, OTDs give rise to double donors in the upper half of the band gap of silicon, while here we are dealing with mid-gap hole traps. In addition, from the negative flat-band voltage shift of the capacitors with and without SL it has been derived that the hole traps behave as positively charged deep donors in the bottom half of the bandgap [12]. At the same time, it has been shown that the capacitors on p-type Si behave like p-type capacitors, i.e., with accumulation for a negative gate voltage, so that it is unlikely that an n-type surface layer is formed by type conversion through a compensation by shallow OTDs.

In summary, it is suspected that some bonding configuration between silicon and oxygen might be responsible for the deep hole traps observed in Si-O superlattices. These can also be present in the vicinity of the Si/SiO$_2$ interface. For the moment, one can only speculate on the exact nature of the defects. Electron paramagnetic resonance (EPR) on similar samples did not reveal any additional features except for the dangling bond centres [25]. This indicates that the mid-gap states are either not paramagnetic or their concentration is below the detection limit of EPR. Alternatively, Recent density functional theory (DFT) calculations have shown that Si-O-Si bridges connecting Si{100} surfaces are likely to form in Si-O superlattices [26]. Other configurations have been suggested before [9, 27], however, without going into detail of the possible electrical activity. Given the technological importance of the Si/SiO$_2$ interface, it is of utmost importance to identify the chemical nature of the deep hole traps reported here.

5 Conclusions It has been shown that in Si-O superlattices fabricated on p-type Cz silicon wafers a band of deep hole traps can be found by DLTS. They resemble strongly similar bands of states observed at the Si/SiO$_2$ interface, suggesting the same origin. In addition, the observed defects are sensitive to a FGA in the 300-500 °C temperature range, whereby the deeper states are largely annihilated or passivated while the shallower states are maintained. This suggests the presence of at least two different types of deep hole traps at the Si/SiO$_2$ and Si-O interface.

Acknowledgements We acknowledge TMEIC (Toshiba-Mitsubishi Industrial Systems Corporation) for providing an O3 generator. We also thank the European Commission for financial support through the 2D Nanolattices Project no. 270749.

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