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Analysis of anomalous transport mechanism across the interface of Ag/*p*-Si Schottky diode in wide temperature range

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ABSTRACT

We have investigated the detailed temperature dependent mechanism across the interface formed in Ag/*p*-Si Schottky diode. The Schottky diodes were fabricated by depositing highly pure silver and aluminum metals on the front and back sides of the boron doped *p*-type semiconductor to form the Schottky and ohmic contacts respectively. The fabricated diode clearly illustrates the rectifying properties between 80 K and 300 K temperature range due to the interface band discontinuity and formation of depleted region. According to thermionic emission diffusion theory the transport mechanisms across the interface reveals abnormal increase in potential barrier and decrease in ideality factor with increase in the temperature due to the potential fluctuations and spatial inhomogeneities at the interface. The inhomogeneities at the interface possess the Gaussian distributions of barrier heights having mean experimental barrier height ($\bar{\phi}_{b0}$), 0.91 eV and standard deviation (σ), 0.11 eV respectively. The mean barrier height ($\bar{\phi}_{b0}$) of 0.93 eV and Richardson,s coefficient (A^{**}) of 2.7×10^5 $Am^{-2}K^{-2}$ were obtained from the modified activation energy plot. The Richardson's constant, 2.7×10^5 $Am^{-2}K^{-2}$ is of the order of known theoretical value of 3.2×10^5 $Am^{-2}K^{-2}$ for *p*-Si. The existence of interface states decreases the capacitance with decrease in the temperature at each applied bias voltage. The higher value obtained for barrier height from $C-V$ analysis in comparison to that $I-V$ analysis is due the existence of tunneling factor and barrier inhomogeneities. The parameters which characterize the interfacial region were also calculated from $C-V$ analysis and found to vary with temperature. The obtained results showed that the fabricated Schottky diode may be a good candidate in the electronic devices.

1. Introduction

The efficiency of integrated circuits and semiconductor devices depends upon the quality of the metal-semiconductor contacts and good ohmic as well as Schottky contacts are necessary for excellent performance of these devices. These diodes are widely utilized in power applications and solar cells due to low turn on voltage, capacitance, and recovery time. The investigation of physical and electrical properties of a semiconductor material and its surfaces can also be performed with help of Schottky contacts. A Schottky junction diode can be obtained when a metal is directly in contact with a semiconductor or by inserting an insulator layer between a metal and semiconductor [1–5]. These diodes show the rectifying properties due the existence of energy barrier as a result of the formation of suitable depletion region at the interface. The suitability of barrier formed at the interface depends upon the choice of

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the metal-semiconductor combination because if the barrier formed is high, the contact will possess high resistance and hence shows the rectifying properties whereas low barrier formed has negligible resistance leading to the non-rectifying behavior of the device. While investigating the traditional semiconductors characteristics, it is necessary to pay special attention to such heterostructure Schottky diodes which improve the ultimate performance of the device. Moreover, the heterojunction effect gets magnified and even become more critical when nanoscale materials are utilized [6]. The heterojunction which shows rectifying characteristics with resistive switching is known as ohmic-Schottky or Schottky-Schottky conjoint whereas which does not show these characteristics known as ohmic-ohmic conjoint [7].

It is impossible to completely understand the nature of the space charge region formed at the metal-semiconductor junction and the transport mechanism across it simply by making observations and analysis only at room temperature alone. Hence the wide temperature range measurements of these devices are absolutely necessary to comprehensively analyze nature of barrier formed and transport mechanism through their interface [8–12]. The current-voltage relationship for the diode exhibits linear behavior up to the certain limit of applied voltages but when the bias voltage increases beyond this limit then diode parameters such as potential barrier, resistance and ideality factor significantly dominate leading to nonlinearity of the current-voltage relationship [13–16].

The inequality in the work functions of metal and semiconductor gives the numerical value of the potential barrier formed at the interface of the Schottky diode. The model with Gaussian distribution of barrier inhomogeneity or the potential fluctuations has successfully explained the current transport across the Schottky barrier [17]. The potential barrier formed at the metal-semiconductor interface, ideality factor and diode's series resistance in the forward bias configuration give the useful information about the electronic properties of these devices [18,19]. The barrier height increases whereas ideality factor decreases on increasing the temperature of the diode and the changes are found to be more and more prominent at low temperatures. The variations of barrier height and ideality factor with temperature result the non-linearity of activation energy plot for the heterojunction diode [20,21]. The Gaussian distribution function can be used to correlate the experimental data of the heterostructures with spatial barrier inhomogeneities [22–29]. The low temperature analysis is essential because the thermal imaging technique for night vision cameras and infrared detectors operating at very low temperatures use the low potential barrier Schottky diodes [30–34]. The low voltage drop in the forward biasing and high switching speed make these diodes of great importance in electronic circuits [35–41].

The $C-V$ analysis provides an important non-destructive way to obtain information about the rectifying properties of the heterostructures. The variation of capacitance with frequency was used to determine the surface states density role in these devices [42]. The flow of electrons through metal-semiconductor junction is enhanced by the factor $\exp(\frac{qV_a}{kT})$ with forward applied voltage V_a . But the experimentally obtained results deviates from this rule therefore investigations to explore the basic mechanism of Schottky barrier formation is absolutely necessary. In the present study Ag/*p*-Si Schottky diode was fabricated and experimentally analyzed in the temperature range varying from 80 K to 300 K to obtain its electrical and interfacial parameters. Frequency dependent $C-V$ analysis has also been performed to extract information about interface state effect or interface trap states.

2. Experimental procedure

Boron doped silicon wafer with resistivity 1–5 Ωcm having (100) surface orientation was used as a substrate to fabricate Ag/*p*-Si Schottky diodes. Before the fabrication process the substrates were cleaned by the means of ultrasonication in organic solvents C_2HCl_3, CH_3COCH_3 and CH_3OH for 10 min at each step then rinsing with deionized water and drying. The oxide layer on the substrate was removed with 40% HF etching solution followed by rinsing and drying again. After cleaning the substrate, it was placed in the chamber of vacuum deposition unit to make the ohmic contact of highly pure aluminum metal under 3×10^{-6} mbar vacuum. The substrate was then annealed for an hour at 300 °C temperature to improve ohmic character. Finally, silver metal was deposited on the polished side of the *p*-Si in circular shape of 1 mm diameter under 3×10^{-6} mbar vacuum to form Ag/*p*-Si Schottky diodes. Block diagram of diode along with measurement system is illustrated in Fig. 1. The work function of Silver metal is smaller than that of the work function of *p*-Si, which is necessary condition for the formation of Schottky contact whose band diagram is shown in Fig. 2 [43,44]. Keithley 2400 source-meter was used to perform $I-V$ measurements. The Lakeshore 331 temperature controller along with helium refrigeration unit was employed to check the temperature of the sample. All the electrical observations were carried out by a microcomputer and IEEE-488 ac/dc interface card. The $C-V$ measurements were carried out with the help of Wayne Kerr 6520A, precision impedance analyzer.

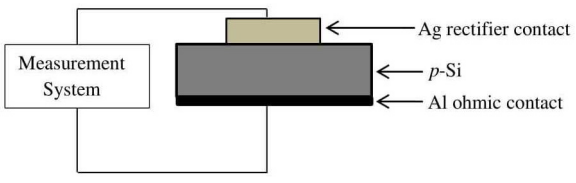

Fig. 1. Block diagram of Ag/*p*-Si Schottky diode.

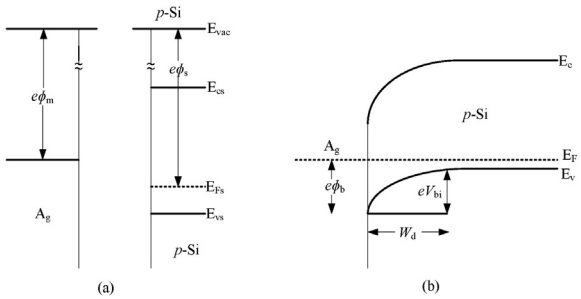

Fig. 2. Band diagram of metal-semiconductor (a) before contact (b) after contact.

3. Results and discussion

3.1. Current-voltage characteristics

Experimental semilogarithmic current of Ag/*p*-Si Schottky diodes having typical junction area 1 mm^2 at various temperatures has been represented in Fig. 3. Reverse and forward biasing of the diode clearly introduces the transport asymmetry indicating excellent rectifying properties between 80 K and 300 K temperature range. The current at fixed positive voltage to negative voltage gives the asymmetry of current transport phenomena i.e. *I(+nV)/I(-nV)*. The positive applied field facilitates the majority charge carries to contribute towards the current transport mechanism whereas negative applied field hinders the contribution of majority charge carriers. Further analysis shows that at room temperature the barriers at interface of diode limit the linear portion of current profile to small bias voltages. When temperature is lowered from 300 K to 80 K, the curves become more and more linear up to the larger biased voltages. Moreover, as the temperature decreases these curves become straight to a larger current range.

The plots are linear in the intermediate forward applied voltages and considerably deviate from linear behavior at higher voltages because of the series resistance and the variations with temperature make it different with respect to conventional diode in which $I-V$ properties are independent of the variations in temperature with forward applied voltages. This was attributed to Richardson's effect where the carriers are driven over the potential barrier at the interface with smaller bias voltages at higher temperature. The leakage current increases hence $I-V$ curves become steeper with increasing temperature because of the decrease in the junction resistance. When the heterojunction is considered with series resistance, the forward current is exponentially related to the forward applied voltage by the thermionic emission equation as:

$$I = I_S \exp\left(\frac{q(V - IR_S)}{\eta kT}\right)\left[1 - \exp\left(\frac{-q(V - IR_S)}{kT}\right)\right], \tag{1}$$

with

$$I_S = A_d A^{**} T^2 \exp\left(\frac{-q\phi_{b0}}{kT}\right), \tag{2}$$

where I_S is saturation current at $V = 0$ in reversed biased diode, q is electron charge, A_d is diode area, A^{**} is Richardson constant whose value is $3.2 \times 10^5 Am^{-2}K^{-2}$ for *p*-type silicon, k is the Boltzmann constant, ϕ_{b0} is the zero-bias barrier height, T is temperature

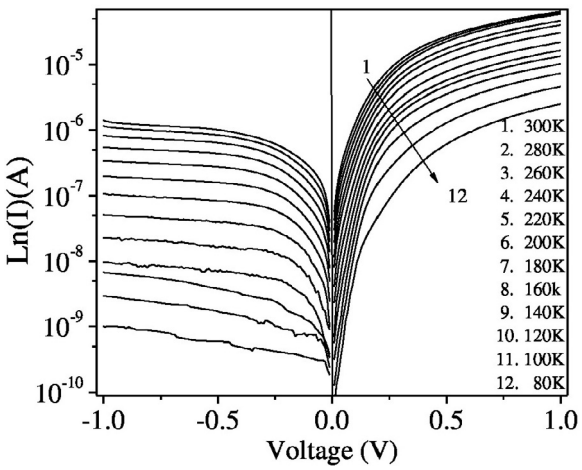

Fig. 3. Current-voltage characteristics of Ag/*p*-Si Schottky diode at different temperatures.

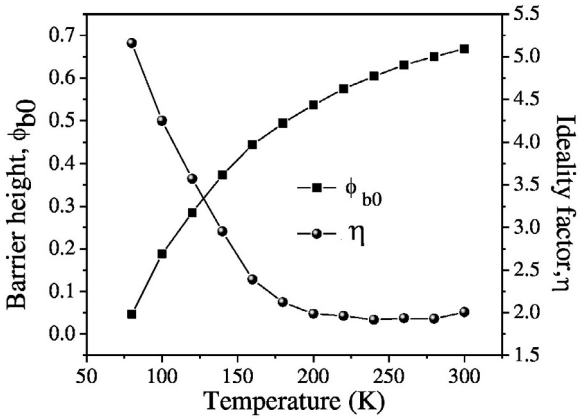

Fig. 4. Barrier height and ideality factor as a function of temperature for Ag/*p*-Si Schottky diode.

in kelvin, η is ideality factor and R_S is series resistance. By extrapolating the ln(I)−V plot to V = 0V i.e. from the intercept point on current axis we can find the value of reverse saturation current (I_S) given in equation (2). The slopes of extrapolated linear segments give the values of ideality factor η at different temperatures. First the value of (I_S) is calculated from equation (1) by employing a MATLAB program then the zero biased barrier height is determined from equation (2) at any required temperature. The barrier height is very sensitive and a key parameter for the analysis of the transport properties across the interface. Fig. 4 illustrates the experimental values of ideality factor and barrier height obtained from the I−V characteristics at different temperatures. The barrier height possesses larger values at higher temperatures as compared to lower temperatures while the ideality factor follows the reverse order to that of barrier height. From Fig. 4 it can be found that the value of barrier height is 0.67 eV at 300 K and 0.05 eV at 80 K while ideality factor has value 2.01 at 300 K and 5.16 at 80 K which shows that both the quantities are strongly dependent on diode temperature. This type of variations in ϕ_{b0} and η with temperature are caused due to the interfacial inhomogeneity in thickness and charges [45]. The current conduction process through the metal-semiconductor interface is activated by the diode temperature so lower barrier patches contribute dominantly in the conduction process because the carriers easily surmount the lower barriers patches at low temperatures resulting in larger ideality factor [23]. With rise in the temperature more and more carries attain the essential required thermal energy to surmount the higher barrier patches, hence the effective barrier height increases. The variations of ideality factor and barrier height clearly confirm that current conduction process deviates from pure thermionic emission theory due to the series resistance of the device. Moreover, image force effect, recombination-generation process and tunneling factor may increase the value of ideality factor.

The Richardson's plot of the reverse saturation current provides another technique to extract the barrier height. The equation (2) after taking the natural logarithmic can be rewritten as

$$\ln\left(\frac{I_S}{T^2}\right) = \ln(A_d A^{**}) - \frac{q\phi_{b0}}{kT} \tag{3}$$

The equation (3) shows that variations $\ln(\frac{I_S}{T^2})$ with inverse of temperature for the diode should be linear between 80 K and 300 K temperature range, whose slope gives the barrier height ϕ_{b0} and intercept provides the values of Richardson constant A^{**}. The

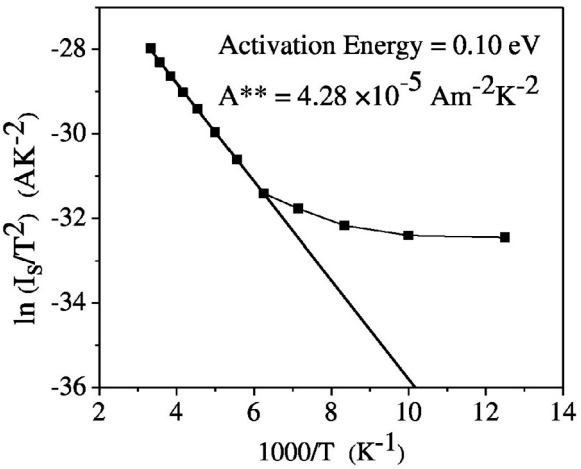

Fig. 5. The activation energy plot of Ag/*p*-Si Schottky diode.

dependence of $\ln(\frac{I_S}{T^2})$ on $\frac{1000}{T}$ as shown in Fig. 5 shows nonlinearity in the considered temperature range. Linear fit to the profile gives mean activation energy 0.10 eV and Richardson constant A^{**} 4.28 × 10^{-5} $Am^{-2}K^{-2}$. The Richardson constant A^{**} obtained from above analysis is found to be much lower as compared to the theoretical calculated value of 3.2 × 10^5 $Am^{-2}K^{-2}$ for *p*-type silicon. Temperature dependence of ϕ_{b0} and the ideality factor leads to the erroneous outcomes from the Rechardson's plot. The deviation in Richardson's plot may be due the presence of defects at the interface such as spatial barrier inhomogeneity and potential fluctuations at the interface that consist of low and high barrier areas [46]. The observed variations in the ideality factor, barrier height with decrease in temperature and deviation of activation energy from linearity at low temperatures indicate the inconsistency of pure thermionic emission mechanism, which demand the requirement of other techniques that facilitates the temperature independent values so that the observed behavior can be understood more precisely with further investigations.

3.2. Analysis of barrier height inhomogeneities

The *I*−*V* properties of the diode can be explained by equation (1) if the spatially inhomogeneous barrier heights or potential fluctuations at metal-semiconductor interface resulting the anomalous behavior of ideality factor, activation energy, Richardson's constant with temperature are modeled by modifying the conventional Richardson's plot assuming Gaussian distribution of barrier heights in the Schottky contact area with mean barrier height $\bar{\phi}_{b0}$ and standard deviation σ [10,33,24,32]. Barrier homogeneity is measured in terms of standard deviation. Therefore, the modified expression for barrier height with Gaussian distributions can be given as:

$$\phi_{ap} = \bar{\phi}_{b0} - \frac{q\sigma^2}{2kT} \tag{4}$$

where ϕ_{ap} is experimentally obtained apparent barrier height. The equation (4) represents a straight line as ϕ_{b0} varies with inverse of temperature whose intercept is $\bar{\phi}_{b0}$ and σ can be calculated from the slope. The value of ϕ_{b0} can be obtained from the fitting the experimental observations in equation (2) and which should consistent with equation (4). The plot between ϕ_{b0} versus 1000/T drawn with help of the data extracted from fig (3) for the Ag/*p*-Si Schottky diode is illustrated in Fig. 6 which is linear and depicts not only the spatial inhomogeneities and potential fluctuations but also the existence barrier heights with Gaussian distributions and standard deviation, σ = 0.11eV. The linear fitting of the plot yields zero biased mean barrier heights 0.91eV. The current conduction in Schottky diode Ag/*p*-Si get changed due the presence of potential fluctuations and barrier heights obeying the Gaussian distributions at the interface. Using equations (3) and (4) the conventional Richardson's plot modifies as:

$$\ln(\frac{I_S}{T^2}) - \frac{q^2\sigma^2}{2k^2T^2} = \ln(A_d A^{**}) - \frac{q\bar{\phi}_{b0}}{kT} \tag{5}$$

According to equation (5) the variations of $\ln(\frac{I_S}{T^2}) - \frac{q^2\sigma^2}{2k^2T^2}$ i.e. the modified activation energy with 1000/T and the original one is shown in Fig. 7. The values of modified $\ln(\frac{I_S}{T^2}) - \frac{q^2\sigma^2}{2k^2T^2}$ are calculated by using the standard deviations obtained from Fig. 6. The standard deviation of 0.11 eV is used in equation (5) for the temperature varying from 80 K to 300 K. Over the whole range of temperature the linear modified Richardson's plot gives single activation energy. The slope and the intercept at the ordinate yield the mean barrier heights $\bar{\phi}_{b0}$ and the Richardson's constant A^{**}. The modified A^{**} and $\bar{\phi}_{b0}$ of 2.7 × 10^5 $Am^{-2}K^{-2}$ and 0.93 eV, respectively are obtained from the best linear fit of the data. Richardson constant is comparable with its theoretical known value of 3.2 × 10^5 $Am^{-2}K^{-2}$ for *p*-type silicon. The mean barrier heights $\bar{\phi}_{b0}$ is higher than that of 0.78 eV found in literature [47] and Richardson's constant closer to its theoretical known value of 3.2 × 10^5 $Am^{-2}K^{-2}$ for *p*-type silicon.

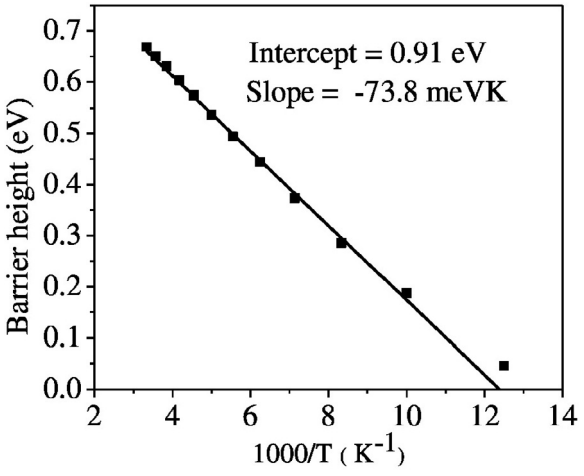

Fig. 6. The apparent barrier height ϕ_{ap} obtained from *I-V* measurements as a function of inverse temperature.

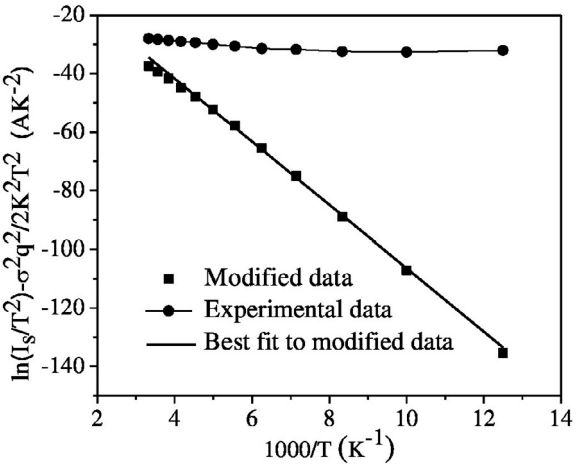

Fig. 7. Modified activation energy plots corresponding to the standard deviation σ = 0.11 V.

The junction capacitance was analyzed in the reverse biased configuration in the wide temperatures range using the following relation [48,49]:

$$\frac{1}{C^2} = \frac{2(V_{bi} + V)}{q\varepsilon_S \varepsilon_0 A_d^2 N_D} \tag{6}$$

where, ε_s, ε_0, N_D and V_{bi} are dielectric constant of silicon, permittivity of free space, equivalent carrier concentration and built-in voltage respectively. Reverse biased C^{-2} $-V$ curves at frequency 1000 kHz for the whole temperature range considered is shown in Fig. 8. As the depletion layer width increases with increase in the reverse applied voltage from 1 to 4 V, the capacitance decreases linearly at each temperature with constant slope indicating the uniform doping. The linear behavior of the profiles is also attributed to the fact that at high frequency ac signals there is no contribution of inversion layer charges as well as of interface states towards the capacitance of the Schottky diode as they cannot able to follow the signal at this frequency.

The straight line C^{-2}-V curves at each temperature, if fitted well, then intercept at $C^{-2} = 0$ provides the value of V_{bi} while from the slope of the profile the N_D was calculated. In the valence band of silicon the effective density of states, N_C can be defined as, $N_C = 4.82 \times 10^{15} T^{3/2} (\frac{m_e^*}{m_0})^{3/2}$with m_0 and m_e^* be the rest and effective mass of the electrons. The obtained temperature dependent values of N_D and N_C are given in Table 1 and found to decrease with decrease in the temperature from 300 K to 80 K. This may be attributed to the fact that at cryogenic temperatures more and more electrons get frozen into the donors at the required levels because of incomplete ionization in the freeze out region. The depletion layer region shrinks with increase in the temperature as given in Table 1. As the temperature increases density of charge carriers increases as a result some carriers get accumulated at the junctions resulting a decrease in the depletion layer width. Maximum value of electric field E_m decreases with increase in temperature as shown in Table 1.

With rise in temperature the effective concentration of intrinsic carriers increases which in turn increases the fermi energy in the diode. The fermi level is close to the conduction band in *n*-type semiconductor and close to the valence band in *p*-type semiconductor and the difference between two gives the built-in-voltage. The fermi level in the doped semiconductor with rise in temperature moves

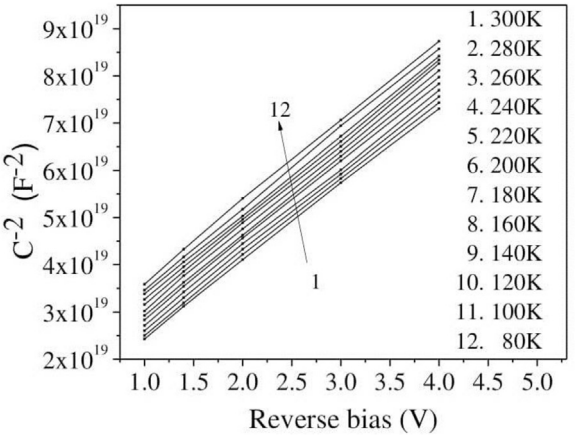

Fig. 8. The $1/C^2$*vs* V characteristics of the Ag/*p*-Si Schottky diode at a frequency of 1 MHz at different temperatures.

Table 1
The values of N_D, V_{bi}, fermi energy E_f, N_C, width of depletion region W_D , electric field E_m, density of interface states N_{SS}, image force lowering $\Delta\phi_b$.

Temperature (K)	$N_D(cm^{-3})$	V_{bi} (eV)	E_f (eV)	$N_C(cm^{-3})$	W_D(cm)	$E_m(Vm^{-1})$	$N_{SS}(eV^{-1}cm^{-2})$	$\Delta\phi_b$(eV)
300	1.25×10^{16}	0.72	0.18	1.02×10^{13}	4.92×10^{-3}	389	8.70×10^{12}	2.18×10^{-4}
280	1.23×10^{16}	0.76	0.17	9.21×10^{12}	5.06×10^{-3}	396	8.04×10^{12}	2.20×10^{-4}
260	1.22×10^{16}	0.79	0.16	8.24×10^{12}	5.18×10^{-3}	402	8.96×10^{12}	2.21×10^{-4}
240	1.22×10^{16}	0.83	0.15	7.31×10^{12}	5.31×10^{-3}	410	8.63×10^{12}	2.24×10^{-4}
220	1.19×10^{16}	0.87	0.14	6.42×10^{12}	5.49×10^{-3}	414	9.70×10^{12}	2.25×10^{-4}
200	1.18×10^{16}	0.92	0.13	5.56×10^{12}	5.68×10^{-3}	424	9.65×10^{12}	2.27×10^{-4}
180	1.15×10^{16}	0.97	0.12	4.75×10^{12}	5.91×10^{-3}	429	8.86×10^{12}	2.29×10^{-4}
160	1.12×10^{16}	1.03	0.11	3.98×10^{12}	6.18×10^{-3}	438	1.03×10^{13}	2.31×10^{-4}
140	1.13×10^{16}	1.09	0.10	3.26×10^{12}	6.32×10^{-3}	454	1.69×10^{13}	2.35×10^{-4}
120	1.12×10^{16}	1.16	0.09	2.58×10^{12}	6.54×10^{-3}	465	1.36×10^{13}	2.38×10^{-4}
100	1.11×10^{16}	1.23	0.08	1.97×10^{12}	6.78×10^{-3}	477	2.73×10^{13}	2.41×10^{-4}
80	1.10×10^{16}	1.30	0.07	1.41×10^{12}	6.99×10^{-3}	488	3.60×10^{13}	2.44×10^{-4}

closer to the intrinsic fermi level hence the built-in voltage decreases as can be seen from Table 1. The restructuring and reordering of interface states with rise in temperature at the semiconductor-metal junction decreases the values of density of interface states N_{SS}. The image force lowering is defined by the relation $\Delta\phi_b = (\frac{qE_m}{4\pi\varepsilon_S\varepsilon_0})^{1/2}$, E_m decreases with temperature hence the value of $\Delta\phi_b$ also.

The plots for junction capacitance at various frequencies and voltages are shown in Fig. 9. The existence of interface states at the semiconductor-metal interface was proved by the frequency dependent $C-V$ curves. The accumulation capacitance is found to decrease with increase in the frequency because interface states do not contribute at higher frequencies and also due to the movement of carriers across the depletion region. The capacitance also decreases with increase in the reverse applied voltage as result of increase in the depletion width. The absolute depletion of the junction barrier is indicated with reverse voltage while it shrinks with the forward voltage [50,51]. The Mott-Schottky plot was summarized in Fig. 10 with help of the data obtained from the $C-V$ analysis at different frequencies. Rectilinear response was found for the inverse of square of capacitance with voltage at 1000 kHz, 500 kHz and 100 kHz of frequency having 4.54×10^{-11} $m^2/(nF)^2V$, 4.43×10^{-11} $m^2/(nF)^2V$ and 4.04×10^{-11} $m^2/(nF)^2V$ of slope values, respectively. The traps and recombination centers in depletion region along with effective surface states increase the slopes with the signal frequency [50,51].

The barrier heights can also be obtained from $C-V$ analysis which is shown in Fig. 11 with built-in-voltage and barrier heights obtained from $I-V$ analysis. The two techniques used to evaluate the barrier height of Ag/p-Si are in disagreement with each other due to different nature. The insulating layer or interface charges, image force lowering effect, bulk traps and leakage currents are responsible for the different barrier heights obtained from the two techniques [52–55]. The inhomogeneities of interfacial layer offer another explanation for it [24,56,57]. The average value of high and low barrier heights patches of the Schottky contact was taken in $C-V$ technique whereas $I-V$ technique is sensitive to image force barrier lowering effect due to the surface density of interface states.

4. Conclusion

Ag/p-Si Schottky barrier diodes were fabricated by depositing pure silver metal on p-type silicon substrate in a clean vacuum coating system. The conduction process shows rectification with respect to forward and reverse biasing, throughout the considered temperature range. The potential barrier and ideality factor illustrate anomalous character with the temperature variation due to the

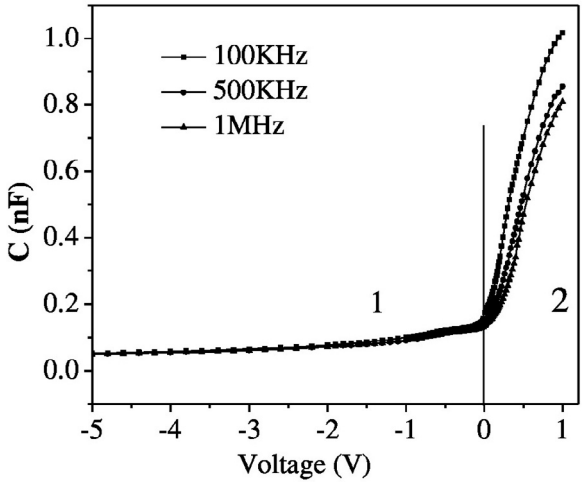

Fig. 9. The $C-V-f$ characteristics of the Ag/p-Si Schottky diode measured at room temperature.

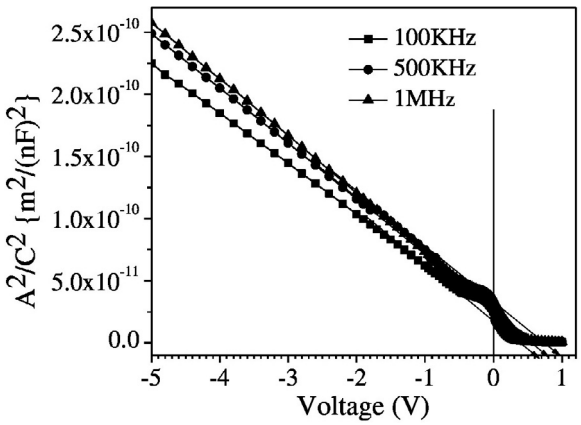

Fig. 10. Mott-Schottky plots of the capacitance-voltage characteristics of the Ag/*p*-Si Schottky diode.

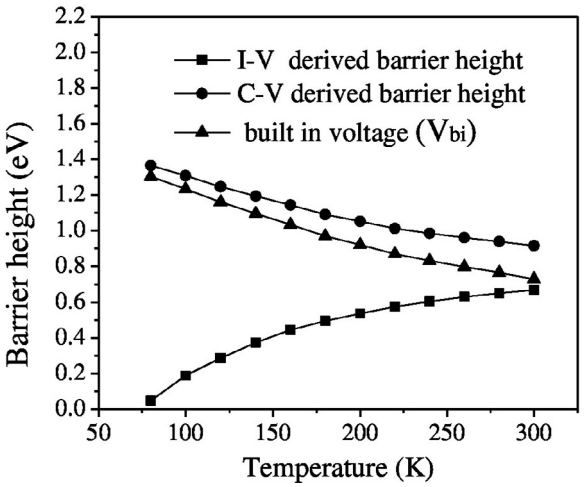

Fig. 11. Barrier height derived from the current-voltage and capacitance-voltage measurements along with built-in voltage for the heterojunction diode at 1 MHz frequency.

inhomogeneities at the metal-semiconductor interface. The inconsistency with the pure thermionic emission theory was proved by the nonlinearity of the activation energy and was removed with the consideration of Gaussian distribution of barriers formed at interface with mean barrier height 0.91 eV and 0.10 V of standard deviation. Linear fit to the conventional Richardson plot gives mean activation energy 0.10 eV and Richardson constant A^{**} 4.28 × 10^{-5} $Am^{-2}K^{-2}$. The theoretical known value of Richardson's constant *p*-type silicon is much higher than this value. Considering the barrier inhomogeneities and its Gaussian distributions, the modified Richardson's plot depicts the rectilinear dependence of activation energy with temperature giving much improved Richardson's constant, 2.7 × 10^5 $Am^{-2}K^{-2}$ and barrier height, 0.93 eV. The insulating layer or interface charges, image force lowering effect, bulk traps and leakage currents are responsible for the different barrier heights obtained from *C*−*V* and *I*−*V* techniques. The accumulation capacitance is found to decrease with increases in the frequency because interface states do not contribute at higher frequencies and due to the movement of carriers across the depletion region. The existence of interface state was also indicated by the Mott-Schottky response. The various interfacial parameters obtained from *C*−*V* analysis shows temperature dependent response.

References

[1] H.C. Card, E.H. Rhoderick, Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes, J. Phys. D Appl. Phys. 4 (1971) 1589–1601.
[2] A. Singh, K.C. Reinhardt, W.A. Anderson, Temperature dependence of the electrical characteristics of Yb/*p*-InP tunnel metal-insulator-semiconductor junctions, J. Appl. Phys. 68 (1990) 3475–3483.
[3] S. Chand, J. Kumar, Current–voltage characteristics and barrier parameters of Pd_2Si/*p*-Si(111) Schottky diodes in a wide temperature range, Semicond. Sci. Technol. 10 (1995) 1680–1688.
[4] I. Dokme, The analysis of I-V characteristics of Schottky diodes by thermionic emission with a Gaussian distribution of barrier height, Microelectron. Reliab. 51 (2011) 360–364.
[5] S. Cetinkaya, H.A. Cetinkara, S. Kahraman, F. Bayansal, Characterization of Al/*n*-ZnO/*p*-Si/Al structure with low-cost solution-grown ZnO layer, Philos. Mag. A 93 (2015) 550–559.

[6] Y.H. Chang, C.M. Liu, C. Chen, H.E. Cheng, The heterojunction effects of TiO_2 nanotubes fabricated by atomic layer deposition on photocarrier transportation direction, Nanoscale Res. Lett. 7 (2012) 231.
[7] E.H. Rodriguez, A.M. Herrera, E.Z. Alejandre, M.M. Lira, W.D.L. Cruz, M.Z. Torres, Effect of electrode type in the resistive switching behaviour of TiO_2 thin films, J. Phys. D Appl. Phys. 46 (2013) 045103.
[8] S. Karatas, S. Altındal, A. Turut, A. Ozmen, Temperature dependence of characteristic parameters of the H-terminated Sn/*p*-Si(1 0 0) Schottky contacts, Appl. Surf. Sci. 217 (2003) 250–260.
[9] S. Altındal, S. Karadeniz, N. Tugluoglu, A. Tataroglu, The role of interface states and series resistance on the I–V and C–V characteristics in Al/SnO_2/*p*-Si Schottky diodes, Solid State Electron. 47 (2003) 1847–1854.
[10] J.H. Werner, H.H. Guttler, Barrier inhomogeneities at Schottky contacts, J. Appl. Phys. 69 (1991) 1522–1533.
[11] S. Zeyrek, S. Altındal, H. Yuzer, M.M. Bulbul, Current transport mechanism in Al/Si_3N_4/*p*-Si (MIS) Schottky barrier diodes at low temperatures, Appl. Surf. Sci. 252 (2006) 2999–3010.
[12] S. Zhu, R.L.V. Meirhaeghe, C. Detavernier, F. Cardon, G.P. Ru, X.P. Qu, B.Z. Li, Barrier height inhomogeneities of epitaxial $CoSi_2$ Schottky contacts on *n*-Si (100) and (111), Solid-State Elecron. 44 (2000) 663–671.
[13] S.M. Sze, Physics of Semiconductor Devices, second ed., Wiley, New York, 1981.
[14] J.H. Werner, Schottky barrier and pn-junction I/V plots- small signal evaluation, Appl. Phys. A 47 (1988) 291–300.
[15] P. Chattopadhyay, Effect of localized states on the current-voltage characteristics of metal-semiconductor contacts with thin interfacial layer, Solid State Electron. 37 (1994) 1759–1762.
[16] P. Cova, A. Singh, Temperature dependence of *I-V* and *C-V* characteristics of Ni/*n*-CdF_2 Schottky barrier type diodes, Solid State Electron. 33 (1990) 11–19.
[17] A. Kumar, K.K. Sharma, R. Kumar, S. chand, A. Kumar, Structural and electrical properties of Ag/*n*-TiO_2/*p*-Si/Al heterostructure fabricated by pulsed laser deposition technique, J. Electron. Mater. 46 (2017) 6422–6429.
[18] R.T. Tung, Recent advances in Schottky barrier concepts, Mater. Sci. Eng. R Rep. 35 (2001) 1–138.
[19] A. Gumus, A. Turut, N. Yalcin, Temperature dependent barrier characteristics of CrNiCo alloy Schottky contacts on *n*-type molecular-beam epitaxy GaAs, J. Appl. Phys. 91 (2002) 245–250.
[20] S. Chand, J. Kumar, Electron transport and barrier inhomogeneities in palladium silicide Schottky diodes, Appl. Phys. A 65 (1997) 497–503.
[21] S. Karatas, S. Altındal, M. Cakar, Current transport in Zn/*p*-Si (1 0 0) Schottky barrier diodes at high temperatures, Physica B 357 (2005) 386–397.
[22] W.J. Monch, Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities, Vac. Sci. Technol. B 17 (1999) 1867–1876.
[23] R.T. Tung, Electron transport at metal-semiconductor interfaces: general theory, Phys. Rev. B 45 (1992) 13509–13523.
[24] Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, On the difference in apparent barrier height as obtained from capacitance-voltage and current-voltage-temperature measurements on Al/*p*-InP Schottky barriers, Solid State Electron. 29 (1986) 633–638.
[25] J. Osvald, Z.J. Horvarth, Theoretical study of the temperature dependence of electrical characteristics of Schottky diodes with an inverse near-surface layer, Appl. Surf. Sci. 234 (2004) 349–354.
[26] H. Cetin, E. Ayyildiz, Temperature dependence of electrical parameters of the Au/*n*-InP Schottky barrier diodes, Semicond. Sci. Technol. 20 (2005) 625–631.
[27] S. Karatas, S. Altındal,, Analysis of I-V characteristics on Au/*n*-type GaAs Schottky structures in wide temperature range, Mater. Sci. Eng. B 122 (2005) 133–139.
[28] Z.J. Horvarth, Comment on "Analysis of I-V measurements on $CrSi_2$Si Schottky structures in a wide temperature range, Solid State Electron. 39 (1996) 176–178.
[29] R.C. Rossi, M.X. Tan, N.S. Lewis, Size-dependent electrical behavior of spatially inhomogeneous barrier height regions on silicon, Appl. Phys. Lett. 77 (2000) 2698–2700.
[30] P.G. McCafferty, A. Sellai, P. Dawson, H. Elabd, Barrier characteristics of PtSi/*p*-Si Schottky diodes as determined from I-V-T measurements, Solid State Electron. 39 (1996) 583–592.
[31] N.L. Dimitruk, O.Y. Borkovskaya, I.N. Dmitruk, S.V. Mamykin, Z.J. Horvath, I.B. Mamontova, Morphology and interfacial properties of microrelief metal-semiconductor interface, Appl. Surf. Sci. 190 (2002) 455–460.
[32] S. Chand, J. Kumar, On the existence of a distribution of barrier heights in Pd_2Si/Si Schottky diodes, J. Appl. Phys. 80 (1996) 288–294.
[33] S. Chand, J. Kumar, Current transport in Pd_2Si/*n*-Si(100) Schottky barrier diodes at low temperatures, Appl. Phys. A 63 (1996) 171–178.
[34] B. Abay, G. Cankaya, H.S. Guder, H. Efeoglu, Y.K. Yogurtcu, Barrier characteristics of Cd/*p*-GaTe Schottky diodes based on I-V-T measurements, Semicond. Sci. Technol. 18 (2003) 75–81.
[35] S. Aydogan, M. Saglam, A. Turut, On the barrier inhomogeneites of polyaniline/*p*-Si/Al structure at low temperature, Appl. Surf. Sci. 250 (2005) 43–49.
[36] M. Biber, O. Gullu, S. Forment, R.L. Van Meirhaeghe, A. Turut, The effect of Schottky metal thickness on barrier height inhomogeneity in identically prepared Au/*n*-GaAs Schottky diodes, Semicond. Sci. Technol. 21 (2006) 1–5.
[37] S. Alialy, A. Kaya, E. Maril, S. Altındal, I. Uslu, Electronic transport of Au/($Ca_{1.9}Pr_{0.1}Co_4O_x$)/*n*-Si structures analyzed over a wide temperature range, Philos. Mag. A 95 (2015) 1448–1461.
[38] S. Altındal, A. Tataroglu, I. Dokme, Density of interface states, excess capacitance and series resistance in the metal–insulator–semiconductor (MIS) solar cells, Sol. Energy Mater. Sol. Cells 85 (2005) 345–358.
[39] I. Dokme, S. Altindal, Comparative analysis of temperature-dependent electrical and dielectric properties of an Schottky device at two frequencies, IEEE Trans. Electron Devices 58 (2011) 4042–4048.
[40] A. Kaya, O. Vural, H. Tecimer, S. Demirezen, S. Altındal, Frequency and voltage dependence of dielectric properties and electric modulus in Au/PVC + TCNQ/*p*-Si structure at room temperature, Curr. Appl. Phys. 14 (2014) 322–330.
[41] E. Maril, S. Altındal, A. Kaya, S. Kocyigit, I. Uslu, On double exponential forward bias currentvoltage (I–V) characteristics of Au/$Ca_3Co_4Ga_{0.001}O_x$/*n*-Si/Au (MIS) type structures in temperature range of 80–340 K, Philos. Mag. A 95 (2015) 1049–1068.
[42] E.H. Nicollian, A. Goetzberger, The Si-SiO_2 interface electrical properties as determined by the metal-insulator-silicon conductance technique, Bell Syst. Tech. J. 46 (1967) 1055–1133.
[43] R.K. Pandey, A.K. Singh, R. Prakash, Enhancement in performance of polycarbazole-graphene nanocomposite Schottky diode, AIP Adv. 3 (2013) 122120.
[44] R.K. Pandey, R. Mishra, P. Tiwari, R. Prakash, Interface engineering for enhancement in performance of organic/inorganic hybrid heterojunction diode, Org. Electron. 45 (2017) 26–32.
[45] R. Kumar, S. Chand, Structural, electrical and red emission properties of Pd/*n*-ZnO/*p*-Si/Al heterostructures, Electron. Mater. Lett. 11 (2015) 973–981.
[46] R. Kumar, S. Chand, Fabrication and Electrical Characterization of nickel/p-Si Schottky diode at low temperature, Solid State Sci. 58 (2016) 115–121.
[47] S. Acar, S. Karadeniz, N. Tugluoglu, A.B. Selcuk, M. Kasap, Gaussian distribution of inhomogeneous barrier height in Ag/*p*-Si(1 0 0) Schottky barrier diodes, Appl. Surf. Sci. 233 (2004) 373–381.
[48] M. Sharma, S.K. Tripathy, Study of barrier inhomogeneities in I–V-T and C-V-T characteristics of Al/Al_2O_3/PVA:*n*-ZnSe metal–oxide–semiconductor diode, J. Appl. Phys. 112 (2012) 024521.
[49] O. Gullu, S. Aydogan, A. Turut, High barrier Schottky diode with organic interlayer, Solid State Commun. 152 (2012) 381–385.
[50] V.V. Brus, A.K.K. Kyaw, P.D. Maryanchuk, J. Zhang, Quantifying interface states and bulk defects in high-efficiency solution-processed small-molecule solar cells by impedance and capacitance characteristics, Prog. Photovoltaics Res. Appl. 23 (2015) 2586.
[51] S. Chand, R. Kumar, Electrical characterization of Ni/*n*-ZnO/*p*-Si/Al heterostructure fabricated by pulsed laser deposition technique, J. Alloy and compound 613 (2014) 395–400.
[52] R.T. Tung, A.F.J. Levi, J.P. Sullivan, F. Schrey, Schottky-barrier inhomogeneity at epitaxial $NiSi_2$ interfaces on Si(100), Phys. Rev. Lett. 66 (1971) 72–76.
[53] C.R. Crowell, The physical significance of the *T*0 anomalies in Schottky barriers, Solid State Electron. 20 (1977) 171–175.
[54] M.S. Tyagi, Metal-semiconductor Schottky Barrier Junctions and Their Applications, Plenum, New York, 1984.
[55] E.H. Rhoderick, R.H. Williams, Metal-Semiconductor Contacts, Clarendon Press, Oxford, 1988.
[56] K.M. Kim, B.J. Choi, M.H. Lee, G.H. Kim, S.J. Song, J.Y. Seok, J.H. Yoon, S. Han, C.S. Hwang, A detailed understanding of the electronic bipolar resistance switching behavior in Pt/TiO2/Pt structure, Nanotechnology 22 (2011) 254010.
[57] B. Akkal, Z. Benamara, B. Gruzza, L. Bideux, Characterization of interface states at Au/InSb/InP(100) Schottky barrier diodes as a function of frequency, Vacuum 57 (2000) 219–228.