

Modeling the diffusion and depletion capacitances of a silicon pn diode in forward bias with impedance spectroscopy

Cite as: J. Appl. Phys. 136, 115702 (2024); doi: 10.1063/5.0230008

Submitted: 21 July 2024 · Accepted: 2 September 2024 ·

Published Online: 19 September 2024



View Online



Export Citation



CrossMark

P. Casolaro,^{1,2,a} V. Izzo,² G. Giusi,³ N. Wyrsch,⁴ and A. Aloisio^{1,2,5}

AFFILIATIONS

¹ Department of Physicas "Ettore Pancini," Università degli Studi di Napoli Federico II, Complesso Univ. Monte S. Angelo, Napoli I-80126, Italy

² INFN Sezione di Napoli, Complesso Univ. Monte S. Angelo, Napoli I-80126, Italy

³ Department of Engineering, University of Messina, Messina I-98166, Italy

⁴ Photovoltaics and Thin Film Electronics Laboratory (PV-LAB), Institute of Electrical and Microengineering (IEM), Ecole Polytechnique Fédérale de Lausanne (EPFL), Maladière 71B, 2000 Neuchâtel, Switzerland

⁵ Task Force of Bioelectronics, Università degli Studi di Napoli Federico II, Complesso Univ. Monte S. Angelo, Napoli I-80126, Italy

^aAuthor to whom correspondence should be addressed: pierluigi.casolaro@unina.it

ABSTRACT

We investigated the capacitance of a forward-biased silicon pn diode using impedance spectroscopy. Despite extensive research spanning decades, no single model in the literature adequately describes the impedance behavior for bias up to the built-in voltage. By employing the 1N4007 diode as a case study, we analyzed the impedance over a wide frequency range, from 1 Hz to 1 MHz. Our analysis reveals that impedance can be effectively studied by combining two models. In both models, the depletion capacitance is assumed to be an ideal capacitor with a value independent of frequency. One model accounts for diffusion processes, while the other addresses interfacial effects, as well as potential and capacitance distributions across the junction. This approach offers valuable insights into the complex capacitance behavior of pn junctions as a function of the bias voltage. Measurements of depletion and diffusion capacitances, as well as of the diode transit time can be achieved from a set of impedance spectroscopy data.

© 2024 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/5.0230008>

21 September 2024 07:34:31

I. INTRODUCTION

Impedance spectroscopy (IS) is a powerful technique to characterize key physical parameters of silicon pn junctions and provide valuable information on manufacturing processes in a non-destructive way. In IS experiments, the sample is driven with a small sinusoidal signal superimposed to a constant bias level (voltage or current) and the impedance (modulus and phase) is measured as a function of frequency. IS is widely used in electrochemical analysis, corrosion studies, as well as in the characterization of energy storage elements and biosensors. We present an IS-based approach to disentangle the depletion and diffusion capacitances of a silicon pn junction in forward bias by using AC impedance data. The first numerical calculation of depletion

capacitance C_j (also known as transition, dual layer, or space-charge capacitance) was made by Breitschwerdt¹ and Lee² for junctions with different doping profiles in epitaxial structures. A closed form of C_j for both symmetrical and asymmetrical junctions was derived by Chang³ both in reverse and forward bias. The deviation observed from the classical Schottky theory, particularly notable under reverse bias conditions, was attributed to additional carrier dynamics. The evaluation of capacitance in forward bias was later corrected by Kleinknecht⁴ by taking into account high injection effects. The capacitance for plane, cylindrical, and spherical pn diffused junctions was calculated by Lee and Sze⁵ and the voltage dependence for Gaussian diffusion junctions was derived by Wilson.⁶ Small-signal analysis of the total junction capacitance

showed how the sum of diffusion capacitance C_d and C_j justifies the monotonic increase of the total capacitance in forward bias.⁷ The effect of the lead inductance and bulk resistance on the junction capacitance was investigated by O'hearn and Chang⁸ through a small-signal analysis of abrupt pn junction capacitance. Among the early papers, the most accurate and complete analysis of the junction capacitance was presented by Green and Gunn.⁹ They studied the total capacitance in the low-frequency limit and the inductive behavior at high forward bias.

In this paper, as a case study, we present an IS-based analysis of 1N4007, a slow rectifier narrow-base silicon diode with an asymmetric p⁺n junction. We discuss two models: one based on the transmissive finite-length Warburg (TFLW) element, the other, based on the constant phase element (CPE). Finally, we present our results, which include the measurement of depletion and diffusion capacitances and of the diode transit time as a function of bias.

II. MATERIALS AND METHODS

A. The 1N4007 diode

The 1N4007 diode is a planar diffused p⁺n diode produced by many Si foundries, also available as bare die.¹⁰ It is a member of the 1N400x family, composed by devices with increasing peak reverse voltage, from 40 V (1N4001) to 1000 V (1N4007). The assembly of 1N4007 is shown in Fig. 1 (left), with the molded epoxy body partially removed. The x-ray picture in Fig. 1 (right) shows the top and bottom contacts of the die, which is about 250 μm thick.

According to Bisquert and Garcia-Belmonte,¹¹ in this diode, the size of the n bulk region W_n is of the order of 10 μm and the hole diffusion length in slow diodes is $L_p \sim 100 \mu\text{m}$, making this device a narrow-base diode ($W_n \ll L_p$).

B. Experimental setup

Measurements have been taken with a Solartron Modulab-XM ECS potentiostat. The diode has been placed in a Faraday cage to reduce environmental interference, mainly due to the power grid and switching power supplies. All measurements have been done at a fixed temperature of 23 °C.

DC measurements have been taken in the *staircase linear sweep voltammetry* mode. The measurement of the IV curve has

been performed with a step of 2 mV, a scan rate of 5 mV/s, and an integration time of 10 Power Line Cycles (PLCs).

Small-signal AC analysis has been performed by adding a sine wave with a rms amplitude of 4 mV to the DC bias voltage. The small amplitude of the sine wave allows performing a linear analysis with a good signal-to-noise ratio.¹² Measurements based on frequency sweeps (ranging from 1 Hz to 1 MHz) have been performed with an integration time of 20 PLCs. A 1 s delay has been introduced between each frequency change and the subsequent measurement. Such a delay has been shown to be a key factor in reducing the noise, in particular, at low-frequency. The Mott-Schottky measurement has been performed with a step of 10 mV, a scan rate of 5 mV/s, a frequency of 20 kHz, and an integration time of 100 PLCs.

C. Preliminary characterization

The IV curve in reverse bias and forward bias of the 1N4007 diode used in this paper is shown in Fig. 2(a). We evaluated the saturation current by fitting the IV curve in reverse bias with the Shockley equation,

$$I = I_s(e^{\frac{V}{nV_T}} - 1),$$

where I is the current, I_s is the saturation current, V is the bias voltage, $V_T = KT/q$ is the thermal voltage, q is the elementary charge, K is the Boltzmann constant, T is the absolute temperature, and η is the diode ideality factor that will be discussed later. We found that $I_s = 1.31 \pm 0.05 \text{nA}$. The inset shows the differential resistance $R_{dc} = (dI/dV)^{-1}$ in forward bias.

The Mott-Schottky plot in Fig. 2(b) shows $1/|C|^2$ as a function of bias, where the complex capacitance C is defined as¹³

$$C = \frac{1}{j\omega Z_{exp}}, \quad (1)$$

and Z_{exp} are the measured values of impedance.

From this plot, a built-in voltage $V_{bi} = 689 \pm 1 \text{ mV}$ has been estimated.

D. AC impedance calculation

The AC impedance of pn junctions has been discussed in classical treatises on the physics of semiconductor devices by assuming

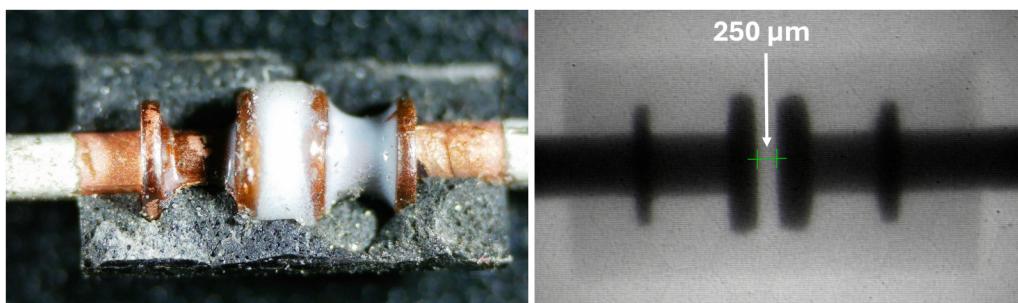


FIG. 1. 1N4007 internal structure with molded epoxy partially removed (left); X-ray image showing the contacts with the die and its thickness (right).

21 September 2024 07:34:31

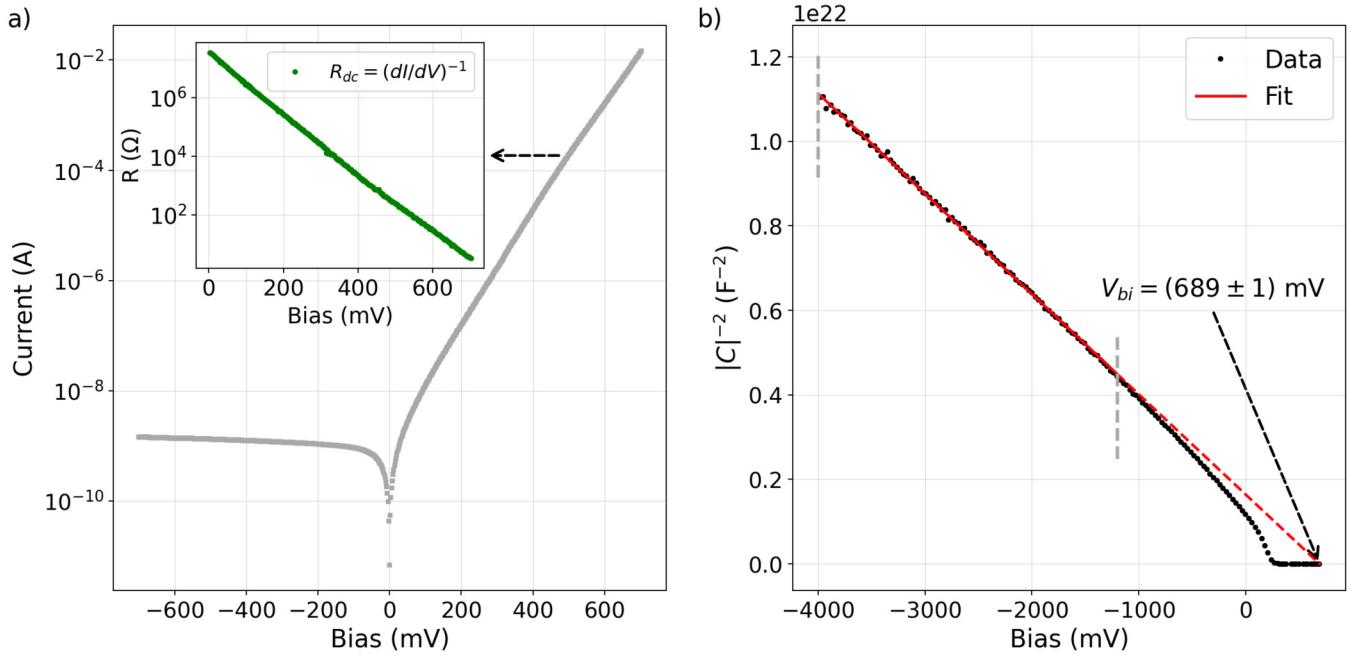


FIG. 2. (a) The IV curve from -700 to 700 mV; the inset shows the differential resistance in forward bias. (b) The Mott–Schottky plot, data between gray dashed lines are fitted to evaluate V_{bi} .

21 September 2024 07:34:31

that diffusion is the only contribution of the junction capacitance.^{14,15} In these works, the resistance and diffusion capacitance have been calculated for an asymmetric pn junction with the p side highly doped with respect to the n side. The low-frequency limits ($\omega\tau_p \ll 1$) of the resistance $R^{(lf)}$ and diffusion capacitance $C_d^{(lf)}$ are

$$\begin{cases} R^{(lf)} = \frac{\tau_p V_T}{A q L_p p_{n0}} e^{-V/V_T} = R_{dc}, \\ C_d^{(lf)} = \frac{\tau_p}{2R_{dc}}, \end{cases} \quad (2)$$

where ω is the angular frequency, τ_p is the hole lifetime, V is the bias voltage, A is the junction area, q is the elementary charge, L_p is the hole diffusion length, p_{n0} is the electron concentration at equilibrium, and R_{dc} is the differential resistance obtained from the IV curve. The high-frequency limits ($\omega\tau_p \gg 1$) are

$$\begin{cases} R^{(hf)} = R_{dc} \sqrt{\frac{2}{\omega\tau_p}}, \\ C_d^{(hf)} = \frac{1}{R_{dc}} \sqrt{\frac{\tau_p}{2\omega}}. \end{cases} \quad (3)$$

In the high-frequency limit, both the resistance and diffusion capacitance show a dependence from $\omega^{-1/2}$, the typical signature of diffusion processes. It should be noted that capacitance is a function of the specific waveform applied to the junction.¹⁴ Pierret¹⁶ has highlighted that at small forward biases, the depletion layer is the primary source of capacitance; however, as the bias increases, the diffusion capacitance eventually becomes dominant. Van der

Ziel¹⁷ showed that the diffusion capacitance is present even in reverse bias, but it vanishes when the applied voltage is larger in modulus with respect to the thermal voltage. Lindmayer and Wrigley¹⁸ provided a comprehensive discussion of the AC impedance of narrow-base diodes. Here, we refer to the case of the n-region size W_n being much smaller than the hole diffusion length ($W_n \ll L_p$). The narrow-base impedance $\hat{Z}(\omega)$ can be written as

$$\hat{Z}(\omega) = R_{dc} \frac{1}{\sqrt{j\omega \frac{W_n^2}{D_p}}} \tanh \left(\sqrt{j\omega \frac{W_n^2}{D_p}} \right), \quad (4)$$

where D_p is the hole diffusion coefficient.

In the following, we present two models to study the AC impedance. In both models, C_j is assumed to be an ideal capacitor, with a value independent of the frequency. In Model-1, C_j is in parallel with a network including a TFLW element to take into account 1D diffusion processes with non-blocking contacts. In Model-2, C_j is in parallel with a network including a CPE that addresses interfacial effects and potential and capacitance distributions across the junction.

E. Model-1

Following Bisquert and Garcia-Belmonte¹¹ and Garcia-Belmonte *et al.*,¹⁹ impedance of Eq. (4) is analogous to the impedance of a 1D diffusion process with non-blocking contacts (also known as

transmissive or with permeable boundaries^{20,21}) in a finite zone. Such a diffusion process can be modeled with the TFLW element, whose impedance is defined as

$$Z_{\text{TFLW}}(\omega) = R_{\text{TFLW}} \frac{\tanh(\sqrt{j\omega\tau_{\text{TFLW}}})}{\sqrt{j\omega\tau_{\text{TFLW}}}}, \quad (5)$$

where R_{TFLW} and τ_{TFLW} are the resistance and the time constant, respectively. The real and complex parts of the TFLW impedance of Eq. (5) are²²

$$\begin{cases} Z'_{\text{TFLW}}(\omega) = \frac{RTFLW}{\sqrt{2\omega\tau_{\text{TFLW}}}} \frac{\sinh(\sqrt{2\omega\tau_{\text{TFLW}}}) + \sin(\sqrt{2\omega\tau_{\text{TFLW}}})}{\cosh(\sqrt{2\omega\tau_{\text{TFLW}}}) + \cos(\sqrt{2\omega\tau_{\text{TFLW}}})}, \\ Z''_{\text{TFLW}}(\omega) = -\frac{RTFLW}{\sqrt{2\omega\tau_{\text{TFLW}}}} \frac{\sinh(\sqrt{2\omega\tau_{\text{TFLW}}}) - \sin(\sqrt{2\omega\tau_{\text{TFLW}}})}{\cosh(\sqrt{2\omega\tau_{\text{TFLW}}}) + \cos(\sqrt{2\omega\tau_{\text{TFLW}}})}. \end{cases} \quad (6)$$

The comparison of Eq. (5) with Eq. (4) shows that the two parameters of the TFLW element are

$$\begin{cases} R_{\text{TFLW}} = R_{dc}, \\ \tau_{\text{TFLW}} = \frac{W_n^2}{D_p}. \end{cases} \quad (7)$$

The equivalent circuit used for fitting the data in the full frequency range is shown in Fig. 3.

C_{j1} is the depletion capacitance and its value does not depend on the frequency. The series of the charge transfer resistor R_{diff} and the TFLW element is in parallel with C_{j1} . This parallel network is in series with the inductor L_1 to model the effects of the cabling harness, the stray inductance of the diode package, and the modulation of the bulk resistance.^{8,9} R_{s1} takes into account the series resistance of the diode. We have found that this circuit provides a better agreement with experimental data with respect to the one described by Bisquert and Garcia-Belmonte.¹¹

F. Low-frequency limit of Model-1

At high frequencies, the diffusion capacitance vanishes [see $C_d^{(hf)}$ in Eq. (3)]. On the contrary, at low frequencies, it competes with C_j , becoming predominant over C_j at high forward bias. Therefore, the low-frequency limit of the diffusion capacitance is investigated below.

A very detailed discussion of the TFLW low-frequency limit has been carried out by Moya.²³ Among the studied expansions, the Cauer circuit shown in Fig. 4 provides the best approximation to the TFLW impedance for frequencies below the characteristic angular frequency $\omega_d = 2.5/\tau_{\text{TFLW}}$.

The Cauer circuit shown in Fig. 4(a) is made by a series of the resistor $R_{x0} = R_{\text{TFLW}}/6$ with a parallel network of the resistor $R_{x1} = 5R_{\text{TFLW}}/6$ and a capacitor,

$$C_{x0} \equiv C_{d1}^{(lf)} = \frac{12\tau_{\text{TFLW}}}{25R_{\text{TFLW}}}. \quad (8)$$

It is interesting to note that the value of $C_{d1}^{(lf)}$ is very similar to the value of $C_d^{(lf)}$ reported in Eq. (2), being only 4% smaller. The low-frequency limit ($\omega < \omega_d$) of Model-1 (to which we will refer to as Model-1^(lf)) is shown in Fig. 4(b). In the following, $Z_1^{(lf)}$ is the total impedance of Model-1^(lf).

G. Model-2

In Model-2, we keep assuming C_j being frequency-independent, while we model the diffusion capacitance with a network including a CPE. This approach is motivated by the presence of interfacial effects as well as potential and capacitance distributions along the pn junction,²⁴ especially at low forward bias. The CPE has been used to model the pn junction interface uniformity and quality,²⁵ surface disorder, roughness, varying geometry,²⁶ growth-related issues of complex semiconductor structures,²⁷ as well as a distribution of capacitance due to current and potential non-uniformity.²⁸ Recently, the CPE has been used in solar cells to model the capacitance of the pn junction²⁹ and the distribution of trap levels.^{30,31} CPE has been also used to model the non-ideality behavior of double-layer capacitance in many electrochemical systems.^{32–34} Bisquert and Compte³⁵ have studied the electrochemical impedance of anomalous diffusion in a spatially restricted layer, showing that this impedance can be approximated by a parallel network of a resistance and a CPE. Furthermore, Niya and Hoofar³⁶ have shown that, in specific cases, most of the aforementioned interpretations can be addressed by using a framework based on anomalous diffusion. However, it should be noted that the origin of the CPE is still unclear and there is a wide debate on its application to IS modeling.^{32,37} The equivalent circuit used for fitting the data in the full frequency range is shown in Fig. 5.

21 September 2024 07:34:31

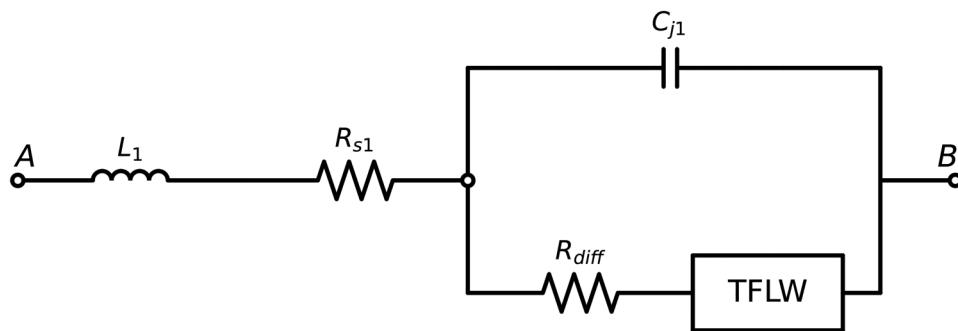


FIG. 3. Model-1 based on the TFLW element. L_1 : inductor, R_{s1} : series resistance, C_{j1} : depletion capacitance, R_{diff} : charge transfer resistance, TFLW: transmissive finite-length Warburg element.

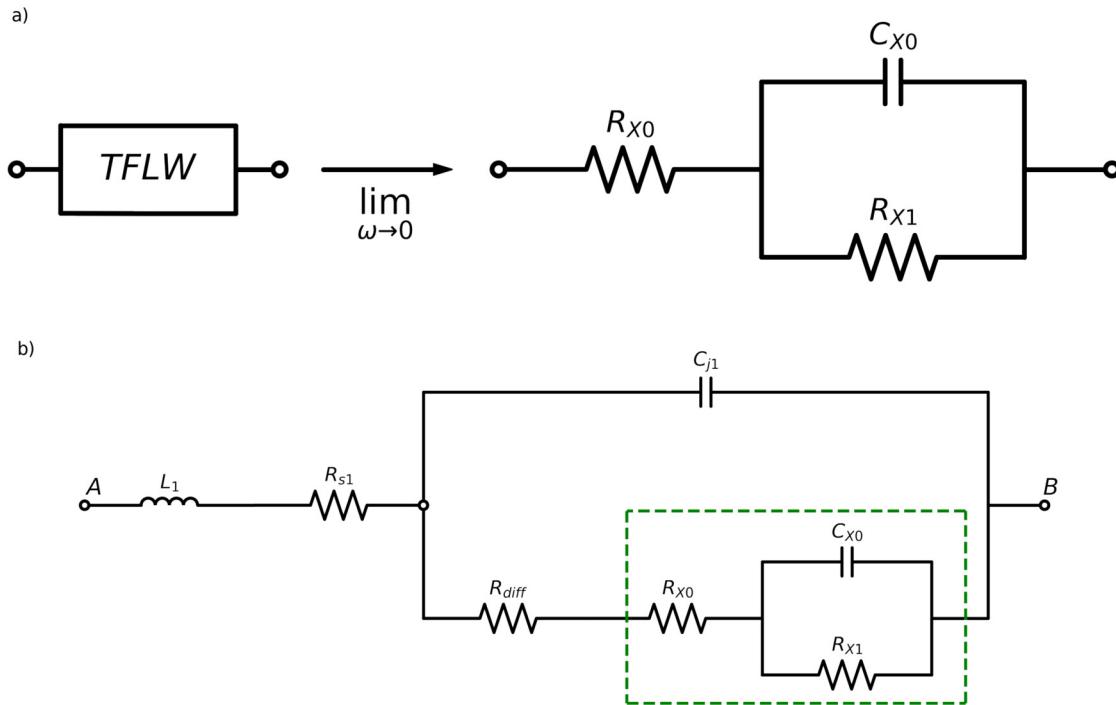


FIG. 4. (a) Cauer approximation to the TFLW element.²³ (b) Low-frequency limit of Model-1: Model-1(lf). The green dashed box surrounds the Cauer circuit.

21 September 2024 07:34:31

In the same way as for Model-1, C_{j2} is the depletion capacitance. The series of ohmic resistance³⁸ R_e with the parallel of the finite diffusion resistance R_{fd} and the CPE is, in turn, in parallel with C_{j2} . This parallel network is in series with the inductor L_2 and R_{s2} . The impedance of the CPE is given by³²

$$Z_{CPE}(\omega) = \frac{1}{(j\omega)^\phi Q} = \frac{\cos(\phi\pi/2)}{Q\omega^\phi} - j\frac{\sin(\phi\pi/2)}{Q\omega^\phi},$$

where Q is measured in $F \cdot s^{\phi-1}$ and ϕ is a dimensionless variable taking any value in the range from -1 to 1 . When $\phi = 1$, the impedance is formally equivalent to that of a pure capacitor of value Q . In all other cases, Q does not have the dimension of a capacitance, so any model deriving a capacitance from Q and ϕ requires an in-depth analysis of the device characteristics.³³ When $\phi = 0.5$, the CPE impedance corresponds to the high-frequency limit of the TFLW and it is usually interpreted as associated to the diffusion

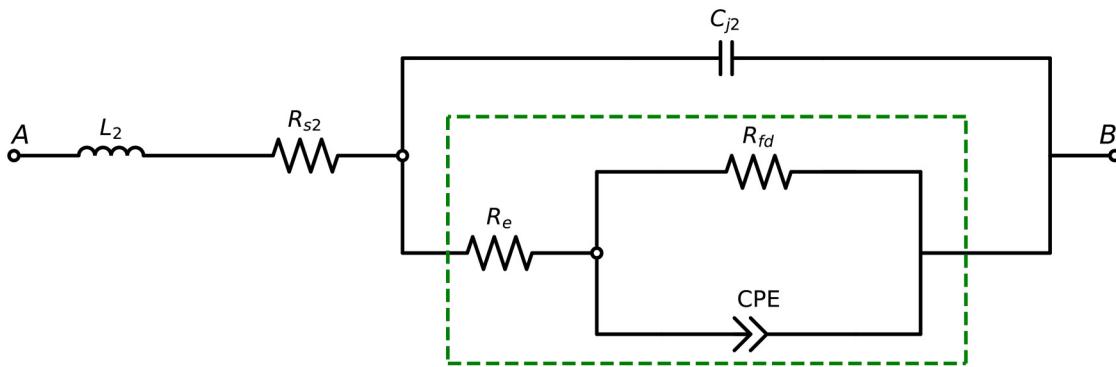


FIG. 5. Model-2 based on the CPE element. L_2 : inductor, R_{s2} : series resistance, C_{j2} : depletion capacitance, R_e : ohmic resistance, R_{fd} : finite diffusion resistance, CPE: constant phase element.

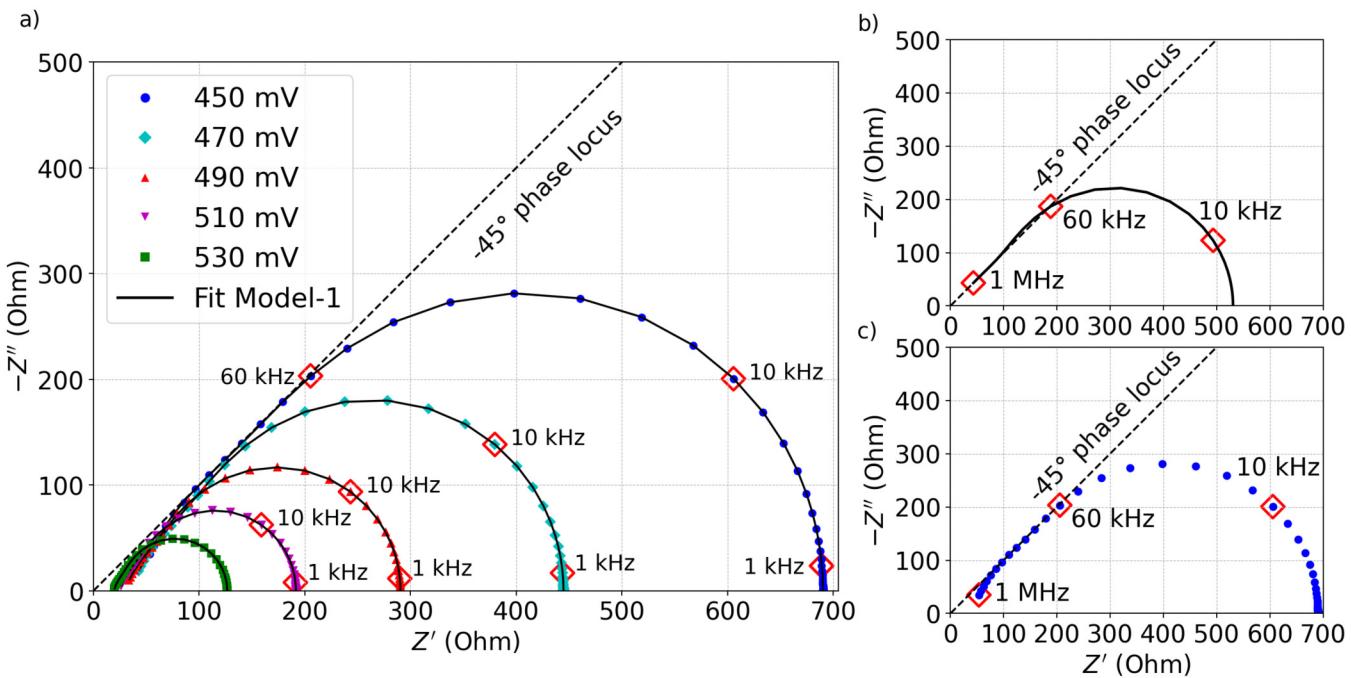


FIG. 6. (a) Nyquist plots in the range 450–530 mV fitted with Model-1. (b) Nyquist plot of the TFLW element evaluated at 450 mV. (c) Nyquist plot of the data at 450 mV.

21 September 2024 07:34:31

process in semi-infinite space.³⁹ When \$\phi = 0\$, the CPE performs as a resistor, and when \$\phi = -1\$, the CPE performs as an inductor.

The impedance \$Z_2\$ of Model-2 can be written as

$$Z_2 = j\omega L_2 + R_{s2} + \frac{1}{j\omega C_{j2} + Y},$$

where \$Y\$ is the admittance of the dashed network in Fig. 5. According to Hirschorn *et al.*,³⁸ the admittance \$Y\$ is

$$Y = \frac{1}{R_e} \left[1 - \frac{R_{fd}}{R_e + R_{fd}} \left(1 + \frac{R_e R_{fd}}{R_e + R_{fd}} Q(j\omega)^\phi \right)^{-1} \right].$$

Here, we have assumed that the CPE behavior comes from capacitance and time constant distributions on the junction surface. We can derive a value for the diffusion capacitance from the CPE by using Brug's formula^{38,40}

$$C_{d2} = Q^{1/\phi} (R_e^{-1} + R_{fd}^{-1})^{\frac{\phi-1}{\phi}}. \quad (9)$$

III. RESULTS AND DISCUSSION

A. Nyquist plots fitted with Model-1

Nyquist plots are graphical representations of the imaginary part of the impedance with minus sign \$-Z''\$ as a function of the

real part \$Z'\$. The Nyquist plots in the range from 450 to 530 mV fitted with Model-1 are shown in Fig. 6(a).

In the high-frequency region, above 60 kHz, the experimental data follow a straight line with a slope of \$-45^\circ\$, the typical Warburg signature.²⁰ In order to evaluate the contribution of the TFLW element to the whole impedance, it is useful to compare the experimental data with the plot of the TFLW element alone, calculated according to Eq. (6). As an example, this comparison is shown in Figs. 6(b) and 6(c) at 450 mV bias voltage, highlighting the contribution of the TFLW element to the Nyquist plot. In Fig. 6(a), at very high frequencies (close to 1 MHz), the Nyquist plot deviates from the \$-45^\circ\$ phase locus due to the combined effects of wiring and the interplay of capacitance with bulk resistance modulation. The inductive behavior becomes more and more evident by increasing the forward bias. Figure 7 shows the Nyquist plots for bias voltages ranging from 650 to 690 mV. These plots exhibit a positive imaginary part of the impedance starting from approximately 250 kHz.⁹

Figure 8 shows a set of plots of \$|Z''|\$ as a function of \$Z'\$ from 200 to 600 mV on a log-log scale.

At bias voltages \$\geq 380\$ mV, Model-1 allows fitting the data with high accuracy. At lower biases and high frequencies (\$>60\$ kHz), the accuracy of Model-1 gets worse (physical motivations will be discussed later).

In order to verify the low-frequency approximation, Model-1 and Model-1^(f) are compared at the bias voltage of 450 mV. In Fig. 9(a), the Nyquist plots of impedance \$Z_1\$ and its low-frequency limit \$Z_1^{(lf)}\$ are depicted, showing an excellent agreement for \$\omega < \omega_d\$.

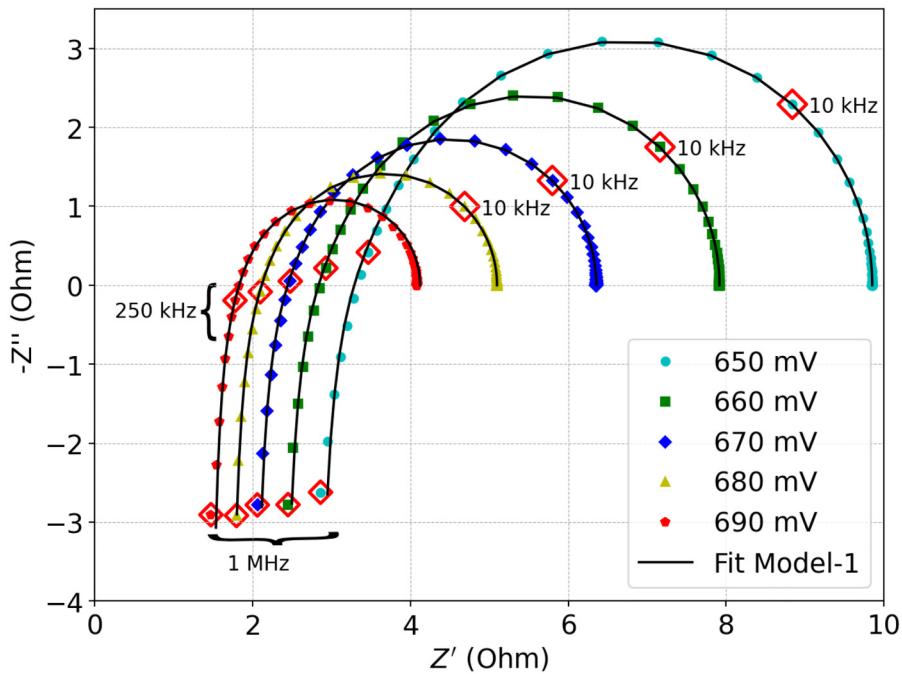


FIG. 7. Nyquist plots in the range of 650–690 mV fitted with Model-1.

The difference between Z_1 and $Z_1^{(lf)}$, normalized to Z_1 , is shown in Fig. 9(b) for the real and imaginary parts of the impedance,

$$\begin{cases} \text{Re}\left[\frac{\Delta Z}{Z_1}(\omega)\right] = \frac{\text{Re}[Z_1^{(lf)}(\omega)] - \text{Re}[Z_1(\omega)]}{\text{Re}[Z_1^{(lf)}(\omega)]}, \\ \text{Im}\left[\frac{\Delta Z}{Z_1}(\omega)\right] = \frac{\text{Im}[Z_1^{(lf)}(\omega)] - \text{Im}[Z_1(\omega)]}{\text{Im}[Z_1^{(lf)}(\omega)]}. \end{cases} \quad (10)$$

The relative error in using the low-frequency model is, hence, less than 0.5% up to the characteristic frequency $\omega_d/(2\pi)$.

21 September 2024 07:34:31

B. Nyquist plots fitted with Model-2

Figure 10(a) shows $|Z''|$ as a function of Z' for biases from 200 to 600 mV on a log-log scale. In Fig. 10(b), Model-1 and Model-2

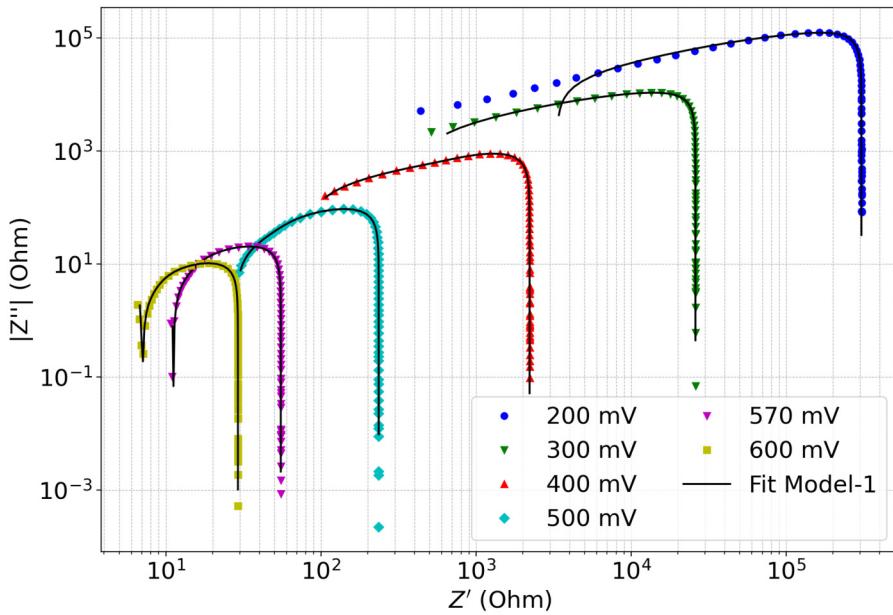


FIG. 8. $|Z''|$ vs Z' plots from 200 to 600 mV fitted with Model-1.

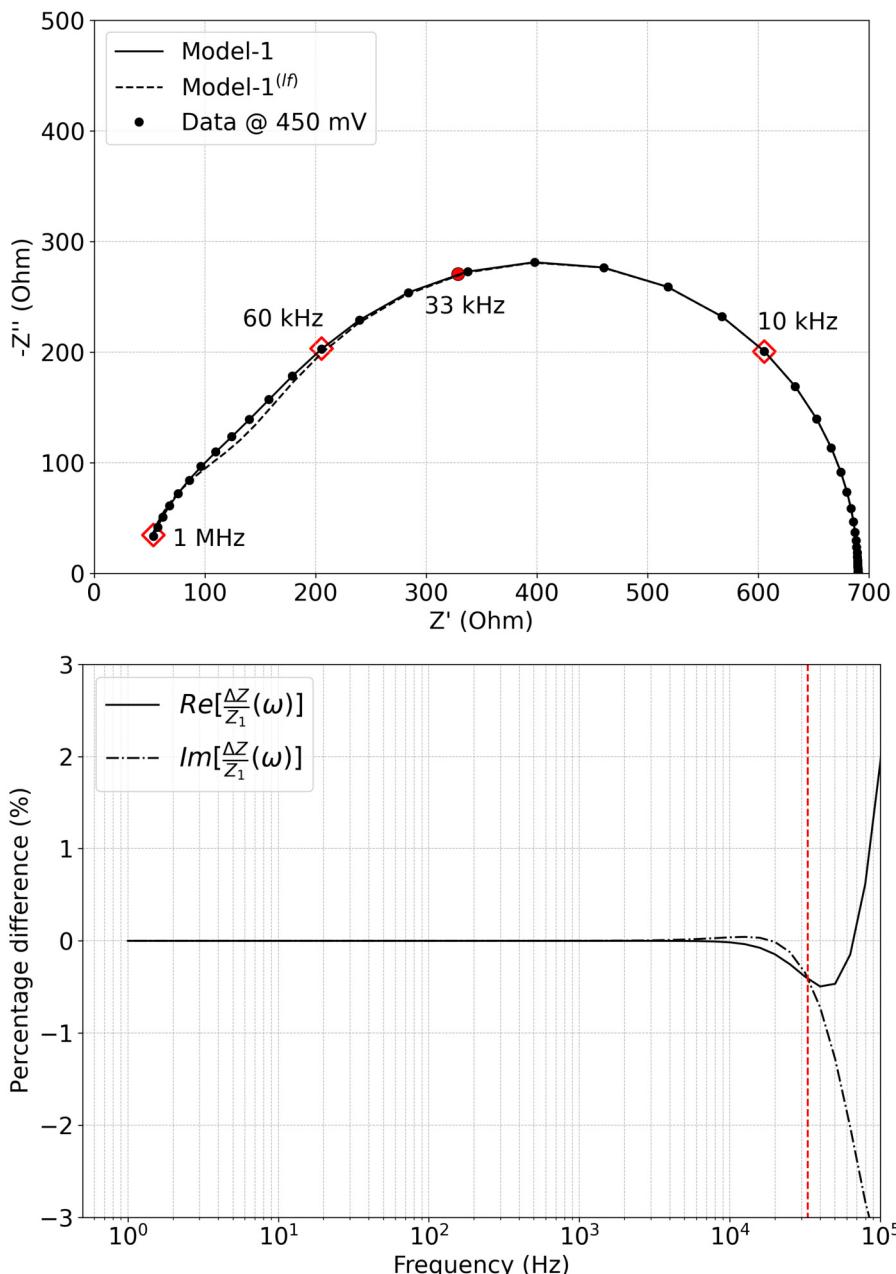


FIG. 9. (a) Nyquist plot of data at 450 mV fitted with Model-1 superimposed with Model-1^(lf). Red dot marks the characteristic frequency $\omega_d/(2\pi)$. (b) Percentage difference vs frequency of $\text{Re}[\frac{\Delta Z}{Z_1}(\omega)]$ and $\text{Im}[\frac{\Delta Z}{Z_1}(\omega)]$ defined in Eq. (10) at 450 mV. Red dashed line marks the characteristic frequency $\omega_d/(2\pi)$.

21 September 2024 07:34:31

fits are compared, showing the better accuracy of Model-2 at biases lower than 380 mV.

The Nyquist plots in the bias range from 200 to 300 mV fitted with Model-2 are shown in Fig. 11.

The absence of asymptotic Warburg behavior at high frequencies motivates that Model-1 is not suitable in low-bias and high-frequency regions. To compare the goodness of the fits performed with Model-1 and Model-2, we introduce the modulus-weighted

squared residuals Res^2 at a given bias, defined as^{41,42}

$$Res^2(\omega_i) = \left(\frac{Z'_{exp}(\omega_i) - Z'_{fit}(\omega_i)}{|Z_{exp}(\omega_i)|} \right)^2 + \left(\frac{Z''_{exp}(\omega_i) - Z''_{fit}(\omega_i)}{|Z_{exp}(\omega_i)|} \right)^2,$$

where $Z'_{exp/fit}(\omega_i)$ and $Z''_{exp/fit}(\omega_i)$ are the real and imaginary parts of the experimental/fitted impedance data at angular frequency ω_i .

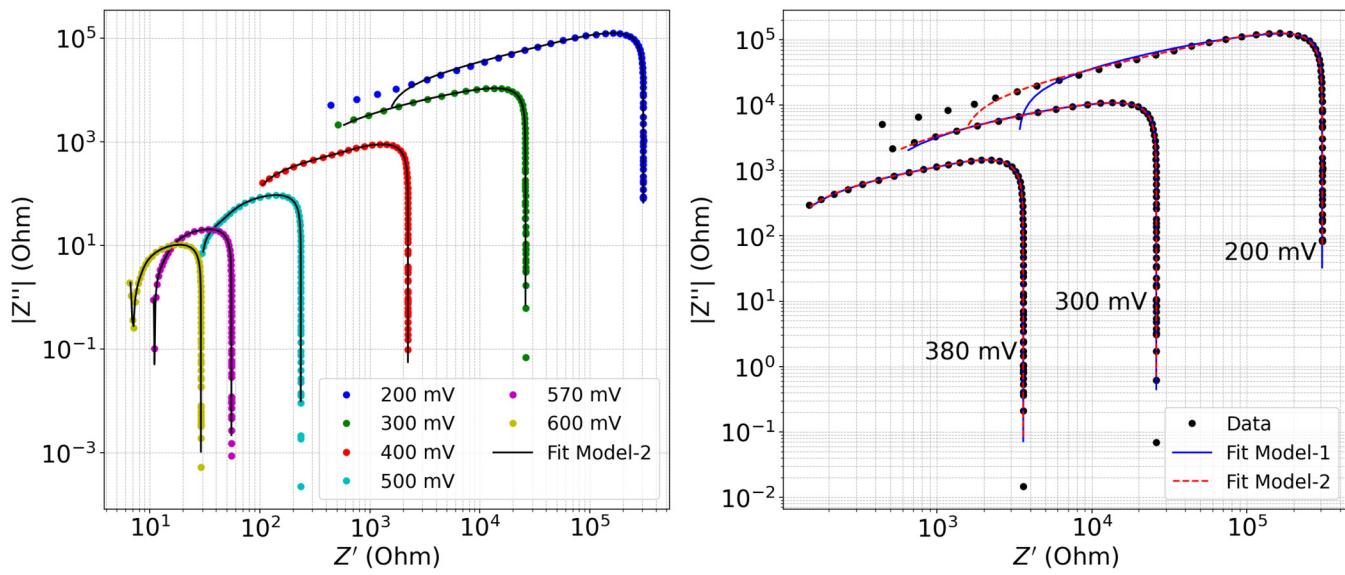


FIG. 10. (a) $|Z''|$ vs Z' plots from 200 to 600 mV fitted with Model-2. (b) Model-1 and Model-2 fits compared at 200, 300, and 380 mV.

Figure 12 presents Res^2 as a function of bias voltage and frequency domain ($200 \text{ mV} < V < 700 \text{ mV}$ and $1 \text{ Hz} < f < 1 \text{ MHz}$) for the two models: (a) Model-1 and (b) Model-2.

In the corner ($V < 380 \text{ mV}$ and $f > 60 \text{ kHz}$), Res^2 of Model-1 increases by nearly four orders of magnitude compared to the remaining domain. In the same frequency-bias corner, Res^2 of Model-2 increases only by a factor 5.

C. Model-1 vs Model-2

The trend of ϕ as a function of bias voltage for the CPE in Model-2 is shown in Fig. 13(a). As previously discussed, CPE behaves as a capacitance in the limit as ϕ tends to 1. Figure 13(b) shows that the numerical values of Q approach C_{d2} defined in Eq. (9) from 380 mV. Therefore, in the limit as ϕ tends to 1, when

21 September 2024 07:34:31

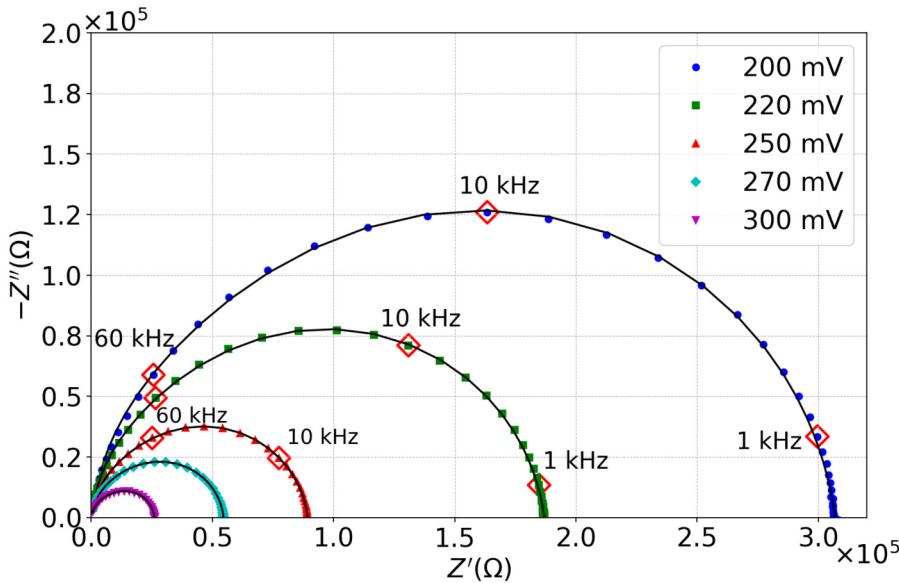


FIG. 11. Nyquist plots in the range of 200–300 mV fitted with Model-2.

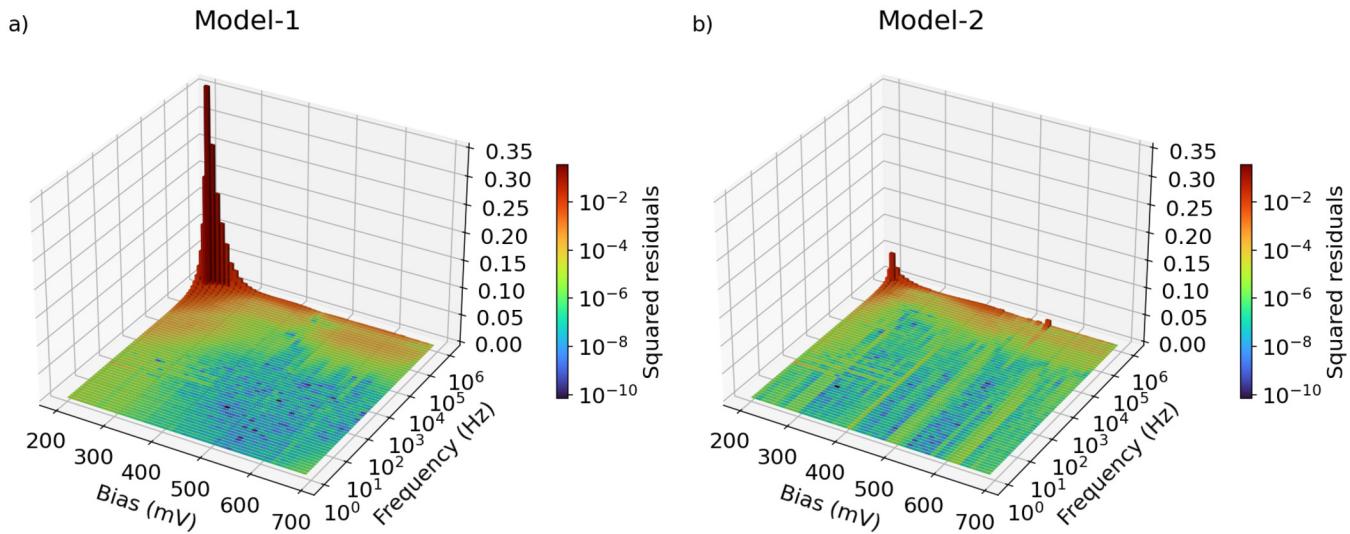


FIG. 12. (a) Modulus-weighted squared residuals vs bias voltage and frequency for Model-1. (b) Same as (a) for Model-2.

the CPE can be replaced by a capacitance, the circuits of Model-2 and Model-1^(f) can be considered to have the same topology.

For biases lower than 380 mV, ϕ steeply falls down to about 0.8, and the CPE cannot be replaced by a capacitance. It is interesting to note that Model-2 can be obtained from Model-1 by replacing the TFLW element with the parallel network of a CPE and the resistor R_{fd} . Therefore, according to Bisquert and Compte,³⁵ Model-2 allows investigating anomalous diffusion and, in this interpretation, ϕ is equal to the sub-diffusion power.³⁶

D. Diffusion capacitance

Figure 14 shows the trends of $C_{d1}^{(f)}$ [see Eq. (8)] and C_{d2} [see Eq. (9)] as a function of the forward bias voltage. For bias higher than 380 mV, Model-1^(f) and Model-2 provide similar values. This is due to the formal equivalence of the circuit topology in the limit of ϕ that tends to 1. The circuit elements of the two models are compared in Fig. S1 in the [supplementary material](#), while the breakdown of the C_{d2} formula is shown in Fig. S2 in the [supplementary material](#).

21 September 2024 07:34:31

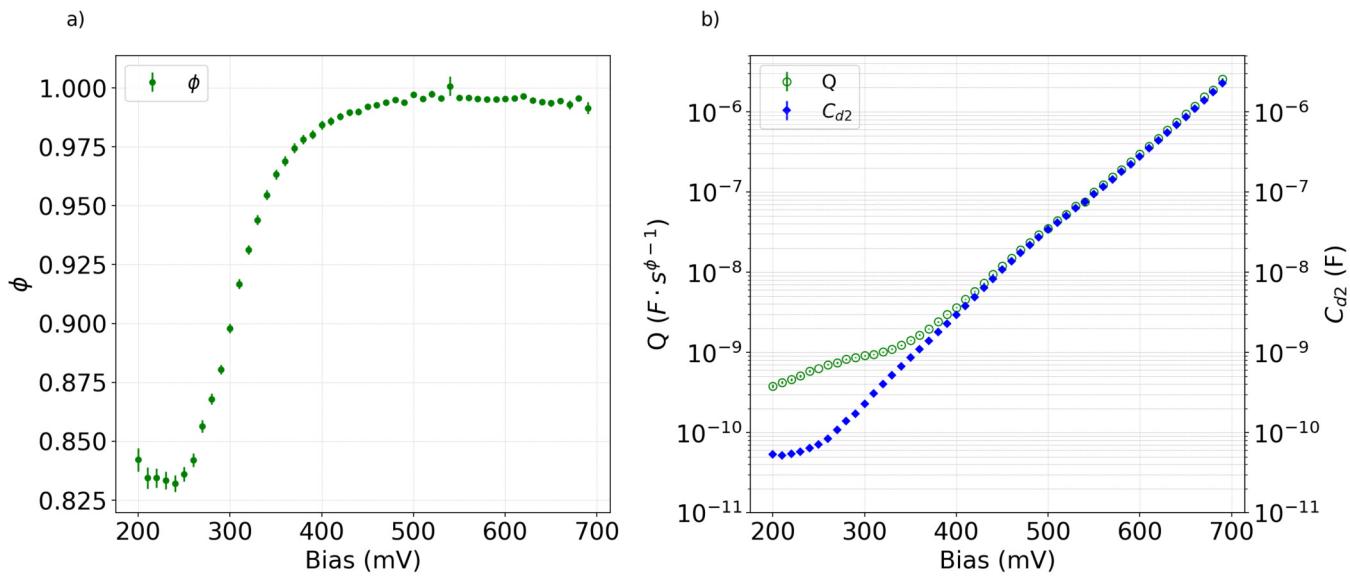


FIG. 13. (a) CPE ϕ values in Model-2 as a function of the bias voltage. (b) CPE Q and C_{d2} in Model-2 from Eq. (9) as a function of the bias voltage.

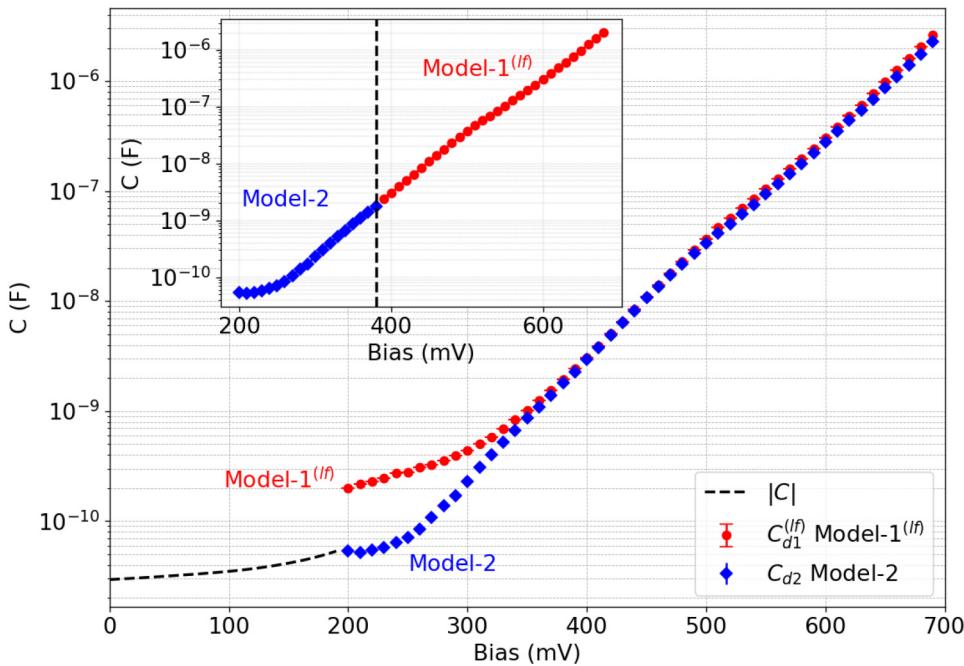


FIG. 14. Diffusion capacitance vs bias voltage for Model-1^(lf) and Model-2, together with $|C|$ measurements at low bias. The inset shows the composite model obtained by matching Model-1^(lf) and Model-2.

21 September 2024 07:34:31

At bias above 380 mV, Model-1^(lf) is preferred because of the strong physical motivation coming from the 1D diffusion process modeled by the TFLW element. At bias below 380 mV, the two models do not agree, with Model-1 giving values of $C_{d1}^{(lf)}$ systematically greater than those from Model-2. We have already noticed that

Model-1 fails in reproducing accurately the data in the low-bias high-frequency corner. On the other hand, Model-2 aligns well with the modulus of the complex capacitance (dashed curve in Fig. 14) taken at low bias. Therefore, our composite model consists of Model-2 up to 380 mV and Model-1^(lf) for higher biases. The inset of Fig. 14

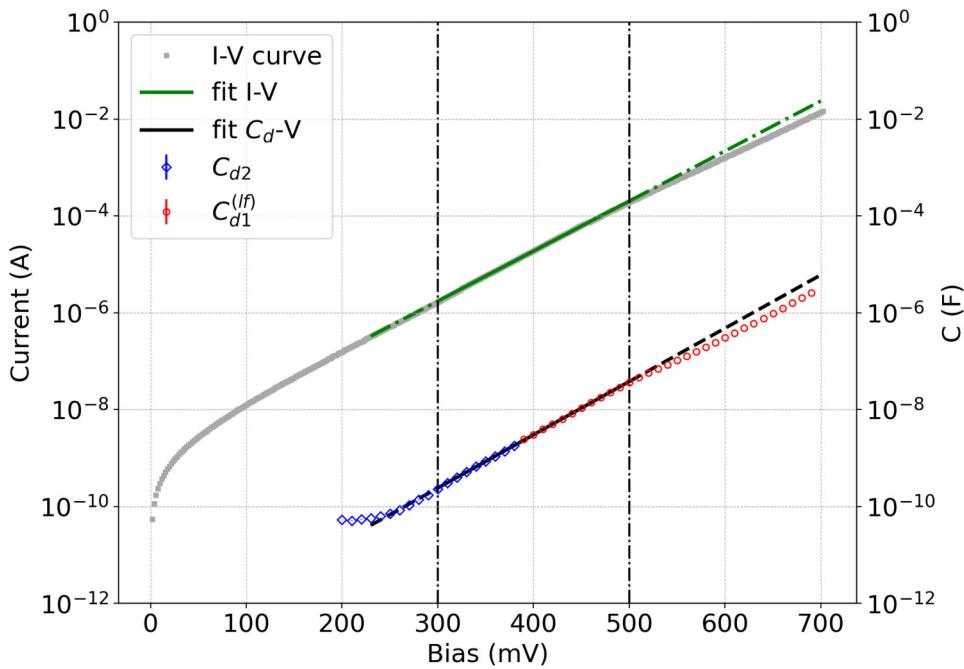


FIG. 15. Comparison of current and diffusion capacitance vs bias. Green and black lines show linear best fit to the current and capacitance vs bias curves, respectively. Data between gray dashed lines are used for the fit.

TABLE I. Ideality factors from current (η_{IV}) and diffusion capacitance (η_{C_dV}).

Fit range (mV)	η_{IV}	η_{C_dV}
300–500	1.6 ± 0.1	1.5 ± 0.3
500–700	1.8 ± 0.1	1.7 ± 0.3

shows the diffusion capacitance from the composite model with values spanning over four orders of magnitude from about 10^{-10} to 10^{-6} F near the built-in voltage. Figure 15 shows the current and diffusion capacitance vs bias, together with their best fits.

As expected, the capacitance is proportional to the current. The ideality factors evaluated in the range 300–500 and 500–700 mV for the current (η_{IV}) and diffusion capacitance (η_{C_dV}) vs bias are reported in Table I, and they are compatible within the experimental uncertainties.

The increase in ideality factor η_{IV} at higher forward bias (from 300–500 to 500–700 mV) is consistent with that reported in the literature,^{18,43} and we observe the same trend also for η_{C_dV} .

E. Depletion capacitance

The classical expression for the depletion capacitance C_j ^{16,44} is

$$C_j = \frac{C_{j0}}{(1 - V/V_{bi})^m}, \quad (11)$$

where V is the applied bias voltage ($V > 0$ in forward bias; $V < 0$ in reverse bias), C_{j0} is the capacitance at zero bias, V_{bi} is the built-in voltage, and m is the grading coefficient, whose value typically ranges from 1/3 to 1/2. It is well known that Eq. (11) has limited applicability at high forward bias due to the C_j divergence

as V tends to V_{bi} . Such a non-physical behavior was addressed by Gummel and Scharfetter,⁴⁵ Poon and Gummel,⁴⁶ and Chawla and Gummel⁴⁷ by introducing an offset voltage to V_{bi} . The model developed in the latter paper also found that the transition region capacitance should eventually decrease after V_{bi} . By adopting a phenomenological approach, Lindholm⁴⁸ found that C_j increases at high forward biases proportionally to $e^{V/(4V_T)}$ before reaching a peak value. The peak position was investigated by Park *et al.*⁴⁹ and van den Biesen,⁵⁰ whose models predict that the peak lies within a range of a few V_T from V_{bi} . After the peak, C_j is expected to decrease proportionally to $e^{-V/(4V_T)}$ for asymmetrical step junctions and to $e^{-V/(2V_T)}$ for linearly graded junctions.⁴⁹ A comprehensive review on the understanding of C_j in forward biases can be found in Liou and Lindholm.⁵¹

Figure 16 shows the values of the depletion capacitance from the composite model.

For bias voltages lower than 330 mV, C_j is proportional to $V^{-1/2}$ (see the inset of Fig. 16) as foreseen by the model by Chawla and Gummel,⁴⁷ also discussed in Liou and Lindholm.⁵¹ From 600 mV, C_j increases proportionally to $e^{V/(\alpha V_T)}$. By fitting the data, we found $\alpha = 3.2 \pm 0.2$. From 670 mV, C_j decreases proportionally to $e^{-V/(\beta V_T)}$, where $\beta = 2.8 \pm 0.3$. The bias V_{pk} corresponding to the peak value has been determined by intersecting the two exponential functions. Its value has been found to be $V_{pk} = 661 \pm 1$ mV. Considering V_T at 23 °C, the peak position is $V_{pk} = V_{bi} - 1.2V_T$, where V_{bi} has been estimated by the Mott-Shottky plot of Fig. 2(b). Overall, the C_j trend around the peak and the peak position with respect to V_{bi} are in reasonable agreement with the models in the literature. It is interesting to note that we also observe the shoulder present in the C_j plot for asymmetrical pn junctions, as predicted by van den Biesen.⁵⁰

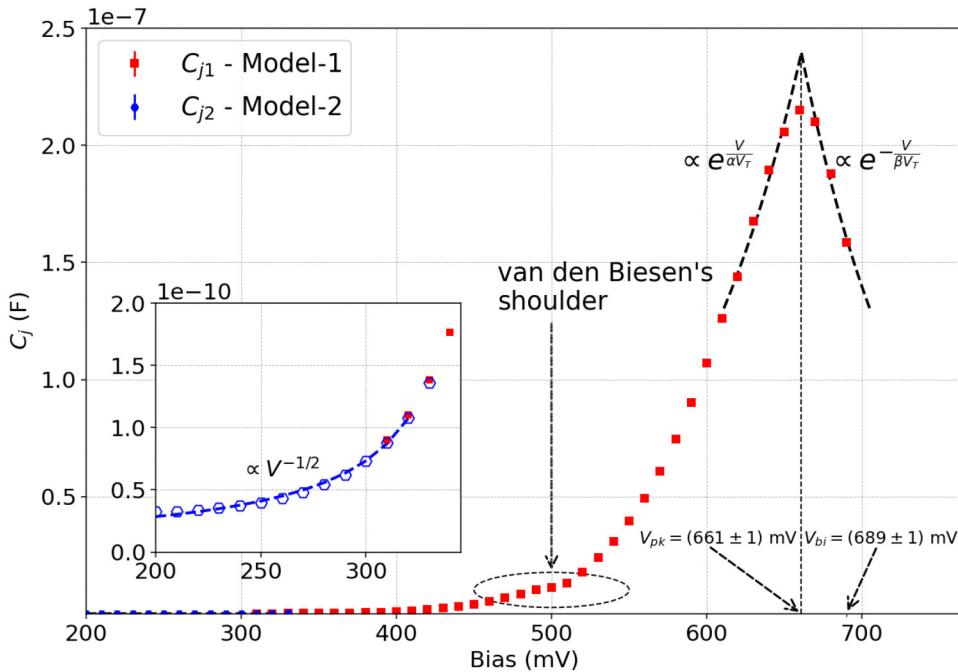


FIG. 16. Depletion capacitance C_j vs bias. The inset shows C_j at very low biases.

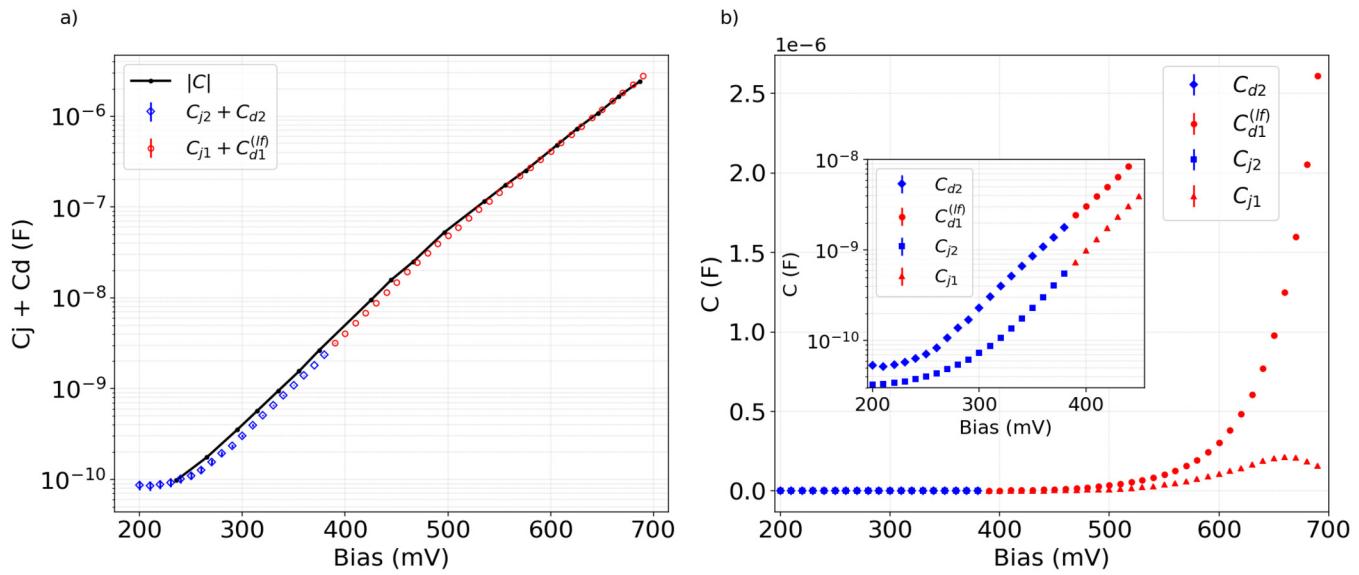


FIG. 17. (a) Total capacitance $C_d + C_j$ from the composite model as a function of the bias voltage superimposed on the measured data of $|C|$. (b) Trends of C_d and C_j as a function of bias; the inset shows the zoom of the main plot in the 200–450 mV range on a log scale.

F. Total capacitance

Figure 17 presents the values of the total capacitance $C_d + C_j$ from the composite model as a function of bias.

It is noteworthy that the values of $C_d + C_j$, spanning over more than 4 orders of magnitude in the investigated bias range, align well with the measured data of $|C|$ defined in Eq. (1). This serves to

validate the accuracy of the values of $C_d + C_j$ obtained from the fit. Additionally, Fig. 17(b) allows comparing depletion and diffusion capacitances vs bias voltage. C_j is less than C_d over the whole explored bias range. Moreover, at V_{pk} (bias voltage where C_j reaches its peak value), the ratio $C_j/C_d = 0.17$. This ratio has its maximum at 210 mV where $C_j/C_d = 0.64$. This analysis is relevant for bipolar

21 September 2024 07:34:31

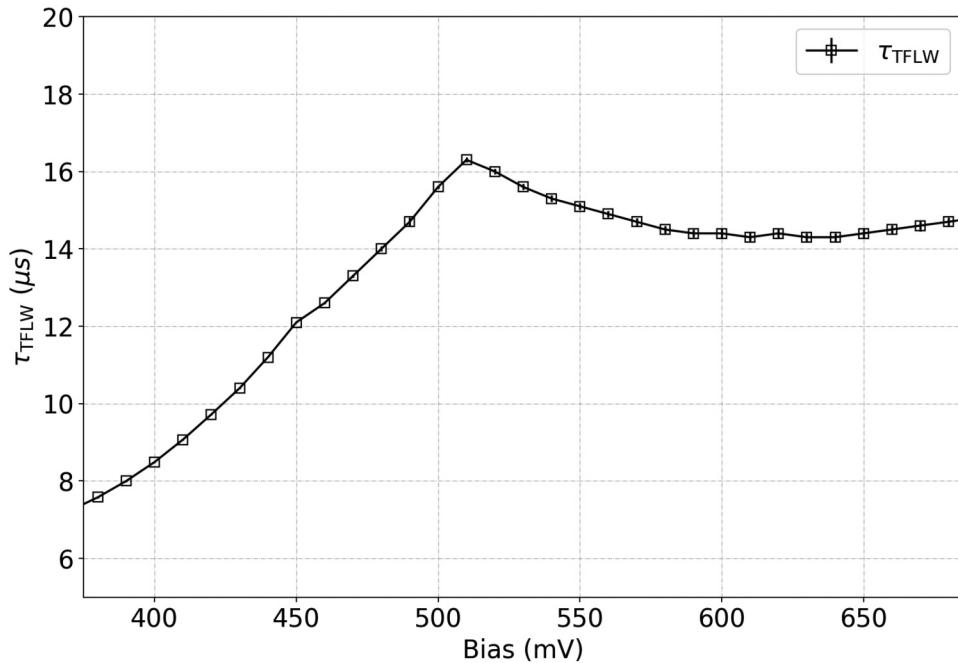


FIG. 18. Time constant τ_{TFLW} from Model-1 vs bias voltage.

transistors because the emitter-base junction has the largest bandwidth when the ratio C_j/C_d is close to 1.⁴⁷ In a future work, we plan to apply our experimental approach to the characterization of more complex devices, such as solar cells and photosensors, which are very often modeled using multiple junctions in series.

G. Diffusion characteristic time constant and transit time

From Model-1, we evaluate the diffusion characteristic time constant τ_{TFLW} . Figure 18 shows the trend of τ_{TFLW} as a function of the bias voltage.

From 380 to 500 mV, τ_{TFLW} increases due to the reduction in the size of the depletion region, resulting in the increase of W_n [see Eq. (7)]. The saturation of τ_{TFLW} at approximately 14 μs implies that W_n has reached a constant value, which is independent from the bias voltage. Our findings align well with those reported by Bisquert and Garcia-Belmonte.¹¹ According to Lindmayer,¹⁸ the diode transit time τ_t is defined as the proportionality factor between the current and the charge stored in the diffusion capacitance. From the diffusion characteristic time constant, τ_t can be derived as

$$\tau_t = \tau_{\text{TFLW}}/2.$$

Notably, the knowledge of the diode transit time allows us to evaluate the diode recovery time in the transient regime.⁵²

IV. CONCLUSIONS

The capacitance of pn junctions in forward bias has been addressed in many papers, starting from the early stage of investigation of doped semiconductors. While theoretical approaches and experimental techniques are well established to characterize the total capacitance, disentangling the contributions of depletion and diffusion is still a debated and controversial topic. The characterization of various Si solar cells has contributed in the last few years to shed new light on the two capacitances and their impact on device performance and reliability. In this paper, we employ two models to study the AC impedance of a narrow base diode. In both models, the depletion capacitance is treated as an ideal capacitor, with a value independent of frequency. Model-1 is based on the TFLW element to take into account 1D diffusion processes with non-blocking contacts. Model-2 is based on the CPE element that has been used in the literature to address interfacial effects, potential and capacitance distributions, as well as anomalous diffusion processes. From Model-1, we estimated the low-frequency limit of the diffusion capacitance. By composing the two models, we find the trends of diffusion and depletion capacitances known from the literature as a function of bias. The transient behavior can also be investigated by means of the diode transit time obtained from Model-1. The proposed methodology can be tailored for characterizing a broad class of solid-state devices, including photovoltaic cells and photosensors, that are based on multiple junctions in series.

SUPPLEMENTARY MATERIAL

See the [supplementary material](#) for further discussion on the comparison of circuit elements of Model-1^(f) and Model-2, and on the breakdown of the C_{d2} formula.

ACKNOWLEDGMENTS

This work was supported by the Italian Research Infrastructure “PRP@CERIC—Pathogen Readiness Platform for CERIC ERIC upgrade” (IR0000028) and by the PRIN 2022 PNRR—OPTICS, both funded by EU—Next Generation EU.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

P. Casolari: Conceptualization (lead); Formal analysis (lead); Investigation (equal); Methodology (equal); Project administration (lead); Software (lead); Validation (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (lead). **V. Izzo:** Formal analysis (supporting); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **G. Giusi:** Formal analysis (supporting); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **N. Wyrsh:** Formal analysis (supporting); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **A. Aloisio:** Data curation (lead); Formal analysis (supporting); Funding acquisition (lead); Investigation (equal); Methodology (equal); Resources (lead); Software (supporting); Supervision (supporting); Validation (equal); Visualization (equal); Writing – original draft (lead); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

- ¹K. Breitschwerdt, “Characteristics of diffused PN junctions in epitaxial layers,” *IEEE Trans. Electron Devices* **12**, 13–19 (1965).
- ²T. Lee, “Calculations of cutoff frequency, breakdown voltage, and capacitance for diffused junctions in thin epitaxial silicon layers,” *IEEE Trans. Electron Devices* **ED-13**, 881–896 (1966).
- ³Y. Chang, “Capacitance of *p-n* junctions: Space-charge capacitance,” *J. Appl. Phys.* **37**, 2337–2342 (1966).
- ⁴H. P. Kleinknecht, “Space-charge capacitance of asymmetric, abrupt *p-n* junctions,” *J. Appl. Phys.* **38**, 3034–3035 (1967).
- ⁵T. Lee and S. Sze, “Depletion layer capacitance of cylindrical and spherical PN junctions,” *Solid-State Electron.* **10**, 1105–1108 (1967).
- ⁶P. Wilson, “Depletion layer and capacitance calculations for Gaussian diffused junctions,” *Solid-State Electron.* **12**, 1–12 (1969).
- ⁷Y. Chang, “The capacitance of PN junctions,” *Solid-State Electron.* **10**, 281–287 (1967).
- ⁸W. O’hearn and Y. Chang, “An analysis of the frequency dependence of the capacitance of abrupt *p-n* junction semiconductor devices,” *Solid-State Electron.* **13**, 473–483 (1970).
- ⁹M. Green and M. Gunn, “The capacitance of abrupt *p-n* junction diodes under forward bias,” *Phys. Status Solidi A* **19**, K93–K96 (1973).

- ¹⁰See https://my.centralsemi.com/datasheets/CPD69-1N4007_WPD.PDF for information about “Datasheet for CPD69-1N4007” (last accessed August 29, 2024).
- ¹¹J. Bisquert and G. Garcia-Belmonte, “Complex plane analysis of PN junction forward-voltage impedance,” *Electron. Lett.* **33**, 900–901 (1997).
- ¹²W. Lai, “Fourier analysis of complex impedance (amplitude and phase) in non-linear systems: A case study of diodes,” *Electrochim. Acta* **55**, 5511–5518 (2010).
- ¹³M. Itagaki, S. Suzuki, I. Shitanda, and K. Watanabe, “Electrochemical impedance and complex capacitance to interpret electrochemical capacitor,” *Electrochemistry* **75**, 649–655 (2007).
- ¹⁴J. Millman and C. Halkias, *Integrated Electronics: Analog and Digital Circuits and Systems*, 2nd ed. (McGraw-Hill, New York, 1972).
- ¹⁵S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, 2021).
- ¹⁶R. F. Pierret, *Semiconductor Device Fundamentals* (Pearson Education, 1996).
- ¹⁷A. Van der Ziel, *Solid State Physical Electronics* (Prentice Hall Inc., Englewood Cliffs, NJ, 1968).
- ¹⁸J. Lindmayer and C. Y. Wrigley, *Fundamentals of Semiconductor Devices* (R. E. Krieger Pub. Co., 1979).
- ¹⁹G. Garcia-Belmonte, J. Bisquert, and V. Caselles, “The small signal AC impedance of a short *p-n* junction diode,” *Solid-State Electron.* **42**, 939–941 (1998).
- ²⁰K. Ariyoshi, Z. Siroma, A. Mineshige, M. Takeno, T. Fukutsuka, T. Abe, and S. Uchida, “Electrochemical impedance spectroscopy part 1: Fundamentals,” *Electrochemistry* **90**, 102007 (2022).
- ²¹A. Moya, “Comparing the characteristic frequencies of the transmissive and reflexive finite-length Warburg diffusion processes,” *J. Electroanal. Chem.* **929**, 117132 (2023).
- ²²T. Q. Nguyen and C. Breitkopf, “Determination of diffusion coefficients using impedance spectroscopy data,” *J. Electrochem. Soc.* **165**, E826–E831 (2018).
- ²³A. Moya, “Low-frequency development approximations to the transmissive Warburg diffusion impedance,” *J. Energy Storage* **55**, 105632 (2022).
- ²⁴A. Ankudinov, A. Titkov, R. Laiho, and V. Kozlov, “Study of the potential distribution in a forward-biased silicon diode using electrostatic force microscopy,” *Semiconductors* **36**, 1058–1064 (2002).
- ²⁵M. Patel and A. Ray, “Evaluation of back contact in spray deposited SNS thin film solar cells by impedance analysis,” *ACS Appl. Mater. Interfaces* **6**, 10099–10106 (2014).
- ²⁶M. Sugiyama, M. Hayashi, C. Yamazaki, N. B. Hamidon, Y. Hirose, and M. Itagaki, “Application of impedance spectroscopy to investigate the electrical properties around the PN interface of Cu (In, Ga) Se₂ solar cells,” *Thin Solid Films* **535**, 287–290 (2013).
- ²⁷H. Sari, H. Sakakura, D. Kawade, M. Itagaki, and M. Sugiyama, “Quantification of sputtering damage during NiO film deposition on a Si/SiO₂ substrate using electrochemical impedance spectroscopy,” *Thin Solid Films* **592**, 150–154 (2015).
- ²⁸P. Córdoba-Torres, T. Mesquita, O. Devos, B. Tribollet, V. Roche, and R. Nogueira, “On the intrinsic coupling between constant-phase element parameters α and Q in electrochemical impedance spectroscopy,” *Electrochim. Acta* **72**, 172–178 (2012).
- ²⁹M. M. Shehata, T. N. Truong, R. Basnet, H. T. Nguyen, D. H. Macdonald, and L. E. Black, “Impedance spectroscopy characterization of c-Si solar cells with SiO_x/poly-Si rear passivating contacts,” *Solar Energy Mater. Solar Cells* **251**, 112167 (2023).
- ³⁰J. Panigrahi, A. Pandey, S. Bhattacharya, A. Pal, S. Mandal, and V. K. Komarala, “Impedance spectroscopy of amorphous/crystalline silicon heterojunction solar cells under dark and illumination,” *Solar Energy* **259**, 165–173 (2023).
- ³¹Y. Proskuryakov, K. Durose, B. Taele, and S. Oelting, “Impedance spectroscopy of unetched CdTe/CdS solar cells—Equivalent circuit analysis,” *J. Appl. Phys.* **102**, 024504 (2007).
- ³²A. Lasia, “The origin of the constant phase element,” *J. Phys. Chem. Lett.* **13**, 580–589 (2022).
- ³³S. M. Gateman, O. Gharbi, H. G. de Melo, K. Ngo, M. Turmine, and V. Vivier, “On the use of a constant phase element (CPE) in electrochemistry,” *Curr. Opin. Electrochem.* **36**, 101133 (2022).
- ³⁴M. Schalenbach, Y. E. Durmus, H. Tempel, H. Kungl, and R.-A. Eichel, “Double layer capacitances analysed with impedance spectroscopy and cyclic voltammetry: Validity and limits of the constant phase element parameterization,” *Phys. Chem. Chem. Phys.* **23**, 21097–21105 (2021).
- ³⁵J. Bisquert and A. Compte, “Theory of the electrochemical impedance of anomalous diffusion,” *J. Electroanal. Chem.* **499**, 112–120 (2001).
- ³⁶S. M. R. Niya and M. Hoofar, “On a possible physical origin of the constant phase element,” *Electrochim. Acta* **188**, 98–102 (2016).
- ³⁷M. S. Abouzari, F. Berkemeier, G. Schmitz, and D. Wilmer, “On the physical interpretation of constant phase elements,” *Solid State Ionics* **180**, 922–927 (2009).
- ³⁸B. Hirschorn, M. E. Orazem, B. Tribollet, V. Vivier, I. Frateur, and M. Musiani, “Determination of effective capacitance and film thickness from constant-phase-element parameters,” *Electrochim. Acta* **55**, 6218–6227 (2010).
- ³⁹A. Moya, “Identification of characteristic time constants in the initial dynamic response of electric double layer capacitors from high-frequency electrochemical impedance,” *J. Power Sources* **397**, 124–133 (2018).
- ⁴⁰G. Brug, A. L. van den Eeden, M. Sluyters-Rehbach, and J. H. Sluyters, “The analysis of electrode impedances complicated by the presence of a constant phase element,” *J. Electroanal. Chem. Interf. Electrochem.* **176**, 275–295 (1984).
- ⁴¹Z. Zhao, Z. Lai, H. Zhi, Y. Zou, Y. Jin, and K. Zeng, “Automated workflow of EIS data validation and quality improvement based on the definition, detection, and removal of outliers,” *Electrochim. Acta* **461**, 142661 (2023).
- ⁴²X. Zhang, S. O. Pehkonen, N. Kocherginsky, and G. A. Ellis, “Copper corrosion in mildly alkaline water with the disinfectant monochloramine,” *Corros. Sci.* **44**, 2507–2528 (2002).
- ⁴³S. Wang, “Fundamentals of semiconductor theory and device physics,” in *Prentice Hall Series in Electrical and Computer Engineering* (Prentice Hall, 1989).
- ⁴⁴A. S. Sedra and K. C. Smith, *Microelectronic Circuits* (Oxford University Press, 2015).
- ⁴⁵H. Gummel and D. Scharfetter, “Depletion-layer capacitance of *p⁺n* step junctions,” *J. Appl. Phys.* **38**, 2148–2153 (1967).
- ⁴⁶H. Poon and H. Gummel, “Modeling of emitter capacitance,” *Proc. IEEE* **57**, 2181–2182 (1969).
- ⁴⁷B. R. Chawla and H. K. Gummel, “Transition region capacitance of diffused PN junctions,” *IEEE Trans. Electron Devices* **18**, 178–195 (1971).
- ⁴⁸F. A. Lindholm, “Simple phenomenological modeling of transition-region capacitance of forward-biased *p-n* junction diodes and transistor diodes,” *J. Appl. Phys.* **53**, 7606–7608 (1982).
- ⁴⁹J.-S. Park, F. A. Lindholm, and A. Neugroschel, “An analytical study of the *p/n* junction space-charge region under high forward voltage,” *J. Appl. Phys.* **62**, 948–953 (1987).
- ⁵⁰J. van den Biesen, “P-N junction capacitances, part I: The depletion capacitance,” *Philips J. Res.* **40**, 88–102 (1985).
- ⁵¹J. J. Liou and F. A. Lindholm, “Capacitance of semiconductor PN junction space-charge layers: An overview,” *Proc. IEEE* **76**, 1406–1422 (1988).
- ⁵²P. O. Lauritzen and C. L. Ma, “A simple diode model with reverse recovery,” *IEEE Trans. Power Electron.* **6**, 188–191 (1991).