MOS Capacitance–Voltage Characteristics II. Sensitivity of Electronic Trapping at Dopant Impurity from Parameter Variations*

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Abstract: Low-frequency and high-frequency Capacitance–Voltage (C–V) curves of Metal–Oxide–Semiconductor Capacitors (MOSC), including electron and hole trapping at the dopant donor and acceptor impurities, are presented to illustrate giant trapping capacitances, from $> 0.01C_{ox}$ to $> 10C_{ox}$. Five device and materials parameters are varied for fundamental trapping parameter characterization, and electrical and optical signal processing applications. Parameters include spatially constant concentration of the dopant-donor-impurity electron trap, N_{DD}, the ground state electron trapping energy level depth measured from the conduction band edge, $E_C - E_D$, the degeneracy of the trapped electron at the ground state, g_D, the device temperature, T, and the gate oxide thickness, x_{OX}.

Key words: trapping capacitance; donor dopant impurity; electron trap; MOS
DOI: 10.1088/1674-4926/32/12/121001 **PACC:** 7340Q **EEACC:** 2560R

1. Introduction

It has been known for 50 years that the CV or C–V (capacitance–voltage) characteristics of Metal–Oxide–Semiconductor Capacitors (MOSC) are distorted due to electronic (electron and hole) trapping at bulk and interfacial (SiO_2/Si) imperfections. The senior author reported a detailed theoretical study during 1960–1964 of the CV characteristics of silicon MOSC's containing point electronic trapping centers, including one and also many combinations of shallow and deep energy-level chemical impurity and physical defect centers, which were experimentally known electronic or electron-hole generation-recombination-trapping (grt) centers, in the bulk of the Si semiconductor[1]. The study also included one and many (distributed in energy) discrete energy-level defect at the SiO_2/Si interface such as the dangling bonds and random-variations of the angle and length of the Si:O and Si:Si bonds. A sample of the computed CV curves is shown in Fig. 1 which is Fig. 16.1.19 of Ref. [1]. This figure shows four theoretical Low-Frequency MOS CV (LFCV) curves in silicon containing one dopant acceptor impurity species, at four different dopant acceptor impurity hole trapping energy levels. One is a very shallow acceptor impurity hole trap, or hole binding energy at a normalized energy level of $U_A = (E_I - E_A)/k_BT = 20$ which is near the silicon valence band edge, since $(E_I - E_V)/k_BT = \sim 22$, therefore, the hole binding energy is $(E_A - E_V)/q = (E_I - E_V)/q - (E_I - E_A)/q = (22 - 20)(k_BT/q) = 2k_BT/q = \sim 52$ mV. Its C_{gb}–V_{GB} shows little visible capacitance peak due to hole trapping because of masking by the high hole (majority carrier) storage capacitance. Another of the four cases is the very deep acceptor impurity hole trap with energy level at the intrinsic Fermi Energy, E_I, or very near the mid-gap of the Si energy gap, $U_A = 0$. Its CV shows a huge hole trapping capacitance peak[2]. The four capacitance peaks of the four curves in Fig. 1, located about 0.50 to 0.75 V, could easily be interpreted erroneously as due to the capacitance minimum

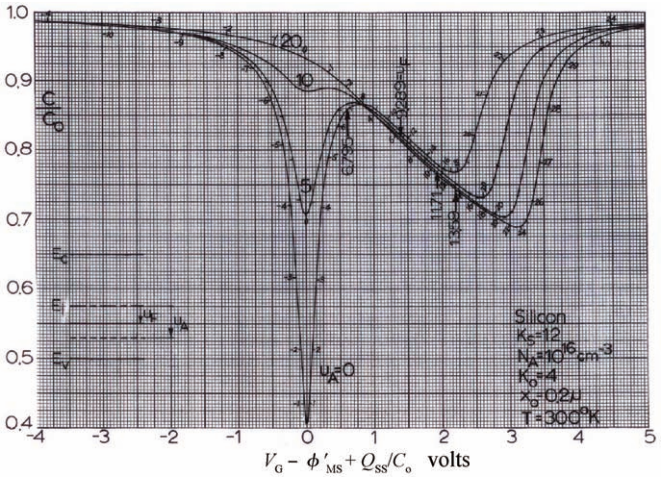

Figure 16.1.19. The low frequency capacitance voltage characteristies of a single level acceptor impurity in silicon.

Fig. 1. Four low-frequency capacitance-voltage characteristics of MOS capacitors on $P_{AA} = 10^{16}$ cm^{-3} acceptor-doped p-type Silicon, with acceptor energy level as the constant parameter given by $(E_I - E_A)/k_BT \equiv U_A = 0$, 5, 10 and 20 where 20 is near the Silicon valence edge and 0 is near the silicon midgap. Computed by Sah in 1961 using slide rules. (See Fig. 2) This figure is the Figure 16.1.19 on p.64 of Ref. [1]. The surface energy band bending or the normalized surface potentials are given by the tick marks on each CV curve, from $(qV_S/k_BT) = U_S = -10$ to $+20$.

* This investigation is supported by Xiamen University, China, and also the CTSAH Associates (CTSA), founded by the late Linda Su-Nan Chang Sah.
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Received 20 September 2011, revised manuscript received 20 October 2011

Fig. 2. Some of the three slide rules used by the senior author, Sah Chihtang, during 1961–1964 to compute the CV curves in Fig. 1 and the curves of the ∼55 figures in Ref. [1]. The top slide rule engraved in ivory is a 1937–1944 slide rule used by A.P.T. Sah (Adam Pen-Tung Sah) (See the black engraving initials on the left bottom side.) made by Chen Yun-Tun Laboratory of China (See the red engravings in the middle of the upper edge.). The middle slide rule engraved in ivory was manufactured by Keuffel & Esser Co. New York in 1947, which was used by Chih-Han Sah during 1950–1954–1955, earning his BS Physics and MS Mathematics degrees at UIUC. (See his pencil handwritten name, home address and phone number, Chih-Han, Sah 607 W. Penn 7-5556, Urbana, in the middle of the lower edge of the long instruction card below the middle Slide Rule.) The lower slide rule in painted (peeling off after 50 years) aluminum was the most precise and had the most functions at the time, made by Pickett & Eckel of Chicago in 1949, used by Chih-Tang Sah during 1961–1981 before he started FORTRAN programming using the DEC FORTRAN on the VAX750, the MicroVAX-2 minicomputers, and the VAXstations 3100-76, 490 and 496. It was easy to use these slide rules to compute the seemingly rather complex C and V_{GB} values at a given U_S as the independent input parametric variable. But it was not possible to use the slide rules to calculate the capacitance for a given V_{GB} as the independent input variable since many high-accuracy iterations are needed to find the highly accurate U_S in order to compute V_{GB} at the computed U_S.

at flat-band, $U_S = 0$ which is marked on the four curves in Fig. 1 and they coincide with zero of the shifted gate-voltage axis, if one forgets the continued decrease of the hole (majority carrier) storage capacitance with increase of positive gate voltage from flat-band gate voltage, which repels and depletes holes in the surface space charge layer. This will be evident in later figures showing the high-frequency CV curves at a sufficiently high signal frequency that hole trapping could not keep up with high frequency signal variation. Such a frequency can be estimated by a simple estimate of the hole trapping rate at the boron acceptor hole trap. See Ref. [3], p.166 and Sections 380 and 381 on p.296–300. The estimate at $T = 300$ K gives $e_p = c_p \times p_1 \equiv \sigma_p \times \theta_p \times N_V \times \exp[-(E_A - E_V)/k_BT] \equiv \pi(\sim 14 \times 10^{-8})^2 \times (\sim 10^7) \times 2.509 \times 10^{19} \times \exp(-2) = 2 \times 10^{12}$ s^{-1} $= (0.5$ ps$)^{-1} = 2\pi f$ or $f \approx 300$ GHz and $\lambda \approx 1$ mm.

These low-frequency C–V curves were computed 50 years ago (1961–1964) by the senior author using slide rules. (See Fig. 2 for the photograph of the three slide rules used.) The Boltzmann distribution was used for the assumed low concentrations of the electrons and holes. Our current interest on the capacitance due to trapping at the bulk dopant impurities was recently intensified[6] by the larger CV distortion at the higher bulk dopant impurity concentrations used in the increasingly faster state-of-the-art transistors of smaller dimensions, due to two possible applications in addition to its importance, always neglected, in CMOS analog and switch applications: **(1)** experimental characterization of the quantum mechanical properties of electronic trapping at the dopant impurities in semiconductors, such as **(1a)** the 'static' properties: energy levels or electronic binding energies, and their three degeneracies (spin, orbital or position $\boldsymbol{r}$, and momentum $\boldsymbol{p} = \hbar\boldsymbol{k}$ or velocity–Magnetic field splitting is deferred to a later report.); and **(1b)** the kinetic properties: rates of electronic, or electron and hole, transitions via the thermal emission to the conduction band of the electron trapped or bound at the donor impurity electron trap, and via the thermal capture of a conduction band electron by the empty donor impurity electron trap, and the two similar transitions of thermal emission and capture of a hole at an acceptor impurity hole trap (just estimated in the last part of last paragraph), which are approached by the increasing frequency (300 GHz) and switching rate (0.5 ps) in applications; as well as the rates of generation and recombination of electrons and holes at these donor and acceptor impurity centers, and **(2)** highly sensitive detectors of the spin states of the trapped electrons (and holes), the charge states of the dopant impurity centers, and the local phonon modes, in signal processing applications, including infrared and far-infrared optical, millimeter-submillimeter electromagnetic waves, and acoustic waves[3, 7], because these detectors can be easily monolithically integrated with the Si MOS transistors and MOS signal processing circuits. The feasibility of **(1)** was theoretically demonstrated and reported recently by us using n-Si MOSC with Phosphorus as the donor impurity[6]. In that feasibility study, we ignored the fine structures in the CV curves arisen from carriers trapped at the excited states and from the spin-orbit-momentum degeneracies of the ground and excited states. We also limited our initial exploration in Ref. [6] to just the shallow level phosphorus donor because the electrons trapped at the excited electron states at the phosphorus donor can be neglected in the usual thermal case, since the energy of excited states are several k_BT's above ground state. At the room temperature of $T = \sim 300$ K $= \sim 27$ C, with $k_BT \approx 25$ meV, an electromagnetic photon of this energy has a wavelength of about 0.05 mm $= 50$ μm and a frequency of 6 THz $= 6000$ GHz $= 6 \times 10^{12}$ Hz. See the Shockley Nomogram[7]. Due to the significant energy elevation of the excited states above the ground state, few donor impurity electron traps (and acceptor impurity hole traps) have its bound (captured or trapped) electron (hole) at one of the excited states, except at temperatures sufficiently high when the thermal energy, k_BT, is comparable to the energy difference between the ground and excited state. Other methods of excitation to populate the excited states, aside from the black-body thermal excitation at thermodynamic equilibrium, have been envisioned and delineated by us, which is the subject of a future report[10, 11]. Thus, under thermodynamic equilibrium considered in this report, electron is usually trapped at the ground state of the phosphorus donor electron trap (or hole, the boron acceptor hole trap). Very few occupied, hence neutral, phosphorus donor (or boron acceptor) impurities are at their excited states. However, when the excited state is within or less than a k_BT above the ground

state, the excited state would and could significantly contribute to the distortion of the CV curve, via additional trapping capacitance contributions from the electrons trapped at the excited states. Regardless of the excited states, the energy position or binding energy of ground state of the electronic trapping energy level, must significantly affect the CV distortion because the capacitance peak occurs in the applied gate voltage range where the electronic trapping rate is the highest, which is limited by the two continual series or sequential electronic transitions, for example, at the donor impurity electron trap: the capture of a conduction-band electron into the electron trap followed by the emission (or release) of a trapped electron back into the conduction band, and the two steps are continued sequentially. The condition of maximum transition rate is one when both electron capture and emission transition are the largest, which occurs when the concentration of the trapped electron that can be released or emitted and the concentration of the unoccupied traps that can trap or capture an electron are equal, that is, half of the electron traps, $N_{DD}/2$, are empty of and the other half, $N_{DD} - N_{DD}/2 = N_{DD}/2$ are occupied by a trapped electron. In this report, we provide the computer generated graphs to illustrate the maximization of the CV distortions due to electron trapping at the dopant donor impurity from varying four fundamental and device parameters: N_{DD} (10^{16} to 10^{19} cm^{-3}), $E_C - E_D$ (10 to 450 meV), $g_D = g_s g_r g_k$ (2 to 64) and T (4 to 600 K). These dopant donor-impurity electron-trap-specific graphic results in n-type semiconductors are applicable to dopant-acceptor-impurity-hole-traps in p-type semiconductors. They can also be extrapolated to n-type donor-impurity-doped semiconductors containing compensating acceptor-impurities, and vice versa[8], and to semiconductors containing generation recombination centers[1]. Their computed details are described in future reports[8, 9].

The definitions of the four parameters and the equations and numerical values of the fundamental constants used in computation are exactly the same as those described in Ref. [2] with the Boltzmann distribution replaced by the Fermi distribution to account for the high concentration of the electrons (or holes). Briefly, N_{DD} is the concentration of the electrically active donor impurity (which is the sum of those not occupied by an electron, hence in +1 charge state, and those occupied by or trapped an electron, hence in the 0 or neutral charge state.) $E_C - E_D$ is the binding energy of the trapped electron or E_D is the energy level of the electron bound or trapped at the donor-dopant-impurity electron trapping center, measured from an understood but unspecified and arbitrary potential energy reference, such as E_C ($x = \infty$) or a point far away from the device region of the material under consideration (such as the SiO_2/Si interface, located at $x = 0$). g_D is the degeneracy or the number of bound wavefunction of different shapes with which the electron can be bound by the impurity potential center at a given binding energy of $E_C - E_D$. It consists of three vector space components, $g_D = g_s g_r g_k$: (i) the spin space $\boldsymbol{s} = (\uparrow, \downarrow)$, $g_s = 2$ for electron spin; (ii) the crystal position space $\boldsymbol{r} = (x, y, z)$, $g_r = n^2$ where $n = 1, 2, 3, \ldots$ is the principle quantum number for the different orbitals or wavefunctions the electron can be bounded to the point-charge donor; and (iii) the crystal momentum space $\hbar\boldsymbol{k} = (\hbar k_x, \hbar k_y, \hbar k_z)$, $g_{k\text{-Si}} = 6$ and $g_{k\text{-Ge}} = 4$. (See [10] or [11]. The presence of a magnetic field introduces a fourth degeneracy.) T is the device temperature at thermodynamic equilibrium, $T_{electron} = T_{hole} = T_{phonon} = T_{photon} = T$. (See Sections 200, 201 and 202 on pages 152 to 159 of Ref. [3] on the necessary and sufficient conditions of equilibrium.)

2. Theory of Capacitance–Voltage Characteristics with Trapping Capacitance

The silicon semiconductor capacitance, C_s, consists of three components in parallel, $C_s = C_n + C_p + C_{nt}$. They are respectively electron and hole storage capacitances, C_n and C_p, and trapped electron (or hole) charge storage capacitance, C_{nt} (or C_{pt}). Their derivation were reported in1964[1] and listed in Ref. [2]. They were extended to high electron and hole concentrations by replacing the Boltzmann distribution with the Fermi (Fermi–Dirac) distribution[3] which are given in the appendix of Refs. [10] or [11] with the numerical constants used. The measured capacitance between the MOS gate and the silicon body or bulk, C_{gb}, generally depends on the measurement frequency because the majority (electrons) and minority (holes) carriers cannot be supplied and extracted instantaneously. But, C_{gb} will reach the asymptotic values at two measurement frequencies, (1) much higher than the trapping frequency, $C_{gb\text{-}hf}$, with C_{nt} dropped out of C_s to give $C_s = C_n + C_p$ and (2) much lower than the trapping frequency, $C_{gb\text{-}lf}$, with C_{nt} fully included in $C_s = C_n + C_p + C_{nt}$. Practical realizations of these asymptotic measurement conditions and of other physical realizations are described in a future report[11]. The independent variable parameter in the calculations is the surface potential or the total energy band bending from the SiO_2/Si interface ($x = 0$) to the distant majority carrier (electron) contact to the body ($x = \infty$). We shall normalize all the electric and electrochemical (when considering electrical non-equilibrium later) potentials to the thermal voltage, $k_B T/q$, where k_B is the Boltzmann constant, T the temperature and q the magnitude of the electron charge. Thus, the normalized electric potential at the interface, or the normalized surface potential, is given by $U_S = U(x = 0) = qV_S/k_B T = qV(x = 0)/k_B T$. Fermi–Dirac distribution is used to take into account of high concentrations of electrons and holes. Distribution or occupation fraction of the electron traps is employed for the trapped electron concentration, denoted by $f_D = N_D/N_{DD}$ where N_D is the concentration of trapped electrons which is also that of the neutral donors, i.e., those donor atoms each occupied by a trapped electron. As explained in the introduction section, the excited states are unimportant in this simplest capacitance model at thermal equilibrium, therefore, we consider only the ground state of the donor electron trap with a total degeneracy of trapped electron wavefunction given by $g_D = g_s g_r g_k$ where $g_s = 2$ is the electron spin degeneracy; $g_r = 1$ for the 1s ground state and $g_r = n^2$ for the excited states ($n = 2, 3, \ldots$) from the hydrogen point-charge model for the impurity potential, which would be split by the non-spherical and non-point-charge components from the finite core charge distribution and from crystalline field; and g_k is the degeneracies due to multiple energy valleys of the conduction band in the momentum ($\hbar\boldsymbol{k}$) space, or the wavenumber-space or k-space ($g_k = 6$ for Si and $g_k = 4$ for Ge[3]); and due to multiple degeneracy of the p-like valence band in k-space which gives $g_k = 2$ for both the p-like Si and Ge va-

lence bands with the third p-state split off by 50 meV for Si and 150 meV for Ge from spin-orbit interaction. The capacitance and the gate-voltage equations are given by the following list. Since the oxide capacitance is readily measured or known from device design, the physics picture of the CV curve is then easier to comprehend with all the computed CV curves normalized to the oxide capacitance per unit area C_{ox}.

$$C_n = -d(-Q_N)/dV_S = -q(N_S - N_\infty)/E_S, \quad \text{Eqs. (410.23)}^{[3]}; \text{(16.11.1B)}^{[1]}, \quad (1)$$

$$C_p = -d(+Q_P)/dV_S = +q(P_S - P_\infty)/E_S, \quad \text{Eqs. (410.22)}^{[3]}; \text{(16.11.1A)}^{[1]}, \quad (2)$$

$$C_t = C_{nt} = -d(-Q_{NT})/dV_S = +q(N_{DS} - N_{D\infty})/E_S, \quad \text{Eqs. (16.11.1C, D)}^{[1]}, \quad (3)$$

$$C_{gb\text{-}lf} = C_{ox}(C_n + C_p + C_t)/(C_{ox} + C_n + C_p + C_t), \quad (4)$$

$$C_{gb\text{-}hf} = C_{ox}(C_n + C_p)/(C_{ox} + C_n + C_p), \quad (5)$$

$$C_{gb\text{-}lf} - C_{gb\text{-}hf} = C_t\{C_{ox}C_{ox}/[(C_{ox} + C_n + C_p + C_t)(C_{ox} + C_n + C_p)]\}, \quad (6)$$

$$[(C_{gb\text{-}lf})^{-1} - (C_{ox})^{-1}]^{-1} - [(C_{gb\text{-}hf})^{-1} - (C_{ox})^{-1}]^{-1} = C_t, \quad (7)$$

$$V_{GB} = +\phi_{MS} - (Q_{OX} + Q_{IT})/C_{ox} + V_S + \varepsilon_{Si}E_S/C_{ox}, \quad \text{Eqs. (412.15)}^{[3]}, \quad (8)$$

$$\begin{aligned} E_S = {} & (\text{sign}U_S)(2k_BT/\varepsilon_S)^{-1/2} \\ & \times \{ + N_V[F_{3/2}(U_F - U_V - U_S) - F_{3/2}(U_F - U_V)] \\ & + N_C[F_{3/2}(U_S + U_C - U_F) - F_{3/2}(U_C - U_F)] \\ & + N_{DD}[-U_S + \log_e(1 + g_D\exp(U_S + U_D - U_F)) \\ & - \log_e(1 + g_D\exp(U_D - U_F))]\}, \end{aligned} \quad (9)$$

$$\begin{aligned} \phi_{MS} &= \phi_M - \chi_{Si} - (E_C - E_F)/q \\ &= 0.65 \pm 0.08 - (E_C - E_I)/q - V_F, \end{aligned} \quad \text{Eqs. (412.12F)}^{[3]}, \quad (10)$$

3. Computed Capacitance–Voltage Characteristics with Trapping Capacitance

The family of seven figures given in Fig. 3, parts 3(a) to 3(g), shows the effect of the energy level or the binding energy of the electron bound to the ground state at the donor trap on the appearance and size of the trapping capacitance peak, C_{nt}. As expected from the 1964 results for the acceptors[1], with a sample shown in Fig. 1 in this report, the electron trapping capacitance peak, $C_{nt\text{-}peak}$, is almost completely masked off by the large or huge electron storage capacitance, C_n, when the donor energy level is near the conduction band edge or the binding energy of the electron trapped at the donor impurity is small. For the low-frequency $C_{gb\text{-}lf}$–V_{GB} curves in Fig. 3(a), the trapping capacitance peak near $V_{GB} = +0.5$ V is nearly invisible for the donor trap at 10 meV due to masking by C_n. As the trapping energy level deepens, the trapping capacitance peak gradually shows up, with a shoulder appearing at 100 meV, a visible peak at 150 meV and full blown peak at 300 meV and deeper, at $T = 300$ K or $k_BT = 25.85$ meV. Figure 3(b) shows increasingly smaller electron and hole storage capacitance, C_n and C_p, contributions to the high-frequency MOS capacitance $C_{gb\text{-}hf}$ as the trap energy level is deepened, because as the energy level deepens, C_n drops steeply to zero as the gate voltage decreases from about $V_{GB} = +0.5$ V to expel and deplete the electrons in the silicon surface space charge layer. Similarly, C_p drops steeply to zero as the gate voltage increases from about $V_{GB} = -1.0$ V to expel and deplete the holes in the silicon surface space charge layer. The deepened trap energy level gives the increasingly larger difference between the low-frequency and high-frequency capacitances, $C_{gb\text{-}lf} - C_{gb\text{-}hf}$, shown in Fig. 3(c). This difference-trapping-capacitance peak is really huge, 53.5% of C_{ox} for the 450 meV deep trap and still 4.83% for the 50 meV trap which corresponds to the spin degenerate ground state of the phosphorus donor dopant impurity in Silicon, although perhaps a little bit small of only 1.28% for the 10 meV dopant donor electron trap in Ge. Figure 3(d) shows the peak-normalized and voltage-shifted CV lineshapes for further aiding the experimental characterization of an unknown donor trap, and for experimental seeking of an optimum donor electron trap to give the largest capacitance signal in applications. Actually, due to the high precision arithmetics offered by run of the mill personal computer today, or even the handheld calculators such as the perennial favorite and best-seller, the 30-year-old HP11C-16C, it is just as easy to compute the reciprocal of the measured high and low frequency capacitances. Their difference, using (7), is shown in Fig. 3(e). But the reciprocal capacitance difference, gives exactly the reciprocal trapping capacitance itself, regardless of the oxide capacitance, as proven algebraically by Eq. (7), or simply by inspection of the capacitance equivalent circuit of the oxide capacitance in series of the semiconductor capacitance which consists of the electron and hole storage capacitances and the electron (and hole if acceptors are present) trapping capacitance, all in parallel. So, the large electron and hole storage capacitances, C_n and C_p are subtracted out in this difference computed from the reciprocal of the measured capacitances at low and high frequencies. Without the reduction by the series C_{ox}, the result, now the C_{nt}, shows its true and larger trapping capacitance, 116% of C_{ox} for the 450 meV deep trap, and nearly 42.5% of C_{ox} for the 50

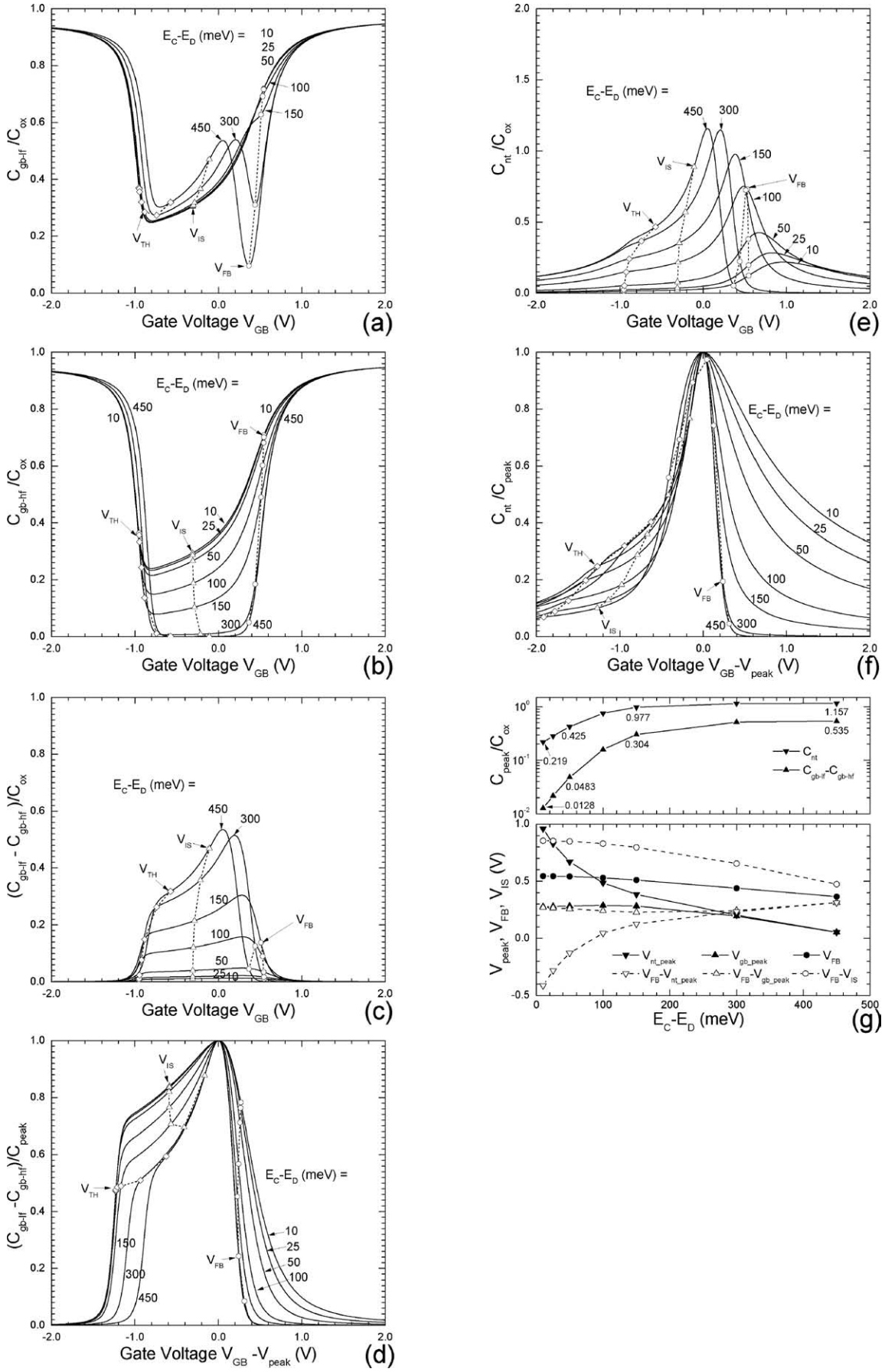

Fig. 3. Capacitance–Voltage characteristics of Si MOS capacitors. (a) Low-frequency capacitance $C_{\text{gb-lf}}$. (b) High frequency capacitance $C_{\text{gb-hf}}$. (c) Low and high frequency capacitance difference, $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) Peak-normalized-voltage-shifted $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (e) Trapping capacitance, C_{nt}. (f) Peak normalized-voltage-shifted C_{nt}. (g) Capacitance and voltage peaks versus donor energy level. Parameters of model Silicon nMOS capacitors: $X_{\text{ox}} = 3.5$ nm, $N_{\text{DD}} = 10^{18}$ cm^{-3}, $T = 300$ K, $g_{\text{D}} = 2$.

meV trap (the model phosphorus donor in Si), and even 21.9% of C_{ox} for the 10 meV trap (some dopant impurities in Ge). The computational processing of the measured difference of the reciprocal capacitance data at high and low frequency is particularly simplified in the elimination of the random baseline due to measurement noises and stray capacitances in the measurement setups and also in device geometry and wiring, because the trapping capacitance has to asymptotically approach zero on both side of the peak. Figure 3(f) gives the lineshape plot of the difference reciprocal capacitance, which are shaper than the difference direct capacitance of Fig. 3(d). The seventh sub-figure, Fig. 3(g), shows the variation of the Capacitance peak magnitudes of both $(C_{gh\text{-}lf} - C_{gb\text{-}hf})/C_{ox}$ and C_{nt}/C_{ox} and their gate voltages at the capacitance peaks as a function of the dopant donor impurity electron trapping energy, $E_C - E_D$. An important feature is that the voltages of the peaks of the reciprocal of the difference reciprocal capacitances or the trapping capacitance (inverted solid triangles) lie below the flat-band voltage (the filled circles) when the trap is deeper than about 90 meV and crosses below for traps shallower than about 90 meV. However, the voltages at the peak capacitance of the difference capacitance, shown in Fig. 3(c), and Fig. 3(g) (the upright solid triangles), are always below the flat-band voltage (the filled circles) or in the weak inversion range.

The remaining four families of seven figures each are given in Figs. 4, 5, 6 and 7 to show the dependences of the CV curves on the remaining four device material parameters (N_{DD}, g_D, x_{ox}, and T). Figures 4(a) to 4(g) show the dopant donor impurity concentration dependences with $N_{DD} = 10^{16}$ to 10^{19} cm^{-3} at $g_D = 2$, the model of phosphorus in Si. The expected $C_{nt\text{-}peak} \propto N_{DD}$ is observed in the line joining the inverted triangles in the upper part of Fig. 4(g). Figures 5(a) to 5(g) show the dependences on the spin-orbital-momentum degeneracies, $g_D = g_s g_r g_k = 2$ to 64, for the model electron trap of phosphorus donor in Si at $E_C - E_D = 50$ meV (or hole bound to the boron acceptor which has about the same binding energy) with a technology-typical concentration of $N_{DD} = 10^{18}$ cm^{-3}. The values of g_D selected, however, are for spacing the curves relatively evenly, not all the possible physical-real values. Figures 6(a) to 6(g) show the dependences on the gate oxide thickness, $x_{ox} = 1.0$ to 5.5 nm, covering the past and latest new technology ranges. They are equivalent electrical SiO_2 thickness for physically much thicker gate insulator of multiple layers of higher dielectric constants than $\varepsilon_{SiO_2} = 3.9$, so that no tunneling current in our theoretical model. Figures 7(a) to 7(g) show the dependences on the device temperature, $T = 4$ to 600 K, again the practical range, which is aimed (i) to exploit the freeze-out of the majority carrier storage capacitance, C_n, to bring out the majority carrier trapping capacitance, C_{nt}, as indicated by the sharp peaks of C_{gb} when T drops below 77 K (the $T = 40$ K and 4 K curves) shown in Fig. 7(a), and (ii) to reveal the presence of the excited states by populating the excited states by heating to thermally excite the bound electron in some phosphorus donor center ground state at $E_C - E_D = 45$ meV to the not-central-cell down-shifted effective-mass ground 1s-states at $E_C - E_D = \sim 30$ meV, since $k_B T_{600} = \sim 50$ meV is significantly larger than the 15 meV central-cell down-shift, giving a fraction of the bound electrons in the excited state of $\exp(-15/50)/[1 + \exp(-15/50)] = 0.43$ or 43% in the excited state, compared with 35% at 300 K.

The general features in the results of the seven sub-figures given in the four families of figures (Figs. 4 to 7) need no further elaboration since they are similar to the corresponding seven parts of Fig. 3 for which, the features or structures in the CV curves and their fundamental and consumer application purposes were explained and these explanations are applicable to Figs. 4 to 7.

4. Summary

The main result from this survey calculation is the increase of the trapping capacitance contribution to the measured Capacitance as the binding energy of the trapped electron increases or the energy level of the trap deepens, because of the lowered masking of the trapping capacitance by the charge storage capacitance of the majority carriers, electrons for the n-Si MOSCs. This suggests the capability of directly observable giant trapping capacitance from the deeper-energy-level donor and acceptor dopant impurities to monitor their presence. For silicon, all four group-V donors (P, As, Sb, and Bi) have rather small electron binding energies or rather shallow energy levels, near the conduction band edge, therefore, the electron trapping capacity in n-Si, C_{nt}, are always significantly masked by the much larger electron storage capacitance, C_n. However, for the four group-III dopant impurity acceptors or hole traps (B, Al, Ga, In), the hole binding energy at the In acceptor is about $E_A - E_V \approx 150$ meV which would give a large and directly observable hole trapping capacitance peak. This was demonstrated by the CV of the deep donor counter-part with $E_C - E_D = 150$ meV among the family of curves in Fig. 3(a), having $(E_C - E_D)$ varied from 10 to 450 meV. But, the structure of the 150 meV C_{gb}–V_{GB} curve in Fig. 3(a) is still rather small, due still to the masking by the much larger majority carrier storage capacitance. These survey results lead to development of novel means to directly reveal the giant trapping capacitance in the terminals required for practical applications, which are described in two future reports[10, 11].

Acknowledgements

This article is dedicated to centenarian Academician Tsai Khi-Rui (Cai Qirui) 蔡启瑞, Professor of Physical and Surface Chemistry at Xiamen University and a pioneer of catalysis science and technology of China.

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[1] Chih-Tang Sah, "Theory of Metal Oxide Semiconductor Capacitor," Technical Report No.1, ∼155 pages and ∼55 figures. Solid State Electronics Laboratory, Electrical Engineering Research Laboratory, University of Illinois, Urbana, Illinois. December 14, 1964. Fourth printing, February 1, 1974. Digital copy available to qualified researchers via email request to the authors.

[2] The hole trapping capacitance was indeed derived during 1961–1964 as reported in Ref. [1] as $C_A + C_{pA}$ in Eq. (16.1.10), defined by the charge-control capacitance definitions, given by Eqs. (16.1.11C) and (16.1.11D), all on page 17 of Ref. [1]. Furthermore, the charge density of the trapped holes on the dopant acceptor impurities was indeed included in the derivation of the gate voltage, given by the electric field equation (16.1.81) on

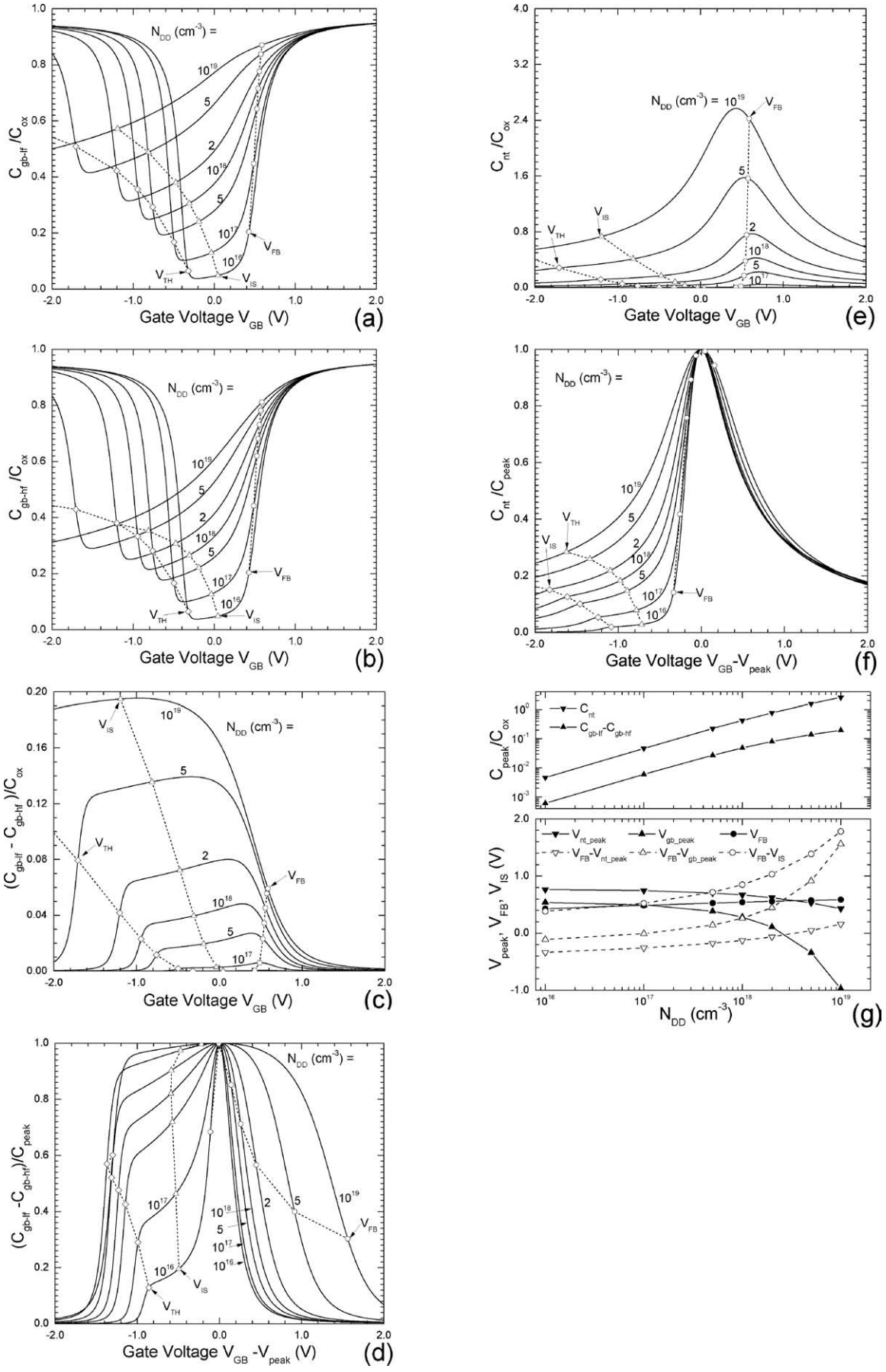

Fig. 4. Capacitance–Voltage characteristics of Si MOS capacitors. (a) Low-frequency capacitance $C_{\text{gb-lf}}$. (b) High frequency capacitance $C_{\text{gb-hf}}$. (c) Low and high frequency capacitance difference, $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) Peak-normalized-voltage-shifted $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (e) Trapping capacitance, C_{nt}. (f) Peak normalized-voltage-shifted C_{nt}. (g) Capacitance and voltage peaks versus dopant concentration. Parameters of model Silicon nMOS capacitors: $X_{\text{ox}} = 3.5$ nm, $T = 300$ K, $E_{\text{C}} - E_{\text{D}} = 50$ meV, $g_{\text{D}} = 2$.

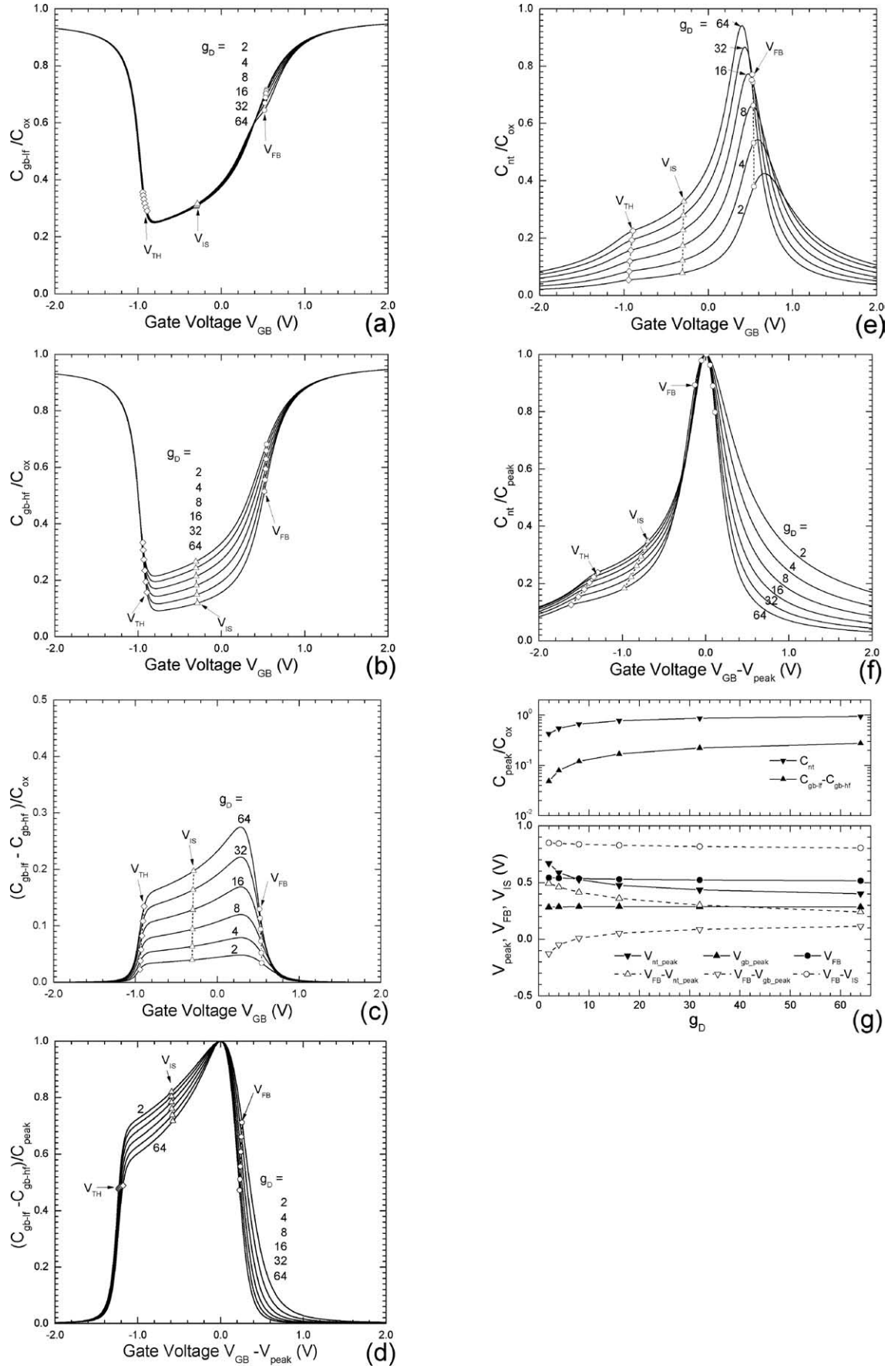

Fig. 5. Capacitance–Voltage characteristics of Si MOS capacitors. (a) Low-frequency capacitance $C_{\text{gb-lf}}$. (b) High frequency capacitance $C_{\text{gb-hf}}$. (c) Low and high frequency capacitance difference, $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) Peak-normalized-voltage-shifted $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (e) Trapping capacitance, C_{nt}. (f) Peak normalized-voltage-shifted C_{nt}. (g) Capacitance and voltage peaks versus donor degeneracy. Parameters of model Silicon nMOS capacitors: $X_{\text{ox}} = 3.5$ nm, $N_{\text{DD}} = 10^{18}$ cm^{-3}, $T = 300$ K, $E_{\text{C}} - E_{\text{D}} = 50$ meV.

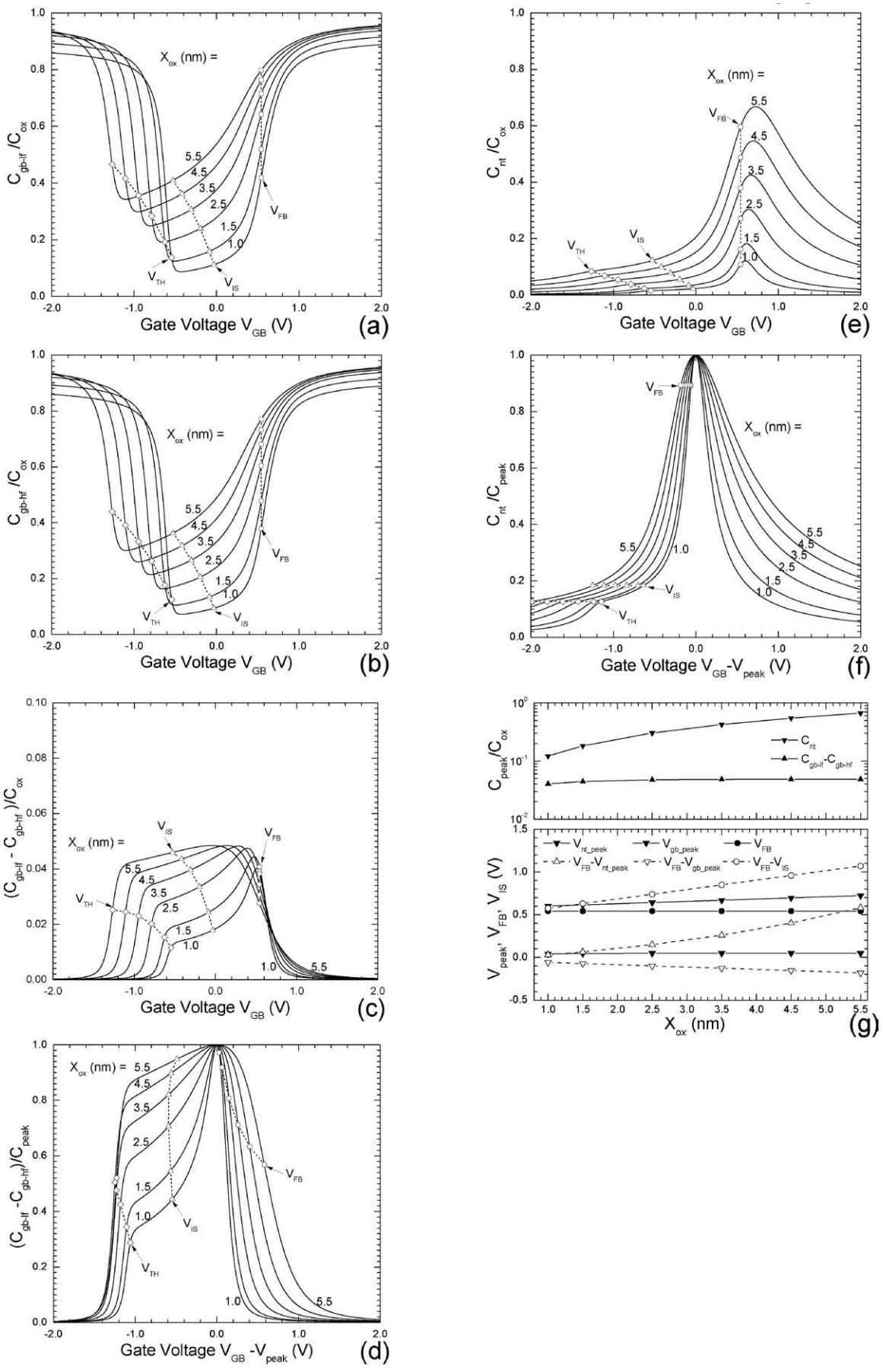

Fig. 6. Capacitance–Voltage characteristics of Si MOS capacitors. (a) Low-frequency capacitance $C_{\text{gb-lf}}$. (b) High frequency capacitance $C_{\text{gb-hf}}$. (c) Low and high frequency capacitance difference, $C_{\text{gb-lf}}-C_{\text{gb-hf}}$. (d) Peak-normalized-voltage-shifted $C_{\text{gb-lf}}-C_{\text{gb-hf}}$. (e) Trapping capacitance, C_{nt}. (f) Peak normalized-voltage-shifted C_{nt}. (g) Capacitance and voltage peaks versus gate oxide thickness. Parameters of model Silicon nMOS capacitors: $N_{\text{DD}} = 10^{18}$ cm^{-3}, $T = 300$ K, $E_{\text{C}} - E_{\text{D}} = 50$ meV, $g_{\text{D}} = 2$.

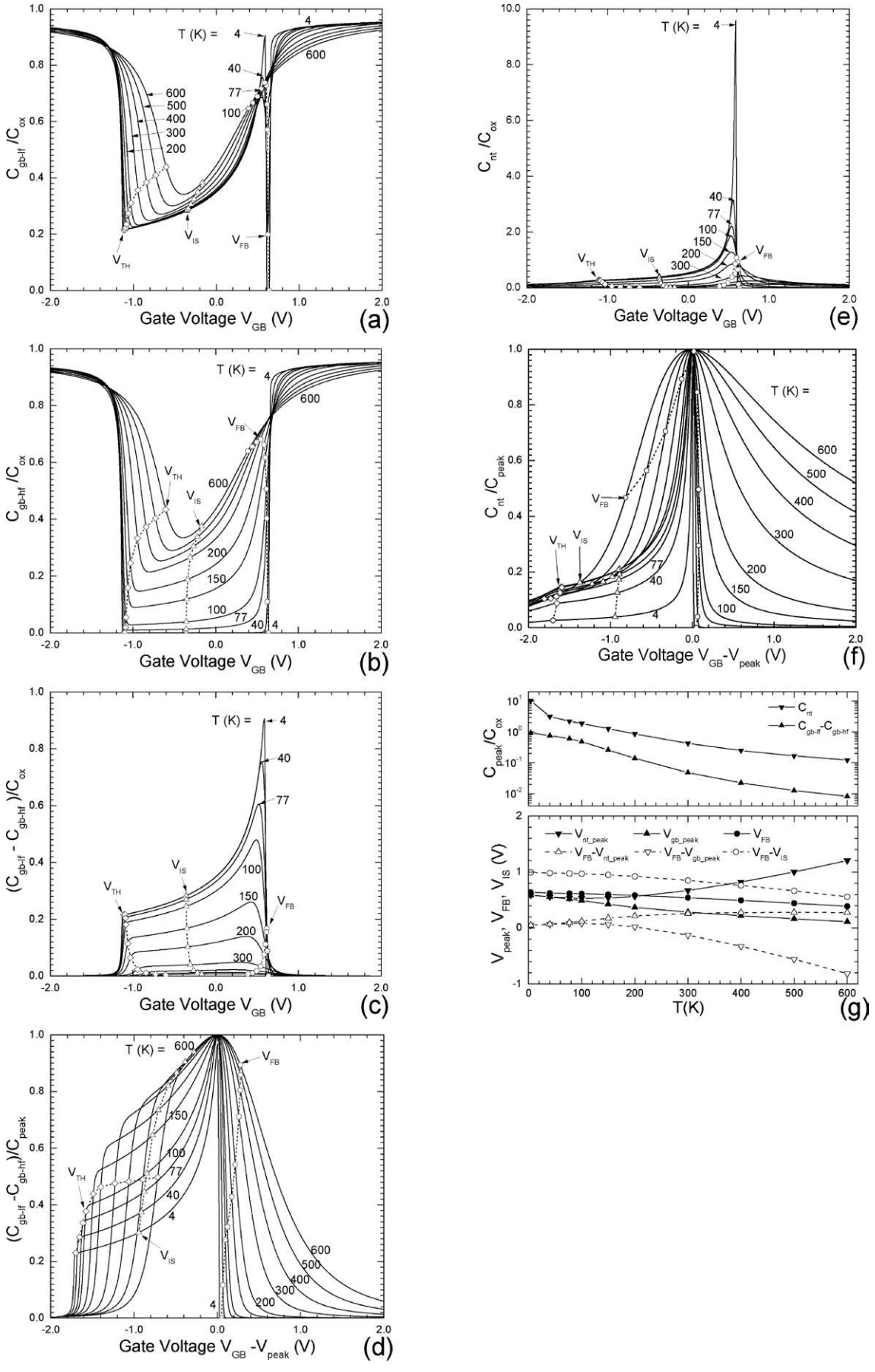

Fig. 7. Capacitance–Voltage characteristics of Si MOS capacitors. (a) Low-frequency capacitance $C_{\text{gb-lf}}$. (b) High frequency capacitance $C_{\text{gb-hf}}$. (c) Low and high frequency capacitance difference, $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (d) Peak-normalized-voltage-shifted $C_{\text{gb-lf}} - C_{\text{gb-hf}}$. (e) Trapping capacitance, C_{nt}. (f) Peak normalized-voltage-shifted C_{nt}. (g) Capacitance and voltage peaks versus temperature. Parameters of model Silicon nMOS capacitors: $X_{\text{ox}} = 3.5$ nm, $N_{\text{DD}} = 10^{18}$ cm^{-3}, $E_{\text{C}} - E_{\text{D}} = 50$ meV, $g_{\text{D}} = 2$.

page 63 of Ref. [1]. In fact, in the evaluation of the MOS capacity given in the 1964 report[1], the hole trapping capacitance C_{pt} (notation used in this paper) $\equiv C_A + C_{pA}$ (notation used in Ref. [1] of 1964) was indeed included as the third part of the semiconductor capacitance given by Eq. (16.1.82) on page 63 of Ref. [1], listed below, with the intrinsic Debye capacitance defined by $C_{Di} = [\varepsilon_{Si}(k_BT/q)/2qn_i]^{1/2}$ where ε_{Si} = permittivity and n_i the intrinsic carrier concentration of the semiconductor, or Si in this case. Boltzmann distribution of the electron and hole concentrations were used. $C_S \equiv C_p + C_n + C_{pt} = C_{Di} \times \text{sign}(U_S) \times \{\sinh(U_S - U_F) + [(1 + e^{U_F - U_A})/(1 + e^{U_F - U_A - U_S})] \times \sinh(U_F)\}/F(U_S, U_F)$, where the normalized electric field was given by Eq. (16.1.81) on page 63 of Ref. [1]. $F(U, U_F) = \sqrt{2} \times \{\cosh(U - U_F) - \cosh(U_F) + \sinh(U_F) \times (1 + e^{U_F - U_A}) \times [U + \log_e(1 + e^{U_F - U_A - U})/(1 + e^{U_F - U_A})]\}^{1/2}$ and the Voltage Equation was given by Eq. (16.1.21) on page 21 of Ref. [1]. $V_{GB} = V_{MS} - (Q_{IT} + Q_{OX})/C_{ox} + V_S + (k_BT/q) \times (C_{Di}/C_{ox}) \times \text{sign}(U_S) \times F(U_S, U_F)$. The interface and oxide charges, Q_{IT} and Q_{OX}, are taken as zero in the present report on trapping capacitances at the bulk traps. The gate-metal/semiconductor (electron) work function difference is given by the usual definition[1], namely the electron work function of the metal in vacuum less the electron work function of the semiconductor in vacuum or the common material, oxide, that replaces the vacuum in Metal/Oxide/Semiconductor. If the thin gate oxide composition is constant, then its work function in vacuum is constant throughout the thin gate oxide, which then give[1, 3] $V_{MS} = V_{MOS} = (W_{Aluminum-Vacuum} - W_{SiO_2-Vacuum}) - (W_{Si-Vacuum} - W_{SiO_2-Vacuum}) = 4.679 - 0.90 - \{[4.029 + (E_C - E_F)/q \pm 0.08] - 0.90\} = 4.679 - 4.029 \pm 0.08 - (E_C - E_I)/k_BT - V_F = 0.65 \pm 0.08 - (E_C - E_I)/q - V_F$. Therefore, the flatband gate-base (or gate-body) voltage (defined as the $V_{GB} = V_{FB}$ when $V_S = 0$) is a function of the dopant impurity concentration P_{AA} or the equilibrium Fermi level in the bulk or body of the semiconductor, V_F which for the asymptotic case of low dopant impurity concentration (N_{DD} or $P_{AA} < \sim 2.5 \times 10^{19}$ cm^{-3} for +20% error in concentration. See Fig. 251.1 on p. 202 of Ref. [3])and very shallow energy level dopant impurity sothat all are ionized (N_{DD} or $P_{AA} < \sim 2.5 \times 10^{17}$ cm^{-3} for ~10% deionization. See Fig. 252.1 on p. 207 of Ref. [3].) isgiven by $V_F - V_I = (k_BT/q)\log_e(P_{AA}/n_i)$ which isusually insufficiently accurate near and at flatband ($V_S \rightarrow 0$) and the solution of the all-term electrical neutrality conditions must be obtained, using Fermi statistics and distribution function for the electrons and holes, $P - P_A - N + N_D = 0$ and $PN = K$ where the equilibrium 'reaction' constant K is the Fermi equivalent of the Boltzmann n_i^2 for low carrier concentrations. (See Section 242 on p.187 of Ref. [3].)

[3] Chih-Tang Sah, Fundamentals of Solid-State Electronics, 1001pp. World Scientific Publishing Company, Singapore. 1991. Values of the numerical constants and additional numerical solutions are given in Ref. [4]. More accurate recent values of the fundamental constants, q, $\hbar$, k_B, and m_0 in the computation presented in this report are taken from Ref. [5].

[4] Chih-Tang Sah, Fundamentals of Solid-State Electronics—Study Guide, 423pp. World Scientific Publishing Company, Singapore. 1993.

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