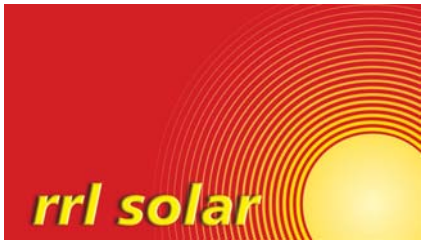
Phys. Status Solidi RRL **10**, No. 6, 443–447 (2016) / **DOI** 10.1002/pssr.201600080



Thermal activation and deactivation of grown-in defects limiting the lifetime of float-zone silicon

Nicholas E. Grant[*,1], Vladimir P. Markevich[2], Jack Mullins[2], Anthony R. Peaker[2], Fiacre Rougieux[1], and Daniel Macdonald[1]

[1] Research School of Engineering, College of Engineering and Computer Science, Australian National University, Canberra ACT 2601, Australia
[2] Photon Science Institute and School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

Received 24 March 2016, revised 7 April 2016, accepted 7 April 2016
Published online 14 April 2016

Keywords float-zone silicon, heat treatment, charge carrier lifetimes, defects, vacancies

[*] Corresponding author: e-mail nicholas.e.grant@warwick.ac.uk, Phone: +44 247 652 8590

By studying the minority carrier lifetime in recently manufactured commercially available n- and p-type float-zone (FZ) silicon from five leading suppliers, we observe a very large reduction in the bulk lifetime when FZ silicon is heat-treated in the range 450–700 °C. Photoluminescence imaging of these samples at the wafer scale revealed concentric circular patterns, with higher recombination occurring in the centre, and far less around the periphery. Deep level transient spectroscopy measurements indicate the presence of recombination active defects, including a dominant center with an energy level at ~E_v + 0.5 eV. Upon annealing FZ silicon at temperatures >1000 °C in oxygen, the lifetime is completely recovered, whereby the defects vanish and do not reappear upon subsequent annealing at 500 °C. We conclude that the heat-treatments at >1000 °C result in total annihilation of the recombination active defects. Without such high temperature treatments, the minority carrier lifetime in FZ silicon is unstable and will affect the development of high efficiency (>24%) solar cells and surface passivation studies.

1 Introduction Float-zone (FZ) silicon is a commonly used material for the fabrication of very high efficiency (>24%) laboratory solar cells, and is used extensively as a control material for comparison with other types of silicon wafers. While float-zoning can lead to a higher purity material when compared to Czochralski (Cz) silicon, the incorporation of intrinsic defects (vacancies and silicon self-interstitials) during crystal growth is unavoidable, whereby the type of intrinsic defect is determined by the growth rate (V) and thermal gradient (G). For example, when FZ crystals are restricted to slow growth rates such that V/G is below a critical value, silicon interstitials are created [1–7]. The silicon interstitials may then form swirl defects which become recombination active and significantly limit the bulk lifetime of minority carriers (τ_{bulk}) [3, 4, 8]. In contrast, when FZ crystals are subject to fast growth rates such that V/G is above a critical value, vacancies are generated which can then aggregate into voids. Although voids are in general less recombination active than swirl defects [3, 4, 8], voids can compromise the mechanical strength of the crystal. Thus, to suppress the formation of voids and swirl defects, FZ silicon crystals are commonly doped with nitrogen during crystal growth [1]. The most common nitrogen defect in crystalline silicon is a pair of interstitial nitrogen atoms, i.e. the nitrogen dimer. It is thought that the nitrogen dimer is electrically neutral in silicon and it interacts effectively with both vacancy- and self-interstitial-related defects so preventing agglomeration of intrinsic defects [1]. On the other hand, this leads to much higher concentrations of un-clustered vacancies and interstitials, which may result in other recombination active centers.

This work aims to extend and consolidate our previous studies on the recombination activity of intrinsic defects

which limit the lifetime of high purity FZ silicon [9, 10]. We examine the activation and deactivation of recombination-active defects by heat-treatments over a wide temperature range of 200–1100 °C. We perform photoluminescence imaging to detect spatial non-uniformities in the bulk lifetime when the defects are activated. Finally, electrically active defects are examined by deep level transient spectroscopy (DLTS).

2 Experiment The samples under investigation were (100) float-zone (FZ) silicon wafers and their diameter was 100 mm. Details of the samples investigated are outlined in Table 1.

The wafers were cleaved into quarters, etched in a 1% HF solution and then RCA cleaned. Following the RCA clean and a subsequent 1% HF dip (to remove the chemically-grown oxide), the samples were loaded into a clean quartz tube furnace and annealed at the set temperature for 30 min in dry oxygen with a flow rate of ~150 l/h. For temperatures higher than 700 °C, there was an additional ramp up and cool down period. The ramp up and cool down rates were ~20 °C/min.

To examine the impact of annealing temperature on the bulk lifetime, minority carrier lifetime measurements were performed using a room temperature hydrofluoric acid surface passivation technique [11, 12].

To investigate the spatial non-uniformity of the bulk lifetime using photoluminescence imaging, some wafers were passivated with a 20 nm atomic layer deposited (ALD) aluminium oxide (Al_2O_3) film. The Al_2O_3 films were deposited at 175 °C using a Beneq TFS200 ALD system. Post deposition, the Al_2O_3 films were annealed in forming gas at 400 °C for 30 min to activate the surface passivation.

For DLTS measurements, 1 mm diameter Schottky diodes were formed on n-type samples by thermal evaporation of Au, and on p-type samples by plasma sputtering of Ti through a shadow mask. A thick layer of Al(Au) was evaporated onto the back side of the samples to form an Ohmic contact. Current–voltage and capacitance–voltage measurements at different temperatures were carried out in order to evaluate the quality of the diodes and to determine the concentration of uncompensated shallow acceptors/donors in the regions probed by DLTS. Deep electronic levels were characterized with conventional DLTS and high-resolution Laplace DLTS (L-DLTS) techniques [13].

The nitrogen concentration in the FZ wafers was determined by secondary ion mass spectroscopy (SIMS) measurements. For samples with an undetectable quantity of nitrogen, we report the detection limit of the system (5×10^{13} cm^{-3}) as the upper limit.

Table 1 FZ materials used in this work. The nitrogen concentration was determined by SIMS and the resistivity is as quoted by the manufacturers.

manufacturer	resistivity (Ω cm)	doping type	nitrogen (cm^{-3})
A	1.5	n	5.0×10^{14}
B (ingot 2)	10	n	3.0×10^{14}
B (ingot 3)	>100	n	4.0×10^{14}
C	5	n	10^{14}–10^{15}†
D	2	p	1.0×10^{15}
E	>100	p	$<5.0 \times 10^{13}$*

† Estimated by the manufacturer but not measured.
* Detection limit of SIMS.

3 Results Figure 1 plots the bulk lifetime versus annealing temperature of FZ silicon wafers taken from 5 different ingots, each of which was sourced from different manufacturers. For each annealing temperature, new samples were used. For the lifetime reported in Fig. 1, an injection level of $\Delta n = 10^{15}$ cm^{-3} was chosen instead of the more usual $0.1 \times N_{doping}$ because such low injection levels could not be measured for some samples (i.e >100 Ω cm). This results in the lifetime of the 100 Ω cm samples being measured at "high" injection levels where some recombination centres will be saturated.

Prior to any thermal treatment, all samples show bulk lifetimes in the millisecond range (1–10 ms), however, these values are well below the Auger limit [14], indicating the existence of grown-in defects which are causing additional bulk recombination. Interestingly, when the silicon wafers are annealed at 200 °C and then 300 °C, some increase in τ_{bulk} is observed for both n- and p-type silicon wafers. This increase in lifetime is consistent with our previous work on deactivation of defects at low annealing temperatures [9], and thus the increase in lifetime as seen in Fig. 1 is not related to surface passivation instabilities.

Figure 1 highlights (light blue region) the temperature range (250–450 °C) over which common dielectric films are deposited or annealed. In many cases, the deposition of dielectric films will not result in bulk lifetime degradation,

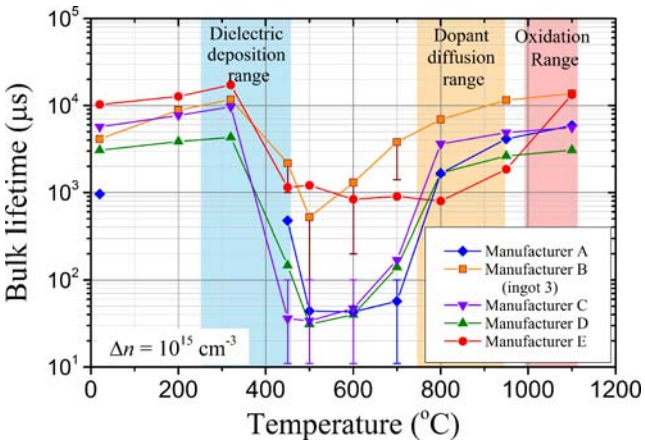


Figure 1 Bulk lifetime (at $\Delta n = 10^{15}$ cm^{-3}) versus annealing temperature for five different FZ silicon ingots. Annealing was performed in dry oxygen for 30 min. Each data point represents a new sample.

however, for temperatures exceeding 400 °C, the bulk lifetime may be severely degraded as evident in Fig. 1. It should be noted that if the dielectric film provides a source of hydrogen, the degradation in bulk lifetime may be prevented or reduced [10, 15].

When the silicon samples were heat-treated in the temperature range 450–700 °C, the lifetime was found to decrease significantly, and in the worst case (5 Ω cm n-type), τ_{bulk} decreased by more than two orders of magnitude. The large error bars for the samples annealed at 450, 500, 600 and 700 °C represent the uncertainty in the true bulk lifetime, as the photoconductance lifetime measurements of these samples were affected by the spatially non-uniform bulk lifetime, as will be shown in the following section. Furthermore, when the lifetime is <100 µs, transient photoconductance measurements become increasingly inaccurate.

To elucidate why a very large decrease in τ_{bulk} is observed, photoluminescence (PL) images of samples annealed at 550 °C were recorded.

Figure 2 depicts a calibrated lifetime image of a FZ 10 Ω cm n-type silicon wafer annealed at 550 °C. The figure clearly demonstrates that the lifetime significantly decreases and becomes spatially non-uniform, as evident by the disc/ring patterns. Such a defect distribution is characteristic for FZ ingots grown with a fast growth rate, whereby *V*/*G* is high in the crystal core and low around its periphery causing a transition from vacancy mode to interstitial mode [1, 2, 5, 16]. We therefore suggest that the central region (lower lifetime region) of the wafer shown in Fig. 2 is dominated by vacancy related defects, while the periphery (higher lifetime region) corresponds to silicon interstitials or defect neutral regions (regions where interstitials and vacancies self-annihilate) [2–5, 7]. It must be mentioned, while Fig. 2 only displays one example, we have observed similar defect patterns in many other annealed FZ wafers.

When the silicon samples were subject to heat-treatments at temperatures ≥800 °C in an oxygen ambient for 30 min, the defect regions as seen in Fig. 2 vanish and do not reappear upon subsequent annealing at 500 °C [17]. Furthermore, from Fig. 1 it can be seen that the bulk lifetime not only recovers, but improves relative to the as-grown lifetime in most cases. These findings indicate that the defect is permanently deactivated during a high temperature oxidation.

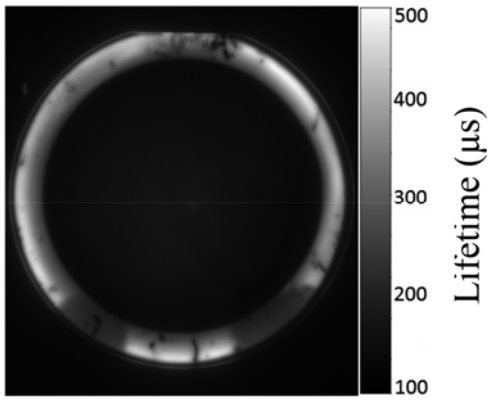


Figure 2 Calibrated lifetime image of a 100 mm diameter FZ 10 Ω cm n-type silicon wafer (manufacturer B (ingot 2)) annealed at 550 °C. The sample was passivated by 20 nm of ALD Al_2O_3.

From Fig. 1, it is interesting to note that the sample which has a nitrogen concentration below the detection limit (red circles), exhibits a different trend in the bulk lifetime with temperature. Although the lifetime does decrease upon heat-treatments at 450–700 °C, the recovery in lifetime does not occur until a temperature of ≥900 °C is achieved. Furthermore, the trend in lifetime is quite different to those samples which contain larger concentrations of nitrogen. One reason for this difference could be a higher void concentration, which can occur when nitrogen lean silicon crystals are pulled quickly [1, 3–7]. Thus, the annealing behaviour of this sample suggests nitrogen may not be a primary defect limiting the lifetime of FZ silicon.

Figure 3 shows conventional DLTS spectra recorded on samples from the central region of p-type FZ silicon wafers with an initial resistivity of 2 Ω cm (wafers from manufacturer D in Table 1); as-grown and subject to a 30 min heat-treatment in oxygen at 500 °C and 1000 °C. In the spectra of the as-grown and 1000 °C annealed samples, only a weak signal due to a trap with the activation energy for hole emission to the valence band (E_h) being 0.47 eV occurs. Annealing at 500 °C resulted in the appearance (spectrum 2 in Fig. 3) of two other peaks with their maxima at ~130 K and 300 K. The E_h values for the corresponding hole traps have been determined as

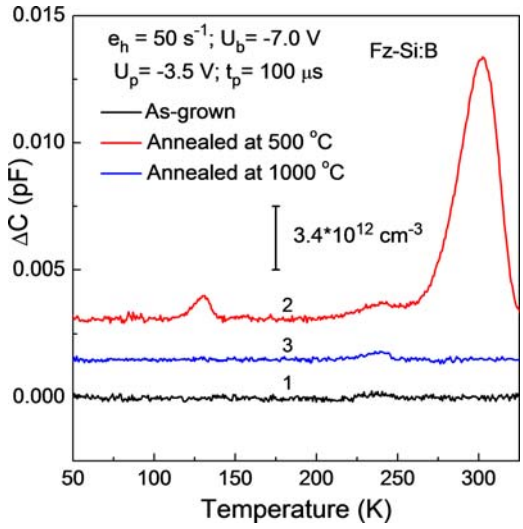


Figure 3 DLTS spectra recorded on p-type FZ silicon samples with a resistivity of 2 Ω cm: (1) as-grown sample; and samples annealed in oxygen ambient for 30 min at (2) 500 °C and (3) 1000 °C. The samples were cut from the central parts of the as-grown and annealed wafers. Measurement settings are given in the graph. Spectra 2 and 3 are shifted on the vertical axis for clarity.

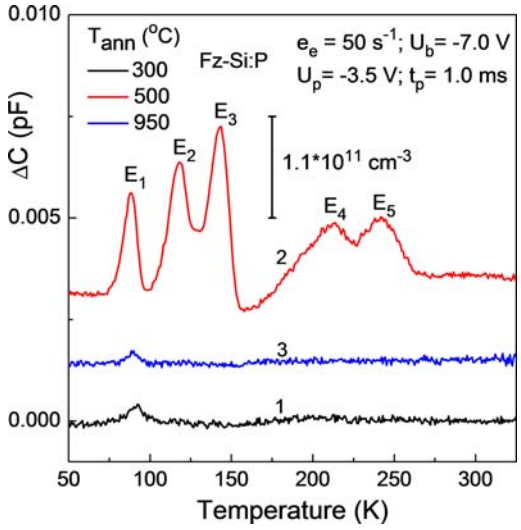


Figure 4 DLTS spectra of n-type FZ silicon samples with initial resistivity of 100 Ω cm annealed in oxygen ambient for 30 min at (1) 300 °C, (2) 500 °C and (3) 950 °C. The samples were cut from the central parts of the as-grown and annealed wafers. Measurement settings are given in the graph. The spectra 2 and 3 are shifted on the vertical axis for clarity. The corresponding electron activation energies for E_1, E_2, E_3, E_4 and E_5 are 0.159 ± 0.002, 0.2 ± 0.002, 0.284 ± 0.002, 0.435 ± 0.004 and 0.434 ± 0.006 eV, respectively.

0.26 ± 0.01 eV and 0.66 ± 0.01 eV, respectively, from Arrhenius plots of T^2-corrected hole emission rates measured with the use of the L-DLTS technique. From a combined analysis of emission and capture data for the 0.66 eV trap, a position of the trap energy level in the gap has been found to be ~0.50 eV above the valence band edge. Bulk concentration of the 0.66 trap is close to 1×10^{13} cm^{-3} in the sample which was annealed at 500 °C. Although we have not carried out direct measurements of the minority carrier capture cross section for the 0.66 eV trap, its concentration and energy level position in the band-gap indicates that this trap is responsible for the degradation of the minority carrier lifetime induced by the heat-treatments of p-type FZ silicon in the temperature range 450–700 °C (Fig. 1).

Figure 4 shows conventional DLTS spectra recorded on samples from the central region of n-type FZ wafers with an initial resistivity of ~100 Ω cm (wafers from manufacturer B in Table 1), which were subject to a 30 min heat-treatment in oxygen at 300, 500 and 950 °C. In the spectra of the samples annealed at 300 °C and 950 °C, only one peak (labeled as E_1 in the graph) with its maximum at ~90 K is observed. This peak is related to emission of electrons from an energy level of a defect to the conduction band. Four other peaks (E_2–E_5) have appeared in the spectrum of the sample, which was annealed at 500 °C. Electronic signatures (activation energy for electron emission to the conduction band (E_e)) for all traps detected have been determined from Arrhenius plots of T^2-corrected for hole emission rates as measured by the L-DLTS technique and are listed in the caption of Fig. 4. Bulk concentrations of the traps detected are in the range from 5×10^{10} cm^{-3} to about 2×10^{11} cm^{-3} in the sample, which was annealed at 500 °C. A detailed study of majority and minority capture cross sections has not been carried out for the E_2–E_5 traps, but from an analysis of their concentrations and positions of energy levels in the gap, it can be suggested that at least one of these traps is responsible for the degradation of the minority carrier lifetime induced by the heat-treatments of this material in the temperature range 450–700 °C (see Fig. 1).

For investigating the spatial distribution of the defects responsible for the lifetime degradation as shown by the PL images in Fig. 2, we have measured DLTS spectra on samples from the edge parts of a 100 Ω cm n-type wafer after a 30 min heat-treatment in oxygen at 500 °C (the same wafer as used in Fig. 4). The magnitude of the signals due to the E_1–E_5 traps (see Fig. 4) was negligible in the spectrum of the sample from the edge part of the wafer, and this is consistent with a higher lifetime around the periphery as seen in Fig. 2.

4 Summary The work presented in this paper has demonstrated that FZ silicon should no longer be assumed to be defect lean nor have the highest and most stable lifetimes. We demonstrated that when commercially available FZ silicon wafers are heat-treated in oxygen at >1000 °C, the vacancy rich regions, which become highly recombination active when subject to heat-treatments of 450–700 °C, vanish and do not reappear upon subsequent annealing at 500 °C (permanently annihilated). The findings of this work offer a simple method to greatly improve the stability and lifetime of FZ silicon, which is essential for the development of very high efficiency solar cells and surface passivation studies.

Acknowledgements This work has been supported by the Australian Renewable Energy Agency (ARENA) fellowships program and the Australian Research Council (ARC) Future Fellowships program. Responsibility for the views, information or advice expressed herein is not accepted by the Australian Government. The work in UK has been supported by EPSRC under a Supergen contract EP/M024911/1.

References

[1] T. Abe, J. Cryst. Growth **334**, 4 (2011).
[2] T. Abe and T. Takahashi, J. Cryst. Growth **334**, 16 (2011).
[3] T. F. Ciszek, T. H. Wang, T. Schuyler, and A. Rohatgi, J. Electrochem. Soc. **136**, 230 (1989).
[4] T. H. Wang, T. F. Ciszek, and T. Schuyler, J. Cryst. Growth **109**, 155 (1991).
[5] V. V. Voronkov, J. Cryst. Growth **59**, 625 (1982).
[6] Topsil Application Note (2014).
[7] K. Tempelhoff and N. Van Sung, Phys. Status Solidi A **70**, 441 (1982).
[8] H. Riemann, A. Ludge, and K. Schwerd, in: High purity silicon VI: Proc. 6th Int. Symp. (Electrochemical Society, Bellingham, WA, 2000), pp. 509–515.

[9] N. E. Grant, F. E. Rougieux, D. Macdonald, J. Bullock, and Y. Wan, J. App. Phys. **117**, 055711 (2015).
[10] F. E. Rougieux, N. E. Grant, C. Barugkin, D. Macdonald, and J. Murphy, IEEE J. Photovolt. **5**, 495 (2015).
[11] N. E. Grant, K. R. McIntosh, and J. T. Tan, J. Solid State Sci. Technol. **1**, P55 (2012).
[12] N. E. Grant, J. Vis. Exp. **107** (2016), DOI: 10.3791/53614.
[13] L. Dobaczewski, A. R. Peaker, and K. Bonde Nielsen, J. Appl. Phys. **96**, 4689 (2004).
[14] A. Richter, S. W. Glunz, F. Werner, J. Schmidt, and A. Cuevas, Phys. Rev. B **86**, 165202 (2012).
[15] P. Hamer, B. Hallam, S. Wenham, and M. Abbott, IEEE J. Photovolt. **4**, 1252 (2014).
[16] M. A. Khorosheva, V. I. Orlov, N. V. Abrosimov, and V. V. Kveder, J. Exp. Theor. Phys. **110**, 769 (2010).
[17] N. E. Grant, F. E. Rougieux, and D. Macdonald, Solid State Phenom. **242**, 120 (2016).