DLTS Study of Defect Distribution in Metal-Porous Silicon-Silicon Structures for Solar Application

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Abstract. The paper presents the results of Deep Level Transient Fourier Spectroscopy (DLTFS) analysis of MOS structures based on a porous p-Si substrate prepared by metal assisted anodic etching. Only three types from five types of samples were appropriate for DLTFS study by their electrical parameters. DLTFS measurements show that metallic contamination occurred in the sample preparation process. The reference, non-etched sample was also subjected to high temperature annealing to form thermal oxide. Au and Zn were confirmed in all DLTFS investigated samples. The impact of anodic etching parameters on defect distribution in the investigated samples is discussed.

INTRODUCTION

Photovoltaic conversion of solar radiation is one of the best ways to extract solar energy and convert it to electrical energy. Power generation cost using solar panels depends on getting as much electricity out of the panels as possible while keeping the manufacturing costs low. Continuous research of new candidates for low cost high efficiency solar cells is an actual task for scientists. One of many improvements is the usage of an antireflective coat to reduce light reflection energy losses. However, these layers are too expensive. A potential solution in this field would be the utilization of "black silicon" or "nanostructured porous silicon" [1].

This promising material makes possible to dispense the coatings, hence a chemical treating of silicon cells producing tiny submicron silicon structures is capable to prevent light reflection and gives a black appearance. Black Si, thus ultralow reflectivity Si surfaces, have been produced by fabrication of nanostructures on Si surfaces, e.g., porous Si using electrochemical etching, stain etching, Si nanowire, etc. In fact, porous Si is formed by an electro-chemical reaction expanding from the surface towards bulk, where the molecules influenced by the electric field migrate in the formed layer. The MOS structure based on a porous p-Si substrate - SiO_2/PS (Porous Silicon) structures are of crucial importance for the formation of pn-type solar cells on crystalline c-Si with acceptable output parameters [2-5]. The thickness of the porous silicon layer, the shape and size of the texture have a positive effect on the conversion efficiency of the solar cell. A desired goal is to tune this electrochemical process, by optimizing the formation parameters of porous silicon [6].

When anodic etching is used, the electrochemical cell does not need any catalyst, hence the etching process is only supported by an external bias. This technically less complicated process gives positive values for a broader application [7]. A negative side of this approach is a higher probability of contamination by electrically active defect states in the etched part of the silicon substrate. Therefore, it is also important to investigate electrically active defects that can have further downgrading affects. Furthermore, the SiO_2/PS structures enable to identify

Applied Physics of Condensed Matter (APCOM 2019)
AIP Conf. Proc. 2131, 020016-1–020016-4; https://doi.org/10.1063/1.5119469
Published by AIP Publishing. 978-0-7354-1873-8/$30.00

recombination processes under the surface. A lot of research efforts are focused on understanding the reasons of the generated defects and the growth methods optimization.

One of the most important versatile spectroscopy methods for investigation of emission and capture processes of charge carriers via detection of deep energy levels (deep traps, defects) in a band gap of semiconductor, thus to determine the origin of impurities, which have significant roles in device evolution is the Deep Level Transient Spectroscopy (DLTS). DLTS has a key role in defect characterization and it satisfies basic requirements of diagnosis, such as accuracy, non-destructive character and sensitivity. The values of the fundamental parameters governing thermal emission and capture on electron deep level -activation energies ΔE_T and capture cross sections σ_T were calculated from an Arrhenius diagram [8]. We are focusing on one of digital DLTS modifications, hence the DLTFS method (Deep Level Fourier Transient Spectroscopy [9]). This modification was developed according to increasing needs of high sensitivity, reliability and accurate results.

This paper introduces DLTS study of the SiO_2/PS structures based on the porous p-Si substrate using the anodic etching method in the electrochemical cell without a metallic cathode with various anodization voltages, currents and times. This study was realised with aim to contribute to optimize the parameters of the electrochemical formation of porous silicon.

EXPERIMENTAL

Five types of SiO_2/PS structures labelled as S3/ 7/ 1-5 prepared with various anodization voltages, currents and times as shown in **TABLE 1** were investigated. A p-type (100)-oriented boron-doped silicon substrate with resistivity 8-12 Ωcm was used to prepare the samples. The thickness of the Si substrate is 600 to 650 μm. Upon completion of the process of porous Si surface formation, the samples were subjected to oxidation by annealing in oxygen at 850 °C for 10 minutes at atmospheric pressure. The gates of the MOS structures were prepared by vapour deposition of Al with an area of 0.318×10^{-6} m^2. From the back of the Si wafer, an ohmic contact was created by vapour deposition of Al on the whole surface of the wafer. Prior to measuring the current and capacitance properties, the MOS structures were stabilized by annealing in a forming gas (90% N_2 + 10% H_2) at 450 °C for 30 minutes. From the *C-V* curve **FIGURE 1** of the reference structure S3/ 7/ 1, the thickness of SiO_2 was determined to be approx. 14 nm [10]. The flat band voltage $V_{FB} \sim$ -3 V, determined from the *C-V* curve **FIGURE 1** of the structure S3/ 7 / 4 suggests a relatively large positive defect charge in the oxide and at the interface with silicon [10].

TABLE 1. Investigated Samples with Various Formation Conditions of the Porous Surface of Silicon

Sample of p-Si	**Formation**	**Etch conditions**		
		Time (s)	**Voltage** (V)	**Current** (mA)
S3/ 7 / 1	Reference	0	0	0
S3/ 7 / 2	PS	15	24.6	0
S3/ 7 / 3	PS	30	24.6	0
S3/ 7 / 4	PS	60	13.6	50
S3/ 7 / 5	PS	90	13.6	50

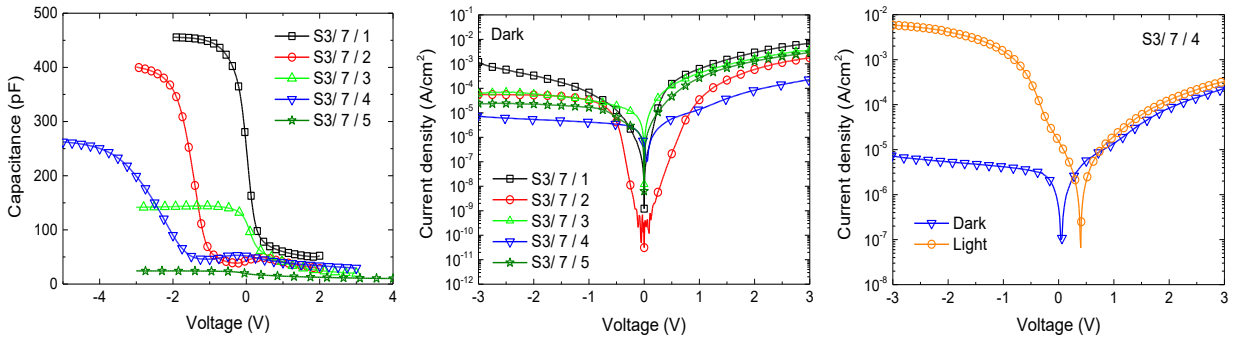

FIGURE 1. (a) *C-V* curves of samples (S3/ 7 / 1-5) prepared by anodization under different conditions, (b) *I-V* curves of samples (S3/ 7 / 1-5) prepared by anodization under different conditions, (c) *I-V* curves measured on sample S3/ 7 / 4 with a PS layer in the dark and under illumination [10].

From current measurements in the dark and under illumination (**FIGURE 1** (c)), the photovoltaic response was recorded only for sample S3/ 7 / 4 with an open circuit voltage of 0.45 V. The total current was significantly affected by indirect tunnelling through interface traps (Trap Assisted Tunnelling). The current flow of light-generated carriers is strongly influenced by recombination of the charge carriers, depending on the density and position of the deep energy levels in the Si volume and the density and energy distribution of interface traps. Based on C-V measurements (**FIGURE 1**), it was decided that the DLTFS study would be carried out only on the most relevant type of samples S3/ 7 / 1, S3/ 7 / 2 and S3/ 7 / 4. Electrically active traps were identified by the capacitance DLTFS method. DLTS measurements were performed in the temperature range from 85 to 420 K using the BIORAD DL8000 measuring system equipped with Fourier transform analysis of measured capacitance transients.

RESULTS AND DICSUSSION

FIGURE 2 displayed typical DLTS spectra measured on samples S3/ 7 / 1, S3/ 7 / 2, and S3/ 7 / 4 at different measurement conditions. We detected six deep energy levels (hole like defects), the parameters and corresponding origin in Silicon (Au, Zn, Fe, Pd-Fe, Ti a Cu [11]) are listed in graphs for each sample **(FIGURE 2)**.

The results of DLTFS study show a large impact of the DLTFS measurement alone on the concentration of defects in the measured structures. Each measurement affects to the state of localized charges in the sample, but at the same time a part of the defects are annealed, resulting in a change in defect concentration in the sample. After that the defect concentration is only qualitative, values are influenced by the length of time have to relax between measurements. The highest defect concentration at the same conditions was measured in sample S3/ 7 / 2.

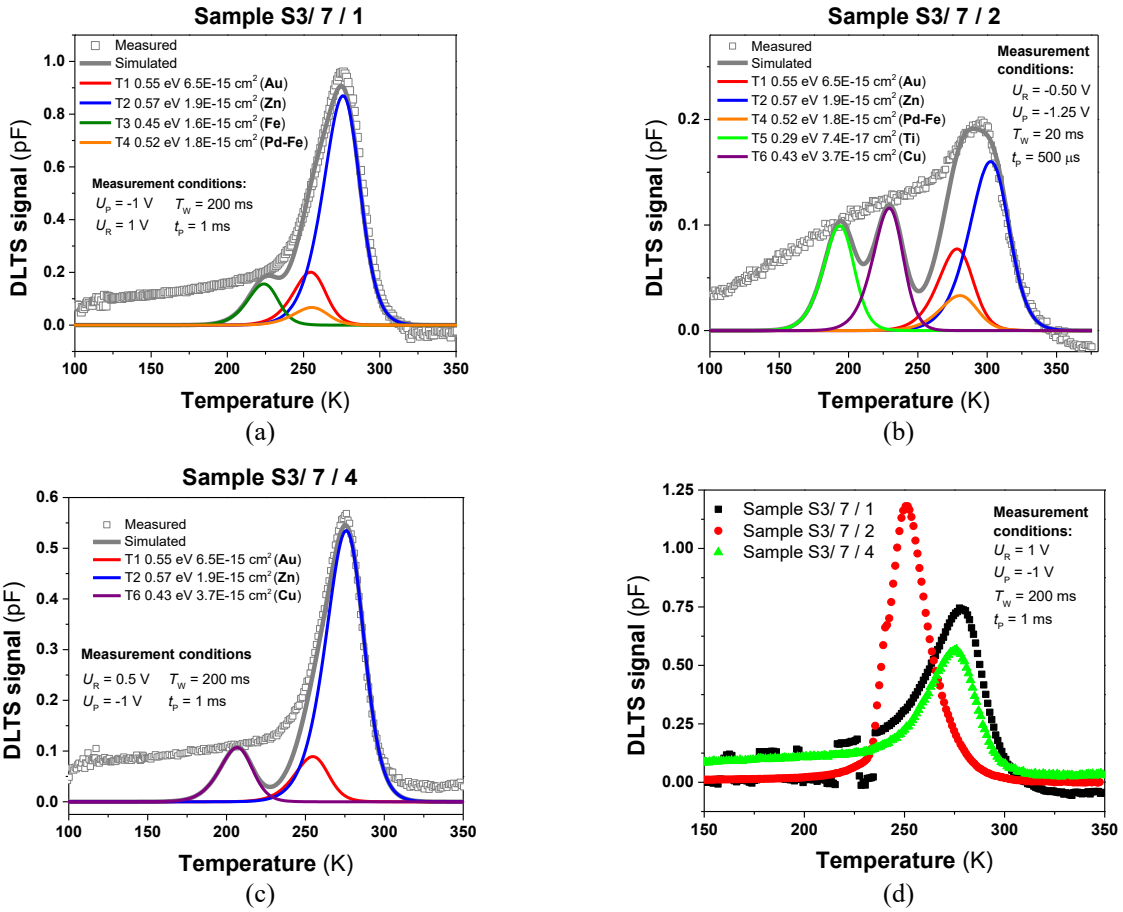

FIGURE 2. Deep levels identified in investigated samples (measured DLTFS spectrum, values of activation energy and cross captures with simulated curves and measurement conditions parameters): (a) S3/7/1, (b) S3/7/2, (c) S3/7/4 and (d) comparing of DLTFS signals of all samples for the same measuring conditions - the highest concentration of the sample defects was in S3/7/2.

We detected contamination by hole type impurities (identification of Au, Zn, Fe, Pd-Fe, Ti a Cu) after high temperature annealing in an oxidation atmosphere. As seen in **FIGURE 2**, we identified deep levels of gold (traps T1 activation energy $\Delta E_T = 0.547$ eV and capture cross-section $\sigma_T = 6.5\times10^{-14}$ cm^2) and zinc (traps T2 activation energy $\Delta E_T = 0.567$ eV and capture cross-section $\sigma_T = 1.9\times10^{-15}$ cm^2) in all examined samples. The reference, non-etched sample was also subjected to high temperature annealing to form thermal oxide. For the etched and subsequently annealed sample, deep level T1 was found with the same activation energy as in the reference sample but with a lower signal amplitude. DLTFS measurements show that metallic contamination occurred in the sample preparation process. This can be caused by formation of an accumulated layer of minority electrons below the gate. Under such conditions, with the assumption of a lower density of interface traps and the presence of an accumulated layer of minority electrons, suitable conditions were achieved for the existence of the photovoltaic phenomenon.

CONCLUSION

This paper presents the results of a DLTFS study of three types of MOS structures based on a porous p-Si substrate. The observed DLTFS results show that in our case the highest influence on the quality of the structures was the size of the electric voltage during etching. Sample S3/7/4 was etched four times longer as S3/7/2 and 50 mA flowed through it, and determined concentration of defects in S3/7/4 is much smaller as S3/7/2 at the same measuring conditions. Gold and zinc were found in all 3 samples. As sample S3/7/1 was not etched, we assume that gold and zinc contamination occurred before the black silicon preparation process. As optimal conditions of anodic preparation of the PS structure after thermal oxidation from investigated samples we consider sample S3/7/4 created on p-type silicon with anodization voltages 13.6 V, currents 50 mA and times 60 s.

ACKNOWLEDGMENTS

The work has been supported by the Scientific Grant Agency of the Ministry of Education, Science, Research and Sport of the Slovak Republic and of the Slovak Academy of Sciences (projects APVV-15-0152 and VEGA 1/0668/17).

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