

Physica B: Physics of Condensed Matter
Interpretation of the I-V, C-V and G/ω-V characteristics of the Au/ZnS/n-GaAs/In structure depending on annealing temperature
--Manuscript Draft--

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Keywords:	Schottky Diode; ZnS; Electrical Characteristics; Dielectric properties; Spray Pyrolysis
Abstract:	The ZnS , which is included in the Au/n-GaAs/In diode as the interface layer, was grown on the n-GaAs substrate by the spray pyrolysis method. First, to reveal some structural, surface and electrical properties of the ZnS thin film, XRD, SEM and absorption measurements were taken. Later, the electrical measurements of the Au/ZnS/n-GaAs/In structure were taken at T=300K, and various parameters of the structure were calculated with different methods. In order to reveal the effects of annealing temperature on the electrical measurements of device , the device was annealed at 100, 200 and 300 °C, respectively, in nitrogen gas environment. The characteristic parameters were calculated again and the results were interpreted comparatively. With the help of the C-V and G/ω-V characteristics, the dependence on bias voltage and frequency of the parameters such as dielectric constant, dielectric loss, loss tangent, electrical conductivity and electric modulus of the diode has been revealed.

Ref. No: PHYSB-D-20-02379

The manuscript title: Interpretation of the $I-V$, $C-V$ and $G/\omega-V$ characteristics of the $Au/ZnS/n-GaAs/In$ structure depending on annealing temperature

Authors: Ali Baltakesmez, Betül Güzeldir and Mustafa Sağlam

Thank you very much for your carefully review on our manuscript. The paper has been revised throughout. Our answers on your comments are as follows:

Reviewer # 1:

Authors are bringing into community the interesting experimental results. But physical reasons of results are not discussed enough. I recommend a major revision. I have following comments.

1. The information about annealing time is absent.

Authors answer:

Au/ZnS/n-GaAs/In structure was annealed for 5 minutes in the annealing furnace set at 100, 200 and 300 °C, respectively. Information about the annealing time is also provided in the text (page 1, abstract section, line 19 and page 4, experimental procedure section, line 18).

2. How does the XRD pattern indicate nano crystalline nature? The peak 28.3 is not broadened enough.

Authors answer:

As is known, XRD is an extremely important method in the field of material characterization to obtain information on an atomic scale from both crystalline and non-crystalline (amorphous) materials. It can be used to determine the phase content in many minerals and materials. Experimentally obtained diffraction pattern of the sample is compared with Joint Council Powder Diffraction (JCPDS) data for Standards. This gives information of different crystallographic phases, the relative abundance and preferred orientations. From the width of the diffraction peak, average crystallite size (D) in the film can also be estimated. Inter-planar spacing d can be calculated from the X-ray diffraction profiles using the Bragg equation. Using the d -values the set of lattice planes ($h k l$) which identified from the standard data and the lattice parameters can be calculate using the well-known relations for the tetragonal systems. The crystallite size can be evaluated using Debye-Scherrer's formula. The sharpness of the diffraction peaks suggests a good crystallinity of the films.

Therefore, taking into account the justified criticism of the referee, "nano crystalline nature" in the XRD comment on page 4 was removed from the text.

3. The accuracy of parameter determination (e.g., Fig.5, Fig.8) is not specified.

Authors answer:

The details of the calculation of parameters such as turn-on, leakage current, rectification ratio, ideality factor, barrier height, series resistance, diffusion potential, concentration of

donor atoms and Fermi level are widely covered in the literature, so they are not detailed in this article. At the same time, our research group has many publications on the calculation of these parameters. All of the parameters we used in our study were meticulously calculated within experimental errors. Since the volume of the prepared article was very large and many parameters were examined, no additional error calculation was made.

4. The voltage of rectification ratio determination is not specified.

Authors answer:

The voltage of rectification ratio determination was chosen as 0.7 Volts for forward and reverse bias and the values have been revised due to calculation error in the normalization process (Fig. 5(a)). This value is also presented in the text, at the page 6, lines 19-21 as follows:

The rectification ratio values of the Au/ZnS/n-GaAs/In structure were determined as the ratio of the forward bias current to the reverse bias current at the application voltage of 0.7 V for each annealing temperature.

5. Using of equation $n=(q/kT)(dV/d\ln I)$ leads to dependence of ideality factor on voltage. What voltage value was used to determine the ideality factor in the paper?

Authors answer:

As is known, the ideality factor is calculated by using the slope of the linear region of the forward bias $\ln(I) - V$ graph using the $n=(q/kT)(dV/d\ln I)$ equation. In our sample, voltage ranges corresponding to linear regions for D0, D1, D2 and D3 (for as-deposited and each annealing temperature) were determined as 0.06-0.3 V.

6. Fig. 1(a) shows the inhomogeneity of ZnS thin film. But spatial inhomogeneity of barrier height is not discussed. For example, a change in the visible barrier height after annealing may be associated with increase in film homogeneity, rather than with metallurgical reactions.

Authors answer:

As is known, the room temperature analysis of Schottky barrier diodes based on I-V characterization enables the extraction of several important parameters such as ideality factor, barrier height and series resistance of the Schottky diodes, but it doesn't provide detailed information about the electron transport mechanism or the nature of the barriers formed at the metal-semiconductor interface. Temperature dependent current-voltage measurement is a much more effective tool in characterizing the electron transporting mechanisms in the rectifier contacts. However, this article focuses on the interpretation of the I-V, C-V and G/w-V characteristics of the *Au/ZnS/n-GaAs/In* structure at room temperature depending on the thermal annealing performed at low temperatures. Therefore, the spatial inhomogeneity of the barrier height is not considered. The spatial inhomogeneity of the barrier height is not addressed, as the article is sufficiently long and detailed as it is.

Nevertheless, comments on metallurgical reactions have been reinterpreted as follows at the recommendation of the referee (page 7, lines 11-20):

The increase in barrier height up to 200 °C thermal annealing may be associated with increase in film homogeneity. In other words, voids and cracks, which are rarely found on the surface of the ZnS film, may have decreased in thermal annealing up to 200 °C and thus the surface homogeneity of the film may have increased. The decrease in the defects and interfacial states in the interface region depending on film surface homogeneity can be seen as the reason for the increase in barrier height of the structure. Conversely, the decrease in barrier height in thermal annealing at 300 °C may be most likely associated with the deterioration of the surface homogeneity of the film, possibly due to changes in film stoichiometry, and hence renewed defects and interface conditions.

7. On my humble opinion, the log-scale in frequency axis will be better in Fig. 8.

Authors answer:

Considering the recommendation of the referee, the frequency axes of the Figure 8 graphs are arranged in logarithmic scale and are presented in the article as below:

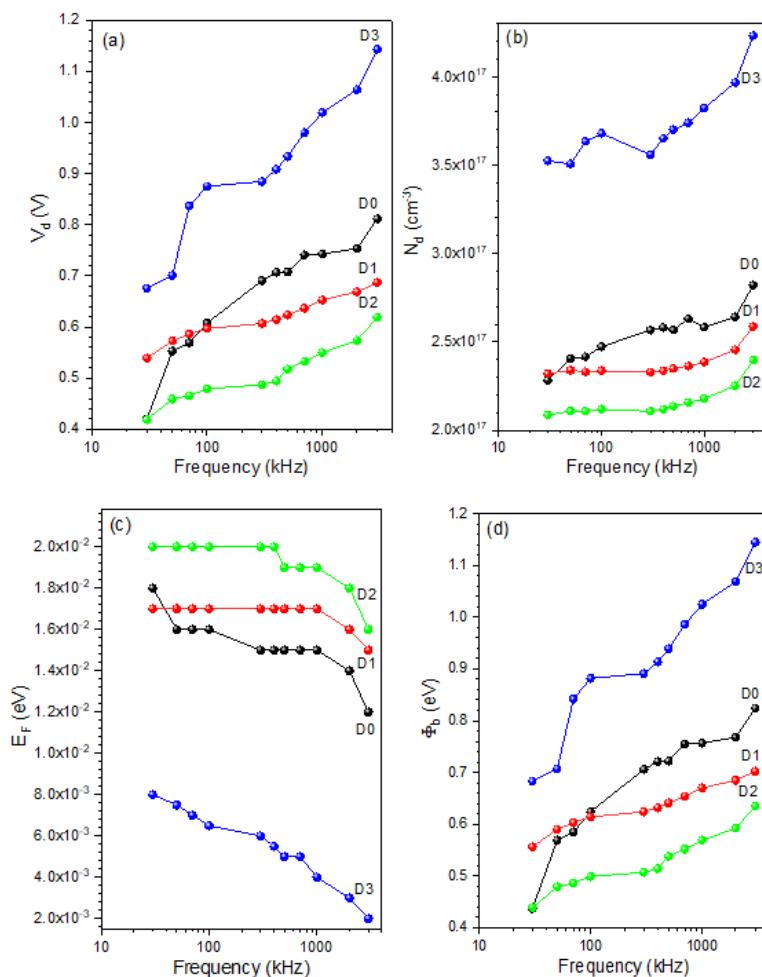


Figure 8. The changes of the V_n , N_d , Φ_b and V_d values obtained from the C^2 -V characteristics depending on thermal annealing and measurement frequency for (a) D0, (b) D1, (c) D2 and (d) D3.

8. It is stated at page 9 " As can be clearly seen from these graphs [Fig.9], the measured G/ω were quite sensitive to applied bias voltage and frequency especially in the depletion region." But it is not evident. The reverse voltage leads to increase in depletion region, but reverse characteristics are identical for all frequencies, all samples, all voltage values. Besides, the statement "the G/ω values depending on the frequency in D0, D1 and D2 are almost the same, in D3 the G/ω values has decreased significantly." (page 10) does not reflect a monotonic decrease in G/ω value with increasing of annealing temperature in Fig. 9.

Authors answer:

Considering the justified criticism of the referee, the comments on the figure 9 on page 10 have been changed as follows:

As can be clearly seen from these graphs, the measured G/ω was quite sensitive to applied bias voltage and frequency especially in the positive bias voltages. The G/ω values are decreasing rapidly with increasing frequency. Again, the decrease in the G/ω values with increasing frequency is due to the inability of the interface states to respond to high frequencies. Therefore, the variation of G/ω -V characteristics with frequency may be attributed the existence of interface states [50].

9. It is necessary to substantiate the physical mechanism of "significant changes in the concentrations of the various charges and traps at the ZnS/n-GaAs interface with thermal annealing". Generalities about metallurgical reaction, structural changes or new phases formation do not look convincing and require confirmation by experiment or reference data.

Authors answer:

As the referee pointed out, the following comment on page 11 was omitted from the text because we could not provide sufficient experimental evidence:

"These results can be attributed to significant changes in the concentrations of the various charges and traps at the *ZnS/n-GaAs* interface with thermal annealing at 300 °C (D3). It can be said that thermal annealing of as-deposited the *Au/ZnS/n-GaAs/In* structure can significantly alter the electrical conductivity due to the formation of interfacial layer, formation of new phases at the interfaces, and most importantly interdiffusion between ZnS layer and *n-GaAs*. The important electrical parameters in such structures are very sensitive to changes in interface of the metal-semiconductor junction."

10. The main goals of paper are not clear. Why is the ZnS layer used? Has research shown the advantages of a ZnS layer over other materials?

Authors answer:

The paragraph prepared as follows on the purpose of the article and the importance of the ZnS layer has been added to the introduction section on page 3:

To summarize, a nontoxic ZnS is one of the most important materials for both device applications and basic research. ZnS have outstanding quality for device applications as it is

a material with wide band gap, high dielectric constant, excellent insulating properties, stable chemical structure and direct transition [1-4]. In this study, the ZnS thin film was used as the interfacial layer in the *Au/n-GaAs* junction. These type devices have important application in a wide variety of the optoelectronic, bipolar integrated circuits and high frequency applications. It is well-known that interface properties have a dominant influence on the device performance, reliability and stability. It can be supplied the stability of the barrier height value by means of some process such as the formation of thin layer between metal-semiconductor interface and by annealing the metal-semiconductor contact. It is probable that the ZnS thin film forms a physical barrier between the metal and *n-GaAs* semiconductor substrate, which prevents the metal from directly contacting the *GaAs* surface. Therefore, in this study, it has been used ZnS thin film with this aim in the *Au/n-GaAs* structure.

11. The conclusion "the presence of an interfacial layer and surface states between metal and semiconductor can cause significant fluctuations in both electrical and dielectric properties" is far from original.

Authors answer:

The sentence "As a conclusion, these experimental results show that the presence of an interfacial layer (ZnS) and surface states between metal and semiconductor can cause significant fluctuations in both electrical and dielectric properties" given in the conclusion has been removed from the text.

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Authors: Ali Baltakesmez, Betül Güzeldir and Mustafa Sağlam

Thank you very much for your carefully review on our manuscript. The paper has been revised throughout. Our answers on your comments are as follows:

Reviewer # 2:

Commentary:

I review the manuscript with **PHYSB-D-20-02379** number and written by Baltakesmez et al. In this study, Au/ZnS/n-GaAs/In structures were fabricated and then to investigate their conduction mechanism and interface nature, the I-V and (C-V-f, G/ ω -V-f) characteristics were investigated in very detail at room temperature depending on three different annealing temperatures (100, 200 and 300 °C). They show that that the optimum/best thermal annealing temperature is 200 °C in respect of low ideality factor, low turn-on voltage, low leakage current and minimum and high barrier height, high rectification ratio values. According to me, this manuscript is very well organized, written, scientific, and presented by author as carefully, but there are some typist errors. Therefore, it should be accepted after some these minor corrections were completed by authors:

Comments:

1. The name of sample should be same in the whole manuscript such as structure, diode or Schottky diode. In addition, the used impedance analyzer for impedance measurements may be HP 4192A (5 Hz-13 MHz) LF analyzer not HP 4142A (50 Hz-13 MHz) LF.

Authors answer: The name of the sample has been corrected as a structure throughout the article.

The information about our new impedance analyzer has been corrected as:

The C-V and G/ω -V measurements were performed with HIOKI IM 3536 (4 Hz-8 MHz)/LCR meter at the frequency range 30 kHz-3MHz with DC power supply at room temperature and in the dark.



2. In reference list; C₂₀H₁₂, Al₂O₃, ... should be given as C₂₀H₁₂, Al₂O₃,...

Authors answer: In the references list, C₂₀H₁₂, Al₂O₃,... has been corrected as C₂₀H₁₂, Al₂O₃,....

3. In conclusion “At the same time, the ϵ' , ϵ'' , M', M'', tan δ and σ_{ac} values ... using the G/ ω -V measurements between 30-3000 kHz, (-2)-(4) V, respectively..” should be changed as “.....C-V and G/ ω -V measurements in the frequency range of 30-3000 kHz. Because the measured range of **voltage** for C-V and G/w-V is different. I think that the value of Capacitance goes to negative for high forward biases (\geq 2.4-4.0 V). Especially in GaAs devices, C goes to negative whereas G/w goes maximum (Negative-capacitance/dielectric or conductivity behavior) due to its high-mobility, surface, states, and resistance as observed give some references below:

Authors answer: In conclusion “At the same time, the ϵ' , ϵ'' , M', M'', tan δ and σ_{ac} values ... using the G/ ω -V measurements between 30-3000 kHz, (-2)-(4) V, respectively..” has been corrected as “.....C-V and G/ ω -V measurements in the frequency range of 30-3000 kHz”.

4. In order to see more clearly the C-V plots in Fig. 6(d) and G/w-V plots at Fig. 9 (c,d), they should be opened like others. For example, the max. y-axis in Fig. 6(d) may be given 0.4 nF.

Authors answer: In order to compare the changes in C-V characteristics for D0, D1, D2 and D3, the scale of the vertical axis was taken at the same magnitude in Figure 6 (a), (b), (c) and (d). However, in line with the justified suggestion of the referee, the vertical axis of Figure 6 (d) was expanded and presented in inset of this graph as follow. Similar procedures were also applied to the G/w-V plots in Figures 9 (c) and (d) as follows:

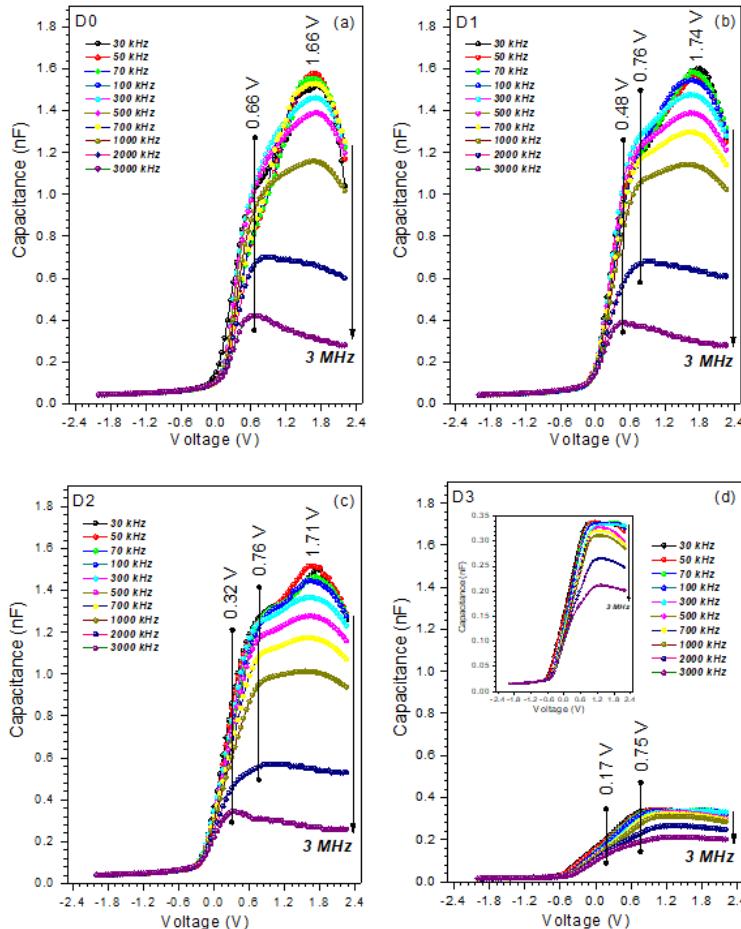


Figure 6. The C - V characteristics of the $Au/ZnS/n$ - $GaAs/In$ structure measured at $T=300$ K in the frequency range of 30-3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. The maximum of the capacitance axis has been changed in the inset in the D3.

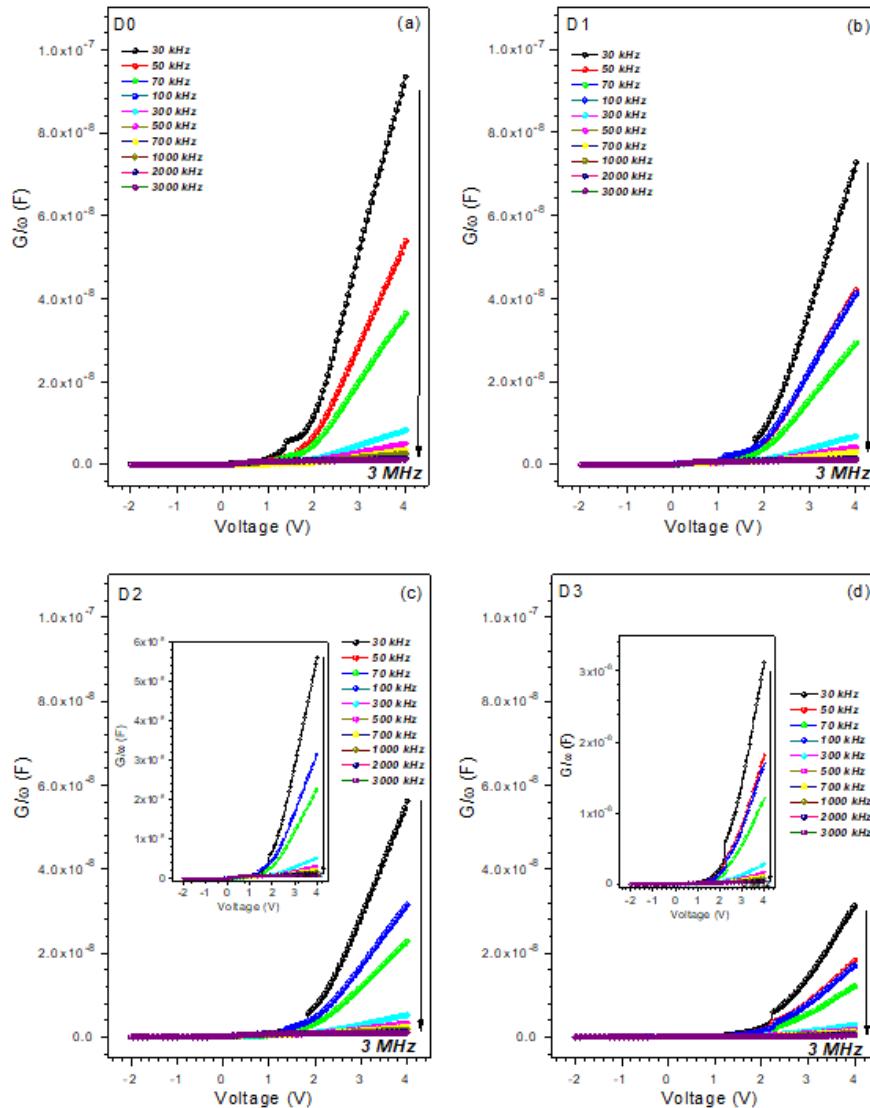


Figure 9. The G/ω - V characteristics of the $Au/ZnS/n$ - $GaAs/In$ structure measured at $T=300$ K in the frequency range of 30-3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. The maxima of the G/ω axis have been changed in the inset in the D2 and D3.

5. In Figs. 13-16 (b), the M'' vs M' plots, the related voltages should be defined such as 0, , 1 V.
 Authors answer: In Figs. 13-16(b), the M'' vs M' plots, the related voltages have been defined.

6. References are enough and related, but some new references on the anomalous peak in the C - V or ϵ' - V plots and conductive behavior may be given as follow or similar:

a) Journal of Physics and Chemistry of Solids 148 (2021) 109740.

- b) Physica B 594 (2020) 412274.
- c) Journal of Physics and Chemistry of Solids 144 (2020) 109523.
- d) Journal of Electronic Materials 48 (2019) 887-897.
- e) Indian J Phys., 93(6) (2019) 739–747.
- f) Physica B 582 (2020) 411979.
- g) Journal of Non-Crystalline Solids 356 (2010) 1006-1011.

Authors answer: The articles given below have been added to the reference list:

Ç. G. Türk, S. O. Tan, Ş Altindal and B. İnem, Frequency and voltage dependence of barrier height, surface states, and series resistance in Al/Al₂O₃/p-Si structures in wide range frequency and voltage, Physica B, 582 (2020) 411979.

B. Akın and Ş. Altindal, On the frequency and voltage-dependent main electrical parameters of the Au/ZnO/n-GaAs structures at room temperature by using various methods, Physica B, 594 (2020) 412274.

S. Karadaş, S. Altindal Yerişkin, M. Balbaşı and Y. Azizian-Kalandaragh, Complex dielectric, complex electric modulus, and electrical conductivity in Al/(Graphene-PVA)/p-Si (metal-polymer-semiconductor) structures, Journal of Physics and Chemistry of Solids, 148 (2021) 109740.

Typographical errors in the text have been corrected as suggested by the referee. The corrections made in the manuscript are shown as red colour.

As a result, this manuscript can be accepted for publication after above some minor typist errors were corrected by authors.

Best regards.

16.11.2020

Prof. Dr. Şemsettin Altindal

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Gazi University, Ankara-TURKEY

Interpretation of the I - V , C - V and G/ω - V characteristics of the $Au/ZnS/n$ - $GaAs/In$ structure depending on annealing temperature

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Abstract

The Zinc Sulphide (ZnS) thin film, which is included in the Au/n - $GaAs/In$ diode as the interface layer, was grown on the n - $GaAs$ semiconductor substrate by the spray pyrolysis method. First, to reveal some structural, surface and electrical properties of the ZnS thin film, XRD, SEM and absorption measurements were taken. It was determined that the ZnS thin film completely covering the surface of the n - $GaAs$ semiconductor substrate has a hexagonal structure and a forbidden energy range of 3.83 eV. Later, the current-voltage (I - V), the capacitance-voltage (C - V) and the conductance-voltage (G/ω - V) measurements of the $Au/ZnS/n$ - $GaAs/In$ structure were taken at room temperature, and various important parameters of the structure were calculated with different methods. In order to reveal the effects of annealing temperature on the I - V , C - V and G/ω - V measurements of $Au/ZnS/n$ - $GaAs/In$ structure, the device was annealed at 100, 200 and 300 °C respectively for 5 min in nitrogen gas environment. The characteristic parameters were calculated again and the results were interpreted comparatively. At the same time, with the help of the C - V and G/ω - V characteristics, the dependence on applied bias voltage and frequency of the parameters such as dielectric constant, dielectric loss, loss tangent, ac electrical conductivity and real and imaginary part of electric modulus of the diode have been revealed. After thermal annealing at 200 °C, it has been determined that the ideality factor, turn-on voltage and leakage current values are at minimum level and the barrier height and rectification ratio values are at maximum level. In other words, it has been revealed that the optimum thermal annealing temperature for this device is 200 °C.

Keywords: Schottky Diode; ZnS; Electrical Characteristics; Dielectric Properties; Spray Pyrolysis

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1. Introduction

II-VI group thin films such as ZnS are getting great attention today as they have potential applications in a wide range of electronic devices such as nano-electronics, optoelectronics and photovoltaics [1-4]. Especially ZnS with a wider band-gap is preferred as a non-toxic buffer layer in solar cells [3]. ZnS, which has a cubic crystal structure in its most stable state, has two types of crystal structures, hexagonal wurtzite and cubic zinc blende [5]. Due to its high dielectric constant, excellent insulating properties and stable chemical structure, ZnS thin films can be also used for the passivation of the semiconductor surface in metal-semiconductor rectifier contacts. Although it can be produced by many methods [6-11], one of the most common methods used in the production of ZnS thin films is spray pyrolysis, because of its simplicity, low cost, high capacity to deposit smooth, uniform and homogeneous thin films over a large area [4,12]. In this method, carrier gas flow rate, solution flow rate, substrate temperature, scanning speed and distance between substrate and nozzle can be easily adjusted to obtain high quality doped and undoped ZnS thin films. Deposition rate and thickness of the films can be easily controlled by changing the spraying parameters.

In metal-semiconductor rectifier junctions, the effects of the interface layer on the electrical characteristics of the junction is well known, and the behavior of the junctions produced using different interface layers has been extensively investigated in recent years [13-22]. When such a thin layer is placed between the metal and the semiconductor, both the electrical and dielectric properties of the junction can be modified. Placing such an interfacial layer in the junction can increase its performance and stability by reducing the magnitude of the interfacial states and dislocations present on the semiconductor surface at the junction interface [23-24]. Generally, the capacitance of these structures is independent of frequency, especially at frequencies greater than 1 MHz. But, due to the frequency dependence of the *ac* signal, there is a capacitance arising from the interface states in addition to the depletion layer capacitance. The capacitive behavior of the junction differs from the ideal case due to the capacitance resulting from the interface states and often referred to as excess capacitance. Since this excess capacitance is strongly dependent on the applied bias voltage and frequency, the *C-V* and *G/ω-V* characteristics of the device are significantly affected. Therefore, in the investigation of the electrical and dielectric properties of the device, the effects of the applied bias voltage and frequency must be taken into account. In low frequency application signals, the frequency response of parameters such as the dielectric constant, dielectric loss and loss tangent is very dominant, and their physical source is still under investigation [25]. At the same time, the values of the parameters that characterize

1 the performance of the junction are highly related to the thickness and morphological structure
 2 of the interface layer used. Therefore, the interfacial layer must be perfectly homogeneous, free
 3 from defects such as pin-holes with high dielectric breakdown, and provide a very high quality
 4 interfacial layer / semiconductor interface without unsaturated bonds [26-27]. It is now well
 5 known that such properties are required to develop novel microelectronic devices.

6 To summarize, a nontoxic ZnS is one of the most important materials for both device
 7 applications and basic research. ZnS have outstanding quality for device applications as it is a
 8 material with wide band gap, high dielectric constant, excellent insulating properties, stable
 9 chemical structure and direct transition [1-4]. In this study, the ZnS thin film was used as the
 10 interfacial layer in the *Au/n-GaAs* junction. These types of devices have important application
 11 in a wide variety of the optoelectronic devices, bipolar integrated circuits and high frequency
 12 applications. It is well-known that interface properties have a dominant influence on the device
 13 performance, reliability and stability. The stability of the barrier height value can be supplied
 14 by processes like the formation of thin layer between metal-semiconductor interfaces or by
 15 annealing the metal-semiconductor contact. It is probable that the ZnS thin film forms a
 16 physical barrier between the metal and *n-GaAs* semiconductor substrate, which prevents the
 17 metal from directly contacting the *GaAs* surface. Therefore, in this study, ZnS thin film has
 18 been used with this aim in the *Au/n-GaAs* structure. Considering the information presented
 19 above, the *Au/ZnS/n-GaAs/In* structure was produced under laboratory conditions in the present
 20 study and its electrical and dielectric properties were investigated depending on the thermal
 21 annealing. The **structure**, whose ideality factor, barrier height, series resistance, leakage current
 22 and rectification ratios were determined **by** the *I-V* measurements, and the dependence of its
 23 parameters such as dielectric constant, dielectric loss, loss tangent, *ac* electrical conductivity
 24 and real and imaginary part of electric modulus on applied bias voltage and frequency was
 25 revealed with the help of the *C-V* and the *G/ω-V* measurements.

26 2. Experimental Procedure

27 In this study, the *Au/ZnS/n-GaAs/In* structure was produced using *n*-type *GaAs* semiconductor
 28 with (100) surface orientation and about $2.5 \times 10^{17} \text{ cm}^{-3}$ carrier concentration and electrical
 29 characteristics such as the *I-V*, *C-V* and *G/ω-V* of this **structure** were investigated depending on
 30 annealing temperature. Before the ohmic contact was made, the *n-GaAs* wafer was chemically
 31 cleaned using the standard cleaning method [28]. To obtain low resistance ohmic contact,
 32 indium metal was evaporated on the back surface of the *n-GaAs* wafer under vacuum (10^{-6}
 33 Torr), and then the *In/n-GaAs* junction was thermally annealed at 450 °C for 3 minutes in

1 flowing nitrogen in a quartz tube furnace. To place the desired interface layer into the **structure**,
 2 ZnS thin film was grown by spray pyrolysis method on the cleaned and polished surface of *n*-
 3 *GaAs* substrate with ohmic contact with indium metal. The spray solution was prepared by
 4 mixing CH₄N₂S and ZnCl₄ chemical materials. S²⁻ and Zn²⁺ ions were sourced from cationic
 5 and anionic precursors. Deionized water served as a solvent. The substrate temperature was set
 6 at 450 °C. The nozzle-to-substrate distance was optimized to be 30 cm. The other deposition
 7 parameters were a solution flow rate of 5 mL/min and 90° angle of the spray nozzle with respect
 8 to the substrate. In addition, air was used as a gas carrier under 3 bar pressure. Next, to
 9 determine the **contact area of structure** and to perform the electrical measurement, Au metal
 10 was evaporated onto the ZnS in a vacuum-coating unit at 10⁻⁶ Torr and the contact area was
 11 determined as 7.85x10⁻³ cm². Thus, the *Au/ZnS/n-GaAs/In* structure was obtained. The process
 12 steps of the manufactured **structure** were summarized in Fig. 1. **The I-V, C-V and G/ω-V**
 13 **measurements of the *Au/ZnS/n-GaAs/In* structure were measured using HP 4140B**
 14 **picoampermeter and HIOKI IM 3536 (4 Hz-8 MHz)/LCR meter at the frequency range of**
 15 **30 kHz-3MHz with DC power supply at room temperature and in the dark., respectively.** In
 16 order to observe the effects of the thermal annealing, the **structure** was annealed at 100, 200 and
 17 300 °C **respectively for 5 min in nitrogen gas environment.** Electrical measurements were
 18 repeated under the same conditions after each annealing process. In the evaluation of the device
 19 characteristics, a naming was made as follows:

- 20 D0: Characteristics of as-deposited *Au/ZnS/n-GaAs/In* structure
 21 D1: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 100 °C
 22 D2: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 200 °C
 23 D3: Characteristics of *Au/ZnS/n-GaAs/In* structure annealed at 300 °C

25 3. Results and Discussion

26 3.1 XRD, SEM and UV-Visible Absorption Analysis of ZnS Thin Film

27 As stated in the introduction part of the article, ZnS thin films can exist in a cubic (zinc-blende
 28 type) or hexagonal (wurtzite) phase. The XRD spectra of ZnS thin film prepared at the substrate
 29 temperature of 450 °C are shown in Fig. 2. **The XRD pattern shows preferential orientation at**
 30 **20 equal to 28.3°.** According to standard JCPDS data (File No. 36-1450), this peak can be
 31 indexed as the (002) reflection of the hexagonal ZnS phase and the other peaks located at
 32 different 2θ angles can be also indexed as reflections (100), (101) and (100), (012), (110) (022)
 33 and (013), respectively. The presence of different peaks in the XRD pattern indicates that the
 34 film has a polycrystalline nature. At the same time, apart from the characteristic peaks of ZnS,
 35 (002) reflection which may belong to hexagonal ZnO was also detected. This situation has been

1 attributed to the occupation of some S sites in the ZnS lattice by oxygen atoms in the air which
 2 is used as carrier gas. This observation suggests that the films are single phase and oxygen
 3 atoms might have substituted S site without changing the hexagonal structure. Oxygen from
 4 carrier gas may diffuse through voids in the film and oxidize during the film formation [1, 29-
 5 30].

6 SEM is a good technique to examine the surface topography of thin films. The surface
 7 microstructure of the ZnS thin film as observed by SEM was shown in Fig. 3 (a). It is seen from
 8 the image captured that the deposited film is uniform throughout the entire surface. The film
 9 covered the surface of the *n*-GaAs semiconductor substrate well, without voids or cracks. It is
 10 clear from the image that there are agglomerations of small sized grains and these grains are
 11 randomly oriented on the substrate, consistent with the polycrystalline observed in the XRD
 12 pattern. At the same time, the closely packed nano-grains showed good adhesion and
 13 homogeneous distribution on the substrate. Therefore, it can be easily said that the ZnS thin
 14 film produced based on morphological findings can be used as a good interface layer in the
 15 metal-semiconductor rectifier junctions.

16 Optical measurements are one of the most common methods used to determine the energy band
 17 gap value of thin films. In this method, the spectrometer gives the film absorption depending
 18 on the wavelength of the light used. The relationship between absorption coefficient (α), band
 19 gap energy (E_g) and photon energy ($h\nu$) is as $\alpha h\nu = B(h\nu - E_g)^{1/2}$ [5]. Where B is an energy
 20 independent constant, but generally depend on the refractive index and the effective masses of
 21 the hole and electron respectively. According to this equation, the energy band gap value of the
 22 thin film can be determined by extrapolating the straight portion of the $(\alpha h\nu)^2$ versus $h\nu$ plot to
 23 $(\alpha h\nu)^2=0$. The absorbance-energy plot of the ZnS thin film obtained by spray pyrolysis method
 24 was presented in Fig. 3 (b). The energy band gap value obtained from this graph corresponds
 25 to 3.83 eV and this value is very close to the energy band gap values obtained for ZnS thin films
 26 in the literature [4, 11, 31-34]. The wide band gap energy (as 3.83 eV) of ZnS thin film can be
 27 shown as a reason why it is preferred as the interface layer in devices such as Schottky barrier
 28 diodes.

29

30 **3.2 Analysis of the *I-V* Characteristics of the Au/ZnS/*n*-GaAs/In Structure Depending**
 31 **on Thermal Annealing**

32

33 The importance of thermally stable and reliable metal-semiconductor junctions in device
 34 technology is well known. The performance of these junctions depends on the quality of the

1 interface between the metal and the semiconductor surface. In such junctions, the quality of the
 2 interface can be increased by processes such as surface passivation and thermal annealing.
 3 Therefore, in order to obtain a high-performance device in this study, both the ZnS thin film
 4 was used as the interface layer in the *Au/n-GaAs* junction and this **structure** was thermally
 5 annealed at low temperatures such as 100, 200 and 300 °C **respectively for 5 min in nitrogen**
 6 **gas environment.**

7 The forward and reverse bias the *I-V* and the *ln(I)-V* characteristics of the *Au/ZnS/n-GaAs/In*
 8 structure were given in Fig. 4 (a) and (b) as a function of thermally annealing, respectively. In
 9 a practice diode, the turn-on voltage can be defined using the point where the diode begins to
 10 transmit exponentially. Using Fig. 4 (a), the turn-on voltage values of the device were calculated
 11 for each annealing temperature and it was observed that it decreased significantly after heat
 12 treatment at 200 °C. The relationship between the turn-on voltage and the annealing
 13 temperature was shown in Fig. 5 (a). That is, the diode voltage required to produce a certain
 14 current was decreased after thermal annealing at 200 °C. At the same time, using the *ln(I)-V*
 15 characteristics given in Fig. 4 (b), the diode leakage current and rectification ratio values were
 16 calculated and their changes depending on the annealing temperature were given in Fig. 5 (a).
 17 **The rectification ratio values of the *Au/ZnS/n-GaAs/In* structure were determined as the ratio of**
 18 **the forward bias current to the reverse bias current at the application voltage of 0.7 V for each**
 19 **annealing temperature.** It was observed that the largest rectification ratio and the smallest
 20 leakage current normalized values were reached by thermal annealing at 200 °C. After thermal
 21 annealing at 300 °C, the leakage current of the diode increased, and hence the rectification ratio
 22 decreased. In other words, considering the turn-on voltage, leakage current and rectification
 23 ratio parameters together, we can say that the appropriate thermal annealing for this structure
 24 is 200 °C. Again, based on the graph given in Fig. 4 (b) and using the thermionic emission
 25 [$n = (q/kT)(dV/d\ln I)$ and $\Phi_b = (kT/q)\ln(AA^*T^2/I_o)$] [35-36], Norde [$\Phi_b = F(V_0) + (V_0/\gamma) -$
 26 (kT/q) and $R_s = kT(\gamma - n)/qI$] [37] and Mikhelashvili [$\beta = qV_m(\alpha_{max} - 1)/kT \alpha_{max}^2$,
 27 $\Phi_b = kT[(\alpha_{max} + 1) - \ln(I_{T_m}/ST^2A^*)]$ and $R_s = V_m/I_{T_m} \alpha_{max}^2$] [38] methods, the ideality
 28 factor, barrier height and series resistance values of the **structure** were calculated as a function
 29 of the annealing temperature. Details on the calculation of these parameters can be found in the
 30 given references. The *F(V)-V* curves obtained from the Norde method were given in Fig. 4 (c)
 31 and the α_{max} -*V* curves obtained from the Mikhelashvili method were also given in Fig. 4 (d).
 32 Variations of the ideality factor, barrier height and series resistance depending on the annealing
 33 temperature were shown in Fig. 5 (b), (c) and (d), respectively. As can be seen from these

graphs, the lowest values of the ideality factor and the highest values of the barrier height were reached in the thermal annealing at 200 °C. In the thermal annealing at 300 °C, while the values of the ideality factor increased, the barrier height values decreased. We can say that the series resistance changes similarly. In practice, since it is desired that the ideality factor is low and the barrier height is high, we can say that thermal annealing at 200 °C is quite suitable for this structure. The fact that the ideality factor value is greater than one indicates that apart from thermionic emission, transport mechanisms such as recombination, tunneling and interface traps, which are effective on the diode, should also be taken into account [39]. The increase in barrier height up to 200 °C thermal annealing may be associated with the increase in film homogeneity. In other words, voids and cracks, which are rarely found on the surface of the ZnS film, may have decreased in thermal annealing up to 200 °C and thus the surface homogeneity of the film may have increased. The decrease in the defects and interfacial states in the interface region depending on film surface homogeneity can be seen as the reason for the increase in barrier height of the structure. Conversely, the decrease in barrier height in thermal annealing at 300 °C may be most likely associated with the deterioration of the surface homogeneity of the film, possibly due to changes in film stoichiometry, and hence renewed defects and interface conditions.

3.3 Analysis of the C-V Characteristics of the Au/ZnS/n-GaAs/In Structure Depending on Thermal Annealing

With the help of the C-V measurements, the nature of the diode's space-charge region can be investigated. Since charges or traps located in the interface are sensitive to the frequency of the applied ac signal, making the C-V measurements depending on the frequency can provide detailed information about this region. Therefore, the forward and reverse bias the C-V characteristics of the as-deposited and annealed at different temperatures the Au/ZnS/n-GaAs/In structure were measured at room temperature in the frequency range of 30-3000 kHz. The C-V characteristics of the device are shown in Fig. 6 for D0, D1, D2 and D3. Since the width of the depletion layer changed with applied bias voltage, the capacitance under the reverse bias increased slowly with decreasing bias voltage. As can be seen in Fig. 6, the C-V characteristics of the as-deposited and annealed structure have also an anomalous peak. These peaks in the capacitance curves may be related to the distribution of deep traps in the gap, series resistance and interface states [40]. The peak values of the capacitance in these characteristics both decreased with increasing frequency and the positions of the peaks shifted towards lower

voltages. The decrease in capacitance with increasing frequency is due to the inability of the interface states to respond to high frequencies. As can be found in many studies in the literature, the shift in the peak positions may be caused by interface states that response differently at low and high frequencies [41-46]. In each graph in Fig. 6, the voltage values corresponding to the peak values of the capacitance are shown on the graphs. While the magnitudes of the peak values of the capacitance depending on the frequency in D0, D1 and D2 are almost the same, in D3 the capacitance has decreased significantly. This change can be attributed to structural changes occurring in the junction with thermal annealing at 300 °C.

In metal-semiconductor rectifier junctions, the space charge region capacitance per unit area is given by the relation $C^{-2} = 2(V_d + V)/q\epsilon_s A^2 N_d$ [35-36]. Where q is the electronic charge, ϵ_s is the dielectric constant of semiconductor, A is the effective area of the junction, N_d is the concentration of ionized donor atoms in the n-type semiconductor and V_d is the diffusion potential at zero bias and is determined from the extrapolation of the linear C^{-2} -V plot to the V axis. From the C^{-2} -V plots, the values of the barrier height can be obtained by the relation $\Phi_b = V_d + V_n$. Where V_n is the potential difference between the Fermi level and the bottom of the conduction band in the neutral region of semiconductor and can be calculated from $V_n = kT \ln(N_c/N_d)$ relation knowing the N_d [47]. The plots of $1/C^2$ as a function of bias voltage for the as-deposited and annealed the Au/ZnS/n-GaAs/In structure are shown in Fig. 7. As can be clearly seen from these graphs, the C^{-2} -V curves displayed linear behavior over a wide range of bias voltage for D0, D1, D2 and D3. Linearity of C^{-2} -V plots indicates a uniform doping density throughout the active regions of samples. The changes of V_d , N_d , V_n and Φ_b parameters obtained from these graphs depending on the annealing temperature and measurement frequency are given in Fig. 8. The obtained ionized donor atoms concentrations were found in the range of 2.282×10^{17} - 2.825×10^{17} cm⁻³ for D0, 2.086×10^{17} - 2.397×10^{17} cm⁻³ for D1, 2.320×10^{17} - 2.586×10^{17} cm⁻³ for D2 and 3.524×10^{17} - 4.232×10^{17} cm⁻³ for D3 for the 30-3000 kHz frequency range, respectively, which is similar to the value provided by the manufacturer. Then the barrier heights were calculated in the range of 0.437 - 0.824 eV for D0, 0.439 - 0.635 eV for D1, 0.556-0.702 eV for D2 and 0.683- 1.145 eV for D3 for the 30-3000 kHz frequency range, respectively. It can be seen from Fig. 8 that the values of barrier height increase with increasing frequency. The higher the barrier height at higher frequencies is due to the ZnS interface layer. Since the presence of a sufficiently thick interface layer leads to a high, intercept point (V_d), higher values of the barrier height at higher frequencies can be attributed to the ZnS interface layer. Other important parameters that may cause this situation can be listed as the maximum electric field

1 in the junction, the depletion region width, interface states and the image force effect [48].
 2 Again, the graphs in Fig. 8 show that the values of parameters such as V_n , N_d , V_d and Φ_b are
 3 strongly dependent on frequency because of the quality of the ZnS interface layer. It can be
 4 clearly stated that the thickness of the interfacial layer placed in the junction and the uniformity
 5 of the barrier height are very important in the C - V and the G/ω - V characteristics.

6

7 **3.4 Frequency and Voltage Effects on The Dielectric Properties and Electrical**
 8 **Conductivity of the Au/ZnS/n-GaAs/In Structure Depending on Thermal**
 9 **Annealing**

10 As known, while conductivity is related to the motion of free electrons, dielectric constants are
 11 related to the behavior of bound electrons. We can say that the dielectric constant is a measure
 12 of the extent to which a substance concentrates the electrostatic lines of flux. Dielectric constant
 13 can also be expressed as the ratio of the amount of electrical energy stored in an insulator **when**
 14 **static** electric field is applied to the dielectric material with respect to the vacuum. Apart from
 15 vacuum, the response of dielectric materials to external fields generally depends on the
 16 frequency of the imposed field. The dependence on this frequency is due to the fact that the
 17 polarization of a material does not respond immediately to the applied field. Therefore, the
 18 dielectric constant is usually expressed as a complex function of the frequency of the applied
 19 field. The response of materials to alternating fields is characterized by a complex dielectric
 20 constant consisting of real and imaginary parts. When an electric field is applied to a dielectric
 21 medium, the current flowing through the real dielectric is the sum of conduction and
 22 displacement currents. While the conduction current is extremely small in good dielectrics, the
 23 displacement current can be thought of as the elastic response of the dielectric material to any
 24 change in the applied electric field. As the magnitude of the electric field increases, a
 25 displacement current flows and, the additional displacement is stored as potential energy in the
 26 dielectric. Unlike, when the electric field is decreased, the dielectric releases some of the stored
 27 energy as a displacement current. There are two types of losses in all dielectrics except vacuum.
 28 One of them is a conduction loss and the other is a dielectric loss. While the conduction loss
 29 represents the flow of actual charge through the dielectric, the dielectric loss is due to the
 30 rotation or motion of atoms or molecules in the alternating electric field.
 31 It is very important to consider the admittance data analysis method in the characterization of
 32 metal-interface layer-semiconductor structures. Investigating the role of interfacial states in
 33 different polarization mechanisms in dielectric materials, taking into account the G/ω - V

1 properties in a wide frequency range, may contribute to a better understanding of possible
 2 current conduction mechanisms through the dielectric medium. At the same time, studying the
 3 dielectric loss can also contribute to understanding the dissipation of energy in the form of heat
 4 through dielectric materials [49]. The capacitance and conductance expressions for such
 5 structures are derived by Nicollian and Goetzberger [50]. The G/ω -V characteristics of the
 6 *Au/ZnS/n-GaAs/In* structure obtained by considering this method are given in Fig. 9 at variable
 7 frequencies and annealing temperatures. As it can be clearly seen from these graphs, the
 8 measured G/ω was quite sensitive to applied bias voltage and frequency especially in the
 9 positive bias voltages. The G/ω values are decreasing rapidly with increasing frequency. Again,
 10 the decrease in the G/ω values with increasing frequency is due to the inability of the interface
 11 states to respond to high frequencies. Therefore, the variation of G/ω -V characteristics with
 12 frequency may be attributed the existence of interface states [50]. The conductance is associated
 13 with the losses originating from the exchange of majority carriers between *ZnS/n-GaAs*
 14 interface and majority carrier band of semiconductor when an *ac* signal is applied to structure
 15 [51].

16 Details of the calculation of dielectric parameters such as complex dielectric permittivity, *ac*
 17 conductivity and complex electrical modulus of diodes with interfacial layer from measured
 18 capacitance and conductance data are widely available in the literature [43,49-52]. Generally,
 19 the dielectric constant is defined as a measure of the energy/charge stored in the material by
 20 electrical polarization. As stated in above references, the complex dielectric constant or
 21 permittivity ϵ can be written as $\epsilon = \epsilon' - i\epsilon''$, considering the real ($\epsilon' = Cd_i/A\epsilon_0$) and
 22 imaginary ($\epsilon'' = Gd_i/\omega A\epsilon_0$) components. Where i is the square root of -1, C is the measured
 23 capacitance, G is the measured conductance, A is the junction area, d_i is the interfacial layer
 24 thickness and ϵ_0 is the permittivity of free space (8.85×10^{-12} F/m). ϵ'' is a measure of how
 25 dissipative or loss a material to an external electric field. This parameter is also called the loss
 26 factor and its value is always greater than zero and is usually much smaller than ϵ' . It can be
 27 said that the energy losses in the material are caused by the orientation of the molecular dipoles
 28 or the conduction of ionic and slow polarization currents. The static permittivity is a good
 29 approximation for altering fields of low frequencies, and as the frequency increases a
 30 measurable phase difference δ emerges between the electric field and the electric flux density.
 31 The $\tan \delta$, which is known as dissipation factor or dielectric loss tangent can be expressed as
 32 $\tan \delta = \epsilon''/\epsilon'$. Another important parameter used to investigate the polarization and relaxation
 33 process in ionic-electronic conducting materials is the complex electric modulus expressed as

1 $M = \frac{1}{\varepsilon} = M' + iM'' = \frac{\varepsilon'}{(\varepsilon')^2 + (\varepsilon'')^2} + i \frac{\varepsilon''}{(\varepsilon')^2 + (\varepsilon'')^2}$. That is, the complex electric modulus, M , is
 2 expressed as the reciprocal of the complex dielectric permittivity, ε . The M' and M'' are the real
 3 and imaginary components of M , respectively. Thus, the relationship between the above
 4 parameters and *ac* electrical conductivity can be expressed as $\sigma_{ac} = \omega C \tan \delta(d_i/A) =$
 5 $\varepsilon'' \omega \varepsilon_0$ [53]. According to this equation, *ac* electrical conductivity is directly proportional to
 6 dielectric loss. Figs. 10, 11 and 12 shows the variation of the ε' , ε'' and $\tan \delta$ as a function of
 7 frequency in the range 30 kHz to 3000 kHz with varied voltages from 0 V to 1 V, respectively.
 8 At the same times, the changes of the ε' , ε'' and $\tan \delta$ with $\ln(\omega)$ are presented in inset these
 9 graphs. It is seen from these graphs that all three parameters are strongly dependent on both
 10 applied bias voltage and frequency. High values of dielectric constant at low and moderate
 11 frequencies can be explained by the interface polarization model. Especially at these
 12 frequencies, dipoles have enough time to align by the electric field before the field changes.
 13 Space charge polarization due to an accumulation of space-charges between interfacial layer
 14 and semiconductor can be also demonstrated by causing high values of ε' at low frequencies
 15 [54]. In the high frequency region, the dielectric constant values are low as the contribution of
 16 atomic and electronic polarization is negligible. That is, dipoles cannot follow the field at high
 17 frequencies. It can also contribute to polarization at charges in interface traps. But, this
 18 contribution is usually negligible at high frequencies. Again, ε' - $\ln(\omega)$ graphs confirm that ε' is
 19 very sensitive to both applied bias voltage and frequency. The dielectric loss factor which
 20 depends upon various structural factors and shows energy dissipation in dielectric material is
 21 due to the relaxation losses at high frequencies. It was previously stated that dielectric loss
 22 occurs when the electrical polarization in the dielectric cannot follow the varying electric field.
 23 An applied field can change this energy difference by producing a net polarization which lags
 24 behind the applied field because the tunnel transition rates are finite. This kind of the
 25 polarization which is not in phase with the applied field is called dielectric loss [55]. As can be
 26 seen from the $\tan \delta$ - $\ln(\omega)$ graphs in Fig. 12, $\tan \delta$ values decrease at low frequencies, remain
 27 almost constant at moderate frequencies and increase with increasing frequency at high
 28 frequencies. It can also be said that $\tan \delta$ values increase with increasing bias voltages. These
 29 results reveal that the $\tan \delta$ parameter is closely related to conductivity. The increase in
 30 electrical conductivity can be explained by the increase in eddy currents. While the values of
 31 the ε' , ε'' and $\tan \delta$ parameters changed in almost the same magnitude and style for D0, D1 and
 32 D2, their values decreased significantly in the case of D3. Therefore, the changes of M' and M''
 33 parameters obtained from ε' and ε'' data in the range 30 kHz-3000 kHz frequency with varied

1 voltages from -2 V to 4 V can be seen in Figs 13, 14, 15 and 16 (a). The M'' - V changes are given
 2 in inset of these graphs. Graphs of M'' versus M' are also given in Figs. 13, 14, 15, 16 (b). The
 3 applied bias voltage and frequency dependence of these modulus values is clearly seen in the
 4 graphs. From these profiles, it can be said that both components of complex electric modulus
 5 are sensitive to changes in frequency. In fact, the observed spectra of ε' and ε'' shown in Figs.
 6 10 and 11 are the indication of such frequency and voltage dependent profiles of M . The values
 7 of M' decrease significantly with increasing forward bias voltages. It can be seen in inset Figs.
 8 13-16 that the M'' - V plots have a **peak** at 0.11, -0.05, -0.21 and -0.05 V applied bias voltages
 9 for D0, D1, D2 and D3, respectively. The values of M' and M'' reach a maximum constant value
 10 corresponding to $M_\infty = \frac{1}{\varepsilon_\infty}$ due to the relaxation process. The frequency dependence of the
 11 complex electrical modulus components can be interpreted by the contribution of interface trap
 12 charges which are effective in depletion and accumulation regions. These results can be
 13 attributed to the specific distribution of charges in the surface states and relaxation times due to
 14 thermal annealing [56-57]. The changes of M'' versus M' are plotted in Figs. 13-16 (b) at discrete
 15 excitation frequencies within 30-3000 kHz. Generally, while M' values increase for all
 16 frequency values, M'' values increase and reach a maximum value and then decrease again. That
 17 is, the changes for M'' versus M' are almost semicircular, and the reduction in the radii of these
 18 diagrams explains the change in the conductivity of the space charge region in the device.
 19 Additionally, semicircle width is the value of the recombination resistance and the maximum
 20 imaginary impedance corresponds to the product from which the electron lifetime was
 21 calculated [52].

22 Figs. 17-20 shows the σ_{ac} - V , σ_{ac} - $\ln(\omega)$ and $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots obtained from the G/ω - V data of
 23 the Au/ZnS/n-GaAs/In structure as a function of applied bias voltage and frequency for D0, D1,
 24 D2 and D3, respectively. As stated above, the *ac* conductivity is directly proportional to
 25 dielectric loss. From these graphs it is clear that, σ_{ac} is dependent on the frequency and applied
 26 bias voltage. The values of *ac* electrical conductivity increase with increasing frequency and
 27 they have a maximum value in accumulation region. This increase is the result of the increasing
 28 eddy current, that cause increases the energy $\tan \delta$ [58]. It can be seen from the σ_{ac} - V plots that
 29 the conductivity is nearly frequency independent at low frequency (up to 500 kHz). However,
 30 as the frequency increases from 500 kHz to 3000 kHz the conductivity becomes more and more
 31 frequency dependent. The basic fact that *ac* conductivity in disordered solids is a function of
 32 increasing frequency is well known from solid state physics. Since transport takes place on
 33 infinite paths, the *ac* conductivity is nearly constant at low frequencies. At regions where the

conductivity is strongly dependent on frequency, the transport is dominated by contributions from hopping infinite clusters. Then, the region of saturation is reached where the high frequency cutoff begins to play a role [59]. Compatible with the change in the G/ω - V plots, while the change of σ_{ac} values in D0, D1 and D2 are almost the same, in D3 its values has decreased significantly. The σ_{ac} - $\ln(\omega)$ plots at various positive bias voltages are given in inset Figs. 17-20 (a) for D0, D1, D2 and D3, respectively. It can be seen from these graphs that σ_{ac} values increase **almost exponentially** with increasing both frequency and positive bias voltages for D0, D1 and D2, respectively. However, in D3, the change in the σ_{ac} values is less. We can say that the increase in σ_{ac} values with increasing frequency is caused by the relaxation phenomenon due to mobile charge carriers and charge hopping mechanism. Likewise, the change in *ac* conductivity with frequency can also be caused by polarization effects [54]. Figs. 17-20 (b) shows the $\ln(\sigma_{ac})$ - $\ln(\omega)$ plots in the range of 0-4 V for D0, D1, D2 and D3, respectively. In all graphs, while there is a single slope with linear change at low voltages, two linear regions with different slopes are observed at large voltages. Based on these results, we can say that *dc* conductivity is dominant in regions where the conductivity is almost independent of frequency, and *ac* conductivity is more dominant in other regions.

4. Conclusions

To investigate the current conduction mechanism and the interface nature of the *Au/ZnS/n-GaAs/In* structure produced under laboratory conditions, the forward and reverse bias *I-V*, *C-V* and G/ω - V characteristics of this structure were studied in the room temperature depending on thermal annealing at 100, 200 and 300 °C, respectively. From XRD, SEM and absorption measurements, it was determined that the ZnS thin film is in hexagonal crystal structure, covers the surface of the *n-GaAs* substrate almost homogeneously and the forbidden energy gap is 3.83 eV. From the analysis of the *I-V* characteristics, it was determined that while the diode turn-on voltage, leakage current and ideality factor values **were** decreased by thermal annealing up to 200 °C, barrier height and rectification ratio values **were** increased. From the *C-V* characteristics, diode parameters such as V_n , N_d , V_d and Φ_b have been calculated based on thermal annealing as a function of frequency. At the same time, both the frequency and voltage dependent of the ϵ' , ϵ'' , M' , M'' , $\tan \delta$ and σ_{ac} values of this structure were investigated by using the ***C-V* and *G/ω-V* measurements in the frequency range of 30-3000 kHz**. It has been observed that all of these parameters are strongly dependent on frequency and voltage. While the values of the ϵ' , ϵ'' and $\tan \delta$ parameters changed in almost the same magnitude and style for D0, D1

1 and D2, their values decreased significantly in the case of D3. These results may be most likely
 2 associated with the deterioration of the surface homogeneity of the film due to changes in film
 3 stoichiometry, and hence renewed defects and interface conditions. The change in *ac*
 4 conductivity with frequency has also been attributed to polarization effects within the device.
 5 It has been revealed that the optimum thermal annealing temperature for this device is 200 °C.

6

7 Credit author statement

8 A. Baltakesmez: Conceptualization, Methodology, Investigation, B. Güzeldir:
 9 Conceptualization, Visualization, Investigation, Writing-review & editing. M. Sağlam:
 10 Conceptualization, Visualization, Investigation, Writing-review & editing, M. Biber:
 11 Methodology, Investigation

12

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1 **FIGURE CAPTIONS**

2 **Figure 1.** Summary of the process steps of the manufactured device

3 **Figure 2.** XRD pattern of ZnS thin film

4 **Figure 3.** a) SEM images of the ZnS thin film on *n*-GaAs substrate, b) The absorbance-energy
5 plot for ZnS thin film

6 **Figure 4.** (a) The forward and reverse bias *I-V*, (b) $\ln(I)$ -*V*, (c) $F(V)$ -*V* (Norde method) and (d)
7 α_{max} -*V* (Mikhelashvili method) characteristics of the Au/ZnS/*n*-GaAs/In structure as a function
8 of thermal annealing

9 **Figure 5.** (a) The changes of the values of turn-on voltage, leakage current and rectification
10 ratio, (b) The changes of the values of the ideality factor obtained from thermionic emission
11 and Mikhelashvili methods, (c) The changes of the values of the barrier height obtained from
12 thermionic emission, Norde and Mikhelashvili methods and (d) The changes of the values of
13 the series resistance obtained from Norde and Mikhelashvili methods with the annealing
14 temperature for the Au/ZnS/*n*-GaAs/In structure

15 **Figure 6.** The *C-V* characteristics of the Au/ZnS/*n*-GaAs/In structure measured at T=300 K in
16 the frequency range of 30-3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. **The maximum of**
17 **the capacitance axis has been changed in the inset in the D3.**

18 **Figure 7.** The C^2 -*V* characteristics of the Au/ZnS/*n*-GaAs/In structure measured at T=300 K in
19 the frequency range of 30-3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3.

20 **Figure 8.** The changes of the V_n , N_d , Φ_b and V_d values obtained from the C^2 -*V* characteristics
21 depending on thermal annealing and frequency for (a) D0, (b) D1, (c) D2 and (d) D3.

22 **Figure 9.** The G/ω -*V* characteristics of the Au/ZnS/*n*-GaAs/In structure measured at T=300 K
23 in the frequency range of 30-3000 kHz for (a) D0, (b) D1, (c) D2 and (d) D3. **The maxima of**
24 **the G/ω axis have been changed in the inset in the D2 and D3.**

25 **Figure 10.** The ϵ' -*V* plots of the Au/ZnS/*n*-GaAs/In structure at various frequencies for (a) D0,
26 (b) D1, (c) D2 and (d) D3. The ϵ' - $\ln(\omega)$ changes are given in inset of the graphs.

27 **Figure 11.** The ϵ'' -*V* plots of the Au/ZnS/*n*-GaAs/In structure at various frequencies for (a) D0,
28 (b) D1, (c) D2 and (d) D3. The ϵ'' - $\ln(\omega)$ changes are given in inset of the graphs.

29 **Figure 12.** The $\tan \delta$ -*V* plots of the Au/ZnS/*n*-GaAs/In structure at various frequencies for (a)
30 D0, (b) D1, (c) D2 and (d) D3. The $\tan \delta$ - $\ln(\omega)$ changes are given in inset of the graphs.

31 **Figure 13.** a) The M' -*V* and M'' -*V* plots of the Au/ZnS/*n*-GaAs/In structure as a function of
32 voltage at various frequencies b) Changes of M'' versus M' for D0.

33 **Figure 14.** a) The M' -*V* and M'' -*V* plots of the Au/ZnS/*n*-GaAs/In structure as a function of
34 voltage at various frequencies b) Changes of M'' versus M' for D1.

35 **Figure 15.** a) The M' -*V* and M'' -*V* plots of the Au/ZnS/*n*-GaAs/In structure as a function of
36 voltage at various frequencies b) Changes of M'' versus M' for D2.

37 **Figure 16.** a) The M' -*V* and M'' -*V* plots of the Au/ZnS/*n*-GaAs/In structure as a function of
38 voltage at various frequencies b) Changes of M'' versus M' for D3.

39 **Figure 17.** For D0 at T=300 K a) The σ_{ac} -*V* plots of **structure** depending on the frequency. The
40 σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ -
41 $\ln(\omega)$ plots in the range of 0-4 V of **structure**.

42 **Figure 18.** For D1 at T=300 K a) The σ_{ac} -*V* plots of **structure** depending on the frequency. The
43 σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ -
44 $\ln(\omega)$ plots in the range of 0-4 V of **structure**.

45 **Figure 19.** For D2 at T=300 K a) The σ_{ac} -*V* plots of **structure** depending on the frequency. The
46 σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ -
47 $\ln(\omega)$ plots in the range of 0-4 V of **structure**.

48 **Figure 20.** For D3 at T=300 K a) The σ_{ac} -*V* plots of **structure** depending on the frequency. The
49 σ_{ac} - $\ln(\omega)$ changes at various positive bias voltages are given in inset of the graph. b) The $\ln(\sigma_{ac})$ -
50 $\ln(\omega)$ plots in the range of 0-4 V of **structure**.

Figure 1.

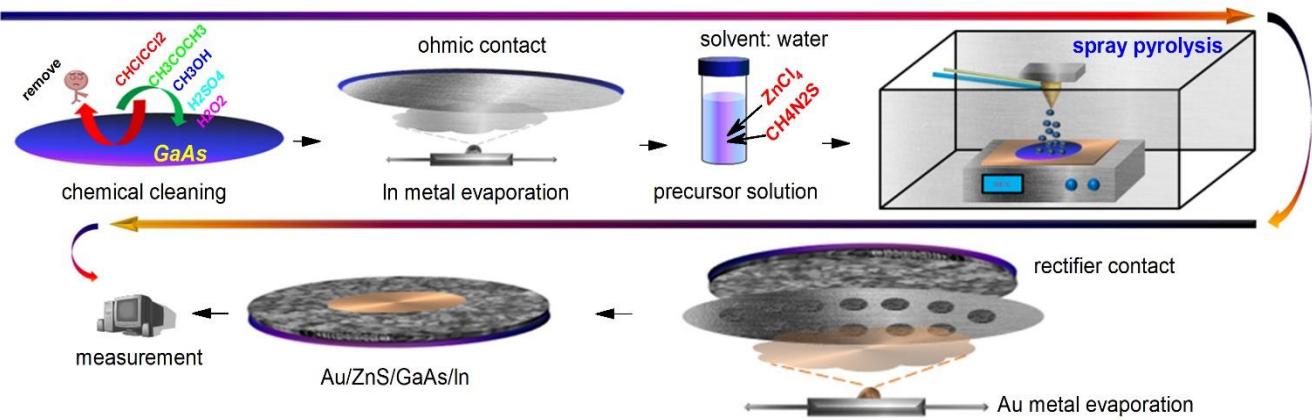


Figure 2.

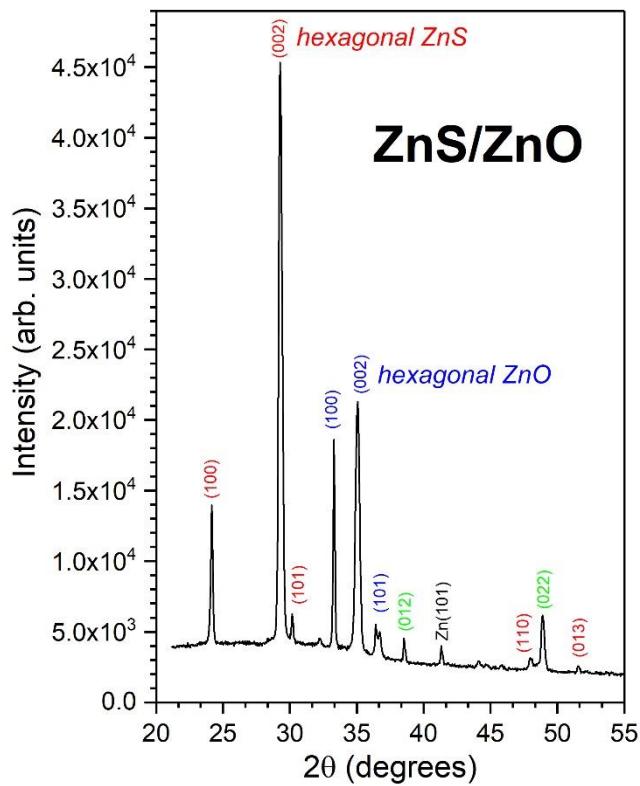
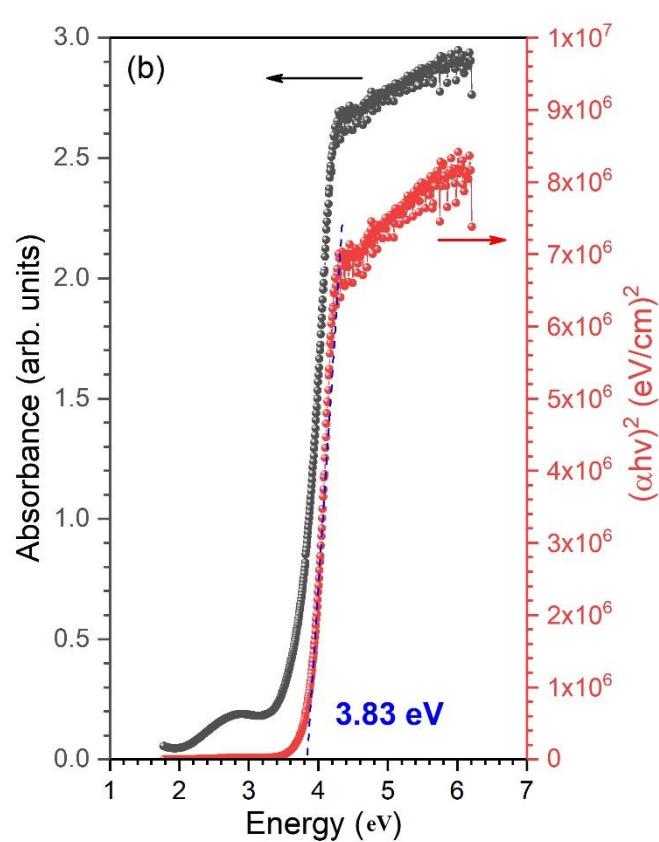
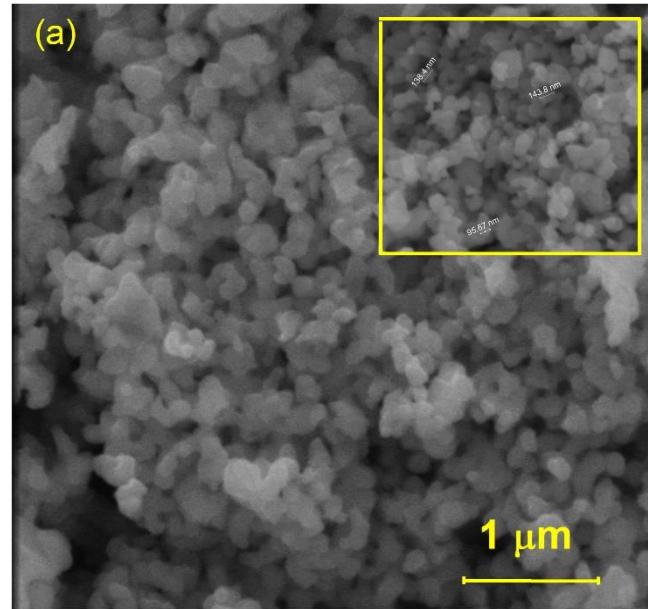
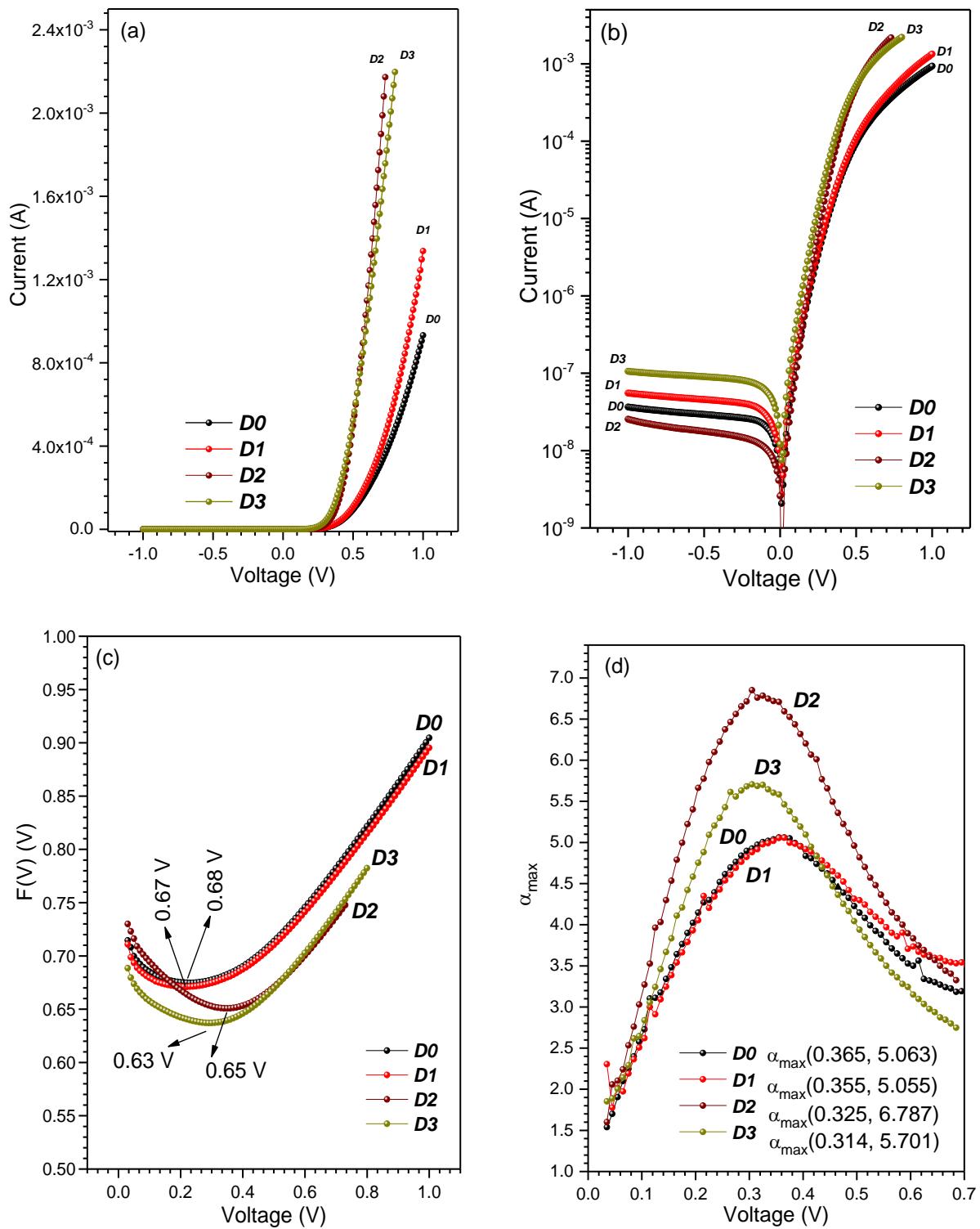


Figure 3.



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Figure 4.

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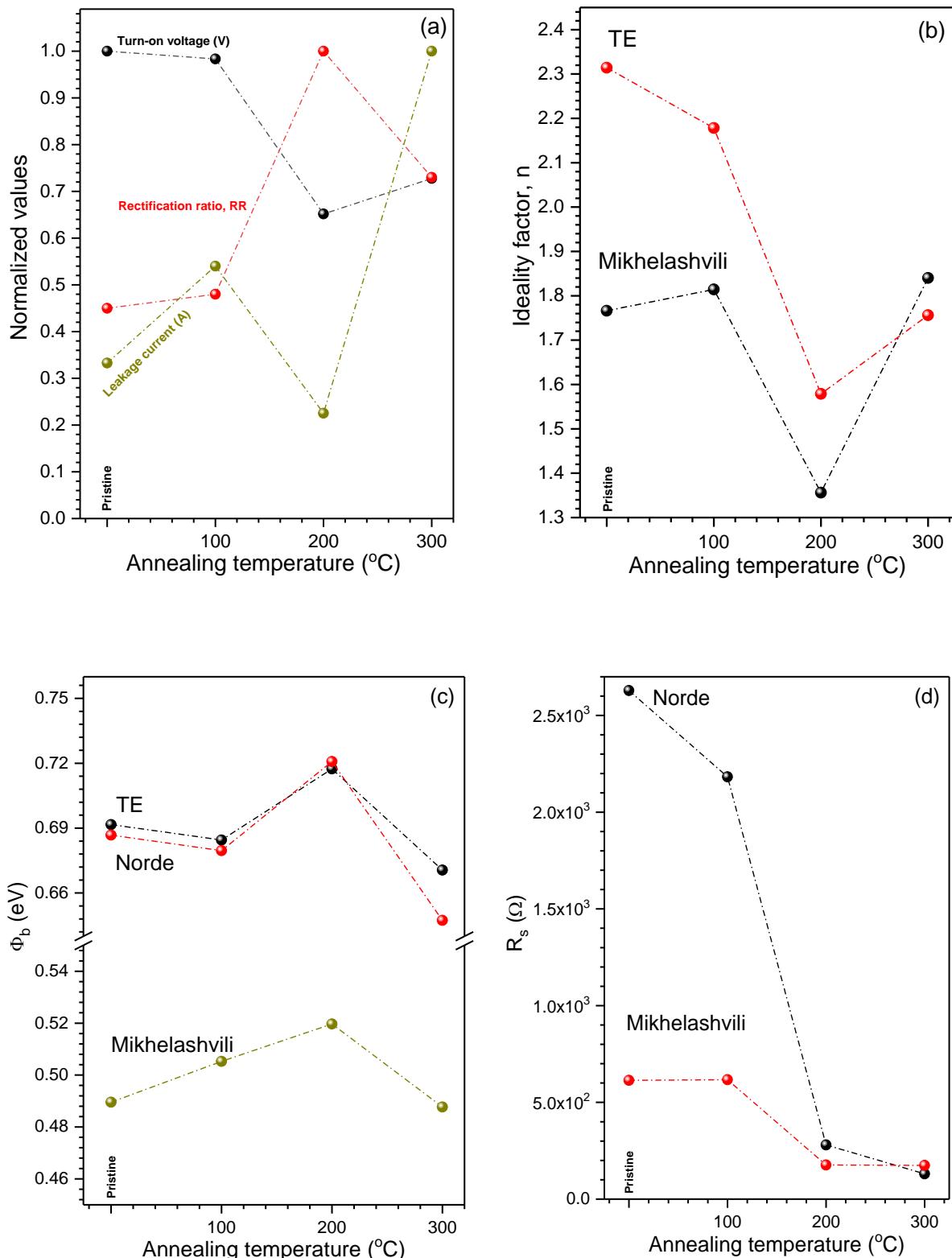
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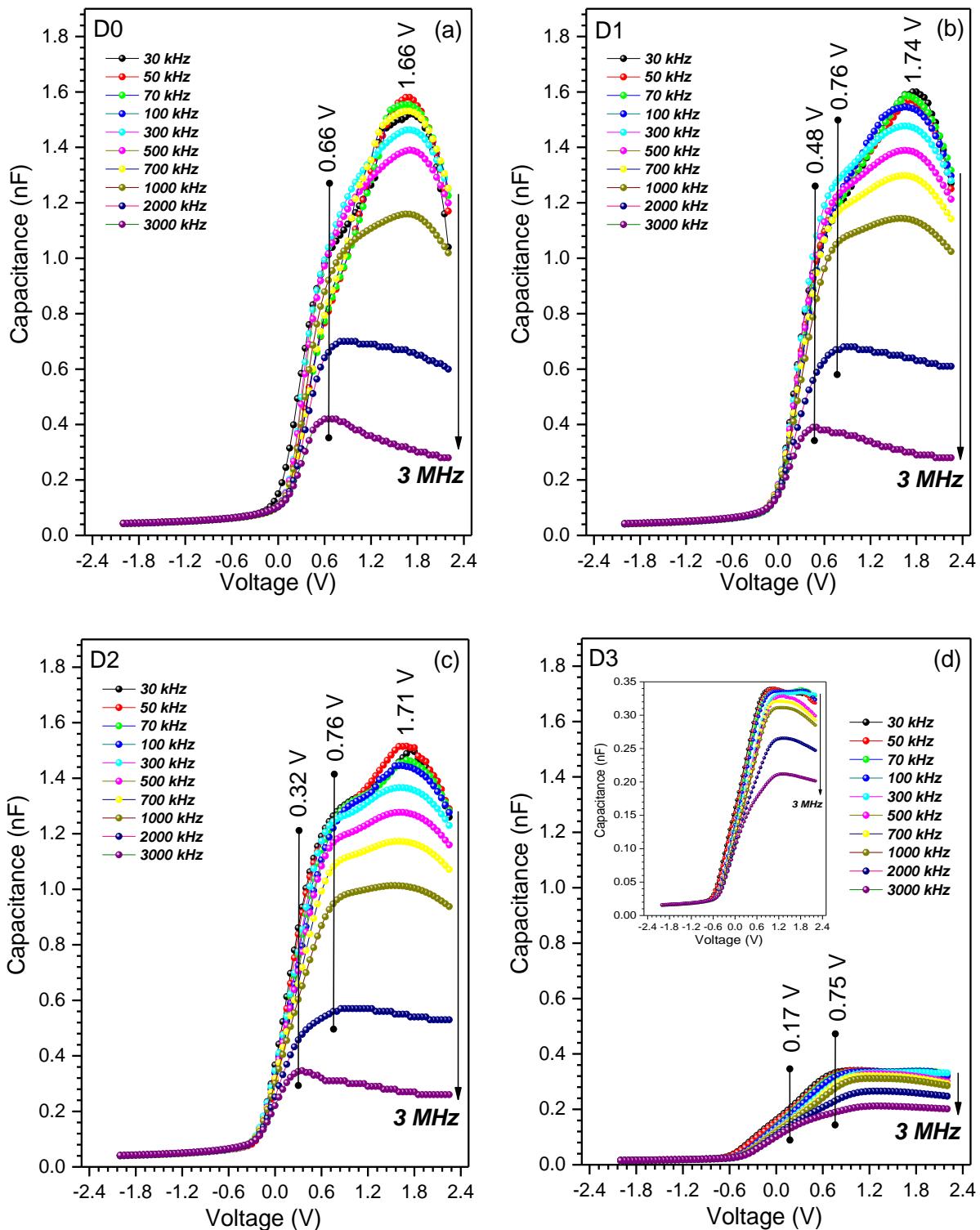
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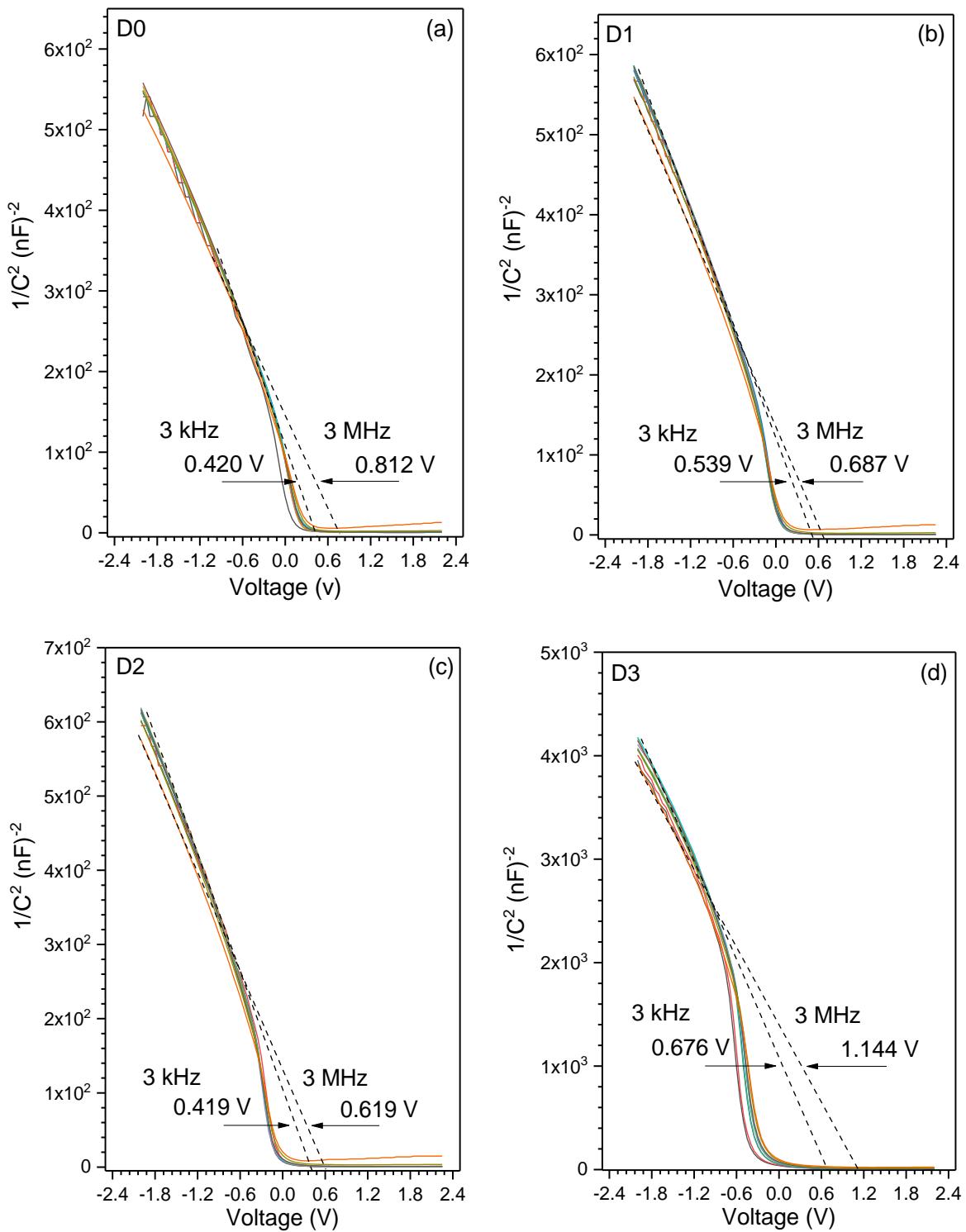
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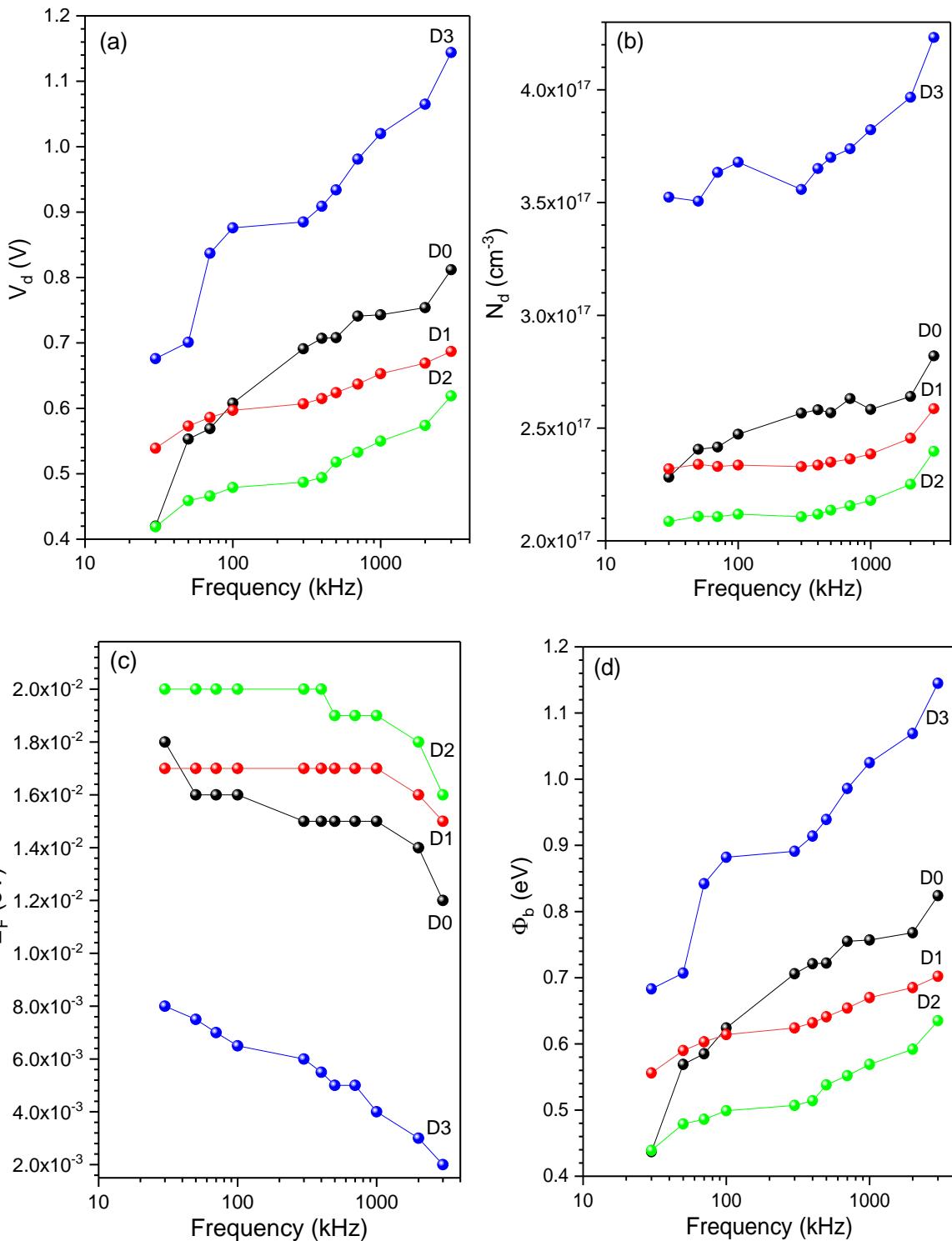
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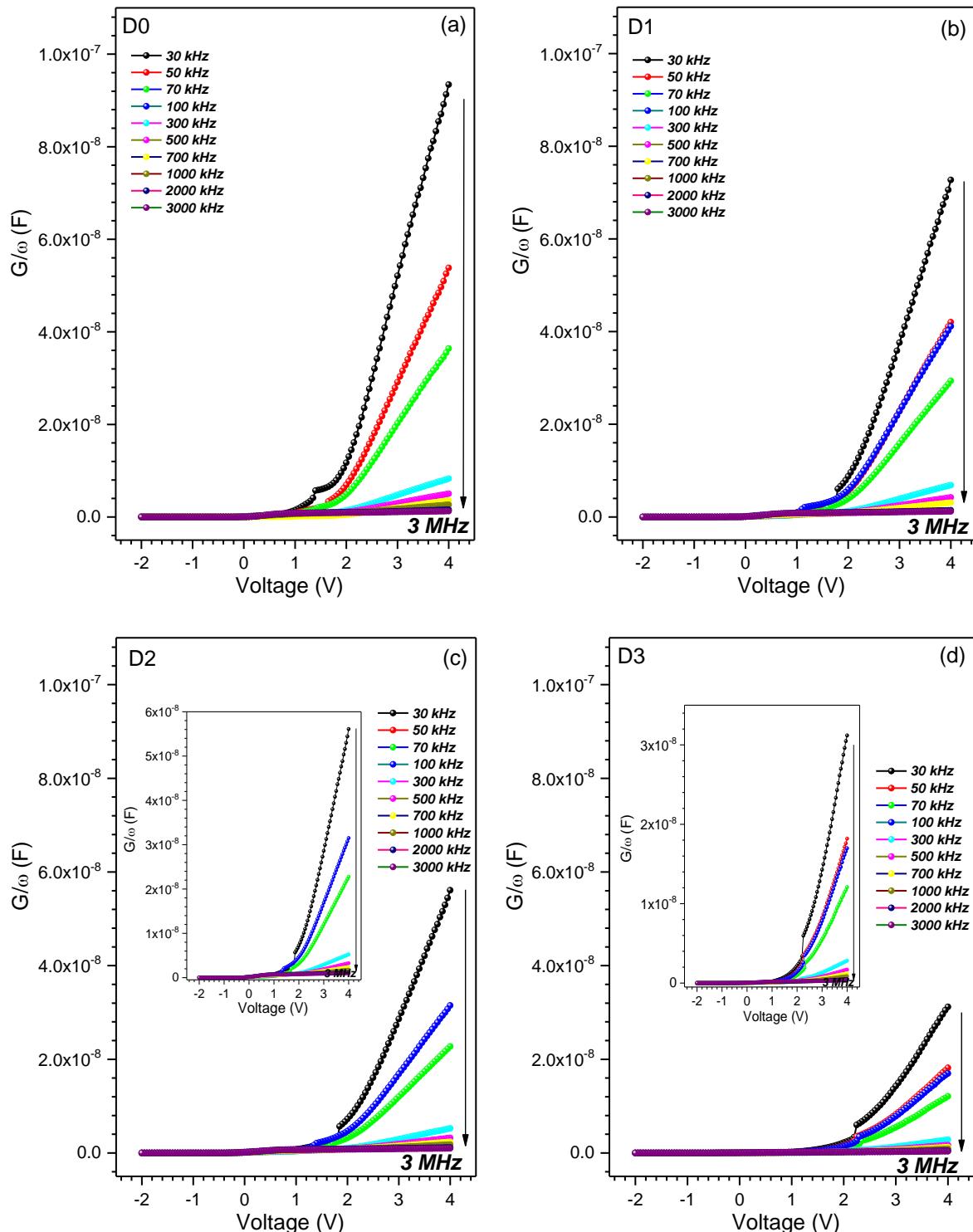
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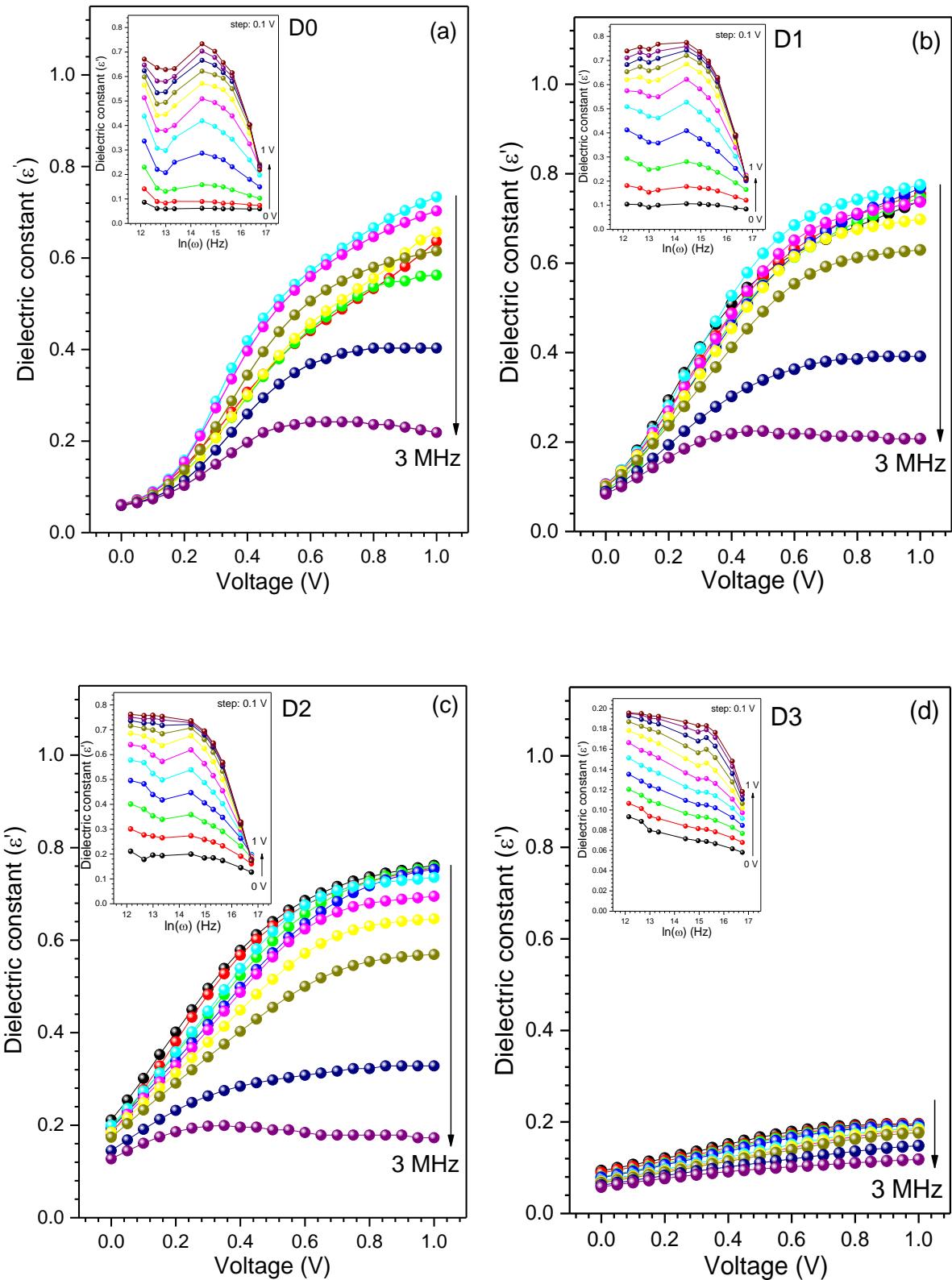
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Figure 10.

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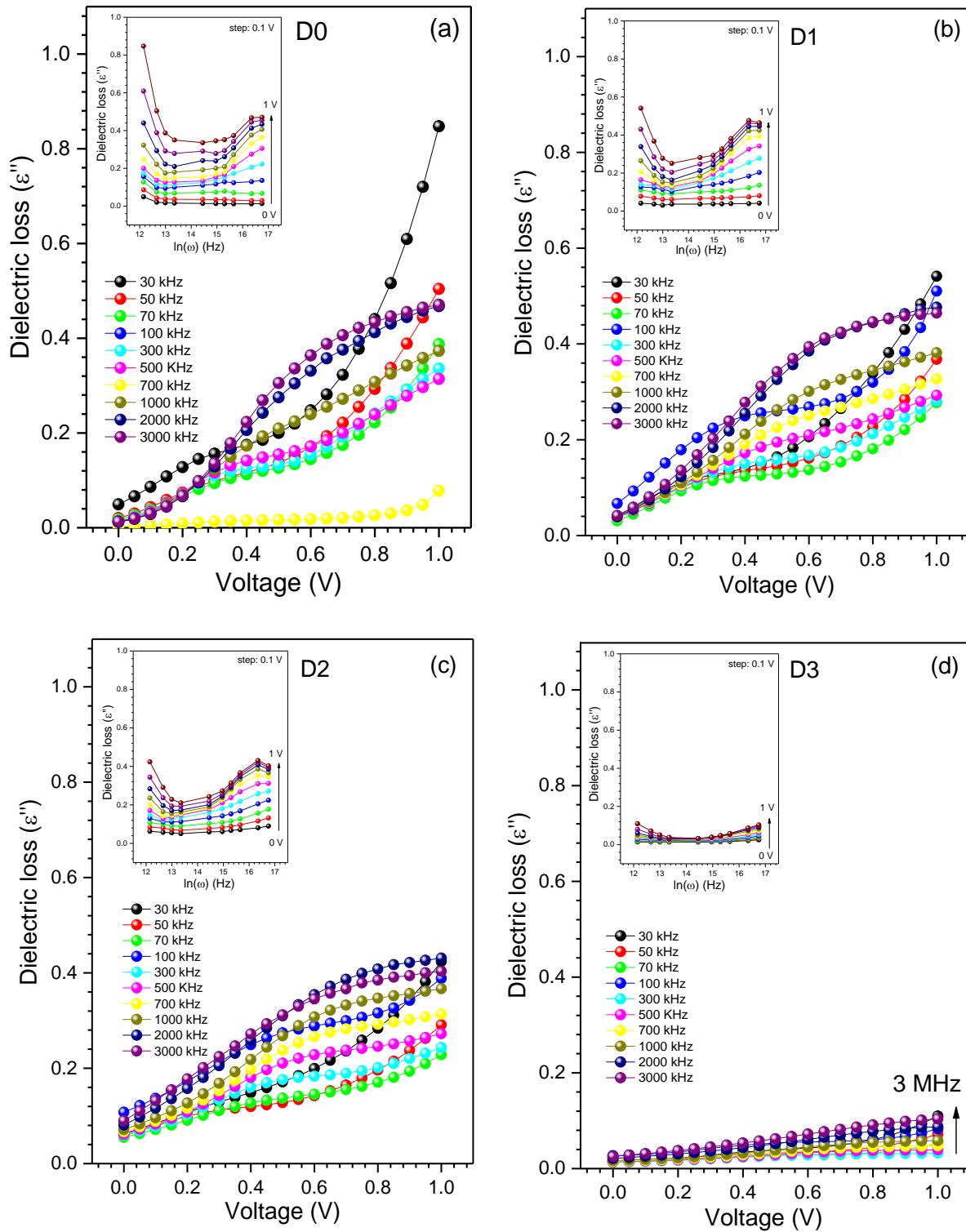
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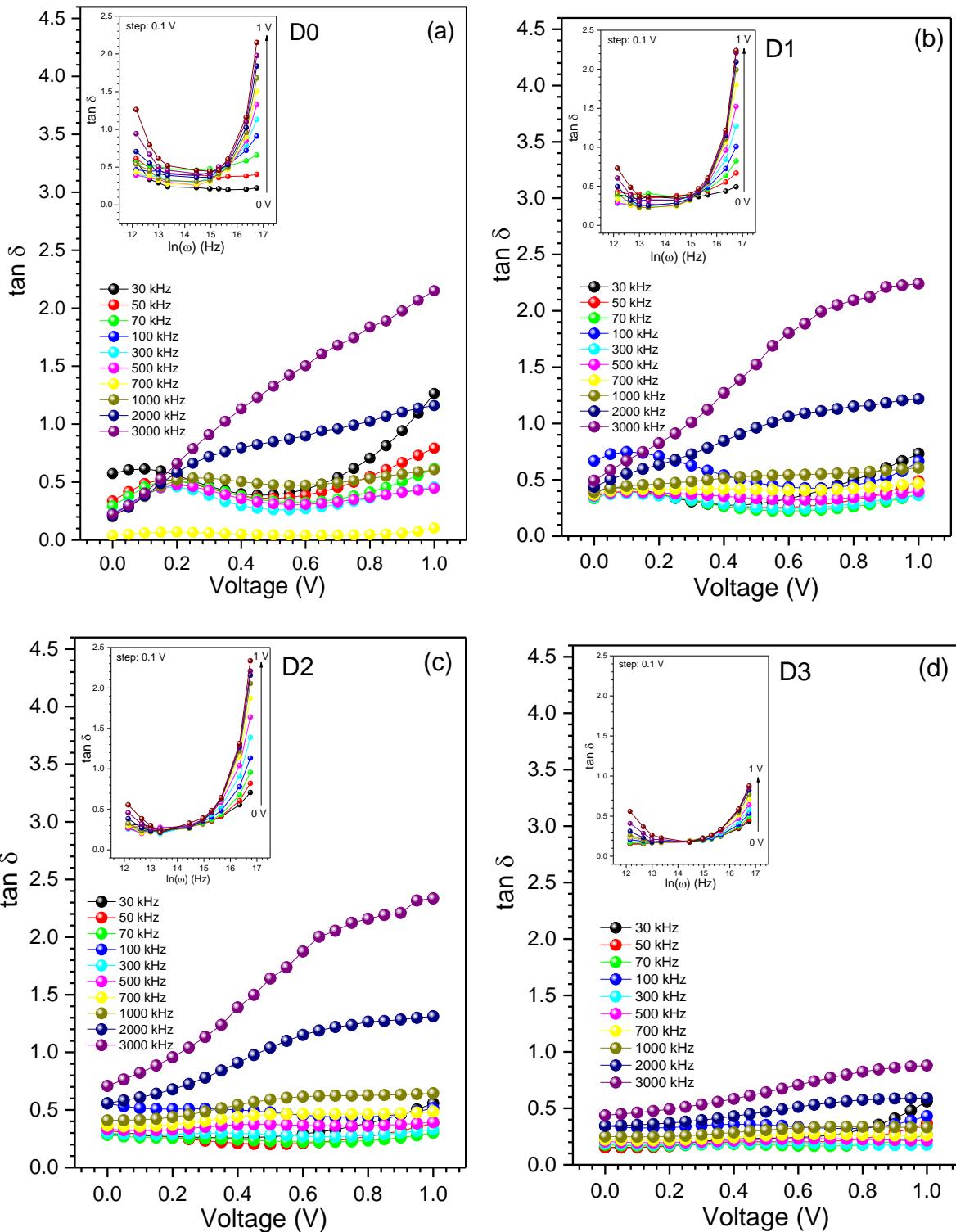
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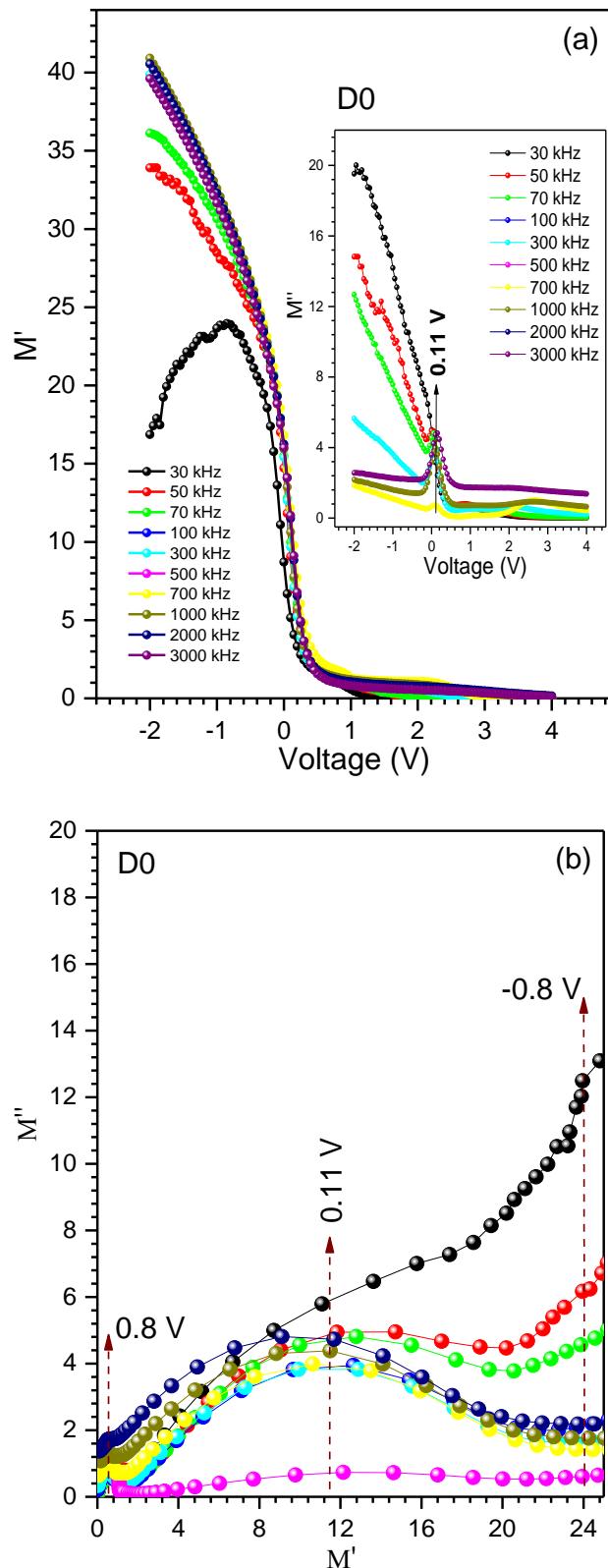
4

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Figure 13

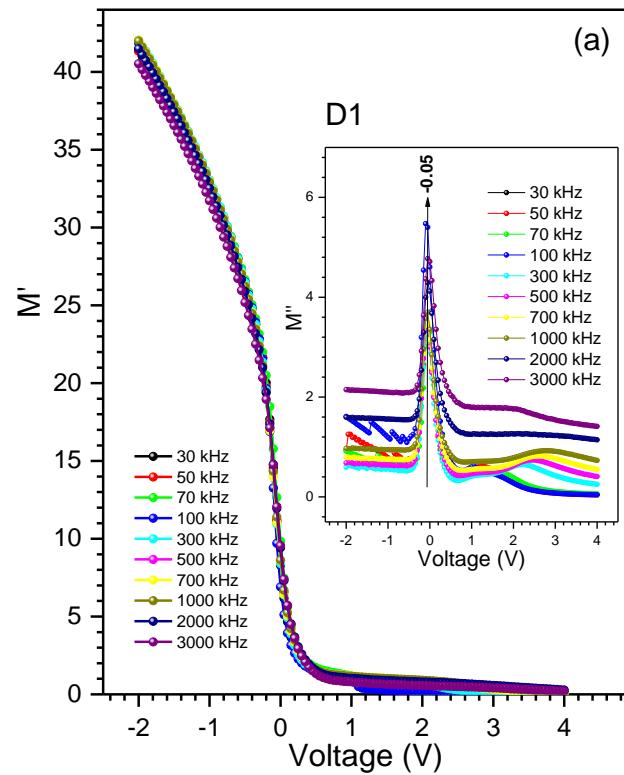
2

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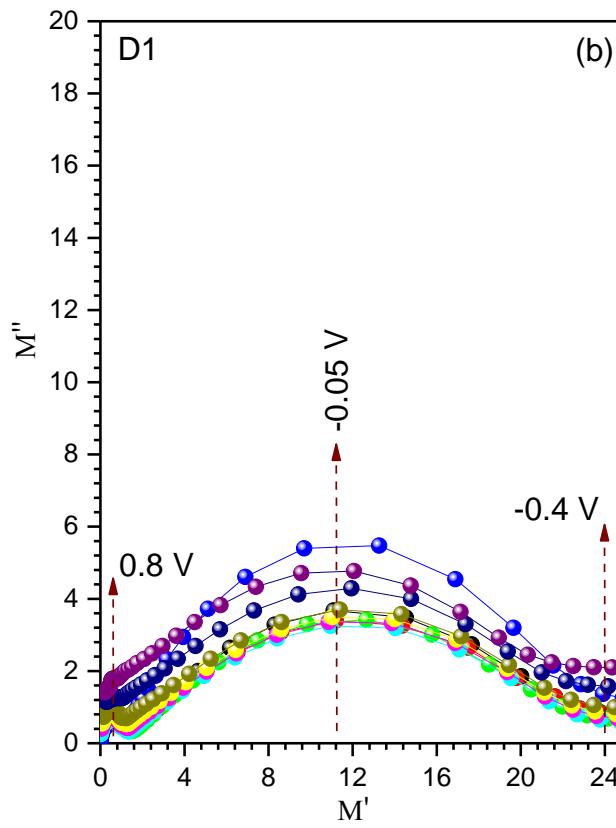
4

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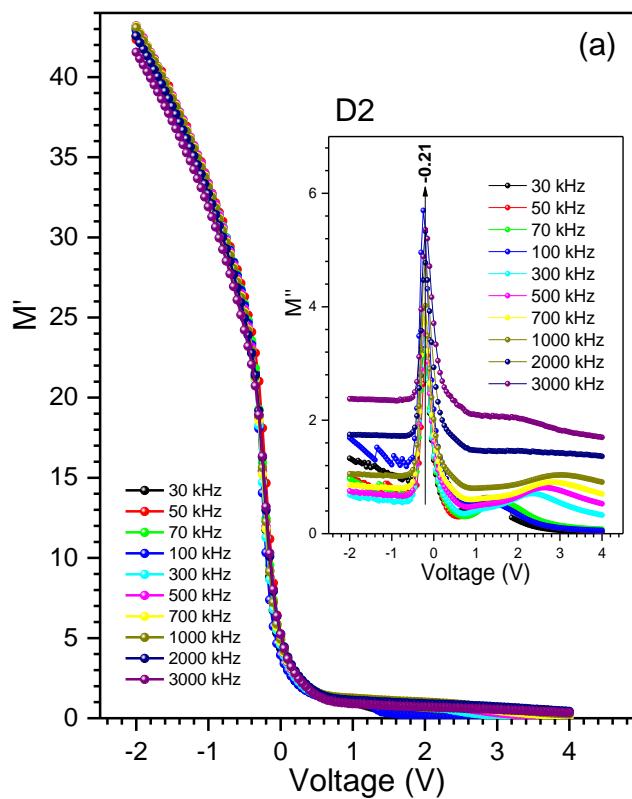


3

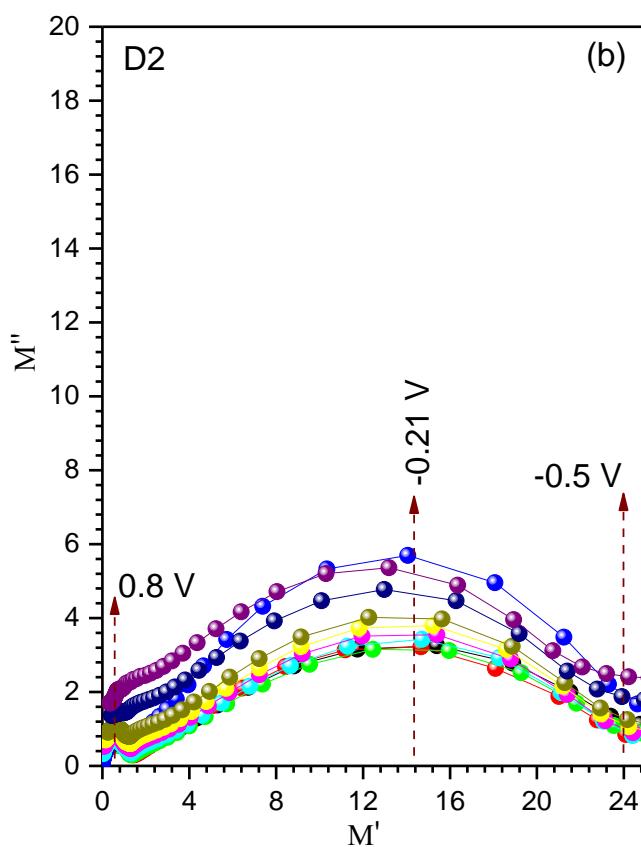
4

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Figure 15

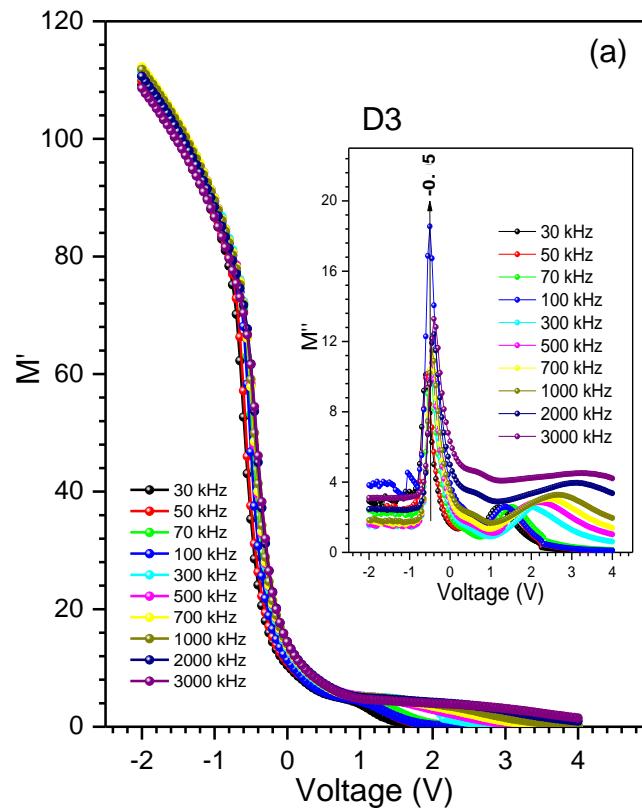
2



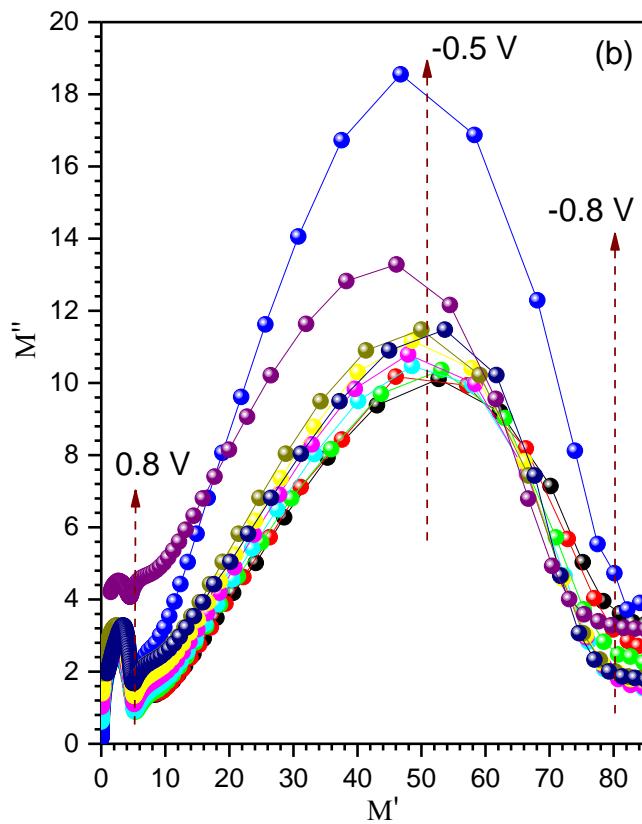
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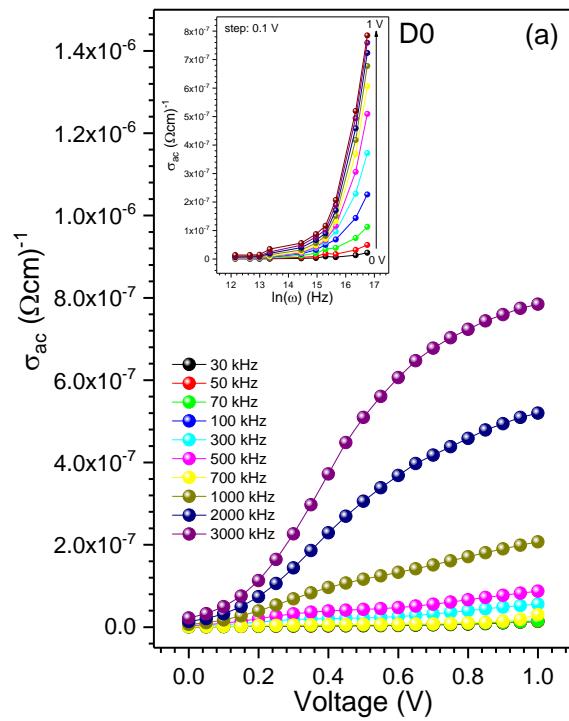
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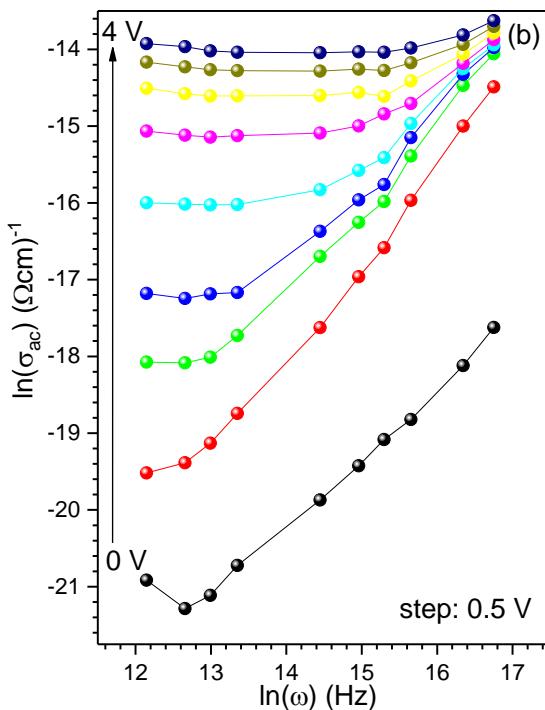
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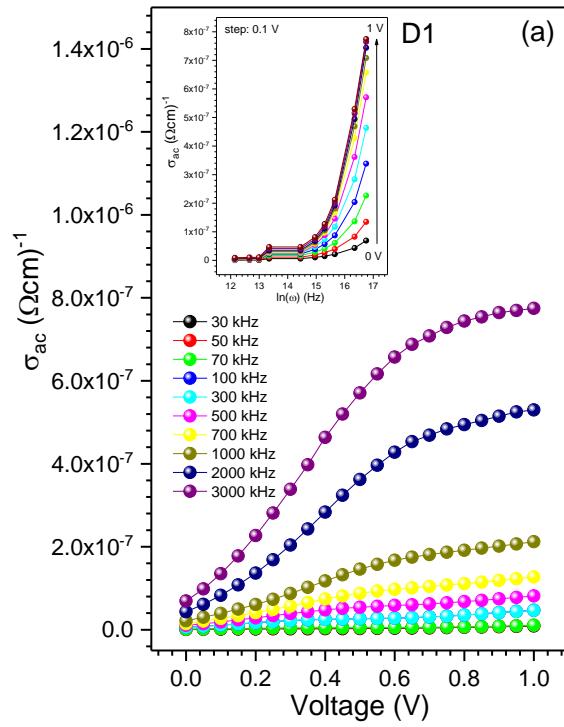
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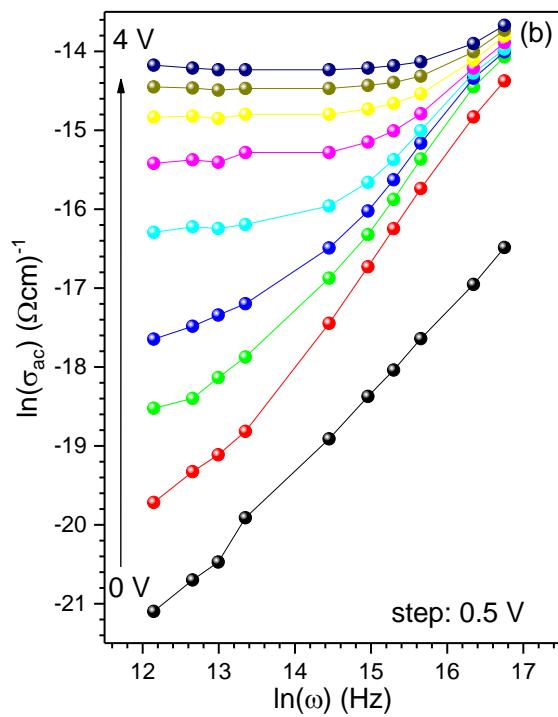
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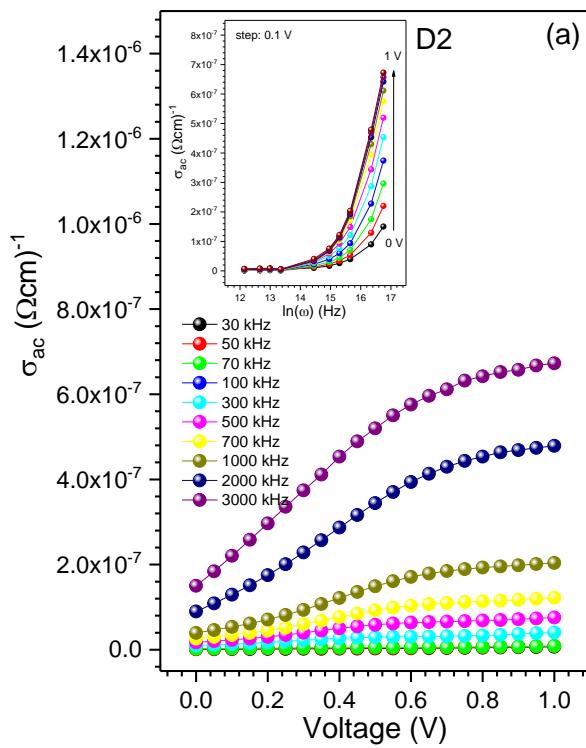
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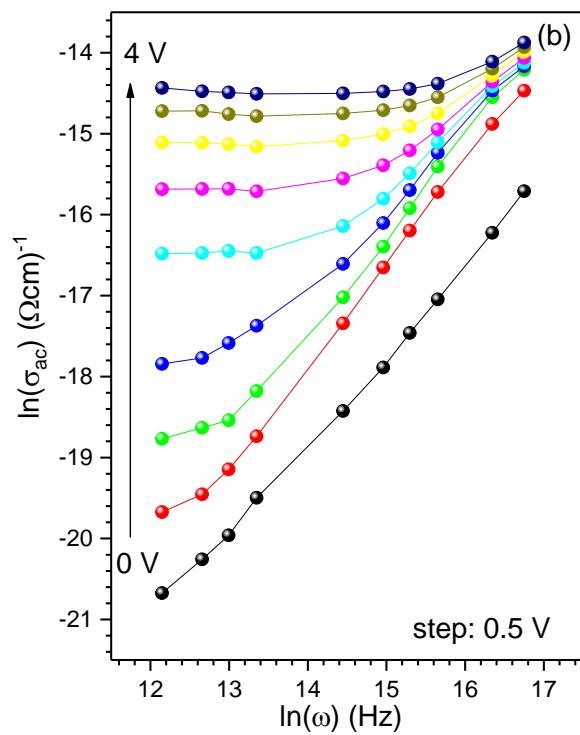
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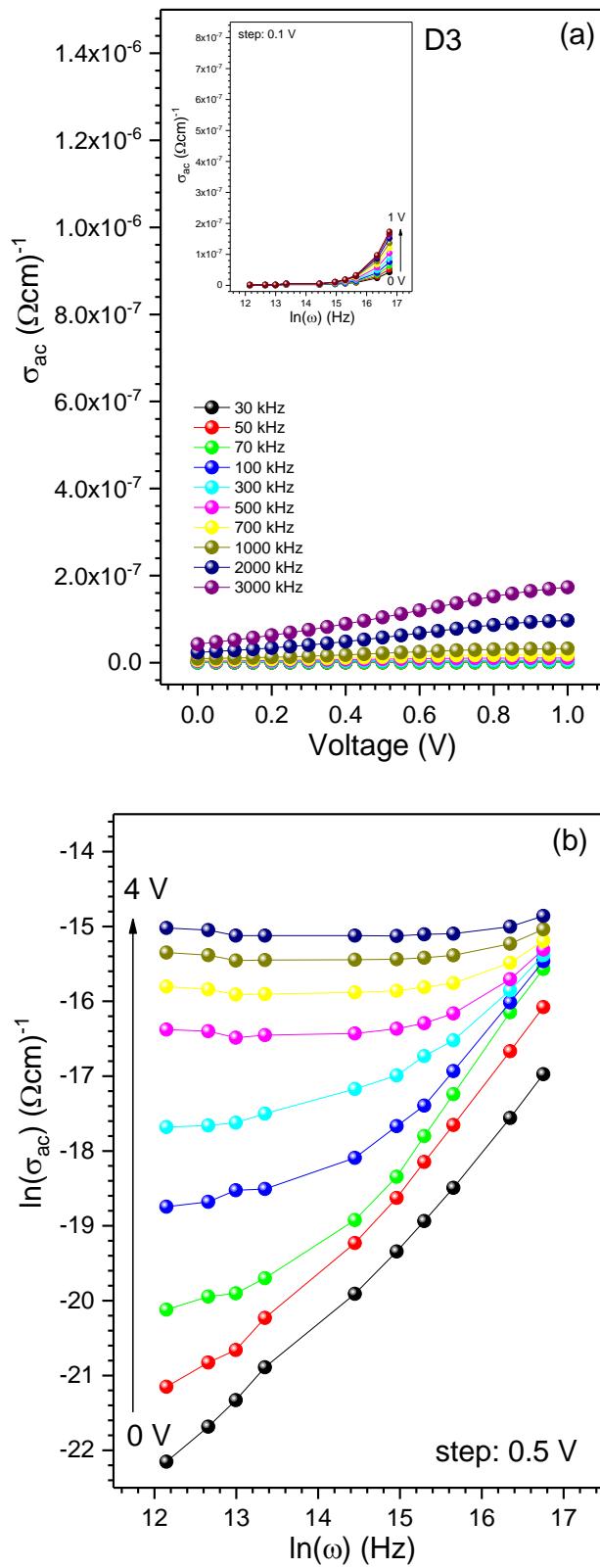
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Figure 20

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Research Highlights

- ✓ The ZnS thin film used at Au/n-GaAs junction was grown the spray pyrolysis method.
- ✓ The some structural, surface and electrical properties of the ZnS thin film were examined with XRD, SEM and absorption measurements.
- ✓ The **I-V**, **C-V** and **G/o-V** characteristics of the **Au/ZnS/n-GaAs/In** device were examined depending on thermal annealing.
- ✓ The results obtained from different models were compared.