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Modeling organic thin-film transistors based on the virtual source concept: A case study☆

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ABSTRACT

We apply the virtual source concept to describe the DC current-voltage characteristics of organic thin-film transistors. The draining of charge carriers from the virtual source is calculated using emission-diffusion theory. The electrical characteristics of organic thin-film transistors are commonly analyzed employing a drift mobility that is enhanced by the transistor overdrive. One possible origin of such a mobility model is charge trapping. We show that the direct parametrization of the fraction of mobile to total charges including trapped ones allows for a straight forward adaptation of the virtual-source emission-diffusion theory to organic electronics capable of describing measured transfer and output curves with a small number of parameters. The resulting model offers an alternative parametrization of well-known bias and temperature dependences. Beyond others, a limited charge injection does not arise from the high-field bulk saturation velocity but from the unidirectional thermal velocity and the charge carrier mean free path is a critical model parameter. Moreover, diffusivity replaces the drift mobility as the current scaling factor, which would lead to slightly different predictions for the current-voltage curves in the case that the Einstein relation is not valid.

1. Introduction

Thin-film technologies enable large area, low cost, roll-to-roll manufacturing of flexible electronics [1]. A large variety of active layer materials and device architectures has been investigated. However, in general performance limitations of thin-film transistors (TFTs) still prevent a successful product placement in many commercially interesting societal sectors. Especially the low mobility of charge carriers in organic semiconductors, either in the form of polymers or small molecules, is challenging. TFT-circuit interactions can only be studied with the help of simplified current-voltage models, which preferable should be based on general principles and be easy to calibrate to guarantee technology independent applicability.

The state of the art [2–4] in compact DC modeling of organic thin-film transistors (OTFTs) has been recently reviewed [5]. Moreover, a late addition to the set of available TFT models is described in [6]. All described and extensively used models are derived from averaging the current J_D per gate width over the channel length. Alternatively, model equations can be developed describing the charge injection into the channel throttled by a potential barrier, which is controlled by the source (S), gate (G) and to a weaker extent drain (D) potential. The existence of such a current control point might be less obvious in TFTs than in MOSFETs, where the pn junction close to the source naturally leads to a potential barrier. On the contrary, contact regions in TFTs are not necessarily heavily doped. Nevertheless, the presence of a Schottky barrier and the electrostatic doping induced by the gate-source capacitance of the otherwise only unintentionally and weakly chemically doped organic semiconductor will have a similar effect. The limited rate of charge injection from the top of a potential barrier can be attributed to and termed as a virtual source (VS).

The VS concept has been first described for short-channel MOSFETs in [7]. Assuming a traditional MOSFET point of view, the velocity for injecting charges from the VS will be limited by a maximum effective saturation field, yielding $1/v_{inj} = 1/v_{injo} + 1/v_{sat}$ [8]. However, the saturation velocity is given by the unidirectional thermal velocity as already shown in [9]. Originally, the VS model introduced an empirical transition $F_{sat}(V_S, V_G, V_D)$ between the low and high drain bias regime employing a gate-dependent saturation field, which is obtained by interpolating between its weak and strong accumulation value. However, the current at VS is diffusive and emission-diffusion (ED) theory allows to put F_{sat} on a more physical foundation and most important allows to extend the VS concept to long-channel devices [10,11]. Thus, ED theory enables to join the knowledge of two formerly distinct areas, the modeling of nanoscale FETs and TFTs. As a first step, we adapt in the

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present study the VSED model to TFTs by acknowledging an increased number of traps present in amorphous materials. So far, the term "virtual source" has not been used in device modeling approaches for organic electronics. Obviously, working OTFT compact models exist and one might question the need for another modeling approach. As we will show, an organic virtual-source emission-diffusion (OVSED) model provides a new perspective on well-known bias (and temperature) dependences of electrical OTFT characteristics. Moreover, the approach can tap into the extensive body of knowledge on contact and charge effects in organic-based electronic devices and their consequences to compact modeling and parameter extraction strategies [12–14]. As a case study, we extract and discuss the parameters of the OVSED model from experimental OTFT data taken from [5,6].

2. Model description

Model equations are given in terms of intrinsic channel voltages. Internal nodes are connected to external nodes by serial resistances R_S and R_D. In the following the model of a p-type transistor with symmetric source and drain is described. Thus, the source is the terminal with the highest potential and all source referenced voltages are negative. Nodal and device sign conventions for OTFTs are described in the appendix of [15]. The drain current of a p-type transistor exits the channel and flows into the drain node and thus is positive. The drain current density at the VS reads:

$$J_D = I_D/W = v_{sat}\,F_{sat}\,Q_{free}, \tag{1}$$

$$Q_{free} = q\,\sigma_V \times \left(\frac{Q_{tot}}{q\sigma_{traps}}\right)^{l}. \tag{2}$$

For an exponential tail of trapping states reaching from the valence band edge into the band gap, the free and total density of charge carriers are related by a power law since all states are occupied according to the same quasi Fermi level, see Eq. (B4) in [16] and its preceding derivation. Here, σ_V and σ_{traps} denote the density of valence and trapping states within a monolayer of the organic semiconductor at the VS, respectively. The exponent l is determined by the ratio of the effective "temperature" that parametrizes the exponential energy distribution of the trap states and the device temperature originating from the Boltzmann energy distribution of the free charge carriers. However, l is treated as model parameter since the exact trap distribution is generally unknown. The distinction between free and trapped charge carriers as given by Eq. (2) is the main adaptation of the VSED framework to thin-film materials proposed in the present work.

For a depleted organic semiconductor an exponential accumulation of holes is expected with increasing gate field, which ceases when substantial screening by the accumulated charge sheet sets in. The following phenomenological expression first proposed in [17] is employed:

$$Q_{tot} = C_I\,n\,V_T \ln\left[1 + \exp\left(\frac{\psi_{VS} - V_{GS}}{n\,V_T}\right)\right], \tag{3}$$

$$\psi_{VS} = V_{tho} + |\delta|\,V_{DS}. \tag{4}$$

The insulator capacitance is determined by the dielectric constant ϵ and thickness t_I of the gate insulator $C_I = \epsilon/t_I$ and V_T denotes the thermal voltage $V_T = kT/q$. The transition from weak to strong accumulation is modeled by the parameters n, V_{tho} and δ. Originally, the parameter n arises from the charging of the semiconductor region adjacent to the gate insulator interface by filling surface states, repelling mobile electrons and attracting mobile holes, which influences the rate of band bending with the gate bias. Beyond a gate bias of ψ_{VS} the interface potential becomes basically independent of V_{GS}. ψ_{VS} is therefore also known as threshold voltage. These concepts can be readily applied to parametrize the gate bias control of the top of the potential barrier that the free charge carriers cross by diffusion. In other words, the parameter ψ_{VS} represents the critical bias for which the potential at the VS becomes independent of the gate voltage. In OTFTs, the onset of strong accumulation is sometimes shifted to a higher gate field for a larger drain bias. Thus, δ does not represent necessarily a drain induced barrier lowering (DIBL). During accumulation of holes at the gate insulator interface, both n and l describe the charging of trap states. Indeed, in this operation regime the voltage scale for the exponential increase of the drain current with gate bias is given by $(n/l)V_T$ in the OVSED model.

The velocity of injecting the charges Q_{free} into the transistor channel is often discussed as $v_{inj} = v_{sat}F_{sat}$. The common practice to estimate the drain current in OTFTs as drift movement of the injected charge carriers may lead to the conclusion that v_{sat} equals the high-field bulk saturation velocity. However at the VS and in any low-field region, the derivative in respect to position of the quasi Fermi potential and not of the electrostatic potential drives the current. Therefore, the saturation velocity is set by the unidirectional thermal velocity, see e.g. [8]:

$$v_{sat} = 2D/\bar{\lambda}_{free} = 2\mu\,V_T/\bar{\lambda}_{free}, \tag{5}$$

which is here parametrized by the diffusion coefficient D and may be related to the drift mobility μ via the Einstein relation. At low drain bias charge carrier diffusion is the dominant transport mechanism in large parts of the OTFT and not only at the VS. The characteristic length in Eq. (5) will no longer be given by the mean free path $\bar{\lambda}_{free}$ but by the diffusion length. Since only charge carrier of a single type are injected into a basically intrinsic organic semiconductor the diffusion length might be very large and comparable to the device dimension given by the gate length L_G. As we shall see, F_{sat} will introduce a length scale $\lambda = L_G/\bar{\lambda}_{free}$, which effectively replaces $\bar{\lambda}_{free} \to L_G$ at low drain bias.

The remaining function F_{sat} describes the draining of the accumulated holes. For long-channel OTFTs emission-diffusion theory [10,11] represents an interesting framework for determining F_{sat}:

$$F_{sat} = \frac{1}{1+2t}\,\frac{1-\exp(-V_{SD}/V_T)}{1+\exp(-V_{SD}/V_T)/(1+2t)}. \tag{6}$$

For a drain bias sufficiently larger than the thermal voltage the transition function amounts to $F_{sat} = 1/(1+2t)$. The critical probability factor t is given by an averaged Boltzmann factor across the channel portion under gate control and can be calculated from the specific potential profile. For long channel devices the following analytic form has been suggested, see Eqs. (4)–(12) in [10]:

$$t = \frac{2\lambda}{m^2(1-\eta^2)}[(1-m\,\eta)\exp[-m(1-\eta)] - (1-m)], \tag{7}$$

$$\eta = 1 - \tanh(V_{SD}/mV_T), \tag{8}$$

$$m = \frac{2V_{Gt}/V_T}{1+\sqrt{2V_{Gt}/V_{crit}}}, \quad V_{Gt} = Q_{tot}/C_I. \tag{9}$$

An increased transistor overdrive leads to a spacious diffusion region and shifts the onset of saturation to a larger drain bias. At large gate bias the required increase in the saturation voltage slows down and turns into a square-root growths for $V_{Gt} > V_{crit}$. Note that the saturation velocity given by Eq. (5) is only reached for both, large V_{SG} (low barrier) and large V_{SD} (charge sink). In general, the critical length for diffusion that substitutes $\bar{\lambda}_{free}$ in Eq. (5) is a gate bias dependent fraction of L_G. As further detailed in the following paragraph, the required V_{Gt} to reach the maximum injection velocity given by the unidirectional thermal velocity decreases with L_G. Note that we employ as transition function between the low and high drain bias regime a parameter-free $\tanh(x)$. If required, this transition function can be replaced by $x/(1+x^{\beta})^{1/\beta}$ introducing an additional fitting parameter β. The simpler transition proves to be sufficient for describing the experimental data in the present study. The comparison with the original VSED model [10,11] reveals that t can be interpreted as the critical length for diffusion

dominated transport in the device measured in units of the free mean path. As such, t scales with λ that has a different meaning here than in [10,11].

In the following we discuss some model equations under simplifying assumptions for bias values. For a large range of bias conditions, F_{sat} can be simplified to:

$$F_{sat} \approx \frac{1}{1+2t}, \quad t \approx \frac{2\lambda}{m(1-\eta^2)}. \tag{10}$$

In *saturation* $V_{SD} \gg mV_T$, i.e. $\eta = 0$, and for $V_T \ll V_{Gt} \ll V_{crit}$ the probability factor becomes $t \approx 2\lambda/m = \lambda V_T/V_{Gt}$. For $\lambda \gg V_{Gt}/2/V_T$ even a large transistor overdrive can result in a large $t \gg 0.5$ and thus a small $F_{sat} \approx 1/2/t = V_{Gt}/V_T/2\lambda \ll 1$. Under these assumptions the saturation current increases with Q_{tot}^{l+1}. In the case of $l = 1$ the well-known parabolic increase of the saturation current with the transistor overdrive is recovered. For a short channel OTFT, however, a large transistor overdrive exceeds λ resulting in $t \to 0$ and $F_{sat} \to 1$. In this case, the saturation velocity is given by Eq. (5) and $I_{D,sat} \sim Q_{tot}^{l}$, i.e., $I_{D,sat}$ grows slower with V_{GS} than in the long channel case. A *linear* dependence of F_{sat} on V_{SD} is observed for $V_{SD} \ll mV_T$. Thus, a pronounced linear output characteristic of an OTFT indicates large serial resistances R_S and R_D. Since $t \approx \lambda V_T/V_{SD} \gg 1$, the draining function can be calculated as $F_{sat} \approx 1/2/t \approx V_{SD}/V_T/2\lambda$. In both low and high drain bias regimes $F_{sat} \sim 1/2\lambda$, modifying the characteristic length scale for the diffusion velocity for long channel OTFTs. An interesting property of the model is that the free mean path $\bar{\lambda}_{free}$ not only determines μ but also appears directly as fitting parameter in the form of the dimension-free length scale λ required to describe correctly the size modulation of the OTFT's low-field region with the drain bias. Therefore, OTFT characteristics provide valuable information about $\bar{\lambda}_{free}$ when analyzed with the help of the OVSED model.

In the present work the VSED framework is suggested as a base for the compact modeling of OTFTs but the model has not yet been implemented in a circuit simulator. Beyond others, a full Verilog-A model to be used in circuit simulators needs to satisfy the Gummel symmetry test (GST). The VSED equations do pass the GST as, e.g., shown in [18]. The addition of Eq. (2) will not change the symmetry properties of the model. Only during the revision of the present manuscript we came aware of the very interesting application of the VSED framework to black phosphorous field-effect transistors presented in [18], which adds further evidence that the VS concept can be successfully extended to long channel devices with the help of emission-diffusion theory. Although the VS concept has been already successfully applied to emergent materials like carbon nanotubes [19], VSED has been applied so far only to silicon based transistors.

3. Extraction procedure

Eqs. (1)–(9) form the physical base of the modified VS approach suggested here. However, the three physical parameters v_{sat}, σ_V and σ_{traps} are difficult to directly calculate or measure. Inserting Eqs. (2) and (3) in Eq. (1) shows that these parameters can be lumped into a single bias-independent parameter:

$$J_T := qq\sigma_V (C_I n V_T/q\sigma_{traps})^l v_{sat}. \tag{11}$$

The drain current density J_D scales with J_T, i.e., with the linear current density caused by free charge carriers induced by a gate bias of nV_T and diffusing from the VS into the channel. Although J_T depends also on n and l, the pre-factor can be considered as independent fit parameter since its value can always be adjusted by changing one of the three parameters v_{sat}, σ_V and σ_{traps}, which do not appear in any of the other model equations. Therefore, we discuss the electrical transistor characteristics in terms of seven intrinsic model parameters, namely: J_T, V_{tho}, δ, l, n, λ and V_{crit}. Employing this set of parameters simplifies the value extraction from experimental current-voltage curves of OTFTs but does not imply any change in the model equations. Parasitic elements include the serial resistances $R_S = R_D$ and a constant leakage current $J_{D,leak}$. The latter is simply added to the intrinsic component given by Eq. (1). To include the former, the intrinsic channel voltage is calculated by reducing the external drain bias by $2R_S I_D$ in a self-consistency loop, which is normally taken care of by the circuit simulator. Different model parameters impact different regions in the output and transfer curves and thus can be obtained from these regions: (i) The transfer curve at low drain bias gives V_{tho}, l, n, $J_{D,leak}$, (ii) the transfer curve at high drain bias gives δ, l, n, (iii) the linear output curve gives R_S, λ and (iv) the saturated output curve gives V_{crit}, λ. Nevertheless, the limited number of model parameters allows to fit all values at once by employing a nonlinear least-squares solver, which is the procedure of choice here. To this extent all available output and transfer curves where interpolated to the same voltage grid to serve as input matrix of the least-squares algorithm.

All parameters with the exception of δ and V_{crit} have a significant influence on the current-voltage characteristics at low drain bias. For an OTFT operating in the linear regime and at a sufficient large gate overdrive:

$$I_D = WJ_T \frac{V_{SD}}{V_T} \frac{1}{2\lambda} \left(\frac{V_{SG} + V_{tho}}{nV_T} \right)^l. \tag{12}$$

This expression exhibits the same bias dependences as the ones obtained for a generic charge drift model with gate bias enhancement of the mobility [20]. Thus the parameter extraction strategies described in [20,21] are readily applicable to the OVSED model and allow a decoupled determination of parameter values. However, the employed multidimensional least-squares fit algorithm gives good convergence and a further refinement of the extraction procedure is left for future work. The similarity of Eq. (12) with predictions from charge drift models that include a mobility enhancement factor is no surprise. As discussed in [22], the power law dependence of the mobility on the transistor overdrive can be traced back to the drift of charges in a transport band in the presence of trap states. The mobility is then modified by the fraction of mobile to trapped charges, which corresponds to Eq. (2). Moreover, variable range hopping theory, although using a different parametrization, gives expressions for mobility and DC characteristics with almost identical bias and temperature dependences. The analysis of the latter leads to a final interesting observation. For the operation regime in which Eq. (12) holds, the scaling with temperature T is described by:

$$\frac{I_D(T)}{I_D(T_{ref})} = \frac{T_{ref}}{T} \frac{D(T)}{D(T_{ref})}. \tag{13}$$

In the case that the Einstein relation between diffusivity D and drift mobility μ holds, as assumed in Eq. (5), the OVSED and a generic charge drift model predict the same dependence of the drain current on temperature. However, for disordered organic semiconductors the Einstein relation may be violated in the presence of deep traps [23]. Although beyond the scope of the present work, thus, analyzing temperature-dependent current-voltage curves of OTFTs with the help of the VSED framework may shed new light on the validity of the Einstein relation in organic semiconductors.

4. Case study

The results of the parameter extraction are summarized in Fig. 1 and Table 1. Three devices have been analyzed with different geometries and channel materials. In all cases the calibrated OVSED model is in excellent agreement with the measured characteristics proving that the given approach is universal. Interestingly, the FlexOS™TFT by NeuDrive Limited exhibits the smallest R_S and the smallest n, i.e. the steepest transition from weak to strong accumulation.

The parameters of the OVSED model have a clear physical meaning. λ is the inverse carrier mean free path scaled by the channel length.

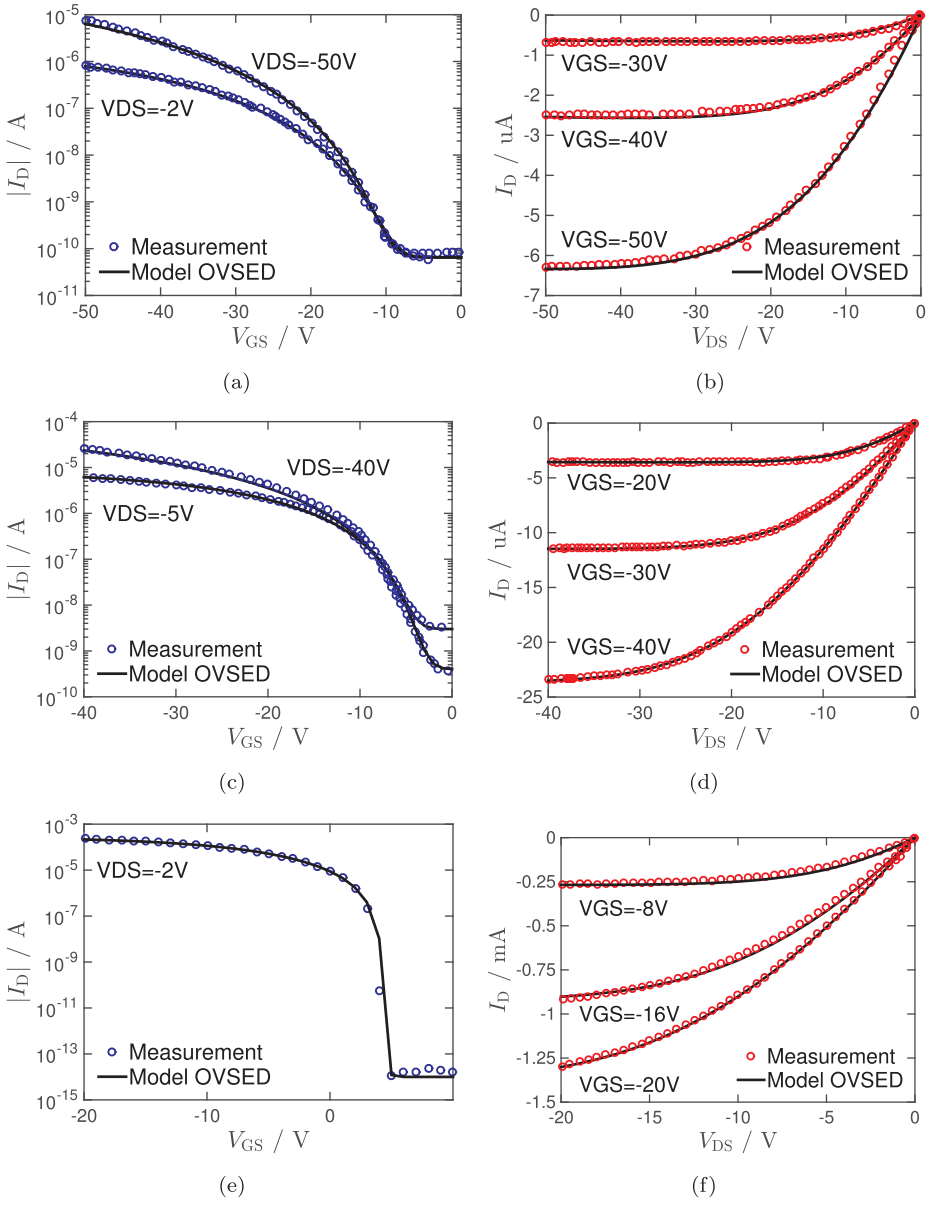

Fig. 1. Comparison between measured and simulated transfer (left) and output curves (right) for OTFTs described in [5](a,b) as well as in [6] (c,d) and (e,f).

Table 1
Extracted model parameter.

Material Geometry	pentacene TCBG [5] $W = 0.1$ cm $L_G = 40$ µm	C16IDT-BT BCTG [6] $W = 0.1$ cm $L_G = 70$ µm	FlexOS™ BCTG [6] $W = 0.1115$ cm $L_G = 8.1$ µm
V_{tho} [V]	−8.57	−3.44	+4.47
δ	0.0123	0.0032	0.0029
n	108	57.4	5.14
l	3.18	2.14	2.4
λ	1490	3010	586
V_{crit} [V]	32.3	15.8	14.7
J_T [µA cm^{-1}]	0.097	5.68	0.358
$I_{D,leak}$ [nA]	0.065	0.4–3	10^{-5}
R_S [kΩ]	500	242	3.13

Thus fitting the dimension-free value of λ allows to determine $\bar{\lambda}_{free} = L_G/\lambda$. The pentacene TCBG [5], $L_G = 40\,\mu m$, serves as an example in the following. The extracted value of $\lambda = 1490$ implies a relatively large $\bar{\lambda}_{free} = 27$ nm. Knowledge of the mean unidirectional carrier velocity v_T would allow to estimate the mobility. However, the required effective mass can be enhanced by polaronic effects and will differ from its density-of-states estimate. Pulsed source-sided carrier injection and measurement of the source-to-drain transition time in a drift field should provide an upper limit, since the frontier of the injected charge cloud moves with $v_{drift} + v_T > v_T$. Such measurements have been carried out yielding a velocity of $4.4 \times 10^3\,cm\,s^{-1}$ [24]. Thus:

$$\mu = \frac{v_T}{2V_T}\bar{\lambda}_{free} < 0.23\ cm^2\,V^{-1}\,s^{-1}, \tag{14}$$

which is a reasonable estimate for a pentacene based OTFT. The mobility in the OVSED model does not exhibit an explicit gate voltage dependence. The given upper estimate is slightly larger as the value extracted in [5] for the largest gate overdrive. This has to be expected since parasitics like defects and serial resistances are included here.

The extracted values for J_T and l allow to estimate the trap density. For the device under consideration $C_I = 3.3$ nF cm^{-2}. As estimate for the density of valence states within a monolayer of pentacene, we multiply the third root of the unit cell volume, 0.69 nm^3 [25], with a volume

density slightly below the one of pentacene molecules, i.e. 10^{21} cm^{-3} [26], yielding:

$$\sigma_{traps} = \frac{C_I n V_T}{q}\left(\frac{q\sigma_V v_{sat}}{J_T}\right)^{1/l} = 3.9 \times 10^{11}\,\text{cm}^{-2}. \quad (15)$$

The density of trapping states relative to extended states amounts to $\sigma_{traps}/\sigma_V = 0.0044$, which is slightly below other estimates varying from 0.1 to 0.01 [26]. However, the VS might be not located directly at the interface to the insulator but further into the bulk where a reduced number of defects has to be expected.

5. Conclusion

We applied the virtual source concept combined with emission-diffusion theory in the presence of charge carrier traps to the modeling of organic TFTs. The DC OVSED model employs only seven intrinsic parameters with clear physical meaning and allows easy parameter extraction across different technology platforms. Implemented as Verilog-A code in a circuit simulator it permits the fast assessment of the device impact on the figures of merit of TFT based electronic circuits. The power-law dependence of the drain current on the transistor overdrive is explained by charge trapping. A gate bias dependent charge carrier mobility, widely used to describe the electrical characteristics of OTFTs, can be traced to a similar origin. However, parametrizing explicitly the fraction of mobile to total charge carrier density allows for a straight forward extension of the VSED set of equations to the modeling of organic semiconductors. The OVSED model yields directly informations about the carrier mean free path and the exponential tail of the density of trap states. Such parameters are usually not used in compact models. From a top-down perspective, the OVSED model opens therefore new routes to device and material optimization.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, athttps://doi.org/10.1016/j.sse.2019.107639.

References

[1] Nathan A, Ahnood A, Cole MT, Lee S, Suzuki Y, Hiralal P, et al. Flexible electronics: the next ubiquitous platform. Proc IEEE 2012;100(Special Centennial Issue):1486–517.
[2] Marinov O, Deen MJ, Zschieschang U, Klauk H. Organic thin-film transistors: part I—compact DC modeling. IEEE Trans Electron Dev 2009;56(12):2952–61.
[3] Estrada M, Cerdeira A, Puigdollers J, Reséndiz L, Pallares J, Marsal LF, et al. Accurate modeling and parameter extraction method for organic TFTs. Solid State Electron 2005;49(6):1009–16.
[4] Li L, Debucquoy M, Genoe J, Heremans P. A compact model for polycrystalline pentacene thin-film transistor. J Appl Phys 2010;107(2):024519.
[5] Kim C-H, Bonnassieux Y, Horowitz G. Compact DC modeling of organic field-effect transistors: review and perspectives. IEEE Trans Electron Dev 2014;61(2):278–87.
[6] Zhao J, Yu P, Qiu S, Zhao Q, Feng L, Ogier S, Tang W, Fan J, Liu W, Liu Y, Guo X. Universal compact model for thin-film transistors and circuit simulation for low-cost flexible large area electronics. IEEE Trans Electron Dev 2017;64(5):2030–7.
[7] Khakifirooz A, Nayfeh OM, Antoniadis D. A Simple semiempirical short-channel MOSFET current-voltage model continuous across all regions of operation and employing only physical parameters. IEEE Trans Electron Dev 2009;56(8):1674–80.
[8] Lundstrom MS, Antoniadis DA. Compact models and the physics of nanoscale FETs. IEEE Trans Electron Dev 2014;61(2):225–33.
[9] Lundstrom M. Elementary scattering theory of the Si MOSFET. IEEE Electron Dev Lett 1997;18(7):361–3.
[10] Rakheja S, Lundstrom M, Antoniadis D. A Physics-Based Compact Model for FETs from Diffusive to Ballistic Carrier Transport Regimes. 2014 IEEE International Electron Devices Meeting IEEE; 2014. p. 35.1.1–4.
[11] Lundstrom M, Datta S, Sun X. Emission-diffusion theory of the MOSFET. IEEE Trans Electron Dev 2015;62(12):4174–8.
[12] Tejada JAJ, Awawdeh KM, Villanueva JAL, Carceller JE, Deen MJ, Chaure NB, et al. Contact effects in compact models of organic thin film transistors: application to zinc phthalocyanine-based transistors. Org Electron 2011;12(5):832–42.
[13] López-Varo P, Jiménez-Tejada JA, Marinov O, Carceller JE, Chen CH, Deen MJ. Boundary condition model for the simulation of organic solar cells. Org Electron 2017;48:85–95.
[14] Romero A, González J, Picos R, Deen MJ, Jiménez-Tejada JA. Evolutionary parameter extraction for an organic TFT compact model including contact effects. Org Electron 2018;61:242–53.
[15] Marinov O, Deen MJ. Quasistatic compact modelling of organic thin-film transistors. Org Electron 2013;14(1):295–311.
[16] Mark P, Helfrich W. Space-charge-limited currents in organic crystals. J Appl Phys 1962;33(1):205–15.
[17] Wright GT. Threshold modelling of MOSFETs for CAD of CMOS-VLSI. Electron Lett 1985;21(6):223.
[18] Yarmoghaddam E, Haratipour N, Koester SJ, Rakheja S. A virtual-source emission-diffusion I-V model for ultra-thin black phosphorus field-effect transistors. J Appl Phys 2019;125(16):165706–18.
[19] Lee CS, Pop E, Franklin A, Haensch W, Wong HSP. A compact virtual-source model for carbon nanotube FETs in the Sub-10-nm regime – part I: intrinsic elements. IEEE Trans Electron Dev 2015;62(9):3061–9.
[20] Marinov O, Jamal Deen M, Feng C, Wu Y. Precise parameter extraction technique for organic thin-film transistors operating in the linear regime. J Appl Phys 2014;115(3):034506–11.
[21] Deen MJ, Marinov O, Zschieschang U, Klauk H. Organic thin-film transistors: part II-parameter extraction. IEEE Trans Electron Dev 2009;56(12):2962–8.
[22] Marinov O, Deen MJ, Datars R. Compact modeling of charge carrier mobility in organic thin-film transistors. J Appl Phys 2009;106(6):064501–14.
[23] Li L, Lu N, Liu M, Bässler H. General Einstein relation model in disordered organic semiconductors under quasiequilibrium. Phys Rev B 2014;90(21). 214107–6.
[24] Manaka T, Lim E, Tamura R, Iwamoto M. Direct imaging of carrier motion in organic transistors by optical second-harmonic generation. Nat Photonics 2007;1(10):581–4.
[25] Kakudate T, Yoshimoto N, Saito Y. Polymorphism in pentacene thin films on SiO2 substrate. Appl Phys Lett 2007;90(8):081903–4.
[26] Kalb WL, Batlogg B. Calculating the trap density of states in organic field-effect transistors from experiment: a comparison of different methods. Phys Rev B 2010;81(3). 523–13.

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