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Influence of crystal defect density of silicon wafers on potential-induced degradation (PID) in solar cells and modules

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Potential-induced degradation (PID) was recently identified as one of the most important degradation mechanisms. It can be due to many different reasons during the manufacture and application of solar energy system. In this study, the effect of defect density of silicon wafers on the PID phenomenon is revealed by PID simulation tests at both the cell and module levels. Silicon wafers of the same and different crystal structures with various defect densities are studied, respectively. The results, which are coincident, showed that the extent of PID has a positive correlation with defect density. The increased defect density can lead to a drastic decline in R_{sh}, finally promoting the PID phenomenon. Silicon wafers with the lowest defect density demonstrate the least current leakage and highest PID resistance after PID simulation tests. Therefore, the result of this study shows the correlation between the PID strength of solar cells and defect density of silicon wafers, which can be easily measured during wafer manufacture.

1 Introduction Silicon solar cells, acting as the main force of solar energy, have been widely used recently due to their merits of environment friendliness and mature manufacture process compared to other solar technologies. However, during the running of the solar power station, different failure modes arise according to its complex operating conditions [1, 2]. Potential-induced degradation (PID) is one of the most common degradation phenomena caused by a high negative bias and harsh environments [3–5].

Nowadays, there are still some debates on the mechanism of the PID phenomenon. The most accepted one is the migration of Na^+ under the electrical field between the aluminum frame and solar cells, which formed the so-called shunts and led to the degradation in solar cell efficiency [6]. Bauer et al. [7] thought that positive ions (e.g., Na^+) in the vicinity of the Si surface are expected to increase the electron concentration in the emitter rather than inverting it, the accumulation of negative charges will destroy the original p–n junction of the solar cell, thus leading to the leakage current. Lausch et al. [8] found that PID-affected sites always produced stacking faults decorated with Na atoms, implying the stacking faults can make a contribution to the PID phenomenon. They also prove that the Na^+ not only comes from the glass but also may arise from contamination present on the solar cell surface [9]. For p-type c-si modules, on a macroscopic level, many reasons have been proposed that can influence the PID, such as the temperature, humidity, voltage, the materials used during module manufacture and so on [10, 11]. Different methods have been applied to suppress the PID depending on those correlations, including the utilization of advanced materials like sodium-free glasses, resistive encapsulants [12–14], the application of a reverse potential at night [15–17], and the improvement in the antireflecting coating (ARC) layer [18–20].

According to the former studies, Na^+ and stacking faults in crystalline silicon can be responsible for PID, and many methods were applied during the manufacture to prevent the diffusion of Na^+. However, for now, there is no corresponding research to show the correlation between the crystal defect density under photoluminescence (PL) and the PID phenomenon, and no measures have been taken at the wafer source to prejudge the PID. In this study, multicrystalline silicon with various defect densities as well as monocrystalline silicon, monolike-crystalline silicon solar cells are studied to reveal the impact of defect density on the PID phenomenon, a PIDcon device and a climate chamber are employed to simulate the PID phenomenon, power loss and electrical performance after PID simulation text are analyzed to investigate their correlation.

2 Experimental

2.1 Fabrication of solar cells and minimodules Four groups of multicrystalline wafers ($156 \times 156\,mm^2$, p-type, thickness of 190 μm, resistivity of 1–3 Ω cm) with different defect densities were selected according to their PL and electroluminescence (EL) images. All the multicrystalline wafers are from the same ingot, wafers in the same group are adjacent in order to ensure their homologous crystalline structure. All the wafers are processed into solar cells in the same batch on the same conventional mass production line. Their production processes include texturing (acidic method), diffusion, etching, PECVD (SiN_x coating), and silk-screen printing. After each process, the main parameters are tested, including the square resistance, thickness, refractive index of SiN_x, and so on, these parameters are recorded for the selection of the PID test.

In order to further understand the impact of defect densities on the PID phenomenon, monocrystalline silicon with low defect density and monolike-crystalline silicon with high defect density are also studied as comparative groups, and they were manufactured on the same solar cell production line by using the same process. It should be noted that during the manufacture of monocrystalline solar cells, the same acidic texturing method is used instead of the alkali method in order to keep the same process. All the solar cells are encapsulated into minimodules for the purpose of PID module testing.

2.2 PID test Two different kinds of methods are used to simulate the PID phenomenon of solar cell and module, respectively. At the solar-cell level, the PID test is accomplished by a PIDcon device. It is a very easy and convenient method that opens up the opportunity to test the materials and solar cell before module lamination, more details can be found in Ref. [16]. The solar cell was placed on a temperature-controlled aluminum platform, which also acts as the rear electrode, then the solar cell was covered by EVA and glass ($100 \times 100\,cm^2$) in that order. On the front side, a contact needle is used as the electrode, which can be pressed on the busbar of solar cells when the box is closed. In this study, the experimental parameters are set as follows: preheating temperature 80 °C, preheating time 5 min, testing voltage 1500 V, temperature 85 °C, time 24 h. At the solar module level, PID testing is accomplished in a climate chamber according to the standard of international engineering consortium (IEC62804), the minimodules are covered by aluminum foil to simulate the aluminum frame of a standard module. The parameters are set as follows: temperature 85 °C, humidity 85%, bias voltage 1000 V, time 96 h.

During the PID test, the solar cells selected from different groups must have similar square resistance, thickness, refractive index of SiN_x and R_{sh}. The materials and room temperature are the same in the whole testing. The purpose of this is to avoid the effect of other factors.

2.3 Equipment PL images are acquired with a PLI-101 of Semilab company. EL images before and after PID testing are acquired with an OPT-EL-M600, and electrical performances are characterized by Berger equipment under standard test condition ($1000\,W\,m^{-2}$, AM1.5).

3 Result and discussion Multicrystalline silicon samples of different defect densities were selected by a PLI-101 device, a device that has been widely used in the solar-cell industry to detect the quality of silicon wafers before production. It is a PL machine integrated with lifetime measurement, and some crystal defects can be recognized according to the lifetime detected by the PLI device, and different types of defects can be differentiated by the accumulation features of the defects. In this study, two types of crystal defects are roughly separated by the PLI-101 equipment. The first type are grain boundaries with contamination. At the locations where different grains meet, strain fields can attract contamination and leading to an increased recombination activity [21], these are marked by green lines in the PL image. The second type are dislocations, since it has been studied by Secco etching that dislocations always have a line-like feature, the accumulated purple lines under PL are identified as dislocations by the PLI-101. Nevertheless, both of them are crystal defects. PL images of multicrystalline wafers in different groups are shown in Fig. 1. It can be seen from this that their crystal defect densities increased gradually from group A to group D. The defect area percentage can be calculated by LingoPL software, the software divided the whole image into many pixels, the defect area percentage is calculated according to the number of the pixels marked as defects. From group A to group D, the average defect area percentages are 3.69, 6.55, 10.11, and 11.15%, respectively. After solar-cell manufacture, the average conversion efficiency of four groups are 18.38, 18.22, 18.11, and 18.09%, respectively. As shown in Fig. 1e, the increased defect area percentage will lead to a decrease in solar-cell efficiency because of the increased stress/strain and combination centers in higher defect density silicon.

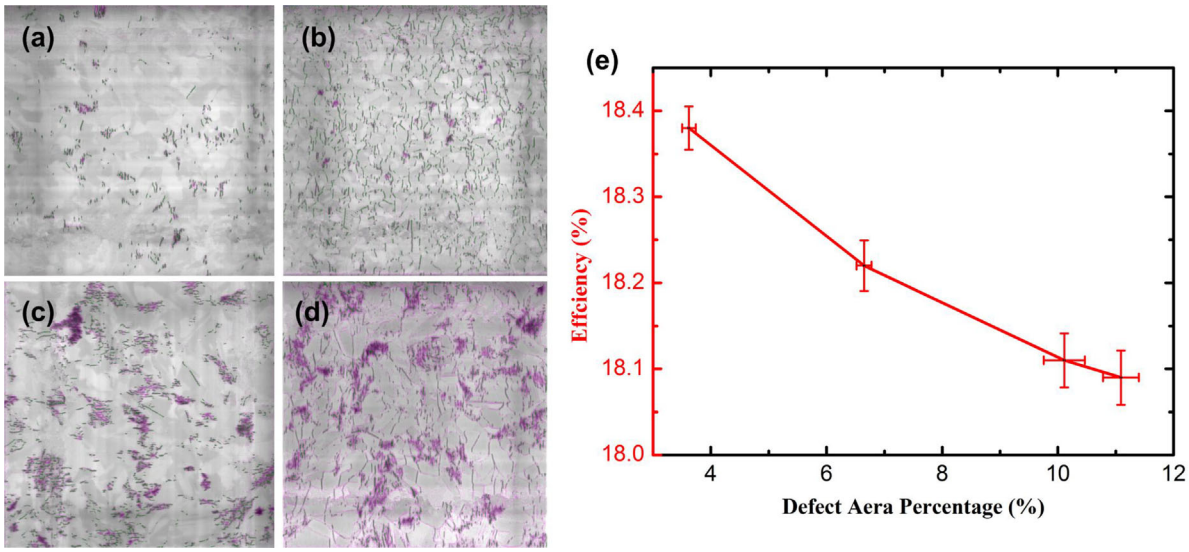

Figure 1 (a–d) PL images of multicrystalline silicon wafers with different defect area percentages, (e) efficiency as a function of defect area percentage.

In order to investigate the influence of defect density on the PID phenomenon, a PID test is performed at the cell level, where solar cells with similar parameters are selected from each group for the test. The results of the PID test are shown in Fig. 2. When the testing time increased, the parallel resistance (R_{sh}) decreased drastically in the first few hours and finally reached a stable numerical value. This suggested that the so-called shunts have occurred in all the groups of solar cells under the voltage of 1500 V and a temperature of 85 °C. Moreover, the black arrow in Fig. 2 indicates that wafers with higher defect density spent shorter times to reach the stable situation. This suggests that defects can accelerate the occurrence of shunts and the PID phenomenon. The inset of Fig. 2 is the magnification of the R_{sh} curves in the last few hours, and it can be seen from the picture that from A to D, the R_{sh} numerical value is getting smaller and reaches a stable status eventually, indicating that wafers with higher defect density will lead to more shunts.

It has been reported that PID is associated with the reduction of R_{sh}, a lower R_{sh} will result in a lower V_{oc}, thereby further decreasing the conversion efficiency, the estimated correlation between power loss and R_{sh} according to the PIDcon device are shown in Eq. (1) [16].

$$\frac{\Delta P}{P_0} = 100\% \times \frac{V_{mpp} \times A_{Cell}}{R_{sh} \times I_{mpp} \times A_{pid}}. \quad (1)$$

where ΔP is the absolute power loss, P_0 is the nominal power under standard test condition (STC), V_{mpp} is the voltage at maximum power, I_{mpp} is the current at maximum power, R_{sh} is the measured parallel resistance, A_{cell} and A_{pid} are the cell area and PID-tested area, respectively.

According to the equation, the power losses of the four groups are calculated and displayed in Fig. 3. Figure 3a shows the trend of power loss of the four cells, the results are similar to the R_{sh} results mentioned above, the change rate of power loss gradually increased when the defect density increased. Their correlation is shown in Fig. 3b, the power losses of four groups are 25.41, 30.92,

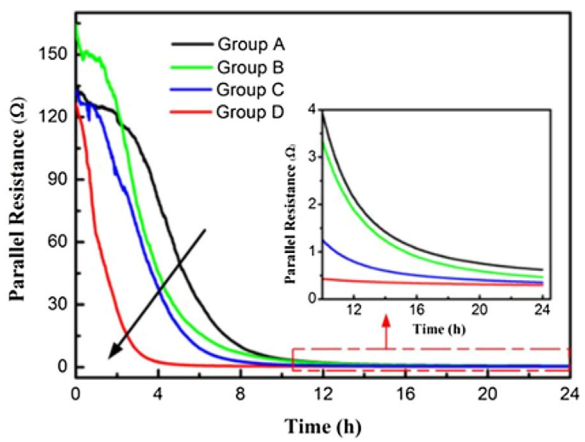

Figure 2 Plot of the parallel resistance versus PID testing time.

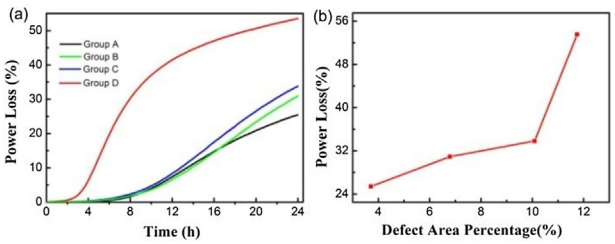

Figure 3 (a) Power loss of four groups versus time, (b) power loss as a function of defect area percentage.

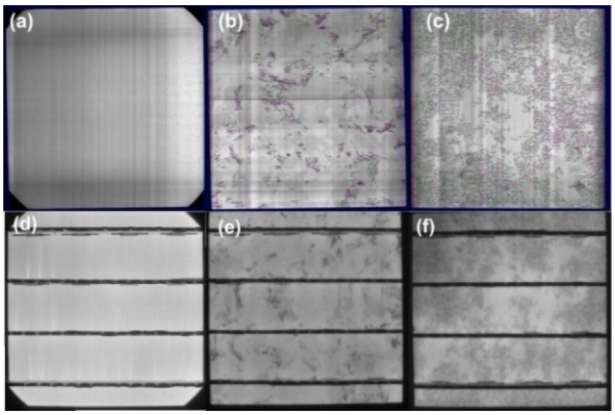

Figure 4 PL images of (a) monocrystalline silicon, (b) multicrystalline silicon, (c) monolike-crystalline silicon. EL images of (d) monocrystalline silicon, (e) multicrystalline silicon, (f) monolike-crystalline silicon.

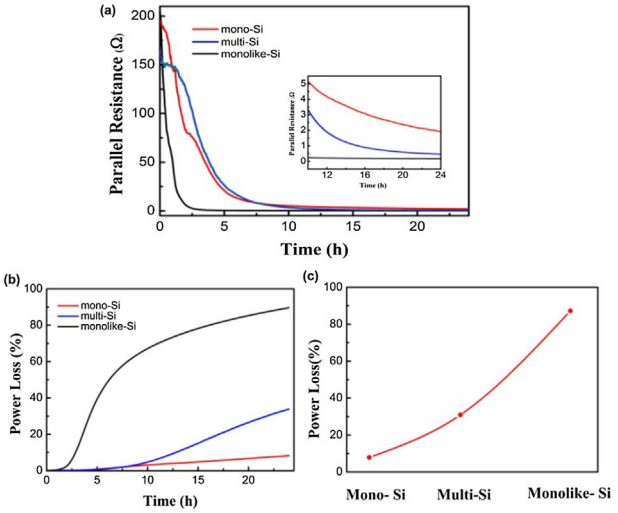

Figure 5 (a) Plot of the parallel resistance of different crystal structure silicon versus PID testing time, (b) power loss of different crystal structure silicon versus time, (c) power loss as a function of defect area percent.

33.81, and 53.53%, respectively, as the defect density increased, the PID phenomenon becomes more and more serious. This may due to the Na^+ diffusion in defects, the radius of Na atoms is larger than that of silicon atoms, so Na atoms in vacancy sites will increase lattice expansion around the silicon atoms [22], which will decrease the vacancy formation energy, further resulting in a higher vacancy equilibrium concentration. When the defect density increased in cells, Na^+ can go through the p–n junction much more easily, leading to a short circuit between the emitter and the collector electrode and eventually turns into leakage current. This kind of phenomenon is very similar to the "tunnel mechanism" of semiconductor failure mode.

Monocrystalline silicon with a low defect density and monolike-crystalline with a high defect density are employed as comparative groups. Usually, the defect density in monolike crystalline silicon should be smaller than that in multicrystalline silicon, however, in this study, monolike crystalline wafers on the top of silicon ingot with exceedingly high defect densities are selected to make the comparison more obvious. Their PL and EL images are shown in Fig. 4. Figure 4a is the image of a monocrystalline silicon wafer, it has very uniform brightness and hardly find any grain boundaries and defects can be seen. Figure 4b is the image of multicrystalline silicon wafer, grain boundaries and many dislocations can be recognized from the purple and green areas. Figure 4c is the image of monolike-crystalline silicon, it has more defects compared to multicrystalline silicon. Figure 4e and f are their EL images corresponding to (a–c), the location of shadows completely matched the purple and green parts on the PL image, which further proves the increased defect density in these three types of solar cells.

The same PIDcon test method mentioned above is used to evaluate the PID phenomenon of mono-, multi-, and monolike-crystalline silicon, and the results are shown in Fig. 5. Figure 5a shows the time dependence of the R_{sh}, all the cells show a typical degradation behavior the same as Fig. 2. It can also be seen from the inset of Fig. 5a that a monocrystalline solar cell has the highest R_{sh}, followed by multi- and monolike silicon, corresponding to the growth of defect density. The power losses of the three kinds of cells are shown in Fig. 5b and c, after 24 h degradation, their power loss are 7.9, 30.92, and 87.24%, respectively. This result further confirms the influence of the defect density on the PID phenomenon. In addition, it can also be seen from Fig. 5b that the power reduced very slowly in mono- and multicrystalline silicon, while it decreased very fast in monolike-crystalline solar cell in the first few hours. This is not only due to the high defect density in monolike-crystalline solar cell but also the large accumulation area of dislocations and contamination. The accumulation of the defects can make Na^+ depositing more easily, and further accelerate the PID phenomenon.

The PID tests at the module level are also conducted to support the results at the cell level. Figure 6 shows a picture of a minimodule and the EL images before and after PID testing. All the modules degraded heavily after PID testing,

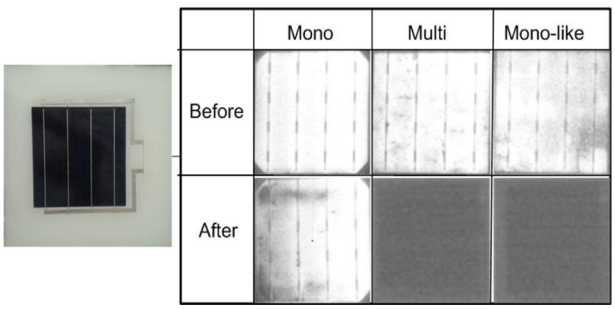

Figure 6 Picture of minimodule and the EL images before and after PID testing.

Table 1 Electric performance parameters before and after PID.

	efficiency (%)	V_{oc} (V)	I_{sc} (A)	FF (%)	R_{sh} (Ω)
mono					
before	17.77	0.641	9.19	73.44	89.44
after	11.9	0.619	8.47	55.19	21.45
multi					
before	17.23	0.629	9.208	72.47	107.45
after	4.68	0.38	8.22	36.41	0.11
mono-like					
before	16.54	0.618	9.102	71.55	139.41
after	0.77	0.121	6.051	25.58	0

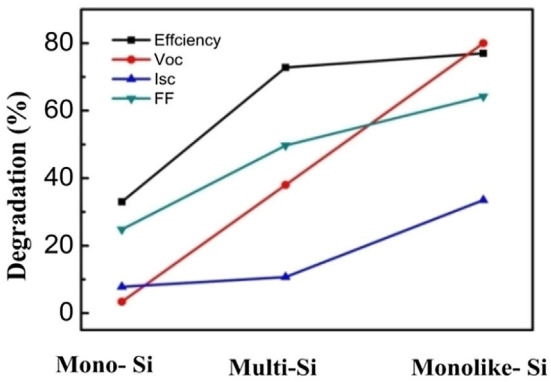

Figure 7 Electrical performance parameters of different solar cells.

multi- and monolike-crystalline samples totally turned black, while some parts of the monocrystalline remained bright, which proves that the mono-sample has the best resistance to the PID phenomenon, which is attributed to its low defect density. Since the last two modules are completely short circuited, electric performance parameters are measured to analysis their anti-PID performance. The results are shown in Table 1, it can be seen from the table that all the modules have an obvious decline in all the electric performance parameters. However, their ranges of decline are different, more details are shown in Fig. 7, from mono- to monolike-crystalline solar cells, the rates of efficiency degradation are 33, 78, and 98.3%, respectively, the degradation increases with the increase of defect density, further supporting the results we already have at the cell level. Moreover, it can be seen from Fig. 7 that when the defect density is increased, all the electric performance parameters have a tendency to decrease, including I_{sc}, V_{oc}, and fill factor, and among all the parameters, the V_{oc} changed most clearly, and almost have a linear correlation with the defect density, which is because R_{sh} has the strongest impact on V_{oc} compared to other parameters. The results of the PID testing at the module level perfectly match the results at the cell level conducted by a PIDcon device.

4 Conclusions PID tests at both cell and minimodule levels are conducted in this paper to reveal the correlation between the defect density and the PID phenomenon. In the series of multicrystalline silicon, the PID phenomenon became more and more serious with the increase of defect area percentage. In different crystal structures of silicon material, monocrystalline silicon with the lowest defect area percentage showed the highest tolerance to PID, followed by a multicrystalline silicon with a medium defect area percentage and a monolike-silicon with the highest defect area percentage. Na^+ diffusion in defects is considered to be the main reason leading to the decline of R_{sh} then V_{oc} and subsequently efficiency. Therefore, at the silicon wafer level, the higher defect density can lead to greater PID strength of solar cells. The results could be significant for solar-cell factories during manufacture.

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