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# Effects of temperature on series resistance determination of electrodeposited Cr/*n*-Si/Au–Sb Schottky structures

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ABSTRACT

Temperature dependences of the series resistance in the Cr/*n*-Si/Au–Sb Schottky structures prepared by electrodeposition method have been studied using current–voltage (*I–V*) characteristics in the 80–320 K temperature range by steps of 20 K. However, the values of series resistance obtained from Cheung functions were compared with each other, and it was seen that there is a good agreement between the values of the series resistance. A modified Norde's function combined with conventional forward *I–V* method was used to extract the parameters including barrier height and the series resistance. The barrier height and series resistance obtained from Norde's function were compared with those from Cheung functions. The values of barrier height and series resistance have very different especially towards to the lower temperatures. This is attributed to non-ideal *I–V* characteristics of the Cr/*n*-Si/Au–Sb Schottky structure and non-pure thermionic emission theory due to the low temperature effects.



## 1. Introduction

Metal–semiconductor (MS) structures play an important role in integrated device technology, and these structures have been extensively investigated due to their technological applications. Si is one of the important materials used for semiconductor devices, light emitting diodes and solar cells [1–4]. Ideal metal–semiconductor structures are considered to be intimate, abrupt and laterally homogeneous, and the continuum of the metal-induced gap states (MIGS) determines their barrier heights [5]. The fact that the fundamental physical mechanisms that determine Schottky barrier diode (SBD) parameters such as ideality factor $n$ and the barrier height $\Phi_b$ are fully understood are of vital importance to all electronic and optoelectronics device [6–10]. The barrier height is an important parameter that determines the electrical characteristics of metal–semiconductor structures. The ideality factor is a measure of conformity of the diode to the pure thermionic emission. The series resistance is an important parameter, which causes the electrical characteristics of Schottky structures to be non-ideal. The formation of more reliable and thermally stable Schottky barrier diodes (SBDs) is essential for the application of power amplifiers and optoelectronic devices operating at different temperatures. Therefore, it is necessary to understand the behaviour of metal contacts to Si at different temperatures. At the same time, the fabrication of these structures plays a crucial role in the construction of some useful devices.

The choice of electrodeposition is motivated by the possibility of fabricating Schottky structures by obtaining good quality metal layers on semiconductors [11,12]. Many metallic systems (such as Pt, Cu, Au, Ag, Pb, etc.) on *n*-Si were investigated by electrodeposition [13–17]. Many of these works focused in the fundamentals of nucleation and growth modes as well as the charge transfer mechanisms during electrodeposition [18–20]. However, only a few works present a detailed study of the electrodeposition of Co, Ni [21–23]. The evaporation of Cr is not an easy process. Electrodeposition is low-temperature, cost effective, and particularly attractive for its vital role in the fabrication of self-assembled magnetic nanostructures where line-of-sight techniques do not work [24–28]. Among the different methods available for metallization of Si surfaces, vacuum deposition is the usual metallization method. However, electrodeposition is an advantageous alternative to the common expensive physical technologies for the metallization of semiconductors. This technique can especially be preferred for the deposition of metals with high melting points such as Cr, Ni, Co, etc., which are very difficult to evaporate by physical techniques [20,21,23,27,28]. Moreover, it provides the possibility of depositing film structures different from those being produced from the vapour phase. Recently, the electrodeposition technique also offers several advantages in the preparation of semiconduct-

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ing compound and alloy films [20–28]. Moreover, film thickness, morphology and composition can be controlled easily by voltage and current density in this technique. Consequently, Si is an important integral for very-large-scale integration (VLSI) circuits in many applications.

The analysis of the current–voltage characteristics of the Schottky structures obtained only at room temperature does not give detailed information about the charge transport process and about the nature of the barrier formed at the metal semiconductor interface. The temperature dependent studies of the Schottky structures enable us to understand the charge transport process through metal semiconductor contact and also give a better picture of the conduction mechanisms [29–34]. For this, in this work, the variations in electrical characteristics of Cr/*n*-Si Schottky structure have been systematically investigated as a function of temperature using current–voltage measurements in a wide temperature (80–320 K) range. The characteristic parameters of the structure such as barrier height, ideality factor and series resistance were determined from the current–voltage measurements. Also, Cheung functions and Norde method were used to plot the *I–V* characteristics and, to extract the characteristic parameters of the Schottky contact.

## 2. Experimental procedure

The *n*-type Si wafer used in this study was (1 0 0) oriented and with free carrier concentration of $1.25 \times 10^{15}$ cm$^{-3}$ obtained from the reverse bias $C^{-2}$–*V* characteristics at room temperature. The wafers were chemically cleaned using the RCA cleaning procedure [i.e., a 10 min boil in $NH_4OH + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$]. The native oxide on the front surface of the substrates was removed in HF:$H_2O$(1:10) solution and finally the wafer was rinsed in de-ionized water for 30 s. Then, low resistivity ohmic back contact to the *n*-type Si wafer was made by using Au–Sb alloy, followed by a temperature treatment at 420 °C for 3 min in $N_2$ atmosphere. The electrodeposition of Cr Schottky contacts on the *n*-Si substrate was carried out in the galvanostatic mode from an electrolyte containing $CrO_3$ (250 g/l) and $H_2SO_4$ (2.5 g/l) at room temperature. The Schottky structures were formed on the front face of the *n*-Si substrate as dots with diameter of about 1 mm (the diode area = $7.85 \times 10^{-3}$ cm$^2$) by the galvanostatic electrodeposition of Cr. Acid resistant adhesive tape was used to mask off all the substrate except for the deposition area. A Pt plate was used as anode while the *n*-Si substrate was connected as cathode. A current density of 100 mA/cm$^2$ was maintained between the two electrodes. Film thickness was adjusted as 150 nm by deposition time.

The *I–V* characteristics of the devices were measured in the temperature range of 80–320 K using a temperature controlled janes vpf-475 cryostat, which enables us to make measurements in the temperature range of 80–320 K, and a Keithley 220 programmable constant current source and a Keithly 199 dmm/scanner under dark conditions. The sample temperature was always monitored by using a copper–constantan thermocouple and a lakeshore 321 auto-tuning temperature controller with sensitivity better than ±0.1 K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card. The schematic structure of the Cr/*n*-Si Schottky diode is shown in Fig. 1.

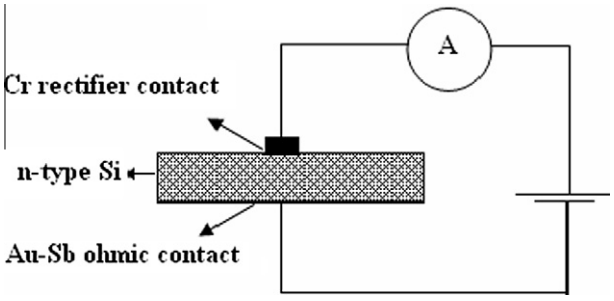


**Fig. 1.** The schematic structure of the Cr/*n*-Si Schottky structure.

## 3. Results and discussion

The plots obtained from the current–voltage (*I–V*) measurements of the Cr/*n*-Si (MS) Schottky structure in the temperature range of 80–320 K are shown in Fig. 2. The *I–V* measurements are one of the methods to determine the some electrical properties in Schottky structures. The diode parameters are determined from the forward bias *I–V* characteristics, which is usually described within the thermionic emission theory. If a Schottky diode with a series resistance is considered, it is assumed that the forward bias-thermionic emission current of the device can be expressed as [35,36]:

$$I = AA^*T^2\left(-\frac{q\Phi_{bo}}{kT}\right)\exp\left(-\frac{q(V-IR_S)}{nkT}\right) \quad (1)$$

where *V* is the applied voltage drop across the junction, *q* is the electronic charge, *k* is Boltzmann's constant ($8.62 \times 10^{-5}$ eV/K), *T* is the absolute temperature in Kelvin, *n* is the diode ideality factor and $I_0$ is the saturation current. $I_0$ is obtained from the intercept of ln *I* versus *V* plot (Fig. 2) at *V* = 0, and is expressed as [2,3,35–37]:

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{bo}}{kT}\right) \quad (2)$$

where *A* is the diode area (=0.00785 cm$^2$), $A^*$ is the effective Richardson constant (112 A cm$^{-2}$ K$^{-2}$) based on effective mass of *n*-Si [2,3,20–23,36] and $\Phi_{bo}$ is the zero-bias barrier height. Once $I_0$ is determined, the zero-bias barrier height ($\Phi_{bo}$) is obtained by rewriting Eq. (2) as:

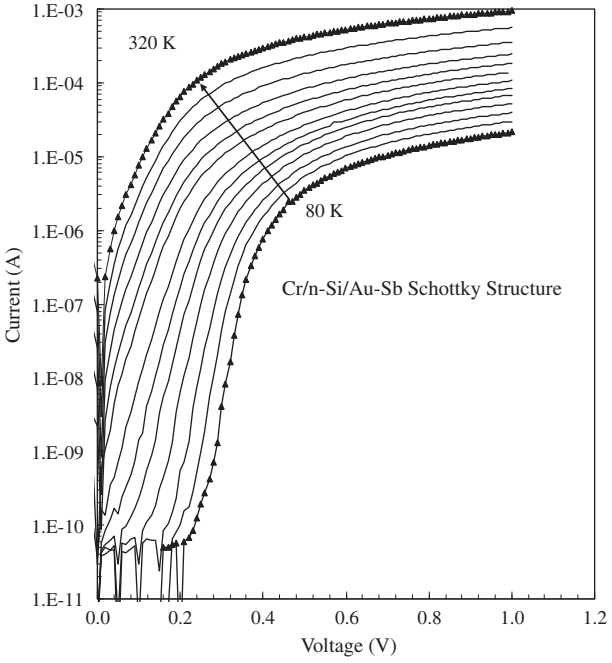


**Fig. 2.** Current–voltage characteristics of the Cr/*n*-Si Schottky structure as a function of temperature.

$$\Phi_{bo} = \frac{kT}{q}\ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \tag{3}$$

The ideality factor, $n$, is a measure of conformity of the diode to pure thermionic emission. If the ideality factor $n$ is equal to one, the pure thermionic emission is occurring. However, $n$ has usually a value greater than unity and it is obtained from the slope of the straight line region of the semi-log forward bias $I$–$V$ characteristics through the relation;

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{4}$$

The barrier height (BH) $\Phi_{bo}$ and ideality factor $n$ values of the Cr/$n$-Si/Au–Sb Schottky structure were calculated with the help of Eqs. (3) and (4) from the $y$-axis intercept and slope of the linear region of the semi-log-forward bias $I$–$V$ plots, respectively. The ideality factor has been found to increase, while the zero-bias barrier height $\Phi_{bo}$ decrease with decreasing temperature. The experimental value of barrier height ($\Phi_b$) and the ideality factor ($n$) obtained from $I$–$V$ measurements for the Cr/$n$-Si/Au–Sb structure Schottky structure change from 0.316 eV and 2.257 (at 80 K) to 0.688 eV and 1.211 (at 320 K), respectively. These experimental values are given in Table 1. Since current transport across the metal–semiconductor interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers and therefore current transport will be dominated by current flowing through patches of the lower Schottky barrier height and a larger ideality factor [29,37,38]. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barriers. As a result, the dominant barrier height will increase with the temperature and bias voltage. The high values of ideality factor $n$ can be attributed to the presence of the thin interfacial native oxide layer between the metal and semiconductor [37–39]. On the other hand, the high values of $n$ can be attributed to the effects of the bias voltage drop across the interfacial layer and series resistance, therefore, of the bias voltage dependence of the barrier height, and/or such as a thin interface insulator layer, probably the oxide layer ($SiO_2$ or SiOx), may be form natively at Cr and $n$-Si interface layer.

The methods to extract information for the series resistance $R_S$ of Schottky structures have been suggested [40,41]. In our study, we have applied the methods developed by Cheung and Cheung [40] and Norde [41]. For the present, to determine diode parameters such $n$, $\Phi_b$ and $R_S$, let us obtain the functions of Cheung and Cheung [40]. The Cheung's method is achieved by using the functions:

$$\frac{dV}{d(\ln I)} = IR_S + n\frac{kT}{q} \tag{5}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{6}$$

where $H(I)$ can be written as:

$$H(I) = IR_S + n\Phi_{bo} \tag{7}$$

Eq. (5) should give a straight line for the data of downward curvature region of the forward bias $I$–$V$ characteristics. Therefore, the slope and $y$-axis intercept of a plot of $dV/d\ ln(I)$ versus $I$ will give $R_S$ and $nkT/q$, respectively. The plots associated with this function are given in Fig. 3 as a function of temperature. Using the $n$ value determined from Eq. (5) and the data of downward curvature region in the semi-log forward bias $I$–$V$ characteristics in Eq. (6), a plot of $H(I)$ versus $I$ according to Eq. (7) will also give a straight line with $y$-axis intercept equal to $n\Phi_b$. The slope of this plot also provides a second determination of $R_S$ which can be used to check the consistency of Cheung's approach. The plots associated with this function are given in Fig. 4 as function of temperature. The values of series resistance obtained from Figs. 3 and 4 as function of temperature are given in Table 1. As seen in Table 1, the values of series resistance obtained from $H(I)$–$I$ plots, are appropriate with obtained from $dV/d\ \ln I$–$I$ plots. It is shown that the series resistances obtained from both plots are appropriate with each other. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. The average series resistance values of the Cr/$n$-Si/Au–Sb Schottky structure are varied from 26.344 to 0.807 kΩ: the barrier heights are increased from 0.193 to 0.292 eV and the ideality factors are decreased from 3.19 to 1.55 with increasing temperature, respectively. However, it can clearly be seen that there is a relative difference between the values of the ideality factor obtained from the downward curvature region of the forward bias $I$–$V$ plots and from the linear regions of the same characteristics. This difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the Schottky barrier height, according to the voltage drop across the interfacial layer and charge of the interface states with bias in this concave region of the current–voltage plot [36]. Due to the potential drop across the interfacial layer, the zero bias barrier height is lower than that expected in an ideal diode, and similarly the potential across the interfacial layer varies with bias because of the electrical field present in the semiconductor and the change in the interface [42].

The second method proposed by Norde is an alternative method to determine the values of the series resistance and barrier height, and is based on plotting several functions [41]:

**Table 1**
The experimental parameters obtained from different methods as a function of temperature for the Cr/$n$-Si Schottky structure.

| $T$ (K) | $n$ $IV$ | $n$ Cheung | $\Phi_b$ (eV) $IV$ | $\Phi_b$ (eV) Cheung | $\Phi_b$ (eV) Norde | $R_S$ (Cheung) $H(I)$ (kΩ) | $R_S$ (Cheung) $dV/d\ \ln(I)$ (kΩ) | $R_S$ (Norde) (kΩ) |
|---|---|---|---|---|---|---|---|---|
| 80 | 2.257 | 3.19 | 0.316 | 0.193 | 0.492 | 26.474 | 26.215 | 138.937 |
| 100 | 1.622 | 2.94 | 0.399 | 0.199 | 0.509 | 19.192 | 17.461 | 41.6322 |
| 120 | 1.494 | 2.74 | 0.440 | 0.209 | 0.528 | 14.807 | 13.100 | 38.818 |
| 140 | 1.423 | 2.53 | 0.487 | 0.225 | 0.544 | 11.250 | 9.777 | 29.312 |
| 160 | 1.398 | 2.35 | 0.498 | 0.242 | 0.56 | 8.918 | 7.632 | 21.649 |
| 180 | 1.359 | 2.24 | 0.527 | 0.252 | 0.583 | 7.517 | 6.402 | 13.806 |
| 200 | 1.341 | 2.14 | 0.553 | 0.265 | 0.599 | 6.062 | 5.234 | 11.230 |
| 220 | 1.312 | 2.02 | 0.576 | 0.268 | 0.613 | 4.923 | 4.222 | 8.729 |
| 240 | 1.285 | 1.90 | 0.599 | 0.271 | 0.631 | 3.853 | 3.397 | 5.098 |
| 260 | 1.266 | 1.79 | 0.624 | 0.277 | 0.649 | 2.947 | 2.777 | 3.343 |
| 280 | 1.248 | 1.73 | 0.646 | 0.278 | 0.671 | 2.058 | 2.108 | 1.720 |
| 300 | 1.218 | 1.66 | 0.671 | 0.283 | 0.691 | 1.261 | 1.440 | 0.942 |
| 320 | 1.211 | 1.55 | 0.688 | 0.292 | 0.707 | 0.642 | 0.973 | 0.466 |

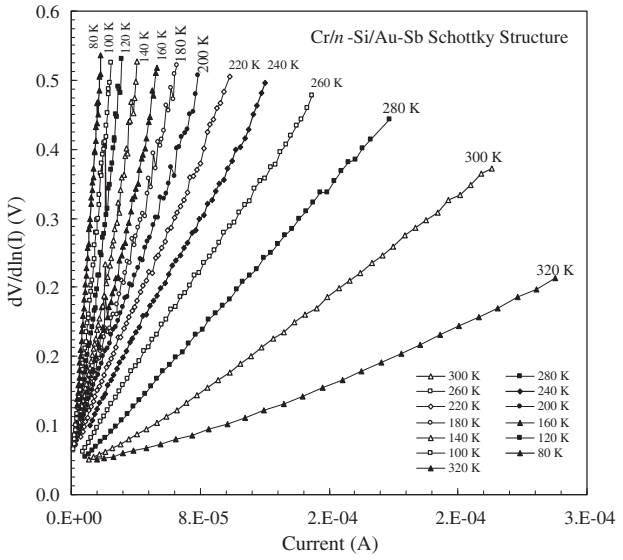


**Fig. 3.** Experimental $dV/d(\ln I)$–$I$ curves of the Cr/$n$-Si Schottky structure as a function of temperature.

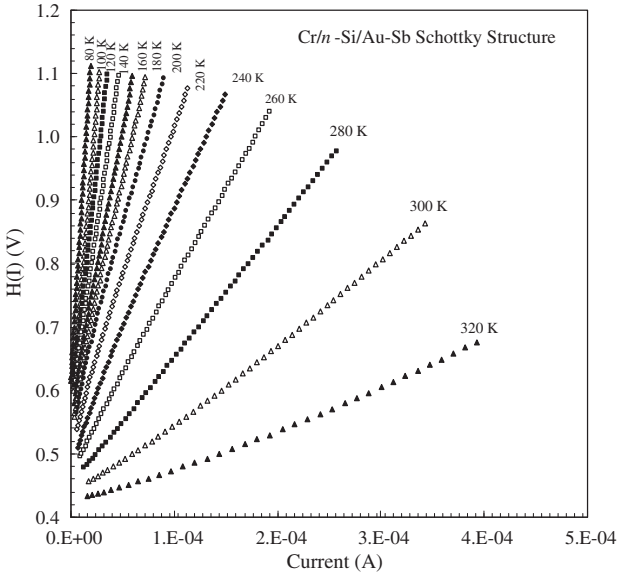


**Fig. 4.** Experimental $H(I)$–$I$ curves of the Cr/$n$-Si Schottky structure as a function of temperature.

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{8}$$

where $\gamma$ is the first integer (dimensionless) greater than ideality factor, and $I(V)$ is the current obtained from the $I$–$V$ curve and the other parameters are described above. Therefore, the barrier height and series resistance can be determined by

$$\Phi_{bo} = F(V_0) + \left[\frac{\gamma - n}{n}\right]\left[\frac{V_0}{\gamma} - \frac{kT}{q}\right] \tag{9}$$

where $F(V_0)$ is the minimum value of $F(V)$, $V_0$ is the corresponding voltage. Fig. 5 shows the $F(V)$–$V$ plots of the Cr/$n$-Si/Au–Sb Schottky structure as a function of increasing temperature. From Norde's functions, the series resistance ($R_S$) value can be determined as:

$$R_S = \frac{\gamma - n}{I}\frac{kT}{q} \tag{10}$$

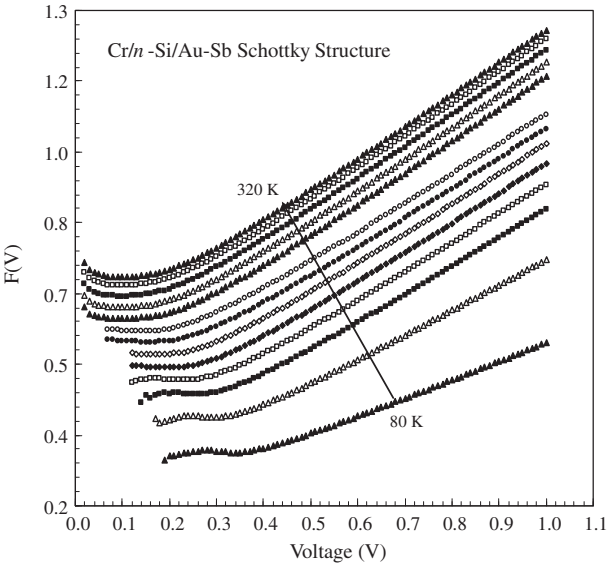


**Fig. 5.** $F(V)$ versus $V$ plot of the Cr/$n$-Si Schottky structure at various temperature.

Once the minimum of the $F$ versus $V$ plot is determined, the value of barrier height can be obtained from Eq. (9). As seen in Table 1, the values of the barrier height and series resistance obtained from the Norde's functions have been slightly changed with increasing temperature. It can be said that, especially, the values of series resistance obtained from both methods are slightly different from each other. In most cases, the parameters obtained from the Cheung functions and the Norde's functions are not in agreement with each other. From the $F(V)$–$V$ plots, the values of the barrier height and series resistance ($R_S$) have been determined as 0.707 eV; 0.466 kΩ at 320 K and 0.492 eV; 138.937 kΩ at 80 K, respectively. In general, the values obtained from the Cheung methods are lower than obtained from the Norde's method. Because, the Cheung functions are only applied to the nonlinear region (high voltage region) of the semi-log forward bias $I$–$V$ characteristics whereas, the Norde's functions are applied to the full forward bias $I$–$V$ characteristics of the junctions.

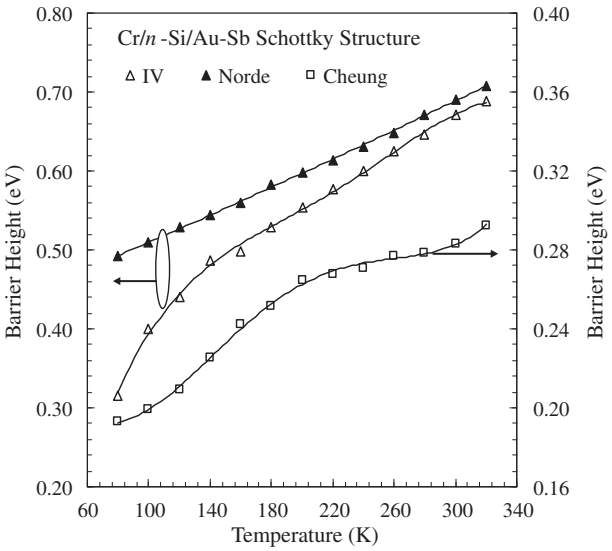


**Fig. 6.** Temperature dependence of the barrier heights obtained from Cheung and Norde's method for Cr/$n$-Si Schottky structure.

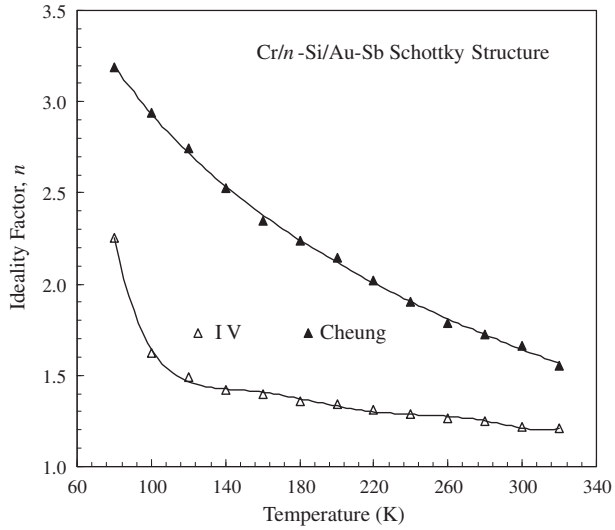


**Fig. 7.** Temperature dependence of the ideality factors for Cr/*n*-Si Schottky structure.

Fig. 6 shows the variation of the barrier heights obtained from the different methods of Cr/*n*-Si/Au–Sb Schottky structure in the temperature range of 80–320 K. As can be seen from Fig. 6 and Table 1, the values of the barrier height obtained from three different methods have increased with increasing temperature. The values of barrier height obtained from the Norde method are higher than obtained from the Cheung's method. Fig. 7 shows the variation of the ideality factors obtained from the *I–V* and Cheung's method in the temperature range of 80–320 K. In Table 1 and Fig. 7, the values of *n* obtained from the *I–V* characteristics are lower than obtained from the Cheung's method. In general, it is found that, these parameters far from the ideal diode parameters at high voltage region because there is a voltage drop in this region and this cause a non-ideal behaviour. Due to the decrease in the series resistance with increasing temperature, the *n* values have been decreased with increasing temperature. Fig. 8 shows the variation of the series resistance of the Cr/*n*-Si/Au–Sb Schottky structure obtained from the Cheung and Norde methods as a function of temperature. It can be said that, especially, the values of series resistance obtained from the Cheung's method are approximately

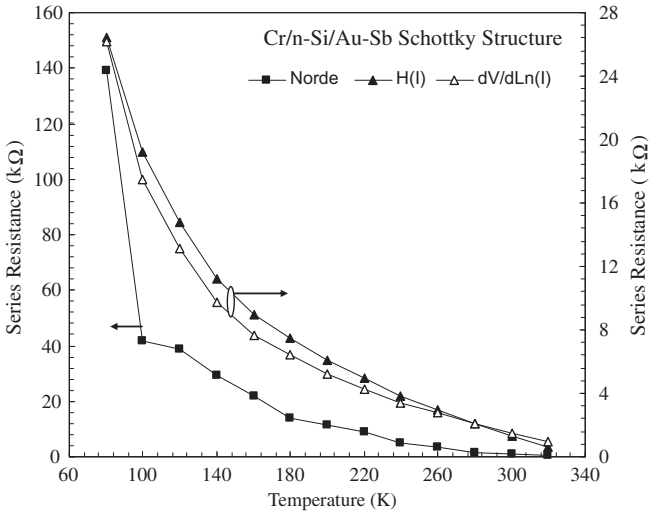


**Fig. 8.** Temperature dependence of the series resistances of Cr/*n*-Si Schottky structure.

in agreement with each other. However, according to Table 1, the values of $R_S$ obtained from the Norde's method are higher than obtained from the Cheung's method. In the conclusion, the parameters obtained from the Cheung functions and the Norde's functions are not agreeing with each other, especially at low temperatures. As mentioned above, the Cheung functions are only applied to the non-linear region (high voltage region) of the forward bias *I–V* characteristics, while Norde's functions are applied to the full forward bias *I–V* characteristics of the junctions. The increase in the BH at higher temperatures also may be due to the interface states and chemical reactions between the metal and the semiconductor at the interface [43,44].

## 4. Conclusion

In this study, the temperature dependences of the electrical characteristics of Cr/*n*-Si/Au–Sb Schottky structures prepared by electrodeposition method have been investigated using current–voltage (*I–V*) characteristics in a wide temperature range. The basic diode parameters such as ideality factor and barrier height were extracted from electrical measurements. The estimated barrier height $\Phi_{bo}$ and the ideality factor *n* assuming thermionic emission mechanism show strong temperature dependence. Furthermore, the values of the barrier height and the ideality factor and series resistance of Cr/*n*-Si/Au–Sb Schottky structure as a function temperature have been determined from the ln *I–V* plots, the Cheung plots and the Norde plots, respectively. The values of series resistance obtained from the Cheung's method are approximately in agreement with each other. However, there is a good agreement between the values of the series resistance obtained from Cheung and Norde methods for high temperatures. It is seen that the electrical characteristics of this structure are remarkably changed with temperature.

## References

[1] H.C. Card, E.H. Rhoderick, J. Phys. D 3 (1971) 1589.
[2] S.M. Sze, Physics of Semiconductor Devices, second ed., Wiley, New York, 1981.
[3] E.H. Rhoderick, R.H. Williams, Metal–Semiconductor Contacts, second ed., Clarendon, Oxford, 1988.
[4] B. Sahin, H. Cetin, E. Ayyildiz, Solid State Commun. 135 (2005) 490–495.
[5] R.F. Schmitsdorf, W. Mönch, Eur. Phys. J. B 7 (1999) 457.
[6] Ş. Karataş, A. Türüt, Phys. B 381 (2006) 199.
[7] S. Pandey, S. Kal, Solid-State Electron. 42 (1998) 943.
[8] Ş. Karataş, Ş. Altındal, Mater. Sci. Eng. B 122 (2005) 133.
[9] G. Gomila, J.M. Rubi, J. Appl. Phys. 81 (1997) 2674.
[10] Ş. Karataş, Ş. Altındal, M. Çakar, Phys. B 357 (2005) 386.
[11] M.L. Munford, M.L. Sartorelli, L. Seligman, A.A. Pasa, J. Electrochem. Soc. 149 (2002) C274.
[12] T. Kılıçoglu, Thin Solid Films 516 (2008) 967.
[13] J.G. Oskam, G. Long, A. Natarajan, P.C. Searson, J. Phys. D: Appl. Phys. 31 (1998) 1927.
[14] Chunxin Ji, G. Oskam, P.C. Searson, J. Electrochem. Soc. 148 (2001) C746.
[15] G. Oskam, P.C. Searson, Surf. Sci. 446 (2000) 103.
[16] K. Marquez, G. Staikov, J.W. Schultze, Electrochim. Acta 48 (2003) 875.
[17] J.C. Ziegler, R.I. Wielgosz, D.M. Kolb, Electrochim. Acta 45 (1999) 827.
[18] M.E. Aydin, F. Yakuphanoglu, T. Kılıçoğlu, Synth. Met. 157 (2007) 1080.
[19] C.A. Moina, M. Vazdar, Electrochem. Commun. 3 (2001) 159.
[20] G. Güler, Ş. Karataş, Ö. Güllü, Ö.F. Bakkaloğlu, J. Alloys Comp. 486 (2009) 343.
[21] G. Güler, Ö. Güllü, Ş. Karataş, Ö.F. Bakkaloğlu, Chin. Phys. Lett. 26 (6) (2009) 067301.
[22] Ö. Güllü, T. Kilicoglu, A. Türüt, J. Phys. Chem. Solids 71 (2010) 351.
[23] G. Güler, Ö. Güllü, Ö.F. Bakkaloglu, A. Türüt, Phys. B: Conden. Matter 403 (2008) 2211.
[24] P.N. Bartlett, M.A. Ghanem, I.S.E. Hallag, P. de Groot, A. Zhukov, J. Mater. Chem. 13 (2003) 2596.
[25] Michail E. Kiziroglou, Alexander A. Zhukov, Mamdouh Abdelsalam, Xiaoli Li1, Peter A.J. de Groot, Philip N. Bartlett, Cornelis H. de Groot, IEEE Trans. Magnet. 41 (2005) 10.
[26] Z.L. Bao, K.L. Kavanagha, J. Vac. Sci. Technol. B 24 (2006) 2138.
[27] S. Forment, R.L. Van Meirhaeghe, A. De Vrieze, K. Strubbe, W.P. Gomes, Semicond. Sci. Technol. 16 (2001) 975.
[28] M.E. Kiziroglou, A.A. Zhukov, M. Abdelsalam, X. Li, P.A.J. de Groot, P.N. Bartlett, C.H. de Groot, IEEE Trans. Magn. 41 (2005) 2639.
[29] J.P. Sullivan, R.T. Tung, M.R. Pinto, W.R. Graham, J. Appl. Phys. 70 (1991) 7403.

[30] M. Pattabi, S. Krishnan, Ganesh, X. Mathew, Sol. Energy 81 (2007) 111.
[31] I. Dokme, S. Altindal, M.M. Bulbul, Appl. Surf. Sci. 252 (2006) 7749.
[32] F. Yakuphanoglu, Phys. B 389 (2007) 306.
[33] S. Kumar, Y.S. Katharria, D. Kanjilal, J. Appl. Phys. 100 (2006) 113723.
[34] J. Osvald, Z.J. Horvath, Appl. Surf. Sci. 234 (2004) 349.
[35] P. Chattopadhyay, B. RayChaudhuri, Solid-State Electron. 36 (1993) 605.
[36] M. Sağlam, A. Ateş, B. Güzeldir, A. Astam, M.A. Yıldırım, J. Alloys Comp. 484 (2009) 570.
[37] V. Janardhanam, A. Ashok Kumar, V. Rajagopal Reddy, P. Narasimha Reddy, J. Alloys Comp. 485 (2009) 467.
[38] A. Gumuş, A. Türüt, N. Yalçın, J. Appl. Phys. 91 (2002) 245.
[39] S. Aydoğan, M. Sağlam, A. Türüt, Appl. Surf. Sci. 250 (2005) 43.
[40] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. 49 (1986) 85.
[41] H. Norde, J. Appl. Phys. 50 (1979) 5052.
[42] A. Keffous, M. Siad, S. Mamma, Y. Belkacem, C. Lakhdar Chaouch, H. Menari, A. Dahmani, W. Chergui, Appl. Surf. Sci. 218 (2003) 337.
[43] V.R. Reddy, P.K. Rao, C.K. Ramesh, Mater. Sci. Eng. B 137 (2007) 200.
[44] C.K. Ramesh, V.R. Reddy, C.J. Choi, Mater. Sci. Eng. B 112 (2004) 30.