Materials Science and Engineering B 159–160 (2009) 269–273

Contents lists available at ScienceDirect

Materials Science and Engineering B

journal homepage: www.elsevier.com/locate/mseb

Effect of internal gettering of iron on electrical characteristics of devices

H. Talvitie*, A. Haarahiltunen, H. Savin, M. Yli-Koski, M.I. Asghar, J. Sinkkonen

Helsinki University of Technology, Department of Micro and Nanosciences, P. O. Box 3500, FI-02015 TKK, Finland

ARTICLE INFO

Article history:
Received 1 May 2008
Accepted 30 October 2008

Keywords:
Semiconductor devices
Silicon
Iron
Gettering

ABSTRACT

Different types of gettering treatments were applied to a real device process to evaluate their ability to remove iron contamination from the device layer and improve the electrical characteristics of the devices. NMOS and PMOS transistors and other test structures were manufactured on boron doped, both iron contaminated and uncontaminated Cz silicon wafers with or without gettering treatment. Gettering treatments, which were designed to induce sufficient iron precipitate nucleation in the bulk to ensure iron precipitation, were inserted in the fabrication process after the last high temperature treatment in which the iron solubility was higher than the contamination level. The electrical characteristics of the devices, such as leakage currents, were measured. The applied gettering treatments were found to be inefficient to improve the device performance, possibly due to stronger gettering to heavily doped, ion implantation damaged device layer.

1. Introduction

Continuously decreasing dimensions and increasing complexity of integrated circuits set strict limits to the acceptable defect density in the device area of the silicon wafer. Iron is very detrimental contaminant in silicon and unavoidable in semiconductor processing environment. Therefore there is a need for effective gettering treatment, which would reduce the iron concentration in the device layer. Earlier gettering studies have usually been carried out on entire wafers, though effects of various internal gettering and segregation gettering treatments on pn-junction leakage currents have been investigated [1–5]. Typically the device layer contains both highly phosphorus doped and boron doped regions with ion implantation induced damage. Due to the damaged, highly doped device regions competitive gettering between relaxation gettering and segregation gettering to highly doped regions must be taken into account in the design of the gettering treatments [6,7]. In our previous studies on competitive gettering we have found that certain gettering treatments can reduce the iron concentration in boron doped device layer [8,9]. In this study the effects of those treatments on device characteristics are evaluated.

Iron nucleation at gettering sites is needed to produce effective internal gettering of iron [10]. However, high temperature steps of device fabrication process can cause iron to dissolve and precipitate many times. The gettering treatment which includes iron nucleation step is inserted in the process after the last high temperature step which causes total iron dissolution, i.e. iron solubility at that temperature is higher than the contamination level. It is assumed here that the device performance is determined by the final concentrations of iron precipitates and dissolved iron in the device layer. In this paper, we try to evaluate this assumption experimentally using simple BiCMOS process.

2. Experimental

Simple NMOS and PMOS transistors and various capacitor and diode structures were fabricated to evaluate the effect of the gettering treatments on device performance. Substrate wafers were p-type boron doped (100) Cz silicon wafers of about 17–24 Ωcm resistivity and 100 mm diameter. Interstitial oxygen concentration was measured with FTIR spectroscopy to be 11.1–12.5 ppma (ASTM F 121-83 standard). Prior to the device fabrication process, some of the wafers were contaminated with iron by immersing wafers in iron spiked NH_4OH:H_2O_2:H_2O solution and subsequently diffusing iron at 850 °C for 55 min and finally removing the surface contamination. Contamination level after intentional iron contamination was $1–2 \times 10^{13}$ cm^{-3} measured with μPCD method. Background contamination caused by the processing in uncontaminated wafers was determined to be about 7×10^{11} cm^{-3}.

Appropriate thermal anneals were included in the thermal oxidation steps to induce oxygen outdiffusion from the wafer surface and oxide precipitate growth in the bulk of the wafer. An additional step to induce higher nucleation of oxide precipitates was also included in the process sequence of the wafers, which received the gettering treatments. The purpose was to maximize the effect of the gettering treatment with respect to the wafers without gettering.

* Corresponding author. Tel.: +358 9 451 4987; fax: +358 9 451 5008.
E-mail address: heli.talvitie@tkk.fi (H. Talvitie).

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doi:10.1016/j.mseb.2008.10.048

Table 1
The device fabrication process.

1.	Ion implantation mask oxide growth for 50 mm at 1050 °C to 435 nm thickness and high temperature annealing for oxygen outdiffusion for 310 min at 1100 °C
2.	N-well area patterning
3.	Low temperature annealing for oxide precipitate nucleation for 360 min at 550 °C for wafers which will later receive gettering treatment and ion implantation screen oxide growth for 27 min at 1000 °C to 30 nm thickness
4.	Phosphorus implantation $l \times 10^{13}$ cm^{-2} at 150 keV energy for n-well doping
5.	Screen oxide removal
6.	Oxidation for ISO min at 1000 °C and high temperature annealing for phosphorus drive-in and oxide precipitate growth for 1080 min at 1100 °C
7.	Oxide removal
8.	Boron implantation 2×10^{12} cm^{-2} at 30 keV energy for NMOS threshold voltage adjustment
9.	Field oxide growth for 70 min at 1000 °C to 30 nm thickness
10.	MOS active area patterning
11.	Ion implantation screen oxide growth for 27 min at 1000 °C to 30 nm thickness
12.	Phosphorus implantation $l \times l0^{15}$ cm^{-2} at 70 keV energy for NMOS source and drain doping
13.	Boron implantation $l \times 10^{15}$ cm^{-2} at 30 keV energy for PMOS source and drain doping
14.	Doping activation annealing for 30 min at 950 °C
15.	Screen oxide removal
16.	Gate oxide growth for 55 min at 950 °C to 30 nm thickness
17.	Gettering treatment
18.	Contact hole patterning
19.	Aluminum sputtering to 300 nm thickness and MOS gate and contact patterning
20.	Aluminum sintering for 15 min at 450 °C

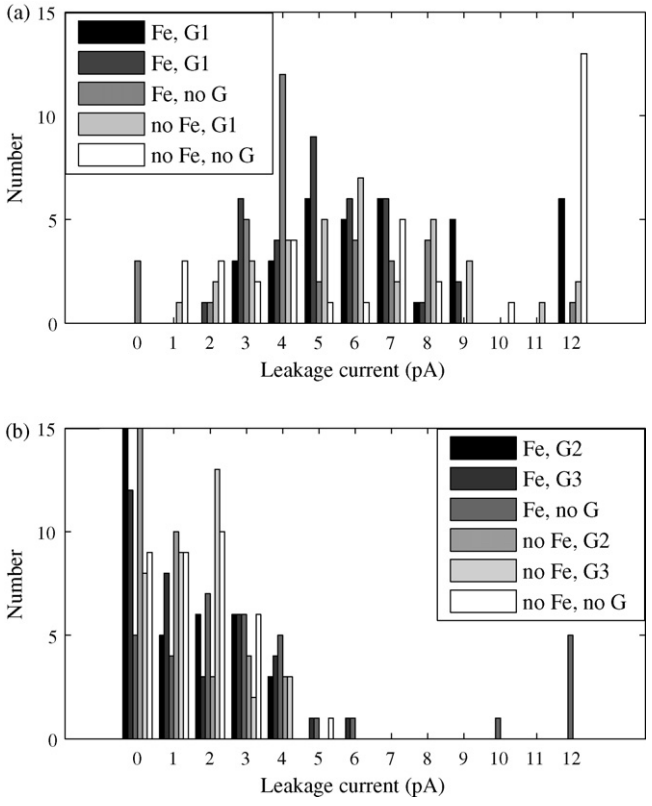

Fig. 1. p$^+$n-junction leakage current distribution for wafers to which (a) gettering treatment G1: 270 °C for 1 h + RT + 700 °C for 1 h and (b) gettering treatment G2: 450 °C for 1 h or G3: 450 °C for 1 h + 700 °C for 1 h has been applied. Results for wafers without gettering treatment are also shown.

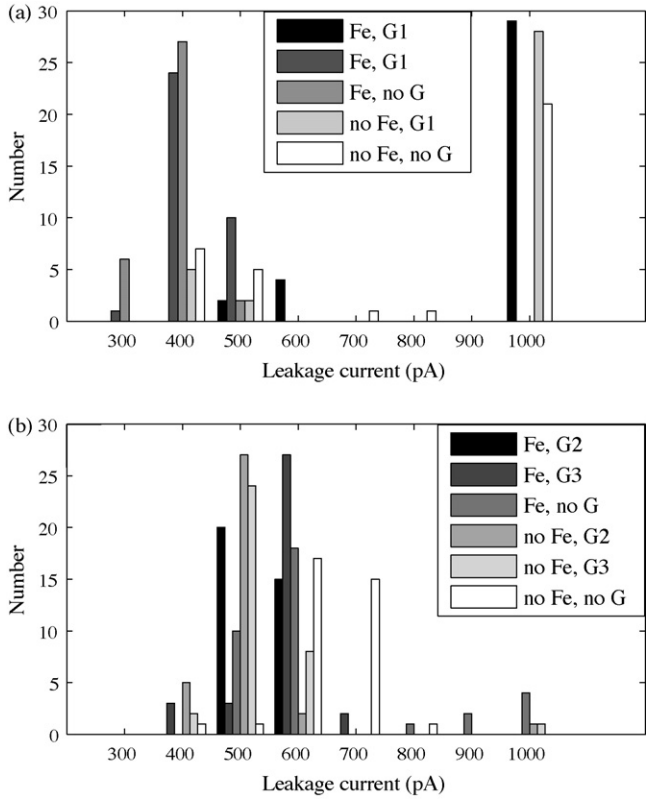

Fig. 2. n$^+$p-junction leakage current distribution for wafers to which (a) gettering treatment G1: 270 °C for 1 h + RT + 700 °C for 1 h and (b) gettering treatment G2: 450 °C for 1 h or G3: 450 °C for 1 h + 700 °C for 1 h has been applied. Results for wafers without gettering treatment are also shown.

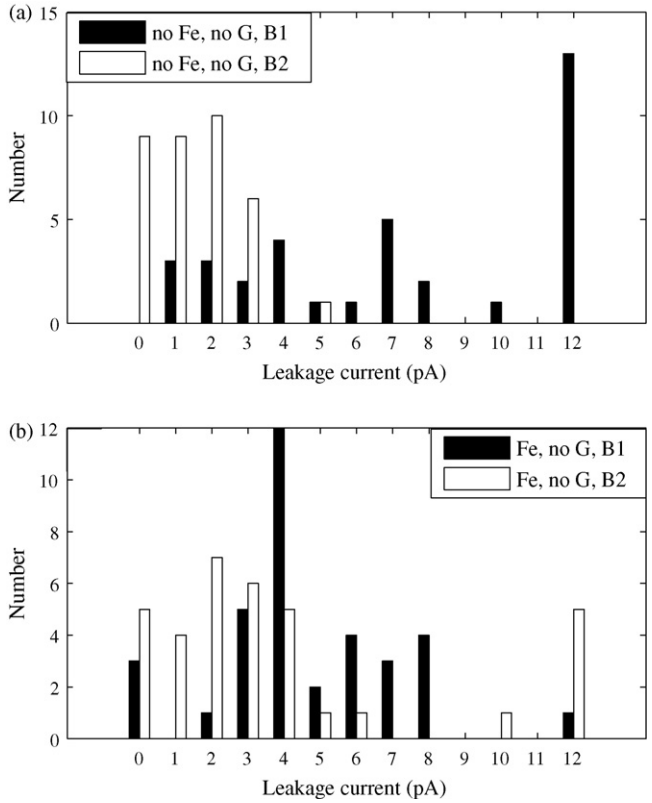

Fig. 3. p$^+$n-junction leakage current comparison between (a) uncontaminated and (b) iron contaminated wafers without gettering treatment from different processing batches B1 and B2.

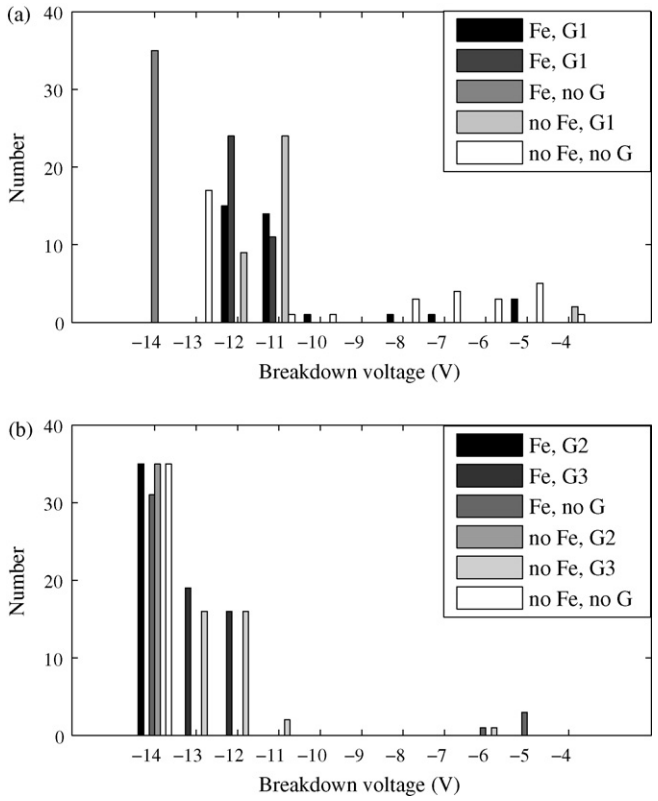

Fig. 4. Breakdown voltage distribution of PMOS transistors of 10 μm long and 50 μm wide channel for wafers to which (a) gettering treatment G1: 270 °C for 1 h + RT + 700 °C for 1 h and (b) gettering treatment G2: 450 °C for 1 h or G3: 450 °C for 1 h + 700 °C for 1 h has been applied. Results for wafers without gettering treatment are also shown.

N-well was formed with phosphorus implantation of 1×10^{13} cm^{-2} at 150 keV energy, NMOS threshold voltage was adjusted with boron implantation of 2×10^{12} cm^{-2} at 30 keV energy, NMOS source and drain were formed with phosphorus implantation of 1×10^{15} cm^{-2} at 70 keV energy and PMOS source and drain with boron implantation of 1×10^{15} cm^{-2} at 30 keV energy. The fabrication process is described in more detail in Table 1.

The gettering treatment was placed in the process after the last high temperature treatment in which the iron solubility was higher than the contamination level. The applied gettering treatments were room temperature (RT) + 270 °C for 1 h + RT + 700 °C for 1 h + RT denoted as G1, RT + 450 °C for 1 h + RT denoted as G2, RT + 450 °C for 1 h + ramp up to 700 °C at a rate of 10 °C/min + 700 °C for 1 h + RT denoted as G3. Each gettering treatment was applied to intentionally iron contaminated and uncontaminated wafer. In addition, iron contaminated and uncontaminated wafers were processed without any gettering treatment for references.

NMOS and PMOS transistors of four different dimensions were fabricated; transistors of 50 μm channel width and 6, 10 or 20 μm channel length and 82 μm channel width and 10 μm channel length. Additionally different capacitor and diode structures of 300 μm × 400 μm area were produced. The number of each device on a wafer was 35. Threshold voltage, transconductance, drain current and breakdown voltage of each MOS transistor were measured. Drain current was measured at $V_{ds} = V_{gs} = 3.3$ V and breakdown voltage nondestructively at 1 μA current. Leakage currents were measured at 2.5 V on p$^+$n-junctions fabricated on n-well and n$^+$p-junctions fabricated on p-type substrate.

3. Results

Fig. 1 presents p$^+$n-junction leakage current distribution, i.e. the number of components at each leakage current value for wafers on which gettering treatments G1, G2 and G3 were performed and for simultaneously processed wafers without any gettering treatment. There is not significant difference between the three iron contaminated wafers; two wafers which received gettering treatment G1 and one without gettering treatment (Fig. 1(a)). What comes to uncontaminated wafers, for the wafer without gettering higher leakage currents were measured compared to the wafer with gettering treatment G1. Gettering treatments G2 and G3 did not induce clear difference to p$^+$n-junction leakage current with respect to wafers without gettering (Fig. 1(b)). Fig. 2 shows n$^+$p-junction leakage current distribution for wafers to which gettering treatment G1 (Fig. 2(a)) and gettering treatments G2 or G3 (Fig. 2(b)) were applied. Surprisingly, the wafers without iron contamination showed higher leakage currents compared to contaminated wafers. It is possible that the background contamination level between processing batches varies as Fig. 3 implies. p$^+$n-junction leakage current comparison has been made between wafers without iron contamination and gettering treatment from processing batches B1, which included gettering treatment G1 wafers and B2, which included gettering treatment G2 and G3 wafers (Fig. 3(a)). There is an indication of higher background contamination in batch B1. Iron contaminated wafers without gettering treatment from batches B1 and B2 are also compared (Fig. 3(b)).

Fig. 4 shows PMOS breakdown voltage distribution for 10 μm long and 50 μm wide channel transistors and Fig. 5 shows NMOS breakdown voltage distribution for transistors of the same size

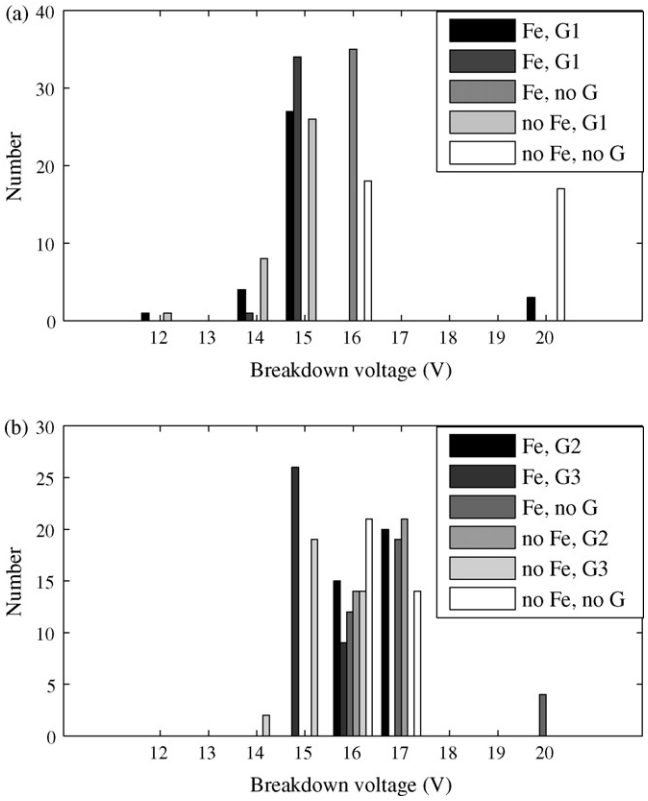

Fig. 5. Breakdown voltage distribution of NMOS transistors of 10 μm long and 50 μm wide channel for wafers to which (a) gettering treatment G1: 270 °C for 1 h + RT + 700 °C for 1 h and (b) gettering treatment G2: 450 °C for 1 h or G3: 450 °C for 1 h + 700 °C for 1 h has been applied. Results for wafers without gettering treatment are also shown.

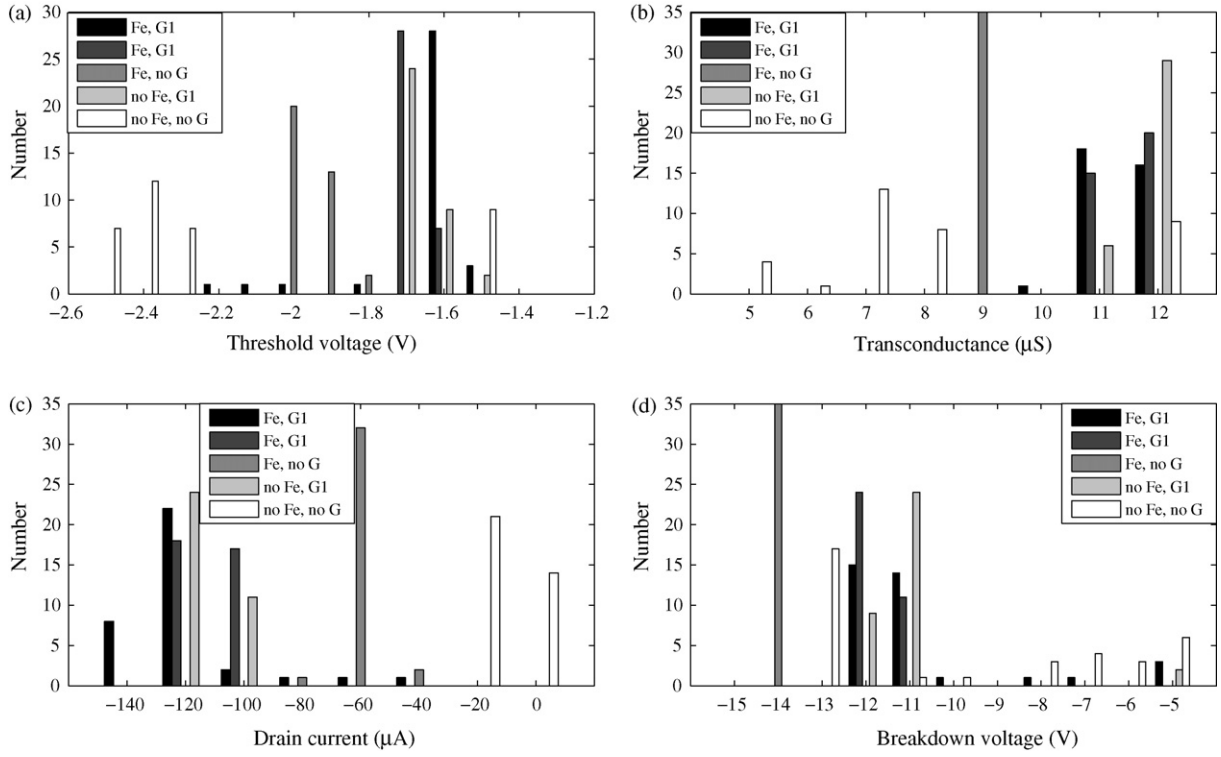

Fig. 6. (a) Threshold voltage, (b) transconductance, (c) drain current and (d) breakdown voltage distributions of PMOS transistors of 10 μm long and 50 μm wide channel for wafers with and without gettering treatment G1: 270 °C for 1 h + RT + 700 °C for 1 h.

when gettering treatments G1, G2 or G3 have been applied. Fig. 6 represents the distributions of the measured MOS characteristics among PMOS transistors of 10 μm long and 50 μm wide channel after gettering treatment G1. There is a difference between electrical characteristics of devices on wafers with and without gettering treatment. However, the difference could be attributed to a difference in gate oxide thickness between those wafers.

4. Discussion

The reason for the inefficiency of the gettering treatments to improve the device characteristics could be the segregation of iron to the heavily doped device layer and strong precipitation to the ion implantation induced defects, which competes with the gettering to the bulk gettering sites. Gettering by highly doped regions might just be enough (to clean areas close to the device) in processes in which the volume of the highly doped regions is rather high, which is in agreement with Polignano et al. [2]. Besides, multiple iron dissolution-precipitation cycles during the device fabrication process may produce lattice defects in the device layer. They can later serve as gettering sites and degrade the ability of the gettering treatments to remove iron from the device layer. Moreover, the amount of samples was quite low after all and we cannot exclude the possibility of variation in the unintentional contamination.

5. Conclusions

Gettering treatments of various types were applied to a device process to evaluate their ability to remove iron from the device layer and to affect the device performance. Gettering treatments were designed to induce sufficient iron precipitate nucleation at the bulk gettering sites so that internal gettering of iron would be effective. MOS transistor characteristics and p^+n- and n^+p-junction leakage currents were measured on both iron contaminated and uncontaminated wafers with or without gettering to see the effect of the gettering treatments. Significant difference in electrical characteristics of devices on wafers with gettering treatments compared to wafers without gettering could not be seen. The reason for this can be that gettering to highly doped areas on device layer which involve also ion implantation induced damage is stronger than internal gettering to the bulk. Multiple iron dissolution-precipitation cycles during processing possibly producing defects in the device layer can also degrade the gettering efficiency of the gettering treatments. However, in future it would be interesting to study the leakage currents in larger p^+n- and n^+p-junctions to see the possible contribution of the junction area.

Acknowledgements

The authors acknowledge the financial support from the Finnish National Technology Agency, Academy of Finland, Okmetic Oyj, Endeas Oy, Semilab Inc., VTI Technologies Oy and Micro Analog Systems Oy. The authors are grateful to Micro Analog Systems Oy for performing the device measurements.

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