



# Mechanisms and modification of nonlinear shunt leakage in $\text{Sb}_2\text{Se}_3$ thin film solar cells



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## ABSTRACT

Antimony selenide ( $\text{Sb}_2\text{Se}_3$ ) based thin film solar cells have recently drawn a growing research interest due to their increasing power conversion efficiency, proper bandgap, high absorption coefficient, and earth abundant nature. Herein, the  $\text{Sb}_2\text{Se}_3$  thin films were prepared by close spaced sublimation (CSS) for efficient  $\text{Sb}_2\text{Se}_3$  solar cells. The origin and the mechanisms of shunt current were analyzed. Non-ohmic space-charge limited current (SCLC) was identified to be an important contribution to the nonlinear shunt current in  $\text{Sb}_2\text{Se}_3$  thin film solar cells. To tackle this issue, a high-resistance  $\text{SnO}_2$  buffer was introduced at the front contact. With the insertion of a  $\text{SnO}_2$  buffer, the micro-shunt paths were modified and a significant efficiency improvement to 5.18% was obtained.

## 1. Introduction

Antimony selenide ( $\text{Sb}_2\text{Se}_3$ ) is a promising photovoltaic material with a variety of attractive features, such as proper band gap (1–1.2 eV), high absorption coefficient, intrinsically benign grain boundaries, low toxicity, earth-abundant elements and high theoretical conversion efficiency up to 31% [1,2].  $\text{Sb}_2\text{Se}_3$  based thin-film solar cells have demonstrated increased power conversion efficiency ( $\sim 6.5\%$ ) in recent years [2–4]. However, due to the relatively short history and rather small scientific community devoted to the  $\text{Sb}_2\text{Se}_3$  solar cell research, many fundamental problems, both material and device, are remained to be investigated. From the point of view of material,  $\text{Sb}_2\text{Se}_3$  has a one-dimensional (1D) crystal structure. The film growth and microstructure are very sensitive to preparation process and experimental conditions. To improve the solar cell performance further, the most challenging work is to obtain high quality  $\text{Sb}_2\text{Se}_3$  film [4]. So far, various approaches including vacuum evaporation, sputtering, spin-coating, electrodeposition, spray pyrolysis, and chemical bath deposition have been explored to fabricate the  $\text{Sb}_2\text{Se}_3$  thin films [4–10]. Tang et al. had developed a fast  $\text{Sb}_2\text{Se}_3$  film deposition based on rapid thermal evaporation (RTE) technique, which demonstrated a simple and successful method to get high quality p- $\text{Sb}_2\text{Se}_3$  layer that can be finished in tens of seconds [2,4]. From the point of view of device, the  $\text{CdS}/\text{Sb}_2\text{Se}_3$  thin film solar cell is typically made in the superstrate configuration with Glass/TCO/ $\text{CdS}/\text{Sb}_2\text{Se}_3$ /Metal structure [3,4].

Thickness of the  $\text{Sb}_2\text{Se}_3$  layer influences the performance of the devices. Taking into account the factors such as the optical absorption coefficients, the junction depletion width and the minority carrier (electron) diffusion length, the optimal thickness of the  $\text{Sb}_2\text{Se}_3$  absorber layer was found to be about 500 nm [11]. This is a rather small thickness and is one reason for the limited efficiency of the devices reported. In  $\text{Sb}_2\text{Se}_3$  solar cells, the  $\text{CdS}$  layer works as a n-type window layer, which absorbs photons with energy greater than its bandgap of 2.42 eV [12]. In order to reduce the light absorption in the  $\text{CdS}$  window layer, the thickness of  $\text{CdS}$  layer should be decreased to as thin as several ten nanometers. However, when the  $\text{CdS}$  layer is too thin, the pinholes or discontinuity would inevitably happen so that  $\text{Sb}_2\text{Se}_3$  directly contacts the front electrode, leading to electric micro-shunt paths and low quality p-n junction diode [12,13]. In addition, due to the fabrication procedure of superstrate structure, the interdiffusion/reaction occurred at the  $\text{CdS}/\text{Sb}_2\text{Se}_3$  interface during the subsequent deposition of  $\text{Sb}_2\text{Se}_3$  would lead to part of the  $\text{CdS}$  consumed up [14]. Actually, the discontinuity in  $\text{CdS}$  or the interdiffusion at junction interface induced shunt leakages have been reported in both superstrate  $\text{CdTe}$  thin film solar cells and substrate  $\text{CuIn}_{1-x}\text{Ga}_x\text{Se}_2$  thin film solar cells [15,16]. Shunt leakage is a key issue affecting solar cell performance especially for large area thin film solar cells. Shunt currents are detrimental to the cell/module output parameters, especially fill factor (FF) and open-circuit voltage ( $V_{oc}$ ) [13]. Understanding the origin of shunt current and minimizing shunt current loss are essential to enhance solar cell efficiency further.

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Herein, we employ close spaced sublimation (CSS) deposition to grow  $\text{Sb}_2\text{Se}_3$  thin films. CSS is a rapid and industrially scalable deposition technique which was widely used in many kinds of inorganic film deposition for photovoltaic application, like binary compound CdTe [17]. This work demonstrated that CSS is highly suitable for fabrication of  $\text{Sb}_2\text{Se}_3$  thin film solar cells. Focusing on the relatively large and nonlinear shunt current discovered in this study, we tried to make clear the physical origin of shunt leakage in  $\text{Sb}_2\text{Se}_3$  solar cells and to find solutions to improve the device performance. On the basis of the experiments and theoretical models, the device characteristics were analyzed and the non-ohmic space-charge limited current (SCLC) was identified to be responsible for the nonlinear shunt current in  $\text{Sb}_2\text{Se}_3$  solar cells. The shunt paths were found mainly caused by the local discontinuity or pinholes in the CdS window layer. With the insertion of a high-resistance tin oxide layer as front contact buffer, the micro-shunt paths were effectively modified. The presence of  $\text{SnO}_2$  buffer significantly reduced the shunt current and improved the junction quality, resulting in the cell efficiency increasing from 3.73% to 5.18%.

## 2. Experimental

The  $\text{Sb}_2\text{Se}_3$  solar cells fabricated in this study had superstrate structures of glass/FTO/CdS/ $\text{Sb}_2\text{Se}_3$ /Au or glass/FTO/ $\text{SnO}_2$ /CdS/ $\text{Sb}_2\text{Se}_3$ /Au. CdS window layers with a thickness of  $\sim 60$  nm were prepared on glass/FTO or glass/FTO/ $\text{SnO}_2$  substrates by chemical bath deposition (CBD) technique from a solution composed of de-ionized water, cadmium acetate, ammonium acetate, and thiourea. The  $\text{Sb}_2\text{Se}_3$  absorber layers, which had a thickness of  $\sim 550$  nm, were deposited by the CSS technique in a home-made film-deposition system, as sketched in Fig. 1(a). The source material is commercial  $\text{Sb}_2\text{Se}_3$  powder with

99.999% purity. The source temperature was  $520^\circ\text{C}$  and the substrate temperature was  $320^\circ\text{C}$ . The detailed CdS and  $\text{Sb}_2\text{Se}_3$  fabrication processes can be found in our previous work [10,15]. The highly resistive  $\text{SnO}_2$  buffer layer between FTO and CdS was deposited by the RF magnetron sputtering technique at a substrate temperature of  $200^\circ\text{C}$ . A 99.99%  $\text{SnO}_2$  target (diameter 3 in.) was sputtered in a reactive gas mixture of  $\text{O}_2$  and Ar with an  $\text{O}_2/\text{Ar}$  pressure ratio of 1/20. The working pressure was 0.5 Pa and the RF power was 60 W. The  $\text{SnO}_2$  layer thickness was controlled by varying the sputtering time. The Au back contact was prepared by thermal evaporation in a vacuum chamber. The size of individual  $\text{Sb}_2\text{Se}_3$  solar cell was  $4 \times 4 \text{ mm}^2$  defined by Au contacts.

The film morphologies were characterized by using a field emission scanning electron microscope (SEM, FEI Apreo LoVac) and conductive atomic force microscopy (C-AFM, Veeco Multimode V). X-Ray Diffraction (XRD) measurements were performed by an X-ray diffractometer (Bruker D8 Advance). The solar cell current density–voltage (J–V) curves of  $\text{Sb}_2\text{Se}_3$  solar cells were recorded using a Keithley 2400 source measurement unit and a Newport solar simulator (Oriel-SOI3A) with an AM1.5 G spectrum. The light intensity was adjusted to  $100 \text{ mW/cm}^2$  using a standard Si solar cell (91150 V). The external quantum efficiency (EQE) spectra were measured with a spectral response system (Enlitech QE-R).

## 3. Results and discussion

### 3.1. Properties of $\text{Sb}_2\text{Se}_3$ thin film and solar cell performances

The quality of the  $\text{Sb}_2\text{Se}_3$  absorber layer is crucial to the performance of  $\text{Sb}_2\text{Se}_3$  solar cells. Fig. 1(b) shows the surface morphology of a

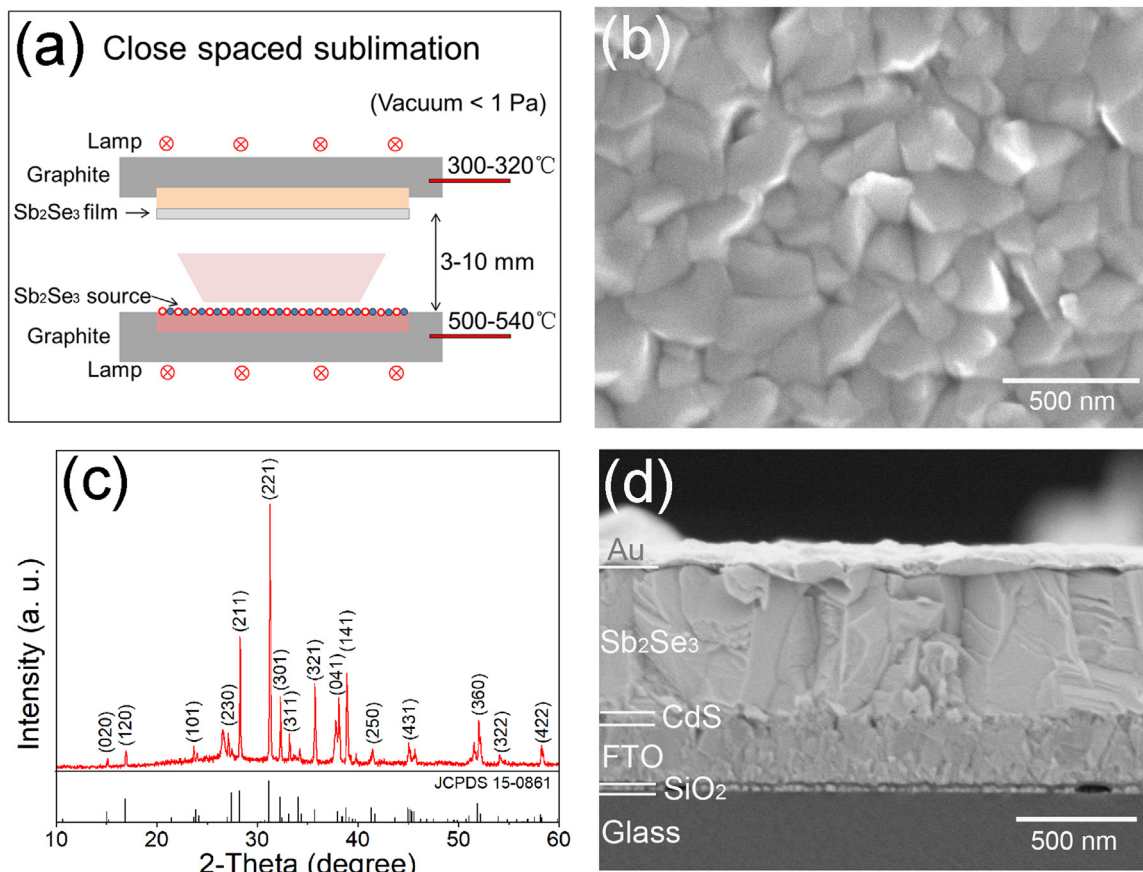
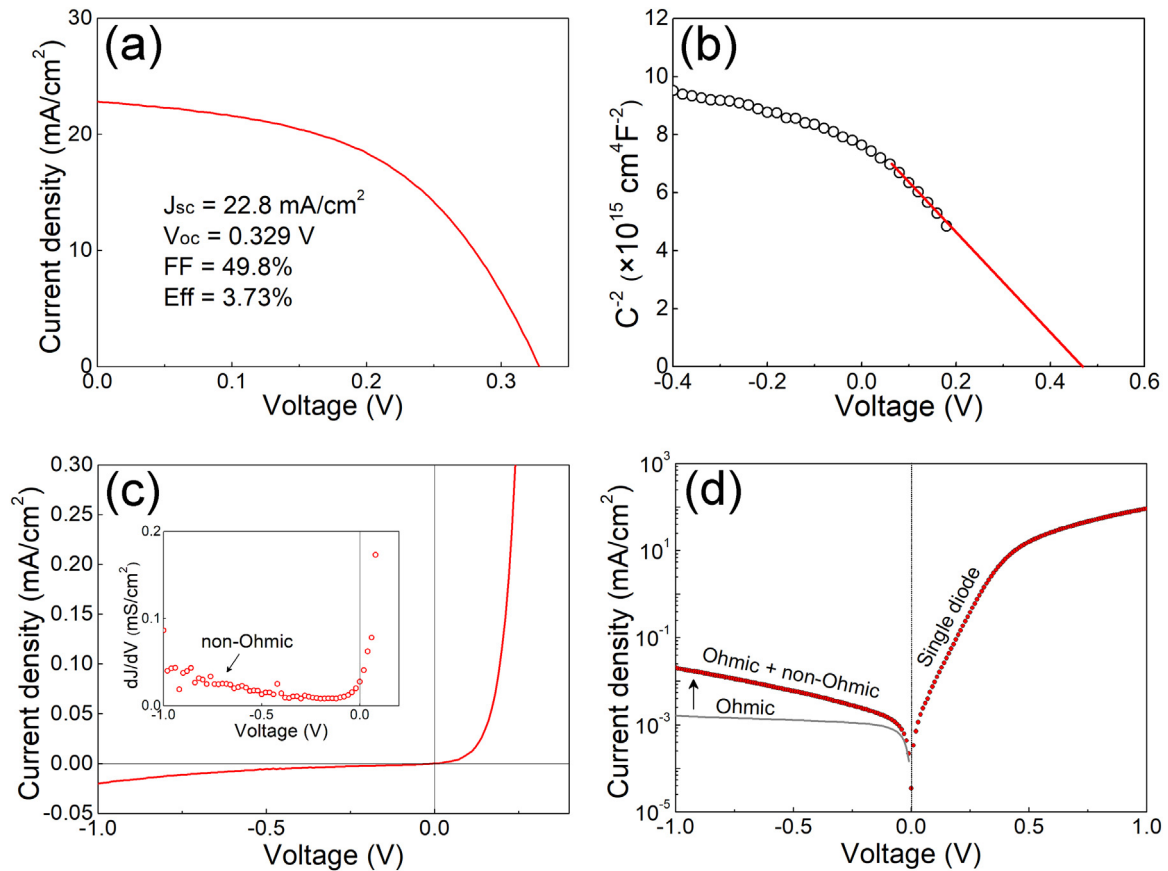


Fig. 1. (a) The schematic diagram of CSS equipment for  $\text{Sb}_2\text{Se}_3$  film deposition; (b) SEM surface morphology and (c) XRD pattern of  $\text{Sb}_2\text{Se}_3$  film with a thickness of  $\sim 550$  nm; (d) cross-sectional SEM image of a  $\text{Sb}_2\text{Se}_3$  thin film solar cell with a structure of glass/FTO/CdS/ $\text{Sb}_2\text{Se}_3$ /Au.



**Fig. 2.** (a) Light  $J$ - $V$  and (b)  $C^{-2}$ - $V$  and (c) dark  $J$ - $V$  and (d) dark  $J$ - $V$  (shown on semi-log plots) curves of the  $\text{Sb}_2\text{Se}_3$  solar cells. The (c) inset shows shunt characterization by  $dJ/dV$ - $V$  curve.

$\text{Sb}_2\text{Se}_3$  film prepared by CSS with a thickness of  $\sim 550$  nm. It can be seen that the  $\text{Sb}_2\text{Se}_3$  film had an excellent crystallinity. The grains were densely packed and had an in-plane size of  $200 \sim 400$  nm. As a one-dimensional material, orientational control of the  $\text{Sb}_2\text{Se}_3$  film is believed to be the key factor to realize an efficient carrier transport and benign grain boundaries. To have a better understanding of the crystal orientation and the crystallinity of the obtained  $\text{Sb}_2\text{Se}_3$  film, the XRD curves are shown in Fig. 1(c). The diffraction patterns showed that all the peaks were the characteristic peaks of  $\text{Sb}_2\text{Se}_3$ . The film growth showed preferential orientations. Two strong diffraction peaks at  $28.2^\circ$  and  $31.2^\circ$  were attributed to the (211) and (221) lattice planes, respectively. The cross-sectional microstructure of a  $\text{Sb}_2\text{Se}_3$  solar cell is shown in Fig. 1(d). It can be seen that the  $\text{Sb}_2\text{Se}_3$  film had through-thickness grains, which facilitated the transport and collection of photo-generated carriers.

$\text{Sb}_2\text{Se}_3$  solar cells with the structure of glass/FTO/CdS/ $\text{Sb}_2\text{Se}_3$ /Au were fabricated. As can be seen in Fig. 2(a), typical device performance revealed a short-circuit current density ( $J_{\text{SC}}$ ) of  $22.8 \text{ mA/cm}^2$ , open voltage ( $V_{\text{OC}}$ ) of  $329 \text{ mV}$  and fill factor (FF) of  $49.8\%$ . The series resistance  $R_s$  was calculated to be  $1.17 \Omega \cdot \text{cm}^2$  based on the  $dV/dJ$ -( $J + J_{\text{SC}}$ ) $^{-1}$  curve [18]. The performance of the devices was relatively low. The main reason could be the poor CdS/ $\text{Sb}_2\text{Se}_3$  junction quality as will be evidenced by the  $C$ - $V$  and dark  $J$ - $V$  curves. As shown in Fig. 2(b), the built-in voltage ( $V_{\text{bi}}$ ) and the carrier concentration of  $\text{Sb}_2\text{Se}_3$  films were investigated by  $C$ - $V$  measurement. The experiment was tested at room temperature in darkness at a frequency of  $100 \text{ kHz}$  and AC amplitude of  $30 \text{ mV}$  [19]. The  $V_{\text{bi}}$  and the carrier concentration were calculated to be  $0.47 \text{ V}$  and  $7.6 \times 10^{15} \text{ cm}^{-3}$ , respectively. The smaller  $V_{\text{bi}}$  compared with the theoretical value of  $V_{\text{bi}}$  ( $0.81 \text{ V}$ ) demonstrated a low heterojunction quality [19,20]. And the big gap between the  $V_{\text{OC}}$  and  $V_{\text{bi}}$  indicated the interface/bulk recombination had non-neglected impact on

$\text{Sb}_2\text{Se}_3$  solar cell performance [21]. The dark  $J$ - $V$  curve showed a much increased shunt leakage at the reverse voltage. Moreover, the shunt current is increased non-linearly at the reverse voltage larger than  $-0.4 \text{ V}$ , as shown in Fig. 2(c). For dark  $J$ - $V$  curve, the current in reverse bias is dominated by shunt current and the current in forward bias is dominated by the main diode. In traditional equivalent circuit model for  $\text{Sb}_2\text{Se}_3$  solar cell, the shunt current is considered to be ohmic in nature, and the shunt current predicts a linear response. So any deviation from the linear behavior implies the presence of non-ohmic shunt currents [16]. Furthermore, Fig. 2(c) inset shows the derivative  $dJ/dV$  against  $V$  near  $J_{\text{SC}}$  and in reverse bias. If the shunt mechanism is ohmic,  $dJ/dV$  will be flat with the value in reverse bias equal to shunt conductance  $G$ . The increase of  $dJ/dV$  with the increased reverse voltage also indicated the non-ohmic shunt mechanisms in the device.

Shunt current sensitively depends on the solar cell fabrication technologies, cell types and microstructures of devices. For a realistic/non-ideal solar cell, especially for thin film solar cells, the possible shunting mechanisms include: (i) ohmic shunts: due to pinholes or via low-resistance grain boundaries in the absorber/window layer; (ii) space charge limited currents (SCLC): due to the presence of metal/semiconductor/metal-like regions, which may form upon discontinuity in the buffer layers and the subsequent localized absence of the junction built-in field; and (iii) weak diode: due to tunneling currents via high densities of mid-gap defect states in the depletion region of the p-n junction [16]. The non-ohmic shunts for both SCLC and weak diode have been observed in most types of solar cells, which were proved to have an important impact on the cell performance. In order to have a more identifiable analysis of the junction characteristics and shunting mechanisms, the dark  $J$ - $V$  curves were shown on a semi-log plot. As can be seen in Fig. 2(d), the shift from a linear ohmic shunt current in reverse voltage indicates the presence of an additional non-ohmic shunt



pathway. For thin film solar cells, non-linear dark current in reverse bias can be attributed to an effect of SCLC or diode breakdown, while the current caused by diode breakdown rarely occurs in the voltage range (up to  $-1$  V). So, for the non-linear dark current in reverse bias  $\text{Sb}_2\text{Se}_3$  thin film solar cells, SCLC is the most likely candidate to describe the non-ohmic shunts. In addition, the forward dark  $\ln(J)$  is increased linearly with the voltage at the voltage range of  $0 - 0.4$  V. The curve doesn't show an identifiable shoulder at the low forward bias, which indicates the forward current was dominated by single diode and no observable shunt current caused by the weak diode [16].

Actually, SCLC has been reported in many kinds of solar cells, such as inorganic Si, CdTe,  $\text{CuIn}_{1-x}\text{Ga}_x\text{Se}_2$ , and organic solar cells [15,16,22–24]. SCLC was supposed to exist in metal/semiconductor/metal-like microstructures [22,25]. In principle, SCLC was not expected in CdS/ $\text{Sb}_2\text{Se}_3$  solar cells which had an asymmetric structure and built-in potential. However, as the CdS window layer was very thin ( $\sim 60$  nm), the structure of FTO/ $\text{Sb}_2\text{Se}_3$ /Au could be formed by locally poor coverage of the CdS on FTO. In order to examine the possible shunt paths of SCLC, the local electrical conductivity of a 60-nm-thick CdS film grown on a glass/FTO substrate was probed by conductive atomic force microscopy (C-AFM) [26]. The poling voltage of  $-5$  V is applied over a  $2 \times 2 \mu\text{m}^2$  area. The C-AFM image and the corresponding AFM image of the surface of glass/FTO/CdS were shown in Fig. 3. The white dots on the C-AFM images represented detected current. Abundant leakage current contribution was clear from the C-AFM image. From the C-AFM images, we can see that the conductive regions of FTO/CdS, which was corresponding to the poor coverage of CdS, were randomly and densely distributed on the surface. According to the device structure and the above discussions, it could be believed that the SCLC shunt paths were mainly due to the local discontinuity or pinholes in the CdS thin film, forming the microstructure of FTO/ $\text{Sb}_2\text{Se}_3$ /Au (metal/semiconductor/metal-like microstructure). The model and the data fittings in the following strongly support this suggestion.

To make clear how and where the shunting paths influenced the device performance, a compact electric circuit model was developed to analyze the dark  $J-V$  characteristics of the cell device. Fig. 4(a) schematically shows the electric transport paths presented in a polycrystalline thin film  $\text{Sb}_2\text{Se}_3$  solar cell. The equivalent compact electric circuit for a thin film  $\text{Sb}_2\text{Se}_3$  solar cell is composed of an ideal diode and 2 shunting contributions, one ohmic shunting path represented by shunt resistance  $R_{sh}$ , and one non-ohmic shunting path represented by SCLC, as shown in Fig. 4(b). According to the equivalent circuit model, the total dark current density  $J_D$  of a cell device can be expressed as in the following [16],

$$J_D = J_0(e^{q(V-J_D R_s)/Ak_B T} - 1) + K(V - J_D R_s)^m + (V - J_D R_s)/R_{sh}$$

The first term  $J_0(e^{q(V-J_D R_s)/Ak_B T} - 1)$  represents the main diode

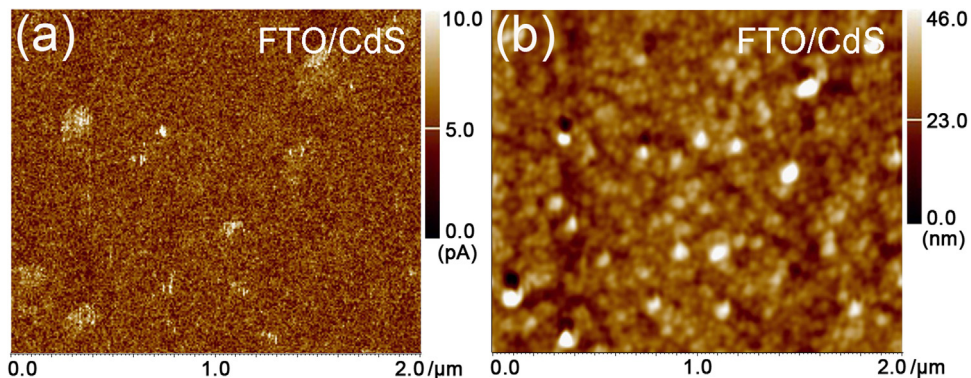


Fig. 3. (a) The C-AFM images of the FTO/CdS, and (b) is the corresponding AFM images obtained by scanning the same area on the sample where the C-AFM image was obtained, respectively.

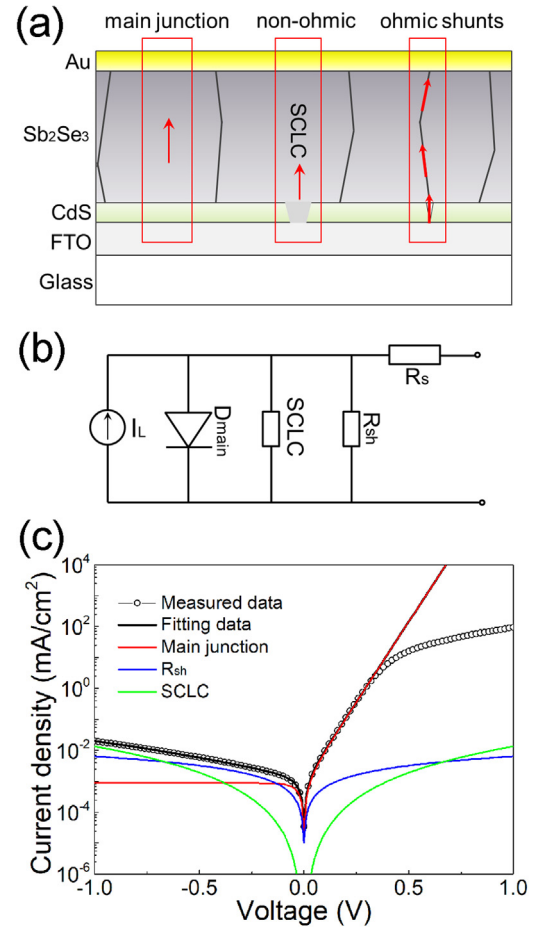
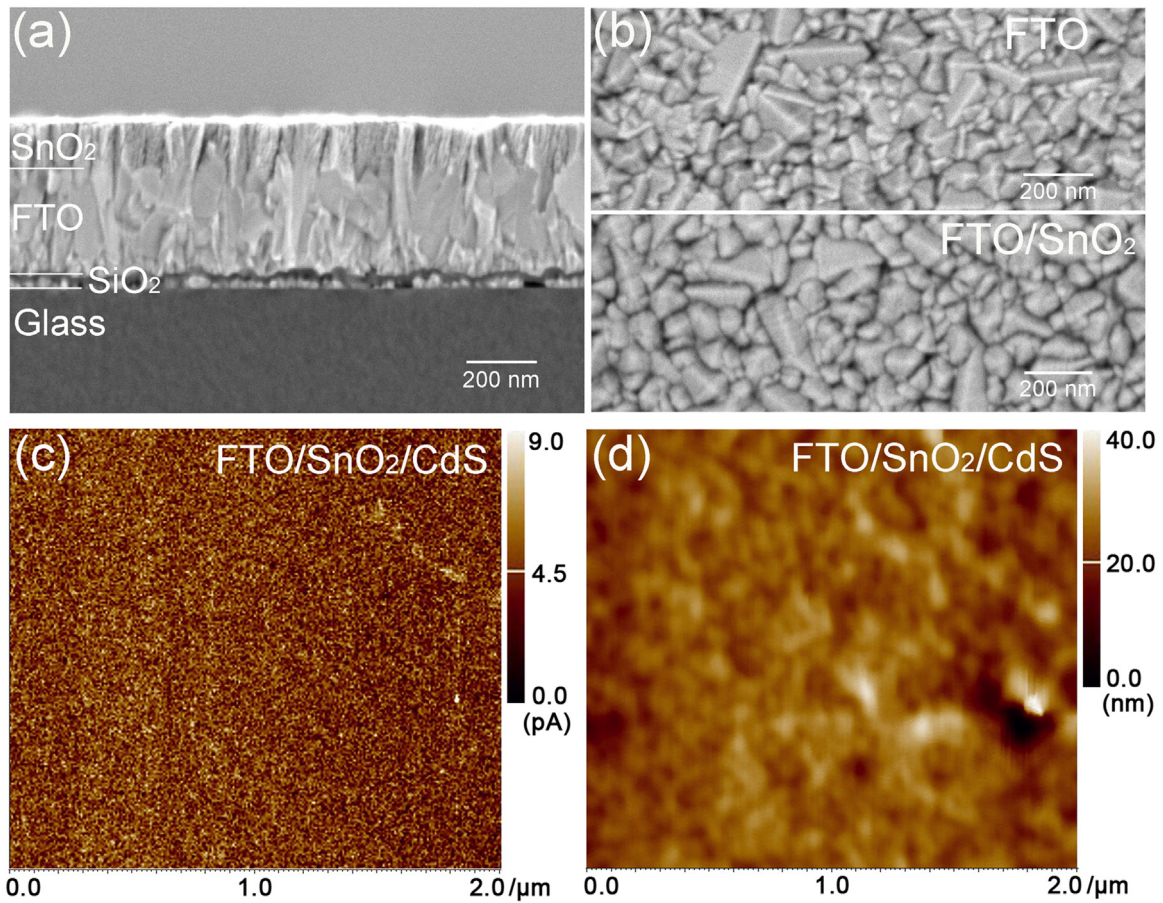


Fig. 4. (a) Schematic diagram of electric shunting paths presented in a  $\text{Sb}_2\text{Se}_3$  thin film solar cell; (b) equivalent compact electric circuit model for a  $\text{Sb}_2\text{Se}_3$  thin film solar cell; (c) experimental dark current-voltage data and the fitting curves from the contributions of different shunting paths.

junction.  $J_0$  is the reverse saturation current density,  $V$  is the output voltage,  $A$  is the ideality factor for the diode,  $R_s$  is the lumped ohmic series resistance. The term  $K(V - J_D R_s)^m$  represents the space-charge limited current, where  $K$  is related to the film thickness, trap distribution, and conductivity of the transport path.  $m$  is related to the density of states of the transport path,  $m = 2$  for a SCLC without traps and  $m > 2$  with traps [27]. The  $(V - J_D R_s)/R_{sh}$  represents the ohmic shunting current, which is mainly caused by pinholes in the CdS/ $\text{Sb}_2\text{Se}_3$  interface or via low-resistance grain boundaries in the junction region.

Fig. 4(c) shows the experimental dark  $J-V$  data and the curve



**Fig. 5.** (a) The cross-sectional SEM of a 150-nm-thick  $\text{SnO}_2$  layer deposited on glass/FTO substrate; (b) the top-view SEM of (upper) FTO and (lower) FTO/ $\text{SnO}_2$  (30 nm); (c) The C-AFM images of the FTO/ $\text{SnO}_2$ /CdS, and (d) is the corresponding AFM images obtained by scanning the same area on the sample where the C-AFM image was obtained, respectively.

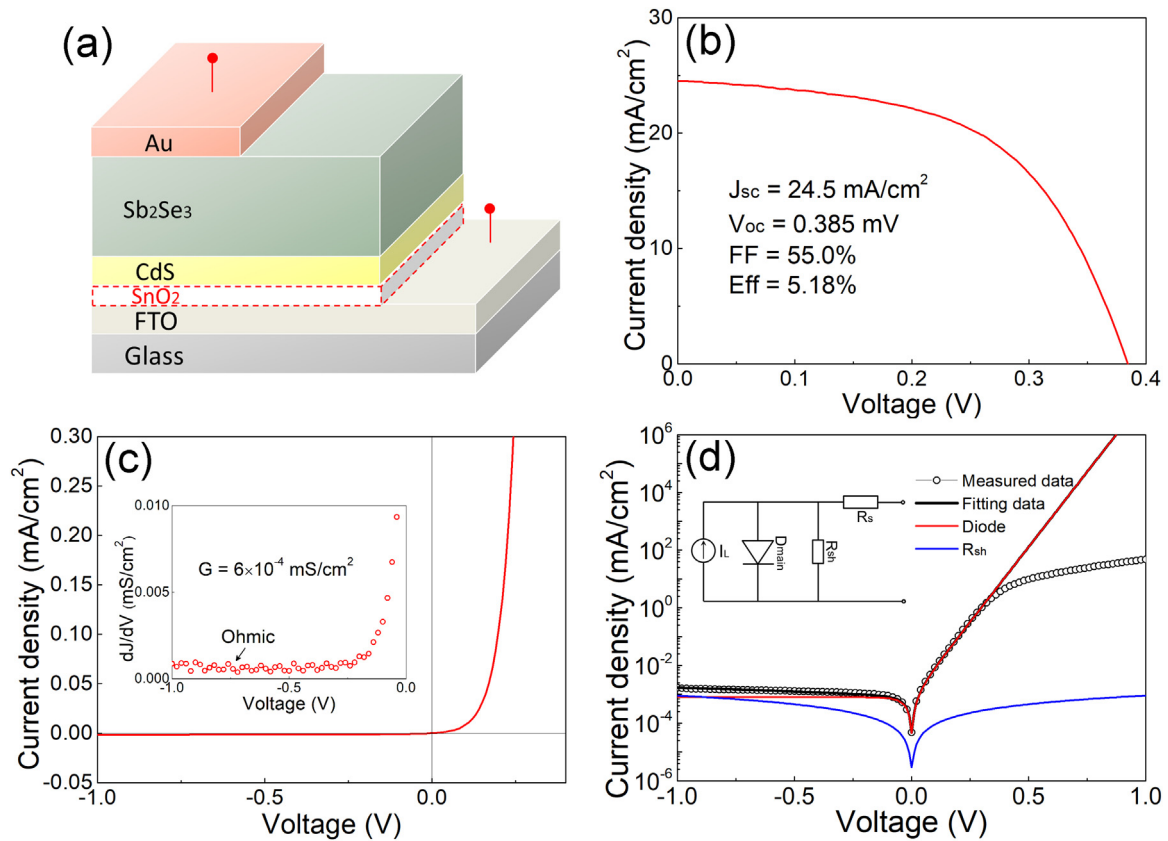
fittings, which accounted for the different contributions induced by the shunting paths discussed above. It can be seen that the main shunt paths come from the ohmic shunt resistance  $R_{\text{sh}}$  and the SCLC. For the region of high reverse voltage ( $V < -0.6$  V), the main shunt mechanism was non-ohmic shunt leakage and the shunt current came from SCLC was higher than the one came from  $R_{\text{sh}}$ . It was the contribution of SCLC that made the reverse dark  $J-V$  curve shift from the linear ohmic shunt current as shown in Fig. 2(c) and (d). It's worth pointing out that, the level off of the experimental  $J-V$  curves in Fig. 4(c) at voltage higher than  $\sim 0.4$  V was induced by the voltage drop on the series resistance  $R_s$ . Under the reverse and forward voltage with an voltage value smaller than  $\sim 0.4$  V, the dark current was relatively low and so was the value of  $J_D \times R_s$ . So the series resistance  $R_s$  had little effect on the shunt current related data analysis. The parameters of the equivalent electric circuit model can be extracted from the curve fittings [15]. The reverse saturation current density  $J_0 = 9.1 \times 10^{-4}$  mA/cm<sup>2</sup> is relatively high compared with other efficient CdTe solar cells which usually has a value smaller than  $10^{-7}$  mA/cm<sup>2</sup> [14]. The diode ideality factor  $A$  is 1.6, indicating that the junction current was dominated by the Shockley-Read-Hall recombination. The ohmic shunt resistance  $R_{\text{sh}}$  obtained by the fitting is  $1.5 \times 10^5 \Omega \cdot \text{cm}^2$ . In addition, the SCLC parameters  $K = 1.4 \times 10^{-2}$  and  $m = 2.8$  are related to the characteristics of the charge-transport path.  $m > 2$  indicates that the trap states are distributed in energy below the conduction band [27]. The values of SCLC parameters were rather large, indicating the non-ohmic shunt mechanism played an essential role in the electric shunting of the device.

### 3.2. $\text{Sb}_2\text{Se}_3$ thin film solar cells with high-resistance $\text{SnO}_2$ buffer at the front contact

In order to reduce the formation of shunt paths at the FTO/ $\text{Sb}_2\text{Se}_3$  interface, a high-resistance transparent  $\text{SnO}_2$  layer was deposited on the surface of FTO as a buffer between FTO and the CdS window layer. To verify the detailed microstructures of FTO/ $\text{SnO}_2$  interface and  $\text{SnO}_2$  layer, a 150-nm-thick  $\text{SnO}_2$  layer was fabricated, as shown in Fig. 5(a). Thicker  $\text{SnO}_2$  layer made it easier to image the layer under SEM. It can be seen that the  $\text{SnO}_2$  layer had a good conformal structure with the FTO substrate. The film had a good crystallinity and the grains were grown in the vertical direction. The upper part of Fig. 5(b) shows the surface morphology of the 300-nm-thick FTO, and the lower part shows the surface morphology of a 30-nm-thick  $\text{SnO}_2$  layer (the film thickness was used in the device) deposited on FTO/glass substrate. The cladding  $\text{SnO}_2$  layer was continuously and uniformly deposited on the surface of FTO. The C-AFM image and the corresponding AFM image of the surface of FTO/ $\text{SnO}_2$ /CdS were shown in Fig. 5(c) and (d). The C-AFM image reveals that the local conductive regions were reduced obviously. With the insertion of  $\text{SnO}_2$  buffer, the direct contact between FTO and  $\text{Sb}_2\text{Se}_3$  was blocked, and the corresponding shunt currents were reduced.

The performance of  $\text{Sb}_2\text{Se}_3$  solar cell with a  $\text{SnO}_2$  buffer is demonstrated in Fig. 6. The cell has a  $V_{\text{OC}}$  of 385 mV,  $J_{\text{SC}}$  of 24.5 mA/cm<sup>2</sup>, FF of 55.0%. The efficiency was increased by 38% from the value of 3.73–5.18%. It is notable that, with the insertion of a  $\text{SnO}_2$  buffer layer, the device demonstrated a nearly ideal dark  $J-V$  curve with linear and much lower reverse leakage current, as shown in Fig. 6(c). The linear behavior indicated the shunt current was ohmic in nature. The ohmic





**Fig. 6.** (a) Schematic of superstrate CdS/Sb<sub>2</sub>Se<sub>3</sub> solar cell; (b) light J–V and (c) dark J–V curves of the Sb<sub>2</sub>Se<sub>3</sub> solar cells with SnO<sub>2</sub> buffer layer; (d) experimental dark current–voltage data and the fitting curves from the contributions of different shunting paths for the Sb<sub>2</sub>Se<sub>3</sub> solar cells with SnO<sub>2</sub> buffer layer; the (c) inset shows shunt characterization by dJ/dV–V curve.

shunting can be confirmed by the dJ/dV–V curve as shown in Fig. 6(c) inset. The dJ/dV was flat with a constant value  $G = 6 \times 10^{-4} \text{ mS/cm}^2$ . Furthermore, the dark current density including the contributions of an ideal diode and an ohmic shunt resistance  $R_{sh}$  has been calculated and fitted to the experimental current data. The fittings are shown in Fig. 6(d). For the cell with SnO<sub>2</sub> buffer, the current under the forward bias was dominated by the main diode due to the forward bias carrier injection at the CdS/Sb<sub>2</sub>Se<sub>3</sub> junction. In the reverse bias, the main shunting path is the ohmic shunting. The shunt current caused by SCLC can be ignored. Including the effect of SCLC, the experimental data would be overestimated in the voltage range of  $< -0.5 \text{ V}$ . Compared to the solar cell without SnO<sub>2</sub> buffer, the diode of the device with SnO<sub>2</sub> had almost the same parameters with  $J_0 = 8.0 \times 10^{-4} \text{ mA/cm}^2$  and  $A = 1.6$ . While the shunt current related parameters were very different. The ohmic shunt resistance  $R_{sh}$  was  $1.1 \times 10^6 \Omega \cdot \text{cm}^2$ , which was consistent with the shunt conductance  $G$  calculated in Fig. 6(c) inset. The  $R_{sh}$  of the cell with SnO<sub>2</sub> buffer was about 7 times higher than that of the cell without SnO<sub>2</sub> buffer, indicating a smaller shunt current induced by ohmic shunt paths.

To evaluate the validity of including SCLC in the equivalent circuit model, the dark J–V curves of the Sb<sub>2</sub>Se<sub>3</sub> thin film solar cells with and without SnO<sub>2</sub> buffer were taken at various temperatures (303–383 K). Fig. 7(a) shows the dark J–V curves of the cell without SnO<sub>2</sub> buffer measured under different temperatures. The reverse dark current showed apparent non-linear behaviors under the reverse bias at 303 K, which was mainly caused by the SCLC as discussed before. With temperature increasing, the shape of reverse dark current changed a lot and the non-linear behaviors became weaker and weaker. The changes of the dark currents at different temperatures can be explained by the different temperature dependence of different shunting mechanisms. Different from other kinds of shunting mechanisms, SCLC had a weak

temperature dependence [23]. With temperature increasing, the dark current increased because of the increases of diode current and ohmic shunt current, but the increase of non-ohmic SCLC was much smaller because of the weak temperature dependence. The contribution of SCLC to total dark current at high temperature ( $> 383 \text{ K}$ ) was much less or even could be ignored, which resulted in the disappear of non-linear curve under reverse bias. For the device with SnO<sub>2</sub> buffer, the dark current increases as the temperature increases, since there is no effect of SCLC, the shape of the curves keeps almost the same (see Fig. 7(b)). We fitted the dark J–V curves of the cell without SnO<sub>2</sub> buffer employing the compact electric model proposed in this study. The values of the parameter  $m$  obtained at different temperatures are shown in the Fig. 7(c). The value of  $m$  is between  $2.4 \sim 2.8$ , and its temperature-dependent variation can be described by  $m = 554/T + 1$ , namely,  $m$  is proportional to the inverse of  $T$ . This temperature-dependent behavior is completely consistent with the theoretical prediction of  $m = T_c/T + 1$  [27]. Here,  $T_c = 554 \text{ K}$ . The value of the parameter  $K$  is increased with increased temperature, and this is also consistent with the previous theoretical study [27].

#### 4. Conclusion

In conclusion, we had prepared Sb<sub>2</sub>Se<sub>3</sub> absorber layers by close spaced sublimation for efficient Sb<sub>2</sub>Se<sub>3</sub> thin film solar cells. It was found that the device with the structure of glass/FTO/CdS/Sb<sub>2</sub>Se<sub>3</sub>/Au had a relatively large and non-ohmic shunt current. The origin and the mechanisms of shunt current were analyzed. An equivalent circuit model containing non-ohmic SCLC shunting mechanism was developed to describe the dark J–V characteristics in Sb<sub>2</sub>Se<sub>3</sub> solar cells. Finally, with the insertion of a SnO<sub>2</sub> buffer, the non-ohmic SCLC was suppressed and the total shunt current was reduced, leading to an enhancement in

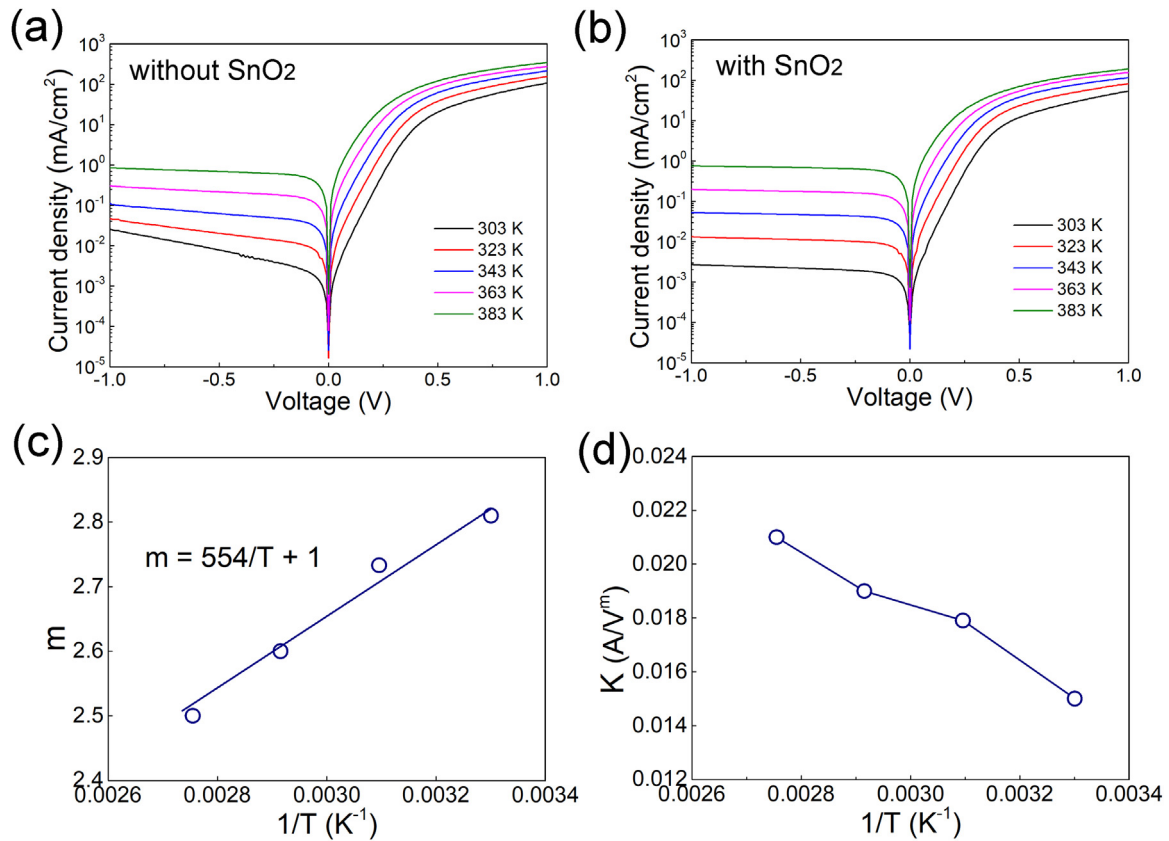


Fig. 7. Temperature-dependent dark J–V curves of (a) the  $\text{Sb}_2\text{Se}_3$  solar cells without and (b) with  $\text{SnO}_2$  buffer layer at different temperatures. (c) and (d) the parameter  $m$  and  $K$ , which were extracted from the curve fittings of J–V curves of the  $\text{Sb}_2\text{Se}_3$  solar cells without  $\text{SnO}_2$  buffer at different temperature, versus the inverse temperature  $1/T$ .

efficiency by 38% and an increase in open-circuit voltage by 17% compared to the one without  $\text{SnO}_2$ . This study demonstrated an important design strategy to reduce micro-shunting paths and to improve cell performance as well.

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