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A statistical model for the gettering of impurities on an atomistic scale

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The phenomena of impurities in Si in thermal equilibrium can be described on an atomistic scale. This model can statistically estimate the thermal equilibrium concentrations and the distribution of any metallic contamination atoms in advanced wafer structures if the gettering site densities in the wafer and their binding energies for the metallic impurity atoms are known. This model has the advantage that gettering phenomena can be calculated based on ab initio calculation results. Ab initio calculations indeed allow calculating the binding energy of any kind of contamination atom at any position in crystals without the need to perform extensive experiments. The model is illustrated for the gettering of Cu atoms in a p-type Si double layer structure consisting of a moderately B-doped layer, the "device layer," and a heavily B-doped layer, the "substrate." By using this statistical approach, we can also predict Cu solubility in Si wafers for various B-doping levels without the assumption of any solubility data in a previously-known doping level, as is typically found in the literature. The calculated results show good agreement with published experimental observations.

1 Introduction Gettering techniques are a key technology in Si-based VLSI manufacturing. Heavily B-doped Si substrates with a low doped epitaxial Si layer are one of the most promising solutions in future applications. Cu is the most important element to develop a gettering technique because it is widely used for interconnection inside Si device chips. However, it can be very harmful when it is present in the junction areas. Cu is also a very fast diffuser in Si and is mobile even at room temperature, see e.g. Ref. [1] and the references therein. Among the transition metals, Cu is the only one with a strong segregation at the Si surface after a drive-in from the surface to the bulk of the wafer. This segregation at the surface starts immediately after the surface has been cleaned by hydrochloric acid [1] and occurs even at room temperature during storage of the wafer for a longer time. Due to that, the stability and diffusion behavior of Cu in Si have been investigated extensively on the atomic scale [2-4]. However, these approaches are limited to bulk and do not explain the Cu behavior near and at the Si surface. An atomistic model for statistically describing the gettering of impurities has been proposed [5]. This atomistic model can in principle predict the thermal equilibrium concentrations and the distribution of any metallic contamination atoms in advanced wafer structures if the gettering site densities in the wafer and their binding energies for the metallic impurity atoms are known. By using this model, the thermal equilibrium concentration of Cu atoms in each part of a wafer structure was estimated [5].

In this paper, we survey the principle of this model by showing the gettering efficiency for a Si epitaxial wafer with a heavily B-doped substrate. In addition, we demonstrate the dependence of Cu solubility in a Si wafer on doped B concentration and temperature, as an example of applications using our model. The importance of the surface condition will be discussed.

2 Model for wafers on an atomistic scale
2.1 Cu diffusion model in a Si epitaxial wafer with heavily B-doped substrate [5] All gettering techniques are based on atomistic phenomena because the in-

dividual metal atoms that are diffusing through metastable sites are captured by stable gettering sites in the wafer. Therefore, a quantitative gettering model should be constructed by using an atomistic approach taking into account the total number of each type of gettering site including of course also the decrease in the formation energy, which is defined as the binding energy of a Cu atom to that gettering site. The building of an overall gettering model is illustrated for a two-layer Si structure shown schematically in Fig. 1(a). The formation energy decrease in a Cu atom happens not only when a Cu atom binds to a substitutional B atom but also when a Cu atom with a different charge state is formed by the change in the Fermi level. The latter change is dependent on temperature and is calculated for p⁻, p⁺, and p⁺⁺ (B concentration; $1×10^{15}$, $1×10^{19}$, $5×10^{19}$/cm³), respectively, as shown in Fig. 1(b) [5]. Thus, Cu atoms are considered to migrate inside the epitaxial wafer as they feel a potential as described in Fig. 2 [5].

(a)

(b)
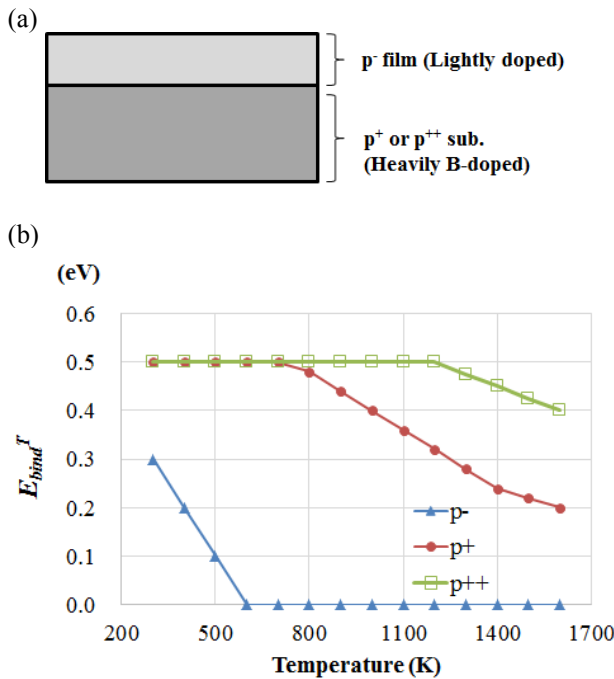
Figure 1 (a) Schematic view of the two layer system, (b) calculated binding energy of a Cu atom at the T-site as a function of temperature for three boron concentrations [5, 6].
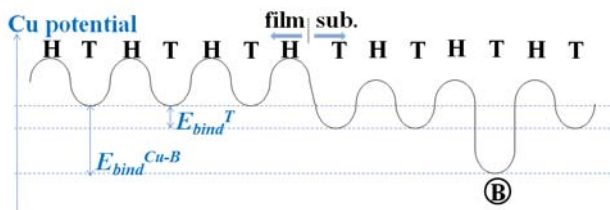
Figure 2 Schematic potential curve for Cu diffusion inside a Si epitaxial wafer with heavily B-doped substrate (under the condition; $E_{bind}^{T} = 0$ for p-Si film in Fig. 1(b)).

Basically, Cu atoms can migrate from a tetragonal (T)-site to the next T-site through a hexagonal (H)-site inside a Si crystal, but they tend to be bound at T-sites inside a heavily B-doped substrate, especially in the vicinity of B atoms.

2.2 Appling statistical dynamics To calculate occupation probabilities p^i for site type i in Eq. (1) by using a partition function Z in a standard form (see Eq. (2)), the number of the sites N^i (per area of the wafer surface) for type site i of the two illustrated in Fig. 2 was estimated [5].

$$p^i = \left\{ N^i \exp\left[-\frac{E_{bind}^i}{k_B T} \right] \right\} / Z . \tag{1}$$

$$Z = \sum_i N^i \exp\left[-\frac{E_{bind}^i}{k_B T} \right]. \tag{2}$$

In these equations, E_{bind}^i, k_B, and T are the binding energy for site type i, the Boltzmann factor, and temperature, respectively. The binding energy of the Cu-B pair E_{bind}^T is reported to be 0.57 eV [3], which is used in the following calculations.
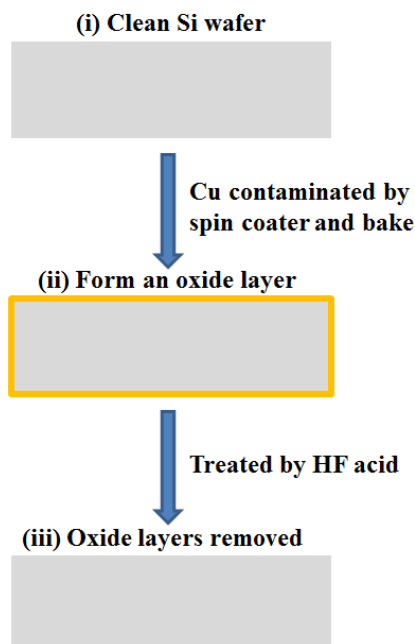
3 Results and discussion
3.1 Gettering efficiency for a Si epitaxial wafer with heavily B doped substrate Using Eqs. (1) and (2), the gettering efficiency at the substrate depending on the temperature for a 3-μm epitaxial wafer with a p⁺ substrate and p⁺⁺ substrate, respectively, of 100, 50, and 30 μm thickness, was calculated (Fig. 3 [5]). The open symbols are experimental data in Ref. [8], and they obtained a good coincidence.
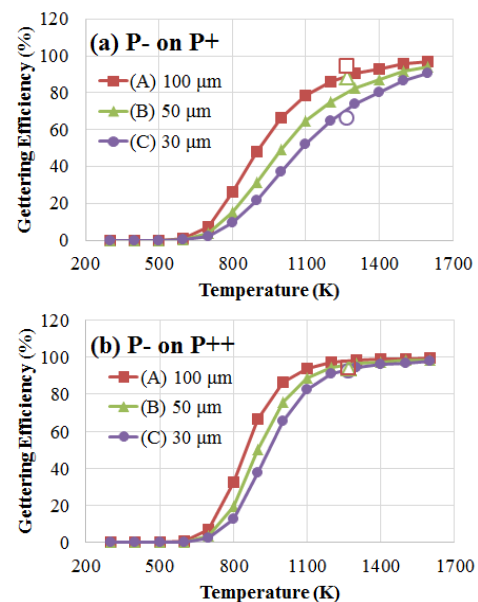
Figure 3 Calculated dependence of gettering efficiency on the temperature for a 3-μm epitaxial wafer with (a) p⁺ substrate and (b) p⁺⁺ substrate, respectively, of 100, 50, and 30 μm thickness [5]. Open symbols are published experimental data [7].

3.2 Importance of surface conditions of the wafer in gettering tests As experimentalists reported [1], the surface condition changes as the steps in the test proceed. In the preparation for gettering tests, test wafers must be finalized using chemical cleanings to remove contaminations from the surfaces, and the bare surfaces are kept clean or covered by a very thin chemically-formed oxide layer (step (i) in Fig. 4) before starting the test. Such surfaces will be required to allow driving intentionally contaminated atoms into the inside of the wafer in this step and/or the next bake step. During the bake step, oxide layers with a considerable thickness cover the wafer surfaces (step (ii) in Fig. 4). Due to this, the contaminated atoms inside the wafer are relatively stable and prevent out-diffusion.

(i) Clean Si wafer

Cu contaminated by spin coater and bake

(ii) Form an oxide layer

Treated by HF acid

(iii) Oxide layers removed

Figure 4 Typical procedures for contamination test and schematic illustration of the wafer in each step.

Models discussed in the previous section had to include also a description of gettering at the wafer surface, in which the existence of binding sites for Cu atoms is assumed. A schematic model for a Cu diffusion with surface oxide layers (corresponding to step (ii) in Fig.4) is shown in Fig. 5(a), in which gettering sites just under the oxide layers are also shown. Such sites will be formed in the reaction of surface oxidation during the bake. The existence of a thin SiO layer between thermally oxidized SiO_2 and the Si substrate was re-recognized [8], and Cu atoms were actually detected inside this SiO layer [9]. This means that such a SiO layer had stable binding sites for Cu atoms in an atomistic scale. In the calculations for Fig. 3, the density of this site just under the SiO_2 layers is assumed to be equal to the density of the dangling bonds at the Si(100) surface, which is about 2.7×10^{15} cm^{-2} [5]. With these as-

sumptions, reproducing the contamination level in the surface (probably including the sub-surface region or the SiO layer) is straightforward when the surface oxides are removed, as they were in the experiment performed by Shabani et al. [1] within the experimental error, assuming that the binding energy for Cu atoms just under the SiO_2 layers E_{bind}^{surf} is 1.387 eV for the lower level of Cu contamination [5].

As mentioned in the introduction, Cu is the only transition metal with a strong segregation at a Si surface. This segregation starts just after the surface oxide layer is removed (step (iii) in Fig. 4). This segregation at a Si surface is a slow phenomenon probably due to the band bending near the surface [10], but it is very strong. This strength is probably because a lot of space is available to store Cu atoms, e.g., Cu aggregations near the surface or Cu atoms terminating Si dangling bonds at the surface although the structure is still unclear in detail. Thus, we can describe such surfaces with so many marks that mean gettering sites at or near the wafer surface in Fig. 5(b).

(a)

(b)
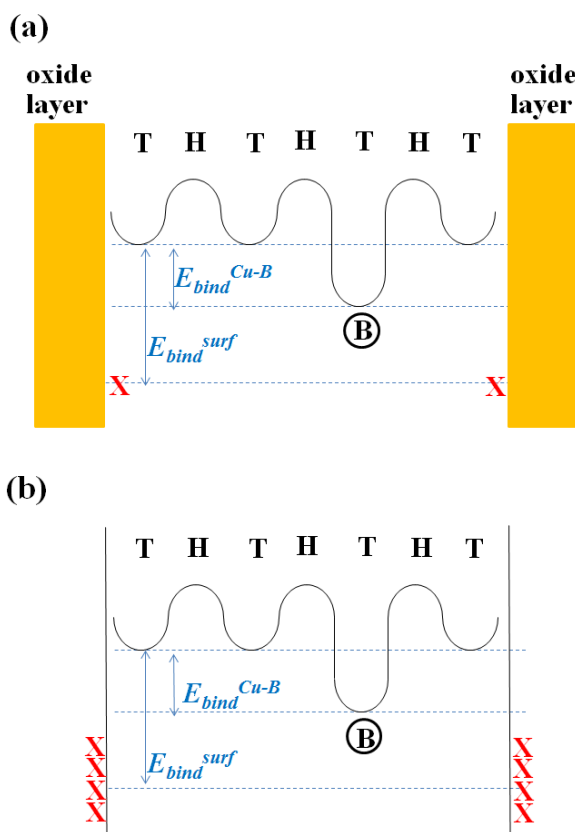
Figure 5 Schematic models for a Cu diffusion with wafer surfaces; (a) with surface oxide layers, (b) without surface oxide layers. The mark (X) means gettering sites at or near the wafer surface.

3.3 Cu solubility in a Si wafer Finally, we calculated the doped B concentration and dependence on tem-

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perature of Cu solubility in a Si wafer by using our proposed model. In the calculation, we did not use Cu solubility in intrinsic Si experimentally obtained as was used previously reported [11]. However, in our calculation, we considered step (ii) in Fig. 4(b), in which the surface oxide is formed because this formation is unavoidable in usual solubility tests (high temperature bake). Therefore, we used only both gettering site densities and their binding energies described in Fig. 5(a).

During the drive-in process under this situation, a bottle neck occurs in the path near the wafer surface for Cu atoms to diffuse into inside of the wafer. Solubility is defined as the maximum concentration in a crystal. Therefore, solubility under this situation is defined as the Cu concentration inside the wafer when the condition, $C_{contami} \times p^{surf} = N_{bind}^{surf}$, is achieved, where $C_{contami}$ is the maximum amount of the total contaminated Cu atoms per unit area of the wafer surface inside the oxide layers. Using the same parameters (energies and site number) for the calculation in Fig. 3, we obtained the calculated solubility as functions of doped B concentration inside the wafer and temperature in Fig. 6. In the calculations of Fig. 6, the wafer thickness was supposed to be 1 mm, but the calculated solubility was in the same range as if the thickness was as thin as 1 nm. The calculated results show good agreement with the published experimental observations [12]. However, the solubility could be higher if the bottle neck in the diffusion path during the drive-in were removed using some techniques like surface reforming.
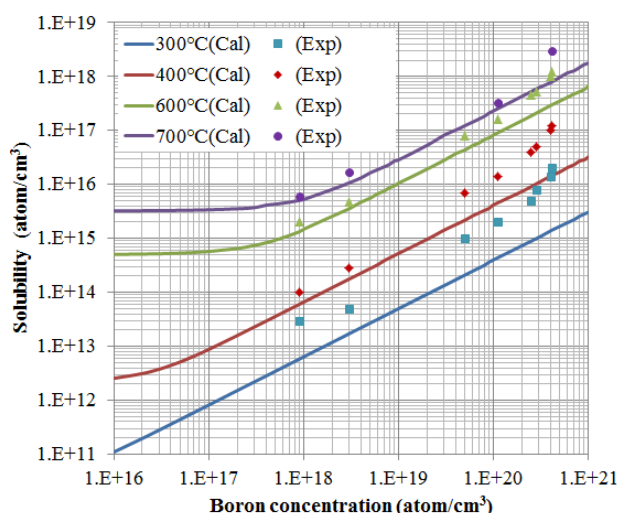
Figure 6 Calculated Cu solubility in a Si wafer with 1 mm thickness as functions of doped B concentration inside the wafer and of temperature (lines). Symbols are published experimental data [12].

4 Conclusion A method was proposed to estimate statistically the thermal equilibrium concentrations and the distribution of any metallic contamination atoms in advanced wafer structures if the gettering site densities in the wafer and their binding energies for the metallic impurity atoms are known. This model has a similar essence to the method called the "Hakoniwa method" in Ref. [13]. The model is illustrated for the gettering of Cu atoms in a p-type Si double layer structure consisting of a moderately B doped layer, the "device layer," and a heavily B doped layer, the "substrate." By using a statistical approach, we predict the gettering efficiency at the substrate. We also obtain the calculated solubility as functions of doped B concentration inside the wafer and temperature. These results show good agreement with published experimental observations. For these phenomena during the drive-in of Cu atoms inside the wafer, the surface condition is the key to controlling them.

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