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Thermal annealing studies in epitaxial 4H-SiC Schottky barrier diodes over wide temperature range

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ABSTRACT

Thermal annealing effects on electrical characteristics of Ni/4H-SiC and Ti/4H-SiC Schottky barrier diodes (SBDs) are investigated in the temperature range of 400–1100 °C. The thermal evolution of deep level traps in annealed SBDs is also analyzed by thermally stimulated capacitance (TSCAP) spectroscopy. As-deposited Ni/4H-SiC SBDs exhibited non-ideal electrical properties compared to Ti/4H-SiC SBDs. The electrical parameters of the Ni/4H-SiC SBDs are improved upon annealing at 400 °C for 30 min. in Ar ambient. However, deterioration in the SBD characteristics is observed from the temperature of 500 °C, so optimal annealing temperature for our Ni/4H-SiC SBDs is 400 °C. On the other hand, electrical properties of the Ti/4H-SiC SBDs are found to degrade even from the annealing temperature of 400 °C and hence as-deposited Ti/4H-SiC SBDs have the better properties. No considerable changes in the trap concentrations at E_c-0.63 eV and E_c-1.13 eV are identified in the SBDs up to the annealing temperature of 600 °C. The heat treatment on or above 800 °C results in poor rectifying behavior in both the SBDs, therefore the diode rectification is disappeared from 800 °C.

1. Introduction

Epitaxial 4H-silicon carbide (4H-SiC) Schottky barrier diodes (SBDs) are recommended for high-power electronic systems [1, 2], high-temperature applications [3], and radiation detection in hostile environments [4, 5]. For the possible use in these applications, the electrical properties of the 4H-SiC SBDs need to be optimized and improved. As deposited 4H-SiC SBDs may exhibit non-ideal electrical characteristics [6–9]. The electrical parameters of the SBDs can be improved by thermal annealing [10–16]. Among the metals suitable for contacts, Ni and Ti are preferred for Schottky contact on n-type epitaxial 4H-SiC [6–17]. The low work function of the Ti (unlike Ni) allows the formation of Ohmic contact on highly doped ($> 10^{18}\,cm^{-3}$) n-type 4H-SiC substrate with a low specific contact resistivity (SCR) of $2.25 \times 10^{-3}\,\Omega$-$cm^2$ [18] without any heat treatment [10, 19]. Hence, two types of SBDs such as Ni/4H-SiC SBDs and Ti/4H-SiC SBDs (Ti/Au bimetal layer Schottky contact) are fabricated in this work, with the Ti/Au bilayer as an Ohmic contact for both the SBDs.

Many authors investigated the thermal annealing induced changes in the electrical characteristics of Ni/4H-SiC and Ti/4H-SiC SBDs with Ni as back Ohmic contact [11, 12, 15, 16, 20–27]. Whereas, limited reports are available for heat treatment effects on 4H-SiC SBDs with the Ti Ohmic contact [10, 13, 14, 17, 19]. Kestle et al. [10] obtained an improved electrical performance at an annealing temperature of 500 °C for Ni/4H-SiC/Ti SBDs; but the authors observed poor rectifying nature at 600 °C. Vacuum annealed Ni/4H-SiC/(Ti/Ni/Ti) SBDs have shown [13] better Schottky barrier properties at the temperature of 500 °C. Zaman et al. [19] investigated the thermal annealing impacts on Ni/4H-SiC/(Ti/Ni/Ag) SBDs in the temperature range of 600 °C to 800 °C; the authors identified degradation in the diode rectifying behavior even at the annealing temperature of 600 °C. The Ni/4H-SiC SBDs and Ti/4H-SiC SBDs used in this work have the physical structure of Ni/4H-SiC/(Ti/Au) and (Ti/Au)/4H-SiC/(Ti/Au). Gupta et al. [14, 17] reported an improvement in the electrical characteristics of Ni/4H-SiC/(Ti/Pt/Au) SBDs upon annealing at 400 °C for 30 min in Ar ambient. Since our Ni/4H-SiC SBD structure is similar to Gupta et al. [14, 17], the same annealing parameters (30 min annealing in Ar ambient) are considered and the 400 °C is chosen as the lower limit for the annealing study. It is reported that Ni can form an Ohmic contact even with the lightly doped ($\sim 4 \times 10^{15}\,cm^{-3}$) n-type 4H-SiC around the annealing temperature of 950 °C [28–30]. Hence, annealing studies are carried out up to an elevated temperature of 1100 °C. The current work may be helpful in determining the optimal annealing temperature of similar kinds of SBD structures and to understand the annealing effects on their electrical characteristics over wide temperature range than studied so far.

The SBD characteristics not only depend on the metal/

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semiconductor interface properties, but also on the electrically active defects present in the SBDs [1, 4, 5, 8]. The thermal evolution of electrically active defects in the 4H-SiC SBDs has been studied by deep-level transient spectroscopy (DLTS) [31, 32]. Storasta et al. [31] analyzed the high-temperature annealing (1600–1800 °C) effect on $Z_{1/2}$ defect in Ni/4H-SiC/Al SBDs. Recently, Mannan et al. [32] reported the thermal annealing (100 °C to 800 °C) of deep level defects in Ni/4H-SiC/Ni SBDs for the annealing time of 30 min. In the above works, the contacts were formed only after the annealing process. Therefore, the current work is focused to analyze the thermal evolution of the trap signatures in the fabricated SBDs (i.e. after the contact formations) for the further improvement of the SBD characteristics. Thermally stimulated capacitance (TSCAP) spectroscopy [33–36], an irreversible single-shot capacitance transient technique, has been used [37] to identify the traps in the 4H-SiC SBDs. The attractive feature of the TSCAP compared to DLTS is the simple measurement setup. Furthermore, alike DLTS, the TSCAP is suitable to determine the type of defects (electron/hole trap) in the sample and the signal sensitivity is independent of the device leakage current. The changes in the trap concentrations are examined after annealing by using TSCAP.

2. Experiment

The SBDs were fabricated on 30 μm thick n-type epitaxial 4H-SiC substrate (epilayer doping $5 \times 10^{14}\,cm^{-3}$) from CREE Inc. The 4H-SiC SBD fabrication process steps are explained elsewhere [4, 5, 37]. In Ni/4H-SiC SBDs, Ni was considered as Schottky contact on Si-face and bimetal layer Ti (50 nm)/Au (150 nm) was used as Ohmic contact on C-face. On the other hand, in Ti/4H-SiC SBDs, the Ti (50 nm)/Au (150 nm) bilayer was chosen for the Schottky and Ohmic contacts. Both the SBDs were unterminated and unpassivated. The samples were not undergone any heat treatment after the contact formations. The active area of the studied SBDs was 3.8 mm^2.

2.1. Electrical and TSCAP measurements

Initially, I-V and C-V characteristics of the SBDs were measured at room temperature. The TSCAP measurements [37] were carried out in the temperature range of 150–650 K by using the Janis® cryogenic probe station. For acquiring the TSCAP spectrum, at first, the device under test (DUT) was cooled down to a low temperature of ~150 K (T_0) with or without the bias voltage of −40 V. Afterwards, the trap levels in the DUT were populated by forward biasing the SBD (with a current of 2 mA) for 100 s at T_0. At last, the DUT was heated at a heating rate of 0.12 K/s under −40 V bias voltage from the T_0 and changes in the DUT capacitance vs. DUT temperature (i.e. TSCAP spectrum) were recorded in the LabVIEW interfaced NI-PXI 1031 system. During the TSCAP scan, the SBD depletion capacitance was measured at 1 MHz frequency and with a 30 mV AC signal by using Agilent 4285A LCR meter and the DUT temperature was monitored by the Lakeshore 336 temperature controller.

2.2. Thermal annealing process details

The thermal annealing of SBDs was performed in the temperature range of 400 °C to 1100 °C with a step of 100 °C by using CARBOLITE GERO tube furnace (STF 16/450). The samples were loaded into the furnace from the room temperature to a particular annealing temperature, and then samples were annealed for 30 min in Ar atmosphere. After the heat treatment, the samples were unloaded from the furnace and were cooled under normal ambient conditions for 30 min. Subsequently, the electrical and TSCAP measurements were conducted.

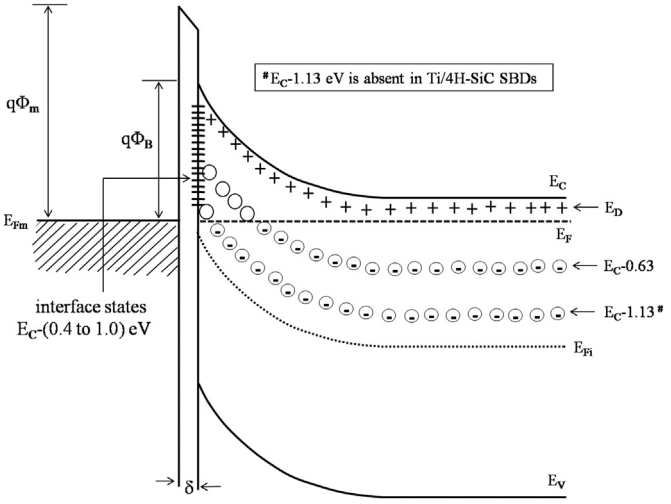

Fig. 1. The energy band diagram of 4H-SiC Schottky barrier diode with a thin interfacial oxide layer (δ) under equilibrium condition; the figure also displays the energy location of the deep level traps (E_C-0.63 eV and E_C-1.13 eV) in the 4H-SiC epitaxial layer and the energy level distribution (E_C-0.4 eV to E_C-1.0 eV) of the interface states at the metal/4H-SiC.

3. Results and discussion

3.1. As-deposited SBD characteristics

Electrically active defects (traps) in the SBDs identified by the TSCAP spectroscopy are reported elsewhere [37] and are summarized: Two deep traps such as P1 (E_C-0.63 eV, $Z_{1/2}$) and P2 (E_C-1.13 eV, EH5) are identified in the Ni/4H-SiC SBDs with a trap concentration of $\sim 7 \times 10^{12}\,cm^{-3}$ and $\sim 1.3 \times 10^{13}\,cm^{-3}$. It should be noted that the trap P2 (EH5) is detected in the TSCAP spectrum for the DUT cooling procedure carried out with and without bias voltage. Thus, the trap P2 does not exhibit the metastable nature of the EH5 defect reported in the literature [38, 39]. While, a single trap level P1 is found in the Ti/4H-SiC SBDs with the trap density of $\sim 6 \times 10^{12}\,cm^{-3}$. The trap P2 is not observed in the TSCAP spectrum for both the cooling conditions revealing that the P2 is absent in the Ti/4H-SiC SBDs. Fig. 1 shows the energy band diagram of the 4H-SiC Schottky barrier diode with a thin interfacial oxide layer (δ) under thermal equilibrium condition; the figure also displays the energy location of the deep level traps (E_C-0.63 eV and E_C-1.13 eV) in the 4H-SiC epitaxial layer and the energy level distribution (E_C-0.4 eV to E_C-1.0 eV) of the interface states at the metal/4H-SiC. The energy band diagram of the Ti/4H-SiC SBD also looks similar to the Fig. 1, except the absence the deep trap level E_C-1.13 eV.

Fig. 2 shows the forward current-voltage (I_F-V_F) characteristics of as-deposited Ni/4H-SiC SBDs along with the I_F-V_F at the annealing temperature of 400 °C (discussed later) and the inset displays the pre-annealing reverse current-voltage (I_R-V_R) plot. The forward voltage drop across the SBD at 1 mA is obtained as ~1.5 V. Two linear regions noticed in the semi-log I_F-V_F characteristics indicating the existence of inhomogeneous Schottky barrier height (SBH) at the Ni/4H-SiC interface associated with two distinct SBHs [6, 40, 41]. The SBH (Φ_B) is calculated by using the following expression [14, 17, 42]

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_S}\right) \quad (1)$$

where k is the Boltzmann's constant, T is the temperature, q is the elementary charge, A^* is the effective Richardson constant for n-type 4H-SiC ($146\,A\,cm^{-2}\,K^{-2}$) [14, 17, 43], and J_S is the reverse saturation current density (J_S) extracted from the linear region of $\ln(J_F) - V_F$ characteristics. The SBH for linear-1 and linear-2 regions is found to be

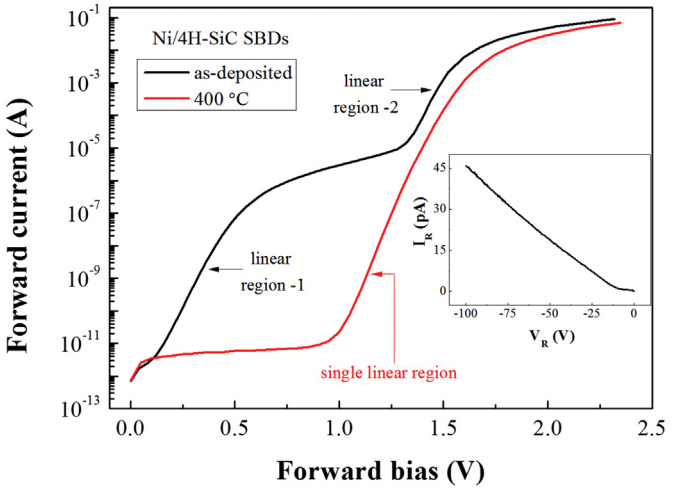

Fig. 2. Forward current-voltage (I_F-V_F) characteristics of as-deposited and annealed (at 400 °C) Ni/4H-SiC SBDs, and the inset shows pre-annealing reverse current-voltage (I_R-V_R) plot.

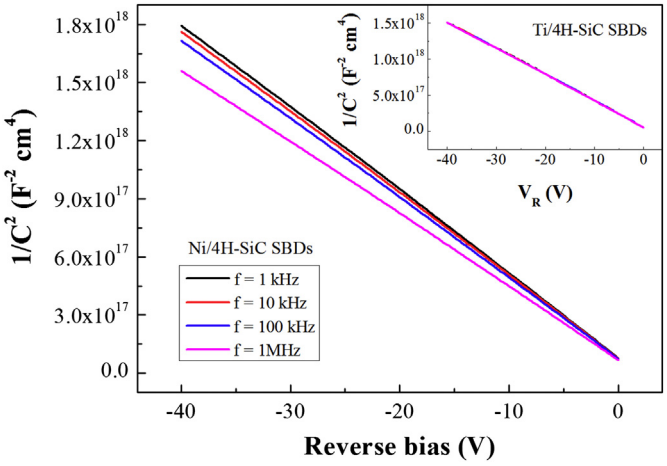

Fig. 3. Typical ($1/C^2$)-V characteristics of as-deposited Ni/4H-SiC SBDs at various signal frequencies (1 kHz to 1 MHz) and the inset displays frequency independent ($1/C^2$)-V characteristics of as-deposited Ti/4H-SiC SBDs.

1.2 eV (SBH1) and 1.51 eV (SBH2), respectively. The ideality factor (n) is computed by substituting the slope $dV_F/d(\ln J_F)$ of the $\ln(J_F) - V_F$ plot linear region into the below equation [14, 17, 42]

$$n = \frac{q}{kT}\left[\frac{dV_F}{d(\ln J_F)}\right] \tag{2}$$

The ideality factor for the linear-1 and linear-2 regions is determined as 1.4 (n1) and 1.6 (n2). These results suggest that the Ni/4H-SiC interface of the SBD might be rough [44], as a result the spatial variation in the SBH is presumed along the interface with two different values. This dual SBH behavior is also observed in SiC SBDs by Defives et al. [6], Bhatnagar et al. [40], and Zhang et al. [41]. It is considered that the electrons tend to flow through the SBH-1 at low bias voltages up to a condition that the voltage is sufficient to activate the current conduction via SBH-2 [6, 41]. Due to the current conduction through the localized regions at the Ni/4H-SiC interface, large deviations in the ideality factor (> 1) are noticed from the thermionic emission theory.

From the inset of Fig. 2, the increase in the reverse current (I_R) is noted with the bias voltage and the I_R at −100 V is found to be ~45 pA for Ni/4H-SiC SBDs. As expected [1, 40, 45], the leakage current is primarily generated due to the tunneling of electrons from metal to semiconductor rather than the thermionic emission, image force lowering, and thermal generation current components, as identified from the device simulations reported in our earlier work [37].

The typical ($1/C^2$)-V characteristics of the as-deposited Ni/4H-SiC SBDs at different signal frequencies (1 kHz to 1 MHz) are shown in Fig. 3 and the frequency independent ($1/C^2$)-V characteristics of the pre-annealed Ti/4H-SiC SBDs are depicted in the inset (discussed later). It is noticed that the Ni/4H-SiC SBDs exhibit frequency dependent ($1/C^2$)-V characteristics, i.e. capacitance increases with the signal frequency may be due to the presence deep level defects and/or interface states at metal/4H-SiC [42, 43, 46–48]. The thermal emission time constant $\tau(E)$ of deep level traps/interface states follows the equation [43]

$$\tau(E) = \frac{1}{\sigma \upsilon_{th} N_C}\exp\left(\frac{E_C - E}{kT}\right) \tag{3}$$

where σ is the capture cross section of the trap, υ_{th} is the carrier thermal velocity, N_C is the effective density of states in the conduction band, and E_C is the bottom of the conduction band energy. The estimated thermal emission time constant for traps $Z_{1/2}$ and EH5 is about 25 ms and 10^7 s at room temperature by taking the reported capture cross sections of 3.4×10^{-15} cm^2 [32] for $Z_{1/2}$ and 3.5×10^{-15} cm^2 [49] for EH5. Hence, the thermal emission time constant of these traps is supposed to be much longer than the measurement time (1 ms) even at the lowest operating frequency of 1 kHz. Thus, the deep level defects may not be responsible for the frequency dependent ($1/C^2$)-V characteristics of the Ni/4H-SiC SBDs and then it might be because of the interface states. Note that, the interface states may follow the applied AC signal at low frequencies and subsequently include their effect on the measured capacitance; but they may not follow the signal at high frequencies (> 100 kHz) [43, 48]. So, the increase in the $1/C^2$ at low frequencies (< 100 kHz) may reveal the existence of acceptor-like interface states at the Ni/4H-SiC SBDs. The negatively charged acceptor-type interface states can effectively reduce the measured capacitance at low signal frequencies. For this reason, the effective doping concentration (N_D) is calculated at the highest signal frequency of 1 MHz from the ($1/C^2$)-V characteristics to minimize the interface state charge effects, by using the following equation [17, 42]

$$N_D = \frac{2}{q\varepsilon_S}\left(\frac{d(1/C^2)}{dV}\right)^{-1} \tag{4}$$

where ε_S is the permittivity of 4H-SiC. The SBH can also be determined from the ($1/C^2$)-V characteristics as per the expression [17, 42]

$$\Phi_B = V_{bi} + \frac{kT}{q} + \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{5}$$

where V_{bi} is the built-in-voltage. The effective doping concentration of $\sim 5 \times 10^{14}$ cm^{-3} is computed using Eq. (4). The linear ($1/C^2$)-V characteristics seen in Fig. 3 indicate that the donor doping concentration is almost uniform across the 4H-SiC epilayer [17, 42]. The V_{bi} of ~2 V is extracted from the x-intercept of the ($1/C^2$)-V characteristics and the SBH of ~2.3 eV is estimated according to the Eq. (4); but this value greatly disagrees with the reported SBH from the C-V characteristics [14, 17, 50–53] and with the theoretical SBH of ~2.05 eV (determined using equation $\Phi_B = \Phi_m - \chi_s$ [42] by taking Ni work function as 5.15 eV and 4H-SiC electron affinity as 3.1 eV [52]). The large x-intercept value obtained from the ($1/C^2$)-V characteristics might specify the presence of interfacial layer at the Ni/4H-SiC interface [46, 47, 54]. Due to this anomalous behavior, SBH extracted from ($1/C^2$)-V characteristics are not presented further.

Fig. 4 shows the semi-log I_F-V_F characteristics of the as-deposited Ti/4H-SiC SBDs and the inset displays the pre-annealing I_R-V_R plot. In contrary to the Ni/4H-SiC SBDs, only one linear region is found in the semi-log I_F-V_F with a low forward voltage drop of 1.1 V at 1 mA. In particular, a high SBH of 1.3 eV is obtained together with a minor deviation in the ideality factor of 1.14. This is the best SBH value obtained

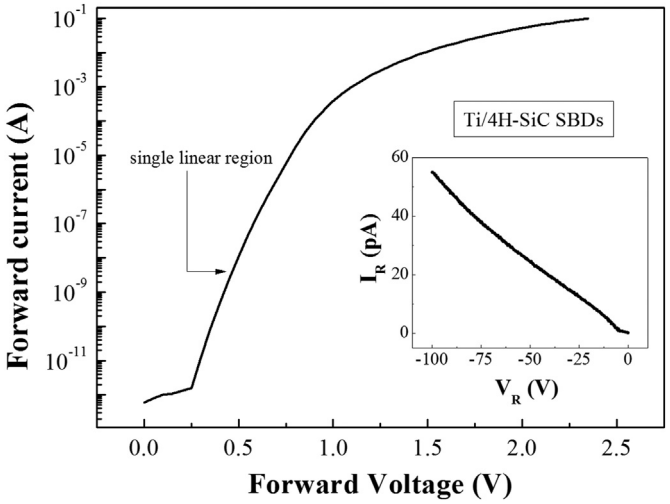

Fig. 4. Semi-log I_F-V_F characteristics of the as-deposited Ti/4H-SiC SBDs and the pre-annealed I_R-V_R characteristics are plotted in the inset.

for Ti/4H-SiC SBDs from the forward I-V characteristics, as compared to the literature data [1, 6, 7, 12, 16, 26, 51, 52]. Since the tunneling current is directly proportional to the square of the electric field (E_m^2) at the Ti/4H-SiC interface [1], the increase in the reverse current is observed with the bias voltage (see the inset of Fig. 4). The leakage current of the Ti/4H-SiC SBD at -100 V is ~55 pA, which is almost near to the reverse current of the Ni/4H-SiC SBDs and this observation is presumed as follows: the reverse current conduction preferentially occurs through the spatially localized barrier regions (rather than via SBH-2) in the Ni/4H-SiC SBDs. On the other hand, in Ti/4H-SiC SBDs, the electrons principally surmount the high SBH of 1.3 eV for producing the reverse current. Furthermore, the frequency independent ($1/C^2$)-V characteristics seen in the inset of Fig. 3 reveal the quality of the Ti/4H-SiC interface. From the results, it is noted that the Ti/4H-SiC SBDs may be attractive for high-power electronics by considering the low turn-on voltage and leakage current requirements.

3.2. Annealed Ni/4H-SiC SBD characteristics

The TSCAP spectra for annealed Ni/4H-SiC SBDs in the temperature range of 400 °C to 600 °C are displayed in Fig. 5. Note that, the TSCAP steps (P1 and P2) in Fig. 5 indicate electron traps in the SBD and height of the TSCAP step provides the trap concentration [37]. Downward

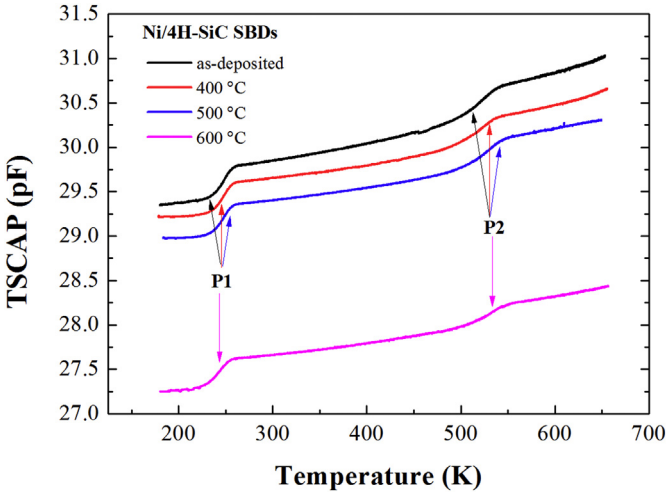

Fig. 5. TSCAP spectra for Ni/4H-SiC SBDs annealed in the temperature range of 400 °C to 600 °C.

shifting of the TSCAP spectrum is noticed after the annealing (discussed later). A small reduction in the trap concentration (N_T) for P1 and P2 is observed at each annealing temperature and are summarized in Table 1. However, there are no considerable changes in the trap density for P1 and P2 up to the annealing temperature of 600 °C, as similar to the observations of Mannan et al. [32]. The TSCAP measurements on the annealed Ni/4H-SiC SBDs are unsuccessful at 700 °C; hence the thermal evolution of the trap concentrations cannot be identified from 700 °C.

Fig. 6 shows the I_F-V_F characteristics of the Ni/4H-SiC SBDs as a function of annealing temperature (400 °C to 800 °C). A decrease in the forward current is noticed with the annealing temperature. The annealing induced changes in the forward voltage drop (V_F) at 1 mA, SBH, ideality factor of Ni/4H-SiC SBDs are calculated and are summarized in Table 1. The dual SBH behavior of the as-deposited Ni/4H-SiC SBDs are eliminated after annealing at 400 °C, as perceived from Fig. 2; thus a stable SBH (1.47 eV) and an improved ideality factor (1.2) are obtained at 400 °C. Probably due to the enhancement in the SBH, the increase in the forward voltage drop (V_F) at 1 mA (1.6 V) is noted at 400 °C. Nonetheless, the electrical parameters of the Ni/4H-SiC SBDs are found to be degraded from the annealing temperature of 500 °C (refer Table 1). Conversely, the increase in the V_F at 1 mA is observed from 500 °C even though the SBH reduces with the annealing from that temperature.

To understand the anomalous changes in the I-V characteristics of 4H-SiC SBDs at different annealing temperatures, density of the interface states (N_{SS}) in equilibrium with the semiconductor is determined from the forward I-V characteristics. Card et al. [55] reported that the SBH and ideality factor become bias-dependent in the forward region whenever the interfacial oxide layer and interface states present in the SBDs. The bias-dependent SBH can be considered as effective SBH (Φ_{eff}) in the calculation [14, 56]

$$\Phi_{eff} = \Phi_B + \left(1 - \frac{1}{n(V_F)}\right)V_F \tag{6}$$

where $n(V_F)$ is the bias-dependent ideality factor, which is calculated at each voltage as per the equation [14, 56]

$$n(V_F) = \frac{qV_F}{kT\ln(I_F/I_S)} \tag{7}$$

where I_S is the saturation current. In SBD, the density of interface states (N_{SS}) in equilibrium with the semiconductor is given as [14, 56]

$$N_{SS} = \frac{1}{q}\left(\frac{\varepsilon_i}{\delta}(n(V_F) - 1) - \frac{\varepsilon_S}{W}\right) \tag{8}$$

where W is the space charge width determined from ($1/C^2$)-V characteristics at 1 MHz, ε_i is the permittivity of the interfacial oxide layer, and δ is the thickness of the interfacial layer estimated from the C-V characteristics at 1 MHz [14]. In n-type semiconductor, the energy location of the interface states (E_{SS}) with respect to the conduction band edge (E_C) is written as [14, 56]

$$E_C - E_{SS} = q(\Phi_{eff} - V_F) \tag{9}$$

Fig. 7 shows the N_{SS} as a function of $E_C - E_{SS}$ for annealed (400–700 °C) Ni/4H-SiC SBDs calculated using Eqs. (6)–(9). An exponential increase of N_{SS} towards the bottom of the conduction band is seen in Fig. 7, similar to the earlier reported works [14, 56]. The energy level of the interface states is distributed in the range from E_C-0.4 eV to E_C-1.04 eV. The interface states at E_C-(0.4 to 0.515) eV may follow the applied AC signal during the C-V measurements at 1 kHz, as identified (using Eq. (3)) from the thermal emission time constant (< 1 ms) of these traps by assuming a capture cross section of 10^{-15} cm^2 [43]. Furthermore, it is estimated that the interface states near to the energy level E_C-0.4 eV ($\tau = \sim 10^{-5}$ s) may affect the capacitance up to the frequency of 100 kHz. Thus, the interface states located at the energies

Table 1
Changes in the electrical parameters and trap concentrations for Ni/4H-SiC SBDs after annealing.

Temp. (°C)	V_F at 1 mA (V)	SBH Φ_B (eV)	Ideality factor (n)	N_{eff} ($\times 10^{14}$ cm^{-3})	N_T ($\times 10^{13}$ cm^{-3})	
					P1	P2
As-deposited	1.5	1.2 (SBH1) 1.51 (SBH2)	1.4 (n1) 1.6 (n2)	~5	~0.7	~1.3
400 °C	1.6	1.47	1.2	~4.9	~0.65	~1.2
500 °C	1.65	1.3	1.66	~4.7	~0.6	~1.15
600 °C	1.75	1.18	1.72	~4	~0.55	~1.1
700 °C	1.85	1.1	2.2	~2.7	*	*
800 °C	4.35	1.03	10.1	#	*	*
900 °C	13.9	0.98	16.6	#	*	*
1000 °C	> 20	0.99	18.2	#	*	*
1100 °C	> 20	0.89	51	#	*	*

#N_{eff} is not obtainable due to the nearly geometrical capacitance.
*TSCAP is not measurable.

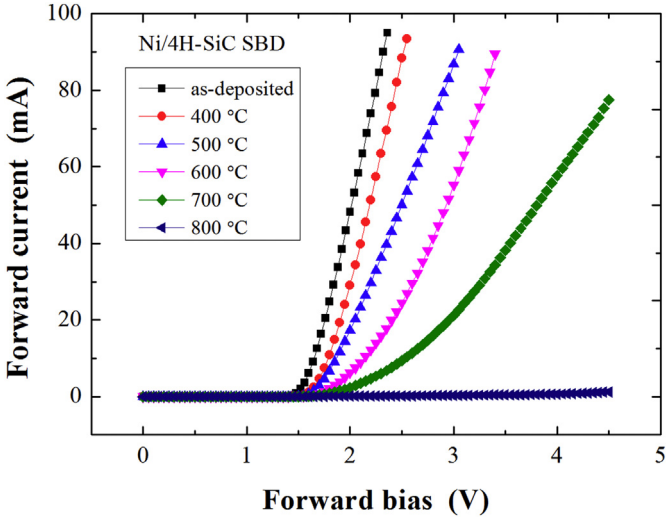

Fig. 6. Typical I_F-V_F characteristics of Ni/4H-SiC SBDs as a function of annealing temperature (400 °C to 800 °C).

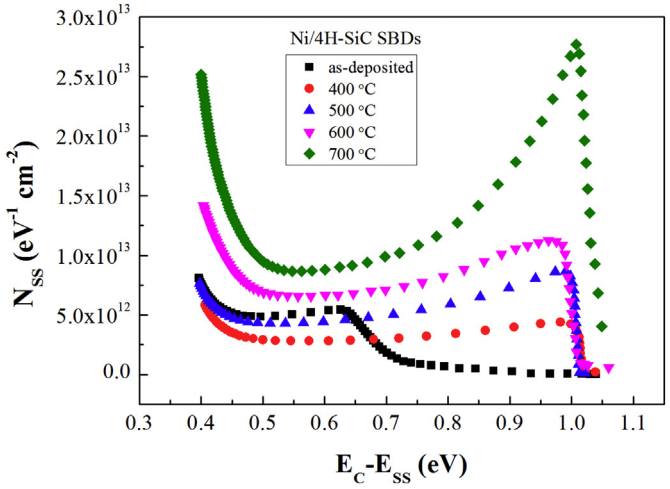

Fig. 7. The density of interface states (N_{SS}) distribution as a function of E_C-E_{SS} obtained from forward I-V characteristics of annealed (400–700 °C) Ni/4H-SiC SBDs.

E_C-(0.4 to 0.515) eV may be responsible for the frequency dependent C-V characteristics of the as-deposited Ni/4H-SiC SBDs (see Fig. 3). After annealing at 400 °C, considerable reduction in N_{SS} is noticed between the energies viz. E_C-0.4 eV to E_C-0.65 eV; this suggests that the interface traps responsible for the double SBHs are eliminated by the heat treatment at 400 °C. However, N_{SS} increases with the annealing temperature from 500 °C. At 600 °C, the increase in the N_{SS} is found to be 1.1×10^{13} eV^{-1} cm^{-2} at E_C-0.9 eV (from 4×10^{12} eV^{-1} cm^{-2} at 400 °C) and 1.4×10^{13} eV^{-1} cm^{-2} at E_C-0.4 eV (from 5.8×10^{12} eV^{-1} cm^{-2} 400 °C). Recall that, there are no significant variations in the concentration of the deep level traps (P1 and P2) up to 600 °C. Hence, the observed peculiar changes in the Ni/4H-SiC SBD electrical parameters (from 500 °C) are attributed to the annealing induced increase in the density of interface states, as noted from Fig. 7.

The annealing effects (400–700 °C) on the I_R-V_R characteristics of the Ni/4H-SiC SBDs are shown in Fig. 8. The SBD leakage current (4 pA at −100 V) is decreased by an order of magnitude after annealing at 400 °C may be due to the improvement in the Ni/4H-SiC interface quality with the stable SBH of 1.47 eV. Nevertheless, increase in the reverse current (degradation in I_R-V_R properties) is noticed from 500 °C possibly because of the reduction in the SBH (refer Table 1) and increase in the N_{SS}. Accordingly, it is considered from Fig. 7 that annealing the Ni/4H-SiC SBDs on or above 500 °C forms some new interface traps that yet again create an inhomogeneous Schottky barrier at the Ni/4H-SiC interface and effectively reducing the SBH. Consequently, the current conduction may occur through the localized barrier regions leading to an undesirable increase in the reverse current starting from the annealing temperature of 500 °C, as observed from Fig. 8.

Fig. 9 displays the ($1/C^2$)-V characteristics at 1 MHz of the Ni/4H-SiC SBDs obtained for different annealing temperatures. As the

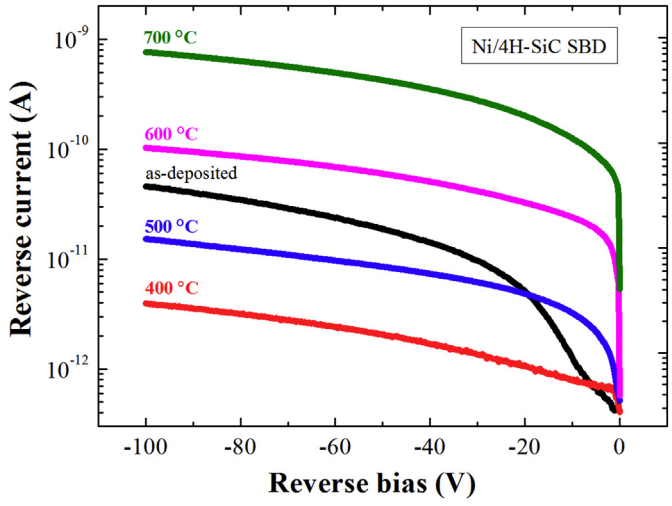

Fig. 8. Annealing induced changes in the I_R-V_R characteristics of Ni/4H-SiC SBDs for the temperatures of 400 °C–700 °C.

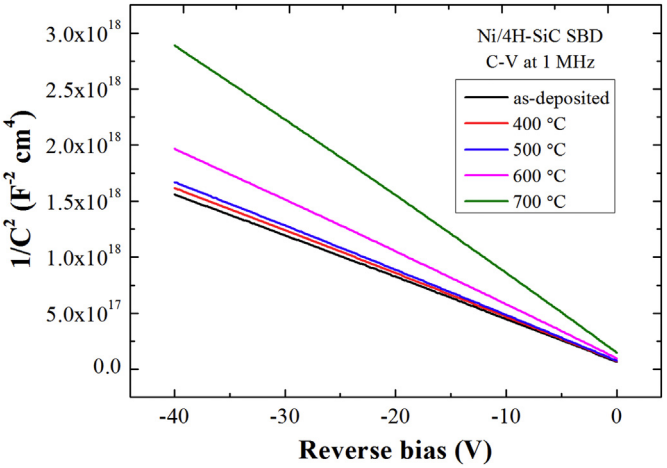

Fig. 9. Changes in the $(1/C^2)$-V characteristics at 1 MHz of the Ni/4H-SiC SBDs after annealing (400 °C–700 °C).

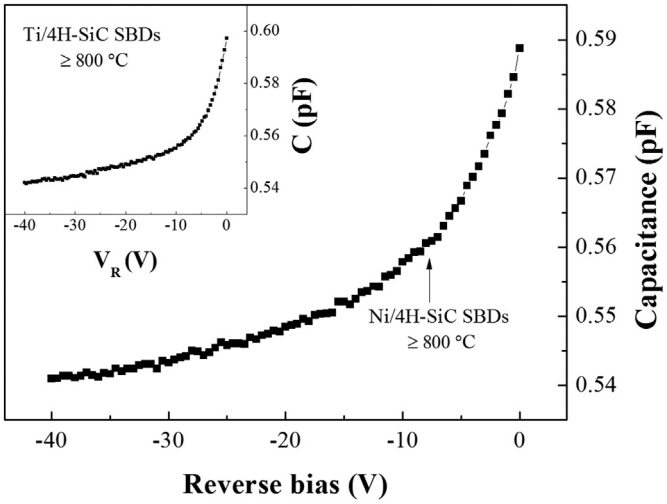

Fig. 10. Typical C-V characteristics (in diode geometrical capacitance range) measured at all signal frequencies of the annealed Ni/4H-SiC SBDs on or above the temperature of 800 °C and the inset shows the C-V plot of the Ti/4H-SiC SBDs from the annealing temperature of 800 °C.

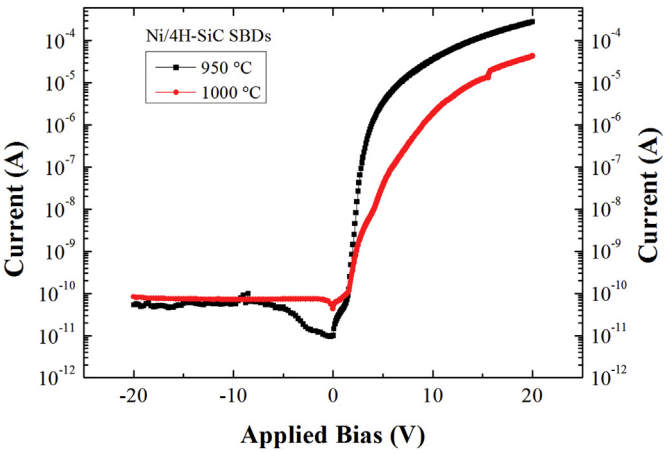

Fig. 11. Typical I-V characteristics (−20 V to 20 V) of the Ni/4H-SiC SBDs at the annealing temperatures of 950 °C and 1000 °C.

capacitance decreases ($1/C^2$ increases) with the annealing temperature, the downward shifting of the TSCAP spectrum is realized in Fig. 5 at each annealing condition. Moreover, the decrease in the effective doping concentration is identified from the $(1/C^2)$-V characteristics for annealed SBDs, as given in Table 1. The TSCAP results suggested that the donor concentration in the 4H-SiC epilayer is not affected by the deep level traps after the annealing. Therefore, the effective doping concentration of the epilayer is underestimated from the $(1/C^2)$-V characteristics might be due to the generation of acceptor-like interface states upon annealing. At 700 °C, the effective doping concentration is underrated by ~2 times of its original value, revealing the considerable increase in the negatively charged acceptor-type interface traps due to the annealing, as inferred from Fig. 7. Alike $(1/C^2)$-V characteristics shown in Fig. 3, the Ni/4H-SiC SBDs annealed at 400 °C exhibited frequency dependent $(1/C^2)$-V characteristics ($1/C^2$ decreases with frequency). Moreover, it is observed that the $(1/C^2)$-V characteristics of the Ni/4H-SiC SBDs are strongly frequency dependent for the annealing temperatures of 500–700 °C (not shown). This also indicates that the acceptor-type interface states exist in the annealed (≥500 °C) Ni/4H-SiC SBDs with significant concentrations.

The typical C-V characteristics (at all signal frequencies) of the Ni/4H-SiC SBDs on or above the annealing temperature of 800 °C are plotted in Fig. 10. Although a little change in the capacitance is seen with respect to the bias voltage, the obtained capacitance value is in the range of diode geometrical capacitance with a thickness of ~395 μm (including substrate and epilayer thickness) for the active area of 3.8 mm^2. For this cause, the effective doping concentration is not obtainable from the $(1/C^2)$-V characteristics from 800 °C. Furthermore, annealing the Ni/4H-SiC SBDs at or beyond 800 °C results in poor rectification properties such as very high V_F of > 5 V (at 1 mA), low SBH of < 1 eV and abnormal ideality factor of > 10 (refer Table 1). So, the electrical parameters of the Ni/4H-SiC SBDs are highly undesirable from 800 °C.

The I-V characteristics (−20 V to 20 V) of the Ni/4H-SiC SBDs at the annealing temperatures of 950 °C and 1000 °C are shown in Fig. 11. Asymmetrical I-V characteristics are perceived in Fig. 11. It is known that the Ni can form an Ohmic contact with the lightly doped n-type 4H-SiC epilayer around the temperature of 950 °C [28–30]. The Ni/4H-SiC SBDs used in this work have not shown the Ohmic I-V characteristics even after annealing at 1000 °C. In addition, it is reported that Ni Schottky contact (on 4H-SiC) properties are considerably improved upon the annealing temperatures of 500–700 °C due to the nickel silicide formation [9, 51, 52]. Here, substantial degradation in the Ni/4H-SiC SBD characteristics is observed for those annealing temperatures (500–700 °C). As a result, the deterioration in the back contact properties (Ti/Au bilayer with 4H-SiC) may be the reason for the disappearance of the SBD rectification, beginning from the temperature of 800 °C. But, the 800 °C is not the eutectic temperature of the Ti/4H-SiC interface, as noted from the work of Kim et al. [12]. So, further studies are needed to identify the mechanism behind the device failure at ~800 °C. Nevertheless, the current results clearly indicate that the rectification of the Ni/4H-SiC SBDs is vanished from the annealing temperature of 800 °C.

As similar to the work of Gupta et al. [14, 17], electrical properties of the Ni/4H-SiC SBDs are improved at the annealing temperature of 400 °C. Kestle et al. [10] and Zaman et al. [19] observed poor rectification in Ni/4H-SiC SBDs (with Ti based Ohmic contacts) even at the annealing temperature of 600 °C. The Ni/4H-SiC SBDs used in this work have shown reasonable electrical characteristics up to 600 °C and their rectification properties are disappeared only at 800 °C. Therefore, our Ni/4H-SiC SBDs have performed better than those reported in the annealing temperatures [10, 19].

3.3. Annealed Ti/4H-SiC SBD characteristics

Fig. 12 shows the TSCAP spectrum obtained with the Ti/4H-SiC SBDs upon the heat treatments from 400 °C to 600 °C. The movement of

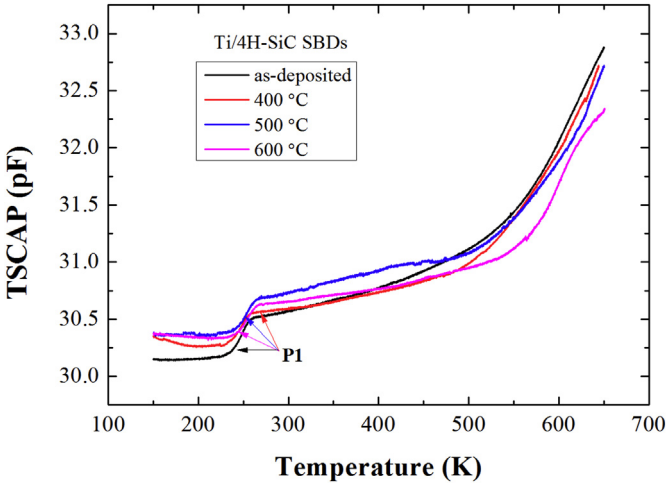

Fig. 12. TSCAP spectrum obtained with the Ti/4H-SiC SBDs upon the annealing temperature of 400 °C to 600 °C.

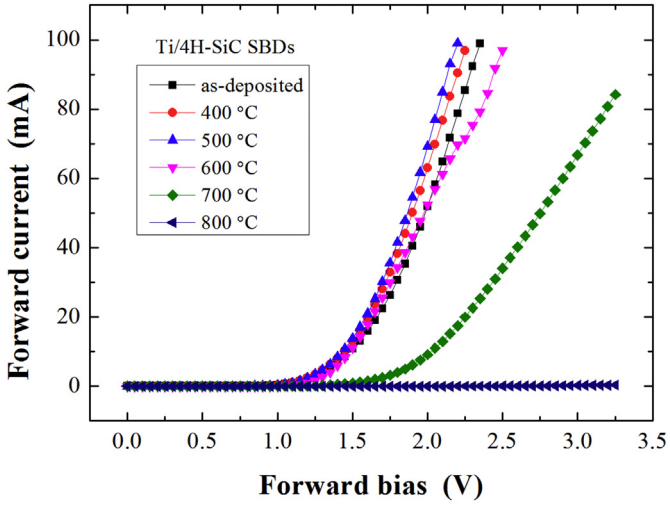

Fig. 13. I_F-V_F characteristics of the Ti/4H-SiC SBDs for different annealing temperatures (400 °C to 800 °C).

Table 2
Annealing induced changes in the electrical parameters and trap concentrations for Ti/4H-SiC SBDs.

Temp (°C)	V_F at 1 mA (V)	SBH Φ_B (eV)	Ideality factor (n)	Neff ($\times 10^{14}$ cm^{-3})	N_T for P1 ($\times 10^{13}$ cm^{-3})
As-deposited	1.1	1.3	1.14	~5	~0.6
400 °C	1.08	1.26	1.22	~5	~0.55
500 °C	1.07	1.2	1.32	~5.2	~0.52
600 °C	1.2	1.12	1.82	~4.9	~0.5
700 °C	1.55	1.08	3.24	~3.4	*
800 °C	4	1.01	6.8	#	*
900 °C	8.5	0.96	12	#	*
1000 °C	13	0.93	17.6	#	*
1100 °C	> 20	0.83	34	#	*

#N_{eff} is not obtainable due to the nearly geometrical capacitance.
*TSCAP is not measurable.

post-annealing spectrum is observed with respect to the as-deposited curve due to the annealing induced variations in the measured capacitance. Likewise the Ni/4H-SiC SBDs, no significant changes in the P1 trap concentration are identified in the Ti/4H-SiC SBDs up to the annealing temperature of 600 °C as summarized in Table 2.

The I_F-V_F characteristics of the Ti/4H-SiC SBDs annealed in the temperature range of 400 °C to 800 °C are displayed in Fig. 13. The annealing induced changes in the electrical parameters of Ti/4H-SiC SBDs are summarized in Table 2. The forward current is found to increase (i.e. V_F at 1 mA decreases) with the annealing temperature up to 500 °C may be due to the decrease in the SBH (refer Table 2). On the other hand, the increase in the V_F at 1 mA is detected from 600 °C (same behavior as Ni/4H-SiC SBDs), even though the SBH decreases with the annealing. The ideality factor of the Ti/4H-SiC SBDs has become worse upon the heat treatments.

Fig. 14 shows the density of interface states (N_{SS}) as a function of $E_C - E_{SS}$ for the annealed (400–700 °C) Ti/4H-SiC SBDs. It is determined from Figs. 7 and 14 that the N_{SS} is low in the as-deposited Ti/4H-SiC SBDs (5×10^{12} eV^{-1} cm^{-2} at E_C-0.4 eV) as compared to the Ni/4H-SiC SBDs (8.6×10^{12} eV^{-1} cm^{-2} at E_C-0.4 eV); which confirms the interface quality of Ti/4H-SiC SBDs as discussed in the Section 3.1. After annealing, the N_{SS} for Ti/4H-SiC SBDs is found to increase with the temperature. At 700 °C, the N_{SS} is considerably increased to 1.4×10^{13} eV^{-1} cm^{-2} at E_C-0.4 eV from its pre-annealing value. Moreover, it is viewed from Fig. 15 that the reverse current of the Ti/4H-SiC SBDs increases with the annealing temperature may be due to the reduction in the SBH and the increase in the N_{SS}. Overall, the

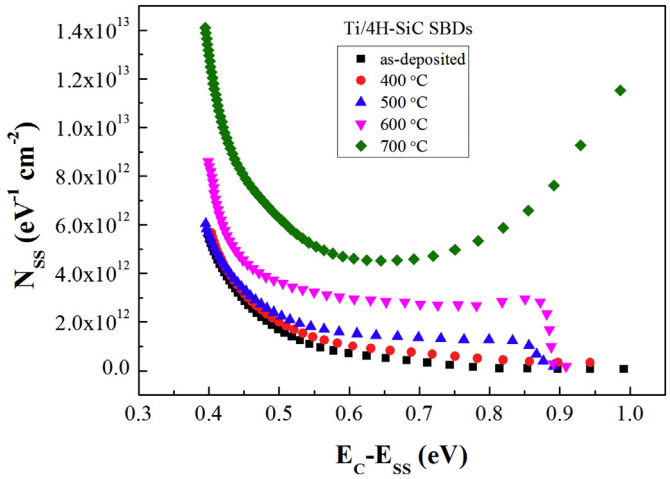

Fig. 14. Distribution profile of interface states density (N_{SS}) as a function of E_C-E_{SS} for annealed (400–700 °C) Ti/4H-SiC SBDs.

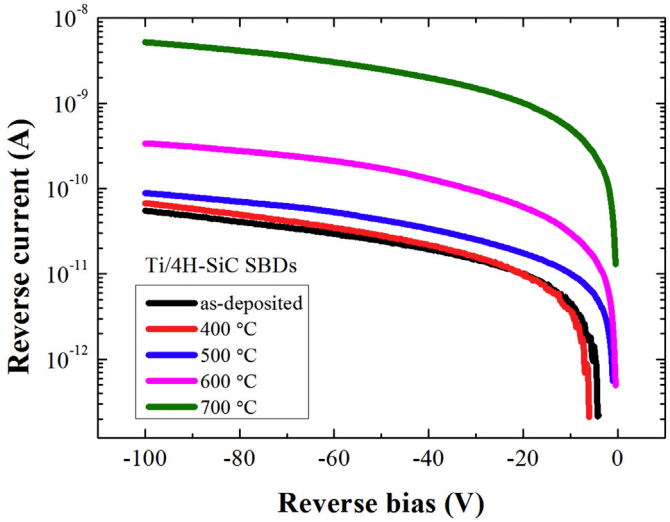

Fig. 15. Annealing induced changes in the I_R-V_R characteristics of Ti/4H-SiC SBDs for the temperatures of 400 °C–700 °C.

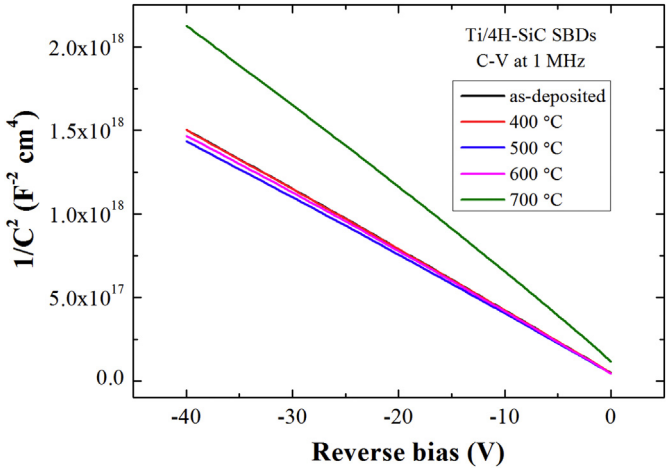

Fig. 16. Annealing effect on the $(1/C^2)$-V characteristics at 1 MHz of the Ti/4H-SiC SBDs for the temperatures 400 °C–700 °C.

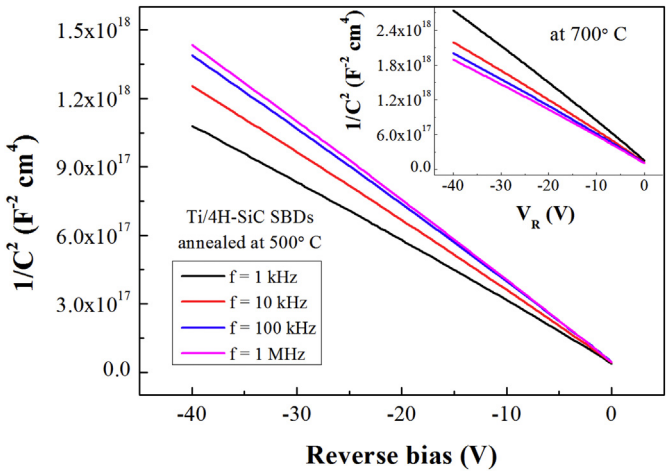

Fig. 17. $(1/C^2)$-V characteristics at different frequencies (1 kHz to 1 MHz) of Ti/4H-SiC SBDs at the annealing temperature of 500 °C and 700 °C.

electrical properties of the Ti/4H-SiC SBDs are degraded even from the annealing temperature of 400 °C.

The $(1/C^2)$-V characteristics at 1 MHz of the Ti/4H-SiC SBDs obtained after the annealing (400–700 °C) are plotted in Fig. 16. Almost the same $(1/C^2)$-V characteristics are perceived at 400 °C. So, the effective doping concentration is unchanged after the heat treatment at 400 °C. But, the annealed (at 400 °C) Ti/4H-SiC SBDs exhibited a little frequency dependent $(1/C^2)$-V properties (not shown). In this case, $1/C^2$ is found to increase with the signal frequency (in opposite to the Ni/4H-SiC SBDs) possibly due to the creation of donor-like interface states upon annealing [9]. From Fig. 17, strong frequency dependency is identified in the $(1/C^2)$-V plot of the Ti/4H-SiC SBDs annealed at 500 °C. May be due to the generation of donor-like traps at the Ti/4H-SiC interface, the $1/C^2$ is decreased at the annealing temperature of 500 °C (see Fig. 16). Accordingly, the effective doping concentration is slightly overestimated ($\sim 5.2 \times 10^{14}$) from the $(1/C^2)$-V characteristics at 500 °C (refer Table 2). While, the $1/C^2$ is found to increase with the annealing temperature from 600 °C (relative to the curve at 500 °C) and also the capacitance increases with the signal frequency (like Ni/4H-SiC SBDs). From the inset of Fig. 17, it is noticed that the $(1/C^2)$ decreases with the signal frequency at the annealing temperature of 700 °C. Accounting these results, it is assumed that annealing the Ti/4H-SiC SBDs on or above 600 °C produces acceptor-like interface states and that are dominant beyond the annealing temperature of 600 °C. The underestimation of the effective doping concentration ($\sim 3.4 \times 10^{14}\ cm^{-3}$) at 700 °C may also reveal that the above assumption is true. The anomalous variations in the Ti/4H-SiC interface properties (refer Fig. 14) might be the reason for the irregular forward I-V characteristics noticed from the annealing temperature of 600 °C. It is observed that the heat treatment process does not provide any improvement in the Ti/4H-SiC SBD characteristics.

The typical C-V characteristics (at all signal frequencies) of the Ti/4H-SiC SBDs on or above the annealing temperature of 800 °C are plotted in the inset of Fig. 10. The geometrical capacitance range is identified in the entire applied reverse bias voltage, as similar to the Ni/4H-SiC SBD case. In addition, the poor rectifying nature ($V_F > 4$ V at 1 mA, SBH < 1 eV and ideality factor > 7) is observed in the Ti/4H-SiC SBDs from the annealing temperature of 800 °C. The Ohmic I-V characteristics (like the I-V in Fig. 11) are also not noticed in the Ti/4H-SiC SBDs up to the temperature of 1100 °C. Thus, alike Ni/4H-SiC SBDs, the rectifying property of the Ti/4H-SiC SBD is vanished from 800 °C.

4. Conclusion

Annealing induced effects in the Ni/4H-SiC and Ti/4H-SiC SBDs are investigated in the temperature range of 400–1100 °C. As-deposited Ni/4H-SiC SBDs have shown non-ideal electrical characteristics might be due to the inhomogeneous SBH at the interface associated with the two distinct SBHs. On the other hand, high and stable SBH (1.3 eV), good ideality factor (1.14), low forward voltage drop (1.1 V at 1 mA) and low leakage current (~55 pA at −100 V) are obtained for the Ti/4H-SiC SBDs before annealing. Considering the low turn-on voltage and leakage current requirements, the Ti/4H-SiC SBDs are attractive for high-power electronics. The electrical properties of the Ni/4H-SiC SBDs are improved with the stable SBH of 1.46 eV after the heat treatment at 400 °C. However, from 500 °C, the electrical parameters are found to deteriorate with the annealing temperature. Hence, the optimum annealing temperature for our Ni/4H-SiC SBDs is ~400 °C. Whereas, there are no improvements in the Ti/4H-SiC SBD characteristics upon the heat treatments. Most importantly, the rectifying behavior of both the SBDs is disappeared from the temperature of ~800 °C.

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