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Analysis of interface states and series resistance of MIS Schottky diodes using the current–voltage (*I–V*) characteristics

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Abstract

The purpose of this paper is to analyze interface states in Al/SiO_2/p-Si (MIS) Schottky diodes and determine the effect of SiO_2 surface preparation on the interface state energy distribution. The current–voltage (*I–V*) characteristics of MIS Schottky diodes were measured at room temperature. From the *I–V* characteristics of the MIS Schottky diode, ideality factor (n) and barrier height (Φ_B) values of 1.537 and 0.763 eV, respectively, were obtained from a forward bias *I–V* plot. In addition, the density of interface states (N_{ss}) as a function of (E_{ss}–E_v) was extracted from the forward bias *I–V* measurements by taking into account both the bias dependence of the effective barrier height (Φ_e), n and R_s for the MIS Schottky diode. The diode shows non-ideal *I–V* behaviour with ideality factor greater than unity. In addition, the values of series resistance (R_s) were determined using Cheung's method. The *I–V* characteristics confirmed that the distribution of N_{ss}, R_s and interfacial insulator layer are important parameters that influence the electrical characteristics of MIS Schottky diodes.

Keywords: MIS Schottky diodes; *I–V* characteristics; Ideality factor; Barrier height; Interface states

1. Introduction

Surface and interface properties play an important role in the electrical performance of metal–semiconductor (MS) Schottky diodes and metal–insulator–semiconductor (MIS) structures with small dimensions. The performance of these devices especially depends on the formation of interfacial insulator layer between metal and semiconductor, the interface states located at the semiconductor/insulator interface, series resistance and an inhomogeneous Schottky barrier contacts. There are currently a vast number of reports of experimental studies on Schottky barrier heights in a great variety of MS and MIS Schottky diodes [1–13]. The first studies on the interfacial insulator layer, between metal and semiconductor in Schottky diodes were made by Cowley and Sze [4] who obtained their estimations from an analysis of the Schottky barrier heights with different metallization as a function of metal work function. The detailed discussion of the formation of barrier height between the metal and semiconductor on n-type and p-type Si wafer was given by Card [14]. He has shown that Φ_{Bn} (for n-Si) can be as low as 0.45 eV and Φ_{Bp} (for p-Si) as high as 0.75 eV in the presence of oxide/insulator layer between Al and Si. Card and Rhoderick [6] estimated the interface state density located at the insulator (SiO_2)/semiconductor (Si) interface and examined effects of the interface states on the ideality factor of the forward bias *I–V* characteristics.

Some studies [6–9,15–18] inspected the effects of the presence of an interfacial insulator layer and the interface states on the behaviour of Schottky diodes, and extracted the density distribution of interface states in the semiconductor band gap from the forward bias *I–V* characteristics.

In general, there are several possible sources of error, which cause deviations of the ideal behaviour such as

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electrical properties. Therefore, these errors must be taken into account. These include the effects of insulator layer between metal and semiconductor; interface state (N_{ss}), series resistance (R_s) and formation of barrier height. The series resistance is an important parameter, which causes the electrical characteristics of MIS Schottky diodes to be non-ideal [19–23].

In this work, we report on extraction of interface state density of Al/SiO_2/p-Si (MIS) Schottky diodes using the current–voltage (I–V) characteristics. The other purpose of this paper is the calculation of the characteristics parameters such as ideality factor, barrier height, density of interface states and series resistance of Al/SiO_2/p-Si Schottky diodes obtained from I–V characteristics at room temperature.

2. Experimental procedure

The Al/SiO_2/p-Si (MIS) Schottky diodes were fabricated on the p-type (B-doped) Si single crystals, with a (1 0 0) surface orientation, 280 μm thick, 2″ diameter and 8 Ω cm resistivity. For the fabrication process, Si wafer was degreased in organic solvent of $CHCLCCL_2$, CH_3COCH_3 and CH_3OH consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$:1 HF:35 H_2O, 20% HF and finally quenched in de-ionised water for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ cm for a prolonged time.

Immediately after surface cleaning, high purity aluminium (Al) metal (99.999%) with a thickness of ~2000 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer in the pressure of $\sim 2\times10^{-6}$ Torr in oil vacuum pump system. The ohmic contact was formed by sintering the evaporated Al back contact at 750 °C for 60 min in the flowing dry oxygen (O_2) ambient at rate of a 2 l/min. This process served both to sinter the Al and to form the required thin SiO_2 on the upper surface of the wafer. After following oxidation, the Si wafer was placed in the vacuum system and circular dots of 1 mm in diameter and 2000 Å thick aluminum rectifier contacts were deposited onto the SiO_2 surface of the Si wafer through a metal shadow mask in vacuum system in the pressure of $\sim 2\times10^{-6}$ Torr. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor. The deposition rates were about 1–3 Å/s. The interfacial layer thickness was estimated to be about 52 Å from measurement of the interface capacitance in the strong accumulation region for MIS Schottky diode [6].

The current–voltage (I–V) measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card at room temperature.

3. Results and discussion

When a metal–insulator–semiconductor (MIS) Schottky diyote with an interfacial insulator layer and series resistance R_s is considered, the current through a Schottky diode at a forward bias ($V \geqslant 3\,kT/q$), according to the thermionic emission (TE) theory, is given by [1–3]

$$I = I_o \exp\left(\frac{q(V-IR_s)}{nkT}\right)\left[1-\exp\left(-\frac{q(V-IR_s)}{kT}\right)\right] \quad (1)$$

where V is the applied voltage across to rectifier contact, n is the ideality factor, R_s is the series resistance including bulk and contact resistance, T is the absolute temperature in K, q is the electronic charge, k is the Boltzmann constant; and I_o is the reverse saturation current and can be written as

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \quad (2)$$

where A is the area of rectifier contact, A^* is the effective Richardson constant and equals to 32 $Acm^{-2}\,K^{-2}$ for p-type Si and Φ_B is the zero-bias barrier height. The ideality factor is a measure of the conformity of the diode to be pure thermionic emission, and it is determined from the slope of the linear region of the forward bias ln(I)–V characteristics through the relation,

$$n = \frac{q}{kT}\frac{d(V-IR_s)}{d(\ln I)} \quad (3a)$$

where d(V-IR_s)/dln$I$ is the slope of linear region of ln(I)–V plots. Also, the voltage-dependent ideality factor $n(V)$ can be written from Eq. (1) as

$$n(V) = \frac{q}{kT}\frac{(V-IR_s)}{\ln(I/I_o)} \quad (3b)$$

Fig. 1 shows the forward and reverse bias ln(I)–V characteristics of the MIS Schottky diode at room temperature. As can been seen in Fig. 1, the I–V characteristic of the MIS Schottky diode shows a good rectifying behaviour with relatively low leakage current of 0.5 μA at reverse bias of $V_R = -5$ V. The current curve in forward bias quickly becomes dominated by series resistance from contact wires or bulk resistance of the semiconductor, giving rise to the curvature at high current in the semilogarithmic ln(I)–V plot. Using Eqs. (2) and (3a), the values of the barrier height and the ideality factor were found to be $\Phi_B = 0.763$ eV and $n = 1.537$, respectively.

For MIS Schottky diode, this value of ideality factor obtained from the forward bias I–V plot is greater than unity, indicating the presence of a thin interface insulator layer between the Al layer and p-Si semiconductor. Also, such behaviour of ideality factor has been attributed to particular distribution of the interface states [15], the image-force effect, recombination–generation; and tunnelling may be other possible mechanisms that could lead to an ideality factor value greater than unity [2,6,7,24–26]. It should be noted that the effect of the series resistance in

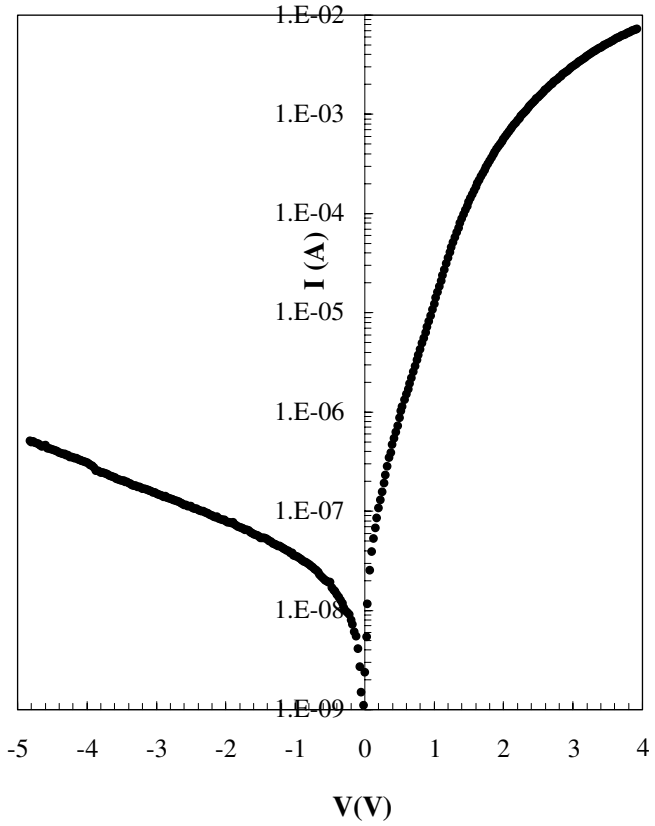

Fig. 1. The forward and reverse-bias I–V characteristics of the MIS Schottky diode at room temperature.

the linear region of forward bias I–V plot could be neglected in Fig. 1, but deviate considerably from the linearity due to the effect of series resistance, the interfacial insulator layer, and the interface states when the applied voltage is sufficiently large. In addition, the current rises slowly with the applied reverse bias and does not show any effect of saturation. This soft or slight non-saturating behaviour of reverse current may be explained in terms of the image force lowering of Schottky barrier height [2] and the presence of the interfacial insulator layer at metal–semiconductor interface [2,7].

The interface states for electrons or holes, while the density of states is always affected by interfaces, must not necessarily introduce energy levels in the band gap; i.e., only the density of states in the valence and conduction bands may be affected. The non-linearity of I–V characteristics of the Schottky diode at high bias values indicates a continuum of interface states, in which at equilibrium with the semiconductor [6]. Nevertheless, the Schottky diodes exhibit excellent rectification characteristics with a relatively low leakage current density. The effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and interface states located at the SiO_2/Si interface. The applied voltage dependence of the barrier height can be written as

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n(V)} \tag{4}$$

where β is the voltage coefficient of the effective barrier height Φ_e and is given by [6–9,27]

$$\Phi_e = \Phi_B + \beta(V - IR_s) = \Phi_B + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{5}$$

The Φ_e is a parameter that includes the effects of both interface states in equilibrium with the semiconductor [6]. For MIS Schottky diodes having interface states N_{ss} in equilibrium with semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [6], and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \tag{6a}$$

where ε_i and ε_s are the permittivity of the insulator layer (SiO_2) and the semiconductor, respectively; and W_D is width of the depletion region. This expression of voltage-dependent ideality factor is identical to Eq. (18) of Card and Rhoderick [6]. The expression for the interface state density as deduced by Card and Schroder [5,28] is reduced to [2,29]

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{6b}$$

where δ is the thickness of the interfacial insulator layer. The other parameters have been defined as before. The thickness δ can be obtained for the MIS Schottky diode from sufficiently high frequency ($f \geqslant 500$ kHz) C–V measurements using the equation $C_i = \varepsilon_i\varepsilon_o A/\delta$, where C_i is the capacitance of the interfacial insulator layer (SiO_2) [1,22], and ε_o is the permittivity of free space. The depletion layer width W_D being deduced from the experimental C–V measurements at high frequency is given by [1]

$$W_D = \sqrt{\frac{2\varepsilon_s}{qN_A}\psi_s} \tag{7}$$

where ψ_s is the surface potential and N_A is the carrier concentration. Furthermore, in p-type semiconductors, the energy of interface states E_{ss} with respect to the top of the valance band, E_v, at the surface of semiconductor is given as [6,9,30]

$$E_{ss} - E_v = q(\Phi_e - V) \tag{8}$$

Usually, the forward bias current voltage (I–V) characteristics are linear in the semilogarithmic scale at low voltages but deviate considerably from linearity due to the effect of parameters such as the R_s and the N_{ss} when the applied voltage is sufficiently large. The values of series resistance R_s were carried out using another method developed by Cheung [31]. The Cheung's functions given as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{9}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{10}$$

and

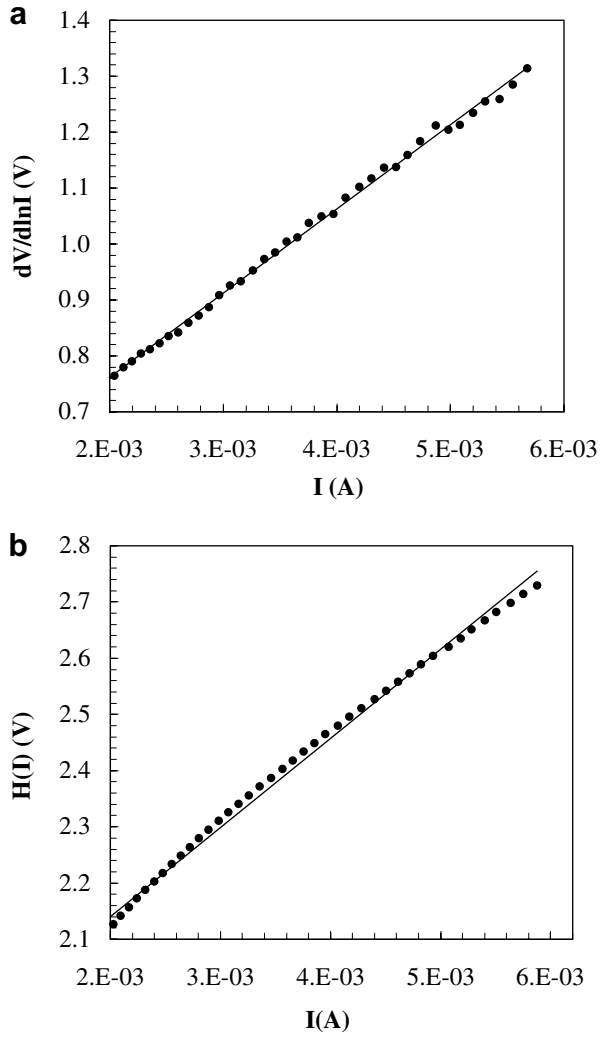

Fig. 2. (a) Experimental dV/dln$I$ vs. I and (b) H(I) vs. I plots for the MIS Schottky diode.

$$\mathrm{H}(I) = IR_s + n\Phi_B \tag{11}$$

should give a straight line for the data of downward curvature region in the forward bias I–V characteristics. The term IR_s is the voltage drop across the series resistance of Schottky diode. In Fig. 2a and b, the experimental dV/dln$I$ vs. I, and H(I) vs. I plots are for the MIS Schottky diode, respectively. Thus, the values of R_s and nkT/q have been obtained from the slope and y-axis intercept of the plot dV/dln$I$ vs. I.

Also, Fig. 2b obtained from Eq. (11) shows the plot of H(I) vs. I and gives a straight line with the y-axis intercept equal to $n\Phi_B$. The slope of this plot also provides the second determination of R_s, which can be used to check the consistency of Cheung's approach. The values of series resistance calculated from Eqs. (9) and (11) are presented in Table 1. As can be seen in Table 1, the values of series resistance R_s (dV/dln$I$) and R_s (H(I)) calculated from Cheung's functions dV/dln$I$ and H(I), respectively are in good agreement with each other [16,32–34].

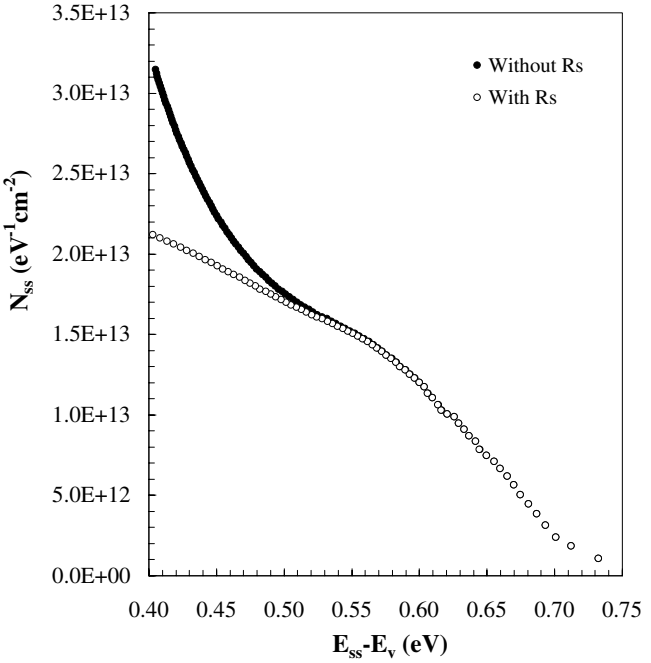

Fig. 3. The density of interface states (N_{ss}) distribution profiles as a function E_{ss}–E_v obtained from the forward bias I–V characteristics.

The energy distribution profiles of the interface states N_{ss} was obtained from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height Φ_e with and without series resistance R_s. The values of N_{ss} were calculated from Eq. (6b), by taking the values of voltage-dependent $n(V)$, $\varepsilon_s = 11.8\varepsilon_o$, $\varepsilon_i = 3.8\varepsilon_o$ and $\delta = 52$ Å.

Fig. 3 shows the density of interface states (N_{ss}) distribution profiles as a function E_{ss}–E_v at room temperature. The exponential increase of the interface states density from mid-gap towards the bottom of the conductance band is very apparent [5,6,28–30,35,36].

As seen in Fig. 3, the magnitude of the N_{ss} with and without the R_s at 0.40 $-E_v$ (eV) has changed in the range from 3.27×10^{13} to 2.14×10^{13} eV^{-1} cm^{-2}, respectively. The values of N_{ss} obtained by taking into account the R_s are lower than those of without the R_s. The above explanations clearly show that the R_s value should be taken into account in determining the interface state density distribution profiles. Similar results have been reported in the Refs. [12,15,16].

Table 1
Various parameters determined from I–V characteristics of Al/SiO_2/p-Si (MIS) Schottky diode

I_o (A)	n	Φ_B (eV)	R_s (dV/d(ln$I$)) (Ω)	R_s (H(I)) (Ω)	W_D (cm)	N_{ss} (eV^{-1} cm^{-2})
3.55×10^{-9}	1.537	0.763	150.69	158.84	2.74×10^{-4}	2.15×10^{12}

4. Conclusions

In this study, the electrical properties of $Al/SiO_2/p$-Si (MIS) Schottky diodes have been analyzed by using the current–voltage (I–V) characteristics at room temperature. The non-ideal forward bias I–V behaviour observed in the structure is attributed to a change in the metal/semiconductor barrier height due to the interface states, the interfacial insulator layer and series resistance. The applied bias voltage drops partially across the interface layer causing the forward current to drop, thus this case has resulted in strong deviation from the ideal I–V characteristics. The values of ideality factor and barrier height have been calculated as 1.537 and 0.763 eV, respectively, from forward bias I–V measurements. The n values obtained from I–V characteristics are higher than unity, and that is attributed to the presence of a thin interfacial insulator layer between the metal and semiconductor. The downward curvature at sufficiently large voltages is caused by the effect of series resistance R_s, apart from the presence of the interface states, which are in equilibrium with the semiconductor. The value of the R_s has been calculated from high voltage region of the structure by using Cheung functions. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots. In summary, in the present study, we conclude that the prepared MIS Schottky diodes have been controlled by the interfacial insulator layer and interface states, which are responsible for the non-ideal behaviour of I–V characteristics.

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