Carrier transport in indium-doped p-channel silicon-on-insulator transistors between 30 and 285 K

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Low-temperature carrier transport is investigated for indium-doped p-channel transistors and compared with that for boron-doped ones. It is shown that, with a doping concentration of 3×10^{17} cm^{-3}, while hopping conduction via acceptor sites predominates in boron-doped transistors, indium-doped ones exhibit strong carrier localization at 30 K. For temperatures between 100 and 285 K, the transport in indium-doped transistors is dominated by thermally activated valence-band conduction, and its activation energy coincides with the indium ionization energy. © *2011 American Institute of Physics*. [doi:10.1063/1.3605546]

I. INTRODUCTION

Dopant-related carrier transport in metal-oxide-semiconductor field-effect transistors (MOSFETs) has been extensively studied both from the view points of transistor technology[1–8] and basic physics.[9–18] Recently, this research field has been reactivated, mostly with the final goal of charge and/or spin control using individual dopants in MOSFET channels.[19–30] However, the research has concentrated on shallow dopants, such as phosphorus and boron. There have been very few studies on deeper dopants, and none have been reported for low-temperature transport of indium-doped MOSFETs.

Indium is a group-III element and acts as an acceptor in silicon. Because indium has a much larger ionization energy E_I ($\sim$ 160 meV) (Refs. 31 and 32) than other group-III elements with a lighter mass (boron, aluminum, and gallium), it is expected to possess distinguishable physical properties, such as longer charge trap retention, better photovoltaic efficiency,[33] and a faster electron-hole recombination rate via radiative processes.[34] These properties are beneficial and promising for future silicon-based quantum nanoelectronics.

The aim of this paper is to investigate the basic transport characteristics of indium-doped MOSFETs at temperatures between 30 and 285 K. We made a comparative study with boron-doped MOSFETs in order to clarify the difference of indium-doped ones from those with shallow acceptors. The present focus is buried-channel[1–3] pMOSFETs, i.e., p-channel MOSFETs with p-type channel dopants. Since, in this type of MOSFET, the Fermi level E_F of the channel lies at around the valence bandedge, the transport characteristics are influenced by dopant-related phenomena, such as carrier freeze out and hopping (or tunneling via dopant sites).[35]

In this paper, we will show that, with a doping concentration of 3×10^{17} cm^{-3}, while the hopping process predominates in boron-doped MOSFETs, indium-doped MOSFETs exhibit a strong carrier localization at 30 K, and the transport is dominated by thermally activated valence-band conduction at temperatures higher than $\sim$ 100 K. The activation energy is found to coincide with the indium ionization energy, and we will point out that this coincidence arises from the field effect in the MOS configuration, which is not seen in uncompensated bulk silicon.

II. DEVICE STRUCTURE, FABRICATION PROCESS, AND MEASUREMENTS

The MOSFETs were fabricated on (100) silicon-on-insulator (SOI) wafers. SOI is now recognized as an important structure not only for advanced Si devices but also for a basic understanding of transport[36] in Si owing to its useful dual (front and back) gates, each of which can work equivalently. The type of SOI used was "SIMOX" (separation-by-implanted oxygen),[37] which was made from boron-doped Si wafers with a doping concentration on the order of 10^{14} cm^{-3}. The wafers underwent a thermal process at 1350 °C for buried-oxide formation. This high-temperature process improves the flatness of the back interface dramatically.[38]

The device fabrication started with mesa etching of the SOI layer by reactive ion etching (Fig. 1). This was followed by thermal oxidation to form a 35-nm-thick oxide for an implantation mask. Indium or boron ions were then implanted. The implantation energies and the dose were 110 keV (the projected range $R_p = 51$ nm) for indium and 16 keV ($R_p = 49$ nm) for boron. The implantation dose was 2×10^{13} cm^{-2} for both indium and boron. Thermal activation was carried out at 900 °C for 5 min in dry N_2. This was followed by deposition of a 55-nm-thick additional oxide with TEOS and subsequent annealing at 900 °C for 15 min in dry N_2. The phosphorus-doped n^+ poly-Si gate was then defined. The source/drain implantation was done with boron using the poly-Si gate as a mask, which was followed by activation at 900 °C for 15 min in dry N_2. Note that we also made n^+ contacts, [see Fig. 1(a)], but these terminals were not used for the present study and were grounded in all measurements.

In the resultant devices, the 48-nm-thick SOI layer is separated from the front and back gates by 90-nm-thick gate oxide and 380-nm-thick buried oxide, respectively. The final

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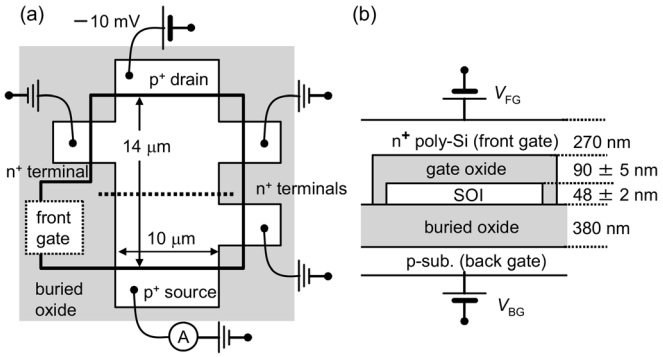

FIG. 1. Schematic top (a) and cross-sectional (b) views of the device. The horizontal dotted line in (a) indicates the location of the cross section of (b).

doping concentration N_A, estimated using Eq. (1) in Ref. 14, was 3×10^{17} cm^{-3}, for both indium and boron, which corresponds to 1.4×10^{12} cm^{-2} for 48-nm-thick SOI. We should note that significant dose loss ($\sim$ 90%) was observed for both indium and boron, the major cause of which might be the diffusion of dopants through the oxide.

Two-terminal conductance measurements were performed at temperature T between 30 and 285 K with source/drain voltage V_{SD} at – 10 mV and with a zero magnetic field. The conductance G, which is I_{SD}/V_{SD} with I_{SD} of source/drain current was recorded as a function of front-gate voltage V_{FG} and back gate voltage V_{BG}. Note that the data obtained are reproducible and showed no significant difference among several measured devices for both boron- and indium-doped MOSFETs.

III. RESULTS AND DISCUSSION

Before showing the measurement data, we first overview possible conduction mechanisms because the conductance characteristics depend on the gate bias conditions and are complicated. Figure 2 shows a schematic illustration of the band diagrams around the valence bandedge at a certain low temperature.

Figure 2(a) shows the situation for the flat-band condition. The present MOSFETs consist of a p-type substrate and an n^+ poly-Si gate. Thus, the flatband conditions are given by $V_{BG} = 0$ V and $V_{FG} = V_{FB}$, where V_{FB} is the flatband voltage between the n^+ poly-Si gate and p-type channel. For a low temperature, $kT \ll E_I$, where k is the Boltzmann constant, E_F (dashed line in the figure) is located somewhere between the valence bandedge and acceptor level. We have two competing conduction mechanisms: the band conduction by valence band holes and the hopping conduction by holes at the acceptor sites. When the temperature is low, most of the holes are at the acceptor sites and the conductance of the band conduction is small. The conductance of the hopping conduction, on the other hand, can be large and depends on the doping concentration and the Bohr radius of the dopant charges. If they are high enough, hopping conduction is observable. For either case, hopping or band conduction, the current flows in the entire SOI layer, which we call the volume conduction or buried-channel conduction, and increases as the temperature rises.

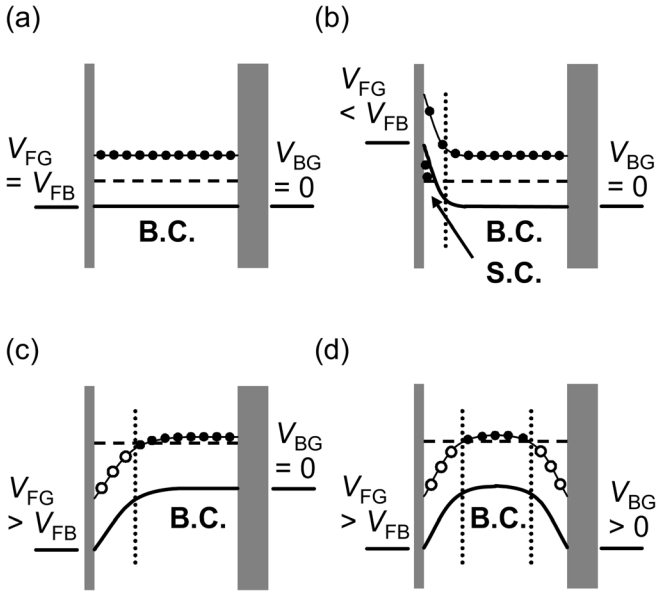

FIG. 2. Schematic illustration of the band profile around the valence bandedge for various gate bias conditions at a certain low temperature. The thin and thick vertical lines in gray indicate the front and back gate oxides, respectively. The horizontal thick, thin, and dashed lines are, respectively, the valence bandedge, the acceptor level, and E_F. The closed circles are the holes trapped at the acceptor sites, while the open circles indicate negatively ionized acceptors. B.C. and S.C. denote the buried and surface channel, respectively. In the diagrams, holes in the valence band are not drawn because of their low density at low temperatures.

Figure 2(b) shows the situation when a negative voltage is applied to the front gate. The band bends at the front interface and a strong accumulation takes place there. The conductance is dominated by this surface channel. On the other hand, a positive bias to the front gate results in the formation of a depletion layer at the front interface side as shown in Fig. 2(c). The number of the acceptor negative charges is equal to that of the positive charges induced by the gate, and the electrical flux from the gate is shielded by this depletion layer. The buried channel remains at the back interface side. As shown in Fig. 2(d), when we additionally apply a positive bias to the back gate, the conduction area is restricted to a central area of the SOI, and the channel is literally *buried*.

A. Boron-doped MOSFETs

Figure 3(a) shows a gray-scale plot of G in the $V_{FG} - V_{BG}$ plane measured at 30 K. In the figure, the gray scale is cycled twice so that the surface channel subthreshold region becomes the brightest and the contour lines inside the buried-channel region become visible. Note first that the conductance characteristics are symmetric with respect to V_{FG} and V_{BG} with voltage scaling factor $\alpha \approx 4$, which is the ratio (C_F/C_B) of the front- to back-gate capacitances or the ratio of the back- to front-gate oxide thicknesses (380 and 90 nm, respectively).

The band profile for points A – D in the figure corresponds to (a)–(d) in Fig. 2. When both V_{FG} and V_{BG} are positively large, the MOSFET is in its off-state (black region in the figure). When either V_{FG} or V_{BG} varies in the negative voltage direction, the buried channel first opens unless either

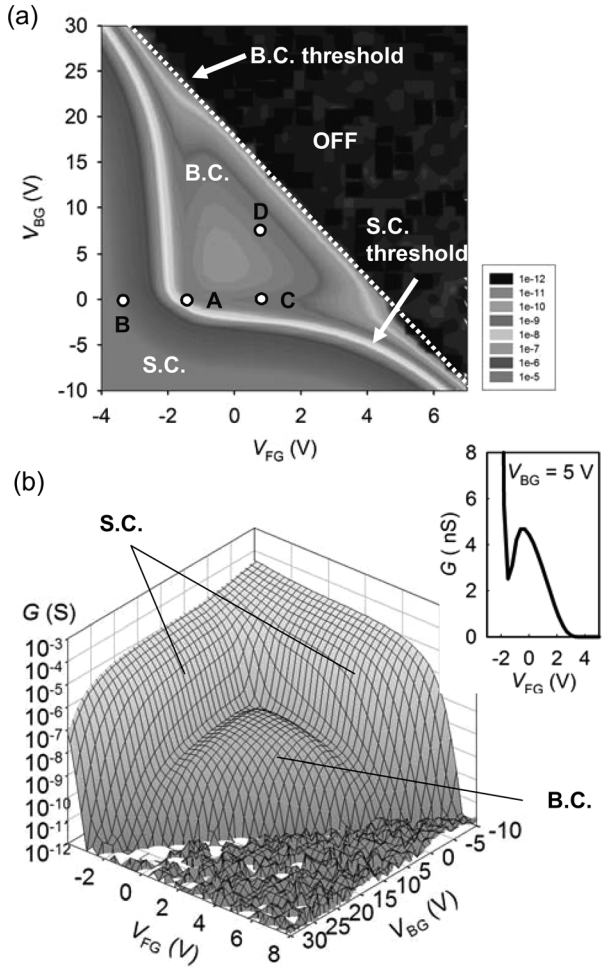

FIG. 3. Gray scale (a) and 3D (b) plots of the conductance of a boron-doped MOSFET measured at 30 K. B.C. and S.C. denote the buried and surface channel, respectively. In (a), the white dotted line is a guide for the eye of the buried-channel threshold line. Points A–D correspond to the bias condition described in Figs. 2(a)–2(d), respectively. Inset in (b) is the $G - V_{FG}$ curve for $V_{BG} = 5$ V.

V_{FG} or V_{BG} is extremely large. A further decrease of V_{FG} or V_{BG} results in the opening of the surface channel. A noticeable difference between the buried and surface channels is the shape of the threshold line. The line is straight and its slope is α (≈ 4) for the buried channel, while it is bent for the surface channel. The line for the surface channel is bent because the number of ionized acceptors varies depending on the gate bias conditions.[1–3,14,17,21] This bending therefore confirms that acceptors are incorporated inside the SOI layer and their charge states can be controlled by the gates. On the other hand, the line of the buried-channel threshold is straight because nearly all acceptors are ionized and thus the number of ionized charges is kept constant on this threshold line.

Figure 3(b) is a three-dimensional (3D) plot of Fig. 3(a). Inset of Fig. 3(b) picks up $G - V_{FG}$ curve at $V_{BG} = 5$ V. As one can see in these figures, the buried-channel component exhibits negative differential conductance (NDC). This typical feature appears when the conductance reflects the density of states around the impurity band of the dopants.[9,10,17] Therefore, this is strong evidence that the buried-channel component is dominated by hopping (or tunneling) via boron sites, as we have observed in phosphorus-doped n-channel MOSFETs with similar doping concentrations.[17]

B. Indium-doped MOSFETs

Figure 4 shows the gray-scale and 3D plots of G in the $V_{FG} - V_{BG}$ plane measured at 30 K. One can see that the surface channel threshold line is bent as in the case of boron, confirming that the indium atoms work as acceptors. The buried-channel conduction is not discernable, indicating that the hopping rate is quite low and the indium charges are localized. The hopping probability P is proportional to $\exp(-2d/a)$, where $d = N_A^{-1/3}$ is the mean separation between dopants and a is the characteristic decay length of the acceptor charge wave-function.[35] Since a is given by $(h/2\pi)/(2mE_I)^{1/2}$, where m and h are the hole mass and Plank constant, we expect that a large E_I for indium results in a significant reduction of P. It is the light hole that governs the decay length, and using the light hole mass, a comes to 1 nm for indium with $E_I = 155$ meV.[32] This is about half of the value for boron. The ratio of P of indium to that of boron, P(indium)/P(boron), is then given by $\exp[-2d(a(\text{indium})^{-1} - -a(\text{boron})^{-1})]$. Using the light hole mass, which gives us the upper bound of P(indium)/P(boron),

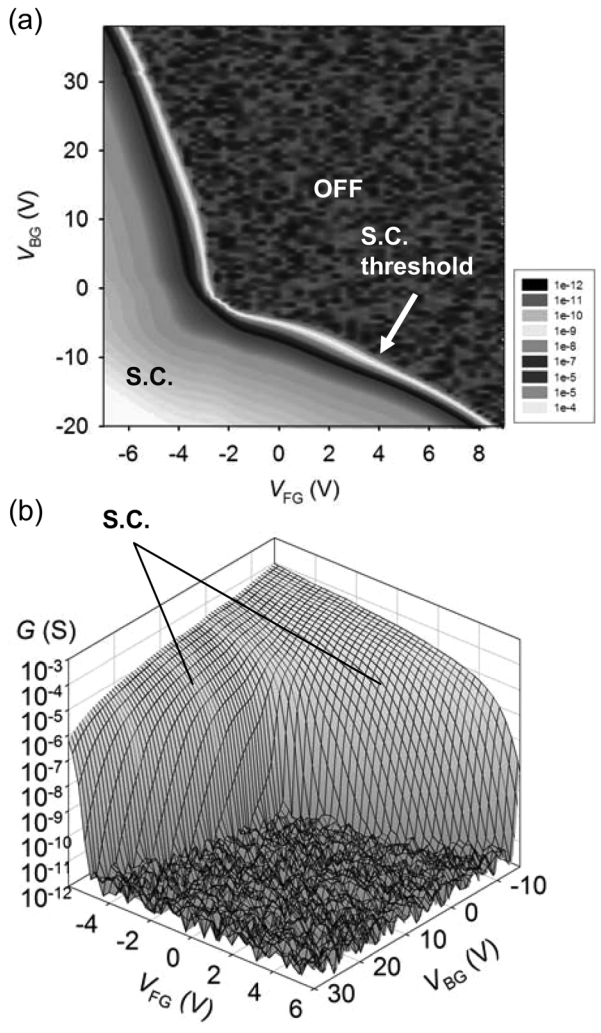

FIG. 4. Gray scale (a) and 3D (b) plots of the conductance of an indium-doped MOSFET measured at 30 K. S.C. denotes the surface channel.

P (indium)P(boron) is estimated to be 10^{-5} for the present $N_A = 3 \times 10^{17}$ cm^{-3}. Such a small value of P(indium)/P(boron) explains the absence of hopping conduction in indium-doped MOSFETs.

Buried-channel conduction was measurable only when the temperature was raised. Figure 5 shows G measured at $T = 130$ K as a function of V_{FG} and V_{BG}. A hump appears in the buried-channel region, but no NDC was observed, suggesting that the conduction mechanism is different from that in the boron-doped case.

For a more detailed analysis, we investigated the temperature dependence of the conductance. Figure 6(a) shows $G - V_{FG}$ curves at $V_{BG} = 0$ V for $T = 80$–285 K. The data can be divided into four regions. For $V_{FG} \gtrsim 4$V, the conductance rises sharply. This is the subthreshold region of the buried-channel. The region between -1.6 and 4 V corresponds to the buried channel. Then, followed by a narrow transition region between $-2.6 \lesssim V_{FG} \lesssim -1.6$ V, the surface channel component predominates in the conductance. Figure 6(b) shows an Arrhenius plot of the conductance for various V_{FG}'s, where V_{FG} is changed in 0.2–V step. From this graph, the activation energy was evaluated, and it is plotted in Fig. 6(c).

Looking at Fig. 6(b), the Arrhenius plot for each V_{FG}'s is nearly straight for $V_{FG} \gtrsim -1.6$ V. This indicates that the activation energy can be defined for each V_{FG} in the buried channel and in its subthreshold regions. As one can see in Fig. 6(c), the activation energy decreased as V_{FG} decreased and it converges to 155 meV, which is the indium ionization energy.[32] This behavior can be explained as follows. When V_{FG} is positively high, E_F is far above the acceptor level and the conduction relies on a minute number of holes thermally activated to the valence band. When V_{FG} decreases and reaches the acceptor level, E_F is *pinned* at this level, and the pinning continues until all the indium sites are filled with holes. This simple picture is valid as long as the temperature dependence of the mobility is weak, and, according to a previous report,[32] it indeed holds true for indium-doped bulk silicon samples.

After all the acceptors are filled with holes, the slope again starts to change in Fig. 6(b). In other words, E_F starts to move down toward the valence bandedge. The region $-2.6 \lesssim V_{FG} \lesssim -1.6$ V can be regarded as a transition region

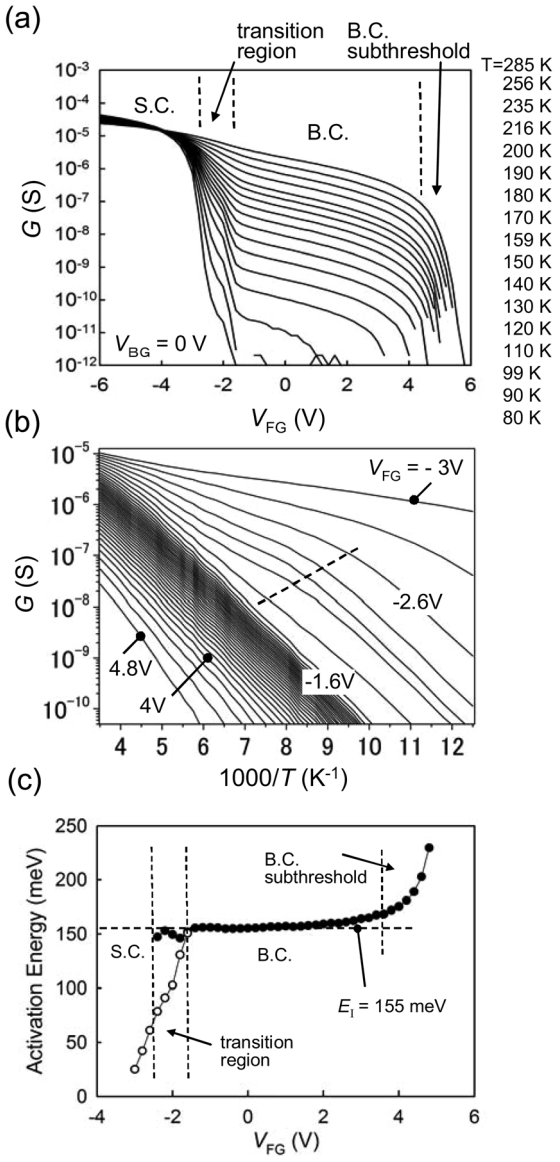

FIG. 6. Temperature dependence of $G - V_{FG}$ curves for $V_{BG} = 0$ V (a), Arrhenius plot (b), and the activation energy (c). B.C. and S.C. denote the buried and surface channel, respectively. In (c), the closed circles show the activation energy for the buried channel and the open circles show that of the surface channel.

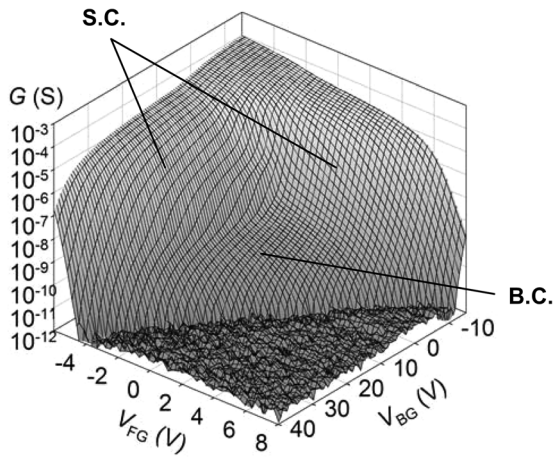

FIG. 5. 3D plot of the conductance of an indium-doped MOSFET measured at 130 K. B.C. and S.C. denote the buried and surface channel, respectively.

from the buried channel to the surface channel. In this region, each Arrhenius curve comprises two slopes. The one on the high-temperature side changes with V_{FG}, while the one on the low-temperature side stays nearly constant at around the indium ionization energy. In Fig. 6(b), these two regions are separated by a dashed line, and both activation energies are plotted in Fig. 6(c). For the lowest part of $V_{FG} < -2.6$ V, the surface channel predominates and the Arrhenius curves becomes straight again.

Figures 4–6 demonstrate that indium acceptors in the MOSFET channel work as strong carrier traps at 30 K and that the buried-channel conduction is dominated by holes excited to the valence band. The activation energy for this excitation was found to be close to the ionization energy of the indium acceptors. We emphasize here that this pinning of E_F at the indium energy level is not trivial. This is because

such pinning does not occur in uncompensated bulk silicon. In a bulk sample with no gates, E_F is governed by the charge neutrality requirement as

$$p + N_D^+ = N_A^-, \tag{1}$$

where p, N_D^+, and N_A^- are the densities of valence band holes, ionized donors, and acceptors, respectively. When $N_D^+ = 0$, Eq. (1) comes to $p = N_A^-$, resulting in $E_F \approx E_I/2$ (not $\approx E_I$) for $kT \ll E_I$. The E_F pinning at E_I happens only when sufficiently large numbers of positive charges ($p \ll N_D^+$) are present. Acceptor negative charges are then balanced to those positive charges so that $N_D^+ = N_A^-$, which results in $E_F \approx E_I$. In a MOSFET channel, it is the gate-induced positive charges that balance to the indium negative charges. In other words, the pinning of E_F is due to the *field effect* by the gates and thus is a unique feature of doped semiconductors in the MOS configuration. The charge neutrality condition is now given by

$$p + [C_F(V_{FG} - V_{FB}) + C_B V_{BG}] = N_A^-. \tag{2}$$

One can see from this equation that when we set $V_{BG} = 0$ V, $p = N_A^-$ holds only when $V_{FG} = V_{FB}$, that is, in the flatband conditions. This is why $E_F = E_I/2$ ($\simeq 80$ meV) is seen only in a limited range of V_{FG} (on the high-temperature side of the transition region) in Figs. 6(b) and 6(c). For positive gate voltages, positive charges generated by the gates induce negative indium charges in the depletion layer, and at the same time, E_F reaches E_I in the buried-channel region. Note that we indeed confirmed this pinning effect by a self-consistent calculation of the electrical potential and charges (data not shown).

We finally mention a kink, or a sudden increase of conductance, observed in the transition region for T lower than 140 K [Fig. 6(a)]. We do not understand the origin of this kink at present, but charge trap centers in the interface region may play an important role. In the buried-channel conditions with positive gate voltages [Figs. 2(c) and 2(d)], such charge trap centers may be ionized, causing remote impurity scattering[39,40] to the valence band holes in the buried channel. Assuming that those trap centers have energy levels near the bandedge as in the case of ordinary interface traps,[41,42] such remote charges would disappear just before the surface channel opens. This would result in an increase in the conductance level though, clarifying this point remains as a future work.

IV. CONCLUSIONS

Low-temperature carrier transport was investigated for p-channel MOSFETs doped with indium and boron, with the aim of clarifying the conduction mechanisms of deep-acceptor (indium)-doped transistors. With a doping concentration of 3×10^{17} cm^{-3}, while hopping conduction via acceptor sites predominates in boron-doped MOSFETs, indium-doped ones exhibit strong carrier localization, and the transport is dominated by thermally activated valence-band conduction with activation energy close to the indium ionization energy.

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