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# The evaluation of the current–voltage and capacitance–voltage-frequency measurements of Yb/*p*-Si Schottky diodes with a high zero-bias barrier height

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**Abstract**
The rare-earth metal Yb (Ytterbium) which has a very low work function of 2.60 eV has been shown to high quality Schottky contacts to *p*-Si. Two distinct linear regions in the semi-logarithmic current density–voltage plot are observed for Yb/*p*-Si Schottky diodes. From the linear regions, the very high zero-bias barrier height values are determined as 0.83 and 0.88 eV. The value of rectification ratio is in order of ~ $10^6$ which is close to the commercial Schottky diodes. From Cheung functions, the value of series resistance is found to be 12.60 Ω. Furthermore, the important contact parameters of the diodes are calculated by using modified Norde method. The contact parameters obtained from reverse bias capacitance–voltage-frequency measurements do not show an important dependence on frequency. The calculated values of acceptor concentration are in close agreement with the value of doping concentration of the *p*-Si wafer used in this study.

**Keywords** High barrier height · Silicon · Schottky diodes · Rare Earth metals · Electrical properties

## 1 Introduction

The studies on Schottky diodes still attract attention since the first published paper on an asymmetrical nature of conduction between metal wires and various metal sulfides in 1874 [1, 2]. Their variety of applications in electronics industry encouraged many researchers to understand, improve and control of metal–semiconductor interfaces. The fast recovery time and low voltage drop on forward bias of Schottky diodes make them preferred diode type in a number of applications such as switching, mixing, RF electronics, power detection and microwave network circuits [3, 4]. Besides aforementioned applications, Schottky contacts are employed for conversion of the sun's energy into electricity and detection of the light [5–7].

The large reverse leakage current density and reverse voltage dependence of reverse current are of the main disadvantages of Schottky diodes [8, 9]. Owing to these drawbacks, Schottky diodes do not prefer in peak detection circuit and reverse voltage polarity protection. Researchers propose some ways to improve the large reverse current. The junction barrier diode structure, which includes a Schottky barrier with pn junction is proposed to eliminate above handicaps [10, 11]. Besides this, the deposition or growth of an insulating layer between the metal and semiconductor is one of suggestion to overcome the large reverse leakage current density problem [12]. The ways mentioned above include a structural changing of Schottky diodes. Another way which does not require the structural changing chooses metal with appropriate work function. According to Schottky–Mott theory [13], the contact between a metal with a high work function and an *n*-type semiconductor gives a high zero-bias Schottky barrier height which provides a small reverse leakage current density while the contact between a metal with a low work function and a *p*-type semiconductor gives the high zero-bias Schottky barrier height. However, these predictions are in need of experimental results.

The zero-bias Schottky barrier height are given within the 0.40–0.73 eV for *p*-Si in the literature [14–21], whereas the values of zero-bias Schottky barrier height for metal/*n*-Si Schottky diodes have been reported up to 0.92 eV [22]. Hence, the Schottky barrier formation of

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metal/*p*-Si with a high zero-bias barrier height is still a scientific challenge. The rare-earths metals such as Y, Gd, Tb, Er and Yb with an extremely small work function [23, 24] have a potential for the high zero Schottky barrier height to *p*-Si. Among them, Yb has a very small work function of 2.60 eV [24] and a contact between Yb and *p*-Si can yield a high zero-bias Schottky barrier height. Yb can also be evaporated, thermally. In spite of the potential, few studies have been reported about Yb/*p*-Si and $YbSi_2$/*p*-Si Schottky diodes [19–25]. In some studies, an insulator layer between metal and semiconductor has been used for increasing the zero-bias barrier height. Recently, the zero-bias barrier height value of 0.89 eV has been reported for Al/YMOO/*p*-Si structure [26]. Çağlar et al. [27] have obtained a value of 0.87 eV for Al/$SnO_2$/*p*-Si diodes. Al/pure $ZrO_2$/*p*-Si Schottky diodes exhibits a very high zero-bias barrier height value of 1.05 eV [28]. Unfortunately, the using an interfacial layer gives rise to an ideality factor greater than unity.

Our goal is to fabricate Schottky diodes with a high barrier height and small leakage current density and also provide an understanding of Yb/*p*-Si Schottky contacts. For this purpose, current density–voltage (*J–V*) and capacitance–voltage-frequency (*C–V–f*) measurements of Yb/*p*-Si Schottky diodes presented in this study have been taken at room temperature and analyzed by using well-known methods.

## 2 Experimental procedure

In this study, the [100] oriented *p*-type Si semiconductor substrate with 1 Ω·cm resistivity was used. This substrate was conventionally subjected to wet chemical cleaning procedure to remove organic, inorganic impurities and oxide layer from the surface. This cleaning process was performed in three stages. In the first stage, the *p*-Si semiconductor substrate was first boiled in acetone at 70 °C for 10 min and then held in methanol for 5 min. In the second step, it was boiled in $NH_4OH + H_2O_2 + 5H_2O$ (1:1:5) for 10 min at 70 °C and $HCl + H_2O_2 + 5H_2O$ (1:1:5) at 70 °C for 10 min. In the last stage, it was kept in 2% aqueous HF solution for 2 min to remove oxide layer on the surface of Si. Al was evaporated to back surface of cleaned *p*-Si substrate. This structure was annealed in $N_2$ atmosphere at 575 °C for 3 min, and so, the ohmic contact was obtained. The mask which had dots with a 1.5 mm diameter was placed on the front surface of the *p*-Si. Then, Yb was thermally evaporated by using a tantalum boat. Thus, the manufacture of Yb/*p*-Si/Al Schottky diodes was completed.

Current–voltage (*I–V*) and capacitance–voltage-frequency (*C–V–f*) measurements of the diodes are taken in dark and at room temperature. *I-V* data of these diodes were taken with Keithley 2400 SourceMeter at ±2 V range while the *C–V–f* data of these diodes were measured with 4192A LF impedance analyzer in the frequency range of 1 kHz–3 MHz.

## 3 Results and discussion

### 3.1 Analysis of current–voltage characteristic of Yb/p-Si Schottky diodes

In metal semiconductor contacts, the current carriers can exceed the potential barrier at the metal/semiconductor interface due to their thermal energies. Thus, these carriers can move easily from metal to semiconductor or from semiconductor to metal. This situation is examined by the thermionic emission (TE) theory. This theory predicts the relation between the *J* and *V* as in the following equation [29]:

$$J = J_o \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(-\frac{q(V - IR_s)}{nkT}\right)\right] \quad (1a)$$

$$J_o = A^* T^2 \exp\left(-\frac{q\Phi_{bo}}{kT}\right) \quad (1b)$$

Here, $A^*$ is the effective Richardson constant and its value for *p*-Si is 32 A $cm^{-2}$ $K^{-2}$ for *p*-Si [29]. The value of saturation current density ($J_o$) can be found from the part of straight-line intercept of semi-logarithmic *J–V* characteristic at zero-bias. $\Phi_{bo}$ denotes the zero-bias barrier height. The value of ideality factor ($n$) for a metal–semiconductor contacts can be calculated from the slope of linear part of semi-logarithmic *J–V* characteristic and also can be given as [29]:

$$n = \frac{q}{kT}\frac{dV}{d(\ln(J))} \quad (2)$$

The value of $\Phi_{bo}$ can be calculated by the following equation:

$$\Phi_{bo} = \frac{kT}{q}\ln\left(\frac{A^* T^2}{J_o}\right) \quad (3)$$

The forward and reverse bias semi-logarithmic *J-V* characteristics of the Yb/*p*-Si Schottky diodes are given in Fig. 1. The semi-logarithmic *J-V* characteristics of the Yb/*p*-Si Schottky diodes have two linear regions in the wide current density range. The first linear region (region I) is between 0.14 V and 0.26 V, the second linear region (region II) is between 0.28 V and 0.52 V. The forward bias *J–V* curve shows a bending after about 0.56 V. This situation can be attributed to the presence of $R_s$ which limits the flow of current [29–31]. The power dissipation is an important

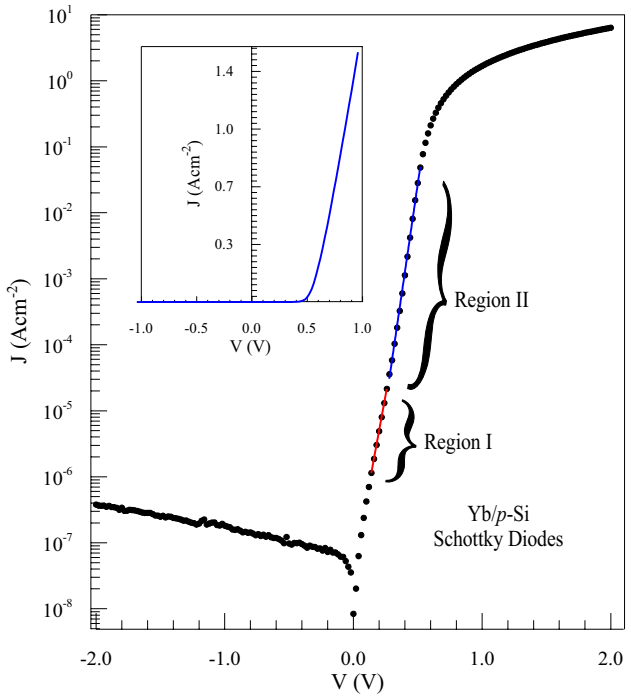


**Fig. 1** The semi-logarithmic *J–V* characteristics of the Yb/*p*-Si Schottky diodes at room temperature

parameter for Schottky barrier diodes and depends on forward voltage drop, series resistance and reverse leakage current density. To minimize the power dissipation and provide a better device performance, the voltage drop on forward bias and reverse leakage current density are desirable to be as low as possible. The Schottky barrier plays an important role in this state. The use of metal forming a low barrier in metal semiconductor contacts provides the advantage of a low voltage drop on forward bias. However, the leakage current density increases strongly, and this is not suitable for high temperature operation at Schottky barrier diodes. On the contrary, the use of metal forming a high barrier causes low leakage current densities and high voltage drop on the forward bias [32]. As is known, a pn silicon diode is voltage drop on forward bias between 0.6 and 0.7 V while the Schottky diode has voltage drop on forward bias between 0.15 and 0.45 V [33]. The voltage drop on forward bias for the Yb/*p*-Si Schottky diodes was found to be approximately 0.52 V (see Fig. 1). This value is slightly higher than expected. However, it is observed that our diodes have a high barrier height and a low leakage current density.

As is known, the most important features of a quality Schottky barrier diode in terms of performance and reliability are a high barrier height, a low leakage current density, and a good rectification ratio ($RR = J_{forward}/J_{reverse}$). The value of *RR* was obtained as $9.24 \times 10^6$ (at $\pm 1$ V) for Yb/*p*-Si Schottky diodes. The value of leakage current density was

**Table 1** Some electrical parameters obtained from the semi-logarithmic *J–V* characteristics for Yb/*p*-Si Schottky diodes

| Region | Voltage range (V) | $n$ | $\Phi_{bo}$ (eV) | $J_o$ (A cm$^{-2}$) |
|---|---|---|---|---|
| I | 0.14 ~ 0.26 | 1.58 | 0.83 | $3.75 \times 10^{-8}$ |
| II | 0.28 ~ 0.52 | 1.26 | 0.88 | $5.51 \times 10^{-9}$ |

found as $3.80 \times 10^{-7}$ A cm$^{-2}$ (at $-2$ V). When some studies in the literature were examined, it was seen that the value of leakage current density for metal/semiconductor contacts made by using different metals on *p*-Si wafer is about the order of $10^{-4}$ A cm$^{-2}$ [34–36] and the value of the *RR* was observed about the order of $10^3$ [37, 38]. These results show that the Yb/*p*-Si Schottky diodes have a good *RR* and a low leakage current density with compared to diodes presented in the literature. Some electrical parameters such as $n$, $\Phi_{bo}$ and $J_o$ obtained from the *J-V* characteristic (for linear two regions) for Yb/*p*-Si diodes are given in Table 1. The values of $n$ are greater than unity ($n = 1$) [29] for I and II regions. This case can be generally attributed to the inhomogeneous barrier height, the dependence of the barrier height to the applied voltage, the effect of the image force, the generation-recombination of charges at interfacial layer and the presence of a possible tunneling mechanism [29, 30].

An oxide interfacial layer with a thickness of 10 Å is naturally occur on the surface even if chemical cleaning is performed on the semiconductor surface. The presence of such a layer may cause the values of $n$ to be higher than the unity. In the low forward bias currents, if the Schottky barrier height is greater than half of the semiconductor bandgap, the density of the minority carriers is high in the regions close to the metal. In this case, some of the minority carriers can diffuse into the neutral region of the semiconductor and so an injection of minority carriers realize. Thus, deviations from the ideal case can occur and the value of $n$ can be obtained higher than unity. The value of $\Phi_{bo}$ in the region II is higher than the region I, but the value of $n$ is lower (Table 1). In this case, it can be said that the increase in the $\Phi_{bo}$ in the high forward bias regions causes the injection of the minority carriers to be reduced, and so the diode approach the ideal situation [29, 39].

The value of $\Phi_{bo}$ was found as higher than barrier height value of some metal/*p*-Si contacts in the literature (Table 2) [14, 16–20, 40, 41]. This is due to the fact that when a metal and semiconductor contact is made, the contact potential is related to the work function of the metal ($\phi_m$) and the semiconductor ($\phi_s$) [24, 42, 43]. It is known that the metal semiconductor contacts produced by using *p*-type semiconductor are expected to use metal with low work function for best device performance (Table 1). Here, it is seen that the rare-earth metal Yb is a suitable metal to produce a Schottky diode with a high barrier height. The calculated

**Table 2** Experimental zero-bias barrier height values reported for metal/*p*-Si Schottky diodes

| Metal | $\phi_m$ (eV) [24, 42] | Pauling electronegativity [43] | $\Phi_{bo}$ (eV) |
|---|---|---|---|
| Yb | 2.60 | 1.10 | 0.64 [19] |
| Tb | 3.00 | 1.20 | 0.63 [19] |
| Y | 3.10 | 1.22 | 0.68 [19] |
| Er | 3.12 | 1.24 | 0.68 [19] |
| Zr | 4.05 | 1.33 | 0.58 [41] |
| Ga | 4.20 | 1.81 | 0.63 (at 301 K) [20] |
| Ga | 4.20 | 1.81 | 0.76 (at 305 K) [20] |
| Cd | 4.22 | 1.69 | 0.73 [17] |
| Pb | 4.25 | 2.33 | 0.56 [14] |
| Ag | 4.26 | 1.93 | 0.55 [14] |
| Al | 4.28 | 1.61 | 0.58 [14] |
| Ti | 4.33 | 1.54 | 0.69 [18] |
| Sn | 4.42 | 1.96 | 0.70 [16] |
| Cu | 4.65 | 1.90 | 0.46 [14] |
| Au | 5.10 | 2.54 | 0.32 [40] |
| Ni | 5.15 | 1.91 | 0.51 [14] |

barrier height value for our diode is higher than the barrier height value given for Yb/*p*-Si Schottky diodes in Table 2. The Yb/*p*-Si Schottky diodes in Ref. [19] diodes were fabricated on *p*-Si wafer with resistivity of 15 Ω·cm, and the wafer was kept at 100 °C during the deposition of Yb. The acceptor concentration of *p*-Si is lower than the wafer used in our study. Furthermore, e-beam technique was employed for the deposition of Yb. Therefore, the acceptor concentration difference and reaction of Yb with Si can cause the low zero-bias barrier height. Furthermore, the ideality factor is greater than unity for our Yb/*p*-Si Schottky diodes. This case shows the existence of an oxide interfacial layer between Yb and *p*-Si. This layer can reduce the leakage current and increase the zero-bias barrier height.

Mönch has reported that the continuum of metal-induced gap states (MIGS) determines the barrier heights of ideal, i.e., defect-free, intimate, abrupt and homogeneous Schottky contacts [43, 44]. The value of barrier height for metal/*p*-Si Schottky contacts can be estimated by the following equation using a combination of the physical MIGS and the chemical electronegativity theory [15, 43, 45]:

$$\Phi_{bo} = 0.36 - 0.101\left(\mathrm{X}_m - \mathrm{X}_{Si}\right) \tag{4}$$

Here, the $X_m$ and $X_{Si}$ are Miedema electronegativities of metal and Si, respectively. The electronegativities in Miedema unit can be obtained from the following equation [43]:

$$\mathrm{X}_{\mathrm{Mied}} = 1.93 \cdot \mathrm{X}_{\mathrm{Paul}} + 0.87 \tag{5}$$

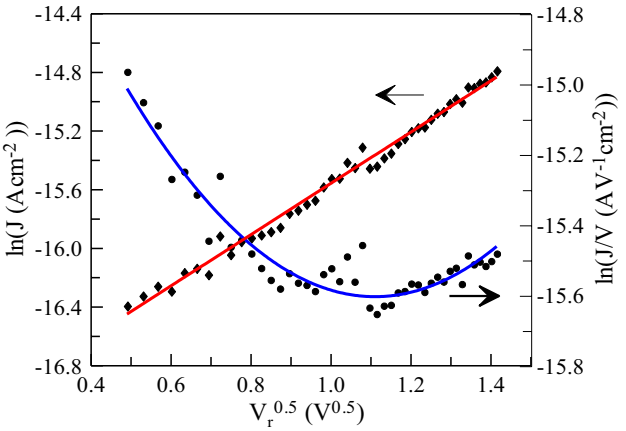


**Fig. 2** Schottky and Poole–Frenkel emissions plots of Yb/*p*-Si Schottky diode under reverse bias. Red fit line is for ln*J* versus $V_r^{0.5}$ plot

Here, the $X_{\mathrm{Paul}}$ is Pauling electronegativity. Pauling electronegativities of Yb and Si are given as 1.10 and 1.90, respectively (Table 2) [43]. The value of $\Phi_{bo}$ was determined as 0.52 eV by using Eqs. 4 and 5 for our diodes. This value is much smaller than the value of $\Phi_{bo}$ calculated by using *J*–*V* characteristic (Table 1). This inconsistency in the two results can be attributed to the interface dipoles, interface structure and interface defects related to the structure [44].

In Fig. 1, the reverse current density rises slowly with increasing applied reverse bias, and does not show any effect of saturation. This behavior can be explained by the existence of an interfacial insulator layer which causes the barrier lowering or the dependence of the barrier height on electric field [46]. Furthermore, the image force lowering of the barrier height can be shown as a reason [29]. The current conduction mechanism under reverse bias ($V_r$) is generally controlled by Schottky emission and Poole–Frenkel emission. While ln*J* is proportional to $V_r^{0.5}$ for Schottky emission, ln*J*/*V* is proportional to $V_r^{0.5}$ for Poole–Frenkel [39]. As can be seen from Fig. 2, the plot of ln*J* vs $V_r^{0.5}$ is linear. Thus, it can be said that the Schottky emission is dominant in current conduction mechanism.

## 3.2 Effects of the series resistance

One of the important parameters affecting the electrical characteristics of metal semiconductor contacts is $R_s$. The presence of $R_s$ can arise from contact of the probe wire to the gate, lack of quality of the ohmic contact, organic impurities, interfacial states and bulk resistance of the semiconductor [30]. The following functions have been proposed by Cheung and Cheung to determine the values of $R_s$, *n* and $\Phi_b$ [31]:

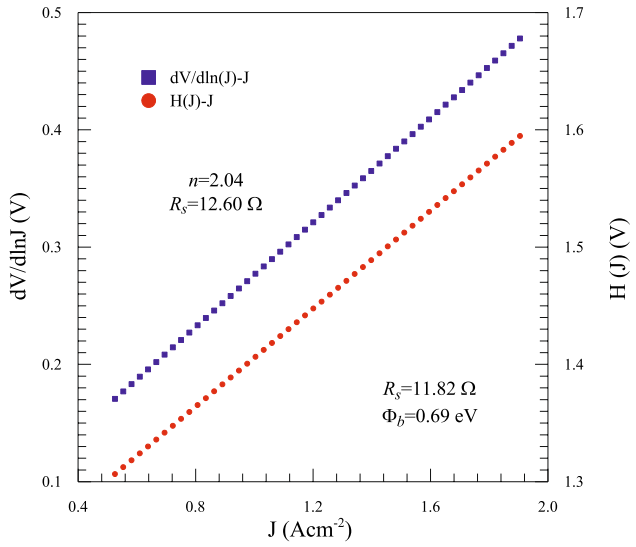


**Fig. 3** The d*V*/dln*J*–*J* and H(*J*)–*J* plots for the Yb/*p*-Si Schottky diodes at room temperature

$$\frac{dV}{d(\ln J)} = \left(\frac{nkT}{q}\right) + JR_s \tag{6}$$

$$H(J) = V - n\frac{kT}{q}\ln\left(\frac{J}{A^*T^2}\right) = n\Phi_b + JR_s \tag{7}$$

The characteristics of d*V*/dln *J*–*J* and H(*J*)–*J* for the Yb/*p*-Si Schottky diodes are given in Fig. 3. The curves show a linear behavior. Here, the value of *n* was calculated as 2.04 from the d*V*/dln *J* curve. The value of $R_s$ was determinate as 12.60 Ω from the slope of d*V*/dln *J* curve. From *H*(*J*)–*J* plot, the value of $\Phi_b$ was calculated as 0.69 eV by using *n* whose value determined from d*V*/dln*J*–*J*plot. The value of $R_s$ was found as 11.82 Ω from the slope of the *H*(*J*) curve. The presence of a high series resistance gives rise to a limitation in the forward bias current and thus high power dissipation occurs. If the series resistance is small, the diode exhibits a characteristic close to ideal case. The low quality of ohmic contact is the main reason of high series resistance. The value of $R_s$ for our Yb/*p*-Si Schottky diodes is small and close to the value of commercially used Schottky diodes. This shows that a low resistivity ohmic contact have been achieved between *p*-Si and Al. The value of *n* obtained from Cheung functions is greater than unity. At the same time, it is seen that the values of *n* are greater than logarithmic *J*-*V* characteristic. However, the values found in the semi-logarithmic *J*-*V* characteristic are obtained from the linear region of the graph. Therefore, the values of *n* obtained for the two methods are different from each other. Another reason for this difference is dependency of *n* on the applied bias voltage [29, 44].

To obtain the values of $\Phi_b$ and $R_s$ can be used the Norde function modified by Bohlin. The modified Norde function is given as follows [47, 48]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{J(V)}{A^*T^2}\right) \tag{8}$$

$$\Phi_b = F(V_{\min}) + \frac{V_{\min}}{\gamma} - \frac{kT}{q} \tag{9}$$

$$R_s = \frac{(\gamma - n)kT}{qJ_{\min}} \tag{10}$$

Here, the value of $\gamma$ should be selected as a number greater than the value of *n* obtained from the semi-logarithmic *J*–*V* characteristic. Two different *n* values were obtained from two different linear regions of semi-logarithmic *J*–*V* characteristic (Table 1). A number greater than the values of *n* was selected ($\gamma = 2$). The characteristic of *F*(*V*)–*V* is plotted and shown in Fig. 4. Both the value of minimum voltage ($V_{\min}$) and the value of minimum current density ($J_{\min}$) corresponding to the minimum value of *F*(*V*) [$F_{\min}(V)$] are obtained from the characteristic of *F*(*V*)–*V*. The values of $R_s$ and $\Phi_b$ were calculated for two different ideality factor values. Obtained electrical parameters from modified Norde functions are presented in Table 3.

It is seen that the values of $R_s$ obtained from modified Norde functions are smaller than the values of $R_s$ obtained from Cheung functions. Cheung and Norde method have

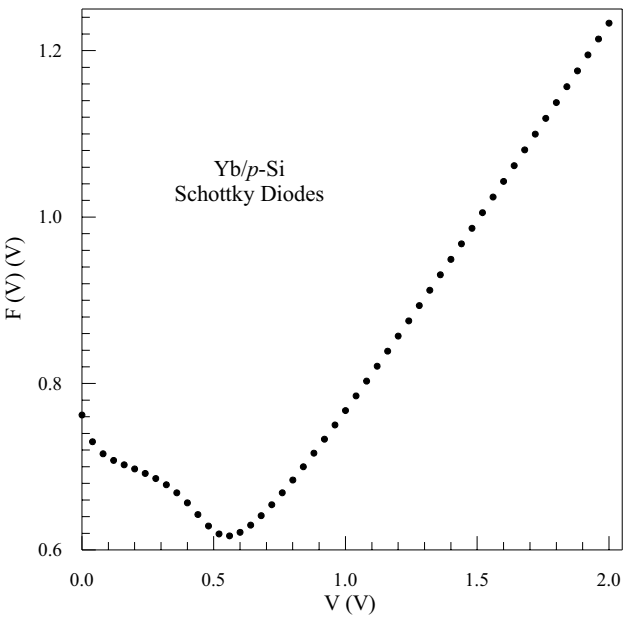


**Fig. 4** The characteristic of *F*(*V*)–*V* for the Yb/*p*-Si Schottky diodes at room temperature

**Table 3** Some electrical parameters obtained from modified Norde functions for the Yb/*p*-Si Schottky diodes

| Region | $F(V_{min})$ (V) | $V_{min}$ (V) | $J_{min}$ (A cm$^{-2}$) | $n$ | $\gamma$ | $R_s$ (Ω) | $\Phi_b$ (eV) |
|---|---|---|---|---|---|---|---|
| I | 0.72 | 0.56 | $1.15\times10^{-1}$ | 1.58 | 2 | 5.36 | 0.79 |
| II | 0.72 | 0.56 | $1.15\times10^{-1}$ | 1.26 | 2 | 9.43 | 0.87 |

advantages and disadvantages according to each other. The main disadvantage of Norde method is difficulty in the determination of the minimum point of the $F(V)$–$V$ plot [31]. The data were used by the Norde method take place in the linear region of the semi-logarithmic $J$-$V$ plot. In this region, the current increase with the applied forward bias, exponentially. So the failure to determine the exact value of $J_{min}$ may cause such a inconsistency [49]. The values of $R_s$ obtained from both modified Norde function and Cheung functions for Yb/*p*-Si Schottky diodes are highly small compared to the values of $R_s$ of some metal/*p*-type semiconductor contacts in the literature [50–53].

### 3.3 C–V–f characteristics of Yb/p-Si Schottky diodes

The depletion layer capacitance of a Schottky diode depend on the applied voltage and the relationship between them can be given by the following equation [30, 39]:

$$C^{-2} = \frac{2\left(V_d + V_r - kT/q\right)}{\varepsilon_s \varepsilon_o N_A} \tag{11}$$

where $C$ is the capacitance per unit area and the diode area is 0.018 cm$^2$. $V_d$ is the diffusion potential, $V_r$ is the applied reverse bias, $N_A$ is the acceptor concentration, $\varepsilon_s$ is the relative dielectric constant of semiconductor (11.7 for Si [54]), $\varepsilon_o$ is the permittivity of free space $kT/q$ is the correction term. This term comes from the effect of the penetration of electrons from the metal to the depletion region. It is known as Debye's tail [55]. As can be seen from above statement, if the acceptor concentration across the barrier area is constant, the graph of $C^{-2}$ versus $V$ is a linear line. Extrapolation of this line to the point of $C^{-2}$=0 gives intercept voltage $V_o$ which is $V_d - kT/q$.

The value of barrier height, $\Phi_b(C\text{–}V)$, can be found with the use of the following equation [39]:

$$\Phi_b(C-V) = V_d + \frac{kT}{q}\ln\frac{N_V}{N_A} \tag{12}$$

where $N_V$ is the effective density of states in Si valance band and its value is $1.04\times10^{19}$ at 300 K [54].

Some fundamental properties of Schottky barrier diodes can be revealed by analysis of its $C$–$V$ characteristic. For this purpose, the $C$–$V$ measurements of the Yb/*p*-Si Schottky diodes were taken between 1 kHz and 3 MHz at room temperature. The measured capacitance is sensitive to bias voltage and frequency. Capacitance per unit area versus voltage

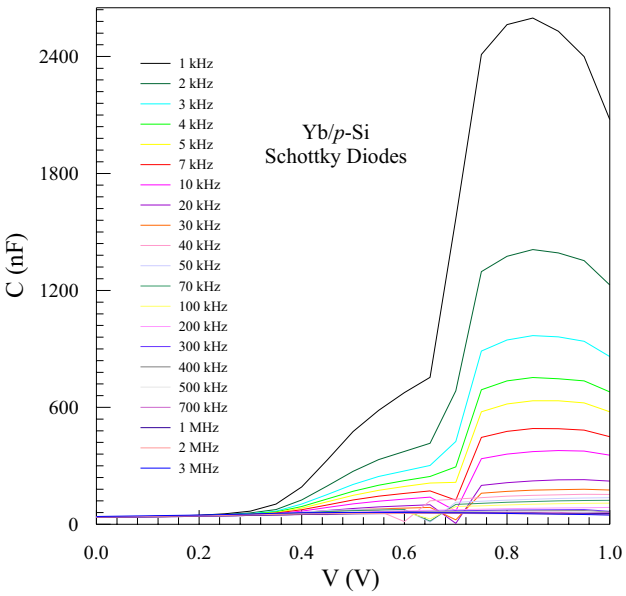


**Fig. 5** The forward $C$–$V$ characteristics of the Yb/*p*-Si Schottky diodes between 1 kHz and 3 MHz at room temperature

characteristics ($C$–$V$) are given in Fig. 5. Each $C$–$V$ curve has three regimes. These are depletion, inversion and accumulation region. Such behavior of $C$ is attributed to the specific distribution of surface/interface states at between the Yb/*p*-Si interfaces. The $C$–$V$ curves give a peak for each frequency. The position of the peaks according to voltage axis changes with applied frequency. The presence of the interface states can be given as a reason for this. The dependency on the applied voltage and frequency is due to the particular features of the metal–semiconductor contacts such as impurity level, high series resistance, doping concentration, interface states and surface polarization. In forward bias region, an increase in capacitance values is observed by decreasing frequency. This situation is generally ascribed to frequency dependence of the capacitance of the interface states. At low frequencies, the interface states can easily follow the AC signal and give a contribution to contact capacitance. The value of this excess capacitance is related to the carrier lifetime ($\tau$) of interface states and the frequency of applied AC signal. If the carrier lifetime is much larger than $1/2\pi f$, the charges at the interface cannot follow applied AC signal and the contribution of interface states to contact capacitance decrease [30, 56, 57]. If the frequency of the applied AC signal is 1 MHz or greater, the interface states cannot contribute to the contact capacitance. In this case, the contact

capacitance is only due to the movement of depletion layer charge of the semiconductor [29, 58, 59]. This phenomenon makes the contribution of interface state capacitance to the contact capacitance considerably smaller [60].

One of the most important parameters affecting the *C–V* characteristic of a Schottky diode is the series resistance. A peak occurs in the forward bias region of the *C–V* characteristic connected to $R_s$. The value of $R_s$ varies with the applied voltage and frequency. Chattopadyay and Raychaudhuri showed that the peak in *C–V* curve is stem from existence of the series resistance and the position of the peak depends on the density of interface states [59]. The peaks observed in *C–V* curves of the Yb/*p*-Si Schottky diodes can be ascribed to the series resistance. Diode parameters can be calculated by using $C^{-2}$–*V* characteristics. The $C^{-2}$–*V* plots were drawn by using values of capacitance per unit area (in Fig. 6). The $C^{-2}$–*V* characteristics along the reverse bias region give linear lines. The slope and intercept voltage of the $C^{-2}$–*V* plot are function of the interface insulator layer and the density of interface states [61–63]. The value of $V_d$ is obtained by means of extrapolation of this linear line to the voltage axis. The values of $N_A$, $\Phi_b$ and $E_F$ are extracted from the reverse bias $C^{-2}$–*V* plots for each frequency, respectively. These values for the Yb/*p*-Si Schottky diodes are given in Table 4. A wide frequency range has been selected to elaborate the frequency dependence of important diode parameters. The contact capacitance is under the influence of ionized acceptors in semiconductor and interface states between metal and semiconductor. At enough high frequency, the charges at the interface cannot follow an external AC signal, the contribution of interface states to the total capacitance can

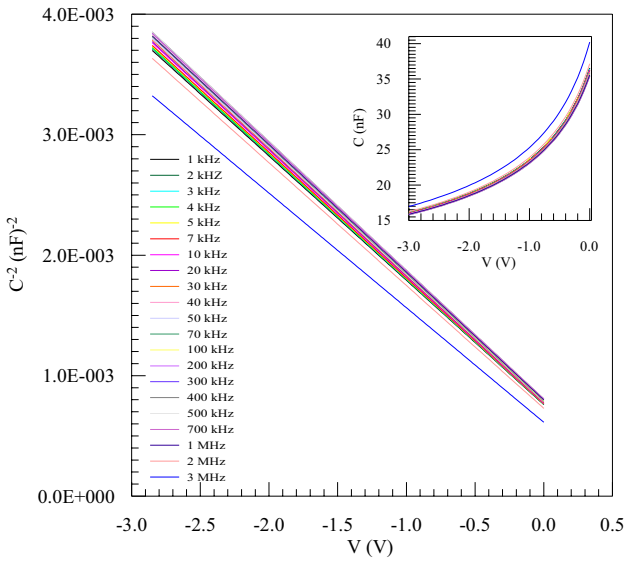


**Fig. 6** The reverse bias $C^{-2}$–*V* characteristics of the of the Yb/*p*-Si Schottky diodes (inset figure, reverse bias *C–V* characteristics of the diodes)

**Table 4** The values of various parameters for the Yb/*p*-Si Schottky diodes determined from $C^{-2}$–*V* characteristics in 1 kHz–3 MHz

| *f* (kHz) | $V_o$ (V) | $V_d$ (V) | $N_A$ ($10^{16}$ cm$^{-3}$) | $E_F$ (eV) | $\Phi_b$ (eV) |
|---|---|---|---|---|---|
| 1 | 0.72 | 0.75 | 1.17 | 0.18 | 0.92 |
| 2 | 0.73 | 0.75 | 1.16 | 0.18 | 0.93 |
| 3 | 0.73 | 0.76 | 1.16 | 0.18 | 0.93 |
| 4 | 0.73 | 0.76 | 1.16 | 0.18 | 0.93 |
| 5 | 0.73 | 0.76 | 1.16 | 0.18 | 0.94 |
| 7 | 0.73 | 0.76 | 1.16 | 0.18 | 0.93 |
| 10 | 0.73 | 0.76 | 1.15 | 0.18 | 0.93 |
| 20 | 0.74 | 0.76 | 1.15 | 0.18 | 0.94 |
| 30 | 0.74 | 0.76 | 1.14 | 0.18 | 0.94 |
| 40 | 0.74 | 0.76 | 1.14 | 0.18 | 0.94 |
| 50 | 0.74 | 0.77 | 1.14 | 0.18 | 0.94 |
| 70 | 0.74 | 0.77 | 1.14 | 0.18 | 0.94 |
| 100 | 0.74 | 0.77 | 1.13 | 0.18 | 0.94 |
| 200 | 0.75 | 0.77 | 1.13 | 0.18 | 0.95 |
| 300 | 0.75 | 0.78 | 1.13 | 0.18 | 0.95 |
| 400 | 0.75 | 0.78 | 1.13 | 0.18 | 0.95 |
| 500 | 0.75 | 0.78 | 1.13 | 0.18 | 0.96 |
| 700 | 0.76 | 0.78 | 1.13 | 0.18 | 0.96 |
| 1000 | 0.75 | 0.78 | 1.14 | 0.18 | 0.95 |
| 2000 | 0.71 | 0.74 | 1.19 | 0.18 | 0.92 |
| 3000 | 0.65 | 0.67 | 1.27 | 0.17 | 0.85 |

be neglected [30, 64–67]. In general, at sufficiently high frequencies, the value of the capacitance is independent of the frequency. For the ideal case, the capacitance is expected to decrease as the applied voltage increases in reverse bias region. The values founded for $N_A$, $V_d$, $E_F$ and $\Phi_b$(*C–V*) are $1.14\times10^{16}$ cm$^{-3}$, 0.78 V, 0.18 eV, 0.95 eV at 1 MHz, respectively. The value of $N_A$ is close to the theoretical value ($1.39\times10^{16}$ cm$^{-3}$) of *p*-Si. Also, $N_A$ does not exhibit frequency dependence. This situation proves that the Yb/*p*-Si Schottky barrier diodes show nearly ideal behavior [68]. The barrier height value of Yb/*p*-Si Schottky diodes calculated by the *J–V* measurements is lower than those obtained by their *C–V* measurements. The different nature of the methods and non-ideal interface between Yb and *p*-Si can be shown as the reason. The origin of the non-ideal interface can be due to the presence of a thin insulating layer or charges at the metal-semiconductor interface and edge leakage current densities [29, 69, 70].

Electrical characteristics of metal semiconductor contacts are affected by the presence of interface states. It is important to examine the distribution profile of the interface states in order to obtain reliable electrical characteristics for the device. The density of the interface states ($D_{it}$) can be obtained by using the measured capacitance values for high frequency and low frequency. The values of $D_{it}$ can be calculated by using the following equation [71, 72]:

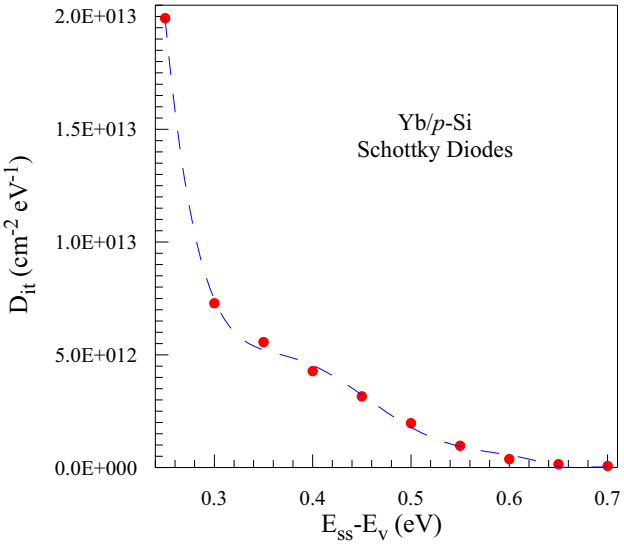


**Fig. 7** The distribution of interfacial states density for Yb/*p*-Si Schottky diodes

$$D_{it} = \frac{1}{qC_{HF}}\sqrt{\frac{q\varepsilon_s N_A}{2\Psi_s}}\left(C_{LF} - C_{HF}\right) \tag{13}$$

where $\Psi_s$ is surface potential ($=V_d$–$V$), $C_{LF}$ is capacitance for low frequency, and $C_{HF}$ is capacitance for high frequency. In a *p*-type semiconductor, the energy of the interface states ($E_{ss}$) with respect to the valance band edge ($E_v$) at the surface of the semiconductor can be determined as [73]:

$$E_{ss} - E_V = q\left(\Phi_b - V\right) \tag{14}$$

In Fig. 7, the energy distribution of the interface states density have been obtained in the energy range of $(0.20 - E_v) - (0.70 - E_v)$ eV. The interface states density ranges from $6.90\times10^{10}$ $eV^{-1}$ $cm^{-2}$ in $(0.70 - E_v)$ eV to $5.05\times10^{13}$ $eV^{-1}cm^{-2}$ in $(0.20 - E_v)$ eV. It can be seen that the density of the interface states increases from mid-gap toward the top of the valance band, exponentially.

## 4 Conclusion

Yb/*p*-Si Schottky diodes have been fabricated by thermal evaporation of Yb on *p*-Si. These diodes have been found to have a good rectification ratio, the high barrier height, and the low leakage current density, which are important for high device performance and reliability. It is seen that *J*-*V* characteristics of the Yb/*p*-Si Schottky diodes show two linear regions. The value of *n* is closer to unity for region II. This situation has been attributed to the reduction of the injection of minority carriers in the high forward bias regions, where the barrier height increases. The forward bias *J*-*V* curve shows a bending after about 0.56 V. It can be attributed to the presence of $R_s$ which gives rise to a limitation in the forward bias current. The value of $R_s$ for our Yb/*p*-Si Schottky diodes has been calculated as highly small from functions of Cheung and modified Norde and close to the value of commercially used Schottky diodes. The values of $N_A$, $V_d$, $E_F$ and $\Phi_b$ for the Yb/*p*-Si Schottky diodes are calculated as $1.14\times10^{16}$ $cm^{-3}$, 0.78 V, 0.18 eV, 0.95 eV at 1 MHz, respectively. The value of $N_A$ was found close to the theoretical value of *p*-Si. This situation proves that the Yb/*p*-Si Schottky barrier diodes show nearly ideal behavior. The barrier height value calculated by the *J*–*V* method is lower than those obtained by the *C*–*V* method. This is attributed to the different nature of the methods used. The interface states density ranges from $6.90\times10^{10}$ $eV^{-1}cm^{-2}$ in $(0.70 - E_v)$ eV to $5.05\times10^{13}$ $eV^{-1}cm^{-2}$ in $(0.20 - E_v)$ eV.

**Table 5** Comparison of the Yb/*p*-Si Schottky diodes and commercial 1N5819

| Parameters | 1N5819 | Yb/*p*-Si |
|---|---|---|
| *n* | 1.03 | 1.58 (Region I) |
| | | 1.26 (Region II) |
| $J_o$ (A $cm^{-2}$) | $5.07\times10^{-5}$ | $3.75\times10^{-8}$ (Region I) |
| | | $5.51\times10^{-9}$ (Region II) |
| *RR* (±1 V) | ~$10^5$ | $9.24\times10^6$ |
| *C* at −2 V, 1 MHz (nF $cm^{-2}$) | ~12.2 | 18.5 |

For the sake of comparison, some electrical parameters of commercial 1N5819 (silicon Schottky barrier rectifier diode) and the Yb/*p*-Si Schottky diodes are summarized in Table 5. Our Yb/*p*-Si Schottky diodes have low saturation current density and higher rectification ratio than 1N5819 Schottky diodes. But, the ideality factor and reverse capacitance at -2 V of our diodes are greater than commercial one. It is clear that Yb is an attractive element for obtaining high quality Schottky diodes which have the high barrier height and the low leakage current density.

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