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Understanding the charge transport mechanisms through ultrathin SiO_x layers in passivated contacts for high-efficiency silicon solar cells

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ABSTRACT

We report on the microscopic structure of the SiO_x layer and the transport mechanism in polycrystalline Si (*poly*-Si) passivated contacts, which enable high-efficiency crystalline Si (*c*-Si) solar cells. Using electron beam induced current (EBIC) measurements, we accurately map nanoscale conduction-enabling pinholes in 2.2 nm thick SiO_x layers in a *poly*-Si/SiO_x/*c*-Si stack. These conduction enabling pinholes appear as bright spots in EBIC maps due to carrier transport and collection limitations introduced by the insulating 2.2 nm SiO_x layer. Performing high-resolution transmission electron microscopy at a bright spot identified with EBIC reveals that conduction pinholes in SiO_x can be regions of thin tunneling SiO_x rather than a geometric pinhole. Additionally, selectively etching the underlying *poly*-Si layer in contacts with 1.5 and 2.2 nm thick SiO_x layers using tetramethylammonium hydroxide results in pinhole-like etch features in both contacts. However, EBIC measurements for a contact with a thinner, 1.5 nm SiO_x layer do not reveal pinholes, which is consistent with uniform tunneling transport through the 1.5 nm SiO_x layer. Finally, we theoretically show that reducing the metal to the *c*-Si contact size from microns, like in the *p*-type passivated emitter rear contact, to tens of nanometers, like in *poly*-Si contacts, allows lowering of the unpassivated contact area by several orders of magnitude, thus resulting in excellent passivation, as has been demonstrated for these contacts.

Solar energy is a prime candidate for meeting future world energy demands, and Si photovoltaics (PV) is the leading technology dominating the solar market. However, to utilize its full potential and lower the net $/kWh cost of electricity, it is important to increase the cell efficiency. Efficiency improvements in monocrystalline silicon (*c*-Si) based solar cells have been achieved by transitioning from the traditional Al-back surface field (20.3%)[1] to the *p*-type passivated emitter rear contact (*p*-PERC) (25.0%),[1] to polycrystalline Si (*poly*-Si) contacts (26.1%),[2] and to Si heterojunction cells (26.7%).[3] These improvements are enabled by lowering or almost completely eliminating the fraction of the silicon surface that is directly in contact with the metal used for charge collection. Amongst these high-efficiency architectures, *poly*-Si contacts are prime candidates for next-generation Si PV because their high thermal stability makes them compatible with current mainstream cell manufacturing processes like Ag-paste firing.[4–9] However, the wide-scale industrial implementation of these structures has been limited due to high processing costs and a lack of fundamental understanding from a manufacturing perspective.

The very low defect density at the SiO_x/*c*-Si interface is crucial to enable the ultrahigh efficiencies reported for these cells. Passivation with SiO_x has been previously utilized in both the Al-BSF and *p*-PERC cells.[10] The *poly*-Si/SiO_x/*c*-Si structure has also been well studied in various Si based electronic devices such as bipolar junction transistors.[11] The *poly*-Si/SiO_x contact structure was introduced into *c*-Si solar cells by Yablonovitch in the 1980s,[4] followed by Gan in the 1990s.[5] However, only

recently, significant improvements to this structure were reported.[6,7] Since then, interest in this topic has piqued, but one of the main factors still not well understood is the carrier transport through the SiO_x layer.[12,13]

Based on the thickness of the SiO_x layer, *poly*-Si/SiO_x passivated contacts can be classified into two broad categories. The first category is described as tunneling contacts with SiO_x thickness ≤1.5 nm incorporated into a *poly*-Si/SiO_x/*c*-Si stack, which are then annealed between 850 and 900 °C and have resulted in 25.8% cell efficiency.[14] For these contacts, tunneling through the SiO_x layer is likely the dominant conduction mechanism.[12,15] The second category, described as pinhole contacts, consists of an SiO_x layer with thickness >2 nm within the *poly*-Si/SiO_x/*c*-Si stack, which are annealed at significantly higher temperatures between 1000 and 1050 °C and have resulted in 26.1% cell efficiency.[2] For these contacts, the dominant conduction mechanism is proposed to be direct conduction between the *poly*-Si layer and the *c*-Si absorber through geometric pinholes in the SiO_x layer, formed due to high temperature annealing.[5,13] Nanoscale pinhole formation via balling-up of SiO_x is governed by thermodynamics and occurs so as to reduce the surface energy of the SiO_x layer.[16] The extent of balling-up depends on both SiO_x thickness and annealing temperature, and hence, these parameters need to be taken into consideration while optimizing the *poly*-Si/SiO_x/*c*-Si contact performance for passivation and conduction. While evidence of localized conducting regions in an otherwise insulating SiO_x layer can be inferred by measuring conductivity through the SiO_x layer[17] and via selective etching with a tetramethylammonium hydroxide (TMAH) solution,[18] the actual observation of the pinhole structure through imaging techniques is challenging due to their small size, likely 10 s of nm, and the low surface density, ~10^5–10^9 cm^{-2}.

In this work, we aim to verify the existence of pinholes in both thick (>2 nm) and thin (<2 nm) SiO_x passivating contacts using electron-beam-induced current (EBIC) measurements that allow for the detection of conductive regions non-destructively, while revealing their microscopic origin through high-resolution transmission electron microscopy (TEM). Our EBIC measurements support the hypothesis that uniform tunneling transport and locally enhanced conduction through thinner SiO_x regions are the dominant transport mechanisms in contacts with 1.5 and 2.2 nm SiO_x layer, respectively. Performing TEM in a region identified as a pinhole with EBIC reveals this location to be a thinner SiO_x region facilitating tunneling transport instead of direct conduction between *poly*-Si and *c*-Si. To maintain consistency with the current terminology, we use the term "pinholes" to refer to features that allow for locally enhanced conduction through an otherwise non-conducting SiO_x layer, which are not necessarily a geometric pinhole.

Double-side-polished, phosphorous-doped, float-zone Si(100), 1–5 Ω·cm resistivity, ~280 μm thick wafers were cleaned followed by treatment with 1% aqueous HF. Subsequently, either a 1.5 or 2.2 (±0.05) nm thick dry thermal SiO_x layer was grown on the cleaned wafers in a quartz tube furnace with a 6:1 N_2-to-O_2 gas flow ratio. The SiO_x thickness was determined by spectroscopic ellipsometry. Doped or intrinsic (*i*) hydrogenated amorphous Si (*a*-Si:H) was then deposited on both sides of the oxidized wafers using plasma enhanced chemical vapor deposition.[19] For the contacts with a 1.5 nm SiO_x layer, the n^+–*a*-Si:H/SiO_x/*c*-Si/SiO_x/p^+–*a*-Si:H structures were annealed at 850 °C for 30 min in a quartz tube furnace under N_2. For the pinhole contacts with a 2.2 nm SiO_x layer, first the *i*–*a*-Si:H/SiO_x/ *c*-Si/SiO_x/*i*–*a*-Si:H structures were annealed at 1025 °C for 30 min. Following treatment with 1% aqueous HF, doped *a*-Si:H layers were deposited to form n^+–*a*-Si:H/*i*–*poly*-Si/SiO_x/*c*-Si/SiO_x/ *i*–*poly*-Si/p^+–*a*-Si:H structures and the samples were annealed at 850 °C for 30 min resulting in n^+–*poly*-Si/SiO_x/ *c*-Si/SiO_x/ p^+–*poly*-Si structures. We performed a two-step annealing process for the 2.2 nm SiO_x contacts to ensure that the extent of conduction pinhole formation in SiO_x was not influenced by different dopant types, i.e., phosphorous and boron,[20] thus resulting in the best passivation. The structures were then coated with Al_2O_3 grown by atomic layer deposition, followed by annealing in forming gas.[19,21] Few of these samples were metallized with Al via thermal evaporation through shadow masks to create 4 cm^2 bifacial test cells. No post-metallization annealing was performed. Cell performance was quantified using current-voltage (J–V) measurements. EBIC measurements were performed on the same cells, in un-metallized regions, using a scanning electron microscope (SEM) (JEOL JSM-7600) with images acquired using an electron beam accelerating voltage of 5 kV and a beam current of ~1 nA. Unmetallized sister samples were used for TMAH etching experiments.

The open-circuit voltage (V_{oc}) of test cells with 1.5 and 2.2 nm SiO_x layers was 705 ± 2 and 695 ± 2 mV, respectively, indicating good passivation in both contacts. The corresponding fill-factors were 75.1% ± 0.5% (1.5 nm SiO_x) and 66.3% ± 0.5% (2.2 nm SiO_x), which translate into series resistances[22] of 0.86 and 1.46 Ω·cm^2 respectively, indicating that there is sufficient conduction through the SiO_x layer in both the contacts. Thus, we can infer that both the cells have passivated contacts suitable for follow-up measurements. To ensure unambiguous interpretation of TMAH-etching and EBIC experiments, the bifacial test cells were fabricated with polished Si wafers without a transparent conducting oxide or anti-reflection layer. We have demonstrated ~21.4% front/back *poly*-Si cells using very similar processing conditions.[23]

TMAH is very selective in removing Si over SiO_x. For example, using a 15% TMAH solution at 75 °C, the etch times for our 50 nm thick n^+–*poly*-Si layer and 1.5 nm thermal SiO_x layer are ~10 and ~300 s, respectively. Hence, by over-etching the n^+ *poly*-Si, in our case for 3 min, etch pits can be created in the underlying *c*-Si wafer through pinholes that may be present in the SiO_x layer. However, a similar experiment is difficult to perform for p^+–*poly*-Si contacts due to comparable etch times for a 50 nm thick p^+–*poly*-Si and a 1.5 nm thermal SiO_x layer. Figure 1 shows the SEM images of the wafer surface with different initial film stacks after etching with TMAH solution. Etching of a wafer with a 2.2 nm thermal SiO_x layer does not result in any surface features [see Fig. 1(a)]. However, when a n^+–*poly*-Si layer with 2.2 nm SiO_x is etched [see Fig. 1(b)], we observe numerous inverted pyramid-like features, highlighted by dotted circles. These are formed due to local non-uniformities in the SiO_x layer which originate due to annealing of the 2.2 nm SiO_x contact at

1025 °C. Figure 1(c) shows the SEM image of an etched wafer surface with a 1.5 nm thermal SiO_x layer only. Surprisingly, we notice numerous inverted pyramid-like features. These are observed for various etching conditions, 3–15 min in TMAH at 60–75 °C. Since it is known that SiO_x grows uniformly and almost stress-free on a flat *c*-Si surface,[24] we speculate that the etch pits in Fig. 1(d) (n^+–*poly*-Si with 1.5 nm SiO_x contact) are artifacts created by non-uniform TMAH-etching of the thin SiO_x layer. Hence, the reason for the formation of etch pits in a 1.5 nm SiO_x contact is unclear. Therefore, we further studied these contacts using EBIC measurements, which are non-destructive and sensitive to electronic effects.

The intensity in EBIC images results from the separation of electron-hole pairs generated by the electron beam within a SEM and subsequent collection of these excited carriers, which results in a current.[25] The generated current depends on the interaction of charge carriers with defects or inhomogeneities in the device and the carrier collection probability. Thus, EBIC measurements can result in maps with no features due to spatially uniform carrier collection, darker features due to carrier recombination in regions with defects, or brighter features due to enhanced local carrier collection. Figures 2(a) and 2(b) show the EBIC images of the metallized test cells measured on the p^+-*poly*-Si side with 2.2 and 1.5 nm SiO_x contacts, respectively. Figures 2(c) and 2(d) show the schematic of the proposed carrier recombination and current pathways. The density of bright spots in the EBIC images for the n^+–*poly*-Si side of the same test cells was similar to that for the p^+-*poly*-Si side and therefore not discussed. We can see that while the EBIC map for the 2.2 nm SiO_x contact shows numerous bright spots, the 1.5 nm SiO_x contact does not show any features. We attribute the bright spots in Fig. 2(a) to enhanced conduction through the 2.2 nm SiO_x layer. If recombination at a pinhole in a conducting SiO_x layer is significant, then a pinhole region should appear darker in EBIC. However, for the case of a contact where the SiO_x layer is non-conducting, carrier collection probability is much higher in proximity to a pinhole, thus resulting in a higher EBIC signal.[25] As shown schematically in Fig. 2(c), there are two components in the locally enhanced EBIC signal in Fig. 2(a): first, a depletion region forms underneath a pinhole due to higher dopant diffusion from p^+–*poly*-Si into the wafer directly through the SiO_x pinhole compared to the continuous SiO_x layer, thus improving carrier separation.[26] Second, there is reduced charge collection far from pinholes due to lateral diffusion requirements introduced by the insulating 2.2 nm thick continuous SiO_x layer. Any holes excited away from the pinhole need to first diffuse to a pinhole location before being collected by the p^+–*poly*-Si layer. The measured current will reduce due to hole recombination during this diffusion. While the quantification of these and/or other effects is difficult, nonetheless, we can infer from the bright spots in the EBIC image in Fig. 2(a) that local pinhole-like transport dominates for the contacts with a ~2.2 nm thick SiO_x layer. Further analysis shows that the intensity of the bright spots varies: this suggests that the size of the pinhole-like features varies or carrier collection probability varies due to differences in the structures of these defects.

The lack of contrast in the EBIC image for the 1.5 nm SiO_x contact [Fig. 2(b)] means that the carrier collection efficiency is uniform over the sample surface. This is possible only when the resistance to carrier transport through a SiO_x layer and pinholes (if they exist) is comparable during the EBIC measurement. Thus, we can conclude that tunneling through SiO_x is the likely dominant carrier transport mechanism for the 1.5 nm SiO_x contact. It must be noted that the absence of any bright or dark spots compared to the background in the EBIC image for these

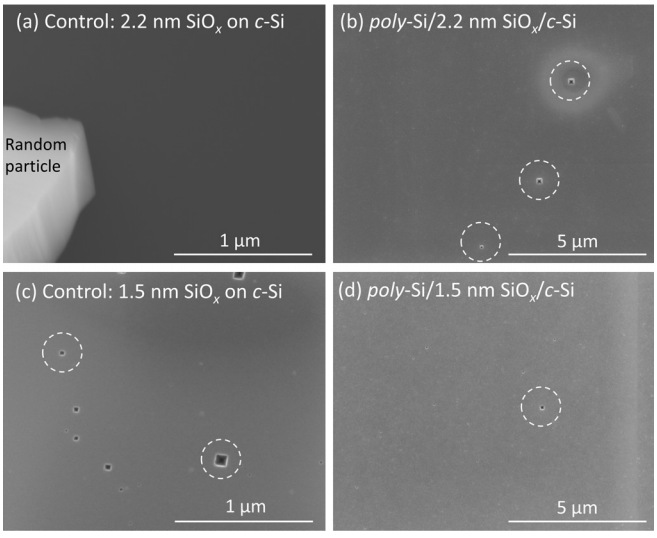

FIG. 1. SEM images of a polished *c*-Si surface after etching different test structures in 15% TMAH solution at 75 °C for 3 min. The images correspond to (a) a *c*-Si wafer with a 2.2 nm thick SiO_x layer, (b) a n^+-*poly*-Si contact with a 2.2 nm thick SiO_x layer that was annealed at 1025 °C, (c) a *c*-Si wafer with a 1.5 nm thick SiO_x layer, and (d) a n^+-*poly*-Si contact with a 1.5 nm thick SiO_x layer that was annealed at 850 °C.

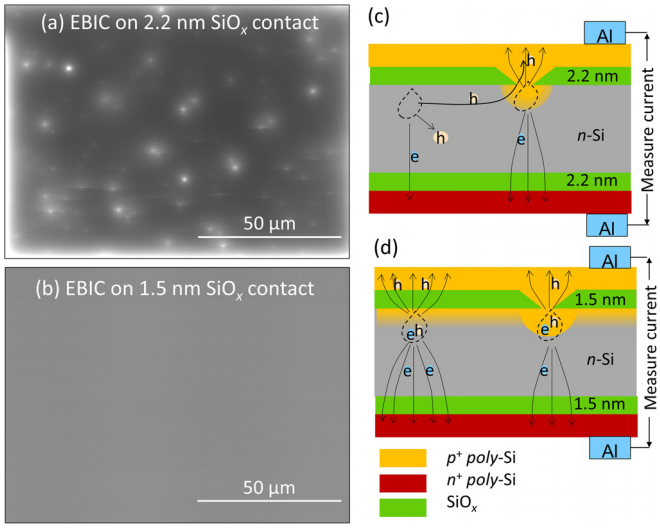

FIG. 2. EBIC maps of p^+-*poly*-Si passivated contacts with (a) 2.2 nm and (b) 1.5 nm thick SiO_x layers. Schematic of proposed current transport pathways in passivated contact cell test structures with (c) 2.2 nm and (d) 1.5 nm thick SiO_x layers.

contacts cannot be interpreted as the absence of pinholes. It is possible that the diffused junction underneath the SiO_x layer, formed due to dopant diffusion during the 850 °C anneal,[26] separates the carriers very efficiently. Hence, recombination at pinholes, which would otherwise lead to dark spots, might not influence EBIC intensity, i.e., field-effect passivation dominates over chemical passivation.[27]

Since the probability of detection of pinholes using techniques like TEM is very low due to their small size and low surface density, we perform site-specific TEM of a potential pinhole via EBIC imaging in a dual-beam focused ion beam (FIB) workstation. After identifying a region with a few bright spots in EBIC [see the dotted rectangle in Fig. 3(a)], a protective Pt layer was locally deposited on top of it. The TEM cross-section specimen was then prepared near the center of bright spots by standard FIB liftout methods. Diffraction and phase contrast high-resolution TEM imaging were then performed on the prepared sample using a TEM operated at 200 kV. Most of our ~260 high-resolution TEM images appear as shown in Fig. 3(b); a uniform layer of ~2.3 nm thick SiO_x separating the *c*-Si wafer and the *poly*-Si layer. However, in one image [see Fig. 3(c)], we observed significant localized thinning of the ~2.3 nm thick SiO_x layer to ~1.4 nm. We refer to this thinned down SiO_x region as a conduction pinhole. We consider this as a significant finding since previous TEM studies demonstrating SiO_x balling-up were performed on samples intentionally annealed to very high temperatures or had a very thin SiO_x layer causing significant SiO_x balling-up, resulting in very poor passivation.[12,16] Our sample still retained good passivation (695 mV V_{oc}) and conduction. The ~1.4 nm thick SiO_x layer is within the tunneling regime and should manifest similarly to a geometric pinhole, i.e., enable conduction, may create etch pits during TMAH-etching, and appear as a bright spot in EBIC. Additionally, the thinner SiO_x layer will allow for more dopant diffusion than the thicker SiO_x layer, as shown by the secondary ion mass spectrometry (SIMS) depth profile in Fig. 3(d), which has been reproduced from our previous work.[26] This enhanced dopant diffusion will create a local depletion region under the thinner SiO_x region allowing for more efficient carrier separation during the EBIC measurements, thus resulting in conduction pinholes to appear bright as witnessed in Fig. 2(a). We would like to clarify that in our experiments we have separated the conduction pinhole formation step (1025 °C) and the dopant diffusion step (850 °C). Since SIMS does not have the lateral resolution to distinguish the locally thin ~1.4 nm SiO_x regions from the surrounding 2.2 nm thick SiO_x regions [see Fig. 3(c)], we instead performed SIMS on two separate samples with 1.5 and 2.2 nm thick SiO_x layers within the *poly*-Si/SiO_x/*c*-Si stack annealed to 850 °C.

The results in Figs. 2 and 3 show that tunneling through SiO_x is the dominant transport mechanism in both 1.5 and 2.2 nm SiO_x contacts. The visual identification of the conduction pinhole as a locally thinned tunneling SiO_x layer was possible due to *in situ* milling within the vicinity of a bright spot identified during the EBIC measurement. However, it is possible that we may have milled away the actual pinhole and are instead just imaging a section that is away from the center of a crater-shaped structure. We also cannot rule the possibility that while some

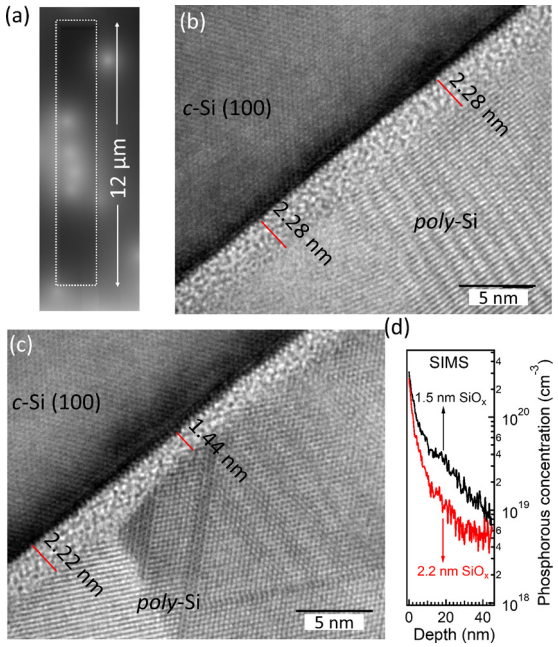

FIG. 3. (a) EBIC image of the region lifted out by FIB for TEM. The dotted rectangle shows the signal generated under the protective Pt layer. The cross-sectional TEM image of the pinhole type passivated contact at two different locations showing (b) uniform SiO_x thickness and (c) local thinning of the SiO_x layer. (d) The SIMS depth profile of phosphorous underneath the SiO_x layer of a passivated contact with 1.5 (black) and 2.2 (red) nm thick SiO_x layers after annealing at 850 °C. SIMS data reproduced from Ref. 26.

conduction pinholes may be true geometrical pinholes, others might correspond to regions with a locally thin tunneling SiO_x layer as suggested in Fig. 3(c). This agrees with the fact that the brightness of the pinholes varies in the EBIC image for the pinhole type contact shown in Fig. 2(a).

The high performance of Si solar cells is enabled by passivated contacts with low contact resistivity while maintaining a high degree of surface passivation. In *p*-PERC cells with an efficiency potential of ~24%,[28] good surface passivation is realized by localized back surface field contacts between Al and *c*-Si through 10s of microns of wide openings made through a dielectric Al_2O_3/SiN_x passivation layer stack. Below, we show that the contact performance is expected to improve remarkably by reducing the local contact (geometric pinhole) size to nanometers. Indeed, the metal to semiconductor contact area fraction f determines the surface recombination losses in the cell via the total diode current pre-factor $J_{o,total}$, which is given by Eq. (1), where $J_{o,pinhole}$ and $J_{o,oxide}$ are the pre-factors for the unpassivated metallized region and the passivated oxide region, respectively

$$J_{o,\,total} = f \times J_{o,\,pinhole} + (1-f) \times J_{o,\,oxide}. \quad (1)$$

On the other hand, the total contact resistivity, which determines the fill-factor, is a sum of area-independent specific contact resistivity, $R_{pinhole}$ ($\Omega\cdot cm^2$), in the pinhole and the spreading resistance within the wafer underneath the pinhole. The spreading resistance for pinhole radii, r, which are much less than the

wafer thickness, can be approximated as $\rho_w/4r$ for the wafer bulk resistivity ρ_w.[29] Thus, the total contact resistivity, R_{total}, is

$$R_{total} = \left(R_{pinhole} + \frac{\rho_w}{4r} \times \pi r^2\right)/f \approx \pi \rho_w r/4f. \quad (2)$$

The 2nd term in Eq. (2), which relates to the spreading resistance, is 2–3 orders of magnitude greater than the $R_{pinhole}$ term for pinhole sizes between 1 nm and 10 μm. The interesting conclusion from Eq. (2) is that for the same R_{total}, as the size of the pinhole decreases from ~10 μm in *p*-PERC to ~10 nm in pinhole containing *poly*-Si contact, the unpassivated area fraction f can be lowered by nearly three orders of magnitude. This feature of nanostructured >2 nm SiO_x contacts allows for sufficient conduction through the pinholes in the SiO_x layer in passivated contacts, while resulting in very low J_o. It must be noted that while the $J_{o,\,pinhole}$ term in Eq. (1) has some inverse dependence on the pinhole size,[30] the 26.1% cell demonstrated by such contacts shows a clear advantage in device performance when using nanostructured contacts.[2] Hence, we can treat pinhole containing *poly*-Si contacts as a category of PERC, i.e., "nano-PERC" contacts, exhibiting nanometer size instead of micron size holes in the passivating SiO_x layer. We also propose that instead of using high temperature annealing, other pinhole formation techniques such as nano-imprint lithography[31] could be explored. Therefore, local nano-pinhole contacts are excellent candidates for the next generation c-Si PV and could have potential uses in other photovoltaic and electronic technologies.

In summary, we have demonstrated the use of EBIC to map conduction-enabling pinholes in *poly*-Si/SiO_x passivated contacts. Pinhole-like structures appear as bright spots in EBIC for contacts with a ~2.2 nm SiO_x layer due to carrier transport and collection limitations. Site-specific TEM investigation reveals that a conduction pinhole can be a region of the tunneling SiO_x layer. The detection of similar pinholes in 1.5 nm SiO_x contacts was challenging due to TMAH-etching artifacts and defect detection limitations in EBIC measurements: this is consistent with the tunneling nature of the 1.5 nm SiO_x layer. Thus, the carrier transport mechanism in both 1.5 and 2.2 nm thick SiO_x contacts is through tunneling, the difference being uniform tunneling in the first case while tunneling through locally thin SiO_x regions in the latter. Finally, we propose a nano-PERC concept which might allow for high efficiency c-Si cells.

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