Solid State Sciences 58 (2016) 115–121

Contents lists available at ScienceDirect

Solid State Sciences

journal homepage: www.elsevier.com/locate/ssscie

Fabrication and electrical characterization of nickel/p-Si Schottky diode at low temperature

Rajender Kumar*, Subhash Chand

Department of Physics, National Institute of Technology, Hamirpur, 177005, HP, India

ARTICLE INFO

Article history:
Received 9 November 2015
Received in revised form
8 June 2016
Accepted 10 June 2016
Available online 18 June 2016

Keywords:
Current-voltage characteristics
Capacitance-voltage characteristics
Barrier height
Ideality factor
Ni/p-Si Schottky diode

ABSTRACT

In this study the current–voltage and capacitance–voltage characteristics of metal semiconductor Ni/p-Si(100) based Schottky diode on p- type silicon measured over a wide temperature range (60–300 K) have been studied on the basis of thermionic emission diffusion mechanism and the assumption of a Gaussian distribution of barrier heights. The parameters ideality factor, barrier height and series resistance are determined from the forward bias current–voltage characteristics. The barrier height for Ni/p-Si(100) Schottky diode found to vary between 0.513 eV and 0.205 eV, and the ideality factor between 2.34 and 8.88 on decreasing temperature 300–60 K. A plot involving the use of φ_b versus 1/T data is used to gather evidence for the occurrence of a Gaussian distribution of barrier height and obtain the value of standard deviation. The observed temperature dependences of barrier height and ideality factor and non-linear activation energy plot are attributed to the Gaussian distribution of barrier heights at the metal-semiconductor contact. The barrier height of Ni/p-Si(100) Schottky diode was also measured over wide temperature from the capacitance-voltage study.

1. Introduction

Metal-semiconductor (MS) contacts have attracted increasing interest owing to their various potential technological applications [1–12]. The metal-semiconductor contact is a simple and technologically important in semiconductor devices. The performance of the Schottky diodes is dominated by the properties of the barrier formed at the contact interface. The quality of the diode is evaluated by the Schottky barrier height and ideality factor. For the case of an ideal Schottky diode, its barrier height should same and the ideality factor should remain almost close to unity over the temperature range. In a practical Schottky barrier [13–17], the current–voltage (I–V) characteristics of the metal-semiconductor contacts usually deviate from the ideal thermionic emission (TE) current model.

Huang et al. [18] studied the electrical characteristics of Ni/Si(100) solid-state reaction with yttrium (Y) addition. The electrical characteristic measurements reveal that no significant Schottky barrier height modulation with the addition of Y occurs. Kim et al. [19] studied the growth of Ni silicide nanowires by physical vapor deposition. The electrical and morphological changes of silicide formation were observed on a gradient Ni film thickness, which visualized the critical thickness is 60–80 nm to grow nanowires. Demirezen et al. [20] investigated the current-transport mechanisms of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN Schottky barrier diodes (SBDs) over the wide temperature range of 80–400 K. Kiziroglou et al. [21] fabricated the electrodeposited Ni–Si contacts and the transport mechanisms through the formed Schottky barrier are studied. Highly doped Si is used to enable tunneling currents.

Kiziroglou et al. [22] fabricated the Ni–Si Schottky barrier diodes by electro-deposition using Si substrates and studied the I-V and capacitance-voltage (C-V) characteristics at low temperature. A mean value of 0.76 V and a standard deviation of 66 mV were reported for the Schottky barrier height at room temperature with a linear bias dependence. Nakatsuka et al. [23] investigated the effects of C^+ ion implantation into Si substrates on electrical properties of NiSi/Si(001) contacts. Zhu et al. [24] studied the I–V and C–V characteristics of Ni silicide/n-Si(100) contacts, were formed at various annealing temperatures from 350 to 800 °C. The experimental I–V data of the low temperature annealed diodes obey the traditional thermionic emission (TE) model quite well, and the barrier heights are deduced to be approximately 0.62 eV for Ni_2Si/Si and 0.67 eV for NiSi/Si diodes respectively. Roccaforte et al. [25] investigated the structural and electrical properties of Ni/Ti/SiC

* Corresponding author.
E-mail addresses: rkthakurnitham@gmail.com (R. Kumar), schand64@gmail.com (S. Chand).

http://dx.doi.org/10.1016/j.solidstatesciences.2016.06.003
1293-2558/

Schottky contacts upon thermal treatments. The physical information obtained from the study of this bilayer can be extremely important in the control of the electrical properties of Schottky barriers for advanced devices on SiC. Sahay et al. [26] have investigated the room temperature I-V and C-V characteristics of Ni/n-Si SBDs fabricated by the vacuum vapor deposition, and found a value of barrier height 0.73 eV from the forward bias I-V characteristics at 300 K. In this work, we have fabricated the Ni/p-Si Schottky diode and studied the electrical properties, temperature dependent I-V and C-V characteristics in the temperature range 60–300 K.

2. Experiment

The Ni/p-Si Schottky diode was fabricated on boron doped p-type (1 Ω-cm resistivity) silicon wafer of (100) orientation. Prior to back ohmic contact and Schottky contact deposition, the silicon wafer was properly cleaned and etched for native oxide removal from the surface. The wafer was first cleaned with organic solvents viz., trichloroethylene, acetone and methanol in succession then rinsed in demonized water of resistivity 18 MΩ-cm and then etched in a 40% HF solution for 1 min. After each cleaning step, the silicon wafer was rinsed thoroughly in demonized water of resistivity 18MΩ-cm for 1 min. After cleaning and etching steps, the silicon wafer was loaded in 12" vacuum coating unit Model 12A4D. Ohmic contact was established on the back side of the p-type silicon wafer by depositing high purity (99.999%) aluminum at a constant pressure of 3×10^{-6} mbar with a thickness of ~2000 A°. The back ohmic contact was annealed at 300 °C for 1 h in a vacuum of 1×10^{-3} mbar. The back ohmic contact was protected by picein.

The nickel film (Thickness~2000A°) was subsequently deposited by 12" vacuum coating unit Model 12A4D on the front side of p-type silicon wafer by using metal mask having holes of diameter 1 mm in a vacuum of 3×10^{-6} mbar to form a Schottky junction. Before metal deposition the silicon wafer was cleaned and etched in a 40% HF solution for 1 min to remove the native oxide layer formed on silicon wafer. The temperature dependent I-V measurements were performed by using a programmable Keithley 2400 source meter in the temperature range of 60–300 K using a Lake shore model 331 temperature controller cryogenics HC2. In addition, the whole I-V measurements were performed by using a computer through an IEEE-488 interface card. The C-V measurements were performed with Precision Impedance Analyzer (Wayne Kerr 6520A) and close cycle helium refrigerator with temperature controller.

3. Method of analysis

On the basis of thermionic emission-diffusion theory the current through a Schottky diode is given by Ref. [1,2].

$$I = I_S\left[\exp\left(\frac{q(V - IR_S)}{kT}\right) - 1\right] \quad (1)$$

with

$$I_S = A_d A^{**} T^2 \exp\left(\frac{-q\varphi_b}{kT}\right) \quad (2)$$

where I_s is reverse saturation current at zero bias, A_d is the diode area, A^{**} is the effective Richardson constant, T is the temperature in Kelvin, k is the Boltzmann constant, q is the electronic charge, φ_b is the barrier height, η is the ideality factor and R_s the diode series resistance. It is customary to make ln(I) versus V plots at various temperatures and extract from the straight-line portion the saturation current (I_s) by extrapolation to zero-bias and the ideality factor from the slope itself. Alternatively, a computer program is utilized to fit the experimental I-V data in the thermionic emission-diffusion Eq. (1) using least square fitting by iteration to find I_s , η and R_s [15]. Once I_s is known, the barrier height φ_b can easily be determined from (2) at any temperature for a given diode area A_d and Richardson constant A^{**} (3.2×10^5 Am^{-2} K^{-2} for p-type Si [27,28]).

4. Results and discussion

4.1. Forward I-V characteristics

The measured forward current-voltage (I-V) characteristics of Ni/p-Si(100) Schottky barrier diodes in the temperature range 60–300 K are shown in Fig. 1. These plots clearly depict linearity over several order of current. Further, they progressively become straight over a wide current range with decrease in temperature. The increase in the slope of the straight-line portion of the ln(I)-V curve and the gradual shift of the plot towards higher voltage side observed with decrease in temperature are in agreement with TED Eq. (1). The measured I-V data of Fig. 1 is fitted in TED current Eq. (1) to derive the apparent barrier parameters, namely, the barrier height, ideality factor and series resistance. The variation of these parameters as a function of temperature is shown in Figs. 2, 3 and 5, respectively.

Fig. 1 shows the variation of zero-bias barrier height φ_{b0} decreases with decrease of temperature steadily in the beginning but sharply at low temperatures. At temperature below 180 K there is deviation from linear rise in current at low bias and extra current exist at low bias below this temperature.

Decreased barrier height would mean that the ln(I)-V plots originates from higher current on the ordinate at any given temperature, i.e. the device exhibits higher current than the ideal case where the measured current will decrease much and the derived barrier height would remain flat. This extra current may be arising due to leakage effect. For extraction of barrier parameters the linear part at selective bias region used in the fitting process. The ideality factor η initially increases slowly with decrease in temperature but rises significantly below 100 K and attains a value of 8.88 at 60 K as shown in Fig. 3.

The barrier height can also be determined from the activation energy plot and for this Eq. (2) can be rewritten as

$$\ln\left(\frac{I_s}{T^2}\right) = \ln(A_d A^{**}) - \frac{q\varphi_b}{kT} \quad (3)$$

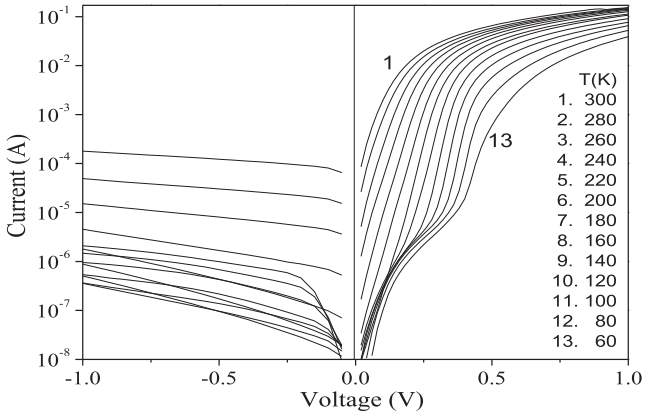

Fig. 1. The forward current-voltage characteristics of Ni/p-Si Schottky contacts measured at various temperatures.

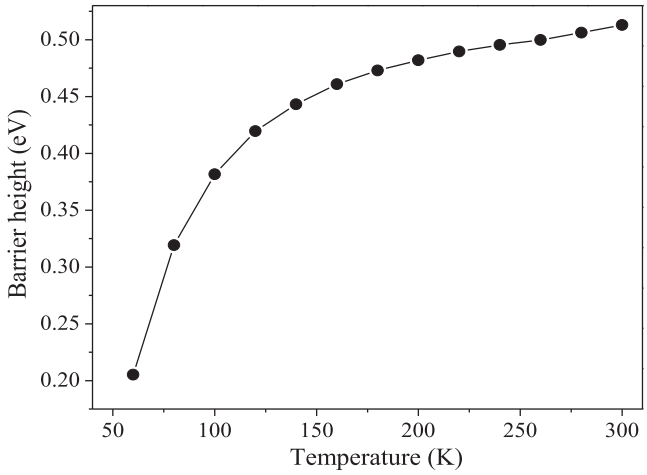

Fig. 2. The variation of apparent derived barrier height as a function of temperature for Ni/p-Si Schottky contacts.

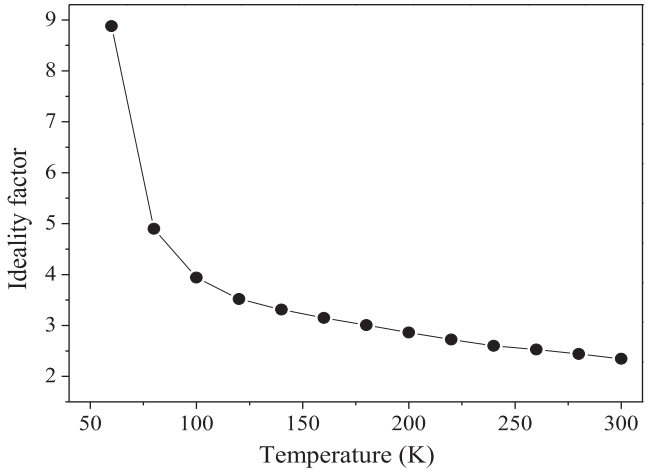

Fig. 3. The variation of apparent derived ideality factor as a function of temperature for Ni/p-Si based Schottky contacts.

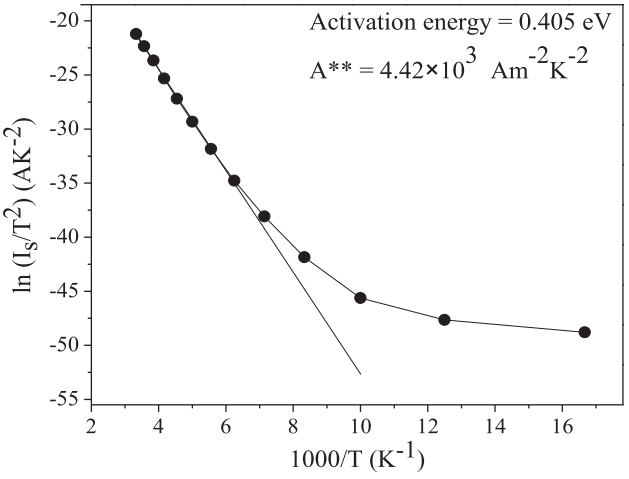

Fig. 4. Conventional activation energy ($\ln(I_s/T^2)$ vs. 1000/T) plot.

Therefore, the $\ln(I_s/T^2)$ versus 1/T plot should be a straight line with slope determining the barrier height (φ_b) and the intercept at the ordinate giving the Richardson constant itself for a known diode area A_d. This method gives a single value of barrier height. Fig. 4 shows the plot of $\ln(I_s/T^2)$ versus 1000/T. The experimental data appear to fit, in straight line at higher temperature regime giving activation energy (0.405 eV). The value of A^{**} obtained from the intercept of the straight portion at the ordinate is equal to 4.42×10^3 Am^{-2} K^{-2}, which is much lower than the known value of 3.2×10^5 Am^{-2} K^{-2} for p-type silicon.

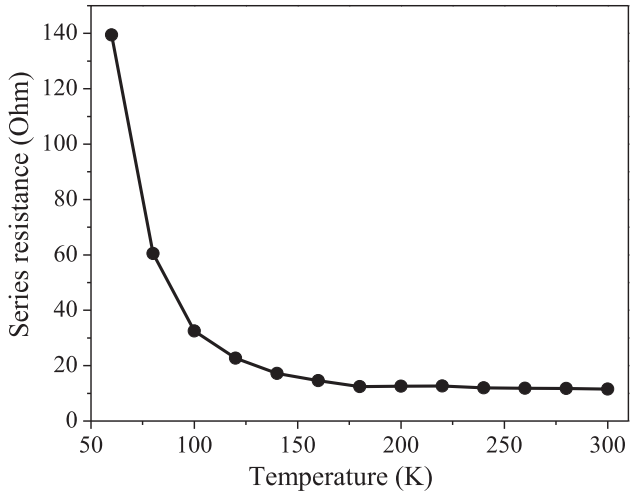

Fig. 5. The temperature dependence of series resistance R_s. It shows the sharp increase in R_s as the temperature falls below ~140 K.

The decrease in barrier height, increase in ideality factor and non-linear activation plot at low temperature are at first sight indicative of deviation from the pure thermionic emission-diffusion mechanism. The possible reason could be extra current caused by tunneling through the barrier and/or the generation-recombination process occurring in the depletion region. The parameter that determines the relative importance of tunneling (thermionic-field emission or field emission) and thermionic emission-diffusion is given by Ref. [28].

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_A}{m_h^* \varepsilon_S}\right)^{1/2} \tag{4}$$

where $m_h^* (= m_r m_0)$ is the effective mass of holes, $\varepsilon_s (= \varepsilon_r \varepsilon_0)$ is the permittivity of semiconductor, m_0 the electron rest mass and N_A is the acceptor concentration in m^{-3}. The Field Emission (FE) becomes important when $E_{00} \gg kT/q$, whereas, the Thermionic-Field Emission (TEF) dominates when $E_{00} \sim kT/q$, and thermionic emission-diffusion if $E_{00} \ll kT/q$. In the present case, N_A is1.3×10^{22} m^{-3} for the p-Si wafer used to make Schottky diode. The corresponding E_{00} value turns out to be 0.82 meV with $m_r = 0.56$ and $\varepsilon_r = 11.9$. Obviously, the condition prevailing is $E_{00} \ll kT/q$ and, therefore, the possibility of the FE and TEF can easily be ruled out. Also, the TFE causes reduction in the barrier height by an amount [28].

$$\Delta\varphi_t = \left(\frac{3}{2}\right)^{2/3} (E_{00})^{2/3} (V_d)^{1/3}. \tag{5}$$

where V_d stands for the voltage corresponding to the band bending. Thus, for E_{00} = 0.82 meV and V_d = 1.0 V, barrier lowering of ~11.5 meV should occur, which is indeed very small. In fact, the lowering is temperature dependent, whereas Eq. (5) suggests barrier lowering independent of temperature.

All the considerations advanced above suggest that tunneling

can become increasingly important only in highly doped semiconductors having $N_A > 10^{23}$ m^{-3}. At lower dopant concentrations, the contribution of tunneling (FE and TFE) becomes insignificant and TED dominates. Similarly, the recombination current can be described by Ref. [29].

$$I_r = I_{r0}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \tag{6a}$$

with

$$I_{r0} = \frac{qn_iA_dw}{2\tau} \tag{6b}$$

and

$$n_i = (N_CN_V)^{1/2}\exp\left(\frac{-qE_g}{2kT}\right) \tag{6c}$$

here w is the thickness of the depletion region, τ is the effective minority carrier lifetime within the depletion region, n_i is the intrinsic carrier concentration, E_g is the energy band gap and N_C and N_V are the effective conduction and valence band density of states, respectively.

The recombination of the electrons and holes is normally most effective near the center of the band gap. If the recombination current exists and is neglected, the barrier height evaluation on the basis of TED theory yields progressively lower values with decrease in temperature; for example if I_r, constitutes 91% of the total current at (say) 100 K, the expected barrier decrease is 0.02 eV [30]. This is the level of change actually observed in the present work (Fig. 2). However, such a possibility requires I_r to be of the same order as the current caused by the TED mechanism. In other words, the saturation current I_{r0} should be ~10^{-14} A at 100 K as against the estimated value of 10^{-34} A using Eq. (6b). Also, assuming the experimental current to be just recombination current I_{r0}, the energy band gap E_g can be determined from the slope of the $\ln(I_{r0}/T^{3/2})$ versus 1/T plot. This gives straight line only in the higher temperature range with value of E_g to be 0.77 eV, which is quite a low value than the actual value of the silicon band gap of 1.12 eV. Moreover, the depletion region recombination current is expected to become important only for Schottky diodes with large barrier height, low temperatures and lightly doped semiconductors with low carrier lifetime [2]. Therefore, one may infer that recombination current is also insignificant in the present case.

The above considerations, together with the fact that the ln(I) versus V becomes increasingly straight covering a larger span with decrease in temperature, suggest that the thermionic emission-diffusion mechanism is indeed operative even below 100 K. Therefore, an apparent increase in η and decrease in barrier height at very low temperatures are possibly caused by some other effects (inhomogeneities of thickness and composition of the silicide layer, non-uniformity of the interfacial charges, etc.) giving rise to extra current such that the overall characteristic still remains consistent with the thermionic emission process. The variation of series resistance (R_s) as a function of temperature is shown in Fig. 5. The sharp increase of R_s below 100 K is quite similar to the reported observations in a PtSi/silicon Schottky barrier diode and is believed to result from lack of free charge carriers at low temperatures [31].

4.2. Barrier inhomogeneities

The significant decrease of barrier height and increase of ideality factor at low temperatures are caused by barrier heights (BH) inhomogeneities possibly resulting due to variation in thickness and composition of silicide layer, describing the BH inhomogeneities with a Gaussian distribution function [32–35]. Assuming linear bias dependence of both the mean BH and standard deviation with coefficients γ and ξ, respectively, (Eqs. (1) and (2)) get modified in such a way that η_{ap} and φ_{ap} appear in place of η and φ_b [15–17,32,33]. The φ_{ap} and η_{ap}, are termed as apparent zero-bias barrier height and apparent ideality factor, respectively, and is given as

$$\varphi_{ap} = \overline{\varphi}_{b0} - \frac{q\sigma_0^2}{2kT} \tag{7}$$

$$\frac{1}{\eta_{ap}} = (1-\gamma) - \frac{q\sigma_0\xi}{kT} \tag{8}$$

where $\overline{\varphi}_{b0}$ stands for the mean barrier height and σ_0 is the standard deviation, both at zero-bias. Eq. (7) indicates that φ_{ap} versus 1/T plot should be a straight line, from the intercept and slope of which one can calculate mean barrier height and the standard deviation of the distribution. Fig. 6 shows φ_{ap} versus 1/T plot and from this plot we get $\overline{\varphi}_{b0} = 0.587$ eV and $\sigma_0 = 0.06$. Eq. (8) can be used to find bias coefficient of mean barrier height and the standard deviation of the Gaussian distribution from the plot of $1/\eta_{ap}$ versus 1/T. Fig. 7 shows $1/\eta_{ap}$ versus 1/T plot which is approximately linear and it yields $\gamma = 0.527$ and $\xi = 0.317$.

The temperature dependence of the ideality factor (η_{ap}) can be understood on the basis of Eq. (8). It indicates that $1/\eta_{ap}$ versus $1/T$ plot should yield a straight line with slope giving $\sigma_0 q\xi/k$ and intercept $1-\gamma$ The factor$1/(1-\gamma)$ is solely determined by the rate of change of the barrier height with bias and corresponds to the ideality factor of a Schottky diode having a homogeneous barrier of height $\overline{\varphi}_{b0}$. The increase of η_{ap} with fall in temperature arises due to the term containing ξ (i.e., rate of change of σ with bias). The plot of $1/\eta_{ap}$ versus $1/T$ (Fig. 7) corresponds to a negative slope in the present Ni/p-Si Schottky diodes and so ξ is essentially negative; the values being 0.317 for Ni/p-Si Schottky diode. These experimental results coupled with the positive values of γ(~0.5272) revealed that the increase of ideality factor is caused by the voltage dependence of σ (through ξ); also the contribution becomes significant at low temperatures.

Using Eqs. (2) and (7), one can write

$$\ln\left(\frac{I_s}{T^2}\right) - \frac{q^2\sigma_0^2}{2k^2T^2} = \ln(A_dA^{**}) - \frac{q\varphi_{b0}}{kT} \tag{9}$$

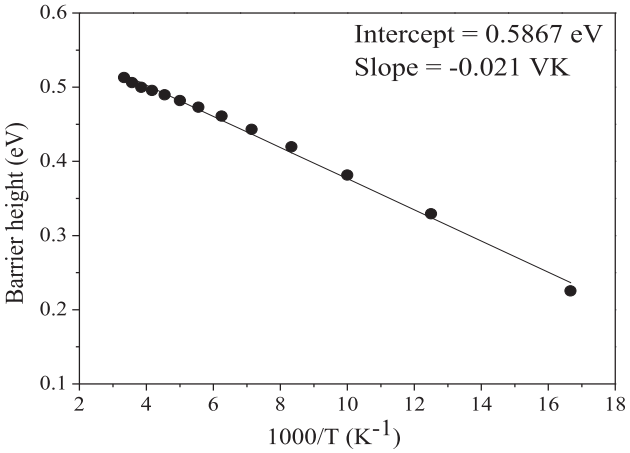

Fig. 6. The barrier height φ_{ap} obtained from I-V measurements as a function of inverse temperature.

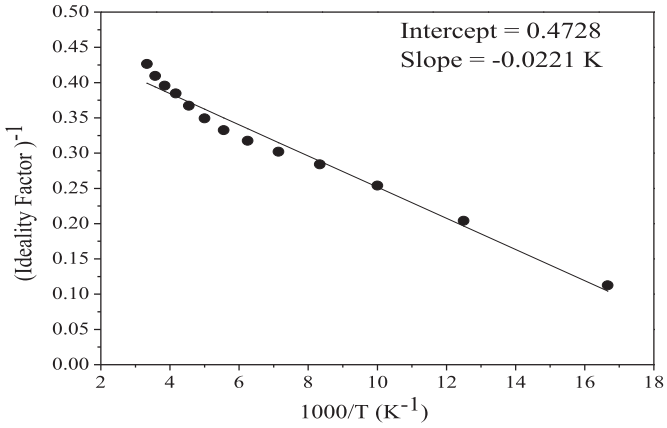

Fig. 7. The variation of inverse ideality factor as a function of inverse temperature in Ni/p-Si Schottky contact.

Thus the conventional activation energy equation gets modified under the assumption of Gaussian distribution of barrier heights. The nonlinearity in the activation energy plot can be understood on the basis of Eq. (9). The factor $\ln(I_s/T^2) - (q^2\sigma_0^2/2k^2T^2)$ is calculated to modify the experimental data and plotted as a function of $1/T$ which yields a straight line. Fig. 8 shows the modified activation energy plot along with the unmodified activation plot of Fig. 4 in the temperature ranges 60–300 K. From the intercept of the straight line in modified activation energy plot at ordinate the Richardson constant is calculated. The value obtained is 4.91×10^5 Am^{-2} K^{-2} for diodes on *p*-type silicon. From the slope of this modified activation energy plot the value of the mean barrier, $\overline{\varphi}_{b0}$ is calculated and comes out to be 0.594 V.

Thus the experimental results fit very well in Eqs. (7) and (8), giving $\overline{\varphi}_{b0} = 0.587$ V, $\sigma_0 = 0.060$, $\gamma = 0.527$ and $\xi = 0.317$. Moreover, Richardson constant now turns out to be 4.91×10^5 Am^{-2} K^{-2}, in close agreement with the known value of 3.2×10^5 Am^{-2} K^{-2}. These findings clearly point that the origin of decrease of the barrier height, increase of ideality factor and non-linear activation energy plot at low temperatures arises due to the barrier heights inhomogeneities prevailing at the metal-semiconductor interface.

4.3. Capacitance-voltage characteristics

The room temperature capacitance-voltage characteristics of Ni/p-Si Schottky diode were measured at different frequencies (100 KHz, 500 KHz, 1 MHz and 5 MHz) as shown in Fig. 9.

There are two defined regions of capacitance-voltage characteristics as shown in Fig. 9. The first region (from 0 to −2 V) shows the saturation region of the measured capacitance providing evidence on the total depletion of barrier height junction layer. The second region (0–1 V) shows the dependence of the measured capacitance on the forward bias which shows that the width of the depletion region decreases with the increase in the forward bias [36].

The Mott-Schottky plot $(A/C)^2$ versus V derived from the measured capacitance-voltage characteristics is discussed as shown in Fig. 10. There are linear dependence of $(A/C)^2$ versus V measured from capacitance-voltage characteristics at frequencies 100 KHz, 500 KHz, 1 MHz and 5 MHz with different slope values −0.67 V, −0.25 V, −0.050 V and 0.30 V respectively. The slopes value increases with the increase in frequency which indicates the contribution of the interface states at higher frequencies [36].

The C-V characteristics have been analyzed using the Schottky-Mott Eq [2].

$$\frac{1}{C^2} = \frac{2}{A^2 q \varepsilon_S \varepsilon_0 N_A}(V_{bi} + V) \tag{10}$$

where A is the diode area, q is electronic charge, ε_s is the dielectric constant of semiconductor, ε_0 is the dielectric constant of free space, N_A is the doping density, V_{bi} is the built-in voltage of the diode and V is the applied voltage. The Eq. (10) can be used to determine the doping density from the slope of the linear region of a C^{-2} against V graph. Fig. 11 shows C^{-2} against V graph for the Ni/p-Si Schottky diodes. From the Eq. (10), it is to clear that the built-in voltage (V_{bi}) can be calculated from the intercept of the straight line on the voltage axis. The Schottky barrier height is then obtained from the relation [1,2].

$$\varphi_b = V_{bi} + \frac{kT}{q} + \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \tag{11}$$

where, k is the Boltzmann constant, T is temperature, N_A is the acceptor concentration of p-type semiconductor and N_V is the

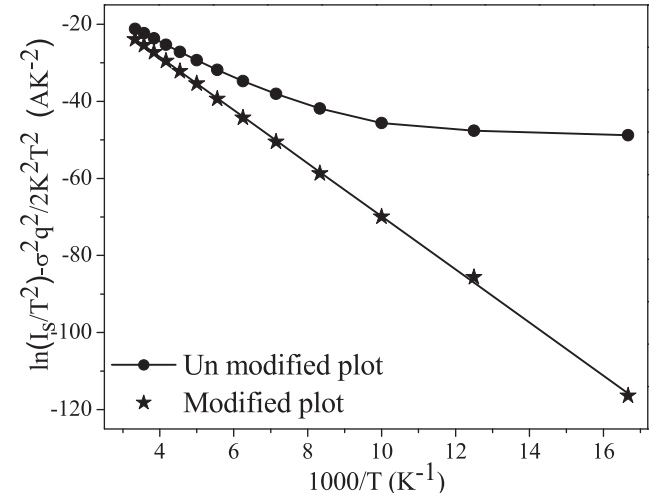

Fig. 8. The modified activation energy $\{\ln(I_s/T^2) - \sigma_0^2q^2/2K^2T^2$ verse 1000/T} plots with zero bias standard deviation σ_0 of 0.06 V.

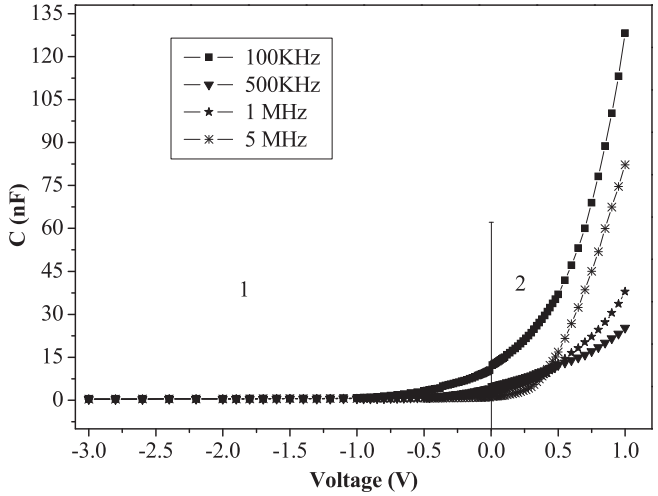

Fig. 9. The capacitance-voltage characteristics of the Ni/p-Si Schottky diode measured at room temperature.

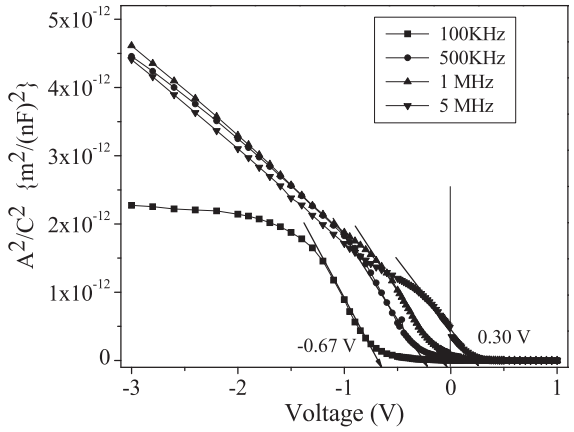

Fig. 10. Mott-Schottky plot of the capacitance-voltage characteristics of the Ni/p-Si Schottky diode.

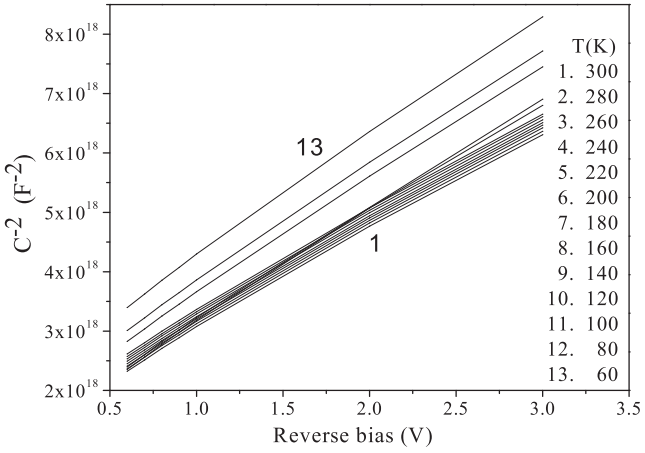

Fig. 11. Reverse bias $C^{-2} - V$ characteristics of the Ni/p-Si Schottky diode at a frequency of 1 MHz with temperature.

effective density of states in the valance band of p-Silicon, as given by Ref. [1].

$$N_V = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \tag{12}$$

Here, m_p^* is the effective mass of hole and his Plank's constant. From the intercept of the $1/C^2$ versus V curve on the voltage axis, the value of the barrier height is calculated.

The plots of C^{-2} as a function of reverse bias voltage are linear that indicates the formation of Schottky diodes [27]. With the help of Eq. (10), the values V_{bi} can be determined from the intercept of the extrapolated $C^{-2} - V$ plot on voltage axis. From the slope of $C^{-2} - V$ plot the acceptor density N_A of p-type silicon used for Schottky diodes fabrication is calculated to be 5.00×10^{16}/cc which is slightly higher than the acceptor concentration 1.30×10^{16}/cc of silicon corresponding to its specified 1 Ohm-cm resistivity.

From the measured C-V data, the barrier heights were calculated at frequencies 1 MHz using the intercept voltage of C^{-2}-V plot. The variation of barrier height as a function of temperature and the built-in potential of Schottky diode is shown in Fig. 12. The capacitance–voltage derived barrier heights for the Ni/p-Si diode found to vary from 0.89 eV to 1.05 eV on decreasing temperature from 300 K to 60 K. Fig. 12 also shows the I-V derived barrier height. As expected, the C-V derived barrier height value is higher than the barrier height derived from the I-V measurements.

The C–V curves gave a barrier height value higher than those obtained from the I–V measurements. This discrepancy can be explained by the different nature of the C–V and I–V measurement techniques. The barrier heights deduced from two techniques are not always the same. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise, they will yield different values. The different behaviour of Schottky barrier height obtained from the two techniques can be explained by a distribution of Schottky barrier height due to the inhomogeneities (as a combination of the interfacial insulator layer composition, non-uniformity of the interfacial insulator layer thickness, and distribution of interfacial charges) that occur at metal/semiconductor interface [28,29,33]. In C–V measurements only the edge of depletion layer is modulated, and short-wavelength potential fluctuations at the metal–semiconductor interface are screened at the edge of the space-charge region [37]. The capacitance is insensitive to potential fluctuations at a length scale of less than the space-charge width. The dc current I across the interface depend exponentially on barrier height and thus is sensitive to the detailed barrier distribution at the interface. Consequently, for an inhomogeneous interface, spatial variations of band bending and barrier height result in different Schottky barrier height for current and capacitance. In addition, the C–V technique averages over the whole area and measures the barrier height of Schottky diode. On the other hand, the barrier height from the I-V method includes any barrier lowering effect due to the interfacial insulator layer or the interface states, and an effective barrier height is measured. Other than this, the determination of Schottky barrier height from I-V characteristics is only reliable if one can be confident that the current is determined by TE theory. For this to be so, forward portion of the characteristics must be a good straight line with low value of ideality factor [2,34,35].

5. Conclusions

Forward I-V characteristics of the Ni/p-Si Schottky barriers follow thermionic emission-diffusion mechanism in a temperature range of 60–300 K.

While the barrier height φ_b decreases, ideality factor η and series resistance R_s increase with a decrease in temperature; the changes being quite significant at very low temperatures. The ln(I_s/

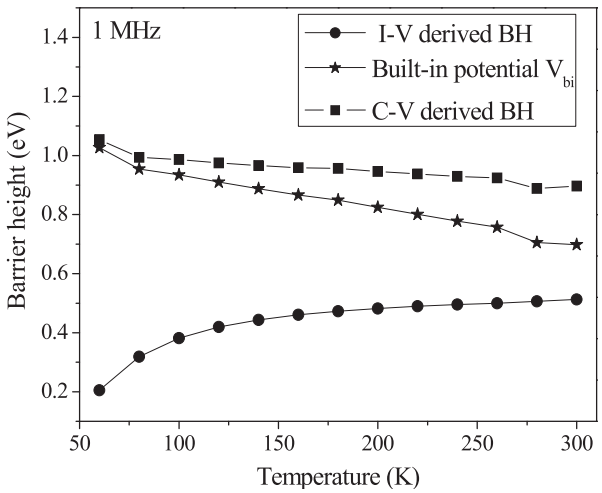

Fig. 12. Variation of barrier height and built in potential as a function of temperature derived from the measured C-V data at 1 MHz frequency.

T^2) versus 1000/T plot shows deviation from linearity at low temperatures. From the activation energy plot the zero-bias barrier height of Ni/p-Si Schottky diodes found to be ~0.405 V and the Richardson's constant A^{**} obtained from the intercept of the straight portion at the ordinate found to be 4.42×10^3 Am^{-2} K^{-2}, much lower than the known value of 3.2×10^5 Am^{-2} K^{-2} for p-type silicon.

Barrier height inhomogeneities at the interface caused deviation in the barrier height and ideality factor at low temperatures and gives rise to non-linear activation energy plot. The inhomogeneities were found to have Gaussian distribution of barrier heights with mean 0.587 eV and standard deviation 0.06 eV. Moreover, the effect of bias is to homogenize barrier heights at a slightly higher mean value.

The barrier heights of Ni/p-Si obtained from C-V measurements are 0.89 eV at 300 K, 1.05 eV at 60 K at1 MHz frequency.

References

[1] S.M. Sze (Ed.), Physics of Semiconductor Devices, Wiley, New York, 1981.
[2] E.H. Rhoderick, R.H. Williams, Metal-semiconductor Contacts, second ed., Claredon, Oxford, 1988.
[3] J.H. Werner, Appl. Phys. A 47 (1989) 291.
[4] R.T. Tung, Phys. Rev. B 45 (1992) 13509.
[5] K. Akkilic, A. Turut, G. Cankaya, T. Kilicoglu, Solid State Commun. 125 (2003) 551.
[6] H. Cetin, B. Sahin, E. Ayyildiz, A. Turut, Semicond. Sci. Tech. 19 (2004) 1113.
[7] N. Tugluoglu, S. Karadeniz, S. Acar, M. Kasap, Chin. Phys. Lett. 21 (2004) 1795.
[8] N. Tugluoglu, S. Karadeniz, M. Sahin, H. Safak, Semicond. Sci. Tech. 19 (2004) 1092.
[9] N. Tugluoglu, S. Karadeniz, M. Sahin, H. Safak, Appl. Surf. Sci. 233 (2004) 320.
[10] S. Asubay, O. Gullu, B. Abay, A. Turut, A. Yilmaz, Semicond. Sci. Tech. 23 (2008) 035006.
[11] E. Gur, C. Coskun, S. Tuzemen, J. Phys. D. Appl. Phys. 41 (2008) 105301.
[12] O.F. Yuksel, Physica. B 404 (2009) 1993.
[13] W.C. Huang, S.H. Su, Y.K. Hsu, C.C. Wang, C.S. Chang, Super. Lattices Microstruct. 40 (2006) 644.
[14] W.C. Huang, T.F. Lei, C.L. Lee, Jpn. J. Appl. Phys. 42 (2003) 71.
[15] S. Chand, J. Kumar, Semicond. Sci. Technol. 10 (1995) 1680.
[16] S. Chand, J. Kumar, Appl. Phys. A 63 (1996) 171.
[17] S. Chand, J. Kumar, J. Appl. Phys. 80 (1) (1996) 288.
[18] Yi-Fei Huang, Yu-Long Jiang, Guo-Ping Ru, Xin-Ping Qu, Bing-Zong Li, Microelectron. Eng. 85 (2008) 2013.
[19] J. Kim, E.S. Lee, C.S. Han, Y. Kang, D. Kim, W.A. Anderson, Microelectron. Eng. 85 (2008) 1709.
[20] S. Demirezen, S. Altındal, Curr. Appl. Phys. 10 (2010) 1188.
[21] M.E. Kiziroglou, X. Li, A.A. Zhukov, P.A.J. de Groot, C.H. de Groot, Solid-State Electron. 52 (2008) 1032.
[22] M.E. Kiziroglou, A.A. Zhukov, X. Li, D.C. Gonzalez, P.A.J. de Groot, P.N. Bartlett, C.H. de Groot, Solid State Commun. 140 (2006) 508.
[23] O. Nakatsuka, K. Okubo, A. Sakai, M. Ogawa, Y. Yasuda, S. Zaima, Microelectron. Eng. 82 (2005) 479.
[24] S. Zhu, R.L. Van Meirhaeghe, S. Forment, G.P. Ru, B. Li, Solid-State Electron. 48 (2004) 29.
[25] F. Roccaforte, F. La Via, A. Baeri, V. Raineri, L. Calcagno, F. Mangano, J. Appl. Phys. 96 (2004) 4313.
[26] P.P. Sahay, M. Shamsuddin, R.S. Srivastava, Microelectron. J. 23 (1992) 625.
[27] V. Saxena, R. Prakash, Polym. Bull. 45 (2000) 267.
[28] E.H. Nicollian, A. Goetzberger, Appl. Phys. Lett. 7 (1965) 216.
[29] B. Akkal, Z. Benamara, B. Gruzza, L. Bideux, Vacuum 57 (2000) 219.
[30] T.P. Chen, T.C. Lee, C.C. Ling, C.D. Beling, S. Fung, Solid State Electron 36 (1993) 949.
[31] M.Y. Ali, M. Tao, J. Appl. Phys. 101 (10) (2007) 103.
[32] J.H. Werner, H.H. Guttler, J. Appl. Phys. 69 (1991) 1522.
[33] Y.P. Song, R.L.V. Meirhaeghe, W.H. Laflere, F. Cardon, Solid-State Electron 29 (1986) 633.
[34] R.T. Tung, Mater. Sci. Eng. R. 36 (2001) 138.
[35] S. Altindal, S. Karadeniz, N. Tugluoglu, A. Tataroglu, Solid State Electron 47 (2003) 1847.
[36] V.V. Brus, A.K.K. Kyaw, P.D. Maryanchuk, J. Zhang, Prog. Photovolt. Res. Appl. 23 (2015) 1526.
[37] E.H. Nicollian, J.R. Brews, MOS Physics and Technology, Wiley, New York, 1982.