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# Light assisted multilevel resistive switching memory devices based on all-inorganic perovskite quantum dots

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## ABSTRACT

All-inorganic perovskite quantum dots (APQDs) have emerged as excellent materials which have been widely used in numerous micro-nano photoelectric devices. However, resistive random access memory (RRAM) devices based on APQDs are relatively scarce. In this work, RRAM based on $CsPbBr_3$ APQDs prepared by the solution processed method was fabricated at room temperature. The sandwich structure memory device shows high reproducibility, good data retention ability, and light assisted multilevel storage capability. The resistance ratio (ON/OFF) of the RRAM device between the high resistance state and the low resistance state reaches almost $10^7$. Additionally, the device exhibits high performances under low power consumption—low reading voltage (−0.3 V) and operation voltage (−2.4 V/1.55 V). It is suggested that the connection and rupture of conducting filaments, which are formed by Br vacancies under an electric field, are responsible for the resistive switching effect. Our work provides an opportunity to develop the next generation high-performance and stable nonvolatile memory devices.



Resistive random access memory (RRAM), as one of the most promising next-generation nonvolatile memory devices, has attracted increasing attention due to its simple sandwich architecture, good endurance, fast switching speed, retention properties, low power consumption, high storage density, and complementary-metal-oxide-semiconductor (CMOS) compatibility.[1,2] The structure of RRAM is a traditional metal-active layer-metal sandwiched structure, in which the active layer acts as the switching media. In terms of switching media, on the one hand, a large number of amorphous Si, carbon-based materials,[3,4] oxides,[5–7] and even 2D and quantum dots (QDs) materials have demonstrated excellent resistive switching (RS) performance,[8–12] but they are often synthesized via expensive processing. On the other hand, $ABO_3$ type ceramic perovskites, including $BaTiO_3$, $SrRuO_3$, $SrZO_3$, and $SrTiO_3$, have been widely used as switching materials for RRAM devices.[13–17] However, the high temperature fabrication process limits the future applications of ceramic perovskites.

Recently, resistive switching devices based on hybrid methylammonium (MA) lead halide perovskites ($MAPbX_3$, X: I, Br, Cl, or their mixtures) have been demonstrated and attracted enormous attention due to their remarkable physical properties, such as bandgap tunability, ambipolar charge transport, long charge diffusion length, and magnetism.[18–24] However, the intrinsic thermal instability of MA was really a limitation for the development of hybrid MA lead halide perovskite based electronic devices.[25] In order to overcome the disadvantage, replacing the organic cation with an inorganic cation such as Cs was attempted and reported.[26,27] All-inorganic perovskites $CsPbX_3$ (X: I, Br, Cl), reported for a broad range of photovoltaic and transistor devices, including solar cells, photodetectors, and light emitting diodes,[26–31] have remained stable above 100 °C structurally and thermally. Thus, these materials are expected to obtain thermally stable perovskite resistive switching memories with low cost.[32–36]

Conventional memory technologies use only a single physical quantity (electrical) input to operate memory devices. But to achieve high density data storage, the multilevel memory approach, which combines multiple physical quantities (such as optical, electrical, and magnetic) on a single device, is an effective alternative method.[37–39] All-inorganic perovskites, especially All-inorganic perovskite quantum dots (APQDs), have better electronic and optical properties than traditional bulk materials, Perovskite materials.[10,18,27,40,41] Besides, the APQDs layer contains many kinds of point defects, including vacancies, interstitials, and substitutions, which have low formation energies. Many experimental studies have verified that the migration of vacancies can be controlled by the electric field or light.[20,42] As a result, accumulation of a high concentration under an electric field or light illumination can form conduction channels and cause a decrease in resistance of the memory device. Therefore, RRAM based on APQDs can combine optical and electrical properties on a single device, which can achieve multilevel memory and high density data storage.[42] In this work, we present a sandwiched light assisted multilevel RRAM based on $CsPbBr_3$ APQDs by the solution processed method. The $CsPbBr_3$ APQDs served as the active material, sandwiched between the bottom indium-tin oxide (ITO) and top Au electrodes, respectively. Our $CsPbBr_3$ QDs based RRAM shows great reproducibility, good data retention ability, and light assisted multilevel storage capability. The resistance ratio (ON/OFF) of the RRAM device between the high resistance state (HRS) and low resistance state (LRS) can reach almost $10^7$. Additionally, the device exhibits high performances under low power consumption—low reading voltage (−0.3 V) and operation voltage (−2.4 V/1.55 V). What is more, due to the fact that the resistance of HRS can be controlled by an incidence 405 nm laser, the device shows light assisted multilevel storage capability. Conductive atomic force microscopy (C-AFM) measurements confirm that the formation and rupture of conducting filaments were responsible for the RS of the APQDs based memory device. To study the $CsPbBr_3$ QDs based RRAM provides an opportunity to develop the next generation high-performance and stable nonvolatile memory devices.

Figure 1(a) shows the schematic diagram of the $CsPbBr_3$ QDs based RS device structure by the Layer-by-layer assembling method. First, a glass with an ITO film was precleaned sequentially using deionized water, propanol, and ethanol in an ultrasonic bath, each for 10 min. Then, five layers of $CsPbbr_3$ QDs were spin-coated on the ITO film by the Layer-by-layer method from toluene solution at 2000 rpm for 60 s. The detailed synthesis method of $CsPbBr_3$ QDs is provided in the supplementary material. At last, the Au electrode was deposited on the top by thermal evaporation through a shadow mask. In the current-voltage (I-V) characteristic measurement, a source measure unit (Keithley 2400) was used to supply the bias voltage between the top and bottom electrodes. The ultraviolet-visible (UV-Vis) absorption and photoluminescence (PL) spectra of the prepared $CsPbBr_3$ QDs were measured using a Zolix-$\lambda$300 spectrometer. All of the measurements were performed at room temperature and in an ambient environment. The cross-sectional scanning electron microscopy (SEM) image of the memory device is shown in Fig. 1(b). The thickness of the $CsPbBr_3$ QDs layer is about 400 nm. The smooth surface of the $CsPbBr_3$ QDs layer is confirmed by the atomic force microscopy (AFM) image as depicted in Fig. S1(a). Figure S1(b) presents the AFM image of the topography of the $CsPbBr_3$ QDs single layer and the average size of the quantum dots is about 15 nm. Figure 1(c) shows the

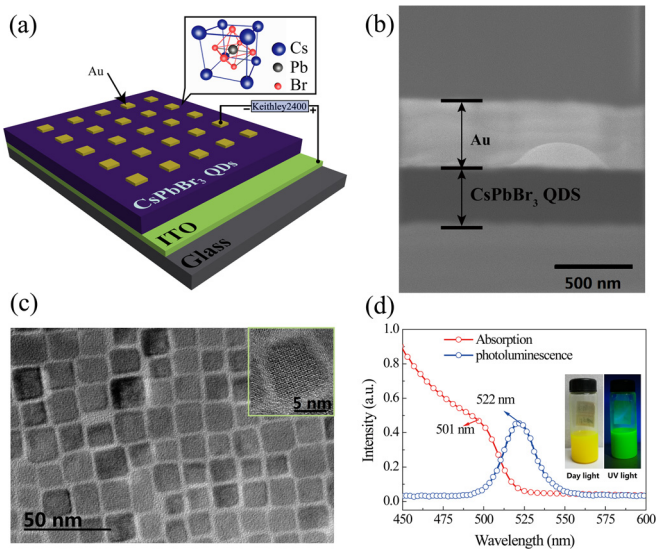


**FIG. 1.** (a) Schematic of the configuration of $CsPbBr_3$ QDs based resistive switching device. (b) Cross-sectional scanning electron microscopy image of the $CsPbBr_3$ QDs based resistive switching device. (c) TEM image of $CsPbBr_3$ QDs and the corresponding high resolution TEM image. (d) The absorption (Abs) and photoluminescence (PL) of $CsPbBr_3$ QDs. The right illustration is the images of $CsPbBr_3$ QDs solution in day and UV light.

transmission electron microscopy (TEM) image of $CsPbBr_3$ QDs and the high resolution TEM image. The interplanar distance and Fast Fourier transformed micrograph of $CsPbBr_3$ quantum dots are shown in Figs. S2(a) and S2(b). All the TEM images illustrate the cubic perovskite structure with an average size of about 15 nm and high crystalline quality of $CsPbBr_3$ QDs. The X-ray diffraction (XRD) pattern of the $CsPbBr_3$ QDs sample is shown in Fig. S3. The characteristic diffraction peak is 30.72° corresponding to the (200) crystal plane of cubic $CsPbBr_3$. Figure 1(d) shows the UV-Vis absorption and PL spectra of the prepared $CsPbBr_3$ QDs and the right illustration shows the images of $CsPbBr_3$ QDs solution in day and UV light. The sharp PL spectra and obvious exciton absorption peak suggest that the particle size of $CsPbBr_3$ QDs is uniform. Figure 2(a) displays the *I-V* characteristics for the $CsPbBr_3$ QDs based memory device under the voltage sweep sequence of 0 V → −3 V → 0 V → 3 V→ 0 V. Initially, the state of the device was HRS (or OFF state) and the current was nearly $10^{-7}$ mA under the read voltage of −0.3 V. When the external voltage was swept from 0 V → −3 V →0 V, the device switches to a LRS (or ON state) at around −2.4 V and the current dramatically increases to 1 mA under the same read voltage of −0.3 V. The ON/OFF ratio was about $10^7$. This process is termed as the SET process and then the LRS maintains until the RESET voltage was applied. When the external voltage swept from 0 V → 3 V→ 0 V, the resistance transits from LRS to HRS at around 1.55 V, which means that the RESET process occurs. The bias voltage of SET and RESET is opposite, indicating that the devices exhibit bipolar RS characteristics.

The switching voltage distribution of the $CsPbBr_3$ QDs memory is shown in Fig. 2(b). The RESET and SET voltages are distributed in ranges of 0.1 V–1.6 V and −0.4 V to −3.9 V, respectively. The distribution of RESET voltage is much more concentrated than those of SET

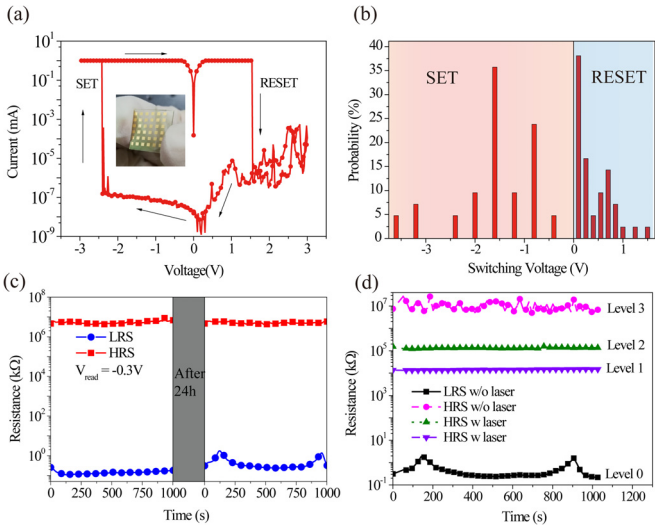


**FIG. 2.** (a) Resistive switching property of the device based on $CsPbBr_3$ QDs. During SET and RESET, a compliance current of 1 mA was applied to prevent the device from hard breakdown. The middle inset is the photograph of the memory device. (b) Histograms of the SET/RESET switching voltage during 50 times tests. (c) Retention characteristics of LRS and HRS states, and the reading voltage for all resistive states is −0.3 V. The ON/OFF ratio is almost $10^7$. (d) Multilevel operation with light illumination. The measurement applied back illumination, that is, the 405 nm laser through the ITO glass and incidence to the active layer. The incidence 405 nm laser power density of levels 1 and 2 is about 80 mW/cm$^2$ and 30 mW/cm$^2$, respectively.

voltages. The possible reason is that in the process of each SET, the conducting channel is formed in different positions and tends to be more random, but in each RESET, the rupture of filaments is only for filaments that have been formed. In order to study the electrical reliability of the memory device, data retention characteristics of LRS and HRS in the $CsPbBr_3$ QDs based memory device were measured with a reading voltage of −0.3 V. As shown in Fig. 2(c), the ON/OFF ratio is nearly $10^7$. The LRS and HRS values are almost the same even after 1000 s. After 24 h retest, there is a slight fluctuation in the values of the LRS and HRS , but the ON/OFF ratio remained unchanged. At the same time, we test the stability of the memory device under a continuous read pulse and the result is shown in Fig. S4. After 500 quick read tests, the resistances of the device in HRS and LRS still remain very stable. Then, we test the reproducibility of the memory device. The distribution of the LRS current and HRS current of 20 different RRAM cells in three substrates is shown in Fig. S5. The LRS currents of 20 RRAM different cells all distributed in the range from 0.1 mA to 1 mA [Fig. S5(a)], and most of the HRS currents concentrate in near $10^{-7}$ mA [Fig. S5(b)]. The LRS/HRS current ratios are almost concentrated in near $10^7$.

Multilevel storage capability is an attractive approach to realize cost-effective high density memory. In RRAM, the most common way is to control the different current compliances. We first test the I-V curves under different current compliances, and the results are displayed in Fig. S6. The SET and RESET voltages of the RRAM device decreased with the decrease in the current compliance and different LRS with nearly the same HRS were obtained when current compliance varied from $10^{-3}$ mA to 1 mA. The results indicated that the device based on $CsPbBr_3$ QDs shows electronic controlled multilevel storage ability. As mentioned above, the $CsPbBr_3$ APQDs are excellent photoelectric materials and the optoelectronic characteristics are illustrated in Fig. S7. From Fig. S7, a pronounced increase in photocurrent ($I_{ph} = I_{illuminated} - I_{dark}$) was observed when the device was illuminated by the laser, which suggests that the device has a strong, repeatable, and stable response to the light illumination. Therefore, we next explored the multilevel data storage capability of HRS at different incidence laser power densities. The retention ability of the memory device under dark and laser illumination is shown in Fig. 2(d). As shown in the figure, the different resistances can be well maintained for more than 1000 s. When the power densities of the 405 nm laser were 0, 30 mW/cm$^2$, and 80 mW/cm$^2$, the resistances of HRS were about $10^7$ kΩ, $10^5$ kΩ, and $10^4$ kΩ, respectively. The results suggest that the resistance of HRS can be modulated by tuning the power density of the incidence laser, showing the multilevel resistance ($10^4$ kΩ, $10^5$ kΩ, and $10^7$ kΩ for level 1, level 2, and level 3, respectively) at HRS and LRS (level 0). From the photocurrent–voltage (I-V) characteristics shown in Fig. S7, it can be found that the slopes of the I-V curves gradually increase with the increase in light intensity. Thus, light assisted multilevel data storage is possibly attributed to the photoconductive effect. When the 405 nm laser, whose photon energy is higher than the bandgap of $CsPbBr_3$ QDs, reached the $CsPbBr_3$ QDs layer, electron-hole pairs are generated and then they are divided and drifted toward the two electrodes under the electric field (read voltage). As a result, the output current increases and the resistance decreases. The number of photon generated electron-hole pairs is proportional to the power of the laser. Thus, the device can realize light assisted multilevel data storage.

In previous research, many mechanisms were presented to explain the RS in memory devices, such as ion migration,[19,20] trap-controlled space-charge-limited conduction (SCLC),[21,42] and conduction filaments.[43,44] However, the possible intrinsic mechanisms are still divergent. In this work, we plotted the *I-V* characteristics of SET and RESET processes in double logarithmic coordinates in Figs. 3(a) and 3(b) to explore the mechanism. When the device is in LRS, the relationship between current and voltage follows Ohm's law ($I \propto V^1$). However, when the device is in HRS, the I-V characteristics show two distinct linear regions at low voltage in which the relationship almost follows Ohm's law ($I \propto V^1$) and a region at high voltage in which this relationship conforms to the SCLC law ($I \propto V^2$). The different *I-V* characteristics between HRS and LRS suggest that the conduction filament was formed in the $CsPbBr_3$ QDs layer. For the perovskite layer,

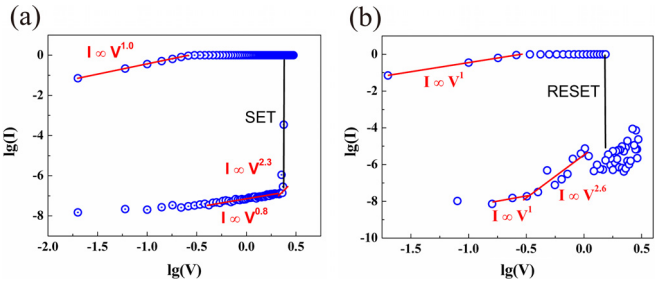


**FIG. 3.** Measured and fitted *I-V* curves of the perovskite resistive switching memory device. (a) *I-V* curves of the SET process. (b) I-V curves of the RESET process.

Cs vacancies, Pb vacancies, and Br vacancies can be formed during the fabrication of the memory device.[22,45] The migration of different kinds of ions under an electric field leads to the redistribution of the corresponding vacancies in the $CsPbBr_3$ QDs layer. The aggregation of these vacancies may form along line defects and the line defects can form some local conductive channels.[46,47] These local conductive channels connect each other under an electric field and through the entire perovskite layer, and thus, the device transits from HRS to LRS. Besides, the aggregation of vacancies also reduces the Schottky barrier height at the interface between the ITO electrode and the perovskite layer. As mentioned above, the conduction filaments are most possibly provided by Br vacancies, because of their lowest activation energy.[22,31] Initially, a lot of Br vacancies distribute in the $CsPbBr_3$ QDs layer [Fig. 4(a)] and the Br vacancy conductive channels have not formed yet, and thus, the active layer is in the HRS. At the same time, as shown in Fig. S8(a), the Schottky barrier formed between the ITO electrode and the $CsPbBr_3$ QDs layer also makes the device difficult to conduct. When a negative voltage is applied, the $Br^-$ ions are attracted to the anode (Au electrode) and this process creates a lot of Br vacancies in the $CsPbBr_3$ QDs layer, and the highest Br vacancy concentration is near in the cathode (ITO electrode). Continuously increasing the bias voltage will cause the expansion of Br vacancy rich regions toward the anode and eventually form a conduction channel bridging the two electrodes, and the height of the Schottky barrier is also reduced [Fig. S8(b)]. Therefore, the electrons can migrate by vacancy to vacancy hopping and the device is in LRS, as schematically shown in Fig. 4(b). This is the SET process. When an opposite voltage is applied, the conduction channel of Br vacancies will be ruptured due to the $Br^-$ migration back and the device is in HRS, as shown in Fig. 4(c). This is the RESET process. In order to provide experimental evidence of the conducting filamentary mechanism of the device, the C-AFM measurement was carried out.[48,49] The result is shown in Fig. S9. Initially, the film was in the HRS state and there was no obvious current under a voltage of 1 V [Fig. S9(a)]. When applying a 5 V bias, several highly conductive areas were observed in the current map. It indicates that the resistance of the film undergoes transition from HRS to LRS. The measurement results confirm that the formation and rupture of conducting filaments were responsible for the RS of the APQDs based memory device.

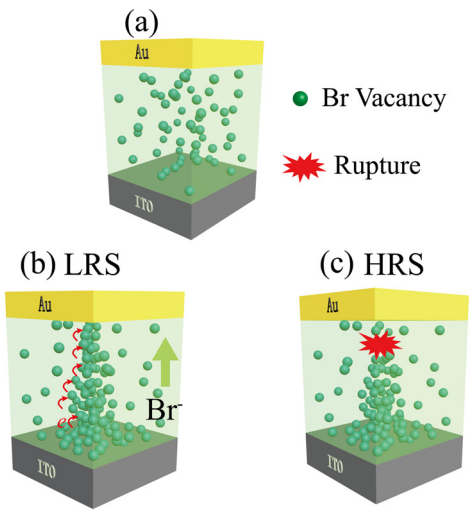


**FIG. 4.** Schematic diagrams for the mechanism of the resistive switching process in the device.

In summary, we reported a sandwiched structure RRAM based on $CsPbBr_3$ APQDs by the solution processed method. The resistive memory device shows bipolar RS characteristics with a low operation voltage of about −2.4 V/1.55 V, a high ON/OFF ratio of $10^7$, a long data retention of over 1000 s, and light assisted multilevel storage capability. The C-AFM measurement confirmed that the LRS and HRS transition originates from the formation/rupture of the conducting channel. This work is benefit to understanding the resistive switching characteristics in the $CsPbBr_3$ QDs based RRAM devices, which have great potential applications in the future.

See supplementary material for the $CsPbBr_3$ synthesis and the used materials, AFM and TEM images of the $CsPbBr_3$ QDs, stability test of the memory device under a read pulse, XRD pattern of the $CsPbBr_3$ QDs sample, sector graph of the LRS and HRS current statistical distribution, resistive switching property of the device based on $CsPbBr_3$ QDs at different compliance currents, photocurrent–voltage (I-V) and photoswitching characteristics of the memory device, the Schottky barrier between the ITO electrode and perovskite layer, and C-AFM measurement results under varied bias voltages applied on the C-AFM tips.

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The authors declare no competing financial interest.

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