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Review

Deep depletion capacitance–voltage technique for spatial distribution of traps across the substrate in MOS structures

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ABSTRACT

It is important to characterize the distribution of spatial traps in the MOS structure for separating the interface states from the subgap density-of-states. In this study, we report a characterization technique for the spatial distribution of traps using the C-V characteristics under deep-depletion bias. Depletion capacitance is determined by the depletion depth (X_d) and the dielectric constant with the MOS structure. Thus, the distribution of spatial depletion charges can be identified if only the depletion capacitance can be separated from the measured gate capacitance. In the case of MOS structure with spatial traps in the element, it will show a deviated characteristic from the ideal depletion capacitance. Therefore, this allows us to characterize the spatial distribution of traps in MOS structures. The spatial distribution of traps from a single crystal silicon MOS capacitor was extracted $N_{trap,max} = 3.45 \times 10^{18}$ cm^{-3} ass the maximum value in the interface, indicating that the concentration tends to decrease more in the substrate direction.

1. Introduction

As electronic devices are scaled down, the ratio of trap charges to total charges in the substrate channel region is increasing. Therefore, the change in the electrical characteristics of devices due to the trap is increasing. For this reason, characterization and modeling of traps and interface states in MOS structure become increasingly important [1–10]. As a result, the demand for the characteristics of spatial distribution and energy distribution of the subgap ($E_V < E_t < E_C$) density of state (DOS) in MOSFETs (metal–oxidesemiconductor field effect transistors) and TFTs (thin-film transistors) with insulated gate structures is increasing [11–14]. Previous Trap research reports have focused on energy distribution [11–14]. With non-destructive C-V characterization of vertical trap location in LTPS TFTs and MOSFETs, it allows systematic characterization of the grain boundary location in LTPS TFTs and the trap locations caused by fabrication process and/or degradation through electrical stress in the channel of TFTs and MOSFETs. This allows more intuitive and systematic characterization of spatial location as well as the energy distribution of traps and interface states in FETs. This is expected to be useful for device reliability analysis and provide systematic guidance in the process improvement. Recently there was a report on the separation of the bulk DOS from the interface states [15]. However, this study requires several devices with different substrate thickness assuming a fixed bulk DOS even for devices rather than a single device. In general, both the concentration and the distribution of traps depend strongly on the thickness of the active layer and the manufacturing process. Therefore, it is difficult to accurately extract traps if the device is not a single device in the characterization process. Another report suggests a theoretical model, and extraction is conducted using the calculated results [16,17]. This method requires a complicated calculation process and inherently carries various error factors.

For comprehensive characterization traps over the energy bandgap, a two-dimensional distribution must be known for space and energy. If there is a technique for separated extraction, as mentioned above, it will be very helpful in the characterization of traps for implementation of robust MOSFETs and TFTs.

Therefore, we report a novel technique for characterizing the vertical spatial distribution of traps for each single MOS device. We combined the capacitance model with experimental capacitance–voltage (C–V) data obtained through the deep depletion mode of bias. Thus, allows extended modulation of the depletion of the substrate suppressing the pinning of the surface potential by the inverted carriers in slow sweep

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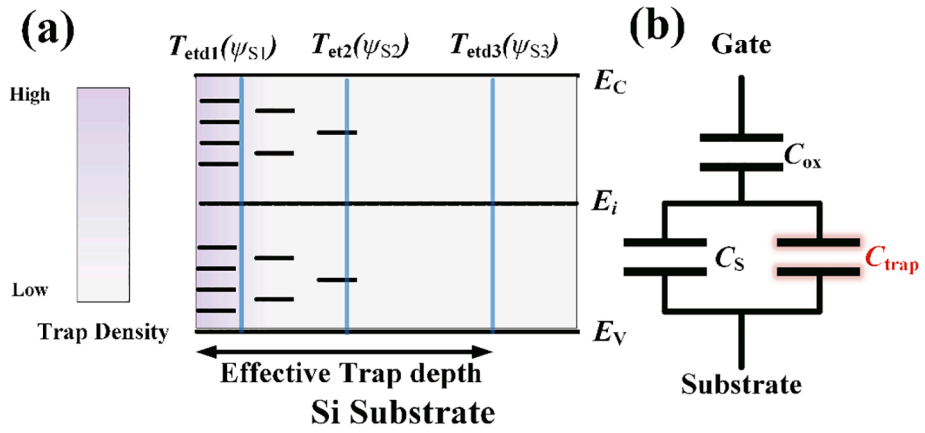

Fig. 1. (a) Schematic of a MOS structure with spatial trap distribution. (b) Equivalent capacitance circuit model with substrate capacitance (C_S) and trap capacitance (C_{trap}) for the MOS structure.

measurement. We expect that the proposed C–V technique for the spatial distribution of traps is useful to the quantitative and reliable analysis of traps linking the electrical characteristics to the process parameters in MOS-based devices.

2. Experimental

The equivalent capacitance (C_G) for the insulated gate structure (MOS and MIS) is modeled by a series connection of the oxide capacitance (C_{ox}: bias-independent) and the substrate capacitance (C_S: bias-dependent). The bias-controlled surface potential (ψ_s)-dependent substrate capacitance ($C_S(\psi_s) = C_{SD}(\psi_s) + C_{trap}(\psi_s)$) is a parallel connection of the depletion capacitance (C_{SD}) for the depleted dopants in the substrate with the trap-induced capacitance (C_{trap}). In the absence of traps over the substrate, the substrate capacitance is solely determined by the depletion capacitance ($C_S(\psi_s) = C_{SD}(\psi_s)$) under the depletion state of the gate bias ($0 < \psi_S < \phi_f$) is inversely proportional to the square root of the surface potential with ϕ_f as the bulk fermi potential. However, this relation is different when traps are introduced. This is because the effective trap depth (T_{etd}) increases with the change of the surface potential, with the trap in the energy band bent region affecting device capacitance as shown below in Fig. 1(a).

The capacitance for the MOS structure in MOSFETs and TFTs can be modeled as

$$\frac{1}{C_{gp}(\psi_S)}\ [\mathrm{F}^{-1}] = \frac{1}{C_S(\psi_S)} + \frac{1}{C_{ox}} \tag{1}$$

$$C_{ox}\ [\mathrm{F}] = \frac{\epsilon_{ox}}{t_{ox}} A_g; A_g\ [\mathrm{cm}^2] \equiv WL \tag{2}$$

$$C_S(\psi_S)\ [\mathrm{F}] \equiv C_{SD}(\psi_S) + C_{trap}(\psi_S) \tag{3}$$

$$C_{SD}(\psi_S)\ [\mathrm{F}] \equiv \frac{dQ_{SD}(\psi_S)}{d\psi_S} = \frac{\epsilon_{si} A_g}{T_{dep}(\psi_S)} = A_g \sqrt{\frac{qN_{sub}\epsilon_{si}}{2}\frac{1}{\psi_S}} \tag{4}$$

$$C_{trap}(\psi_S)\ [\mathrm{F}] \equiv \frac{dQ_{trap}(\psi_S)}{d\psi_S} = \left(\frac{dQ_{trap}(\psi_S)}{dT_{dep}(\psi_S)}\right)\left(\frac{dT_{dep}(\psi_S)}{d\psi_S}\right) \tag{5}$$

with ϵ_{ox} as the dielectric constant of the gate insulator, t_{ox} as the oxide thickness, ϵ_{si} as the dielectric constant of the substrate (i.e., silicon), q as the absolute charge of an electron, A_g as the gate area, and N_{sub} as the substrate doping concentration.

We note that the depletion depth (X_d) can be mapped to the spatial location as

$$X_d(\psi_S) = \sqrt{\frac{2\epsilon_{si}}{qN_{sub}}\psi_S} = A_g\frac{\epsilon_{si}}{C_{SD}(\psi_S)} \tag{6}$$

The depletion depth is dependent on the surface potential and modulated by the gate voltage. Assuming the density of trap is comparable to or less than the substrate doping concentration, the effective trap depth (T_{etd}) from the substrate capacitance (C_S) using can be obtained through

$$T_{etd}(\psi_S)\ [\mathrm{nm}] = A_g\frac{\epsilon_{si}}{C_S(\psi_S)} \approx A_g\frac{\epsilon_{si}}{C_{SD}(\psi_S)} \tag{7}$$

In the absence of traps with $C_{trap} = 0$, the ideal gate capacitance (C_{gi}) relationship under depletion mode of bias can be simplified as

$$\left(\frac{1}{C_{gi}(\psi_S)} - \frac{1}{C_{ox}}\right)^2 [\mathrm{F}^{-2}] = \left(\frac{1}{C_{SD}(\psi_S)}\right)^2 = \frac{2}{A_g^2 q\epsilon_{si}N_{sub}}\psi_S \tag{8}$$

and linearly proportional to the surface potential. On the other hand, with traps in the substrate, the practical gate capacitance (C_{gp}) can be expressed as

$$\frac{1}{C_{gp}(\psi_S)}\ [\mathrm{F}^{-1}] = \frac{1}{C_{SD}(\psi_S) + C_{trap}(\psi_S)} + \frac{1}{C_{ox}} \tag{9}$$

with C_{trap} as the ψ_S-dependent capacitance for traps.

Comparing with a graph of the ideal C_{gi}-V without traps, we characterize the spatial distribution of the trap from the deviation of the practical C_{gp}-V curve with the trap from the C_{gi}-V curve without traps. In MOS structures with a constant doping concentration as in the crystalline substrate, it is expected that traps exist only near the interface and traps do not exist in the substrate region. In other words, the substrate capacitance has only the depletion capacitance ($C_S \cong C_{SD}$) under high gate bias during the fast sweep of C-V characterization under deep depletion state.

Assuming a negligible trap density in MOS structure, experimental C_S^{-2} at large gate bias can be extrapolated ($C_{SD,ext}$) to the small gate bias range. This makes possible to get C_{trap} by the traps near the Si/SiO_2 interface from the difference ($\Delta Q_{trap}(\psi)$) for the differential change of the surface potential ($\Delta\psi_S$) by the gate bias in the experimental C-V data through

$$Q_{trap}(\psi_{Sn})[C] = qWL\sum_{k=1}^{n} N_{trap}(\psi_{Sk})\Delta T_{etd}(\psi_{Sk}) \tag{10}$$

$$\Delta Q_{trap}(\psi_S)\ [\mathrm{C}] = Q_{trap}(\psi_S + \Delta\psi_S) - Q_{trap}(\psi_S) \tag{11}$$

$$C_{trap}(\psi_S)\ [F] = \left(C_{gp}^{-1}(\psi_S) - C_{ox}^{-1}\right)^{-1} - C_{SD,ext}(\psi_S) \tag{12}$$

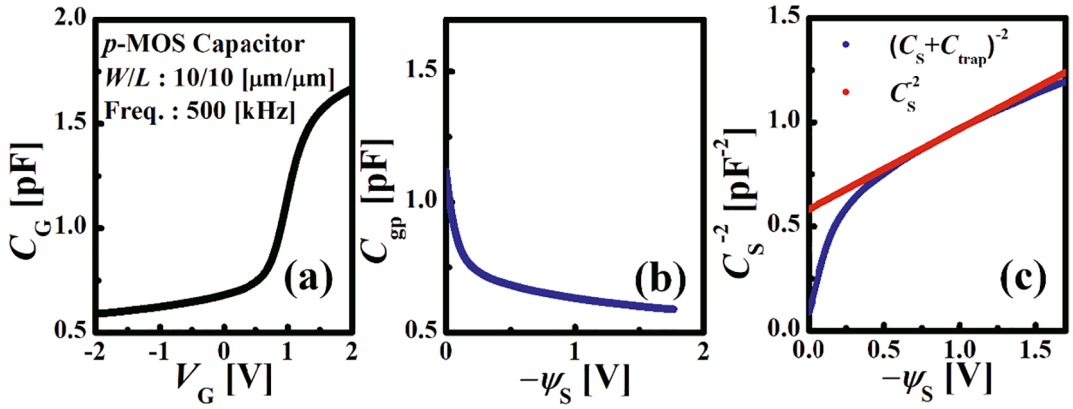

Fig. 2. (a) Measured C–V characteristics under deep depletion mode of gate bias with fast sweep (50 mV/s) mode. (b) Measured C-ψ_S characteristics. (c) Experimental C_S^{-2} versus ψ_S curve for extraction of the trap distribution from the deviated C–V curves.

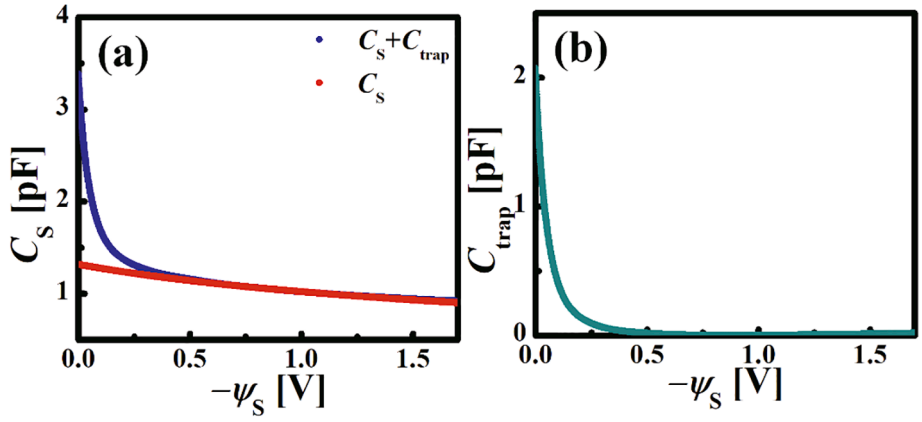

Fig. 3. Experimental capacitance including trap influence (blue) and not including trap influence (red). (b) Extracted trap capacitance (C_{trap}). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

with $Q_{trap}(\psi_S)$ as the trap charge change at the effective trap depth (T_{etd}) for the surface potential. This finally allows us to obtain the spatial distribution of the trap ($N_{trap}(\psi_S)$ [cm^{-3}]) through

$$C_{trap}(\psi_S) = \frac{dQ_{trap}(\psi_S)}{d\psi_S} = qWLN_{trap}(\psi_S)\frac{\Delta T_{etd}(\psi_S)}{\Delta\psi_S} \tag{13}$$

$$N_{trap}(\psi_S)\ [\mathrm{cm}^{-3}] = \frac{C_{trap}(\psi_S)}{qWL} \times \left(\frac{\Delta T_{etd}(\psi_S)}{\Delta\psi_S}\right)^{-1} \tag{14}$$

with W as the gate width and L as the gate length, and $\Delta T_{etd}(\psi_S)$ as the bias-dependent differential change of the effective trap depth of the MOS device under C–V characterization.

3. Results and discussion

We employed silicon MOS capacitors with n-type substrate (constant doping: $N_{sub} = N_D = 2.6 \times 10^{19}$ [cm^{-3}]) with $W/L = 10/10$ [μm/μm] and $t_{ox} = 20$ [nm] for experimental application of the proposed C–V technique. We first obtained experimental C–V data for the device through fast sweep mode of measurement for extended modulation of

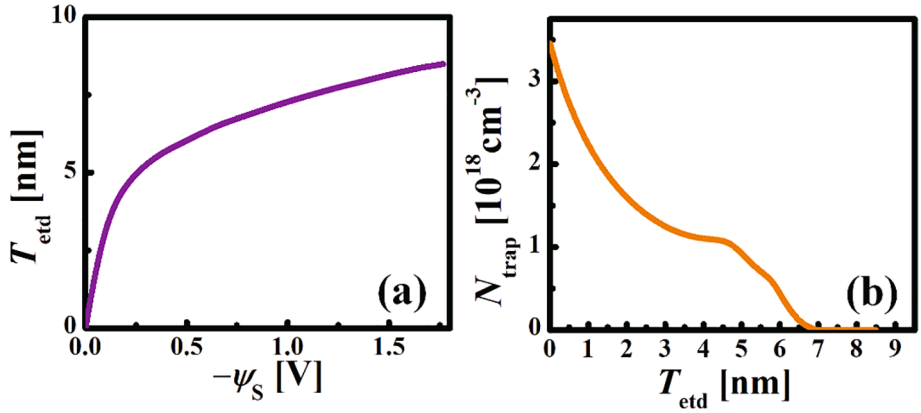

Fig. 4. (a) Effective trap depth as a function of the surface potential. (b) Spatial distribution of traps ($N_{trap}(T_{etd})$ [cm^{-3}]) in MOS capacitor with n-type substrate.

effective trap depth the substrate as shown in Fig. 2(a). The V_G-dependent surface potential ($\psi_S(V_G)$) is mapped from the experimental C–V data through

$$(V_G - V_{FB})\ [\mathrm{V}] \cong \psi_{ox}(V_G) + \psi_S(V_G) \tag{15}$$

$$\psi_S(V_G)\ [\mathrm{V}] = \int_{V_{FB}}^{V_G} \left(1 - \frac{C_g(V_G)}{C_{ox}}\right) dV_G \tag{16}$$

Combining Eq. (15) with Eq. (8), we obtain Fig. 2(c) applicable to Eq. (10) for the trap capacitance. When the surface potential is large, C_S^{-2} is linearly proportional to the surface potential. We also note that considerable deviation of the experimental data from extrapolated straight line is observed due to high density of traps near the Si/SiO2 interface.

Next, we extracted the trap capacitance from the difference between the C–V data with traps and that without traps. In Fig. 3(a), we plotted $C_S = C_{SD} + C_{trap}$ with the extrapolated depletion capacitance ($C_S = C_{SD,ext} = C_{SD}$ with $C_{trap} = 0$) as a function of the surface potential. Finally, we experimentally obtained the trap capacitance through Eq. (10) as shown in Fig. 3(b).

We also note that the substrate capacitance (C_S) is obtained from the experimental C-V data and we obtained T_{etd} nm from the C_S by Eq. (7). For spatial distribution, we mapped the surface potential to the effective trap depth through Eq. (7) as shown in Fig. 4(a). As shown in Fig. 4(b), we finally obtained the trap distribution as a function of the effective trap depth in the MOS capacitor with $N_{trap,max}$ at the Si/SiO2 interface.

4. Conclusion

In this work, a C-V technique is reported for characterization for the spatial distribution of traps across the substrate in MOS structures. A fast sweep mode of C-V measurement was employed for deep and extended depletion of the substrate. From the deviation of the experimental C-V data with traps from the ideal C-V curve, the spatial distribution of the traps across the substrate from the Si/SiO_2 interface is obtained through the equivalent capacitance model. Using the deep depletion mode C-V technique for extended characterization of traps, we extracted the trap distribution across the substrate in uniformly doped MOS structure and obtained the maximum of the trap density to be $N_{trap,max} = 3.45 \times 10^{18}$ cm^{-3}. By modifying this technique, we expect that both energy and spatial distributions of subgap traps in poly- and amorphous semiconductor can be extracted for MOSFETs and TFTs.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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