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APPARATUS AND DEMONSTRATION NOTES

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Department of Physics, Reed College, Portland, OR 97202

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Capacitance-voltage profiling of MOS capacitors: A case study of hands-on semiconductor testing for an undergraduate laboratory

J. Joy, M. P. Date, B. M. Arora, K. L. Narasimhan, and S. Tallur[a)]
Department of Electrical Engineering, IIT Bombay, Mumbai, MH 400076, India

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Catering to a large undergraduate laboratory class requires the experiments to be robust, low maintenance, and easy to set up with low cost test equipment at the disposal of most university laboratories. Most introductory undergraduate semiconductor device laboratory courses utilize packaged semiconductor integrated circuit chips to illustrate the functioning and applications of fundamental semiconductor devices such as diodes and transistors. While such methods do justice to the illustration of device concepts, the packages abstract the device physics and manufacturing and promote a "black-box" mentality towards device engineering. We have proposed and implemented a novel undergraduate device laboratory experiment, where metal oxide semiconductor capacitor (MOSCAP) devices were designed and fabricated at our university cleanroom and provided to students to perform basic capacitance-voltage profile measurements. To allow over a hundred students to simultaneously perform the experiments, we fabricated miniature test jigs that served as probe stations with spring-loaded pogo pins to make electrical contact with the devices. Using a simple op-amp based circuit that is easy for second year undergraduates to analyze, students are able to successfully extract device parameters such as substrate doping density and flat-band voltage using this experiment, and visualize the different modes of operation of a MOSCAP. © *2018 American Association of Physics Teachers.*
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I. INTRODUCTION

Advances in semiconductor technology have greatly accelerated the development and proliferation of electronics in everyday life. The introduction of integrated circuits (ICs) as a result of extensive directed investments in CMOS processing led to miniaturization and driving down of manufacturing costs of this technology. Considering the impact of this technology in all walks of life, it is no surprise that a course on semiconductor device physics commonly forms a key component of undergraduate curricula in physics, electrical and electronics engineering. While device physics and fabrication are easily taught in a classroom setting, the success of IC technology has also partly hindered efforts to have students appreciate the device fabrication and back-end processing in a laboratory setting. Most undergraduate laboratory courses use packaged ICs for experiments to familiarize students with basic semiconductor devices such as p-n diodes, bipolar junction transistors (BJTs), and metal-oxide-semiconductor field effect transistors (MOSFETs). It is easy to interface these ICs to measurement equipment and power supplies by assembling all required components on bread-boards. Laboratory experiments are made interesting and effective by focusing on teaching students how to characterize these devices through current-voltage (I-V) profile measurements and building basic application circuits using these devices such as rectifiers, amplifiers, and MOS inverter. Consequently, most undergraduate students do not obtain hands-on experience in characterization of bare (unpackaged) devices as part of their curricula, and develop a "black-box" mentality towards device engineering.

We sought to challenge the norm in undergraduate semiconductor device laboratory education by designing and setting up an experiment where a class of 140 students, working in pairs, perform capacitance-voltage (C-V) profile measurement of unpackaged metal-oxide-semiconductor capacitors (MOSCAPs) using miniature probe stations. The MOSCAP is chosen for this experiment as the study of MOS transistors starts with understanding the principle of operation of the MOSCAP. Moreover, it is the simplest two terminal device

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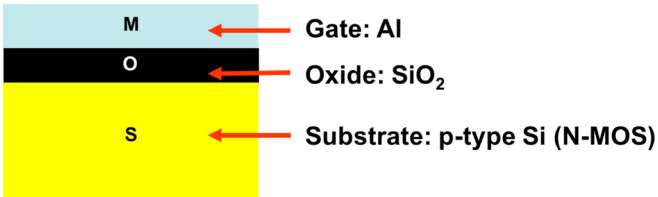

Fig. 1. Illustration of the different materials in a MOSCAP.

that can be fabricated in a university cleanroom to educate students about most concepts pertaining to MOSFETs, as detailed in Sec. II. The primary challenges required to be addressed were the fabrication of multiple devices in our university cleanroom (IITBNF), designing a repeatable and reproducible measurement scheme and a foolproof, robust measurement jig that could be replicated on multiple lab benches simultaneously to enable the entire class to perform the experiment during the stipulated laboratory slot. Section II describes the underlying theory governing the operation of MOSCAPs, and Secs. III–VI discuss the fabrication process flow for the devices, design of the measurement circuit, measurement jigs, and analysis of experimental observations. Our main emphasis has been on teaching the underlying principle of C-V measurement to a large class. Essentially, this is done using commonly used lab equipment in an undergraduate electronics lab and not using expensive semiconductor parameter analyzers and probe stations, conventionally used for such testing. Moreover, this also allows us to walk the students through capacitance measurement circuit techniques which are otherwise abstracted by sophisticated test equipment.

II. PRINCIPLE OF OPERATION OF THE MOSCAP

A. Relevance of MOSCAP characterization in an undergraduate lab

Before embarking upon explaining how a MOSCAP functions, it is necessary to understand why this device is relevant in advanced undergraduate or graduate lab curricula. The MOSCAP can be visualized as a metal-oxide-semiconductor sandwich. The most common MOS structures contain silicon as the semiconductor, silicon dioxide as the oxide, and aluminum as the metal. Since the metal plate is used to apply electric fields that alter the behavior of the MOSCAP, this terminal is also referred to as the gate, as shown in Fig. 1. Unlike an ideal capacitor that undergraduates may be familiar with from their introductory circuits courses, the capacitance of a MOSCAP depends on the electric field in the device (and thereby, the potential difference across the plates), due to band bending in the semiconductor, which leads to voltage dependent change in charge concentration at the semiconductor-dielectric interface.

It is important to study the MOS capacitor because it forms the basis for the MOS transistor, the heart of modern electronics and telecommunication industries. To ensure good yield and device performance in MOSFETs, it is necessary to monitor and maintain the quality and reliability of the gate oxide. The most common technique for the study of gate oxide quality is capacitance-voltage (C-V) profile measurement. This technique allows a large number of device parameters to be extracted from a simple measurement, such as: oxide (dielectric) thickness, oxide breakdown strength, doping concentration, doping profile in the silicon, properties of interface traps, minority carrier lifetime in silicon, etc. Physics and electrical engineering undergraduates learn these concepts in their advanced semiconductor device courses and can appreciate them better through a hands-on lab exercise.

B. Modes of operation of MOSCAP capacitance

This section presents the principle of operation of a MOSCAP in brief. Readers interested in a detailed discussion are encouraged to refer to textbooks on semiconductor devices, that typically have an entire chapter dedicated to MOSCAPs,[1–3] or Appendix A of this manuscript for a comprehensive treatment of the underlying physics. The MOSCAP has three modes of operation based on the externally applied voltage to the gate with respect to the substrate. The capacitance of the MOSCAP varies based on the electrostatics at the semiconductor surface. The three modes are:

- Accumulation mode, in which the majority carriers accumulate at the surface. In this mode, the total capacitance is primarily due to the dielectric (silicon dioxide) capacitance.
- Depletion mode, wherein the semiconductor surface is depleted of majority charge carriers. In this mode, the total capacitance is a series combination of dielectric capacitance and depletion capacitance. The depletion region width increases with increasing applied voltage, causing the depletion capacitance to decrease.
- Inversion mode, in which the semiconductor surface has a large number of minority carriers from the substrate. The total capacitance is a series combination of the dielectric capacitance and a small-signal semiconductor capacitor (refer to Eq. (A6) for details).

The distinction between the three modes arises due to two voltages, (a) flat-band voltage (V_{FB}) which separates the accumulation mode from the depletion mode and (b) the threshold voltage (V_{th}) which distinguishes the depletion mode from the inversion mode. While the threshold voltage is a concept familiar to any reader that is familiar with semicondcutors, the flat-band voltage may not be a commonly known concept. A brief explanation of the flat-band voltage is presented below using the band diagram of the M-O-S sandwich in Fig. 2.

When a metal and semiconductor substrate are assembled together with an insulator layer (SiO_2) sandwiched in between, and the gate grounded ($V_g = 0$), the electrons in the metal move to the substrate (in case of a p-type substrate) through the external circuit (since the oxide layer will not allow any electron transport). The movement of electrons continues until thermal equilibrium is established (by aligning Fermi levels of the metal and semiconductor through band bending). For p-type silicon, the bands bend downwards as shown in Fig. 2. As a result, a sheet of electrons is deposited on the semiconductor surface while a layer of positive ions is formed on the metal side of the interface resulting in an electric field across the SiO_2 layer. The magnitude of band bending in the semiconductor layer is determined by the difference between the work function of the metal ($\phi_M = 4.1$ eV for aluminum, in this case) and the semiconductor (ϕ_S for p-type silicon, in this case). When a negative voltage is applied to the gate (while grounding the substrate), the band bending in the semiconductor decreases. At large enough negative voltage, it exactly compensates the electric

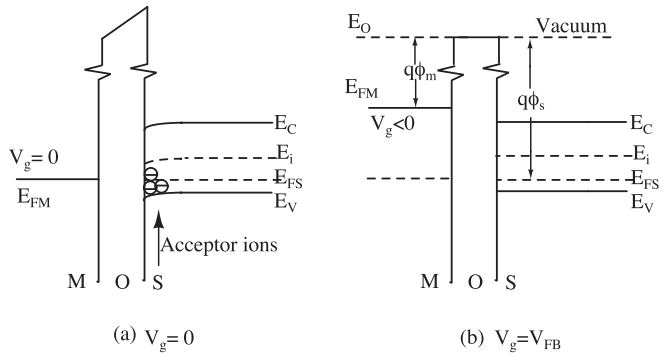

Fig. 2. Band diagram in a MOSCAP showing (a) band bending at $V_g = 0$ and (b) flat band condition. E_{FM} and E_{FS} denote the Fermi levels in the metal and semiconductor, respectively.

field arising from the work function difference, thereby causing the energy bands (E_c and E_v) of the substrate to be flat at the Si-SiO_2 interface as shown in Fig. 2. E_c and E_v are energy levels of the conduction band bottom and valence band top, respectively. The value of this voltage required to cause the bands to become flat, called as the flat-band voltage (V_{FB}), depends on the doping density of the semiconductor and on any residual interface charge that may exist at the interface between the semiconductor and the insulator.

C. Voltage dependence of MOSCAP capacitance

In the experiment, the gate voltage is swept from a large negative value, to a large positive value, observing that capacitance varies with the applied voltage as the device switches across different modes of operation. Figure 3 shows an illustration of the C-V profile of a MOSCAP that would be observed, highlighting different operation regimes and summarizing the different voltage dependent capacitance contributions. It is clear that to the left of point "a," where the gate voltage is a large negative value, holes (majority charge carriers) accumulate at the semiconductor surface, and the total capacitance is maximum and is essentially the oxide capacitance. The capacitance per unit area (C_{ox}) can be expressed in terms of permittivity of silicon dioxide ($\epsilon_{ox} = 0.34$ pF/cm) and nominal oxide thickness (d_{ox})

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}}. \tag{1}$$

As the gate voltage is increased (made less and less negative), the semiconductor surface becomes depleted and at the flat band voltage (point "b"), the electric field in the oxide layer diminishes to zero. A charge neutral surface with width equal to the Debye length L_D is formed, causing the overall capacitance per unit area to reduce, given by the series combination of C_{ox} and C_{Debye}, where

$$C_{Debye} = \frac{\epsilon_{Si}}{L_D}. \tag{2}$$

The accumulation region to the left of the knee is called strong accumulation when the device behaves like a perfect parallel plate capacitor. The region between the knee of the curve and point b is called weak accumulation, where the capacitance starts reducing slowly as the surface charge starts reducing. As the gate voltage is further increased, the

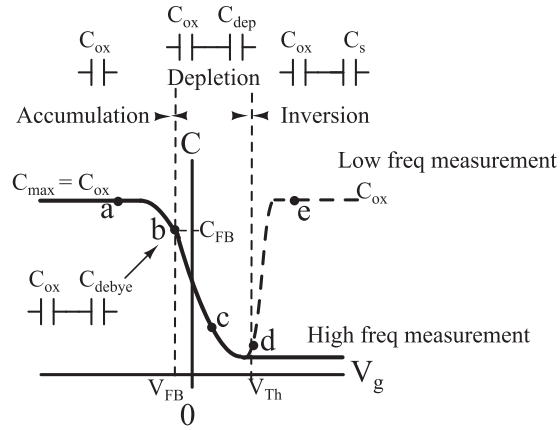

Fig. 3. Illustration of different regimes of operation of the p-substrate MOSCAP.

depletion layer capacitance C_{dep} (point "c") appears in series with C_{ox}

$$C_{dep} = \frac{\epsilon_{Si}}{W}, \tag{3}$$

where $W = \sqrt{(2\epsilon_{Si}\phi_{Si}/qN_A)}$ is the width of the depletion region, q is the elementary charge on an electron, N_A is the doping density, and ϕ_{Si} is the work function of silicon.

The capacitance continues decreasing with increasing gate voltage (as the width of the depletion region W increases) until inversion occurs when the voltage equals V_{th} (point "d"). The effective capacitance (per unit area) is then minimum and equal to a series combination of C_{ox} and a small signal semiconductor capacitance C_s

$$C_s = \frac{\epsilon_{Si}}{W_T}, \tag{4}$$

where $W_T = \sqrt{(\epsilon_s\phi_F/qN_A)}$ and $\phi_F = (kT/q)\ln(N_A/n_i)$, where n_i is the intrinsic carrier concentration. The region between point d and point "e" is called the weak inversion region where the minority carrier density increases exponentially and the capacitance per unit area quickly increases to C_{ox} in low frequency measurement. The measured capacitance in the inversion mode depends strongly on the frequency of the AC component of applied voltage. For higher frequency signal, a smaller capacitance is measured as the inversion layer charge carriers (minority carriers from generation-recombination processes) cannot be supplied/removed quickly enough to respond to the change in the gate voltage.

Appendix A of this manuscript provides a comprehensive summary of these modes, with associated equations required to extract the device parameters. Low frequency C-V measurement in the inversion regime is challenging due to low frequency noise in active electronic components such as the operational amplifiers commonly used in undergraduate labs, and hence we only focus on high frequency measurements in this manuscript.

D. Extraction of device parameters

We can extract following parameters from C-V measurement:

(1) Thickness of the oxide (d_{ox}): The oxide thickness can be extracted from C_{ox} using Eq. (1) by measuring the accumulation capacitance (point a in Fig. 3). The capacitance per unit area may be estimated, provided the accurate area of the metal gate electrode is known. The students could be provided the electrode size (diameter as drawn in the layout mask for fabrication). If the actual area of the gate electrode post-fabrication is not measured on individual devices, the students could be provided the thickness of oxide (measured with an ellipsometer), and asked to extract the area of the electrode. The electrode size is kept large so that: (i) the capacitance is large, making it easier to measure, and (ii) the students can align the device to the electrical contact on the probe station with naked eyes, without requiring any microscope or magnifying optics.
(2) Doping density (N_A): This can be obtained from C_{min} (point d in Fig. 3) which is the series combination of C_{ox} and C_s. After obtaining C_s from Eq. (4), N_A can be extracted from the expression for maximum depletion width W_T, by solving Eqs. (A7) and (A8) using numerical methods.
(3) Flat band capacitance C_{FB}: C_{FB} (per unit area) can be evaluated as a series combination of C_{ox} and C_{Debye}, from Eqs. (1) and (2).
(4) Flat band voltage: The voltage corresponding to C_{FB} in the C-V profile is the flat band voltage, V_{FB}.

III. DEVICE FABRICATION

The MOSCAP devices were fabricated at the Indian Institute of Technology Bombay Nanofabrication Facility (IITBNF), which is a central research fabrication facility. However, this experiment gave the opportunity to our sophomores not only to witness the complete fabrication cycle at this facility but also to handle the devices fabricated there and to characterize them for the first time in their curriculum. P-type ⟨100⟩ silicon wafers (2-inch diameter) were chosen as substrate wafers with resistivity 4–7 Ω cm. The wafers underwent an RCA clean process, and subsequent dry oxidation in a CMOS clean furnace, with process parameters targeted for ≈100 nm of silica (silicon dioxide) thickness. To form back-contact to the silicon substrate, the silica grown on the bottom side of the wafer had to be removed. This was done by gently rubbing the wafer bottom with a cleanroom swab dipped in buffered hydrofluoric acid (5:1) to etch away the silica. Oxide removal was verified by performing sheet resistance measurement of the wafer bottom with the four-point probe method. Metal contacts were formed on both sides of the wafer using 200 nm aluminum deposited with thermal evaporation. A shadow mask was used for the top side of the wafer to obtain isolated electrodes for separate devices. The wafers were then annealed at 630 °C for 20 minutes with the forming gas. Finally, each wafer was diced into individual chips by scribing the wafer. Figure 4 shows an illustration of the process steps.

IV. PROBE STATION DESIGN

A typical MOSCAP sample assembled on the probe station is shown in Fig. 5. There are as many MOSCAPs on the sample as dots on the top surface, corresponding to separate gate electrodes. Students can choose any one of the dots (gates) for characterization. The silicon substrate is common to all gate electrodes. The sample is glued to a small phosphor bronze plate (any conducting material can be used) using silver adhesive paste. This serves two main goals: it reduces the contamination of the device (by having students handle the phosphor bronze plate instead of touching the wafer) and also protects the devices from damage due to electrostatic discharge (ESD). Thus, we need to make two electrical contacts; one with the dot (gate) on the top and the other with the bottom terminal (phosphor bronze plate). The top contact is made through the POGO pin (spring test probe receptacle). The POGO pin is connected to the wire labeled "Gate (G)" through a brass rod (that rests on a non-conductive acrylic stand-off) via a phosphor bronze clip. The phosphor bronze clip is used for the alignment of the POGO pin contact on the desired dot. This is achieved by controlling the alignment screw in the acrylic stand. The base of the test set up is a copper plate which itself acts as another contact, connected to the wire labeled "Substrate (S)" as shown in Fig. 5. The copper plate makes direct electrical contact with the phosphor bronze plate. From any electrical perspective, any metal would work as the substrate. Our emphasis was on keeping manufacturing costs low, and so we worked with materials available in the lab. An engineering drawing of the probe station is provided in Appendix D. The total cost of every measurement jig, including the bill of materials (BoM) and machining costs, is approximately INR 250 (≈USD $4) per setup. While any conducting material is acceptable in lieu of the phosphor bronze clip for making an electrical contact, phosphor bronze is used because it provides good spring action and does not deform permanently upon applying a force.

V. CAPACITANCE MEASUREMENT CIRCUIT

The primary considerations for the circuit to be used for this experiment are:

- Should be easily implementable on a bread-board and use standard measuring instruments like a digital storage oscilloscope (DSO) and function generator to make it cost effective.

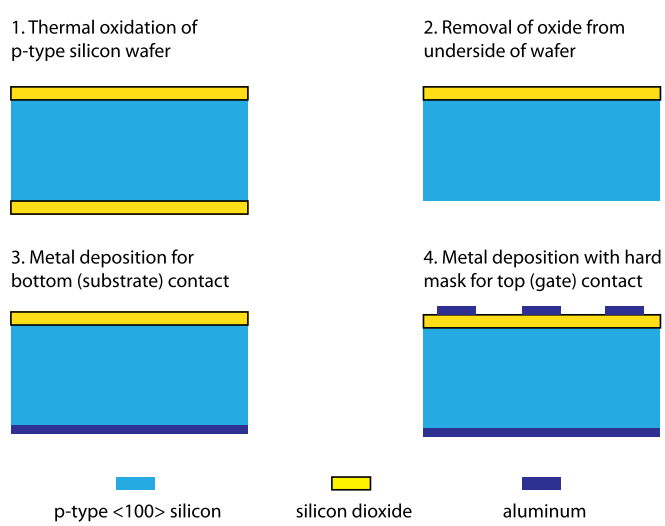

Fig. 4. Illustration of the process flow used to fabricated the MOSCAP devices.

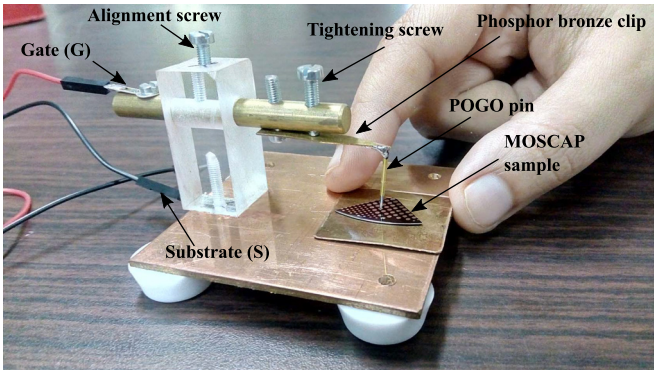

Fig. 5. Photograph of the probe station designed for the lab with a MOSCAP sample.

- Should not require expensive components or equipment (such as a semiconductor device parameter analyzer, precision LCR meter, etc.)
- Should use circuit blocks familiar to second year undergraduate students to understand the principle behind the measurement and analyze observations.

The capacitance of the MOSCAP depends strongly on the applied DC voltage. Since the experiment involves measurement of the C-V profile of the capacitor, the circuit must also be designed to apply an additional DC voltage across the capacitor that can be varied, while measuring the AC current to extract the capacitance. Figure 6 shows a schematic of the circuit used for our measurement. In our setup, we apply a variable DC bias and a small AC signal (small enough not to perturb DC bias) to the DUT (Device Under Test). This is accomplished by using a basic inverting summing amplifier that adds the variable DC voltage (with unity gain $= R/R_2$) and the small signal AC voltage (with attenuation factor $1/10 = R/R_1$), the output voltage of which is then connected to the DUT. The voltage V_{DUT} in Fig. 6 is thus given by the following equation:

$$V_{DUT} = -R\left(\frac{V_{DC}}{R_2} + \frac{V_{AC}}{R_1}\right). \tag{5}$$

The AC voltage amplitude across the DUT is thus one-tenth of the applied input DC voltage. Gate (G) terminal of the MOSCAP is connected to the output of the summing circuit while the substrate terminal (S) is virtually grounded due to negative feedback in the op-amp circuit. To measure the capacitance, we utilize the fact that the current through a capacitor is proportional to the applied AC sinusoidal voltage. We use a transimpedance amplifier (I to V converter) so that the current flowing through the capacitor is converted into voltage, the AC component of which is measured using a DSO. The transimpedance amplifier generates a voltage output that is proportional to the DUT capacitance (C_{DUT}) and V_{DUT}. The magnitude of this voltage is given by following equation:

$$|V_{out}| = |V_{DUT}|\frac{C_{DUT}}{C_F}\frac{1}{\sqrt{1+\frac{1}{(\omega R_F C_F)^2}}}. \tag{6}$$

By monitoring the amplitude of the AC component of V_{out} at the frequency of the small signal AC voltage applied to the input of the summing amplifier, C_{DUT} could be estimated.

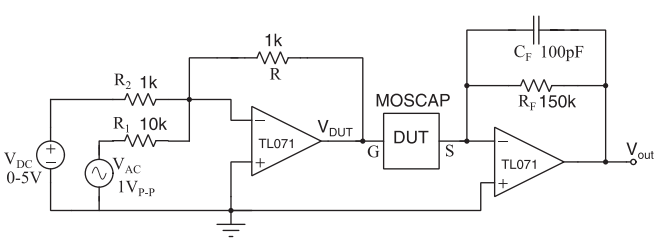

Fig. 6. Schematic of the circuit used to apply DC bias to the gate and measure the capacitance of the device under test (DUT) from small signal AC gain.

VI. ELECTRICAL MEASUREMENTS

The capacitance of the MOSCAPs we fabricated is in the range of few hundred picoFarads. Due to low frequency noise sources in the op-amp ICs used in the experiment, and the small value of the capacitance to be measured, the low frequency C-V profile measurements are prone to large errors. Hence, we focus on high frequency C-V profile measurements only in this experiment. Using $C_F = 100\,\text{pF}$ and $R_F = 150\,\text{k}\Omega$, the resulting cut-off frequency for the high-pass filter corner in the transimpedance amplifier is 10 kHz. For high frequency C-V measurements, we choose a frequency of 100 kHz and a peak-to-peak voltage of 1 V at the input. The op-amps used in the experiment are all Texas Instruments TL071 ICs. The circuit gain can be ascertained by observing the input and output peak-to peak voltage values on a digital storage oscilloscope (DSO), and C_{DUT} can be extracted using Eq. (6).

As the capacitance values of the MOSCAPs used in this experiment were typically in the range 100–300 pF, the circuit was tested by connecting commonly available capacitors (100 and 330 pF) as the DUT to verify the correctness of the range of capacitance measurement. Once the measurement limits are established, the capacitors are removed and the output of the summing circuit is connected to the gate of the DUT using the POGO pin of the probe station. Figure 7 shows a photograph of the experimental setup with the MOSCAP under test. The substrate of the device which is on the base metal of the probe station is connected to the input of the I-V converter. Input V_{dc} of the summing circuit is varied from 0 to +4 V and the output voltage is measured. The input DC polarity is then reversed to measure the capacitance in the range 0 to −4 V.

The C-V profile of the MOSCAPs thus measured by some students for a gate voltage (V_g) range of −4 to +4 V is shown in Fig. 8. The device parameters obtained from the op-amp circuit based C-V measurement are shown in Table I (see procedure explained in Sec. II D). Students were provided the oxide thickness (98 nm as measured with an ellipsometer) and asked to extract the electrode diameter from their measurements. The calculated electrode diameter is in the same order of magnitude as the 1 mm diameter drawn in the layout. The fabrication tolerance and variations will introduce deviations from 1 mm in the fabricated device, but these variations are not measured for this experiment. The doping density for these wafers of resistivity 4–7 Ω cm is expected to be $\approx 0.5 \times 10^{16}\,\text{cm}^{-3}$. The error in extraction of this specification is due to errors in the capacitance measurement, which are not calibrated with precision semiconductor

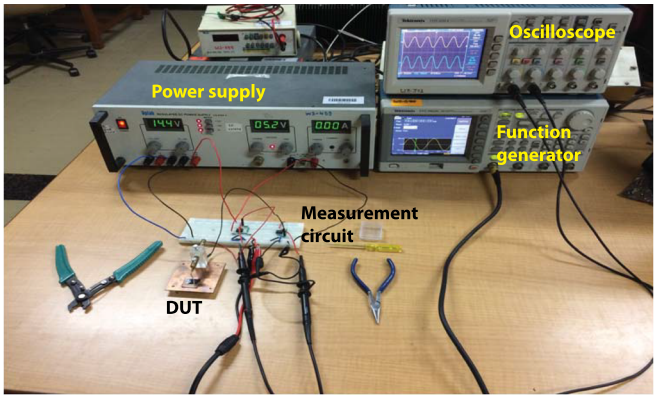

Fig. 7. Photograph of the experimental setup used in the lab.

analyzers to remove the effect of device parasitics. Apart from parasitic capacitance, the measurement circuit also introduces an error of $\pm 10\%$ in the capacitance measurement, as was verified with an Agilent 4284A precision LCR meter. The flat-band capacitance and flat-band voltage are within reasonable ranges expected for such a MOSCAP.[3]

VII. CONCLUSION AND DISCUSSION

While fabricating and storing devices for a large class, care must be taken to ensure proper storage conditions. The silicon dioxide layer in a MOSCAP is notoriously hygroscopic, and by absorbing moisture from ambient humidity, the MOSCAPs may present DC offset at the output of the measurement circuit shown in Fig. 6, due to the leakage path offered by absorbed moisture. To avoid such moisture absorption, we recommend storing these devices in a dessicator chamber. If such chambers are not available, the devices need not be discarded, but must be "baked" to restore their performance. We recommended that the MOSCAP devices be baked at 150 °C for 3 hours, either in an oven or on a hot plate, to dehydrate the devices before measurement.

In conclusion, we demonstrate a case study to educate undergraduate students in physics or electrical engineering on semiconductor device testing and analysis using MOSCAP devices and measuring their C-V profile. The students were also given a lab tour of the microfabrication facility at IIT Bombay (IITBNF) after they performed the experiment, to enable them to appreciate the underlying technical expertise that is required in the manufacturing of semiconductor devices, and to excite and enthuse them in semiconductor device technology. The experimental demonstration designed to meet this goal can be leveraged and replicated easily by most university instructional laboratories, and MOSCAP devices can be fabricated externally should the university not have its own microfabrication facility (see Appendix B). Such experiments will make a hands-on experience with semiconductor device physics accessible to a multitude of undergraduate students to reinforce the concepts taught in a corresponding classroom course.

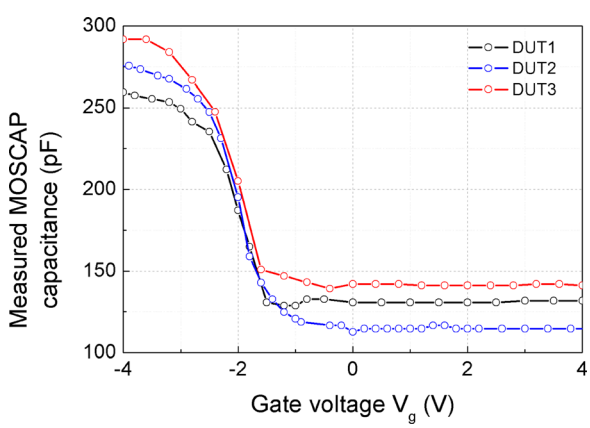

Fig. 8. Measured high frequency C-V profile of MOSCAP devices, from lab readings obtained by three students. The capacitance is extracted from the voltage measurements using Eq. (6).

Table I. MOSCAP parameters extracted from the C-V profile based on measured data collected by 3 students (DUT refers to the Device Under Test).

Device parameter	DUT1	DUT2	DUT3
Electrode diameter (mm)	0.97	1.01	1.03
Doping density ($10^{16}\,\mathrm{cm}^{-3}$)	1.14	0.48	0.92
Flat-band capacitance (pF)	228	233	255
Flat-band voltage (V)	−2.4	−2.3	−2.5

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APPENDIX A: MODES OF OPERATION IN MOSCAP

The C-V measurement is carried out by sweeping the gate voltage from ($V_g \ll V_{FB}$) which is a sufficiently large negative voltage to a voltage ($V_g \gg V_{th}$) which is sufficiently large positive voltage. Based on the biasing (i.e., voltage applied to the gate, relative to the substrate), there are three modes of operation of a MOSCAP (the substrate is grounded, in all discussions below):

- **Accumulation**: When the applied gate voltage (V_g) is more negative than the flat-band voltage (V_{FB}), i.e., $V_g < V_{FB}$, the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. A small amount of band bending builds up the accumulation charge so that almost the entire electric field appears across the oxide. In this mode, only the oxide (dielectric) contributes to the capacitance. The capacitance per unit area (C_{ox}) can be expressed in terms of permittivity of silicon dioxide ($\epsilon_{ox} = 0.34$ pF/cm) and nominal oxide thickness (d_{ox})

$$C_{ox} = \frac{\epsilon_{ox}}{d_{ox}}. \tag{A1}$$

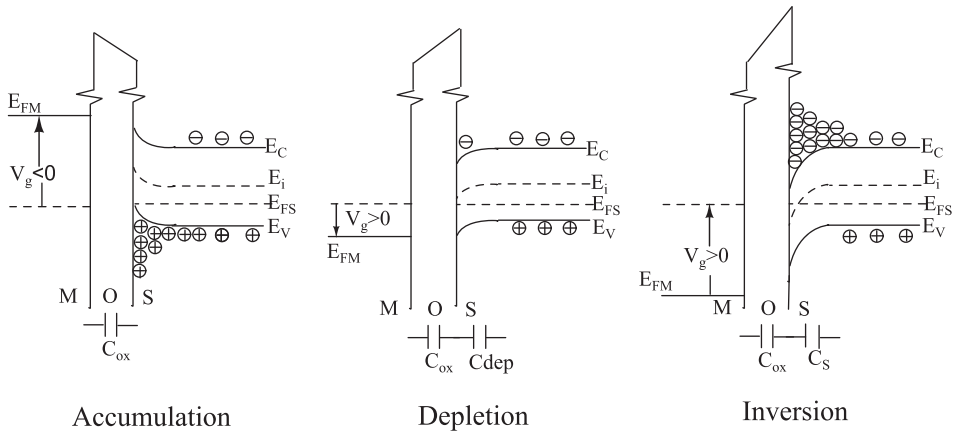

Fig. 9. Illustration of different regimes of operation of the p-substrate MOSCAP: (a) accumulation, (b) flat-band, and (c) depletion.

- **Flat-band**: The flat-band condition separates the accumulation and depletion modes of operation, and is not counted as a separate operating mode. At the flat-band condition, the surface will neither be accumulated nor depleted, i.e., the silicon is neutral everywhere. Thus, variations in V_g will result in incremental changes in the substrate charge at length L_D, the extrinsic Debye length. The Debye length is a characteristic shielding distance at which the external electric field is reduced by factor $1/e$. The Debye length depends on the permittivity of the silicon (ϵ_{Si}), electron charge ($q \approx 1.6 \times 10^{-19}$ C), and doping density of silicon (N_A) per cm^3

$$L_D = \sqrt{\frac{\epsilon_{Si} kT}{q^2 N_A}}. \tag{A2}$$

Here, ϵ_{Si} is the permitivity of silicon ($\epsilon_{Si} = 1.05$ pF/cm), k is the Boltzmann constant, and T is the temperature of the substrate in K. This neutral silicon results in another capacitance C_{Debye}, in series with C_{ox}

$$C_{Debye} = \frac{\epsilon_{Si}}{L_D}. \tag{A3}$$

The flat-band capacitance C_{FB} (per unit area) is given by

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_{Debye}}. \tag{A4}$$

The gate voltage corresponding to C_{FB} is the flat-band voltage which may be larger (i.e., more negative) than the work function difference ($\phi_M - \phi_S$) due to interface traps. The work function of p-type silicon (ϕ_S) depends on doping density, and hence both V_{FB} and C_{FB} depend on the doping density of the substrate.

- **Depletion**: When a small positive voltage is applied to the gate, such that $V_{FB} < V_g < V_{th}$, where V_{th} is the threshold voltage required to form the inversion layer (see below for definition of inversion), the device operates in the depletion mode. The majority carriers (holes) get repelled from the oxide-substrate interface. Hence, the surface of the semiconductor is depleted of mobile carriers (holes) leaving behind a negative space charge. In the depletion region, the hole concentration decreases, moving E_i closer to E_F, bending the bands downwards near the Si–SiO$_2$ interface as shown in Fig. 9. Consequently, in order to maintain the charge conservation of the system, the depletion region must have a net negative space charge, provided by uncovered ionized acceptors. Since these ions are not mobile, the conductivity of the depletion region is much lower than the rest of the bulk semiconductor thus creating another layer of non conducting region contributing to depletion capacitance (C_{dep})

$$C_{dep} = \frac{\epsilon_{Si}}{W}, \tag{A5}$$

where $W = \sqrt{(2\epsilon_{Si}\phi_{Si}/qN_A)}$ is the width of the depletion region and ϕ_{Si} is the work function of silicon. Hence, the capacitance per unit area of a MOS structure in depletion is the series combination of C_{ox} and C_{dep} and is lower than C_{ox}. Further increase in gate voltage causes the capacitance to decrease as W grows until inversion is reached.

- **Inversion**: If the positive bias is increased further, the density of holes decreases exponentially from the surface going into the bulk. Since the MOSCAP is always in quasi-equilibrium, the law of mass action is valid. Thus at the surface, the number of holes decreases as the applied voltage is increased while the number of electrons (thermally generated minority carriers) at the surface increases. At a particular voltage called the threshold voltage (V_{th}), the concentration of electrons at the surface exceeds the concentration of holes in the bulk causing the conductivity type of the silicon surface to invert. Further increase in the applied gate voltage results in a linear increase in the charge per unit area of the inversion layer. The effect of increased positive bias is to bend the bands downwards until the intrinsic level and the Fermi level are just equal at the surface as shown in Fig. 9.

It should be noted that after inversion, the MOSCAP capacitance depends on whether the signal applied at the gate is a low frequency signal (typically less than 100 Hz) or a high frequency signal (typically larger than 100 kHz). In inversion, the charge carriers are made available due to generation-recombination and they respond slowly to the applied high frequency gate signal. The time required to build inversion-layer charge is given by $2\tau_0 N_A/n_i$, where τ_0 is minority-carrier lifetime at the surface and n_i is the intrinsic carrier concentration.[3] In low frequency measurements, the inversion layer charge can be supplied/removed quickly enough to respond to changes in the gate voltage. Incremental charge is effectively added/subtracted at the surface of the substrate, and the capacitance is merely C_{ox}. In high frequency measurements, the inversion-layer charge cannot be

supplied/removed quickly enough to respond to changes in the gate voltage. Incremental charge is effectively added/subtracted at a depth W_T in the substrate. The total capacitance is then a series combination of C_{ox} and C_s, where

$$C_s = \frac{\epsilon_{Si}}{W_T}, \tag{A6}$$

$$W_T = 2\sqrt{\frac{\epsilon_s \phi_F}{qN_A}}, \tag{A7}$$

$$\phi_F = E_i - E_f = \frac{kT}{q} ln \frac{N_A}{n_i}. \tag{A8}$$

APPENDIX B: DEVICE AVAILABILITY FOR REPLICATION OF THIS EXPERIMENT

At IIT Bombay, we are privileged to have a micro- and nano-fabrication facility that enables us to fabricate several such devices to facilitate the design of such a lab experiment for our undergraduate students. We understand that many universities may not have such facilities, and a natural question that arises is how such a lab experience could then be provided to students. One option that could be availed is to procure silicon wafers with silicon dioxide of desired thickness pre-grown from wafer vendors. The metal deposition and annealing may be performed in non-cleanroom labs, if the necessary equipment are available.

For labs that do not have such equipment, and are desirous of making MOSCAP devices available to their students, we encourage reaching out to us at IITBNF. Through the Indian Nanoelectronics Users Program (INUP, http://www.inup.iitb.ac.in/inup/index.php), a project funded by the Ministry of Electronics and Information Technology (MeitY), Government of India, such labs may be able to avail the services of IITBNF facilities to obtain MOSCAP devices. Alternately, through the NEMS and MEMS Prototyping Facility at IIT Bombay (NMPF, https://www.memsprotofab.com/), also established with support from MeitY, one may directly place an order to buy such devices.

APPENDIX C: C-V PROFILING OF SOLAR CELLS

When availability of MOSCAPs is a challenge, one of the options is to buy commercially available devices, such as solar cells or Schottky diodes,[4] which are easily available on online retail websites. By soldering wires to the two terminals of an individual solar cell, students can perform current voltage profiling (I-V) and C-V profiling of these devices by simply plugging them into breadboards. To obtain measurable

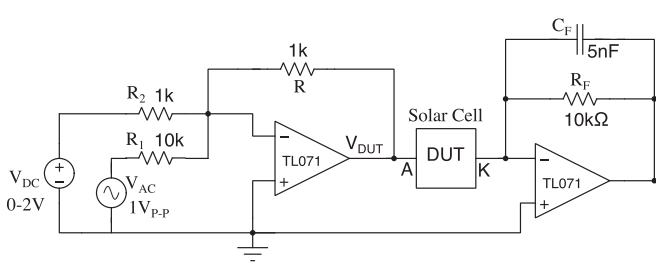

Fig. 10. Schematic of the circuit used to apply reverse bias and extract the capacitance of the device under test (DUT) by measuring small signal AC gain.

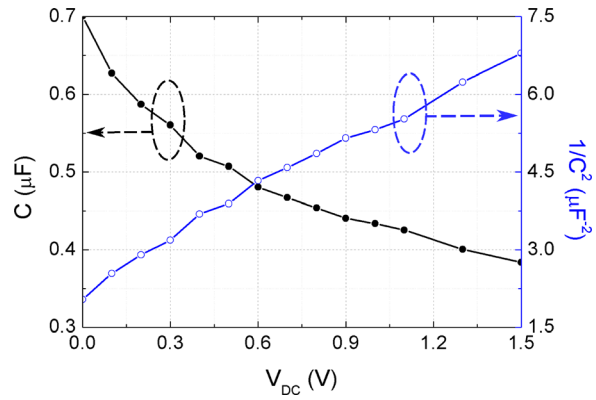

Fig. 11. C-V profiling and variation of $1/C^2$ with applied DC voltage for a solar cell.

capacitance values with the circuit presented in this manuscript, we recommend procuring solar cells with an area of at least 4 cm × 4 cm. At IIT Bombay, we also include solar cell C-V profile measurements in our undergraduate lab course, using the circuit presented in this manuscript. A brief guide based on our experiment is presented below.

The first course in semiconductor device physics for undergraduate students usually deals with physics of a p-n junction as it is one of the most commonly encountered concepts in semiconductors. Apart from basic I-V characteristics of a p-n junction, C-V measurement is also important in applications such as switches, where the capacitance sets the bandwidth limitation of a device. The capacitance of a p-n junction is dominated by different physical mechanisms depending on the bias voltage:

(a) junction capacitance in the depletion region (dominant in reverse bias) and
(b) diffusion capacitance (dominant in forward bias).

The C-V measurement experiment described in this manuscript is adapted to study how the junction capacitance varies with applied reverse bias and to estimate the doping density and built-in potential. In commercially available diodes, the junction capacitance is designed to be as low as possible to enable fast switching operation. This poses problems in the measurement of capacitance of such devices in the laboratory using educational grade measurement equipment. To overcome this limitation, we use a solar cell, which is essentially a large area p-n junction diode that thereby has larger and hence measurable capacitance.

1. Voltage dependence of p-n junction capacitance

When a p-n junction is reverse biased, uncompensated acceptor ions in the p- side of the junction and an equal number of ionized donors on the n- side of junction form the space charge region. Since there are no mobile carriers in this region, only the free carriers at the edge of the depletion region can respond to the externally applied ac field. The junction thus resembles a parallel plate capacitor, whose capacitance is specified as

$$C = \left| \frac{dQ}{dV_{DC}} \right| = \frac{\epsilon_0 \epsilon_s A}{x_d}, \tag{C1}$$

where Q is the charge (free charge carriers) on either side of the junction, V_{DC} is the applied voltage, ϵ_s is the dielectric constant of the semiconductor, ϵ_0 is the permittivity of free

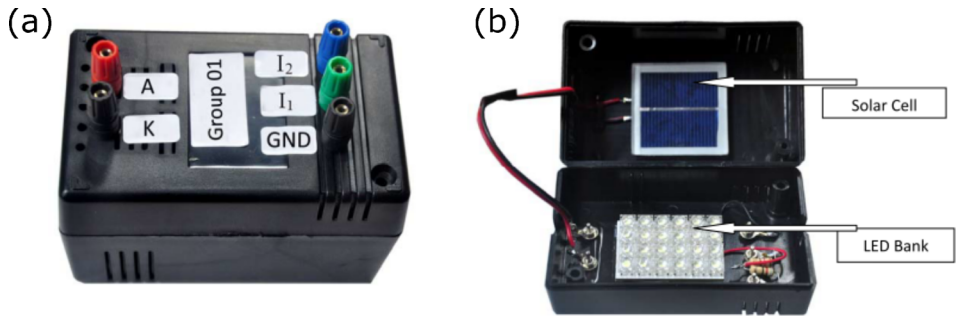

Fig. 12. (a) Black box package used for solar cell measurement and (b) inner view showing the LED bank and 4 cm × 4 cm solar cell.

space, and A is the area of the p-n junction. The depletion region width, x_d, for a reverse biased junction with constant doping density N_d is given by

$$x_d = \left[\frac{2\epsilon_0\epsilon_s(V_{bi}+V_{DC})}{qN_d}\right]^{\frac{1}{2}}. \tag{C2}$$

V_{bi} is the built-in voltage, q is the charge on an electron (1.6×10^{-19} C) and N_d is the doping density. From Eqs. (C1) and (C2), it follows that

$$\frac{1}{C^2} = \left[\frac{x_d}{\epsilon_o\epsilon_s A}\right]^2 = \left[\frac{2(V_{bi}+V_{DC})}{q\epsilon_o\epsilon_s A^2 N_d}\right]. \tag{C3}$$

A plot of $1/C^2$ v/s V_{DC} is a straight line with slope $d(1/C^2)/dV = 2/(q\epsilon_o\epsilon_s A^2 N_d)$. By obtaining this plot, students can easily find doping density N_d from the slope. The built-in potential V_{bi} could be estimated from either the X-axis intercept ($-V_{bi}$) or the Y-axis intercept ($2V_{bi}/(q\epsilon_o\epsilon_s A^2 N_d)$). A detailed treatment of C-V profile of a p-n junction is available in semiconductor device reference books.[1,3]

2. Experiment and results

The capacitance measurement circuit from the MOSCAP measurement is adapted to measure the C-V profile of a solar cell (area 4 cm × 4 cm), using the circuit shown in Fig. 10.

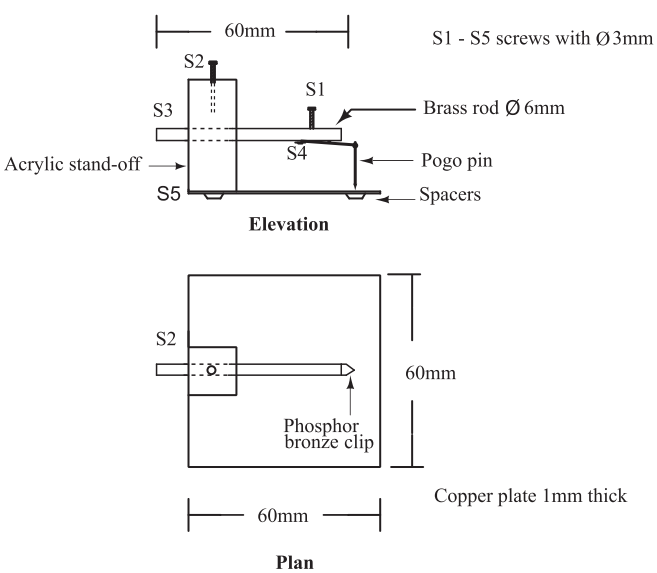

Fig. 13. Engineering drawing of the probe station used in this experiment.

The transimpedance amplifier circuit components are changed to suit the C-V measurement for the solar cell. The small signal AC voltage peak-peak amplitude is set to 1 V, which is further attenuated by a factor of 10. The DC bias is varied in steps from 0 to 1.5 V. The C-V profile and $1/C^2$ v/s V_{DC} plots obtained from measurements performed by a student are shown in Fig. 11. From the slope of a linear least-squares fit to the $1/C^2$ v/s V_{DC} plot, the doping density is estimated to be $N_d = 2\times10^{16}\,\mathrm{cm}^{-3}$ and from the Y-axis intercept, the built-in voltage is estimated to be $V_{bi} = 0.75$ V.

The characteristics of a solar cell depend on the illumination, so care must be taken to ensure controlled experimental conditions. In our experiment, we encase the solar cell (size 4 cm × 4 cm) in a black colored box, shown in Fig. 12. We have included provision for an LED bank and two resistors to set two different illumination levels (terminals I_1 and I_2), which are used in a separate experiment to study lighted I-V characteristics of a solar cell. For this C-V measurement experiment, we turn off the LED bank and measure the dark characteristics.

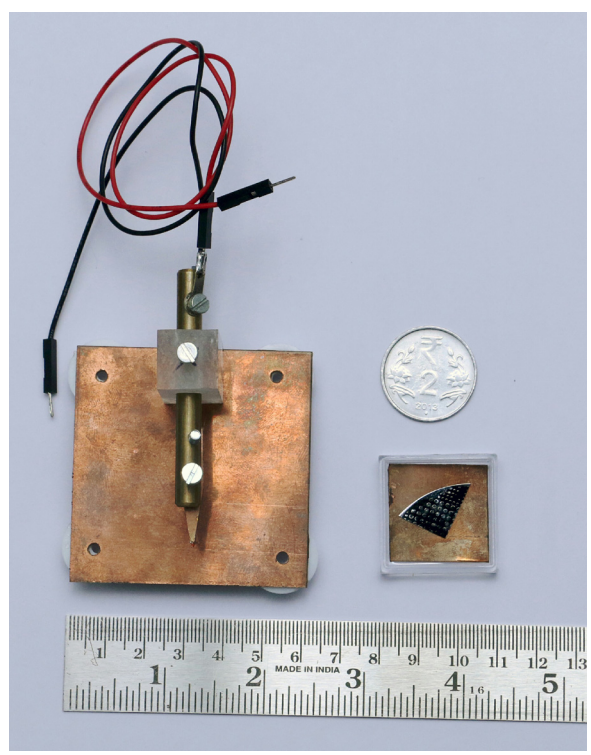

Fig. 14. A representative MOSCAP sample with a probe station shown with a ruler and an INR 2 coin

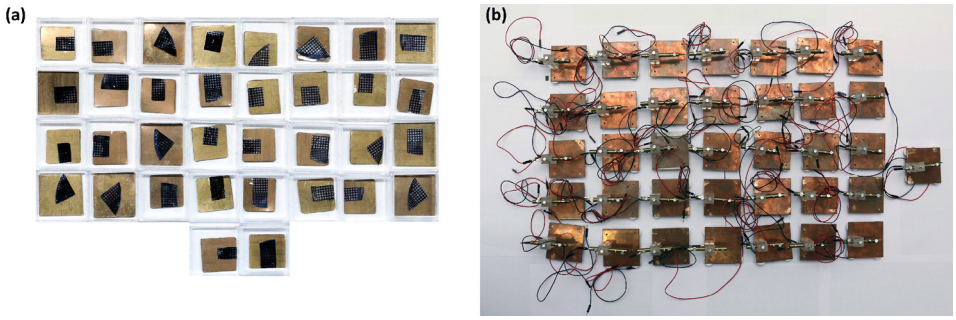

Fig. 15. (a) MOSCAP samples fabricated for the lab experiment. (b) Probe stations assembled for the lab experiment.

APPENDIX D: DETAILS OF PROBE STATION DESIGN

The dimensions of various components of the probe station in the drawing shown in Fig. 13 are based on the design we made for this experiment. The dimensions should merely serve as guidelines, and any modifications to enhance the utility of the design are most welcome.

APPENDIX E: ORIGIN OF THE EXPERIMENT

The idea for the experiment was conceived when B.M.A. and K.L.N. were instructors for EE236: Electronic Devices lab course (for sophomores) in Fall 2016 at IIT Bombay. The efforts gathered momentum when S.T. and K.L.N. took charge of EE236 in the Fall 2017 semester. The teaching assistants for this lab fabricated the devices at IITBNF under the guidance of S.T. and K.L.N., and J.J. designed the measurement circuit and collected experimental data under the guidance of B.M.A. and K.L.N. to fine-tune the experiment. M.P.D. managed the activities and guided the lab staff at Wadhwani Electronics Lab at the Electrical Engineering department in IIT Bombay to get the probe stations designed and assembled. The lab experiment debuted in Fall 2017 for a class of 140 students. This manuscript was written by M.P.D. and S.T., with contributions from other authors.

Figure 14 shows a picture of the probe station and MOSCAP sample with an INR 2 coin and a ruler for reference. The compact arrangement can serve even the most space-constrained labs easily. To enable the entire class to simultaneously perform the experiment (experiments are performed in pairs, in two separate batches), more than 30 probe stations were designed. A photograph of all the samples and probe stations designed for this experiment is shown in Fig. 15.

[a]Electronic mail: stallur@ee.iitb.ac.in

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