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Fabrication and electrical characterization of Au/p-Si/STO/Au contact

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ABSTRACT

Au/STO/p-Si/Au structure is fabricated using pulsed laser deposition technique at room temperature. The current–voltage (*I–V*) characteristics of the device show rectification behavior. Various junction parameters such as ideality factor, barrier height and series resistance is determined using conventional forward bias *I–V* characteristics, Cheung method and Norde's function. Au/STO/p-Si/Au structure shows non-ideal diode characteristics with the value of ideality factor of ~5.1 and barrier height of ~0.40 eV.

1. Introduction

Schottky junctions based on perovskite-oxide have attracted considerable attention because of their potential applications in non-volatile memory device [1]. Among these perovskite-oxides, strontium titanate (STO) is widely used because of its remarkable ferroelectric and high dielectric constant [2]. Because of its high dielectric constant, STO is considered as an alternative material to replace SiO_2 as a gate oxide in metal-oxide-semiconductor device [3]. The electrical properties of STO could be changed from insulator to n-type semiconductor by introducing oxygen vacancy or impurity [4]. These oxides based p–n junctions have been reported to show magnetic characteristics compared to traditional semiconductor p–n junctions [5].

Guo et al. have fabricated STO/p-Si junction at 670 °C using laser molecular beam epitaxy technique [6]. The current–voltage (*I–V*) characteristics in the temperature range of 300 K–200 K show rectification behavior. Zhao et al. have reported ultraviolet detector based on STO/p-Si junction [7]. High epitaxial STO films were grown on silicon substrate to study the transport behavior of the junction at high temperature [2]. Although the electrical properties of epitaxial STO/silicon junction grown at high temperature has been studied earlier, but no detail diode parameters analysis using different methods such as Cheung and Norde's methods have been done. Our motivation is to study the junction properties of amorphous STO film on silicon wafer in detail. Literature survey reveals that there is no report on junction parameters of STO/p-Si using different techniques such as conventional forward bias *I–V* characteristics, Cheung and Norde's methods. In this study, we report the fabrication of amorphous STO/p-Si junction grown by pulsed laser deposition technique at room temperature. Different diode parameters such as ideality factor, barrier height and series resistance are determined using different methods.

2. Experimental details

Pulsed laser deposition technique is used for deposition of gold contact and STO film. The gold target for contact deposition is purchased from Kart J. Leasker, United States. The STO powder is purchased from Alfa-Aesar, United States. The STO target is made by cold pressing the STO powder at 6×10^6 N/m^2 load, followed by sintering at 950 °C for 12 h. The devices were prepared using p-type silicon wafer. Prior to deposition of contact and STO film, the wafer was chemically cleaned using RCA technique. The oxide layer on silicon wafer was removed using HF:10H_2O solution followed by sonication in acetone and isopropanol, respectively. STO film was deposited on silicon wafer at room temperature un-

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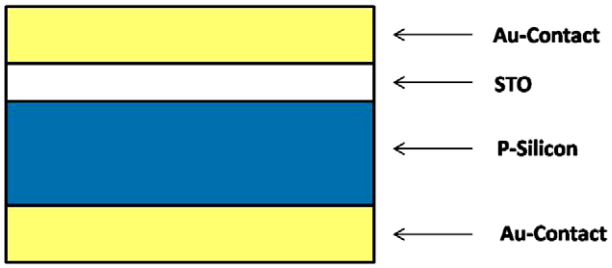

Fig. 1. A schematic cross-section of Au/p-Si/STO/Au structure.

der vacuum of base pressure 1.0×10^{-6} mbar. Gold contacts were also deposited at room temperature under vacuum of base pressure 1.0×10^{-6} mbar. KrF excimer laser (Lambda Physik COMPex, $\lambda = 248$ nm and pulsed duration of 20 ns) is used for deposition of the films. The laser was operated at a pulse rate of 10 Hz, with an energy of 300 mJ/pulse. The thickness of STO layer was measured by atomic force microscopy and was observed to be ~85 nm [8]. The schematic cross-section of the Au/p-Si/STO/Au is shown in Fig. 1. The *I–V* characteristics of device were measured using programmable electrometer (model 617, Keithley) and programmable voltage source (model 230, Keithley). All the data were collected using an IBM-compatible PC via IEEE-488 interface.

3. Results and discussion

The forward and reverse bias current–voltage characteristic of Au/p-Si/STO/Au structure is shown in Fig. 2. The *I–V* characteristics of the device clearly show the rectification behavior. Such type of behavior is best described by thermionic emission theory. According to this theory, current in such device could be expressed as [9]

$$I = I_o[\exp(qV/nkT) - 1], \tag{1}$$

where I_o is the saturation current, k is the Boltzmann constant, T is the absolute temperature, q is the elementary electric charge, V is applied voltage, and n is the ideality factor. The saturation current I_o is given as

$$I_o = AA^*T^2 \exp(-q\phi_b/kT), \tag{2}$$

where A is the active device area, A^* is the effective Richardson constant equal to 32 A/cm^2 K^2 for p-type silicon [10], and φ_b is the barrier height. The ideality factor is determined from the slope of the linear region of forward bias ln *I–V* plot. The ideality factor is expressed as

$$n = [q/kT] \cdot [dV/d(\ln I)], \tag{3}$$

whereas the barrier height of the device is calculated using the following equation:

$$\phi_b = kT/q \ln(AA^*T^2/I_o). \tag{4}$$

The barrier height is estimated to be 0.41 eV at room temperature. The value of ideality factor at low voltage is estimated to be 5.1. High ideality factor (10) is observed for the device at high bias voltage. It is reported that the ideal value of ideality factor as 1 at low voltage and 2 at high voltage for an ideal Schottky diode [11]. In general, high value of ideality factor could be due to presence of native oxide layer, accelerated recombination of electrons and holes in depletion region, the presence of interfacial layer [12], and the presence of imperfections [13].

Luo et al. have reported the value of ideality factor as 2.1 at low voltage for highly epitaxial STO film on silicon [2]. The high ideality factor of our device at low voltage may be due to amorphous nature of STO films. The ideality factor of STO/silicon junction could be improved by growing the epitaxial STO film on silicon at high temperature [2]. The presence of high ideality factors suggests that charge transport through junction is no longer due to thermionic emission [18]. To understand which mechanisms can control the junction behavior, the *I–V* characteristics of the device is studied in log–log scale.

Fig. 3 exhibits the double logarithmic plot of forward bias *I–V* characteristic of the Au/p-Si/STO/Au device. The linear behavior of log(*I*)–log(*V*) plot shows the presence of space-charge-limited current (SCLC) mechanism through the junction. Sugiura et al. have also observed that the transport through p–i–n junction based on STO material is mainly due to SCLC mechanism [14]. According to Child's law, $I \propto V^2$ for pure space-charge limited conduction with no traps. But in presence of traps, power law behavior for current and voltage ($I \propto V^{m+1}$) is observed [15]. The log(*I*)–log(*V*) plot clearly shows the power law behavior of current and voltage. It is observed that the double logarithmic plot of forward bias *I–V* characteristics have three linear regions separated by transition segments. The region (I) and (III) have slope of 2.2 and 2.3, respectively, while the region (II) has the slope of 3.3. The decreases in slope at high voltage could be due to 'trap-filled' limit of the device at high voltage [16,17]. Gullu et al. have also observed same behavior for orange G/n-Si junction [18].

The shape of the *I–V* characteristics depend on the series resistance (R_s) of the device. If the series resistance is high, the *I–V* curve will show wide curvature, and if the effect of series resistance is less, then the non-linear region of forward bias *I–V* curve will be

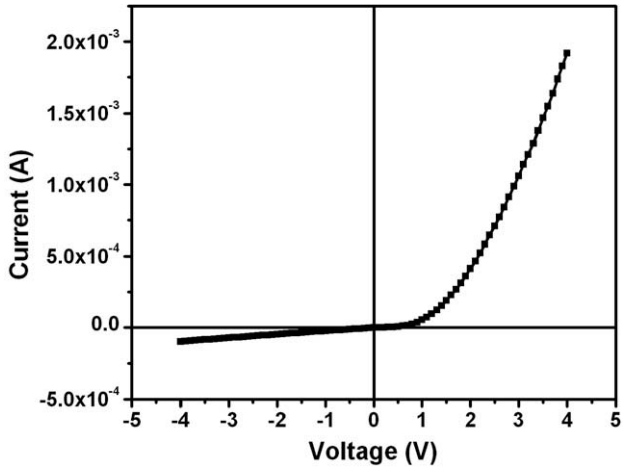

Fig. 2. *I–V* characteristic of Au/p-Si/STO/Au structure.

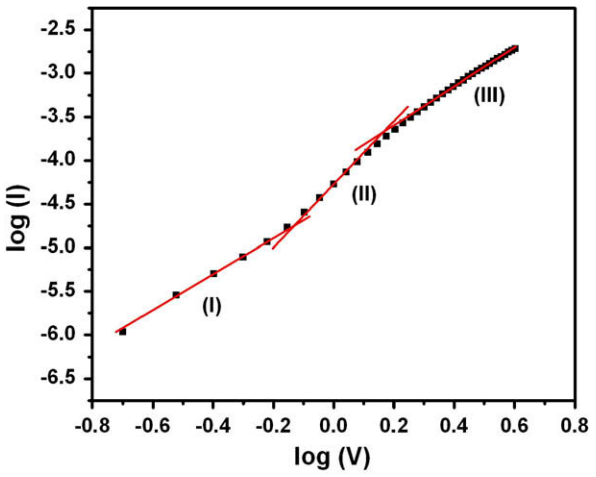

Fig. 3. The forward bias log(*I*)–log(*V*) plot of Au/p-Si/STO/Au structure.

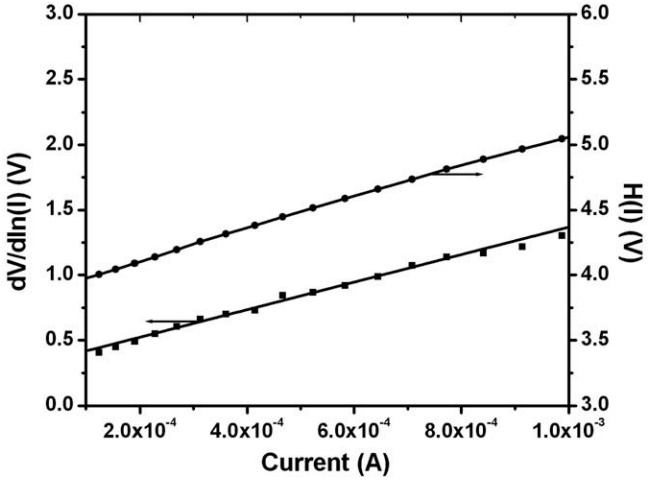

Fig. 4. The forward bias dV/d(ln I)–I and H(I)–I plot.

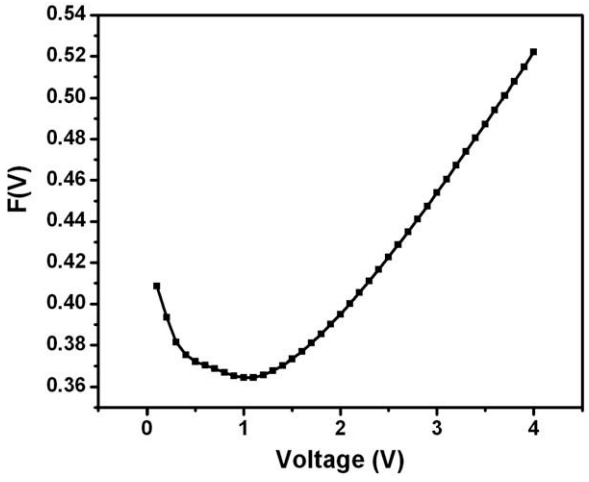

Fig. 5. $F(V)$–V plot of the Au/p-Si/STO/Au structure.

small [19]. The series resistance of device is calculated using three different methods. In first method, the series resistance is calculated using the I–V data of the device at higher voltage. The series resistance is calculated to be 1.16 kΩ. The second method is developed by Cheung and Cheung to determine the series resistance [20]. According to this method, the forward bias I–V characteristics of a device having series resistance is given as

$$I = I_o \exp[q(V - IR_s)/nkT], \tag{5}$$

where IR_s is the voltage drop across the series resistance of device. The value of series resistance, ideality factor and barrier height is determined by the following equations:

$$dV/d(\ln I) = nkT/q + IR_s, \tag{6}$$

$$H(I) = V - (nkT/q)\ln(I/AA^*T^2), \tag{7}$$

and $H(I)$ is given as follows:

$$H(I) = n\phi_b + IR_s. \tag{8}$$

A plot of dV/d(ln$I$) vs. I will be linear and the slope will give the value of series resistance and intercept will give the value of ideality factor of device. Fig. 4 shows the plot of dV/d(ln$I$) vs. I. The values of n and R_s have been calculated as $n = 10.4$ and $R_s = 9.6 \times 10^2\ \Omega$, respectively. It is observed that there is a difference between the values of ideality factor obtained from the forward bias ln$I$–V plot and from the dV/d(ln$I$)–I plot. This difference could be due to the presence of series resistance, interface states and to the voltage drop across the interfacial layer [21]. Series resistance and barrier height could be also calculated from Eq. (8) using the value of ideality factor obtained from Eq. (6). A plot of $H(I)$ vs. I will linear, the slope of this plot gives a value of series resistance and intercept gives the barrier height (Fig. 4). From $H(I)$ vs. I plot, the barrier height and series resistance of the device is also calculated as 0.39 eV and 1.1 kΩ respectively.

The third method used to determine the series resistance is called Norde's method [22]. Norde's method uses the following function to determine the series resistance and barrier height

$$F(V) = V/\gamma - (kT/q)\ln[I(V)/AA^*T^2], \tag{9}$$

where γ is the integer (dimensionless) greater than n, here it is taken as 10. $I(V)$ is the current obtained from the I–V characteristic. The value of barrier height is calculated after getting minimum of F vs. V plot. Fig. 5 shows the $F(V)$ vs. V plot of the device.
The barrier height is given as

$$\phi_b = F(V_o) + V_o/\gamma - kT/q, \tag{10}$$

where $F(V_o)$ is the minimum point of $F(V)$ and V_o is the corresponding voltage. The value of series resistance is also calculated using the formula

$$R_s = kT(\gamma - n)/qI. \tag{11}$$

The value of barrier height and series resistance is observed as 0.42 eV and $8.2 \times 10^2\ \Omega$, respectively. A small difference in values of series resistance obtained from Cheung and Norde's method is observed. This difference may be due to the fact that Cheung's model is applicable in high voltage region of the forward bias ln I–V characteristics, while Norde's model is applied to the full voltage range of forward bias ln I–V characteristics of the junctions.

4. Conclusions

The Au/p-Si/STO/Au structure is fabricated using pulsed laser deposition technique. The current–voltage characteristics of the device show non-linear behavior. The diode parameters such as ideality factor, barrier height and series resistance have been calculated using different methods. The diode parameters obtained from Norde's method is compared with those from Cheung functions, and it is observed that there is a good agreement between the values from both methods. The presence of high series resistance produces the downward concave curvature of the forward bias I–V characteristics at high voltage. The high ideality factor of the device may be due to large series resistance and amorphous nature of STO film.

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