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A method for characterizing near-interface traps in SiC metal–oxide–semiconductor capacitors from conductance–temperature spectroscopy measurements

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ABSTRACT

The state-of-the-art technology for gate oxides on SiC involves the introduction of nitrogen to reduce the density of interface defects. However, SiC metal–oxide–semiconductor (MOS) field-effect transistors still suffer from low channel mobility even after the nitridation treatment. Recent reports have indicated that this is due to near-interface traps (NITs) that communicate with electrons in the SiC conduction band via tunneling. In light of this evidence, it is clear that conventional interface trap analysis is not appropriate for these defects. To address this shortcoming, we introduce a new characterization method based on conductance–temperature spectroscopy. We present simple equations to facilitate the comparison of different fabrication methods based on the density and location of NITs and give some information about their origin. These techniques can also be applied to NITs in other MOS structures.

I. INTRODUCTION

Compared to other wide bandgap semiconductors, SiC has the advantage of being able to grow a native oxide. This desirable property has driven investment in SiC power devices over the past two decades.[1,2] However, the quality of as-grown oxides in dry O_2 is insufficient to be used as the gate dielectric for metal–oxide–semiconductor field-effect transistors (MOSFETs).[1,2] The quality of SiC gate oxides was improved significantly with the introduction of nitrogen into the fabrication process.[1–11] Oxide growth or post-oxidation annealing in N_2O or NO ambient reduces the density of interface defects to sufficient levels for commercial fabrication of SiC MOSFETs.[1–11]

However, despite these improvements, SiC MOSFETs have still not achieved the theoretical limits of the material. One issue with modern SiC MOSFETs is low channel-carrier mobility.[1,2] Fast traps, sometimes labeled "NI," have been assumed as one of the primary contributors to this problem.[1,12–14] These traps can be observed in the high frequency or low temperature conductance of test MOS capacitors.[12–14]

When the conventional interface-trap analysis is applied to these defects, the extracted properties are physically unreasonable, leading to questions about their origin. Recently, new evidence has suggested that these traps are due to near-interface traps (NITs), rather than conventional interface states. In our previous paper, we showed that the peak of the NI signal in conductance–temperature (G–T) spectroscopy measurements is associated with a specific surface electron density, irrespective of the gate bias.[15] Zhai *et al.* found a similar result by using standard interface trap characterization of low temperature conductance–frequency measurements.[16] They observed that the trap time constant was independent of the

surface potential.[16] Neither of these results can be accounted for by the conventional interface states, and so suggest that the signal is caused by NITs which are aligned with the SiC conduction band.

In light of this new evidence, it is clear that interface trap characterization techniques are not appropriate for the NI signal. However, characterization is still important for modeling and for the evaluation of different fabrication processes. One approach to this issue is to implement numerical simulations of NIT conductance and then extract the properties by fitting to the measured data.[15] This approach works but it is far too computationally expensive to see the practical use for comparing oxidation processes, especially at scale.

With this in mind, this paper introduces a new method for characterizing the NI signal from G–T measurements. The method is based on newly derived simple equations, which allow for fast approximation of trap densities and lateral positions to enable rapid evaluation of oxide quality. Furthermore, the equation parameters can be used to plot the theoretical conductance signal. We verify the new method and equations by comparing an NO post-oxidation annealed MOS capacitor to one with an oxide grown in NO.

II. CHARACTERIZATION METHOD

The most important assumption in this work is that the traps exchange electrons with the SiC conduction band via tunneling. Therefore, the process by which the electrons are released from the traps is temperature independent. This is based on the recent reports regarding the NI trap properties, which were outlined in Sec. I.[15,16] This is critical, and the present analysis is only possible because this has now been verified.[15,16]

To begin, we must first consider that at a fixed frequency, most of the measured NIT conductance signal will be due to a very narrow range of traps (in both energy and lateral depth). Therefore, we will assume that the conductance can be reasonably approximated as that of an average trap, with an effective areal density N_T and a single electron capture and release rate (R_C and R_R), as opposed to rate distributions. This is a necessary simplification; in the standard interface trap analysis, the treatment of a continuum of traps is made possible only because the traps are in thermal equilibrium with the semiconductor.[17] For NITs, this is not the case, and so complete knowledge of the trap distribution and response characteristics throughout the SiO_2 bandgap would be required to accurately model the conductance. Not only is this impractical, but due to the current lack of knowledge about the responsible defect(s), it is not possible. That being said, just because this assumption is required does not mean it is poor, as has been shown in numerical simulations[15] and as we will see later in this work.

The parallel conductance (G_P) of traps characterized by a single capture and release rate is given by[17]

$$G_P = \frac{q^2 N_T A}{kT} \times \frac{R_C R_R}{R_C + R_R} \times \frac{\omega^2}{(R_C + R_R)^2 + \omega^2}, \tag{1}$$

where q is the elementary charge, A is the gate area, k is Boltzmann's constant, T is the absolute temperature, and ω is the angular frequency. Equation (1) was first derived for interface traps,[17] but it equally applies for NITs. A derivation of Eq. (1) is included in the Appendix. From Eq. (1), it is clear that the strongest signal will be detected when the capture and release rates are both equal to $\omega/2$. It is reasonable to assume that the "average" trap will be one with the strongest response since traps around this will produce most of the measured signal. Therefore, we will assume that the "average" trap will be one with $R_R = \pi f$, where f is the measurement frequency. The G–T spectroscopy signal occurs because, by changing the temperature, we sweep R_C continuously from $<R_R$ at low temperatures to $>R_R$ at high temperatures, generating a conductance peak in the process.

The conductance from Eq. (1) appears in parallel with the semiconductor capacitance, and in series with the oxide capacitance, as depicted in Fig. 1(a). On the other hand, measurements frequently apply a parallel conductance–capacitance model to interpret the amplitude and phase relationships between the voltage and current signals [Fig. 1(b)]. Therefore, the first step in our method is to extract the trap conductance from the measured signal. The parallel conductance can be extracted from the measured capacitance (C_m) and conductance (G_m) by[18]

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \tag{2}$$

where C_{ox} is the oxide capacitance.

When using other analysis techniques, the conductance is frequently normalized before it is interpreted. In our case, it is convenient not only to normalize the conductance by dividing by ωA, as is common, but also to multiply it by T. This removes the $1/T$ term in Eq. (1), which can cause the peak location to shift slightly. On a plot of $G_P T/\omega A$ vs T, the peak occurs exactly when $R_C = R_R = \pi f$. Substituting this into Eq. (1), we get the following equation, which allows us to extract the trap density from the normalized conductance peak:

$$N_T = \frac{8k}{q^2} \left(\frac{G_P T}{\omega A} \right)_{peak}. \tag{3}$$

Next, to determine the trap depth, we need to describe the capture process. Using a semi-classical model, R_C is the product of

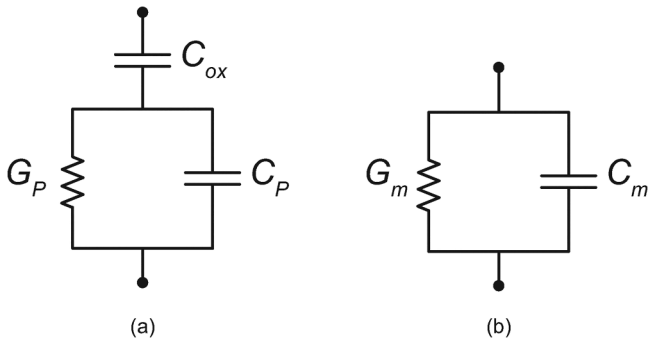

FIG. 1. (a) Equivalent circuit of a MOS capacitor and (b) the measured circuit.

the number of electrons that hit the interface per unit time and area (N_{hits}), the capture cross section (σ), and the tunneling probability (P),[15]

$$R_C = \sigma P N_{hits} = \sigma P \frac{4\pi m k^2 T^2}{h^3} \exp\left(\frac{q(\varphi_s - V_S)}{kT}\right), \tag{4}$$

where m is the electron effective mass, h is Planck's constant, and φ_S is the surface potential. V_S is the difference between the Fermi level and the bottom of the semiconductor conduction band in the bulk,

$$V_S = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right), \tag{5}$$

where N_D is the donor concentration and N_C is the effective density of states at the bottom of the conduction band.

At the peak, we can evaluate N_{hits} [see Eq. (4)]. Then, given that the capture rate at the conductance peak is equal to πf, Eq. (4) can be rearranged for P. Note that this requires using an assumed value for σ, and in the subsequent analysis this value is presumed to be independent of the applied temperature.[15] If a Wentzel–Kramers–Brillouin (WKB) approximation for a square barrier is used to model the tunneling probability, then the trap depth (x) is

$$x = x_0 \ln\left(\frac{\sigma N_{hits-peak}}{\pi f}\right), \tag{6}$$

with

$$x_0 = \frac{h}{4\pi\sqrt{2 m_t q \phi_B}}, \tag{7}$$

where m_t is the electron tunneling effective mass and ϕ_B is the barrier height (in eV).

Extraction of the trap depth and subsequent modeling of the G–T characteristic requires precise knowledge of φ_S. Any method to extract this quantity can be used; however, the capacitance–voltage (C–V) characteristic becomes highly non-ideal in the vicinity of the NI signal, meaning traditional methods based on the use of C–V curves may become unreliable.

To proceed, we propose a new technique to extract φ_S directly from the width of the NI peak in $G_P T/\omega A$ vs T plots. If the peak is described by Eqs. (1) and (4), then we can evaluate R_C at any point on the theoretical curve (in terms of the measurement frequency). Relevant examples of these R_C values are listed in Table I. We can then take two temperatures (T_1 and T_2), and assuming that φ_S is approximately constant between them, generate two simultaneous equations from Eq. (4). Solving for φ_S, we find

$$\varphi_s = \frac{-kT_2T_1}{q(T_1 - T_2)} \ln\left(\frac{R_{C1}T_2^2}{R_{C2}T_1^2}\right) + \frac{T_1 V_{S2} - T_2 V_{S1}}{T_1 - T_2}, \tag{8}$$

where the subscripts on R_C and V_S denote which temperature (T_1 or T_2) they are evaluated at.

TABLE I. NIT capture rate at various locations in $G_P T/\omega A$ vs T plots. Values given in terms of ω.

Percentage of peak conductance	R_C/ω	
	$T < T_{peak}$	$T > T_{peak}$
95	0.3410	0.7166
90	0.2863	0.8333
80	0.2172	1.0425
75	0.1918	1.1477
70	0.1698	1.2574
60	0.1330	1.5000
50	0.1027	1.7924

The choices of the two temperatures are critically important; too close, and the equations are ill-conditioned and prone to measurement error/noise, but too far away and the assumption of constant φ_S may break down. For this work, we will take T_1 and T_2 as the pair of points where the conductance is 70% of the peak value. This corresponds to $R_C = 0.1698\,\omega$ and $1.2574\,\omega$.

III. APPLICATION AND RESULTS

To test the characterization method, we fabricated MOS capacitor test structures on commercial 4H-SiC epitaxial layers with donor concentrations of $10^{16}\,\mathrm{cm}^{-3}$. The substrates were highly doped 4° off-axis n-type 4H-SiC wafers. For one sample, the oxide layer was formed by oxidation in dry O_2 at 1250 °C for 1 h; this was followed by post-oxidation annealing in pure NO for another hour at the same temperature. The final oxide thickness was approximately 41 nm, as measured by the accumulation capacitance at room temperature. For the second sample, the oxide was grown in pure NO for 20 h at 1250 °C. The final dielectric thickness was approximately 85 nm. Sputtered Al was used as the gate metals and the backside Ohmic contacts for both samples.

Sample conductance was measured with an Agilent E4980A LCR meter using a 10 mV signal amplitude. Measurements were performed in a closed-cycle helium cryostat controlled by a Lake Shore Cryotronics model 331 cryogenic temperature controller. Samples were pre-cooled to 50 K, followed by application of a DC gate bias between −0.5 V and −0.75 V for the NO annealed sample and between 0 V and 0.25 V for the NO grown sample. These voltage ranges correspond to depletion and to the appearance of the NI peak between ∼75 K and ∼200 K in the G–T spectra (depending on frequency and gate bias). As the samples were heated back to room temperature at a rate of 5 K/min, the conductance was periodically measured at seven different frequencies ranging from 1 kHz to 1 MHz.

Examples of the resulting G–T spectra are shown in Fig. 2 for the NO annealed sample and in Fig. 3 for the NO grown sample. The measurements of the NO annealed sample exhibit two distinct types of peaks. The smaller peaks at lower temperatures are due to nitrogen dopants in the bulk SiC.[13] The larger peaks are the so-called NI signal and are due to NITs.[12–16]

By comparison, the NO grown sample exhibits more peaks than the NO annealed spectra. The dopant signals are still present

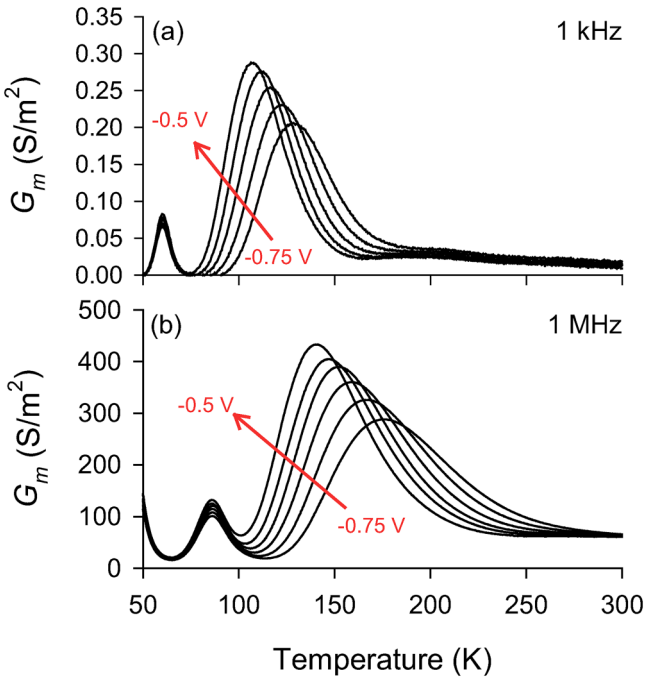

FIG. 2. Conductance–temperature spectra of the NO annealed MOS capacitors measured with a (a) 1 kHz and (b) 1 MHz test signal. The gate voltage was varied from −0.75 V to −0.5 V in 50 mV steps.

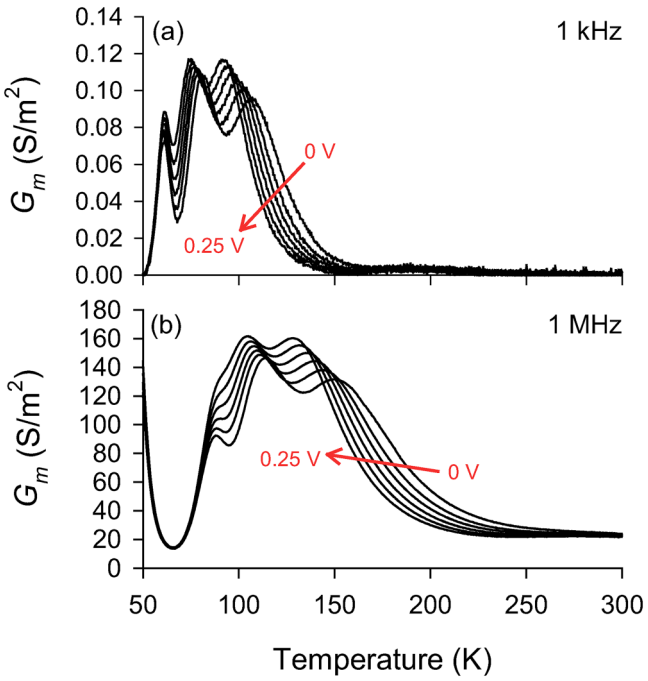

FIG. 3. Conductance–temperature spectra of the NO grown MOS capacitors measured with a (a) 1 kHz and (b) 1 MHz test signal. The gate voltage was varied from 0 V to 0.25 V in 50 mV steps.

at the same temperatures as in the NO annealed sample, but they are partially overlapped by two other peaks; the NI signal (which is the highest temperature peak) and a new defect signal unique to NO grown oxides which has not been reported previously. In the measured voltage range, this new peak is suppressed following the normalization; therefore, we will focus solely on the NI peak from this point onward.

The methods outlined in this paper can be used to extract the effective trap density, trap lateral depth within the oxide (distance from the interface), and φ_S from these peaks. The trap density as a function of gate bias and distance from the interface is shown in Fig. 4 for the NO annealed sample and in Fig. 5 for the NO grown sample. The different trap depths are obtained from measurements at different frequencies, with higher frequencies probing closer to the interface (since the tunneling probability is higher, traps closer to the interface respond faster).

The mean φ_S values at each gate bias are listed in Table II, assuming they are constant with temperature. In addition to the φ_S values, Table III lists E_C-E_F at the interface for select conductance peaks (where E_C is the bottom of the conduction band and E_F is the Fermi level).

To perform the extractions, we assumed a capture cross section of 10^{-13} cm^2, a barrier height of 2.7 eV, an electron effective mass of $1.2m_e$ (where m_e is the free electron mass), and a tunneling effective mass of $0.42m_e$.[15,19–21] Note that the contribution of the additional conduction band minima present in SiC has been included in the effective mass value.[20]

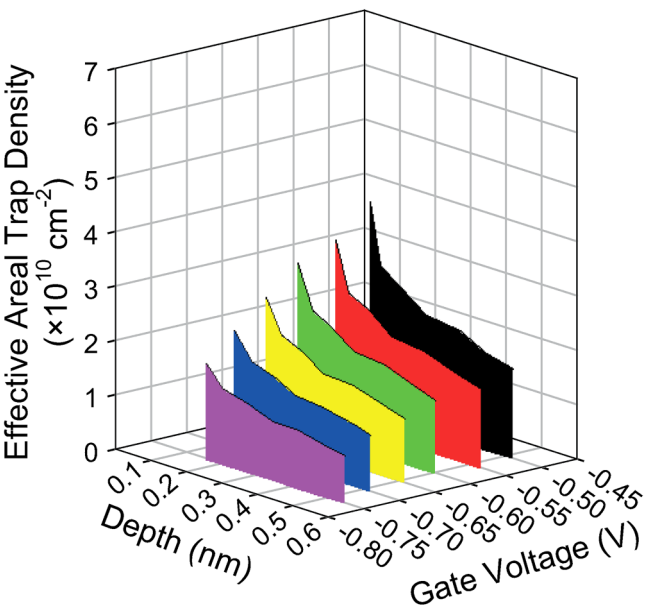

FIG. 4. Effective areal NIT density as a function of distance from the interface and the gate DC bias applied during the measurement for the NO annealed sample. Trap densities were evaluated using Eq. (3), while the lateral depth was determined by Eq. (6).

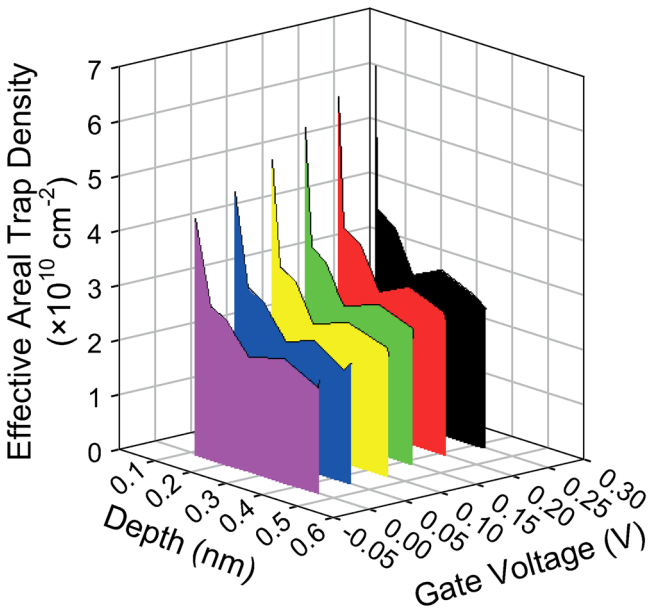

FIG. 5. Effective areal NIT density as a function of distance from the interface and the gate DC bias applied during the measurement for the NO grown sample. Trap densities were evaluated using Eq. (3), while the lateral depth was determined by Eq. (6).

The extracted parameters can be used to model the theoretical *G*–*T* spectra. A comparison of the theoretical and experimental measurements is shown in Fig. 6 for the NO annealed sample for gate biases of −0.5 V and −0.75 V and for frequencies of 1 kHz and 1 MHz. Figure 7 shows the same comparison for the NO grown sample (with different gate biases). There is good agreement in the vicinity of the peak, especially at low frequencies. Note that to plot the modeled curves, we have assumed that the properties in the vicinity of the peak (namely, σ and φ_S) are temperature independent and can be extended to regions away from the peak. We also assumed complete ionization of the dopants, which is justified at the considered temperatures even though some error can be contributed by this assumption (note that the surface electric field will cause additional ionization at the interface as compared to the bulk semiconductor).

TABLE II. Surface potential extracted from Eq. (8) for each sample and gate bias. Values are averaged from measurements at different frequencies. The minimum and maximum deviations from the mean are also listed (in meV).

NO annealed		NO grown	
Gate bias (V)	Mean surface potential (meV)	Gate bias (V)	Mean surface potential (meV)
−0.75	$-94.0^{+1.4}_{-1.2}$	0	$-89.1^{+6.1}_{-2.9}$
−0.70	$-93.2^{+2.1}_{-1.7}$	0.05	$-85.9^{+5.3}_{-2.7}$
−0.65	$-91.6^{+2.0}_{-1.9}$	0.10	$-84.2^{+5.3}_{-3.5}$
−0.60	$-89.7^{+1.7}_{-1.7}$	0.15	$-84.0^{+5.0}_{-3.2}$
−0.55	$-85.6^{+3.6}_{-2.5}$	0.20	$-83.0^{+4.0}_{-2.2}$
−0.50	$-83.6^{+3.0}_{-3.1}$	0.25	$-81.6^{+3.6}_{-2.9}$

TABLE III. Difference between the conduction band minimum (E_C) and the Fermi level (E_F) at the interface for the highest measured gate voltages (V_G) of both samples (−0.5 V and 0.25 V for the NO annealed and NO grown samples, respectively). Data shown at four different temperatures, corresponding to the locations of the $G_pT/\omega A$ peaks for four different measurement frequencies (1 kHz, 10 kHz, 100 kHz, and 1 MHz).

	NO annealed ($V_G = -0.50$ V)		NO grown ($V_G = 0.25$ V)	
Frequency (kHz)	Peak T (K)	E_C-E_F (meV)	Peak T (K)	E_C-E_F (meV)
1	116	140	103	133
10	127	150	116	142
100	141	163	132	154
1000	166	176	160	169

IV. DISCUSSION

The conductance peaks that we measure occur at similar temperatures to other signals detected using the deep level transient

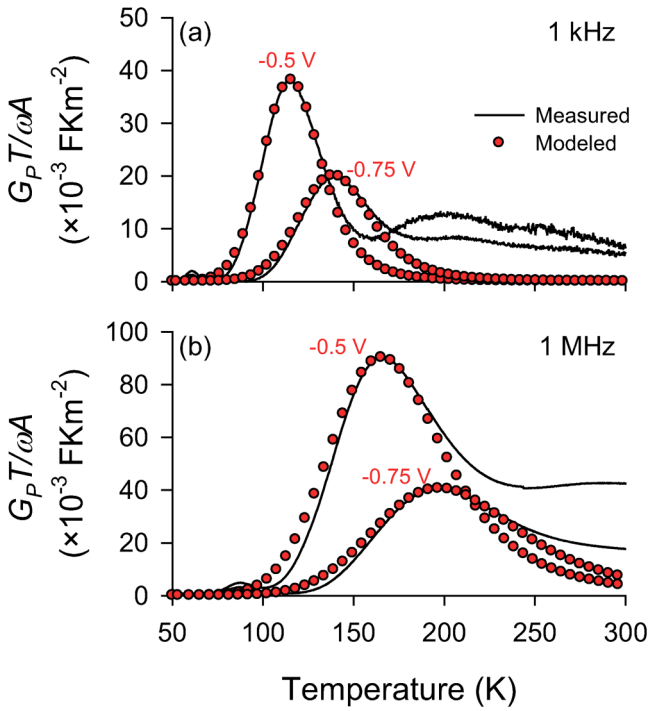

FIG. 6. Measured (lines) and modeled (symbols) normalized conductance–temperature spectra for the NO annealed MOS capacitors at (a) 1 kHz and (b) 1 MHz. To improve clarity, only data at the highest and lowest gate biases are shown (−0.5 V and −0.75 V). The modeled plots are constructed from Eqs. (1) and (4), using the extracted parameter values.

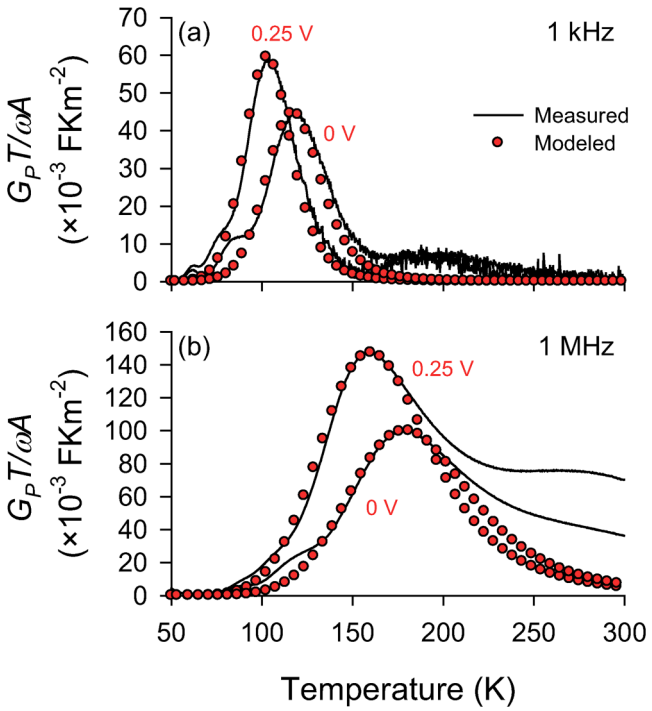

FIG. 7. Measured (lines) and modeled (symbols) normalized conductance–temperature spectra for the NO grown MOS capacitors at (a) 1 kHz and (b) 1 MHz. To improve clarity, only data at the highest and lowest gate biases are shown (0.25 V and 0 V). The modeled plots are constructed from Eqs. (1) and (4), using the extracted parameter values.

spectroscopy (DLTS) or thermal dielectric relaxation current (TDRC) techniques.[22,23] Therefore, it is tempting to try to compare those established methods to our characterization. However, both DLTS and TDRC mainly detect the interface trap signal present in thermally grown oxides. This signal (which sometimes labeled "OX" in G–T spectroscopy measurements) is strongly reduced following nitridation and only contributes a weak background signal to the present measurements.[12–15] DLTS and TDRC are fundamentally low frequency (<1 kHz) measurements, and they rely on the temperature dependent emission process for interface traps. This is different from the higher frequency temperature-independent release process being probed in this work. Therefore, we expect no correlation between those signals and the NI signal that we are investigating.

We can attempt to estimate the volumetric trap densities from the effective areal densities given in Figs. 4 and 5. To do this, let us assume that the trap occupancy is governed by a logistic function of lateral depth which is normalized by x_0. This is equivalent to the Fermi-Dirac distribution, but in distance rather than energy and with x_0 replacing kT in the exponential. In these circumstances, the volumetric trap densities can be approximated by dividing the areal densities by x_0. Doing this gives values on the order of $\sim 10^{18}$ cm^{-3}, a value that seems reasonable. However, the validity of assuming such a distribution is questionable. Furthermore, there is no salient energy scale to use here, and so this estimation is still unable to account for the energy distribution.

The properties extracted via our new characterization technique can be used to draw some basic conclusions about the nature of the NITs being measured. For instance, we can see that the effective trap density appears to decay with distance away from the interface. This is in line with some measurements of the defect density in SiC MOS capacitors[24] and some others attempt to electrically characterize NITs.[25,26]

The length scales involved are on the order of inter-atomic distances. The distribution appears continuous and not discrete as would be expected of an ordered bond structure. This points to a region of high disorder at the interface, which generates a variety of bond lengths and so makes the trap distribution appear continuous. Such a region has been observed by other groups in SiC MOS capacitors.[24,27–30] The trap density increases with increasing gate bias; this may indicate an energetic distribution of traps, which would also be expected for a disordered interface region.[31]

The NO grown devices exhibit a higher density of NITs as compared to the NO annealed capacitors. This is especially the case for the fast traps very near the interface. A higher density of very fast NITs in NO grown oxides has been observed using other electrical characterization techniques.[32] X-ray photoelectron spectroscopy studies have shown a higher concentration of nitrogen at the interface in NO grown vs NO annealed gate oxides.[33] This correlates with the higher NIT densities we observe, and so may indicate a possible defect origin. We would expect that the higher concentration of fast NITs in NO grown oxides would result in lower channel-carrier mobility as compared to NO post-oxidation annealing. However, interfacial nitrogen also reduces the interface state density.[1–11] Mobility measurements on SiC MOSFETs will be necessary to determine whether the increasing NIT density or the decreasing interface trap density dominates the relationship between the nitrogen concentration at the interface and MOSFET mobility.

There are some limitations of the presented method, particularly involving the φ_S. Any dependence of φ_S on temperature beyond linear it not accounted for and factors that cause peak-broadening (such as large φ_S fluctuations, other signals, and temperature dependencies that are unaccounted for) will also result in errors in the extracted value. As we move to lower temperatures, we also need to consider that the donors will no longer remain fully ionized, as stated previously. Despite these limitations, the extracted values are still effective for modeling purposes, as demonstrated by the agreement between the model and the measurements in Figs. 6 and 7. Also, the trap density information does not depend on φ_S, and so still provides a useful metric for comparing capacitors.

V. CONCLUSION

In this work, we have derived and applied the equations for a new method of characterizing NITs in nitrided SiC MOS capacitors. The method allows for fast approximation of the trap densities, lateral depths, and the surface potential, using G–T spectroscopy measurements. The obtained results enable evaluation and comparison of MOS fabrication processes for use as the gate dielectric in SiC MOSFETs. The equations also enable modeling of

the G–T spectra, providing some insight into the physical origin of the responsible traps. The method can be applied to signals other than the NI peak, such as those in MOS samples with different dielectrics/semiconductors, provided that the signal in question is caused by NITs.

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APPENDIX: DERIVATION OF CONDUCTANCE

The occupancy probability of a trap (f_T) is governed by the following differential equation (using small signal notation):[15,17]

$$\frac{df_T}{dt} = r_C(1 - f_T) - r_R f_T. \tag{A1}$$

The capture rate can be expressed in terms of the applied signal,[15,17]

$$r_C = R_C \exp\left(\frac{qv}{kT}\right) \approx R_C[1 + v_{th}], \tag{A2}$$

where v is the oscillation in the surface potential due to the applied voltage and $v_{th} = qv/kT$. If we substitute Eq. (A2) into Eq. (A1), split f_T into a sum of a small signal part and a bias and substitute $r_R = R_R$ (since the release process is independent of the applied signal), we get

$$\frac{df_t}{dt} = R_C(1 + v_{th})(1 - F_T - f_t) - R_R(F_T + f_t). \tag{A3}$$

Assuming that f_t is sinusoidal, then

$$\frac{df_t}{dt} = j\omega f_t. \tag{A4}$$

Furthermore, in the absence of a small signal, we can derive from Eq. (A1) that

$$F_T = \frac{R_C}{R_C + R_R}. \tag{A5}$$

Substituting Eqs. (A4) and (A5) into Eq. (A3) and rearranging

$$f_t = \frac{R_C R_R}{R_C + R_R} v_{th} \frac{R_C(1 + v_{th}) + R_R - j\omega}{[R_C(1 + v_{th}) + R_R]^2 + \omega^2}. \tag{A6}$$

The current produced by the traps is[15,17]

$$i = qAN_T \frac{df_t}{dt}. \tag{A7}$$

Combining Eq. (A7) with Eqs. (A6) and (A4), and assuming $v_{th} \ll 1$, the admittance (Y) can be derived as

$$Y = \frac{q^2 AN_T}{kT} \times \frac{R_C R_R}{R_C + R_R} \times \frac{\omega^2 + j\omega(R_C + R_R)}{(R_C + R_R)^2 + \omega^2}. \tag{A8}$$

The parallel conductance is the real part of Eq. (A8).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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