Progress in p-type Tunnel Oxide-Passivated Contact Solar Cells with Screen-Printed Contacts

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Herein, an update on the work on high-efficiency p-type solar cells with p-type-passivating rear contacts formed by low-pressure chemical vapor deposition and screen-printed contacts is given. It is shown that thin polysilicon layers enable a high level of surface passivation but do show increased contact resistivity and especially contact recombination. Commercially available pastes and dependence of contact resistivity and contact recombination on polylayer thickness and firing set temperature are investigated. For 240 nm-thick poly-Si layers, the values down to 4 mΩ cm^2 and 60 fA cm^{-2} are observed. For the presented process sequence, improved hydrogenation as one possibility to increase the passivation quality of the passivating contact structure is identified. Implementing all findings into a final solar cell, a maximum total area conversion efficiency of 21.2% is reported.

1. Introduction

P-type silicon solar cells are still the working horse for the photovoltaic community. The majority of these solar cells are fabricated in the passivated emitter and rear cell (PERC) architecture.[1] However, currently, there is large interest in solar cells with passivating contacts, which consist of an interface oxide in combination with a doped deposited silicon layer[2,3] and which are denoted as, e.g., tunnel-oxide passivated contacts (TOPCon).[4] For most of such solar cells, the TOPCon layer is placed at the cell's rear side, where, in general, a high−low junction is formed, i.e., base substrate and TOPCon layers are of the same doping types. As the n-type passivating contact has some physical and technical advantages over the p-type counterpart such as passivation quality or a more straightforward

metallization by screen-printed silver pastes,[5] most TOPCon solar cells are fabricated on n-type wafers.[6–11]

However, a possible integration into existing PERC lines would be a lot easier if large parts of the process sequence can be left unchanged, which explains the interest in p-type TOPCon solar cells and why we rate this approach to be of industrial relevance. For p-type solar cells with p-type passivating rear contacts, work often focuses on simulation[12–15] as certain input parameters can be obtained from test structures or characterization of test structures.[16] However, the actual demonstration of a solar cell with screen-printed metallization that comes near the determined efficiencies in simulation can be challenging, for the reasons explained earlier, resulting only in a limited amount of publications.[17,18] Alternatively, in other contributions, physical vapor deposition (PVD) is used often for rear metallization[19–22] due to the noninvasiveness of this technology. As laser damage from local ablation of dielectric capping layers can be kept to a minimum if the polysilicon layer does not go below a certain thickness,[21] the TOPCon interface properties should ideally not be affected by metallization. Yet, in photovoltaics manufacturing, screen printing is and probably will stay the technology of choice for years to come, due to its low complexity, low capital expenditure, and high throughput.[1] For screen printing, the task is to develop suitable metallization pastes for p-type TOPCon layers that allow for low contact resistivity and low carrier recombination at the same time.

This article gives an update on our work on p-type solar cells with a p-type-passivating rear contact formed by low-pressure chemical vapor deposition (LPCVD) of an in situ boron-doped polysilicon layer on top of an in situ-grown tunnel oxide. The process sequence thus makes use of the optimizations identified in the past, such as alkaline saw damage-etched surfaces,[23] optimized screen-printed Ag pastes for poly-Si metallization[24] in combination with a busbarless layout for reduced contact resistances at the rear,[18] and optimizations of the process sequence itself.[18] The bifacial layout of the solar cells makes them especially suited for bifacial modules, to benefit from rear albedo. First, we report on the impact of polysilicon layer thickness d on the passivation quality and show experimentally determined values for contact recombination and contact resistivity of several commercially available Ag and Ag-/Al-based metallization pastes. Then, we will integrate the identified metallization pastes in our cell process, indicate related challenges, and propose ways for further improvement.

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2. Sample Preparation

As to the best of our knowledge, when we conducted the experiment, there were no dedicated pastes available for metallization of p^+ TOPCon layers. Because of this, there was a very high need for development of such pastes, which ideally featured a low contact resistivity and at the same time a low contact recombination. Our approach for determination of the status of paste development is explained in the following paragraphs.

For fabrication of test structures, M2-sized n-type wafers with a thickness of 200 μm are used. After saw damage removal in alkaline solution and wet chemical cleaning, formation of the passivating contact takes place in an LPCVD tube furnace system. The passivating contact consists of an interface oxide of around 1.2−1.4 nm thickness and an in situ boron-doped polysilicon layer, both of which formed in the same process without vacuum breakage. Please note that this experiment includes a variation of the polysilicon layer thickness, d, namely, $d = 96$, 144, 192, and 240 nm, which is realized by controlling the process time in four subsequent process runs. A subsequent annealing step at 900 °C for 30 min in nitrogen ambient activates the dopant and forms the rear dopant profile underneath the interface oxide. This is followed by direct plasma-enhanced chemical vapor deposition (PECVD) of a SiN_x:H layer onto both sides. These samples are being used to identify the most promising screen-printed metallization paste. To compensate for the limited amount of samples available, several commercially available Ag and Ag-/Al-containing metallization pastes have been selected and 5−6 from them have been screen printed onto one single wafer at different positions, using 5−6 screens per wafer, as indicated shown in **Figure 1**. In the following, the pastes will be labeled using consecutive letters, i.e., pastes A to H are Ag pastes and pastes I to L are Ag/Al pastes. Finally, the samples are subject to contact firing in an industrial conveyor belt furnace at three different set temperatures of $T_{set} = 810$, 840, and 870 °C. Thus, as in total 11 different Ag-containing pastes from four suppliers have been evaluated on each polysilicon layer thickness and for each firing set temperature, this experiment includes a total of 132 groups. Each group consists of 3−4 wafers.

Each printed layout from Figure 1 contains two fields, one for the determination of the contact resistivity ρ_c and a second one for evaluation of the contact recombination $J_{0,met}$. The small field features parallel, not connected, fingers with a distance of 1 mm and an opening width of 50 μm. This structure serves for determination of the contact resistivity ρ_c by laser scribing stripes of 1 cm width with isolation of the edges of the fingers, applying the transfer length method (TLM). The large field with parallel, not connected, fingers with a finger distance of 0.5 mm and a similar opening width of 50 μm in the screen, yielding a metallization ratio of roughly 10%, allows for the determination of contact recombination $J_{0,met}$ by photoluminescence (PL) imaging and numerical simulations, as explained in the study by Herrmann et al.[25] Please note that this procedure of printing several metallization pastes onto one wafer implicates that the paste printed first is dried 5−6 times, whereas the paste printed last is dried only once. For a total of 11 metallization pastes tested, this led to problems with adhesion in two cases. In most figures in this work, however, for clarity, we will only show results for selected pastes. The nonmetallized centre of the wafers enables a quasi steady-state photoconductance (QSSPC) measurement using a Sinton Lifetime Tester WCT-120. The surface recombination parameter J_0, pass is then extracted using the procedure described in a study by Kimmerle et al.[26]

The boron-doped Cz−Si wafers, which are used for solar cell fabrication, are 190 μm thick and of M2 dimension. As for the test samples, the process sequence starts with saw damage removal, cleaning, interface oxide formation, in situ boron-doped poly-Si deposition, and thermal annealing, as shown in **Figure 2**, with the same processes described earlier and $d = 240$ nm. Here, a SiN_x:H capping layer of 75 nm is deposited only on one side, which will be the rear side in the final device. Next, random pyramids are formed on the nonprotected front side by etching in alkaline solution, which, elegantly also removes the parasitic, unwanted deposition of the polysilicon layer on the front side. This is followed by $POCl_3$ diffusion with a sheet resistance of 90−95 Ohm/sq., phosphosilicate glass (PSG) removal, cleaning, and front-side passivation by a combination of thermal annealing and SiN_x:H deposition by PECVD. The rear-side SiN_x:H layer acts as an etch mask and diffusion barrier during these processes, which causes its thickness to decrease slightly.

Our metallization approach is based on the use of fire-through screen-printed Ag pastes on both sides of the samples, here in a busbarless layout with 110 fingers on the front and 208 fingers on the rear side. The actual finger width is around 40 μm on front and 50 μm rear side, respectively, yielding metallization ratios of 2.8% and 6.7%. Processing concludes with conventional contact cofiring in a conveyor belt furnace. Figure 2 (right) shows a schematic cross section of the solar cell. All solar cells reported in this article have a total area of 244.3 cm^2.
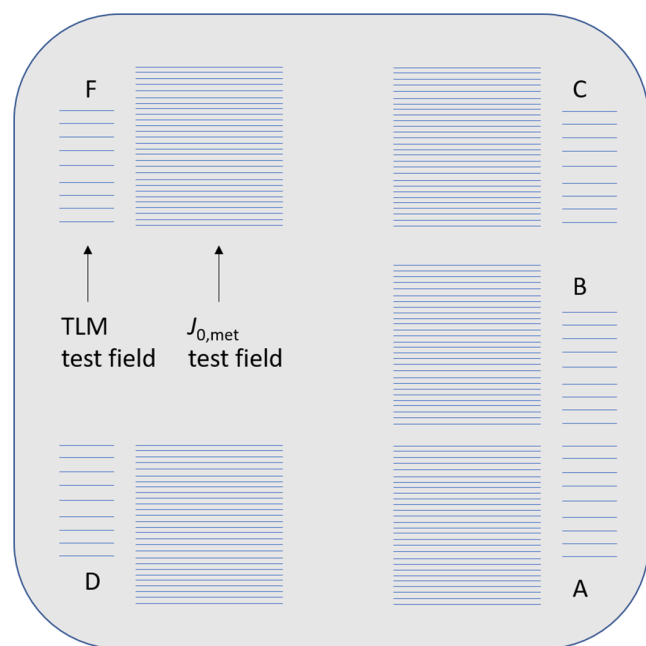

Figure 1. Schematic drawing of a test wafer with five different metallization pastes screen printed onto it in five subsequent printing steps.
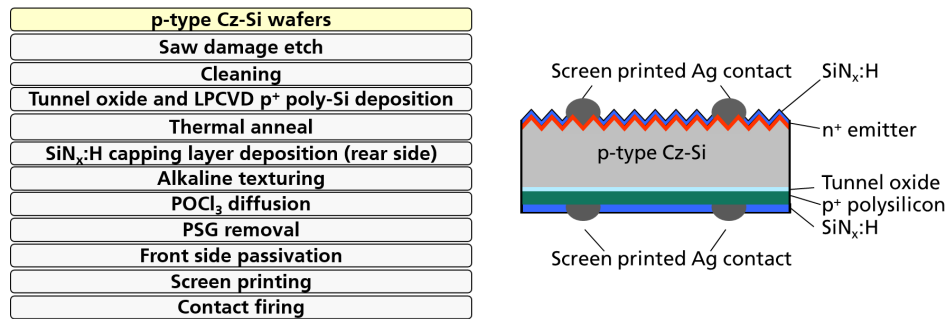
Figure 2. (left) Process flow for the fabrication of p-type TOPCon solar cells. (right) Schematic cross section of the fabricated solar cells.

3. Results

3.1. Dopant Profile

During thermal annealing, the polysilicon layer acts as a dopant source, and annealing parameters are chosen such that some boron dopant also is driven into the silicon wafer. As the experiment also includes a variation of the polysilicon layer thickness d, the different doping doses could have an impact on the resulting dopant profile in the c-Si substrate. To investigate this in more detail, electrochemical capacitance voltage profiling (ECV) measurements have been carried out, and the results are shown in **Figure 3**. On the one hand, the position of the SiO_x interface is clearly indicated by a rather constant dopant concentration within the polysilicon layer and a steep decrease in N_A beyond the interface. The determined thicknesses correspond very well with the targeted values. On the other hand, it becomes clear that higher thicknesses result in an increase in the averaged polysilicon dopant concentration, from 4.8×10^{19} cm^{-3} for the 96 nm-thick layer to 6.3×10^{19} cm^{-3} for 240 nm-thick layer. The corresponding overall sheet resistances R_{sheet} for the polysilicon layer including the tail, as measured by four-point-probe (4pp) measurements on n-type reference wafers, are shown in Figure 3. For unknown reasons, the process with the 192 nm-thick layer has a slightly more pronounced tail in crystalline silicon than the other profiles. Please note that we smoothed the data in the plateau region over seven data points for better visibility.

3.2. Passivation Quality

The results of symmetric carrier lifetime samples, which represent the rear side of the solar cell without metallization, are shown in **Figure 4**. The QSSPC measurements have been carried out after annealing, double-sided SiN_x:H deposition, and contact firing in the center of the metallized wafer. The results indicate a passivation quality, which might be somewhat linked to differences in the dopant concentration and profile of the passivating contact, which includes the tail in crystalline silicon underneath the tunnel oxide, as similar J_0 results have been expected. Overall, $J_{0,pass}$ is in the range of $10-20$ fA cm^{-2}, which is just at the edge of being acceptable for the investigation presented later, but considerably larger than values achieved in the past, where, typically, $J_{0,pass} < 4$ fA cm^{-2} has been reached,[24] and similar values have been reported also by other authors.[15,22] At this point, the reason
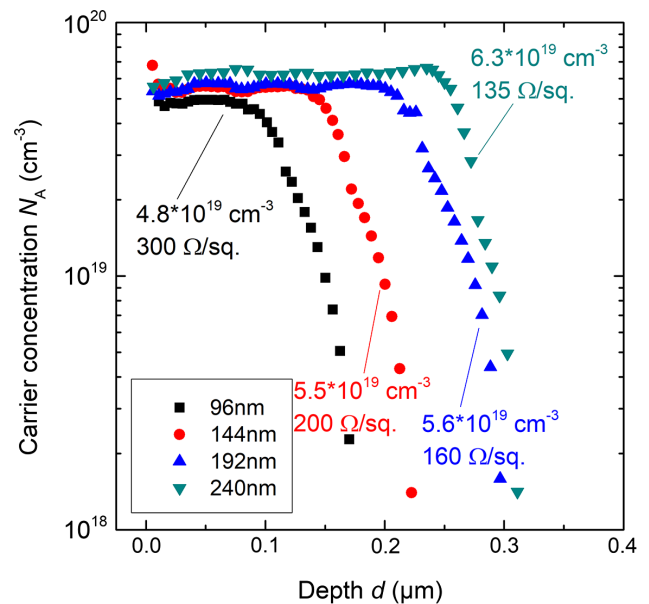

Figure 3. Active dopant concentration of polysilicon layers and resulting doping profile for variations in the polysilicon layer thickness measured by ECV in the center of one wafer. Please note that we smoothed the data over seven measurement points in the plateau region.

for the rather high recombination current densities is unclear. There is a tendency toward lower $J_{0,pass}$ for higher firing set temperatures T_{set}, in accordance with earlier results.[24] In addition, the higher $J_{0,pass}$ for the 192 nm-thick layer correlates well with the stronger tail shown in Figure 3. The lower $J_{0,pass}$ for the 96 nm process might be as well linked to the lower doping density, which leads to less in-diffusion. Alternatively, it might be a result of an improved surface passivation by the interface oxide due to a lower resulting boron concentration within the oxide layer itself, as boron solubility in oxide layers is higher than that in silicon,[27] and increased boron concentrations in silicon oxide layers are known to enhance recombination.

3.3. Contact Resistivity

Figure 5 (left) shows the contact resistivity ρ_c of all pastes for a fixed polysilicon layer of thickness $d = 240$ nm plotted versus the
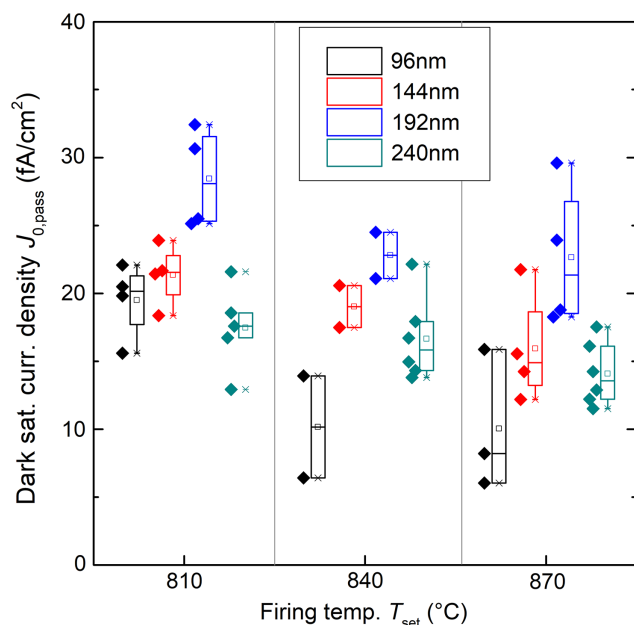
Figure 4. Recombination parameter $J_{0,pass}$ for different polysilicon layer thicknesses determined by QSSPC on symmetric lifetime samples after SiN$_x$:H deposition and contact firing at different set temperatures.

firing set temperature T_{set}. Pastes A−H represent Ag pastes and pastes I−L represent Ag/Al pastes. Overall, Ag/Al pastes do not show low ρ_c in this experiment; in the following paragraphs, we will therefore focus on Ag pastes. The results indicate a strong dependency of ρ_c on T_{set}. For the lowest firing set temperature of 810 °C and $d = 240$ nm, ρ_c was found to be higher than 100 mΩ cm^2 for 9 out of 11 pastes. For clarity, the values are not shown in Figure 5. However, it is noteworthy that Ag paste C did indeed lead to $\rho_c = 27$ mΩ cm^2 at that firing temperature. Increasing T_{set} to 840 °C reduced ρ_c to 4−5 mΩ cm^2 for three pastes, and at $T_{set} = 870$ °C, the lowest $\rho_c = 3$ mΩ cm^2 is found for several Ag pastes, whereas for other Ag pastes, ρ_c is still in the range of 200 mΩ cm^2 and even higher for some Ag/Al pastes, indicating no contact formation. It appears, as for most pastes tested, that firing set temperatures of $T_{set} = 870$ °C are needed, to allow for low ρ_c, which, however, might be too high for solar cell integration. At $T_{set} = 840$ °C, only 2−3 pastes yield low ρ_c; however, one of them showed very low adhesion, which led to

the paste mainly peeling off, because of which this paste has not been taken into account any further for solar cell testing. It must be mentioned that the saw damage-etched rear surface represents a challenge for contact formation and that pastes might lead to lower contact resistivity on, e.g., alkaline-textured surfaces. Figure 5 (right) shows the dependency of ρ_c for the two most suitable pastes fired at $T_{set} = 840$ °C, for different polysilicon layer thicknesses plotted versus T_{set}. As discussed, ρ_c decreases significantly for higher polysilicon layer thicknesses. For example, for paste C and a firing set temperature of $T_{set} = 840$ °C, ρ_c decreases from around 100 mΩ cm^2 for a 96 nm-thick layer to $\rho_c = 4$ mΩ cm^2 for a 240 nm-thick layer. This behavior might partly be linked to the slightly higher maximum dopant concentration at the surface in the thicker polysilicon layer, but mainly due to the higher dopant reservoir for the thicker layer, which facilitates contact formation. Overall, we observe that for effective contacting, mainly dedicated TOPCon pastes should be used, and some of the pastes which are being promoted for n-doped TOPCon layers also work quite well for p-doped TOPCon layers. The main findings are in good agreement with other early investigations from our side[24] and other authors.[7,15,28–31] The comparison of both pastes for the same polysilicon thickness reveals that paste C forms a lower ohmic contact than paste F at $T_{set} = 840$ °C firing, but at $T_{set} = 870$ °C, the opposite holds true.

3.4. PL Imaging

Of course, contact resistivity is only one part of the equation, and the related minority carrier recombination at the metal contacts is of high importance as well. **Figure 6** shows the PL images of samples with polysilicon thickness $d = 96$ nm (top row) and $d = 240$ nm (bottom row), with a variation of the firing set temperature of $T_{set} = 810$ °C (left), 840 °C (middle), and 870 °C (right). The five large different fields indicate the five metallization pastes, which are present on this wafer. As apparent from the lower luminescence signal and thus darker appearance, the use of paste D results in a higher recombination than for paste C on each wafer, respectively. This trend is visible on all six wafers shown here.

Apparently, the interaction between metallization paste and the polysilicon layer cannot be neglected, and carrier recombination is increased locally, where the paste is printed. This finding
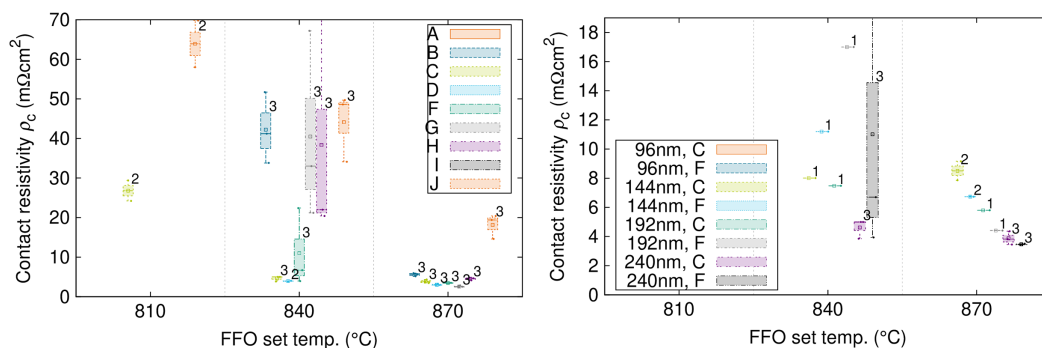

Figure 5. (left) Contact resistivity ρ_c for all pastes and firing set temperatures T_{set} and fixed polysilicon thickness of $d = 240$ nm. Pastes K and L are beyond the scale. (right) Contact resistivity ρ_c for two Ag pastes, plotted versus the firing set temperature T_{set}, with d as parameter.
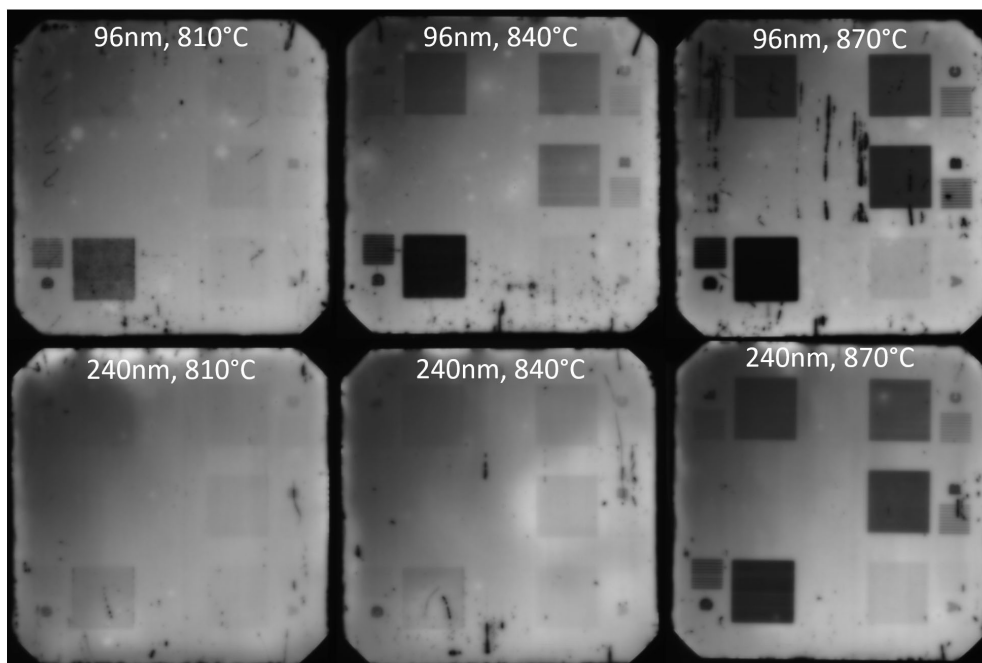
Figure 6. PL images recorded from the nonmetallized side, for the same set of five metallization pastes, with polythicknesses of 96 nm (top row) and 240 nm (bottom row) and firing set temperatures of 810 °C (left), 840 °C (center), and 870 °C (right).

agrees with other literature data[24,28,31] and again highlights the complexity when identifying screen-printed metallization pastes for TOPCon layers, and keeping the passivating contact intact can be at least challenging.

Paste A does not form any contact at all; in fact, it is one of the pastes mentioned earlier, that also fell off the wafers during contact firing. Comparing the six wafers, luminescence at the test fields decreases with higher firing set temperature (from left to right side) or thinner polysilicon layers (top versus bottom), both indicating higher damage to the interface oxide. For brevity, the PL images of $d = 144$ nm and $d = 192$ nm are not shown here, but the effect of decreased luminescence for decreasing polysilicon thickness d also holds true here.

Separate from the metallized test fields, an inhomogeneity of the PL signal background ϕ over the sample becomes obvious. In numbers, e.g., for the sample with $d = 240$ nm and $T_{set} = 870$ °C, the PL signal in the upper-left (nonmetallized) corner is $\phi \approx 7500$ counts/pixel whereas in the upper-right corner it is $\phi \approx 19\,500$ counts/pixel. The origin for this finding is so far unclear. As this finding is present on all samples though, either a tunnel oxide of different thicknesses in that corner or a differing dopant concentration compared with the rest of the wafer, which formed during polysilicon layer deposition, might be a possible explanation. This might lead, for example, to an enhanced or equally possible retarded carrier in-diffusion during annealing and thus a reduced passivation quality.

3.5. Contact Recombination

Using a combination of lifetime and PL measurements supported by numerical simulations in Quokka3,[25] we are able to determine absolute values for $J_{0,met}$. We account for the

nonuniformity of the PL signal background ϕ by the use of additional reference fields in the direct vicinity of the test fields. For more reliable data, another approach for sample preparation is preferred, as described in the study by Herrmann et al.[32] However, this was not implemented in the experiments of this work due to the high complexity and the large number of process variations. As explained earlier, for the PL images in Figure 6, the vicinity of paste F shows a lower PL signal than the other three corners. As also mentioned earlier, a varying tunnel oxide thickness or doping profile might be the reasons for that, which might as well influence the determined $j_{0,met}$ values.

The results are shown in **Figure 7**, for two exemplary pastes, paste F (left), which was used in previous experiments,[24] and paste C (right), which has been identified as a promising paste due to its rather low ρ_c at $T_{set} = 840$ °C in this work. Intuitively, $J_{0,met}$ increases for a higher firing set temperature, as was apparent from the PL images shown in Figure 6, presumably due to the deeper penetration of the metallization paste into the passivating contact. This affects the interface properties and once again shows that the use of the expression "passivating contacts" might be partially not fulfilled in its original meaning, at least for the samples and pastes investigated in this study, in accordance with literature.[15] For lower polysilicon layer thickness d, a trend toward higher $J_{0,met}$ is visible, at least for firing set temperatures of $T_{set} = 840$ °C and above, where the pastes form a contact with a reasonable contact resistivity. At $T_{set} = 810$ °C, the pastes do not form a low ohmic contact to the polysilicon layer and thus, the low $J_{0,met}$ results are probably not relevant. The comparison of Figure 7a,b reveals quite similar $J_{0,met}$ for both pastes. For example, for paste F and $d = 240$ nm, we find quite low $J_{0,met} = 63$ fA cm^{-2} at $T_{set} = 840$ °C and $J_{0,met} \approx 240$ fA cm^{-2} at $T_{set} = 870$ °C firing and $J_{0,met}$ at ≈ 64 fA cm^{-2} and $J_{0,met}$ at
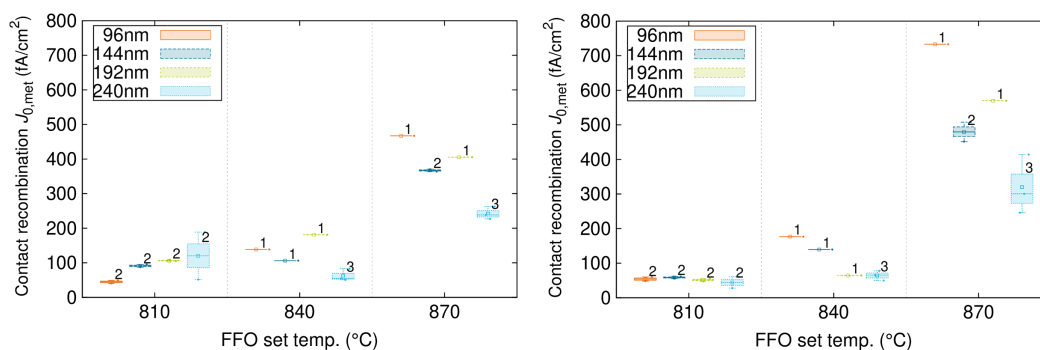
Figure 7. Results of the $J_{0,met}$ analysis determined by PL analysis and numerical simulation for paste F (left) and paste C (right) plotted versus the firing set temperature and with the polysilicon layer thickness as a parameter.

$\approx 320 \, \text{fA cm}^{-2}$ for paste C, respectively. These data are slightly lower than values reported by other authors.[15] Thus, at $T_{set} = 840\,°C$, the two pastes yield quite similar $J_{0,met}$ values, whereas at $T_{set} = 870\,°C$, paste C shows slightly higher $J_{0,met}$ than paste F. We conducted a similar analysis for all investigated pastes and the results varied up to $280 \, \text{fA cm}^{-2}$ at $d = 240 \, \text{nm}$ and $T_{set} = 840\,°C$. In addition, $J_{0,met}$ as high as $1500 \, \text{fA cm}^{-2}$ has been determined at $d = 240 \, \text{nm}$ and $T_{set} = 870\,°C$, which is considerably higher than the values shown in Figure 7 and highlights the necessity to select appropriate metallization pastes and firing conditions.

3.6. Solar Cells: Passivation Quality

The implied open circuit voltage iV_{oc} as well as the implied fill factor iFF as determined by QSSPC measurements are important characteristics when it comes to evaluating the efficiency potential of cell precursors, i.e., solar cells without metallization. In contrast to, e.g., J_0 values, which describe the effective surface recombination at a virtual surface, both iV_{oc} and iFF not only take into account the recombination at surfaces, but also in the wafer itself, and both are determined at different injection levels, which makes them especially interesting. These values represent upper levels to the open-circuit voltage V_{oc} and the pseudo-fill factor pFF. The following **Figure 8** shows measurement results for iV_{oc} and iFF of solar cell precursors that have been processed with the process flow of Figure 2 but without screen-printing steps. In addition, for a second group, we increased the duration of the phosphosilicate glass removal step, which leads to the complete removal of the rear SiN_x:H layer. For this group, we deposited a renewed SiN_x:H layer on the rear surface after front passivation.

For the reference group "original SiN_x:H layer", where the rear SiN_x:H layer is left in place, median $iV_{oc} = 684 \, \text{mV}$ and $iFF = 84.2\%$ are determined. However, the replacement of the rear SiN_x:H layer by a renewed one leads to a strong increase to $iV_{oc} = 698 \, \text{mV}$ and $iFF = 84.9\%$. The results are a strong evidence toward a so far insufficient hydrogen passivation of the rear interface oxide for the reference group, which would lead to a higher recombination and thus a lower passivation quality. We expect the initial rear SiN_x:H layer to lose hydrogen during further processing, especially during $POCl_3$ diffusion, in accordance with findings for another process sequence.[33] The

renewed SiN_x:H layer thus provides more hydrogen during contact firing, which leads to an overall reduced recombination and thus higher iV_{oc} and iFF values. A modification of the SiN_x:H layer, which is deposited after polysilicon layer annealing, e.g., by an increased hydrogen concentration, would be an option to increase the iV_{oc} and iFF for the simpler reference cell process. The importance of efficient hydrogenation of the interface has also been stressed in another publication.[34] Alternatively, also, annealing of polysilicon layers in mixtures of water vapor and nitrogen has been reported to be effective in reducing overall carrier recombination.[35] The high iV_{oc} level close to 700 mV reveals that the bulk lifetime for the p-type wafer remains high despite the use of two thermal processes in the sequence, annealing of the polysilicon layer and $POCl_3$ diffusion. PL images did not show indication for ring structures; thus, the minority carrier lifetime in the bulk seems to not be strongly affected by oxygen precipitation.[36]

3.7. Solar Cells: Cell Results

Apparent from Figure 5 and 7, the pastes F and C enable both low contact resistivity and moderate contact recombination and thus were chosen for solar cell processing. Three groups of solar cells are fabricated according to Figure 2 with polysilicon layer thickness $d = 240 \, \text{nm}$: a first group with the reference paste F,[24] a second group with paste C, and a third group with the same paste C but a renewed rear SiN_x:H layer, as described earlier in "Solar cells: Passivation Quality". Apart from the rear metallization paste and the renewed passivation in group 3, the solar cells were processed identically. Here, we chose other T_{set} than for the test structures to hit optimum firing conditions for the solar cells.

Figure 9 shows the $I–V$ parameters of the fabricated busbarless solar cells for front-side illumination extracted from measurements in an industrial cell tester equipped with a GridTouch unit and conducted after cell fabrication (as processed). Solar cells with the reference paste F yield a peak efficiency of $\eta = 20.5\%$, with a pronounced dependency on the firing set temperature, which is due to a limitation of the fill factor FF. TLM measurements reveal that this originates from a high contact series resistivity $\rho_c \approx 10 \, \text{m}\Omega \, \text{cm}^2$ at the rear side for $T_{set} = 850\,°C$, in accordance with results shown in Figure 5. However, a $T_{set} = 870\,°C$ firing process already negatively affects V_{oc}. In contrast to this, implementing the newly found
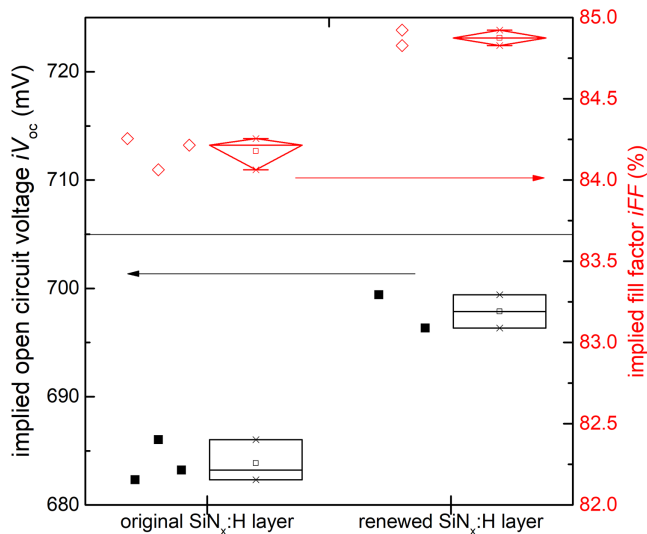
Figure 8. Results of the passivation investigation (iV_{oc} left, iFF right) of solar cell precursors, measured after contact firing, for wafers with the original SiN$_x$:H left in place and for wafers with a renewed SiN$_x$:H passivation layer after phosphosilicate glass etching.

metallization paste C as identified in the test structures, the conversion efficiency is improved strongly up to $\eta = 21.1\%$ at $T_{set} = 830\,°C$. In addition, the firing window is not only considerably wider but also yields strongly improved performance at lower firing set temperatures, as shown by the results in Figure 5. Lower firing temperatures in turn match better the optimum firing conditions for the front-side paste, which presumably is already overfired at $T_{set} = 870\,°C$.

In addition, the results clearly show the advantage in iV_{oc} and iFF, as shown earlier by implementing a renewed SiN$_x$:H passivation layer. This approach translates into a 4 mV higher V_{oc} and a 0.8% higher pseudo-fill factor pFF and thus also higher FF. The small increase in the series resistance R_s most probably originates from an etching of the emitter during the prolonged PSG etch for removal of the rear SiN$_x$:H layer. Please note that no further optimization of the rear SiN$_x$:H layers has been conducted yet, so an adaption of the initial rear SiN$_x$:H layer might even render the removal step unnecessary, as discussed earlier. Also, by increasing the hydrogen content, the second-deposited SiN$_x$:H layer should have a positive impact on the passivation quality for the renewed passivation, as shown in Figure 8. Although the fabricated solar cells feature a rear grid with 208 fingers, R_s is still rather high with $0.55-0.6\,\Omega\,cm^2$. The results strongly hint toward the rather high contact resistivity ρ_c at the rear side as the reason for this, compared with PERC solar cells, which typically feature a series resistance below $0.5\,\Omega\,cm^2$. Overall, the outlined optimizations earlier result in a total area cell efficiency of 21.2%. It is noteworthy that for identical T_{set} and considering only maximum values, the renewed SiN$_x$:H layer leads to a conversion efficiency increase of 0.2% absolute.

For our cells, we find a J_{sc} of $39.5-39.6\,mA\,cm^{-2}$, which is somewhat short of the typically seen $\approx 40\,mA\,cm^{-2}$ for our PERC solar cells[37] and which we expect to be a result of free carrier absorbance at the highly doped polysilicon layer at the rear side with a thickness of $d = 240\,nm$ in our case. Taking into account the vast development in metallization pastes for TOPCon layers, a further developed Ag paste should allow for reducing the thickness d while maintaining low ρ_c and $j_{0,met}$ and lead to a higher J_{sc}.
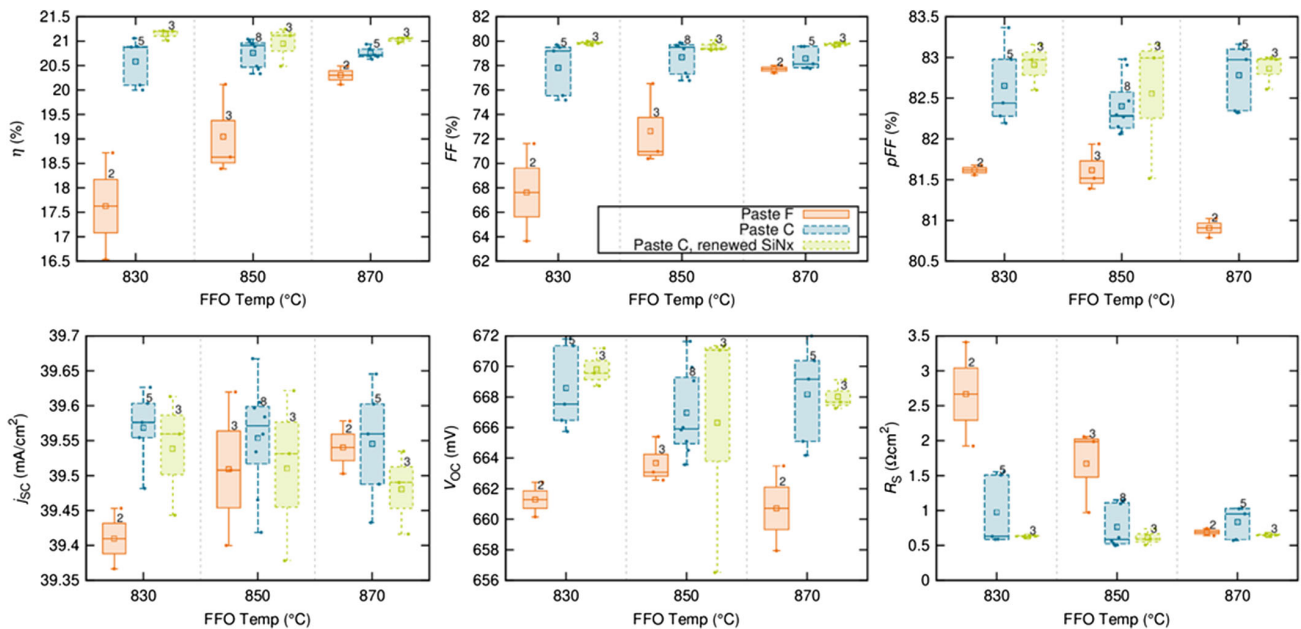

Figure 9. Results of the $I-V$ measurements in an industrial cell tester measured after processing for three different process groups plotted versus the firing set temperature. The cell tester is equipped with a GridTouch unit for measurements of the busbarless solar cells. The cell area is 244.3 cm^2.

4. Challenges

In our study, we investigated a possible replacement of the AlO_x passivation layer on the rear side of PERC devices by a p^+ polysilicon layer in a passivated contact solar cell. We found several challenges that made this task more difficult than expected. These challenges were namely: 1) strong dependence of the passivation quality of polysilicon layers on the rear morphology[23] and thus a complex process sequence, 2) hydrogen loss of passivation layers during processing, which requires additional hydrogen treatment, 3) limited boron dopant concentration within the polysilicon layer, 4) not optimized metallization pastes for this application and thus the need for rather thick polysilicon layers, which lead to strong free carrier absorbance and thus reduced J_{sc}, 5) a rather low throughput of polydeposition, compared with today's needs, as well as 6) not ideal hardware setup to allow for a homogeneous deposition over full loads of 1200 wafers.

Some of these challenges could most probably be addressed by additional effort. In an alternative application, p^+ polysilicon could be used, e.g., also as a rear emitter in n-type cells, or alternative metallization technologies could be used. In a second route, low-temperature metallization pastes could be used for metallization of the rear polylayer, after laser contact opening (LCO) of the rear SiN_x:H layer; however, this would require a very tight alignment of laser processing and screen printing,[38] which would put additional complexity to the process route, possibly with the benefit of reduced $J_{0,met}$. Alternatively, the combination of LCO and Ni/Cu plating has shown also very promising for especially very thin n-doped polysilicon layers[39] and could be tested for this application.

5. Summary and Conclusion

In this work, we have shown that there are large differences in contact formation of screen-printed Ag and Ag/Al pastes when aiming at contacting p^+-doped polysilicon layers. Within a large experiment including 132 groups only for test structures, we identified several commercially available Ag pastes that allow for a rather low ρ_c of $4-5\,m\Omega\,cm^2$ and at the same time only yield low $J_{0,met}$ of $60\,fA\,cm^{-2}$ for typical firing set temperatures as used in solar cells. We have shown that the best overall results have been achieved for a polysilicon layer thickness of 240 nm. Finally, we have applied the most promising metallization pastes on solar cells, to check its compatibility with the solar cell sequence. Putting the p^+ polysilicon layer on the rear of the solar cell and including an improved hydrogenation step by implementation of a sacrificial SiN_x:H layer, we have been able to increase iV_{oc} of solar cell precursors without metallization by 14 mV and solar cell efficiency to 21.2% for this solar cell concept. We further have given insight into the challenges of this solar cell concept and given an outlook into possible routes that might use the presented results.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

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