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Current-voltage and capacitance-voltage characteristics of cadmium-doped p-silicon Schottky diodes

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ABSTRACT

This study reports on a change in current-voltage (*I–V*) and capacitance-voltage (*C–V*) characteristics of silicon (Si) diodes due to doping Si with cadmium (Cd). Effects of Cd-doping on diode parameters and conduction mechanism are investigated. The results obtained here indicate that the diodes are well fabricated and introducing Cd in Si results in a diode *I–V* behaviour changing from normal exponential to ohmic. An ohmic behaviour indicates that the diode conduction mechanism is dominated by defect levels at the centre of the Si energy gap. These defects are responsible for generation of minority carriers to recombine majority carriers resulting in an increase in material resistivity. A change in a direction of a *C–V* trend showing an inversion of a material conductivity-type confirms the generation of minority carriers after doping Si with Cd. A high resistivity material is important for radiation detection since a full space charge region width can be attained at a reasonable operating voltage. The ohmic behaviour and a conductivity-type inversion have been observed on diodes that are resistant to radiation damage. Cd is, therefore, a suitable dopant in defect-engineering studies to improve radiation hardness of Si for high energy physics experiments.

1. Introduction

Using Si-based detectors in high energy physics experiments (HEPE) is of great interest due to the qualities that are possessed by Si. Qualities such as abundance in nature, a reasonable energy gap, a possibility of changing the material properties by doping, a presence of natural oxide, and microscopic structuring [1] make Si a suitable material for fabrication of radiation detectors and other electronic devices. Despite these qualities, detector performance degrades during the operation due to defect levels that are created in the Si energy gap. These levels change the electrical properties of the detectors [2], resulting in instability and unreliability of detectors when used in extreme radiation environments. The detectors cannot meet future demands, like in Large Hadron Collider experiments, where they would be expected to operate in environments harsher than the current ones [3].

To improve the efficiency of Si detectors operating in extreme radiation environments, defect-engineering of Si has been a promising method [4]. The method involves a deliberate introduction of defects in a controllable manner such that the desired properties are improved while the unfavourable ones are minimized or suppressed. Gold (Au) and platinum (Pt) are promising dopants to improve the properties of Si for the fabrication of an efficient radiation detector [5,6]. However, these metals, Au and Pt, are relatively expensive for studies, and their diffusion mechanisms in Si are not fully understood to associate the induced crystal defects with the formed levels in the energy gap. In addition, doping Si with Au and Pt results in a high leakage current of the detector, limiting the radiation sensitivity of the material-based detector [6]. It is, therefore, important to establish a relatively cheap alternative dopant to improve radiation-hardness of Si. Material resistivity needs to be increased to attain a full space charge region (SCR) width of the detector at a reasonable low voltage.

Cd is a group II element with electronic configuration $\{Kr\}4d^{10}5s^2$ having two valence electrons. Acceptor levels induced by Cd at $E_C - 0.54$ eV and at $E_C - 0.33$ eV in the energy gap are attributed to substitutional Cd in Si [7]. Similar to Au and Pt, Cd is a lifetime killer and it creates recombination centres in Si [8]. It is, therefore, expected that a free charge carrier density will reduce, resulting in an increase in the resistivity of Si after doping with Cd. Shallow donors, in contrast, are attributed to the intrinsic interstitial Cd atoms and oxygen vacancies in Si [9,10]. The donors are expected to increase the resistivity of *p*-Si. A study of the electrical character-

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istics of diodes fabricated on Cd-doped Si, therefore, is of interest to have a clear understating on the properties of Cd in Si.

A defect level of the primary interest induced by Cd in Si is $E_C - 0.54$ eV, which is close to the centre of the Si energy gap. The defect level is induced by Au [6] and Pt [11] in Si and it is responsible for the relaxation behaviour of the material [12]. Diodes fabricated on relaxation material show an ohmic *I–V* behaviour with high resistivity and they have been found resistant to radiation damage [5,6]. According to the best of our knowledge, *I–V* and *C–V* characteristics of the diodes fabricated on Cd-doped Si have not been reported before.

2. Experimental details

2.1. Material preparation

In this study, a *p*-type Si wafer polished on one side was diced into 0.9 cm × 0.9 cm square pieces. The resistivity of the wafer was quoted ranging from 1 to 22 Ω-cm with a thickness of 255 ± 25.0 μm. A standard cleaning procedure using methanol, acetone, trichloroethane, and de-ionized water was used [13] to remove all residue and handling grease. An oxide layer on a surface of the wafer was removed by dipping the pieces into a 40 % hydrofluoric (HF) solution, then blow-dried using nitrogen gas before loading them into a high-vacuum chamber for ion implantation. The pieces mounted on holder marked B17 were implanted with Cd ions at 160 keV using the Varian-Extrion 200−20A2F ion implanter based at iThemba LABS (Gauteng), South Africa, to a fluence of ~3.5×10^{15} ion. cm^{-2}, the highest fluence that could be achieved. The highest fluence and the energy were adopted to ensure that a high defect density is created deep in Si bulk.

2.2. Diode fabrication

Schottky diodes were fabricated on undoped and Cd-doped crystalline *p*-Si. Si pieces were cleaned again using a similar procedure as described in Ref. [13] before being loaded into an evaporation chamber for the formation of Schottky contacts. The contacts were achieved by evaporation and deposition of 20 nm Al through a mask of 0.6 mm diameter holes. An ohmic contact was then realized by evaporation and deposition of 25 nm Au onto the back (unpolished) surface of the pieces. For both contacts the deposition was carried at 10^{-6} mbar and at a rate of 1 Å.s^{-1}. The finished devices, each consists of four diodes on the wafer with one common ohmic contact. The diodes were labelled undoped and Cd-doped Si diodes for those that were fabricated on undoped and Cd-doped crystalline *p*-Si, respectively. An oxide layer of 10−30 Å thick is always available on the surface, even after etching Si wafers with an HF solution [14]. The effects of the layer on diode properties are, therefore, assumed to be common to all the diodes since they were fabricated under the same conditions. A change in diode properties would, therefore, be due to Cd-doping.

2.3. Device characterization

The fabricated Schottky diodes were characterized using *I–V* and *C–V* techniques in a dark environment and at room temperature. Metres for current and capacitance measurements have been made in-house. The metres use the same hardware, and they focus on software to implement the functions. A probe station was connected to the metres, which was read by a LabVIEW program specifically coded for the measurements. A contact between the diode under test and the probe was determined accurately by enlarging the diode under microscope. During the measurements, the device under test was placed in a test fixture for a voltage sweep run. A metallic shield was used to cover the test fixture to isolate the measurement system from outside electromagnetic fields and keeping the probe station in a dark environment at room temperature. The *I–V* measurements were taken over the range of -4 to 4 V to ensure that the tunnelling electrons overcome thermionic emission electrons [2]. At voltages above ± 4 V, the forward current saturates because of series resistance and the reverse current is less dependent on the applied voltage. Throughout the experiments, the time between the measurements was maintained for 1 s to give the diode enough time to stabilize.

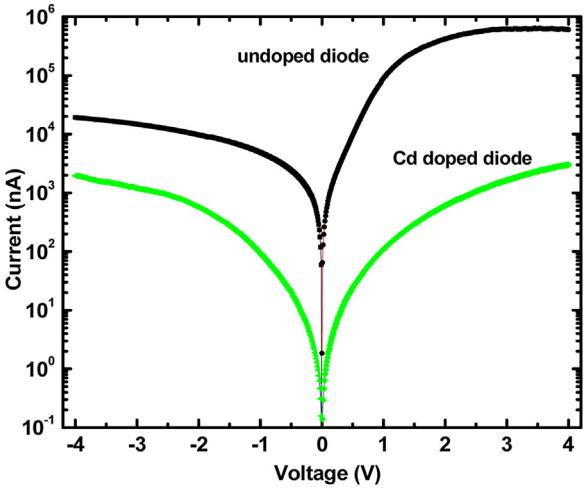

Fig. 1. Forward and reverse bias semi-logarithmic I-V characteristics of the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature.

C–V measurements on the fabricated diodes were taken over the range of 0 to -4 V at 5 kHz. The measurements were unstable at frequencies higher than 5 kHz and the measured capacitance was very low, close to the limit (pF) for our system. A measurement frequency of 5 kHz is the lowest that could be adopted for our diodes to minimise the effects of metal-semiconductor (*m–s)* interface on the measured capacitance. Thus, charges at the interface cannot follow an a.c signal at the measurement frequencies ≥5 kHz [15] for the fabricated diodes. Based on this measurement setup, it was then safe to assume that the measured capacitance was mainly due to SCR.

3. Results and discussion

3.1. Current-voltage measurements

Semi-logarithmic *I–V* characteristics of the diodes fabricated on undoped and Cd-doped *p*-Si are shown in Fig. 1. Considering a thermionic emission theory, *I–V* characteristics of a diode with series resistance, R_s is given [16] as

$$I = I_s \left[\exp\left(\frac{q(V - IR_s)}{\eta kT} - 1\right)\right] \quad (1)$$

and

$$I_s = AA^*T^2\exp\left(\frac{-q\phi_{IV}}{kT}\right) \quad (2)$$

where I_s is the saturation current, q is the electronic charge, V is the applied voltage, η is the ideality factor, k is the Boltzmann's constant, T is the temperature, A is an active area of the diode (= 2.83 × 10^{-3} cm^2), A^* is the Richardson constant for *p*-Si (= 32 A cm^{-2} K^{-2}) and ϕ_{IV} is the Schottky barrier height. I_s can be determined from the region of the straight-line *y*-intercept of semi-logarithmic *I–V* characteristics in forward bias. η is equal to unity in the ideal diode

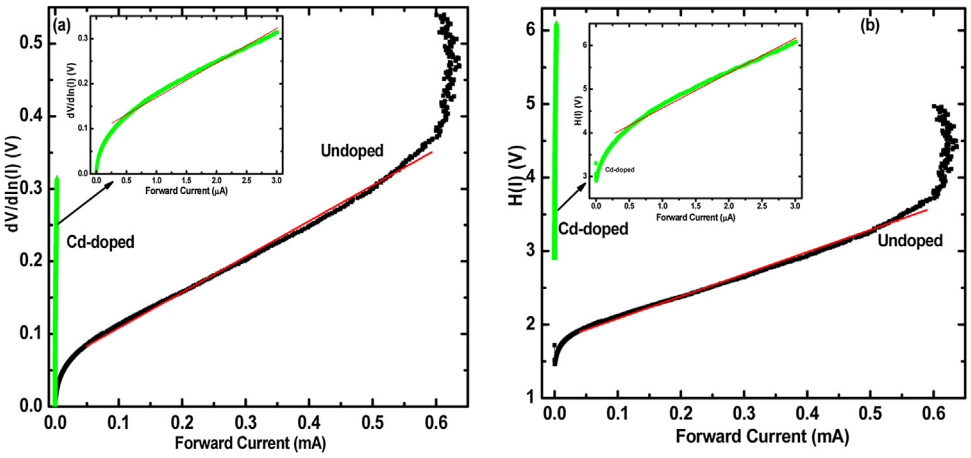

Fig. 2. $\frac{dV}{d(\ln I)}$ versus I (a) and H (I) versus I (b) plots for the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature. Red solid lines define the linear regions used to evaluate the parameters.

Table 1
Parameters for the diodes fabricated on undoped and Cd-doped *p*-Si evaluated using different methods.

	ln *(I)*-*V*			$\frac{dV}{d(\ln I)} - I$		*H (I)* – I		$R_i - V$	
p-Si diode	I_s(nA)	η	ϕ_{IV}	η	R_s (kΩ)	ϕ_{IV}	R_s (k Ω)	R_{sh} (k Ω)	R_s (k Ω)
Undoped	78.96	2.23	0.66	2.42	0.47	0.75	2.85	201	4.15
Cd-doped	0.28	3.34	0.80	3.60	77.29	0.98	806.97	2750	1000

case and it can be obtained from the slope of the linear region of semi-logarithmic *I*–*V* characteristics in forward bias as,

$$\eta = \frac{q}{kT}\frac{dV}{d\ln(I)}. \quad (3)$$

ϕ_{IV} can be calculated by substituting the value of I_s in Eq. 2 as

$$\phi_{IV} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right). \quad (4)$$

A decrease in the diode current for the whole voltage range, shown in Fig. 1, shows that the resistivity of Si increases after doping with Cd. This increase in the resistivity is as a result of defects that are induced by Cd in Si. The induced defects act as recombination/compensation centres to reduce the density of charge carriers in SCR. An increase in the resistivity has been reported on Au- and Pt- doped *p*-Si diodes [17] and on the diodes irradiated with protons [18] and neutrons [19].

As seen in Fig. 1, at high voltages the forward bias semi-logarithmic *I*–*V* characteristics deviate from linearity due to the existence of R_s. The values of R_s for the fabricated diodes can be calculated using Cheung's method [20] as

$$\frac{dV}{d(\ln I)} = \left(\frac{\eta kT}{q}\right) + IR_s \quad (5)$$

$$H(I) = V - \left(\frac{\eta kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (6)$$

and $H(I)$ is given as

$$H(I) = \eta\phi_{IV} + IR_s. \quad (7)$$

Eq. (5) shows that the value of R_s is evaluated from the slope of $\frac{dV}{d(\ln I)}$ versus *I* plot and η can be calculated from *y*-axis intercept. Fig. 2 (a) shows the plots of $\frac{dV}{d(\ln I)}$ versus *I* for the fabricated diodes. Using the value of η determined from Eq. 5, a plot of H*(I)* versus *I* is linear and *y*-axis intercept can be used to calculate ϕ_{IV}. The slope of *H(I)* versus *I* plot can be used for the second determination of R_s. Fig. 2 (b) shows the plots of *H(I)* versus *I* for the fabricated diodes. The parameters evaluated from the linear regions of $\frac{dV}{d(\ln I)}$ versus *I* and H*(I)* versus *I* plots are presented in Table 1. A drastic increase in $\frac{dV}{d(\ln I)}$ and *H(I)* at high current observed in Fig. 2 is unusual and it may be attributed to the existence of high resistivity layer at the *m*–*s* interface.

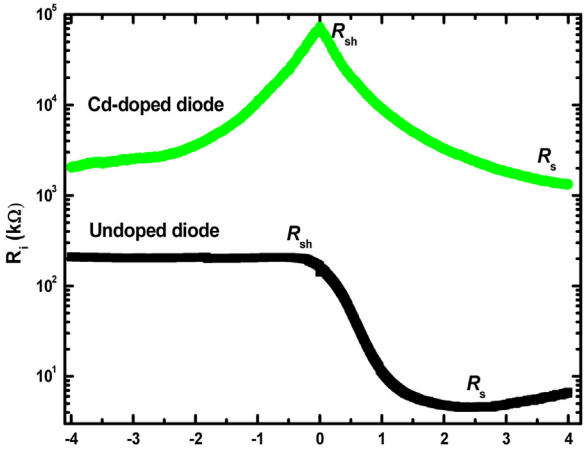

Fig. 3. Junction resistance against voltage plots for the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature.

Fig. 3 shows the plots of junction resistance ($R_i = \partial V/\partial I$) versus voltage for the fabricated diodes. R_i of the undoped diode is independent of the reverse voltage, indicating that SCR extends into the bulk and the material resistivity is constant. A low charge injection rate in SCR after Cd doping is observed by a gentle decrease of R_i with the reverse voltage for Cd-doped diode. An absence saturation of R_i versus voltage plot for the Cd-doped diode in reverse bias indicates that the density of Cd-induced defects decreases with the penetration depth of Cd in the bulk of Si. An onset of the saturation is, however, observed at ~ −2 V to show that the R_i versus voltage plot for Cd-doped diode would not decrease indefinitely. At a certain reverse voltage greater than −4 V, R_i would attain a constant value that would be ~ 201 kΩ. This voltage would be associated with the maximum penetration depth of 170 nm, as estimated

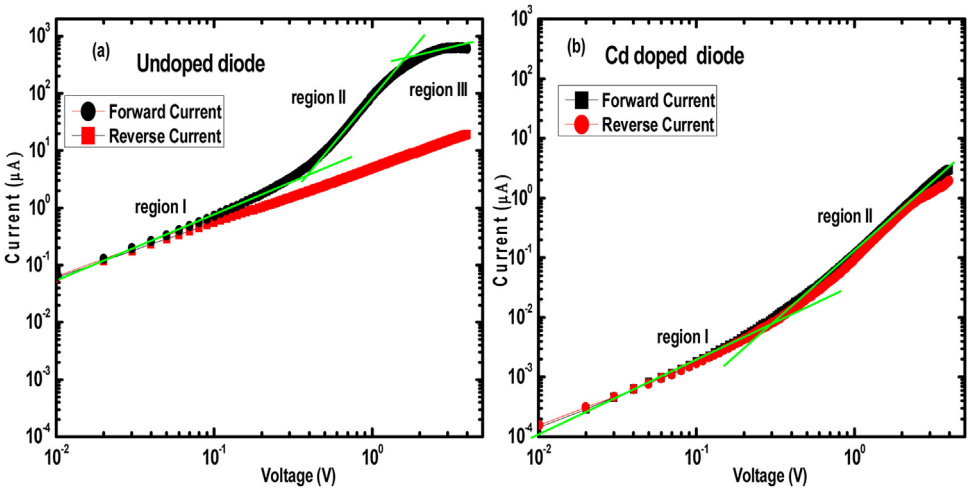

Fig. 4. The double logarithmic I-V plots for the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature. Green solid lines define the different linear regions of the plots.

by the TRIM calculation. A depth profile of the induced defects is, however, not the subject of this work.

R_s and the shunt resistance, R_{sh}, of the fabricated diodes are obtained from the plots of R_i against voltage as presented in Fig. 3. The minimum value of R_i at sufficiently high forward voltage corresponds to R_s while the maximum value in reverse voltage corresponds to R_{sh}. The values of R_s and R_{sh} for the fabricated diodes are presented in Table 1. A low (high) value of R_s (R_{sh}) for the undoped diode evaluated from the plot of R_i versus voltage confirms the good rectification behaviour of the diode [21].

Table 1 shows that the R_s values evaluated using the three methods differ. This discrepancy in R_s is also reported on Au/Pyronin-Y/*p*-Si/Al Schottky diode and it is explained in terms of an increase in the charge injection rate in SCR due to an insulating layer at high voltage region [22]. The difference in values presented in Table 1 thus shows that an insulating layer has been formed at *m–s* interface. The interface layer formed could be SiO_2 because oxygen is always present on the surface of Si, even after chemical treatment of the wafer [14]. Despite these differences, the values of R_s and R_{sh} increased as a result of doping, indicating an increase in the resistivity due to recombination of charge carriers by Cd-induced defects in Si [9].

In Table 1, the value of I_s for undoped diode, 78.96 nA, is higher than 1.23 nA, that obtained for Al/methyl violet/*p*-Si diode [23] and it is lower than 87.1 μA, that obtained on undoped *p*-Si [17]. The I_s value evaluated for undoped diode is within the range of those presented in the literature [17,23], indicating that the diodes were well fabricated using Al for Schottky contacts. Table 1 shows that the value of I_s decreases from 78.96 nA to 0.28 nA after doping with Cd. A decrease in I_s is attributed to a reduction in charge carrier density as a result of Cd-induced defect levels in the Si energy gap. These levels are responsible for recombination/compensation of charge carriers, resulting in an increase in the resistivity of the material after Cd-doping.

The ideality factor values evaluated using ln *(I)*-*V* (2.23) and $\frac{dV}{d(\ln I)}$ -*I* (2.42) methods for undoped diode are similar to each other. The ideality factor, 2.0, close to the one evaluated in this work, was reported based on Al/SnO_2/*p*-Si diodes [24]. The evaluated values of the ideality factor for the undoped diode agree with MIS configuration rather than an ideal diode, confirming the presence of an insulating layer in the diode structure [25]. The ideality factor which is greater than unity implies the deviation from ideal diode and suggesting that the current conduction mechanism is not only due to thermionic emission but also tunnelling mechanism [25,26]. The deviation may be associated to the series resistance, barrier inhomogeneity, and image force effect [25–28]. It can be seen from Table 1 that the values of η for Cd-doped diode are higher than those evaluated for undoped doped, suggesting that there is an additional diode current conduction mechanism after Cd-doping.

The values of Schottky barrier height evaluated using ln *(I)*-*V* (0.66 eV) and H*(I)*-*I* (0.75 eV) methods for undoped diodes are similar to each other. The evaluated values of Schottky barrier height for undoped Si diode (0.66 eV) is close to 0.68 eV, reported on polypyrrole/*p*-Si/Al [29] confirming the existence *m–s* interface layer. It can be seen from Table 1 that the values of barrier height evaluated using different methods for Cd-doped diode are higher than those evaluated for undoped diode. These high values of the barrier height are associated to a decrease in the saturation current in accordance with Eq. 4. As explained, a decrease in the saturation current is as a result of charge carrier recombination/compensation by Cd-induced defects.

As shown in Fig. 4 (a), the double logarithmic *I–V* plot for undoped diode is characterized by three different linear regions (regions I, II and III) indicating different conduction mechanisms [30]. The slopes evaluated from these regions are 1.16, 3.6 and 0.36, respectively. The evaluated slope of the linear region I (0–0.33 V) is close to unity, indicating that the dominant conduction mechanism is ohmic, the current is proportional to the voltage, in this region. An ohmic behaviour is due to the domination of thermally generated current over the injected free carrier generated current though SCR [30,31]. In region II (0.35–1.5 V), the slope is greater than two, representing the trapped charge limited current (TCLC) mechanism with exponent trap distribution [31,32]. The last linear region of the forward logarithmic *I–V* plot for the undoped diode has a slope of 0.36, less than unity, indicating the current is less dependent on voltage, possibly due to the effects of R_S at high voltages.

The double logarithmic *I–V* plot of Cd-doped diode presented in Fig. 4 (b) shows linear regions with slopes, 1.21 and 2.27, for regions I and II, respectively. The slope evaluated in region I (0 – 0.35 V) for the Cd-doped diode is similar to that evaluated for undoped diode in the same region to show that the diode conduction mechanism is not affected by Cd-doping. The current and voltage relationship is ohmic in this region, indicating that the conduction mechanism for both diodes is dominated by thermally generated current over the injected free carrier generated current though SCR [30,31] at low voltages. The slope of region II for Cd-doped is 2.27, lower than the one evaluated for undoped diode for the same region. A decrease in the slope from 3.6 to 2.27, close to 2, at this region indicates a

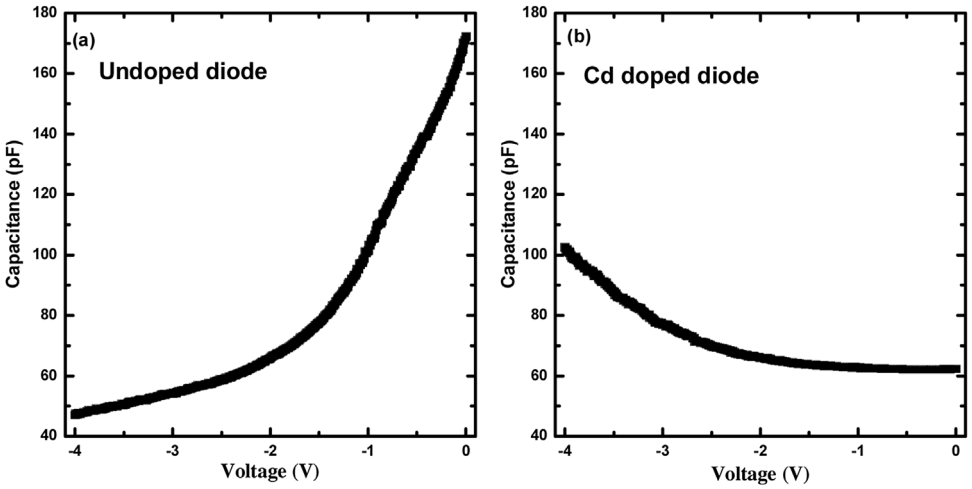

Fig. 5. C-V characteristics of the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature. The measurements were carried out at 5 kHz.

change in the diode conduction mechanism from TCLC to the space charge limited current (SCLC) [32] after doping Si with Cd.

Another observation from Fig. 4 is that the reverse current (generation) and forward current (recombination) are the same, indicating that the diode behaviour, in general, is ohmic after doping Si with Cd. This ohmic behaviour indicates that the charge carrier generation (g) and recombination (r) rates are equal. The rates are equal to show that generation-recombination (g–r) centres dominate the conduction mechanism. g–r centres are defect levels positioned at the centre of the energy gap and they interact equally with both the conduction and the valence bands [6,12]. The Fermi energy of Si is, therefore, pinned at the intrinsic position and it is independent of the incident radiation [33]. The electrical properties of the material-based diodes are stable during radiation detection process [12].

The ohmic I–V behaviour was reported on the diodes that were fabricated on Au- and Pt-doped Si diodes [6,17] and on the diodes that were heavily irradiated by 1 MeV neutrons [2]. The behaviour was explained in terms of defect levels that were induced by the metals and radiation at the centre of the Si energy gap [6,17]. The diodes exhibiting ohmic I–V behaviour were found to be resistant to radiation damage [6]. Thus, in Si, Cd exhibits similar properties as metals and pre-heavy irradiation.

A change in rectifying behaviour of Si diode due to Cd-doping is investigated by the rectification ratio (RR) evaluated for both diodes. RR is a ratio of the forward current to the reverse current at $\pm 4\,V$ and it decreases from 33.74 to 1.55 due to Cd-doping. A decrease in RR is explained in terms of an increase (decrease) in the density of minority (majority) charge carriers [2]. As observed in Fig. 4, the forward and reverse current trends have decreased, indicating that both carrier types decrease with the majority carrier density decreasing with the higher rate after doping with Cd.

3.2. Capacitance-voltage measurements

Fig. 5 (a) shows that the capacitance of undoped diode decreases with an increase in reverse voltage. A decrease in capacitance with voltage is as a result of the withdrawal of charge carriers from SCR. The observed drastic decrease in the capacitance at low reverse voltage indicates that the charge withdrawal rate is high in this region. An absence of the capacitance trend to saturate indicates that a voltage higher than −4 V is needed to attain a full depletion of SCR for the undoped Si diode. A diode with high full depletion voltage (FDV) results in a noise during radiation detection due to a high electric field in SCR [34]. At high FDV the diode operates at breakdown voltage or at the voltage higher, where the efficiency of the detector during operation is impossible [35,36]. A capacitance trend for the undoped Si diode is similar to those that are presented in the literature [37–39] to show that the diodes are well fabricated.

The capacitance trend in Fig. 5 (b) is opposite to that in Fig. 5 (a), indicating that the conductivity-type of material is inverted from p to n after doping with Cd. A conductivity-type inversion was reported on the Si diodes that were irradiated by 800 MeV protons to the fluence of 1.0×10^{14} p.cm^{-2} [40] and on those that were irradiated by 1 MeV neutrons to a fluence of 1.5×10^{13} n.cm^{-2} [41]. This conductivity type-inversion of the material was also reported on the diodes that were fabricated on Pt- doped n-Si diodes [42,43]. According to the best of our knowledge, a material conductivity-type inversion on p-Si is reported for the first time in this work.

Unlike in Fig. 5 (a) where the saturation is not observed, Fig. 5 (b) shows that the capacitance at the range, 0 to −2 V is independent of the reverse voltage. The independence of the capacitance indicates that a full depletion voltage of SCR has been reduced after doping the material with Cd; though it is at the opposite voltage due to a material conductivity-type inversion. A decrease in FDV after Cd-doping is due to a decrease in the doping density [36,44] as shown later in the text. A gentle increase in capacitance at the voltage higher than −2 V in Fig. 5 (b) indicates a low charge carrier injection rate in SCR after doping. The results presented in Fig. 5 indicate that sweeping the voltage from 0 to −4 V results in the charge carrier withdrawal from SCR for undoped diode, while for Cd doped diode the charge carriers are injected in SCR.

The capacitance, C, of a Schottky diode is a function of the doping density, N_D, in the semiconductor material and can be described [35,36] as

$$C^{-2} = 2\left(\frac{V_{bi} + V}{q\varepsilon_s\varepsilon_0 A^2 N_D}\right) \tag{8}$$

where V_{bi} is the built-in voltage, ε_s is the dielectric constant of Si and ε_0 is the dielectric permittivity of vacuum.

C^{-2}-V plots for the fabricated diodes are presented in Fig. 6. Both plots show two linear regions, indicating that a doping density profile is non-uniform [45]. For undoped diode, Fig. 6 (a), the first linear region at low voltage range, 0 - -0.78 V (region I), shows that charge carriers at the interface contribute to the measured capacitance as the SCR begins to move from m–s interface to Si bulk [46]. At the interface, the generation of charge carriers is due to the electric field also to the temperature, making the doping density being higher at this region. The linear region in a high voltage range (region II) of

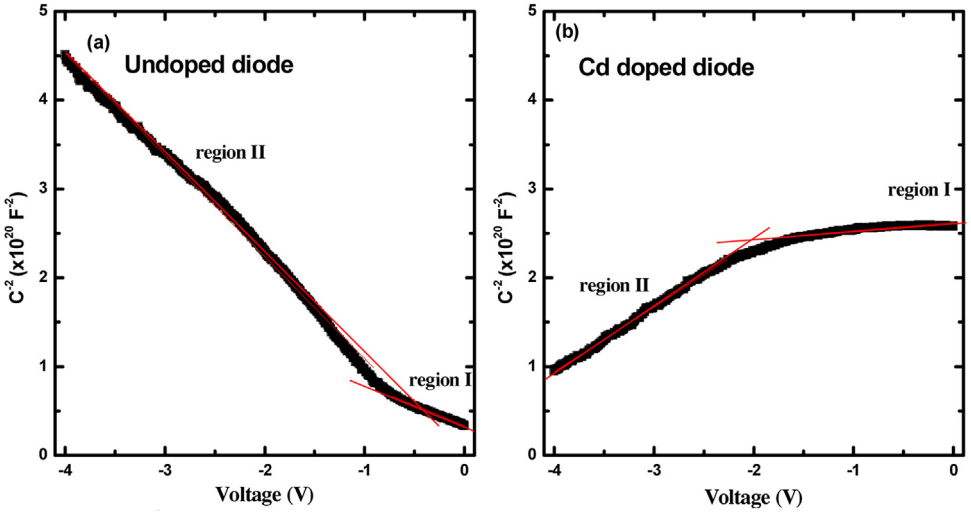

Fig. 6. C^{-2}–V characteristics of the diodes fabricated on undoped and Cd-doped p-Si in the dark and at room temperature. Red solid lines define the different linear regions of the plots.

Table 2
Diode parameters evaluated from C^{-2}-V plots for diodes fabricated on undoped and Cd-doped p-Si diodes. Parameters are evaluated from two linear regions of the plots in Fig.6.

p-Si diode	N_D (10^{16} cm^{-3})		V_{bi} (V)		ϕ_{cv} (eV)		$\Delta\varphi$ (eV)		ξ_{max} (keV/cm)		W_D (10^{-5} cm)	
Region	I	II	I	II	I	II	I	II	I	II	I	II
Undoped	3.28	1.06	0.65	0.50	0.80	0.68	0.03	0.01	101.90	78.40	1.64	2.54
Cd-doped	0.57	0.39	27.50	5.32	27.71	5.45	0.27	0.07	219.60	79.50	250.56	133.49

the C^{-2}-V plot shows a constant doping density for sufficiently high reverse voltage range for undoped diode.

Fig. 6 (b) shows that the first linear region (region I) of C^{-2}-V plot has increased after doping to show that as it penetrates the bulk, Cd induces defects from the surface. These defects recombine charge carriers at the interface resulting in a decrease in the doping density (shown in Table 2). A decrease in doping density as shown by high C^{-2} at a low voltage range indicates that as they are generated by Cd induced defects, minority carriers recombine with majority carriers, resulting in a decrease in charge carrier density in SCR. At a high reverse voltage range, on the other hand, a slope of C^{-2}-V plot in Fig. 6 (b) is opposite from that observed in Fig. 6 (a) confirming that at this region, the diode conduction is dominated by minority carriers after doping.

Linear regions of C^{-2}-V plots observed in Fig. 6 for both diodes were used to extract parameters presented in Table 2. N_D is calculated from a slope of linear regions while V_{bi} is determined from the intercept on the voltage axis of the C^{-2}-V plot. The calculated N_D and V_{bi} are used to determine the Schottky barrier height, ϕ_{cv}, [36,44] as

$$\phi_{cv} = V_d + E_F - \Delta\varphi_b \tag{9}$$

where V_d is the diffusion voltage and is calculated [36,44] as

$$V_d = V_{bi} + \frac{kT}{q}. \tag{10}$$

The Fermi energy, E_F, is given [36,44] as

$$E_F = \frac{kT}{q}\ln\left(\frac{N_v}{N_D}\right) \tag{11}$$

where N_V is the effective density of states in the valence band. $\Delta\varphi_b$ is the image force barrier lowering and is given [36] as

$$\Delta\varphi_b = \left(\frac{q\xi_{max}}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2} \tag{12}$$

where ξ_{max} is the maximum electric field, given [36] as

$$\xi_{max} = \frac{2qV_dN_D}{\varepsilon_s\varepsilon_0}. \tag{13}$$

As seen from Table 2 the values of N_D evaluated from regions I are higher than those evaluated from regions II of Fig. 6 for both diodes possibly due to the contribution of charge carriers at the interface [45]. The values of N_D evaluated from two linear regions for undoped diode, 3.28 × 10^{16} cm^{-3} and 1.06 × 10^{16} cm^{-3}, are close to (1.30–1.38) × 10^{16} cm^{-3} those reported [46,47] for p-Si. The values of N_D evaluated from both regions for Cd-doped diodes are lower than those evaluated for undoped diode indicating that the Cd-induced defects are responsible for recombination of mobile charge carriers, hence a decrease in charge carriers density. A decrease in the carrier density is confirmed by high parasitic resistance (Table 1) evaluated for Cd-doped diode. Thus, both techniques, I–V and C–V, complement each other to show that in Si, Cd is responsible for an increase in the material resistivity. A decrease in doping density (increase in the resistivity) was also reported on Au- and Pt, -doped p-Si diodes [48] and on gamma-irradiated Al/SiO_2/p-Si diode [49]. Thus, the effects of Cd on electrical properties of Si diode are similar to those of Au, Pt and radiation.

The values of ϕ_{cv} evaluated from regions I are higher than those evaluated from regions II for both diodes. The barrier height evaluated from region II was expected to be higher than that evaluated from region I since the doping density evaluated from this region is lower for undoped diode. This discrepancy could be an indication that the barrier height is more of the surface property than bulk. A conjecture of the parameter being more surface property is confirmed by unreasonably high values Schottky barrier height evaluated on the linear regions, especially at region I for Cd-doped p-Si diode. These high values of Schottky barrier height may also indicate that the parameter is meaningless for a diode fabricated on a material rich of defects positioned at the centre of the energy gap.

ϕ_{cv} is always higher than ϕ_{IV} since *C–V* measurements is influenced by the distribution of charge carriers at the depletion region boundary while *I–V* measurements are dominated by the current that flows through the region of low Schottky barrier height [50,51]. The difference between barrier heights obtained from these measurements is also due to surface properties such as interfacial layer, interfacial states, barrier inhomogeneity and the effects of image force barrier lowering [49–52].

4. Conclusion

In this work, Schottky diodes were well fabricated on undoped and Cd-doped *p*-Si. The diodes were characterized using *I–V* and *C–V* techniques to investigate a change in diode properties due to Cd doping. A change in various diode parameters due to the doping was also investigated. Both techniques complement each other indicating that in Si, Cd is responsible for an increase in the resistivity of the material. An increase in the material resistivity is confirmed by an increase in diode parasitic resistance and a decrease in the doping density after Cd-doping. An increase in the resistivity is as a result of recombination of majority carriers by the generated minority carriers. The generation of minority carriers by Cd-induced defects is shown by a drastic decrease in diode forward current and inversion of material conductivity-type after doping.

In general, the results indicated that the diode conduction mechanism was dominated by charge carriers generated in the centre of the Si energy gap as confirmed by diode ohmic *I–V* behaviour after doping. This ohmic behaviour and the material conductivity-type inversion have been reported on the diodes fabricated on Au- and Pt-doped Si diodes and those heavily irradiated by neutrons and have been found resistant to radiation damage. Thus, Cd is also a suitable dopant in defect-engineering studies to improve radiation-hardness of Si for fabrication of detectors to meet the current and future demands.

Author statement

J. O. Bodunrin: student investigator, data analysis, original draft preparation

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Declaration of Competing Interest

The authors report no declarations of interest.

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