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Invited Review

Silicon Solar Cells

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The key attributes for achieving high-efficiency crystalline silicon solar cells are identified and historical developments leading to their realization discussed. Despite the achievement of laboratory cells with performance approaching the theoretical limit, commercial cell designs need to evolve significantly to realize their potential. In particular, the development of cell structures and processes that facilitate entirely activated device volumes in conjunction with well-passivated metal contacts and front and rear surfaces is essential (and yet not overly challenging) to achieve commercial devices of 20% efficiency from solar-grade substrates. The inevitable trend towards thinner substrates will force manufacturers to evolve their designs in this direction or else suffer substantial performance loss. Eventually, a thin-film technology will likely dominate, with thin-film crystalline silicon cells being a serious candidate. Present commercial techniques and processes are in general unsuitable for thin-film fabrication, with even greater importance placed on the achievement of devices with entirely activated volumes (diffusion lengths much greater than device thicknesses), well-passivated metal contacts and surfaces and the important inclusion of light trapping. The recent achievement of 21.5% efficiency on a thin crystalline silicon cell (less than 50 μm thick) adds credibility to the pursuit of crystalline silicon in thin films, with a key attribute of this laboratory cell being its extremely good light trapping that nullifies the long-term criticism of crystalline silicon regarding its poor absorption properties and correspondingly perceived inability to achieve high-performance thin-film devices. For low-cost, low-quality polycrystalline silicon material, the parallel–multijunction cell structure may provide a mechanism for achieving entirely activated cell volumes with the potential to achieve reasonable efficiencies at low cost over the next decade.

INTRODUCTION

The photovoltaic effect was first observed in 1839 by the French physicist Edmund Becquerel when he observed a voltage between the electrodes of his electrochemical cell when illuminated. A similar effect was observed in 1876 by two British scientists W. G. Adams and R. E. Day while working on a solid-state device made of selenium. However, it was not until 1883 that C. E. Fritts realized the potential of the 'photo cell' as a means for converting solar radiation into useful electrical energy.[1] Despite progress over the next 60 years with a range of materials, including copper–cuprous oxide,[2] selenium and thallous sulphide for the active phtovoltaic materials, conversion efficiencies remained less than 1% until the rapid evolution of silicon technology in the 1950s. Since this time, bulk

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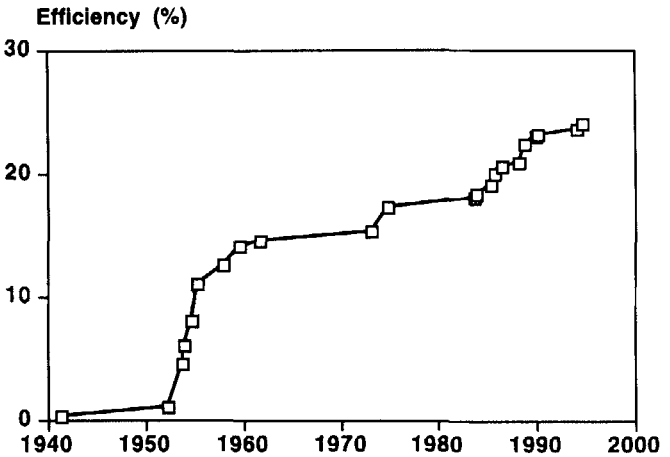

Figure 1. Evolution of silicon solar cell efficiencies

silicon has remained the 'work-horse' for outdoor applications, withstanding challenges by thin-film cells based on cadmium sulphide in the 1970s and on amorphous silicon alloy in the 1980s. Improved cell designs and increasingly streamlined manufacturing, combined with excellent field reliability and stability, ensure an ongoing role for this technology into the future.

HISTORICAL PERSPECTIVE OF SILICON CELL EVOLUTION

Silicon solar cells date back more than 50 years to the early 1940s, predating the beginning of the silicon bipolar device era. Throughout the subsequent decades, clearly identifiable changes in device structures and methods for formation have taken place. Major developments have been contributed to by many research groups and individuals, with corresponding improvements in device performance as shown in Figure 1. During the 1950s, major advances took place in crystal quality and through the development of semiconductor processes and techniques such as solid-state diffusion, which have remained essentially unchanged to this day. During the 1970s, the potential for higher performance came through the development of fine-line metallization capabilities through work at COMSAT. However, it was not until the late 1970s and early 1980s that metal contact passivation and surface passivation were improved sufficiently to enable much of the potential improvement achievable through fine-line capabilities to be realized. The benefits of isolating the high surface recombination velocity associated with the metal/silicon interface from the active regions of the device via a heavily diffused layer appear to have been first realized in the early 1970s. Fortuitously, the p+ region formed beneath the rear metal contact through high-temperature sintering of aluminium acted to suppress localized minority carrier concentrations, thereby reducing the extent of recombination near the metal contact. These benefits appear to have been initially mistaken as being wholly due to gettering enhancements produced by the sintered aluminium. Improved surface passivation appears to have been first successfully incorporated into high-performance cell processing in the early 1980s at The University of New South Wales. However, it was not until the late 1980s that researchers at Stanford University demonstrated improved clean device processing that resulted in high post-processing minority carrier lifetimes and corresponding devices with an entirely active volume. The point contact solar cells developed by this group heralded a new era for photovoltaic devices in which near-unity internal quantum efficiencies for all relevant wavelengths of light could be achieved through a number of different cell structures, each of which have in common the important features of well-passivated front and rear surfaces, minority carrier diffusion lengths substantially greater than device thicknesses and low metal/silicon contact areas with underlying

heavily diffused regions to isolate the high recombination velocity metal/silicon interface from active regions of the device.

Figure 1 shows the performance levels reached throughout the 50-year period of development, with the rate of progress varying quite significantly with changes in design and improved understanding. The following outlines the major changes that have taken place in cell design and structure, with the main features contributing to the improved performance being highlighted and discussed.[3]

First silicon cells, 1940–1950

While studying recrystallized melts of commercial high-purity silicon, Russell Ohl of Bell Laboratories observed well-defined barriers.[4] Fortuitously, these natural junctions resulted from impurity segregation during the recrystallization process. He called the side of the junction becoming positive under illumination 'positive' or 'p-type' and the other 'n-type' (the roles of acceptors and donors were only subsequently clarified). This fortunate choice of nomenclature has simplified calculation of cell voltage polarity for later generations! Ohl made working cells from these natural junctions, as shown in Figure 2, but with efficiencies well below 1%, primarily due to the lack of control over the junction location and the quality of the crystalline silicon material.

Helium ion bombardment junction cells, 1951–1953

Kingsbury and Ohl, in 1952, used helium ion bombardment of the silicon surface to deliberately and more controllably form a junction. A similar contacting scheme was used as for Ohl's earlier devices, but with the achievement of significantly higher conversion efficiencies in the vicinity of 1%. In this case, however, the rear metal contact became positive in polarity, as shown in Figure 3.

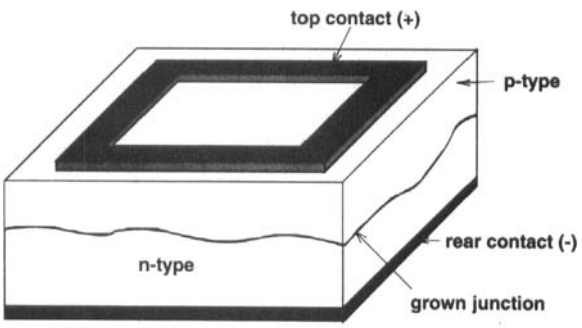

Figure 2. Silicon solar cell reported in 1941 relying on 'grown-in' junctions formed by impurity segregation in recrystallized silicon melts

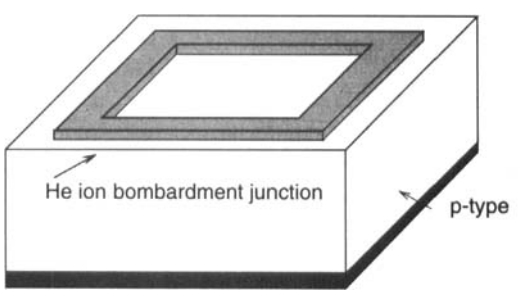

Figure 3. Helium-ion bombarded junction device of 1952

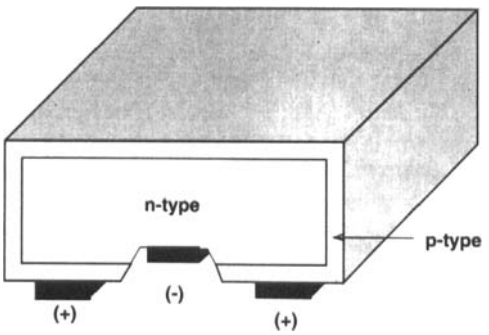

Figure 4. First model silicon cell, reported in 1954, fabricated on single-crystalline silicon wafers with the p-n junction formed by dopant diffusion

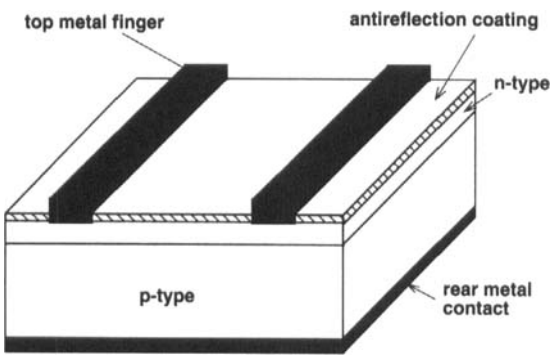

Figure 5. Space silicon cell design developed in the early 1960s which became a standard design for over a decade

Space cell era, 1954–1970

Rapid developments in silicon crystal growth and in the high-temperature diffusion of dopants to form junctions took place in the early 1950s. This led to the achievement of a lithium-diffused single-crystal silicon cell of about 4.5% efficiency by Pearson, Fuller and Chappin of Bell Laboratories in 1954.[5] The lithium diffusion was soon replaced by a boron diffusion, with the efficiency increasing to 6% .[6] These cells opened up the first real prospects for photovoltaic power generation. They used a 'wrap-around' structure as shown in Figure 4, with both metal contacts located on the rear surface. This avoided shading of the top surface, simplified cell interconnection, but led to high resistive losses in the p-type layer across the top surface.

Cell design and performance continued to evolve rapidly throughout the 1950s, with added impetus provided by interest in photovoltaics as a power source by the space industry. By 1960, the cell design had evolved to that shown in Figure 5, with a key feature being the use of a grid metallization contact on the top surface. Due to the importance of cells for space use, cell design evolved to satisfy the corresponding requirements such as maximizing radiation resistance. Key features included the use of high-resistivity, 10-$\Omega \cdot$cm p-type substrates to maximize radiation resistance and the use of a heavily and deeply phosphorus-diffused emitter to prevent junction shunting by the contact metallization. A silicon monoxide antireflection coating was used to minimize reflection from the top surface of the cell. Vacuum evaporation was used to deposit the metal contact through a shadow mask. In principle, the materials and techniques used for device fabrication have changed little since this time.

During the 1960s and early 1970s cell design and performance remained static as space continued to

dominate the interest in photovoltaic devices, with little incentive to make changes to an already space-certified cell design.

Violet cell, 1970–1973

It was realized by the early 1970s that sintered aluminium along the rear improved performance, probably by a combination of gettering and formation of a heavily doped rear interface known as a 'back surface field'. By suppressing minority carriers, this doped region reduces rear recombination, improving cell current and voltage. Additional improvements originated from COMSAT Laboratories through the use of photolithography to produce finer and more closely spaced fingers for the top metallization contact. By reducing pressure upon the sheet resistivity, this removed the need for heavy phosphorus doping along the top surface, eliminating the surface dead layer and improving the response to short wavelengths of light.[7] At the same time improvements were made in the antireflection coating through the use of titanium dioxide. The thickness of these coatings was deliberately selected to be more effective for shorter wavelengths of light than were traditional coatings due to the improved response to the shorter wavelengths. This gave the cells their characteristic violet appearance and hence their title.

For the first time, the performance of the cells was to be influenced by the quality of the top surface passivation, with the transparent emitter making both the current generation (particularly for short wavelength light) and voltage dependent upon the recombination taking place at the silicon surface. A schematic of the violet cell is shown in Figure 6.

Black cell, 1974–1983

Not long after the superior performance of the violet cell had been established, a further boost in performance was obtained by texturing the top surface of the cell using anisotropic etching of (100) orientation wafers to expose [111] planes.[8] This led to the formation of upright pyramids on the top surface, as shown in the cell design of Figure 7. These pyramids reduce the reflection from the top surface to the extent that after antireflection coating the cells look like black velvet. The pyramids also act to obliquely couple the light into the silicon material, therefore allowing absorption closer to the junction with a corresponding effective enhancement in the diffusion lengths for the silicon material. The significant improvements associated with the violet cell and the subsequent innovation of texturing led to a substantial increase in terrestrial cell efficiencies during the mid-1970s. In 1976 Rittner and Arndt reported terrestrial cell efficiencies approaching 17%. Following these rapid improvements, cell technology again stagnated for approximately a decade until the mid-1980s.

Metal–insulator–semiconductor (MIS) cells, 1983–1984

Following the development of the violet cell, closely followed by the black cell, little change took place in cell design or performance for approximately a decade. It was commonly accepted that the practical

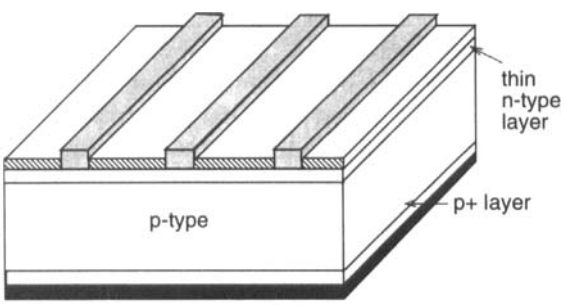

Figure 6. Shallow junction 'violet' cell with closely spaced fine metal lines

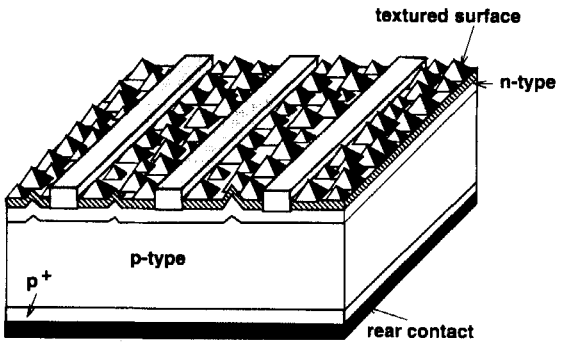

Figure 7. Chemically textured non-reflecting 'black' cell

limit to silicon solar cell efficiency was 20%, leaving relatively little room for improvement over the developments of the early 1970s. During the 1980s, however, surprisingly rapid progress was made with correspondingly large and somewhat unexpected improvements in performance. This was triggered in the early 1980s by a focused effort at reducing recombination throughout the entire cell structure and particularly at the cell surfaces and metal contacts.

An important contributing factor to the rapid developments of the 1980s was an improved understanding of the underlying theory associated with cell operation and the fundamental limits to cell performance.[9] In conjunction, greater knowledge and understanding of phenomena and parameters such as bandgap narrowing, intrinsic carrier concentration, values for diffusivity, Augur coefficients and injection effects were used to advantage.

In 1983, a quite different approach to forming the metal contacts, based on an MIS tunnelling junction, was demonstrated for photovoltaic devices. In these devices, particular attention was paid to the passivation of the top surface through the use of a thin high-quality thermally grown oxide to reduce the surface recombination velocity. Just as importantly, the normally high recombination velocity associated with the metal/silicon interface was avoided by including a very thin oxide between the metal and the silicon, thin enough to facilitate quantum mechanical tunnelling to prevent excessive resistive losses. In these devices, a p-type substrate was used in conjunction with a low-workfunction metal such as magnesium, titanium or aluminium for the top contact grid, which in the presence of the thin oxide induced a thin inversion layer (equivalent to a thin n-type layer) at the top surface of the p-type material. However, the requirement for low metal shading losses necessitated the use of other techniques for electrostatically inducing the surface inversion layer over most of the top surface. Unfortunately, such devices that rely on the presence of positive charge stored in either the oxide or overlying dielectric tend to be somewhat unstable in the long term.

In 1983, the MIS structure was modified slightly to include a lightly diffused n-type layer at the top surface to remove the stability problems. The resulting MINP structure of Figure 8 was the first silicon cell to demonstrate 18% efficiency.[10] Perhaps the most impressive aspect of these new cells was the substantial increase achieved in the open-circuit voltage by paying careful attention to minimizing recombination at the top surface and in the bulk. The bulk component of the dark saturation current was minimized through the use of heavily doped 0.2 $\Omega \cdot$cm substrates. This had the added advantage of reducing the sensitivity of the cell performance to the rear surface recombination velocity by effectively shifting it to being more than a diffusion length away from the junction. The obvious disadvantage accompanying the reduced minority carrier lifetimes in the bulk was a poorer response to long wavelengths of light and a corresponding reduction in short-circuit current, although this was more than offset by the improved voltage.

To assist in minimizing the contribution of the top surface to the dark saturation current, a double-layer antireflection coating was used to alleviate the need for textured surfaces. Textured surfaces not only

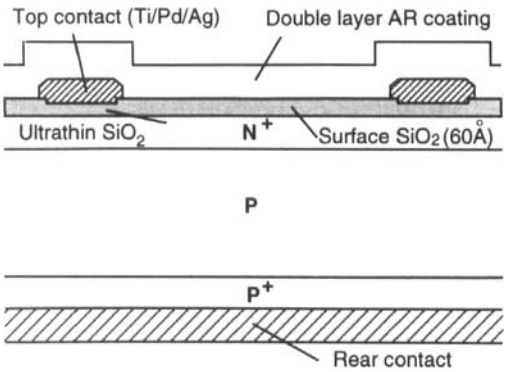

Figure 8. Metal–Insulator–NP junction (MINP) solar cell

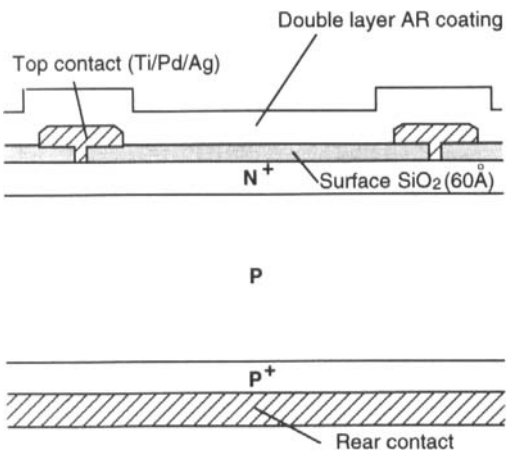

Figure 9. The passivated emitter solar cell (PESC) was the first to reach the milestone of 20% efficiency (1985)

increase the surface area but also rely on the exposure of [111] crystallographic planes, which are more difficult to passivate than the polished surfaces of (100)-oriented silicon.

Despite the achievement of record performance levels, the increased understanding of recombination mechanisms and processes that limit performance facilitated rapid evolution in cell design, with corresponding increases in performance over the coming decade. The achievement of much higher voltages facilitated close examination of the components of the cell design that dominate the generation of the dark saturation current. The MINP structure, although triggering this period of rapid development, dominated cell design for only a short period due to its displacement by a simpler structure.

Passivated emitter solar cell (PESC), 1984–1986

The PESC solar cell structure of Figure 9 achieved the important milestone of 20% efficiency under standard test conditions for non-concentrating solar cells.[11] The substantial performance improvement relative to the MINP cell may suggest significant evolution in cell technology. However, close examination between Figures 9 and 8 reveals that the PESC cells simply represent a minor variation from the MINP cells with the incorporation of texturing and the opening of a fine slot in the oxide underneath the top surface metal to reduce contact resistance. Key features for these cells included the use of conventional metallization (vacuum-evaporated titanium/palladium plus plated silver), a

metal/silicon contact area of only 0.3% at the top surface, an aluminium-alloyed rear contact to form a conventional 'back surface field', a thin high-quality thermally grown oxide to passivate the textured surface, a lightly phosphorus-diffused emitter in conjunction with closely spaced metal fingers (which facilitated near-unity collection probabilities for carriers generated at the top surface, while simultaneously minimizing lateral resistive losses) and the use of a double-layer antireflection coating (ZnS/MgF_2) for low reflection.

The improved top surface allowed advantage to be taken of high-quality FZ silicon. Previous cell designs and technologies could also, of course, be applied to FZ silicon. However, little performance improvement would be noticed, since cell structures were unable to capitalize on the superior FZ properties. Due to the good top surface of the PESC cell and its relatively poor rear, best results were obtained when low-resistivity FZ material was used (0.2 Ω·cm, boron doped), giving high V_{oc} and reasonable J_{sc}. Since corresponding diffusion lengths are only comparable to the normal wafer thickness, the importance of the rear quality is de-emphasized.

An efficiency of 20.1% was measured for a PESC cell by the present National Renewable Energy Laboratory (NREL) in October 1985, with subsequent refinements at UNSW, increasing this to 20.6% in 1986. These results were duplicated at Hitachi with 19.8% independently confirmed (global spectrum) for a nearly identical structure.[12] The Jet Propulsion Laboratory (JPL), with a similar structure but randomly textured, also fabricated cells in 1986 initially reported as 20% efficient,[13] although independently confirmed as 19.3% under current calibrations. More recently, PESC technology has been transferred to Applied Solar Energy Corporation with good results.[14]

Point contact solar cells, 1987–1988

An important breakthrough arose from the Stanford University rear point contact cell of Figure 10. For the first time devices demonstrated fully active volumes (i.e. high collection probabilities for carriers generated throughout the entire device). This not only required post-processing minority carrier diffusion lengths far in excess of the device thickness, but also well-passivated surfaces and metal contacts on both the front and rear. An important contributing factor to the success of this cell was the use of 'cleaner' processing conditions that facilitated the high post-processing bulk minority carrier lifetimes without relying on the gettering contributions of aluminium alloying at high temperature.

Although developed for operation under concentrated sunlight, the point contact cell also performs well when designed for non-concentrating conditions. In 1988, 22.3% aperture area efficiency was demonstrated for an 8.5-cm^2 cell.[15] Subsequently, a larger 37.5-cm^2 cell demonstrated an efficiency

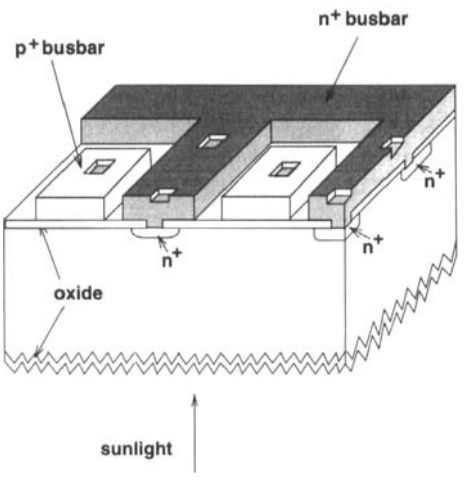

Figure 10. Rear point contact solar cell which demonstrated 22% efficiency in 1988 (cell rear shown uppermost)

converting to 21.6% under current standards.[16] Contacting to small regions of the rear places far more severe demands upon both the bulk silicon quality and surface passivation than previous designs. Photogenerated carriers, most generated within microns of the cell surface, must diffuse to the rear while squeezing into the small contact areas. As a consequence, carrier diffusion lengths must be many times the wafer thickness for carriers to be collected with high probability. Similarly, top surface recombination has to be extremely low. This makes the approach unsuited for space cells where the top surface is quickly degraded by radiation damage. Modifications to the original design were also required to enable cells to withstand high-energy ultraviolet photons in terrestrial sunlight, although most of these would be filtered by lenses, superstrates or laminating materials in typical applications.

The cells used high-resistivity n-type substrates and microelectronic-quality oxide growth for surface passivation. The original cell design required six photolithographic masking layers,[17] with minimum mask features around 5 μm. One possible production difficulty is that the rear oxide has to isolate the rear metal from the substrate over nearly the total cell area. Similarly, the two rear contact metals are spaced only 5 μm apart over an enormous length, inviting shunts. The University of Louvain developed a similar structure in the mid-1980s with slightly lower performance.[18] Reasonable success in reproducing device performance has also been obtained by SERA Solar and Amonix. The SunPower Corporation, involving key members of the Stanford group, has commercialized this technology using a simplified approach with reduced numbers of masking levels.[19]

Passivated emitter and rear locally diffused (PERL) cells, 1989–1993

Capitalizing on the improvements in processing techniques and cleanliness made at Stanford University and aspects of the point contact cell design, the rear contact for the PESC cell was redesigned so as to eliminate the need for aluminium alloy across the entire rear surface. Being better suited to non-concentration applications, the PERL cell of Figure 11 facilitated further substantial improvements in cell performance. A microelectronics quality oxide enshrouded the cell surface. Chlorine-based sequences, both for tube cleaning and during oxide growth, gave improved oxide quality and much higher post-processing lifetimes. With these changes, Al gettering at the cell rear to ensure high post-processing lifetime could be eliminated.

The top surface of the PERL cell resembles that of the earlier PESC device of Figure 9. However, major changes are apparent at the rear. Most of it is passivated by oxide with the p-type contact being made to small regions diffused with boron, similar to the approach for both polarity contacts in the point contact cell. One important difference is that the rear metal is isolated from the cell by an oxide overlying material of only one polarity. Pin-holes, while undesirable, are not disastrous. This rear treatment provides far superior surface passivation than the earlier PESC approach and allows a much wider choice of substrate resistivity. The separation of the rear metal from silicon by an intervening

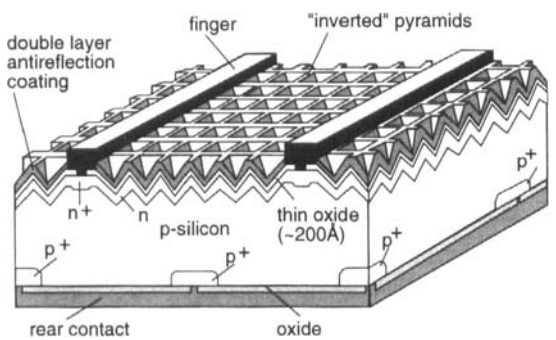

Figure 11. The PERL cell (passivated emitter and rear locally diffused) achieved an efficiency of 24% during 1994

oxide also improves its reflectance.[20] For internal light incident perpendicularly, the rear reflectance is about 95%. This decreases to about 90% as the critical angle for total internal reflection at the Si/SiO_2 interface is approached. Once this angle is exceeded, the internal reflectance steadily approaches 100%. The inverted pyramids along the top surface exploit this improved rear reflectance. For external light, reflection is reduced as for upright pyramids and microgrooves. However, weakly absorbed light is obliquely reflected from the rear. Upon reaching the top surface, light internally striking a pyramid face oppositely orientated to the face which coupled it in is coupled out of the cell. Light striking other faces is totally internally reflected and trapped into the cell. An additional refinement is the use of separate doping levels in contacted and non-contacted areas of the top surface, allowing separate optimization for their conflicting requirements. During the early 1990s, these cells demonstrated efficiencies of 23% constituted by $V_{oc} \sim 700$ mV, J_{sc} of 41 mA cm^{-2} and fill factors around 81%.[21]

Understanding the limiting processes in these PERL cells is far more challenging than in earlier generations of devices. Despite the high open-circuit voltage and efficiency, an injection level-dependent recombination mechanism associated with the rear surface leads to a high ideality factor at the maximum power point and correspondingly degraded fill factors. Equivalently, there is effectively a high rear surface recombination velocity for low bias levels (such as at short-circuit condition), transforming into a low effective recombination velocity for bias levels approaching the open-circuit voltage. Unfortunately, the rear surface is in a state of transition for voltages around the maximum power point leading to the high ideality factors. Explanations for this phenomenon and solutions to the problem are addressed in the context of the rear floating junction cells (PERF cells) in the next section.

Recently, other groups have partially reproduced these PERL cell results. The Fraunhofer Institute, using similar structures but with rear p^+ regions formed by Al alloying, have had efficiencies of up to 22.3% confirmed at the Fraunhofer Institute, Freiburg. Using a similar structure but with random texturing, Sharp has recently reported efficiencies of 22% ('in-house' measurements) using 200-μm thick CZ substrates.[22] The V_{oc} is a modest 627 mV, the fill factor is a creditable 81.5%, but the J_{sc} is enormous at 43 mA cm^{-2}. Given the reduced thickness, the lower grade substrate and the high recombination within the device that led to the low V_{oc}, it would seem unlikely that such a high J_{sc} close to, if not above, the theoretical limit for silicon would be measured under independent testing to present international standards. The estimated J_{sc} under these conditions would be close to 10% lower than that given by 'in-house' measurements. The correspondingly reduced efficiency remains creditable for a CZ substrate.

The above discussion highlights the importance of independent confirmation of high-efficiency cell measurements. Reference cells are, almost inescapably, of lower performance than improved cells. This can produce errors from spectral mismatch between reference and test cells. Independent test centres such as JRC-ISPRA in Europe, the Fraunhofer-ISE and PTB in Germany, ENEA in Italy, JMMII in Japan, RAE in the UK and both NREL and Sandia in the USA[23] have experience in testing a wide variety of cells and are better able to adjust for such mismatch. Standardized techniques are also used for measuring other critical parameters such as cell area.

Passivated emitter and rear floating junction (PERF) cells, 1994 onwards

Two contributing factors to the unusual rear surface behaviour of the PERL cells have been identified, both equating to a saturation in the rear surface recombination current with increasing junction bias. One of these factors is based on electrostatic effects while the other results from unequal electron and hole capture cross-sections at the rear surface. This latter effect has been studied for a number of years by Aberle *et al.*[24] If electrons have a higher capture cross-section than holes at an oxidized p-type rear surface, then for low junction bias, when the minority carrier concentration (electrons) at the rear is low, the recombination rate is determined by the electrons and is therefore relatively high. Characterization of experimental devices indicates that the effective rear surface recombination velocity (RSRV) is very large for these low bias levels, with the recombination only being limited by the supply of electrons to the rear surface.

However, as the junction bias increases, eventually the ratio of electrons to holes at the rear surface will exceed the respective ratio of capture cross-sections, therefore resulting in recombination at the rear surface being limited by the hole concentration and their rate of recombination. For a range of higher bias levels, the hole concentration will remain approximately constant until the electron concentration approaches the same value. The resulting saturation in the rear surface recombination[25] for this range of bias levels causes the ideality factor to exceed unity.

Similar but independent effects to those associated with unequal capture cross-sections can result electrostatically through the presence of positive oxide charge, metal/silicon work function differences and/or boron depletion at the silicon rear surface. These cause the conduction band to bend downwards at the surface. Therefore (even for equal capture cross-sections), the rear surface recombination will still saturate as it shifts from being dominated by the electron concentration to the hole concentration. This is because the hole concentration continues to remain approximately constant with increasing injection level until the electron concentration exceeds the hole concentration by an amount determined by the degree of band bending. A region of high ideality factor therefore again results as the effective RSRV reduces and the recombination current approximately saturates. A more detailed analysis of this effect and its relevance to device performance has been carried out by Robinson *et al.*[26]

The combined contributions of the two described effects effectively cause a reduction in the RSRV from quite high to quite low values as a function of the carrier concentrations (injection level). This region of high ideality factor has impacted on the maximum power point voltages rather than the open-circuit voltages in experimental PERL cells, therefore giving degraded fill factors (and hence efficiency) while still achieving very high open-circuit voltages.

The PERF cells provide an approach to overcoming the coincidence of the region of high ideality factor with the maximum power point by deliberately increasing the band bending at the rear surface so as to shift to lower values the voltage at which the rear surface recombination becomes dominated by the holes. Initially this was accomplished for the PERL cells by deliberately enhancing the electrostatic effects through control of the rear oxide properties in conjunction with the overlying low-workfunction metal (aluminium) and to a lesser extent the boron depletion at the surface. This facilitated the formation of an electrostatically induced n-type layer across the rear surface, corresponding to voltages at the maximum power point with the rear surface transition region having been shifted to lower voltages. These modifications led to improved fill factors up to 82% and V_{oc} values up to 710 mV and the demonstration of 24.0% efficiency (Sandia National Laboratories). The same approach was used with the record thin-film crystalline silicon cell to be discussed in the next section. Figure 12 shows the corresponding dark current/voltage characteristic curve, clearly showing the hump corresponding to the transition region for the rear surface, with voltages above the transition region corresponding to the presence of the electrostatically induced rear n-type floating junction. The more recently adopted approach at The University of New South Wales has been to lightly diffuse n-type dopants into the rear surface to ensure the existence of the rear floating junction for all injection levels. This in turn ensures that the holes determine the recombination rate at the rear surface. Non-optimized test structures based on this approach have demonstrated record open-circuit voltages independently measured in excess of 720 mV. However, complicated two-dimensional effects associated with lateral conduction within the n-type floating layer at the rear can have a serious impact on performance. These effects have been studied and remedies demonstrated.[27]

Summary—key attributes for high-efficiency solar cells

The important attributes for achieving high-efficiency silicon solar cells are as follows:

(i) high aspect ratio metallization with corresponding fine-line capabilities—this allows shading and resistive losses to be minimized while facilitating lightly diffused emitters for good short-wavelength response;
(ii) well-passivated surfaces and metal contacts—minimizes recombination and dark saturation current,

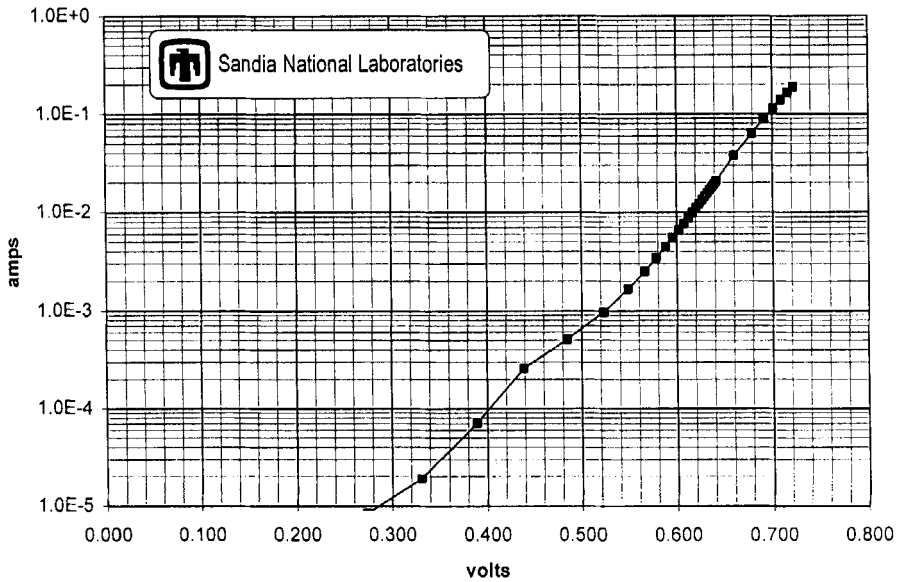

Figure 12. Dark current–voltage curve for a 47-μm thick crystalline silicon cell fabricated using the PERL sequence with an electrostatically induced n-type (inversion) layer across the rear surface. An efficiency of 21.5% was independently confirmed (Sandia, 1995). The knee in the curve corresponds to the injection level at which the rear surface transforms into one with substantially lower recombination velocity

giving higher open-circuit voltages and collection probabilities for carriers generated near the surfaces;

(iii) minority carrier diffusion lengths well in excess of device thickness—this ensures that the device volume is entirely activated, which in conjunction with factor (ii) ensures near-unity internal quantum efficiencies for all relevant wavelengths of light;

(iv) Good optical design, including means for achieving low surface reflection and high internal light trapping.

These key attributes are all found to differing degrees in the highest efficiency PERL cells with electrostatically induced rear floating junctions (PERF cells). Deficiencies include less than optimal antireflection coatings, relatively poor light trapping (compared to theoretically achievable limits), thicker than optimal substrates in the vicinity of 400 μm, surface-limited open-circuit voltages and high recombination around the edges of the device. Many of these deficiencies are actually interrelated. For instance, surface-limited open-circuit voltages lead to the preferential use of thicker substrates (since the dark saturation current contribution from the substrate is relatively small), which in turn reduces the importance of light trapping.

Further improvement in the quality of surface passivation has been demonstrated in test structures by replacing the electrostatically induced rear floating junction with a deliberately phosphorus-diffused rear floating junction in the PERF cell structure. A substantial increase in open-circuit voltage resulted, with over 720 mV being independently confirmed by Sandia National Laboratories under standard test conditions.[27] The corresponding substantial reduction in the effective dark saturation current contribution from the rear surface now forces the cells into a regime in which the bulk component appears to dominate. This offers considerable scope for further improvements through reduced thickness, but must be accompanied by improved light trapping to prevent unacceptable current loss.

The described attributes for high-efficiency cells become far more important for thin-film crystalline silicon solar cells. An interesting result that is relevant to this high-efficiency work was the recent

achievement of 21.5% efficiency[28] with a thin crystalline silicon solar cell of thickness less than 50 μm. Although this thickness is considerably less than optimal for peak device performance, this cell demonstrated vastly improved light trapping over previous devices. Measurements and analysis at Sandia National Laboratories indicated that, on average, light passes 58 times across the wafer before escaping. Not surprisingly, in conjunction with a rear surface reflectance of 98%, a short-circuit current density (almost 38 mA cm^{-2}) approaching the theoretical limit was achieved. As expected, the open-circuit voltage (almost 700 mV) was strongly limited by surface recombination, placing the device in the interesting regime whereby large variations in the bulk minority carrier diffusion length could be tolerated while having virtually no impact on either current generation or open-circuit voltage.

COMMERCIAL CELL PROCESSES

Introduction

Many of the processes, techniques and materials used for the fabrication of high-efficiency laboratory cells are far too complex and costly for consideration by terrestrial cell manufacturers. Rarely are vacuum evaporations, photolithography and masking processes, double-layer anti-reflection coatings, titanium/palladium/silver metallization schemes, the use of polished substrates or solid source diffusion, etc., considered viable. In principle, the key attributes for high-efficiency solar cells listed in the previous section should be feasible for commercially viable implementation. However, at the present immature stage of development for commercial photovoltaic technologies, existing processes and techniques prevent their realization. The remainder of this section outlines processes currently considered viable for commercial production.

Ingot growth

In order to make silicon cells of reasonble performance, large-grained multicrystalline or single-crystal substrates of high purity are required. The main technique for preparing crystalline silicon is the Czochralski (Cz) method. High-purity, fine-grained polysilicon is melted in a quartz crucible. A seed is inserted into the melt and slowly withdrawn. Oxygen from the crucible becomes incorporated as an impurity into the growing crystal. Carbon is also inadvertently introduced from heating elements, with boron usually deliberately added as a p-type dopant. While the oxygen content is closely controlled for microelectronics, solar cells can tolerate lower grade material. Correspondingly, oxygen content is often not specified for wafers to be used in cell fabrication. Similarly, the high-purity polysilicon source material need not be microelectronics quality. Cell manufacturers growing their own ingots often use polysilicon 'off-specification' for microelectronics. Purchased wafers correspondingly are either 'off-specification' or grown with relaxed quality control.

A recent refinement is the use of magnetic confinement during growth (MCz growth). By placing strong magnets around crucibles, melt convection can be controlled improving growth conditions. Magnetic Cz silicon is suited for fabricating very high-efficiency cells, with better control possible over oxygen, carbon and crystal defects. Although equipment costs are higher, faster growth rates are feasible under the improved growth conditions. Another process, float-zone (FZ) growth, also produces crystalline silicon. A rod of fine-grained polycrystalline silicon is recrystallized by passing a molten zone from a seeded end to the opposite end. This produces crystals with much lower oxygen and carbon than the Cz process and of better quality for cell fabrication. Reduced consumables such as crucibles counteract higher equipment costs to some extent. At present the dominance of Cz for the microelectronics industry and the ready availability of second-hand equipment make it difficult for MCz and FZ to compete in large-scale photovoltaic manufacturing.

All of the above techniques were originally developed for microelectronics. More recently, other approaches for producing multicrystalline ingots have been developed specifically for photovoltaics. These are based on slowly solidifying molten silicon in crucibles. Differences between these include: the

way crucibles are loaded, either by solid or molten material; crucible material, commonly graphite, quartz coated with silicon nitride, or silica ceramic; and the way the melt is cooled and growth nucleated, either from the bottom or crucible wall. Compared to crystalline approaches, equipment is simpler and less costly with less stringent requirements upon feedstock. Ingots are larger with a more ideal square cross-section. Disadvantages include poorer material quality within crystals, grain boundaries that generally require special attention during cell fabrication and poorer material uniformity within an ingot and between different ingots.

Shaping and wafering

After their growth, ingots can be cut to more appropriate geometries, e.g. edges sawn off cylindrical ingots or large multicrystalline ingots cut into smaller blocks. Alternatively, cylindrical ingots can be ground to uniform diameter for processing as round wafers. After shaping, ingots are sawn into wafers. Normally, this is by inner-diameter blade sawing, which uses a thin metal blade held rigid under tension. The blade has an internal hole with the perimeter diamond-coated to provide the cutting edge. An alternative, increasingly used in production, is continuous wire cutting. A thin wire is passed over rollers to form a parallel array which simultaneously cuts hundreds of wafers by grinding an abrasive slurry through the ingot. Similar techniques include the multi-blade slurry technique using fixed blades to guide the slurry and the FAST technique, using continuous wire impregnated with diamonds.[29]

Etching and texturing

Frequently, etches based on NaOH are used to remove saw damage, to prepare surfaces for texturing and to texture surfaces to produce square-based pyramids. The damage removal etch is typically 300 g l^{-1} NaOH at 80°C. Additives can improve the surface for subsequent texturing.[30] After rinsing, wafers are texture etched, typically using 20 g l^{-1} NaOH at 90°C. The altered concentration increases etching rate anisotropy, with (111) crystallographic planes being etched relatively slowly. With wafers of (100) surface orientation, this etch exposes (111) equivalent planes which intersect to form the pyramids. An important component of the texturing etch is isopropanol, with other additives able to reduce the dependence on isopropanol thereby removing some of the problems associated with its volatility and giving greater control of pyramid formation and size independently of wafer finish.

For many manufacturers, texturing is one of the more difficult processing steps in cell fabrication. Common production problems include repeatability, pyramid nucleation towards the end of texturing which destroys existing pyramids, lack of control over pyramid size, etching of pyramid peaks through excessive propanol concentration or solution turbulence, the presence of untextured regions between pyramid bases because of low pyramid nucleation density and reflective pyramid bases where adjacent (111) planes intersect. Correct isopropanol concentrations and evaporation rates, solution surface area to volume ratio, temperature, NaOH concentration, length of texturing and solution turbulence can solve these problems.[30] Poor texturing quality from inferior parameter combinations may be partially compensated by modifying the wafer surface finish resulting from the prior damage removal etch or through use of appropriate additives in the texturing solution as partial substitutes for isopropanol. After texturing, wafers are prepared for junction diffusion by rinsing in deionized water.

For multicrystalline wafers, only a small fraction of grains are of the correct orientation for texturing. However, many orientations give tilted pyramids which initially appear to give high reflection for unencapsulated cells but can lead to relatively low reflection after encapsulation due to reflected light striking the glass/air interface outside the escape angle therefore being totally internally reflected back to the solar cell surface.[31] Anisotropic etching also gives different etch rates for different grains, producing steps at grain boundaries. This can complicate the subsequent screening of metal pastes. Often, isotropic etching based on a hydrofluoric/nitric acid solution is used for multicrystalline material to give flat surfaces, with texturing deliberately suppressed.

Diffusion and edge junction isolation

Since wafers used in cell processing are usually boron-doped, an n-type junction is generally diffused into the cell. Phosphorus is the usual n-type diffusant, with various phosphorus sources used commercially. In some cases, the source is phosphine gas passed down the diffusion tube. In other cases, a carrier gas is passed down the tube after bubbling through liquid sources such as $POCl_3$ or PB_3. Alternatively, a solid source such as P_2O_5 is heated at the end of the furnace tube. In all these cases, oxygen is simultaneously passed down the tube with wafers forming phosphorus-doped surface oxides. At the temperatures involved (850°–950°C), phosphorus diffuses from the oxide into the cell. Other techniques include the deposition of phosphorus-doped oxides on cell surfaces from liquid sources by spinning or spraying or screen printing before loading into furnace tubes, the deposition from mists, the use of interleaved solid source wafers of the same size as the processed wafers and the implantation of phosphorus ions. Regardless of source, sufficient phosphorus is introduced to give a sheet resistivity of 30–50 $\Omega\,\square^{-1}$ for screen-printed metallization sequences or closer to 100 $\Omega\,\square^{-1}$ for metallization schemes with fine-line capabilities. The existence of sheet resistives below about 100 $\Omega\,\square^{-1}$ or poor surface passivation will lead to degradation in the cell's response to short wavelengths of light and possible voltage loss. After diffusion, processing can diverge for different manufacturers. In some sequences, the diffusion oxides are removed in HF-based etches, although, more simply, the diffusion oxide can be left and metal contacts fired through it.

Unfortunately, phosphorus not only diffuses into the desired wafer surface but also the side and the opposite surface to some extent. This gives a shunting path between the cell front and rear. Removal of the path around the wafer edge, 'edge junction isolation', is commonly effected by 'coin stacking' the cells. Stacked cells are placed into a plasma etching chamber to remove the exposed edges. No attempt is usually made to remove the rear junction. The firing conditions for the rear contact are chosen to neutralize its effects, often not with complete success. Figure 13 gives a simplified Ebers–Moll equivalent circuit for the case where the rear p-n junction is partially shorted by the resistor R. The value of R is dependent upon a number of factors such as the metal firing conditions and contact area, the type of metal used, the amount of phosphorus and depth of its diffusion on the rear, etc. Ideally, the value of R approaches zero although an even more desirable condition is whether an open circuit at point 'A' gives rise to a rear floating junction (PERF cell) that in many ways acts like a back surface field. The deliberate use of an additional rear junction was discussed in an earlier section on PERF cells.

In the general case of Figure 13, we effectively get two series-connected solar cells with opposing polarities. The rear junction causes greater degradation of the cell output characteristics (more effectively opposes the front junction) when either R is high or I_{L2} is high. The latter occurs with increasing light intensity, although for some technologies the described effect is quite significant even at one-sun light intensities. A comparison between dark I–V measurements and light I–V measurements will usually

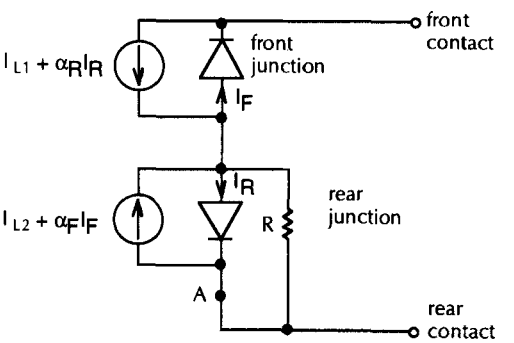

Figure 13. Simplified equivalent circuit for a solar cell with an unwanted rear p-n junction that is partially shorted by a resistance R

identify such effects. For instance, in the dark, with I_{L2} being zero, the rear junction merely manifests itself as a resistance R, in series with the front junction. In the light, however, the ideality factor of the total device artificially appears to be reduced, often to values below unity and in extreme cases becoming negative. A detailed analysis of this effect has been reported by Wenham and Gee.[32]

Some manufacturers use either aluminium metal paste or aluminium-doped silver paste at the rear, with the expectation that the aluminium as a p-type dopant will alloy to the silicon, thereby destroying any n-type layer. Unfortunately, thermal gradient zone melting for the aluminium/silicon molten region in conjunction with a very poor phosphorus solubility in the aluminium/silicon melt[33] often leads to the n-type layer being ineffectively destroyed.

Contact screening and firing

Metal contacts can be screened onto the wafer front and rear using a paste comprising small metal particles, low-melting-point glass composites (frit), organic binders and solvents. For top contacts, the screened paste normally consists of Ag powder. Sometimes phosphorus compounds are added to dope underlying regions more heavily n-type and to improve contact resistance. For rear surface pastes, as previously mentioned, Al is often added to dope underlying regions p-type. Immediately after screening each side, pastes are dried by heating to 350–400°C.

Contacts must be fired at above 700°C to give reasonable metal conductivity, which is still three times worse than pure Ag. The final top contact quality, in terms of contact resistance to silicon, can be very sensitive to firing conditions. Infrared lamps are often used for firing, rather than normal furnace heating elements. Rear contact firing can also be critical to ensure that the rear junction is neutralized. Temperature gradient zone melting can be an important issue when attempting to form 'back surface fields' by alloying of Al paste components.[33] Many pastes for rear contact screening are also predominantly silver, although at least a small percentage of aluminium is often used.

Anti-reflection coating

For textured crystalline cells, surface reflection is low even without antireflection coating. Even in this case, about 4% performance boost after encapsulation can be obtained by antireflection coating at the end of processing. Since multicrystalline cells cannot be readily textured, antireflection coating is essential in present sequences, usually by chemically or spray-deposited TiO_2. Silicon nitride is also sometimes used. Steps are often taken to ensure contact regions are free from this deposited layer for solderability.

Grooving of silicon surfaces

The buried-contact solar cell (BCSC) approach relies on the use of grooves in the surface of the silicon for subsequent location of the metal contact. One key advantage of using grooves in this manner is the corresponding achievement of very high aspect ratios and low metal shading losses for the metallization. Demonstrated methods for groove formation include laser scribing, mechanical scribing using dicing wheels, scratching of the surface using diamond-tipped scribing implements, chemical etching, plasma etching or combinations of the above. Grooving of the top surface can also be used to reduce surface reflection and also to potentially contribute to light-trapping schemes. Laser scribing and mechanical scribing through dicing wheel saws are at present the two most commonly used approaches for groove formation. For larger-scale production, the lower running costs of the laser are important, while for smaller scale production the lower initial capital costs of mechanical scribers make them an attractive option. Surface grooving for reflection reduction has not as yet been implemented commercially, but would probably favour mechanical grooving approaches due to the relative ease for simultaneously scribing many grooves using a 'ganged blade' arrangement such as shown in Figure 14, or specially developed cutting tools embodying the same principle.

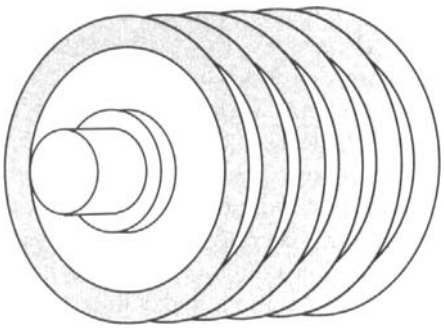

Figure 14. Ganged dicing wheel blades can be used for scribing grooves into the silicon

For metallized grooves, laser scribing appears to have a minor advantage over the use of dicing wheel saws in terms of line width and groove aspect ratio, although little difference in the final performance of cells has been observed.[34] A problem with mechanical scribing approaches is the inability or difficulty in starting and terminating grooves inside the edge of the wafer at high speed. Lasers, on the other hand, can be easily turned on and off at high speed with high precision. A caution with laser scribing concerns possible non-uniformity in groove depth, particulatly if a Q-switched laser is used. Q-Switching allows much higher peak powers to be achieved by deliberately introducing 'loss' into the optical cavity to prevent the lasing action, thereby allowing energy to be stored in the laser crystal through exposure to a bright pumping lamp. After a specified time interval the deliberate 'loss' from the optical cavity is eliminated, therefore facilitating stimulated emission as photons passing up and down the optical cavity trigger radiative recombination as electrons in highly excited states emit photons in phase with those stimulating the emission. A high-energy pulse results, which is coupled to the silicon surface via appropriate optics.

One common problem with laser scribing with Q-switched lasers at high speed is the inability to use a mechanical shutter to give the necessary precision to turn the laser beam on and off. Consequently, electronic means are necessary via the Q-switching arrangement, which can then lead to the laser crystal storing different levels of energy depending on the length of time delay between the end of one cut and the start of the next. Larger levels of energy storage in the laser crystal will lead to the first pulse of the next cut penetrating much more deeply into the silicon, which can cause subsequent problems with regard to chemically removing the damage, diffusing the groove walls and in extreme circumstances shunting through the wafer if the pulse penetrates through to the rear surface. These problems can be easily eliminated by operating the laser on continuous wave between cuts, which simultaneously prevents energy build-up and oblation of the silicon between cuts in unwanted areas.

The majority of commercially manufactured BCSCs at present use high speed Q-switched lasers to economically form the grooves [35]. However, it is unclear as to whether a moving x-y table with multi-beam system or else a system in which the optics are used to shift the beam is more appropriate. Unfortunately, off-the-shelf laser scribers for these purposes are not readily available, with corresponding developmental costs for large scale production expected to be quite substantial.

Electroless metal plating

Numerous metals can be deposited via electroless plating. Commonly used metals for solar cell applications include nickel, copper, tin and silver. A common configuration involves the use of copper as the main conductor due to its excellent conductivity and low cost. However, a flash of silver is commonly used on the top surface to isolate the copper from encapsulants. Also a thin layer of nickel is often used underlying the copper to give good ohmic contact onto the silicon by forming nickel silicide

and simultaneously producing a diffusion barrier to prevent copper penetrating into the junction region. This is a space-certified metallization scheme.

Numerous varieties of electroless plating solutions are available commercially (some acid based, some alkaline based) depending on the requirements. Surfaces must be appropriately prepared and activated to facilitate plating. For nickel plating, the level and type of activation will determine the suitability of the solution to plate to either n-type or p-type or both types of silicon and even dielectrics and plastics if desired. Similarly, the surface of the nickel must be active (no nickel oxide) for copper plating. Most copper plating solutions are autocatalysing, generating their own hydrogen through the plating process that is necessary to keep the plating reaction going. Consequently unless the nickel surface is initially active, the electroless copper plating will not initiate and, similarly, if sufficient area for copper plating does not exist within the plating bath then the reaction will terminate due to insufficient hydrogen generation to maintain the process.

Disposal of waste products from the electroless plating of solar cells is not a serious problem[36] compared to the issues already faced and dealt with by the printed circuit-board industry. The four potential advantages of electroless-plated contacts over screen-printed contacts are lower cost, ease of application, much higher conductivity and much lower temperature processing.

Interconnection and moduling

After testing and sorting, cells are connected into modules. Briefly, by soldering interconnects, cells are assembled into their final layout within the module. The interconnected cells are then placed in a stack consisting of the glass superstrate, a layer of ethylene vinyl acetate (EVA), the interconnected cells, another layer of EVA and then a backing layer, usually Tedlar. Sometimes 'scrim' or spacer layers are interleaved in the stack, which is then laminated together under vacuum at elevated temperature.

Ethylene vinyl acetate was specifically developed for this use during the US Department of Energy's photovoltaic program of the 1970s. Polyvinyl buteral (PVB) had been used in a similar role, but EVA is cheaper and more easily stored. Although standard for many years in modules, recent results show that EVA can discolour after several years in the field, particularly when modules reach high temperatures.[37] Discolouring is associated with the deterioration of ultraviolet absorbers added to the EVA. Although not a major problem unless module temperature is enhanced, such as by reflectors, some performance loss can be expected after several years in the field until improved formulations are developed. The development of new encapsulants has been reported by some companies, including Mobil Solar (now ASE America), although many years of field testing are probably necessary to give confidence in such new products.

Multicrystalline cells

Although commercial processes can be equally well applied to multicrystalline and single-crystal wafers with the minor differences already noted, more complicated sequences can give rewards in terms of increased multicrystalline cell performance. In particular, phosphorus diffusion down grain boundaries and/or hydrogen exposure during processing can neutralize grain boundary activity. High-throughput equipment for hydrogen ion implantation near the end of processing has been described.[38]

Alternatively, the whole processing sequence can be built around hydrogen incorporation. One such sequence involves silicon nitride deposition after the top surface diffusion under conditions encouraging hydrogen incorporation.[39] During subsequent processing, the nitride prevents hydrogen egress.

Manufacturing costs

Recent studies suggest that manufacturing costs for modules lie in the vicinity of US$3.00 (1995 US dollars),[40] assuming an annual production of about 10 MW. Both multicrystalline and single-crystal Cz substrates give similar costs.[41,42]

For crystalline substrates, about half this total cost arises from the wafer cost. Processing of wafers

into cells and encapsulation are roughly equal in cost and account for the remainder. Multicrystalline cells have slightly lower wafer costs but higher costs in other areas, due to lower cell efficiency. Wafer costs, therefore, dominate present module costs, with a large fraction of these arising from the cost of cutting wafers from ingots.

COMMERCIAL CELL TECHNOLOGIES

Introduction

Since the rapid evolution of technology in the 1950s, bulk silicon has remained the 'workhorse' for outdoor applications, withstanding challenges by thin-film cells based on cadmium sulphide in the 1970s and on amorphous silicon alloy in the 1980s. Improved cell designs and increasingly streamlined manufacturing, combined with excellent field reliability and stability, ensure an ongoing role for this technology into the future.

The major emphasis in industry is to produce solar cells of reasonable performance, with a life expectancy in excess of 20 years, at the lowest possible cost per unit of electrical energy generating capability. This necessitates the use of large-area substrates as many of the fabrication costs vary little as a function of substrate area. The trend has therefore been towards ever increasing substrate areas with typical diameters being 2″ in the early 1970s, 3″ in the late 1970s, 4″ during the 1980s and in the 4–6″ range during the early 1990s. Due to the close ties between the integrated circuit (IC) industry and the photovoltaics industry and the use of common substrates, this trend has been largely influenced by the evolution taking place in IC fabrication. However, the ability of a given solar cell to extract current from the contacts without excessive resistive losses has tended to limit the size of substrates suitable for solar cell use.

The large discrepancy between laboratory cell efficiencies and those achievable commercially is somewhat contributed to by the difficulty of achieving high performance with large-area devices. Despite this, a certain performance level must be achieved by commercial cells due to the importance of encapsulation and balance of system costs.[43] The latter is clearly application dependent, making it somewhat difficult to determine an optimal performance/cost trade-off applicable to all manufacturing.

The importance of cost necessitates commercial technology to be simple, capable of high throughput and high yields. However, apart from cost and performance requirements, commercial cells must satisfy environmental and life expectancy criteria. For present commercial technology, single-crystal and

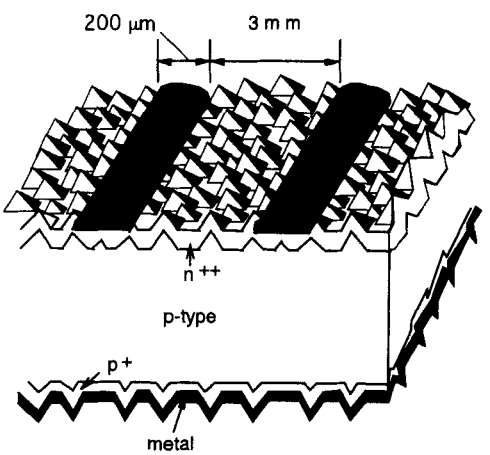

Figure 15. Screen-printed crystalline silicon solar cell, typical of commercially manufactured cells over the last 15 years

multicrystalline silicon substrates are primarily used and have dominated the market for more than a decade in conjunction with the screen-printed solar cell structure of Figure 15. Despite the more recent development of alternative higher performance commercial cell technologies, screen printing is withstanding the challenge to still dominate current manufacturing, largely assisted by the high cost associated with establishing new technology. The equipment for screen printing in most commercial production lines has already been fully depreciated, reducing the incentive to incorporate new technology unless it is able to utilize existing equipment. However, with rapid market growth in photovoltaics, considerable pressure is being exerted by newer technologies which appear capable of reducing costs while simultaneously yielding higher performance.[44]

A further challenge to existing manufacturing has taken place in 1995, with the development of a modified processing sequence for the buried-contact solar cell, that is largely compatible with existing manufacturing equipment for screen-printed solar cells. This new technology will be described following a description of the screen-printed solar cell and corresponding processing sequence. Information will then be provided on another new commercial technology based on the MIS technology. These three technologies comprise virtually all recent bulk device manufacturing, although some interest is being shown in other alternatives for the near future.

Screen-printed solar cells

Figure 15 gives the typical cross-section of a screen-printed solar cell, in which both metal contacts are formed by the screen printing of metal pastes followed by appropriate firing. A typical processing sequence begins with wafer formation (either crystalline or polycrystalline), followed by chemical etching to remove saw damage and if appropriate texturing of the surface. Assuming the use of p-type substrates, a phosphorus diffusion is then effected, forming the p-n junction near the top surface (and often an unwanted p-n junction near the rear surface). In some processes, the antireflection coating is applied prior to metallization. More commonly, however, the rear metal contact is screened and fired, following which a chemical clean of the top surface is used in preparation for the screening and firing of the top metal contact. Edge isolation and antireflection coating complete the processing, after which cell testing, sorting and encapsulation take place.

The screen-printed cell technology was developed by Spectrolab in the late 1970s, at which time the demonstrated efficiencies of around 13% were not far behind the best efficiencies achievable in laboratories. However, since this time laboratory cells have almost doubled in performance, while independent measurements under the global air mass 1.5 spectrum at 25°C indicate that the performance of crystalline silicon screen printed cells still lies in the 13–15% range. Multicrystalline cell performance typically lies in the 10–14% range.

Major differences between the best laboratory cells and screen-printed cells originate from the top contact design. To minimize the sum of top contact losses, metallization should have a high aspect ratio (height divided by width), fine linewidth, high conductivity and low contact resistance to the underlying silicon.[45] Screen printing pays for its simplicity by being poor in all four of the above areas. The normal screening process gives linewidths of about 150 μm (although special screens can do better, these are not suitable for high-throughput production). Upon baking and firing, the screen-printed metallization contracts to about half its original thickness. Typically, the paste is printed to 20 μm thickness, reducing to about 10 μm after firing. The aspect ratio is therefore very poor, only about 0.06. The conductivity of the fired paste is only about one-third that of pure silver, exaggerating the effect of the poor aspect ratio. Additionally, the metallization has a high contact resistance to silicon, arising from the glass frit required for bonding to silicon. Contact resistance depends critically upon both firing conditions and surface doping, although recent improvements in paste formulations and firing conditions have reduced this sensitivity and the magnitude of the contact resistance.

Due to the poor aspect ratios and low conductivity, screen-printed fingers can carry current over only short distances without incurring appreciable resistance losses. An intercorrect strap design has therefore proved popular for screen-printed cells. By having two interconnects running across the cell, the effective

finger length is reduced to below 2.5 cm for a 10-cm square cell. To accommodate differential thermal expansion, these interconnects have to be thin and reasonably wide, typically shading 4–5% of the cell. The contact resistance problem means that the underlying silicon must be heavily doped, even with phosphorus incorporated into the paste, while the coarse linewidth forces screen-printed fingers to be reasonably far apart for low shading loss. This supplements the need for heavy junction diffusion, since carriers have to flow reasonable distances laterally along the top surface.

The performance penalty from the simple screen-printing process is therefore enormous. For the reasons mentioned, top surfaces of screen-printed cells are shaded by about 10% metal, compared to 3% in a 24% efficient cell. Even with this increased shading, resistive losses are much higher. Combined resistive losses in a commercial cell give a further 10% loss compared to 1–2% in the 24% efficient cell. Additionally, the heavy diffusion necessary for tolerable top-diffused layer resistance losses reduces cell blue response, since it creates an inactive surface layer. This further reduces short-circuit current density (J_{sc}) by roughly 10%.

Recent improvements in fine-line capabilities for screen printing at IMEC offer the potential for improved performance screen-printed solar cells .[46] Lines of width in the vicinity of 100 μm now appear feasible although not yet demonstrated in commercial production. The correspondingly reduced spacing between metal fingers facilitates the use of a more lightly diffused emitter and improved short-wavelength response, provided that good surface passivation is included. Screen-printed laboratory cells have now demonstrated efficiencies as high as 16.7%,[46] somewhat narrowing the gap relative to laboratory buried-contact solar cells on similar Cz substrates which have achieved independently confirmed efficiencies in the vicinity of 20%. However, in the commercial environment, the performance difference is almost as large, with 18.8% efficiency having being demonstrated for BCSCs in comparison to 15–16% efficiency for screen-printed cells.[47]

Buried-contact solar cells (BCSC)

These have been reported extensively in the literature,[48] with laboratory efficiencies as high as 21.3% having been independently measured[49] using FZ substrates, while 18.8% efficiency has been achieved in pilot commercial production using Cz substrates.[47] Perhaps less well known are the published data relating to production costs for this technology relative to conventional screen-printed solar cell technology. The conclusion drawn, based on production experience by BP Solar is that new production capacity based on the two technologies would produce cells at the same cost per unit area.[47] This translates to a substantially lower cost in dollars per watt for the BCSC technology due to its significant performance advantage over screen-printed solar cells. Additional advantage is gained from the higher efficiency in terms of balance of system costs, many of which are area related.

Conventional BCSC processing

Wafers are processed initially as in a normal screen-printing operation. After saw damage removal and testuring, the wafer surface is diffused, although more lightly than for screen-printed cells, and the wafer oxidized. The deep grooves apparent in Figure 16 are then formed in the top surface either by laser or mechanical grooving. This is followed by a groove etch and a second, heavy diffusion confined to the grooves by the oxide covering non-grooved areas. Aluminium is then applied to the cell rear, either by screen printing or evaporation, and alloyed. The cells are then plated by electroless nickel, sintered and plated in electroless copper and silver solutions. These metals plate only to the conductive cell aeas, namely grooved areas on the top and entire rear surface. Edge junctions are then isolated by laser scribing of the cell edges, or by normal 'coin-stack' etching which could also have been carried out immediately following the first junction diffusion.

A particularly elegant feature is the way the top surface oxide is used in several different ways both during fabrication and in the final cell. It serves as a shroud protecting against impurity ingress during processing, a diffusion mask, a plating mask, a surface passivation layer and a rudimentary antireflection coating. A sequence has also been developed using silicon nitride in place of the oxide, reducing reflection

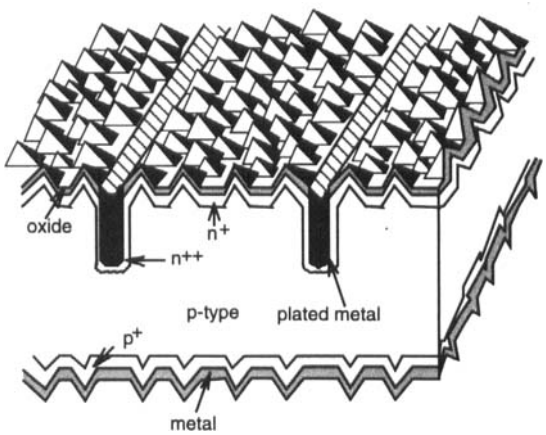

Figure 16. Buried contact solar cell, first commercially available in the early 1990s

in the completed cells.[50] Compared to a screen-printing process, additional steps are laser grooving of the top surface, groove etching and diffusion and contact plating. The top surface screen-printing process is not required and the process eliminates expensive silver pastes.

Simplified BCSC process to suit existing manufacturers

Despite conventional BCSC processing being costed as achieving lower dollars per watt than conventional screen-printed processes, recent developments with the BCSC have adapted and simplified the processes to suit existing infrastructure and equipment of screen-printing manufacturers. The conventional process was originally developed to take full advantage of the high performance capabilities of FZ material, with voltages approaching 700 mV having been demonstrated. However, the simplified new process sacrifices the high voltage capability[51] to give open-circuit voltages that are only marginally higher than achievable with screen-printed processes. This modification is appropriate in view of the voltage limits imposed in commercial production by the lower quality substrates. Consequently, although the following sequence produces substantially lower efficiencies on FZ than the conventional BCSC, relatively little difference results when solar-grade Cz or multicrystalline substrates are used.

Following wafer formation, the simplified process commences with grooving of the top surface, with the subsequent etching–texturing process being used to simultaneously clean the grooves, remove saw damage from the top surface, texture the top surface and form horizontal pyramids on the groove walls. The phosphorus diffusion is effected simultaneously to groove and top surface regions, following which the rear metal contact is screened and fired. The antireflection coating is then applied (such as spray-on TiO_2), following which electroless metal plating of nickel/copper/silver is carried out. The process is completed with edge junction isolation.

The equipment used in this process is essentially unchanged from that used in a typical screen-printing production line, except for the inclusion of the initial grooving equipment. The second screen printer and firing furnace can be eliminated, while the second wet chemistry bath is convected for electroless plating. Table I summarizes the simplified BCSC process juxtaposed to a typical screen-printing process.

Key aspects of the new process include the use of the antireflection coating to mask the top surface with a relatively thick layer, while regions of the grooves receive a much thinner coating, particularly on the underneath faces of horizontal pyramids. This facilitates selective plating to the grooves following an HF treatment to activate the groove surfaces relative to the top surface. The phosphorus diffusion is achieved by depositing phosphorus glass at a sufficiently low temperature to prevent solid-state diffusion occurring prior to forming a thick enough layer for it to act as an infinite phosphorus source in all regions of the surface and grooves irrespective of the geometry. The $80\,\Omega\,\square^{-1}$ resistivity in conjunction with the wall-passivated surface through retention of the diffusion oxide gives a good

Table I. Summary of the simplified buried-contact solar cell process juxtaposed with a typical processing sequence for screen-printed cells

Buried-contact cells	Screen-printed cells
1. Groove formation	1. Texturing
2. Texturing	2. n-Type diffusion
3. n-Type diffusion	3. Screen and fire rear metal
4. Screen and fire rear metal	4. Chemical clean
5. Antireflective coating	5. Screen and fire front metal
6. Electroless Ni/Cu/Ag	6. Antireflective coating
7. Edge junction isolation	7. Edge junction isolation

response to short wavelengths of light without necessitating more closely spaced fingers than the conventional BCSC process. The transparent emitter in the groove wall causes an increase in the dark saturation current contribution from the metal/silicon interface. Whereas the same metallization scheme with a heavy groove diffusion is consistent with achieving voltages of 700 mV, this is reduced to approximately 630 mV in the simplified process described. This is adequate for production with solar-grade substrates.

A number of antireflection coatings can be used in the above process, although the material must be capable of acting as a plating mask to the nickel, copper and silver plating solutions while simultaneously having the right optical properties, such as transmission and refractive index.

Metal–insulator–semiconductor technology

A commercial version of the MIS cell technology described earlier has also been recently demonstrated by the installation of over 300 kW of product in the IMW Toledo photovoltaic demonstration plant.

This sequence involves very few processing steps, although efficiencies demonstrated to date appear to be lower than would be achieved by a good-quality screen-printing process on similar quality substrates and substantially lower than with the buried-contact sequence. The relativities are very well demonstrated by the previously mentioned Toledo installation. Screen-printed multicrystalline cell modules were used as a direct replacement for MIS cells on Cz substrates with very similar performance levels anticipated, suggesting that screen-printed cells on crystalline substrates would give slightly higher performance than these MIS cells. However, buried-contact cells in the same installation demonstrated enormous advantages over either when it came to deploying real product in the field. As opposed to the 11 rows of modules of combined screen-printed/MIS cells required to generate 450 kW in this installation, only seven rows of buried-contact cells were required, with correspondingly large savings in BOS costs.

The sequence used for the MIS cells involves primarily rear aluminium contact evaporation, sintering (with tunnelling oxide simultaneously formed), top aluminium contact evaporation through a metal shadow mask, immersion in caesium solution (to enhance inversion in non-metallized regions of the final device) and low-temperature silicon nitride antireflection coating deposition. Applying this sequence to FZ wafers has resulted in test cells of independently confirmed efficiency up to 15.7%,[52] with only slightly lower efficiencies claimed for large-area devices fabricated on Cz substrates.

The key to further efficiency improvement appears to be to deposit the nitride layer at higher temperature. Unfortunately, this means that the nitride has to be deposited prior to the top MIS tunnel contact, introducing the need for photolithography and pushing costs beyond those commercially viable.

Waferless technologies

Ribbon technologies

Two techniques for producing silicon substrates directly in the form of thin ribbons have been developed to a high level of refinement over the last 20 years: the dendritic web approach and the edge-defined film-fed growth (EFG) method. The comparative strengths and weaknesses of these two approaches have been discussed elsewhere.[53,54] The main advantage is the removal of wafering costs, which becomes quite a significant factor as silicon material costs reduce. The main disadvantage is the relatively low throughput, particularly for the dendritic web approach. The two technologies are presently being championed by Ebara Solar and ASE America, respectively.

Spherical cells

When melted on an appropriate platform, surface tension allows silicon powders to conglomerate into small spheres. During solidification, impurities are swept to the outer shell of the sphere. By crude processes such as grinding, the outer shell can be removed and the process repeated. Crude solution grades can thereby produce relatively pure spherical balls. The balls can be diffused, slotted into an aluminium mesh and processed to convert each into a small cell, connected in parallel with neighbours. Inoperative balls are disconnected during processing. In this way, large cells 10 cm square have been fabricated with efficiencies up to 11%.[55]

Attractions of this approach are that crude grades of silicon can be used and wafering eliminated. Disadvantages include the processing complexity required to make cells and the inherently low efficiency potential. Given the small cell size and consequent handling constraints, it is difficult to imagine 'state-of-the-art' performance being obtained. This difficulty is compounded by relatively low packing densities of the spheres (about 70%), suggesting little room for improvement beyond the 11% efficiency already demonstrated. The material intensiveness of the approach is an additional long-term disadvantage.

Solution growth and thin-film technologies

Inevitably crystalline silicon technologies will evolve or develop to make use of processes that avoid the use of high cost high purity silicon wafers. Numerous thin-film technologies based on crystalline silicon layers are presently being developed and will be discussed in more detail in Section 5. The technology reportedly based on solution growth developed at Astro Power according to recent reports, appears to be nearing commercial production. Instead of using wafer technology, a foreign substrate is used onto which crystalline silicon material is deposited/grown with a fairly thick layer (in excess of 100 microns) presently required to give adequate quality material in the surface regions to achieve reasonable device performance.

Challenge for future commercial cell technologies

The key attributes for high-efficiency solar cells were summarized earlier. Recent developments with commercial technologies have made progress in the areas of fine-line capabilities with high aspect ratios for metallization, surface and metal contact passivation, and optical design to reduce surface reflection. However, no commercially implemented technologies have as yet demonstrated designs characterized by an entirely activated cell volume with corresponding good passivation of all surfaces. The poorer quality of commercial-grade substrates makes this considerably more challenging than for laboratory cell technologies. The double-grooved BCSC of Figure 17 does achieve this goal when implemented with FZ substrates, but not with commercial-grade substrates unless device thicknesses are reduced to below 200 μm.

An alternative approach is to implement a multijunction structure such as shown in Figure 18, whereby active collecting junctions on both the front and rear can assist in providing a fully activated volume even for substrates of present thickness. These transistor-structure solar cells were proposed in the

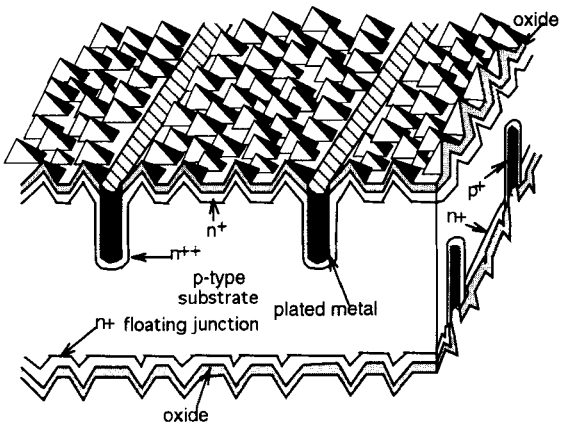

Figure 17. Bifacial buried contact solar cell with grooves in both surfaces

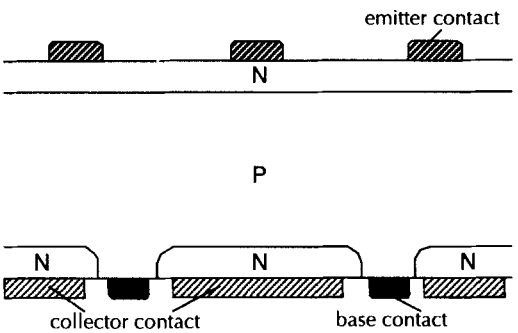

Figure 18. Double-junction solar cell with collecting junctions at both front and rear surfaces to facilitate carrier collection throughout the entire device thickness

mid-1970s,[56] although as yet have never been implemented in large-scale commercial production.

The trend in commercial production is for the thickness of bulk substrates to be reduced to facilitate cost reductions. Wire sawing because of its reduced kerf losses and surface damage to the silicon wafer is contributing to this trend. At present, however, manufacturers seem to be concerned that the reduced thickness will reduce cell performance and yields. Improved processing controls are necessary to avoid the latter, while improved cell design will lead to higher performance rather than lower performance when the thicknesses are reduced to about 150 μm. A device with well-passivated surfaces, 150-μm thickness, reasonable light trapping, low surface reflection and shading can easily achieve 20% efficiency on present commercial substrates. However, the present poor design of most solar cell rear surfaces will lead to loss of performance with device thinning until metal contact designs and rear surface passivation are improved.

Device thinning with uniform-quality material (such as Cz) should facilitate voltages and higher currents. This may not hold for polycrystalline substrates of less uniform quality, since thinning will remove material from the good-quality grains which is 'active', while only removing 'inactive' material from those with short diffusion lengths. These short diffusion length grains tend to limit the performance (particularly voltage) of polycrystalline cells and can prevent voltage increases through thinning.

THIN-FILM CRYSTALLINE SILICON TECHNOLOGIES

Introduction

Recent theoretical and experimental developments have reawakened interest in thin-film cells based on multicrystalline silicon. Initial interest dates to the early 1970s, although poor progress shifted the emphasis to the ribbon and cast ingot approaches. One difficulty is silicon's weak light absorption. This implied that silicon had to be thick to absorb a reasonable fraction of sunlight. Developments in the early 1980s with 'light trapping' have changed this assessment. Theoretically, weakly absorbed light can be trapped for at least 50 passes across the cell, with similar values having been recently demonstrated experimentally through thin laboratory cells using the PERL process. This allows a cell thickness less than 10 μm to be seriously considered. Reducing cell thickness also reduces allowable grain size in multicrystalline material, since this only has to be several times the material thickness for good performance.

Experimentally, good progress has been made with the growth of relatively thin silicon cells on ceramic substrates. Although process details have not been released, it appears that a seeding layer may be deposited onto an expansion-matched ceramic substrate and this layer either recrystallized[57] or a layer grown from solution onto the seeds.[58] An efficiency approaching 15% has been independently confirmed for cells produced with this general approach, although an apparent limitation appears to be the difficulty in achieving adequate material quality adjacent to the ceramic to allow the silicon/ceramic interface to comprise part of the light-trapping scheme.

The highest efficiency thin-film crystalline silicon devices, whose design is potentially compatible with the implementation of light trapping (to confine the light to within regions where all the silicon is active), have been fabricated by Sanyo.[59] In these devices amorphous silicon is deposited onto a metal substrate and subsequently crystallized to give a thickness of 10 μm for the active material. Rather than a p-n junction being formed in the top surface, a heterojunction using another layer of amorphous silicon is used. Even though efficiencies to date are well below the long-term goals, this approach appears to have considerable potential. However, much higher material quality in the crystallized silicon layer will be necessary.

Additional interest in thin films of silicon on foreign substrates also comes from the consumer electronics area. Some active-matrix liquid-crystal television displays currently use thin films of polycrystalline silicon, chemically deposited over large areas, in which to form transistors.[60] Although these films are much thinner than necessary for photovoltaics, only about 0.1 μm thick, this work suggests that technology for depositing silicon of good electronic quality on foreign substrates will significantly advance over the coming decade. A thin-film, high-efficiency silicon technology may well provide the path for evolution of photovoltaics from its current dependence on thick, self-supporting substrates.

Thin-film cell design/technology challenge

Thin-film crystalline silicon solar cells can only achieve high efficiencies if light trapping can be used to give a long optical pathlength, while simultaneously achieving near-unity collection probabilities for all generated carriers. This necessitates a supporting substrate of a foreign material, with refractive index compatible with light-trapping schemes for the silicon. The resulting inability to nucleate growth of crystalline silicon films of good crystallographic quality on such foreign substrates at present prevents the achievement of high-efficiency devices using conventional single-junction solar cell structures. Existing commercial technologies based on the thick substrates in general also use processes incompatible with the achievement of this long-term goal due to poor passivation of surfaces and metal contacts, lack of light trapping, heavily diffused 'dead' layers (particularly the emitter) and the general inability to apply these processes to thin-film device fabrication at low cost. Considerable evolution in techniques, processes and cell design must take place to facilitate the inclusion of the high-efficiency cell attributes listed earlier into a viable crystalline silicon cell technology. Without these attributes it will be nearly impossible to achieve the long-term goal of a 15% efficient module.

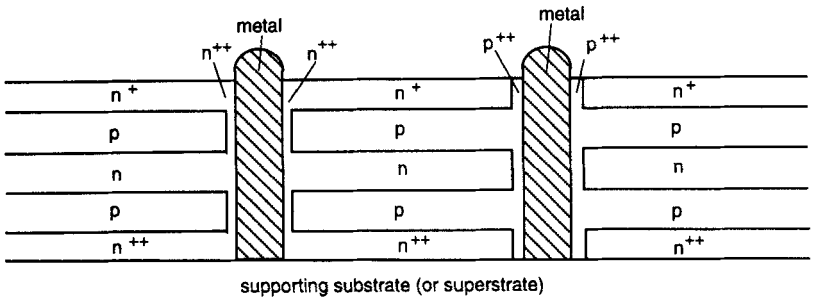

Figure 19. Schematic of a thin-film parallel multijunction solar cell using 'buried contacts' for the metallization to facilitate contacting of the buried layers

The parallel multijunction solar cell appears to provide a new approach for achieving the high efficiency attributes listed earlier, while working with very poor quality material. Near-unity collection probabilities for all generated carriers are achieved through approprate junction spacing and the use of shallow junctions at each surface to isolate the effects of surface recombination. Heavy doping is used to minimize the dark saturation current contribution from the layers, therefore allowing respectable voltages.

Parallel multijunction solar cells

Numerous groups have reported the results of theoretical studies based on the concept of parallel multijunction solar cells.[61–64,68] The general consensus appears to be that the conventional single-junction approach rarely, if ever, offers a performance advantage over the parallel multijunction approach, with the latter having significant advantages in the presence of only moderate levels of light trapping, moderate surface passivation or poor minority carrier diffusion lengths. Figure 19 shows a schematic (not to scale) of the cross-section of a multilayer buried-contact solar cell. The junctions are spaced so as to ensure that carrier collection probabilities approach 100% throughout each layer, irrespective of material quality. The detrimental effects on current generation of high recombination velocities at the front and rear surfaces can be virtually eliminated through the use of very thin surface layers, preferably n-type for easier surface passivation. Lateral resistive losses in the surface layer can in theory also be made negligible, as junction interaction facilitates the injection of majority carriers from the surface layer across the junction and into the underlying layer of opposite polarity where it diffuses as a minority carrier to the next underlying junction for collection.[66] The buried-contact approach appears capable of neatly providing a means for contacting each of the underlying layers of the appropriate polarity.[65] In addition, it retains the usual low-cost, high-efficiency attributes such as low metal shading, simultaneous electroless plating of both polarities of contacts, low metal resistive losses and high voltage capabilities by isolating the metal/silicon interface from the active device regions. Tolerance to grain boundaries has also been reported to be a strength of the multijunction solar cell.[67] Extensive two-dimensional modelling of these structures has been performed by Honsberg *et al.*[66]

Low-quality crystalline silicon layers such as those grown by Sanyo have their diffusion lengths limited primarily by crystal grain sizes and crystallographic quality rather than Auger recombination. Heavy doping of the silicon in the multilayer structure (typically 2–3 orders of magnitude greater than in conventional bulk devices) allows minimization of the dark saturation current while still achieving near-unity internal quantum efficiencies for all wavelengths. In a 10-μm thick device, the heavy doping of the layers in conjunction with the junction interaction through carrier injection provides extremely good lateral conductivity, sufficient to facilitate more widely spaced fingers than even found on screen-printed solar cells.

Junction recombination has been flagged[62,63] as being a key issue in multijunction devices formed

from low-quality material, due to the large depletion region volume. Theoretical studies[68,69] give some insight although experimental results are probably necessary for clarification. As yet there have not been any results published for experimental multijunction devices formed onto foreign substrates. However, encouraging efficiencies approaching 18%[70] have been independently confirmed for multijunction devices formed by chemical vapour deposition onto single-crystal silicon substrates with deliberately degraded minority carrier lifetimes.

Module yields will be a key issue for any thin-film technology in which individual cell testing and sorting is not feasible. The role of bypass diodes takes on increased importance, particularly if able to be included for each device. The inclusion of Zener bypass diodes in multijunction devices appears to be feasible without increased complexity or cost[71] and may have important consequences for module yields, performance (tolerance to cell mismatch/shading) and life expectancy.

CONCLUSIONS

The trend for crystalline silicon solar cells is for wafer thicknesses to decrease for both economic and performance reasons. Most current cell technologies are incapable of producing devices with well-passivated front and rear surfaces, therefore leading to the inevitable consequence that device performance will fall as device thicknesses are reduced.

Twenty per cent efficiency for a commercial process using solar-grade Cz substrates of 150 μm thickness should be feasible in the near future. To achieve this, a device design ensuring an entirely activated bulk volume is essential which, in particular, necessitates improved rear contact design for most technologies. Moderate levels of light trapping will also be necessary. However, improved passivation of the rear surface can easily be accompanied by high rear surface reflection, which in conjunction with front surface texturing will automatically provide adequate levels of light trapping. The technologies that achieve this 20% milestone in commercial production will be those with fine-line metallization capabilities and simple methods for passivating the metal/silicon contacts and cell surfaces.

With the push to reduce cell costs, a thin-film technology will likely eventually dominate commercial production. Thin-film crystalline silicon cells are a potential candidate for this long-term dominance with distinct advantages over alternative materials based on the wide acceptance of crystalline silicon, related technologies with the IC industry, proven reliability and stability, material availability and low cost, environmental friendliness and the apparent ability to achieve high performance. The recent demonstration of 21.5% efficiency for a thin crystalline silicon solar cell of thickness less than 50 μm, although not using practical processes, demonstrated the ability to achieve high performance through the use of light trapping to overcome silicon's limitation of poor light absorption properties (relative to many other potential candidate materials for thin-film technologies). High efficiencies in a commercially viable thin-film crystalline silicon cell can only be achieved through a design that facilitates near-unity internal quantum efficiencies for all wavelengths of light, which by necessity requires well-passivated surfaces and metal contacts in conjunction with diffusion lengths that are substantially greater than the device dimensions. These qualities can only be achieved through the use of a rear reflector or equivalent to ensure that light does not pass out of the active cell volume into inactive regions or material. Additionally, light returning within the silicon to the front surface must be prevented from escaping through the use of an appropriate light-trapping scheme.

Considerable research worldwide is taking place with thin-film crystalline silicon cells. Despite recent rapid progress, significant improvement in the quality of the layers formed onto foreign substrates is necessary to enable the fabrication of cells with entirely active volumes through which the light passes. A possible alternative approach is to use a parallel multijunction structure to reduce the distances travelled by generated charge carriers before collection. This approach appears to greatly relax the requirements for material quality, while simultaneously appearing to offer the potential for low cost and high performance. A commercial product based on the parallel multijunction cells concept is not expected to be available within 5 years. This provides a window of opportunity for other technologies, including

thinned, very high-performance Cz cells, perhaps even making use of static or even active concentrating systems.

Acknowledgements
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