



## Bi-polysilicon passivating contact technique for crystalline silicon solar cell



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### ABSTRACT

Polysilicon (poly-Si) passivating contacts overcome the direct metal–semiconductor contact drawback of traditional industrial crystalline silicon (c-Si) solar cells by inserting a layer stack of poly-Si and silicon oxide layers at the rear full-area metal/c-Si interface, which is well-known as a tunnel oxide passivating contact (TOPCon). In conventional industrial TOPCon devices, the direct contact problem affects the emitter, which deteriorates the passivation quality and suppresses the open-circuit voltage ( $V_{oc}$ ). We herein introduce an innovative bi-poly-Si technique (Bi-TOPCon) featuring rear full-area passivated poly-Si and emitter locally passivated poly-Si to improve the passivation quality of the TOPCon device. The local emitter poly-Si is introduced using metal mask alignment, and its properties are optimised toward high passivation quality and low contact resistance. The Bi-TOPCon device shows a significant improvement in  $V_{oc}$  ( $V_{oc} > 700$  mV). Bi-TOPCon is a promising technology for high-efficiency, next-generation industrial TOPCon devices.

### 1. Introduction

Crystalline silicon (c-Si) photovoltaics (PVs) are practical resources in the solar energy transition to a low-carbon society. Over the last several decades, crystalline silicon (c-Si) has become an acceptable-cost power source due to manufacturing chain advancements. In 2020, c-Si modules made up 95% of the global PV market, with an installed capacity of over 700 GW [1]. C-Si PVs will likely dominate global power production by 2040–2050 [2–4]. PV technology must progress to fulfil global electricity needs.

In c-Si technology, use of metallic electrodes to extract charge carriers is problematic. Direct metal–semiconductor interaction causes recombination, owing to high defect density at the contacts. The traditional full-area aluminium back-surface field (Al-BSF) technology, which was first introduced in 1972 [5], suffers severely from such direct interactions, limiting its efficiency to approximately 20% [6]. Direct contact's disadvantages may be mitigated in two ways. **First, reduce metal–Si contact area.** The metal electrodes were metallised locally on heavily doped small portions with low contact resistivity while the rest

of the surface was passivated. This approach is utilised in industrial passivated emitters and rear totally diffused (PERT) or rear cell (PERC) designs [7,8]. Laser ablation and/or photolithography opens small regions of the dielectric passivation area at the rear, followed by electrode metallisation. PERT advances are projected to dramatically decrease rear-side recombination and enhance rear reflectivity, resulting in higher open-circuit voltage ( $V_{oc}$ ) and short-circuit current density ( $J_{sc}$ ) than Al-BSF devices [9,10]. Despite breakthroughs with a laboratory-level efficiency of 25% [7], direct contact defects restrict  $V_{oc} \leq 700$  mV [11].

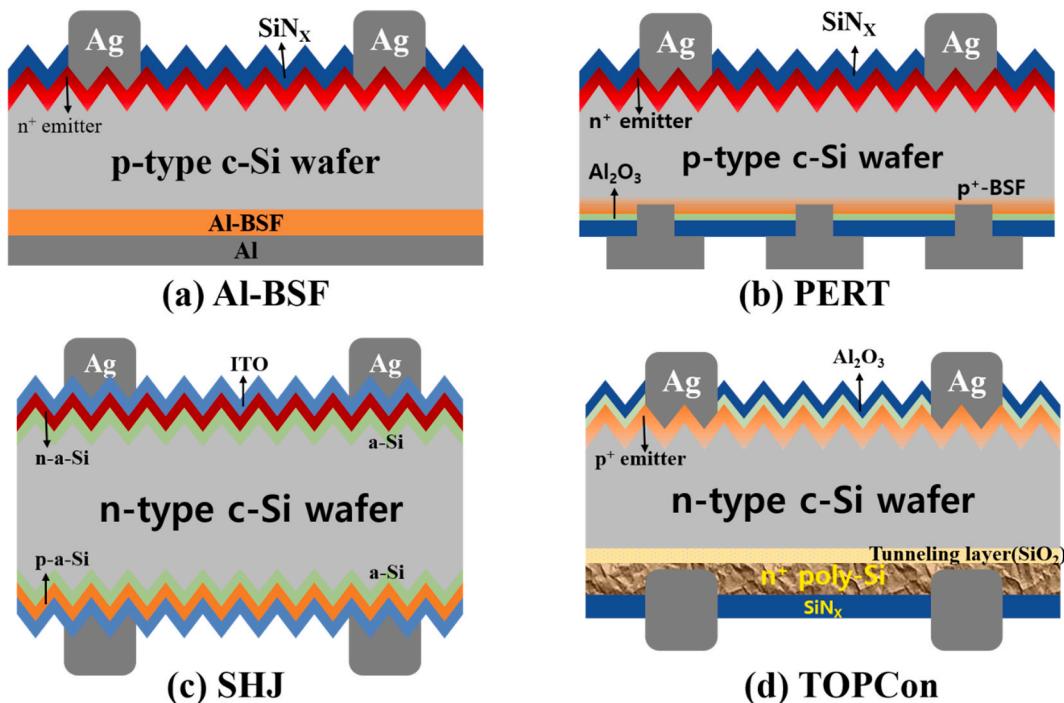
**The second approach separates the metal electrode from the Si wafer using passivating contact layers.** The most common designs are silicon heterojunction solar cells (SHJ) [12–14] and tunnelling oxide passivating contacts (TOPCons) [15,16]. The SHJ designs exhibit  $V_{oc}$  exceeding 745 mV, owing to excellent passivation [11,17]. Fig. 1 depicts Al-BSF, PERT, SHJ, and TOPCon structures in schematic. TOPCon devices outperform SHJ in stability because of their high process temperatures and using poly-Si passivation contact [10,18]. Because of their high absorption coefficients and parasitic absorption losses, TOPCon

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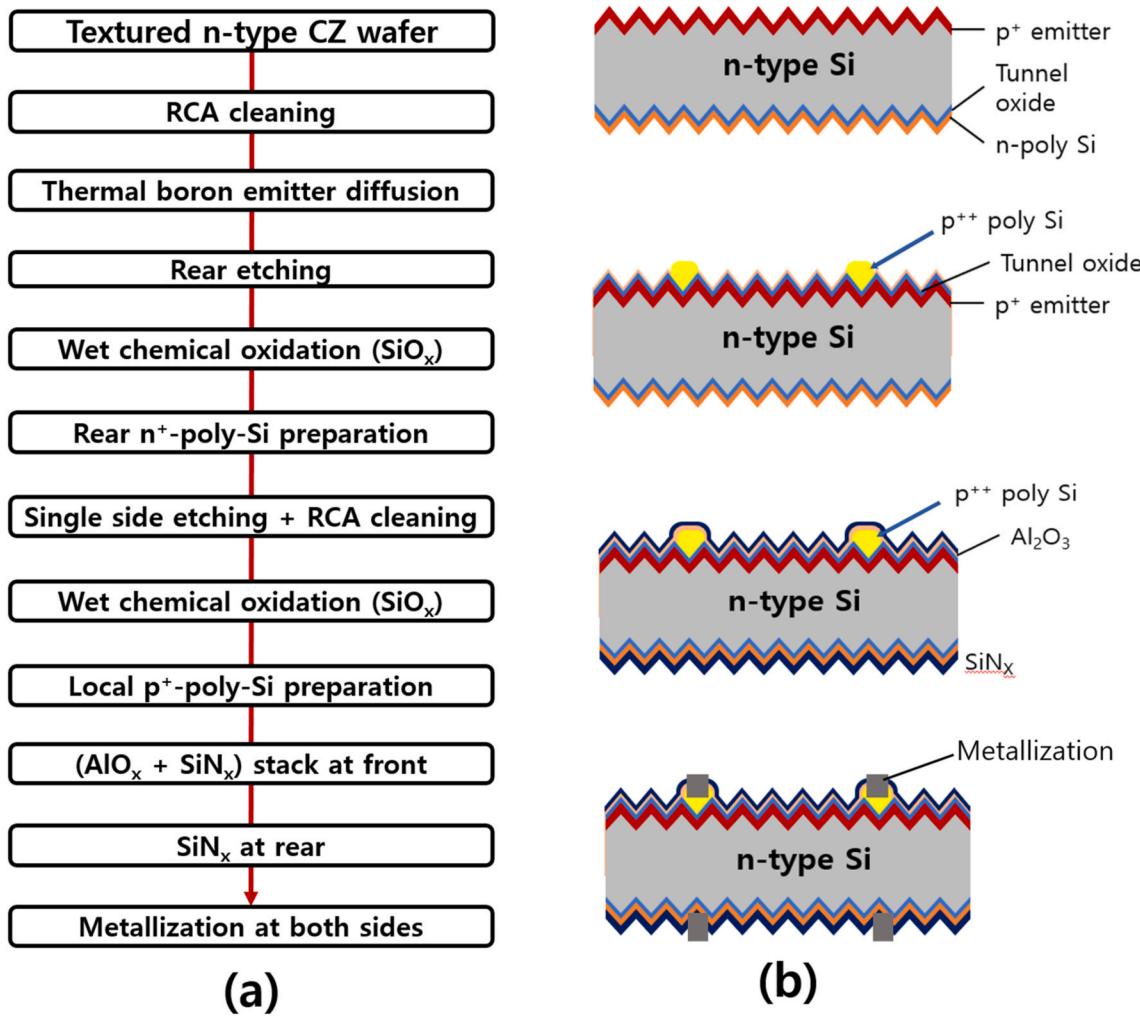
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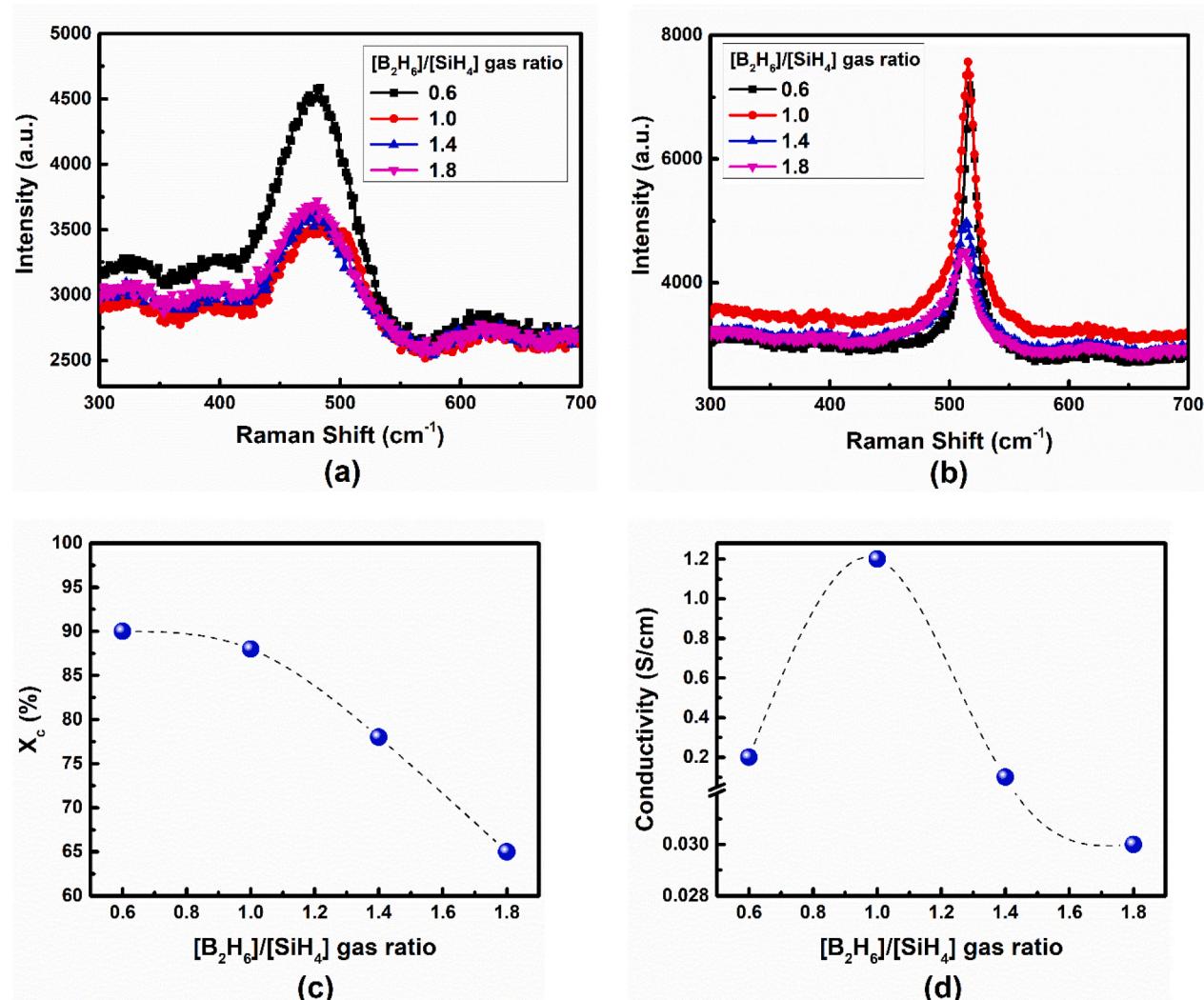
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**Fig. 1.** Typical schematics of common c-Si solar cells including a) aluminium back-surface field (Al-BSF), b) passivated emitter, and rear totally diffused (PERT), c) silicon heterojunction solar cell (SHJ), and d) tunnelling oxide passivating contact (TOPCon).



**Fig. 2.** a) Experimental steps of the TOPCon device manufacturing, and b) schematic structures of some typical steps.



**Fig. 3.** Raman spectra of  $p^+$ -poly-Si as a function of GR (a) before and (b) after annealing process, respectively, and (c) volume crystalline factor, and d) dark conductivity of  $p^+$ -poly-Si as a function of GR.

devices use poly-Si contacts at the rear. An industrial TOPCon device has a boron-diffused junction at the passivated emitter, followed by localised fire-through metallisation [1,10]. This technique risks emitter direct contact, lowering  $V_{oc}$  [19].

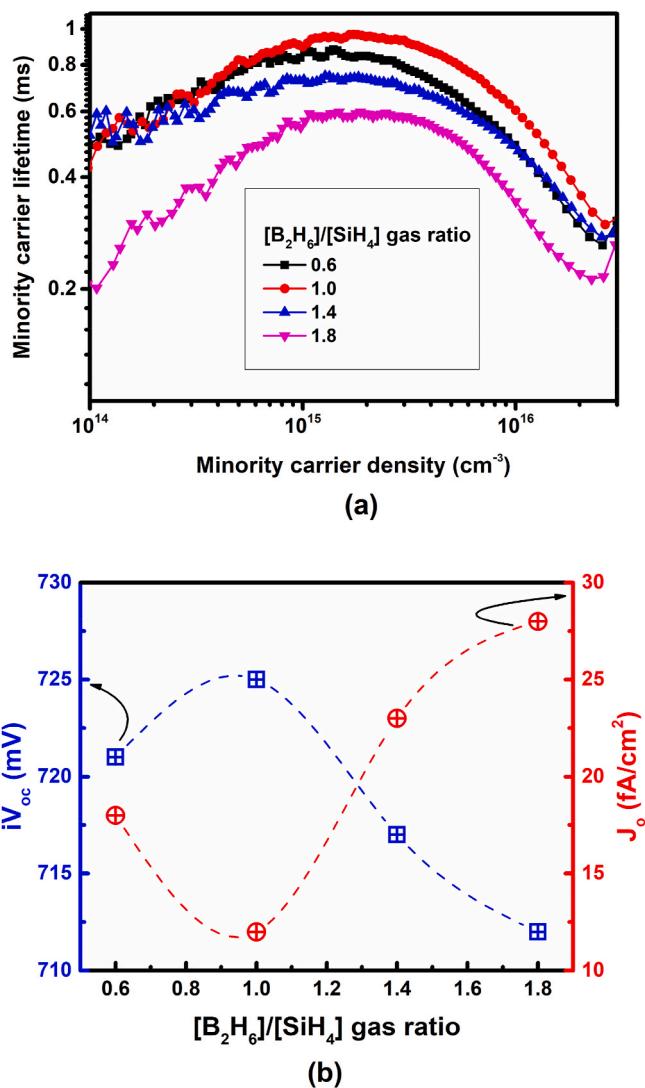
To address the passivation quality risk for industrial TOPCon devices, we develop a bi-poly-Si passivating technique (Bi-TOPCon) with rear full-area passivated poly-Si, and a locally passivated poly-Si emitter. To limit metal–Si contact and ensure great light transmission into the absorber, poly-Si is only below the front metallisation [20–22]. Local poly-Si is prepared using a mask-aligning technique, without photolithography step. The mask and poly-Si are optimised to reduce the parasitic absorption and contact resistance losses. The preliminary results show that locally optimised poly-Si may improve passivation while minimising contact resistance losses.

## 2. Experiment

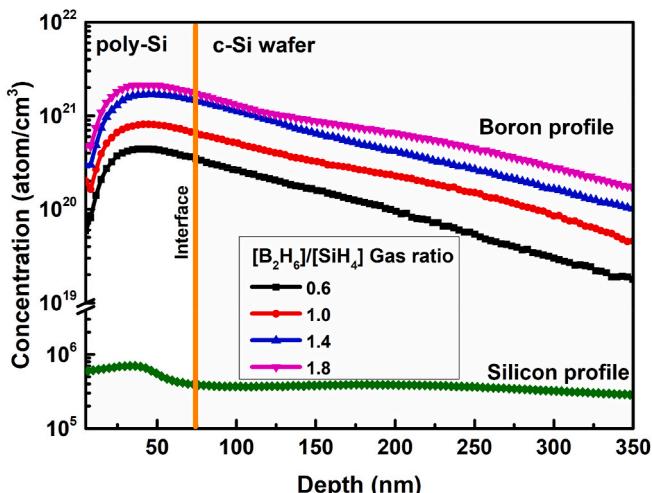
Fig. 2a depicts the experimental steps of the device process, and Fig. 2b depicts the schematic structures of some of the essential steps in the device process. The procedure was performed on n-type Czochralski (CZ) silicon wafers with a thickness of 200  $\mu\text{m}$  and a resistivity of 0.2–1.0  $\Omega \text{ cm}$ . The wafers were subjected to alkaline texturing, followed by the standard Radio Corporation of America wet chemical cleaning

process before thermal boron emitter diffusion ( $\sim 120 \Omega/\square$ ) using a tube furnace in a  $\text{BBr}_3$  gas environment. A single-sided etching procedure using hydrofluoric acid and nitric acid mixtures was used to eliminate the boron-doped region at the rear. Subsequently, the rear surface was oxidised in a wet chemical nitric acid solution to form a thin interfacial  $\text{SiO}_x$  layer  $\sim 1.5$  nm. Highly phosphorous-doped polysilicon ( $n^+$ -poly-Si) (150 nm of thickness) was formed on top of the  $\text{SiO}_x$  layer by depositing doped hydrogenated amorphous silicon (a-Si:H) using the plasma enhanced chemical vapour deposition (PECVD) method with gas precursors such as silane ( $\text{SiH}_4$ ), hydrogen ( $\text{H}_2$ ), and phosphine ( $\text{PH}_3$ ), followed by a thermal solid-phase crystallisation at 900  $^\circ\text{C}$  for 30 min. A single-side etching and the wet chemical oxidation were implemented at the front to form the  $\text{SiO}_x$  layer, followed by PECVD-based  $p^+$ -a-Si deposition using mask alignment with  $\text{SiH}_4$ ,  $\text{H}_2$ , and diborane ( $\text{B}_2\text{H}_6$ ) gas precursors. Local boron-doped poly-Si ( $p^+$ -poly-Si) layers were formed after the thermal solid-phase crystallisation. Dielectric passivation layers, including stacks of atomic layer deposition (ALD)-based  $\text{Al}_x\text{O}_y$  (10 nm)/PECVD-based  $\text{SiN}_x$  (65 nm), and PECVD-based  $\text{SiN}_x$  (75 nm) were grown at a temperature of  $< 200$   $^\circ\text{C}$ , followed by post-heating at 450  $^\circ\text{C}$ , on the front and rear sides, respectively. Finally, screen-printed metallisation was applied to both sides of the sample.

To obtain single-layer properties,  $p^+$ -poly-Si layers were deposited on symmetrical both sides of planar CZ wafers and on one-side of quartz



**Fig. 4.** Passivation quality as a function of GR, including (a) lifetime, and (b) implied  $V_{\text{oc}}$  ( $iV_{\text{oc}}$ ) and recombination current density ( $J_o$ ).



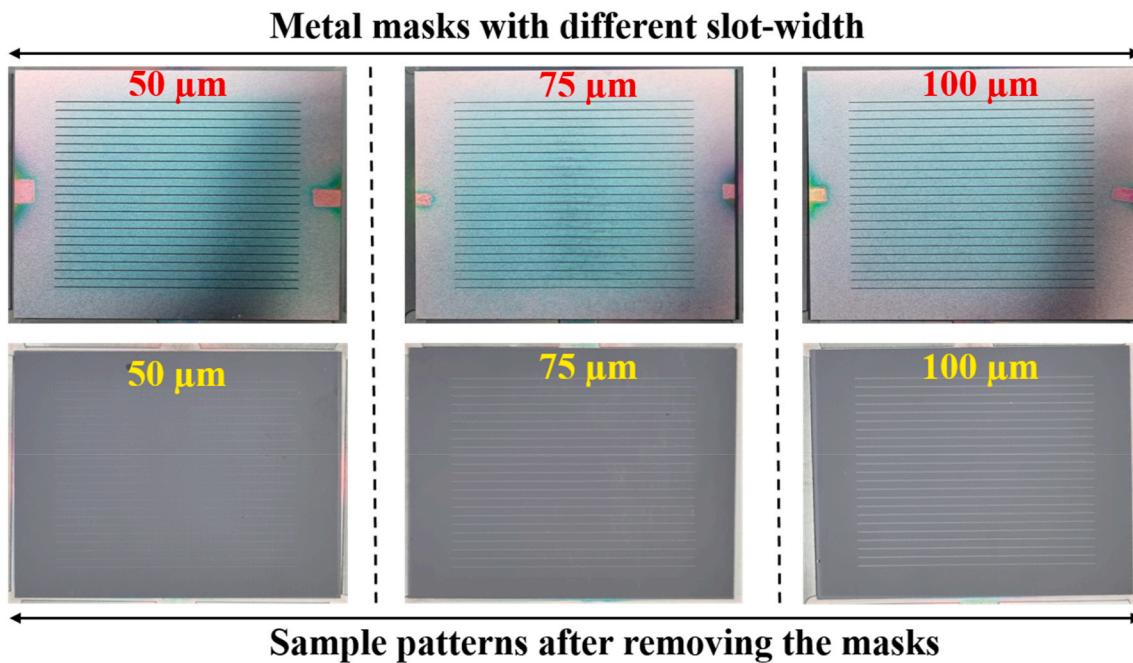
**Fig. 5.** Boron profile as a function of poly-Si/c-Si depth at different GR using SIMS measurement.

substrates. Raman spectroscopy (500i Ramboss system, Dongwoo Optron) and high-resolution transmission electron microscopy (HRTEM; JEM-2100F, JEOL) were used to characterise the film structure. Raman signals and cross-section HRTEM images were taken for the poly-Si deposited on the quartz and CZ wafer substrates, respectively. From the Raman spectra, the crystalline volume factors ( $X_c$ ) were calculated using the following equation:  $X_c = I_{521}/(I_{521} + I_{480})$ , where  $I$  and the subscript represent the integrated area and peak position at the corresponding wavelength numbers, respectively. The surface passivation quality due to the  $p^+$ -poly-Si layers, fully covered symmetrically on both sides of the planar CZ wafers after the thermal process, was evaluated based on the minority carrier lifetime and implied open-circuit voltage ( $iV_{\text{oc}}$ ) using a photoconductance lifetime tester (WCT-120, Sinton). In addition, the recombination current density ( $J_o$ ) values were extracted using the Kane-Swanson approach [23] from transient photoconductance decay tests. Secondary ion mass spectroscopy (SIMS) and transfer length measurement were used to evaluate the carrier concentration doped into the samples and contact resistivity ( $\rho_c$ ), respectively. For conductive characterisation,  $p^+$ -poly-Si layers were deposited on quartz substrates and measured on a surface couple of evaporated aluminium electrodes. The devices were characterised by light I-V curves (LIV) under standard illumination (1 sun, AM1.5, and 25 °C).

### 3. Results and discussion

The passivation quality of a poly-Si passivating contact is derived from the chemical surface passivation of thin  $\text{SiO}_x$  and the additional field-effect passivation (AFP) of heavily doped poly-Si layers [16,24,25]. As a result, poly-Si optimisation for high crystallisation and heavy doping is a prerequisite. Furthermore, owing to the device's use as the emitter, the thickness of the poly-Si layer must be optimised to minimise parasitic absorption losses while maintaining a high conductivity for carrier collection. The doping level and crystallinity of poly-Si are examined by varying the  $[\text{B}_2\text{H}_6]/[\text{SiH}_4]$  gas ratio (GR) during PECVD-based a-Si:H deposition, and the thickness is then optimised using the metal masks. Fig. 3a and b shows the Raman spectra of  $p^+$ -poly-Si as a function of  $[\text{B}_2\text{H}_6]/[\text{SiH}_4]$  gas ratio (GR), such as 0.6, 1.0, 1.4, and 1.8, before and after annealing, respectively. Before annealing (Fig. 3a), the amorphous phase, characterised by a broad peak at  $480 \text{ cm}^{-1}$ , dominated the film structure. After annealing (Fig. 3b), there was a phase transition from an initial amorphous phase to solid-phase crystallisation (poly-Si), characterised by sharp peak intensities at  $520 \text{ cm}^{-1}$ . As shown in Fig. 3b, the intensity of the peaks was reduced significantly when GR > 1.0. Fig. 3c shows a significant reduction in  $X_c$  from ~90% at GR ≤ 1 to ~68% at GR > 1. This indicates that the solid-phase crystallisation and/or crystalline quality of  $p^+$ -poly-Si after annealing degrades with increasing doping concentration (GR > 1). A high dopant level can cause significant defects such as lattice dislocations, vacancies, and/or interstitial impurities, which can degrade the crystalline quality. In addition, the degradation can impede dopant activation and thus reduce the conductivity [13,14]. Fig. 3d shows the dark conductivity of poly-Si as a function of GR. The conductivity was reduced at GR > 1 instead of increasing further with increasing doping level (GR). This implies that the degradation in crystallisation at GR > 1 appeared to negatively affect both the dopant activation (carrier concentration) and carrier mobility, resulting in detrimental conductivity.

Fig. 4 shows the passivation quality as a function of GR, including the lifetimes (4a),  $iV_{\text{oc}}$  (4b), and  $J_o$  (4b). The lifetime (injection level of  $10^{15} \text{ cm}^{-3}$ ) increased from 875  $\mu\text{s}$  to 915  $\mu\text{s}$  with increasing GR from 0.6 to 1.0, then decreased considerably to 612  $\mu\text{s}$  and 506  $\mu\text{s}$  with increasing GR to 1.4 and 1.6, respectively. When GR increased from 0.6 to 1.0,  $iV_{\text{oc}}$  increased from 721 mV to 725 mV but then decreased significantly when GR > 1.  $J_o$  exhibited an inverse correlation with  $iV_{\text{oc}}$ . A good poly-Si passivating contact must have a high  $iV_{\text{oc}}$ , and/or low  $J_o$  and  $\rho_c$  [9, 26]. The optimal point for passivation quality may be at GR = 1.0, where a high  $iV_{\text{oc}}$  of 725 mV and a low  $J_o$  of 12  $\text{fA}/\text{cm}^2$  were achieved. AFP may



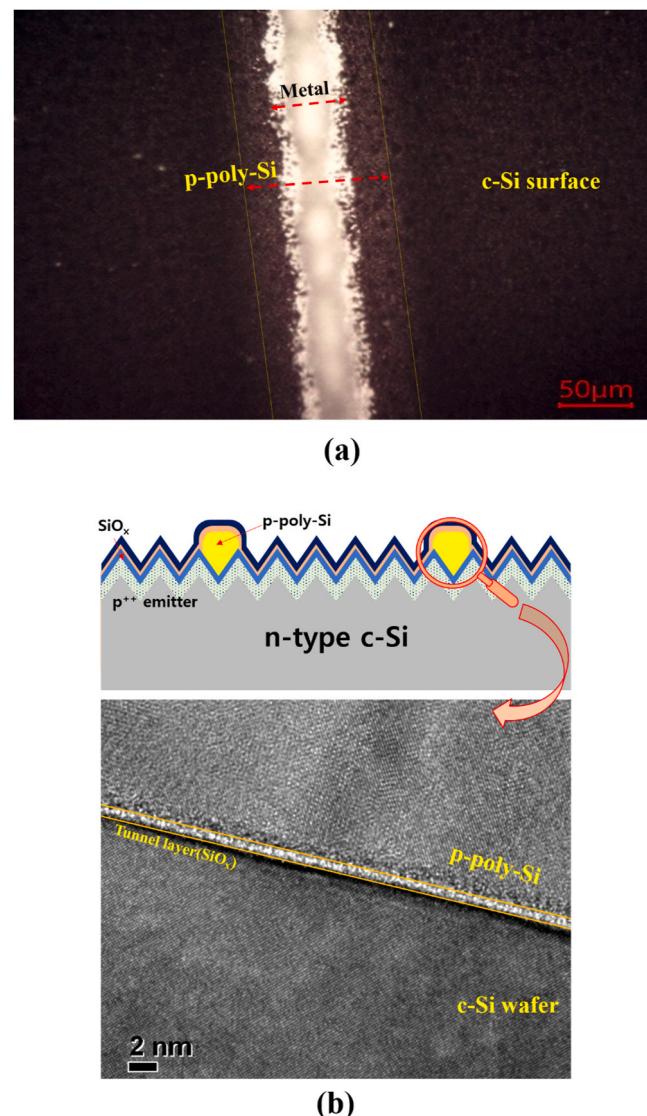
**Fig. 6.** Actual photos of masks with different finger widths (slot widths) (row up) and p<sup>+</sup>-a-Si:H patterns deposited on planar wafers using the corresponding masks.

be responsible for the improved passivation quality at GR = 0.6–1.0. In AFP, highly active dopants (high conductivity) are required to raise the Fermi level closer to their conduction band, resulting in higher band bending at the c-Si interface, better carrier-selective contact effect, and therefore, better passivation quality [16,25]. However, when GR exceeds 1.0, crystallisation degradation may reduce dopant activation and cause recombination, such as Auger recombination, within poly-Si, resulting in a poor passivation quality. In addition to impairing crystallisation, excessive doping at GR > 1 may promote intense dopant diffusion into the absorber during annealing, resulting in Auger recombination within the c-Si host and poor passivation quality. Fig. 5 depicts the boron profile as a function of depth at different GR. The doping concentration within the poly-Si layer increased with increasing GR. A high boron concentration of over  $10^{21}$  atom/cm<sup>3</sup> was recorded within p<sup>+</sup>-poly-Si at GR > 1, resulting in a high dopant concentration of  $>6 \times 10^{20}$  atom/cm<sup>3</sup> diffused deeply at a distance of 200 nm from the interface. It is suggested that the dopant from poly-Si shallowly diffused into the c-Si interface to form a conductive contact (pinhole) [19,27,28]. However, deep diffusion, as in the case of GR > 1, might result in increased Auger recombination at the interface, thereby reducing the passivation quality [16]. GR ≤ 1 significantly reduced dopant diffusion, resulting in enhanced passivation quality. Notably, the SIMS profile provides the total amount of boron within a sample; however, the conductivity of a sample is mostly determined by the quantity of activated dopant and carrier mobility. Although a high dopant concentration of  $>10^{21}$  atom/cm<sup>3</sup> was detected at GR > 1, inefficient dopant activation owing to crystalline degradation may be one of the main reasons for the low conductivity, as shown in Fig. 3d.

Mask alignment was employed to fabricate a TOPCon device from p<sup>+</sup>-poly-Si at GR = 1. The masks were prepared with finger widths (slot widths) of 50, 75, and 100 μm. Initially, boron-doped hydrogenated amorphous silicon (p<sup>+</sup>-a-Si:H) layers were deposited on planar wafers using masks to test uniformity. Fig. 6 shows photographs of the masks with different finger widths and the corresponding p<sup>+</sup>-a-Si:H patterns deposited on wafer substrates. The width of the local poly-Si should perfectly match the optimal finger width for metallisation (~40 μm).

The 50-μm finger-width mask showed poor uniformity of local p<sup>+</sup>-a-Si:H fingers, owing to significant shadow-effect - scattering at the edges of the mask during plasma deposition, whereas the 75- and 100-μm finger-width masks showed good uniformity. However, the local 100-μm p<sup>+</sup>-poly-Si fingers are significantly larger than those of metallisation (40 μm), and they cause significant parasitic absorption losses. As a result, a 75-μm mask was selected as the best mask for device fabrication. Fig. 7a shows an optical microscopy image of the local p<sup>+</sup>-poly-Si after metallisation. It was determined that a 75-μm-wide p<sup>+</sup>-poly-Si layer formed locally just underneath a 40-μm metal finger. The finger metallisation was positioned at the centre of the poly-Si width, indicating proper mask alignment. Fig. 7b shows the cross-sectional HRTEM images of the poly-Si/c-Si contact. This defines the formation of a thin interfacial SiO<sub>x</sub> (~1.5 nm) layer followed by a highly crystalline p<sup>+</sup>-poly-Si layer. The HRTEM results indicated that the initial p<sup>+</sup>-a-Si:H phase transformed into a highly polycrystalline phase (large crystalline grains) after the annealing process.

Fig. 8a shows the schematic structure of the 75-μm mask-fabricated device. Fig. 8b and c shows the  $\rho_c$  and LIV curves of the devices, respectively, as a function of the local p<sup>+</sup>-poly-Si thickness. Table 1 shows the cell parameters, including the open-circuit voltage ( $V_{oc}$ ), short-circuit current density ( $J_{sc}$ ), fill factor, and efficiency ( $E_{ff}$ ), as a function of thickness. A reference device without local p<sup>+</sup>-poly-Si was described for comparison. In Fig. 8b,  $\rho_c$  increased slightly to 8.4 mΩ cm<sup>2</sup> at 70 nm thickness, which was slightly higher than the 2.4 mΩ cm<sup>2</sup> of the reference, and then increased significantly over 15 mΩ cm<sup>2</sup> at thickness >70 nm. As shown in Table 1, the reference device had a low  $V_{oc}$  of 695 mV and high  $J_{sc}$  and FF of 40.6 mA/cm<sup>2</sup> and 81%, respectively. When compared to the reference cell parameters, the  $V_{oc}$  of the devices with local poly-Si increased, while the  $J_{sc}$  and FF decreased consistently with increasing thickness. The increased thickness of the local poly-Si may effectively prevent direct contact, resulting in improved surface passivating quality and a higher  $V_{oc}$ . However, such an increase almost definitely resulted in large parasitic absorption losses at the front because of the high absorption of p<sup>+</sup>-poly-Si, which increases with thickness and deteriorates  $J_{sc}$ . In addition, as shown in Fig. 8b,



**Fig. 7.** (a) Optical microscopic image, and (b) cross-section HRTEM image of local  $p^+$ -poly-Si after metallisation.

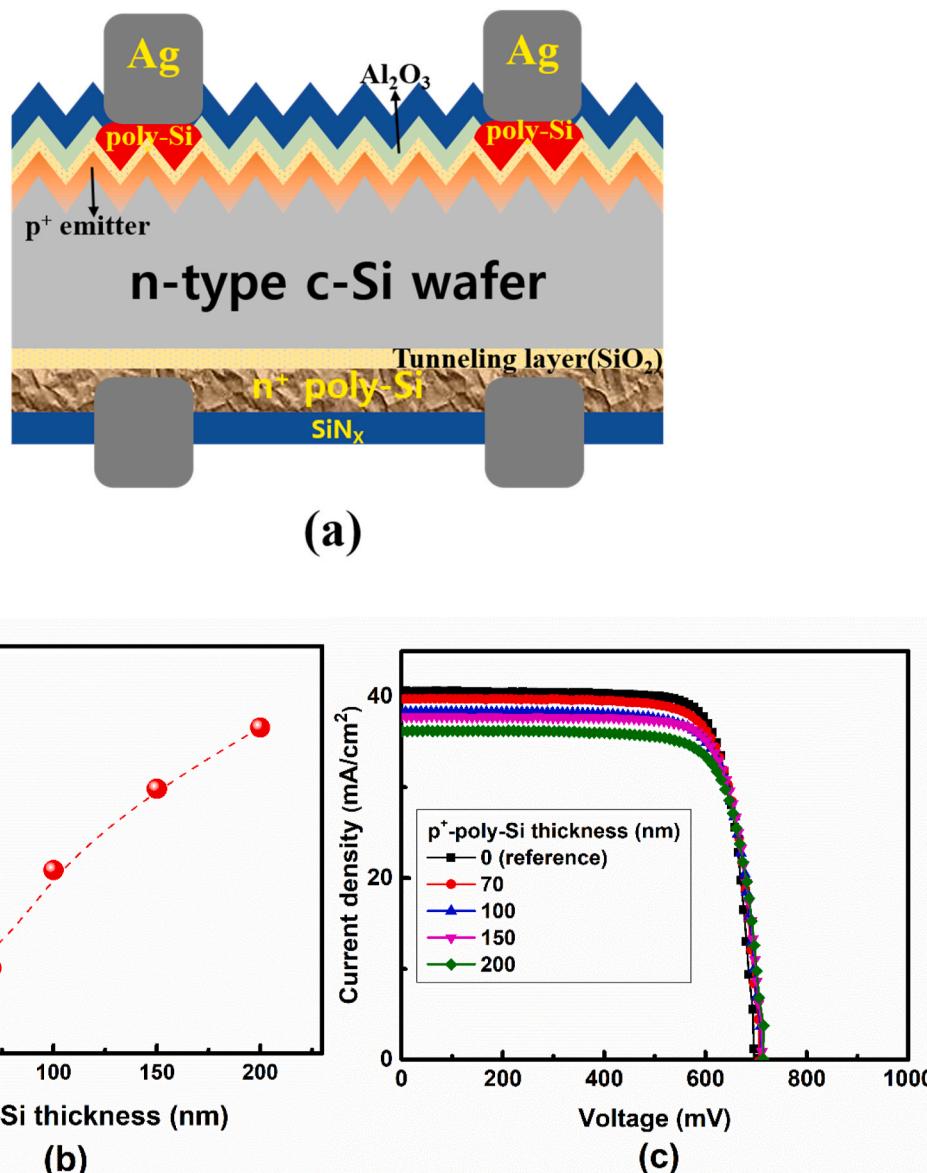
increasing the thickness causes an increase in  $\rho_c$ , resulting in a detrimental FF. While  $V_{oc}$  was improved, the considerable deterioration in  $J_{sc}$  and FF apparently resulted in efficiencies of the devices with the local poly-Si being lower than the reference. The  $E_{ff}$  (22.1%) of the 70-nm local  $p^+$ -poly-Si device was comparable to that of the reference (22.8%). To improve the efficiency, parasitic absorption losses and deleterious  $\rho_c$  at the front of the local poly-Si should be considered in future studies. Nevertheless, the local  $p^+$ -poly-Si method has considerable potential for reducing the direct contact at the front of the TOPCon device, thereby improving  $V_{oc}$ .

#### 4. Conclusions

To minimise direct contact between the metal and the c-Si host, a local poly-Si passivating contact was formed exclusively below the metal fingers utilising mask alignment. Poly-Si was designed with good passivation quality and low contact resistance. The masks were adjusted for optimum poly-Si area homogeneity, and to match the width of the

metal finger (40 μm). Because of the considerable reduction in direct contact, the TOPCon devices with local poly-Si demonstrated an excellent improvement in  $V_{oc}$  compared to the reference. However, they suffer mostly from degradation in  $J_{sc}$  and FF as a result of the greater finger area (75 μm) of local poly-Si than that (40 μm) of the metallisation. This results in significant parasitic absorption losses and an increase in  $\rho_c$ . Nonetheless, the local poly-Si employing the mask-alignment methodology proved to be a simple and effective method for overcoming the direct contact disadvantage in c-Si solar cells. The following strategies should be used to enhance the  $J_{sc}$  and FF:

- To eliminate parasitic absorption losses at the front, the mask-alignment method should be optimised considering the poly-Si finger area, set precisely equivalent to that of metallisation. Otherwise, wide-gap materials should be used instead of the local poly-Si.
- To further minimise  $\rho_c$ , the doping concentration, thickness reduction, and high-quality crystallisation of local poly-Si should be addressed.



**Fig. 8.** (a) Schematic structure of fabricated TOPCon device, (b) contact resistivity ( $\rho_c$ ), and (c) LIV curves of the TOPCon device as a function of p<sup>+</sup>-poly-Si thickness.

Cell parameters of the TOPCon devices as a function of p <sup>+</sup> -poly-Si thickness.				
Local p <sup>+</sup> -poly-Si thickness (nm)	V <sub>oc</sub> (mV)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	FF (%)	E <sub>eff</sub> (%)
0 (reference)	695	40.6	81	22.8
70	705	39.7	79	22.1
100	709	38.3	78.4	21.2
150	711	37.8	78.0	20.9
200	714	36.2	76.3	19.7

This will potentially aid the further development of local poly-Si at the emitter in TOPCon solar cells.

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#### CRediT authorship contribution statement

**Sungheon Kim:** Writing – original draft, Methodology, Data curation, Conceptualization. **Sungjin Jeong:** Investigation, Formal analysis. **Hongrae Kim:** Investigation, Formal analysis. **Muhammad Quddamah Khokhar:** Software, Data curation. **Suresh Kumar Dhungel:** Resources, Methodology. **Vinh-Ai Dao:** Software, Formal analysis. **Duy Phong Pham:** Writing – review & editing, Writing – original draft, Validation, Supervision, Methodology, Conceptualization. **Youngkuk Kim:** Visualization, Validation, Supervision. **Junsin Yi:** Writing – review & editing, Supervision, Project administration, Funding acquisition.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

Data will be made available on request.

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