Physica B 403 (2008) 3718–3723

Contents lists available at ScienceDirect

Physica B

journal homepage: www.elsevier.com/locate/physb

The structural and electrical properties of TiO_2 thin films prepared by thermal oxidation

P. Chowdhury [a,*], Harish C. Barshilia [a], N. Selvakumar [a], B. Deepthi [a], K.S. Rajam [a], Ayan Roy Chaudhuri [b], S.B. Krupanidhi [b]

[a] Surface Engineering Division, National Aerospace Laboratories, Bangalore 560 017, India
[b] Material Research Center, Indian Institute of Science, Bangalore 560 012, India

ARTICLE INFO

Article history:
Received 7 May 2008
Received in revised form
11 June 2008
Accepted 17 June 2008

PACS:
72.20.−i
72.60.+g
73.40.Qv

Keywords:
Titanium oxide
Metal–oxide–semiconductor
Oxidation
Sputtering

ABSTRACT

Thin films of TiO_2 were grown on n-type Si substrate by thermal oxidation of Ti films deposited by dc sputtering. The phase purity of TiO_2 was confirmed by Raman spectroscopy, and secondary ion mass spectroscopy was used to analyze the interfacial and chemical composition of the TiO_2 thin films. Metal–oxide–semiconductor capacitors with Al as the top electrode were fabricated to study the electrical properties of the TiO_2 films. The current conduction mechanisms in thermally grown TiO_2 films were observed to follow the space charge-limited current mechanism followed by a Schottky emission process both at and above room temperature. Three orders of magnitude of reduction in current density were observed for thermally grown samples while measured the *I–V* characteristics at 77 K and Fowler–Nordheim (F–N) tunneling was found to be a dominant conduction mechanism at higher biasing voltages.

1. Introduction

Rapid scaling down of the transistor feature size to 45 nm has forced to decrease the gate dielectric thickness and the channel length. Though it is possible to scale down the thickness of nearly perfect SiO_2 gate dielectric in the current complementary metal–oxide–semiconductor (CMOS), there are two limiting factors to overcome. One is the drastic increase of the leakage current due to the direct tunneling limit for SiO_2 thickness of 1.5 nm [1]. Other limiting factor is the reliability, i.e., the breakdown voltage decreases with decreasing the gate thickness because of increasing electric field at the same gate bias. Replacing SiO_2 gate dielectric with a high-κ material faces a formidable challenge.

Keeping the motivation for the search of high-κ materials, extensive studies have been carried out on several metal oxides, such as ZrO_2 [2,3], Ta_2O_5 [4], TiO_2 [5–8], Al_2O_3 [9,10] and HfO_2 [11,12], for the replacement of SiO_2. TiO_2 is considered as one of the potential candidates because its rutile phase has a high dielectric constant (~80), better thermal stability on Si and low leakage current density [1]. Another metastable phase of TiO_2 is anatase, whose dielectric constant varies from 12 to 30 [7]. Phase transition from anatase to rutile is possible with annealing in O_2 environment at temperatures higher than 700 °C [5]. To implement TiO_2 as a gate dielectric material, it is essential to understand both the structural and the electrical properties of this material. Both these properties strongly depend on the deposition techniques and the growth environment. Various techniques have been used to deposit TiO_2 films, such as chemical vapor deposition (CVD) [5], dc magnetron sputtering [7], jet vapor deposition (JVD) [13], thermally grown [6] and plasma oxidation [14]. In most of the deposition techniques, it was reported that annealing in O_2 or N_2 environment is required to reduce the leakage current as compared to the as-grown films [5]. The improvement in the oxide properties after annealing at higher temperatures is often counter-balanced by an increased thermal treatment and the growth of an interfacial SiO_2 layer at the TiO_2/Si interface.

Recently, growth of uniform TiO_2 films was reported using thermal oxidation of e-beam-evaporated Ti films in O_2 ambient by Chong et al. [6]. It has been shown that it was possible to achieve the leakage current density of 1×10^{-8} A/cm^2 for the films annealed at 550 °C for 30 min. Though their observed leakage current densities are of similar order of magnitude as reported by other deposition techniques, presence of traps or defects in the

* Corresponding author. Tel.: +91 080 250856452; fax: +91 080 25210113.
E-mail address: pchowdhury@css.nal.res.in (P. Chowdhury).

0921-4526/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.physb.2008.06.022

oxide was confirmed while analyzing the measured *I–V* data. Therefore, it is necessary to carry out further investigation on electrical properties of thermally oxidized Ti films grown by different techniques. Synthesis of dense rutile phase of TiO_2 thin films by thermal oxidation of sputtered Ti films was reported by Ting et al. [15], and extensive studies have been carried out on the structural and optical properties of the films annealed at different temperatures. Therefore, in the present work, we have synthesized TiO_2 film by thermal oxidation of sputter-deposited Ti films in the O_2 environment. To study the transport properties, Al top and bottom electrodes were deposited using thermal evaporation. We discuss in detail both the structural and the electrical properties in thermally grown samples.

2. Experimental

Thin films of titanium of thickness 15–20 nm were deposited using dc magnetron sputtering system on n-type Si (resistivity ~10–40 Ω cm) substrates at room temperature. The substrates were cleaned in an ultrasonic bath using acetone, absolute alcohol and trichloroethylene. Titanium (purity ~99.99%) of 76 mm diameter and 6.4 mm thickness has been used as a sputtering target. Pure Ar (99.999%) was used as the sputtering gas. The target to substrate distance was 54 mm. Before the deposition, the target was cleaned in order to remove the surface oxide layer. The base pressure of the chamber was $\sim 10^{-5}$ Pa and the low partial pressure of other impurity gases (such as hydrogen (10^{-5} Pa), nitrogen (2×10^{-6} Pa), oxygen (10^{-6} Pa) and moisture (4×10^{-6} Pa)) was confirmed using residual gas analyzer (RGA). During the deposition, dc power of 35 W was applied, which resulted in a deposition rate of 2 Å/s. As deposited Ti films were thermally oxidized at 500 °C in 1 mbar O_2 pressure for 3 h.

Secondary ion mass spectroscopy (SIMS) used for studying the interface profile is of quadrupole type (Model MIQ 256, Cameca-Riber). The depth profiling of Si/TiO_2 structure was carried out with Ga primary ions and the positive secondary ions were collected for the analysis. The beam energy and the current were optimized at 25 keV and 4 nA, respectively. The sputtered area was approximately $10 \times 10\ \mu m^2$.

The phase purity of TiO_2 films was characterized using a DILOR-JOBIN-YVON-SPEX-integrated micro-Raman spectrometer. An HeNe laser of 20 mW was used as the excitation source. The details of the experimental setup are described elsewhere [16,17]. The surface morphology of the oxide films was studied using atomic force microscopy (AFM). Metal–oxide–semiconductor (MOS) capacitor structures were fabricated to characterize the TiO_2 thin films. Both top and bottom contact pads of area $2.5 \times 10^{-3}\ cm^2$ were made by aluminum of thickness ~500 Å, which were deposited by thermal evaporation. The capacitors thus fabricated were electrically characterized by current–voltage (*I–V*) and capacitance–voltage (*C–V*) methods. *I–V* characteristics measurements were carried out using Keithely 2400 source meter at different set temperatures. Room temperature *C–V* measurements were performed using Agilent 4294 impedance analyzer. The voltage bias was ramped from inversion to the accumulation region.

3. Results and discussion

3.1. Structural analysis

Fig. 1 shows the Raman spectrum of the TiO_2 film grown by thermal oxidation. It is to be mentioned that Raman measurements have been carried out on film of thickness of 100 nm for better signal. The peak centered at 521 cm^{-1} is due to silicon. Reported peak positions for anatase phase of TiO_2 are 145, 395, 514 and 639 cm^{-1}, whereas for rutile phase of TiO_2, the peak positions are 447 and 612 cm^{-1} along with a broad peak at 230 cm^{-1} [18]. From Fig. 1, it is clear that thermally grown sample shows rutile phase. These results confirm that the rutile phase formation is possible even at 500 °C for 6 h annealing of Ti film. This transformation of Ti film to single-phase rutile TiO_2 at 500 °C for longer duration or at higher oxidation temperatures is in agreement with the literature [15].

Fig. 2 shows SIMS depth profile of the TiO_2 /Si structure grown by thermal oxidation from 15-nm-thick Ti film. It is observed that both TiO and TiO_2 signals decay slowly with increasing the depth till 28 nm and with further increasing the depth, both the signals reduce sharply. When Ti film is fully oxidized to TiO_2, it is reported that the thickness of the film expanded by factor of 1.8 and therefore oxide thickness was expected to be 27 nm [6]. This value perfectly matches with value provided by the SIMS depth profile measurement. For depth greater than 28 nm, Ti signal intensity reduces at slower rate than those observed for the oxide signals, which indicates that the concentration of O atoms decreases as approached towards the Si substrates. This might be due to the diffusivity of Ti atom in Si as mentioned in the literature and this is almost one order magnitude higher than that of O in Si [19]. This also indicates that the interfacial layer has formed by reactions among Ti, Si and O atoms. The formation of SiO_2 and titanium silicate ($TiSiO_3$) at the interface at temperatures above 400 °C for thermally grown samples was reported by several authors [5,6,20].

The surface morphology of TiO_2 film was carried out by AFM and showed an rms roughness of 3.5 nm.

3.2. Current transport mechanism

Fig. 3 shows the *C–V* measured at 1 MHz frequency on 20-nm-thick thermally grown sample. When the device is biased in the strong accumulation region, the high frequency (1 MHz) capacitance was taken as the oxide capacitance (C_{ox}). The dielectric constant of the MOS capacitor is calculated from C_{ox} assuming the

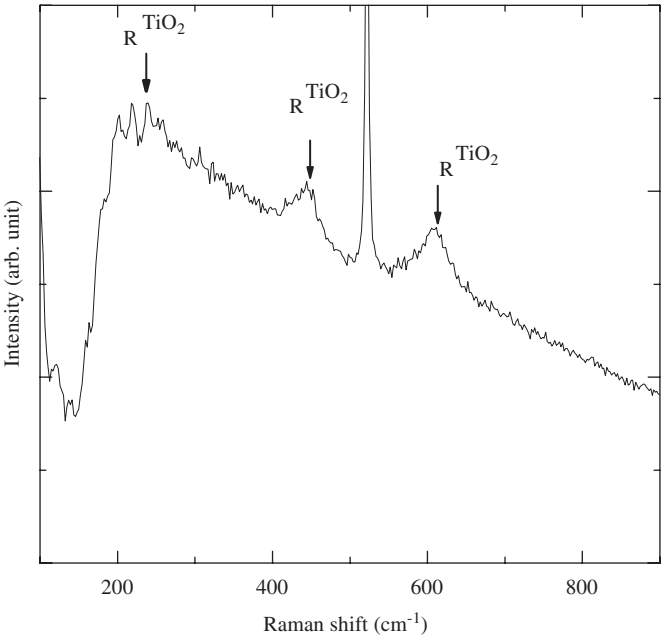

Fig. 1. Raman spectrum of thermally grown TiO_2 thin film. Observed rutile peak positions are indicated by arrowheads.

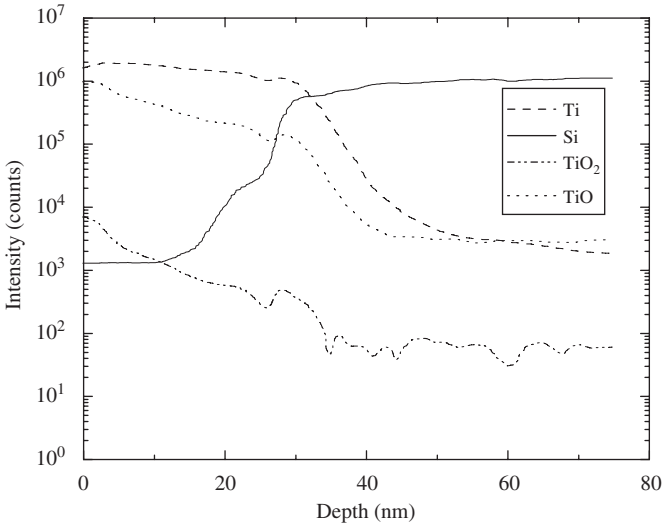

Fig. 2. SIMS depth profile of TiO_2 thin film grown by thermal annealing from 15-nm-thick Ti film.

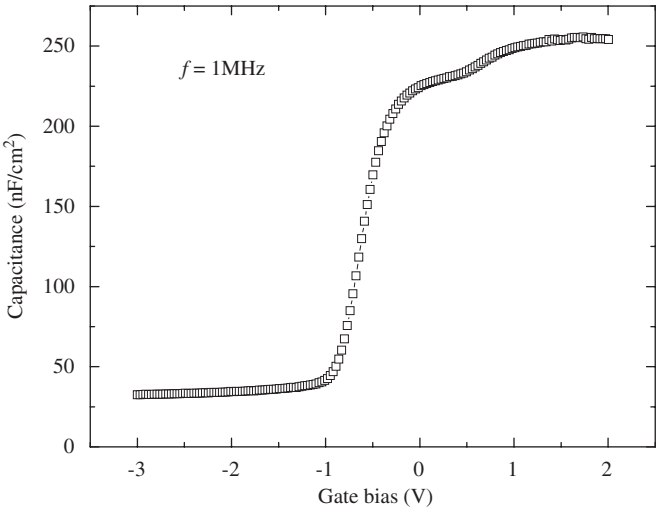

Fig. 3. *C–V* plot of TiO_2 thin film measured at frequency of 1 MHz.

nominal oxide thickness of 36 nm and the calculated value of dielectric constant was found to be 12.0. This value was very much close to the reported value of dielectric constant for thermally grown sample [6]. It is to be noted that due to thermal oxidation of 20-nm-thick Ti thin film, the film thickness was expanded by a factor of 1.8 and therefore the oxide thickness was estimated here as 36 nm.

C–V measurement is an effective method to evaluate fixed charges in the interfacial layer formed between the TiO_2 and Si interface. The source of fixed charges is thought to originate from the bonding of the atoms associated with the metal oxide dielectric materials near the dielectric/semiconductor interface. They are un-rechargeable and impact on electron channel mobility and hence result the degradation of the leakage current. This can be reflected from the shift of *C–V* curve while comparing with the ideal one.

Comparing the *C–V* data with the ideal simulated *C–V* curve, the flat band voltage (V_{FB}) was estimated as ~ -0.57 V. The oxide charge density (Q_i) can be calculated using the formula

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_{ox}},$$

where Φ_{ms} is the metal and semiconductor work function potential difference and was found out to be -0.35 V. Using Φ_{ms} and C_{ox}, the density of charge (negative), Q_i, is estimated to be $2.35 \times 10^{12}\,cm^{-2}$. Similar order of magnitude of the oxide charge density is reported in the literature for different MOS capacitor structures [1].

I–V characteristics of TiO_2 films have been studied with a MOS capacitor structure. The schematic diagram of the contact configuration of MOS capacitor structure is shown in the inset in Fig. 4. In our notation, the applied voltage V_B is positive, when the top electrode, i.e., metal gate, is positively biased with respect to the ohmic contact, and V_B is negative, when the gate is negatively biased with respect to the ohmic contact. In this MOS structure with n-type Si substrate, when a positive voltage ($V_B > 0$) is applied to the gate, the top of the conduction band bending towards Fermi level causes an accumulation of minority carriers (electrons) near the semiconductor–insulator interface. This region is called accumulation region, and in an ideal MOS structure there is no current flow in the semiconductor. When a negative voltage is applied, the minority carriers (electrons) are depleted at lower voltages, resulting in a so-called depletion region, and with further increasing the bias voltage, an inversion region is formed, where the density of majority carriers (holes) is more than the minority carriers near the semiconductor–insulator interface. All the *I–V* measurements have been carried out here for both positive and negative gate bias voltages and the expected currents are predominantly due to electrons and holes for positive and negative gate bias voltages, respectively.

Fig. 4 shows the *I–V* characteristics of TiO_2 MOS capacitor grown by thermal oxidation. These measurements have been carried out by sweeping the applied voltages from positive to negative side corresponding to the maximum current density of $1\,A/cm^2$. The results of current densities as a function of biasing voltages both in accumulation and inversion regions are shown in Fig. 4. *I–V* data have been recorded for two sets of temperatures, 300 and 77 K. The measurement at 77 K shows the reduction of the current density by three orders of magnitude at lower voltages, i.e., for $V_B < 3$ V, and its temperature dependence becomes weak with further increasing the bias voltage as shown in Fig. 4. This large reduction of the leakage current density at low temperature implies that thermally excited carriers play an important role in the current conduction at room temperature.

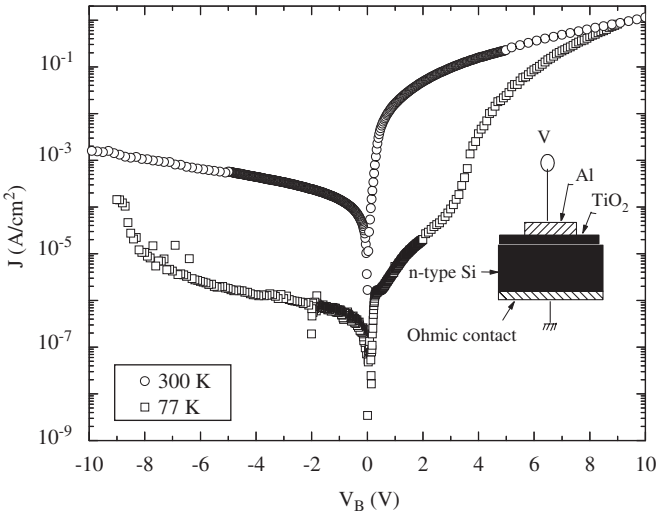

Fig. 4. Current–voltage characteristics of MOS capacitor with TiO_2 film with Al top electrode. *I–V* data are measured at 300 and 77 K. The inset shows the schematic diagram of Al/TiO_2/n-Si capacitor structure.

To understand these observed features, we have carried out further *I–V* measurements at different temperatures above 300 K.

3.2.1. High-temperature analyses

Fig. 5 shows *I–V* characteristics in log–log plot measured at different temperatures. All the high-temperature measurements were restricted to the compliance current of 10 mA. The whole dataset can be divided into three different domains based on the applied bias voltages, yielding different current conduction mechanism. We will discuss each region in the following section.

In most of the reported results [5,6,21], it has been shown that conduction mechanism in low bias region is governed by hopping mechanism. In this mechanism, the current is carried by thermally excited electrons hopping from one isolated state to the next. This mechanism yields an ohmic characteristic exponentially dependent on temperature and is described by the following relation [22]:

$$J = cV_B \exp\left(-\frac{\Delta E_{ae}}{k_B T}\right), \tag{1}$$

where ΔE_{ae} is the activation energy of the electrons and k_B is the Boltzman constant. The signature of ohmic region (with slope ~1.0), i.e., the first domain, measured at different temperatures is shown in Fig. 5 and exists till for the bias voltage of 0.1 V. The plot of $\ln(I)$ vs. $1/T$ gives a linear slope and the activation energy calculated from these data is ~0.2 eV.

For higher gate voltages, two main conduction processes were invoked to explain the carrier transport in this sample, i.e., Schottky or thermionic emission (SE) [5,6,22] and space charge-limited current (SCLC) [22–24].

The thermionic or SE across the metal–insulator interface or the insulator–semiconductor interface is responsible for the carrier transport. Generally, the conduction through SE process depends strongly on the barrier between the metal and the insulator and is generally observed for the insulators with fewer defects. The *I–V* relationship of the SE can be expressed as [6,22]

$$J = A_{th}T^2\left[\exp\left(-\frac{q\Phi_0}{k_B T}\right)\right]\exp\left[\frac{q}{k_B T}\left(\frac{qV_B}{4\pi\varepsilon_r\varepsilon_0 d_{ox}}\right)^{1/2}\right], \tag{2}$$

where Φ_0 is the extraction work function at the metal–semiconductor interface, ε_r is the relative dielectric constant, ε_0 is the vacuum permittivity, d_{ox} is the oxide thickness and A_{th} is the Richardson–Dushmann constant. The extrapolated value of the current density to zero voltage gives the saturation current density, J_s, and the barrier height can be obtained using the following relation:

$$\Phi_0 = \frac{k_B T}{q}\ln\left(\frac{A_{th}T^2}{J_s}\right). \tag{3}$$

Fig. 6 shows the I vs. $V_B^{1/2}$ plot in semi-log scale of the experimentally measured *I–V* data above 300 K in the applied voltage range between 0.1 and 0.5 V. The straight-line characteristics at different temperatures confirm the SE process. The extracted Schottky barrier heights obtained are 0.78 ± 0.05 V. These values are very close to the reported data for TiO_2 thin films [8]. Therefore, for the second domain, i.e., for voltage range $0.1 < V_B < 0.5$ V, the *I–V* data can be explained very well using the SE process.

Fig. 7 shows a linear behavior in $\ln(I)$ vs. $\ln(V_B)$ plot for voltages above 0.5 V for different set temperatures. It is interesting to see that the slope, n ($= |\mathrm{d}\ln(I)/\mathrm{d}\ln(V_B)|$), was obtained as 1.8 ± 0.1 for all the curves, which is very close to 2. This implies that the current density is directly proportional to the square of the voltage and could be explained using SCLC conduction mechanism. Presence of SCLC in sputter-deposited TiO_2 thin films was reported by Stamate [24]. For structures where carriers can readily enter the insulator and freely flow through the insulator, one finds that the resulting current and carrier densities are much higher. The high density of these charged carriers causes a field gradient, which limits the current density. Then the current dependence on the voltage drop for the unipolar trap free case follows a well-known quadratic law [22]:

$$J_{sc} = \frac{9}{8}\frac{\mu\varepsilon_r\varepsilon_0}{d_{ox}^3}V_B^2, \tag{4}$$

where μ is the carrier mobility. The agreement of the *I–V* data with SCLC mechanism, even for different set of temperatures, implies that the defects densities in thermally grown samples are less. Presence of structural defects in the insulator causes additional energy states close to the band edge, called traps. These traps restrict the current flow because of a capture and emission process. Under this condition, the current transport in the insulators is well explained by Poole–Frenkel (P–F) emission in different oxide materials [1,6,21].

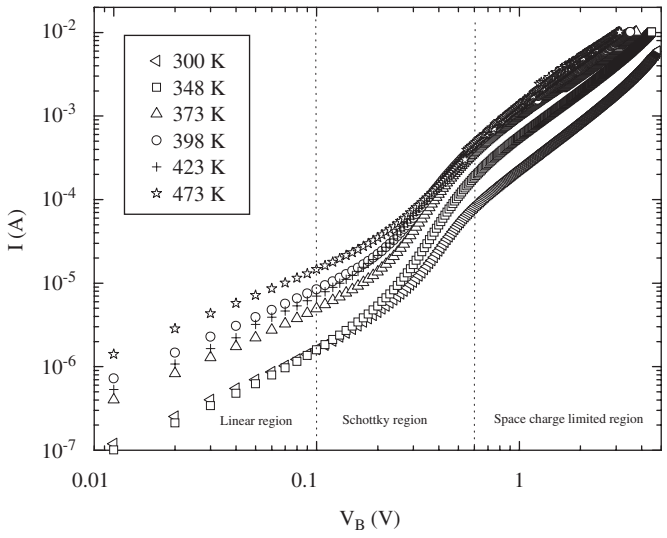

Fig. 5. A log–log plot of current voltage characteristics of MOS capacitor measured at different temperatures at and above 300 K. *I–V* set measured at different temperatures can be divided into three regions: linear, Schottky and space charge-limited regions. See the text for details.

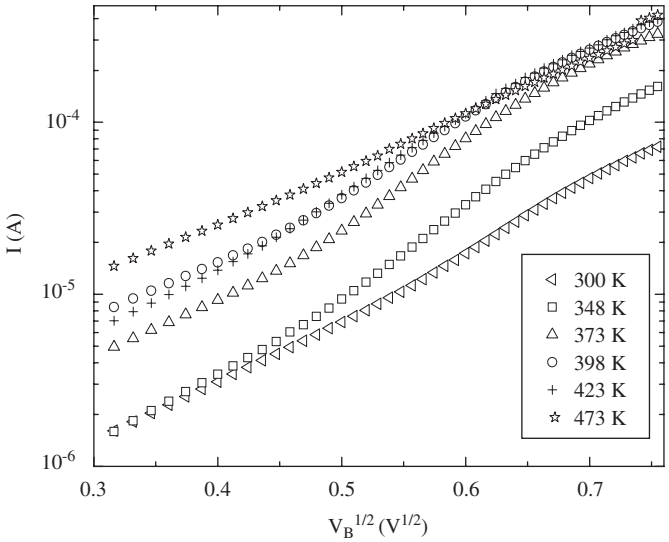

Fig. 6. Schottky plots of measured *I–V* data at different temperatures.

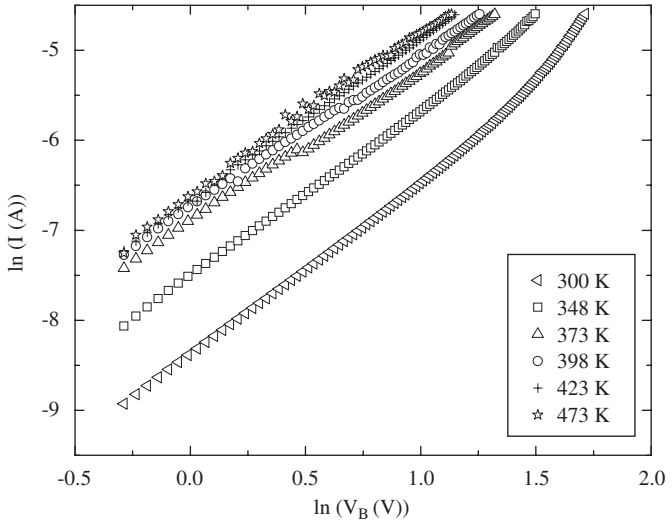

Fig. 7. Plot $\ln(I)$ vs. $\ln(V_B)$ of *I–V* data measured at higher bias voltages and at different temperatures. The slope $\sim 1.8 \pm 0.1$ of these linear plots implies that I is proportional to V_B^2.

3.2.2. Analyses at low temperature

At 77 K, the conduction by thermal-activated carriers will be suppressed. Therefore, a reduction of leakage current density by almost three orders of magnitude was observed. Analyses of *I–V* data for this sample revealed that the whole dataset can be divided into three regions based on different conduction mechanisms, as shown in Fig. 8. At lower biases region, i.e., for $V_B < 0.5$ V, the hopping conduction is a dominant current transport mechanism. As the bias is increased, the current increases exponentially and follows SE behavior as described by Eq. (2). The linear plot of $\ln(I)$ vs. $V^{1/2}$, shown in upper inset in Fig. 8, confirms the presence of SE process for the voltage ranges between $0.5\,\text{V} < V_B < 3.0\,\text{V}$ and the barrier height 0.8 eV. With further increasing the gate voltages above 3.0 V, the conduction is dominated by conventional Fowler–Nordheim (F–N) relationship [6,21,22], as shown in lower inset in Fig. 8. In this mechanism, the electrons will tunnel through the triangular barrier to the conduction band (valance band) of the oxide. The F–N tunneling can be expressed as

$$J_{FN} = A_{FN} V^2 \exp\left(-\frac{B_{FN}}{V_B}\right), \tag{5}$$

where A_{FN} and B_{FN} are constants and B_{FN} can be expressed as

$$B_{FN} = \frac{8\pi\sqrt{2m^* m_0}(q\Phi_B)^{3/2} d_{ox}}{3qh}, \tag{6}$$

where all the symbols are defined as earlier. The F–N plot of Al/TiO_2/p-Si capacitor for positive gate bias is shown in lower inset in Fig. 8. This shows a linearity in F–N plot of about three orders of magnitude of the leakage current and the tunneling barrier, Φ_B, between TiO_2 and Si at the conduction band was estimated using Eq. (6), which gives $0.5\,\text{eV} \pm 0.05\,\text{V}$. Theoretically, the conduction band offset from TiO_2 to Si is around 1.2 eV and experimentally reported value for Pt/TiO_2/p-Si was 0.73 eV [6]. Our estimated value of Φ_B is less in comparison to the reported value due to the Al top electrode, which was observed to react with the oxygen in the TiO_2 thin films at the Al/TiO_2 interface and the effective oxide thickness is depleted [6]. Evidence of F–N tunneling at low temperature and SCLC mechanism at high temperatures confirms less defects in the thermally annealed oxide samples. Because during this annealing process, the probability of introducing defects is very less as it is a diffusive process.

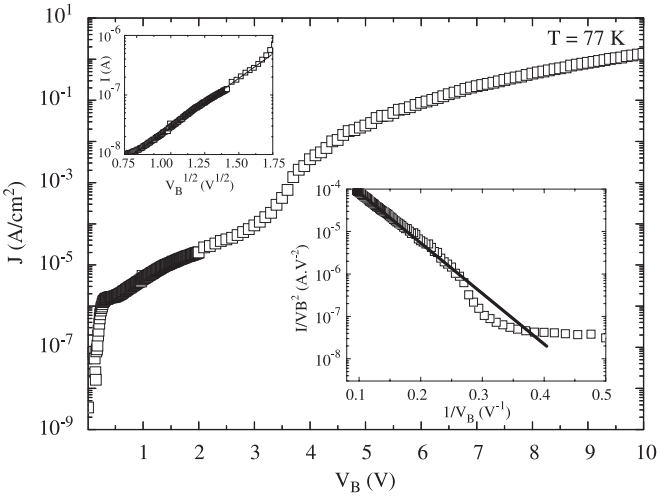

Fig. 8. Current–voltage plot in semi-log measured at 77 K. The upper inset shows the Schottky plot of the data for voltage vs. I in the range of 0.5–3.0 V. The lower inset presents I/V_B^2 vs. $1/V_B$ in a semi-log scale. The linear behavior of this plot implies Fowler–Nordheim behavior for biasing voltages above 3.0 V.

4. Conclusion

We have fabricated MOS capacitor with top Al electrode to study the structural and electrical properties in thermally grown TiO_2 thin films. Raman spectrum confirmed the rutile phase formation of TiO_2 films grown by annealing at 500 °C for 3 h in O_2 ambient. SIMS data indicate that the interface layer has formed by reacting among Ti, Si and O atoms. It also reflects that the diffusivity of Ti atoms in Si substrate is higher than that of O atom. Both at and above room temperatures, space charge-limited current mechanism was found to be the dominant mechanism for these films. However, at low temperature, F–N tunneling of electrons was observed to be a dominant mechanism.

Acknowledgments

The authors thank the director, NAL, for giving permission to publish these results. Mr. Jakeer Khan and Ms. B. Deepthi are thanked for sample preparation.

References

[1] G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. 89 (2001) 5243.
[2] M. Houssa, V.V. Afanas'ev, A. Stemans, M.M. Heyns, Appl. Phys. Lett. 77 (2000) 1885.
[3] T. Nagi, W.-J. Qi, R. Sharma, J. Fretwell, X. Chen, J.C. Lee, S. Banerjee, Appl. Phys. Lett. 76 (2000) 502.
[4] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka, M.M. Heyns, J. Appl. Phys. 87 (2000) 8615.
[5] S.A. Campbell, H.-S. Kim, D.S. Gilmer, B. He, T. Ma, W.L. Gladfelter, IBM J. Res. Dev. 43 (1999) 383.
[6] L.H. Chong, K. Malik, C.H. De Groot, R. Kersting, J. Phys.: Condens. Matter 18 (2006) 645.
[7] M. Kadoshima, M. Hiratani, Y. Shimamoto, K. Torii, H. Miki, S. Kimura, T. Nabatame, Thin Solid Films 424 (2003) 224.
[8] S. Chakraborty, M.K. Bera, S. Bhattacharya, C.K. Maiti, Microelectron. Eng. 81 (2005) 188.
[9] E.P. Gusev, M. Copel, E. Cartier, I.J.R. Baumvol, C. Krug, M.A. Gribelyuk, Appl. Phys. Lett. 76 (2000) 176.
[10] J. Kolodzey, E.A. Chowdhury, G. Qui, J. Olowolafe, C.P. Swann, K.M. Unruh, J. Suehle, R.G. Wilson, J.M. Zavada, Appl. Phys. Lett. 71 (1997) 3802.
[11] B.H. Lee, L. Kang, R. Neih, W.-J. Qi, J.C. Lee, Appl. Phys. Lett. 76 (2000) 1926.
[12] S.J. Lee, H.F. Luan, W.P. Bai, C.H. Lee, T.S. Jeon, Y. Senzaki, D. Roberts, D.L. Kwong, IEDM Tech. Dig. (2000) 31.
[13] X. Guo, X. Wang, Z. Luo, T.P. Ma, T. Tamagawa, IEDM Tech. Dig. (1999) 137.
[14] J.C. Tinco, M. Estrada, G. Romero, Microelectron. Reliab. 43 (2005) 895.
[15] C.C. Ting, S.Y. Chen, D.M. Liu, J. Appl. Phys. 88 (2000) 4628.

[16] H.C. Barshilia, K.S. Rajam, Surf. Coat. Technol. 201 (2006) 1827.
[17] H.C. Barshilia, K.S. Rajam, J. Mater. Res. 19 (2004) 3196.
[18] T. Mazza, E. Barborini, P. Piseri, P. Milani, D. Cattaneo, A. Li Bassi, C.E. Bottani, C. Ducati, Phys. Rev. B 75 (2007) 045416.
[19] H. Bracht, N.A. Stolwijk, Landolt-Bornstein—Group III Condensed Matter, vol. 33, Springer, 1998, p. 196.
[20] I.J.M.M. Raaijmakers, A.H. Reader, P.H. Oosting, J. Appl. Phys. 63 (1988) 2790.
[21] R. Perera, A. Ikeda, R. Hattori, Y. Kuroki, Microelectron. Eng. 65 (2003) 367.
[22] S.M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1969, p. 496.
[23] M.P. Houng, Y.H. Wang, W.J. Chang, J. Appl. Phys. 86 (1999) 1488.
[24] M.D. Stamate, Appl. Surf. Sci. 205 (2003) 353.