



Negative capacitance and negative dielectric behavior of MIS device with Rhenium-Type Schottky contacts

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ABSTRACT

This study offers a thorough examination of the negative capacitance/dielectric behavior of an MIS device with rhenium (Re) type Schottky contact and native oxide interlayer. The pulsed laser deposition method was used to deposit Re as the Schottky contact on the n-type GaAs substrates. Thus, the electrical and dielectric properties were evaluated by $I-V$, $C-V$, and $G/\omega-V$ tests at a high frequency (1 MHz). Experimental results demonstrated that capacitance characteristics showed a marked increase from the inversion region to depletion, with a localized peak observed at 0.26 V. Exceeding 4.16 V, the capacitance values turn negative, signifying a shift to inductive behavior, as shown by a rapid increase in conductance values under the same conditions. In addition, the dynamic resistance profile indicates that the series resistance (R_s) reaches its peak at near-zero bias and stabilizes under significant forward bias, approaching the device's intrinsic series resistance. Analysis of the $C-G/\omega-V$ data also showed two distinct peaks in the corrected conductance (G_c/ω) at -0.55 V and +0.1 V, due to the response of interface states (N_{ss}) located at distinct energy levels inside the GaAs bandgap. The transition from capacitive to inductive behavior was recorded with high enough forward bias, at which point the dielectric constant (ϵ') turns negative, showing the effects of polarization reversal and reactive energy storage. Additionally, the complex impedance analysis revealed distorted semicircular arcs and loop formations, indicative of interfacial inhomogeneities and multiple charge transport channels. As a result, these findings demonstrate that integrating Re into the MIS structure significantly improves the device's electrical stability and functional response under varying bias conditions, demonstrating its potential in advanced high-frequency and low-power electronic applications.

1. Introduction

Negative capacitance (NC) and negative dielectric (ND) behavior are developing phenomena that have attracted considerable interest in materials science and device engineering, especially with GaAs-based Schottky devices, some types of transistors, and other modern electronic devices [1–5]. These phenomena contest traditional interpretations of dielectric characteristics and capacitive behavior, presenting new avenues for novel applications in electronics, photonics, and energy storage systems. The study of negative capacitance is particularly important as it could open the way to devices with better

performance characteristics, such as faster switching speeds and lower power consumption [6].

Negative capacitance is a phenomenon in which a decrease in charge is the result of an increase in voltage across a dielectric material, which is in direct opposition to the behavior anticipated by standard capacitors. This phenomenon can be attributed to the occurrence of ferroelectric materials or specific composite structures exhibiting a negative dielectric constant under certain conditions. For instance, substances such as perovskites and specific varieties of Schottky devices [2,7–10]. Substances like perovskites and certain types of GaAs-based Schottky devices, irrespective of a particular interlayer, exhibit negative

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dielectric qualities, which can be utilized in the advancement of contemporary electronic gadgets [11–13]. The fundamental principles are often associated with complex interactions at material interfaces, where the dynamics of polarisation are essential for the emergence of negative capacitance.

Incorporating negative capacitance into metal-insulator-semiconductor (MIS) type Schottky devices can markedly improve their performance attributes. Negative capacitance can reduce the effective capacitance of the device, enabling faster switching times and reduced energy loss during operation [14–16]. This is especially pertinent in high-frequency applications where conventional capacitive components may restrict performance.

Negative dielectric behavior, characterized by a negative dielectric constant, is an essential feature of certain composite systems, including those that include carbon nanotubes or hybrid metal and dielectric. The distinctive electromagnetic properties of these materials are crucial for the advancement of metamaterials and photonic devices, facilitating functionalities such as negative refraction and customized light-matter interactions through meticulous control of structural design and composition [17–19].

The investigation of negative capacitance and negative dielectric properties in MIS devices is enhanced by the examination of innovative material systems and fabrication methods. Recent breakthroughs in nanocomposite materials, particularly those utilizing graphene and other two-dimensional substances, have exhibited the possibility of attaining adjustable dielectric characteristics applicable to device technologies. The integration of these materials into MIS structures optimizes dielectric responsiveness and improves charge transport properties, thus enabling the development of high-performance electronic devices [20–22].

Schottky devices, which form at the interface between metals and semiconductors, play an important role in improving the efficiency of electronic devices. The overall efficiency of devices such as diodes, transistors, and photodetectors is affected by the height of the Schottky devices, which greatly influences the mobility of charge carriers at the interface [23,24]. The simplicity of Schottky devices, combined with their ability to provide rectifying behavior, makes them highly desirable for applications in high-speed electronics and optoelectronics [25–27]. The integration of materials exhibiting negative capacitance properties into these structures can further enhance their performance by enabling faster switching and lower energy losses during operation [28,29].

MIS structures have significant potential because they combine the advantages of metal–semiconductor (MS) and metal–insulator (MI) interfaces. By introducing an insulating layer between the metal and the semiconductor, these devices improve charge transport control and stability [30]. The insulator interlayer can often be a natural oxide layer, or sometimes a specially grown layer. On the other hand, although well-known materials such as gold (Au), silver (Ag), and aluminum (Al) are preferred for metal contacts, it is beneficial to examine new materials in ohmic or Schottky contacts to improve Schottky device technologies. Rhenium (Re) is a potential material for use as a metal contact and to improve modern electronic device technologies.

Re, a transition metal recognized for its elevated melting point and superior electrical conductivity, has surfaced as a viable choice for Schottky connections in MIS devices. Its capacity to establish stable interfaces with various semiconductors enhances device efficiency, particularly under elevated temperature conditions, by diminishing contact [31–33]. The incorporation of Re into negative capacitance architectures facilitates the creation of advanced devices that use its exceptional electrical characteristics and distinctive behavior within the framework of negative capacitance [34].

Nanocomposites that use Re and GaAs semiconductors have made it possible for negative capacitance and dielectric properties to improve in MIS devices. Rhenium's high melting point and electrical conductivity make it appropriate for Schottky contacts, while GaAs-type semiconductors offer enhanced photodetection and charge transport

properties [35,36].

This paper looks at how to make and describe advanced MIS devices with Re-type Schottky contacts, focusing on their negative capacitance and negative dielectric properties. The subsequent sections will delineate the materials and methodologies, present experimental results through graphs and analysis, and assess the implications of these findings.

2. Experimental details

The application process of this study consists of three stages: 1) Cleaning the n-type GaAs semiconductor wafer, 2) Fabrication of the MIS devices consisting of Re-type Schottky/rectifier contacts and a natural oxide interlayer, and 3) Performing the current–voltage (*I*-*V*) and capacitance-conductance-voltage (*C*-*G*/ ω -*V*) measurements.

Typical chemical cleaning processes were used to clean semiconductor wafers. That is the GaAs wafer was initially subjected to a degreasing process utilizing an organic solvent mixture (methyl alcohol, acetone, and trichloroethylene) for approximately five minutes. Subsequently, the wafer was subjected to a series of etching processes involving H_2SO_4 and H_2O_2 , 20 % HF, a solution of $6HNO_3:1HF:35H_2O$, and 20 % HF, and at each stage of the cleaning procedure, the wafer was rapidly cooled in deionized water.

Following the completion of the cleaning processes, the fabrication of Re/n-GaAs type Schottky devices with a native oxide layer of a fairly thin thickness (approximately 1.64 nm) commenced with the formation of an ohmic contact utilizing high-purity (99.999 %) Au metal. At this juncture, Au-type metal was thermally evaporated onto the rear surface of the n-GaAs wafer within a high vacuum system, and the formed sample was then subjected to annealing at 450 °C for approximately five minutes, a process that yielded low-resistivity ohmic contact. The ohmic contact thickness was set to be approximately 200 nm.

In the next stage, the GaAs/Au-type wafer was kept in a clean room for a while for the formation of the natural oxide layer. The native oxide layer, with an estimated thickness of approximately 1.64 nm, may act as a tunneling barrier for carriers under forward bias. However, due to its unintentional and disordered formation, it is also expected to host a significant number of localized defect states. These states contribute to the density of interface states (N_{ss}), which play a key role in the observed dielectric and frequency-dependent characteristics of the device.

In the final stage of production, Re with 99.9 % purity was coated onto the front side of the substrate using the Pulsed Laser Deposition (PLD) technique. Consequently, Schottky contacts with a diameter of 1.5 mm and a thickness of approximately 200 nm were produced.

Consequently, the fabrication process of the Re/n-GaAs type Schottky devices with a native oxide interlayer was completed. Still, more detailed information about production processes can be found in reference [31].

The devices are now ready to be characterized using *I*-*V* and *C*-*G*/ ω -*V* measurements. At this stage, the Hewlett-Packard impedance analyzer was employed to obtain *C*-*G*/ ω -*V* data at enough high frequency (1 MHz). The Keithley 2410 source meter was also used to obtain *I*-*V* data at room temperature to better understand the capacitance and dielectric behavior. The schematic diagram of the measurement system and fabrication processes of the MIS devices are provided in Fig. 1. As can be observed in the figure, the measurement was conducted in the cryostat to eliminate external effects and noise.

3. Results and discussion

Measurements of capacitance and conductance are essential for comprehending the electrical characteristics and efficacy of Schottky structures. These measurements are crucial for ascertaining parameters such as interface states, insulating layer properties, and carrier concentration. To appropriately examine these values, it is essential to account for the influence of series resistance (R_s). Series resistance can

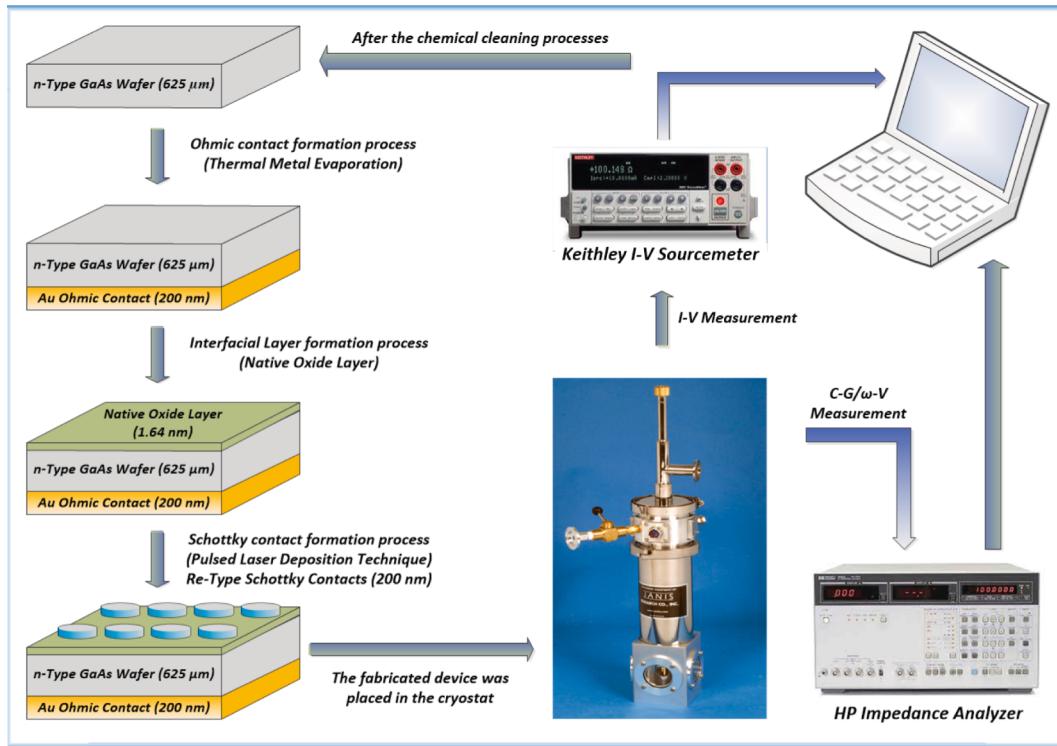


Fig. 1. Preparation and measurement processes of Re-based MIS-type Schottky devices.

markedly affect capacitance and conductance results, particularly in high-frequency tests, complicating the accurate assessment of device attributes. Consequently, the precise determination of R_s in Schottky structures facilitates a more dependable assessment of their electrical characteristics. In this study, the series resistance of Schottky structures was calculated with the equation given below (Eq. (1)).

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \quad (1)$$

In this equation, G_m indicates the measured conductance, C_m indicates the measured capacitance, and $\omega (=2\pi f)$ refers to the angular frequency. This method has enabled the exact estimation of series resistance, allowing for a more precise understanding of the electrical properties of Schottky structures. In this context, Fig. 2a illustrates the C -V and G -V

curves, while Fig. 2b represents the R_s -V curves.

The capacitance and conductance profiles presented in Fig. 2a were obtained using an impedance analyzer operating at 1 MHz frequency. As shown in the figure, the capacitance values gradually increase from the inversion region toward the depletion region, reaching a peak at approximately 0.26 V. Beyond this voltage, the capacitance values begin to decrease and eventually cross the zero axis at around +4.16 V, indicating the transition toward negative capacitance behavior. The emergence of NC and ND values at higher forward biases has generally been attributed to the inductive effect inherent in Schottky devices [37–39].

To clarify the voltage-dependent behavior, the operational regions can be delineated as follows: the inversion region spans approximately from -7 V to -1.5 V, where the capacitance remains relatively constant.

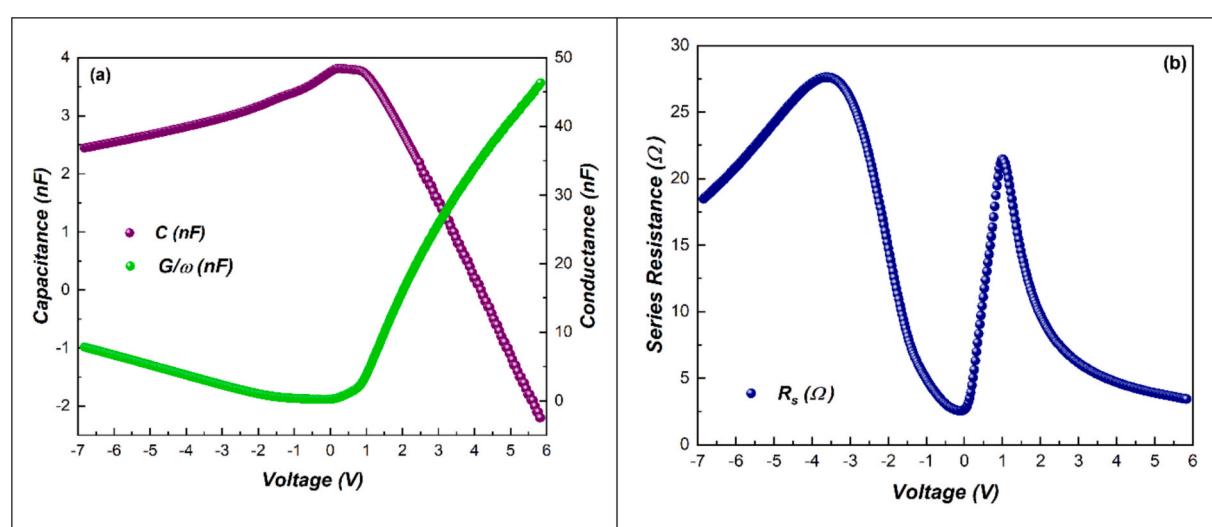


Fig. 2. C-G/ω-V and R_s -V characteristics of the Re-based MIS-type Schottky device.

The depletion region extends from about -1.5 V to $+0.26$ V, where the capacitance increases steadily. After the peak point ($+0.26$ V), the accumulation region begins and ultimately transitions into the negative capacitance regime beyond $+4.16$ V.

In parallel, it is observed that as the capacitance begins to take on negative values, the conductance increases rapidly, further reinforcing the notion of an inductive response at high forward biases. This phenomenon is likely related to the time-dependent response of dipole polarization-induced traps within the natural oxide layer between Re and n-GaAs when subjected to an AC signal [40–42]. Although this behavior is mainly related to inductive responses, it also has important consequences for device performance and stability. The onset of NC at higher voltages is attributed to the rhenium metal contact, which offers several advantages in terms of device functionality [37]. By enabling the positive capacitance to be maintained over a wider voltage range, it can both improve electrical stability and enable more precise control in applications where capacitance must remain constant. The expanded operational range also enhances the device's adaptability, particularly in high-voltage applications where positive capacitance protection is essential. In addition, the delayed transition to NC increases device reliability by avoiding early instabilities that are often encountered in similar systems. Although this transition at higher voltages requires caution in some sensitive applications, the operational stability and extended functional operating range make rhenium a highly advantageous contact material for advanced MIS structure designs [43]. Furthermore, the voltage dependence of the R_s was also examined to further assess the influence of the metal–semiconductor interface.

Fig. 2b illustrates the detection of two peaks in the R_s as a function of voltage, which is closely linked to the interface states trapped at the MS interface and the natural oxide layer formed between the metal and semiconductor. The first peak is typically ascribed to the specific arrangement of interface states and their trapping effects, whereas the second peak is a result of the influence of the insulating or native interfacial layer [44,45]. These peaks are caused by the voltage distribution throughout the device, where the interfacial layer and interface states' contributions increase in importance in particular voltage ranges. As the influence of the interface states and interfacial layers decreases at greater forward biases, R_s approaches its actual value, demonstrating that R_s is voltage-dependent and related to the diode's structural characteristics [46]. This value corresponds to approximately $3.36\ \Omega$ for the maximum bias, which corresponds to the voltage of 6 V.

Fig. 3 displays the C^2 -V characteristics of the fabricated Re-based MIS-type Schottky device. **Fig. 3a** shows the overall behavior across the full voltage range, while **Fig. 3b** provides a zoomed-in view within the linear region of the C^2 -V characteristics at negative biases, which is

used to extract key electrical parameters. Based on the linear region of the C^2 -V plot, the acceptor concentration (N_A), Fermi energy (E_F), maximum electric field (E_m), and depletion layer width (W_D), as well as barrier height (Φ_B) with the image force barrier lowering ($\Delta\Phi_B$), can be calculated using the following equations (Eqs. 2–8).

$$C^{-2} = \frac{2(V_D - kT/q - V)}{qN_A\epsilon_S\epsilon_0 A^2} \quad (2)$$

$$N_A = \frac{2}{q\epsilon_S\epsilon_0 A^2 \tan(\theta)} \quad (3)$$

$$E_F = \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right) \quad (4)$$

$$E_m = \sqrt{\frac{2qN_A V_0}{\epsilon_S\epsilon_0}} \quad (5)$$

$$W_D = \sqrt{\frac{2\epsilon_S\epsilon_0 V_0}{qN_A}} \quad (6)$$

$$\Phi_B = V_0 + \frac{kT}{q} + E_F - \Delta\Phi_B \quad (7)$$

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\epsilon_S\epsilon_0}} \quad (8)$$

In these expressions, ϵ_S represents the dielectric constant of the semiconductor, while ϵ_0 denotes the vacuum permittivity. The parameters V_0 and V_D correspond to the intercept voltage and the diffusion potential, respectively, where the diffusion potential is defined by the relation $V_D = V_0 + kT/q$.

Using the experimental results, the V_0 was found as 0.723 V, and the diffusion voltage V_D was 0.749 V. Besides, the doping concentration was calculated as $N_A = 2.68 \times 10^{18}$ cm $^{-3}$, and the E_F was found to be -0.047 eV, which is slightly below the intrinsic level, suggesting a degenerate doping condition near the interface. Although negative values for E_F can seem unphysical, they have also been observed and reported in previous studies, particularly in regions exhibiting strong interface Fermi-level pinning due to localized interface states or high interface-trap densities [47,48]. The E_m at the interface was calculated as 7.40×10^5 V/cm, and the W_D as 1.95×10^{-6} cm. Consequently, the Φ_B was evaluated to be approximately 0.611 eV.

It is worth noting that the calculated built-in potential is slightly higher than the Schottky barrier height. Although this may appear

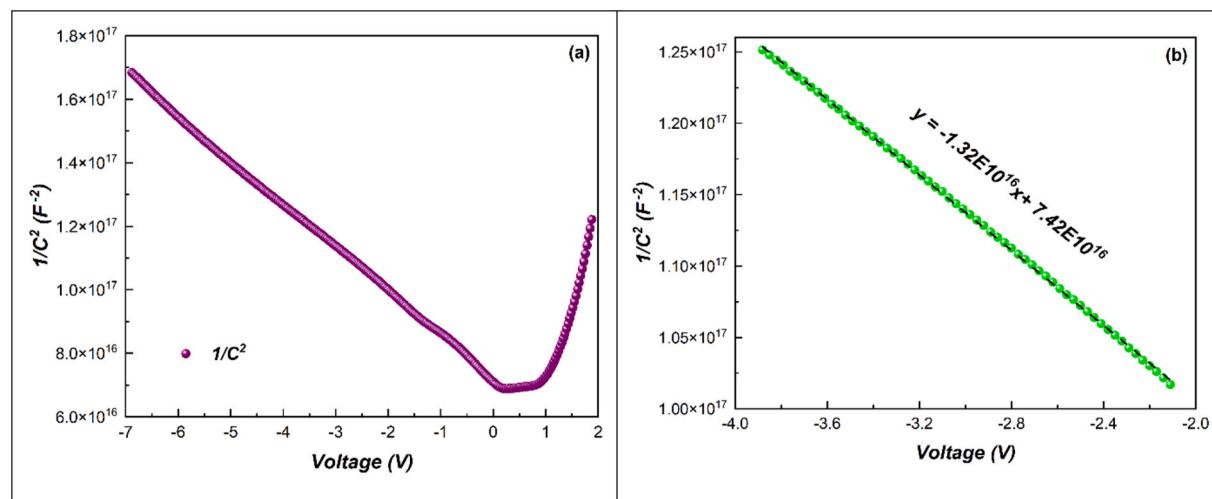


Fig. 3. $1/C^2$ -V characteristics of the Re-based MIS-type Schottky device.

counterintuitive under ideal assumptions, such a result can be attributed to several non-ideal effects, including Fermi-level pinning and the presence of a high density of interface states at the Re/n-GaAs interface. Furthermore, the high doping concentration ($\approx 2.68 \times 10^{18} \text{ cm}^{-3}$) may lead to band structure modifications that shift the equilibrium conditions. Discrepancies between V_0 and Φ_B values obtained from C-V analysis have been reported in similar GaAs-based MIS structures and are not necessarily indicative of calculation errors, but rather of the complex interfacial physics in such systems [49]. The finding that the Fermi energy level exhibits negative values lends further credence to the aforementioned information.

Furthermore, similar non-idealities have been reported in GaAs-based Schottky devices, where built-in potentials obtained from C-V analyses exceed the Schottky barrier heights measured via $I-V$ methods. For example, Hudait and Krupanidhi [49,50] found this behavior in Au/n-GaAs diodes, and Soylu et al. [49,50] observed a similar discrepancy in Al/p-GaAs devices. These differences were explained by interfacial oxide layers, high interface state densities, and spatial inhomogeneities in barrier heights.

To better illustrate the energy level distribution and interface effects in the fabricated structure, the schematic energy band diagram of the Re-based MIS device under thermal equilibrium is presented in Fig. 4. This figure supports the physical interpretation of the observed $V_0 > \Phi_B$ condition and highlights the role of interface states at the oxide/semiconductor junction.

The diagram given in Fig. 4 shows the alignment of key energy levels, including the Schottky barrier height, built-in potential, and Fermi level. The native oxide layer ($\approx 1.64 \text{ nm}$) contributes to the formation of interface states and dielectric dispersion. The observed condition ($V_0 > \Phi_B$) is consistent with the degenerate doping profile in n-GaAs.

The corrected capacitance (C_c) and corrected conductance (G_c) were calculated using the following equations (Eqs. 9–11) to more accurately analyze the dielectric and conductive response of the Re-based MIS device. These expressions allow the separation of the intrinsic dielectric properties from parasitic elements such as R_s , providing a more accurate interpretation of the measured admittance parameters.

$$C_c = \frac{((G_m)^2 + (\omega C_m)^2)C_m}{a^2 + (\omega C_m)^2} \quad (9)$$

$$G_c = \frac{((G_m)^2 + (\omega C_m)^2)a}{a^2 + (\omega C_m)^2} \quad (10)$$

$$a = G_m - ((G_m)^2 + (\omega C_m)^2)R_s \quad (11)$$

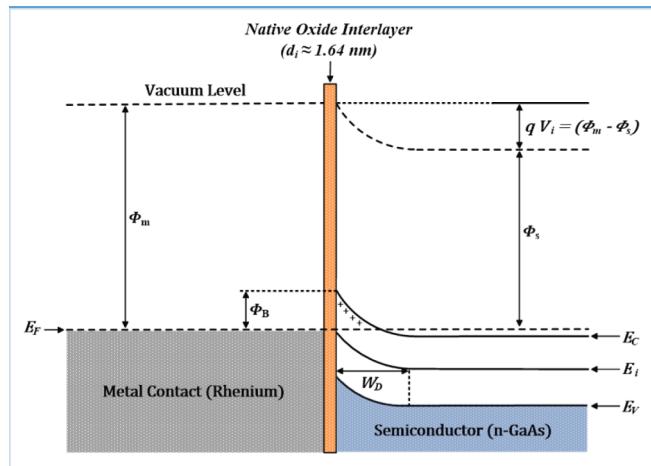


Fig. 4. Schematic energy band diagram of the Re-based MIS device under thermal equilibrium.

In the context of MIS devices with rhenium-type Schottky contacts, two distinct peaks in the G_c/ω values were observed as shown in Fig. 5. The first peak occurs at approximately -0.55 V and the second at around $+0.1 \text{ V}$. These peaks are attributed to interface states and their distribution within the energy bandgap of the semiconductor at the metal–semiconductor interface. The absence of these peaks in the measured conductance data is due to the influence of R_s , which suppresses the contribution of the N_{ss} and masks their visibility in raw measurements. Their presence suggests that load transfer occurs through these interface states, in agreement with similar findings documented in the literature. The first peak, located within the depletion region, shows that interface states facilitate charge transfer, and the second peak is probably associated with the density distribution of N_{ss} across two distinct energy levels within the bandgap of Si [51,52].

The significant influence of R_s noted in both depletion and accumulation zones underscores the necessity of accounting for voltage- and frequency-dependent electrical characteristics in these systems. Furthermore, it is imperative to acknowledge that the distinct peaks observed in the G_c/ω curve are attributable to fluctuations in carrier concentration, energy levels of interface states, and polarization effects. The effect of dipole polarization-induced traps of the natural oxide layer at the interface, causing a delay in the response to the AC signal, is also observed here. This situation is the cause of phase shift and energy dissipation in the dielectric response of the device. The occurrence of these peaks suggests the potential involvement of polarization processes in conjunction with stationary charge transfers [8,40,53,54].

On the other hand, with an increase in applied bias, the capacitance value diminishes, indicating the introduction of additional free carriers and their screening effect, which subsequently modifies the electrical properties of the device. The observations align with the experimental findings of this study, reinforcing the conclusion that the peaks in G_c/ω primarily result from physical and chemical interactions at the metal–semiconductor interface [55].

Fig. 6 shows the voltage-dependent variations of the real (ϵ') and imaginary (ϵ'') components of the complex dielectric constant (Fig. 6a), with the depiction of the complex dielectric plane ($\epsilon'-\epsilon''$) given in Fig. 6b for the manufactured Re-based MIS-type Schottky device. Fig. 6a shows that ϵ' exhibits anomalous behavior under forward bias, shifting from positive to negative values beyond approximately 4.16 V . This adverse response exhibited by the system to the applied field may be attributed to dynamic processes such as phase-delayed charge transfer, charge-trapped inductive interaction, and charge backflow [56,57]. Simultaneously, ϵ'' significantly increases, indicating heightened dielectric loss due to charge carrier hopping and interfacial polarization. These dielectric parameters were calculated using the complex dielectric constant ϵ^* , defined as follows (Eqs. 12–14). In these equations, Y^* corresponds to the complex admittance, C_0 ($=\epsilon_0 A/\delta_i$) is the geometrical capacitance, and G is the conductance.

$$\epsilon^* = \epsilon' - j\epsilon'' = \frac{Y^*}{j\omega C_0} = \frac{C}{C_0} - j \frac{G}{\omega C_0} \quad (12)$$

$$\epsilon' = \frac{C}{C_0} = \frac{C\delta_i}{\epsilon_0 A} \quad (13)$$

$$\epsilon'' = \frac{G}{\omega C_0} = \frac{G\delta_i}{\epsilon_0 \omega A} \quad (14)$$

On the other hand, Fig. 6b demonstrates the Cole-Cole plot, deviates from the ideal semicircular shape, showcasing an asymmetric and distorted arc with a tail extending into the negative ϵ' region. This asymmetric behavior indicates that multiple polarization mechanisms with distributed relaxation times are effective in the device instead of a single time constant [58,59]. The aberrant behavior, along with the observed loop creation, also indicates the existence of numerous relaxation processes and significant interfacial effects at the Re/n-GaAs interface. The

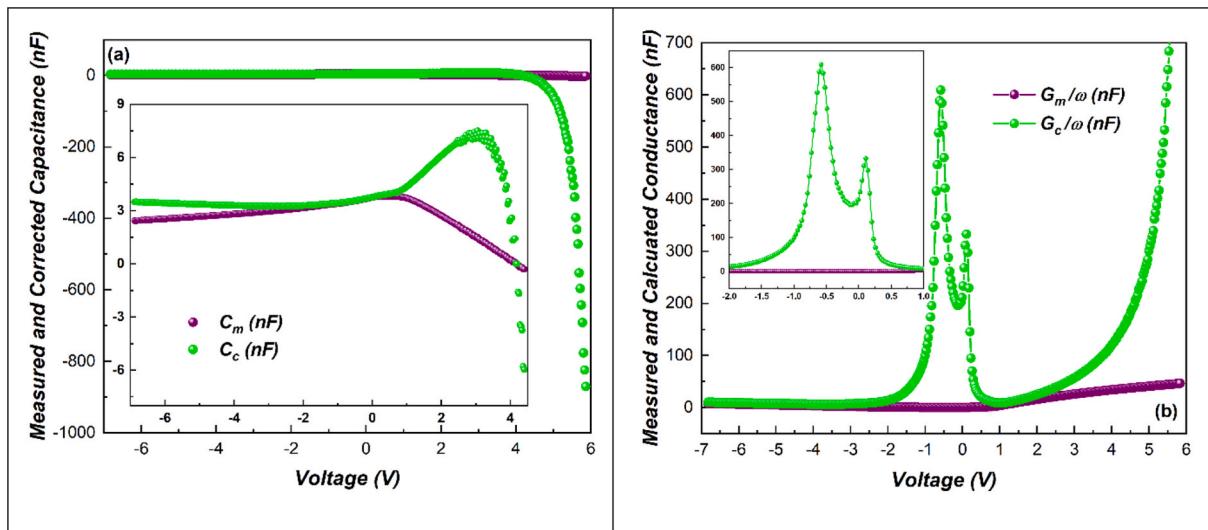


Fig. 5. C_m - C_c - V and G_m/ω - G_c/ω - V characteristics of the Re-based MIS-type Schottky device.

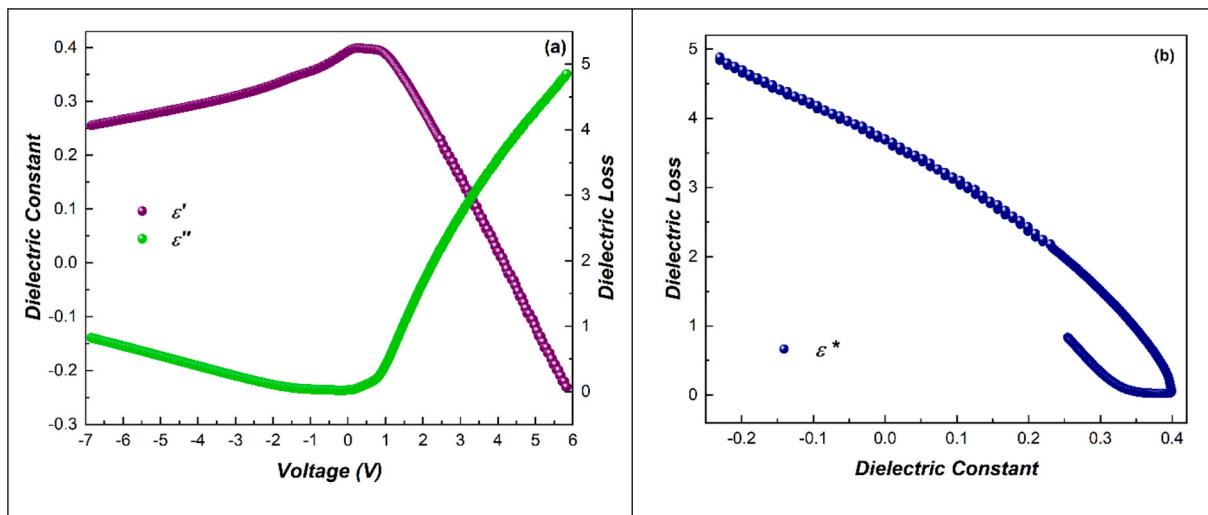


Fig. 6. ϵ' - ϵ'' - V and Cole-Cole (ϵ' - ϵ'') characteristics of the Re-based MIS-type Schottky device.

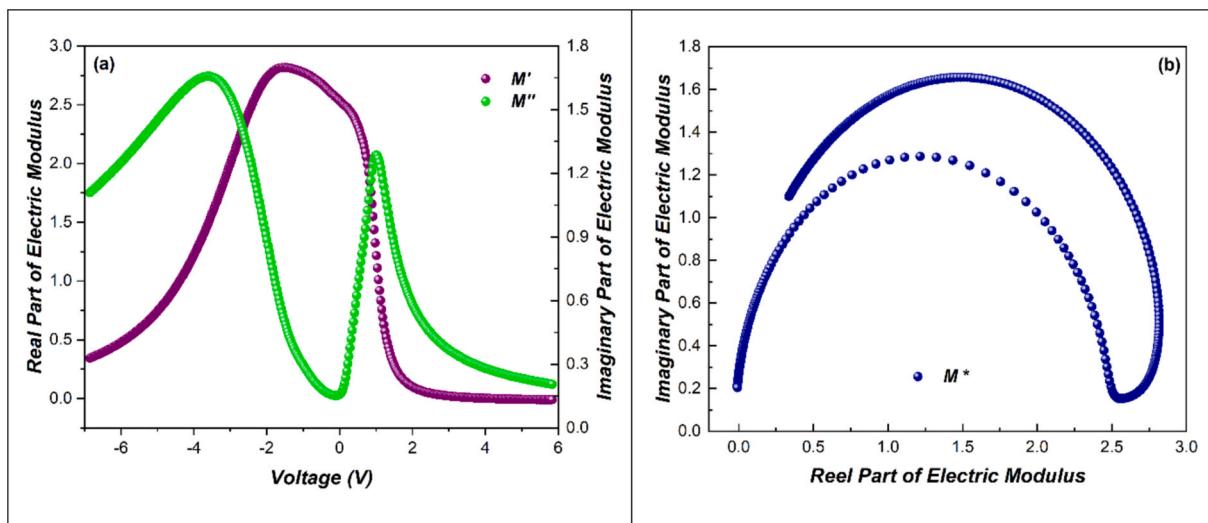


Fig. 7. Electric modulus and complex modulus characteristics of the Re-based MIS device.

presence of negative ϵ' values further substantiates the existence of negative capacitance and non-ideal dielectric polarization, affirming the intricate characteristics of dielectric behavior in the device.

The complex electric modulus M^* is mathematically defined as the reciprocal of the complex dielectric constant ϵ^* as given by Eq. (15) [60]. In this equation, Z^* is the complex impedance, and C_0 is the vacuum capacitance.

$$M^* = j\omega C_0 Z^* = \frac{1}{\epsilon^*} = \frac{\epsilon'}{\epsilon'^2 + \epsilon''^2} + j \frac{\epsilon''}{\epsilon'^2 + \epsilon''^2} = M' + jM'' \quad (15)$$

Fig. 7 shows the variation of the real (M') and imaginary (M'') parts of the electric modulus with applied voltage in **Fig. 7a** and the complex modulus plane ($M'-M''$) in **Fig. 7b** for the Re-based MIS-type Schottky device. The modulus formalism is particularly useful for suppressing electrode polarization effects and for identifying microscopic processes responsible for dielectric relaxation and conduction mechanisms [61]. Furthermore, **Fig. 7a** shows that the M' displays a singularly pronounced peak centered at approximately -1.6 V, due to voltage-dependent charge redistribution and localized relaxation effects within the depletion zone. Moreover, the imaginary component exhibits two distinct peaks: the first peak is observed at around -3.5 V, while the second peak is located near +1.0 V. These two separate peaks observed in M'' , just like in G_c/ω , once again show that interface traps polarized at different energy levels cause time-dependent charge transfer [62,63]. These peaks also represent discrete dielectric relaxation processes associated with interfacial polarization and various trap levels [64].

On the other hand, although the referenced study [60] utilizes the $Z-Z''$ impedance formalism, the observed depressed semicircular arc is conceptually analogous to the distorted $M'-M''$ plot in **Fig. 7b** of this work. Both representations reflect non-Debye-type relaxation behavior, characterized by a distribution of relaxation times and strong interfacial effects. The distorted $M'-M''$ arc observed in **Fig. 7b** reflects a non-Debye type relaxation mechanism, likely due to distributed relaxation times and interfacial polarization, as previously reported in polymer-based dielectric systems [65]. The maximum of the M^* arc occurs at about $M^* \approx 1.7$, further confirming the strong relaxation event at that bias.

To further interpret the device's dielectric response, equivalent circuit models frequently employed in the literature have been utilized [66]. The models shown in **Fig. 8** are considered in two different configurations, each representing the device behavior under distinct bias and frequency regimes. The extended model in **Fig. 8a** incorporates the oxide capacitance (C_{ox}), space charge capacitance (C_{sc}), interface state capacitance (C_{it}), and parallel resistance (R_{it}) that accounts for the response of interface traps. This arrangement accurately reflects the non-ideal dielectric behavior noted, especially at low frequencies and forward bias, when interface states play an important part in the total response. In contrast, the simplified circuit seen in **Fig. 8b**, including only C_{ox} and C_{sc} , represents the ideal situation that is more relevant under high-frequency settings where the impact of interfacial states is negligible. Especially at forward biases above +2 V, this transition, which becomes evident as the ϵ' tends to negative values, indicates that the inductive effect is activated and becomes dominant. It is for this reason that a series inductor is often incorporated into the circuit

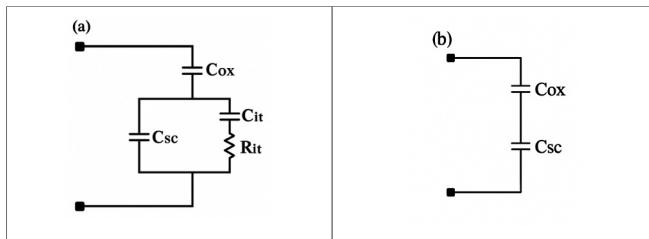


Fig. 8. (a) Extended and (b) simplified equivalent circuit models of the Schottky devices.

configuration of numerous devices, intending to underscore this concept [67]. This shift from capacitive to inductive behavior suggests reactive energy storage and further supports the use of the extended equivalent model for the accurate depiction of the device's electrical characteristics in this regime.

Fig. 9 illustrates the energy-related electrical responses of the Re/n-GaAs Schottky device using loss tangent ($\tan\delta$) and AC conductivity (σ_{ac}) plots. The loss tangent, which expresses the ratio of the dissipated to stored energy in the dielectric, is defined by Eq. (16). Here, ϵ_s and ϵ_∞ are the static and optical dielectric constants, respectively, and τ is the relaxation time.

$$\tan\delta = \frac{\epsilon''}{\epsilon'} = \frac{\epsilon_s - \epsilon_\infty}{\epsilon_s + \epsilon_\infty \omega^2 \tau^2} \omega \tau \quad (16)$$

The sharp spike observed in $\tan\delta$ near +4.1 V, as shown in **Fig. 9a**, indicates a strong dipolar relaxation condition, in agreement with similar peak behavior attributed to interface states and interfacial polarization in MIS-type devices [68]. In addition, this observed sharp spike can be considered as an indication that the traps at the interface operate close to the resonance condition and the electric field is terminated with maximum energy loss in this region [40,57].

On the other hand, the σ_{ac} can be calculated from the dielectric loss using Eq. (17). In this equation, d represents the thickness of the oxide layer, A is the contact area, and ϵ_0 is the vacuum permittivity. The parameters ω and $\tan\delta$ have been previously defined.

$$\sigma_{ac} = \left(\frac{d}{A} \right) \omega C \tan\delta = \epsilon'' \omega \epsilon_0 \quad (17)$$

As seen in the right-hand plot (**Fig. 9b**), σ_{ac} remains relatively low and stable under reverse bias conditions and then increases rapidly above +1.5 V, reaching values as high as 2.8×10^{-6} S/cm at +6 V. This increase reflects field-induced conductivity enhancement and supports the formation of additional charge transport channels, such as via interface states or trap-assisted conduction mechanisms [69].

Fig. 10 shows the variation of the real (Z') and imaginary (Z'') components of complex impedance in relation to the applied voltage (**Fig. 10a**), accompanied by the matching Nyquist plot in the complex plane illustrating Z (**Fig. 10b**).

The real component Z' indicates the resistive characteristics of the device, whereas the imaginary component Z'' is primarily linked to capacitive characteristics and dielectric relaxation. Z' and Z'' reach their peak values at around -3.6 V and -1.5 V, respectively. The prominent peaks are ascribed to voltage-dependent relaxation processes and charge-trapping phenomena within the device, perhaps due to interfacial effects at the metal-semiconductor junction [70]. Moreover, the occurrence of these peaks in Z' and Z'' at distinct voltage values indicates that the interface charges and potential barrier change with voltage. In summary, the evidence suggests that the charge storage and transport mechanisms of the device are subject to alteration through the implementation of voltage control [57,71]. As is well documented in the extant literature, the complex impedance can be expressed by Eq. (18).

$$Z^*(\omega) = Z'(\omega) - jZ''(\omega) = \frac{1}{j\omega C_0 \epsilon^*(\omega)} = \frac{\epsilon''}{\omega C_0 [\epsilon'^2 + \epsilon''^2]} - j \frac{\epsilon'}{\omega C_0 [\epsilon'^2 + \epsilon''^2]} \quad (18)$$

As can be seen in **Fig. 10b**, the Nyquist plot shows a depressed and asymmetric semicircular arc, indicating deviation from ideal Debye behavior and the presence of multiple relaxation processes within the Re/n-GaAs structure. The large arc diameter reflects a significant charge accumulation or contact resistance at the metal-semiconductor interface, whereas the low-frequency tail suggests slow charge carrier dynamics and possible barrier effects [70]. It can also be said that it shows that localized charge accumulation at the interface and time-resolved dipole relaxation processes are effective together [71,72].

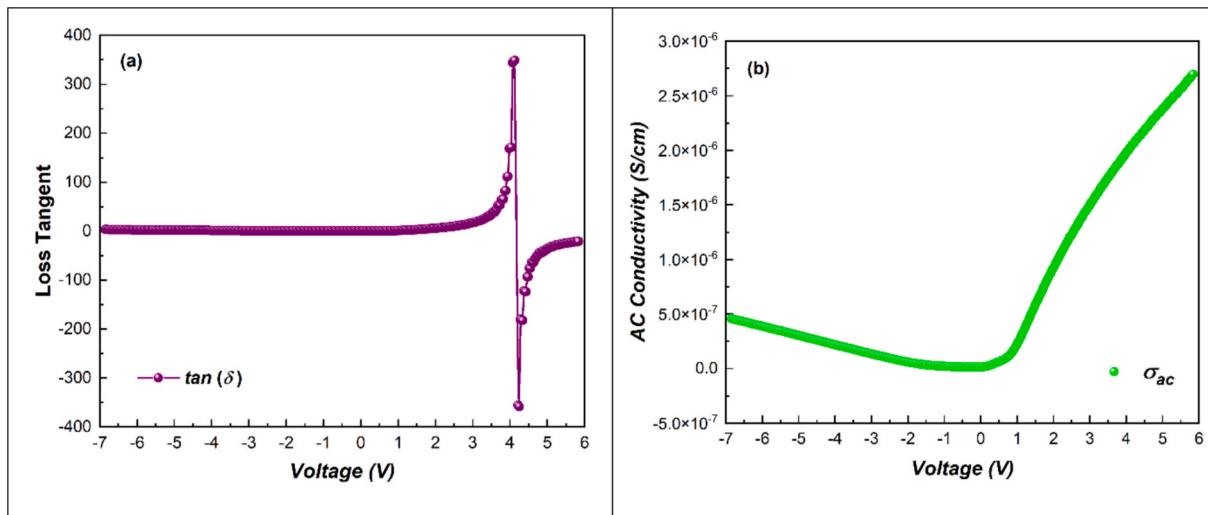


Fig. 9. Loss tangent and AC conductivity characteristics of the Re-based MIS device.

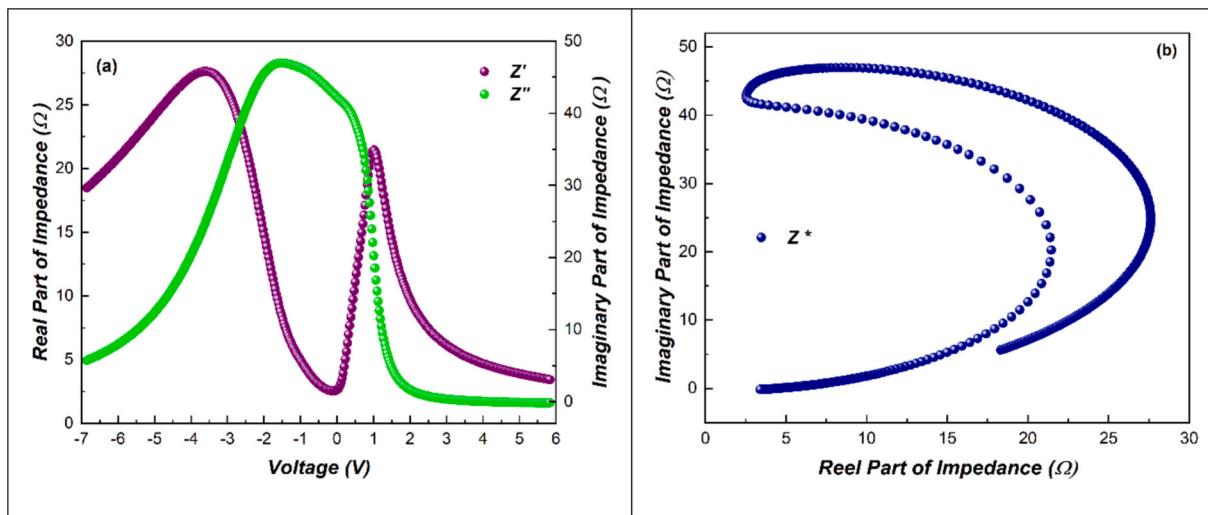


Fig. 10. Impedance and complex impedance characteristics of the Re-based MIS device.

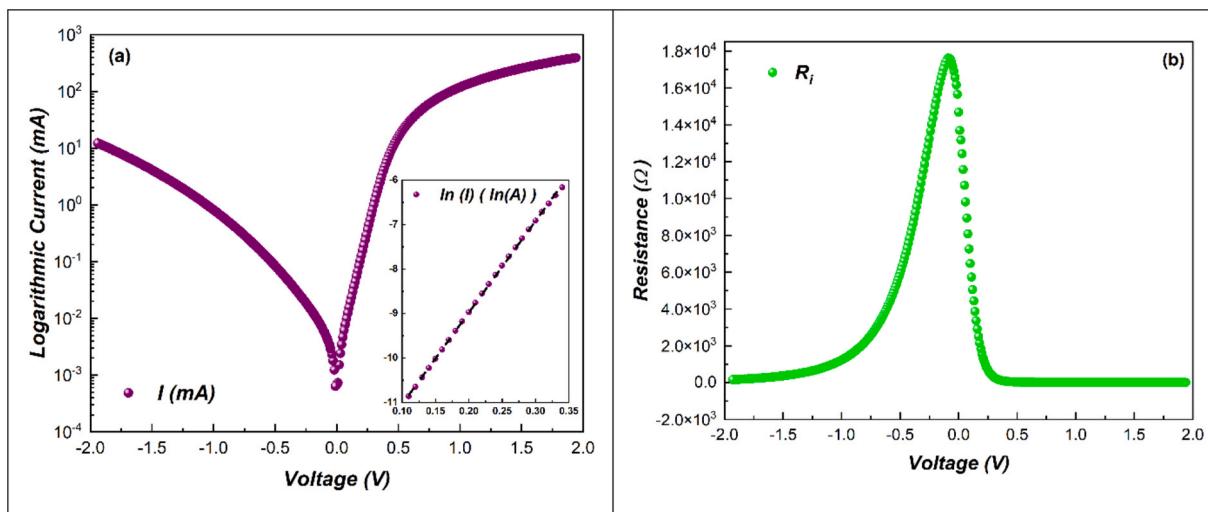


Fig. 11. Current-voltage and internal resistance characteristics of the Re-based MIS device.

Fig. 11 illustrates the logarithmic current–voltage (I - V) characteristics and the dynamic resistance behavior of the Re-based MIS-type Schottky device. As seen in **Fig. 10b**, the dynamic resistance (R_i) reaches its peak value near zero bias and decreases significantly under both forward and reverse bias conditions. At higher forward voltages, the R_i values become nearly constant and converge toward the series resistance R_s , indicating that R_i in this regime effectively reflects the actual series resistance of the device [73]. This behavior further supports the conclusion that the back Au contact is ohmic in nature. The symmetric reverse bias response and the stable low dynamic resistance under forward bias, as shown in **Fig. 11b**, confirm that the back contact does not impede current flow. Additionally, the linear trend observed in the $\ln(I)$ - V plot (**Fig. 11a**, inset) aligns with thermionic emission theory, further validating the ohmic character of the contact. The extracted values of series resistance ($R_s \approx 4.89 \Omega$) and shunt resistance ($R_{sh} \approx 143 \Omega$) also support the quality and reliability of the back contact.

On the other hand, analyses show that the series resistance extracted from I to V measurements is approximately 4.89Ω , while their value obtained from C - V characteristics is around 3.36Ω . The close agreement between these two results confirms the consistency of the measurement methods. However, since the capacitance–voltage method provides higher sensitivity and resolution, especially at low frequencies, it is considered more reliable for precise extraction of the series resistance in Schottky structures [73].

The behavior as shown in **Fig. 11a** reflects the transition from the non-linear region to the exponential conduction region in the forward bias, where the current rapidly increases with the applied voltage as the device enters its typical forward conduction mode. The saturation current (I_0) and the ideality factor (n) can be calculated from the linear region of the semi-logarithmic I - V graph employing thermionic emission theory, yielding $I_0 \approx 2.05 \times 10^{-6}$ and $n \approx 1,876$. The research also determined the zero-bias barrier height (Φ_{B0}) to be around 0.584 eV. Compared to the barrier height obtained from the C - V analysis (0.611 eV), a discrepancy of about 27 meV was observed. This variation is primarily attributed to the existence of interface states and the voltage-dependent properties of the depletion region, which frequently cause the C - V approach to produce significantly higher barrier height values compared to the I - V method. On the other hand, the difference in series resistance values derived from I to V and C - V measurements is mainly due to the enhanced sensitivity and resolution of the C - V technique, making it more adept at identifying parasitic and interfacial effects than the I - V method.

In addition to the forward conduction characteristics, the I - V behavior in reverse bias exhibits a rapidly increasing current at higher reverse bias voltages. This behavior can be attributed to trap-assisted tunneling mechanisms and field-enhanced emission processes facilitated by the native oxide layer (≈ 1.64 nm) at the Re/n-GaAs interface. The naturally formed oxide is structurally non-uniform and may host a significant density of defect-related interface states and localized trap centers. Under strong reverse bias, these centers can provide alternate conduction paths by enabling tunneling or hopping transport. Furthermore, local barrier thinning and potential field concentration at weak spots within the oxide can lead to increased leakage, consistent with the observed current rise. These phenomena are commonly observed in MIS structures with thin or native oxide layers and reflect the interfacial nature of the device, rather than indicating electrical degradation.

The collective results obtained from electrical and dielectric measurements, including I - V , C - V , G/ω - V , impedance, modulus, and loss analyses, consistently demonstrate the influence of the native oxide layer and rhenium contact on the charge transport and polarization dynamics of the Re/n-GaAs MIS device. The observed negative capacitance and dielectric behaviors under forward bias, along with distinct interface-state-related peaks and the shift from capacitive to inductive response, provide strong evidence for field-sensitive interfacial phenomena. The extracted electrical parameters (Φ_B , V_0 , W_D , N_A , E_F , as well as R_s and R_{sh}) further confirm the presence of degenerate doping

conditions and support the hypothesis of Fermi-level elevation above the conduction band minimum. The rapid increase in reverse current and the asymmetric Nyquist response are consistent with trap-assisted tunneling and interface-driven leakage. Together, these findings reveal that the incorporation of rhenium metal and the presence of a native oxide interface play a critical role in shaping the dielectric and conduction characteristics of the device, validating its potential for high-frequency and non-ideal interface engineering applications.

4. Conclusion

In this study, the electrical and dielectric properties of Re/n-GaAs MIS-type Schottky devices fabricated by the PLD method have been extensively investigated. All measurements were carried out at a frequency of 1 MHz to reveal the frequency-dependent behavior of the structure under different bias conditions. The experimental findings provide significant evidence for the presence of significant NC and ND phenomena, especially in the forward bias region. C - V and G/ω - V analyses showed two distinct peaks in the G/ω profile around -0.55 V and $+0.1$ V. These peaks are associated with interfacial states with different energy levels within the GaAs bandgap. At forward biases above 4.16 V, a transition from capacitive to inductive behavior is observed, with the C and ϵ' tending towards negative values. This indicates polarisation reversal and reactive energy storage effects. The M' and M'' analyses also supported these findings, showing characteristic peak structures that indicate non-Debye-type dielectric relaxation mechanisms. While two distinct peaks around -3.6 V and $+1.0$ V were detected in the M'' component, a single peak around -1.5 V was observed in the M' component. This indicates that more than one charge relaxation mechanism and interfacial polarisation effects are active in the structure. Complex impedance analyses and Nyquist diagrams exhibited depressed and asymmetric half-circle structures showing deviations from the ideal Debye behavior. This suggests that multiple relaxation processes, interfacial irregularities, and potential barrier effects play an important role in device conductivity. Furthermore, the AC conductivity increase observed after $+1.5$ V supports the formation of trap-assisted carrier transitions and interfacial-induced carrier channels. Quantitative parameters such as built-in potential ($V_0 = 0.723$ V), barrier height ($\Phi_B = 0.611$ eV), and series resistance ($R_s \approx 4.89 \Omega$ (I - V), 3.36Ω (C - V)) were consistently obtained between the methods used. This demonstrates the reliability of the measurement and analysis techniques. The R_i reached a peak near zero bias and stabilized at higher voltages, aligning with the series resistance values. The combined evaluation of the simplified and extended equivalent circuit models showed that the extended model, which includes interfacial effects, provides a more accurate representation, especially in the high-frequency and forward bias regions. Overall, this study reveals that the integration of Re metal into an MIS-type structure produces significant changes in the electrical/dielectric performance of the device and provides strong control over the interfacial polarisation and relaxation dynamics. To put it briefly, the results show that Re-based Schottky devices have the potential for high-frequency, low-power, and advanced functional electronic applications.

CRediT authorship contribution statement

Mehmet İzzeddin Güler: Writing – original draft, Visualization, Investigation, Formal analysis, Conceptualization. **Ahmet Kaymaz:** Writing – review & editing, Visualization, Validation, Investigation, Conceptualization. **Esra Evcin Baydilli:** Writing – review & editing, Visualization, Methodology, Investigation. **Haziret Durmuş:** Writing – review & editing, Methodology. **Şemsettin Altındal:** Writing – review & editing, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial

interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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