Carrier transport in graphite/Si_3N_4-nanobelt/PtIr Schottky barrier diodes

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(Received 10 August 2014; accepted 3 November 2014; published online 11 November 2014)

Understanding the roles of contacts and interfaces between metals and semiconductors is critically important for exploring nanostructure-based nanodevices. The present study shed some light on the dominated mechanism of size-dependent carrier transfer in the Schottky barrier diodes configured by the Pt-Ir/Si_3N_4-nanobelt/graphite (metal-semiconductor-metal (MSM)) sandwiched structure via a conductive atomic force microscopy using nanobelts with various thicknesses. The observed *I-V* behaviors suggested that the charge transports under the low and high biases were dominated by the reverse-biased Schottky barrier and space-charge-limited current (SCLC), respectively. The intermediate region between the low and high biases presented the transition between the Ohmic and SCLC behaviors, in which the ≡Si and =N dangling bonds acted as the defects within the Si_3N_4 nanobelt surface are predominant in the charge transfer. © *2014 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4901821]

Silicon nitride (Si_3N_4), with large bandgap (5.1 eV) and outstanding physical and chemical properties has attracted considerable attention in electronic devices and optoelectronic devices due to its compelling applications in high temperature (>200 °C), high power and high-frequency harsh environments, in which the Si and GaAs semiconductors cannot be qualified.[1–7] For example, thin layers of crystalline Si_3N_4 bulks for insulation were normally used for surface encapsulation and packaging in the integrated circuits.[8] As compared to their bulk counterparts, Si_3N_4 nanostructures could exhibit fascinating physical[9] and electronic properties with the promising applications in the opto/electronic nanodevices.[10–14] For exploring the semiconductor nanodevices, the MSM sandwiched structures are often utilized. Thus, to meet the emergency in realizing Si_3N_4 nanostructure-based nanodevices, the foundation understanding is desired for concerning on the current transport within the Si_3N_4-metal interface of the MSM structures as well as the details of current injection from a metal electrode into the one-dimensional (1D) Si_3N_4 nanostructures.

However, up to date, regardless of much progress developed for the growth of Si_3N_4 nanostructures such as nanowires and nanobelts,[11,15–19] there were few reports on the electrical transport in Si_3N_4 nanostructures, which remain as an obstacle for the exploration of Si_3N_4 nanodevices. In this study, the *I-V* characteristics of a set of configured Schottky barrier diodes, with Si_3N_4 nanobelts ranged in 50–200 nm thicknesses, were investigated by conductive atomic force microscopy (C-AFM). We focused on following issues: (i) What the role of the trap level played in the energy band of Si_3N_4 nanobelt at room temperature, and how the electronic properties of Si_3N_4 nanobelt influenced by its thickness; (ii) What is the conduction mechanism for electron transfer in the 1D Si_3N_4 nanobelt under negative and positive bias; (iii) What is the effect of the existence of defect types, and their distribute location in the Si_3N_4 nanobelt.

α-Si_3N_4 nanobelts were synthesized via pyrolysis of a polyaluminasilazane precursor assisted by the Al catalysts, which were reported in our previous work.[20] For measuring the *I-V* properties, a drop of alcohol solution containing the α-Si_3N_4 nanobelts was dripped onto a metallic highly oriented pyrolytic graphite (HOPG) substrate, followed by being dried in the vacuum oven at 60 °C. The nanobelts were characterized using field emission scanning electron microscopy (FESEM, S-4800, Hitachi, Japan). The *I-V* measurements were performed using a conductive atomic force microscopy (C-AFM, Nanoscope V, Veeco, USA) with Pt/Ir-coated tips (force constant: 0.2 N/m) at room temperature.

Figures 1(a)–1(b) show the typical SEM images of the as-synthesized α-Si_3N_4 nanobelts under different magnifications, suggesting the large-scale growth of the nanobelts with typical lengths in the range of several to hundreds of micrometers. According to the TEM analyses,[20] the Si_3N_4 nanobelts are highly qualified with a single-crystalline nature.

Figure 2(a) presents the schematic diagram of the experimental set up. The AFM tip is fixed onto the top surface of the nanobelt lying on the HOPG substrate, leading to the formation of the diodes configured by Pt-Ir/Si_3N_4 nanobelt/graphite metal-semiconductor-metal (MSM) sandwiched structures. Figures 2(b)–2(d) display the typical AFM images of the given single nanobelts with different thicknesses of 50, 100, and 200 nm, respectively. Their corresponding line profiles of the heights are shown in Figure 2(e). It seems that all the three nanobelts possess very smooth surfaces with a uniform width along their length direction. Figure 2(f) shows the *I-V* plots of the MSM structure constructed by different thicknesses of the nanobelts under the fixed loading force of

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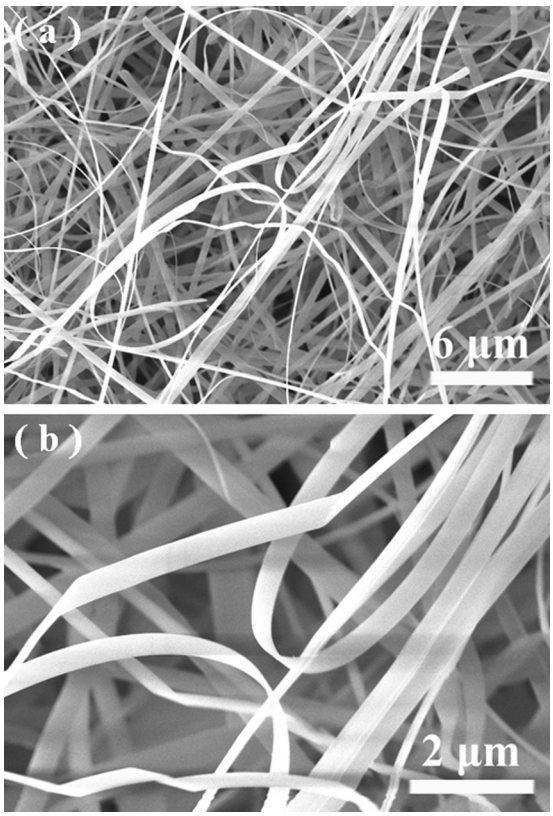

FIG. 1. (a) and (b) Typical SEM images of the α-Si_3N_4 nanobelts under different magnifications.

100 nN (the pressure is *ca.* 8.3×10^9 N/M^2 at the contact point), suggesting that the variations of the current are clearly dependent on the Si_3N_4 nanobelt thicknesses. In the present work, the contact between the tip and nanobelt can be regarded as point contact, while the one between the nanobelt and graphite substrate is surface contact due to the nanobelt lying on the graphite surface. When a bias is applied, the carrier will flow along the AFM tip, the nanobelt, and the graphite substrate. That is to say, the carrier transport is mainly through the transverse direction of the nanobelt, due to the point contact with the max diameter of 20 nm (i.e., the diameter of the AFM tip).[21] The change of the current distribution along the width direction can be negligible if the width is much more than 20 nm. In current case, the widths of the nanobelts are in the range of 400 ~ 600 nm, which are far greater than the diameter of the tip sized in 20 nm. Therefore, the variety in the electrical properties is mainly dependent on the thicknesses, regardless of various widths of the nanobelts. It seems that the currents of the nanobelts with the thicknesses of 50 and 100 nm constantly stay at −10 nA ranged from −4 to +4 V (Fig. 2(f)), which can be attributed to the leak current resulted from the surface state. It is known that there are abundant surface defects within the nanobelts. Such defects play an important role on determining the OFF current in the cut-off region of the constructed diode, which is named as the leak current. As compared to the nanobelt with the width of 200 nm, the counterparts with the widths of 50 and 100 nm have larger surface areas with richer surface states for adsorbing more oxygen molecules from air, which would cause the capture of free electrons on the nanobelt's surface, leading to the formation of the leak current. The distinct rectifying behavior with a large voltage range (0 ~ 6 eV) can be observed once the thicknesses of the nanobelts are below 100 nm. At the same applied negative bias, the absolute value of negative current is found to increase quickly with the decrease of the nanobelt thickness. The positive current density also shows the similar behaviors. Their corresponding rectifying ratios show a function of the nanobelt thicknesses, which are *ca.* 456 at ±7.26 V and 147 at ±7.3 V, respectively. In addition, the turn-on voltages of the MSM systems with the belt thicknesses of 50, 100, and 200 nm are of −5.4, −6, and −7.5 V, respectively, clarifying that they are also dependent on the nanobelt thicknesses. The experimental results suggest

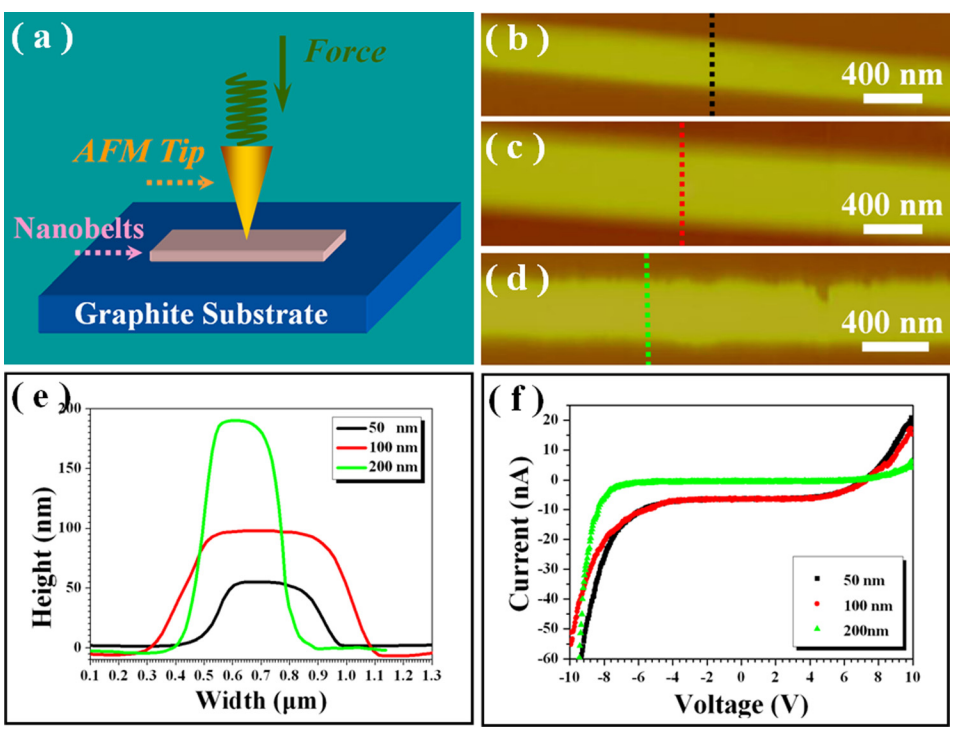

FIG. 2. (a) The experimental set up for the *I-V* characterization of the Schottky barrier diodes configured by the Pt-Ir/Si_3N_4 nanobelt/graphite structure. (b)–(d) Typical AFM images of the three used Si_3N_4 nanobelts. (e) The height data of the nanobelts with thicknesses of 50, 100, and 200 nm, respectively. (f) The *I-V* characterizations of the diodes configured by the nanobelts with thicknesses of 50, 100, and 200 nm, respectively.

that the thicknesses of the Si_3N_4 nanobelt play a determined role on the properties of the diodes.

To investigate the contact and transport mechanism in the MSM structure, following analysis was conducted. Assuming that there are no defects or trapped charges at the interface between the nanobelt and the two electrodes, the band diagrams for the diode at thermal equilibrium can be used for explaining the formed mechanism of the Schottky barrier before and after the contact between the AFM tip and the nanobelts under a positive bias at the graphite side, which are schematically shown in Figs. 3(a) and 3(b), respectively. The work functions of Si_3N_4 semiconductor, graphite, and Pt/Ir AFM tip are about 4.75 eV, 4.40 eV,[22] and 5.10 eV,[23] respectively. Thus, the Si_3N_4-graphite contact is Schottky with a barrier height of 0.35 eV at the bottom, and the Pt/Ir-Si_3N_4 contact should be Schottky with a barrier height of 0.35 eV at the top surface. Thus, the Pt/Ir-Si_3N_4-graphite contact is a typical metal-semiconductor-metal (M-S-M) architecture with two opposite Schottky barriers, which leads to the formation of a back-to-back schottky diode separated by the Si_3N_4 nanobelt. Actually, the nonlinearity and asymmetric behaviors of the *I-V* curves together with the high turn-on voltages in Fig. 2(f) can directly disclose that the AFM-tip/Si_3N_4 junction belongs to a Schottky contact. As shown in Fig. 3(b), when a negative bias is applied to the diode at the AFM-tip side, the electron will flow along the AFM tip, through the nanobelt's conductive band, and out of the graphite substrate. Due to the formation of graphite/Si_3N_4-nanobelt/PtIr schottky barrier diode, the increase of current under the negative bias can be observed. However, the current cannot be effectively injected into the AFM-tip from the nanobelt side under the positive bias, which could be attributed to the built-in field at the interface.

It is well known that the Schottky barrier can be strongly affected by the surface and trap states, which, in turn, plays a profound effect on the electrical transport in the 1D-nanostructure based nanodevices. According to our previous work on the photoluminescence (PL) properties of currently used α-Si_3N_4 nanobelts,[20] it could be confirmed that abundant defects should act as the luminescence centers within the nanobelt. There are mainly four types of defects in the Si_3N_4 based material: Si–Si and N–N bonds, and ≡Si and =N dangling bonds, respectively.[7] The ≡Si dangling bonds can further form a donor level ($\equiv Si^-$) and acceptor level ($\equiv Si^0$), which participate in the radiative transition giving rise to the broad emission.[24,25] Thus, based on the literature reports,[7,26] the following conclusions can be drawn: (i) The PL peaks of Si_3N_4 nanobelts centered at 1.9 eV, 2.3 eV, and 3.1 eV (Ref. 20) can be attributed to the electronic transition of $E_c \rightarrow \equiv Si^-$, $\equiv Si^0 \rightarrow =N$ and $\equiv Si^0 \rightarrow E_v$, respectively, as shown in Fig. 3(c). (ii) The predominant defects in the Si_3N_4 nanobelt are consisted as ≡Si and =N. In addition, the Fermi level of surface state (~1.7 eV) cannot be clearly observed in our PL peak. In other words, the number of defect states per area is not large

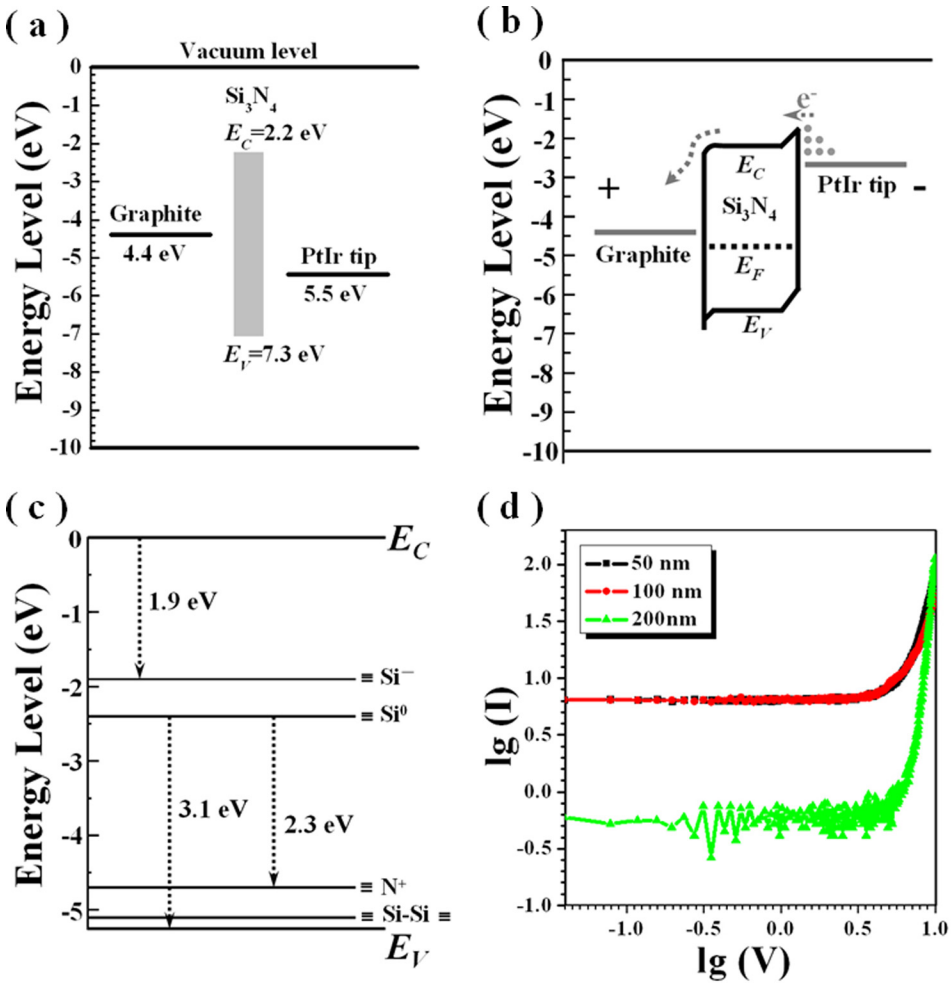

FIG. 3. (a) Energy band diagrams of Graphite, Si_3N_4, and PtIr tip. E_C and E_V represent the conduction band and valence band of Si_3N_4, respectively. (b) Energy band diagrams of the fabricated diodes under a positive bias at the graphite side. (c) Model for photoluminescence behaviors within the α-Si_3N_4 nanobelts. (d) $\lg(|I|)$-$\lg(|V|)$ curves of the diodes under negative biases.

enough to totally pin the Fermi level of the semiconductor to surface potential. Herein, the influence of the surface state on the current can be ignored due to its small contribution.

It has been reported that three distinct *I-V* characteristics with the typical features of symmetric, rectifying, and linear can be often observed in the electronic nanodevices constructed by 1D semiconductor nanostructures.[27] However, the *I-V* curves shown in Fig. 2(f) are neither linear (e.g., the diodes with nanobelts sized in 50 and 100 nm in thicknesses) nor rectifying (e.g., the diode with nanobelt sized in 200 nm in thickness). They all exhibit unsymmetric and nonlinear *I-V* behaviors. In general, the classic nonlinear conduction could be attributed to following typical mechanisms, such as space-charge-limited current (SCLC), Schottky emission, Poole-Frenkel (PF) emission (field-assisted carrier excitation from centers within the bandgap), and Fowler-Nordheim (FN) quantum tunneling. The FN tunneling emission can be first ruled out due to the given belt thicknesses ranged in 50–200 nm. The other two conduction models (i.e., PF and Schottky emissions) can be characterized by linear $\ln(I/V) \sim V^{1/2}$ for PF[28–30] and linear $\ln(I) \sim V^{1/2}$ for Schottky emission. No straight lines in both $\ln \sim V^{1/2}$ curves can be obtained, indicating that these two mechanisms can also be excluded. It has been pointed out that the space charge limited transport always occurs in the undoped wide bandgap semiconductors, in which the density of charge carriers at equilibrium is vanishingly small. Figure 3(d) exhibits the plots of the negative branch of the forward curve (from 0 to −10 V) in Fig. 2(f) as a $\lg(|I|)$-$\lg(|V|)$ curve. There are three regions in these logarithmic curves, namely, two linear change regions for the small (<turn on voltage) and high voltage (>|−8 V| for most curves), as well as a nonlinear change one within the intermediate voltages, which agree well on the typical SCLC features.[31,32] Due to the current *I* being dependent on the nanobelt thicknesses, the thinner samples can carry a considerable higher current than the thicker one at the similar voltage level. According to the SCLC theory, in the voltage region lower than the turn-on voltage where *I* is proportional to *V* and Ohm's law is obeyed, the field density *J* follows the relation as

$$J = \mathrm{e} n_0 \mu \frac{\mathrm{V}}{d}, \tag{1}$$

where n_0 is the concentration of thermally generated electrons in the conduction band, μ is the mobility, *V* is the applied voltage, and *d* is the Si_3N_4 thickness, respectively. Due to the Si_3N_4 belongs to the wide bandgap semiconductor with the energy gap of 5.1 eV, the intrinsic carrier concentration in our undoped nanobelt is very low, and can contribute little during the conducting process. In other words, the current passing through the system is very small and the total voltage is distributed mainly on the Schottky barriers. At the larger voltages region (i.e., >8 V), the current obeys the following equation:[33]

$$J = \mathrm{e}\mu N_C \left(\frac{\varepsilon}{eN_0 kT_t}\right) \frac{V^{l+1}}{d^{2l+1}}, \tag{2}$$

where N_c is the effective density of states in the conduction band, ε is the permittivity, $l=n-1$ (*n* is the power-law exponent), N_0 is the trap density per unit energy range at the conduction band edge, and T_t is a temperature parameter characterizing the distribution. In this region, the large current can be attributed to the increase of the free electron concentrations, due to the carrier injection greatly exceeding the equilibrium one in the nanobelt.

According to the SCLC mechanism, the free electrons contribute small to the current transport, due to the fact that the carrier injection greatly exceeds the equilibrium concentration in the nanobelt. The intermediate region represents the transition between Ohmic and SCLC behaviors, which could provide the information about the trap distribution within the nanobelt. For pure semiconductor in nanoscale with high quality, the bulk density of traps is very low, and the total number of traps at the nanobelt surface can be comparable or even larger than the total amount of bulk traps. Thus, the charge trapped at the surface strongly determines the measured current. Combining with the PL results,[20] the electron traps formed by defects in nanobelt mainly origin from ≡Si and =N dangling bonds, which exist mainly on the surface of the nanobelt. Therefore, in the intermediate region, four possible trap levels and five transfer processes can contribute to the current: (i) The direct tunneling of electrons from trap states located in $\equiv Si^-$ level near the conduction band of the Si_3N_4; (ii) The direct tunneling of holes from trap states located in $\equiv Si^0$ level; (iii) The direct tunneling of holes from trap states located in =N level; (iv) The direct tunneling of holes from trap states located in ≡Si-Si≡ level; (v) FN tunneling of holes in the valence band. Considering that these trap states can be almost filled with electrons at thermal equilibrium during the current injection from the AFM tip to the nanobelt under a negative voltage applied to the metal electrode, and these states could be filled by the field induced electrons, there is no current contribution from hole-based charge transfer (mutual annihilation due to the hole contacts with electrons in the trap state). Thus, the transfer processes (ii)–(v) can be excluded. At the same time, direct tunneling can be suppressed due to the filling-up of the electrons in the trap states under thermal equilibrium. Herein, it can be considered that trap states located in $\equiv Si^-$ level are predominant in charge transfer under a negative voltage. While under the positive bias for the same intermediate region, the charge transfer can be considered as the electron transfer from the empty trap states in the Si_3N_4 nanobelt to the AFM tip, together with the holes transfer from the trap states to the graphite. With respect to the facts that Si_3N_4 nanobelts are of intrinsic semiconductors with negligible hot electrons, as well as the trap states are almost unfilled ones on their surface, the transfer processes (i)–(iii) can be ruled out due to their deep energy level (i.e., $\equiv Si^0$ and =N level) and donor level (i.e., $\equiv Si^-$ level). Meanwhile, owning to the trap states (i.e., ≡Si-Si≡ level) lying close to the valence band edge, the transfer process (iv) can be regarded as the dominated one. That is to say, the current transfer within the nanobelts under a positive voltage should be through the direct tunneling of holes from trap states located in the ≡Si-Si≡ level. This also could be supported by our experiment results with the small current values (smaller trap states in ≡Si-Si≡ level compared to those in $\equiv Si^-$ level) in the nanobelt. In addition, considering that

the applied force can modify the nanobelt surface with only several nm thicknesses, thus process (v) might make a small contribution to the current.

In summary, we have demonstrated the current transport behaviors of single Si_3N_4 nanobelts with the thicknesses ranged in 50–200 nm within the Schottky barrier diodes configured by MSM structure via a C-AFM. The predominant defects in the Si_3N_4 nanobelts are consisted of ≡Si and =N dangling bonds, and the SCCL mechanism dominated the conduction at high voltages. The trap states located in $\equiv Si^-$ level are predominant in charge transfer under a negative voltage applied to the tip electrode. However, the current transfer within the nanobelts under a positive voltage should be through the direct tunneling of holes from trap states located in ≡Si-Si≡ level. Current work might make some foundation understanding to the conducting and trapping behaviors of the Si_3N_4 semiconductors in nanoscale, which benefits to exploring the nanodevices based on the metal-semiconductor-metal sandwiched structures.

The work was financially supported by 973 program (Grant No. 2012CB326407), National Natural Science Foundation of China (NSFC, Grant Nos. 51372122 and 51202115), and Key Technology Program of Ningbo Municipal Government (Grant No. 2013B6007).

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