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Open-circuit voltages: Theoretical and experimental optimizations of rear passivated silicon solar cells using Fz and Cz wafers

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ABSTRACT

The theoretical and experimental open-circuit voltage optimizations of a simple fabrication process of silicon solar cells n^+p with rear passivation are presented. The theoretical results were obtained by using an in-house developed program, including the light trapping effect and metal-grid optimization. On the other hand, the experimental steps were monitored by the photoconductive decay technique. The starting materials presented thickness of about 300 μm and resistivities: FZ (0.5 Ω cm), Cz-type 1 (2.5 Ω cm) and Cz-type 2 (3.3 Ω cm). The Gaussian profile emitters were optimized with sheet resistance between 55 Ω/sq and 100 Ω/sq, and approximately 2.0 μm thickness in accordance to the theoretical results. Excellent implied open-circuit voltages of 670.8 mV, 652.5 mV and 662.6 mV, for FZ, Cz-type 1 and Cz-type 2 silicon wafers, respectively, could be associated to the measured lifetimes that represents solar cell efficiency up to 20% if a low cost anti-reflection coating system, composed by random pyramids and SiO_2 layer, is considered even for typical Cz silicon.

1. Introduction

The silicon solar cells with record efficiencies developed by UNSW have been based on n^+p structures and rear passivated silicon solar cells, such as PERC [1] and for PERL [2] with $\eta = 23\%$ and $\eta = 24.7\%$, respectively. However, they present a complex process of fabrication, involving ultra clean facilities, several steps of photolitography, double anti-reflection coating over inverted pyramids and therefore, becoming a high cost technology.

Aiming the cost reduction in the fabrication and the maintainance of a high efficiency, some modifications have been developed such as the solar cells Random Pyramids Passivated Emitter and Rear Cell (RP-PERC) [3] and LASER fired contact (LFC) [4], developed by Fraunhofer Institute or as a recent pendent patent developed by an industry [5]. In the former, the anti-reflection system is simpler than the ones developed by UNSW, being composed by random pyramids and a single anti-reflection coating, and the rear contacts are formed by photolitography. Meanwhile, the latter type of solar cells is characterized by having the electric contacts formed through the rear SiO_2 by a LASER beam that incides on the surface locally (resulting $100 \times 100\ \mu m^2$ squares with 1 mm dot pitch), and consequently, dropping out one of the required photolitographic steps.

This work presents the theoretical optimization of the open-circuit voltages and the development of a fabrication process of rear passivated n^+p structures using silicon wafers of two different types, FZ (with 0.5 Ω cm) and Cz (with 2.5 Ω cm and 3.3 Ω cm).

Thus, it is imperative to follow two tasks: (a) to obtain a high quality surface passivation over n^+-type and p-type silicon and (b) to perform thermal processes, clean enough to preserve the wafer bulk lifetime even if non-ultra cleaning facilities are used. Another important requirement imposed by the Cz silicon wafers, due to their higher oxygen and carbon concentrations, is the thermal budget of the fabrication process.

The theoretical optimization was performed using an in-house developed code, including light trapping effects and metal-grid optimization. The contour plots of the open-circuit voltages and efficiencies as functions of the emitter surface doping level and thickness are used as guides for designing the fabrication process of the devices.

On the other hand, the experimental optimization was characterized by the measurement of the effective lifetime after each thermal step of the fabrication process using the photoconductive decay technique (PCD). The PCD technique was chosen for being non-destructive, fast and of low cost, thus representing an important tool for monitoring fabrication processes.

2. Theoretical analysis

In previous works [7–9] silicon solar cells with Al diffused over the whole rear surface and low cost optical systems (SiO_2 layer

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random pyramids) were developed providing high short-circuit current densities, J_{sc}, suitable for high efficiency silicon solar cells. However, aiming to increase the open-circuit voltage and the efficiency of the devices, the fabrication technology needs to be changed to rear passivated silicon solar cells.

Thus, in order to design the fabrication process steps of the device, theoretical optimizations were performed using simulacell (v. 2.0), an in-house developed program [10]. The homogeneous emitters were admitted to have the surface recombination velocities under the passivated regions dependent on the surface doping level, $S_p = 10^{-16} \times N_s$ cm/s, characteristic of a passivation performed by a thermal oxidation followed by forming gas annealing (FGA). In other hand the surface recombination for the metal-contact regions are about $S_p = 3 \times 10^6$ cm/s [11]. The p-type base with ⟨1 0 0⟩ orientation presented 1 Ω cm resistivity, 300 μm thickness and a 1.5 ms minority carrier bulk lifetime. The rear surface recombination velocity was admitted to be null, in order to put the emitter characteristics into evidence.

The short-circuit current density, J_{sc} was calculated taking into account the light trapping effect, while the open-circuit voltage, V_{oc}, was determined as a function of total emitter recombination, J_{oe}, and the base recombination. The contour plots of the theoretical open-circuit voltages and efficiencies were obtained as functions of the emitter surface doping level and thickness as presented in Figs. 1 and 2, respectively.

According to Fig. 1, the homogeneous emitter and rear passivated silicon solar cells can provide the high open-circuit voltages; if emitters with up to 2 μm thickness and moderately doped (4×10^{18} cm^{-3} < N_s < 2×10^{19} cm^{-3}) are considered.

The best efficiencies (higher than 25.3%) can be reached for a wide range for surface doping concentration and thicknesses. In Fig. 2, it can be observed in 25.3% curve that the upper bound of the surface doping concentration, $N_s \cong 2 \times 10^{19}$ cm^{-3} allows thicknesses about 0.5 μm < W_e < 1 μm, while the lower bound ($\cong 4 \times 10^{18}$ cm^{-3}) imposes thicknesses belonging to the range 1–3 μm.

An example of parameters for a solar cell with an intermediate surface doping level, $N_s = 7.5 \times 10^{18}$ cm^{-3} and 1.7 μm (87.5 Ω/sq), are $J_{sc} = 43.4$ mA/cm^2, $V_{oc} = 710.3$ mV (as in Fig. 1), FF = 0.826 and $\eta = 25.5\%$ (as in Fig. 2), with optimized metal-grid $F_s = 3.21\%$ and spacing between the fingers $D \cong 1.24$ mm.

It is important to point out that the theoretical optimizations above were performed in order to put into evidence the emitter characteristics, assuming null the base recombination current density and a rear surface recombination velocity. Thus, the reached maximum efficiencies are a bit overestimated when compared to the world record efficiency silicon solar cells [2].

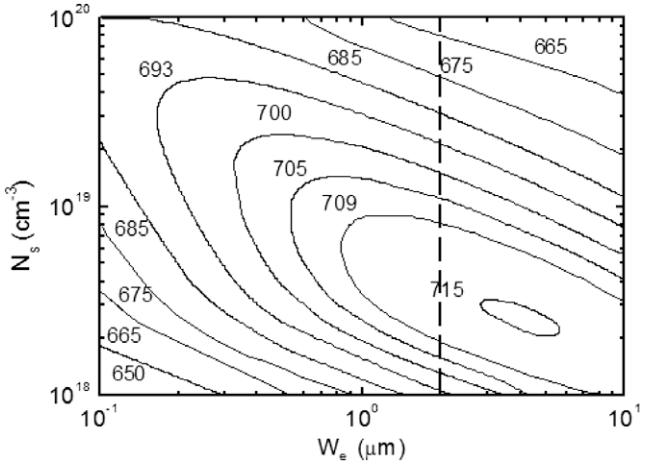

Fig. 1. Open-circuit voltage, V_{oc} (mV) contour plots as functions of emitter surface doping level, N_s and emitter thickness, W_e for n$^+$p structures with 300 μm thickness and 1 Ω cm resistivity. The dash line represents the emitters with about 2.0 μm depth.

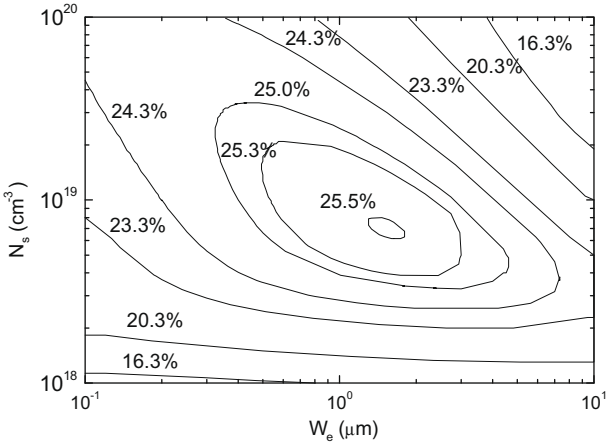

Fig. 2. Solar cell efficiency contour plots as functions of emitter surface doping level, N_s and thickness, W_e for n$^+$p structures with 300 μm thickness and 1 Ω cm resistivity.

3. Photoconductive decay technique and fabrication process monitoring (PCD)

The photoconductive decay technique is a contactless technique able to measure the effective minority carrier lifetime (τ_{eff}) as function of the excess carrier density, Δn, generated by optical excitation.

In order to perform the measurements, the WCT-100 Lifetime Tester equipment from Sinton Consulting [12] was used. In this technique, a flash-lamp pulse incides over the sample and a calibrated solar cell at the same time, then the carrier concentration decay in the sample is measured, as voltage variations of a RF bridge (10 MHz). An oscilloscope registers the data that are stored in a computer for analysis. The flash-lamp pulse can last either a long period (milliseconds) by choosing the quasi-steady state photoconductive decay mode (QSSPCD) or a short period (microseconds) by choosing the transient operation mode (T-PCD).

According to Schmidt and Aberle [13], the measured effective lifetime is related to the recombination that occurs at the surface, τ_s, and in the bulk, τ_{bulk}, as can be seen in:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_s} + \frac{1}{\tau_{bulk}} \quad (1)$$

Thus, in order to extract some information about the bulk lifetime in the analyzed sample, it is imperative to minimize the surface recombination velocity by passivating the surfaces, either using chemical passivation with HF [14], thermal oxidation [13,15,16], light diffusion (n$^+$pn$^+$ structures) [13,17,18] or silicon nitride [19,20].

Aiming the monitoring of a typical rear passivated silicon solar cell process, the thermal oxidation (over p-type and n$^+$-type) was chosen.

4. Experimental details

The FZ wafers with about 0.5 Ω cm resistivity and the Cz samples with 2.5 Ω cm (type 1) and 3.3 Ω cm (type 2) with 3 cm × 3 cm area, were undergone to the standard RCA cleaning and dry oxidation using chlorinated additives (under the

Table 1
Base and emitter characteristics of the samples processed with the n^+p structure (rear passivated with frontal useful area of 4 cm^2): base resistivity (ρ) and thickness (W); emitter sheet resistance (R_{sq}), thickness (W_e) and surface doping level (N_s).

Sample	Material	ρ (Ω cm)	W (μm)	R_{sq} (Ω/sq)	W_e (μm)	N_s (cm^{-3})
B-23-4	Fz	0.5	354	55	1.8	1.22×10^{19}
A-22-2	Cz (type 1)	2.5	341	55	2.1	1.18×10^{19}
5-2	Cz (type 2)	3.3	290	101	1.9	3.76×10^{18}

temperature $T = 1100$ °C). This first oxide has had two main functions: acting as a frontal mask for the phosphorus pre-deposition step and passivating the rear surface. As the effective rear surface recombination velocity is one of the most important parameters for processing n^+p rear passivated structures, this oxide must provide a high quality surface passivation and requires a careful optimization. Then, after being submitted to a photolithographic step, in order to obtain a 4 cm^2 active frontal area, the phosphorus pre-deposition was performed in conventional open-tube using liquid source of $POCl_3$ under 850 °C temperature.

In sequence, the samples had the PSG layers etched and were undergone to a final thermal oxidation using chlorinated additives. This oxidation was planned in order to achieve Gaussian profile emitters with about 2 μm thicknesses and surface doping levels belonging to the optimized range shown in Fig. 1 (dashed line).

Another point is that at this step, the n^+p structures were completely formed, presenting front and rear passivation with SiO_2 layer, excepting by the frontal and back metal contacts (possible to be obtained using different techniques as commented at item 1). Then, a hydrogenation technique can be chosen, either forming gas annealing (FGA) or "alneal" (aluminum alneal), as the most proeminent one to analyze the surface effect.

The typical characteristics of the bases (resistivity and thickness) and the obtained emitters (sheet resistance, thickness and surface doping level) are shown at Table 1, where the samples B-23-4, A-22-2 and 5-2 are the most representative ones of the developed process.

The emitter sheet resistances were measured using the four-probe equipment, presenting surface doping levels and thicknesses in the range of the theoretically optimized emitters of Figs. 1 and 2. The thicknesses were obtained by cylinder etching technique and the surface doping levels were calculated using T-Suprem code. Another important point is that the samples B-23-4 and A-22-2 were processed together, thus presenting the same sheet resistance.

5. Results

The effective minority carrier lifetime was measured as function of the excess carrier density after each thermal process step in order to optimize and monitor the fabrication process, as follows: (a) initial thermal oxidation; (b) phosphorus pre-deposition, (c) PSG dropping out followed by thermal oxidation, (d) forming gas annealing and (e) alneal.

In order to illustrate the measurements that were performed, the effective lifetimes as function of the excess carrier concentration density measured after the hydrogenation technique "alneal" in the chosen samples, B-23-4 (FZ), A-22-2 (Cz-type 1) and 5-2 (Cz-type 2), are presented in Fig. 3.

Adopting the excess carrier density at 1 Sun operation point (in V_{oc} condition), the behavior of the measured effective lifetimes after each thermal step is presented and compared at Fig. 4.

Analyzing Fig. 4, it can be observed that despite the slight decrease in the lifetimes after phosphorus pre-deposition, they can be recovered just after the final oxidation, being surpassed if some kind of hydrogenation technique is performed. The alneal was shown to be the most prominent, reaching the effective lifetimes

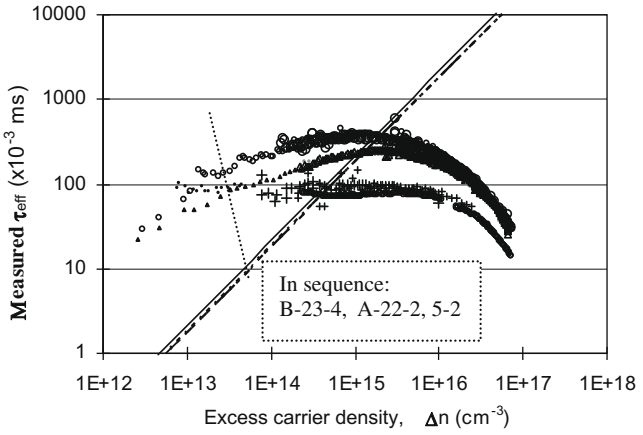

Fig. 3. Measured effective lifetime as function of the excess carrier density in three different samples after the hydrogenation technique alneal, following the growing order sequence: B-23-4 (FZ – 0.5 Ω cm), A-22-2 (Cz – 2.5 Ω cm) and 5–2 (Cz – 3.3 Ω cm). The dash and the continuous lines are associated to the Δn at 1 Sun operation point for Cz silicon and FZ silicon, accordingly.

of 0.09 ms, 0.25 ms and 0.35 ms at 1 Sun operation point for the samples B-23-4, A-22-2 and 5-2, respectively. Another point to be considered is that the measured values of effective lifetimes represent the lower bounds of wafer bulk lifetimes [20].

Another parameter that can be extracted from the PCD measurements is the implied open-circuit voltages, $V_{oc\text{-}imp}$. As these voltages have been proved previously to be quite near the open-circuit voltages of complete devices (with metal contacts) [20,21], they can be considered a suitable parameter to predict the potentiality of the processed devices. Thus, in order to estimate the achievable efficiencies with the n^+p rear passivated structure by the processed samples, the implied open-circuit voltages were also calculated at 1 Sun operation point, and presented at Fig. 5 after performing the hydrogenation techniques: forming gas annealing and alneal.

Analyzing Fig. 5 it can be observed that the alneal step allowed both type of materials, FZ and Cz, to increase the reached implied open-circuit voltages, resulting excellent values, in agreement to Fig. 1. The difference between the implied open-circuit voltages of samples 5-2 and B-23-4 is only about 7 mV, showing the excellent quality of the used Cz silicon (type 2) despite being a lower cost material.

Aiming to estimate the achievable efficiencies by the developed devices, some theoretical simulations were performed using the PC1D code. These theoretical results presented in Table 2 were calculated considering a typical frontal surface recombination velocities for texturized surfaces (random pyramids) plus SiO_2 layer ($S_p = 3000$ cm/s)[22], the lower bounds of bulk lifetimes from Fig. 4 (as discussed previously) and the emitter parameters from Table 1. Some predictions, considering a double layer anti-reflection coating, were also performed. The metal-grid (front and rear) effect was considered, admitting optimized contacts [20].

A comparison among the measured implied open-circuit voltages from Fig. 5, the estimated efficiencies for each sample and

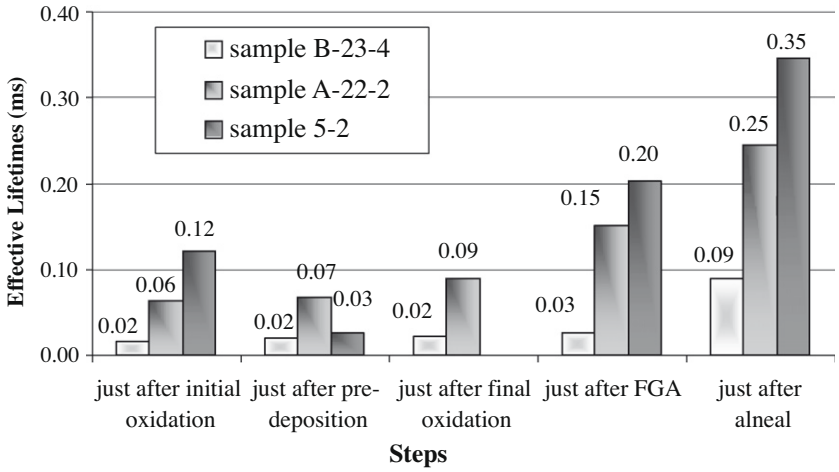

Fig. 4. Effective lifetimes measured after each thermal step (initial oxidation, phosphorus pre-deposition and final oxidation), considering the excess carrier density at 1 Sun operation point at V_{oc} condition. The effect of hydrogenation techniques (FGA-forming gas annealing and "alneal") are also presented.

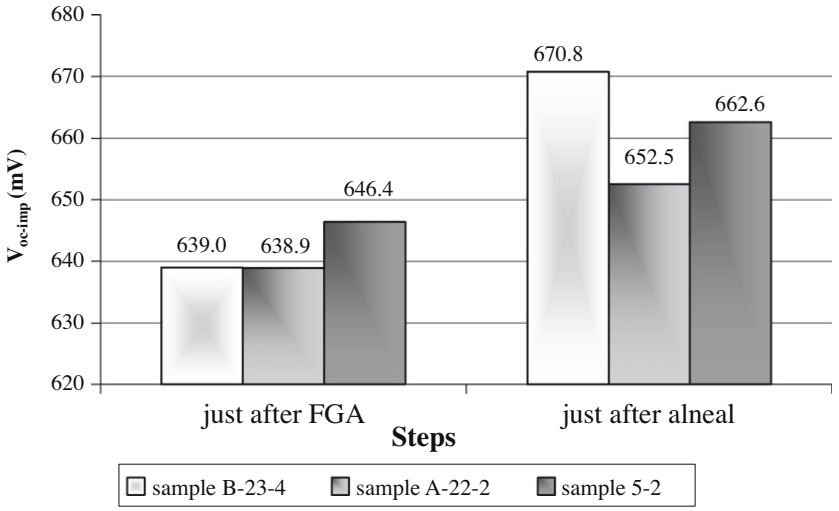

Fig. 5. Implied open-circuit voltages, $V_{oc\text{-}imp}$ after the hydrogenation techniques for the FZ silicon wafer (B-23-4) and the Cz silicon wafers, type 1 (A-22-2) and type 2 (5-2).

Table 2
Comparison between the implied open-circuit voltages obtained at LME-EPUSP, the theoretical predictions using two different types of anti-reflection coatings (single layer, SiO_2, and double layer, $ZnS + MgF_2$) over random pyramid frontal surfaces, and previous works developed in other research centers.

Research center	Values	ρ (Ω cm)	R_{sq} (Ω/sq)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	η (%)
B-23-4 (FZ)	Experimental	0.5	55		670.8 ($V_{oc\text{-}imp}$)		
	Theoretical (text + SiO_2)	0.5	55	37.0–37.5	665.8	0.810	20.0–20.2
	Theoretical (text + ZnS/MgF_2)	0.5	55	38.1–38.6	665.8	0.810	20.5–20.8
A-22-2 (Cz)	Experimental	2.5	55		652.5 ($V_{oc\text{-}imp}$)		
	Theoretical (text + SiO_2)	2.5	55	37.4–37.9	649.4	0.800	19.4–19.7
	Theoretical (text + ZnS/MgF_2)	2.5	55	38.5–39.3	649.4	0.800	20.0–20.3
5-2 (Cz)	Experimental	3.3	101		662.6 ($V_{oc\text{-}imp}$)		
	Theoretical (text + SiO_2)	3.3	101	37.7–38.2	659.6	0.794	19.7–20.0
	Theoretical (text + ZnS/MgF_2)	3.3	101	38.8–39.4	659.6	0.794	20.3–20.6
Universität Konztanz (FZ) [23]	(Text + SiO_2)	0.3	–	37.2	671.0	0.818	20.4
Samsung [24]	(Text + SiO_2)	0.5	–	37.2	666.3	0.807	≅20.0
Fraunhofer Institute RP-PERC (Cz) [3]	(Text + SiO_2)	1.0	–	37.7	656.3	0.795	19.7

the ones obtained in previous works using starting materials with similar resistivities is shown in Table 2. Obviously, the lower resistivity substrates are able to provide the higher open-circuit voltages. Thus, the comparison among the results found in this work and the ones from other research centers is only qualitative, and it was performed with the objective of illustrating the potential of the developed technique, even if industrial like environments are used to process the devices. Another point to be considered is that the high fill factors used to calculate the efficiencies can be experimentally achieved by 2.5–3.3 Ω cm base resistivity wafers, only if technologies as LASER-fired are used to obtain the rear point contacts [6]; otherwise, the rear contact resistance will be high.

In Table 2 it can be seen that the theoretical predicted efficiencies for samples B-23-4 (η = 20.0–20.2%), A-22-2 (η = 19.4–19.7%) and 5-2 (η = 19.7–20.0%) are comparable to the ones experimentally reached by other works [23,24,3], since a single layer of

SiO_2 over random pyramids. On the other hand, if a double layer coating of ZnS/MgF_2 is adopted, the efficiencies of the three samples could reach to about 21%.

Another observation is that the implied open-circuit voltages (experimentally optimized) are lower than the theoretical predictions presented in Fig. 1, despite having their emitter optimized. This difference can be attributed to the fact that the processed samples have base recombination and rear surface recombination velocity different from zero as it was assumed in the theoretical calculations.

6. Conclusions

Low resistivity FZ (0.5 Ω cm) and Cz (2.5 Ω cm and 3.3 Ω cm) silicon wafers were used to process n^+p rear passivated structure. The developed Gaussian profile emitters showed to have the theoretical optimized characteristics (emitter sheet resistance between 100 Ω/sq and 55 Ω/sq).

Each thermal fabrication process step was monitored by using the photoconductive decay technique: (a) initial oxidation; (b) phosphorus pre-deposition; (c) PSG etching followed by oxidation; (d) FGA and (e) alneal. According to the measurements, the effective minority carrier lifetimes could reach the values of 0.09 ms, 0.25 ms and 0.35 ms for the three of most representative samples B-23-4, A-22-2 and 5-2, respectively at 1 Sun operation point (open-circuit voltage conditions).

The implied open-circuit voltages could also be evaluated by the PCD technique, resulting in values of about 670.8 mV (FZ 0.5 Ω cm), 652.5 mV (Cz 2.5 Ω cm) and 662.6 mV (Cz 3.3 Ω cm).

Thus, a fabrication process has been developed providing excellent open-circuit voltages even if a low-cost silicon wafer is used (Cz with 2.5 Ω cm and 3.3 Ω cm) and a simple anti-reflection coating system (SiO_2 over random pyramids) is adopted. It allows to reach the mark of 20% using facilities like industrial enviroments. In case of a double layer of ZnS–MgF_2 replaces the SiO_2 layer the efficiencies could reach to about 21%.

Another remarkable point is that the found values for the implied open-circuit voltages are characterized by belonging to the theoretically optimized ranges for the emitter surface doping level and thickness, and despite not having null rear recombination (as in the theoretical optimizations), high values could be achieved in an industrial like facility.

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