Materials Today: Proceedings 44 (2021) 2033–2037

Contents lists available at ScienceDirect

Materials Today: Proceedings

journal homepage: www.elsevier.com/locate/matpr

Admittance spectroscopy and material modeling for organic electronic applications

R. Liguori *, A. Rubino

Department of Industrial Engineering, University of Salerno, Via Giovanni Paolo II, 132, 84084 Fisciano, SA, Italy

ARTICLE INFO

Article history:
Received 30 September 2020
Received in revised form 30 September 2020
Accepted 4 December 2020
Available online 21 January 2021

Keywords:
Organic semiconductor
Modeling
OTFT
Admittance spectroscopy
Interfaces
Trap states

ABSTRACT

Organic materials, both insulators and semiconductors, led to impressive applications in recent years and particular attention was paid to their performance reliability under realistic atmospheric conditions, fundamental need for the feasibility of organic electronic devices. In this context one of the most critical topics is the investigation of elements affecting device performance, such as trap states at the interface between different materials, and a fundamental target is to provide reliable physical models. By the means of admittance spectroscopy, in this paper, an electrical model was developed to explain the different dynamics of an organic device. Every element of the model was connected to each other through different relationships, each describing a single process. The model provides an efficient parameter extraction method, allowing for example the characterization of the diffusion of mobile ions, the dispersive transport in organic semiconductor bulk, the contact resistance at the metal-organic interface. As a consequence, the model is useful to compare the properties and the performance of devices with respect to the geometries, the materials and the fabrication process conditions.

Selection and peer-review under responsibility of the scientific committee of the International Conference on Materials, Processing & Characterization.

1. Introduction

Organic materials hold promise for low-temperature, large-area and low-cost applications. While some electronic devices based on them are already on the market – one only needs to think of the latest generation OLED (Organic Light Emitting Diode) screens – the considerable variability often observed in the electronic behavior of other components, such as OTFTs (Organic Thin Film Transistors), still requires the investigation of the physics underlying their operation [1]. Considerable effort has been devoting to the understanding of the transport mechanisms in organic materials, charge injection processes and carrier trapping phenomena, in order to improve the electrical performance and stability [2]. With this aim the theoretical interpretation of electronic and optical properties of organic electronic devices is fundamental.

The operation of an electronic device could be significantly affected by the material disorder degree but the most critical aspect is represented by the interfaces formed between adjacent layers [3]. A fundamental example is the interface between the organic semiconductor layer and the dielectric layer in an OTFT [4]. Electrical measurements under light conditions were revealed to be effective in investigating the presence of traps located at insulator-semiconductor interface [5]. Experiments suggested that electron traps induce instability of the threshold voltage (the voltage at the gate contact needed to form a conducting channel between source and drain terminals) and hole traps affect the dependence of charge carrier mobility on gate bias. The multiple trapping and release mechanism (MTR) was used to explain this behavior.

Accurate analytical models with their basis in physical theory help to predict the behavior of devices based on innovative materials [6,7]. In this work, we fabricated and studied two-terminal devices with the same layer structure of an OTFT, forming a metal-insulator-semiconductor (MIS) capacitor, in order to investigate the mechanisms occurring in each material layer of an organic field effect device. In particular, we employed admittance spectroscopy technique to discriminate the different processes involved in the organic device [8,9], with the aim of developing an electrical model able to describe the different dynamics observed in materials.

2. Experimental details and results

MIS capacitors (Fig. 1) were fabricated starting from a heavily p-doped silicon wafer acting as the gate metal plate, with a 400 nm

* Corresponding author.
E-mail address: rliguori@unisa.it (R. Liguori).

https://doi.org/10.1016/j.matpr.2020.12.132
2214-7853/
Selection and peer-review under responsibility of the scientific committee of the International Conference on Materials, Processing & Characterization.

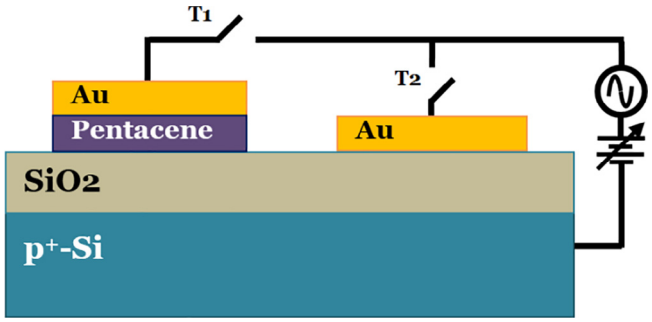

Fig. 1. Cross section of the organic MIS and MIM capacitors, fabricated on a silicon wafer. The connections represent the basic setup used for capacitance measurements: T_1 on for MIS capacitance measurement, T_2 on for MIM measurements.

thick thermal silicon dioxide layer on it used as gate dielectric. A semiconductor film, based on the small molecule pentacene showing a prevalent p-type behavior, was deposited with a thickness of about 60 nm by thermal evaporation, with a base vacuum level of about $2{\cdot}10^{-7}$ mbar and a deposition rate of 0.5 Å/s, keeping the substrate at room temperature. Subsequently, a gold electrode – hereinafter referred to as source – with a diameter of 2 mm was evaporated on the top. The semiconductor layer and the electrode were patterned with the same shadow mask in order to avoid peripheral effects. For each sample, a part of surface was left free of organic semiconductor, in order to allow the fabrication of an equivalent metal–insulator-metal (MIM) junction (Fig. 1), used for the reference measurements to be compared with the organic MIS structure.

The admittance of the device was measured using an Agilent E4980A LCR meter: the high terminal of the instrument was connected to the gate contact of the capacitor under test, while the low one to the source electrode. Measure accuracy was improved by connecting the outer shielding conductors of the coaxial cables to the guard terminal. A small signal with an amplitude of 10 mV was superimposed to the dc bias (V_{GS}) between gate and source terminals swept between −40 and 40 V, while frequency ranged from 200 Hz to 2 MHz. Open and short compensations before measurements allowed reducing the effect of connections and cables.

The complex admittance $Y(\omega)$ provided by the instrument was set according to the parallel circuit model, written with the capacitance C_P and the conductance G_P, functions of the angular frequency ω:

$$Y(\omega) = j\omega C_P(\omega) + G_P(\omega) = j\omega\left[C_P(\omega) - j\frac{G_P(\omega)}{\omega}\right] \quad (1)$$

C_P contains information about the polarization properties, including the response of both fast species, able to follow instantaneously the electric field, and slow species, such as ions, defects and impurities. The imaginary part of the capacitance, i.e. conductance divided by angular frequency, G_P/ω, takes account of the energy dissipated by the device and was referred to as loss (L_P).

The admittance characteristics of the MIS and MIM capacitors were reported in Fig. 2 as function of the signal frequency. The device sweeps from the hole accumulation regime at V_{GS} = −40 V to a deep depletion at V_{GS} = 40 V, i.e. the depletion region extended across the full thickness of the semiconductor. No inversion can be observed, because of the extremely long generation times of the minority carrier in the wide bandgap semiconductor. While at the lowest frequencies the capacitance depends on the bias, with the highest capacitance value measured in accumulation related to the insulator layer capacitance and the lowest one in depletion regime corresponding to the series sum of insulator and depleted semiconductor layers (referred to as geometric capacitance), at higher frequencies the capacitance is weakly dependent on the bias and is close to the geometric capacitance. Furthermore, by comparing the capacitance and the loss curves, three dispersion phenomena are evident, at low, intermediate and high frequencies, respectively attributed to interface states at the insulator-semiconductor interface, to semiconductor relaxation and to semiconductor–metal interface. These dispersions were highlighted in a Cole-Cole plot (Fig. 3) where they take the shape of circles with the center located on the real axis or below it.

3. Modeling

Starting from a theoretical approach, the proposed equivalent electrical model was progressively built through the experimental observations and improved by the introduction of elements interconnected to each other thought different relationships, each describing a single physical process occurring in the MIS device (Fig. 4). Each layer, in principle, could be described by the parallel combination of equivalent capacitance and conductance [10], where the capacitance represents the ability of storing charge and therefore could be used for the characterization of trap states and the conductance is related to the relaxation time constant and therefore gives information about trap state thermalization time and energy depth.

3.1. Insulator layer

The insulator layer was described by a capacitor with plates of cross-sectional area A, separated by a dielectric with thickness t_i and dielectric constant ε_i:

$$C_i = \varepsilon_0\varepsilon_i\frac{A}{t_i} \quad (2)$$

Its value was directly measured from the MIM capacitor fabricated on the same substrate and corresponds to the maximum capacitance measured in MIS device. The anomalous dispersion visible along a large range of frequency was attributed to the diffusion current of slow ions through the insulator layer, responsible for the bias stress effect observed in OTFT, and was described with a complex susceptibility X_{diff} [11] placed in parallel to the capacitance:

$$X_{diff} = A_{diff}(j\omega)^{-\delta} \quad (3)$$

where the amplitude A_{diff} depends on the ion concentration, the insulator thickness and the temperature, and δ is a parameter defining the continuous time random walk of particles ranging between 0 and 0.5 for anomalous diffusion (the case δ = 0.5 corresponds to normal diffusion). In silicon dioxide, this phenomenon is supposed to be generated by the reaction between the Si–OH bonds present at the surface and water molecules diffused through the organic film, however, it is prevalent when a polymeric insulator is used.

3.2. Depletion layer and interface states

While sweeping the bias from −40 V towards 40 V, the majority carrier density decreases, gradually driving the semiconductor film from accumulation into depletion regime. The region free of charge, defined depletion layer, reacts as a dielectric and therefore can be represented through a capacitor C_D, as for (2), with dielectric constant ε_{osc} of the semiconductor and depletion layer width w_D. In this regime the effect of trap states at the semiconductor-insulator interface can be probed. In particular, each trap level contributes to some energy dispersion, introducing a relaxation time constant, τ_{it}, described by the series combination of a capacitance and a conductance [12]: as frequency increases traps lag behind the ac signal,

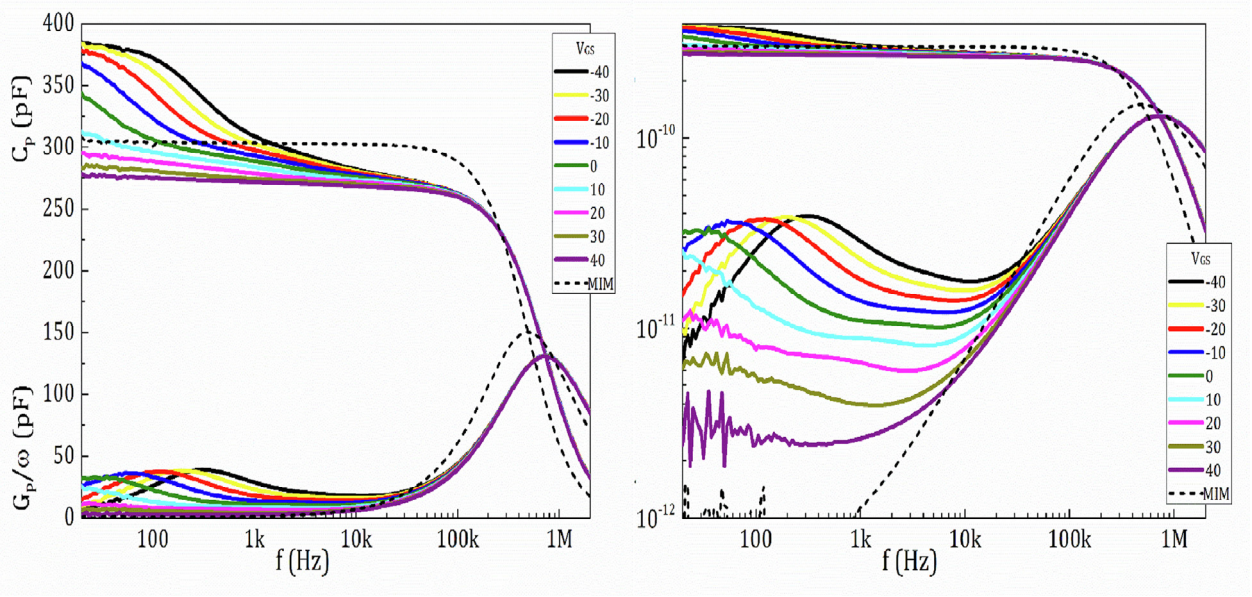

Fig. 2. Frequency–dependence of the capacitance, *C*, and the loss, G/ω, of a MIS capacitor fabricated with pentacene and of a MIM with silicon dioxide. The linear scale (a) underlines the capacitance variation, while the logarithmic scale (b) points out the dispersion peaks exhibited by the loss curves.

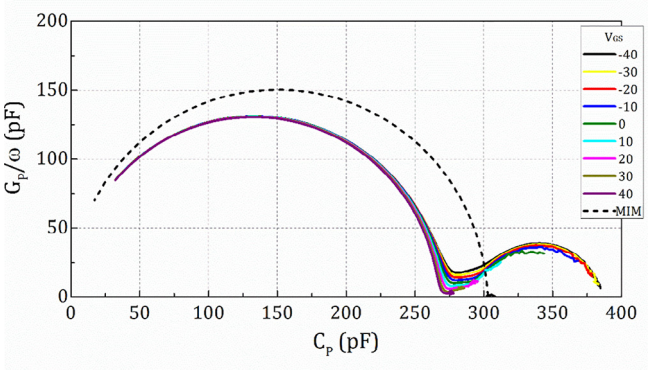

Fig. 3. Cole-Cole plot for the MIS and MIM capacitors, reporting the imaginary and real parts of the admittance. In the MIS capacitor three circles are visible: the largest one, on the right side, was related to the contact resistance, the left one to the trap states at the insulator-semiconductor interface, the suppressed circle in the middle to the bulk semiconductor traps.

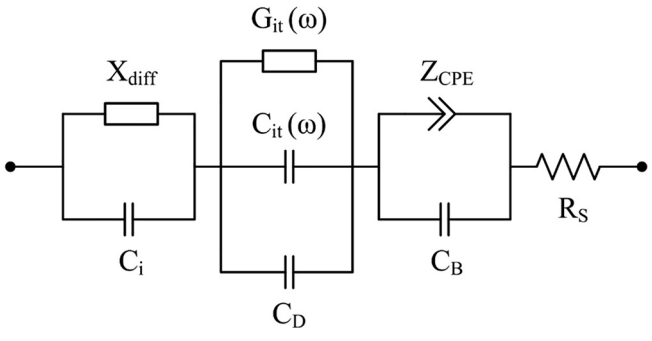

Fig. 4. Equivalent circuit for an organic based MIS capacitor. It is constituted of four main blocks, arranged in the order: gate insulator layer, depletion layer in the semiconductor with interface trap states, organic semiconductor bulk and contact resistance.

causing a decrease in the capacitance while generating a peak in loss spectrum at the frequency $\omega_{max} = 1/\tau_{it}$. Since these effects are cumulative, a distribution of interface trap levels over the semiconductor bandgap (with a density D_{it} per unit area per eV) introduces a continuous distribution of relaxation times, generating broader admittance plots with a loss peak of amplitude equal to $0.4qD_{it}$ occurring at the frequency $\omega_{max} = 1.98/\tau_{it}$. The equivalent admittance becomes:

$$Y_D(\omega) = j\omega\left[C_D + \frac{qD_{it}}{\omega\tau_{it}}\arctan(\omega\tau_{it})\right] + \omega\frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right] \quad (4)$$

3.3. Organic semiconductor bulk

Trap states in the semiconductor bulk also are known to cause a frequency dispersive capacitance and a conductance contribution [12] and therefore also the pentacene bulk layer, not depleted, with thickness t_{osc}–w_D and resistivity ρ_{osc}, can be described by a capacitance C_B and a resistance R_B, whose product gives the relaxation time of the organic material, defined as the time needed by the majority carriers to neutralize a disturbance:

$$\tau_B = C_B R_B = \varepsilon_0\varepsilon_{osc}\frac{A}{t_{osc}-w_D}\cdot\rho_{osc}\frac{t_{osc}-w_D}{A} = \varepsilon_0\varepsilon_{osc}\,\rho_{osc} \quad (5)$$

However, the arcs in the Cole-Cole plot associated to the organic semiconductor bulk exhibit a depressed shape with the center displaced below the real axis. This can result from a system with deep traps homogenously distributed in energy with relaxation times exponentially depending on the trap depth. Therefore, in the proposed model the Cole-Cole theory [13] usually used for polar liquid and solids was found to be more adequate to describe the dispersion in the organic semiconductor:

$$\varepsilon^* - \varepsilon_\infty = \frac{\varepsilon_s - \varepsilon_\infty}{1+(j\omega\tau_0)^{1-\gamma}} \quad (6)$$

Here, ε^* is the complex dielectric constant, ε_s and ε_∞ are the static and high frequency limits of the dielectric constant, respectively, τ_0 is the most probable relaxation time and the parameter γ, assuming a value between 0 and 1, indicates the width of distribution of relaxation times (the case $\gamma = 0$ corresponds to Debye

equation). The dielectric response of the polycrystalline organic semiconductor was described by a complex impedance, which could consider the capture processes from deep traps in the bandgap and the relaxation process related to the excitation from them. In particular, the semiconductor layer was represented by the parallel combination of a capacitor, C_B, and a constant phase element (CPE) with the dispersion parameter α:

$$Z_{CPE} = R_B(j\omega\tau_B)^{-\alpha} \tag{7}$$

This expression for the CPE was designed in order to generate an admittance for the organic semiconductor layer, which could yield an infinite capacitance for low frequencies ($\omega \ll 1/\tau_B$) and a capacitance coinciding with the bulk layer for high frequencies ($\omega \gg 1/\tau_B$). The resulting equation for semiconductor bulk combined with the series of the insulator and depletion capacitances, C_0, led to an expression, for the total admittance of the circuit in Fig. 4, reproducing the Cole–Cole equation:

$$Y_{tot} = j\omega\left[\frac{C_0 C_B}{C_0 + C_B} + \frac{C_0^2}{C_0 + C_B}\cdot\frac{1}{1 + \frac{C_0 + C_B}{C_B}(j\omega\tau_B)^{1-\alpha}}\right] \tag{8}$$

Here, the static limit of the capacitance is C_0, while the high frequency limit is the geometric capacitance of the device, independent from the operating regime. It can be demonstrated that the dispersion peaks decrease when devices are driven from accumulation into depletion region, in accordance to experimental data. Since the CPE is not supported in time–domain compact circuit simulators, it could be replaced with a set of series–RC branches in parallel [14]. Theoretically the number of branches is infinite, but it could be limited given a required phase tolerance and a finite frequency range over which the approximation must hold.

3.4. Contact resistance

The dispersion phenomenon occurring at very high frequencies was finally attributed to the series resistance R_S, nearly independent from the operating regime, due to both the resistance of silicon wafer and the charge injection barrier for holes between gold and pentacene. The relaxation time introduced by the electrode is therefore given by the product of series resistance and geometric capacitance of the device.

4. Discussion

The analytic equations of the equivalent circuit developed to describe the different materials and their interfaces in a MIS device were simulated and compared with the experimental data with the aim of extracting the fundamental physical parameters and relating them to the fabrication process. The resulting fitting curves reported in Fig. 5(a) well describe the experimental data.

From the MIM capacitance, assuming a dielectric constant of 3.9 for the SiO_2 layer, an insulator thickness of about 380 nm was obtained. However, observing the maximum capacitance measured in accumulation regime at low frequency in the MIS device, which should correspond to the insulator capacitance, a reduced thickness of about 300 nm was extracted and was explained further on. The anomalous diffusion was described by an amplitude $A_{diff} = 20$ pF(rad/s)$^{\delta}$ and a parameter $\delta = 0.2$.

At intermediate frequencies, the finite conductivity of the semiconductor bulk yields the reduction of the overall capacitance. Here the dispersive transport due to the structural disorder imposes an upper limit on the frequency at which the injected holes are able to follow the applied ac signal. This critical frequency falling between 1 and 10 kHz is evident from the loss peaks, whose widths are broader than a peak related to a dispersion with a single time constant. The relaxation time constant of the semiconductor, as well as the dispersion parameter α, gradually increase by moving the dc bias towards the depletion regime; this behavior was justified through the increasing resistivity due to the greater disorder of the probed bulk region ever closer to the contact generated during deposition.

When the gate bias sweeps from negative toward positive values, a depletion layer is formed and expands in the semiconductor and the capacitance drops to the series sum of C_i and C_D, including the interface trap contribution. In particular, by tuning the gate bias it is possible to change the band bending at the semiconductor surface and to examine the states changing their occupancy. As the probed defects become deeper into the bandgap with decreasing concentration, they give rise to loss peaks that shift to lower frequencies, from which the density of interface states, D_{it}, within a range of a few kT, was extracted and reported, along with relaxation time constants τ_{it}, in Fig. 5(b).

The inspection of the experimental curves provided also the values of depletion and bulk capacitances, which could be used to evaluate the depletion layer width. In this case, an anomalous layer

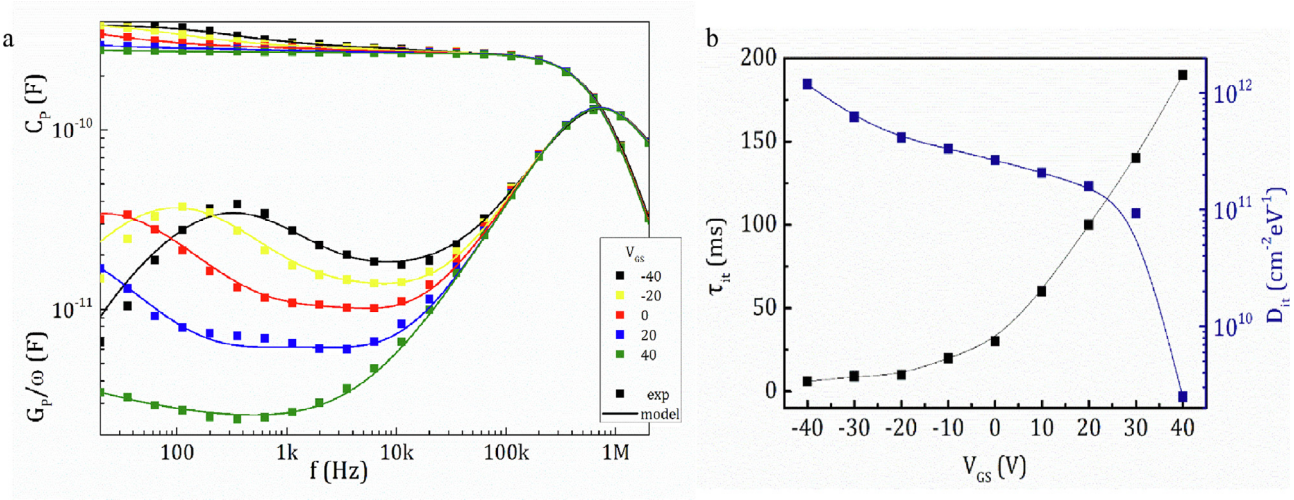

Fig. 5. (a) Fitting of experimental data to the proposed model equations; (b) extracted values for relaxation time and surface density of interface trap states.

between semiconductor and insulator arose with a thickness corresponding to the difference between the two discordant values extracted for the insulator thickness. This behaviour revealed the presence of an interface layer at the silicon dioxide surface, modified in its structure by the deposition of pentacene.

Finally, at high frequency, where the contact produces a dispersion for all gate biases, the extracted series resistance ranges from 805 and 840 Ω, decreasing when the device is driven into accumulation, in accordance with the reduction of injection barrier observed in staggered OTFTs [15].

5. Conclusion

Admittance spectroscopy was revealed to be an effective technique to characterize the different materials and the interfaces occurring between adjacent layers in an electronic device, especially in applications where the study of the physical phenomena underlying the device operation is still necessary to improve performance and stability. This is the case of electronic devices based on organic materials become very attractive in recent years. In this work an electrical model able to predict and fully describe their dynamics was proposed and is useful to compare the properties of devices fabricated with different geometries, materials and deposition conditions. The results obtained in a pentacene-based MIS capacitor suggested the presence of hole trapping states at the insulator-semiconductor interface affecting the charge transport.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] X. Guo et al., IEEE Trans. Electron Dev. 64 (2017) 1906–1921.
[2] R. Liguori, A. Botta, S. Pragliola, A. Rubino, et al., Semicon. Sci. Technol. 32 (2017) 065006.
[3] G.D. Licciardo, L. Di Benedetto, S. Bellone, IEEE Trans. Electron Dev. 63 (2016) 1783–1787.
[4] R. Liguori, H. Usta, S. Fusco, A. Facchetti, et al., IEEE Trans. Electron Dev. 64 (2017) 2338–2343.
[5] R. Liguori, A. Rubino, Org. Electron. 15 (2014) 1928–1935.
[6] L. Di Benedetto, L. Licciardo, T. Erlbacher, A.J. Bauer, et al., IEEE Trans. Electron Dev. 63 (2016) 3795–3799.
[7] G.D. Licciardo, L. Di Benedetto, S. Bellone, Mater. Sci. Forum 858 (2016) 825–828.
[8] M.R. Fiorillo et al., Mater. Today Proc. 4 (2017) 5053–5059.
[9] E. Bezzeccheri et al., Mater. Today Proc. 4 (2017) 5045–5052.
[10] P. Stallinga, Electrical Characterization of Organic Electronic Materials and Devices, Wiley, Chichester, UK, 2009.
[11] R. Ledru et al., Org. Electron. 13 (2012) 1916–1924.
[12] E.H. Nicollian, J.R. Brews, MOS (Metal-Oxide-Semiconductor) Physics and Technology, Wiley, New York, 2002.
[13] K.S. Cole, R.H. Cole, J. Chem. Phys. 9 (1941) 341.
[14] J. Scott, P. Single, IEEE Trans. Biomed. Circuits Syst. 8 (2014) 382–390.
[15] G. Horowitz, P. Lang, M. Mottaghi, H. Aubin, Adv. Funct. Mater. 14 (2004) 1069–1074.