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A method for determining average damage depth of sawn crystalline silicon wafers

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The depth of surface damage (or simply, damage) in crystalline silicon wafers, caused by wire sawing of ingots, is determined by performing a series of minority carrier lifetime (MCLT) measurements. Samples are sequentially etched to remove thin layers from each surface and MCLT is measured after each etch step. The thickness-removed (δt) at which the lifetime reaches a peak value corresponds to the damage depth. This technique also allows the damage to be quantified in terms of effective surface recombination velocity (S_{eff}). To accomplish this, the MCLT data are converted into an S_{eff} vs δt plot, which represents a quantitative distribution of the degree of damage within the surface layer. We describe a wafer preparation procedure to attain reproducible etching and MCLT measurement results. We also describe important characteristics of an etchant used for controllably removing thin layers from the wafer surfaces. Some typical results showing changes in the MCLT vs δt plots for different cutting parameters are given. © *2016 AIP Publishing LLC.* [http://dx.doi.org/10.1063/1.4944792]

I. INTRODUCTION

Sawing is a crucial step in converting a Si ingot into wafers, which are then processed to make electronic devices, including solar cells. Unfortunately, sawing is not only an expensive step, but it causes a significant waste of material due to cutting (Kerf) loss and by introducing damage on the wafer surfaces, which must be removed before fabrication of devices.

For the last two decades, the most common method for sawing semiconductor wafers has been slurry cutting, which uses free-abrasive suspended in the slurry.[1,2] However, a newer technique of diamond wire sawing (DWS) has recently been introduced and is gaining wide acceptance, particularly in the photovoltaic Si cutting.[3] The DWS is a fixed-abrasive approach in which the cutting wire is coated with diamond chips (fixed-abrasive). Typically, the merit of a wafer sawing process is evaluated in terms of throughput, total thickness variation (TTV) of the wafers, and other factors such as cost of ownership and how easily Si can be recovered from used slurry.

For photovoltaic wafers, which are quite thin (<180 μm), there is an additional factor—the depth of surface damage, that becomes important. Because PV wafers are thin, etching of significant thickness as a part of damage removal is a major fraction of the wafer thickness. Concomitantly, it is desirable to minimize the surface damage as a part of cutting process itself. Thus, it is necessary to control and minimize the cutting damage. Generally, wafer manufacturers can easily measure physical parameters of wafers (such as, TTV and wafer-to-wafer thickness variation), but there are no easy ways to measure depth and distribution of damage. Yet, this information is needed by sawing companies for optimizing throughput while minimizing the damage to the wafer surfaces. It is also needed by the solar cell manufacturers to ensure that all the damage is etched away during wafer preparation before solar cell processing.

The surface damage due to sawing is caused by the stress produced by the grit and the wire during cutting. It occurs in the form of dislocation loops, phase changes, and lattice stress/deformation, as discussed more in Sec. II. Typically, the surface damage is measured in qualitative ways, as physical manifestation of damage, by a number of approaches, which include XRD, TEM, and angle polishing followed by defect etching[4–6]—all of which examine the mechanical damage only. Furthermore, all these techniques are very tedious, time-consuming, and only produce local information that can greatly vary over the wafer. A technique based on measurement of surface photovoltage (SPV) produced at the wafer surface after step etching thin layers of damage from the wafer was developed long time back.[7] This approach worked very well for wafers produced by slurry cutting, which yields wafers with quite planar surfaces, allowing easy placement of the capacitive probe on the surface during measurement. However, the DWS wafers can have large surface features, making it difficult to place a capacitive coupling probe, especially over a large area.

Here, we describe a new, simpler approach for determination of the average damage depth and its distribution over a large area. This method uses minority carrier lifetime (MCLT) measurement by photoconductance decay (PCD) instead of capacitively coupled SPV and uses an RF conductive probe in the form of a coil. It is very accurate, fast compared to all other methods, applicable to wafers with rough surfaces, can be easily adapted in a solar cell facility having a lifetime measurement system, and as shown in this paper, is also capable of yielding in-depth distribution of damage.

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II. PRINCIPLE OF THE TECHNIQUE

It is fruitful to first briefly describe the nature of damage due to sawing and identify its electronic effect of carrier recombination. The process by which cutting of Si occurs is primarily by brittle fracture mechanism (with a small component of ductile flow mode).[8] Because both these mechanisms require large mechanical stresses (exceeding 1 GPa) to chip away small chunks of the material, cutting process is accompanied by other unwanted phenomena associated with large stresses. These include: (i) phase transformations into possible seven other crystalline forms and into amorphous Si;[9] (ii) formation of dislocations in the form of small loops, which remain frozen in near-surface regions of the wafers due to the fact that dislocation propagation velocity is quite low at the cutting temperatures; (iii) generation of some micro-cracks caused by brittle fracture, which can be effectively eliminated by optimizing the cutting process; and (iv) lattice distortions without accompanying dislocations.

The dominant part of the damage, which contributes to excessive carrier recombination, is associated with dislocations. Traditionally, the most common way to observe the dislocations generated in the near-surface region due to wafer cutting is to angle polish a sample followed by defect etching. This is illustrated in Figure 1, which shows optical micrograph of a DWS sample that is chemically mechanically polished at 10° and then defect etched using Sopori etch to delineate dislocations.[10] It is seen that dislocation loops are clustered in high densities around the striations produced by wire motion (directional) on the as-cut surface, and that dislocations propagate beneath the surface to a depth of about 5 μm. It should be kept in mind that polishing at 10° angle causes a vertical magnification of 5.6. One can also see that the penetration of dislocations is not spatially uniform.

Although the saw damage is mechanical in nature, it is accompanied by changes in the electronic properties of the wafer surfaces. In particular, dislocations produce dangling bonds and interface states, which lead to very high carrier recombination in the damaged region. A more detailed discussion of damage is given in a previous paper.[6] Here, we would like to mainly point out that the damage produces

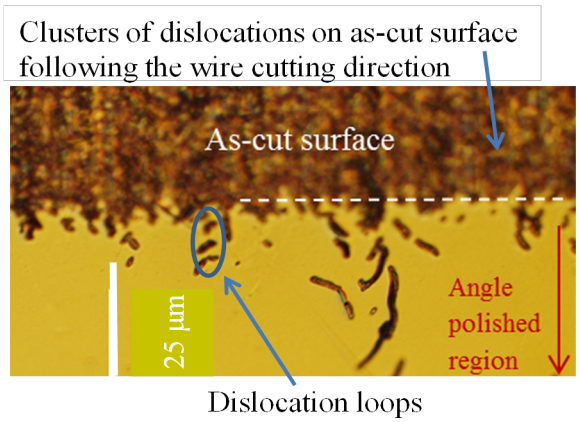

FIG. 1. Defect-etched, 10° angle polished sample from a DWS wafer, showing dislocation loops at the as-sawn surface and dislocations penetrating below the surface. The vertical height is magnified by 5.6 X because of angle polishing.

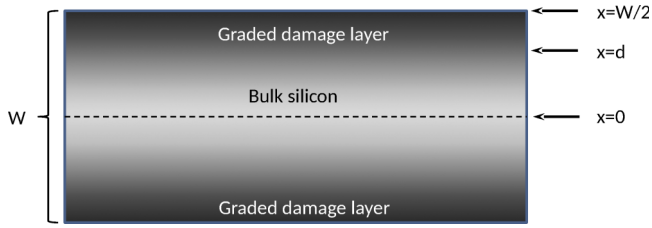

FIG. 2. An illustration of a typical DWS wafer with surface damage. The saw damage on each surface is shown to be graded to a depth of "d". The bulk lifetime of the wafer is τ_B.

an in-depth non-uniformity in the carrier recombination of the wafer, with highest recombination at the surface. This is illustrated in Fig. 2, where a sawn wafer is considered to be comprised of three regions—a bulk region of lifetime (τ_b) and two near-surface regions with graded damage and carrier recombination region below each surface.

These high carrier recombination regions contribute to a high surface recombination velocity during MCLT measurement, and its effect on the measured lifetime (τ_{eff}) can be expressed by a well-known expression;[11]

$$\frac{1}{\tau_{eff}} = \left(\frac{1}{\tau_B}\right) + 2\frac{s_{eff}(\delta t)}{W}, \quad (1)$$

where τ_{eff} is the measured lifetime, τ_B is the bulk lifetime, W is the thickness of the wafer, and S_{eff} is the effective surface recombination velocity of minority carriers resulting from the residual damage layer. It should be pointed out that factor 2 in Equation (1) appears because the wafer has damage on both surfaces and is etched from both sides.

The basic principle of this method is to measure the effect of the surface recombination on the effective MCLT. It should be noted that S_{eff}, which represents total recombination within the damage layer, is a function of etch depth (δt) and is related to in-depth damage distribution. If thin layers are etched away from the surface, the surface recombination velocity (SRV) will progressively decrease till the MCLT reaches a peak. Here, we illustrate the concept by actual measured data. A measured plot of τ_{eff} vs δt is shown in Fig. 3 (dotted line). This measurement was made by sequentially etching and measuring τ_{eff} values of the same wafer, but no external passivation of

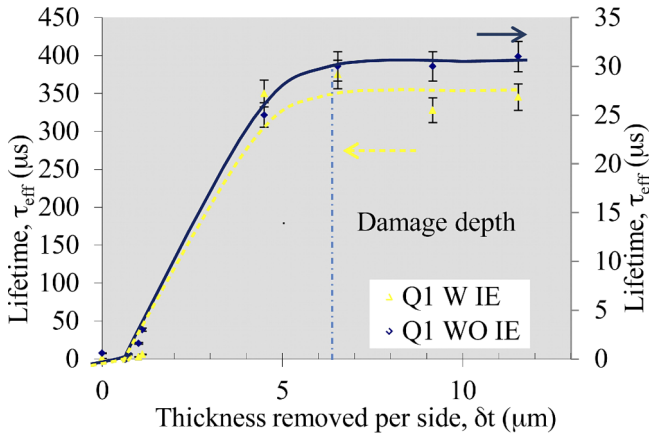

FIG. 3. τ_{eff} vs δt plot for a set of DWS wafers: without I-E passivation and with I-E passivation.

the wafer was used. It is clearly seen that lifetime reaches a peak after removing about 6 μm of thickness from each surface, indicating the damage depth to be 6.5 μm. It may be noticed that the measured lifetime reaches to a maximum of only 30 μs (although the bulk lifetime of the wafer was about 450 μs). This is simply because no surface passivation was applied during the measurement.

However, if the measurement is made with I-E passivation (as described in Section III), the sensitivity of the measurement can be greatly increased and the maximum lifetime will reach close to the bulk lifetime value. Figure 3 also shows the corresponding τ_{eff} vs δt plot (with IE passivation). Note that the damage depth remains unchanged.

III. EXPERIMENTAL DETAILS

Although the proposed method is simple and straight forward, its experimental implementation requires two essential tasks: (i) a chemical etchant that can remove thin layers in a highly controlled manner and (ii) a robust wafer preparation procedure before and after each etching step that can result in a reproducible lifetime measurement.[12] Here, we describe an etching procedure that we have studied in detail for removing thin layers of Si uniformly over 156 mm × 156 mm wafers.

Our initial measurements (see, Fig. 3) were made by sequentially etching the same wafer and taking lifetime measurements after each etch step. However, we found that I-E solution used for passivation is very difficult to clean and leaves a residue, which interferes with cleaning and etching in the subsequent steps. To overcome this, we arrived at a simpler procedure of using 8 samples, obtained by cleaving two full size adjacent (sister) wafers into 8 quarters, and each of them is etched for different times. This replaces the tedious procedure of sequentially etching the same wafer. This is a much quicker approach and gives same results as sequential etching of same wafer.

A. Wafer cleaning before and after etching

The sawn wafers are first gently scrubbed with a piece of lint-free cheese cloth soaked in oil-free soap and water solution, and then, rinsed in deionized (DI) water to remove any loose material from the surface. Then, the samples are solvent cleaned in acetone, rinsed in isopropyl alcohol (IPA), dried and then rinsed in DI water. Next, they are cleaned in piranha ($2H_2SO_4$: H_2O_2) at 80 °C for 20 min. The piranha cleaned samples are rinsed in DI water, dried, and they are ready to be etched as described in Section III B. After etching, the samples are again rinsed in DI water/dried, piranha cleaned, dipped in dil. HF, rinsed in DI water/dried. The dried samples are placed inside a polyethylene bag and passivated using a few drops of (I-E) solution (0.1 M) on each surface. Iodine-ethanol solution is gently spread over the entire wafer and the bag is sealed and is ready for lifetime measurement. Lifetime is measured with the sample inside the I-E containing polyethylene bag.

B. Chemical etching for removal of thin layers of damage from silicon wafer

We have used an etching solution that was reported long time back for etching damage on small-area Si samples with small surface roughness. This particular etch (now simply called as 115 etch) consists of HF: HNO_3:CH_3COOH in 1:1:5 proportions. Because our current samples are large, DWS wafers (typically 156 mm × 156 mm, pseudo square), which also have large surface roughness, the properties of this etch were restudied and the procedure developed for controlled etching of large samples. Here, we briefly present some recent results of this etch for removing small thicknesses from large Si wafers.

This etchant has a very low etch rate for undamaged Si and is uniform over large area wafers. For example, for a polished Si wafer, the etch rate is <0.05 μm/min per side. Etch rate increases if the wafer surface is rough (even without surface damage). For damaged Si, etch rate in 115 etch depends on the degree of damage of the wafer—etch rate is higher for wafers with higher degree of damage. Etch rate also depends on the condition of the etch bath such as its usage and its volume. In particular, the reactivity of 115 etchant increases with its use, often referred to as "etchant activation."

Figure 4 shows thickness-removed and the etch rate as a function of etch time for a set of as-sawn samples. These samples were prepared and cleaned as described in section A and etched sequentially for increasing amounts of time in a large etch bath (total volume = 2.4 l) and the thickness-removed was measured by weighing the silicon sample before and after etching. As expected, etch rate is not linear; it is seen that the etch rate first decreases and then increases as the number of samples etched in that etchant increases. This non-uniform etch rate can be reconciled by keeping the following etch characteristics in mind. The initial reactivity of the etchant depends on the degree of the surface damage, which decreases as the wafer surface is etched. However, the etchant activity of most HF: HNO_3:CH_3COOH based etchants increases as the solution gets used, as has been very well described in previous papers.[13,14] Based on the etchant activation alone, one would expect etch rate to increase monotonically as more and more Si is etched and gets dissolved into the etchant. In practice, as

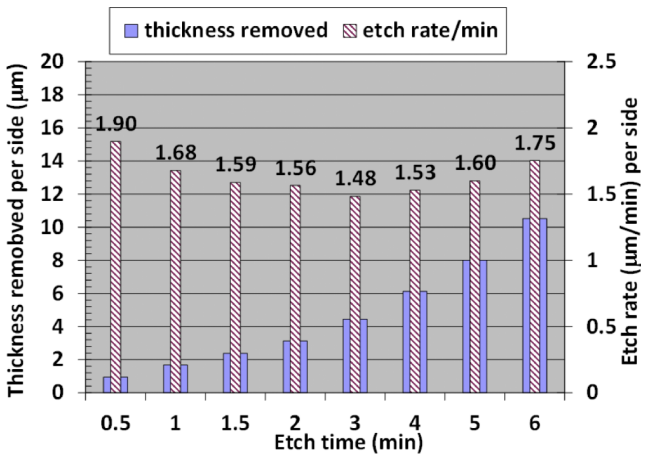

FIG. 4. Wafer thickness removed and the corresponding etch rate as a function of etch time.

the damage is being removed and the etchant gets activated, the etch rate experiences a dip (resultant of lowest etch rate for damage free surface), as seen in the etch rate plot [see, Fig. 4].

It should be pointed out that measurement of small thickness (~1 μm) removed after each etching step is quite challenging because as-cut PV wafers have large surface feature height variation (>5 μm) and significant thickness variations (TTV ~15 μm). We have made the thickness measurements in two different ways—(i) using a sensitive dial gauge and measuring the thickness in the same spots over the wafer after each etch step. This seems to work well for samples that have low surface roughness such as slurry cut wafers or DWS wafers cut by thin wire and (ii) weighing samples before and after etching, which worked well for this study. The average thickness removed is then given by, $\Delta W/(\rho.A)$. Where ΔW is the change in weight, ρ = density of Si, and A is the sample area. Typically, the ΔW is 50 mg/μm (for a quarter taken from 156 mm × 156 mm commercial wafers). Hence, a change in the thickness can be easily measured to an accuracy of ±0.1 μm with a scale having a sensitivity of ±1 mg.

C. Lifetime measurement

In this study, the MCLT of the samples was measured using Sinton tool, WCT 120. In this system, the carriers are generated in the sample by optical excitation from a flash lamp and photoconductance is measured either in a quasi-steady state (QSS) mode or as a transient decay. In the QSS mode, the system measures the total conductance of the wafer as a function of injection level and is used if the wafers have short (<few hundred microseconds) τ_{eff}.[15] Because the initial MCLTs of as-sawn wafers are quite low, we used QSS mode in all the measurements. Furthermore, we used the maximum effective lifetime obtained from each measurement done after each etch step. Typically, the maximum lifetime occurs in the vicinity of the same injection level in all these measurements. The measurement area is determined primarily by the coil size, which is typically about 2 cm in diameter.

Because during the lifetime measurement, carriers are generated within the entire thickness of the wafer and experience a net flow to the wafer surfaces, the damage layers act as very large recombination regions causing the as-sawn wafer to yield τ_{eff} that is much lower than τ_b. However, as the surface layers are removed by chemical etching, the τ_{eff} will increase until the damaged layer is fully removed. As pointed out earlier in the paper, using I-E passivation greatly improves the sensitivity of the measurement.

Figure 5 shows results of sequentially measured lifetime as a function of injection level (or minority carrier density, MCD) after etching 7 quarter-samples, from two adjacent wafers. These were diamond wire sawn, P-type, 2 Ω-cm (B doped) wafers. Each set of data is corrected for the thickness change due to etching. These data show several features: (a) the maximum τ_{eff} increases with each etch step till all damage is removed. We should, however, point out that there is generally a slight decrease in MCLT after the damage is fully removed (also see Figs. 6 and 7). This decrease is because the wafer becomes thinner with each etching and the effective photon absorption within the wafer decreases; (b) under low injection,

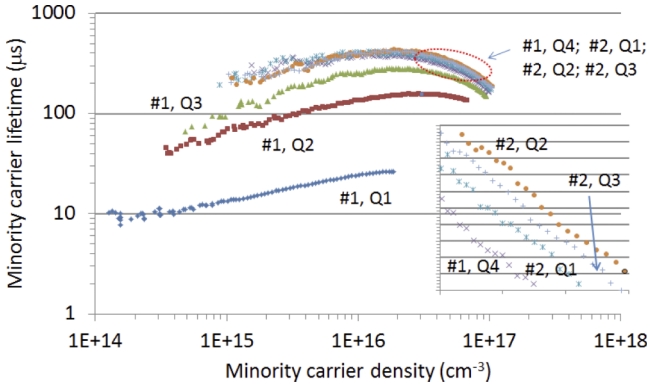

FIG. 5. Injection level dependence of 7 quarter-samples, from adjacent 2 wafers (labelled as #n, Qm, where n = 1, 2 and m = 1, 2, 3, 4). The inset shows that the MCLT of #2, Q3 falls below #2, Q2.

τ_{eff} increases with increase in MCD. This behavior is well known and is attributed to impurity recombination (such as Fe or Fe-B); (c) the peak of τ_{eff} shifts slightly to higher MCD with progressively increasing etch steps. This behavior is due to increasing MCD with increasing τ_{eff} and with reducing sample thickness after each etching step.

IV. RESULTS

We have applied this technique to numerous wafers that were cut with commercial saws with two different sawing methods—slurry and diamond wire. We will only describe the results of diamond wire sawing because slurry cutting has already been well established (we have used it primarily for a reference for testing). We will describe examples of different damage distributions resulting from wafers cut with DWS.

We first show τ_{eff} vs δt plots of wafers taken from four (A, B, C, D) different ingots (P-type), which were cut by the same type of wire—having core size of 120 μm and grit size of 10-20 μm, other cutting parameters such as wire usage and feed rate and wire velocity etc. were also the same. These results are shown in Fig. 6. As expected, it can be seen that

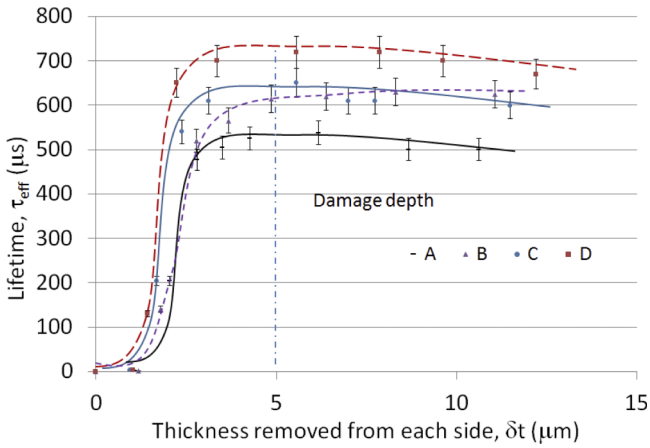

FIG. 6. τ_{eff} vs δt (thickness removed from each side) plot for a typical diamond sawn wafers.

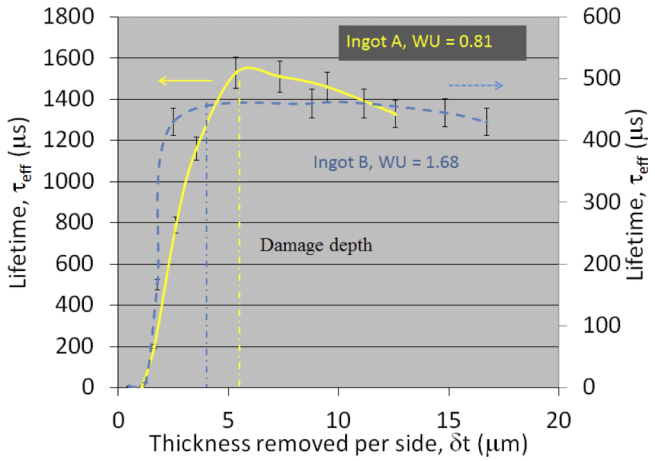

FIG. 7. Measured lifetime as a function of surface thickness removed per side. The starting thickness of the wafer was 145 μm. The wafer with higher MCLT is N-type.

all plots reach to a peak τ_{eff} at about the same value of δt, implying that the damage depth is about the same for all the wafers from these four ingots. The lifetimes peak at about 5 μm as shown by the vertical line in Fig. 6, implying this to be the damage depth. Because these four ingots differ in material quality, the peak τ_{eff} values for the τ_{eff} vs δt plots are different.

The next example is of two ingots, cut by the same type of wire but the wire use (WU) parameter is different. The wire usage is defined as the average wire length used in meters per wafer (m/wfr). A higher WU values implies more fresh wire is used during cutting. Figure 7 shows τ_{eff} vs δt plots for wafers from two DWS ingots A and B, cut with WU values of 0.81 m/wfr and 1.68 m/wfr, respectively. One of the ingots, with lower MCLT is P-type while the other with higher MCLT is N-type. As seen from this figure, both N- and P-type wafers are well passivated by I-E. The wire and grit sizes for both cases were 80 μm and 6-12 μm, respectively, and other cutting parameters were the same.

From Fig. 7, we can determine the damage depth for plots A and B to be 4 μm and 5.4 μm, respectively, indicating that using less wire (WU = 0.8m/wfr) creates deeper damage. We should also point out that the rise (slope) of the lifetime

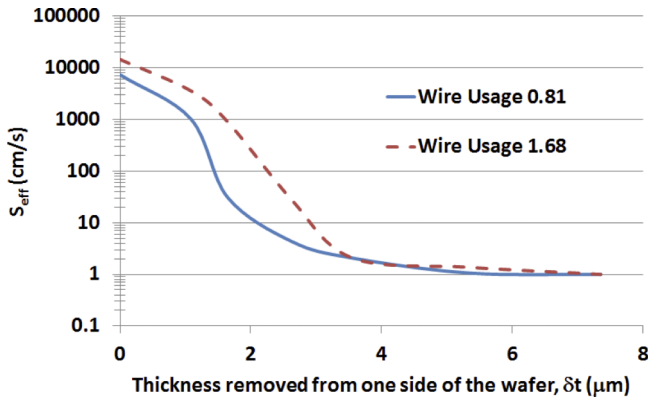

FIG. 8. Effective surface recombination velocity (S_{eff}) representing damage distributions corresponding to data of Fig. 7.

is related to the depth distribution of damage and can be represented as variation in the S_{eff}. From the data in Fig. 7, we can calculate S_{eff} as a function of depth, using Equation (1) (see, Fig. 8). It is seen that for WU = 0.8, S_{eff} is higher and stays above a value of 1 deeper below the surface. Here, S_{eff} = 1 corresponds to surface recombination of undamaged Si using our I-E passivation. These results show that reducing the wire consumption creates higher damage that also propagates deeper into the wafer. Because S_{eff} represents the total recombination of carriers in the damage layer below the surface, for a given δt, it is not a true damage distribution. To convert this into a true damage distribution, it is necessary to deconvolve S_{eff} using a detailed model that will be presented elsewhere.[16]

V. CONCLUSION/DISCUSSION

We have described a new technique for measurement of average damage depth and its in-depth distribution by sequentially etching thin layers from the Si wafer samples and making MCLT measurements after each etch step. The depth of damage is determined as the thickness removed that yields the peak MCLT. The τ_{eff} vs δt data are converted into S_{eff} vs δt plot that represents *integrated damage* below the surface. Although S_{eff} vs δt is not true damage vs δt, it can be converted into true damage distribution through a model that is described in a forthcoming paper.[16] We have also described 115-etch and the etching procedure, which allows very small thicknesses to be controllably etched from the PV wafer surfaces. Examples of changes in the damage depth caused by changes in some cutting parameters are given to illustrate the application of this technique. Although not discussed in this paper in detail, we have found that the surface damage determined by this technique compares very well with that of angle polishing and defect etching.

This technique yields more accurate and meaningful measurement of damage depth than any other technique available to us. Capability of making large-area (about 2-cm dia) MCLT measurement is particularly important for solar cell manufacturing because damage removal is typically done as a texture etching step, which is controlled by using average etch rate of large area wafers. The present technique also allows determination of in-depth distribution of surface damage. Although we have not presented any results in this paper, this technique applies equally well to multi-crystalline Si wafers.

ACKNOWLEDGMENTS

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