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Improvements to the solar cell efficiency and production yields of low-lifetime wafers with effective phosphorus gettering

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ABSTRACT

This research focuses on the improvement of solar cell efficiencies in low-lifetime wafers by implementing an appropriate gettering method of the diffusion process. The study also considers a reduction in the value of the reverse current at −12 V, an important electrical parameter related to the hot-spot heating of solar cells and modules, to improve the product's quality during commercial mass production. A practical solar cell production case study is examined to illustrate the use of the proposed method. The results of this case study indicate that variable-temperature gettering significantly improves solar cell efficiencies by 0.14% compared to constant-temperature methods when the wafer quality is poor. Moreover, this study finds that variable-temperature gettering raises production yields of low quality wafers by more than 30% by restraining the measurement value of the reverse current at −12 V during solar cell manufacturing.

1. Introduction

The photovoltaic industry has been undergoing rapid growth, with worldwide production of photovoltaic modules exceeding 20 GW in 2011 [1]. The key components driving the economic viability of solar power have been high-efficiency modules, highly productive manufacturing lines and low material costs. The majority of photovoltaic modules are now produced from multicrystalline silicon (mc-Si) solar cells. Therefore, low-cost wafers and high production volumes make mc-Si a promising material for use in low-cost, high-efficiency, and high-quality solar cells to fulfill the requirements for high efficiencies and product quality in solar modules [2]. However, mc-Si can contain high impurity concentrations and defects that affect the minor carrier's lifetime and limit the solar cell's performance [3]. In addition, a solar wafer contains large quantities of impurities and contaminant residues that can induce electrical failure and hot-spot heating [4].

Over the past two decades, research has focused on identifying impurity gettering methods for mc-Si solar cells, including boron gettering [5], aluminum gettering [6], and phosphorus gettering [7,8,9]. Phosphorus gettering (p-gettering) is known to enhance the removal of impurities, resulting in an increase in the minority carrier lifetime of solar-grade silicon. In addition, p-gettering does not add an extra step to the existing solar cell production process [10,11], a key requirement identified by previous researchers [12–16].

However, an extended single high-temperature gettering step suffers from thermal degradation, and has therefore been deemed unsuitable for improving gettering results [17]. A long gettering process time also leads to high residual impurity concentrations and is unsuitable for commercial mass production [8]. Plekhanov et al. [6] have proposed a numerical model of a variable-temperature gettering process using low-temperature gettering tails to shorten the required gettering time and achieve low residual impurity concentrations. Since the introduction of this variable-temperature gettering method, its strengths have been described extensively in the literature for applications that improve minor carrier lifetimes [18,19] and shorten the duration of the diffusion step, as required for commercial production [8]. This method has proven effective at reducing unwanted impurities, and has been introduced as a functional method to aid researchers in increasing the conversion efficiency of solar cells based on lifetime predictions [5]. Some researchers have evaluated this gettering effect using small samples [20].

Despite the large number of studies that have implemented variable-temperature p-gettering to improve the lifetimes of solar cells hindered by low-lifetime wafers, a practical solution for its commercial application has not yet been identified. Most research to date has incorporated only a few samples to illustrate the connection between wafer minor carrier lifetimes and mc-Si solar cell efficiency [2,19]. However, the quality of the mc-Si material is not a constant, but varies among suppliers and even from ingot to ingot when obtained from the same supplier [21]. Therefore, one cannot generalize the results obtained from a few samples to accurately describe all mc-Si material used in the processing of solar cells. From the literature review, it is apparent that there is limited

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research focusing on how to improve solar cell efficiency and quality in commercial solar cell production with p-gettering. The data in this study are gathered through mass-production data measurements and are therefore highly reliable.

The present study analyzes the strength of a variable-temperature p-gettering process, using wafers of differing quality, at improving solar cell efficiencies and production quality. Section 2 discusses the experimental details of a quantitative comparison of the enhanced solar cell efficiencies of wafers with varying quality, while Section 3 presents the experimental results and implications of the experimental analysis. The conclusion and future research directions are described in Section 4.

2. Experiment

This experiment is performed with p-type 180-μm-thick mc-Si wafers with an area of $12.6 \times 12.6\,cm^2$ and a resistivity of 0.5–3 Ωcm. It should be mentioned that before going forward to manufacture the solar cell, neither the removal of native oxide layer nor any cleaning procedure was applied.

2.1. Case study

The manufacturing at Gintech Energy Corporation, a solar cell manufacturing company in Taiwan, is investigated in this case study. The principal mass-production processing steps at this company and in the case study are shown in Fig. 1 and described below.

(1) Surface texturing: After sorting, the silicon wafer saw marks are eliminated and the wafer surfaces are rough-etched using acid. This processing step is normally used to create a textured surface that will reduce the total reflection of incident light and increase the wafer's efficiency.
(2) Phosphorus diffusion: Phosphorus gas is injected into the wafer in a high-temperature chamber to create electrical holes in the rich p-type silicon wafer's surface, which are then infiltrated with phosphorus to form an n-type area containing a greater quantity of electrons. This process is the so-called formation of a P–N junction for photovoltaic conversion effects. The phosphorous diffusion is performed in a quartz tube furnace using $POCl_3$ and O_2. During the high temperature diffusion process, $POCl_3$ could be decomposed to PCl_5 which is highly corrosive and cause damage to the wafer surface. Therefore, O_2 is induced to react with PCl_5 to form P_2O_5 and reduce the PCl_5 as much as possible. The typical thickness of oxidation layer and phosphorous gettering layer is about 30 and 200 nm, respectively; both of these layers were removed by hydrofluoric acid (HF) after.
(3) Phosphorus glass etching: During the phosphorus diffusion process, silica-phosphate glasses on the outer surface of the wafers are created. The silica-phosphate glasses must be removed with HF washing to continue follow-up solar cell process.
(4) Plasma-enhanced chemical vapor deposition (PECVD): The interaction of silane and ammonia in the vacuum furnace of a PECVD system can create a thin silicon nitride SiN_x:H layer that serves as an antireflection coating. In addition to its optical benefits, this dielectric coating can improve the electrical properties of the cell by surface passivation. The deposition occurs at temperatures of approximately 400 °C.
(5) Screen printing: A conductive paste of silver and aluminum is used to screen print thin and thick electrodes onto both surfaces of the wafer. This process includes three steps: printing of the front sides, printing of the thick electrode, and using the aluminum paste to print the remaining area on the reverse side. Between each printing step, the wafer must pass through the drying furnace (200 °C for 9 min) and optical testing system to confirm that the screen printing details and positioning are correct.
(6) Rapid sintering: Once the metal paste has gone through the screen printing and drying steps, it is rapidly sintered to penetrate the silicon nitride coating on its front and infiltrate the wafer's surface binding tightly to conduct the electrical current. A full aluminum layer printed on the back of the cell, with subsequent alloying via firing, in a belt furnace with a set peak temperature of 920 °C and a belt velocity of 6 m/min, produces a back-surface field (BSF) and improves the cell bulk.
(7) Edge isolation: The front side of a solar cell made from a p-type silicon wafer is negative (−) and the back is positive (+). A notch, deeper than the P–N junction on the wafer's edge, is cut using laser dicing to avoid a short circuit between the positive and negative sides. This process can also be performed during the plasma treatment and chemical etching stages.
(8) Performance testing and classification: Once the appearances of the wafer's front and back surfaces are examined, its photovoltaic conversion efficiency and other electrical characteristics are measured using automatic testing equipment. The samples used for cell analysis are measured in the solar simulator under $100\,mW/cm^2$ (AM 1.5) illumination, and the electrical performance and conversion efficiency of the solar cell are simulated by measuring the power output under a Berger flash system with AAA-class spectrum, uniformity, and temporal stability. After performance testing, the cell sorter typically classifies the products based on cosmetic and electrical parameters and sorts them into different product grades and cell stacks.

2.2. Experimental scheme

The proposed experimental scheme in this study is shown in Fig. 2.

2.2.1. Wafer sorting according to lifetime characteristics

Prior to processing, the wafers are sorted using a wafer inspection system (WIS), which separates wafers with varying lifetime specifications using a micro-photoconductivity decay (μ-PCD) method. The wafer sorting process typically classifies the incoming wafers based on parameters such as material lifetime, resistivity, microcracks, and others, and sorts them into different cell stacks.

The mc-Si wafers used in this study are provided by two different suppliers, S_A and S_B. Wafers from the first supplier, S_A, are made from high-quality ingot and their base minority carrier lifetimes are greater than 1.4 μs. Parts of the wafers from the second supplier, S_B, do not meet the cell manufacturer's quality specifications, which require minority carrier lifetimes of at least 0.8 μs. The results of the mass production of the wafers provided by suppliers S_A and S_B are shown in Table 1.

Table 1 defines five product categories. A-grade solar cells are prime flawless solar cells, while B-grade cells are solar cells containing visual flaws that do not affect the power. C-grade solar cells are those with flaws that affect the power output, so the output conversion efficiency is less than 12.5% for whatever reason. R-grade solar cells are those with flaws that affect the measured R_{sh} values, so the output R_{sh} is lower than 10 Ω for whatever reason, while I-grade solar cells are those with flaws that affect the measured reverse current at −12 V ($Irev_2$), so the output $Irev_2$ is greater than 2.5 A. The production yield is equal to the ratio of A-grade cells to other cells. The other product grades are generally considered scrap.

As shown in Table 1, the solar cells mass produced from the S_B wafers exhibit lower efficiencies than the cells produced from S_A wafers, with results typically approximately 0.33% lower. Moreover, the ratio of A-grade products from the S_A wafers is significantly higher than that from the S_B wafers due to failure of the

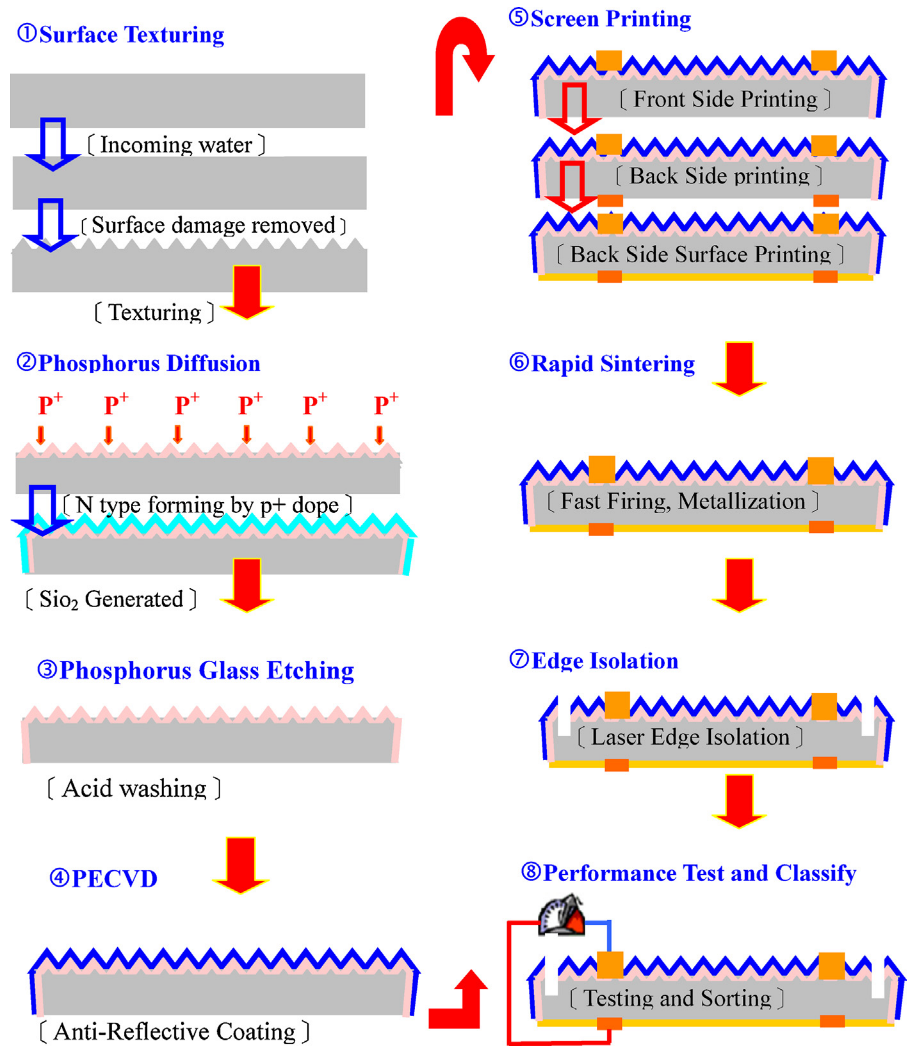

Fig. 1. Commercial mc-Si solar cell processing steps.

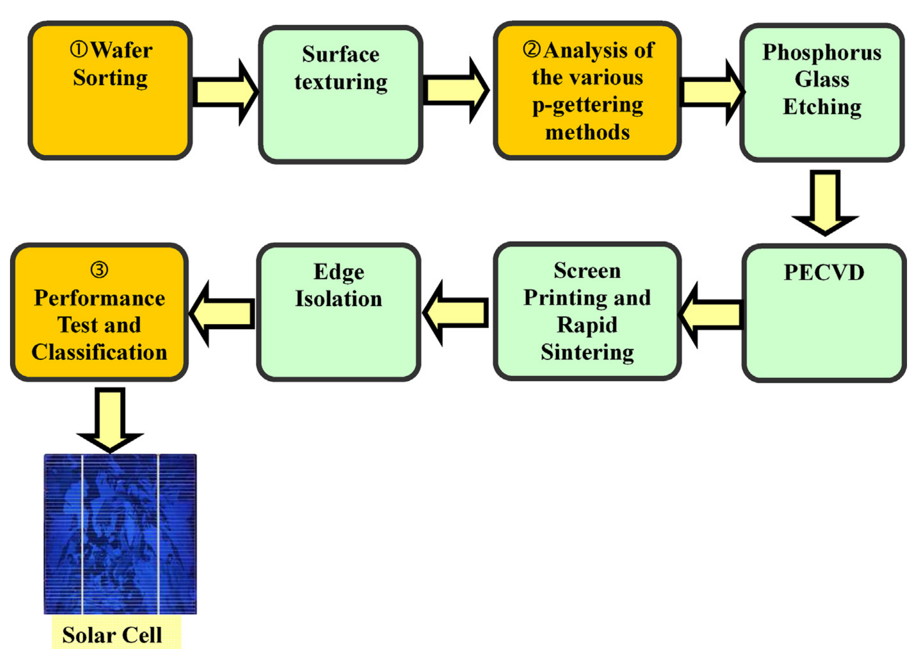

Fig. 2. Proposed experimental scheme.

Table 1
Mass production results for wafers provided by suppliers S_A and S_B.

Parameter	Parameter description	Supplier	
		S_A	S_B
η (%)	Mean solar cell conversion efficiency	16.38	16.05
Q'ty	Number of measurement data	47,481	57,762
I_{sc} (A)	Short circuit current	5.379	5.284
V_{oc} (V)	Open circuit voltage	0.622	0.618
FF (%)	Fill factor	77.56	77.96
$Irev_2$ (A)	Reverse current at −12 V	0.188	0.671
R_s (mΩ)	Series resistance of solar cell	3.909	4.089
R_{sh} (Ω)	Shunt resistance of solar cell	179.51	109.85
A-grade (%)	Ratio of A-grade products quantity	99.66	94.48
B-grade (%)	Ratio of B-grade products quantity	0.01	0.07
C-grade (%)	Ratio of C-grade products quantity	0.13	0.86
R-grade (%)	Ratio of R-grade products quantity	0.19	0.64
I-grade (%)	Ratio of I-grade products quantity	0.01	3.95

I-grade ratio and the $Irev_2$ of the S_A wafer, which is significantly lower than that of the S_B wafer. The efficiency percentage of a solar cell η can be written as follows:

$$\eta = \frac{P_{\max}}{P_{in}} = \frac{I_{SC} \times V_{OC} \times FF}{1000 \times C_r} \quad (1)$$

in which $P_{\max}$ is the maximum output power of the solar cell and P_{in} is the incident optical power as defined by the measured relevant area with respect to a reference cell, C_r. The value of C_r is 0.015849 m^2. In this case study, the uncertainties of η (%), I_{sc} (A), V_{oc} (V), and FF (%) in the Berger flash system measurements are controlled within 0.05%, 0.08 A, 0.002 V, and 0.5%, respectively, during the production period.

2.2.2. Analysis of various p-gettering methods

This study utilizes two distinct temperature profiles, shown in Fig. 3, to investigate how varying the p-gettering method affects both the wafer quality and the conversion efficiency of a mc-Si solar cell.

This experiment uses the original diffusion/gettering process with constant-temperature profiles and a 61-min process time as the reference scenario, denoted as p_1. A fine-tuned p-gettering process, denoted as p_2, extend the low-temperature tail based on an optimized reduced process time with improved efficiency. This study implements a design of experimental method by setting the duration of the process, the temperature in the furnace, the gas flows (O_2, N_2, N_2 carrying $POCl_3$), and the vacuum pressure to achieve optimized efficiency. In addition, the total process time required for a p_2 recipe is 84 min, which is shorter than that of a previous study that requires 2.5 h [8]. All wafers have a target sheet resistance of 65 Ω/square.

2.2.3. Performance testing and classification

The quality of the mc-Si solar cells is determined by the cell's electrical parameters following the performance testing. In the photovoltaic industry, the end users-module makers are concerned mainly with obtaining both high conversion efficiency and high-quality mc-Si solar cells with low-cost materials such as low-lifetime mc-Si wafers. Thus this study is focused on the electrical performance results given by the Berger flash instrument, e.g. η, I_{sc}, V_{oc}, $Irev_2$, etc., to optimize the p-gettering method. Especially, $Irev_2$ is the implicit electrical parameter, by which wafers with higher Fe concentrations and possible inducing hot-spot heating [4] could be checked. It is expected that with appropriate gettering methods, Fe concentration in these low-lifetime wafers could be reduced to a very low value that not limits the bulk lifetime and the solar cell efficiency.

Table 2
Minority carrier lifetime results by wafer type tested.

Sample code	Tested Q'ty	Lifetime	
		Average (µs)	Ratio of test samples
A_1	31,579	1.41	46.97%
B_1	28,295	1.16	42.09%
B_2	3415	0.99	5.08%
B_3	3940	0.57	5.86%

3. Experimental results and discussion

This section examines the proposed experimental scheme in Section 2 to compare the results of the two p-gettering methods under study.

3.1. Experimental results

3.1.1. Wafer sorting according to lifetime characteristics

The experiment explores four types of wafers supplied by companies S_A and S_B, and encompass most of the minority carrier lifetime categories for wafer quality, including lifetimes longer than 0.8 µs (denoted as A_1 when supplied by S_A and B_1 when supplied by S_B), lifetimes shorter than 0.8 µs (denoted as B_2 when supplied by S_B), and lifetime variations among wafers greater than 0.6 µs (denoted as B_3 when supplied by S_B). The lifetime variation is represented by $\Phi_{lt}(i)$, as shown in the following equations:

$$\tau_i^+ = \max_i \left\{\tau_{i1},\ \tau_{i2},\ \ldots,\ \tau_{ij},\ \ldots,\ \tau_{in}\right\}\ i = 1,\ 2,\ \ldots,\ m;\ j = 1,\ 2,\ \ldots,\ n$$

$$\tau_i^- = \min_i \left\{\tau_{i1},\ \tau_{i2},\ \ldots,\ \tau_{ij},\ \ldots,\ \tau_{in}\right\}\ i = 1,\ 2,\ \ldots,\ m;\ j = 1,\ 2,\ \ldots,\ n$$

$$\Phi_{lt}(i) = \tau_i^+ - \tau_i^- \quad (2)$$

Thus, the lifetime value (τ_{ij}, $i = 1, 2, \ldots, m$; $j = 1, 2, \ldots, n$) indicates the jth lifetime measurement in a data set containing a total of n points per sample with respect to the ith sample, for which m samples are consistent with the values provided in Table 1. The variables τ_i^+ and τ_i^- represent the maximum and minimum lifetime values of the ith samples, respectively, and the isolation of the ith sample's lifetime is represented as $\Phi_{lt}(i)$. Table 2 summarizes the results sorted according to lifetime specifications for the incoming wafers.

These results indicate that the lifetimes are significantly higher for the A_1 wafers than for the lower quality B_1, B_2, and B_3 wafers supplied by S_B. Sets of various wafers are used to compare the effectiveness of the p-gettering methods.

3.1.2. Analysis of the various p-gettering methods under study

Wafers produced with various gettering methods are used in the same solar cell production process to avoid the effects of other parameters. Therefore, differences in the wafer after processing can be interpreted as a function of the different gettering processes and are not dependent on the wafer characteristic.

3.1.3. Performance testing and classification

A small quantity of abnormal experimental data obtained during a laboratory process can affect the quality of all measured results when determining gettering effectiveness. Therefore, the measured gettering efficiencies are assumed to be unaffected by wafer conditions when acquiring mass production data with which to compare different p-gettering methods. As shown in Table 2, each sample code quantity represents over a thousand wafer pieces.

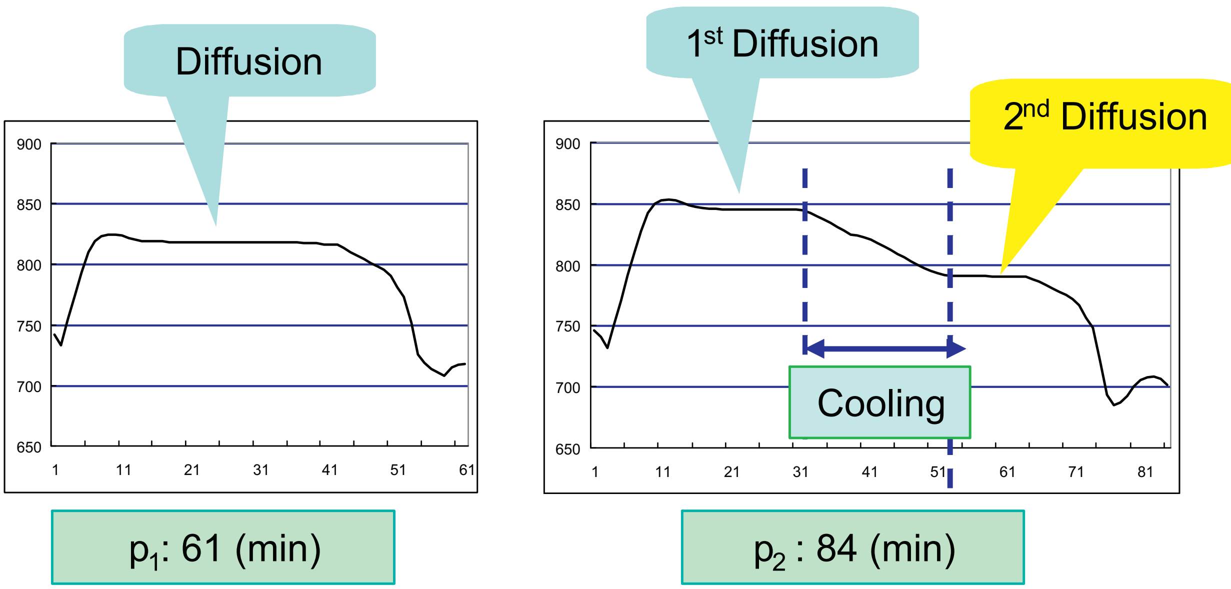

Fig. 3. Schematic of the two different temperature profiles used in this study.

3.2. Discussion

The average values for the electrical characteristics of solar cells made from each sample code with various gettering methods are shown in Table 3.

The statistical data indicate that the highest mean value of the solar cell efficiency, A_1, is 16.41% with p_1 gettering, and the cell efficiency of B_3 with p_1 has a minimum mean value of 15.92%. The average cell efficiency gain from p_2 gettering exhibits a minimum 0.08% increase over that of p_1 for each sample code for S_B wafers. There is sufficient evidence to prove that the p_2 gettering method is more efficient at improving a low-lifetime material (B_2 and B_3 wafers) than an improved starting material (A_1 and B_1 wafers). The cell efficiency can be improved up to 0.14% on B_3 wafers with the lowest minority carrier lifetime. The fact that the p_2 gettering method fails to improve the performance of A_1 wafer may be the evidence that side effects of thermal degradation can overcome the benefit of gettering effects, as has been proposed by Macdonald and Cuevas [17]. In addition, the p_2 gettering method can maintain a lower $Irev_2$ value than the p_1 gettering on S_B wafers. This result

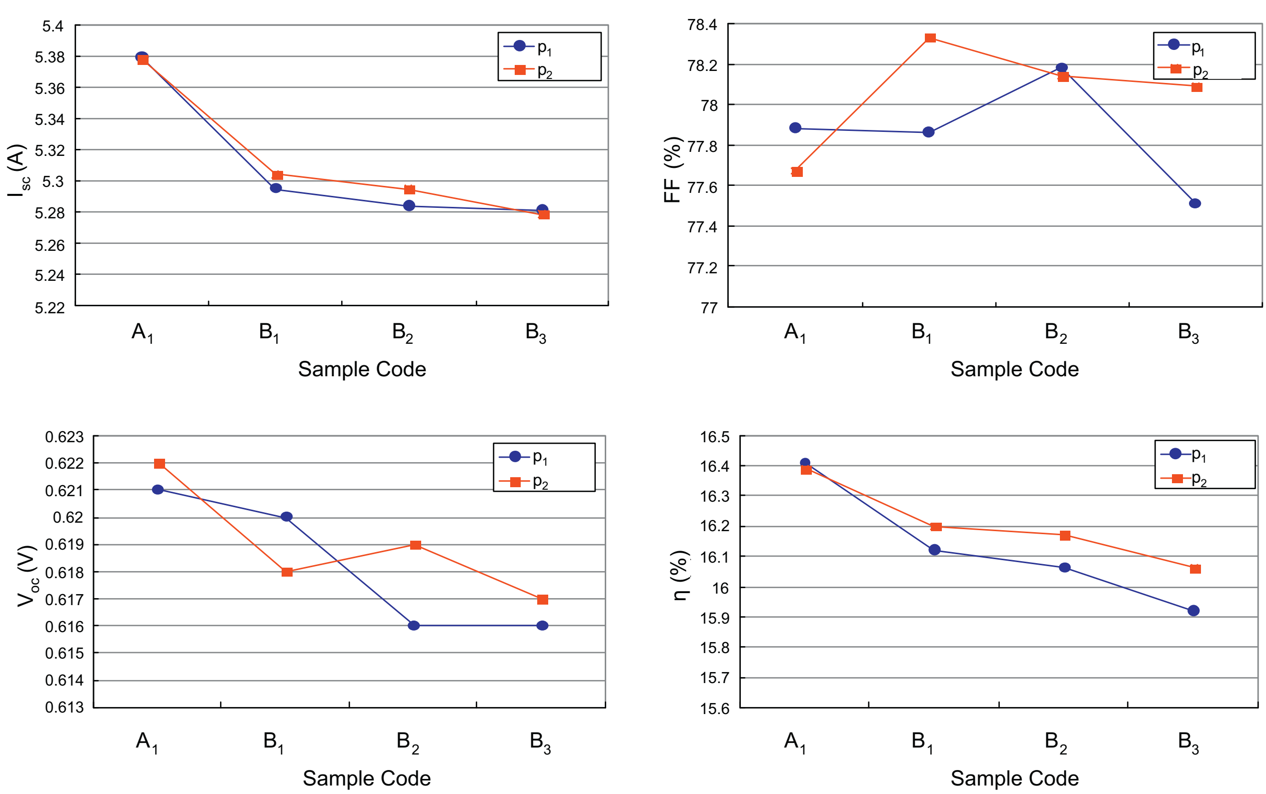

Fig. 4. Comparison of the solar cell electrical data measured for each sample code.

Table 3
Comparison of the electrical characteristics of solar cells made using various gettering methods.

Supplier	Sample code	Gettering method	Measured cell parameters						
			I_{sc} (A)	V_{oc} (V)	*FF* (%)	R_s (Ω-cm²)	R_{sh} (kΩ-cm²)	$Irev_2$ (A)	η (%)
S_A	A_1	p_1	5.379	0.621	77.88	3.783	187.9	0.167	16.41
		p_2	5.378	0.622	77.67	3.629	182.1	0.178	16.39
S_B	B_1	p_1	5.295	0.620	77.86	4.015	109.9	0.407	16.12
		p_2	5.304	0.618	78.33	3.828	110.2	0.329	16.20
	B_2	p_1	5.284	0.616	78.18	3.690	119.2	0.608	16.06
		p_2	5.295	0.619	78.14	3.886	93.5	0.301	16.17
	B_3	p_1	5.281	0.616	77.51	4.125	69.6	0.859	15.92
		p_2	5.279	0.617	78.09	3.786	103.5	0.584	16.06

Table 4
Comparison of the output ratio of each product grade made with various gettering methods.

Supplier	Sample code	Gettering method	Output ratio of each grade of product					
			Q'ty	B-grade (%)	C-grade (%)	R-grade (%)	I-grade (%)	A-grade (%)
S_A	A_1	p_1	15,771	0.03	0.06	0.10	0.03	99.79
		p_2	15,732	0.01	0.24	0.19	0.01	99.54
S_B	B_1	p_1	14,029	0.02	0.19	0.56	0.62	98.61
		p_2	14,078	0.13	0.07	0.48	0.43	98.88
	B_2	p_1	1703	0.06	0.70	1.17	1.35	96.71
		p_2	1698	0.06	0.41	0.47	0.41	98.65
	B_3	p_1	1942	0.21	4.22	1.44	28.84	65.29
		p_2	1984	0.10	1.01	0.30	1.71	96.88

should not be ignored because the criterion can affect solar cell production yield.

Table 4 shows the mean values of each product grade's output ratio when produced with the various gettering methods reported herein. These materials are originally divided into equal quantities after being obtained from different experiments, but scrap quantities due to production breakage must be deducted. The results indicate that S_A wafers maintain a higher A-grade output percentage than S_B wafers. The average decrease in the quality of S_B wafers is considered as a ratio of I-grade cells, which is much greater than that of S_A wafers. In addition to the ratio of I-grade cells, which are outside the specification limits, the primary defect in S_B wafers consists of C-grade and R-grade cells. When the p_2 method used on S_B wafers is compared to those produced with p_1, the latter exhibit more low-quality products with greater C-grade, R-grade, and I-grade output ratios. With the use of better starting materials (A_1 and B_1 wafers), the defect gap in the low-quality output between the different gettering methods can decrease. A comparison of the C-grade, R-grade, and I-grade output ratios with respect to B_2 and B_3 wafers indicates that p_2 gettering is superior to p_1. Tables 3 and 4 also provide a comparison of different gettering methods in B_3 wafers, indicating that p_2 gettering can significantly reduce the proportion of low-quality products by restraining the $Irev_2$ value. Hence the A-grade output ratio is improved from 65.29% to 96.88%, by which the production yield is raised by more than 30%. A previous study has revealed that p_1 cannot effectively remove the high quantities of impurities and contaminant residues that are induced by electrical failure and hot-spot heating [4,22].

The results shown in both Tables 3 and 4 indicate that compared with the p_1 method, the p_2 method can produce a higher A-grade wafer ratio with S_B wafers while maintaining a lower diffusion throughput. In the high-quality wafer scenario with the S_A wafers, the optimum solution requires the use of the p_1 method, but the p_2 method which cannot produce a higher A-grade ratio, is also acceptable. Thus, these mass-production results confirm the importance and effectiveness of variable-temperature gettering at improving solar cells made from low-lifetime wafers.

A comparison of the electrical data for I_{sc}, V_{oc} and *FF* indicates that none of these factors are strongly affected by p_1 and p_2, as illustrated in Fig. 4. A comparison of the solar cell efficiency indicates a dramatic shift in the effect of the p_1 and p_2 methods depending on the wafer source.

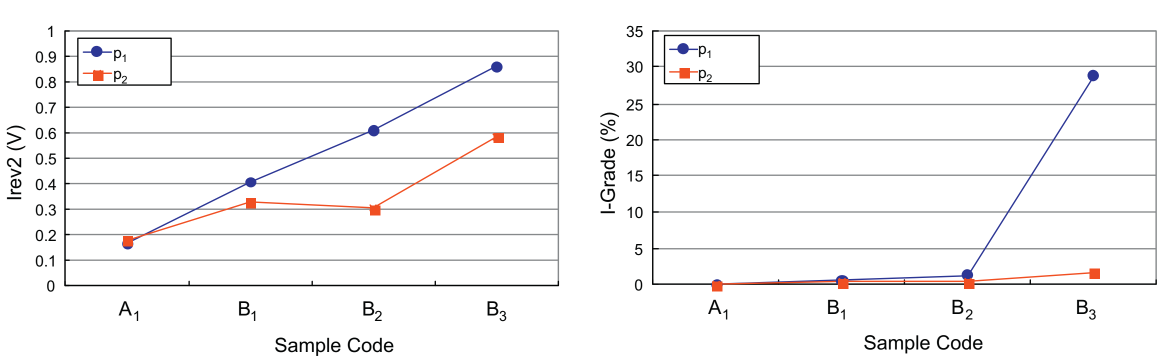

Fig. 5. Comparison of the solar cell $Irev_2$ data measured for each sample code.

Fig. 5 compares the mean $Irev_2$ values for each sample code. When using p_1 gettering, the $Irev_2$ values and the I-grade ratios are worse for wafers of poor initial quality. Wafers from source B_3, in particular, exhibit I-grade ratios dramatically higher than the others. In contrast, the p_2 gettering method effectively restrains the I-grade ratios and reduces the mean values of the $Irev_2$ data.

4. Conclusions and future research opportunities

The goal of this research is to define an effective gettering method that would improve the electrical performance and mass-production output results of solar cells. This study proposes a variable-temperature gettering method to solve the problems of low efficiency and poor quality that arise from the application of low cost but also low-lifetime wafers. Although the improvement of cell efficiency by 0.14% on the low-lifetime wafer is not a huge number comparing to other researches [2,22], it is substantive to the solar energy industry that could effectively increase the conversion efficiency of crystalline-Si cell products while further reduce the production cost with the capability of using low-quality wafers. The mass production data measurements gathered by this study provide reliable conclusion for a concrete technology scenario in commercial solar cells. Moreover, the proposed gettering method is based on an existing diffusion process that does not introduce extra equipment to the cell manufacture process. Thus the actual efficiency improvement proved in this study is meaningful to cell manufacturers and helpful to wafer makers to sustain their continuous efforts on the development of low-cost production approaches, which is always an universal tough issue to all of the alternative energy enterprises as competing with conventional fossil fuel energy.

A number of conclusions can be drawn by analyzing the results. First, variable-temperature gettering can significantly improve solar cell electrical performance when the wafer quality is poor. Second, high-quality wafers need not be used for effective variable-temperature gettering. Third, the proposed gettering method can maintain a lower $Irev_2$ value on low-lifetime wafers. This result should not be ignored because there are certain criteria of $Irev_2$ for commercial solar cells. Solar cells with higher $Irev_2$ beyond the specification criterion are considered unqualified products, which is harmful to the yield of solar cell production. Finally, this study concludes that variable-temperature gettering not only improves solar cell efficiency but also significantly improves production yields by restraining the $Irev_2$ value during mass production.

The limitation of the proposed research for the lifetime measurement after diffusion process requires removing both emitter and passivating surfaces. The linking mechanism between the accuracy of lifetime improvement after diffusion process and the results of cell performance has the potential to improve solar cell industry. This will become the direction of future research.

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